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Toward 5G Software Defined Radio Receiver Front-Ends

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To my family

Motto: Simplicity is complexity resolved

Constantin Brincusi

Foreword

The first GSM telephone conversation took place in July 1991. This achievement was the result of a herculean R&D collaboration between major telecom industry manufacturers from 13 European countries. And it took us 10 years to develop. The task was huge, involving various engineering disciplines for defining the network architecture, protocols, modulation schemes, and digital signal processing algorithms, for designing integrated circuits, and for organizing the handover between different telecom operators. And all this happened in a political context with conflicting national interests and language barriers.

And yet, looking in retrospect, GSM was relatively easy. It involved only one type of modulation (GMSK) and only one multiplexing scheme (TDMA). Initially, there was only one frequency band allocated for this new communications medium (around 900 MHz), and all communications used the same channel bandwidth (200 kHz).

By the time that the GSM technology became mature and the sales figures reached their height, the successor technology was already available: In 2001, exactly 10 years after the GSM launch, the first 3G networks came into operation. The new technology offered a 30-fold data rate increase, compared with the original GSM technology. Therefore, it came just at the right moment to grasp the wave of Internet explosion. And again, it took us 9 years of R&D efforts to develop. But by that time, European manufacturers had already lost their lead to companies in the USA and Far East.

The 3G air interface is less "unified" than its 2G counterpart: although the 3GPP standard clearly defines the channels (5 MHz) and the modulation scheme (WCDMA), there are 31 frequency bands ranging from 850 MHz to 3.5 GHz. This renders the design of a radio front end more complex and calls for some "programmability" of the radio center frequency.

After 3G came 4G: in response to customer demand for increasing data rates, a new radio technology was introduced, based on orthogonal frequency-division modulation. Although, initially, there were two competing standards named WiMax (introduced for the first time by Sprint in 2007 and heavily backed by Intel) and LTE (backed by the 3GPP consortium and implemented in a commercial phone for the first time in 2011), only the LTE system survived. And again, 10 years of R&D efforts passed between the first WiMax specification and the first LTE phone.

From a radio front-end perspective, LTE is even less unified: not only are there more than 20 frequency bands allocated, the channel bandwidth itself can vary according to the needs of the customer and to the signal-to-noise ratio of the radio channel. This calls for programmability of the cutoff frequencies of all filters in radio receiver and transmitter.

I know that it starts to be boring, but after 4G comes 5G: resulting from the ever-increasing need for higher-speed data communications and more network capacity (to serve the Internet of Everything), it is forecasted that the 4G networks will run out of steam. If we extrapolate the history (2G in 1991, 3G in 2001, 4G in 2011), 5G would arrive in 2021. And again from a historical extrapolation, it will take us 10 years of R&D efforts to develop it. Hence, by now, we should be very busy designing integrated circuits for this new technology. But unfortunately, this is not the reality. At present, it is unclear what 5G will be. It is unclear what user scenarios will be served. It is unclear what modulation schemes, what antenna techniques, what radio frequencies, or what bandwidths will be used. However, one thing is certain: 5G will not exploit a single air interface. It will be a combination of multiple standards, to be used for different user scenarios and for different network conditions. One might expect a combination of low-power standards such as ZigBee for low-rate applications (e.g., readout of electricity meters or other sensor interfaces), of millimeter-wave high-bandwidth radio standards exploiting multiple-antenna technologies for high-speed data communications in urban areas, of dedicated radio technologies for communications between cars or between wearable devices, and of legacy backup technologies for rural areas where the cost of new deployments is not justified. Furthermore, since radio spectrum is scarce, there will be no unique worldwide frequency band available. Hence, the number of different allocated frequency bands can only increase.

Another lesson from history shows us that customers want the benefits from new technologies, *at zero additional cost*. For an early-adopter 5G phone, cost will be less important. But in time, it will be of prime importance that we are able to build such a complex multi-standard 5G phone in a cost-effective way. Therefore, it will be necessary that multiple communications protocols share the same radio receiver and transmitter circuits.

As a result, for the first time, 5G will require programmability, not only of the radio center frequency and the channel bandwidth but also *of the modulation*

scheme itself. This means that the circuits will have to allow for varying, under software control, of such aspects as the signal gain partitioning, the filter roll-off, the selectivity, the transmitter out-of-band noise, and, most important, the power consumption.

This book therefore arrives exactly in time.

Leuven, Belgium, 2016

Dr. Frank Op 't Eynde
RFIC consultant

Preface

The advent of wireless communications of the last decades has spun an exponential increase in the number of users, hardware, and data rates. On the brink of the fifth wave of wireless system development (5G), it is forecasted that the world will become even more interconnected at ever-growing speeds. The radio front-end circuit designer needs to be prepared to handle this imminent wave. This translates to the designer being ready to interpret quickly any wireless standard.

This book brings to light a new approach aimed at finding the optimal design path for next-gen software-defined radio receiver front-ends (SDRXs): a standard-independent structured design methodology, which is setting the receiver architecture and electrical specifications and meets the submicron CMOS transistor-level implementation constraints that drive the topologies of the SDRX building blocks.

In my opinion, in today's design world, the main design challenges reside at system level, as significant progress has been made to improve the key RF and mixed-signal circuits performance.

First, I find a lack of a systematic approach in the system-level analysis of SDRXs and create a standard-independent, systematic methodology to help derive the receiver key electrical specifications. The novelty consists in the fact that the developed methodology empowers the designer to tackle the multi-standard environment in a parallel way rather than serially, as is the case with previous published works. This is a critical feature for any design methodology targeting 5G circuits and systems. The methodology is based on manual analysis that suits best an intuitive understanding, as this is the most efficient way for a designer to have the grasp on the design process.

Throughout the book, the SDRX design follows the key wireless standards of the moment (i.e., GSM, WCDMA, LTE, Bluetooth, WLAN), since a receiver compatible with these standards is the most likely candidate for the first design iteration in a 5G deployment. Thus, a multi-standard SDRX is constructed. Due to the newly developed standard-independent system-driven design methodology, the designer is enabled to handle efficiently the large amount of information provided in the wireless standards and to remain in control of the system being designed. Moreover,

this methodology has the advantage in that it can be used very effectively in the case of the new, soon-to-be-developed, wireless standards of the 5G wave.

Hence it is shown that direct conversion architecture is the most suited choice for the SDRX. Further on, I demonstrate the fundamental choice the designer has to make is the optimal channel selection: how much of the blockers/interferers will be filtered in the analog domain and how much will remain to be filtered in the digital domain. Also this opened the path for the novel "smart" gain−noise−linearity partitioning tailored toward SDRXs that optimally leverages the extreme reception conditions specific to the wireless environment.

With the new analysis methodology, this book lays down a concept in creating standardized tools for tomorrow's SDRX designers. Basically, these tools represent the compass used to explore the SDRX domain map.

The introduction of the new and efficient tool *the generic blockers diagram*, together with the newly defined figure of merit (FOM) FOM_{CHS}, enabled the proper evaluation of the key trade-off that shapes the receiver design: the trade-off between the receiver low pass filter (LPF) area and its analog-to-digital converter (ADC) power consumption; thus, the optimum filter partitioning between the SDRX baseband analog LPF and the digital filter following the ADC is found in one single plot.

One of the key features of the developed system-level analysis is that the direct sampling architecture is treated as a particular case of mixer-based direct conversion architecture. Thus, given a power consumption budget, one can evaluate specifically, by considering the ADC performance characteristics and the corresponding blocker diagram, how much filtering is required on the receive path.

Finally, I would like to take this opportunity to acknowledge Dr. Frank Op't Eynde for our countless technical discussions that consolidated the research revealed in this book and Dr. Klaas Bult for his always-present insightful technical observations that were of great aid in understanding the art of IC design. Also I would like to express my sincere gratitude to my Ph.D. advisor and mentor Prof. Mircea Bodea.

Tustin, CA Silvian Spiridon

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Chapter 1
Overview of Wireless Communication in the Internet Age

1.1 Software Defined Radios

Communication is an intrinsic part of the human nature. Through communication information is conveyed. The simplest model of a communication system requires the presence of a transmitter and a receiver. The communication process takes place between receiver(s) and transmitter(s) over the communication medium or channel.

The first communication system, in a relaxed interpretation, was the postal service. The first well-documented postal service was organized in Rome during the times of Augustus Cesar, around 50 BC. The common information conveyed through this service were letters, and given the high service cost and the low level of literacy, only few people could make use of it. Since then its evolution was fairly slow, as the service was based on the horse powered couriers for almost two millennia.

It wasn't until late nineteenth century when a real breakthrough happened: the invention of the telegraph by Carl Friedrich Gauss and Wilhelm Weber in 1833. The telegraph allowed long distance communications through copper wires, giving birth to the terminology of wired communications. By 1866, the telegraph had opened the era of instant transatlantic communication that would shape the century to come.

The next important milestone in the communication history is the patent awarded to Alexander Graham Bell for the electric telephone by the United States Patent and Trademark Office (USPTO) in March 1876. This milestone represents the birth date of the fixed telephony service. Since then the service expanded continuously to peak at about 19 fixed telephone lines per 100 inhabitants in 2006, see Fig. 1.1 [1].

Following the experiments of Hertz, which targeted to prove Maxwell's equations, Gugliemo Marconi has managed to develop a wireless telegraph system by 1895, opening the realm of wireless communications. In 1909, he was awarded the Nobel Prize, shared with Karl Ferdinand Braun, in recognition of his contributions to the development of wireless telegraphy.

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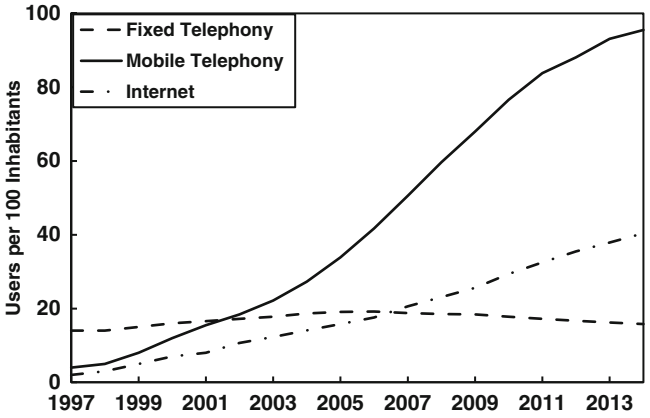

Fig. 1.1 Internet usage—the driving force behind the need for SDRs

Originally radio communications served mainly military and broadcasting services. It was until 1973, when the first hand-held wireless devices were available for the large public.

Moving closer to present times, if in the beginning of the twentieth century, the analog fixed telephony was just introduced, by the end of the same century the wireless revolution conquered the planet. By the beginning of the year 2015, the mobile telephony growth reached an astonishing peak of 96 subscribers per 100 inhabitants worldwide [1].

Two very important milestones for the development of the communication sector were the invention of what is known today as the "Internet" in 1969 in the USA, and the development of the Personal Computer (PC). The PC was also introduced for the first time in the USA by Apple in 1976. By allowing all PCs to be connected into a world wide web, the Internet opened the market for broad-band personal connections.

The Internet foundations were laid in 1960s by the USA military research projects aimed at building distributed computer networks. The internet mass global spread was delayed due to lack of networking infrastructure and limited number of PC users. However, in mid-1980s the PC market boomed due to IBMs Personal Computer based on Intel 80286 microprocessor and operated by Microsoft's Disk Operating System (MS-DOS). This combination formed the template for all PC developers and vendors. Hence, during the 1990s, it was estimated that the number of Internet users doubled each year, with a brief period of explosive growth in 1996 and 1997. By end of 2014, the Internet reached about 41 users per 100 inhabitants worldwide, see Fig. 1.1 [1].

In order to show the strong relation between the IT industry and the communication sector, Fig. 1.1 plots the number of worldwide subscribers of fixed and mobile telephone networks and Internet users. The Internet access connects the two sectors.

In the early 1990s, the Internet used the long established fixed telephony infrastructure to reach the large audience. The latest trends show the communication sector is strongly going mobile, as today the mobile subscribers number surpasses the fixed telephony one by a factor of more than 5. This translated to the development of a market of mobile personal broad-band Internet access perfectly suited for the new set of electronic equipment, the "smart" mobile phone.

1.1.1 Digital Communications of the Internet Age

All the communication systems developed in the last two centuries are based on Maxwell's equations [2]. The information is conveyed through the medium, either wired or wireless, in the form of electromagnetic waves or photons.

The Figure of Merit (FOM) for the information transfer is the data rate, defined as the amount of conveyed information divided by the amount of time required for it to be transferred between participants.

In 1949, Claude Shannon has calculated the maximum capacity, or data rate, of a communication channel characterized by Gaussian noise (N) as a function of its bandwidth (BW) and of the signal power (S) at the receive side [3]:

$$Channel\ \ Maximum\ \ Data\ \ Rate = BW\log_2\left(1+\frac{S}{N}\right) \tag{1.1}$$

Equation (1.1) comprises the key trade-off in digital communications: the trade-off between Signal-to-Noise Ratio (SNR) and channel bandwidth, or equivalently, between the modulation scheme complexity and BW. In the last 50 years the need of faster and faster Internet access led to the continuous increase in the maximum data rate, as detailed in this section.

The increase of the communication data rate was driven by: (a) the increase in bandwidth (if and where it was possible) and (b) the increase in the modulation scheme complexity.

The Internet was initially developed as a "wired" network. There are four ways to get Internet access through a wired network, depending on the infrastructure available:

- Using fixed telephony network
- Through the cable TV infrastructure
- Via the power lines
- Optical fiber

The third option, although available in a large number of countries, is not so popular at present, due to the very hostile signal perturbations and impedance variations present on the medium.

The evolution of the most popular Internet access methods over a wired copper cable over the past 20 years is presented in Fig. 1.2.

Given the latest trends revealed by Fig. 1.1, mobile Internet access became available. In the *wireless* communication sector, the most popular standard is by far the Global System for Mobile Communications or GSM [4] as it is estimated that 80 % of the global market uses the standard. The first GSM standard has been introduced in 1990 and by the end of 1993 over a million subscribers were using GSM networks being operated by 70 carriers across 48 countries; in 2011, about 1.5 billion people across more than 212 countries and territories are using a mobile terminal under the GSM standard.

GSM is a long-range standard based on a cellular network architecture, with a cell having a maximum coverage range of 120 km. GSM represents the second generation (2G) wireless telephone technology, as its communication frame is digital as opposed to the first generation (1G) networks which implemented analog communication. Alongside the main voice service, due to the digital nature of its communication frame, GSM introduced the low-cost alternative of the Short Messaging Service (SMS). The Internet could be accessed over GSM networks through an equivalent dial-up service. Though, low data rates were possible (max. 9.6 kbit/s) as only one communication channel could have been used. Nevertheless, the information technology revolution empowered by the Internet expansion led to the extension of GSM to allow simultaneous voice and data communications and higher data transfer rates: in 1997, the General Packet Radio Service (GPRS) has been introduced and provided data rates of 56–114 kbps. GPRS consists in allocating more than one of the multiplexed time slots for a given communication. The embedding of GPRS into a 2G GSM network represented an intermediate step (2.5G) before the third generation (3G) wireless network. By 1999, even higher data rates could be achieved as Enhanced Data Rates for GSM Evolution (EDGE) GSM extension (2.75G) was able to allow 180 kbps. EDGE is an extension of GPRS whereby the classical 1-bit-per-symbol GMSK modulation is replaced by an 8-phase modulation scheme.

Further on the development of the standard led to the birth of the 3G wireless telephony networks: Universal Mobile Telecommunications System (UMTS) [5]. UMTS data transfer can reach 384 kbps. If the 3G UMTS network implements the High-Speed Downlink Packet Access (HSDPA), this combination being considered the 3.5G, it can reach a downlink data rate of 7.2 Mbit/s. The Long Term Evolution (LTE) [6] project upgrades UMTS to 4G. 4G systems are providing data rates in the range of 100 Mbit/s. The continuous increase in the data rate from 2G to 4G networks is due to the permanent enhancement of the implemented modulation schemes/techniques, to the channel bandwidth increase and to the enhancement of multiple access methods. Furthermore, the data rate is foreseen to increase to Gbit/s when 5G systems will be deployed.

Given the large number of world-wide users, GSM-UMTS-LTE are by far the standards driving the world of wireless mobile communication. However, also short-range standards have been created to allow broadband Internet access and

to enhance wireless interoperability of mobile terminals. Amongst them, the most popular at present are W-LAN and Bluetooth.

A wireless local area network (W-LAN) connects various devices through a wireless distribution method [7]. Although originally developed for interconnecting standalone desktop PCs, the standard became popular, given the success of notebook computers. Nowadays, W-LAN compatibility is also a key feature of the most advanced mobile terminals, or smart phones. The W-LAN protocol is regulated by the IEEE 802.11 family of standards [7–12]. The original standard introduced in 1997 specified two data rates of 1 and 2 Mbit/s. When first updated (to revision a) in 1999, it allowed a gross bit rate of 54 Mbit/s. By 2003, the new g flavor was able to provide 128 Mbit/s when the BW was increased from the normal 20 to 40 MHz. By 2009, the next W-LAN amendment, the version n, is able to offer an astonishing data rate of up to 600 Mbit/s, by exploiting MiMo techniques. And, the latest addition, the ac version, can deliver up to 3.39 Gbit/s due to the channel bandwidth increase to 160 MHz and the use of four antennas.

Bluetooth is a wireless protocol for exchanging data over short distances. Introduced in 1998, the version 1.2 has a data rate of 1 Mbit/s. By 2004, the protocol was updated to version 2.0 that allows 3 Mbit/s [13]. In 2009, the third version included a high-speed feature that used the collocated W-LAN link to transmit data with rates up to 24 Mbit/s [14]. And, the fourth version, in 2010, added features for low power operation [15].

Figure 1.3 plots the evolution of the maximum data rate of both long-range wireless standards and short-range ones.

In order to simplify the communication, the latest wireless standards converge towards a "one size fits all" solution, e.g., IEEE 802.16m or WiMAX mobile [16]. The standard, introduced in 2007 and updated in 2009, embeds the feature of both long- and short-range communication standards by using almost all modulation schemes and by enforcing a variable channel bandwidth.

Hence, depending on the wireless link SNR, the WiMAX network can adjust dynamically its data rate, from a minimum of a few kbps to maximum of 100 Mbit/s. The 3GPP Long Term Evolution (LTE) standard introduced by the Mobile Communications operators is the competitor for WiMax. Although LTE and WiMax use comparable technologies and offer a comparable user experience, LTE won the battle.

In conclusion, all the wireless digital communication of the future will have to embed the main features of LTE, features that make the standard fit perfectly the drive to reach both higher data rates and cover a longer distance, as it results for (1.1):

- Compatibility with a large number of modulation schemes/techniques
- The ability to handle multiple RF frequency bands and variable baseband channel bandwidths

Finally, by comparing the plots from Figs. 1.2 and 1.3, we can clearly state that the wireless communication is catching-up fast with the wired communication data rate.

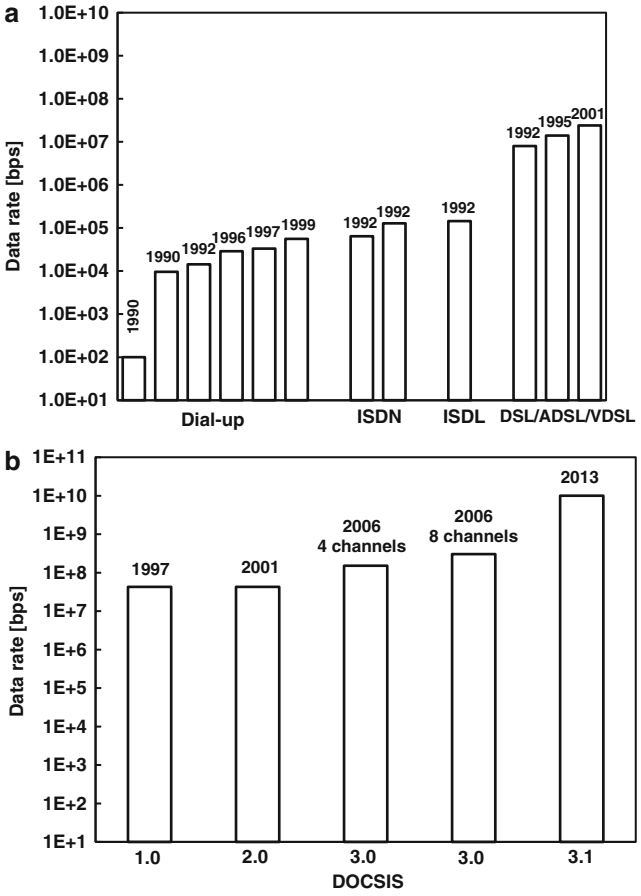

Fig. 1.2 Internet access data rate of copper wire networks: (**a**) Fixed telephony; (**b**) Cable TV

1.1.2 The Need for Software Defined Radios

One of the major problems in the mobile communication systems of today is that every standard requires a particular set of hardware equipment to allow a compatible dialogue. On top of it, because implementation details differ from network operator to network operator, even the same standard requires different hardware depending on the continent of deployment. The most prominent example is LTE that can be found worldwide on 44 frequency bands (see Table 3.1).

A similar issue characterized the early beginnings of the IT industry in 1980s. There was no compatibility in between different Personal Computers (PCs) available on the market. The major differences that impeached the development of the overall sector were the lack of uniformity in both data storage and data

management. The natural solution to these issues turned out to be the "WINTEL" monopoly, an Intel-based PC run by a Microsoft Operating System (OS). Basically, all the divergent trends in the IT sector converged to making the "WINTEL" platform the dominant desktop and laptop computer architecture.

For the mobile communication sector the development was completely different to allow a similar monopoly to be formed. The globalization allowed various players to enter the geographically different markets at about the same time, thus fairly dividing the market share. Also, in terms of frequency band allocation, the various independent national/federal/continental organizations allocated different bands for the same particular standard.

The present business environment is a global one, requiring constant travel. Not only that, but also, leisure activities (like tourism) fit the same profile. Since, unifying various communications standards is not a real possibility, given the huge number of users dedicated to a given wireless standard there is a request of mobile equipment that needs to ensure compatibility over a wide variety of environments.

On top of it the current mobile devices evolved into real portable PCs. A 2015 handset includes an FM radio, MP3 player, MPEG4 media player, backed by a multi-core processor. All these hardware features are coordinated via an operating system: the most popular ones are the iOS, Microsoft, and Android. Hence, purely on the communication side, the present mobile equipment requires compatibility with all the standards maximizing its interaction capabilities: GSM/GPRS, UMTS, LTE, Bluetooth, Wireless LAN. Further on, considering the 5G deployment, the mobile terminal needs to coop with new standards enhancing its connectivity, by also providing backwards compatibility.

The first obvious solution was to incorporate for each standard a separate dedicated IC or ASIC (Application Specific Integrated Circuit) into the mobile device. One still has to have in mind that the first Nokia mass production GSM mobile phone, the Nokia 1011 developed in the early 1990s, was built from more than a two dozen separate ICs and weighted about half a kilo, while by mid-2000s, solutions offering fully integrated quad-band GSM SoCs were already available.

A first step in cost reduction was allowed by CMOS technology scaling: It opened the possibility of building "combo" ASICs, combining two or more SoCs on the same IC. However, these circuits still contain one RF front-end per communications standard.

So, in order to reduce cost even further, another step must be taken. In the IT world of the late 1970s this step came naturally, as INTEL developed what it turned out to be a general-purpose microprocessor. This approach allowed the hardware manufacturer to grasp almost all the consumer market, as its microprocessor turned out to be used in almost all commercial applications. Given the historical differences between the IT industry and the mobile communication sector development, such a scenario did not occur in the latter domain.

Building a reconfigurable ASIC, able to ensure compatibility with the wide array of communication standards in use today, is efficient from two main reasons:

- One "universal" design is required; thus design, packaging, and testing costs are minimized.
- As the "universal" ASIC is compatible with a wide array of wireless communication standards, the previous various ASICs can be merged; thus the overall area of ASICs comprised in a mobile terminal is minimized.

In the "digital" realm, the first step on this track is the development of the new multi-core DSP architectures. Such processors optimally leverage the power consumption with the cost, or equivalently occupied die area. The idea is to enforce as much parallel processing as possible to maintain a maximum "usage" of the chip die area during operation.

In this context, it is required to develop a transceiver capable to interface such a DSP. The transceiver must have a versatile architecture, able to change its characteristics dynamically, given the wireless standard and communication burst it has to handle.

The optimal design of a re-configurable receiver front-end embedded in a software-driven System-on-a-Chip (SoC) represents the target of this book. The block schematic of the system is depicted in Fig. 1.4.

1.1.3 The Software Defined Radio RF Front-End

The three main blocks comprising the SDRX transceiver front-end of Fig. 1.3 are:

- The frequency synthesizer (FS), made out of a Phase Locked Loop (PLL) and a wide-band frequency divider (DIV)
- The receiver (RX)
- The transmitter (TX)

The transceiver acts as an analog signal conditioning block. It either prepares the received signal for digital demodulation or it shapes the digitally modulated signal for the wireless transmission. The digital signal processor (DSP), also known as the baseband processor, represents the digital back-end processing block. The DSP drives the analog front-end via the digital interface.

By dynamically changing the transceiver settings, its performance can be adjusted depending on the requirements (e.g., noise or linearity performance, output power level) of the particular communication burst.

The FS is the transceiver core. Its beat is represented by the generation of the local oscillator (LO) signals which drive the receiver, respectively the transmitter chain mixer.

The task of any wireless receiver is to ensure the received signal analog signal conditioning allows its correct digital demodulation.

Oppositely to the RX, the TX chain must ensure the up-conversion on the RF frequency of the digitally modulated baseband signal. In the transmitter case the accent is placed on (1) avoiding the disturbance of adjacent radio frequencies and (2) maintaining a good signal integrity. This implies the whole process of

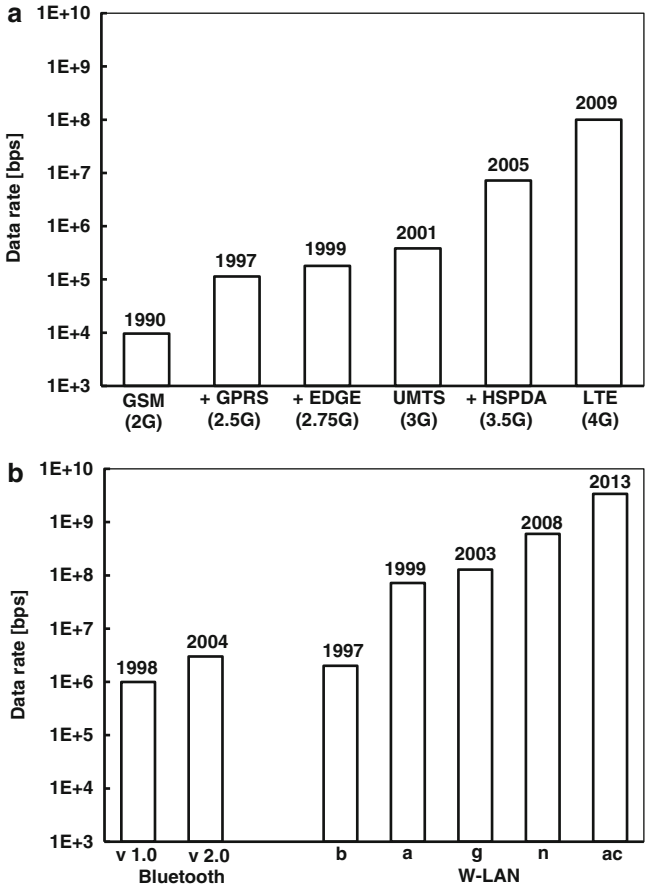

Fig. 1.3 Maximum Internet access data rates for the most popular commercial wireless standards: (**a**) Long range; (**b**) Short range

up-converting the wanted informational signal, from baseband to the RF carrier frequency, (1) dispenses almost all the transmitted energy into the allocated bandwidth in (2) a linear way.

1.2 Goals

The book is focused on the RF and analog signal conditioning part of the receiver of the System on Chip (SoC) in Fig. 1.3 and has the following four main goals:

1. The identification of the *most suited architecture for the Software Defined Radio Receiver* (SDRX), in the deep sub-micron era of CMOS processes

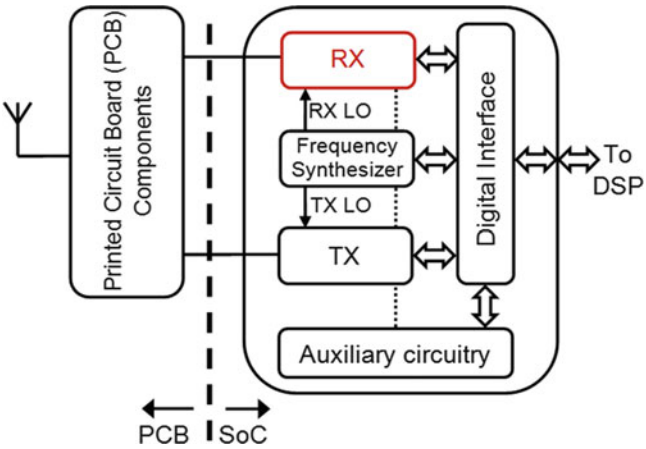

Fig. 1.4 Software Defined Radio transceiver block schematic

2. *The development of new tools, based on simple and efficient models suited for manual analysis that enable the designer to handle efficiently the large amount of information comprised in the wireless standards*. In other words, the SDRR domain map is explored using these new tools as a compass
3. *The development of a new standard independent, system level driven design methodology that permits the identification of the optimal circuit solution in term of power and area saving*
4. *Using the newly developed system-to-circuit level design methodology to derive the key electrical specifications for the first design iteration of a general-purpose SDRX*

1.3 Overview

1. The book first goal, the identification of the most suited architecture for the SDRX, is discussed at large in Chap. 2.

   Based on the analysis and evaluation of figures of merit of existing radio receiver architectures, the direct conversion topology was selected for the SDRX architecture. The key issues of direct conversion receivers, like offset, 1/f noise, and self-mixing, are presented and solutions are proposed to make this architecture ready for monolithic integration.
2. Once the architecture is set, the multi-standard environment is evaluated, as a first step in deriving the electrical specifications for the receiver. *A first order, system level, standard independent analysis methodology* was developed in Chap. 3 to enable the designer to handle efficiently the large amount of information provided in the envisaged wireless standards. Based on this new methodology, the designer is able to attack in parallel the wireless standards when

deriving the SDRX specifications. Thus, the key SDRX electrical specifications (i.e., NF and IIP3) are derived in a standard independent way.

3. Moreover, a new and efficient tool is introduced: *the generic blockers diagram*. This represents an exhaustive blocker map, which enables the designer to determine the worst case scenarios for blocker tests. Being thus prepared, the designer is now ready to properly address the optimal filtering partitioning between the analog LPF and the digital filter following the ADC in conformity with Chap. 4 explanations. *Through the introduction of a new Figure of Merit (FOM), the trade-off between the analog LPF area and ADC power consumption is evaluated in one single plot*. This new FOM represents another efficient design tool that empowers the designer to choose the optimal SDRX filtering configuration, the key feature for the SDRX implementation.
4. Further on, in Chap. 5, the analysis focuses on another key trade-off in wireless receiver design: the trade-off between its noise and linearity performance. Based on the presented analysis, a novel gain partitioning strategy is introduced. The strategy is tailored towards multi-standard radio receivers and optimally mitigates the extreme reception conditions specific to the wireless environment.

   By allowing the receiver gain, noise and linearity performance to scale with the useful input signal level variation, the SDRX is empowered to optimize its output SNR, given the particularities of each reception burst. This concept represents the "smart" receiver gain partitioning.
5. Chapter 6 starts by presenting the SDRX electrical specifications that should be considered as a first design iteration towards building a general-purpose SDRX suited for the 5G deployment. Moreover, the chapter details the noise and linearity partitioning between the SDRX high-frequency part and its low-frequency part.
6. Chapter 7 overviews the modern receiver's building blocks and presents the most suited bias block that will ensure minimal variation of the key design parameters. Also, the low-frequency part noise breakdown is presented.
7. Chapter 8 concludes the book and gives a sneak-peak into the future developments.

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Chapter 2
Defining the Optimal Architecture

2.1 Introduction

The basic modern communication system comprises a large array of mobile equipment into a wireless network. The communication between all these equipment is regulated by various communication standards, depending on the type of wireless network in which they are connected.

In order to maximize the potential of wireless communications, the latest wireless standards converge towards a "one size fits all" solution. As an example, the W-LAN standard, IEEE 802.11ac, uses almost all basic digital modulation schemes (i.e., BPSK, QPSK, 16-QAM, 64-QAM, 256-QAM, and 1024-QAM) on OFDMA carrier support with variable modulation depths, while it still maintains compatibility with the earlier IEEE 802.11 lower data rate standards.

Hence, the latest developments in standardization point to a software re-configurable hardware solution for the radio front-end as the best way to trade-off backwards compatibility with future trends. This observation is critical as we move on towards the 5G deployment.

The main target of this chapter is to determine the optimum architecture choice suited for the SDRX. The analysis starts with an overview of the standard receiver architectures in Sect. 2.2 and, subsequently in Sect. 2.3, and determines the quadrature direct conversion topology suits best the envisaged purpose. For such receiver architectures, regardless of the communication wireless standards, the received signal is downconverted directly to baseband and the digital signal processor (DSP) software demodulation scheme is changed accordingly such as it can handle it. Hence, the possibility of implementing a "universal receiver" is revealed [1].

The chapter continues, in Sect. 2.4, by constructing the solutions that make direct conversion receivers ready for monolithic integration. *The presented solutions are realized without introducing particular analog tricks to satisfy the needs of only one of the standards, as the SDRX must represent a "universal receiver,"*

S. Spiridon, *Toward 5G Software Defined Radio Receiver Front-Ends*,
SpringerBriefs in Electrical and Computer Engineering,
DOI 10.1007/978-3-319-32759-4_2

and not be turned into a "multi-standard Application Specific Integrated Circuit (ASIC)."

Further on, Sect. 2.4 presents the natural architectural evolutions due to the increased power consumption efficiency of modern ADCs.

2.2 Overview of Receiver Architectures: Following the Image Rejection

2.2.1 Superheterodyne Receivers

Single Conversion

The superheterodyne architecture was developed in 1918 by Edwin Armstrong as a viable alternative to the regenerative receiver with respect to the technical issues of vacuum tubes implementation [1]. The basic block schematic of this concept is depicted in Fig. 2.1. The original superheterodyne uses only one downconverter mixer, *single conversion* superheterodyne, and mixes the Radio Frequency, RF, input signal with the Local Oscillator, LO, signal.

The resulting signal frequency is shifted down to an Intermediate Frequency, IF, equal to the difference between the RF carrier and LO signal frequencies.

Intrinsically the mixing process will render at the mixer output also the sum frequency component. For most applications this component represents an unwanted signal and is filtered by the band-pass filter following the mixer and/or in the mixer output stage.

The major issue of superheterodyne topology is the image frequency rejection. The problem resides in the fact two symmetrical signals with frequencies spaced apart by twice the IF frequency are downconverted by LO mixing to the same IF frequency, as shown in Fig. 2.2.

If the communication is dual sideband, meaning both RF signals convey the same useful information, there is the no problem, since spectrum overlapping in the IF band is beneficial. However, this is not the case for the vast majority of applications, which are employing single side band communication. Thus, the unwanted image signal rejection becomes critical.

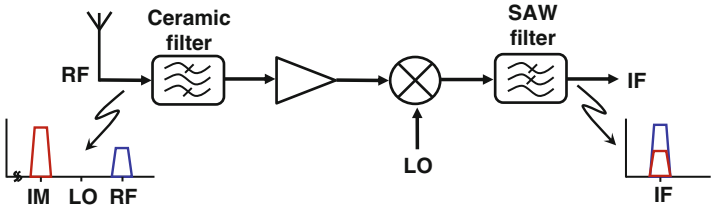

Fig. 2.1 Single conversion superheterodyne receiver block schematic

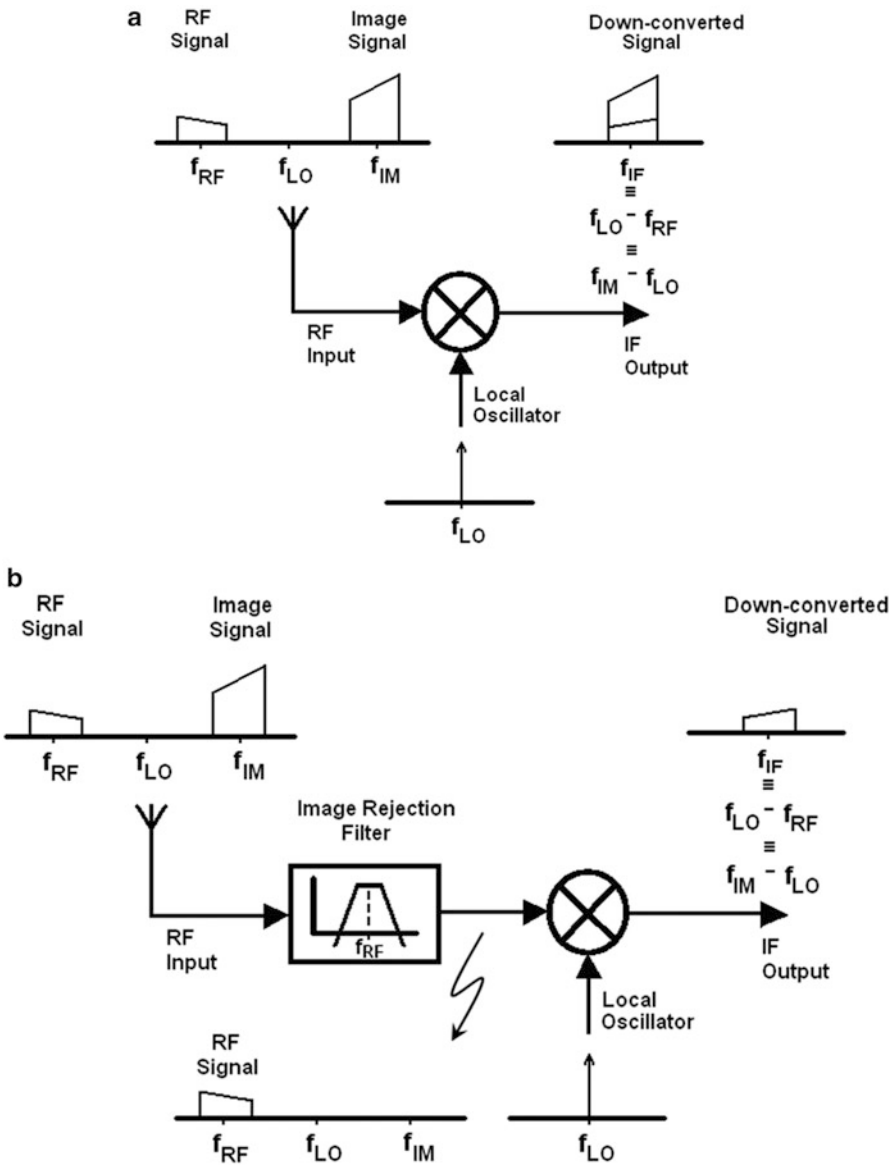

Fig. 2.2 Downconversion: (**a**) without Image Rejection and (**b**) with Image Rejection

The superheterodyne architecture solves the issue by filtering the image signal before it enters the mixer, or more precisely, immediately after the antenna. The image rejection filter specifications depend on the IF value and they are more relaxed as the image frequency is larger, respectively, as the distance between the RF carrier and its image is larger.

Signal conditioning constraints, set by the channel selection filter—the second band-pass filter of Fig. 2.1, prevent the choice of a very large IF, thus toughening image filtering requirements. In practice, ceramic filters satisfy the constraints, although they possess two major drawbacks: they are quite expensive and by far not compatible with monolithic integration.

Channel selection is also demanding, as for many applications channel bandwidth is fairly small compared with IF. In such context, bandpass Surface Acoustic Wave (SAW) filters are used for analog channel selection. However, these types of filters are unattractive to SoC ICs for the same two reasons as the ceramic antenna filters: incompatibility with monolithic integration and high cost.

In conclusion, single conversion superheterodyne receiver design is driven by the trade-off between antenna and channel filtering, which imposes the optimum IF frequency.

Dual or Double Conversion

For *Single Conversion* superheterodyne, the choice of a low IF leads to tough specifications for the antenna filter but does not affect the ones for the channel filter, while a high IF constraints the channel filtering and relaxes the antenna filter specifications. Either way, for most wireless applications, the antenna filtering requirements lead to choosing a cumbersome ceramic filter as the image filter and the IF filtering requirements impose a SAW filter for analog channel selection.

The *Dual Conversion* superheterodyne, which principle schematic is depicted in Fig. 2.3, uses two IFs to ease the image filtering and channel selection, respectively, to relax the antenna and channel filters specifications. The idea is to first up-convert the incoming RF signal to a high IF, relaxing image filtering requirements, while the downconversion mixing is made to a low IF, simplifying channel selection. Still, for most applications, the antenna and image filters will require implementation by ceramic filters.

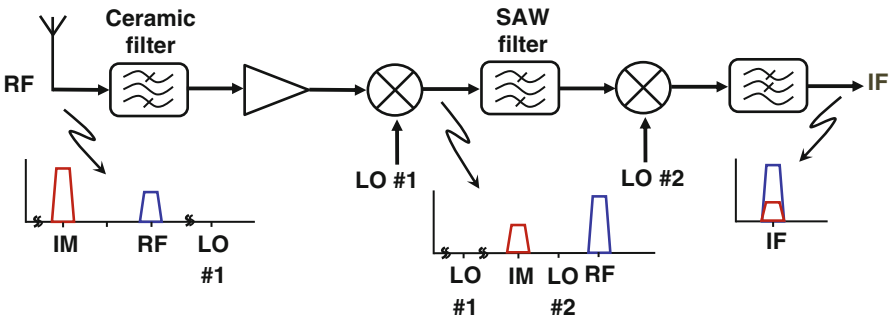

Fig. 2.3 Dual conversion superheterodyne receiver block schematic

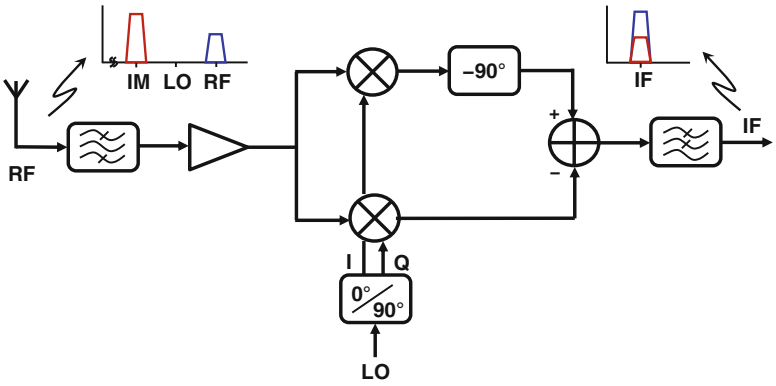

Fig. 2.4 Image rejection receiver

Hence, superheterodyne architectures cannot solve the image rejection problem monolithically.

2.2.2 Image Rejection Receivers

So far, the design of superheterodyne receivers has been optimized to alleviate image rejection rather than optimizing RF performance.

An image rejection receiver uses a "*complex*" mixer to cancel out the unwanted image signal, removing the lock on architecture and allowing the system design to optimize RF performance. The principle schematic of such a receiver is depicted in Fig. 2.4.

The "*complex*" mixer is made out of two mixers which share the same RF input, while the LO port is controlled by two quadrature signals. By adding a 90° delay line in one signal path, the downconverted image signals will be in-phase, while the useful signals will be 180° delayed. Hence, by considering the difference between the two paths the image signal is cancelled, while the useful signal is added.

The major advantage of this approach is the antenna filtering becomes less critical. Thus, the use of expensive and bulky, external (off-chip), ceramic filters is no longer required. On the other hand, the image rejection now depends on the quadrature accuracy of both gain and phase of the LO and IF paths. If the two LO signals exhibit exactly 90° phase delay and have the same amplitude, while the gain of the two paths are perfectly matched, the unwanted image signal is completely rejected.

Hence, image rejection receivers cancel out the image signals by subtracting two potentially very large signals, and resulting in a difference that is theoretically equal to zero. However, any gain or phase error between the two signal paths will result in incomplete cancelation of the image signal. Thus, the image rejection is given by [2]:

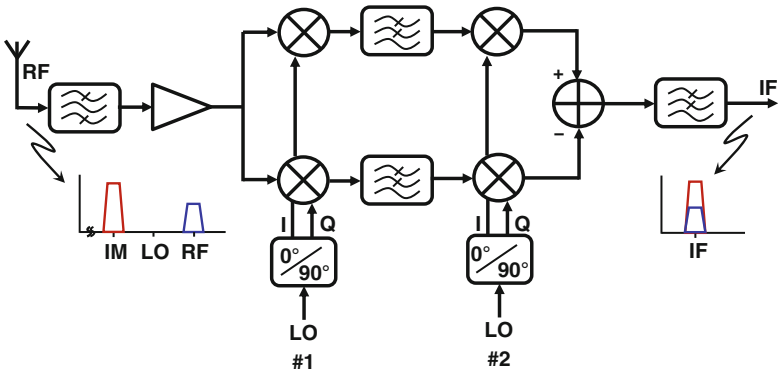

Fig. 2.5 Weaver receiver

$$\text{Image Rejection} = -20\log\left\{\frac{1}{2}\left[\frac{Gain_{I-Q\ \ err}}{Gain} + tg\left(Phase_{I-Q\ \ err}\right)\right]\right\}\ \ [\text{dBc}] \quad (2.1)$$

where *Gain* represents the receiver's gain, $Gain_{I\text{-}Qerr}$ is the I-Q gain mismatch, and $Phase_{I\text{-}Qerr}$ is the I-Q phase mismatch.

Since accurate wide-band quadrature phase shifters are difficult to design, Weaver receivers of Fig. 2.5 are preferred. To cancel the need for 90° phase shifter on signal path, an extra pair of mixers and quadrature LO signals are required.

Still, the LO signals quadrature accuracy, of both gain and phase, and the gain matching of the quadrature downconverted channels set the image rejection performance as described by (2.1).

For both image rejection approaches, if a low IF is chosen then the IF filtering requirements are relaxed, as well as subsequent A/D conversion or baseband processing. The image rejection can typically be lowered to about −35 dB with quadrature generators like Poly Phase Filters or divide-by-2 Johnson Counters.

2.2.3 Direct Conversion Receivers

All receiver architectures presented so far have to fight image rejection. In general, a signal and its image are spaced apart by twice the Intermediate Frequency (IF). To reject the image, superheterodyne receivers require the use of expensive off-chip SAW filters, while dual-conversion architectures trade-off the SAW filter for a standard, but still bulky and expensive, ceramic filter, at the expense of an extra up-converter mixer.

In Fig. 2.6 the typical block schematic of a quadrature direct conversion receiver is depicted. Quadrature LO drive enables the receiver to demodulate the RF signal regardless of the phase relation between the LO and incoming RF signals [1].

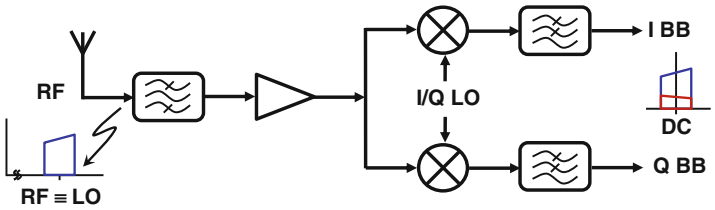

Fig. 2.6 Quadrature direct conversion receiver

In direct conversion receivers, also known as homodyne or zero-IF, the IF frequency is zero. Hence, the useful signal is its own image. *Therefore, in a zero-IF system the image signal has an amplitude comparable to the useful signal, and thus, image rejection requirements are drastically relaxed.* Furthermore, all baseband processing, like analog baseband signal conditioning, analog-to-digital conversion and the digital demodulation, take place at the lowest possible frequency.

These features make the direct conversion receiver an ideal candidate for monolithic integration and open the possibility of creating a "*universal*" receiver, compatible with all wireless standards. However, although direct conversion receivers monolithic integration seems straightforward, there are several drawbacks to this approach.

First of all, the zero-IF architecture is extremely sensitive to DC offset and 1/*f* noise. As the signal is directly converted to baseband, receiver noise figure is affected by 1/*f* noise and its output risks of being overloaded even for small values of the DC offset, in the order of a few tens of μV. Such low DC offset, or 1/*f* noise, values are not easily achievable in practice. Regular AC coupling will not be solving the issue, as receiver settling will be severely affected by a low cutoff frequency, in the order of a few hundred Hz.

Some of these problems have been already addressed at protocol level, as the latest wireless standards tend to use modulation schemes that minimize the baseband signal low frequency spectral energy. Also, for Time Division Multiple Access (TDMA) systems, a dedicated time slot for calibration is foreseen: the guard band. Hence, static offset cancelation is possible before each actual receive burst.

The second major issue of direct conversion architecture is that even-order distortions generate a signal-dependent DC offset. Handling dynamic offset, to the extent required by almost all commercial wireless standards, implies the usage of a differential architecture for the whole receiver chain, starting with its Low Noise Amplifier (LNA).

Another issue of such architecture is self-mixing. The LO signal, which in most cases is orders of magnitude larger than the RF signal, leaks to the RF port of the mixer and is mixed down to baseband. If the LO leaking signal is phase shifted with respect to the real LO, this almost always being the case in practice, the DC offset caused by self-mixing dominates the mixer output. Hence, very good isolation between RF and LO mixer ports is required for good receiver performance.

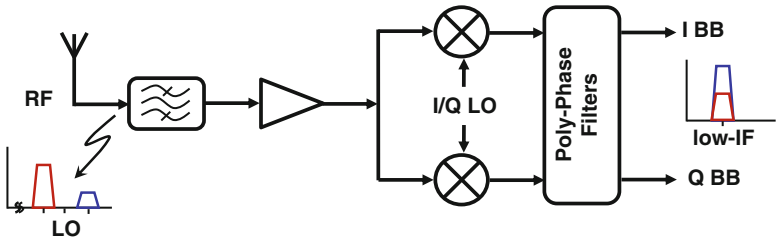

Fig. 2.7 Low-IF receivers

Also, because the large gain of the direct conversion receiver is focused at one frequency, the isolation between input and output of the receiver is critical, as any parasitic feedback loop may lead to system instability.

2.2.4 Low-IF Receivers

Finally, although direct conversion architecture has very relaxed image rejection specifications, it has to fight with DC offset, 1/f noise, and self-mixing.

Hence, the low-IF architectures (see Fig. 2.7) become attractive. Essentially, the RF signal will now be downconverted to a low-IF frequency (i.e., up to a few hundred kHz) and thus, the issues of direct conversion receivers are alleviated.

However, the image rejection requirements are again heavily constricted. This stresses the implementation of the active poly-phase filter that follows the complex mixer and is used for image rejection and channel selection.

2.3 Final Decision: w/ IF vs. w/o IF (Zero-IF)

The main features of a SDRX must be a versatile architecture and the ability to be reconfigured on-the-fly as the communication burst requires.

From the perspective of SoCs, the optimization of the chip power dissipation and die area is mandatory. As the SDRX will be embedded in an SoC, this trade-off must be the main guideline in sizing the SDRX design, as well as in choosing its architecture, as a first and, very important, starting point. *The SDR architectures of choice are superheterodyne* (*w/ IF*)*, either single or dual conversion, low IF* (*w/ IF*) *or direct conversion* (*w/o IF*).

From area perspective the cumbersome image rejection filters of superheterodyne topology are not so attractive for monolithic integration. On the other hand, for direct conversion the image rejection requirements are much smaller than for any other receiver architecture.

Furthermore, the IF selection for superheterodyne architectures is fairly cumbersome and cannot be extrapolated in a systematic way to all standards, as it would be required for a true SDRX [3]. Basically, the IF should be chosen to avoid the in-band downconversion of strong interferers. In most applications the nearest strong interferers are located three channels apart from the RF carrier. As the channel bandwidth differs even within the same wireless standard, it is not possible to select intermediate frequencies which will lead to reuse of same image filters for a multi-bandwidth environment compatible receiver.

From the power consumption perspective, the direct conversion topology has even more advantages.

First of all, the baseband signal processing takes place at the lowest possible frequency.

Secondly, this topology is not tributary to the 3 dB noise penalty of superheterodyne architectures [2]. Basically, direct conversion quadrature receivers are using the information from both sidebands, as the image is actually the useful signal. While, for most commercial applications, the superheterodyne receivers are using only one sideband, as the image signal is not a useful signal (see Fig. 2.8).

By using an additional bandpass ceramic filter after the LNA, the single sideband superheterodyne receivers noise penalty is reduced. However, this makes the overall system even more unattractive for monolithic integration.

So far the zero-IF architecture had presented overwhelming advantages to the heterodyne approach, including also here the low-IF architecture, in terms of image rejection, and thus, for monolithic integration purposes.

It is true that the direct conversion has some issues with DC offset and 1/f noise that the low-IF architecture can overcome. However, these issues can be overcome as discussed in detail in Sect. 2.4, whereas the low-IF systems still have to fight very tough image rejection specifications.

Hence, it becomes clear that direct conversion receivers are the only ones capable of satisfying the requirements of a true SDRX.

Table 2.1 summarizes the advantages and disadvantages of the three architectures with respect to monolithic integration in a SDRX SoC.

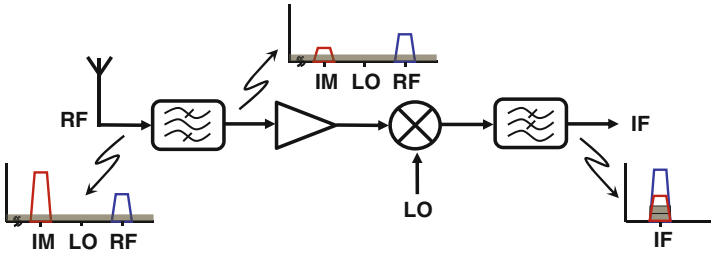

Fig. 2.8 Superheterodyne 3-dB noise penalty

Table 2.1 Heterodyne and low-IF vs. direct conversion receivers comparison regarding SoC integration—PROs and CONs

Superheterodyne		Low IF		Direct conversion	
PROs	CONs	PROs	CONs	PROs	CONs
☺ Well known	☹ **High image rejection requirement**	☺ No DC Offset	☹ **High image rejection requirement**	☺ **Low image rejection requirement**	☹ DC Offset
	SAW Filter	☺ Reduced 1/f noise	SAW Filter	No SAW Filter	☹ 1/f noise
	☹ IF selection	☺ Reduced self-mixing		☺ Image is wanted signal mirror	
	Difficult to mitigate the multi-standard environment			Mirror signal is not a strong interferer	
	☹ Power consumption			☺ Power consumption	
	Baseband signal conditioning is done at IF			Baseband signal conditioning is done at lowest frequency	
	☹ 3 dB noise penalty			☺ No 3 dB noise penalty	
	Image frequency band degrades receiver SNR by 3 dB			Quadrature receiver	

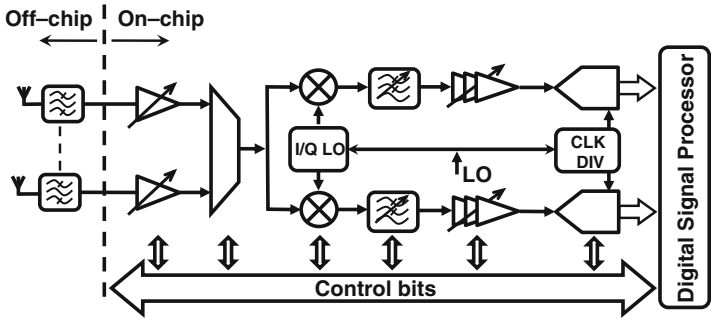

Fig. 2.9 SDRX block diagram

2.3.1 Receiver Block Schematic

The block schematic of a true multi-standard re-configurable receiver, including the final ADC, is depicted in Fig. 2.9.

The main tasks of a radio receiver consist in isolating the wanted, useful signal from other electromagnetic signals arriving at the antenna, amplifying and converting it from a (high) radio frequency (RF) to baseband (BB).

The incoming RF signal is picked up by the receiver's antenna and is amplified by one of its LNAs. Multiple LNAs can be integrated, depending on the envisaged use.

The *amplified* RF signal is then converted to current in the mixer input gm-stage and downconverted directly to baseband by mixing with a local oscillator signal of equal frequency. Hence, at the mixing stage output the signal has a spectrum spanning from DC to a maximum frequency that is dependent on the wireless communication standard, as detailed in Sect. 3.1.

After mixing, the signal is conditioned by a low-pass filter (LPF) and a variable gain amplifier (VGA), before its conversion to digital spectrum by an ADC.

Through digital control the SDRR blocks main characteristics (e.g., bandwidth, noise, and linearity) can be changed dynamically depending on the particular standard requirements or even on the particular communication burst necessities.

Basically, the receiver chain of Fig. 2.9 is split into a high-frequency (HF) part, comprised by the LNA and the gm stage of the downconverter and a remaining baseband low-frequency (LF) part, following the mixer's switching stage.

The receiver design is a result of noise-linearity trade-offs under power consumption constraints. The key trade-off shaping its design is the one between the LPF order and ADC power consumption, as detailed in Chap. 4. The receiver's high-frequency part is shaped mainly by noise requirements, while its baseband blocks must enforce a linear channel selection to prevent the RF useful signal distortion, as is detailed in Chap. 5.

2.4 Making Direct Conversion Receivers Ready for Monolithic Integration

2.4.1 Key Issues

As detailed in Sect. 2.2 and in-depth analyzed in [4], due to intrinsic operation of zero-IF systems, they exhibit a large sensitivity to DC offset, either static or dynamic, and 1/*f* noise. Also, self-mixing issues can dramatically reduce performance of receivers implemented with direct conversion architectures.

First of all, direct conversion architecture is extremely sensitive to static DC offsets and 1/*f* noise. As the signal is directly converted to baseband, receiver noise figure is affected by 1/*f* noise. Generally the mixer output is DC coupled to the LPF, since a major part of the received signal baseband spectral energy is located at low frequency (i.e., the GSM standard). Regular AC coupling will not solve the issue, as receiver settling will be severely affected by a low cutoff frequency in the order of a few hundred Hz. Also, given the large VGA gain, usually larger than 60 dB, the receiver output risks of being overloaded even for small values of the DC offset, in the order of a few hundred μV.

The second major issue of the zero-IF receiver architecture is even-order distortions generate a signal-dependent DC offset. As the received input power can change dynamically, since other transmitters may start to communicate, a dynamic offset component is generated due to the receiver second-order nonlinearity.

Also, the self-mixing process, determined by the LO mixing with the LO signal leaking from the Voltage Controlled Oscillator (VCO) to the receiver input, can generate a large DC offset overloading the receiver output.

The section main goal is to determine the architectural changes in Fig. 2.9 receiver, required to compensate the abovementioned issues. Section 2.4.2 covers the architecture sensitivity to static DC offsets and 1/*f* noise and explains the dynamic offset generation in the presence of second-order distortions. In Sect. 2.4.3, the best method to avoid self-mixing process is presented. Finally, Sect. 2.4.4 presents the updated SDRX block schematic, while Sect. 2.4.5 presents the natural evolution of Fig. 2.9 receiver.

2.4.2 DC Offset Compensation

Static Offset Removal

Low DC offset and 1/*f* noise values are required for proper signal demodulation during the receiving phase. In practice these low values are not easy to get without calibration.

Wireless communications are burst communications and a dedicated time slot for calibration is foreseen: the guard band. Thus, static offset cancelation is possible before each actual receive burst.

While the LNA is AC coupled to the mixer, the mixer output is DC coupled to the baseband part of Fig. 2.9 receiver. One of the possibilities to calibrate the receiver static DC offset is the use of the correlated double sampling technique [5]. This offset compensation technique is preferred to chopper stabilization [6] as there is no risk of spurs overwhelming the receiver output spectrum.

This analog technique, described by Fig. 2.10, implies in a first phase (i.e., *Offset_meas* control signal @ "High"—switches closed) sampling the baseband chain DC offset on a capacitor, via the additional transimpedance amplifier, while the antenna input is shorted to ground [7].

During normal operation, the second phase (i.e., *Offset_meas* @ "Low"—switches open), the RF input is connected again to the antenna and the signal flows through the receiver, while the DC offset is inherently cancelled out. The frequency of two phases alternation is set by the baseband signal bandwidth: the smaller the baseband signal bandwidth, the higher is the duration of the DC offset sampling (see Table 3.1).

The advantage of this technique is the 1/*f* noise is also reduced, next to the static offset cancelation; the drawback is the white noise level doubling because of the aliasing. Hence, in order to reduce the increase of the wideband noise, for standards

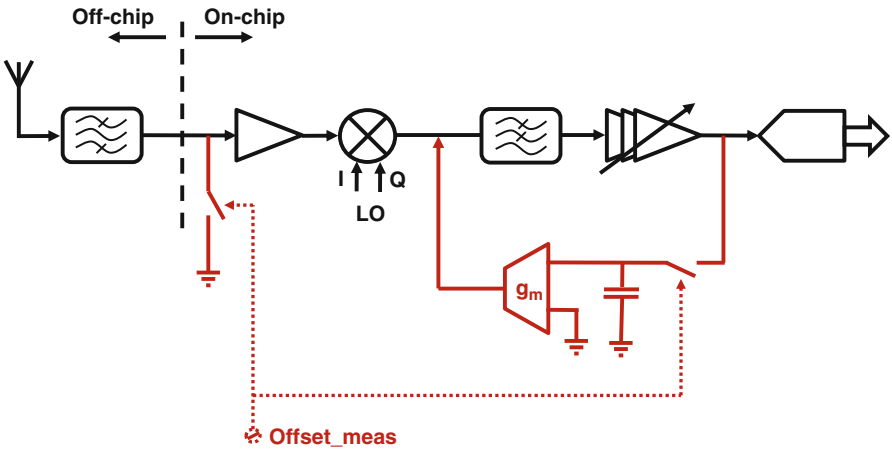

Fig. 2.10 Receiver block schematic with analog offset compensation (only one baseband channel is shown)

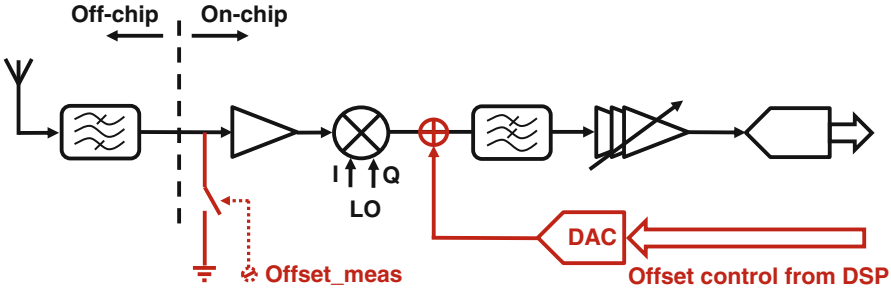

Fig. 2.11 Receiver block schematic with digital offset compensation (only one baseband channel is shown)

with a larger baseband bandwidth, regular AC coupling can be used for the LPF, while the DC offset compensation can be applied only to the VGA.

Another possibility for offset compensation is to measure the offset in the digital domain, and then correct it in the analog domain through a digital-to-analog converter (DAC). An example is shown in Fig. 2.11.

Handling Dynamic Offset

During the receiving period, the RF input power may change significantly, as the other transmitters in the receiver's neighborhood begin to transmit. The receiver's even-order distortions will change the received signal DC offset component. This *dynamic offset* effect disturbs the received signals demodulation, especially if the

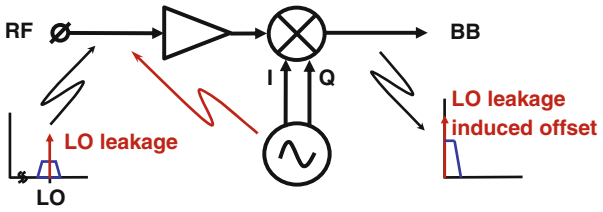

Fig. 2.12 DC offset generation due to self-mixing

envisaged modulation concentrates a large part of the symbol spectral power at low frequency.

Although the latest wireless standards use modulation schemes that do not require the preservation of the signal DC energy, this is not the case for older standards (i.e., GSM). Hence, handling dynamic offset implies the receiver must embed a fully differential signal conditioning chain that offers a high second-order input intercept point ($IIP2_{RX}$). The worst case scenario is met for the GSM standard which requires an $IIP2_{RX}$ of +46 dBm.

2.4.3 Reducing Self-Mixing

The self-mixing process occurs when the large swing LO signal, originating directly from the VCO, leaks to the antenna input, gets amplified by the LNA, and gets mixed with itself in the downconverter, as shown in Fig. 2.12. Hence, a large DC offset is produced at the mixer output. Subsequently, this may eventually clip the receiver output due to the large gain of the receiver baseband chain.

In order to overcome this issue, the VCO must not oscillate at the same frequency with the RF carrier frequency. Hence, the quadrature LO signals driving the downconverter mixer must be obtained by dividing down the VCO frequency. In order to generate good quality quadrature LO signals over a wide frequency band, the best option, relative to a multi-standard implementation, is to use a Johnson counter (e.g., [8]). For such quadrature generators, the VCO frequency must be at least twice of the desired LO frequency.

Thus, since the VCO is not oscillating at the wanted RF carrier frequency, the self-mixing offset is reduced considerably. There is still some residual self-mixing offset, as the divided quadrature LO signal leaks through the mixer switches gate-to-drain capacitance to its input. This offset is of same nature with the static offset, since it is only conditioned by the presence of the LO signal and not by the input signal. Thus, it can be calibrated out if the DC offset compensation loop is applied to the mixer's baseband stage as well.

2.4.4 Enhanced Receiver Schematic

Based on analysis presented in this section, Fig. 2.13 depicts the zero-IF radio receiver block schematic ready for monolithic integration in a re-configurable

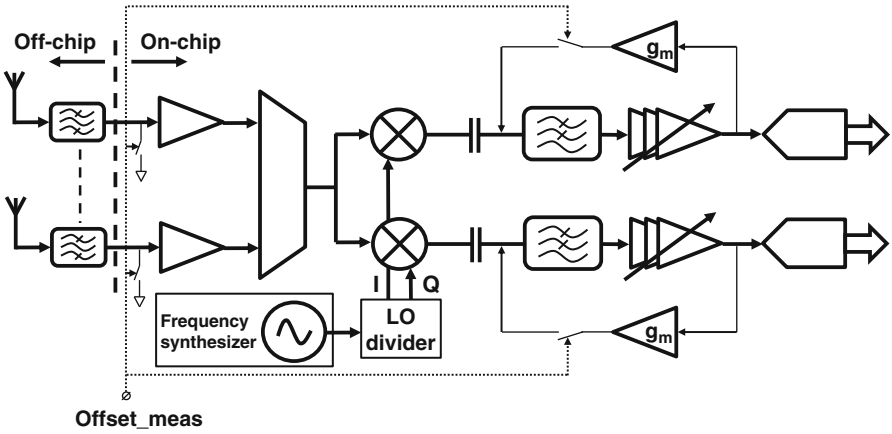

Fig. 2.13 SDRX block schematic embedding DC offset compensation and LO dividers

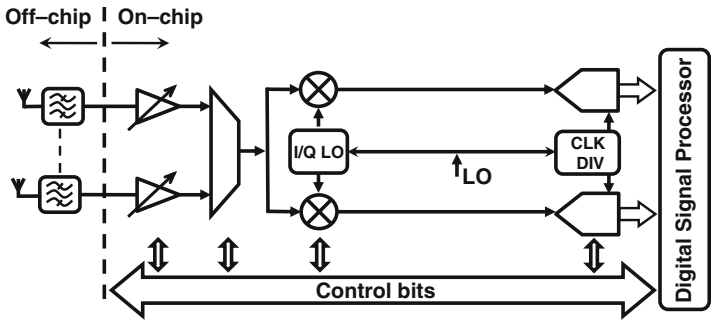

Fig. 2.14 Filter-less SDRX front-end

multi-standard radio transceiver. The schematic is the extension of the SDRX represented by Fig. 2.9. Moreover, the SDRX of Fig. 2.13 has the general characteristics specific to a true multi-standard solution.

2.4.5 Architectural Evolutions: Filter-Less and Mixer-Less Front-Ends

Given the latest trends in ADC dynamic range, sampling speed, and power efficiency improvement [9, 10], the first step in the evolution of Fig. 2.13 receiver is the elimination of the analog signal conditioning baseband chain, comprised by the LPF and VGA. Figure 2.14 depicts the filter-less SDRX front-end.

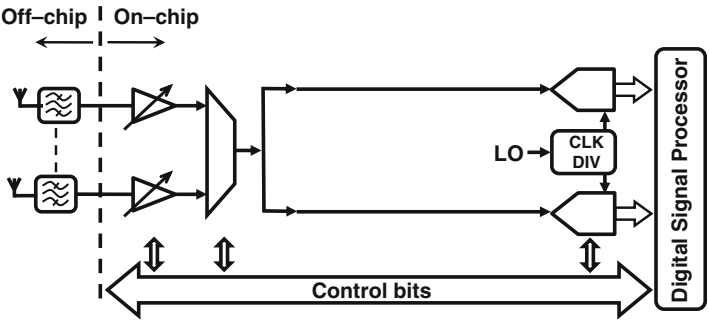

Fig. 2.15 Filter-less SDRX front-end

Of course, once the ADC conversion is performed, the filtering takes place in the digital domain.

Finally, there is another natural step to the evolution of Fig. 2.14 SDRX: the ADC engulfing the mixer as well. Thus, Fig. 2.15 depicts the direct sampling or mixer-less receiver. In this case, all signal processing takes place in the digital domain.

Hence, the designer is faced with three options:

(1) Mixer-based w/ analog baseband signal conditioning (Fig. 2.13)
(2) Mixer-based w/o analog baseband signal conditioning (Fig. 2.14)
(3) Mixer-less or direct sampling (Fig. 2.15)

Considering a given area and power budget, the optimal choice between the 3 options is given by the key trade-off shaping the SDRX design: the trade-off between the ADC power consumption and LPF area. This trade-off is evaluated in Chap. 4.

2.5 Conclusions

This chapter overviewed most common receiver architectures and concluded that direct conversion is the most suited option for a true SDRX. The major advantage is that it allows monolithic integration, since, unlike heterodyne and low-IF architectures, it has much lower image rejection requirements. Moreover, there is another significant advantage that simplifies the implementation from a multi-standard point of view, because the direct conversion topology has always the same IF: zero. Not to mention, in the case of direct conversion-based receiver, all baseband signal processing is done at the lowest possible frequency, and thus it has the lowest power consumption.

Further on, the direct conversion receiver architecture issues relative to the monolithic integration in a SDRX were analyzed. By implementing a DC offset compensation loop, the receiver static DC offset, and inherently 1/*f* noise, are calibrated out during the guard band. The dynamic offset is made negligible by implementing a fully differential receiver chain which offers a high *IIP*2. The self-mixing effects are alleviated by using a VCO oscillating at a different frequency than the RF carrier frequency, and wide-band frequency dividers to generate the quadrature LO signals.

Figure 2.13 depicts the enhanced SDRX schematic with DC offset compensation and wide-band quadrature dividers. Given the ADC performance increase, the natural trend leads to the ADC engulfing the analog baseband signal conditioning chain (see Fig. 2.14), and even the mixer (Fig. 2.15). The optimal choice between the 3 SDRX options is given by the key trade-off shaping the SDRX design: the trade-off between the ADC power consumption and LPF area. This trade-off is evaluated in Chap. 4.

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Chapter 3
From High-Level Standard Requirements to Circuit-Level Electrical Specifications: A Standard-Independent Approach

3.1 Multi-standard Environment Impact on the SDRX Building Block Features

3.1.1 Multiple Frequency Bands

A multi-standard environment is first of all characterized by multiple frequency bands in which the communication takes place. The uplink and downlink frequency coordinates for the targeted wireless standards are presented in Table 3.1.

Hence, a true multi-standard downconverter must contain *multiple* LNAs. Each LNA will be tuned to a specific downlink band by means of external impedance matching. Only one LNA will operate at a given time, as the SDRX provides hardware compatibility with a large number of wireless standards, but it only has one receiver chain.

Given the frequency bands covered by the envisaged applications, each of the LNAs must allow *wideband impedance matching*, for maximum efficiency of SDRX design, because, as mentioned in Sect. 1.1, the SDRX purpose is to offer a general solution to a large number of particular applications.

A tuned LNA design with tunable resonance frequency (e.g., [1]) would be an optimal choice for the SDRX. It will eliminate the intrinsic noise folding of wideband LNA-based receivers. Also, while the input impedance can be matched over a wide frequency band, the band-pass characteristic will also knock down the out-of-band blockers and interferers. Likewise, receivers based on N-path filtering (e.g., [2]) bring the same benefits.

3.1.2 Variable Channel Bandwidths

Multi-standard environment is also characterized by a multitude of RF channel bandwidths. Table 3.1 also presents the RF channel bandwidths for the major commercial wireless standards.

S. Spiridon, *Toward 5G Software Defined Radio Receiver Front-Ends*,
SpringerBriefs in Electrical and Computer Engineering,
DOI 10.1007/978-3-319-32759-4_3

Table 3.1 Targeted major commercial wireless standards key specifications

Wireless standard		Frequency plan [MHz]		Modulation type	SNR_0 [dB]	RF signal BW/channel spacing [MHz]	Specified sensitivity [dBm]	Sensitivity at $NF_{RX} = 3$ dB [dBm]
		Downlink	Uplink					
GSM [4]	GSM 850	869 . . . 894.8	824 . . . 849.8	GMSK	9	0.2	−102	−109
	GSM 900	935 . . . 960	890 . . . 915					
	DCS 1800	1805 . . . 1880	1710 . . . 1785					
	PCS 1900	1930 . . . 1990	1850 . . . 1910					
UMTS [5]	I	2110 . . . 2170	1920 . . . 1980	QPSK on WCDMA support	−12 (at 12.2 kbps)	3.84/5	−117	–
	II	1930 . . . 1990	1850 . . . 1910					
	III	1805 . . . 1880	1710 . . . 1785					
LTE [6]	44 frequency bands	From 452.5 MHZ to 3800 MHZ in 44 frequency bands		QPSK/ 16QAM/ 64QAM on OFDM support (up to 2048 carriers)	−3 (at QPRSK)	1.4/3/5/	−106.2/−102.2/	–
						10/5/20/ 100 (with carrier aggregation)	−100/−97/	
							−95.2/−94 (Band35, QPSK)	
Bluetooth [7]		2402 . . . 2480		FSK	11	1	−70	−95
W-LAN IEEE 802.11b (DSSS) [8]	1/2 Mbit/s	2400 . . . 2485		DBPSK/ DQPSK	−4/−2	14/5	−80	−104/−102
	5.5/11 Mbit/s			CCK	9/11		−76	−91/−89
W-LAN IEEE 802.11 a, g, n (OFDM) [9, 10]	6/9 Mbit/s	2400 . . . 2485 (a, g, n)		BPSK	6/7	16.6/20	−82/−81	−93/−92
	12/18 Mbit/s			QPSK	10/12		–79/−77	−89/−87
	24/36 Mbit/s	5150 . . . 5350 and 5725 . . . 5825 (a, n)		16QAM	15/17		−74/−70	−84/−82
	48/54 Mbit/s			64QAM	21/23		−66/−65	−77/−75
W-LAN IEEE 802.11ac (160 MHz, OFDM) [11]	780/867 Mbit/s (up to 3.39 Gbit/s with four antennas)	5150 . . . 5350 and 5725 . . . 5825		256QAM	28/30	Up to 160 MHz	−50/−48	−61/−59

The direct conversion architecture (see Fig. 2.9) downconverts the RF signal directly to the baseband.

Since RF signal bandwidths are relatively small, up to a few hundreds of MHz (see Table 3.1), the signal frequencies after downconversion are also relatively small. Hence, circuits with negative feedback can be used to improve the baseband system linearity. Thus, as detailed in Sect. 7.2, all baseband blocks will contain opamps that sustain a feedback network embedding programmable passive elements (e.g., [3]).

In this way, the LF part of the SDRX will offer the flexibility required by the multi-standard operation, while maintaining a high linearity.

3.1.3 Different Burst Durations

Since digital communication is realized in bursts, the minimum frequency in the informational baseband signal spectrum, f_m, is given by the inverse of the duration of the transmitted burst.

Considering the maximum frequency in the baseband signal spectrum, f_M, from Table 3.1, regardless of the modulation scheme used, the signal spectral energy is bounded by the frequency limits f_m and f_M.

3.1.4 Different Modulation Schemes and Techniques

Multi-standard environment is also characterized by multiple modulation schemes and techniques in conveying the informational signal over the communication channel.

Also, for enhanced wireless link reliability, improved noise budget, and interference immunity, the standardization trends are focused on accommodating multiple modulation schemes and also on the possibility to change them dynamically. This is the case with IEEE standard families 801.11, 801.16, and 3GPP-LTE.

Hence, there is the need of a radio receiver capable of dynamically adjusting its characteristics such as it can demodulate the incoming RF burst. This requirement fits exactly the concept of software-defined radio.

3.2 Introducing the Minimum SNR for Proper Signal Demodulation

The front end must be able to downconvert the useful signal without hampering its electrical properties, such as the baseband processor is able to demodulate the information within a specified bit error rate (*BER*).

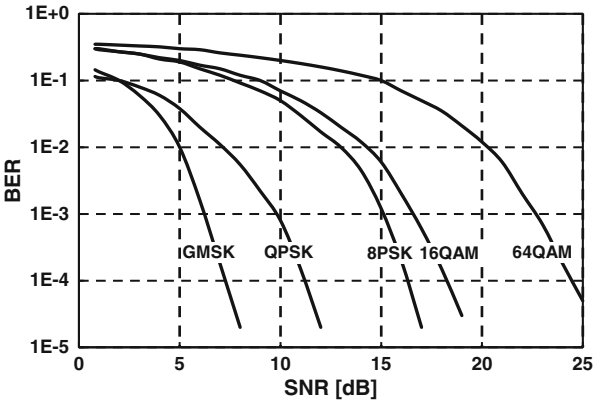

Fig. 3.1 BER versus SNR curves for GMSK, QPSK, 8PSK, 16QAM, and 64QAM

As the modulation becomes more complex, the bit rates (BRs) increase, and obviously, it becomes more difficult to properly demodulate the signal. This phenomenon can be quantified by analyzing the *BER* versus signal-to-noise ratio (SNR).

Based on the analysis presented in [12], in Fig. 3.1 the *BER* versus SNR for different modulation techniques is presented. As expected, higher SNRs are required to demodulate the signal within the same BER as the modulation number of bits per symbol increases.

Given the curves of Fig. 3.1, the systems that supports multiple modulation types (e.g., W-LAN) can (dynamically) choose the appropriate one according to the expected channel quality.

The informational digital stream was encoded using natural binary code. As more complex encoding algorithms are used, the effective SNR required to demodulate the signal within the same BER will decrease, until eventually reaching Shannon limit.

Increasing the SNR requirements is achieved at the cost of higher power consumption, by increasing the signal power, or at the cost of lowering the bandwidth.

In any case, there is a trade-off between power consumption and bit rate (BR). This can be mathematically expressed as follows:

$$\begin{cases} S = BR \cdot E_b \\ N = BW \cdot N_0 \end{cases} \tag{3.1}$$

where S and N are the receiver input signal and noise power, respectively, E_b is the energy per bit, and N_0 is the noise power density at the receiver input. In practice, $N_0 = k_B T \cdot F$—where F is the receiver noise factor.

Given (3.1), the maximum bit rate from the Shannon theorem (see (1.1)) can be rewritten as

$$BR \le BW\log_2\left(1+\frac{S}{N}\right) = BW\log_2\left(1+\frac{BR\cdot E_b}{BW\cdot N_0}\right) \tag{3.2}$$

Given (3.2), it results there is a minimum amount of signal energy required to transmit a bit:

$$E_b \ge N_0 \cdot \frac{2^{BR/BW}-1}{BR/BW} \tag{3.3}$$

Equation (3.3) shows the minimum E_b only depends on N_0 and on the coding scheme, through the BR/BW ratio. There are two extreme cases depending on the BR/*BW* ratio value.

Firstly, if BR/BW is very low (i.e., a large BW is used for a small *BR*), the limit from (3.3) is

$$E_b \ge N_0 \cdot \ln 2 \tag{3.4}$$

This case is exploited by spread spectrum systems (e.g., CDMA).

Secondly, for large BR/*BW* (e.g., for 64QAM), (3.3) becomes

$$E_b \ge N_0 \cdot \frac{2^{BR/BW}}{BR/BW} \tag{3.5}$$

Hence, the signal-to-noise ratio is

$$SNR = \frac{S}{N} = \frac{BR\cdot E_b}{BW\cdot N_0} \ge 2^{BR/BW} \tag{3.6}$$

As an example the SNR from (3.6) translates to 18-dB SNR for 64QAM. Of course, this theoretical limit translates to a few dB higher values in practical implementation.

> Hence, there is a minimum SNR at the receiver output, SNR_{out}, required for the digital demodulator to properly demodulate the useful signal. This minimum SNR_{out} value is further on denoted as SNR_0.

Based on the analysis presented in [12], the SNR_0 as a function of the *BER* has been determined for the basic modulation schemes. Table 3.1 notes the targeted standard signal modulation and the corresponding SNR_0 values.

> *The use of the concept "SNR_0" facilitates the calculation of the SDRX key electrical parameters by enabling a standard-independent approach.*

3.3 Deriving the SDRX Noise Figure

One of the most important parameters of a wireless receiver is its sensitivity, S_{RX}. The sensitivity is defined as the minimum input signal the receiver must be able to demodulate within the specified *BER*. Thus, when the input signal is at the sensitivity level, the SNR at the RX output (SNR_{out}) has to be above SNR_0 for a proper signal demodulation.

As each standard specifies a sensitivity level, given the useful signal RF bandwidth, BW_{RF}, the receiver NF, NF_{RX}, is calculated as [13]

$$NF_{RX} \leq S_{RX} - 10\log BW_{RF} - SNR_0 - N_0 \tag{3.7}$$

where $N_0 = k_B T = -174$ dBm/Hz represents the noise power spectral density at the antenna output for $T = 270$ K. In practice, an overhead to SNR_0 should be considered in (3.7), since the overall receiver SNR is degraded by multiple factors, not only by noise (e.g., imperfect impedance matching).

The receivers' NF specifications for all the wireless standards can be calculated based on (3.7) by accounting the specified sensitivity levels from Table 3.1. A low NF, as derived by (3.7), can be obtained at the expense of larger power consumption of the receiver. In order to maximize the link budget, most commercially available receivers push their sensitivity level toward smaller and smaller values by decreasing NF_{RX}.

Hence, a true SDRX must embed a receiver with a small NF (typically <3 dB) in order to be able to achieve a low enough sensitivity for all the targeted standards. Table 3.1 also comprises the required sensitivity levels, assuming $NF_{RX} = 3$ dB.

3.4 Generic Blocker Diagram

Besides the useful signal, other interferers and blockers can be present at the antenna input. The receiver's not perfectly linear transfer characteristic will produce intermodulation products that fall in band. These unwanted products cannot be disseminated from the useful signal causing SNR degradation.

An interferer is a signal which is modulated in the same way as the useful signal, while a blocker can have a different modulation or can just be a continuous wave (CW).

Depending on the relative frequency position of the interferer to the carrier, there are several types of interferers: co-channel interferers, adjacent channel interferers, and alternate interferers. Based on the same criteria, blockers can be categorized as either in band or out of band, as they occur in or out the receive band.

For each wireless communication standard, a *receiver blocker diagram* is specified. The diagram consists of all blockers and interferers present at the receiver's antenna input, under which influence the receiver must be able, still, to successfully

demodulate the wanted signal. This implies the SNR at the RX output, SNR_{out}, is above SNR_0, required to achieve the specified *BER* (see Table 3.1).

> In order to facilitate the multi-standard implementation, a new and efficient tool was developed, *the generic blocker diagram* [14] (see Table 3.2) *that offers a general perspective on the blockers and interferers present at the receiver input, independent of a particular wireless standard.*

The key advantage of this diagram is that it enables the designer to properly judge the optimal filter partitioning explained in Chap. 4. Nonetheless, it can be easily morphed to either of the envisaged standard blocker diagram.

Table 3.2 completes the Fig. 3.2 diagram by gathering for all the targeted standards blockers and interferers their explicit power levels, $P_{blk,\text{RF}}$, and frequencies, $f_{blk,}$. In Table 3.2 $\Delta f_{blk} = |f_{RF} - f_{blk,RF}|$ is the distance between the wanted signal and the interferer/blocker frequencies.

3.5 Blocker and Interferer Impact on the SDRX Linearity

Based on the targeted standard blocker diagram analysis, it results that there are two major issues due to blockers and interferers:

- The receiver output clipping, due to the large receiver gain requirements and the large difference between the useful signal and the blocker levels (i.e., typically greater than +40 dBc)
- Intermodulation distortions that fall in band, due to the receiver's not perfectly linear transfer characteristic

The receiver output clipping is handled through *optimal filter partitioning* [14] and *smart gain partitioning* [15], as is detailed in Chap. 4 and Chap. 5, respectively.

On the other hand, intermodulation distortions are unwanted products that potentially fall in band and cannot be disseminated from the useful signal. Thus, the wanted signal demodulation is affected due to the SNR degradation.

Further on, the analysis presented in this section focuses on finding the values for the figures of merit (FOMs) used in evaluating the radio receiver linearity performance: the second-order input-referred intercept point, *IIP*2, and third-order input-referred intercept point, *IIP*3. Figure 3.3 depicts how these parameters are being measured considering a four-port circuit.

Considering the notations from Fig. 3.3, it results through geometrical extrapolation that

$$\begin{cases} IIP2 = P_{IN} + P_{IM2} \\ IIP3 = P_{IN} + P_{IM3}/2 \end{cases} \tag{3.8}$$

Table 3.2 Interferers and blockers for the envisaged wireless standards

Category	ACI	AACI		Blocker						
Standard	B[a]	C[a]	D[a]	E[b]	F[b]	G[b]	H[b]	I[b]	J[b]	
GSM	Δf_{blk} [MHz]	0.2	0.4	≥0.6	0.6...0.8	0.8...1.6	1.6...3.2	≥3	≥3	20
	Level [dBc]	+18	+50	+58	+56	+56	+66	+76	+70	+99
UMTS	Δf_{blk} [MHz]	5	10	≥15	≥60	≥85	–	–	–	–
	Level [dBc]	+41	+38	+53	+67	+72	–	–	–	–
LTE	Δf_{blk} [MHz]	1.4/3/5/10	15	20	≥15	≥60	≥85		–	–
	Level [dBc]	+33	+30	+27	+56.2	+70.2	+85.2		–	–
802.11g on OFDM	Δf_{blk} [MHz]	20	40	≥60	≥240	–	–	–	–	–
	Level [dBc]	16...−1	32...15	32...15	−10 dB	–	–	–	–	–
802.11ac 160-MHz channels	Δf_{blk} [MHz]	160	≥160	≥320	≥480	–	–	–	–	–
	Level [dBc]	−9	9	9	−10 dB	–	–	–	–	–

[a]B is the adjacent channel interferer (ACI), and C and D signals are the first, second, and so on; alternate adjacent channel interferer (AACI)
[b]E, F G, H, I, and J are blockers

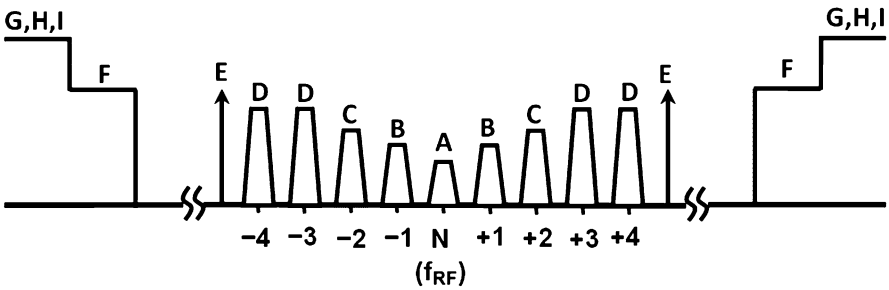

Fig. 3.2 Receiver generic blocker diagram [14]. *A* is the received useful signal, *B* is the adjacent channel interferer (ACI), and *C* and *D* signals are the first, second, and so on; alternate adjacent channel interferer (AACI); the signals from *E* represent the blockers

3.5.1 Finding the SDRX IIP2

While receiving, the RF input power may change significantly because of the reception of unwanted blockers/interferers. Due to the receiver's even-order distortions, the received signal DC offset component will change. This *dynamic offset* effect upsets the received signal demodulation, especially if the envisaged modulation concentrates a large part of the symbol spectral power at low frequencies.

This is the case for older standards like GSM, as the latest wireless standards (e.g., W-LAN) use modulation schemes that do not carry information at low frequencies. The figure of merit quantizing the analog front-end's second-order distortions is the second-order intercept point, *IIP*2.

Figure 3.4 depicts a generic situation for the effects of the second-order distortions on the receiver output. Basically, next to the very small useful RF signal, the receiver is exposed to a very large blocker.

As the blocker presence or, respectively, moment of appearance is completely orthogonal to the RF signal broadcasting, due to second-order nonlinearity, the receiver output DC level will be larger or, respectively, change.

Following the representation of Fig. 3.4, from immediate calculation using (3.8), *IIP*2 is given by

$$IIP2 \geq 2 \times P_{blk} - P_{in} + \left(P_{BB} - P_{offset}\right) \tag{3.9}$$

where P_{blk} is the power of the blocker at the receiver input, P_{in} and P_{BB} represent the useful RF signal power at the receiver input and output, and P_{offset} is the DC level of the second-order intermodulation product.

Equation (3.9) imposes a restriction on the maximum level for the offset component stemming from the second-order intermodulation:

$$P_{BB} - P_{offset} \geq SNR_0 \tag{3.10}$$

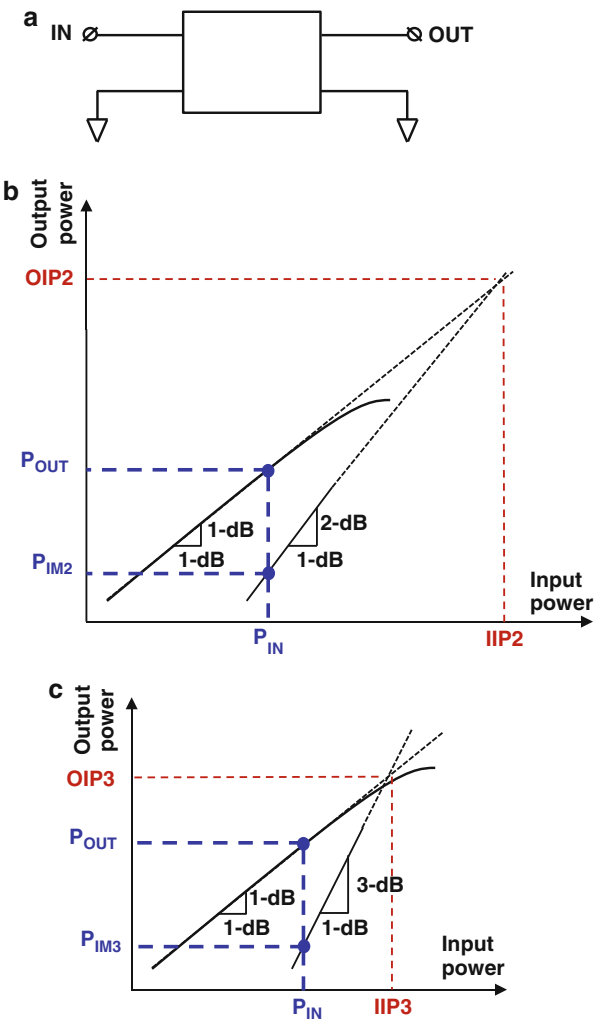

Fig. 3.3 (**a**) Four-port circuit, (**b**) IIP2, and (**c**) IIP3

In practice, the designer should consider an extra margin in (3.10) as the real SNR is degraded by multiple factors, not only the second-order distortions.

Thus, (3.9) translates to

$$iIP2 = 2 \times P_{blk} - P_{in} + SNR_0 \tag{3.11}$$

Based on the specified blocker diagram analysis for the targeted standards, it results that the worst-case scenario is the GSM standard which requires a receiver $IIP2$ of $+46$ dBm.

The second-order and, in general, even-order distortions can be dramatically reduced, ideally canceled, by using *differential circuits*. In order to achieve such

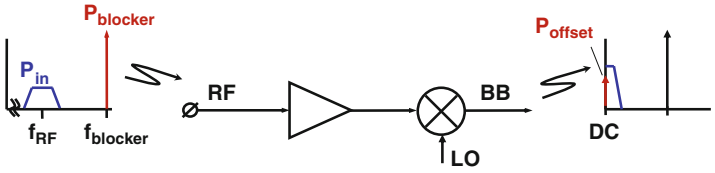

Fig. 3.4 DC offset generation due to receiver second-order nonlinearity

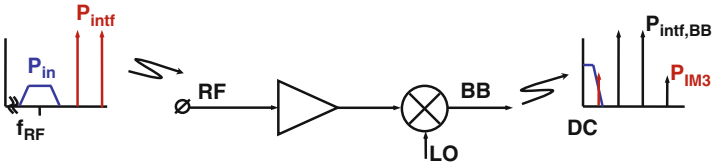

Fig. 3.5 Third-order interference intermodulation impact on downconverted signal

high *IIP*2 values, the receiver should be implemented by fully differential blocks.

3.5.2 Finding the SDRX IIP3

Due to the interferer and blocker presence at the receiver antenna input, the receiver's not perfectly linear transfer characteristic will produce intermodulation products that fall in band. These unwanted products cannot be disseminated from the useful signal and cause an effective SNR degradation, as shown by Fig. 3.5.

For most wireless receivers, given the fully differential circuit implementation, the dominant nonlinear contribution comes from the third-order coefficient of power series expansion of their transfer characteristic.

The maximum in-band level of the third-order intermodulation product, P_{IM3}, must be smaller than the useful RF signal level with SNR_0:

$$P_{IM3} \leq P_{in,\mathrm{BB}} - SNR_0 \tag{3.12}$$

In practice, supplementary headroom to SNR_0 should be considered, since the overall receiver SNR is degraded by multiple factors, not only by the downconverted spurs.

Given (3.12), the receiver IIP3, $IIP3_{\mathrm{RX}}$, must meet the condition

$$iIP3_{\mathrm{RX}} \geq P_{\mathrm{int}} + \frac{P_{\mathrm{int}} - P_{IM3}}{2} \tag{3.13}$$

where P_{int} is the power per interferer of two blockers that cause the in-band third-order distortion.

In Fig. 3.5 the blockers are considered to be continuous waves (CWs), since this is the worst-case scenario. However, if they are modulated, a correction factor that depends on the modulation type can be applied to the resulting intermodulation product [16].

A special case is represented by OFDM signals. An OFDM signal comprises frequency orthogonal subcarriers [12]. Receiver nonlinearity leads to formation of bogus signals in band due to subcarrier intermodulation. The figure of merit in evaluating the third-order intermodulation products thus formed is the composite triple beat (CTB). As is pointed out in [17], the worst case for the CTB product level is found in the center band of the OFDM signal spectrum:

$$CTB \ \ [\text{dB}] \leq -2(IIP3_{\text{RX}} - P_{in}) + 1.74 \tag{3.14}$$

where P_{in} is the OFDM signal power in all the carriers.

Hence, in order for the digital back end to be able to still demodulate properly the wanted signal, the CTB level must be smaller than the useful RF signal level per carrier with SNR_0:

$$CTB \leq P_{in} - 10\log N - SNR_0 \tag{3.15}$$

where N represents the number of OFDM subcarriers.

In (3.14) SNR_0 represents the corresponding SNR headroom of the OFDM subcarrier modulation.

Given (3.14) and (3.15), it results that in order to avoid destructive inter-carrier intermodulation, the $IIP3_{\text{RX}}$ must meet the following condition:

$$IIP3_{\text{RX}} \geq \frac{1}{2}(P_{in} + 10\log N + SNR_0 + 1.74) \tag{3.16}$$

Each wireless standard specifies a set of particular intermodulation conditions. By analyzing all the targeted standards, the receiver $IIP3$ specifications were derived using (3.13) or (3.16).

The results are summarized in Table 3.3.

3.6 LO Phase Noise Impact on the Receiver

While receiving, due to the LO signal phase noise, the receiver downconverts a fraction of the signals located in the adjacent channels. Hence, at the mixer output, the downconverted unwanted signals will overlap on top of the useful signal, thus decreasing the SNR.

The total receiver in-band SNR in the presence of phase noise, SNR_{total}, is given by

Table 3.3 Multi-standard wireless receiver *IIP*3 specifications

Standard	Intermodulation conditions	Receiver *IIP*3 [dBm]	
		Equation	Value
GSM	P_{int} @ −45 dBm, P_{in} @ −101 dBm	(3.13)	−19
UMTS	P_{int} @ −46 dBm, P_{in} @ −104 dBm	(3.13)	−23
LTE	P_{int} @ −46 dBm, P_{in} @ −85 dBm (in 20 MHz)	(3.13)	−28
Bluetooth	P_{int} @ −39 dBm, P_{in} @ −64 dBm	(3.13)	−18.5
W-LAN 802.11b, g (DSSS)	P_{int} @ −39 dBm, P_{in} @ −74 dBm (DQPSK −11Mbit/s)	(3.13)	−12
W-LAN 802.11 (OFDM)	Interferer intermodulation: P_{int} @ sensitivity, P_{in} @ AACI, all modulations	(3.13)	−32
	Blocker intermodulation: P_{blk} @ −10 dBm, P_{in} @ −42 dBm, BPSK −6 Mbit/s	(3.13)	+8.5
	Subcarrier intermodulation: P_{in} @ −10 dBm, $N = 52$ carriers, 20 MHz 802.11g	(3.16)	+10
	Subcarrier intermodulation: P_{in} @ −30 dBm, $N = 484$ carriers, 160 MHz 802.11ac	(3.16)	+14

$$(SNR_{total})^{-1} = (SNR_{in})^{-1} + PN \cdot P_{blk}/P_{in} \tag{3.17}$$

where PN is the LO phase noise at the blocker frequency and P_{blk} is the power level of the unwanted signal picked up by the LO signal noise tail; all quantities are in watt or watt/Hz.

Knowing the required SNR that allows a proper demodulation of the received signal, denoted SNR_0 (see Table 3.1), and the receiver blocker diagram of Fig. 3.2, (3.17) allows the calculation of the frequency synthesizer's phase noise requirements during the receive phase.

3.7 Conclusion

The analysis presented in this chapter was focused on finding the key electrical requirements of the SDRX (see Fig. 2.9) targeting compatibility with the major commercial wireless standards (see Table 3.1).

Thanks to the standard-independent systematic approach, the values for the key SDRR electrical specifications (i.e., NF_{RX}, $IIP2_{\mathrm{RX}}$, and $IIP3_{\mathrm{RX}}$) were determined.

Of course, a true SDRX has to be robust enough to adjust dynamically its performance (e.g., NF_{RX}, $IIP3_{\mathrm{RX}}$) depending on the communication burst particularities, as detailed by Chap. 5. Nonetheless if a SDRX targets compatibility with the standards from Table 3.1, it must meet the electrical specifications determined in this analysis.

To conclude, the presented analysis constitutes the starting point in building the SDRX.

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Chapter 4
Optimal Filter Partitioning

4.1 Defining the Channel Selection Strategy

The most important issue due to blockers and interferes is the risk of the receiver output clipping. This is due to (1) the large receiver dynamic range and, thus, gain imposed by the low sensitivity levels (see Table 3.1) and (2) the large difference in power levels between the blockers and the RF useful signal (see Table 3.2). Hence, the receiver selectivity is critical and a thorough analysis of the channel selection strategies is required [1].

The RF path filtering resides mainly on the antenna band-pass filter, placed before the LNA (see Fig. 2.9). However, the filter has a large enough band pass to allow the channel reception (e.g., more than 240 MHz for W-LAN IEEE 802.11g). Thus, the interferers and blockers, located within the antenna filter pass band, get transferred unattenuated to the LNA input. Due to the wideband nature of the multi-standard RF front end, it can be assumed there is no additional filtering on the RF path. Hence, the SDRX front end typically benefits from a fairly limited RF selectivity, although there are recent efforts aimed at performing channel selection directly at RF (e.g., [2–5]). However, baseband filtering remains a challenging task.

In order to relax baseband filtering, typically the downconversion mixer incorporates, in its output stage, a first-order low-pass filter. Thus, the relative interferer/blocker power after downconversion, $P_{blk,\mathrm{BB}}$, is given by

$$P_{blk,BB} = P_{blk,RF} - 10log\left[1 + \left(\triangle f_{blk}/f_{-3dB,MIX}\right)^2\right] \tag{4.1}$$

where $f_{-3\mathrm{dB,MIX}}$ is the mixer LPF −3-dB frequency. The $f_{-3\mathrm{dB,MIX}}$ is made programmable to mitigate the multi-standard requirements. In order to optimize the chip area, the filter bandwidth is set to the smallest AACI-D frequency (see Table 3.2).

S. Spiridon, *Toward 5G Software Defined Radio Receiver Front-Ends*,
SpringerBriefs in Electrical and Computer Engineering,
DOI 10.1007/978-3-319-32759-4_4

The subsequent baseband filtering can be performed either:

(a) Fully in the analog domain, by using a channel selection anti-aliasing filter to reduce the interferer and blocker level below the useful signal level with SNR_0 and then using a VGA, to optimally load the ADC
(b) Partly in both domains, by low-pass filtering the mixer output and amplifying the outcome for the final conversion to the digital domain
(c) Fully in the digital domain, by converting the MIX output to digital without any subsequent low-pass filtering
(d) Fully in the digital domain, by direct sampling the LNA output

The trade-off between the LPF order and ADC resolution and speed is the key point in the above channel selection strategies.

To this aim we defined and introduced the figure of merit, FOM_{CHS}, metric that accounts the LPF area, A_{LPF}, and the ADC power consumption, P_{ADC}. The FOM is focused on these two major parameters of the receiver design and ignores second-order aspects, such as the ADC area, the VGA, and the digital filter area and power consumption.

Firstly, given the low bandwidths of the targeted standards and the low noise of wireless receivers, the LPF area is directly linked to the amount of integrated capacitance and thus to the LPF order, n_{LPF}:

$$A_{\mathrm{LPF}} \tilde{} n_{\mathrm{LPF}} \tag{4.2}$$

Secondly, the ADC power consumption, P_{ADC}, can be described by considering the figure of merit in evaluating the ADC performance FOM_{ADC} or the ADC energy consumption per conversion cycle. Thus, P_{ADC} is given by [6]

$$P_{\mathrm{ADC}} = FOM_{\mathrm{ADC}} \cdot f_S \cdot 2^n \tag{4.3}$$

where n represents the ADC effective resolution and f_S its sampling rate. Today, state-of-the-art ADCs with moderate speeds exhibit a FOM_{ADC} of about 10 fJ/conv., while wideband ADCs are in the 100 fJ/conv. range [7]. By combining (4.2) and (4.3), the FOM_{CHS} in evaluating the channel selection options results

$$FOM_{CHS} = (1 + n_{\mathrm{LPF}}) \cdot P_{\mathrm{ADC}} \tag{4.4}$$

where a unity was added to n_{LPF} to account for the case of the fully digital channel selection, which does not use a filter.

4.2 Deriving the ADC Specifications

The ADC converter specifications of resolution and speed are determined such as the SNR at the receiver output is maintained after the signal conversion from the analog to the digital domain. The ADC effective resolution is given by

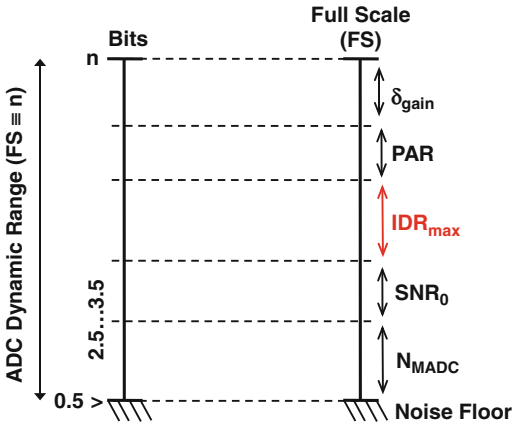

Fig. 4.1 Nyquist ADC dynamic range partitioning

$$n = (SNR_{\text{ADC}} - 1.76)/6.02 \tag{4.5}$$

where SNR_{ADC} is the ADC effective dynamic range.

Regardless on how the filtering is performed, the ADC dynamic range is partitioned like in Fig. 4.1.

Firstly, it is required the ADC noise, N_{ADC}, is lower than the noise at the receiver output, $N_{RX\ out}$, with a certain noise margin, N_{MADC}, such as the ADC impact on the overall receiver NF is minimized:

$$N_{\text{ADC}} \leq N_{RX\ \ out} \ - \ N_{ADCM} \tag{4.6}$$

Considering the worst-case scenario for noise, when $NF_{RX} = 3$ dB, and assuming the ADC contribution to this value is equivalent to 0.5 dB, it results that the NF of the receiver chain excluding the ADC, NF_{RX-ADC}, is only 2.5 dB. Thus, N_{MADC} is about 10 dB, as

$$N_{\text{MADC}} = -10\log\left[1 - 10^{(NF_{\text{RX-ADC}} - NF_{\text{RX}})/10}\right] \tag{4.7}$$

Secondly, the ADC converter must not be overloaded. A headroom margin should be considered from the ADC full scale, FS. The margin value is set by the VGA gain resolution.

Thirdly, the ADC dynamic range should provide enough headroom for the received signal peak, given its peak-to-average ratio (PAR). For the basic modulation schemes, the *PAR* is 3 dB, while for OFDM signals, it is in the order of 15 dB.

Please note that the *PAR* is the received signal PAR, not necessarily the wanted signal PAR! In case the blocker is larger than the wanted signal, then the *PAR* is the blocker signal PAR.

Finally, the ADC dynamic range should compensate for the residual blocker level after low-pass filtering, *IDR*.

The key element in finding the optimal filtering is $IDR_{\max}$ or the amount of residual blockers/interferers that loads the ADC.

$IDR_{\max}$ is given by

$$IDR_{\max} = \max\left\{20\log\left(1+10^{P_{blk,i}/20}\right) \underset{P_{blk,i}>>0\text{dBc}}{\cong} P_{blk,i}\right\} \tag{4.8}$$

with $P_{blk,i}$ representing the interferer power at the block i output and $i=$ VGA for baseband filtering scenarios (a) and (b), $i=$ MIX for (c), and $i=$ LNA for (d).

For completing the calculation of $IDR_{\max}$, one must determine first $P_{blk,i}$. Figure 4.2 represents the blockers at the various SDRX block outputs, and $P_{blk,i}$ results as

$$\begin{cases} P_{blk,LNA} = P_{blk,RF} \\ P_{blk,MIX} = P_{blk,LNA} - 10\lg\left[1+\left(\Delta f_{blk}/f_{-3dB,MIX}\right)^2\right] \\ P_{blk,LPF} = P_{blk,VGA} = P_{blk,MIX} - 10\lg\left[1+\left(\Delta f_{blk}/BW_{LPF}\right)^{2n_{LPF}}\right] \end{cases} \tag{4.9}$$

where BW_{LPF} is the LPF bandwidth and is set to half the RF bandwidth, as for every zero-IF receiver (see Table 3.1). For a multi-standard receiver, BW_{LPF} is programmable.

Figure 4.3a depicts $IDR_{\max}$ computed considering the blocker diagram from Table 3.2. As can be seen, complete analog channel selection (i.e., $IDR_{\max}=0$ dB) is achieved for a fifth-order LPF, while if no filter is used (i.e., $n_{\text{LPF}}=0$ or direct sampling), the increase in the residual blocker level is substantial: in the case of GSM standard, 31 dB between a second-order LPF bi-quad and no LPF and 39 dB between second-order LPF and direct sampling.

Hence, to ensure the signal demodulation is done within the specified *BER*, corresponding to SNR_0 (see Table 3.1), SNR_{ADC} should meet the following condition:

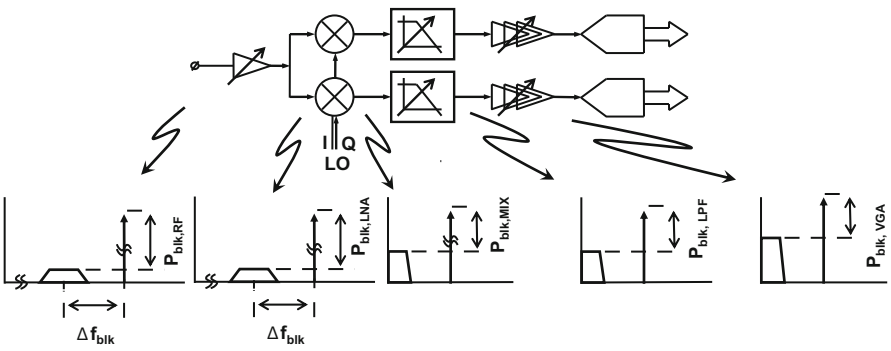

Fig. 4.2 Relative blocker power over the RX chain (an example)

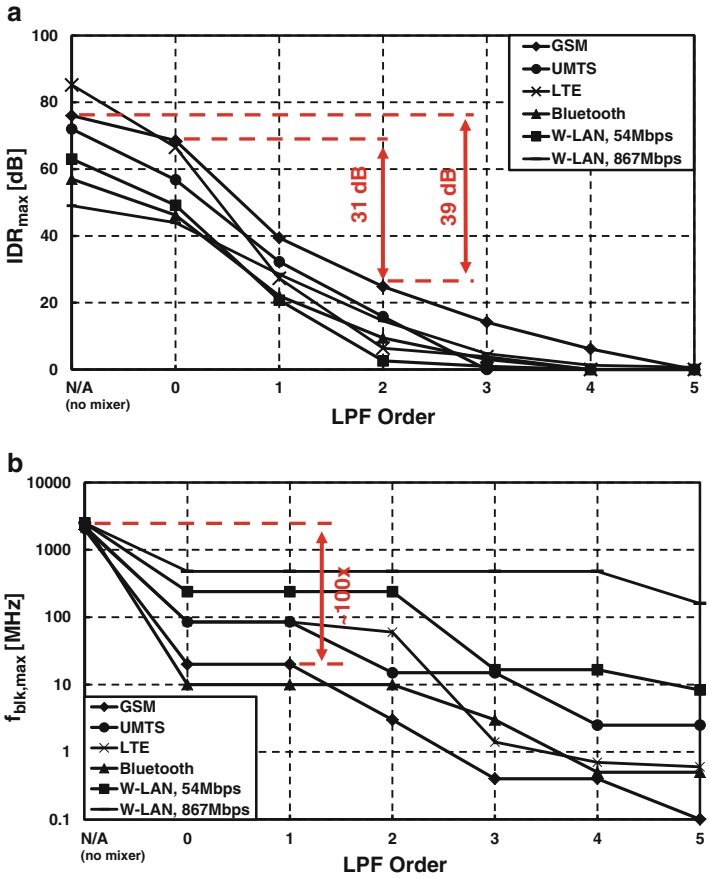

Fig. 4.3 (**a**) $IDR_{\max}$ vs. n_{LPF} and (**b**) $f_{blk,\max}$ vs. n_{LPF}

$$SNR_{\mathrm{ADC}} \geq SNR_0 + \Delta A_{VGA} + PAR + N_{M\mathrm{ADC}} + IDR_{\max} \ \ [dB] \tag{4.10}$$

For oversampled ADC converters, their dynamic range is increased proportionally with the oversampling ratio, *OSR*: for each doubling of the sampling rate above the Nyquist rate, the ADC dynamic range increases by 3 dB. Thus, the ADC effective number of bits, n, can be reduced by means of oversampling to

$$n \geq (SNR_0 - \Delta A_{\mathrm{VGA}} + PAR + N_{MADC} + IDR_{\max} + 10\log OSR)/6 \tag{4.11}$$

To avoid the ADC destructive interferer/blocker aliasing [8], the ADC f_S must be chosen larger than the highest unfiltered interferer/blocker frequency, $f_{blk,\max}$, such as

$$f_{blk,\mathrm{alias}} = f_S - f_{blk,\max} \geq BW_{\mathrm{RF}} \tag{4.12}$$

where $f_{blk,\text{alias}}$ is the frequency at which the blocker is aliased and BW_{RF} is the effective signal bandwidth (see Table 3.1).

Figure 4.3b plots $f_{blk,\max}$ as a function of the LPF order. When the interferers/blockers are completely filtered out in the analog domain, $f_{blk,\max} = BW$. Thus, $f_S \geq 2BW$. Otherwise, the aliased interferers/blockers must be filtered to below the useful signal level with SNR_0, for proper digital demodulation.

Assuming the digital filter has a pass band equal to BW and its order is $n_{\text{LPF,dig}}$, it results in

$$f_{blk,\text{alias}} \geq BW\left[10^{\left(SNR_0+P_{blk,\text{LPF}}\right)/10}-1\right]^{\left(0.5/n_{\text{LPF,dig}}\right)} \tag{4.13}$$

For a fair comparison, the same $n_{\text{LPF,dig}}$ is taken for all targeted standards. Since high-order digital filters are susceptible to limit cycles, we restrict to $n_{\text{LPF,dig}} = 10$.

By using (4.13) in (4.12), f_S can be immediately derived. Based on (4.10), (4.12), and the data from Fig. 4.3, the receiver ADC specifications of resolution and speed are determined. The results are presented in Fig. 4.4 and in Table 4.1.

The Fig. 4.4 plots are standard independent, and for simplicity for direct sampling systems, the ADC f_S is 5 GHz for all standards (exception is the 5-GHz W-LAN band where a 12-GS/s ADC would be required). The plots show that filter-less solutions require, as expected due to the large blocker levels, very high-dynamic range ADCs.

Moreover, direct sampling systems require wideband ADCs; for example, in the case of GSM, the SDRX needs a 17-bit ADC sampling at about 5 GHz that is 250 times higher than if a mixer would be employed and 1250 times higher than if a second-order LPF bi-quad would be used.

Table 4.1 summarizes the ADC specifications for a fourth-order LPF. The most demanding ADC requirements result for W-LAN 802.11ac standard, which requires a 10-bit, 670-MS/s. ADC.

4.3 The Optimal Trade-Off Between LPF Order and ADC Specifications

By using (4.5) and (4.12) in (4.3), P_{ADC} is computed for $FOM_{\text{ADC}} = 100$ fJ/conv. in Fig. 4.5. Again, due to the large blocker levels, the increase in ADC power consumption between the direct sampling system and a second-order LPF SDRX is dramatic. The plot in Fig. 4.5 reveals an increase of more than 400 times between the case of a mixer-based SDRX and a direct sampling system and an increase of more than 300,000 times if a mixer-based SDRX employing a second-order LPF is used rather than a mixer-less SDRX.

Finally, the optimum filter partitioning corresponds to the LPF order that renders the lowest FOM_{CHS} set by (4.4). Due to the high $n_{\text{LPF,dig}}$, f_S is very close to the limit

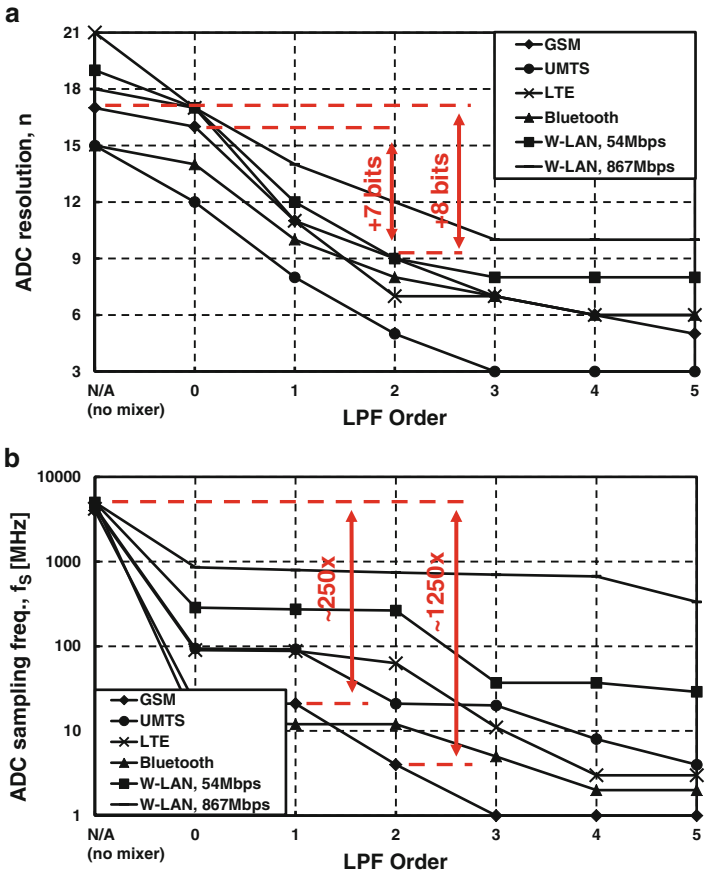

Fig. 4.4 (**a**) ADC resolution and (**b**) ADC sampling frequency vs. LPF order

set by (4.12) for all the targeted standards. Using (4.10) into (4.5), FOM_{CHS} from (4.4) is plotted as a function of n_{LPF} (see Fig. 4.6).

Thus, through the FOM_{CHS} *plotted in* Fig. 4.6*, this standard-independent approach addresses in one single plot the key trade-off in next-gen radio front-end design.*

First of all, the plots from Fig. 4.6 show an LPF order larger than 4 brings no further benefit, as the lowest FOM_{CHS} is achieved for $n_{\mathrm{LPF}} = 4$.

Secondly, Fig. 4.6 shows a complete digital channel selection ($n_{\mathrm{LPF}} = 0$) is not really an alternative, as the present CMOS processes available cannot provide,

at reasonable area and power consumption costs, such high performance for the ADC. For instance, considering the GSM standard, an ADC with a resolution higher than 17 bit at a speed of more than 20 MSamples/s is required to handle the J blocker of Table 3.2 at an estimated power consumption larger than 100 mW

Table 4.1 Nyquist rate ADC specifications for a system embedding a fourth-order LPF

Standard		Modulation	PAR [dB]	IDR_{max} [dBc]	ADC specs.	
					n [bits]	f_S [MS/s]
GSM		GMSK	0	6.2	5	1
UMTS		WCDMA	10	0	3	8
LTE (OFDM)		Up to 64QAM	10	0	7	10
Bluetooth		FSK	0	0	5	2
W-LAN (IEEE 802.11b,g DSSS)	1 Mbit/s	DBPSK	3	0	4	20
	2 Mbit/s	DQPSK			5	
	5.5 Mbit/s	DQPSK			5	
	11 Mbit/s	DQPSK			5	
W-LAN (IEEE 802.11g OFDM)	6 Mbit/s	BPSK	10	0	6	40
	9 Mbit/s	BPSK			6	
	12 Mbit/s	QPSK			6	
	18 Mbit/s	QPSK			6	
	24 Mbit/s	16QAM			7	
	36 Mbit/s	16QAM			7	
	48 Mbit/s	64QAM			8	
	54 Mbit/s	64QAM			8	
W-LAN (IEEE 802.11ac 160-MHz channel, OFDM)	780 Mbit/s	256QAM	12	1.2	10	670

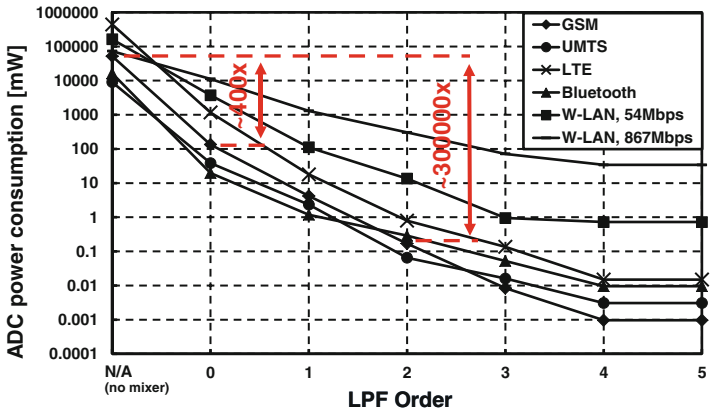

Fig. 4.5 ADC power consumption vs. LPF order

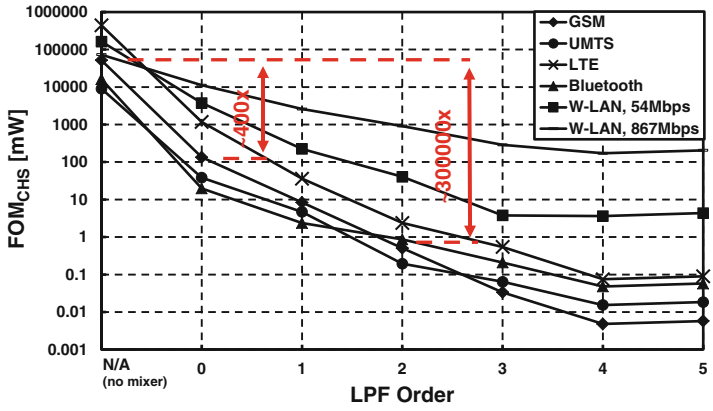

Fig. 4.6 FOM_{CHS} vs. n_{LPF}

(i.e., 400 times larger than if a mixer would be employed and 300,000 times larger than if after the mixer there is a second-order LPF).

Thirdly, a complete analog channel selection requires an LPF order of 5 (see Fig. 4.3a at $IDR_{\max} = 0$ dB). This channel selection option allows for the minimum ADC power consumption, as both the ADC sampling rate and resolution are kept at the lowest possible values, but at the expense of the LPF area.

Hence, an LPF order of 4 trades off optimally the receiver area and power consumption.

4.4 Conclusion

The introduction of the generic blocker diagram in Sect. 3.4 allowed a standard-independent approach in evaluating the filter partitioning for channel selection in the multi-standard receiver. Moreover, the FOM_{CHS} defined in Sect. 4.1 allowed the evaluation of the trade-off between the LPF area and the ADC power consumption in one single plot. Figure 4.6 revealed almost parallel plots for the envisaged standards. This confirms the filter partitioning analysis and the FOM_{CHS} validity and its usage in the context of a multi-standard implementation.

Also, the Fig. 4.6 plots showed that an LPF order larger than 4 brings no further benefit for the targeted standards channel selection.

Nonetheless, depending on which is the parameter to be optimized, either the receiver power consumption or its area, the baseband filter partitioning strategy can range between a complete analog channel selection ($n_{\mathrm{LPF}} = 5$) and a fully digital approach employing a mixer ($n_{\mathrm{LPF}} = 0$). And an interesting conclusion is direct sampling SDRXs are still about two orders of magnitude away from a mixer-based solution in terms of power consumption.

However, the rate at which ADC power efficiency improves (i.e., about ten times every 4 years [9]) may make them attractive on medium term.

Thus, this general character of the presented filter partitioning methodology fits best a true SDRX implementation.

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Chapter 5
Smart Gain Partitioning for Noise: Linearity Trade-Off Optimization

The SDRX is exposed to extreme conditions specific to the wireless environment. Since long time the receiver must be able to cope with multiple transmitters. Hence, the received signal comprises not only the wanted signal but also additional blockers and interferers, generated by adjacent transmitters. Also, the receiver can be located either far away or close to the wanted transmitter, can have direct visibility of the transmitter, or can be isolated from it. Thus, the wanted signal may suffer additionally due to reflections and multipath propagation.

All these possibilities can be summarized by a few extreme cases that serve as guidelines to designing any radio receiver focused on wireless mobile communications [1]:

(a) The wanted signal is very weak, or, equivalently, its received power is equal to the SDRX sensitivity.
(b) The wanted signal is weak, and it is surrounded by blockers and interferers according to the specified blocker diagrams (see Fig. 3.2 and Table 3.2).
(c) The wanted signal is strong, and its level is well above the SDRX sensitivity level.

To accomplish the envisaged goal of finding the optimal gain–noise–linearity partitioning strategy, Sect. 5.1 introduces a standard-independent systematic approach in the analysis of the three receive scenarios and explains why and how the receiver NF, NF_{RX}, and IIP3, $IIP3_{\mathrm{RX}}$, vary with the receiver RF front-end gain. Subsequently, Sect. 5.2 defines the receiver gain settings and sets for each of them the NF and IIP3 values. Further on, Sect. 5.3 presents the novel gain partitioning strategy tailored toward SDRXs that optimally mitigates the extreme reception conditions specific to the wireless environment.

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5.1 Proposed Gain–Noise–Linearity Partitioning Strategy

A versatile receiver must be able to mitigate all three presented scenarios by trading-off between its noise and linearity performance for maintaining a signal-to-noise-and-distortion ratio (SNDR) at its output, SNR_{out}, larger than SNR_0. Thus, not only the receiver gain, A_{RX}, will be a function of the received input power but also its NF and IIP3. This concept is described by Fig. 5.1.

In the first case, (a), when the wanted signal is very weak, the receiver noise performance is critical; thus, its noise figure must be at its lowest value.

For the second scenario, (b), given the weak input signal, still a good noise performance is required; however, the linearity constraint becomes critical. A higher linearity becomes mandatory to keep intermodulation at low levels.

Third, for scenario (c), the stronger wanted signal level makes the receiver linearity performance important while completely relaxing its noise requirements. The receiver must have a linear enough response to guarantee the SNR_{out} is within the limits required for a proper signal demodulation.

In order to ensure optimal performance, the multi-standard receiver embeds two blocks with adjustable gain (i.e., the LNA and the VGA), as featured in Fig. 2.9. Firstly, the LNA makes the RF front-end gain programmable. As discussed, for optimal performance the LNA should allow at least three gain steps (i.e., at least one for each receive scenario) to keep the mixer properly loaded. Secondly, there is a need for an additional variable gain block after the channel selection filter, to ensure the ADC is optimally loaded (i.e., close to its full-scale (FS) range to fully make use of the available dynamic range).

The low sensitivity levels (see Table 3.1) impose a large dynamic range requirement for the SDRX. Assuming the interferers/blockers have been completely removed by the wideband LPF with variable bandwidth, the receiver maximum gain, $A_{RX\ max}$, needed to reach the specified sensitivity level, is given by

$$A_{RX\ \ max} = FS_{ADC} - S_{RX} - \Delta \tag{5.1}$$

where FS_{ADC} is the ADC input full-scale (FS) range and Δ is the margin required to avoid the ADC overloading.

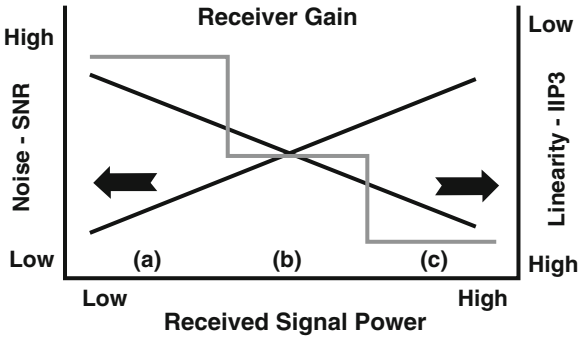

Fig. 5.1 Noise–linearity trade-off setting the gain of a wireless receiver

The margin Δ is set by the VGA gain resolution and the PAR of the received signal:

$$\Delta = \Delta A_{\mathrm{VGA}} + PAR \tag{5.2}$$

The highest gain value $A_{\mathrm{RX\ max}}$ is set when no blockers are present and the signal is at the sensitivity level. Table 5.1 notes the receiver signal conditioning path maximum gain requirement for the key wireless standards of the moment calculated based on (5.1) for a 1-V FS ADC and for a receiver matched to 100 Ω with $\Delta A_{\mathrm{VGA}} = 1$ dB.

Table 5.1 The receiver gain range requirements

Standard		$A_{\mathrm{RX\ max}}$ [dB]	A_{HF} [dB]	$A_{\mathrm{VGA\ max}}$ [MHz]
GSM		110	34. . .46	76. . .64
UMTS		134	34. . .46	100. . .88
LTE (20-MHz channel)		87	34. . .46	53. . .41
Bluetooth		101	22. . .34	79. . .69
W-LAN IEEE 802.11b,g (DSSS)	1 Mbit/s	107	34. . .46/ 22. . .34	73. . .61/ 85. . .73
	2 Mbit/s	105		71. . .59/ 83. . .71
	5.5 Mbit/s	94		60. . .48/ 72. . .60
	11 Mbit/s	92		58. . .46/ 70. . .58
W-LAN IEEE 802.11b (OFDM)	6 Mbit/s	89	34. . .46/ 22. . .34	55. . .43/ 67. . .55
	9 Mbit/s	88		44. . .42/ 66. . .54
	12 Mbit/s	86		52. . .40/ 64. . .52
	18 Mbit/s	85		51. . .39/ 63. . .51
	24 Mbit/s	70		46. . .34/ 58. . .46
	36 Mbit/s	79		45. . .33/ 57. . .45
	48 Mbit/s	73		39. . .27/ 51. . .39
	54 Mbit/s	72		38. . .26/ 50. . .38
W-LAN IEEE 802.11ac (160-MHz channels, OFDM)	780 Mbit/s	54	34. . .46/ 22. . .34	20. . .8/ 32. . .20
	867 Mbit/s	53		19. . .7/ 31. . .19

The large receiver dynamic range must be partitioned over the two gain blocks, the LNA and the VGA. As wireless communications are burst communications, the VGA gain change doesn't have to be continuous. Hence, for each received burst, the LNA and the VGA gain are constant.

5.2 Defining the SDRX Gain Settings

First of all, for the HF part, a novel approach is considered for the noise–linearity–gain partitioning. For optimum performance (i.e., robustness to interferers), the multi-standard receiver HF part gain is made programmable by enabling the LNA gain to change in *four* discrete steps. Since the mixer can also provide gain, the combined LNA and mixer gain represent the RF front-end receiver gain, A_{HF}.

More than four ranges can be considered for A_{HF}. Nonetheless this may limit the RF front-end bandwidth, due to the inherent parasitic elements associated with a larger circuit complexity running at high frequencies.

In order to optimally partition the receiver dynamic range in a log scale, the *four* receiver gain settings are obtained by successive divisions by 4 from the maximum $\mathrm{A_{HF}}$, $A_{\mathrm{HF\ max}}$:

$$A_{\mathrm{HF}\ i} = \begin{cases} A_{\mathrm{HF\ max}}, & i = 4 \\ A_{\mathrm{HF}\ i+1}/4, & i = 1,\ 2,\ 3 \end{cases} \tag{5.3}$$

Since the A_{HF} gain step is 4, each $A_{\mathrm{HF}\ i}$ discrete value can be chosen within a 12-dB interval, as shown in Fig. 5.2.

The A_{HF} gain settings are determined by the noise–linearity trade-off. The higher the A_{HF}, the lower is the receiver baseband block noise contribution. However, $A_{\mathrm{HF\ max}}$ is limited by linearity constraints. Since the interferer/blocker level present at the receiver input may be considerably larger than the useful signal (e.g., $\geq$+70 dBc; see Table 3.2), a too large A_{HF} value can clip the receiver RF

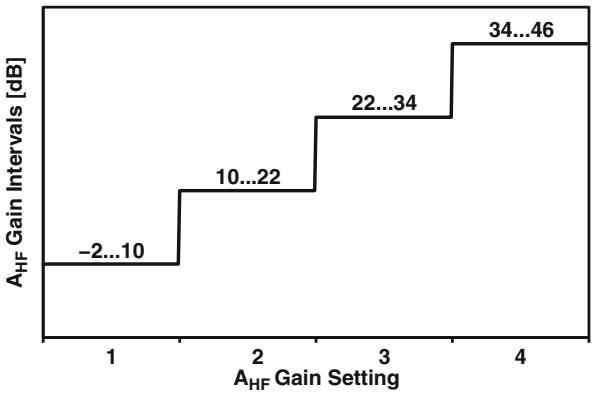

Fig. 5.2 A_{HF} gain intervals

front-end output. It also leads to poor linearity for the LNA or the mixer circuits. Thus, the receiver $A_{\mathrm{HF\ max}}$ value is limited to 200 or 46 dB.

The NF_{RX} and $IIP3_{\mathrm{RX}}$ adjust accordingly depending on the A_{HF} gain setting:

(a) *High A_{HF} gain results in low NF_{RX}.* The A_{HF} gain for this scenario, $A_{\mathrm{HF\ 4}}$, is larger than 50 (34 dB) and is limited at 46 dB (200). The targeted value for the minimum receiver NF is 3 dB. For this gain setting, the receiver linearity requirement is not really a constraint by a hard standard specification (see Table 3.3). Nonetheless, extrapolating the GSM standard requires a clean reception in the presence of a +54-dBc interferer while receiving the useful signal at its sensitivity level or −110 dBm. It results that a receiver IIP3 of −21 dBm guarantees 3.5 dB of margin, according to (3.13).

(b) *Average A_{HF} gain implies average NF_{RX} and $IIP3_{\mathrm{RX}}$.* For this range of input powers, two A_{HF} gain settings are foreseen to enhance the receiver robustness to blockers/interferers: $A_{\mathrm{HF\ 2}}$ and $A_{\mathrm{HF\ 3}}$. The higher gain range, $A_{\mathrm{HF\ 3}}$, is bounded within 34 and 22 dB, while the lower gain range, $A_{\mathrm{HF\ 2}}$, assumes a front-end gain between 22 and 10 dB. Still, the $A_{\mathrm{HF\ 2}}$ and $A_{\mathrm{HF\ 3}}$ exact values are set by (5.3) from $A_{\mathrm{HF\ 4}}$.

The higher gain configuration ($A_{\mathrm{HF\ 3}}$) is used for all the standards requiring a dynamic range smaller than 100 dB and a NF_{RX} below 10 dB (but larger than 5 dB). A NF_{RX} of 8 dB satisfies the requirements with a margin of 2 dB. Also, this gain setting must satisfy the $IIP3_{\mathrm{RX}}$ specifications of Table 3.3. The $IIP3_{\mathrm{RX}}$ is set to −9 dBm, ensuring a margin of 3 dB in the worst case (the GSM standard).

The $A_{\mathrm{HF\ 2}}$ RF front-end gain setting is used to enhance the receiver robustness. The received input signal is already large enough not to require such a low *NF*. Hence, assuming a degradation of 1 dB in the *NF* for 1 dB of gain reduction compared with the $A_{\mathrm{HF\ 3}}$ gain case, it results the receiver NF is 20 dB.

The same approach is used for determining the linearity performance: 1 dB degradation in the *IIP*3 for 1 dB of gain increase compared with the smallest receiver gain setting ($A_{\mathrm{HF\ 1}}$) *IIP*3. In anticipation, this renders an $IIP3_{\mathrm{RX}}$ target of +3 dBm.

(c) *Low A_{HF} gain implies a high $IIP3_{\mathrm{RX}}$.* The lowest receiver gain range, represented by $A_{\mathrm{HF\ 1}}$, spans between −2 and 10 dB. For this gain setting, the receiver must be able to satisfy the +14 dBm linearity requirements of W-LAN (see Table 3.3). By taking 1 dB margin, the $IIP3_{\mathrm{RX}}$ is +15 dBm.

On the other hand, NF_{RX} is not important in this case and is taken 32 dB, assuming 1 dB/dB slope of NF degradation versus A_{HF} decrease.

Table 5.2 summarizes the $IIP3_{\mathrm{RX}}$ and NF_{RX}, while Fig. 5.3 presents the $IIP3_{\mathrm{RX}}$ and NF_{RX} versus A_{HF}.

The remaining gain control is made via the VGA. The VGA gain is set such as it loads optimally the ADC converter.

Given the targeted *NF* numbers of Table 5.2, Table 5.1 notes the required receiver RF front-end gain for the reception of a minimal useful signal. Depending on the

Table 5.2 $IIP3_{RX}$ and NF_{RX} as a function of the A_{HF}

		NF_{RX} [dB]		$IIP3_{RX}$ [dBm]	
A_{HF} gain setting	A_{HF} gain range [dB]	Spec	Target	Spec	Target
1	−2…10		32	+14	+15
2	10…22	–	20	–	+2
3	22…34	(10)[a]	8	−12	−9
4	34…46	3	3	(−24.5)[a]	−21

[a]The specifications in brackets are not hard specs

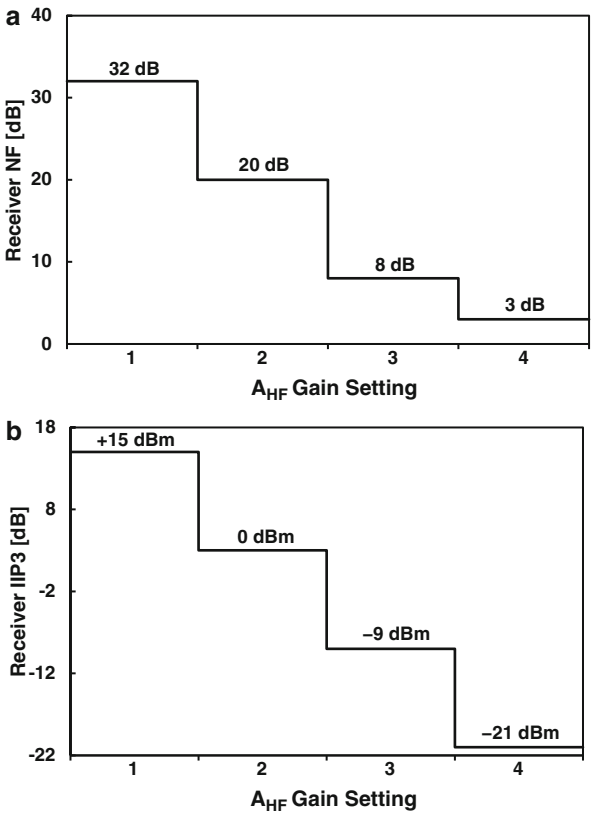

Fig. 5.3 (**a**) NF_{RX} and (**b**) $IIP3_{RX}$ versus A_{HF} gain settings

targeted NF, A_{HF} is chosen between the highest gain settings ($A_{HF\,4}$ and $A_{HF\,3}$). Thus, the maximum VGA gain, $A_{VGA\ max}$ (also noted in Table 5.1), results in

$$A_{VGA\ \ max} = A_{RX\ \ max} - A_{V\ \ HF} \tag{5.4}$$

Since a back-off, equal to the VGA gain step, ΔA_{VGA}, is required to avoid the ADC overloading, the effective VGA dynamic range is

$$VGA\ \ dynamic\ \ range = A_{\mathrm{VGA\ \ max}} + \Delta A_{\mathrm{VGA}} \tag{5.5}$$

Given the data from Table 5.1 and assuming $\Delta A_{\mathrm{VGA}} = 1$ dB, it results that a VGA with a maximum 100 dB dynamic range is enough to cover the receiver gain requirements for all the targeted standards.

5.3 Proposed Gain Partitioning Algorithm

The SDRX gain partitioning strategy is conceived to:

1. Optimize the SNR at the receiver output, SNR_{out}.
2. Ensure robustness to interferers/blockers by selecting the minimum RF front-end gain that ensures $SNR_{out} > SNR_0$.

The SNR_{out} that allows the proper demodulation of the received signal within the specified BER must satisfy the condition

$$SNR_{out} = SNR_{in} - NF_{\mathrm{RX}} \geq SNR_0 \tag{5.6}$$

where SNR_{in} is the SNR at the receiver input:

$$SNR_{in} = P_{in} - 10\log BW - N_0 \tag{5.7}$$

The proposed gain partitioning algorithm optimizes SNR_{out} by choosing the smallest A_{HF} that satisfies condition (5.6). Thus the probability of overloading the receiver RF front-end output due to the presence of the unwanted interferers/blockers is minimized.

The input power range for which the condition (5.6) is met is calculated by replacing SNR_{in} from (5.7) into (5.6):

$$SNR_{out} = P_{in} - 10\log BW - N_0 - NF \geq SNR_0 \tag{5.8}$$

Since NF_{RX} is a function of A_{HF} and the RF front end has *four* gain settings, there will be *four* values for P_{in} at which the left term of the inequality (5.8) is reaching its minimum equal to SNR_0.

Hence, in order to optimize the receiver robustness to blockers/interferers, an additional margin, SNR_M, is taken for the larger gain settings, where noise performance is not critical (i.e., 3 dB for $A_{\mathrm{HF\ 3}}$, 6 dB for $A_{\mathrm{HF\ 2}}$, and 9 dB for $A_{\mathrm{HF\ 1}}$ as noted in Table 5.3):

$$SNR_{out} = P_{in} - 10\log BW - N_0 - NF \geq SNR_0 + SNR_M \tag{5.9}$$

Table 5.3 comprises the input power ranges for each of the RF front-end gain settings for all the envisaged wireless standards, and Fig. 5.4 depicts SNR_{out} versus

Table 5.3 The receiver gain range requirements

A_{HF} versus input power range						
A_{HF} gain setting			4	3	2	1
SNR_M			0	3	6	9
Input power range [dBm]	GSM		−109 to −101	−101 to −86	−86 to −71	> −71
	UMTS		−117 to −109	−109 to −94	−94 to −79	> −79
	LTE		−106 to −98	−98 to −83	−83 to −68	> −68
	Bluetooth		−95 to −87	−87 to −72	−72 to −57	> −57
	W-LAN IEEE 802.11b,g (DSSS)	1 Mbit/s	−104 to −96	−96 to −81	−81 to −66	> −66
		2 Mbit/s	−102 to −94	−94 to −79	−79 to −64	> −64
		5.5 Mbit/s	−91 to −83	−83 to −68	−68 to −53	> −53
		11 Mbit/s	−89 to −81	−81 to −66	−66 to −51	> −51
	W-LAN IEEE 802.11g (OFDM)	6 Mbit/s	−95 to −87	−87 to −72	−72 to −57	> −57
		9 Mbit/s	−94 to −86	−86 to −71	−71 to −56	> −56
		12 Mbit/s	−92 to −84	−84 to −69	−69 to −54	> −54
		18 Mbit/s	−90 to −82	−82 to −67	−67 to −52	> −52
		24 Mbit/s	−87 to −79	−79 to −64	−64 to −49	> −49
		36 Mbit/s	−83 to −75	−75 to −60	−60 to −45	> −45
		48 Mbit/s	−79 to −71	−71 to −56	−56 to −41	> −41
		54 Mbit/s	−78 to −70	−70 to −55	−55 to −40	> −40
	W-LAN IEEE 802.11ac (160MHz channels, OFDM)	780 Mbit/s	−61 to −50	−50 to −38	−38 to −23	> −23
		867 Mbit/s	−59 to −48	−48 to −36	−36 to −21	> −21

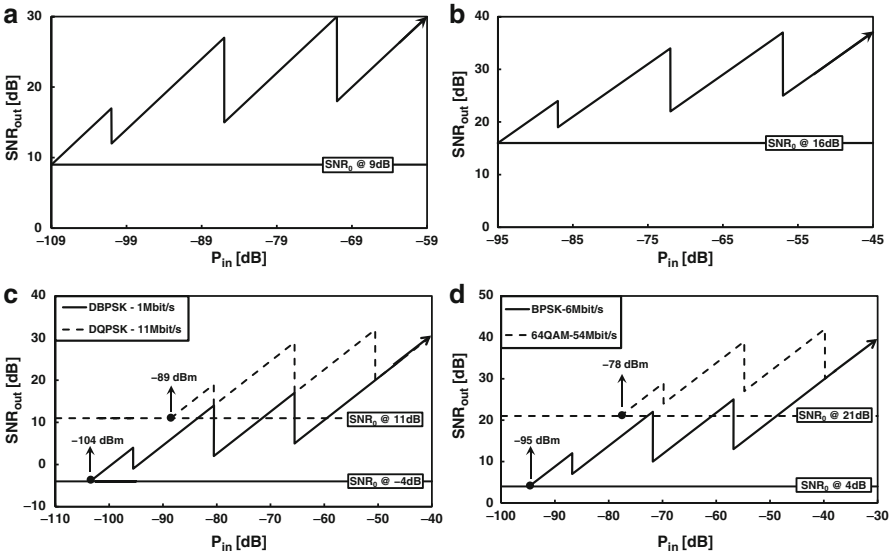

Fig. 5.4 SNR_{out} versus P_{in}: (**a**) GSM, (**b**) Bluetooth, (**c**) W-LAN 802.11b,g (DSSS), and (**d**) W-LAN 802.11g (OFDM)

the received input power for a selection of the envisaged wireless standards of Table 3.1.

In Fig. 5.4 the RF front-end gain is set according to the conditions used to derive (5.8) (i.e., $NF_{\mathrm{RX}} = 3$ dB corresponds to $A_{\mathrm{HF}\,4}$), while the VGA gain is calculated to ensure the ADC optimal loading:

$$A_{\mathrm{VGA}} = A_{\mathrm{RX}} - A_{\mathrm{HF}} \tag{5.10}$$

5.4 The Automated Gain Control Loop

Before each communication burst, the received sample amplitude must be evaluated. Based on this measurement, the SDRX gain must be set such as its output falls within the ADC FS.

The gain partitioning is realized by the automated gain control (AGC) loop. This involves a dialogue between the baseband processor (DSP) and the receiver. By measuring the receiver signal strength indicator (RSSI), the DSP makes a good estimate of the input signal power and can adjust the receiver's gain accordingly.

The main drive in the gain setting algorithm is the SNR optimization: the algorithm should always shoot for the lowest possible A_{HF} gain setting, which doesn't overload the chain and ensures a SNR_{out} larger than SNR_0.

Also, the AGC algorithm must set the receiver gain within the allocated time frame, the guard band. In order to optimize the AGC operation speed, the algorithm should aim for a minimum number of changes in the RF front-end gain.

Changing A_{HF} requires the LPF output to settle in order for the ADC to receive a valid signal, while the VGA gain changing can be done much faster.

5.5 Conclusion

Through a first-order, system-level analysis, a standard-independent methodology was developed for finding the optimal gain partitioning strategy for SDRXs embedding analog signal conditioning.

The proposed gain partitioning is based on splitting the receiver gain between an RF front end embedding four gain settings and a high-dynamic range VGA. As the NF_{RX} and $IIP3_{\mathrm{RX}}$ change with A_{HF}, the multi-standard receiver is able to optimally leverage the extreme receive conditions specific to the wireless environment. The proposed gain partitioning algorithm optimizes SNR_{out} for each of the targeted standards by selecting the minimum A_{HF} that guarantees proper signal demodulation (see Fig. 5.4).

Given the generic algorithm it is based on, the proposed solution fits best a true SDRX implementation.

Reference

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Chapter 6
SDRX Electrical Specifications

6.1 Electrical Specifications

In previous chapters, the SDRX specifications have been derived based on an in-depth standard-independent analysis suited for manual analysis. Table 6.1 compiles the multi-standard receiver electrical specifications.

The electrical specifications from Table 6.1 need to be partitioned among the SDRX building blocks. However, as a first step, they will be partitioned between the SDRX high-frequency (HF) part (i.e., the LNA and the gm stage of the mixer, if any) and its low-frequency (LF) part (i.e., the mixer transimpedance amplifier, the LPF, and the VGA) [1].

6.2 Noise Partitioning

The overall receiver noise budget, represented by the receiver NF, NF_{RX}, is partitioned between the receiver LF and HF parts. According to Friis' formula, the receiver global NF, NF_{RX}, can be calculated from the individual contributions of HF and LF parts:

$$NF_{\mathrm{RX}} = 10\log\left(F_{\mathrm{HF}} + \frac{F_{\mathrm{LF}} - 1}{A_{\mathrm{HF}}^2}\right) \ \mathrm{dB} \tag{6.1}$$

where F_{HF} and F_{LF} represent the noise factors of the HF part and LF part, respectively, and $A_{\mathrm{HF}} = A_{\mathrm{LNA}} \cdot A_{\mathrm{MIX}}$ is the voltage gain of the receiver's HF front end and it is equal to the product between the LNA gain, A_{LNA}, and the mixer gain, A_{MIX}.

Equation (6.1) shows that the LF part noise contribution is reduced by the RF front-end gain. Hence, the noise partitioning assumes the largest part of the receiver

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Table 6.1 SDRX electrical specifications[a]

A_{HF} range	4	3	2	1	Unit
RF frequency	0.7...6 GHz				GHz
Baseband BW	0.1...160 MHz				MHz
A_{HF}[b]	200	50	12.5	6.25	–
	40	28	16	4	dB
NF_{RX}	3	8	(20)	(32)	dB
$IIP3_{RX}$	(−21)	−9	(+2)	+14	dBm
LPF order	4				
VGA gain range	0...84				dB
ADC full scale	1				Vpd

[a]The specifications in brackets are not hard specs
[b]The A_{HF} values are chosen in the middle of the RF front-end gain ranges of Table 5.2

NF is due to the RF front-end. Thus, knowing $NF_{HF} = 10\ \log(F_{HF})$, the LF part noise figure, NF_{LF}, results as:

$$NF_{LF} = 10\log\left[1 + A_{HF}^2\left(10^{NF_{RX}/10} - 10^{NF_{HF}/10}\right)\right] \tag{6.2}$$

Both the receiver HF and LF part noise figures can be expressed as a function of their equivalent noise resistance:

$$NF_{HF} = 10\log\left(1 + \frac{4R_{n\ HF}}{R_S}\right) \quad NF_{LF} = 10\log\left(1 + \frac{4R_{n\ LF}}{R_S}\right) \tag{6.3}$$

where $R_{n\ HF}$ is the receiver RF front-end equivalent noise resistance, $R_{n\ LF}$ is the receiver baseband chain equivalent noise resistance, and R_S is the antenna's resistance.

The noise partitioning is most critical when the receiver input signal is at its lowest value. Hence, A_{HF} is at its highest value $A_{HF\ max} = 40$ dB to keep $NF_{RX} = 3$ dB.

For this case, Fig. 6.1 plots the NF_{LF}, $R_{n\ HF}$, and $R_{n\ LF}$ vs. NF_{HF}, $R_{n\ HF}$, and $R_{n\ LF}$, respectively, which represent the link between the receiver HF part power consumption, determined by $R_{n\ HF}$, and LF part area, determined by $R_{n\ LF}$.

Because of the large $A_{HF\ max}$, $R_{n\ LF}$ is much larger than $R_{n\ HF}$ (i.e., a few orders in magnitude). Thus, the receiver HF part consumes much more power than its LF part to achieve the same noise when referred at the receiver input.

Therefore, in order to reduce the receiver power consumption, the smart noise partitioning allows the receiver HF part to contribute more to the overall NF_{RX}. This translates to choosing a larger $R_{n\ HF}$, while allowing a bit smaller $R_{n\ LF}$. Nonetheless, a smaller $R_{n\ LF}$ translates to a larger receiver area, as larger capacitances must be chosen to keep the same IF bandwidth.

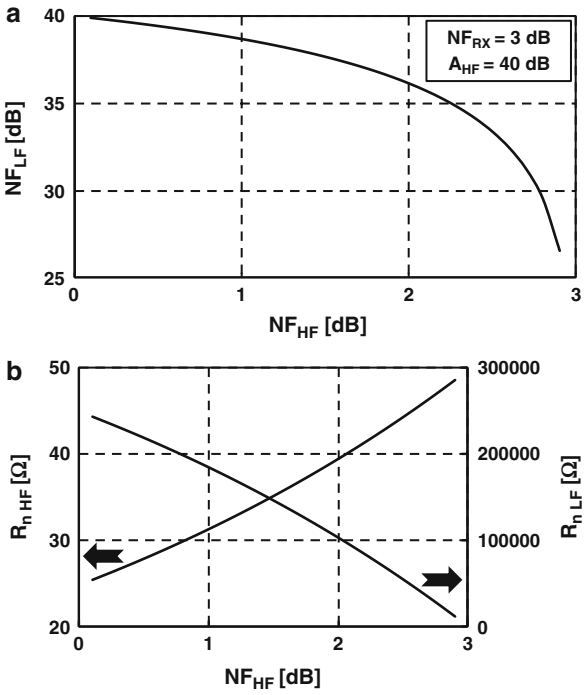


Fig. 6.1 (**a**) NF_{LF} vs. NF_{HF}; (**b**) $R_{n\ \mathrm{LF}}$ vs. NF_{HF} ($NF_{\mathrm{RX}} = 3$ dB and $A_{\mathrm{HF}} = 40$ dB)

The plots from Fig. 6.1b represent the key trade-off that shapes the noise partitioning: the trade-off between the receiver power consumption, represented by $R_{n\ \mathrm{HF}}$, and its area, set by $R_{n\ \mathrm{LF}}$.

Hence, in the case where the minimum receiver NF is required, NF_{HF} is accounting 2 dB, while the baseband chain and the ADC share the remaining 1 dB from the 3 dB global NF_{RX}. This translates to a NF_{LF} of about 33 dB.

For the situation where $NF_{\mathrm{RX}} = 8$ dB, the noise partitioning assumes 5 dB comes from the RF part ($NF_{\mathrm{HF}} = 5$ dB) and half from the baseband chain. For the remaining two smallest A_{HF} gain settings, a 1 dB per dB degradation with the front-end gain for NF_{RX} is assumed.

Figure 6.2 plots the NF_{HF} and NF_{LF} vs. the A_{HF} gain settings. Equivalently, by using (6.2), and knowing NF_{HF} and NF_{LF}, both $R_{n\ \mathrm{HF}}$ and $R_{n\ \mathrm{LF}}$ can be calculated. Figure 6.3 reveals $R_{n\ \mathrm{HF}}$ and $R_{n\ \mathrm{LF}}$ for the four A_{HF} settings.

The smart noise partitioning of the noise budget between NF_{HF} and NF_{LF} accounts for the degradation of only NF_{HF} while keeping the same NF_{LF}. This potentially allows power saving in the front-end RF part, since its noise requirements are relaxed with the A_{HF} decrease.

While for the baseband part, the same NF_{LF} is foreseen regardless of the RF front-end gain setting. This is beneficial since power reduction would affect the LF part building block linearity, and since it opens the possibility of an optimized design.

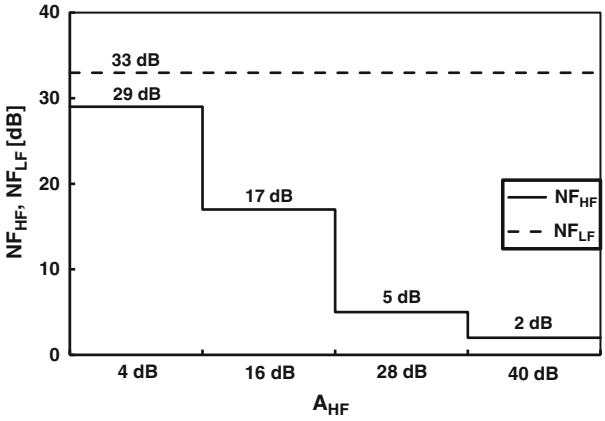
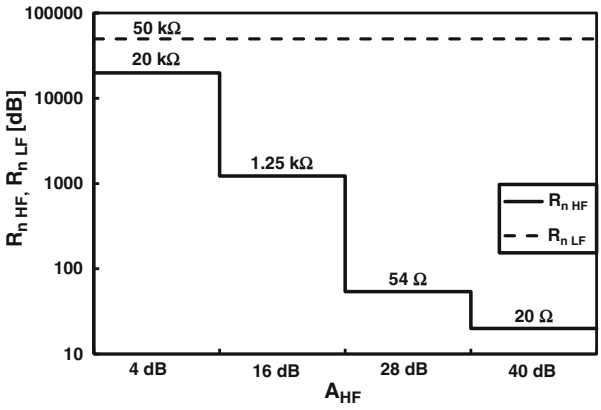


Fig. 6.2 NF_{HF} and NF_{LF} vs. A_{HF}

Fig. 6.3 $R_{n\ \mathrm{HF}}$ and $R_{n\ \mathrm{LF}}$ vs. A_{HF}



6.3 Linearity Partitioning

The linearity partitioning strategy tackles the receiver overall *IIP*3, $IIP3_{\mathrm{RX}}$, budget split between its HF and LF parts. Hence, it calculates $IIP3_{\mathrm{RX}}$ as a function of the RF front-end *IIP*3, $IIP3_{\mathrm{HF}}$, and of the baseband chain *IIP*3, $IIP3_{\mathrm{LF}}$:

$$\frac{1}{IIP3_{\mathrm{RX}}^2} = \frac{1}{IIP3_{\mathrm{HF}}^2} + \frac{A_{\mathrm{HF}}^2}{IIP3_{\mathrm{LF}}^2} \tag{6.4}$$

where all *IIP*3 values are measured in V.

I would like to stress out that in (6.4), $IIP3_{\mathrm{RX}}$ represents the figure of merit for the SDRX distortion budget, while $IIP3_{\mathrm{HF}}$ and $IIP3_{\mathrm{LF}}$ represent corresponding figure of merits for the HF and LF part distortion budgets. Even if the distortion mechanisms can be different for the HF and LF parts (e.g., the HF part is exposed to high-level blockers that intermodulate

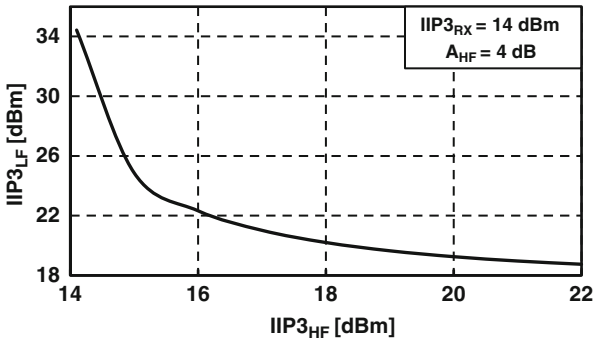


Fig. 6.4 $IIP3_{HF}$ vs. $IIP3_{LF}$

in band, while the LF part is facing multi-carrier signals that also intermodulate in band), the distortion budget represents the amount of distortion signal that overlaps and thus corrupts the wanted signal. Thus, using IIP3 to quantify the amount of distortion leads to a simple and clear way to distribute the distortion contributions alongside the RX chain.

Linearity constraints are important at high signal levels, when A_{HF} is small. For this case (i.e., $A_{HF} = 4$ dB), by using (6.4), Fig. 6.4 plots $IIP3_{LF}$ vs. $IIP3_{HF}$ for $IIP3_{RX} = 14$ dBm.

Like expected, the plot reveals that for a more linear RF front end, we can tolerate more nonlinearity from the LF chain. However, given the high operation frequency, a more linear RF front-end burns more power to achieve the distortion contribution when compared with the LF part blocks.

Moreover, as presented in Sect. 7.2 given the low baseband signal bandwidth (i.e., maximum 160 MHz for W-LAN 802.11 ac among envisaged standards), the LF part circuits can very efficiently make use of negative feedback based on low-power feedback amplifiers to achieve a high linearity.

Hence, the smart linearity partitioning accounts equal contributions from the receiver HF part and from its LF part when referred to the input (i.e., $IIP3_{LF}/A_{HF}$). Thus, it results in

$$IIP3_{HF} = IIP3_{LF}/A_{HF} = IIP3_{RX} \cdot \sqrt{2} \tag{6.5}$$

The smart gain partitioning foresees the $IIP3_{RX}$ reduction at a rate of 1 dB/dB with the A_{HF} increase. Similarly to the noise partitioning, the smart linearity partitioning allows the degradation of only the RF front-end linearity performance (i.e., $IIP3_{HF}$). Hence, given the (6.5), Fig. 6.5 reveals $IIP3_{HF}$ and $IIP3_{LF}$ for the four A_{HF} settings. And again the same conclusion arises: since the LF part linearity performance is the same regardless of A_{HF} (i.e., $IIP3_{LF} = +21$ dBm), the LF part block design is simplified, and it can be optimized by designing dedicated building blocks.

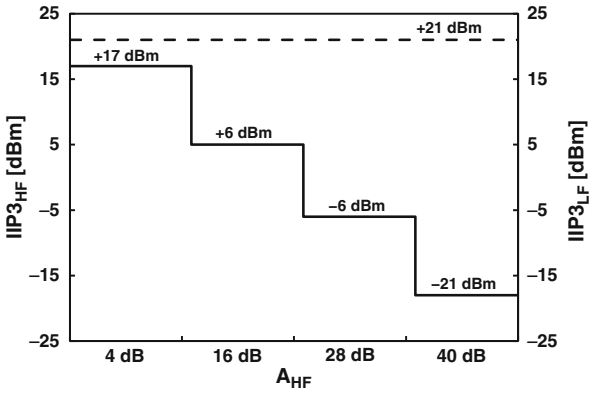


Fig. 6.5 $IIP3_{HF}$ and $IIP3_{LF}$ vs. A_{HF}

6.4 Conclusion

This chapter analyzed the noise–linearity breakdown between the HF part and LF part of a direct conversion SDRX. By using a systematic approach of the noise–linearity partitioning, power saving is enabled in the HF part through changing the SDRX HF part noise and linearity performance with its RF front-end gain. While for the LF part, the analysis revealed the performance can be kept the same to allow power optimization through dedicated circuit design.

The general characteristic of the proposed smart noise–linearity breakdown methodology fits best a true SDRX receiver implementation.

Reference

1. S. Spiridon, C. Dan, M. Bodea, Smart noise-linearity breakdown in homodyne multi-standard radio receivers, in *Proceedings of the International Conference on Advances in Cognitive Radio COCORA 2012* (Chamonix/Mont Blanc, France, May 2012), pp. 46–49

Chapter 7
A System-Level Perspective of Modern Receiver Building Blocks

7.1 SDRX HF Part Building Blocks

7.1.1 The Wideband Low-Noise Amplifier

Usually, since the *RF* signal picked up by the antenna is very small, a low-noise amplifier (LNA) is required to boost its level. The signal level rise should be done with both minimum distortions and minimum degradation of signal-to-noise ratio (*SNR*). As the amplifier operates at microwave frequencies, the LNA input impedance value must be matched to the antenna resistance, usually 50 or 100 Ω, to achieve the maximum power transfer. The LNA intrinsic noise performance is described by its noise figure, NF_{LNA}. The LNA effective noise figure, $NF_{LNA\ eff}$, taking into account the LNA input impedance matching to the antenna resistance, is given by

$$NF_{LNAeff} = NF_{LNA} - IL \tag{7.1}$$

where *IL* is the insertion loss given by the ratio of power passed to LNA from the antenna to the total power received by the antenna.

Since the analysis focuses on CMOS receivers, the designer choice of the gain-stage configurations is restricted either to the common gate (CG) or to the common source (CS). The common collector (CC) configuration is ruled out because it does not provide voltage gain.

Although both topologies offer the same intrinsic voltage gain, the CG stage suffers a noise penalty as its g_m is locked by input impedance matching constraints. Because the CG-stage input resistance is fixed to approximately $1/g_m$, the designer loses one degree of freedom, being unable to tweak anymore the circuit noise performance.

Figure 7.1 presents the commonly used topologies for a multi-standard LNA (biasing not shown) described in various publications and summarized in [1, 2].

S. Spiridon, *Toward 5G Software Defined Radio Receiver Front-Ends*,
SpringerBriefs in Electrical and Computer Engineering,
DOI 10.1007/978-3-319-32759-4_7

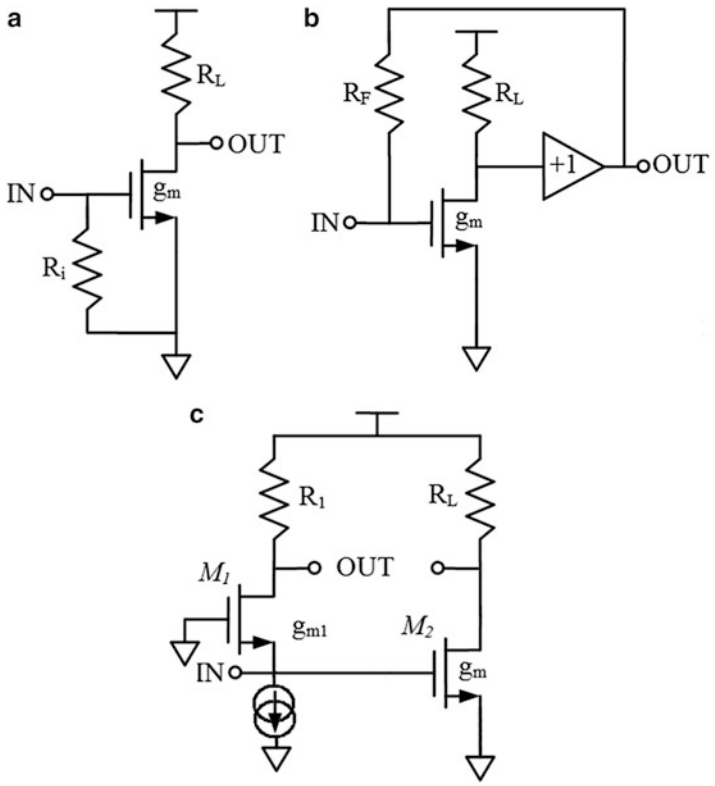


Fig. 7.1 Commonly used wideband LNA topologies (nmos-only stage is preferred to maximize the impedance matching frequency range)

All three configurations can get input impedance to the antenna resistance matching over a large frequency range (this is why the nmos-only input stage was shown), and, as expected, all are CS amplifiers. All key parameters of the presented topologies (gain, minimum noise factor, and the input impedance) are summarized in Table 7.1.

The LNA of Fig. 7.1a trades off noise figure for wideband input impedance matching, as all the noise originating from matching resistor R_i, connected from input to ground, overlaps on top of the input signal.

Due to impedance matching constraints, R_i is equal to the antenna resistance, R_S, thus making this LNA topology minimum noise figure larger than 3 dB.

Figure 7.1b topology uses negative feedback to set the input impedance to the appropriate value, given by

$$Z_{in} = R_F/(1 + A_V) \tag{7.2}$$

with $A_V = g_m R_L$ representing the LNA's voltage gain, where g_m is the input-stage transconductance and R_L the load resistance.

Table 7.1 Key parameters of the low-noise amplifier

Parameter		Equation		Preferred bias
Gain	Av	Fig. 7.1a, b	g_mR_L	Constant g_mR
		Fig. 7.1c	$2g_mR_L$	
Noise	$F_{\min}$ ($NF = 10 \log F$)	Fig. 7.1a	$\geq 2 + const/g_m$ ($\geq$3 dB)	Constant g_mR
		Fig. 7.1b	$1 + R_F/R_S = 1/(1 + A_v)$	
		Fig. 7.1c	$1 + R_S/R_1$ (@ large g_m)	
Input impedance	Z_{in} ($Z_{in} = R_S$)	Fig. 7.1a	$1/R_i$	Constant g_m
		Fig. 7.1b	$R_F/(1 + A_v)$	or
		Fig. 7.1c	$1/g_{m1}$	Constant g_mR

Due to the wideband nature of the structure, its A_V is constant over a wide frequency range. Hence, the LNA can be impedance matched as desired. The noise penalty for this LNA type is much lower than in the previous case, since the negative feedback reduces the equivalent noise contribution of the input impedance matching resistor, R_F, by $(1 + A_V)^2$.

Finally, the LNA presented in Fig. 7.1c uses noise cancelation technique [1]. Basically, it is composed from a CG input stage, M_1, in parallel with a CS stage, M_2. The idea behind noise cancelation technique is to use the CG stage as a matching amplifier stage, taking advantage of its low input impedance, equal to $1/g_{m1}$, to allow for wideband impedance matching. By combining its output with the voltage sensing CS-stage output, its channel thermal noise gets canceled out if $R_1 = g_mR_LR_S$. From noise perspective, this LNA is equivalent to a CS stage.

An interesting conclusion stemming from Table 7.1 which summarizes the key parameters of the LNA topologies is that a constant-g_m R biasing is required to immunize them to process and temperature effects.

7.1.2 The Highly Linear Downconversion Mixer

The LNA is followed by a zero-*IF* downconverter, which mixes the amplified RF signal with a quadrature local oscillator signal centered on the signal carrier.

The most linear mixer in CMOS implementation is the current-driven passive mixer depicted in Fig. 7.2. Usually, this type of mixer embeds a gm stage that interfaces the LNA output to the mixer switches by providing the V–I conversion. To save power in some cases, this gm stage can be excluded. In Fig. 7.2, the LO signals are assumed to be 50 % duty cycle. However, 25 % duty cycle LO signals can be used to improve circuit-level performance [3].

Due to the large signal amplitude at the mixer's input, the V–I conversion linearity must be enhanced by resistively degenerating the transistor pair (see Fig. 7.2). The input g_m-stage current is set then as a result of noise–linearity

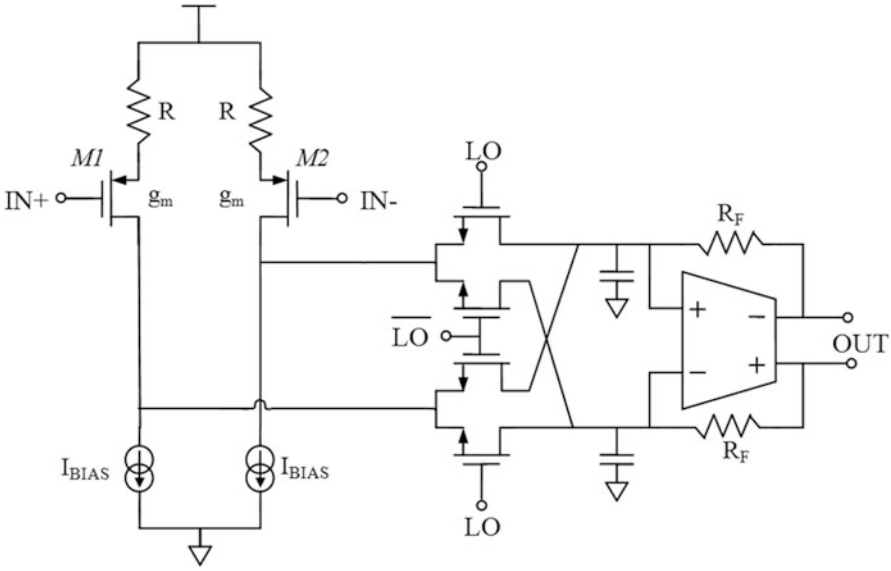


Fig. 7.2 Current-driven double-balanced passive mixer (only one channel shown)

trade-offs, as both the mixer noise figure and the third-order harmonic distortions of a source-degenerated transistor depend on the product of the devices' g_m and the degeneration resistor, R.

The mixer g_m-stage output signal current flows into the path of minimal impedance and thus enters the mixer switches. The switches exhibit a strong nonlinear characteristic relative to the LO port and, in the presence of a time variant drive (i.e., ideally a rectangular signal), perform the RF current frequency translation. The resulting signal contains both (1) the downconverted baseband component spanning from DC to the receiver baseband bandwidth and (2) a high-frequency up-converted component by-product at twice the RF frequency, which can be filtered out easily. Both components are attenuated as a direct result of the intrinsic mixing process, thus degrading the overall receiver noise performance. In practice the high-frequency component is filtered by placing capacitors to ground after the mixer switches (see Fig. 7.2). Looking from the RF side, this corresponds to an impedance transformation [4].

Finally, following the mixer switches, there is a transimpedance amplifier to provide the final I–V conversion. This block belongs to the LF part of the transceiver.

The overall mixer downconversion gain and its linearity and noise characteristics are summarized in Table 7.2. An interesting conclusion is maintaining all key downconverter parameters constant with process spread, and temperature requires a constant-$g_m R$ bias.

Table 7.2 Key parameters of the downconversion mixer

Parameter		Equation	Preferred bias
Gain[a]	A_v	K $g_m R_L/(1+g_m R)$	Constant $g_m R$
Linearity[b]	*IM*3	~$1/g_m R$	Constant $g_m R$
Noise[b]	*NF*	$1+\text{const}/g_m R^2/R_S$ (@ $g_m R \gg 1$)	Constant $g_m R$

[a]The K factor represents the intrinsic attenuation of the mixing process. Its value ranges from 0.5 to $2/\pi$, as the LO drive is a sine/square wave. R_L is chosen such that it compensates for the gain drop due to mixing. Usually, the mixer gain is low (0–6 dB)

[b]The switch noise and nonlinear contributions to the mixer output have been neglected, as no DC current flows through the switches. Hence, no alleviation is possible from biasing circuitry perspective. Also, the noise and linearity contribution of the transimpedance amplifier were not counted, since the amplifier is a baseband building block and its performance is considered in Sect. 7.2

7.2 SDRX LF Part Building Blocks

7.2.1 The LF Part Building Brick: The Fully Differential Feedback Amplifier

In direct conversion receivers, the RF signal is downconverted directly to baseband. Given the low values for the maximum frequency in the baseband signal spectrum of Table 3.1, the designer is legitimated to fully take the advantage of negative feedback to control the baseband system linearity (e.g., [5–8]).

> After all, the optimal direct conversion receiver design makes the noise of the baseband chain less critical (due to the RF front-end gain), while linearity performance is more stringent (due to lack of consistent filtering on the RF path). Thus, the negative feedback use represents the only way the designer can control and, subsequently, meet the specifications, alleviating the technology implementation.

This aspect becomes more critical as the System-on-a-Chip (SoC) implementation moves toward deep-submicron CMOS processes, where system-level design should not be limited by particular technology characteristics, like leakage.

> Hence, all baseband blocks will contain operational amplifiers to sustain a feedback network. Figure 7.3 presents the baseband chain building block diagram. The base amplifier is implemented as a fully differential amplifier, while the feedback network is built of linear elements, like resistors and/or capacitors.

The negative feedback system block diagram is presented in Fig. 7.4. The system's output signal is given by

$$OUT = IN \times a/(1+a\beta) \tag{7.3}$$

In the assumption the feedback network is composed only of linear elements, (7.3) shows the output signal is a linear replica of the input signal if the loop gain, $a\beta$, is much larger than 1.

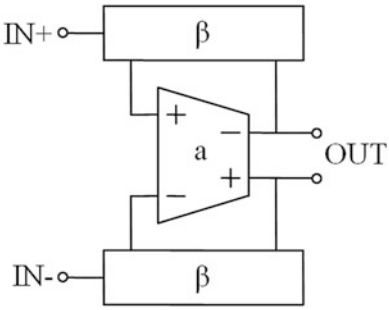


Fig. 7.3 SDRX LF part building brick

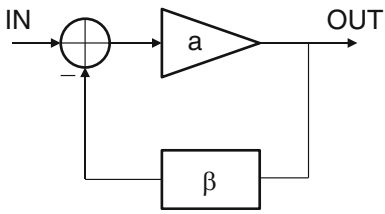


Fig. 7.4 Negative feedback systems

As proposed in [9], to quantify the reduction of the amplifier's distortion, a strong negative feedback is assumed. Thus, a linear base amplifier combines all its weak nonlinearity in an equivalent signal *DIST*, which is added to the amplifier's linear output *FUND*. So, for a weakly nonlinear system having only third-order distortions, the overall system output becomes

$$OUT = FUND + \frac{1}{1+a\beta}DIST = \frac{a}{1+a\beta}\times IN + \frac{1}{(1+a\beta)^4}\times k_3 IN^3 \overset{a\beta\gg 1}{\cong} \frac{1}{\beta}\times IN \quad (7.4)$$

where k_3 represents the base amplifier third-order distortion coefficient; because typically $k_3 < 0$ as the input signal *IN* becomes larger, the fundamental is compressed.

Equation (7.4) shows that the base amplifier nonlinearity is reduced by an amount equal to the loop gain. Assuming a one-pole amplifier, described by the DC open loop gain, a_0, and the pole frequency, f_0, the base amplifier distortion reduction becomes

$$\text{Distortion reduction} \overset{a_0\beta\gg 1}{\cong} \begin{cases} 1/(a_0\beta), & f \ll f_0 \\ f/(\beta GBW), & f \gg f_0 \end{cases} \quad (7.5)$$

where *GBW* represents the amplifier gain-bandwidth (GBW) product given by

$$GBW = a_0 f_0 \tag{7.6}$$

The distortion reduction given by (7.5) has been calculated under the assumption the loop DC gain is larger than unity: $a_0\beta \gg 1$. The maximum DC gain of active load one-stage amplifier is set by the process; for submicron processes, a typical value is about 40 dB, decreasing significantly for deep-submicron processes. Thus, to meet a given linearity specification at a given frequency, the loop must provide enough gain at that frequency to cancel out the amplifier distortions, or, equivalently, the loop response must be strong and fast enough to suppress the amplifier nonlinearity. For a weakly nonlinear system of bandwidth BW, exhibiting only third-order distortions, the $IM3$ requirement is met if

$$IM3 \leq \frac{BW}{\beta GBW} \times IM3_a \tag{7.7}$$

where $IM3_a$ is the base amplifier $IM3$. Typically, $IM3_a$ degrades with frequency.

As β is fixed by noise-power consumption trade-off constraints to a typically low 150 value, the amplifier's GBW must be chosen high enough to provide the required distortion reduction.

7.2.2 LF Part Modular Architecture

The fully differential feedback amplifier (FDFA) is assumed to have a voltage feedback at the input and a current feedback at the output of the base amplifier. Thus, the system acts as a voltage amplifier. Managing voltages represents the natural solution in the analog conditioning of the downconverted RF signal in a CMOS process, which benefits from the capacitive input impedance of the MOS device.

Moreover, if used efficiently, this approach enables the design porting to lower feature-size CMOS processes with minimal design effort and with best results. The negative feedback will inherently alleviate specific issues of a deep-submicron CMOS implementation (e.g., leakage).

Thus, all the SDRX LF blocks (i.e., the mixer TIA, the LPF, and the VGA) will be implemented by using a sequence of modules based on the FDFA of Fig. 7.3, as it is shown in the example of Fig. 7.5 [10].

First, the mixer transimpedance amplifier will be based on one single FDFA cell embedding a simple, one-pole, RC feedback network. Thus, the mixer stage has also a first-order low-pass filter characteristic that will reduce the level of nearby blockers.

Second, the LPF order, and thus the number of FDFA cells that will be used in building it, is given by the key trade-off shaping the SDRX LF part design. In Chap. 4, the trade-off between the LPF order and the ADC specifications of resolution and speed has been analyzed in depth. For the most popular wireless

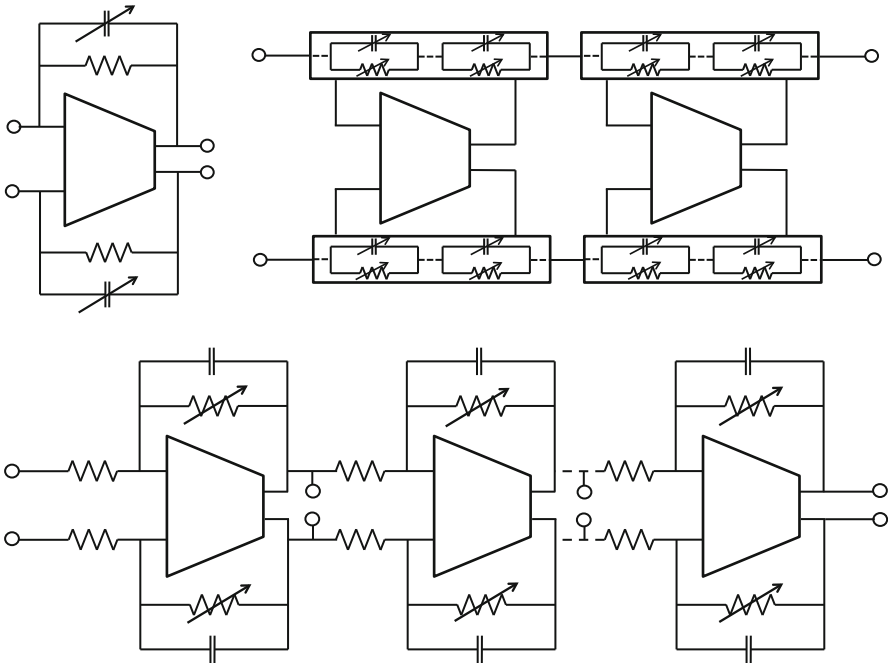


Fig. 7.5 The modular architecture of the SDRRX LF blocks. (**a**) Mixer TIA stage; (**b**) the LPF and (**c**) the VGA

standards, a LPF order of 4 was found as the optimal choice, hence the representation of two bi-quad cells in the example of Fig. 7.5b, each made of one FDFA circuit with RC feedback (e.g., [6]). Nevertheless, considering the fast rate at which the ADC power efficiency improves the analog LPF order, and thus the RX area, the LPF can be further reduced.

Finally, the VGA generic block diagram is depicted in Fig. 7.5c. The optimal number of stages is found from the trade-off between the circuit linearity and its power consumption. In [11], the author has analyzed the optimal number of stages for a VGA built for wireless applications and found that seven stages represent the optimal choice for a dynamic range of 84 dB. Each stage is made out of a FDFA with a feedback network made out of programmable feedback resistors to achieve the variable gain in parallel with an optional feedback capacitor that limits the noise bandwidth (e.g., [5]).

7.2.3 FDFA Power Optimization

Once the SDRRX LF block topology has been defined, the designer focus shifts toward identifying the constraints of the multi-standard environment on the key active component that is the baseband amplifier.

A multi-standard environment assumes multiple bandwidths for the baseband channel. Lately, variable signal bandwidths are foreseen even within the same wireless standards.

Thus, the SDRX LF part bandwidth needs to be made programmable by implementing the FDFA feedback network with programmable arrays of resistors and capacitors. A one-stage design for the base amplifier would be sensitive to changes in its feedback network, since its load is actually changing depending on the wanted bandwidth value. Thus the optimal choice for the opamp is to be implemented by two stages. The opamp output stage acts as a buffer and thus reduces the loading effect on its intrinsic parameters, mainly on the opamp gain-bandwidth (GBW) product.

A true reconfigurable receiver must optimally trade off its power consumption with the baseband signal bandwidth. The major constraints on the FDFA current consumption are set by four factors: noise, linearity, stability, and current driving capability. Further on we will address the four factors from the perspective of a flexible baseband bandwidth.

Firstly, for all the envisaged standards, the receiver foresees a 3 dB minimum NF and, thus, a constant noise spectral density for the baseband chain blocks (see Fig. 6.2). This first constraint blocks the current through the FDFA base amplifier input stage and sets the feedback network resistor value.

Secondly, according to (7.7), the FDFA linearity performance is proportional to BW/GBW, the ratio between the maximum frequency of interest (BW) and the opamp GBW. Hence, for the standards or signal bursts with smaller BW, the opamp GBW can be also lowered accordingly.

Thirdly, the FDFA opamp stability requirement (i.e., a phase margin larger than 60°) is met with enough output current in the final opamp stage. When the required BW is smaller, the feedback network capacitance will be increased accordingly. This capacitance (in the order of a couple pF) is the dominant part of the opamp load capacitance. This constraint blocks the output-stage quiescent current.

Finally, the output-stage current drive capability should be the same with respect to the variable signal bandwidth.

Since the output-stage current drive capability is linked to the DC quiescent current, it naturally results that the optimal choice for a power-efficient design is a class AB output stage.

Table 7.3 summarizes the impact of all these constraints on the FA base amplifier design.

Table 7.3 The major constraints on the FDFA power consumption

Parameter	Impact on the opamp power consumption
Noise	Sets a first lower limit for the opamp first-stage current, as the noise performance is inversely proportional to the first-stage transconductance, g_{mI}
Linearity	Sets another lower limit for the opamp first-stage current, as the FDFA linearity performance is proportional to BW/GBW and GBW is set by g_{mI}
Stability	Sets a first lower limit for the opamp second-stage current, as the phase margin is proportional to the second-stage transconductance, g_{mII}
Current drive	Sets another lower limit for the opamp second-stage current required to prevent slewing

7.2.4 FDFA Opamp Generic Topology

The opamp generic block diagram is depicted in Fig. 7.6.

The circuit is a fully differential two-stage opamp with an input stage based on a source-coupled pmos differential pair and a class AB output stage. The opamp $1/f$ noise optimization led to the pmos input-stage selection, while the power consumption optimization sets the class AB topology for the output stage. Also, since the amplifier is fully differential, a common mode feedback loop (CMFB) is required to set the amplifier output common mode voltage.

Table 7.4 summarizes the key parameters of the baseband chain circuits' building blocks. The data shows that noise, linearity, and system stability performance depend on (a) the operational amplifier *GBW*, set by the input-stage transconductance, $g_{m\mathrm{I}}$, and (b) on the second-stage transconductance, $g_{m\mathrm{II}}$. It results a constant-g_m biasing is required to keep the main parameters of the circuits based on the concept depicted in Fig. 7.6 invariant to process and temperature variations.

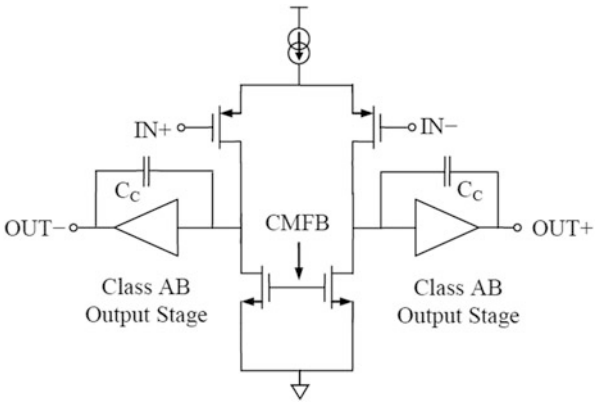


Fig. 7.6 Opamp generic topology

Table 7.4 Key parameters of the baseband chain circuits

Parameter		Equation	Preferred bias
Linearity	*IM3*	$IM3_a \times BW/\beta GBW \sim 1/g_m$	Constant g_m
Noise	*SNR*	$\beta^{-2} \times V^2_{\mathrm{sig}}/(v^2_{n\beta} + v^2_{\mathrm{na}}) \sim g_m$	Constant g_m
		V_{sig}—input signal	
		$v^2_{n\beta}$—feedback network equivalent noise	
		v^2_{na}—base amplifier equivalent noise	
Stability (for $\beta = 1$)	*Phase margin*	60° for $f_{p\mathrm{II}}/f_{p\mathrm{I}} = 2.2 \sim g_{m\mathrm{II}}/g_{m\mathrm{I}}$	–
		$f_{p\mathrm{I}}$—main pole frequency	
		$f_{p\mathrm{II}}$—output pole frequency	

7.3 SDRX Bias Block

The information from Tables 7.1, 7.2, and 7.4 provides the main requirements for the bias circuit: it must ensure minimal process and temperature-related variations of the receiver noise and linearity performance. A constant-g_mR current reference accomplishes the task, by generating a bias current that tracks with process and temperature.

Constant-g_mR CMOS biasing circuits are inspired by *proportional-to-absolute temperature* (PTAT) bipolar current source [12]. The biasing circuit idea is illustrated by the basic schematic presented in Fig. 7.7 [13]. By making transistor $M1$ larger than transistor $M2$, I_{REF} current is generated over R, as the current mirror, represented by equally sized devices $M3$ and $M4$, forces equal currents to flow through $M1$ and $M2$. The final implementation of this biasing circuit requires start-up circuitry to avoid transistors' zero current circuit's stable state.

The output current, mirrored by $M5$, is given by

$$I_{OUT} = NI_{REF} \tag{7.8}$$

where N represents the ratio between the output current source $M5$ size and diode-connected $M3$ size.

The I_{REF} current is given by

$$I_{REF} = \frac{V_{OV1}}{R}\left(\sqrt{P} - 1\right) \tag{7.9}$$

where $P = (W_1/L_1)/(W_2/L_2)$ is $M1$ and $M2$ transistors' size ratio, $M1$ being the largest device, and V_{OV1} is the overdrive voltage of $M1$.

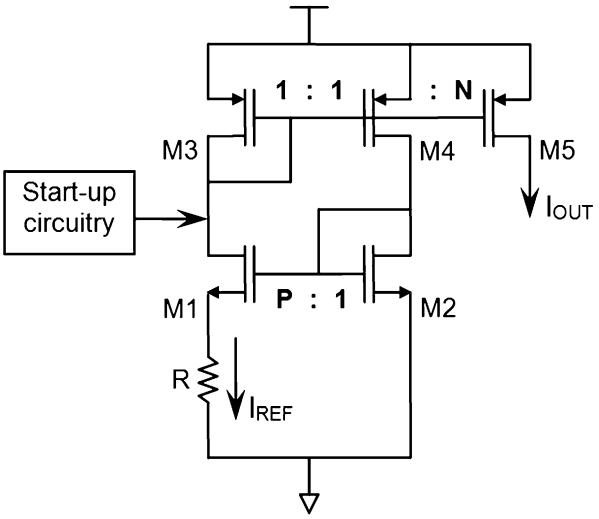


Fig. 7.7 Constant-g_mR biasing current source

The overdrive voltage, V_{OV}, of a MOS transistor operating in strong inversion and in saturation is

$$V_{OV} = V_{GS} - V_T = \sqrt{I_D / \left(\frac{K'}{2}\frac{W}{L}\right)} = \frac{2I_D}{g_m} \tag{7.10}$$

where V_{GS} is the bias point gate-to-source voltage, V_T the transistor's threshold voltage, I_D the drain current, $K' = \mu C_{ox}$ with μ being the channel charge carrier mobility and C_{ox} the gate oxide specific capacitance, and W/L the transistor's aspect ratio.

From (7.9) and (7.10), it results that the Fig. 7.7 current source provides a temperature-independent $g_m R$ product:

$$g_m R = 2\left(\sqrt{P} - 1\right) \tag{7.11}$$

This characteristic is realized at the expense of the reference current dependency on temperature, since (7.9) can also be written as

$$I_{REF}(T) = \left(\frac{\sqrt{P} - 1}{R}\right)^2 \left(\frac{\mu(T)\, C_{ox}}{2}\frac{W_1}{L_1}\right)^{-1} \tag{7.12}$$

where the channel charge carrier mobility depends on absolute temperature [14]:

$$\mu(T) = K_\mu T^{-1,5} \tag{7.13}$$

Given the temperature coefficient small value (a few ppm/°C) of the poly resistors implementing bias resistor R, the circuit of Fig. 7.7 can also be viewed as a constant-g_m biasing with temperature.

The dependency of the reference current, I_{REF}, vs. $M1, M2$ transistors' size ratio, P, with the ratio V_{OV1}/R as parameter—calculated using (7.9)—is presented in Fig. 7.8a.

To optimize power consumption, the bias current value is typically smaller than 500 μA. A good practice is to keep I_{REF} higher than 100 μA to maintain the mirroring ratio to the "load" circuit to reasonable values. The bias resistor, R, value is chosen such as the nominal I_{REF} value is within the aforementioned range.

The overdrive voltage V_{OV1} and size ratio, P, values are locked by matching requirements between the bias transistor $M1$ and its "load" counterpart [13].

Based on (7.13), and neglecting resistor R weak temperature dependency [15], the relative variation of I_{REF} current with temperature, ΔI_{REF}^T, results in

$$\Delta I_{REF}^T = \frac{I_{REF}(T) - I_{REF}(T_0)}{I_{REF}(T_0)} = \frac{T^{1.5} - T_0^{1.5}}{T_0^{1.5}} \tag{7.14}$$

where $I_{REF}\ (T_0)$ is the I_{REF} nominal value at room temperature.

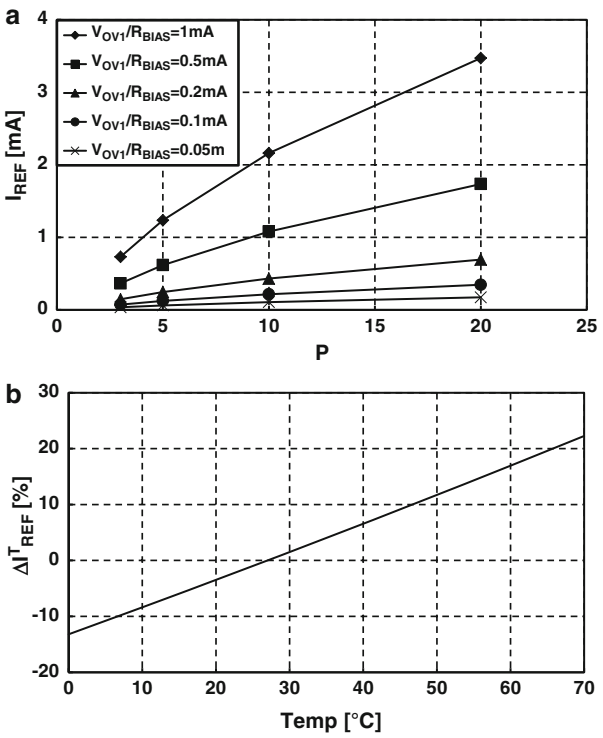


Fig. 7.8 (**a**) I_{REF} nominal value at room temperature vs. $M1/M2$ size ratio, (**b**) relative variation of I_{REF} with temperature (resistor R is supposed temperature independent)

Basically, within the commercial application temperature range (0...70 °C), the I_{REF} variation, relative to its nominal value at room temperature of 27 °C, is about 35 %, as shown in Fig. 7.8b.

To derive (7.9) and (7.12), some second-order effects regarding the transistors M_1 and M_2 were neglected, the most important being (a) threshold voltage mismatch (the threshold voltages were supposed to be identical) and (b) channel length modulation (supposed to be zero).

In the in-depth analysis from [13], it was concluded the overall error in the g_mR product is within ±15 % for a generic 0.13 µm CMOS process, and it decreases with the increase in the device channel length and area.

7.4 Baseband Noise Partitioning

7.4.1 Noise Excess Factor

Given the baseband building block structure (see Fig. 7.3), the equivalent input-referred noise spectral density at the LF chain input, $\overline{v_{n\ \mathrm{LF}}^2}/\Delta f$, can be split between the noise

contributions from the LF operational amplifiers, $\overline{v_{n\ \mathrm{LF\ a}}^2}/\Delta f$, and from the LF part feedback network, $\overline{v_{n\ \mathrm{LF\ \beta}}^2}/\Delta f$:

$$\overline{v_{n\ \mathrm{LF}}^2}/\Delta f = \overline{v_{n\ \mathrm{LF\ a}}^2}/\Delta f + \overline{v_{n\ \mathrm{LF\ \beta}}^2}/\Delta f \tag{7.15}$$

Thus, the LF part of the spot noise factor, F_{LF}, results as

$$F_{\mathrm{LF}} = 1 + \left(\overline{v_{n\ \mathrm{LF}}^2}/\Delta f\right)/(k_B T R_S) \tag{7.16}$$

where k_{B} is the Boltzmann constant, T the absolute temperature, and R_S the equivalent antenna noise resistance.

By using (7.15) in (7.16), we can clearly distinguish the two contributions to F_{LF}: one is originating from the feedback resistors and the other one is the overhead generated by the LF part operational amplifiers.

In order to properly evaluate the overhead to the overall noise budget of the LF part operational amplifiers, we introduce the LF part excess noise factor k_{LF}, defined by [16]

$$k_{\mathrm{LF}} = \left(\overline{v_{n\ \mathrm{LF\ a}}^2}/\Delta f\right)/\left(\overline{v_{n\ \mathrm{LF\ \beta}}^2}/\Delta f\right) \tag{7.17}$$

Thus, using k_{LF}, we can rewrite (7.16) to

$$F_{LF} = 1 + (1 + k_{\mathrm{LF}})\left(\overline{v_{n\ \mathrm{LF\ \beta}}^2}/\Delta f\right)/(k_B T R_S) \tag{7.18}$$

The LF part feedback resistor noise spectral density is equivalent to

$$\overline{v_{n\ \mathrm{LF\ \beta}}^2}/\Delta f = 4 k_B T R_{n\ \mathrm{LF\ \beta}} \tag{7.19}$$

where $R_{n\ \mathrm{LF\ \beta}}$ is the LF part equivalent noise resistance of the differential amplifier feedback networks.

Similarly, the noise spectral density originating from the LF opamps is

$$\overline{v_{n\ \mathrm{LF\ a}}^2}/\Delta f = 4 k_B T R_{n\ \mathrm{LF\ a}} \tag{7.20}$$

where $R_{n\ \mathrm{LF\ a}}$ is the equivalent noise resistance of the LF base amplifiers.

Given the noise contributions from (7.19) and (7.20), the total input-referred LF noise spectral density of (7.16) becomes

$$\overline{v_{n\ \mathrm{LF}}^2}/\Delta f = 4 k_B T \left(R_{n\ \mathrm{LF\ a}} + R_{n\ \mathrm{LF\ \beta}}\right) \tag{7.21}$$

Thus, the LF part spot noise factor, F_{LF}, results as

$$F_{LF} = 1 + (1 + k_{\mathrm{LF}}) 4 R_{n\ \mathrm{LF\ \beta}}/R_S \tag{7.22}$$

7.4.2 The Trade-Off Between LF Part Power Consumption and Area

From (7.22), the minimum F_{LF}, F_{LFmin}, is achieved when the base amplifier noise is negligible compared to the feedback resistance noise ($k_{LF} = 0$). By rearranging (7.22), the $R_{n\ LF\ \beta}/R_S$ ratio as a function of k_{LF} results as

$$\frac{R_{n\ LF\ \beta}}{R_S} = \frac{F_{LF} - 1}{4(1 + k_{LF})} \tag{7.23}$$

Figure 7.9a plots the $R_{n\ LF\ \beta}/R_S$ ratio as a function of k_{LF}. As expected, the larger is the noise spectral density from the base opamps, a smaller value for feedback resistors is required to keep the same noise spectral density contribution for the baseband blocks. However, in the same time, the integrated capacitance must be increased accordingly to the requirement of maintaining the low-pass filter (LPF) bandwidth and, thus, the baseband integrated output noise. This is the key trade-off between the LF part circuit's power consumption and area.

Figure 7.9b plots on the same graph $R_{n\ LF\ \beta}$, as a measure of the area consumption, and $R_{n\ LF\ a}$, as a measure of the power consumption, vs. k_{LF} for $R_S = 100\ \Omega$.

Due to the low baseband bandwidth of the envisaged standards (i.e., 100 kHz for GSM), the receiver area is mainly determined by the amount of integrated LPF capacitance. Hence, the trade-off represented in Fig. 9b is the key issue of the receiver baseband noise partitioning.

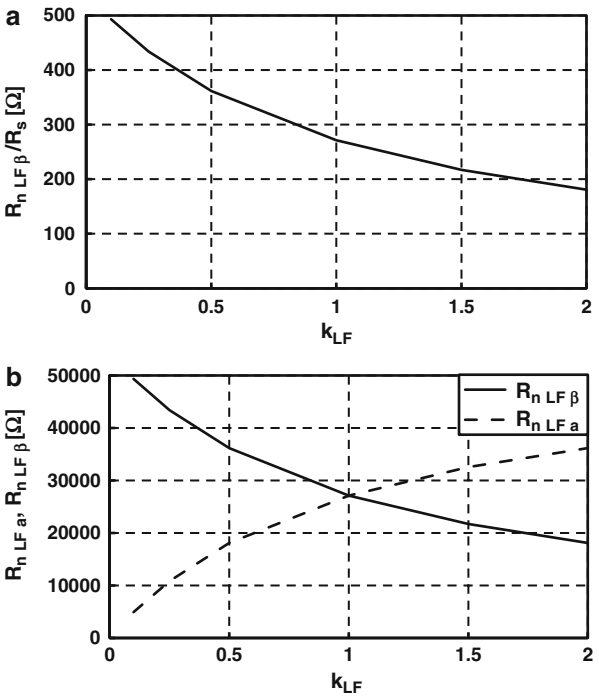


Fig. 7.9 (**a**) $R_{n\ LF\ \beta}/R_S$ and (**b**) $R_{n\ LF\ a}$, $R_{n\ LF\ \beta}$ vs. k_{LPF}

7.4.3 Noise Partitioning

The SDRX LF chain building blocks are the mixer transimpedance amplifier (TIA), the LPF and the VGA. Since all of these blocks are based either on one or on a cascaded series of fully differential feedback amplifiers embedding linear feedback networks, the noise contribution of the individual blocks can be split between the base operational amplifiers and the feedback network resistors. The noise breakdown of the LF part blocks is presented in Table 7.5.

Given the notations from Table 7.1, the total input-referred LF noise spectral density is

$$\begin{aligned}\overline{v_{n\ \mathrm{LF}}^2}/\Delta f &= \overline{v_{n\ \mathrm{TIA}}^2}/\Delta f + \overline{v_{n\ \mathrm{LPF}}^2}/\Delta f + \overline{v_{n\ \mathrm{VGA}}^2}/\Delta f \\ &= 4k_BT \times (1+k_{\mathrm{LF}})R_{n\ \mathrm{LF}} \\ &= 4k_BT \times (1+k_{\mathrm{LF}})(R_{n\ \mathrm{TIA}} + R_{n\ \mathrm{LPF}} + R_{n\ \mathrm{VGA}})\end{aligned} \tag{7.24}$$

where k_{TIA}, k_{LPF}, and k_{VGA} represent the mixer TIA, LPF, and VGA noise excess factors.

In line with the modular design of the receiver LF part, its noise partitioning assumes $k_{\mathrm{LF}} = k_{\mathrm{TIA}} = k_{\mathrm{LPF}} = k_{\mathrm{VGA}}$. In order to optimize the area consumption, not all of the three individual block noise contributions will be the same. Since the receiver area is mainly dominated by the amount of integrated LPF capacitance, the

Table 7.5 Receiver LF part noise breakdown

LF block	Contributors	Formula	Notes
Mixer baseband amplifier	Base amplifier	$\overline{v_{n\ \mathrm{TIA\ a}}^2} = 4k_BTR_{n\ \mathrm{TIA\ a}}\Delta f$	$R_{n\ \mathrm{TIA\ a}}$ is the mixer's opamp equivalent noise resistance
	Feedback network	$\overline{v_{n\ \mathrm{MIX\ \beta}}^2} = 4k_BTR_{n\ \mathrm{MIX\ \beta}}\Delta f$	$R_{n\ \mathrm{MIX\ \beta}}$ is the mixer's feedback network equivalent noise resistance
	Total	$\frac{\overline{v_{n\ \mathrm{TIA}}^2}}{\Delta f} = \frac{\overline{v_{n\ \mathrm{TIA\ a}}^2}}{\Delta f} + \frac{\overline{v_{n\ \mathrm{TIA\ \beta}}^2}}{\Delta f}$	$k_{\mathrm{TIA}} = \frac{\overline{v_{n\ \mathrm{TIA\ a}}^2}/\Delta f}{\overline{v_{n\ \mathrm{TIA\ \beta}}^2}/\Delta f}$
LPF	Base amplifier	$\overline{v_{n\ \mathrm{LPF\ a}}^2} = 4k_BTR_{n\ \mathrm{LPF\ a}}\Delta f$	$R_{n\ \mathrm{LPF\ a}}$ is the LPF opamp equivalent noise resistance
	Feedback network	$\overline{v_{n\ \mathrm{LPF\ \beta}}^2} = 4k_BTR_{n\ \mathrm{LPF\ \beta}}\Delta f$	$R_{n\ \mathrm{LPF\ \beta}}$ is the LPF feedback network equivalent noise resistance
	Total	$\frac{\overline{v_{n\ \mathrm{LPF}}^2}}{\Delta f} = \frac{\overline{v_{n\ \mathrm{LPF\ a}}^2}}{\Delta f} + \frac{\overline{v_{n\ \mathrm{MIX\ \beta}}^2}}{\Delta f}$	$k_{\mathrm{LPF}} = \frac{\overline{v_{n\ \mathrm{LPF\ a}}^2}/\Delta f}{\overline{v_{n\ \mathrm{LPF\ \beta}}^2}/\Delta f}$
VGA	Base amplifier	$\overline{v_{n\ \mathrm{VGA\ a}}^2} = 4k_BTR_{n\ \mathrm{VGA\ a}}\Delta f$	$R_{n\ \mathrm{VGA\ a}}$ is the VGA opamp equivalent noise resistance
	Feedback resistors	$\overline{v_{n\ \mathrm{VGA\ \beta}}^2} = 4k_BTR_{n\ \mathrm{VGA\ \beta}}\Delta f$	$R_{n\ \mathrm{VGA\ \beta}}$ is the VGA feedback network equivalent noise resistance
	Total	$\frac{\overline{v_{n\ \mathrm{VGA}}^2}}{\Delta f} = \frac{\overline{v_{n\ \mathrm{VGA\ a}}^2}}{\Delta f} + \frac{\overline{v_{n\ \mathrm{VGA\ \beta}}^2}}{\Delta f}$	$k_{\mathrm{VGA}} = \frac{\overline{v_{n\ \mathrm{VGA\ a}}^2}/\Delta f}{\overline{v_{n\ \mathrm{VGA\ \beta}}^2}/\Delta f}$

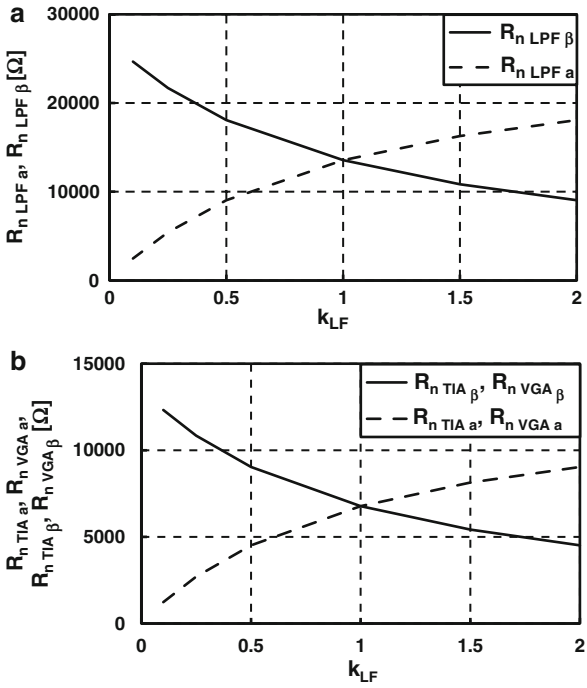


Fig. 7.10 (**a**) $R_{n\ \mathrm{LPF\ a}}$, $R_{n\ \mathrm{LPF}\ \beta}$, and (**b**) $R_{n\ \mathrm{TIA\ a}}$, $R_{n\ \mathrm{TIA}\ \beta}$, $R_{n\ \mathrm{VGA\ a}}$, $R_{n\ \mathrm{VGA}\ \beta}$ vs. k_{LPF}

LPF will be allowed to contribute as much as the mixer transimpedance amplifier and the VGA all together, while the two will contribute the same. This translates to the following condition:

$$R_{n\ \mathrm{LPF}\ \beta} = 2R_{n\ \mathrm{TIA}\ \beta} = 2R_{n\ \mathrm{VGA}\ \beta} \tag{7.25}$$

Hence, we can conclude:

$$R_{n\ \mathrm{LPF}\ \beta} = R_S \frac{F_{\mathrm{LF}} - 1}{8(1 + k_{\mathrm{LF}})} \tag{7.26}$$

Figure 7.10 shows the $R_{n\ \mathrm{TIA\ a}}$, $R_{n\ \mathrm{TIA}\ \beta}$, $R_{n\ \mathrm{VGA\ a}}$, and $R_{n\ \mathrm{VGA}\ \beta}$ as a function of k_{LF}. Finally, the proposed receiver baseband noise partitioning gives the same importance to both area and power consumption by setting $k_{\mathrm{LF}} = 1$. It results in $R_{n\ \mathrm{TIA}\ \beta} = R_{n\ \mathrm{VGA}\ \beta} \leq 7.5\ \mathrm{k\Omega}$ and $R_{n\ \mathrm{LPF}\ \beta} \leq 15\ \mathrm{k\Omega}$.

7.5 Conclusion

This chapter analyzed the modern receiver building blocks from a system-level perspective. For the SDRX's HF part, the main choices for wideband LNAs were presented, and a potential candidate for a highly linear downconverter was

introduced. While for the SDRX's LF part, it became clear that a modular design build on FDFA employing a programmable array of linear elements (i.e., poly-Si resistors and metal–insulator–metal capacitors) sustained by a two-stage class AB opamp is the optimal choice: (1) because it controls the system linearity, through the FDFA GBW, and (2) it facilitates design porting to newer, lower feature-size CMOS processes.

However, the main purpose of the analysis was focused on determining the building block key parameters that define the receiver noise and linearity performance and linked them to the receiver overall performance. Also, a secondary conclusion was a constant-g_mR biasing is required to keep these parameters as constant as possible with process and temperature variations.

Finally, the introduction of a new tool, k_{LF}, the LF part noise excess factor, as the ratio between the baseband opamps noise contribution and the feedback resistors noise, clarified the power consumption/area trade-off at the center of the LF part noise partitioning: the larger is the noise of the base opamps (i.e., larger k_{LF}, equivalent to lower opamp current consumption), a smaller value for feedback resistors is required to keep the same noise contribution for the baseband blocks; but, in the same time, the integrated capacitance must be increased accordingly to maintain the same LF chain bandwidth. Overall, the receiver baseband noise partitioning gives the same importance to both area and power consumption by setting $k_{\mathrm{LF}} = 1$.

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Chapter 8
Conclusions and Future Developments

8.1 Conclusions

The research comprising the present book tackled one of the major problems in today's mobile communication systems: the optimal design path for software-defined radio receiver front-ends. The research is focused on the analysis and design of SDRX part of multi-standard RF front-ends compatible with the major commercial wireless standards of the moment. Such a system is the most suited candidate for the first design iteration in the case of the next-gen 5G deployment.

The success of this research was ensured by the systematic approach used in all the stages of the SDRX design. Basically, this book has completed a study on the system-level analysis of the RF and analog baseband signal conditioning for multi-standard radio receivers.

From the beginning the designer must set *clear design targets* which should be the enabling factor in identifying the *key trade-offs* shaping the SDRX design.

First, I have analyzed the receivers' architectures in order to identify the most suitable architecture for a multi-standard software reconfigurable receiver relative to cost/performance ratio. The direct conversion architecture was proven to be the best candidate for this task by optimally leveraging the chip area; the PCB design, implemented with a minimal bill of materials (BOMs); and the low power consumption required by wireless mobile operation.

The architecture was extended by the inclusion of (a) an offset cancelation loop and (b) wideband quadrature generators in order to make easier the monolithic integration. The implemented architecture is able to coop with multiple modulation techniques and schemes, to handle a wide RF range (it incorporates multiple LNAs and programmable wideband quadrature frequency dividers), and to change on the fly its baseband channel bandwidth.

All these features offer to the implemented architecture an edge relative to the future trends in wireless communication standardization. Also, a significant

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advantage of the zero-IF architecture is its tolerance to process scaling. Thus porting is possible without any change to the developed architecture.

Once the optimal architecture was selected, the electrical specifications for the SDRX need to be determined. Hence, I have developed a standard-independent, systematic methodology to help derive the SDRX key electrical specifications. The main target in developing the methodology was building a SDRX model suited for an intuitive understanding of the design. Based on the first-order system-level analysis, the SDRX front-end key electrical parameters were identified. All these parameters are common for all standards, and only their values differ.

Thus, for the first time to the author's knowledge, the designer is enabled to tackle the multi-standard environment in a parallel way rather than serially. Consequently, the designer is enabled to handle efficiently the large amount of information provided in the envisaged wireless standards. Furthermore, understanding and validating more complex receiver models implemented in CAD tools (e.g., MATLAB) becomes much easier.

Also this methodology has the advantage; it can be used very efficiently for newly developed wireless standards or even for other types of non-wireless communication (e.g., cable communication [1, 2]).

The design of any wireless receiver is determined by the interdependency between its noise, linearity, and gain performance. With a smart design the input impedance influence can be equated out. Figure 8.1 sketches the liaisons between the individual trade-offs shaping the SDRX front-end design. The most important consequences of solving the trade-offs are (1) the optimal filter partitioning, as the solution for the trade-off between the SDRX area and power consumption, and (2) the smart gain partitioning, as a solution for the trade-off between the SDRX noise and linearity performance.

Thus, the most important problem due to blockers and interferers, the critical issue of the receiver selectivity, was addressed. I found the optimum filter

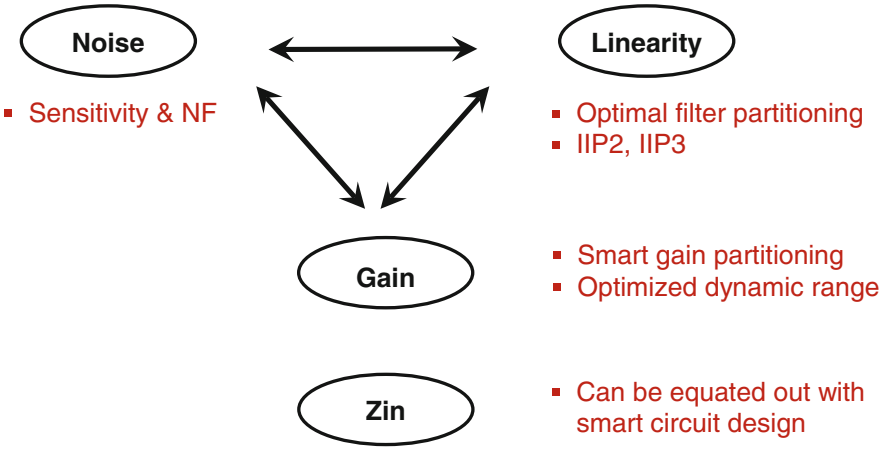

Fig. 8.1 The key trade-offs shaping the SDRX front-end design

partitioning between the SDRX baseband analog LPF and the digital filter following the A/D conversion. As a direct result of the newly developed systematic analysis, I have introduced a new and efficient tool: the generic blocker diagram. Subsequently, I have defined FOM_{CHS}, a FOM that enables the proper evaluation of the key trade-off between the analog LPF area and ADC power consumption in one single plot. Based on the FOM_{CHS} analysis, it resulted a LPF order larger than 4 brings no further benefit.

Also, by analyzing further the FOM_{CHS}, I determined that depending on which is the parameter to be optimized, either the receiver power consumption or its area, the baseband filter partitioning strategy can range between a complete analog channel selection ($n_{\mathrm{LPF}} = 5$) and a fully digital approach ($n_{\mathrm{LPF}} = 0$). This general character of the presented filter partitioning methodology fits best a true SDRX implementation.

And an interesting conclusion is direct sampling SDRX is still about two orders of magnitude away from a mixer-based solution in terms of power consumption. However, the rate at which ADC power efficiency improves (i.e., about ten times every 4 years [3]) may make attractive on medium-term direct sampling systems.

Once the optimal filter partitioning was determined, I have tackled the key issue of the extreme reception conditions specific to the wireless environment. Thus, in order to optimally mitigate these extreme receive scenarios, I have developed a novel gain partitioning strategy tailored toward multi-standard radio receivers.

Basically, the smart gain partitioning foresees splitting the receiver gain between an RF front-end embedding programmable gain and a high-dynamic range variable gain amplifier. I have proposed a generic algorithm to find the optimal gain partitioning between the SDRX's two variable gain blocks, accounting the fact that the receiver NF and IIP3 change with the RF front-end gain. The proposed gain partitioning algorithm optimizes the signal-to-noise ratio at the receiver output for each of the targeted standards by selecting the minimum RF front-end gain that guarantees proper signal demodulation. Thus, the SDRX robustness to blockers and interferers is enhanced while still ensuring a good noise performance at low input power levels. Given the generic algorithm it is based on, the proposed solution fits best a true SDRX implementation.

Further on, the developed first-order system-level analysis was used to determine the optimal noise–linearity breakdown between the SDRX's HF and LF parts. By using the developed methodology, power saving is enabled in the HF part through changing the SDRX HF part noise and linearity performance with its RF front-end gain. While for the LF part, the analysis revealed the performance can be kept the same to allow power optimization through dedicated circuit design.

Thus, finally, the path toward circuit optimization has been opened. Starting from system level, an overview of modern receiver building blocks was presented. The analysis was focused on determining the building blocks' key parameters that define the receiver noise and linearity performance and link them to the receiver overall performance.

The analysis revealed the receiver RF front-end (i.e., the LNA and mixer) should be built using differential or pseudo-differential transistor pairs. The trade-off

between the noise and linearity performance is set by the amount of source degeneration: when low noise is required, the RF front-end gain is set to the maximum, and subsequently no degeneration is to be implemented, at least in the LNA; on the other hand, when high linearity is required, it can be achieved by degenerating the source of the differential pair devices.

The main goals in choosing the baseband blocks architecture are (a) high linearity and (b) immunity to particular technology characteristics and easiness of the design porting. To control the baseband chain linearity, given the rather low baseband signal bandwidth, low-power feedback amplifiers are used as the building brick of all the low-frequency part circuits. The amplifier implementation is based on high-GBW fully differential opamp and on a linear feedback network of programmable poly-Si resistors and/or metal–insulator–metal capacitors. The two-stage opamp concept is implementing a class AB output stage (a) to leverage the noise–linearity constraints with the low power consumption requirement of mobile applications and (b) to decouple the intrinsic opamp parameters (e.g., GBW) from the output load. So, from the system-level perspective, the noise of the LF chain is split between the noise contributions of its operational amplifiers and of its feedback resistors. By introducing a new tool, the LF part noise excess factor, as the ratio between the noise from the opamps and the noise from the feedback resistors, the system-level analysis highlighted in a clear way the power consumption/area trade-off in the SDRX's LF part noise partitioning strategy.

A side conclusion of the circuit implementation analysis was a constant-g_mR biasing is required to keep the key parameters of the SDRX's HF and LF part as constant as possible with process and temperature variations.

8.2 Future Developments

The advent of embedded wireless radio front-ends has started in the early 2000s with the first fully integrated transceivers [4, 5]. During the next decade, the SDRX designs matured and became fully reconfigurable [6–8]; even blocker-tolerant receivers were developed [9]. State-of-the-art cellular SDRXs achieve less than 2-dB NF [10]. Moreover, alternative approaches of blocker-tolerant SDRXs [11, 12] (i.e., based on N-path filters) propose noise cancelation [13], phase noise cancelation [14], and both [15] by employing multiple receiving paths.

Hence, the advances on circuit design represent a clearly defined base of options constructed on the mixer-based direct conversion architecture. However, the fast increase of performance for modern ADCs may render feasible the mixer-less direct sampling architecture.

As concluded in [16], looking in the future, the trend is to move as much as possible the processing of the RF/analog signal into the digital domain. Literature papers [17, 18] have shown the feasibility of analog circuit content reduction in radio transmitters and synthesizers, in favor of more digital circuits.

Also, techniques in calibrating transceiver impairments by using the relative inexpensive digital gates are starting to appear. Already for calibrating transmitter impairments, such breakthrough techniques have been recently published in [19]. Moreover, if GHz bandwidths are needed, wideband DAC-based transmitters have become mainstream in wireline applications [20–22].

For radio receivers, such leap forward methods have been reported for the low-frequency part. In [23], a novel architecture for the BB chain of a multi-standard wireless receiver has been presented: almost the whole baseband receiver can be described in an RTL and can be implemented using a standard digital design approach, except a small macroblock located after the downconverter mixer.

By extrapolating this trend and by considering the high rate at which the ADC's power efficiency is improved [3] on short or medium term, Mitola's SDR [24] will become a reality.

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