Lecture Notes in Electrical Engineering 466

Christophe Labbé
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Gargi Raina
B. Bindu
Editors

Nanoelectronic Materials and Devices

Select Proceedings of ICNETS2, Volume III

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Preface

This book volume is based on the talks delivered in Symposium C entitled Nanoelectronic Materials and Devices at "International Conference on NextGen Electronic Technologies–Silicon to Software" (ICNETS2). The theme of this symposium relates to the advances and emerging directions made in the fabrication, application as well as simulation of novel nanoelectronic materials and their impact on diverse electronic device technologies. The articles in this book volume focus on diverse topics encompassing functional electronic nanomaterials, nanocomposites for energy application, sensing and high-strength materials and simulation of novel device design structures for ultra-low-power applications.

Nanotechnology has been perceived as an enabler of extending the Moore's law in nanoelectronic domain in the present technology era. This symposium brought together experts from across international and national academic communities as well as industries to discuss fabrication, characterization and computational aspects in the field of nanoelectronics.

This book volume provides a compilation of different functional nanoelectronic materials such as graphene oxide-based metal oxide nanoparticles, nanocomposites and InAs/GaAs quantum dots and their device application in memristors, MEMs, CNTFETs, TFETs and memory circuits. We hope this book provides insight into and perspective on the domain of nanoelectronic materials to upcoming young researchers and non-specialists.

Mumbai, India — Dr. Subhananda Chakrabarti
Caen, France — Dr. Christophe Labbé
Chennai, India — Dr. Gargi Raina
Chennai, India — Dr. B. Bindu

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We are thankful to the VIT management for all the support and encouragement for the successful conduct of this conference and enabling our participation.

We express our heartfelt thanks to the invited speakers and keynote speakers for taking time off from their busy schedule and travelling long distance to share with us their research insights in the upcoming domain of nanoelectronic materials and device applications. We are thankful to all the authors who participated and contributed their research findings towards bringing out this book volume.

The editors wish to acknowledge the important contributions of Dr. Mohanaprasad and Dr. Annis in coordinating and assembling the contributions for the book. Last but not least, we would like to thank and appreciate our publication partners at Springer, especially Swati Meherishi and Aparajita Singh, for helping us bring out this special volume comprising invited and keynote talks.

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About the Editors

Dr. Christophe Labbé is an Associate Professor at CIMAP Lab (Centre de Recherche sur les Ions, les Matériaux et la Photonique), Caen, France, in the engineering school ENSICAEN. He obtained his PhD in Rare Earth Lasers at the Interdisciplinary Research Center Laser Ions, Caen, in 1999. After a postgraduate position at the Laser Arava Laboratory of the Ben-Gurion University of the Negev, Israel, on ionic matrix lasers pumped by diode, he became an Assistant Professor at the Laboratory of Optical Functions for Telecommunications (FOTON Lab) in Rennes, France, in 2002. His ongoing research focuses on photon sources for telecommunications or visible light applications and on photovoltaic cells.

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The Effect of Functionalized MWCNT on Mechanical and Electrical Properties of PMMA Nanocomposites

Amrit Mallick, Punyapriya Mishra and Sarat Kumar Swain

Abstract Proper assortment of compatible reinforcement and matrix could improve the mechanical strength and electrical properties of the nanocomposites. This chapter proposes a novel sequential approach of fabrication and testing for mechanical strength and electrical conductivity of the multiwall carbon nanotube (MWCNT) reinforced PMMA composite by extrusion technique along with their morphological analysis by field emission scanning electron microscope (FESEM). The MWCNT dispersion is a major challenge; encountered particularly in the thermoplastic polymer nanocomposites. Functionalized MWCNTs (f-MWCNTs) in varying weight proportions of 0.1, 0.3, 0.5, 0.7, and 1.0 wt% were added to the thermoplastic polymer matrix such as polymethyl methacrylate (PMMA) and then extruded into ASTM standard specimens. The mechanical properties such as tensile stress, tensile strain, tensile modulus at maximum load, and impact strength were measured, and their improved magnitudes reaffirmed effective dispersion of f-MWCNTs in matrix. Composites replacing the conventional engineering materials in electronic devices should have better electrical conductivity for various applications. Hence, the conductance of specimens was measured and showed a very low percolation threshold for electrical conductivity.

Keywords f-MWCNT · PMMA · Nanocomposite · FESEM · Tensile strength Flexural strength · Impact strength · Electrical conductivity

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1 Introduction

Composite materials are the paramount substitute of the conventional engineering materials in terms of ease of manufacture, reliability, higher physical property, and biodegradability. The potential uses of the composites in aerospace and electronics have drawn attention to develop the new materials to cater the domestic and industrial needs. Composite materials are fabricated as that desired properties are tailored based upon the requirement. Nanocomposites reinforced with functionalized carbon nanotubes in metal matrix reveal strong interfacial bonding [1]. The nanoplatelets of graphite and multiwall carbon nanotubes substantially increase the electrical conductivity and thermal stability of the polymer composites [2, 3]. Short glass fibers/multiwall carbon nanotube composites show significant improvement in the electrical, rheological, and mechanical characteristics [4].

2 Materials and Fabrication Technique

2.1 Materials

The multiwall carbon nanotubes, procured from Sisco Research Laboratory, Mumbai, India, with an average diameter of 10–20 nm and length of 10–30 nm were chosen as suitable reinforcement for nanocomposite. Transparent thermoplastic polymer such as polymethyl methacrylate was used as matrix, which was purchased from HIMEDIA, Mumbai, India, with an average molecular weight of 15,000.

2.2 Functionalization of MWCNTs

To enhance the interfacial adhesion to polymer matrix, functionalization of pristine MWCNTs is carried out prior to fabrication. Nanotubes are treated with concentrated sulfuric acid (H_2SO_4) and concentrated nitric acid (HNO_3) mixture in ratio of 3:1 v/v, stirred at room temperature [5], and then again treated with oxidizing agents such as concentrated sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) that cut the edges and adds carboxyl groups to the surfaces of MWCNTs. Chemically treated f-MWCNTs were dehydrated in oven at 80 °C for 24 h followed by cryomilling at low frequency.

2.3 Fabrication Method

f-MWCNTs in various weight percentages of 0.1, 0.3, 0.5, 0.7, and 1.0% of the total composite were taken in five batches. The DSM XPLORE 5 Microcompounder is used for compounding this small quantity mixture of 10 gm weight containing both the f-MWCNTs and the PMMA. The mixture is heated up to 220 °C temperature with 13–15 revolutions per minute of twin screws for 20 min of compounding time [6]. DSM micro 10 cm^3 mini injection molding machine used for injection molding of ASTM standard specimens with the pressure of 0.8 bar [7].

2.4 Specimen Preparation

Tensile test standard specimens of f-MWCNT/PMMA composite as per ASTM D638 were fabricated. The flexural test standard specimens of f-MWCNT/PMMA composite as per ASTM D790-99 were fabricated for a three-point bending test. Similarly, the impact test standard specimen ASTM D-256 was also prepared with varying weight proportions of f-MWCNTs 0.1, 0.3, 0.5, 0.7, and 1.0 wt% in the nanocomposites. The fabricated tensile, flexural, and impact test standard specimens are shown in Figs. 1, 2, and 3 respectively.

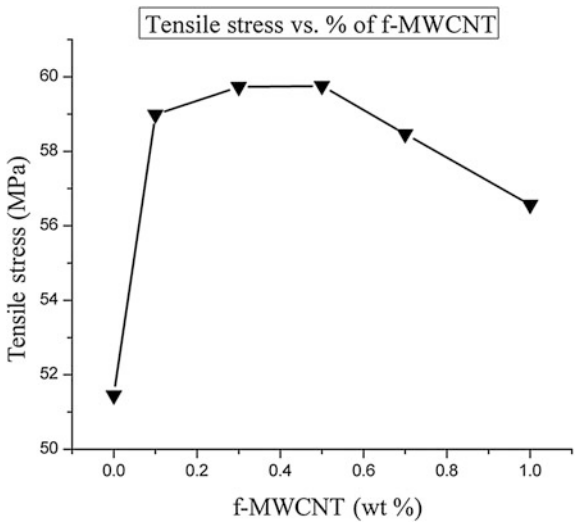

Fig. 1 Tensile stress of f-MWCNT/PMMA composites as a function of wt% of f-MWCNTs

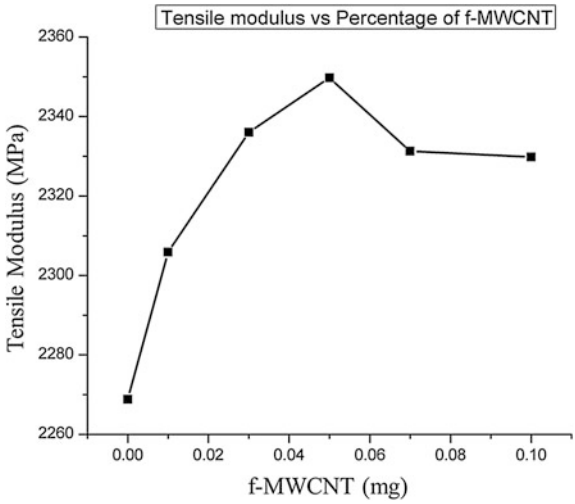

Fig. 2 Tensile modulus of f-MWCNT/PMMA composites as a function of f-MWCNTs weight

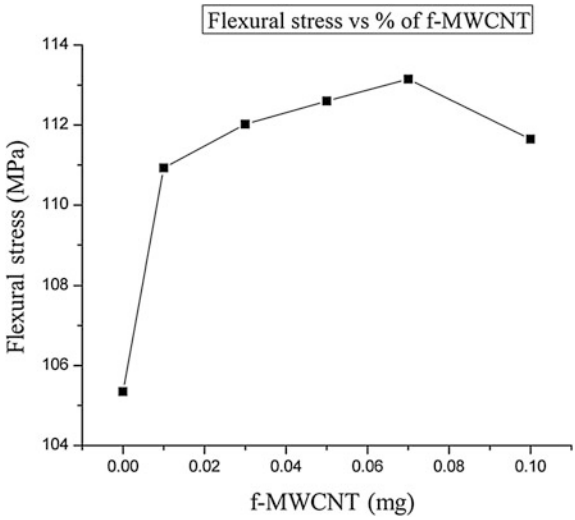

Fig. 3 Flexural stress of f-MWCNT/PMMA composites as a function of f-MWCNTs weight

2.5 Testing of Specimens

The tensile strength, tensile modulus, and tensile strain were measured by the INSTRON-3382 universal testing machine. The displacement was measured with 50-mm extensometer at a rate of 1 mm per minute at room temperature with loading of 5 KN. The stress versus strain curve was plotted. The flexural test was carried out using INSTRON-3382 by three-point bending method at a cross-head speed of 1.38 mm per minute. The flexural stress and flexural modulus for each of the f-MWCNT/PMMA nanocomposite samples were recorded. Impact testing and

Izod test of the specimens with varying weight percentages of f-MWCNTs were carried out using the Tinius Olsen impact tester with pendulum energy 2.7475 J. The notch depth of 2.5 mm with radius of 0.25 mm was maintained as per ASTM D-256 standard.

3 Experimental Results

Table 1 shows the stress–strain curves of f-MWCNT/PMMA composite for a different f-MWCNT percentages, i.e., 0, 0.1, 0.3, 0.5, 0.7, and 1.0%, respectively. From the plots, it is observed that tensile stress increases with the increase in percentage of reinforcement [8]. This trend of increase in the tensile stress is found up to 0.5% (0.05 mg) of f-MWCNT content which has a maximum tensile stress value of 59.755 MPa and then decreases for the further addition of reinforcement to the polymer. This trend is evident from tensile stress versus wt% of f-MWCNTs and tensile modulus versus weight of f-MWCNTs from Figs. 1 and 2.

It is also observed from Table 1 that the flexural stress increases for 0.1–0.7% and then decreases for 1.0%. This shows a sharp increase and then slightly decreasing trend from Figs. 2 and 3. The maximum value of flexural stress and modulus is 113.15 and 3144.28 MPa at 0.7% of f-MWCNT, which is much larger in comparison with tensile stress and tensile modulus at maximum load. This indicates that by sacrificing the tensile strength, the flexural strength has been increased. Similarly, composite samples showed increased flexural modulus than pure PMMA. There is 7.4% and 4.4% increase in flexural stress and flexural modulus of composite than pure PMMA sample (Fig. 4).

The energy absorbed by the composite during Izod impact test is measured. The variation of impact strength with percentage of f-MWCNT witnessed decrease in the impact strength with the increase in f-MWCNT from the plotted values in Figs. 5 and 6. The cause for decrease in impact strength is attributed to the percentage increase of f-MWCNT in composite that makes the composite more and more brittle and inadequate adhesion between matrix and reinforcement.

Table 1 Mechanical properties of f-MWCNT/PMMA composites as a function of wt% of f-MWCNTs

wt% CNTs	Mechanical properties					
	Tensile stress (Mpa)	Tensile modulus (Mpa)	Flexural stress (Mpa)	Flexural modulus (Mpa)	Break in Joule	Impact strength in J/m^2
0	51.47	2268.86	105.35	3011.79	0.0643	1.97
0.1	58.99	2305.85	110.93	3091.84	0.049	1.89
0.3	59.73	2336.04	112.02	3109.72	0.0450	1.39
0.5	59.75	2349.75	112.60	3141.98	0.0430	1.26
0.7	58.47	2331.26	113.15	3144.28	0.0424	1.25
1.0	56.56	2329.83	111.65	3123.42	0.0388	1.18

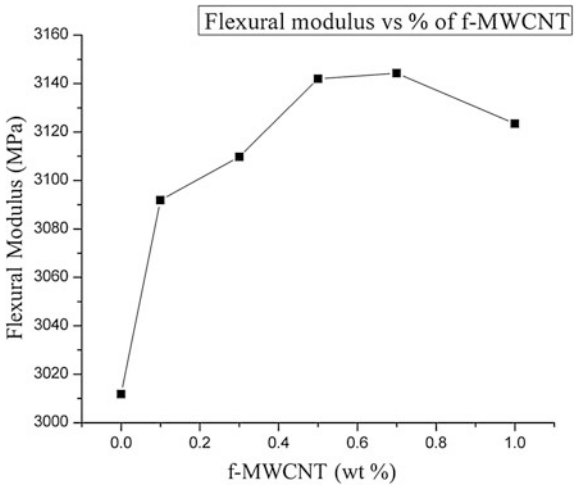

Fig. 4 Flexural modulus of f-MWCNT/PMMA composites as a function of wt% of f-MWCNTs

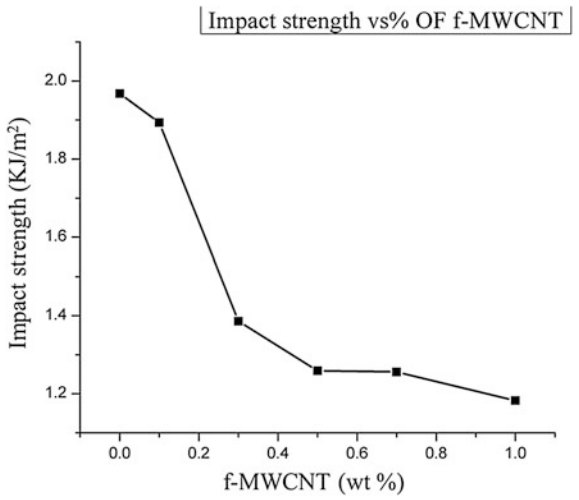

Fig. 5 Impact strength of f-MWCNT/PMMA composites as a function of wt% of f-MWCNTs

Electrical properties of nanocomposites generally depend upon the structure, extent of dispersion, and particle size of conducting fillers along with the properties of host polymers. The conductivity of nanocomposites found to be increased with the increasing f-MWCNTs wt% in the composites as shown in Fig. 7.

The conductivity of PMMA is about 1.3×10^{-13} S/cm in the initial stage, and this is consistent with the magnitude of an insulator. At slightly higher filler concentration, the nanocomposites experience a transition from low conductivity to a rapid increase in conductivity. The sharp increase in conductivity observed in case of PMMA/f-MWCNT nanocomposite as compared to virgin PMMA and it was due to the percolation threshold.

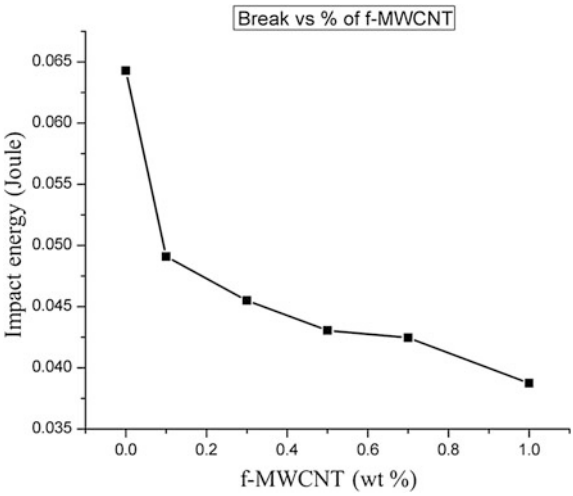

Fig. 6 Impact energy of f-MWCNT/PMMA composites as a function of wt% of f-MWCNTs

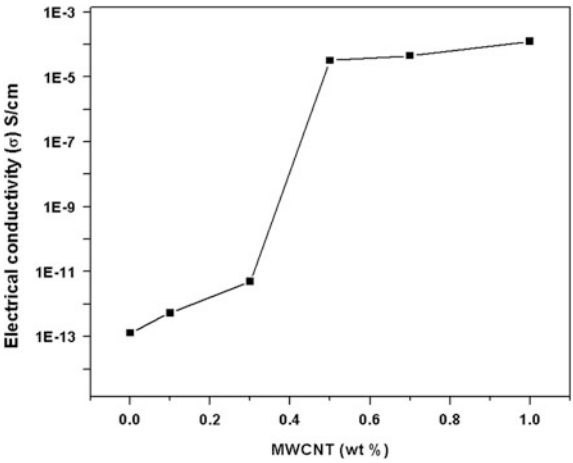

Fig. 7 Electrical conductivity of f-MWCNT/PMMA composites as a function of wt% of f-MWCNTs

The f-MWCNT/PMMA composite shows a very low percolation threshold for electrical conductivity due to high aspect ratio, nanoscale structure, and dispersion f-MWCNT in the polymer [9].

The Electrical conductivity versus f-MWCNT wt% was plotted at constant frequency of 1 MHz. The sharp increase in conductivity from 0.3 to 0.5 wt% is due to exceeding of percolation threshold value and leading to increased conductivity. At this stage, the conductivity of the nanocomposite material is about 1.24×10^{-4} S/cm, which is nearly consistent with that of a conductor. The PMMA/f-MWCNT nanocomposites exhibited a very low percolation threshold for electrical conductivity because of large surface area and the nanoscale dimension of f-MWCNTs.

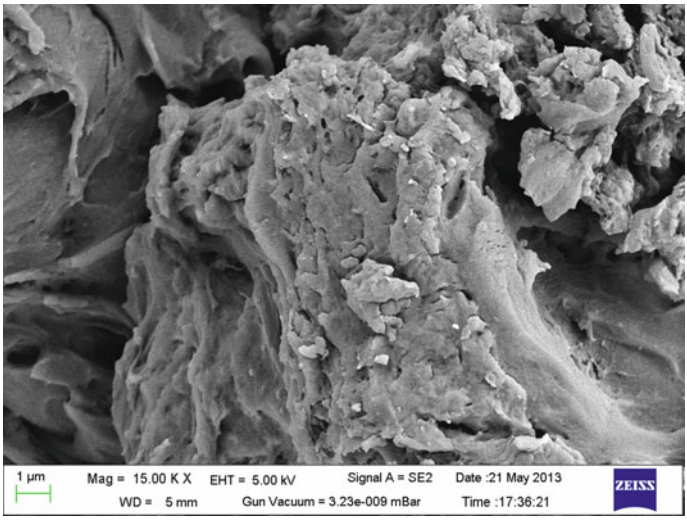

Fig. 8 SEM image of f-MWCNT/PMMA composite with 0.3 wt% of f-MWCNTs

FESEM of the tensile cleavage of f-MWCNT/PMMA nanocomposite reinforced by 0.3 and 0.5 wt% of f-MWCNT is shown in Figs. 8 and 9. In Fig. 8, it is noticed that there is number of voids created in PMMA matrix, whereas these pores are minimized with the increase in percentage of f-MWCNT in 0.5% in Fig. 9. The average size of pores is 1 µm. The nanodispersion of f-MWCNTs in the PMMA as in Fig. 9 shows lesser voids in composites. The lesser interfacial adhesion between f-MWCNT and PMMA matrixes and voids leads to local agglomeration of f-MWCNT on the matrix surface.

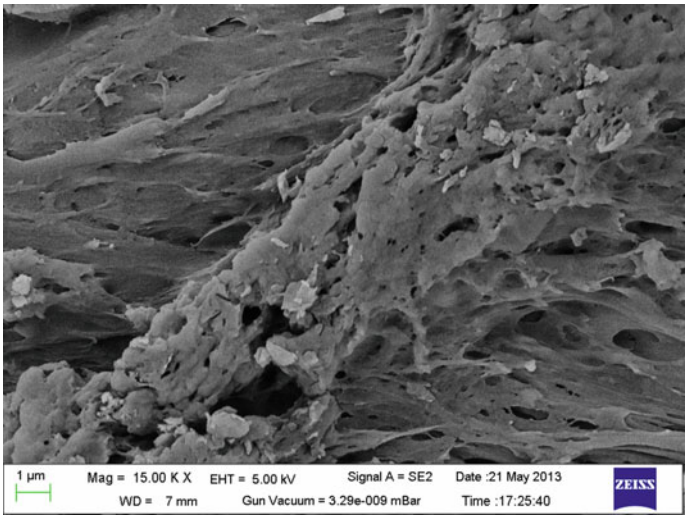

Fig. 9 SEM image of f-MWCNT/PMMA composite with 0.5 wt% of f-MWCNTs

4 Conclusions

The tensile stress and modulus have been increased for the composites with the increase in percentage of the f-MWCNT. This trend is observed for up to a certain percentage with increase of f-MWCNT and then declined due to agglomeration in the viscous polymer. Similar fashion is also observed for flexural stress and flexural modulus. The impact test results show a declining trend of values for the increasing wt% of f-MWCNTs, showing that composites have low impact strength than pure polymer. The increase in electrical conductivity for 0.3–0.5 wt% addition of f-MWCNTs ascertains the electrical conductivity property of nanocomposite. The decrease in the mechanical strength after certain percentage of f-MWCNTs addition points toward the challenges in dispersion of CNTs.

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Performance Analysis of Dual Metal Double Gate Tunnel-FETs for Ultralow Power Applications

D. Gracia and D. Nirmal

Abstract Dual metal double gate tunnel FET device has been presented to overcome the challenges in conventional TFET. This device gives a very good I_{on}/I_{off} ratio and an average subthreshold slope. The performance analysis is done for various values of oxide thickness and doping concentrations for the device. It has very low leakage current (9.27×10^{-20} A/μm), a huge on-current (4.85×10^{-7} A/μm), I_{on}/I_{off} ratio of 10^{12}, and a steep subthreshold slope of 34 mV/dec.

Keywords Dual metal · Tunnel FET · High-*k* dielectric · Subthreshold slope

1 Introduction

Tunnel field-effect transistors (TFETs) are the upcoming devices for its less leakage current and steep subthreshold slope and are much useful to applications which use less power [1–3]. TFETs are based on the passage of the majority charge carriers and an electric field formed in the channel region which is the switching mechanism for tunneling [2–5]. The conventional TFET is a p-i-n gated structure having non-uniformly doped source and drain, and the carrier passage takes place from one band to another.

The major challenges in TFET are small drive current and ambipolarity. To master these challenges, high-*k* dielectrics in the double gate TFETs are proposed [6, 7]. It increases on-current and reduces the leakage current, and hence, on-to-off current ratio is increased [6]. Device analogue/RF characteristics are investigated for gate–drain underlap area [8]. The device uses non-local path (BTBT) model for

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simulation. Due to the tunneling process, the device requires a fine mesh around area where the switching mechanism takes place. In [9], the tunneling takes place from the source to drain depletion regions. The paper [10] discusses the device electrostatic role of three diverse TFET structures, i.e., tunnel FET with two gates, tunnel FET with different dielectrics, and tunnel FET with two metals with different dielectrics. The latter excels the other two TFET structures.

Several structures are proposed by the researches to enhance the on-current of the TFET. In [11–15, 16] dual-gate tunnel FET with different junction for applications that consumes less power is discussed. Vertical TFET with n- and p- type source underlapped structure with submicron 10-nm technology is discussed [17]. In [18], junctionless tunnel FET and [19] gate all around TFET have been discussed. In [20], a dopingless FET (DL-FET) source/drain (S/D) areas were created by metal work function engineering and show a fine control over short channel effects. The problem of ambipolarity is the device operates for both positive and negative values of gate voltage making the TFETs not suitable for digital circuits. Several techniques [21, 22] to control ambipolarity are reducing the drain electric field, reducing the doping concentration, and using large bandgap heterostructures in the drain end. Molybdenum has been shown as a potential candidate for the future metal gate technology in [23–25].

This paper deals with the performance analysis of dual metal double gate TFET for different doping concentrations, and oxide thickness has been analyzed. The dependence of on-current, off-current, SS on device parameters is studied in detail. Section 2 covers the structure design and simulation. Section 3 summarizes the findings and discussion. Section 4 provides the conclusion followed by acknowledgment and references.

2 Structure Architecture and Parameter Description

In Fig. 1, the 2-D structure of double metal dual-gate TFET is shown. The structure creation and the simulations are performed using Sentaurus Technology Computer-Aided Design (TCAD) software [26]. The gate oxide thickness (T_{ox}) is 2 nm with channel thickness of 10 nm. Molybdenum and aluminum are used as metal with the minimum energy of 4.4 and 4.0 eV, respectively. In addition to conventional SiO_2, high-k dielectric HfO_2 is used as gate oxides. The source region is heavily doped with p-type material, while the drain is oppositely doped with n-type impurities. The most important models used for simulation are non-local BTBT model, bandgap narrowing model, SRH model. The transfer characteristics of dual metal gate with heterodielectric TFET have been investigated by varying doping concentrations and thickness of gate oxides.

Table 1 gives the structure dimensions. Figure 2 gives the band diagram of the device in its active as well as in off state. The graph is plotted between the energy band and the position along the length of the device. In its put off state, tunneling

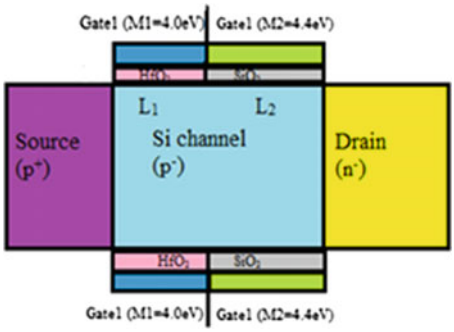

Fig. 1 2-D structure of dual metal double gate TFET

Table 1 Device dimensions

Parameter	Values
Gate length (L_g)	50 nm
Oxide thickness (T_{ox})	2 nm
Channel thickness (T_{si})	10 nm
Source concentration (N_a)	$1e^{20}$ cm^{-3}
Channel concentration (N_{ch})	$1e^{15}$ cm^{-3}
Drain concentration (N_d)	$1e^{18}$ cm^{-3}
Gate voltage (V_g)	2 V
Supply voltage (V_d)	0.5 V

does not occur if the gate bias is very low due to the barrier width between the valence band of the source area and the conduction band of the channel area are high. Furthermore, in the active case, for positive gate bias, the barrier width, a potential boundary leading to tunneling of carriers, is reduced because the gate pulls down the barrier closer to each other.

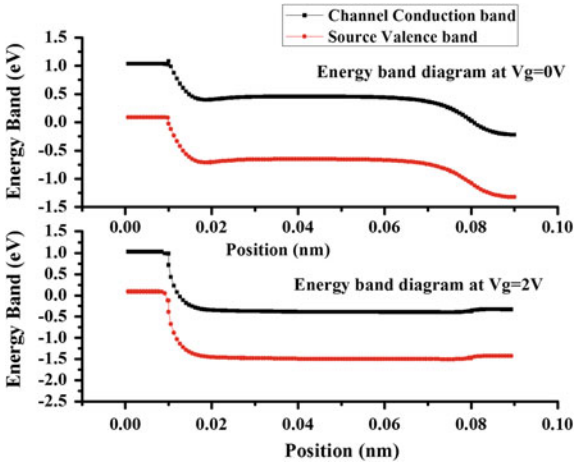

Fig. 2 Energy diagram of dual metal double gate TFET

3 Results and Discussion

3.1 Transfer Characteristics

Figure 3a gives the dual metal double gate TFET transfer characteristics. The analysis has been carried out by swinging the V_g from 0 to 2 V, and the drain current variation is observed. The simulated on-current of the device is 4.85×10^{-7}, and the leakage current is 9.27×10^{-20} giving a very good I_{on}/I_{off} ratio in the order of 10^{12} for a low supply voltage of V_{dd} = 0.5 V. In TFET [27], BTBT is the primary device physics to be modeled. This is fundamental to all lateral BTBT devices. In the simple local BTBT model, the carrier generation rates are determined mainly from the local electric field only [27]. In one common expression, based on the Kane's derivation,

$$G^{\mathrm{BTBT}} = A \cdot E^{\alpha} \exp\left(-\frac{B}{E}\right) \tag{1}$$

Figure 3b shows the $I_d - V_d$ of the device. The analysis is carried out by swinging the drain voltage from 0 to 0.7 V for different gate voltages. The drain current is 4.8457×10^{-7} A.

3.2 Steeper Switching Behavior

The subthreshold swing is the variation in voltage that is used in order to provide a change of one order of magnitude of the drain current. Subthreshold swing is given by

$$S = \frac{dvg}{d(\log Id)}\,[\mathrm{mV/dec}] \tag{2}$$

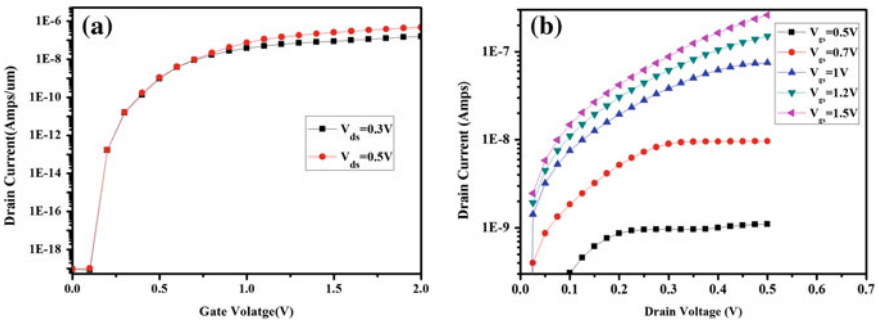

Fig. 3 **a** $I_d - V_d$ for different V_{ds}, **b** $I_d - V_d$ for different V_{gs}

The operating mechanism of MOSFET is based on thermionic injection where electrons travel over an energy barrier, which confines the SS by the Boltzmann distribution of charge to 60 mV/decade. For dual metal double gate TFET, sub-threshold swing is 34 mV/decade. Using high-k in gate oxide provides a steeper slope.

3.3 Effects of Various Doping Concentrations

Figure 4 shows the device characteristics for different doping concentrations. Doping concentration is proportional to on-current, and therefore, increasing source doping will enhance the drive current of the device even at low supply voltage, and hence, TFETs are promising candidates to low power applications.

3.4 Effects of Different Oxide Thickness

Figure 5 shows the $I_d - V_g$ for different oxide thickness keeping the supply voltage 0.5 V. Oxide thickness plays a vital role in the tunneling mechanism. According to the Eq. (3), the current in the active state (on-current) will increase by increasing the oxide thickness of the transistor.

$$I_d = \mu_n c_{ox} \frac{w}{l} \left[\left(V_{gs} - V_t \right) V_{ds} - \frac{V_{ds}^2}{2} \right] \tag{3}$$

where mobility is given by μ_n, c_{ox} is the capacitance of the gate oxide, w/l is the scaling parameter.

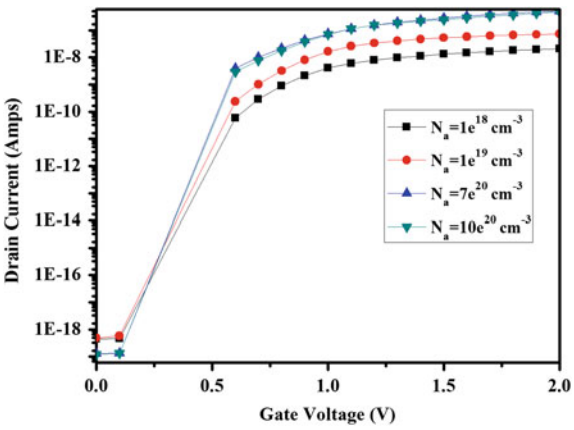

Fig. 4 $I_d - V_g$ for different doping concentrations

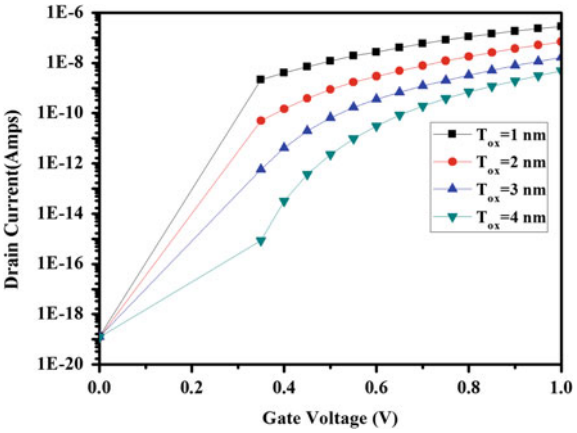

Fig. 5 $I_d - V_g$ for different oxide thickness

where oxide capacitance is given by,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{4}$$

4 Conclusion

The dual metal double gate TFET and their characteristics for different device parameter are discussed. This device gives excellent I_{on}/I_{off} ratio of 10^{12} for a very small supply voltage of 0.5 V. Drive current can be increased by increasing the doping concentration and by using thin gate oxide. The dual metal double gate TFET device is a good candidate for applications that use less power. This work can be extended further by using Ge and III–V materials to enhance the mobility.

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Films of Reduced Graphene Oxide-Based Metal Oxide Nanoparticles

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Abstract Functional materials based on reduced graphene oxide (rGO) and metal oxide nanoparticles possess superior properties arising from the synergy of the individual properties. Obtaining these materials in the form of large area films are advantageous for most applications involving sensing, photovoltaics, supercapacitors, etc. We have synthesized free standing, thin films of rGO with semiconductor nanostructures such as ZnO, CuO, SnO_2, and magnetic nanoparticles such as Fe_2O_3 at a liquid/liquid interface employing a simple interfacial reaction of the precursors. The method can be adopted as a general route to prepare rGO-based metal oxide films. rGO-ZnO films consist of hexagonal cylinders of ZnO, and rGO-Fe_2O_3 films exhibit particle or rod-like morphologies of iron oxide interspersed with rGO layers. The applications of these hybrid films as renewable surface-enhanced Raman substrates (SERS) and supercapacitors are demonstrated. The higher photodegradation rates provided by the metal oxide-rGO hybrids enable regeneration of the used SERS substrate while the contribution from electric double layer capacitance of rGO and pseudocapacitance due to metal oxide enhances the charge storage in hybrids.

Keywords Reduced graphene oxide · Hybrid films · Metal oxides
SERS · Supercapacitor

1 Introduction

Nanoscale metal oxides is one of the most exciting and widely investigated research areas by the scientific community due to their remarkable applications in various fields such as pollutant removal, photovoltaics, photocatalysis, solar cells,

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surface-enhanced Raman spectroscopy (SERS), and supercapacitors [1]. Combining graphene or its derivatives such as reduced graphene oxide (rGO) with metal oxides can offer materials with superior properties for the applications. rGO possess exceptional properties like high electrical conductivity, surface area, optical, mechanical, and thermal properties [1]. A variety of methods have been explored to synthesize rGO-based metal oxide composites such as solution-based methods, solvothermal, and sonochemical techniques [1]. Liquid/liquid interface method is one of the upcoming methods [2] and has not been explored to a great extent even though it has many advantages. The interface is a non-homogeneous and nanometer scale region, which is formed between two immiscible liquids consisting of polar and nonpolar solvents and provides a confined environment to self-assembly of materials at an interface. The assembly of nanostructures minimizes the interfacial energy, and hence, the formation of materials at the interface is thermodynamically favoured. This may be utilized to obtain large area, ultra-thin, self-assembled films of rGO with various inorganic nanostructures. The films obtained are free standing and enable facile transfer to any desired substrate depending on the envisaged application.

In this study, we exploit in situ interfacial reaction at the water/toluene interface for the synthesis of metal oxides and rGO-metal oxide hybrid films including ZnO, rGO-ZnO, Fe_2O_3, and rGO-Fe_2O_3. Here, GO acts as a surfactant to hold the metal oxide nanoparticles (NPs) at the interface and the NPs are seen well anchored on the surface of self-assembled rGO sheets at the interface. These large area ultra-thin films of rGO-metal oxides NPs are collected on various substrates for demonstration as promising SERS substrates that are renewable and electrode materials for supercapacitors. We have also synthesized rGO-CuO and rGO-SnO_2 NP hybrid films employing this method and demonstrated their potential as reusable SERS substrates for fluorescent analytes [3].

2 Experimental Details

2.1 Synthesis of rGO-Metal Oxide NP Films

The hybrid films of rGO-ZnO, rGO-CuO, rGO-SnO_2, rGO-Fe_2O_3 were prepared by taking the corresponding metal acetylacetonate in toluene phase and GO along with hydrolyzing agent in the aqueous phase. Generally, the hydrolyzing agents used were KOH or ammonia, and in the case of Fe_2O_3, dimethylamine was used. In a few cases, a reducing agent, tetrakis(hydroxymethyl)phosphonium chloride (THPC) was also added in the aqueous phase to facilitate GO reduction. The whole system was heated at 90 °C in an oil bath for 2 h. After 1 h, an ultra-thin film of rGO-metal oxide NPs is observed at liquid/liquid interface. The films were collected on desired substrates after the toluene evaporation.

3 Results and Discussion

The liquid/liquid interface method for the synthesis of rGO-based metal oxide NP hybrid films involves taking a metal precursor in the organic phase over a GO dispersion along with the required reagent for interfacial reaction. The reduced GO adsorb the hydrolyzed metal ions followed by self-assembly at the interface. The hydrolysis and reduction of metal precursor and GO at the interface are facilitated by the increased thermal motion of reagent molecules during heating [4, 5]. Figure 1 displays the schematic of the method.

The crystal structure of hybrid films are studied by XRD and depicted in Fig. 2a. XRD patterns of ZnO and rGO-ZnO films confirm that ZnO has crystalline nature and the peaks at 31.8° (100), 34.4° (002), 36.3° (101), 47.6° (102), 56.7° (110), 62.9° (103), 66.4° (200), 67.9° (112), 69.2° (201), 72.7° (004), and 77° (202) correspond to hexagonal wurtzite structure of ZnO. Fe_2O_3 films and rGO-Fe_2O_3 hybrid films show peaks corresponding to a mixture of α and γ phases, 33.2 (α104), 35.6 (γ311), 40.5 (α113), 53.7 (γ422), 62.5 (α214), and 62.9 (γ440). In the case of rGO-metal oxide hybrid films, a broad amorphous peak is observed at 23° due to exfoliated rGO layers. The optical absorption of as-synthesized hybrid films are given in Fig. 2b, and ZnO, rGO-ZnO, Fe_2O_3, and rGO-Fe_2O_3 exhibit the absorption bands at 350, 360, 414, and 476 nm, respectively. The band edge absorption for ZnO and rGO-ZnO are close to that seen for bulk ZnO (370 nm). In the case of rGO-metal oxides, the absorption extended into the visible region due to the presence of rGO layers. The π-π* transition of rGO absorption is seen at 265 nm. Inset of Fig. 2b shows the Tauc plot of Fe_2O_3 and rGO-Fe_2O_3 films. The band gap values are in the range of 2.4 and 2.9 eV, respectively. The band gap values are higher than the bulk Fe_2O_3 (2.1 eV). FTIR spectra of hybrid films (Fig. 2c) show signatures of acetylacetonate and dimethylamine in addition to rGO and metal oxide features. In the case of rGO-ZnO film, the band at 447 cm^{-1} corresponds to ZnO vibration and the other vibrational bands around 1026, 1108, 1423 cm^{-1} correspond to the ρCH_2, τCH_2, τCH_3, of acetylacetonate, respectively. In the case of rGO-Fe_2O_3 hybrid film, two major broad peaks at 460 and 580 cm^{-1} correspond to Fe–O bending and stretching vibration modes of Fe_2O_3 and the bands at 3334 and 1035 cm^{-1} belong to the N–H and C–N stretching vibrational modes of dimethylamine. This indicates that ligands from the precursors attach to metal oxide

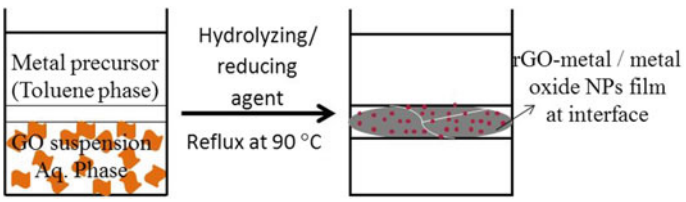

Fig. 1 Pictorial presentation of the liquid/liquid interface method for the preparation of rGO-metal oxide NP hybrid films

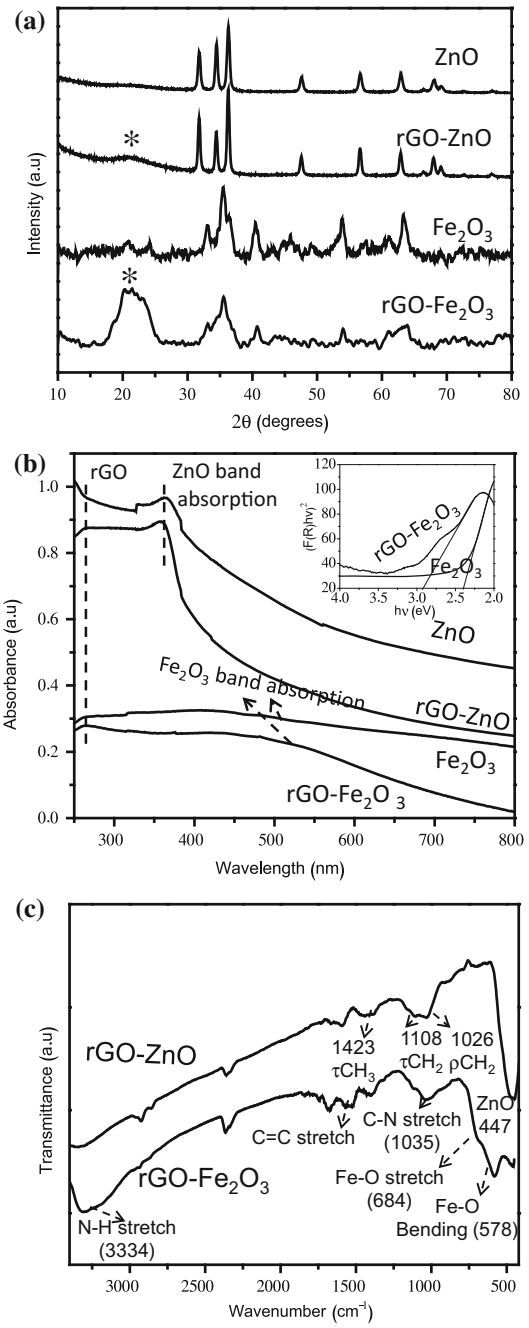

Fig. 2 **a** XRD patterns; *amorphous peak of rGO, **b** UV-visible absorption spectra; inset shows the Tauc plots for band gap determination of Fe_2O_3 and rGO-Fe_2O_3, **c** FTIR spectra of the as-synthesized hybrid films ZnO, rGO-ZnO, Fe_2O_3, and rGO-Fe_2O_3 prepared by liquid/liquid interface method

nanostructures during their formation. The band at 1580–1600 cm^{-1} is observed in both the cases, which is C=C stretching vibration of rGO.

Surface morphology of as-synthesized films of ZnO, rGO-ZnO, Fe_2O_3, and rGO-Fe_2O_3 NPs are given in Fig. 3. Figure 3a shows the bare ZnO NPs, which are hexagonal in shape and majority of them are seen stacked together to form a cylindrical shape. In the case of rGO-ZnO (Fig. 3b), the hexagonal cylindrical ZnO NPs are well anchored on the surface of the rGO sheets. The dimensions of ZnO NPs are highly polydisperse and are in the range of 70–90 nm in width and 50–80 nm in length (Fig. 3e). The inset of Fig. 3b shows a magnified image of one such ZnO cylinder. Bare Fe_2O_3 films show small Fe_2O_3 NPs (Fig. 3c) that are aggregated and interconnected to form dendritic network structures. In the case of rGO-Fe_2O_3 (Fig. 3d), Fe_2O_3 particles are rod-shaped and aggregates of nanorods (NRs) form flower-like structures on rGO layers. The length and width of Fe_2O_3 NRs on the rGO are 120–240 nm and 40–80 nm, respectively (Fig. 3f).

The potential application of rGO-zinc oxide hybrid films as reusable SERS substrates has been explored and is shown in Fig. 4. We have examined Raman spectra of Rhodamine 6G (R6G) as a fluorescent analyte. Figure 4 shows Raman spectra of 1 mM R6G adsorbed on the surface of bare ZnO and rGO-ZnO NPs coated on glass substrates (10 μL of 1 mM R6G was drop cast on the film, washed and dried). Raman band signatures of R6G are seen at 623, 784, and 1184 cm^{-1}, corresponding to the in-plane C–C–C ring, out of plane C–H bending and C–C stretching vibrational bands of R6G, respectively. The Raman bands at 1314, 1368, 1523, 1592, and 1647 cm^{-1} correspond to the C–C stretching vibrations of R6G [6]. R6G Raman bands on rGO-ZnO hybrid film appear significantly enhanced compared with that of bare ZnO NPs film with a slight suppression in the fluorescence background. The enhancement is attributed to the synergic contribution between rGO and metal oxide NPs, and also charge transfer between the analytes, rGO, and metal oxide NPs. The possible charge transfer pathways are (1) photoexcitation of electrons in ZnO to the defect levels by visible light radiation, which is employed for Raman scattering and further transfer to LUMO of analyte molecules (2) photoexcitation of electrons in HOMO-LUMO levels of dye molecules by visible light and further transfer to the conduction band of ZnO or rGO, which leads to the quenching of the fluorescence of the analytes and enhancing the Raman bands. In the case of rGO-ZnO NP hybrid film, the remnant oxygen functional groups present on the rGO sheets can enhance the local electric field, which also contributes to the enhancement in Raman bands in addition to charge transfer that leads to the suppression in the fluorescence of the analyte. To know the quantitative enhancement in the Raman bands of R6G on the hybrid films, enhancement factor (EF) has been calculated from the following equation [6].

$$\mathrm{EF} = I_{\mathrm{SERS}}/I_{\mathrm{Bulk}} \times N_{\mathrm{Bulk}}/N_{\mathrm{SERS}},$$

where N_{bulk} is the number of the probe molecules under laser illumination in the bulk sample and N_{SERS} is the number of the molecules probed on the hybrid nanoparticle substrate, respectively. I_{SERS} and I_{bulk} are the vibrational intensities of

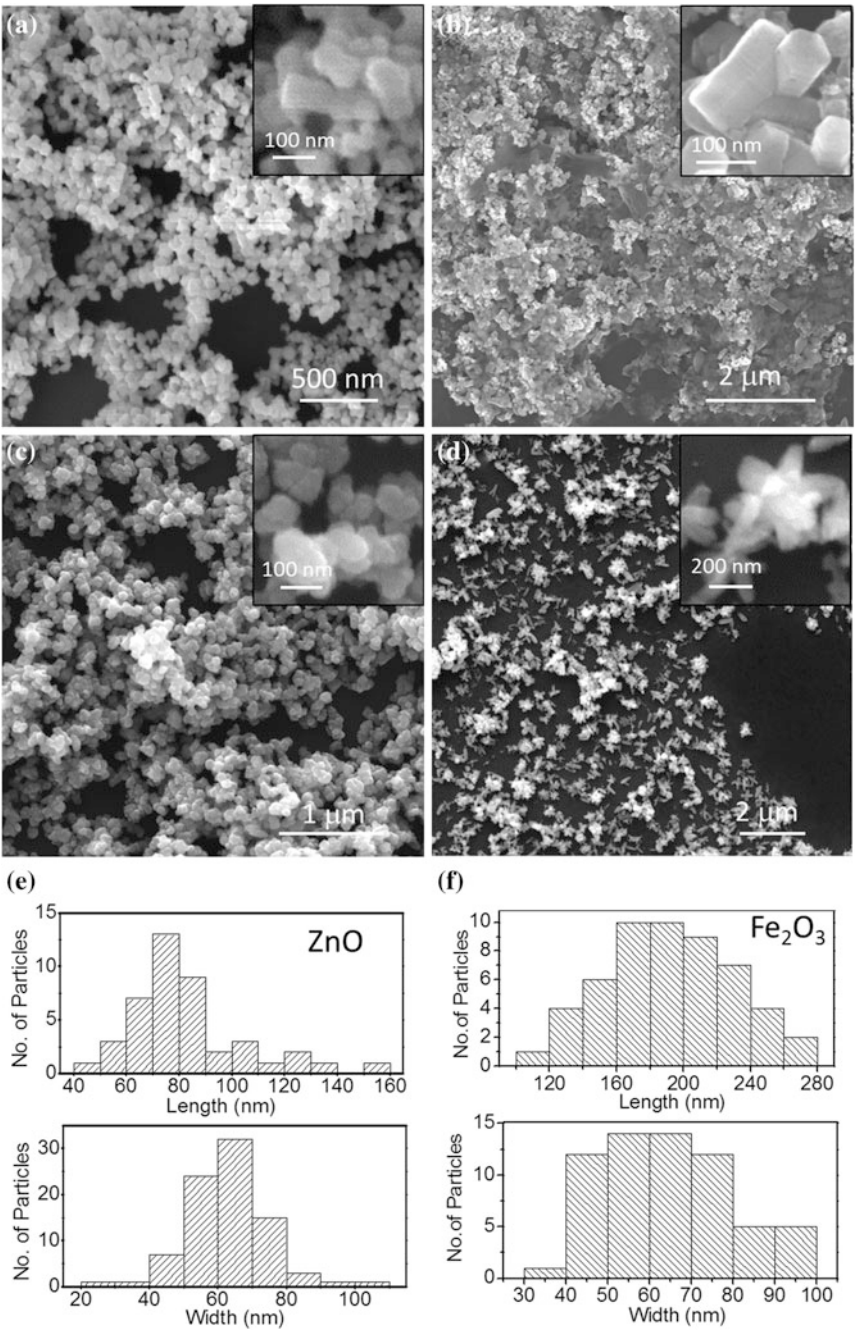

Fig. 3 Surface morphology of metal oxide and rGO-metal oxide hybrid films prepared by interfacial reaction **a** ZnO NPs, **b** rGO-ZnO NPs, **c** Fe_2O_3 NPs and **d** rGO-Fe_2O_3 NPs; insets show the magnified FESEM images, **e** Hexagonal ZnO particles size distribution histogram, **f** Fe_2O_3 nanorods size distribution histogram

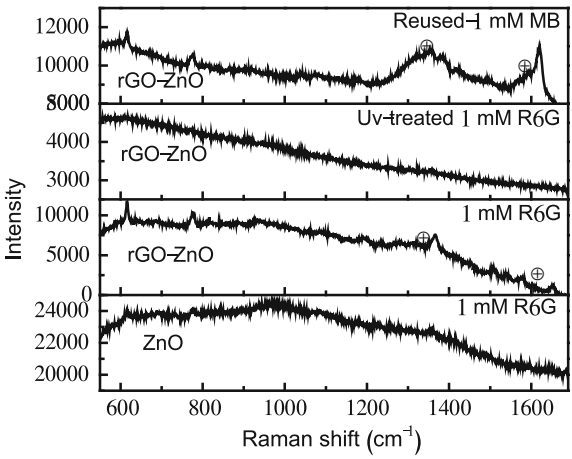

Fig. 4 SERS spectra of 1 mM R6G adsorbed on the surface of bare ZnO and rGO-ZnO NP hybrid film coated on glass substrate along with reusability of rGO-ZnO hybrid film as SERS substrate (⊕Raman bands of rGO)

R6G with excitation of 532 nm laser. The calculated EF values are $\sim 4.15 \times 10^2$ for rGO-ZnO NP hybrid and $\sim 9.5 \times 10^1$ for bare ZnO NPs film (1 mM R6G). We have studied the reusability of the rGO-ZnO NP hybrid film as a SERS substrate for various analytes, R6G, and methylene blue (MB). It has already been shown that when ZnO nanoparticles are combined with rGO, the recombination rates of photogenerated electrons and holes can be suppressed, which are further available for degradation of dyes. Thus, the photocatalytic efficiency of rGO-ZnO is much higher than bare ZnO [7]. This has been exploited to achieve renewable SERS substrates by degradation of adsorbed dye molecules. The surface of rGO-ZnO hybrid films is irradiated with UV light (365 nm) for 30 min in wet condition to regenerate the fresh surface. SERS spectra of R6G before and after photodegradation along with that of MB dye adsorbed on the regenerated substrate are also shown in Fig. 4. After UV light irradiation, the signatures of R6G disappeared and only a featureless background is observed. The regenerated surface is used for the detection of another dye, MB. The signatures of MB are clearly seen in the Raman spectra. A similar trend is observed in the case of rGO-CuO and rGO-SnO_2 NP hybrid films.

The capacitive behavior of Fe_2O_3 and rGO-Fe_2O_3 films is studied by cyclic voltammetry (CV) in 2 M KOH aqueous electrolyte at room temperature using three electrode systems. For this, the films were coated on to pencil graphite and are used as working electrodes. CV measurements were performed at various scan rates in the potential window, −1.2 to 0 V (vs. Ag/AgCl) and are shown in Fig. 5. The cyclic voltammetry graphs exhibit distinct redox peaks in the anodic and cathodic sweep within the voltage range of −1.2 to 0 V. The redox peaks are well defined in the rGO-Fe_2O_3 hybrid films compared with the bare Fe_2O_3 film (see inset of Fig. 5). The redox peaks arise because of the reversible conversion of iron oxidation states $Fe^{2+} \leftrightarrow Fe^{3+}$ [8]. The charge storage process is due to the diffusion of K^+ or H_3O^+ ions and e- within Fe_2O_3 contributing to pseudocapacitance. The effect of scan rate has also been investigated, we observe that the current density and the area under the redox peaks increase with increasing scan rate, which indicates the fast diffusion

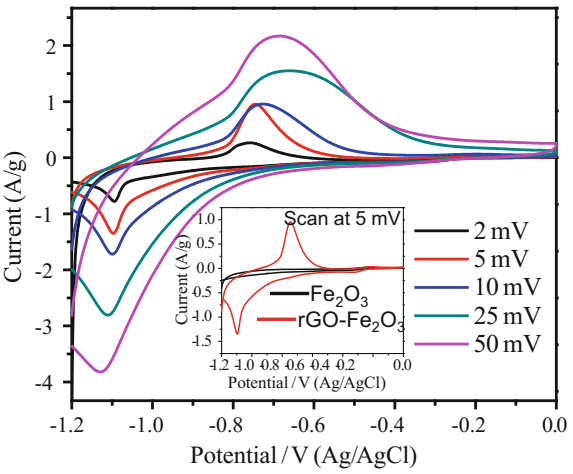

Fig. 5 CV graphs of rGO-Fe_2O_3 hybrid films coated on to pencil graphite electrodes with various scan rates; Inset of Fig. 5 shows the CV of bare Fe_2O_3 and rGO-Fe_2O_3 NRs at a scan rate of 5 mV/s

of electrolyte ions onto the surface of electrode materials. In the case of rGO-Fe_2O_3 NR hybrid film, the area under the curve (inset of Fig. 5) is much higher than the bare Fe_2O_3 NPs. The specific capacitance has been calculated from the CV curves of hybrid films using the $C = a/2mv\Delta V$, where a is the integrated area of the CV cycle, m is the mass of the electrode material (g), v is the scan rate (V/s), and ΔV is the potential voltage window [9]. At a scan rate of 2 mV/s, the values for bare Fe_2O_3 and rGO-Fe_2O_3 NR hybrid are 9.8 and 47.5 F/g, respectively. A higher capacitance is observed in the case of rGO-Fe_2O_3, which is ~fivefold higher than the bare Fe_2O_3. This is due to the synergic property between the rGO and Fe_2O_3 arising from contributions due to double layer capacitance of rGO and pseudocapacitance of Fe_2O_3 NRs. rGO also provides large surface area and aids in the transport of electrons from Fe_2O_3 to the current collector.

4 Conclusion

We have demonstrated a general route to prepare rGO-based metal oxide hybrid films employing liquid/liquid interface method. The free-standing films formed at the interface are thin, uniform, and are transferable to any desired substrates. The morphologies of metal oxide nanostructures are found to vary with the type of metal oxide involved. rGO-ZnO and rGO-Fe_2O_3 films have been demonstrated as reusable SERS substrates and electrode materials for supercapacitors, respectively. SERS enhancement factor for rGO-ZnO is 4.15×10^2 for R6G dye, and the surface has been regenerated by UV exposure for probing a different dye. rGO-Fe_2O_3 films exhibit fivefold higher capacitance than the bare Fe_2O_3 film. The synergic effect between the rGO and metal oxide plays important role in the enhanced performances.

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Size Optimization of InAs/GaAs Quantum Dots for Longer Storage Memory Applications

V. Damodaran and Kaustab Ghosh

Abstract A theoretical model and simulation is presented to express the electron and hole dynamics in InAs/GaAs quantum dots (QDs). For a fixed aspect ratio of 0.3, quantized energy states were computed using eight-band k.p model by varying the QD size and for different operating temperatures. Computational results show alteration in the dynamical behaviour at different temperatures. We obtained longer electron storage capability for 20 nm dot as compared to holes at room temperature operation. However, due to slower tunnelling rate at cryogenic temperatures within 20–50 K, smaller-sized QDs of 12 nm are suitable for memory devices in information storage for greater time span.

Keywords Quantum dots · Memory devices · Carrier dynamics
Theoretical model

1 Introduction

Self-assembled quantum dots (QDs) gained prominence over the years due to its special characteristics such as three-dimensional quantum confinement, 'delta-like' density of states and size-dependent optical spectra. All these qualities are utilized for fabricating high-performance lasers, photodetectors and solar cells [1–6]. However, a new application and research in data processing and data storage is witnessed for QDs in the last decade, and this function is utilized in the generation of memory devices [7–13]. The QDs in the memory devices can be employed to store information or data in the form of charge carriers. Carriers stored in the QD can escape through thermal and tunnelling emissions, and the rate of these emissions is the key parameters that describe memory performance in terms of its data retention potentiality. Hence, in this paper, theoretical modelling and simulation is

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presented to describe the carrier flow dynamics in InAs/GaAs QD and understand its information storage capability. The aim of this work is to optimize the performance of the device and design superior quality memory devices.

It is well known that the control over the dimensions of nanostructures can be employed to engineer the material properties for specific applications. Hence, change in the size of the dots can be utilized to alter the confinement potential which causes a change in the charge emission characteristics. This in turn leads to the change in the data retention capability for memories. In view of the same, we have carried out a comparative analysis on the emission characteristics for electron and holes in different-sized QDs. Arrhenius plots for the same are computed to elucidate the effects of temperature which are analysed and discussed.

2 Theoretical Model

We developed our theoretical model for a truncated pyramidal InAs/GaAs QDs which are embedded in the depletion region of a reverse-biased *p*-*n* junction diode as shown in Fig. 1a. We assumed a forward pulse of 20 ms which reduces the depletion width of the diode. For a p^+-*n* diode structure, forward biasing places the QD layer inside the *n*-type region of the diode as shown in Fig. 1b. This cause the capture of the majority carrier electrons in the dot, and the rate of capture is given by [13]

$$c_n = \gamma_n X \sigma_{\text{th}}^n T^2 \exp\left(-\frac{\Delta E_{\text{C}}}{k_{\text{B}} T}\right) \tag{1}$$

where X is the spin degeneracy factor, σ_{th}^n is the capture cross section for electrons, ΔE_{c} is the change in the conduction band energy at the interface of the dot and the barrier material, and γ_n is a temperature-independent constant given by

$$\gamma_n = \sqrt{2(2\pi)^3}\left(k_{\text{B}}^2/h^3\right) M_{\text{c}} m_{\text{e}}^* \tag{2}$$

where M_{c} is the number of conduction band minima and m_{e}^* is the electron effective mass.

For a n^+-*p* diode, forward biasing places the dot in the *p*-side of the diode and causes hole capture into the dot, the rate of which is given by

$$c_{\text{p}} = (\gamma_{\text{p}}/X)\sigma_{\text{th}}^p T^2 \exp\left(-\frac{\Delta E_{\text{V}}}{k_{\text{B}} T}\right) \tag{3}$$

where ΔE_{V} is the change in the valence band energy at the dot–barrier interface.

After the forward bias pulse, captured electron in the dot escapes from the QD through thermal and tunnelling emissions.

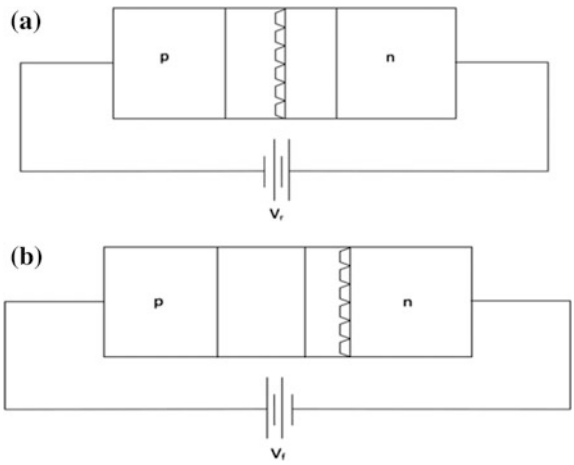

Fig. 1 **a** Schmatic sketch of the reverse baised *p-n* junction diode with InAs/GaAs QDs embedded in the depletion layer. **b** Forward biased diode p^{+}-*n* diode which places the QDs in the *n*-region for carrier capture

The thermal emission of electrons from the QD is given by [7]

$$e_{\text{th}} = \gamma_n X \sigma_{\text{th}}^{n} T^2 \exp\left(-\frac{E_{\text{A}}}{k_{\text{B}} T}\right) \tag{4}$$

Here in Eq. (4), E_{A} is the activation energy of the electron which is defined as the energy difference between the conduction band of the barrier and the quantized energy state of the electron. We have used eight-band k.p model to compute the quantized state of the electrons and hole. The computation was performed using Tiber CAD simulation software.

In the similar manner, thermal emission for holes can also be computed as Eq. (4) by considering the capture cross section σ_{th}^{p}, temperature-dependent constant γ_{p} and the activation energy for holes.

Apart from thermal emission, electrons can also undergo quantum mechanical tunnelling emission from the QD. One such emission is the direct tunnelling through the one-dimensional triangular potential barrier from the QD, the rate of which is given by [13]

$$e_{\text{dt}} = \frac{qF}{4\sqrt{2m_{\text{e}}^{*} E_{\text{A}}}} \exp\left(-\frac{4}{3}\sqrt{\frac{2m_{\text{e}}^{*}}{\hbar^2}}\frac{E_{\text{A}}^{3/2}}{qF}\right) \tag{5}$$

where 'F' is the applied electric field.

Another is the phonon-assisted tunnelling in which electron from the lower quantized state is excited to the highest bound state thermally and then tunnels through the barrier layer. The phonon-assisted tunnelling rate is given by [11]

$$e_{\text{pht}} = \gamma_n X \sigma_{\text{tun}}^n T^2 \int_0^{E_A} \exp\left[(-E_A/k_B T) + \left(4\sqrt{2m_e^*}E_B^{3/2}/3\hbar qF\right)\right] dE_A \quad (6)$$

Here in Eq. (6), E_A is the energy difference between the lower quantized state and the highest bound state of the QD, and E_B the barrier energy which is to be ascertained from the highest bound state to the conduction band edge.

The total emission rate of electrons from the QD can be expressed as

$$e_{\text{tot}} = e_{\text{th}} + e_{\text{dt}} + e_{\text{pht}} \quad (7)$$

3 Results and Discussions

Arrhenius plots of electron emission for QDs of different size are presented in Fig. 2 for temperature ranging from 10 to 300 K. The emission curve for QD size of 14 nm is seen to flatten at lower temperature range of $30 \leq 1000/T \leq 100$ which can be ascribed to the temperature-independent direct tunnelling from the QDs. For higher temperatures $1000/T \leq 30$, the curve is seen to increase with a particular slope. This can be ascribed to the overriding of thermal emission over tunnelling in the aforesaid temperature range. The emission curve slope for QDs of other three sizes is seen to increase with increase in temperature. This can be attributed to the dominance of phonon-assisted tunnelling at lower temperatures followed by thermal emission at higher temperatures. The inset in Fig. 2 shows the Arrhenius plots at the higher temperature side from $1000/T \leq 10$. In this temperature range, it can be seen that the large-sized QD of 20 nm base dimension is having the lowest emission rate. This is due to the largest confinement potential of the electron captured in this dot as compared to the other dot sizes. Defining the storage time as the inverse of emission rate, it can thus be inferred that at room temperature, larger QD size can be suitably utilized for fabricating memory devices having longer duration data storage capacity. We have not considered dot size larger than 20 nm as it might lead to coalescence of dots and structural defects. However, with decrease in temperature for $20 \leq 1000/T \leq 80$, the emission rate for 20-nm dot increases compared to the other QD, and it can be seen that the smaller QD size of 12 nm is having the least emission rate. This attributes to the suitability of smaller-sized QDs for better memory applications at cryogenic temperatures.

Arrhenius plot for hole emission from the InAs/GaAs QD is depicted in Fig. 3. The inset in the figure shows the same at the higher temperature range, which also portrays lowest emission rate for holes for larger-sized QD of 20 nm dimension. Even at lower temperatures, unlike that of electrons, the emission rate from this QD is the least. Hence, it can be inferred that QDs having larger dimension are

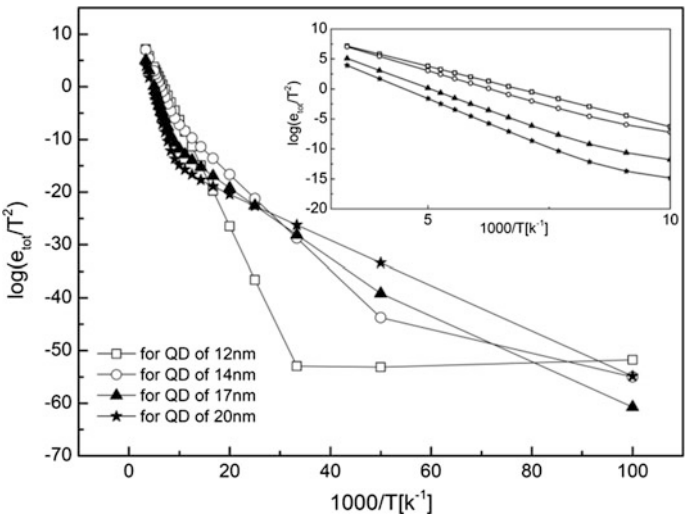

Fig. 2 Arrhenius plot for electron emission rate for QDs of different base dimensions

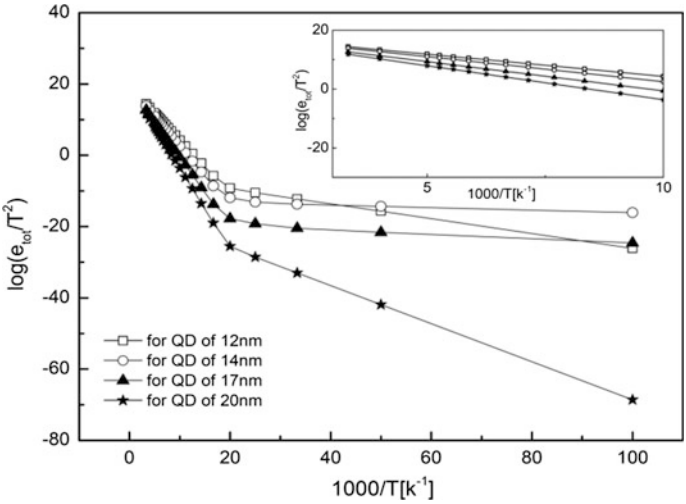

Fig. 3 Arrhenius plot for hole emission rate for QDs of different base dimensions

preferable for longer duration information storage in the form of holes at all temperatures.

Comparison of Arrhenius plot of the electron emission rates for QD size of 20 nm, 12 nm and hole emission for 20-nm QD is presented in Fig. 4. It can be seen that the electron emission is lesser than holes at room temperature for 20-nm dot. With decrease in temperature for $20 \leq 1000/T$, electron emission increases as

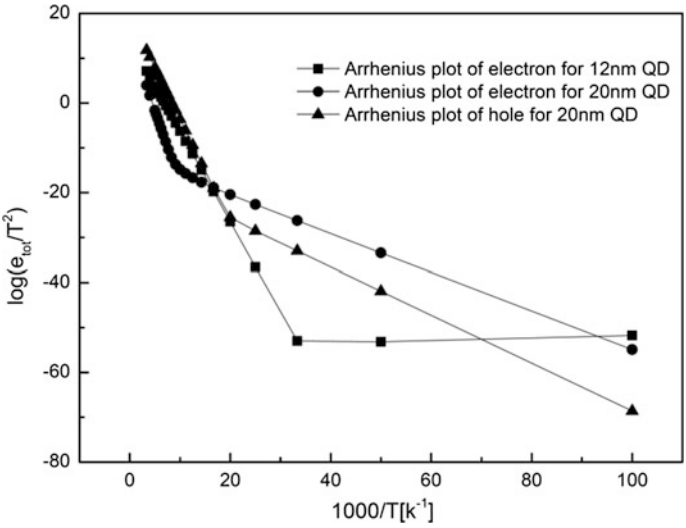

Fig. 4 Comparison on the Arrhenius plot for electrons and holes for different-sized QDs

compared to holes. However, electron emission for 12-nm dot is lesser than holes in the temperature range $20 \leq 1000/T \leq 50$. Thus, from this study, it can be surmised that for InAs/GaAs QD, electrons are preferable than holes for longer storage duration memory devices for a broad range of temperature from 20 to 300 K. Larger-sized QDs is more suited for room temperature memory device, whereas smaller size is suitable for cryogenic devices [14] operating within 20–50 K.

4 Conclusion

In summary, the theoretical modelling and simulation on the carrier flow mechanism in InAs/GaAs QDs described in this paper illustrates the suitability of electrons over holes as information processing and storage for quantum dot memory devices. Our computation predicts large-sized QDs for longer storage of information at room temperature and smaller QD of 12 nm dimension for the same at cryogenic temperatures within 20–50 K. This study thus provides important information and design guideline on the size of the 0-D nanostructure and its role in data storage capability for next-generation memory devices.

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Design and Analysis of a CMOS 180-nm Fractional-N Frequency Synthesizer

P. Parvathy and N. Saraswathi

Abstract The design of a Fractional-N Frequency Synthesizer in CMOS 180-nm that operates in GHz range is discussed. The proposed frequency synthesizer is realized using a phase-locked loop with phase frequency detector (PFD), charge pump, loop filter, voltage controlled oscillator (VCO), and a programmable frequency divider. The characteristics of the PFD are extremely linear as one of the input frequencies is modulated. The frequency divider deigned is a programmable one as it can generate noninteger division ratios unlike an integer PLL.

1 Introduction

A frequency synthesizer finds application in the receiver section of an RF circuit. As the name indicates, a frequency synthesizer synthesizes a wave with a particular frequency. Various circuits are available for this purpose. But frequency synthesizer using PLL is preferred over others. The reason is the phase and frequencies of input and output are not only in locked state but also if PLL needed can track the input frequency.

In [1], a circuit-level model of Fractional-N Frequency Synthesizer for millimeter frequency with a programmable divider in the feedback loop has been discussed. The idea of using D flip-flops had been mentioned in [2] first. Yet the blind zone associated with the design is rather large. Unlike an integer PLL, a fractional frequency synthesizer can generate noninteger division ratios. It provides better step size as resolution increases. The static frequency divider chain is realised using CML latches [3]. The static frequency divider has a fixed frequency division ratio. So the loop band with of the filter is fixed . On the other hand in a fractional

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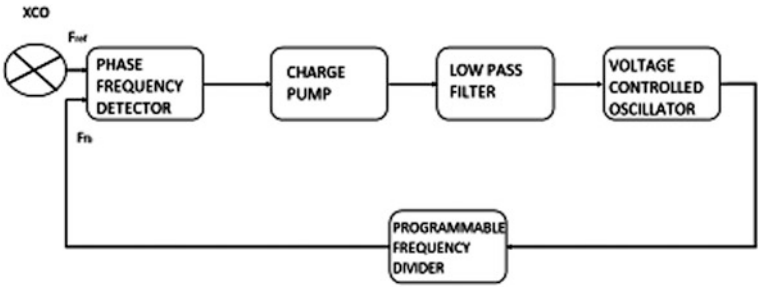

Fig. 1 Block diagram of fractional frequency synthesizer

frequency synthesizer loop band with varier. Different types of PLL architectures are analog PLL [4] digital PLL [5]. High phase noise in PLL is due to quantization error. Different blocks of the proposed system are discussed in the sections given below (Fig. 1).

2 Fractional-N Frequency Synthesizer

The input reference frequency is in GHz range. The reference and feedback frequencies are compared using a phase frequency detector (PFD). The output generated is in accordance to the difference in phase and frequency of the two input signals. The PFD designed minimizes the blind zone by detecting very low offsets in these two frequencies. An active low pass filter follows the phase frequency detector circuit. The center frequency of the voltage controlled oscillator is 2.48 GHz. The feedback path has a programmable frequency divider with a frequency limit up to 2.48 GHz. Unlike integer PLL programmable frequency divider in a fractional frequency synthesizer can generate noninteger frequency division ratio.

3 Phase Frequency Detector (PFD)

A PFD compares the input phase and reference and feedback frequencies and translates the information into proportional UP and DOWN pulses

- When both reference and feedback inputs matched
- When reference leads feedback input
- When feedback leads reference input

are the three operating conditions of PFD (Fig. 2).

In the first case, both the up and down signals are negligible. Yet in the second case up signal is in voltage range while down signal is negligible and vice versa in third case. In the proposed PFD unlike [2] the PFD input connections are rerouted

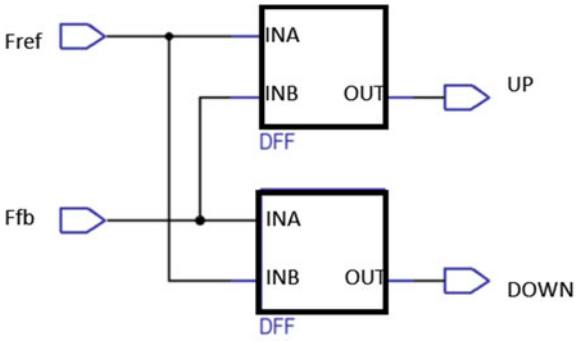

Fig. 2 Phase frequency detector with d flip-flops

to the next flip-flop, thereby eliminating the reset path. The reset signal for the one flip-flop is generated by input of the other

The circuit operation is as follows, when reference frequency is greater, push UP signal to logical high while the other flip-flop is pulled down by reset path. When feedback frequency is greater, DOWN is at logic high the other flip-flop is grounded. The proposed phase frequency detector operates at low power with minimum dead zone. The DFF is enhanced to operate at high frequency, thus ensuing wide loop bandwidth.

4 Charge Pump

Three states of phase frequency detector, PFD, control the charge pump thus it acts as an electronic switch. When either up or down pulses are high owing to the difference in frequencies between feedback and reference signals, a pump voltage V or a pump current I is delivered to the loop filter.

The loop filter is isolated from the charge pump when both up and down signals become negligible. The circuit is realized using 180-nm technology. The (*W*/*L*) ratios of nmos and pmos are taken as 2 µ/180 n (Fig. 3).

5 Loop Filter

Loop filter is the block that follows charge pump in a frequency synthesizer. Since VCOs are usually voltage controlled rather than and current, the loop filter converts the output of the charge pump into a control voltage that drives the voltage controlled oscillator. Loop bandwidth, settling time, and phase noise are the important characteristics of a PLL that is dependent on loop filter design. It can be either passive or active. Most passive loop filters are second order or third order. Higher order filters have capacitor values that are small with respect to the VCO input

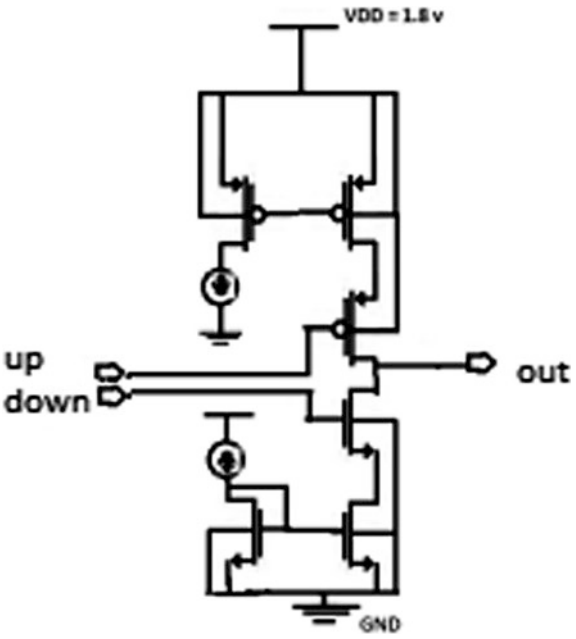

Fig. 3 Charge pump

capacitance. An active loop filter with an operational amplifier is needed when the VCO requires a higher tuning voltage.

6 Voltage Controlled Oscillator

One of the most important building blocks in the frequency synthesizer is an oscillator. It generates periodic signal. The integrated oscillator is of three types: Ring oscillator, source coupled oscillator, and LC oscillator. An LC oscillator could operate at a higher frequency and provide a better phase noise performance compared to ring oscillators. The most popular oscillator topology in the integrated RF transceiver is the cross-coupled oscillator. A cross-coupled transistor pair and a LC resonator together make the oscillator circuit.

For frequency tuning MOS varactor diodes are preferred. Positive resistance dissipates energy while negative resistance generates energy. Negative resistance by the cross-coupled transistor pair generates oscillations. To decrease the sensitivity to the supply voltage in order to suppress the common-mode noise coupling a current source is used. It offers a high-impedance at the common-mode point for proper differential operation. The output of VCO will be a triangular wave. So a buffer is added to get square wave as output. The circuit is designed to work at a maximum frequency of 3 GHz (Fig. 4).

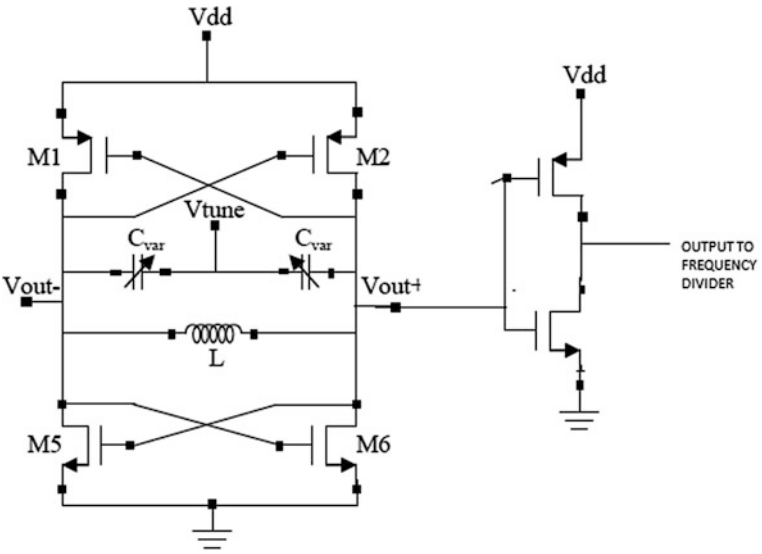

Fig. 4 Voltage controlled oscillator

An LC oscillator suffers from some losses. These losses can be represented as a parallel resistor R_p. Negative resistor is to counterbalance the losses due to R_p. Negative resistance is to generate and sustain oscillations. VCO has cross-coupled pmos and nmos transistors. This is to generate negative resistance.

Inductor has an $R_p = (L.w)Q = R_p = L(2 \times 3.14 \times f_{min})Q$
Assume $L = 1$ nH and $Q = 12$
Then $R_p = 113\ \Omega$
We know that $R_p > 2/g_m$
So here g_m becomes 35.37 mS
Assume the value to be $g_m = 40$
From the I_d equation of transistor in saturation;
$g_m = (2K_p(W/L)I_d)^{1/2}$
Assume $I_d = 5$ mA; K_p for nmos is 200 and that of pmos is 100
So $W_{nmos} = 50\ \mu m$
$W_{pmos} = 100\ \mu m$
[Assume that pmos is scaled twice as much as nmos so that gm would be same]
We know that device capacitances: overlap (c_{gs0} and c_{gd0}) is 0.3 fF/μm^2 and gate oxide capacitance (c_{ox}) is 15 fF/μm^2
The cross-coupled nmos and pmos is called core.
Here consider zero crossings that is both voltages are equal; differential voltage is zero ($V_a - V_b = 0$)
Then the total parasitic capacitance is ½ [$c_{gsn} + 2\ c_{dsop} + c_{gsp} + c_{dson}$].

Table 1 Tuning range of VCO

Tuning voltage (V)	Frequency (GHz)
0	2.51
0.6	2.34
0.9	2.30
1.5	2.23
1.8	2.21

Here the overlap capacitance at saturation is $2/3 \times C_{ox} \times W \times L$

And C_{gs} is $½ \times C_{ox} \times W \times L$

So the C_{core} = 90 fF

The buffer capacitances: $½ [C_{gsn} + C_{dsop} + C_{gsp} + C_{dson}]$ = 33.75 fF

The size of the buffer is determined by the load capacitances

The size of the varactors is determined by its K_v number. Ideal value is determined by trial error method.

The tuning range of VCO is shown in Table 1.

7 Programmable Frequency Divider

One of the unavoidable blocks of the phase-locked loops (PLLs) in a transmitter/receivers is a frequency dividers (FD). The frequency of operation of the divider and VCO are same hence its design determines the maximum usable frequency of the frequency synthesizer. Frequency dividers are of three types: cascaded, dual modulus, and programmable It is important to choose a design that achieves high design flexibility and low-power dissipation. High operating frequency, low noise, and a flexible and wide division factor range are the characteristics of a programmable divider.

Digital frequency dividers are made of digital blocks with latches, flip-flops, and other logic gates. A divider acts as a counter by counting the number of cycles received and once the count is achieved it outputs a slower cycle. The basic building block in frequency dividers is the divide-by-2 block. It can serve as a building block to several other dividers, i.e., a divide by 3 circuit by gating a divider by 2 circuit. It is possible to create dual-modulus prescalers (DMPs) like divide by 4/5 and 8/9, etc. A conventional programmable frequency divider has three blocks a dual modulus (M) prescaler, a program (P) counter, and swallow (S) counter. The prescaler can divide input frequency by $M + 1$ or M, controlled by modulus control input. The program counter can have a frequency division ratio of P. The swallow counter divides the prescaler output by S.

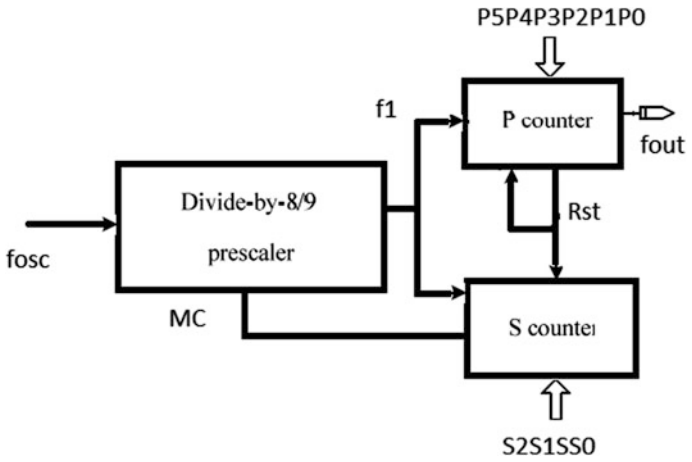

Fig. 5 Conventional frequency divider

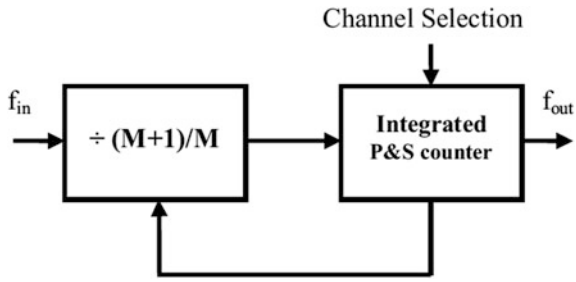

Fig. 6 Proposed frequency divider

For the prescaler in the divider, initially the control input is 0, so the division ratio of prescaler is $M + 1$. When the swallow counter counts up to S MC becomes 1, and prescaler division ratio switches to M. So $(P - S)$ number of cycles are to be counted by the P counter.

So the division ratio becomes (Fig. 5)

$$(M+1) \times S + (M) \times (P - S) = MS + S + MP - MS = MP + S$$

In the proposed design, the P & S counters are integrated together. This helps to reduce the circuitry (Fig. 6).

Different blocks in this design are: a dual modulus prescaler and an integrated P & S counter.

7.1 Dual Modulus Prescaler

The circuit is designed using D flip-flops. The MC input controls the division ratio of the prescaler. The circuit operation is as follows

- MC = 0; prescaler divides by 8
- MC = 1; Q_1 is reset by transistors $M1$, $M2$, $M3$ since Q_2, Q_3 = 1; so 111 is eliminated and division ratio becomes 7

True Phase Single Clocked D flip-flops are used to design the prescaler (Fig. 7).

7.2 Integrated P & S Counter

The Integrated P & S counter consists of a divide by 64 counter; XNOR gates ($X_0 - X_4$), AND gates (A_0, A_1), and a RS flip-flop. When the output of the P counter is equal to C value (which is the input reference frequency), output of AND gate goes high and RS flip-flop is set; so prescalar division ratio becomes 7. On the other hand if the output of the AND gate is high the flip flop resests and the division ratio is set as 8.

For example, the digital equivalent of input reference frequency is 00110. When the P counter value reaches predefined C $\{P_5P_4P_3P_2P_1P_0 = 1C_4C_3C_2C_1C_0$, RS flip-flop is set; so prescalar division ratio becomes 7.

Till P counter reaches 111111. The next value is 000000, so the flip-flop is reset and MC becomes divide by 8 (Fig. 8).

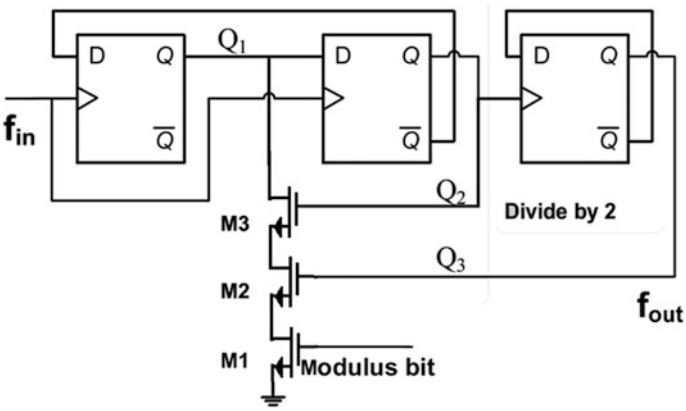

Fig. 7 8/7 dual modulus prescalar

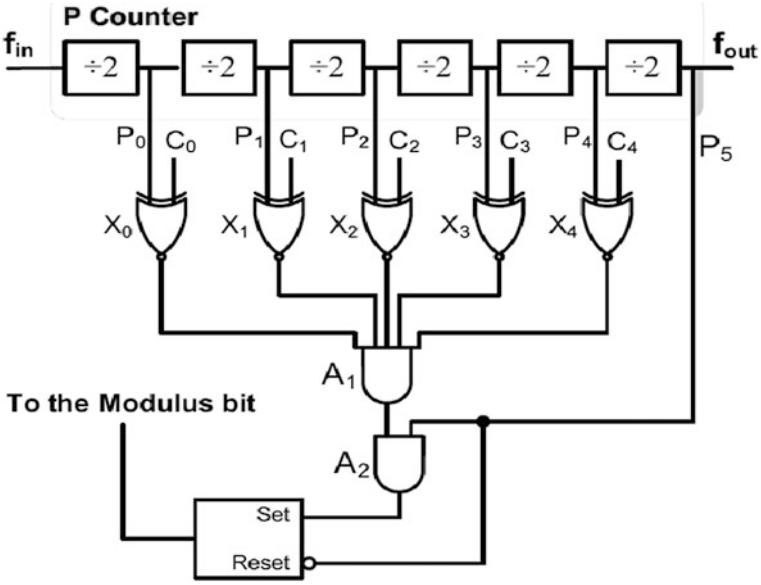

Fig. 8 Integrated *P* & *S* counter

8 Simulation Results

The proposed fractional frequency synthesizer (Fig. 1) was designed by using Advanced Design System, ADS tool. Simulation results for various blocks are given separately.

The first block is phase frequency detector (PFD). Depending on the input frequencies both reference and feedback frequencies, three different cases are there,

- Reference frequency is greater than feedback frequency
- Reference frequency is less than feedback frequency
- Reference frequency is equal to feedback frequency

Consider the case when reference frequency is greater than feedback frequency (Fig. 9).

The input frequencies (feedback and reference) are in GHz range, 1 and 2 GHz, respectively. Since the input reference frequency is higher the feedback frequency, UP signal is HIGH and DOWN signal is LOW. The output of PFD is feed to charge pump which favors the UP signal.

Consider the case when reference frequency is less than feedback frequency (Fig. 10).

The input frequencies (feedback and reference) are in GHz range, 2 and 1 GHz, respectively. Since the input reference frequency is lesser than feedback frequency,

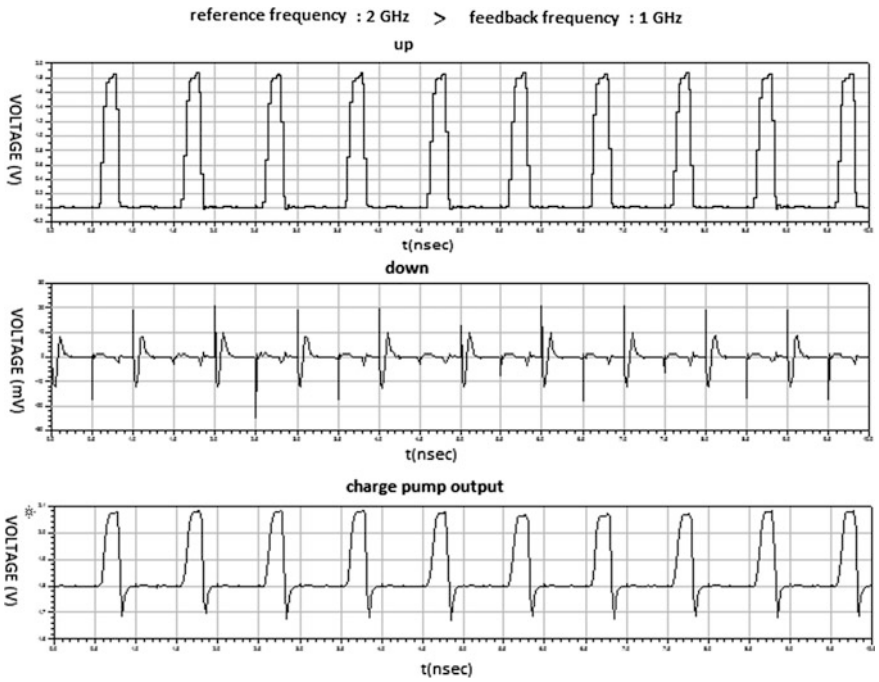

Fig. 9 Output of phase detector and charge pump when reference frequency is greater than feedback

UP signal is LOW and DOWN signal is HIGH. The output of PFD is feed to charge pump which favors the DOWN signal.

Consider the case when reference frequency is greater than feedback frequency (Fig. 11).

Since the input reference frequency is equal to feedback frequency, UP and DOWN signal is LOW. The output of PFD is feed to charge pump which is also LOW.

The output of programmable frequency divider is as follows:

- When modulus control is equal to zero the circuit acts as divide by 8, i.e., $f_{out} = f_{in}/8$. Here, the input frequency of the signal is 2 GHz (so Time period (0.5 ns) and amplitude is 1 V. So the f_{out} becomes 250 MHz (Fig. 12)
- When modulus control is equal to one the circuit acts as divide by 7, i.e., $f_{out} = f_{in}/7$. Here, the input frequency of the signal is 2 GHz (so Time period: 0.5 ns) and amplitude is 1 V. So the f_{out} becomes 312.5 MHz (Fig. 13)

A voltage controlled oscillator (VCO) can be realized using different topologies (Table 2).

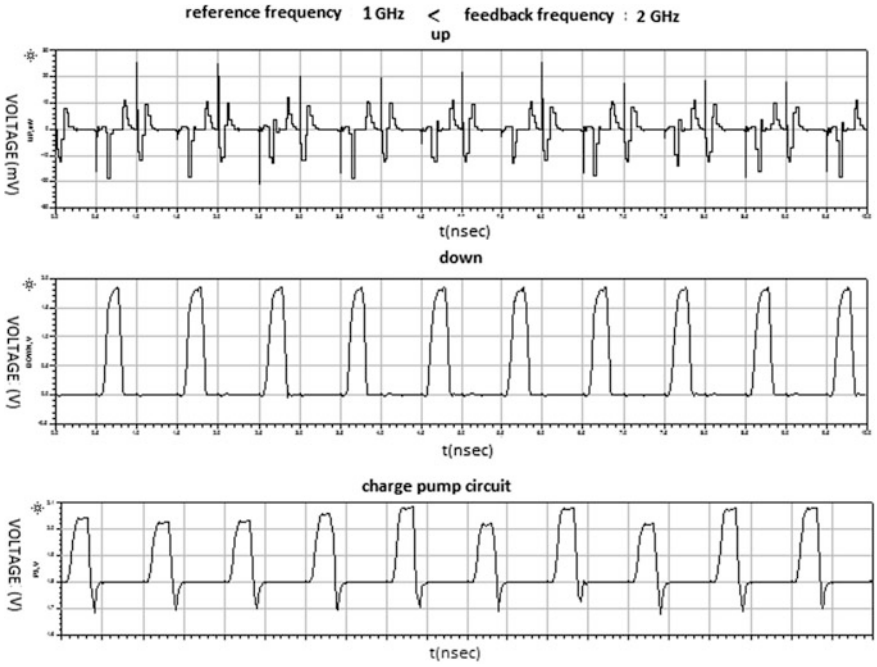

Fig. 10 Output of phase detector and charge pump when reference frequency is greater than feedback

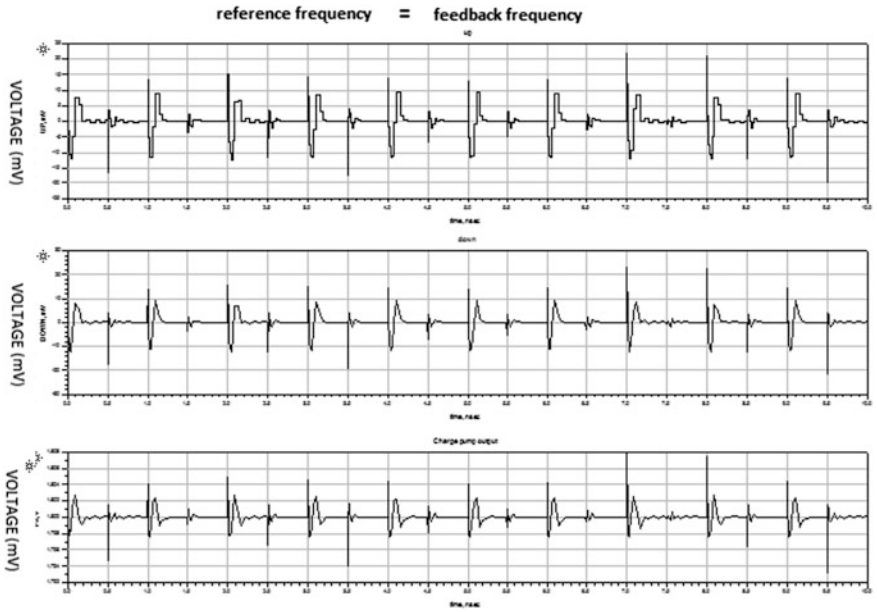

Fig. 11 Output of phase detector and charge pump when reference frequency is equal to feedback

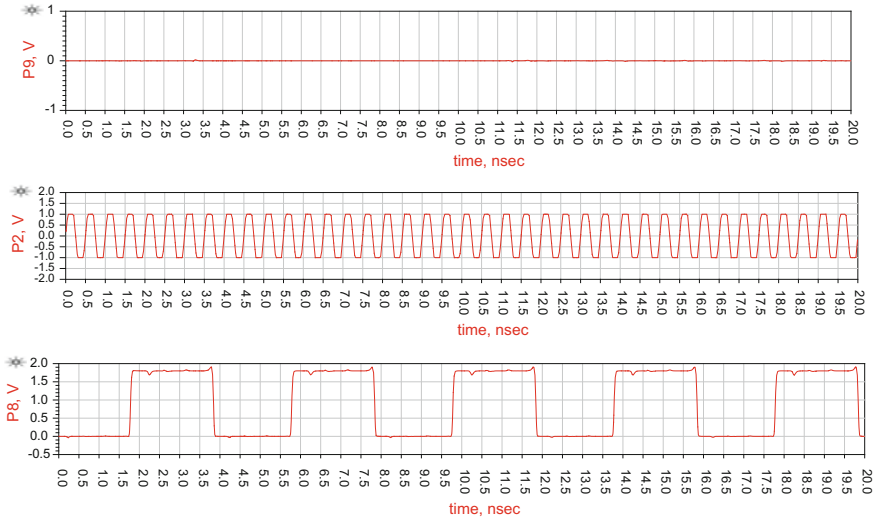

Fig. 12 Output when MC = 0

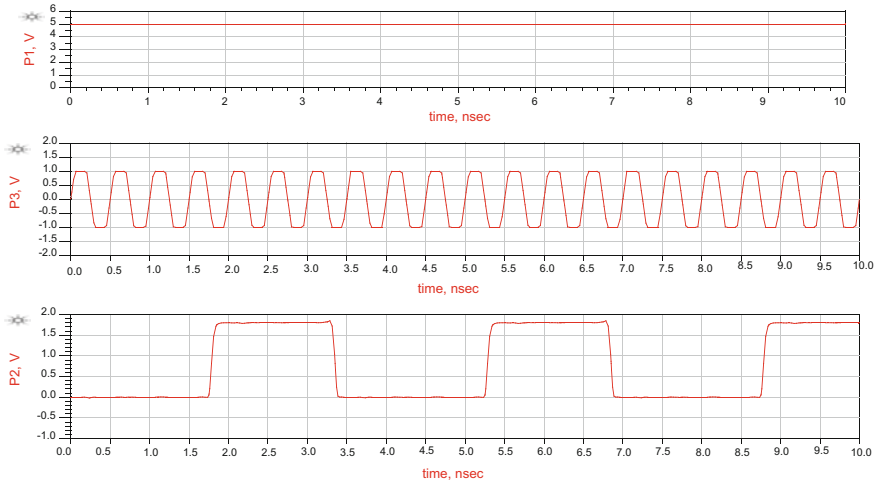

Fig. 13 Output when MC = 1

Table 2 Comparison of various VCO topologies

Specifications	Ring VCO	Source coupled VCO	LC oscillator
Technology	180 nm	180 nm	180 nm
Supply voltage	1.8 V	1.8 V	1.8 V
Frequency range	5.68 MHz to 1.25 GHz	33.33 MHz to 2.5 GHz	2.21–2.5 GHz

9 Conclusion

In this paper, a novel architecture for a fractional frequency synthesizer that operates in GHz range is proposed. The phase frequency detector is designed to have minimum blind zone since the input signal is constantly being modulated. Instead of using a ring oscillator, an LC oscillator is preferred because LC oscillators could operate at a higher frequency and provide a better phase noise performance than the ring oscillators. Most importantly, the frequency divider preferred is a programmable one instead of static high operating frequency, low noise, and a flexible and wide division factor range. Since the division ratio is programmable the PLL can generate noninteger division ratios unlike an integer PLL.

The circuit is designed using gpdk 180-nm library. This limits the operating frequency range of the frequency divider. The maximum frequency of operation was found out to be 5 GHz. Thus, such a system is unsuitable for higher frequency such as millimeter ranges.

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Memristor-Based Approximate Adders for Error Resilient Applications

S. Muthulakshmi, Chandra Sekhar Dash and S. R. S. Prabaharan

Abstract Image processing is a type of memory-access-intensive application that requires to access memory for a longer duration thereby lowering the overall throughput of the system by limiting the speed of memory access and bandwidth. This profound memory wall problem can be overcome by using memristor-based Computation-In-Memory (Memory-driven) architecture that can be simultaneously utilized as memory and processing element. To further enhance the computational speed and to perform energy/power-efficient operations, approximate computing is employed by allowing leverages in output for certain combination of inputs. In image processing applications, the computing blocks consist of multipliers and delays whose working is determined by suitable combination of adders. In this work, memristor-based approximate full adder is designed by random incorporation of errors in SUM and CARRY, respectively, and the resulting truth table is verified. The capability of proposed approximate adder is validated by designing (in Cadence Virtuoso) a 4-bit ripple carry adder (RCA) to perform bit-wise pixel addition of two grayscale images of same size and compared with an image obtained by exact addition method.

Keywords Memristors · Image processing · Adder · Inexact adder
Approximate computing

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1 Introduction

Approximate computing aims at reducing the overall power and energy consumption, by allowing leverages in output for certain combination of inputs. An error in output result is accepted until it is not upsetting the genuineness of the application. This is widely used in processing of audio and visual signals as they are error resilient due to lack of golden or precise results [1]. The random errors like minor loss in the quality of the image or missing a specific frame hardly upset the user satisfaction. This is achieved by lowering the number of components (transistors in case of CMOS, CNTFET, memristor, etc.), which thereby reduced the signal path from input to the output, thus lowering the overall delay of the circuit. The decrease in the number of components lowers die area and power dissipation [2–5]. Nano-ionic devices based on modest to fast ion conductor as active materials begin to occupy nano-electronic applications since 2008 when HP laboratories unveiled first practical memristor based on TiO_2 [6]. This has brought impetus to the practical implementation of fourth missing element called "Memristor" correlating charge (q) and flux (ϕ) based on the conceptual thought by Chua in 1971 [1]. Image processing is a class of memory-access-intensive application that uses memory for maximum duration thereby decreasing the overall throughput of the system by limiting the speed of memory access and bandwidth. This memory wall problem can be overcome by using memristor-based Computation-In-Memory architecture, where it can be utilized as memory and processing element at same time [7]. In image processing applications, the computing blocks predominantly comprised of multipliers and delays whose working is determined by suitable combination of adders. Though there are ample reports on memristor-based adders [8–11], we have proposed memristor-based approximate full adder and verified its performance in image processing application by adding two images of same size.

2 Background

2.1 Mathematical Modeling of Memristor

Memristor is an acronym of memory–resistor which was mathematically predicted by Leon Chua in 1971. Nevertheless, a physical example of bipolar switching of Pt-TiO_2-Pt memristor system has been successfully demonstrated by HP laboratories (USA) in 2008. The name Memristor (memory + resistor) was proposed by Leon Chua in 1971 and device was first developed by HP laboratories in 2008. It consists of one stoichiometric TiO_2 layer over which non-stoichiometric (TiO_{2-x}) is deposited, and it is sandwiched between top and bottom platinum electrodes [6]. This creates a non-equilibrium state which results in formation and rupture of conductive filaments on the application of electric field [6]. The above two phenomenon yields a nonlinear pinched hysteresis and thus able to switch the device

among the two stable resistance states, i.e., low-resistance state and high-resistance state which is considered as Logic "1" and Logic "0", respectively. Although many mathematical models are reported that elucidate the working of memristor, but lack of threshold parameters such as current/voltage has restrained them from explaining controlled switching mechanism and corroborated with experimental results obtained with memristors fabricated using various materials. In this context, recently Kvatinsky et al. reported ThrEshold Adaptive Memristor Model (TEAM) and Voltage ThrEshold Adaptive Memristor Model(VTEAM) which functions on the basis of current and voltage threshold, respectively [12, 13].

2.2 Approximate Computing

Approximate computing aims at reducing the overall power and energy consumption, by allowing leverages in output for certain combination of inputs. With the emergence of Internet of Things (IoT), there is a huge growth of digital data which demands fast access and high-density storage technologies. The applications like pattern recognition, signal processing, fuzzy, neuro and evolutionary computing are featured with an intrinsic error-resilience character, i.e., they process data from various types of sensors which are noisy and redundant in nature and produce results which are acceptable rather than exact result, i.e., they do not need to produce an accurate or golden numerical results [2].

Recent progress in the memory-driven computing prompted researchers to prefer approximate computing, which mainly focuses on reducing the number of circuit components and signal path from input to the output thereby reducing the overall delay. Memristive computing as memristor is simultaneously employed as memory and logic element which prompted us to design memristor-based approximate adder to further reduce the computational complexity for error resilient applications [7].

3 Results and Discussion

With the emergence of memory-driven computing and further ability of memristor being simultaneously used as logic and memory element, this provides a scope to go beyond traditional Von-Neumann architecture as both memory and logic units can be placed in the same block [14]. The presence of various resistance states aid in saving grayscale values of image, where the grayscale value can be "0" and "1" corresponds to HRS and LRS, respectively. Memristor-based crossbar memory array can be employed, in order to store image and as adder being the integral part of DSP blocks which can be placed within the memory array have prompted us to design and study memristor-based approximate adders which is discussed in detail in the subsequent section

3.1 1-Bit Full Adder

The sum of products expression for Sum and Carry for a single-bit all-memristor-based full adder is given as follows:

$$\text{SUM} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$\text{CARRY} = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

It is designed using 33 memristors, with an assumption that all the inputs are available as such. The schematic of 1-bit memristor-based conventional full adder is as shown in Fig. 1.

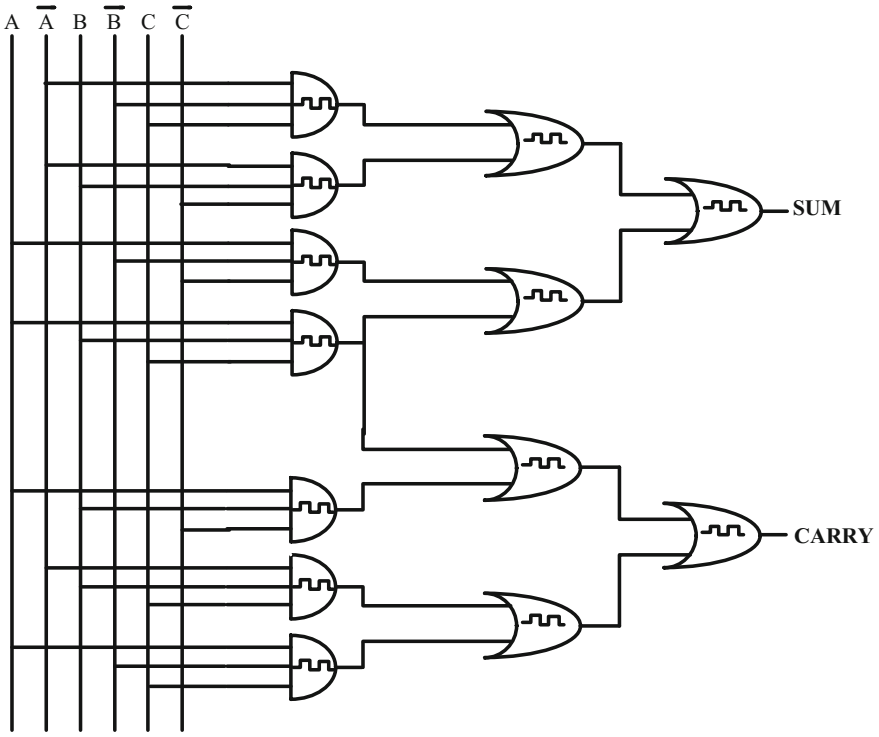

Fig. 1 Memristor-based 1-bit exact adder

3.2 1-Bit Approximate Adder

In order to enhance the computational speed and lower circuit complexity 1-bit approximate full adder is proposed by intentional introduction of errors in the Sum and Carry as shown in Table 1.

The Sum of Product (SoP) Boolean expressions for the proposed approximate full adder is given as follows:

$$\text{SUM} = \bar{A}C + BC + A\bar{B}\bar{C}$$

$$\text{CARRY} = \bar{A}C + AB$$

The schematic of proposed 1-bit approximate adder is shown in Fig. 2. It utilizes 14 memristors, where 66.7% decrease in the die area consumption and an improved delay performance is observed in comparison to approximate 1-bit conventional full adder as mentioned in Table 2.

3.3 4-Bit Ripple Carry Adder

The exact and proposed 1-bit Full Adder is used to design 4-bit Ripple Carry Adder as shown in Fig. 3. Note CMOS buffers and inverters are inserted at the required place where signal inversion or boosting is required. The error distance and error rate [14] is found to be 6, 6/8, respectively.

Table 1 Proposed truth table of approximate 1-bit full adder

			Actual		Approximate	
A	B	C	Sum	Carry	Sum	Carry
0	0	0	0	0	0	0
0	0	1	1	0	1	**1** ×
0	1	0	1	0	**0** ×	0
0	1	1	0	1	**1** ×	1
1	0	0	1	0	1	0
1	0	1	0	1	0	**0** ×
1	1	0	0	1	0	1
1	1	1	1	1	1	1

×—Errored Sum and Carry

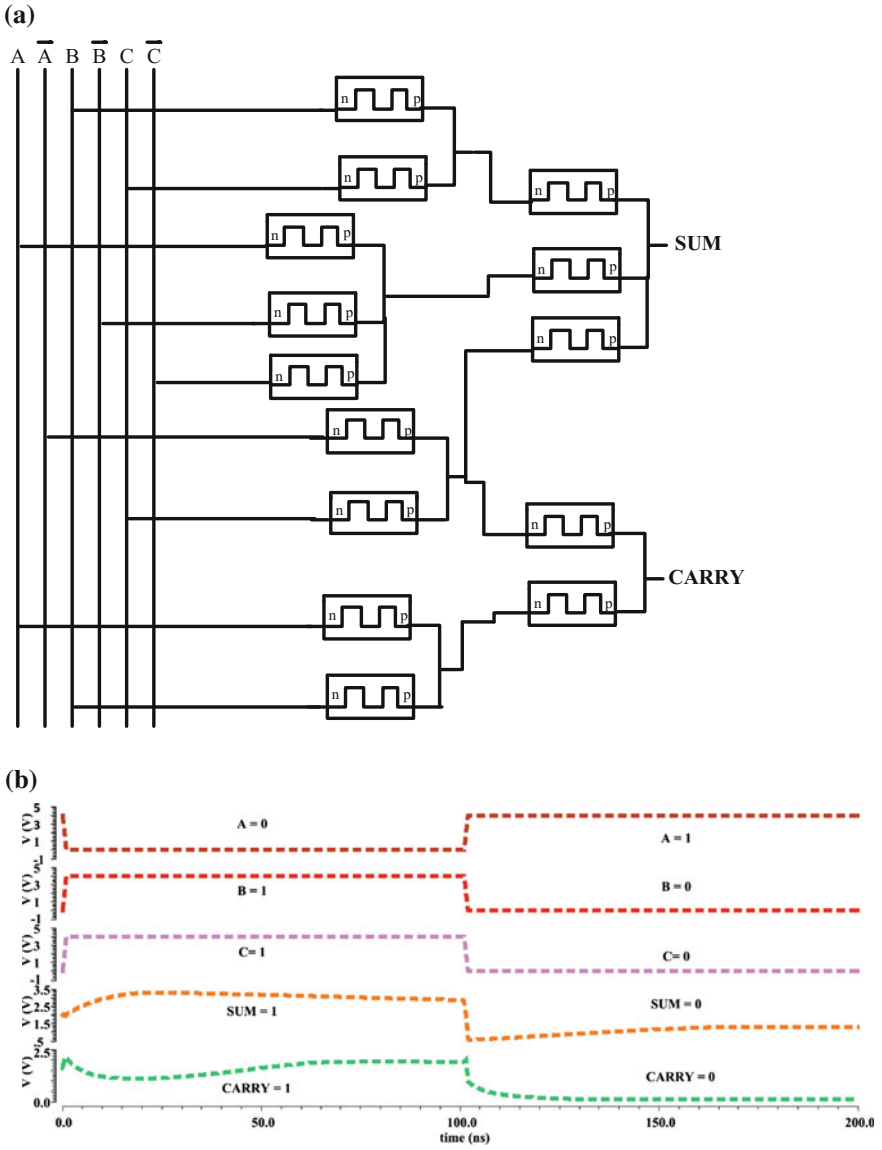

Fig. 2 **a** Schematic of proposed 1-bit approximate adder, **b** output waveform of proposed 1-bit approximate adder

Table 2 Parametric comparison of exact and approximate adder

Parameters	Values	
	Exact	Approximate
Delay (1-bit)	32.56 ns	0.802 ns
No. of memristors (1-bit)	33	14
No. of memristors (4-bit)	116	64
No. of CMOS transistors (4-bit)	18	6
Error distance	6	
Error rate	6/8	

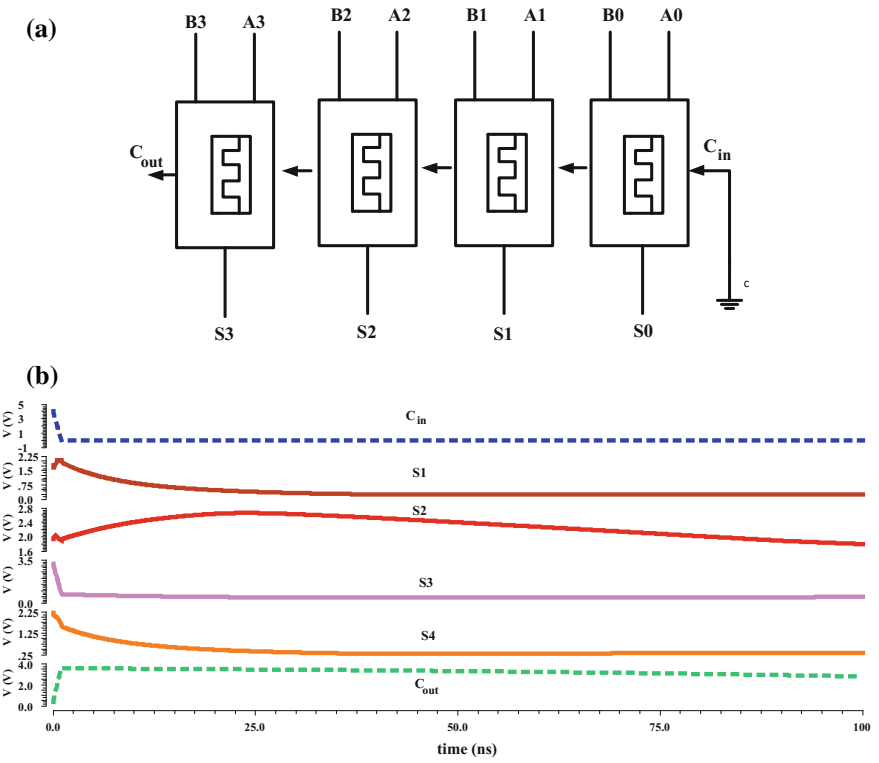

Fig. 3 **a** 4-bit ripple carry adder, **b** output waveform of proposed 4-bit approximate adder

3.4 Application in Image Processing

The proposed adder is further validated by adding two images of same size and performance metrics like mean square error and PSNR is deduced using MATLAB as mentioned in Table 3 [4, 15].

Table 3 Performance metrics of image comparison

Parameters	Value
Peak signal to noise ratio (PSNR)	121.68
Mean square error (MSE)	0.3373

Two images of Lena are added using exact and approximate logic and as shown in Fig. 4, the resultant image is recognizable when compared with the image obtained by exact addition.

Fig. 4 **a** Input image I, **b** input image II, **c** output image obtained upon exact addition, **d** resultant image obtained after approximate addition

4 Conclusion

This paper presented the success in design and working of a new 4-bit memristor-based approximate adder where an improvement in delay and die area consumption is observed due to reduction in number of components in comparison with the exact memristor-based adder. Furthermore, pixel addition of two identical images of same size is performed and performance metrics are deduced for the first time.

Acknowledgements Authors are indebted to the University management for their extending the simulation facilities to carry out this work.

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Integrated MEMS Capacitive Pressure Sensor with On-Chip CDC for a Wide Operating Temperature Range

Y. G. S. S. Sai Charan and Ananiah Durai Sundararajan

Abstract As the technology has grabbed a lot attention, the Micro-Electro-Mechanical Systems (MEMS)-based capacitive pressure sensors are the promising devices with good performance. These are capable of observing the temporal effects of the environment and to calibrate the values in order to provide information regarding the physical parameters by studying the deflection of the diaphragm structure. This paper presents a new model of capacitive pressure sensor along with a complementary metal–oxide–semiconductor (CMOS). The stress–strain characterization of poly-SiGe is used to develop and model the structure of the sensor's diaphragm element. The alternate edge supported octagonal-structured diaphragm held pentagonal-shaped clamps to yield good linearity, wide dynamic range, and better sensitivity. To improve the central deflection of the octagonal diaphragm, alternate opposite edges are fixed to divert the entire stress to the center of the diaphragm. The circuit presented over here uses a sigma–delta technique to convert the input capacitance into digital form. A constant-g_m biasing technique is used for high-temperature performance. The entire structure of the sensor is modeled in COMSOL Multiphysics, and the interface electronics are designed in Mentor Graphics using UMC 90 nm technology and achieves a better gain of 57-dB at the readout of the circuit. Simulation results show better sensitivity of 0.028 fF/hPa (for 1.8 V supply), and the nonlinearity is around 1% for the full scale applied pressure range from 0 Pa to 1500 hPa, the sensor is interfaced with the CMOS circuitry. The intelligent sensor is around 500 μm × 500 μm with the side of the octagonal diaphragm being 146.443 μm, respectively. Compared to commercial pressure sensor this device achieves wider low-pressure sensing range at minimum supply voltage.

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Keywords MEMS capacitive pressure sensors · CMOS interface electronics Capacitance to digital converter · Stress wide temperature

1 Introduction

The need of MEMS pressure sensors which works for wide operating temperature range finds its place in various fields like automobiles, industrial process control, oil and gas exploration, and for many space aeronautical applications at which the temperature of operation varies from standard military and industrial specification from −55 to +125 °C [1]. MEMS capacitive pressure sensors are widely used in many of the above-stated applications, as they were good at reliability, sensitivity, and accuracy, low-temperature coefficient and consume low power. These pressure sensors targets to provide better system performance, low cost, and portability when compared with conventional larger devices [2].

The implementation and the design of pressure sensors is done by the transduction of two well-known techniques called piezo-resistance and piezo-capacitance. The need of lesser number of fabrication mask steps along with environmental effects and insensitive to thermal variations has made the capacitive sensing technique a preferable one when compared with the other piezo-resistive type of sensing. In capacitive sensing technique, we come across some parasitic effects like curling boundary fields which degrades the performance of this type of sensing. Therefore, it needs interface electronics for better performance. The spatial dimensions of the pressure sensor were greatly reduced by the advent of CMOS SiGe MEMS technique [3]. The proposed design gives extended pressure sensing range at lower power supply.

Different sizes and shapes and structures of diaphragms for capacitive sensing have been explored to enhance the system performance. Even though the thickness of the diaphragm has been reduced and a trade-off lies between sensitivity and linearity. The design that we proposed in this paper has mainly centered to overcome this trade-off between sensitivity and linearity. The block diagram of the proposed integrated CMOS SiGe MEMS pressure sensor system is shown in Fig. 1. In order to reduce the electrostatic pull-in voltage, the diaphragm of the sensor is also perforated. The complete design target for the CMOS SiGe MEMS pentagonal edge clamped perforated octagonal diaphragm structure is to obtain wide temperature range with better linearity and sensitivity. To detect very low-pressure loads, pentagonal edge supports are clamped at alternate opposite edges of the octagonal diaphragm.

To increase signal-to-noise ratio and to decrease complexity in wiring, it is beneficial to place the interface electronics near to the sensor. Therefore, these sensor interface electronics should be able to work at the same temperature as that of the sensor. The design of sensor interface electronics is a challenging task at extreme hot and cold environments where the temperature ranges from −55 to

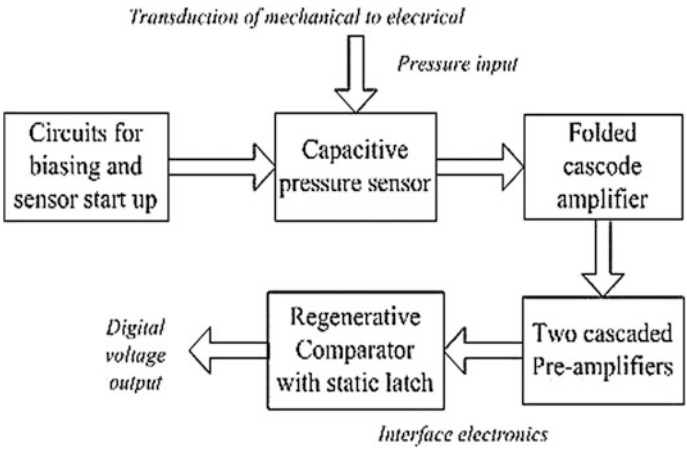

Fig. 1 Block diagram of proposed design for the capacitive pressure sensor and interface electronic circuits in CMOS poly-SiGe MEMS

+250 °C and this requires special design considerations and fabrication processing steps as well.

Complementary metal–oxide–semiconductor (CMOS) process which is widely used technology in the semiconductor manufacturing industry. This technology offers different advantages like ability to manufacture digital and analog circuits on same chip, low power consumption, and also ease of scaling down the technology. However, the electronic circuits that are manufactured with conventional bulk CMOS technology face many violations at high temperatures which includes drop in threshold voltages, decrease in mobility of holes/electrons, increase of leakage currents at the junctions. Among all these violations at high temperatures increased leakage currents at the junctions are predominant and are harmful. These currents cause loss of bias currents which reduces the circuit performance and more precisely the chip get failed due to latch-up. Therefore, most of these electronics circuits are required to work at high temperatures and use specialized process such as silicon carbide (SiC) or silicon-on-insulator (SOI) technologies which decrease these junction leakage currents. But the materials and the processing of these technologies are not maturely developed and are very expensive when compared with CMOS technology.

In this paper, we present the design of the system. The CMOS SiGe MEMS capacitive pressure sensor along with capacitance to digital converter (CDC) circuit is designed to work at high temperatures ranging from −55 to +250 °C The CDC circuit uses sigma–delta technique to convert the measured capacitance to digital format. The novelty of the work has low power consumption, higher level of integration and also provides digital output without any use of complex analog-to-digital converters (ADC's). In the organization of this paper, the implementation and the design of SiGe MEMS capacitive pressure sensor is discussed in

detailed in Sect. 2. Coming to the Sect. 3, we present the complete design of interface electronics. The simulation results are provided in detail in Sect. 4 and finally, the closing remarks are presented in Sect. 5.

2 Implementation and Design of the SiGe Pressure Sensor

The technique in our paper is a capacitive type of sensing, which is a simple method of low noise transduction mechanism that makes use of a change in mechanical displacement (parallel plate separation) to obtain a transduced electrical signal and also the desired physical quantity can be sensed. Under harsh environments, this type of method is less resilient when compared with piezo-resistive type of sensing. With better structural design, lower hysteresis and good stability can be achieved and are notable advantages for this capacitive type of sensing.

2.1 Fundamentals of Octagonal Diaphragm

The capacitive type of pressure sensor can be viewed as a parallel plate capacitor in which the octagonal-structured diaphragm acts a top plate to the sensor. To achieve the design target, a number of regular geometrically aligned planar perforations are made on the diaphragm which enhances the linearity of the sensor. In excess clamping, the alternate opposite edges of the diaphragm with the pentagonal supports provide reasonable low-pressure sensitivity. When load or vertical stress (pressure) is applied on the diaphragm, it causes bending of the diaphragm which results in change in displacement between the bottom plate (electrode) and the diaphragm and there by producing a change in capacitance. Neglecting the flux caused by the fringing electrostatic fields, the change in capacitance 'C' is given by [3]

$$C = A\frac{\varepsilon_0 \varepsilon_r}{d} \tag{1}$$

where the permittivity of the free space is defined by ε_0 which is 8.854×10^{-12} F/m. ε_r being the relative permittivity of the dielectric material used between the electrodes, the area of cross section of the diaphragm is given by A and d is the distance between the top and bottom plates (electrodes) of the capacitive sensor. Upon application of vertical pressure, the diaphragm gets deformed and as a result the stress and strain are distributed entirely over the diaphragm. The deflection of the diaphragm will be in non-uniform fashion due to the clamping of the diaphragm with pentagonal edge supports. Therefore, the displacement variation between the bottom electrodes and the diaphragm is not uniform over the cross-sectional area of the sensor. Thus, (1) must be deduced by using surface integral over the spatial distance (2-D) between the plates (electrodes) and this can be expressed as [3]

$$C = \iint \left[\frac{\varepsilon_0 \varepsilon_r}{\{d_0 - D(x,y)\}} \right] \mathrm{d}x\mathrm{d}y \tag{2}$$

where d_0 will be the distance between the electrodes when no pressure (zero) is applied and at a spatial location a (x, y) the incremental change in the separation after the deflection of the diaphragm is given by $D(x, y)$. The effective deflection of the top plate (d') for the octagonal diaphragm is obtained by

$$d' = \frac{1}{(A1 - 4A2)} \iint [D(x,y)] \mathrm{d}x\mathrm{d}y \tag{3}$$

where $A1$ is the area of the square which encompasses the total area of the octagonal diaphragm and all the four corresponding triangles as shown in Fig. 2. The area of one such triangle is given by $A2$. The effective deflection (d') of the octagonal diaphragm is observed in z-dimension, and it is obtained by the spatial integration of the deflection over the lateral surface area of the diaphragm. Kirchhoff's assumptions are to be used in the analysis of the stress because the thickness of the diaphragm is very small when compared with the rest of its dimensions. Moreover, the displacement of the diaphragm will be approximately half of its thickness and therefore, the stress analysis of the thin plates in two-dimensional (xy plane) is apt for this design. Thus, σ_z,τ_{xz}, and τ_{yz} being the stress tensor components will be zero and the stress tensor matrix will be reduced to

$$\sigma = \begin{matrix} \sigma_x \\ \sigma_y \\ \tau_{xy} \end{matrix} \tag{4}$$

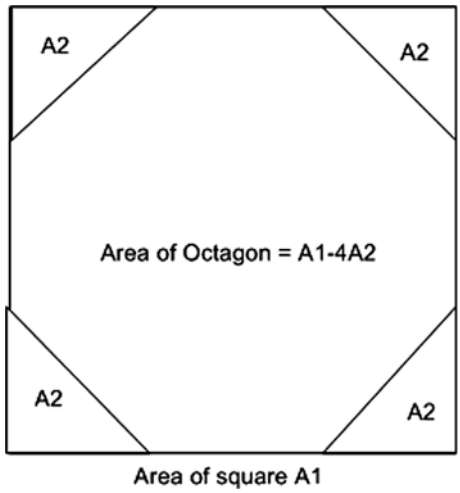

Fig. 2 Determining the area of octagon

Considering the material of the diaphragm is an isotropic, the behavior of the stress and strain is to be linear within its elastic limit range. Based on the Hooke's law of elasticity, the assumption of the stress–strain linearity till the elastic limit is governed by the equation

$$\sigma = \varepsilon E \tag{5}$$

where the action σ is the stress caused by the pressure applied on the plate (diaphragm) and the reaction results in the strain (ε). The modulus of elasticity is given by E. The octagonal structure can be taken from one of the regular polygonal structures with the number of sides and vertices is equal to eight each.

2.2 Structural Design of Octagonal SiGe Diaphragm

An octagonal-structured diaphragm which uses poly-SiGe material is clamped at the alternate edges to achieve curvilinear deformation of the diaphragm when low pressures are applied, the deflection of the octagonal diaphragm yields low dynamic range and poor sensitivity when all its edges are clamped. The pentagonal alternate edge clamp supports and also the planar perforations overcome the requirement for decreasing the thickness of the diaphragm structure and thereby the trade-off between linearity and sensitivity can be surpassed. The material used for the edge supports is silicon (Si) which is a semi-conductive material. Car must be taken while designing the bottom electrode to avoid possible short circuit and leakages. The perforations/release holes are of square shape with the dimensions 15 μm × 15 μm, and each perforation is separated by 20 μm pitch all over the structure of the diaphragm. As a result at high-pressure range, the diaphragm performs comparatively lesser deflection. COMSOL Multiphysics shows that the displacement is of 2.3 μm when the pressure applied is 1500 hPa, which is almost half the thickness of the diaphragm (≈5 μm) the narrow 5 μm separation between the diaphragm and the bottom electrode restricts the sensor's dynamic range. Further, the assumption of the analysis of thin plates does not satisfy for larger dimensions (which exceeds 2.5 μm in this case). Generally, when the deflection of the diaphragm exceeds half of its thickness, due to electrostatic pull-in short circuit and leakage effects come into action. The dynamic range and the linearity of the proposed poly-SiGe MEMS sensor can be improved upon by using a perforated octagonal diaphragm which is capable of reducing the occurrence of early pull-in that was caused by the reduction of surface area of the capacitance. Using COMSOL Multiphysics, finite element analysis (FEA) is performed and reveals that the deflection of the diaphragm up to 2.5 μm does not degrade the performance of the sensor. To obtain better sensitivity, thinner diaphragms which provide larger deflections are preferred but this results in the negatives consequence with the linearity. Therefore, more priority was given to the characterization of side length of the octagonal diaphragm to be a regular structure. The Young's modulus (modulus of elasticity E) of poly-SiGe material is

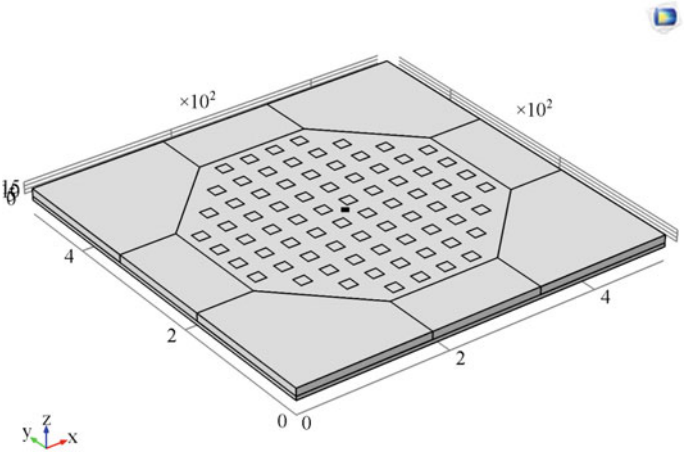

Fig. 3 Geometrical structure of SiGe MEMS of capacitive pressure sensor

very low of 130×10^9 Pa and this provides better deflection when low pressures around 100 Pa are applied. By this low minimum detectable pressure and wide dynamic range can be achieved by using this poly-SiGe diaphragm (Fig. 3).

3 Design of Interface Electronics

The on-chip sensor interface electronic circuit should convert the weak noisy signal which comes as a transduced output of the capacitance pressure sensor. This weak signal is to be amplified into an useful electronic signal for further processing of information. The weak output signal from the sensor may get more degraded due to resistances and capacitances of the transmission lines which connect the MEMS diaphragm and the CMOS metal wires in the chip. Thus, the design of signal readout circuit is a challenging one and the entire performance depends on implementation of this sensor module. The CMOS circuit presented over here aims at some of the performance parameters like high gain, high linearity, low power consumption, and wide temperature range of operation [4]. The change in capacitance due to the pressure applied on the diaphragm is converted into an electrical signal through a folded cascode amplifier as shown in Fig. 4.

3.1 CMOS Interface Circuit Design and Architecture

The schematic diagram of CMOS interface electronic circuit which works over wide temperature range for capacitive MEMS pressure sensor is shown in Fig. 4.

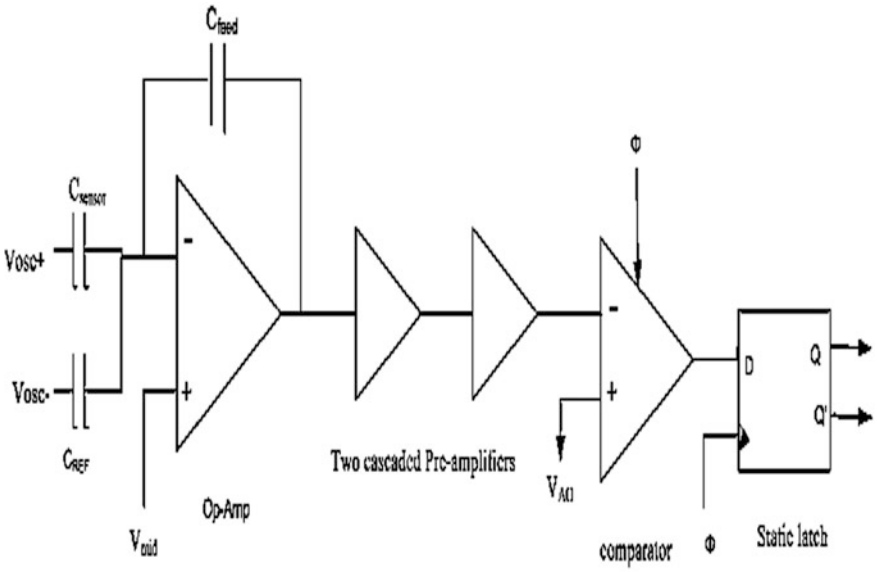

Fig. 4 Schematic diagram of CMOS interface electronic circuit

The architecture of this interface electronic circuit is similar to regular sigma–delta analog-to-digital converter (ADC) except there is no digital-to-analog converter (DAC) and separate reference and input voltages in it. A switched capacitor technique is used in the circuit along with a novel differential input circuit that works with MEMS capacitive pressure sensor having a wide range of capacitance varying from 0.1 to 5 pF under steady-state condition. This circuit determines the capacitance of external pressure sensor C_{sensor}, and an analog voltage output V_{out} is produced. C_{ref}, being the reference capacitor is required which has similar steady-state capacitance values as that of the pressure sensor device to extend the dynamic range of detection.

The reference capacitor C_{ref} and the sensor capacitor C_{sensor} are driven using two —kHz square wave signals $V_{\text{osc+}}$ and $V_{\text{osc–}}$ with opposite in phase and same amplitude ΔV_{osc}. ADC voltage V_{mid} is applied at non-inverting terminal of the amplifier. C_{feed} is the feedback capacitor of 1 pF which is used in the design. The input and output waveforms are shown in Fig. 4. The output voltage with the amplitude is given by

$$V_{\text{out}} = \frac{(C_{\text{sensor}} - C_{\text{ref}})}{C_{\text{feed}}} \times \Delta V_{\text{osc}} + V_{\text{mid}} \tag{6}$$

The overall performance especially the decrease of bandwidth and the loss of open loop gain of the operational amplifiers degrades drastically when they are

implemented in CMOS process at high temperatures. To reduce the excessive leakage current and to compensate high-temperature effects, an effective circuit design techniques are required. Among various high-temperature compensation techniques, at wide temperature range, constant-g_m bias technique is preferred and has been proven to be effective. The biasing circuit which uses constant-gm biasing technique is shown in Fig. 5.

Based on the type of application, the capacitance values of C_{ref} and C_{sensor} are to be chosen. In the applications like matching CMOS capacitors are used for DAC and ADC, both C_{ref} and C_{sensor} are chosen to be constant, whereas in the cases like capacitive pressure sensors and accelerometers, the capacitances C_{ref} and C_{sensor} may be time varying. In this typical capacitive MEMS pressure sensor read out circuit, the reference capacitance is C_{ref} while C_{sensor} is a variable capacitor which is to be measured.

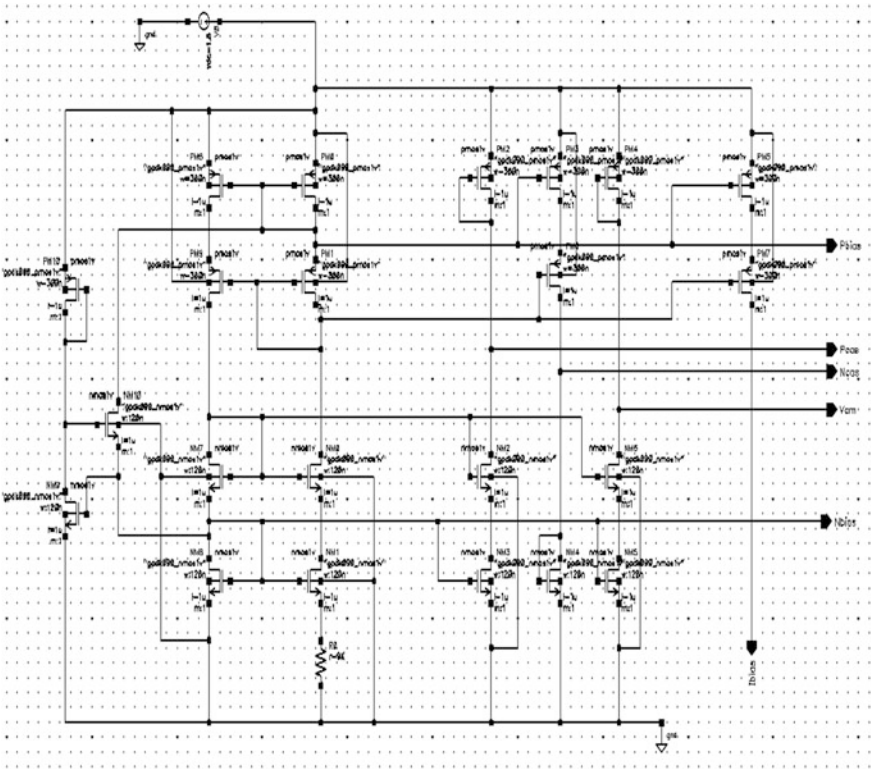

Fig. 5 Schematic of constant-g_m biasing circuit

3.2 Detailed Design of CMOS Signal Conditioning Circuits

3.2.1 Constant-g_m Biasing Circuit

The biasing circuit which uses constant-g_m biasing technique is shown in Fig. 5. The constant-g_m biasing technique works on the principle of providing a copy of current to bias the MOS transistor, the current being inversely proportional to carrier mobility. The critical parameter g_m (transconductance) effects the stability, gain, and bandwidth of the operational amplifier. In the saturation region of a MOS transistor, neglecting the back gate effect and the channel length modulation the transconductance g_m is governed by the equation [5]

$$g_m = \sqrt{2I_D\mu_n C_{ox}\frac{W}{L}} \tag{7}$$

where L and W are the channel length and channel width of the MOS transistor, the oxide capacitance per unit area is given by C_{ox}, μ being the carrier mobility and I_D is the drain current at the drain terminal of the MOS transistor. From (7), it is clear that when the carrier mobility is decreased g_m also gets decreased and this happens when the temperature is increased. From Fig. 5—the bias current I_b which flows through biasing resistor R_b when the body effect and the channel length modulation are neglected is expressed as

$$I_b = \frac{2}{R_b^2\mu_n C_{ox}}\left[\sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}}\right]^2 \tag{8}$$

where the transistor is biased by the biasing current I_b by substituting Eq. (8) in Eq. (7) the g_m of the transistor can be expressed as

$$g_m = \frac{2}{R_b}\left[\sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}}\right]\sqrt{\frac{W}{L}} \tag{9}$$

From the above equation, we can clearly justify that the g_m of the transistor is inversely proportional to R_b. Under ideal conditions, the g_m of the transistor will be constant for the temperature variations, only when the temperature coefficient of biasing resistor R_b is zero. Further, the temperature stability can be improved by using both negative and positive temperature coefficient resistors that are to be connected in series such that the equivalent resistor is achieved with near zero temperature coefficient.

3.2.2 Folded Cascode Amplifier

At high temperatures, the gain of the amplifier falls due to decrease in g_m. So to maintain sufficient gain, a high gain amplifier is necessary. Figure 6 shows a folded cascode amplifier with single-ended output is used as an operational amplifier. Constant-g_m biasing circuit generates the necessary bias voltages for the folded cascode amplifier. With reasonable aspect ratios of the device, larger gain can be achieved with NMOS as input pair to the amplifier. The folded cascode amplifier provides better performance stability with lower voltage head room requirement when compared with telescopic amplifier [6].

3.2.3 Comparator

A regenerative comparator with static latch is used in the implementation of comparator. To obtain high precision, the voltage difference at the input is applied to larger extent by placing two cascoded preamplifiers prior to the regenerative comparator [7]. Here also constant-g_m biasing circuit provides the necessary bias

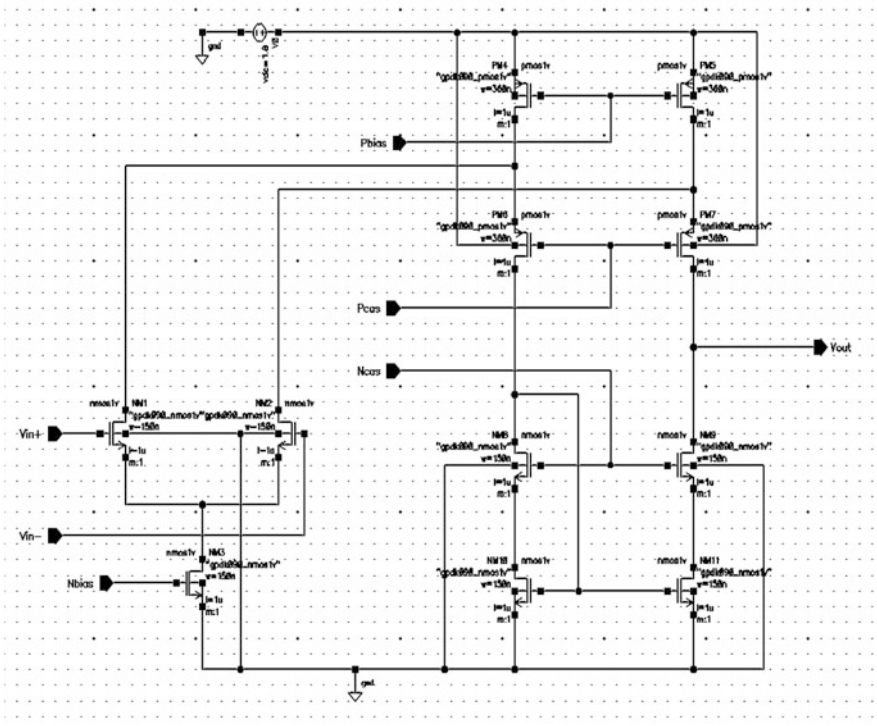

Fig. 6 Schematic of folded cascode amplifier

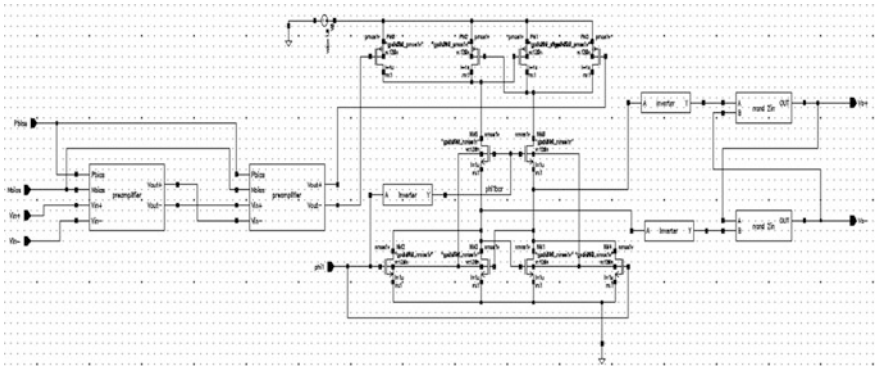

Fig. 7 Schematic of regenerative comparator with static latch and two preamplifiers

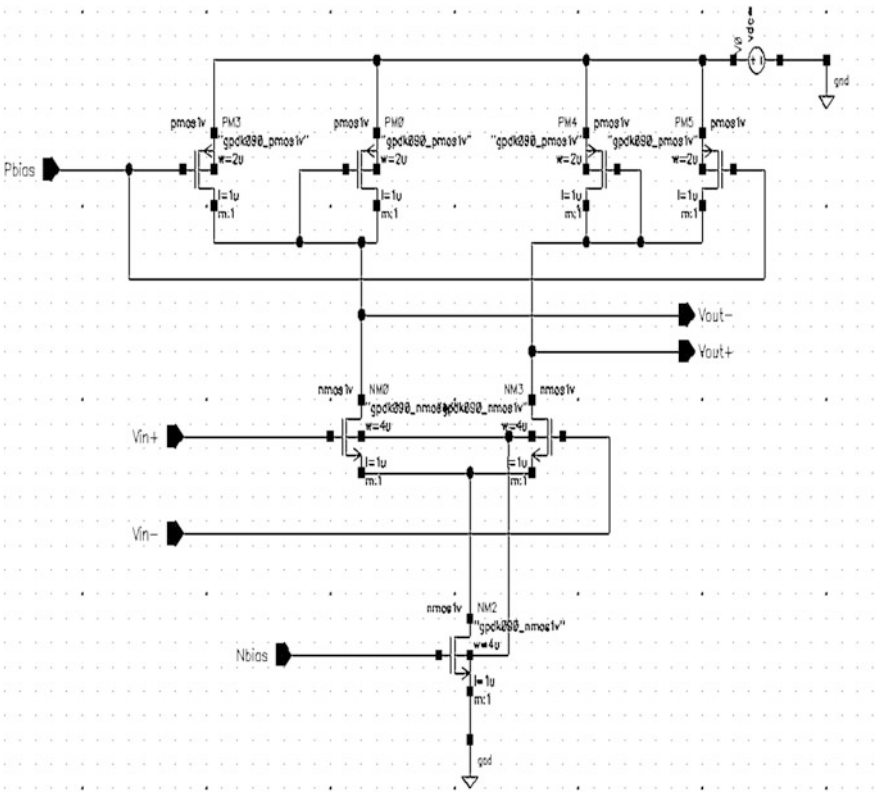

Fig. 8 Schematic of preamplifier

voltages to the preamplifiers for maintaining its bandwidth and gain over a wide range of temperature. The schematic of this clocked comparator is shown in Fig. 7. And the schematic of preamplifier is shown in Fig. 8. At high temperature, the offset voltage and noise of the comparator are increased. As the comparator is situated after the integrator, its offset and noise are modulated in the same way as that of the quantization noise. To some extent, these can be reduced by the large DC gain of the integrator. Thus, the performance of the circuit is in sensitive to offset and noise of the comparator.

4 Simulation Results and Discussions

4.1 Sensor Simulation Techniques

For optimizing the dimensions of the octagonal diaphragm, finite element analysis (FEA) is performed using finite element software COMSOL Multiphysics. In this computer-aided design (CAD) tool, it consists of Structural Mechanics, a physics module in which the Electro-Mechanics Multiphysics module is used for the entire design of the MEMS capacitive pressure sensor. Electro-Mechanics module is a combination of both Electrostatics and Solid Mechanics modules.

The side length of the octagonal diaphragm is targeted to achieve optimal deflection of the diaphragm by optimizing its dimensions. The dynamic range of the sensor is limited by two cases, firstly to obtain linear capacitance change with applied vertical pressure and secondly to increase the central deflection of the diaphragm for wide dynamic range without the plates getting shorted (causing touch down). To perform thin plate analysis, the dimensions of octagonal diaphragm are optimized to obtain maximum displacement of 2.3 μm (for a fixed 5 μm thickness of the diaphragm as per the specifications of SiGe process. In CAD tools, perforated geometries are not predefined and there is no such model for creating the geometry in the available 3-D work plane. Hence in 2-D work plane, octagonal geometry is defined with the optimized dimensions. A single small 2-D square block having dimensions 15 μm × 15 μm is drawn and from this an array of such block have been arranged symmetrically throughout the octagonal diaphragm with pitch size of 20 μm. Boolean difference operation is invoked to remove the array of squares from the solid octagonal 2-D structure. Thus, octagonal perforated diaphragm is created in 2-D and was extruded to convert 2-D model into 3-D model. Material properties are applied to the entire sensor with poly-SiGe being the material diaphragm, and the rest of the geometry is of silicon. Moreover, boundary conditions are specified and free tetrahedral with normal and fine meshes are applied for FEA analysis. The meshing of the sensor is shown in Fig. 9 with fine meshing to the diaphragm and normal meshing to the rest of the sensor. To characterize the sensor, linear elastic material is used. Stationary analysis is used to study capacitance and displacement of the diaphragm for the pressure applied and

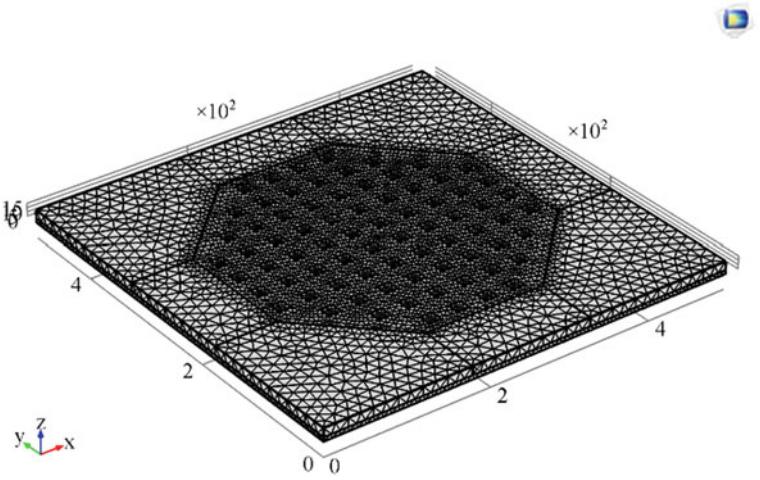

Fig. 9 Free tetrahedral meshing of the capacitive pressure sensor

the temperature operated. The optimized side length of the diaphragm was 146.443 µm. Parametric sweep analysis is performed for the applied vertical pressure from 0 to 1500 hPa in steps of 50 hPa. This resulted in the displacement varying from 0.0236 to 2.32 µm and the change in capacitance produced by the deflection of the diaphragm is from 0.18 pF to 0.222 fF when there is no thermal stress. From the above simulated results, the sensitivity of the sensor is obtained around 0.028 fF/hPa and the nonlinearity is around 1.1%.

Under thermal stress condition, when the coefficient of thermal expansion of the material is taken into consideration, the displacement changes from 0.0236 to 1.85 µm and the capacitance produced was found to be varying from 0.18 to 0.211 pF for the same range of applied pressure. In this situation, the sensitivity was found to be 0.0216 fF/hPa and the nonlinearity is 0.9%. The deflection analysis of perforated poly-SiGe octagonal diaphragm from the simulations of COMSOL is shown in Figs. 10, 11, 12, 13, 14 and 15 with the characteristics of change in capacitance and displacement of the diaphragm versus applied pressure is platted. The results obtained depict the performance enhancement in terms of minimum detectable stress (pressure), elastic limit of the diaphragm and dynamic range.

The above 3-D plot states the distribution profile of the electric potential in the free space of the sensor (here the free space is filled with air). The electric field tends to decrease as we move away from the diaphragm and at the perforations.

From the above 2-D plot of Fig. 13, it shows two different kinds of displacement of the diaphragm for the applied load stress. One is the central deflection and the other is overall average deflection of the diaphragm under both no thermal stress and with thermal stress conditions.

The plot in Fig. 15 gives the amount of capacitance obtained due to the deflection of the diaphragm for applied pressure of 500 hPa over a wide range of

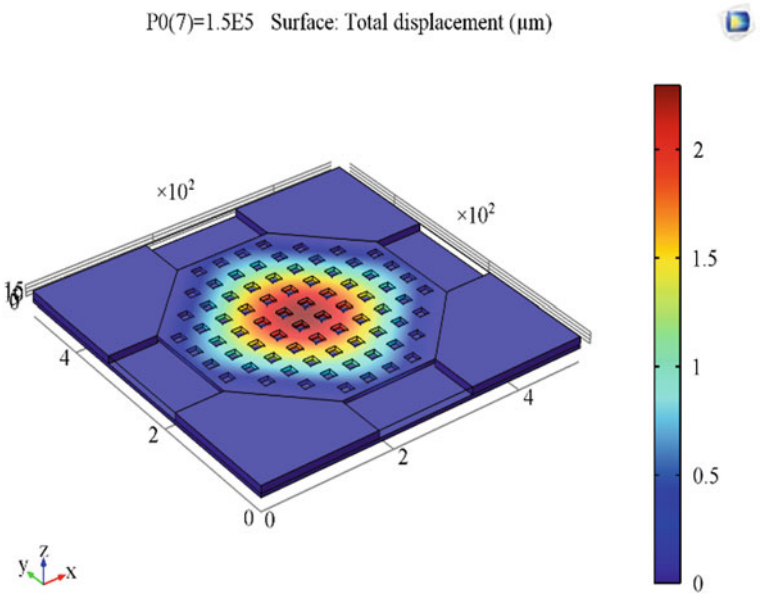

Fig. 10 3-D plot of displacement versus pressure under no thermal stress

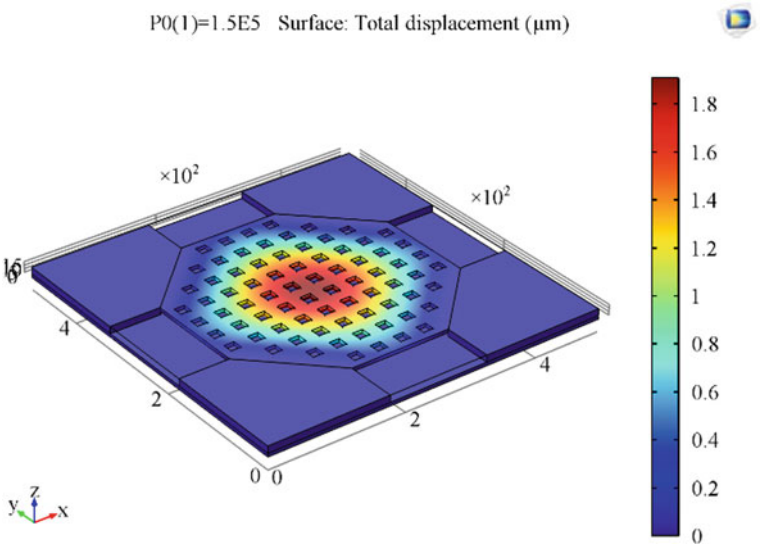

Fig. 11 3-D plot of displacement versus pressure under thermal stress

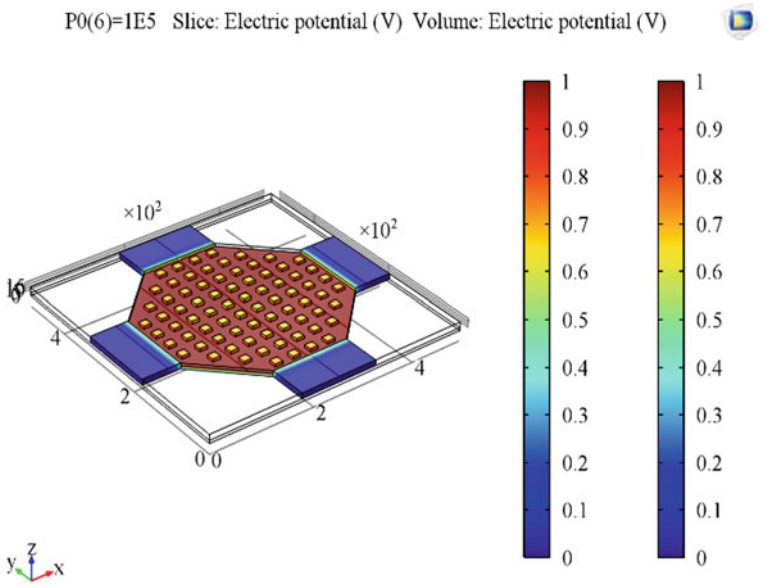

Fig. 12 3-D plot of volume electric potential profile

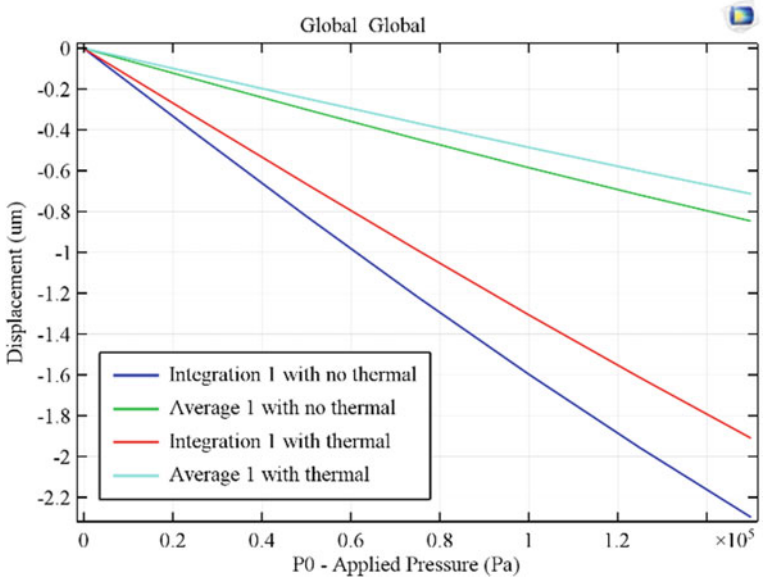

Fig. 13 Diaphragm displacement versus pressure

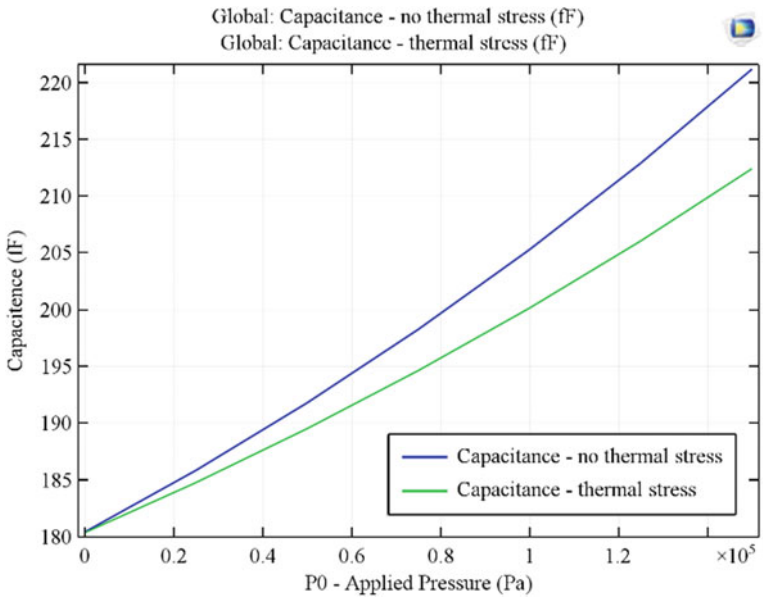

Fig. 14 Applied pressure versus capacitance plot under thermal stress and no thermal stress conditions

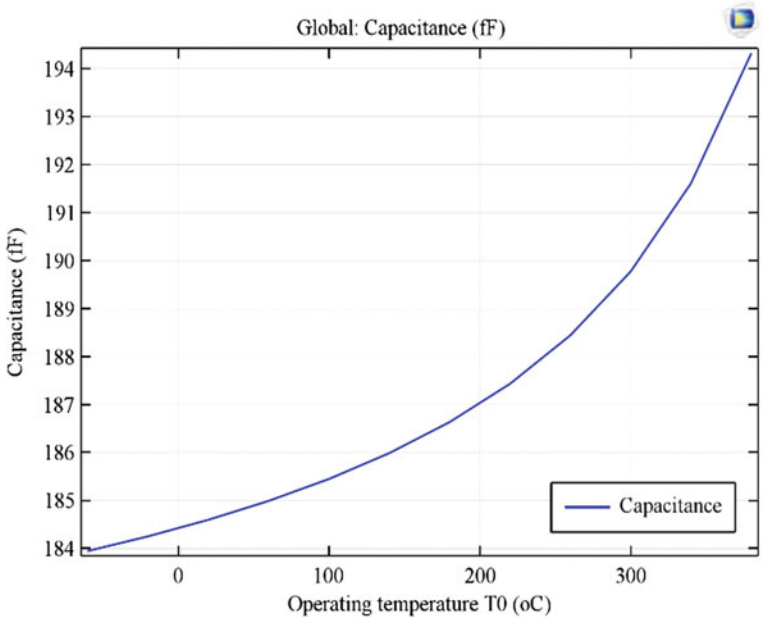

Fig. 15 Operating temperature versus capacitance plot

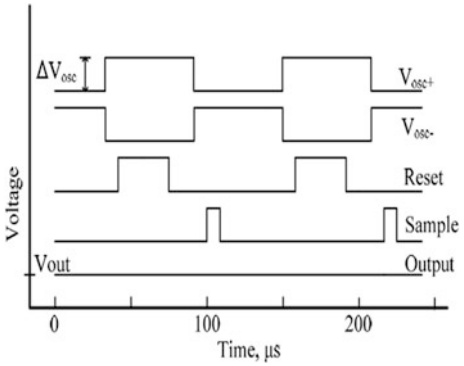

Fig. 16 Competitor's output waveform

temperature varying from 60 to 400 K. As the temperature raises, the capacitance also increases due the phenomena of thermal expansions of the materials which is also taken into consideration.

4.2 Circuit Simulation Techniques

The analysis and design of CMOS interface electronic circuit are performed using Mentor Graphics UMC 90 nm Technology and Cadence gpdk 90 nm. The simulation results of the circuit designed is shown in Fig. 16.

5 Conclusion

In the summary we have presented a structural model and analysis of a SiGe MEMS capacitive pressure sensor with a CMOS capacitance to digital converter circuit for a wide operating range of −55 to +250 °C is designed using COMSOL Multiphysics and UMC 90 nm CMOS technology with 1.8 V power supply. The capacitive MEMS pressure sensor is measured and simulated under different pressure loads varying from 0 to 1500 hPa. This new model octagonal diaphragm clamped to pentagonal supports at alternate edges of the diaphragm exhibits good linear operation over a wide dynamic range. Pentagonal edge supports increased the sensitivity and without degrading the linearity. A high-gain signal conditioning circuit for low supply voltage and weak sensor signal is designed. Nonlinearity is around 0.5% which is obtained for full-scale pressure range. Constant-g_m biasing technique is used to mitigate performance degradation. Simulation results show better temperature stability from −55 to 250 °C. The novelty is that it has high level of integration, reduced sensitivity to non-ideal effects, and it gives digital output without any use of complex analog-to-digital

converters. The interface electronic circuit performance can be increased by a fully differential architecture. This integrated MEMS capacitive pressure sensor with overall sensitivity of 0.028 fF/hPa for supply voltage of 1.8 V that can be used for various applications such as biomedical applications, intraocular measurement of pressure, and industrial process control.

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A High SNDR and Wider Signal Bandwidth CT ΣΔ Modulator with a Single Loop Nonlinear Feedback Compensation

Simhadri Chandra Sekhar and Ananiah Durai Sundararajan

Abstract A continuous time Gm-C-based ΣΔ modulator has some advantages over active RC-based ΣΔ modulator. The drawback of RC filter is the phase lag due to the pole of RC elements that affect the modulator loop stability. The compensated Gm-C filter provides better stability and less complexity. Moreover, the high input impedance of Gm-C employed in modulator eliminates the strong linear driving stage, because it uses NMOS as Gm1 input stage. A single loop, third-order Gm-C ΣΔ modulator with 4-bit quantizer avoids the high output power drives due to the lower load. Multi-bit operation basically suffers from digital–to-analog data converter nonlinearity. The incremental element matching is also ineffective at low oversampling. Hence, increasing the sampling frequency f_s will maximize bandwidth and provide high resolution to the modulator. The modulator constructed using cascaded Gm amplifiers have low linear range, which means the larger nonlinear range leads to low SNDR.

Keywords CT · DT · ΣΔM · DAC · NTF

1 Introduction

A configuration of the linearized trans-conductor for low voltage and the high-frequency application has been constructed. The continuous time (CT) modulators are playing a wider role to the discrete time (DT) against the robust to defects in sampling and speed requirements of operation [1–10]. Some factors are affecting the sigma–delta modulator (ΣΔM) performance, one of which is nonlinearity due to the transconductance mismatch of the driver stage.

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Nonlinearity cancelation is achieved by using a double pseudo-differential pair with degenerative transistors, which are in the linear region. A small change in the transconductance produces high linearity and speed but results in 30% extra power consumption. Therefore, tune the transconductance. Most of the circuitry of ΔΣM have been built with discrete-time (DT) switched-capacitor circuits. If settling time requirement is present in the DT circuits, then the clocked restriction exists, which reduces the speed of modulator. These restrictions are normalized by using CT circuitry instead of DT circuitry. The DT ΔΣM already has resolution and power advantages; here it is shown that CT ΔΣM could hold these advantages while operating at higher speeds. As per the literature, it has been stated that the CT circuitry is gaining more attention by the use of high-resolution ADC for higher speed requirements.

The Gm-C-based CT ΣΔM with Gm-C filter has improved linearity, stability, and reduced power consumption. Almost all RC-based CT ΣΔ modulators are designed with RC filter for a wider range of bandwidths [2, 4–6]. On the other hand, Gm-C filters have advantages over the RC filters. Firstly, due to high resistive loads in active RC-based ΣΔM, it must have more input signal currents than feedback path through DAC1, which is subtracted from the input signal of the loop filter. Therefore, the 20% of total power consumed by the modulator is used to input signal current to drive the modulator. For this requirement, the driving stage must consume nearly half of the power in the overall modulator for high-performance designs. Secondly, due to the virtual ground, the input node of the op-amp is carrying a high-frequency current pulse. So, the high-quality virtual ground will carry a high frequency of the current pulse. Therefore, the op-amp must meet the requirements of higher gain and wider bandwidth.

A Gm-C-based ΣΔM has a high input impedance which is capable of avoiding the high linear driving stage depicted in Fig. 1. The output of DAC1 is a high-frequency current pulse which flows through a load capacitor (C_1) to produce the required input signal for the transconductance amplifier (G_{m2}). The G_{m1} is outside the loop consists of DAC1, a loop filter, and quantizer, which is handling only narrow signal band. Therefore, the phase lagging of G_{m1} will not affect the modulator delay and stability. The loop filter formed by G_{m2}, G_{m3}, $G_{m\mathrm{F}}$ and $G_{m\mathrm{R}}$ should meet the high gain requirements at very low frequencies and must act as a low dynamic gain at higher frequencies for required bandwidth. Here $G_{m\mathrm{F}}$ and $G_{m\mathrm{R}}$ are feed forward and feed reverse transconductance amplifiers, respectively. Therefore, the loop filter must respond to the in-band signal (low frequencies) and eliminate the out-band signal frequencies due to the transfer function (TF) limitation. The TF has a finite gain equal to $K * I_{\mathrm{error}}(s)$. Here K is the loop filter gain and $I_{\mathrm{error}}(s)$ is the error current across the load capacitor C_1. The quantizer is constructed using the comparators with flash type analog-to-digital converter (ADC). The output of the quantizer is a bit stream, it is applied to the D-positive triggered flip-flop bank to provide the half delay from clock to output $Q(T_{\mathrm{clk}\text{-}Q})$, of the D flip-flop. This delayed bit stream is converted into high-frequency current pulses using DAC1. The remaining half delayed bit stream is fed back to quantizer input as a feedback [1].

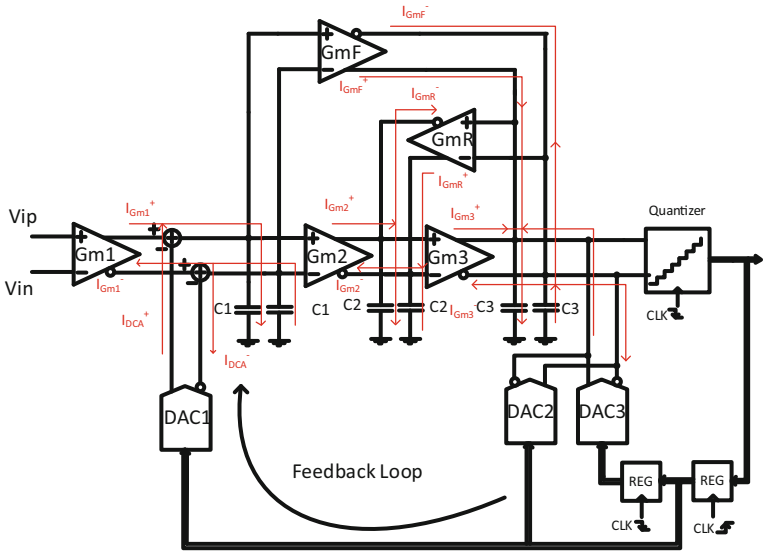


Fig. 1 A system architecture of third-order CT ΔΣ modulator designed with Gm-C filters. The current paths are mentioned in red color

2 Modulator Architecture

The ΣΔM consists of a digital low pass filter, one or more comparators, integrators and summing circuits, a DAC. The ΣΔM has an advantage on oversampling to reduce the quantization noise created by the quantizer which constructs by comparators. The oversampling method does not only reduce the noise but also the noise shaping and increase the signal band. A perfect sampling design with n-bits has a quantization noise of $q/\sqrt{12}$, where q is the voltage value of the least significant bit (LSB). The noise shaping is improved by increasing the order of modulator. The main drawback of RC-based ΣΔM is the sampling frequency limitation (f_s) by the op-amp. This restriction is not valid to Gm-C-based ΣΔMs. So that even higher rate of sampling also can achieve in ΣΔM. Here a high oversampling of 650 MHz is used for design and noise reduction. The noise shaping is achieving by the increase the order of loop filter, but it can create the instability problems in modulators. As result, the high-order designs are not stable systems. Therefore, 2-stage loop filter provides the stability to the modulator.

3 Circuit Implementation

3.1 Simulation Tool

The implementation of Gm-C-based ΣΔM is using the Mentor Graphics software.

(a) Pyxis is used for implanting the circuits.
(b) Eldo is used for simulation and perform the AC, DC, pole–zero, and noise analysis.

3.2 Device-Level Implementation

The third-order Gm-C-based ΣΔ modulator is designed in a 0.18 μm CMOS process.

3.2.1 Transconductance Amplifier G_{m1}

This work verifies the nonlinearity compensation technique with source degenerated telescopically as shown in Fig. 2. The degenerate transistors M_3 and M_4 are operated in the linear region and very near to cuff region. Due to this transistor region, the more current can pump into the output port. The maximum allowable output current can flow through the M_5–M_8. So, the aspect ratio of these transistors is identical. The transistors M_1–M_2 and M_9–M_{11} are created the resistive path to form the loop. Where the M_1–M_2 operates as the voltage controlled resistor and pulling the biasing current through the loop. Moreover, the M_{11} is operating in the linear region and it has the large output resistance. The incremental output currents are flows through this transistor to linearize the I–V characteristics of the G_{m1}. The speed requirement of this transconductance amplifier is defined by the aspect ratio of the degenerate transistors. Since the operating region of these transistors, the speed requirement is quite low. As a result, the additional power is needed to suppress the distortion and to get the high G_m of this circuit. As the more power is presented in the circuit, the circuit noise is normalized. Therefore, the circuit needs the quite more supply voltage. Hence, the circuit is operating with 2.3 V. The biasing circuits are providing the proper current mirroring.

3.2.2 DACs

As shown in Fig. 3, DAC1 is implemented for 16 logic levels represented in current values. The range of these values is from $-7.5(I_{LSB})$ to $+7.5(I_{LSB})$. Here I_{LSB} is the differential unit current that represents the least segmented bit (LSB). These currents are flowing through the bank of <15:1> differential pairs. These differential

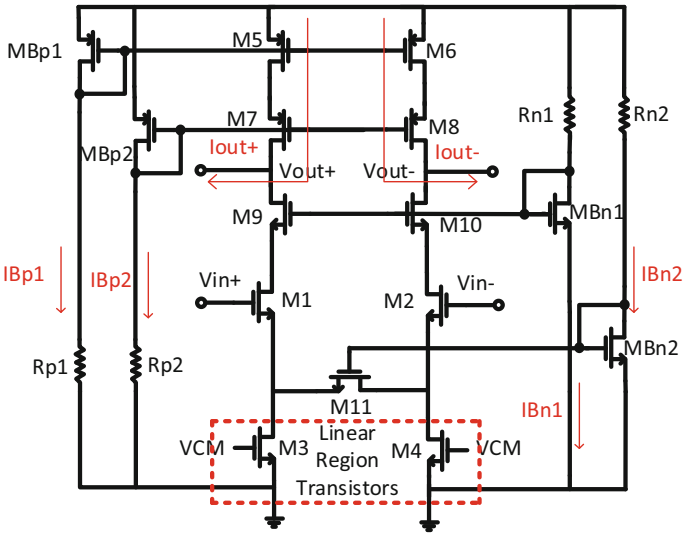
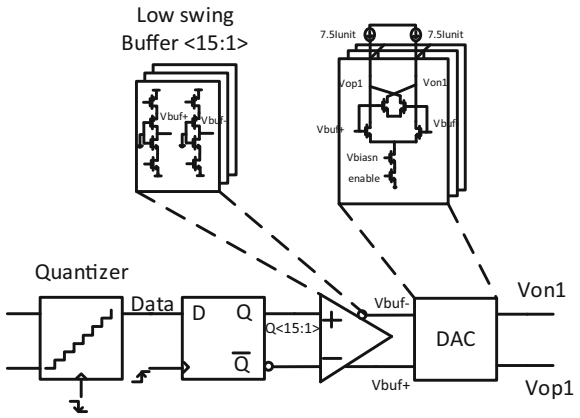


Fig. 2 Device-level implementation of G_{m1} with degenerative transistors M_3–M_4 (red dotted box) those operates in the linear region

Fig. 3 Signal path of DAC_1



pairs are driven by the low-swing buffers. These buffers are decreased the input voltage swing and also providing the time delay for differential pair proper operation. The delay must match the time required for desired logic level current completely flows through the current sink transistors. If this requirement is not matched, then the un-sink (current spikes) current is dissipated as the heat in a differential pair during switching. Moreover, these sink transistors are must long channel to take an advantage of flicker noise and also provide the larger overdrive voltage. The increasing the overdrive voltage, the thermal noise is reducing. The

differential pair of cross-coupled transistors is reducing the clock signal through the parasitic capacitor C_{gd} of input stage transistor. These cross-coupled pair transistors are operating as switches, but these drain voltages are in opposite potentials. Off course these transistors are identical.

Similarly, the DAC_2 and DAC_3 are implemented same as DAC_1. The difference in these DACs is the DAC_1 only has the cross-coupled transistors.

3.2.3 Transconductance Amplifiers G_{m2}, G_{m3}, $G_{m\mathrm{F}}$, and $G_{m\mathrm{R}}$

The transconductance G_{m2} amplifier is a simple differential pair with source degenerated as shown in Fig. 4. Here the linearity improved by same as the G_{m1}. These transistors M_3–M_4 are operating in linear and very near to cutoff region. The maximum allowable output current is controlled by the transistor M_5–M_6. These transistors must have biased at required current, which is equally to the output current. This output current is driving the load capacitor C_2. As a result, the C_2 produces the biasing voltage to G_{m3}. The differential current sensing is achieved by the transistors M_7–M_8, those are operating in the linear region.

The loop filter must have the more gain requirement, which is achieved by using folded cascade transconductance amplifier, the G_{m3} as shown in Fig. 5. The output current is provided by the transistors M_5–M_8. This output current controls the biasing for quantizer input driving stages. Therefore, the above transistors are perfectly matched and have less output impedance ($1/g_{m(M5–M8)}$). However, the more current can flow through the differential pair transistors M_1–M_2. This current divergence decreases the output current. As a result, the quantizer input stage is unbiased. To overcome this drawback, we can bias the transistors M_3–M_4 at very nearer to the cutoff region. Since there is less ground path through these transistors, the more current can flow through the folded cascade. For transistors M_9–M_{12} which are operating near the cutoff region, the more current can flows through the load capacitor C_3.

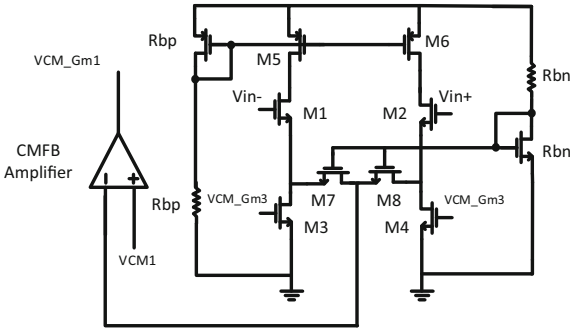


Fig. 4 Circuit diagram of G_{m2}

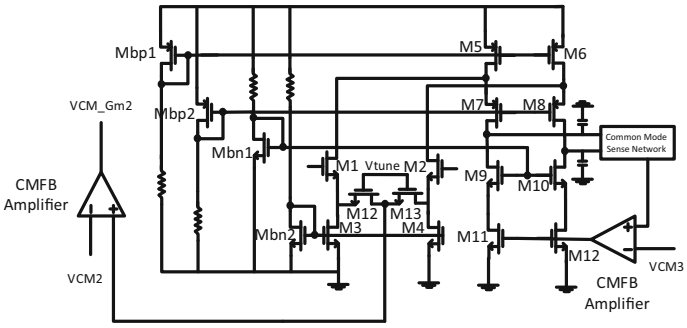


Fig. 5 Circuit diagram of G_{m3} and $G_{m\mathrm{F}}$

A dedicated common mode voltage sensing network for G_{m3} is needed for providing the wider output swings. G_{m3} and G_{mF} are designed with the folded cascade as shown in Fig. 5. The transconductance amplifier G_{mR} is in local feedback block (loop filter), and it is used to shift zeros of noise transfer function (NTF) from DC to in-band of the loop filter. For these reason, transconductance of $G_{m\mathrm{R}}$ has <2% of G_{m3}. Hence, it is realized by a large r_{ds}, the feedforward current through it is negligible compared with G_{m3} current and therefore does not change the loop characteristic.

3.2.4 A 4-Bit Quantizer

The 4-bit quantizer is composed of 15 comparators with a thermometer-coded output and its LSB is 80 mV. As shown in Fig. 5, the comparator consists of a double differential input stage and a regenerative latch. At CLK high phase, the reset switch in the input stage is turned on and the signal current flows through it. When CLK transits from high to low, the reset switch is turned off to start regeneration. In order to ensure 80 dB SFDR, the comparator offsets are designed to be within ¼ LSB (Figs. 6, 7, 8 and 9; Table 1).

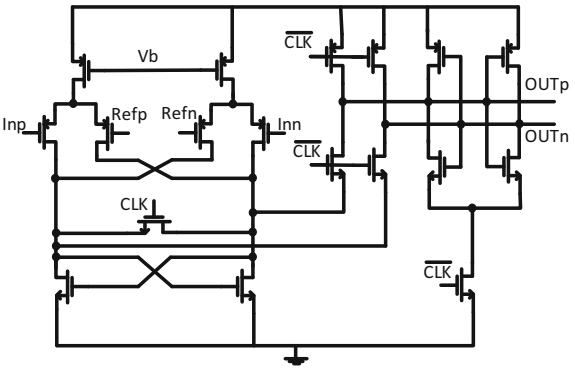


Fig. 6 Circuit diagram of a comparator in the 4-bit quantizer

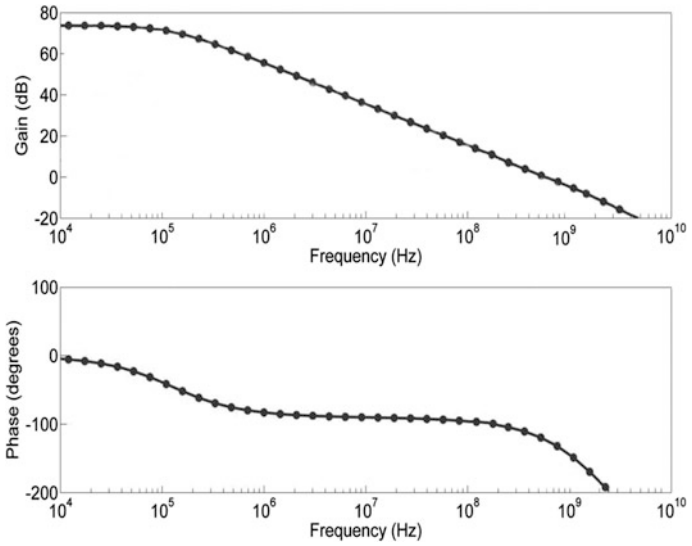


Fig. 7 Magnitude and phase plots

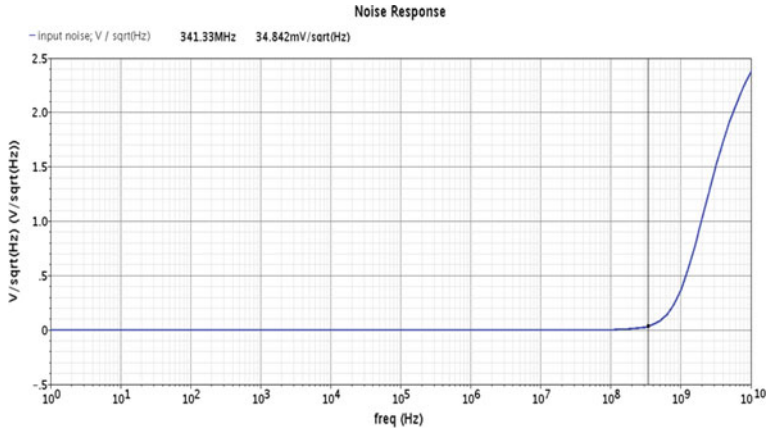


Fig. 8 Input noise reference

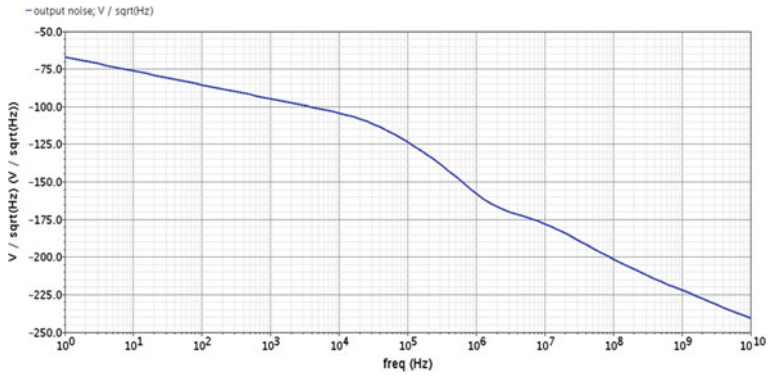


Fig. 9 Output noise reference

Table 1 Comparison of this work with other design

References	BW/Fs (MHz)	SNDR (dB)	Power (mW)	Process technology (μm)
[1]	10/600	75	70	0.18
[2]	25/500	67.5	8.5	0.09
[3]	10/950	72	40	0.13
[4]	20/900	78.1	87	0.13
[5]	25/500	63.5	8.5	0.09
[6]	10/600	76.6	16	0.09
[7]	20/640	63.9	58	0.13
This work	10/610	71.9	63	0.18

4 Conclusion

In this work, we implemented the delta–sigma modulator with nonlinear compensation technique for high SNDR dynamic range. This compensation is achieved by degenerative technique, as well as DAC transfer function matching to G_{m1}, through the feedback path. This design is implemented in 0.18 μm process technology. By using the G_m-C-based modulator, the high linear driving stage not needed. So, the complexity of design is simpler in real-time applications.

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Design of Current-Mode CNTFET Transceiver for Bundled Carbon Nanotube Interconnect

P. Murugeswari, A. P. Kabilan and V. E. Jayanthi

Abstract This paper proposes the carbon nanotube field-effect transistor-based current-mode transceiver for on-chip bundled CNT interconnect. Transceiver ensures current-mode signal transmission between devices and interconnects in on-chip. In proposed transceiver, the transmitter architecture drives the interconnect with less load, and the receiver section offers low impedance channel termination which results speedy operation with low power dissipation. The proposed design is exploited with the benefits of current-mode signaling and ideal characteristics of carbon nanotube. Performance evaluation has been done for the proposed carbon nanotube field-effect transistor architecture in HSPICE with 22 nm technology. The results are compared against the metal oxide semiconductor field-effect transistor counterpart. Simulation results justify that the proposed transceiver exhibits lesser delay by the factor of 1000 and 100 times lower power dissipation compared to metal oxide semiconductor field-effect transistor-based transceiver.

1 Introduction

Silicon-based technology has conquered the mainstream computing for the last four decades. Scaling of MOS devices and interconnects over different technology nodes results growth in VLSI technology leads to higher integration density and perfor-

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mance. As the VLSI technology progresses toward nanometer era, interconnect performance is the determining factor of the overall performance of an IC. When IC scales below 32 nm technology, copper interconnects suffer from significant sizing effects [1] such as surface and grain boundary scattering and electromigration. These effects increase the copper resistivity that leads to increase of delay and power dissipation. These limitations of copper imposed by scaling forced the designers to find an alternate interconnect material for next-generation ICs. Carbon nanotube (CNT), optical waveguide and graphene nanoribbon (GNR) have emerged as promising alternates for copper interconnect [2, 3]. In this paper, CNT has been chosen as an alternate to copper because of its outstanding electrical properties [4]. CNT exhibits both metallic and semiconducting behavior depending on its chirality vector [5].

Metallic CNT is used as on-chip interconnects in local, semi-global, and global. Depending on the number of tubes, CNT can be classified into single-walled CNT (SWCNT), SWCNT bundle and multi-walled CNT (MWCNT). In this paper, SWCNT bundle is considered as CNT interconnect. The application of CNT as interconnect is extensively studied with voltage-mode signaling [6–8].

CNT interconnect shows better performance than copper comparably lesser than optical interconnect [9]. The current-mode signaling is proposed for on-chip CNT interconnect to achieve the ITRS expectations and to reach the performance of optical interconnects.

Transceivers ensure the current-mode signal transmission through interconnect. It acts as interfacing circuit between devices and interconnect in integrated circuits [10]. It consists of transmitter or driver, interconnect, and receiver. Highly sensitive and high-speed transceivers are required for transmitting and receiving the signals through interconnects. In the proposed interfacing circuit, transmitter produces differential current and is sensed with current-sensing receiver. In transmitter side, single transistor with gate control architecture is used to convert voltage to current and transmits through interconnect. Interconnect is terminated with transimpedance amplifier section of receiver. It gives fewer loads to interconnect line compared to the transceiver used in [11]. In this paper, proposed current-mode transceiver is designed with CNTFET, and its performance is compared against voltage and current-mode MOSFET-based transceiver. CNTFET- and MOSFET-based transceivers are implemented with Stanford CNTFET model and TSMC BSIM4 model in HPSICE 22 nm technology. The designed transceivers are tested both in voltage and current-modes for CNT and copper interconnects.

This paper is organized as follows: Sect. 1.1 presents the review of CNTFET. Sect. 2 proposes the current-mode CNTFET transceiver. Sect. 3 analyzes the performance of CNTFET transceiver and compared with MOSFET counterpart through simulation results, and Sect. 5 presents the conclusion.

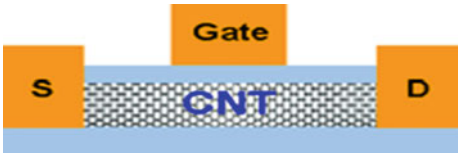

Fig. 1 Structure of MOSFET-like CNTFET

1.1 CNT Field-Effect Transistor

Carbon nanotube field-effect transistor (CNTFET) structure and operation are similar to that of conventional MOSFET devices. In CNTFET, conducting channel between source and drain is implemented with single-wall semiconducting carbon nanotube as shown in Fig. 1. The CNTFET can be turned ON or OFF electrostatically through the gate. The current—voltage characteristics of CNTFET are thirteen times better than MOSFETs. The threshold voltage of MOSFETs is fixed one, but in CNTFET threshold voltage can be varied by changing the tube diameter. The relationship between CNTFET threshold voltage (V_{th}) and its tube diameter of CNT is given in Eq. (1) [12, 13]. The diameter of CNT (D_{CNT}) has been computed from chirality vector (n, m) given in Eq. (2).

$$V_{th} = \frac{0.42}{D_{CNT}}. \tag{1}$$

$$D_{CNT} = 78.32 \times 10^{-12} \sqrt{n^2 + m^2 + nm}. \tag{2}$$

Because of analogous characteristics of CNTFET and MOSFET, the existing CMOS design infrastructures can be implemented with CNTFET to realize the future ICs with high-speed and low power dissipation [14, 15].

2 Current-Mode CNTFET Transceiver Design

Current-mode CNTFET-based transceiver is proposed for CNT interconnect to achieve wide bandwidth communication. Transceivers ensure the high-speed signal communication between interconnects and other devices present in ICs. Transceivers are comprised with transmitters and receivers. Current-mode transmitter, is the driver, is used to encode the digital data into current signal and transmits it via interconnect. The signals transmitted through interconnect experience attenuation. Receivers are the sense amplifiers which sense and amplify the attenuated signal from interconnect and latch it to the next stage. Clock signals are used to control transmitter and receiver to reduce static power dissipation [14].

2.1 Current-Mode Pseudo CNTFET Transmitter

A differential current-mode signaling is employed in pseudo CNTFET transmitter to improve both speed and power compared to voltage-mode CNTFET transmitter. It converts digital data into current signal and transmits it into interconnect. It does not require any predriver and driver like in voltage-mode transmitter, so that it reduces the area and delay overhead in signal transmission. Current-mode transmitter consists of two current sources (PCN1 and PCN2) and pseudo CNTFET logic-based control gates as shown in Fig. 2. In this circuit, transmitter generates the differential current and launches into interconnect. Signal Transmit Enable (TEN) controls the transmitter operation and enables the transmitter to charge and discharge interconnects. When TEN is enabled, signal current is transmitted through interconnect depends on the digital data (DIN) available at the input of transmitter. As DIN is high, PCN1 is ON; current is transmitted through $\overline{Dwire}$. When DIN is low, PCN2 is ON, current is drawn only in *Dwire*. Input DIN must be stable as long as the transmitter is enabled. When TEN is low, NCNTFETs (NCN1 and NCN2) are turned ON and discharges interconnect through them. It makes the transmitter for next data transmission.

The response time plot of *SPCNF* transmitter obtained from HSPICE simulation is shown in Fig. 3. DIN and TEN are the input and control signals, and Dwire and Dwire' are the true and complement output currents. The observed average power and delay from simulation are 51.7 μW and 1.68 pS, respectively.

2.2 CNTFET Clamped Interconnect Current Sense Amplifier

To overcome the delay, power dissipation, and other physical limitations of MOSFET-based sense amplifiers, a CNTFET-based clamped interconnect current

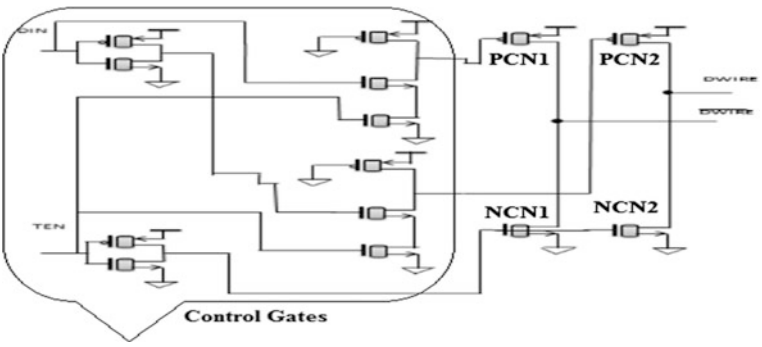

Fig. 2 Current-mode single PCNTFET (SPCNF) transmitter

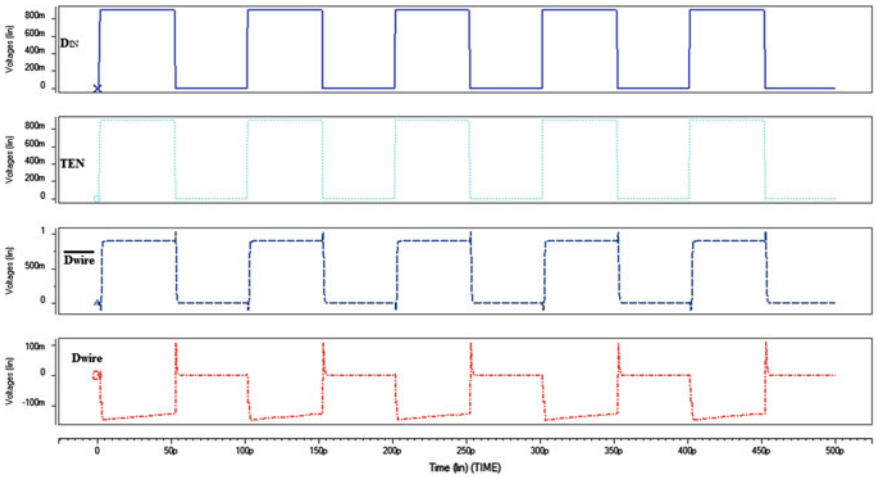

Fig. 3 Transient response of current-mode SPCNF transmitter

sense amplifier (CICSA_CNT) is proposed. It has transimpedance amplifier as input stage and cross-coupled inverter as load as shown in Fig. 4. The input stage consists of common gate with CNTFETs CN1 and CN2 which exhibits low input impedance. CNTFETs CN3–CN6 forms the cross coupled inverter.

When the clock is in the pre-charge phase, outputs are charged to VDD through CN7 and CN8 despite the consequences of input. In the evaluation phase of the clock, this circuit responds to the inputs at the sense nodes. Once the difference signal sensed at the output, cross-coupled inverters execute the regenerative

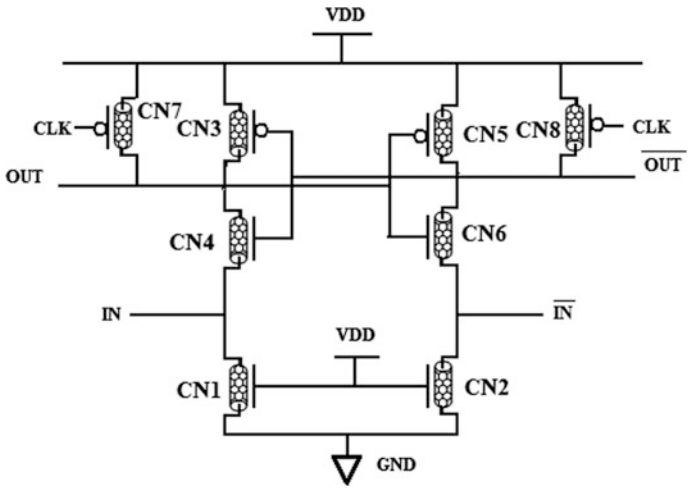

Fig. 4 CICSA_CNT architecture

operation which forces the one of the output to low, and the other to high. The high speed of response to the inputs is achieved in it due to less number of transistors in the evaluation path as well as the high current carrying capability and ballistic transport of CNTFET. Furthermore, a visible increase in bandwidth is observed. CICSA_CNT consumes less power due to the combined effect of CNT and current sensing.

3 Performance Analysis

CNTFET- and MOSFET-based transmitters and receivers with voltage and current-mode signaling are simulated in HSPICE. Performance parameters obtained from simulation are summarized in Table 1. Voltage-mode transmitter architecture in [11] implemented with MOSFET and CNTFET and MOSFET current-mode transmitter in [15] are taken for performance comparison, and the comparison is extended for the proposed CNTFET architecture as shown in Fig. 2. Voltage-mode receiver architecture in [16] implemented with MOSFET and CNTFET and MOSFET current-mode receiver in [17] are taken for performance comparison.

In voltage and current-mode signaling, CNTFET-based transmitter and receiver exhibit better delay and power performance as compared with MOSFET due to ballistic transport, large mean free path, and remote joule heating effect of carbon

Table 1 Performance comparison of MOSFET and CNTFET transceivers

	Signaling techniques	Technology	Performance metrics	
			Delay (pS)	PDP (fJ)
Transmitter	Voltage-mode	MOSFET [11]	140	78.0
		CNTFET	32.2	15.5
	Current-mode	MOSFET [15]	36.6	174
		CNTFET	0.2	0.002
Receiver	Voltage-mode	MOSFET [16]	33	1.650
		CNTFET	3.3	0.155
	Current-mode	MOSFET	7.33	0.0076
		CNTFET	1.5	0.006
Interconnect (10 mm length)	Voltage-mode	Cu	21,700	2000
		CNT	1100	0.049
	Current-mode	Cu	11,500	37,950
		CNT	37.9	0.00011
Total interconnect link	Voltage-mode	Cu + MOSFET	217,173	14,529
		CNT + CNTFET	135.5	101.85
	Current-mode	Cu	115,043	5,552,220
		CNT	41.08	0.00811

nanotube [18]. In MOSFET-based transmitters, current-mode signaling gives less delay and more dissipation during signal transmission as compared to voltage-mode, whereas in CNTFET-based transmitters, current-mode exhibits 160 times less delay and 10^3 orders less power dissipation compared to voltage-mode because of high current carrying capacity of CNT and the benefits of current-mode signaling and pseudo logic. In pseudo CNTFET logic, the threshold voltage is increased in accordance with the CNT tube diameter which reduces the short circuit current in CNTFET results low power dissipation.

Low input impedance of current-sensing receiver terminates the interconnect by short which avoids the charging and discharging of interconnect capacitor. This reduces switching activity and becomes independent of dynamic power dissipation. So that both current-mode MOSFET and CNTFET receivers are more power efficient as compared to its voltage-mode counterpart. The proposed CNTFET-based current-sensing receiver has high speed of signal sensing and more power efficient due to intrinsic properties of CNT and remote joule heating effect. Table 1 summarizes the performances of transmitters and receivers.

From Table 1, it is observed that current-mode CNT interconnect (10 mm) is the optimum choice with significant performance. The proposed current-mode SWCNT-bundle interconnect has 29 times lesser delay compared to voltage-mode SWCNT bundle, whereas in copper interconnect, current-mode produces only two times lesser delay compared to voltage-mode. Current-mode copper dissipates more power compared to voltage-mode, whereas in CNT interconnect, current-mode dissipates less power compared to voltage-mode.

4 Test Setup

The proposed CNTFET- and existing MOSFET-based transmitter and receiver architectures are optimized individually against the test circuit as shown in Fig. 5. The test architecture consists of interconnect link between two functional blocks. To test the performance of MOSFET- and CNTFET-based transceivers, copper and metallic SWCNT bundle are used as interconnect.

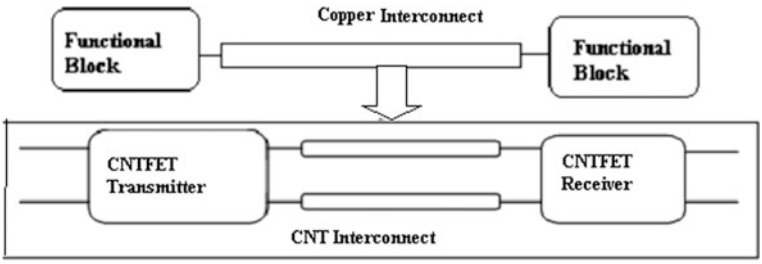

Fig. 5 Test architecture

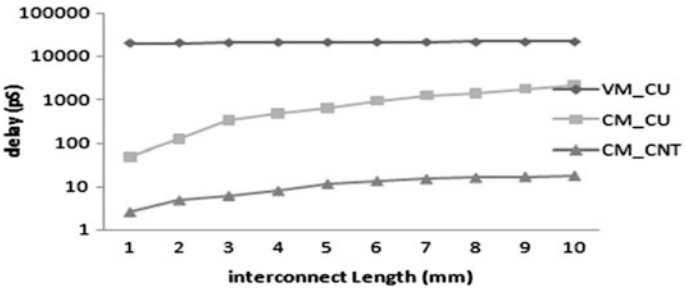

Fig. 6 Performance comparison of CNT and copper interconnect link

Table 2 Performance comparison between CMCNT and optical interconnect link

	Delay (pS)		PDP (fJ)	
	OI [19]	CMCNT	OI [19]	CMCNT
Transmitter	23.8	0.2	119	0.002
Receiver	4.2	1.5	1.26	0.006
Interconnect	46.7	37.9	0.45	0.00011
Total	74.7	41.08	120.71	0.00811

The delay performance of voltage and current-mode copper and current-mode SWCNT bundle is graphically shown in Fig. 6. Current-mode SWCNT-bundle interconnect link exhibits lesser delay as compared to voltage-mode copper by 570 times and current-mode copper by 302 times for 10-mm interconnect length. The sum of individual delay and power delay product of transmitter, receiver, and interconnect gives the total delay and power delay product of the transceiver.

From Table 1, it is observed that interconnect delay determines the overall delay performance of total interconnect link, whereas pertaining to the power delay product, transmitter decides the overall performance of interconnect link. The performance of CNT interconnect link is also compared against optical interconnect link, and the results are summarized in Table 2. The performance metrics of optical interconnect link is taken from [19]. From Table 2, the MOSFET-based driver and receiver circuits limit the performance of the optical interconnect link, whereas current-mode CNTFET transceiver shows outstanding performance.

5 Conclusion

In this paper, current-mode CNTFET transceiver is proposed for on-chip SWCNT-bundle CNT interconnects. The novelty applied on CNTFET current-mode transceiver achieves high-speed signal transmission with lower power dissipation in CNT on-chip interconnect. Performance comparisons in Table 1 show that current-mode CNTFET transceiver exhibits better delay performance as

compared to MOSFET counterpart. Since CNT dissipates heat remotely and current-mode signaling is independent of signal frequency, proposed CNTFET current-mode transceiver achieves more than 90% power efficiency than transceivers used in optical interconnects. In both voltage and current-mode signaling, copper interconnect significantly determines delay and PDP performance, whereas in CNT interconnect link, interconnect determines the delay performance and transmitter determines the power delay performance. Pseudo CNTFET logic-based control gates decrease the power dissipated in transmitter that results reduction in overall power dissipation of CNT interconnect. From the above analysis, it is concluded that current-mode CNTFET transceiver can be used to achieve high-speed (THz) signal transmission with low power dissipation in future ICs.

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Weak Cell Detection Techniques for Memristor-Based Memories

V. Ravi and S. R. S. Prabaharan

Abstract By virtue of its non-linear switching characteristics manifested by ionic percolation in the solid lattice under the influence of applied voltage, memristor is regarded as non-volatile memory (NVM) otherwise known as resistive random access memory (RRAM). It possesses promising characteristics such as low power, non-volatility, high density and multi-level functions to replace the present CMOS gates and memories. Nevertheless, it is greatly affected by process variations, particularly variation in thickness. Fault analysis proves that there are number of stability faults occur in addition to other typical memory faults. This research work presents a novel built-in self-test techniques to test the weak memory cells in memristor memory arrays. The basic idea is to create electrical stress to the cells such that the strong cells will retain its state while the weak cells expected to flip its state. Most of the design for testability (DFT) techniques employ the deterministic test patterns algorithm like March tests. Though March tests are very effective for the conventional memories, they are not so effective in case of memristor-based memories. Stability faults such as the undefined state faults cannot be sensitized using the conventional March test patterns. Thus, to enhance the fault coverage, new weak read and weak write mode approaches namely short refresh time (SRT), short write time (SWT) and low write voltage (LWV) are to be employed in the test sequence. Cadence Spectre gpdk180 library and memristor linear ion drift model with Biolek window function were used to perform the stability fault injection and circuit functional simulation.

Keywords Memristor · Design for testability · Faults · March test
Resistive random access memory

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1 Introduction

Though the top semiconductor companies like Intel, Samsung and TSMC expected to produce 10 nm ICs in the forthcoming year, the shrinking may not continue in future, in the sense that the popular Moore's law almost comes to an end. Industries started working on identifying new devices which are more capable and smaller in size. One such device is memristor (memory resistor) which is under research to replace CMOS in digital, memory and neuromorphic applications. Memristor was initially coined by Leon Chua [1] in 1971 by theoretically showing presence of fourth passive element, relating the flux and charge. Memristor is a type of resistive random access memory (RRAM) and is one of the outstanding candidates for next generation memory technology due to its low power, high performance, high density, non-volatile data and multi-level cell (MLC) operations.

An RRAM memory uses a range of resistance values to represent the logic states of the memory. Generally, low resistance state (LRS) is fixed as logic high and high resistance state (HRS) has denoted as logic low. Whereas in multi-level cell (MLC) memory operations, the total range of the resistance is divided in such a way that each range represents a logic state.

In 2008, HP presented [2] the first physical version of the memristor using bipolar Tio_2 thin film technology. Further HP proposed the nanowire-based crossbar architecture to improve the density of the memory. After HP's development, many companies and researchers tried to fabricate memristors with different materials to improve the performance, characteristics, speed and compatibility of the device with CMOS. One of the easiest ways to develop a memristor-based memory is to design a crossbar structure with memristor placed at the junction of the row and column of the memory array. This arrangement is sometimes called as 1 M memory array, and it provides the highest density. However, it faces the memristor specific problem called "sneak path". The sneak path is the undesired path for current in parallel with expected path. This unwanted current flow results in fruitless operations in the cell under operation and undesired disturbances in the other neighbouring cells. Numerous methods were proposed to solve the sneak path problems [3, 4]. One of the basic ideas to address the sneak path problem is to use an additional selector device like transistor or diode to choose the cell under consideration. So each memory array junction point in the crossbar structure comprises of one selector device and one memristor. This arrangement is called as 1T1 M or 1D1 M memory when the selector device as transistor or diode, respectively. In addition to the sneak path problems, the effect of process variations is high in memristor-based memory.

Research articles [5, 6] discuss the process variations and its influence in memristor-based memories. Many research outcomes prove that the density defects in nanoscale technologies are considerably higher than the silicon technologies due to its non-deterministic nature of the post-lithographic fabrication at nanoscale level [7]. Contributions of this research work are as follows

1. Define fault models to represent the unique defects of the memristor
2. Analysis and modelling of resistive defects of the memristor memory
3. Electrical simulation for fault-free memristor memory and faulty memristor memory
4. Three techniques to detect unstable memristor cells of the memristor-based memory.

This paper is described into six different sections. Section 2 briefs the memristor-based memory and its crossbar architecture. Section 3 discusses the various defects and faults of the memristor-based memory. Section 4 summarizes few existing techniques to test the memristor-based memories. Section 5 describes the proposed weak cell detection techniques and its simulation results, and Sect. 6 reviews and concludes the article.

2 Memristor-Based Memory

Ho [8] proposed the idea of using memristor for non-volatile memory design. The memristor fabricated by HP in 2008 used titanium oxide material which was injected with various oxygen atom doping rates. This material is electrically switchable. As shown in Fig. 1, for a device length of D, it contains a doped region of length w, and the rest $D - w$ of undoped region. The length of doped region (w) can be varied by applying a voltage across the two-terminal memristor device.

Based on the memristor normalized internal state **w/D**, the logic value can be determined. The internal state denotes the dopants drift along the memristor and is inversely proportional to the memristance. Since the memristor cells are analogue devices, there is a need to define the logic states based on the internal state as in Fig. 2. Though, ideally $w/D = 0$, $w/D = 1$ are treated as logic-0 and logic-1, it is always safe to introduce some margins to counter noise injections. Accordingly, logic state is defined as follows: logic 1 0.6 < **w/D** < 1, logic 0 0 < **w/D** < 0.4 and undefined (0.4 < **w/D** < 0.6).

Figure 3 shows the implementation of memristor memory write and read operation. Generally, bias voltage is applied in such a way that the resistance of the memristor changes to low for logic 1 and high for logic 0, whereas the read operation is not easy as write operation. To read the internal state, certain voltage is

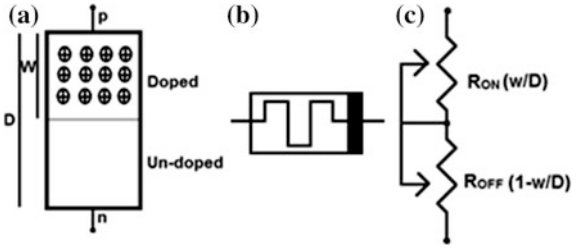

Fig. 1 **a** Model **b** symbol **c** electrical model

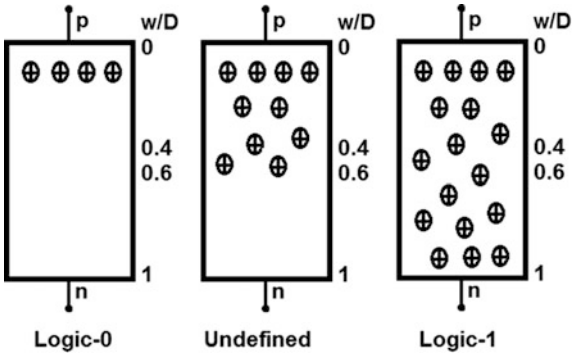

Fig. 2 Logic state definition

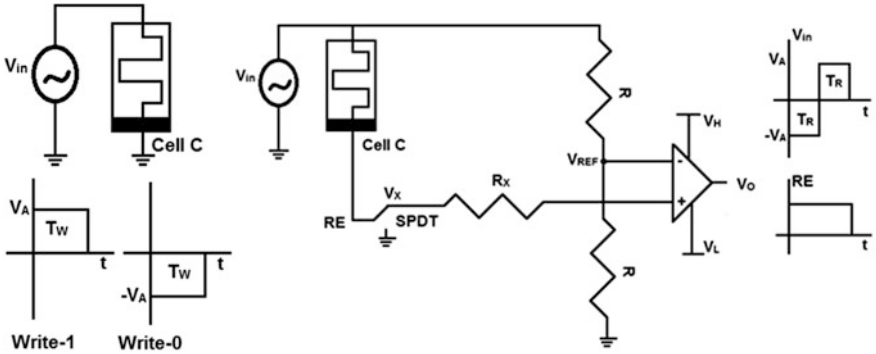

Fig. 3 Write and read operations

to be applied in order to sense the state. If this sensing operation is not carefully designed, it may destruct the content of the cell. There are different techniques proposed to read the data without disturbing the data [9]. One such technique is to apply a negative followed by a positive pulse as shown in Fig. 3; pulse width T_R and amplitude $|V_A|$ are applied across the memristor in order to sense the internal state and recover the state back to the original state.

3 Memristor Memory: Defects and Faults

Faults in memristor-based memories are classified as internal faults (due to memristor cell and memory array defects), external faults (due to peripheral circuitry defects) and nanowire faults (due to defects in nanowires). As the external faults and nanowire faults are commonly present in the MOS memories and being addressed in the number of research papers, only memristor faults are discussed in

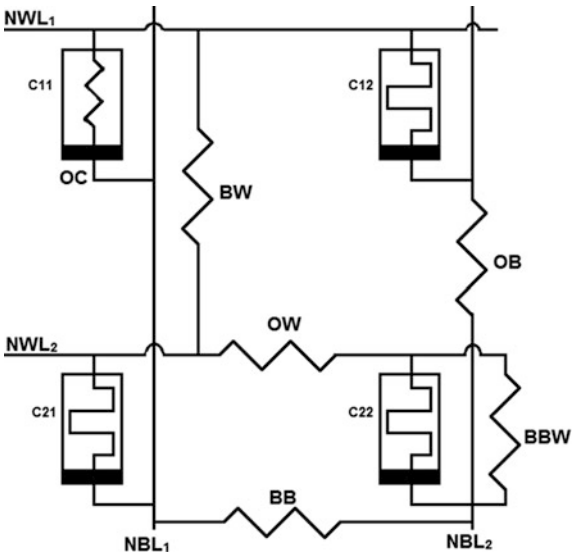

Fig. 4 Memristor memory internal faults

this section. Figure 4 shows some of the possible internal faults such as open-circuit fault (OC) in the cell C11, open bit-line fault (OB), open word-line fault (OW), bit-line and word-line bridge fault (BW), bit-line and bit-line bridge fault (BB).

Any deviation in the length or area of the memristor results in a change in the resistivity of the material and hence changes in the resistance. This change in resistance depends on the doped and undoped regions of the memristor. So, there will be a non-uniform shift in the minimum ($R_{off} + \Delta R_{off}$) and maximum ($R_{on} + \Delta R_{on}$) value of the resistance. As a result, three different faults are possible namely fast write fault, slow write fault and deep fault [10]. Any variation in the doping affects the mobility of the ions/charge carriers in the memristor. Excessive doping produces fast switching between the states, and less doping yields slow transition from one state to another state. Any broken contact or missing metal wires, extra lines, etc., are considered as open or short defects. It can be electrically modelled as undesired series resistance namely R_{open} and R_{short} between any circuit paths to the memristor.

4 Memristor Memory: Testing Techniques

March test is one of the standard test methods used for testing the memories. The traditional March test only detects the conventional faults such as stuck-at faults (SA-1 and SA-0), transition faults (TF-0 and TF-1), address decoder faults and coupling faults. The conventional March algorithm is modified by [11] to catch the two new memristor faults namely write disturbance fault (WDF) and dynamic write disturbance fault (dWDF) in 1M1T cell. The idea of testing each junction point

(cell) of the crossbar memory one by one is time consuming and more laborious. More efficient testing methods are required to test nanoscale memories to catch maximum possible faults without increasing the test duration. One such novel technique was proposed by [12] and follows the "Divide and Conquer" approach to detect faults simultaneously in a group of cells by that it significantly reduces the test duration. The proposed testing approach uses additive nature to catch the faults. This technique equally divides the search space into two halves recursively until catching the fault. As we have to measure either current or voltage to locate the fault, one possible way to speed up test process is to measure the several currents or voltages simultaneously in the group of cells to decide whether the fault is present or not. The comparison of actual current flowing through the memristors with expected current allows deciding whether the fault is present or not.

5 Proposed Weak Cell Detection Techniques

This section discusses about the proposed weak cell detection techniques for the memristor-based memories. The fundamental idea behind the weak cell detection techniques is to electrically stress the cell such a way that strong cells will retain its state, whereas the weak cells are expected to complement its logic state. The proposed techniques use three electrical parameters namely write voltage (low write voltage), write time (short write time) and refresh time (short refresh time) to stress the cells. The simulations are performed using the Cadence Spectre gpdk180 library with Verilog A model for memristor. Linear ion drift model with Biolek window function incorporated to limit the internal state changes to the boundary condition (i.e. device limits) is considered. The Verilog A model published in [12] is used for the simulations. The device specifications are: $D = 2$ nm, $R_{on} = 100\ \Omega$, $R_{off} = 200{,}000\ \Omega$. The ratio of w and D is defined as the normalized width of the memristor. Figure 5 shows the behaviour of strong memory cell for write and read operations.

Fig. 5 Fault-free write and read operation

5.1 Low Write Voltage (LWV)

Low write voltage method detects the weak cells by applying low write voltage. On applying low write voltage, the good cells will not get adequate voltage to alter its state from one logic to another logic level, whereas the weak cells get affected by this voltage stress and flip its state from undefined state to defined state.

The following steps are followed to detect the weak cells.

1. Initialize the memory cells with logic 1
2. Write logic 0 to each cell
3. Apply weak logic 1 by low write voltage
4. Read the cells; good cells produce logic 0, whereas faulty cell produce logic 1
5. Repeat the steps 1–4 for the complementary.

Figure 6a indicates the response characteristics of fault-free cell for weak write voltage, and Fig. 6b illustrates the characteristics for the faulty cell. Figure 6a clearly shows that the fault-free cell's normalized width is not able to rise up to the level where it can be sensed as logic high, whereas the faulty cell whose normalized width may be in the undefined state will easily flip to the applied weak write operation.

5.2 Short Write Time (SWT)

Short write time technique senses the weak cells by applying write voltage for short span of time. On applying short write time, the strong cells will not get adequate time to alter its state from one logic level to another logic level, whereas the weak cells get affected by this stress and flip its state from undefined state to defined state. Figure 7a, b illustrates the response of fault-free cell and faulty cell for short write time method.

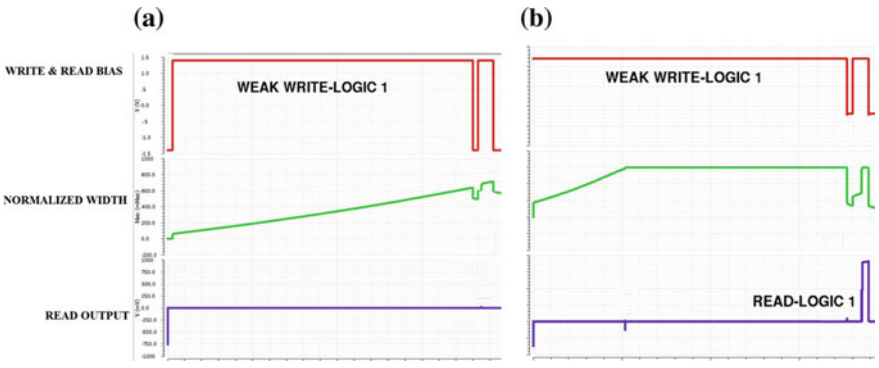

Fig. 6 **a** Weak write voltage-fault-free cell **b** weak write voltage-faulty cell

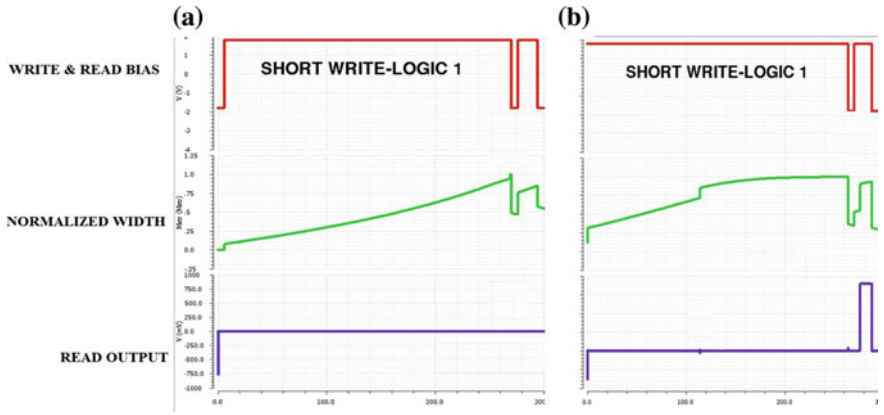

Fig. 7 **a** Short write time-fault-free cell **b** short write voltage-faulty cell

The subsequent steps are adopted to spot the weak cells.

1. Initialize the memory cells with logic 1
2. Write logic 0 to each cell
3. Apply logic 1 for short amount of time
4. Read the cells; good cells produce logic 0, whereas faulty cell produce logic 1
5. Repeat the steps 1–4 for the complementary.

5.3 Short Refresh Time (SRT)

This technique finds the weak cells by offering less refresh time during the read cycle. Generally, we need to apply voltage for small duration to read the content of the memristor memory cell. But this bias voltage disturbs the state of the memristor and hence destructs the content of the cell. To avoid the destructive read, we need to apply compensation pulse for the required amount of time (refresh time) to restore the internal state back to its initial state after each read operation. In this technique, the electric stress is created applying refresh pulse for short amount of time. On applying short refresh time, the strong cells will get marginally affected whereas the weak cells considerably affected. The weak cells can be identified by performing consecutive read operation.

Figure 8a, b illustrates how short refresh time can be used to differentiate good cells and weak cells, respectively.

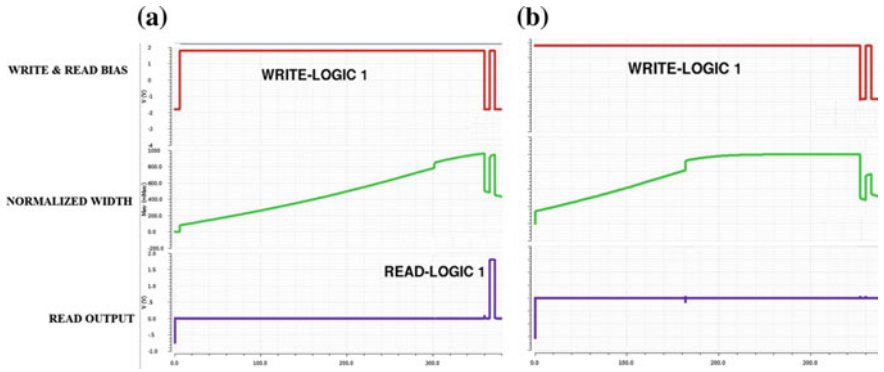

Fig. 8 **a** Short refresh time-fault-free cell **b** short refresh time-faulty cell

The subsequent steps are followed to identify the weak cells.

1. Initialize the memory cells with logic 1
2. Read logic 1 from cells, but with short refresh time
3. Read the cells again; good cells produce logic 1, whereas faulty cells produce logic 0
4. Repeat the steps 1–4 for the complementary.

6 Conclusion

In this research work, we have presented the new testing methods to catch the weak memristor memory cells. The electrical simulation results were presented to prove that the proposed weak cell detection techniques are effective in catching the weak cells. The discussed methods can be considered as the part of the built-in self-test circuits of the memristor-based memory chip. Due to the non-deterministic nature of the post-lithographic fabrication at nanoscale level, the behaviour of the memristor memory is not uniform across the PVT (process, voltage, temperature). So applying fixed stress may not be more effective in weak cell detection. So the stress parameters namely voltage, write time, refresh time can be made programmable by including additional circuitry in the design which will allow us to tune the optimum stress to be applied to identify the weak cells.

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Enhancement of Transconductance Using Multi-Recycle Folded Cascode Amplifier

Mayur T. Kalkote and S. Ananiah Durai

Abstract Background: Many analog design techniques and methodology have been devised for better performance of amplifier. Nowadays operational amplifier is the backbone of the analog and mixed-signal device. It is fundamental block of the many design circuit that utilizes high gain, high bandwidth, fast settling time. Op-amp is one of the basic building blocks of analog circuit which has wide range of application such as biomedical application, ADC converter, switched capacitor filter. **Methods/Statistical analysis**: This paper presents the novel structure of folded cascode amplifier for enhancing the gain. In this quadruple recycling folded cascode (QRFC), operational transconductance (OTA) amplifier is used to improve the performance over the conventional folded cascode (FC), double recycle, and improved recycle folded structures. The proposed structure uses positive feedback, cross-coupled transistors which significantly improve its unity gain bandwidth, DC gain, and slew rate as compared to others OTA structures. Circuit-level simulations and analysis results were done with 180 nm CMOS technology validate the improved gain of 95 dB for single-stage fully differential mode and enhance bandwidth of 185.2 MHz. **Findings**: A location-based layout study is done. The problem with this method is that while we go to increase gain of amplifier as much as high we have to compromise with phase margin. **Application/Improvements**: By using this current reuse technique we achieve high gain as compared with the other operational amplifiers. Also due to this method, its gain bandwidth frequency also increases.

Keywords Operational transconductance amplifier · Recycling current
Folded cascode · DRFC

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1 Introduction

Generally, the operational transconductance amplifiers (OTAs) are extensively used in analog device (medical application like biosensors, industrial automation sensors) and mixed-signal device for their better performance and its high gain. Telescopic and folded cascode are the two major building blocks for CMOS device in analog circuit, but instead of telescopic, the folded cascode is preferred due to its better gain and signal swing at output [1]. Although multistage amplifiers are used for the better gain, but in consideration of bandwidth, single-stage OTAs are better than multistage. It is one of the most important blocks in analog circuit design which plays a major role.

Recently one of the most common architecture which is widely used in analog and mixed-signal circuit, which is single stage in multistage known as folded cascode amplifier which is used for its better gain and swing in future CMOS technology process. The folded cascode amplifier (FC) is basically used for low-voltage application and operated at very low input signal to achieve high gain and bandwidth [2]. The performance of OTAs is limited due to various factors such as gain, bandwidth, slew rate, voltage swing, etc. for this different work used different techniques to increase the gain as well as bandwidth with low power consumption [3]. As we go for improvement of the performance of FC, OTA power budget is a major Calibriant (power increased with FC op-amp performance improvement techniques). This has to be done without compromising the gain or UGBW with reduction in transconductance (g_m) [4]. On other hand, if we use.

Multistage amplifier for higher gain which introduce its own problem like, additional pole–zero, noise which degrade the performance of the micro sensor

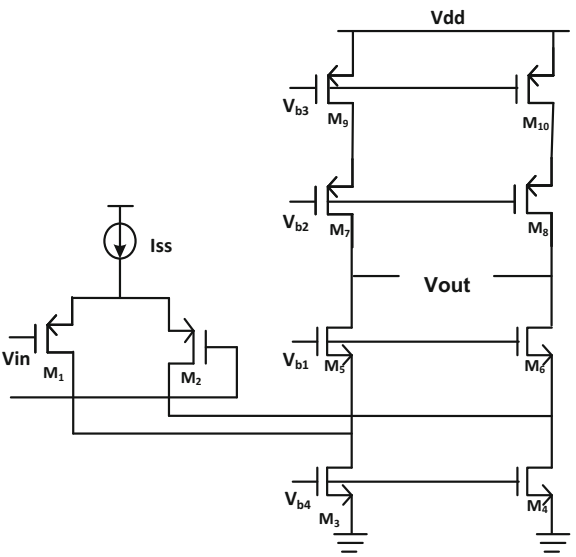


Fig. 1 Basic cascode OTA

circuit [5]. In addition, in the driver transistor, PMOS input pair is used in case of NMOS because of its less flicker noise, high dominant pole.

The simple conventional folded cascode amplifier is shown in Fig. 1.

In which the transistor M_1 and M_2 act as driving transistor which equally fold the current through input and output [6]. As a result, the transistors M_3 and M_4 draw most current through it and act as a current source without any signal amplification. However, their role is limited to provide folding node for the small current which is generated by that two driver transistor. Numerous techniques have been proposed in various paper to enhance the significant performance of folded cascode such as recycle the input stage means recycle the current through multipath (double-recycle, multi-recycle tech) [7]. Also used positive feedback stages, cross-coupled transistor to increase the overall performance of the conventional folded cascode stage.

2 Conventional FC and RFC Structure

The conventional FC and RFC are shown in Figs. 1 and 2. To improve the efficiency of conventional FC design the modified FC called Recycle Folded. The input drivers in FC M_1 and M_2 are split in half to produce transistors $M_{1a(b)}$ and $M_{2a(b)}$. As mentioned before, M_1 is twice of that M_{1a} and conduct twice amount of current ($g_{m1} = 2g_{m1a}$) for same power consumption. Which conduct fix and equal current $I_b/2$ (Fig. 2). Also, the bottom-most transistors M_3 and M_4 also split as $M_{3a(b)}$ and $M_{4a(b)}$ with the ratio of K:1 which draw more current through it. The cross-connection of the current mirror to insure that small current added in the source of M_5 and M_6 (Fig. 2). Due to this, the small current is amplified by the ratio factor K. Transistors M_{11} and M_{12} are used to maintain the constant drain potential of $M_{3a(b)}$, $M_{4a(b)}$. The transconductance of FC is Gm, but due to splitting of transistor, the effective transconductance improve [8].

In order to achieve enhancement in the transconductance, its needful to operate all transistor in saturation region, and it follows square law for drain current which is given by,

$$I_D = 1/2\,\mu_n C_{OX}\,W/L\left(V_{gs} - V_{th}\right)^2$$

Here, to maintain same power budget for both FC and RFC shown in Figs. 1 and 2. Current through M_5-M_{10} is a function of K which maintains same budget.

So, the enhance transconductance helps to boost the gain of amplifier and also the bandwidth. Design and choose the ratio factor such that it fit into all required parameter but it is limited by ratio factor we can't increase more because the degradation in phase margin. K must be chosen < 3 for proper performance. Hence, the transconductance of the RFC is double than FC so that gain, voltage swing,

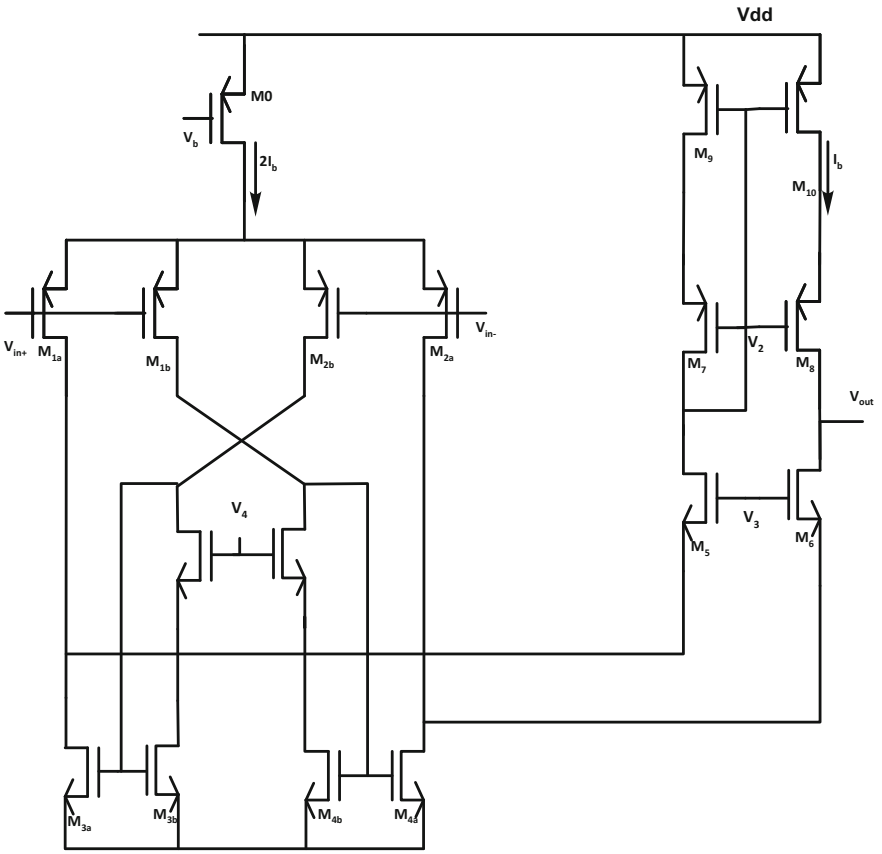


Fig. 2 Recycle-folded cascode OTA

GBW are higher than FC. The small signal analysis of both FC and RFC is as follows:

$$G_{\mathrm{mRFC}} = g_{\mathrm{m1a}}(1+K) \tag{1}$$

$$G_{\mathrm{mFC}} = g_{\mathrm{m1}} \tag{2}$$

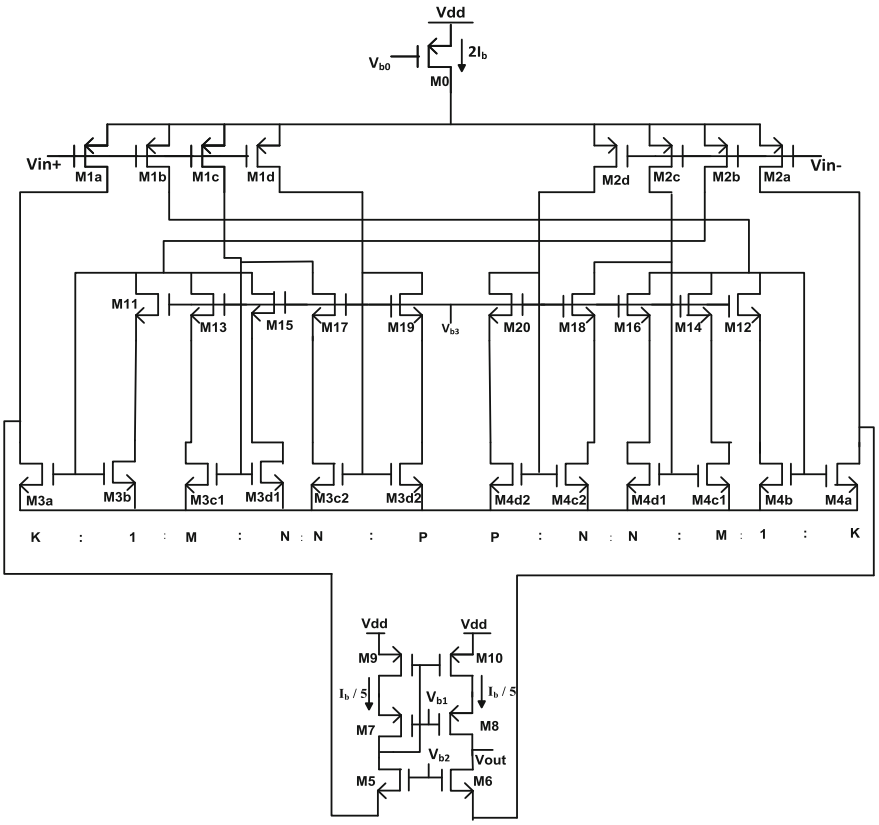


Fig. 3 Proposed QRFC OTA

3 Proposed QRFC OTA Structure

Figure 3 shows the quadruple recycling folded structure (QRFC). The differential pair of input is now replaced with four times as compared with the conventional FC (M_{1a}-M_{2a}, M_{1b}-M_{2b}, M_{3a}-M_{3b}, M_{4a}-4b), and the current source (M_{3c}-M_{4c}) are divided in (M_{3c1}-M_{3d1}, M_{4c1}-M_{4d1}, M_{3c2}-M_{3d2}, M_{4c2}-M_{4d2}). The purpose of this splitting of transistor is to reuse the shunt current source more times to increase the performance without more power loss.

Recently, Zushu Yan purposed an double recycling method which is used for folded cascode amplifier in which M_{3c}-M_{4c}, M_{3d}-M_{4d} is added in the input structure and the transistor M_{13}, M_{14}, M_{15}, M_{16} are used for matching the bias current. Since, the bias current in diode-connected M_{3b} and M_{4b} are reduced while M_{1b}, M_{1c}, M_{2b}, M_{2c} remains unaltered, so in this paper, recycling those current source again which results in higher performance of amplifier. The main aim of this paper is to improve

the overall output resistance across the output. We propose the robust gain boosting technique for single-stage amplifier using the shunt current source reusing and achieve gain 30 dB more than the conventional amplifier without compromising stability.

3.1 Circuit Description

Figure 3 shows the structure of modified QRFC-proposed OTA. The differential driver transistor pair is split four times to recycle the source current more times. Since RFC, DRFC, and proposed QRFC are modified from main conventional folded cascode OTA as shown in Fig. 1 by properly adjustment of current mirror ratio which exact comparison between these four types of OTA in terms of transconductance, slew rate, bandwidth.

As mentioned before, the transconductance of FC is Gm and transconductance of RFC is $(K + 1)$ gm1 which cannot exceed more than three times because of its symmetric slew rate. The proposed structure given by Zushu Yan is DRFC shown in whose transconductance is written as,

$$G_{\mathrm{mDRFC}} = [1 + \{2[K(2M + 1) - (M + N + 1)/K + M + N + 1\}] \tag{3}$$

In this DRFC, the current source provides much freedom for recycling the current through it by adjusting the size value K, M, N of the bottom transistor which help to increase the effective transconductance of DRFC. Also, in QRFC, these current sources again reuse to enhance performance by adjusting K, M, N, P value of transistor which result the transconductance improved in QRFC is more than FC/RFC/DRFC. The gain and gain bandwidth (GBW) product are also higher as compared to other. Similarly for QRFC, these current sources reuse four times so it's called quadruple recycle OTA.

Adjusting value of K, M, N, P design, the QRFC helps to enhance the overall performance of OTA compared with others. The following equations show the mathematical analysis of all OTAs. The transistors M_{11} and M_{12} in RFC shown in Fig. 2 split into M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, and M_{20} in which M_{19}, M_{3d2}, M_{20}, M_{4d2} provide high impedance to the path. The small current flows through current mirror node which is larger than the previous method. The small signal current is strengthened by the ratio of K, M, N, P. In this, most of the transistors are working in subthreshold region which helps to ignore the variation in the small signal input.

3.2 Equations and Mathematical Analysis

For output resistance of OTA is given by,

$$R_{\mathrm{oFC}} \approx g_{\mathrm{m6}} r_{\mathrm{d6}} (r_{\mathrm{ds2}} || r_{\mathrm{ds4}}) || g_{\mathrm{m8}} r_{\mathrm{ds8}} r_{\mathrm{ds10}} \tag{4}$$

$$R_{\mathrm{oRFC}} \approx g_{\mathrm{m}\,6} r_{\mathrm{d}\,6} \left(\frac{K+1}{K-1} r_{\mathrm{ds}\,2} || r_{\mathrm{ds}\,4} \frac{K+1}{K} \right) || g_{\mathrm{m}\,8} r_{\mathrm{ds}\,8} r_{\mathrm{ds}\,10} \tag{5}$$

$$R_{\mathrm{oIRFC}} \approx g_{\mathrm{m}\,6} r_{\mathrm{d}\,6} \left(\frac{K+M+1}{K-M-1} r_{\mathrm{ds}\,2} || r_{\mathrm{ds}\,4} \frac{K+M+1}{K} \right) || g_{\mathrm{m}\,8} r_{\mathrm{ds}\,8} r_{\mathrm{ds}\,10} \tag{6}$$

$$\mathrm{R_{oDRFC}} \approx \mathrm{g_{m\,6} r_{d\,6}} \left(\frac{\mathrm{K+M+N+1}}{\mathrm{K-M-N-1}} \mathrm{r_{ds\,2}} || \mathrm{r_{ds\,4}} \frac{\mathrm{K+M+N+1}}{\mathrm{K}} \right) || \mathrm{g_{m\,8} r_{ds\,8} r_{ds\,10}} \tag{7}$$

$$R_{\mathrm{oQRFC}} \approx g_{\mathrm{m}\,6} r_{\mathrm{d}\,6} \left(\frac{K+M+N+P+1}{K-M-N-P-1} r_{\mathrm{ds}\,2} || r_{\mathrm{ds}\,4} \frac{K+M+N+P+1}{K} \right) || g_{\mathrm{m}\,8} r_{\mathrm{ds}\,8} r_{\mathrm{ds}\,10} \tag{8}$$

Equation 8 shows the mathematical value or theoretical analysis of QRFC compared with others the output resistance increase which effect in increases the overall gain of the circuit.

We know that

$$A_{\mathrm{v}} = G_{\mathrm{m}} * R_{\mathrm{out}} \tag{9}$$

Equations 6 and 7 show the proposed work done in literature survey. According to this, they got this equation and the enhancement in gain, but in QRFC, we modified the gain stage and tried to enhance the gain more than others. For the value of K, M, N, P listed above, we take some assumption for this, $g_{\mathrm{m6}}\, r_{\mathrm{d6}} = g_{\mathrm{m8}}\, r_{\mathrm{d8}}$, $r_{\mathrm{ds10}} = r_{\mathrm{ds2}} \| r_{\mathrm{ds4}}$. Due to this, the output resistance is higher than others. Which effect on reduced the bias current from the driver transistor and bottom-most transistor which help to enhance the performance of the QRFC circuit. Due to change in the current shunt circuit which effect on the overall circuit performance. We reuse the current source more times which effects the overall Gm (Transconductance) of the circuit, which is also modified because of reusing and splitting the driver transistors. The effective transconductance is given by,

$$G_{\mathrm{mQRFC}} = [1 + \{2[K(M(2N+1) - (M+N+P+1))]\}/K + M + N + P + 1] \tag{10}$$

Equation 10 shows value of G_{m} changes accordingly with the current source reusing. Which will increase the overall gain of the system. While using the current shunt sources more times, the output resistance increases in large extent which will help to increase the overall GBW product. Due to large GBW product which effect on the settling time, but QRFC settling time is still good compare with other structure.

The proposed method QRFC has a very high gain and gain bandwidth frequency but it also shows the better linearity in closed loop and better input referred noise and figure of merit (FOM) with highly stable pole-zero location, because of high gain and GBW we have to compromise with the phase margin. Due to this, phase margin reduction is more as compared to FC, RFC, and others, but the achievable phase margin is still sufficient for well performance of transient response with lower settling time. Certainly, phase margin of conventional FC is very high, and due this, we get slow step response, but we focus on gain and GBW. The proposed structure of QRFC is shown below:

Figure 3 shows the actual schematic of QRFC on virtuoso. The output stage is similar to all other OTA's.

For slew rate of OTA is denoted as SR_{QRFC} and given by following relation,

$$SR_{QRFC} = I_{BIAS}(I_{10})/C_L \tag{11}$$

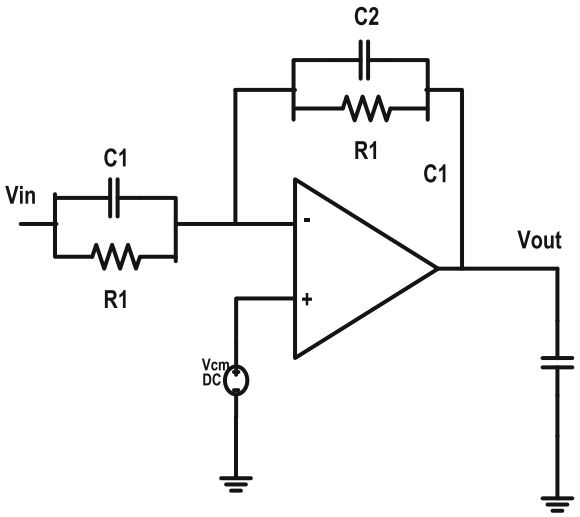
Figure 3 shows the proposed structure of QRFC. As Compared with the FC and RFC, the current source recycle many times to enhance the performance as the FC and RFC the current equally pass through the input and output stage but here the splitting the transistor four times which draws different current, according to bottom-most transistor. The bias current reduces from the input branch, and the bottom transistor works in triode region to limit the current which help to improve the overall output resistance. The transistor M_8 draws current less than Itail/2 which effects slew rate.

Some of the transistors are working in subthreshold region which has negligible effect of small signal variation. The current variation from the driver transistor depends upon their ratio which differently draws current. Transistors M_{3a} and M_{4a} draw more current which add small signal as well as current coming from source-side call I_{bias} which add in Node A and Node B. Due to this transistor M_{3a} and M_{4a} draws more current. Which result the overall output resistance increases.

4 Simulation and Results

For fair comparison between all the OTA's like FC, RFC, DRFC, QRFC they are design by using the value of K, M, N, P with take care of power and area budgets. We perform all the test on QRFC on virtuoso using 0.18 nm technology. According to test performance, it shows the following result. By performing all tests, it shows the QRFC structure which enhances the gain and GBW with greater stability.

Fig. 4 Unity gain amplifier



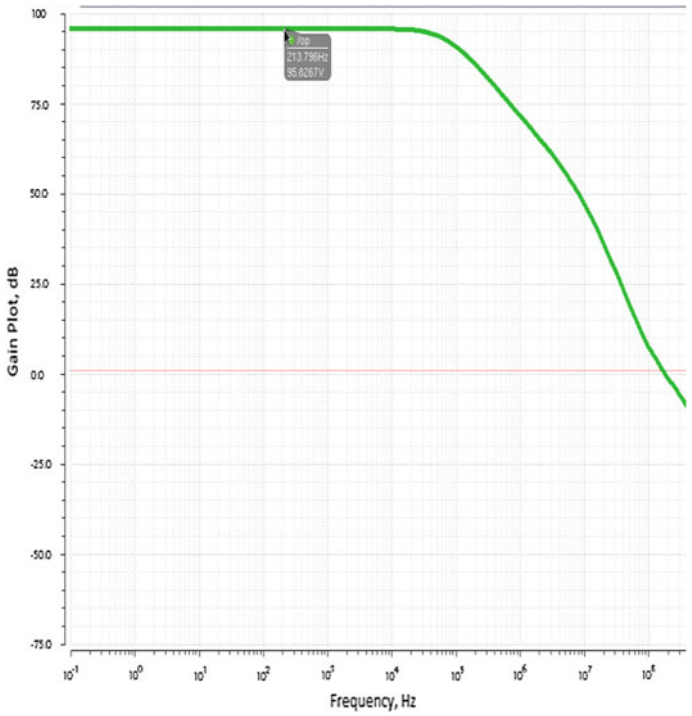


Fig. 5 Gain plot in dB of QRFC

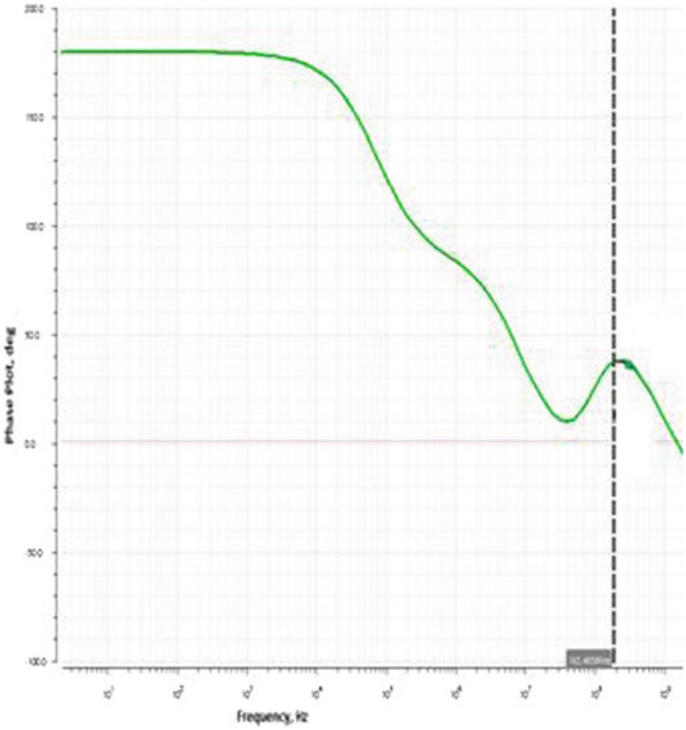


Fig. 6 Phase plot of QRFC

Figure 4 shows the closed loop test for all OTA's which show the system performance. All the three amplifiers are used as unity gain amplifier and perform test. Figure 5 where $C_1 = 1$ pf, $C_2 = 5 - 8$ pf, $R_1 = 600$ KΩ.

Figure 5 shows the gain plot obtained in dB which shows the exact gain of the QRFC. A DC gain enhancement will be obtained.

By using this quadruple recycle folded cascode OTA. Also the output resistance enhances because of the increase in the output impedance of M_{3a} and M_{1a} which helps to increase this overall transconductance of QRFC stage. Due to this, there is an increase in gain of amplifier with larger extent.

Figure 6 shows the phase plot which nearly equal to 40°. It decreases due to high gain.which shown in Fig. 5 the maximum gain obtain due to this proposed method is 95 dB which better as we compare with other OTA's, but as we go for increasing the gain of an amplifier as high as much possible we have to compromise with phase margin. For operation amplifier, this much phase margin is sufficient for working.

Figure 7 shows the transient response of the QRFC. From this, we know the voltage swing obtained at the output is very high, nearly equal to 1 V which is good for high swing application. Most of the application like bio-medical used in medical

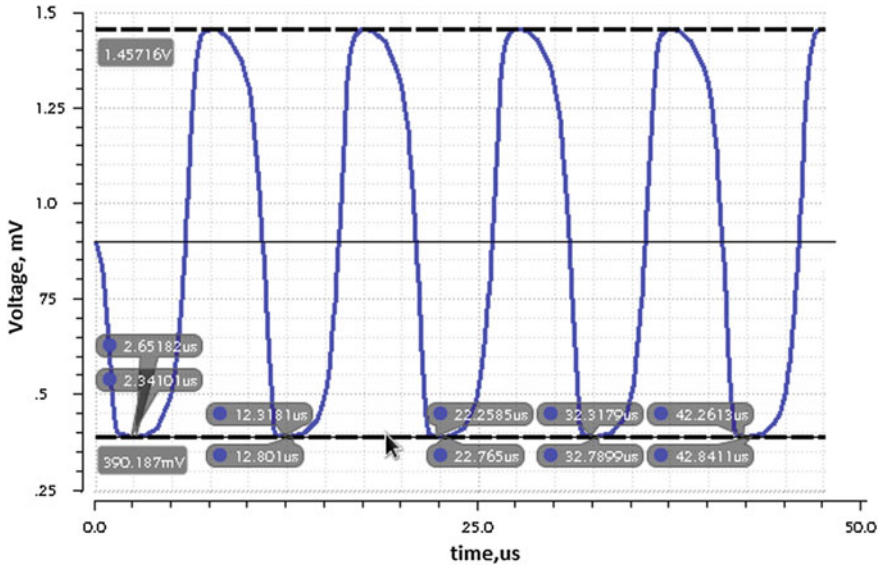


Fig. 7 Transient response of QRFC

Table 1 Performance summary of FC, RFC, DRFC, QRFC

Parameter	Conventional folded cascode (Xiao Zhao method)	Recycle folded cascode (Xiao Zhao method)	Double recycle folded cascode (Zushu Yan) Method	Proposed method quadruple recycle folded cascode
Supply voltage (V)	1.2	1.2	1	1.8
Bias current (μA)	110	110	800	200
Capacitive load (pF)	8	8	10	0.5
DC gain (dB)	71.2	79.5	54.5	95.82
GBW (MHz)	12.5	25.4	203.2	182.81
Phase margin (deg)	79.3	76.5	66.2	40.08
Average slew rate (V/μs)	5.8	13.4	84.1	78.4

field application, industrial instrumentation application which require large gain with high gain bandwidth frequency for this application QRFC play major role. From Table 1 we compare with other OTA's QRFC is high gain OTA with good GBW frequency and voltage swing. This enhancement is obtained due to recycling the current shunt source more time.

5 Conclusion

A QRFC operational transconductance amplifier shows greater significant performance over all existing OTA's FC, RFC, DRFC, etc. It enhances the overall gain up to 95 dB which is quite large as compared to others. By recycling the current source of the input stages of DRFC more times, we enhance the effective gain and GBW of OTA with less power budget. Due to this there a is reduction in phase margin but is still enough for operating.

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Nondestructive Read Circuit for Memristor-Based Memories

Marreddy Guru Sai Prasad Reddy and V. Ravi

Abstract Background: Memristor is a two-terminal passive nanodevice whose resistance (conductance) is a function of the past current flow. It is nonvolatile in nature and stores the binary data in the form of resistance. Its compatibility with the existing CMOS memory peripherals makes it interesting in the field of memory design. High density memories are realizable with the use of multilevel crossbar array of memristors. To write data into the memristor are as simple as to apply a DC bias. But reading in a similar trend would yield the loss of data. Various solutions based on AC bias, etc., have been proposed earlier. **Methods/Statistical analysis**: This paper explains a nondestructive read circuit which does not require an AC bias scheme. The proposed technique uses memristor as a feedback element in the noninverting operational amplifier. Hence, the resistance of the element is not much affected due to read operation. This makes the circuit more stable and nondestructive read operation. **Findings**: As the proposed circuit reads the content of the memristor memory without disturbing the content of the cell, it avoids refreshing or restoration of the memristor content after each read operation. By that, it improves the speed of the memory access and reduces the power dissipated. **Application/Improvements**: As the memristor memories support multilevel data storage, the proposed circuit can be modified to perform nondestructive read the content of multilevel memristor memories.

Keywords Memristor · Resistive random access memory · Nondestructive read circuit · Nonvolatile memory

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1 Introduction

Since the invention of an integrated circuit in 1960, the chip density kept on increasing till date. This increase in chip density gave an upper hand for the high performance system developers in incorporating more processing elements and huge memory on chip. Gordon Moore, the co-owner of Intel in 1965 predicted this growth of twice the chip density in every 18 months known as Moore's law. This growth has been possible due to the miniaturization of the device [1]. But the miniaturization of MOS devices has reached its saturation as further miniaturization is not possible due to the growing second-order consequences. Thus, there exists an immediate requirement for a novel device which can be scaled beyond 10 nm. The existing technologies such as SRAM, DRAM, flash trap charge in MOS transistors to store data. These technologies are aggressively scaled down for the past 25 years for improved chip density. But further scaling is not possible due to the increase in bit error rate [2] and decrease in write endurance [3]. Write endurance determines the maximum number of write cycles a memory accepts before it goes unreliable. These charge trap technologies are to be replaced by the emerging resistance-based technologies through which nonvolatile memories can be built. These memories are classified under the resistive RAM type. A similar technology to that of RRAM known as phase-change memory (PCM) exists where the resistance is varied by the change in state from polycrystalline to amorphous through the applied heat. Resistive RAM (RRAM) is one such technology which can achieve higher density and lower power compared to the existing technologies [4]. Use of devices such as memristors which have the capability to be scaled beyond 10 nm and compatible to the existing CMOS technology solves the problem.

Memristor-based RRAM structure contains memristor cell array at the top. Each cell is located at the crosspoint of the nano-width metal wires. This feature helps to build a low power and high density memory array.

The bottom layer of the memristor-based RRAM structure contains the CMOS-based circuits. The processing elements and peripherals are located at this layer. The middle layer or the sandwich layer which connects memory cells to the CMOS circuits is the CMOS-to-Nano Vias (CNVs). Thus, a three-dimensional chip is to be realized constituting the memristor-based memory cells at the top, CNVs in the middle, and CMOS-based peripheral circuits or other related circuits at the bottom.

Besides these advantages, memristor-based memories also suffer from disadvantages such as destructive read, sneak path current in crossbar array, etc. In this paper, we present a nondestructive read circuit for memristor-based memories. The section that follows briefly explains the write and read operations of a memristor. Section 3 deals with the existing nondestructive read circuit, Sect. 4 explains the proposed circuit followed by the simulation results in Sect. 5.

2 Memristor Write and Read Operations

2.1 Write Operation

To perform write operation, V_{WRITE} signal is applied across the memristor as shown in Fig. 1a. To write logic-1, a positive voltage V_A is applied as V_{WRITE} signal for a duration of t_{W1}. Due to the applied positive potential, dopants drift from doped region to un-doped region. Thus, the resistance of the memristor decreases to R_{ON}.

To write logic-0, a negative voltage-V_A is applied as V_{WRITE} signal for duration of t_{W0}. Due to the applied negative potential, the dopants drift from un-doped region to doped region.

Thus, the resistance of the memristor increases to R_{OFF}. Figure 1b shows the V_{WRITE} signal patterns for write-1 and write-0 operations. The amplitude and duration of V_{WRITE} are critical, since low amplitude or short duration may lead to weak write and thus push the device to undefined region [2].

2.2 Read Operation

Bench setup to perform a read operation is shown in Fig. 2. The V_{READ} signal is applied at the positive terminal of memristor. The negative terminal is connected to the noninverting terminal of the comparator.

Resistor R_X drops a voltage V_X at the noninverting terminal. The remaining two resistors form the voltage divider network. They present a reference voltage V_{REF} at the inverting terminal. The comparator compares the two signals and produces output accordingly.

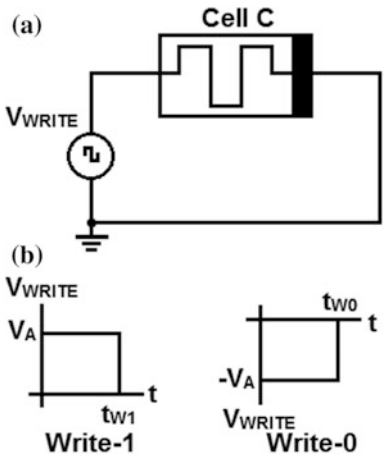

Fig. 1 **a** Write operation bench setup. **b** V_{WRITE} pattern

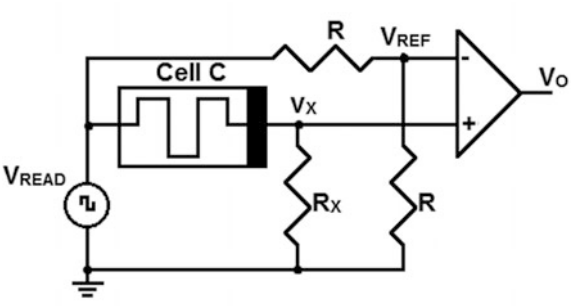

Fig. 2 Read operation bench setup

When a positive voltage is applied as V_{READ} signal for a small duration, current flows through the memristor. The amount of current flow depends on the present state (resistance) of the memristor. Based on the amount of current, resistor R_X drops voltage V_X at the noninverting terminal of comparator. The comparator compares V_X with V_{REF} and produces output accordingly.

But during the read-0 operation, the state (resistance) of the memristor alters as shown in Fig. 3a. Thus, the read operation is destructive. The section that follows explains the nondestructive read circuits.

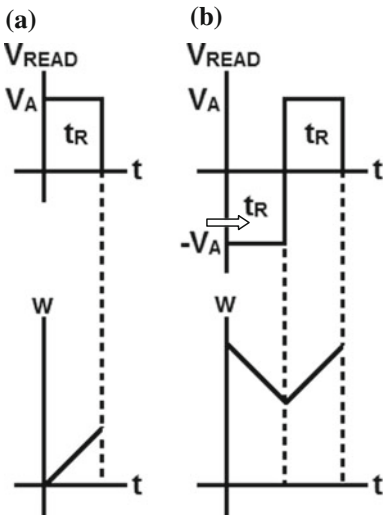

Fig. 3 V_{READ} pattern and memristor internal state *w* **a** destructive **b** non-destructive

3 Nondestructive Read Methods

To read is not as simple as a write operation. To read the internal state, certain voltage is to be applied in order to perturb the state. If carefully not designed, it may kill the data after repetitive read operations. As in Fig. 3b, a negative followed by a positive pulse, each of width t_R and amplitude $|V_A|$ is applied across the memristor (V_{READ}) in order to sense the internal state and recover the state back to the original state [5]. AC bias scheme is another similar nondestructive read approach which requires biasing circuitry which makes the read circuitry complex. Alternating current helps in performing the nondestructive read operation [6].

The positive pulse applied after the negative pulse fails to restore the state accurately due to the following reasons.

(a) Mismatch in the duration or amplitude of positive pulse and negative pulse.
(b) The durations of write-0 and write-1 are not equal due to the nonlinear I–V characteristics of memristor.

Unlike the sense and restore using negative pulse followed by positive pulse, another nondestructive scheme based on diode is proposed in [7]. Figure 4 shows the nondestructive read circuit using diode. Memristor M_0 operates in high resistance state and acts as a load resistor. The reverse direction of M_0 ensures no current flow through it, and thus, its state does not alter. The use of memristor in place of conventional resistor offers advantages such as less area, low power consumption, etc.

During the read operation, a positive pulse is applied at V_{READ}. If the memristor stores a logic-0, i.e., offers high resistance, then a large voltage drops across the memristor, and thus, the voltage V_D is small. The diode goes off since the voltage V_D is lower than its threshold voltage and does not allow any current flow.

If the memristor stores a logic-1, i.e., offers low resistance, then the memristor drops very small voltage and voltage V_D almost equals V_{READ}. The diode turns on since the voltage V_D is higher than its threshold voltage and allows a finite current flow. In this case, V_{READ} drops negligibly at memristor, diode, and appears at the output V_O.

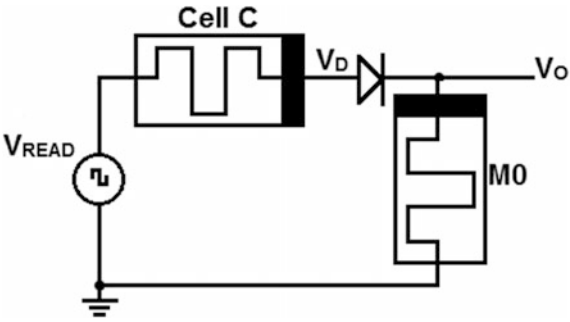

Fig. 4 Diode-based nondestructive read circuit

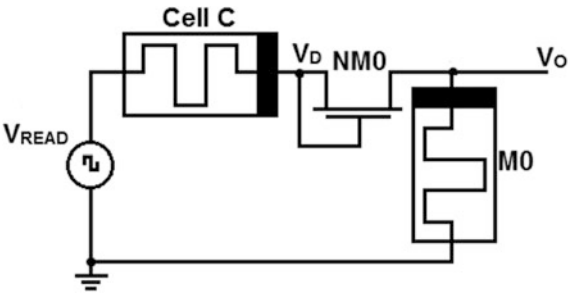

Fig. 5 Modified nondestructive read circuit

In neither of the read cases, the state of memristor is altered, and thus, the operation is termed nondestructive. The threshold voltage of the diode is critical for the nondestructive read circuit. But use of PN junction diodes results in allowing a leakage current in the order of nA. Use of transistor in diode-connected configuration (shorted drain and gate) offers very high resistance and thus very low reverse leakage currents. Figure 5 shows the modified nondestructive read circuit. The transistor NM0 is operated either in cut-off or saturation.

The section that follows explains the proposed nondestructive read circuit.

4 Proposed Nondestructive Read Circuit

Figure 6 shows the proposed nondestructive read circuit. The op-amp is operated in the noninverting configuration. The memristor is connected as the negative feedback element, i.e., the memristor is placed between the output and the inverting input terminals of the op-amp. Reference voltage V_{REF} is applied to the noninverting input.

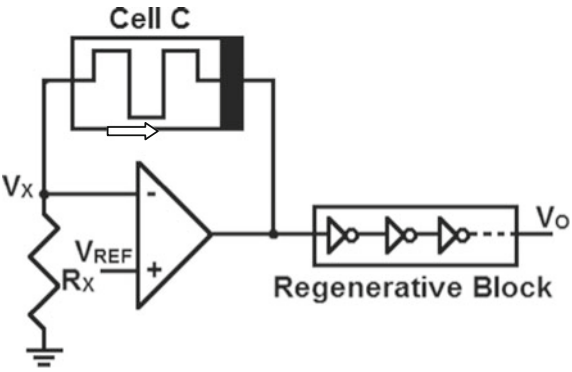

Fig. 6 Proposed nondestructive read circuit

Assuming ideal op-amp (infinite open-loop gain), the closed-loop gain purely depends on the externally connected passive components (resistor and memristor). Though the negative feedback reduces the gain from infinite (ideal) to $1 + (R_C/R_X)$, it makes the circuit deterministic and stable. Where R_C is the resistance of the memristor and R_X is $(R_{ON} + R_{OFF})/2$.

The output voltage depends on the reference voltage V_{REF}, R_X, and R_C. Since V_{REF} and R_X are constants, output voltage is a pure function of R_C (memristor state). For each different memristor resistance (internal state), a different output voltage level (multilevel) appears.

The output of op-amp feeds the regenerative block. Regenerative block consists of chain of odd number of CMOS inverters. The multilevel voltage levels are pushed to either of the supply rails due to the regenerative property of CMOS logic. V_{REF} determines the match of the op-amp output noise margin to the input noise margin of the regenerative block. The op-amp output voltage is directly proportional to the resistance of memristor. Odd number of inverters brings up the required inverse relation.

The nondestructive nature of the proposed circuit exists due to the fact that no current flows through the memristor in forward direction.

5 Simulation Results

All the simulations are carried using the Cadence Specter. gpdk180 library and Verilog A model for memristor are used. Linear ion-drift model with Biolek window function incorporated to limit the internal state changes to the boundary condition (i.e., device limits) is considered. The Verilog A model published in [8] is used for the simulations. The device specifications are: $D = 10$ nm, $R_{ON} = 100\ \Omega$, $R_{OFF} = 200{,}000\ \Omega$.

Parametric analysis is performed by varying initial internal state w from 0 to 1 (i.e., 0–10 nm). Figure 7 shows the waveforms for the parametric analysis of the proposed nondestructive read circuit. Multilevel voltage outputs each corresponding to each of the initial internal state are produced as the output of op-amp. The regenerative block produces the perfect logic levels as shown in Fig. 7. The simulation is run for 30 ns (continuous read operation), and as can be seen, the internal state is hardly disturbed by 0.0025 nm. It proves the nondestructive nature of the proposed read circuit.

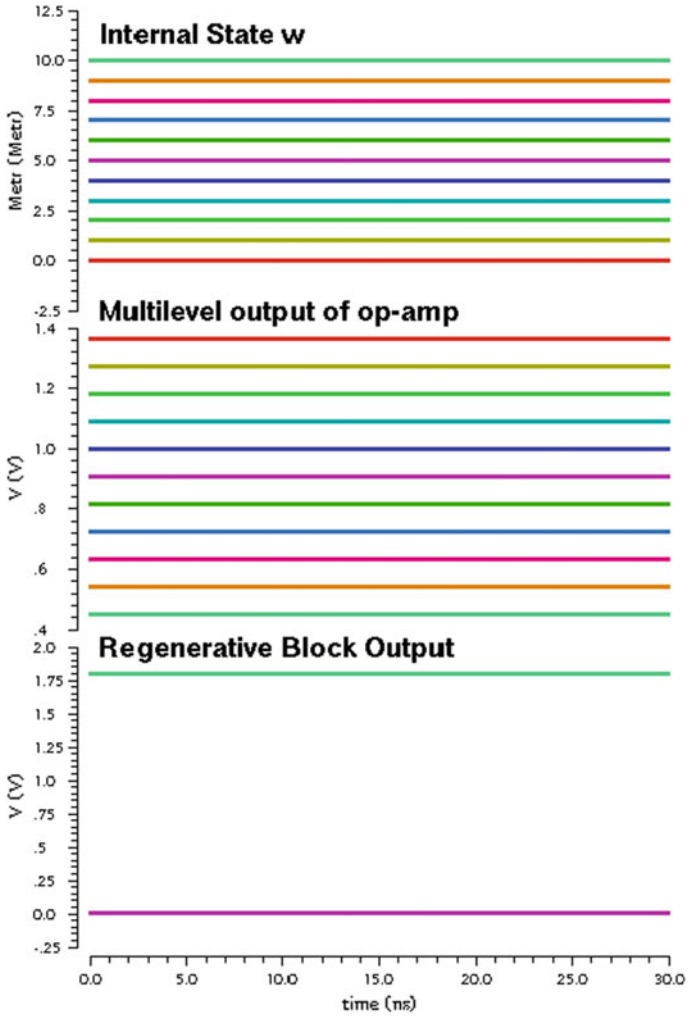

Fig. 7 Parametric analysis of proposed circuit with internal state *w* varied from 0 to 10 nm

6 Conclusion

In this paper, the existing nondestructive read methods are discussed and a new circuit is proposed. The proposed design hardly alters the resistance of memristor. The circuit can also be used to read the multilevel memristor cells.

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A Built-in Self-Repair Architecture for Random Access Memories

Sanjay Patnaik and V. Ravi

Abstract Objectives: Faults in the random access memories have been a major cause of concern with increase in technology. Built-in self-test technique is generally used to detect the faults in memories, and built-in self-repair (BISR) technique has been widely used to repair the memories. This paper discusses the configurable BISR (CBISR) technique for repairing random access memories with variable sizes and redundancy structures. An effective redundancy analysis method is proposed to replace defective cells. **Methods/Statistical analysis**: In this paper, stuck-at faults basically the stuck-at 1 (SA1) fault are detected and a built-in self-repair (BISR) architecture for the random access memories mainly for SRAM is designed and implemented on Cadence Virtuoso-64 tool in 180 nm technology. **Findings**: An efficient method to test and repair the stuck-at faults by redundancy. The redundancy method repairs the faulty memory with a fault-free one using a redirection mechanism. **Application/Improvements**: Better coverage of stuck-at faults and repair of the faulty memory.

Keywords Built-in self-repair (BISR) · Static random access memories (SRAMs) Stuck-at faults

1 Introduction

The random access memories (RAMs) occupy a major proportion of the chip so they are also more reclined toward manufacturing error. The errors may be due to stability or due to weak interconnects and transistor defects in the SRAM. These cause a weaker bit lines or word lines which are one of the reasons for the stuck-at faults in memories. The BISR configuration shows a method to repair a faulty

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SRAM cell [1]. Design and development of the circuit are done on Cadence Virtuoso-64 on 180 nm technology. The six transistor configurations or 6T is used as a memory cell in the 4 × 4 memory array to be considered as circuit under test (CUT).

Test of a logical circuit means assigning the required test inputs and patterns to the circuit and comparing it with the normal mode of the circuit [2]. In general, we have three types of testing procedures for the random access memories, namely micro-coded BISR, programmable BISR, hardwired BISR. As per the survey done on the above methods, it is found out that the hardwired BISR consumes lesser time [3]. The fault detection in this paper deals with the storing and retrieving of data caused due to stuck-at faults. The parallel in parallel out register (PIPO) acts as a pattern generator which is given to fault activator to activate the spare memory's bit and bit bar lines.

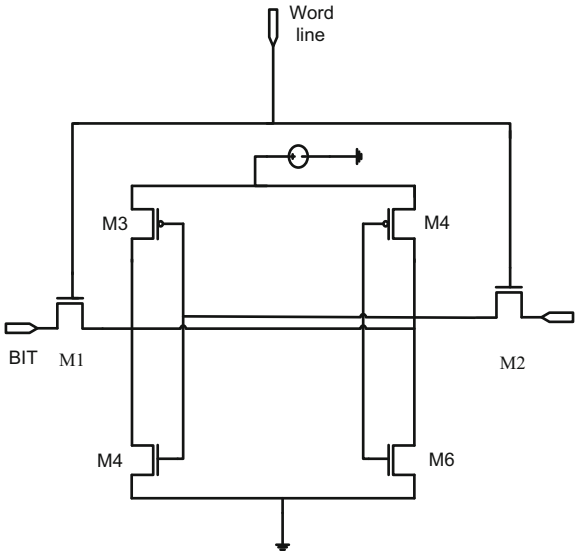
One of the methods like the triple modular redundancy is a good approach, but it is not expedient as it has an excessive overhead area 4. The CUT used here is a six transistor SRAM which is most generally used SRAM. An SRAM generally has two access transistor named here as M_1 and M_2, two load transistors M_3 and M_4, two driver transistors M_5 and M_6. The access transistors are used to access the circuit, and it is connected to the word line which is used according to the read 0 or read 1 operation. The pattern generator is a parallel in parallel out (PIPO) register that generates input to be given to the spare row 6. The BISR scheme in the paper enlightens a new method by use of a spare memory used to give the perfect output instead of defective or faulty output. It repairs the input through the repair mechanism which is discussed in the paper. The BISR configuration reduces the access time penalty. The fault activator reduces the intricacy of the hardware in the BISR circuit. The BISR method as in this paper uses redundancy. Redundancy literally means using of the spare memory that may be either a row or a column to be redirected such that it replaces the faulty memory with a spare one. Altogether it helps in increasing the manufacturing yield of memory.

2 Proposed Methodology

The proposed architecture has a spare memory which is activated when there is a fault detected when a test procedure is carried out. This BISR scheme can be utilized for the manufacturing time reduction as it provides us an approach which is equally efficient to deal with the fast and shrinking technology, and may be used with the future nanoelectronic technology.

The paper is organized as follows. In Sect. 3, we will discuss the 6T-SRAM, Sect. 4 about the types of faults in SRAM. Section 5 discusses the design of BISR and the types of faults, Sect. 6 about functioning of BISR and Sect. 7 about working of BISR.

Fig. 1 SRAM cell



3 Review of SRAM

SRAM is a volatile semiconductor which is used to either store at 0 or at 1. It is bi-stable latching circuit which is generally used to store bits. On comparing it with the dynamic random access memories (DRAMs), we do not need a capacitor for refreshing it on each cycle in the SRAM7. The access transistors keep the direction of the current flowing in either of that of 0 or 1. The 6T-SRAM is the improvement of the 4T-SRAM, so the resistance/load is replaced by PMOS called as load transistors M_3 and M_4. The driver transistors are the one in which we have NMOS transistors M_5 and M_6. The load transistors M_3 and M_4 with the M_5 and M_6 together form a cross-coupled inverter which is accessed by M_1 and M_2 as shown in Fig. 1, an SRAM is called as the self-inflicting storage cells, and the benefit of the 6T-SRAM is that it endeavors better electrical realization of the noise, speed, standby current than that of that of 4T-SRAM.

4 Failures in SRAM

The types of fault that may occur in the SRAM are of many types from that of the stuck-at faults, write failures, read failure access failure, stability failure, storage, and retrieval faults that are mainly due to the transition. In this paper, as discussed above, we will discuss the stuck-at faults that cause storage faults and retrieval faults. The storage and retrieval faults in a SRAM cell occur as and when the data that which are to be written and read by the sense amplifier have stuck-at values. If

the SRAM cell has a stuck-at faults are either stucked at '0' or 19 at the bit lines or word lines due to shorting of the interconnects or transistor defects the data is not stored. Hence, it becomes a tedious process for a test engineer to repair the defects after the burn-in test and to start everything from the scratch 10. The BISR scheme develops a method to repair the faulty memory by using the redundancy to repair the faulty memory 11.

There are basically eight parts of the circuits which are used in this BISR scheme, they are write circuitry, decoder, CUT, up-down counter sense amplifier, pattern generator, switching circuit, and fault activator.

4.1 Write Circuitry

The write circuit consists of pass transistor logic as shown in Fig. 2 which has a word line and data as inputs. The data given are as required either 0101 or 1010. The main motive behind using pass transistor logic is that it uses a lesser number of transistors and is faster.

4.2 Decoder

The decoder used in this paper is a 2:4 decoder where the inputs are given according to the truth table. These inputs are then given to the 4 × 4 SRAM array. Figure 3 shows a schematic of a decoder consisting of two inputs and four. It is a

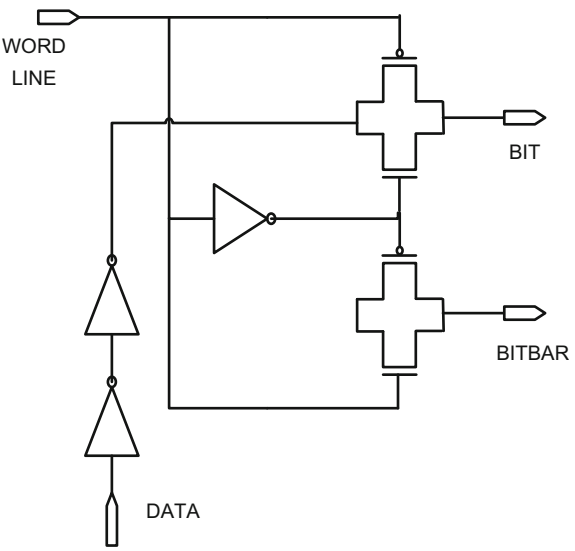


Fig. 2 Write circuitry

combinational logic circuit that converts a value of binary integer to the value of output pattern bits.

4.3 Circuit Under Test

The SRAM 4 × 4 array is the CUT or the circuit under test. The inputs of the CUT in the BISR configuration is the bit lines and word lines for the storage and retrieval of the data we need to check for any kind of faults that may occur in the SRAM cell. Then we compare the expected output with the desired output to check for any types of faults.

4.4 Sense Amplifier

The main aspect of the sense amplifier is to sense the lower-powered signals from the bit line or the bit bar line and amplify those small voltage swings to detectable logic levels 12. They can be assessed as output outside the memory. The sense amplifiers are the sole analog circuit part in the memory design where each column of a memory cell will be attached to a sense amplifier. The sense amplifier consists of the local precharge and sense enable. In Fig. 4 as the inputs are given to the bit and the bit bar for reading either a 0 or 1, the differential amplifiers amplify the small voltage signals to logic levels of 0 or 1.

Up-down counter is used in the BISR scheme to select a 0 or 1 regarded as an up or down. An up-down counter basically has two T-flip flops with arrangements of gates. The up-down counter is then connected to a multiplexer that selects a 1 or 0 with the help of select line. The up-down counter shown in Fig. 5 has inputs as up and down and outputs as OUT1 and OUT2.

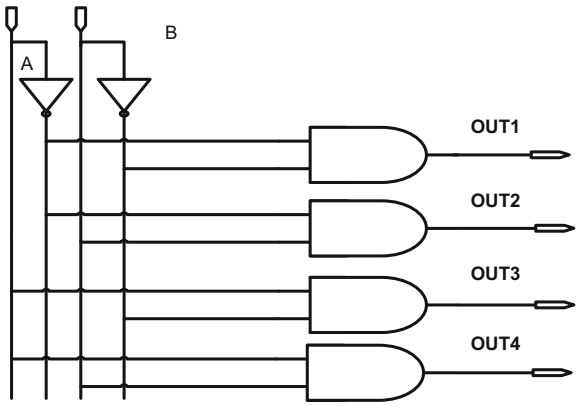


Fig. 3 Decoder used in the SRAM array

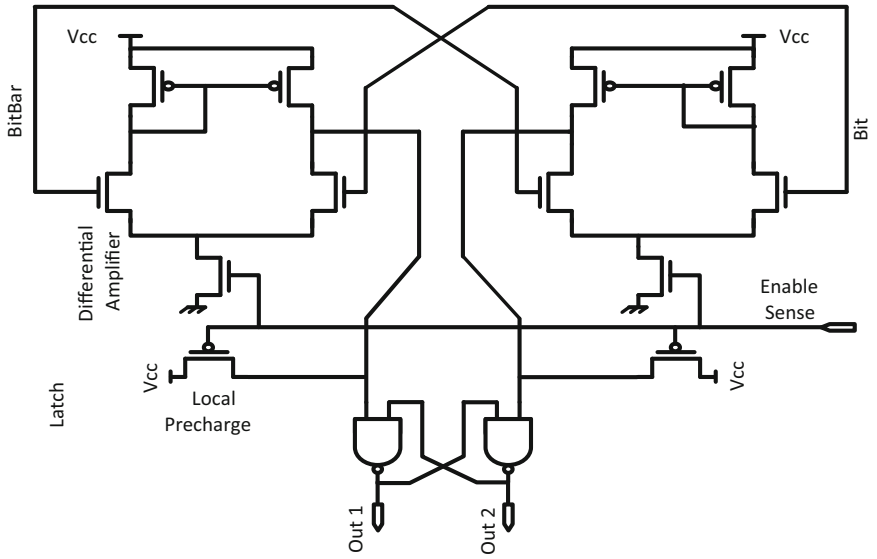
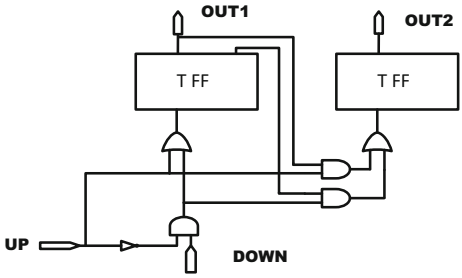


Fig. 4 Sense amplifier

Fig. 5 Up-down counter



4.5 Switches

The switches used in the circuit are used for isolating the circuit under test to the repair mechanism whenever the BIST [4] signal is made ON. The repair of the faulty memory takes place when the 4 × 4 array which is placed as a CUT and a faulty bit line given as an input depicting stuck-at faults. The data given to the spare SRAM are activated only when the switches are activated. Figure 6 shows a schematic of the switching circuit in which we have five inputs and four outputs, whenever the b_on signal is high.

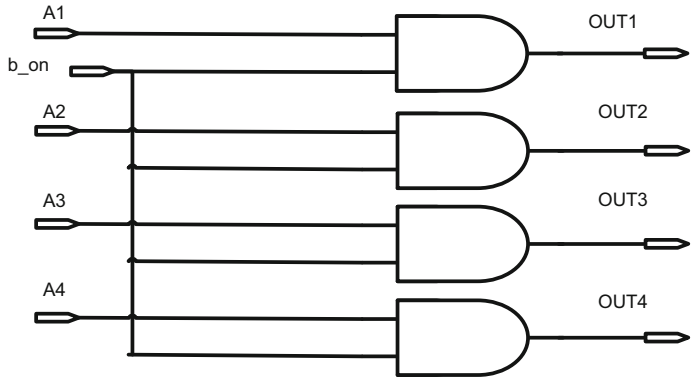


Fig. 6 Switches

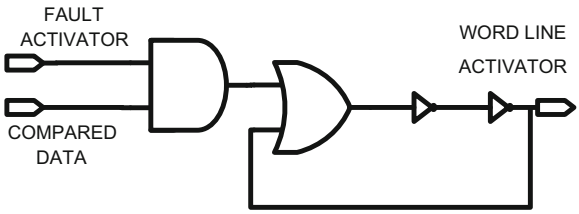
4.6 Fault Activator

The fault activator is generally used to activate the word line present in the SRAM 4 × 4 array. The fault activator mainly has two inputs, one is the fault activator and the other is the word line. The fault activator circuit consists of AND gate and an OR gate with two inverters connected back to back. Figure 7 shows the fault activator with one of the inputs given by the output of the OR gate and the other with the output of an up-down counter.

4.7 Parallel Input Parallel Output

Depending upon the usage, the registers are divided into storage register and a shift register. The test pattern generator is generally a shift register. The parallel input and parallel output (PIPO) is generally called as storage register or buffer register. The data given to the write circuitry are given through this shift register which generates pattern to be stored. The data stored are given at the falling edge of the clock. The shift register shown in Fig. 8 is the schematic representation of the register. There are inputs as D_1, D_2, D_3, D_4, and outputs Q_1, Q_2, Q_3, Q_4 is, respectively, storing data 1010 or 0101.

Fig. 7 Fault activator



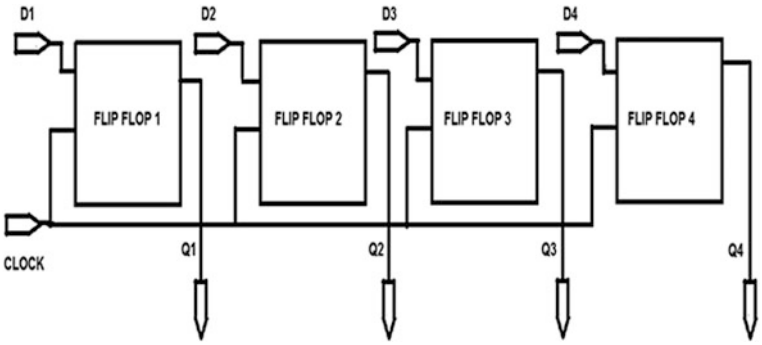


Fig. 8 Pattern generator

5 Functionality of SRAM

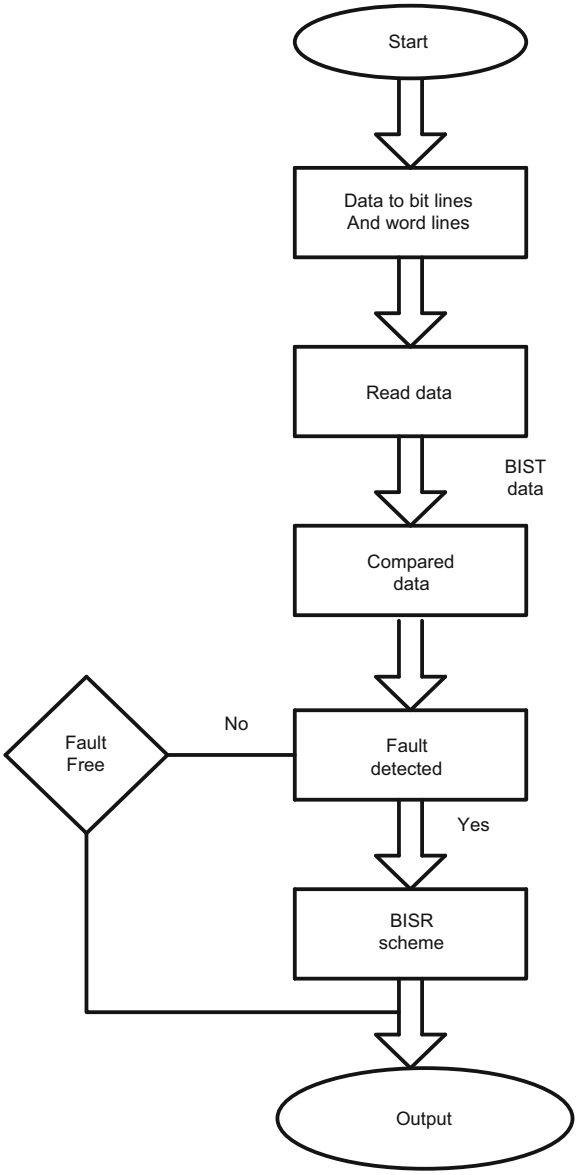
The functionality of a BISR configuration is shown in the diagram given below. The flow diagram of this BISR configuration starts with the generation of word line and data lines 13. The sense amplifier present in the circuit reads the data and is compared for the faults in the BIST [5]. The case of stuck-at 1 fault denoted as (SA1) is detected in this paper. As discussed earlier in the paper, these faults cause storage. Thus, for this fault, we use a spare memory which is fault free with presence of a fault mechanism that repairs [6] the fault by giving expected output. The flow diagram in Fig. 9 explains that if data are fault free it gives direct output, otherwise by using a spare memory [7] we will be able to get the expected output.

6 BISR Architecture

In the BISR configuration, we have a 2:4 decoder. This decoded output is given to the word line of a 4 $\times$ 4 SRAM array. The write circuitry generates bit and bit bar outputs according to the data given.

The read operation takes place with the use of a sense amplifier which is then given to a two inputs OR gate used as a comparator [8]. The stuck-at fault that occurs due to weak bit lines is compared with the correct outputs. Here we detect a stuck-at 1 fault or SA1fault. This part acts as a BIST [9] circuit which shows the types of fault present in the circuit. The multiplexer selects input of logic 1 given as output by the up-down counter. The fault activator activates the word line of the spare memory [10]. When the switch is made ON, the comparative data from the BIST [11] part and the up-down counter make up the controller part of the BIST14. The parallel in parallel out shift register also known as buffer register gives data to the write circuitry, and the data are then read by the sense amplifier for the spare

Fig. 9 BISR flow



memory. In Fig. 10, the repair mechanism starts when the fault activator activates the word line of spare memory by redundancy. Redundancy literally means using of spare memory to repair the fault and give expected outputs 15. The proposed architecture repairs the fault and gives a fault-free output as shown in the simulation results.

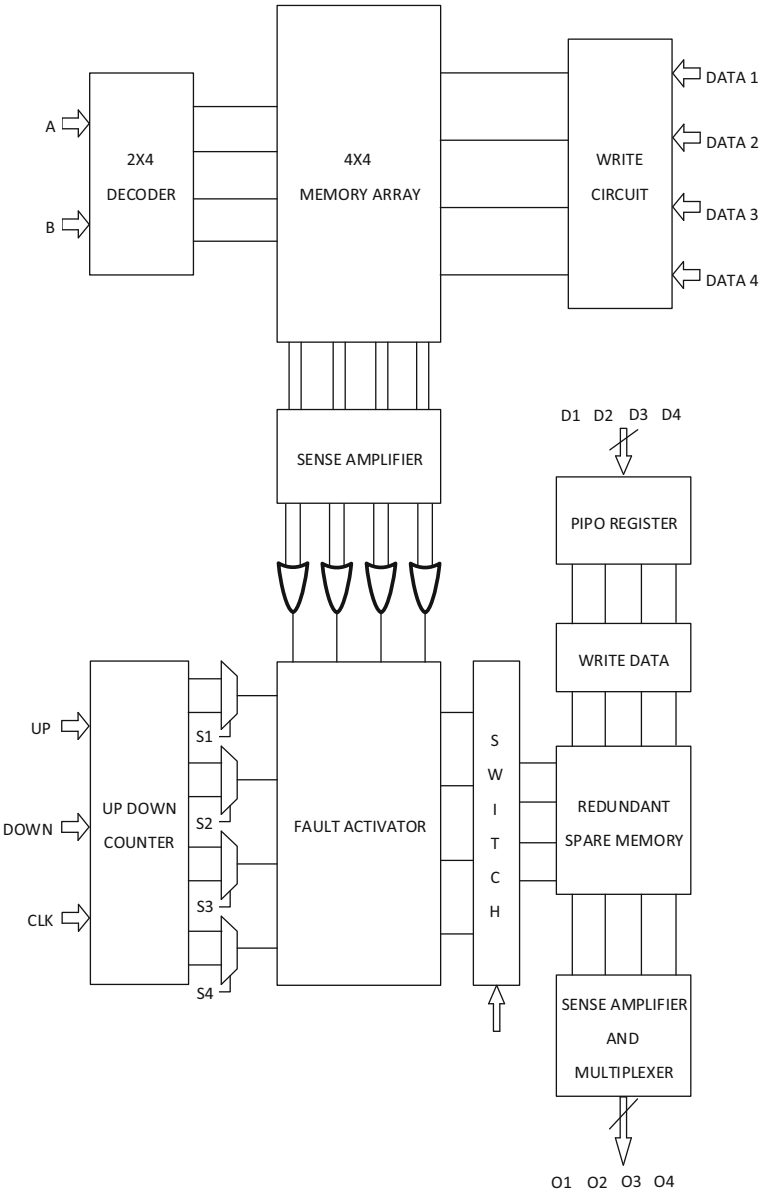


Fig. 10 Proposed architecture

7 Simulation Results

The input given to the memory array from the write circuitry is given to the sense amplifier, and the sense amplifier, as discussed above about its working, either reads a 0 or a 1. Thus, when the sense enable is high, one of the outputs reads 0 and other reads 1. The result shown in Fig. 11 proves that there is a transition of 0101in bit and 1010 in bit bar respectively.

When there is no transition that means there will be weak word line or bit lines, in other word, if the value is at stuck-at 1, it does not have any transition. Storing and retrieving of data do not occur, as a result, there will be a faulty output given to the comparator. The results shown in Fig. 12 are a faulty one as no transition is present.

This fault is further carried to the repair circuitry which gives the expected output through the BISR configuration.

The output from the sense amplifier is then given to the OR gate which is compared to detect the fault. In Fig. 13, when the error-free output is given to the memory, array can go through the burn-in test.

The storage and retrieval of data take place when there are no stuck-at faults, but if there is a stuck-at 1 fault present as shown in the Fig. 14, then the fault repair

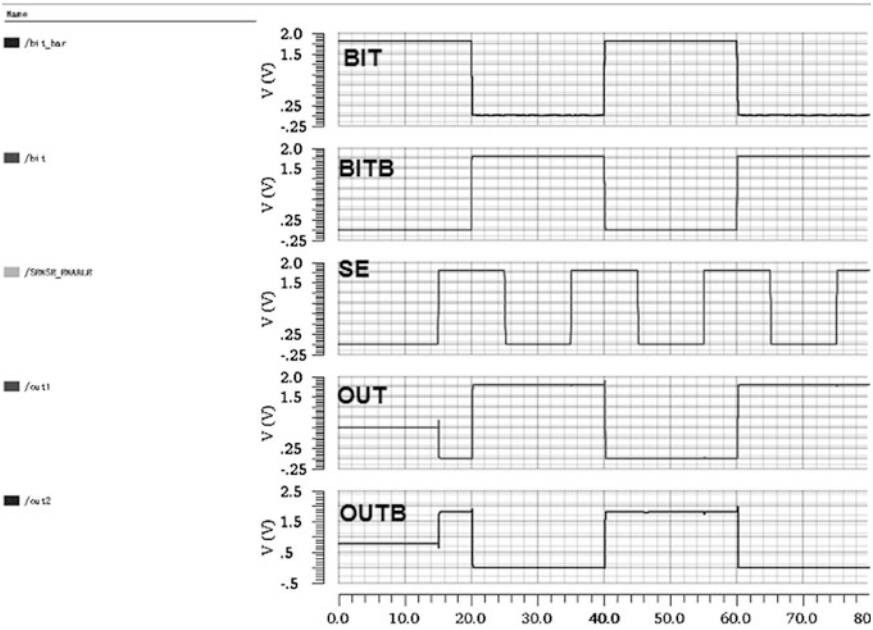


Fig. 11 Sense amplifier faulty output

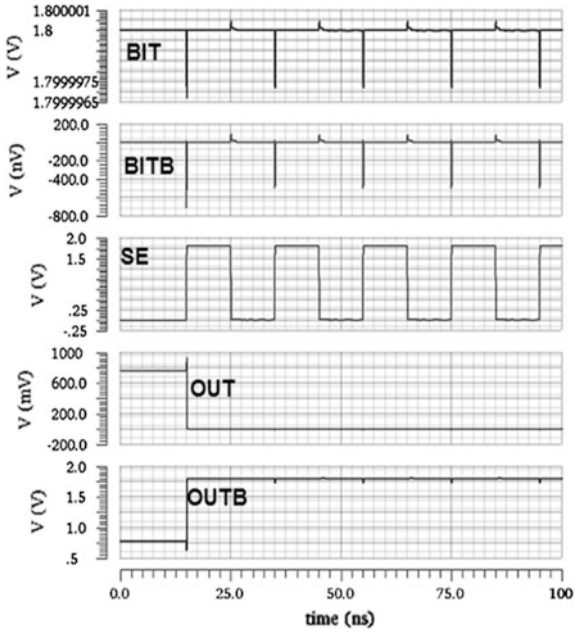


Fig. 12 Faulty sense amplifier output

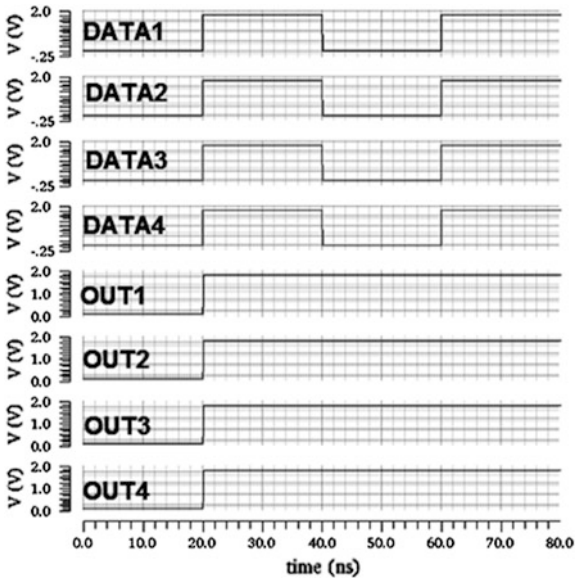


Fig. 13 Fault-free output

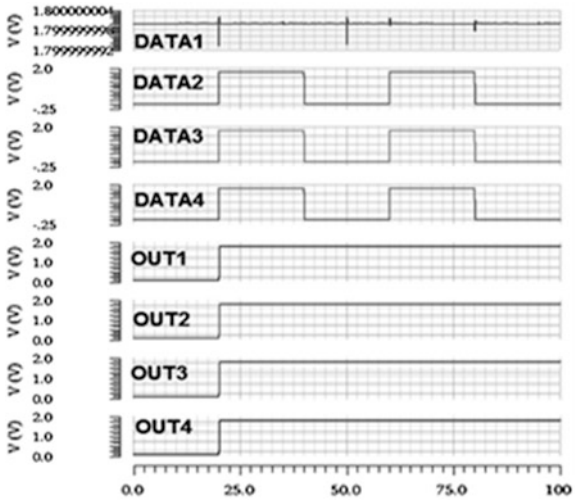


Fig. 14 Faulty output

mechanism of BISR [12] repairs the faulty memory by replacing it with a fault-free spare memory activated by fault activator. BISR scheme repairs the data and gives output similar to that of a fault-free case.

8 Conclusion

In this paper, we have analyzed the method to repair the faults in an SRAM. The stuck-at 1 fault (SA1) in built-in self-repair architecture as shown in this paper repairs faults by a method called as redundancy. This redundancy method redirects the fault-free memory to be replaced by a fault-free memory by improving the manufacturing yield.

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A Current-Mode DC–DC Boost Converter with Fast Transient and On-Chip Current-Sensing Technique

S. Sudheer Sagar and P. Reena Monica

Abstract **Objectives**: Design of a converter with high accurate feedback system is the objective of this paper. **Statistical analysis**: Design of a current-mode CMOS DC–DC boost converter with fastest settling time and less quotient current with a feedback control is presented. Efficient compensation with soft-start is used to make the quotient current low. An on-chip current-sensing circuit is introduced with less number of I/O pins for current-mode control. The design is carried out in CADENCE Virtuoso, and simulation results show successful working of DC–DC boost converter. **Findings**: The system is designed using 0.18 μm, 5 V supply CMOS technology. With wide range of loads, it provides 25 V at the output, 50 mA load current with 90% efficiency. Circuit is operated at 500 kHz clock frequency with output ripple voltage of 21 mV by using 4.7 μF off-chip capacitor and 55 μH off-chip inductor. **Improvements**: Design of converter in current-mode control with high accurate current-sensing technique increases the controllability on PWM signal. Modified OTA design helps in the fast settling of the converter.

Keywords Boost converter · DC–DC converter · Transient response
Compensation ramp · Current-mode control · Current-sensing circuit
PWM · Switched-mode power converter

1 Introduction

Power management system is the most important part of an IC in the modern technology. In particular, developments in the portable devices which are operated with batteries are more dependent on power supplies. Since they have modules

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operated with different voltage supplies, DC–DC converters play major role in the power management system.

It is indicated that DC–DC boost converter provides regulated voltage supply which is more than the voltage provided. This converter can operate in different modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM) [1]. However, these modes are limited to relatively high power consumption due to the peaking in inrush current provided by the inductor [2–4]. To minimize the inrush current, an efficient controller IC is designed for reasonably high-speed operations. However, there is a compromise on low power and high speed, which makes the controller design a difficult task.

There are two modes of controller operation for DC–DC converter: voltage-mode control (VMC) and current-mode control (CMC) [1]. CMC has higher bandwidth than VMC, in which response is low when there is an abrupt change in output. Normally, power stage in both the modes introduces two poles generated by externally placed inductor and capacitor. It indirectly works as a low-pass filter. Hence, it complicates the circuit compensation design to make the total system stable in VMC. The CMC has wider bandwidth and quick response to the abrupt changes in the output. One of the poles present nearer to the switching frequency enables the simplification of compensation design to make the system stable.

However, as compared to VMC, CMC needs one more loop for detecting inductor current to compare with error voltage. Figure 1 shows the simple block diagram of DC–DC boost converter. This converter is composed of the power stage and its controller by using feedback.

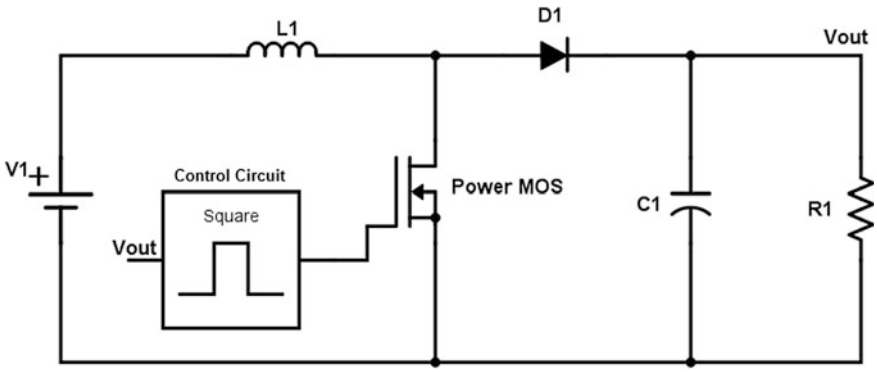


Fig. 1 Basic block of DC–DC boost converter

2 Design Issues in Current-Mode Control

In CMC, sub-harmonic oscillation is a well-known problem. When the duty cycle is more than 50%, as shown in Fig. 2 [3–5], an artificial slope compensation ramp signal is needed to solve the stability problem.

If the duty cycle ratio is more than 0.5, oscillations will be as shown in Fig. 2b. Dotted waveform shows that the inductor current deviates positively in the beginning of the cycle. But in the next cycle, it becomes negative with little increase in amplitude. For the next cycle, it becomes positive, but amplitude is increased even further. To avoid the sub-harmonic oscillations, slope of the added ramp m_r must be larger than that of half of the slope of inductor current m_l in the interval $(1 - D)T_s$ as shown in Fig. 3:

$$m_r \geq \frac{m_l}{2} \tag{1}$$

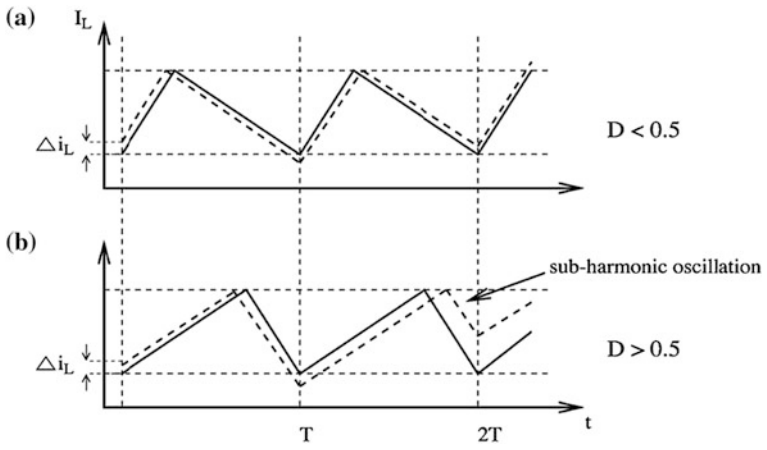


Fig. 2 Study state and oscillated inductor current waveform

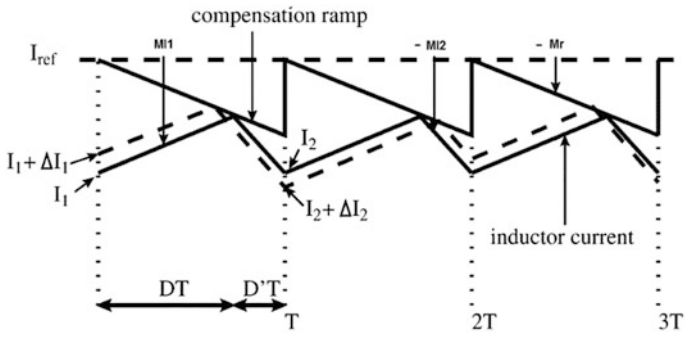


Fig. 3 Inductor current waveform with compensated ramp

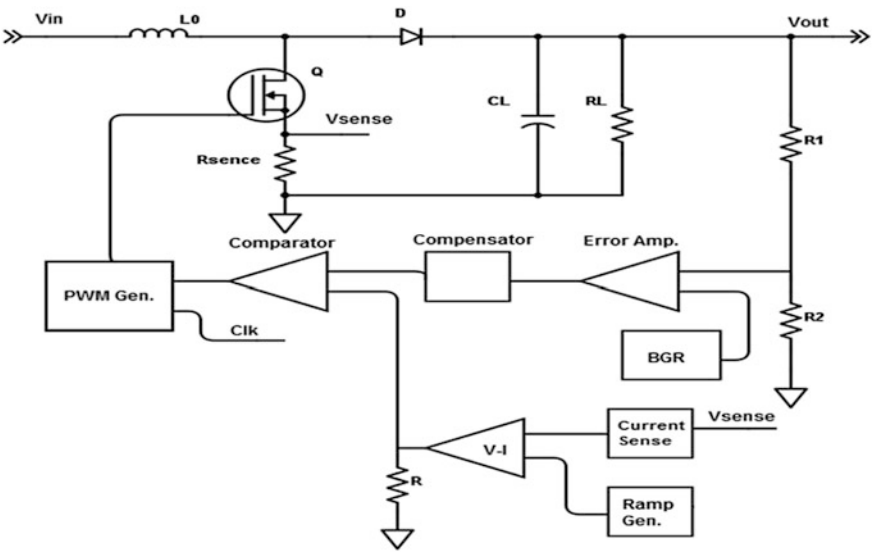


Fig. 4 DC–DC boost converter with feedback controller blocks

The compensated ramp, sensed signal, and inductor current, respectively, are shown in Fig. 3 [3].

Current-mode DC–DC boost converter topology is shown in Fig. 4. The controller has two loops: output voltage control and inductor current control. It is a simple operation where the inductor current is sensed, and whenever it reaches a particular peak, it makes the power transistor OFF. In order to maintain the regulated output voltage, the duty cycle of the pulse generated must be modulated, to supply the same voltage for various load conditions. In this paper, the converter design provides wide bandwidth with the fastest settling with less inrush current.

Current-mode DC–DC boost converter has a right half plane and two poles, in which one pole is nearer to the switching frequency. Therefore, it is approximated as one pole and one RHP zero system. The transfer function equation of the control current to the output voltage is given in Eq. (2).

$$g_{\mathrm{VC}}(s) = \frac{v_o}{i_c} = \frac{(1-D)R_l}{2} * \alpha \tag{2}$$

where

$$\alpha = \frac{\left(1 - \frac{s(L)}{(1-D)^2 R_l}\right)(1 + sR_{\mathrm{esr}C}C_o)}{\left(1 + \frac{sR_lC_o}{2}\right)} \tag{3}$$

D is the duty cycle of the PWM signal.

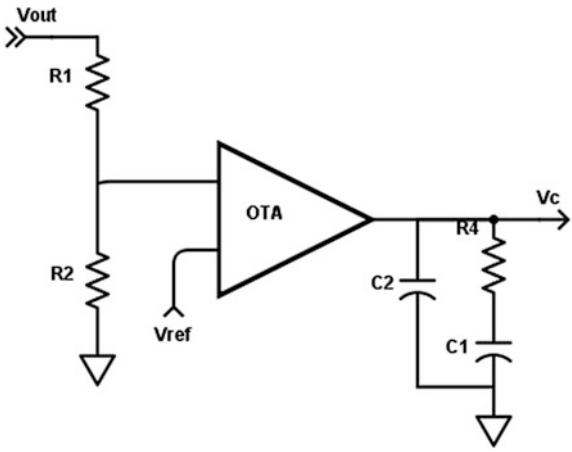


Fig. 5 OTA with compensation

As CMC has one pole lesser than VMC, the control on output voltage can be obtained using a simple proportional–integral (PI) compensation [6]. We use an operational transconductance amplifier as an error amplifier. R_1 and R_2 resistors are used as an output voltage divider. To enter into AC analysis, the ratio of these divider resistors is only the main concern. Normally, in CMC, the Type II compensation scheme is used to flatten the gain and increase the phase by adding an extra RC branch to OTA as shown in Fig. 5.

3 Circuit Implementation

This section gives information about the stage-by-stage implementation of current-mode DC-DC boost converter as shown in Fig. 4. Emphasis will be on the functionality of two loops with new OTA design, combining current-sensing signal with ramp [7, 8].

3.1 Proposed OTA

A conventional current mirror-loaded operational transconductance amplifier (OTA) is chosen as error amplifier, for better understanding of fast transient response in DC–DC boost converter.

Figure 5 shows OTA structure used with compensation for stability.

This circuit is designed using standard 0.18 µ CMOS process operating at 5 V supply. This type of OTA architecture gives wide output swing by using single stage. There is no need of a second stage unless there is a need for high gain.

Transconductance of this OTA is given as follows:

$$g_m(\text{amp}) = N * g_m(M1) = N * g_m(M1) \tag{4}$$

where N is the mirror ratio given by:

$$N = \left(\frac{W}{L}\right)_{M9} \Big/ \left(\frac{W}{L}\right)_{M10} = \left(\frac{W}{L}\right)_{M4} \Big/ \left(\frac{W}{L}\right)_{M8} \tag{5}$$

Gain:

$$G = \frac{g_m \frac{M1}{M2}}{[g_{mM10} + g_{mM8}]} \tag{6}$$

where

$$g_{mM1/M2} = \sqrt{2\mu_p C_{oX} \left(\frac{W}{L}\right)_{1,2} I_d} \tag{7}$$

I_d is the current in the biasing transistor.

The new gain curve of the proposed OTA with compensation is shown in Fig. 6. Since the multiplier ratio at output current mirror stage is about 20, current in the output stage is 20 $\times$ I_d. By increasing this ratio, we can get higher currents for fast settling, but it causes rise in the quiescent current of the amplifier. To get fast settling converter, we need more current at the output stage. To achieve that, a new

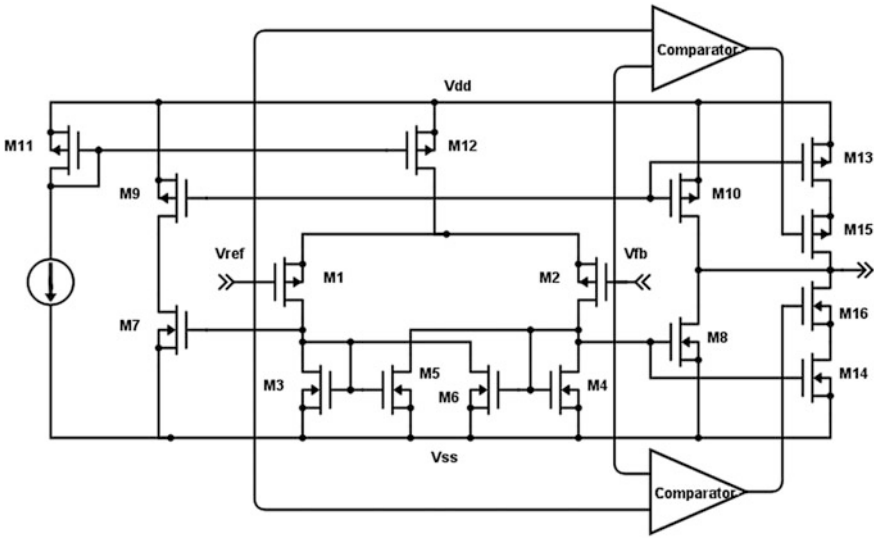


Fig. 6 OTA with extra current path

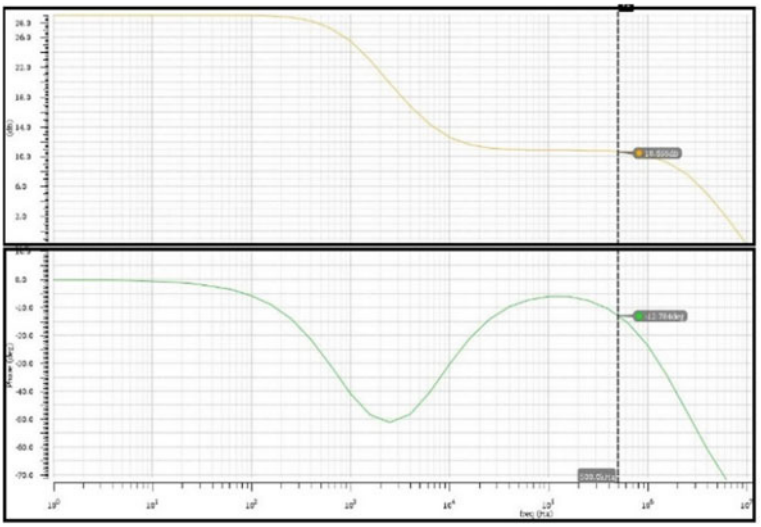


Fig. 7 Gain and phase of compensated OTA

architecture is added up to the OTA, as shown in Fig. 7, which doubles the current in the output stage. The extra transistors M_{15} and M_{16} are operated with the respective comparators PCOMP and NCOMP, which makes the circuit bigger, and there is more power dissipation. By selecting the comparator's offset effectively, power consumption can be reduced by making this extra circuit switch off after the system settles down at the particular output voltage. The graph for transconductance is shown in Fig. 8.

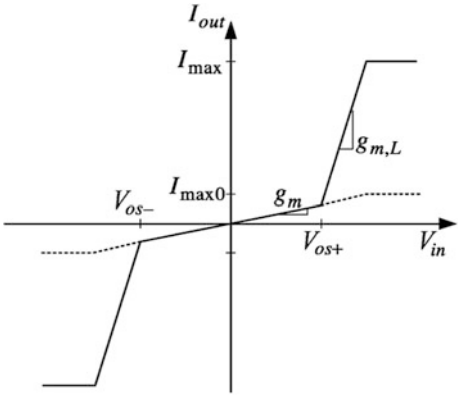


Fig. 8 Modified conductance curve

3.1.1 Compensation

In the current mode of control feedback loop, using an error amplifier is an advisable design to control the naturally occurring characteristics of the power stage. The compensation scheme adds an RC pair to flatten the gain and increases the phase in mid-frequencies. By introducing the separation of the pole and zero causes increase in the stability of the compensator, hence, the phase is increased. This compensation gives a pole near origin P_0 and a pair of pole P_1 and zero Z_1. The values of these pole and zero frequencies are decided by the sizes of the resistors and capacitors as given in Eqs. (11–13) [9, 10]:

$$f_{P_0} = \frac{1}{2\pi R_1 C_1} \tag{8}$$

$$f_{P_1} = \frac{1}{2\pi R_3 C_2} \tag{9}$$

$$f_{Z_1} = \frac{1}{2\pi R_3 C_1} \tag{10}$$

By rewriting Eqs. (8–10), we can determine the values of each component:

$$C_1 = \frac{1}{2\pi R_1 f_{P_0}} \tag{11}$$

$$R_3 = \frac{1}{2\pi C_2 f_{P_1}} \tag{12}$$

$$C_2 = \frac{f_{Z_1}}{2\pi R_1 f_{P_0} f_{P_1}} \tag{13}$$

3.2 *Current Sense*

Series-sensing resistor technique inserts a sense resistor in series with the power MOS, because the value of the resistor is known and the current flowing through the power MOS is determined by the voltage across it, as shown in Fig. 9. Select sense resistor is of very small so the power dissipation is less, for example, 50 mΩ. When power MOS is turned on, current flows through the resistor and the cross-voltage is:

$$V_{\text{sense}} = I_{\text{sense}} * R_{\text{sense}} \tag{14}$$

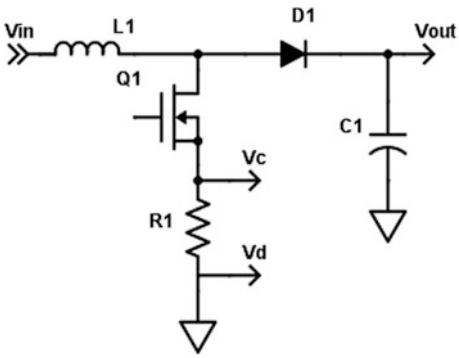


Fig. 9 Current-sensing resistor

$$V_{\text{out}} = \text{be obtained by use of a simple } I_L R_{\text{sense}} \frac{R_2}{R_3} \tag{15}$$

As $R_2 = R_3$, then $V_{\text{out}} = I_L R_{\text{sense}}$.

The novel current-sensing circuit shown in Fig. 10 uses current mirror to replace the conventional op-amp, which is less affected by the process. The current mirror works as a depth negative feedback circuit, making the voltage $V_A = V_B$. Some extra compensation current flows through transistors driving from the current mirror to make voltages at A and B equal.

Table 1 illustrates the sample error of the current-sensing amplifier.

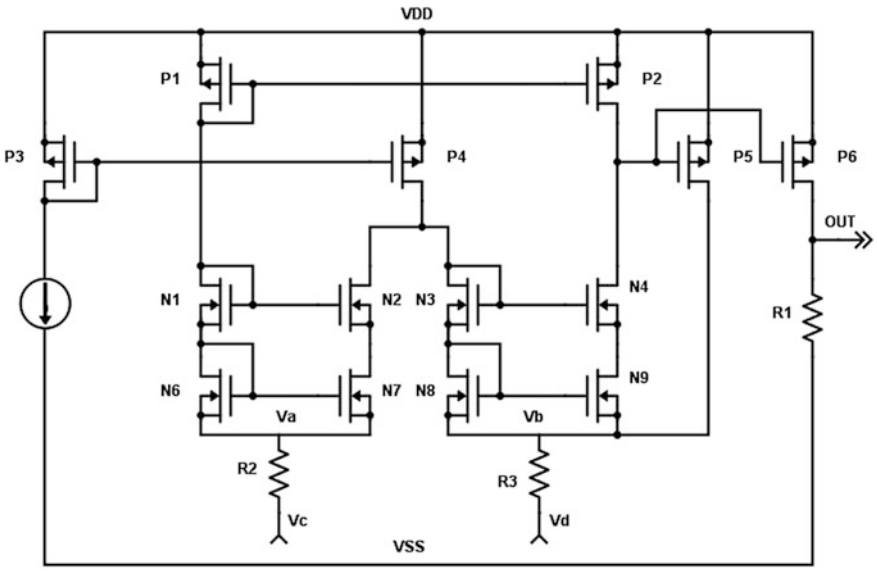


Fig. 10 Current sense amplifier

Table 1 Sensed current at 'out' pin in Fig. 10

I_L (mA)	I_{ideal}	I_{actual}	Sample error (%)
220.9	2.20	2.2563	−2.14
240.07	2.40	2.4317	−1.29
260.01	2.60	2.6189	−0.72
280.07	2.80	2.806	−0.18
300.04	3.00	2.9923	0.26
320.74	3.20	3.1856	0.68

3.3 Comparator

Comparator is needed in the DC–DC boost converter to generate a PWM signal and to generate a ramp signal. Even comparators with different offset voltages are needed in the proposed error amplifier design [5]. A source-coupled differential, single-ended amplifier with positive feedback is used to provide high gain in this design. The gain of the design shown in Fig. 11 is given by Eq. (16):

$$A_v = \sqrt{\frac{\mu_p \left(\frac{w}{L}\right)_2}{\mu_n \left(\frac{w}{L}\right)_4}} * \frac{1}{1-\beta} \tag{16}$$

where μ_p and μ_n are the mobilities of the hole and electron, respectively.

β is the feedback factor given by Eq. (17):

$$\beta = \frac{\left(\frac{w}{L}\right)_6}{\left(\frac{w}{L}\right)_4} \tag{17}$$

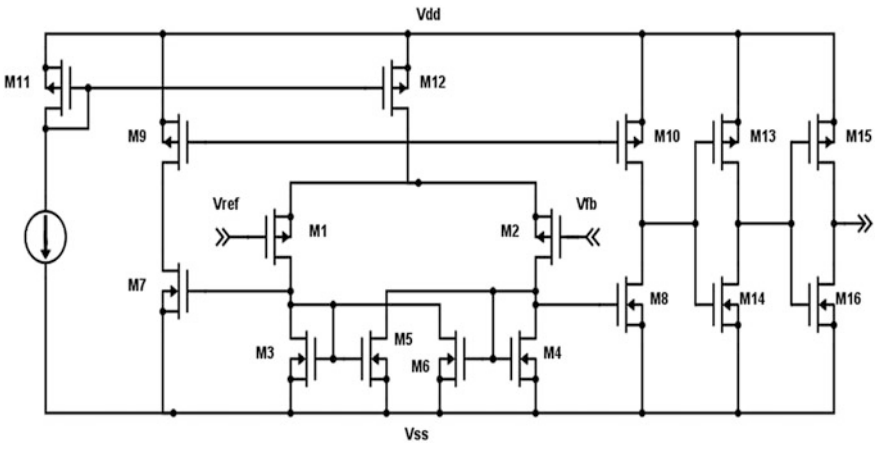


Fig. 11 Conventional comparator

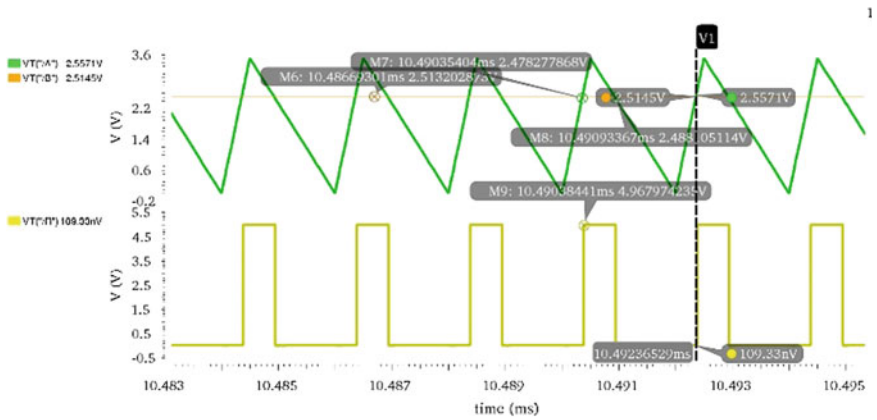


Fig. 12 Comparator output

Simulation results show the output of comparator operating at 500 kHz frequency as shown in Fig. 12.

3.4 Ramp Generator

A circuit is designed to generate compensated ramp and lock pulse as shown in Fig. 13. The slope of the compensated ramp is derived from reference current I_{ref} and capacitor C_1. When transistor Q_3 is ON, the I_{ref} current charges the capacitor.

As the node voltage at capacitor crosses the maximum reference level V_{refH} set by the hysteresis loop, it sets the SR latch and makes the Q_3 OFF and Q_4 ON. At

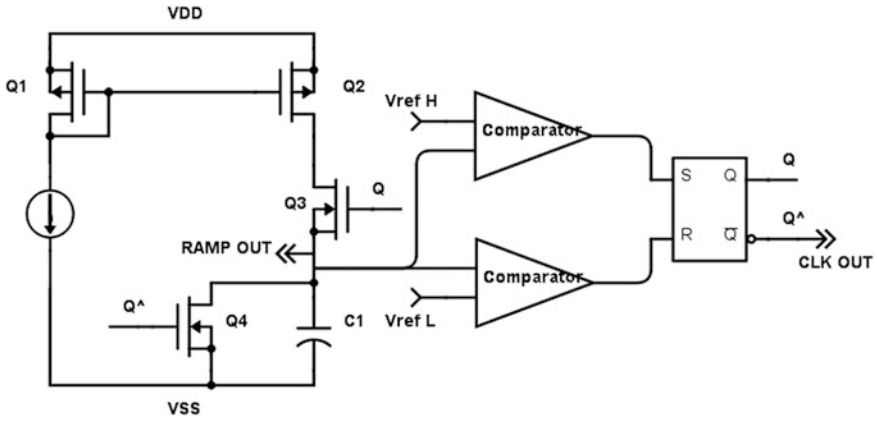


Fig. 13 Ramp and clock generator

this time instant, capacitor starts discharging through Q_4, until it reaches the minimum reference level V_{refL} set by hysteresis loop. The loop resets the SR latch and makes Q_3 ON and Q_4 OFF again.

3.5 Adder

An adder is required in current-mode controllers to add ramp with inductor current signal to prevent the system from sub-harmonic oscillations. There are so many ways to add two signals, and using an op-amp is one of that.

However, adding ramp signal with inductor current is not desirable with an op-amp. By converting the signal into current in nature, it helps to increase the accuracy. Therefore, V–I converter is designed to convert the voltage signals into current in nature. Then, both converted signals are passed through a knowing resistance for addition. The construction is done using two identical V–I converters as shown in Fig. 14. As per the construction, current mirrors M_5 and M_6 maintain the same current. The transistors M_3 and M_4 are driving inputs to the mirror for differential comparison, so that the difference is provided by the transistors M_7 and M_8. As the input ramp and current-sensed signals are in the range of 100–1000 mV, these are unable to drive the transistors M_3 and M_4. M_1 and M_2 transistors act as level shifters.

Voltage observed at node A is given by Eq. (18).

$$V_A = V_{\text{in}} - V_{\text{GS2}} \tag{18}$$

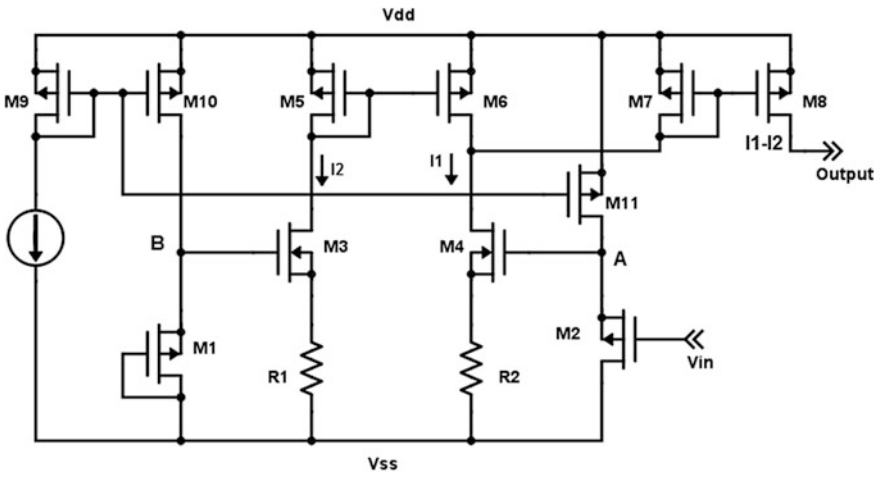


Fig. 14 V–I converter

V_A provides gate driving voltage to M_4. So the gain of this stage is determined by

$$G_{m4} = \frac{I_1}{V_A} = \frac{g_{m4}}{1 + g_{m4}R_2} \approx \frac{1}{R_2} \tag{19}$$

Here, I_1 is determined by

$$I_1 = \frac{V_A - V_{GS4}}{R_2} = \frac{V_{in} - V_{GS2} - V_{GS4}}{R_2} \tag{20}$$

To eliminate the extra terms $V_{GS2} + V_{GS4}/R_2$, the second stage is introduced which provides I_2, as shown in Fig. 13.

$$I_2 = \frac{V_B - V_{GS3}}{R_1} = \frac{-V_{GS1} - V_{GS3}}{R_1} \tag{21}$$

Output current I_{out} is given by

$$I_{out} = I_1 - I_2 = \frac{V_{in} - V_{GS2} - V_{GS4}}{R_2} - \frac{V_{GS1} - V_{GS3}}{R_1} \tag{22}$$

By maintaining the circuit as $I_{out} = V_{in}/R$, $R = R_1 = R_2$ and $V_{GS2} = V_{GS1}$, $V_{GS3} = V_{GS4}$.

$$I_{out} = \frac{V_{in}}{R} \tag{23}$$

3.6 PWM Generator

A SR latch is used for pulse width generation. However, in SR latch when both inputs are high, then outputs Q and $\overline{Q}$ both are forced to low. So, these set of inputs are forbidden. Anyhow after reaching the system into steady-state operation of current-mode boost converters, both the inputs do not go to high simultaneously. Even in start-up, the compensated error signal is anyhow lesser than that of adder output. As we are driving R with a pulse generated from fixed ramp generator, R is always present even in start-up to prevent the condition of both inputs going high.

To prevent this unreliable condition of SR latch, AND and NAND logic gates are added at the input stage of SR latch as shown in Fig. 15.

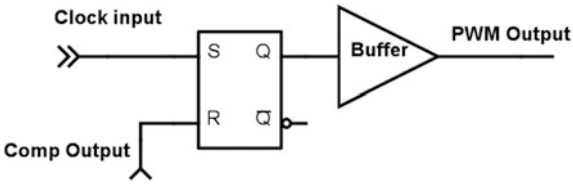


Fig. 15 PWM generator

4 Measured Results

The current-mode DC–DC boost converter has been implemented with a slandered 0.18 µm CMOS technology. The off-chip components used are shown in Fig. 16 and Table 2.

The power stage is designed for output ripple of ∼20 mV, at 25 V regulated output voltage. Figure 17 shows the output voltage with minimum ripple of 17 mV. In practice, it may vary since the ESR of the capacitor varies from component to component. Generally, ceramic capacitors are used for accuracy.

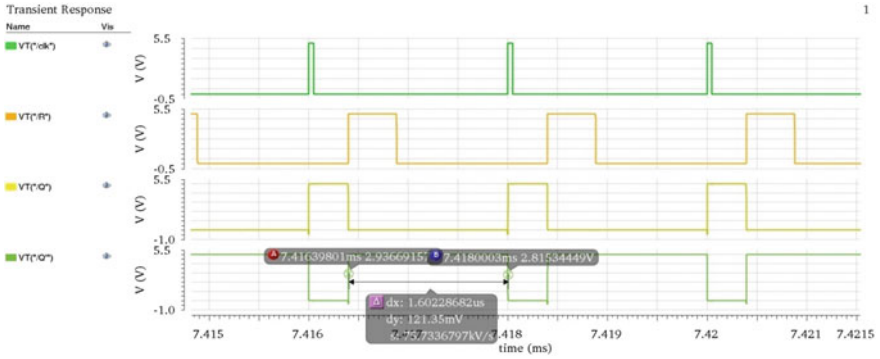


Fig. 16 PWM output waveforms

Table 2 External component values of DC–DC Converter

Component	Value	Component	Value
C_L	4.7 µF	R_L	0.5 kΩ
L	4.7 µH	R_1	2.2 MΩ
Diode	PMEG3010BEA	R_2	110 kΩ
C_1	100 nF	R_3	10 kΩ
R_{sense}	15 mΩ	R_4	1.5 kΩ

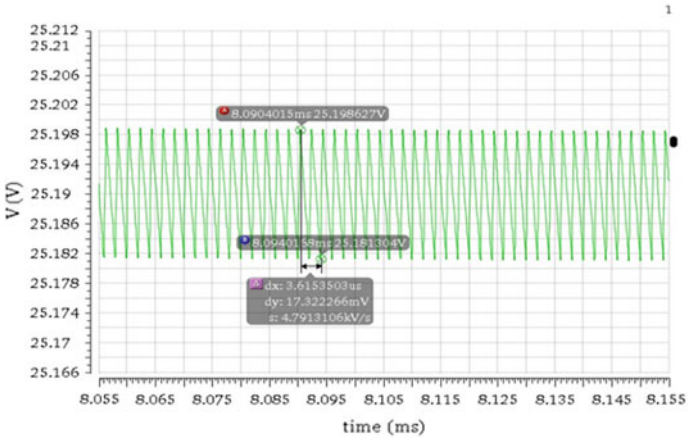


Fig. 17 Output ripple (17.3 mV) at output voltage 25 V

By introducing soft-start at V_{ref}, it is easier to control the inrush current in the inductor. The normal output voltage with effect of quiescent current is shown in Fig. 18. Due to the effect of quiescent current, output voltage reaches peak voltage (here 33.5 V) before it settles down at 25 V. Due to the large difference at the input terminals of OTA in the initial state, it makes error signal boost up; therefore, the pulse generated from PWM generator having high duty cycle causes inrush current. By using soft-start circuit as shown in Fig. 19, controlling the error signal is possible and prevents the peak output as shown in Fig. 20 [11]. Compared to Figs. 18 and 20, the response time is very less (i.e., decreased to half). Respective peak

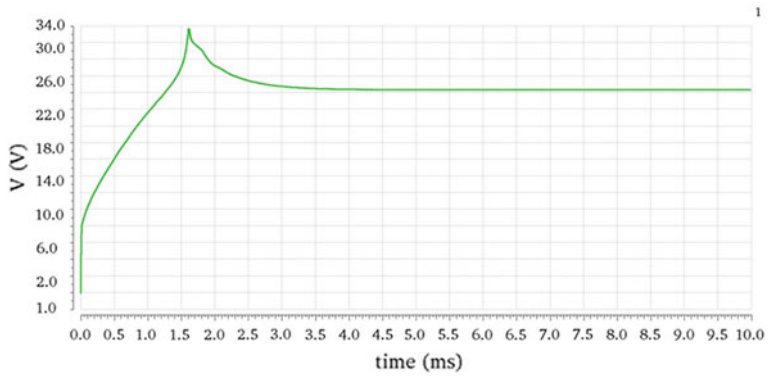


Fig. 18 Output voltage with huge inrush current

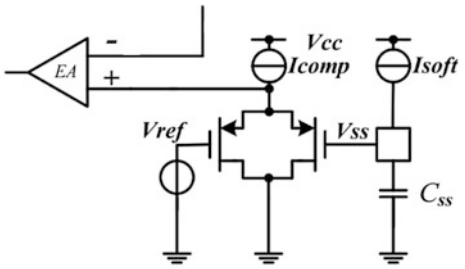


Fig. 19 Soft-start technique

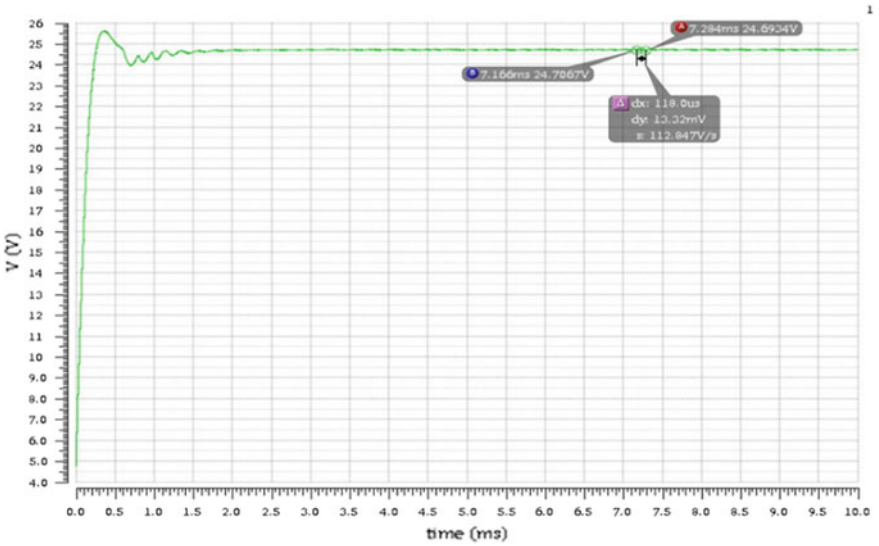
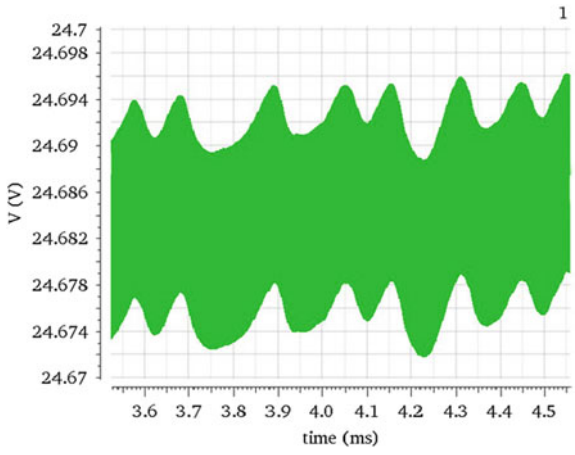


Fig. 20 Output voltage while using soft-start mechanism

Fig. 21 Output voltage at various loads (200 Ω–2 kΩ)



voltage is also reduced to 25.7 V from 33.5 V as shown in Figs. 18 and 20. In order to evaluate the load regulation of the controller, load is changed from 100 Ω to 1.5 kΩ at 1 ms. The regulated output voltage at various load conditions in CCM mode converter is shown in Fig. 21.

5 Conclusion

In this paper, the design of current-mode CMOS DC–DC boost converter with featured OTA for fast transient time and on-chip current-sensing technique for feedback current control mechanism is presented. The transconductance of the error amplifier is well controlled by using comparators in this design to maintain stability of the system. The stages of feedback control and implementation, including stage-wise outputs and measured results, are illustrated. An effective addition of compensation ramp to the current-sensing signal makes the output accurate, and on-chip current-sensing circuit reduces output pins and complexity of the design. This current-mode DC–DC boost converter with on-chip current sensing can operate at 500 kHz frequency with various loads and produces 25 V regulated voltage signal providing 5 V input voltage.

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A Modified GDI-Based Low-Power and High Read Stability 8-T SRAM Memory with CNTFET Technology

Apoorva Amdapurkar, Dinesh Wani, Pooja Shinde and P. Reena Monica

Abstract Background/Objectives: There is an enhancement in the short channel effects and leakage current as the devices are scaled down. Hence, it is almost impossible to design SRAM with high storage capacity and lower power dissipation using the current technology. To achieve higher efficiency and to decrease the power dissipation, a migration to Carbon Nanotube Field Effect Transistor (CNTFET) technology is imperative. GDI technique is one of the low-power methodologies employed to enhance the efficiency of the logic circuit. But to further reduce the leakage power of the circuits, the modified GDI (m-GDI) technique is used. **Methods/Statistical analysis**: The proposed work aims at designing an 8-T SRAM cell for high read stability and low power dissipation, using the modified GDI cell (m-GDI) technique based on conventional GDI cell. The simulation is done using Cadence Virtuoso with a supply voltage of 900 mV. Stability analysis is also performed for the SRAM cell. **Findings**: m-GDI technique solves the problem of voltage degradation in GDI technique. An 8-T SRAM cell with low power and high read stability is implemented. CNTs with chirality vector (13, 0) are found to be a good choice for low-power and stable SRAM cell. **Improvements/Applications**: CNTFET with m-GDI-based memories with their low power and high read stability has the potential to replace the current technology, if the shortcomings in the implementation are conquered.

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Keywords Carbon nanotube field effect transistors (CNTFETs)
Gate diffusion input (GDI) · Modified gate diffusion input (m-GDI)
Dynamic threshold-metal oxide semiconductor field effect transistors
(DT-MOSFET) · Static noise margin (SNM)

1 Introduction

SRAM is the fundamental block of a digital circuit. It consumes more area than any of the block in digital circuit. SRAM memories are the vital cause of static power. For an effective memory design, some parameters such as less chip area, low static power dissipation, and high performance should be considered. For achieving better stability in the SRAM memories, it can be designed with Carbon Nanotube Field Effect Transistors (CNTFETs). CNTFET provides advantages of ballistic transport and high scaling as compared to MOSFET. These unique properties of CNTFET make it a beneficial candidate while designing a memory.

Gate diffusion input (GDI) is a low-power technique which is popular for its low complexity and simple implementation with only two transistors implementing a wide range of complex logic functions [1]. Implementation of GDI cell using CNTFET is demonstrated in [2]. The GDI circuit suffers a degraded swing because of threshold drop. Therefore, a modified GDI technique (m-GDI) is demonstrated in [3]. The CNTFETs in m-GDI technique are used to enhance efficiency and reduce power consumption and chip area. In the m-GDI cell, DT-MOSFET technique is used to reduce the leakage power which makes it more useful in design of memories with high capacity. In this work, m-GDI cell with CNTFET is employed to design 8-T SRAM cell. When compared to conventional 6T CMOS SRAM, the 8-T SRAM with m-GDI cell gives advantages of less chip area and low power consumption. It also provides the improvement in reading stability of the SRAM cell. The simulation is done using Cadence Virtuoso with a supply voltage of 900 mV. A 4×4 SRAM memory is implemented, but for the sake of simplicity, the analysis of read, write, and hold cycle is performed using 1×1 SRAM cell. This paper is organized as follows: The GDI and m-GDI techniques are presented in Sect. 2. In Sect. 3, the 1×1 structure of 8-T SRAM cell using m-GDI technique is discussed. Section 4 presents the simulation results. Section 5 concludes the paper.

2 Gate Diffusion Input (GDI) and Modified GDI Tecnique

CMOS Logic has been the most popular design style, but there have been many efforts to find a better replacement for achievement of low power dissipation, minimized area, and better performance. Earlier, pass-transistor logic (PTL) was introduced as another replacement to static CMOS logic, but it was found to be well-matched to the circuits that contained huge number of multiplexers and XOR

gates, like an arithmetic unit. PTL applications of NAND gates and NOR gates are slower and dissipate more power than CMOS applications. This happens due to the drop of threshold near a single-channel pass transistor, and the output swing gets reduced. Moreover, the leakage problem of PTLs was much greater than that of CMOS.

The gate diffusion input (GDI) technique for reduction of power and area was proposed in 2002 [1]. This GDI approach was presented for fabrication in Silicon on Insulator (SOI) and twin-well CMOS processes initially. GDI technique simplifies the operation of a huge range of complex logic functions by using two MOS transistors only. This method provides enhanced characteristics of reduced power and reduced area than conventional static CMOS and current-known PTLs, and it is appropriate for designing the standard digital circuits. Similar to PTL implementations, the GDI circuit suffers a degraded swing because of threshold drop. Still, the flexible logic of the fundamental GDI cell and a significantly reduced transistor count provide power reduction.

The basic GDI cell is same as an inverter, but the drain and source terminal of PMOS and NMOS are not connected to V_{DD} and Gnd. The GDI cell has three terminals: *G* (the common input to the gate of both the PMOS and the NMOS), *P* (input terminal to the source or drain of the PMOS), and *N* (input terminal to the source or drain of the NMOS).

The bulks of both the NMOS and PMOS are connected to *N* terminal and *P* terminal, respectively, so they can be arbitrarily biased, unlike those of a static CMOS inverter. Table 1 shows the GDI cell's various functions when different configuration of input is applied.

Advantages of GDI:

1. GDI cells have less area and versatility than conventional static CMOS gates: Great diversity of functions implementation can be seen using GDI cell with just two transistors.
2. GDI cell has very low leakage: subthreshold leakage current is less, and gate leakage current can also be reduced.
3. Drop of threshold voltage can be solved with multithreshold techniques in GDI cell.
4. Power and delay are very much less in GDI logic style than CMOS logic style.

Table 1 Different functions performed by a GDI cell

N	P	G	D	Functions
LOW	B	A	A′B	F1
B	HIGH	A	A′ + B	F2
HIGH	B	A	A + B	OR
B	LOW	A	AB	AND
C	B	A	A′B + AC	MUX
LOW	HIGH	A	A′	NOT

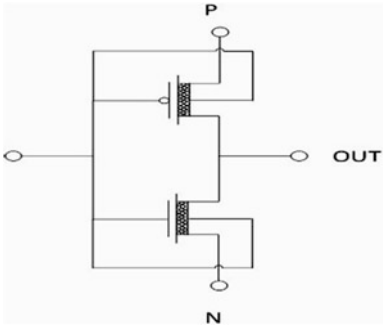

Fig. 1 Basic m-GDI cell

The CNTFET-based m-GDI cell is shown in Fig. 1. In m-GDI cell, the N-MOSFET and P-MOSFET are replaced by the N-CNTFET and P-CNTFET, respectively, and the bulk or the substrate of the CNTFETs is connected to the gate of the respective CNTFETs.

This type of arrangement is based on the Dynamic Threshold-Metal Oxide Semiconductor Field Effect Transistors (DT-MOSFET) technique. Use of m-GDI cell overcomes the voltage degradation problem of the GDI cell. This is evident from the comparison of the simulated waveforms of GDI cell and m-GDI cell in Figs. 2 and 3, respectively. The output waveform of the GDI cell is degraded to 700 mV, whereas the m-GDI output is at the applied 900 mV.

The power, delay, and power delay product of all functions using CNTFET-based GDI cell are presented in [2]. The power is in nanowatt (nW) for CNTFET as compared to MOS logic where it is in milliwatt (mW). The delay is also less as compared to the MOS logic implementation. This is because of the ballistic transport in channel modeled in the CNTFET model [4] as opposed to the diffusive transport of MOSFET channel. The quality of a digital gate is determined

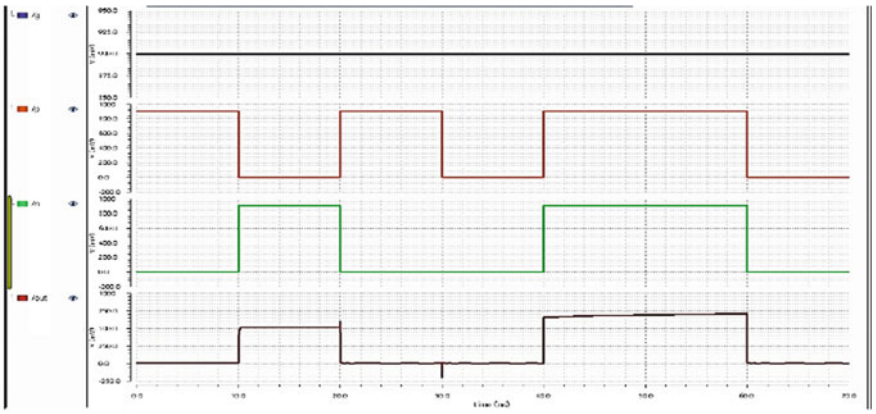

Fig. 2 Simulated waveform for different functions of GDI cell

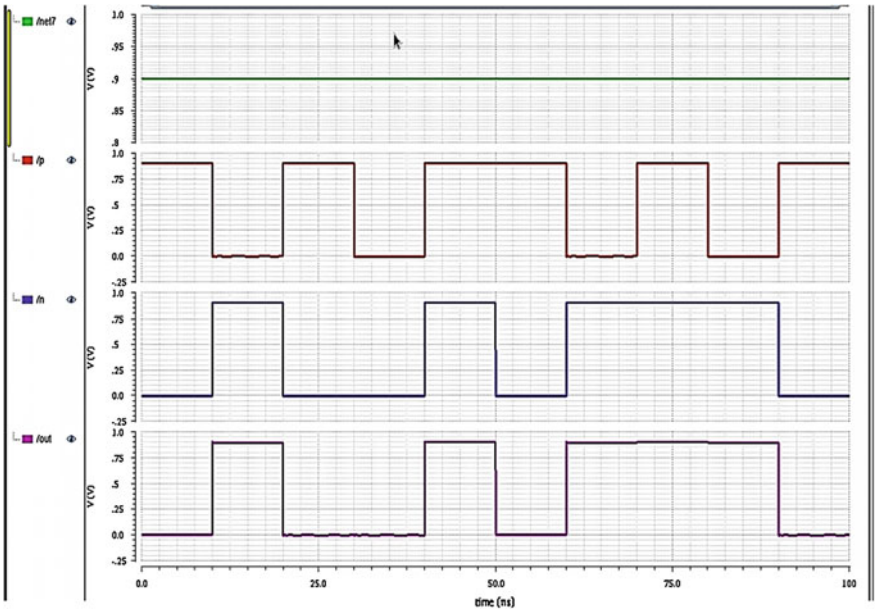

Fig. 3 Simulated waveform for different functions of m-GDI cell

by power delay product (PDP) which is a measure of average energy consumed per switching event. PDP is reduced drastically using combination of GDI logic and CNTFET [2].

3 8-T SRAM Cell Using CNTFET and M-GDI Technique

Figure 4 shows the structure of 8-T SRAM cell using CNTFET and m-GDI cell. The 8-T SRAM cell can have two structures, i.e., NLPA (N-CNTFET latches P-CNTFET access) and PLNA (P-CNTFET latches N-CNTFET access). The delay of NLPA structure is less when compared to PLNA; as far as power consumption is concerned, PLNA structure is superior to NLPA [5]. This work is with the PLNA structure of 8-T SRAM.

The m-GDI cell with F1 function is used for the analysis of read operation of SRAM cell. The transistors ENL and ENR are P-CNTFETs used as the driving transistors, while the transistors AL and AN are N-CNTFETs used as the access transistors. The transistors AL and AN provide the access of bit and bit bar line. The NL, PL, NR, and PR are the transistors used for m-GDI cell with F1 function. The two m-GDI cells are used for the improved stability of the SRAM. The operation of write, hold, and read of SRAM cell can be understood as follows:

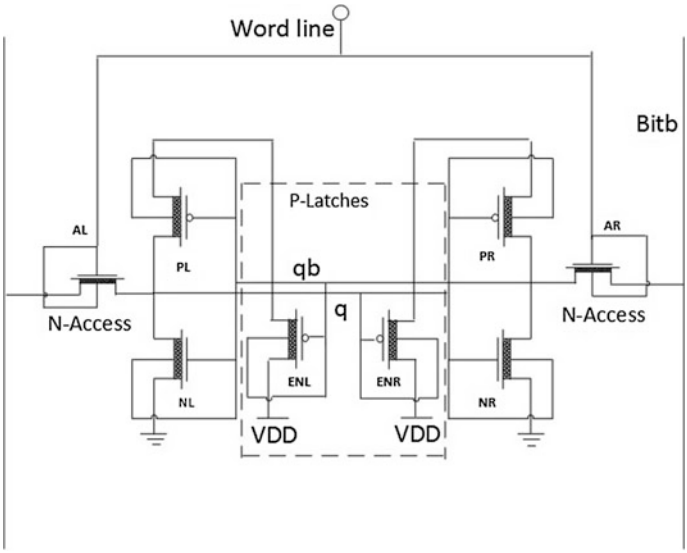

Fig. 4 8-T SRAM cell using m-GDI technique

WRITE:

To write data into the SRAM cell, the wordline should be enabled by providing high voltage to the wordline. When the wordline goes high, the access transistors AL and AN are turned ON and provide access of bit lines to the cell. The data at bit lines gets stored into the nodes *q* and *qb* of the SRAM cell. The speed of the data written into the cell is high.

HOLD:

Hold cycle starts when the voltage at the wordline goes low. The cell has no connection with the external circuitry, as the access transistor gets turned off. During the hold cycle, the cell holds the data written in the write cycle. With the help of m-GDI cell with F1 function, data is held.

READ:

Before the beginning of the read cycle, the bit and bit bar lines are pre-charged with the supply voltage. When the read operation starts, the voltage of the wordline goes high so the access transistor gets turned on. The data and the complement of the data which are stored in *q* and *qb*, respectively, can be attained by the data lines. The difference in the voltages of bit and bit bar lines will be sensed by the sense amplifier. Here, the m-GDI cells are used with F1 function to hold the data so the distortion of the data will not take place, which helps to improve the reading stability of the SRAM cell. The driver transistor added to the SRAM cell helps to decrease the capacitance on the data lines.

4 Simulation Results

The analysis of the read, write, and hold cycles is performed in Cadence Virtuoso. Figure 5 shows the writing operation of a 1 × 1 8-T SRAM cell. When the wordline goes high, the data on bit and bit bar lines is written into the *q* and *qb* nodes; also when the wordline goes low, the nodes q and *qb* hold the value written into it. Table 2 shows the comparison of NLPA and PLNA structure of 8-T SRAM on the basis of delay and power. The comparison shows the rapidness of NLPA structure and low power of PLNA structure. Figure 6 shows read operation of 1*1 8T Sram Cell.

Table 3 shows the effect of changing the chirality vectors of CNTFET on the power and delay of 8-T SRAM cell. CNTFET with chirality vector (13, 0) is found to be a good choice for low power.

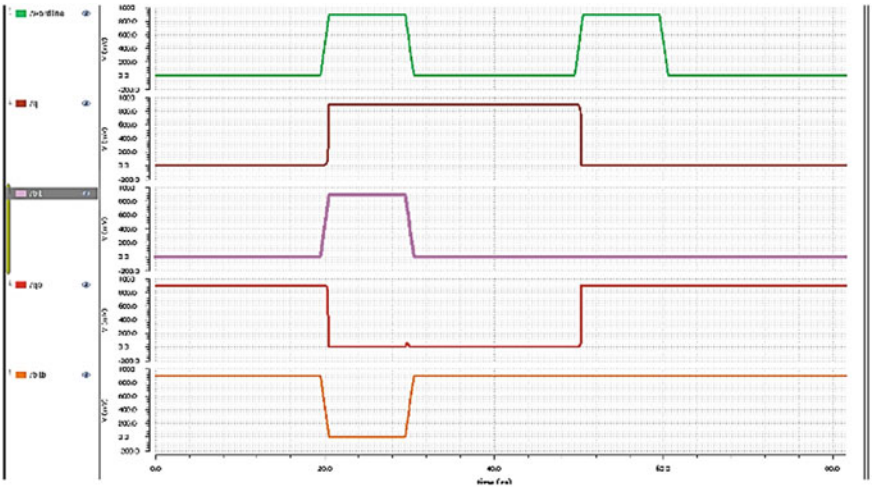

Fig. 5 Write and hold cycle of 8-T SRAM cell

Table 2 Power and delay comparison of NLPA and PLNA structure

Structure	Delay	Power
NLPA	817.8 fs	32.67 nW
PLNA	41.85 ps	14.53 nW

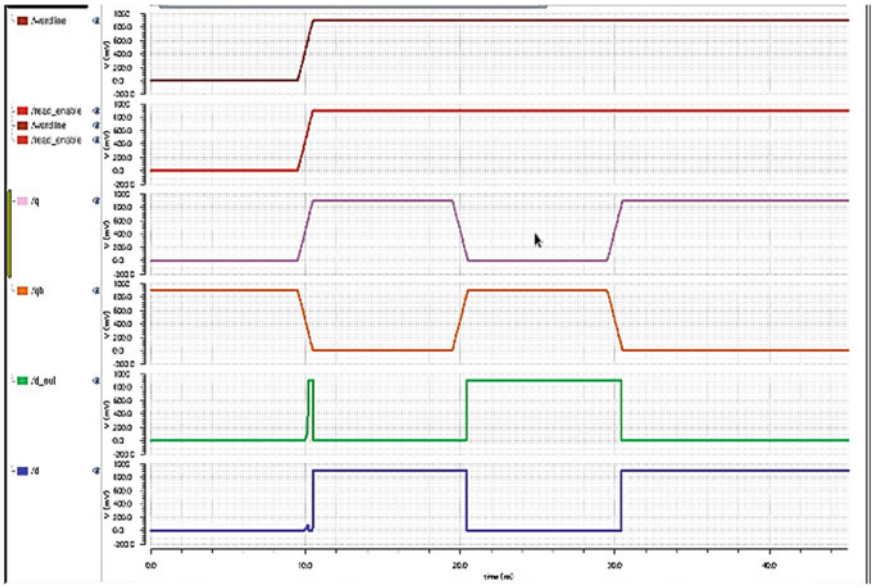

Fig. 6 Read cycle of 8-T SRAM cell

Table 3 Effect of chirality vector on power and delay of 8-T SRAM cell

Chirality vectors (n, m)	Delay (ps)	Power (μW)
(13, 0)	1.71	1.98
(16, 0)	1.33	5.6
(19, 0)	1.14	9.9
(22, 0)	1.06	14.28

5 Stability Analysis with Butterfly Curve

Figure 7 shows the static noise margin (SNM analysis) of the read operation of 8-T SRAM cell. Stability is measured in terms of static noise margin which is the tolerance of DC noise voltage, without the flipping of data stored in cell. To ensure nondestruction operation during hold, HSNM analysis is used [6]. During hold cycle, wordline is disabled which will turn off access transistors, and the bit lines q and qb are swept from 0 to Vdd. By plotting the VTC curves, the butterfly curve for HSNM was derived. With the help of diagonals of the maximum embedded squares, we can calculate the sides. The maximum stability is obtained for chirality (13, 0). By decreasing the chirality, the stability increases for CNTFET.

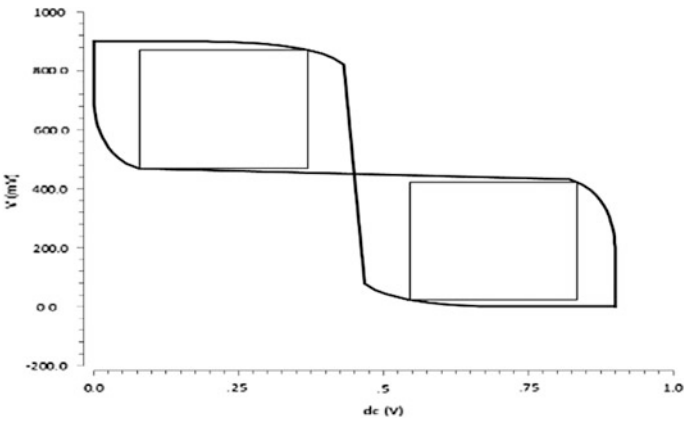

Fig. 7 SNM analysis of hold cycle of 8-T SRAM

6 Conclusion

An 8-T SRAM cell using m-GDI technique based on conventional GDI cell was designed and analyzed for read, write, and hold cycles. The voltage degradation problem in GDI cell is overcome by employing m-GDI cell for the design of 8-T SRAM. The effect on power and delay of 8-T SRAM cell by changing the chirality vectors of CNTFET was analyzed. SNM analysis is also carried out. CNTFET with chirality vector (13, 0) is found to be a good choice for low-power and stable SRAM cell. CNTFET with m-GDI-based memories with their low power and high read stability has the potential to replace the current technology, if the shortcomings in the implementation are conquered.

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To Refer a Research Article

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High Performance Trench Gate Power MOSFET of Indium Phosphide

Geeta Tahalyani, Raghvendra Sahai Saxena and T. Vigneswaran

Abstract Indium Phosphide material-based trench gate power MOSFET has been proposed as an efficient power device for low to medium voltage power applications. Use of Indium Phosphide material, because of its larger band gap, improves the OFF-state performance, like increased breakdown voltage and reduced OFF-state leakage current. On the other hand, its high electron mobility and diffusivity result in higher drive current capability, which in turn, significantly improves the transconductance and reduces ON-state resistance. Using 2D numerical simulations, we have shown that the proposed Indium Phosphide-based trench MOSFET shows 36% improvement in breakdown voltage, 75% reduction in ON resistance and 400% improvement in peak transconductance as compared to the equivalent Si trench MOSFET of ~50 V class.

Keywords ON resistance · Power MOSFET · Transconductance
Trench MOSFET

1 Introduction

Trench gate configuration of a power MOSFET provides minimum ON-state resistance compared to that of any other MOSFET configurations of otherwise similar specifications [1, 2]. It finds several applications in low to medium voltage power switching, like microprocessor power supply, automobiles. To get high

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Table 1 Comparison of material parameters of silicon and Indium Phosphide [14]

Parameters	Silicon	InP
Energy bandgap (eV)	1.12	1.34
Intrinsic carrier concentration (cm^{-3})	1×10^{10}	1.3×10^{7}
Breakdown field (V/cm)	3×10^{5}	5×10^{5}
Electron mobility ($cm^2\ V^{-1}\ s^{-1}$)	1400	5400
Diffusion coefficient ($cm^2\ s^{-1}$)	36	130

efficiency and low loss in power control, very low ON-state resistance is required along with reasonable OFF-state performance. However, all the important performance parameters of a trench MOSFET are interlinked and any effort to change one parameter affects the others [2]. Therefore, improving the device performance further is a very challenging task.

Silicon is traditionally being used for fabricating majority of the semiconductor devices, including the trench power MOSFETs, from several decades. To meet ever persistent demand of improved performance has resulted in several innovative design improvements of conventional Si-based trench MOSFETs [3–7]. All these techniques provide better compromise among the performance parameters usually at the cost of increased fabrication complexity. Since now Si has reached to its performance limits, alternate materials such as strained Si, SiGe, SiC, GaAs, InGaAs, InP are being explored from past a few years to enhance the performance of various devices [8–13].

In this paper, we propose to use Indium Phosphide as an alternate material for fabrication of trench MOSFET, which possesses higher electron mobility, higher saturation velocity and higher diffusion coefficient in comparison to Si, proving better current capability [13]. On the other hand, its higher bandgap, lower intrinsic carrier concentration and larger breakdown field provide low leakage current and large breakdown voltage. Some of the important electrical properties of InP and Si are shown in Table 1 for comparison [14]. Using 2D numerical simulations in ATLAS device simulator [15], we have shown Indium Phosphide trench MOSFET exhibits significant improvement on all the performance parameters as compared to Si-based trench MOSFET of equivalent device architecture.

2 The Device Structure

Trench MOSFET is a vertical MOSFET structure, wherein the current flows from the substrate side, which acts as drain, to the surface of the chip, which acts as source. The architecture of an N-channel trench MOSFET is shown as a cross-sectional view in Fig. 1.

The gate of this MOSFET is created in deep trenches opened through the oppositely doped body region. When sufficiently high voltage is applied between the gate and the source, a channel of electrons is created near the trench surface in

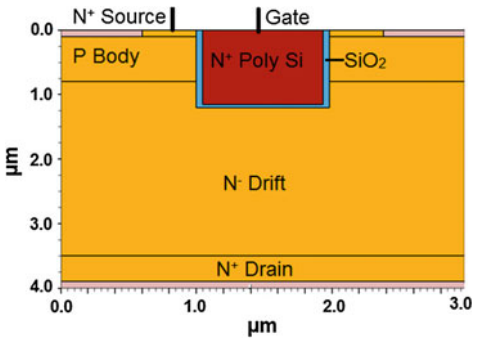

Fig. 1 Cross-sectional view of trench gate power MOSFET

body region. In this condition, the current conduction starts between drain and source, if a suitable drain-to-source voltage is applied.

3 Simulation Details

To compare the performance of proposed Indium Phosphide trench gate power MOSFET with the conventional Si trench MOSFET, we have simulated the standard architecture of trench MOSFET as shown in Fig. 1 for both the materials and performed 2D numerical simulation in ATLAS device simulator. We have used the dimensions as shown in the figure and carrier concentrations were set to be 1×10^{19}, 1×10^{17}, 2×10^{16} and 1×10^{19} cm^{-3} for the source, the body region, the drift region and the drain, respectively.

We have used Shockley-Red-Hall (SRH) recombination, concentration-dependent mobility (CONMOB) and band gap narrowing (BGN) models for these simulations and used the default parameters of these materials as available in the simulator.

4 Results and Discussion

We have obtained a very significant improvement in the performance parameters of Indium Phosphide (InP) trench MOSFET compared with those of Si, which is summarized in Table 2. A brief description of these parameters is as follows:

Table 2 Comparison of performance parameters of silicon and Indium Phosphide trench MOSFETs

Performance parameters of trench MOSFET	Si	InP
Threshold voltage (V)	1.6	1.8
ON current @ V_{DS} = 0.1 V, V_{GT} = 5 V (μA/μm)	9	42
ON-resistance @ V_{DS} = 0.1 V, V_{GT} = 5 V (Ω μm)	11.0	2.4
Peak transconductance (μS/μm)	7	35
Breakdown voltage (V)	55	75
Gate capacitance @ V_{GT} = 2 V (pF/μm)	1.12	1.12

4.1 ON-State Performance

The ON state refers to the state when the applied gate to source voltage, V_{GS} is sufficiently higher than the threshold voltage and the device conducts high current through it. For a good switching performance, the power device should be able to carry high current and resistance should be near zero so as minimize the I^2R power loss while conducting huge current. For a good power amplifier, the device should have high transconductance to attain high cutoff frequency.

The ON-state performance of Si and InP trench MOSFETs is compared in Fig. 2a–c, wherein ON current (I_{ON}) for V_{DS} = 0.1 V, ON resistance (R_{ON}) and transconductance (g_m) are plotted as functions of V_{GT} (V_{GS}–V_{Th}). We find that InP provides significant decrease in ON resistance of ∼75% and a very significant rise in peak transconductance of ∼400%.

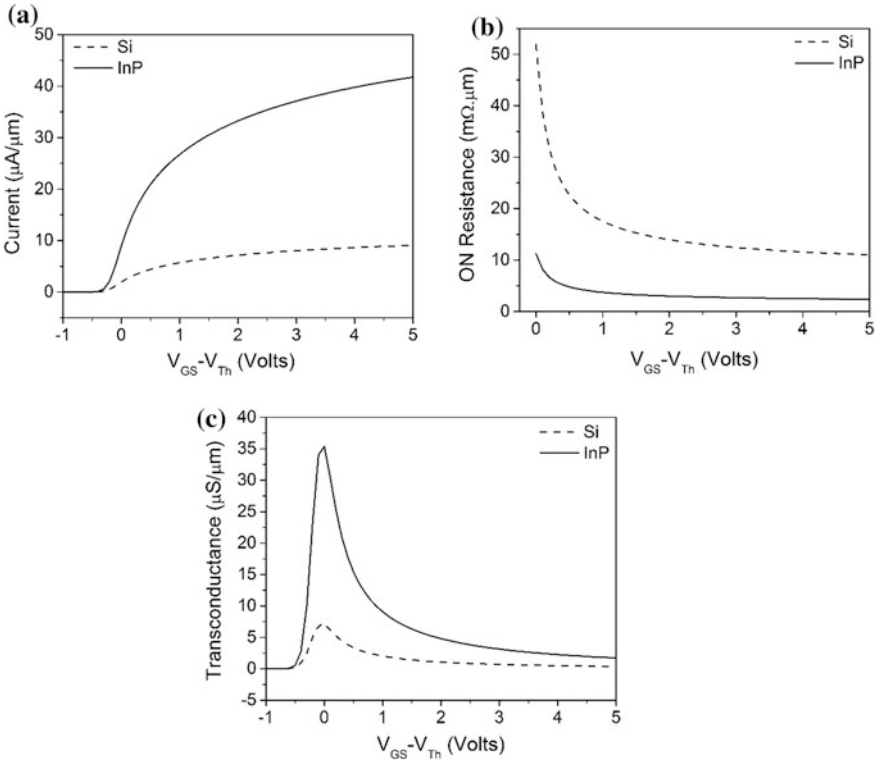

Fig. 2 Simulated characteristics of ON-state performance of Si and InP trench MOSFETs, **a** I_{DS}–V_{GS} characteristics for V_{DS} = 0.1 V, **b** R_{ON} versus V_{GT} curves, **c** transconductance versus V_{GT}

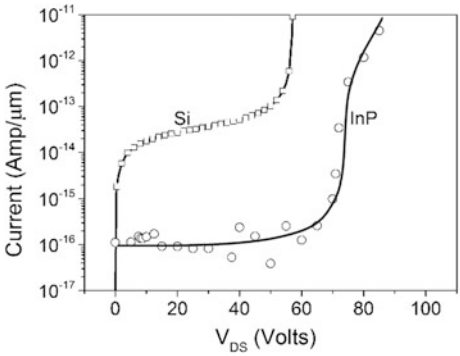

Fig. 3 Simulated I_{DS} versus V_{DS} characteristics for V_{GS} = 0.0 V, for both Si and InP trench MOSFETs, showing there breakdown

4.2 OFF-State Performance

In OFF state, the V_{GS} is kept below threshold voltage, usually V_{GS} = 0.0 V and device sustains a high V_{DS} voltage across it. For a good switching performance, the power device should be able to sustain a very high reverse voltage, known as the breakdown voltage and should allow very small reverse leakage current through it so as to minimize OFF-state power losses.

The OFF-state performance of Si and InP trench MOSFETs is compared in Fig. 3, wherein I_{DS} as a function of V_{DS} is shown for V_{GS} = 0.0 V. We find that leakage current through InP trench MOSFET is only 10^{-16} A/μm, more than two several orders of magnitudes lower than that of Si trench MOSFET, which has leakage current in the range 10^{-14}–10^{-13} A/μm. Also the breakdown voltage of InP trench MOSFET is ∼75 V compared to ∼55 V of Si trench MOSFET, indicating a 36% improvement in breakdown voltage.

4.3 Gate Capacitance

Another very important parameter of a power MOSFET is the gate capacitance as it governs the switching losses and the speed of the switching. For a good switching performance, total gate capacitance C_G should be small.

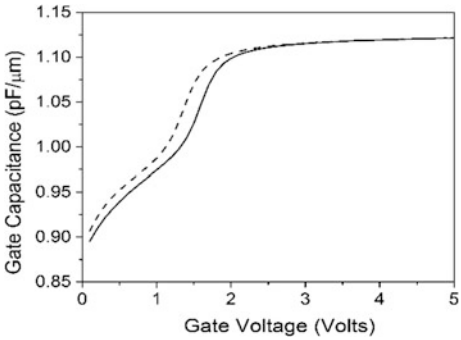

Fig. 4 Quasi-static capacitance–voltage profiles of gate electrode of both Si and Indium Phosphide MOSFETs

Quasi-static *C-V* characteristics of Si and InP MOSFETs are shown in Fig. 4. From the figure, it may be seen that the *C-V* profiles for both the MOSFETs are almost the same. The shift of about 0.2 V in the *C-V* characteristics is because of the difference in their threshold voltages.

5 Conclusion

We have proposed a trench gate power MOSFET of InP and compared its performance with the conventional Si-based trench MOSFET using standard device simulator ATLAS. We have demonstrated that all the performance parameters can be improved very significantly over Si by using InP material for trench MOSFETs. This may lead to a very attractive power device for low to medium voltage power applications.

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Memristor Equipped Error Detection Technique

Anindita Nayak, Satyajeet Sahoo and S. R. S. Prabaharan

Abstract Objectives: Memristor, an emerging technology, is a non-volatile random access memory (NVRAM), i.e., it does not loose its data even when the power is switched off. Memristor devices can also retain its behavior in logic design. Digital data transmission has made today's world more efficient for data communication. The paper emphasizes on the implementation of one of the error detection technique using memristor. **Methods/statistical analysis**: To procure better simulation result on the basis of accuracy and computational efficiency, the hybrid memristor-based parity generator and checker circuit is designed after performing the parametric variation in VTEAM Model using Cadence Virtuoso Environment. **Findings**: The hybrid memristor-based 3-bit odd and even parity generator and checker circuit is designed using memristor-based XOR gate by varying the resistance (R_{off} and R_{on}) values of each memristor and hence verified for all the possible input combinations of the design. **Improvements/applications**: The proposed memristor-based circuit, if implemented physically in digital communication system, will definitely strive the hunger in terms of area and power as compared to CMOS-based parity generator and checker circuit.

Keywords Memristor · Non-volatile memory · Voltage controlled Error detection · Parity generator · Checker

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1 Introduction

In the year 1971, Leon Chua postulated a fourth fundamental component [1] known as memristor, a two-terminal device. Further, Chua and his student Kang [2] elaborated the relation between the time integral of voltage (v) and current (i), defined by:

$$v(t) = R(w) \cdot i(t) \tag{1}$$

$$\frac{\mathrm{d}w}{\mathrm{d}t} = f(w, i) \tag{2}$$

where $R(w)$ is called as instantaneous resistance that depends on state variable (w) of the memristive device. It remained theoretically, but in the year 2008, HP Laboratory [3] demonstrated prominent nanoscale fabricated memristor device showing the pinched-hysteresis curve. The emerging technology, memristor is non-volatile in nature, i.e., it retains its history when the device is turned on. Apart from its significant application which is memory, it finds multiple applications in oscillator, basic logic design [4–6] and neuromorphic system [7–10].

Noise is an important factor that affects the data bits during the transmission through communication channel in digital communication. A parity bit is an extra bit, i.e., required to detect the erroneous message, if present, in the data stream. To make the original message bit stream even or odd number of 1's, a parity bit is required. The original signal is transmitted along with the extra bit and then at the receiver end, the error is checked. There is an error present if the transmitted or the received data are mismatched.

This paper is categorized as follows: Sect. 2 gives the details of VTEAM model; Sect. 3 explains the detailed design and implementation of error detection technique; Sect. 4 gives the number of memristor and CMOS are used for the design; Sect. 5 concludes the paper.

2 Voltage Threshold Adaptive Memristor (VTEAM) Model

Previously, many memristor models [11–14] were proposed. In case of physical memristor, by performing many experiments it was proved that it is due to the existence of the threshold voltage rather than the threshold current [3, 15, 16]. The TEAM model is basically found to be dependent on the current threshold, i.e., below certain range of current there is no change in the resistance level.

The VTEAM model is nothing but the extension of earlier proposed TEAM model (i.e., designer-friendly, simple) with the threshold voltage and the model assumes asymmetric and nonlinear switching behavior [14]. The VTEAM model is

computationally efficient and accurate in comparison to the existing device models [17]. The above expressions show the presence of a threshold voltage. The internal state variable derivative of VTEAM is mathematically [18] presented as:

$$\frac{\mathrm{d}w(t)}{\mathrm{d}t} = \begin{cases} k_{\mathrm{off}} \cdot \left(\frac{v(t)}{v_{\mathrm{off}}} - 1\right)^{\alpha_{\mathrm{off}}} \cdot f_{\mathrm{off}}(w), & 0 < v_{\mathrm{off}} < v \\ 0, & v_{\mathrm{on}} < v < v_{\mathrm{off}} \\ k_{\mathrm{on}} \cdot \left(\frac{v(t)}{v_{\mathrm{on}}} - 1\right)^{\alpha_{\mathrm{on}}} \cdot f_{\mathrm{on}}(w), & 0 < v_{\mathrm{on}} < v \end{cases} \tag{3}$$

where, k_{off}, k_{on}, α_{on}, α_{off} are constants, parameters v_{on} and v_{off} are threshold voltages $f_{\mathrm{off}}(w)$ and $f_{\mathrm{on}}(w)$ are the window function [19]. The I–V relation is expressed as:

$$i(t) = \left[R_{\mathrm{on}} + \frac{R_{\mathrm{off}} - R_{\mathrm{on}}}{w_{\mathrm{off}} - w_{\mathrm{on}}} \cdot (w - w_{\mathrm{on}})\right]^{-1} \cdot v(t) \tag{4}$$

where w_{on} and w_{off} describes the bounds of internal state variable w [17].

In VTEAM, below a particular threshold voltage, the resistance of the memristor will not be altered. For logic operation and memory application, threshold voltage of a memristor is more accurate that of threshold current in comparison to TEAM model [14].

Figure 1 shows the variation in threshold voltages i.e. V_{on} and V_{off} determine how fast the RESET operation is performed. Observing the figure, the threshold voltages values taken from $V_{\mathrm{on}} = -0.2$ V and $V_{\mathrm{off}} = 0.02$ V have faster reading mechanism than $V_{\mathrm{on}} = -0.5$ V and $V_{\mathrm{off}} = 0.05$ V [14]. In comparison to the previous existing models, the hysteresis plot shows that the response is asymmetric in nature and it has a fast switching as the reading operation is performed faster [14].

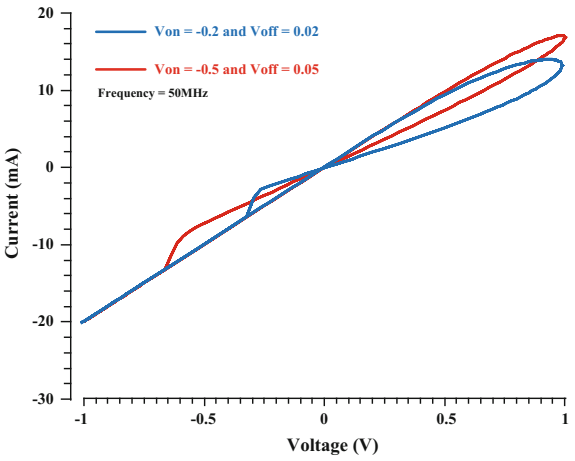

Fig. 1 Current–voltage characteristics of memristor due to variation of threshold voltage

3 Error Detection Technique

Error detection is a method that validates the transfer of digital data over unreliable channel. When signal is sent through transmission media, it is subjected to attenuation, noise and other impairments for which some bit stream at the transmitted output gets corrupted, in other words, it gives rise to some erroneous message at the receiver end. So in order to achieve reliable communication through the unreliable media, we have to device the mechanism for checking the error that occurs during transmission.

Parity bit is the simplest and the most popular scheme for error detection. In order to have total number of 1's either even or odd, an additional bit, called parity bit is provided with the data stream. If number of 1's in the bit stream is even, then it is even parity, and if the number of 1's in the bit stream is odd, then it is odd. In this paper, 3-bit even parity scheme is taken as a case study.

In the transmitter side, the combinational design of a parity generator introduces the parity bit. In the receiver side, to check the bit stream with parity bit, parity checker logic design is used. In the even parity generator scheme, the parity bit is 0, if the bit stream consists of the even number of 1's and the parity bit is 1, if the bit stream consists of odd number of 1's. Table 1 represents the truth table for even parity bit generator circuit.

A minimized expression of the parity bit is achieved from the above truth table which can be written as $P = A \oplus B \oplus C$. The hybrid memristor-based circuit for 3-bit even parity generator, shown in Fig. 2, consists of two XOR circuit [16]. The basic expression of the XOR gate used is $A \oplus B = (AB + A'B')'$, where the OR implementation is replaced by NMOS and is driven by a NMOS device instead of simple resistor [14].

To elaborate the operation of XOR circuit, $A = 1$ and $B = 0$ is taken as a case study. We know R_{off} (high resistance) >> R_{on}(low resistance). The current flows through V_{cc} (logic 1) to ground (logic 0). When the current passes from memristor $M1$, the resistance of $M1$ increases to R_{off} and the resistance of $M2$ decreases to R_{on} and current reaches to the ground (logic 0) node. Logic 0 is obtained at the common

Table 1 Truth table for 3-bit even parity generator

3-bit message			Even parity bit
A	B	C	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

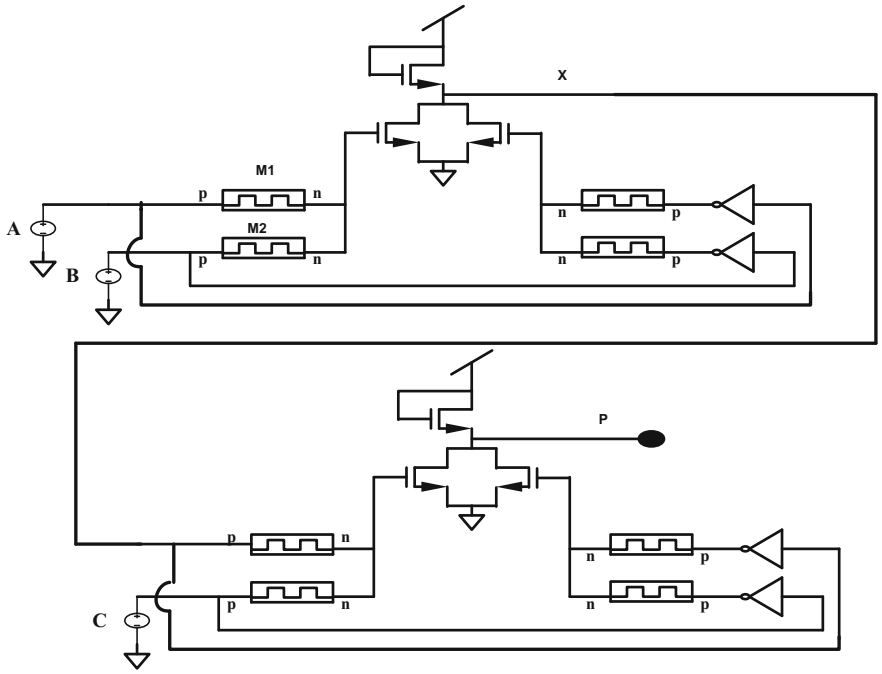

Fig. 2 Schematic of 3-bit even parity generator

node of $M1$ and $M2$ according to voltage divider rule and the logic is fed to NMOS and it gets off.

The output voltage (X) is calculated as:

$$\begin{aligned} X &= V_{cc} * \left(\frac{R_{on}}{R_{off} + R_{on}} \right) \\ &= V_{cc} * \frac{R_{on}}{R_{off}} \ll V_{cc} \approx \text{ground} \end{aligned} \tag{5}$$

Now, the entire supply voltage with some drop due to the resistance appeared at the output node, and hence, the output is logic 1. The parity checker circuit checks whether the parity generated signal along with the 3-bit message, erroneous or it is the original one. The output waveform for 3-bit even parity generator circuit is shown in Fig. 3 for few combinations as a case study.

Now, to check the probability of error on the data stream, four input bits are applied to the parity checker logic design. Any occurrence of error in the message is received which shows the presence of odd number of 1's otherwise even number of 1's. Table 2 shows the truth table for the even parity checker circuit. From the

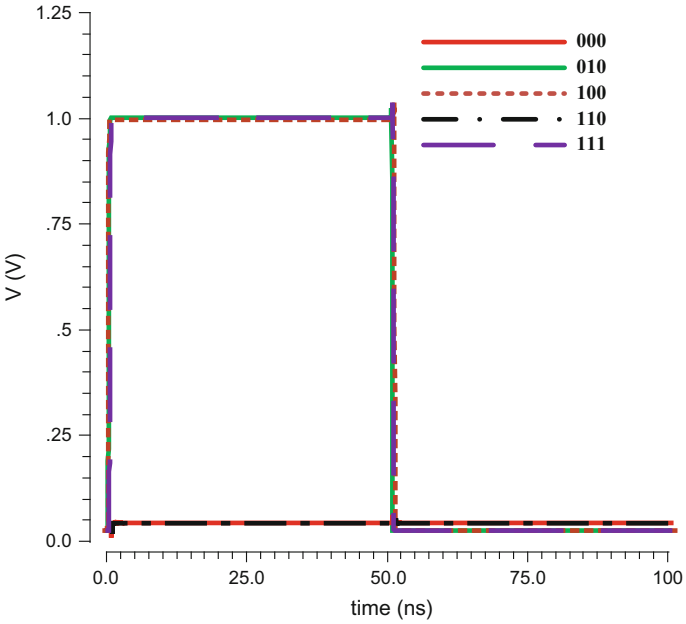

Fig. 3 Output waveform for 3-bit even parity generator circuit

Table 2 Truth table for 4-bit even parity checker

4-bit message received				Parity error check
A	*B*	*C*	*P*	*Y*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

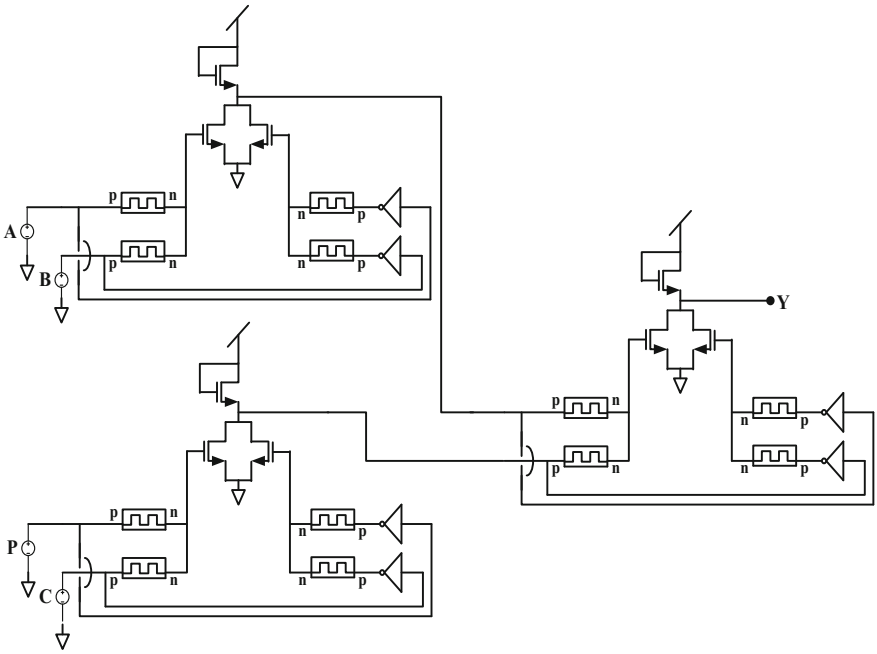

Fig. 4 Schematic diagram 4-bit even parity checker

Table 2, the minimized expression for parity checker is $Y = (A \oplus B) \oplus (C \oplus P)$. By using three memristor-based XOR design, the even parity checker design is implemented as depicted in Fig. 4. The output waveform for 3-bit even parity checker circuit is shown in Fig. 5 for few combinations as a case study.

4 Results and Discussion

Based on the above study, the number of memristor and transistor required for 3-bit even parity generation and checker logic design is shown in Table 3.

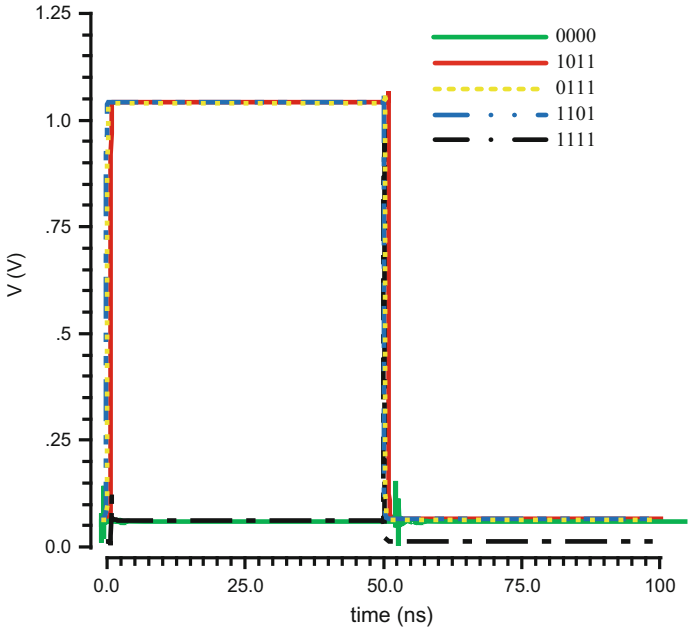

Fig. 5 Output waveform for 4-bit even parity checker circuit

Table 3 Number of memristor and transistor in 3-bit even parity generation and checker logic design

	Hybrid memristor-based design (number of memristors (M) and transistors (T))
Parity generation	8M + 14T
Parity checker	12M + 21T

5 Conclusion

The memristor-based on Verilog-A is modeled with the changes in threshold voltages. Parametric analysis, I–V plot and logical computations have been performed using Cadence Virtuoso tool, to show the effectiveness of VTEAM model. Based on the present study, it is found that the switching operation can be performed faster compared to the existing models. Accordingly, the memristive model is successfully implemented for parity generation and checker logic design by changing the resistance value in the design. If the circuit implemented physically in digital communication system, then it would have an alternative way for the communication system thereby reducing the area and power consumption as compared to CMOS-based parity generator and checker circuit design.

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28 nm FD-SOI SRAM Design Using Read Stable Bit Cell Architecture

A. Lourts Deepak, Mrinal Gandotra, Shailja Yadav, Himani Gandhi and S. Umadevi

Abstract Background: Memories occupy the majority of chip area, and the response time for any system depends on its memory too. So, SRAMs are critical to the speed of processor operations and thus need to be rigorously optimized. The optimizations have to be in such a way that the constraints of better performance as well as reliability are met. **Methods/Statistical analysis**: The proposed bit cell is compared with conventional 6T bit cell for access time, read stability, on-current, and off-current, and the suitable sense amplifiers and decoder are analyzed. **Findings**: The proposed architecture for SRAM design meets the criteria of faster access time and read stability as compared to the conventional 6T SRAM. Write 1 operation achieves a rise of 16%, while write 0 and read 1 are better than 6T by 70 and 90%, respectively. The design was implemented on 28 nm FD-SOI platform. **Application/Improvements**: The proposed design has the better read stability as compared to the conventional 6T SRAM bit cell design.

Keywords SRAM · 6T · 5T · Dual port · Read stable

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1 Introduction

One of the most essential elements in any system is its embedded memory. SRAM is an increasingly popular choice as the both on-chip and off-chip memories. The SRAMs are generally implemented using arrays of densely packed bit cells along with the peripheral circuitry like pre-charge circuitry, write circuitry, sense amplifier. A conventional SRAM cell is 6T SRAM which has two back to back connected inverters and requires access transistors as well. 6T SRAM cell faces difficulty meeting the growing demand for a large memory capacity in terms of reliability and stringent sizing demands [1].

This paper proposes a novel 5T dual port SRAM cell. The behavior of the cell under various operating modes has been explained and is supported with simulations. Read and write operations are performed from different ports accessible through word line. The proposed design has been tested for on-current, off-current, access time, and noise margin. The proposed design has a faster access as compared to conventional 6T.

After a brief description about the standard array configuration with 6T bit cell in Sect. 2 and previous bit cell designs in Sect. 3, we will elaborate on our proposed 5T bit cell design along with its operations in Sect. 4. The Sense amplifier and decoder design are then subsequently elaborated upon in Sects. 5 and 6. The simulation results are presented in Sect. 7 with Sect. 8 concluding the paper and listing future scope for the design.

2 Conventional SRAM Array

An SRAM array, Fig. 1, has a decoding unit that gives the address bits n for input and m for output, to access one of the bit cell for read and write operation via word line (WL). One of the bit cells is chosen out of the memory array according to that address given at inputs.

A typical 6T SRAM bit cell is shown in Fig. 2 consists of two cross-coupled inverters with two NMOS transistors connected on each end to access the bit lines. The storage nodes Q and Q_B are directly accessed by the bit lines for the read and write operations. In the figure, the back to back inverters are formed by the PMOS–NMOS pairs P_0–N_0 and P_1–N_1 with node Q at output of INV_0 and node Q_B at output of INV_1. The access transistors are A_1 and A_2 for BL and BLB, respectively.

During a write operation, the BL and BLB are set to with the data and its complement, respectively. For example, to write logic '1' the BL is pre-charged to V_{DD} and BLB to V_{SS}. When WL is turned on, node Q is set to logic '1' through access transistor A_1 and BL, which turns on N_1 and sets the node Q_B to logic '0'. This turns transistor P_0 on re-enforcing logic '1' at Q.

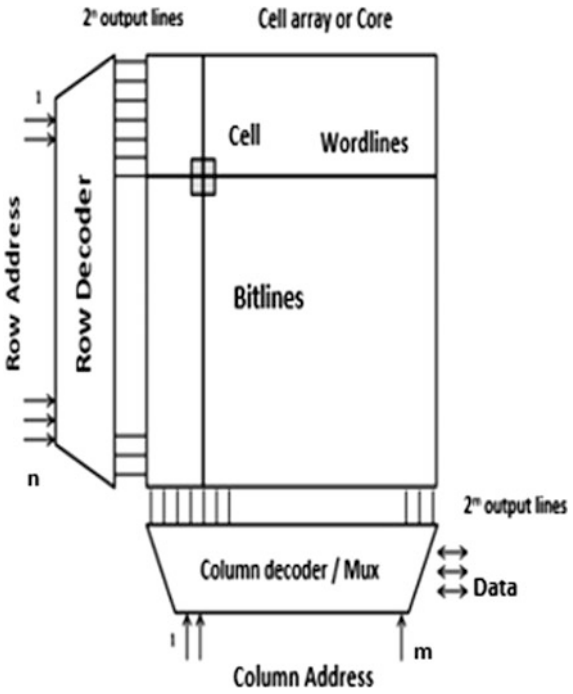


Fig. 1 Memory array

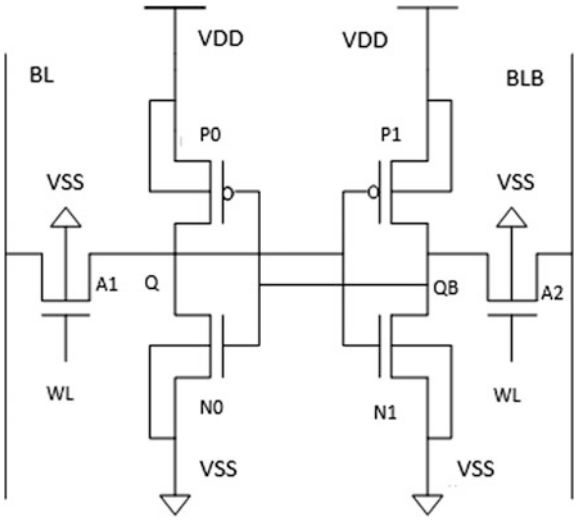


Fig. 2 Conventional 6T SRAM cell

During the read operation, both the bitlines are pre-charged to V_{DD} or logic '1'. When WL is turned on, there is a discharge to V_{SS} depending on the charge at storage nodes generating a voltage difference between the two lines. The sense amplifier senses this difference and gives the value of stored bit at its output. For

example, if the data stored at Q is '0', BL would discharge to V_{SS} through the transistor N_0 and BLB remains at '1' thus creating a voltage difference which can now be sensed.

When a read operation is performed, the data may get affected by the external noise during this direct data-read-access mechanism of a standard 6T SRAM circuit (destructive read).

Also, in order to maintain the data stability and functionality of a 6T SRAM cell in low-voltage regime, there are strict constraints on the sizing of transistors [2]. The current conducting capability of N_0 and N_1 must be higher as compared to the access transistors A_1 and A_2 for a better read stable mechanism. Similarly, the current conducting capability of A_1 and A_2 must be stronger as compared to P_0 and P_1 for better write stability. These necessities can be fulfilled by stringent sizing of transistor. Thus, new configurations are being explored for the SRAM cell.

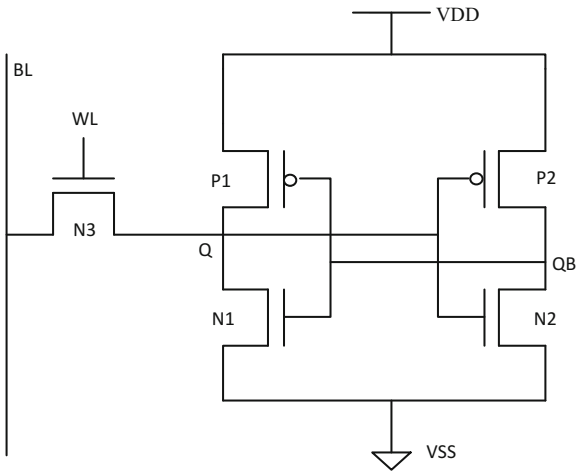
3 Previous Bit Cell Designs

Numerous cell designs have been previously proposed as improvements to the 6T SRAM cell reliability. These designs are based on numerous cell configurations to achieve the read stability.

5T SRAM [3] uses asymmetric sizing to significantly improve read stability versus 6T on the cost of inferior writability. It also proposes the benefits of the 5T relative to the 6T improve with process scaling, Fig. 3.

The design [4] uses cross-coupled inverters as storage unit and single bitline with one NMOS write access and two NMOS as read access transistor. It uses one word line and one read line Fig. 4. The design achieves lower power consumption and better SNM.

Fig. 3 5T SRAM



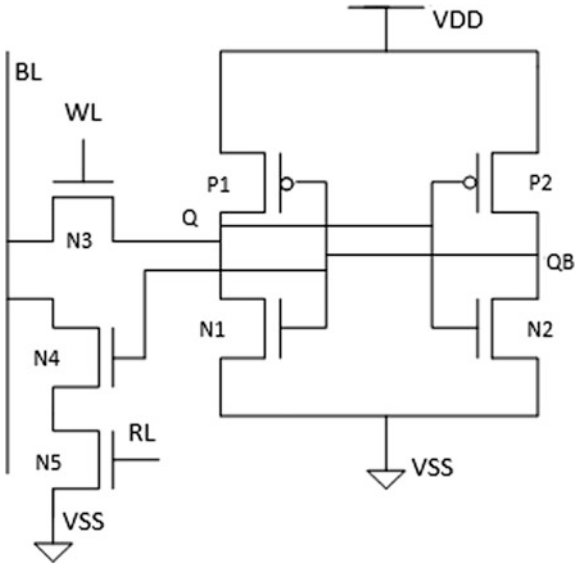


Fig. 4 7T SRAM

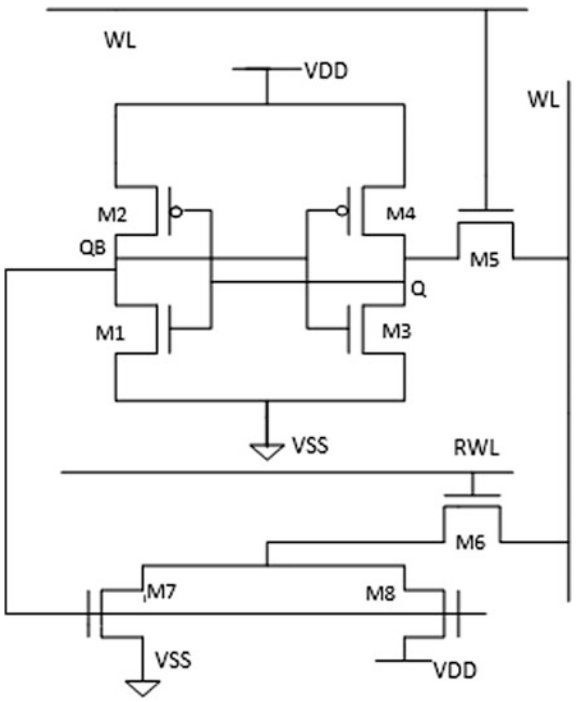


Fig. 5 8T SRAM

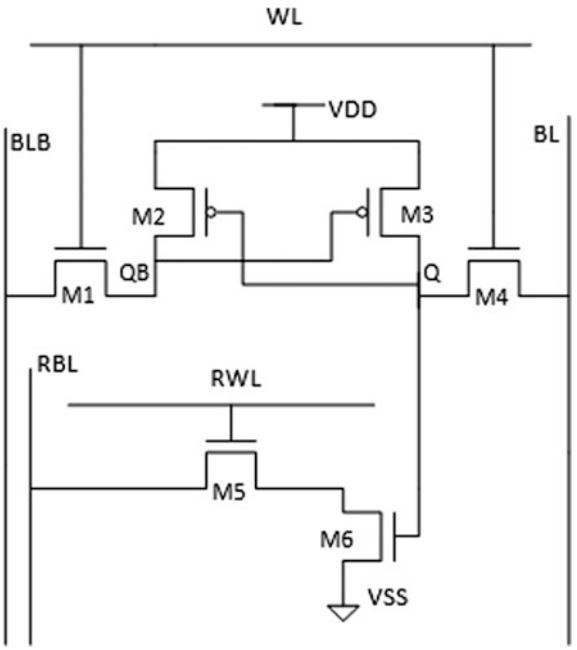


Fig. 6 6T SRAM

Another design [5] uses cross-coupled inverters, single bitline with one NMOS write access and three transistors as read access transistor. It has 1 word line and 1 read line Fig. 5. The design achieves higher read SNM with a tradeoff of power consumption.

The design [6] has a 6T configuration which uses the bit cell in with additional read port [7]. This design gives faster access and has a comparable area to that of 6T, Fig. 6.

4 Proposed Design

The proposed design uses a buffer formed by N_0 and P_0 as a storage unit with node Q storing the bitline input. The write bitline (WBL) has NMOS, N_1 as access transistor, and read bitline (RBL) has two NMOS as access transistors N_2 which is connected to read line (RWL) and N_3 which is connected to Q, Fig. 7.

4.1 Design Consideration

The proposed bit cell design is 5T SRAM with dual data access port and dual word line. We considered a buffer P_0–N_0 as our storage node. The data access lines

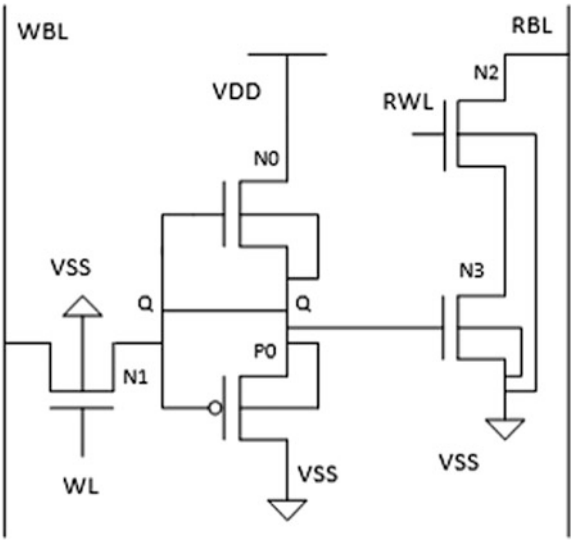


Fig. 7 Proposed 5T SRAM

namely WBL and RBL are for write data and read data, respectively. The bit cell is accessed through the word line, WL for write and the read line, RWL for read operation.

The write port, WBL, is connected to the storage node Q via NMOS access transistor N_1 with word line (WL) as its control input. Similarly, the other end is the read port with RBL connected to storage node via a N_2 and N_3 transistor with read line (RWL) as control input.

4.2 Write Operation

During write operation, when data to be written has been placed on the WBL by write circuitry and now has to be written into, the cell can be accessed by taking the word line WL at logic '1'. This turns the write access transistor, N_1 on. While write operation, in order to reduce the static power consumption, RBL and RWL are kept at logic '0' and thus read access transistors N_2 is off. The state of N_3 depends on the data previously stored in the bit cell. If the data on node Q is '0' previously then N_3 is off during write, or if the data on Q was '1' N_3 is on. Data is transferred to node Q through N_1.

If the data to be stored is '0', that is WBL = '0', initially Q = '1', and the pull-up N_0 is on. When the WL is turned on, data at WBL is transferred to node Q making it '0' and pull-down P_0 is turned on as shown in Fig. 8.

Similarly for writing logic '1', that is WBL = '1', initially Q = '0', and the pull-down P_0 is on. When the WL is turned on, data at WBL is transferred to node Q. So now Q = '1' and pull-up N_0 is turned on depicted in Fig. 9.

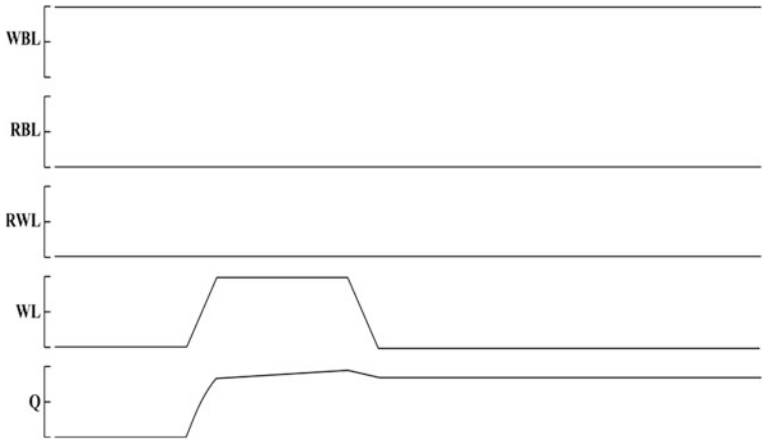


Fig. 8 Proposed bitcell: write 0

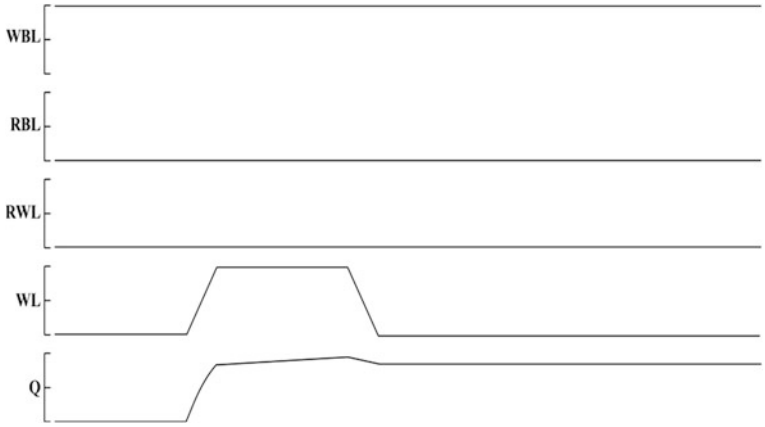


Fig. 9 Proposed bitcell: write 1

4.3 Read Operation

During read operation, data is to be read out of the cell. RBL is pre-charged to V_{DD}. And it discharges to V_{SS} or holds steady at V_{DD} depending on the data in the cell. WBL and WL are held at '0' during read. The cell is accessed by taking the read line RWL to logic '1'. This turns N_2 on and the data can now be read out. The transistor N_3 here either lets the RBL discharge or hold at V_{DD} according to the data in storage node Q. The sense amplifier thus is such that it compares the value with a reference voltage and gives the required output.

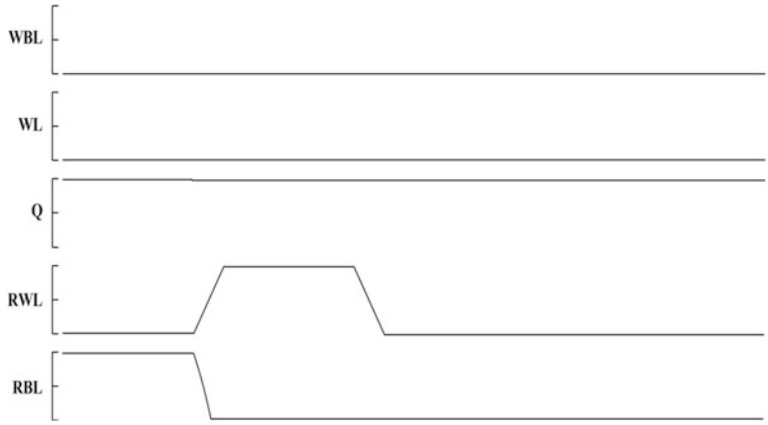


Fig. 10 Proposed bitcell: read 1

If the data to be read is '0', Q = '0' and the pull-down P_0 is on and N_3 is off. When the RWL is taken to logic '1', N_2 turns on. And RBL holds at V_{DD}.

Similarly for reading '1', Q = '1' and the pull-up N_0 is on and also N_3 is on. When the RWL is turned on, the voltage at RBL discharges to V_{SS} through N_2–N_3, and the operation is shown in Fig. 10.

5 Sense Amplifier

A sense amplifier works by sensing a relatively small difference between the voltages of the two bitlines, then amplifying the difference at the output to show if a cell is storing either a logic 1 or 0 [1, 8, 9].

5.1 Considered Designs

We considered a differential voltage amplifier as shown in Fig. 11. The amplifier is composed of a differential pair (transistors N_1 and N_2) with an active current mirror load (P_1 and P_2) and a biasing current source (N_3). We considered the read bitline, RBL as one input and other input as reference voltage V_{ref}. The reference voltage V_{ref} is taken as half of the supply voltage. The differential sense amplifier is commonly used because it is simple and reliable [10, 11].

As the bitline discharges during the read 1 operation, the sense amplifier will sense the difference between the inputs and accordingly gives the desired outputs which are complementary to each other as soon as the sense enabled is on. But during read 0 operation, due to leakage, the high and low logics are not obtained at

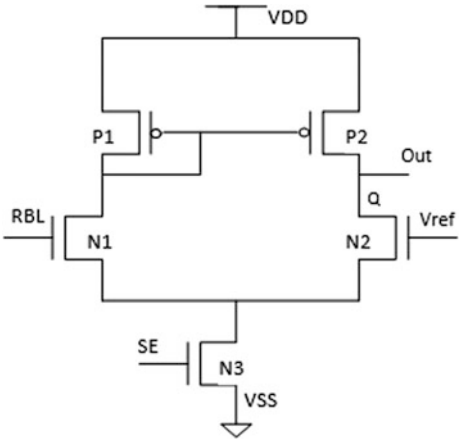


Fig. 11 Differential voltage sense amplifier

the output. Also, at the low technology node, the short channel effects also play an important role in deciding the transistor sizing and getting the required output. Therefore, we moved to latch-type voltage sense amplifier.

This design combines aspects from the latch-based voltage mode sense amplifier and the differential pair amplifier as shown in Fig. 12.

Here too, we considered one input as read bitline, that is, RBL and other as reference voltage, V_{ref}. When the amplifier is off, the signal SE is at a logic low.

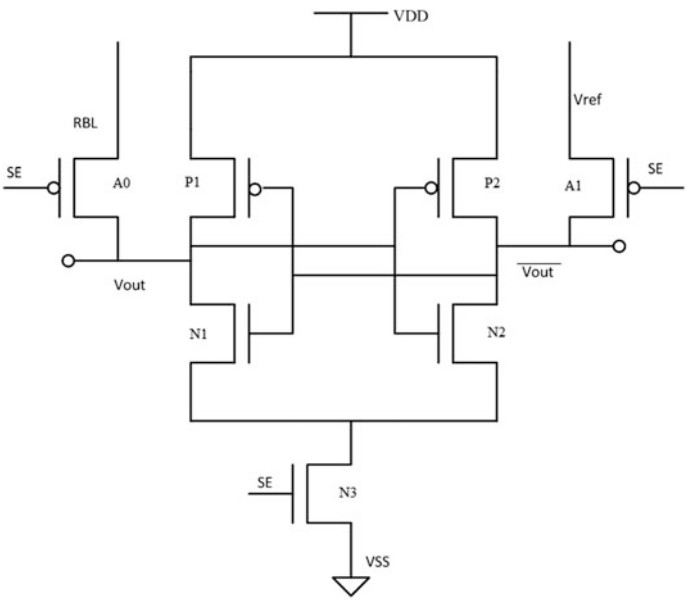


Fig. 12 Latch-type voltage sense amplifier

This turns on the reset transistors A_0 and A_1, clearing the previous latched value. When the sense amplifier is enabled, the reset transistors turn off, and the current source transistor turns on, causing the current to flow through each half of the amplifier. Since the sense amplifier is asymmetric, so the channel widths are chosen accordingly to meet the desired results.

The bitline that is discharging causes the corresponding transistor's gate voltage to drop, which decreases the current flowing through that side of the amplifier and causes the voltage to rise. This causes the amplifier to latch, which stops the static flow of current and displays a valid value at the output.

6 Decoder Design

The considered 5:32 decoder is a 2 stage, active HIGH static decoder consisting of NAND, NOR, and NOT gates [12]. The block diagram is as shown in Fig. 13. The first stage is a pre-decoding stage, in which two pre-decoder circuits are used. The pre-decoder circuit is a simple 2:4 NAND decoder. The pre-decoding at first stage results into 8 intermediate outputs from O_0 to O_8. In the second stage, 32 3-input pseudo-NOR gates are used. The input to the second stage is a combination of outputs from first stage along with the highest order bit in 4 and its inverted output.

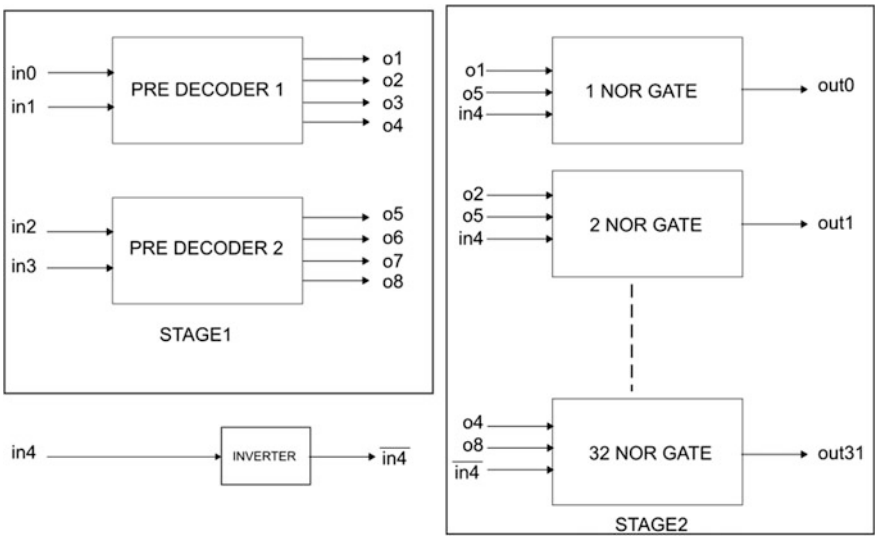


Fig. 13 Block diagram of 5:32 decoder

7 Simulation Results

7.1 Bit Cell Simulation Results

The SRAM characteristics that were calculated for proposed design and 6T SRAM cell are I_{on}, I_{off}, access times, RNM, power consumption. The simulation results for bit cell are in Table 1.

The read noise margin of the proposed design is excellent, that is, as compared to the RNM of 6T SRAM cell. The proposed design is not affected at all by presence of noise during read operation as other port is cut off from the storage nodes.

7.2 Sense Amplifier Simulation Results

The simulation results for sense amplifier are in Table 2.

Table 1 Simulation results for bitcell

Parameter	5T SRAM	6T SRAM
Access delay		
Write 1	21.364 ps	25.437 ps
Write 0	3.451 ps	11.64 ps
Read 1	674.522 fs	7.316 ps
Read 0	NA	7.316 ps
On-current (A)		
$Q = 1$	2.89×10^{-6}	7.75×10^{-5}
$Q = 0$	2.89×10^{-6}	7.75×10^{-5}
Off-current (A)		
$Q = 1$	7.27×10^{-11}	1.31×10^{-9}
$Q = 0$	7.27×10^{-11}	1.31×10^{-9}

Table 2 Simulation results for sense amplifier

Parameter	Differential voltage sense amplifier	Latch-type voltage sense amplifier
Access delay		
Read 1	141.914 fs	2.77 ps
Read 0	9.7 ns	62.87 ps

Table 3 Simulation results for decoder

Parameter	Value
T_{PLH}	59.90874 ps
T_{PHL}	158.47458 ps
Propagation delay, T_{PD}	109.191 ps
No. of transistors	170

7.3 Decoder Simulation Results

The simulation results for decoder are in Table 3.

8 Conclusion

The proposed 5T bit cell achieved excellent RNM while achieving better access time than the conventional 6T cell. Write 1 operation achieved a rise of 16%, while write 0 and read 1 are better than 6T by 70 and 90%, respectively. Out of both the sense amplifiers, differential sense amplifier was found to give a better access time. The decoder design considered a pseudo-NOR architecture which achieved a propagation delay of 109.191 ps.

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Design and Verification of Memory Controller with Host Wishbone Interface

Dinesh Katuri and S. Umadevi

Abstract This paper presents the design of Wishbone compliant memory controller which behaves as interface between processor and memory. Memory controller is a digital circuit which manages the flow of data to and fro from the processor to the memory. Instead of processor handling all the read and write operations into the memory, it allocates its work to memory controller so that processor can do some other work during the same time. This in turn leads to increase processor's performance. The memory controller used in this work supports synchronous static random access memory (SSRAM), synchronous dynamic random access memory (SDRAM), and synchronous chip select device. It also deals with the verification and functional coverage of the controller. The design part has been done using Xilinx ISE tool, and the verification part has been done using Mentor Graphics Questa Sim 10.0b.

Keywords Memory controller · Wishbone interface · Design · Verification SSRAM · SDRAM · Synchronous chip select device

1 Introduction

Memory controller is a digital circuit designed in order to reduce the microprocessor's extra effort in writing and reading into the memories [1]. Processor configures the memory controller to do its job of writing and reading from memories [2]. The memory controller architecture uses the Wishbone interface in order to communicate from different types of memories like SSRAM, SDRAM, and

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synchronous chip select devices. The detailed explanation of the architecture, design, and the verification of the memory controller is discussed in this paper. The design has several features such as supporting different types of memories, eight chip selects which are uniquely programmable, flexible timing accommodation for different types of memory devices, supporting up to 8 * 64 MB memory size, comfortable read and write operations from different types of memory devices [1]. The verification part includes verifying the read and write transactions targeting different memories connected to different chip selects [2]. The design part is coded using Verilog HDL, and the verification part is coded in System Verilog HDL.

The paper is organized as follows: Sect. 2 describes the literature survey. Sections 3 and 4 say about the architecture of the memory controller and its design requirements. Section 5 depicts the memory timing configuration. Section 6 describes the configuration and status registers. Section 7 deals with the final design implementation, design summary, timing details, and RTL Schematic of the memory controller design. Section 8 explains about complete verification flow of the memory controller. Sections 9 and 10 deal with results discussion and conclusion.

2 Traditional Implementation Details of the Memory Controller

Memory Controllers are implemented based on the type of the memory it supports [3]. The main intension of implementing the memory controller is to increase the performance of the processor [4]. The memory controllers are implemented for different memory technologies. Based on the memory technologies, it is important to build a memory controller in order to handle the memories with different technologies [5]. All the previous works on implementing memory controller are done based on the type of the memory technology and their enhancements. The papers on DDR memory controllers and NAND flash controllers support single memory with different bus interfaces [3, 4, 6].

The verification done previously on these implementations is either using Verilog or by FPGA kits [7]. This paper deals with verification of the memory controller supporting different memories like SDRAM, SSRAM, and synchronous chip select devices using System Verilog HDL. The interface used in this paper is of Wishbone-type interface which makes SoC and design reuse easy by creating a standard data exchange protocol [8]. The main advantage of using Wishbone interface is due to its simplicity and compactability. The verification done using System Verilog HDL gives a lot of flexibility to create verification environment and also provides confidence building parameters to verify the design completely.

3 Memory Controller Architecture

The architecture of the memory controller is shown in Fig. 1, and the functioning of each and every block present in the architecture is discussed in this section.

3.1 Refresh Controller

SDRAMs are to be refreshed periodically in order to prevent data loss. The main functionality of this block is to generate refresh cycle requests for SDRAM's periodically. Until the request for the refresh is done, the refresh request signal will be HIGH and once it is done the refresh ACK signal becomes HIGH. All the SDRAMs which are connected to the memory controller has to be refreshed by the shortest time among all [1].

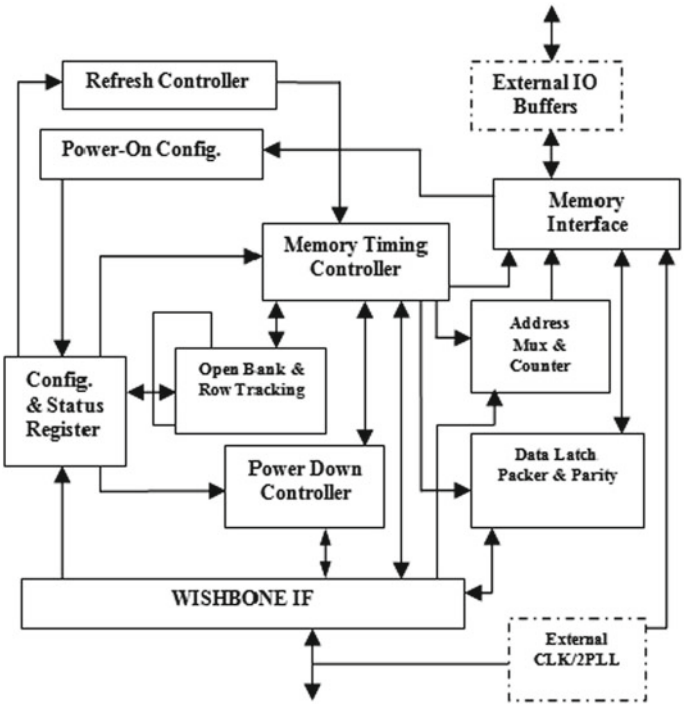

Fig. 1 Memory controller architecture

3.2 Open Bank and Row Tracking

The main function of this block is to remember which bank is open and which row is open at the specified time interval. It allows fast accessing to the bank and rows which are already opened [1].

3.3 Address Mux and Counter

The main functionality of this block is to generate addresses to the memory devices which are connected to the memory controller such as SDRAMs, SSRAMs, and synchronous chip select devices. Based on memory connected to the chip select by the configuration register, the proper address to the memory device connected is selected [1].

3.4 Configuration and Status Registers

The main functionality of this block is to hold the entire information of all the registers present in the memory controller. This block also helps in actual decoding of the chip selects.

3.5 Power on Configuration

The function of this block is to latch the value available in memory data bus during RESET. The initial configuration of the memory controller is determined by the value latched.

3.6 Data Latch, Packer, and Parity

The main function of this block is to establish connection between the memory bus and the Wishbone bus. The data which goes out to the memory controller is latched at appropriate times, and the data which is read from the memory controller is done either by latching the data to the Wishbone bus or the data goes through a data packet first. The role of data packer is to assemble a 32-bit word from 16- or 8-bit wide devices on the memory bus.

3.7 Memory Timing Controller and Memory Interface

The main functionality of memory timing controller block is to manage memory timing and control for different memories. This is done by configuring each register. It also generates control signals for memories based on controller configuration register [1], and the main functionality of memory interface block is to provide synchronization for inputs and outputs.

4 Memory Controller Design Requirements

4.1 Wishbone Interface

The Wishbone interface is a general purpose interface used to connect two core modules. The main purpose of using this interface is to achieve the decoding functionality of the two modules easily with less complexity. It is flexible to reuse and can be easily understood by the developer and an end-user [8]. Table 1 shows the various signals with their description involved in the Wishbone interface. Few features of the interface are it supports structured design methodologies used by large project teams and full set of popular data transfer bus protocols including READ/WRITE cycle, burst transfer cycle, read modify write (RMW) cycle. This interface also provides modular data bus widths and operand sizes for proper synchronization.

Table 1 Wishbone interface signal description

Name	Width	Direction	Description
clk_i	1	I	Wishbone clock input
rst_i	1	I	Wishbone RESET input
wb_addr_i	32	I	Address input
wb_data_i	32	I	Data input
wb_data_o	32	O	Data output
wb_sel_i	4	I	Indicates which bytes are valid on the data bus
wb_we_i	1	I	Input for slave. Indicates write cycle
wb_cyc_i	1	I	Input for slave. Encapsulates a valid transfer cycle
wb_stb_i	1	I	Input for slave. Indicates valid transfer cycle
wb_ack_o	1	O	Acknowledgment output. Indicates a normal cycle termination
wb_err_o	1	O	Error acknowledgment output. Indicates abnormal cycle termination

4.2 Memory-Specific Requirements

Memory controller designer needs to figure out the memories it should support. For example, in this design, it has to support SDRAM, SRAM, and synchronous chip select device. Each memory has specific requirements as listed below.

SSRAM specific requirements:

- SSRAM access is word accessing-based access.
- Memory controller should generate addressing in word format.
- Memory controller should take care of read delay cycles.

SDRAM specific requirements:

- Has to generate periodic refresh cycles [9, 10].
- Generate row and column address for the current bank.
- Timing has to be compatible with memory being targeted [9].

Synchronous chip select device requires:

- To target command registers in the synchronous device to read/write memory contents.
- Memory controller should generate write/read to command registers.

5 Memory Timing Configuration

Memory timing is defined using Timing Select Register (TMSn). Each memory type has different meaning for TMSn register. The timing register of each memory type has to be configured first to perform the operations on particular memory [1]. For this, the timing details of different memories are described below.

5.1 SDRAM Timing Configuration

SDRAM commands typically required the following

- Activate command: In this both bank address along with row address is given.
- Pre-charge command: In this the opened row is closed.
- Transaction command: In this write/read transaction to memory happens.

The signals involved in the SDRAM are row address strobe (RAS), column address strobe (CAS), bank address (BA), write enable (WE), clock enable (CLKE). SDRAM may be operated in two modes one is keeping the current row open as shown in Fig. 2. In this, after the initial active command, subsequent access to the same row need not have to go through activation cycles again and again [9].

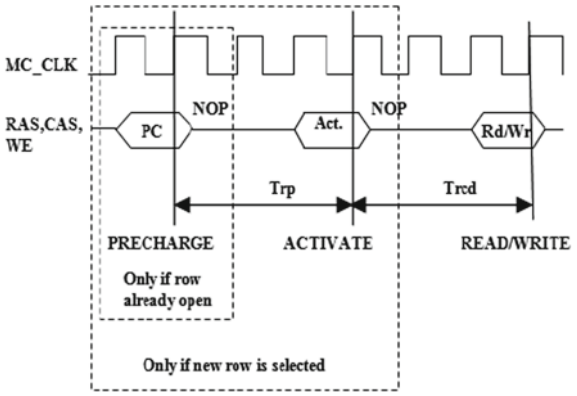

Fig. 2 Keep row open SDRAM access

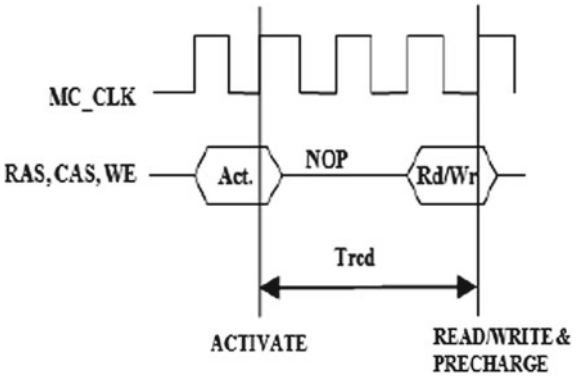

Fig. 3 Close row SDRAM access

The second one is closing the row immediately after the read or write operation is completed as shown in Fig. 3.

5.2 SSRAM Timing Configuration

For designing of the SSRAM, there is no need of extra timing parameters as that are in the SDRAM. Figure 4 shows the SSRAM write cycle. The data is valid only when MC_ADSC signal is low; MC_ADV signal is high; and MC_WE signal is low [1].

Figure 5 shows the SSRAM read phase. The data is valid only when MC_ADSC signal is high; MC_ADV signal is low; and MC_OE signal is low.

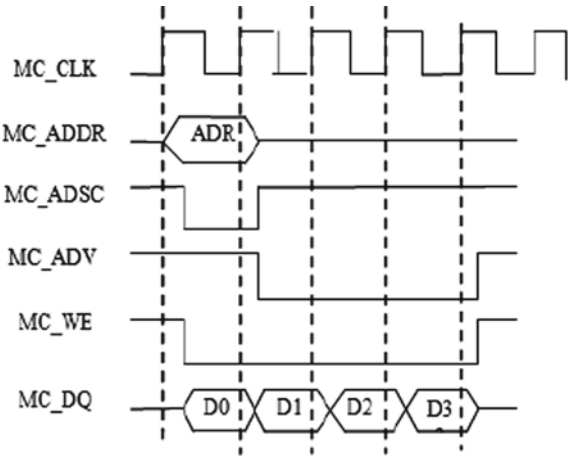

Fig. 4 SSRAM write cycle

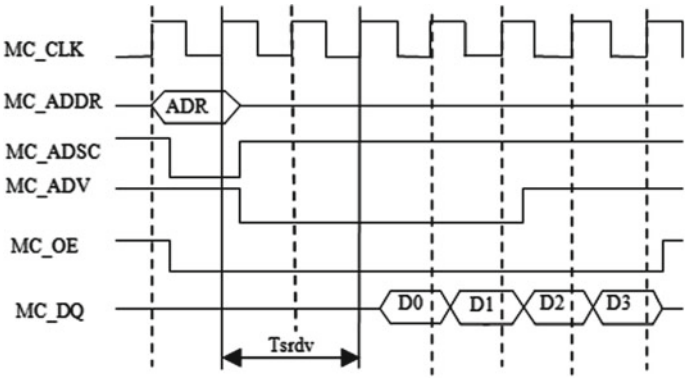

Fig. 5 SSRAM read cycle

5.3 Synchronous Chip Select Devices

Synchronous chip select devices are the devices which are synchronous to the memory controllers clock; for synchronous chip select devices, the signal ACK must be asserted for indicating the acceptance of data or providing valid data in return. Figure 6 shows the write cycle timing diagram of synchronous chip select device. The data is valid when MC_WE is active low and MC_ACK is HIGH. For read cycle, the signals MC_OE should be LOW and MC_ACK signal should be HIGH. The signal MC_CSn is the chip select signal which gives the information about the chip select for which the device has been connected [1]. Figure 7 shows the read cycle of a synchronous chip select device.

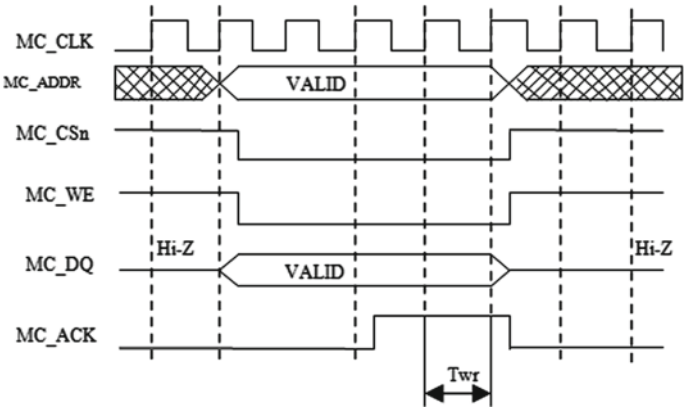

Fig. 6 Synchronous chip select device write cycle

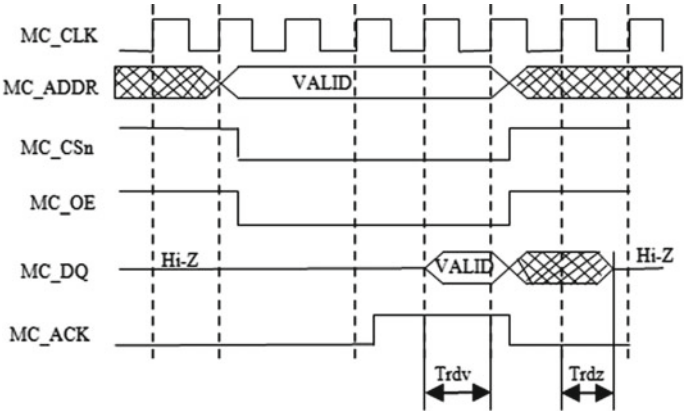

Fig. 7 Synchronous chip select device read cycle

6 Configuration and Status Registers

Configuration and status registers hold all the registers of memory controller. Few registers such as chip select configuration register (CSCn), base address mask register (BA_MASK), Timing Select Register (TMSn). All these registers have to be configured to achieve the functionality of the memory controller. All the registers hold the value based on the configuration done by the processor and functions according to the processor commands. The CSCn has to be configured eight times since there are eight chip selects in the design. Configuration of these registers tells about the address range and the type of memory connected to each chip select. Bit wise description of the chip select configuration register is shown in Table 2.

Table 2 Chip select register (CSCn)

Bit	Access	Description
31:24	RO	Reserved
23:16	RW	Chip select
15:12	RO	Reserved
11	RW	Parity enable/disable
10	RW	Keep row open
9	RW	Bank address select
8	RW	Write protect
7:6	RW	Memory size
5:4	RW	Bus width
3:1	RW	Memory type
0	RW	Chip select enable

Table 3 TMSn configuration for SDRAM's

Bit	Access	Description
31:28	RW	Reserved
27:24	RW	Trfc
23:20	RW	Trp
19:17	RW	Trcd
16:15	RW	Twr
14:10	RW	Reserved
9	RW	Write burst length
8:7	RW	Operation mode
6:4	RW	CAS latency
3	RW	Burst type
2:0	RW	Burst length

Similar to CSCn registers, the TMSn registers has to be configured, but the configuration of TMSn registers is different for each memory device; hence, the timing parameters for each memory are different. Table 3 describes the TMSn configuration for SDRAMs.

For SSRAM, there is no meaning for TMSn register; hence, all the values are fixed and are predefined based on the timing diagrams related to SSRAM. For synchronous chip select devices, the TMSn register is responsible to hold the internal counters, memory bus clock responsible to clock all the internal counters. It also maintains the time required for accessing various parameters. Table 4 describes the TMSn parameters for synchronous chip select devices.

Table 4 Synchronous chip select device TMSn parameters

Bit	Access	Description
24:16	RW	Tto determines maximum time MC has to wait for mc_ack to be asserted
15:12	RW	Twr determines 4-bit write pulse width counter value
11:8	RW	Trdz determines 4-bit read to high z counter value
7:0	RW	Trdv determines 8-bit read to data valid counter value

7 Final Design Implementation, Timing Details, and Design Summary

Figure 8 shows the final design implementation inputs and outputs of the memory controller.

Figure 9 shows the design summary of the final design.

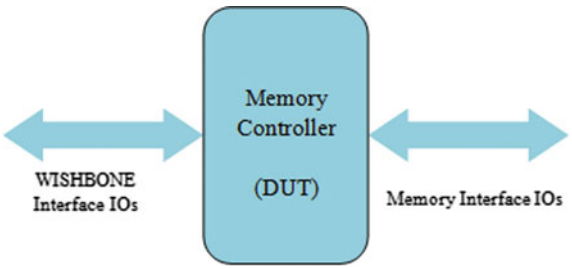

Fig. 8 Final design implementation

mc_top Project Status (11/18/2015 - 15:23:22)			
Project File:	memory_controller_design.xise	**Parser Errors:**	No Errors
Module Name:	mc_top	**Implementation State:**	Synthesized
Target Device:	xc3s100e-4cp132	**• Errors:**	No Errors
Product Version:	ISE 14.3	**• Warnings:**	328 Warnings (294 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1876	960	195%
Number of Slice Flip Flops	1729	1920	90%
Number of 4 input LUTs	2741	1920	142%
Number of bonded IOBs	267	83	321%
Number of GCLKs	3	24	12%

Fig. 9 Design summary

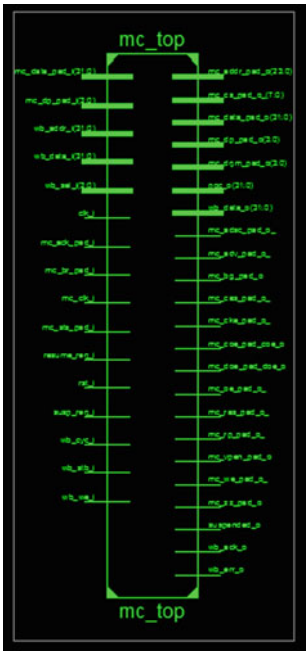

Fig. 10 Final design RTL schematic

The total timing delay in nanoseconds is obtained as 12.756 ns. The RTL Schematic for the final design is shown in Fig. 10.

8 Memory Controller Verification Flow

The most important part after designing is the verification of the design. The verification plays a major role in verifying each and every feature related to the design and has to possibly cover the entire design to detect the bugs. In short, verification is nothing but verifying all the features of the design. Figure 11 shows the detailed verification flow of the memory controller [11].

8.1 Features Listing Down

Feature listing down is the first thing to start with for verification, for example. MC supports different types of memories is a feature and it is verified by targeting each and every memory, i.e., SDRAM, SRAM, and synchronous chip select device for write and read operation.

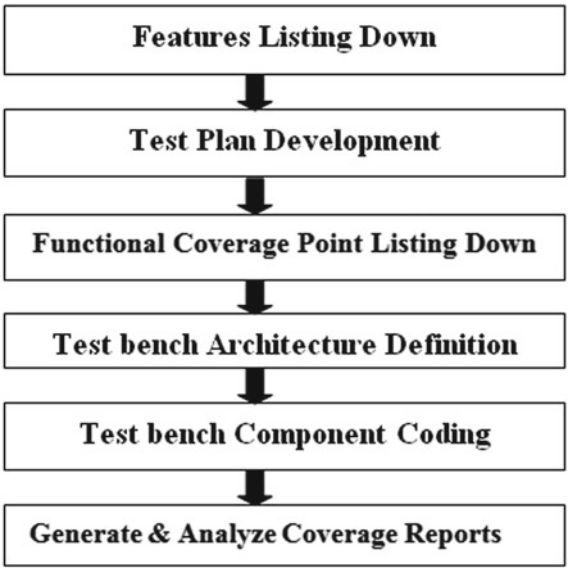

Fig. 11 Memory controller verification flow

8.2 Test Plan Development

It is all about developing the plan for what are the things to be verified and listing down all the things that are needed for the design to be verified. Table 5 shows some of the features of the memory controller and the testcase flow required to verify particular feature.

8.3 Functional Coverage Point Listing Down

Functional coverage says "how much coverage is done?" or "how much the design is verified?" or "how many features of the design are still now verified?" The main

Table 5 Test plan development

No.	Feature	Scenarios	Test case flow
1	Targeting registers	Register default values	1. Apply RESET 2. Read all registers 3. Compare the default values with expected
2	Targeting registers	Register write/read	1. Apply RESET 2. Write to all registers 3. Read all registers 4. Compare the read values with write values

(continued)

Table 5 (continued)

No.	Feature	Scenarios	Test case flow
3	Chip select CS0 SSRAM	CS0 enable with SSRAM	1. Connect SSRAM to CS0 2. Apply RESET 3. Configure corresponding registers for CS0 SSRAM 4. Perform write/read to CS0 5. Compare the write and read data
4	Chip select CS0 SDRAM	CS0 enable with SDRAM	1. Connect SDRAM to CS0 2. Apply RESET 3. Configure corresponding registers for CS0 SDRAM 4. Perform write/read to CS0 5. Compare the write and read data
5	Chip select synchronous chip select device	CS0 enable with synchronous chip select device	1. Connect synchronous chip select device to CS0 2. Apply RESET 3. Configure corresponding registers for CS0 SDRAM 4. Perform write/read to CS0 5. Compare the write and read data
6	All Chip selects connected	Each CS connected to different memory	1. Connect different memories to each chip select 2. Apply RESET 3. Configure corresponding registers for different memories 4. Perform write/read to different memories 5. Compare the write and read data

and important advantage of the functional coverage is that it helps us in writing some meaningful test cases (what are the features left out?).

8.4 Test Bench Architecture Definition

This defines the overall architecture of the verification of the memory controller and is shown in Fig. 12. In real life, the memory controller will be driven by the processor, but a processor is typically replaced with bus functional model (BFM) and a generator, assumption is that both play the role of a processor.

The generator component generates stimulus to the DUT. The generated stimulus is in random nature based on the test case given. For simple memory, stimulus generator generates read and write operations. The bus functional model (BFM) for a device interacts with the DUT by both driving and sampling the DUT signals. A bus functional model is a model that provides a task or procedural interface to specify certain bus operations for a defined bus protocol.

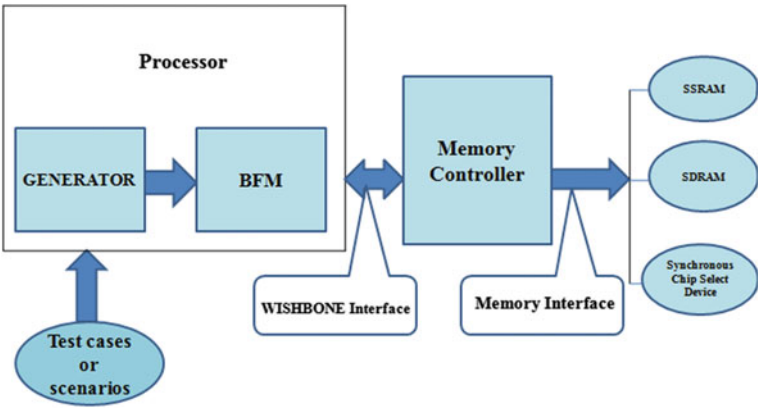

Fig. 12 Test bench architecture for verification

8.5 Test Bench Component Coding and Coverage Reports

The components in the test bench architecture need to be coded in order to generate coverage reports. The coverage reports generated has to be analyzed finally.

9 Results and Discussion

Verifying the Features

1. Applying the RESET and reading the default values from the resisters

Whenever the verification starts, the first thing to do is to apply the RESET signal and start reading the default values present in the design and the default values should be according to the design. Figure 13 shows the default values in all the registers; for instance, the address location 60000000'H has the data 00000000'H and is valid only when wb_ack signal is HIGH. Similarly, all the register's default data in different address locations is read. The data kept in 60000014'H and 60000008'H is FFFFFFFF'H and 000007FF'H by default.

2. Write and read to all the registers

Write Operation: It will write the values into all the registers in different address location and check whether the write data is matching with the read data. Figure 14 shows the write operation performed on all the registers, the operation of write and read is given by "wb_we" signal if its value is high indicates write operation otherwise it is read operation. The data in the address location 60000008'H is valid only when "WB_ACK" signal is HIGH and is 000000D2'H. For the read operation,

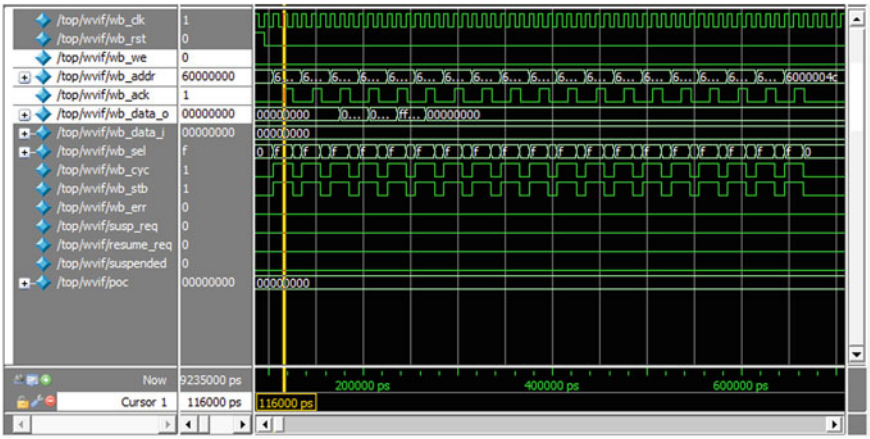

Fig. 13 RESET, reading the default values from the registers

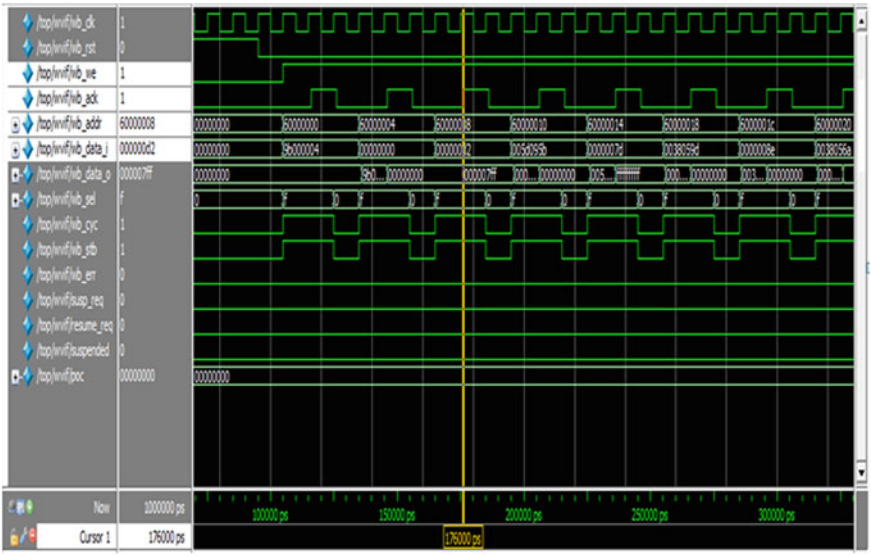

Fig. 14 Write operation to all registers

it is necessary to check the values in all registers and verify whether writing of data into all the registers exactly matches when we read those registers.

Read Operation: Figure 15 shows the read operation performed into the all the registers; the data is valid only when "wb_ack" signal is HIGH, and read operation is obtained if "wb_we" is LOW. For the address location 60000008H, the data obtained is 000000D2H which is the same date that has been written. Similarly, it is

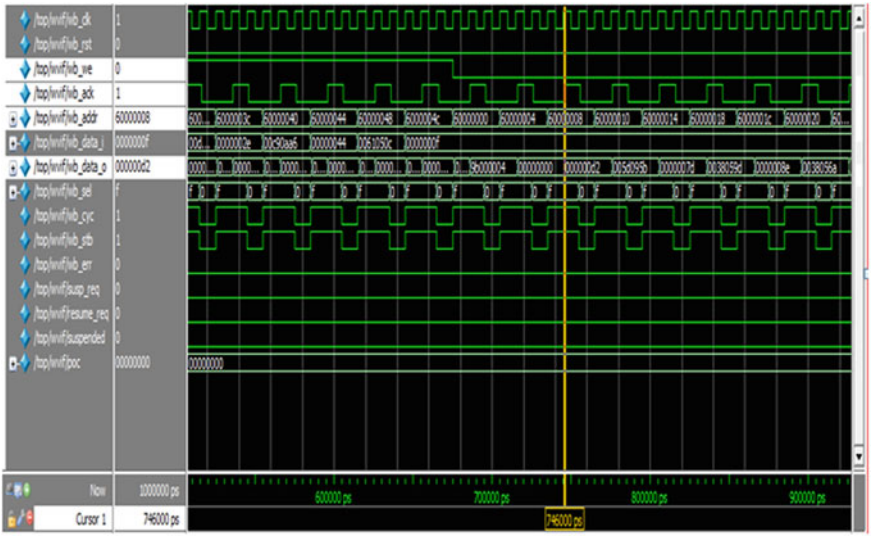

Fig. 15 Read operation from all the registers

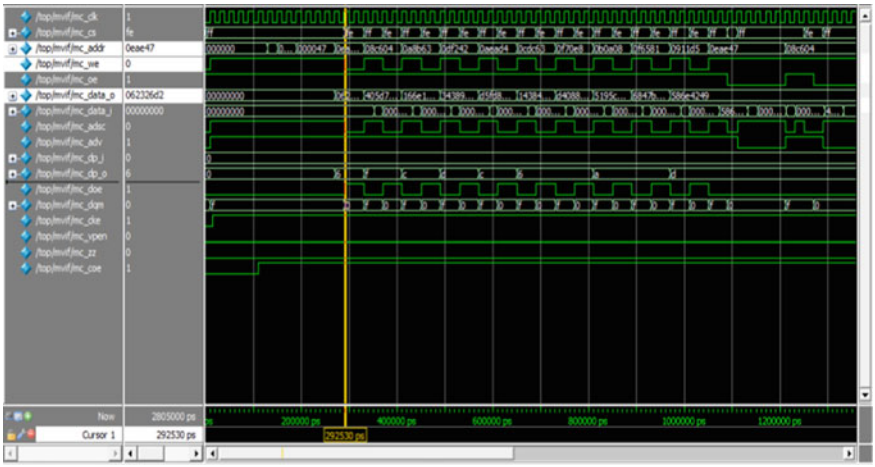

Fig. 16 Write operation to SSRAM connected to CS0

checked for the remaining registers address location and data written into them and verified whether the read data exactly matches with the write data.

3. Write and read to SSRAM connected to CS0

Write Operation: The write operation into SSRAM is shown in Fig. 16; for the write operation, MC_WE signal and MC_ADSC signals are LOW while MC_ADV

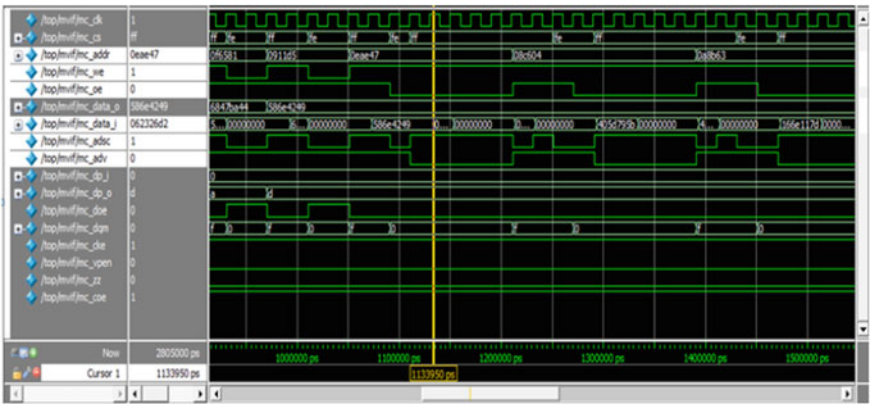

Fig. 17 Read operation from SSRAM connected to CS0

signal and MC_OE signals are HIGH, and in the address location 0EAE47'H, the data written is 062326D2'H.

Read Operation: The read operation into SSRAM is shown in Fig. 17; for the read operation, MC_WE signal and MC_ADSC signals are HIGH while MC_ADV signal and MC_OE signals are LOW, and in the address location 0EAE47'H, the data read is 062326D2'H which matches with written data.

4. Write and read to SDRAM connected to CS0

Write Operation: The write operation into SDRAM is shown in Fig. 18; for the write operation, MC_WE signal and MC_CAS signals are LOW while MC_RAS signal is HIGH, and in the address location 002442'H, the data written is 3438959D'H.

Read Operation: The read operation into SDRAM is shown in Fig. 19; for the read operation, MC_WE signal and MC_CAS and MC_RAS signals should be HIGH, and in the address location 002442'H, the data read is 3438959D'H which matches the written data.

5. Write and read to synchronous chip select device connected to CS0

Write Operation: The write operation into synchronous chip select device is shown in Fig. 20; for the write operation, MC_WE signal is low while MC_OE and MC_ACK signals are HIGH, and in the address location 08C604''H, the data written is 405D795B'H.

Read Operation: The read operation into synchronous chip select device is shown in Fig. 21; for the read operation, MC_OE signal is LOW while MC_WE and MC_ACK signals are HIGH, and in the address location 08C604''H, the data read is 405D795B'H which matches the written data.

6. Write and read to different memories connected to different chip selects

Now connect different memories in random to different chip selects, for instance, synchronous chip select device is connected to CS0; SDRAM is connected to CS3;

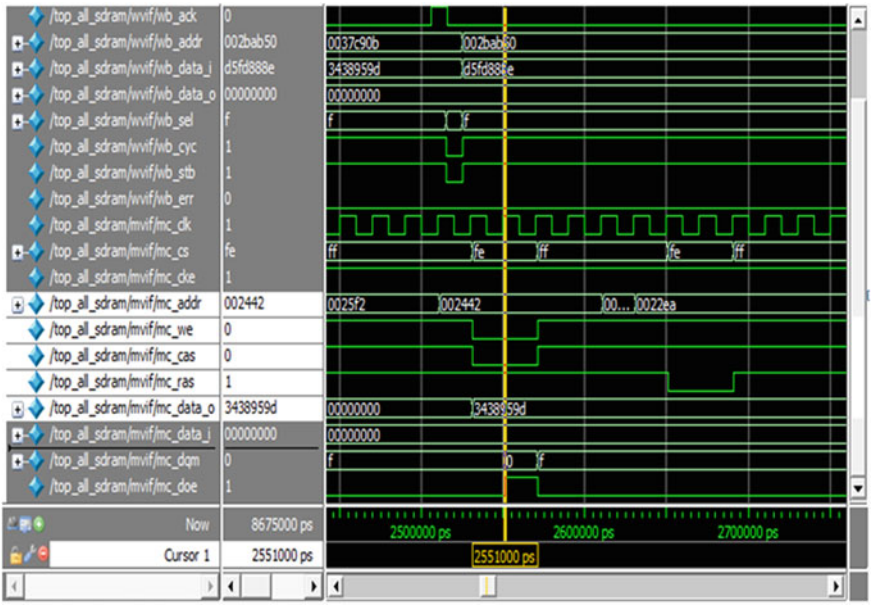

Fig. 18 Write operation to SDRAM connected to CS0

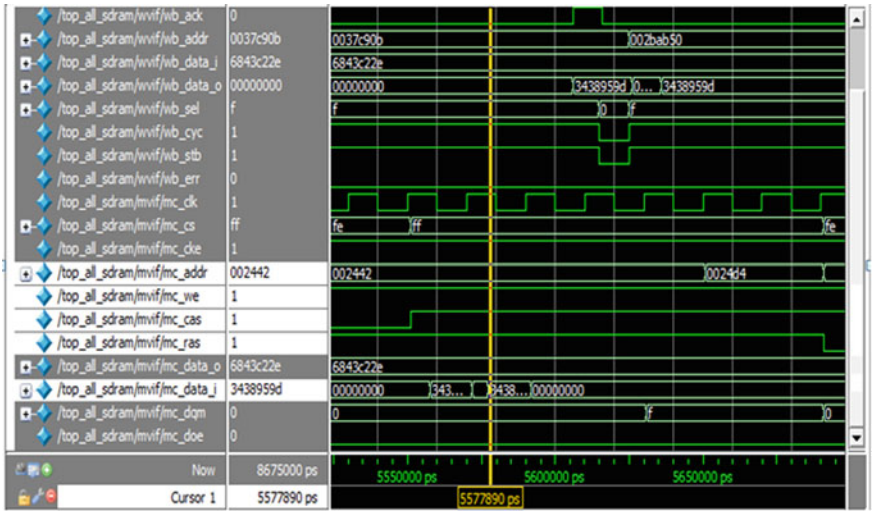

Fig. 19 Read operation from SDRAM connected to CS0

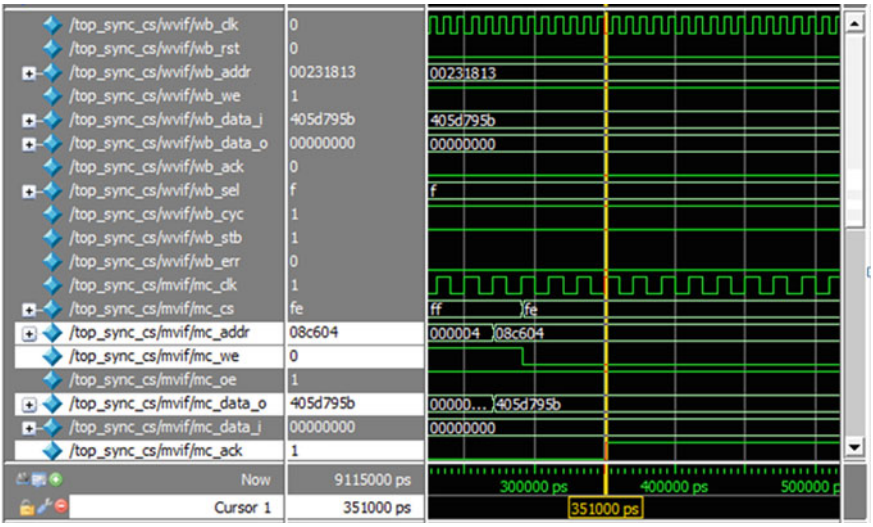

Fig. 20 Write operation to synchronous chip select device

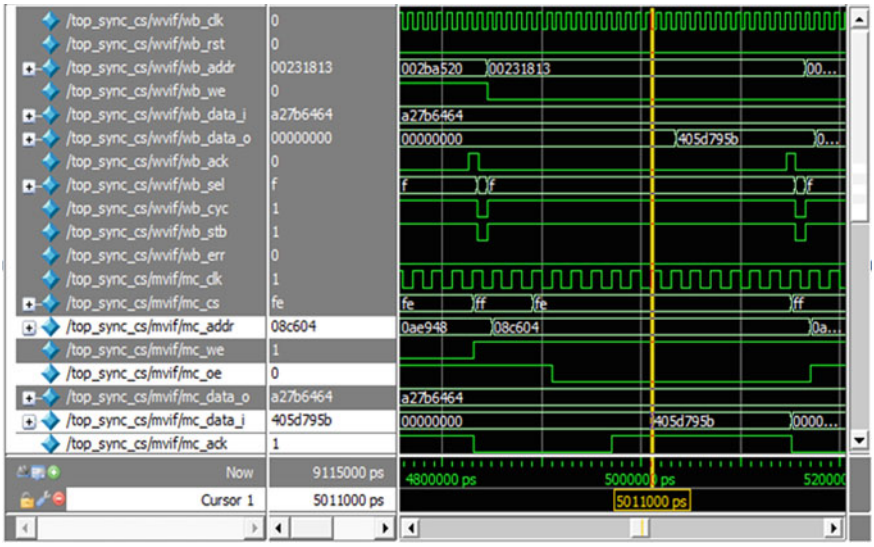

Fig. 21 Read operation from synchronous chip select device

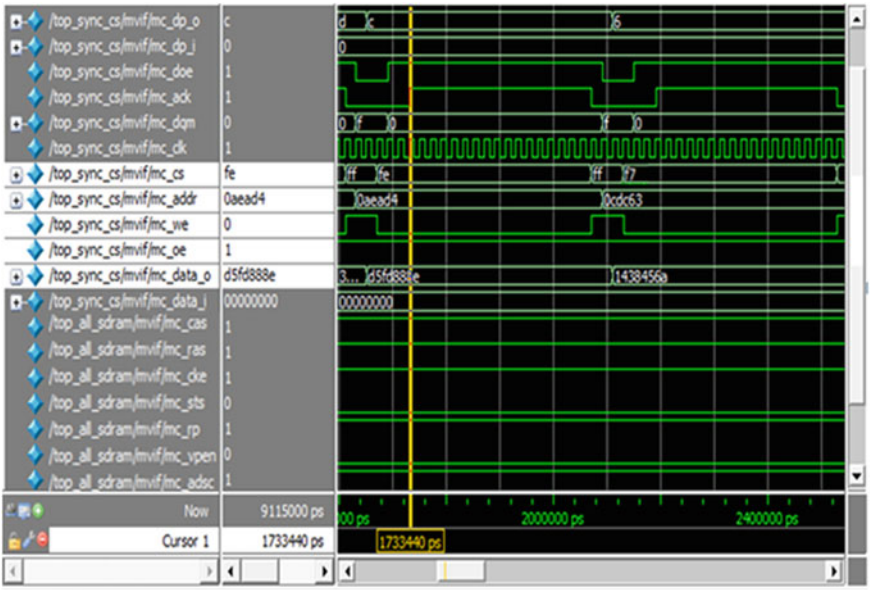

Fig. 22 CS0 synchronous chip select device write

and SSRAM is connected to CS7. Figure 22 shows the CS0 write operation. The read operation for CS0 is shown in Fig. 23, and the read data matches with the write data.

The write operation in SDRAM connected to CS3 is shown in Fig. 24. To perform this, chip select signal MC_CS signal should possess a value of F7'H.

Figure 25 shows the read operation performed from the chip select CS3.

The CS7 chip select is connected with SSRAM, and the signal MC_CS holds a value of 7F'H. Figure 26 shows the write operation performed to CS7.

Figure 27 shows the CS7 chip select read operation. The read data matches with the write data.

Functional Coverage: As 70% of the time spent on verification rather than design, it is important for the verification engineer to have certain parameters to sign off the correct functionality of the design. The design features are said to be verified based on functional coverage parameter. Figure 28 shows the functional coverage obtained for the complete verification of list of features. The 100% functional coverage indicates that all the features have been targeted successfully. The verification closing criteria are done by achieving 100% functional coverage.

The results obtained in this paper show the verification of the memory controller features. The simulation results at each stage for verifying the required feature are explained by performing write and read operations on to the memory. The verification is done using System Verilog which allows the verification engineer to specify the design behavior more concisely than previous possibilities.

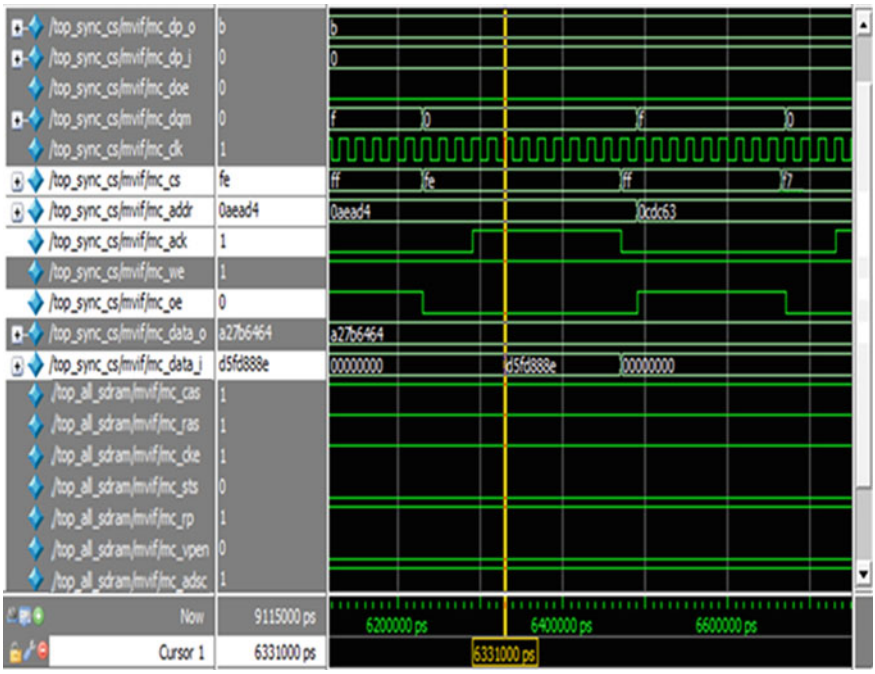

Fig. 23 CS0 synchronous chip select device read

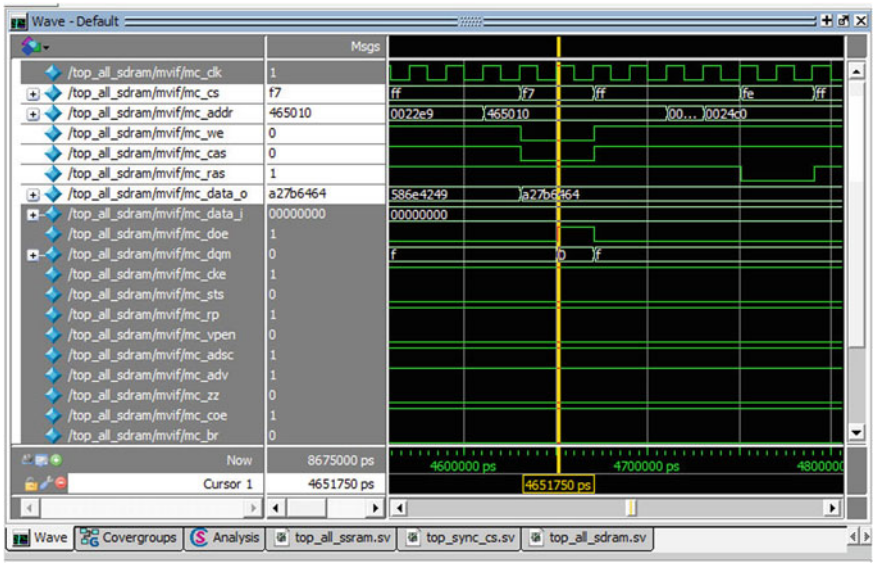

Fig. 24 CS3 SDRAM write operation

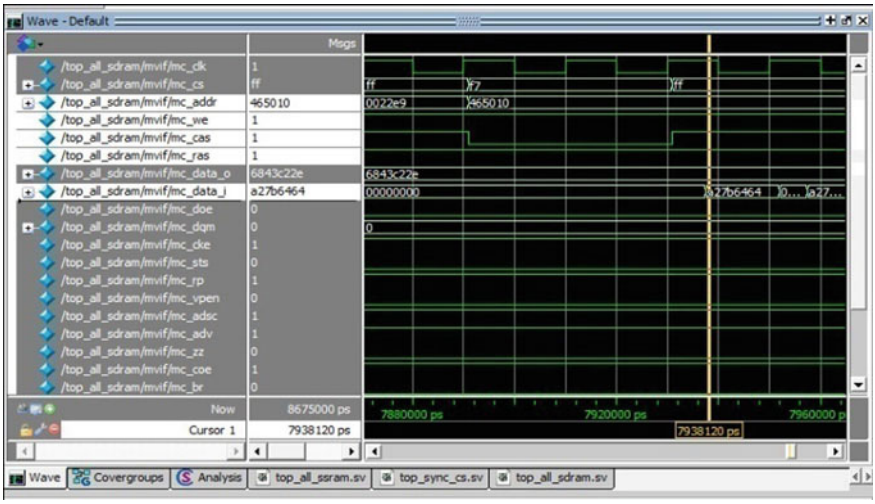

Fig. 25 CS3 SDRAM read operation

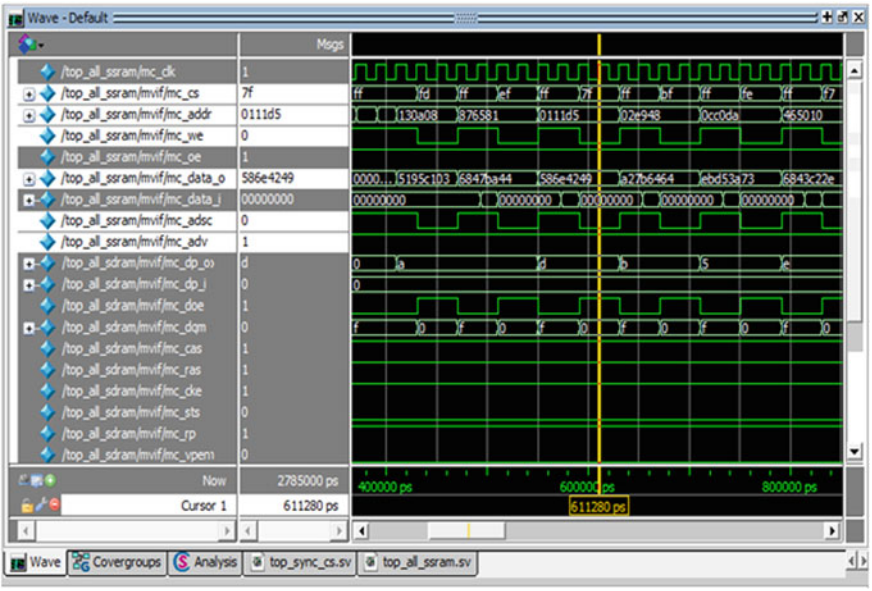

Fig. 26 CS7 SSRAM write operation

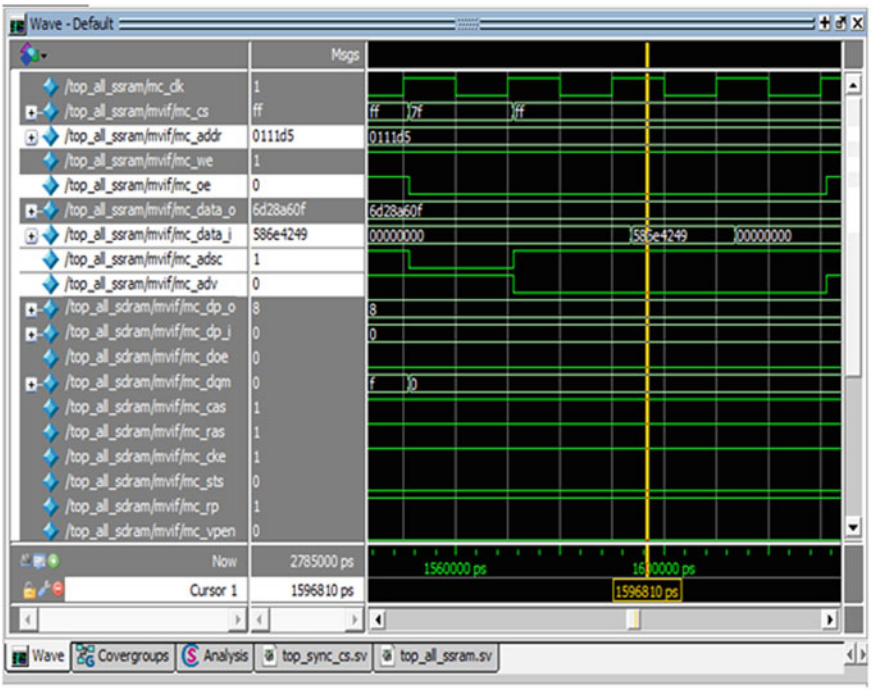

Fig. 27 CS7 SSRAM read operation

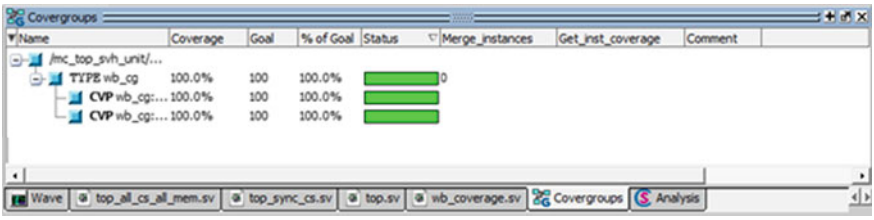

Fig. 28 Functional coverage obtained

10 Conclusion

In this paper, a memory controller having a list of features has been designed in order to reduce the extra effort to perform write and read operation by the processor. The verification part is done using System Verilog which gives a lot of flexibility to the verification engineer to target complete functionality of the design. Unlike the verification of the design by Verilog HDL, System Verilog provides advanced confidence building design sign off parameter like functional coverage. This will

help to reduce the time to market. The designed memory controller DUT in this paper gives 100% functional coverage which confirms a good verification for signing off the design.

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8-Bit Asynchronous Wave-Pipelined Arithmetic Logic Unit

Polani Rahul, Korada Prudhvi Raj and S. Umadevi

Abstract In this paper, an 8-bit asynchronous wave-pipelined arithmetic logic unit has been modified with set of 8 arithmetic and 12 logical operations. All the internal modules have been modified in order to reduce power and latency by using ASIC semi-custom design flow in cadence® environment using gpdk-180-nm technology. This modified design has achieved reduction in power by 45%, reduction in delay by 19%, reduction in area by 43%, reduction in cell count by 49% as compared to the existing ALU.

Keywords INIT · ROUT1 · ROUT2 · SUM · Wave-pipelined ALU

1 Introduction

High-performance microprocessor [1] ALUs have more switching activity on chip because of unnecessary switching of gates due to clock and clock drivers. Because of this, the ALU has most percentage of power consumption in overall power consumption of microprocessor. In order to reduce the switching activity, a new method has been employed to design an ALU, i.e., wave pipelining [2, 3].

Most of the papers have proposed ALUs based on bit-serial architectures [4], synchronous systems [5], and pipelined architectures [6]. Bit-serial architecture is the most common architecture in designing high-performance ALU because of its less architectural requirements. In bit-serial architecture, the main problem is that

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latency increases with increase in operand size. In Synchronous ALUs all the state changes depends on the clock but these types of ALUs have disadvantages with high clock skew and power consumption [3]. To overcome all these limitations, pipelined ALUs have been designed.

Existing wave-pipelined ALU [7, 8] design is based on Kogge–Stone algorithm [9], all the internal modules have been implemented by using dual-input D-flip-flop [10], toggle flip-flop, and C-gate [11], because of internal gates in all the modules the power consumption, area are high. In modified ALU, all the modules have been designed by using combinational circuits which intern reduction in power consumption, area, and gate count.

In this paper, Section C of ALU architecture deals with the implementation of internal modules of existing ALU, and Section D deals with limitations of exiting ALU internal modules and modifications done for improving the performance. Section III deals with comparison of modified ALU with existing ALU.

2 ALU Architecture

2.1 Kogge–Stone Adder

The ALU design is based on Kogge–Stone adder which performs carry-look ahead addition, and it follows Kogge–Stone algorithm [4]. The Kogge–Stone adder has lower fan-out in each stage; it increases the performance of ALU. Figure 1 is an example of 4-bit Kogge–Stone adder. All vertical stages will produce *G* (generate) and *P* (propagate) bit, where *G* tends to carry and *P* tends to sum.

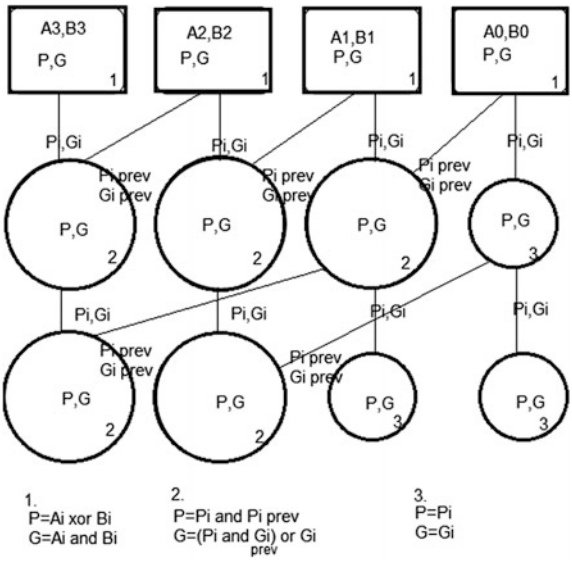


Fig. 1 Kogge–Stone adder

2.2 Wave-Pipelined Architecture

Wave pipelining is currently being used in advanced VLSI designs as an alternative to pipelining because it involves design and analysis across the design levels of VLSI. It reduces the area, power, and clock loads while maintaining the functionality and timing. This technique also increases the frequency of operation because the propagation of logic depends upon the difference between longest path and shortest path delay. As a result, several computation "waves," i.e., logic signals related to different clock cycles, can propagate through the logic concurrently. The number of stages in pipelining depends on operand size. For 2^n-bit data, we need n stages of pipelining. Table 1 shows the operations performed by ALU with a given instruction set. A ready signal has been used to make ALU ON. Figure 2 shows the block-diagram of 8-bit wave-pipelined ALU which contains four modules; INIT, ROUT1, ROUT2, and SUM.

Table 1 List of operations performed by ALU

Instruction set	Operation
00000	NOP
00100	Exnor (A,B)
00101	Exnor (A,(∼B))
00110	Exnor (∼A,B)
00111	Exnor ∼A, ∼B
01000	And A,B
01001	And A,(∼B)
01010	And (∼A),B
01011	Nand (A,B)
10000	Exor A,B
10001	Exor A,(∼B)
10010	Exor (∼A),B)
10011	Exor (∼A),(∼B)
10100	Sub A,B
10101	Sub A,∼B
10110	Sub (∼A),B
10111	Sub (∼A),(∼B)
11000	Add A,B
11001	Add A,(∼B)
11010	Add (∼A,B)
11011	Add (∼A),(∼B)
11011	Add (∼A),(∼B)

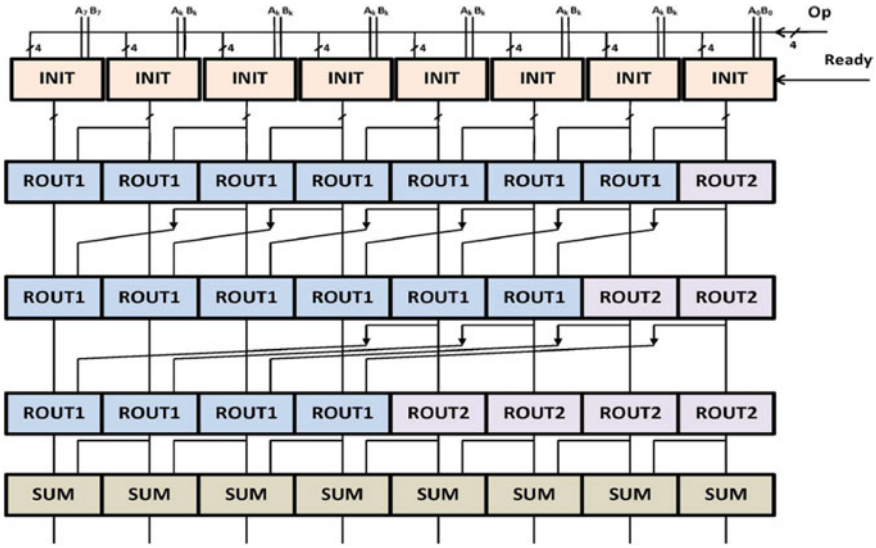


Fig. 2 Block diagram of 8-bit wave-pipelined ALU

2.3 Internal Modules of Existing

2.3.1 INIT Module

The most important part of ALU is INIT. It performs logical operations on individual bits of operands based on control signal and produces generator (G) and propagator (P) as outputs. Figure 3 shows the internal design of INIT module. The INIT module in existing ALU has been designed by using "TRS" is Toggle Flip flop and "D2" is Dual input D-latch combine known as Data-Pulse counter which performs arithmetic and logical operations. The "D" is D-latch which has been used in circuit for synchronization. This performs operations on two-bit data based on given instruction set [8].

2.3.2 ROUT1 Module

8-bit wave-pipelined ALU has used ROUT1 for the purpose of routing the partial carry generator and propagator to next stage. This routing is based on Kogge–Stone adder. The ROUT1 module takes the partial generator and propagator and produces another set of generator and propagator. Figure 4 shows the ROUT1 module designed by using D-latch and C-gate. Equations (1) and (2) given below are internal operations done by the ROUT1 module, where P_i and G_i are propagator and generator of present stage, and P_{prev} and G_{prev} are propagator and generator of previous stage.

Fig. 3 INIT module

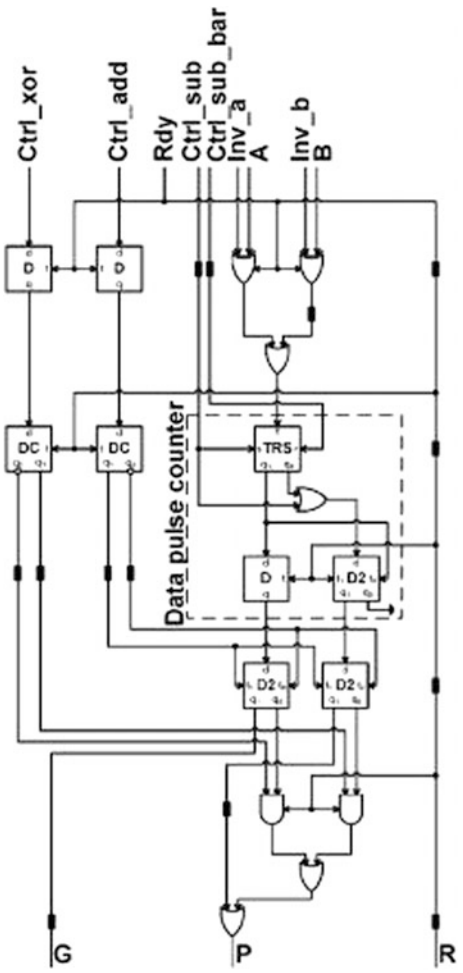
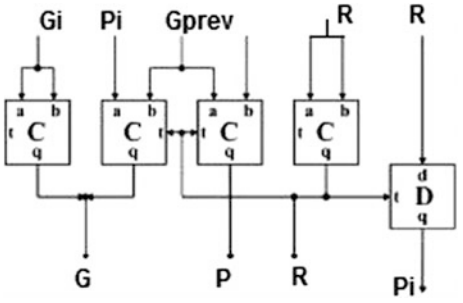


Fig. 4 ROUT1 module



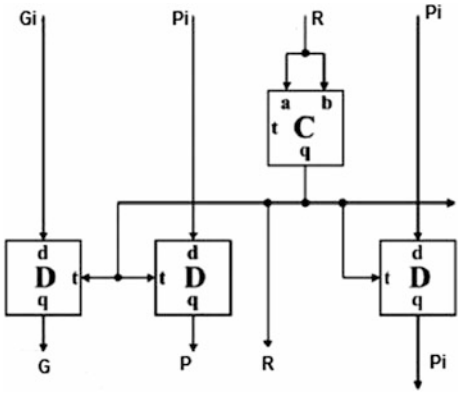


Fig. 5 ROUT2 module

$$P = P_{\mathrm{i}} \text{ and } P_{\mathrm{iprev}} \tag{1}$$

$$G = (P_{\mathrm{i}} \text{ and } G_{\mathrm{iprev}}) \text{ or } G_{\mathrm{i}} \tag{2}$$

2.3.3 ROUT2 Module

ROUT2 module in ALU is also part of routing which acts as buffer to pass the carry generator and propagator produced by INIT to next stage. Figure 5 shows the internal architecture of ROUT2 module designed by using C-gate and D-latch.

2.3.4 SUM Module

Figure 5 shows the SUM module in ALU by using controlled XOR gate which performs XOR operation on carry generator and propagator and produces sum as output (Fig. 6).

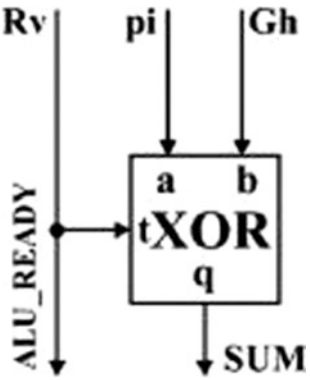


Fig. 6 SUM module

2.4 Internal Modules of Modified ALU

2.4.1 INIT Module

Figure 7 shows the INIT module of modified ALU which is designed by using logic gates performs all primitive logic operations on individual bits of operands based on control signal like existing INIT. K-map technique has been used in designing INIT module. In this modified INIT module, all the unnecessary latches have been successfully eliminated by preserving the circuit operation. This helps to reduce the power consumption, area, and delay. In this, the instruction size is also reduced from 6 bits to 5 bits.

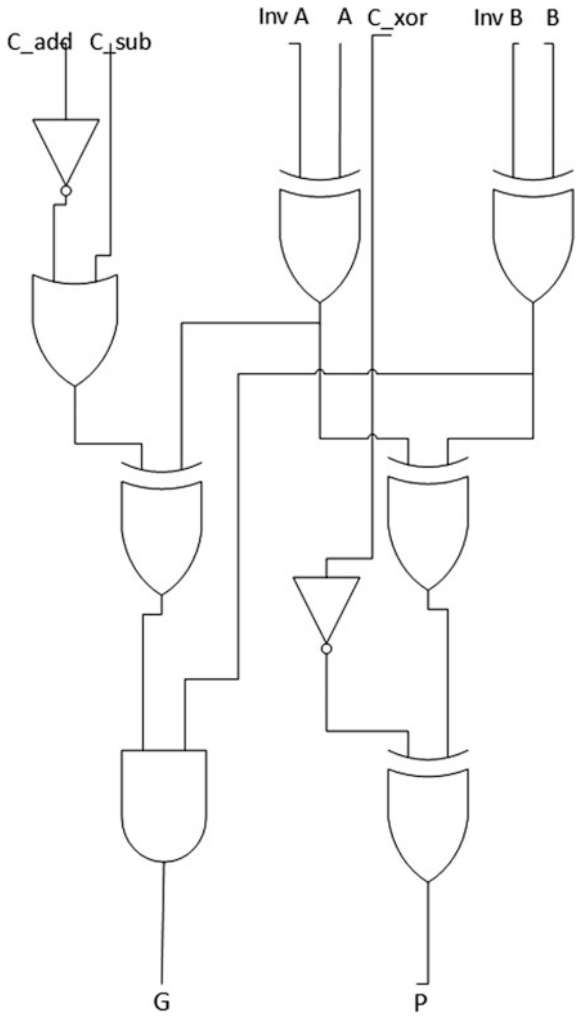


Fig. 7 INIT module

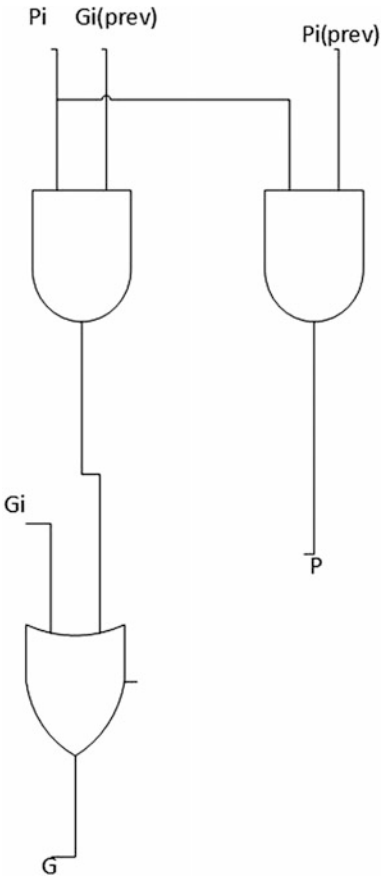


Fig. 8 ROUT1 module

2.4.2 ROUT1 Module

Figure 8 shows the modified ROUT1 which has been designed based on Eqs. (1) and (2). The ROUT1 in existing ALU performs the same operation but uses four C-gates and one D-latch in design which will increase the power consumption, area, and delay. To overcome, these gates have been used for implementing the ROUT1 module in modified ALU.

$$P = P_{\mathrm{i}} \text{ and } P_{\mathrm{iprev}} \tag{1}$$

$$G = (P_{\mathrm{i}} \text{ and } G_{\mathrm{iprev}}) \text{ or } G_{\mathrm{i}} \tag{2}$$

2.4.3 ROUT2 Module

ALU uses ROUT2 module as buffer to pass the carry generator and propagator produced by INIT to next stage, so it is designed by using the D-latches. Figure 9 shows the internal architecture of ROUT2 module.

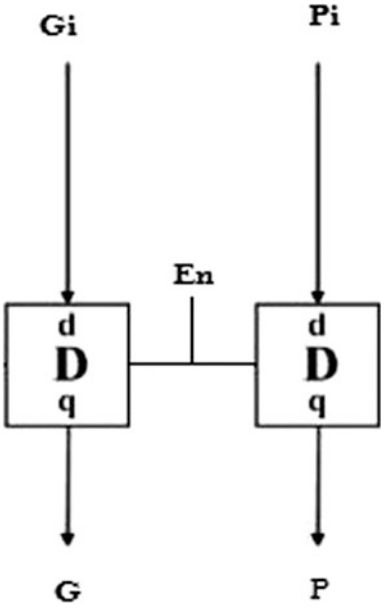


Fig. 9 ROUT2 module

2.4.4 SUM Module

Figure 10 shows the SUM module used in modified ALU. In this, the same SUM module has been used because it is nothing but an XOR gate with controlling input.

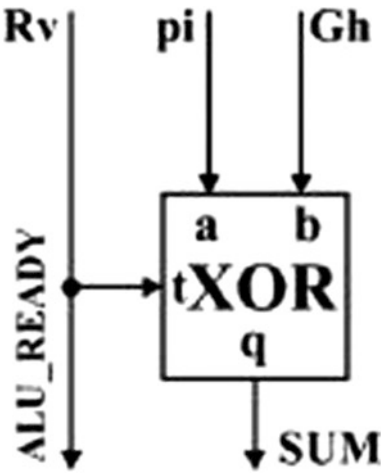


Fig. 10 SUM module

3 Results and Discussion

Both the ALUs have been simulated by using Cadence® NC simulator in which both the ALUs are exhibiting the same results for given set of instructions. Table 2 shows the power, area, cell count, and timing reports of both the ALUs which are acquired by using Cadence® RC launcher. Cadence® encounter has been used to generate layout and also to perform post-layout verification. Table 3 shows the power and gates report of both ALUs after post-layout verification. Figure 11 shows the comparison chart of Table 2, and Fig. 12 shows the comparison chart of Table 3.

Table 2 Comparison table of Synthesis reports

	Modified ALU	Existing ALU
Power (mW)	0.15	0.270
Area	5795	10012
Cell count	289	565
Timing (ps)	1678	2069

Table 3 Comparison after post-layout verification

	Modified ALU	Existing ALU
Power (mW)	0.2114	0.310
Cell count	289	565

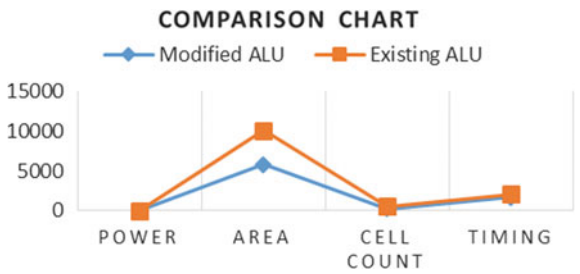


Fig. 11 Comparison of synthesis report

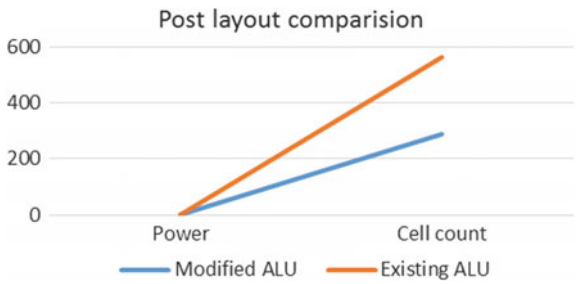


Fig. 12 Comparison of post-layout verification

4 Conclusion

This ALU design based on Kogge–Stone adder employs an asynchronous wave-pipelined approach. This wave-pipelined ALU operates with more frequency as compared to pipelined ALUs. But all internal modules have been designed by using latches which results increase in power consumption, area, and delay. To make this ALU a high-performance ALU, all the internal modules are modified with less number of gates, and same set of operation has reduced the power consumption, area, and delay.

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