P R O J E C T

Computer Architecture (Graded as one Test! 20 to 30%)

June 2020

Design a simple processor having 3 or 4 bits for opcode based on the number of instructions you want to support. The purpose of this project is to give you freedom and exposure in designing a processor of your own; think out of the box to come up with innovative ideas, and don't be biased or limited by the examples given bellow and processors you have studied in class.

Submission is in two phases:

PHASE I (SUBMISSION DEADLINE: mid June , 2020) 5 TO 10%

In phase one, you have to submit your proposal document containing the following information:

1. List of **instructions** you want your processor to execute.
2. Specification of your processor
    a. Instruction format
    b. Answer all design issues in chapter 5 (Read chapter 5 slide on pages 8,51,52)
    c. Block diagram of the proposed processor (You may use Buss, Register, ALU (Use a 4 bit ALU, 74xx381 or 74xx382 ; cascade them to support 8 or 16 bit), Multiplexer, Register file, RAM, ROM etc). You should indicate control inputs to all block components. Here is a sample.

PHASE II (SUBMISSION DEADLINE: early July, 2020, PRESENTATION IN recorded video) 15 TO 20%

In phase two, you need to conduct detailed design and simulation on Proteus.

1. Components should be identified and listed
2. Identify Micro-instructions and program your controller (load rom file on to ROM). Here is a sample.
3. Simulate your processor. Here is a sample.