*Lecture 4*

# Design For Signal Integrity

# In this lecture

- Noise, Distortion and Frequency Response
- Inductive and Capacitive Coupling
- Power and Ground Plane
- PCB Electrical Characteristics Modeling
- Routing and Placement Guidelines

# Noise in PCB

- Can be broadly classified as Background noise and Intrinsic Noise
- Background noise:
  - Uncontrolled signal that originates from the working env't
- Intrinsic Noise: *Four types of intrinsic noise*
  - Thermal noise, shot noise, contact noise, popcorn noise
- Minimizing noise is addressed by the circuit designer rather than the PCB designer.
  - Noise should be handled long before the layout is started

# Intrinsic Noise

- Thermal Noise (aka Johnson noise):
  - Due to motion of electrons in conductors
  - It's a white noise which is a function of temperature
- Shot noise (aka Poisson noise):
  - Due to potential barriers mostly in semiconductors
  - Also a white noise
- Contact noise
  - Due to imperfect contact in junctions or interfaces
  - Large at low frequencies (prop'l to $^1/_f$)
- Popcorn noise (aka burst noise):
  - Due to manufacturing defects in semiconductors and Ics
  - Typically proportional to $^1/_{f^2}$

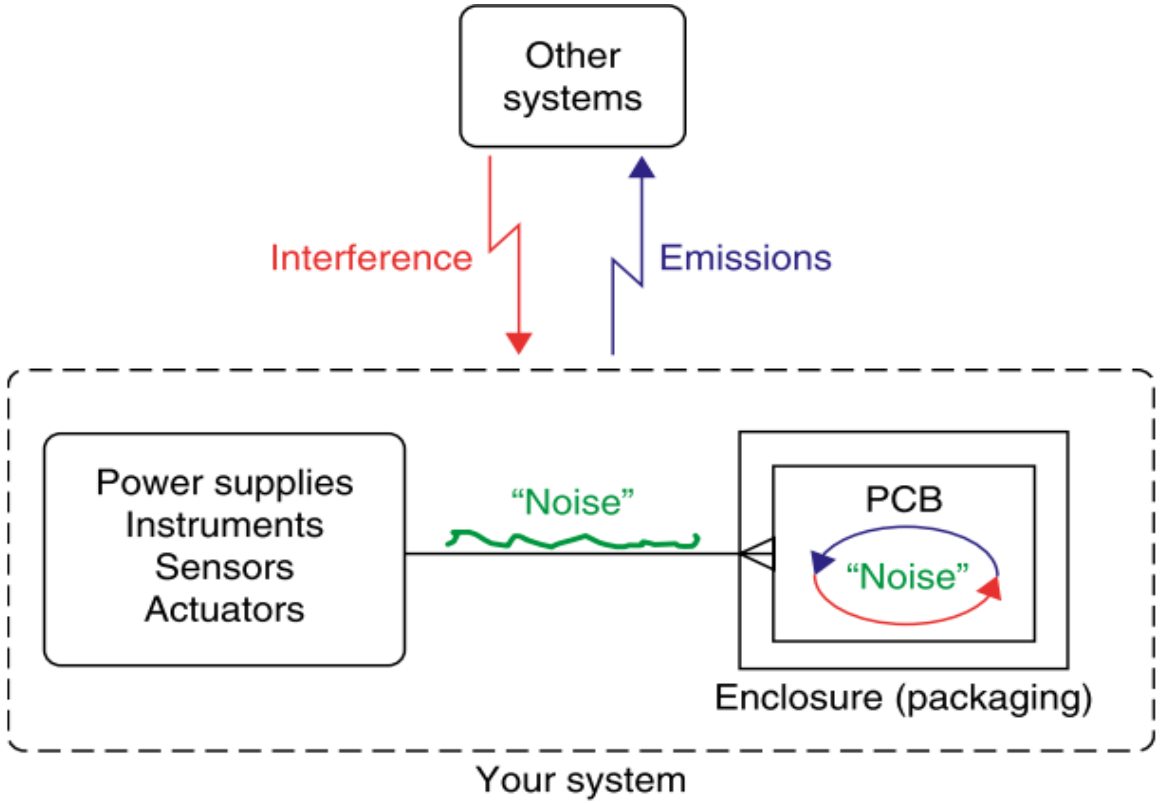
# Distortion

- Amplitude, phase and harmonic distortions
- Amplitude Distortion:
  - Clipping, overshot, undershot, …
- Phase Distortion:
  - Due to slew rate, propagation delay or phase shift
- Harmonic Distortion:
  - Due to composite signals of multiple frequency components
  - Fourier transform to identify the spectrum

# Signal Integrity

**3** Goals in designing PCBs for signal integrity

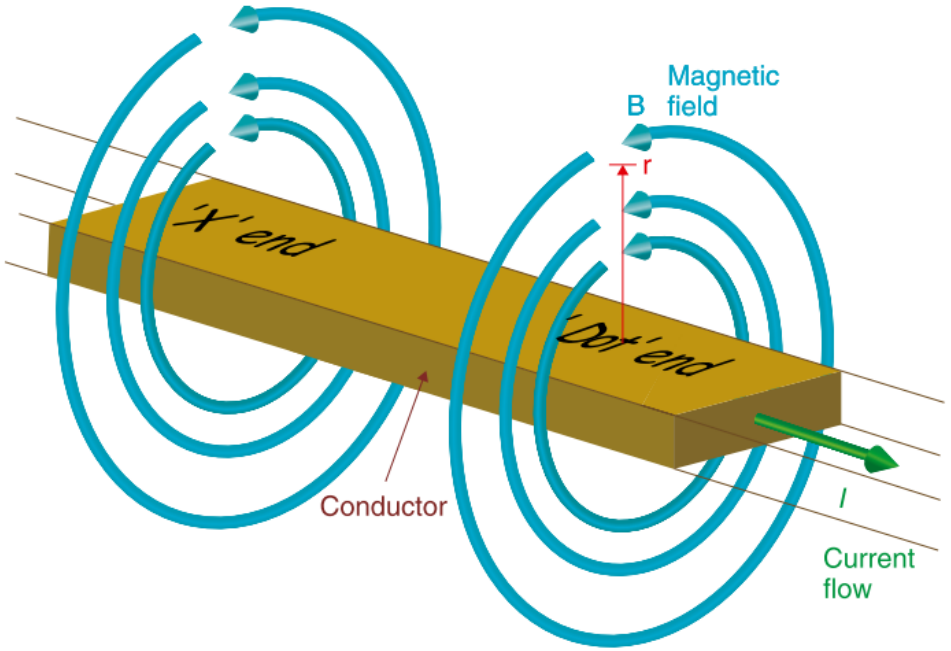
1. It should be immune to Interference from other systems
2. It should not produce emissions that cause problems for other systems
3. It should exhibit the desired signal quality



# EMI and EMC

- Electromagnetic Interference (EMI)
  - *When electromagnetic waves get in to your system or vice versa*
- Electromagnetic Compatibility (EMC)
  - *The ability for systems to "play nice together"*
- The method by which systems "reach out and touch" another system is by inductive and capacitive coupling
- Carefully laying out the PCB greatly reduces EMI and improves EMC
- Many established standards and regulations on the level of emission and immunity for all classes of products

# Inductive Coupling




✓ Magnetic field at r:

$$B = \frac{\mu_0 I}{2\pi r^2}$$

✓ Magnetic flux in an area A:

$$\Phi = BA\ \cos(\theta)$$

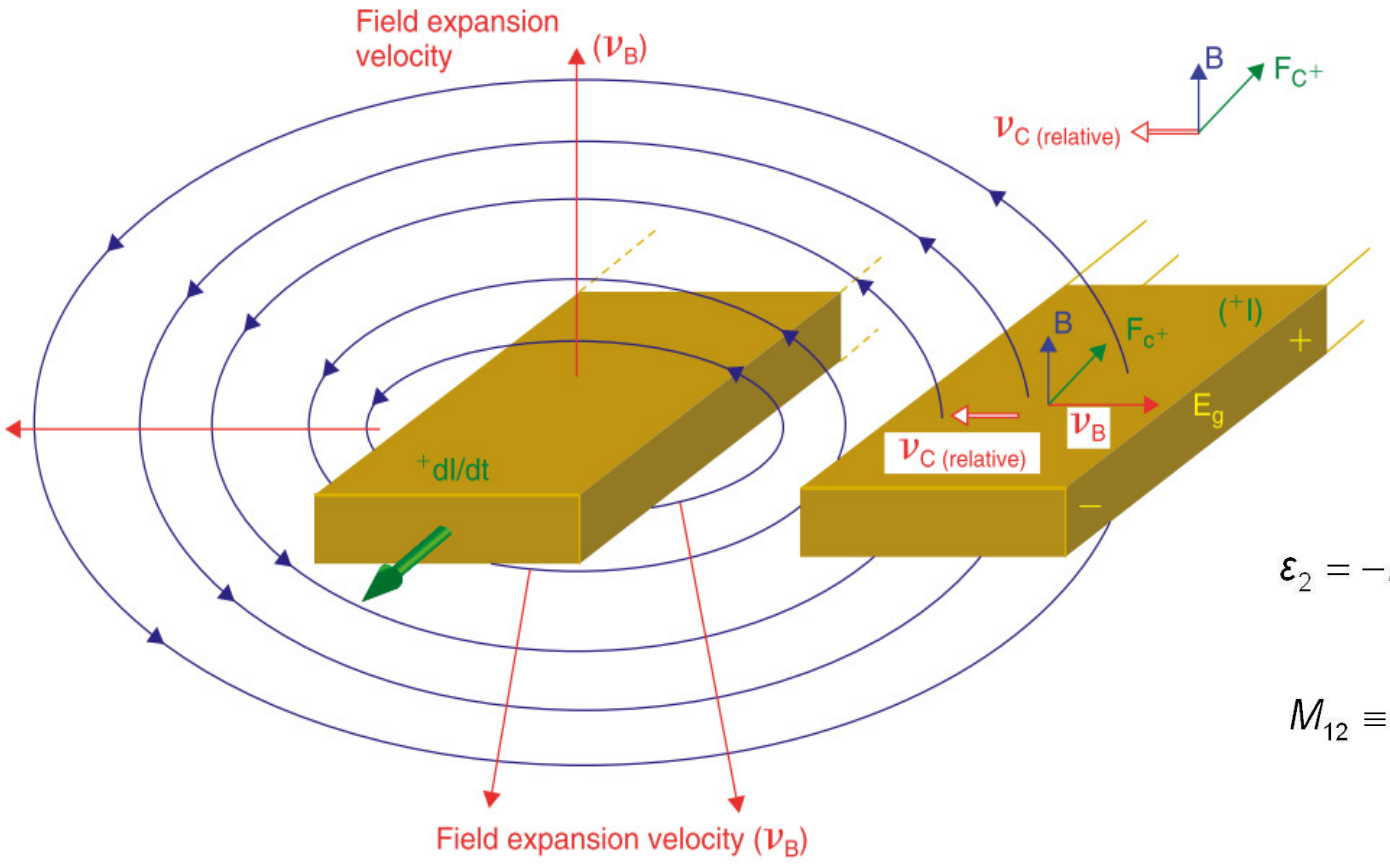
✓ Induced Voltage (Faraday's Law):

$$E = -\frac{d\Phi}{dt}$$

- Emf induced into the conductor produces a current in the conductor that creates a magnetic flux that will oppose the changing flux --- *self inductance*
- Self inductance tends to limit how fast current can change in a conductor
  - *Hence ac impedance due to inductance:* $Z_L = X_L = j\omega L$

$$L = \frac{N\Phi_m}{I}$$ (N = 1 for PCB trace and its return path)

# Inductive Coupling



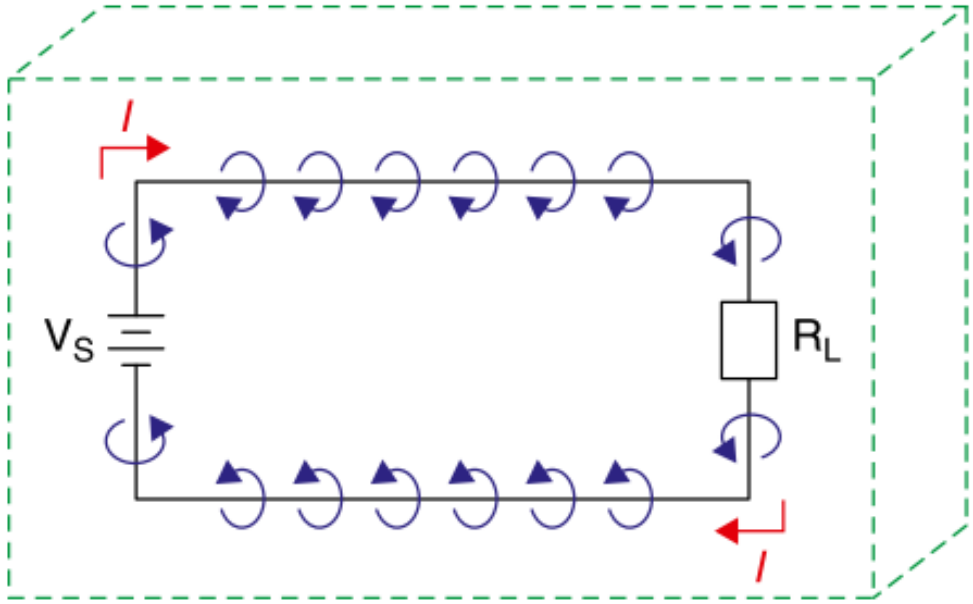

$$\varepsilon_2 = -N_2 \frac{d\Phi_{12}}{dt} = -M_{12} \frac{d\,I_1}{dt}$$

$$M_{12} \equiv \frac{N_2 \Phi_{12}}{I_1}$$

Voltage, Eg is generated in a nearby trace due to inductive coupling of magnetic field

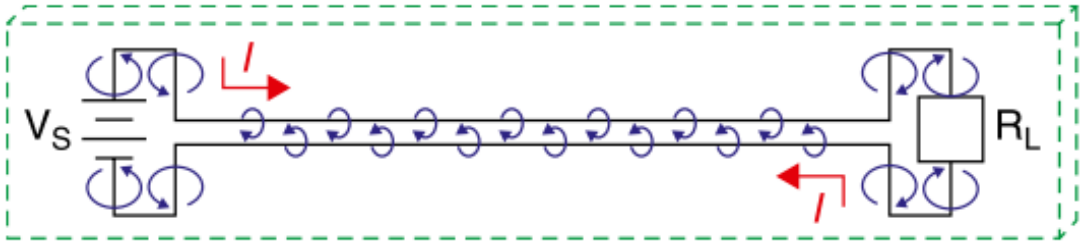
- *Mutual Inductance … In PCB it's called Crosstalk*

# Loop Inductance




- ✓ Total loop inductance:
  $L = \mu_0 n^2 A\ell$
- ✓ For PCB traces, *n = 1*
- ✓ For most materials used in PCB, $\mu = 1$
- ✓ Generally,
  $L = A\ell$

- Loop inductance of a PCB trace and return path depends on the volume that the circuit occupies -> *Reduce circuit volume*



# Loop Inductance

- Note that, the source and return current are in opposite direction and hence produce opposing magnetic fields.
- The opposing magnetic fields result in partial flux cancellation
- The amount of cancelation depends on the amount of mutual inductance which in turn depends on the distance between the traces.

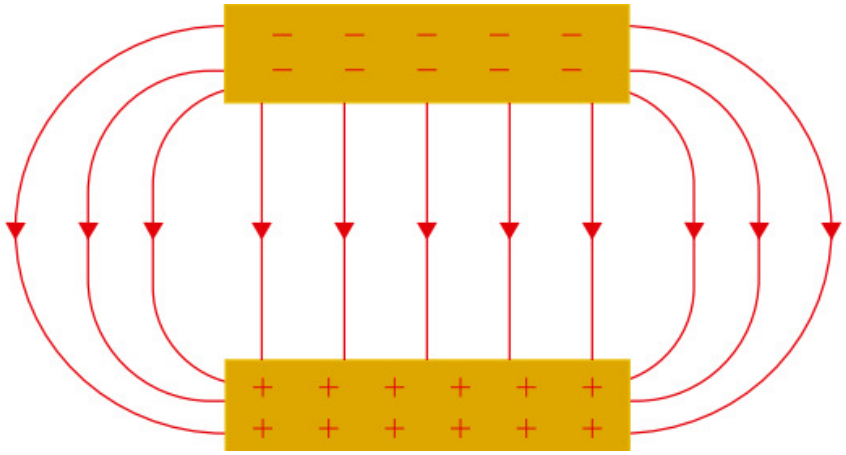
# Loop Inductance

- If the return trace is in close proximity to the signal trace, the loop inductance is reduced.
- If the loop inductance is reduced in an AC circuit, there will be less inductive reactance ($X_L$), less voltage drop, and less crosstalk -> *fewer EMI problems*

$$X_L = 2\pi f L$$

- To maintain a small $X_L$, we need to have a return path as wide as possible (low self inductance) and as close as possible to the signal path (max coupling and small cross-sectional area)
  - *Easiest way to achieve this is using a plane layer as return path*

# Capacitive Coupling



✓ Capacitance b/n two plates:

$$C = \frac{\varepsilon_0 A}{d}$$

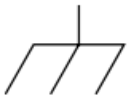
✓ Capacitive reactance:

$$X_C = \frac{1}{2\pi f C} = \frac{d}{2\pi f \varepsilon_0 A}$$

- By keeping unrelated signal traces farther apart (large d), the reactance b/n the traces is higher and the coupling (crosstalk) is reduced.
- Both in magnetic and electric fields, the wider the return path (area of conductor) and the closer the signal trace to the return path, the better the coupling

# Ground Plane

- The “ground plane” has nothing to do with “ground” unless it’s attached to the earth by some means
  - *“Ground” has long been used to mean return path*
- A “ground” that is an omnipresent and equipotential reference is a misconception.

| Symbol | Name | Purpose/usage |
|---|---|---|
| | Earth GND | A direct connection to the earth. |
|  | | A direct connection to a vehicle’s or an airplane’s frame that serves the same function as earth ground. |
|  | Noiseless GND | Used to indicate a low or noiseless earth ground. |
|  | Safety GND | Used to indicate a ground connection that serves a safety function against electric shock. |
|  | Chassis GND | A connection to a chassis, or frame, or similar connection of a *printed circuit board* and may be completely different from earth ground. |
|  | Return | Used to indicate common return connections. |

# Ground Plane

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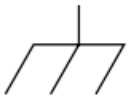
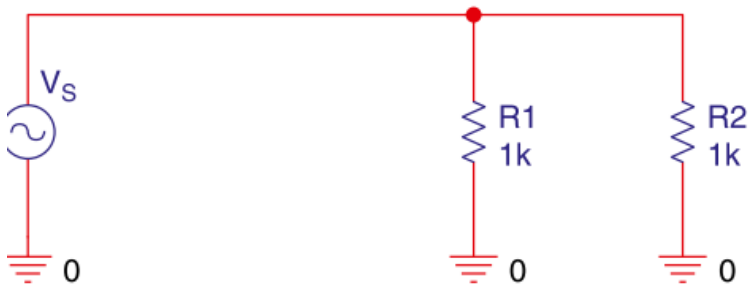
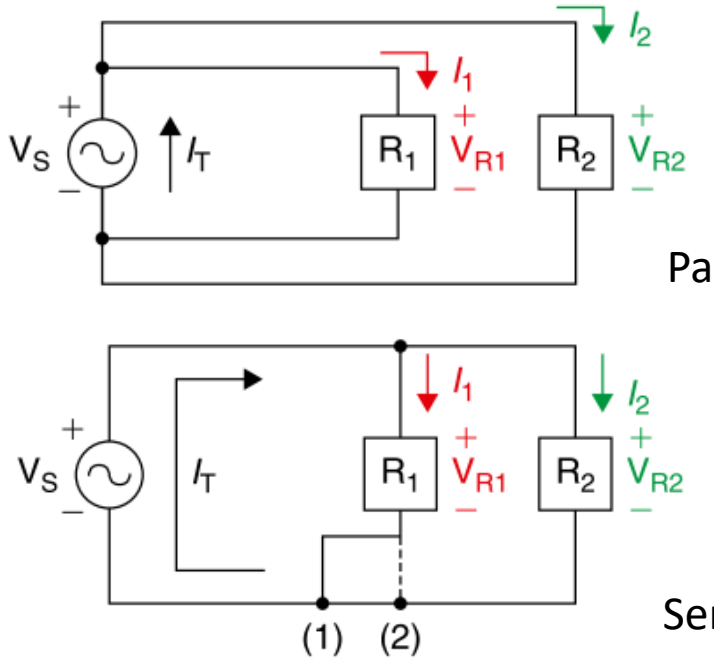
|  | Chassis GND | A connection to a chassis, or frame, or similar connection of a *printed circuit board* and may be completely different from earth ground. |
|  | Return | Used to indicate common return connections. |

# Signal and return connection

- There are two basic source and return(ground) connection schemes
  - *Parallel and series*



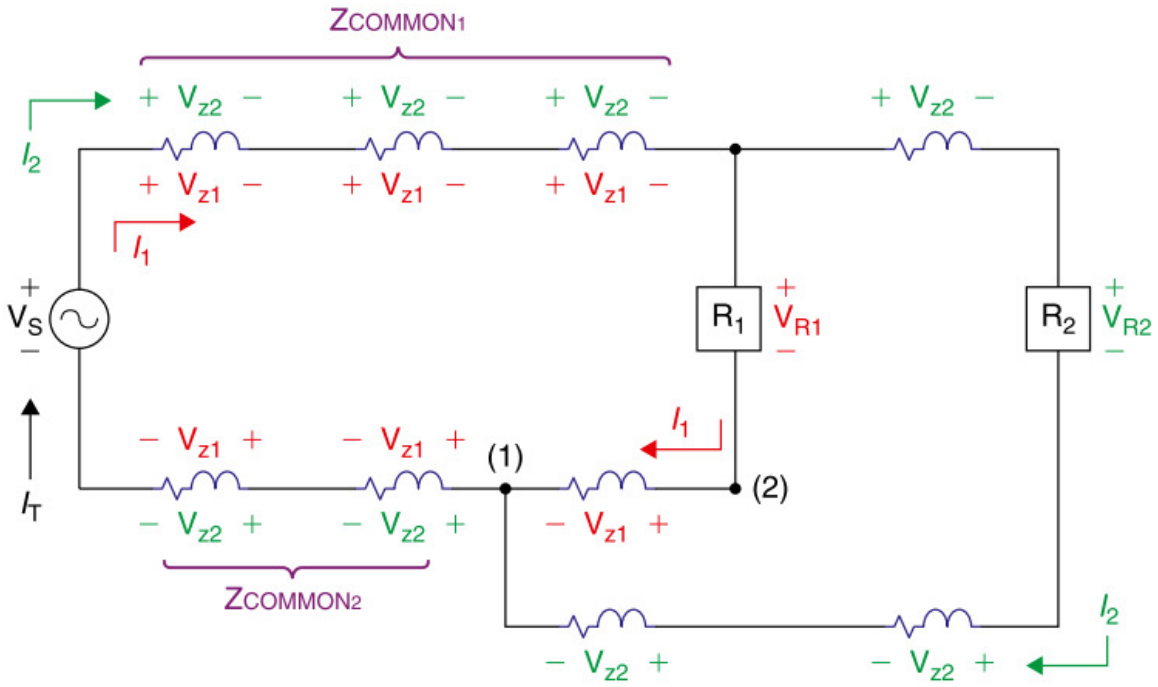




✓ On schematic level, in both cases:

$$I_T = I_1 + I_2 \text{ and } V_{R1} = V_{R2} = V_S$$

- At schematic level, both are identical and mathematically the same
- On PCB, they are significantly different
  - Even connecting at 1 and 2 makes a difference in the series connection

# Signal and return connection

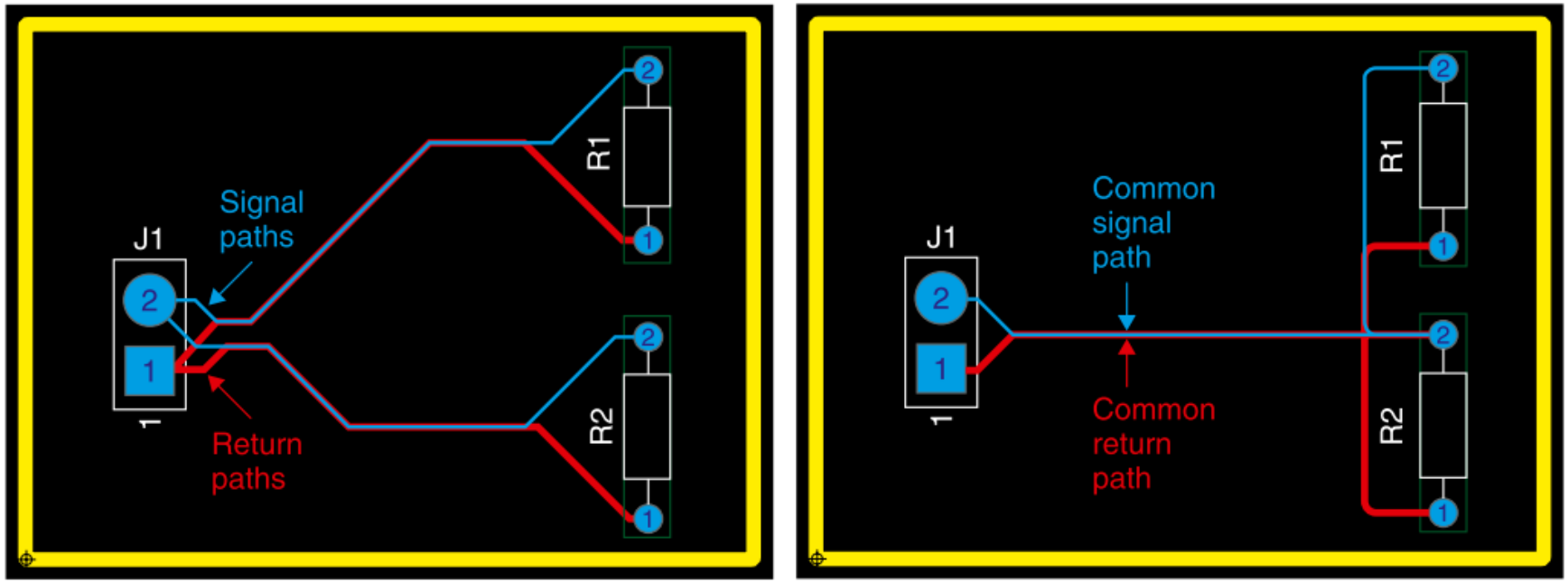



✓ Still $I_T = I_1 + I_2$, but

$V_{R1} \neq V_{R2} \neq V_S$

- There are voltage drops along shared and individual impedances b/n source and each of the loads.
  - *These impedances (hence voltage drop) increases with frequency of the signals*

# Signal and return connection

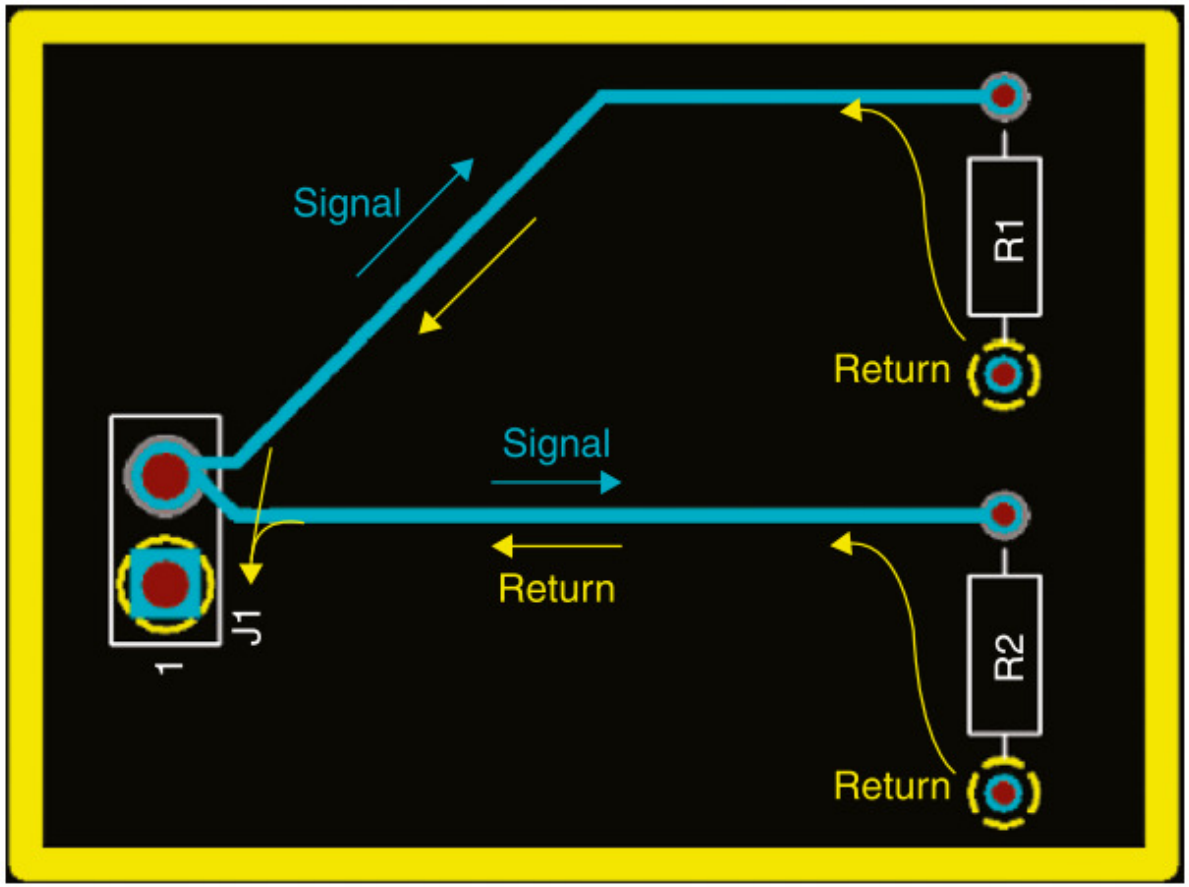



Parallel

Series

- Clearly, best return system is the parallel system. However, it would be incredibly cumbersome to route a PCB using this approach.
  - ***Solution -> Ground Plane***

# Ground Plane

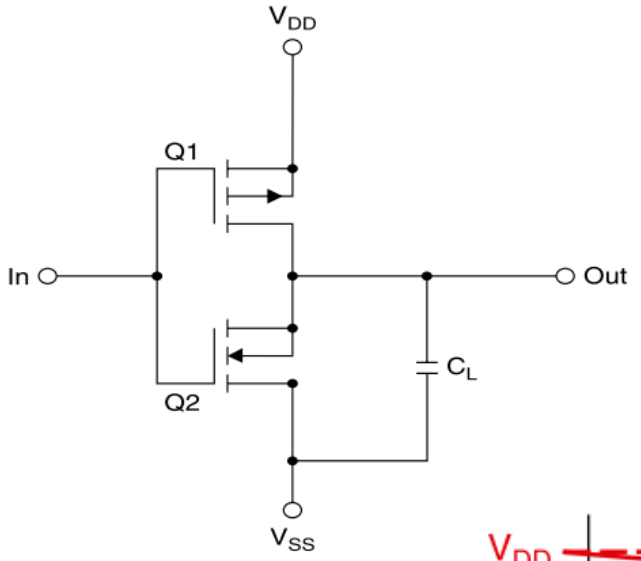



- This solves the routing problem, minimizes loop inductance and makes the return path close to be a “common reference”

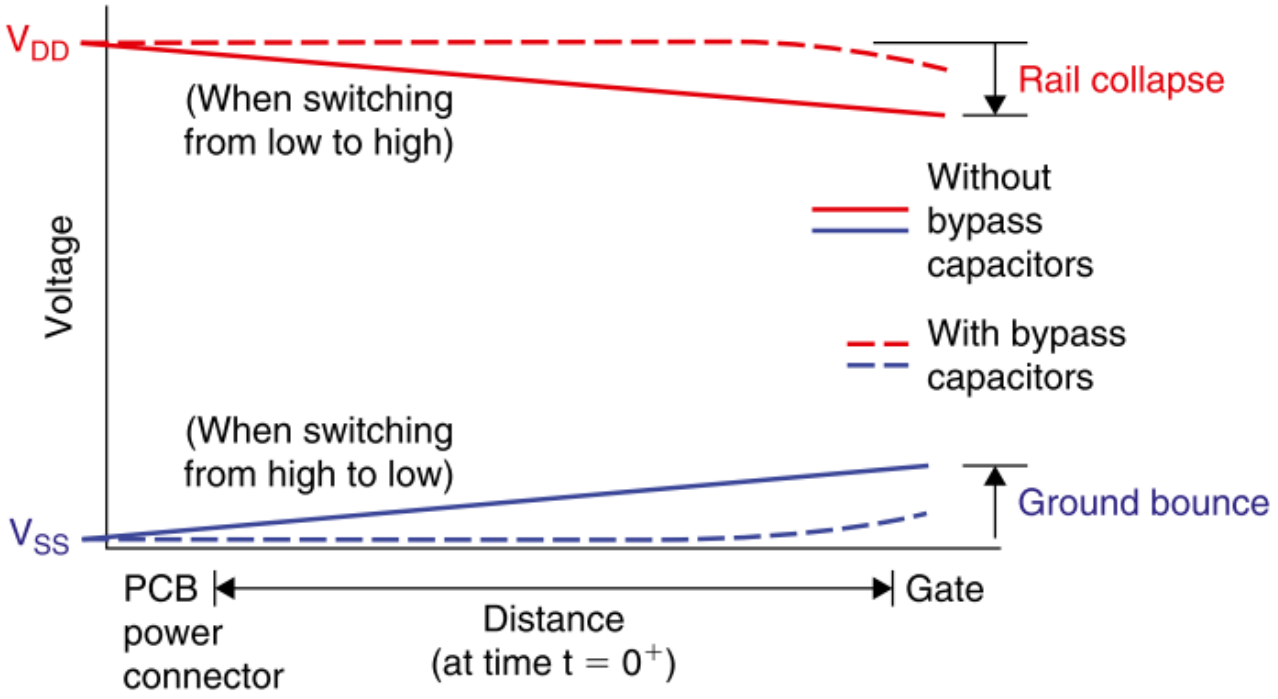
# Ground bounce and rail collapse

- In typical PCB, the power distribution system contains power and ground planes
- The planes are very wide traces (have little impedance) and usually adjacent to each other (high capacitance)
- While this is ideal power distribution system, a problem arises in high speed digital systems when switching from one state to the other.
  - ***Generally known as switching noise***
- This is because there is always some impedance even on the so called ground plane -> The plane is not a superconductor!
- Next picture shows the concept of “ground bounce” and “rail collapse”

# Ground bounce and rail collapse




- Placing bypass capacitor b/n $V_{DD}$ and $V_{SS}$ as close as possible to the gates minimizes the collapse and bounce of voltages on the planes

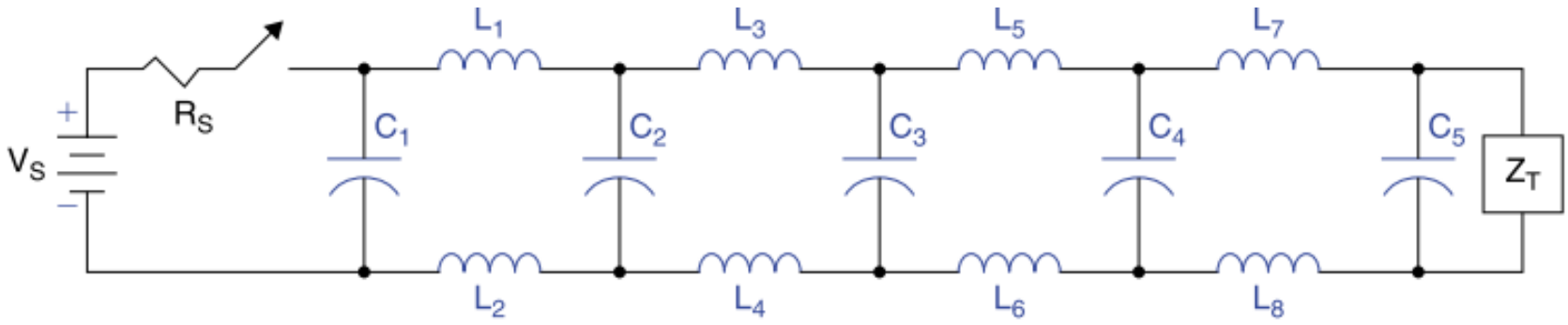


# PCB Electrical Characteristics

- Characteristics Impedance
- Transmission Lines
- Signal Reflection and ringing
- Electrically long traces
- Transmission line terminations
- Modeling and simulation of transmission lines

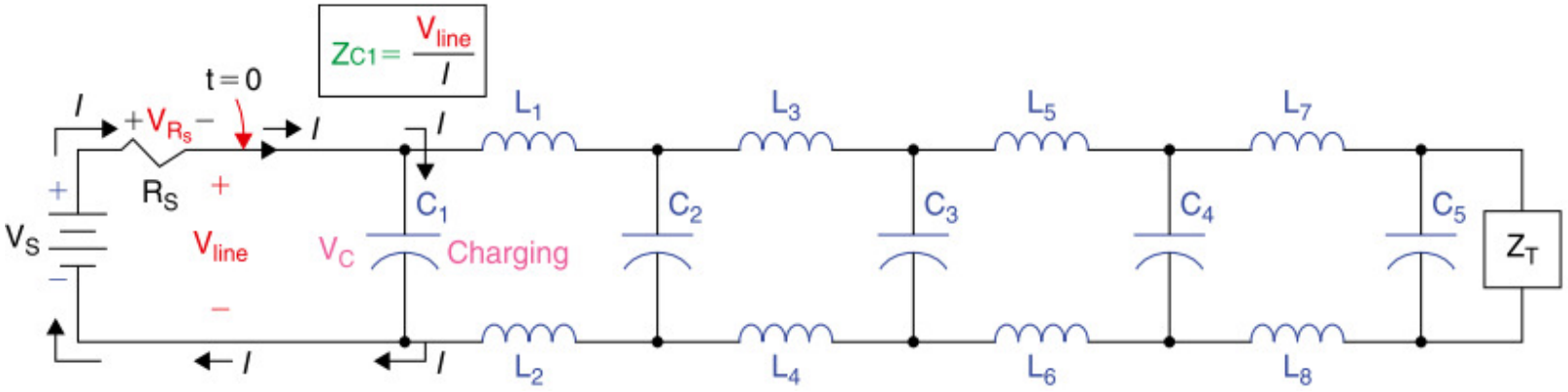
# Characteristics Impedance

- What is characteristics Impedance?
- Lumped-element Model of A transmission line
  - The series resistance is negligible
  - The line is “infinitely” long
  - Each LC lump represents a finite section of the line



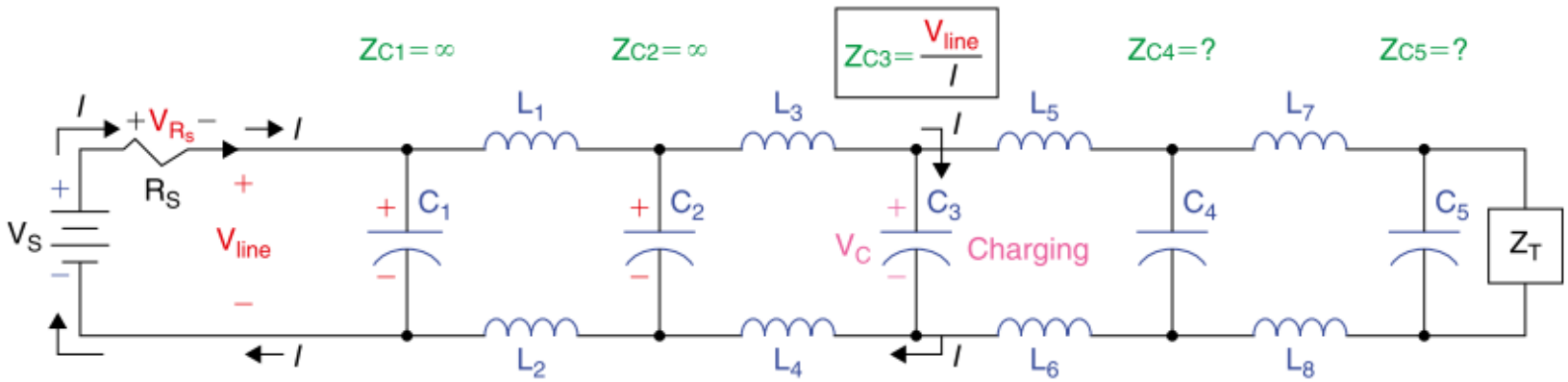
# Characteristics Impedance

- Analysis
  - At t=0, the switch is closed and Vs is applied to the line
  - Initially C1 acts as a short circuit, so I = Vs/Rs
  - A displacement current will circuit through C1 back to source
  - The instantaneous impedance is $Z_{C1} = V_{line}/I$
  - As C1 charges, current begins to flow in to L1, and so on..
  - As each Capacitor charges along the line, $Z_{Cn} = V_{line}/I_{Cn}$ and it dynamic..



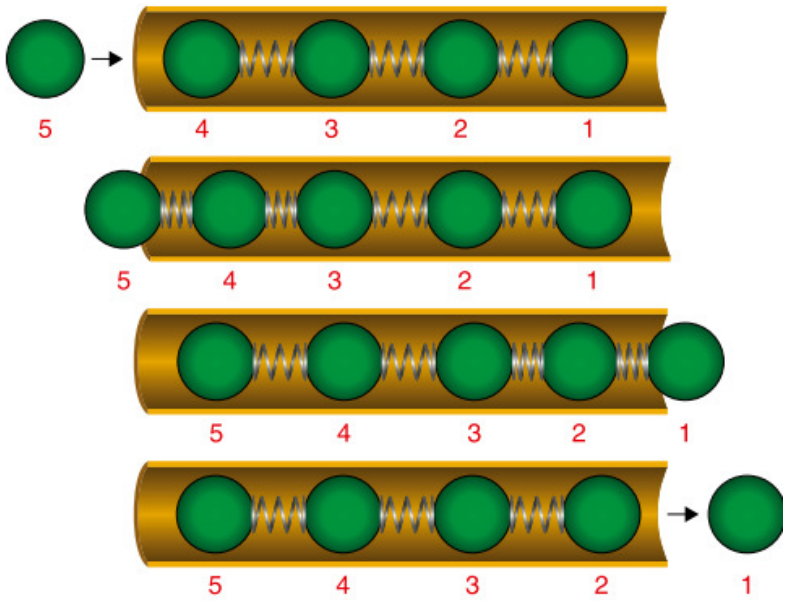
# Characteristics Impedance

- Analysis
  - The speed at which $Z_{ins}$ travels along the line depends on inductance and capacitance of each section.
  - If the impedance of each section is the same all along the line, we call the instantaneous impedance the characteristics impedance of the line ($Z_0$)



# Characteristics Impedance

- Analysis
  - The current actually “propagates” along the line like a wave
  - We consider displacement current rather than conduction
  - So, in TR line electrons travel slowly, but EM waves travel fast
  - Velocity of am EM wave thru a medium: $v_{EM} = \frac{1}{\sqrt{\varepsilon_0 \varepsilon_r \mu_0 \mu_r}}$



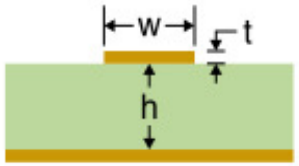
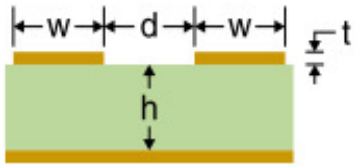

Or: $v_{EM} = c \times \frac{1}{\sqrt{\varepsilon_r \mu_r}}$

For typical PCB materials:

$$v_{EM} = c \times \frac{1}{\sqrt{\varepsilon_r}}$$

# Characteristics Impedance

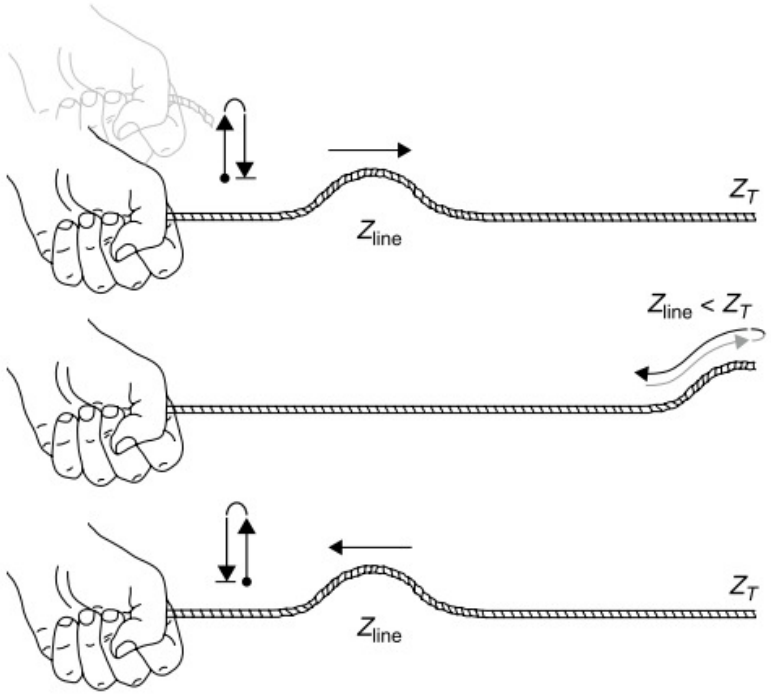
- Simplified equations for surface microstrip lines

| Microstrip transmission lines | | $Z_0(\Omega)$ | $C_0$ (pF/in.) |
|---|---|---|---|
| Surface |  | $Z_0 = \frac{k}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$ | $C_0 = \frac{0.67(\varepsilon_r + 1.41)}{\ln\left(\frac{5.98h}{0.8w + t}\right)}$ |
| Surface differential |  | $Z_{diff} = 2Z_0\left[1 - 0.48 \times e^{\left(-0.964\frac{d}{h}\right)}\right]$ | |
| | | $Z_0$ same as surface microstrip | |

$L_0 = (Z_0^2 \times C_0)/12$ in nH/in, where $k = 87$ for $15 < w < 25$ mils and $k = 79$ for $5 < w < 15$ mils. Restrictions: $0.1 < w/h < 3.0$ and $1 < \varepsilon_r < 15$ (typically 4.0 to 4.5 for FR4).

# Reflections

- What happens when the voltage wave, $V_{line}$ reaches $Z_T$?
  - Ans: It depends on what ZT is.
- First, assume $Z_T$ is open (infinite impedance)
  - Using a rope analogy below:
  - If no friction, the wave will propagate back unattenuated (reflection)

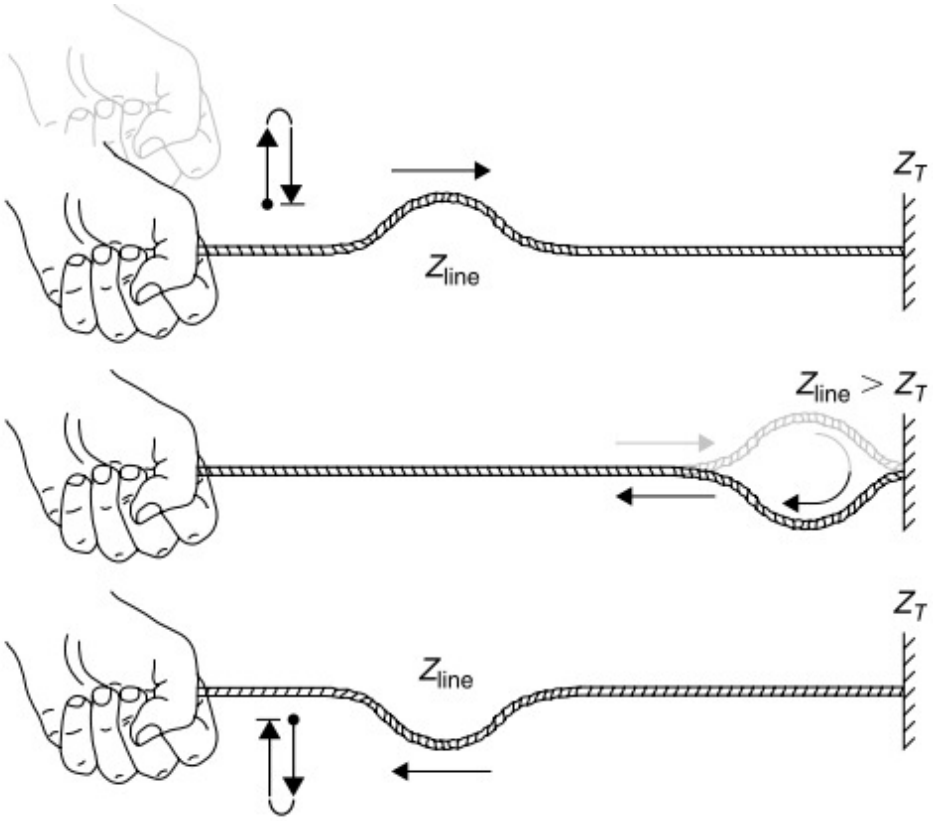



Magnitude of reflected wave, ρ:

$$\rho = \frac{Z_T - Z_{line}}{Z_T + Z_{line}}$$

# Reflections

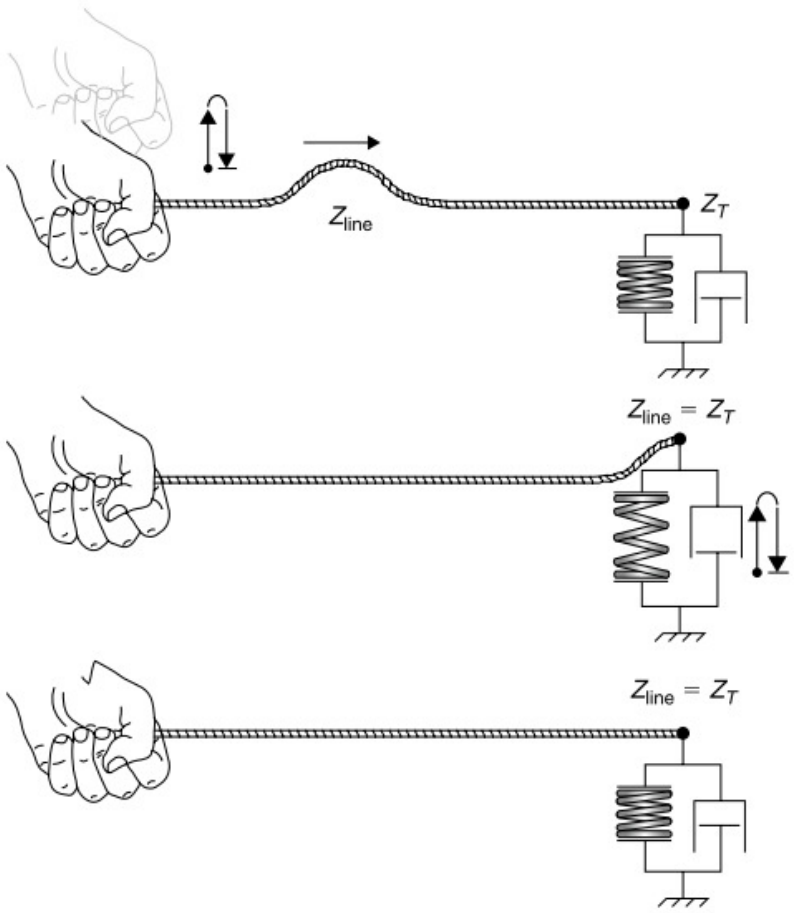
- Assume $Z_T$ is a short circuit
  - If no friction, the wave will be reflected negatively




Magnitude of reflected wave, ρ = -1

# Reflections

- Assume $Z_T$ is same as $Z_{line}$ ($Z_0$)
  - If no friction, the wave will be reflected negatively



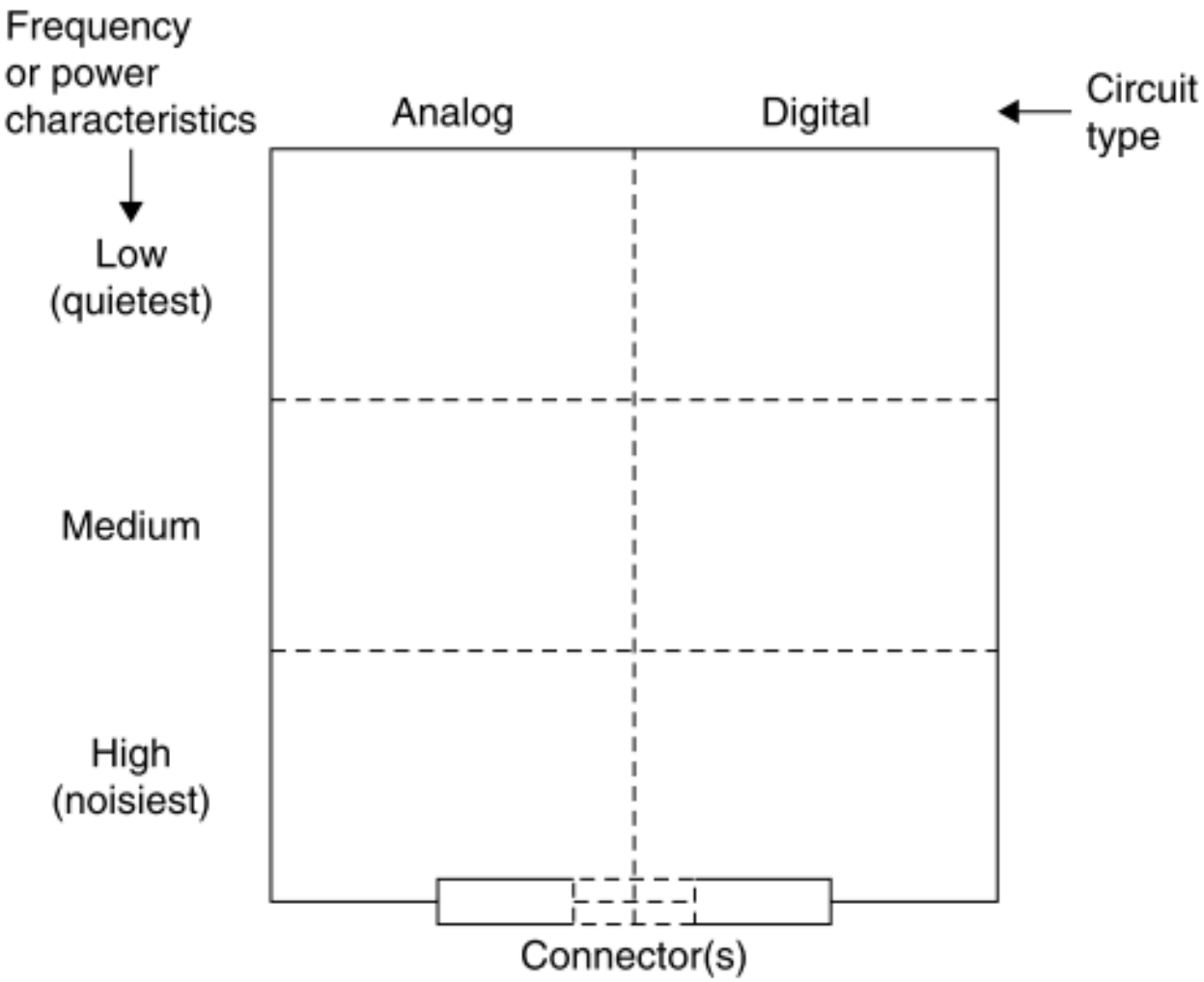

Magnitude of reflected wave, ρ = 0

# Ringing

- If there is little or no loss along the line, the reflected waves will bounce back and forth b/n source and termination (load)
  - This is called **Ringing**.
  - The voltage at any point along the line is uncontrollable
  - Causes undershoot/overshoot and create EMI problems and possibly damage sensitive components.
  - Magnitude and frequency of ringing depend on speed of the wave through the transmission line

    Text: PP 129 - 136

# Placement for signal integrity

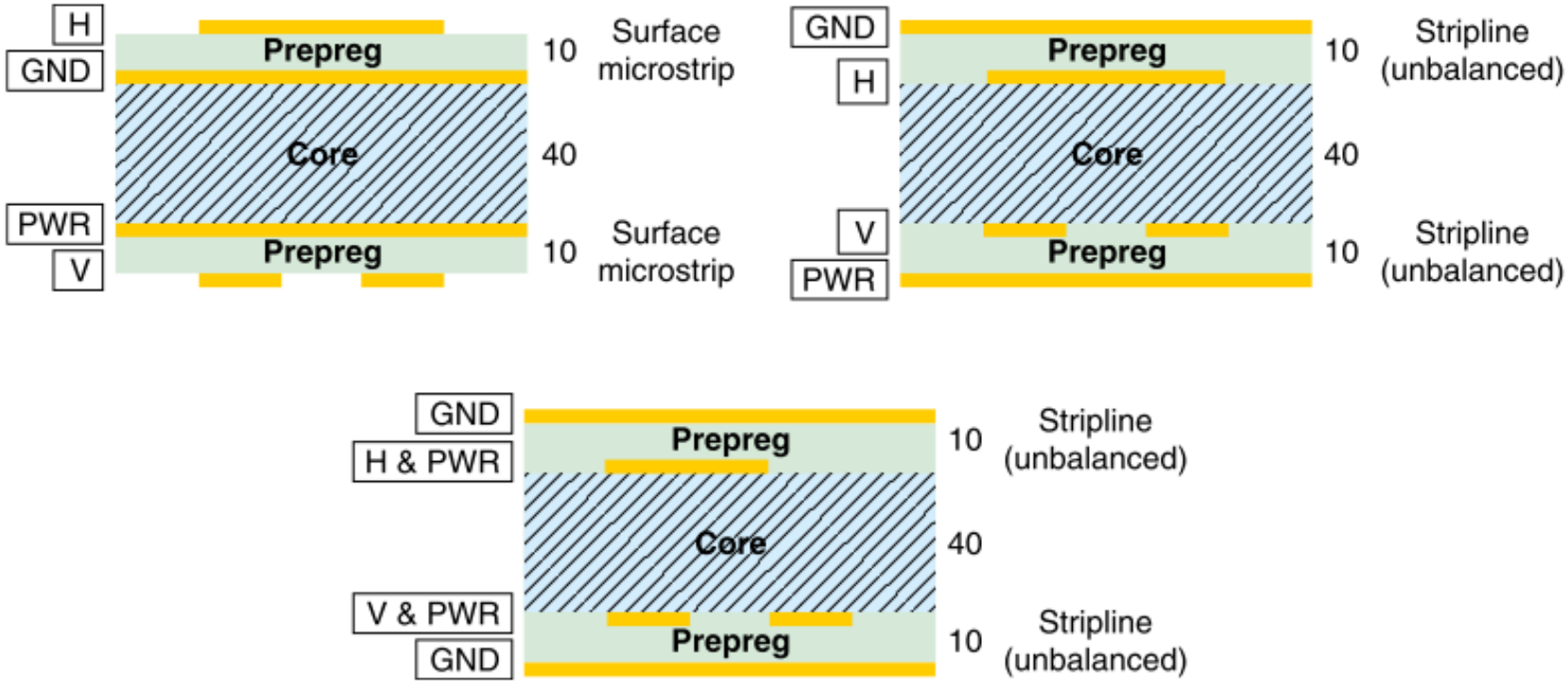


# Placement for signal integrity

- Signal flow from one edge to the other (no zigzag flows)
- For digital and high speed circuits keep related parts close together and lines short as possible
- Divide circuit into rooms (orCAD's "Room" property)
- Keep noisy parts/circuits separate and far away from analog circuits --- keep noisy ones at the edge
- Maintain split power and ground planes for analog and digital sections in mixed signal systems

# Placement for signal integrity

- Typical 4-layer stackup

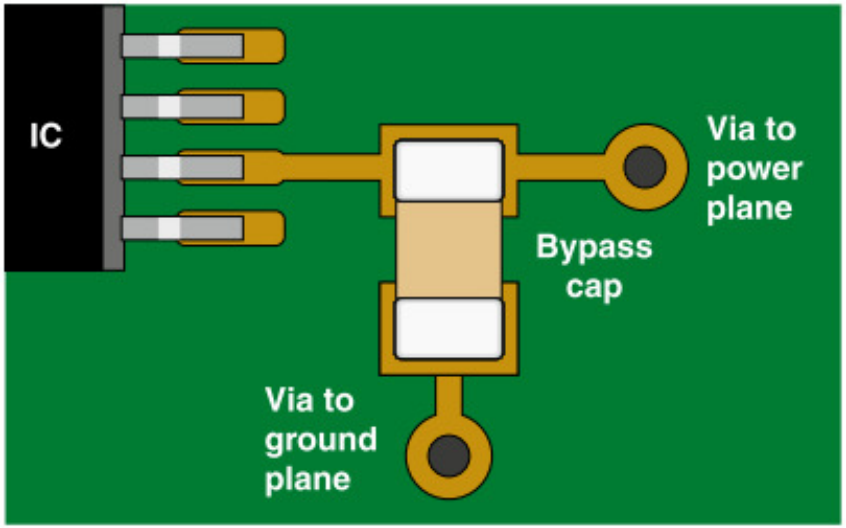


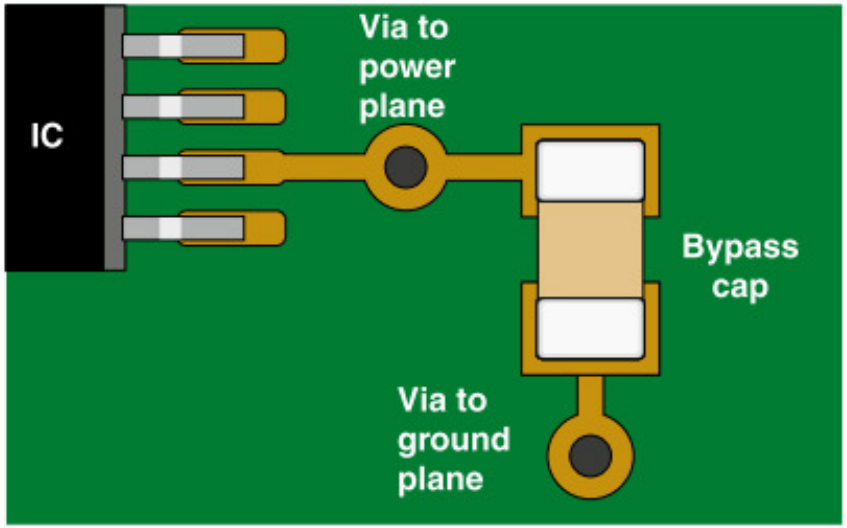
# Placement for signal integrity

- Bypass Capacitors and fan-out
  - Bypass capacitors have two purposes

    i) To short high frequency noise to ground

    ii) To serve as current reservoirs
  - Fan-out is the method of connecting traces to power/ground planes

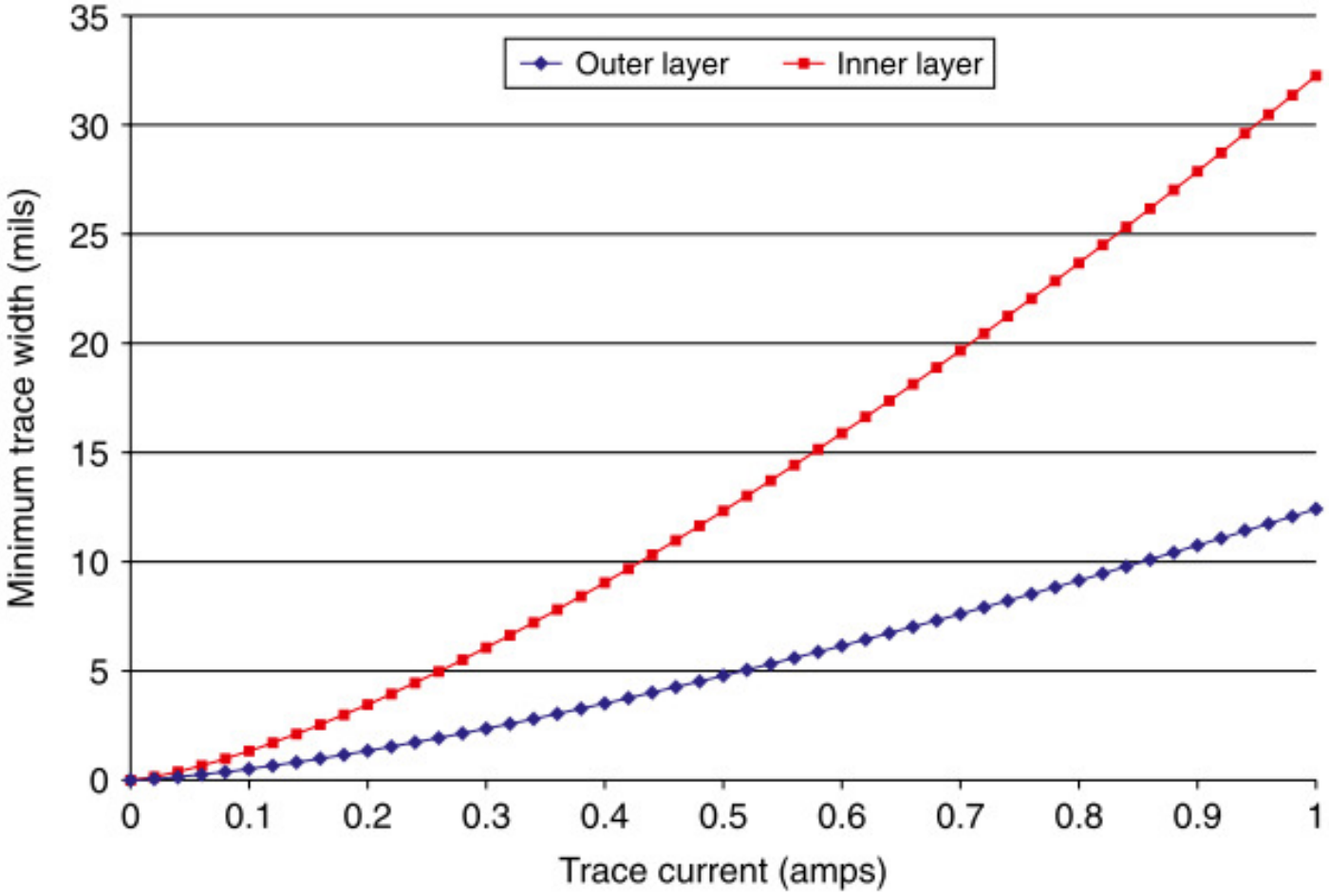


# Trace width Vs Current

$$w = \left(\frac{1}{1.4 \times h}\right) \times \left(\frac{I}{k \times \Delta T^{0.421}}\right)^{1.379}$$

For $\Delta T = 10°C$



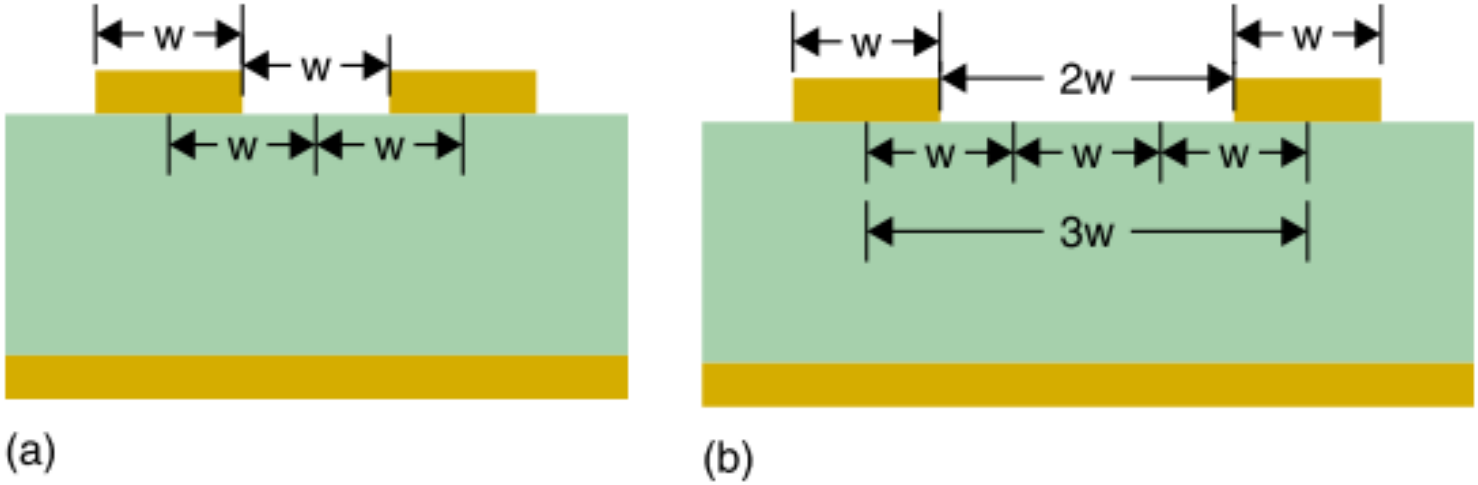
# Trace spacing Vs Voltage

Minimum trace spacing in mils (40mil = 1mm) – IPC-2221A

| Voltage between conductors ($V_{DC}$ or $V_{p-p}$) | Internal traces | External traces | | |
|---|---|---|---|---|
| | | Bare | Soldermask only | Conformal coating |
| 0–15 | 2 | 4 | 2 | 5 |
| 16–30 | 2 | 4 | 2 | 5 |
| 31–50 | 4 | 24 | 5 | 5 |
| 51–100 | 4 | 24 | 5 | 5 |

# Trace spacing Vs Crosstalk

3W Rule --- trace spacing edge-to-edge

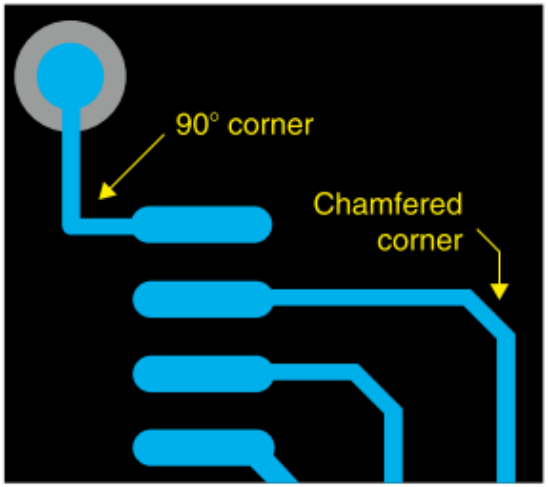


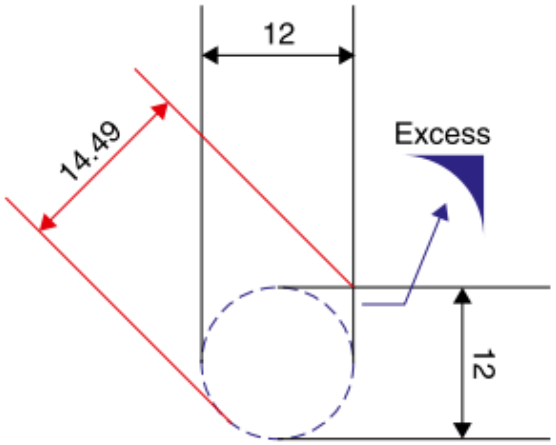

a) Typical trace spacing
b) 3W spacing to minimize crosstalk

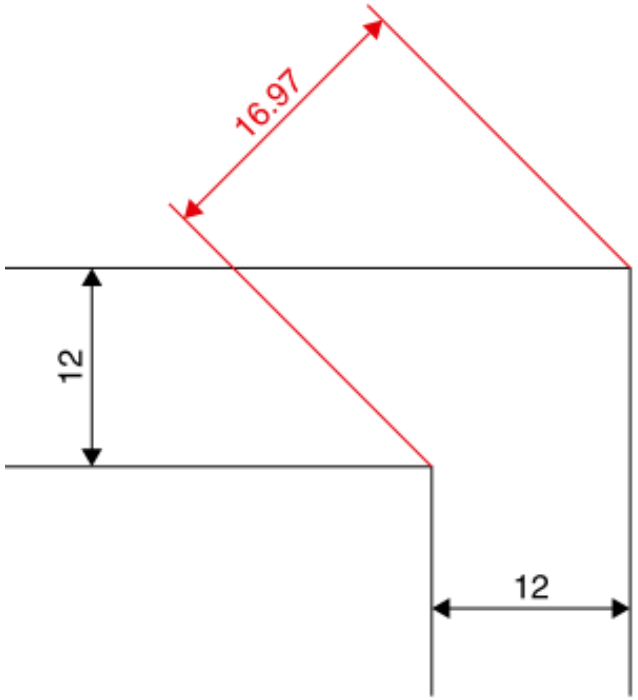
# Trace width/spacing for controlled impedance

Text PP147 - 153

# Acute Angle Control




- Acute angles change Z0 of the line at the corner b/c of increase in capacitance.
- For controlled impedance traces, 90° angles should be avoided