Lecture 3

Design For Manufacturing

In this lecture

- PCB Assembly Process
- Soldering Process
- Placement Guide
- Foot Print/pad design Guideline

PCB Assembly

- Manual Assembly or Automated Assembly
- Depends on the class of component technology
  - Class A, B,C, X, Y, Z
- Also Depend on # of boards to be assembled at one time
  - Pannelization
- The method of assembly plays a big role on the layout of the PC board.
  - Clearance, orientation, pad size …

Manual Assembly

- For Prototype and low volume production
- Post-automated assembly for odd shaped components
- Tedious, inconsistent, low yield

Automated Assembly

- “Mostly Automated”
- SMTs are “picked & placed”, then “reflowed” first
- PTHs are “inserted” auto or manual and wave or IR soldered.
- The complete process takes 6 – 9 steps

PCB Assembly

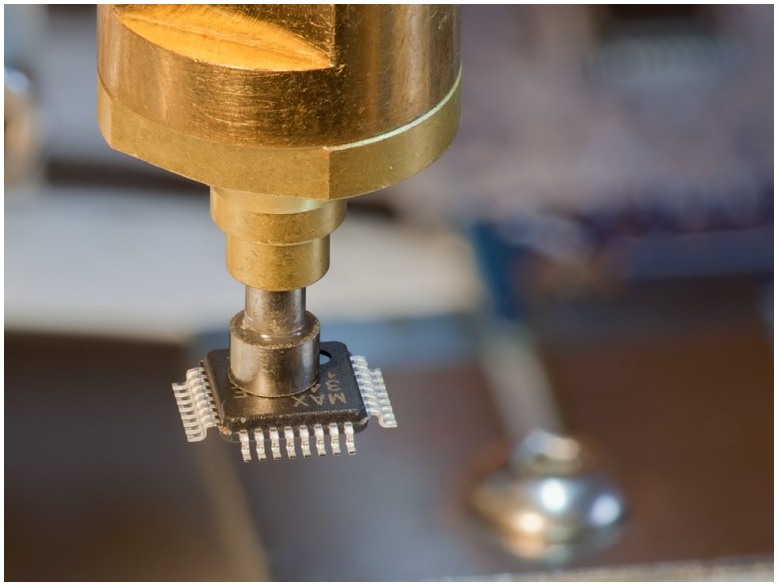
Stencil Printing

- Stencil is a punched aluminum plate in the negative pattern of the solder resist layer.
- Used to apply/"print" solder paste on footprint pads
- A stencil printer can be manual, semi-auto or fully-auto

PCB Assembly

Pick and Place

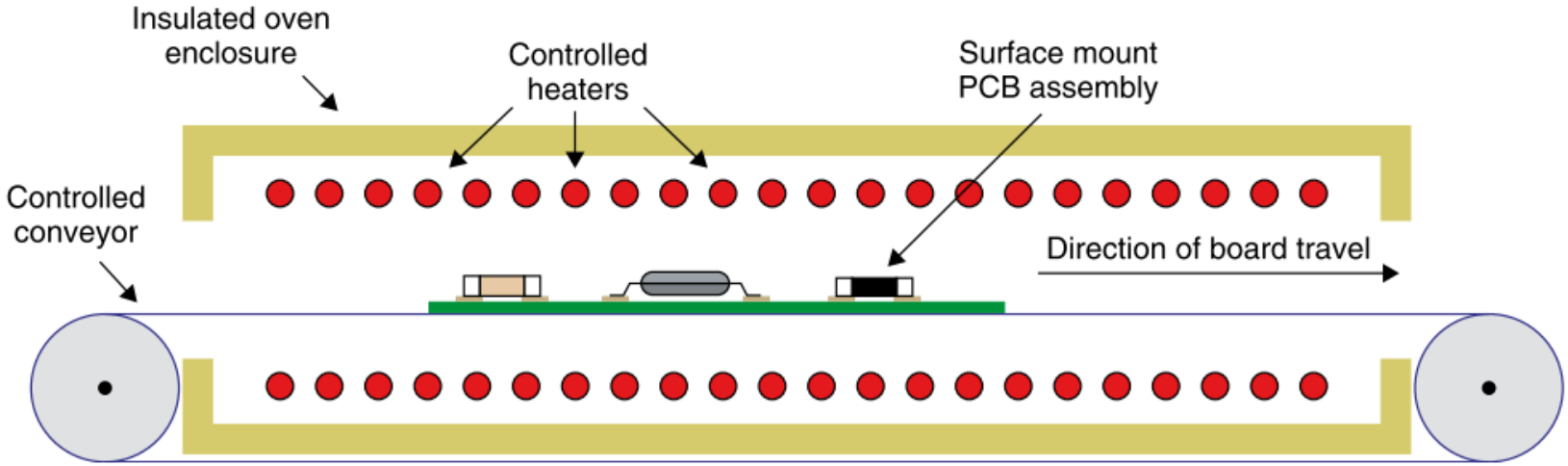
- Components are loaded in reels, tapes, tubes and trays.
- Robotic arm ‘picks and places’ components at high speed and precision
- Equipped with camera, LASER guide and X-ray to place fine-pitch leadless components.



PCB Assembly

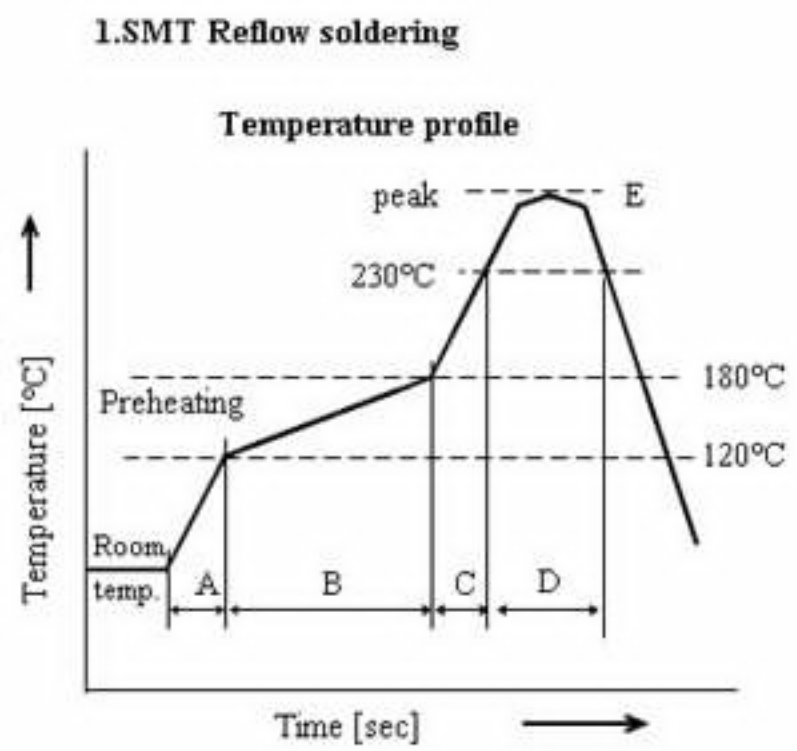
Reflow Soldering

- Used to melt (reflow) the solder paste to form firm connection b/n component pins and PCB pads.
- Performed in spatially temperature controlled oven



PCB Assembly

Reflow Oven and Temperature Profile



PCB Assembly

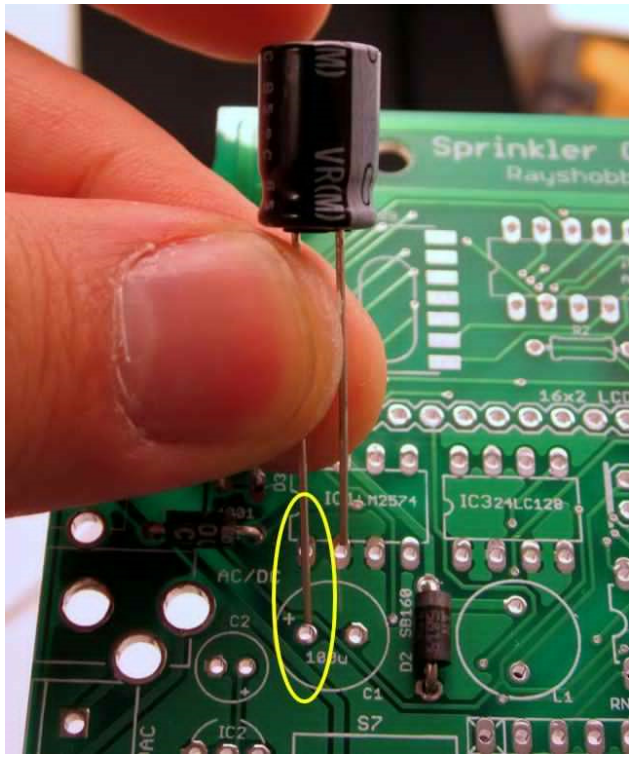
Inspection

- Automated or Visual
- Automated Optical Inspection (AOI)
  - Machine Vision/Artificial Intelligence

PCB Assembly

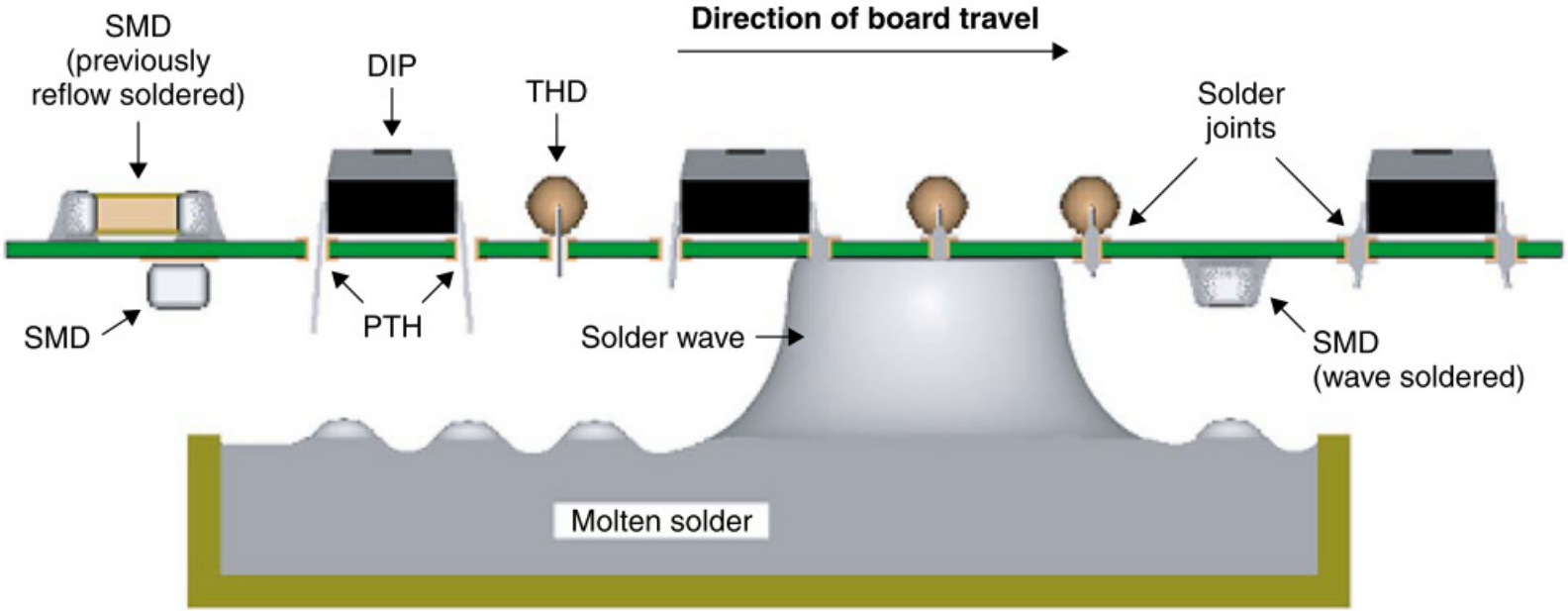
THD Insertion

- Large or odd shaped parts are usually manual inserted
- Small PTH parts can be placed using automatic insertion machine



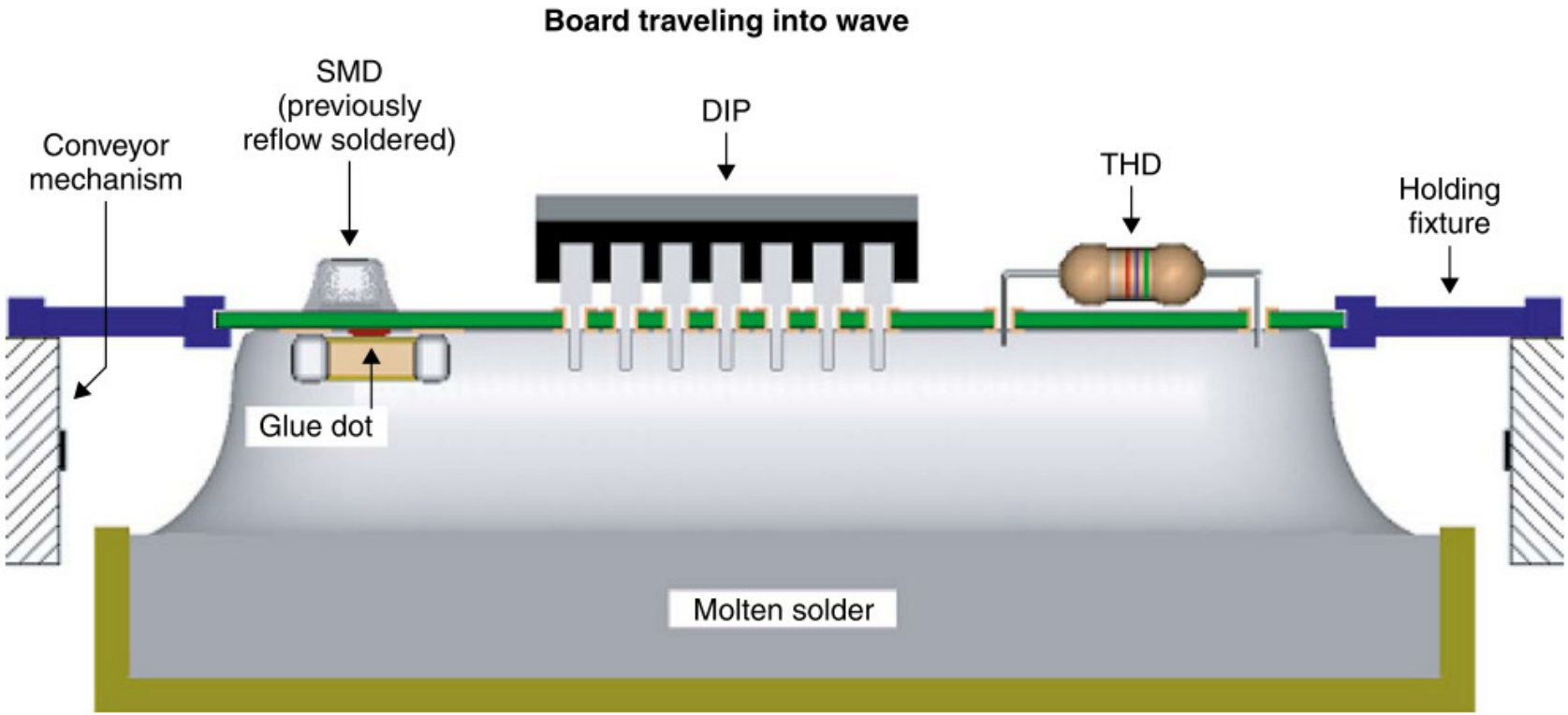
Wave Soldering

- Used to solder PTH components (also SMT parts)
- Board is conveyed atop a bath of molten solder.
- A wave of solder is socked in to metal pads of the PCB thereby joining the component pins and PCB pad



Wave Soldering

- Rear View



Placement Guideline

- The board design has significant impact on how easily parts can be placed and attached to the board and how reliable the end product is.
- How parts are placed and spaced on board depends on:
  - Board topology (class and level)
  - Component technology (SMD or PTH)
  - Soldering method (reflow or wave soldering)
- Placement Orientation and Spacing is dictated by all factors mentioned above

Placement Guideline

1. Components should be placed so that they are neat and organized with uniform spacing and alignment.
2. Components should be oriented such that component ages are parallel to the board edge
3. Keep components only on one side of board whenever possible
4. Polarized capacitors and diodes should be placed consistently throughout the board for ease of optical inspection
5. Allow adequate space along board edges for easy handling
6. Components heavier than 5g/lead should be mechanically supported
7. Electrical issues usually have higher priority over mechanical issues unless it will result in mechanical failure
8. Noise, crosstalk, thermal and power issues should always be taken seriously. Segregate components and PCB area based on these.

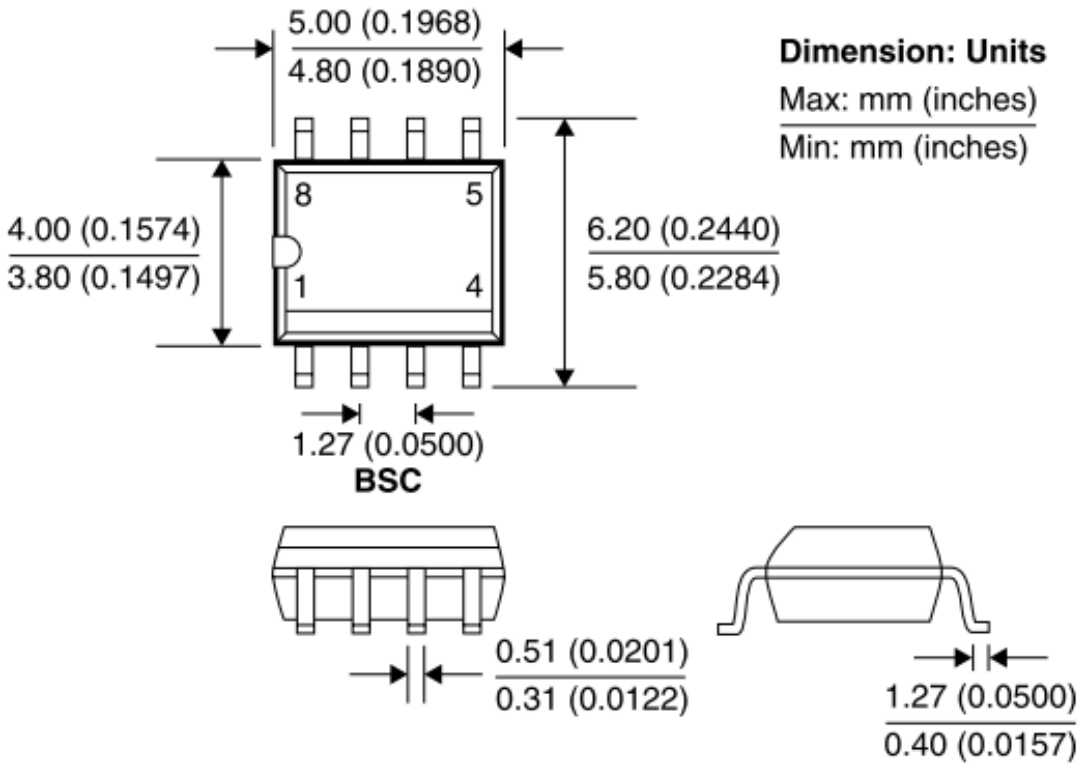
Placement Guideline

Spacing rules by component type refer:

- Text Book on pages 83 – 89
- IPC-2221A, Page 56
- IPC 7351, Tables 3-3 to 3-9

Surface Mounted Devices (SMDs)

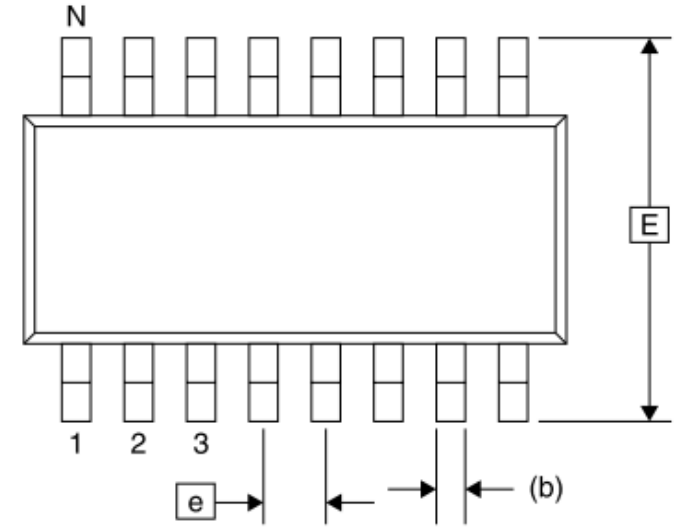
- Follow reference foot print on datasheet or JEDEC
- JEDEC only provides package dimensions not footprint dimensions – Needs translation.



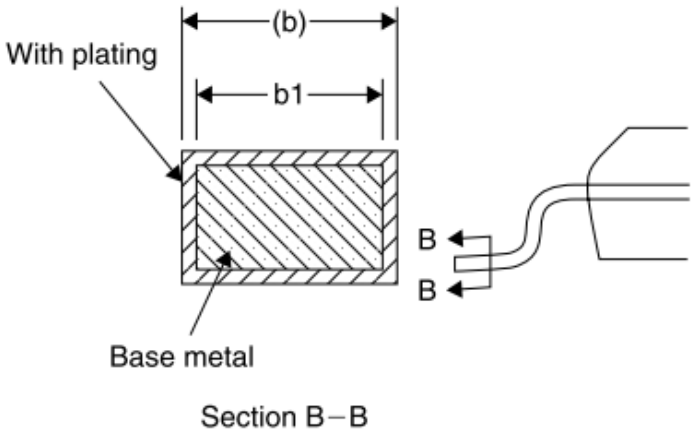
Dimension data for 8 pin Small Outline IC (SOIC-8P) as given in datasheet

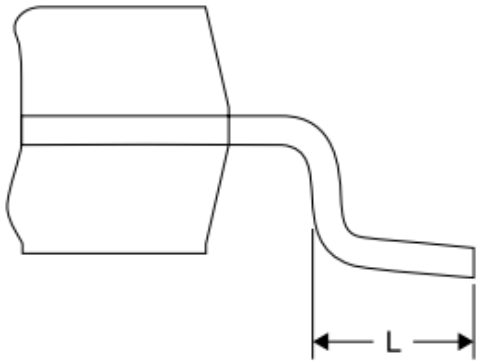
Surface Mounted Devices (SMDs)

- JEDEC Package Dimensions (typical Conventions)



Symbol	Common dimensions			Note
	MIN	NOM	MAX	
b	0.31	–	0.51	7.8
b1	0.28	–	0.48	7.8
E		6.00 BSC		
e		1.27 BSC		
L	0.40	–	1.27	



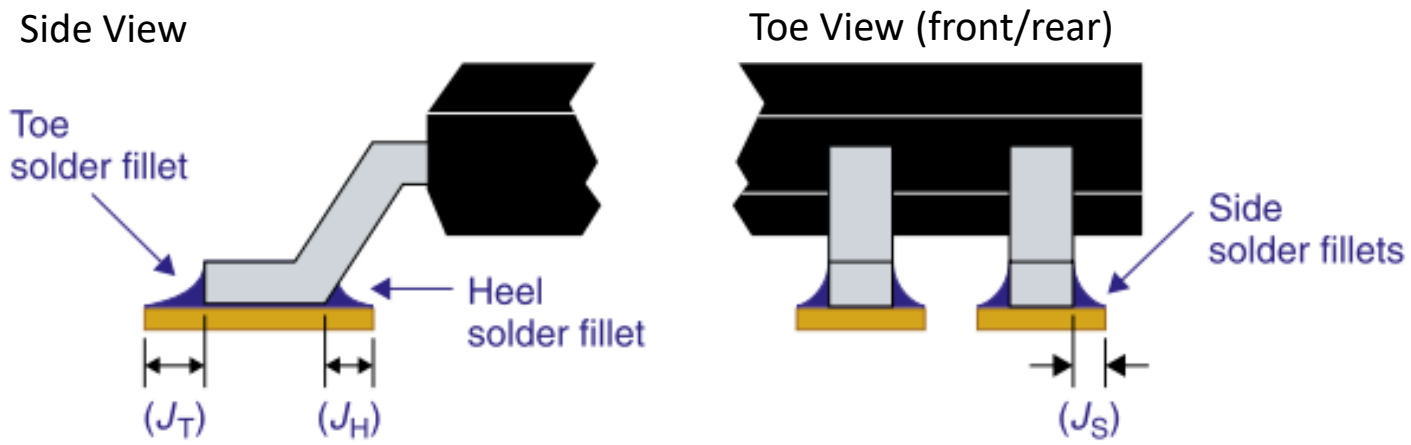


SMDs Padstack design (Padstack = Solder Pad)

- A good padstack promotes the best possible solder joint between a component termination (lead) and the PCB.
- The padstack must allow for:
  - Component dimensional variations
  - PCB fabrication tolerance
  - Placement tolerance and
  - Solder fillet specifications
- IPC-7351 is the standard for SMD padstack design

SMDs Padstack design

- Solder pads needs to be larger than component lead to allow a proper solder joint.



- Values of JT, JH and JS depend on type of Components and desired density level (A to C)
  - Refer Tables 5-8 – 5-9 on page 91 of text book for nominal values

SMDs Padstack design

- The maximum pad width and height can be calculated according to the ff equations:

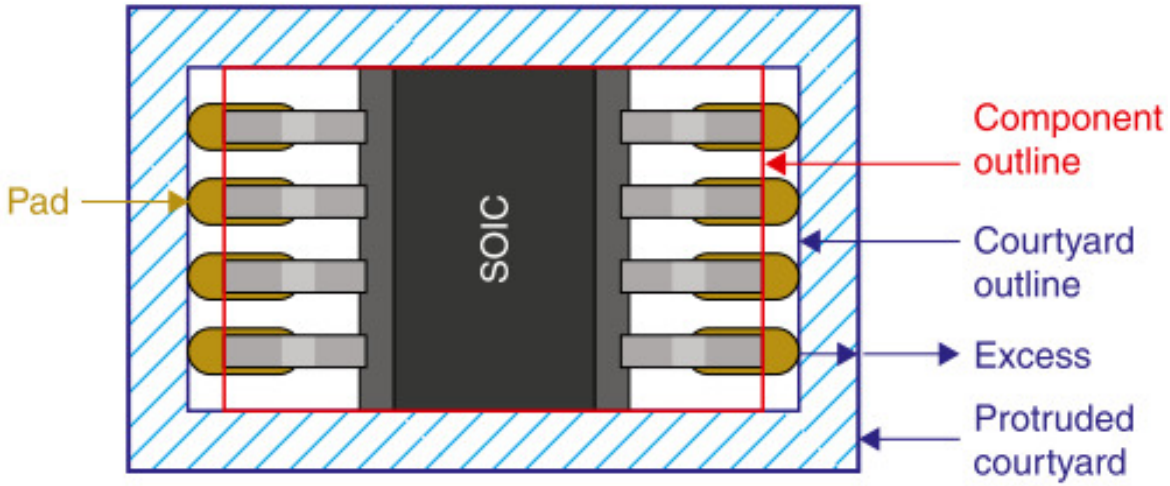
$$W_{P(\mathrm{MAX})} = E_{\mathrm{MIN}} - (E_{\mathrm{MAX}} - 2L_{\mathrm{MIN}}) + 2J_{\mathrm{T}} + 2J_{\mathrm{H}} + 2\sqrt{(E_{TOL(\Delta)})^2 + F^2 + P^2},$$

$$H_{P(\mathrm{MAX})} = b_{\mathrm{MIN}} + 2J_S + \sqrt{(b_{TOL(\Delta)})^2 + F^2 + P^2}$$

  - F = fabrication tolerance, P = placement tolerance
  - Emin, max, tol = distance b/n the ends of the leads and its tolerance
  - bmin, tol = minimum lead width and its tolerance
- Equations are nominal and simplified from IPC-7351

SMD Footprint

- Once the padstack are designed, they need to be correctly located to complete the footprint design.
- 8 pin SOIC example is shown below acc. IPC-7351



- More on Footprint design on Ch-5 on OrCAD

THD Padstack design

- Through-hole devices fall generally into one of the two categories:
  - Axial leaded or radial leaded
- Fig (a) shows radial and (b) axial generic examples

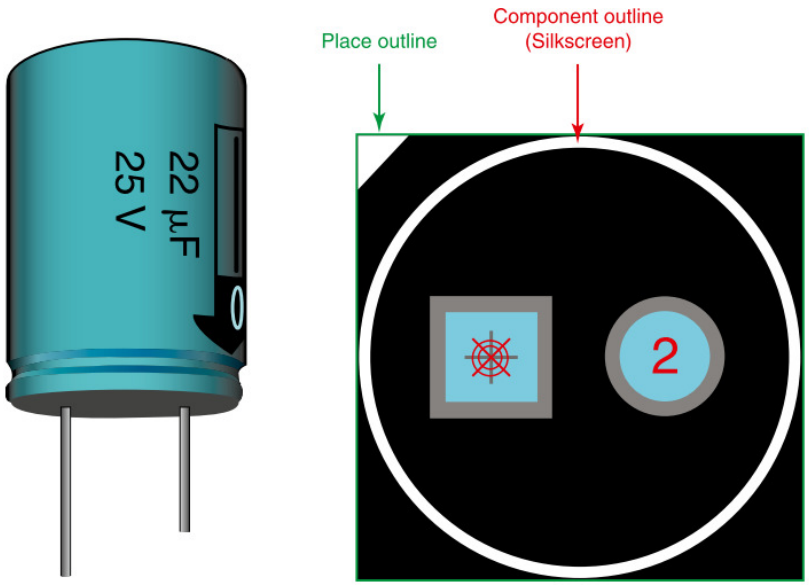


Fig a – radial leaded capacitor

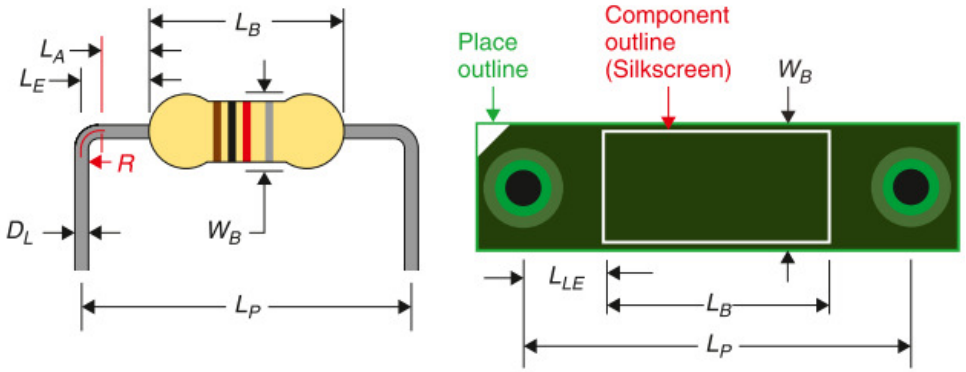
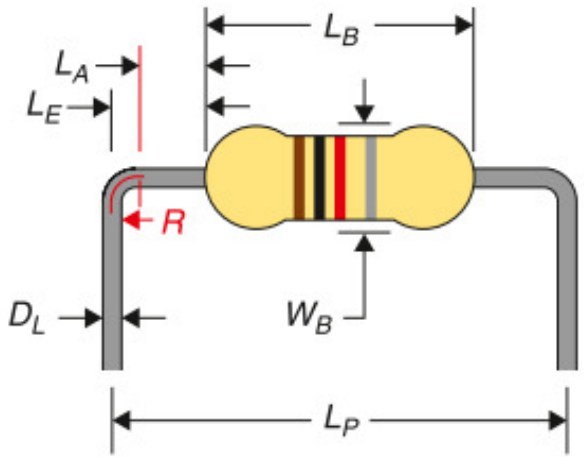
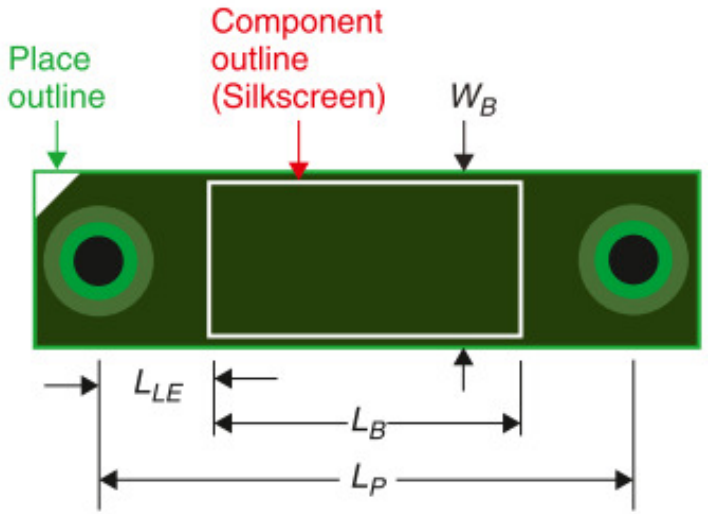


Fig b – axial leaded resistor

THD Padstack design

- Generic padstack guideline:





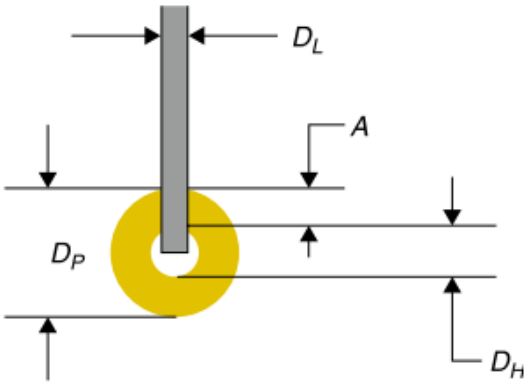
$$L_P = L_B + 2(R + L_A)$$

- The size of PTH hole should be large enough so that the lead can easily slip in to the hole, but not too large to prevent capillary action during soldering.

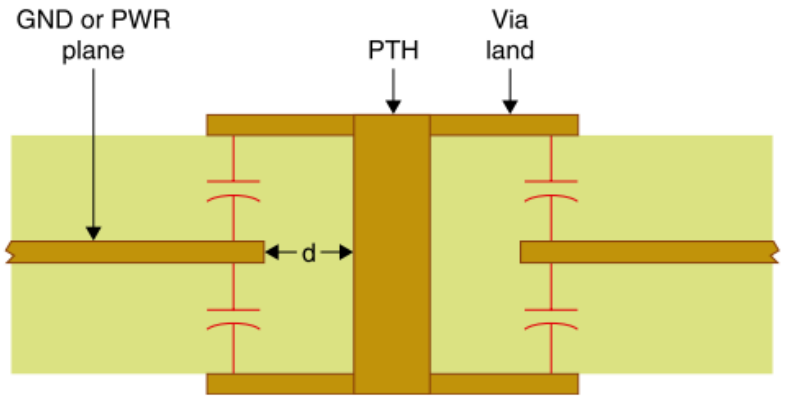
THD Padstack design

- Hole-to-lead ratio is determined in two ways:
  - Using the equation $D_H = (D_L + 2T_P) \times k$

    (DH = hole diameter; DL = lead diameter, Tp =hole plating thickness; K = tolerance (1.05 < K < 3))
  - Or Using a lookup table
- Pad design and clearance from plane layers are shown below



$$D_P = a + 2b + c$$



Oversized pads can create intrinsic capacitors