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Lorenzo Pavesi
David J. Lockwood *Editors*

Silicon Photonics III

Systems and Applications

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Silicon Photonics III

Systems and Applications

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Preface

This is the third volume in the Silicon Photonics series, which we started in 2004 with a book simply entitled Silicon Photonics. At that time, the field was in its infancy and the research was concentrated on the basic building blocks for integrated photonic circuits. Then in 2011, we edited the second volume, Silicon Photonics II: Components and Integration. This volume was devoted to the description of the different requirements needed to integrate the basic building blocks into integrated circuits. Today, we present this book where we focus on the state of the art of silicon photonics in industry and also make comparisons with other competing technologies. It is impressive to see the paradigmatic change that the field has witnessed in just 5 years. Specifically, silicon photonics has moved from the research laboratory to manufacturing companies. Indeed, in the first books, the contributors were mainly from academia, while in the present volume, more than half of them are from companies.

In Chap. 1, the use of silicon photonics to solve the bandwidth bottleneck of inter-chip interconnects is addressed. Fully hybrid integrated systems are described and a bandwidth density of 30 Tbps/cm^2 is demonstrated. In addition, the problem of the temperature reliability of the system is addressed with the discussion of error-free data links operating up to 125 °C at 25 Gbps. The use of quantum physics and its integration in silicon photonics is at the heart of Chap. 2. Quantum technologies promise to revolutionize the way we handle information. Though the control of quantum systems remains extraordinarily challenging, silicon quantum photonics, with its density and manufacturability, is a credible challenger.

One still open issue in silicon photonics is the temperature dependence of many of its components. Chapter 3 reviews the various approaches to overcome the high temperature dependence of wavelength-filtering devices such as ring resonators and arrayed waveguide gratings. Based on specific designs, athermal devices are presented. Key to this achievement is a proper simulation software that enables the development of athermal geometries. Chapter 4 discusses the challenges and the opportunities in photonic integrated circuit design software tools, examines existing design flows for photonic design, and how these fit different design styles.

Modeling of chip-scale interconnects is presented in Chap. 5 with reference to high-performance computer systems that need to distribute extremely large amounts of data in an energy efficient manner. A fully functional co-integrated hardware–software system is presented to encompass device functionality, control schema, and software logic seamlessly. Each layer, ranging from individual device characterization, to higher layer control of multiple devices, to arbitration of networks of devices, and ultimately to encapsulation of subsystems to create the entire computing system is explored.

Silicon photonics is going to enable more and more commercial applications as the technology matures. This will increase the demand for foundries to produce the photonic integrated chip. The accessibility to foundries becomes then a critical aspect for any business models. Chapter 6 reports on the foundry services for multi-project wafer shuttles, customized process runs, and small volume production. Results and challenges in setting up a CMOS manufacturing foundry line for silicon photonics research and development along with commercialization are also presented. A specific aspect is the move from the chip to the packaged device. In Chap. 7 the path from a device-by-device packaging to automatic packaging, which allows scaling to high volumes, is described. Packaging challenges still remain in areas such as fiber array coupling, laser source and electronic integration, and efficient thermal management. The problems and the challenges to automatize the fiber array pigtailing and the laser integration in relation to silicon photonics devices are addressed in Chap. 8. Solving these manufacturing issues, whether silicon photonics needs a dedicated fab or not, still remains an open topic. Megafabs produce 10,000–25,000 12″ wafers per week in their normal capacity. The silicon photonics industry has the potential for approximately 25,000 wafers per year or ~500 wafers per week by 2021. This volume forethought and the path to low-volume production of silicon photonics devices are presented in Chap. 9. With growing production volume, dedicated fabs are needed. Chapter 10 presents the development of silicon photonics within a CMOS line. Cost process issues, efficient electronic and photonic integration, a usable design kit, an industrial testing strategy, and a low cost packaging strategy are discussed and presented from the perspective of a complete industrialization of silicon photonics.

Applications of silicon photonics are diverse. Chapter 11 reports on the use of silicon photonics for signal processors in microwave photonic frontends. These are especially attractive for their compact size and performance. Silicon photonics for optical interconnect applications is addressed in Chap. 12. The development of transceivers is presented starting from wafer process technology to photonic device libraries, to integration with electronic circuits and optical probing technology. An alternative approach to silicon photonics transceivers is discussed in Chap. 13. The heterogeneous integration of InP into a silicon photonics platform enables the inclusion of all photonic elements in a cost-effective manufacturing process. Chapter 14 compares the two technologies and reviews the technical merits of silicon photonics devices and integrated circuits. Various applications such as chip-scale optical interconnects, short-reach communications in datacenters and supercomputers, and metro/long-haul optical transmissions are enabled by the

technical merits of silicon photonics. Specifically, in Chap. 15 silicon photonics for telecom and datacom is reviewed. Detailed architectures to enable high-performance systems are discussed. Chapter 16 focuses on the fundamental and high-speed characteristics of small-footprint integrated optical modulators designed and fabricated with silicon photonics. Here the application framework is digital coherent communication in optical fiber links and the demonstration of long-haul transmission of up to 1000 km in length at a bit rate as high as 128 Gbps is reported. Datacenters are the application discussed in Chap. 17. An overview of optical interconnect requirements for large-scale datacenters is presented here together with a comparison between silicon photonics technologies and more traditional options in meeting these requirements. Finally, Chap. 18 unfolds a technology roadmap of VLSI photonics applications for datacenters from an industrial perspective. The roadmap of the microelectronics industry development indicates that Si will remain the prime microelectronics material. Therefore, sophisticated silicon photonics devices will serve as the backbone for new architecture to bring the next generation of datacenters to the world soon.

We feel honored to be the editors of this series of volumes on Silicon Photonics, because we have witnessed the evolution of this field from a privileged point of view and could accompany it from its infancy to full maturity. Nevertheless, in these volumes, we have also tried to perceive the future of silicon photonics in terms of both industrial applications and fundamental research. We thank all the authors of the present volume for their invaluable contributions, the staff of Springer for their support, and our co-workers for sharing with us their research in this field. We look forward to further excitement ahead and new developments in silicon photonics, and we hope to share them with you, our esteemed readers, in the next volume of this series.

Trento — Lorenzo Pavesi
Ottawa — David J. Lockwood
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Contents

1 Silicon Optical Interposers for High-Density Optical Interconnects 1
Yutaka Urino, Takahiro Nakamura and Yasuhiko Arakawa
1.1 Introduction 1
1.1.1 Trends and Requirements of Computing Systems in Data Centers 1
1.1.2 Problems with Electrical Interconnects 2
1.1.3 Optical Interconnects with Silicon Photonics 3
1.1.4 Vision for on-Chip Servers 3
1.1.5 Photonics-Electronics Convergence System Technology (PECST) Project 4
1.2 Photonics–Electronics Convergence System for Inter-chip Interconnects 4
1.2.1 Optical Interconnects for Short Reach 4
1.2.2 Integration Between Photonics and Electronics 5
1.2.3 Light Source Integration 6
1.2.4 Photonics–Electronics Convergence System with Silicon Optical Interposers 8
1.3 Configuration and Characteristics of Optical Components for Silicon Optical Interposers 9
1.3.1 Silicon Optical Waveguides 9
1.3.2 Hybridly Integrated On-Chip Light Sources 10
1.3.3 Silicon Optical Modulators 14
1.3.4 Germanium Photodetectors 15
1.4 Silicon Optical Interposers for High Bandwidth Density 16
1.4.1 Design Consideration for Bandwidth Density and Optical Power Budget 16
1.4.2 Integrated Fabrication Process 17
1.4.3 Data Link Experiments 18
1.4.4 Significance of Bandwidth Density 20

1.5 Silicon Optical Interposers for Wide Temperature Range Operation . . . 20
1.5.1 Hybridly Integrated Athermal Light Sources and Their Thermal Characteristics . . . 21
1.5.2 Optical Modulators and Their Thermal Characteristics . . . 23
1.5.3 Photodetectors and Their Thermal Characteristics . . . 25
1.5.4 Data Link Experiments Over Wide Temperature Range . . . 26
1.6 25-Gbps Data Links Using Silicon Optical Interposers and FPGA Transceivers . . . 28
1.7 Advanced Fabrication Process and Optical Components for Wider Bandwidth in Future . . . 30
1.7.1 Hybridly Integrated 1200-Channel Light Source . . . 30
1.7.2 High-Speed Ring-Resonator-Based Optical Modulators . . . 31
1.7.3 High-Speed Germanium Photodetectors with Low Contact Resistance . . . 31
1.7.4 300-mm Wafer Processes with ArF Immersion Lithography for WDM . . . 32
1.8 Perspectives on Inter-chip Interconnects . . . 32
1.8.1 Vision for On-Board Datacenters . . . 32
1.9 Optical I/O Cores . . . 33
1.9.1 Further Efficient Interconnects for On-Board Datacenters . . . 35
1.10 Conclusion . . . 35
References . . . 36

2 Silicon Quantum Photonics . . . 41
Damien Bonneau, Joshua W. Silverstone and Mark G. Thompson
2.1 Introduction . . . 41
2.1.1 Quantum Information . . . 43
2.1.2 Optical Requirements for Quantum Applications . . . 45
2.1.3 Scaling up Quantum Optics . . . 48
2.1.4 Silicon Quantum Photonics . . . 48
2.2 Linear Optics . . . 49
2.2.1 Beam Splitter . . . 50
2.2.2 Phase Shifter . . . 52
2.3 Photon Sources . . . 53
2.3.1 Requirements for Photon Sources . . . 54
2.3.2 A Brief Summary of SFWM Experiments in SOI . . . 54
2.3.3 Theory of SFWM Sources . . . 55
2.3.4 Silicon Waveguide Photon-Pair Sources . . . 57
2.3.5 Ring Resonator . . . 62
2.4 On-Chip Detectors . . . 69

2.5 Integration . . . 70
2.5.1 Multiple Sources . . . 71
2.5.2 Sources and Filters . . . 72
2.5.3 Multiple Sources and Interferometers . . . 74
2.6 Outlook . . . 75
2.6.1 Conclusion . . . 75
References . . . 76

3 Athermal Silicon Photonics . . . 83
Jong-Moo Lee
3.1 Introduction . . . 83
3.2 Background of Athermal Technology . . . 84
3.2.1 Temperature-Dependent Wavelength Shift . . . 84
3.2.2 Thermo-Optic Coefficient of Materials . . . 85
3.2.3 Athermal Silica AWG . . . 86
3.3 Athermal Silicon Photonics Using Polymer Cladding . . . 88
3.4 Athermal Silicon Photonics Using Titania Cladding . . . 93
3.5 Athermal Silicon MZI Without Negative TO Material . . . 95
3.6 Summary . . . 97
References . . . 97

4 Design Flow Automation for Silicon Photonics: Challenges, Collaboration, and Standardization . . . 99
Mitchell Heins, Chris Cone, John Ferguson, Ruping Cao, James Pond, Jackson Klein, Twan Korthorst, Arjen Bakker, Remco Stoffer, Martin Fiers, Amit Khanna, Wim Bogaerts, Pieter Dumon and Kevin Nesmith
4.1 Silicon Photonics—History Repeats Itself . . . 100
4.2 Photonic Integrated Circuit Design Methodologies and Flows . . . 100
4.2.1 Front End Versus Building Blocks Methodology . . . 101
4.2.2 Process Design Kit Driven Design . . . 101
4.2.3 Overview of Flow—Comparison to Analog Design Flow . . . 103
4.2.4 Schematic Capture . . . 106
4.2.5 Photonic Circuit Modeling . . . 108
4.2.6 Model Extraction for Compact Models . . . 114
4.2.7 Schematic-Driven Layout . . . 116
4.2.8 Overview of Physical Verification for Silicon Photonics . . . 122
4.3 Manufacturing and Lithography: Accuracy Problems and Process Variation . . . 139
4.3.1 Silicon Photonics Fabrication Processes . . . 139
4.3.2 Lithography . . . 140

4.4 The "CoDesign" Problems. 142
4.4.1 Co-layout 143
4.4.2 Co-simulation 143
4.4.3 Cointegration 144
4.4.4 Packaging 145
4.5 Standards Organizations Helping Evolve a Disintegrated Design, Manufacturing, Packaging, and Test Ecosystem 145
4.5.1 Photonics Fitting into EDA 145
4.5.2 Adding/Modifying for Photonics 146
4.5.3 Process Design Kits (PDKs) 146
4.5.4 Formats. 150
4.5.5 Standards Development Organizations. 150
4.6 The Need for an Optoelectronic Unified Design Flow. 152
4.7 Summary 154
References 154

5 Hardware–Software Integrated Silicon Photonics for Computing Systems 157
David M. Calhoun, Qi Li, Dessislava Nikolova, Christine P. Chen, Ke Wen, Sébastien Rumley and Keren Bergman
5.1 Silicon Photonic Systems: A Subsystem Rationale 157
5.2 Chip-Scale Silicon Photonic Subsystems 158
5.2.1 Silicon Photonic Manufacturing Platforms 159
5.2.2 Photonic Packaging 159
5.2.3 End-to-End Connection in a Silicon Photonic Link. . . . 160
5.2.4 Systems Enabled by Programmable Logic Devices 162
5.2.5 System Considerations 163
5.3 Device Control for Thermal Stabilization 163
5.4 High-Speed Silicon Photonic Subsystems 164
5.4.1 Traveling-Wave Mach–Zehnder Modulator and Microring Modulators 165
5.4.2 Mach–Zehnder Interferometer and Microring Switches 167
5.4.3 Microring Performance Dependencies 168
5.5 Data Synchronization for Link-Based Delivery and Management 169
5.5.1 Burst Mode Data for Link Connections. 169
5.5.2 Synchronization 170
5.5.3 Exploring Software Protocols for Circuit-Based Connection Management of Characterized Links 173
5.6 Hardware–Software Implementation for System Integration 175
5.6.1 Abstracting a Chip-Scale Silicon Photonic System 176
5.6.2 Software Control and Management. 178
5.6.3 Example of Software Request-Grant-Based Control of Switched Silicon Photonic Circuits 181

5.6.4 Control-Centric Integration: Power-Optimized Silicon Photonic Spatial Switching 182
5.6.5 Network-Centric Integration: Programmable Wavelength Routing 184
5.7 Conclusion 186
References 186

6 Path to Silicon Photonics Commercialization: The Foundry Model Discussion 191
Andy Eu-Jin Lim, Tsung-Yang Liow, Jun-Feng Song, Ming-Bin Yu, Chao Li, Xiao-Guang Tu, Kok-Kiong Chen, Roger Poh-Cher Tern, Ying Huang, Xian-Shu Luo and Guo-Qiang Lo
6.1 Introduction 191
6.2 Silicon Photonics Technology Status 192
6.2.1 Fabless Semiconductor Model 192
6.2.2 Monolithic Integration Through CMOS Photonics 193
6.2.3 Technology Platform for Hybrid Integration 195
6.3 Role of Research and Development Foundries 199
6.3.1 Standardized Shuttle Runs 199
6.3.2 Customized Process Platform 202
6.3.3 Small Volume Production 202
6.4 Route to Commercialization 204
6.4.1 Manufacturing in CMOS Foundry 205
6.4.2 Process Qualification and Reliability 209
6.4.3 Outlook and Trends 210
6.5 Conclusion 212
References 213

7 Packaging of Silicon Photonic Devices 217
Peter O'Brien, Lee Carrol, Cormac Eason and Jun Su Lee
7.1 Introduction 217
7.2 Optical Packaging 220
7.2.1 Fiber-Coupling 221
7.2.2 Grating-Coupling 222
7.2.3 Edge-Coupling 225
7.2.4 Laser Integration 226
7.2.5 Micro-Optic Hybrid Integration 227
7.2.6 VCSEL Hybrid Integration 228
7.3 Electrical Packaging 228
7.3.1 Packaging to PCB 229
7.4 Standardization 232
7.5 Conclusions 233
References 233

8 Silicon Photonics Packaging Automation: Problems, Challenges, and Considerations 237
Giovan Battista Preve
8.1 Introduction 237
8.2 Automated Fiber Array Pigtailing on Gratings 239
8.3 Optical Fiber Interface and Laser Integration on PICs: A Survey of Innovative Concepts and Automation Considerations 248
8.3.1 Optical Interface with External Fibers 249
8.3.2 Approach Two 250
8.3.3 Laser Integration on PICs 256
8.4 Conclusions 258
References 258

9 CMOS Cost–Volume Paradigm and Silicon Photonics Production 261
Amit Khanna, Dieter Bode, Carl Das, Philippe Absil and Steve Beckers
9.1 Introduction 261
9.2 Low Volume Production 263
9.2.1 Multi-project Wafers or MPWs for Affordable Prototyping 263
9.2.2 Commercial R&D Project 264
9.2.3 Corner Lot 265
9.2.4 Low Volume Production Lot 266
9.3 Markets and Volumes 266
9.3.1 Datacom 266
9.3.2 Telecom 268
9.3.3 Sensors 268
9.3.4 Volume Evolution 269
9.4 From Prototype to Volume Production: Technical Stages and Challenges 270
9.4.1 PDK and Design Flow 270
9.4.2 New Tape-Out (NTO) 270
9.4.3 Flow Setup and Follow-up 273
9.4.4 Qualification and Yield Analysis 274
9.4.5 Dicing 274
9.4.6 Packaging and Reliability 275
9.5 Summary 275
References 275

10 Silicon Photonics Research and Manufacturing Using a 300-mm Wafer Platform 277
Frédéric Bœuf, Jean Francois Carpentier, Charles Baudot, Patrick Le Maitre and Jean-Robert Manouvrier
10.1 Introduction 277
10.2 Industrialization Strategy and Electronics: Photonics Integration 279
10.2.1 Silicon Photonics Qualification Methodology 279
10.2.2 Electronics and Photonics Integration 280
10.2.3 Industrial Testing Strategy for Wafer Sorting 283
10.3 Photonics Process Integration and Process Control on 300 mm Wafers 285
10.3.1 Optical Component Patterning 286
10.3.2 Active Optical Component Definition 287
10.3.3 Middle of Line (MEOL) and Back End of Line (BEOL) 287
10.3.4 Device Performance 287
10.3.5 Toward Optical Test Chip Development for Process and Performance Monitoring 288
10.4 Design Kit and Spice Model Approach 294
10.4.1 Photonics Spice Model Development 295
10.4.2 Spice Model Extraction Flow 298
10.4.3 Spice Models Hardware Correlation 298
10.4.4 Spice Model Platform Capabilities 300
10.5 Process Exploration for Design and Performance Improvement 301
10.5.1 Improving Surface Coupling Efficiency 302
10.5.2 Advanced Silicon Patterning 306
10.5.3 Application to Ring Modulator Devices 308
References 312

11 Silicon Photonics-Based Signal Processing for Microwave Photonic Frontends 317
Minghua Chen, Hongchen Yu and Jingjing Wang
11.1 Introduction 317
11.2 Silicon-Based Signal Processors 318
11.2.1 FIR Signal Processors 319
11.2.2 IIR Signal Processors 326
11.2.3 FIR/IIR Hybrid Signal Processors 327
11.3 Silicon Photonics-Based Photonic Frontends 331
11.3.1 Parallel Down-Conversion Frontends 331
11.3.2 OEO Frontends 333
11.4 Photonic-Assisted SDR Transceiver 338
11.5 Conclusions 344
References 345

12 Advanced Silicon Photonics Transceivers 349
Attila Mekis, Thierry Pinguet, Gianlorenzo Masini, Subal Sahni, Michael Mack, Steffen Gloeckner and Peter De Dobbelaere
12.1 Introduction 349
12.2 Silicon Photonics for Optical Interconnect 350
12.3 Silicon Photonics Technology Advancements 351
12.3.1 Silicon Photonics Wafer Processing Flow 351
12.3.2 Silicon Photonics Devices 354
12.3.3 2.5 D Integration for Combining Electronic and Photonic Circuits 357
12.3.4 Wafer-Scale Optical Probing of Silicon Photonics 358
12.4 Advanced Optical Transceiver Design in Silicon Photonics Technology 361
12.4.1 Design Infrastructure: Design Kit 361
12.4.2 Transmitter Design 362
12.4.3 Receiver Design 364
12.4.4 Transceiver Architecture 365
12.5 Light Source for Silicon Photonics 367
12.6 Packaging 371
12.7 Conclusions 372
References 373

13 Optical Transceivers Using Heterogeneous Integration on Silicon 375
Gregory A. Fish and Daniel K. Sparacin
13.1 Introduction 375
13.2 Heterogeneous Integration 376
13.2.1 Components 379
13.2.2 Lasers 379
13.2.3 Semiconductor Optical Amplifiers 380
13.2.4 Modulators 381
13.2.5 Photodiodes 382
13.2.6 Circuits 383
13.3 Packaging 390
13.4 Conclusion 394
References 394

14 Merits and Potential Impact of Silicon Photonics 397
Po Dong, Guang-Hua Duan, Young-Kai Chen and David T. Neilson
14.1 Technical Merits of Silicon Photonic Devices 398
14.1.1 High-Index-Contrast Silicon Waveguides 398
14.1.2 High Integration Level of Silicon Photonics 400
14.1.3 High Yield and Low Cost by Mature CMOS Fabrication 401

14.2 Applications 403
14.2.1 Telecommunication Applications 403
14.2.2 DataComm Applications 406
14.2.3 Chip-Scale Interconnects 408
14.3 Silicon Photonic Integrated Circuits 410
14.3.1 WDM Transmitters 410
14.3.2 WDM Receivers 412
14.3.3 Coherent Optical Transmitters 413
14.3.4 Coherent Optical Receivers 414
14.4 Conclusion 416
References 417

15 Silicon Photonics for Telecom and Datacom Applications 421
Francesco Testa, Alberto Bianchi, Stefano Stracca and Roberto Sabella
15.1 Introduction 422
15.2 Optical Switching Devices for Access and Mobile Networks 422
15.2.1 Silicon Integrated Mini-ROADM 425
15.2.2 Silicon Integrated Devices for Multidirectional ROADMs 429
15.3 High Scale Photonic Integrated Device for Optical Switching in Metro Transport Nodes and Data Centers 432
15.3.1 Silicon Photonics Integrated TPA: IRIS Project 436
15.4 Perspectives and Research Directions 443
References 444

16 Is Silicon Photonics a Competitive Technology to Enable Better and Highly Performing Networks? 447
Kensuke Ogawa and Kenji Nishide
16.1 Introduction 448
16.2 Fundamental Characteristics of Rib-Waveguide Phase Shifter 449
16.2.1 Rib-Waveguide Phase Shifter in MZ Interferometer . . . 449
16.2.2 Optical Loss Characteristics 451
16.2.3 Series Resistance Reduction for Shorter RC Delay 455
16.2.4 EO Response 457
16.3 Free-Carrier Plasma Dispersion for High-Speed Silicon Optical Modulator 458
16.3.1 Energy Transfer in Drude Theory 458
16.3.2 TEC-Free DC Optical Characteristics 460
16.3.3 Frequency Chirping 460

16.4 Silicon Optical Modulators in High-Capacity Optical Networks . . . 462
16.4.1 On-off Keying Characteristics . . . 462
16.4.2 Phase-Shift Keying Characteristics . . . 464
16.5 Conclusion . . . 469
References . . . 469

17 Silicon Photonics Technologies: Gaps Analysis for Datacenter Interconnects . . . 473
Ryohei Urata, Hong Liu, Lieven Verslegers and Chris Johnson
17.1 Introduction . . . 473
17.1.1 The New Internet . . . 473
17.1.2 Datacenter Network Architecture . . . 475
17.2 Performance Metrics for Intra-datacenter Interconnect . . . 476
17.2.1 Cost . . . 476
17.2.2 Power, Density, Size . . . 478
17.2.3 Cable Efficiency . . . 480
17.2.4 Latency . . . 481
17.2.5 Serviceability: Pluggable Versus Embedded Transceivers . . . 482
17.2.6 Performance . . . 485
17.3 Conclusion . . . 486
References . . . 487

18 VLSI Photonics for High-Performance Data Centers . . . 489
Di Liang, Marco Fiorentino and Raymond G. Beausoleil
18.1 Photonic-Interconnected Data Center Architectures . . . 490
18.2 Si Microring-Based Transceivers . . . 496
18.3 Hybrid III–V-on-Si Transceivers . . . 500
References . . . 511

Index . . . 517

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Chapter 1
Silicon Optical Interposers for High-Density Optical Interconnects

Yutaka Urino, Takahiro Nakamura and Yasuhiko Arakawa

Abstract One of the most serious challenges in the information industry is bandwidth bottlenecks in inter-chip interconnects. We proposed a photonics–electronics convergence system in response to this issue, demonstrated silicon optical interposers integrated with all optical components on a silicon substrate, and achieved a high bandwidth density of 30 Tbps/cm^2, which is sufficient for the needs of the late 2010s.

1.1 Introduction

1.1.1 Trends and Requirements of Computing Systems in Data Centers

First, we give an overview of the trends in computing systems mainly used in data centers, and point out requirements led by these trends. In the application layer, the most significant trend is data explosion. According to a report from IBM, 90 % of data in the world was created in the last 2 years alone [1]. This is a simple and impressive fact to understand the speed of the recent data explosion. The data explosion speed is expected to become faster due to the penetration of data analytics using "big data" and Internet of Things (IoT), because these applications will

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handle much bigger data sets than conventional web-searching or video-casting. Data centers are facing serious challenges to catch up with this data explosion. These trends are encouraging a shift to data-centric computing in data centers.

In the system layer, we believe that "disaggregation" of computing resources such as processors, memories, storages, and networks to make the system more flexible, scalable, and efficient is a notable new trend, as well as data-centric computing [2]. These trends require wider bandwidth and longer reach for interconnects between devices. The appearance of mega data centers also requires longer reach interconnects.

In the device/module layer, we point out three trends. First, although transistor size is still shrinking based on Moore's law, its clock frequency has already hit the ceiling [3]. This trend is consequently requiring enhanced performance from many-core processors (MCPs) by means of parallelism. As a result, data quantity handling within a processor die is still growing. The second trend is three-dimensional (3-D) packaging, which has been mainly introduced for stacked memory modules such as Wide I/O 2 [4], high bandwidth memory (HBM) [5], and hybrid memory cube (HMC) [6], and successfully provides large capacity and wide bandwidth for inter-die (intra-module) interconnects by using through-silicon vias (TSVs). The 3-D packaging can be also applied to increase the capacity of non-volatile memory such as flash memory used as a solid-state drive (SSD), for data storage. As a result, data quantity handling within a memory module is also increasing. The third trend is system in a package (SiP) or multi-chip module (MCM), which consists of multiple chips in a single package and provides multiple functions with higher flexibility and shorter developing time than system on a chip (SoC). Generally, SiP can be implemented by 2.5-D packaging, where some bare dice are stacked vertically and some single chips or stacked dice are mounted side-by-side on an interposer. All of these three trends also require wider bandwidth for inter-chip interconnects.

1.1.2 Problems with Electrical Interconnects

Although wider bandwidth for inter-chip interconnects is required from application, system and device/module layers, the bandwidth of conventional inter-chip interconnects with electric wires is limited due to their low channel line rate and low input/output (I/O) pin density, namely low bandwidth density. For example, we estimate the required inter-chip bandwidth will be several tens of Tbps in the late 2010s, while LSI I/O pad pitches, such as flip-chip pad pitches, are expected to remain large at around 100 μm [7]. This is why the required line rate for inter-chip interconnects is estimated to exceed 40 Gbps by the late 2010s, and there are currently no known solutions to achieve the line rate with electrical interconnects on a printed circuit board (PCB) [7]. The reach of electric wires with a high channel line rate is also limited due to their high transmission loss on the PCB and reflections at connectors.

1.1.3 Optical Interconnects with Silicon Photonics

Optical interconnects with silicon photonics are potential candidates for solving the bandwidth bottleneck and limited reach problem and have been investigated [8–11]. We believe they have three major advantages. The first is the intrinsic properties of optical signals, such as wide bandwidth, low latency, low power consumption, and low mutual interference, compared with those of electrical signals. The second is the industrial advantages of silicon with which we can share the huge amount of existing resources in the electronics industry in terms of design, fabrication, testing, and supply chain. For example, we can use electronic design automation (EDA) tools and foundry services with 300-mm wafers for silicon photonics as with electronics. The common platforms between photonics and electronics also lead to high adaptability to photonics–electronics convergence. The third is the compactness due to their optical waveguides (OWs) with high refractive index contrast. The device compactness also leads to high performance in terms of speed and power consumption.

1.1.4 Vision for on-Chip Servers

Based on the examination of the above-mentioned trends, requirements, and problems of computing systems in data centers, we have propose a concept of an on-chip server in which the functions and performance of a present on-board server will be integrated on a substrate in the 2020s, as shown in Fig. 1.1 [12]. It is a kind of SiP or MCM. A 3-D MCP, 3-D memory (3-D Mem), and 3-D SSD are integrated on an interposer. While the vertical interconnects between stacked dice are electrical through TSV, horizontal interconnects between modules that consist of the stacked dice are mainly optical with silicon photonics. We call this system the photonics–electronics convergence system. More details are given in the following sections.

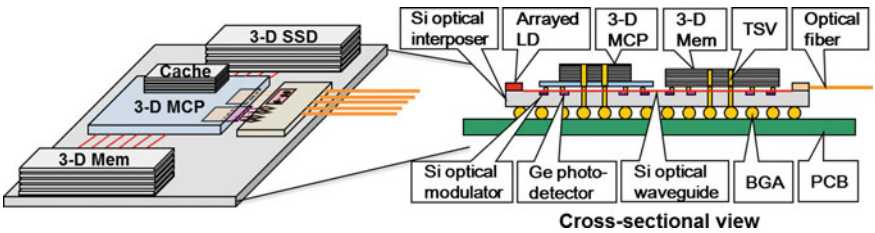


Fig. 1.1 On-chip servers based on silicon optical interposers

1.1.5 Photonics-Electronics Convergence System Technology (PECST) Project

To develop interconnects for future on-chip servers in Japan, the Photonics-Electronics Convergence System Technology (PECST) project was started in March 2010 as one of the 30 Funding Programs for the World-Leading Innovative R&D on Science and Technology (FIRST) projects supported by the Council for Science and Technology Policy in the Cabinet Office. This project was carried out for 4 years, mainly involving the University of Tokyo, Photonics Electronics Technology Research Association (PETRA), and Advanced Industrial Science and Technology (AIST). The PECST aimed to establish chip-to-chip interconnect technologies with a bandwidth density of 10 Tbps/cm^2. This chapter mainly describes the vision, methods, and achievements of the PECST project.

In Sect. 1.2 of this chapter, we first introduce our proposed photonics–electronics convergence system based on silicon optical interposers and in Sect. 1.3, we explain the configuration and characteristics of optical components for silicon optical interposers. Then, we discuss the evaluation of these optical interposers for high bandwidth density and wide temperature range operation in Sects. 1.4 and 1.5. Furthermore, we discuss the 25-Gbps data links using silicon optical interposers in Sect. 1.6 and the advanced fabrication and optical components for wider bandwidth in Sect. 1.7. Finally, we provide a perspective on inter-chip interconnects in Sect. 1.8 and conclude the chapter in Sect. 1.9.

1.2 Photonics–Electronics Convergence System for Inter-chip Interconnects

1.2.1 Optical Interconnects for Short Reach

Figure 1.2 shows the building blocks of optical interconnects, which consist of a light source, light distributor, electrical-to-optical (E/O) signal converter, optical wire, optical to electrical (O/E) signal converter, transmitter (Tx) circuits, and receiver (Rx) circuits. The photos in the figure show our optical components for examples of an arrayed laser diode (LD), silicon optical splitter (OS), silicon optical modulator (OM), silicon OW, and germanium photodetector (PD). With this system, light is not modulated directly by the light source, so the light source is not required to have high-speed operation but high output power is required for multichannel distribution. To build the integrated optical interconnects, we have to examine two integration methods, photonics–electronics integration and light source integration.

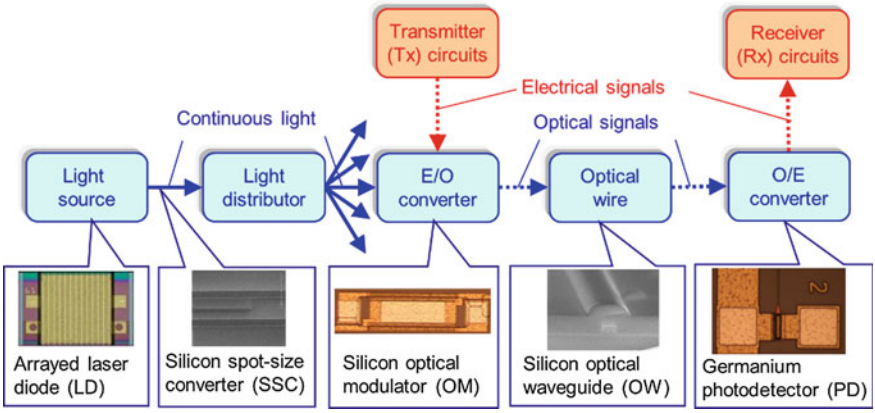


Fig. 1.2 Building blocks of optical interconnects

1.2.2 Integration Between Photonics and Electronics

Because the performance of electrical interconnects generally declines more rapidly with their distance than does that of optical interconnects, it is important to place optical transceivers (E/O and O/E signal converters) as close to large-scale integration (LSI) chips as possible for wide-bandwidth inter-chip interconnects with photonic wiring. Silicon photonics is the most suitable technology for these applications because of its compactness and compatibility with LSIs.

Generally, there are three types of integration methods between photonic and electronic circuits with silicon photonics. Their schematic cross sections are shown in Fig. 1.3: front-end integration, back-end integration, and flip-chip bonding. In front-end integration, both electronic and photonic circuits are integrated near the surface of a silicon substrate by a front-end process. In back-end integration, photonic circuits are integrated on the wiring layer by a back-end process. In flip-chip bonding, electronic and photonic chips are fabricated separately then stacked by flip-chip bonding. The first two are monolithic integrations and the last is a hybrid integration. The characteristics of these integrations are compared in Table 1.1. Monolithic integration, especially front-end integration, is expected to provide higher speed and lower assembling cost than hybrid integration, but it requires very strict CMOS compatibilities in terms of design, fabrication, and testing. We believe that it will be a long time before the technology is mature enough. In contrast, hybrid integration enables us to individually choose the most suitable technology nodes for photonic and electronic circuits, to design, fabricate and test them separately, and then combine their good dies. This scheme can improve product yields and stimulate horizontal specialization between electronics and photonics or between LSI chips and their inter-chip interconnects. Therefore,

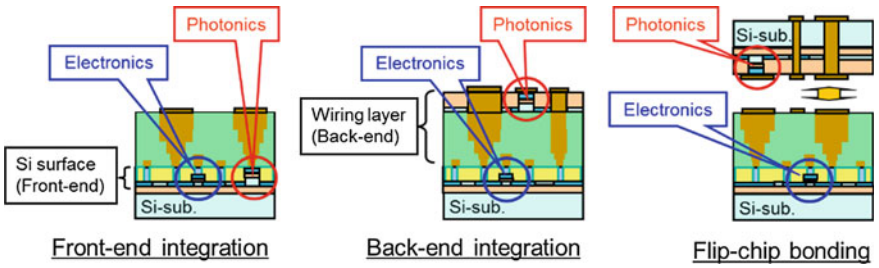


Fig. 1.3 Schematic cross sections of integration between photonic and electronic circuits

Table 1.1 Comparison of photonics–electronics integration methods

Integration type	Monolithic		Hybrid
	Front-end integration	Back-end integration	Flip-chip bonding
Operation speed	Higher	Lower	Lower
Assembly cost	Lower	Lower	Higher
Wafer process cost	Higher	Intermediate	Lower
Challenge for integration	Harder	Harder	Easier
Available waveguide	SOI, bulk-Si	SiN, a-Si	SOI

since we believe that hybrid integration is the most practical choice both now and in the near future, we have taken the hybrid-integration route to photonic–electronic integration for inter-chip interconnects.

1.2.3 Light Source Integration

Generally, light sources for high-density inter-chip interconnects are classified, as shown in Fig. 1.4. First, when considering the light source arrangement in our inter-chip optical interconnects, we have to choose between off-chip or on-chip sources. Although off-chip light sources are the more flexible of the two, they require highly precise optical connectors and care regarding polarization dependence to deliver optical power from the off-chip light sources into the substrate via optical fibers. Because we believe that this is not practical for large-scale interconnects, we chose on-chip light sources, which require neither optical connecters nor special care regarding polarization dependence. Although on-chip light sources are often affected by heat generated by LSIs mounted near the light sources, we

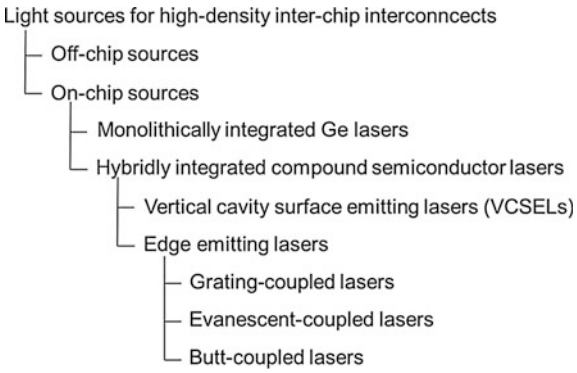


Fig. 1.4 Classification of light sources for high-density inter-chip interconnects

introduce a solution for this problem, as mentioned in Sect. 1.5. There are two types of integration for on-chip light sources: monolithic integration with germanium lasers and hybrid integration with compound semiconductor lasers. Because the efficiency and output power of monolithically integrated Ge-on-Si lasers are still low for inter-chip interconnect applications [13], we chose hybridly integrated lasers. There are two types of compound semiconductor lasers for optical interconnects: edge-emitting lasers and vertical cavity surface emitting lasers (VCSELs). Because VCSELs cannot maintain single-mode operation when the optical output is high, we chose edge-emitting lasers. There are also three types of edge-emitting lasers in terms of optical coupling structures between active OWs in the LDs and silicon OWs: grating-coupled lasers [14], evanescent-coupled lasers [15], and butt-coupled lasers [16]. The grating-coupled laser is a subassembly module, in which an LD, ball-lens, isolator, and 45° mirror are packaged in a hermetic silicon housing [14]. Although this method is highly reliable and tolerant of optical feedback, the module is much bigger than bare LD chips in the following methods. It is difficult to apply an arrayed LD chip for scale-out. The evanescent-coupled lasers have higher tolerance against alignment error when the compound semiconductor chips are mounted on the silicon substrate than the butt-coupled lasers do. However, we found that the bandwidth density and power consumption per channel in LDs can be improved using a branching configuration, in which the light from a single LD is divided and distributed to many channels [17], and we believe the efficiency and output optical power of the evanescent-coupled lasers are not high enough for the branching configuration. We therefore chose to use butt-coupled hybrid lasers for inter-chip interconnect applications and developed spot-size converters (SSCs) between LDs and silicon OWs to relax the alignment tolerance, as mentioned later.

1.2.4 Photonics–Electronics Convergence System with Silicon Optical Interposers

Based on the above examinations, we propose a photonics–electronics convergence system for inter-chip interconnects [12, 18]. A conceptual model of the system is shown in Fig. 1.5. This model is designed to provide optical interconnects among four LSI bare chips on a silicon substrate. The upper-left LSI chip on the silicon substrate has been removed to enable the substrate surface area that it covered to be seen. OMs and PDs are monolithically integrated on the silicon substrate under the LSI bare chips. Since high-speed I/O ports of an LSI are usually laid out near edges of the LSI die, OMs and PDs are laid out in the corresponding areas on the silicon substrate. The LSI bare chips are mounted on the substrate using flip-chip bonding and are electrically connected to the OMs and PDs. Arrayed LDs are hybridly integrated on the substrate. The LDs, OMs, and PDs are optically linked to each other by silicon OWs and OSs. We call the silicon substrate a "silicon optical interposer."

The inter-chip interconnects with the silicon optical interposers operate as follows. Arrayed LDs are driven simultaneously by direct currents (DCs). The CW light from each LD is divided by an OS and launched into an OM. OMs are directly driven by Tx circuits in one LSI. The modulated optical signals propagate along inter-chip OWs and are the input for PDs under another LSI. The electrical signals from those PDs are the input for Rx circuits in the LSI that the PDs are under.

This system enables us to replace conventional electronic wires on a PCB with the optical interconnects on a silicon substrate, which is about one hundredth the size of a PCB. Such silicon optical interposers have wide-bandwidth capabilities due to the properties of their optical signals. Since the silicon substrates can be fabricated using a CMOS-compatible process, they have quite high density and are low in cost. Furthermore, because this system is optically complete and closed without any optical inputs or outputs, users do not have to worry about optical issues, such as optical coupling, optical reflection, or polarization dependence. The hybridly integrated LDs are capable of high optical output power and a

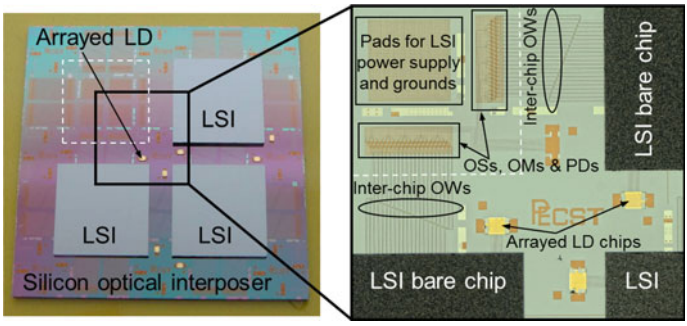


Fig. 1.5 Conceptual model of photonics–electronics convergence system

multichannel distribution. The hybrid integration between photonics and electronics allows us to individually choose the most suitable technology nodes for the photonics and electronics, respectively.

1.3 Configuration and Characteristics of Optical Components for Silicon Optical Interposers

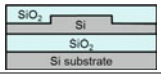
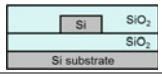
To confirm the feasibility of our photonics–electronics convergence system, we discuss high-density silicon optical interposers that mainly consist of silicon OWs, hybridly integrated on-chip light sources, silicon OMs, and germanium PDs. The configurations and characteristics of these optical components were investigated as follows.

1.3.1 Silicon Optical Waveguides

Generally, there are two types of silicon OWs in terms of their core cross-section shapes: rib-shaped and rectangular. Their cross sections and characteristics are compared in Table 1.2. The propagation loss of the rib-shaped OWs is lower than that of the rectangular ones, but the rib-shaped OWs pose difficulties in the fabrication process in that we have to stop etching the silicon layer to leave a precisely thin silicon slab. We believe this issue is critical in terms of yields in mass production, especially (as will be explained later) for yields of OMs. We therefore chose rectangular core OWs for our silicon optical interposers.

To reduce the relatively high propagation loss of the rectangular core OWs, we developed fine fabrication processes that mainly consist of a multiple exposure technique in variable-shaped-beam (VSB) electron beam (EB) lithography, and optimization of EB resist and etching processes. By applying these techniques, the field stitching error and line edge roughness (LER) are drastically reduced to 7.9 and 1.9 nm, respectively [19]. Figure 1.6 shows the core width dependence of the propagation loss for the TE-like mode at 1550-nm wavelength. The core height is 220 nm. The propagation losses are nearly constant and less than 2 dB/cm

Table 1.2 Comparison of silicon optical waveguides

Core type	Rib-shaped	Rectangular
Core cross section		
Propagation loss	Lower	Higher
Etching process	More difficult	Easier
Spot-size converter	More difficult	Easier

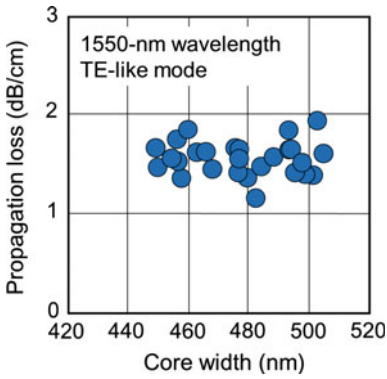


Fig. 1.6 Core width dependence of propagation loss

regardless of their core width. Such small core width dependence implies that the scattering loss caused by the side-wall roughness is negligible in our rectangular core OWs. The losses are comparable to those of rib-shaped OWs.

1.3.2 Hybridly Integrated On-Chip Light Sources

1.3.2.1 Arrayed Laser Diodes

Figure 1.7a shows a microscope image of a 13-channel arrayed LD chip (bottom side) to be mounted on the silicon optical interposers. It is an InGaAsP quantum-well LD array emitting 1530-nm wavelength light. Each channel is a Fabry–Perot-type LD with a spot-size converter [16]. The cavity length is 400 μm. The arrayed LD chip has a single common pair of electrodes for all 13 channels that simultaneously emit light by a single input current. This common electrode structure enables a narrow channel pitch of 30 μm. The chip also has a pair of alignment marks used for a passive alignment technique [20]. The near field pattern and output intensity of the 13-channel arrayed LDs are shown in Fig. 1.7b. The output power uniformity across all channels is better than 0.7 dB.

The measured wall-plug efficiency (WPE) of the LDs at room temperature is shown in Fig. 1.8. When the LD output is low enough, power consumption under a lasing threshold is dominant, and the efficiency is low. On the other hand, when the LD output is high enough, the output is saturated by heat and the efficiency decreases. As a result, the highest WPE of 35 % is obtained around 14 dBm of output power per channel. Therefore, we set the LD output power around 14 dBm to maximize the WPE in the data link experiments mentioned in Sect. 1.4.

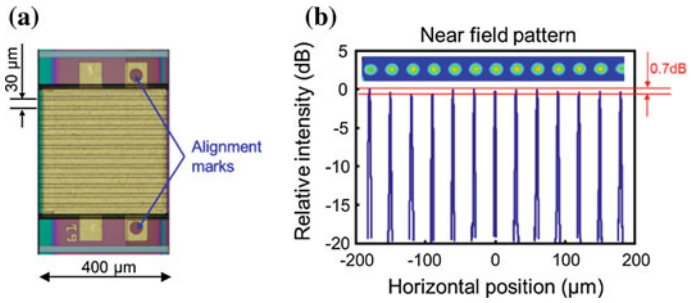


Fig. 1.7 13-channel arrayed laser diodes. **a** Microscope image of bottom side. **b** Near field pattern and output intensity

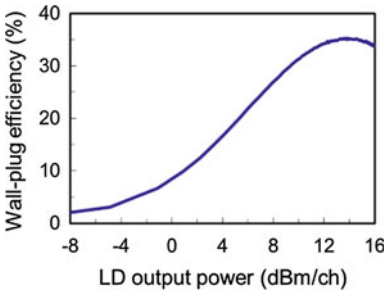


Fig. 1.8 Measured wall-plug efficiency of laser diodes at room temperature

1.3.2.2 Spot-Size Converters

Spot-size converters between the LDs and silicon OWs are key components for the silicon optical interposers in terms of their optical power budget and fabrication process simplicity. We previously used three types of SSCs: tapered silicon OW, inversed taper silicon OW, and SiON OW. Although the first two did not require additional processes, the first had a large coupling loss [18] and the second had a very small process margin, as will be discussed later. The third type had a low coupling loss but required additional processes [16]. We subsequently introduced a novel SSC called a trident [21], the schematic structure and scanning electron microscope (SEM) images of which are shown in Fig. 1.9. It consists of only three narrow silicon OWs fabricated without additional processes.

The measured coupling losses of the trident SSCs and a conventional inversed taper SSCs with various tip widths are shown in Fig. 1.10a. The coupling loss of the trident SSCs is low and insensitive to its tip width, unlike the inversed taper SSCs. This is because the spot size of the trident SSCs does not mainly depend on its tip width but mainly on its tip pitch. The line pitch is usually less sensitive to fabrication errors than the line width. Therefore, the trident SSCs are tolerant of fabrication errors. The measured coupling losses between the LDs and trident SSCs with various alignment deviations in the horizontal and vertical directions are plotted in

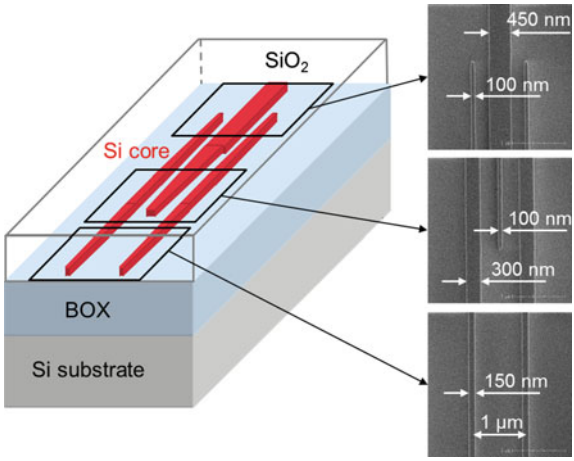


Fig. 1.9 Schematic structure and scanning electron microscope images of trident spot-size converters

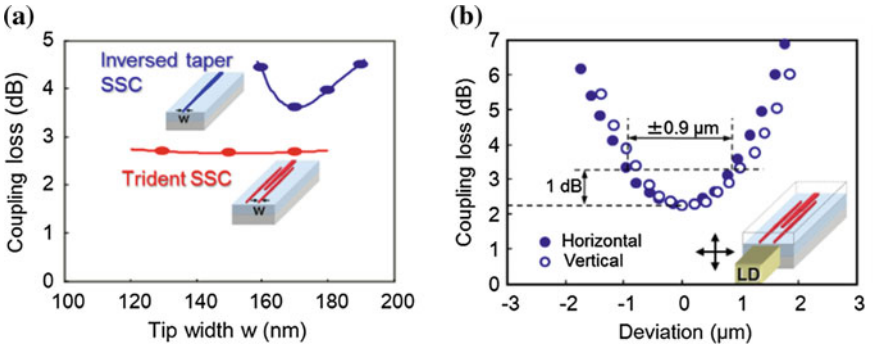


Fig. 1.10 Measured characteristics of trident spot-size converters (SSCs). **a** Coupling losses of trident SSCs and conventional inversed taper SSCs with various tip widths. **b** Alignment tolerance between laser diodes and trident SSCs in horizontal and vertical directions

Fig. 1.10b. The minimum coupling loss is as low as 2.3 dB, and the alignment error tolerance up to a 1-dB loss increase is about ±0.9 μm in both directions, which is large enough for our alignment precision (±0.5 μm) with a passive alignment technique [20].

1.3.2.3 Flip-Chip Bonding of Arrayed LD Chip

To form a hybridly integrated on-chip light source, an arrayed LD chip is flip-chip bonded to a silicon substrate with a passive alignment technique, as schematically shown in Fig. 1.11. The LD chip is vertically aligned just by mounting it on the

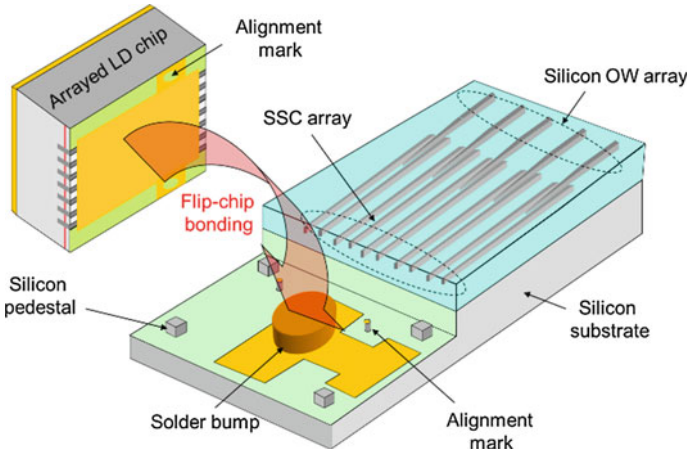


Fig. 1.11 Flip-chip bonding of arrayed laser diode chip to silicon substrate with passive alignment technique

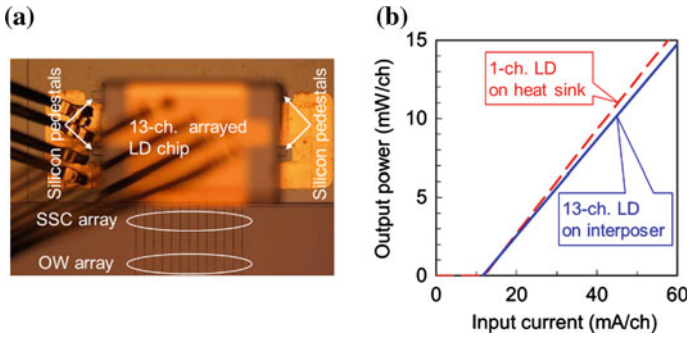


Fig. 1.12 Thirteen-channel arrayed laser diodes (LDs) mounted on silicon optical interposers. **a** Microscope image of *top*. **b** Measured per-channel *I–L* characteristics of 13-channel arrayed LD mounted on interposer and one-channel LD mounted on heat sink. Both were measured without temperature control

silicon pedestals, and it is horizontally aligned by overlapping the alignment marks on the bottom of the LD chip and the silicon substrate. Then the LD chip is fixed and electrically and thermally contacted to the substrate with the AuSn solder bumps. This structure enables low thermal resistance between the LD chip and silicon substrate [22]. As a result, the LD array is butt-coupled to the silicon OW array via the SSC array.

Figure 1.12a shows a microscope image of a 13-channel arrayed LD flip-chip mounted on a silicon optical interposer. The measured per-channel *I–L* characteristics of the LDs without temperature control are plotted in Fig. 1.12b, where the solid line indicates the *I–L* characteristics of the 13-channel arrayed LD hybridly integrated on

the interposer and the broken line indicates those of a 1-channel LD mounted on a heat sink. Since all 13 channels are driven simultaneously, the actual current injected into the whole arrayed LD chip is 13 times the value in the horizontal axis. Although the heat generation in the 13-channel LD is 13 times as high as that in the 1-channel LD, both *I–L* characteristics have about the same threshold currents and slope efficiencies, and there are no output power saturations up to 15 mW or higher per channel. This suggests that the hybridly integrated arrayed LD exhibits no degradation due to its high-density array and quite a high heat dissipation capability. We consider these high output power and high heat dissipation capabilities to indicate the superiority of our butt-coupled hybrid lasers over evanescent-coupled ones [22].

1.3.3 Silicon Optical Modulators

There has been extensive research on silicon OMs using the carrier plasma effect in PIN or p–n diodes, most of them focused on using a doped silicon slab in the rib-shaped OWs to make electric contact between the OW core and metal electrodes [23–25]. In these cases, the gaps between P- and N-doping areas should be wider than the width of the optical mode profiles to prevent optical absorption loss due to the highly doped carriers. The optical mode profiles in these rib-shaped OWs extend to the slab areas, and a thicker slab causes a wider mode profile and P-N gap. The wider P-N gaps increase resistivity and decrease modulation efficiency and modulation speed. Because OM characteristics such as optical loss, modulation efficiency, and speed are sensitive to the slab thickness in this way, we have to stop etching the silicon layer to leave a precisely thin silicon slab. To overcome these design and fabrication difficulties, we propose a novel structure for the electric contact between the OW core and electrodes to be used instead of the silicon slab. Figure 1.13a shows a schematic of the structure of our proposed OM [26], which is a Mach–Zehnder interferometer (MZI) composed of phase shifters and multimode

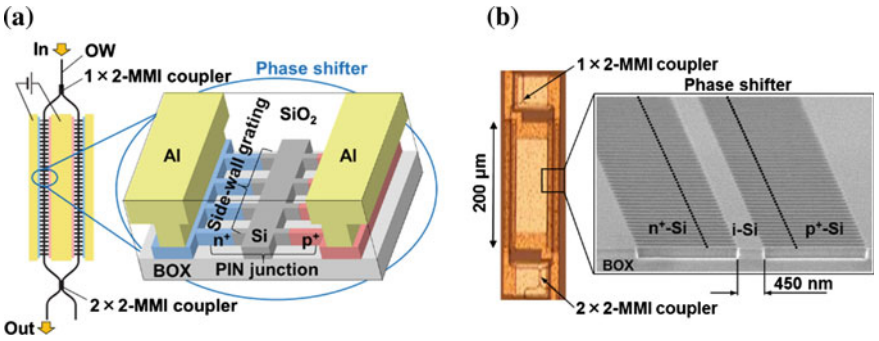


Fig. 1.13 Silicon optical modulators (OMs) with side-wall gratings. **a** Schematic structure. **b** Microscope and scanning electron microscope images of fabricated OMs

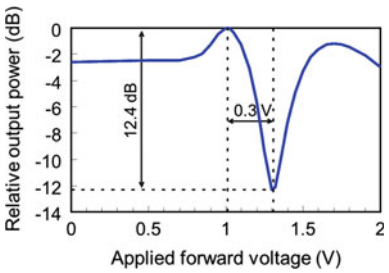


Fig. 1.14 Measured direct current response of optical modulators

interference (MMI) couplers. The phase shifters, which have side-wall gratings on both sides of the OW core to enable electric contact between the core and metal electrodes, can change their refractive indices by the carrier plasma effect in lateral PIN diode structures. Figure 1.13b shows microscope and SEM images of the fabricated OM. Because the OWs and side-wall gratings have a uniform thickness of silicon over the entire OM, the etching process to form the OWs and side-wall gratings is much easier than that to form rib-shaped OWs. Moreover, this structure enables stronger lateral optical mode confinement, narrower optical mode profile, narrower P-N gap, lower resistivity, higher efficiency, and higher speed than the OMs with rib-shaped OWs. The pitch of the side-wall gratings is 285 nm, which is designed so that their stop-band wavelength is much shorter than the operation wavelength to prevent diffraction by the gratings. The interaction length of the phase shifter (L) is 200 μm.

The measured DC response of our OM is plotted in Fig. 1.14. The π-phase shift voltage ($V\pi$) is 0.3 V and the modulation efficiency ($V\pi \cdot L$) is 0.006 Vcm, which is twice as high as the efficiency of our previous OM with rib-shaped OWs [18]. The extinction ratio is 12.4 dB. Since the frequency response of the OM is similar to that of a series resistor–capacitor (RC) circuit, we used pre-emphasis to compensate for the frequency response. The 3-dB bandwidth with pre-emphasis is estimated to be 12.5 GHz [26].

1.3.4 Germanium Photodetectors

There are generally two types of germanium PDs that we can monolithically integrate on a silicon substrate: PIN-PDs and metal-semiconductor-metal (MSM) PDs [27]. The MSM-PDs require fewer fabrication steps but finer patterning and alignment than PIN-PDs. For this work we chose PIN-PDs for the silicon optical interposers. Figure 1.15a shows a schematic cross section of our germanium PIN-PDs and Fig. 1.15b shows an SEM image. The measured frequency responses of the PDs with 0-, 1-, and 2-V biases are plotted in Fig. 1.16. The 3-dB cutoff frequencies are 10 GHz with a 0-V bias voltage and 26 GHz with a 1-V bias voltage. The dark current is about 1 μA with a 1-V bias voltage.

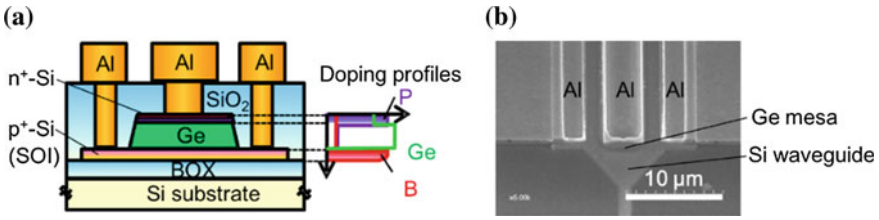


Fig. 1.15 PIN-type germanium photodetectors. **a** Schematic cross section. **b** Scanning electron microscope image

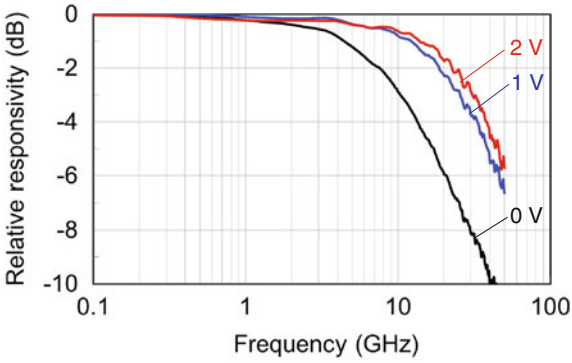


Fig. 1.16 Frequency responses of PIN-type germanium photodetectors

1.4 Silicon Optical Interposers for High Bandwidth Density

1.4.1 Design Consideration for Bandwidth Density and Optical Power Budget

As mentioned earlier, LSI bare chips are supposed to be mounted on the interposers using flip-chip bonding. The ITRS projections have indicated that the pitches of flip-chip pad arrays should stop shrinking at around 100 μm [7]. Therefore, we designed our silicon optical interposers so that the pad pitches of the OMs and PDs were 100 μm.

We found that the LD power consumption per channel can be improved by using a branching configuration, in which the light from a single laser is divided and distributed to many channels, because the power consumption under lasing threshold is shared by many channels [17]. Since the wall-plug efficiency of the LD is at a maximum around 14-dBm LD output, as shown in Fig. 1.8, we designed optical links of our silicon optical interposers by using the branching configuration so that the LD output was about 14 dBm for maximum energy efficiency. Since we expected that we had a margin of about 6 dB in the optical link power budget, we introduced 1 × 4 MMI couplers as OSs for the branching configuration.

1.4.2 Integrated Fabrication Process

The fabrication processes of our silicon optical interposers are listed in Fig. 1.17. The silicon optical interposers were fabricated from 4-inch silicon-on-insulator (SOI) wafers in the Super Clean Room at AIST Tsukuba West by CMOS process technology. The thicknesses of the buried oxide layer and the SOI layer were 3 μm and 220 nm, respectively. The silicon OW cores, as well as trident SSCs, 1 × 4 MMI couplers, MZIs, and side-wall gratings for the OMs were formed by VSB-EB lithography and dry etching. Lateral PIN junctions for the OMs and vertical ones for the PDs were formed by B and P ion implantations. Epitaxial germanium mesas for the PDs were selectively grown on the silicon cores by chemical vapor deposition (CVD). All the components were covered with a SiO_2 upper cladding layer by CVD. Contact holes and metal electrodes were formed by dry etching. The OW end-faces, silicon pedestals, and alignment marks for LD mounting were formed by dry etching. Electrodes and solder bumps for LDs were formed on the bottom. Finally, the arrayed LD chips were mounted on the pedestals using a passive alignment technique [20].

Microscope images of one of our fabricated silicon optical interposers are shown in Fig. 1.18 [28]. The substrate is 4.7 × 4.5 mm. Two 13-channel arrayed LD chips are hybridly integrated on the silicon substrate, and 26 trident SSCs, 26 1 × 4 OSs, 104 OMs, 104 inter-chip Ows, and 104 PDs are monolithically integrated on the substrate. Unit cells of the OMs and PDs are 400 × 100 μm and 200 × 100 μm, respectively. They are tiled so that their pad pitches are 100 μm. Two LSI bare chips are supposed to be mounted on the right and left sides of the substrate using flip-chip bonding to be optically connected to each other.

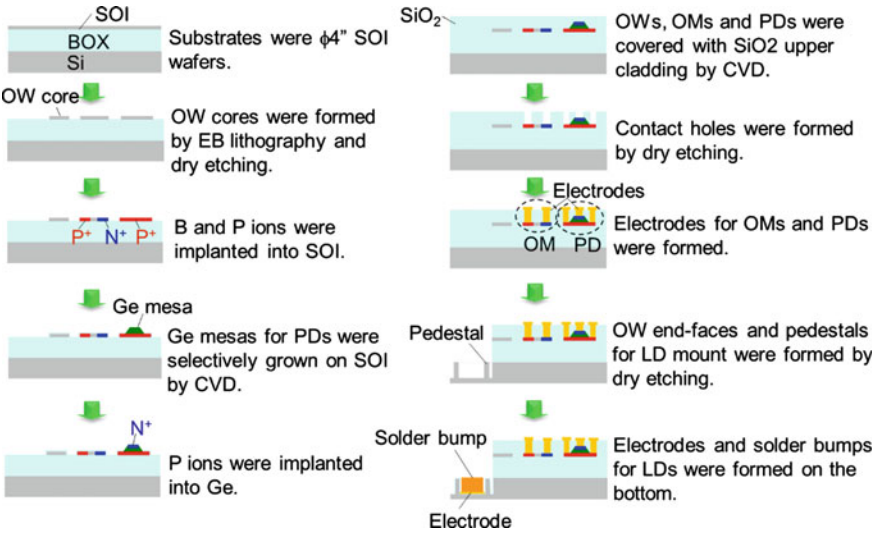


Fig. 1.17 Fabrication process of silicon optical interposers

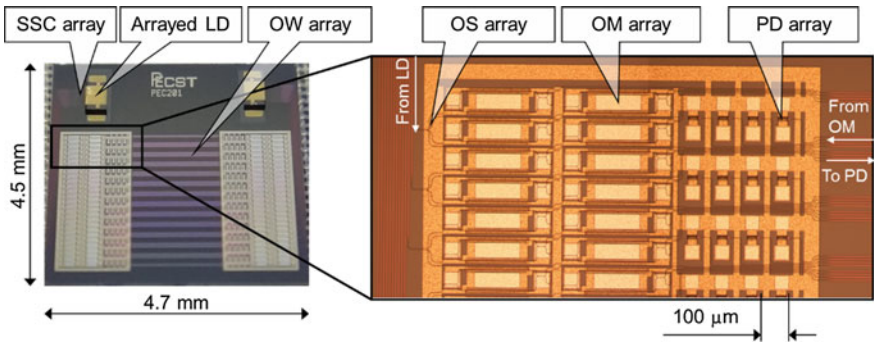


Fig. 1.18 Microscope images of fabricated silicon optical interposers

1.4.3 Data Link Experiments

We conducted data link experiments as follows. All 13 channels of an arrayed LD were simultaneously driven by a single DC current. The CW light from the LD was a wavelength of 1530 nm and a TE-like mode. It was coupled to a silicon OW by a trident SSC and then divided into four by a 1 × 4 OS and each of them was launched into a OM. The radio frequency (RF) input signals were pre-emphasized by a differentiator composed of passive RC circuits and drove the OM. The voltage amplitude after pre-emphasis was 3.5 V peak to peak. The modulated optical signals propagated along an inter-chip OW and were then input to a PD and converted into electrical signals.

The measured eye diagram of the PD output at 20-Gbps NRZ with a 2^7-1 pseudo-random binary sequence (PRBS) is shown in Fig. 1.19a. The clear eye opening indicates that the optical links are capable of a 20-Gbps data link. The measured bit error rates (BERs) for the 20-Gbps PRBS are plotted in Fig. 1.19b. We confirmed that the BER was less than 10^{-12} when the received power of the PD was larger than −5 dBm. An error-free data link at 20 Gbps via the 1 × 4 OS was achieved. These results demonstrate that the silicon optical interposers are capable of a 2.1-Tbps bandwidth for inter-chip optical interconnects.

To evaluate inter-channel crosstalk, we also demonstrated four-channel simultaneous operation. Because we did not have the equipment for 4 × 20 Gbps simultaneous operation, we did it with 4 × 12.5 Gbps. Figure 1.20a shows BERs of four individual channels when the four channels simultaneously operated. We confirmed four-channel simultaneous error-free operation. Figure 1.20b shows the BERs of a particular channel with (circles and solid line) and without (triangles and broken line) simultaneous operations of the other three channels. Because the BER difference is very small, we believe the power penalty due to the inter-channel crosstalk was negligible in these data link experiments.

The per-channel optical power budget of the data link experiments when the error-free data links were achieved is summarized in Table 1.3. The optical output

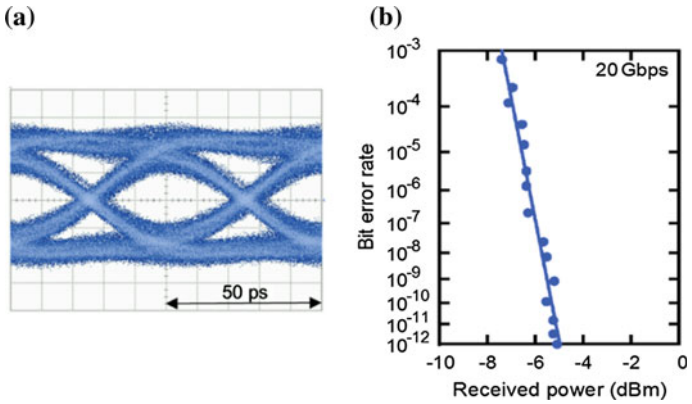


Fig. 1.19 Photodetector outputs of data link experiments at 20 Gbps. **a** Eye diagram. **b** Bit error rates

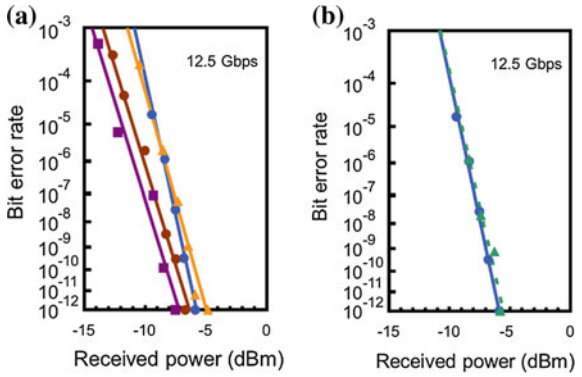


Fig. 1.20 Bit error rates (BERs) in four-channel simultaneous operation. **a** BERs of 4 individual channels when the 4 channels operated simultaneously. **b** BERs of a particular channel with (*circles* and *solid line*) and without (*triangles* and *broken line*) simultaneous operations of the other 3 channels

Table 1.3 Per-channel optical power budget of data link experiments

Item	Power (dBm)	Loss (dB)
LD output power	13.0	–
LD to OW coupling loss	–	2.3
Inherent 1 × 4 branching loss	–	6.0
1 × 4 OS excess loss	–	0.5
Inherent modulation loss	–	3.0
OM excess loss	–	2.8
OW propagation loss	–	2.2
Other losses	–	1.2
PD input power	−5.0	–

Table 1.4 Footprints of optical components per channel

Optical component	Footprint (mm^2)
Laser diode (LD)	0.0077
Optical modulator (OM)	0.0400
Photodetector (PD)	0.0200
Total	0.0677

power from the LD was 13 dBm, where the WPE of the LD was a maximum, as mentioned in the previous section, and the optical input power to the PD was −5 dBm. Therefore, the overall optical loss was 18 dB, including an inherent 6-dB branching loss and a 3-dB modulation loss.

1.4.4 Significance of Bandwidth Density

The footprints of the optical components per link channel are listed in Table 1.4. The total footprint was 0.0677 mm^2 per channel, meaning we could achieve a high bandwidth density of 30 Tbps/cm^2 with a channel line rate of 20 Gbps. Since LSI bare chips are supposed to be mounted on the silicon optical interposers by flip-chip bonding, as shown in Fig. 1.5, and the footprints of the optical components and Tx and Rx electrical circuits overlap, we believe the overall bandwidth density with the electrical circuits is similar to that of optical components. To our knowledge, this was the highest bandwidth density for an inter-chip optical interconnect. Since the maximum lithography field size (stepper shot size) in area and signal I/O pad percentage out of total pads for CPUs have currently been 8.58 cm^2 and 33 % respectively and will be so in the future [7], we can obtain an overall inter-chip bandwidth at the level of several tens of Tbps by using silicon optical interposers, which is sufficient for the required bandwidth in the late 2010s or early 2020s.

The footprints of the OMs and PDs mainly depend on their pad pitches, which were 100 μm in this case. Therefore, we believe that it is possible to reduce their footprints with smaller pad pitches, by one-fourth with a 50-μm pitch for example.

Since this system is optically complete and closed and no temperature sensitive components are used, we did not need to align the fibers, control the polarization, or control the temperature throughout the experiments.

1.5 Silicon Optical Interposers for Wide Temperature Range Operation

In the previous section, we discussed silicon optical interposers fully integrated with the optical components on a silicon substrate, achieving a high bandwidth density of 30 Tbps/cm^2 at room temperature. For practical applications, interposers

should be usable under high temperature conditions and rapid temperature changes without complex feedback controls, namely athermal, so that they can cope with heat generated by the mounted LSIs. Since the LSI bare chips are mounted near LDs, as shown in Fig. 1.5, the LDs are expected to be affected by the heat. Because the output power of conventional LDs usually declines as temperature rises, the system requires temperature-insensitive LDs.

Quantum dot LDs (QD-LDs) are expected to be used under these thermally severe conditions because of their output power characteristics with low temperature sensitivity [21, 29–32]. Although QD-LDs monolithically integrated on silicon substrates by heteroepitaxy or wafer bonding have been reported, their characteristics and reliability have not been enough for applications due to the large lattice mismatch and thermal expansion coefficient difference with the silicon substrate [30–32]. We previously reported that QD-LDs hybridly integrated on silicon substrates were suitable for high-density and heat-tolerant optical interconnect applications [21]. Even if we use QD-LDs as on-chip light sources, lasing wavelength shifts due to temperature variation are unavoidable. Therefore, the other optical components integrated with QD-LDs should be not only temperature insensitive but also wavelength insensitive over the whole wavelength range where the lasing wavelength shifts upon changes in temperature.

In this section, we describe our athermal silicon optical interposers hybridly integrated with QD-LDs and monolithically integrated with other temperature- and wavelength-insensitive components on a silicon substrate. We discuss the error-free data link performance with the interposers over a wide temperature range without adjusting their biases or signals.

1.5.1 Hybridly Integrated Athermal Light Sources and Their Thermal Characteristics

Our 13-channel arrayed LD chips for the athermal silicon optical interposers were fabricated by QD Laser, Inc. Figure 1.21a shows a microscope image of a 13-channel arrayed QD-LD chip (bottom side) to be mounted on athermal silicon optical interposers. Each channel is a Fabry–Perot-type LD emitting around 1310-nm wavelength light [21]. The cavity length is 600 μm. The arrayed QD-LD chip has a single common pair of electrodes, the same as the arrayed QW-LD mentioned in Sect. 3.2.1. The channel pitch is also 30 μm. The chip also has a pair of alignment marks used for a passive alignment technique [20]. The measured per-channel current-light output power (*I*–*L*) characteristics of the QD-LDs on a heat sink at various temperatures are shown in Fig. 1.21b [38]. The QD-LDs can maintain their output power higher than 10 mW per channel up to 100 °C. The measured temperature dependence of the threshold current is shown in Fig. 1.22a. Temperature sensitivity of the threshold current is low, and the characteristic temperature is 114 K from 25 to 120 °C. The measured temperature dependence of

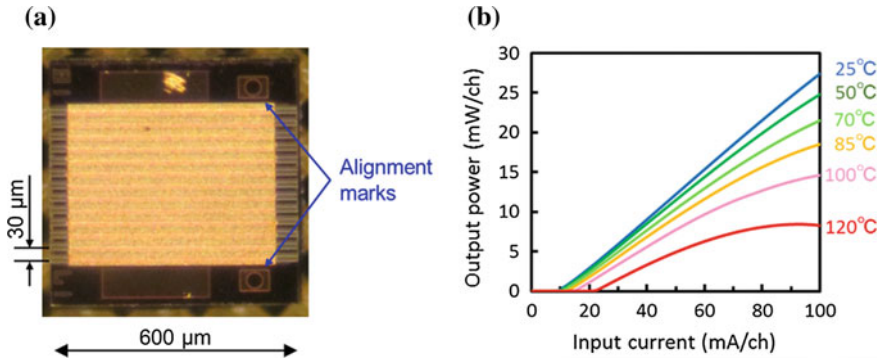


Fig. 1.21 Thirteen-channel arrayed quantum dot laser diodes (QD-LDs). **a** Microscope image of bottom side. **b** Measured per-channel current–light output power (*I–L*) characteristics of QD-LD on a heat sink at various temperatures

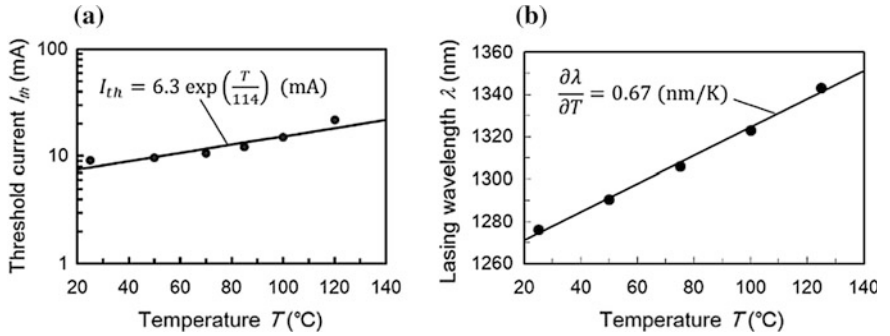


Fig. 1.22 Measured temperature dependence of quantum dot laser diode characteristics. **a** Threshold current. **b** Lasing wavelength

the lasing wavelength is shown in Fig. 1.22b. The lasing wavelengths are 1276 nm at 25 °C and 1343 nm at 125 °C, meaning the temperature coefficient of the lasing wavelength is about 0.67 nm/K. Therefore, the other optical components integrated with the QD-LDs should be not only temperature insensitive but also wavelength insensitive around the above wavelength range.

The arrayed QD-LD chips are hybridly integrated on a silicon OW platform. The silicon OWs have rectangular cross-section cores that are 200-nm thick and 348-nm wide for bent OWs and 3-μm wide for straight ones. The narrower waveguides are designed for single mode ones around a 1.3-μm wavelength. The propagation losses at a wavelength of 1310 nm are about 3 dB/cm with 348-nm wide and 0.5 dB/cm with 3-μm wide cores. The propagation losses of the OWs have little sensitivity to both temperature and wavelength over the ranges concerned (25–125 °C and 1270–1350 nm). The measured temperature dependence of the coupling loss between the mounted QD-LDs and silicon OWs from 25 to 125 °C are plotted in Fig. 1.23. The

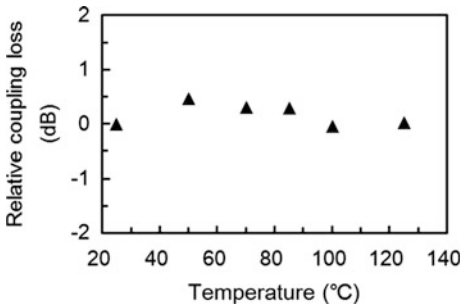


Fig. 1.23 Measured temperature dependence of the coupling loss between mounted quantum dot laser diodes and silicon optical waveguides at various temperatures

coupling loss is nearly constant across the entire temperature range. These results suggest that misalignment between the LDs and OWs due to temperature change is negligible across the entire temperature range. Since the optical system is complete and closed within the interposer substrate, it does not require external fiber alignment or polarization control. Therefore, we believe that the system is robust against both thermal and mechanical fluctuations.

1.5.2 Optical Modulators and Their Thermal Characteristics

As mentioned previously, the OMs integrated with the QD-LDs should be not only temperature insensitive but also wavelength insensitive over the whole wavelength range where the lasing wavelength shifts upon changes in temperature. Ring- or disk-resonator-based OMs are compact, but they are inherently sensitive to both temperature and wavelength [32–36]. Although some athermal or thermally stabilized resonator-based OMs have been reported, they were still sensitive to wavelength, and they usually required monitoring and feedback circuits for wavelength locking [33–36]. We believe that these additional circuits can be obstacles to developing large-scale integrated interconnect systems in terms of their footprint, power consumption, and cost. Therefore, we chose symmetric MZI-based OMs, which are inherently insensitive to both temperature and wavelength and do not require the additional circuits [37].

The structure of silicon OMs for athermal silicon optical interposers is similar to that shown in Fig. 1.13. It is a symmetric MZI. The side-wall grating is designed so that the stop-band wavelength is sufficiently shorter than the operating wavelength, and the transmission spectrum is flat around the operating wavelength. In fact, the measured wavelength dependence of passive insertion loss of the OMs without DC bias or RF signal is shown in Fig. 1.24. The wavelength dependence is less than 1 dB across the wavelength range concerned. Therefore, the OMs are wavelength

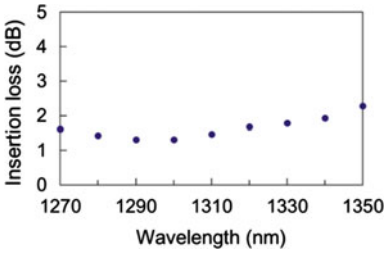


Fig. 1.24 Measured wavelength dependence of the passive insertion loss of optical modulators without DC bias or RF signal

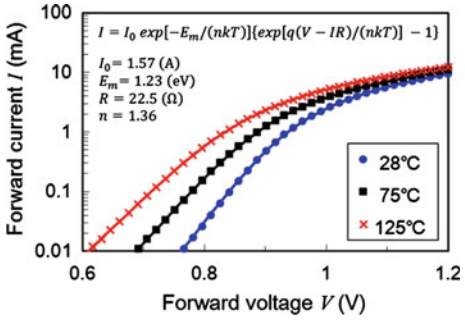


Fig. 1.25 Measured current–voltage (*I–V*) characteristics of optical modulators versus the forward bias voltage at operating temperature of 28, 75, and 125 ºC

insensitive. One MMI coupler connected to the input port is 1 × 2, and another connected to the output ports is 2 × 2 so that we can use differential outputs from both cross and bar ports. This configuration also allows us to apply the same bias voltages or currents to both arms of the MZI to satisfy a quadrature condition. This symmetric bias can cancel the OM output deviation due to the bias shifts in both arms due to temperature change.

The measured current–voltage (*I–V*) characteristics of the OMs with forward bias voltage at 28, 75, and 125 °C are plotted in Fig. 1.25 [38]. The measured *I–V* characteristics can be well expressed by the following equations:

$$I = I_0 \exp\left(-\frac{E_m}{nkT}\right)\left\{\exp\left[\frac{q(V-RI)}{nkT}\right]-1\right\},\ I_0 = 1.57\,\mathrm{A},\ E_m = 1.23\,\mathrm{eV},\ R = 22.5\,\Omega,\ n = 1.36, \tag{1.1}$$

where q is the electron charge, k is the Boltzmann's constant, and T is temperature. The solid lines in Fig. 1.25 were calculated using (1.1). Here n is the diode ideality factor, E_m corresponds to the band gap energy, and R corresponds to the series

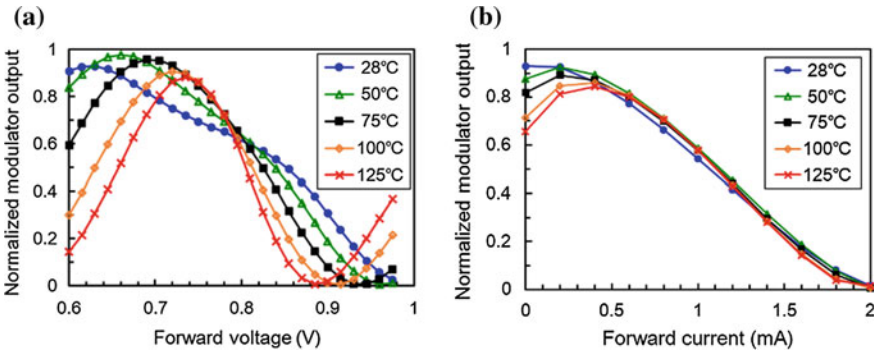


Fig. 1.26 Measured DC responses of optical modulators at various temperatures as functions of **a** forward bias voltage and **b** forward bias current

resistance. These parameters are useful for SPICE simulations. The diode current I under a constant bias voltage V around 0.8 V exponentially increased as the temperature rose.

The measured DC responses of the OMs at various temperatures as functions of forward bias voltage and forward bias current are shown in Fig. 1.26a, b, respectively [38]. On the horizontal axes in both figures, the biases were applied to both arms in an MZI on a push-pull basis so that the sum of voltages always equaled 1.575 V in (a) and the sum of currents always equaled 2.0 mA in (b). The vertical axes are normalized by the sum of the output power on both the cross and bar ports without applying bias at each temperature. In both figures, the quadrature conditions exhibit small temperature sensitivities due to the same biases being applied to both arms. However, the modulation efficiency as a function of voltage exhibits larger temperature sensitivity than that of the current. As a result, the DC responses as functions of the bias current are quite insensitive to temperature, unlike those obtained as functions of the bias voltage. Therefore, we used a constant bias-current condition for the following data link experiments.

1.5.3 Photodetectors and Their Thermal Characteristics

The structure of PDs for the athermal silicon optical interposers is similar to that shown in Fig. 1.15. The measured photo and dark currents of the PDs at various temperatures with 1-V reverse bias voltage are plotted in Fig. 1.27 [38]. The photo current is insensitive to temperature, meaning the responsivity of the PDs also exhibits little sensitivity to temperature. The dark current I_d, namely the leakage current in the PIN diode with reverse bias, can be well expressed by the following equation:

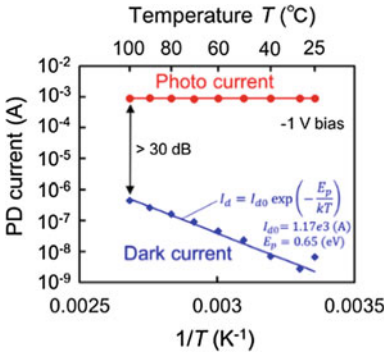


Fig. 1.27 Measured photo and dark currents of photodetectors with 1-V reverse bias voltage at various temperatures

$$I_d = I_{d0} \exp\left(-\frac{E_p}{kT}\right), \text{ with } I_{d0} = 1.17 \times 10^3 \text{ A, and } E_p = 0.65 \text{ eV}. \quad (1.2)$$

The E_p corresponding to the band gap energy is in good agreement with that of germanium (0.69 eV). Although the dark current increases exponentially with temperature rise, the photo-to-dark current ratio is higher than 30 dB up to 100 ºC.

1.5.4 Data Link Experiments Over Wide Temperature Range

We carried out data link experiments with the athermal silicon optical interposers over a wide temperature range. A silicon optical interposer was put on a probe station under temperature control. The DC and RF driving conditions for LDs, OMs, and PDs were similar to those mentioned in the previous section. The measured BERs at 20 Gbps at various temperatures as functions of LD input current and PD received power are shown in Fig. 1.28a, b, respectively [38]. For these measurements, we intentionally changed the LD current to change the BER at each temperature but did not adjust the bias current of the OMs, bias voltage of the PDs, or RF input signals to the OMs throughout the entire temperature range from 25 to 125 ºC. The penalty of the LD current above 100 ºC was mainly caused by the decline in LD output. The penalty of the PD received power at 125 ºC mainly caused by thermal noise is about 1 dB. We confirmed that the BER is less than 10^{-12} even at 125 ºC when the PD received power is higher than −7.4 dBm. We achieved error-free data links at 20 Gbps without adjusting the OMs or PDs across the entire temperature range.

We also observed an eye diagram under fixed bias and signal conditions for the LDs, OMs, and PDs while the temperature was continuously changed from 25 to 125 ºC. The average temperature-raising rate was about 0.8 ºC/s. The eye diagram snapshots at some temperatures are summarized in Fig. 1.29. The magnification

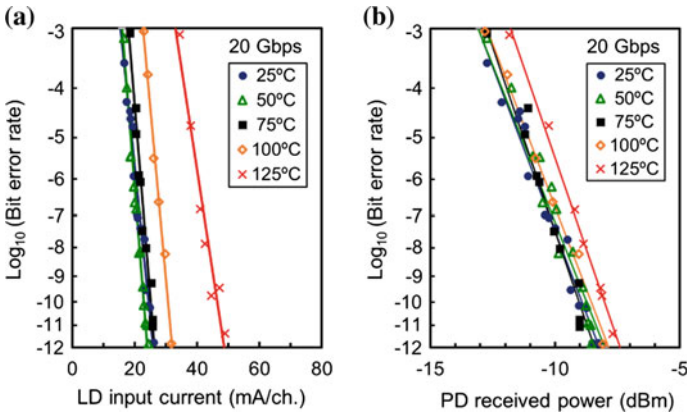


Fig. 1.28 Measured bit error rates at 20 Gbps at various temperatures as functions of **a** laser diode input current and **b** photodetector received power

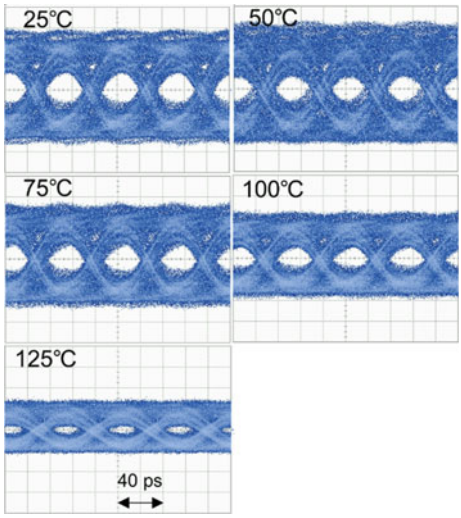


Fig. 1.29 Eye diagram snapshots at 20 Gbps under fixed bias and signal conditions for laser diodes, optical modulators, and photodetectors while the temperature was continuously changed from 25 to 125 °C

ranges on the vertical axes are common among of them. Although the eye amplitude decreases due to the decline in LD output as temperature rises above 100 °C, we confirmed that the eye keeps opening across the entire temperature range without adjusting the device biases or signals. These experimental results suggest that the silicon optical interposers do not require additional monitoring or feedback circuits to stabilize temperature and/or wavelength across the wide temperature range from 25 to 125 °C or under a rapid temperature change of 0.8 °C/s.

We believe that the significance of the athermal operation up to 125 °C is as follows. Since the maximum junction temperatures in most LSIs have currently been below 125 °C and will be so in the future [7], our silicon optical interposers are

tolerant against the heat generated by the mounted LSIs. Furthermore, since an extended industrial temperature range, which is the widest one for ordinary electronic devices, is usually defined as −40 to 125 ºC, the interposers are usable for a wide range of applications without complex monitoring or feedback controls.

1.6 25-Gbps Data Links Using Silicon Optical Interposers and FPGA Transceivers

To verify the feasibility of the silicon optical interposers with more practical configurations, we also demonstrated 25-Gbps optical data links on silicon optical interposers mounted on a PCB with a transimpedance amplifier (TIA) and a field-programmable gate array (FPGA) [39].

The setup for the data link experiments is shown in Fig. 1.30. A silicon optical interposer and a TIA are mounted close together on a PCB, and are linked by wire bonding. Bonding pads and coaxial connectors on the PCB are linked via differential microstrip lines. An FPGA (Altera Stratix V GT) is mounted on another PCB, and both PCBs are linked by coaxial cables. While the layout of the silicon optical interposers discussed in Sect. 1.4 is designed for flip-chip bonded LSIs, the layout in this section is designed for wire bonding. Therefore, the OMs and PDs are placed near both edges of the interposers to shorten the bonding-wire length. Each channel supports differential signals to suppress common mode noises mainly radiating from the bonding wires in the OM side and received by the bonding wire in the PD side. Namely, an OM driven by a pair of electrical differential signals modulated CW light from an LD and output a pair of optical differential signals to a pair of OWs. A pair of PDs converted a pair of optical differential signals into a pair of electrical differential signals, then output them to a differential TIA. The differential system can also compensate modulation loss by the OMs up to 3 dB. The FPGA has four-channel 25-Gbps transceivers equipped with PRBS signal generators and

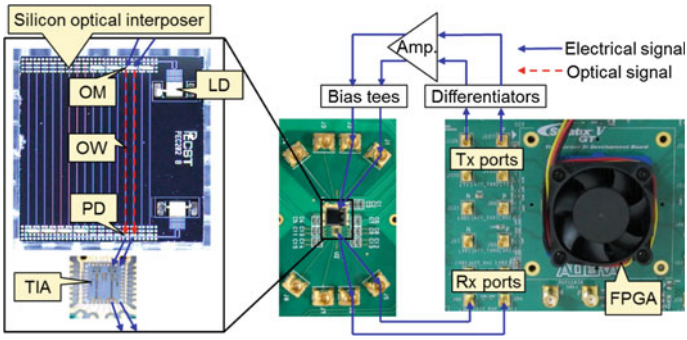


Fig. 1.30 Setup for data link experiments with silicon optical interposers, transimpedance amplifiers, and field-programmable gate arrays on printed circuit boards

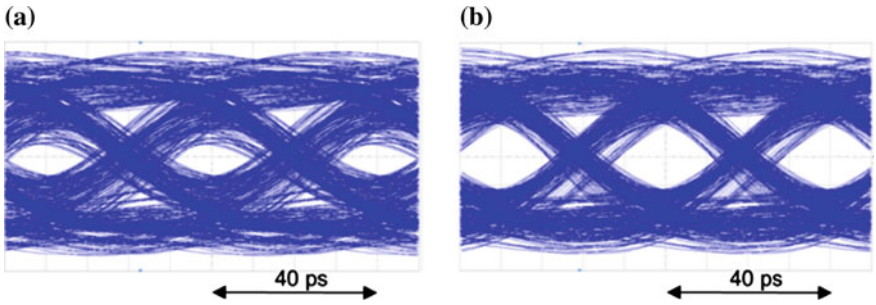


Fig. 1.31 Eye diagrams of transimpedance amplifier differential output at 25 Gbps **a** without and **b** with the pre-emphasis in field-programmable gate array transmitter

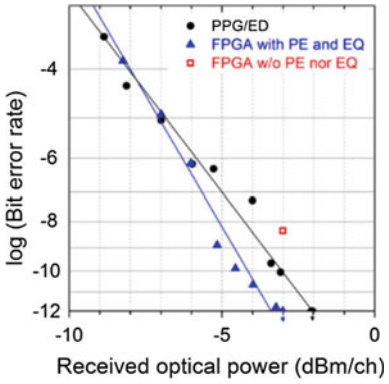


Fig. 1.32 Bit error rates at 25 Gbps without field-programmable gate array (FPGA), with FPGA without pre-emphasis (PE) or equalization (EQ), and with FPGA with PE and EQ

BER testers. The Tx has a pre-emphasis (PE) function using a three-tap finite impulse response (FIR) filter, and the Rx has an equalizer (EQ), such as a continuous time linear equalizer (CTLE).

We investigated three cases of data link experiments: (case 1) without FPGA, where the differentiators were connected to a pulse pattern generator (PPG) instead of the FPGA Tx and the TIA was connected to an error detector (ED) instead of the FPGA Rx; (case 2) with the FPGA without PE in the Tx nor EQ in the Rx; and (case 3) with the FPGA with PE and EQ. Figure 1.31 shows eye diagrams of the TIA differential output at 25 Gbps (a) without and (b) with PE in the FPGA Tx. The eye diagrams are degraded mainly due to the parasitic capacitance and inductance of the bonding wires, microstrip lines, and connectors on the PCBs. The eye diagram in Fig. 1.31b is improved by PE compared with that in Fig. 1.31a. The measured BERs in cases 1, 2, and 3 at 25 Gbps are plotted in Fig. 1.32. We confirmed error-free data links in cases 1 and 3. The receiver sensitivity is improved by about 1 dB by PE and EQ in the FPGA. The total footprint of the optical components is 0.0877 mm^2 per channel because the PD footprint is doubled for a differential receiver compared with that in Table 4.5. We achieved about 29 $Tbps/cm^2$ with a channel line rate of 25 Gbps.

1.7 Advanced Fabrication Process and Optical Components for Wider Bandwidth in Future

Because it generally takes a longer time and requires higher risk to design and fabricate fully integrated silicon optical interposers than to design and fabricate individual optical components, we used enough mature component designs and fabrication processes for the fully integrated silicon optical interposers mentioned in the previous sections. More advanced optical components and fabrication process, which are expected to be applied for optical interconnects that will have wider bandwidth in the future, have been also developed in the PECST project. Some are introduced in this section.

1.7.1 Hybridly Integrated 1200-Channel Light Source

We discussed a high bandwidth density of 30 Tbps/cm^2 with silicon optical interposers in Sect. 1.4. However, we not only need high bandwidth density but also wide bandwidth for practical optical interconnect applications. To achieve wide bandwidth, high channel-count light sources are required. Therefore, a hybridly integrated 1200-channel light sources were demonstrated [40]. Three 25-channel arrayed LD chips were mounted on a silicon OW platform by using flip-chip bonding with a passive alignment technique, as mentioned in Sect. 3.2.3, and each LD channel was split into 16 output ports by double cascade 1 × 4 OSs. Figure 1.33 shows the near-field pattern of outputs from the hybridly integrated 1200-channel light sources. The pitch of the output ports was 8 μm to include 1200 ports in 1 cm corresponding to a stepper shot size. The footprint of the light sources was 9700 × 1210 μm^2. The 1200-channel light source can provide 30-Tbps bandwidth with 25-Gbps OMs.

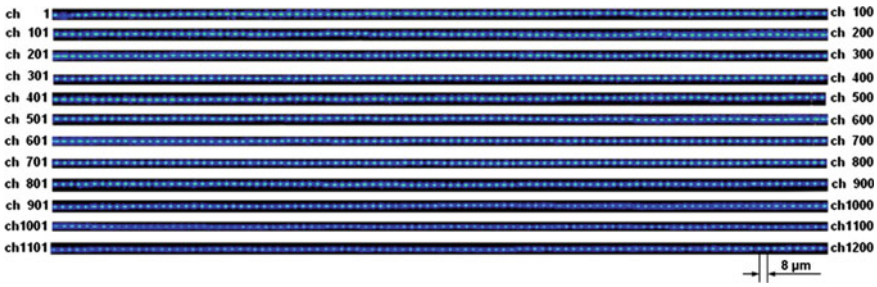


Fig. 1.33 Near-field pattern of outputs from hybridly integrated 1200-channel light sources

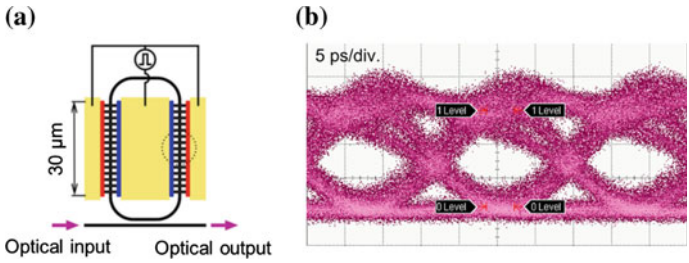


Fig. 1.34 Ring-resonator-based optical modulators (OMs) with side-wall gratings. **a** Schematic structure. **b** Eye diagram of OM output at 56 Gbps

1.7.2 High-Speed Ring-Resonator-Based Optical Modulators

Although symmetric MZI-based OMs are inherently insensitive to both temperature and wavelength, as shown in Sect. 1.5, they usually require longer interaction length or higher driving voltage than ring-resonator-based OMs. The relatively long interaction length or high driving voltage often limits their modulation speed. Therefore, ring-resonator-based OMs with side-wall gratings and PIN junctions for higher speed and smaller footprint, namely higher bandwidth density, were demonstrated [41]. Figure 1.34a shows a schematic structure of the ring-resonator-based OMs. The structure of the phase shifter was similar to that mentioned in Sect. 1.3.3. The phase shifter length was 60 μm. Figure 1.34b shows a clear eye opening by the OMs at a high bit rate of 56 Gbps.

1.7.3 High-Speed Germanium Photodetectors with Low Contact Resistance

The response speeds of conventional PIN-type germanium PDs were mainly limited by their contact resistance between metal electrodes and the germanium mesa. The reduction in the contact resistance with a silicon capping layer over the germanium mesa was investigated [27]. Figure 1.35 shows the 3-dB bandwidth and eye diagrams of the improved PDs. The structure was similar to that shown in Fig. 1.15. The bandwidth was 23 GHz without bias voltage and 45 GHz with 2-V or higher bias voltages. Clear eye openings at 25 Gbps without bias voltage and at 40 Gbps with a 3-V bias were demonstrated.

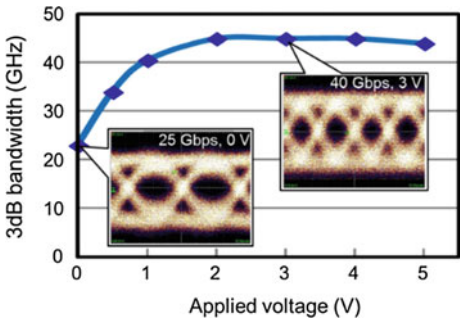


Fig. 1.35 3-dB bandwidth and eye diagrams of photodetectors with reduced contact resistance

1.7.4 300-mm Wafer Processes with ArF Immersion Lithography for WDM

Wavelength division multiplexing (WDM) is an attractive candidate to achieve off-substrate optical interconnects with further wide bandwidth because WDM can reduce its fiber count. Interferometers or resonators composed of silicon OWs, which are expected to be used for wavelength filters or multiplexers/demultiplexers, are often affected by fluctuations in their characteristics due to fluctuations in their core dimensions. High refractive index contrast of silicon OWs requires quite small errors in patterning their cores. To mitigate the problem, a 300-mm SOI wafer process with ArF immersion lithography was introduced [42]. The measured width deviation in the silicon OW cores over a 300-mm SOI wafer was less than 2.5 nm, and the measured resonance wavelength deviation of ring resonators was less than 1.2 nm, which is sufficiently small for coarse WDM systems. Sixteen-channel arrayed waveguide gratings (AWGs) with 200-GHz channel spacing fabricated using precise SOI wafer processes combined with a carefully optimized design to reduce their crosstalk were also demonstrated [43]. Figure 1.36 shows the measured wavelength response of an AWG. A low crosstalk floor of −23 dB was achieved.

1.8 Perspectives on Inter-chip Interconnects

1.8.1 Vision for On-Board Datacenters

In Sect. 1.4, we introduced a vision of on-chip servers, with which functions and performance of present on-board servers will be integrated on a substrate in the 2020s. Then, the functions and performance of present server racks will be also integrated with the on-chip servers on a board, and the high-speed inter-substrate interconnects will be optical. We call this system an on-board data center. We believe that an optical PCB that supports both electrical and optical interconnects will be required to realize on-board data centers, and an efficient and low-cost

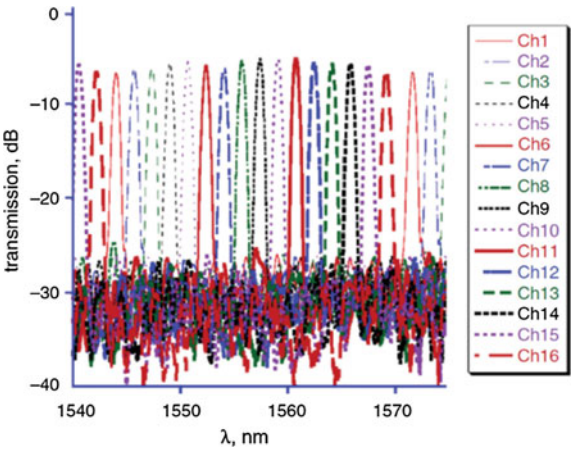


Fig. 1.36 Measured wavelength response of a 16-channel arrayed waveguide grating with 200-GHz channel spacing fabricated using a 300-mm silicon-on-insulator wafer process with ArF immersion lithography

coupling between optical devices on silicon optical interposers and external OWs, such as optical fibers or optical PCBs, will be a key technology.

The Integrated Photonics-Electronics Convergence System Technology Project, which is one of the projects in Future Pioneering Projects entrusted by the Minister of Economy, Trade and Industry (METI) of Japan, was started in 2012 as a 10-year project. The final target of this project in 2022 is to demonstrate the feasibility of on-board data centers. Therefore, optical PCBs are also being developed in the project [44]. In addition to the final target, we had set two milestones for practical applications. The first is an optical I/O core for application to an active optical cable (AOC) in 2015, and the second is an LSI package with optical I/Os in 2020. The AOCs are expected to be reduced in size and their power consumption and to extend their reach, as described in the following section. The LSI packages with optical I/Os are also expected to solve the bottlenecks of bandwidth density in the LSI pin and server front-panel.

1.9 Optical I/O Cores

Figure 1.37 shows photographs and schematic cross sections of four-channel parallel optical I/O cores, which are designed to be mounted either in an AOC module for the first milestone or around a host LSI in the LSI package for the second milestone [45]. They consist of a silicon photonics platform, optical coupling pins, a glass with through glass vias (TGVs) and a CMOS IC (driver or TIA). The use of the optical coupling pins and the TGVs simplifies the handling and setup for evaluating the samples because the optical and electrical I/O surface is flat enough to probe and mount easily. The SSCs, silicon OMs, and grating couplers are monolithically integrated on the silicon photonics platform in a Tx, and

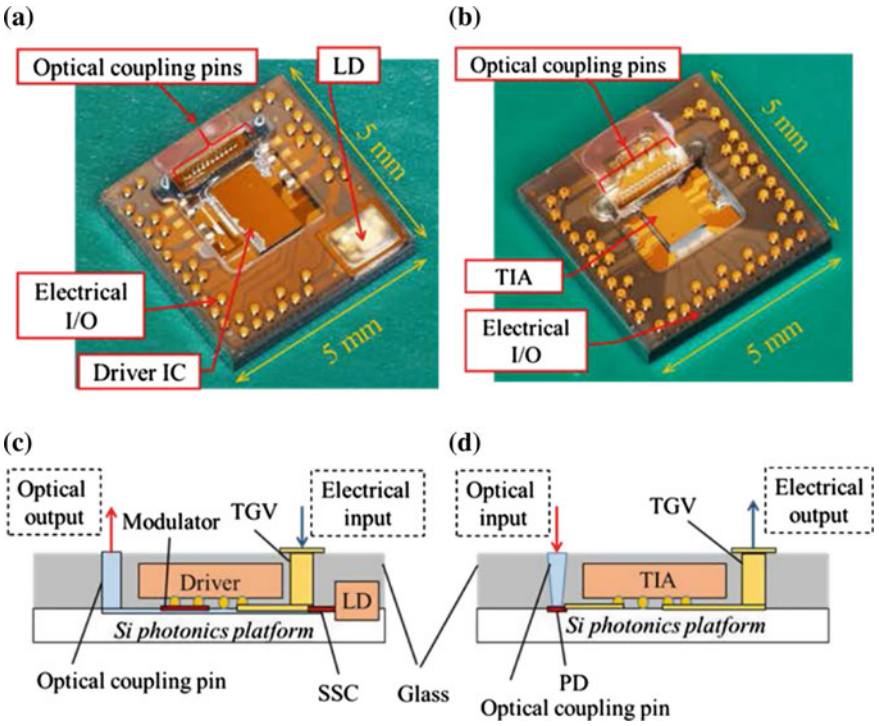


Fig. 1.37 Four-channel × 25-Gbps parallel optical I/O cores. Photographs of **a** transmitter (Tx) and **b** receiver (Rx). Schematic cross section of **c** Tx and **d** Rx

surface-illuminated germanium PDs are integrated in a Rx. An arrayed LD chip is flip-chip bonded to the substrate using a passive alignment technique, as described in Sect. 1.3.2.3. The CMOS ICs are also flip-chip bonded to the silicon photonics platform. Although the size of each optical I/O core (Tx, Rx) is only 5 × 5 mm^2, it is possible to support up to 12 channels. We believe that the small size is achieved mainly due to the hybrid integration between the photonics and electronics described in Sect. 1.2.2 and also hybridly integrated butt-coupled lasers described in Sect. 1.2.3. This small size will contribute to smaller form factors for AOCs and wider I/O bandwidth for LSI packages. Error-free data links at 25 Gbps per channel over a 300-m multimode fiber (MMF) were demonstrated. The results suggest that the optical I/O cores are usable for 100-Gbps (25 Gbps × 4 channel) transceivers, and the reach is extended by 3 times compared with conventional interconnects using VCSEL and MMF at 100 Gbps, which is up to 100 m [46]. Furthermore, the total power efficiency (or energy cost) for both Tx and Rx is 5 mW/Gbps (or pJ/bit) excluding the laser power. We estimate that the power consumption is lower than that of conventional 100-Gbps transceivers such as SR10, SR4, LR4, and PSM4 [47], even if the power consumption of LDs and clock data recoveries (CDRs) are

counted. The low power consumption was achieved mainly due to developing a lower-voltage (0.9 V) driven OM and using a 28-nm CMOS driver and TIA, which is also thanks to the hybrid integration between photonics and electronics.

1.9.1 Further Efficient Interconnects for On-Board Datacenters

Since the power consumption of a processor chip is expected to be around 100 W now and in the future, the power consumption of the optical I/O cores will exceed the processor power consumption if the power efficiency remains at 5 mW/Gbps and the inter-chip bandwidth grows beyond 20 Tbps. Therefore, our final target of power efficiency in the project is 1 mW/Gbps in 2022. To develop efficient devices, we may need stronger interactions between photons and electrons by using nano-structures such as photonic crystals [48] or plasmonics [49], and/or by using new materials such as compound semiconductors [50] or graphenes [51]. To develop efficient and flexible systems, we have to also examine network topology and routing architectures. We therefore may need efficient optical circuit switches or wavelength selective switches.

1.10 Conclusion

The problem we focused on was regarding bandwidth bottlenecks in inter-chip interconnects. To solve this problem, we first examined integration between photonics and electronics and integration between light sources and a silicon OW platform. Based on these examinations, we proposed a photonics–electronics convergence system with silicon optical interposers, which are hybridly integrated with LSIs and LDs and monolithically integrated with the other optical components on a silicon substrate. It is an optically complete and closed system. We also investigated configurations and characteristics of optical components for the silicon optical interposers, such as silicon OWs, hybridly integrated on-chip light sources, silicon OMs, and germanium PDs. The configurations are unique such as OWs with rectangular cores, light sources with high-density arrayed LDs and trident SSCs, and OMs with side-wall gratings, and the characteristics are suitable for the integrated silicon optical interposers. Then, we designed and fabricated silicon optical interposers integrated with the optical components on a silicon substrate. We achieved error-free data links with high bandwidth density of 30 Tbps/cm^2 by using the silicon optical interposers. The bandwidth density is sufficient for demand in the late 2010s. For practical applications, the optical interposers should be usable under high temperature conditions and rapid temperature changes so that they can cope with the heat generated by mounted LSIs. Therefore, we also designed and

fabricated athermal silicon optical interposers integrated with QD-LDs and other temperature-insensitive optical components. We demonstrated error-free data links with the athermal interposers operating up to 125 ºC without any adjustments. The interposers are tolerant of the heat generated by the LSIs and usable over the extended industrial temperature range without complex monitoring or feedback controls. To verify the feasibility of the silicon optical interposers with more practical configurations, error-free data links at 25 Gbps with silicon optical interposers, TIAs, and FPGAs mounted on PCBs were also demonstrated. More advanced optical components and fabrication process, which are expected to be applied for optical interconnects that will have wider bandwidth in the future, have also been developed in the PECST project, some of which were introduced. Finally, we introduced the new IPECST project aim of demonstrating the feasibility of on-board data centers in 2022 and one of their latest achievements, optical I/O cores.

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Chapter 2
Silicon Quantum Photonics

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Abstract The recent development of chip-scale integrated quantum photonic circuits has radically changed the way in which quantum optic experiments are performed, and provides a means to deliver complex and compact quantum photonic technologies for applications in quantum communications, sensing, and computation. Silicon photonics is a promising material system for the delivery of a fully integrated and large-scale quantum photonic technology platform, where all key components could be monolithically integrated into single quantum devices. In this chapter, we provide an overview of the field silicon quantum photonics, presenting the latest developments in the generation, manipulation, and detection of quantum states of light key on-chip functions that form the basic building blocks of future quantum information processing and communication technologies.

2.1 Introduction

By harnessing the unique properties of quantum mechanics (*superposition* and *entanglement*) to encode, transmit, and process information, quantum information science offers significant opportunities to revolutionize information and communication technologies. The first quantum information technologies have begun to arrive, but significant scientific and technological advances are required to realize their full potential. These quantum technologies include quantum communication, which offers the ultimate in information security, and is in the first stages of commercial exploitation [1]; quantum sensing, which enables enhanced measurement precision, beyond the shot-noise limit [2]; and quantum computation and quantum simulation [3, 4], which offer exponentially greater computing power than

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today's conventional technologies, and could have major impacts in many areas of science and technology.

Of the various approaches to realizing quantum technologies (including ion traps, nuclear magnetic resonance, superconductors, and solid state systems), photonics is particularly prominent, where single particles of light (photons) are used to encode, transfer, and process quantum information in the form of quantum bits (qubits). Photons are ideal quantum particles for communications due to their speed-of-light travel, and their excellent transmission properties, as is evident from the success of the fiber-optic communications network. Photons are also a leading contender for the *processing* of quantum information, owing to their low noise (they do not decohere), and their ease of manipulation. Each individual photon—representing a qubit of information—can be generated, controlled, interfered, manipulated, and detected using optical components.

The field of quantum optics, established in the early 1980s with the first demonstrations of entanglement [5], has flourished, with many proof-of-principle demonstrations testing the very foundations of modern physics, and with the development of new applications—from fundamental demonstrations of 11-dimensional quantum entanglement [6] to the commercialization of secure quantum communications systems [7]. However, current state-of-the-art experiments are limited to the "few- photon" regime, occupying many square meters of space on an optical table, constructed from discrete bulk optical elements, with no routes to scalability and far from outperforming conventional technologies.

Integrated quantum photonics has recently emerged as a new approach to address these challenges [8, 9]. Initial demonstrations focused on glass-based waveguide technologies, with demonstrations including waveguide circuits with high-fidelity quantum interference and quantum logic operations [8], multiparticle quantum walks [10], generation and manipulation of entanglement with a reconfigurable quantum circuit [11], and bosonic sampling [12–14].

Despite having propelled the field into new directions, integrated quantum photonics is already reaching limitations in complexity and functionality—with even simple circuits requiring devices 10 cm in length, and with limited prospects of scaling up. Silicon photonics provides a promising technology platform to overcome these limitations. Silicon photonics offers the potential for a fully integrated and large-scale quantum technology platform, having individually demonstrated all the key components required for linear quantum optics. Its high refractive index contrast, strong light confinement, and small waveguide dimensions ($200 \times 400\ nm^2$) enable ultra-compact photonic components and bend radii of 1 μm—resulting in component densities 100,000 times greater than glass waveguide circuits—with demonstrations of devices comprising thousands of individual optical elements within just millimeters of footprint [15, 16].

In this chapter, we outline the key requirements for a linear optic quantum technology platform in silicon. We present the current state-of-the-art in silicon quantum photonics, highlighting key demonstrations of single-photon building

blocks, and show the first stages of integration. Silicon photonics has demonstrated (to varying degrees of performance) all the key functions required for linear quantum optics—however, there are a number of outstanding challenges that remain. Individual components must be engineered to achieve sufficiently high performance, and particularly with low photon loss. All components must be integrated into a single system. If superconducting single-photon detectors are used, then cryogenic operation will be required. The longer term active control with fast switching and feedforward is needed for many quantum information processing architectures, which will require integration with control electronics, low-loss optical delay lines, and fast optical switching. Ultimately, a scaling up to many hundred thousands of individual optical elements will be required for quantum computing applications.

Silicon quantum photonics has the potential to deliver a fully functioning scalable, reliable, and compact quantum technology platform that is amenable to large-scale manufacture, and will enable new applications in quantum communication, sensing, simulation, and computation. Ultimately, it could enable quantum-enhanced applications to exist outside of the research laboratory, in the real world.

2.1.1 Quantum Information

The unique properties of quantum systems can be leveraged to handle information. In some cases, manipulation of quantum information can be dramatically more efficient than would be possible classically. Quantum mechanics enables point-to-point communication with physically guaranteed security [17–19]. Measurements made with entangled quantum particles can achieve maximum sensitivity, beating the shot-noise limit [20]. Finally, quantum computation [3] and simulation [21] offer tremendous improvements in processing power for certain algorithms.

The photon's light-speed travel and long coherence time make it an obvious information carrier for both quantum communication and measurement schemes. However, these same properties seem to hinder its use in computation. In 2001, a scheme was developed for quantum computation with photons that does not require photonic qubits to interact for computation to proceed [22]. The scheme (KLM, after its inventors) simply requires a source of identical photons, a reconfigurable optical interferometer, and detectors able to tell how the photons scattered in the interferometer. This invention started the field of linear optical quantum computation (LOQC). Since 2001, other proposals have improved upon KLM, to increase its efficiency and better handle various quantum and classical errors. The technological requirements, however, remain largely unchanged, and very challenging.

2.1.1.1 Entanglement

Quantum speed-ups—in communication, measurement, and computation—are due to entanglement, a strange property of multiparticle quantum systems. Entanglement between photons and the vacuum lends quantum communication channels their security; entanglement between photons passing through a sample allows its high-sensitivity measurement; and entanglement between quantum bits allows for the non-local calculations of quantum computation.

Entanglement is the property of a coherent multiphoton state which—if present—prevents the state of each photon from being described independently. If each photon *can* be described independently, the state of the system is 'separable'—the opposite of 'entangled'. Due to this backward description—a state is entangled if it is not separable—entanglement can be difficult to quantify [23]. The control and quantification of entanglement forms a large part of our discussion, in Sect. 2.5, of silicon quantum photonic experiments performed to date.

2.1.1.2 Path-Encoded Qubits

A quantum bit—or 'qubit'—is like a classical bit in that it can take on one of the two values: 0 or 1. We write these values in terms of state vectors, as $|0\rangle$ and $|1\rangle$. States of multiple qubits are written like bit strings: $|00\rangle$ represents two qubits, each in the 0 state, for example. Unlike classical bits, however, quantum bits can occupy states in a *superposition* between strict 0 and 1 s. In general, the state of a single qubit is written as

$$\cos(\theta/2)|0\rangle + \sin(\theta/2)\mathrm{e}^{i\phi}|1\rangle, \tag{2.1}$$

where the angles θ and ϕ uniquely describe the state. When $\theta = 0$, the qubit is $|0\rangle$; when $\theta = \pi$, the qubit is $|1\rangle$; and when $\theta = \pi/2$, the qubit is in a perfect superposition between $|0\rangle$ and $|1\rangle$, as evidenced by the equal amplitudes of the two states' coefficients in (2.1). The angle ϕ is known as the *phase* of the qubit, and has no classical analog. It is what separates the qubit superposition $(|0\rangle + |1\rangle)/\sqrt{2}$ from flipping a balanced coin with 0 on one side and 1 on the other. The two angles θ and ϕ provide a convenient representation for a single qubit, in terms of spherical coordinates. A qubit occupies a point on the surface of the Bloch sphere (Fig. 2.1a) given by the polar angle θ and the azimuthal angle ϕ.

Photonic qubits encoded in the path degree of freedom have historically been referred to as dual-rail qubits. Here, we refer to them simply as *path* qubits. This nomenclature fits with the widely discussed *polarization* and *time-bin* qubits. A path qubit is a photon spread between two spatial modes. In integrated quantum optics, these are normally the modes of single-mode waveguides, so a path qubit lives within a pair of waveguides. Basic operations on path qubits are shown in Fig. 2.1b. We can manipulate path qubits with rotations around the Bloch sphere as shown in Fig. 2.1a. $\hat{R}_z$ and $\hat{R}_y$ rotations are realized, respectively, by a phase shifter,

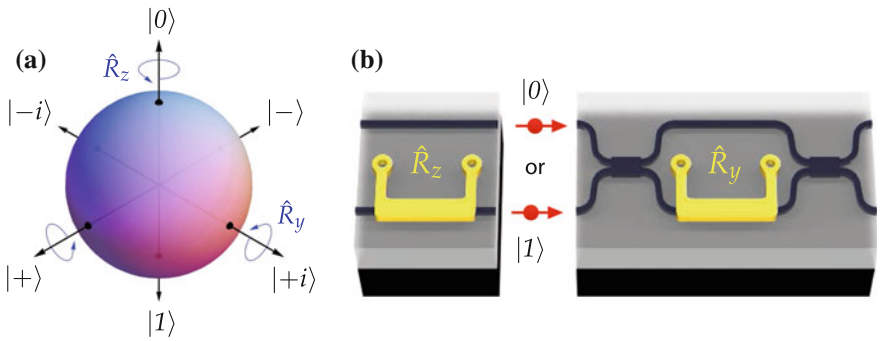

Fig. 2.1 Photonic qubits. **a** The standard Bloch sphere representation of a qubit, with typical cardinal states labeled. **b** Path encoding for photonic qubits. Path qubits are encoded in a single photon which occupies one of the two waveguide modes. If the photon is in the *top* (*bottom*) mode, we call it $|0\rangle$ ($|1\rangle$). Rotations about the z- and y-axes are shown, labeled $\hat{R}_z$ and $\hat{R}_y$, respectively, and formed by a single-phase shifter, and a Mach–Zehnder interferometer

and a phase shifter between two beam splitters—a Mach–Zehnder interferometer (MZI). An arbitrary preparation of a single qubit, starting from $|0\rangle$, is implemented using two rotations, $|\psi\rangle = \hat{R}_z(\theta_2)\hat{R}_y(\theta_1)|0\rangle$, and an arbitrary operation on a single qubit is implemented using three, $|\psi\rangle = \hat{R}_z(\theta_2)\hat{R}_y(\theta_1)\hat{R}_z(\theta_0)|\phi\rangle$, for an arbitrary $|\psi\rangle$ and $|\phi\rangle$.

2.1.2 Optical Requirements for Quantum Applications

To realize the optical quantum advantages discussed in Sect. 2.1.1, there are several technological requirements which must first be satisfied. A general linear optical quantum system is depicted in Fig. 2.2, broadly comprising photon sources, reconfigurable interferometers, and single-photon detectors.

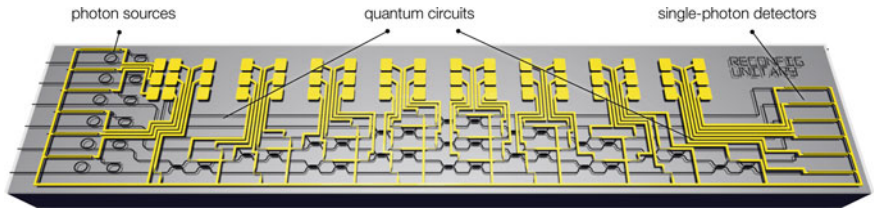

Fig. 2.2 General picture of linear optical quantum technologies, showing the three main components: a source of photons, a linear optical quantum circuit, and single-photon detectors

2.1.2.1 Photon Sources

First, we require a source of single photons—special states of light with no uncertainty in intensity [24]. Since laser light, sufficiently attenuated, resembles a single photon, applications which require just one photon can use attenuated laser pulses. This is the case for quantum key distribution (QKD) systems, for example. LOQC and quantum metrology applications require bursts of many photons, so the attenuated laser approach is insufficient.

True single photons [24] are emitted by singly-excited atom-like systems: atoms, solid state color centers, and quantum dots. However, most quantum optics experiments to date have not used single photons, but correlated *pairs* of photons, produced by nonlinear optical processes.

In $\chi^{(2)}$ nonlinear media, spontaneous parametric down-conversion (SPDC) allows a single photon from a bright pump to scatter into two daughter photons of lower frequency. SPDC is difference frequency generation, but with the usual stimulating field instead provided by vacuum fluctuations. Similarly, in $\chi^{(3)}$ nonlinear media, the spontaneous version of four-wave mixing (FWM) can be used. In spontaneous four-wave mixing (SFWM), two photons from a bright pump (frequency ν_p) are scattered to higher and lower frequencies (signal ν_s, and idler ν_i), such that

$$2\nu_p = \nu_s + \nu_i. \tag{2.2}$$

Multiplexing has been proposed to engineer true on-demand single-photon sources from probabilistic SPDC and SFWM photon-pair sources. One photon from a pair is used to *herald* the presence of the other. The original space-multiplexed proposal [25] by Migdall has been elaborated on [26], and converted into time-multiplexed [27–29], time-frequency [30], and time-space hybrid [31] architectures. Several small-scale experiments have been performed [31, 32], including with some parts integrated [33, 34]. Multiplexing requires fast single-photon detection, control logic, and optical switching.

2.1.2.2 Linear Optics

Given a suitable source of photons, we must be able to manipulate them to encode our quantum algorithm, our measurement, or our communication protocol. This is facilitated by linear interferometers formed by generalized beam splitters and phase shifters.

Since quantum states cannot be copied, quantum states of light cannot be amplified. For this reason, low optical loss is of primary importance for quantum optical systems. All optics must have high transmission. The chance to transmit N photons through an optical system with transmission η scales as η^N. Since

experiments to date have used only a handful of photons (e.g., $N = 2$), significant loss has been tolerable. As the number of photons increases, however, this exponential penalty will become very costly for lossy optical systems.

To apply different algorithms or protocols to our photons, and to tune systems into high-fidelity operation, we require interferometers to be reconfigurable. This reconfigurability should maintain the coherence of transmitted light—it must be stable. The stability of our devices must extend to optical path length and phase, as well. Bulk- and fiber-optic interferometers must be actively phase-locked.

Indistinguishability underpins linear quantum optics. For two photons to be indistinguishable, they must be identical in all degrees of freedom: arrival time, frequency spectrum, polarization, transverse mode, and et cetera. When these criteria are satisfied, indistinguishable outcomes can interfere quantum mechanically, either growing or shrinking in likelihood.

The quintessential example of quantum interference, demonstrated by Hong–Ou and Mandel in 1987 [35], involves causing two photons to meet in the simplest nontrivial linear interferometer—a beam splitter. This situation is depicted in Fig. 2.3. Photons transmitted across the beam splitter acquire a phase of $\pi/2$, while those reflected acquire no phase. The two bunching events—either in the top output or the bottom output—are distinguishable, so do not interfere. In one splitting event, when both photons are transmitted, each photon acquires a $\pi/2$ phase, so together they acquire a phase of π. In contrast, when both photons reflect, neither acquires a phase, and the total phase is 0. Thus, the probability amplitudes for the two events have opposite sign and cancel, preventing any splitting from occurring ($e^{i\pi} = -e^{i0} = 1$). In contrast, for distinguishable photons (or coin flips), each of the four eventualities has the same probability: $1/4$.

Hong–Ou–Mandel interference, due to its sensitivity to photon distinguishability in any degree of freedom, is used extensively to test the quality of photons.

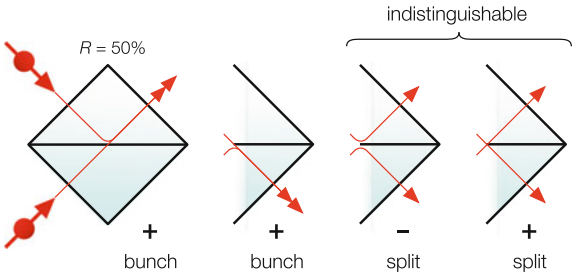

Fig. 2.3 Hong–Ou–Mandel quantum interference. Two photons are injected into each port of a beam splitter, and the two ways they can split at the output are indistinguishable. The two split possibilities destructively interfere, so only bunching is observed at the output. The canonical HOM 'dip' apparatus and result is shown in 4

2.1.2.3 Single-Photon Detection

Once photons have been sourced, then scattered inside a linear interferometer, we must determine in which output mode they scattered to. We require a single-photon detector. As with photon loss, we want detectors which miss as few photons as possible—we want detectors with high detection efficiency. After detection efficiency, we want detectors which can operate with a fast clock rate, detectors with a short reset time. Finally, if the previous criteria are satisfied, we want detectors with low timing jitter—i.e., with small uncertainty between when the photon arrives and when the detection signal emerges.

2.1.3 Scaling up Quantum Optics

To build quantum optical devices and systems on the large scale, we must integrate the functionalities of Sect. 2.1.2 on a common platform. Integrated optics has distinct advantages, over bulk and fiber implementations, in its small footprint, scalable manufacturing, and phase stability.

The on-chip integration of quantum optics proceeded from the first on-chip photon-pair source, in a lithium niobate waveguide in 2001 [36], to the first on-chip quantum interference, in glass waveguides in 2008 [8], to the first waveguide-coupled single-photon detector, based on superconducting nanowires (SNSPD) on gallium arsenide waveguides in 2011 [37]. These three pillars—photon sources, linear optics, and detectors—have flourished with various materials and new technologies. Photon-pair sources, reconfigurable optics, and superconducting single-photon detectors have been shown in silicon-on-insulator waveguides [38–40], but also in lithium niobate [41–43], silicon nitride [44–46], silica [11, 47, 48], and gallium arsenide [49, 50] waveguide systems.

2.1.4 Silicon Quantum Photonics

To process quantum information with photons and linear optics, we need unprecedented control of light, on an unprecedented scale. We need high-performance and high-yield optics, with the ability to reconfigure on the fly, as dictated by a large classical control system. We also need a source of photons, and a way to detect them. As we have discussed, several platforms have shown these key components for the on-chip quantum processing of photons.

Classical silicon photonics satisfies many of these requirements already. It provides high-density, high-yield optics. It offers methods to control light on very short-time scales. It also allows the direct integration of modern silicon microelectronics—for control and feedforward—alongside silicon optics [51]. Silicon

photonics is the most exciting growth field of integrated optics today, with huge ongoing investment from the microelectronics industry.

Silicon *quantum* photonics seeks to exploit the advantages, investment, and potential of silicon to achieve the large scales needed to process *quantum* information with photons. In silicon, photons can be sourced from the $\chi^{(3)}$ nonlinearity, manipulated using dense optics, detected on-chip, and acted on by integrated electronics and fast electro-optics. In the remainder of this chapter, we review the progress to date in developing and integrating them on a common silicon photonic platform, and discuss the challenges which lie ahead.

2.2 Linear Optics

Photonic quantum technologies require us to launch multiple single photons into large linear interferometers. These interferometers are composed of beam splitters and phase shifters. Linear optical quantum circuits (LOQC) can be conveniently analyzed using the 2nd quantization formalism [52]. We consider a linear optical network with input spatial modes $a_{\text{in},i}$ and output spatial modes $a_{\text{out},i}$ (this can be generalized to any kind of modes: polarization, time, etc.). The input modes are related to the output modes via a transfer matrix S such that the classical electromagnetic input and output field amplitudes are related via

$$\begin{pmatrix} E_{\text{out},1} \\ E_{\text{out},2} \\ \vdots \\ E_{\text{out},N} \end{pmatrix} = S \begin{pmatrix} E_{\text{in},1} \\ E_{\text{in},2} \\ \vdots \\ E_{\text{in},N} \end{pmatrix} \tag{2.3}$$

The input and output quantum states of light can be described using a Fock basis $|n_1 n_2 \ldots n_N\rangle$ where each n_i represents the number of photons in the given spatial mode i. In general, a photonic quantum state is a superposition of multiple possible photon number distributions across all the modes, with an associated probability amplitude A_k to each possibility $|n_{1,k} n_{2,k} \ldots n_{N,k}\rangle$

$$\sum_k A_k |n_{1,k} n_{2,k} \ldots n_{N,k}\rangle \tag{2.4}$$

The probability to measure a given configuration is obtained by taking the modulus squared of the probability amplitude

$$p\left(|n_{1,k} n_{2,k} \ldots n_{N,k}\rangle\right) = |A_k|^2 \tag{2.5}$$

The evolution of any arbitrary quantum state of light through such a network can be expressed using creation operators $a^{\dagger}_{\text{in},i}$ and $a^{\dagger}_{\text{out},i}$, which add a photon to an input

or output mode i, respectively. To compute the evolution through a linear interferometer, we only require the following two properties of the creation operators.

1. They obey the ladder rule:

$$a_i^\dagger |n_1 n_2 \ldots n_i \ldots n_N\rangle = \sqrt{n_i + 1}\,|n_1 n_2 \ldots n_i + 1 \ldots n_N\rangle. \tag{2.6}$$

2. The input operators can be expressed as a function of the output operators using the classical transfer matrix:

$$\begin{pmatrix} a_{\text{in},1}^\dagger \\ a_{\text{in},2}^\dagger \\ \vdots \\ a_{\text{in},N}^\dagger \end{pmatrix} = S^T \begin{pmatrix} a_{\text{out},1}^\dagger \\ a_{\text{out},2}^\dagger \\ \vdots \\ a_{\text{out},N}^\dagger \end{pmatrix}. \tag{2.7}$$

2.2.1 Beam Splitter

2.2.1.1 Quantum Interference

Quantum interference on a beam splitter—depicted in Fig. 2.3—is at the heart of many photonic implementations of quantum information protocols (e.g., [53]). In the canonical example, two photons are impinged on a beam splitter while photon coincidences are recorded between the two output spatial modes. We consider a beam splitter parameterized in the following way:

$$S^T = \begin{bmatrix} \sqrt{R} & i\sqrt{T} \\ i\sqrt{T} & \sqrt{R} \end{bmatrix}, \tag{2.8}$$

labeling the two input spatial modes as a and b, and the two output spatial modes as c and d.

Distinguishable photons Starting first with the case where the two photons are fully distinguishable (assuming they arrive in separate time bins t_1 and t_2), the input state is

$$|\Psi_{in}\rangle = |11\rangle = a_{t_1}^\dagger b_{t_2}^\dagger |00\rangle, \tag{2.9}$$

with their output state given by

$$|\Psi_{out}\rangle = \left(\sqrt{R}c_{t_1}^\dagger + i\sqrt{T}d_{t_1}^\dagger\right)\left(\sqrt{R}d_{t_2}^\dagger + i\sqrt{T}c_{t_2}^\dagger\right)|0000\rangle \tag{2.10}$$

$$= \left[i\sqrt{RT}\left(c_{t_1}^{\dagger} c_{t_2}^{\dagger} + d_{t_1}^{\dagger} d_{t_2}^{\dagger} \right) + R c_{t_1}^{\dagger} d_{t_2}^{\dagger} - T c_{t_2}^{\dagger} d_{t_1}^{\dagger} \right] |0000\rangle \tag{2.11}$$

$$= i\sqrt{RT}(|1100\rangle + |0011\rangle) + R|1001\rangle - T|0110\rangle \tag{2.12}$$

where the Fock basis order is $|0_{c_{t_1}} 0_{c_{t_2}} 0_{d_{t_1}} 0_{d_{t_2}}\rangle$. It follows that the probability to obtain a coincidence between modes c and d is $P_{\text{dist}} = R^2 + T^2$, which for a balanced beam splitter ($T = R = \frac{1}{2}$) provides $P_{\text{dist}} = \frac{1}{2}$.

Indistinguishable photons In the case where the two photons are indistinguishable, the input state can be written as

$$|\Psi_{in}\rangle = |11\rangle = a^{\dagger} b^{\dagger} |00\rangle. \tag{2.13}$$

The output state is then given by

$$|\Psi_{\text{out}}\rangle = \left(\sqrt{R} c^{\dagger} + i\sqrt{T} d^{\dagger} \right) \left(\sqrt{R} d^{\dagger} + i\sqrt{T} c^{\dagger} \right) |\text{vac}\rangle \tag{2.14}$$

$$= \left[i\sqrt{RT}\left(c^{\dagger 2} + d^{\dagger 2} \right) + c^{\dagger} d^{\dagger} (R - T) \right] |\text{vac}\rangle \tag{2.15}$$

$$= i\sqrt{2RT}\left(|20\rangle_{cd} + |02\rangle_{cd} \right) + (R - T)|11\rangle_{cd} \tag{2.16}$$

It follows that the probability to obtain a coincidence between modes c and d is $P_{\text{dist}} = (R - T)^2$, which vanishes for a balanced beam splitter. The probability amplitude for both photons to be reflected interferes destructively with the one for both photons to be transmitted. This forces the two photons to exit the beam splitter together from the same spatial output mode.

2.2.1.2 Quantum Interference in Silicon Photonics

Evanescent couplers and multimode interference (MMI) couplers are the two main choices for implementing 2×2 beam splitter transformations in silicon photonics. Demonstrations of quantum interference in MMI (Fig. 2.4b) and evanescent couplers (Fig. 2.4c) were initially reported in 2012, with 80 % raw visibility (Fig. 2.4d), and in 2013 with 90 % raw visibility [39, 54], respectively. In both cases, the quantum interference between the two photons was demonstrated by introducing distinguishability in the photons' arrival time as highlighted on a schematic of the measurement shown in Fig. 2.4a.

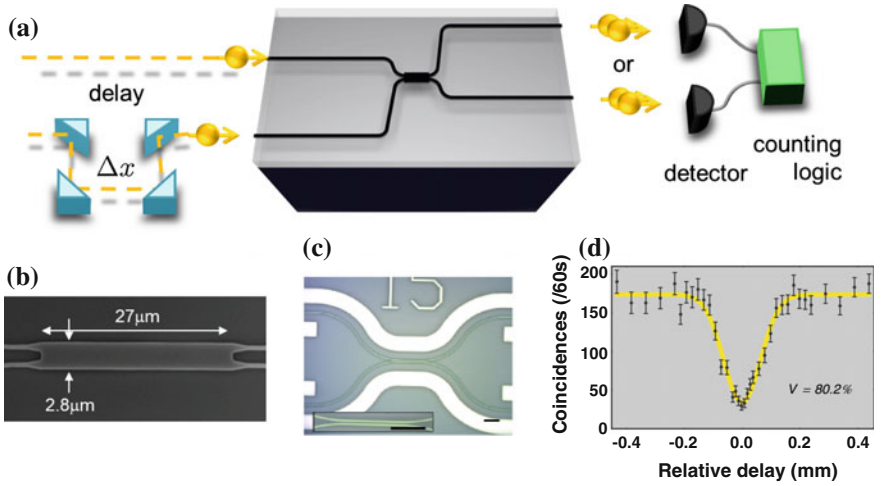

Fig. 2.4 **a** Schematic of the two-photon quantum interference experiment. Two photons are launched in a 2×2 coupler, with one going through a tunable optical delay line before insertion. Each output is monitored by a single-photon detector and coincidental events between the two detectors are recorded as a function of the relative delay Δx. **b** SEM picture of an MMI interferometer used to demonstrate quantum interference [39]. **c** Picture of an evanescent coupler used to demonstrate quantum interference [54]. **d** Signature of quantum interference in the MMI: number of coincidental events recorded as a function of the optical delay (the dip occurring at zero relative delay) [39]

2.2.2 *Phase Shifter*

The phase shifter is central to both classical and quantum interference and is especially relevant for implementing path-encoded photonic qubits (Sect. 2.1.1.2, Fig. 2.1). The demonstration of a silicon Mach–Zehnder interferometer (MZI) implementing single- and two-photon states manipulation has been reported in 2012 [39]. The evolution of the states through the MZI can be understood from the transfer matrix

$$U_{\mathrm{MZI}} = i\mathrm{e}^{-\frac{\phi}{2}} \begin{bmatrix} -\sin\left(\frac{\phi}{2}\right) & \cos\left(\frac{\phi}{2}\right) \\ \cos\left(\frac{\phi}{2}\right) & \sin\left(\frac{\phi}{2}\right) \end{bmatrix} \tag{2.17}$$

The evolution of a single-photon input state (Fig. 2.5a) is given by $|10\rangle \rightarrow -\sin(\phi/2)|10\rangle + \cos(\phi/2)|01\rangle$. The single-photon probability distribution across the two output modes is the same as the intensity distribution resulting from a classical input beam with respective probabilities $p_{\mathrm{top}} \equiv p(|10\rangle)/p_{\mathrm{bot}} \equiv p(|01\rangle)$ from exiting the top/bottom output (Fig. 2.5c, top frame),

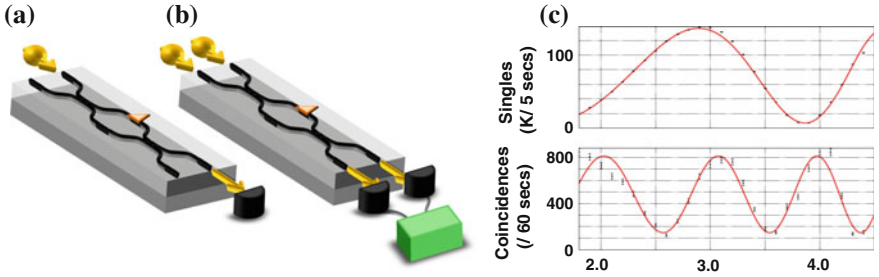

Fig. 2.5 **a** Schematic of the Mach–Zehnder interferometer probed by single photons. **b** Schematic of the Mach–Zehnder interferometer for two-photon fringe measurement. **c** Single-photon and two-photon fringes obtained from an on-chip silicon Mach–Zehnder interferometer. The *top* plot shows single-photon count rate as a function of voltage applied to the thermo-optic phase shifter for the input state $|10\rangle$ when using configuration (**a**). The *bottom* plot shows two-photon coincidence count rate as a function of applied voltage for the input state $|11\rangle$ when using configuration (**b**)

$$p_{\text{top}} = \sin^2\left(\frac{\phi}{2}\right) \qquad p_{\text{bot}} = \cos^2\left(\frac{\phi}{2}\right). \tag{2.18}$$

In order to show operation with quantum light, one can measure the effect on a two-photon input state, $|11\rangle$. When measuring the coincidence counts between the two outputs (Fig. 2.5b), the resulting $\frac{\lambda}{2}$-like fringe has no classical counterpart. The evolution proceeds as

$$= |11\rangle = a^\dagger b^\dagger |00\rangle \tag{2.19}$$

$$\rightarrow \left[\frac{\sin(\phi)}{2}\left(d^{\dagger 2} - c^{\dagger 2}\right) + \cos(\phi) c^\dagger d^\dagger\right]|\text{vac}\rangle \tag{2.20}$$

$$= \frac{\sin(\phi)}{\sqrt{2}}(|02\rangle - |20\rangle) + \cos(\phi)|11\rangle. \tag{2.21}$$

The probability to measure a coincidence is then $p(|11\rangle) = \cos^2(\phi)$, which fluctuates twice as fast as a function of the phase compared with the single-photon case (2.18). An example of this phase-doubled fringe is shown in the bottom frame of Fig. 2.5c.

2.3 Photon Sources

The generation of single photons on-demand is a key requirement for photonic implementations of quantum information tasks. Silicon benefits from a large $\chi^{(3)}$

third-order nonlinearity which enables *spontaneous four-wave mixing* (SFWM), an elastic process by which two photons from a bright laser beam are converted into two photons at different frequencies (Fig. 2.7b), which we label as *signal* (with average wave number k_s, and angular frequency ω_s) and *idler* (with wave number k_i, and angular frequency ω_i). Such a photon-pair source can then be used as a *heralded single-photon source* (by measuring one photon and thus heralding its partner) which, in combination with fast switches, enables the generation of single photons on-demand [55].

2.3.1 Requirements for Photon Sources

A useful heralded single-photon source should fulfill the following requirements.

- It should be efficient, meaning that it requires little pump power to generate the photon pair. This criterion is especially important to limit the total consumption of a complex circuit as well as keeping reasonable requirements on the pump removal filtering stages.
- The single photon should be in a pure state. This can only be achieved if the two photons from the pair are fully disentangled in all degrees of freedom; especially, there should be no spectral correlations.
- For the source to be used in a scalable architecture, it should have a high heralding efficiency, meaning that provided the *idler* is detected, the *signal* should have a high probability of exiting the source too.
- It should be possible to manufacture multiple sources outputting the same pure state such that quantum interference can arise between multiple sources with high fidelity.

2.3.2 A Brief Summary of SFWM Experiments in SOI

Silicon-waveguided SFWM has been shown in strip waveguides [38, 56–60] with control over polarization [61] and glass waveguide integration [62]; single-ring resonators [63–69] (Fig. 2.6b), in a self-locking double-bus configuration [70], and in coupled-resonator optical waveguides (CROWs) [71, 72] (Fig. 2.6f); very high-Q microdisk resonators [73–75] (Fig. 2.6c); one-dimensional photonic crystal resonators [76] (Fig. 2.6d); and photonic crystal line-defect waveguides [33, 77] (Fig. 2.6a), and cavities [78, 79] (Fig. 2.6e).

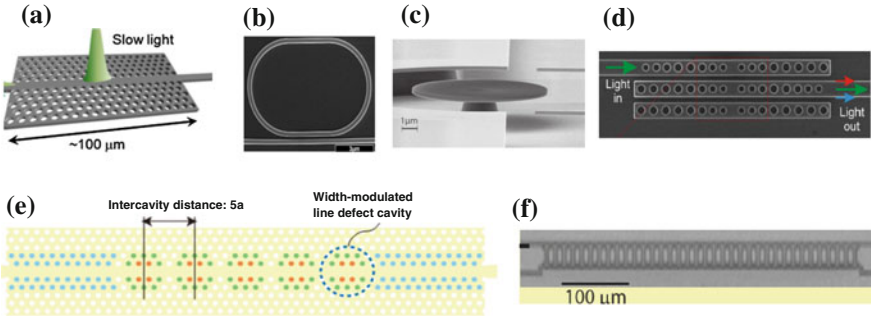

Fig. 2.6 Examples of structures for enhancing pair generation. **a** Photonic crystal waveguide. **b** Ring resonator. **c** Microdisk resonator. **d** Photonic crystal resonator. **e** Photonic crystal cavities. **f** Coupled ring optical waveguide (CROW)

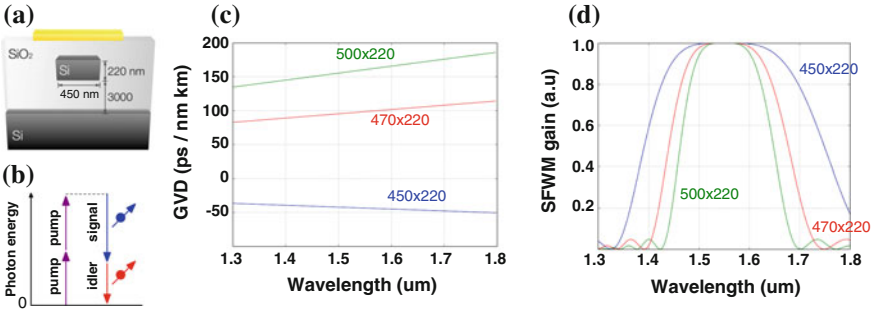

Fig. 2.7 **a** Waveguide cross section, **b** spontaneous four-wave mixing process: two pump photons are converted in a signal and idler photons, **c** Group velocity dispersion (GVD) and **d** SFWM efficiency for three different waveguide cross sections of 450 × 220 nm^2 (*blue*), 500 × 220 nm^2 (*red*), and 550 × 220 nm^2 (*green*) assuming a pump wavelength at 1550 nm and a 2.6-mm-long straight waveguide

2.3.3 *Theory of SFWM Sources*

As in the case of *stimulated* four-wave mixing, *spontaneous* four-wave mixing benefits from multiple aspects of the silicon-on-insulator platform. Silicon has an intrinsically high $\chi^{(3)}$ ($\sim$100 times bigger than in glass) with an associated intensity-dependent refractive index n_2 between 4 and 9×10^{-14} cm$^2 \cdot$ W^{-1} [80–83]. For an SOI waveguide of 450 × 220 nm^2 (Fig. 2.7a) this translates to an effective nonlinear coupling constant at 1.55 μm of $\gamma = k_0 n_2 / A_{\text{eff}} \approx 200$ m$^{-1} \cdot$ W^{-1} ($A_{\text{eff}} \approx 0.04$ μm^2 is the effective area of interaction). The high confinement of the light results in an enhancement of the power density, which increases the effective coupling by several orders of magnitude compared to bulk silicon.

For a given nonlinear interaction medium supporting a single spatial mode a, the process is described by the following Hamiltonian [84]:

$$\hat{H} = \hat{H}_L + \hat{H}_{NL} \tag{2.22}$$

where

$$\hat{H}_L = \int dk \hbar \omega_k a_k^\dagger a_k \tag{2.23}$$

is the vacuum Hamiltonian. And the nonlinear interaction is given by the SFWM Hamiltonian

$$\hat{H}_{NL} = -\int dk_1 dk_2 dk_3 dk_4 S(k_1, k_2, k_3, k_4) a_{k_1}^\dagger a_{k_2}^\dagger a_{k_3} a_{k_4} + H.c. \tag{2.24}$$

where $H.c.$ stands for Hermitian conjugate, and S captures the interaction between the different modes of the structure we are interested in (i.e., the input pump modes and the output single-photon modes).

The full procedure to compute the output state from the Hamiltonian is given in [84]. In general, one can then compute the pair generation to first order (i.e., with one pair being emitted)

$$|\Psi_{\text{out}}\rangle = \left[1 + \frac{i\beta}{\sqrt{2}} \int dk_1 dk_2 \Phi_{II}(k_1, k_2) a_{k_1}^\dagger a_{k_2}^\dagger\right] |\text{vac}\rangle \tag{2.25}$$

where

$$\Phi_{II}(k_1, k_2) = \frac{2\sqrt{2}\pi\alpha^2}{\hbar\beta} \int dk_3 dk_4 \Phi_p(k_3) \Phi_p(k_4) S(k_1, k_2, k_3, k_4) \delta(\omega_1 + \omega_2 - \omega_3 - \omega_4) \tag{2.26}$$

where Φ_p is the normalized pump spectral distribution, α is the amplitude of the pump, and β is defined such that

$$\int |\Phi_{II}(k_1, k_2)|^2 dk_1 dk_2 = 1. \tag{2.27}$$

Φ_{II} describes the shape of the joint spectral probability amplitude distribution between the signal and idler photons. It encapsulates all the contributions from the pump spectrum, the waveguide dispersion, the energy conservation, and any spectral structure due to the system considered. β reflects the efficiency of the source.

2.3.4 Silicon Waveguide Photon-Pair Sources

In this section, we discuss the simplest system in which SFWM can be implemented in SOI. It consists in a long straight waveguide which is sometimes wrapped into a spiral. We first discuss the condition for pair generation by discussing the phase-matching process. We then discuss typical pair generation rate, how to optimize the waveguide length for maximal brightness and provide experimental guideline for measuring these structures and the key notion to analyze the data measured in typical experiments.

2.3.4.1 Phase Matching

For a straight waveguide, the nonlinear interaction cross section S (cf. 2.24) depends on the phase-matching function I and the effective modal area A_{eff} as

$$S(k_1, k_2, k_3, k_4) \propto \frac{I(k_1, k_2, k_3, k_4)}{A_{\text{eff}}}, \tag{2.28}$$

where

$$I(k_1, k_2, k_3, k_4) = \int_{-L/2}^{L/2} \mathrm{e}^{i\Delta kL} = L\mathrm{sinc}\left(\frac{\Delta kL}{2}\right) \tag{2.29}$$

is the phase-matching function with $\Delta k = k_3 + k_4 - k_1 - k_2$.

The pair generation probability is proportional to the square of the phase-matching function. In addition to energy conservation, the second condition for obtaining SFWM is to operate in the regime where the phase-matching function is nonzero, and ideally where the sinc is close to 1 for maximum efficiency (see Fig. 2.7d).

We note that we ignored the pump self-phase modulation (SPM)—the process by which the pump power changes the refractive index, which in turn affects the phase of the pump beam—and cross-phase modulation (XPM) between the pump and the signal (or idler) photon—the process by which the pump changes the refractive index seen by the signal (idler) photon. This assumption holds as long as the pump power is low enough. In practice, both processes have very little impact if the pump power is low and the waveguide is short ($P < 10$ mW, $L < 1$ cm).

For long waveguides, the phase-matching condition is strictly enforced (the cardinal sine is non-vanishing only when $\Delta k \approx 0$). In the absence of SPM and XPM, the dispersion of the material imposes $2k_p = k_i + k_s$ for generating photon pairs; this is true only in the absence of second-order dispersion.

For the case we are concerned with, we do not strictly require $\Delta k_{\text{total}} = 0$. As long as the waveguide is short enough (~ 1 cm), a gain bandwidth of a few tens of nanometres can be achieved even if the waveguide cross section implies $\Delta k < 0$. This arises from the following observations. The sign of the linear phase mismatch Δk essentially depends on the group velocity dispersion (GVD) of the material [80, 85]. This can be shown by taking the Taylor expansion up to the second order of $k(\omega)$ near the pump frequency, ω_p:

$$\Delta k = 2k_p - k_i - k_s \tag{2.30}$$

$$\approx -2\left(\omega_i - \omega_p\right)^2 \text{GVD}\left(\omega_p\right), \tag{2.31}$$

where we used the energy conservation $2\omega_p = \omega_i + \omega_s$. This expression highlights that the sign of Δk depends directly on the sign of

$$\text{GVD}(\omega_0) \equiv \frac{\partial^2 k(\omega)}{\partial \omega^2}(\omega_0). \tag{2.32}$$

2.3.4.2 Pair Generation Rate

The pair generation probability (for low pump powers) in a straight waveguide of length L is given by the following relation:

$$p_{\text{pair generation}} = \frac{P^2 L^2 \gamma^2}{2} \Delta t \Delta v \tag{2.33}$$

where $\gamma = 3\chi^{(3)}\omega / 4\epsilon_0 v_g^2 A_{\text{eff}}$ is the nonlinear coupling constant. The expression (2.33) is the probability for obtaining one pair for a pulse of length Δt. In the case of a pulsed laser, the pair rate is the pair generation probability multiplied by the laser repetition rate f_{rep}. In the CW case, $f_{\text{rep}} \Delta t = 1$ (with $f \to 0$ and $\Delta t \to \infty$). Therefore, the pair generation rate per second is $R = P^2 L^2 \gamma^2 \Delta v / 2 \equiv \gamma_{\text{eff}} P^2$. We note that the dependence on the pump power is quadratic, as expected from a nonlinear process, requiring two input photons. The enhancement of the nonlinear constant due to the mode area is contained in γ. The quadratic dependence on the length is only a consequence of the approximation of a flat SFWM bandwidth. In very long waveguides, we cannot neglect the $\text{sinc}^2(\Delta k L)$ spectral shape which narrows with increasing length; this reduces the original quadratic length dependence to a linear one. Using a filter bandwidth of 1 nm, we obtain $\Delta v = 120$ GHz. For a waveguide length $L = 3$ mm, and using $\gamma = 200\ \text{m}^{-1}\text{W}^{-1}$, we obtain an effective nonlinear efficiency of about $\gamma_{\text{eff}} = 4\ \text{kHz} \cdot \text{m}\ \text{W}^{-2}$.

2.3.4.3 Optimizing a Straight Waveguide Source for Brightness

A straight waveguide with a given cross section has an effective nonlinear coupling constant γ and a given linear loss per unit length σ. The overall pair generation rate R of the process follows the following relation:

$$R \propto \gamma L^2 \left(e^{-\sigma L}\right)^2 \tag{2.34}$$

If the loss is in dB/cm, this translates to

$$R \propto L^2 \left(10^{-\frac{\sigma_{dB}}{10} L}\right)^2 \tag{2.35}$$

This function is maximal for

$$L = \frac{10}{\sigma_{dB} \ln(10)} \tag{2.36}$$

For a typical loss in a SOI waveguide of 2 dB/cm, we obtain an optimal length (for maximizing brightness) of 2.17 cm.

2.3.4.4 Pair Generation Measurement

A measurement of SFWM is typically implemented using a pump laser (pulsed or CW) seeding a nonlinear medium from which the photon pairs are collected (Fig. 2.8). Two critical filtering steps are required: a band-pass filter to prepare the pump, at the input; and a notch filter to separate the pump from the generated photons, at the output.

Any input pump power, however, small, must be removed from the spectral regions in which single photons are to be collected. We can achieve this, for instance, by combining a fiber Bragg grating and an optical circulator. The background must be suppressed down to the noise level of the detectors (typically 1000 dark counts per second, for a superconducting nanowire single-photon detector operated at high efficiency, or 10^{-5} dark count probability per gate for an InGaAs avalanche photodiode). If the in-channel noise level of the pump is around -40 dBm,[1] then filtering on the order of 100 dB is typically required.

The second step of filtering arises after the pairs have been generated. The signal and idler must be isolated from the pump before they can be detected. Assuming a CW seed of 1 mW and 1000 dark counts per second in the detector, given a single 1.55-μm photon has energy of 1.3×10^{-19} J, 130 dB of pump isolation is required.

[1]This is the case for a laser, outputting 10 mW, with a typical signal-to-source spontaneous emission ratio (SSE) of around 50 dB.

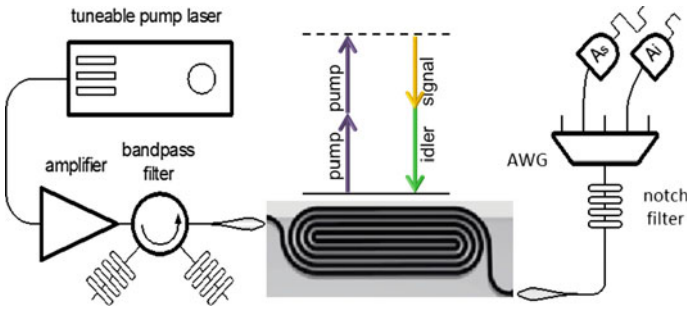

Fig. 2.8 Schematic of a SFWM experiment in a straight waveguide

This can be implemented with a single arrayed waveguide grating DWDM or by simply cascading several notch filters.

2.3.4.5 Analysis of Pair Generation Data

Photon-pair generation can be modeled as shown in Fig. 2.9a (with an example measurement apparatus shown in Fig. 2.8). Assuming a pump with low enough power such that all nonlinear processes except for SFWM can be neglected and that we can neglect multi-pair production, the following three quantities can be measured and are sufficient to characterize the process: C_s, the number of photons recorded in the *signal* channel; C_i, the number of photons recorded in the *idler* channel; and CC, the number of coincidental events recorded between the two channels.

$$C_s(P) = \eta_s\left(\gamma_{\text{eff}}P^2 + \beta P\right) + DC_s \tag{2.37}$$

$$C_i(P) = \eta_i\left(\gamma_{\text{eff}}P^2 + \beta P\right) + DC_i \tag{2.38}$$

$$CC(P) = \eta_i\eta_s\gamma_{\text{eff}}P^2 + ACC(P) \tag{2.39}$$

where $\gamma_{\text{eff}} \equiv \frac{\gamma^2 L^2}{2}\Delta t \Delta v f_{\text{rep}}$ and $ACC(P)$ (standing for accidentals) is the number of coincidental events detected which do not correspond to a pair generated.[2] When working with higher pump power, cross two-photon absorption and free-carrier absorption can be added to the model, including power dependent losses which encompass these effects [86]

[2] ACC is defined as the number of uncorrelated events leading to coincidental detections per second. It can be either directly measured or estimated using the fact that it is the product of the independent probabilities $p_i \equiv C_i\tau$ and $p_s \equiv C_s\tau$ for getting a single click from each channel within τ, multiplied by the number of coincidence window in one second $\frac{1}{\tau}$, giving $ACC(P) = C_i(P)C_s(P)\tau$.

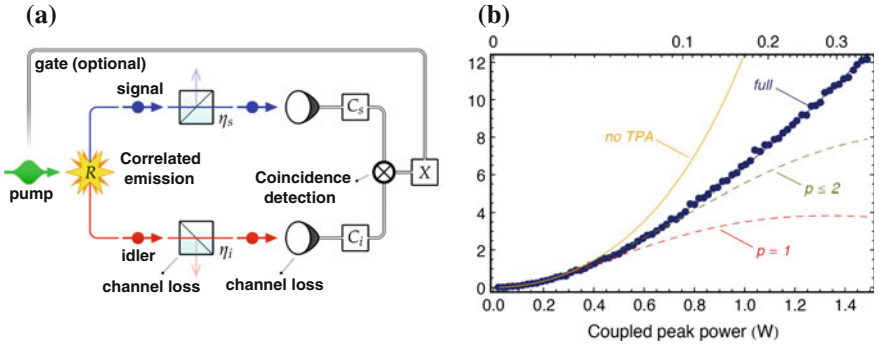

Fig. 2.9 **a** Schematic of a photon-pair generation experiment. A bright pump is used to generate photon pairs via SFWM, which are collected via two channels. The loss in each channel can be modeled by a beam splitter. It encompasses all the transmission efficiencies including off-chip coupling, filtering, and detector efficiencies. **b** Measurement of photon-pair generation in a 2.6-mm-long SOI waveguide using a picosecond-pulsed laser (≈5 ps pulse, repetition rate of 51 MHz). The squeezing parameter is shown along the top edge. The linear loss model is shown in *yellow*. The nonlinear loss model (including XTPA and FCA) accounting for different orders in the pair generation process are shown in *dash-red* (one pair), *dash-green* (one and two pairs), and *blue* (up to four pairs). The fit results in a nonlinear coefficient $\gamma = 182/\text{W m}$ and a TPA coefficient $\alpha_2 = 3.1$ ps/m

$$\eta_{\text{XTPA}}(P) \equiv \frac{1}{(1+\alpha_2 P L_{\text{eff}}/A)^2} \tag{2.40}$$

$$\eta_{\text{FCA}}(P) \equiv \frac{1}{(1+\sigma_c N_c(P) L_{\text{eff}}(2\alpha))^{\frac{1}{2}}} \tag{2.41}$$

where P is the power coupled in the waveguide, $\sigma_c \approx 1.45 \times 10^{-21}\ \text{m}^{-2}$ is the free-carrier cross section [87], $L_{\text{eff}} \equiv \frac{1-e^{-\alpha L}}{\alpha}$ is the effective length, α is the waveguide loss per unit length, A is the effective mode area, α_2 is the TPA coefficient, $L_{\text{eff}}(2\alpha) \equiv \frac{1-e^{-2\alpha L}}{2\alpha}$, $N_c(P)$ is the concentration of free carriers induced by TPA and is given by [88]

$$N_c(P) \approx \frac{\alpha_2 \tau P^2}{2h\nu A^2} \tag{2.42}$$

where $\tau = \tau_c$ in case of CW excitation with $\tau_c \approx 1.9$ ns is the free-carrier lifetime [89], or τ is of the order of the pulse length for pulsed excitations with pulse duration $\Delta t \ll \tau_c$.

η_i and η_s need to be replaced by η_i' and η_s' in 2.39 to account for XTPA and FCA by

$$\eta_i'(P) \equiv \eta_i \eta_{\mathrm{XTPA}}(P) \eta_{\mathrm{FCA}}(P) \tag{2.43}$$

$$\eta_s'(P) \equiv \eta_s \eta_{\mathrm{XTPA}}(P) \eta_{\mathrm{FCA}}(P) \tag{2.44}$$

In order to also account for multi-pair emission, a squeezed state model should be used [90]. If the photons are disentangled, a two-mode squeezed state model [91] can be used to approximate the output state. The output state can then be written as

$$|\Psi\rangle = \sqrt{1 - |\xi|^2} \sum_{n=0}^{\infty} \xi^n |n\rangle |n\rangle \tag{2.45}$$

Using (2.45) to account for multi-pair emission, a coincidental event is obtained if at least one photon is detected per channel. The full expression for the probability to detect a coincidence after subtracting the accidentals is then

$$p_{CC}(P) = (1-x) \sum_{n=0}^{\infty} x^n \left(1 - \left(1 - \eta_i'(P)\right)^n\right)\left(1 - \left(1 - \eta_s'(P)\right)^n\right) \tag{2.46}$$

$$= \frac{x \eta_i \eta_s (x^2 (1-\eta_i)(1-\eta_s) - 1)}{(1 - x(1-\eta_i))(1 - x(1-\eta_{is}))(x(1-\eta_i)(1-\eta_s) - 1)} \tag{2.47}$$

with $x \equiv \tanh^2\left(\frac{PL\gamma}{2}\sqrt{\Delta t \Delta \nu}\right)$.

Equation 2.46 can then be used to fit pair generation data. Figure 2.9b shows the difference between using the linear and nonlinear model as well as the influence of the truncation of the series describing the number of photon pairs emitted (2.46).

2.3.5 Ring Resonator

While pair generation is possible in a simple straight waveguide, the SFWM efficiency of this structure is very modest. This could be compensated in principle by adding more pump power; however, there are two reasons to avoid this approach:

1. Separating the signal and idler photon from the pump is a key challenge of SFWM sources. The more pumps we inject, the more noise we need to remove; which puts even more constraint on already drastic filtering requirements.

2. The biphoton state generated in a straight waveguide is highly entangled in frequency. The pump bandwidth needs to be greater than the filtering bandwidth to minimize the correlations between the two photons—and hence get useful photons for multiple photon experiments. Since, for a straight waveguide, the number of pairs generated is proportional to the collection bandwidth, obtaining high pair rates of decorrelated photons in straight waveguides would require very short pulses.

These two points can be addressed using resonant structures, including photonic crystal waveguides [33, 77] and cavities [76, 78, 79], microdisk [73, 74], microring resonators [63–69], or coupled-resonator optical waveguides (CROWs) [71, 72].

Among these structures, the rings are relatively easy to engineer and provide Q-factors in the 10^4–10^5 range [92, 93], which are suitable for quantum photonics applications. Higher Q-factors would result in cavity lifetimes (and photon coherence times) in the nanosecond regime, which would therefore prevent gigahertz repetition or clock rates.

Unlike normal waveguided SFWM, pairs generated by SFWM in a resonator have a fine spectral structure, which reflects the spectral structure of the host resonator. The phase-matching bandwidth itself is large—much larger than it would be in a straight waveguide of equivalent brightness—since it is only constrained by the length of the cavity. For a typical cavity length of $\sim$70 μm, the signal-idler emission bandwidth extends hundreds of nanometers from the pump. However,

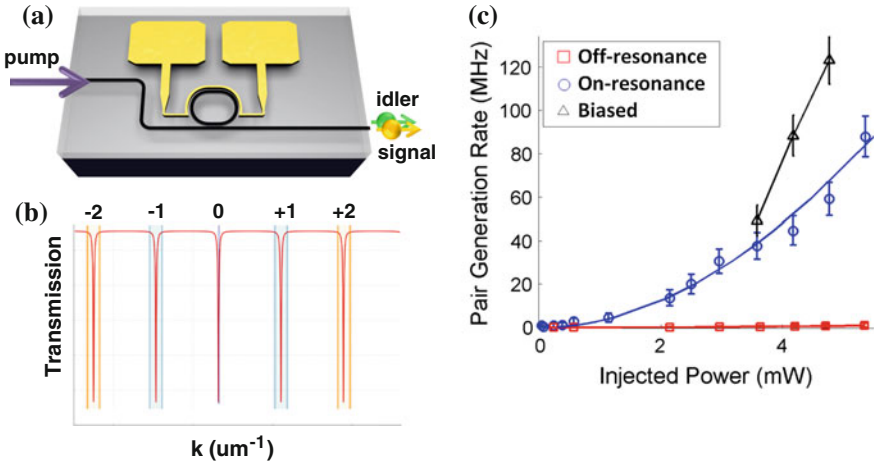

Fig. 2.10 **a** Schematic of pair generation in a ring resonator device. **b** Illustration of conditions for SFWM in a ring resonator. The *red solid line* represents the ring transmission as a function of the wave number k. Setting the pump at k_0, correlated photon pairs are generated in the resonances k_N and k_{-N} where N is an integer. Two regions where correlated pairs are generated are highlighted in *blue* (± 1) and *orange* (± 2). **c** Number of on-chip generated photon pairs as a function of the injected power in a chip [68] for three different cases: the ring is off resonance (*red*), the ring is on resonance (*blue*), and the ring is reversed bias to extract the carriers (*black*)

photon pairs tend to be generated only in the narrow resonances of the cavity (Fig. 2.10). So, for pair generation to happen in the ring, the three following conditions must be fulfilled:

1. the pump must be resonant with the ring;
2. the idler and signal must each be emitted resonantly; and
3. energy must be conserved.

We pump with a monochromatic pump (ω_0, k_0) in the middle of a resonance. For a pair of idler (ω_i, k_i) and signal (ω_s, k_s) photons to be generated, energy conservation imposes $2\omega_0 = \omega_i + \omega_s$. k_0 being the pump resonance, we define the conjugated resonant peaks k_{+N} and k_{-N} equally separated from the pump, where N is an integer. Assuming no dispersion, energy conservation leads to $k_i + k_s = 2k_0$ and we can write k_i and k_s as functions of the closest resonance index N and a detuning δk from this resonance: $k_i = k_{-N} - \delta k$ and $k_s = k_N + \delta k$. Photon pairs are generated at wavelengths for which δk is small enough (on the order of resonant linewidth).

The pair generation probability in a ring resonator, coming from a given pair of resonances (k_N and k_{-N}) pumped by a CW laser during a time Δt is given by [94]

$$p = \gamma^2 P^2 \Delta t \frac{L}{4} v_g \frac{t^8}{(1 - r\tau)^7} \tag{2.48}$$

where γ is the SFWM effective coupling constant, I is the pump intensity, L is the resonator length ($\sim$70 μm for a 1 THz FSR), $v_g = \frac{c}{n_g}$ is the group velocity in the ring waveguide, t, r, and τ are, respectively, the bus-to-ring coupling, the bus-to-bus coupling, and the ring round-trip amplitude transmission. The pair generation rate can be written as

$$R = \gamma^2 P^2 \frac{L}{4} v_g (1 - r\tau) F_{\max}^8. \tag{2.49}$$

Since four photons are involved in the process, the $F_{\max}^8$ factor can be understood as collecting a factor of intensity enhancement ($F_{\max}^2$) for each photon: two from the pump, and one each from the produced signal and idler photons. Additionally, a factor of $1 - r\tau$ results from the simultaneous production of signal and idler. Since the generation of each photon is not independent, the effect of the ring—the field enhancement—cannot be applied to each separately. It is worth noting that, in the presence of dispersion, the resonances remain equally spaced in k, but not in ω. Therefore, resonances further from the pump (large N) suffer a drop in SFWM efficiency due to a frustration in energy conservation (Fig. 2.11).

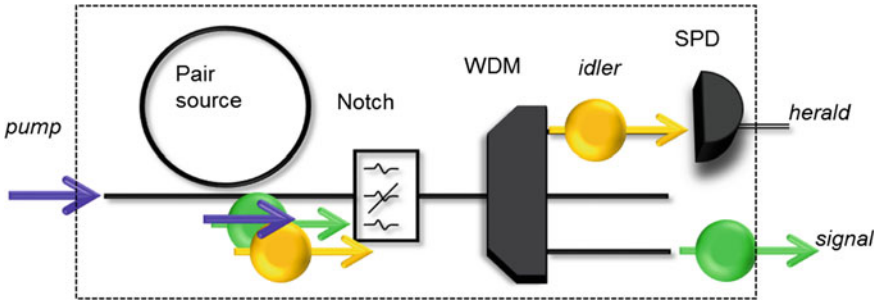

Fig. 2.11 A pump is launched in a ring resonator, producing photon pairs. The pump is suppressed with a notch filter. The single photons are filtered in different output channels with a WDM. The idler is detected with a single-photon detector (SPD), producing a *heralding* electrical pulse signaling the emission of the other photon (signal)

2.3.5.1 Optimization of the Ring Resonator for Pair Generation

A critically coupled ring ($r = \tau$) provides the maximal field enhancement. However, such a structure is not optimal as a photon-pair source. In this section, we consider the requirements for building either high-brightness photon-pair sources or heralded single-photon sources. For simplicity, we will ignore TPA, FCA, and self-phase modulation in this section.

Optimizing for brightness in the CW case The pair generation rate inside the ring resonator for a CW pump of intensity I is given by

$$R_{CW} = \gamma^2 P^2 \frac{L}{4} v_g \frac{t^8}{(1 - r\tau)^7} \tag{2.50}$$

where L is the resonator length, γ is the effective nonlinearity, v_g is the group velocity, and t is the field transmission from the straight waveguide to the ring. $r = \sqrt{1 - t^2}$ is the field reflection coefficient and τ is the field transmission per round trip ($1 - \tau^2$ being the intensity loss per round trip).

For a fixed amplitude transmission per round trip τ, R_{CW} is not maximized at critical coupling ($r = \tau$) but is maximized when $r = \frac{8 - \sqrt{64 - 28\tau^2}}{2\tau} < \tau$. However, we must also consider the probability that both photons escape the ring. Thus, the greatest pair rate inside the ring does not necessarily coincide with the most externally bright source.

When a pair is generated in the ring, each photon has a probability to escape every round trip of $T = t^2$ and it has a probability to successfully achieve another round trip of $(r\tau)^2$. The overall probability for each photon to escape is therefore given by

$$p_{\text{escape}} = T\sum_{n=0}^{\infty}(r\tau)^{2n} = \frac{1-r^2}{1-\tau^2 r^2} \tag{2.51}$$

and so the pair generation rate output by the ring is given by

$$R_{\text{CWnet}} = \frac{L}{4}\gamma^2 P^2 \Delta t v_g \frac{t^8}{(1-r\tau)^7} p_{\text{escape}}^2 \tag{2.52}$$

$$= \frac{L}{4}\gamma^2 P^2 \Delta t v_g \frac{(1-r^2)^6}{(1-\tau^2 r^2)^2 (1-r\tau)^7}. \tag{2.53}$$

Thus, the optimal ring coupling for source brightness is obtained when R_{CWnet} is maximized, which requires the ring to be somewhat over-coupled.

Optimizing for a heralded single photon-pair source We consider here the implementation of a HSPS (as defined in Sect. 2.3.1) using ring resonators for the pair generation stage. Labeling the collection efficiencies η_s and η_i for the signal and idler arms, the heralding efficiency is simply η_s. Assuming unit detection efficiency detectors, and lossless waveguides outside of the ring, η_s is then limited by the internal loss of the ring resonator. The purity of the emitted photon is directly related to the joint spectrum of the biphoton wavepacket, which is largely governed by the pump bandwidth if a resonator is used. Here, we focus on the brightness and heralding efficiency. The pair generation probability per pulse for low pump power when the ring is seeded with nearly uniform pulses in the cavity bandwidth is given by[3]

$$p_{\text{pulsed}} = \frac{\pi}{8}\frac{E_p^2 \gamma^2 \Delta t^2}{L^2} v_g^4 \frac{t^8}{(1-r\tau)^4} \tag{2.54}$$

where E_p is the energy per pulse, Δt is the pulse duration, and the other parameters are the same as defined previously. The above relation (2.54) is only valid as long as $p_{\text{pulsed}} < 0.1$.

The probability to produce a pair which exits the ring is then given by

$$P_{\text{pulsed net}} = p_{\text{pulsed}} p_{\text{escape}}^2 \tag{2.55}$$

approximated by

$$P_{\text{pulsed net}} \approx \frac{E_p^2 v_g^4 \pi \Delta t^2}{8L^2}\gamma^2 \frac{(1-r^2)^4}{L^2(1-r\tau)^4}\left(\frac{1-r^2}{1-\tau^2 r^2}\right)^2$$

[3]The derivation follows the framework developed in [95] analyzed using quantum a ring in [96].

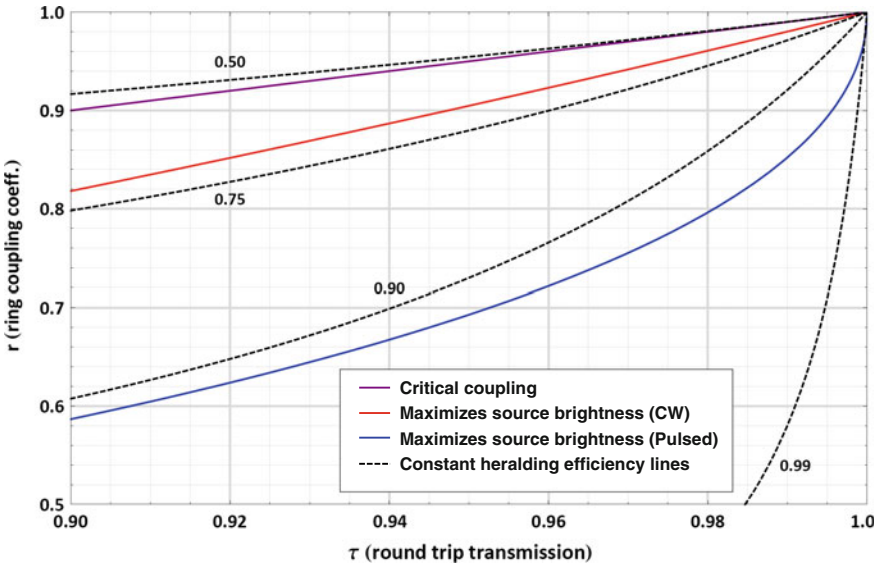

Fig. 2.12 Optimal ring coupling (r) as a function of round-trip transmission (τ) for ring designs with various purposes. The *purple line* represents the critical coupling condition when the ring is used as a filter. The *red line* is the optimal coupling for source brightness when the ring is pumped in the CW regime. The *blue line* is the optimal coupling for source brightness when the ring is pumped in the pulsed regime. The *dashed lines* represent constant heralding probabilities with values 50, 75, 90, and 99 %

$$= \frac{E_p^2 v_g^4 \pi \Delta t^2}{8L^2} \gamma^2 \frac{(1-r^2)^6}{(1-\tau^2 r^2)^2 (1-r\tau)^4} \tag{2.56}$$

We summarize in Fig. 2.12 the optimal ring designs and indicate some contours of constant heralding efficiency. The optimal pulsed case was calculated using the low pump power regime (2.56). The maximally achievable τ is constrained by the fabrication process while r can be chosen by varying the coupling length.

2.3.5.2 Experimental Pair Generation in Ring Resonators

Experiments probing the power dependence of SFWM in ring resonators must account for the resonant red shift due to thermal effects, as pump power increases. Consequently, the ring must either be tuned to compensate, or the pump wavelength must be adjusted. Several demonstrations of ring resonators for pair generation have been reported, with a 10^5 theoretical enhancement [63] compared with the straight waveguide that would have the same length as the resonator. Pair generation rates around 100 MHz have been observed [68], and a direct comparison of on- and

off-resonant behavior have been presented (showing a factor of ≈100 brightness difference). This last demonstration also included a P–N junction, used to sweep free carriers from the waveguide, and mitigate FCA; a doubling of photon-pair flux was observed when a reverse bias was applied. Time-bin entanglement from ring resonators has been demonstrated using a Franson interferometer [64, 65] with pair generation rates on the order of 10 MHz.

2.3.5.3 Joint Spectral Correlation and Source Purity

When photon pairs are produced in a parametric process, such as SPDC or SFWM, they can be entangled in several degrees of freedom. In fact, unless the source is carefully designed, the signal and idler photons will be entangled spectrally. Considering SFWM in a waveguide, with a CW pump, when a photon pair is produced, energy is conserved. Therefore, if we measure one photon, we fix the energy of the other photon such that $\omega_s = 2\omega_p - \omega_i$, where ω_i, ω_s, and ω_p are, respectively, the angular frequencies of the idler, signal, and pump photons. Such a source would produce photon pairs in a mixed state: each heralded single photon would have a different wavelength each time. In order to avoid this, a pulsed laser, with a broader pump spectrum than the resonance, can be used [96–98].

The degree of entanglement can be quantified with the Schmidt number (K) of the biphoton state which is directly related to the purity of the heralded single photon. The Schmidt number [99] $K \equiv \sum_i \frac{1}{\lambda_i^2}$ characterizes the number of orthogonal pure state vectors which are required to describe the biphoton state. The λ_i are the probability amplitudes associated with each vector in the Schmidt decomposition required for expressing the biphoton state [100]. A fully separable state is described by only one vector $|\Phi_i\rangle|\Phi_s\rangle$ with an associated eigenvalue $\lambda = 1$ and therefore $K = 1$. For an entangled state, $K > 1$, with the precise value of K depending on the dimensionality of the system and the degree of entanglement. The visibility V of a heralded HOM dip is a useful reference point for the Schmidt number K, where

$$V \leq \frac{1}{K.} \tag{2.57}$$

Thus, more entangled photon pairs yield heralded single photons which can only interfere poorly, with visibility bounded by the Schmidt number.

We provide joint spectrum simulations in Fig. 2.13 for a ring optimized for pulsed operation having $r = 0.76$ and $\tau = 0.98$. For a 1-ps pulse, the pump is

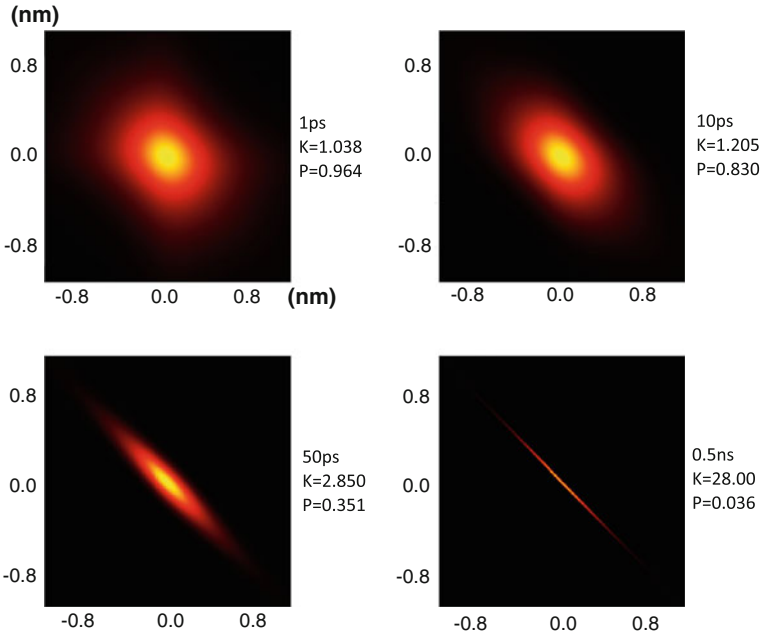

Fig. 2.13 Simulation of joint spectrum of the biphoton state obtained for different pump pulse durations in a microring resonator. Each axis represents the wavelength detuning of each photon from its average value, measured in nanometers. The color at a given pair of signal-idler frequencies represents the normalized probability to observe a photon pair at those frequencies ($|\Phi_{II}(k_1, k_2)|^2$). The three numbers displayed next to each plot are, from *top* to *bottom*, the pulse duration in ps, the Schmidt number, and the corresponding purity

spectrally flat across the resonance, which results in a high purity of the heralded photon ($\sim$96 %) and a near-unit Schmidt number. As we increase the pulse duration, the pulse no longer fully fills the resonance, and the resulting energy entanglement leads to stronger and stronger spectral correlations between the two photons; the Schmidt number increases and the purity of the heralded photon decreases.

2.4 On-Chip Detectors

No demonstrations yet exist of a waveguide-coupled single-photon detector which works at or near room temperature. Operating around 2 K, superconducting nanowire single-photon detectors (SNSPD) have recently been developed [101]. They realize near-ideal detection characteristics in a very simple package, requiring only a single patterning step (albeit a high-resolution one). Devices have primarily

employed thin films of polycrystalline NbN [101–103], but interest is moving to the amorphous WSi [104–106], MoSi [107, 108], and MoGe [109] superconductors, which allow higher yield and simpler fabrication. Detectors, primarily of NbN, have been coupled to waveguides of various materials [37, 103, 106] including silicon [40, 110]. These devices use the intimacy between guided mode and nanowire to allow for very short meanders—increasing yield—while maintaining near-unit absorption in the near-infrared. An alternate route to yield, using fabrication on a nitride membrane and a transfer technique, has been shown to allow high-yield detectors made of NbN [110], also coupled to silicon waveguides.

2.5 Integration

With the core silicon quantum photonic components demonstrated, the next logical step is to demonstrate their integration into small systems. Due to their room-temperature operation, this has largely involved the integration of photon-pair sources with passive and reconfigurable linear optics.

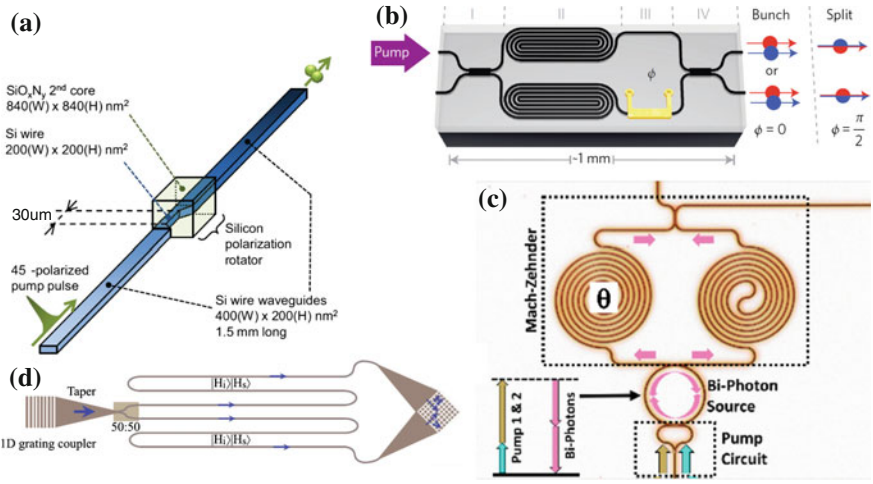

Fig. 2.14 **a** Source of polarization entangled photons. A pump is launched to excite both TE and TM equally. The TE part is phase matched to generate TE photon pairs in the first half of the source. The pump and the photons undergo then a $\pi/2$ polarization rotation. The TE photon pair is rotated to TM. The TE component of the pump after the rotator generates more TE photon pairs thus providing a polarization entangled state at the end of the source [111]. **b** Two straight waveguides are pumped simultaneously. A photon pair is in superposition of being in the *top* and *bottom* waveguides. This path entanglement is then converted to polarization entanglement, thanks to a 2-D-grating coupler [59]. **c** Path entanglement is generated between two spiral waveguides. This entanglement is analyzed on-chip using a phase shifter leading to two photon fringes [60]

2.5.1 Multiple Sources

Several groups have reported SFWM photon-pair sources embedded in simple linear interferometers: formed entirely on-chip in path [60], with counter-propagating generation in a microring resonator [66]; or formed by pumping two paths [59], or two polarizations [111], and analyzed by off-chip waveplates. In their coherent pumping of two photon-pair sources, all these devices (shown in Fig. 2.14) operate on the same principle. To elucidate this principle, we will detail the operation of the all-path-encoded version (Fig. 2.14b, [60]). This experiment resulted in high-fidelity quantum interference between two spiraled-waveguide sources enclosed in a MZI.

Starting with an input pump beam in one arm, this pump is split on the first coupler (*I*). Each arm (*II*) generates photon pairs in a state superposition. Labeling the signal, idler, top, and bottom modes as s, i, t, and b, respectively, the resulting two-photon state has the form $|1_s 1_i\rangle_t |0_s 0_i\rangle_b - |0_s 0_i\rangle_t |1_s 1_i\rangle_b$. This internal state is common to all four experiments.

A phase shift θ (*III*) is then applied to the bottom arm. Since each photon acquires the phase once, it is taken doubled by the two-photon state. The state after the phase shift is therefore $|1100\rangle - e^{i2\theta}|0011\rangle$. Finally, recombining this state on a balanced beam splitter (*IV*) leads to

$$|\Psi_{\text{out}}\rangle = \cos\theta\,|\Psi_{\text{bunch}}\rangle + \sin\theta\,|\Psi_{\text{split}}\rangle \tag{2.58}$$

where

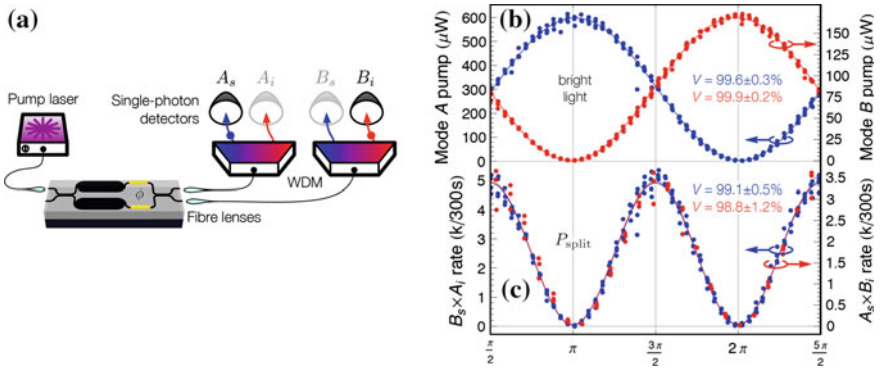

Fig. 2.15 **a** Schematic of the measurement of the two-source device. A CW pump laser is injected in the chip. Photon pairs are collected via wavelength demultiplexers (WDM), enabling the isolation of the pump from the signal and the idler. Each single photon is then measured by a single-photon detector and coincidental events are recorded. **b** Fringes obtained from the pump for both output channels as a function of the phase. **c** Coincidental events as a function of the internal phase when measuring the two different configurations for the *split* output

$$|\Psi_{\text{bunch}}\rangle \equiv \frac{|1100\rangle - |0011\rangle}{\sqrt{2}}, \quad \text{and} \quad |\Psi_{\text{split}}\rangle \equiv \frac{|1001\rangle + |0110\rangle}{\sqrt{2}}. \tag{2.59}$$

$|\Psi_{\text{bunch}}\rangle$ groups the terms where the two photons emerge in the same waveguide together, while $|\Psi_{\text{split}}\rangle$ describes the two photons emerging from different waveguides. Faithful device operation was demonstrated by measuring the two different contributions to $|\Psi_{\text{split}}\rangle$ as a function of θ, and recording a phase-doubled fringe (Fig. 2.15c).

2.5.2 *Sources and Filters*

The integration of pump rejection filters is a key step toward the operation of monolithically integrated photon-pair sources and single-photon detectors. When typically pumping with mW of power, one needs to suppress this pump below the noise level of the SNSPD (typically 1000 dark counts per second). With a single-photon energy of the order of 1.3×10^{-19} J, the filter has to provide at least 130 dB pump suppression. In most quantum photonics experiments, this filtering is performed off-chip using standard telecommunication components.

A device featuring photon-pair generation and filtering on the same chip has been realized [67] (Fig. 2.16). This device uses a Bragg grating to achieve a pump rejection of 65 dB, limited by strain reflection from the cladding and the substrate and due to the small separation between the input and output fiber couplers. Cascading two chips, and using additional integrated add–drop filters to isolate the signal and idler, a total of 150 dB pump rejection is estimated. This was tested by generating SFWM photon pairs, removing the pump on-chip, and observing a coincidence-to-accidental ratio of ≈50.

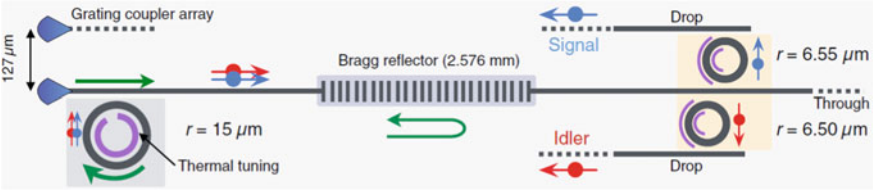

Fig. 2.16 A device enabling photon-pair generation, then suppressing most of the pumps using a distributed Bragg grating and finally isolating the signal and idler using ring resonator add–drop filters [67]

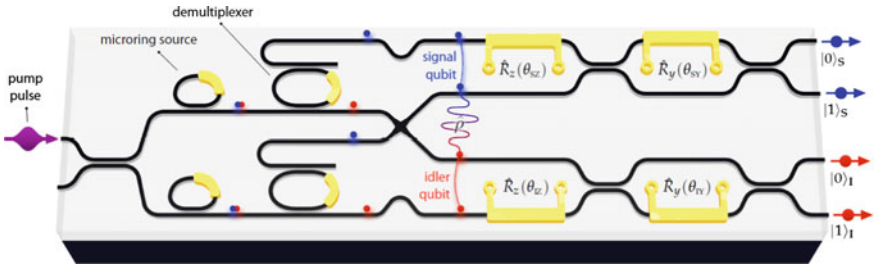

Fig. 2.17 A device enabling photon-pair generation, separation of signal/idler using ring add–drop filters, and analysis of the two-qubit entangled state on-chip [112]

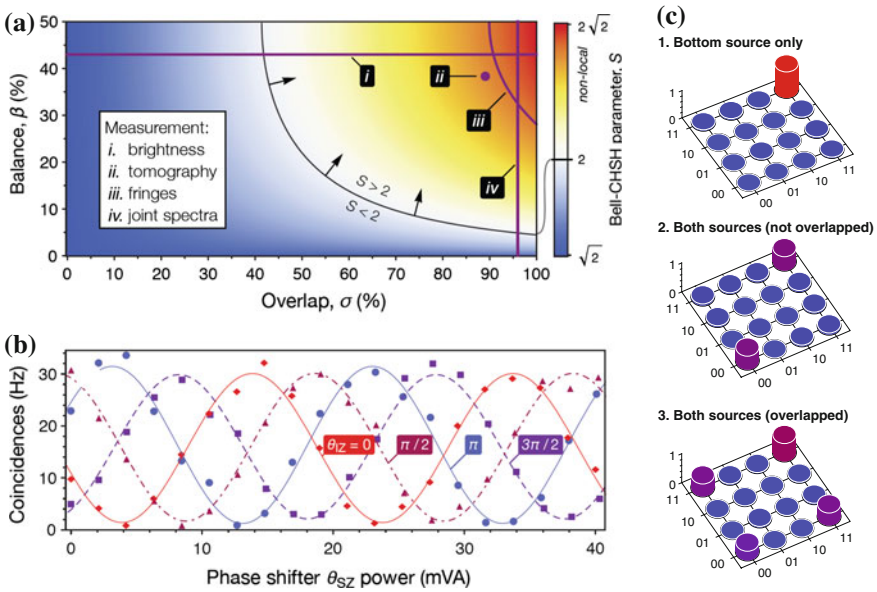

Fig. 2.18 Summary of measurements in the context of Bell-CHSH inequality violation. **a** Map showing violation S as a function of source balance β and overlap σ, with listing of measurement results overlaid. When $S > 2$, the measurement correlations are consistent with a non-local, entangled state. By measuring: (i) the brightness of each source, we can estimate the balance β; (ii) the quantum state, via quantum state tomography we can estimate both the balance β and the overlap σ; (iii) correlated fringes, we obtain a value for the violation $S(\beta, \sigma)$; and (iv) the overlap between measured joint spectra gives σ. The measurement of σ in (iv) naturally excludes multiphoton contamination, while the other measurements (i–iii) necessarily include it, and result in lower values of σ as a consequence. **b** Fringes generated by R_z rotations on signal and idler qubits, allowing a direct measurement of CHSH S parameter (denoted measurement (iii) in part a). **c** On-chip states for various device configurations, estimated using integrated analysis interferometers. Measured states are enlarged at *left*, with target states and corresponding fidelity (as defined in text) at *right*. State corresponding to *1 bottom* source only (with *top* source detuned) *2* both sources tuned but not overlapped, showing mixed state, and *3* both sources tuned and overlapped, showing path qubit entanglement

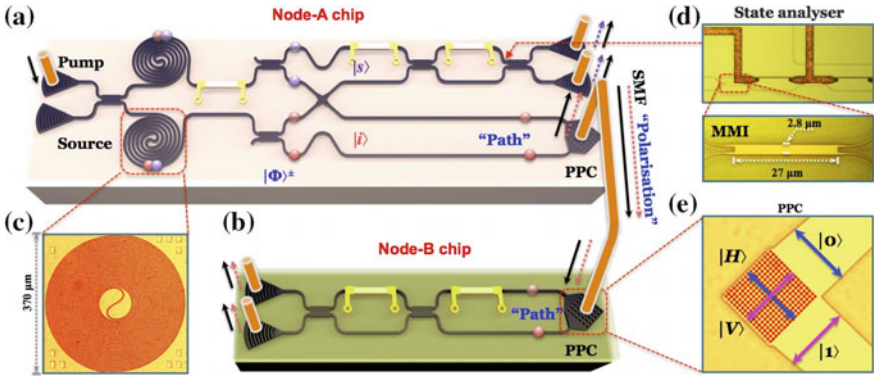

Fig. 2.19 A Bell state is generated on Alice (**a**) using spiral waveguides as photon-pair sources (**c**). MMIs are used as non-deterministic splitters to separate the idler from the signal. The idler/signal wavelengths are post-selected using an off-chip filter. One qubit goes through a single-qubit analyzer on Alice and is then sent to a signal photon detector to be measured off-chip. The second qubit is sent to a path-to-polarization converter (**d**) thus changing the path-encoded qubit to a polarization-encoded qubit. The latter is transmitted to Bob (**b**) via a single-mode fiber where it goes through a single-qubit analyzer before being detected off-chip

2.5.3 Multiple Sources and Interferometers

2.5.3.1 Integrated Path Entanglement Generation and Analysis

The demonstration of a more complex interferometer, integrated with two photon-pair sources, and frequency demultiplexers, has been achieved in 2014 [113]. The device is capable of generating and analyzing two-qubit entangled states, generated by SFWM in microring resonators. This device is shown in Fig. 2.17. A picosecond-pulsed pump is injected into the chip, where it is divided between two paths. Each path is coupled to a ring resonator, which acts as a photon-pair source, followed by an add–drop ring demultiplexer, which splits the signal and idler based on their frequencies. This device generates a two-qubit path-entangled state (see Sect. 2.1.1.2), which was analyzed using quantum state tomography [114] (Fig. 2.18), and the Bell-CHSH test for quantum non-locality [5].

2.5.3.2 Entanglement Distribution Between Two SOI Chips

The distribution of entanglement across different chips is a key development toward hybrid quantum photonics devices, multi-chip scaling, and quantum communication. The demonstration of two-qubit entanglement distribution has been performed across two chips (Fig. 2.19). A path qubit entangled state is generated on a first chip, and half of the entangled state is sent to an analyzing stage on-chip. The other

part goes off-chip via a 2-D-grating coupler, coherently converting the path qubit into a polarization qubit sent over an optical fiber. On the second chip, another 2-D-grating coupler converts the qubit back in path encoding. The qubit then goes through an on-chip analyzer. Measuring the state of the two qubits, the quality of the entangled state after distribution was then witnessed by a Bell-CHSH inequality violation of 2.63 ± 0.04.

2.6 Outlook

In Sect. 2.1.2, we outlined the elements required for realizing linear optical quantum technology with photons, and in Sects. 2.2–2.4 we detailed the community's significant progress to date in realizing these elements in silicon photonics. One core technology which silicon quantum photonics needs but currently lacks is a low-loss, and ideally fast (GHz bandwidth), switch. Several candidates exist classically [16, 115–119], but none has yet been applied to single photons, with switches come control and feedforward electronics. To date, both conventional CMOS- and superconducting SFQ-based circuits have been demonstrated [51, 120].

The final challenge to silicon quantum photonics is to integrate these elements not just on a common platform, but in a common device. This is already beginning to happen (Sect. 2.5). Detectors, in their current superconducting form, present the most complicated challenge to integration—they require everything be brought to cryogenic temperatures. Pure nonlinear optical processes are largely temperature-independent [121], so the current $\chi^{(3)}$ photon-pair sources will survive the trip, as will the current passive linear optics. The widely used thermo-optic tuners, however, must be replaced, and cryogenic operation greatly limits our choice of optical modulator. These challenges, and countless others, must be overcome before truly integrated silicon quantum photonics is possible.

2.6.1 Conclusion

Quantum technology promises to revolutionize the way we handle information. Although the control of quantum systems remains extraordinarily challenging, silicon quantum photonics, with its density and manufacturability, is a credible challenger. Silicon technology may well lead us to a second *quantum* information technology revolution.

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Chapter 3
Athermal Silicon Photonics

Jong-Moo Lee

Abstract Temperature-dependent change in refractive index of photonic waveguide devices is useful in several applications such as thermo-optic (TO) wavelength tuning and TO switching. The TO effect, however, becomes a significant burden in wavelength-filtering devices such as ring resonators and arrayed waveguide gratings (AWG) which need stable operation independent of ambient temperature. Precise temperature control is usually necessary for the stable functioning of the wavelength filters, and it cannot but cause the problem of high power consumption and high production cost. Silicon has a very high TO coefficient compared to silica, and the temperature dependence is one of the big hurdles that must be overcome to realize a massive commercialization of silicon photonics technology. This chapter reviews the various approaches to overcome the high temperature-dependent wavelength shift of photonic waveguide devices and discuss the possibility of athermal technology suitable for the silicon photonics industry.

3.1 Introduction

Wavelength-filtering devices such as AWG, Mach–Zehnder interferometer (MZI), and Bragg gratings have been successfully used for data communications. Silica material has been used most popularly for the wavelength filters for the data communications, but, recently, silicon photonics technology attracts both data and computer communications with the expectation of compact size and mass productions.

One of the problems with the wavelength filters is that temperature-dependent change in refractive index of waveguide materials can cause a high temperature-dependent wavelength shift (TDWS) [1–3]. The wavelength filters with high TDWS

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can be used if the environmental temperature is precisely controlled, but the temperature control requires extra costs in production and operation.

Silica glass is with a relatively small TO coefficient (TOC) that is about $1.1 \times 10^{-5}/^{\circ}\mathrm{C}$ and it can induce TDWS about 11pm/°C for silica-based AWG [4]. There have been many efforts to reduce TDWS of silica AWG such as using polymer material with negative TOC [4] or using thermally expanding metals to compensate the TO effect by silica [5], and some of the athermal technology have been successfully applied to commercial silica AWGs [6].

Silicon is with a relatively high TOC that is about $1.8 \times 10^{-4}/^{\circ}\mathrm{C}$ and it can induce TDWS about $70 \sim 80\mathrm{pm}/^{\circ}\mathrm{C}$ for silicon photonic devices [7]. Realization of commercially available athermal silicon photonic devices has been delayed because of the excessively high TO coefficient of silicon and the requirement of CMOS-compatible fabrication process for mass production.

In this regards, this chapter reviews the various approaches to overcome the high temperature-dependent wavelength shift of photonic waveguide devices and discuss the possibility of athermal technology suitable for the silicon photonics industry.

3.2 Background of Athermal Technology

3.2.1 Temperature-Dependent Wavelength Shift

There have been many theoretical reports on temperature-dependent wavelength shift of wavelength filters [8–10]. The free-space wavelength for the center of the wavelength filters λ_0 will obey the following equation:

$$\lambda_0 = n_{\mathrm{eff}} \frac{L}{m}, \tag{3.1}$$

where L is the physical delay length of the filter (such as the difference between neighboring waveguide arms of AWG and the circumference of ring resonator), m is an integer for the order of the filter, and n_{eff} is the effective index of the waveguide. L is a function of temperature T (considering the thermal expansion of the waveguide material) and n_{eff} is a function of temperature (considering the TO coefficient of the waveguide material), and wavelength λ (considering the refractive index dispersion of the waveguide).

Temperature-dependent variation of λ around λ_0 is derived from (3.1) as the following [8]:

$$\frac{\mathrm{d}\lambda}{\mathrm{d}T} = \left(\frac{\partial n_{\mathrm{eff}}}{\partial T} + \frac{\partial n_{\mathrm{eff}}}{\partial \lambda} \frac{\mathrm{d}\lambda}{\mathrm{d}T} \right) \frac{L}{m} + \frac{n_{\mathrm{eff}}}{m} \frac{\mathrm{d}L}{\mathrm{d}T}, \tag{3.2}$$

Temperature-dependent wavelength shift is derived from (3.2) as the following equation:

$$\begin{aligned}\frac{\mathrm{d}\lambda}{\mathrm{d}T} &= \frac{\lambda}{n_{\mathrm{eff}} - \lambda\frac{\partial n_{\mathrm{eff}}}{\partial\lambda}}\left(\frac{\partial n_{\mathrm{eff}}}{\partial T} + n_{\mathrm{eff}}\frac{1}{L}\frac{\mathrm{d}L}{\mathrm{d}T}\right), \\ &= \frac{\lambda}{n_g}\left(\frac{\partial n_{\mathrm{eff}}}{\partial T} + n_{\mathrm{eff}}\alpha\right)\end{aligned} \tag{3.3}$$

where n_g is the group index of waveguide and α is the coefficient of thermal expansion (CTE).

From (3.3), we can estimate TDWS of waveguide filters by calculating the effective index of waveguide depending on temperature and wavelength. CTE of silicon is $2.6 \times 10^{-6}/^{\circ}\mathrm{C}$ [11, 12] which is much smaller than TO coefficient of silicon ($1.8 \times 10^{-4}/^{\circ}\mathrm{C}$) by two orders. The influence of CTE to TDWS is negligibly weak compared to TO coefficient for silicon photonic wavelength filters. So, there have been many efforts to reduce TDWS of silicon photonic wavelength filters by adjusting the temperature dependence of the effective index.

3.2.2 Thermo-Optic Coefficient of Materials

Temperature dependence of wavelength filters is mainly caused by TO coefficient of waveguide materials, and the temperature dependence can be reduced if we adjust the temperature dependence of the effective index of waveguides. The effective index of waveguide can be varied by the cross-sectional structure that is composed of more than two materials and the temperature dependence of the effective index can be adjusted by the combination of materials with different TO coefficients [1–4].

TOC of material $\mathrm{d}n/\mathrm{d}T$ is known to be a sum of electronic and lattice contribution as the following equation:

$$\frac{\mathrm{d}n}{\mathrm{d}T} = \left(\frac{\mathrm{d}n}{\mathrm{d}T}\right)_{\mathrm{Electronic}} + \left(\frac{\mathrm{d}n}{\mathrm{d}T}\right)_{\mathrm{Lattice}}, \tag{3.4}$$

where the electric contribution is related to the energy band of the material and the lattice contribution is related to the thermal expansion of the material as in reference [13].

Negative temperature-dependent energy gap of semiconductor materials [14] causes a positive electronic contribution to TOC, and positive thermal expansion of materials cause a negative lattice contribution to TOC. Many materials such as silicon and silica with positive TOC are influenced dominantly by energy gap, but some materials such as polymers are influenced dominantly by its high positive CTE that is broadly distributed from ten to several hundred ppm/°C depending on its composition [12].

Table 3.1 Material properties of waveguide materials

Materials	Refractive index (at 1550 nm)	TOC ($\times 10^{-4}/^{\circ}C$)	CTE ($\times 10^{-6}/^{\circ}C$)
SiO_2	1.445	0.1	0.38
Si	3.478	1.8	2.6
Si_3N_4	1.98	0.24	3.0
Polymer	1.3 ~ 1.6	−1.0 ~ −4.5	40 ~ 200
TiO_2 (Rutile Bulk)	2.45	–	7.5
TiO_2 (Sputtered film)	2.42	−1.0 ~ 2.15	–
TiO_2 (Evaporated film)	2.13	−3.0 ~ −7.0	–

CTE of titania (TiO_2) crystal is $7.5 \times 10^{-6}/^{\circ}C$ [12] which is larger than CTE of silicon ($2.6 \times 10^{-6}/^{\circ}C$) [12] but not so much as TEC of polymer that is ten times larger than titania. But there have been many experimental reports on highly negative TOC for amorphous or polycrystalline titania materials and titania is getting attractions as a CMOS-compatible highly negative TO material.

Various combinations of materials have been tried to adjust TDWS of waveguide filters. TOC and other properties of waveguide materials are summarized in Table 3.1 based on [12, 15, 16]. The material property of polymer is variable depending its composition and the property of titania is also variable depending its formation.

3.2.3 Athermal Silica AWG

The thermo-optic coefficient of silica is 18 times lower than silicon and silica. AWG is insensitive to temperature that much compared to silicon AWG. But the industrial demand of dense wavelength division multiplexing (DWDM) application has required further temperature-insensitive athermal operation of silica AWG for 100 and 50 GHz spaced DWDM application. Through many efforts, athermal silica AWGs with TDWS less than ±10 pm for the temperature rise from 0 to 70 °C have been commercially available [6]. To understand the athermal technologies available for silicon photonics, this section reviews what kinds of efforts have been made to realize the athermal silica AWGs.

The attempt for an athermal waveguide filters has begun using polymeric material with negative TOC to compensate the positive TOC of silica [1]. Kokubun et al. proposed to use polymer upper cladding to compensate TDWS of NA45 glass core slab waveguide and experimentally showed the reduction of TDWS down to 7 % from original TDWS. They measured TDWS by inserting the slab waveguide in a Mach–Zehnder interferometer (MZI) at the wavelength of 633 nm. They used silica as the lower cladding, NA45 as the core, and Methyl Methacrylate (MMA) as the upper polymer cladding as in Fig. 3.1. Their concept of using a polymer for an

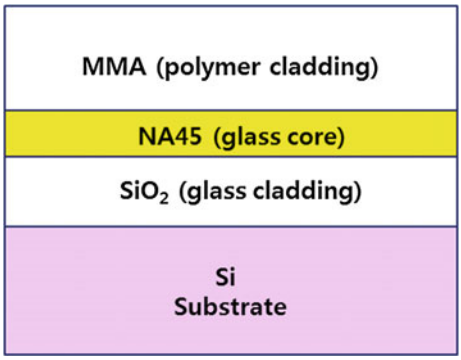

Fig. 3.1 Schematic structure of an athermal waveguide with a polymer upper cladding

athermal waveguide filter leads a new research area of athermal waveguide filters and many groups have applied their concept to almost every type of waveguide filters such as MZI, AWG, and ring resonators [1–3, 17, 18].

Inoue et al. showed another way of using polymer for an athermal silica AWG [4]. They formed a triangular groove filled with silicone adhesive, which has a negative TOC, to compensate the temperature-dependent optical path difference in a silica-based AWG. The temperature-dependent wavelength shift was reduced from 950 to 50 pm for the temperature rise from 0 to 85 °C in their experiment.

The silica athermal AWG using polymer for the TO compensation showed very nice results, but there was another method to compensate TDWS of silica AWG. Saito et al. showed an athermal silica AWG using a metal pate to compensate TDWS of a silica AWG. Figure 3.2 shows the structure of the athermal AWG with a metal plate. The circuit of AWG is cut at one of the slab waveguides and the two parts are connected by a copper plate [5, 6].

Figure 3.2 shows the mechanism of the compensation schematically. The copper plate compensates the temperature-dependent shift of focus point as shown in Fig. 3.2. The temperature-dependent wavelength shift was less than ± 10 pm for the temperature rise from 0 to 70 °C in their experiment. The athermal AWG using metal plate showed the best quality in athermal property, and the method has an additional merit of adjusting the center wavelength to ITU grid during the process of bonding the metal plate. So, the technology has been commercially used for athermal silica AWGs.

We can expect an athermal technology to be available soon for a silicon photonics from the review on athermal silica AWGs. However, there are several limiting conditions in silicon photonics compared to silica waveguide:

- High-index contrast of silicon photonic waveguides (restriction in using polymer cladding);
- CMOS-compatible fabrication process (restriction in using polymer for the low thermal degradation temperature of polymer);
- High-density integrated photonics (restriction in using metal plate because the wavelength filters have to be integrated with other photonic circuit elements).

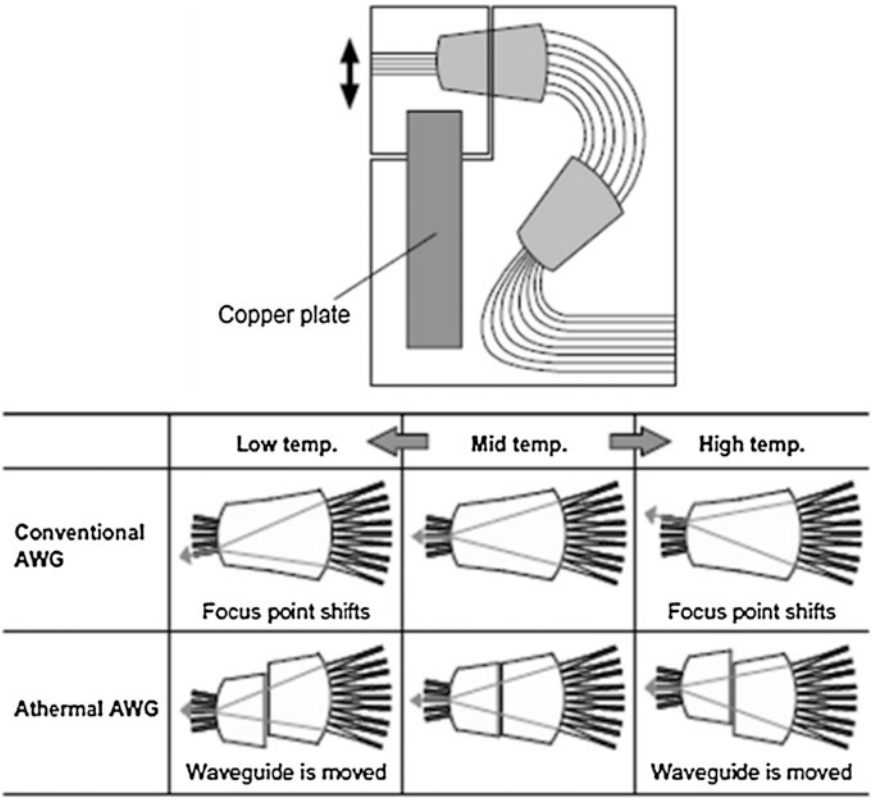

Fig. 3.2 The structure of athermal AWG using a metal plate and the mechanism of compensation, from [6]

There have been many efforts to find a technology in silicon photonics to find an athermal technology satisfying the requirements, and we will discuss it in the following sections.

3.3 Athermal Silicon Photonics Using Polymer Cladding

Successful results of athermalization using polymer cladding have been reported by many groups for silica waveguide after the first report of using polymer cladding by Kokubun et al. [1]. Thermo-optic compensation using polymer cladding can also be considered for silicon photonics, but it is much more challenging for silicon photonics than silica waveguides. TO coefficient of silicon is 18 times higher than that of silica, and the guided mode is confined too tightly within the silicon core. For an effective thermal compensation, the guided mode volume should be expanded

enough to the polymer cladding. So it is necessary to find the proper cross-sectional dimension of waveguide to compensate TDWS of silicon photonics devices.

TDWSs of silicon ring resonators for the various dimensions of the waveguide with and without polymer cladding were calculated and experimented by Lee et al. [17]. Figure 3.3 shows the schematics of their experiment using polymer cladding for thermal compensation of a silicon ring resonator. They used an SOI wafer with a top silicon layer of 220 nm and a buried oxide (BOX) layer of 3000 nm. Electron-beam lithography and dry etching were used in the fabrication of the silicon core patterns (SSC). Ultra-violet (UV) curable resin based on perfluorinated acrylate with refractive indexes of 1.49 (WIR30-490 from ChemOptics) was used as the upper cladding. TOC of WIR30-490 was about $-1.8 \times 10^{-4}/^{\circ}\mathrm{C}$ which is the same but with a reverse sign to the silicon.

They showed TDWS of silicon waveguide with the core dimension of 500×220 nm can be compensated enough for TM mode using polymer cladding but not enough for TE mode. They experimentally showed TDWS of silicon ring resonator with the core dimension of 500×220 nm and could be reduced down to 5 pm/°C for TM mode by using polymer cladding as in Fig. 3.4.

There was a minor point to discuss in their calculated results in the reference [17]. They used effective index n_{eff} instead of group index n_g for (3.3) in their calculation [17]. Figure 3.4 shows the correction in calculation of TDWS by proper use of n_g for (3.3).

They also showed the possibility of thermal compensation by polymer cladding for TE mode by inserting a waveguide section with the core dimension of 250×220 nm in a race track ring resonator as in Fig. 3.5. They experimentally showed that TDWS of silicon ring resonator including the core dimension of 250×220 nm could be reduced down to -10 pm/°C even for TE mode as in Fig. 3.5.

A slot waveguide attracts scientific attention with its peculiar property of guiding light within a narrow low-index slot between high-index materials [19]. The slot waveguide is very attractive because various materials can be inserted within the slot to change the optical property of the waveguide. Lee et al. showed that TDWS

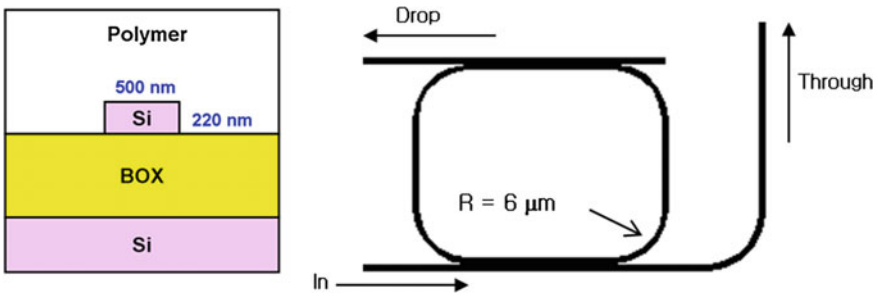

Fig. 3.3 Schematic diagram of silicon ring resonator and the cross-sectional structure of waveguide with polymer cladding

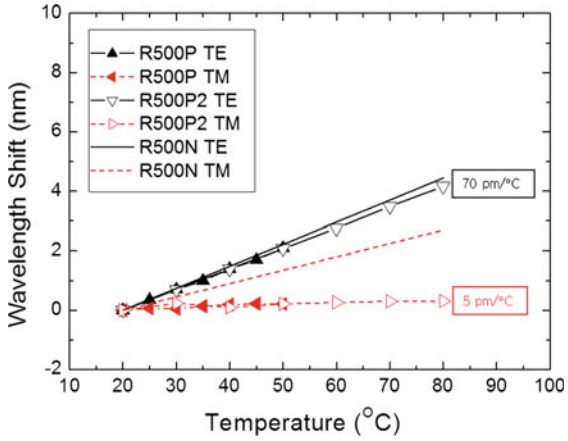

Fig. 3.4 Measured TDWS of the ring resonator with polymer cladding (R500P), in comparison with the calculated shifts without polymer (R500N). R500P2 is for another waveguide chip to show the reproducibility of the method

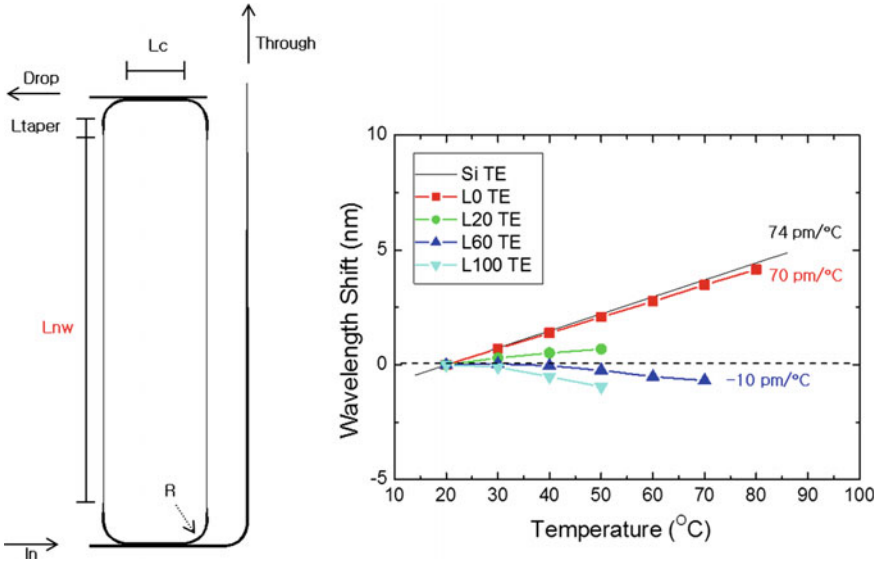

Fig. 3.5 Schematic diagram of a ring resonator with 250-nm-wide waveguide sections and the measured TDWS of the ring resonator with polymer cladding for TE mode. L20 is for Lnw of 20 μm, L60 for 60 μm, L100 for 100 μm, and L0 for the case without the narrow waveguide section. Si TE is for the calculated wavelength shift for L0

of the silicon ring resonator could be effectively reduced by adding polymer within slot waveguide [18].

Figure 3.6 shows the schematic structure and mode profile of silicon slot waveguide with polymer on it and the SEM images of the silicon slot waveguide ring resonator. The silicon slot waveguide was fabricated using electron-beam lithography and dry etching on an SOI wafer with a 220-nm-thick top silicon layer and a 3000-nm-thick buried oxide (BOX) layer. The slot was located asymmetrically between 210 and 290-nm-wide silicon wires to reduce bending loss. The width of the slot (Ws in the figure) is varied from 90 to 120 nm to control the temperature dependence of the ring resonator.

The waveguide is covered with a polymeric material to compensate the temperature dependence of the waveguide. UV curable polymers WIR30-490 and ZP49 were used separately for a comparison. The refractive indexes for the two materials were the same as 1.49, but TOC was different. TOC of WIR30-490 was about $-1.8 \times 10^{-4}/^{\circ}\mathrm{C}$, and TOC of ZP49 was about $-0.8 \times 10^{-4}/^{\circ}\mathrm{C}$. The polarization of TE mode was considered in this experiment and calculation, because TE mode is more popularly used in silicon photonics than TM mode with the merits of a low bending loss and a low leakage to the silicon substrate under the thin BOX layer.

Figure 3.7 shows the measured TDWS data in comparison with the calculation for TE mode. The experimental result was well in accord with the calculation as in

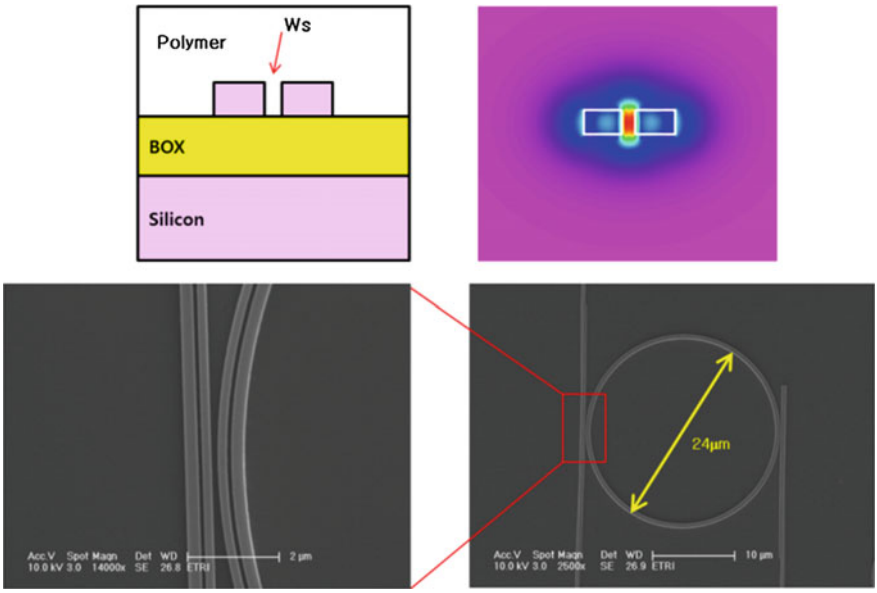

Fig. 3.6 Schematic structure and mode profile of silicon slot waveguide with polymer on it and the SEM images of the silicon slot waveguide ring resonator

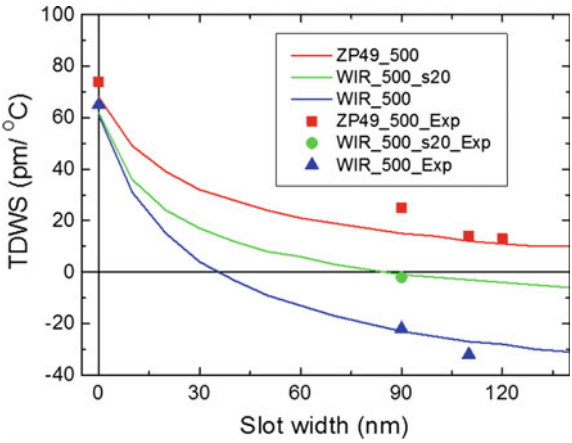

Fig. 3.7 Comparison of measured data with calculated TDWS of ring resonators depending on the width of the slot. ZP49_500_Exp is for slots with ZP49 and WIR_500_Exp is with WIR30-490 cladding. WIR_500_s20_Exp is for a rib-type slot with a 20 nm slab with WIR30-490 cladding

Fig. 3.7. These results show that TDWS can be controlled by adjusting various variables of the slot waveguide filled with polymer cladding, but the requirement of narrow width of the slot fabricated by electron-beam lithography can be a burden for a commercial application of this technology that is based on DUV photo lithography.

There have been many theoretical and experimental reports on athermal silicon photonics using polymer cladding.

Ye et al. showed general design criteria for athermal high-index-contrast waveguides using cladding materials with negative TOC [9]. They showed both analytical and empirical equations on the athermal conditions of channel waveguides of arbitrary geometry with arbitrary high-index-contrast ratio.

V. Raghunathan et al. demonstrated TDWS of 0.5 pm/°C for a silicon ring resonator with polymer cladding by considering the second-order variation of effective index and confinement factor in athermal design [10].

J. Teng et al. showed the ideal width to achieve athermal condition for the TE mode of 220-nm-height SOI waveguides around 350 nm with the bending radius of 15 μm. The narrow SOI waveguides were fabricated by DUV lithography with standard CMOS fabrication technology [20].

L. Wang et al. used polymer cladding to reduce TDWS of a compact athermal SOI-based 1 × 8 AWG with 400 GHz channel spacing [21]. The AWG was fabricated by DUV lithography with standard CMOS fabrication technology, and the size was 350 × 250 μm. By insertion of the straight narrowed arrayed waveguides and overlay polymer layer, TDWS of the AWG was successfully reduced to −1.5 pm/°C.

The remaining problem of the method using polymer cladding is the thermal degradation of the polymer during the back-end process of CMOS fabrication process. Back-end CMOS compatibility requires polymer materials with high

decomposition temperature (>400 °C) [22]. Back-end interconnect architecture on a CMOS platform involves metallization and annealing steps around 400 °C. This demands the use of a polymer clad with a high decomposition temperature. There have been many efforts to find a polymer material with high TOC and high decomposition temperature, but there has not been a report on polymer cladding satisfying both the requirements of high TOC and high decomposition temperature.

3.4 Athermal Silicon Photonics Using Titania Cladding

Using polymer cladding to reduce TDWS of silicon photonic devices is a very effective way, but polymer cladding has limits in an application for the low decomposition temperature of the polymer. P. Alipour et al. showed the possibility of using titania (TiO2) cladding instead of polymer cladding in reducing TDWS of silicon photonic ring resonators [23]. Titania is very attractive with the expectation of overcoming the temperature dependence of silicon photonic devices using CMOS compatible fabrication process because titania is a well-known CMOS-compatible material. The optical property of a titania film was not constant but variable depending on the condition of fabrication. Table 3.1 summarizes previously reported results on optical properties of titania films and their effects on reducing the temperature dependence (Table 3.2).

The refractive index of titania film has not been consistent but distributed from 2.11 to 2.42 which is lower than the index of rutile (2.45) at the wavelength of 1550 nm. TOC of titania film has been distributed from −7 to +0.2 $\times 10^{-4}/^{\circ}\mathrm{C}$ depending on the method of deposition such as sputtering, evaporation, and atomic layer deposition (ALD). Sputtering has been popularly used in deposition of titania and TOC of sputtered titania film was around $-2.0 \times 10^{-4}/^{\circ}\mathrm{C}$, which requires the width of silicon core as narrow as 275 nm [24] to effectively reduce TDWS of

Table 3.2 Optical properties of titania films and TDWS of ring resonator with the titania as cladding for TE-like mode

Deposition	Refractive index (at 1550 nm)	TOC ($\times 10^{-4}/^{\circ}\mathrm{C}$)	Si core (nm)	TDWS (pm/°C)	References
Bulk (Rutile)	2.45	–	–	–	[29]
Evaporation	2.11	−6.7	500 × 220	+5.5	[23]
ALD	2.3	−0.5 ~ +0.2	–	–	[30]
Sputtering	2.42	−2.15	275 × 250	−1.6	[24]
Sputtering	2.35	−1.0	450 × 220 150 × 220	+90 −30	[31]
Sputtering	2.18	−2.5 ~ −0.1		–	[15]
Evaporation	2.13	−5 ~ −7	450 × 220	−20 ~ + 20	[16]

silicon ring resonators for the TE-like mode. Such a narrow width of silicon core has a problem of accompanying high propagation loss and large bending radius.

In other hands, TOC of titania film deposited by evaporation was around $-6 \times 10^{-4}/^{\circ}\mathrm{C}$, which is three times higher than the sputtered titania film [23]. J.-M. Lee et al. showed that the highly negative TOC of titania film was enough to reduce TDWS of compact 5-μm-radius silicon ring resonator with the common dimension of 450 × 220 nm silicon core that is fabricated by DUV lithography [16]. TDWS of the TE-like mode of the ring resonator was reduced to $-20 \sim 20$ pm/K from 74 pm/K without a noticeable degradation in insertion loss by the addition of titania cladding as in Fig. 3.8.

One problem of the temperature dependence of the ring resonator with titania cladding was that TDWS was not consistently repeated as the temperature varied up and down. It was varied with a hysteresis during the temperature variation as in Fig. 3.9. It means the TOC of titania cladding in this experiment varied from −7 to

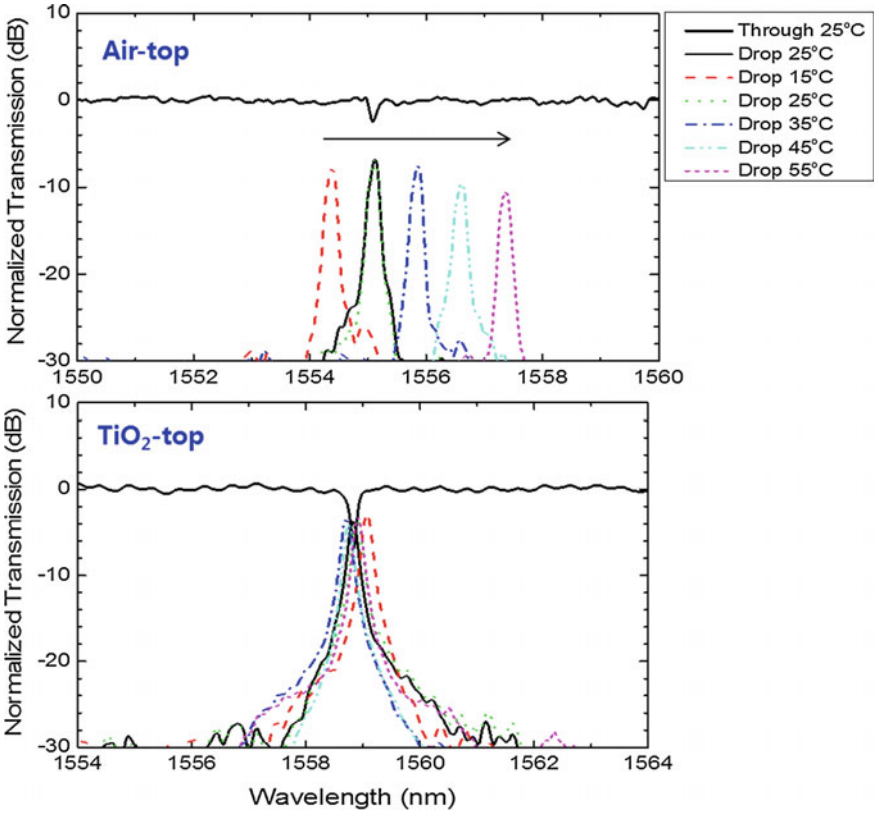

Fig. 3.8 Normalized transmission spectra of silicon ring resonator without (Air-*top*) and with titania cladding (TiO2-*top*) as the temperature varies from 15 to 55 °C

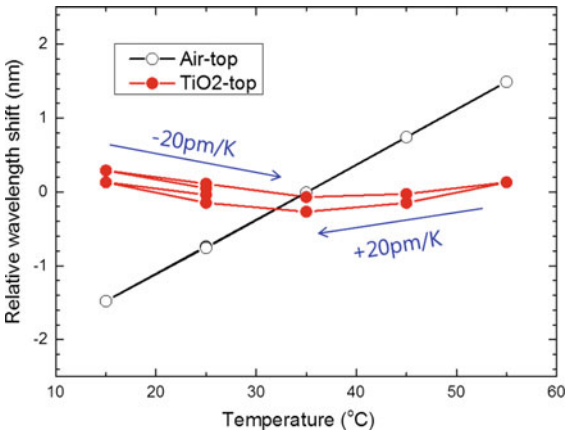

Fig. 3.9 Relative wavelength shift of silicon ring resonator without (Air-*top*) and with titania cladding (TiO2-*top*) as the temperature varies up and down from 15 to 55 °C

$-5 \times 10^{-4}/^{\circ}\mathrm{C}$ during the temperature variation. The variation of TOC of titania remains as a problem should be overcome in order to realize a stable operation of silicon photonic device with titania cladding.

3.5 Athermal Silicon MZI Without Negative TO Material

There have been many results showing the athermal silicon photonic devices using a negative TO material such as polymer or titania, but there remain problems in using the negative TO material. The polymer has difficulty in meeting CMOS compatibility because of its low decomposition temperature, and titania has the problem of hysteresis for the repetition of temperature going up and down.

In case of silicon photonic Mach–Zehnder interferometer (MZI), there is another method to reduce the TDWS of MZI without using a negative TO material [25–27]. TDWS of silicon MZI was shown to be reduced using different widths of waveguide [25, 26] as in Fig. 3.10, or using different polarizations in each of the MZI arms [27], respectively. The difference in each of the MZI arms can induce a different temperature-dependent phase change for the each arm resulting in the reduction of TDWS for the MZI.

M. Uenuma et al. proposed a method using a combination of wide and narrow waveguide in MZI to compensate TDWS of MZI coming from the change in effective length difference of the two arms. It also experimentally showed minimizing the temperature dependence down to 28 $\mathrm{pm}/^{\circ}\mathrm{C}$ using the combination of 400 and 1000 nm widths of 300-nm-thick silicon core for the asymmetric MZI

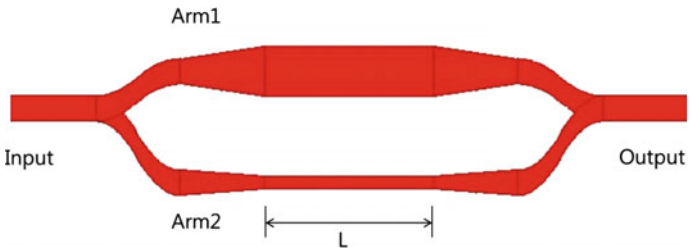

Fig. 3.10 Schematic diagram of athermal MZI with different widths of waveguide arm

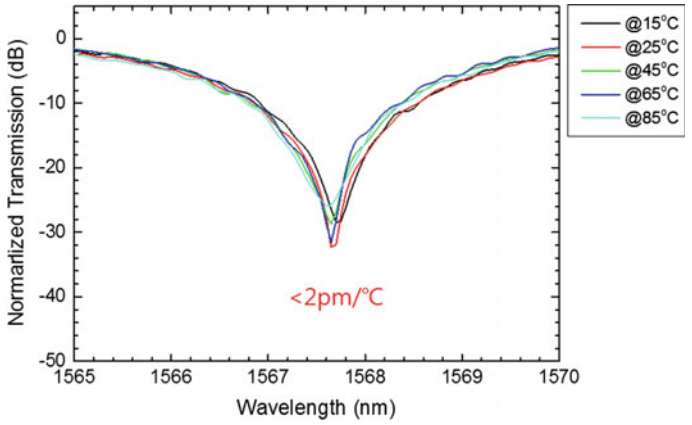

Fig. 3.11 Transmission spectra through athermal MZI when the temperature was varied from 15 to 85 °C

arms. B. Guha et al. showed TDWS of 5 pm/°C by a combination of 420 and 190 nm widths of 250-nm-thick silicon core.

Recently, J.-M. Lee et al. showed TDWS of 2 pm/°C as in Fig. 3.11, by a combination of 350 and 1000 nm widths of 220-nm-thick silicon core that was fabricated by standard CMOS fabrication process of using DUV lithography [28]. J.-M. Lee et al. also showed that the TDWS of the MZI can be negatively intensified to −340 pm/°C, when the MZI with the wide and narrow waveguide is covered by titania cladding [16]. These results show the possibility of fully CMOS compatible athermal MZI device, and we expect that the same principle can be applied to AWG by proper design of waveguide arms.

Using wide and narrow waveguide arms has been so successful in reducing TDWS of MZI but the method has been demonstrated only for MZI by now and it needs waveguide arm as long as several 100 μm for athermal condition.

3.6 Summary

We reviewed various approaches to overcome the high temperature-dependent wavelength shift of silicon photonic wavelength filters such as ring resonator, AWG, and MZI. There have been many results showing the possibility of athermal silicon photonic devices using a negative TO material such as polymer or titania to compensate the highly positive TO effect of silicon, but there remain problems in using the negative TO material. The polymer was not satisfactory in CMOS compatibility because of its low decomposition temperature, and titania is doubted in stability with the problem of hysteresis for the repetition of temperature going up and down. There have been other approach for MZI to use wide and narrow waveguide arms and successful in reducing TDWS of MZI, but the method has been demonstrated only for MZI by now and it needs waveguide arm as long as several 100 μm for athermal condition. So there is no perfect athermal technology yet, but we expect athermal technology suitable for the silicon photonics industry to be realized based on the recent results shown in this review.

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Chapter 4
Design Flow Automation for Silicon Photonics: Challenges, Collaboration, and Standardization

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Abstract Silicon photonics is nothing new. It has been around for decades, but in recent years, it has gained traction as electronic design challenges increase drastically with their atomic-level limitations. Silicon photonics has made significant advancements during this period, but there are many obstacles without an acceptable level of comfort as seen by the lack of semiconductor community involvement. Apart from a series of technological barriers, such as extreme fabrication sensitivity, inefficient light generation on-chip, etc., there are also certain design challenges. In this chapter, we will discuss the challenges and the opportunities in photonic integrated circuit design software tools, examine existing design flows for photonics

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design and how these fit different design styles, and review the activities in collaboration and standardization efforts to improve design flows.

4.1 Silicon Photonics—History Repeats Itself

Integrated photonics has been around for many years, and like the electronic semiconductor industry, it continues to evolve and change. Its progression is similar to electronics with a progression from discrete products assembled on a printed circuit board to more highly integrated circuits.

In the late 1970s and early 1980s, there was a significant shift in the electronics market in the designing of custom integrated circuits. The shift came in the form of the use and reuse of pre-characterized building blocks or "cells" as opposed to designing each transistor from scratch for each new chip. This technique later became known as "standard cells" or cell-based design, and it became the standard way used to build application-specific integrated circuits (ASICs).

At the same time, there was a major shift in the methodology used to design and verify integrated circuits (ICs). General-purpose computing and engineering workstations were becoming available to the engineering community in conjunction with the advent of computer-aided design (CAD) tools. Later, this turned into an entire industry now known as electronic design automation (EDA). Additionally, over the next several decades, hierarchical design and test methodologies [1] were codified, taught, and used to progressively enable scaling of IC design complexity from small-scale integration (SSI) to very large-scale integration (VLSI) and to what we now know as system on chip (SoCs).

Photonics is now in a similar state as to what the IC industry was in the early 1980s. There is a desire in the industry to integrate photonic components onto a common substrate and to bridge these photonics with their electrical counterparts monolithically either on the same die or on a separate die, but within the same package. Like the IC design in the early 1980s, there is now a need to codify design methodologies and to put into place the necessary industry ecosystems to support the scaling, both technical and economical, of integrated photonic design, manufacturing, and testing.

The good news for the industry is that engineers can leverage much of the infrastructure and learning that has gone into the electronics IC industry over the last 30 years.

4.2 Photonic Integrated Circuit Design Methodologies and Flows

Integrated photonic circuit design follows much the same design methodology and flows as traditional electrical analog circuit design. However, there is still a weakness in the photonic design process, and that is a successful circuit-like,

schematic capture, approach. Even today, many photonic engineering teams with considerable design expertise start from the layout. Unlike digital electrical design, it is not easy to abstract the circuit into simple logical gates synthesized from a high-level design language. Instead, the circuit is envisioned at the system level and usually modeled at that level with tools like MATLAB [2], C-coded models, Verilog-A [3], or scattering matrices. Once an engineer designs the high-level function, it is then up to the optics designer to partition the design and map it into photonic components realized in the integrated circuit. This mapping process is typically a manual task and involves many trade-offs based on the material and the fabrication facility to be used to manufacture the product. Eventually, the design is captured and simulated with physical effects of the material being taken into account. After the physical design is complete, the design is checked for manufacturing design rule compliance and then passed on to the fab in industry standard GDSII format to be manufactured.

4.2.1 Front End Versus Building Blocks Methodology

As with electronic design of the late 1970s, it is not uncommon for photonic designers to bypass logic capture and go straight to physical design of individual components. In many cases, each component is laid out and simulated with mode solvers and propagation simulators to ensure that the component's design meets the designer's intent. These steps repeat for each component and then the designer places and routes the entire circuit together and resimulates with a circuit simulator using compact models for the components derived from the physical simulations or measurements.

As explained in the introduction, many designers continue to start from layout (front end). But as the photonic circuit becomes larger and more complex, it becomes essential to start from the circuit or logic level (using photonic building blocks to construct a photonic circuit), where system specifications dictate how to build the circuitry. Specialization occurs: some photonic designers focus on the physical properties of single components (e.g., MMIs, waveguide bends, MZIs, splitters, rings, etc.) and perform physical simulations. Others concentrate on the logic level, where circuit simulations use compact models.

Circuit simulation is possible, because, different from RF design, the dimensions of most building blocks are larger than the wavelengths of interest. In most cases, this allows a logic separation of the building blocks. Optical waveguides are used to connect the building blocks, and act as a dispersive medium.

4.2.2 Process Design Kit Driven Design

It was at the end of the 1980s and in the early 1990s that integrated photonics research started to surface and become visible to a wider audience. Materials like

polymers, doped glass, and dielectric thin film materials like silicon oxide and nitride were dominant at that time. This new emerging field was called integrated optics, studying lightwave devices or planar lightwave circuits (PLC). As a result of these research activities, a need for proper design software emerged focusing on the simulation of mostly passive optical structures at the micrometer scale and the mask layout for the actual fabrication of the structures and devices. This was reflected in the start of an annual conference on Optical Waveguide Theory and Numerical Modeling (OWTNM) in 1992, and the first commercial activities for design services and simulation tools (BBV [today PhoeniX Software] in the Netherlands in 1991 and PhotonDesign in the United Kingdom in 1992).

As with electronic design moving into the 1980s, the optic design flow is now giving way to a more traditional flow as used by electrical analog design. Since the early 1990s, photonic IC design software has developed into what is available today; a set of more or less integrated solutions from a variety of vendors covering different levels in what is called the photonics design flow (PDF) or photonics design automation (PDA). The required software tools to create a full PDF or PDA include circuit simulators, mask layout tools, measurement databases, and design rule checkers. However, they also include physical modeling tools such as mode solvers and propagation simulators.

From the beginning, the designers in the field of integrated photonics have been working with a bottom-up approach, starting with the fabrication technology and materials and taking these as a starting point to develop integrated photonic devices. With the introduction of more standardized and generic fabrication processes since 2005 and the resulting creation of process design kits (PDKs, also called physical design kits) (see Sect. 4.5.3), a mixed design approach has evolved in which a group of designers develop the contents of the PDKs and a second group of designers use these PDKs in a top-down approach starting from the system or circuit level.

There are more fabrication facilities becoming available for complex photonic designs. The fab-provided PDKs contain documentation, rule "decks" for verification software, process information, technology files for software, a device library of basic devices (referred to as "PDK cells") that are validated by the process, and layout guidelines for designing custom devices (further referred to as "user cells"). These PDKs are developed and maintained by the fabrication facility and include plugins for commercial CAD tools. Depending on the application or completeness of the foundry PDK, photonic designs make heavy (like digital IC design) or light use (like analog IC design) of PDK cells vis-à-vis user cells. Nevertheless, compared to the digital IC design flow, fabrication facility-provided photonic PDKs today address few aspects of a complete design flow and contain a limited device library.

Once a designer chooses a technology platform, they are required to obtain the PDK for that technology, which gives the designer everything needed for the physical design of the chip, including custom device design. For example, each technology will specify a recommended typical and minimum bend radius for the waveguides (below which the bend will lead to sizable waveguide loss). Alternatively, process tolerance information like the maximum width deviation of the waveguide core can be ±1 nm. The designer needs to take all these rules and

guidelines into account when laying out custom cells. On the other hand, the library of validated cells allows for top-down design. Compact models enable the designer to make the connection between the higher level circuit design and the devices available in the technology of interest, without needing to resort to electromagnetic or device simulation.

Photonic PDKs contain various cells and templates, proven to work for a certain wavelength. Here are a few examples:

- [fixed cell] A grating coupler, used to couple light from an optical fiber (vertically) in/out of the chip. Different cells may exist with each designed and tested for various wavelength ranges.
- [fixed cell] A 3 dB splitter, used to split input light into two channels (50 %/50 %).
- [templates] Waveguide templates, which specify the cross section of a waveguide (i.e., thickness of the core and slab region), typically designed to offer minimal loss.
- [fixed cell] A high-speed PN junction-based MZI modulator.
- [custom cell] Typical custom cells are introducing filtering and processing of the optical signals. A widely applied custom cell or parametrized photonic building block is the arrayed waveguide grating (AWG). This AWG, in fact, acts as a MUX or DEMUX and can contain up to hundreds of waveguide sections.

The PDK-supplied rule decks for DRC and LVS enable the designer to verify his design against design rules and ensure consistency between schematic and layout prior to sending the design to the fab.

Several key items in the above description are still under active development. In particular, today's silicon photonic PDKs most often lack compact models for devices and, while LVS for photonics is still being developed, a few early rule decks do exist.

In conclusion, PDKs allow the user to carry out the physical implementation of the design, based on building blocks made available by the fab combined with custom designed cells based on given design rules.

4.2.3 Overview of Flow—Comparison to Analog Design Flow

With the advent of predefined photonic components and multiple foundries, the design flow and the methodologies used to create photonic integrated circuits (PICs) become directly analogous to electrical analog design. The foundry collects the predefined components into a PDK that is developed and maintained for each of their supported photonic processes. Once a PDK is installed the photonics designer can select from the PDK cells and instantiate and place their multiple copies, adjust their parameters when provided, and then connect them together with waveguides. As designs become more complex, the PIC designer can employ the use of

hierarchy, which allows for the copy and reuse of blocks or "cells" of connected custom components with well-defined interfaces, throughout a design. These user cells can be documented and stored for reuse by other designers. In the electrical design world, this collection of cells is typically called a library. A PDK is a distinct type of library as it is a set of programmable cells (pcells) that come directly from the foundry and are already pre-characterized.

Furthermore, designers are now working with more third-party foundries to make predefined and characterized components available, best tuned for the selected foundry process. Unlike digital design, these components are not static but instead are parameterized to allow the optics designer to be able to dial-in certain parameters to meet design requirements. Once the parameters are set, the programmable device autogenerates the component layout along with a compact model used for circuit-level simulation. As with electrical analog design, these programmable components also check for valid ranges of input parameters for which the compact models will be valid. The idea is to use as many of these predefined components as possible to reduce risk and time required to create the detailed, yet fab-compliant, layouts and fab-qualified models. Such libraries are being developed with photonics designers or CAD tool vendors in collaboration with the fab.

4.2.3.1 Schematic-Driven Layout

With the increase in complexity, many designers wish to capture their circuit at the logic level before spending a considerable amount of time creating layout. This desire is directly analogous to analog design in the electrical world. Instead of jumping right to layout after system design, the designer captures the design in a schematic abstraction of the circuit. The symbols used in the schematic have a direct one-for-one relationship with the programmable components used during layout. The CAD flow automatically makes a connection between the logic symbols and the correct compact models for circuit simulation. The symbols are placed and connected together with abstractions for the waveguides, ideal parameters are set on the components and waveguides in the schematic, and then the circuit is simulated. The designer iterates on the design, changing parameters on components, adding or removing components, and resimulating until all design objectives are met.

The benefit of using the abstracted level of the design at this stage, is that it allows the designer to focus on getting the circuit to function as desired without getting bogged down in the details of layout design rules, layout placement, and shaping of individual waveguides that can be very time-consuming. The idea is to avoid spending too much time crafting placements and waveguides only to find out that the basic circuit still is not functioning.

Once the PIC designer is satisfied that the design is converging, the layout process can begin. Electrical designers have learned over the years that it is best to use a methodology known as schematic-driven layout (SDL). SDL employs a correct-by-construction (CBC) methodology whereby the CAD tools do not allow

the designer to layout and connect up something that does not match the connectivity of the schematic design.

SDL also ensures that all parameters used during the schematic design get used for the correct generation of the programmable components, so there are no surprises caused by accidentally using the wrong parameters on the optical layout components. At this stage, we want the designer focused on the best possible placement of the components that allows for straightforward connections by the necessary waveguides and avoiding interference between multiple neighboring components.

Since the designer must work in a confined 2-D environment, there will most likely be some parameters or constraints that were forward annotated from the schematics to the layout that cannot physically be met; these could be, for example, nonverified user cells. When this happens the CAD flows must allow the designer to adjust parameters in the layout and then back-annotate these changes into a view of the schematic that can be resimulated.

4.2.3.2 Design for Test and Manufacturability

At the current stage of integrated photonics, the concepts of design for test (DFT) and design for manufacturing (DFM) have not been well addressed. Most fabrication facilities have limited DFT sites to test the functionality of PDK cells for wafer qualification. As silicon photonic circuit design complexity increases, netlist-driven automated DFT site generation will be increasingly important. DFT development will follow a mature SDL environment. DFM in silicon photonics today consists only of basic design verification comprising rules for shapes of polygons within a process layer (width, space, diameter, etc.), and rules for inter-process layer alignments (overlaps, enclosures, etc.). The current DFM maturity is only sufficient for checking the manufacturability of the design but not its yield, functionality, or reliability. (In commercial manufacturing sites, mainly PLC and InP, these things are in place.)

Like electronic design, the design specialty field of DFT and DFM for integrated photonics will eventually be required, especially as the design complexity for integrated photonics continues to grow. DFM will be of particular interest to photonic designers, as subtle changes in the process can have dramatic effects on the performance and functionality of photonic components. As the integrated photonics industry matures, additional work to characterize areas of yield loss will be required, and methods will need to be created for optics designers to design in such a way for the designs to be robust to process variations.

4.2.3.3 Design Sensitivity

For interferometric devices, the phase relationship between two waveguide paths determines the overall behavior of the device; examples include ring resonators,

Mach–Zehnder interferometers, and so on. This behavior is quite comparable to RF design, where the exact wire length and shape largely affect the overall behavior.

Even more so, the fabrication tolerances are very strict. A 1 nm change in waveguide width can cause a 1 nm shift in filter response [4]. A 1 nm shift, at a wavelength of 1.55 μm, corresponds to a frequency shift of 125 GHz, which is sufficient to span more than one channel in a typical wavelength division multiplexing (WDM) device. The same holds for temperature changes: a temperature change of roughly 12 K corresponds to the same 1 nm shift [5].

For this reason, smart designs can be made that compensate for design tolerances [6], which are a real challenge for designing photonic chips that contain interferometric devices. Good control over the waveguides line shape in the technology process, together with clever engineering, can reduce the risks for not obtaining the targeted specifications. For more information, see Sect. 4.3.1 on silicon photonics fabrication processes.

4.2.4 Schematic Capture

A schematic is an abstracted view of the circuit at the logic level. The objects placed in the schematic can come directly from a foundry PDK or could be symbols created by the designer that represent more levels of design hierarchy. Schematics serve many purposes. They are used to capture the implemented logic, as well as design intent. Design intent can be in many forms, but the most common are simple textual notes that record the designer's assumptions. Designers also annotate their schematics with instructions for how the associated layout should handle various components. In both electrical and photonic domains, designers annotate parameters on the instances of schematic components that use both the simulation and the layout of the actual component.

More advanced schematic capture packages also allow the designer to represent repeated structures in very compact forms like buses and "for loops" that contain circuit components. Schematics are meant to be printed, and when circuits get too large they cannot be represented on one schematic. There are special annotations that allow the designer to continue the design on more pages of the same schematic hierarchy. Similarly, there are conventions that can be used to simplify the schematic drawing so that referencing connections is made between components on opposite sides of the schematic by name instead of having to route a line between them. The idea here is to make capture of the logic accessible so that the designer can get to simulation and debug of the circuit behavior quickly—the less drawing and more debugging, the better. To deal with hierarchy, the CAD tools make use of the concept of pins and ports on components as a way for the software to keep track of connections between levels of hierarchy and connections from page-to-page. At a given level of the hierarchy, "ports" are defined as the interface for the cell being designed. Once the cell is complete, the CAD tools have automated ways to create an abstracted symbol for the cell. The symbols have "pins" which are connection

points for the symbol. There is a one-for-one correspondence for ports in the schematic for each pin on the symbol. Typically, these associations are done by name on the port and associated pin. A newly created symbol for a schematic placed in a library, instantiated, and then used in other levels of the design hierarchy, helps the user to abstract the design at any level of hierarchy to something that is meaningful to anyone else who reads the schematic.

4.2.4.1 Interface to Simulation and Analysis

In both the electronic and photonic domains, designers employ circuit simulators to verify and debug the function of their designs. The schematic serves as a way to capture the circuit in a form that the simulator can use through steps known as elaboration and netlisting. A netlist is a non-graphical representation (and typically human readable) of the connectivity of the design. Netlists can be hierarchical or flat and typically carry the property information needed by downstream tools like simulators and layout generators. Elaboration is the step that unwinds the higher levels of abstraction into specific instances that will be simulated and generated in the layout. An example of this in electronic design is when the designer uses something called a multiplier factor parameter or "M factor" parameter [7]. A transistor symbol, with an *M* factor of 4, means that the designer will actually get four transistors for the one abstracted symbol in the schematic. Each of these four transistors connects in parallel, and each will have the same properties as assigned to the symbol on the schematic. The elaboration step expands the one transistor into four in the netlist and makes sure that all of the appropriate properties are on each of the new instances.

In addition to the netlist, simulators also need a variety of inputs from the user. This would include things like identification of circuit input and output terminals for the simulation, identification of signals that the designer wishes to monitor for viewing in a waveform viewer, and other analysis points on the circuit that the user may want the simulator to monitor and output for debug purposes. The user interface for this is typically integrated with the schematic to make it easy for the designer to identify graphically nodes of the circuit as opposed to having to type in terminal names. The CAD tools also have graphical interfaces to allow the designers to map the symbols to different levels of simulation models allowing for mixed-level simulations. Not all simulators are capable of this, so the CAD tools typically have dialog boxes that are unique to the chosen simulator. This user interface allows the designer to use the same schematic capture system for high-level systems design, circuit design, and mixed mode simulations where parts of the circuit are still at behavioral levels while other areas of the circuit are at the component level.

In more advanced design flows, the netlister and elaborator are also responsible for forward annotating constraints captured by the designer in the schematic on to the layout generation tools. The netlister and elaborator take care of all of the internal connections that must be made between the different editing tools so that the designer can focus on design and not tool integration complexities.

4.2.4.2 Matching Simulation to Layout

A general methodology used by electrical designers is to design their analog circuit first as an ideal circuit. Ideally, in this case, it means that the designer debugs the circuit without taking into account the physical effects of component placement and the parasitics due to routing. In this case, the circuit is simpler in nature, and it should be easier to tune the design to get the desired response. The same is true in photonics design. Wires connect the major components in the schematic. These wires represent waveguides in the layout. The parameters of the abstracted components and waveguides are set by the designer in the schematic and then work using the simulator to bring the circuit to the desired behavior.

Once this step is close to completion, the designer then moves to layout. The idea here is that the parameters used in the ideal circuit are forward annotated to the layout system where a CBC layout methodology is used to try to meet the original assumptions of the designer. Presumably, if the designer can meet the original assumptions, then the post-layout simulations of the virtual layout should match the simulations of the idea circuit. Matching the original circuit simulation and post-layout simulation can be challenging, and this is especially true for photonics. In photonics, this is because the phase has to be controlled precisely (e.g., in Mach–Zehnder interferometers, ring resonators, etc.). Phase is a function of the topology and materials of the components and waveguides, and the designer is not yet aware of these at schematic capture time. The CBC methodology proposes that the phase relationships are passed on to the layout tools, which would then try to construct the components and waveguides in such a way that the phase relationships are maintained. Depending on the overall circuit, this may not be possible. In which case, some of the parameters on the components and waveguides will need to be changed to accommodate the physical constraints of the area allowed for the layout. When this happens, the CAD tools must have a mechanism to back-annotate and merge the changed parameters of the layout with the original parameters of the ideal design. This data is stored as a revision of the netlist so that the original ideal circuit description is not lost. The revised netlist can then run against the same simulation test benches used to debug and characterize the ideal circuit. A designer then compares the results between the ideal circuit and the virtual layout and any issues caused by the changes must then be resolved either by changing the layout or by changing the logic circuit to be more robust to the physical effects and ultimately reiterating the design.

4.2.5 Photonic Circuit Modeling

Numerical modeling is an essential part of any modern circuit design, whether electrical or photonic. A designer performs simulations to optimize the circuit and ensure that it will meet its performance requirements. Also, circuit simulation can provide information on circuit yield if the effects of realistic manufacturing

imperfections can be correctly taken into account, allowing the designer to optimize the circuit for manufacturability. The key requirement of circuit simulation is that it must be predictive, or in other words, that the results of the circuit simulation agree to sufficient accuracy with the actual circuit performance after manufacturing.

4.2.5.1 Electronic Simulations Using SPICE

For electronic circuits, SPICE is the de facto standard for simulating resistors, capacitors, and inductors (RLC circuits) better known as linear electrical circuits. Moreover, there are many methods for modeling nonlinear devices, such as diodes and transistors, by linearizing them around operating points. A SPICE tool can then simulate the small-signal frequency domain or (transient) time domain behavior of the circuit. On a higher level of abstraction, Verilog-A can be used to describe the input–output relationship of an arbitrary component and, at the system level, IBIS can be used for modeling communication links with SerDes devices [8]. Advanced simulation strategies can then seamlessly interpret all this information and perform a coherent simulation.

4.2.5.2 Electronic Versus Photonic Simulation

Similar to electronic circuit simulation, photonic circuit simulation commonly requires both transient and scattering data analysis to model signal propagation within the time and frequency domain. Therefore, one approach has been to reuse circuit simulation algorithms originally designed for the simulation of electrical circuits such as SPICE [9]. However, as photonic circuits are physically described using wave phenomena, it is not straightforward to map this onto an SPICE-like formalism, which assumes that the wavelength of the information carrier is much larger than the size of the components and can be treated as lumped elements. Typical photonic circuits exist of several building blocks, which themselves are often larger than the signal wavelengths: the signal wavelengths are in the visible to near-infrared (i.e., 700 nm–10 μm, with 1.3 μm, and 1.55 μm the most commonly used wavelength bands for data and telecom applications). In contrast, individual building blocks can be of the size of $\sim$10–1000 μm^2, depending on the technology.

Unlike electrical circuit simulators, photonic circuit simulators must take into account the complex nature of light that includes the optical signal's polarization, phase, and wavelength. The optical simulation and analysis of PICs is particularly challenging because it involves bidirectional, multichannel, and even multimode propagation of light and waveguide connections between consecutive components require specialized treatment unlike that done for electrical traces [10]. In addition, photonic circuit components often involve both electrical and optical signals, and there is still little standardization for how to perform the necessary, mixed-signal simulations in the time domain. Lasers, modulators, couplers, filters, and detectors are just a few of the different components present in a complete PIC. Each of these

components has different operation principles that are highly dependent upon the particular process, technology, and physical geometry. Photonic circuit simulators, therefore, must rely on proper compact models, calibrated for a particular foundry process, which accurately represent the optical and electrical responses of these components in the time and frequency domains.

4.2.5.3 Photonic Circuit Simulation

Photonic building blocks or components are linked using waveguides that guide optical signals. They are represented as a delay line, adding delay and phase to the signal. To complicate matters: both the group delay and the phase delay can be very dependent on the signal wavelength, and multiple wavelength carriers can be used simultaneously in the same waveguide circuit.

In a photonic circuit simulation, each component (including waveguides) is represented by a black box model with input and output ports and a linear or nonlinear model describes the relationship between the ports. The larger photonic circuit contains the collection of these building blocks, connected at the ports, with a given connection topology. These connections are purely logical (Figs. 4.1, 4.2, 4.3 and 4.4).

Designers implement the building block model description in different ways: purely linear, frequency domain based, or a more complex description for time domain and/or nonlinear interaction. For the linear part, matrix formalism can be used. The two most commonly used formats are

(1) Transfer-matrix methods: in this case, the assumption is made that there is a set of input and a set of output ports. The output ports of component 1 cascade to the input ports of component 2. This method is simple and easy to understand (and can be easily implemented, e.g., in MATLAB or Python), but it has the drawback that no reflections or feedback loops are possible.

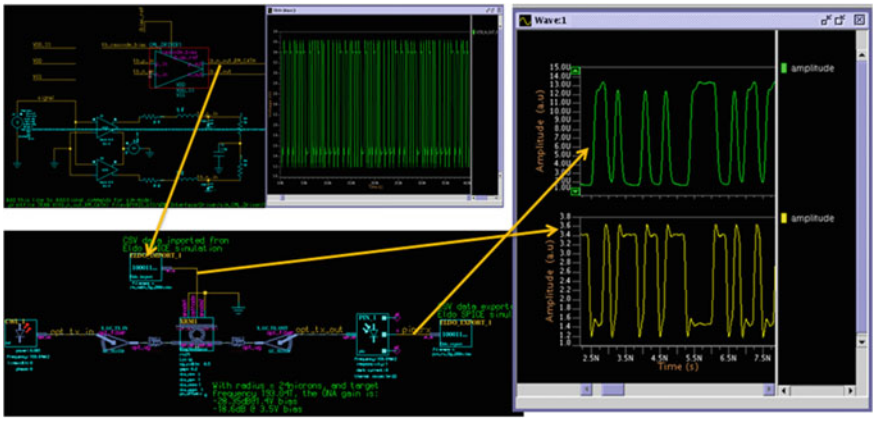


Fig. 4.1 Multiple schematic views of simulations

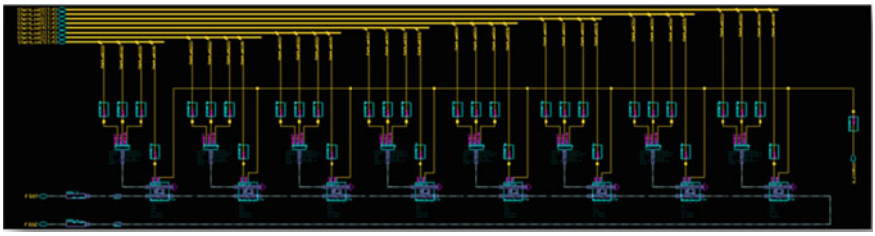


Fig. 4.2 Detailed layout placement of a design

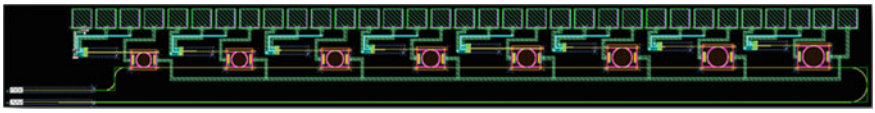


Fig. 4.3 Schematic-driven layout ensuring a correct-by-construction layout

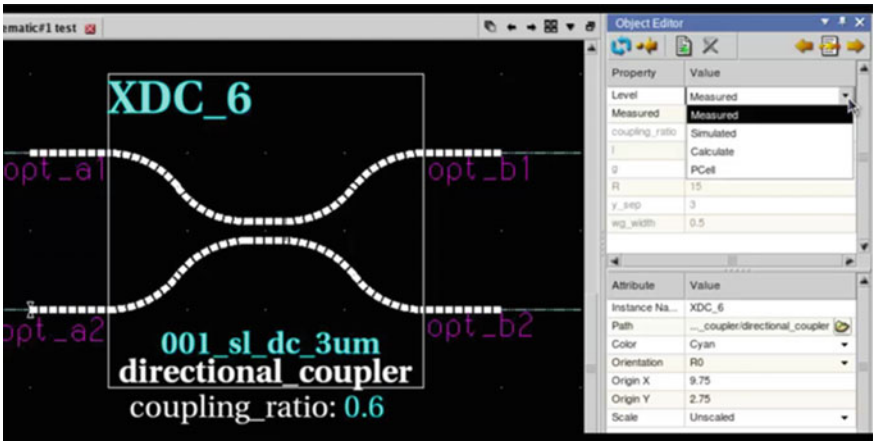


Fig. 4.4 Example of photonic pcell—elaboration passes appropriate parameters to simulation and layout

(2) Scattering matrix methods (see Fig. 4.5): here, reflections and feedback loops can be taken into account. As most photonic circuitry will contain these two effects, it will lead to a more accurate result. For complex circuitry, it quickly becomes beneficial to adopt the scatter matrix formalism. A mathematical description of how to calculate the system response based on individual scattering matrices can be found in [11].

Time domain models that take nonlinearities into account can augment both methods. The main advantage of this approach is the natural representation of variables such as temperature, carriers (e.g., the plasma dispersion effect), and

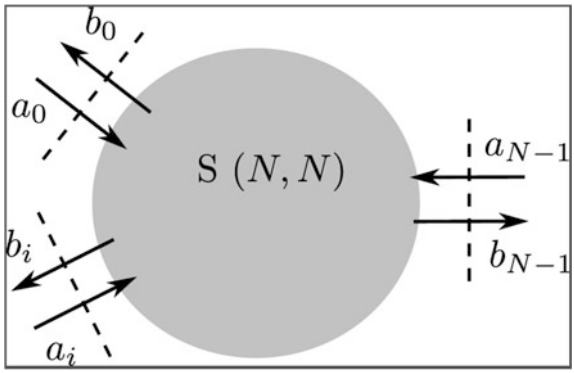


Fig. 4.5 A *N*-port linear component can be represented by an (*N*, *N*) scatter matrix **S**. The input signals (represented by the input vector **a**) are related to the output (represented by the vector **b**) using the following equation: **b = S a**

resonator energy (for coupled mode theory models), making it simpler to interpret these models.

When combining photonic circuits with electronic circuits, it is not trivial to balance the two different simulation strategies. One approach is to reduce the photonic model to a description that a designer can implement into Verilog-A then simulate using an electronics simulator. This approach requires that some photonic quantities, such as optical power and phase, map into native Verilog-A variables. Also, more elaborate information of the photonic model, such as multiwavelength behavior, polarization, etc., are not taken into account, or need to be simulated as a parameter sweep. Such a compact model can work well in a small operation region (i.e., for a fixed wavelength, temperature, and voltage). As long as this model satisfies the need for a particular application (e.g., single-wavelength optical interconnects), this approach can be used for the co-simulation of photonics and electronics. The challenge is to find a good compact model that is valid over the operation region of the circuit. This simulation strategy has the lowest threshold for electronic engineers engaging in the field of photonics and has some limitations as described.

It is worth noting that while some electrical simulators support scatter matrices (which can map onto an RLC circuit), the shape of the response will determine accuracy. Moreover, nonlinearity/reflections are not easy to model accurately.

4.2.5.4 Frequency Domain Analysis

Frequency domain analysis is performed using the same type of scattering analysis used in the high-frequency electrical domain for solving microwave circuits, enabling bidirectional signals to be accurately simulated [12]. This approach can be extended to allow for an arbitrary number of modes in the waveguide with possible

coupling between those modes that can occur in any element. Consequently, the scattering matrix of a given element describes both the relationship between its input and output ports and the relationship between its input and output modes. The advantage of frequency domain analysis is that it is relatively standardized. The so-called S-matrices for each component (including possible coupling between modes on the same waveguide ports) are all that is required to perform a frequency domain simulation of the circuit. However, the frequency domain simulation, while very valuable for a broad range of design challenges, is insufficient for most circuits and systems that make use of active components, which require the simulation of both electrical and optical signals.

4.2.5.5 Time Domain Analysis

Unlike frequency domain analysis, there is little standardization in time domain analysis. For time domain analysis, it is necessary to represent multichannel signals in multimode waveguides with bidirectional propagation. These waveguide modes must not limit polarization states to only two, which are a clear distinction, compared to many fiber-optical systems. Also, there must be the ability to support both electrical and digital waveforms since, for example, an electro-optical modulator must take both electrical and optical inputs to produce a modulated optical output.

One approach is to use a dynamic data flow simulator. When a simulation runs, data flows from the output port of one element to one or more input ports of one or more connected elements. When an element receives data, its compact model applies the element's behavior to the data and generates the appropriate output. In the time domain simulation, data can be represented as a stream of samples where each sample represents the value of the signal, either optically, electrically or even digitally, at a particular point in time. This approach has the flexibility to represent different element behaviors and signal types, which enables the development of compact models that can comprehensively address the variety of active and nonlinear optoelectronic devices present in photonic integrated circuits.

This type of simulation approach used in combination with electrical circuit simulation methods such as SPICE is the simplest method to run separate electrical and optical simulations, and exchange waveforms between them, and this approach has been demonstrated successfully [13]. In the future, it will likely be necessary to extend this to a full co-simulation approach whereby the photonic circuit simulation runs in a larger scale electronic simulation.

The time domain signal integrity analysis of a circuit under test is performed by analyzing the input or output signal at different ports, which may be electrical, optical, or digital. A typical result from a time domain simulation is the eye diagram, as shown in Fig. 4.6. The analysis of the eye diagram offers insight into the nature of the circuit imperfections. The time domain simulation can calculate the eye diagrams, and the resulting analysis can determine key signal integrity parameters such as bit error rate (BER), optimum threshold and decision instant, and extinction ratio. As increasingly complex modulation formats become more

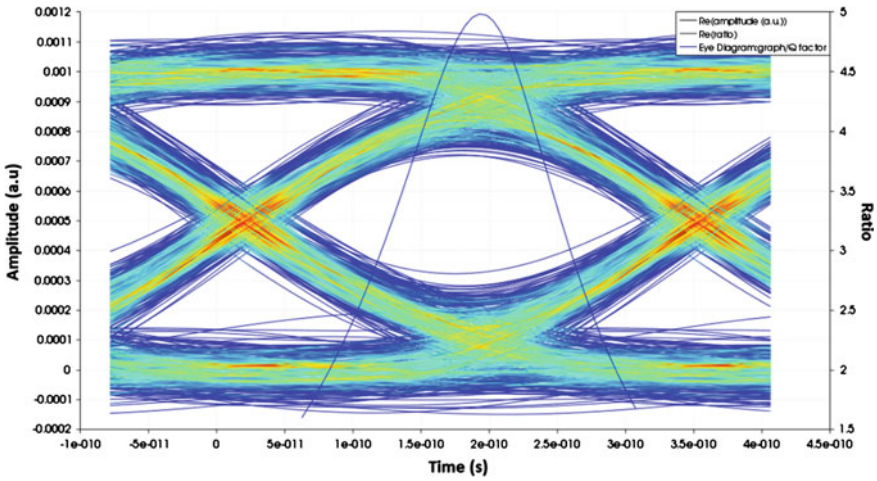


Fig. 4.6 The eye diagram resulting from a simulation of an optical transceiver

widespread, such as quadrature phase-shift keying (QPSK), calculating constellation diagrams will produce the best signal integrity analysis. An example of the eye diagram and constellation diagram from a simulation of an optical QPSK with electrical 16-QAM (quadrature amplitude modulator) system is shown in Fig. 4.8 as part of an example circuit.

4.2.6 Model Extraction for Compact Models

The compact models required for PICS modeling must be generated using a combination of experimental results and accurate optical and electrical physical simulation. If the optical component is passive and linear, it suffices to provide a scattering matrix (typically wavelength dependent). Devices with dynamical behavior will need more complex models (e.g., an optical phase modulator will require the electrical voltage over the p(i)n diode as additional input).

In the case of passive components, the scattering matrix can be obtained by performing a full physical simulation (e.g., finite-difference time domain [FDTD]). Previously, fabricated components can be measured to obtain a wavelength-dependent spectrum.

From the given spectrum, compact models can be made that represent the original component, within a given accuracy. Measurement noise has to be eliminated in order to create a useful model in cases where a designer obtains the spectrum from a measurement. Passivity and reciprocity are essential properties of the model obtained.

One example of creating these models is the vector fitting method [14]. With this method, an arbitrary S-matrix is approximated with a set of poles and zeros. Some

challenges with this method are to find a good filter order and to cope with non-symmetry of the optical filters due to dispersion.

A second example is to model scattering matrices using FIR filters, which have more degrees of freedom than IIR filters, but are computationally more demanding to execute. In the case of active components, the model, characterization, and parameter extraction need to be tailored for each component. For example, an optical laser can be described using rate equations [15]. Optical phase modulators have a voltage-dependent transmission, described as a series of steady-state, voltage-dependent scattering matrices, or with a more dynamical model, where the transmission is dependent on the number of free carriers in the p(i)n junction, and an ordinary differential equation (ODE) simulates the number of free carriers. All of these methods are vital when building robust PDKs (see Sect. 4.2.2).

4.2.6.1 Methods and Challenges

Waveguides are an excellent example of components that require a combination of simulated and experimental data. A mode solver, knowing the cross-sectional geometry, can generate the effective index, group index, and dispersion. It is possible to calculate the dependence of these quantities on geometric changes such as waveguide width and height, as well as external influences such as temperature, electrical fields, or mechanical stress. However, the waveguide loss, in a well-designed geometry, comes primarily from sidewall roughness. While it is possible to simulate these losses if enough information on the roughness measurements of surfaces (RMS) and correlation length is known, in practice, it is much easier to use experimental waveguide loss results when creating the compact model.

4.2.6.2 Model Extraction from Physical Simulations

Similarly, the majority of passive component compact models can be calibrated using a combination of simulation results and experimental data. For example, when creating a compact model for a splitter, the insertion loss (IL) may come directly from the experimental data. However, even well-designed splitters have a small but nonnegligible reflection that is challenging to measure directly. In this case, a simulation of the design can provide the reflection and the phase of the S-parameters while confirming the experimental IL data. As with waveguides, the simulation can provide sensitivity analysis, such as the dependence of parameters on waveguide thickness, which may be challenging to obtain experimentally.

4.2.6.3 Compact Models in the Time Domain

Compact models for electro-optical modulators for time domain simulations are much more challenging. To simulate a Mach–Zehnder modulator requires, at a

minimum, the waveguide effective index and loss as a function of bias voltage calculated by a combination of electrical and optical simulations, where the electrical simulations must be calibrated against experimental data such as the capacitance versus voltage curve. Excellent agreement with experimental results with a DC bias can be obtained [16] once calibrated, as well as with the spectral response under different bias conditions [17].

For time domain simulations, the compact model must be able to respond to time-varying electrical and optical stimuli. When driven at higher frequencies, the Mach–Zehnder modulators frequently have complex effects that must be accounted for, such as: impedance mismatches of the transmission line and the feeds; improper termination of the transmission line; and velocity mismatches of the transmission line and the optical waveguide. To accurately simulate a modulator driven by an electrical bit sequence that contains frequencies from DC to 10s of GHz and beyond, it is necessary to calibrate carefully the models to account for these effects.

The photodetector responsivity versus bias voltage is often measured experimentally under continuous-wave (CW) illumination, and this data can be used to create the compact model. The high-frequency behavior can be recreated using a filter with parameters calibrating against experimental data. Similarly, the dark current is often measured experimentally. The temperature dependence of these quantities can be obtained experimentally if available, or it is simulated with a combination of optical and electrical solvers.

4.2.6.4 Photonic Circuit Modeling Examples

A typical circuit analyzed in the frequency domain is an optical switch [18, 19]. These circuits can include hundreds of components due to all the waveguide crossings that are required. An example circuit diagram is shown in Fig. 4.7, which also makes it clear that the larger the number of elements, the more necessary the circuit hierarchy becomes.

The entire circuit is displayed together with a zoomed view of a portion of the circuit including the optical network analyzer. Also shown, is the inside of a subcircuit element that includes a large number of waveguide crossings. The entire circuit contains hundreds of elements. Nevertheless, the results of the optical network analyzer can be calculated in less than a minute over a typical range of frequencies.

In the time domain, a typical circuit to simulate is a transceiver [20]. In Fig. 4.8, a 16-QAM transmitter is shown along with the resulting eye and constellation diagrams.

4.2.7 Schematic-Driven Layout

In photonics, historically most emphasis has been on the full-custom layout of the individual components and combining these into (simple) circuits. Today, with the

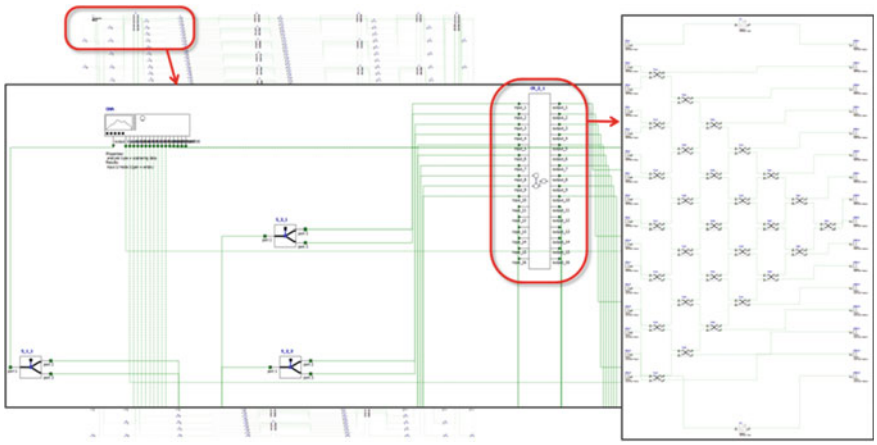


Fig. 4.7 Circuit diagram for an optical switch

increasing complexity of the circuits the mask layout ideally should be generated from the schematic, as created with a circuit design tool.

Schematic-driven layout (SDL) is a methodology and design flow whereby the layout tool continually checks the connectivity of the layout against the connectivity of the elaborated netlist. If the designer tries to connect up something in the layout that is not in the elaborated netlist, the CAD tool will flag the issue to the designer. In some companies, policies are put in place whereby the CAD tool is set up to not allow changes to the connectivity within in the layout tool. The schematic must include any connectivity changes which forces the designer to remember to rerun simulation verification on the new netlist. Other companies find this too restrictive and allow for design connectivity changes made directly in the layout. This practice, however, should be discouraged, as it is very difficult to back-annotate design changes from the layout to the schematic. It should also be noted that since CAD tools can be set up to allow for different change scenarios, SDL should not be relied upon as the last check before manufacturing to ensure the circuit layout is connected up. It is the responsibility of the designer to both resimulate the design and to run physical verification tools that perform a more exhaustive check of all layout versus schematic connectivity.

In addition to checking connectivity, the SDL flow is also responsible for setting parameters of any programmable layout cells (pcells) forward annotated from the schematics. It should be noted, at this point, that the hierarchy of the layout does not need to match the hierarchy of the schematic. If this is the case, the CAD tool is responsible for all name and parameter mappings between the two hierarchies. CAD tools that handle this methodology typically have a hierarchy browser that lets the designer cross-probe between the schematic and the layout views even when the hierarchies of the two views are different.

The benefit of using an SDL-based design methodology becomes clear when design sizes increase, especially when a team of designers is working on a project

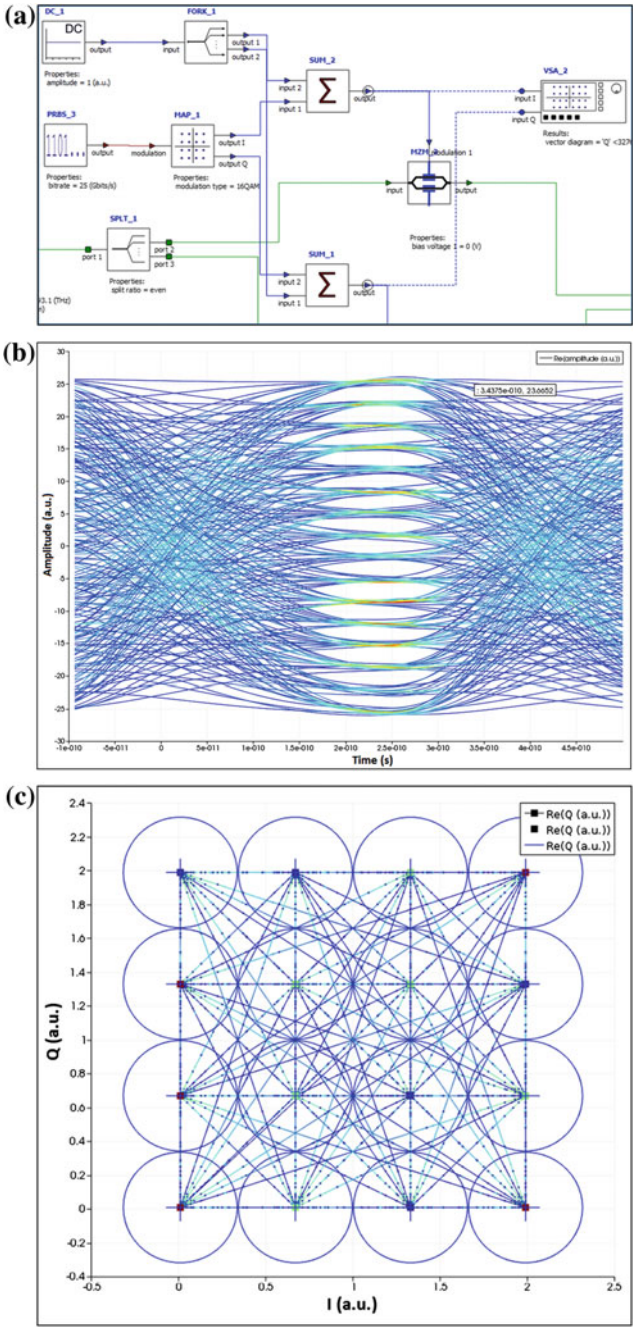


Fig. 4.8 A circuit diagram for an optical QPSK with an electrical 16-QAM system is shown in (**a**). The resulting eye diagram is shown in (**b**), and the constellation diagram is shown in (**c**). Elements of the displayed circuit diagram are themselves subcircuits, which contain a number of elements

as opposed to a single designer. Different people usually do circuit design and layout design. Using SDL ensures accurately communicated design connectivity between the schematic and layout stages. A second benefit of using an SDL-based flow is that last minute design changes can be tracked by the CAD system to ensure that the changes made in the layout are, in fact, the same changes that are in the schematic. The CAD tool will flag the differences it sees in the layout versus the newly updated schematic.

CAD tools ensure that connectivity is correctly preserved in the layout tool using the SDL-based flow that enables the use of more advanced constraint-driven layout engines such as pcells, auto-placement, and autorouting.

The SDL strategy is well developed in electronics, using semiautomated algorithms for placing "functional pieces" and routing the connecting "wires". Electronic design is very suitable for this since, in most designs, the wires can be considered as "just a connection" and they do not influence the overall design, for example, due to increased delay times. For many low(er) speed applications, the electric wires on the chip are just a low-loss way to transmit signals. Therefore, the placement of the functional parts with nonoverlapping wires between the different pieces is a purely geometrical problem. This simple concept requirement is frequently solved using autorouting approaches of the wires, where the paths are typically vertical or horizontal (Manhattan) routing patterns. Nowadays, routing at angles other than 90° is sometimes also supported, but then at only a few fixed angles, like 30°, 45°, and 60° only.

For high-speed (RF) tracks, analog design, and high-speed (>10 GHz) digital designs these assumptions are no longer valid as the transmission losses can become considerable and both impedance mismatches, voltage drops over the wire, and timing delays are becoming crucial as in photonic designs. For photonics, the "wires" are in most cases, not just simple connections. The physical properties are starting to play a role or are even determining the functionality of a component or the whole photonic circuit. Therefore, the connecting "wires" between building blocks or components are called "waveguides," because the purpose of the connection is to guide an electromagnetic wave from one place to another. Remember that the telecom C band comprises infrared wavelengths around 1550 nm, corresponding to a frequency of 193 THz. Quite often, the functional pieces themselves consist mainly of waveguides and/or waveguiding structures with very specific requirements for individual waveguides or combinations of waveguides. These detailed requirements can fluctuate from a very precise control over the length and width or length and width differences and even mathematically defined varying widths along the length of a waveguide (so-called tapering). These fluctuations are also why a proper translation of the actual design intent for the waveguide structures into the final discretized mask file (GDSII) is paramount, avoiding gridding and rounding errors.

Based on these boundary conditions, it is easily understood that a mask layout tool for photonics has some unique requirements, not necessarily available in electronics mask layout tools. All angle capabilities, the ability to produce very smooth curves, and connectivity are the most important ones. Since the actual shape of the waveguides plays a dominant role, designers want to have full control over

these shapes and how these shapes connect. In 1992, the concept of parametric design was introduced for this purpose. Instead of drawing the shape, a designer sets some parameters and software will then translate this design intent into a set of geometric shapes like polygons.

Based on a library of predefined geometrical primitives, dedicated for integrated photonics, all required waveguide structures can be designed and used in larger structures or composite building blocks, like a Mach–Zehnder interferometer, an arrayed waveguide grating, and even full circuits. The crucial step of translating the "design intent" into the final "geometry" can be covered by manual coding in generic script languages, like Python, as used in Luceda's IPKISS [21], or Mentor Graphics' AMPLE [22], as applied in the Mentor Graphics®' Pyxis™ layout framework, used for the formulation of parametric cells. PhoeniX Software's OptoDesigner [23] provides domain-specific scripting capabilities also to the built-in photonics aware synthesizers as well as specific layout preparing functionalities, thus removing this translation burden from the designer.

4.2.7.1 Floorplanning

Floorplanning is a stage of layout whereby the layout designer partitions the layout space of the overall photonic die to accomplish several objectives. Some of these goals include allocating space for die interfaces that will match up to the packaging methodology of choice. As an example, a SiGe die with VCSEL lasers is flip chipped onto a silicon photonic substrate. The substrate floorplan must comprehend the location of the VCSELs to make sure the laser to grating interfaces work properly. Another objective is ensuring that adequate space exists for photonic components and their associated waveguides.

A challenge that is unique to photonics is that the waveguides that connect components are typically created using only one physical layer as opposed to electrical connections that may use many layers of metal interconnect. As the designer must ensure that there is adequate room to place the waveguides in a planar fashion, this makes the placement of components more challenging. Care must also be taken in the placement of components so that they do not interfere with each other in their function.

Connectivity of the individual parts of the waveguide structures, and the connections between the building blocks or components, is required to be able to make designs that contain multiple parts, without the need to manually adjust positions when there are additional changes to parts of the design. A good example of this is a Mach–Zehnder interferometer composite building block constructed of several photonics primitives like junctions, bends, and straights. These individual waveguide parts all have their parameters, depending on the actual waveguide shape or cross section, the wavelength of interest, and the phase difference that is required. These individual waveguide parameters relate strongly to the composite building block parameters often using fairly simple equations: for example, the path length of one branch of a Mach–Zehnder interferometer should be a precise amount longer

than the other branch. The waveguide materials, dimensions, and required filtering characteristics determine this length difference. When designing such a composite building block, it is very beneficial that all the individual smaller pieces stay connected when changes are made to the design based on simulation results or measurement data. The need for connectivity and the automatic translation of the design intent into the required layout instead of drawing or programming these complex polygons by hand is now well understood.

4.2.7.2 Routing

Waveguide routing is unique to photonics. As mentioned previously, waveguides typically only run on one physical layer. However, unlike electronic integrated circuits, it is possible to run many different wavelengths down the same waveguide. The concept of a bus becomes more like a highway on which multiple different types of cars can travel, as opposed to electronics, where a bus has dedicated lanes and can only be shared by multiplexing and demultiplexing in different signals. With photonics, multiple wavelengths and light modes can all share the same waveguide at the same time.

Waveguides are also unlike metal traces in electronic ICs because they can allow for intersections between waveguides on the same layer, which is analogous to an intersection on a highway. Care must be taken, however, as light from one direction will bleed into the other waveguides of the intersection, and the circuit must be able to handle this functionally.

Waveguides also play a very active role in the function of the photonic circuit. As mentioned previously, turns in waveguides are typically made with curvilinear shapes, not the orthogonal shapes used in electronic design. The number of turns, the radius of those turns and the width of the waveguide all affect the performance of the waveguide and the overall circuit. Once the waveguides have been routed all of these parameters for the resulting waveguide need to be back-annotated to the schematic for post-layout circuit verification using the photonics circuit simulator.

4.2.7.3 Specialty Design

Although integrated photonics is very similar to analog IC design, there are no libraries of photonics components that will meet the requirements of individual designer's application. Today, a typical PIC design contains more than 70 % custom design. Except for the provided IO modules (fiber chip couplers) and a photodiode or modulator, most of the design is entirely or partly customized. Moreover, even the above-mentioned example library components are tweaked or changed to meet the wavelength requirements for a particular application. As a result of this, designers need flexible tools to work with, being able to cope with the special requirements for photonics design. Especially at the layout level, a large variety of designs can be observed, creating functions that at the circuit level are

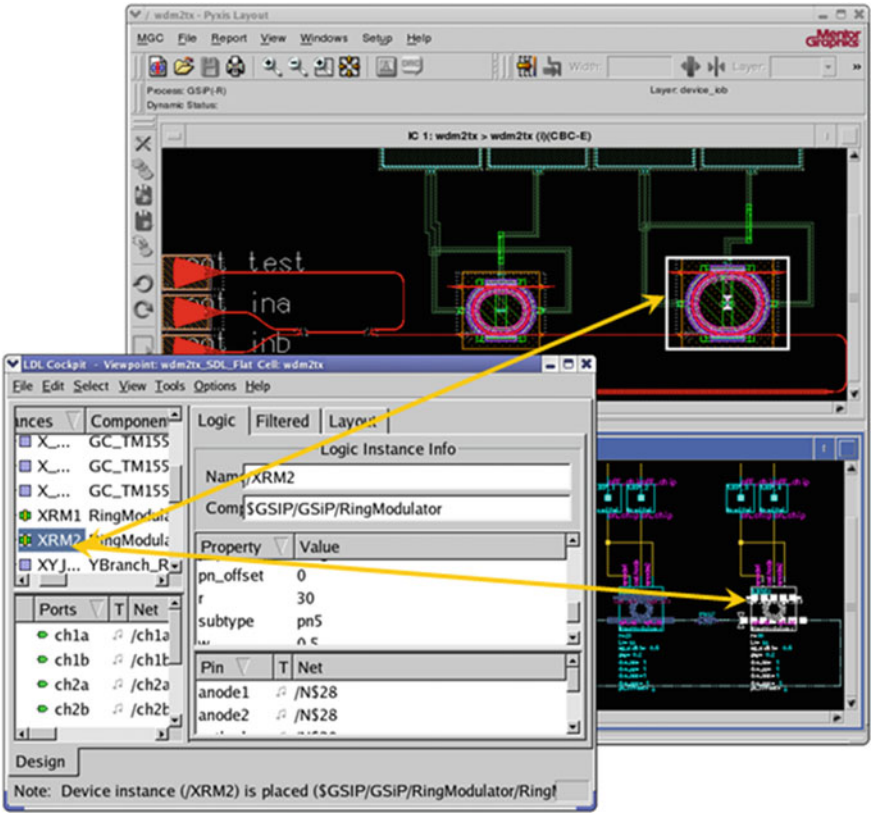


Fig. 4.9 Example of SDL-based cross-probing between schematic (*bottom*) and layout (*top*)

very similar. This large variety is a result of technology constraints (material properties, waveguide types, process variations, etc.) and the need to use the chip area as efficiently as possible. Phase relations create many photonic functions and therefore folding, bending, and/or rotating are widely used during the layout implementation (Figs. 4.9 and 4.10).

Figure 4.11 shows how photonics designers can automatically generate layout implementations after being given the required technology information and optically or geometrically defined photonics building blocks (PhoeniX Software's OptoDesigner).

4.2.8 *Overview of Physical Verification for Silicon Photonics*

As silicon photonics design migrates from research into commercial production, photonics designers must borrow some techniques from complementary metal–

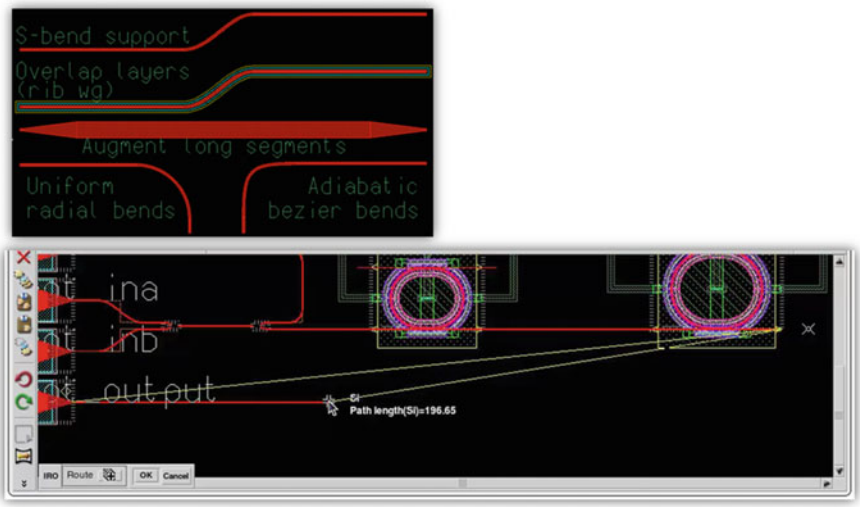


Fig. 4.10 Examples of curved waveguides used in photonics

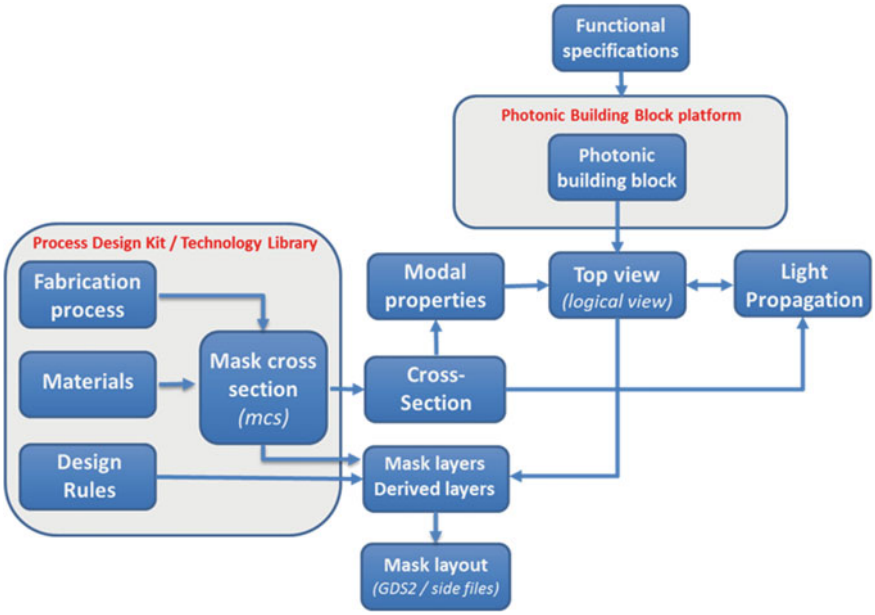


Fig. 4.11 Automatic module generation through "photonic synthesis"

oxide–semiconductor (CMOS) design in order to fully realize these benefits. One of the key challenges is to adapt existing IC design tools into an EDA design flow that is compatible with silicon photonics design characteristics [24]. Physical

Verification (PV) is one of the key components of the EDA design flow. The role of the PV flow is to ensure

- the design layout is appropriate for manufacturing given the target foundry or fab
- the design layout meets the original design intent.

There are a number of components borrowed from the traditional CMOS IC physical verification. All, however, will require some modification. By leveraging the advanced capabilities of today's leading physical verification products, it is likely that existing tools can achieve all of these requirements. However, tools need the addition of dedicated rule files for nonphotonic purposes, separate from rule files associated with the same process.

The main tasks associated with PV and DFM can vary slightly from process to process, but typically consist of the following: design rule checking (DRC), fill insertion, layout versus source (LVS), parasitic extraction (PEX), lithography process verification or checking (LPC or LFD), and chemical–mechanical polish analysis (CMPA). Enabling this level of verification requires both process specific information, as well as details of the expected behavior of the components implemented into the design layout. This information typically provided by the foundry or fab, targets the manufacture of the design in the form of rule files, which are typically ASCII files, written in tool proprietary syntaxes that may be left readable to the user or may be encrypted.

PV for photonics will differ from that of the IC world. Rather than pushing electrons through metal wires and vias, photons are being passed through waveguides. This has an impact on the LVS and the PEX aspects of the design flow, as the device and interconnect physics applied is now different.

4.2.8.1 Design Rule Checking

DRC ensures that the geometric layout of a design, as represented in GDSII or OASIS data formats, adheres to the foundry's prescribed rules in order to achieve acceptable yields. An IC design must go through DRC compliance, or "sign-off," which is the fundamental procedure for a foundry to accept a design for fabrication. DRC results obtained from an automated DRC tool from a trusted EDA provider validates that a particular design adheres to the physical constraints imposed by the technology.

Traditional integrated circuit DRC uses one-dimensional measurements of geometries and spacing to determine rule compliance. However, photonic layout designs include nonrectilinear shapes, such as curves, spikes, and tapers, which require an extended DRC methodology to ensure reliability and scalability for fabrication (Fig. 4.12). These shapes expand the complexity of the DRC task—in some cases it may not be possible to describe completely the physical constraints with traditional one-dimensional DRC rules.

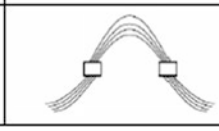
Photonic component		Curvilinear path length	Curvature
Waveguide Interconnection		✔ Signal integrity	✔ Signal integrity
Ring resonator		✔ Signal integrity ✔ Functional	✔ Signal integrity
Directional coupler		✔ Signal integrity ✔ Functional	✔ Signal integrity
Focused grating coupler			✔ Functional
Y-junction splitter		✔ Signal integrity	✔ Signal integrity
Mach-Zehnder interferometer (MZI)		✔ Signal integrity ✔ Functional	✔ Signal integrity
Array waveguide grating (AWG)		✔ Signal integrity ✔ Functional	✔ Signal integrity

Fig. 4.12 Various photonic components that require curvilinear parameter validation

One technique used is upfront scaling of the design by a factor of 10,000× so that snapping and rounding issues are alleviated. However, some conventional EDA tools snap curvilinear shapes to grid lines during layout. Such snapping renders this technique useless for conjoint photonic structures, which are formed by abutment of primitive shapes, since the intersection of these shapes may not lie on a grid point.

Another approach relies on a DRC capability called equation-based DRC (eqDRC), which works well with photonic designs [25]. This facility extends traditional DRC technology with a programmable modeling engine that allows users to define multidimensional feature measurements with flexible mathematical expressions. EqDRC can be used to develop, calibrate, and optimize models for design analysis and verification.

False Errors Induced by Curvilinear Structures

Current EDA DRC tools support layout formats such as GDSII, where polygons represent all geometric shapes. The vertices of these polygons snap to a grid, the size of which is specified by the technology or process node. Traditional DRC tools are optimized to operate on rectilinear shapes. However, photonic designs involve curvilinear shapes to create various device structures as well as in waveguide routing to minimize internal losses. The design fragments into sets of polygons that approximate the curvilinear shape for geometrical manipulation in DRC and other processes to handle curved shapes. These result in discrepancies between the intended design and what the DRC tool measures.

While this discrepancy of a few nanometers (dependent on the grid size) is negligible compared to a typical waveguide design with a width of 450 nm, its impact on DRC is significant. The tiniest geometrical discrepancies, which DRC reports, can add up to an enormous number of DRC violations (hundreds and thousands of errors on a single device), which makes the design nearly impossible to debug. Figure 4.13 shows a curved waveguide design layer, with the inset figure showing a DRC violation of minimum width. Although the waveguide is correctly designed, there is a discrepancy in width value between the design layer (off-grid) and the fragmented polygon layer (on-grid), creating a false width error.

Even though the designers carefully followed the design rules, a significant number of false DRC errors are reported. The extensive presence of curvilinear shapes in photonics design makes debugging or manually waiving these errors both time-consuming and prone to human error and is a typical scenario where designers

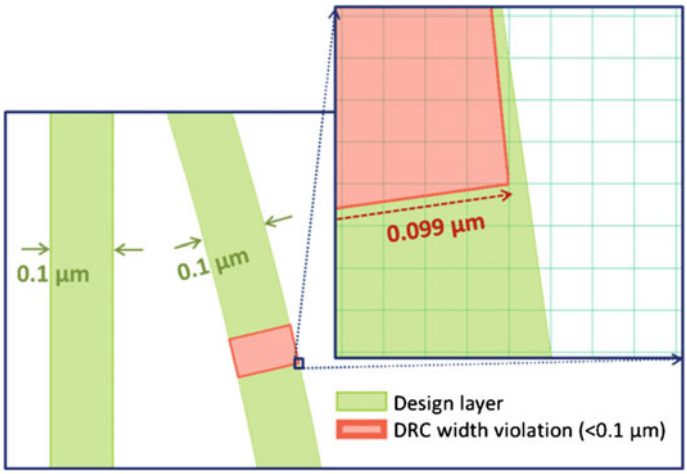


Fig. 4.13 The *green* waveguide is an example of an off-grid, *curved* waveguide design layer, while the *red* polygon is an example of the on-grid, fragmented polygon layer. The *inset* shows an enlarged view including the polygon layer that flags the width error of the waveguide. The polygon vertices are on-grid, which results in the discrepancy in the width measurement

can take advantage of eqDRC capabilities. They can use the DRC tool to query various geometrical properties (including the properties of error layers), and perform further manipulations on them with user-defined mathematical expressions to filter out the false DRC errors. In addition to knowing whether the shape passes or fails the DRC rule, users can also determine the amount of error, apply tolerances to compensate for the grid snapping effects, perform checks on property values, and process the data with mathematical expressions.

To illustrate this approach, one can compare the traditional technique with an eqDRC implementation. First, let us examine the result given by a traditional DRC format. A conventional width check can be written as 4.1:

$$\text{thin wg} := \text{width}(\text{wg}) < w \tag{4.1}$$

where width stands for the DRC operation or operations that generate the error layer under a specified width constraint (smaller than w), and wg is the name for the waveguide layer that is examined by the width operation.

Using eqDRC, the width check can be extended as follows:

$$\begin{aligned} &\text{if wg is non-Manhattan then} \\ &\text{thin wg} := [\text{width}(\text{wg}) + \text{tol factor}] < w \end{aligned} \tag{4.2}$$

where the conditional statement evaluates whether the waveguide polygon is non-Manhattan-like (i.e., curvilinear, based on the user's definition). Then tol is a tolerance value that is set to discriminate for any possible error induced by grid snapping. Combining with the Boolean expression, the rule functions as a traditional check while also incorporating the user-specified conditional and mathematical expressions needed to minimize false errors. Debugging also becomes much easier, with property values (e.g., the error width, the adjusted width, and the amount of adjustment needed) visually displayed on the layout.

Multidimensional Rule Check on Tapered Structures

Another important photonic design feature that does not exist in IC design is the taper, or spike, which is when, in any geometrical facet, the two adjacent edges are not parallel to each other (Fig. 4.14). This kind of geometry exists intentionally in the waveguide structure, where the optical mode profile is modified according to the cross-sectional variation, including the width from the layout view and the depth determined by the technology. The DRC width checks to ensure that fabrication of these structures must flag those taper ends when thinned down too far, which can lead to breakage, and possible diffusion to other locations on the chip to create physical defects. It also holds true for the DRC spacing checks in the case of taper-like spacing.

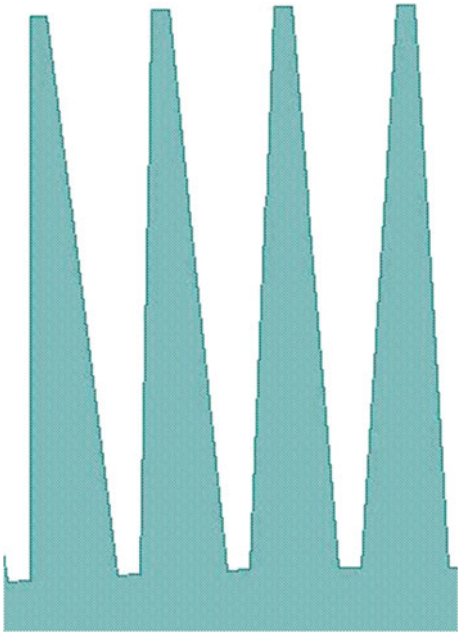


Fig. 4.14 Taper design from a photonic device

A primitive rule to describe this constraint could be stated as:

$$\begin{aligned}&\text{Minimum taper width should be larger than } w;\\ &\text{otherwise, if it is smaller than } w,\\ &\text{the included angle at the tapered end must be larger than } a.\end{aligned} \tag{4.3}$$

This primitive rule is a simple way of describing the width constraint for a tapered design. It differs from the conventional width rule for IC design in that it involves the angle parameter in addition to the width, which allows more flexibility in this kind of feature, which is typical for photonic designs. However, the implementation of the rule is impossible with one-dimensional traditional DRC since more than one parameter must be evaluated at the same time.

Conversely, using eqDRC capability, users can code a multidimensional rule:

$$\text{sharp end} := \text{angle}(\text{wg; width} < w) < a \tag{4.4}$$

where angle stands for the DRC operation that evaluates the angle of the tapered end with a width condition (smaller than w), which means that users can perform checks that were not previously allowed by traditional DRC.

These are just a couple of examples of the issues involved in DRC for photonic circuits. Because photonic circuit design requires a wide variety of geometrical shapes that do not exist in CMOS IC designs, traditional DRC methods are unable to fulfill the requirements for reliable and consistent geometrical verification of such

layouts. However, the addition of photonics property libraries and the ability to interface these libraries with a programmable engine to perform mathematical calculations mean that photonic designs can enjoy an elegant solution for an accurate, efficient, and easy debugging DRC approach for PICs. Such an approach helps effectively filter false errors, enables multidimensional rule checks to perform physical verification that was previously impossible, and implements user-defined models for a more accurate and efficient geometrical verification that finds errors that would otherwise be missed.

In addition to the traditional EDA DRC solutions, there are tools that from nature are coping with all angle designs. These tools provide a relevant set of DRC capabilities especially targeting the curvilinear structures so common in PIC design.

Density and Fill Insertion

An additional part of DRC is to check adherence to density rules. Density rules check the ratios of given layers within a region across the chip and are used to ensure that they meet the manufacturing requirements as dictated by the chemical–mechanical planarization (CMP), etching, and other parts of the manufacturing process. They ensure that no one portion of a design has too much or too little of a given layer to cause a problem.

In the case where a region is too dense, the only recourse is to modify the design to spread the structures out. In the case where a region is insufficiently dense, however, fill techniques can be used to help correct the problem. Fill shapes are geometric structures with one or more layers inserted into the layout, but not connected to any of the circuit components. Because these serve no function in the circuit itself, they are often referred to as "dummy" objects.

In electronics, the DRC tools are used to insert these dummy fill objects into the layout. The simplest approach is to identify low-density areas and then fill them as much as possible with rectangular dummies, ensuring that these structures do not interact or come to close to existing circuit geometries. This approach, however, can be overly corrective. Adding too many dummies may cause two neighboring regions to now have vastly different densities, causing new manufacturing problems. Also, these dummy structures may still have some impact on the neighboring circuit structure behavior.

For these reasons, new fill techniques have been introduced. Referred to as "smart fill", these techniques are designed to be aware of the full circuit density from a local scope in the neighborhood of each local region, to the entire circuit. With this knowledge, the tools can automate the insertion of fill structures to enable the fewest geometries required to meet all density requirements, without overfilling. These approaches also enable the creation and placement of more complex structures including multiple layers and hierarchical cell structures.

These smart fill techniques are also implemented for use in photonics layout, either by the layout tool directly or in the post-processing step with DRC tools. Separate filling rules can be set to separate out the spacing required for fill shapes

and circuit topology shapes based on the device type. Impact on the optical behavior of the circuit can be significantly reduced by reducing the number of added fill shapes.

4.2.8.2 Layout Versus Schematic

In a traditional IC process, designers create a design based on the desired electrical behavior, typically using a schematic capture tool. Next, they simulate the circuit's performance using foundry device models, usually in the SPICE format, to ensure the achieved behavior. Finally, they build a layout to implement the schematic design. As noted, this layout must comply with the foundry's process design rules, which is confirmed by passing the design layout, typically in a layout format such as GDSII, to a DRC tool ensure that the drawn layout can be manufactured. It does not guarantee that the silicon represented by the layout will behave as designed and simulated. To achieve expected behavior, the physical circuit design is validated using an LVS comparison flow. The LVS flow reads the physical layout and extracts a netlist that represents its electrical structure in the form of a SPICE circuit representation. A comparison of this extracted netlist to the original netlist simulation is then made. If they match, the designer has confidence that the layout is both manufacturable and correctly implements the intended performance. When they do not match, error details can be provided to help the designer fix and debug common errors such as short circuits, open circuits, or incorrect devices.

Challenges of Silicon Photonics for LVS

However, this process flow does not work well for silicon photonics. While photonic design shares many similarities with custom analog IC design at a high level, the challenge is in the details. Although silicon photonics design also relies heavily on early model simulations, SPICE does not have the sophistication required to simulate optical devices, as described before. Most notably, a large portion of a PIC design is made out of custom cells or parameterized building blocks, and only a fraction is composed of the pre-characterized components from the library or PDK.

Another complication in LVS for photonic circuits lies in the unusual nature of the devices. The typical LVS flow goes through three stages: recognition of the devices in the layout, characterization of the devices, and comparison of the device connectivity and parameters with those in the schematics. The first step presents a relatively small challenge because the photonic devices are formed from easily recognizable patterns. However, the complexity and curved nature of these patterns make device characterization very difficult [26]. The performance of the photonic devices depends on many details of the complex shapes that form the devices, as well as adjacent layout features (Fig. 4.15).

Figure 4.16 shows a simple ring resonator device. There are four pins—In1, In2, Out1, and Out2. Six parameters (all of which can vary independently) are relevant

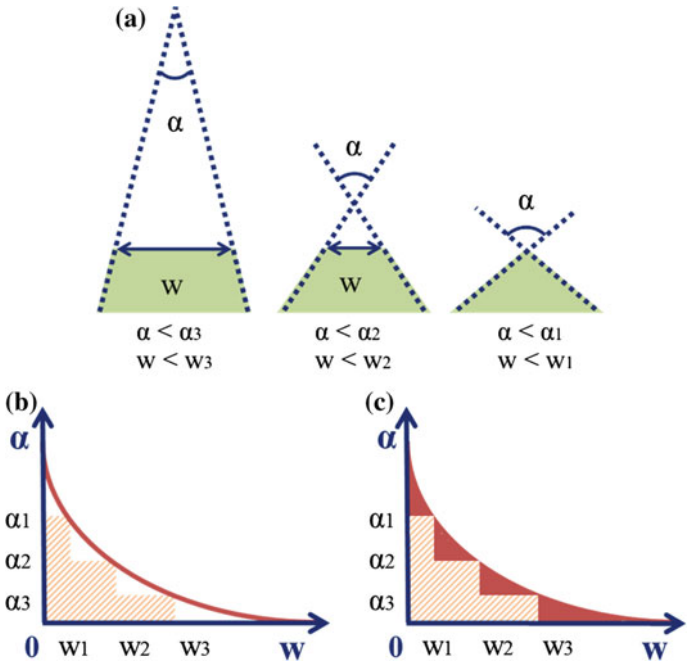


Fig. 4.15 **a** Width constraints ($w3 > w2 > w1$) dependent on taper angle conditions ($\alpha 3 < \alpha 2 < \alpha 1$). **b** The plot of real-world physical constraint (*solid line*) and the corresponding design rules (*shaded area*). **c** Discrepancy highlighted between the discrete design rules and the physical constraints

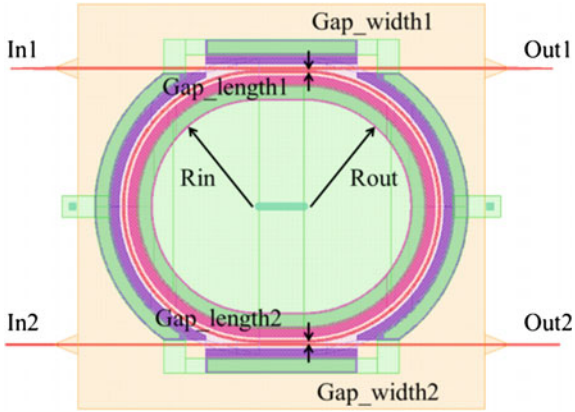


Fig. 4.16 Ring resonator device with six specified parameters that must match the parameters of the pre-characterized device. *Source* Ring resonator layout design from the Generic Silicon Photonics (GSiP) PDK, developed by Lukas Chrostowski and his team from University of British Columbia

to the behavior of this device—Rin, Rout, Gap_length1, Gap_width1, Gap_length2, and Gap_width2. If any parameter differs from the intended value, the device will not implement the intended behavior. Given the curved nature of the Rin and Rout, it is hard to represent the design accurately in GDSII, which is a rectilinear format (i.e., straight lines), used to represent the shapes and their locations in the physical design. As a result, inaccuracies in the radii of a curved photonic device can occur, which may be significant enough to cause a functionality problem.

The traditional approach to device characterization in LVS is to collect all layout objects around the device that could possibly affect its performance, and take measurements to describe the interactions between these features and the device itself, such as distances and projection lengths. These measurements are substituted into closed-form expressions, either based on first-principle theories (i.e., physical equations) or by empirical curve fitting techniques.

However, this approach fails when many features can affect the device, or the nature of the interaction between layout objects cannot be captured with sufficient accuracy by a few simple measurements, which is the case for photonic devices. This situation is very similar to the problems faced by analog circuit designers, where device performance sometimes depends on mutual capacitances and inductances of thousands of layout objects, in addition to the few objects making up the device itself.

Adjustments to the LVS Flow

One possible solution is to forgo characterization based on precise measurements, and instead recognizes devices from a set of known patterns, including both the primary device features and the surrounding "halo" of layout shapes. The devices can be pre-characterized using existing silicon photonics simulators. If necessary, a small number of degrees of variability can be introduced into the pattern, but, for the most part, the device in the layout must match one of the pre-characterized patterns exactly. When the designer implements these pre-characterized devices in the layout, the LVS tool can extract the device, measure its relevant parameters, and compare them to the pre-characterized pattern. Any device that is not found in the pattern library is flagged as an unknown device and considered a layout error.

This, of course, introduces a strict limitation: each device instantiated into the layout must match the expected layout pattern. The preference is to enable a similar recognition based on pre-characterized devices, which may vary in a set of known parameters. This must be achieved, in a way, that passes the intended device shape for each placement to the verification system. This is possible through design tool and flow integrations. While generating a photonics circuit layout, a pre-characterized device can be placed with initial parameters, be they physical or optical. The rendering of the shapes into the layout will require sophisticated calculation from an optical design tool, which will return the layout shapes based on curve equations. It is possible at that point to have the curve equations also fed forward to the physical verification flow. At the time of LVS, the verification tool

can render the same set of equations for each placed object. Using various comparison techniques, any outliers to the expected shape, either in rendering or due to interaction with other structures in the circuit, can be identified and highlighted to the designer for correction. Given the ability to compare intended structure to the layout, and knowing the original parameters used to generate such a structure, once the component shape has been verified as meeting expectations, it is no longer necessary to physically reextract the parameters. Instead, the original parameters used when placing the structure can be passed back out to the extracted layout. The original parameters may be passed to the LVS in the form of text in the layout associated with the specific device or structure, or through other formats passed to the LVS flow.

Another challenge for the LVS verification of photonic circuits arises at the circuit comparison stage. Most LVS tools advance under the assumption that an analysis of the layout can rely on logic properties of individual CMOS gates described in widely available libraries. The basic elements of a photonic circuit, such as resonators, modulators, and multiplexers, are quite different. Until silicon photonics reaches greater maturity, it is unlikely that common LVS tools will support all the fundamental photonic devices as "native devices" at the same level as they support metal–oxide–semiconductor field-effect transistors (MOSFETs) and CMOS gates. Instead, the LVS tool must support user-defined devices and circuit patterns. Verifying device parameters also requires additional flexibility—some of the parameters apply to the entire device, while others associate with a particular device pin or group of pins (e.g., transmission and cross talk of a particular waveguide in a multiplexer). Instead of "standard" gates, pattern-driven recognition of circuits is necessary to isolate elements performing specific functions.

Conceptually, this approach resembles the solution typically applied to the analog device characterization problem: the exact performance characteristics of these devices are complex and often poorly understood. The designers often lack an accurate compact model with a few well-known parameters. Instead, the complex interactions of many geometries in a relatively large layout context determine the device performance. The situation is remarkably similar for photonic devices, whose performance is determined by fine details of the many layout shapes that comprise the device; details that are affected by the artifacts introduced when the smooth curves of the drawn geometries are rendered to GDSII polygons, then further fractured into elements suitable for mask making machines, and finally distorted by the lithography process. As a result, one should not expect a reliably characterized device using only a small number of parameters related to its scale and size. Instead, the LVS tool must compare the devices with a library of known good and qualified configuration variants. When there is a found match, the performance parameters can be extracted directly from the library entry. Devices that are "similar," but do not quite match any of the library variants, should be flagged as warnings.

Silicon photonic designers can gain confidence from true LVS verification when the LVS tool can identify and extract user-defined devices with complex curved shapes, and extract appropriate physically measured device parameters for comparison to a carefully pre-characterized device library. Using this LVS approach,

intended device-to-device behavior can be verified, ensuring the absence of unintended shorts or opens. Careful verification further ensures the expected behavior of each device in the circuit that the "as-drawn" device parameters match the intended, pre-characterized behavior. Perhaps most important, unintended design errors are identified early and presented to the user in a well-structured design environment, allowing fast and easy debug, saving unnecessary manufacturing cycles, and dramatically cutting time to market.

4.2.8.3 Parasitic Extraction

In the electronics world, extraction and comparison of the circuit are not sufficient to ensure that the circuit will meet the intended behavior. That is because the metal interconnects have resistive and capacitive impacts on the circuit. In traditional LVS, these interconnects are treated as "ideal." There is nothing to compare them to as there is no place in the historic SPICE format to hold the parameters. As such, the parasitic extraction flow is used to characterize interconnects to identify and insert into an extracted netlist where these parasitic resistors or capacitors may reside. This extracted netlist can then be used in subsequent simulations to validate whether their impact has invalidated the design behavior beyond expectation.

While the transport mechanisms in the optics world are much different from the electronics world, there may be an equivalent to the parasitic extraction flow for photonics. If a photonic layout is generated using traditional EDA tools, it is likely that the waveguide interconnects are also not considered as devices with a function, but just as a connection between two ports when passing to simulation. These will need to be extracted and passed to get the most accurate post-layout simulation results. In fact, photonic designers may prefer to build strictly from the layout, skipping any schematic capture from the start. In this situation, post-layout simulations can rely only on what can be extracted out. Of course, this makes debugging of shorts and opens dependent on simulation results only, increasing debug time.

Fortunately, this can be achieved relatively easily and can be done as part of LVS. Waveguide interconnects can be broken down into components including straight segments, bend segments, and potentially tapered segments. All other segments, including Y-branches and waveguide crossings, should be treated as devices to help ensure intended interactions. In this way, any single waveguide is known to connect only two photonic devices.

By breaking a waveguide into the basic component types, each component can then be recognized as a device during the time of LVS extraction. Parameters such as lengths, widths, and curvatures can be extracted so long as each is known to start and end with a straight, Manhattan segment, even if that segment is only a single database unit in length. These components can be ignored (shorted) at the time of LVS comparison, but can be retained in the form of an extracted netlist for passing to post-layout simulation.

In a traditional PDA flow, the layout tools are building the total mask layout as a netlist of photonic primitives, like straights, a variety of different types of bends,

tapers, etc. In such an environment, all the information is available while generating the GDS data and this data can be provided to the LVS tool either annotated in the GDS file or as a separate netlist file to support a better LVS extraction and reconstruction of the circuit from the GDS data.

4.2.8.4 Design for Manufacturability

Waveguide discretization and the following physical production steps have a vast impact on the performance characteristic of photonic integrated circuits. The typically used GDSII mask format has two principle limits:

- its database unit is usually set at 1 nm
- the maximum integer of 32 bit

So with the typical, mainly flat, silicon photonics waveguide designs, there is a lack of data preparation space. Also, fab mask writing machines have limited precision depending on how they write the masks:

- as (e-beam) grid (e.g., a triple write with 25 nm beam thus 8.3 nm delta)
- as smoother curves using e-beam or laser steering in any direction using well-known GDSII extensions as the Raith-GDSII format and its associated writers

However, the cleanroom processes itself causes nonideal etching, which also impact high contrast waveguides severely. While electronic circuits can easily handle nm variations, this deteriorates photonics performance in propagation losses, back reflections, and scattering.

The first effect (GDS) is being deterministic, and some aspects of the problem are handled with the newer OASIS format. However, both mask writing and cleanroom processing cause statistical variations and, therefore, require careful handling. OASIS allows arbitrary integer sizes and thus removes the second data limit and consequently the first one. However, smooth silicon photonic waveguide curves are still not easy to describe in OASIS, as the normally used polygons are very verbose and lead to large data sets (polygons of 100,000s of points) rather than a few curvilinear segments describing the same photonic structures. These large data sets lead to unacceptably large mask processing runtime if nonoptimized curvilinear libraries are used.

In the future, as silicon photonic devices share more and more silicon area with conventional CMOS devices, a radically different approach may be required. The state-of-the-art computational geometry library, Computational Geometry Algorithms Library (CGAL), supports curves for the construction of arrangements and the 2-D intersection of curves, but performance is not comparable to standard scanline implementations. Recent advances in processing parameterized curves are needed for an effective solution. Also, silicon photonic layouts, especially waveguides, have properties that are not present in conventional CMOS structures.

Lithographic Checking

Because photonics circuits are extremely sensitive to the exact shapes of devices and waveguides implemented in silicon, lithographic variations must be minimized and accounted for when projecting the behavior of a photonics system. Lithography simulation and hotspot detection capabilities in tools such as Calibre® LFD™ are being extended in collaboration with foundries. These tools can be used to model not only the standard lithographic impacts, but also the variations in the process due to changes in dose, depth of focus, etch rates, etc., which can vary at the lot, wafer, or even die level. These techniques can be used to ensure that silicon photonics designs can be faithfully reproduced on a wafer within the margins required for the performance specifications.

Lithography checking tools use a foundry provided design kit to enable designers to run simulations and obtain an accurate description of how a layout will perform a particular lithographic process. By identifying lithographic hotspots (i.e., areas where the potential variation exceeds a preset boundary) before tape-out, designers can modify the design to eliminate production failures. Here are some examples.

In silicon photonics, the lithographic simulation must accurately predict the curves that will be in the manufactured photonics devices (Fig. 4.17). Designers can achieve this by running a lithographic simulation on multiple process windows to capture the "as-manufactured" dimensions of the design (Fig. 4.18). Leveraging the capabilities in LVS extraction discussed previously, this simulation allows them to compare the "as-manufactured" simulation results to the original intended device curvatures to determine if the dimensions are within requirements and if the manufacturing variance is within an acceptable range. Addressing these issues during design allows for correction before manufacturing.

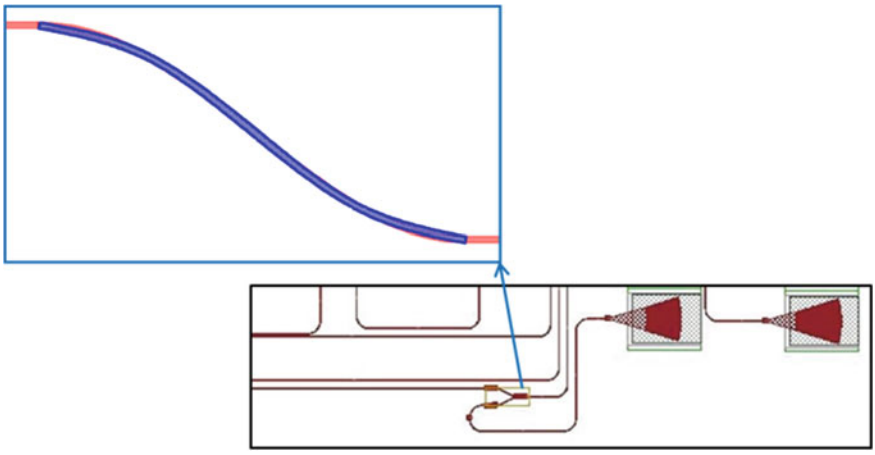


Fig. 4.17 Comparing a component curvature to the rendered layout during layout versus schematic (LVS)

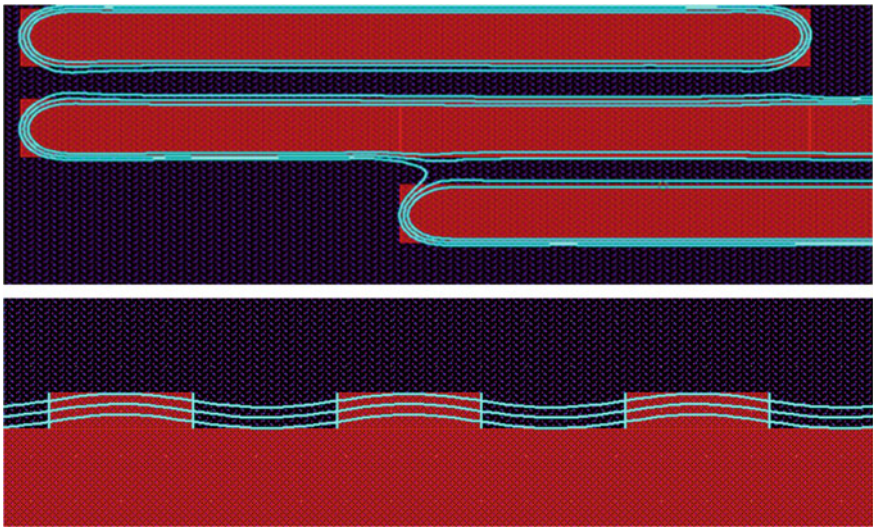


Fig. 4.18 The contours represent the simulated fabricated device. The three curves represent anticipated process variation. *Source* Lukas Chrostowski, University of British Columbia

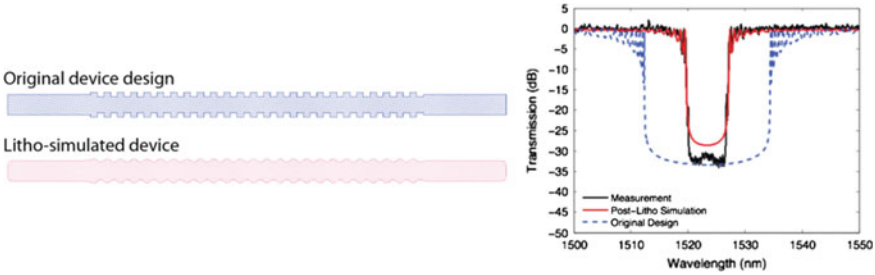


Fig. 4.19 Using lithographic simulation, users can predict "as-manufactured" performance [17]

The parameters associated with the "as-manufactured" simulation results can also be captured and passed back, in the form of device parameters in SPICE, to optical simulation. They are then used to determine the performance impacts of variations in the manufacturing process. Figure 4.19 shows a device designed with 40 nm square corrugations. Using the lithographic simulation of the device in a 3-D Maxwell solver tool like Lumerical's FDTD Solutions, designers can determine if the performance of the simulated device will meet the performance expectations for the manufactured device during the design cycle, greatly reducing the number of design iterations.

While the lithographic process is context sensitive, given the geometries and spacing in current photonic layout, it is expected that device-like components can be accurately modeled in a stand-alone method, so long as sufficient design rules

used ensure no other geometries in the layout have a lithographic impact. In this sense, it is possible that known devices can be pre-characterized for a given process to validate under which range of parameters the device will meet intended optical behavioral expectations.

While visualizing geometric differences between layout and manufacturing, and capturing behavioral simulation differences is helpful, it does not help the designer to know what to do in the case when the circuit layout does not meet the desired behavior. Some method to determine the structures and suggest or even automate changes to the layout that can result in the intended designed representation in the manufactured structure is required. In the IC world, this is often referred to as retargeting.

In the IC world retargeting takes the form of adding or subtracting small shapes at the corners of a Manhattan wire or device shape. By creating these of a small enough size, these shapes, known as serifs, will be too small to manufacture, but their presence (or removal) can pull the lithographic optical imaging of those shapes to more closely meet the original design. Normally, the foundry does this retargeting, but in some cases, the designer may have to do the retargeting if more accuracy is required for simulation.

While this approach may help for structures such as the Bragg grating example, it does not lend itself to the curved shapes in photonics circuits. In this case dedicated design tools like OptoDesigner are required that can process the analytical description of the design intent and the provided information from the LFD simulation to calculate the mask layout that will result in the correct representation after lithography (or etch).

PDKs for Silicon Photonics

Integrated circuit design benefits from a scalable design environment that enables and supports fabless design companies and generations of SoCs that contain billions of transistors. One of the key elements of its success is the concept of PDKs (Sect. 4.2.2), which speed design development by providing designers with the setup configuration and data files required by their design tools and the foundry process. Using the compact models and design rules in the PDK, CMOS IC designers can leverage the experience of other experts by taking advantage of pre-characterized devices, allowing them to focus on applying those into application-focused solutions. PDKs lower risks because a foundry stands behind its PDKs with support and guidance on their use.

In a similar way, we need photonic PDKs that include device compact models with agreed-upon parameters and optical or optoelectronic simulation technology to enable designers to simulate photonics with electronics. We also need design rules that are precise enough to ensure manufacturable devices without generating thousands of false rule check errors, and an LVS flow to ensure that those simulations match the final product.

Since 2007, the PDK approach has been actively developed for photonics, with the activities to create more generic instead of application-specific fabrication processes for InP and silicon photonics by organizations like FhG/HHI, Oclaro, IMEC, and CEA/Leti. Together with software vendors, tool interoperability and more relevant standards for the definition of PDKs have been developed. Today, most facilities that provide access to photonic technologies by multi-project wafer runs are offering a PDK for a variety of tools. The amount of building blocks and maturity of the libraries are varying from fab to fab.

4.3 Manufacturing and Lithography: Accuracy Problems and Process Variation

As already discussed, silicon photonic circuits normally consist of high-contrast, submicron waveguide features of silicon embedded in a cladding of silicon dioxide or air. These waveguides can range from simple lines to complex patterns that control the light based on diffraction, which include photonic crystals, subwavelength gratings, and fiber couplers [27–30]. Most silicon photonics platforms have a similar fabrication strategy: the patterns are defined and transferred into a single-crystal silicon layer on a commercially sourced silicon-on-insulator (SOI) wafer using lithography and plasma etching. Often, two or three patterning steps are used to define different etch depths [31]. This "passive waveguide definition" is considered as the core of the silicon photonics fabrication process, although it only covers a small fraction of the actual fabrication steps.

4.3.1 Silicon Photonics Fabrication Processes

A full-fledged silicon photonics process involves many other process modules, beyond the two or three passive patterning steps. These additional fabrication modules are principally based on modules for CMOS manufacturing. For carrier dispersion modulators, p and n dopants are implanted to create junctions in the silicon waveguides that will enable active refractive index modulation. These junctions are contacted to high-doping regions and silicidation. Photodetectors (for the telecom wavelength range), usually implemented in Germanium, introduce the fairly costly modules of Germanium epitaxy, and the accompanying specialized doping processes. Electrical contacting is usually done through CMOS-like metallization layers. Details vary between the different manufacturers, but the evolution is toward a multilayer Copper damascene metallization to allow sufficiently complex electrical routing.

While all the active functionality involves many more fabrication steps (and, therefore, cost) than the few litho-etch steps of the passive waveguides, the focus of the design of photonic devices is focused on these passive waveguide patterns.

The importance of the waveguide patterns in the silicon layer comes from the high refractive index contrast of the silicon waveguides with its surrounding oxide. The same high contrast that enables submicron waveguides, tight bends, and dense integration also makes the waveguide sensitive to small variations in geometry. Variations in width and thickness of a waveguide will change the propagation constant of the light, and, therefore, the phase and group delay the light will experience. When a waveguide is used in an interferometric filter (a very common function in photonic integrated circuits), a 1 nm linewidth deviation can give rise to a 1 nm shift in filter response, an order of magnitude that can severely affect the performance of telecom devices [32]. The pattern control of the waveguide layer, and design techniques to make high-contrast waveguide geometries more tolerant [6], are essential for the success of silicon photonics.

It is important that the essential geometry parameters be measured during fabrication to keep a process stable, and many fabrication facilities have statistical process controls in place. However, it turns out that the most accurate characterization of the process is actually the optical transmission measurements on the chip itself: because of the sensitivity of the waveguides to minute variations, the optical measurement is much more precise than the accuracy of thickness measurements or SEM linewidth measurements. Still, these data are needed and need to be correlated, but the design rules and compensation techniques in the design flow need calibrating against the actual process and optical measurements.

4.3.2 Lithography

The key step in the definition of patterns is the lithography. It is the step where the design patterns (created by a CAD design tool) transfer to a physical layer on the wafer. Because the lithography process has a strong impact on the quality of the fabricated patterns, it is important to understand the process and to include it as much as possible in the design phase.

For silicon photonics, there are, in general, two lithography processes in common use. E-beam lithography is the most commonly used for research purposes or one-off devices. However, as the industry is embracing silicon photonics, the deep UV-based techniques from CMOS are now being applied to silicon photonics. Both techniques define a pattern to a sensitive resist layer, which uses as a mask for a plasma-based etching process that transfers the pattern into the silicon layer.

4.3.2.1 E-Beam Lithography

E-beam lithography was the first technique used to make nanophotonic silicon waveguides and photonic crystals. The process uses a thin-focused electron beam to direct-write patterns into the resist layer. This serial process makes e-beam lithography only suitable for small volumes and chips of limited size. However, the

short wavelength of the electrons makes it possible to define patterns with nanometer accuracy.

Today's e-beam tools can fabricate designs from general-purpose mask layout files such as GDSII and OASIS, but the best results obtain optimized writing strategies used for all the patterns. The design process should then incorporate these strategies.

For instance, waveguide curves can be defined smoother if the electron beam can follow the curve of the waveguide, rather than rasterizing the bends. Hole size control for gratings and photonic crystal is much better when the beam spot and energy are tuned for individual holes.

Because there is always some scattering of electrons in the resist, nearby patterns can influence one another. This is called "proximity effects." For instance, two waveguides that are brought closely together (to form a directional coupler) will experience a change in line width compared to the isolated case. Alternatively, the first and last lines in a periodic grating will be different because they miss a neighbor on one side. Proximity corrections are included to compensate. The e-beam writing software can handle this, but the best results are when the design flow that generates the waveguide geometries incorporates the compensation strategy.

4.3.2.2 Deep UV Lithography

Where e-beam lithography can fabricate small numbers with extreme precision, optical projection lithography is the most used technique to define small patterns in huge quantities. However, the pattern resolution of optical lithography is limited by the wavelength of the light being used. That is why the CMOS industry has invested heavily in the use of shorter illumination wavelengths (currently 193 nm) and other resolution enhancement techniques (i.e., immersion lithography, double patterning, off-axis illumination, etc.). These developments have driven Moore's law to a point where transistors with linewidths of less than 20 nm are definable.

Deep UV lithography was first applied to silicon photonics in 2001, initially at 248 nm and later 193 nm wavelength [31]. It quickly became apparent that silicon photonics had some fundamental differences from CMOS electronics when it comes to pattern definition. Because silicon photonic waveguides consist of a variety of patterns (isolated and dense lines, holes, arbitrary geometries) that need to be reproduced with a high fidelity, many of the optimization techniques developed for CMOS patterning could not be applied. Transistors are commonly patterned layer by layer, and each layer only contains one type of feature. The precise alignment requirements of photonic waveguides require that a single-defined patterning step include all of the waveguide features. Therefore, typical minimum feature size for a "general-purpose" photonic patterning step is 3–4× larger than with an optimized patterning, for example, contact holes or transistor gates.

Using a general-purpose optical imaging process introduces a number of other problems. Every optical imaging system acts as a spatial low-pass filter. Close to

the resolution limit, sharp features and dense periodic patterns will be rounded and lose contrast.

Also, proximity effects will be present, but more complex than with e-beam lithography, as the optical patterning is a coherent process, and the proximity effects can be both additive and subtractive.

The addition of optical proximity corrections (OPC) is a time-consuming and computationally intensive process usually completed in one of the final steps of the design. However, effectively predicting the effect of the lithography on the actual design pattern should be early in the design flow (while designing building blocks), and designs should be optimized to reduce their sensitivity of the lithography process. Also, proximity corrections can add a significant cost to the photomask, making their use prohibitively expensive for all but real production reticles.

4.4 The "CoDesign" Problems

With the growing interest over the last 5–8 years in silicon photonics, which are manufactured in electronics facilities instead of dedicated photonics or multipurpose facilities, it became apparent that these silicon-oriented facilities are using tools from the electronics domain, especially when dedicated verification and sign-off EDA tools are used.

Additionally, designing a chip that contains both integrated electronics and photonics can be very challenging (in this section referred to as codesigning). Designers trained to design electrical circuits, and designers trained to design photonic circuits, typically come from different backgrounds, and require different know-how.

There is also a big difference in the maturity of both fields. In electronics, design workflows are highly standardized, and designers are trained to use highly mature, tested, and established EDA tools. On the other hand, photonic design is still at an early stage, and the design workflow is far from standardized. Additionally, the physics behind electronics and photonics are very different, leading to very different simulation models and circuit capabilities. However, even in EDA-established environments, the photonics designers tend to apply specialized PDA tools in order to overcome some of the limitations of the EDA tools.

In this context, integration between electronics and photonics design tools, are indispensable to improve the design workflow. To support the industry in moving forward to be able to codesign the photonics and electronics, either on one single chip or as a tightly integrated system in a package, design flows need to support co-simulation, co-layout, and co-verification. Software vendors from EDA and PDA are collaborating to improve design flows for silicon and other photonics technologies, leveraging an electronics design framework by integrating photonics capabilities for simulations, layout generation, verification, and design rule checking.

The following sections discuss the different types of challenges in more detail.

4.4.1 Co-layout

Integrated photonics can take on many forms depending on the type of material used for the electronics, the photonic elements, and the light sources. Some companies envision using a monolithic die that include lasers, transistors, and photonic elements all on the chip. The processing of a monolithic die is necessarily more complex to comprehend the different components, which implies additional spacing and isolation rules that must be adhered to while doing layout of the design. While working with a monolithic die to isolate thermally sensitive optical devices from the heat generated by the electronic portions of the design, comprehending the additional thermal and stress related analysis is a must.

Alternatively, some companies will choose to keep the electronics, photonics, and light sources on separate substrates and package them together as a system in package (SIP). This simplifies the layout of the individual die but shifts more work on ensuring that the multiple die in the package are properly located so that the die can all talk to each other with no loss of fidelity in the system. Particular attention must be paid to the thermal analysis of the SIP to guard against thermally induced failures due to different material coefficients of expansion, especially when employing flip chip and through silicon vias technologies.

4.4.2 Co-simulation

Because of the mismatch in timescale and models, simulation of a combined electronics–photonics chip is far from trivial. For example, in electronics, frequencies of interest range from DC to several tens of GHz, while in photonics, the typical frequencies are on the order of 173 THz (corresponding to 1.55 μm, a standard telecom wavelength). In order to match the timescales, typically the optical signal is represented as a complex envelope. The product of a very fast carrier represents the actual signal, modulated by a complex-valued envelope function. For many applications, it suffices to deal with the envelope function, which typically works on the same timescale as the electronics. When nonlinear effects cause mixing of signals at different frequencies, the simulation becomes more complex. An example of this is four-wave mixing [15]. However, even, in this case, the signal can be split up into multiple carrier wavelengths, and a compact model describing the rate equations can be used to describe the four-wave mixing (FWM) physics.

Depending on the required accuracy, there are different simulation strategies. In order of complexity, the following three approaches can be used to model photonics plus electronics:

(1) Using pure wavelength exchange: the electrical simulator and photonic simulator run separately. The output of one simulation transfers as input for another simulation, then exchange the signal waveforms between them.

A severe limitation of this method is that accounting for interactions between the photonic and electronic circuit is not possible.

(2) Using an electrical simulator to model both the electronics and the photonics was elaborated in Sect. 4.2.5 As long as the photonic models mapped onto electrical models is possible, this method can be very useful. Advantages are that all quantities (carrier density, temperature, etc.) are all mapped onto voltages and currents, making the results harder to interpret. Additionally, some complex photonic circuitry cannot be mapped easily onto electrical models.

(3) Full lockstep co-simulation. In this case, the photonic and electronic simulators are highly intertwined and exchange information on the level of the simulation time step. Although this would enable the capture of interactions between the photonic and electronic circuits, it is very difficult to implement. Also, this raises questions about stability and conservation of energy when exchanging information between the two domains.

Many PICs used in systems require electrical circuitry, and it is desirable to simulate the performance of the entire system. For many systems, this can be achieved by simple waveform exchange [33, 34]. For example, in a transceiver simulation, the electrical driver circuitry can be simulated with SPICE provided that the modulator impedance, which is almost entirely decoupled from the optical stimulus to the modulator, correctly loads the circuit. The waveform from the SPICE simulation can be imported into the PICs simulator where the simulation can continue until the output of the photodetector. While a more sophisticated co-simulation is probable in the future, suitable methods to achieve this are currently being explored.

4.4.3 Cointegration

To enable codesign of electronics and photonics, software tools from the two domains will need to work together to provide an efficient workflow. Existing workflows that combine electronics plus photonics work normally on the basis of exchanging files.

Using standardized database formats, software tools from different vendors will be able to communicate with each other in a more coherent fashion. For example, OpenAccess [35] is a well-established database format that allows the description of layout, schematics, netlists, technology settings, and so on. Because most software tools support OpenAccess, integration between different tools becomes much easier. Additionally, for the simulation aspect, OpenMatrices [36] could be used to exchange simulation information from/to the various software tools.

4.4.4 Packaging

An important and often initially overlooked aspect is the actual use of the fabricated integrated photonics chips. A "bare die" is only practical for initial lab tests, but cannot be used outside such a unique environment. Therefore the packaging of photonics plays an important role and dedicated and specialized packages for high performance were dominant until recently. The substantial cost reduction of a generic approach for the fabrication of the chip is now followed by the introduction of generic and standardized packages, comparable to the electronics world where SIP and 2.5-D and 3-D die integration becomes established. To enable photonics designers to design for packaging, "package and die" templates have been introduced, which form a 2.5-D integration with the high-speed electronic drivers and low-speed environmental control electronics typically within the package. To resolve the interdependent design rules between the package and the chip package providers have developed PDKs with information about the placement of optical and electrical interfaces and physical form factors.

4.5 Standards Organizations Helping Evolve a Disintegrated Design, Manufacturing, Packaging, and Test Ecosystem

From the late 1970s through most of the 1980s, almost all semiconductor ICs were designed, manufactured, packaged, and tested in large integrated device manufacturers (IDMs). In the 1980s packaging and test started to move offshore and eventually into separate companies that specialized in these services. In 1987, a major shift in the semiconductor ecosystem took place with the founding of Taiwan Semiconductor Manufacturing Company (TSMC). The founding of TSMC marked a change from ICs being solely designed, manufactured in IDMs to a disaggregated semiconductor ecosystem in which IC design, mask making, fabrication, packaging, and test were now being handled by multiple companies. Separate companies for IC design (also known as intellectual property or IP) companies would also come into the ecosystem at this time. The best example of this was ARM Holdings, founded in 1990.

4.5.1 Photonics Fitting into EDA

As integrated photonics becomes mainstream, it will be essential for silicon-based integrated photonics to fit smoothly into the existing silicon-based semiconductor ecosystem. For the most part, this means that electronic companies integrating photonics with their semiconductors will try to use existing EDA tools and standard

EDA formats to capture and hand off their designs to manufacturing and test. Photonics, however, presents many new challenges that will require the existing standards to be updated to handle these new challenges efficiently.

4.5.2 Adding/Modifying for Photonics

Each different articulation point in the ecosystem will need to be reviewed and analyzed as to whether or not the current formats and standards can handle integrated photonics. If the prevailing standard is not up to the task, work groups will need to be formed to determine how to best address any deficiencies. Good examples of this are the GDSII and OASIS formats. These formats typically fracture the mask data into rectilinear shapes before sending it to the mask manufacturer. Photonics, however, needs smooth curvilinear shapes printed, so it makes little sense to fracture a smooth curve into rectilinear stair step shapes only to have the mask manufacturer reheal these shapes back into a smooth curvilinear shape on the mask.

In the world of test, entirely new standards will likely be needed for integrated photonics that will augment existing analog and mixed-signal testing techniques. There needs to be particular emphasis placed on the interfaces between optical and electrical simulations and test program generation for photonic and optical testing.

4.5.3 Process Design Kits (PDKs)

Photonic process design kits will need to evolve for integrated photonics to scale to large numbers of designs and this is especially true due to two reasons. The first is the tight dependency between photonic component functionality and the processes that manufacture the devices. The second is the fact that the photonic design community will not own the fabrication process due to the disaggregated nature of the ecosystem. This means that the fabrication companies must spend time to create accurate representations of their processes that can be used by 3-D modeling tools and FDTD type solves to create good compact models that can be used by photonic circuit designers. It is not clear yet how this will play out as most fabrication facilities are reluctant to release this kind of data to their customers for fear of leaking their intellectual property through customers to other competing fabricators. In the case of spice simulation models, the compact models are created at the fabrication vendor for a specific set of devices that become the building blocks used by the circuit design companies. Today there is no agreed-upon set of building blocks for photonic design and in fact designers differentiate themselves by creating better versions of different photonic components. Some new method of handling this model issue will need to be figured out. The same will be true for physical verification rules needed to verify photonic designs. Because of the fidelity issues caused by lithography effects such as line edge roughness and rounding of edges

required for diffraction gratings, the fabrication companies, the EDA companies, and the design companies will need to collaborate on how best to handle these issues during the design phase so that manufacturing will be successful.

4.5.3.1 Electronic PDKs

Electronic process design kits will, for the most part, be as they are today with the exception that there will be a need for variations on standard processes to handle integrated photonics. These changes could have corresponding effects on the modeling of the electrical devices as well as the number of different types of materials that will need to be modeled and comprehended. Most PDKs today are CMOS based and as such the spice simulators and design rule decks have been optimized for this type of silicon-based materials. However, with the advent of monolithic solutions, there will be more III–V and II–IV materials that could come into play and both the compact models and the tools that use them need to understand the modeling of these materials.

4.5.3.2 Silicon Photonic PDKs

The success of the IC industry lies heavily in the standardization of processes and building device libraries based on these standardized processes. These libraries contained devices with the known performance provided by the fabrication facility. These tested devices significantly lowered the risk of the users and allowed them to focus on the complex circuits built through use and reuse of these tested libraries only (digital IC design). Alternatively, fabless users could pursue custom design for a novel device while continuing to take advantage of tested components for all the other essential functions (analog IC design). These electronic file packages of tested devices with known performance and settings for designing custom components are called the process design kit. Similar to IC industry, the standardization of the silicon photonics process in fabrication facilities resulted in the development of silicon photonics PDKs. Today, the PDK enables users to access the fixed standard processes of the foundry and provides a tested photonic library (PDK cells), significantly lowering their barrier to access. Today the photonic PDK typically comprises process and layout documentation, cell library in GDSII format and verification scripts. In scope, the photonic PDK is much limited compared to an IC PDK. For ease of use, the technology settings are also available in commercial CAD tools so users can import the settings to prepare their designs for the design flow for a particular fab (Fig. 4.20).

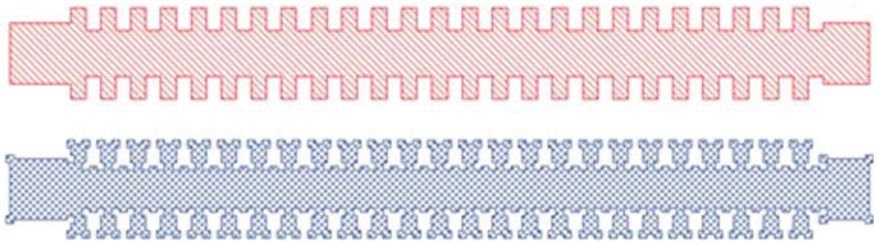


Fig. 4.20 Original (top) and retargeted (bottom) Bragg grating—example from OptoDesigner's automatic compensation capabilities

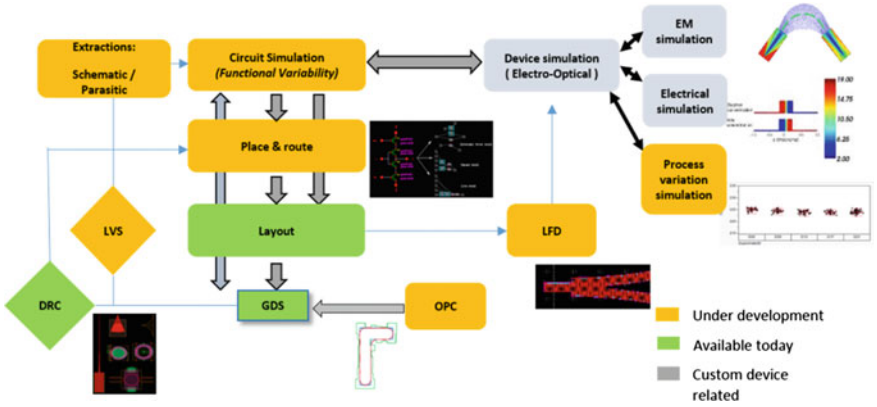


Fig. 4.21 The different stages of design development for silicon photonics design

4.5.3.3 Current Scope with Strengths and Weaknesses

The flowchart presented in Fig. 4.21 represents the different stages of design development for silicon photonics design. Typically, a fabrication facility supplies device models of the various basic components necessary for silicon photonics circuit. These components have known performance (device models) and layout. The models enable users to perform time domain or frequency domain simulations of circuits based on hundreds of such PDK cells while the fab-validated layouts ensure fab-compliant designs.

Nonphotonics users who may only focus on the system performance utilize the approach of simulating circuits based only on PDK cells. The user would export the circuit and connect the devices to actual photonic waveguides and electrical connections for place and route after realizing the target specifications. Such a GDSII file must be verified with LVS to check if no parasitics are introduced, and the design performs as per the circuit simulation results. If not, then the circuit needs to be resimulated to remove the unwanted parasitics. Once the LVS iterations are satisfactory, the final step is to verify fab compliance of the design through a DRC

check. Typically, such PDK-cell dominated circuit designs should readily produce a fabrication facility compliant GDSII file with minimal design iterations.

More experienced users may prefer to innovate the device design to create custom user cells, thus, requiring physical simulation of the device utilizing fab process layer specifications (etch depths, material indices, etc.). This physical simulation is the responsibility of the designer. After identifying the ideal user cell design and corresponding device model through simulations, this user cell can be used for circuit simulations together with PDK cells to realize a complete photonic circuit. Further, since this custom user cell has not been previously fabricated users can use LFD simulation of the device to mimic fabrication-induced imperfections and repeat physical simulations to predict fabricated user cell behavior. A mature and tested LFD toolbox can be a significant step to reduce design–fabrication cycles.

As a final step at the fab itself, OPC will be applied to select areas to compensate for known fabrication effects on select components. OPC is not part of the PDK and a responsibility of the fabrication facility.

Although PDK maturity varies between fabrication facilities, it is safe to say that stages highlighted in green in Fig. 4.21 are currently available in most silicon photonics PDKs. However, depending upon the facility, the stages in orange may or may not be under development to become part of the PDK. Finally, design stages in gray, are custom device simulation requirements addressed by the user directly and typically not within the photonics PDK.

4.5.3.4 Outlook

A significant part of the photonics dream design flow is under development and will become available in the near future. PDK development requires a close collaboration between fabrication facility, multiple CAD tool providers and in some cases also external design houses. It is important to highlight that the relevant actors have grasped the opportunity in silicon photonics technology to step forward and collaborate for this development. A great enthusiasm exists amongst the various actors in developing the different stages of the design flow and most crucially the PDK.

4.5.3.5 Optoelectronics

Optoelectronic components are more challenging than pure electrical or passive optical components. Some examples of common optoelectronic components are active phase shifters, modulators, detectors, and lasers. Due to the materials involved and associated additional process steps, the manufacturing of these components is complicated. For the PDK, one significant challenge is how to develop and calibrate compact models for these components. The frequency domain analysis used for passive optical components is clearly insufficient. As discussed in Sect. 4.2.5, compact models for use in purely electrical simulators have shortcomings that make

them easily applicable only in distinct cases. Therefore, the development of compact models for these components for time domain simulation remains intimately tied to the type of time domain algorithm used. For a given optoelectronic component, PDKs will likely contain different compact models used with various time domain simulators. While standardization is desirable in the future, it is not clear at this point which types of time domain algorithms will predominate, or whether a single time domain algorithm will be sufficient for all kinds of circuits.

4.5.4 Formats

With each step of disaggregation of the ecosystem came the need for standards to be used to hand off data between the various companies at each specialized function. In the mid-1980s standards groups such as JTAG (Joint Test Action Group) worked to create standard methodologies and formats for testing printed circuit boards (IEEE Std 1149.1-1990) and its derivatives. Later in 1999, STIL (Standard Test Interface Language) was created by defining a standard for IC digital vector test representation (IEEE Std 1450.0-1999). In the design world, the advent of EDIF (Electronic Design Interchange Format) began in 1983, a couple of years after third-party EDA vendors like Mentor Graphics and Daisy Systems started to appear on the market. In 1999, a coalition of semiconductor and EDA companies formed a new standard for design databases and application programming interfaces, which would later become known as OpenAccess [35]. At the design-to-mask manufacturing articulation point, multiple formats have been used over the years to pass mask layout data to mask manufacturers, including CIF (Caltech Intermediate Format), GDSII (Graphical Database System II from Calma, now Cadence Design Systems, Inc.), and as of October of 2004, a new format called OASIS (Open Artwork System Interchange Standard) and OASIS.MASK both of which are SEMI-owned standards (SEMI P39 OASIS and SEMI P44 OASIS.MASK). SEMI (Semiconductor Equipment and Materials International) is a global industry association serving the manufacturing supply chain for the micro- and nanoelectronics industries.

Since integrated photonics will inevitably be codesigned and verified with silicon ICs, it makes sense for photonic design automation tools to try to make use of the existing silicon IC EDA formats to enable a smoother integration with EDA tools.

4.5.5 Standards Development Organizations

4.5.5.1 Silicon Integration Initiative (Si2)

CAD Framework Initiative, Inc. (CFI) started out in 1988 as a not-for-profit corporation whose original mission was to develop an open, standard framework for integrating EDA applications from across the entire semiconductor and EDA

industries. The founding members involved in setting up CFI included Cadence Design Systems, Digital Equipment Corporation, Hewlett-Packard, IBM, Mentor Graphics, Motorola, Sun Microsystems, and ViewLogic Corporation. It is important to note that during the early years, the Microelectronics and Computer Consortium (MCC) [37], one of the largest computer industry research and development consortia located in Austin, also provided much support as CFI was being established [38].

In 1997, CFI was renamed Silicon Integration Initiative, Inc. (Si2) to enlarge its scope to define interface standards that facilitate the integration of design automation tools and design data for the benefit of end users in the semiconductor industry and EDA vendors worldwide.

Originally chartered under the "National Cooperative Research Act" of 1984, this was updated to follow the "National Cooperative Research and Protection Act" of 1993 (NCRPA) [39]. The reasoning behind this act is designed to promote innovations, facilitate trade, and strengthen the competitiveness of the United States in world markets. It does this by clarifying the applicability of the rule of reason standard to the antitrust analysis of standards development organizations while engaged in a standards development activity. It continues to provide for the possible recovery of attorney's fees when prevailing in damage actions brought against them under the antitrust laws. Moreover, the NCRPA provides the opportunity to limit any potential monetary damages brought under the antitrust laws for actual damages, as opposed to treble damages.

For a standards development organization, such as Si2, to even be considered to receive protection from the NCRPA, Si2 and its staff must follow certain guidelines that make them truly unbiased and transparent. Si2 plans, develops, establishes, and coordinates voluntary consensus standard procedures that incorporate the attributes of openness, the balance of interest, due process, an appeals process, and voluntary consensus. Si2 cannot be a part of any parties participating in the standards development organization. One of the greatest values that Si2 brings to the electronic design automation (EDA) industry, is that, as a not-for-profit organization with its executive and engineering staff, it can ensure that its members follow these guidelines.

In 2012, Si2 partnered with the European Union to help extend Si2's EDA-based standards to become photonically aware. This event precipitated Si2's creation of the Silicon Photonics Technical Advisory Board (SP-TAB). Through this oversight committee, members have been working on establishing extensions to current EDA standards, but also creating new ones when extending does not make sense. The OpenMatrices file format is a good example of this [36].

The OpenMatrices format describes scatter matrices (S-matrix). In short, a scatter matrix describes the complex-valued transmission from/to each physical port of a component (see Sect. 4.2.5 for more details). The OpenMatrices format was created to provide a standard for representing these matrices, which can be used to share S-matrices between different vendors. For example, a physical FDTD simulation could be used to extract the S-matrix from a component and store into an OpenMatrices. A circuit simulator then receives this data.

The OpenMatrices format is different from the Touchstone format. OpenMatrices is more flexible and can describe S-parameters for a multidimensional set of parameters such as wavelength, temperature, input voltage, etc., which is necessary to model active, nonlinear photonic devices, for example. OpenMatrices is written to disk as an XML file, following a fixed XSD scheme. Although the format's description use was first suggested within the SP-TAB context, it is not limited to photonic components.

4.5.5.2 PDAFlow Foundation

Driven by the identified needs to improve existing design solutions and create design flows, software vendors have started collaborating with each other and with foundries offering the fabrication processes resulting in several standardization and collaboration activities. First, there is the collaboration between Filarete, PhoeniX Software, PhotonDesign, and the Technical University of Eindhoven that started in 2007 and resulted in the creation of the PDAFlow Foundation in 2013, which is a not-for-profit organization for the development, support, and licensing of standards for photonic design automation [40].

In autumn 2015, the PDAFlow Foundation has OptiWave, Synopsys-OSG, Lumerical, VPIphotonics and WieWeb Software as members, in addition to the four founders. The main results of this collaboration are the development of a standard interface (API) to allow interoperability of software tools and the creation of a standard for defining PDKs, resulting in more than 300 designs being made and fabricated over the last 2.5 years based on these PDKs and compliant tools within multiple foundries around the world. Also, the developed standards are being used by a broad range of both commercial as well as academic organizations to streamline their internal design process.

4.6 The Need for an Optoelectronic Unified Design Flow

Today, scalable, SPICE-like optical simulation is still in the early stages but has made great strides. To move forward, we need industry agreement on required device parameters. Design rule checking can be done with existing capabilities, but will necessitate a proliferation of coding practices to avoid the likelihood of generating large numbers of false errors. Current LVS tools can already check and identify shorts and opens for silicon photonics. Device checking is more complex but possible. However, interconnect parameter checking will require new infrastructure that has yet to be developed.

Mentor Graphics has been working with a number of partners to support silicon photonics designs. The Pyxis Wave reference package provides extended features for silicon photonics PDK development, including tiered custom pcell loading, waveguide routing to enable a full SDL flow, and an NDA-neutral silicon photonics

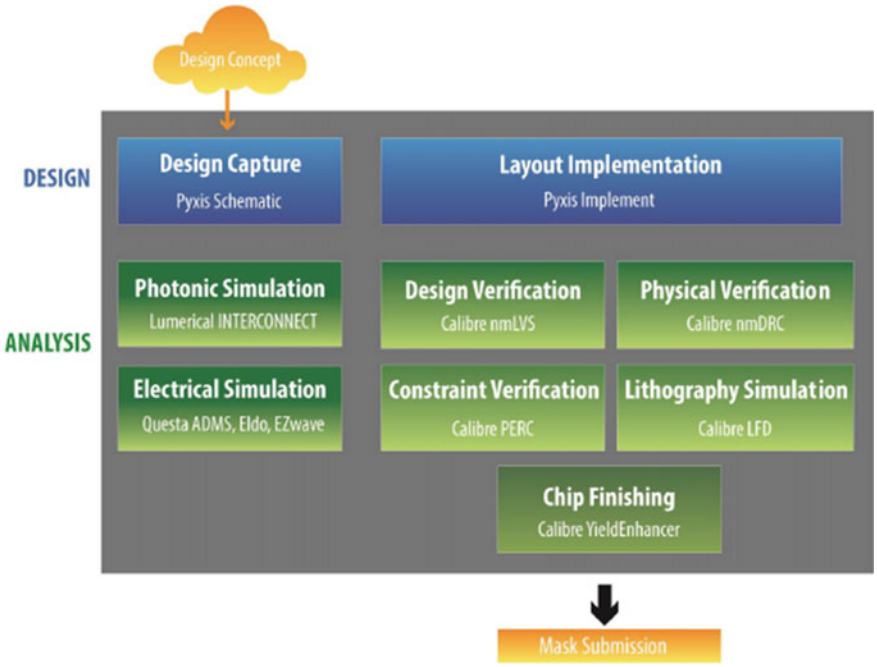


Fig. 4.22 Mentor Graphics/Lumerical Solutions integrated photonic design flow

PDK (created by University of British Columbia). The tools work in conjunction with PhoeniX Software's OptoDesigner to provide dedicated photonic creation capabilities. Interfaces to electrical and mixed-signal simulators, such as Eldo® and Questa® ADMS, allow designers to export Pyxis™ Schematic captured designs to Lumerical INTERCONNECT for simulation analysis. Physical verification tools, such as Calibre® nmDRC™, Calibre® nmLVS™, Calibre® LFD™, have been enhanced to enable verification of silicon photonics within the IC design verification process flow as shown in Fig. 4.22.

As with the electronics world, there are no single suppliers that can solve all photonics design automation problems and even if there were, there are still no EDA vendors who can solve all electronic design automation problems. Given that designers are integrating electronic and photonic designs, it seems certain that they will be using design flows comprised of tools from a combination of vendors. A good example of this today is, with Mentor Graphics, an electronic design automation supplier who supplies two different platforms for custom IC design. Their Pyxis platform runs on the Linux operating system, and their Tanner platform runs on the Windows operating system. On the Pyxis side, Mentor has integrations with Lumerical Technologies [33] and PhoeniX Software photonic design automation tools. On the Tanner side, Mentor has integrations with Luceda and PhoeniX Software photonic design automation tools. As is usually the case, these

combinations of tools are customer driven. The likelihood of a single unified design flow is low, as competition conventionally drives innovation and gives customers more and more productivity as time moves on.

Other photonic-based software tools and their providers include Aspic by Filarete [41], OptiSPICE by Optiwave Systems [42], PICWave by Photon Design [43], and VPIcomponentMaker Photonic Circuits by VPIphotonics [44].

4.7 Summary

In summary, integrated photonic design progression is similar to that of electronics design with a progression from discrete products to more highly integrated circuits. As electronics have scaled over the last three decades, integrated photonics will need to blend into the already established electronics design and manufacturing ecosystems. There are a great number of similarities between photonics and electronics, and the industry would be wise to learn from the electronics industry in these areas. There are also many challenges ahead that are unique to photonics, and the industry would be wise to focus its scarce resources on those areas to accelerate the adoption of this exciting technology.

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Chapter 5
Hardware–Software Integrated Silicon Photonics for Computing Systems

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Abstract A wealth of high-bandwidth and energy-efficient silicon photonic devices have been demonstrated in recent years. These represent promising solutions for high-performance computer systems that need to distribute extremely large amounts of data in an energy-efficient manner. Chip-scale optical interconnects that employ novel silicon photonics devices can potentially leapfrog the performance of traditional electronic-interconnected systems. However, the benefits of silicon photonics at a system level have yet to be realized. This chapter reviews methodologies for integrating silicon photonic interconnect technologies with computing systems, including implementation challenges associated with device characteristics. A fully functional co-integrated hardware–software system needs to encompass device functionality, control schema, and software logic seamlessly. Each layer, ranging from individual device characterization, to higher layer control of multiple devices, to arbitration of networks of devices, and ultimately to encapsulation of subsystems to create the entire computing system is explored. Finally, results and implications at each level of the system stack are presented.

5.1 Silicon Photonic Systems: A Subsystem Rationale

Silicon photonics, with their CMOS compatibility and small size, weight, area, and power consumption, have the capability of accommodating growing volumes of computer data arriving in real time and at very high rates in large-scale distributed computing systems. The wavelength and spatial multiplexing properties of optics

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are beneficially translatable to executing critical bandwidth and communications-intensive connections between increasingly parallel computational resources.

Chip-scale optical interconnects that employ novel silicon photonics devices can potentially leapfrog the performance of traditional electronic-interconnected systems. Silicon photonic interconnect technology is particularly promising for delivering energy-efficient system-scale data movement with extreme bandwidth densities [1]. However, while small-scale integrated silicon photonic devices have been demonstrated in recent years with high-bandwidth and energy-efficient performances, the benefits at the system level are yet to be realized. Simply maintaining the current electronic network architecture and implementing a wire-for-wire replacement of electronic to photonic interconnects will not realize the performance gains possible with optically interconnected systems. Transcending this gap requires innovative system architectures with intrinsically different organizations that can exploit the unique benefits of the potentially two order of magnitude increased bandwidth, along with other noted benefits like distance indifference and wavelength division multiplexing (WDM).

Physical layer functionalities of silicon photonic devices, such as modulators and switches, are naturally extended using integrated hardware control and software management. Chip-scale test, measurement, and validation of high-speed communications systems employing silicon photonics are requisite of hardware–software integrated silicon photonics for computing systems. Beyond simply testing a silicon photonic device to understand its elementary characteristics or operation, a validation process further pushes silicon photonic devices to operate in optical networking and computing scenarios as individualized subsystems. Furthermore, combining chip fabrication with electrical and optical packaging, as well as with system-level operation principles, allows the achievement of ubiquitous optical subsystems with networking capabilities, and subsequently advantageous insertion of hardware–software integration.

In this chapter hardware–software integration is referred to as a means through which hardware—physical layer optics such as modulators, filters, and switches, as well as electrical physical layer components such as transceivers and control loops—is encapsulated as individual subsystems whose functionality is abstracted into software.

5.2 Chip-Scale Silicon Photonic Subsystems

In this subsection, general approaches to applying manufactured silicon photonic subsystems are discussed. This includes how components involved in silicon photonic links are created, and ultimately how advanced silicon photonic networks for computing can be achieved. The need for packaging techniques—required to effectively interface to silicon photonic components both optically and electrically—is also highlighted. This elaboration of silicon photonic chip manufacturing and packaging are the two key components in the physical layer hardware realization process that precludes any hardware–software integration.

5.2.1 Silicon Photonic Manufacturing Platforms

Leveraging the investments made in complementary metal-oxide-semiconductor (CMOS) fabrication, it is possible to build high-complexity systems in silicon that achieve close integration between electronics and photonics, at relatively low cost. In recent years, with a growing number of individual optical devices fabricated, efforts have shifted toward larger scale subsystems integration. Inspired by the fabless semiconductor model, industrial foundries (IMEC, Singapore IME, etc.) offer multi-project wafer (MPW) fabrication, permitting various users to simultaneously fabricate custom architectures. Foundries provide process design kits (PDK) that typically include a library of individual devices. Passive devices include low-loss waveguides, Y junctions, waveguide crossings and grating couplers, among others. Active devices may include high-speed Mach–Zehnder modulators (MZM) and microring modulators and germanium (Ge) photodetectors [2].

These devices are typically based on silicon on insulator (SOI) wafer with 1–3 μm buried oxide layer thickness for efficient optical mode confinement. For chip-scale interoperation, grating couplers and nanotaper waveguides are used for surface and edge coupling, respectively. Fabricated devices have shown good performance parameters in a 30 GHz photonic system platform [3], including channel waveguides of 0.4 dB/cm loss, waveguide crossings with 0.18 dB insertion loss, MZM, and microring modulators with 40 Gb/s OOK data rate, and inductive peaking Ge photodetectors with 58 GHz receiver bandwidth.

5.2.2 Photonic Packaging

Photonic device packaging—both optical and electrical—contributes to a fair amount of overall system cost and complexity. Optical packaging of photonic devices faces several challenges, the most prominent being micrometer-scale alignment tolerance due to the mode mismatch problem. In addition, for volume production the packaging process needs to be passive and automated to address the cost issue [4].

Test and measurement approaches for interfacing with silicon photonics at the chip scale consist of precisely controlled spatial translation stages that are typically required for optimal light coupling in and out of the chip, as shown in Fig. 5.1. Edge coupling often requires a spot-size converter for efficient mode matching between on-chip waveguides and coupling fibers. Grating couplers are used for vertical coupling to specific silicon photonic structures on the surface of a chip die; these can be placed anywhere on a chip die, making such technology highly compatible with wafer-scale testing. The need for micrometer-scale precision optical coupling—on the order of silicon photonic device dimensions—is mitigated via optical packaging techniques, which directly bond either edge or surface

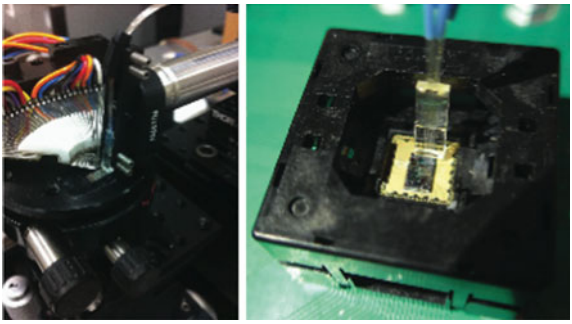

Fig. 5.1 (*Left*) a grating coupler and electrical probing laboratory test and measurement setup; (*Right*) a silicon photonic die wirebonded to a QFN electrical chip carrier with bonded grating fiber array, placed in a QFN chip socket soldered to a PCB

coupling components directly to the chip via curable epoxies or similar bonding techniques.

Similarly, electrical packaging at the chip scale consists of electrical wirebonding, with bonds that are impedance matched to the individual photonic device requirements. Such matching is performed to ensure minimal electrical reflections between an electrical driving source and the photonic device, in terms of both frequency matching and power transfer. A comprehensive review of optoelectronics packaging can be found in [5], and an example of optical and electrical packaging is shown in Fig. 5.1. Chip-scale packaging techniques facilitate silicon photonic computing systems, and subsequently hardware–software integrated approaches, because photonic subsystems with essentially standard hardware interfaces can be achieved. Such subsystems methodologies will be explored further in this chapter.

5.2.3 End-to-End Connection in a Silicon Photonic Link

In communication applications, silicon photonic devices are organized in such a way as to create one or more photonic links. A single photonic link consists of a transmitter, a transmission medium, and a receiver to achieve an optically delivered data connection. The transmitter includes a laser and one or more modulators, while the receiver includes one or more photodetectors, and a demultiplexer if several parallel wavelength channels are exploited. The transmission medium can range from a single straight waveguide to a complex architecture consisting of many straight and bent waveguides, as well as waveguide crossings.

Because silicon as a bulk semiconductor material has an indirect bandgap, efficient lasing is not possible without the introduction of a phonon. Nevertheless, several important approaches to lasing on silicon have emerged in recent years, including silicon Raman lasers, hybrid III-V laser on silicon operating at room temperature, and hybrid silicon microring and microdisk lasers [6].

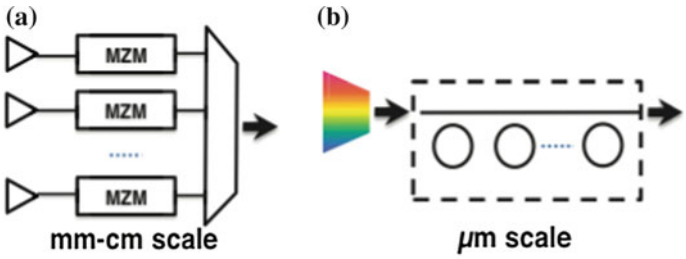

Fig. 5.2 WDM modulation scheme based on **a** MZM and **b** microring modulator structures

The most common methods for modulating light consist of Mach–Zehnder modulators (MZM) and microring modulators, and more recent developments include electro-absorption modulators (EAM) [7]. Modulation is typically based on the electro-optic effect in silicon, with *pn* junctions being the most prominent for high-speed modulation. Figure 5.2a depicts individual wavelengths that are modulated by separate MZMs, and are subsequently combined to create a wavelength division multiplexed (WDM) channel. Figure 5.2b shows cascaded ring resonators that are used to perform WDM modulation, where each ring individually modulates a wavelength channel on the WDM path. The latter type of modulation decreases the overall footprint of the silicon photonic architecture, but comes with a set of challenges [8].

Wavelength division multiplexing is often used to achieve higher aggregate data rates by superimposing several wavelength channels onto the same transmission path. WDM operation requires multiplexing and demultiplexing devices to combine and separate wavelength channels, respectively. Such operation can be realized on-chip via an arrayed waveguide grating (AWG) or a cascaded interferometric architecture in the form of Mach–Zehnder interferometers (MZI) or microring resonators.

A complex silicon photonic architecture can involve one or more optical switches. Switching is a desirable function in a silicon photonic computing system because several devices may be connected to form a network, requiring more than simple point-to-point links. Switching in silicon photonics consists of either spatial or wavelength-selective (individual wavelength) routing. In silicon photonic spatial switching, the whole set of wavelength channels present in the waveguide is driven in a given direction, whereas in wavelength selective routing, different sets of wavelength channels can be routed to different directions. Micro-electro-mechanical system (MEMS) switches have been shown to achieve high radices and microsecond-scale switching times [9]. MZI and microring switches based on the electro-optic effect have been shown to offer nanosecond-scale switching [10].

Photodetectors have the functionality of converting signals from the optical domain to electrical domain, and have performance metrics characterized by a few key parameters such as responsivity, dark current and E/O bandwidth. Germanium can be grown on silicon in an epitaxial fashion, and has become the preferred

light-absorbing material. Other structures such as defect-enhanced all-silicon photodiodes have also been demonstrated for in-waveguide photodetection [11].

5.2.4 Systems Enabled by Programmable Logic Devices

Connecting the individual silicon photonic components with real applications and evaluating the system performance remains a relatively untouched field. Individual silicon photonic device control, including thermal stabilization and link setup and connection maintenance are required for system-level evaluation. Field-programmable gate arrays (FPGA) offer a programmable logic-based platform with the capability of implementing dynamic, high-performance control logic applicable to silicon photonic interconnects for computing systems. The flexibility and performance of FPGAs for control also allow for interfaces to high-speed transceivers, making a FPGA system a promising test vehicle for demonstrating silicon photonic computing systems. The functionality of FPGAs, with specifically implemented logic designs, can be optimized and fabricated as an application-specific integrated circuit (ASIC). This optimization offers reduced electronic device footprint and power consumption, as well as the potential for close-knit integration with CMOS-compatible photonics in a 3D architecture [12].

It is both feasible and effective to implement a software execution stack together with programmable logic. As a standard approach in embedded systems, software can be used to describe underlying system hardware functionality. One such example is a control loop required to thermally stabilize a silicon photonic device. In this way, software can maintain control parameters and perform simple decisions based on changes in these parameters. Software can also be integrated to provide more sophisticated system functionality, where the states of several hardware subsystems are reported to software concurrently, and the software must perform some calculation/transformation to provide a decision based on the interaction of these parameters. Such software includes one or several interfaces for applications to make requests that either monitor or interact with the state of the underlying hardware.

Hardware–software integration provides several layers of interaction between silicon photonics and electrical computing devices, from abstracted control of individual devices in a network to providing a computing application with knowledge of or influence over hardware. Generally, hardware–software integration for silicon photonic computing systems serves as a method to streamline the functionality of silicon photonic devices in a system, and to include this streamlined functionality in inherently software-oriented applications.

5.2.5 System Considerations

While significant research efforts have been made on the performance of individual components as a parametric feedback approach for optimization, system-level demonstrations of optimal link and network performance are lacking. In some cases, this means some device characteristics are overlooked during individual characterization that could impact device operation in a full system. Characteristics such as microring-related performance dependencies will be explored in Sect. 5.4. In other cases, breakthrough performance of an individual device could be insignificant when implemented as part of a full system. The potential performance benefits offered by nanosecond-scale silicon photonic switching might be overshadowed by the performance of electrical link components—such as clock and data recovery and synchronization—that exhibit more than microsecond-scale setup time [13].

5.3 Device Control for Thermal Stabilization

Most integrated optical devices exhibit some vulnerability to temperature changes, mainly due to the thermal sensitivity of materials' refractive indices. Temperature variation can be due both to the device itself (internal causes) and to the surroundings (external causes). In a computing environment, computing-related effects such as CPU activity can generate temperature fluctuation. It is therefore important for a silicon photonic-based computing system to be able to account for, and subsequently counteract, thermal fluctuations to guarantee the proper operation of individual devices as well as the global system.

The high thermo-optic coefficient of silicon, combined with the resonant functionality of many integrated photonic devices, cause a persistent susceptibility to temperature fluctuations that impact the local and global system performance. Silicon integrated photonic devices often exploit these temperature-dependent, wavelength-selective resonance effects to achieve some functionality. However, wavelength selectivity of microring resonators in the presence of temperature deviations greater than 1 K will cause unwanted red- and blueshifting of the device resonance, rendering most silicon microring-based devices inoperable. This susceptibility of microring-based devices is not compatible with standard temperature fluctuations in the microelectronic environment, which can be an order of magnitude greater ($\sim$10 K) [14].

Temperature variations in a system are typically counteracted by means of constant heating and cooling to achieve a stable operation point. In the context of integrated optical devices, thermoelectric coolers (TEC) are often applied to balance out the temperature; however, TEC sizes cannot be reduced to current standards in device size. Integrated resistive heaters can be used only to heat a device, and pseudocooling is achieved by interrupting this heating process to allow heat to dissipate through the silicon substrate when *no other heating sources are present*.

Subsequently, a device whose local temperature is being controlled by an integrated heater is typically operated above the average temperature of the global system [15].

In order for an integrated heater to effectively stabilize the temperature of a microring resonator it must be interfaced with control circuitry. The goal of the control circuitry is to dynamically countertune the integrated heater against thermal fluctuations in the ambient environment, and can be performed using feedback control [16]. This control circuitry serves an additional purpose of rectifying potential fabrication issues inherent to individual devices using this established relationship between temperature and resonance [17]. In addition to thermally stabilizing the microring resonator, this control circuitry should be able to initialize microrings to operate from a larger system perspective by aligning relevant microring resonators with their corresponding laser wavelengths. This process is known as *wavelength locking* [18].

Temperature variations can be detected via direct measurements of the ambient environment using integrated thermistor measurements, similar to standard microelectronics approaches [19]. Another method is to monitor the input/output characteristics of a device or architecture according to absolute power level (in terms of amplitude) or absolute signal quality (in terms of successfully delivered bits), which also feeds into closed-loop control subsystems [20]. In both cases, measurements are translated to integrated heater control, by means of discrete analog electronics [21] or logic-based digital electronics [22], resulting in a closed-loop control subsystem. In the latter case, temperature measurements are sampled and quantized using analog-to-digital converters (ADC), heating requirements are calculated digitally, and heater voltages are generated by digital-to-analog converters (DAC).

Dynamic wavelength-oriented operations can be achieved by taking advantage of the integration of device characteristics and logical control in a silicon photonic multi-device architecture. With a standard hardware interface, this functionality can be encapsulated to implement software programmability. Dynamic hardware–software integrated wavelength routing and locking for computing will be explored in the later section of this chapter.

5.4 High-Speed Silicon Photonic Subsystems

In this section, the efficacy of both Mach–Zehnder and microring-based silicon photonic subsystems particularly for modulation and switching is explored. These integrated structures and operations are highlighted as representative subsystems depicting high-performance operation for computing systems.

5.4.1 Traveling-Wave Mach–Zehnder Modulator and Microring Modulators

There has been considerable research and development both in academia and industry on high-speed silicon photonic modulators. Demonstrated performances are beginning to approach optimality bounds in terms of modulation speed, pushing already present efforts toward commercial products.

Mach–Zehnder modulators (MZM) and microrings are prevalent structures for modulation, and have been demonstrated for high-speed modulation (>50 Gb/s on–off keying per channel), low driving voltage (<1 Vpp) and high aggregate data rate (>320 Gb/s) operation via WDM.

The MZM is generally considered the favorable modulator structure, compared to a microring-based modulator, due to its thermal insensitivity and robustness to fabrication variations. A few important parameters for MZM design are $V\pi$, insertion loss, and speed. The key component of a MZM is the phase shifter, which for high-speed (>25 Gb/s) operation is typically based on a reverse-biased pn diode structure [23]. MZMs supporting 50 Gb/s single channel operation and leading to high extinction ratio (>7.5 dB) and acceptable insertion loss have been reported [24, 25]. In order to achieve high-speed operation, the phase shifter is usually designed to be millimeter scale with optimized doping concentration while maintaining an acceptable insertion loss. A large portion of MZMs employ a "traveling wave" design, where RF driving signals are applied from one end of the optical device and propagate in parallel to the optical signal. In traveling wave designs, maintaining the phase matching between both optical and RF driving signal is critical to achieve maximum efficiency. Figure 5.3 shows an example of a traveling wave MZM with slow-wave electrode design. Due to the high RF effective index in this device, which translates to slow RF signal propagation, periodic optical delay loops are used between the device sections to realign the optical and RF phase [26].

The microring resonator-based modulator (MRM) has also attracted attention for chip-scale applications that require extreme bandwidth densities [27]. MRMs implemented in a modulator bank as depicted in Fig. 5.4, are capable of higher wavelength density as compared to a MZM-based WDM modulator bank, due to the compact device footprint of MRMs. WDM using MRMs can be achieved by either modulating several wavelengths separately to later merge them into a single WDM channel, or through modulation of a WDM channel due to extreme wavelength selectivity. In contrast, MZM-based architectures require only individual wavelength modulation and post-combination to achieve WDM.

The major drawback of the microring structure is its sensitivity to temperature and fabrication variations. This drawback is remedied according to the thermal stabilization approaches described in Sect. 5.3, and motivates hardware–software integration.

Figure 5.4 shows an example of an 8-channel WDM microring modulator with a total footprint of 0.5 mm^2 [28]. Each MRM is demonstrated at 40-Gb/s, resulting in an aggregate data rate of 320 Gb/s. Maximal frequency response is achievable—

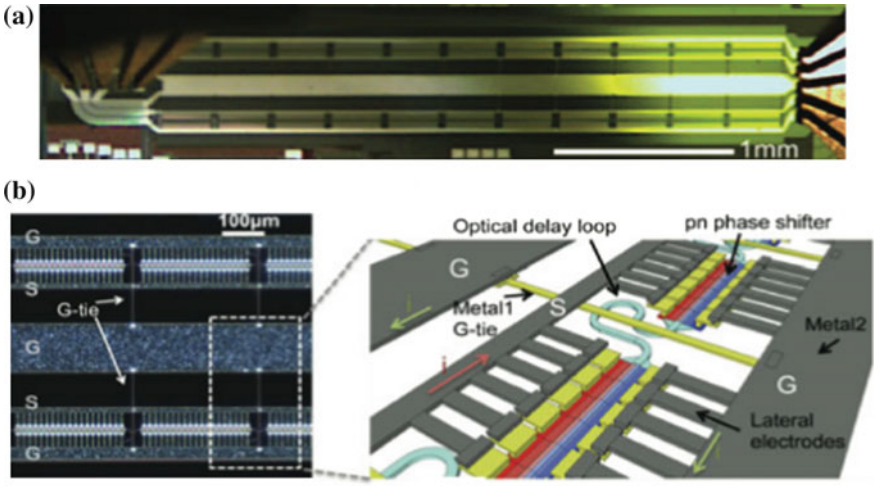

Fig. 5.3 **a** A traveling-wave MZM under probed testing: GSGSG probe on the *right* is for driving, and GSGSG probe on the *left* is for providing 50-Ω termination to each device arm, and **b** microphotograph of a section of the device, mainly top metal (Metal2) is visible. *Inset* (not-to-scale): Details near a ground-plane lateral connection (G-tie) and the optical delay loop for realigning optical and RF phase [26]

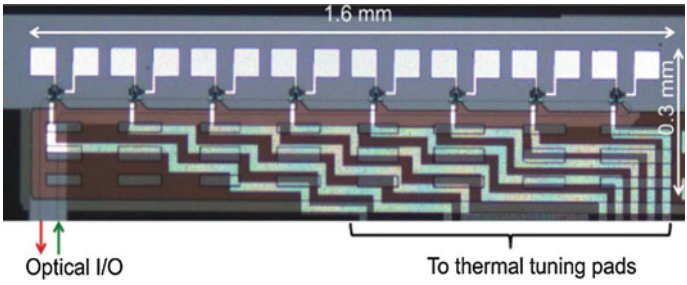

Fig. 5.4 Photograph of an 8-channel WDM microring modulator with each device capable of operating at 40 Gb/s [28]

with low voltage and ultralow power consumption—by optimizing a depletion mode modulator with a vertical pn junction structure instead of lateral or interleaved design [29]. Such a silicon photonic structure can be combined with hardware and software control methodologies and data delivery paradigms to achieve a hardware–software integrated subsystem for computing.

Both MZMs and MRMs have been shown to achieve more sophisticated modulation formats beyond simple on-off keying (OOK). Several methods for phase-shift keying (PSK) and quadrature amplitude modulation (QAM) employing Mach–Zehnder or microrings are reported in [30–33]. The ability to operate silicon photonic links with various modulation formats—achieved using advanced

photonic structures coupled to the appropriate electronic transmit and receive hardware—represent another avenue for hardware–software integration.

5.4.2 *Mach–Zehnder Interferometer and Microring Switches*

In a Mach–Zehnder interferometer (MZI), the phase of light in the two arms is controlled either electro-optically or thermo-optically. In this way, light can be switched to one of the output ports depending on whether constructive or destructive interference occurs. A simple MZI acts as a 2 × 2 switch—shown in Fig. 5.5—and switch fabrics with higher port-count can be implemented by interconnecting multiple 2 × 2 switch elements. As the time of this writing, state-of-the-art work has shown up to 32 × 32 switch fabric integrating 1024 MZI switches on an 11 × 25 mm^2 silicon chip [34].

In contrast to a MZI switch, the microring switch is a type of wavelength selective switch, as only the signal at the wavelength corresponding to the microring resonance is switched. Previously proposed 2 × 2 microring switching elements were composed of two crossing waveguides with two coupled microrings [35]. Each microring was responsible for switching data from one input port to the desired output port. From an architectural point of view, reducing the number of microrings in a switch matrix reduces the footprint, cost, and power consumption, as well as greatly simplifies the complexity of the associated control system of microring wavelength stabilization and locking [36].

In recent work, it was demonstrated that the 2 × 2 switching element (Fig. 5.6a) can be implemented with a single ring, thus reducing the number of microrings required for a given topology by half. As an example, to construct a 4 × 4 switch

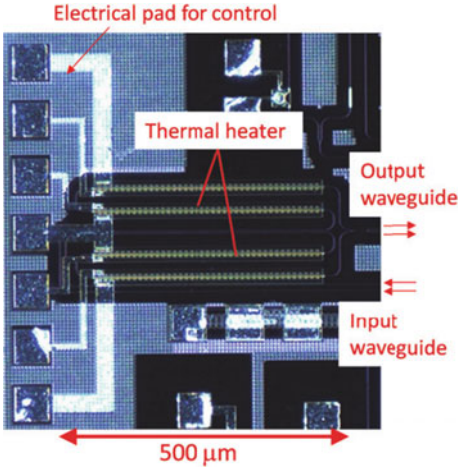

Fig. 5.5 Image of a 2 × 2 silicon MZI switch [50]

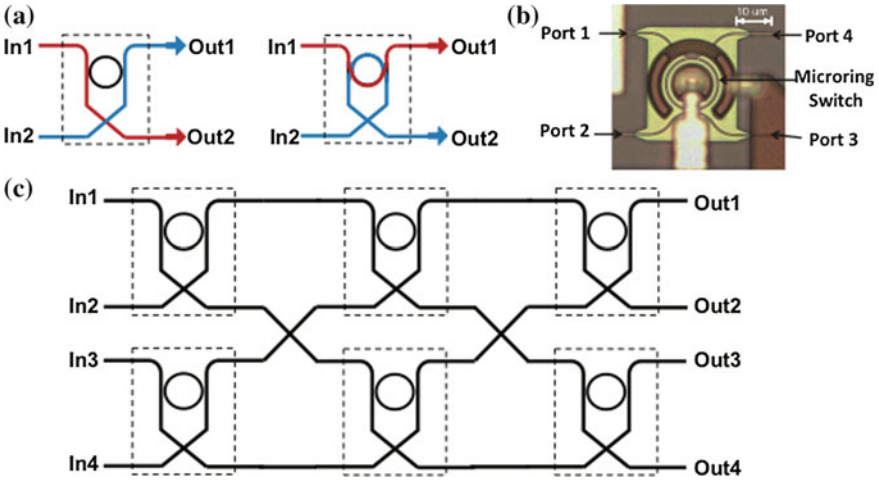

Fig. 5.6 **a** 2 × 2 microring switch in two different states. **b** Image of single microring 2 × 2 switch. **c** 4 × 4 multistage switch with Beneš topology utilizing only 6 microrings [36]

fabric with Beneš topology, 12 microrings are required using the conventional 2 × 2 switch. However, using a single microring as the basic 2 × 2 switching element, only 6 microrings are needed (Fig. 5.6c). A compact, single-device silicon microring-based 2 × 2 switch, with the capability of switching data streams from two input ports simultaneously has been demonstrated in [36], verifying the single microring as a 2 × 2 switch.

Multistage, multi-device switches are exemplary of silicon photonic subsystems for hardware–software integration. Combining individual device control—implemented as hardware logic—with software interfaces provides a network-centric silicon photonic hardware–software integrated subsystem. Such integration for computing systems is explored further in Sect. 5.5.

5.4.3 Microring Performance Dependencies

Resonant silicon photonic devices exhibit performance dependencies to injected optical power level, data format, and data density. Considering these dependencies with regard to silicon photonic subsystems is critical in hardware–software integration. Beyond a certain power level, silicon waveguides are more susceptible to nonlinear phenomena such as two-photon absorption. Absorbed photons result in increased temperature, resulting in refractive index shift and subsequent alteration of the desired device properties [37], and potentially affecting system operation.

As modulators, microrings are one of the first elements in the optical link, and the optical power (per wavelength channel) present at each modulator is of

particular interest. To ensure appropriate optical power is available at the receiver after traversing all components in the optical link, the optical power at the modulator must be allocated appropriately while still avoiding nonlinear effects. Data quality when modulated using a MRM degrades gradually with increasing optical power, primarily due to resonance shift induced by two-photon absorption [38].

Long sequences of consecutive ones and zeros in the modulated data can engender thermal fluctuations to which MRMs are sensitive [39]. Depletion mode microrings are shown to have minimal pattern dependence while injection mode microrings are more susceptible to modulation pattern.

The density of data-carrying wavelengths in a WDM channel is important for both microring modulation and switching. As the density of WDM signals increases (equivalently, as the channel spacing is decreased), the resonant frequencies of neighboring rings begin to overlap. As a consequence, each wavelength is not only affected by its corresponding microring modulator, but by spectrally adjacent modulators as well. This intermodulation crosstalk therefore limits the WDM channel spacing density, with current experimental results indicating nominal WDM channel spacings of 100 GHz and 50 GHz for modulation at 10 Gb/s [8].

5.5 Data Synchronization for Link-Based Delivery and Management

High-speed data delivery in dynamic systems—exemplary of but not limited to computing and network systems such as high-performance embedded computing and datacenter networks—tends to exhibit burst patterns. In the context of silicon photonic interconnected computing systems, the exact profile (timing and arrival) of the data is further complicated by the control and arbitration required to establish a successful path for data propagation. While such data delivery patterns and mechanisms can be achieved in the physical layer by underlying switching and routing capabilities, the ultimate execution of data signaling is a combination of establishing optical connections through synchronization, transceiver capabilities, and link quality, which can all be encapsulated and managed in software.

5.5.1 Burst Mode Data for Link Connections

Burst mode transmission is defined as: a surge of data at high rate, transmitted over a short period of time. In the context of a networked computing system, burst transmission refers to the delivery of network data from source node to destination node that is repeatedly interrupted at either regular or irregular intervals. Conventional protocols that employ burst mode transmission vary depending on the devices intended to communicate—the mechanisms for sending burst data using

high-speed memory differ from those used to read/write a solid state drive (SSD) or peripherals on a PCI Express (PCIe) bus. Since the actual operation of burst mode transmission varies from one type of device to another, it is critical to understand that such transmission must be well defined for the application of interest.

Burst mode data is considered for silicon photonic interconnection systems because of its correlation with the behavior of optical links: connections that can be established to send dense, high-speed information with minimal distance-dependent loss for a given period of time the connection is active. This active connection—otherwise referred to as a circuit—and its behavior is of particular interest due to concerns of link efficiency [27]. This efficiency includes overhead of link control subsystems and link utilization, which can be optimized with intelligent hardware–software integration.

Various optical connection behaviors can be achieved in circuit-switched or packet-switched architectures, which primarily translate to physical layer paths established in a silicon photonic switch architecture, and the rate at which such paths are interrupted or otherwise controlled. The dynamicity of these physical paths used as connections calls for some level of abstraction to allow higher layers of the system to understand and subsequently control underlying physical layer operation.

5.5.2 Synchronization

While the specific operation of data delivery protocols in computing systems—one fairly ubiquitous mechanism that utilizes burst mode transmission is direct memory access (DMA) [40]—and the principles of hardware and software communication will not be covered here, two key approaches to control mechanisms for burst mode delivery in silicon photonic interconnected computing systems will be explored [41]. Additionally, the reader is left to explore the fundamentals of data addressing and arbitration; standard mechanisms for Ethernet and flow control are a good starting point.

As one could surmise, a computing system with various pieces of data of different sizes, which may or may not need to be delivered from the same source to the same destination, requires a layer of control to ensure successful delivery. The concept of synchronization dimensionality imposed in [42] is upheld here; however, the systems described here only consider *non-blocking* control. This means that an interconnect will not be interrupted during transmission of data to handle synchronization control messages. Systems that do not utilize complicated control deliver data in a best-effort fashion, whereas verified data delivery systems employ synchronization. At a high level, in-band and out-of-band synchronization approaches will be explored, which allow nodes in a silicon photonic computing system to establish bidirectional connections where each node is aware of the presence of another node, as well as successful transmission and reception of data.

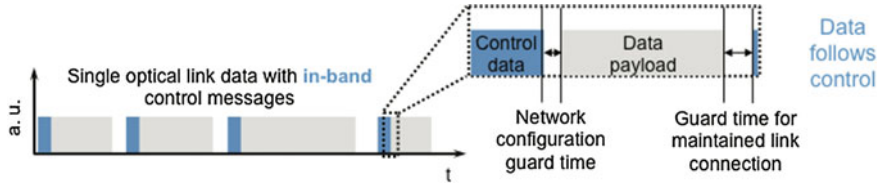

Fig. 5.7 In-band synchronization, including time-division multiplexed data payload and control messages for a "data follows control" synchronization scheme

In-Band Synchronization

In the context of a silicon photonic network in a computing system, in-band synchronization is considered to comprise of control information used to negotiate a connection, and is sent along the optical network path in conjunction with the data. Such control information shares the *same* optical path as the data in the optical connection, and consists of status messages that are used to negotiate these optical paths and negotiate successful data movement. It should be noted that to meet the full specification of in-band defined here, these control messages lead the data and must be transacted prior to initiating data transfer. This sort of transaction is depicted in Fig. 5.7, where control is time-division multiplexed with the data and must therefore be sensed and extracted accordingly. The exact mechanisms for combining data and control on a single channel will not be covered here, but the reader is encouraged to explore the various techniques found in [43–45].

A single static connection benefits from in-band synchronization because in most cases, minimal to no additional hardware is required to send and receive control messages. Control messages are separated from data and parsed *at the location of interest* to recognize requests and acknowledgments, and buffer them accordingly. When considering multiple connections, in-band synchronization requires monitoring of the wavelength channel of interest, and extraction of control messages that may come before or may be embedded in the delivered data. This means that to establish a path through a silicon photonic switch, information must be extracted from the optical path itself before it can be parsed to establish some switch configuration. Data flow through an already established path must therefore be interrupted to generate a new request to the switch, after which additional control messages are passed to/from the source and destination nodes.

The passing of control messages in-band is generally subject to the current state of the network, in that acknowledgments and requests handled by a destination node cannot properly transact until the network is configured accordingly. A connection reconfiguration in the time-multiplexed in-band case shown above is therefore blocked by the time left to handle a data transaction, and establishing a new data transaction is blocked by the time required to transact control messages.

Out-of-Band Synchronization

Out-of-band synchronization is comprised of control messages that are sent in conjunction with the data on a *separate* optical or electrical path. A separate optical

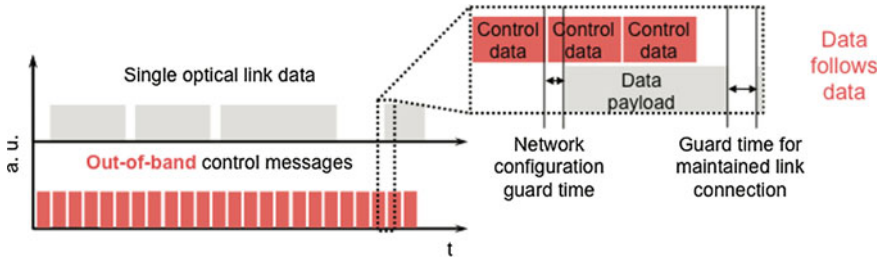

Fig. 5.8 Out-of-band synchronization, including data payload and control messages separated for a "data follows data" synchronization scheme

path means that messages used to make requests or acknowledgments may exist on a separate wavelength channel in a wavelength-multiplexed fashion, or may propagate through an entirely separate optical network. Similarly, an electrical out-of-band scheme requires an entirely separate electrical network. In each case, this additional messaging functionality requires either a more complicated silicon photonic architecture or additional electrical hardware. Nevertheless, the case for both the single static link and multiple connections remains the same in terms of the flow of data and control messages, which are inherently separated. Figure 5.8 shows transactions for a multiple-connection silicon photonic network architecture using electrical out-of-band synchronization, where multiple control messages are sent regardless of the current data transaction.

The out-of-band synchronization approach employs a separate network path for passing messages, and subsequently is independent of the current state of the network. Additionally, control messages can be delivered in parallel to data transactions. This creates complexity in terms of time synchronization for the out-of-band case that is naturally mitigated in the in-band case—meaning, additional logic is required to achieve ordering of control messages.

It should be noted that in-band and out-of band approaches that are explored here differ fundamentally only from the perspective of hardware implementation. From a software perspective, software algorithms must only be cognizant of the information that can be extracted from hardware. With enough abstraction, the same software algorithm can be used to schedule a network of links based on some metric, regardless of the underlying synchronization transactions. The interface to the hardware can differ in that one method may require more setup time or may require actuating fewer control registers; however, software abstracts the hardware functionality to provide primitives without underlining the exact physical hardware interaction, similar to concepts imposed for software-defined networking in data-center networks [46].

Frame Synchronization and Link Quality

What is common to both of the aforementioned synchronization approaches is the need to synchronize burst mode data over a connection, which is the core mechanism in establishing a burst mode data link. Synchronizing electrical transceivers

and clocks is commonplace in high-speed serial data delivery and is critical to a silicon photonic computing system. Clock and data recovery (CDR) mechanisms ranging from carrier sensing to simple line encoding, and even Manchester codes, allow separate nodes to synchronize their data in the time domain by recovering a clock signal. Generally, once a clock is recovered, transceiver synchronization is performed using a unique pattern (or frame) in the delivered data to allow a remote destination to understand that data is going to be delivered.

Such synchronization efficacy is subject to the quality of the optical path in a silicon photonic computing system. Physical layer control mechanisms described in earlier parts of this chapter can be used to tune the quality of the optical path to some optimal value, after which frame synchronization can be properly executed. The physical layer setup and status of the optical path—including spatial switching and wavelength stabilization for a switched, WDM silicon photonic network—can be abstracted in software, and used to communicate to the electrical transceiver synchronization hardware to ensure a stable link quality and successful data delivery.

5.5.3 *Exploring Software Protocols for Circuit-Based Connection Management of Characterized Links*

The efficacy of silicon photonic links for computing is considered in [47] according to the total time to simply synchronize source and destination nodes using CDR and a simple framing mechanism for transceiver synchronization. A software-implemented protocol is used to profile computing applications to be executed, which can be compared to an underlying silicon photonic link and make decisions on how often a particular optical connection should be reconfigured.

Figure 5.9 shows two test scenarios in which spatial switching and thermal initialization latencies are characterized in a piecewise fashion, coupled with FPGA-based transceiver synchronization delay originally demonstrated in [13].

Because of the circuit-switched nature of silicon photonic links, it is necessary to understand and manage the latencies associated with circuit setup and reconfiguration to avoid added delays to application execution time. This experimental system measures the circuit latency of a MZI switch, switching a WDM data channel on the order of single-digit nanoseconds, due to 1.022 and 2.156 ns rise and fall times, respectively. The latency associated with separating the WDM channels to individual wavelengths carrying 10 Gb/s data using a wavelength locking and stabilization control loop is between 200 and 500 μs. Burst mode data is synchronized over a stable optical path with average receiver synchronization—local clock recovery and data synchronization (CDR), as well as frame synchronization —time on the order of 2.635 ms. Measuring frame synchronization separately, the average synchronization time is 1.2 μs, indicating that receiver synchronization is primarily dominated by components in the electrical PHY such as clock recovery, and not necessarily the physical layer optics.

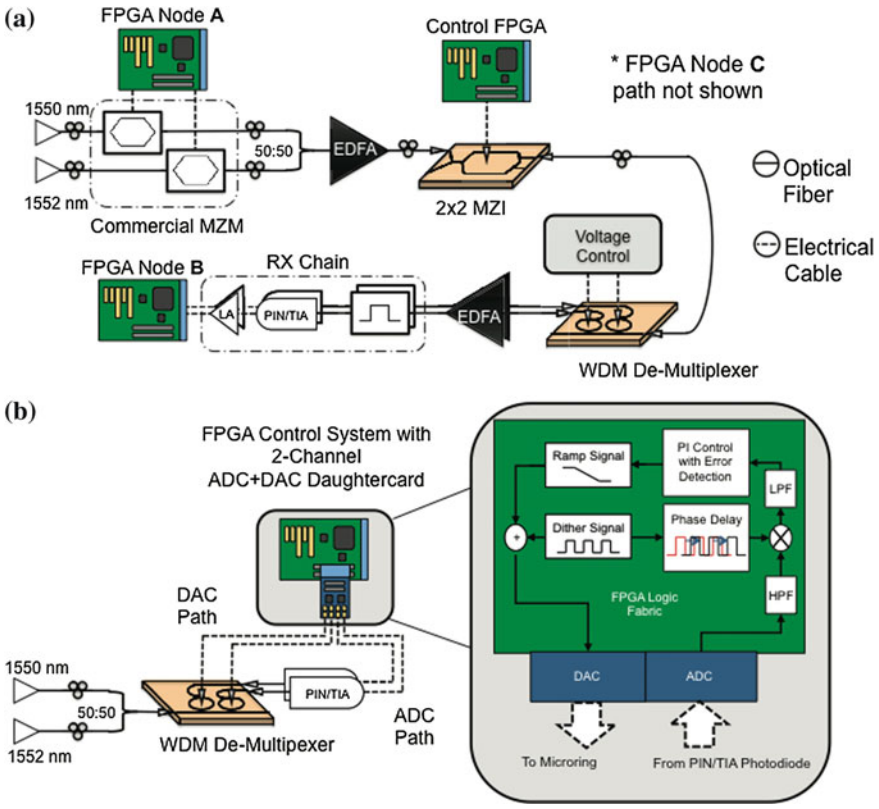

Fig. 5.9 **a** Spatial switching circuit initialization delay experimental testbed with FPGA-based transceiver synchronization characterization capabilities. **b** Thermal control-based wavelength initialization and synchronization experimental testbed with FPGA-based logical control

Due to the nature of this circuit setup latency with respect to potentially varying underlying silicon photonic architectures and electrical PHY hardware, it is necessary to devise methods to amortize the effect of this latency on application execution. A technique adapted from cache optimization relies on maintaining optical circuits based on their usage frequency. Such usage frequency is inversely proportional to the reuse distance of an optical circuit, which can be extracted from the temporal communication pattern of high-performance computing applications. Coupling this extracted metric with various prediction methods—including a previously introduced Markovian transition matrix method [47]—provides insight for how to optimize the rate at which predicted resources are successfully utilized through management-oriented circuit replacement policies.

Although the thermal initialization delay of silicon photonic devices is difficult to minimize due to the limitation of the silicon thermal constant [21], such a penalty can be overcome through careful architectural design. One such method is to explore the temporal locality in a computing application's communication pattern,

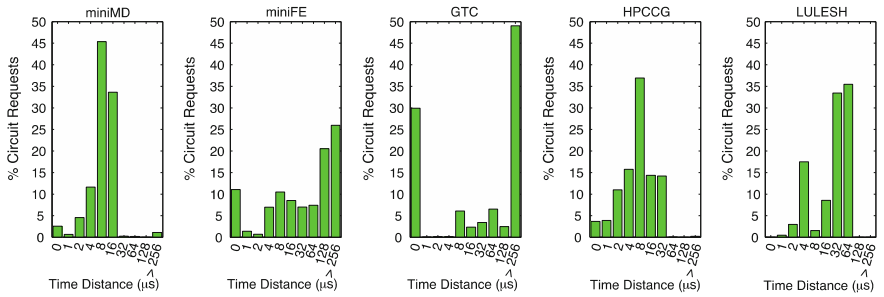

Fig. 5.10 Distribution of time-based reuse distances of scientific mini-app benchmarks (64 nodes). For miniMD, GTC and HPCCG, a high percentage of circuit reuses occur within 16 µs

where a source node could communicate with a destination multiple times within a short period. Figure 5.10 shows the distribution of circuit reuse distance, in the unit of microseconds, in several mini-application benchmarks that represent often-used scientific computation workloads. The results show a high probability that a source node will reuse its circuits within a small time interval. For example, scientific applications such as miniMD, GTC and HPCCG, show a high frequency for time distances less than 16 µs.

If the circuit corresponding to the requested destination can remain active, messages can be immediately transmitted, avoiding the circuit setup penalties. Taking advantage of temporal locality, a set of optical circuits can be maintained for the frequently accessed destinations, significantly increasing the probability of reusing a circuit and hence the application performance. Maximizing the number of reuses of these circuits also helps amortize their initialization overheads.

However, each application can lead to a different reuse pattern. Such difference is related to the application's communication degree (i.e., the number of nodes toward which a given node issues most of its traffic), as well as the application's communication behavior. Therefore, in maximizing reuse of optical circuits, application-specific software–hardware design is critical. One can imagine the union of a software-implemented, circuit replacement policy with the hardware-oriented circuit setup latency characteristics as a software management algorithm that monitors the status of hardware. Approaches that achieve such hardware-software integration will be discussed in the next section.

5.6 Hardware–Software Implementation for System Integration

To achieve a fully interconnected silicon photonic computing system, a combination of various subsystems must be able to communicate effectively. Each of these subsystems—modulators and multiplexers, switches, demultiplexers, filters, and

receivers—requires interfaces between physical layer optics, electrical control hardware, and software to achieve integrated system operation. To understand this entire system of subsystems, the individual silicon photonic devices and architectures needed to build a silicon photonic computing system, and the device-oriented characteristics that must be controlled to ensure proper device operation have been illustrated. Additionally, the communications flows for synchronization in actuating the physical layer link, control synchronization between nodes, and data delivery have been shown. This section addresses the complete hardware–software integration, building on the system architectures and the locations for opportunistic software control and optimization of silicon photonic computing system hardware.

5.6.1 *Abstracting a Chip-Scale Silicon Photonic System*

As developed in the previous sections of this chapter, the overall architecture of a silicon photonic interconnected computing system consists of circuit-based links with individualized silicon photonic subsystems to achieve various functionalities. An example of system-level abstractions for a chip-scale photonic computing network is depicted in Fig. 5.11, highlighting the insertion points for firmware-based logical control and software interfaces in both a node and on a network element. It should be noted that Fig. 5.11 does not suggest a particular network architecture or arbitration mechanism.

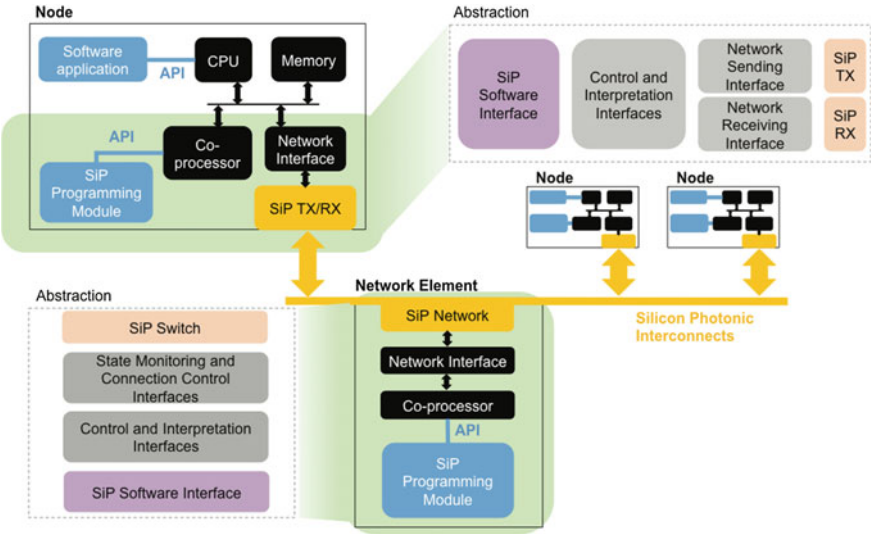

Fig. 5.11 Silicon photonic (SiP) hardware–software integration design, depicting interfaces between conventional electrical compute elements and software via APIs, as well as logical control in a coprocessor and network interface implemented as firmware for optical network hardware

In the node, firmware-based logical control implements a coprocessor specific to the abstracted silicon photonic network hardware. This coprocessor serves as an interface between hardware and software, interpreting software commands received from an application program interface (API) that abstracts the hardware functionality to a software interface. The coprocessor translates software to a form that is communicable with hardware, and may require reading and writing to local memory units, much in the same way that software translates to gate-level interactions in a CPU via an execution stack. A firmware-based network interface receives hardware-centric commands from the coprocessor, primarily through the use of dynamic registers. The network interface serves as a hardware controller to the silicon photonics, monitoring and actuating the optics appropriately, and provides high-speed serialization and deserialization of data propagating within the node from the CPU or memory. Additionally, the network interface includes hardware functionality to perform synchronization, as well as negotiate this synchronization with software through the coprocessor. In the case of out-of-band synchronization, additional interconnects not shown in Fig. 5.11 may be required.

Within the network element, the coprocessor also serves as an interface and interpreter between hardware and software, with abstracted silicon photonic functionality available through an API. The firmware-based network interface provides monitoring and requisite control hardware for the silicon photonic switching device (s), dynamically actuating and maintaining the state of the network element according to commands propagating from software. The network interface also includes arbitration hardware, negotiating with software through the coprocessor to establish the state of the network. It should be noted that in the case of a distributed arbitration architecture, the network element might be implemented within a node.

By extension of controlling this system with both hardware and software, unique functionalities of the silicon photonic network are encapsulated and abstracted. These abstracted functionalities are herein described as "primitives." These include network primitives such as reconfigurable and non-blocking end-to-end connections enabled by a silicon photonic spatial switch, multicast operations enabled by a circuit switch, and wavelength routing operations enabled by microring multiplexers and demultiplexers. So long as some unique functionality exists according to the silicon photonic architecture, and that functionality can be encapsulated using hardware–software integration, it fits within our definition of a primitive.

Figure 5.12 shows a four-node silicon photonic computing network testbed implemented at Columbia University, with an out-of-band electrical control message passing network implemented using JTAG/UART over USB, common to Altera Stratix V-based FPGA platforms on which the computing nodes are emulated. This is an example of out-of-band control in that nodes are made aware of requests and acknowledgments by passing messages through a host computer, over a virtualized electrical network defined by software. The network architecture shown here is centralized, but can be software programmed to implement distributed or centralized arbitration schema.

To set up an optical path—including multiple wavelengths on a WDM channel—and send computational data in this network, the flow of control and data from

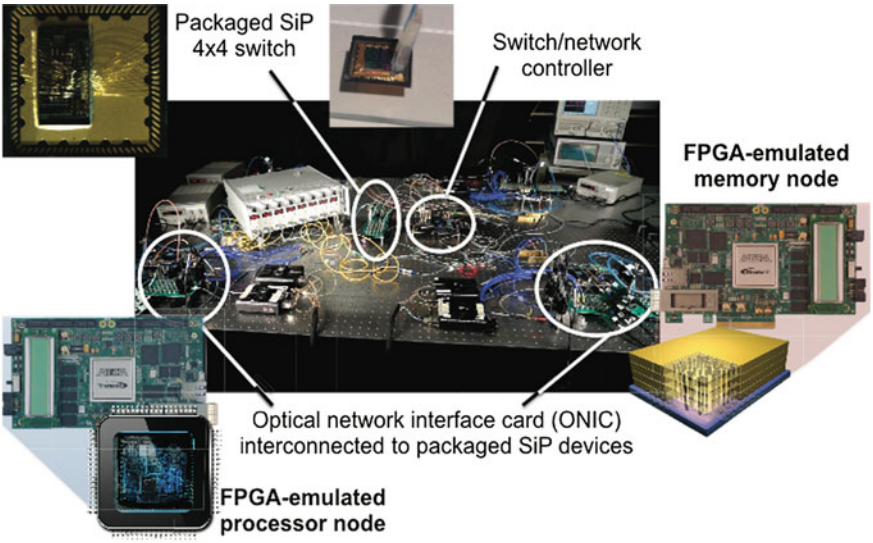

Fig. 5.12 Silicon photonic computing network implemented at Columbia University's Lightwave Research Laboratory, encompassing packaged silicon photonic transmission and receiving devices, a packaged 4 × 4 silicon photonic switch, and commercial off-the-shelf Altera FPGA development kits used for switch control and node emulation (CPU, memory, and ONIC)

one node to another with centralized arbitration follows the propagation depicted in Fig. 5.13.

Optical network interface logic implemented on an FPGA-based node within this system is known as an optical network interface card (ONIC) [48]. The ONIC logic depicted in Fig. 5.14 maintains control of local silicon photonic devices requisite of data delivery, hosts synchronization and arbitration logic pertinent to the mechanisms implemented in the network, and has an embedded coprocessor capable of executing a simple software stack for software integration at the node. This ONIC is one method to achieve the abstraction paradigm associated with Fig. 5.11.

5.6.2 Software Control and Management

In a system where several parallel computing entities contend for silicon photonic network resources, it is necessary to implement an arbitration mechanism to ensure proper data delivery. A scheduling algorithm can account for all abstracted silicon photonic network primitives in software, and translate the needs of network nodes to some network configuration. This scheduling algorithm can be implemented in either a centralized or distributed fashion—meaning, either a single network entity is aware of the state of the network as a whole, or several entities are aware of piecewise components of the overall state of the network. In the case of a central

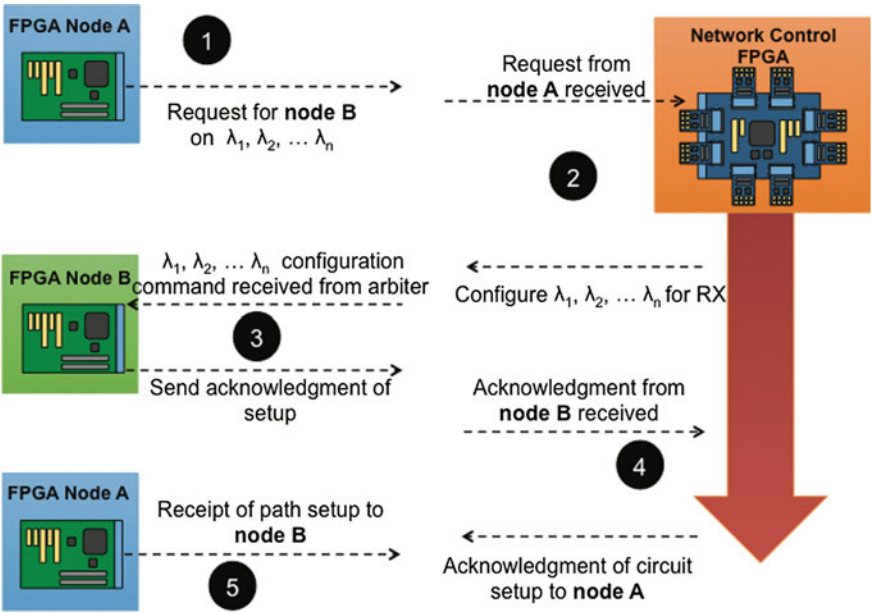

Fig. 5.13 Flow diagram of optical path setup between two nodes, depicting transactions to and from the nodes and sequential status including (*1*) node A's programming requests a link to node B through the central network controller; (*2*) the central controller checks the state of the network and reports the available path to node A; (*3*) node B prepares to receive on the wavelengths of interest; (*4*) the central controller updates the state of the network and node connections; (*5*) node A's programming is able to utilize the setup network path

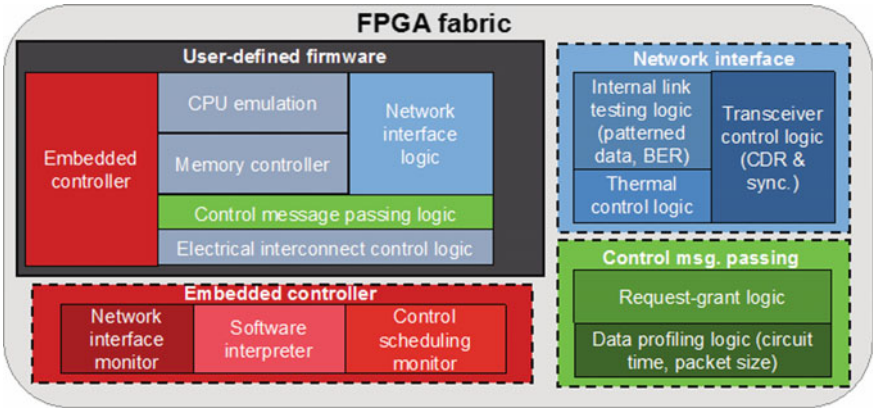

Fig. 5.14 Optical network interface card logic (ONIC) implemented in the logic fabric of a FPGA

network entity, this entity is known as an arbiter. Two main mechanisms for scheduling—request-grant based and predefined time-division multiplexing—both achieve sufficient network utilization, regardless of the underlying mechanism in which control messages are passed between network entities. Both mechanisms require the exchange of management information between the nodes in the system, but the key difference is whether or not this management information is handled by one node altogether, or by several nodes simultaneously.

Distributed Versus Centralized Arbitration

Regardless of the arbitration mechanism, whenever the connectivity of a node is greater than two and spatial switching is required to achieve this connectivity, there will be a switch on the optical path. The desired switch connectivity over time, i.e., which input is transmitted to which output, and for how long, is determined by the arbitration algorithm. The switch controller translates this connectivity into a switch state, determining the state of each individual switching element at any particular instance in time.

Centralized arbitration requires the ability for all nodes to exchange messages with a central arbiter. This form of arbitration is highly susceptible to single-point failure in that failure of the central arbiter results in failure of the entire system. However, it can achieve high total bandwidth utilization of all links and low configuration latency because all nodes are connected via a single hop. A centralized network hardware architecture is also shown in Fig. 5.15, where the central arbitration mechanism is hosted on a central entity in the network that controls a central switch. The central arbiter distributes grants to all nodes, and can also maintain synchronicity among nodes by distributing sync messages or an optical clock. Centralized arbitration, however, is not confined to only a centralized network hardware architecture, and can be implemented on other networks.

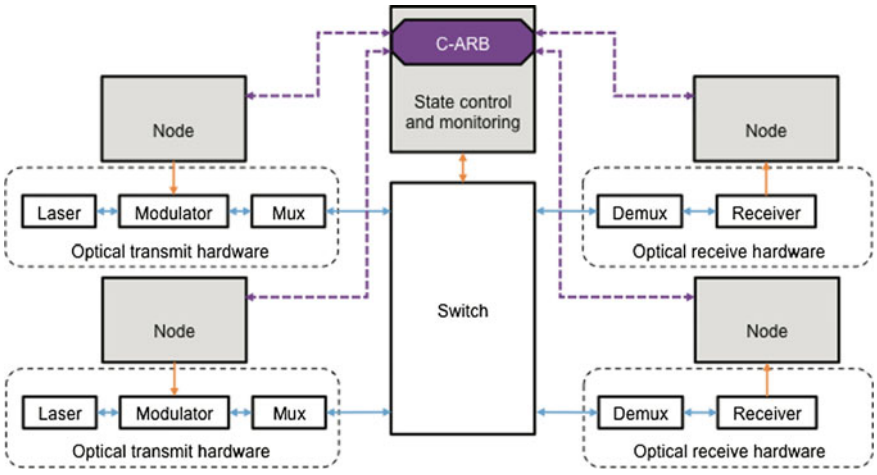

Fig. 5.15 Centralized arbitration (C-ARB) logical architecture implemented on a centralized network hardware with optical interfaces

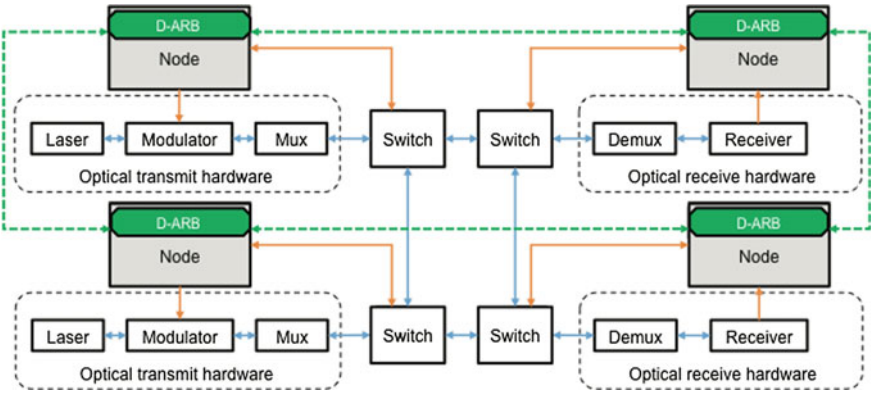

Fig. 5.16 Distributed arbitration (D-ARB) logical architecture implemented on a distributed network hardware with optical interfaces

Distributed arbitration is typically implemented when multiple nodes directly share arbitration information with multiple other nodes. In this architecture, all nodes maintain the same arbitration capabilities; however, they only maintain the state of local connectivity, and therefore must negotiate with local nodes to achieve global connectivity. This form of arbitration is more resilient to single point failures in that a single failure might not result in failure of the whole system. Simplified local architecture and complexity can be achieved at the cost of careful network topology and connectivity design and layout. Figure 5.16 shows the logical connections for a distributed arbitration architecture on a switched network. This arbitration architecture also exemplifies a distributed network hardware architecture, where each node controls a small switch that provides connectivity to other network nodes. Distributed arbitration, however, is also not confined to only a distributed network hardware architecture.

5.6.3 *Example of Software Request-Grant-Based Control of Switched Silicon Photonic Circuits*

The request-grant mechanism of a centrally arbitrated switch system with out-of-band control messaging is depicted in Fig. 5.17. The timing of the messages and data exchanges between two nodes and a switching controller is shown. Whenever a new connection is required, a node signals the central arbiter hosted on the switch controller via an out-of-band electrical network with a request message containing the destination node. The switch controller has a separate connection and port for each node to receive and buffer requests, meaning that there is no possibility for physical contention and only the need to synchronize based on the timing (and possibly priority) of requests. The arbiter algorithm generates a

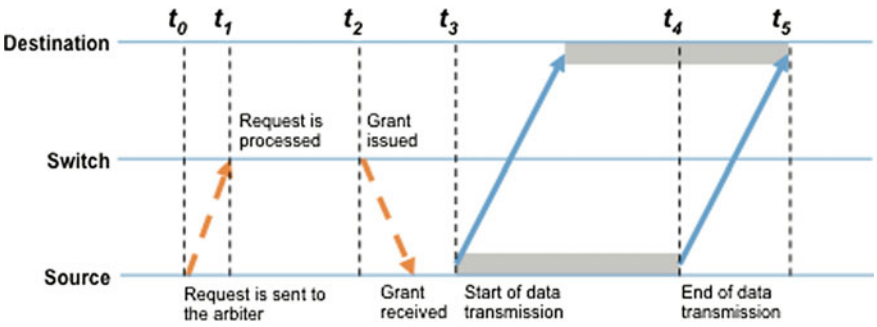

Fig. 5.17 Timing diagram of request-grant arbitration where a central switch hosts arbiter logic to grant a source node request to connect to a destination node. The total latency of the transaction, from the start of a request to the end of data delivery, is given by the interval (t_0–t_5)

corresponding grant that is also communicated to the node as a control message. Once the grant message is received the node starts to transmit information to the destination node for the time indicated in the grant. The timing of the grant message takes into account a certain guard time for the message to be received and processed by the node. In principle, the transaction time needed for each node can be measured precisely at initialization time. The request and grant messages contain the destination address because a node can send several requests for different destinations. Depending on the demand of the other nodes—including length of transmission—the arbiter decides which request to grant first based on a scheduling algorithm. While these messages might only contain requests for a single connection, network architectures can be deployed to achieve multiple simultaneous connections, therefore requiring multiple control messages or control messages containing multiple requests.

5.6.4 Control-Centric Integration: Power-Optimized Silicon Photonic Spatial Switching

Optical switching is often cited as a solution to a host of interconnect challenges present in the field of data communications—in particular, for datacenters and supercomputing [49]. While the silicon photonics medium has been shown to be a viable platform for optical switching [50], understanding the full breadth of silicon photonic-based optical switching exists largely at the level of functional device architectures; however, ongoing efforts aim to extract additional hardware operation of silicon photonic switches to achieve hardware–software integration through logical control. The first of these efforts entails translating power equalization techniques into intelligent spatial switching through a 4-input 4-output (4 × 4) silicon photonic switch fabric using Mach–Zehnder Interferometers (MZI) in a

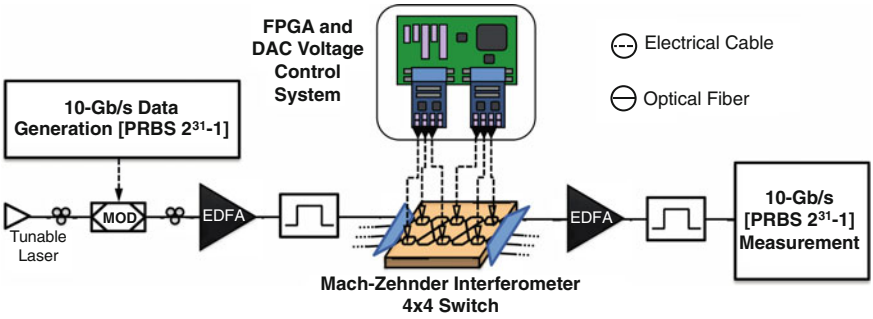

Fig. 5.18 Experimental testbed demonstrating firmware control of power-optimized silicon photonic switching

reconfigurable and non-blocking Beneš topology [51]. The experimental architecture is shown in Fig. 5.18.

The results of efforts examining intelligent switching are twofold: (1) they highlight the efficacy of control of individual devices in a switching architecture to achieve dynamic operation; (2) they highlight the susceptibility of successful system operation to device fabrication tolerances.

Experimental results show error-free data transmission through the switch fabric implementing the intelligent power distribution scheme. An initialization process is performed through a dithering signal technique on the arms of MZI elements to characterize device behavior through determined optical responses. Pathways are then set via FPGA controllers through digital-to-analog converters, resulting in full utilization of the switch fabric (Fig. 5.19).

Multi-node spatial switching offers the advantages of data communication with full connectivity. With high-performance computing centers having to support an increased influx of data, certain applications require the realm of network design that encompasses ubiquitous computing [52]. As a result of this one-to-all functionality, complexity of design considerations will likely increase, as well as the

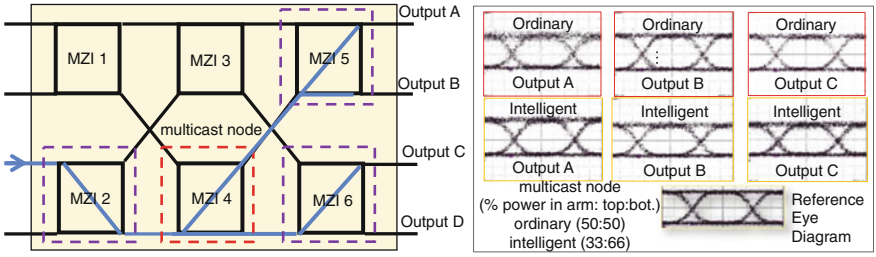

Fig. 5.19 Experimental results showing intelligent power distribution scheme via biasing of switch fabric through control plane. *Dotted lines* of 4 × 4 schematic indicate biased MZI stages, and eye diagrams on the *right* illustrate successful data recovery with variation in power allocation at the multicast node to allocate 50:50 versus 66:33 power ratio to either arms of MZI element

need for increased tolerances in inducing certain additional loss in the system and accounting for slight variability in loss along each of these pathways.

Multicasting across an optical switch fabric is demonstrated, illustrating a feature that can extend data center connectivity. Through this demonstration, it is shown that device-specific physical requirements can be converted into the logical domain. The aim is then to incorporate the device-specific physical demands into an abstracted software layer as part of the process of hardware–software integration.

5.6.5 *Network-Centric Integration: Programmable Wavelength Routing*

The ubiquity of microring resonators for silicon photonic interconnects is attributed to the device's small footprint and wavelength-dependent resonant functionality, which can be leveraged for effective modulation, switching, and filtering techniques requisite of end-to-end optical links. Translating these functionalities into primitives further highlights the benefits of using microring-based architectures at the systems level. Figure 5.20 shows a scenario where microrings in a de-multiplexer configuration were used to achieve arbitrary wavelength selection and routing through software abstraction of a dithering-based wavelength stabilization technique, with control parameters abstracted to software as *wavelength profiles* [53].

In this silicon photonic computing network, both laser tuning and wavelength routing are encapsulated as primitives that can be utilized in software, and subsequently in applications. Digital-to-analog converters (DAC) are coupled to

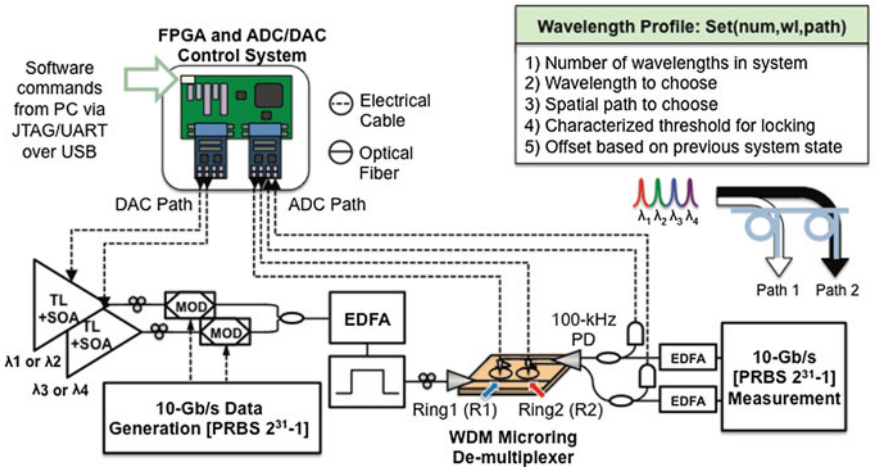

Fig. 5.20 Experimental testbed for software abstracted wavelength profiles for arbitrary wavelength routing on a silicon photonic demultiplexing device

electrical amplifiers to provide a programmable current source to the tunable lasers. The integrated heaters on each microring are connected to DACs in a similar fashion to tune their resonances, while analog to digital converters (ADC) are used on the drop ports of each microring to monitor specific low frequency (compared to data rate) control signals. Arbitrary wavelength routing is achieved in software by monitoring control signals propagating up through a JTAG/UART port in a C-based program. This program is able to first set the wavelengths available via the tunable laser. It can then determine the number of suitable wavelengths present in the system via a calibration process, and can subsequently choose which wavelength each microring can lock to via the encapsulated primitives. The wavelength profile for a certain network state depends on parameters shown in Fig. 5.20; 1, 2, and 3 are system parameters exposed through a software API, and 4 and 5 are system characteristics that are measured and stored for lookup. Parameters 4 and 5 are inherent to the silicon photonic subsystem's devices, and represent interactions between individual devices due to injecting light, heating, and manufactured device characteristics. Such parameter abstraction provides arbitrary and programmable wavelength routing with no significant impact on data quality as shown in Fig. 5.21.

It should be noted that the limiting factor here is the microsecond scale thermo-optic response of the silicon microrings. While this scheme is not as fast as broadband spatial switching techniques [36], it adds an additional layer of network functionality via wavelength routing, and can be used to extend a traditionally broadband circuit-switching optical interconnection networks. Additionally, programmable functionality can also be applied to optimized ASIC technologies, reducing the electrical component footprint and power consumption while retaining the same intelligent signal processing functionality.

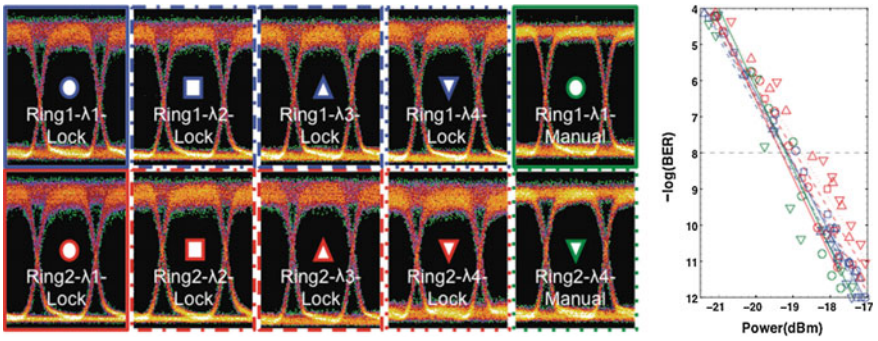

Fig. 5.21 (*Left*) Eye diagrams of a 10-Gb/s signal propagating through programmable wavelength-locked circuit scenarios; (*Right*) BER measurements

5.7 Conclusion

This chapter outlines a subsystem methodology for hardware–software integrated silicon photonics for computing systems, and exemplifies the possible roles for silicon photonics in future high-performance computing technologies [54]. By highlighting the engineering challenges in achieving hardware–software integrated silicon photonic subsystems, the need for system-level design is further emphasized.

The advantages of silicon photonic interconnect technologies are clearly translatable to the needs of high-performance computing. Adopting standard interfaces for controlling silicon photonics with both hardware and software offers advantages for system design. With software programming methodologies and standard interfaces that adhere to optimal computing and network behaviors, emerging silicon photonic devices and subsystems can be architected to function and deliver their aforementioned performance benefits at the system level. These benefits, with hardware–software integration, can be delivered in a way that is fully integrated with system software.

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Chapter 6
Path to Silicon Photonics Commercialization: The Foundry Model Discussion

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Abstract Silicon photonics will increasingly be adopted into commercial applications as the technology matures, and the demand for foundries is growing as companies search for photonic integrated chip (PIC) manufacturing support. The accessibility to foundries becomes a critical aspect for technology advancement and volume production. Foundry services for multi-project wafer (MPW) shuttles, customized process runs, and small volume production are discussed in this chapter. Results and challenges in setting up a CMOS manufacturing foundry line for silicon photonics research and development along with commercialization are also presented. The existing gap in the value chain presents an opportunity for foundries to be involved in a silicon photonics market that is primed for growth.

6.1 Introduction

Silicon photonics has become one of the leading technological solutions for integrated photonics that target applications such as optical communications (telecom/datacom), high-performance computing, optical sensing, and on-chip optical interconnects. Since then, the technology has reached new heights in terms of device performance, levels of integration, and circuit functionality. There is vast interest in the field and recent acquisitions of silicon photonics companies indicate

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an inflexion point for commercialization in the near future [1–4]. Some mega data centers are in transition using single-mode fiber infrastructure with silicon photonics in view. Many have been weighing the technology in full matrix analysis from the viewpoints of application volume demand, costs, reach, power consumption, data bandwidth, port count density, upscaling potential, and importantly the infrastructure readiness.

A key advantage of silicon photonics is to leverage the existing complementary metal–oxide–semiconductor (CMOS)-compatible foundry infrastructure and its technology advancement to fabricate an integrated photonics chip cost-effectively. CMOS technology dominated the microelectronics industry in the last 50 years by enabling complex low-power electronic circuits with high yields. The foundry lines typically produce high-volume CMOS production wafers on standard process flows where fabrication loading is generally in the thousands or tens of thousands of wafers *per month*, depending on the technology node. This is in contrast with the low anticipated initial volumes of silicon photonics wafers which are estimated to be hundreds to thousands *per year* collectively as an industry [5]. The discrepancy in wafer volumes suggests that further scrutiny must be exercised on how capital-intensive CMOS foundry infrastructure can be actually reused economically.

At this juncture of technology adoption, the availability of silicon photonics foundries becomes critical. Therefore, concerted efforts must be made to develop foundry lines for prototyping and chip fabrication in a high-yield manufacturing environment. In this chapter, we review the silicon photonics manufacturing line setup and related foundry efforts to advance the field alongside considerations of research and development needs.

6.2 Silicon Photonics Technology Status

6.2.1 Fabless Semiconductor Model

Silicon photonics has always been envisioned to be able to leverage existing CMOS infrastructure, and thus a fabless model is a characteristic of this industry. With fabless silicon photonics [6], the high cost and barrier to entry into market and technology is drastically reduced by avoiding the associated expense in maintaining a silicon fabrication facility. This enables companies, especially small start-ups, to concentrate solely on photonics integrated circuit (PIC) design and end-user product applications. To achieve this, the typical prerequisites are:

(i) Foundries that run stable and repeatable silicon photonic processes;
(ii) Design rules and verified device libraries with performance specifications pertaining to the process flows;
(iii) The availability of computer-aided design (CAD) tools for device/circuit simulation and design enablement;

(iv) A design platform that interweaves the CAD tools for simulation and layout to facilitate mask tapeout.

Items (ii), (iii), and (iv) are components of a typical process design kit (PDK) in a standard CMOS technology node. There are efforts to mesh silicon photonics software simulation tools together with traditional electronic CAD and layout tools to offer a more complete design platform. This topic is addressed in other chapters of the book for more in-depth understanding.

For the fabless business model to be effective, multi-project wafer (MPW) runs have to be initiated (See Sect. 6.3). These MPW shuttles reduce overheads associated with chip fabrication through the sharing of the costs for photomask and wafer processing. In the electronics industry, this has been well illustrated by, for instance MOSIS, an organization that administers MPW services from various commercial semiconductor foundries for electronics circuit design and innovation [7]. By setting up foundry lines to facilitate a fabless model, this will naturally reduce barriers relating to cost and accessibility for silicon photonics research and development, as well as manufacturing.

6.2.2 Monolithic Integration Through CMOS Photonics

For this discussion, monolithic integration is defined as photonic and electronic devices formed in the frontend-of-line (FEOL) steps of a standard CMOS transistor flow. Monolithic integration of silicon photonic devices and CMOS electronics was deemed as the "holy grail" of an integrated photonics platform back in the 1980s [8]. The motivation was to attain highly compact optical and electrical circuits with reduced interconnection parasitics at a lower cost.

Luxtera has been one of the major players in silicon photonics since 2001. It was the first to announce a CMOS photonics technology in 2006 based on Freescale Semiconductor's 0.13 μm CMOS silicon on insulator (SOI) technology node [8, 9]. From this technology enhancement, silicon photonics transceiver chips were fabricated to build a 40 G (4 × 10 G) active optical cable (AOC) product for datacom applications. This technology remains a closed platform with limited public accessibility. Since then, Luxtera's AOC business was acquired by Molex in 2011 [1], and subsequently, a collaboration with ST Microelectronics (ST) was announced in 2012 to develop a silicon photonics line at ST's 300 mm facility in Crolles, France [10]. More about this subject can be found in a separate chapter in this book.

Meanwhile, International Business Machines (IBM) further demonstrated photonics–electronics integration using a sub-100 nm CMOS SOI technology node in 2012 under its "Silicon Integrated Nanophotonics" program. Assefa et al. monolithically integrated optical modulators and Ge photodetectors into IBM's base 90 nm high-performance logic technology node [11]. Primarily, the employment of an advanced CMOS technology node enables the higher speeds from electronic

circuitry to match the PIC bandwidth. For the 90 nm CMOS integrated Nanophotonics platform, the transistor gate length was additionally scaled down to increase the electronic circuitry bandwidth for a stable 25 Gb/s optical receiver performance. There have been discussions on the general availability of this technology, as IBM's silicon photonics product design kit neared full technology qualification in 2014 [12]. And despite IBM not being a pure-play foundry, the recent acquisition of IBM's microelectronics business by GLOBALFOUNDRIES [13] opens up possibilities for a foundry service in future.

Both Luxtera and IBM required process modifications to the standard CMOS flow for photonics–electronics integration. Alongside these companies projects, monolithic integration of silicon photonics in a 65 nm dynamic random access memory (DRAM) technology [14], and a 0.18 μm CMOS technology [15] on bulk Si substrates were also reported. Going a step further, there has been a significant effort to integrate the photonic devices *without* process alterations in a Texas Instruments 28 nm bulk CMOS process [16], and, subsequently, an IBM 12SOI 45 nm SOI–CMOS process [17, 18]. This was motivated by efforts to use the existing CMOS process and foundry infrastructure as they were. Photonic devices such as polysilicon (and crystalline Si) waveguides, Si ring multiplexers (MUX), modulators, and SiGe detectors with CMOS electronics were demonstrated. In both CMOS technology processes, post-CMOS processing was conducted by locally removing the underlying Si using XeF_2 etching. This was done to eliminate losses associated with the optical coupling to the Si substrate due to a lack of a thick oxide layer beneath the optical devices. Overall, the absence of low-loss crystalline Si waveguides, optical implants for the active devices, and a suitable light detection material at telecommunication wavelengths makes it extremely challenging to build large-scale high-speed photonic systems in a standard CMOS flow without major process alterations.

In general, monolithic integration offers advantages for silicon photonics, but it also introduces complexity in process integration and in the codesigning of photonics and electronic circuitries. The starting substrate itself presents a fundamental difference in which CMOS SOI is optimized for transistor performance and low thermal impedance, while the photonics SOI uses a much thicker buried oxide (BOX) for optical loss reduction. As the critical dimension (CD) scales down for advanced CMOS nodes, there is a further mismatch in device dimensions between the transistors (<100 nm) and the photonic devices (0.1–1 μm). Hence, the photonics devices do not make efficient use of "expensive" wafer area or chip real estate in an advanced electronics node. In addition, two groups of devices with a CD of an order of magnitude difference have to be optimized on the same silicon layer. Notably, Intel, the world's leading semiconductor company in advanced CMOS technologies, has selected a non-monolithic approach for its silicon photonics technology [19].

As an alternative to monolithic integration of photonics with CMOS, a fully integrated photonic BiCMOS platform was presented recently by IHP, Germany [20]. A BiCMOS heterojunction bipolar transistor (HBT) allows for a higher cutoff frequency at a given technology node, as compared to CMOS. This enables

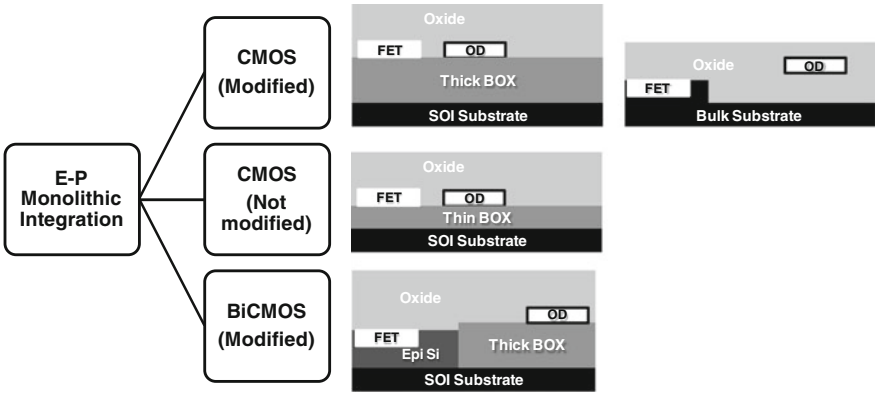

Fig. 6.1 Summary of silicon photonics E–P monolithic integration in recent years with schematics showing how the devices are integrated on the same substrate. Field-effect transistors (FET) and optical devices (OD) are used in the schematics to depict electronics and photonics, respectively. The metallization lines are not shown in the schematics

high-speed electronics to be integrated with photonics at a lower BiCMOS technology node. A 0.25 μm BiCMOS technology was employed for photonics integration and optical device modules were inserted in the baseline BiCMOS flow. This was achieved by forming local SOI and bulk regions on the substrate. A 25 Gb/s receiver was the demonstrator of the integrated electronics–photonics (E–P) platform and device availability is anticipated in 2016. However, these advantages come at the expense of added process complexity in terms of masks levels and related costs. Figure 6.1 summarizes the monolithic integration efforts in recent years.

6.2.3 Technology Platform for Hybrid Integration

Although integrating photonics onto the same chip as electronics might be advantageous for certain applications, the majority of silicon photonics research and development and their prototyping are implemented by forming the PIC on a separate chip. This uses CMOS-compatible process equipment in silicon foundries, but without the need to integrate two different process flows. As such, hybrid photonics and electronics integration becomes a more compelling approach in the near future. It allows the silicon PIC and high-speed electronics integrated circuits (EIC) to be separately optimized and fabricated. This means that both PIC and EIC chips are decoupled as being fabricated in different facilities and/or with different technology nodes, substrate types, and wafer sizes. By doing it this way, PIC developers can be more flexible in optimizing their design and in selecting fabrication support. After fabrication, the PIC and EIC can be integrated by either wire

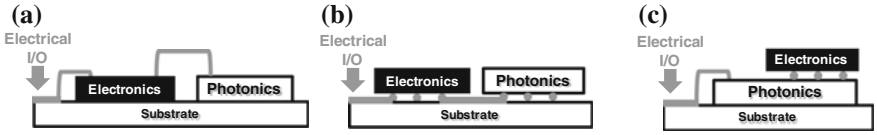

Fig. 6.2 **a** Wire bonding, **b** flip chip, and **c** 2.5-D/3D stacking are different assembly methods that can be used for hybrid E–P integration. A combination of assembly methods can be used to obtain the final system on package

bonding, bump bonding (or flip chip), or a combination of both through 2.5-D/3-D die stacking, as shown in Fig. 6.2. Considering the processes involved, these are relatively easier strategies without the loss of essential performance characteristics, as compared to monolithic integration and thus provide better cost performance trade-offs. Bandwidths in excess of 25 Gb/s have recently been demonstrated using bump bonding [21] and 2.5-D/3-D stacking [22] schemes.

Regarding the substrate, there have been various silicon photonics process platforms based on different starting substrate types, and the relevant ones to date are shown in Table 6.1 [9, 10, 23–28]. Table 6.1 is not an exhaustive list of such substrates, but is meant to illustrate the main differences in substrate choices between groups. SOI substrates with a top Si thickness (t_{TopSi}) of 220 nm and a 2 or 3 µm BOX thickness are most commonly utilized by various academia and industry groups. The 220 nm average t_{TopSi} for a 200 mm wafer is normally within ± 5 nm, but SOI vendors tend to give a thickness specification range of larger than 10 nm. A few foundries have converged to use this substrate in their silicon photonics process flows (See Sect. 6.3). Historically, the substrate of choice was guided by both the foundries and industry. Luxtera also chose a thin SOI platform, albeit a different t_{TopSi} and BOX thickness (t_{BOX}). This started out as a 200 mm monolithic CMOS photonics platform, but was converted to a 300 mm "photonics only" platform when the technology was transferred to ST.

Although a thin SOI-based platform enables compact PIC and high-speed active devices to be built, having a thicker t_{TopSi} allows larger process tolerances, polarization independent performance, and improved coupling efficiencies with proper device designs. A few groups have based their fully integrated platforms on thick SOI substrates (See Table 6.1). For example, Kotura demonstrated polarization independent MUX, and low-fiber coupling loss using a 3 µm SOI platform [26].

Table 6.1 Summary of starting SOI substrates for integrated silicon photonics platforms

SOI type[1]	t_{TopSi}/t_{BOX}	Substrate size (mm)	Ref
Thin	220 nm Si/2 or 3 µm	200 or 300	[23–25]
Thin	310 nm Si/720 nm	200 or 300	[9, 10]
Thick	3 µm Si/0.375 µm	150	[26, 27]
Thick	1.5 µm Si/2 µm	200	[28]

[1]Thin-SOI: $t_{TopSi} < 400$ nm, and Thick-SOI: $t_{TopSi} > 1$ µm

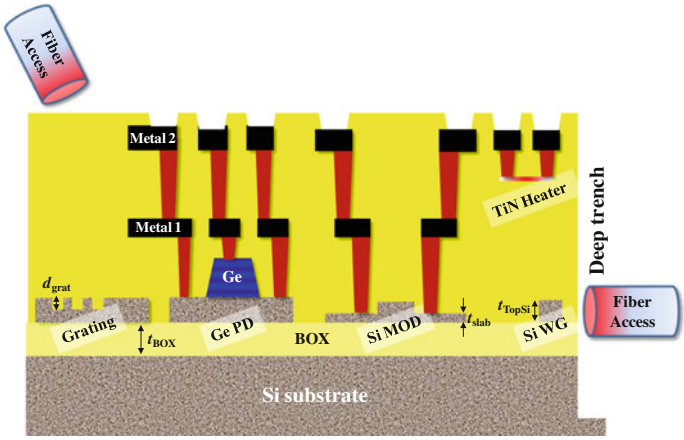

Fig. 6.3 Cross section schematic of an integrated silicon photonics platform where key building blocks such as Si passives, Si MOD, Ge PD, thermal optics, and fiber coupling access are shown. Grating depth (d_{grat}) and slab thickness (t_{slab}) are formed through different partial Si etches. (Dimensions are not to scale.)

Another company, Skorpios uses a 1.5 µm SOI platform which gives high coupling efficiency to III-V laser waveguides [28]. Ultimately, the device specifications from end-user applications will drive the selection of the appropriate SOI platform to be employed in a product.

Figure 6.3 shows a schematic cross section of a generic integrated technology platform consisting of both passives and active devices. The Si passives are formed by the first few mask layers through partial and full Si etching steps. Subsequently, multiple ion implantations are conducted for constructing active devices such as germanium photodetectors (Ge PD), and silicon modulators (Si MOD). A Ge epitaxy step is carried out after the implants in silicon regions and an activation anneal, because of the low thermal budget allowance from Ge. Although in Fig. 6.2 a vertical *pin* Ge PD and Si *pn* Mach–Zehnder (MZ) MOD are presented in the platform, both the Ge PD and Si MOD can be fabricated in other configurations (e.g., a lateral *pin* Ge PD, or a Si *pn* ring MOD). Other photonic devices such as MUX and optical switches, not illustrated in Fig. 6.3, can also be formed with a combination of the above-mentioned process steps. In the back-end-of-line (BEOL) metallization steps, a resistive heater can be included for thermal optical tuning or modulation. A TiN film is widely used to allow large area thermal heating above the Si passives devices. Implanted Si regions formed on the same lithographic layers as the Si passives can also be used as heaters, but heat transmission is restricted laterally, instead of a top-down radiation by a metallic heater [23]. A two-level metallization is shown in Fig. 6.3, but more levels of metallization can be used. A thicker top metal layer is preferred to reduce RF losses in traveling wave devices.

Regarding light coupling, the optical signal from the fiber onto the PIC and vice versa can be done by edge couplers and grating couplers. For edge coupling, a deep

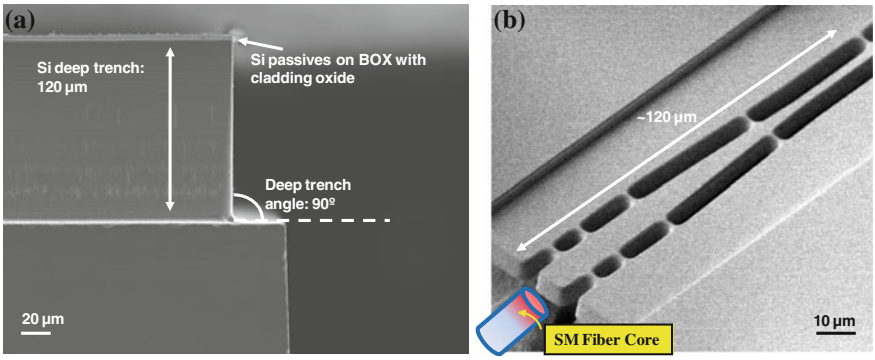

Fig. 6.4 **a** Cross-sectional SEM image of a vertical deep trench in Si that allows fiber access through edge coupling. **b** Tilt-SEM image of a suspended coupler with a single-mode (SM) fiber to illustrate the optical input. This was enabled by an isotropic deep trench in Si

trench is etched in Si to allow fiber access to the edge of the chip. Figure 6.4a shows a cross-sectional SEM image of a 120 µm Si trench formed by a deep reactive-ion etching (RIE) process. The Si trench has to be $\sim 90°$ to allow the fiber to be as close as possible to the PIC for effective coupling. An oxide etch is conducted before the deep RIE step to create a smooth oxide facet to minimize light scattering off the sidewall. This facilitates low-loss coupling from the single-mode fiber to the on-chip edge coupler, and eliminates the need for sidewall polishing of the chip after dicing. For die-level testing, an inverted Si nanotaper of 200 nm or less can be fabricated through the standard lithographic patterning and Si etches, and used to couple light from a 2.5 µm lensed fiber onto the PIC. A coupling loss of less than 3 dB is achievable from this testing setup.

For low-loss coupling from a single-mode cleaved fiber, a suspended oxide mode size convertor can be utilized [29]. Figure 6.4b shows a tilt SEM image of the suspended oxide coupler. This works as a broadband coupler with an operation range of >100 nm at the 1550 nm wavelength regime. The input oxide coupler facet dimension is determined by the total oxide thickness, which includes the t_{BOX} and oxide cladding thickness. With proper design optimization and the usage of a refractive index matching fluid, the coupling losses and alignment tolerance can be reduced to $\sim$1–2 dB/facet and larger than 2 µm, respectively. High precision and reliable fiber-to-coupler attachment is enabled through this structure.

Surface grating coupling can be enabled by a diffractive Si grating (e.g., 1-D or 2-D). The Si grating takes up a small footprint on-chip and is useful for incorporating wafer-level optical testing functionality for both inline during wafer processing or end of line. Low coupling losses can be attained from gratings with the appropriate Si thickness and design [9]. Unlike the edge couplers, gratings are narrowband devices and operate at a smaller operation wavelength range and polarization.

6.3 Role of Research and Development Foundries

Research and development (R&D) foundries are owned either by research institutes that are typically nonprofit organizations and largely funded by the government agency, or by private companies for internal research. For this section, foundries from research institutes are referred to, and their role in silicon photonics commercialization is elaborated for its strategic criticalness in establishing and bridging from a research-intensive technology phase toward product development and a commercialization oriented phase.

Being part of the foundry element in the silicon photonics supply chain, these foundries facilitate initial access to the technology for research and prototyping. In addition, R&D foundries have more flexibility in customized process platform development, as compared to commercial foundries. To augment a fast prototype-to-production cycle, process-specific design kits and yield enhancement methodologies can also be acquired from these foundries. In some cases, assistance in technology transfer for manufacturing, and the undertaking of small production volumes could also be necessary. As part of the case study, the following subsections describe fabrication services offered by R&D foundries and their involvement in silicon photonics.

6.3.1 Standardized Shuttle Runs

Standardized shuttle runs can be administered as MPW services from foundries to provide low-cost PIC fabrication for academic research groups and fabless companies. MPW users can share reticle space and buy into blocks of design area ranging from a few tens to hundreds of square millimeters (mm^2). In the case of using a Nikon stepper for instance, a 200 mm SOI wafer with $\sim$25,000 mm^2 of usable chip area can get up to 30 dies per MPW user from a lithographic shot size of 800 mm^2. Figure 6.5 illustrates how multiple users can share a standardized process by owning a portion of the reticle space on a mask set. Individual dies can be singulated by dicing before shipping to the respective users. This effectively lowers the reticle and wafer processing costs which can run up to hundred thousands of dollars for one user in a dedicated foundry run.

Silicon photonics MPW passive runs were started more than 5 years ago [30, 31]. As the research evolved, it became evident that a MPW platform to include active photonics devices was required for integrated photonic circuit design and product innovation. Table 6.2 shows the silicon photonics MPW services that are available in research and development foundries [7, 31–34]. Geographically, most of the listed institutes are located in Europe with the exception of the Institute of Microelectronics (IME)/A*STAR which is based in Singapore [34]. Although there are other research institutes in Asia working on silicon photonics such as the National Institute of Advanced Industrial Science and Technology (AIST) from

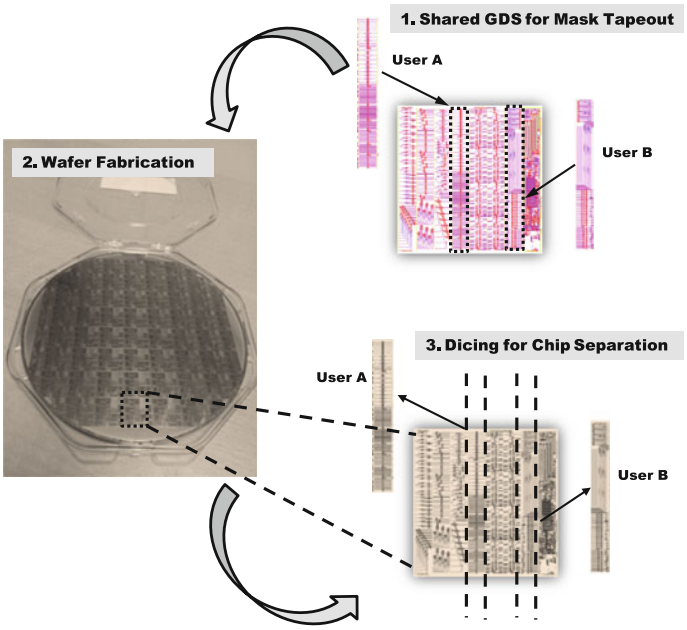

Fig. 6.5 A MPW service allows users to share mask space and fabrication costs by using a fixed silicon photonics process flow

Table 6.2 List of foundries with Silicon Photonics MPW services

Foundry	Starting SOI (Substrate size/t_{TopSi})	Device platform	Administrating organization[a]
CEA-LETI	200 mm/220 nm	Passives and fully integrated	ePIXfab
IMEC	200 mm/220 nm	Passives and fully integrated	ePIXfab, MOSIS
IME/A*STAR	200 mm/220 nm	Fully integrated	CMC, IME/A*STAR
IHP	200 mm/220 nm	Passives and fully integrated	ePIXfab
VTT	150 mm/3 μm	Passives	ePIXfab
AMO	150 mm/220 nm	Passives	AMO

[a]MPW service can be offered directly by the foundries or through administering organizations

Japan [35] and the Electronics and Telecommunications Research Institute (ETRI) from South Korea [36], MPW services are not administered on these silicon photonics fabrication lines.

The total cost for an MPW run can be kept to a few tens of thousands dollars as shown by a 5 × 5 mm^2 block costing ~$2000 USD/$mm^2$ [37]. The silicon photonics MPW unit area cost is actually higher than a 0.13 μm CMOS logic MPW

run, which costs ~1000 USD/mm^2. However, due to the low wafer volumes, a silicon photonics MPW service might not be an attractive business model for commercial foundries and thus it remains to be offered only by research institutes presently. These institutes usually have government-related funding and the gross profit margin is not the sole consideration for a foundry service offering.

One way for rapid technology adoption is to allow widespread and easy access to the technology. An example of this is seen when IME/A*STAR launched a Si passive MPW platform in 2008, followed by a 10G fully integrated MPW platform in 2010 [30, 34]. These platform offerings allow international academia groups and industry early access to the technology. As IME's fully integrated Si photonics platform is developed to 25G and beyond [23], Optoelectronics Systems Integration in Silicon (OpSIS) from University of Washington (and then University of Delaware), USA collaborated with IME to launch the first 25G MPW platform in 2012 [38]. This collaboration complemented IME's state-of-the-art fabrication facilities and existing silicon photonics process flow with OpSIS's design and testing capabilities to administer multiple shuttle runs at rapid turnaround times. Although OpSIS has since closed, the 25G silicon photonics line in IME is still administered either directly by the research institute or through other organizations, e.g., CMC Microsystems (CMC) in Canada. The collaboration of IME with CMC and OpSIS shows how the silicon photonics ecosystem can be expanded by R&D foundries.

In Europe, ePIXfab have similarly been offering a silicon photonics foundry service and to a smaller extent, design and packaging services. ePIXfab hosts a consortium of organizations with the mission of supporting fabless silicon photonics. Recently in 2013, IMEC also announced the launch of its 25G silicon photonics platform (ISiPP25G).

Moving forward, 25G becomes the baseline platform for the 100G enablement of next generation optical communications. To scale to a higher bandwidth of 400G and beyond, a 50G and 100G per lane optical bandwidth may be necessary. Therefore, the development and optimization of existing 25G technology platforms is required by the foundries to achieve this, as being demonstrated in references [23, 39] for 40Gbaud and 50Gbaud efforts.

To augment the MPW fabrication services, design tools were concurrently developed by software companies with the foundries. A design platform that includes, but is not limited to, compact photonics models for circuit simulation, schematic-driven layout, and design rule checks (DRC) are the focus of companies like Mentor Graphics, Lumerical, PhoeniX, Luceda, and many others (see other book chapters). These tools will form part of the PDK tied together with silicon photonics foundries and the relevant process platforms.

6.3.2 Customized Process Platform

The standardized MPW platform provides a path to low-cost fabrication, and is beneficial for foundry users undertaking initial silicon photonics research and prototyping activities. However, the silicon photonics process is relatively new and the technology does not scale in a straightforward manner like CMOS technology nodes do with transistor gate dimensions. There are international standards and alliances for optics being progressively formed and these specifications will guide integrated photonics technology platforms [40–42].

Along the way, there will be numerous developmental efforts to optimize the process platform. This is required when circuit design innovation is unable to achieve the desired PIC performance for a product. These enhancements can come as process modifications or additions, e.g., to implantation conditions, lithographic patterning in critical dimensions and overlay, and etch/deposition thicknesses. A second reason for process customization is the need to create a new platform that deviates significantly from the foundry's silicon photonics baseline flow. An example would be creating devices that are structurally different [43], or with new materials/processes [44, 45]. Sometimes, the chosen foundry does not have a silicon photonics line, and a complete platform has to be established according to the customer's request.

Process optimization changes may be accepted by the foundry under a particular collaboration or business model. However, this is not the ideal scenario for a fabless model when every user requires a different platform. In a commercial semiconductor foundry, large nonrecurring engineering (NRE) costs may be incurred for process development. Process customization should only be done if performance enhancement outweighs the additional process complexity, i.e., costs. This is the area where research and development foundries play a key role by offering process flexibility to foundry users. For example, IME/A*STAR is one of the foundries that offer customized prototyping to its foundry users in addition to MPW runs.

6.3.3 Small Volume Production

For early silicon photonics products, the PICs were fabricated in a dedicated foundry or an in-house foundry for Luxtera and Kotura, respectively. In the last few years, more fabless silicon photonics companies are looking for foundries to prototype early production samples. These wafer volumes are low in the initial years and a relatively large number of chips can be produced from ⟨?⟩ a few wafers. As an example, an 8-inch SOI wafer is able to produce a few hundred transceiver PICs with a chip area of 60 mm^2, or more than a thousand receiver PICs with a chip area of 15 mm^2, assuming a 80 % wafer yield and reticle size of 800 mm^2. Figure 6.6 shows that the market trends for yearly wafer volumes are expected to be at about one thousand wafers until 2018. Beyond 2018, "all optical" data centers will drive

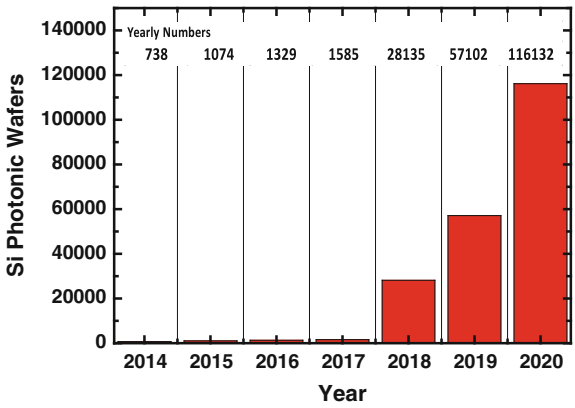

Fig. 6.6 Silicon photonics wafer volume based on transceiver and embedded optics volume from 2014 to 2020. A Si photonics die size of 37 mm^2 and increasing wafer yield from 55 % in 2014 to 74 % in 2020 is used. Sharp increases in 2018 and 2020 are due to "all optical" data center and embedded optics introductions, respectively [5]

the surge in silicon photonics optical interconnects. Another anticipated driver of silicon photonics wafer volumes is the emergence of embedded optics in 2020. The wafer numbers from Reference [5] are based on estimated transceiver volumes, and it indicates an impending uptrend of silicon photonics as a disruptive technology at the global scale. Therefore, it is imperative that commercial foundries commence setting up manufacturing lines, if there is an intention to capture the market share of wafer volumes in the near future. Comparing these silicon photonics wafer volumes to CMOS, there is a clear mismatch in business model for CMOS foundries engaged in high volume manufacturing for the initial stages. However, with the right killer application and the push for higher data bandwidth, these wafer volumes are likely to increase.

Figure 6.7 gives the main considerations when running silicon wafers through a foundry, which is applicable to silicon PIC volume production. During the product development stage, e.g., in Alpha- and Beta runs, wafer quality and process repeatability are essential to meet product specifications and build a predictable process integration flow. Of course, a fast cycle time is also critically desirable, as well as on-time delivery. This will lead to a wafer delivery schedule that is communicated from the foundry to the customer, based on the wafer fabrication loading. Last but not least, it is important to understand the foundry's capability in handling increased wafer volumes for future ramp-ups, i.e., fab capacity.

The gap before the high wafer volume period that fabless silicon photonics companies are facing could be bridged by research and development foundries. To do so, these foundries have to evaluate the main considerations shown in Fig. 6.7, and determine if the small volume production in the existing line is manageable. These include stringent statistical process control (SPC) monitoring and inline metrology checks for process quality control, strategies to meet tight schedules in

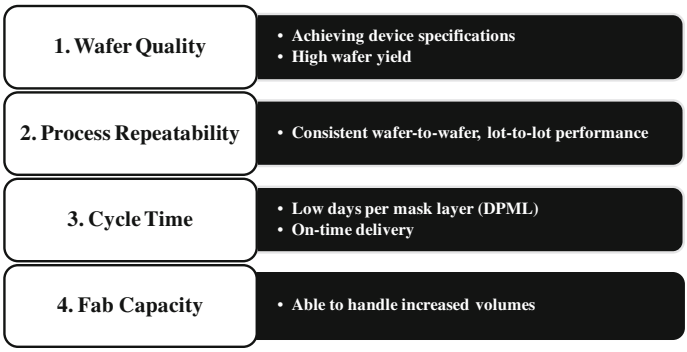

Fig. 6.7 Main considerations for wafer fabrication in a foundry, which are applicable to silicon PICs volume production

product lot cycle times, and a transition path for high volume manufacturing when the wafer volume ramps up. In addition, fabrication capacity has to be allocated between engineering runs and production lots within the R&D foundry. Usually, R&D foundries from research institutes have single-point tools with few or no backups, since this is not originally intended to be a production line. Therefore, to effectively support small volume production, redundancy paths have to be planned and built as part of the risk mitigation strategies. This would include investing in some critical back-up tools, or qualifying outsource vendors, especially for bottleneck processes. Once the manufacturing measures are in place, these foundries can effectively play a vital role to support the value chain.

6.4 Route to Commercialization

Although pathways to PIC prototyping and early production are available, companies need a high volume production route because research and development foundries from research institutes are not suitable when wafer volumes scale up. The silicon photonics foundry model would then shift to commercial foundries for mass production. These foundries provide a manufacturing environment to ensure stable processes are repeatable within predictable margins at high wafer volumes. A PDK for modeling process corners to facilitate a design for manufacturing (DFM) flow is usually available too. Alongside these capabilities, the commercial foundry's supply chain in terms of testing, assembly and packaging, though not necessarily photonics-specific, can be leveraged on.

One of the reasons for the lack of commercial foundries running a silicon photonics line, especially for pure-play electronics IC foundries, may be the absence of silicon photonics technology know-how. Therefore, a technology provider can collaborate with a foundry to transfer the technology. The ST

Microelectronics (ST)–Luxtera collaboration is an example whereby the technology provider, Luxtera, licensed its silicon photonics platform to ST, an IDM semiconductor foundry [10].

Although the business model for large commercial foundries to maintain an open access silicon photonics line is not evident yet, efforts must be taken to allow silicon photonics companies access to foundries for technological development and commercialization. In the following subsections, silicon photonics technology transfer to a CMOS pure-play foundry is described. Si PIC process qualification flow and foundry-related trends are also covered.

6.4.1 Manufacturing in CMOS Foundry

Recognizing that the PIC manufacturing facility is becoming a critical element in the supply chain, a collaborative effort between IME/A*STAR and GLOBALFOUNDRIES, Singapore (GF) for a platform technology transfer was initiated. Bell Labs, Alcatel-Lucent (ALU) was also part of this collaborative effort by providing design support. This technology development was done by transferring IME/A*STAR's silicon photonics platform to GF's 200 mm 0.18 μm CMOS manufacturing foundry line. GF's 0.18 μm CMOS foundry line was selected to provide low-cost processing in a stable manufacturing environment with high yield. The platform description can be found in Reference [24]. To get an estimate of the cost difference between CMOS technology nodes, the cost per mm^2 in a MPW shuttle for a 0.18 μm CMOS node (Logic, Mixed mode/RF) was compared with a corresponding 65 nm CMOS node and found to be ~5 times lower [37]. It is anticipated that the cost per mm^2 for a Si PIC in a manufacturing foundry can be cheaper than the R&D foundries shown in Table 6.2, especially when a less advanced CMOS technology node is utilized. However, cheaper prices are not guaranteed and depend largely on the business strategies assumed by the manufacturing foundries.

Wafer-level testing is essential for the manufacturability of silicon photonics wafers. It ensures that known good dies (KGD) with acceptable PIC specifications are selected for downstream activities like packaging or integration, while providing feedback for yield improvement and process control monitoring (PCM). CMOS foundries have standard electrical test (Etest) blocks placed at the wafer scribe lines to serve as PCM structures. These are measured by commercial electrical probe stations. Optical/optoelectronics (OE) PCM blocks have to be additionally included for photonics device characterization and a wafer-level optical testing platform is required. Figure 6.8 shows a suggested PCM list that can be used to monitor wafer quality and process stability. Structural parameter data are collected inline, while electrical and optical/OE parameters can be measured after fabrication.

Figure 6.9a shows an optical wafer-level tester setup in IME for automated testing. The tester uses a fiber array as the optical probes. During measurements, the fiber probe is ~20 μm above the wafer (in the z-axis). A "golden" Si passive wafer

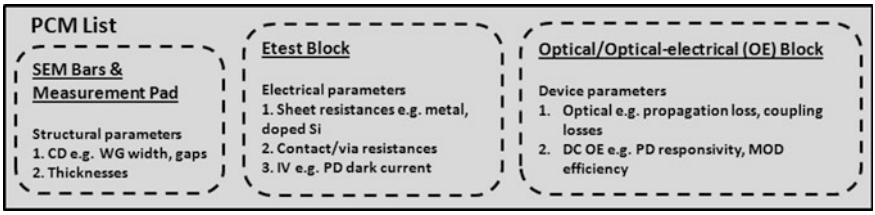

Fig. 6.8 PCM list for a silicon photonics flow whereby structural and electrical parameters can be measured in a standard CMOS foundry. Optical or OE measurements are specific to a photonics flow and customized testers have to be set up

is used as a test set-up reference before measurement to ensure that the fiber probe condition and set-up parameters remain consistent. DC and RF electrical probes can be mounted to the tester for OE measurements when needed. Figure 6.9b shows an optical image of "lighted" gratings used for optical testing. For waveguide (WG) propagation loss extraction, Si WGs attached to the gratings are used in cutback structures (See Fig. 6.9c).

Previously, individual photonic modules (e.g., passives and Ge PD) were verified separately on the GF CMOS manufacturing line before a full integration [24]. Subsequently, the passive and active devices were integrated to deliver a 25G silicon photonics platform. After fab out from GF, waveguide losses were measured on a fully integrated wafer using the wafer-level optical tester. Figure 6.10a, b show the wafer maps of Si channel and rib WG propagation loss at 1550 nm. Optical losses of 1.6 dB/cm ($\sigma = 0.4$ dB/cm) and 0.9 dB/cm ($\sigma = 0.3$ dB/cm) were attained, respectively. The bending loss for a 5 μm Si channel WG bend (width of 500 nm) was less than 0.02 dB per 90° bend. The grating coupler used for wafer-level measurement had a central wavelength of 1535 nm ($\sigma = 3.8$ nm). These gratings having a coupling loss of $\sim$6 dB (measured by angled fiber array) and were not

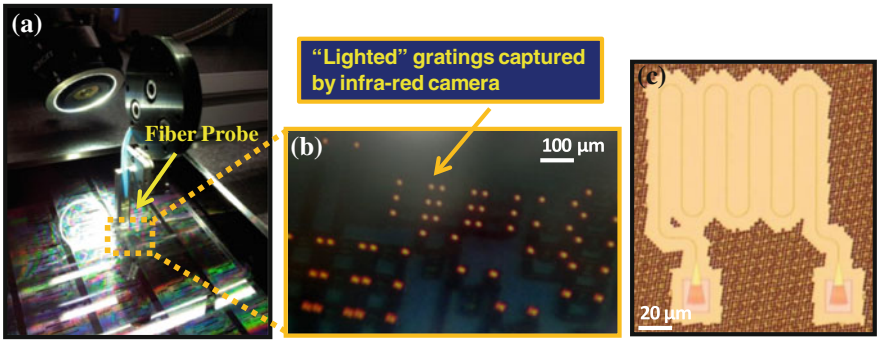

Fig. 6.9 **a** Wafer-level optical tester setup with a fiber array used for optical ports. **b** Optical image of "lighted" Si gratings used for wafer-scale measurements. **c** Optical micrograph of a grating coupler with a Si channel waveguide used in cutbacks to extract the optical propagation loss

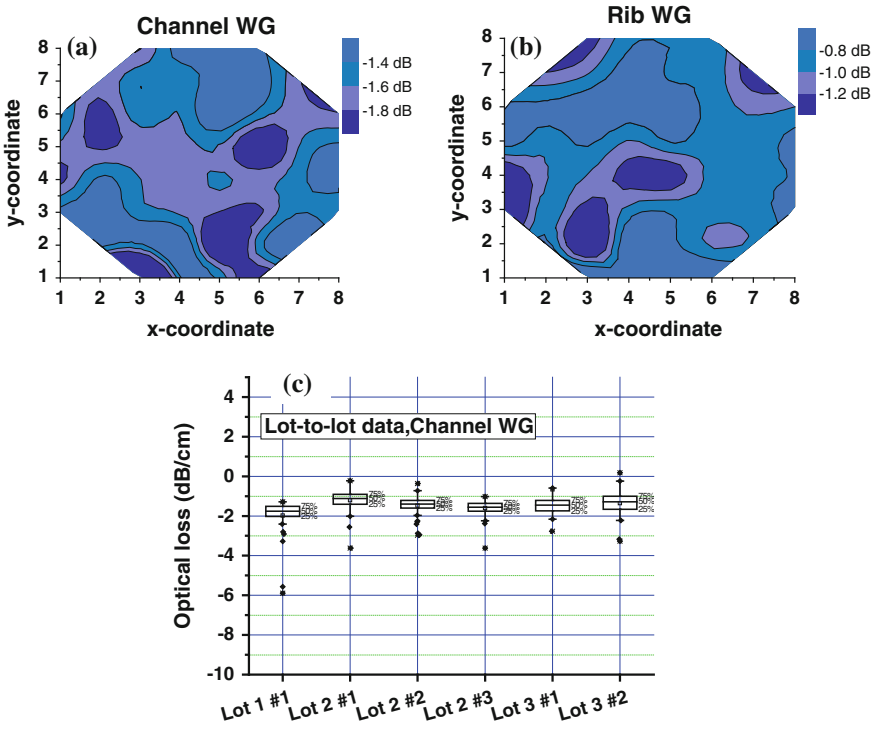

Fig. 6.10 Wafer-level map of **a** Si channel waveguide and **b** Si rib waveguide losses for a fully integrated wafer. The WG width was 500 nm and slab thickness for the rib WG was 90 nm. The average WG loss was 1.6 dB/cm and 0.9 dB/cm for Si channel WG and Si rib WG, respectively. A total of 52 dies were measured. **c** Lot-to-lot data for a channel WG showing consistent Si channel WG losses after 3 lots

optimized for best efficiency. The coupling efficiency can be improved by 50 % using nonuniformed grating couplers [46]. Lot-to-lot data is important to ascertain process stability across a period of time, and key specifications like the optical losses need to be consistent (See Fig. 6.10c). In addition, wafer-to-wafer repeatability data is also collected to check process variability within the lot.

From the same platform, results from a Ge PD and Si MOD are presented. Figure 6.11 shows the TEM images of the Ge PD and Si MOD from this integrated platform. The high-speed Ge PD (>20 GHz) has a low dark current of $\sim$10 nA and a responsivity of $\sim$1 A/W at –1 V (See Fig. 6.12). A specially tuned high quality selective Ge epitaxy recipe was used for Ge integration in GF's line. A low-loss, high-efficient Si MOD was also demonstrated and results are shown in Fig. 6.13. The 4 mm Si MZI MOD had an insertion loss of $\sim$4.4 dB, and 6 V was required for a π phase shift (Vπ) giving a $V_\pi \cdot L$ of less than 2.5 V·cm. Figure 6.13b shows a 3 dB bandwidth of 13 GHz, which signifies the device was capable of 25 Gb/s operation. The baseline modulator can be further optimized through implant

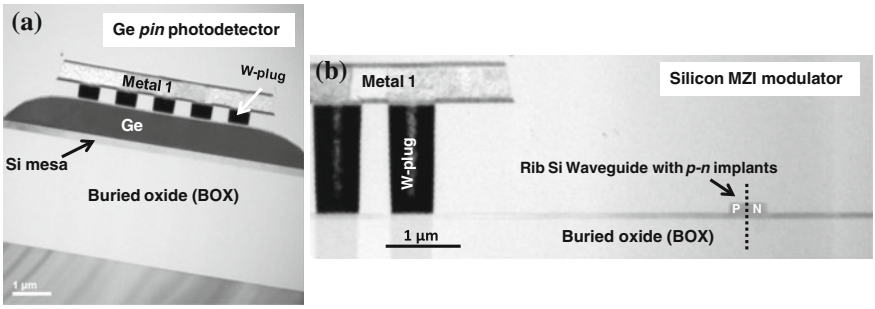

Fig. 6.11 TEM images of active devices such as the **a** Ge *pin* PD and **b** Si MZI modulator from the fully integrated platform

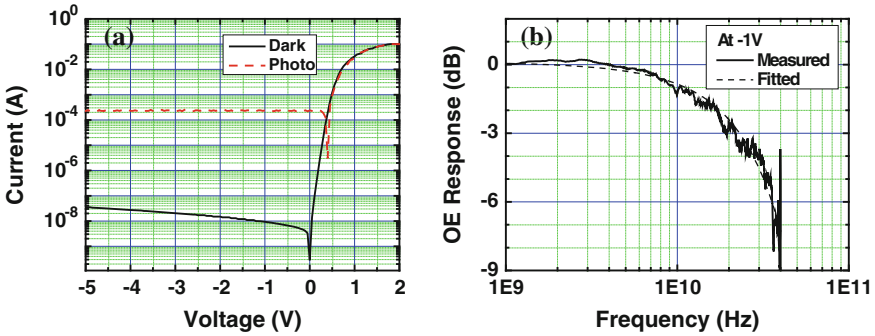

Fig. 6.12 A high-speed Ge PD in a fully integrated platform was fabricated. **a** The dark current and photocurrent (at $\lambda = 1550$ nm) for 8×25 μm Ge *pin* PD is shown. The internal responsivity is ~1 A/W at −1 V reverse bias. **b** 3 dB bandwidth of the Ge PD showing that it is >20 GHz at −1 V

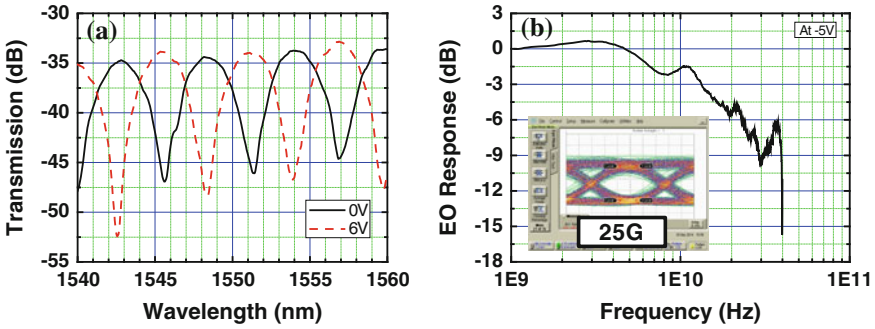

Fig. 6.13 A 4 mm Si MZI MOD was measured and gave a $V\pi \cdot L$ of ~2.5 V·cm. **b** The bandwidth at –5 V was ~13 GHz and the inset shows a 25.6 G eye diagram with an extinction ratio of 4.31 dB (DC bias = –5 V, V_{pp} = 5.7 V)

conditions and device design to achieve a better modulation efficiency and higher bandwidth. The platform also has an integrated TiN heater that is thermally isolated to deliver a heating efficiency of less than 1 mW per π shift, similar to Reference [23]. Efforts are ongoing to understand process corners and to implement DFM guidelines by running additional lots. From these process margin check runs, the data is collected to form a statistical database that can be fitted into a PDK. A subsequent planned release of this platform in a MPW form for preliminary usage is ongoing.

6.4.2 *Process Qualification and Reliability*

For a commercial CMOS foundry, both process qualification and long-term reliability tests have to be conducted to fully qualify a technology platform for production. These reliability tests follow the American National Standards Institute (ANSI) accredited Joint Electron Device Engineering Council (JEDEC) standards for microelectronics qualification.

Thus, a qualification process is also expected for a silicon photonics platform running in a CMOS foundry line to ensure that reliable components and chips are fabricated. Once the device specifications are met and process optimization is completed, the process is frozen and qualification lots are run for reliability testing. The Telcordia Standard is usually used to provide reliability assurance requirements for telecommunications applications [47]. Optoelectronic products in telecom are expected to have operational lives on the order of 20 years. These products are generally made from conventional materials for optical communications such as silica, III-V and lithium niobate. Going through the qualification tests assesses if they are able to meet the stringent reliability criteria.

For silicon photonics qualification, a combination of Telcordia and JEDEC standards should be used, since this is unlike conventional optoelectronics. KGDs are screened for reliability testing after initial inspection and device characterization is conducted. Both die-level and packaged-level qualification of silicon photonics wafers from the foundry can be conducted. Electrical reliability tests can be done at die level, while optical/OE reliability testing requires packaged level for optical input/output during measurements. A full qualification (Full-Qual) timeline can stretch to more than 3 months if stress times go up to a few thousand hours. Therefore, a prequalification (Pre-Qual) with shorter stress cycles, or stress time, can be employed to allow the initial release of the foundry platform.

An example of CMOS foundry-related qualification at the die level is an electromigration (EM) test where change in resistance is monitored after stressing a metal line or contact hole at different currents and temperatures. The time to failure (TTF) for different stress conditions is recorded and used to tabulate whether the EM pass/fail criteria is met. For silicon photonics devices, Telcordia standards can be used as guidelines for reliability testing. The reliability tests are categorized broadly into mechanical integrity tests, non-powered stress tests, and powered stress tests.

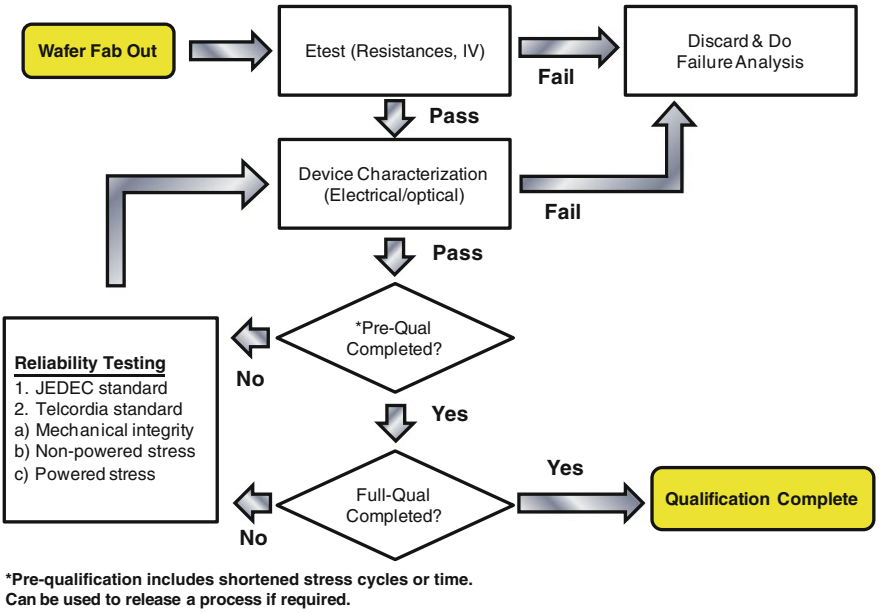

Fig. 6.14 Reliability test flow for silicon photonics platform qualification at a manufacturing foundry line

The tests conditions have to be tailored for silicon photonics products according to end-user applications. Currently, the majority of CMOS or semiconductor foundries do not have photonics testing and packaging capabilities. Therefore, it is expected that the foundry and end users work collaboratively to conduct the qualification together, especially in the preliminary stages of a new platform qualification. The packaged-level reliability tests can also be solely undertaken by the customer in a product qualification [48]. A flowchart for a general reliability test flow for silicon photonics chip qualification is depicted in Fig. 6.14.

6.4.3 Outlook and Trends

Figure 6.15 illustrates key elements in the silicon photonics value chain that are interrelated. The value chain should as much as possible leverage existing infrastructure not only from the foundry lines, but also the design tools, testing equipment, and packaging capabilities available in the semiconductor industry.

In the current design environment, integrated circuit (IC) designers with a Si photonics background largely use standalone simulation and layout tools to design Si PICs. However, a full-fledged CMOS-equivalent PDK with integrated layout and photonic component/circuit simulation tools will prove useful when executing a

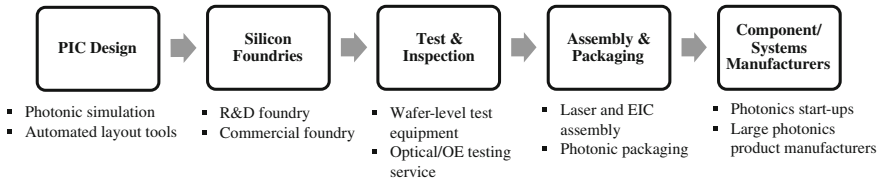

Fig. 6.15 A silicon photonics value chain consisting of key elements like PIC design, silicon fabrication foundries, optical/OE testing, and assembly and packaging for end users like silicon photonics start-ups and large product manufacturers

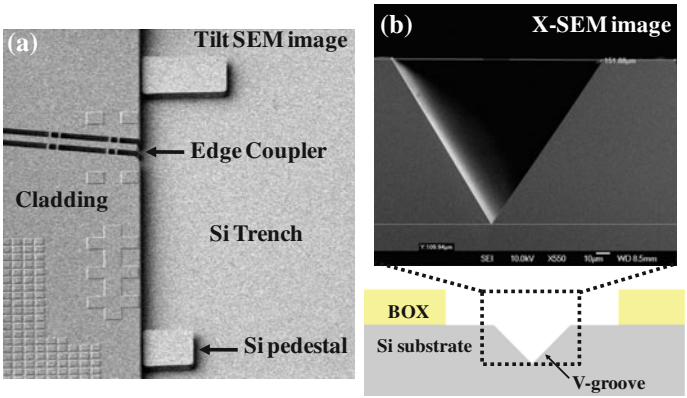

Fig. 6.16 **a** Shallow trench and **b** V-groove are some examples of the structures that use MEMS-like processes for passive alignment of laser diode and fiber, respectively

truly fabless silicon photonics model for manufacturing. IC designers without in-depth photonics knowledge can then easily design using photonics building blocks that have stipulated input/output ports that could be used for electrical co-simulation. The PDK also has to be tied to a silicon photonics foundry process, so it requires software vendors to work with the foundry or the technology provider.

The silicon PIC process platform is fairly well established and, at present, there are more focused efforts on PIC integration with the light source and the optical fiber to enable low cost packaging solutions. The formation of deep Si trenches (larger than a few microns) and V-grooves are some examples of passive alignment structures that are used to enable this integration, as depicted in Fig. 6.16. The structures are formed by MEMS-like processes, and suitable integration schemes have to be developed in the appropriate foundries when translating from a CMOS to a MEMS process flow. For the E–P integration, design rules such as bond pad pitch and size should be complied with. These design rules vary with the choice of assembly, and are usually less stringent for wire bonding, as compared to bump bonding. For bump bonding, bump formation for the top chip has to be additionally considered, and it may be relatively easier to form this on the EIC than the PIC

because of flatter chip topography. The design rules for pad pitch and size are limited by the assembly house, and this has to be taken into consideration during PIC design. Therefore, assembly and packaging schemes should be closely integrated with frontend design and fabrication processes as a holistic integration flow.

After fabrication, rapid testing at the wafer-level is required to screen KGDs. This can be done either by foundries internally, or outsourced to companies that provide optoelectronics test services and solutions. Correspondingly, there will be an increasing number of equipment vendors developing wafer-scale systems for optical testing. The same testing stations can be altered by changing the stage for die-level testing at the assembly and packaging stage.

There will be more silicon photonics start-ups emerging in the coming years to exploit new market opportunities arising from the technology. They could be component makers, technology providers and even design houses for larger photonics product companies. Together with existing silicon photonics product manufacturers, these companies will drive the demand for PIC fabrication services. Although there are increasing numbers of companies growing the technology at present, the lack of a manufacturing platform would prevent them from getting products out fast enough to meet market demands. This might result in smaller start-ups getting stuck in "valley of death" phase, which eventually inhibits growth in the silicon photonics ecosystem and prevents technology advancement [49].

Moving forward, a twofold approach is needed to bridge the absence of a "right size" manufacturing facility for silicon photonics at the moment. Research and development foundries may need to scale up fabrication capacities, while commercial foundries have to accept smaller volumes to meet wafer demands. Before wafer volumes become a viable business for large semiconductor foundries, there is an increasing likelihood that smaller size commercial foundries, in particular specialty foundries, will gain entry into the PIC fabrication service. There are also regional initiatives in countries such as the United States whereby planned investments are set aside to build a manufacturing ecosystem for integrated photonics [50].

6.5 Conclusion

A fabless silicon photonics is imperative for rapid utilization of the technology. There is a need to standardize silicon photonics processes to a generic platform for this to occur. Although monolithic integration of silicon photonics and CMOS electronics was heralded as the solution to integrated photonics, there are still cost-performance trade-offs to consider. On the other hand, hybrid E–P integration holds greater advantages for a cost-effective approach toward commercialization ultimately.

The roles of R&D foundries have expanded to encompass various fabrication services from MPW and customized prototyping to small volume production as a way to meet increasing demands from the silicon photonics community. To further

enable a route to commercialization, major efforts in developing commercial foundries for low-cost manufacturing are near completion and business models have to be set up for production. The strengthening of other critical elements in the value chain will allow silicon photonics to advance technologically and overcome the barriers for mass production.

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Chapter 7
Packaging of Silicon Photonic Devices

Peter O'Brien, Lee Carrol, Cormac Eason and Jun Su Lee

Abstract The demand for photonic systems based on Silicon CMOS technology is driven by its ability to satisfy demands in large markets, particularly for telecoms, datacoms and sensing applications. Device fabrication based on CMOS wafer-scale processes can meet this demand. However, photonic packaging can be a device-by-device process which is difficult to scale to high volumes. Packaging challenges remain in areas such as fiber-array coupling, laser source and electronic integration, and efficient thermal management. This chapter reviews these challenges and solutions that address them. It also reviews efforts to develop common photonic packaging design rules, which if implemented at the device layout stage, can greatly simplify the overall manufacturing process and help reduce production costs.

7.1 Introduction

By exploiting the legacy of established CMOS fabrication technologies used in silicon electronics, the last decade has seen the emergence of silicon photonics as a vehicle for information communication technology (ICT), medical, and sensing applications [1, 2]. Realizing useful photonic integrated circuits (PICs) demands not only the development of individual Si-photonic components and devices, but also on the realization of integrated Si-photonics platforms that can interface with the outside world, through optical and electronic signals. The term "Photonics Packaging" is a catch-all expression that covers the technology needed to support both optical and electronic interfacing with the PIC, and includes fiber-coupling, laser-source integration, wire-bonding, and flip-chip integration for efficient high-speed signaling [3]. By default, "Photonic Packaging" also extends to the

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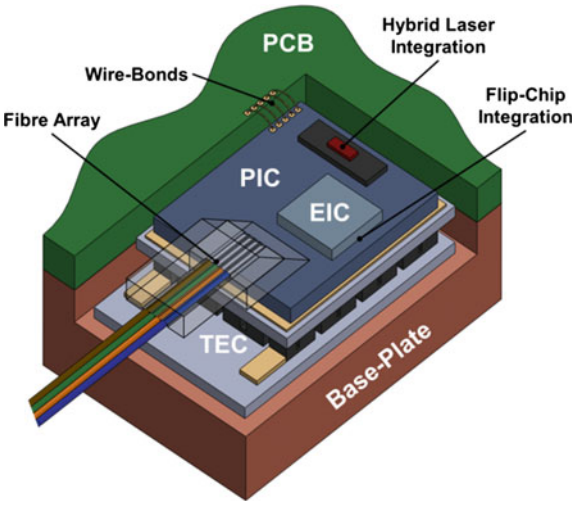

Fig. 7.1 Schematic of the different elements covered by the photonic packaging of a Si-PIC—wire-bonding for electrical contacting, fiber-arrays for optical packaging, flip-chip integration of an electronic-IC, hybrid integration of a laser source, and TEC cooling for temperature stabilization

active thermal management needed by most Si-PICs, because of their strong temperature sensitivity (Fig. 7.1).

Ultimately, the key economic driving force behind Si-photonics is the potential to realize small, highly integrated photonic subsystems that leverage-off the decades of experience and advances behind CMOS electronics [4]. Using these well-established wafer-processing techniques, silicon photonics offers the possibility of low-cost mass-producible photonic systems, complete with integrated electronics. However, the challenges associated with the photonic packaging of silicon devices is often underestimated, and can significantly impact the performance and cost of the photonic module (Fig. 7.2).

This chapter reviews some of the key technological and commercial challenges associated with the packaging of silicon photonic devices. In Sect. 7.2—Optical Packaging—we discuss the efficiency and tolerance of fiber-coupling with edge- and grating-coupling schemes, as well as hybrid laser integration. In Sect. 7.3—Electrical Packaging—we discuss wire-bonding for RF and DC signals, and flip-chip bonding for the 3-D integration of photonic and electronic components. In Sect. 7.4—Thermal Management—we comment on the sensitivity of photonic components to temperature changes, and the need for thermo-electric cooling (TEC) in packaging. In Sect. 7.5—Packaging Design Rules—we motivate the standardization of photonic packaging design rules to help users better access open foundry services, and reduce the cost of producing Si-photonic devices (Fig 7.3).

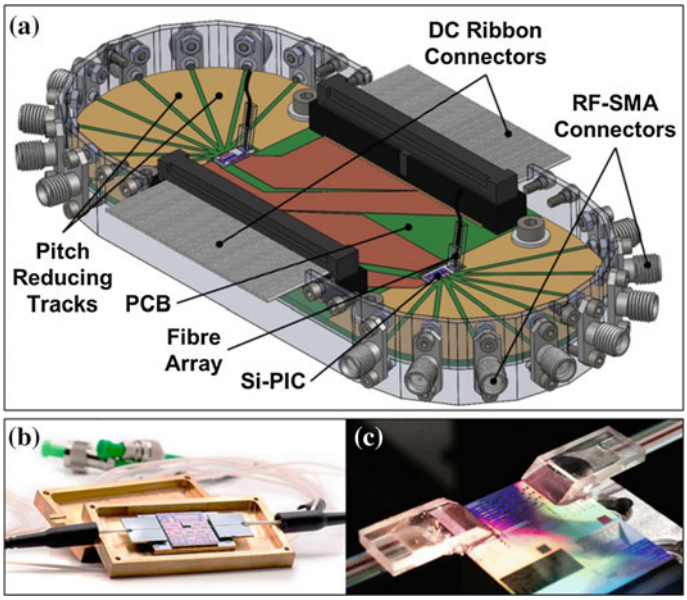

Fig. 7.2 **a** Schematic of a fully packaged photonic module consisting of a pair of Si-PICs for transmission and receiving, high-speed RF electrical signal channels, DC electrical connections, multi-channel fiber-arrays, and active thermal cooling through the base-plate. **b** Image of a Si-PIC optically packaged to a pair of single fibers. **c** Image of a Si-PIC optically packaged to a pair of multi-channel fiber-arrays

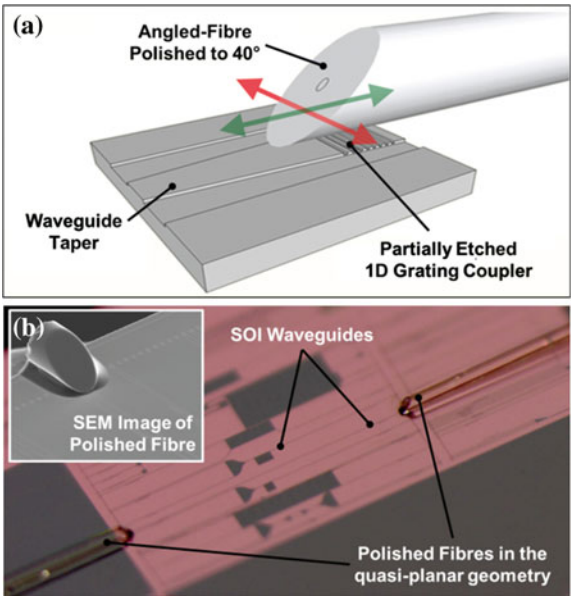

Fig. 7.3 **a** Schematic of fiber-alignment to a 1-D grating-coupler, using the quasi-planar approach. **b** An example of a Si-PIC optically packaged to a pair of single fibers in the quasi-planar geometry. The *inset* shows an SEM image of the polished facet bonded to the surface of the PIC

7.2 Optical Packaging

One of the most significant obstacles to the development of useful Si-PICs is the efficient transfer of light from a laser source into the silicon-on-insulator (SOI) platform [5]. As a Group IV indirect-gap semiconductor, silicon is fundamentally incapable of the direct-gap recombination-rates needed for efficient diode-laser emission. Practical silicon photonics requires the insertion of laser light from a III-V source, and this can be achieved in two ways:

- Transporting light from a stand-alone external laser device to the Si-PIC through a single-mode telecom fiber, followed by the coupling of the fiber-mode into a SOI-waveguide, using either an edge-coupling or grating-coupling element.
- Hybrid/heterogeneous integration of a III–V laser device/material on top of the Si-PIC, followed by evanescent- or diffractive-coupling of the laser mode into the SOI-waveguide.

For many applications in the ICT space, it is not uncommon for optical-packaging of a photonics module to call for both fiber- and laser-coupling, with on-chip multiplexing of signals from several integrated lasers into a single high-speed channel, which can then be launched into a telecom fiber via a grating-coupler [6]. However, for clarity, we will separately discuss the different optical packaging options in this chapter (Fig. 7.4).

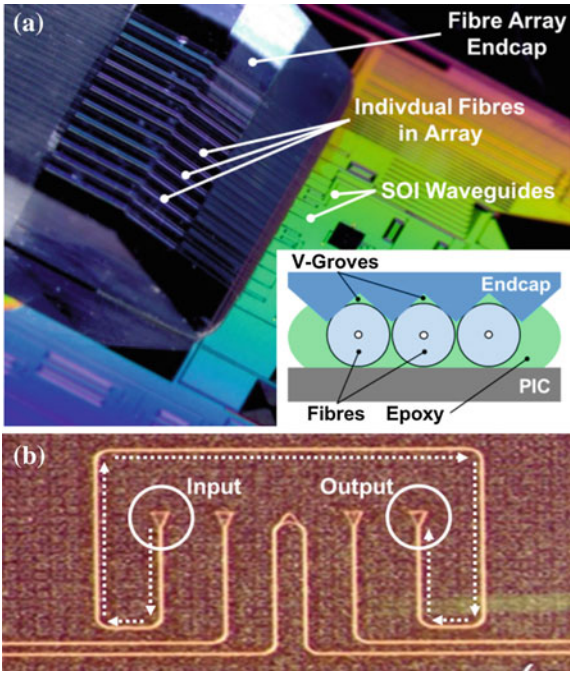

Fig. 7.4 **a** Image of a multi-channel fiber-array coupled to a Si-PIC using the quasi-planar approach. The individual fibers in the array is visible through the end-cap. The inset is a schematic of the fibers self-locating in the v-grooves of the end-cap. **b** Image of an optical-shunt on a Si-PIC. Optimizing the alignment between the fiber-array and the input and output couplers ensures the alignment of the intermediate channels

7.2.1 Fiber-Coupling

The main challenge associated with coupling light from a telecom fiber to a SOI-waveguide is the large mismatch between the mode-sizes and refractive indices of the two systems. In a single-mode telecom fiber, the mean-field diameter (MFD) for 1550 nm light is approximately 10 μm, while the cross-section of the corresponding strip SOI-waveguide is usually just 220 nm × 450 nm. The mode in the SOI-waveguide can be so small, because of the large refractive index difference between the silicon core (n_{Si} = 3.48) and silicon-oxide cladding (n_{Ox} = 1.44). This same index difference enables the small turn-radii and high integration densities that are characteristic of silicon photonics. In addition to the poor geometric overlap between the fiber-mode and the SOI-waveguide mode, polarization effects can play a key role in determining the fiber-to-PIC insertion-losses. By design, the asymmetric SOI-waveguides typically only support the TE-polarized mode, while the polarization-state of the incident fiber-mode is usually unknown and is often unstable, because of thermal-stresses and vibrations along its path length. As a result, it is often necessary to introduce some form of "polarization management" to ensure stable fiber-to-PIC coupling. This can either be implemented directly in the coupler element (as in the case of a 2-D grating-coupler [7]), or as a waveguide elements that filter and rotate the input polarization as necessary [8] (Fig. 7.5).

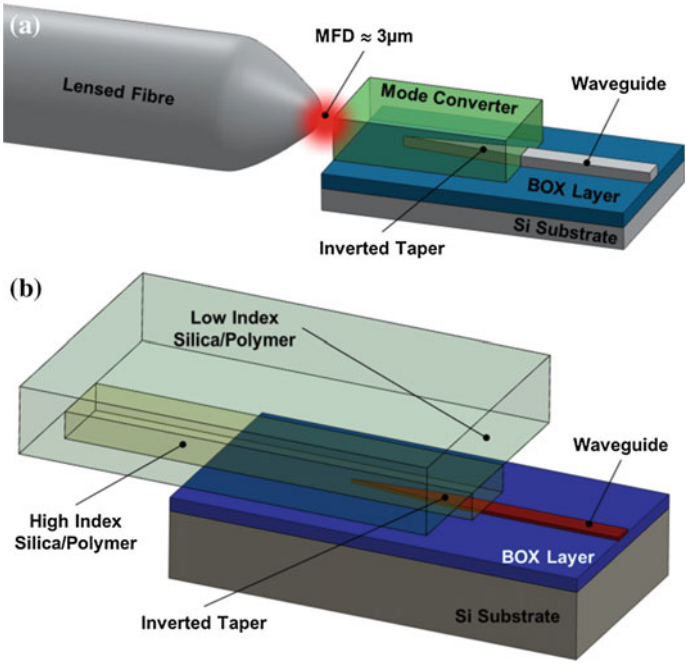

Fig. 7.5 **a** Schematic of edge-coupling between a lensed fiber and a Si-PIC with a mode-adapter and inverted taper. **b** Schematic of a recently proposed relaxed-alignment edge-coupling scheme, using an optical interposer/mode-adapter in soft-contact with the Si-PIC, for multi-channel edge-coupling

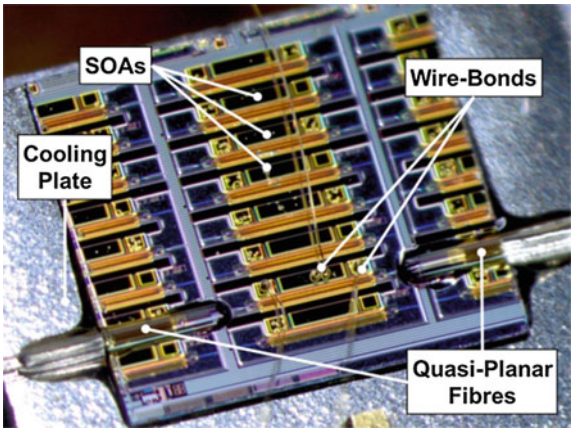

Fig. 7.6 Image of a Si-PIC, with integrated SOAs developed by IIIV-Labs in the Fabulous FP7 project, optically packaged to a pair of single fibers for performance testing. Thermo-electric cooling (TEC) is necessary during the testing, to ensure the SOAs operate within their design specifications

There are two distinct approaches to fiber-coupling: (i) edge-coupling and (ii) grating-coupling. As its name suggests, edge-coupling involves the transfer of light between the edge of the Si-PIC and the telecom fiber. Edge-coupling is already an industry-standard for the optical-packaging of III–V laser devices [9]. The alternative to edge-coupling is grating-coupling, where a sub-wavelength periodic structure is etched into the SOI-platform, creating a condition that diffractively couples light from a near normally incident fiber-mode into the SOI-waveguide [10]. Both approaches have their pros and cons—edge-coupling can offer lower insertion-losses and more broadband coupling than grating-coupling, but has significantly more stringent alignment tolerances and can require non-CMOS post-processing steps. Ultimately, the best fiber-coupling solution for a given Si-PIC is strongly application- and cost-dependent (Fig. 7.6).

7.2.2 Grating-Coupling

The active area of an SOI grating-coupler typically has a 10 μm × 10 μm footprint, consisting of a periodic array of approximately 20 trenches, partially etched into the 220 nm Si-layer [11]. For a given angle-of-incidence (θ), the pitch (P) of the grating-coupler creates a constructive interference condition for the target wavelength (λ_0), which depends on the effective index of the oxide cladding (n_{Ox}) and the partially etched grating (n_{Eff}):

$$\lambda_0 = P(n_{Eff} - n_{Ox}\sin(\theta) \tag{7.1}$$

The value of n_{Eff} is determined by the etch-depth and duty-cycle of the grating-coupler, and a near-normal angle-of-incidence (θ = 10°) provides directionality to the coupled-mode, and to reduce back-reflections into the fiber. Varying

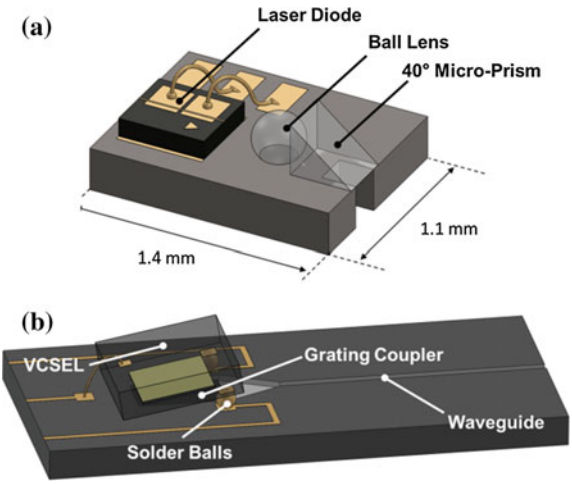

Fig. 7.7 **a** Schematic of the Tyndall-MOB, which consists of a laser diode, ball-lens, and micro-prism, self- and passively aligned on a AlN sub-mount. **b** Schematic of a VCSEL flip-chip bonded to a Si-PIC, using solder-balls to give a tilt-angle of 10° to match the acceptance angle of the grating-coupler

the tilt-angle of the fiber-mode, i.e., θ allows for some tuning of the wavelength of the grating-couplers, typically on the order of 10 nm per 1° (Fig. 7.7).

The etched trenches in the grating-coupler are often curved, to focus the coupled light into the SOI-waveguide, without the need for long adiabatic tapers. The 1 dB alignment tolerance for a typical grating-coupler can be up to ±2.5 μm, because both its footprint and the fiber-mode are on the order of 10 μm [12]. Although this tolerance is not so relaxed as to allow for passive alignment of the fiber with respect to the Si-PIC, it significantly simplifies the process of active alignment, compared to edge-coupling schemes. In addition to offering relaxed-alignment tolerances, grating-couplers can (i) be fully CMOS-compatible, (ii) be straightforward to fabricate, (iii) allow for optical access at any point on the Si-PIC surface, (iv) remove the need for PIC polishing or surface preparation, and (v) allow for wafer-scale testing and characterization of the Si-PICs before dicing. For these reasons, grating-couplers are currently the only optical-coupler element on offer to users of the multi-project wafer (MPW) runs from the IMEC and CEA-Leti Si-photonic foundries [13, 14].

The above advantages are offset by their relatively high insertion-losses of grating-couplers. Finite difference time domain (FDTD) simulations show that the minimum achievable insertion-loss between a standard fiber and a uniform grating-coupler in the 220 nm SOI-platform is –3 dB = 50 % (with pitch = 630 nm, etch-depth = 70 nm, and duty-cycle = 50 %) [15]. To make matters worse, the insertion-loses of MPW fabricated grating-couplers rarely manage to deliver insertion-losses better than –5 dB. Recently, so-called “advanced” grating-couplers (on which a 160 nm poly-silicon over-layer is added on top of the 220 nm Si-layer) have been made available to MPW users, and these promise lower insertion-losses of the order of –2 dB [16]. Several research groups have reported “hero device” grating-couplers, which use bottom-reflectors and apodized trenches to reduce

insertion-losses to less than –1 dB, but these relatively complex designs are not yet available to the wider photonics community [17].

For optimum coupling efficiency, the fiber-mode should be near-normally incident on the grating-coupler. However, if the fiber itself is optically packaged at near-normal incidence, i.e., in the "pigtail" geometry, then the overall device becomes bulky and delicate. To address this issue, a "quasi-planar" approach has been developed, in which the fiber lies on the surface of the Si-PIC, with a 40° polished facet providing a total internal reflection (TIR) condition that directs the fiber-mode onto the grating-coupler at the correct angle of 10° [18–20]. After active alignment, index-matching UV-curable epoxy is used to bond the fiber to the surface of the Si-PIC, exploiting capillary action and surface tension effects to ensure an even application of the adhesive. To ensure the TIR condition at the polished facet is not disturbed, the epoxy cannot be allowed to flow onto the facet. The quasi-planar approach has an easily manageable 1 dB "roll" tolerance of ±2.5°, in addition to the ±2.5 μm 1 dB lateral alignment tolerance, and offers an insertion-loss that is on a par with that of pigtail coupling [20].

For many applications, multiple fiber-channels to the same Si-PIC are needed. Instead of sequentially aligning several individual fibers (which is not practically possible, because of clearance issues), the solution is to use a fiber-array. A fiber-array consists of a glass end-cap, in which v-grooves have been precision-etched with a pitch of 127 μm or 250 μm (matching the diameter of standard telecom fibers), and into which the fibers are inserted. In pigtail fiber-arrays, a "lid" is often added to create a "three point contact" condition that ensures proper centering, but in quasi-planar fiber-arrays the end-cap must be lid-less, so that the fibers can lie in close contact with the surface of the Si-PIC [20]. The precision v-grooves locate the inner-cores of the fiber-channels to within ±1 μm, a nominal position defined by the pitch and etch-depth of the groves in the end-cap. This is well within the ±2.5 μm 1 dB alignment tolerance of the grating-couplers, and so actively aligning the two outer channels of the fiber-array to the Si-PIC also ensures the alignment of all intermediate channels. The outer channels are usually actively aligned by maximizing the fiber-to-fiber transmission across an optical-shunt between two grating-couplers on the Si-PIC. With this approach, multiple fiber-channels (often up to 16) can be aligned for the "cost" of a single active alignment. After alignment through the shunt, index-matching UV-curable epoxy is used to bond the fiber-array to the surface of the Si-PIC (Fig. 7.8).

Ongoing work is directed toward the development of novel designs that do away with the need for active alignment in grating-couplers. For example, flip-chip alignment and bonding of a fiber-array to a grating-array has recently been demonstrated, and suffers a performance penalty of just 0.5 dB compared to active alignment [21]. In this approach, a beam-splitting image-system is used to directly align the inner-cores of the fibers with their corresponding grating-couplers on the Si-PIC, and bring the two components together with a tolerance of better than ±1 μm. Since this is well within the ±2 μm 1 dB alignment tolerance of the

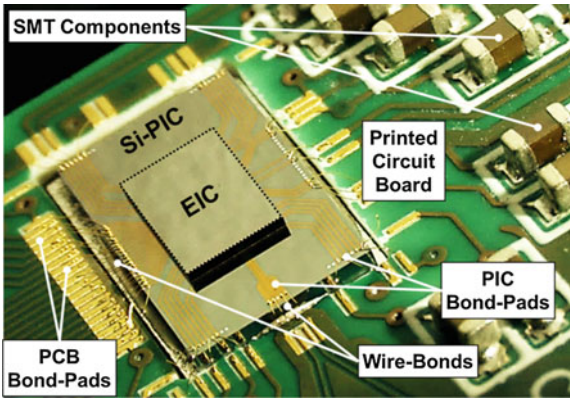

Fig. 7.8 Image of a Si-PIC (with flip-chipped electronic-IC) electrically connected to a surrounding printed circuit board (PCB) using approximately 50 wire-bonds. To keep the wire-bonds as short as possible, it is best to match the pitch of the PCB-side and PIC-side bond-pads. In this image, for clarity of illustration, the fiber-array has not been added to the PIC

grating-couplers, this approach offers an insertion-loss comparable to that of active alignment, but with a much shorter alignment time.

7.2.3 Edge-Coupling

The most convenient means of coupling light from an edge-emitting III-V laser device into an optical fiber is edge-coupling—it is a well-established approach for the commercial packaging of laser-chips [9]. However, in the field of Si-photonics, edge-coupling has been far less widely adopted, despite being able to deliver broadband, polarization-agnostic insertion-losses of better than –1 dB, after careful alignment [22]. A typical edge-coupler on a Si-PIC consists of a relatively long (typically 300 μm) inverted taper, on which a polymer- or nitride-based mode-adaptor has been added using a post-processing step [23, 24]. Since adding the mode-adapter is not a standard CMOS processing step, edge-couplers are not yet offered as part of the IMEC or CEA-Leti MPW runs (although there are rumors that edge-couplers will be included in the 2016 MPWs). Introducing an edge-coupler onto a Si-PIC tends to substantially increase the processing costs, because it usually calls for the accurate dicing and optical-grade polishing of the PIC edges. Edge-coupling schemes, in which V-grooves are etched directly into the SI-PIC, to passively align the fibers with respect to the SOI-waveguides, have been proposed and demonstrated [25]. However, this approach also adds to the fabrication costs, and has the additional drawback of populating a significant fraction of the usable Si-PIC footprint with V-grooves.

Edge-coupling is usually made to/from a lensed-fiber, with a focal length of the order of 3 μm, to reduce insertion-loses by improving the modal overlap with the mode-adapter. The 1 dB alignment tolerance for a typical edge-coupling is sub-micron (approximately ±500 nm), and so requires careful active alignment [22]. Such tight alignment tolerances make edge-coupling to a fiber-array extremely challenging, and so the majority of optical-packaging for edge-couplers is restricted to single-fiber channel applications. Laser-welding is the preferred means of securing the lensed-fiber (mounted in a metallic ferrule) with respect to the Si-PIC, after alignment [9]. Laser-welds do not suffer from the small alignment-drift that sometimes occurs in epoxy-bonds due to age or environmental effects. These drifts are not relevant in grating-coupler schemes, because of their more relaxed-alignment tolerances, but cannot be ignored with the ± 500 nm 1 dB alignment tolerance of edge-couplers. For similar reasons, it is recommended that modules with edge-couplers are mounted in a *Kovar* package, to minimize the effects of thermal expansion and contraction on the optical alignment.

A number of groups are working to develop schemes that reduce the alignment tolerance of edge-coupling, with the aim allowing multiple fiber-channels to be made at the same interface [26, 27]. One interesting approach is to build the functionality of the mode-adapter into an "off PIC" interposer that can be flip-chip aligned and bonded to the inverted tapers on the Si-PIC. This would allow for passive alignment, and mode-size conversion between the SOI-waveguides and the telecom fibers, all without the need for facet-polishing or V-groove etching. Should it be possible to develop a relaxed-alignment multi-channel edge-coupling scheme for Si-PICs, it is quite possible that it would quickly supersede the current dominance of grating-couplers in the field. The high insertion-losses of grating-couplers are routinely identified by industrial partners as a significant barrier to more widespread commercial adoption of Si-photonics.

7.2.4 Laser Integration

There are essentially two schemes for Si-PIC laser integration—hybrid and heterogeneous integration. Heterogeneous integration refers to the bonding of III-V gain material onto the Si-PIC (either directly or with an intermediate polymer adhesive layer), followed by an etching of the III-V material to create the cavity condition needed for lasing. The cavity can be formed between two etched facets, two Bragg reflectors, or even as a micro-ring, depending on the application [28, 29]. The resulting laser emission is usually evanescently coupled into an underlying SOI-waveguide, for distribution to the rest of the PIC. In contrast, hybrid integration involves the coupling of light from a stand-alone discrete III–V laser device into SOI-waveguide, by means of an intermediate micro-opto-electro-mechanical (M-OEM) system. In principle, heterogeneous integration schemes allows for higher integration densities and lower profile devices, but it tend to suffer from

significantly lower device yields and larger performance variation, compared to the "known good device" approach of hybrid integration.

Heterogeneous integration can be considered more as a post-processing step in the fabrication of the Si-PIC, rather than a true packaging step. Heterogeneous integration is often used to embed semiconductor amplifiers (SOAs) onto the SOI-platform, instead of true laser devices. SOAs are an important element of practical Si-PICs, because the optical-gain they provide is used to offset the high insertion-loses and distributed-loses [30]. Electrical packaging of SOAs is generally straightforward, and involves the connection of only a few DC wire-bonds. Heterogeneously integrated SOAs are particularly temperature sensitive, and so need to be cooled to close to room-temperature, for optimum performance.

7.2.5 Micro-Optic Hybrid Integration

Light from a hybrid laser device can be inserted into the SOI-waveguide, by means of edge-coupling to an inverted taper (possibly with the addition of a mode-converter), or by using a grating-coupler. The near-vertical geometry afforded by grating-coupling means that the laser-assembly (usually consisting of a laser-chip and some focusing/steering optics) can be suspended above, or to the side of the Si-PIC, saving valuable "real-estate" on the chip for other components.

Luxtera and Tyndall have both developed hybrid laser integration schemes based on the principle of a micro-optical bench (MOB) [31, 32]. The MOB consists of an AlN or Si sub-mount, on which a (i) an edge-emitting laser-chip, (ii) micro ball-lens, and (iii) reflecting element are aligned and mounted. Light from the laser is collected and focused by the ball-lens, and imaged onto an underlying grating-coupler at near normal incidence by the reflector. Each component on the MOB has a dimension of the order of 300 μm, so the overall footprint is approximately 1 mm × 1 mm. In the hermetically sealed Luxtera MOB, a micro-optical isolator is used to reduce feedback to the laser.

In the case of the Tyndall-MOB, the 300 μm ball-lens self-aligns in a precision laser-drilled hole, which provides a locating reference-point/surface for the micro-prism and laser-chip. This approach means that the MOB can be assembled through a combination of self- and passive-alignment steps. *Zemax*, or other ray-tracing software, is used to determine the optimum dimensions and working-distances of the MOB components. Provided the laser-spot imaged onto the grating-coupler closely matches that of a telecom fiber-mode, the MOB insertion-loss is dominated by the grating-coupler performance. However, if the laser-spot imaged onto the grating-coupler is larger or more asymmetric than a fiber-mode, then an additional performance penalty of up to 3 dB can occur [32]. There is now a drive to optimize grating-coupler designs specifically for free-space coupling to hybrid sources.

To minimize insertion-losses, the MOB must be actively aligned with respect to the grating-coupler on the Si-PIC, and has a 1 dB alignment tolerance that is

comparable to that of Fiber-to-PIC coupling. Once aligned, the MOB should be bonded to the PIC using a thermally conductive epoxy, to ensure that heat can be efficiently conducted away from the laser-chip. Without good thermal contact, the laser-chip can overheat and "burnout." A thermo-electric cooler (TEC), mounted underneath the Si-PIC, is often used to ensure the wavelength stability of the source (temperature tuning of a laser-chip is of the order of 0.1 nm/°C) [33].

7.2.6 VCSEL Hybrid Integration

Hybrid integration of vertical cavity surface emitting lasers (VCSELs) is also possible. Here, the advantage over edge-emitting lasers on a MOB (1 mm × 1 mm) is the significantly reduced footprint of the VCSEL chip (250 μm × 250 μm). This allows for a higher integration density, when the VCSELs are bonded directly on the Si-PIC surface. There are two main challenges associated with the optical packaging of a VCSEL onto a Si-PIC: (i) aligning the laser-spot of the VCSEL onto the 12 μm × 12 μm active are of the SOI grating-coupler, without any intermediate focusing/steering optics, and (ii) ensuring that the laser beam from the VCSEL is incident on the grating-coupler with the correct 10° angle-of-incidence.

One solution is to insert the VCSEL into a PCB sub-mount that has been polished to give the VCSEL the necessary offset-angle, when the sub-mount is flush on the Si-PIC surface. In this case, the VCSEL can then be actively aligned with respect to the grating-coupler, using in-plane adjustments. A second approach is to flip-chip the VCSEL directly onto the Si-PIC, using an asymmetric distribution of solder-balls to create a tilting effect. By engineering the bond-pad sizes, surface tension effects can be used to give VCSEL the necessary tilt-angle [34]. This approach allows for passive flip-chip alignment of the VCSEL, which allows for much faster assembly, but at the cost of (potentially) higher insertion-losses.

In many cases, the beam-profile and divergence of the VCSEL is markedly different to that of a single-mode telecom fiber. This can lead to unacceptably high insertion-losses, when the VCSEL is coupled to a standard grating-coupler, even after active alignment at the correct acceptance angle. Grating-coupler designs optimized for free-space coupling to VCSELs are now beginning to emerge. As these designs mature, it is likely that VCSEL-to-PIC insertion-losses will converge to fiber-to-PIC losses, i.e., 3 dB for standard grating-couplers.

7.3 Electrical Packaging

Optical packaging based on single-mode fibers and the integration of active devices and micro optical components receives most of the attention in reviews of photonic packaging. However, the packaging of electrical interconnects on a photonics chip can be just as challenging as the optical packaging, especially for high-speed

electrical signals (>10 GHz). Practical considerations, such as the need to ensure adequate spacing between electrical and optical ports, are often overlooked by designers, and can lead to reduced device performance, or, in the worst-case scenario, a device that is essentially impossible to package.

Electrical packaging of Si-PICs with electronic drivers, amplifiers and other control circuitry is becoming an ever greater challenge, as demand grows for higher levels of photonic-electronic cointegration. The limited space within a package and the need to support radio-frequency (RF) operating signals have a significant impact on the cost and performance of electrical transmission lines, RF-substrates and RF-connectors. Although it is one of the ultimate goals of silicon photonics, the monolithic integration of photonic and electronic functionality on the same chip is still largely aspirational with current technology. Most designers adopt a hybrid integration approach, either flip-chipping an electronic-IC onto the PIC, or simply connecting the Si-PIC directly to a PCB, on which there can be many electronic components, using wire-bonds. As a practical consideration, this approach can allow for a separation of the CMOS fabrication processes between the 32 nm node in the electronic-IC that supports high-speed electronics, and the less costly 90 nm node needed for the photonic elements.

Furthermore, the integration of electronic-ICs with Si-PICs introduces additional, and often significant, complications to the thermal management of the module. Heat must be efficiently dissipated from the Si-PIC, for stable operation of the photonic components, but some integration schemes call for the conduction of heat from the electronic-IC *through* the Si-PIC. In this section, we review progress in the electrical packaging of Si-photonics, and consider the merits and implementations of 2.5-D versus 3-D integration processes, and the key design issues in the management of thermal effects.

7.3.1 Packaging to PCB

The electronic connections between a Si-PIC and the "outside world" are made using the same wire-bond process developed for electronic circuits. The pitch of DC bond-pads on the Si-PIC is limited to approximately 100 μm to limit the risk of shorting between adjacent ball-bonds. The minimum pitch for a low-attenuation 50 Ω transmission-line on a high-dielectric Rogers-Layer PCB is approximately 300 μm, and so the pitch of RF bond-pads on the corresponding Si-PIC is also 300 μm. For RF Si-PICs that need higher integration densities, a ceramic interposer can be used as a pitch-converter.

7.3.1.1 3-D Electronic Packaging

For very high-speed designs, hybrid flip-chip integration of electronic devices directly on the Si-PIC can bring performance advantages. This face-to-face 3-D

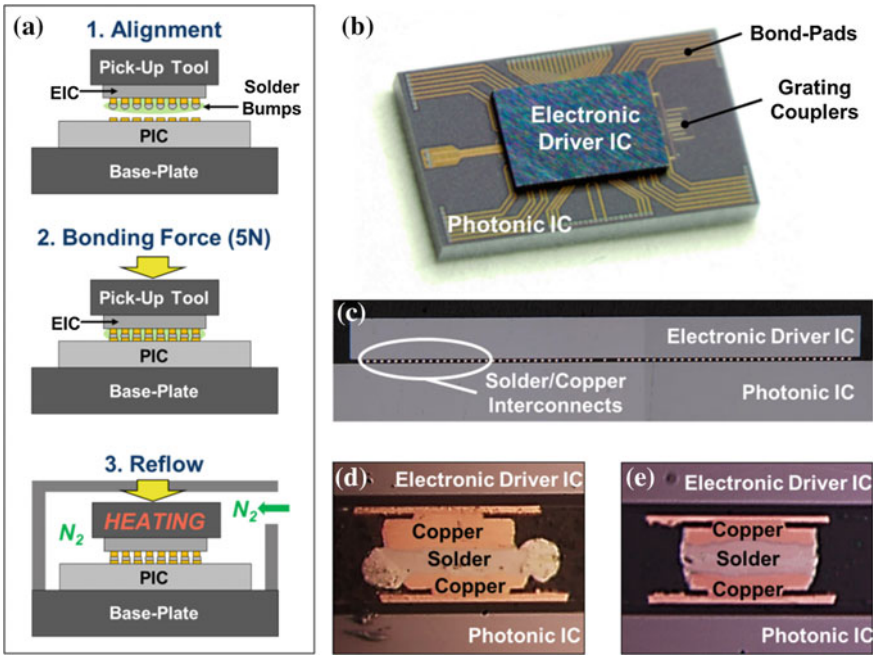

Fig. 7.9 **a** Procedure for the flip-chip alignment and thermo-compression bonding of an electronic-IC to a Si-PIC. **b** Image of the integrated electronic-IC and Si-PIC used in the EU-FP7 FABULOUS project. **c** Cross-section image of the interface between the flip-chipped EIC and PIC, showing multiple interconnects. **d** Microscopy cross-section of a solder/copper interconnect where too much pressure was applied during the thermo-compression. **e** Cross-section of a properly formed solder/copper flip-chip interconnect. "some lettering in the fugue sections is hard to read and needs enlarging"

integration approach replaces long wire-bonds with short interconnects, minimizing parasitic effects, such as increased inductance, which can significantly affect high-RF performance [35–37]. The flip-chip bonding uses micro-bumps (typically solder bumps) to form interconnects between the bond-pads on the electronic-IC and Si-PIC chips. Solder-ball jetting of spheres down to 50 μm diameter is a standard means of depositing interconnect material, with electroplated bumps fabricated directly on the chip allowing even smaller diameters. The most commonly used micro-bumps are copper-pillars, typically fabricated with a diameter of 20–30 μm. These pillars are usually capped with a thin (typically 5 μm thick) solder-alloy layer, such as AgSnCu. Figure 7.9 illustrates the flip-chip thermo-compression integration process. Solder-reflow bonding is also possible, providing a no-clean flux is used, to avoid contamination of the optical interfaces of the Si-PIC.

The stable operation of a Si-PIC requires a considerably more stringent thermal management than that of an electronic-IC, and 3-D integration has a strong impact on the thermal properties of the Si-PIC. The performance of many key photonic

building-blocks, including SOAs and micro-ring resonators, are strongly temperature dependent, and require active cooling, using thermo-electric coolers (TECs), for temperature stabilization [38, 39]. 3-D integration generally involves the conduction of heat dissipated in the electronic-IC *through* the micro-bump interconnects and Si-PIC, before heat-sinking into the cold-side of the TEC. This adds thermal resistance to the design, and elevates the nominal temperature of the Si-PIC, both of which reduce the efficiency of the TEC cooling. Despite this, a properly designed package, with active feedback from an embedded thermistor, can maintain the steady-state temperature of the Si-PIC in a 3-D integrated stack to ±0.01 °C of a room-temperature set-point. However, the power budget of the TEC can be of the same order as the electronic and photonic components, adding considerably to the operation costs of the module (Fig. 7.10).

An ongoing goal of research into thermal packaging is to gain a better understanding of how heat is dynamically distributed within the photonic package, and what heat dissipation features can be added to enable more efficient thermal management. Both COMSOL finite-element simulations mid-infrared imaging are used to investigate the thermal properties of 3-D integrated stacks and packaged modules. The aim is to better configure the location of thermally sensitive components (like SOAs, array waveguides (AWGs), multi-mode (MMI) couplers, etc.) on the Si-PIC, and to minimize thermal drift of the module.

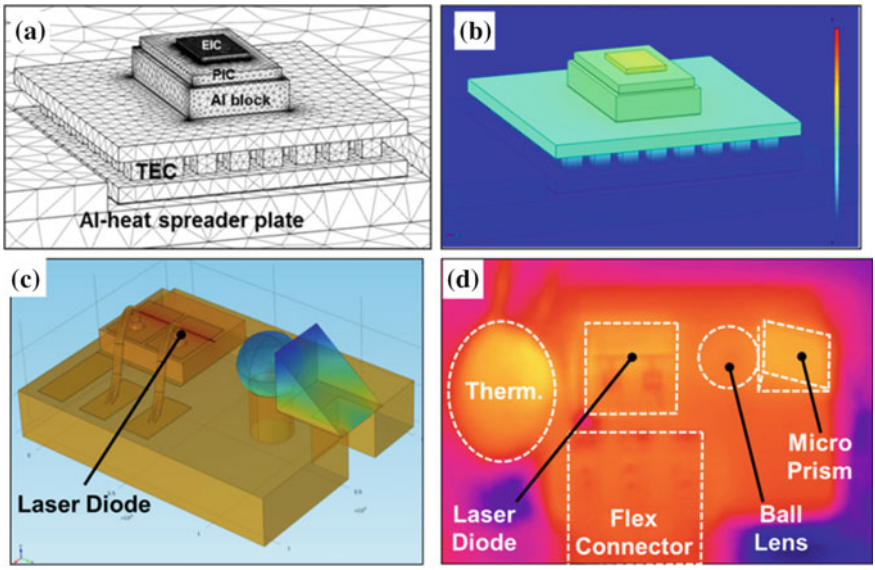

Fig. 7.10 **a** and **b** Thermal simulations of a Si-PIC on which an electronic-IC (EIC) has been flip-chip integrated. Heat flows from the EIC through the PIC, and is trasnferred across the thermo-electric cooler (TEC). **c** Thermal simulation of the Tyndall-MOB showing excessive heating of the active region in the laser diode, during uncooled operation. **d** Thermal microscope image of the Tyndall-MOB showing a nearly uniform temperature distribution, after TEC cooling

7.3.1.2 2.5-D Electronic Packaging

2.5-D integration, sometimes known as side-by-side integration is a compromise solution for 3-D flip-chip integration that allows for relatively high-speed interconnects, without the need to conduct the "waste" heat from the electronic-IC through the Si-PIC. In 2.5-D integration, the electronIC and Si-PIC are placed side-by-side, on top of an electrical interposer that serves as an interface for the two devices [40, 41]. Using through-silicon-vias (TSVs), the distance between the electronic-IC and Si-PIC can be made relatively short (of the order of mm), and the interposer designed with RF transmission lines, such that the high-speed performance can be almost as good as that of 3-D face-to-face integration. The advantage is that only the (minimal) heat evolved on the Si-PIC itself need be removed, in order to ensure the reliable operation of the module—this makes for more efficient TEC stabilization, and a reduced power budget for cooling. The electronic-IC element of the module can be passively cooled, and vary within a large tolerance, before its performance is significantly impacted, which allows for relaxed design considerations in the overall packaging for 2.5-D integrated Si-PICs.

7.4 Standardization

The need to create standardized design rules for photonic packaging is slowly gaining recognition in the Si-photonics community, driven by the dual advantages of removing a design-burden from researchers/engineers, and streamlining the design-to-device process. Developers of photonic packaging solutions are working with industry partners to establish packaging/processing design kits (PDKs) and rules (PDRs) to help users ensure that their Si-PICs and photonic devices are compatible with reliable and cost-effective best-practices in photonic packaging The implementation of these packaging design rules will be especially beneficial to new entrants to Si-photonics space, by helping avoid costly design mistakes that could result in a newly designed Si-PIC being impossible to fully package. Critical PDR parameters include the pitch of grating-arrays on the Si-PIC, the pitch of fibers in the fiber-arrays, the pitch of DC and RF bond-pads, the metallization-type of bond-pads, and the location of coupling elements (grating-couplers and edge-couples) with respect to the electrical interconnects.

Although currently at an early stage of development, it is expected that these packaging design rules will become more widely adopted, especially at the layout phase of the chip-design process. To increase their ease of use, the PDKs are being implemented in software layout tools and templates [42, 43]. This will allow designers to easily access and implement the packaging rules, in conjunction with the photonic elements available from different Si-photonic foundries.

7.5 Conclusions

The growing interest in Silicon photonics is mainly driven by its ability to satisfy demands in large markets, particularly for telecoms, datacoms and sensing applications. Device fabrication based on wafer-scale processes can meet this demand. However, packaging can be a device-by-device process which is difficult to scale, and packaging challenges remain in areas such as fiber-array coupling, source and electronic integration and efficient thermal management.

The sub-micron alignment tolerances needed for the optical-packaging of fibers and laser sources is perhaps the most recognized issue, but electrical packaging and thermal management of Si-PICs are also important (if somewhat overlooked) factors in successful packaging.

As more companies take new devices to market, there is a growing need to develop automated packaging processes that enable higher volume production. To meet this challenge, researchers in photonics packaging are working to develop wafer-scale solutions for laser integration based on passive or machine-vision alignment techniques. Demands for more compact designs, operating at higher frequencies, is pushing photonic packaging toward the 2.5-D and 3-D integration of electronic and photonic devices. These approaches raise new challenges in terms of thermal management, requiring a careful balance between achieving the temperature stability needed for reliable operation, with the power budget available for cooling. Finally, the creation and implementation of new packaging design rules aim to help developers avoid costly mistakes, by ensuring that their Si-PICs and photonic modules are compatible with best-practices in photonic packaging.

There is no doubt that challenges remain in the field of photonic packaging for Si-photonics, but researchers are working with advanced design-tools and evolving packaging-equipment to overcome these challenges.

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Chapter 8
Silicon Photonics Packaging Automation: Problems, Challenges, and Considerations

Giovan Battista Preve

Abstract This chapter will give a survey on the problems and the challenges related to the necessity to automatize the fiber array pigtailing and the laser integration in relation to silicon photonic devices. In fact the only way to make silicon photonics technology really exploitable at industrial level is to solve the manufacturing bottlenecks that nowadays limit the applicability of the technology, in particular related to the multiple optical outputs pluggability and the laser integration.It will start giving some detailed information on what have been developed so far in terms of state-of-the-art pigtailing-automated benches, robotics and their present limitation, making consideration on what will be necessary in the near future.It will then give a survey and an evaluation, respect to automation, on some of the most recent and interesting developments for silicon photonic packaging, in particular for the optical fiber coupling and the future desired pluggable solutions.

8.1 Introduction

Today, pigtailing and assembly are important cost factors for photonic modules. In the future, with more advanced photonic–electronic integration on the roadmap, pigtail and assembly technologies will be the cost drivers for module manufacturing if hitherto applied technologies continue in use. Therefore, only major progress in pigtailing and assembly will enable leveraging the full potential of advanced integrated photonic and electronic circuit technologies.

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Table 8.1 Time required for each process step, showing the relative impact on overall process time for each phase

Process step	Time required (s)	Percentage on total process time (%)
Bench initialization	30	3.9
Pick and place TV	60	7.8
Pick up FA	120	15.4
Grating inspection	30	3.9
Measure FA angles	75	9.7
Measure height	95	12.2
Detect FA and prealign	135	17.4
Glue FA	200	25.8
Release FA	30	3.9

Such progresses must be compliant with the necessity to have industrial automation. We cannot imagine that proper high volume production can be reached in silicon photonics without the development of proper pigtailing technologies scalable to automated processes.

In general it can be said that pigtailing and packaging automation is one of the main, if not the principal, bottlenecks in silicon photonics as well as in optoelectronics. In fact when the final product includes optics, automatically we have to deal with micron or submicron tolerances, critical handling, general limitations strictly related to the optical components (silicon photonics devices, laser diodes, pin diodes, fibers, lenses, etc.), and optical paths and all these limitations make it really difficult to have automatic procedures and processes similar to the existing ones utilized and validated for microelectronics.

In any case, for the reasons mentioned above, if we want real silicon photonics exploitation, the automation is a task that has to be taken into account both in terms of facilitating technologies as well as in terms of equipment. In fact, industries (both equipment suppliers and device/system suppliers) and university institutions have already started to work on it and to give answers to the various issues related to automation. However, no final solution has been successfully implemented.

In this chapter, we give a brief survey of what is necessary and what is currently under study and under development, providing a perspective on which technology looks more automation oriented or not.

To begin with, we examine the automation developed for a real case and we describe what are the actual limitations on silicon photonics automation.

Following this description, we briefly illustrate some emerging pigtailing technologies and we look at them from the automation point of view, trying to see the positives and negatives from this specific perspective.

8.2 Automated Fiber Array Pigtailing on Gratings

It is well known nowadays that the major problems related to silicon photonics packaging are twofold:

- Optical interconnection to fibers
- Laser integration on PIC

Concentrating now briefly on the first one, clearly the major problem stems from the large mismatch in the mode size of waveguides (∼a few hundreds of nanometers) and standard single-mode fibers (SMF; ∼10 μm), which is illustrated in Fig. 8.1.

Various spot-size converters and coupling schemes between the silicon waveguide and fiber have been demonstrated during the years, with losses down to around 1 dB. However, most complex integrated circuits require a high optical "pin-out." Consequently, achieving high-yield, low-penalty coupling to arrays of fibers is the real target. Many solutions to overcome low-efficiency coupling have been proposed and a lot of work has been done trying to improve performance in terms of losses. They follow, in general, one of the following two approaches:

- Lateral coupling (in plane) using generally 2-D spot-size conversion
- Vertical coupling (out of plane) using diffraction via gratings [1]

Over the years, vertical coupling technology has clearly taken an edge over the other. In fact coupling to silicon photonic wires through high-index contrast gratings is a winner because of the relaxed alignment tolerances compared to facet coupling. Grating couplers in fact match standard single-mode fibers and in general

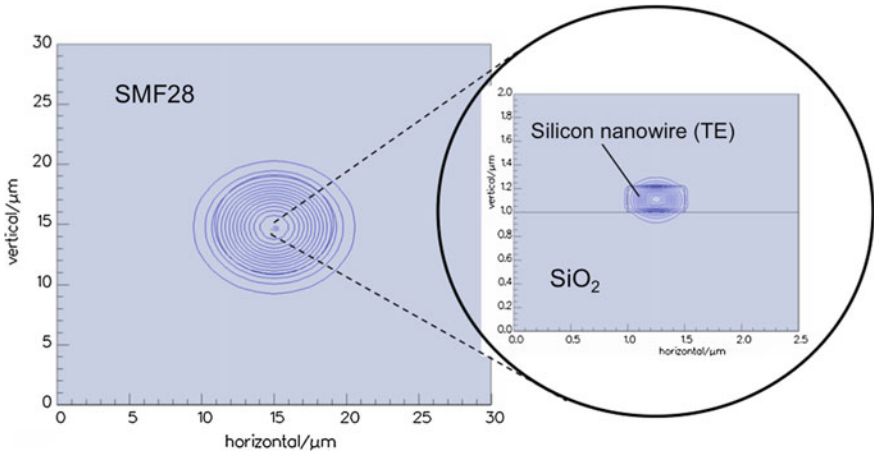

Fig. 8.1 Intensity distribution (modesize) of a standard telecom (SMF28) and a silicon nanowire (TE). The difference in scale is evident. Without mode size adaptation techniques, coupling loss would be in excess of –16 dB

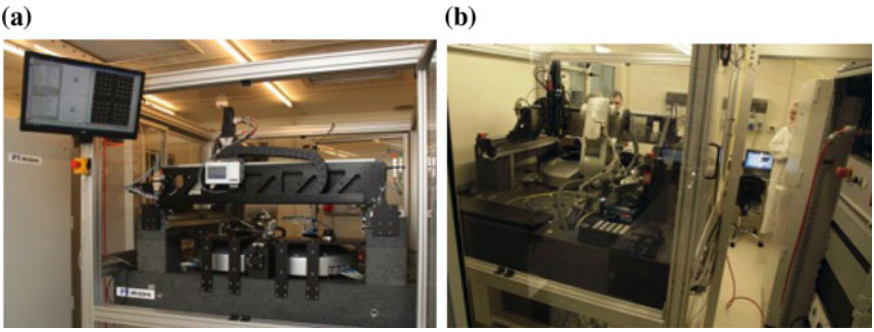

Fig. 8.2 **a** Front view of the automated bench showing the two six-axis platforms and the gantry over them, **b** Rear side of the bench with the robot and the loading stations

there is a penalty of 1 dB for tolerances of ±1 μ on the XY plane around the optimum position and, again in general, a few microns on the perpendicular Z-axis.

With such tolerances it is in fact possible to align and pigtail multiple output fiber arrays to arrayed gratings with reduced optical losses.

Such kind of technological approach (fiber arrays on gratings) is nowadays quite classical in silicon photonics pigtailing [2, 3], but it is still mainly operated in manual mode and based on operator depending processes. The question is: is it possible to have automated processes, operator independent, using this technological approach? How much time can be saved for manufacturing? And more: what are the limits?

To answer to the previous questions, we will describe the bench and the work done at the Inphotec laboratories of Scuola Superiore Sant'Anna in Pisa. In fact such work was mainly focused on automated pigtailing processes of silicon photonics components and will help us to make some conclusions at the end of the paragraph, introducing to the next section where we will try to analyze if better technological approaches are possible and briefly describe them.

The pigtailing bench itself was designed and realized with a system equipment supplier and is shown in Fig. 8.2.

It consists of two six-axis platforms with submicron accuracy, a central stage, a robot, two cameras (1 visible, 1 IR), and a gantry stage fully equipped. The concept behind the overall system is that it has to be completely automatic and that, as a consequence, the operator has to interfere as least as possible during the process. The robot was introduced to make it possible to load and unload the parts as well the epoxy application and curing. The robot path can be programmed and so it is possible to handle properly most of the delicate optical parts in a repeatable way. The robot in itself is not a must; what it is important, from an automation point of view, is the possibility to handle parts and to apply/cure epoxy in a safe and repeatable way with no operator intervention.

The array we consider here, as an example, is a standard 12-way fiber array angled 8° and with a ribbon cable output with MT/MPO connector. The total length

Fig. 8.3 12-way fiber array ribbon inside its bag

of the ribbon is 1.5 m. For the specific application, the fiber array has to be mounted perpendicularly, but the automation concepts described below can be applied to any kind of fiber array design (for example, the Tyndall style that utilizes a total internal reflection in the array and can assure a better horizontal form factor).

Figure 8.3 shows the chosen array inside the bag as supplied by the vendor. This is a quite standard way to receive the product.

It is evident that the way the arrays are normally delivered is not ideal for the task of automation. In fact, before starting the process, the array is manually taken out carefully from the bag, the ribbon is unrolled and the entire part is finally placed aside on a rack, ready to be loaded manually on the bench by the operator at the proper time. This is quite a time consuming procedure; in general it takes around 2–3 min. It is worth mentioning because of the general issues in terms of total process time related to the complete automation procedure. It is clear that the use of an array with a 1.5 m long fiber is in itself a bottleneck in terms of automation. After the preparation of the array, the silicon photonic device (stand alone or inside a package) has to be placed in the proper loading area, where the robot will pick up and place them in a second phase. An example of the pickup area is shown in Fig. 8.4.

This area can be considered standard in terms of preparation and automation.

Once the parts are placed in position and ready, it is possible to launch the complete procedure and process that from now on has to be completely programmed and completely automatic (with some exception as will be mentioned).

As in any automatic procedure, the first part of the process has to provide the loading of the parts:

1. The robot picks up the silicon photonic chip and places it on the central stage using the corresponding tool on the wrist (see Fig. 8.5).

Fig. 8.4 Pickup area of the bench. Package loading station and silicon subassemblies in gelpac box are shown as examples

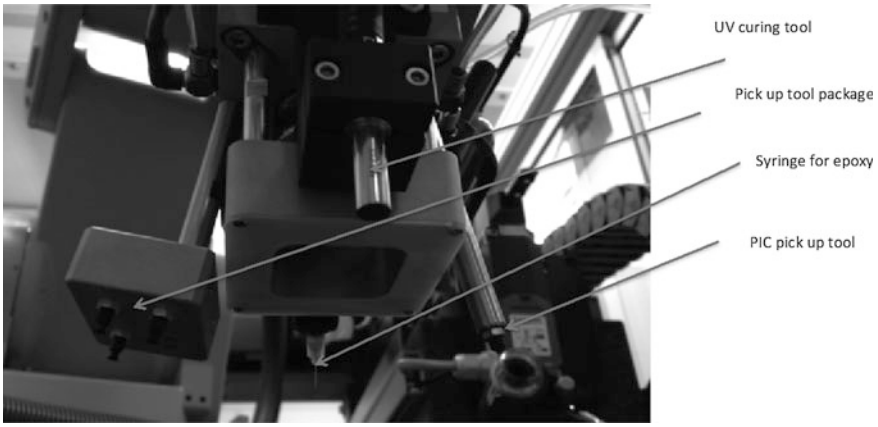

Fig. 8.5 Robot wrist with the different tools scope evidenced

2. Then it is necessary to load the fiber array. As previously mentioned the array itself has been already prepared out of its box. It is important to properly design the gripper and define the mechanical tools for holding the array. In fact the ribbon can apply a big stress and a tension that can result in an imperfect hold during the pigtailing. It has to be guaranteed that the array is properly kept so as to have a safe and repeatable process. As a consequence, as shown in Fig. 8.6, it is better to have a specific load section where to place the array, a special gripper integrated with a mechanical arc behind to guide the ribbon and reduce tensions, and finally a magnetic clamp to firmly fix the ribbon.

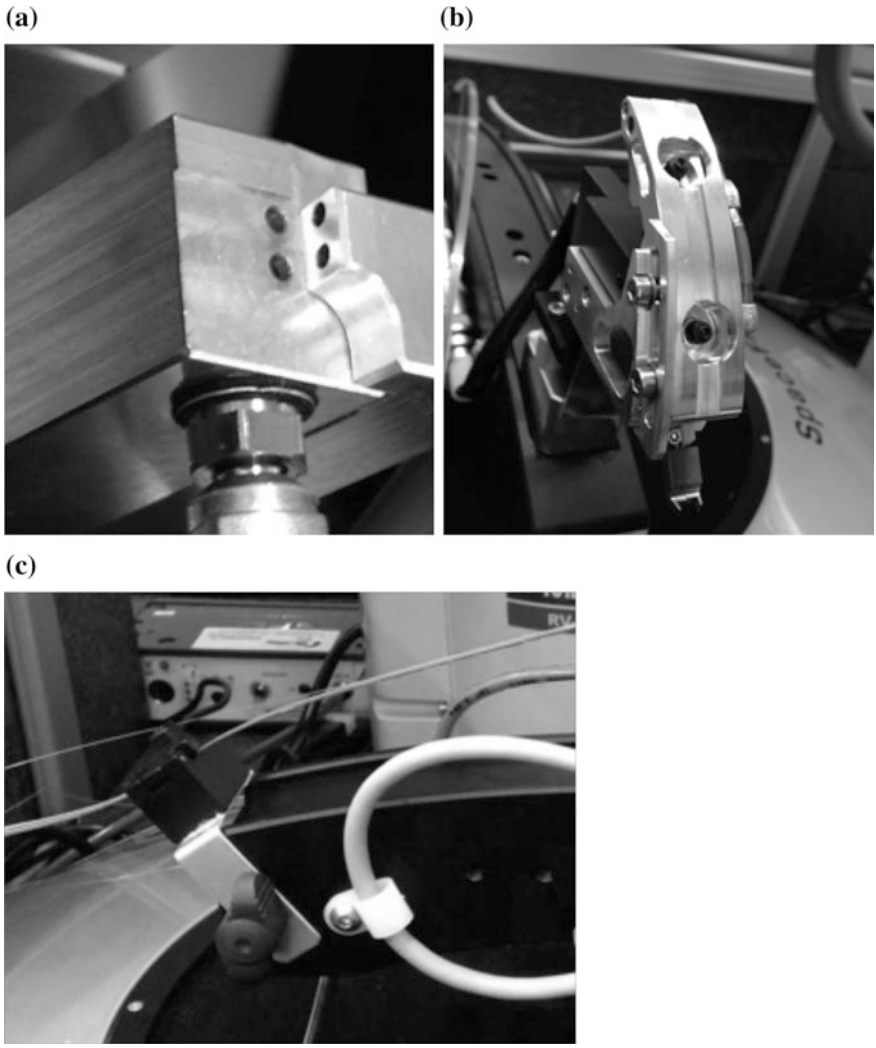

Fig. 8.6 **a** Array load section, where the fiber array is placed and the vacuum through the holes keep it in position to help the gripping phase, **b** gripper with the mechanical arc to reduce stresses, **c** clamp on the rear of the holder to firmly keep the ribbon in position

It is useful to note that, during this phase, the gripper is automatically positioned over the central loading area and waits for the operator manual load of the fiber array. The combination of intermediate station and mechanical gripper positioning gives the best help to the operator for loading the array itself and reduce loss of time. In general, if the intervention of the operator is unavoidable, basically it is necessary to design the mechanical parts so as to minimize the operator's handling. The following photos show some details of this setup, as an example (Fig 8.7).

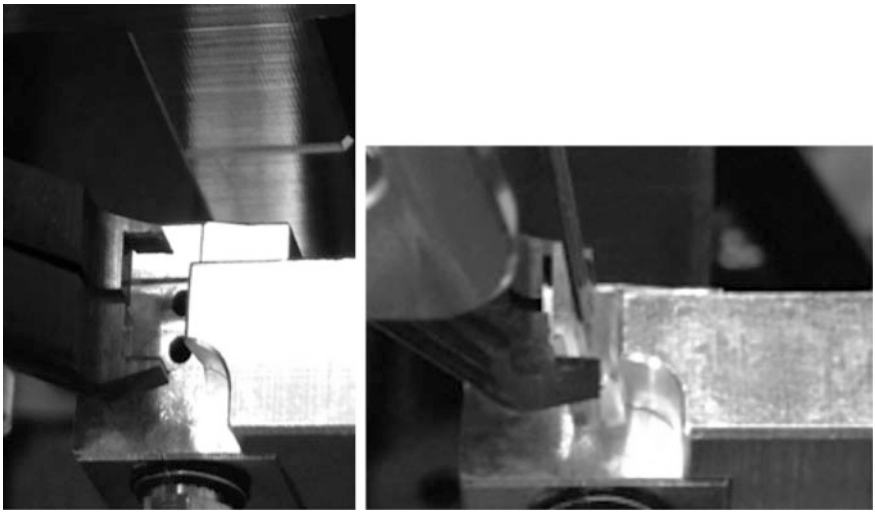

Fig. 8.7 *Left*—gripper on the tool waiting for manual load of array, *right*—fiber array placed on the intermediate station inside the gripper

Finally, the MPO connector is connected through an adaptor to a permanently placed fan-out that separates the ribbon cable to single fibers connected to the instrumentation.

As mentioned above, the solution shown here is related to the specific design of the array and to the vertical orientation of the pigtailing. In any case the basic concepts apply also to the horizontal array orientation. When all the parts are finally loaded, the best way to find the prealignment position (the so-called "first light") is to use vision and imaging techniques to recognize the position of the gratings and the position of the fiber array.

Specifically:

- During grating inspection the top camera goes over the PIC substrate and, depending on the specific design, it recognizes the position of the gratings where we have the loop waveguide for the alignment. A snapshot example of the gratings during inspection and vision recognition is shown in Fig. 8.8. At the end of this step the bench has the X/Y coordinates of the position where to place the array for prealignment. It is also necessary and possible at the same moment to calculate the proper angle so as to compensate the angle differences with the array.
- During fiber array inspection the routine makes many automatic procedures in the following order, as briefly described:
- Measure the FA angles utilizing the top camera and mirrors properly placed (to reflect images to the top camera) so that it is possible to have the best possible angle alignment between the FA and silicon photonic chip gratings.

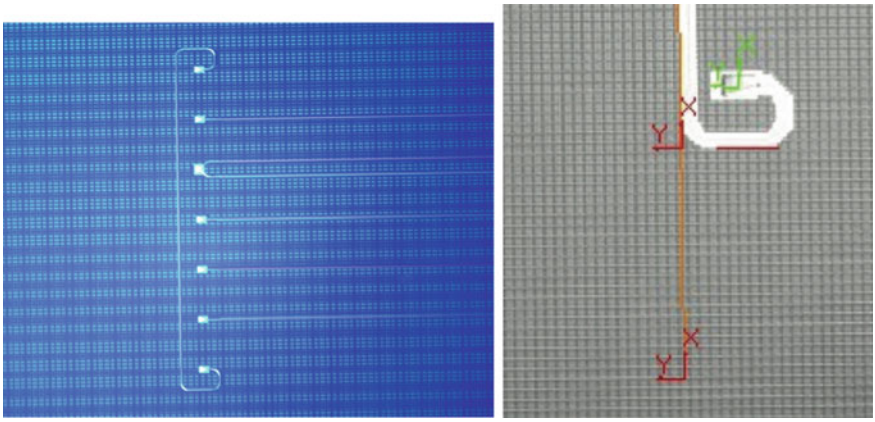

Fig. 8.8 Snapshots of the gratings during the vision-assisted pattern recognition phase. It is possible to find the grating position as well to calculate the relative angles

- Measure the relative height utilizing a force sensor integrated within the central holder.
- Detect fiber array spot to individuate the fiber position. In fact, we already calculated the grating position but we are still missing the fiber position inside the array. It has to be done now, because only now all the relative angles are corrected. To know where is the fiber, we move the array over the IR camera and we send light through the input fiber. The vision system easily detects the spot and calculates the relative position (Fig. 8.9).

After the positions are calculated it is possible to physically prealign the array over the gratings. At this point it is possible to activate the laser source and use an automatic standard peaking routine to maximize the output power using the power meter. Figure 8.10 shows the fiber array prealigned on the PIC and an example of the peaking routine.

After the relative maximum value is obtained, the polarization is optimized utilizing a polarizer. The scrambling speed is generally optimized to reduce time but still have a valuable correction. In case the values obtained are not good or out of specifications, the component can be rejected, of course, and a new loading procedure can start. On the contrary, if the alignment is inside specifications, there are generally six more main phases to consider to complete the pigtailing:

- First: memorize the best position and then take away the array to be able to apply epoxy with no risk of damaging the array itself
- Second: apply the proper quantity of epoxy in the chosen position over the grating, utilizing the robot. The robot moves over the grating position, applies the epoxy and goes back to the home position
- Third: position the array on the saved optimum position and then make another short run to optimize the output power

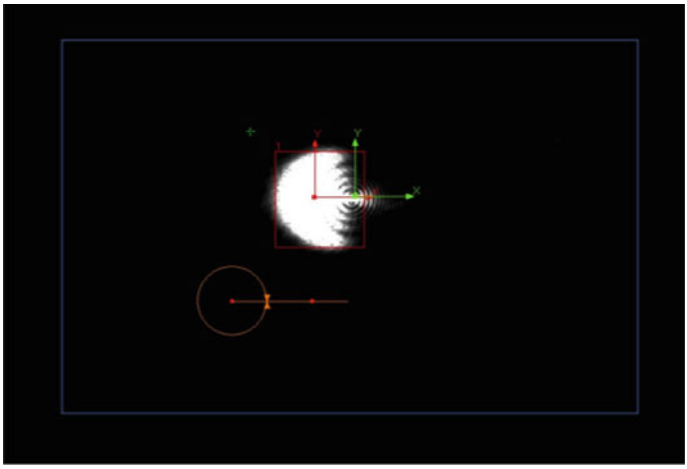

Fig. 8.9 Spot size from the array, as detected by the IR camera. In this way it is possible to calculate the exact position of the input fiber inside the fiber array

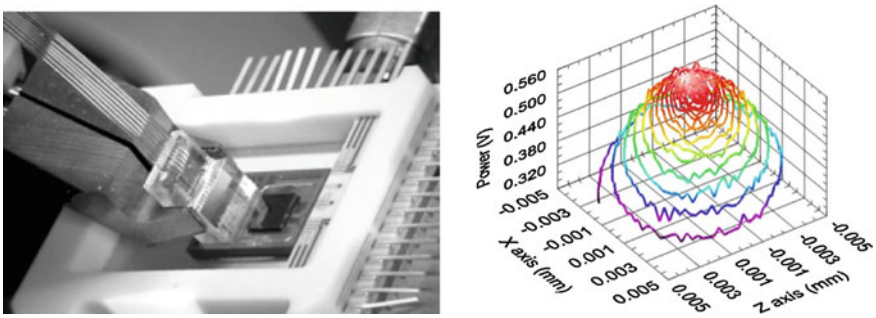

Fig. 8.10 *Left*—the fiber array prealigned to the grating inside the package is ready for the final peaking routine, *right*—an example of the peaking routine results, at the end of which the array will be positioned at the value of maximum optical power found

- Fourth: utilize the robot to bring the UV light fiber at the proper position and distance with respect to the substrate
- Fifth: run the procedure for polymerization of the UV epoxy; this procedure is process related and depends on the epoxy characteristics. In general it is not suggested to apply full UV power for a few seconds; it is better to apply UV in short pulses for a longer overall time to reduce the shrinking effect of the epoxy and to be able to automatically compensate for the eventual submicron movements due to the epoxy shrinking
- Sixth, and lastly, send the robot back to home position

All such procedures have to be done automatically in quick order. It is important to note that all these steps must be operator independent so that the overall procedure is consistent lot to lot. After releasing the fiber array from the gripper it is then possible to unload the pigtailed component and automatically pass on to the next one, and so on.

In general the excess losses obtained for a loop waveguide connecting two gratings are less than 0.5 dB. Such a value can be obtained consistently and is normally considered a good value from an industry viewpoint. Back to the question we asked at the beginning: how long does it takes to complete the entire procedure? The following table shows step-by-step some characteristic value in terms of timing (Table 8.1).

The total time for this specific process is around 13 min.

This number was obtained for a specific component and is reported as an example. It can be bettered and depends on the design, chosen epoxy, general specific routines, loading part preparation, and speed of the robot. In any case it is clear that actually, even with optimizing all the variables, it is quite reasonable to assume that the overall process cannot be much shorter than 10 min. This is a huge advance on the manual process (and it is perfectly repeatable), but it is still a bit disappointing in terms of the full speed automation that we are used to for microelectronics. This is due to the intrinsic problems related to photonic coupling: the submicron tolerances and the consequent necessity to utilize active alignment to be able to get acceptably low losses. In fact in terms of automation and process speed, it would be much better to utilize passive alignment and pigtailing, but actually it is not yet possible to do it with fiber arrays in a satisfactory way. We shall see in the next section some of the possible solutions under development to try to overcome these problems, looking to the future. To conclude this section is worthy to note that these kinds of automated benches based on imaging and sophisticated high precision stages can also be used for laser integration (the other "major problem" mentioned at the beginning). Right now the best way to integrate a laser on a PIC is the Luxtera approach [4], the so-called laser micro package shown in Fig. 8.11.

Such a silicon laser-pill can be aligned and pigtailed on the PIC using similar routines to those described above. In this case it is important to define the gripper that will have to hold the micro package and at the same time supply current using pogo pins. People are working hard to try to integrate in the same mechanical fixture an MM fiber that allows detecting the light and consequently optimizing the alignment (of course positioning a proper "monitor grating" on the PIC).

Or, alternatively, if a fiber array has been previously pigtailed, it is possible to use one of the output fibers available as monitor.

Independently from the monitoring method, it is important to highlight how the approach and procedures described above can apply to both the fiber coupling and the laser integration, using imaging for prealignment and final active alignment for losses optimization.

Finally, another important consideration related to automation is the possibility to have wafer-level pigtailing. As illustrated above, the actual automated bench does not include a wafer-level solution, especially for the fiber array pigtailing. But

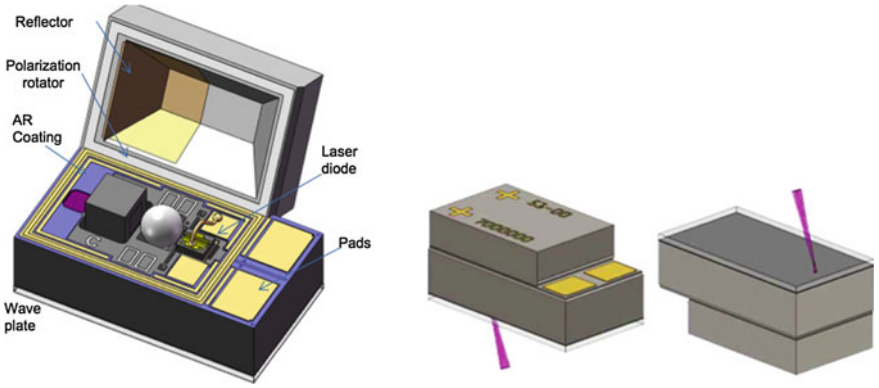

Fig. 8.11 Laser micro package as fabricated by Luxtera (2) with the laser output spot size from the bottom will be aligned actively to the grating

the possibility to operate at wafer level is under development worldwide, either upgrading the equipments based on similar pigtailing concepts or changing the technological approaches using innovative and promising technologies. The next section will survey such technologies and will include some evaluation in terms of their capacity to improve pigtailing automation and process repeatability.

8.3 Optical Fiber Interface and Laser Integration on PICs: A Survey of Innovative Concepts and Automation Considerations

The necessity to find new solutions for automation of laser and fiber pigtailing on PIC is clear. Both equipment suppliers and packaging industrial engineers are working hard on methods, processes, software, and hardware to guarantee the full exploitation at reasonably low cost and high automation for silicon photonics applications. The main concepts considered here for this survey are related to vertical coupling because, as mentioned, this is the best approach in terms of automaton. In fact it is possible to test the devices at wafer level and, as shown before, it is possible to start realizing automation for pigtailing. The two basic requirements coming nowadays from industry and the market are:

- Optical interface with fiber arrays has to be overcome in favor of pluggable solutions
- Laser integration on PIC has to be realized automatically at the wafer level

In this section, we examine the more promising answers and their impact on automation.

8.3.1 Optical Interface with External Fibers

For the optical interface with external optical fibers, the general consensus nowadays is to find a solution that can avoid the use of fiber arrays and consequently to find a pluggable solution where the fiber is plugged into the device just at the end of the entire assembly processes. This is not an easy task, because the tolerances are still small and, in general, the light has to be turned in such a way that the more familiar and industrially accepted form factor is adopted. Also, it is evident that connectors play an important role if a pluggable solution has to be achieved. In general, MPO types of connectors with ribbon fibers have been evaluated and the major proposed solution deals with interfacing the PIC device with such a kind of external connector.

8.3.1.1 Approach One

The first approach to be considered is related to the realization of a small block or ferrule that includes bended insensitive fibers inside it and fits externally with an MPO connector. An example is reported in Fig. 8.12.

The picture shows how the concept works. Substituting the familiar fiber array with the block including bended insensitive fibers allows the possibility to have a pluggable solution. The MPO connector can in fact be plugged in and unplugged after pigtailing and the top spring allows good mechanical contact. This approach is under evaluation. At first sight it does not look like there are that many advantages in terms of automation. In principle it is still necessary to have active alignment as

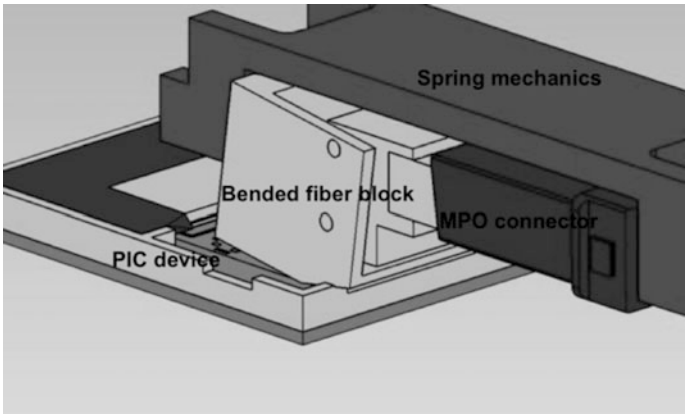

Fig. 8.12 Example of a bended fiber block over the gratings on the SOI chip. The fibers are bending insensitive and placed aligned inside the block. The picture shows that the MPO connector is pushed inside the block using a spring mechanics. Alignment holes and pins guarantee proper alignment tolerances between the MPO and the fiber block

in the fiber array approach. It is worth noting anyway that, if the losses and costs are consistent, the next step for this approach could be the positioning of markers and thus the utilization of flip chip technologies for passive alignment, including wafer-level passive alignment. This could bring it to a consistent automation. On the other side, the total thickness is still quite high and this could limit in future a wide applicability of the concept.

8.3.2 *Approach Two*

The second solution we report was developed by IBM [5, 6] and introduces the basic idea to use different coupling methods and materials (or parts) to be able to take the beam from the nanowires or the grating and be able to adapt/modify it so that in the end it is possible to have a larger beam and a more relaxed tolerance for the fiber interface.

In the present case the solution proposed was to use adiabatic coupling between lithographically defined polymeric waveguides and the silicon nanowires directly (so with no gratings). The basic concept is illustrated in Fig. 8.13.

To make the concept usable IBM completed the design and developed the technologies to be able to fulfill two major steps:

- Use silicon etching and an alignment ridge lithographically realized on the polymer, so as to guarantee the proper position accuracy for adiabatic coupling

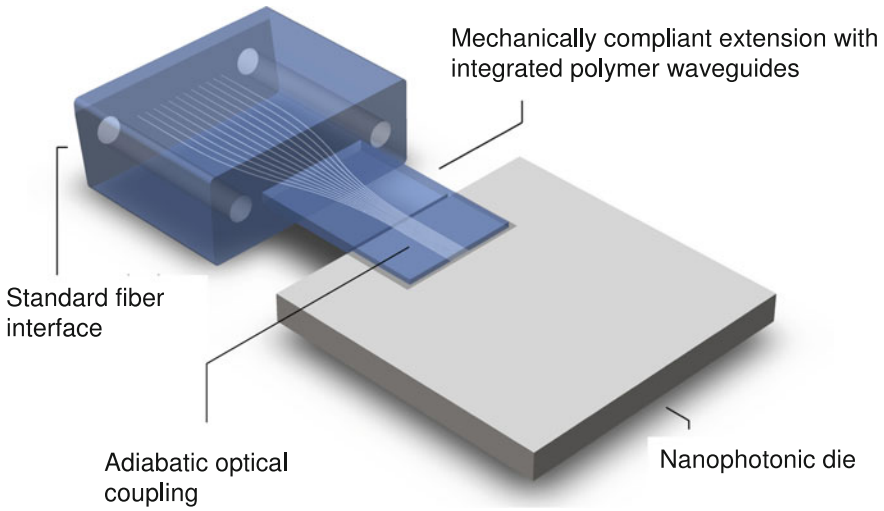

Fig. 8.13 Schematic of the IBM proposed solution. The "standard fiber interface" part fits with the standard MT/MPO connector, allowing pluggability

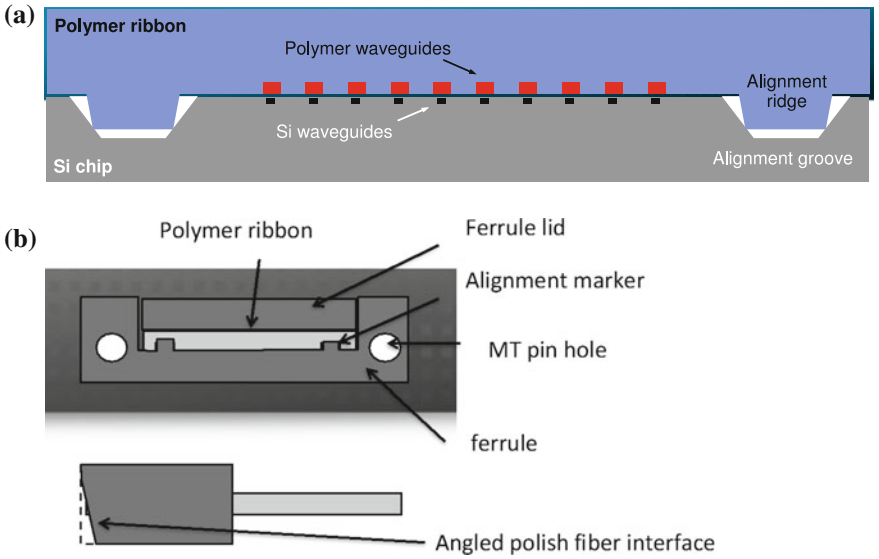

Fig. 8.14 Schematics of the two optical interfaces: **a** shows the polymer–silicon nanowires interface where the adiabatic coupling is obtained thanks to the relative position accuracy guaranteed by the alignment grooves and ridges, **b** shows the "ferrule" that will interface with the MT/MPO connector. Again the polymer ribbon waveguide is aligned using markers and the precisely defined MT pinholes

- Realize a ferrule, with the proper alignment marks, on the output side able to accept pluggable MPO connectors

In Fig. 8.14 the two mentioned steps are shown schematically. In fact not only the coupling between Si chip and Polymer ribbon is based on precise alignment features, but also the ferrule as shown in Fig. 8.14b.

IBM claims that such alignments can be passive because the alignment accuracy due to the two structures is:

- ±0.5 μ for ribbon to silicon
- ±1.5 μ for ribbon to ferrule

Given the tolerances above, it was claimed that a total loss between 1–3 dB was measured from the nanowire output to the external fiber along the optical path (nanowire-polymer waveguide-connector-fiber).

Let us consider this approach from an automation point of view, also comparing it with approach one described above. It is clear that the main advantage of approach two compared to approach one is the possibility to realize structures that are self-aligning with high precision, allowing passive alignment.

So, in principle, it is possible to utilize an advanced flip chip equipment properly equipped with fixtures and tooling able to hold the entire part and to passively align it to the chip. However, this approach does not look feasible for wafer-scale

pigtailing, so that it has to be imagined a "one by one" assembly process, as in the previous case. So, even if passive alignment is a big plus and the use of existing advanced machines is ideal in terms of future production, the difficulty to scale to wafer-level pigtailing (and optical testing as well) could limit the complete future exploitation of this solution for mass production. Finally it is worth noting that from a package perspective, the ferrule will have to be anchored to a package base to reduce stresses and strains, exactly as in the previous case.

8.3.2.1 Approach Three

The third approach worth consideration was introduced by INTEL [7] and gives us another view on how to adapt the parts to be able to simplify pigtailing of PIC. The concept is illustrated in the following isometric views (Fig. 8.15).

At a first sight we can recognize the approach number one described before. The connector body in fact contains bended fibers (bending insensitive) and is designed to accept the MT connector. The fundamental change is mainly in the production and use of the two microlens arrays depicted in Fig. 8.15b. In fact the purpose of such arrays is to collimate (and then focus again) the beam so that it is possible to have reduced tolerances between the connector body (generally called HiDOC90

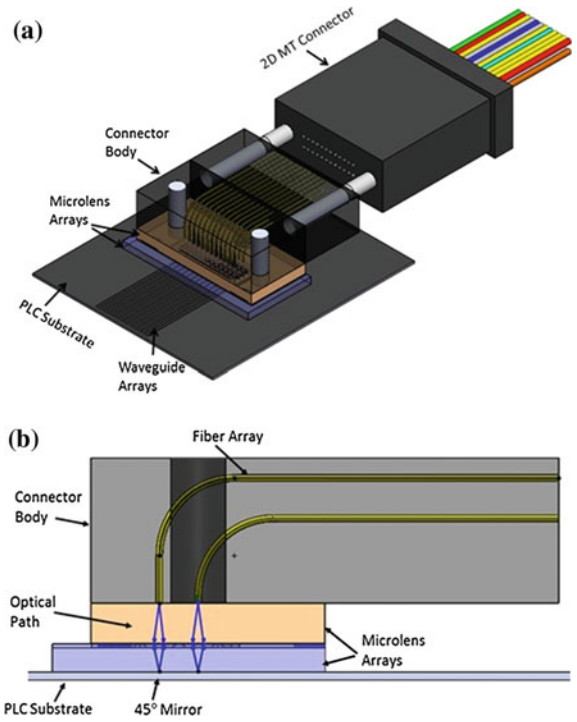

Fig. 8.15 Schematic of the concept proposed by INTEL, **a** top side and **b** lateral side

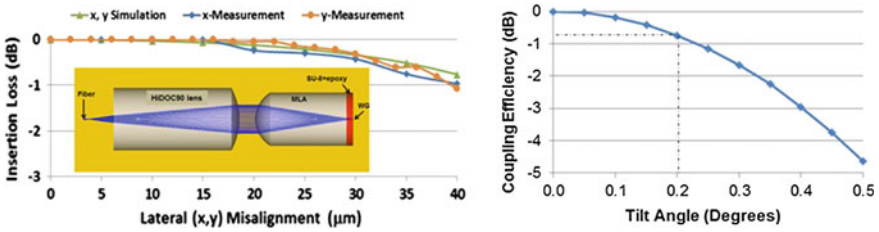

Fig. 8.16 *Left*—comparison of simulation and measurement by INTEL for lateral misalignment of HiDOC90 and PLC module, *right*—impact of the tilt between HiDOC90 and PLC substrate on insertion loss

"high density optical connector with 90 turn") and the PLC substrate, especially in the lateral (x, y) directions.

Examples of the tolerances for such couples of lens arrays are reported in the following Fig. 8.16:

It is clear that advantages can be achieved in terms of tolerances between the two lenses (1 dB inside 40 µ misalignment). Angle tilting has to be carefully controlled, but still it is inside reasonable values in terms of automatic control. Now, what can be said in terms of automation? It is probable that this approach prove to be better than approach one and the main reason is related to the possibility, in the future, to avoid active alignment, or, alternatively, to have active alignment using less expensive equipment and a quicker process time (due to reduced tolerances). In any case, as shown in the previous paragraph, long fibers do not fit well with automation and consequently passive alignment of similar a structure would be the perfect choice as well as wafer-level subassembly.

This approach could really be of great impact if the technologies behind the concept will overcome the necessity to use active alignment (and consequently long monitoring fibers). In fact lens arrays can be integrated at the wafer level and the connector body can be flip chipped using markers at the wafer level as well, increasing process speed and automation level.

8.3.2.2 Approach Four

The final mention goes to a technology that has growth during the last years and nowadays looks very promising for the subject we are discussing: the two-photon absorption laser lithography technology (TPA) [8–11]. Such technology provides the possibility of writing arbitrarily complex structures in three dimensions in polymer or hybrid polymer materials. In this specific optical field, materials that are normally considered are the inorganic–organic hybrid polymers such as ORMOCER or ORMOCOMP.

Based on the possibility to "write" inside the polymer that has been previously deposited on the PIC and to collect light from the gratings, it looks very interesting to evaluate if it is possible to use the same technology to simplify the pigtailing

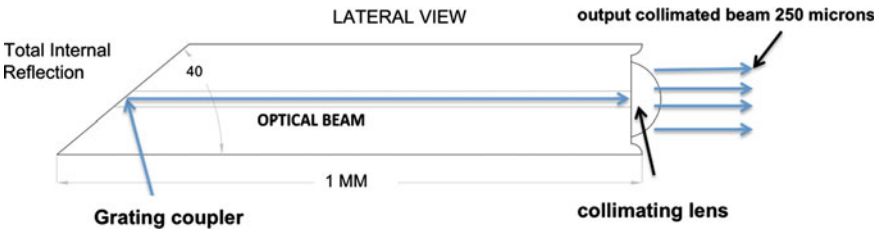

Fig. 8.17 Schematic of the concept to rotate the light and then to collimate it "writing" inside the polymer using TPA laser lithography

phase and consequently allow automatic processes. At the moment it is possible to realize lenses directly on the PIC (as mentioned for approach three), but more intriguing is to push the technology to evaluate if it is possible to turn and collimate the light at the same moment using the same basic structure, writing inside the polymer. An example of the concept is shown below in Fig. 8.17:

The ability to write or realize such structure (in single form or array) could allow having an edge emitting PIC to be pigtailed with the simplifications of the relaxed tolerances due to the collimated beams. And in principle it could also be realized at the wafer level. Clearly, the PIC still needs to be aligned and pigtailed to the external world and this can be done in many different ways and for different packaging approaches.

A couple of conceptual examples are given that shows the possible advantages of such an approach.

The first example shows in Fig. 8.18 how it is possible to apply the concept at the package level.

The PIC, as explained above, thanks to the custom-developed TPA technology, has an array of collimated beams coming from the edge and the MPO adaptor recollects such beams. The MPO adaptor will also have integrated lenses that will focus the beams inside the fibers. The concept inherently allows pluggable solutions and the overall mechanical stability of the system is granted by the package structure itself.

Nowadays, connector producers are working on the adaptor side as well [12], which is not an easy task. An example of what is currently under development is reported in Fig. 8.19 that shows the lenses embedded in the resins with the due precision and tolerances to focus the collimated beams into the external fibers.

If the technologies, in both areas, can be improved and confirm their feasibility at an industrial level, the beauty of the concept is quite evident. The tolerances are relaxed thanks to the collimation and the assembly alignment between PIC and the adaptor can be made quickly, actively, or even passively, with the proper package design and tolerances bringing it to real automation industrial processes. And of course it is a pluggable solution that is a must for such applications.

Another example of applicability, shown below (Fig 8.20), is for the case of "on board" assembly of a PIC.

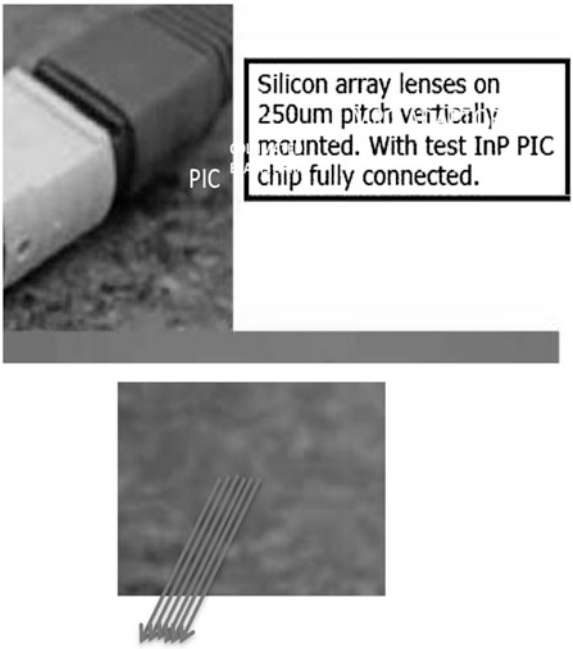

Fig. 8.18 An example of possible final pluggable packaged device. The beams coming from the PIC's gratings are rotated and collimated so that the exit from the PIC is horizontal and the interface with the MPO adapter simplified. The *arrows* on the *right* picture indicate the final output to be collected by the MT connector

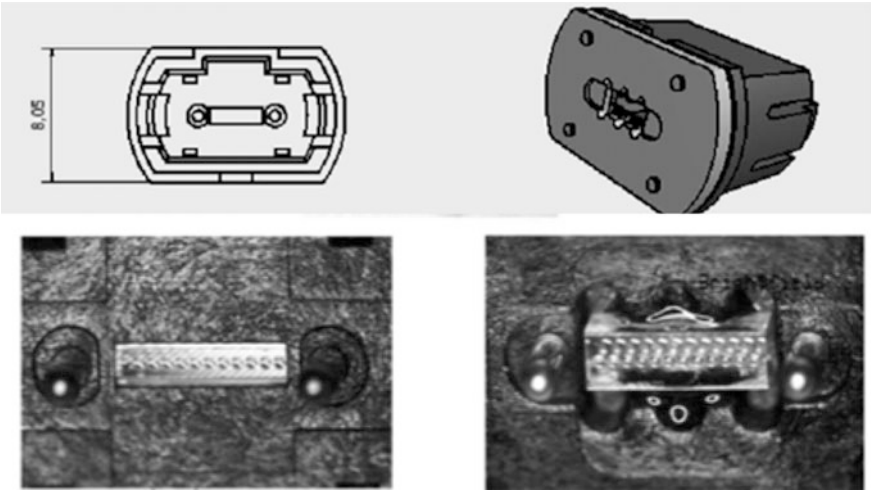

Fig. 8.19 An example of an MPO adaptor with the lens array embedded in the material and aligned respect to the pins for further self-centering to the connector

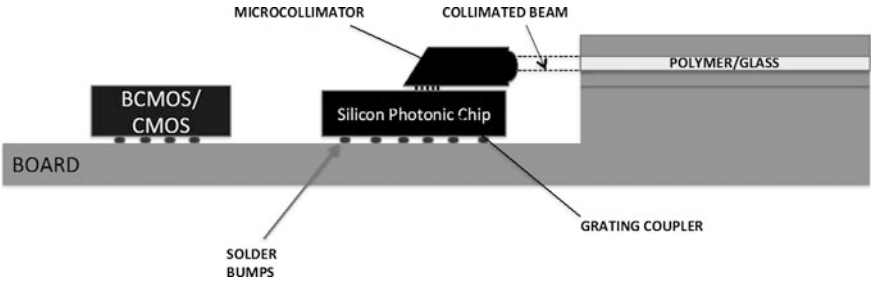

Fig. 8.20 Example of the applicability of the micro structured collimator using the TPA technology. In principle, any combination is possible, interfacing the PIC device directly on the board that can as well have polymer waveguides on it for interboard optical interconnections

In this case the PIC is flip chipped on the solder bumps and can precisely be aligned to the output. Many combinations can be thought of in such cases and the interesting thing is the possibility to have passive alignment using standard industrial flip chip equipment with lower accuracy. As such, depending on the real application, this approach can be widely used and adapted and allows a sure automation especially when it is possible to have passive flip chip attachment. Actually, the TPA technology for this specific use is under development and still has to be proved in terms of losses and performances. By design it is possible to expect around 1 dB of excess losses due to the structure, but so far the technology is not yet ready. It will also be necessary to show the scalability for wafer-level integration and test the thermal behavior of the structure at relatively high temperatures.

8.3.3 Laser Integration on PICs

As mentioned previously, laser integration on PIC is the other main problem in terms of silicon photonic packaging. It is worthy to conclude this chapter with a brief survey on the current situation. Actually, the previously mentioned laser pill developed by Luxtera is in our opinion the best solution and a lot of work has been done toward trying to speed up and automatize the alignment and pigtailing of such a structure. The main bottleneck for full automation of this subassembly is the necessity to have active alignment, but it has to be said that equipment suppliers are working a lot to reduce the cycle time.

A very interesting solution includes the use of a high power external laser source to melt the solder in few seconds and the use of special mechanical fixtures to hold the laser pill and at the same time supply current to the chip. In general such machines use standard vision to recognize the grating position and then integrated piezo stages to quickly actively align the chip. In terms of the mechanical fixture, the main difference with respect to what was shown in the previous paragraphs

stands in the absolute necessity to avoid the use of fiber arrays (as is normally done). For such advanced fixtures, to be able to read the optical power and to optimize it, it will obviously be necessary to have some integrated monitoring (for example, a large core fiber, placed on the same mechanical fixture at a fixed distance) and a proper PIC design to allow such monitoring (for example, a grating coupler placed at the same fixed distance of the same large core fiber). Nowadays, state-of-the-art mechanics combined with advanced high-speed flip chip equipment and improved process technologies allow the mounting of lasers on PIC at wafer level with a very low cycle time (tenths of seconds for each laser) and a very low thermal impact as the laser external source can heat locally without affecting previous attachments. As such, the laser integration automation can be attained at the industrial production level.

Of course, other approaches are investigated, like direct placement of the laser chip on the grating (or on a turned mirrored tapered waveguide). The only way to make possible such "direct" approach is to have a special laser diode chip that can directly turn the light and ready to be soldered on the coupling structure of the PIC. An example is the so-called LISEL (lens integrated surface emitting laser) chip from Oclaro/Hitachi [13], or in general similar approaches (like the one from the PETRA consortium in Japan), where the laser beam is adapted and turned to match as much as possible with the grating coupler. Figure 8.21 shows the concept.

Of course from the automation point of view, this approach is of great interest because of the relaxed tolerances that could allow passive alignment and soldering (with standard evaporated gold/tin solder) of the laser chip (or laser array) directly using flip chip industrial equipment. In any case this approach, in principle, does not provide hermeticity and it keeps open the burn-in issues, to be properly evaluated in the case of real production and automation. Much better in this case would be to use similar diode components previously placed on SiOB substrates to allow testing and burn-in outside the PIC before any subsequent attachment on the PIC.

Variations from the Luxtera approach are well studied and in particular it is interesting to mention the possible use of the TPA technology reported above. As a matter of fact the writing from the laser edge to the grating, for example, could be

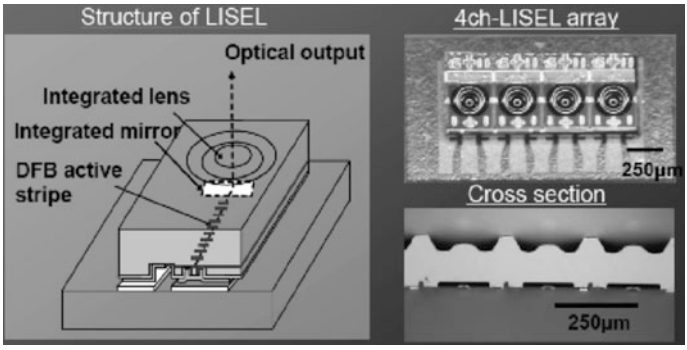

Fig. 8.21 Structure of the LISEL laser proposed by Oclaro

possible and also can be made at the wafer level. Actually, such developments can be even more practical and interesting using TPA in combination with SiOB (silicon optical bench) technologies, to save the possibility of external burn-in of the lasers before integration on PIC. In other words, for laser integration, nowadays the best way to proceed in terms of automation and reliability looks to be to optimize or develop technologies that can guarantee an external realization of a laser on SiOB (including test and burn-in) and an automated active alignment of the same on the PIC using the new available flip chip technologies and equipment.

8.4 Conclusions

Silicon photonics packaging is facing a crucial moment: the necessity to go from R&D and low/medium volume production to high volume production. It means to deal with automation and repeatability for high-scale manufacturing. As a consequence, both in terms of technologies and equipment the development effort is nowadays very high at all the levels of the packaging supply chain. As we illustrated, both pluggable optical interfaces and laser diode array integration, the two main bottlenecks to high volume production, are heavily under development and scrutiny. As a matter of fact various approaches are currently under development and engineering by major industries and institutions. In this chapter we illustrated the more promising ones, not excluding that variations on the same concepts or combinations between them can bring about the winning solution in terms of high volume manufacturing and reliability. It is clear in any case that any real solution will need to have more relaxed tolerances, automated processes that are operator independent, eliminated or simplified (reduced) fiber presence for monitoring reasons, passive alignment or, if active, quick overall cycle time. As shown in Sect. 8.2, remaining with a classical methodology brings limitations even if a dedicated automated bench is designed: reducing cycle time under a certain threshold is impossible with such an approach. To really be able to break the barriers and be effective for high volume production it is mandatory to continue improving innovative packaging technologies, materials and design, as illustrated above, as well pushing equipment upgrades, with special emphasis on flip chip machines and optimized benches supported by vision technology and robotics.

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Chapter 9
CMOS Cost–Volume Paradigm and Silicon Photonics Production

Amit Khanna, Dieter Bode, Carl Das, Philippe Absil and Steve Beckers

Abstract A clear fabless path to silicon photonics R&D and low volume production is taking shape. Current low volume requirements in silicon photonics pose a price challenge for products. Further, technical challenges for low volume production also need to be addressed. In this chapter we discuss the rapidly evolving macro-landscape in datacom traffic and its impact on silicon photonics, other applications domains and their volume requirements, and stages in low volume production with their associated challenges.

9.1 Introduction

In this chapter technological and economic aspects of translating silicon photonics into low volume production are discussed. In the late twentieth century as demand for electronics grew, industry developed megafabs. These megafabs, which require massive investments, revolutionized the electronic industry. Large volume applications justify the investment and allow the megafab to recover the high cost of process developments, operations, and maintenance [1]. Generations of advancements in ecosystem and know-how produced advancing complementary metal oxide semiconductor (CMOS) nodes. This led to improvement in existing products and possibilities for new ones, such as smart phones, tablets, cameras, etc. All these products have enormous device density on chip and high volume consumer markets. However, IC manufacturing has its roots in a preceding era of smaller volumes and a gradually maturing ecosystem. The IC ecosystem comprises not only the fab, but also CAD tools, design houses, IP vendors, design aggregators, brokers, packaging, and testing providers. Incremental technology evolution, from low/medium volume

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to high volume, had its benefits. This allowed the IC ecosystem to mature, based on increasing market interest, to its current advanced state. Today, this ecosystem allows fabless companies to design complex integrated circuits without the need to have their own fab and process know-how.

Currently silicon photonics' primary applications are datacom and telecom. In datacom, silicon photonics competes with copper-based or VCSEL-based interconnects, which are sufficient for below 100 m interconnect lengths in present generation data farms. While in telecom, silicon photonics competes with InP/$LiNbO_3$ technologies which are either mature ($LiNbO_3$) or not CMOS fab dependent (InP). These technologies pose a technology as well as economic challenge to silicon photonics. In particular, the economic challenge restricts low volume of silicon photonics to meet megafab expense with appropriate pricing. In a larger context, due to the inability to reach viability in low volume production most *more-than-Moore*[1] technologies face a tremendous hurdle between proof-of-concept in CMOS R&D lines, to product on the market. This hurdle impedes ecosystem maturity, is a barrier to market acceptability and has a stifling effect on innovation and ecosystem maturity. Therefore, one of the key challenges facing silicon photonics today is the access to low volume manufacturing. The need for a low volume IC business model is relevant for the present and future of the semiconductor industry itself. Use of electronics is growing rapidly in new sectors such as automotive, aerospace, healthcare, Internet of things (IoT), etc. These markets are fragmented, and typically require shorter product lifecycles, greater product functionality, and in many cases, low to medium volume manufacturing. Thus, the low volume on megafab viability challenge that silicon photonics poses, is also pertinent for electronics industry at large.

In the second section we distinguish the different kinds of low volume production, differentiating between them in terms of price, volume, and process flexibility. In the third section, 'Markets and volumes', we explore the different application domains in silicon photonics and their volume demands. Where possible, we also discuss a timeline for their market adoption. Further, we analyze where these volumes fit on the megafab landscape. A possible route to high volume manufacturing for silicon photonics is envisioned. The requirements of silicon photonics devices are unique and pose a new set of technical problems to the CMOS manufacturing ecosystem. In the fourth section, we discuss the different stages in low volume silicon photonics manufacturing. The aim is to familiarize the users with these stages, their challenges, and present them in a chronological sequence.

[1]By definition, *more-than-Moore* technologies benefit from the advancements of the semiconductor megafab, but do not necessarily benefit from scaling of the nodes (*more-of-Moore*). Therefore, after a certain optimum node, the technological benefits do not outweigh the high process cost related with a further advanced node.

9.2 Low Volume Production

In this section we describe the different methodologies for low volume access. They vary in price, process flexibility, typical volume, and timing constraints.

9.2.1 Multi-project Wafers or MPWs for Affordable Prototyping

Multi-project wafers, or MPWs, offer affordable prototyping of IC products in new IC technology for small volume users. This scheme[2] allows users to share mask, processing, and engineering costs. Each user contributes a fraction of the design area, for a fraction of the full run price. MPWs are effective to provide fabless companies, start-ups, and SMEs an opportunity to test new products based on a standard process. All participating users follow the same process, therefore, there is a compromise between process flexibility and access price. The MPW access provider takes necessary steps to ensure the confidentiality of submitted designs (Fig. 9.1).

Due to the low volume nature of the service, megafabs offer MPWs to their direct large customers for prototyping and market sampling. However, such megafabs collaborate with access brokers to introduce the technology through MPW to small volume users. Such open-access supports the emergence of a fabless ecosystem from design to packaging. This ensures that each part of the supply chain begins to gain the necessary expertise. Diversity of the MPW projects also provides valuable experience to the ecosystem to address future product requirements.

Although the overall access price is low in MPWs, the price per chip is not as low as high volume production. Process options are kept to a minimum to maximize cost-sharing. Typical volume for MPW access varies from 1 to 20 wafers per project. Such runs are scheduled periodically and announced by the access brokers in the beginning of the year (Fig. 9.2). Today, megafabs do not offer MPW in silicon photonics technologies, but different CMOS pilot lines provide access to silicon photonics MPW.[3] It is noteworthy how MPW access continues to play a critical role in catalyzing the field of silicon photonics through open-access [6, 7].

[2]Started by MOSIS in the USA and Europractice in Europe.

[3]IMEC (Belgium), CEA-LETI (France), IHP (Germany), VTT (Finland), and IME (Singapore) [2–5].

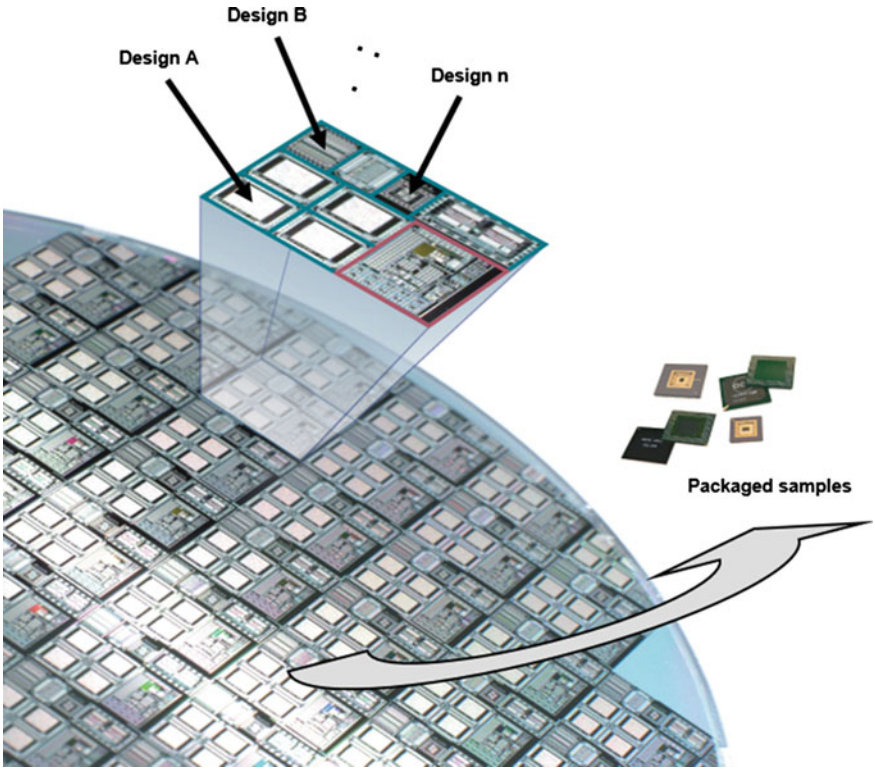

Fig. 9.1 In MPW the mask area is shared with other users. Each die is further sub-diced to deliver to the users chips with only their designed areas

9.2.2 Commercial R&D Project

Commercial R&D projects are used to run R&D lots for testing custom processes, or fine-tuning the MPW process for specific products. Such lots can also include process development. The goal of such R&D projects is to run various experiments to identify the ideal process conditions for the product. The cost of such an R&D lot is typically 10× the cost of MPW access. These projects allow a much larger design area than MPW, process flexibility, and options to add more process modules.

For applications such as datacom and telecom, silicon photonics is similar to electronics in terms of photonics library reuse. However, for applications such as sensing and healthcare, silicon photonics is closer to 'one process–one product' philosophy, similar to MEMS. It is likely that for telecom and datacom applications, commercial R&D lots are useful in the near future, but not in the long term. Whereas for healthcare and sensing applications, the commercial R&D projects may remain a critical step in product development. The typical access volume due to the R&D nature of the lot does not exceed 100 wafers. The turn-around time for

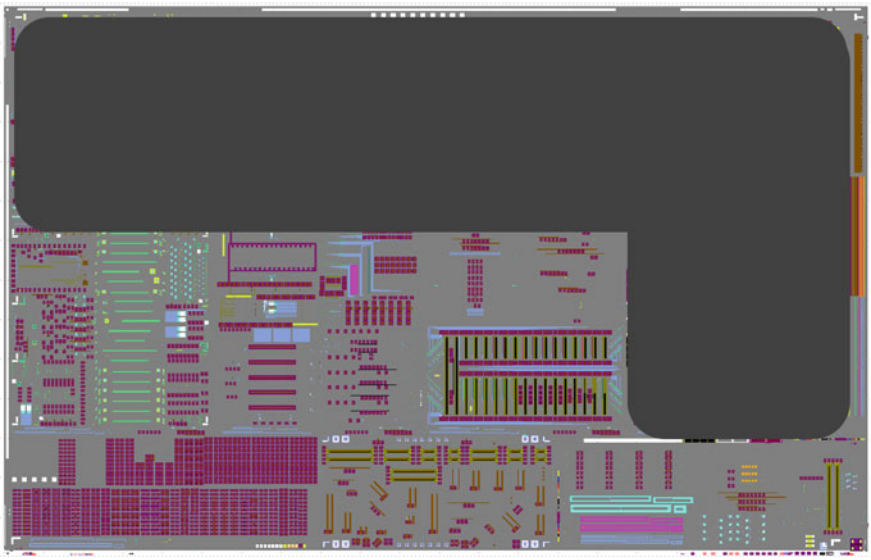

Fig. 9.2 Layout of an MPW mask for silicon photonics (*Courtesy* of IMEC)

such lots is longer than the MPW runs as the processes may be less mature and periodic testing, inspections, and redo may be required. Due to the high investment required, such projects are typically used by research groups from larger industries. This requires a customized process design kit (PDK) supplied to the company with agreed design rules and design layers. Such R&D projects are not implemented in megafabs, which focus on production capabilities, but in CMOS pilot lines. Furthermore, CMOS pilot lines and their volume translation partner agreements are known in silicon photonics [8, 9].

9.2.3 Corner Lot

Corner lots are a critical pre-production validation step. As the name suggests, corner lots run the process at process extremities within the process window. Functional performance of the resulting devices provides a worst-case estimate. If the devices are within targeted functional specifications, then the lot can be forwarded for production. If the functional specifications fail, then the yield of the lot can be compromised. As a result, the process and/or the design may have to be adjusted with an R&D lot (above). In principle, a device that does not 'yield' in the process corners is defined as not manufacturable. To the best of our knowledge, corner lots are currently not executed in silicon photonics. This remains one of the technical challenges of moving into production. To overcome this challenge, digital electronics like standardized device libraries, with elaborate device models tied to

process variations, have to be built. These process tied device models enable the fab to identify the process corners, and when provided in the PDK, allow users to simulate process corners for their designs.

As new process development is not needed, the cost of a corner lot is typically higher than an MPW access but lower than a commercial R&D lot. The process is fixed with only minor modifications to force process extremities.

9.2.4 Low Volume Production Lot

A successful corner lot experiment translates into a device that can proceed for production. The knowledge of the corner lot is pivotal to define the ideal process conditions for production. Once in production, automated inline measurements and inspections are sufficient to indicate whether the process is progressing as expected. Usually, batches of 50–100 wafers are launched and periodically checked for specifications. The price of access can be volume dependent, but, per chip this price is much lower than MPW, commercial R&D projects, and corner lots. As the process is well understood at this stage, there is no process flexibility. Typical volumes for the low volume regime range from 100 to 10,000 wafers/year. Such lots have a fast turn-around time, as minimal or no manual interventions may be required. If this is not the case initially, it is endeavored to attain such a level of maturity during production. As production continues, the yield and the turn-around time can be further optimized.

9.3 Markets and Volumes

In this section we analyze the expected volume requirements for the datacom, telecom, and sensor industry.

9.3.1 Datacom

The approximate number of servers deployed in giant data centers in 2013 was 3–4 M at approximately 30–40 large data centers globally [10]. This gives an estimate of about 100,000–150,000 average number of servers per data farm. The typical size of the racks is 50 cm wide (19 in.). Each rack can house about 30 servers. Therefore, there are about 4000 racks per data farm. Assuming a square grid to populate these racks, and one rack separation between the individual rows and columns for air flow, a 60 × 60 rack configuration will require a total size of 60 m × 60 m. For these distances, VCSEL technology is mature, cost efficient, and

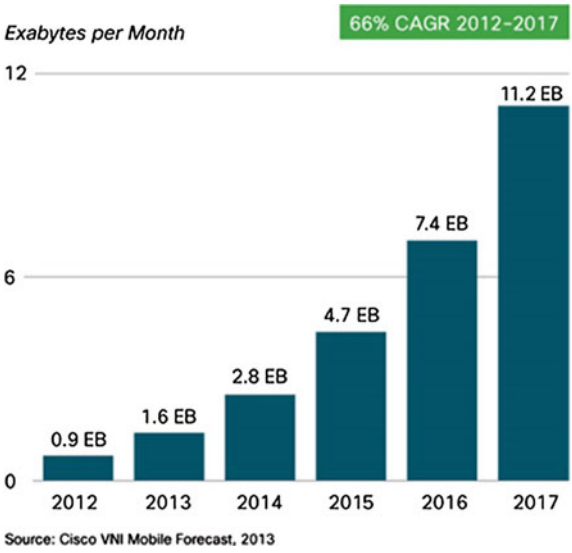

Fig. 9.3 Cisco's forecast on growing mobile traffic up to 2017

capable to meet a 10 Gb/s interconnect requirement [11]. Some results show speeds reaching 25 Gb/s. These high speed optical interconnects comprise:

- transmitter chip, for electro-optic transduction, optical modulation, optical signal multiplexing, etc.,
- fiber optic bundle, carrying the modulated and multiplexed optical signals, and
- receiver chip, for demultiplexing and opto-electronic transduction.

These interconnects are called active optical cables, or AOCs.

A mobile data traffic forecast by Cisco is given in Fig. 9.3. The forecast shows that, since 2012 mobile data traffic has grown by 2.5× every 2 years. In the future, increasing Internet penetration in developing economies, a growing number of interconnected devices (IoT), and further dependence on the cloud for computing and storage, is foreseen. It is reasonable to estimate a similar scale of growth in the number of servers per data center (2.5× every 2 years). Based on this estimate, compared to 2013, by 2017 the number of racks per data center is expected to increase by $\sim$5× (20,000 racks), and by 2021 $\sim$30× (120,000 racks). By 2021, each data center may require high speed connectivity between 3,600,000 servers, housed on 120,000 racks, with inter-rack distances at a 100s of meters. At such distances, VCSEL technology may be stretched to deliver 25 Gbits/s data rates [11]. Initially, silicon photonics may serve the rack-to-rack interconnects for large data centers, while VCSELs may continue to be deployed for server-to-server interconnections. By 2021, it is quite safe to assume silicon photonics AOCs with a large distance-bandwidth product, to be deployed in the data farm architecture in proportion to racks. For 50 large data farms each with 120,000 racks a demand for 6 M AOCs can be foreseen. Furthermore, 6 M AOCs translate to 12 M silicon photonics components. Beyond 2021, as the data rate requirement grows, it is

conceivable that a majority of all the AOCs within a data farm may be silicon photonics based. For enterprise datacenters, the inter-rack distance may not be critical for silicon photonics deployment. Based on bandwidth (such as >50G links), high speed silicon photonics AOCs may also be required for the enterprise or consumer data center market in the future.

9.3.2 Telecom

For telecom, silicon photonics can enhance the spectral efficiency of modulation, avoid the need for complex base stations, etc. [12, 13]. Compared to datacom the component volume requirement in telecom is typically 1000× smaller [14]. Such a low volume is prohibitive for any commercial fab to adopt a silicon photonics process for production. However, it is conceivable that, if a silicon photonics process is maintained at a commercial fab due to the datacom market, use of silicon photonics for telecom may resurge.

9.3.3 Sensors

Silicon photonics is the use of a CMOS fab to build photonic circuits, and is therefore often called CMOS photonics. This definition becomes important when analyzing the silicon photonics sensor applications. Already, there are companies that are using silicon-based medical diagnostic chips [15]. One of the most promising materials, because of its material transparency to visible light, is silicon nitride. Being a CMOS fab material, silicon nitride can also benefit from all the advantages of CMOS processing. The key features of a CMOS fab, to produce highly uniform and extremely large volume products, with reproducibility and reducing cost per chip, have the potential to revolutionize the healthcare industry where such high diagnostic tool quality is desirable. Applications requiring disposable point of care patient diagnostic chips, which can be sold off-the-shelf, can change the way we view the healthcare industry. Other promising sensor industries include structural health monitoring, chemical and gas sensors, etc. A mature ecosystem, from CAD tools to packaging, can attract interest from start-ups and fabless companies, which can benefit from the developments driven by larger volume applications to create innovative products for new high volume application domains. It is nevertheless difficult to predict today the volumes that may be required for sensing applications.

9.3.4 Volume Evolution

It is pertinent to ask, what is large and low volume production in CMOS? As an example in terms of devices, in 2014 the total sales of laptops, PCs, smart phones, and tablets exceeded 1.5B devices. In terms of wafers, it is estimated that the top ten largest semiconductor manufacturing facilities in the world produced ~25 M 12″ wafer equivalents in 2014. The low volume regime is not so well demarcated in terms of wafer quantity alone. Different fabrication facilities have different business models to attract small customers. The most often used approach of megafabs is of that of aggregation. Aggregators like IMEC, Fraunhofer, MOSIS, etc., collect the user designs on shared masks (MPW). These users can be catered for by aggregators up to an agreed volume with the megafab. This agreed limit depends upon the opportunity size. For example, up to 10,000 wafers of 0.18 μm technology or 1000 wafers of 28 nm technology may be defined as the threshold for transfer of a user from the aggregator to the megafab. While the price of 0.18 μm and 28 nm technologies is well known, it is not for silicon photonics technology today.

The silicon photonics datacom market estimate of 12 M devices a year for AOCs by 2021, translates into 25,000 12″ wafer equivalents per year (assuming 1000 chips per wafer, and, yield of 50 %). Clearly, the cumulative demand forecast for silicon photonics AOCs by 2021 does not correspond to large volume. However, depending on the price, this may be low to medium volume. This silicon photonics volume requirement may be served by industrial players such as Intel, IBM, Freescale, and ST Microelectronics, which are investing in silicon photonics processes to serve the datacom market today. This may be the 'tipping point' for silicon photonics volume expansion. A successful ecosystem serving the datacom market by 2021 can become the basis for accelerated development cycles for telecom and sensor applications. Thus, it is possible that through new application areas such as disposable bio-chips, sensors, etc., by 2025 silicon photonics will begin to achieve scales of 250 K wafers per year. It is also possible that the silicon photonics industry moves toward the MEMS way—not running silicon photonics in a large megafab, but in a smaller fab, which can be flexible to adapt its business model to match the silicon photonics industry requirements. A dedicated fab for silicon photonics, however, is yet to be seen.

One of the first motivations to pursue silicon photonics production was on-chip interconnects, to overcome the limitation of copper interconnects on a CMOS chip. By 2025, it is likely that the developments of silicon photonics through datacom, sensors, and telecom will create conditions (through ecosystem maturity) for photonics on the electronic chip, and address that initial motivation. At such a stage, silicon photonics may be a residing process module in megafabs for high-end electronic chips.

9.4 From Prototype to Volume Production: Technical Stages and Challenges

In this section we discuss the technical challenges at different stages of production for a CMOS photonics product.

9.4.1 PDK and Design Flow

A silicon photonics project typically starts with making a choice of the fabrication facility where a commercial R&D project or MPW is to be pursued. Each fab has its own specific PDK. A PDK contains all necessary information about the process, as well as a library of standard tested components. Various design rules are also prescribed, which are necessary to be followed to submit a fab-compliant GDSII file for fabrication. This process is described in the chapter on "Silicon Photonics design flow." A design team usually consists of a few engineers and designers, depending on the complexity of the submission. The design effort can also be outsourced to a photonics design house, to support design work, or completely implement the design, or develop custom components. Once the design is complete, the designs are submitted to the fab for a design rule check (DRC). If the design qualifies following DRC, it proceeds for tape-out. If not, it is returned to the user for compliance with the fab's design rules. Further, almost 50–70 % of user designs in MPW submissions comprise custom components. Use of custom components may require multiple tape-outs to identify the ideal design. This directly impacts a fabless users' R&D effort in terms of time and cost.

PDK development and maintenance are also a challenge due to a diversity of user interests. From more telecom and datacom applications to sensor applications, communication applications typically require more library elements and device models to reliably predict the circuit and system behavior. Whereas for sensors the PDK should enable custom designs on target with minimal tape-out iterations. As described above, the lack of corner simulation capability is also a challenge for moving into production.

9.4.2 New Tape-Out (NTO)

Each fresh design submission to the fab is followed by a new tape-out (NTO). NTO consists of various steps that ensure a successful photonic tape-out. This includes floor planning, IP block replacement, verification, addition of various test sites, following mask-shop guidelines for reticle preparation, mask shop communication, etc.

9.4.2.1 Floor Planning

For MPW, floor planning is a complex process where user's designs are arranged and merged to share mask space, while meeting all users' requirements (process options, number of chips, etc.) from as few wafers as possible. Preparatory work for this stage can start prior to completion of users' design (payload) submissions. If the payload is small, it is also possible to tape-out a multi-layer-mask (MLM). This has the advantage of reducing the total number of reticle plates required and printing more dies per wafer. A larger or full sized reticle limits the number of dies per wafer, but allows more design experiments, or enables more users to participate in an MPW run. For commercial R&D projects, corner lots, or production lots, the payload is dedicated to a single user and therefore floor planning can be simpler.

9.4.2.2 Test Sites: Process Control and Functional Test

User designs are merged with various other structures related to processing and qualification. Processing related structures include:

- various interlayer alignment structures, such as verniers, crosses, etc.,
- inline process monitoring test sites, e.g., to determine the etched or deposited layer thicknesses,
- cross-section sites,
- critical dimension (CD) measurements sites,
- ellipsometry sites for refractive index,
- dicing lanes, guard rings, etc.

The functional test-site includes electrical test sites, such as Kelvin or Van Der Pauw structures, via chains, forks, meanders, etc. An electro-optical test site (modulators, photodiodes) and an optical test site (passive components) for testing the electro-optical library, or other qualification criteria agreed with the user, may also be included. Test sites in CMOS photonics can consume large portions of the mask due to the large sizes of some components such as a travelling wave Mach-Zehnder modulator.

9.4.2.3 IP Blocks

IP blocks or black-box designs can be provided to users by design houses or fabs. These blocks provide users with a known functional behavior. The provider may restrict visibility of the component for IP reasons; these are known as black-box IP. The mask tape-out team replaces the black-box IP blocks with full hierarchy GDSII designs. This stage may be executed by the fab in the case of black-box library elements, or by the design aggregator when replacing IP blocks from design houses. Today, silicon photonics design or IP houses are few and usually provide

non fab-qualified components. In the future, design houses and IP vendors will have to work closely with the foundries to provide tested libraries with application-specific functionality.

9.4.2.4 Manufacturing Rule Check

After the mask is merged each individual reticle layer is extracted, and appropriate boolean operations are done to obtain the final reticle in GDSII format. Each reticle file is then checked with the manufacturing rule check (MRC). This is a necessary tape-out verification methodology, where individual layers are verified to comply with mask-shop requirements. MRC does not check for any functionality or interlayer considerations but only fulfillment of mask-shop guidelines for reticle production. These include identification of minimum line and space dimensions, grid snap issues, etc. Photonic curved structures pose a challenge for IC mask shops due to their unusual shapes, often leading to re-establishing mask acceptance criteria different from that in electronics.

9.4.2.5 Tiling and Fracturing

Depending on a fabs' design flow, tiling can be done by the fab after MRC or by the user prior to DRC. Tiling with dummy fillers is necessary to maintain a uniform layer density across the reticle. Uniform density ensures that the implemented process has a uniform impact over the entire reticle field and, therefore, improving the uniformity of devices across the wafer. Dummy generation is often a process of necessity, e.g., to avoid dishing during chemical mechanical polishing. The impact of design density on front-end passive photonic device layers remains a lesser explored area. However, its study is important to enable first-time-right device designs. Finally, the mask file is magnified based on the requirement of the projection lithography system used in the fab. The GDSII file is then converted into a mask-shop specific file format. The process of converting a GDSII file to a mask-shop compatible file leads to fracturing of the polygons into simplified shapes.

9.4.2.6 OPC, LFD, Biasing

Optical proximity correction (OPC), lithography friendly design (LFD), or biasing, are some of the methods that are useful to ensure that geometric biases due to lithography and density are addressed, and non-CD geometries can be fabricated as intended by the designer. LFD allows users to mimic the fabrication process in their CAD simulators to predict how their custom device will result on chip. This allows any unintended changes due to fabrication to be offset. Biasing is a manual way to correct for such fabrication variation based on a lookup table supplied by the fab.

This bias table contains design geometry versus on chip dimensions. Optical proximity correction (OPC) is performed by the fab, where extra relief is added to the mask file prior to tape-out. These relief structures are added to conform to the on-chip production of design on mask. These design flow related tape-out steps can improve the yield of the design. They are not a standard in photonics today and are the subject of engineering effort.

9.4.2.7 Mask-Shop Communication

It is important to communicate well with the mask-shop regarding the photonic-specific features on the tape-out; specifically regarding the frequent use of discretized curved polygons used in FEOL photonic layers (ring resonators, photonic crystals, etc.). It is preferable to use a small grid size for the mask to minimize random phase error noise. The fractured mask files are sent to the mask-shop for reticle production. The mask-shop in return provides details on CD uniformity, linearity, etc., which require the reticle requestor's approval. There are important differences with electronics in the photonics mask order. For example, electronic IC mask shops use a convention of minimum design size as the critical dimension for mask production. This aspect of electronics is not applicable to photonics. In photonics the minimum feature size may be 100 nm on the mask (e.g., to realize the narrow inverted taper tips) but 80 % of the design may be around the 400 nm regime. The photonics process is intended to yield the 400 nm feature, but the process window allows dimensions down to 100 nm. In such a scenario, communication with mask-shop for photonics tape-out is crucial. Thus, efficient communication where the mask shop understands photonics-specific intricacies, and the mask-requestor the assumptions of electronic tape-outs, is crucial to a successful silicon photonics tape-out.

9.4.3 Flow Setup and Follow-up

While the mask is in preparation, it is possible to begin process preparation. This includes identifying the test wafers and device wafers, deciding process splits, and preparing the lot for the first lithography step. In most fabs today, such process flows are set up electronically. The process modules are archived and reused. Process modules comprise a sequence of steps to achieve a certain result, such as lithography, etch, deposition, etc. Such modules are mature with defined specification limits and frequently monitored through automated recipes. If required, any drifts in the process are immediately corrected. During processing at critical fabrication stages 'holds' are embedded to temporarily stop the processing and allow manual inspections. This is typical after FEOL photonic device patterning to verify CD uniformity, or custom user devices, thickness measurement after germanium growth, to monitor BEOL CMP steps, etc. After critical process milestones, wafers

may be used for functional testing, cross-section analysis, etc., to ensure the targeted specifications are met, and changes if needed can be implemented. Current silicon photonics processing is increasingly complex with upwards of 30 mask layers, complex processes such as epitaxy, 6–10 implant levels, etc. Fabs maintain above 50 process specifications that are periodically tracked to ensure that photonics line processes are maintained well.

9.4.4 Qualification and Yield Analysis

During and after processing, end-of-line functional characterization of the wafers is performed. Since the silicon photonics material system permits high device density, manual measurement can take a very long time and can be less reliable due to the sheer volume of measurements on each wafer. Therefore, wafer scale data is collected through automated wafer scale test setups where fiber probes and electrical pins are programmed to test devices for specified optical spectrum and electrical parameters (measurement recipe). Data analysis of the collected raw data is done to analyze the yield of the wafer. These measurements can take upwards of 4 h to characterize 20 device-under-test (DuT) sites on 20 dies per wafer. The testing time can be reduced with the use of fiber arrays instead of single fiber probes, efficient sources, etc. Various challenges remain in reliably doing wafer scale testing for photonic wafers. Wafer scale optical testing in silicon photonics is enabled by grating couplers. The performance of the input and output grating for any circuit is strongly dependent on the height and angle of the fiber above the wafer. Therefore, a noncontact yet accurate determination of fiber height and its adjustment is essential for reliable analysis of DuTs. Other challenges include impedance matching for travelling wave devices, stable temperature across measurement routines, etc. It is also important to ensure the testing methodology is aligned with the final product performance when the device is packaged.

9.4.5 Dicing

Dicing for photonics is comparable to electronics. However, depending on how the inverted tapers are processed, accurate dicing within 5–10 μm from the device facet may be needed. Further, the inverted taper facet is required to be perfectly vertical. If the facet is not vertical, some light may be reflected out of plane and may contribute to the insertion loss. This issue can be addressed by a deep dry-etch process to realize edge coupler facets. The resulting trenches can then be diced with higher tolerance. Due to the lithographic process, the facet alignment to the taper edge can be quite accurate, and due to dry etch, the facet wall can be optimized to be vertical. Techniques to package the device without the need for diced facets are also being explored [16].

9.4.6 Packaging and Reliability

Packaging is one of the most significant challenges in silicon photonics. The more obvious challenges are the need for matching a single mode fiber's mode field to the 100× smaller mode of a nano-waveguide. Polished fiber facet-based solutions using grating couplers and end fire coupling-based solutions have been proposed. Further, dense single mode fiber connectors to chip that have minimal power penalty are required for photonics chips. For example 40–50 single mode fiber connectors on a single 5 mm × 5 mm chip may be needed. Further, due to the potential to be deployed in high bandwidth systems, electrical connectors that can allow electrical signals up to 50G per channel are required. Apart from these technical requirements, it is essential for the package to be mechanically robust, manage thermal constraints, and provide protection against ambient conditions. Industry is looking to address the challenge of translating proof-of-concepts to automated assembly lines [17, 18].

9.5 Summary

Megafabs produce 10,000–25,000 12″ wafers per week in their normal capacity. The silicon photonics industry has the potential for approximately 25,000 wafers per year or ~500 wafers per week by 2021. This volume forecast is for datacom applications. At that stage, currently invested fabs can meet such demands. This will ensure the ecosystem becomes mature and that the technical challenges of low volume production are overcome. As the technology becomes pervasive it will acquire greater market acceptance. Such a working ecosystem will propel innovation and create new market segments through accelerated product development cycles. It is conceivable that by 2025 the silicon photonics industry will reach medium volume demands through high speed consumer cables and disposable point of care diagnostics. Either through the incremental volume expansion, or through the interconnect bottleneck in CMOS chips, or the convergence of both, silicon photonics may reside as a standard process module within megafabs.

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Chapter 10
Silicon Photonics Research and Manufacturing Using a 300-mm Wafer Platform

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Abstract After 15 years of research, silicon photonics has now reached a sufficient level of maturity at the device level to be implemented into low-cost optical communication products. In this chapter we review the challenges of the industrialization of silicon photonics in 300 mm facilities, using mainstream CMOS methodologies. We first review the challenges of a sustainable electronic and photonic integration allowing the production of low-cost chips for the current 100G generation but also for the future 400G and beyond. Next, the industrial testing strategy and the design of test circuits allowing an efficient process monitoring are discussed. The industrial process integration scheme of optical components on 300 mm wafers is then described, followed by the device model strategy, which is a key element in order to make the link between the photonic design kit and the process. Finally, further R&D efforts in 300 mm allowing new functionality for the longer term Si photonics development are discussed. As examples, the integration of several Si etching levels, the demonstration of smart SOI substrates feasibility for improved coupling efficiency, and integration of ring modulator are detailed.

10.1 Introduction

Since early 2000 a strong research effort has allowed the silicon photonics concept to come out of laboratories and reach industrial development. This increased interest from the industry mainly comes from the continuous growth of data exchange inside data centers, pushed by the development of the Internet mobile communication. Since 2011, this amount of data has reached 1 Zettabyte (ZB) per year. After [1], it is now doubling every 3 years and should reach 7 ZB per year by 2017 (Fig. 10.1). Consequently, the development of the transceiver chip design is

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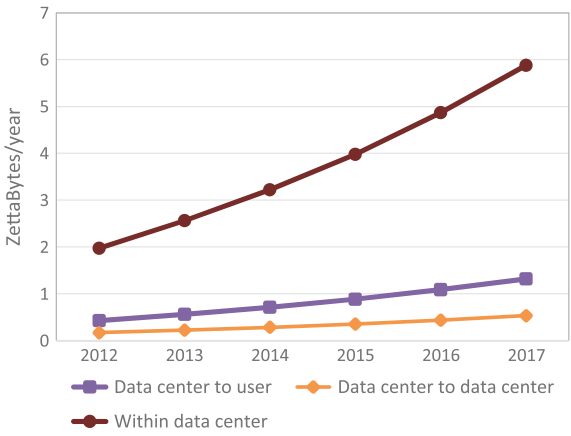


Fig. 10.1 Traffic evolution in data centers, after [1]

now fully addressing the 100 Gb/s market, and will soon move to 400 Gb/s and then reach the 1 Tb/s frontier. The number of chips needed to address the data rate increase of such systems is increasing with the complexity of the data center architecture, and is no longer limited to short distances (1–100 m), but is extending to 2-km reach with the creation of giant data centers [2, 3]. For the front panel, today 100 Gbits/s generation in a data center uses 25 Gb/s VCSEL solutions with multimode OM4 fiber for a 100-m reach. Recent PSM-4 and CWDM-4 MSA consortiums will address the gap between 100G 10 km single-mode multiwavelength solutions and 100G short-reach multimode, multi-fiber solutions. Indeed, combining data rates higher than 25 Gb/s plus a smaller module volume, such as the CFP4 and QSFP28, gives aggressive specifications on power consumption—the typical specifications are 6 W and 3.5 W, respectively. At the same time, the bandwidth requirements are also increasing for ultrashort-reach applications, such as board-to-board and, in the near future, chip-to-chip communications where over tens of Tb/s data rates are desirable (Fig. 10.2).

Optical communications are then expected both in switch and compute nodes. New features mainly concern the distance reach between panels, higher aggregate bandwidth/port density, being closer to ASIC at the board level and potentially the mixing of SDM and WDM approaches. Such requirements imply developments of optical technology to be in line with the specifications for transceiver modules such as low power and to be compliant with packaging constraints, for example.

Due to this increasing demand, the price per chip is also becoming very critical to fulfill the low-cost target. Silicon photonics is expected to play a major role and economic and low-power transceivers are targeted for data center link lengths up to 500 m using single-mode fiber based on emerging Si photonic platforms.

Si photonics has the potential of being compatible with the industrialization methodologies used in CMOS technologies for the last several decades. Of course, since photonics is not scalable in terms of critical dimensions, there is no direct equivalence with Moore's law, which allowed a reduced transistor cost, but Si photonics will benefit from existing fabs and toolsets so that the development cost is

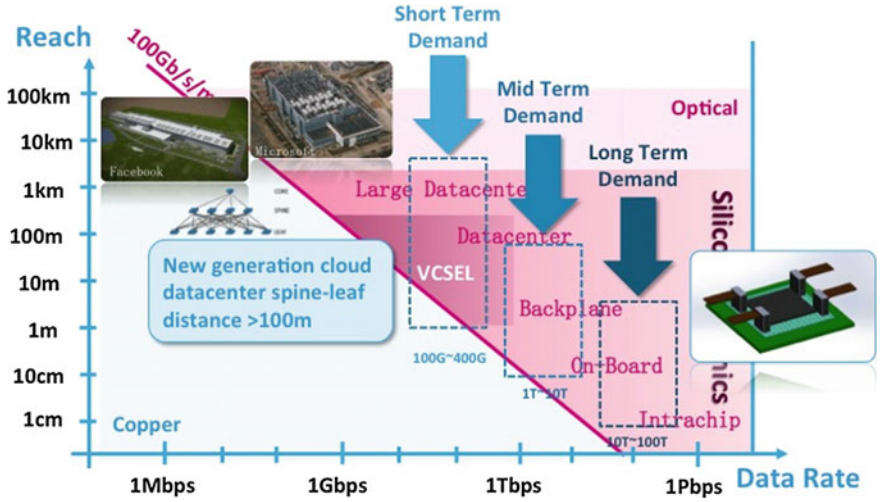


Fig. 10.2 Data rate versus reach Si photonics roadmap, after [4]

far lower than for CMOS technologies. This is where using 300 mm facilities to produce silicon photonics comes into play. These fabs are already massively used for 90 nm down to 10 nm technologies, allowing the process development of silicon photonics to be made with amortized and accurate production tools. At the sub-90 nm node, lithography can be easily controlled with overlay errors of less than 20 nm and sub-100 nm dimensions are commonly achieved with a relatively low-cost lithography mask. For even more precision needs, single patterning 193 nm immersion lithography has also been available for more than 10 years.

But a low-cost process is not a sufficient condition to produce a viable low-cost silicon photonics technology. An efficient electronic and photonic integration, a usable design kit, an industrial testing strategy, and a low-cost packaging strategy are key elements in order to successfully industrialize silicon photonics products. In addition, R&D efforts resulting in new functionality are also key for a longer term view of Si photonics development. This chapter will describe how these elements are handled from the perspective of industrialization, except the packaging part that will be discussed in detail in Chaps. 7 and 8.

10.2 Industrialization Strategy and Electronics: Photonics Integration

10.2.1 Silicon Photonics Qualification Methodology

A technological platform development in silicon photonics has to be done with the same constraints as for any other microelectronics platform, and follows three main criteria [5]:

- Answer to a technological need in terms of performance, cost, quality, and planning
- Use a strict methodology allowing the target to be reached while controlling planning and cost
- Being compliant with the international roadmaps or MSA to ensure that product objectives are coherent and useful.

The overall cost of a technology platform is the sum of the development cost (depending on resources, development duration, technological choices, targeted performances), and the production cost (fab yield performance, cycle time, and testing strategy). The development phase and the associated technological choices made during this period are then fundamental to ensure a sustainable production and the lowest possible product cost. This development phase can be divided in three different subphases:

Phase 0 is the definition of the guidelines for the R&D phase of the technology platform. The main output of phase 0 is the definition of specifications that will be reached at the end of the platform development. All the available data from previous advanced R&D studies, literature benchmarks, standards, and simulations are generally used in order to define the targeted devices and the initial technological choices necessary to reach the final product specifications

Phase 1 is where most of the experiments are carried out and is very resource consuming. Its main objective is to demonstrate on silicon that the technology is able to actually reach the previously defined performances and to extract of first set of spice models to enable building a silicon-based design kit. This will allow the product designers to start preparing prototypes in the targeted production facility.

Phase 2's main objective is to qualify the reliability of the devices at the wafer level, based on thermal and electrical stresses, and to put in place all the tools and methodology that will allow a statistical follow up of the key parameters of the technology at the process and device levels. These key parameters are chosen based on the criticality for the functionality and performance of the technology. At the end of the Phase 2, a low volume risk preproduction can start.

Phase 3 consists in the qualification of the reliability of products, allowing full volume production to begin.

A proper design kit, and especially models as well as reliability are essential components of the industrialization procedure. At the scale of the photonic die (>10 mm) and given the nonregular layouts typical from optical systems, we anticipate that robust design requires behavioral models that include process corners locally and at the die level, plus qualification tests per applicable standards.

10.2.2 Electronics and Photonics Integration

Before discussing the various ways of the cointegration of electronic ICs (EIC) and photonics ICs (PIC) it is worth discussing the requirements of EICs. Figure 10.3

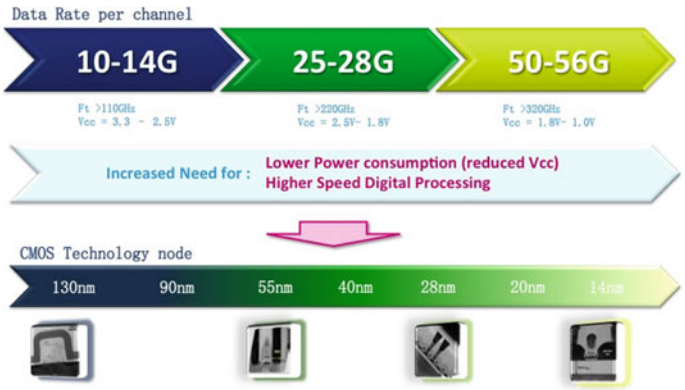


Fig. 10.3 Correspondence between photonics nodes and CMOS nodes

Table 10.1 Available transistor architectures and related substrates for advanced CMOS nodes

CMOS node (nm)	Transistor architecture	Substrate
55	Bulk	Bulk
40	Bulk	Bulk
28	Bulk, FDSOI	Bulk, UTBB SOI
20	Bulk, FinFET	Bulk
14	FDSOI, SOI-FinFET, FinFET	Bulk, SOI, UTBB SOI

shows the evolution of the data rate per channel ("photonics technology node") as expected in the coming years. As data rates are increasing from the 10–14G generation to 25–28G then up to 50–56G, the energy budget per bit has to be reduced. The consequence is that the electronics used to drive the photonics has to feature at the same time a higher $f_t \approx 7.\text{BW}$ together with a lower power supply V_{cc} and an increased processing speed for clock data recovery and SERializer–DESerializer integration. Hopefully, Moore's law is providing the direct answer to this problem through the scaling of CMOS technologies. The lower part of Fig. 10.3 is an attempt to show the CMOS technologies corresponding to the future photonics data rate per channel. If 130 nm technologies were sufficient to sustain the 10–14G photonics node, 25–28G is requiring the use of 55–28 nm general purpose CMOS technologies. As an extension, an energy efficient 50G–56G technology might use 28 nm CMOS down to 14 nm CMOS.

In the past years, the full monolithic integration of CMOS with photonics has been widely developed. The main issue to be solved was the difference in substrate requirements between the electronics and the photonics.

If photonics requires an SOI substrate with a buried oxide (BOX) layer about 1 μm thick, electronics technologies are relying on a considerably different substrate depending on their architectures. Table 10.1 describes the various technologies used between 55 and 14 nm for CMOS nodes.

Proposed solutions are usually either to create locally a thicker BOX, mandatory for the light confinement in Si waveguides, or to adapt the CMOS technology to the SOI and BOX thicknesses chosen for the photonics. The first approach was demonstrated by IHP [6], Samsung [7] and to some extend Micron [8], whereas the second one was industrialized by Luxtera [9] and is also used by IBM [10].

Nevertheless, those strategies successful with a 130–90 nm CMOS node have strong drawbacks when moving to much more complex processes. Indeed, with the first option, integrating a local optical isolation into a bulk, FinFET and UTBB SOI technology will "reset" all the learning on the process technology yield of the initial CMOS node. This will be costly, and necessitate a yield ramp-up of several months. In the second option, the device structure itself needs to be adjusted, with a strong impact on the final design kit and on the production costs, since CMOS device architecture has to be modified. Finally, even if the silicon photonics market growth is important, it is unlikely to justify such investments at each change of "photonics node."

Therefore, the path chosen for the development of a sustainable Si photonics technology roadmap has to rely on independent processes for the EIC and the PIC. Fortunately, advanced CMOS packaging solutions are using 3-D assembly technologies at the industrial level. One of the commonly adopted approaches is known as the face-to-face copper pillar bumps assembly. Typical copper bumps are about 80 µm, which is too big for a low parasitic and high density, and as a consequence we developed a smaller 40 µm pitch copper pillar technology, which is compatible with high-frequency operation. Figure 10.4 shows some examples of assembly used for the production of silicon photonics ICs. With such an integration strategy, electronic and photonic processes are then optimized separately, leading to an integral reuse of the CMOS processes without any modification. The photonic process is also optimized, allowing the implementation of process bricks, and their future evolution (examples will be given in the last two paragraphs of this chapter), answering to the needs of present and future photonics nodes (Figs. 10.5, 10.6, 10.7, and 10.8).

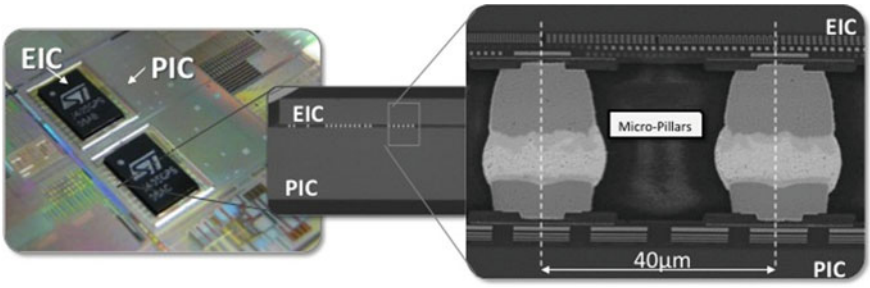


Fig. 10.4 Example of electronic IC and photonic 3-D IC integration using a micropillar technology

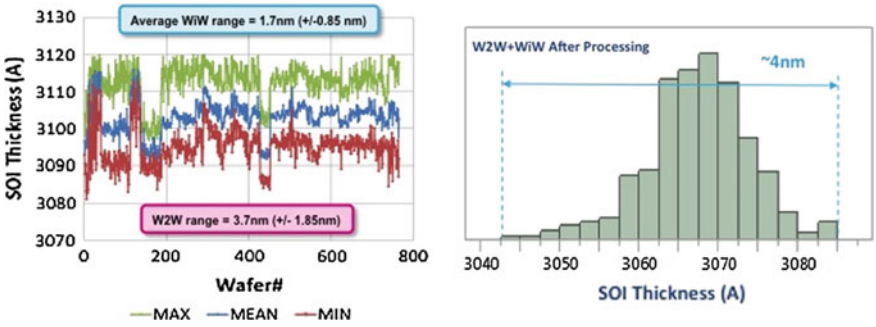


Fig. 10.5 Within wafer (WiW) and wafer-to-wafer (W2W) dispersion of the initial SOI substrate thickness and at the end of the optical component processing

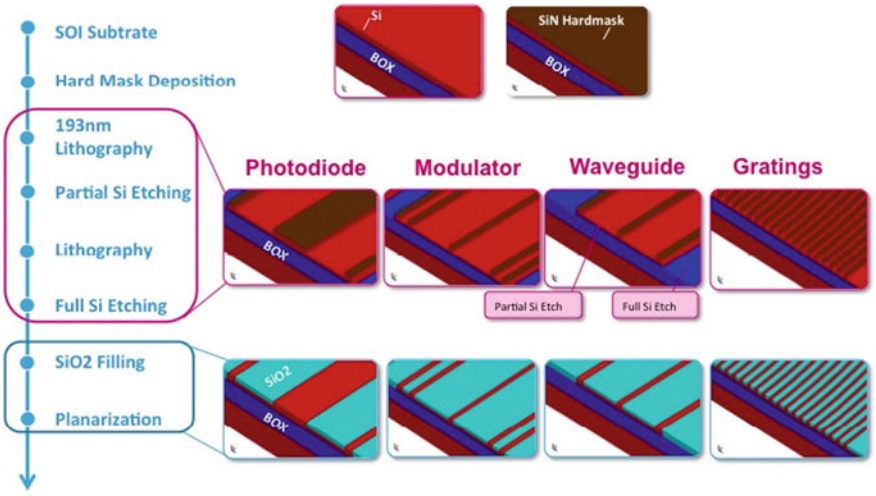


Fig. 10.6 Process flow for optical passive patterning

10.2.3 Industrial Testing Strategy for Wafer Sorting

In order to allow a large volume fabrication of Si photonics products, an adequate optical and electrical wafer sorting (OEWS) strategy is mandatory. The 3-D integration scheme described above allows a separate testing of optical wafers and electrical wafers, prior to the 3-D assembly. This procedure maximizes the yield of the subsystems prior to the integration into the final optical module. After the EIC die to PIC wafer assembly, the complete resulting OIC can be tested and sorted. If the testing procedure of the electrical ICs is widely known and optimized, the wafer sorting of the optical wafers requires optical I/Os compatible with a large-scale

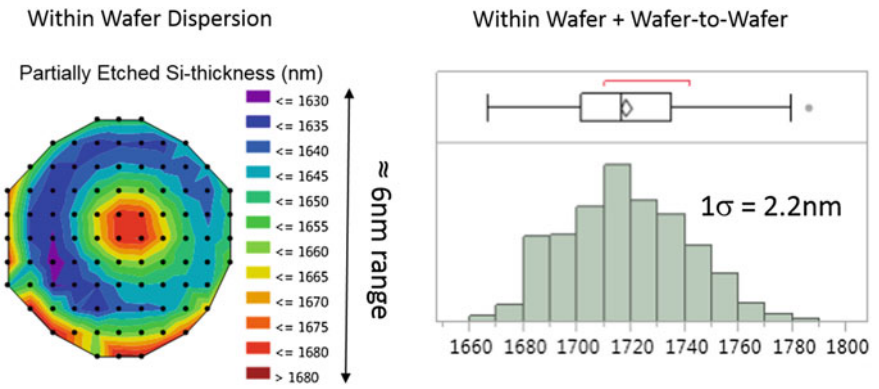


Fig. 10.7 (*Left*) Wafer map of remaining Si thickness after partial etching: (*left*) within wafer, (*right*) wafer-to-wafer and within wafer dispersion of the Si thickness

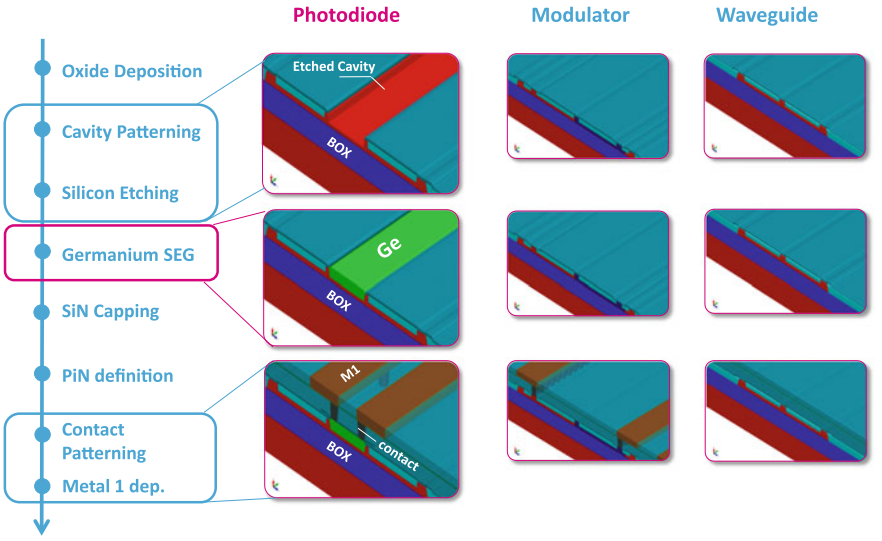


Fig. 10.8 Process flow for high-speed modulator and high-speed photodiode definition, followed by MEOL and first level of BEOL

testing strategy. Since the laser source is external and packaged on the chip at a later stage, the OIC testing relies on optical fiber coupling.

There exist two main optical coupling schemes from optical fiber to silicon photonics chips: edge coupling and surface coupling. The edge coupling principle is to align the core of the optical fiber with the silicon waveguide, generally using a mode converter to minimize the insertion loss coming from the mode mismatch between the fiber (10 μm diameter) and the silicon waveguide (∼0.5 μm). The

coupling performance is generally less than 1 dB [11], polarization insensitive, and with a large optical bandwidth. Nevertheless, this procedure is difficult to apply for optical wafer sorting since it requires a preliminary chip dicing and edge polishing. The second principle is relying on surface grating couplers [12]. Those grating are polarization sensitive, and their typical coupling performance can be 1.5–2.5 dB for TE mode (or less than 1 dB when using a back reflector) and 3–4 dB for TE+TM modes [12, 13]. Their strong interest is the possibility to test optical wafers without any prior dicing, which makes this solution the main choice for a large-scale fabrication of silicon photonics despite some of the limitation of the devices.

Fully automated optical–electrical prober stations are used in our 300 mm facility. In addition to the in-line process parameter, every wafer coming out of the fab can be sorted based on the measurement of key optical parameters such as optical passive device performances (waveguide loss, optical I/O insertion loss and peak wavelength, directional coupler splitting ratio, etc.), high-speed phase shifter (phase shift and loss), and photodiode performance (responsivity, dark current, and optionally 3 dB bandwidth).

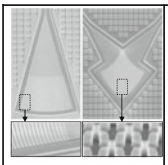
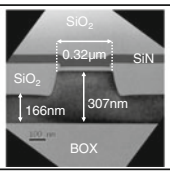
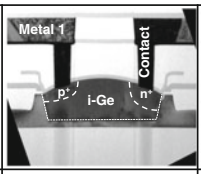
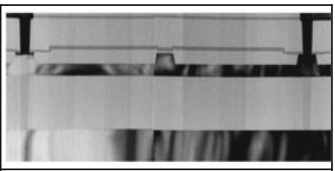
In addition to this device-based wafer sorting, a test chip strategy is being developed. At the 3-D level, between the EIC and PIC, a mechanical stress in the thinned Si photonic chip due to the assembly processes (like mass reflow and thermocompression at the wafer scale [14]) will be present. Moreover, the 3-D interconnection though the micropillar will be very close to optical components to solve area constraints and/or electrical effects. Stress induced locally and at the stack level can affect the refractive index tensors and thus Si photonic devices, which are very sensitive to the change in refractive index, and the magnitude of these phenomena can be checked using a dedicated test chip. Another topic is the local dispersion, which has also to be taken into account.

10.3 Photonics Process Integration and Process Control on 300 mm Wafers

The main advantage of using a 300 mm CMOS facility to develop a Si photonic technology is the availability of a large panel of processing tools featuring a large spectrum of possibilities. The PIC25G platform [15] was therefore developed without any specific process tool investment and by selecting adequate tools within the existing panel. The same is true for SOI substrate manufacturers, and the first consequence of moving to 300 mm from 200 mm wafers was the improvement of the SOI thickness dispersion by a factor of 2 when considering wafer-to-wafer and lot-to-lot variations [16]. The average SOI thickness is 310 nm, with a typical 300 mm intra-wafer exhibiting less than a 2 nm thickness variation measured on a 50-point mapping across the wafer (Fig. 10.5).

Starting with this material, a typical photonics process is described below, and it relies on five main “process modules”:

Table 10.2 Main optical devices processed in the 300 mm photonic platform

			
Single Polarization Grating Coupler & Polarization Splitting Grating Coupler	TE Rib Waveguide	Integrated waveguide Ge High Speed Photodiode	Integrated P/N junction depletion mode High Speed Phase Modulator

- Optical passive component patterning
- High-speed modulator definition
- High-speed germanium photodiode definition
- Middle of the line (MEOL)
- Interconnects (BEOL)

TEM cross-sections of the main optical devices at the end of the process are shown on Table 10.2.

10.3.1 Optical Component Patterning

This module, described in Fig. 10.6, relies on a CMOS 55 nm-based 193 nm lithography allowing a minimum trench resolution of 80 nm and σ = 1.3 nm. This lithography essentially defines all of the passive optical components such as the waveguides, optical I/Os relying on a surface grating coupler, the optical splitters (directional couplers with various ratios, Y junctions), etc.

The etching of SOI is done in two passes. A first partial etching allows defining the slab of the rib waveguide-based component. The average slab thickness is 163 nmat the end of the patterning module. The thickness control of the remaining silicon layer is a key parameter of the photonics process. Indeed, optical properties of passive devices are directly linked to this value. For instance, the dispersion of the peak wavelength of the single polarization grating coupler is directly proportional to the dispersion of the remaining SOI thickness. A typical thickness range obtained using the 300 mm etching tool is 6.5 nm, versus about 18 nm with 200 mm etching tools (Fig 10.7). The dispersion including wafer-to-wafer and lot-to-lot variations has a standard deviation of σ = 2.2 nm. The second patterning step is then applied, consisting of a full etching of the silicon, in order to fabricate the optical isolation and also a set of resistors that are offered together with the platform.

Finally, an oxide filling and a planarization are done, allowing the fabrication of the lateral cladding of the optical components.

10.3.2 Active Optical Component Definition

The high-speed modulator consists of a series of ion implantations into a contacted waveguide, allowing the definition of a PN junction inside the waveguide itself. The positioning of the PN junction into the waveguide is defined by a lithographic overlay of ±20 nm. In order to ensure a low resistivity contact, the area below the contact plugs is silicided using a conventional CMOS process based on $CoSi_2$ material. In order to prevent the silicide to be formed on the optical components a silicon nitride protective layer is deposited and patterned before the Co deposition and silicide formation anneal. Then a SiN contact etch stop layer and SiO_2 hard-mask are deposited prior to the photodetector cavity patterning. After a partial silicon etching, controlled with a range of 10 nm, a selective epitaxial growth (SEG) of germanium is performed using a two-temperature step epitaxy [17]. After a protective SiN layer deposition, a P-i-N diode is defined by lithography and implantation into the germanium. Typical process control is ±10 nm in overlay and ±12.5 nm in CD for the two implantation levels. The corresponding process flow schematic is shown on Fig. 10.8.

10.3.3 Middle of Line (MEOL) and Back End of Line (BEOL)

The MEOL and BEOL bricks rely on a typical CMOS 0.13 µm process. Both W-plugs in contact with Si and Ge are patterned at the same time. The intermediate SiN layer deposited above the germanium acts as a contact etch stop layer for the Ge, whereas the conventional contact etch stop layer previously deposited is used for controlling the contact etching on $CoSi_2$.

Metallic interconnects consist in four levels of metallization plus an aluminum layer and are patterned using a single damascene process. This number of layers is mandatory to allow an electrical routing for transceiver systems having to handle from four to more than eight channels. The need for a four-layer BEOL comes at the price of a trade-off with the optical coupling using surface grating I/Os. Indeed, the dielectric stack is acting as an interferometric filter, and some adjustments have to be carried out to avoid a huge spectrum distortion in the optical signals. Instead of redeveloping the entire BEOL to adapt the thicknesses of the SiO_2 and SiN intermetallic dielectrics in order to minimize the interference effects from 1310 to 1550 nm, we simply removed above the optical I/Os the thick SiN layer used as passivation layer (Fig. 10.9).

10.3.4 Device Performance

Table 10.3 shows a synthesis of the device performances at λ = 1310 nm obtained with the process mentioned above.

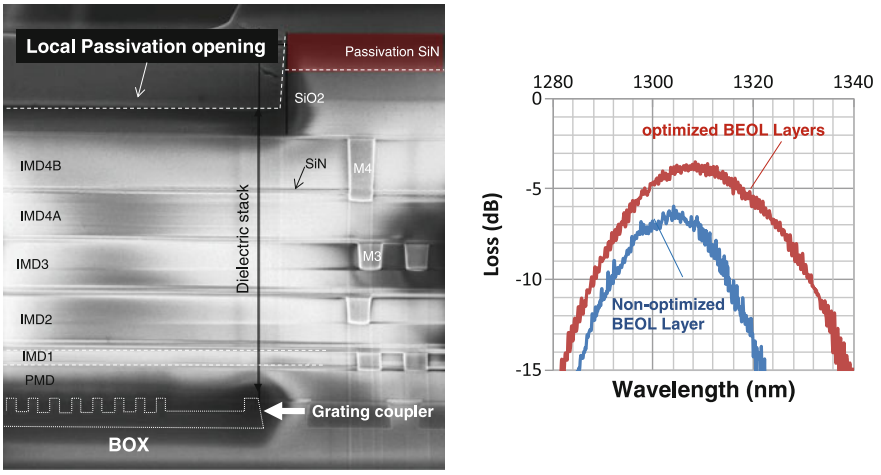


Fig. 10.9 (*Left*) Cross section of dielectric stack above grating couplers (*right*): I/O loop (containing two SPGCs) measurements with and without SiN passivation opening

Table 10.3 Performance table of the main optical devices fabricated in a 300 mm line

	Performance	Standard deviation
Waveguides	SMW loss (dB/cm): 1.8 MMW loss (dB/cm): 0.25	0.18 0.07
SPGC	IL (dB, in air): 2.2	0.15
PSGC	IL (dB, in air): 3.2	0.26
HSPM (2.5 V)	Phase shift (°/mm): 17.2 Loss (dB/cm): 6	0.4 0.14
HSPD (1.0 V)	BW (GHz): >20 GHz Dark current (nA): 100 Responsivity (A/W): 0.98	– 0.34 decade 0.05

10.3.5 Toward Optical Test Chip Development for Process and Performance Monitoring

This section gives details of the possible strategies to handle optical wafer-level testing prior to the 3-D electronic IC.

10.3.5.1 Static Qualification Test Chips: Process Monitoring and 3-D FEBE Optical Compatibility

With respect to the above-mentioned detailed characteristics of Si photonic chips, a strategy must be devised to ensure design manufacturability and to perform qualification tests. The method, which is derived from the semiconductor industry, aims

at facing the characterization of complex integrated circuits. Typically, wafer-level optical testing is necessary to identify KGDs (Known Good Dies) before subsequent assembly with the electronic die and the light source that is performed in assembly houses before the final packaging step. Nevertheless, the die selection strategy is only valid if proof is brought up that none of the assembly and packaging steps can result in additional penalties. For example, stress-induced device drifting due to 3-D assembly should be leveraged.

Process Monitoring

Light loss in optical components based on the TE mode in the rib waveguide is very low (<0.05 dB for the passive ones) and it is necessary to cascade them to monitor the loss with a wafer-level optical tester. In the conventional testing strategy, one test structure is usually preferred for each component (in part due to challenges for multiports measurement with the fiber array because of the intrinsic misalignment of ±1 μm for individual fiber in the V-groove [18]). For each structure, an accurate alignment is mandatory, leading to a long overall testing time and mask area for the process monitoring of a whole component library (i.e., more than 15 components).

The topic of optical wafer sorting from a foundry point of view represents a new era since wafer-scale optical testers are not as mature as electrical testers and the optimum testing strategy for silicon photonics has still to be written. Focusing on time and accuracy, our current developments deal with a solution for which we access the individual loss with only one optical excitation and N output currents, thanks to the integrated photodiodes. A qualification test chip example is illustrated in Fig. 10.10.

A power splitter plus a reference photodiode is used to determine the input photocurrent value versus the wavelength. The loss of an individual component is simply determined by the ratio of the input and output photocurrents, assuming that the photodiode responsivities are the same at the die scale. A supplementary benefit is that the de-embedding of the input grating coupler spectral response is not necessary.

Figure 10.11 shows the spectral response of insertion loss for successive measurements of 15 paths including an SPGC plus a photodiode in serial; the distance between the photodiodes is equal to 100 μm.

We note a very good matching between the responsivities, which confirms our hypothesis at the die scale and illustrates also the robustness of "fiber array to SPGC" alignment methodology with the optical tester.

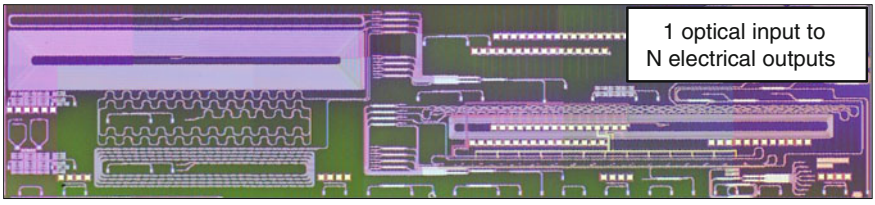


Fig. 10.10 Optical micrograph of an integrated electrical-optic test chip for parametric tests and wafer sorting

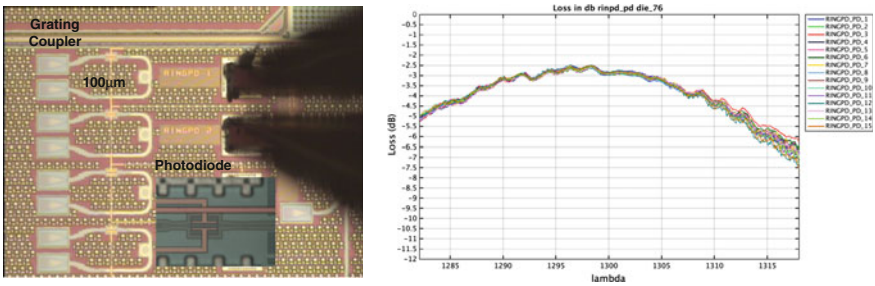


Fig. 10.11 Optical micrograph of a test structure to monitor the photodiode responsivity variability at the die level and insertion loss versus wavelength measurements

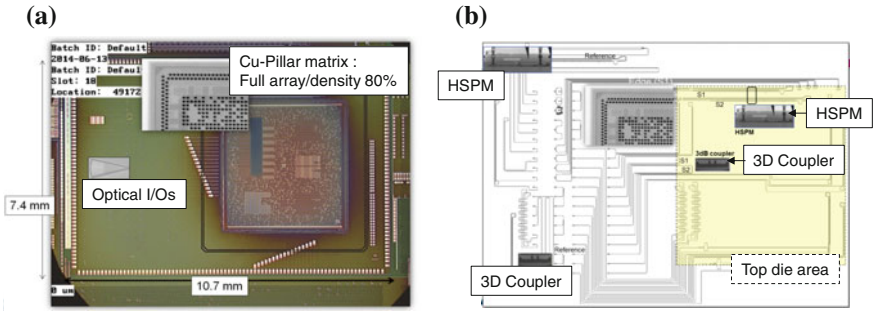


Fig. 10.12 **a** Optical micrograph of Front End Back End (FEBE) optical compatibility test chip. **b** Details of passive and active devices' test structures to track stress effects

3-D FEBE Optical Compatibility

The phase of photonic devices is affected by the refractive index of the waveguide, which can be changed by stress due to the photoelastic effect [19]. To track influence on passive and active components, an example of test chip qualification is presented in Fig. 10.12a. All devices under test are connected to a matrix of grating couplers on the left of the die stack and specific precautions are adopted to allow wafer-scale optical testing with the top die present. The EIC and PIC dice are assembled in a Cu-pillar full-array configuration with a density of 80 %.

The same component is subject to three environments: at the top die periphery (S1), 300 µm inside (S2), and alone (Reference). The X-ray picture highlights that two rows of Cu pillars are present at the periphery of the top die. The present example, Fig. 10.12b, shows locations of 3 dB couplers and diode modulations in the Mach–Zehnder interferometer (MZI).

The coupling coefficients for the stand-alone and peripheral 3 dB, etc., couplers extracted from the measurement of the outputs' optical power are plotted versus the wavelength in Fig. 10.13. Some stationary waves exist between the optical input and output due to reflections from grating couplers and also several transitions like

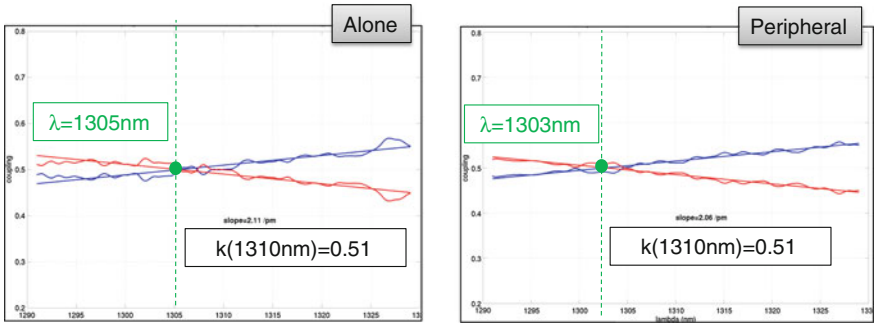


Fig. 10.13 Measured coupling coefficients of a 3 dB coupler for the stand-alone device and the stressed one by EIC (Electrical Integrated Circuit)

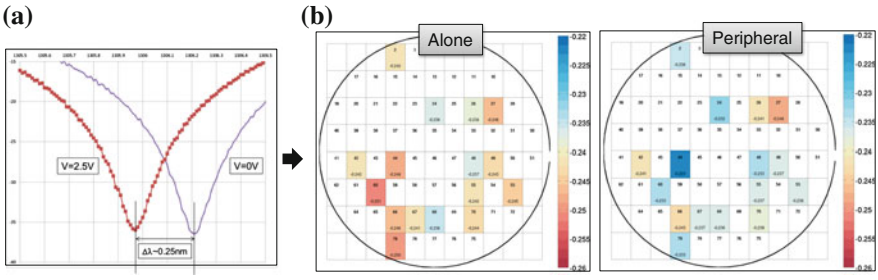


Fig. 10.14 **a** Peak shift of an unbalanced MZI biased on a reverse-biased PN junction. **b** Peak shift at the wafer scale for the stand-alone device and the stressed one by EIC (Electrical Integrated Circuit)

the bend to the multimode waveguide for the long optical path to reach the 3 dB coupler under stress in this case. Final extraction is so done after a fit of the smoothed spectral responses. The coupling coefficients computation does not need de-embedding of the SPGC response.

Inspection of the coupling coefficients looks at two figures of merit: values at the center wavelength (1310 nm in this case) and the wavelength for a 50 % ratio. Similar features are observed and help us to conclude that for such a sensitive device versus the even and odd propagation mode characteristics, stress effects at the wafer scale after 3-D assembly are negligible.

Regarding the potential impact of mechanical stress on optical modulators, in order to extract the phase shift of the carrier depletion-type PN junction an unbalanced MZI configuration is used. The test consists of optical scans across the desired wavelength range as the voltage across the diode is swept. Figure 10.14a shows the spectral response for two voltages (0 and 2.5 V), resulting in a peak shift around 0.25 nm for center wavelength of 1310 nm. We observe that no stationary waves perturb the response and so the accuracy depends only on the step measurement, equal to 0.01 nm in this case.

Random extraction at wafer scale of the peak shift in nanometers is reported in Fig. 10.14b. The medians are, respectively, equal to 0.2425 and 0.2365 nm for the stand-alone and peripheral test structures, respectively. With an intrinsic error of 0.005 nm (due to step measurement), this exercise highlights that potential stress distribution in the SOI photonic interposer has no effect on the phase shift feature.

10.3.5.2 Dynamic Qualification Test Chips Without EIC: The Modulator Example

In silicon photonics, numerous academic and industrial researches have been done on the carrier depletion-mode PN junction to realize an embedded phase shifter within the arm of a MZI or tuning the optical resonance for a ring resonator [20]. The performance of silicon optical modulators has mainly four core metrics: the phase efficiency, the capacitance by unit length, the speed, and the optical loss.

Work to improve the modulation efficiency should not be done at the detriment of spectral bandwidth or increased sensitivity to fabrication errors, for example.

In terms of dynamic qualification circuits at the wafer scale without the top die, we have to manage at least three aspects. The first one is related to equipment issues like RF/DC probes plus fiber array footprint and the way to properly drive the modulators by an external high data rate NRZ signal from the ParBERT (parallel bit error ratio tester). From these constraints, realistic figures of merit have to be identified.

The Mach–Zehnder modulator (MZM) is a simple test vehicle to dynamically qualify the device and integration technology of the optical phase modulator. To illustrate aspects mentioned above, we present in Fig. 10.15 the comparison of a measured eye diagram at 25 Gb/s for a test chip based on the classical traveling wave electrode (TWE) approach [21] and a modular multistage architecture proposed in [22]. Eye diagram measurements are performed on both architectures by directly accessing inputs pads via RF probes with NRZ PRBS (nonreturn-to-zero pseudorandom binary sequence). For the TWE design, the differential NRZ PRBS is amplified by two modulator drivers from SHF suitable for data rates up to 44 Gb/s [23].

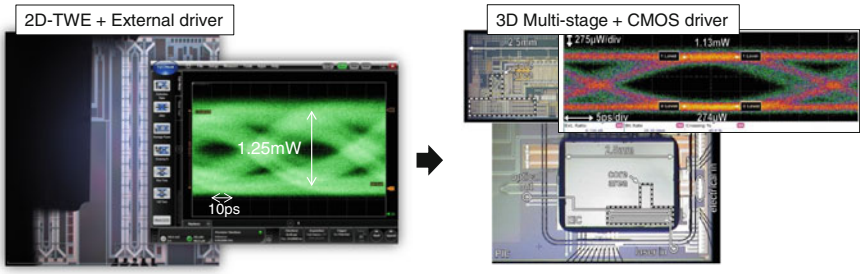


Fig. 10.15 Measured eye diagrams at 25 Gb/s for 2-D traveling-wave modulator and 3-D assembled OIC+EIC solution [22, 26] based on a reverse-biased PN junction

The main difference consists in the way the PN junction sections see the driving voltage. For the 2-D TWE architecture, the MZM insertion loss caused mainly by the impedance matching issues and RF losses, leads to a driving voltage that is not constant along the electrodes. On the contrary, the 3-D multistage solution with micropillars, minimizing the interconnection parasitic capacitances, and the local CMOS driver that ensures the desired voltage amplitude for each capacitive load of the PN section (150fF @ 0 V bias) results in an excellent OMA (optical modulation amplitude) at 25 Gb/s.

For 2-D TWE MZM, there is certainly room for improvement with regard to operation at high speeds since for some time experimental researchers have nevertheless demonstrated good eye opening at speeds higher than 25 Gb/s [24, 25] at the expense of a large footprint for the lateral PN junction.

To obtain a compromise on the electrical and optical I/Os, footprint, OMA, and achievable speed, we have developed the 2-D-meandered modulator presented in Fig. 10.16a. With the implementation of a PN junction in the 180° bend, we can achieve a DC extinction ratio of 9 dB with the additional feature of a 10.5°/mm phase shift under 2.5 V reverse bias for only a 1 mm long footprint (for a total of 5 mm active length). Resistive load termination of the TWE MZM is integrated on-chip, which allows it to be driven in push–pull mode due to only one RF differential probe including DC inputs for reverse bias adjustment and to set the MZM static operating point due to the low-speed forward-biased PIN phase modulators; see Fig. 10.16b [27]. Such layouts are in addition expected for the next generation of transmitters, that will need to satisfy both high data rates (>25 Gb/s) and low power consumption [28].

As an example, we report in Fig. 10.17 the measured eye diagrams at 5 Gb/s for the 2-D TWE architecture and the meandered one at wafer scale. Only the fiber array and the InfinityQuad probe are necessary to perform such dynamic characterization. On the principles detailed for the process monitoring, photodiodes should be used as outputs enabling us to use only one optical fiber and so reap inherent benefits. For the 2-D-meandered solution, the differential line is

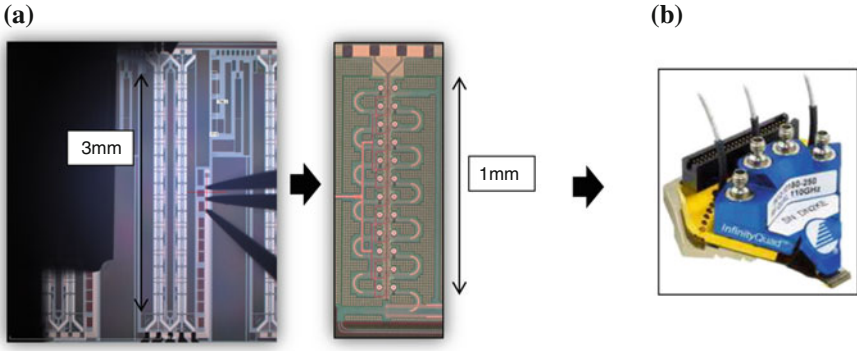


Fig. 10.16 **a** Optical micrograph of all active multisection compact MZI. **b** InfinityQuad™ multi-contact probe

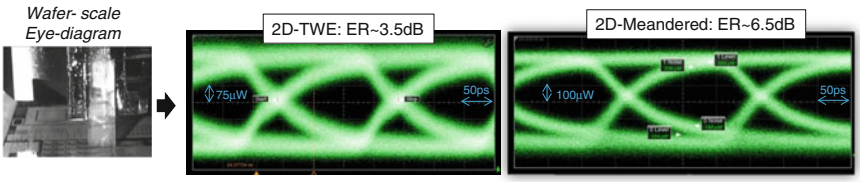


Fig. 10.17 Measured eye diagrams at wafer level of traveling-wave modulator and meandered multisection one based on a reverse-biased PN junction

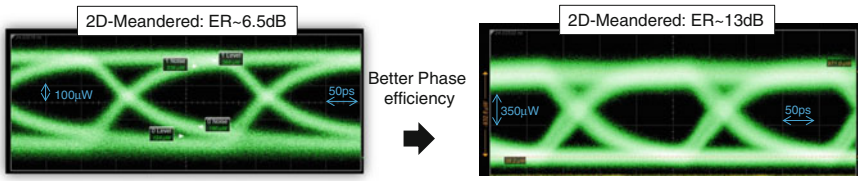


Fig. 10.18 Measured eye diagrams at the wafer level of a meandered multisection modulator based on the optimized doping and junction offset position for a maximum modulation efficiency

periodically loaded by a huge capacitance and this represents an intrinsic speed limitation. However, good OMA achieved at a data rate lower than 10 Gb/sand quickly helped us to validate the new device and associated integration technology based on what we call the "gold modulator."

Pushed by the number of bits per baud increase for higher order modulation like PAM-4 (pulse amplitude modulation), the MZM has to satisfy a minimum extinction ratio to encode two bits into four intensity levels. Keeping the same driving voltage or even lower for power consumption purposes, the phase efficiency must be improved. In the spirit described above, we embed an optimized lateral junction without any design modification in the 2-D-meandered modulator. The measured eye diagram at 5 Gb/s is reported in Fig. 10.18. Straight and bend active sections have expected features and an extinction ratio greater than 10 dB is achieved under push–pull operation mode with an output amplifier driving voltage around 3 Vpp.

10.4 Design Kit and Spice Model Approach

An industrial design kit is a key point to enable silicon photonics products. The design kit is the link between the product designer and the facility in which the silicon wafers are fabricated. The main elements of a silicon photonics design kit (Fig. 10.19) are:

- A Physical Design Kit, allowing the creation of the layout of the optical components in the R&D phase and the fabrication of the development mask sets.

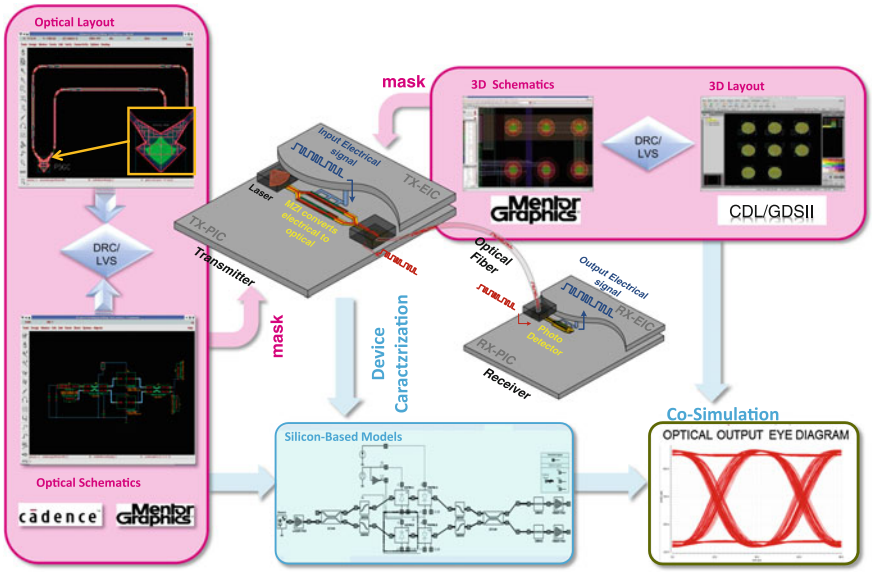


Fig. 10.19 Flow showing the relationship between the different components of a design kit and their usage

- Design Rule Manual (DRM) and Design Rule Checker (DRC) allowing the creation of layout of the optical component (in R&D phase) and full products based on a qualified optical component library. DRM and DRC allow verifying the proper use of dimensionality and density of each layer with respect to the process capability in the fab (e.g., lithography and chemical–mechanical polishing capabilities).
- A Layout versus Schematic Checker (LVS) for both optical and electrical components on the OIC.
- A library of building blocks: parametric cells and optoelectrical silicon-based SPICE models for circuit simulation, including models, corners models, and temperature dependence.
- The capability to run co-simulation with the electronic IC.
- A 3-D capable LVS checker.

10.4.1 Photonics Spice Model Development

10.4.1.1 Development Flow

The spice simulation of photonic devices is quite different from standard electrical simulations due to the optical part of those devices, since it is necessary to work on

the key parameters of the optical signal, which are the power, the phase, and the wavelength.

Those optical signal features are directly given by the carrier's wavelength. Nevertheless, commonly used spice simulators do not have the capabilities to provide large transient simulations in the time range of the electrical signal (here 25 Gb/s), by considering directly the carrier's wavelength due to its very high frequency, approximately equal to 220 THz. It is necessary to work directly on the key parameters on the carrier's wavelength. In the design kit (DK) environment, device symbols use a single pin for an electrical node and a bus for an optical node. Each optical bus is divided into three distinct signals for each optical feature:

- Bus <0>: The power
- Bus <1>: The phase
- Bus <2>: The wavelength

In contrast with CMOS technologies, no standard models presently exist in silicon photonics simulations. We implemented dedicated models for elementary photonic blocks, using Verilog-A, in a simulation environment based on SPICE simulators in order to mimic the methodology used by logic and analog CMOS designers. The compact models are physics based and include:

- Voltage bias
- Relevant geometrical parameters of the device
- Temperature dependencies
- Wavelength dependencies
- Full range simulation from DC to ESD range.
- The wavelength dependencies around the working wavelength provides realistic phase shift and optical loss calculations during simulations
- The silicon properties (energy gap, carrier mobility, electric field, etc.) included in the model provides realistic
  - Temperature impact
  - Bias impact

Moreover, as spice simulators are dedicated to electrical simulations, analogies were made in order to handle optical features as electrical signals.

10.4.1.2 Example: Phase Modulator and Photodiode

Models developed for electro-optic devices such as phase shifters and photodiode are used as examples of model implementation. The HSPM (High-Speed Phase Modulator) diode's basic function is to convert an electrical signal into an optical index change of the underlying silicon. When the diode is reverse biased, the phase of the optical signal in the waveguide is modulated by a charge variation in the space charge region, interacting with the optical mode. This leads to a variation of the refractive index and the absorption coefficient and so to variations of the phase

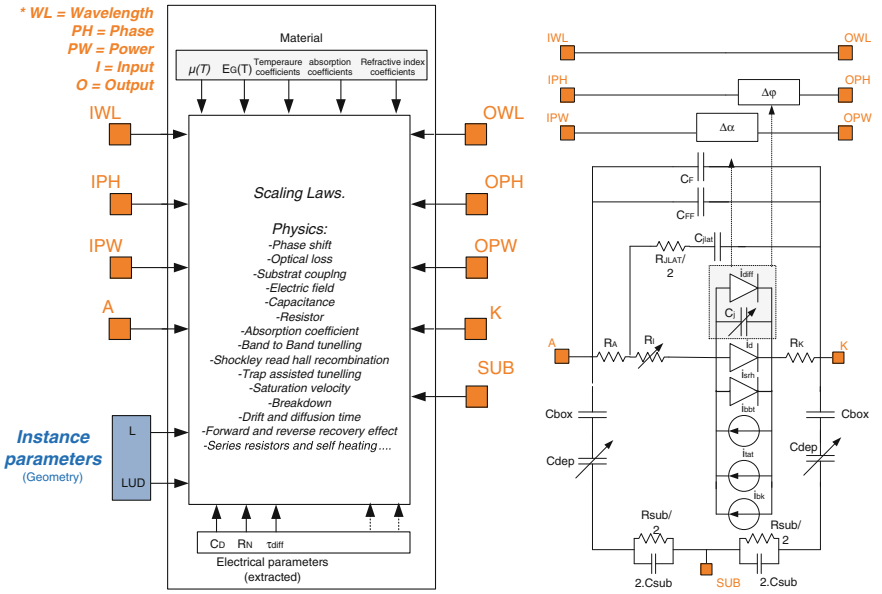


Fig. 10.20 HSPM model structure including intrinsic R and C components

and optical loss. In the associated models the phase shift calculation is directly linked to the electrical charge. Thus, the device optical behavior can be easily adjusted on experimental data by extracting the electrical features and then predict its behavior for a process variation.

In Fig. 10.20, the electrical scheme of the HSPM including the intrinsic R and C components, the substrate/BOX modeling, the leakage current (diffusion, recombination, trap assist, etc.), and the optical parts are described.

The second device described here is the high-speed photodiode (HSPD). The HSPD is used to convert a high- or low-speed optical signal into an electrical current flow proportional to the input optical power level.

The HSPD key performances are:

- *The responsivity* (R, measured in A/W) which is the efficiency of the conversion process, i.e., the amount of generated photocurrent per unit of incident optical power.
- *The dark current*, which is the current in absence of light. The dark current is deleterious because it is not distinguishable from photocurrent (except by turning off the light) and creates shot noise, thus impairing the ability to detect low level signals.
- *The response time* (electrical bandwidth).

When the diode is reverse biased and photons enter the semiconductor with sufficient energy they can create photocarriers (electrons and holes) in the material. Two mechanisms occur simultaneously:

- There is a creation of minority carriers; electrons in the P region and holes in the N region. These carriers create a diffusion current.
- There is a generation of electron–hole pairs in the ZCE, which dissociates under the action of the electric field. These carriers create a drift current.

These two contributions create the photocurrent that is added to the reverse current (leakage without light) of the junction, the dark current. The dark current can be due to

- Shockley Read Hall recombination
- Trap-assisted tunneling
- Band-to-band tunneling

The photodetector model was also developed to take into account all features previously described. The responsivity and the bandwidth are calculated and directly linked to the potential distribution inside the device to predict their evolution with respect to the bias and the temperature.

10.4.2 Spice Model Extraction Flow

The extraction flow methodology is shown in Fig. 10.21. The first step is to provide the process spread by performing parametric tests on different lots and wafers. Then, the golden wafer can be chosen to perform full characterizations on selected dies and on each photonic device in order to have characterization data dedicated to models extraction. The second step is also to perform modeling extraction according to the flow depicted below using DOE to extract model parameters related to physics, geometry, temperature dependencies, wavelength dependencies and including the process spread from the first step.

10.4.3 Spice Models Hardware Correlation

10.4.3.1 The High-Speed Phase Modulator

A voltage sweep between 0–5 V is applied on the cathode of the HSPM and the anode is grounded, in order to have the diode in reverse mode. An optical signal is applied on the input optical port with a 0.1 mW optical power and a phase initialized to 0. The phase shift in degrees, the optical loss in dB and the equivalent capacitance and resistor of this device are compared to measurement in Fig. 10.22. Frequency measurement and modeling of capacitance and resistance are shown in Fig. 10.23.

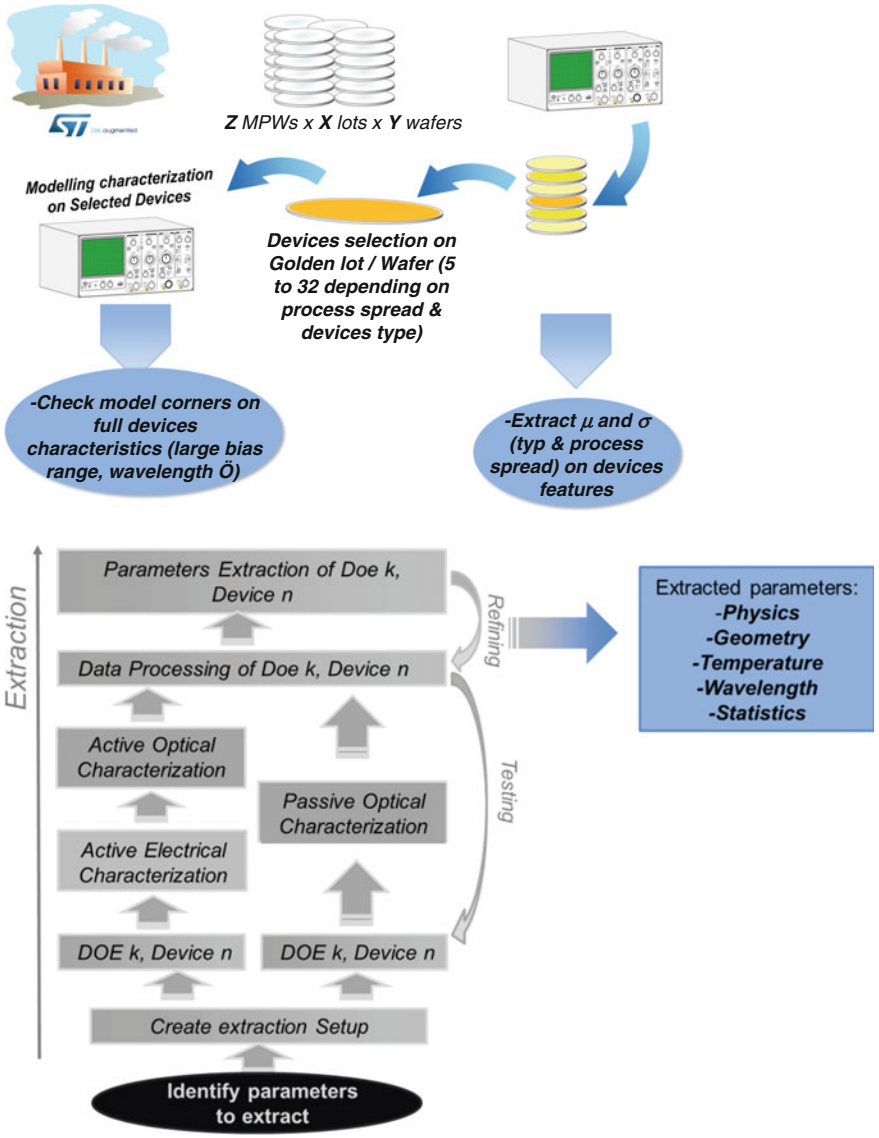


Fig. 10.21 (*Upper*) Process spread extraction flow; (*lower*) modeling extraction flow

10.4.3.2 The High-Speed Photo Detector

A voltage sweep between 0–5 V is applied on the cathode of the HSPD and the anode is grounded, in order to have the diode in reverse mode. An optical signal is applied on the input optical port with a 0.1 mW optical power and a phase

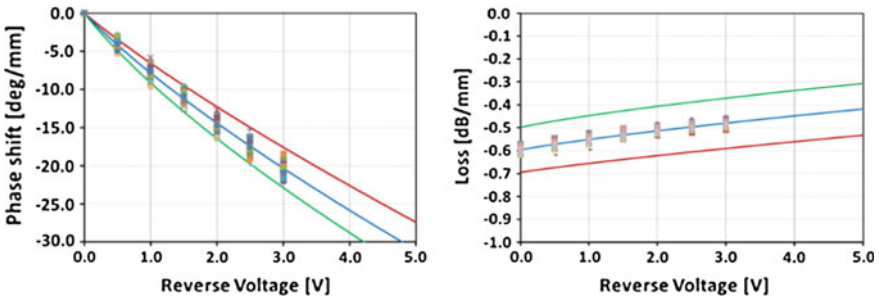


Fig. 10.22 HSPM 1310 nm phase shift and loss with respect to the reverse voltage at 50 °C with corners (process spread)

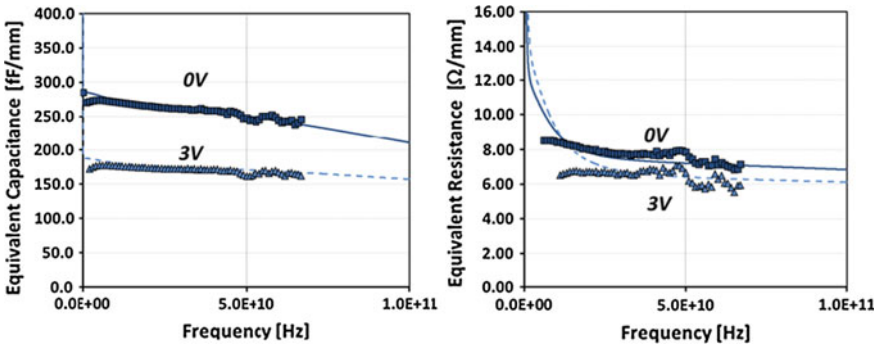


Fig. 10.23 HSPM 1310 nm equivalent capacitance/resistor at 25 °C

initialized to 0. The responsivity and the modulation bandwidth of this device are compared to measurement in Figs. 10.24 and 10.25.

10.4.4 Spice Model Platform Capabilities

The photonics spice models based on extracted silicon allow designers to predict the real behavior and to assess the robustness of their designs by providing a physics-based model including process spread and reliable temperature and wavelength dependencies. The photonics spice models allow the simulations of a RX/TX system with, for example, a MZI simulation in the time domain. Figure 10.26 shows the simulation of a TX eye diagram at 56G [29] that is well correlated with the measurement of the actual circuit fabricated using PIC25G technology described above.

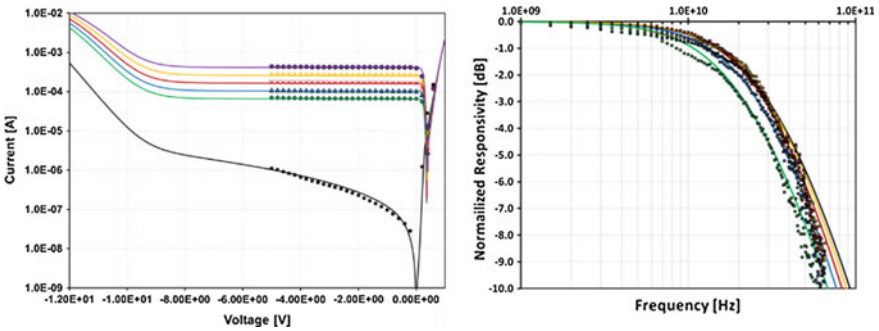


Fig. 10.24 (*Left*) Photodiode darkcurrent and; (*right*) photocurrent (1310 nm) at T = 25 °C: simulation (*line*) and measurement (*dot*)

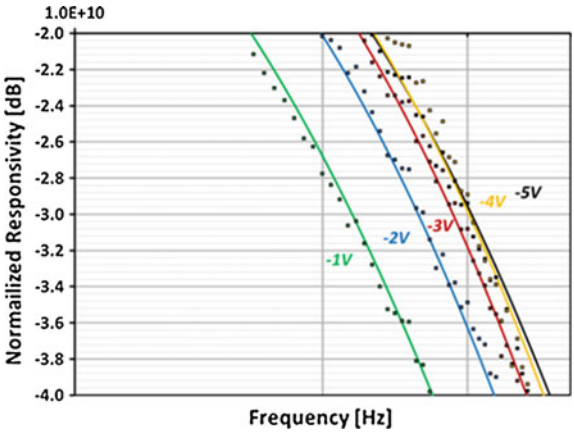


Fig. 10.25 Photodiode (1310 nm) modulation bandwidth at T = 25 °C for different bias: simulation (*line*) and measurement (*dot*)

10.5 Process Exploration for Design and Performance Improvement

Unlike CMOS technology, the rationale behind the silicon photonic technology evolution does not lie in the shrinkage of critical dimensions. The typical sizes necessary to enable optical mode transmission in silicon within the optical data communication band should not vary that much. Another important consideration about silicon photonics is that the main aspects related to large system integration do not only reside in our ability to cointegrate a greater number of devices but also to accommodate a bigger variety of devices. In electronics, very complex functions can be built up using very few elementary devices. However, in photonic technologies the same method cannot be replicated because different optical functions

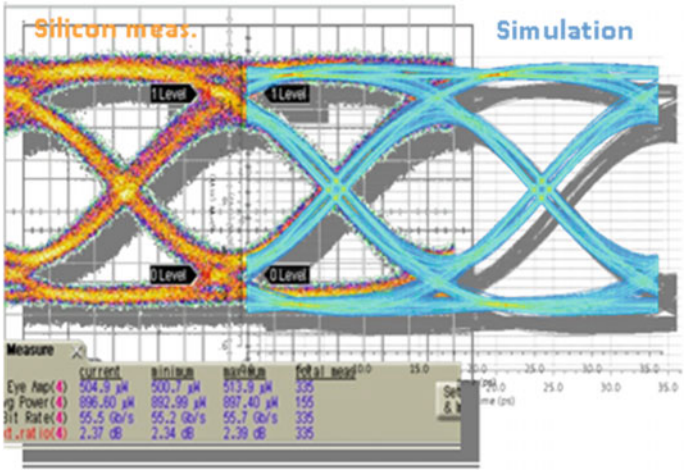


Fig. 10.26 TX Eye diagram at 56G: measurement versus simulation (from [29])

often need dedicated devices. For example, within the framework of data communication, functions such as modulation, detection, switching, routing, and multiplexing cannot be achieved with optimal performances if the same basic devices are used. Consequently, the parameters that can be used to monitor the global photonic system efficiency are mainly the optical losses and electrical power management. Thus, the associated process should enable the cointegration of individual devices with record low levels of losses and consumed power. Among the different building blocks constituting a PIC, there are two that have a major impact on the optical properties of the photonic subsystem: wafer definition and silicon patterning. In this section, a description of how further developments on those two aspects can improve the technology performance, will be given.

10.5.1 Improving Surface Coupling Efficiency

The impact of grating coupler insertion loss on optical circuit performance is critical since these devices are used three times in a typical full-duplex optical transceiver. Therefore, minimizing the insertion loss of grating couplers is a key challenge for silicon photonics applications. Besides improving the grating coupler structure by optimizing the layout and/or enhancing the silicon patterning process, another approach consists of raising the wafer reflectivity. Indeed, a nonnegligible amount of the signal is lost in the wafer due to the relatively poor reflectivity of the BOX/bulk interface. In the current technology node the BOX thickness is chosen to provide an optimal wafer reflectivity in the optical fiber data communication bands. Nevertheless, as shown by the blue and green curves in Fig. 10.27, the latter is rather poor for standard SOI wafers.

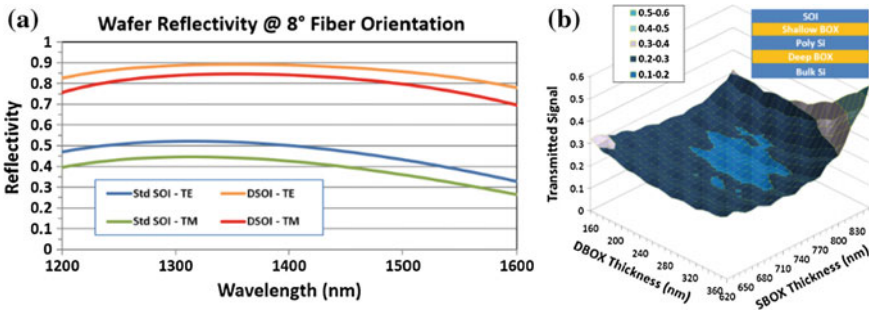


Fig. 10.27 **a** Calculated wafer reflectivity for transverse electric (TE) and transverse magnetic (TM) modes for an off-normal angle of 8°. **b** Simulated reflectivity robustness by varying the Bragg stack

A common approach to improve the surface reflectivity is to include a 1-D photonic crystal, also known as a Bragg reflector, at the relevant interface. In silicon photonics, a spontaneous reaction would consist of thinking about making a double smart cut and wafer bonding. However, this approach would result in very expensive base wafers and, consequently, would not address properly the current silicon photonics market. Our proposed alternative is to deposit a layer of polysilicon within the BOX to achieve the same result. Thus, the process is still limited to a single wafer bonding, which is the most expensive step involved in the wafer substrate fabrication process.

10.5.1.1 Substrate and Back Reflector Optimization

Prior to fabricating the double-SOI (DSOI) wafers, we performed calculations to determine the appropriate Bragg layer thicknesses to achieve optimal reflectivity at the standard data communication wavelengths of 1310, 1490, and 1550 nm. The optimal reflectivity spectrum is obtained for a deep buried oxide (DBOX) of 290 nm, a silicon layer of 85 nm (Poly-Si), and a shallow buried oxide (SBOX) of 740 nm under the silicon-on-insulator (SOI) of 310 nm (red and orange curves of Fig. 10.27a). These thicknesses correspond to the best reflectivity compromise to obtain good performance at the three wavelengths. It should be noted that the reflectivity could be further improved if it were further optimized for a single wavelength. To evaluate the process robustness of fabricating a Bragg reflector within the wafer, a simulation at a constant wavelength of 1310 nm was performed by varying the different layer thicknesses. As shown in Fig. 10.27b, the wafer transmission is almost the same for a broad range of thicknesses. Moreover, using the calculated Bragg stack, the single polarization grating coupler (SPGC) was simulated using a 3-D FDTD model and the relative estimated performance gain is about 0.6 dB when a DSOI wafer is used.

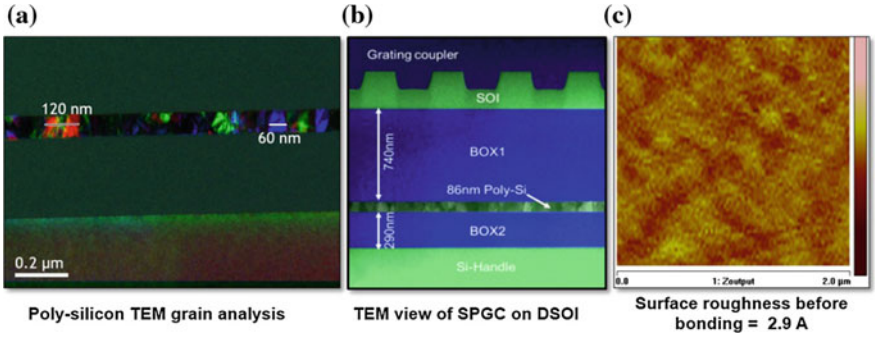


Fig. 10.28 **a** Poly-Si grain size analysis by TEM–EDX. **b** TEM–EDX cross section of SPGC on 300 mm DSOI substrate. **c** SBOX surface analysis by AFM prior to bonding

10.5.1.2 Substrate and Device Fabrication

Starting from a regular 300 mm Si bulk wafer substrate, we performed a 600 nm thermal oxidation followed by a frontside total etch to constitute a backside oxide, in order to minimize the wafer bow prior to the future bonding operation. Then, a 300 nm thermal oxidation was carried out followed by a 90 nm Poly-Si deposition. The Poly-Si characterization by TEM reveals a locally flat surface with grains in the range of the deposited surface thickness (Fig. 10.28a). These two layers together with the Si handle define the Bragg reflector. Following these steps, a 630 nm oxide was deposited and the wafers went through a densification step. The deposited oxide which constitutes the SBOX has a very smooth surface characterized by AFM (Fig. 10.28c). Finally, a 310 nm SOI layer was added using molecular oxide–oxide bonding. Optical passive components, including SPGCs and polarization splitting grating couplers (PSGCs) designed for 1310 and 1490 nm operation, were fabricated on DSOI substrates using 193 nm lithography [15]. A TEM cross section of an SPGC on a 300 mm DSOI substrate is shown in Fig. 10.28b.

10.5.1.3 Optical Characterization and Device Performance

Grating coupler insertion loss performance was measured on several DSOI wafers using a fully automated 300 mm optical prober. As predicted by simulations, a gain of 0.6 dB in insertion loss is obtained. SPGC measurement results show a median insertion loss of 1.47 dB and a best measured loss of 1.25 dB for the 1310 nm design (Fig. 10.29a).

PSGCs, used in the RX parts of transceivers, are key components to manage the detection of a signal with arbitrary polarization. The use of a DSOI substrate is also beneficial for those devices, and a similar insertion loss improvement as for the SPGCs is observed, leading to record low insertion loss of 2.89 dB (Fig. 10.29b). Small peak wavelength shifts of only 7 nm were measured for both devices

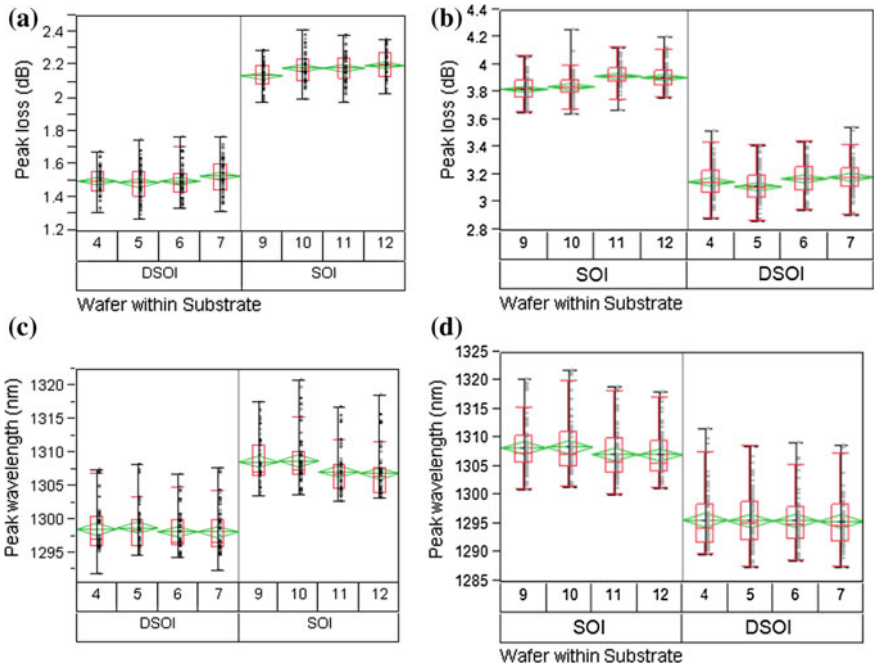


Fig. 10.29 Statistical performance for 1310 nm grating coupler designs on 300 mm standard SOI and DSOI. **a** Insertion loss for the SPGC design. **b** Insertion loss for the PSGC design. **c** Peak wavelength shift for the SPGC design. **d** Peak wavelength shift for the PSGC design

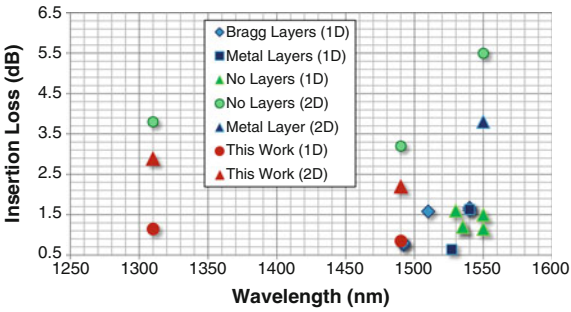


Fig. 10.30 Benchmarking of grating coupler performances for recently published results

(Fig. 10.29c, d) showing that a minor redesign is necessary for the grating couplers. Measurements were also performed for devices at 1490 nm and insertion losses of 0.87 and 2.2 dB were obtained for the best SPGC and PSGC, respectively. In both cases, the wafer-to-wafer variability is low, showing the robustness of the process.

Benchmarking against recent published results shows that our results at 1490 nm are within the best reported and we have demonstrated the lowest insertion loss for 1310 nm 1-D and 2-D grating couplers reported so far [30–42] (Fig. 10.30).

10.5.2 Advanced Silicon Patterning

As mentioned before, new devices are essential to enable more complex photonic functions in advanced integrated circuits. Photonic device geometries are defined, first, by the SOI thickness and, second, by the subsequent silicon etches. In the current node, only one partial etch is used to pattern all the devices in a single step. The chosen etch depth corresponds to the optimal device patterning necessary to obtain the best overall performance at system level. Currently, the two most critical photonic devices in a typical space division multiplexing (SDM) transceiver, from a patterning point of view, are the SPGCs and PSGCs. However, if the number of devices available in the technology's library grows, the single-step unique partial etch compromise becomes very challenging if we were to guarantee optimized device performances. The only way to get around this issue is to increase the number of process parameters. In practical terms, the silicon patterning strategy should be customized so that it can accommodate a larger number of partial etch morphologies. Below, we demonstrate the feasibility of cointegrating two partial etches within the same photonic subsystem.

10.5.2.1 Limitation of Single Etched Waveguides

Simulations using Eigen Mode Solver of Lumerical Mode Solutions have been performed to understand better the challenges of waveguide design. The first consideration is to properly determine the rib waveguide cross section. Parameters driven by the need to properly pattern the grating couplers are a total SOI height of 310 nm and a partially etched silicon thickness of about 163 nm.

Optical signal propagation at the die level can very seldom be limited to straight paths. Consequently, waveguide bends must be properly simulated and designed to find the best trade-off between compact designs and low insertion loss. As shown in Fig. 10.31b, the single-mode waveguide described above is not adapted for small

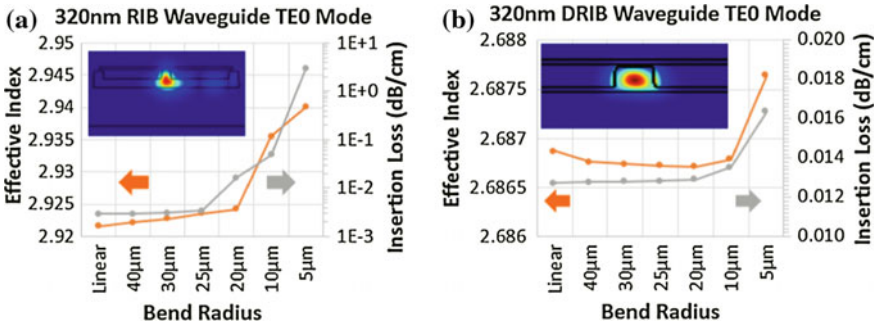


Fig. 10.31 Effective index and insertion loss with respect to bend radius. **a** Slab = 164 nm. **b** Slab = 50 nm

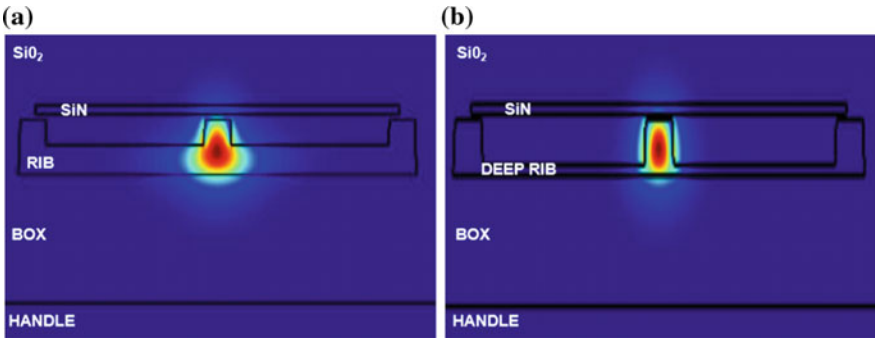


Fig. 10.32 TE0 mode confinement analysis within two rib waveguides of different slab thicknesses. **a** Slab = 164 nm. **b** Slab = 50 nm

bend radii. Indeed, the loss grows by decades when the bend radius is less than or equal to 25 µm. Moreover, the n_{eff} also varies substantially and this results in complex models for the bent waveguides.

Such waveguide properties can be understood better when looking at the TE0 mode confinement (Fig. 10.32a). For a slab thickness of 163 nm, the mode peak intensity region lies below the slab interface. Thus, in bent paths, the mode will readily start to deviate in the slab region and excite parasitic modes. On the other hand, if a rib waveguide bearing a thinner slab is used, the TE0 mode is much better confined and thus, more efficient in bends (Fig. 10.32b). Due to the deeper etch necessary to define that waveguide, the latter is called a deep-rib (DRIB) waveguide. The same n_{eff} and loss analysis have been performed for the DRIB. The optical modes present in the 320 nm wide waveguide are the TE0 and TM0 modes only. Moreover, the intrinsic insertion loss and n_{eff} values remain in an acceptable range even for very small bend radii (Fig. 10.31b).

Consequently, a silicon patterning process has been developed to cointegrate two different etch depths. First, the standard partial etch is performed on the entire circuit. Then, a second photolithographic step is used to mask all the regions where a 163 nm slab is necessary. Thus, the second partial etch will selectively lower the silicon thickness to 50 nm. The critical point in this integration is the proper design and fabrication of the transition taper necessary to switch from a rib to a DRIB region. By making use of the hard-mask present on the top of the waveguides, an autoalignment of the taper is ensured. The design is robust enough to tolerate misalignment overlays of 30 nm, which is the upper limit of our 300 mm technology.

As shown in Fig. 10.33 the DRIB process add-on has successfully been able to demonstrate the feasibility of having two different etch depths cointegrated within the same technology node without impacting the devices and the process of the actual technology node. The taper is properly fabricated (Fig. 10.33b) and the etch profile and critical dimensions are respected (Fig. 10.33d).

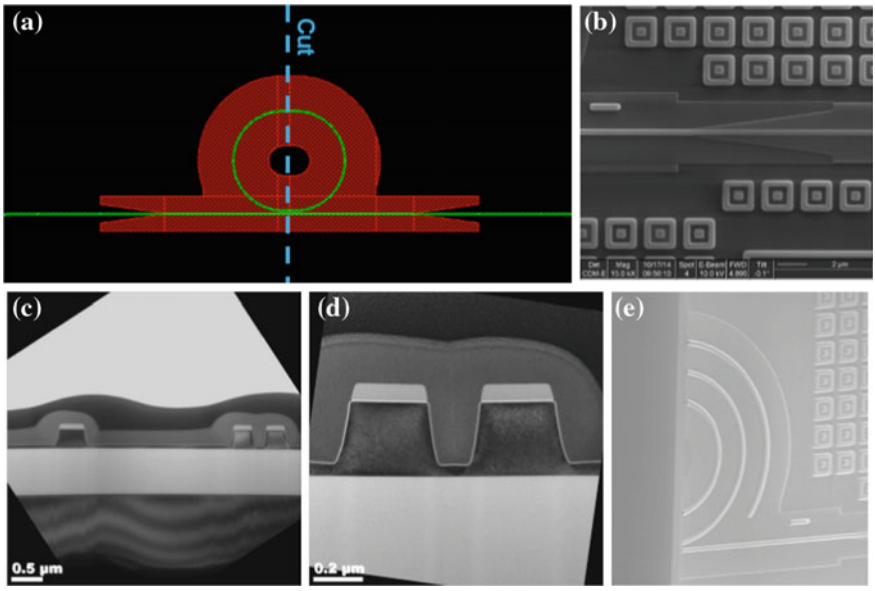


Fig. 10.33 **a** Layout of a DRIB structure. **b** SEM view of the taper. **c** Trench SEM view of the three waveguides described in the cut of (**a**). **d** Enlargement of the coupling region. **e** Overview of an active ring device

10.5.3 Application to Ring Modulator Devices

Ring modulator devices are very appealing devices for silicon photonics. Compared to Mach–Zehnder, they have a much smaller footprint. They have a very narrow bandwidth, which make them perfect devices to build a WDM link in which each wavelength is modulated separately, without prior DEMUX of the wavelength into physically separated waveguides. Ring modulators can achieve a very high data rate, and modulation up to 40 Gb/s has already been achieved with a standard PN vertical junction-based ring modulator [43]. Ring modulators have also been demonstrated to be compatible with multilevel amplitude modulation [44]. At least, ring modulators can be considered as a lumped element, even at high data rate (>10 Gb/s), solving numerous problems caused by the electrical propagation of high-frequency electrical signal, as explained previously. Ultimately, the WDM link will be characterized by several figures of merit: the OMA, the extinction ratio (ER), the data rate (DR), and the crosstalk between two channels.

For radii below 10 µm it is necessary to build a ring modulators system with a free spectral range (FSR) large enough to support a multiple communication channel. Typically, a rib waveguide with a 50 nm slab in a 310 nm thick SOI wafer enables a radius of curvature down to 3 µm. An example of an 8 µm radius ring modulator device fabricated in a 300 mm photonic platform is given in Fig. 10.34.

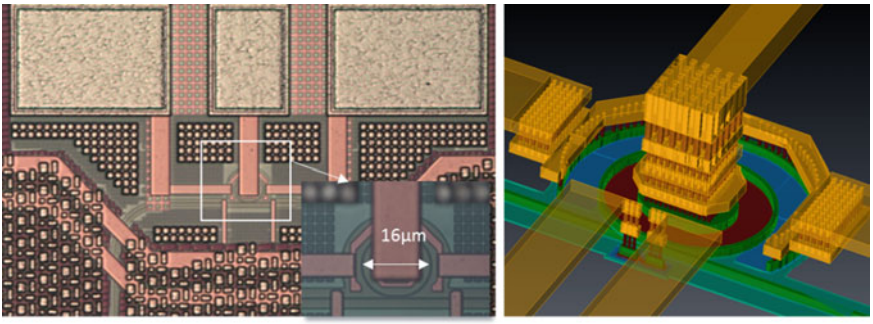


Fig. 10.34 All-pass ring modulator with embedded heater

Integrating the ring modulator within an industrial photonic process requires the above-mentioned addition of a DRIB etching level.

10.5.3.1 PN Versus PIN Architecture

Two types of ring modulator devices can be designed using a silicon photonic platform: a carrier injection PIN diode or a carrier depletion PN junction. Photonic transceiver has already been demonstrated for a PIN diode [45] and a PN diode [46], but those two types of diodes have very different characteristics.

The switching speed of an injection mode PIN diode is limited by the carrier motion in the intrinsic area, but it can achieve a greater displacement of the resonance peak of about 5 nm for 1 mW of current (under a ∼1 V bias). The control of a PIN diode requires additional complexity in the driving circuitry, with signal pre-emphasis to overcome the intrinsic slow carrier motion of the diode [47].

On the contrary, a PN diode's speed is limited by the junction capacitance, which is very small (∼20 fF for a 8 µm ring), and by the photon lifetime in the resonator, which can be controlled by adjusting its quality factor [48]. However, compared to PIN diodes, the displacement of the ring resonance peak is much more limited, up to 18 pm/V [49] for a standard vertical PN junction in the O-band. Although very small, the shift of the peak is sufficient to achieve modulation with a reasonable extinction ratio, greater than 5 Gb/s. Figure 10.35 shows an example of the static peak displacement of a PN diode integrated in a 300 mm photonic platform when a bias is applied, and the NRZ eye diagram measurement is achieved at 10 Gb/s with an external driver.

10.5.3.2 Challenges in Ring Modulator Industrialization

With all the intrinsic qualities of a ring modulator—small foot print, high speed, low power consumption—why has a ring modulator device not yet been widely

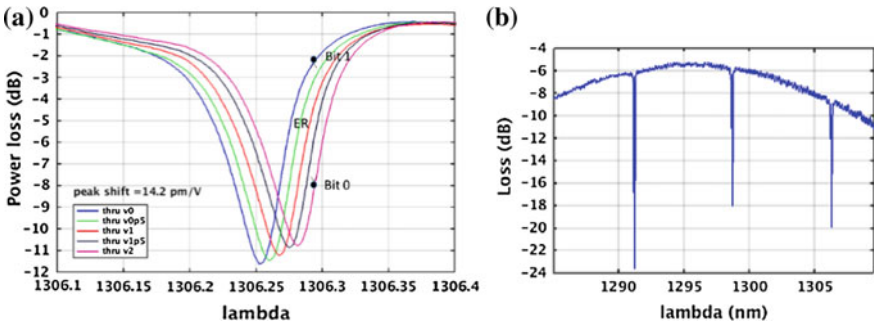


Fig. 10.35 **a** Peak displacement in function of applied voltage for an all-pass PN ring modulator. **b** Full transmission spectrum

adopted for data communication systems? Indeed, although ring modulators in silicon photonics have been extensively studied by different research groups during the last decade, no commercial product currently makes use of this device. Even if recent publications [46] show that ring modulator-based transceivers are close to being ready for an industrial application, ring modulators suffer from one very challenging issue: they are very sensitive to a slight variation of the physical dimension of the rib waveguides. A key challenge is to identify those variations with the fabrication tolerances at wafer scale and to propose an adequate integration technology to minimize them. Widespread adoption of ring-based silicon photonics depends on this progress.

Ring modulators operate using the displacement of resonance peak, when an electrical bias is applied. The wavelength of the laser must be close to the resonance wavelength of the modulator to obtain two logical levels at one lambda (Fig. 10.35). The resonance frequency is proportional to the effective index of the mode propagating (Fig. 10.36). Thus, good control of the effective index is necessary to control the modulation characteristics. For instance, a shift of 10^{-3} in the effective index of an 8 µm radius ring at 1310 nm results in a peak lambda shift of 0.5 nm in resonance wavelength, which is a decade larger than what can be achieved by biasing the PN junction of the modulator. Figure 10.37 illustrates the variation of the peak lambda and quality factor in a mature 300 mm photonics process at the wafer scale. Variations of up to 6 nm in the peak wavelength are observed. Those variations are explained by the variability in the rib waveguide shape, such as slab thickness and rib sidewall. Other known sources of peak wavelength variability are the temperature drift during the transceiver mission mode, and the mechanical stress caused by the vicinity of a micropillar, or through silicon via (TSV) [19], in a 3-D assembly.

The peak wavelength can be controlled dynamically by several technics, such as the use of heater, (Fig. 10.34), but it comes at the expense of additional power consumption and complexity. Achieving a device with uniform OMA and ER requires not only a good control of the position of the resonance peak with regard to the laser frequency, but also a good control of the peak width and sharpness, expressed by the quality factor Q. Adjusting dynamically the quality factor of a ring

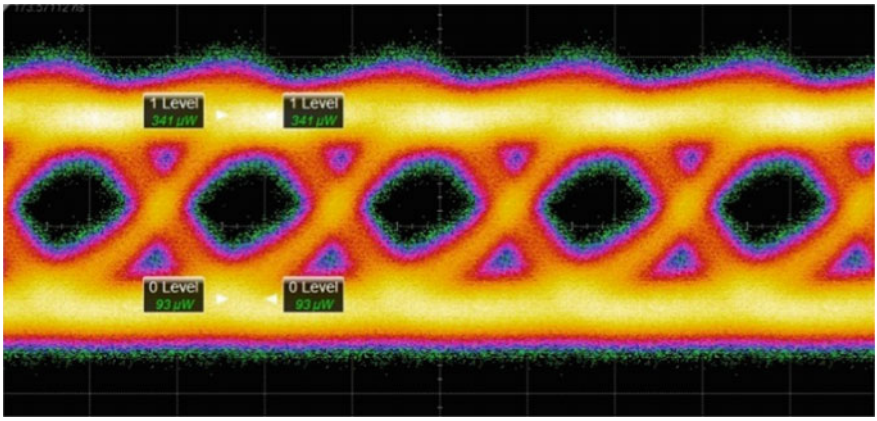


Fig. 10.36 Eye diagram at 10 Gb/s of an all-pass PN ring modulator, radius 8 µm, with an extinction ratio of 5.6 dB

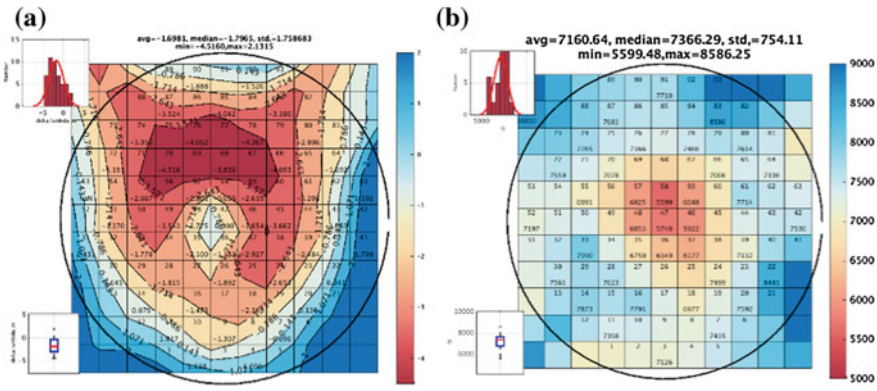


Fig. 10.37 8 µm radius PN ring modulator measured on a 300 mm wafer: **a** peak wavelength variation and **b** Q factor, defined as the peak resonance divided by the full width at half maximum (FWHM)

is even more challenging. Several solutions have been proposed to tune actively the quality factor, such as the use of an embedded Mach–Zehnder to control the splitting ratio of the ring coupler [50].

10.5.3.3 Applications of Ring Modulators

Multiple applications of ring modulator devices can be considered in the near future. We highlight here two of them: process monitoring and chip-to-chip interconnects.

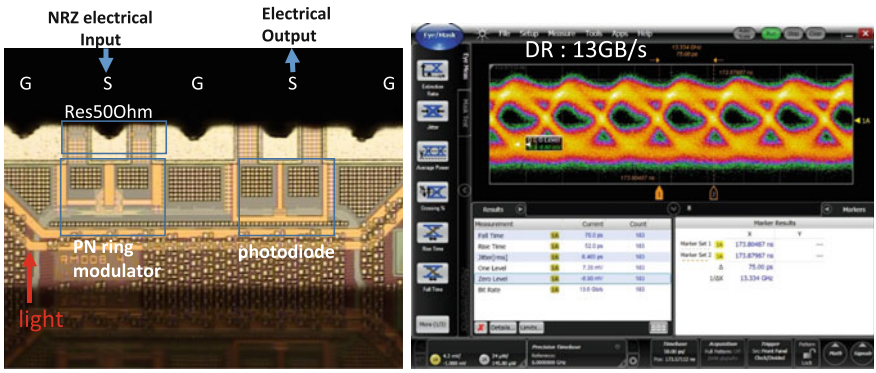


Fig. 10.38 TX/RX ring modulator-based monitoring circuit

The need for process monitoring has been described previously. Dynamic process monitoring can make great use of the compactness of the ring modulator devices. Ring modulators could be used as a reference circuit embedded in any photonics products. It would demonstrate the functionality of the main photonics component, without impacting the footprint of the circuit. The extreme dependence of a ring resonator on the variation of the geometry and loss of a waveguide makes this device a component of choice to track the process variability. Figure 10.38 illustrates this usage: a ring modulator has been connected to a photodiode, allowing full electrical characterization of a RX/TX transmission in a very compact way.

Other applications that could take advantage of the ring modulator characteristics in the near future are the chip-to-chip interconnects and, more specifically, the chip-to-memory interface. To replace chip-to-chip electric interconnects with their demands of an aggregate bandwidth greater than 2–5 TB/s, optical modulators have mainly to be small and low power. A ring modulator based on the depletion-mode junction meets these specifications.

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Chapter 11
Silicon Photonics-Based Signal Processing for Microwave Photonic Frontends

Minghua Chen, Hongchen Yu and Jingjing Wang

Abstract Signal processors are one of the significant elements in microwave photonic frontends, which determine the working ability of the entire system in many aspects. The silicon photonics-based signal processors are especially attractive for their compact size and wonderful performance. We review the development of silicon photonics-based signal processing for microwave photonic frontends.

11.1 Introduction

Microwave photonics frontends as one of the key applications of microwave photonics have been extensively investigated [1–11], which can overcome the limitations in electrical frontends [12, 13], thanks to the advantages of flexible tunability, potential higher dynamic range, and immunity to electromagnetic interference (EMI) [14–16]. Typical microwave photonics frontends consist of a modulator for mixing, a RF oscillator, a signal processor, and a down-converter, among which the signal processor as the key component, especially the integrated ones, has attracted a lot of research interests [17, 18]. Most of the photonic-assisted frontends can be divided into two groups; down-conversion combined with microwave domain filtering based on the microwave photonic filters [9–11], and with optical domain filtering [5–7]. In this chapter, we mainly focus on the frontends based on the down-conversion with optical signal processor, since the bandpass filtering in optical domain simplifies the structure for suppressing the strong out-of-band signals, as shown in Fig. 11.1.

There are mainly three kinds of optical signal processors in the frontends; the finite impulse response (FIR) [19–23], the infinite impulse response (IIR) [24–29], and the hybrid of FIR and IIR [30–32]. FIR signal processers are attractive for their

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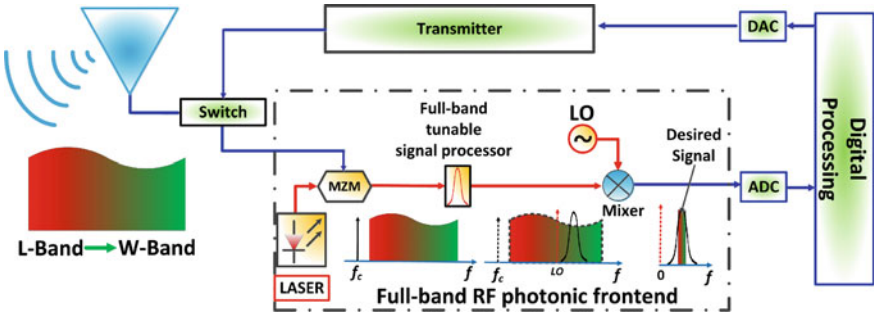

Fig. 11.1 Schematic diagram of the RF photonic transceiver. The transceiver contains two parts, the transmitter and the receiver. In the receiver, the full-band signal received by the broadband antenna would be processed by the photonics method. Owing to the large bandwidth of the photonics methods, it is possible to realize such a full-band RF photonic receiver

linear phase response in the passband. But, constrained by the Mach-Zehnder interferometers (MZIs)-based structure, the free spectral range (FSR) of the signal processor is limited to the same magnitude of the bandwidth. IIR signal processors based on microring resonators are attractive for their compact size and the potential large enough FSR. However, limited by the waveguide loss, to further improve the quality factor (Q) of the filter becomes very difficult. The hybrid signal processors are more flexible to be programmed with both zeros and poles.

In this chapter, we review recent progress in the research on silicon photonics-based signal processing for microwave photonic frontends. We would like to note that the main attention in this chapter will be focused on results obtained in our groups, but it is not our intention here to comprehensively cover all the possible examples of silicon-based signal processing for frontends. The chapter is organized as follows: Sect. 11.2 introduces the signal processors based on silicon photonics. Three different kinds of signal processors have been described; the FIR, IIR, and the hybrid of FIR and IIR signal processors. Section 11.3 emphasizes two kinds of microwave photonic frontends, the parallel system frontend and the optoelectronic oscillator (OEO)-based frontend. Section 11.4 highlights a photonic-assisted software-defined radio (SDR) transceiver based on the silicon signal processing. Finally, we draw a conclusion in Sect. 11.5.

11.2 Silicon-Based Signal Processors

Generally, there are three kinds of integrated signal processors: (1) IIR filters, which usually consist of the feedback loops, have a phase jump in the filter band and are sensitive to fabrication tolerances, (2) FIR filters, which are usually formed by the MZIs and have linear phase responses, (3) FIR and IIR hybrid filter with both zeros and poles. The three kinds of processor characterized for their different properties are presented next.

11.2.1 FIR Signal Processors

The FIR filters have attracted a lot of attention, for their stability, simplicity, and linear phase response. However, all these proposed filters mainly rely on the traditional MZI scheme, whose FSRs are inversely proportional to their differential path length and proportional to their bandwidth [19]. Thus, to avoid this limitation and realize fine and broadband signal processing for their applications, an optical RF channelizer is added to enlarge the FSR [30], which introduces extra loss and complexity to the whole system. So, the multistage cascaded MZIs-based narrow-bandwidth FIR filter is attractive for its enhanced processing range [7, 20, 22, 23] as described below, where the FSR of the filter can be enlarged by increasing the number of MZI stages.

11.2.1.1 Silicon-on-Insulator (SOI) FIR Signal Processor Based on Cascaded MZIs

A schematic diagram of the proposed filter based on multistage MZIs with enhanced processing range and negligible change in the 3-dB bandwidth is shown in Fig. 11.2, where the input- and output-ports on the upper paths (port1 to port2N) are combined one by one. In this design, the differential path length of each stage MZI satisfies the condition by $\Delta L_1 = L$, $\Delta L_2 = 2^{-1}L$,…, $\Delta L_N = 2^{-(N-1)}L$, and the phase-shifters are realized by the microheaters covering on the upper arms of the MZIs. The transfer function of the filter derived from the transfer matrix method [33] can be written as

$$H_{11} = \prod_{i=1}^{N} \left(\sqrt{1-\kappa_{2i-1}}\sqrt{1-\kappa_{2i}}e^{j\phi_i} - \sqrt{\kappa_{2i-1}}\sqrt{\kappa_{2i}}\gamma_i e^{-j\beta(2^{-(i-1)}L)}\right), \tag{11.1}$$

where κ_i ($i < N$) is the coupling coefficient of the ith waveguide coupler that is determined by the coupling length and the distance between the two waveguides, $\gamma_i = e^{-\alpha(2^{-(i-1)}L)/2}$ is the inherent loss induced by the silicon waveguide delay line $\left(\Delta L_i = 2^{-(i-1)}L\right)$ where α is the waveguide power attenuation coefficient, β is the propagation constant along the waveguide, and ϕ_i is the phase difference between the two arms.

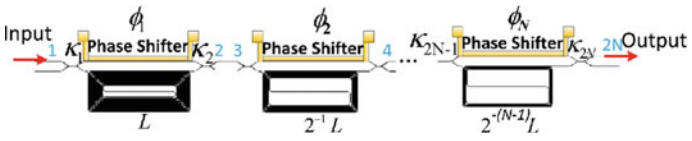

Fig. 11.2 Schematic of the *N*-stage cascaded MZIs tunable filter, in which each stage of the filter can be changed independently

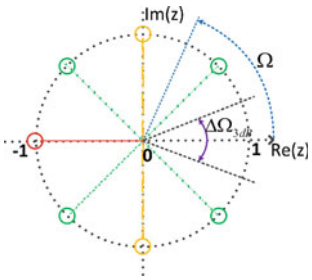

Fig. 11.3 Zeros diagram of three-stage filter. Zeros are shown for the first stage (*green*), the second stage (*yellow*) and the third stage (*red*). The angle covered by the *blue line* represents the amplitude of Ω, and the *arrow* stands for the positive direction. $\Delta\Omega_{3dB}$ corresponds to the 3-dB bandwidth of filter

Totally, 2N couplers are needed for an *N*-stage filter. In order to minimize the transfer loss in passband, the coupling ratios of the couplers are set to satisfy $\kappa_{2i-1} = \kappa_{2i} = (1+\gamma_i)^{-1}$, so that all the zeros are on the unit circle. A simple π phase shift is introduced for each stage in our design to align their resonance, i.e., $\phi_1 = \phi_2 \ldots = \phi_N = \pi$. Therefore, (11.1) can be simplified as

$$H_{11} \propto (-1)^N (1+z^{-2^{(N-1)}})(1+z^{-2^{(N-2)}})(1+z^{-2^{(N-3)}})\ldots(1+z^{-1}), \tag{11.2}$$

where $z = e^{j\Omega}$ and $\Omega = \beta(2^{-(N-1)})L$.

The pole–zero diagram in *z*-plane of a three-stage cascaded MZIs filter is shown in Fig. 11.3, where the zeros distribute around the circle uniformly. One can see from the pole–zero diagram that the FSR of the filter is determined by the last stage of the filter as shown in Fig. 11.2, which can also be derived from (11.2)

$$\mathrm{FSR} = \mathrm{FSR}_N = (c/n_{\mathrm{eff}})/(2^{-(N-1)}L), \tag{11.3}$$

where c is the velocity of the light in vacuum, n_{eff} is the effective index of the proposed structure, N is the stage number, and FSR_N is the FSR of the last stage. As the number of the stages increases, the FSR of the filter is enlarged to 2^{N-1}*FSR_1.$\Delta\Omega_{3\mathrm{dB}}$ corresponds to the 3-dB bandwidth of filter, which is confined by the two zeros separated by the real axis and generated by the first-stage transfer function as shown in Fig. 11.3, i.e., the bandwidth of the filter is mainly determined by the first-stage MZI; meanwhile, the bandwidth will become a little narrower as the number of the stages increases. In addition, the zeros will rotate around the unit circle when the phase difference of each stage MZI changes, which performs a tunable and reconfigurable filter.

The simulation results of the filter response when N = 1, 3, 5 are shown in Fig. 11.4. For N = 1, the FSR is nearly two times of the $\Delta\lambda_{3\mathrm{dB}}$ and the extinction ratio is about 6.5 dB as shown in Fig. 11.4a. For N = 3, the FSR of the filter is enlarged by four times to 16 GHz, nonetheless the $\Delta\lambda_{3\mathrm{dB}}$ decreased a little to

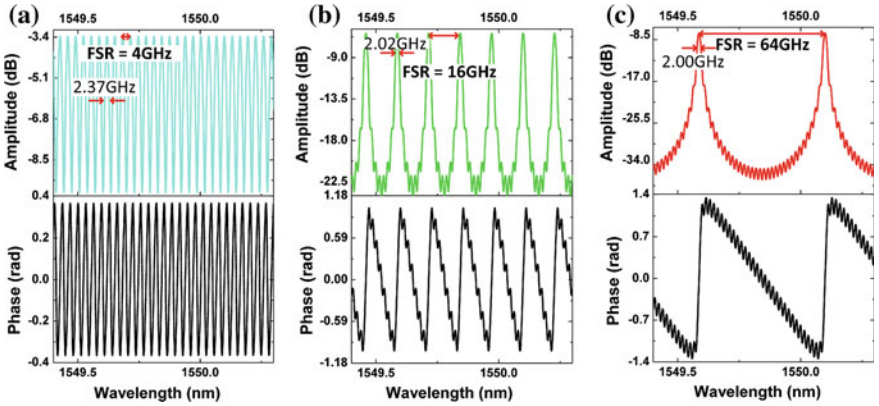

Fig. 11.4 Simulated amplitude and phase response of a multistage cascaded MZIs filter. **a** $N = 1$, **b** $N = 3$, **c** $N = 5$

2.02 GHz and the extinction ratio is about 17 dB. When $N = 5$, the FSR is enlarged to 64 GHz and the extinction ratio is about 30 dB. The phase response is linear as for its FIR features as shown in Fig. 11.4. In this simulation, we assumed L is about 2.98 cm, α is about 3 dB/cm, and a fixed coupling ratio of 0.5 considering the narrow wavelength range, which is in correspondence with practical devices. The results also indicate that as N increases, the FSR can be enlarged by 2^{N-1} times, while $\Delta\lambda_{3\text{dB}}$ almost does not change and the extinction ratio of the filter can also be significantly improved.

The proposed filter with three-stage cascaded MZIs is fabricated on an SOI wafer, considering the current fabrication tolerance, phase matching requirement, and the insertion loss as shown in Fig. 11.5a. The SOI platform used is based on a 220 nm thick silicon layer laid on top of a 2 μm buried-oxide layer by LETI foundry using 193 nm DUV lithography. The width and height of the etched silicon waveguide used in this filter is about 450 nm and 220 nm, respectively; meanwhile, the gap between the coupler waveguides is 200 nm and the coupling length is about 10 μm. The heaters and electrical contact pads, which consist of 110 nm Ti/TiN, are deposited on buried channel waveguides by means of a 600 nm thick silica layer grown on the structure.

Due to the limitation of the available SOI technology, the characteristics of the waveguide structure, for instance, the feather size and propagation loss, may not be identical to that of the designed ones, which would degrade the performance of the fabricated devices. Two methods can be employed to mitigate these limitations. First, gradually changed exposure and oxidation process could be adopted in the optimization procedure to compensate for the exposure dose variation and smooth the waveguide surface, respectively. Second, considering the inevitable technological fabrication tolerances, microheaters deposited on the isolation oxide layer are employed to tune the effective parameters of the device to modify the filtering response of the device.

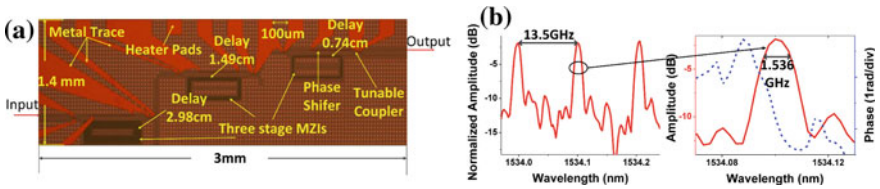

Fig. 11.5 Proposed optical processor with enhanced FSR. **a** Micrograph of the cascaded MZI filter. **b** Measured amplitude and phase of the filter

By independently tuning the microheaters deposited on the MZI arms, we can achieve phase matching between the different stages, and the amplitude and phase response of the device measured by an optical vector analyzer (OVA) as shown in Fig. 11.5b. The bandwidth of the filter is about 1.536 GHz and the FSR is enhanced to 13.5 GHz, which meets the requirement for a processing bandwidth from X- to Ka-band. Besides, the phase response is linear, which agrees well with the theoretical results. The extinction ratio of the measured results decreases a little, because of the fabrication error and mismatching between different MZI stages. Vertical coupling based on a grating coupler is used for coupling light from single mode fiber to the silicon waveguide with about a 10 dB coupling loss. Besides, the insertion loss of the filter itself is about 9 dB. Since the silicon waveguide and the coupling rate of the grating couplers are both polarization sensitive, a polarization controller (PC) has to be used to control the light polarization before the light is coupled into the chip.

11.2.1.2 Si_3N_4 FIR Signal Processor [22, 23]

Nowadays and for near future communication applications, the effective bandwidth of the signal is usually around 100 MHz [34, 35], even at a higher carrier frequency. There is a gap of approximately one order of magnitude between the resolutions of the proposed signal processors and the bandwidth of the desired signal, which are partially limited by the high waveguide loss of the SOI waveguide (approximately 3 dB/cm). The Si_3N_4 waveguide based on the TriPleX^{TM} waveguide technology possesses an ultralow waveguide loss of 0.1 dB/cm at the bend radius of 70 μm [36, 37], which shows the potential of designing longer waveguide delay lines and thus realizing high-resolution signal processors.

In this section, a seven zeros programmable analog signal processor based on the Si_3N_4 waveguide is proposed. The amplitude and the phase of the zeros can be tuned to achieve different shapes of response. The highest resolution and the processing range of the signal processor is less than 143 MHz and larger than 112.5 GHz, respectively, which would be suitable for multiband microwave signal processing.

A schematic diagram of the proposed all-optical analog signal processor is shown in Fig. 11.6. Two parts are contained in this signal processor system, the

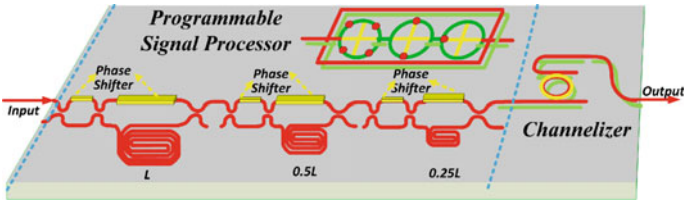

Fig. 11.6 Schematic diagram of the cascaded MZIs-based programmable signal processor

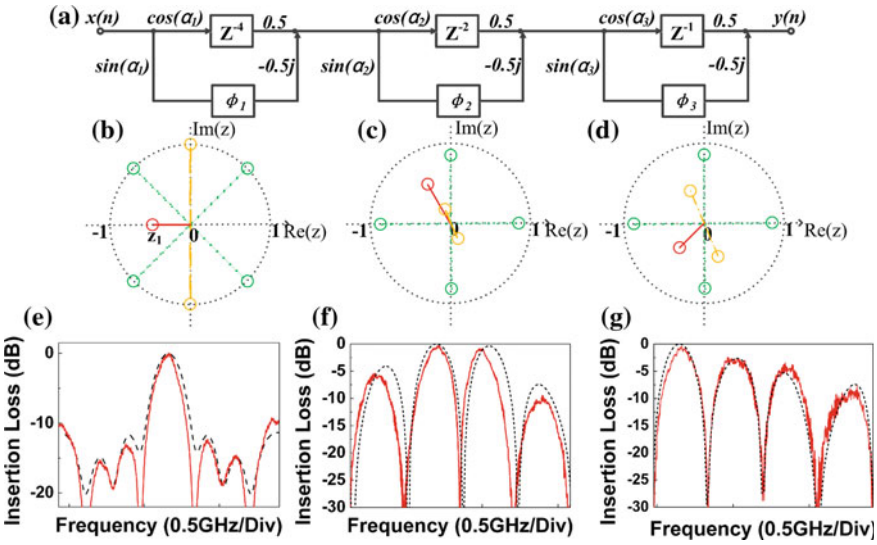

Fig. 11.7 **a** Direct form implementation of the 7-zeros FIR filter. $\cos(\alpha_i)$ and $\sin(\alpha_i)$ are the power distribution ratio to the two arms of the MZIs. Simulation results of the reconfigurable signal processor at different zeros distribution: (**b–d**), the different zeros distribution; (**e–g**), and the response of the signal processor relative to the zeros distribution in (**b–d**). The *solid red lines* are the experimentally measured response and the *dashed lines* are the simulated ones.

programmable signal processor and the channelized filter based on the ring resonator. Such a signal processor can be treated as a three-stage FIR filter. So in the direct form implementation, as shown in Fig. 11.7a, the first stage represents a four-zero structure and for the second and third stages, there are two zeros and one zero, respectively. As presented in Fig. 11.6, three tunable couplers based on symmetric MZIs are employed for the power division to the three-stage asymmetric MZIs. The division ratio that corresponds to $\cos(a_i)/\sin(a_i)$, is tuned by the phase shifter on top of the symmetric MZIs from nearly 0 to 1, which determines the amplitude of the zeros in each stage. The directional couplers in this device are all 1:1 couplers. By tuning the phase shifter on the asymmetric MZIs, the zeros of each stage MZIs would rotate around the unit circle. So with the tuning of the six-phase

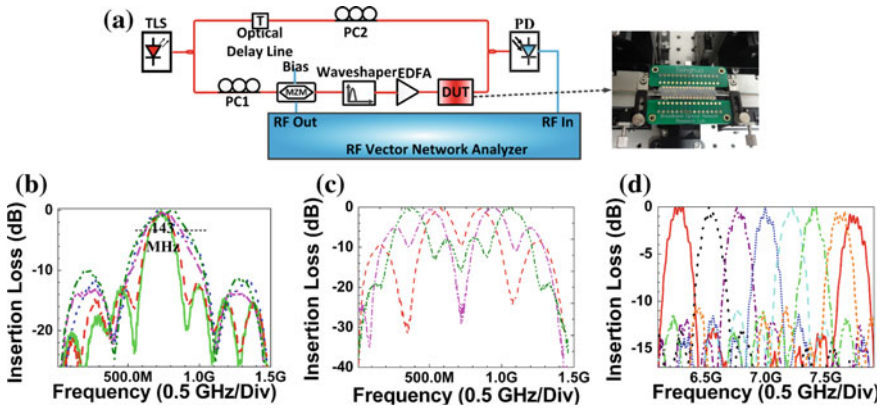

Fig. 11.8 Device measurement with VNA. **a** The setup of the VNA-based high-resolution optical vector network analyzer for measuring the performance of the high-resolution reconfigurable signal processor. At the *right side* is a picture showing packaging of the chip. The response of the programmable signal processor: **b** signal-band response with bandwidth variation from 143 to 300 MHz, **c** dual-band response with different separation, and **d** the center frequency variation of the single bandpass response

shifters in this structure, the zeros can be arranged in the zero-pole map and different shapes can be obtained as shown in Fig. 11.7b–g.

The proposed fully reconfigurable high-resolution FIR signal processor is fabricated by the Si_3N_4 technology as the picture of the packaged device shows in Fig. 11.8a. To achieve a FIR filter with a 3 dB bandwidth of around 100 MHz, the largest delay L in this structure is set to be as long as 50 cm, which would cause a loss difference between the two arms of the MZI. The tunable couplers are introduced to balance the power distribution to the unbalanced two arms of the MZI to optimize the filtering response.

As the resolution of the proposed cascaded MZIs-based bandpass filter is nearly 150 MHz, the OVA with a measuring resolution of nearly 150 MHz would not be able for measuring the response of the filter. So a tunable high-resolution optical network analyzer based on the RF vector network analyzer (VNA) is designed to measure the response of the filter, as presented in Fig. 11.8a. In this system, the output optical wave from a tunable laser source is separated into two paths with a 1:1 coupler. One is used as the optical local oscillator (LO) for down-converting, and the other is used as the optical carrier for upconverting the RF sweeping source from the VNA to optical domain via the Mach-Zehnder modulator (MZM) to be an optical sweeping source with the same sweeping resolution of the RF VNA. The zero-biased MZM is adopted to achieve the carrier-suppressed modulation of the RF sweeping source. In addition, considering the periodicity of the filter response, a single bandpass filter is introduced to filter out the positive modulated band and thus avoid the interference of the negative modulated sideband to produce the clean optical sweeping source. Then, the erbium-doped fiber amplifier (EDFA) is

introduced to amplify the optical sweeping source before being sent into the device-under-test (DUT). As the device is polarization sensitive, a PC is placed before the device to tune the polarization state and obtain the optimized coupling ratio. After that, the modulated bands are filtered by the proposed filter. Then the filtered signal is combined with the LO and detected by the photo-diode. Finally, the obtained RF signal is sent back to the RF VNA to obtain the visualized filtering response of the proposed filter. Because of the size mismatching between the waveguide and the optical fiber, the spot size convertors provided by the LioniX B. V. are utilized to lower the coupling loss.

By properly tuning the phase on one arm of the MZIs, various transfer responses with different shapes have been achieved. For example, in a single FSR, 1-passband, 2-passbands, and 4-passbands filters can be realized and the measured results agree well with the simulated results, as shown in Fig. 11.7e–g, when the zeros are distributed as presented in Fig. 11.7b–d. The device parameters are: $L = 0.5$ m, $n = 1.99$.

For the application of signal extraction, such as in wireless communications [34, 35], the single-passband and dual-passband filters have been realized as shown in Fig. 11.8b, c. The resolution of the filter can be altered from 143 MHz to more than 300 MHz by properly tuning the phase shifters on top of the MZIs as presented in Fig. 11.8b while the FSR of the filter is maintained to be approximately 1.466 GHz, which is enhanced by the scheme of cascaded MZIs. As one can see in Fig. 11.8c, for the dual-passband filter, the interval between the two passbands can be altered without changing the 3-dB bandwidth of the two passbands, by tuning the phase shifters on top of the filter. Besides, the center frequency of the filter can be swept with the temperature electric control (TEC) module, as shown in Fig. 11.8d. However, for such a signal processor based on MZIs, the processing range is usually limited. A channelized filter based on the ring resonator [29] is introduced to enlarge the processing range of the signal processor to a value approaching hundreds GHz, as presented in Fig. 11.9.

In summary, the FIR signal processors based on MZIs can achieve a high-processing resolution and also the shape of the filter can be optimized. The processing range of the FIR signal processors is usually limited, though the

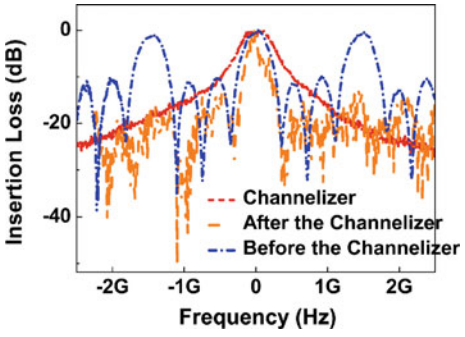

Fig. 11.9 The response of the single-band bandpass signal processor after the channelizer

cascaded scheme is employed to enlarge the FSR. The channelized filters are always required to enhance the processing range.

11.2.2 IIR Signal Processors

IIR signal processors based on microring resonators are attractive for the application in microwave photonic frontends, because of the compact size and the potential high Q and large enough FSR. Because of the high refractive index contrast between the silicon and the SiO_2, the minimum radius can be smaller than 5 μm, so that the FSR of the filter can be very large. By proper design of the radius and the coupling ratios between the rings and the waveguides, the high Q filter with a large processing range can be realized [26–28]. However, there is always a tradeoff between the waveguide loss and the effective refractive index, i.e., between the inherent Q and the minimum radius. For the SOI strip waveguide, the high index contrast results in the high confinement of the optical mode in the waveguide, a small minimum radius, and a large processing range, but the inherent Q of the ring resonator is limited by the high waveguide loss ($\sim$3 dB/cm). To lower the waveguide loss, rib-type waveguides are employed, but the radius of the ring resonators are usually larger than 1 mm, which would cause the FSR of the filter to be smaller than 25 GHz [24]. Then, the Si_3N_4 strip waveguide seems attractive to researchers because of its low waveguide loss (<0.1 dB/cm @ 70 μm radius) and high index contrast (Si_3N_4 = 1.99, SiO_2 = 1.45), which would be better for the high Q and large processing range design.

11.2.2.1 Si_3N_4 Microring IIR Filter [29]

To meet the requirement of the full-band (from L-band to W-band) RF signal processing in the RF photonic receiver, the parameters of the devices are designed as listed below; the radius of the ring is 125 μm, the gaps between the waveguides and the ring are 2 μm, so that the FSR can be larger than 220 GHz (the processing range of the filter is nearly half of the FSR) and the bandwidth of the filter can be as small as hundreds of MHz. The performance of the filter is measured by the OVA, as shown in Fig. 11.10a, and the processing range is larger than 110 GHz (FSR = 225.78 GHz). The processing band of the filter can be tuned for more than one FSR by the microheater on top of the microring, as presented in Fig. 11.10b.

As the resolution of the IIR signal processor is about hundreds MHz, the VNA-based measuring system is also utilized to measure the transfer response of the filter, as shown in Fig. 11.11a. The bandwidth is lower than 420 MHz and the out-of-band suppression ratio is larger than 40 dB, as presented in Fig. 11.11b. The shape of the filter would be maintained when the center frequency is altered, as given in Fig. 11.11c.

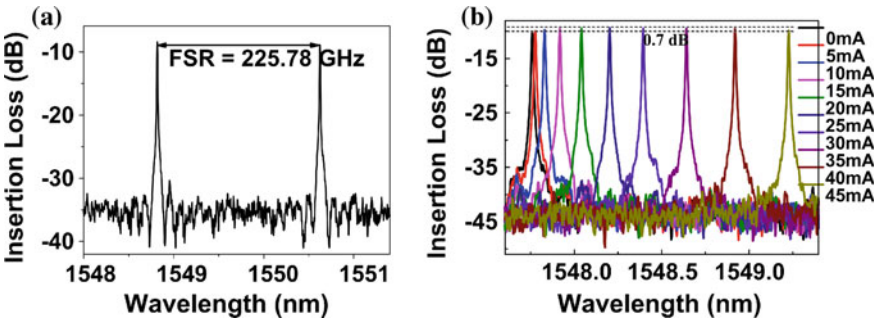

Fig. 11.10 Device measurement. **a** Transfer response of the filter measured by the OVA. **b** The thermal tuning response of the filter for more than 1 FSR

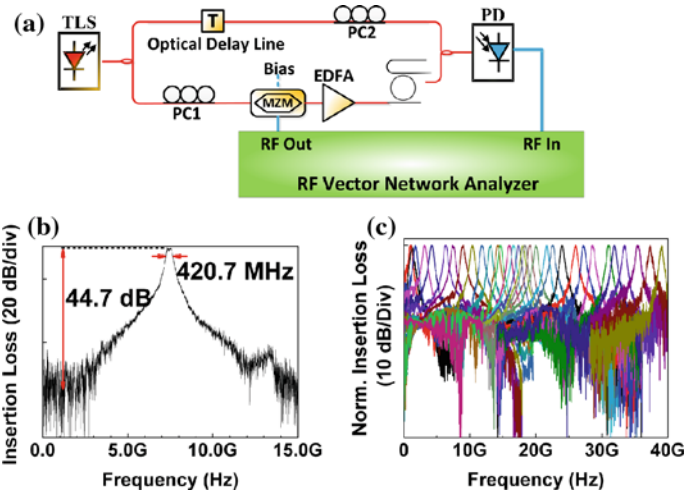

Fig. 11.11 Device measurement with VNA. **a** Schematic diagram of the used system for measuring the transfer response of the filter with VNA, **b** the transfer response of the filter measured by the system in (**a**), **c** thermal tuning response of the filter. The shape of the signal processor is almost maintained while the center frequency is changing

11.2.3 FIR/IIR Hybrid Signal Processors

The hybrid signal processors have potential for more flexible programmability as there are both zeros and poles in the filtering system [30–32]. In [30], the programmable signal processor with one zero and one pole is proposed by Telcordia's researchers. The bandwidth of the filter is nearly 1–2 GHz and it is likely to achieve a 200 MHz high resolution by cascading eight stages of the filtering units. In [6, 31], a potential method for the high-resolution signal processor based on the electromagnetically induced transparency (EIT)-like effect has been proposed,

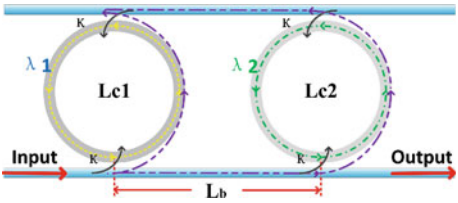

Fig. 11.12 Schematic diagram of the EIT-like effect-based Q-enhanced bandpass filter with two ring resonators

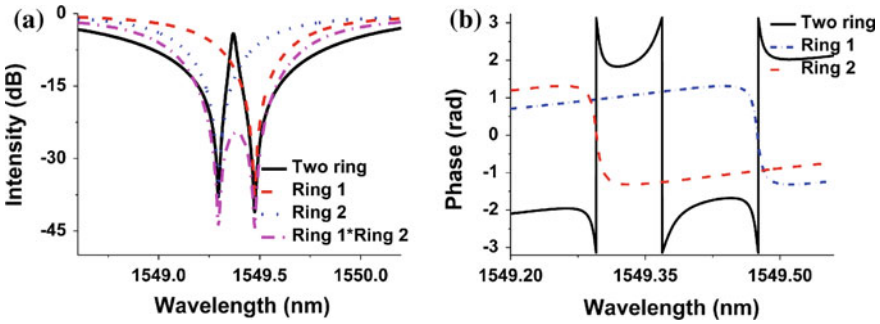

Fig. 11.13 Principle diagram of the EIT-like effect-based Q-enhanced bandpass filter. **a** Q-enhanced EIT-based filter compared with the product of two detuning rings. **b** Phase response of the proposed filter

where an enhancement of about 2–3 orders of magnitude in the Q-value relative to the single ring resonator would be achieved, theoretically. This would be a promising method to achieve an ultra-high Q integrated compact filter for critical applications.

The signal processor composed of two-ring resonators with slightly different resonance wavelengths as shown in Fig. 11.12. In this schematic diagram, three resonances exist, the two ring resonances and the Bragg resonance induced by the two rings. Generally, the three resonances presented are the same at the condition of $Lc_1 = Lc_2 = 2L_b$, where Lc_i is the circular path of the ith ring and L_b is the distance between the two rings. In this design, a slight detuning is introduced to the two rings, indicating $\lambda_1 \neq \lambda_2 \approx \lambda_3$, to utilize the EIT-like effect in the two-ring structure to achieve a Q-enhanced resonance, where $\lambda_{1,2}$ is the resonance wavelength of the first and second ring and λ_3 is the resonance wavelength of the Bragg wavelength. As the Bragg resonance is only formed by two stages, the Bragg resonance is weak relative to the ring resonances and serves as an envelope for the filtering response.

As there is a detuning between the two-ring resonances, the transfer response of the filter is shown as the black curve in Fig. 11.13a exhibits a narrow resonance tip in detuning with the notch band of the two-ring resonances accompanying a

resonance enhancement induced by the EIT-like effect, which is distinct from the product of the detuned two rings as shown in Fig. 11.13a. The phase response is shown in Fig. 11.13b. At the point of the resonance tip, the phases of ring1 and ring2 have equal magnitude and opposite sign, which changes the phase from destructive to constructive interference and indicates a resonance at this point to create the bandpass channel. There are destructive interferences between the two rings responses except of the tip point, for which the sideband suppression will be enlarged and the bandwidth will be narrowed with a Q-enhancement. In addition, by altering the detuning between the two rings, a bandwidth tunable filter can also be achieved [38].

The Q-enhancement of our proposed filter is inversely proportional to the waveguide loss and also to the full width at half maximum (FWHM). Usually, the waveguide loss is induced by the scattering of the rough sidewall of the waveguide and determined by the fabrication technology. For the adopted waveguide of 450 nm width and 220 nm height, the loss is about 3 dB/cm. However, many elaborate designs have been proposed to reduce the loss of the waveguide, e.g., Biberman et al. [24] proposed a rib waveguide with a loss of about 2.7 dB/m. As can be seen from Fig. 11.14a, by reducing the waveguide loss from 5 dB/cm to 0, the FWHM of the proposed filter is decreased to half, while there is only negligible change to the single ring passband. That is to say, the Q-enhancement compared to the single ring would be increased as the loss reduces, as shown in Fig. 11.14b. The parameters in this simulation in accordance with the devices fabricated are listed below. The detuning between the radii of the two rings is about 10 nm, the effective index is set as 2.82, and the coupling coefficients between two waveguides and rings are 0.6. With proper design, the Q-enhancement can be as high as 2–3 orders of magnitude. Utilizing this technology, if the Q of the single ring is high enough, there would be still an enhancement in Q-value. That is to say, this Q-enhanced

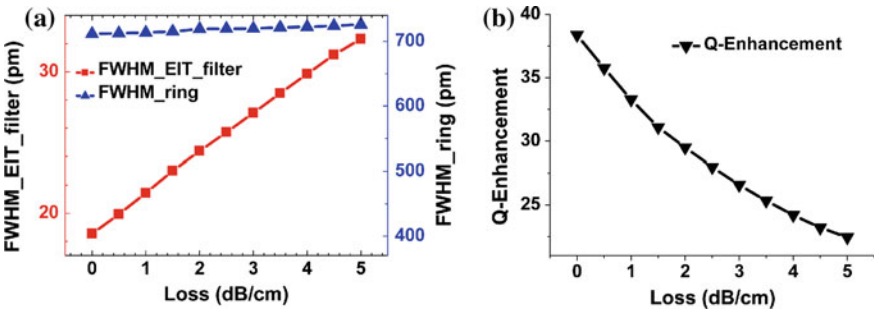

Fig. 11.14 The influence of waveguide loss on the FWHM and Q-enhancement. **a** The FWHMs of the EIT-based Q-enhanced filter and the single ring with different loss coefficients of the waveguides. **b** The Q-enhancement changes with waveguide loss

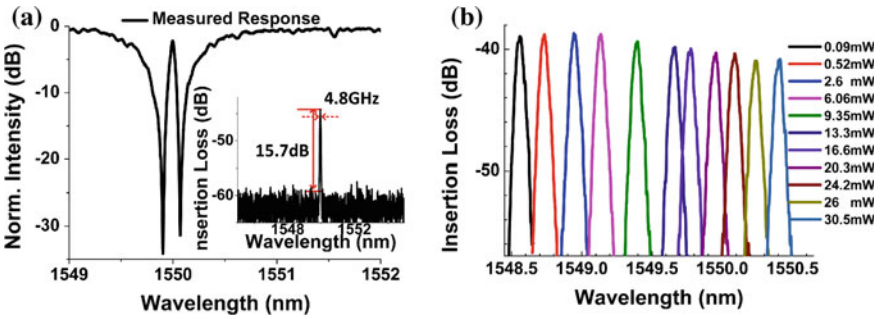

Fig. 11.15 The performance of the proposed *Q*-enhanced filter. **a** The measured *Q*-enhanced filter response we achieved. The *inset* is the response after a channelizer. **b** The passband of the proposed filter shifted with different dissipation input electrical power

EIT-like effect-based filter will be a potential way to achieve an ultra-high *Q* bandpass filter.

As the resonance tip is near the notch bands, the *Q*-enhancement will be larger at the critical condition of the rings with the deepest notch. The filter proposed here contains two coupling waveguides with symmetrical coupling rates, which can approximate the critical condition at a waveguide loss of about 3 dB/cm. At this condition, the depth of the notch reached nearly −30 dB. The coupling ratio between the waveguide and ring of our designed filter is about 0.6, which is too high to get a high *Q* in the single ring resonator bandpass filter, while for our proposed filter, an enhancement in *Q* would be achieved due to the EIT-like effect discussed above.

The performance of the proposed *Q*-enhanced filter is shown in Fig. 11.15. The bandwidth of the filter is about 4.8 GHz and the sideband suppression ratio is about 15.7 dB, which is limited by the noise floor of the OVA as shown in Fig. 11.15a. The *Q* of the single ring at this proposed condition is only 1409, while the *Q* of the proposed filter can be as high as 38,750, thus, the enhancement in *Q* is about 27, which agrees well with the simulation result.

When the proposed filter is used for the application in the microwave photonics, the sideband of the filter should be suppressed. A programmable optical filter (Finisar WaveShaper1000S) with a 3 dB bandwidth of 20 GHz can be used as the channelizer to suppress the sideband of the filter. The channelized filter can be fabricated by the SOI technology, and likely be integrated with the bandpass filter in the down-conversion analog photonics link [28]. Meanwhile, we can use a semiconductor cooler to realize the tunability of the center wavelength of the filter, as shown in Fig. 11.15b. The increased insertion loss of the proposed filter relative to the passband of the single ring is about 6 dB, and an extra nearly 3 dB of loss is introduced by the channelizer.

11.3 Silicon Photonics-Based Photonic Frontends

Several microwave photonic frontends have been proposed, based on the down-conversion and filtering [1–11]. As far as we know, although the silicon-based microwave photonics signal processing technique is regarded as a promising solution to the challenges in the complex photonic frontends, especially in terms of cost, power consumption, and reliability, most recent efforts have focused on silicon-based device function or subsystem performance while only a few reports focus on the applications of these devices in the frontends. Some microwave photonic frontends based on silicon photonics signal processors are described in this section.

11.3.1 Parallel Down-Conversion Frontends [29]

The schematic diagram of the full-band RF photonic receiver is shown in Fig. 11.16. A continuous wave laser (CWL) operating in the optical communication wavelength band (1550 nm) is adopted as the optical carrier. The RF LO is upconverted to the optical domain by a null-biased MZM to achieve a carrier-suppressed modulation. The received RF input signal is applied to a phase modulator for signal upconverting. As the electrooptic (EO) modulators are polarization sensitive, two PCs are placed before the modulators to adjust the polarization states of input signals to have the optimized modulation efficiency. Before being sent into the signal processor, the modulated signal would be amplified by the EDFA to compensate the optical loss through the system. Then the signal is sent into the proposed Si_3N_4 microring-based bandpass filter for signal extracting. The target signal extracted by the proposed high-resolution filter would be combined with the optical LO in the upper branch via a 3 dB coupler and detected by the balanced-photo-diode (BPD) for down-converting. The down-converted signal would be monitored by the electrical

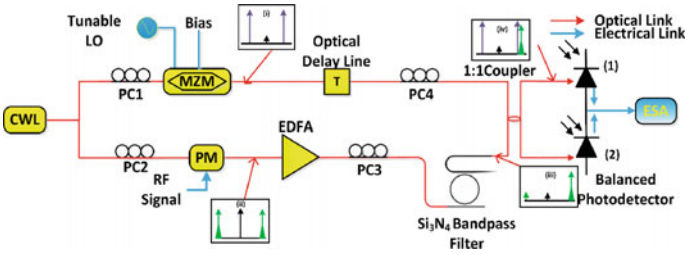

Fig. 11.16 Schematic diagram of the RF photonic receiver. The LO signal is null-biased modulated to the MZM to realize the carrier-suppressed modulation to maximize the power in the modulated sidebands and minimize the carrier contribution to detector shot noise. The desired signal is extracted by the proposed full-band microring-based signal processor. The BPD used in this system can suppress the even-order nonlinear signal and provide additional gain

spectrum analyzer (ESA) or the oscilloscope. In this system, the RF LO is carrier-suppressed modulated onto optical domain to maximize the power in the modulated sidebands and minimize the carrier contribution to the shot noise in detector. Thanks to the high performance of the signal processing in the optical domain, the desired signal would be extracted clearly without any other interference sidebands, which would suppress the nonlinear sideband and improve the spurious free dynamic range (SFDR). The BPD employed in this system is used to provide additional gain and suppress the common-mode noise.

The parameters of the system are listed below. The center frequency and the optical power of the CWL are 1549.407 nm and 16.7 dBm, respectively; the bandwidth of the MZM is 40 GHz, the gain of the EDFA is 20 dBm and the power after the EDFA is 17 dBm. The bandwidth and the half-wave voltage of the phase modulator (PM) are, respectively, 40 GHz and 7 V.

In order to investigate the performance of the RF photonic receiver and the features of the proposed high-resolution optical filter, the receiver performance working within the frequency range from L- to Ka-band (limited by the bandwidth of modulator used in our experiment) has been measured. The power of the RF LO is 20 dBm, and the carrier-suppression ratio of the corresponding null-biased MZM is larger than 20 dB. The two-tone test signals ranging from L-band to Ka-band are injected into the PM. By carefully tuning the microheater on top of the microring, the center frequency of the filter could be altered continuously to select the desired first-order modulated band signal perfectly for down-converting, due the high resolution of the optical filter.

To evaluate the linearity of the receiving system, the SFDRs at the frequency ranging from L- to Ka-band have been measured. The experimental results are discussed below. The signals filtered by the proposed filter are detected by the BPD. Due to the nonlinearity of the system caused by the phase modulation and the photodetection process, not only the down-converted signal at 6.5 and 8.5 MHz, but also the third-order intermodulation distortion (IMD3) at 4.5 and 10.5 MHz are obtained after BPD. The SFDRs of the receiver in C- to K-band have been measured and are plotted in Fig. 11.17a–d (setup of the ESA: RBW = 1 kHz, VBW = 1 kHz, AT = 30 dBm, ST = 720 ms). The measured noise floor is about −151 dBm/Hz. The SFDR of C-band (Signal: 4.8065 and 4.8085 GHz, IF: 6.5 and 8.5 MHz), X-band (Signal: 10.0065 and 10.0085 GHz, IF: 6.5 and 8.5 MHz), Ku-band (Signal: 13.5065 and 13.5085 GHz, IF: 6.5 and 8.5 MHz) and K-band (Signal: 19.0065 and 19.0085 GHz, IF: 6.5 and 8.5 MHz) are respectively 118.6 dB-$Hz^{2/3}$, 116.0 dB-$Hz^{2/3}$, 114.8 dB-$Hz^{2/3}$, 119.1 dB-$Hz^{2/3}$.

The SFDRs of the system with the frequency ranging from 1.5 to 39.5 GHz with a 2-GHz step have also been measured and are presented in Fig. 11.18. In such a frequency range (the largest range that can be realized in our experiment), the system has a good uniformity. It is also predictable that the system would perform well while operating in the higher frequency band, because of the same principle.

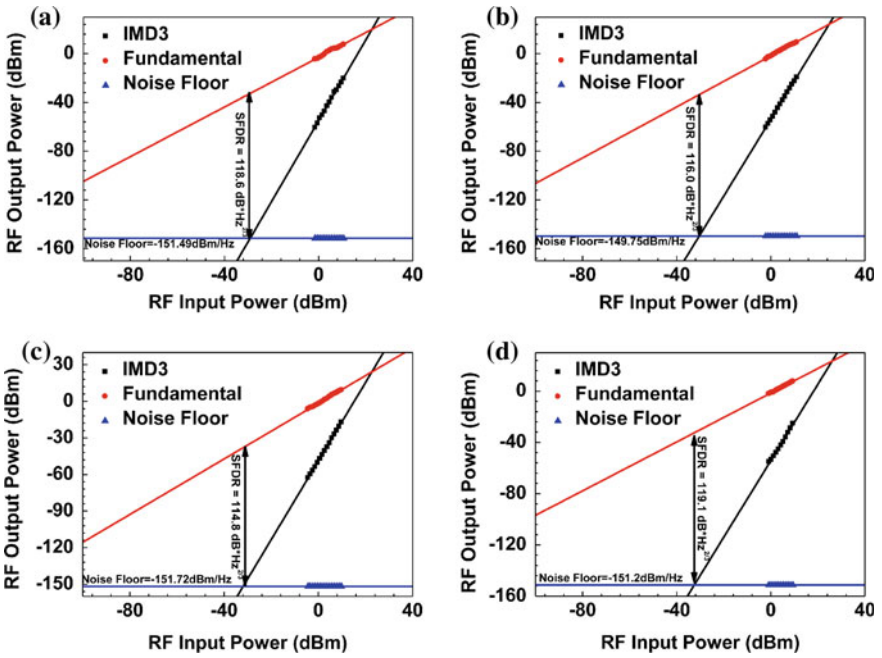

Fig. 11.17 Experiment results. The SFDR of the RF photonic receiver from C- to K-band measured with two-tone test signals. **a** C-band, **b** X-band, **c** Ku-band, **d** K-band

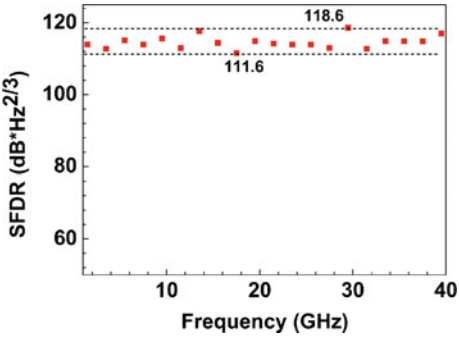

Fig. 11.18 SFDR from L- to Ka-band. The SFDR of the RF photonic receiver from L- to Ka-band measured with two-tone test signals

11.3.2 OEO Frontends

As has been discussed above, typical microwave systems incorporate a modulator for mixing, RF oscillator, signal processor, and down-converter in the RF photonic frontends area, as shown in Fig. 11.19. For most of the RF photonic frontends reported, the photonic tunable down-conversion is realized by tunable LOs [39]. The LOs can be realized by several methods, such as adding one more modulator

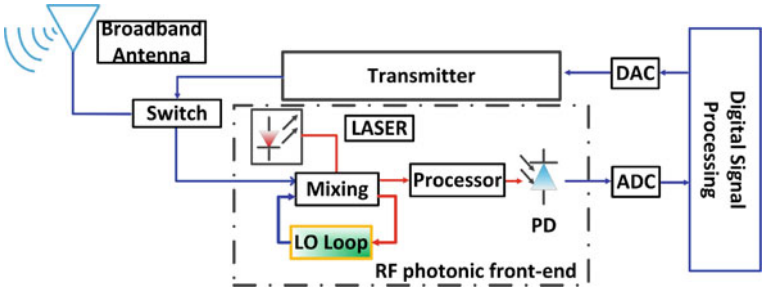

Fig. 11.19 Notional diagram of a simplex radar system consisting of a digital-to-analog converter (DAC), analog-to-digital converter (ADC), transmitter and the proposed RF photonic frontend. The proposed RF photonic frontend contains the mixing process with a feedback loop to generate the LO, a signal processor and the PD-based down-converter

and a microwave source to generate the LO [40] or directly introducing another tunable laser [41] to serve as the LO for mixing. The OEO with a large frequency range and ultralow phase noise can be employed as the LO for mixing in the frontend to achieve a large processing range and fast tunability, which can convert the energy from continuous wave light to the microwave or even millimeter wave signals [42, 43]. To avoid the impact on the oscillation of the OEO, some methods have been proposed, such as utilizing the polarization splitter to divide the RF signal and the LO at different polarization states [44] or employing some more modulators to upconvert the RF signal to a unique wavelength band and filtering out the RF input signal with a wavelength filter in the OEO loop [45]. In [46], taking advantage of the characteristics of the PM-based microwave photonic filter (MPF) in the OEO [43], the signal and LO would be isolated after the photodetector (PD), as the signal is out of the passband of the MPF.

In this section, a large processing range photonic frontend based on the OEO is described, in which the characteristic of the PM has been made full use of to integrate the LO to the upconversion system with the same PM. The processing range of the RF photonic frontend can cover the X- to Ka-band thanks to the large frequency range of the OEO-based LO and the processing ability of the SOI-based signal processor. This proposed RF photonic frontend would be a promising design for monolithic chip integration of the frontends [47].

The schematic diagram of the proposed RF photonic frontend integration with the OEO-based LO is shown in Fig. 11.20a. The RF signal received by the broadband antenna is upconverted to the optical domain by a PM and processed by the tunable bandpass filter (TBPF2) and then mixed and down-converted to get the RF output signal, which can be applied for post-processing as in the blue-dashed frame shown in Fig. 11.20a. There are two TBPFs in the whole RF photonic frontend: the broad bandwidth one (TBPF1) is applied for the LO loop and the narrow bandwidth one (TBPF2) serves as the signal processor for photonic-based microwave signal processing. These two TBPFs in this frontend could be controlled by the control signal given by the post-processing module. The PM for

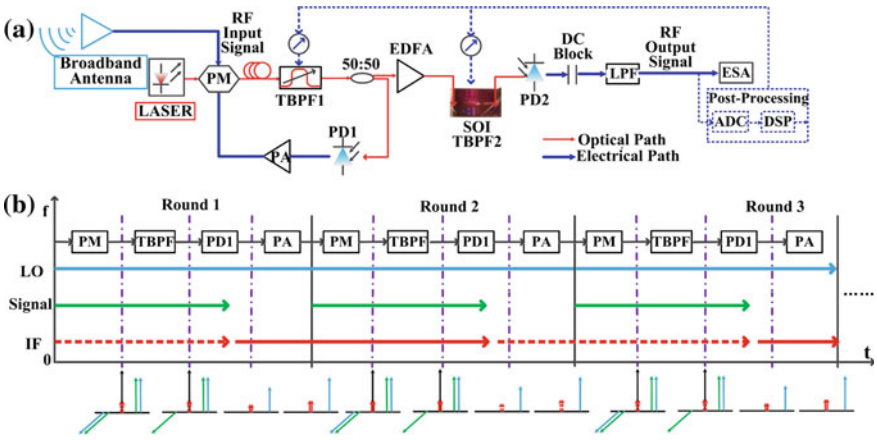

Fig. 11.20 **a** Schematic diagram of the simple photonic frontend integration with the OEO-based LO for mixing and signal processor, **b** three rounds of the OEO loop. The switch between the *dashed* and the *solid arrow line* of IF means the new component is generated and the old is vanished

upconversion is also utilized to construct the OEO-based LO, which contains TBPF1, PD1 and the power amplifier (PA) as well [43]. The principle of the proposed RF photonic frontend integration with the OEO-based LO using a single modulator will be explained below by means of Fig. 11.20b.

A CWL is used as the optical carrier and modulated by the combined RF input signal and the OEO-based LO with the frequency of f_s and f_{LO}, respectively. The modulated signal is then filtered by TBPF1, whose center is set subtly to make sure all the first-order sidebands of the modulated RF input signal are selected by the filter with a bandwidth of about Bw and only either the −1 or +1 order of the LO modulated signal would exist after the filter with a frequency relationship of $f_s < Bw/2$, $f_s < f_{LO}$ and $f_{LO} \approx Bw/2$, as shown in Fig. 11.20b. The filtered signal is separated into two parts by a 3 dB coupler. One way is for high-resolution photonic signal processing and the other way is sent back to the LO loop and detected by PD1. After PD1, mainly two frequency components would exist as shown in Fig. 11.20b: the new generated intermediate frequency (IF) signal with a frequency of $(f_{LO}–f_s)$ and the LO as presented in Round1. The RF input signal is nearly vanished after PD1 as the beat frequency signal between the ±1 order of the RF input phase-modulated signal and the optical carrier have the same frequency and amplitude but a π phase difference. If the beat frequency $(f_{LO}–f_s)$ signal should exist all along since then and be amplified by the PA, there would be a bad impact on the LO, but fortunately, after the modulation and PD1 during Round2, the beat frequency $(f_{LO}–f_s)$ signal would be vanished for the same reason as the RF input signal as shown in Round2 and also Round3. The characteristics of the PM have been made full use of in this RF photonic frontend to eliminate the impact of the RF input signal and the beat frequency $(f_{LO}–f_s)$ signal on the OEO-based LO. So only

one modulator is required in the proposed OEO-based RF photonic frontend for both the upconverting process and OEO loop, without any impact on the oscillation of the OEO.

A stable LO is then achieved for mixing. The mixing signal of the LO and RF input signal is processed by the narrow bandwidth bandpass filter (TBPF2) and down-converted into the electric-domain by the PD2 to achieve the RF output signal. The direct current (DC) block and low-pass filter are introduced to remove the DC component and high-frequency component such as the LO and RF signal. The frequency of the LO can be tuned to achieve a large frequency range, which is determined by the bandwidth tunability of the TBPF1 and limited by the response bandwidth of the PM and PD1 [43].

In the experiment, a CWL with 1550.024 nm wavelength, 1 kHz line width and 23.2 mW optical power is sent into the PM with a modulated bandwidth and half-wave voltage of 40 GHz and 7 V, respectively, and then modulated by the combined two-tone signal and the OEO-based LO. A wave-shaper (Finisar 1000s) with a tunable bandwidth is utilized as the TBPF1, and the PD1 with a bandwidth of 10 GHz is applied to detect and down-convert the signal. Two-stage PAs are used to make the gain of the OEO-based LO loop larger than 1 to obtain and keep the LO.

An EDFA with a gain of about 20 dB is placed before the SOI three-stage cascaded MZIs-based signal processor to overcome the loss of the processing link. The bandwidth of the SOI filter-based signal processor is about 1.536 GHz and the performance is analyzed in Sect. 11.2.1.1. The silicon-based narrow bandwidth bandpass filter is used to filter out the desired part of the mixing signal for down-converting. The processed signal is then detected by PD2 with a bandwidth of 40 GHz and responsivity of 0.62 W/A. The RF output signal is filtered by a DC block and a LPF to remove the DC component and the higher frequency component. The signal is measured by the ESA.

The tunability of the LO with three different frequencies is measured by tuning the bandwidth of the TBPF1 as shown in Fig. 11.21a. The smallest bandwidth ($Bw_{\min}$) of TBPF1 and the bandwidth of the PD are all 10 GHz. Accordingly, the LO frequency cannot be lower than $Bw_{\min}/2 = 5$ GHz or larger than 10 GHz in this experiment. A single mode fiber with a length of about 200 m is introduced into the LO loop to obtain the delay and suppress the phase noise of the LO. As shown in Fig. 11.21b, the phase noise (measured by an Agilent E5052B) at an offset of 10 kHz relative to the center frequency of the oscillation of the OEO are all below −102.5 dBc/Hz.

To investigate the performance of the RF photonic frontend integrated with an OEO-based LO and the SOI-based signal processor, a two-tone signal centered at a frequency of 7.02 GHz with a separation of about 10 MHz and generated by an Agilent 8267D is injected to the PM. The bandwidth of the TBPF1 used in this experiment is 15 GHz and the center frequency is set properly to be near the carrier to get a LO at 7.227 GHz. The experimental result of the RF photonic frontend is also measured, as shown in Fig. 11.22. The down-converted signal measured by the ESA is shown in Fig. 11.22a. The SFDR of the frontend is measured to be

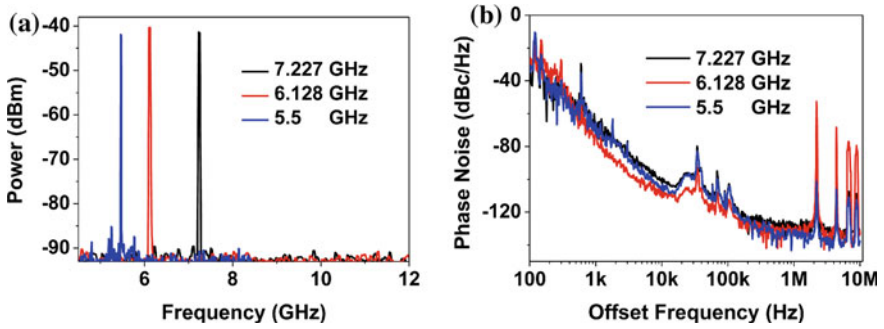

Fig. 11.21 **a** The electric spectrum of the OEO-based LO **b** the phase noise of the LO at frequencies of 5.5, 6.128 and 7.227 GHz

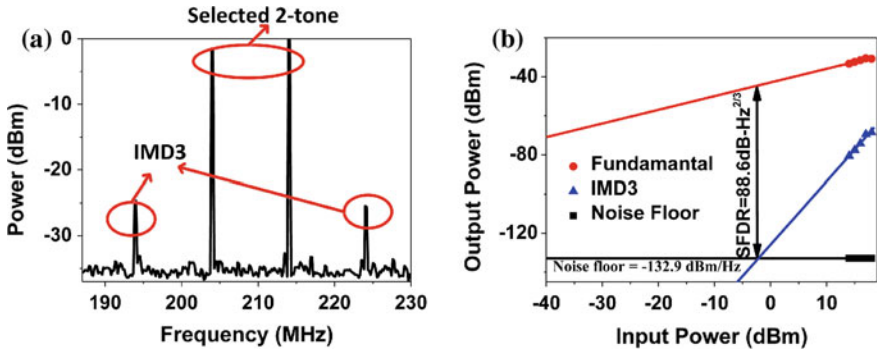

Fig. 11.22 Experimental results of the proposed RF photonic frontend integration with the LO at a frequency of about 7.227 GHz. The two-tone signal is centered at 7.02 GHz with a separation of about 10 MHz. **a** electrical spectrum of down-converted IF signal, **b** the measured SFDR

88.6 dB-Hz$^{2/3}$ which is not so desirable, with a noise floor of about −132.9 dBm/Hz, as shown in Fig. 11.22b. There are three reasons mainly for the low SFDR: first, the high noise floor due to the ASE noise from the EDFA which has been discussed in [6, 7]; second, the low link gain which is mainly because of the large loss of the microwave cables, the maximum optical power of the carrier limited by the low input optical power of the PD and the low responsivity of PD; third, the intrinsic drawbacks in linearity induced by the commercial modulator as described in [48]. These limitations can be overcome by adopting a high-performance PD, a low noise PA, low loss microwave cables, and a new domain-inversion directional coupler modulator [48].

For practical applications, the separation between the received RF signal and the LO cannot be too small and the input power of the RF signal is also limited. Figure 11.23 shows the application condition on Δf, the separation between the RF signal and the LO, and the input RF power. As can be seen from Fig. 11.23, there is

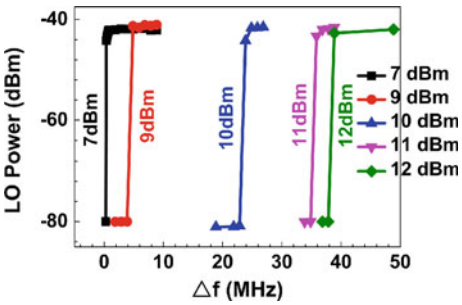

Fig. 11.23 The operation frequency range of the RF input signal at different input power in the proposed RF photonic frontend

a step response of the LO output power relative to the separation at different input RF powers. At a certain input RF power, the LO output power is not changed as the separation is decreased, until a critical point is reached, where the LO output vanishes. As the RF input power increases, the critical point of the separation would be enlarged as shown in Fig. 11.23. So there should be a tradeoff between the RF input power and the separation. Fortunately, the separation can be tuned by tuning the frequency of the LO and the RF input power received by the antenna is not that large. The influence of the low energy signal received by the antenna on the LO can be negligible.

In summary, different kinds of silicon-based microwave photonics frontends have been proposed in the past years and all possess advantages and disadvantages for unique applications. The parallel scheme is suitable for the multiband applications. Furthermore, since the system of the OEO-based frontend is simple, it would be suitable for entire system integration.

11.4 Photonic-Assisted SDR Transceiver

The SDR transceiver was first coined in the 1990s, and has received enormous attention worldwide as the next evolutionary stage for wireless technology [49–51]. Because of the software programmability, an SDR transceiver system is capable of supporting multiple protocols and frequency bands while minimizing the hardware components, which is a promising solution for introducing new technologies and services into existing live networks. Furthermore, the high accuracy offered by the digital signal processor in the SDR system provides reliable services for users. However, due to the bandwidth limitation of the hardware, SDR transceivers can only work up to the C-band (~6 GHz). To process signals more effectively and efficiently with regard to various requirements, the bandwidth of the transceiver must be greatly enhanced.

In the last few years, RF photonic techniques [14, 52–57] have emerged and received significant attention due to their advantages such as large processing bandwidth, and high tunability and flexibility, which could be applied to build photonic SDR transceivers for extending the frequency bandwidth. Even at present, photonic ADC and photonic-assisted RF frontend [54–57] seem to be the most promising methods for use in photonic SDR transceivers. Photonic ADC could achieve orders-of-magnitude improvement in accurate digitization of high-speed RF signals by optical sampling of the signal with ultrashort optical pulse trains, which are available from mode-locked lasers [54]. Based on this method, a fully photonic-based coherent radar system with outstanding performance has been demonstrated [56, 57]. However, limited by the aperture jitter, there would be a tradeoff between the achieved processing bandwidth and the effective number of bits (ENOB) in this kind of schemes. As an alternative, a photonic-assisted RF frontend could be used to significantly reduce the bandwidth requirements for electronic digital signal processing [7, 57]. The solution is to process the original incoming RF signal in the optical domain, before converting it to a lower IF signal. Thus, the bandwidth limitation of the electronic hardware could be inherently avoided. However, as the bandwidth of the passband signal that is to proceed is restricted by the available ADC, the required optical processing needs to be extremely precise [30]. Besides, given that the optical carrier center is at about 200 THz, the wavelength shift of the optical carrier cannot be neglected, which would continue to stress the accuracy capabilities of optical processing technologies. Moreover, the photonic SDR transceiver, using either the photonic ADC or the photonic-assisted RF frontend, could hardly meet the requirement of precise reconfiguration due to the corresponding limitation of optical processing.

In this section, a novel SDR transceiver using combined electronic and optical processing in both the transmitter and receiver is described and the microwave photonic processor discussed in previous sections is employed in the transceiver as the key signal processing element [58].

The schematic diagram of the system is illustrated in Fig. 11.24. Besides the digital signal processing, the electronic part also implements the baseband-IF conversion using a variable LO synthesizer. This way, it is able to process signals of up to 6 GHz. The additional IF-RF conversion is then accomplished with a single CWL in the photonic-assisted stage to largely extend the frequency range of the system. Due to the combined electronic and optical designs, the optical processing in this scheme is not required to be that precise. Instead, we could flexibly select a passband signal with the bandwidth of several gigahertz at an arbitrary frequency in the photonic-assisted RF frontend stage, and accomplish the following IF processing with high refinement as well as the software programmability prior to the narrow band ADC.

The details of the photonic-assisted SDR transceiver are shown in Fig. 11.25a, where the electronic part is depicted on the left and the photonic part is on the right. Both of them are somewhat symmetric in architecture. Additionally, the actual demonstrator unit is shown in Fig. 11.26. Considering that the electronic part could be accomplished with a commercial electronic SDR transceiver module, we will focus on describing the photonic structure in this section.

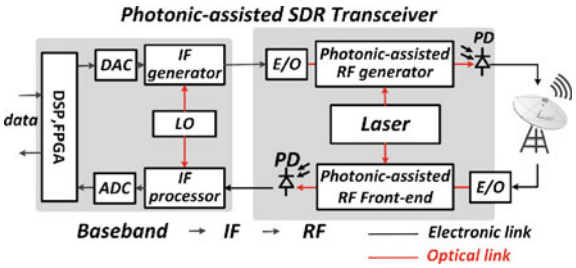

Fig. 11.24 The schematic diagram of the photonic-assisted SDR transceiver

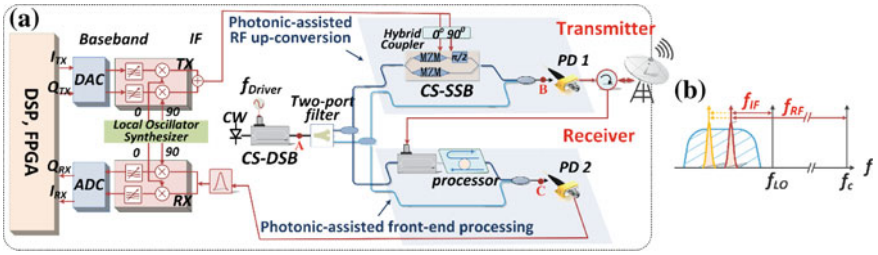

Fig. 11.25 **a** The experimental setup of the photonic-assisted SDR. *CS-DSB* Carrier-suppressed double-sideband, *CS-SSB* carrier-suppressed single-sideband; **b** the schematic diagram of the two-stage processing in the receiver

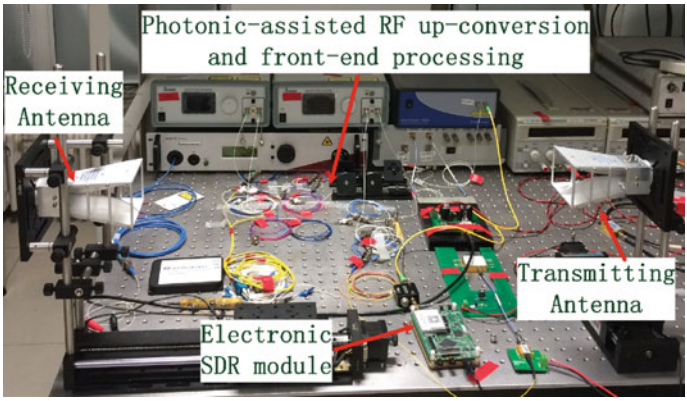

Fig. 11.26 A photograph of the demonstrator unit

As shown in Fig. 11.25a, we used the same optical carrier and LO, which are provided by a single CWL and separately centered at f_C and f_{LO}, in both the photonic RF carrier upconversion and the photonic frontend processing.

The two optical waves are simultaneously acquired from external intensity modulation under a carrier-suppressed double-sideband (CS-DSB) condition, and they are subsequently separated by a two-port optical filter. Due to the intrinsic phase-locking condition of the modulated sidebands, the beating phase noise in the following heterodyne process could be greatly suppressed. Moreover, the flexible tuning of the RF driver ensures the wide band flexibility of the transceiver, where an Δf_D change of the RF driver could lead to a $2\Delta f_D$ change of the RF carrier.

In the transmitter, the digital I/Q data stream is upconverted to analog IF signals by passing it through the electronic SDR module. Although the IF carrier of f_{IF} could be tuned with a variable LO synthesizer, the tuning capacity is limited. To upconvert the carrier to tens of gigahertz, we modulate the obtained IF signal onto the optical carrier, then the modulated sideband could arrive at the photodetector together with the optical LO from another branch. This way, RF carriers with tunable center frequency f_{RF}, which is equal to $f_{\mathrm{IF}} + 2f_D$, could finally be flexibly produced in the output of the photodetector. Note that it has the potential to cover the full RF bands. Moreover, because we employ a carrier-suppressed single-sideband modulation (CS-SSB) to acquire one pure modulated sideband, no additional filters are needed for this transmitter.

In the receiver, RF signals received through the antenna are modulated onto the optical domain to accomplish the optical filtering and down-conversion first. As the employed carrier and LO signals are the same as those of the transmitter, the produced IF tone is centered at the frequency of f_{IF}. The obtained signals would then experience another stage of processing implemented by the electronic SDR transceiver module. The schematic diagram of the two-stage processing in the receiver is depicted in the Fig. 11.25b. The employed optical filter, whose passband is shown as the blue oblique line Fig. 11.25b, no longer needs to directly handle the extremely narrow band RF signals. Instead, it is mainly designed to perform the preprocessing before the RF-IF down-conversion. Thus, the frequency bandwidth of the optical filter could reach the same order of magnitude as f_{IF}, which would also improve the tolerance for the general wavelength shift of the optical waves. The possible passbands in the following electronic IF processing are expressed by the red and orange lines in Fig. 11.25b. Compared with the first-stage optical processing, the second-stage electronic processing is much more precise. Using a low loss double-stripe waveguide, we proposed a Si_3N_4 microring optical filter with high resolution and high out-of-band rejection. The center frequency of the filter passband could be widely and flexibly altered via tuning the phase shifter on top of the ring. In addition, a commercial electronic SDR transceiver provides a mature solution for building the IF processor. This way, the receiver in this proposed scheme could be completed more efficiently.

Experiments were conducted to verify the concept of the proposed photonic-assisted SDR transceiver. As shown in Fig. 11.26, we used a commercial SDR transceiver module, HackRF One, which integrated the electronic components used in this architecture and is specifically designed for 10 MHz–6 GHz wireless signals, to accomplish the electronic functions. In addition, in the photonic-assisted stage, a continuous laser source of 1549.81 nm wavelength, 1-kHz line width, and

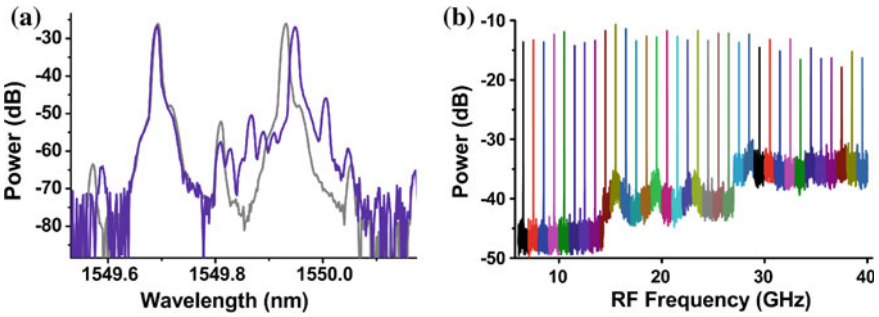

Fig. 11.27 **a** The measured optical spectra in observation points A (*gray*) and B (*violet*) of Fig. 11.25a when the driving frequency is set at 15 GHz and the IF carrier frequency is at 2.5 GHz; **b** the obtained RF carriers range from 6.5 to 39.5 GHz with a 1-GHz step when the driving frequency is tuned from 2 to 17.5 GHz

18-dBm optical power was sent to a 20-GHz null-biased MZM for generating the optical carrier and LO signals. An interleaver with a channel spacing of 25 GHz was then used to separate these two waves.

We tested the transmitter and show the results in Fig. 11.27. Due to the half-duplex characteristic of the LO synthesizer used in the electronic SDR module, we additionally incorporated an arbitrary waveform generator to create the IF signal. Besides, the CS-SSB modulation in the photonic-assisted stage for pure upconversion could be realized by an I/Q modulator with a 12.5-GHz bandwidth combined with a 90° hybrid coupler. We compared the optical spectrum before the photodetector (violet) with the generated optical LO and carrier (gray) in Fig. 11.27a, where the IF carrier frequency f_{IF} is 2.5 GHz and the driving frequency f_D is 15 GHz. The CS-SSB modulation with the suppression ratio exceeding 25 dB ensures the interference suppression. In addition, the 2.5-GHz shifting from the optical carrier to the modulated sideband finally leads to the 32.5-GHz detuning between the two beating waves. We could tune the driving frequency from 2 to 17.5 GHz to test the bandwidth and flexibility of the proposed transmitter. Figure 11.27b shows the obtained RF carrier ranging from 6.5 to 39.5 GHz with 1-GHz steps, where different colors represent different frequencies. The measured increasing noise floor is mainly due to the noise characteristic of the electrical spectrum analyzer, and the decrease of the optical upconversion efficiency with increasing frequency can be ascribed to the frequency response of the employed interleaver, photodetector, and the modulator. These results show that the transmitter is able to upconvert RF carriers up to 40 GHz, limited by the employed photodetector with a bandwidth of 40 GHz. This way, this scheme has the potential to cover the full RF bands if a state-of-art broadband photodetector is adopted.

The transfer response of the microring optical filter used in the receiver is discussed in Sect. 11.2.2. Because of the 420-MHz narrow 3-dB bandwidth and more than 40-dB high out-of-band rejection of the filter, most of the undesired signals could be successfully eliminated in the photonic down-conversion to the IF

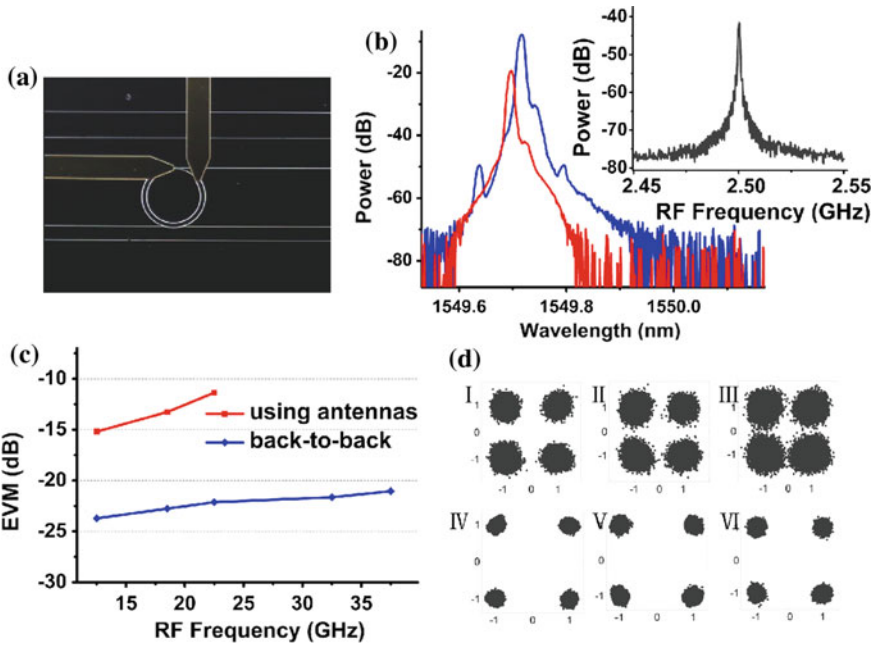

Fig. 11.28 **a** A photograph of the filter with a microheater on top of it (*right-top*); **b** the optical spectra of the modulated sideband (*red line*) and the LO signal (*blue line*) in the receiver, and the electrical spectrum of the corresponding IF signal (*right-top*); **c** the measured EVM curves versus the received RF carrier with 1-m antenna-to-antenna transmission (in *red line*) and with back-to-back connection (in *blue line*); **d** the obtained scatter plots for the RF input at 12.5 GHz (*I*), 18.5 GHz (*II*), 22.5 GHz (*III*) with 1-m antenna-to-antenna transmission, and the obtained scatter plots for the RF input at 22.5 GHz (*IV*), 32.5 GHz (*V*), 37.5 GHz (*VI*) in the back-to-back case

frequency at 2.5 GHz. The residual interference would be avoided in the next electronic stage and the bandwidth redundancy of the optical filter could reduce the impact from the wavelength shift of the optical carrier. Furthermore, by tuning the phase shifter on top of the ring, depicted in the photograph of the Si_3N_4 microring filter in Fig. 11.28a, the center frequency of the passband could be altered widely and flexibly in more than a 110 GHz frequency band.

We tested the receiver and show the results in Fig. 11.28b–d. The optical spectra of the modulated sideband (red line) and the LO signal (blue line) are depicted in Fig. 11.28b. Due to the employment of the same carrier and LO between the transmitter and the receiver, the obtained IF signal after the photodetector is centered at 2.5 GHz, whose electrical spectrum is depicted in the inset of Fig. 11.28b. To verify that the proposed receiver can realize a large bandwidth, high flexibility, and high precision, we generated different frequency RF carriers to transmit quaternary phase-shift keying (QPSK) signals with 1-MHz bandwidth and analyzed the receiving results. Here, the bandwidth of the electronic filter can be defined to be as narrow as a few megahertz to adapt to the 20-MHz ADC used in this scheme. In the first case, we used broadband horn antennas with a frequency band from 2 to

24.5 GHz to transmit and receive the signals through a 1-m distance. The measured error vector magnitude (EVM) curve over the received RF carrier is depicted by the red line in Fig. 11.28c, and the corresponding scatter plots for the input RF carrier at 12.5, 18.5, and 22.5 GHz are depicted in the insets (I), (II), (III) of Fig. 11.28d, respectively. The performance of the receiver deteriorates dramatically with carrier frequency. This can be attributed to the increasing transmission loss with increasing frequency between the antennas, which exceeds 28 dB for the RF signal at 22.5 GHz. In the second case, we compensated for this loss by eliminating the antennas, and the newly obtained EVM curve with back-to-back connection is depicted by the blue line of Fig. 11.28c. The corresponding scatter plots for the RF input at 22.5, 32.5, 37.5 GHz are depicted in the insets (IV), (V), (VI) of Fig. 11.28d, respectively, where the slight differences arise from the frequency response of the photodetector in the transmitter. The results demonstrate that high-frequency RF signals could finally proceed accurately with the available ADC through RF-IF and IF-baseband conversion in this scheme.

In summary, we present a photonic-assisted SDR transceiver where either transmitting or receiving is accomplished with combined electronic and optical stages. In the experiments, RF carriers ranging from the C-band to Ka-band were flexibly generated, limited only by the available bandwidth of the photodetectors. In addition, the receiver could effectively select these RF signals and convert them to baseband for sensitive detection and accurate analysis. We combined the advantages of the RF photonic techniques and conventional SDR techniques to realize large bandwidth, high flexibility, high precision, and software programmability in this demonstrator. To the best of our knowledge, this is the first time these requirements have been achieved significantly for future exploiting of more usable spectra for wireless communication.

11.5 Conclusions

Microwave photonic frontends have attracted a lot of research interest, because of the advantages related to the RF frontends, such as the potential to broaden the working frequency range, large dynamic range, EMI, etc. Signal processing as the key element in most of the proposed photonic frontends, which consist of down-conversion and signal processing, has been researched extensively. Different kinds of integrated signal processors have been proposed, and some of them have already been applied in the frontends for signal processing. Based on silicon photonics, the programmable signal processors with high Q and also large FSR have already been realized. However, there are still some obstacles to be overcome. First, the insertion loss of the signal processors should be lower including the fiber in and out of the chip, which would influence the noise floor of the frontend and the dynamic range. Second, the shape of the signal processors should be optimized, e.g., increasing the roll-off coefficient, which would impact the signal-to-noise ratio. Third, the monitoring and control of the signal processor should be built up for

feedback to track the signals received in the frontends. Thus, for the development of the silicon photonics signal processing-based photonic frontends, the packaging of the chip with low loss and robust performance would be the trend for practical applications. Another direction of our research for the microwave photonic frontends is integration of the entire frontends to a single chip, so that the system would be more compact and robust, which would be attractive for many of the specific applications that care about the weight and size.

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Chapter 12
Advanced Silicon Photonics Transceivers

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Abstract After an introduction on optical interconnect applications, we address key aspects of silicon photonics base technology which includes: wafer process technology, photonic device libraries, integration with electronic circuits, and optical probing technology. Next we cover actual integrated circuit design including transmitters and receivers. Finally, we also address the important aspects of light source and packaging technology.

12.1 Introduction

The use of silicon as a passive and active waveguide material was first proposed in 1986 [1, 2]. A significant acceleration in development activity occurred when lithography tools in the integrated circuit (IC) industry-enabled patterning of the fine structures needed for photonic devices in this material system. Various groups investigated the technology [3–10] and there was also significant funding from governments [11, 12] and the investment community, with the promise that silicon photonics could dramatically save costs and increase functionality by leveraging the capabilities of the semiconductor industry. However, soon it became clear that many other problems had to be solved, including: (1) the light source, (2) low loss optical interfaces and their impact on packaging, and (3) an advanced design environment to design and layout complex combined electronic and photonic circuits. The first commercial product came only in 2009 in the form of an active optical cable [13]. Several other products were introduced at higher data rates [14] as well as implementations of wavelength division multiplexing (WDM) [15, 16]. In recent years, several companies have announced product releases of silicon photonics-based transceiver products. Also products for applications in biosensors

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have been released [17]. Nowadays, silicon photonics is by many deemed to be the technology of choice for the next generation (>25 Gbps), high-density optical transceivers addressing the needs of the growing datacenter and enterprise markets.

12.2 Silicon Photonics for Optical Interconnect

At high data rates (≥25 Gb/s) signal integrity effects, such as losses and reflections, severely limit the reach of electrical interconnects. To an extent, these effects can be mitigated by techniques such as pre-emphasis, equalization, and retiming of the electrical signals. The use of advanced materials for cable and printed circuit board (PCB) implementations is also beneficial in this respect. While these methods may stretch the practical reach of electrical interconnect to a few meters, they significantly increase cost and power dissipation.

Optical data transmission systems suffer much less from the issues listed above since optical fiber is used as the transmission medium. Initial implementations of short reach optical interconnect were based on multimode fiber in combination with 850 nm vertical-cavity surface-emitting lasers (VCSELs). However, modal and chromatic dispersion effects in the fiber limit the bandwidth-reach product of this solution. Those dispersion effects can be either mitigated by optimization of the index profile of the fiber in combination with special methods for coupling light from the VCSEL into the fiber, or by reducing the spectral line width of the VCSELs. At 10 Gb/s a reach of 300 m can be reliably obtained using OM3 multimode fiber in combination with suitable 850 nm VCSELs [18]. At 25 Gb/s it is expected that a reliable reach of 100 m can be supported using OM4 multimode fiber in combination with 850 nm VCSELs having improved bandwidth [19]. This exemplifies that multimode solutions require upgrading of the fiber infrastructure each time, there is an increase in data rate. For a couple of years, silicon photonics has been used as an alternative solution for optical interconnects in high-performance computing and datacenter applications. It does not suffer from any practical bandwidth or reach limitations, because it uses single-mode fiber in combination with narrow line width light sources. Single-mode fiber infrastructure in combination with silicon photonics allows virtually reach independent scalability toward: higher baud rates, higher bit rates per channel (by advanced modulation), multiple fibers (or cores in the fiber), and multiple wavelength channels (WDM).

Another important aspect of silicon photonics is that it lends itself very well for very close integration with ASICs by 2.5 D integration [20]. This allows a drastic reduction in power dissipation by removing impedance-controlled electrical interconnects between the ASIC and optical transceivers. It will also enable never before seen levels of system integration by eliminating stand-alone transceiver devices by integrating their function into the ASIC and drastically reduce the space and density limitations of electrical interconnects.

12.3 Silicon Photonics Technology Advancements

12.3.1 Silicon Photonics Wafer Processing Flow

As of today, Luxtera has developed two silicon photonics technology platforms, on 200 and 300 mm substrates [21, 22], where the latter supports operation at both 1310 and 1490 nm wavelength ranges. The process integration for both of these platforms leverages pre-existing process flows from standard CMOS technologies. This minimizes development risk and maximizes commonality with other high-volume products, ensuring manufacturability of our products. In this section, we focus on the customizations necessary to introduce photonic functionality. Figure 12.1 shows a diagram of a typical process flow broken up into key process modules for our silicon photonics technologies.

The silicon-on-insulator (SOI) substrates used at the start of the process flow are customized to optimize performance of photonics devices, resulting in buried oxide and top silicon thicknesses that are significantly thicker than those used in CMOS SOI processes for electronic circuits. All optical devices are patterned in a single lithography step in one of the very first modules of the flow, followed by a partial etch of the top silicon layer. The requirements on this patterning step are vastly different from traditional CMOS. This is due to the variety of structures needed for all of the different optical devices, including long straight waveguides, bends, gratings of varying pitches and fill factors, and directional couplers. For this reason, the development of this process module requires careful physical characterization of silicon versus drawn shapes to understand process windows, device variability, and optimize overall performance. In addition, tight control of the top silicon thickness and the depth of the silicon etch are critical to maintain a low variability of performance. An example of a cross-section of a single-mode waveguide structure is shown in Fig. 12.2.

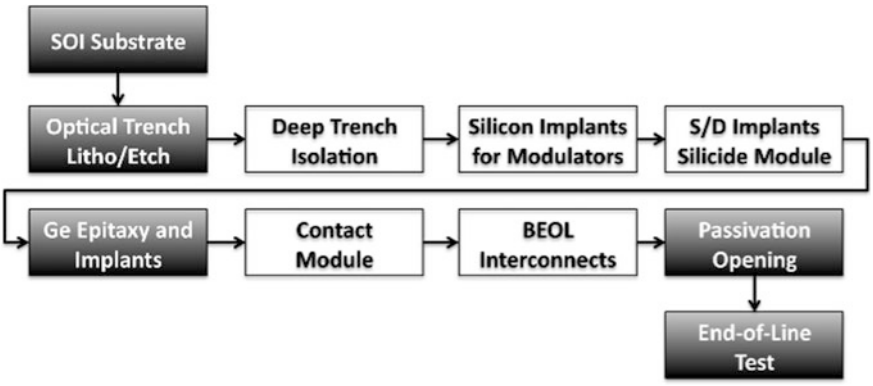

Fig. 12.1 Process flow for Luxtera's Silicon Photonics technologies. *Dark boxes* indicate custom steps; *white boxes* indicate standard steps based on existing CMOS technologies

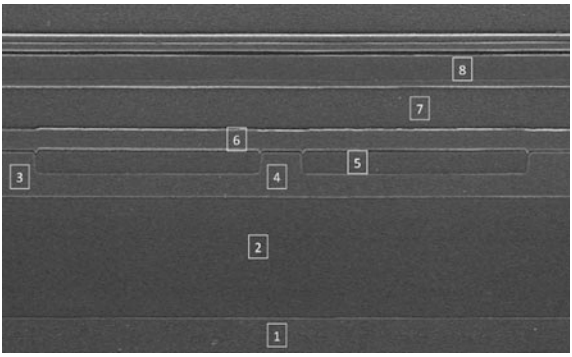

Fig. 12.2 Cross-section of a Silicon Photonics rib waveguide patterned on an SOI wafer and covered with dielectric layers: *1* silicon substrate, *2* buried oxide (BOX), *3* single-crystal silicon layer, *4* rib waveguide, *5* field oxide, *6* contact etch-stop/salicide blocking layer, *7* contact inter-level dielectric, and *8* metal 1 low-k dielectrics

To create optoelectronic devices such as modulators, conventional silicon implant steps are used with energies and densities specifically targeted for photonic devices. A typical configuration is a lateral diode in a silicon waveguide to implement low- or high-speed phase/amplitude modulators operating in forward or reverse bias (depending on the doping).

The next major customization step is the introduction of a 100 % germanium epitaxy and Ge implantation module for the formation of photodiodes.

SiGe epitaxy is nowadays commonly found in modern CMOS processes where it is used to create the source/drain regions of pmos transistors. The use of the wider lattice constant alloy provides the compressive stress in the channel, which increases the hole mobility in these devices. The Bi-CMOS process also makes use of SiGe to form the critical base layer of heterojunction bipolar transistors (HBTs). Both of these processes typically use SiGe alloys with a Ge concentration rarely exceeding 50 %. In silicon photonics, pure Ge is used because of its optical absorption extending up to 1.55 μm, thus covering most of the useful spectral range used in optical communications. Also its chemical similarity to Si is beneficial for process integration. The first attempts toward Ge integration started when solid-state electronics was still in its infancy [23]. Over the last few years, significant progress has been made in improving the performance of Ge on Si photodetectors. A detailed analysis of the different approaches attempted and results can be found in [24].

The main issue when trying to integrate a Ge film on a Si substrate is the difference in lattice parameters between the two materials. A $\sim$4 % difference results in the plastic relaxation of films with thickness just above a few tenths of a nanometer, with the consequent introduction of crystal dislocation defects both at the mismatched interface between the two materials (misfits) and through the body of the film (threads). These defects hinder the performance of the device built using the Ge film, especially by increasing the leakage current. In an attempt to improve

the film quality, high temperature growth can be used; however, the direct deposition of Ge on Si at high temperature results in 3D growth and the formation of islands, because of the lower energy of this configuration [25]. In order to eliminate this issue, a two-step growth was initially proposed in [26]. In this process, a low temperature film is first deposited until the mismatch stress is relaxed through the introduction of misfits, then the growth is continued at higher temperature thus providing a better quality film. Other approaches, not relying on chemical vapor deposition (CVD) have been proposed in the past to fabricate crystalline Ge films on Si, but as of today, CVD epitaxy seems still to be the only manufacturable solution.

Ge can be doped using the same species as Si, and despite a poorer activation efficiency of P (and a very large diffusivity), effective P-i-N junctions can be readily formed using standard ion-implantation and annealing. In some cases, contacts to the doped regions can be formed by heavily doped Si layers, thus eliminating the need for adapting the standard CMOS contact process to Ge [27].

The thermal budget associated with Ge integration in a CMOS flow comprises two main parts: the pre-epitaxy substrate cleaning and the epitaxy itself. Some authors have found also that a post-epitaxy anneal (possibly cyclic) improves the quality of the film by further reducing the threading dislocations. This additional anneal, normally performed at relatively high temperature (800–900 °C), further contributes to the total thermal budget. Ge epitaxy is typically performed at relatively mild temperatures (400–600 °C); therefore, its impact on the total thermal budget is often negligible. On the contrary, the precleaning process typically based on a hydrogen bake performed at $\sim$800 °C can affect the performance of other devices integrated along with the Ge detectors. For this reason, we developed a lower temperature process to accomplish this critical substrate preparation step, using a sequence of deposition and etching aimed at removing the remaining oxygen on the Si surface [28].

After the epitaxy step, a conventional contact module produces the contacts to the silicon by highly doped silicide formation. The contact formation to the Ge photodetector devices occurs at the same time, although no germanicide is used in this case (Fig. 12.3).

Conventional copper metallization is used for the back-end interconnects, which also contain the aluminum pads. However, it is important to select the back-end dielectric layers, which typically consist of oxide and nitride layers, based on the optical transmission properties of the total stack, so that the optical insertion loss of the grating couplers used as optical I/Os is minimized. There are also mechanical and thermal constraints on the back-end technology selection for its compatibility with subsequent packaging/assembly steps such as wire bonding and face-to-face bonding with microbumps as described further in Sect. 12.3.3.

Finally, openings are patterned in the top dielectrics (typically nitride passivation layers) over grating couplers, to reduce the refractive index mismatch between external components, such as fibers and light sources, attached on top of the silicon photonics chip and the dielectric back-end layers.

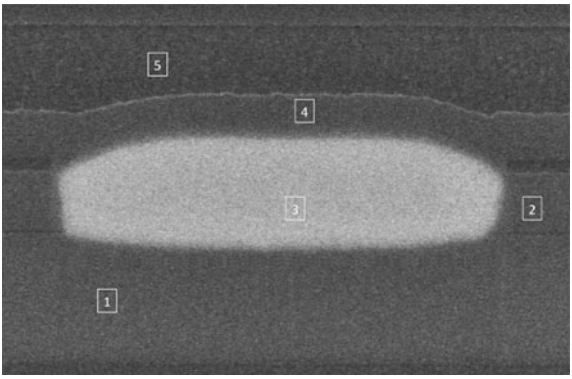

Fig. 12.3 Cross-section of Ge waveguide photodetector (WPD): *1* single-crystal layer, *2* dielectric selective epitaxy masking layer, *3* epitaxial Ge film, *4* dielectric protection layer, and *5* contact interlayer dielectric

12.3.2 Silicon Photonics Devices

The material system used for silicon photonics chips naturally lends itself to the construction of high-density optoelectronic circuits, due to its high refractive index contrast, which allows small device dimensions and area-efficient routing. At the same time, the high-index contrast increases the sensitivity of the device performance to process variability. For this reason, it is critical that the devices are thoroughly characterized to ensure their performance across all process corners.

The first commercial products based on silicon photonics were focusing on optical communications, and thus the emphasis in our PDK is on elements that enable optical transceivers. These devices fall into the following categories: (1) coupling the signal between the optical fiber and the chip, (2) guiding and distributing the light on the chip, and (3) creating and detecting light signals.

We have chosen a surface-coupling technique to transmit the signal from and to the fiber [29]. Grating couplers (GCs) comprise diffractive gratings that provide extra functionalities in addition to transferring the signal. The mode size, the submicron waveguides is about an order of magnitude smaller than in the fiber, so the GCs must appreciably transform the mode size as well. As the waveguides only support a single TE mode, a polarization diversity schema must also be enabled by the GC on the receiver side. For this reason, at least two main types of grating couplers are used in a transceiver. The single-polarization GC (SPGC) is based on a one-dimensionally periodic grating, and it receives light with a known polarization to the chip, or, alternatively, it transmits light from the chip into the fiber with a linear polarization. These GCs form the interface of the transmitter to an external light source and to the fiber. The polarization-splitting GC (PSGC) is employed as the input to the receiver. It comprises a two-dimensionally periodic grating that splits the linear polarization states in the fiber into two separate waveguides on the chip.

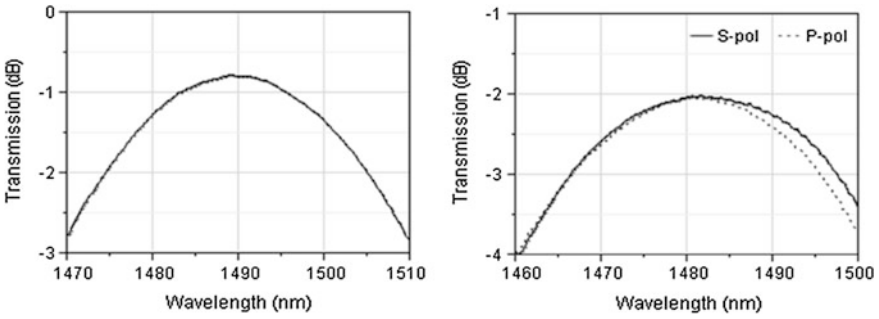

Fig. 12.4 Transmission spectra for SPGC (*left*) and PSGC (*right*)

The insertion loss of the GCs is limited by two main factors: first, the directivity, which quantifies how efficiently light is directed from the waveguide to the direction of the fiber as opposed downward to the substrate; and, second, the modal overlap, which describes the how well the GC mode matches the Gaussian mode of the fiber. We have increased directivity by increasing the reflectivity of the substrate by adding a DBR mirror underneath the buried oxide, and we improved the modal overlap by varying the scattering strength across the grating. The resulting SPGC and PSGC designs have been demonstrated to achieve 0.8 and 2 dB insertion losses [30], respectively. Figure 12.4 shows the transmission spectra for these devices.

The second category of optical circuit elements comprises other passive devices: the waveguide to guide light across the chip, splitters to allow sharing light from the same laser among channels, and optical taps to monitor the signal at multiple points in the circuit. We have implemented various schema to reduce the insertion loss of the waveguide interconnects. A single-mode waveguide (SMW) typically has loss in excess of 1 dB/cm due to scattering losses induced by sidewall roughness; whereas a multimode waveguide (MMW) with width of 1–3 μm can have loss as low as 0.1 dB/cm. In the photonic circuit, the SMW is widened for long runs across the chip to a MMW, with an adiabatic taper connecting the two types of waveguides. When the waveguide connects to another device, or changes direction, it is down tapered to a SMW again. Such an approach can significantly reduce the on-chip link loss.

Given the complexity of the photonic circuits on our transceiver chips, the circuits can contain a multiplicity of bends, and it is therefore essential to reduce their contribution to the link penalty. For bends with small radii at around 30 μm, transition losses due to the curvature discontinuity at the junction between the straight waveguide and the curved bend dominate over the bending losses that are due to the curvature of the bend itself. One solution is to draw the bends with a continuously changing curvature that is zero at the waveguide ends, and is at a maximum at the bend center.

The third device category includes modulators and photodetectors. The electrical signal is impressed onto the continuous wave light from the laser using a high-speed phase modulator (HSPM) employed in a Mach-Zehnder interferometer

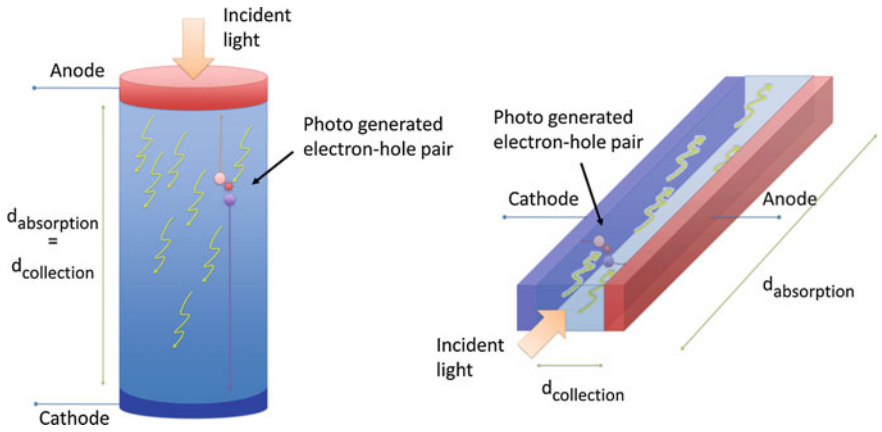

Fig. 12.5 Surface-illuminated and waveguide photodetectors

configuration. The HSPM comprises a reverse-biased p–n junction in the silicon waveguides. Typical performance characteristics are $V\pi L\pi$ = 2.5 V.cm, 6 dB/cm insertion loss, and 350 fF/mm capacitance density. However, the doping and the junction geometry can be adjusted to trade-off phase shifting efficiency and insertion loss, depending on the system requirements.

The germanium photodetector is monolithically integrated in the silicon photonics process. Light is coupled through an integrated optics waveguide into the detector, this enables the use of a waveguide photodetector architecture (Fig. 12.5) which is advantageous with respect to the surface-illuminated photodetector because of the lower parasitics and the freedom from the efficiency-bandwidth trade-off typical of the latter, due to the orthogonal paths of photons (affecting quantum efficiency through absorption) and photogenerated carriers (limiting transit time and device speed). Waveguide photodetectors with a performance on par with similar III–V devices have been demonstrated and are currently used in our products. One of the key advantages of integrated waveguide photodetectors is the very small capacitance that can be conveniently used to achieve very high sensitivity and bandwidth receivers. The Ge photodetector operates at very low applied bias ($\sim$1 V), which is fully compatible with modern CMOS technologies, or even at short circuit when dark current is a concern and a reduced speed can be accepted as in monitor photodiode applications.

The responsivity of our detectors is thus near the quantum limit. For instance, we have demonstrated a typical responsivity of 1.05 A/W at 1310 nm. Another advantage of the waveguide detector is that the receiver bandwidth is not limited by the detector capacitance, which is about 15 fF for the homojunction. The bandwidth of the detector depends on the specifics of the junction design. In a Ge p-i-n homojunction architecture, the 3 dB electrical bandwidth is about 27 GHz, whereas in a Si–Ge heterojunction architecture a bandwidth in excess of 40 GHz has been demonstrated [31].

12.3.3 2.5 D Integration for Combining Electronic and Photonic Circuits

Monolithic integration of photonics along with electronics offers a number of features that provide substantial advantages versus discrete solutions. As an example, the sensitivity of a high-speed receiver greatly benefits from the reduction of parasitic capacitance at the connection between the photodetector and the TIA [32]. Beside these positive aspects, however, monolithic integration brings some important drawbacks. The monolithic approach forces a complete redevelopment cycle each time, a different CMOS technology node, or a different foundry, is chosen as the target for integration with photonics. In the field of optical interconnects, in particular, the progressive increase of the data rate needed to keep pace with increasingly powerful CPUs has prompted the adoption of state-of-the-art CMOS nodes to implement the driver functions of optical devices. If a 130/90 nm node on SOI was sufficient at 10/14 Gbps [33], 28 nm is needed for 25 Gbps, and 16 nm is anticipated to be required at 56 Gbps. Moreover, in certain applications, where lower digital complexity is acceptable and top-notch RF performance is required, a Bi-CMOS process might be a better choice [34]. As discussed in a previous chapter, the integration of photonics functionality requires a substrate change (SOI, custom) along with the introduction of a number of additional process steps, some (such as the Ge epitaxy) bringing a non-negligible thermal budget. All these factors, besides requiring a meaningful investment, result typically in the drift of transistor parametric performance, raising further concerns against the monolithic approach.

Fortunately, similar trade-off considerations have prompted the IC industry a few years ago to investigate and develop new forms of hybrid integration between integrated circuits built on different process technologies, focusing on minimizing interconnect parasitics and keeping a compact form factor. A classic example is that of memory (DRAM) and CPUs. Silicon photonics can take advantage of these hybrid integration processes by confining all the optical functionality to one chip built on a customized CMOS process, and integrating the electrical part (drivers, TIAs, CDRs, control systems) in a "companion" chip built in a fully standard CMOS/bipolar process.

The most common form of hybrid integration uses a "flip-chip" approach: one of the two dies to be interconnected is used as a "substrate" for the second die that is flipped upside down so that the bond pads of the two chip are facing (Chip-on-Chip: CoC) as shown in Fig. 12.6. In order to form a stable and reliable electrical joint between the facing pads, tiny metal pillars (typically made of copper) are plated on top of the pads and are "fused" together through a thin solder joint. The resulting electrical interconnect is very short when compared to a standard wire bond, for example, and provides reduced parasitics. In addition, contrary to a wire bond interface, which is limited to the die perimeter, this approach allows the use of virtually the full surface of the dies for interconnects, thus offering unprecedented I/O density. The space between the two dies, not used by the electrical connections,

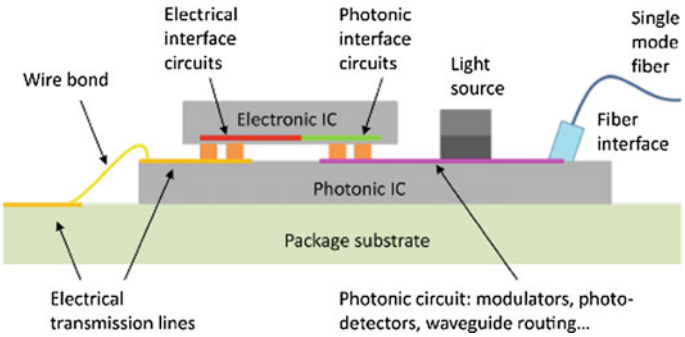

Fig. 12.6 Hybrid integration of electronic and photonic circuits. The electronic IC is face-to-face bonded to the photonic IC by means of microbumps

is normally filled with a resin to improve the mechanical stability of the assembly and offer some level of protection from corrosion for the exposed copper pillars. This type of packaging has been used in the past to connect ICs to laminate or ceramic substrates. In this new development, the substrate is replaced by a second IC bringing some advantage in terms of reliability (better matching between the thermal expansion coefficients of top and bottom sides of the assembly) and I/O density (both sides use CMOS back-end of line (BEOL) processes, capable of micrometric lithography). The latter, in particular, allows an interconnect pitch as small as 40 μm with a pillar size of approximately 20 μm [35]. Thousands of interconnects per assembly can be established using this approach.

In the silicon photonics implementation of the flip-chip process, the bottom die is typically the one carrying the photonics circuitry and it is built in a customized process [21, 22], while the top die integrates the electronics and can be fabricated in an advanced CMOS node (e.g., 28 nm). This approach facilitates the subsequent integration of the optical I/O element and the laser source.

One interesting aspect of this hybrid approach is its scalability to wafer-scale: the placement of the electronics "daughter" dies on the "parent" silicon photonics wafer can occur while the latter is still in wafer form (Fig. 12.7). This brings a number of advantages in terms of material handling (a single 300 mm silicon photonics wafer can have several hundreds of dies on it) and process throughput. The populated wafer is subsequently diced to release the individual assembled units.

12.3.4 Wafer-Scale Optical Probing of Silicon Photonics

A fundamental enabler in the development of a new technology is the ability to test in a fast and efficient manner a large number of experimental designs, exploring geometrical parameter spaces, built on a similarly extensive number of test wafers, covering different process conditions. In electronics, this is readily done using a

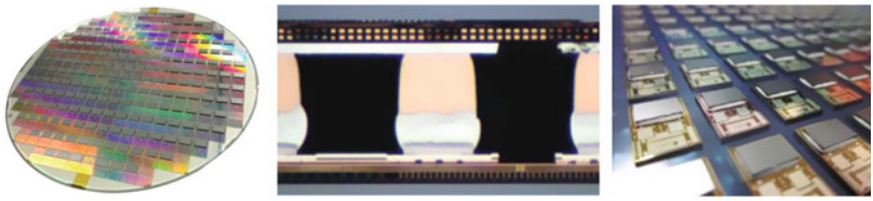

Fig. 12.7 Face-to-face bonding of electronic ICs to photonic ICs while in wafer form (*left*). Cross-section of micro-bump electrical interconnects (*middle*). Chip assemblies (*right*)

testing platform capable of handling full wafers, thus avoiding any delay and additional cost induced by dicing and packaging. Wafer probe stations are complex systems capable of positioning with an accuracy close to 1 μm an electrical probe-card at a specific location on the wafer. Typically, a probe station can automatically load and align wafers from a feeding standard cassette (or FOUP/FOSB for 300 mm wafers) containing up to 25 wafers. Actual electrical testing is normally performed by another system (typically dubbed "tester"), which is coupled to the prober via a mechanical and electrical interface. Wafer probers are used in the development phase of Si technologies to provide test data from experimental device/wafers, as well as during the normal commercial deployment to ensure wafer quality through a series of tests performed on specifically designed structures. The latter is typically performed at the end of the processing of each batch/wafer and goes under the name of Wafer Acceptance Test (WAT). Finally, the wafer prober, in combination with an IC specific test protocol, is used to identify the yielding ICs on a wafer for subsequent packaging. At the core of the economic motivation behind CMOS-photonics stands, the concept of sharing all the key aspects that made the Si industry a success; wafer-scale testing is definitely one of them.

In order to enable wafer-scale testing of photonic devices and systems, a surface-normal way of coupling light is required. Lacking that, testing will only be possible after dicing. As discussed previously, Luxtera has chosen the grating coupler as the optical I/O interface to its systems, one of the reasons being, in-fact, the possibility to enable wafer-scale probing. The grating coupler is designed to match the optical mode characteristics of a single-mode fiber (SMF). In photonics wafer-scale probing, a set of SMF arranged in the array configuration (fiber array: FA), are used as the "probe" to couple light in and out of the device under test (DUT), see Fig. 12.8.

Two major aspects differentiate a standard wafer-scale electrical test from an optical one using grating couplers: the first is that the positioning accuracy required is higher in the optical case (much better than 1 μm in the optical case vs. typically >1 μm in the electronics case). The second is that an optical test does not require physical contact between the probe-card and the wafer, but it still demands a fine control of the distance between the two, on the order of 1 μm. In our approach, the burden of ensuring an accurate positioning of the optical probe is split between the

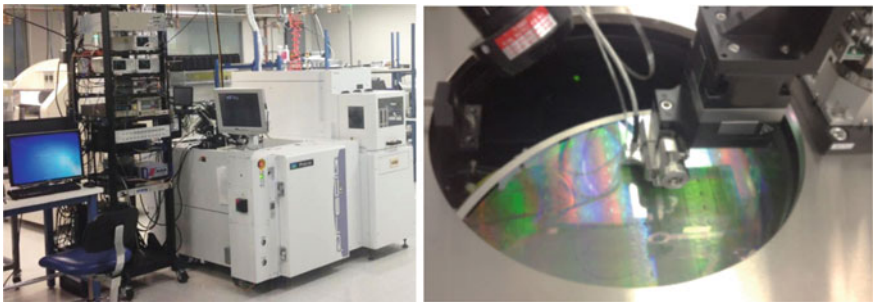

Fig. 12.8 Automated optical probing system and probing head

prober and the "probe-card" itself. As mentioned before, standard electronic probers achieve a positioning accuracy of ~ 1 μm, thus providing a first, coarse, alignment to the photonic DUT. A fine alignment is then achieved using a piezoelectric actuator mounted on the support of the FA. A feedback signal from the DUT is used in this phase (active alignment). Thanks to the high speed of the piezoelectric actuator, a typical alignment procedure takes less than 2 s. The vertical positioning of the FA above the wafer is also ensured by the piezoelectric actuator, using, in this case, a feedback signal from a distance sensor cointegrated with the FA in the optical probe.

The same system is used with the addition of a standard electrical probe and the necessary testing equipment (SMUs, oscilloscopes, pattern generators, LCA), to perform optoelectronic tests, for example, photodiode response and modulator transfer function, both at DC and as a function of the frequency of an excitation signal.

In the simplest form of wafer-scale optical test, after indexing and alignment, a tunable laser is used to produce a wavelength scan while its light is coupled into the input port of the DUT. At the same time, one or more power meters synchronously collect the light intensity from the single or multiple output ports of the DUT. In case of an optoelectrical test, such as that of a photodetector, the power meter is replaced by an SMU and the quantity recorded is the photocurrent generated by the device under a certain illumination and electrical bias. Obviously, the very same photocurrent signal is used to provide the fine alignment to the DUT.

The same approach can be used to test a complete system die in production to ensure compliance to performance specifications. For example in an 8-channel transceiver chip, light can be coupled into the die following the optical path used during normal operation and including the splitter tree, the modulators, the control system, and the output ports, which are monitored individually by SMF mounted in the test head FA. This test allows an evaluation of the loss in the full transmission path as well as to detect the presence of a potential defect in any of the channels. This type of test, offering full coverage of the on-chip optical interconnects, brings to silicon photonics the concept of known good die (KGD), which is a key aspect of the cost optimization process in the electronics industry.

12.4 Advanced Optical Transceiver Design in Silicon Photonics Technology

12.4.1 Design Infrastructure: Design Kit

In order to design successfully advanced silicon photonics transceivers with complex interconnection between a large number of electronic and optical devices, designers need a complete process design kit (PDK) for use in an automated design environment.

Luxtera has developed such design kits for our technologies, with the following main features: (1) validated device library, (2) capability for simulation of complete optoelectronic systems, and (3) physical verification tools to ensure that what is taped out to the manufacturing facility can be produced without defects and with high yield, and also actually matches the intended system design.

The photonic device library contains validated cells for all of the individual devices offered by the technology. Only those cells present in the validated photonic library are allowed for use in product design. Each device is represented by a layout (either fixed or parameterized), a symbol (for use in schematic-driven design), and a model. In our PDKs, photonic device models are based on behavioral code, which allows co-simulation with electronic devices in a standard electronic design automation (EDA) environment for instance using spice models. Additionally, for each of the devices, we performed extensive characterization of their performance across process, temperature, and input variations such as voltage and current (this is known as "corners" in traditional electronic design). This required understanding the process variability for the steps driving device performance and in some cases running wafers with intentional process offsets to represent extremes of the process variability. This information is then captured in the models and designers can select to run simulations where photonic devices models are pegged to best/worst case of the process variability. As a result of this implementation, we are able to simulate end-to-end performance of a complete EO-OE transceiver system from a schematic in a standard EDA environment. Figure 12.9 shows an example of the schematic of an optoelectronic transmitter containing both transistors, other electrical devices, and photonic devices like splitters, combiners, and high-speed phase modulators, as well as a resulting simulated optical eye diagram resulting from an input electrical signal, using the models described above.

The schematic shown above can be iterated until the performance is satisfactory across corners, then it is translated to a physical layout of the chip. Physical layout verification implements a variety of checks, the two most important being design rule checking (DRC), and layout-versus-schematic checking (LVS). DRC is an automated check that compares drawn geometries with design rules that are in place to protect primarily against violations of process capabilities, which could result in defects and yield loss during the manufacturing process. Typical checks include minimum width, minimum spacing, enclosure of one layer by another, and density of features across the entire chip or moving windows. The implementation of DRC

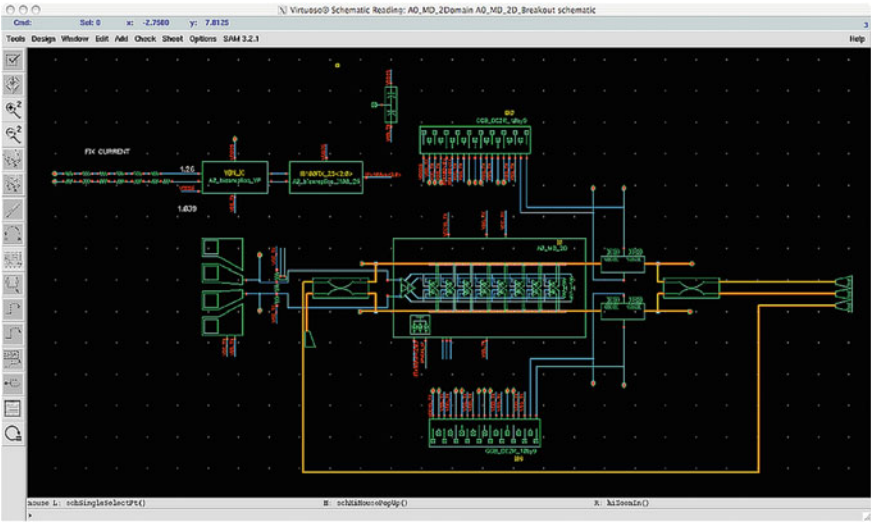

Fig. 12.9 Example view of a design environment: schematic of silicon photonics transmitter with optical and electrical ports and its constituting devices. The schematic allows for full, end-to-end simulation of the combined electronic-photonic circuit

for optical circuits is rendered more complex by the different shapes in use; DRC checkers have long been optimized for the Manhattan geometries employed in electrical circuits and often can struggle with optical circuits, though recent improvements in DRC software have made it possible now to effectively check our designs. LVS is also a critical step that automatically analyzes the layout to extract a schematic, which is then compared to the original schematic that was optimized in the simulation step above. LVS thus ensures that the layout matches exactly the schematic in terms of devices placed (with exact parameters checked) and their connectivity.

The 2.5 D integration as discussed in Sect. 12.3.3 introduces additional complexity because we now need to validate connectivity and simulate across two different technologies (CMOS electronic chip/CuPi/silicon photonics chip), which usually both have their own separate DK, in addition to performing a physical check of the elements related to the CuPi (pads on both chips). As this is a rather immature area, software vendors and foundries are exploring many avenues, often resulting in custom solutions. Luxtera developed an internal solution, which is an extension of what is described above; it has been validated in multiple product tape outs.

12.4.2 Transmitter Design

Luxtera employs external Mach-Zehnder modulators (MZI) in the transmitters, which utilize reverse-biased diodes as high-speed phase modulators (HSPM).

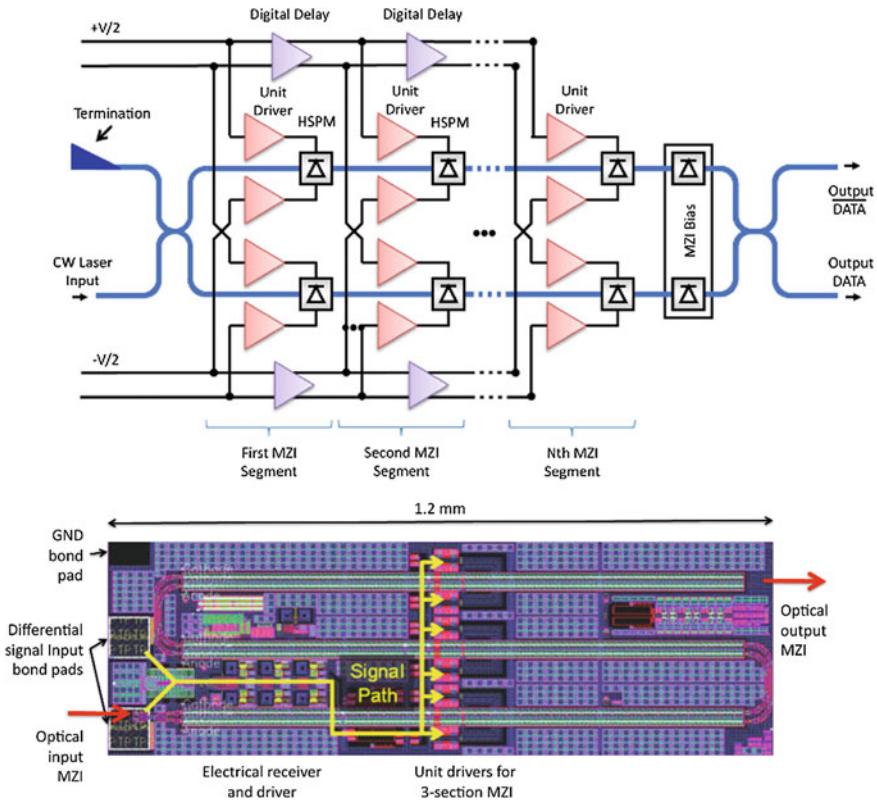

Fig. 12.10 The MZI architecture of the segmented MZI with two voltage domains (*top*). "Serpentine" MZI layout using low loss waveguide turns (*bottom*); this allows reduction of the area and shortens interconnects between unit drivers and HSPMs

The overall length of the MZI is governed by the total phase shift required to produce a large enough extinction ratio at the output, while limiting the optical insertion loss and electrical power dissipation to reasonable levels. The phase shift per unit length, produced by the plasma dispersion effect in the silicon waveguides, is itself restricted by the reverse bias that can be supplied to the diodes within the capabilities of the process technology node used for the driver circuitry. The transmitters designed by Luxtera in the 25 Gbps generation of products use a reverse bias of 2×0.9 V and an overall MZI length of $\sim$2.5 mm. To accommodate the substantial size of the MZI on the die more easily, the HSPM diodes are placed in a serpentine fashion, which, apart from creating a compact layout, helps to reduce the parasitics associated with the Tx driver blocks as shown in Fig. 12.10.

Since the MZI is a relatively long subsystem, providing the modulating electrical signal along the entire length of the interferometer with high fidelity is challenging. Instead of the traditional traveling wave method, Luxtera utilizes a distributed driver approach to get full-scale modulation from all the diodes that constitute the MZI.

The electrical losses in the transmission lines are avoided, while phase matching between the optical and electrical paths is accomplished through fine tuning of the digital delays in the various stages of the distributed driver circuitry. For the driver design itself, it is important to note that encoding data using these transmitters involves modulating the depletion region in the reverse-biased diodes at high speed, which is akin to rapid charging and discharging of a capacitive load. Therefore, rail-to-rail CMOS inverters are ideally suited to driving the phase modulators. The inverters also lend themselves well to the distributed approach for phase matching and power reduction. Capacitive domain splitting before each inverter combined with a push-pull architecture with respect to the driving of the two arms of the MZI, allows the rail-to-rail swing of the inverters to be half of the full reverse bias applied to the phase modulator diodes. All these features allow the transmitters to provide excellent optical modulation amplitude (OMA) characteristics without incurring a significant power dissipation penalty and with extinction ratios above 4 dB.

12.4.3 Receiver Design

High-speed receivers for non-return zero (NRZ) optical signals are typically composed by a trans-impedance amplifier (TIA) followed by a limiting amplifier (LA). The former operates the translation of the optical photocurrent generated by the receiver photodiode into a voltage signal proportional to it, while the second amplifies the voltage signal and transforms it into a digital sequence of high and low levels, irrespective of the actual input optical amplitude (hence the "limiting" attribute). The simplest TIA can be realized with just a load resistor connected to the photodiode (Fig. 12.11). The trans-impedance gain of this stage is the load

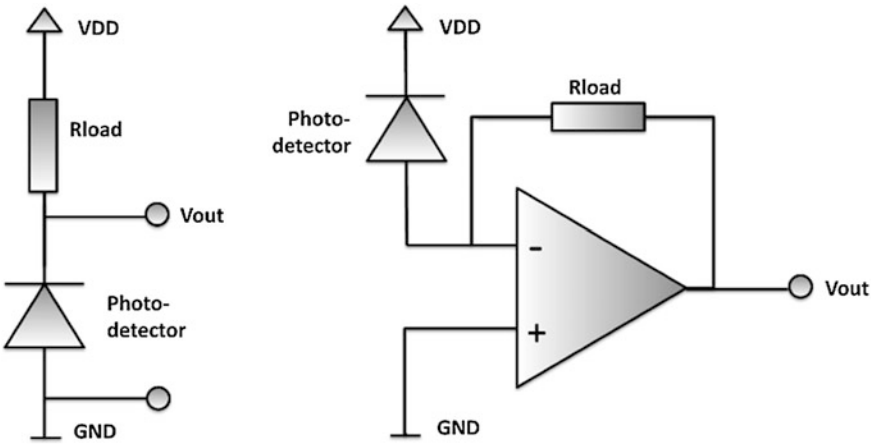

Fig. 12.11 Receiver architectures

resistor value. This architecture, however, is rarely used because of the intrinsic speed limitation represented by the RC time constant created by the load resistance and the detector capacitance. Better performance can be obtained by adding one or more gain stages with the current to voltage conversion resistor connected in a feedback configuration (Fig. 12.11). Using this approach, the effective resistance in the RC time constant is reduced by a factor close to the amplifier voltage gain, thus resulting in a much wider bandwidth for the same trans-impedance gain. While a large voltage gain will be beneficial in this architecture, stability considerations (e.g., the Barkhausen criterion) limit in most cases the maximum number of stages to one. This can be quite restrictive especially in very high-speed TIAs designed in advanced CMOS nodes where the gain available from a single transistor stage is small. The only remaining option to improve the gain-speed trade-off at the TIA is that of reducing the detector capacitance plus the parasitic capacitance. Fortunately, this can be accomplished in an integrated receiver using waveguide photodetectors that have much lower capacitance than that of the surface-illuminated ones, owing to a much smaller junction area. The intimate integration between the PD and the TIA also greatly helps in reducing the parasitics. Our Ge waveguide photodetectors have a capacitance of $\sim$10–15 fF at a reverse bias of 1 V. This is about one order of magnitude lower than that of a typical surface-illuminated photodetector, allowing the achievement of a substantial increase in the TIA trans-impedance gain (for the same bandwidth) or a much wider bandwidth for the same gain.

12.4.4 Transceiver Architecture

With the infrastructure described above, Luxtera has designed and produced a family of parallel advanced optical transceivers. The generic architecture of these transceivers is shown in Fig. 12.12, while an example of a complete assembled chipset for an eight-channel transceiver is shown in Fig. 12.13. The same architecture applies to, for instance, four- and eight-channel transceivers, allowing for maximal reuse of subsystem designs in a family of products.

The interface between the electrical and optical chips is at the set of copper pillars that connect the two in the face-to-face bonding approach. Optically, the current chipsets use a single light source, at either 1310 or 1490 nm, which is coupled to the photonic chip via a grating coupler. The incident light is then split N-ways via an on-chip $1 \times N$ splitter tree, and each transmitter is composed of an MZI including bias and monitor photodiodes for control. The Tx signal is coupled to a fiber or other optical element via a single-polarization grating coupler. On the receiver side, a polarization-splitting grating coupler is used to handle incoming random optical polarization, and light is fed into a two-port waveguide high-speed photodetector.

Table 12.1 shows the typical optical power delivery breakdown for a 100 Gb/s four-channel parallel transceiver chip, itemized for the components in both the transmitter and the receiver path. We assumed that the electrical modulator driver

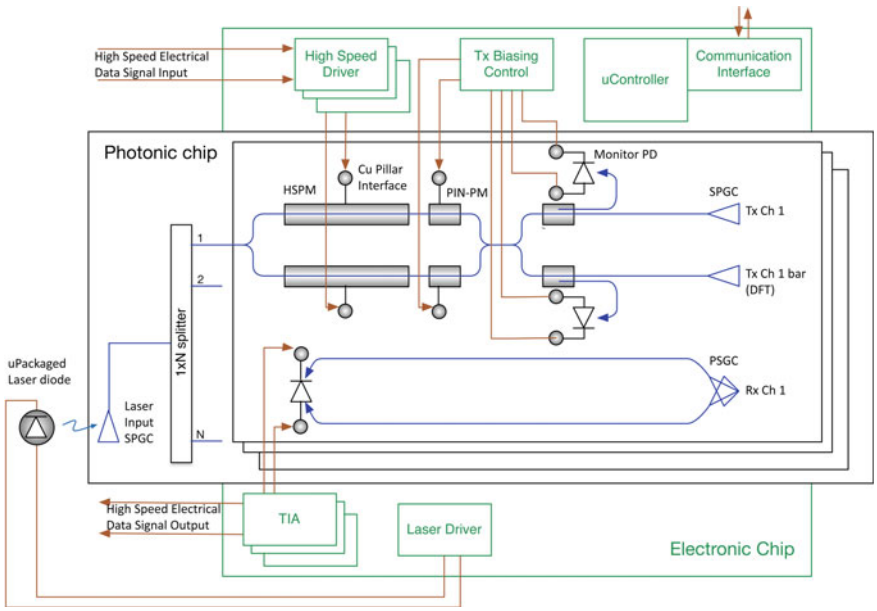

Fig. 12.12 Schematic diagram of 2.5 D integrated advanced silicon photonics transceiver

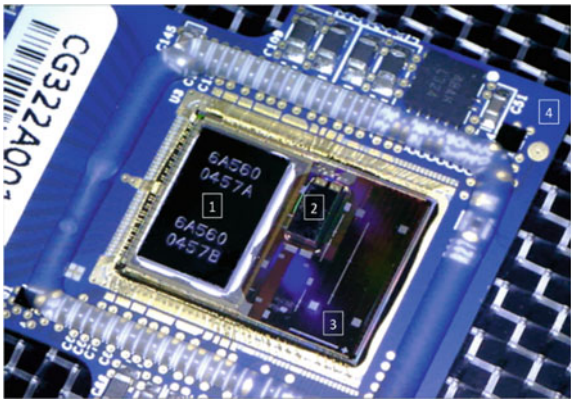

Fig. 12.13 8 × 28 Gbps engine: *1* electronic IC, *2* light source, *3* photonic IC, and *4* PCBA

circuit provides 0.9 V to bias the HSPM diodes, whose total length is 2.5 mm. For the purpose of comparison, we computed the Tx/Rx path loss values in Luxtera's technology as well as for two other silicon photonics platforms, based on the published performance of the components [36, 37]. The superiority of the Luxtera technology is apparent: the transceiver loss penalties in the alternate technologies are about two orders of magnitude higher.

Table 12.1 Comparison of loss penalties for implementations of a 4 × 25 Gbps parallel transceiver in three different process technologies (Luxtera, IME, and IMEC)

Implementation of 4 × 25 G parallel transceiver		Luxtera	IME [36]	IMEC [37]
		Penalty (dB)	Penalty (dB)	Penalty (dB)
Laser input	SPGC	1.8	4.6	2.5
4 by splitter	Two Y-junctions	0.4	1.6	1.0
Modulator	HSPM 2.5 mm	2.1	4.2	8.3
	ER penalty (0.9 V)	2.7	5.1	2.8
	PIN PM (0.25 mm)	0.2	0.1	0.1
Routing	14 mm routing	0.6	1.0	2.1
Light output	SPGC	1.5	4.6	2.5
Total TX loss penalty (dB)		9.2	21.2	19.3
Light input	PSGC	2.7	8.2	7.0
Routing	8 mm routing	0.32	0.56	1.2
Responsivity	PIN-HSPD	−0.2	4.0	3.0
Total RX loss penalty (dB)		2.8	12.7	11.2
Total loss penalty (dB)		12.0	33.9	30.5

The electrical chip contains all of the necessary high-speed drivers and TIAs, as well as the driver for the CW laser and control blocks for the biasing of the various optical systems. In some cases, the electronic chip also contains clock and data recovery (CDR) circuits in the receivers, transmitters, or both.

Beside the functional elements listed previously, there are a number of additional features designed for built-in self-test (BIST) of the chipset as well as features for assisting in optical alignment in the manufacturing flow.

12.5 Light Source for Silicon Photonics

Photonics transceivers require a CW light source as the enabling element of the transmitter. Different integration options are in principle available to combine light sources and CMOS-photonics to construct a photonic transceiver. Various approaches have been pursued and reported by various organizations [38–40]. In our own experimental work, we have found that pairing mature technology such as CMOS with immature laser technologies (e.g., the flip-chip laser approach in Fig. 12.14) results in an overall low maturity of the transceiver system and consequentially low performance (power, thermal performance, spectral performance), reliability, and manufacturability.

Another aspect that favors choosing mature laser and laser packaging technology is the maturity of the transceiver markets itself. Over the last decades, optical transceivers have finally developed volume markets in Fiber-to-The-Home (FTTH), data communications, and telecommunications. Typically, optical transceivers use

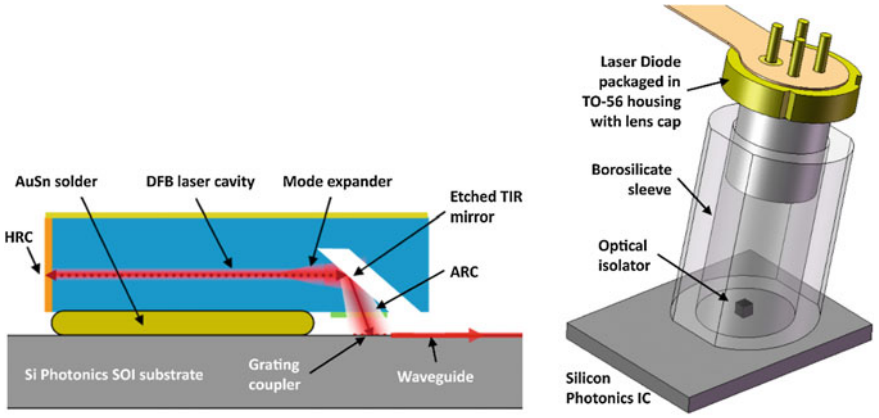

Fig. 12.14 Early Luxtera light source solutions: laser with integrated turning mirror and mode expander directly bonded on silicon photonics IC (*left*). Laser diode in conventional TO-56 housing mounted on silicon photonics IC by a glass sleeve and integrated isolator (*right*)

hybrid assemblies of TOSA, ROSA, and accompanying electronics. The market expectations for product introductions of new technology such as silicon photonics transceivers are based on the already matured photonic product options available, backwards compatibility constraints, as well as roadmap projections. This line of thinking has led us to believe that pairing CMOS-photonics with optical components in use in FTTH applications would allow us, just as in the case with the CMOS technology, to preserve and build upon a mature technology base. This dictated the selection of FTTH-lasers (1490 nm) for our early AOC-transceiver products. This approach had consequences even for the architectural decision of the photonic transceiver. For instance splitting the CW laser light to feed multiple transmitter channels is directly following the approach taken by the FTTH-architecture and for the very same reason of optimizing the cost per channel.

Finally, a packaging technology needed to be chosen. Traditionally, transmitters are packaged inTO-cans and we indeed explored whether TO-cans can be integrated into QSFP-transceivers. We found that the rather large form factor would be very limiting for future scaling of the transceivers and hence explored miniaturized packaging solutions.

MEMS is a technology that has matured tremendously in the last decades and is ideally suited for packaging of micro-optical components, as has been demonstrated in the micro-optical bench approach. MEMS components are produced on the wafer-scale and are, therefore, very amenable to volume production, which is a critical requirement.

We designed a MEMS package (Fig. 12.15) that allows for optimum coupling of the laser light into the silicon photonics CMOS-chip via a grating coupler with an input angle of 13.2° (in epoxy with index n = 1.46), which corresponds to the incident beam angle formed by reflecting the laser off the gold coated (111) silicon mirror facet created by KOH etching of the silicon lid cavity. A high-index and

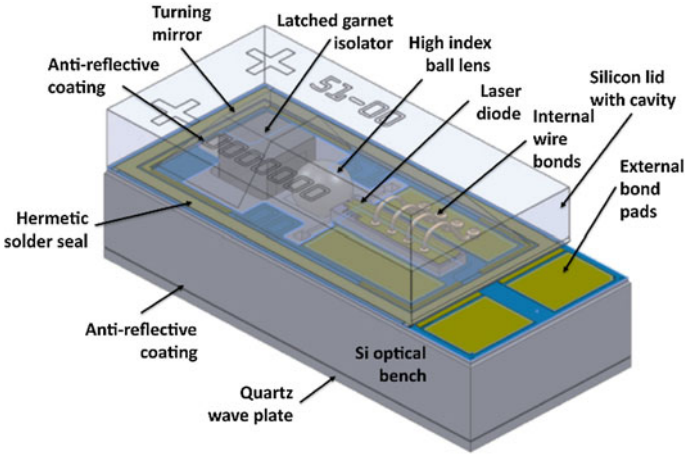

Fig. 12.15 Laser micropackage (LaMP)

tight tolerance ball-lens magnifies the laser output beam to form a beam that is mode size matched to a SMF-28 fiber in the plane of the grating coupler. Initial studies with DFB light sources showed laser instabilities due to reflections from the CMOS die. Insertion of a latching-garnet type Faraday rotator was found to eliminate the laser instability. No polarization analyzer is needed at the input to the CMOS die as the grating coupler acts as a polarizer, since it only supports TE polarized modes and the DFB laser diode itself serves as a polarizer/analyzer for any backward propagating modes. In order to maintain the TE orientation input beam with the Faraday rotator in place, a quartz half-wave plate is incorporated into the bottom of the package that rotates (reciprocally) the input beam polarization.

As the optical system is very sensitive to the axial placement of the laser with respect to the ball-lens, a precise placement of the laser with a tight manufacturing distribution is required. This can only be achieved in wafer-level processing (Fig. 12.16) in a process where the laser diode front facet location and the substrate

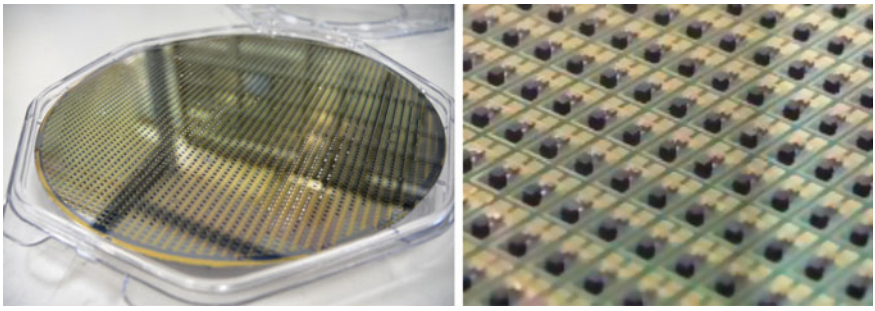

Fig. 12.16 Wafer level LaMP assembly using commercial pick-and-place tools

wafer location are measured with imaging techniques prior to and after the soldering event. With this in-process data, a process control loop can be constructed that allows maintaining the precision of laser placement throughout the assembly of the wafer. We have demonstrated placements of ±1 μm throughout wafers with a CpK of >1.7 for a specification window of ±3 μm.

A low-precision die bonder is used to place all ball lenses into corresponding ball pits formed by KOH etching and the die bonder is also use to place the isolator component. The wire bonding of the laser diodes to pads on the substrate wafer is also carried out on a wafer-level.

The light source packaging takes advantage of MEMS wafer-level packaging (WLP) technologies, such as wafer-to-wafer bonding, which have matured considerably over the last decade. Such a technique is used for bonding a cap wafer to the micro-optical bench wafer. At this point in the process, with all components assembled, the economic value of the wafer requires a high-yielding and robust bonding process to form hermetic cavities for each device. Once the individual devices are formed on the wafer and access to the bond pads external to the cavity is provided, each device can be tested on wafer-level as well. Figure 12.17 shows some measured performance characteristics.

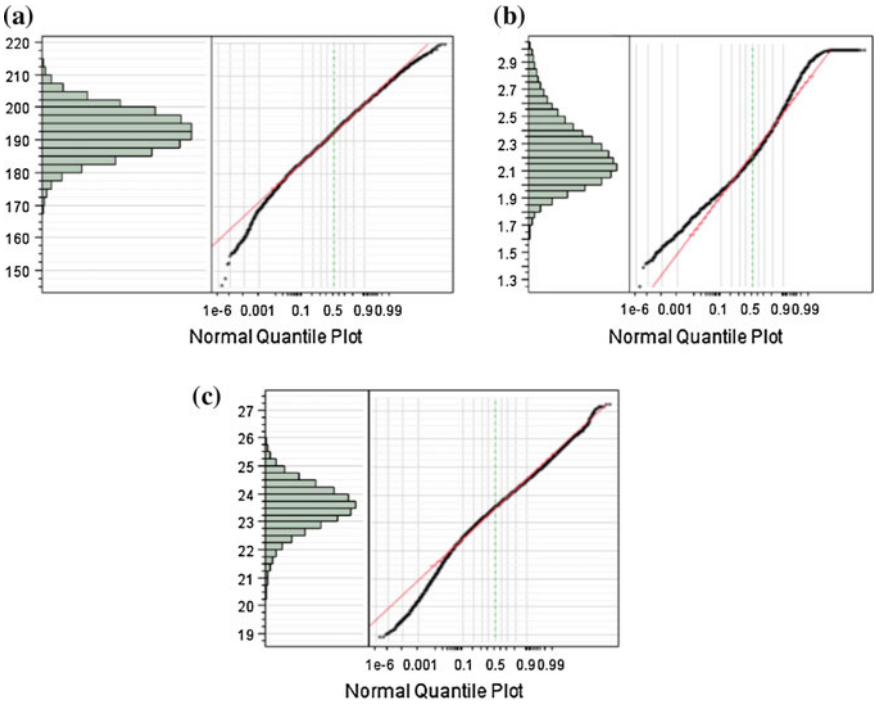

Fig. 12.17 LaMP performance: **a** optical output power (mW) at 480 mA bias current, **b** coupling efficiency (dB), and **c** thermal resistance between laser junction and housing (K/W)

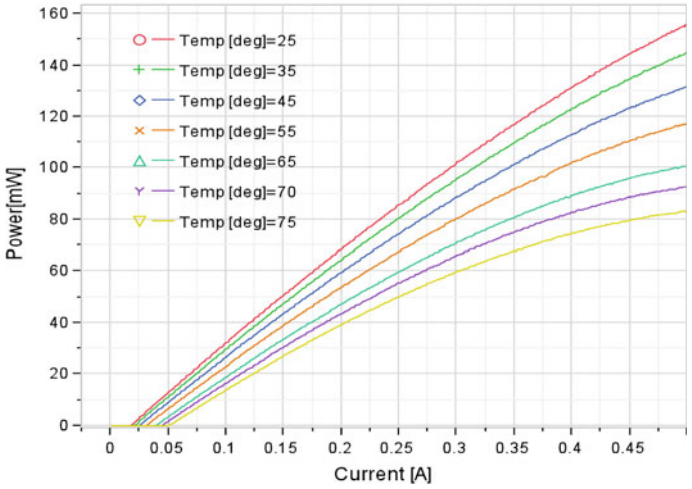

Fig. 12.18 LIV curves LaMP at different housing temperatures

After fabrication, the devices were characterized at different temperatures and a typical measurement of optical power versus temperature and current is shown in Fig. 12.18.

12.6 Packaging

For packaging a silicon photonics chipset, we use a standard printed circuit board as the substrate. The interconnection between IC and PCB is made by wire bonding. For the optical interfaces: light source-to-chip and fiber-array-to-chip, we use active alignment since it has the lowest coupling loss variability and can be executed with high throughput [41]. The fiber array is bonded to the die by an adhesive. Since our technology allows integration of both transmitter and receiver on the same die, we can bond both TX and RX fibers in a single step. The transceiver is usually packaged in a metal housing that provides both electrical and optical connector interfaces, e.g., shown in Fig. 12.19.

The performance of the 100 Gbps transceiver is demonstrated in Table 12.2 and Fig. 12.20. The total power dissipation of the packaged transceiver is <2.8 W.

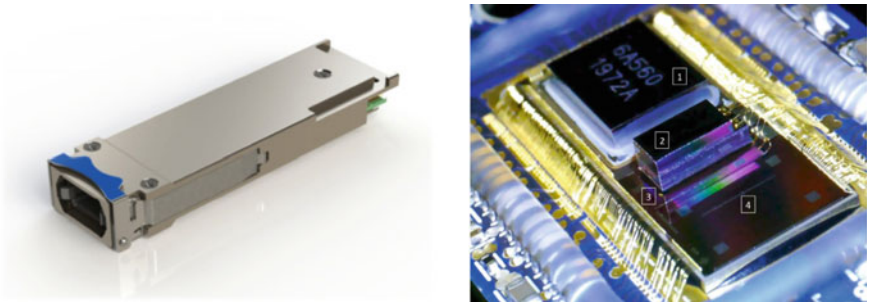

Fig. 12.19 QSFP28 housing for a 100 Gbps (4 × 25 G) single-mode parallel optics transceiver (*left*). Chipset as the optical engine for the QSFP28 module (*right*): *1* electronic IC, *2* LaMP light source, *3* photonic IC, and *4* area of photonic IC for placement of the fiber interface (not shown)

Table 12.2 Typical transceiver performance

Transmitter performance		Receiver performance	
Jitter tolerance	>0.4 UI	Sensitivity	<−13 dBm
Output jitter	<0.2 UI	Output jitter	<0.25 UI
Rise/fall time	<16 ps	Rise/fall time	<15 ps
Extinction ratio	>4.2 dB	–	–
OMA	>2 dBm	–	–

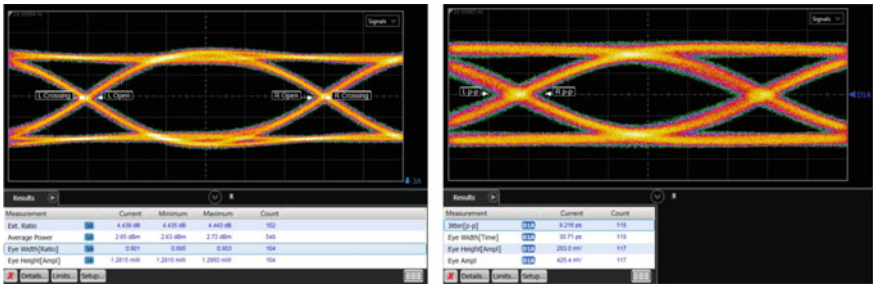

Fig. 12.20 TX (optical) and RX (electrical) eye diagrams of a silicon photonics 4 × 26 Gbps QSFP module

12.7 Conclusions

Silicon photonics is now a mature technology capable of addressing the high volume and high performance needs of current optical interconnect requirements for cloud applications in data centers and wireless systems.

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Chapter 13
Optical Transceivers Using Heterogeneous Integration on Silicon

Gregory A. Fish and Daniel K. Sparacin

Abstract The heterogeneous integration of InP into a silicon photonics platform enables the inclusion of all photonic elements in a cost-effective manufacturing process that fundamentally changes how photonic transceivers can be packaged and integrated into systems. This approach not only allows for best-in-class optical transceiver performance but also at the unprecedented volumes and cost points that are being demanded by modern hyperscale datacenters.

13.1 Introduction

Modern datacenters are creating an unprecedented challenge for optical transceivers requiring not only dramatically lower power and cost to reflect the higher volume and density of interconnections in these applications, but also leading-edge performance (bandwidths greater than 100 Gb/s with a reach of at least 2 km).

As a result of these cost and power pressures, photonic integrated circuits (PICs) based on silicon are already making a commercial impact on the optical transceiver industry since they can integrate nearly all optical functions of the transceiver into a single chip while using the same processes as silicon electronics, thereby leveraging the silicon wafer processing infrastructure and amortizing the accompanying costs of using large ("8–12") wafers. Furthermore, silicon photonics can leverage the low-cost and low-power chip packaging techniques being developed for system-on-chip packaging solutions.

The impact of silicon photonics in datacenter applications, however, has still been limited, held back by silicon's inferior performance compared to traditional InP-based materials for some optical components and its inability to generate light.

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Without integrated lasers and optical amplifiers, the ability of silicon photonics to scale to meet the bandwidth needs is limited. For example, to generate four parallel channels for the 100 Gb/s IEEE optical transceiver standard, four individual lasers need to be aligned and packaged with the silicon photonics chip, and at future bandwidth nodes of 400 Gb/s and >1 Tb/s, even more lasers will need to be packaged with the chips. Packaging silicon photonics with external lasers not only quickly adds cost from added packaging steps—both attaching the lasers and the hermetic packaging of the individual lasers themselves—but more importantly limits the compatibility of the chip with downstream silicon packaging, undercutting one of the reasons to pursue a silicon photonics solution for these applications.

The heterogeneous integration of InP with silicon enables both the manufacturing and performance challenges to be met simultaneously. Best-in-class performance for all photonic functions, including a laser, can be fabricated within the silicon wafer process flow and enable high-bandwidth transceivers to be manufactured using high-yield, established silicon foundry infrastructure from wafer fabrication through packaging and test steps. In other words, by providing a path to allow for full photonic functionality on a silicon substrate, heterogeneous integration enables a scalable photonic solution that can leverage silicon wafer processing, assembly, and test infrastructure for the manufacture of the entire optical transceiver.

13.2 Heterogeneous Integration

An optical transceiver is fundamentally a microsystem with digital electrical, analog electrical, and analog optical functions. In 2010, the International Technology

Roadmap for Semiconductors (ITRS), the organization that publishes the 15 year roadmap for the semiconductor manufacturing industry, recognized the difficulty in achieving such diverse goals in a microsystem with a single technology and introduced the concepts of heterogeneous integration and the More than Moore roadmap as shown in Fig. 13.1.

Silicon CMOS technology has proven to be an extraordinary vehicle to advance digital electrical functions, driven by the cadence of regular reductions in transistor gate length. Labeled “More Moore” by the ITRS, this progression of technology development continues to improve the performance of digital content system-on-chip (SoC) solutions, such as CPUs or other logic functions.

Non-digital applications like RF, sensors, or photonics, however, do not benefit from the miniaturization of gate length and, in fact, use a diversity of materials in addition to silicon such as SiGe, GaN, or InP. These “More than Moore” applications progress on a different development axis. Photonics is a strong example of a More-than-Moore technology—optical components are fixed in size by the wavelength of light and do not benefit from reduction in feature size. In fact, processing photonic components on the most advanced CMOS process node only increases the cost of those components with no major benefit to performance.

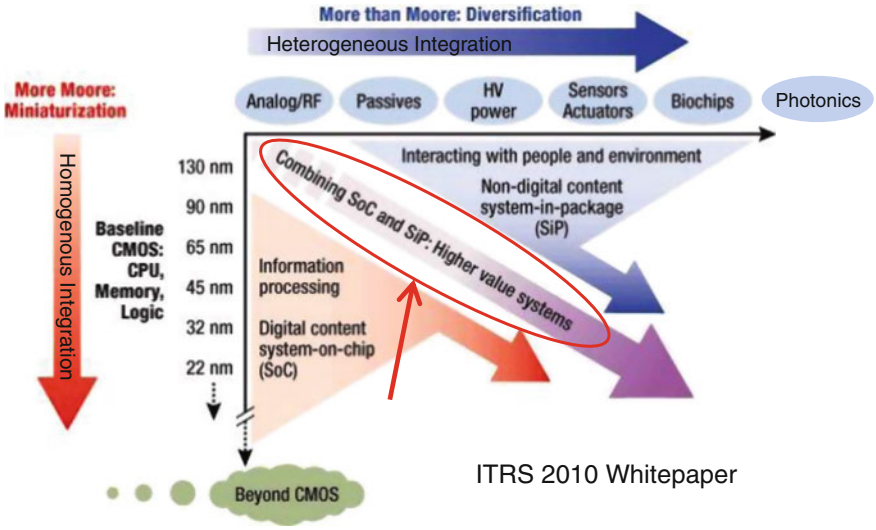

Fig. 13.1 Microsystem roadmap comprised of digital ("More Moore") components which reduce in size and power, and non-digital ("More than Moore") components which add functional diversification. In combination as a system-on-chip (SoC) or system-in-package (SiP), these microsystems enable higher value relative to what a single-chip technology can deliver

The complete transceiver microsystem, however, does benefit from the close integration of CMOS digital electronics for signal processing, SiGe analog electronics for RF amplification, and photonics to achieve a communication bandwidthdistance product that cannot be achieved with electronics. The ITRS laid out an optimized way to combine different technologies on the More-than-Moore roadmap with the standard SoC technologies of the More-Moore roadmap using heterogeneous integration, where different chips are combined in a system-in-package (SiP) to create higher value systems. The combination of VCSEL arrays with digital switch chips by COMPASS EO [1] is an example of SiP heterogeneous integration.

A more prominent market example, however, is the integration of diverse silicon-based chips using 2.5D or 3D SiP packaging technology, which is already making a large impact in the mobile industry [2]. In order for photonics to make a similarly large market impact, it needs to align with high-volume industry packaging methods. In short, photonics needs to be "another silicon chip" compatible with existing 2.5D or 3D packaging methods.

Since the highest performance components for photonic transceivers are made with InP material and not silicon, photonics needs to leverage heterogeneous integration in a second way and integrate diverse materials into the same SoC and maintain compatibility with SiP manufacturing. In other words, by using heterogeneous integration to combine best of breed components onto a silicon substrate, the resulting chip can leverage the silicon electronics assembly ecosystem to

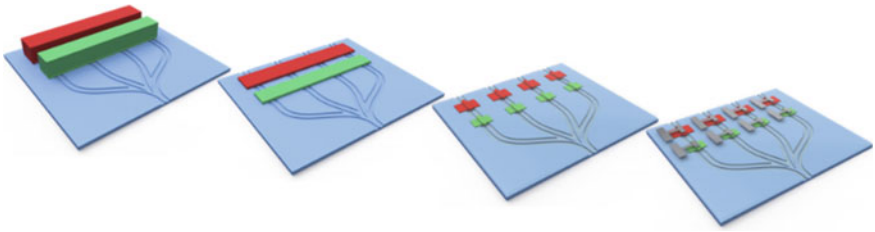

Fig. 13.2 Aurrion's heterogeneous integration process: 1. Die placement 2. Substrate removal 3. III-V processing 4. Interconnect

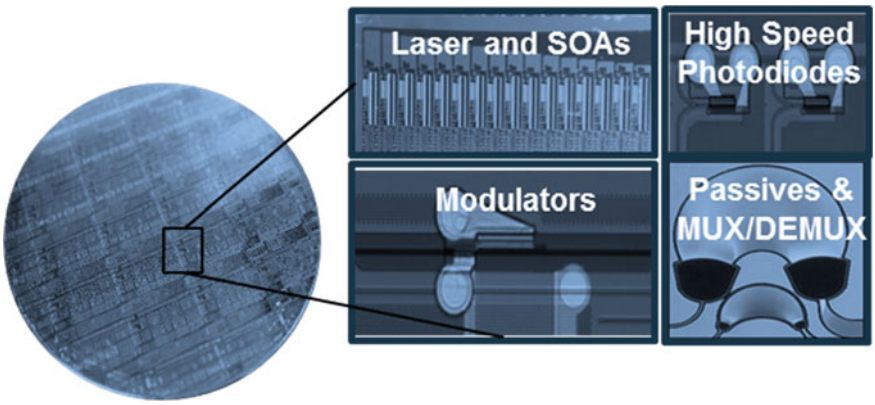

Fig. 13.3 Demonstration of a heterogeneous integration platform for silicon photonics: Processed on silicon wafers using foundry infrastructure, optimized III-V materials for active components with silicon photonics, heterogeneous III-V components on silicon match and even exceed the performance of a native III-V substrate

facilitate low-cost packaging. The Aurrion version of this process is shown in Fig. 13.2.

The basic underlying photonic circuit, comprised of low-loss silicon and dielectric waveguides, is generated on a silicon-on-insulator (SOI) wafer, leveraging standard foundry infrastructure. Then, in order to add InP functionality to the photonic circuits at the wafer-scale, 'chiplets' of custom unprocessed InP epitaxial material are bonded to the silicon photonic circuit. Using standard semiconductor lithography and etch steps, InP-based chiplets are processed in parallel to form lasers, optical amplifiers, modulators, and photodetector devices. In every case, they are registered and optically coupled to the underlying waveguides. Once that has been carried out, further processing steps encapsulate InP with dielectric materials, and also form metal interconnects and contacts for driver and control circuitry.

As a result, complete photonic circuits can be processed on a silicon wafer (see Fig. 13.3) in order to be compatible with downstream silicon packaging.

13.2.1 Components

Critical to having complete photonic circuits is having a complete library of the necessary optical components. A key advantage for any silicon photonics platform is its ability to leverage the high precision process tooling of a silicon foundry to produce the complex passive components needed for a highly integrated photonic circuit. The critical passive components needed for WDM such as arrayed-waveguide gratings (AWGs) can be processed with both high performance and high yield, as shown in Fig. 13.4. Such passive components are discussed extensively in the silicon photonics literature.

Many active components, especially modulators, have also been demonstrated in silicon [3] but despite extensive engineering work, these active components do not have the same performance as their InP-based counterparts. The heterogeneous integration of III-V materials into a silicon photonics platform, however, can bring best-in-class active components to a silicon substrate. Such components are discussed below.

13.2.2 Lasers

Lasers are the first key building blocks of a complex photonic circuit. Figure 13.5 shows the laser output power versus current from a heterogeneously integrated laser on silicon at 20 and 80 C. The laser has greater than 25 % wall plug efficiency at 20 C and greater than 13 % wall plug efficiency at 80 C for output powers in the vicinity of 10 mW [4], which rivals the state of the art for lasers fabricated on traditional InP substrates.

The SMSR of these lasers is consistently above 40 dB and the RIN is below –140 dB/Hz, which is adequate for typical WDM datacom applications. All of these lasers are also designed to be wavelength stabilized using feedback structures

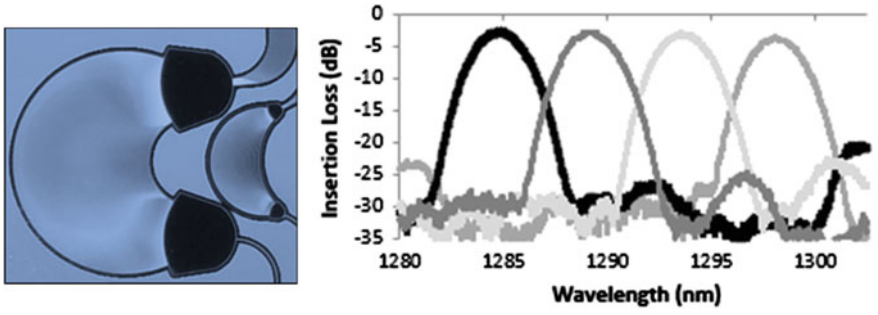

Fig. 13.4 High-yield complex MUX/DEMUX structures manufactured using 200 mm fabrication tooling: low-loss (<1 dB/cm) silicon waveguides and low-loss crossings

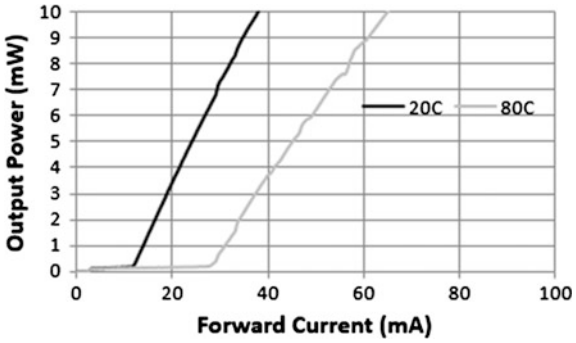

Fig. 13.5 Laser output power versus applied bias current for a heterogeneously integrated InP-based laser on silicon

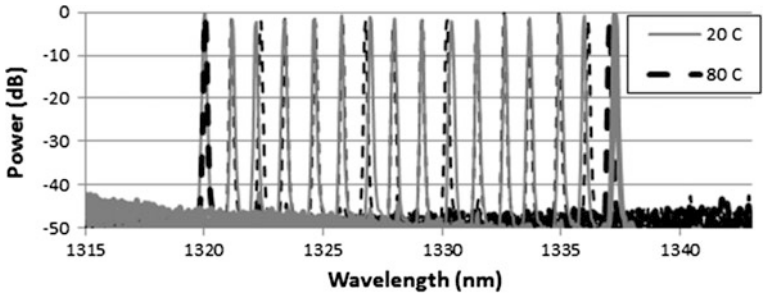

Fig. 13.6 Optical spectrum of uncooled, wavelength-stabilized lasers with 200 GHz channel spacing

designed into the underlying silicon photonics, and Fig. 13.6 shows how the wavelength of operation can be maintained at 20 and 80 C. The wavelengths are also stabilized at all temperatures in this range.

This unique capability allows these lasers to operate in a dense WDM mode without requiring a thermoelectric cooler, thus saving a tremendous amount of power and avoiding packaging complications. In many ways, this on-chip, uncooled WDM laser is poised to disrupt the photonic industry, as it fundamentally changes the economics of implementing a WDM solution.

13.2.3 Semiconductor Optical Amplifiers

The heterogeneous integration process also enables semiconductor optical amplifiers (SOAs), a critical missing function on silicon photonics that can be used for amplification for transmitters or as pre-amplification for receivers to extend the

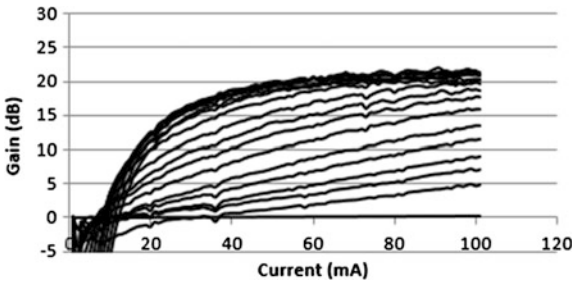

Fig. 13.7 Examples of gain performance from SOAs on silicon using the Aurrion heterogeneous integration technology

reach of a transceiver. Figure 13.7, for example, shows the performance of semiconductor optical amplifiers that exhibit a gain of 300 dB/cm and SNR of >35 dB.

13.2.4 Modulators

In addition to lasers, the platform contains several high-performance modulator designs integrated into the same photonic integrated circuits with the lasers. One example of this is an electro-absorption modulator (EAM) in the O-band which utilizes the band edge absorption of InP materials to form very compact ($\sim 10\times$ smaller) devices than can typically be achieved with silicon photonic Mach–Zehnder modulators.

Figure 13.8 shows the electro-optic frequency response of an EAM that was made simultaneously with O-band lasers. This modulator has a 3-dB bandwidth of more than 35 GHz.

Figure 13.9 shows example eye diagrams taken from this modulator with two different drive voltages. With a 3 V drive the EAM has an extinction ratio of 11 dB,

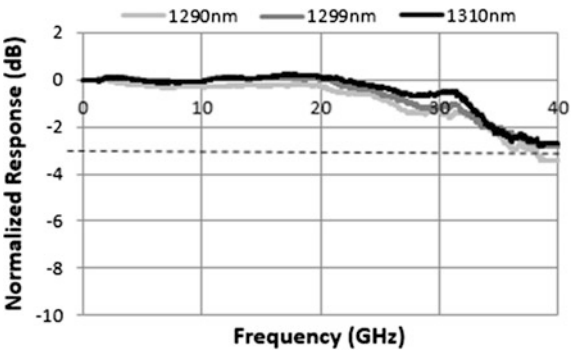

Fig. 13.8 Electro-optic frequency response of a heterogeneously integrated electro-absorption modulator with 3-dB bandwidth greater than 35 GHz

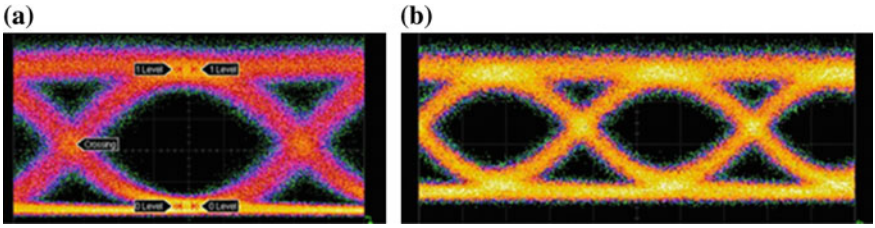

Fig. 13.9 Eye diagrams of a heterogeneously integrated electro-absorption modulator operating at 25 Gb/s with **a** an 11 dB extinction ratio with 3 V drive and **b** a 6 dB extinction ratio with 1.5 V drive

and with a 1.5 V drive its extinction ratio is 6 dB, which is more than adequate for typical datacom applications.

13.2.5 Photodiodes

High-performance photodiodes can also be formed using the same heterogeneous integration method. Figure 13.10 shows the optical-electrical response of a heterogeneously integrated photodetector, which has a 3-dB bandwidth of more than 35 GHz. These devices were also tested with a receiver IC formed using IBM's 130 nm BiCMOS process [5]. In this configuration open eye diagrams up to 60 Gb/s were demonstrated, as shown in Fig. 13.11. The sensitivity for 10^{-12} BER was –13 dBm at 30 Gb/s and less than –4 dBm at 60 Gb/s [5].

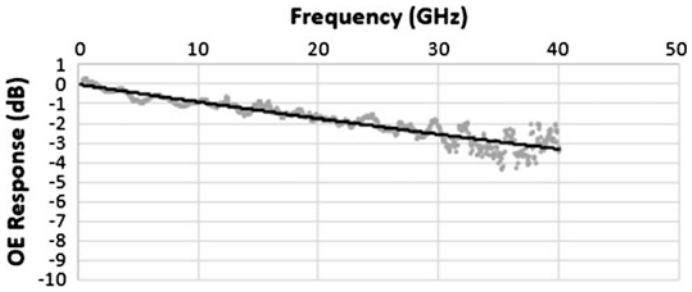

Fig. 13.10 OE frequency response of a heterogeneously integrated photodetector, showing greater than a 35 GHz 3-dB bandwidth

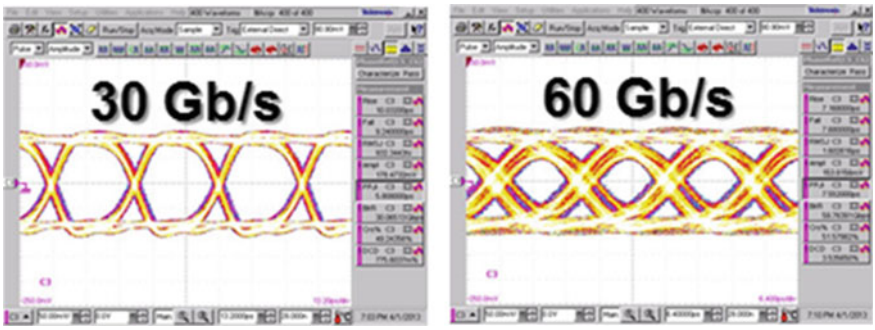

Fig. 13.11 Eye diagrams of a heterogeneously integrated photodetector integrated with SiGe driver circuit, operating at 30 and 60 Gb/s [5]

13.2.6 Circuits

One of the failings of early silicon photonics circuits was a focus on the development of optimized photonic library components without consideration of the integration of these components into a complete circuit. This focus on components in isolation led to clunky, unoptimized systems that delayed the introduction of silicon photonics-based products. A key aspect of component development is the ability to enable flexibility and scalability of circuits that are optimized for manufacturing. As a result, multiple challenges and considerations for circuit design must be considered (Fig. 13.12).

Integration Considerations

The optimization vectors of components often point in conflicting directions with a primary example being that of thermal impedance. Lasers and SOAs benefit from

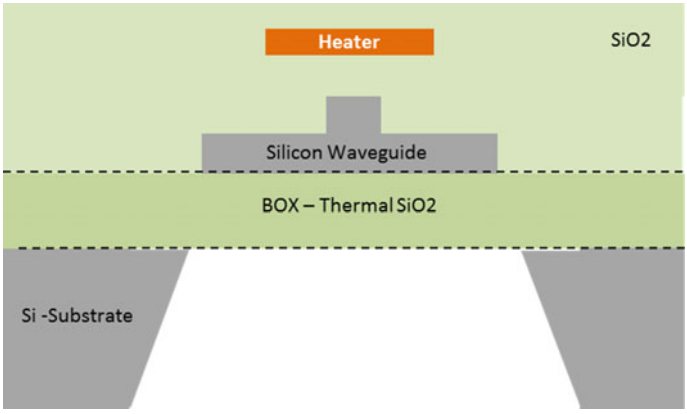

Fig. 13.12 Schematic of a silicon photonics wafer cross-section with a localized backside etch process to remove the substrate under thermal tuning structures, which increases the tuning efficiency by increasing the local thermal impedance

minimized thermal impedance since optical gain mechanisms roll off at higher temperatures. However, thermal tuning structures like microrings or optical switches are fundamentally based on getting a large waveguide index change with a small thermal change and benefit from maximized thermal impedance. A photonic circuit integration platform, therefore, must be able to satisfy conflicting optimization vectors simultaneously in order to achieve the best overall system performance. To satisfy the thermal impedance issue, for example, multiple groups have leveraged the straightforward processing of the backside of a silicon wafer to create different thermal environments within a given circuit [6].

Another critical example is the handling of polarization diversity, which impacts the design of the waveguide itself. Waveguides that can handle diverse polarizations require a square or close to square cross-section to ensure both polarizations have the same group velocity throughout the circuit. This constraint results in waveguides which are fairly thick, impacting a number of design considerations including the efficiency of carrier injection components, which can substantially benefit from thinner waveguides. Furthermore, many silicon photonic platforms use rectangular waveguides to minimize transmission losses that arise from the optical mode overlapping with roughness on the etched sidewalls. Choosing a square cross-section waveguide for polarization diversity can trade with a higher overall insertion loss.

For platforms that use thin, rectangular waveguides, managing polarization through the transmitter is fairly straightforward since the laser output polarization is typically fixed. If the laser is off-chip, however, careful design of the coupling between the laser output and the silicon photonics chip is required and may require a polarization maintaining fiber [7] or more complex means to maintain a single output polarization. Aurrion's heterogeneously integrated lasers are naturally TE-polarized, so the full transmitter chain of laser, modulator, compact multiplexor for WDM, and optional SOA can leverage an optimized thin silicon waveguide.

Incoming polarization at the receiver, however, cannot be predicted and varies with time. A thick, square polarization-insensitive waveguide can accommodate an arbitrary polarized signal at the expense of active and thermal tuning device efficiency. As a result, most silicon photonics transceiver solutions use this approach and separate chips for the transmitter and receiver to account for the incompatible waveguides [8]. In order to avoid this trade-off and gain the benefits of using a single chip, structures to handle polarization diversity can be designed into the platform. For example, two-dimensional grating couplers like the one shown in Fig. 13.13 can be used to accept an incoming signal with an arbitrary polarization and split the optical mode into two separate waveguide paths, which correspond to the TE and TM polarization states. This approach requires two optical receiver paths, which terminate at the same photodiode array. For WDM signals, each path can be carefully routed to a compact demultiplexer. Although thin, high confinement waveguides enable these demux structures to be fairly compact, the footprint can be further minimized by using a bidirectional AWG [9].

The key circuit integration challenge, however, is in the optimization of active components. Lasers, modulators, and photodiodes nominally require three types of

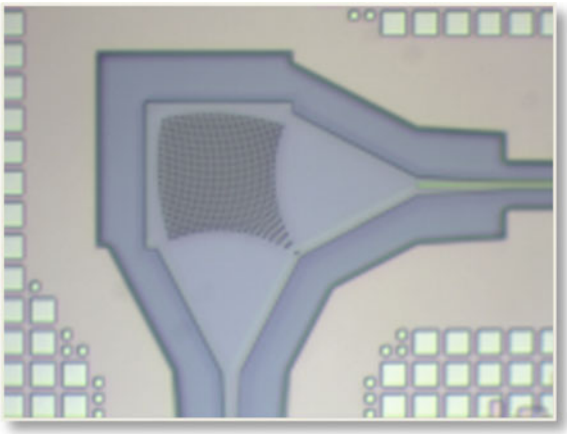

Fig. 13.13 Micrograph of a two-dimensional grating coupler component, which functions to both couple light from a fiber and separate and converge the two incoming polarizations into two TE modes propagating on separate waveguides

optimized epitaxial material. Vendors using traditional forms of InP-based integration have addressed this challenge with complicated regrowth techniques [10], which substantially lower yield and increase the cost of the chip. Silicon photonics platforms can use non-epitaxial material approaches such as carrier injection [11] or field effect devices [12] for the modulators and germanium epitaxial growth for either the modulators or photodiodes [7, 8] but with an increased number of overall processing steps (impacting yield and cost). These approaches must also be designed to be ultimately compatible with the laser integration, which is not always straightforward. By heterogeneously integrating multiple epitaxial materials, as is done on Aurrion's platform, each individual component can be optimized separately yet processed at the same time to minimize cost. This optimization further impacts the achievable wavelength range of the circuit in WDM applications. For circuits that require a standard CWDM grid, which has four lasers that span 80 nm of wavelength range, for example, a single epitaxial material will not be suitable in performance for all four of the lasers. By heterogeneously integrating multiple epitaxial materials for the lasers as well as the materials for the modulators and photodiodes, a circuit that is simultaneously optimized for both performance and minimal processing can be manufactured.

Control Considerations

The components in transceivers always require some level of control to either level the optical power or achieve specific functions like wavelength tuning or optimizing the modulator bias. In an integrated platform, the interactions of these various controls need also to be considered for overall circuit design.

In particular, for uncooled photonic circuits, where fluctuating temperature can result in varying drift of different components within a circuit, the interaction of the components needs to be understood at the system level to ensure the lowest overall power, leading to a control granularity versus power consumption trade. The optical output power control of the laser, for example, can typically be managed at a coarser level than a temperature-sensitive ring resonator filter control circuit.

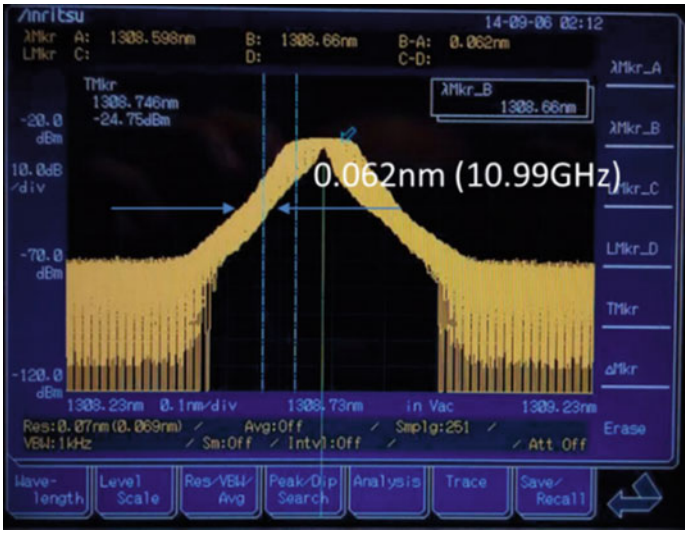

Fig. 13.14 Laser spectrum measurement of an Aurrion uncooled laser with closed-loop control resulting in an 11 GHz laser wavelength uncertainty. Reducing this uncertainty is feasible using control electronics with higher precision

Ultimately, these trade-offs can lead to a given optical function resulting in different optimized photonic and electronic circuit architectures when addressing differing applications.

In addition, the overall architecture needs to be understood so that proper inputs to the control circuitry can be allocated. Typically, monitor photodiodes (MPDs) are added sparingly within a circuit to provide feedback for control. In an integrated platform, however, there is an opportunity to add as many as needed. Key design concerns are placing the MPDs to provide sufficient signal information across the entire circuit, with redundancy where needed, while minimizing the overall power and complexity of the system.

A third consideration is referencing the circuits to absolute wavelength and power references. Adding integrated references can occupy significant package volume, whereas calibration adds manufacturing time and cost.

When all of these control aspects are considered, the result can be fairly disruptive, such as the uncooled, wavelength-stabilized lasers that Aurrion has demonstrated on its platform [4]. Figure 13.14 shows one such laser wavelength locked to within 11 GHz during operation in a transmitter.

Packaging and Test Considerations

As discussed previously, perhaps the most important but most overlooked consideration for an integration platform when targeting lowest cost is the interaction with the downstream assembly and test manufacturing steps.

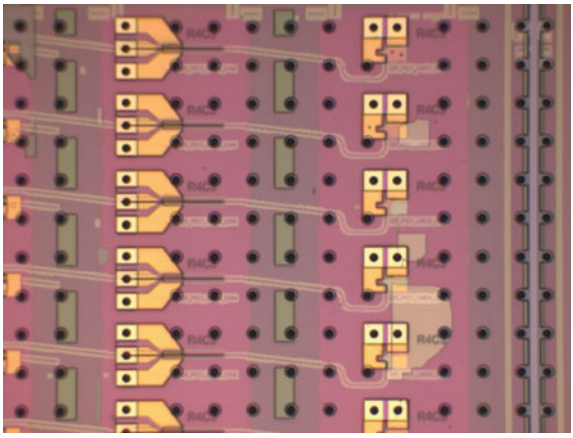

Fig. 13.15 Photograph of a PIC with arrays of bumped electro-absorption modulators and photodiodes ready for flip chip assembly

Packaging considerations are discussed in more detail in the next section, but the key point when trying to minimize packaging cost is to stay compatible with the established processes already used for electronics packaging with ideally the thermal path upwards, and the electrical path downwards. As a result, the placement of components in the circuit must be managed thermally to ensure proper balancing across the chip and electrically to minimize RF signal paths to the corresponding electrical chips. Flip-chipping the PIC enables high I/O and the control complexity for higher functionality, but the placement of the bumps must be considered for both stress and thermal considerations. Bumped devices such as modulators and photodiodes are shown in Fig. 13.15.

The impact of circuit design on testing can be equally important in terms of achieving the lowest overall cost of the transceiver. To first order, the circuits must be designed to be compatible with high-speed, automated testers common to the electronic IC industry, but algorithms must be designed that allow testing at the circuit level to avoid individual interrogation of all the components, which would quickly undercut the low-cost flow. Such approaches are common to the electronic IC industry, which incorporates self-test and other features into the circuits to minimize test time.

Enabling Novel Functionality

Although the previous discussions focused on the challenges associated with integrating diverse optical components into circuits, if the platform is designed correctly to accommodate such diverse functionality, it can actually enable novel functionality. A previously discussed example is that of self-test. If both the transmitter and receiver are integrated on the same chip, loop-back functionality can be added with a simple waveguide switch in order to enable extensive on-chip testing prior to packaging, lowering overall cost, or even self-test in deployment, thereby increasing the intelligence of a network. Similarly, using the same switch, spare channels can be switched-into to provide greater reliability or even enable bandwidth-on-demand functionality.

The ability to integrate disparate wavelength range components adjacent to each other dramatically increases the potential application space. For example, high-volume fiber-to-the-home (FTTH) systems rely on systems on the customer end that have 1490 and 1550 nm photodiodes for receiving the incoming signal and 1310 nm lasers for the uplink signal. On typical integration platforms, these vastly different epitaxial requirements could not be integrated together, but the heterogeneous integration platform enables both to be processed together in a single, low-cost circuit [13].

Example: 100 Gb/s Uncooled WDM Transceiver PIC

An example of a complete photonic transceiver circuit that incorporates the considerations discussed above is shown in Fig. 13.16. This particular circuit contains four wavelength-stabilized lasers that can lock to a grid as tight as 200 GHz in spacing. The output of each laser is routed to a 25 Gb/s EAM, combined with an AWG into a single waveguide, and routed to an optical coupler such that the total single-fiber bandwidth of the chip is 100 Gb/s. A similar optical coupler is used for the receive side, which is demultiplexed by an AWG and routed to an array of photodiodes.

Without significant redesign of the components, similar circuits can be constructed for a high overall bandwidth, which is a critical measure of proper circuit design. As shown in Fig. 13.17, such scaling can extend in any combination of three different vectors: number of fiber connections, data rate per channel, and wavelengths per channel. On Aurrion's platform, the number of fiber connections can be scaled by simply increasing the number of vertical couplers in the array. The speed of the individual channels can be increased by leveraging the high-performance InP-enabled electro-absorption modulators, which currently have 3 dB bandwidths >35 GHz, suitable for 50 Gb/s NRZ or PAM-4 encoding. Finally, by leveraging the ability of the heterogeneous integration platform to create arrays of uncooled WDM lasers that are processed simultaneously, the number of channels can be increased by simply increasing the number of components within the circuit (Fig. 13.18).

Fig. 13.16 Photograph of a 4 × 25 Gb/s transceiver PIC developed by Aurrion that integrates lasers, modulators, a multiplexer, a demultiplexer, photodiodes, and optical fiber coupler devices on a single silicon chip

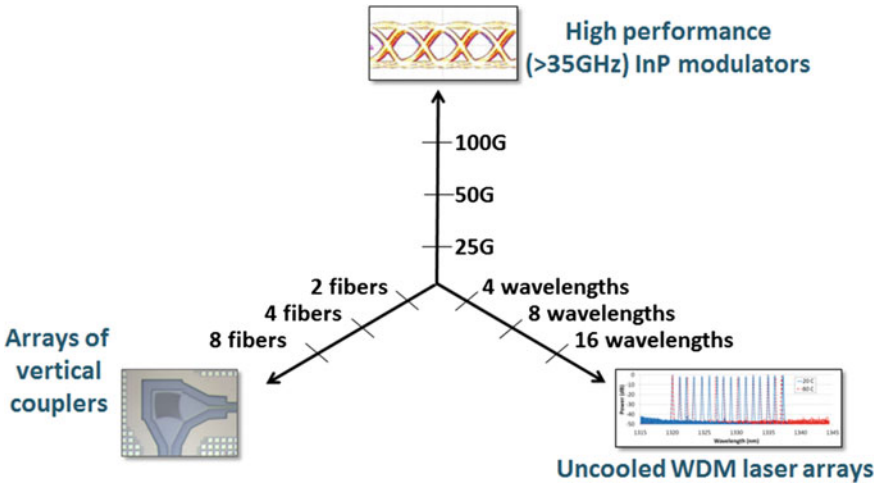

Fig. 13.17 Design space in which optical transceivers with large aggregate bandwidths can be designed and constructed with Aurrion's heterogeneous integration platform

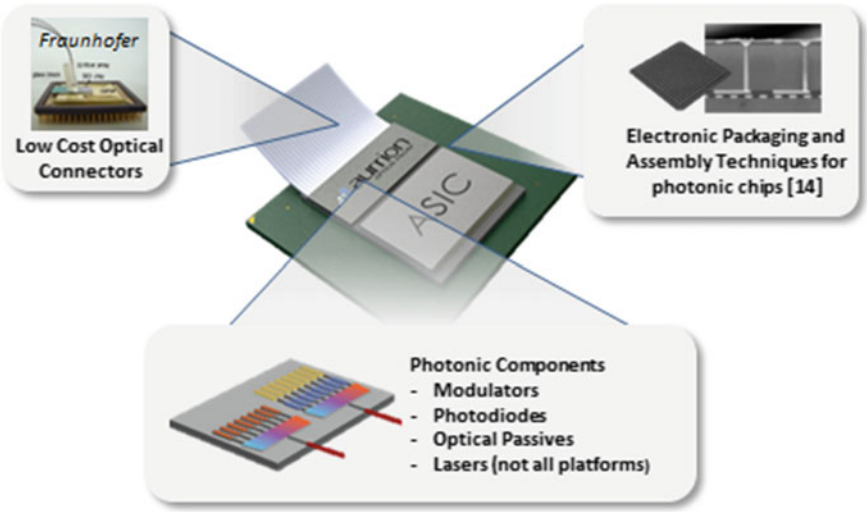

Fig. 13.18 Aurrion's vision of a full photonic transceiver in which all components (photonic and electronic) can be manufactured using silicon wafer foundries and silicon IC packaging infrastructure to enable a technology solution that can deliver high bandwidth at low power and cost

13.3 Packaging

Historically, the publicized advantage that silicon photonics technology has over traditional InP-based photonics is that it leverages the enormous investments in silicon-based IC wafer processing to enable high-volume, low-cost production of complex semiconductor circuits. While most silicon photonics efforts focus on fabricating their circuits with the silicon wafer foundries, it is arguably more important to leverage the low-cost assembly and test infrastructure developed for the silicon IC industry as packaging and testing is typically the costliest part of many photonic products. One of the biggest barriers for silicon photonic transceivers to fully leverage silicon packaging approaches, however, is the inability to integrate all photonic components on a single chip; specifically the light source. By requiring hybrid packaging to add the light source, these solutions are then required to employ the very optical packaging techniques (lens, active alignment, hermiticity) that are responsible for the high cost of InP-based photonic solutions, and diminishes the incentive and benefits of integrating the remaining photonic functions. However, by starting with a complete silicon photonic integration platform using heterogeneous integration, leveraging of silicon foundry, assembly, and test infrastructure is feasible and enables a path to truly low-cost, high-performance optical transceivers.

Heterogeneous Systems in Package

A further advantage of having silicon photonic-integrated circuits that are fully compatible with advanced silicon packaging lies in the ability to incorporate them into heterogeneous systems-in-package (SiP), where the functionality of the microsystem is partitioned into the silicon IC technology that is best suited for the task. These SiP solutions can be as compact as and more cost-effective than fully monolithic ICs. The evolution of this packaging transformation from discrete components toward SiP is shown in Fig. 13.19. For several applications, the forecasted processing power requirements of these multichip modules using SiP technology will exceed the electrical I/O bandwidth permitted by a high-density ball-grid-array (BGA) and photonic I/O solutions are being considered as a solution to address this bandwidth bottleneck. Thus, going forward we will see a transition from making photonic modules that contain electronics to electronic SiP that now contain photonics. A key requirement to this vision requires the photonic IC technology to seamlessly integrate into these advanced packages.

Anatomy of a Package

The challenge of photonic packaging stems from the multi-physics environment (thermal, electrical, optical, mechanical, etc.) that is typical of all packaging, but it now includes components that are more sensitive to stress and temperature than typical electronic ICs and the requirement to maintain micron and even submicron alignments of the optical connections out of the package. Traditional photonic packaging has solved these problems by enclosing the photonic components in stiff, hermetically sealed enclosures with feedthroughs for both the optical and electrical

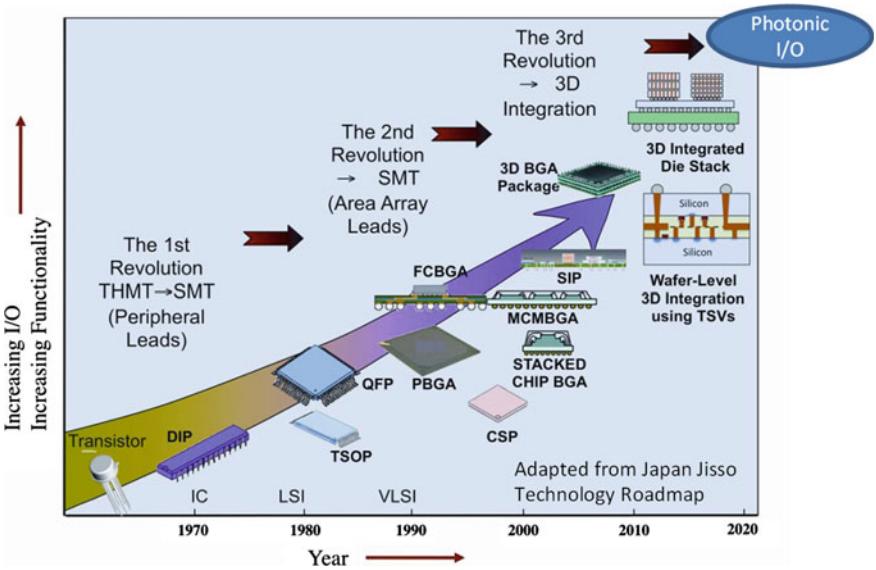

Fig. 13.19 The evolution of the packaging transformation toward system-in-package (SiP)

interconnects. For temperature sensitive photonic chips a thermoelectric cooler (TEC) is added to maintain constant chip temperature in the presence of ambient temperature changes. Typically, these packages remove heat from the bottom side of the package with a TEC and the optical connection is to the side through an edge-coupled facet. The electrical interconnect is also from the side for smaller pin counts, such as with a butterfly package, or through a land grid array (LGA) for larger pin counts. The use of a BGA-based interconnect is typically not possible due to the presence of the epoxy-attached optical fiber interconnect, which is not compatible with solder reflow. The main driver of this architecture is (1) the PIC cooling requirement to maintain operational stability and (2) hermetic environments for reliability of the exposed chip facets. These two requirements significantly increase the complexity and cost of the electrical interconnect for the package. An example of traditional photonic package architecture can be seen in Fig. 13.20, which depicts a block diagram of the package architecture with various optical, thermal, and electrical paths that arise from design trade-offs associated with compound semiconductor photonic integrated circuits and components.

For traditional silicon photonics, hermetic environments are not needed for the Si die, so packaging solutions have evolved to localize the hermetic package to the external light source only. As a result, the package architecture no longer needs a majority of the electrical connections through a hermetic package, which saves cost and provides flexibility in how the optical connector can be attached. To minimize optical junctions (and loss) with an external laser, the optical interconnect to the laser and fiber is through the front of the die and heat is dissipated through the back

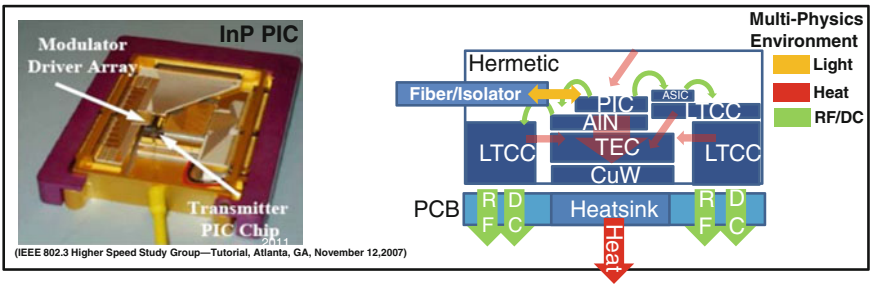

Fig. 13.20 Analysis of the packaging of a photonic system-in-package (*left*) distilled to a block diagram of the architecture (*right*) containing an InP-based photonic integrated circuit. *LTCC* low-temperature co-fired ceramic; *TEC* thermoelectric cooler; *AlN* aluminum nitride; *PCB* printed circuit board; *CuW* copper tungsten

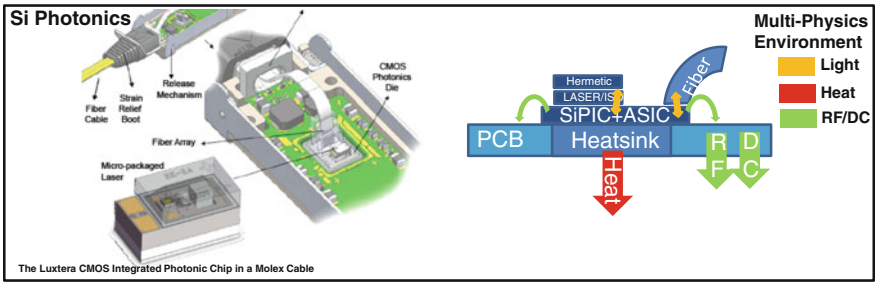

Fig. 13.21 Analysis of the packaging of a silicon photonic system-in-package (*left*) distilled to a block diagram of the architecture (*right*) containing a silicon-based photonic integrated circuit with an external laser. *PCB* printed circuit board; *SiPIC* silicon photonic integrated circuit, *ASIC* application-specific integrated circuit, *ISO* isolator

of the silicon photonic IC. As a consequence of the orientation of the optical interconnect to the laser, the electrical interconnect to the silicon photonics is forced to be wire bonded around the periphery of the die and flip chip-based interconnects are not possible as the laser and fiber block access the electrical interconnect. A schematic of the typical silicon photonic package architecture can be seen in Fig. 13.21, which depicts a block diagram of the package architecture with various optical, thermal, and electrical paths that arise from design trade-offs associated with a silicon photonic die with an external light source.

As industry roadmap projections for electronic systems in package begin to exceed the bandwidth capabilities of BGA interconnects and perceive the need for photonic I/O out of the package, it is instructive to examine an advanced electronic/photonic heterogeneous system in a package. As an example, Fig. 13.22 shows an FPGA-based product with electronic transceivers for data transmission out of the package. This arrangement is chosen to optimize process nodes and supply voltages for the FPGA and transceiver chips in this multi-chip module.

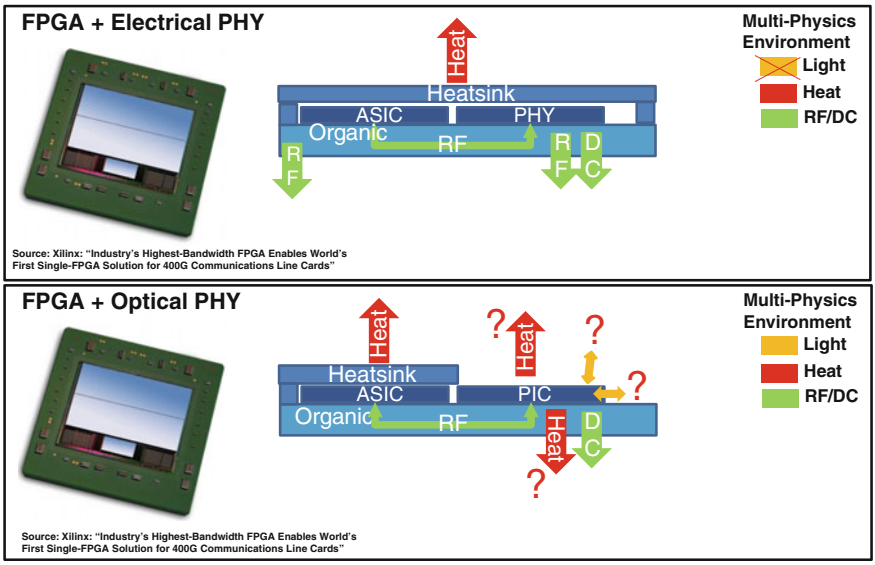

Fig. 13.22 **a** Analysis of the packaging environment of a heterogeneous system-in-package of an FPGA and electrical PHY transceiver. **b** A corresponding version envisaging inserting an optical transceiver into the heterogeneous system-in-package. *FPGA* field programmable gate array; *PHY* physical layer transceiver

A key design factor for virtually all high-performance systems in package architectures is that the heat is removed out of the top of the package, since the heat sinks required for system operation are much larger than the package and the sheer number of pins require flip chip and BGA-based interconnects, which act as poor heat conduits.

As we contemplate how to add photonics to these packages, it becomes clear that the optical interconnect packaging solution must be compatible with a flip chip electrical interconnect to fit and minimize the RF path length within these dense packages. Hence, the incorporation of all photonic components (including the laser), through heterogeneous integration, is required for the entire photonic circuit to have electrical I/O that is flip chip compatible. It follows from these architecture shifts that the optical I/O should ideally be oriented out of the photonic chip through the back of the die, thereby sharing the optical interface with the thermal interface, rather than the electrical interface where real estate is precious. In total, the photonic IC can now be packaged similar to a flip-chipped electronic IC with the addition of an optical connector that sits above the photonic IC. Figure 13.23 shows an example of a packaged photonic IC developed by Aurrion with a flip chip interconnect that is compatible with traditional electronic IC packaging.

An added benefit of this configuration is that it allows the optical interconnect to now leverage the technologies built for low-cost VCSEL-based interconnects (with tolerance enhancements for coupling to single mode fiber), as the optical connection

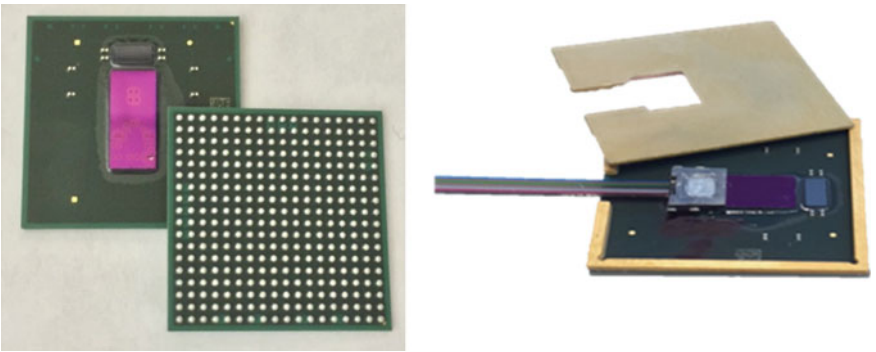

Fig. 13.23 Example of a packaging approach for photonics that simultaneously achieves the goal of best-in-class performance with low-cost, silicon-based packaging processes. A high-bandwidth 100 Gb/s silicon photonics chip is flip-chipped onto a BGA substrate using standard electronics methods

is vertical instead of in-plane. One of the advantages of these connectors is that the fibers' assembly of the connector can be attached to a mechanical interface after the transceiver is reflowed, and attached to the PCB enabling the use of a BGA required for low-profile and high pin count packages [14].

13.4 Conclusion

With optical transceivers facing an unprecedented challenge to meet industry performance and cost requirements, it has become critical for photonics manufacturing to leverage high-yield, established silicon foundry infrastructure from wafer fabrication through to packaging. The heterogeneous integration of InP with silicon enables optics to meet these manufacturing challenges as well achieve best-in-class performance.

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Chapter 14
Merits and Potential Impact of Silicon Photonics

Po Dong, Guang-Hua Duan, Young-Kai Chen and David T. Neilson

Abstract In this chapter, we review the technical merits of silicon photonic devices and integrated circuits, which have benefited from high-index-contrast silicon waveguides, a high integration level of various optical functions on the same chip, and mature complementary metal-oxide semiconductor (CMOS) fabrication techniques. These technical merits assure silicon photonics as a disruptive optical technology that will achieve low-cost and compact optical modules for data communications, with applications such as chip-scale optical interconnects, short-reach communications in datacenters and supercomputers, and metro/long-haul optical transmissions. We discuss various applications in these fields, which may benefit from implementation in silicon photonics. In particular, we review silicon photonic circuits for wavelength-division multiplexing (WDM) transmitters, WDM receivers, coherent optical transmitters and coherent receivers, which all require photonic integration to reduce the cost and module size.

In this chapter, we review the technical merits and their impact on system performance, of photonic devices and integrated circuits fabricated in silicon. Section 14.1 will illustrate these advantages, which are derived primarily from high-index-contrast silicon waveguides and the use of mature silicon complementary metal-oxide semiconductor (CMOS) fabrication techniques. These allow highly compact devices and a high-level integration of various optical elements on the same chip. These merits offer the promise for silicon photonics to be a disruptive optical technology that will enable low-cost and compact optical modules for data communications. In Sect. 14.2, we discuss various applications in these fields, which

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may benefit from silicon photonics. We address a variety of applications over a wide range of distance scales including chip-scale optical interconnects, short-reach communications in both datacenters and supercomputers, and metro and long-haul optical transmission systems. In Sect. 14.3, we review reported silicon photonic circuits for wavelength-division multiplexing (WDM) transmitters, WDM receivers, coherent optical transmitters, and coherent receivers for enhanced functionalities and performance with reduced cost and size.

14.1 Technical Merits of Silicon Photonic Devices

While the term *silicon photonics* can have differing interpretations in the associated processing technologies and materials, in this chapter, we will focus on integrated optical devices and circuits fabricated from silicon-on-insulator (SOI) substrates using CMOS or CMOS-compatible modern micro-fabrication processes [1]. In this technology, silicon optical waveguides are used to form the primary transmission media in the integrated silicon photonic circuits. The high-index contrast of silicon waveguides with surrounding oxide cladding layer is the unique technical differentiation of silicon photonics compared with other low-index contrast technologies such as planar lightwave circuits (PLCs) using silica or polymer waveguides on silicon substrates and other photonic integrated circuits (PICs) fabricated on group III-V materials such as indium phosphide (InP) or gallium arsenide (GaAs). Therefore, the main technical merits of silicon photonics come from the compact high precision waveguide structures, mature materials and well-controlled fabrication processes that commercial CMOS production processes can provide. The organization of this section is as follows: Sect. 14.1.1 describes high-index-contrast silicon waveguides and their technical merits and disadvantages; Sect. 14.1.2 discusses the high integration capability of silicon photonics which is the key to various applications; and Sect. 14.1.3 argues the possibility of high yield and low cost offered from mature fabrications.

14.1.1 High-Index-Contrast Silicon Waveguides

Photonic waveguide devices with high-index-contrast cores provide several unique advantages in guiding and processing optical waves. It provides higher confinement of the optical field in a small waveguide core to allow a very tight bending radius, which results in realizing very compact photonic devices. In general, these small device dimensions lead to a high integration density of a variety of optical components that perform complex optical functions in a highly integrated optical circuit. Specifically, the smaller dimensions further result in lower electrical parasitic loading in electro-optic devices to increase the operating speed, while the

electro-optic interactions are further enhanced by the tightly confined optical field to provide better electro-optic performance and enable new functionalities.

In silicon photonics, the silicon waveguide has an index contrast of ~ 2 with the surrounding silicon dioxide cladding layer, which permits good optical confinement even in a very small silicon core with a sub-micrometer cross-sectional dimensions. Considering a typical waveguide width of 0.5 μm and waveguide heights of 0.2–0.3 μm, a tight bending radius of less than 5 μm can be allowed without suffering much optical loss in the bend. The small waveguide bend radii allow compact optical components and much more flexibility in the design of complex optical circuits. Various mode size converters can be also engineered in the high-index-contrast silicon waveguides to form inverse tapers or grating couplers to couple the light efficiently, either in-plane or vertically, with single mode optical fibers. By vertically coupling the light between the on-wafer vertical grating couplers and the fibers, it enables the wafer-level testing of silicon photonics integrated circuits, which would significantly reduce the expensive testing cost to identify 'known-good' integrated silicon photonics circuits in the production process.

As the waveguide width and height can be precisely fabricated at the nano-meter scale, a submicron silicon waveguide can be engineered to create a large index difference between the transverse-electrical (TE) and transverse-magnetic (TM) modes. This large birefringence can be used to implement very compact and efficient polarization splitters and polarization rotators [2–5], which are critical to construct polarization-diversified PICs without using external bulky optical elements.

The advantage of the high index contrast can be exploited to produce silicon waveguides with a wide range of effective refractive indices from as low as 1.45 (oxide) to as high as 3.48 (silicon), at a wavelength of 1550 nm. The effective refractive index can be prescribed by engineering the cross sections of silicon cores with advanced CMOS fabrication processes. The resultant large span of waveguide indices allows efficient evanescent coupling of silicon waveguides to various types of other adjacent waveguides made from silicon nitride, silicon oxynitride, III–V semiconductors and polymers. This is because the evanescent coupling between different waveguides relies on phase matching conditions, which require that the effective indices of the two waveguides be close in value. This unique property enables silicon photonics as a desirable platform for large-scale photonic integration with multiple optical interconnecting layers of various waveguide materials. One example is a demonstrated silicon-germanium-silicon nitride integration platform where different types of waveguides have been monolithically integrated together on a silicon wafer, as summarized in [1]. Effective low loss coupling between silicon waveguides with heterogeneously integrated III–V waveguides was also demonstrated to form hybrid silicon/III-V lasers, where the silicon waveguide circuitry is an integrated part of laser cavities [6]. Once the light is coupled from an III-V waveguide to a silicon waveguide, more advanced lasers, such as widely tunable lasers [7], can be easily realized by using the highly functional silicon optical circuits as the wavelength filtering and tuning elements.

On the other hand, the large index contrast of silicon waveguides brings technical challenges to the process controls, which would degrade certain optical performance if not properly taken into account in the designs. The waveguide propagation loss would be highly sensitive to the roughness at the silicon and oxide interface, posing significant fabrication challenges especially during silicon waveguide formation. Fortunately, this challenge has been addressed and resolved in the past decade. Today, a rather low propagation loss of 1–3 dB/cm can be routinely achieved in submicron silicon waveguides with high confinement.

With the nano-scaled waveguide dimensions, the effective index of a silicon waveguide is very sensitive to process variations during the fabrication, and to the variation of the silicon thickness of SOI wafers available today. This index variation translates into uncertainty in the optical phase of the guided optical waves when propagating through a waveguide. This phase uncertainty causes a significant challenge to attain accurate wavelength controls in narrow-bandwidth components such as WDM filters. For example, for a silicon micro-ring with a ring waveguide width of 0.5 μm and a height of 0.22 μm, the sensitivity of the center resonant wavelength to the waveguide width deviation is about 0.8 nm/nm. This means that a very small process variation of 1 nm in the width of a silicon waveguide would produce a shift in a resonant wavelength by 0.8 nm. In order to control the resonance within 10 GHz (0.08 nm), it requires a precise dimension accuracy of less than 0.1 nm. As the lattice constant of silicon crystals is 0.5431 nm, it is impractical to fabricate such micro-rings with a prescribed resonant wavelength by CMOS process control alone, and such a device will require active tuning.

The other challenge is related to the large birefringence between TE and TM modes, which would pose a significant challenge to implement polarization-insensitive couplers and filters for photonic circuits such as WDM receivers. Nevertheless, this challenge can be mitigated by using polarization-diversity design techniques, as illustrated in Sect. 14.3.

14.1.2 High Integration Level of Silicon Photonics

Silicon CMOS processes integrate a wide range of functional materials in fabrication including silicon layers with various doping, silicon oxide, silicon nitride, and germanium, as well as various metals and other dielectrics. This enables the implementation of various active and passive photonic devices, such as splitters, couplers, modulators, photodetectors, and thermal phase shifters. All of these active and passive optical components can be integrated onto a single silicon photonics chip with compact sizes and low-power consumption. For example, a silicon-germanium-silicon nitride integration platform allowing the fabrication of a number of optical devices on the same wafer has been illustrated in [1]. Such an integration platform offers the chip-scale integration of diverse optical functions, such as germanium photodetectors, silicon Mach-Zehnder modulators (MZMs), micro-ring devices, arrayed waveguide gratings (AWGs), variable optical

attenuators, polarization rotators (PRs), polarization beam splitters/combiners (PBS/C), variable optical couplers, optical hybrids, and more. Many demonstrated PICs, including WDM transmitters/receivers, polarization diversity coherent receivers and transmitters, were briefly surveyed in [1]. Today, several silicon photonics foundry services are available to provide similar integration of passive components with high-speed modulators and detectors [8, 9]. With heterogeneous integration techniques, more advanced optical functions such as integrated hybrid silicon/III-V lasers with silicon MZMs were also demonstrated [10].

There are several benefits of high scale of optical integration. As more optical components are integrated in a single chip, the back-end optical packaging process can be simplified significantly with fewer optical interfaces. This results in reduction of the overall module cost and possibly better optical performance with less coupling losses. The conventional optical packaging for single-mode devices requires sophisticated precision optical alignments with micro-meter accuracy among multiple micro-optical components such as lenses, power splitters, and polarization elements. This kind of elaborated packaging process is expensive and frequently with low yield, which contributes to a significant portion of the total module cost, even exceeding the material cost of photonic devices. A highly integrated silicon photonics integrated circuit may use a simple packaging process with much fewer external optical components and is compatible with low cost non-hermitic packages. Furthermore, its compact form factor would significantly increase the density and capacity of optical transceivers, which become critical in many applications in densely populated datacenter and central telecom offices. The compactness of silicon photonic devices with high degree integration can naturally address the challenges to achieve low-cost transceivers with small form factors.

14.1.3 High Yield and Low Cost by Mature CMOS Fabrication

The microelectronics industry has made huge progress during the last 45 years with the number of CMOS transistors densely integrated in a micro-processor chip. This electronic integration scale has been doubled every 18 months. By 2015, the most advanced micro processors have more than five billion transistors integrated on a chip. This progress has been made possible through a large investment in both the precision fabrication equipment as well as the maturation of the advanced fabrication processes. Silicon photonics leverages the mature CMOS tools and production processes that have been developed for electronic integrated circuits. Typically, a matured 193 nm deep ultraviolet lithograph tool can delineate critical dimensions down to 120 nm robustly, which is a sufficient resolution to fabricate most silicon photonic devices. This does not require the use of today's state-of-the-art tools to resolve fine feature sizes to fabricate 20 nm CMOS transistors. Other fabrication steps for silicon PICs are similar to the CMOS fabrication

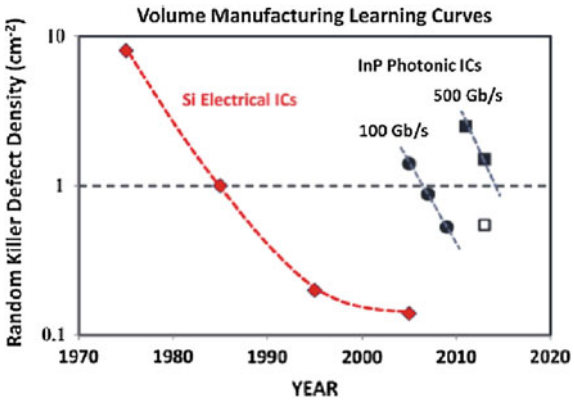

Fig. 14.1 Trends for "killer" random defect density reduction versus time for silicon ICs and InP large-scale transmitter PICs for both 100-Gb/s transmitter products (*solid circles*) and 500-Gb/s transmitter (*open circles*). The 100-Gb/s data points represent average production performance whereas the 500-Gb/s data points are based on sampling of better performing wafers during early production. (From Infinera [11])

processes by adapting to the existing tools, such as dielectric and metallic deposition and etching, ion implantation to make p-doped or n-doped materials, planarization thorough chemical and mechanical polishing (CMP), and so on.

Through the maturation of the silicon electronic integrated circuits, the device yield has been improved and the random killer defect density has been reduced. Figure 14.1 shows the random killer defect density for the electronic integrated circuits and the photonic integrated circuits made on InP-based materials developed by Infinera [11]. As the silicon electronic IC defect density is sufficiently low, the maximum economic chips size is limited by lithographic reticle size rather than by the defect density. The resultant analysis from Infinera shows that the random killer defect levels for InP PICs are around 1.8 defects/cm^2, which are a factor of approximately 15 times higher than the best value achieved in the silicon electronic ICs. Currently there is no published result on the random killer defect density for the silicon PICs, but since silicon photonics uses similar tools, processes, and materials as electronic ICs, it is reasonable to expect that the silicon PICs will be able to achieve similar values in terms of random killer defect density and the yield as with electronic ICs. Consequently the yield of PICs and the number of components that can be integrated in a single PIC will be very high.

The relative material cost of silicon PICs can be benchmarked with that of InP PICs in two ways without taking the yield considerations discussed previously. The first is to consider the production efficiency, which can be measured by calculating the number of wafers processed per operator in a specific time slot. The production efficiency is a good measure of the fabrication cost such as labor cost, facility usage and material consumption. Although a quantitative number is difficult to establish, the highly automatic tools used by silicon IC industry would lead to a very high

production efficiency compared to InP PICs. The second consideration is related to the wafer size. Given the same production efficiency and cost base to fabricate one wafer, the unit cost per chip will be reduced by the use of larger wafers. Today, wafers with diameters of 200 and 300 mm are being used for the fabrication of silicon PICs, while InP PICs use wafers with a diameter of 100 mm or smaller. This indicates the numbers of PIC chips harvested from a silicon wafer is a factor of 4 or 9 more than that from an InP wafer, for the same size of PIC. From those two considerations, we can conclude that the material cost for silicon PICs is likely to be significantly lower than InP PICs.

14.2 Applications

This section explores possible communication applications, which could benefit from highly integrated silicon photonic devices. As illustrated in the last section, the technical strength of silicon photonics comes from high-level integration rather than individual devices. Therefore, silicon photonics would contribute to the introduction of complex optical functionalities for advanced system applications where high levels of integration are required with small form factors. In Sect. 14.2.1, we study applications in conventional telecommunication applications, including long-haul, metro, and routing/switching systems. In Sect. 14.2.2, we will explore applications in datacenters and supercomputers. Future chip-scale optical interconnect applications will be examined in Sect. 14.2.3.

14.2.1 Telecommunication Applications

The capacity of the core network has grown significantly, driven by ubiquitous multimedia users, vast data centers, and cloud-based applications. It is expected that this rate of growth will continue to increase, compelled by several mechanisms. Metro traffic is expected to grow from the need to back-haul increasing amounts of mobile traffic generated by multimedia and cloud-based applications, which will be powered by 5G wireless systems in 2020. Cloud data centers based on regional clusters would be deployed to provide high capacity with low latency. This will demand very large interconnect capacity to connect metro regions with fast synchronization among distributed data clusters. As a result, significant growth rates in the long haul fiber optic transport networks would be required to satisfy ultra-high capacity interconnects to link nationally distributed datacenters together.

Today, 100-Gb/s channel rate transponders are widely deployed to meet the traffic demands, and higher rate transponders are entering service. It is expected that the data rate per transponder will grow to 1 Tb/s and beyond in the next decade [12, 13]. Advanced modulation formats such as quadrature phase-shift keying (QPSK), quadrature amplitude modulation (QAM), discrete multi-tone (DMT) and

orthogonal frequency-division multiplexing (OFDM), in combination with intradyne coherent detection and polarization division multiplexed (PDM) techniques, have been used to increase the spectral efficiency per optical wavelength channel [14, 15]. However, it is likely that future growth in transponder capacity will come through parallel integration of these devices with WDM or spatial diversity multiplexing (SDM) techniques.

Intradyne coherent techniques utilize electronic digital signal processing (DSP) functionality at both the receiver and transmitter. The DSP functions are implemented on CMOS application specific integrated circuits (ASICs) to process modulated optical waveforms to mitigate transmission impairments as well as maximize channel capacity [14, 15].

Today's optoelectronic interfaces in the core and metro networks are mostly implemented with high performance discrete component technologies such as InP lasers and detectors, $LiNbO_3$ modulators, passive silica-based PLC, etc. These optical components are packaged separately to deliver the required performance, which leads to higher cost and size to implement the whole system. In order to grow the capacity and data rate for network nodes, smaller footprint devices will be needed with lower power consumption and higher optical port density. Increased levels of photonic integration and cointegration with electronics will be required to achieve this goal. Silicon photonics is a good solution to address these demands in capacity and density with high levels of integration. It also brings the prospect of integration with CMOS electronics at the chip or wafer level with more optical functionality to enable new system architectures.

Several successful demonstrations of silicon photonic devices have been reported for coherent communications using dual-polarization QPSK coherent receiver and transmitter PICs up to 224 Gb/s [16–18]. Utilizing WDM arrays, higher aggregated capacity were also demonstrated in a 40-channel WDM receiver PIC with a 40 Gb/s data rate per channel [19] as well as a 10-channel silicon modulator chip with a 25 Gb/s data rate for each channel [20]. The emerging co-integration of electronics and photonics [21, 22] will allow the DSP functionality to be combined with the photonic integrated devices to allow further capacity scaling and enable electronic adaptation in the network node. This provides the flexibility required in the dynamic network environment to mitigate transmission impairments and further enhance the stability and robustness of the core networks.

Scaling of optical transport networks can be achieved by connecting distributed switches and routers together with high capacity optical links to efficiently share network transport resources in response to dynamic service demands. Vendors have continued to increase the processing capacity in a core router, but are facing increasing challenge in containing the growing power consumption. So far, the energy per routed or switched bit is falling at around 13.5 %/year in high capacity internet protocol (IP) routers [23]. This rate of reduction in switching power matches the reduction of the feature size of silicon transistors in the earlier years, where the switching speed was slow and the power scaling was not limited by its I/O power consumption [24]. As the I/O switching speed increases to meet the high

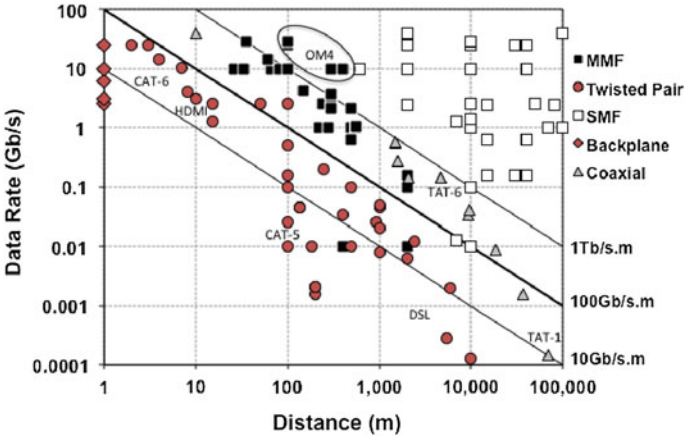

Fig. 14.2 Data rates and distances for commercial interconnects based on [23] with updates. These results show a practical distance bandwidth product limit for electrical interconnects of around 100 Gb/s.m for a twisted pair, around 500 Gb/s.m for coaxial cables and for multimode fiber (MMF) around 1000 Gb/s.m and optimized MMF of OM4 4000 Gb/s.m. Above this single mode fiber is used (SMF). The scaling of MMF can be understood from its modal dispersion of $\sim$500 GHz·m and in copper cables from frequency dependent loss

capacity demands, the recent rate of power reduction has fallen behind the rate of capacity growth since 2006.

With the energy efficiency not scaling as rapidly as the capacity is growing, an increase in power density (20 %/year) is observed. The increased power density leads to increased chip operating temperatures, limits the addition of features to routers, and makes system design more challenging. Ultimately this prevents the accommodation of a highest capacity router into a single rack, which then requires the use of optical interconnects to link multiple racks together as found in current multi-terabit router solutions [25]. Electrical interconnects are both frequency and distance dependent with a practical limit of the distance-bandwidth product of around 100 Gb/s-m [23], as illustrated in Fig. 14.2. To extend the reach in carrying high speed signals, multimode fiber optical interconnects are used today with a distance limited to a few hundred meters with emerging single mode fiber (SMF) optical link to 1 Tb/s-m. There are two main interconnect requirements for routers and switches: client side and internal. The client side interfaces, soon to be 1 Tb/s/line card, conform to standard-based interfaces with a typical reach from 100 m to 80 km. Multimode parallel fiber links would not be practical to serve the client interface, as providing 1 Tb/s over a 100 m reach would require 100 pairs of fibers. Connecting large numbers of fibers faces many challenges such as the limited physical density on both the linecard boards and faceplate. A significantly higher cost will be needed to deploy multi-fiber ribbons. Therefore, SMF interfaces will be needed even in the shorter reach space to possibly employ a high-density silicon photonics solution. Longer reach interfaces such as 40–80 km pose various performance challenges for traditional on–off keying optical signals under tight loss and

dispersion budgets in the link, necessitating a move to more advanced modulation and detection schemes. Additionally there is a need to embed long haul interfaces into the router line cards to enable direct connection with core and metro networks.

Despite a much short interconnect distance, the internal interconnects inside a router or switch typically requires twice the bandwidth than that of the client interface to avoid blocking and to provide system redundancy. For a router with an interconnect distance of 50 m for placement and cabling from rack to rack, this distance makes multimode fiber attractive with a connection rate below 20 Gb/s, while single mode fiber links are more attractive at data rates above 20 Gb/s. Since today's routers have around 5–10 Tb/s of client capacity, this would demand a backplane interconnect capacity in the range of 10–20 Tb/s. If multimode fiber pairs are used at 20 Gb/s, this would require up to 1000 fiber pairs to meet this interconnect capacity. Therefore, it is clear that, to grow these systems in the future with increased data rate in a fiber, single-mode fibers and other multiplexing techniques in the long reach optics, such as WDM, are required for the rack-to-rack data links. Silicon photonics with increasing levels of photonic integration is an attractive option to make such solutions practical in cost, density and thermal management.

14.2.2 DataComm Applications

Optical interconnects for data-communication (DataComm) applications are mainly deployed in datacenters and supercomputers. Datacenters concentrate huge computational resources, including computer servers, storage, media and networking functions, to provide high capacity services and applications. Its processing capacity grows with the ever increasing volume of incoming user-driven internet traffic, establishing new services, and internal intra-datacenter traffic for various data analytics, back end processing and synchronization functions. This growth rate, by some estimated to be more than 60 %/year, exceeds the rate of increase in processing power of individual servers and therefore results in increasing numbers of paralleled and clustered servers and therefor vastly enlarging the footprint and real estate of the datacenter to handle accompanied electricity and cooling needs.

To digest the high volume of data, data center interconnection networks are becoming less oversubscribed, which requires more switches and interconnects. This rapid expansion of computing and data exchange capacity comes with an increase in power consumption, which is becoming a very important issue for present and future deployment of data centers. As large data centers moving to adapt passive cooling techniques to improve their power usage effectiveness (PUE), this reduces the density of equipment deployed in each facility. With lower computation density combined with higher server counts, significant increases in interconnect distance and capacity are required to be deployed within these sparsely populated passively cooled datacenters. It is thus of paramount importance to develop low-cost and power-efficient data link solutions for the clustered datacenters with an interconnect distance from several meters to 2 km.

The supercomputer application shows continued grow rate of around 80 %/year [26]. In order to provide high computation power with large data processing throughput, multi-core and parallel processing architectures are used in supercomputers. The distributed processing cores, memory banks, and I/O controls pose similar challenges to the high capacity interconnects and synchronization as those experienced in the datacenters, however, with shorter interconnect distances. Supercomputers typically require lower latency and precise synchronization in coordinating data with the system clock, and thus require higher bandwidth and density of interconnects.

Today, multimode parallel interconnects represent the most cost-effective solution for supercomputer and datacenter applications, dominating this market with the bit rates of 10 Gb/s. However, the scalability of the current interconnect solution with parallel multi-mode fibers is limited for several reasons. First, the direct-modulation bandwidth of vertical-cavity surface-emitting lasers (VCSELs) is limited by fabricated dimensions and parasitic loading. Despite the availability of some commercial VCSEL products are up to 25 Gb/s with a few laboratory demonstrations up to 50 Gb/s, the available link span with optimized optical multimode (OM) fiber, such as OM3, is limited to about 300 m at 10 Gb/s and further reduced to 70 m at 25 Gb/s. Second, it is very challenging to introduce WDM functionality in optical links using VCSEL sources, which leads to a high price premium to prescribed VCSEL wavelengths and complex fiber coupling schemes with multimode fibers. While some of VCSEL devices can be used with SMFs, this would reduce the available optical link budget and remove many advantages in low-cost packaging with multimode fibers. To maintain desirable reach, VCSEL-based solutions can only be scaled by increasing the number of fibers at lower data rate. This can be problematic in datacenters since using multi fiber ribbons over long distances has significant cost and creates challenges for density of interconnect in supercomputers, routers and switches. With these limitations on VCSEL technology, disruptive solutions taking advantage of WDM in SMFs such as using silicon photonics are being actively pursued to increase transmission bit rates while also extending reaches.

In coming years, we expect the continued growth in the bit rate per channel and the number of WDM channels, with the total capacity per link potentially exceeding 1 Tb/s within the next 10 years. There are several approaches to achieving such a high capacity: by increasing the channel number from 4 up to 16, or by increasing the symbol rate from 25 Gbaud to 50 Gbaud, or using multi-level modulation formats such as four-level pulse-amplitude modulation (PAM-4) allowing multiple bits per symbol. It is likely that all these will be utilized to some degree. Additionally, parallel SMFs or even fibers with multiple single-mode cores can also be used to further increase the total link capacity.

Photonic integration on silicon combining active devices such as lasers and modulators, passive building blocks such as wavelength multiplexers, grating couplers, even co-integrated with CMOS electronics, is widely perceived as the emerging solution for a cost-effective and scalable communication technology for datacenters and supercomputers.

14.2.3 Chip-Scale Interconnects

The proliferations of ubiquitous broadband mobile devices powered by broadband applications have escalated the demand for real-time delivery of rich multimedia content from the remote data centers to the end users. The large volume of data traffic must be aggregated into high capacity optic fiber access networks and then transported by high capacity metro and core optic transport infrastructures to the cloud-based data centers. This indicates that the capacity of data processing and the associated data interconnect capacity in the network processors and switching units will be expected to grow by another 100- to 1000-fold in the next decade.

The processing capacity of electronic has scaled up with the increase in the integration density of CMOS processors, following "Moore's Law" over the evolution of generations of CMOS technology for the past 50 years [27]. However, future scaling of CMOS processors faces serious challenges in advancing all aspects of the density, performance and cost [28]. CMOS has moved out of "Classical (geometrically driven) Scaling" where performance was driven by new lithography tools leading to smaller transistors and performance enhancements. The sub 20 nm technologies represent the era of "Equivalent Scaling" where performance is driven by changes in technology such as strained silicon, high-K/metal gate, multigate transistors and integration of germanium and compound semiconductors.

The clock frequency improvement of the modern nano-scaled embedded CMOS circuitry is limited by the wiring parasitic loading and high power consumption. Multi-core processor architectures are adapted to increase the processing capacity with low speed core to reduce the switching power [29]. The electronic inter-chip and intra-chip interconnections limit the performance and scalability of the processing chips and systems in attaining large bandwidth capacities with stringent latency requirements. New initiatives such as heterogeneous 2-D/3-D IC integration [30], radio frequency [31] and optical interconnects [32] are being actively pursued to deliver high link capacity for intra- and inter-chip interconnections. The optical interconnect technology promises the highest data rates over variable link distance from millimeters to kilometers with scalability, low-latency and low energy per bit [33].

For the chip-scale interconnects, the power consumption of the optical links needs to be extremely low, with an expected value of less than one picojoule per bit. Low-power optical devices have been demonstrated in the emerging silicon photonics technology [34, 35] in combination with energy-efficient CMOS drivers and amplifiers using both hybrid electronic–photonics integration [22] and monolithic integration [21].

Chip-scale interconnects also require high capacity. Advanced modulation formats such as PAM-4 [36], DMT [37], etc., have been demonstrated to attain higher capacity for each channel, and demonstrate data rates over 100 Gb/s even without

coherent detection. With WDM, the aggregated data rate can be increased by using many wavelength channels. Recently, an InP quantum dash mode-locked laser was demonstrated to deliver an aggregated 2.256 Tbps of data from 80 wavelength channels with 22.7 GHz channel spacing [38]. Silicon photonics can integrate compact tunable micro-ring modulators and tunable detectors to deliver 10 × 10 Gbps WDM optical switching and networking functions on a single chip [39], with an example shown in Fig. 14.3. With advanced modulation formats and a compact comb laser source the silicon photonics chip in [39] can be further integrated with CMOS processors to provide switching and processing capacity up to 100 Tbps in a possible compact module as illustrated in Fig. 14.4.

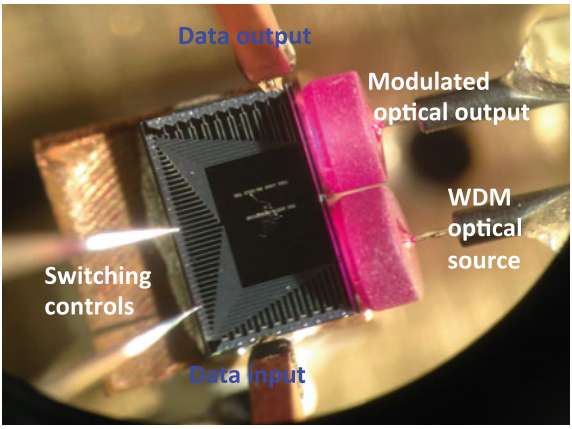

Fig. 14.3 A reconfigurable silicon photonic 100 Gbps network-on-chip with 10 tunable micro-ring modulators and 10 tunable detectors for high speed optoelectronic cross-connect and broadcasting functions

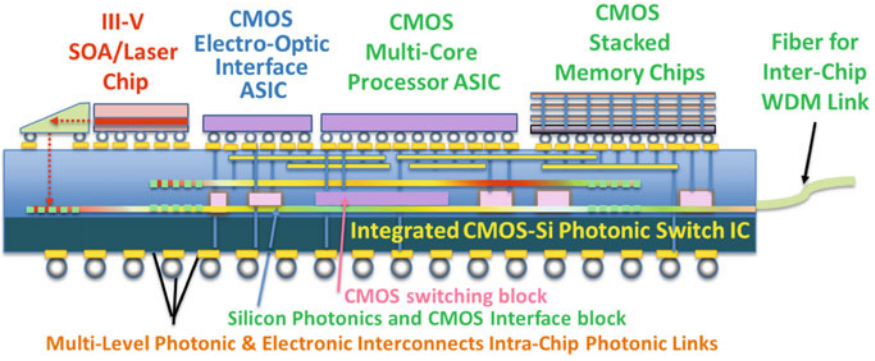

Fig. 14.4 Schematic diagram of a possible compact terabit silicon photonics integrated circuit assembled with CMOS interface ICs, processor, stacked memory chips and III-V laser by heterogeneous integration technology

14.3 Silicon Photonic Integrated Circuits

In this section, we review some recently reported silicon PICs that have demonstrated a high-degree of integration. While large-scale silicon PICs have been presented for various applications including large-count optical switches, optical phase antennas, optical signal processors, and multimode/multicore fiber transmitters/receivers, here we mainly focus on WDM transmitters (Sect. 14.3.1), WDM receivers (Sect. 14.3.2), coherent transmitters (Sect. 14.3.3) and coherent receivers (Sect. 14.3.4).

14.3.1 WDM Transmitters

The integration of multiple parallel transmitter devices on a single silicon photonic chip provides a promising approach to realizing low cost WDM transmitters. Transmitters for WDM systems based on photonic integration on silicon are being actively pursued by a number of companies and research organizations [20, 40–46].

An approach based on the integration of optical devices in the front-end of a 130 nm CMOS SOI process, where transistors and other electrical components can be formed as well, was used to demonstrate a 4 × 28 Gbit/s single-chip solution [40, 41]. This platform aims at embedded applications such as system backplanes and high-performance computing. The optical engine is based on a single 1490 nm DFB laser, shared on the four lanes of a parallel optical interconnection.

In [42], a coarse WDM (CWDM), 4 × 12.5 Gbit/s link solution was demonstrated, aiming at replacing copper links in future generations of computing architectures. The optical engine is based on four hybrid lasers (InP bonded onto SOI), emitting at four wavelengths around 1310 nm, with a channel spacing of 20 nm.

Integrating silicon MZMs with a silicon nitride AWG allowed demonstration of a dense WDM (DWDM) 10 × 25 Gb/s modulator chip with a footprint of only 5 × 8 mm^2 [20], with a circuit diagram shown in Fig. 14.5. The AWG has 100 GHz

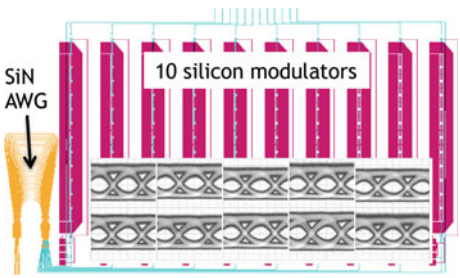

Fig. 14.5 Schematic layout for a silicon PIC to generate the 10-channel DWDM signal reported in [20]. The *insets* show the optical eye diagrams of all ten channels at 25 Gb/s modulation

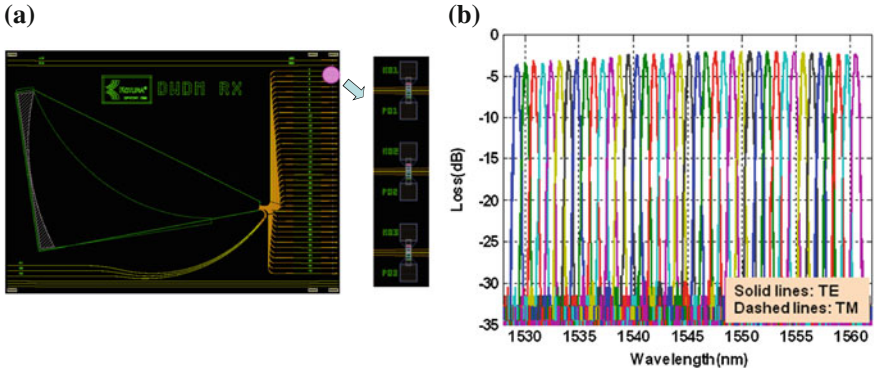

Fig. 14.6 WDM receiver based on large-core silicon echelle grating and germanium photodetectors in [49]. **a** Optical circuit layout; **b** WDM spectra of the etchelle grating

channel spacing and the MZMs have a V_π of ~10 V. With a drive voltage of 6 V and a 3 V reverse bias, the achieved dynamic extinction ratios are 5.6–7.2 dB for the modulators with a total on-chip insertion loss of about 5 dB for all ten channels. Including the coupling loss to fibers and the AWG loss, the total insertion loss is ~18.5 dB. Figure 14.5 shows the chip layout and the optical eye diagrams of all ten channels at a data rate of 25 Gb/s after the AWG multiplexer.

A CMOS photonics-based small form-factor module was demonstrated in [43]. It is compliant with the 100GBASE-LR4 standard (i.e., WDM 4 × 25 Gbit/s around 1300 nm) and uses externally coupled laser(s) and low power consumption modulators. The overall power consumption is 5.5 W.

An ultra-low power 100 Gbit/s silicon photonic WDM transmitter, tunable with off-chip laser sources has been demonstrated in [44] using silicon micro-ring modulators. The hybrid CMOS transmitter consists of eight 12.5 Gbit/s WDM channels, with a total capacity of 100 Gbit/s. In [45], a four-channel WDM silicon photonic transmitter with integrated III-V lasers and electro-absorption modulators fabricated through a wafer bonding technique was demonstrated. The WDM transmitter can operate at a rate of 4 × 28 Gb/s with a bit error ratio (BER) of $<10^{-12}$ and power consumption of 10 pJ/bit. In [46], a four-channel WDM silicon photonic chip was reported, which is capable of generating 4 × 100 Gb/s DMT signals. This PIC integrated four silicon MZMs together with a tunable microring-based WDM multiplexer. The DMT modulation is able to boost the channel rate to 100 Gb/s even with 10 G optical devices, with the potential for 400 G applications using four wavelengths.

14.3.2 WDM Receivers

As explained in Sect. 14.1, there are a number of challenges to implementing WDM receivers, which include fabricating high-performance WDM demultiplexers, managing polarization dependencies and achieving large responsivities. While single-polarization WDM receivers on silicon PICs have been widely reported [19, 47, 48], to date only a few polarization-insensitive WDM receivers have been demonstrated. In this section, we will only review polarization insensitive WDM receivers that use a variety of techniques: by using large-core silicon waveguides for polarization-insensitive WDM filters in [49], using two-dimensional (2-D) gratings for polarization insensitive coupling in [50], using on-chip polarization rotators for polarization diversity in [51], and using on-chip polarization diversity with thermally tunable filters in [52].

A compact, low loss and high-speed WDM receiver by monolithical integration of 40 germanium photodetectors with a 40-channel polarization independent echelle grating has been demonstrated on the large cross-section SOI platform [49]. WDM demultiplexing using an echelle grating built on large-core silicon waveguides can achieve high performance and polarization insensitivity. High-bandwidth optical power detection with large responsivities can be achieved by using a butt-coupled germanium photodetector that has a horizontal p-i-n junction configuration. For the receiver PIC, with a 100-GHz channel spacing device, a 2.5 dB on-chip optical loss and better than 27 dB channel isolation were achieved, shown in Fig. 14.6. The echelle grating exhibited less than 0.5 dB of polarization-dependent loss (PDL) and the germanium photodetector had greater than 28.7 GHz of bandwidth at –1 V reverse bias and a responsivity of 1.0 A/W. The demonstrated WDM receiver has overall fiber-to-photodiode responsivity of 0.4 A/W and >1 Terabit/s total aggregate transmission bandwidth.

A monolithically integrated, polarization-diversified silicon receiver chip with 10 wavelength channels at 100 GHz spacing was demonstrated in [51] based on submicron silicon photonics. On-chip polarization rotators have been used to convert the TM component in an optical signal to TE mode, which is demultiplexed by the same AWG as for the TE component. It showed zero polarization-dependent wavelength shifts and less than 1.8 dB polarization-dependent losses, however, the fiber accessed responsivity is less than 0.1 A/W.

A polarization-insensitive WDM receiver using a 2-D grating coupler and second-order ring filters has been reported in [50]. The 2-D grating simultaneously couples the two orthogonal polarization states of a single mode fiber into two different waveguides on the PIC with both as TE modes. The photocurrents from two polarizations are then combined at the same PD. For the WDM filters, second-order rings are used for five channels with 300-GHz channel spacing. The PIC demonstrated fiber-to-photodiode responsivity of $\sim$0.1 A/W, was polarization-insensitive and had a uniform channel response with crosstalk better than –15 dB.

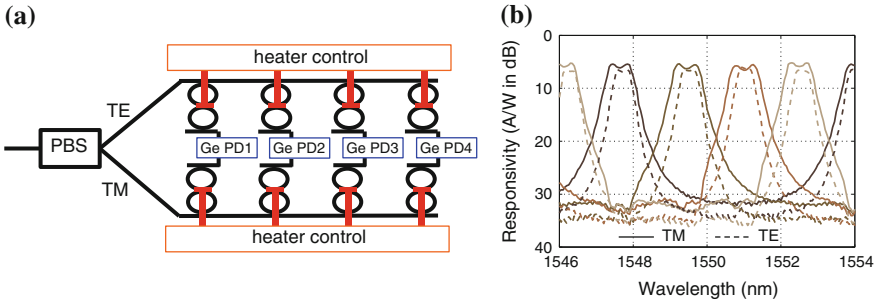

Fig. 14.7 An example of a silicon photonic polarization-insensitive receiver based on microrings and germanium photodetectors [52]. **a** Optical circuit of polarization diversity WDM receiver. **b** Fiber-to-PD responsivity spectra of the WDM receiver for both polarizations and for a 200-GHz channel spacing after the heater powers are optimized

An integrated silicon photonic polarization-diversity WDM receiver chip was reported in [52] based on on-chip polarization diversity. Shown in Fig. 14.7a, the input optical signal from the fiber is first coupled into the silicon waveguide through the inverse taper, and then split by the on-chip PBS into two orthogonal polarizations in TE and TM modes. Each polarization enters four cascaded second-order ring filters specifically designed for the corresponding polarization. Each second-order ring has an independent local heater located on the top of the ring to provide independent tuning of the operating wavelength. A pair of drop waveguides from the TE and TM sides is connected from the two ends of the absorption region of the same germanium photodiode. For this device, 4 × 25 Gb/s polarization-insensitive WDM detection was reported with a fiber-to-photodiode responsivity of greater than 0.26 A/W, a polarization dependent loss less than 0.5 dB, and a crosstalk less than –20 dB for wavelength spacing of 200 GHz, as shown in Fig. 14.7b

14.3.3 Coherent Optical Transmitters

A coherent optical transmitter is required to generate amplitude and phase encoded signals. This typically requires the use of in-phase/quadrature (I/Q) modulators, which consist of two modulators whose output is combined with a 90-degree phase difference. Coherent optical transmission systems generally use polarization multiplexing to double the capacity in the fiber. Dual-polarization transmitters require a pair of these I/Q modulators with the second output being converted to another polarization and combined with the first. An I/Q modulator based on nested single-drive push-pull silicon MZMs was reported in [53], where a 50-Gb/s QPSK signal was generated with only 2.7 dB optical signal-to-noise ratio (OSNR) penalties from the theoretical limit at a BER of 10^{-3}. These silicon MZMs are based

on reverse-biased *p-n* junctions in the middle of silicon waveguides and represented the first successful demonstration of advanced modulation formats using silicon MZMs. By further integrating two I/Q modulators and an on-chip polarization rotator and PBC, a monolithic single-chip dual-polarization coherent modulator was implemented to generate a 112-Gb/s PDM-QPSK [16] and a 224-Gb/s PDM-16-QAM signal [18]. It was shown that the integration of on-chip polarization elements introduces an additional 0.9-dB OSNR penalty due to polarization dependent loss [16]. The polarization rotator is realized using a silicon nitride-assisted taper structure. This PIC was the first monolithic single-chip dual-polarization I/Q modulator and demonstrated the highest photonic integration for this particular application, even when compared to that found in a III-V material system. Dual-polarization I/Q modulators were further demonstrated in [54], where a novel polarization rotator based on silicon-only structure was employed. In [54], 128 Gb/s PDM-QPSK was generated.

Single-polarization silicon I/Q modulators with performance comparable to $LiNbO_3$-based I/Q modulators were also reported using a MOS-capacitor type silicon modulator [55]. A compact I/Q modulator with a size of less than 1 mm × 25 μm per MZM was fabricated and was driven by a low-power CMOS driver with less than 200 mW per channel. 56-Gb/s QPSK signals were generated, and then polarization multiplexed external to the chip to create a 112-Gb/s PDM-QPSK signal, which was transmitted through 2427-km standard single mode fiber. The performance showed negligible OSNR penalty associated with silicon modulator compared to $LiNbO_3$ modulators for back-to-back operation, and a small penalty after transmission due to chromatic dispersion.

Single-polarization I/Q modulators were also demonstrated using silicon-organic modulators, where an electro-optic polymer is spin-coated on silicon slot waveguides [56, 57]. High modulation efficiency could be realized through both the high electro-optic coefficient of the polymer as well as the high electrical field concentration in the slot. Up to 40-Gbaud QAM signals were generated in [57].

14.3.4 Coherent Optical Receivers

Coherent optical receivers must implement optical hybrids to mix an optical signal with a local oscillator (LO) to separate the in-phase and quadrature components of the modulated optical signal. Since the coherent signals are typically polarization multiplexed they must also provide polarization diversity. A grating-assisted coherent receiver PIC, where 2-D gratings are used for fiber coupling was first demonstrated [17], as shown in Fig. 14.8a. Using gratings, the TE and TM components of the signal and LO can be coupled from fibers and separated into different silicon waveguides, and all of the light on the chip is TE polarized. The 2-D gratings simultaneously realize polarization splitting and polarization rotation. The coupled signal and LO pass through two 90-degree hybrids based on 2 × 2 multimode interference (MMIs) couplers with eight germanium photodetectors. Using

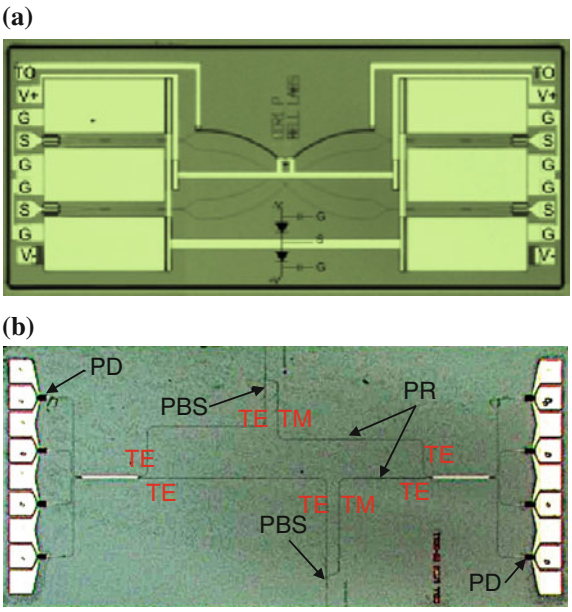

Fig. 14.8 Monolithic silicon PICs for dual-polarization coherent receivers. **a** Optical picture of a silicon-PIC coherent receiver using 2-D gratings as the couplers in [17]. **b** Optical picture of a silicon-PIC coherent receiver using on-chip polarization rotators (PR) and polarization beam splitters (PBS) in [18]

this PIC packaged with transimpedance amplifiers (TIAs), a 112-Gb/s PDM-QPSK signal was successfully detected with a BER performance comparable to a commercial coherent receiver. This PIC elegantly demonstrates the high-degree of optical integration especially for polarization diversity circuits.

While these 2-D gratings are elegant optical elements for a polarization-diversity receiver, their coupling loss is typically high and also the 3-dB optical bandwidth is limited to around 40 nm. To solve these limitations, edge coupling can be used, but then on-chip PBSs and PRs are required. A silicon coherent receiver by integrating on-chip polarization rotators and splitters was implemented in [18]. The optical signal enters the PIC from one facet with two polarizations. The optical LO is coupled into the silicon PIC from the other facet (see Fig. 14.8b). Once coupled in, the signal and LO are divided into TE and TM polarizations by two PBSs. The TE polarized lights proceed to the 4 × 4 MMI-based 90-degree hybrids, whose four outputs are detected by four germanium photodetectors on the left side of the PIC. The TM components from the output of PBSs are converted to TE polarization by two polarization rotators. The converted TE light enters the right-side 4 × 4 MMI-based 90-degree hybrid, which is identical to that for the TE mode. Using this PIC co-packaged with TIAs, a 112-Gb/s PDM-QPSK signal and a 224-Gb/s PDM-16-QAM signal were successfully detected.

Besides typical 90-degree optical hybrids, a monolithic polarization diversity coherent receiver employing 120-degree optical hybrids has been reported in [58]. This PIC monolithically integrates silicon inverse tapers for fiber coupling, silicon polarization splitters, germanium high-speed photodetectors, and 120-degree optical hybrids based on 3 × 3 MMIs. With a chip size only of 2.3 × 1.5 mm^2, 112-Gb/s

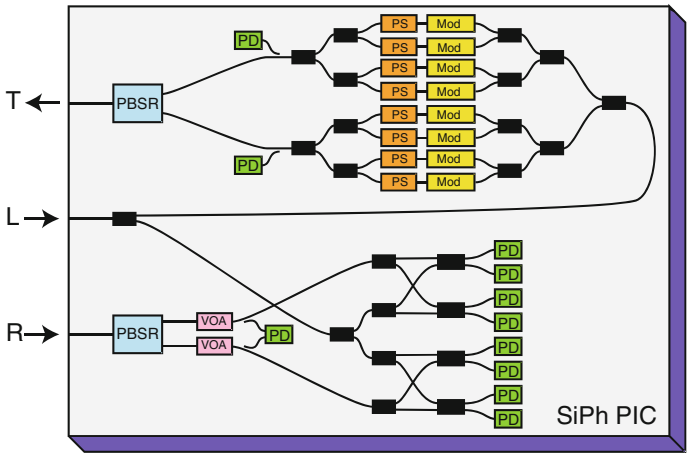

Fig. 14.9 Optical circuit diagram for single-chip coherent optical transceiver in [59]. *PBSR* polarization beam splitter and rotator; *VOA* variable optical attenuator; *PS* phase shifter; *PD* photodetector

PDM-QPSK signals were detected in the wavelength range of 1530–1580 nm. The BER results demonstrate comparable performance to commercial receivers with 90-degree hybrids. The broader optical bandwidth from the use of 120-degree hybrids indicates that this type of receiver may find applications in low-cost transceivers.

In [59], a monolithic silicon PIC containing all the optical frontend for a 100-Gb/s coherent transceiver except the laser was demonstrated, with the optical circuit shown in Fig. 14.9. The silicon PIC was co-packaged with linear modulator drivers and TIAs in a very compact gold-box module with a size of 27 × 35.5 mm^2 and power consumption <4.5 W. This PIC further verifies the high integration level of silicon photonics for coherent optical transceivers, which has been achieved mainly by taking advantage of polarization elements on-chip and compact modulators.

14.4 Conclusion

In this chapter, we have described and evaluated the technical merits of silicon photonic devices and integrated circuits. The advantages derive mainly as result of the use of high-index-contrast silicon waveguides and the high integration level that is enabled by using mature CMOS fabrication techniques. There are additional opportunities from closer integration with silicon CMOS electronics, which can lead to higher function optoelectronic circuits and devices. These technical merits indicate that silicon photonics could be a disruptive optical technology in achieving

low-cost and compact optical modules for data communications. The application spaces include chip-scale optical interconnects, short-reach communications in datacenters and supercomputers, and metro and long haul optical transmission systems. We have described various applications in these fields that would benefit from implementation in silicon photonics. In order to demonstrate the high degree of optical integration, we reviewed specific silicon photonic circuits for WDM transmitters, WDM receivers, coherent optical transmitters and coherent receivers. These PICs will find applications that require photonic integration to reduce the cost and module sizes.

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Chapter 15
Silicon Photonics for Telecom and Datacom Applications

Francesco Testa, Alberto Bianchi, Stefano Stracca and Roberto Sabella

Abstract Photonics for telecom and datacom has extended its range of applications moving from the traditional long distance and metropolitan transport networks to the access segment of fixed and mobile networks. In mobile networks, photonic networking is perceived as a key technology for both the backhaul and the fronthaul applications. Photonics is already considered the most viable technology for intrasystem interconnect in routers, switches, radio base stations, data centers, etc. In fact, driven by the traffic demand explosion, mainly due to the mobile internet, there is a tremendous pressure on the design of next generation telecom equipment with increased flexibility, processing capacity and bandwidth density and at the same time with reduced cost, power consumption and footprint. Photonics in such new applications requires conceiving and realizing new types of optical devices with a very low cost, a high miniaturization, and the capability to be produced in great volume with high production throughput. This requires a change in the paradigm that dictated so far the photonic devices development and that was based on discrete components made by InP material and the related production processes. The new devices will be based on silicon photonics technology exploiting the advantages of a cheap material and a highly developed CMOS production infrastructure that can ensure mass production with good yield and low cost besides the high miniaturization guaranteed by the high index contrast of silicon waveguides. Efficient energy utilization can be also provided by easy photonic–electronic inte-

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gration allowed by silicon photonics. The applications of future silicon photonics devices in telecom and datacom will be presented together with the device architectures under investigation in research projects.

15.1 Introduction

Silicon photonics is gaining momentum and is today widely considered a key technology for intra-system and intersystem interconnects of future generations of telecom and datacom equipment owing to its unique characteristics of low cost, high energy efficiency, and high miniaturization leading to the prospect of meeting the demand for a huge increase in bandwidth density of future hardware platforms.

In addition to this, the recent breakthroughs achieved in CMOS photonics open up the possibility to start scaling the integration level of photonic circuits by not only comprising an increased number of similar photonic circuits in a small silicon chip of a few square millimeters, but also by integrating circuits with many different optical processing functions with the aims of realizing a powerful photonic system on chip (PSoC).

The novel PSoC devices could drive the introduction of optical switching and networking in new applications where the optical transport and switching of high capacity signals will be required but where, at the same time, the use of conventional optical technologies based on discrete components is not viable due to their high cost, power consumption and large footprint.

In this chapter, a new generation of silicon integrated PSoCs for use in telecom and datacom will be presented. They are under investigation and demonstration inside research projects. The chapter is subdivided into two sections: the first deals with optical devices for access and mobile networks and the second with high scale photonic integrated devices for optical switching in metro transport nodes and data centers.

15.2 Optical Switching Devices for Access and Mobile Networks

Optical technologies and network solutions have so far played a crucial role in providing an affordable transport medium in metro and core network segments. While optical fiber is the backbone of the global internet infrastructure, today optical systems are perceived as a promising key piece of the radio access network (RAN) puzzle, in both fronthaul and backhaul transport areas.

The architecture and technologies of the future radio access network are being debated and many proposals have been investigated and demonstrated in different research centers [1–5].

In fronthaul, centralization of baseband processing is emerging as a way to secure performance, flexibility, and scalability of RAN. A centralized pool of baseband processing devices, the radio equipment controllers (RECs), may serve a number of distributed radio equipment (RE) aggregated in clusters optimizing the use of computational resources and enabling a significant energy saving. Figure 15.1 illustrates a possible fronthaul scenario in which a pool of REC devices communicates with a cloud of RE devices, distributed over a geographical area of a few kilometers, through a wavelength division multiplexed (WDM) ring network ensuring high bandwidth, transparency, high scalability, and simplification in cabling arrangement and installation.

Optical technologies can also ensure low latency, which is a crucial feature in radio access networks.

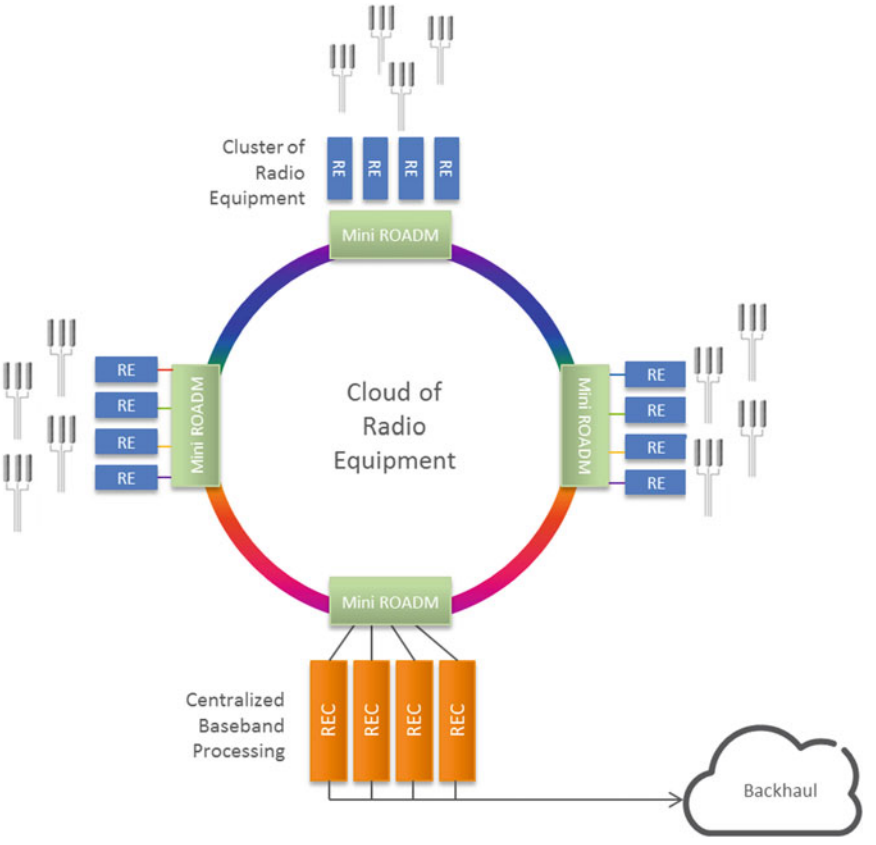

Fig. 15.1 Future fronthaul scenario

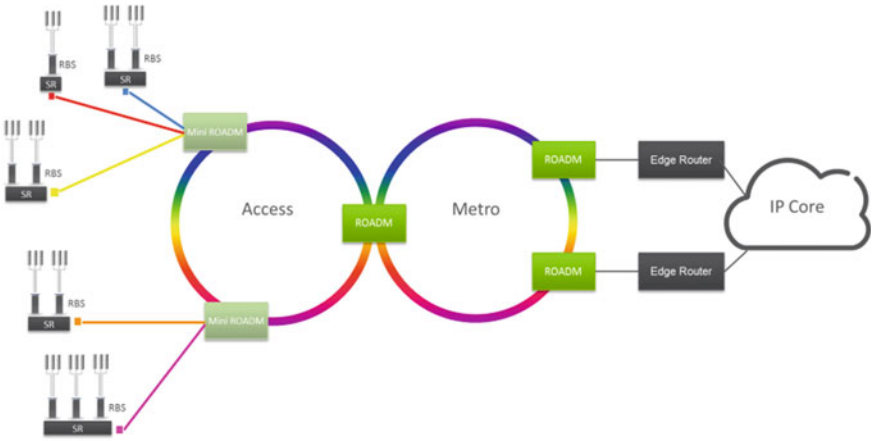

Fig. 15.2 Future backhaul scenario

In backhaul, mobile traffic coming from radio base stations (RBSs) distributed in an access area is aggregated by means of site routers (SRs). In a future backhaul scenario, as depicted in Fig. 15.2, each SR can be connected to the optical network by sending its traffic over wavelengths that are then collected in a WDM access ring. Multiple access rings are coupled with a common metro ring, which finally conveys the traffic toward the edge routers (ERs) for transmission to the IP core network.

The introduction of differentiated broadband services requiring low latency, the increase of the traffic load, the convergence of the mobile and fixed infrastructures, the need for consolidation of sites and energy saving are all reasons calling for the introduction of optical technologies in radio access and backhaul networks, where packet processing is moved at the access and metro edge of the network and intermediate channel add-drop and ring interconnection is performed at the physical layer in the optical domain.

However, conventional optical technologies and node architectures are not applicable to this network segment due to cost and complexity reasons. In particular, smart architectures with different levels of flexibility, possibly based on silicon photonic systems on chip, shall be identified to have a physical layer tuned on the backhaul needs at an acceptable cost and to unlock a diffusive penetration of the optical networking in this key network segment.

In the scenarios presented above optical switching devices are needed. Today WDM optical switches are based on high performances free space optics wavelength selective switches (WSSs) devices [6] that are costly and bulky devices.

The superset of features and functionalities, which are mandatory for metro/core applications, can be reduced in the fronthaul and backhaul area together with the required transmission performances (a lower number of intermediate nodes and shorter path lengths).

15.2.1 Silicon Integrated Mini-ROADM

A new type of device, named Mini-ROADM [3], emerges as an appealing building block to be fruitfully exploited in future mobile fronthaul and backhaul networks, as depicted in Figs. 15.1 and 15.2. This device is simpler with respect to conventional ROADMs: it is used in a ring network and it has only a few line input and output ports and a limited number of local add/drop ports (12 or possibly 24) and it has to handle a limited number of wavelengths (12 or 24). The types of transmitted signals are 10 Gbps common public radio interface (CPRI) for fronthaul and 10 GE for backhaul. The fundamental functions performed by the Mini-ROADM, in the proposed applications, are: multiplexing/de-multiplexing of all the WDM channels (at REC site) and add and drop of selected local channels (at RE site). Mini-ROADM can be automatically reconfigured for failure recovery, without the need to duplicate the optical interfaces at each add/drop port. Wavelengths, in a ring, can be replanned or added with limited over-provisioning and with no need of manual replacement in field. This flexibility is a great benefit for the dynamic nature of the considered mobile traffic.

Mini-ROADM is based on photonic integration, and in particular silicon photonics, which has the highest potential in the implementation of devices presenting low power consumption, high miniaturization, high level of integration (number of integrated functions), and large capacity.

For high volume applications like the ones in mobile fronthaul and backhaul networks, silicon photonics can also guarantee high yield and low cost due to the use of well-developed CMOS infrastructure. The use of cascades of micro-ring resonators as wavelength selective switching elements has been demonstrated in many papers [7–9] to be very promising due to the advantage of small size (a few μm), low loss, and low power (a few mW).

The Mini-ROADM architecture consists of two structures, as depicted in Fig. 15.3: an add bus structure to add wavelength channels to the bus towards both directions (west and east) by using a cascade of micro-ring resonators, and one drop bus structure to drop wavelength channels from the bus from both directions (west and east). This bi-directional functionality will be exploited to ensure the right level of resilience by activating protection mechanisms and will be explained below.

Each of the N add and drop ports is color-coded since each micro-ring resonator switch element is designed to operate over a limited wavelength range with its resonance tuned in correspondence to the channel in case of a switch element set to ON or far from the channels in case of a switch element set to OFF.

Each WDM optical channel is added in fiber1 toward west or in fiber 2 toward east directions by configuring the 1 × 2 integrated optical switch (controlled by the protection CTRL signal in Fig. 15.3) that enables one of the two paths (highlighted in Fig. 15.3 with blue and red dotted lines) and by activating the MRS1 micro-ring resonator. In the add structure, variable optical attenuators are integrated before the switch in order to regulate the signal levels depending on the position of the Mini-ROADM around the ring network. Each WDM optical channel coming from

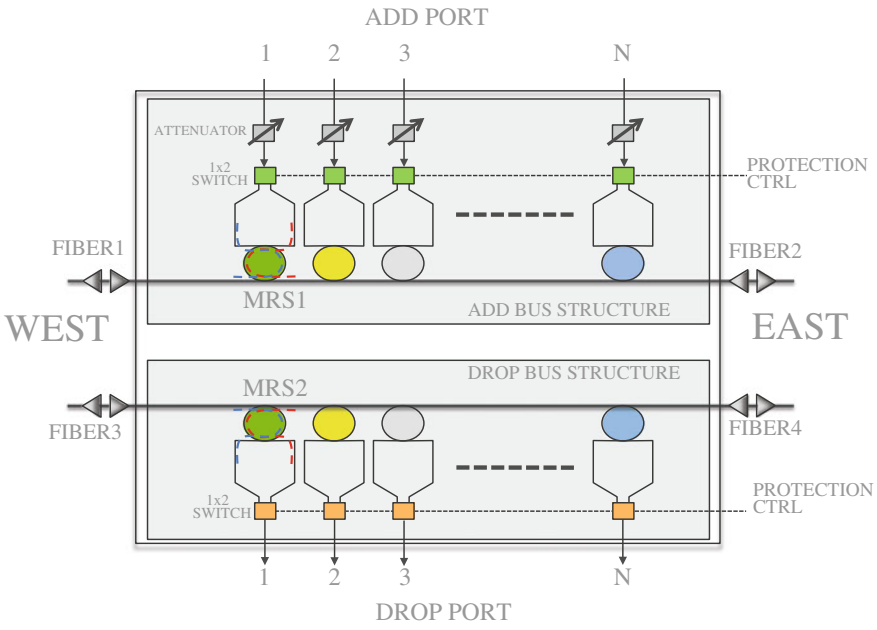

Fig. 15.3 Architecture of the Mini-ROADM

west or east direction (see blue and red dotted lines on MRS2 in Fig. 15.3) is dropped respectively from fiber 3 or fiber 4 by activating the MRS2 micro-ring resonator and the 1 × 2 optical switch.

The micro-ring resonator switching element (MRS) architecture is shown in Fig. 15.4. The MRS is able to add/drop its corresponding wavelength from opposite directions (see blue and red dotted lines in Fig. 15.4) while letting the other wavelengths pass through. The direction of the signals is selected by the 1 × 2 optical switch. The MRS is activated by injecting current in the micro-heater above the micro-ring or injecting carriers directly into the micro-ring.

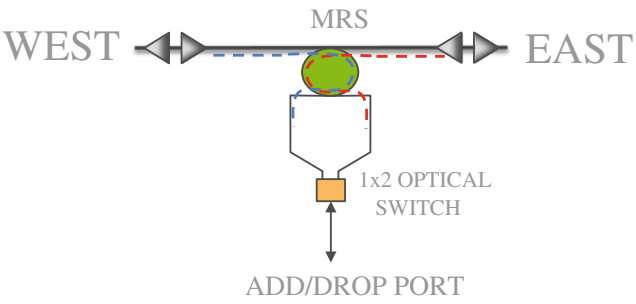

Fig. 15.4 Architecture of the micro-ring resonator switch element

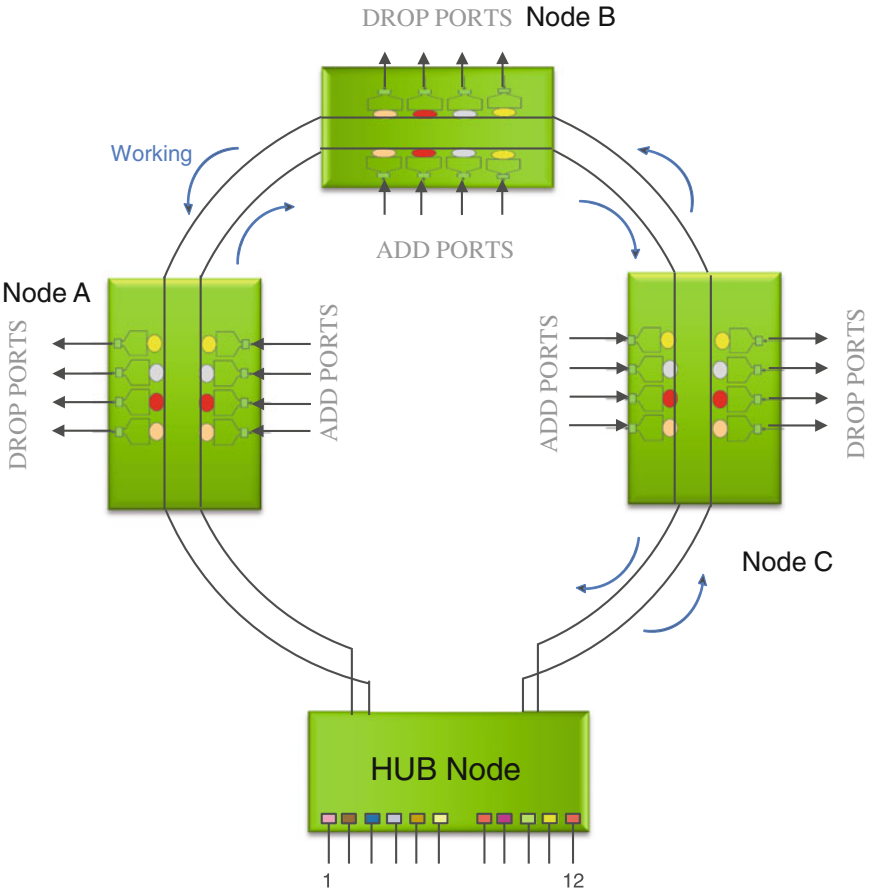

Fig. 15.5 Ring transmission in normal operating conditions

The architecture of the mini-ROADM supports protection mechanisms in the double ring network where it operates as a network switching node.

Figure 15.5 shows how the different wavelength signals are transmitted through four Mini-ROADM nodes in a double ring network. In normal operating conditions (see blue arrows) the downstream WDM optical channels are generated and transmitted by the hub node through the external ring and all the peripheral nodes (node A, B, and C in Fig. 15.5) selects and extracts the signals addressed to them by means of the drop ports of the mini-ROADM. The internal ring is dedicated to the upstream transmission and all the peripheral nodes add their local wavelength signals toward the hub by means of the add port of the mini-ROADM. The use of erbium doped fiber amplifiers (EDFA) at the hub node only can be considered as a means to overcome the node and fiber losses.

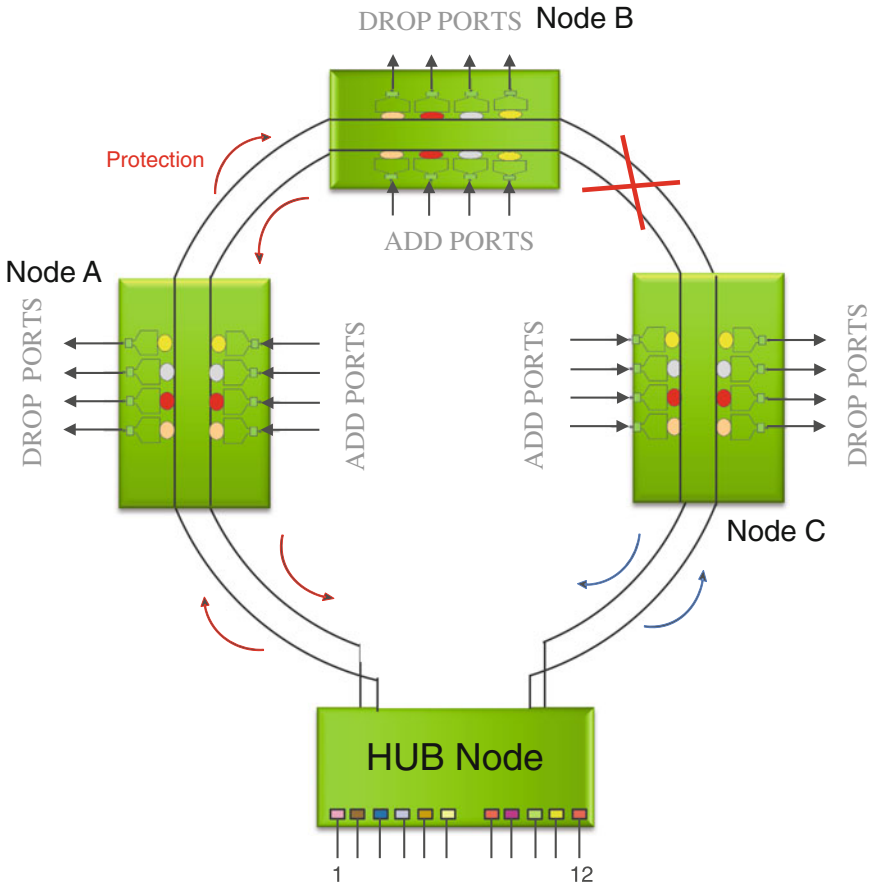

Fig. 15.6 Ring transmission in protection conditions

If a fiber break occurs, as shown in Fig. 15.6, the transmission in some nodes and/or for some wavelengths changes direction (see red arrows).

In nodes A and B the downstream transmission changes direction from counterclockwise to clockwise while the upstream changes from clockwise to counterclockwise. In node C the downstream and upstream transmission directions remain unaltered (see blue arrows).

Finally in the hub node, there is a mixture of transmission directions depending on the wavelengths: downstream wavelengths to node A and B are sent through the external ring clockwise while the wavelengths to node C are sent counterclockwise. Upstream wavelengths are received by the hub node in the internal ring, with counterclockwise direction from node A and B while the upstream wavelengths from node C are received in clockwise direction.

With this node architecture and functions it is possible to ensure in any operating conditions equal path lengths for upstream and downstream links as needed by the strict differential delay requirements of mobile communications.

15.2.2 Silicon Integrated Devices for Multidirectional ROADMs

The Mini-ROADM described above has been designed for communication between a hub node and peripheral nodes inside a double ring network.

In some cases, there is the need for extending the communication to other ring networks. For these applications, the ROADM placed between rings should have a more complex structure to provide multidirectional switching capabilities. In Fig. 15.7 a ROADM placed between two rings is shown and it must be capable of switching wavelength signals between four directions (N-north, S-south, W-west and E-east).

Figure 15.8 provides a sketch of a 4-direction ROADM composed of four silicon integrated wavelength selective switch (SI-WSS) devices. Each SI-WSS comprises local add/drop ports, interconnection links with the other SI-WSS devices and one bi-directional line port.

Optical channels coming from the network from any direction, which have to bypass the node, can be directed to any of the outgoing directions with no limitations.

The internal architecture of each SI-WSS is depicted in Fig. 15.9.

The add and drop switch elements use micro-ring resonators for their capability to switch selectively wavelength channels from the main bus with a low loss, a high level of miniaturization and a low power.

When a set of WDM signals coming from the South direction (see Fig. 15.9) enters the SI-WSS named South (S) they are first amplified by a semiconductor optical amplifier (SOA) and then proceed inside a straight bus waveguide while traversing the cascade A of color-coded micro-ring resonators. When each WDM signal arrives close to the micro-ring designed to resonate at a wavelength corresponding to its wavelength, if the switch is activated by properly tuning its resonance, it is coupled to the micro-ring and finally deviated to the drop port. Because of the wavelength selectivity of the micro-ring-based switch elements, if the

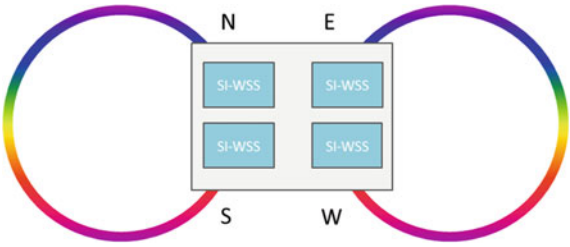

Fig. 15.7 Ring-ring interconnection

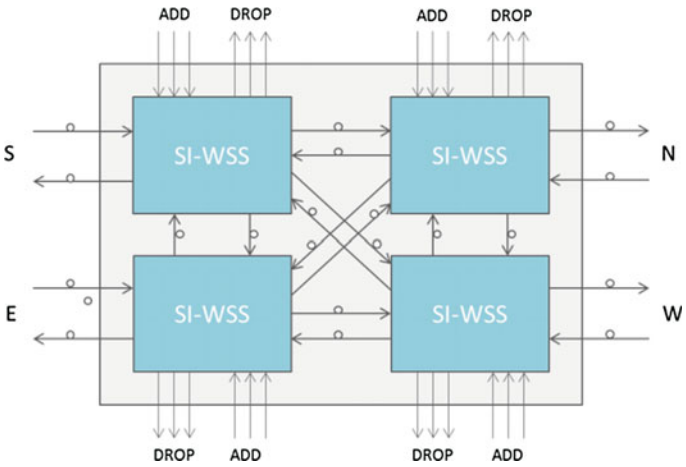

Fig. 15.8 Four directions ROADM

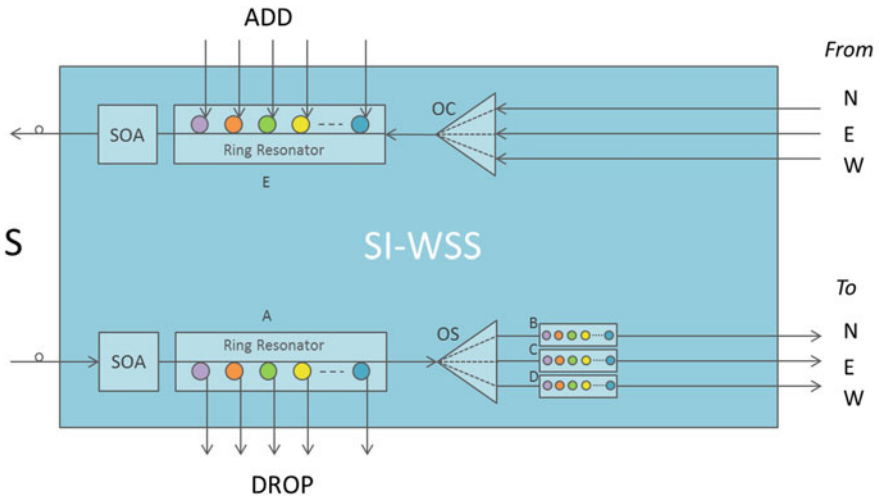

Fig. 15.9 Silicon integrated WSS

corresponding micro-ring switches are not activated, the residual wavelengths proceed in the optical bus with low loss towards the optical splitter (OS) where they are distributed to three new micro-ring cascades B, C, and D that have the function to select, respectively, the set of wavelengths to be routed toward north, east, and west directions. The wavelengths that are not selected for routing by the cascade B, C, and D are blocked.

Signals coming in the opposite direction from the other SI-WSS devices North, East, and West, are combined by an optical combiner (OC) and enter the micro-ring cascade E where they are multiplexed together with the wavelengths to be added.

These wavelengths sent to the corresponding color-coded micro-ring resonators, by activating the switch, are coupled to the micro-ring and finally they are sent to the output port after SOA amplification.

It is possible to build up a ROADM with more than four directions by increasing the splitting ratio of OS and OC blocks in each SI-WSS, but this leads to increasing losses that need to be compensated and eventually limits the practical feasibility.

The node architecture shown in Fig. 15.8 also has some limitations in routing the channels locally. In fact the micro-ring resonators, connected to add and drop ports, are color-coded and the added and dropped signals must operate at a predefined wavelength.

Moreover, add and drop wavelengths are only connected to a single SI-WSS and, as a consequence, they are rigidly assigned to a fixed direction and it is not possible to add and drop signals to other directions.

In all the cases, where these two limitations must be removed and it is required that the node to be colorless (i.e., the freedom to add or drop signals independently of their channel wavelength) and directionless (i.e., the freedom to add/drop wavelengths to/from any direction), the node architecture can be enhanced by including, in the add and drop section, the optical to electrical (O/E) and electrical to optical (E/O) conversion, together with an electrical cross-point switch as depicted in Fig. 15.10 and labeled with "X." The cross-point adds the flexibility to

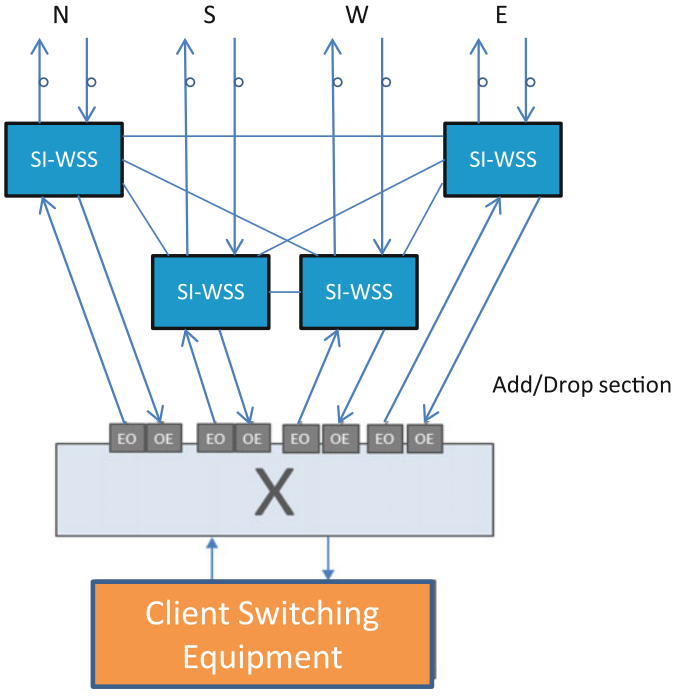

Fig. 15.10 Cross-point connected to SI-WSS based multi-directional ROADM

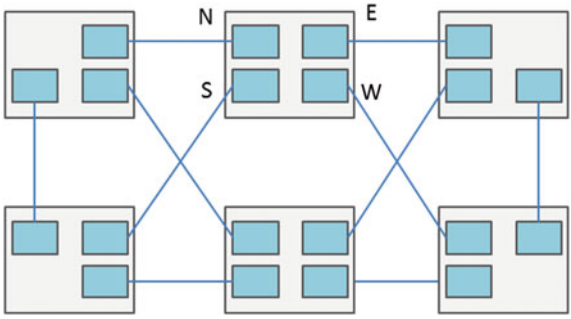

Fig. 15.11 Meshed topology

the proposed node, by cross-connecting, in the electrical domain, the signals from/to the client switching equipment.

It is also possible to use this node based on SI-WSS devices to build meshed topologies like in Fig. 15.11. Here a mix of 3-ways nodes and 4-ways nodes can ensure full mesh connectivity. When using mesh, instead of rings, it is useful to have more sophisticated recovery schemes, resilient to multiple failures, or with some level of resource sharing.

15.3 High Scale Photonic Integrated Device for Optical Switching in Metro Transport Nodes and Data Centers

Next generation optical transport networks must perform a dynamic rearrangement of the bandwidth while optimizing transport resources utilization and lowering the capital cost and power consumption. This will be enabled by highly flexible transport nodes in conjunction with an intelligent control and management plane based on software-defined networking (SDN) [10].

The Optical Transport Network is depicted in Fig. 15.12. It can be schematically divided into the following three segments:

- The metro-aggregation network has the function to concentrate and distribute traffic from/to the Access network. It aggregates typically mobile backhaul traffic coming from radio base stations (RBS) composed by a main unit (MU) and remote radio unit (RRU), ADSL traffic coming from DSLAM or PON. The required node capacity in this segment is typically up to few 100's of Gbps.
- The metro-core network has the function to interconnect nodes in large metropolitan areas with distances between nodes up to a maximum of 600 km and node capacities from hundreds of Gbps up to a few 10's of Tbps.
- The core network interconnects many metro segments with distances of thousands of km and node capacities beyond 10 Tbps up to 100 Tbps.

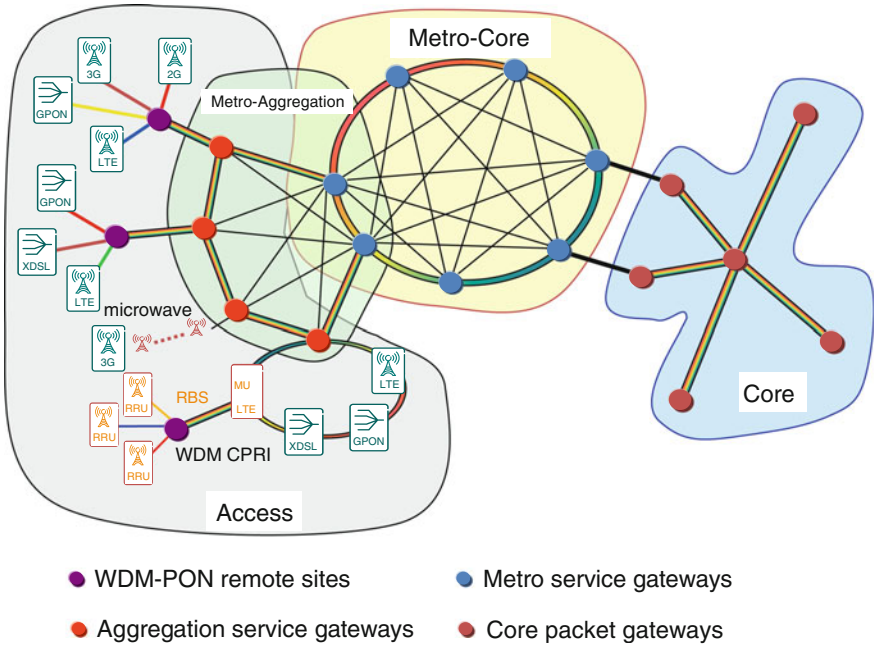

Fig. 15.12 Optical transport network

Metro WDM networks have become very critical to the business cases of many operators who recognize the potential explosion in bandwidth demand over the next several years. In metro network market, where a huge amount of equipment is required, the key feature is the ability to provide services fast, flexibly, and at low cost and with the highest level of scalability. The transmission technology has evolved toward a DWDM with 48 wavelength channels spaced 100 GHz apart in the C-band and the channel transmission rate is dominantly at 10 Gbps with a possible evolution toward 40 Gbps and even 100 Gbps and eventually the use of 96 wavelength channels.

To switch these signals in the metro transport nodes, an all-optical switching layer must be implemented based on scalable, high capacity, and transparent switching subsystems.

At each node, a multi-directional ROADM is placed with the function of adding into the network a certain number of WDM channels carrying traffic from data centers or client switching equipment (routers, packet switches, or SDH cross-connects) and with the function of dropping WDM channels from the network to the local client equipment. The input wavelength channels that are not terminated locally will transit through the node and are routed to one of the output fibers.

Highly flexible optical switching nodes are needed with the following characteristics:

- Full remote reconfigurability without the need for any manual intervention
- Automated control and lightpath set-up (these are key feature for the operators)
- Capability of reconfiguring the light-paths with a speed in the submillisecond regime to allow restoration on the fly in case of fault.

In conventional ROADM nodes (see Fig. 15.13) flexibility is only provided in handling channels of any wavelength coming from the optical network (bypass wavelengths, also known as express traffic) that can be routed from any input direction to any output direction. But at the add and drop sections (A/D), where the transponders are connected, add and drop wavelengths are rigidly assigned to a fixed direction and can only be reconfigured manually. Moreover each transponder is connected to a WDM mux/demux port so that the wavelength of the transponder is fixed and can only be changed by manual rewiring.

Next generation ROADM will be more flexible with respect to the currently deployed optical nodes. New ROADMs will have colorless, directionless and contentionless characteristics so as to extend the flexibility and automation to the end points. In new nodes it will be possible without any manual intervention to change the configuration of add/drop wavelength channels to/from any direction (directionless operation), independently of the transponder wavelength (colorless operation) and by allowing multiple signals with the same wavelength to be handled by the same add and drop structure (contentionless operation).

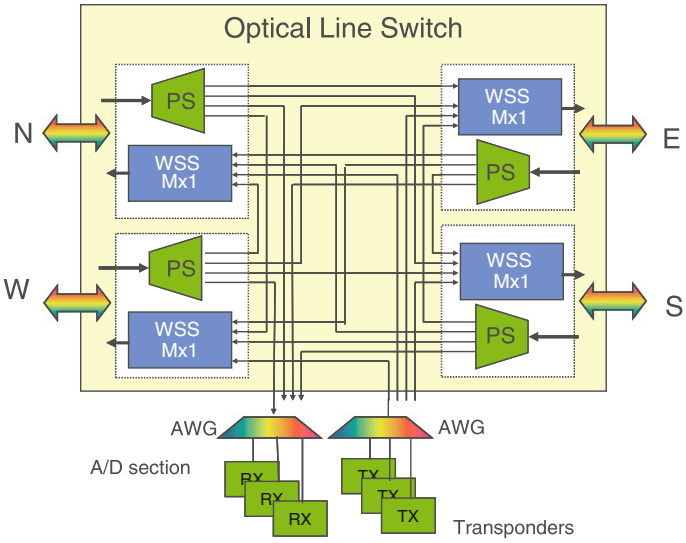

Fig. 15.13 Conventional ROADM architecture

The dynamic colorless, directionless and contentionless add/drop access will give the operator the possibility to optimize the resources utilization, reconfigure network bandwidth according to the variation of traffic pattern depending on time of day and day of week usage and support rerouting functions in case of faults in a cost effective way. To add such flexibility to the existing ROADMs that uses the free space optics-based 1 × N wavelength selective switching (WSS) for optical line switching, new architectures have been presented and they are illustrated in Fig. 15.14. The new colorless, directionless, contentionless (CDC) ROADM makes use of new blocks in the A/D section, called transponder aggregators (TPAs), to distribute and select the multiplexed signals before filtering the individual channel by the use of tunable filters [10].

The TPA adds flexibility to the exact point of the optical node where it is missed, at the end-point between the line switching subsystem and the transponder subsystem. The same TPA scheme can be used for both adding and dropping wavelength channels. It is mainly a N × M local optical switching subsystem (see Fig. 15.15 for the TPA used for dropping channels) with N ports connected to the line switching subsystem (typically from 4 up to 8) and M ports connected to the transponders (typically 12–16). It can be implemented by using an array of N power splitters (PS) connected by M of N × 1 optical switches (SW). This ROADM node architecture is easily scalable with the number of transponders by connecting additional TPA devices to the spare ports of the WSS devices.

An example of TPA is presented in [11], based on PLC splitters/combiners integrated with 1 × M optical switches in the same chip, and external tunable filters.

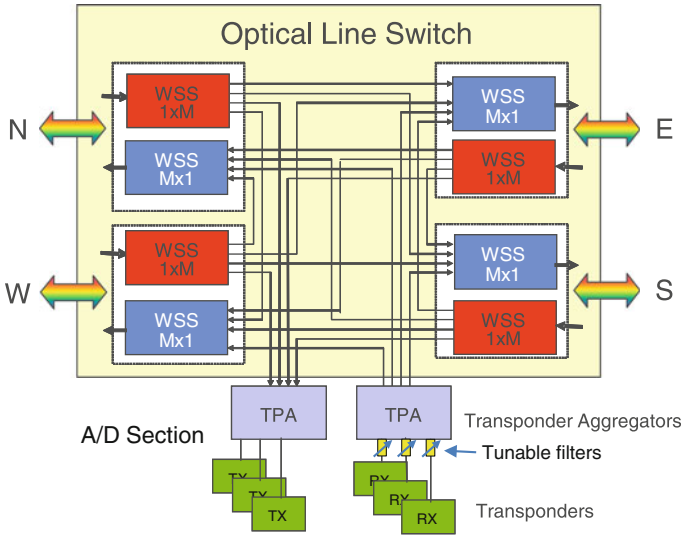

Fig. 15.14 CDC ROADM architecture

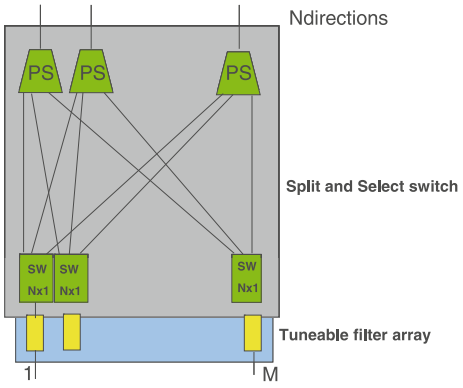

Fig. 15.15 TPA block diagram (for channel dropping)

More recently, silicon photonic integrated TPA devices have been realized, integrating on the same chip a matrix of Mach–Zehnder-based 2 × 2 switch elements and a cyclic 8 × 8 AWG [12].

Silicon photonic integration is a very interesting technology owing to the potential of implementing highly integrated photonic switching devices with low cost, high capacity, and small footprint characteristics together with the capability of a tight integration with the control electronics, implemented in a separate chip, and connected to the photonic chip through high density, low parasitic interconnect technologies like copper pillars. Integrated switching matrices based on micro-ring resonators have been investigated in [13–15].

15.3.1 Silicon Photonics Integrated TPA: IRIS Project[1]

In IRIS a completely new concept of a high scale integrated TPA device has been introduced and is shown in Fig. 15.16.

The fundamental photonic functional building blocks of the novel TPA are:

- AWG multiplexer/demultiplexer
- A matrix of T1 switch elements used to drop wavelength channels to the transponder receivers (Rx)
- A matrix of T2 switch elements used to add wavelength channels from transponder transmitters (Tx)

The various wavelengths, after demultiplexing, travel horizontally along the matrix and enter the T1 switch elements. The T1 switches (see Fig. 15.17) have four

[1]The research leading to these results has received funding from the European Union's Seventh Framework Programme (FP7/2007-2013) under grant agreement n° 619194.

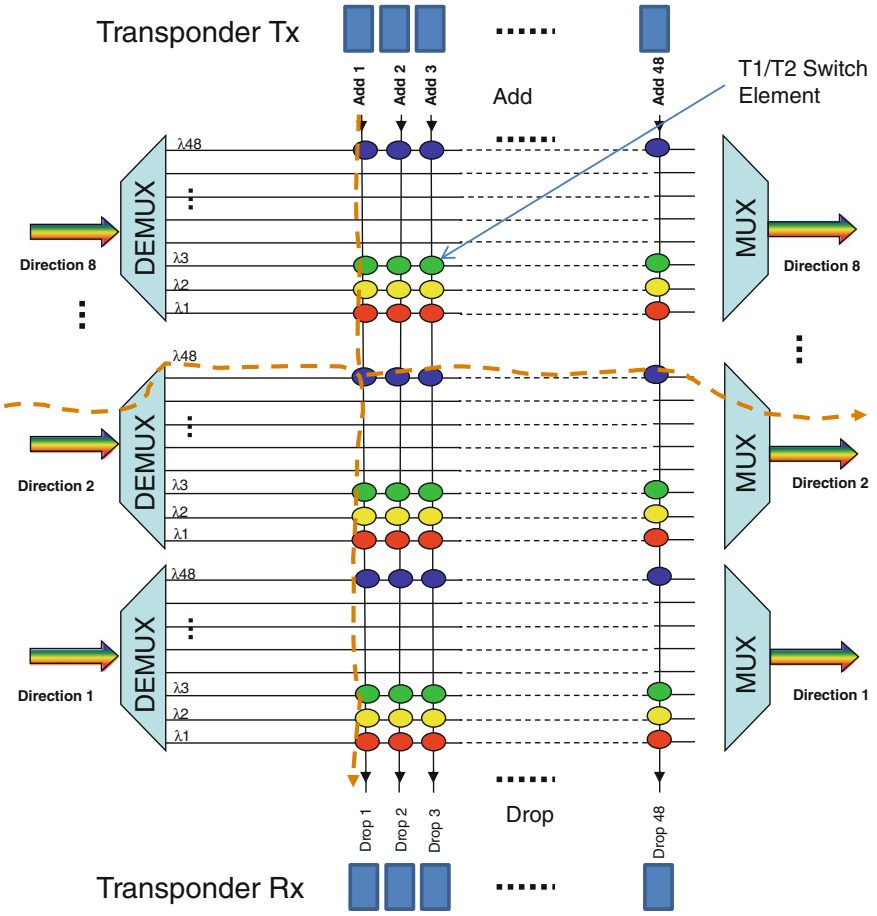

Fig. 15.16 High scale integrated TPA schematic block diagram

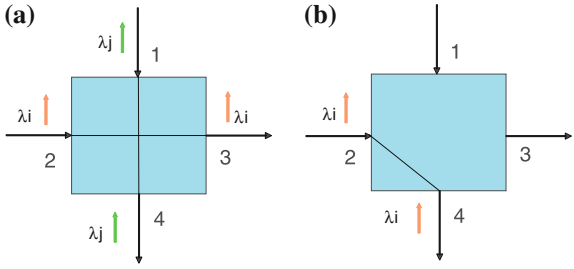

Fig. 15.17 T1 switch element used for drop functions: **a** control OFF, **b** control ON

unidirectional ports, two for input and two for output. Two operating conditions are possible for the T1 switch:

- The wavelength received at input 2 has not to be dropped by the T1 switch but has to proceed horizontally to output 3 while simultaneously a different wavelength, already dropped by another T1 switch, is received at input 1 and proceeds vertically to output 3 toward its transponder Rx (see Fig. 15.17a). The two wavelengths passing the T1 switch do not interact and the switch control is set to OFF.
- The wavelength received at input 2 has to be dropped by the T1 switch. The control signal is set to ON and the wavelength is switched vertically to output 4, toward its designated transponder Rx as depicted in Fig. 15.17b. In this second situation no signal is permitted to be received at input 1 because one and only one wavelength must be dropped to each transponder Rx. This function will be implemented in IRIS using a ring resonator technology as the wavelength selective photonic switch element [14].

The function of the T2 switch is to add wavelengths from transponders Tx to the lines, as shown in Fig. 15.18. The T2 switch has four unidirectional ports, two for input and two for output. In T2 elements switched OFF, a variable wavelength, selected by a tunable transponder, is received at input 1 and proceeds vertically toward output port 4 following its way toward the multiplexer for addition to the line. Simultaneously another wavelength is received at input 2 and proceeds horizontally toward output port 3 (see Fig. 15.18a) to reach the input port of the multiplexer. The two wavelengths will not interact. In T2 elements switched ON, the wavelength received at input 1 is switched to output 3 and no wavelength can be received from input 2 because only one wavelength can reach the input port of the multiplexer (see Fig. 15.18b).

IRIS will implement a complete TPA optical switching subsystem based on the switching matrices described above using monolithic integration of all functions on the same silicon chip.

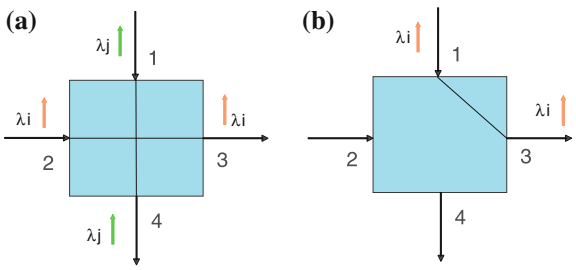

Fig. 15.18 T2 switch element used to perform add functions: **a** control OFF, **b** control ON

15.3.1.1 TPA Block Diagram

The TPA developed in IRIS is a single polarization integrated device, subdivided into two separated matrices: one for dropping WDM channels from the input ports as shown in Fig. 15.19 and one for adding WDM channels to the output ports as shown in Fig. 15.20. The integration of both functions in the same switch element providing add and drop simultaneously, even if theoretically possible, is prevented by the high port isolation requirements for the power imbalance between the added and dropped signals.

In the Drop matrix (see Fig. 15.19) four sets of 12 WDM-200 GHz spaced channels arrive at each input port and are coupled to the chip by single polarization grating couplers (SPGC) with a bandwidth wider than 35 nm. The channels are separated into odd and even by interleaver blocks (INT) to increase wavelength spacing and relax the isolation requirements of the switching matrix and demultiplexers. The separated channels are then demultiplexed by two types of demux blocks, one working with odd wavelengths and one with even wavelengths.

At the demux output the signals are sent to the switching matrix constituted by an optical crossbar of 2-coupled micro-ring resonators with 40 GHz optical 1-dB

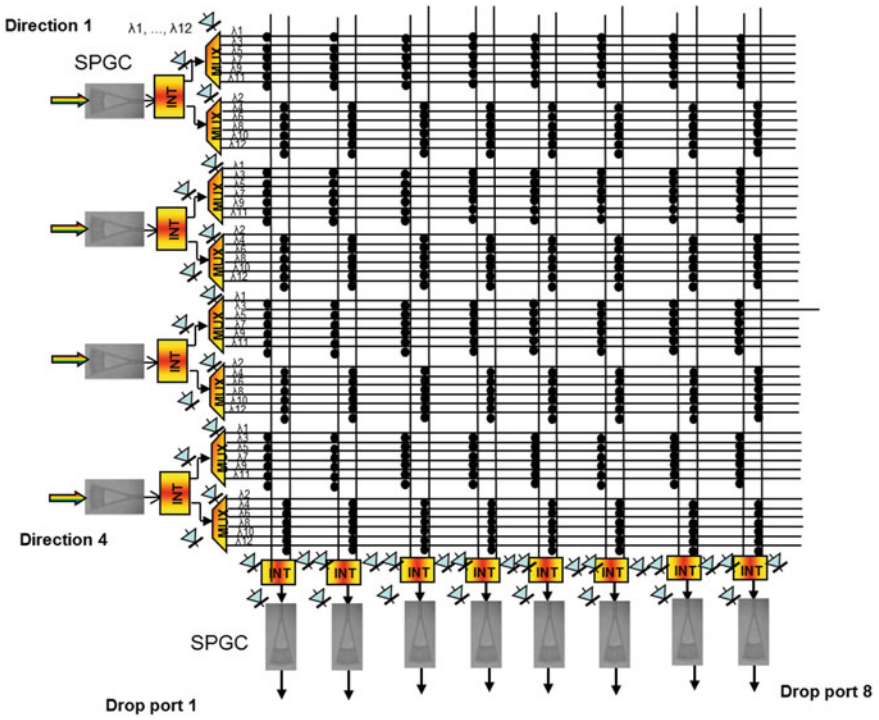

Fig. 15.19 IRIS drop matrix architecture

bandwidth, set to support 100 Gbps coherent transceivers. The matrix has 4 × 12 rows (each row with micro-rings able to switch a certain wavelength) and eight pairs of columns corresponding to the number of the drop ports to be connected to optical receivers. In the switching matrix the separated signals travel horizontally until they arrive in correspondence with the pair of columns connected to the receivers. At this point the coupled micro-ring resonators are activated and the signal is deviated vertically toward the drop port. In each pair of columns, one propagates odd wavelengths and one even wavelengths while an interleaver is used at each drop port to couple the odd or the even wavelength to the drop output where a SPGC is placed for optical fiber interconnection.

Monitor photodetectors are placed at strategic input and output locations to allow wavelength calibration of the different blocks.

In the Add matrix (see Fig. 15.20), eight tunable transmitters are connected to add input ports where a wavelength signal is coupled to the chip by the use of SPGC. Interleaver blocks at each add input are used to properly guide the WDM transmitter channels to the input of the switching matrix constituted by 2-coupled micro-ring resonators organized in 4 × 12 rows and eight pairs of columns. One column is propagating odd wavelengths and the other even wavelengths. Within the

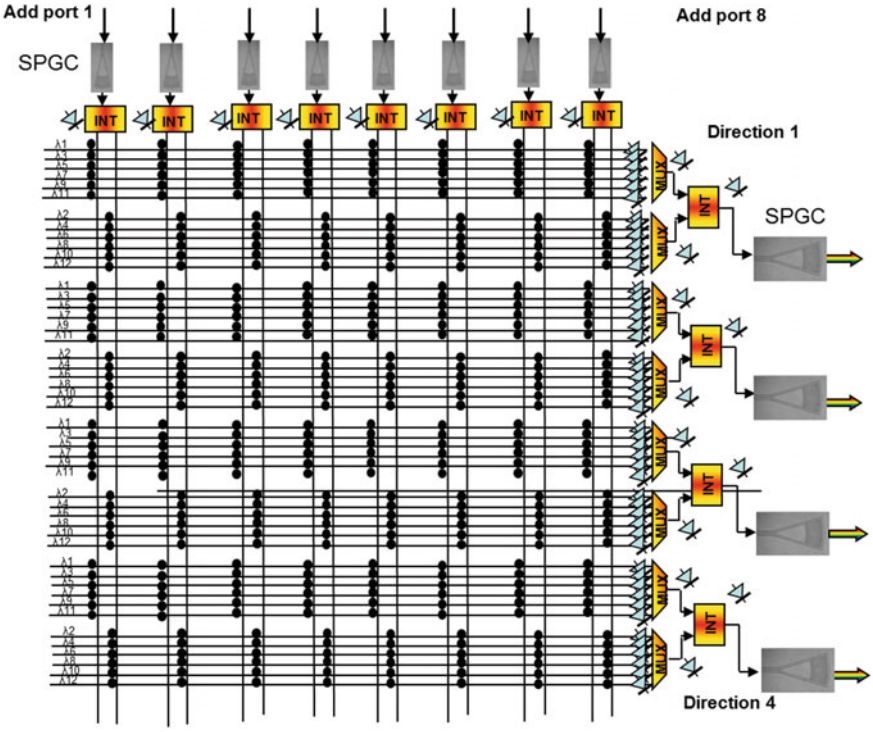

Fig. 15.20 IRIS add matrix architecture

matrix the transmitter signal travels vertically until it arrives in correspondence with the row to which the signal has to be switched horizontally to the wanted multiplexer by activating the proper coupled micro-ring resonators.

The signals propagate horizontally toward the output multiplexers, interleavers and finally SPGCs for line output fiber coupling.

Also in this matrix monitor photodetectors are placed at strategic input and output locations to allow wavelength calibration of the different blocks.

15.3.1.2 Optical Switching in Data Centers

The explosive growth of network traffic, mainly due to mobile terminals, video streaming, and cloud services, is the most challenging aspect that data center operators have to face.

Optical switching technologies are becoming to be perceived as the key technology for supporting the huge increase of capacity requirements in data centers (DC). Optical switching can meet the high bandwidth, traffic diversity and scalability requirements and at the same time it can guarantee low cost, low power consumption, and low footprint, aspects also considered crucial for data centers.

Different types of optical switching have been extensively investigated and demonstrated in the past [16–19]:

- Optical packet switching (OPS)
- Optical burst switching (OBS)
- Optical circuit switching (OCS)

Optical packet switching and OBS networks suffer from fundamental scalability issues while OPS is also challenged by the lack of viable optical buffering technology.

The most promising architecture for future DC is a hybrid architecture in which the OCS is used to augment in a smart way the existing electronic packet switching hierarchy with the scope of achieving a reduced switching complexity, high bandwidth, and significant cost and power reduction.

With this architecture the transparency and high bandwidth features of well proven OCS technologies are conjugated with the powerful capability of the CMOS technology in processing electrically data packets and with the features provided by software defined technology for path and service configuration.

An example of hybrid architecture has been presented and developed in the Helios project [20] and is schematically depicted in Fig. 15.21.

Suitable optical switches for that application have to be scalable, transparent to high data rates (28 Gbps and beyond), with a low footprint, low cost (a fraction of a $ per Gbps of capacity), and low power consumption (a few mW per Gbps).

Silicon photonics is the best candidate for implementing such types of integrated all-optical switches with high capacity.

For applications in the data centers the integrated optical switch can be implemented with the architecture depicted in Fig. 15.22 where it is shown an 8 × 8

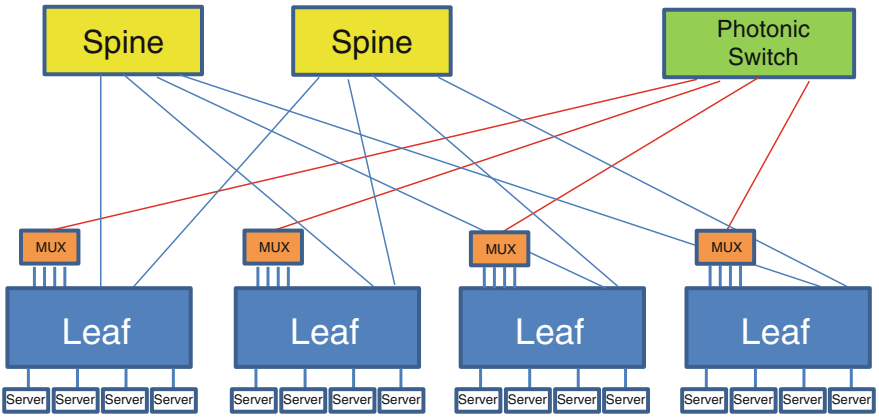

Fig. 15.21 Optical circuit switching for data center

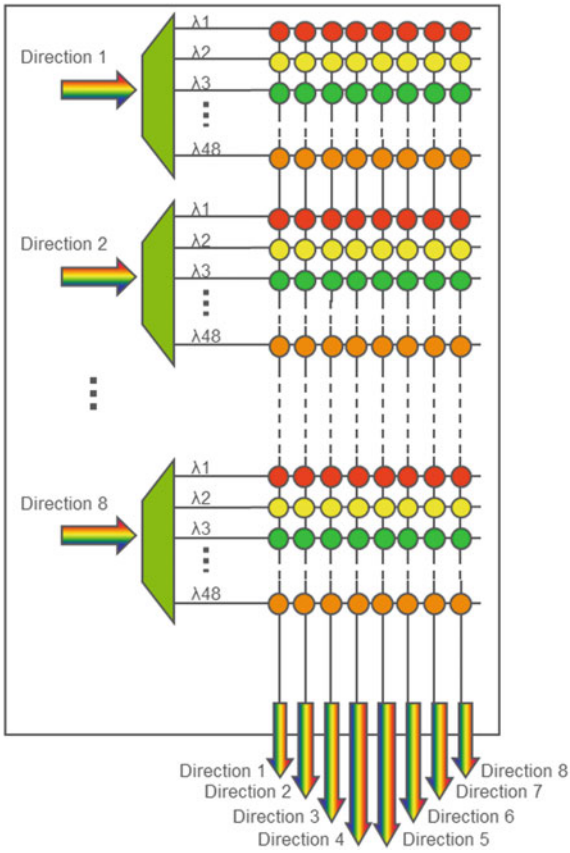

Fig. 15.22 Integrated silicon photonics optical switch architecture for data center

optical switch capable of supporting up to 48 wavelength. If 100 Gbps is the rate used for interconnection, this switch is capable of switching a total capacity of 38 Tbps.

At each fiber port AWG mux/demultiplexers are used to combine/separate the WDM signals coming from the leaf switches. Then switching in the ring resonator matrix takes place. The advantages of the use of a wavelength selective switching matrix based on micro-ring resonators with respect to other types of silicon photonics switches using Mach–Zehnder switch elements [21] is that the various channels can be selectively switched and multiplexed into the output fibers by a single switching matrix without the need to use additional optical components and still keeping low the number of fiber ports in order to simplify the device packaging and its interconnection.

15.4 Perspectives and Research Directions

In this chapter new types of silicon photonics devices have been presented. They are able to perform a complete set of optical processing functions integrated in a photonic system on chip (PSoC) of a few square millimeters area, with potential low cost and low power consumption. Such devices, currently under investigation and in the initial phase of development, will be used in new fields of applications that are very sensitive to the cost, power consumption and footprint.

Among the different possibilities for photonic integration, silicon photonics looks the most promising thanks to its unique characteristics of high miniaturization of optical circuits (due to the high index contrast), potential low cost, and high yield (for the use of the well-developed CMOS production infrastructure used for electronic integrated circuits), and high energy efficiency (due to the tight integration with the control and driving electronics).

The two most critical parameters in the development of high integration level PSoC in silicon photonics are optical losses and crosstalk. The losses are generated by the integration of many cascaded blocks the signals has to traverse inside the chip and by the coupling between the sub-micrometric waveguides typically used in silicon photonics and the optical fibers. The sources of crosstalk that have to be carefully considered and minimized in the chip design arise from different mechanisms and are caused by the nonideal behaviour and limited isolation performances of the various circuits and blocks integrated in the chip: waveguide crossing, AWG-based multiplexers and demultiplexers, Mach–Zehnder-based circuits and micro-ring resonators that, with their Lorentzian-shaped transfer function, sometimes force the designers to use a coupled ring structure to improve the isolation performance.

The optical losses can be compensated by the use of optical amplifiers either in the form of external erbium-doped fiber amplifiers (EDFA), where possible, or in the form of semiconductor optical amplifiers (SOA) directly integrated within the silicon chip in a hybrid fashion. Various papers have been published on this matter

[22–24] and a promising technique to integrate, with low cost, III–V material into a SOI wafer with a wafer-scale CMOS process is reported in [25]. However, the number of integrated SOAs has to be kept to a minimum so as not to increase too much the power consumption and chip area and also avoiding yield degradation. The exploitation in the PSoC architecture of wavelength multiplexing at input and output ports is greatly beneficial. Investigations on the use of SOA with wavelength multiplexed signals have been reported in [26, 27].

To limit the crosstalk and in particular the more detrimental interferometric crosstalk, which arises when the disturbing channel and the wanted channel are at the same frequency, a careful design has to be carried out. For example, the use of two coupled micro-ring resonators instead of a single micro-ring implementation for the switch elements will give a sharper filter transfer function and a consequently higher isolation of unwanted channels even if at the expense of a higher circuit complexity.

Another important aspect to be considered is how the polarization is managed in PSoC. In fact, most of the silicon photonics circuits researched and demonstrated so far, are single polarization devices in which only the transverse electric (TE) mode is propagating and is processed. Polarization diversity structures look today to be the most viable solution to handling signals with an arbitrary state of polarization at the device input, but with the consequences of an increased chip area, increased complexity (needs to include polarization handling blocks) and higher losses.

Finally packaging of PSoC is a crucial challenge due to the many functions it has to provide, encompassing a low parasitic interconnection to the companion control electronic chip, low chip-to-fiber array coupling loss, high efficiency in removing the heat generated inside the chip, and mechanical robustness to protect the internal chip. All this function has to be provided with an assembly procedure that guarantees high throughput and low production cost.

The technique most used for fiber coupling to a silicon chip is based on grating couplers [28]. This has the benefit of a less stringent alignment tolerance and it opens the possibility of wafer level testing, but it has a limited wavelength bandwidth of 30–40 nm that may affect the performance of WDM systems operating in a large wavelength range.

To overcome this limitation for WDM systems a very promising assembling procedure based on the butt coupling technique has been proposed in [29] with potential for high throughput, relaxed alignment tolerance, and low cost.

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Chapter 16
Is Silicon Photonics a Competitive Technology to Enable Better and Highly Performing Networks?

Kensuke Ogawa and Kenji Nishide

Abstract This chapter focuses on the fundamental and high-speed characteristics of small-footprint integrated optical modulators designed and fabricated on the basis of the silicon-photonic platform to assess their key performance factors in applications related to high-capacity energy-efficient optical networks transmitting data in various modulation formats. The design and characteristics of high-speed silicon rib-waveguide phase shifters, which are most essential in the high-speed optical modulators, are described. A low-loss quasi-single-mode silicon rib-waveguide phase shifter with reduced *RC* delay is highlighted along with its design features and fundamental performances in terms of optical loss and on/off dynamic response. Free-carrier plasma dispersion is reviewed as a physical process for performing optical modulation, which allows a reduction in thermal drift and frequency chirping. The plasma dispersion has a unique property in that signal distortion due to residual intensity modulation cancels with the nonlinear voltage dependence of the optical phase, thereby being useful for zero-chirp optical modulators to eliminate transmission impairments. The on-off keying performance of a silicon optical modulator using a single Mach–Zehnder interferometer waveguide is described in the first example of optical network applications with emphasis on a 10-Gb/s dispersion tolerance comparable to that of a commercial lithium niobate modulator. The advantage of silicon-photonic integration is remarkable, in particular, for the ultrasmall-footprint silicon optical modulator consisting of a pair of IQ nested Mach–Zehnder interferometers for two orthogonal polarization components and a polarization multiplexer monolithically integrated on a silicon chip. Such a chip is presented with respect to applications in digital coherent communication in optical-fiber links up to 1000 km long at a bit rate as high as 128 Gb/s.

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16.1 Introduction

High-speed photonic components such as optical modulators operating at bit rates of 10 Gb/s or beyond play significant roles in efficient data transmission in modern optical systems and subsystems. They have been extensively deployed in long-haul optical-fiber telecommunications, and now are adapted to metro-area networks, datacoms, RF photonic links, and on-chip/on-board optical interconnects [1–9]. Photonic integration allows small-footprint high-efficiency photonic components to realize compact and energy-efficient systems and subsystems for high-speed optical data transmission.

There have been arguments in terms of the *pros and cons* of silicon photonics from the point of view of platform technology for monolithic and heterogeneous integration of photonic device blocks to build highly functional photonic integrated circuits (PICs) with both performances and manufacturing costs matching the requirements of the market in the field of high-speed optical networks [10, 11]. High-density integration based on high-index-contrast waveguide optics and low-cost fabrication using CMOS-based processes are favored for high-speed optical transceivers in small footprints, optical switches of high port counts, and so on. It has been often pointed out, however, that the optical and optoelectronic performances of silicon-based PICs do not parallel those of the competing counterpart devices made of electro-optic insulators or compound semiconductors, such as lithium niobate and indium phosphide, and thus provide limited capabilities of application in compensation for the potential benefits of integration and cost reduction.

To obtain an insight into the issue raised above, this chapter focuses on the fundamentals and high-speed characteristics of small-footprint integrated optical modulators designed and fabricated on the basis of the silicon-photonic platform to assess their key performance factors for applications in high-capacity energy-efficient optical networks transmitting data in various modulation formats. The optical modulators reviewed in this chapter are Mach–Zehnder (MZ) modulators because of their advantages of high-contrast modulation in the broad spectral ranges of the C and L bands [12] and chirp-free modulation under push-pull drive [4, 13, 14].

The chapter is organized as follows:

- In Sect. 16.2, the design and characteristics of silicon rib-waveguide phase shifters are described. Reverse-biased lateral PN-junction quasi-single-mode rib-waveguide phase shifters are the most essential parts of the high-speed optical modulators to achieve high-speed optical phase modulation with low optical loss [15]. The key points and efforts for reduction in optical loss and *RC* delay are described.
- In Sect. 16.3, free-carrier plasma dispersion, which is the physical process generating refractive-index modulation [16], is reviewed in the light of high-performance optical phase modulation. The broadband spectral response of free-carrier plasma dispersion, which is crucial to the suppression of thermal

drift and the wavelength dependence of optical phase modulation, is clarified based on the Drude model of conducting carriers in solids in contrast with compound semiconductor optical phase modulator based on quantum-well electroabsorption [17]. It is also shown that free-carrier plasma dispersion is suitable for the suppression of frequency chirping without transmission impairment, thereby endowing a zero-chirp optical modulator with a unique property that the signal distortion due to residual intensity modulation cancels with the nonlinear voltage dependence of optical phase.

- In Sect. 16.4, performances of zero-chirp silicon optical modulators are assessed in applications to data transmission using on-off keying (OOK), binary phase-shift keying (BPSK), quadrature phase-shift keying (QPSK) and dual-polarization quadrature phase-shift keying (DP-QPSK) modulation formats. The last modulation format is exploited for digital coherent communication in high-capacity high-spectral-efficiency optical transport networks at bit rates of 100 Gb/s and higher [18–21]. On-off keying performances of a silicon optical modulator using a single MZ interferometer waveguide at 10-Gb/s bit rate are described in the first example of optical network applications with emphasis on a dispersion tolerance comparable with that of a commercialized lithium niobate (LN) modulator. The advantage of silicon-photonic integration is remarkable, in particular, for the ultrasmall-footprint silicon optical modulator consisting of a pair of IQ nested MZ interferometers for two orthogonal polarization components and a polarization multiplexer integrated monolithically on a silicon chip, which is presented with respect to applications in digital coherent communication in optical-fiber links at distances up to 1000 km and at bit rates as high as 128 Gb/s.

16.2 Fundamental Characteristics of Rib-Waveguide Phase Shifter

16.2.1 Rib-Waveguide Phase Shifter in MZ Interferometer

The rib-waveguide phase shifter inserted in each arm of a MZ interferometer (MZI), as shown in Fig. 16.1, is most essential for high-speed modulation. The optical modulators including MZIs were fabricated on 200-mm diameter silicon-on-insulator (SOI) wafers by using 130-nm node CMOS fabrication processes [22]. The core of the rib waveguide is made of crystalline silicon of the SOI layer. The core is surrounded by top and bottom silicon-dioxide clads. A buried oxide (BOX) layer of the SOI wafer is used as the bottom clad. Silicon rectangular waveguides were used for the other parts of the MZI. The transverse-electric polarization (TE) is stable in the rib waveguide.

A depletion region is located at the boundary of the lateral PN junction in the middle of the rib core under application of a DC reverse bias to the junction. The horizontal width of the depletion region is controlled and thereby the effective

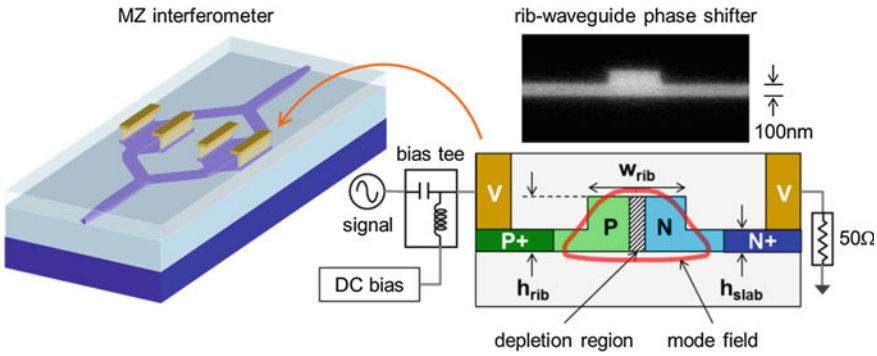

Fig. 16.1 Illustration and SEM image of cross section of rib-waveguide phase shifter inserted in each arm of MZ interferometer with the electrical connection schematic for DC bias and high-speed signal to the PN-junction of the phase shifter via vertical metal interconnect (V)

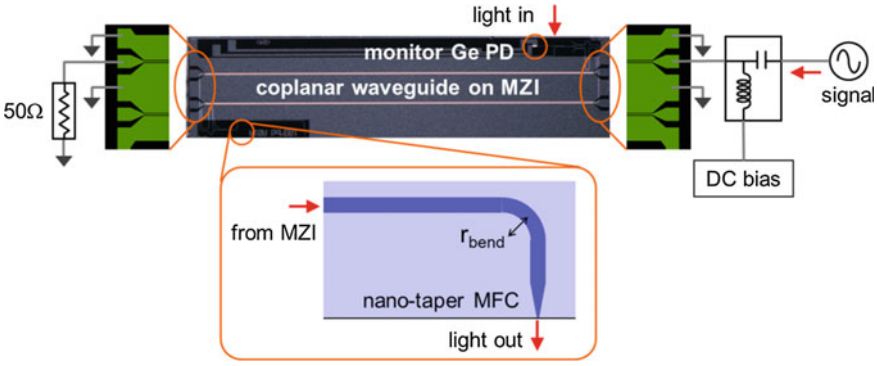

Fig. 16.2 *Top-view* image of an integrated silicon single MZI modulator chip with a schematic diagram of the electrical connection to contact pads on coplanar waveguide electrodes and an illustrated layout of the output waveguide end

refractive index of the rib waveguide is controlled with a signal voltage applied to the PN junction in conjunction with the DC reverse bias [23]. High-speed refractive-index modulation is induced by the high-speed drift motion of electrons and holes near the depletion region under the reverse bias [24].

High-speed electrical signals carrying data are input to a contact pad of a signal line electrode of a coplanar waveguide, which is connected to a rib-waveguide phase shifter in one arm of a silicon MZI through a bias tee, as shown in Fig. 16.2. The DC reverse bias to each phase shifter can be adjusted for optimum modulation performance. The coplanar waveguide was designed using short and straight signal electrodes without bending to eliminate RF signal distortion, thereby enhancing the electro-optic (EO) response beyond 33 GHz [12, 25].

Optical-fiber coupling using straight silicon waveguides connected to both ends of the silicon MZI is not allowed due to a clash with the RF bonding wires connected to the contact pads on the coplanar waveguide electrodes. To avoid this issue, input and output ends of the waveguides were placed on the side facets using high-index-contrast Si channel waveguide bends of 25-μm bending radius (r_{bend}), as shown in Fig. 16.2. The optical loss of the waveguide bends is as low as 0.04 dB per semicircle, and therefore negligible [12, 25]. The low-loss optical beam bending was integrated with the silicon MZI in a footprint as small as 5×1 mm^2 using the silicon-photonic platform. Inverted nano-taper mode-field converters (MFCs) were formed for edge coupling to optical fibers with a coupling loss <2.5 dB per facet [25]. A monolithic monitor Ge PD, which was integrated with a high-index-contrast mode splitter waveguide, allows low-loss performance monitoring of the MZ modulator [26].

16.2.2 Optical Loss Characteristics

Reduction in optical loss in the rib-waveguide phase shifter is crucial for the performance of high-speed silicon optical modulators in the light of the increase in optical signal-to-noise ratio (OSNR) for applications to optical transport networks [21]. Optical loss due to light scattering by side-wall roughness is a significant portion of the phase-shifter optical loss. There are two major paths to approach this subject. One is, of course, to utilize the most advanced CMOS fabrication processes capable of producing smooth and flat waveguide side walls with the finest lithographic and dry etching resolutions. Further reduction in the phase-shifter optical loss is achieved by the other approach including the design consideration of the rib-waveguide phase shifters and the optimization of dopant distribution surrounding the PN junction, as described below.

Light scattering at the rib-waveguide side walls becomes less significant if the width of the top part of the rib core, w_{rib}, is increased, because mode overlap with the side walls is weaker for a wider rib top since weaker tails exist at the side walls. Passive optical losses per unit length of silicon rib waveguides with different rib widths without any doping for the PN junction, averaged over 1545–1555 nm in C band and 1595–1605 nm in L band [27], are listed in Tables 16.1 and 16.2, respectively. The optical losses were measured in transverse-electric (TE) polarization, which is the propagation mode more dominant in the rib waveguides than transverse-magnetic (TM) polarization. The rib waveguides were fabricated using an SOI wafer having a 220-nm thick SOI layer with waveguide dimension parameters, $h_{rib} = 220$ nm and $h_{slab} = 95$ nm, respectively.

A rib waveguide with a wider rib core is favorable for the phase shifters in terms of lower passive optical loss. There is another aspect to be considered, however, to realize high-performance optical modulation using the silicon rib-waveguide phase shifters. Higher-order modes exist as guided modes in the rib waveguides if the rib width is wider than 400 nm. The propagation of higher-order guided modes results

Table 16.1 Optical loss of silicon rib waveguides averaged over 1545–1555 nm in C band

Rib width	400 nm	500 nm	600 nm
loss	0.107 dB/mm	0.074 dB/mm	0.057 dB/mm

Table 16.2 Optical loss of silicon rib waveguides averaged over 1595–1605 nm in L band

Rib width	400 nm	500 nm	600 nm
loss	0.084 dB/mm	0.071 dB/mm	0.055 dB/mm

in performance degradation in optical modulation due to reduction in the on/off extinction ratio in intensity modulation or the Q factor in phase modulation. The higher-order mode propagation must be eliminated for high-performance optical modulation. Profiles of absolute electric fields of the fundamental and first higher-order modes are plotted for rib widths of 400–600 nm in Fig. 16.3. The first higher-order mode is not confined in the rib core and radiated out of it. Single-mode propagation is assured for the 400-nm rib waveguide. The first higher-order mode with a rib width wider than 400 nm, on the other hand, is more strongly localized within the central rib area and more stably propagated through the phase shifter waveguide. The mode profiles in TE polarization were obtained by the film-mode-matching method [28].

Optical attenuation is caused by the optical absorption by free electrons and holes introduced in the PN-junction and adjacent areas by a series of P-and N-doping processes. The higher-order modes are attenuated much more significantly than the fundamental mode if highly doped P+ and N+ areas are formed in the side slab parts of the rib waveguides, as illustrated in Fig. 16.1, because the higher-order modes are more extended towards the side slab wings. The concentration of dopants is typically on the order of 10^{17} cm^{-3} for the P and N areas around the central PN junction and on the order of 10^{18} cm^{-3} in the P+ and N+ areas in the side slab parts, respectively. The carrier-induced optical absorption is, therefore, ten times higher in the P+ and N+ areas than in the central PN junction [16]. The fundamental mode is strongly localized in the central rib part and attenuated negligibly due to the high carrier-induced optical absorption in the side slab parts. With the formation of the side P+ and N+ areas, quasi-single-mode propagation is thereby allowed for the rib-waveguides having a rib width wider than 400 nm. In the simulation of the mode fields, h_{rib} and h_{slab} are 220 and 95 nm, respectively, as in the fabricated waveguides. A rib width of about 500 nm is the optimum choice for an on/off extinction ratio as high as 14 dB at a symbol rate of 10 Gbaud with an on-chip phase shifter optical loss as low as 3 dB [15]. Greater reduction in the phase shifter loss is possible by using a wider rib width, but with a reduction in the extinction ratio as the electric field of the first higher-order mode is less extended towards the side wings. One can further optimize the rib width in terms of the extinction ratio and the optical loss with the accumulation of simulation data on the phase shifters.

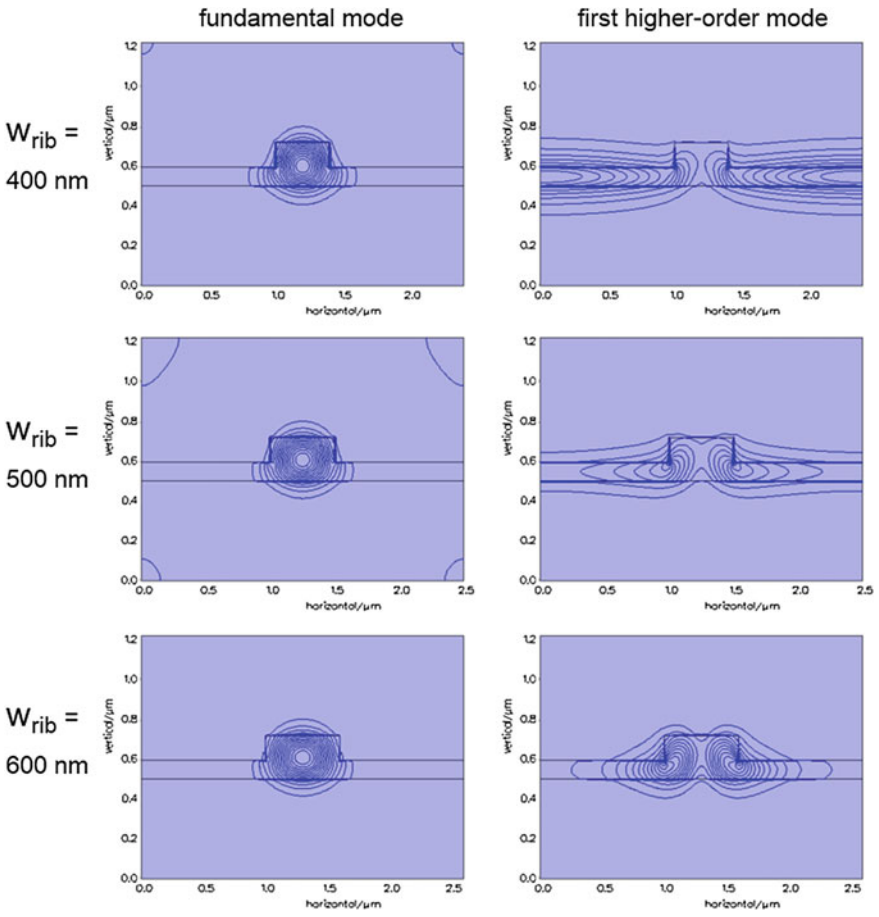

Fig. 16.3 Electric-field contour profiles of fundamental and first higher-order modes in TE polarization in silicon rib waveguides with rib widths of 400, 500, and 600 nm

DC reverse bias dependences of optical phase shift and optical loss were obtained numerically by the simulation of the carrier distribution profile in the PN junction in the silicon rib-waveguide phase shifter with W_{rib} = 500 nm in conjunction with optical-mode-field simulation. The simulation of the two-dimensional electron and hole distribution profile was performed by means of a finite-element solver for the charge continuity and carrier transport equation combined with the Poisson equation. A dopant profile similar to that presented in the literature was adopted [22]. Electron and hole concentrations in N and P areas in the PN junction are 2×10^{17} cm^{-3} and 5×10^{17} cm^{-3}. The carrier distribution profile was converted to a refractive-index profile in the rib waveguide using the empirical formula on the free-carrier plasma dispersion [16, 29]. Higher free-carrier concentration leads to lower refractive index in crystalline Si.

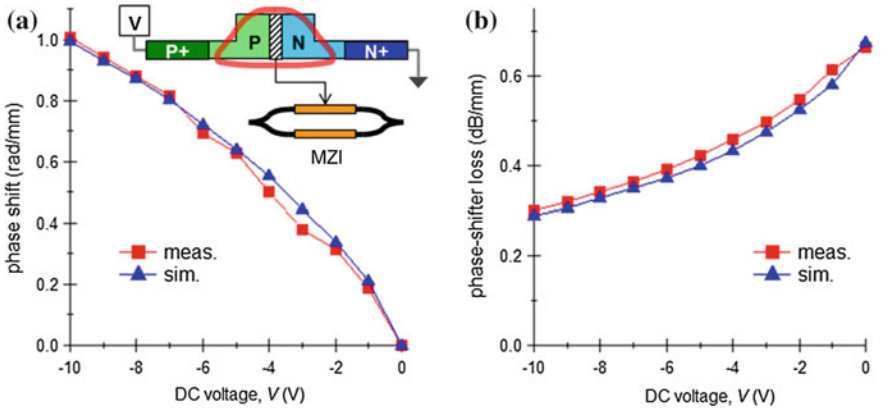

Fig. 16.4 DC reverse bias dependences of the phase shift and optical loss per unit length in a Si rib-waveguide phase shifter

The mode-field simulation using the simulated refractive-index profile in the rib-waveguide phase shifter was based on the beam propagation method [30], which was proven to generate solutions for the mode-field profiles almost the same as those by the film-mode-matching method. The simulated phase shift and carrier-induced optical loss, as plotted in Fig. 16.4, coincide well with the experimental results. This implies that the phase shifter was fabricated with the precise specifications as designed. Further reduction in π-shift voltage, V_π and enhancement of the phase shifter efficiency are possible by design optimization on the doping profile. A voltage-length product defined as $V_\pi \ell$ is a measure of the phase shifter efficiency, obtained as 2.5 V·cm at a reverse bias of –5 V. The residual intensity modulation due to the carrier-induced optical loss is negligible according to the analysis in the literature [14]. The characteristics of the residual intensity modulation are further analyzed with respect to frequency chirping in the next section.

A simultaneous reduction in V_π and the phase-shifter optical loss is not achieved only by adjustment of the doping concentration. Special design improvement is required to overcome this technical difficulty. One of the approaches to this task was adopted by introducing low-doped side-wall areas into the rib-waveguide phase shifters. The low-doped side wall areas, which were formed by compensation doping, namely counter doping to reduce carrier concentration via recombination of carriers of opposite charge polarities, were adopted and proved to be effective for reduction in carrier-induced optical loss without increase in V_π. [31]. The DC performance of a compensation-doped silicon rib-waveguide phase shifter is evaluated in the DC figure of merit (FOM) plotted in Fig. 16.5 as a function of DC reverse bias voltage, V. DC FOM is defined as

$$\mathrm{FOM} = \frac{\pi}{\alpha \ell V_\pi} \tag{16.1}$$

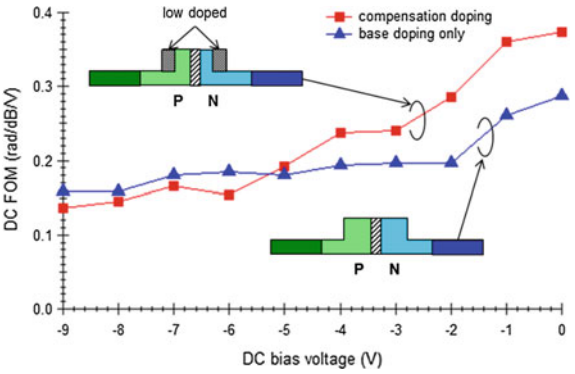

Fig. 16.5 DC FOM plotted against DC reverse bias voltage for silicon rib-waveguide phase shifters with base-doping only and with compensation doping

in which α and ℓ are optical loss per unit length and phase shifter length, respectively. At a DC voltage above –2 V, DC FOM is enhanced almost 30 % in the compensation-doped phase shifter in comparison with the phase shifter with base doping only, which is the rib-waveguide phase shifter shown in Fig. 16.1. The DC FOM of the compensation-doped structure is slightly lower than that with base doping only at a DC voltage below –6 V, because the depletion region is extended closer to the side walls. Optical modulation with lower optical loss at a lower RF voltage is allowed with the compensation-doped phase shifter at a total voltage not lower than –6 V. The electro-optic (EO) responses presented in this section and the high-speed modulation performances in various network applications in the next section were acquired with silicon MZI modulators with compensation-doped phase shifters.

16.2.3 Series Resistance Reduction for Shorter RC Delay

In applications to high-capacity optical networks, *RC* delay is one of the major factors limiting the performances of reverse-biased silicon PN-junction phase shifters. Reduction in the series resistance *R* is crucial, in particular, to preserve V_π as low as possible, because high capacitance is essential for efficient modulation of the carrier concentration, and hence efficient refractive-index modulation in the PN junction. The slab wings in both sides of the central rib core are a resistance bottleneck and adjustment of the slab height h_{slab} is required to reduce the series resistance in the rib waveguide, as shown in Fig. 16.6.

A remarkable reduction in *RC* delay, thereby shortening the rise and fall times in on/off intensity modulation traces, was confirmed for a silicon single MZI modulator having rib-waveguide phase shifters with h_{slab} = 95 nm in comparison with that with h_{slab} = 60 nm [17]. The rise and fall times were measured by applying a square-like periodic RF waveform to a phase shifter in one arm of MZI in each modulator. Mean rise and fall times in the input RF waveform are 20.8 and 21.4 ps.

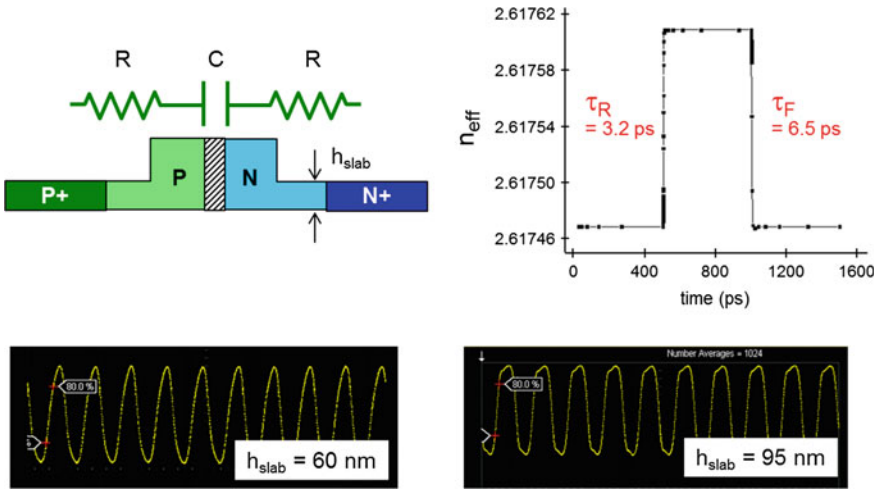

Fig. 16.6 Equivalent circuit model of a silicon rib-waveguide phase shifter, numerical response without series resistance and on/off modulation traces for the phase shifters with h_{slab} = 60 and 95 nm, respectively

In the output waveforms, mean rise and fall times are 39.8 and 29.0 ps for the modulator with h_{slab} = 60 nm, and are 22.2 and 21.5 ps with h_{slab} = 95 nm. The reduction in the rise time is more than 17 ps in good agreement, within the limit of measurement time resolution, with the estimation based on the equivalent circuit model as below. The highly doped side P+ and N+ areas are also advantageous for low series resistances with shorter *RC* delay. The fall-time reduction is 7.5 ps, limited by the response time of the measurement apparatus consisting of a main frame of sampling oscilloscope and a plug-in unit for optical detection.

The *RC* delay time for a rib-waveguide PN-junction phase shifter, τ, is represented as

$$\tau = 2\mathrm{RC} \tag{16.2}$$

with series resistance in a slab wing in each side, R and capacitance of the PN junction, C [15]. The series resistance R is reduced from 8.2 to 5.7 Ω with h_{slab} increased from 60 to 95 nm. The capacitance C is 1.6 pF for a 4 mm-long phase shifter at DC reverse bias voltage below –2 V [22]. Therefore, τ is estimated as 18 ps in the phase shifter with 95-nm slab wings, while as 26 ps for that with 60-nm slab wings. This leads to a reduction in each of the rise and fall times by 16 ps in the output optical waveforms.

The transient refractive-index response was obtained numerically from the time-dependent solution of the two-dimensional electron and hole distribution profile, as plotted in Fig. 16.6. The series resistance was not incorporated in the device model and the total response time, $\tau_R + \tau_F$ is 9.7 ps. The frequency response of the phase shifter is thus as fast as 100 GHz. Further reduction in the series

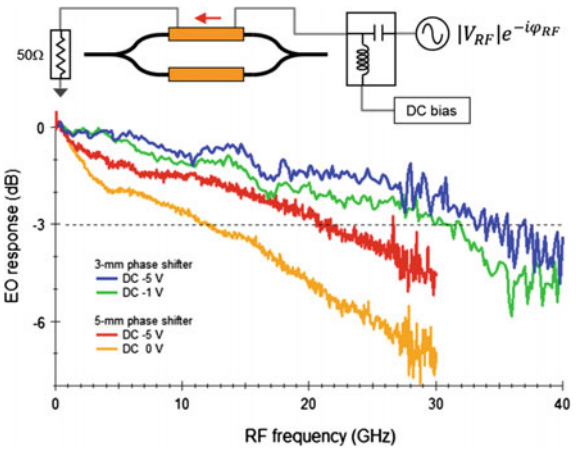

Fig. 16.7 EO responses of Si MZI modulators with 3 and 4-mm phase shifters and illustrated configuration for RF signal and DC bias in the S-parameter measurement

resistance and improvement in the EO response, as described next, will allow optical modulation at symbol rates up to 100 Gbaud and higher with the reverse-biased lateral PN-junction rib-waveguide phase shifter.

16.2.4 EO Response

EO responses of silicon single MZI modulators with 3 and 5-mm phase shifters with W_{rib} = 500 nm obtained in S-parameter measurements are shown in Fig. 16.7 [12, 25]. The RF sinusoidal signal from a vector network analyzer was fed through a bias tee with a DC reverse bias voltage to a phase shifter in one arm of the silicon MZI modulator under test. Optical output from the modulator was input to a detection port of the network analyzer. There are two major factors that limit the EO response of the single silicon MZI modulators. One is RF loss in the phase shifter and the other is *RC* delay, as the roll-off frequency decreases with longer phase shifter length and stronger DC reverse bias voltage, respectively. A stronger DC reverse bias voltage leads to a lower PN-junction capacitance due to added expansion of the depletion region.

The roll-off frequency at 3-dB attenuation is as high as 33 GHz in the EO response of the silicon MZI modulator with 3-mm phase shifters. This allows a phase modulation in QPSK at 64 Gb/s and in DP-QPSK at 128-Gb/s, respectively. A longer phase shifter length is more preferable for optical modulation at lower symbol rates such as 10 Gbaud in OOK format with an advantage of a lower V_{π}. One can adjust the phase-shifter length according to requirements and specifications for the optical network under consideration.

16.3 Free-Carrier Plasma Dispersion for High-Speed Silicon Optical Modulator

16.3.1 Energy Transfer in Drude Theory

High-speed refractive-index modulation in silicon optical modulators is based on the free-carrier plasma dispersion, which is the real part of optical response of charged free carriers interacting with the optical field [16, 32–39]. The imaginary part of the optical response is free-carrier absorption, which has been extensively studied in semiconductors [40–52]. The kinetic energy and velocity of the charged free carriers are depicted schematically against time t in Fig. 16.8. The velocity increases linearly, while the kinetic energy increases quadratically with constant magnitude of the optical field. The optical response is suitable for optical modulators operating in a broad spectral range, such as the C and L bands, because the interaction is nonresonant and occurs irrespective of the wavelength of the incident optical field. Unbound individual carriers are involved in the interaction, and generate a negative refractive-index change with respect to an increase in carrier concentration, which is crucial for the elimination of frequency chirping as described below.

In case (a), where no scattering, or no dephasing, in other words, occurs, the charged carriers are accelerated coherently without disruption in the optical field and the energy of the optical field is transferred efficiently to the charged carriers. The optical-to-electronic energy transfer is inefficient, on the other hand, in case (b), where the charged carriers are not accelerated coherently due to dephasing in the carrier scattering. A large refractive-index change and a high optical absorption are

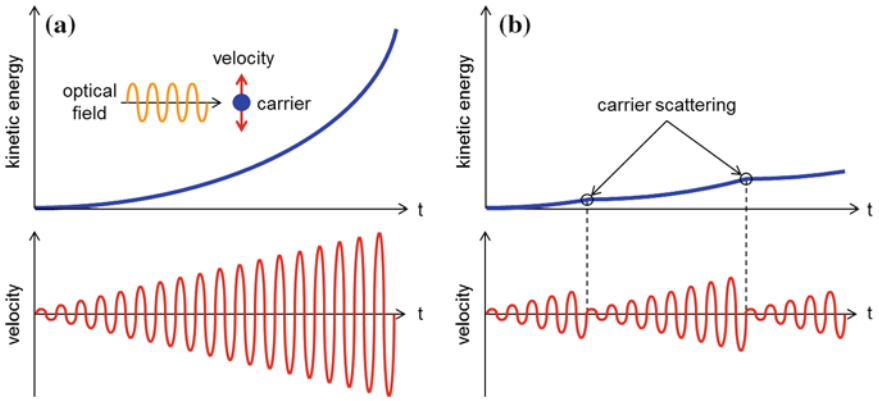

Fig. 16.8 Time evolution of the kinetic energy and velocity of charged free carriers interacting with the optical field in the case of carrier transport with no carrier scattering (**a**) and with carrier scattering (**b**)

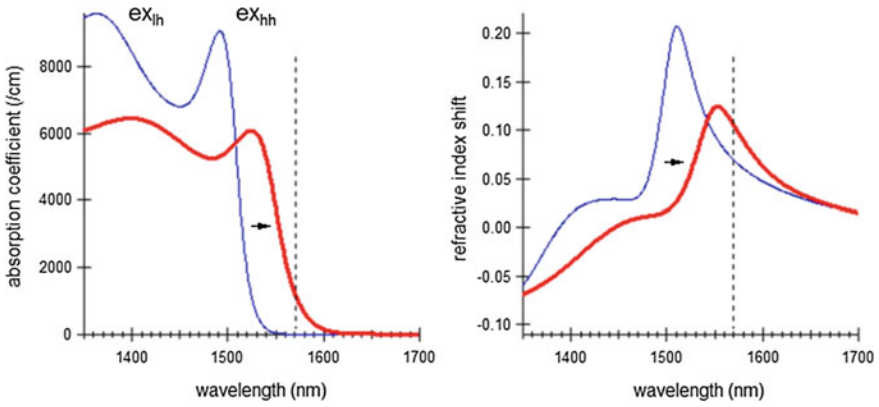

Fig. 16.9 Numerical optical absorption and refractive-index spectra for two-dimensional excitons in quantum well under zero bias (*thin curves*) and reverse bias (*thick curves*)

generated thereby if the charged carriers yield a high mobility according to the classical model of charged carrier transport [53]. Electronic band engineering for higher carrier mobility is an essential approach for a lower V_π in silicon-based optical modulators [54].

The refractive-index change in free-carrier plasma dispersion, Δn and optical loss change in free-carrier absorption, $\Delta\alpha$ are represented within the framework of Drude theory according to the following proportionalities [37]

$$\Delta n \propto -(N_e/m_e + N_h/m_h) \tag{16.3}$$

$$\Delta\alpha \propto -\left(N_e/m_e^2\mu_e + N_h/m_h^2\mu_e\right) \tag{16.4}$$

where, N_e, N_h, m_e, m_h, μ_e, and μ_h denote the electron concentration, hole concentration, electron effective mass, hole effective mass, electron mobility, and hole mobility, respectively. The key feature to note in these equations is that the refractive index change is negative for positive change in the optical loss. This characteristic is inherent to polarizability in the nonresonant optical response of free carriers [55] and crucial to zero-chirp modulation, as described in terms of frequency chirping below. In contrast, the refractive-index change in the quantum-confined Stark effect (QCSE) yields a positive change, which is opposite in sign to the free-carrier plasma dispersion, for a positive change in the optical loss in a wavelength region below the band edge of semiconductor quantum wells [17, 56] with optical absorption and refractive-index characteristics as schematically presented in Fig. 16.9. Model numerical spectra for the heavy-hole exciton (ex_{hh}) and light-hole exciton (ex_{lh}) in quantum wells were taken from the literature [57]. The QCSE is based on the resonant dipole transition of bound electron-hole states.

16.3.2 TEC-Free DC Optical Characteristics

The broadband nonresonant optical response of free carriers has the advantage of optical modulation in a wide temperature range without the need for a thermo-electric cooler (TEC). The change in silicon refractive index due to the thermo-optical effect [58] is not substantial and the optical phase drift induced by heat flow from adjacent active devices can be compensated by adjustment of the DC reverse bias voltage only. Evidence of TEC-free operation of a silicon optical modulator is presented as a DC bias voltage dependence of optical transmittance in Fig. 16.10. The device under test was a silicon single MZI modulator assembled on a chip carrier in a ceramic-based metal package, which is capable of 10-Gb/s OOK transmission in a 100-km link of single-mode fiber (SMF) at 25 °C [25]. Peak transmittance and dip wavelength were maintained between 20 and 80 °C with adjustment of the DC bias voltage applied to one of the MZI arms without a TEC. Therefore, the silicon optical modulator is a candidate for a small-footprint low-cost optical modulator operating in a TEC-free environment.

16.3.3 Frequency Chirping

Zero-chirp modulation is crucial for high-capacity signal transmission in optical transport networks with a high-spectral efficiency [18–21]. A MZI modulator is

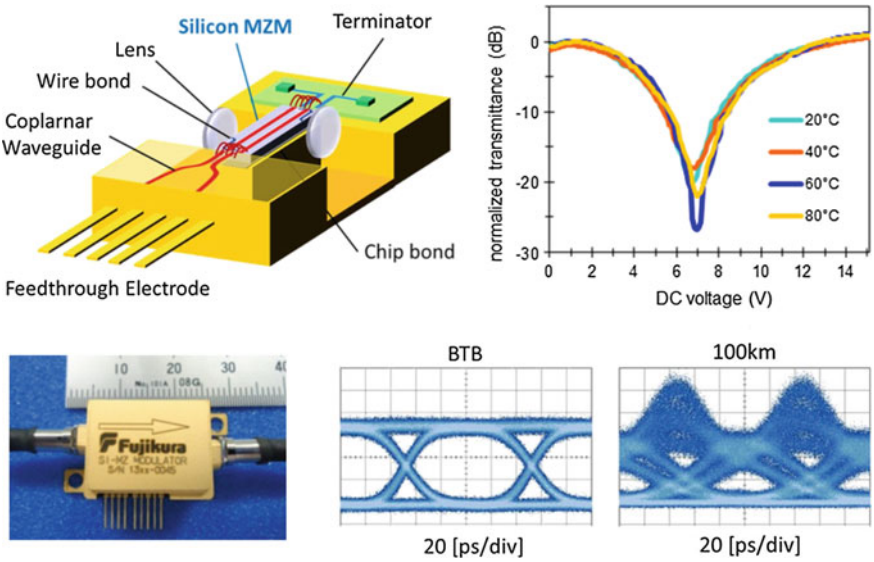

Fig. 16.10 Illustrated are a SI MZI modulator on a chip carrier, the DC bias voltage dependence of the normalized transmittance at temperatures between 20 and 80 °C, a modulator module assembled in a ceramic-based metal package, and 10-Gb/s eye diagrams in back-to-back (BTB) and in 100-km SMF transmission

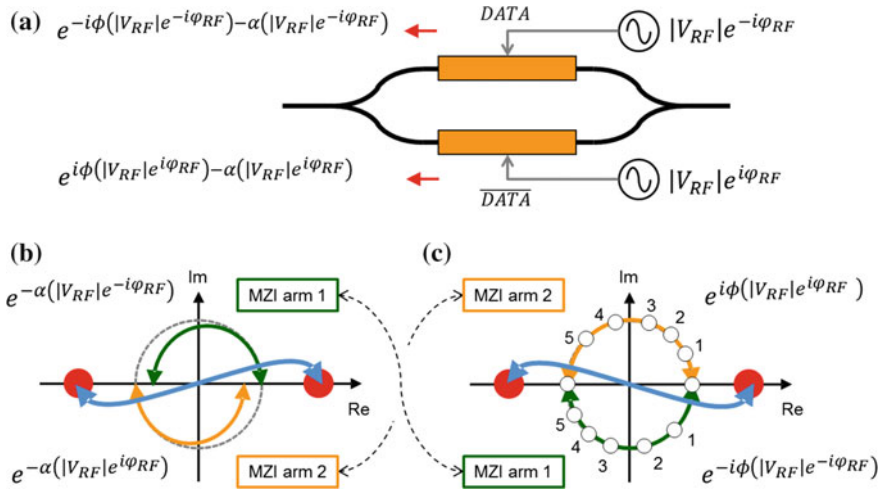

Fig. 16.11 **a** Configuration of RF signals and generated optical waves in each arm of the MZI in push-pull drive. **b** Schematic signal distortion due to the residual intensity modulation represented on a constellation diagram. **c** Schematic signal distortion due to the nonlinear bias dependence of the optical phase represented on a constellation diagram

capable of zero-chirp modulation in a wide spectral range extending over the C and L bands under push-pull drive [4, 13, 14]. It has been often argued that zero-chirp modulation may not be available for silicon optical modulators, because of the intensity modulation based on the free-carrier absorption as the counter part of refractive-index modulation based on the free-carrier plasma dispersion. However, this is not the case with silicon MZI modulators in which reverse-biased lateral PN-junction phase shifters are placed. Signal distortion due to the intensity modulation is compensated by the nonlinear voltage dependence of the phase shift, as illustrated in Fig. 16.11.

In push-pull operation, RF signals in opposite polarities are applied to the respective arms of the MZI, as depicted in Fig. 16.11a. Signal distortion due to the residual intensity modulation is indicated in the constellation diagram in Fig. 16.11b. The distortion is caused by the asymmetric intensity modulation between the two arms of the MZI. Another signal distortion in Fig. 16.11c is generated by the nonlinear voltage dependence of the optical phase shift, as shown in the experimental and numerical characteristics of the phase shift in Fig. 16.4. The latter signal distortion, which is 180° reversed against the distortion due to the residual intensity modulation, cancels with the former signal distortion. Quasi-zero-chirp modulation is thus possible for a silicon MZI modulator with reverse-biased lateral PN junction phase shifters. The inversion of the signal distortion is a consequence of the negative sign in (16.3), inherent to the nonresonant optical response of free carriers in semiconductors over a broad spectral range.

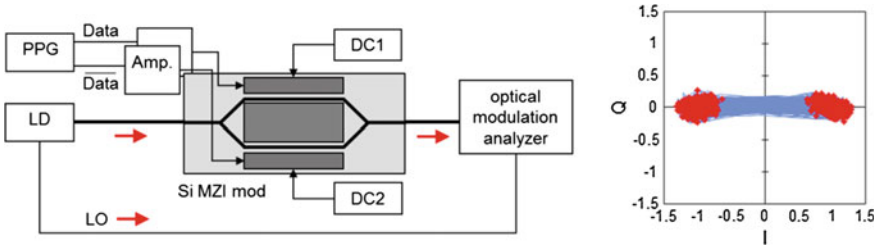

Fig. 16.12 Measurement block diagram and constellation diagram for 22.3 Gb/s BPSK in back-to-back characterization

Quasi-zero-chirp modulation has been confirmed for 22.3-Gb/s BPSK modulation, as presented in Fig. 16.12. The constellation was measured for a back-to-back BPSK signal for confirmation of zero-chirp modulation. In the constellation measurement, the optical signal output from a Si single MZI modulator was input to 90° optical hybrid circuit for coherent homodyne detection and transients of in-phase (I) and quadrature (Q) electric signals were acquired by a real-time oscilloscope. In the BPSK constellation diagram, trajectories in bit transmission are laid along the real axis with residual chirp $|\alpha| < 0.1$. Zero ($x = 1$) and π ($x = -1$) bits are indicated as red points and trajectories of transition between the two bits are in light blue. The trajectories are linear and located on the real axis (x axis) with no imaginary part ($y = 0$).

16.4 Silicon Optical Modulators in High-Capacity Optical Networks

16.4.1 On-off Keying Characteristics

Extensive efforts have been devoted to silicon OOK modulators [59–62]. High-speed OOK modulation has been achieved using a push-pull silicon MZI modulator with reverse-biased lateral PN-junction phase shifters and back-to-back performances have been reported with an extinction ratio of 3.8 dB at 60 Gb/s [62]. High-contrast OOK modulation with an extinction ratio beyond 10 dB was reported and the bit error rate (BER) was characterized for a push-pull silicon single MZI modulator at 11.1 Gb/s [14].

In BER measurements using a BER tester (BERT), different lengths of SMF (20, 40, 60, and 80 km) with a positive dispersion parameter of 17 ps/nm/km at 1550 nm were used. BER measurements were also performed for a negative dispersion parameter using dispersion compensation fiber modules (DCFMs) designed for dispersion compensation for 20, 40, 60, and 80-km SMFs, respectively. The modulation format applied was a 11.1-Gbps nonreturn-to-zero OOK (NRZ-OOK) and pseudo-random bit stream (PRBS) in a bit length of 2^{31}–1 from a pulse-pattern generator (PPG). To avoid BER degradation due to a fluctuation in clock timing, a

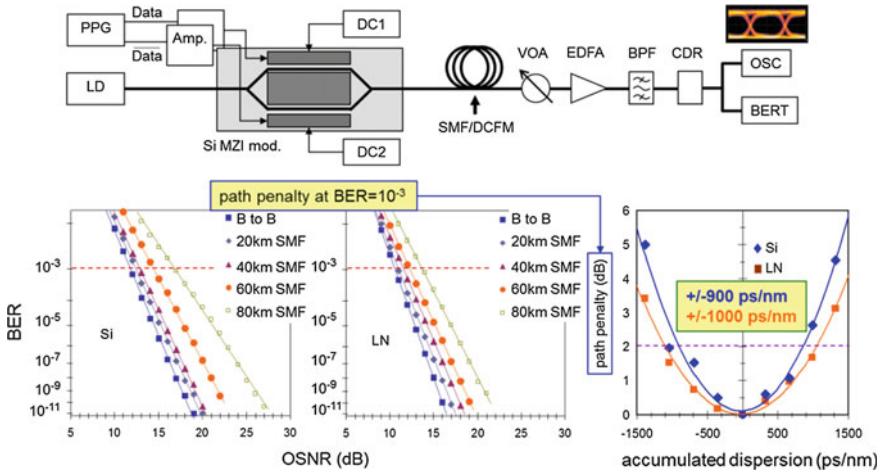

Fig. 16.13 Measurement block diagram for transmission experiments in zero-chirp modulation (*upper*) and characteristics of BER and dispersion tolerance in comparison with a LN modulator (*lower*)

clock data recovery (CDR) unit was incorporated to the receiver unit. The wavelength from a single-mode laser source (LD) was 1550 nm. For BER measurements with variable OSNR, the noise source was amplified spontaneous emission (ASE) in an Er-doped fiber amplifier (EDFA). Control of OSNR was provided by variable attenuation of the transmitted optical signals at a variable optical attenuator (VOA). The bandwidth of ASE was limited by an optical bandpass filter (BPF) within 1-nm full bandwidth at 3-dB attenuation. The OSNR was independently measured by an optical spectrum analyzer with 0.1-nm resolution bandwidth for the noise component as used in other transmission experiments [63]. Eye diagrams were acquired using a sampling oscilloscope (OSC) instead of BERT.

The BER characteristics for the Si MZI modulator and a LN single MZI modulator are plotted in Fig. 16.13. The Si MZI modulator yields a BER performance similar to the LN MZI modulator. The dispersion penalty at a BER of 10^{-3} is also plotted for both MZI modulators in Fig. 16.13.

The accumulated dispersion in the horizontal axis corresponds to the accumulated chromatic dispersion in the respective fiber lengths for SMFs or DCFMs. The dispersion penalty of the Si MZM is very close to that of the LN MZI modulator and almost symmetric with respect to the minimum at zero dispersion (back to back). The zero-chirp modulation in the Si MZI modulator is thus confirmed also in the characteristics of the dispersion penalty. The dispersion penalty of the Si MZI modulator is approximately 2-dB higher at 1320 ps/nm/km (80-km SMF) in comparison with that of the LN MZI modulator. It can be eliminated with further enhancement of high-speed performance of the Si MZI modulator by more precise adjustment of the impedance matching of the traveling-wave electrodes and high-conductivity metallization in the RF regime [64].

16.4.2 Phase-Shift Keying Characteristics

16.4.2.1 Bpsk

The transmission performance of the Si single MZI modulator was evaluated in BPSK at a bit rate of 22.3 Gb/s (11.1-Gbaud symbol rate). The Si MZI modulator was driven in push-pull mode at 8-Vpp amplitude. The actual bitrate of 22.3 Gb/s was intended for 20-Gb/s transmission with accommodation of forward error correction. Eye diagrams and BER measurements were performed in direct differential detection using a 1-bit delay line interferometer (DLI) connected to a balanced photodetector (PD), as depicted in Fig. 16.14. The two types of transmission fibers were used as in the OOK measurements: SMFs for distances up to 20 km and DCFMs, allowing BER measurements with positive and negative accumulated dispersion ranging from –347 to +334 ps/nm. The electrical signal output from the balanced PD was detected with BERT. In eye-diagram measurements, a sampling oscilloscope was connected to the balanced PD instead of the BERT.

Eye diagrams of the BPSK signals with positive and negative accumulated dispersion after transmission through the SMFs and DCFMs are presented in comparison with the back-to-back eye diagram in Fig. 16.14. The eye opening is closed and the signal waveform is more distorted on account of a more highly accumulated dispersion with increasing transmission distance. Eye diagrams with almost the same magnitude of accumulated dispersion are similar each other due to zero chirping in the optical signal generated in the Si MZI modulator.

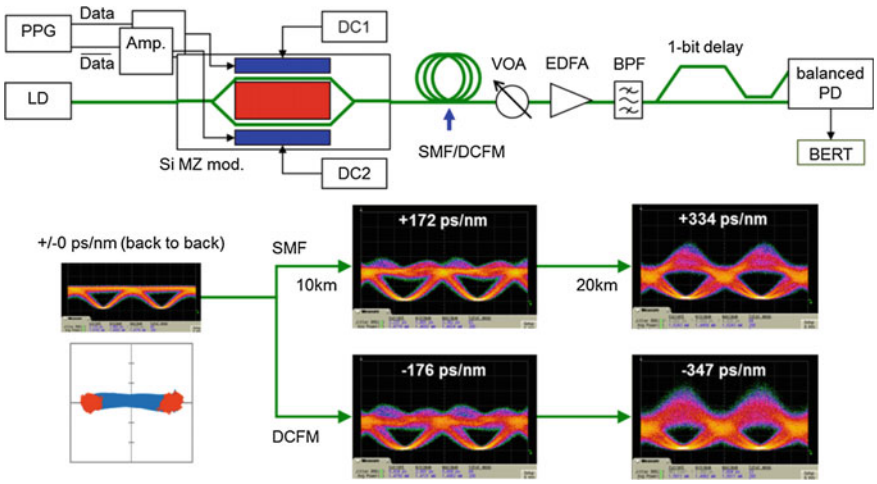

Fig. 16.14 Measurement block diagram for differential detection in BPSK (*upper*) and transmission eye diagrams (*lower*)

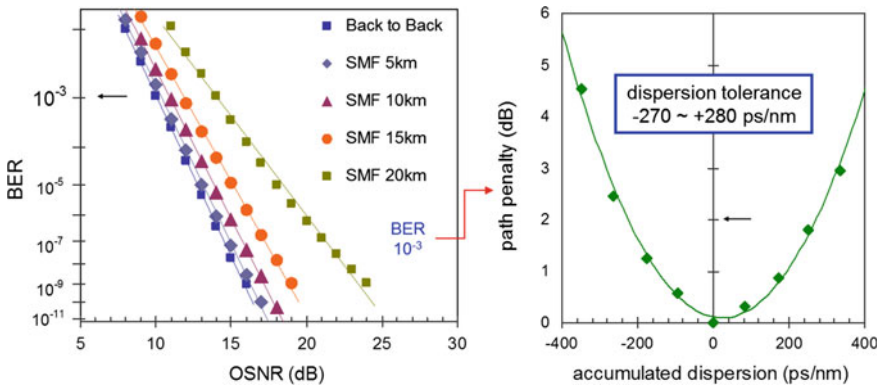

Fig. 16.15 BER characteristics in SMF transmission up to 20 km and the dispersion tolerance obtained from path penalty characteristics

BER characteristics are plotted in Fig. 16.15 as a function of OSNR for transmission through the SMFs. The BER has been measured also for transmission through the DCFMs. The path penalty is obtained as an OSNR penalty in the fiber transmission at BER = 10^{-3} (indicated with an arrow). Path penalty is plotted against accumulated dispersion in Fig. 16.15. The points in the positive side of accumulated dispersion are obtained for transmission through the SMFs, and those in the negative side for transmission through the DCFMs. The solid curve is a fitting curve using a quadratic dependence on accumulated dispersion. The path penalty is symmetric around zero accumulated dispersion, implying zero-chirp modulation. The accumulated dispersion for 2-dB path penalty is –220 and +230 ps/nm. From these values, the dispersion tolerance is 550 ps/nm with 13-dB OSNR. The Si MZI modulator can be used as a small-footprint modulator for 20-Gb/s data transmission in BPSK.

16.4.2.2 Qpsk

Figure 16.16 shows the top-view photograph of a silicon IQ modulator chip for QPSK, which was fabricated on an 8-inch SOI wafer using CMOS compatible processes. The modulator consists of a nested IQ MZI. The nested IQ MZI has two sub-MZIs for I and Q components, respectively, including the rib-waveguide lateral PN-junction phase shifters connected to straight coplanar-waveguide electrodes. The electrodes are connected to input and output contact pads at the edge of the modulator chip with a minimum length without bend waveguides. This design minimizes RF propagation loss on a silicon wafer. A thermo-optic (TO) DC phase shifter allows phase adjustment to sustain a $\pi/2$ phase difference between I and Q sub-MZIs for stable QPSK modulation. These device blocks were monolithically integrated in a footprint as small as 3.5 × 2.9 mm^2. Phase shift and optical loss of the silicon rib-waveguide phase shifter with a 3-mm length were measured using a test sample

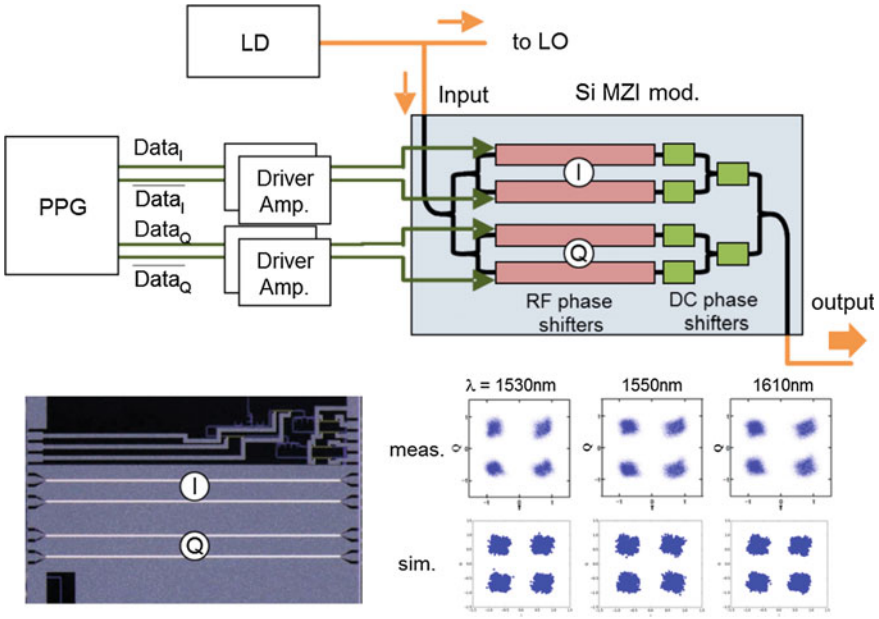

Fig. 16.16 Layout of silicon QPSK modulator chip and measurement block diagram (*upper*) and *top-view* photograph of a small-footprint monolithic QPSK chip with measured and simulated constellation diagrams (*lower*)

of an asymmetric silicon MZI waveguide. V_π is 7.5 V and the optical loss is as low as 2.7 dB at zero bias voltage and 1.9 dB at 5-V reverse-bias voltage, respectively.

The output laser beam from the LD was split into two paths: input light to the modulator and local oscillator (LO) light for homodyne coherent detection in the optical modulation analyzer. Measured and simulated QPSK constellation diagrams of the silicon IQ MZI modulator at 64 Gb/s (32-Gbaud symbol rate) at wavelengths of 1530, 1550, and 1610 nm are plotted in Fig. 16.16. Bit spots are clearly resolved in the measured constellation diagrams. Therefore, 64-Gb/s QPSK modulation is confirmed for the Si IQ MZI modulator. The advantage of a powerful 3rd-generation forward error correction (FEC) in 50-Gb/s QPSK transmission [65] can be accommodated in a capacity of the full transmission rate as high as 64 Gb/s.

Good agreement of the simulated constellation diagrams with the measured diagrams was obtained [66]. Silicon optical modulators for QPSK application can be designed and fabricated on the basis of the silicon photonic platforms for design and fabrication.

16.4.2.3 Dp-Qpsk

A silicon MZI modulator designed for 128-Gb/s DP-QPSK application at 32-Gbaud, in which 3-mm silicon rib-waveguide lateral PN-junction phase shifters

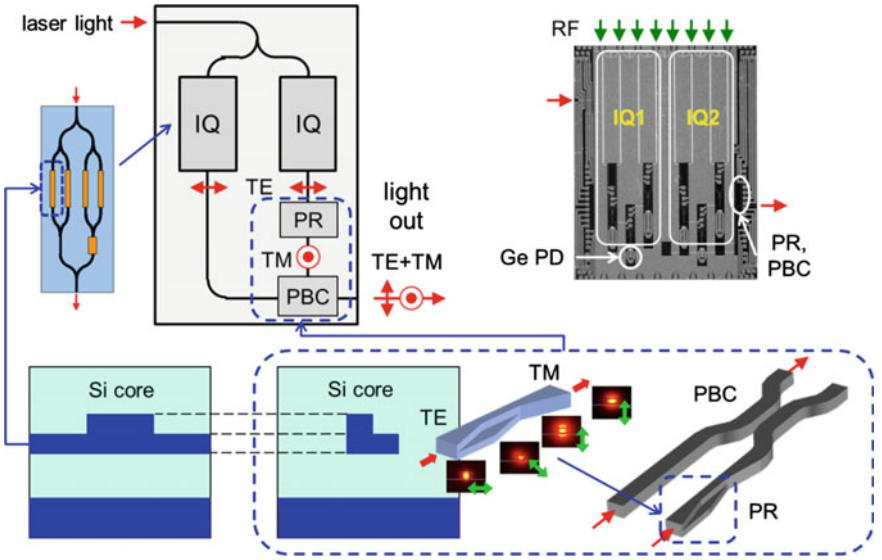

Fig. 16.17 Layout and *top-view* photograph of an ultrasmall-footprint monolithic silicon PDM IQ modulator with the illustrated PDM optical circuit

for IQ modulation were disposed in each arm of IQ MZIs, was fabricated as shown in Fig. 16.17. The Si MZI modulator consists of two IQ MZI modulator units and a waveguide circuit for polarization-division multiplexing (PDM).

A silicon PDM IQ MZI modulator consists of the following four blocks: (16.1) an input waveguide split into two parallel waveguides with a multi-mode interferometer, (16.2) two IQ MZI modulators, each of which consists of a silicon nested MZI incorporating silicon single sub-MZIs on both parent MZI arms and operating in TE polarization, (16.3) a polarization rotator (PR), with which the polarization of the light after one of the IQ MZMs is converted to transverse-magnetic (TM) polarization and (16.4) a polarization beam combiner (PBC) to multiplex TE and TM polarization outputs [67, 68]. A Si PDM IQ MZM was monolithically integrated in an ultrasmall footprint of 6.5 × 5 mm^2 with Ge PDs for performance monitoring and Si rib-waveguide TO DC phase shifters to the adjust phase difference to $\pi/2$ between I and Q components in each polarization. The rib-waveguide-based PR in PDM circuit was designed with common design rules for the rib-waveguide phase shifter, thereby being suitable for high-yield low-cost fabrication.

A Si PDM IQ MZM was mounted in a ceramic-based metal package with four modulator drivers in dimensions of 35 × 15 × 4.5 mm^3, as shown in Fig. 16.18 [69]. Butt fiber coupling with 2.5-dB coupling loss, 1-dB polarization-dependent loss, and 40-dB return loss was achieved for low-profile packaging by using suspended MFCs [70]. The optical insertion loss was measured to be lower than 15 dB in the C band. The output single-ended signal of 0.5 Vpp was directly applied to the

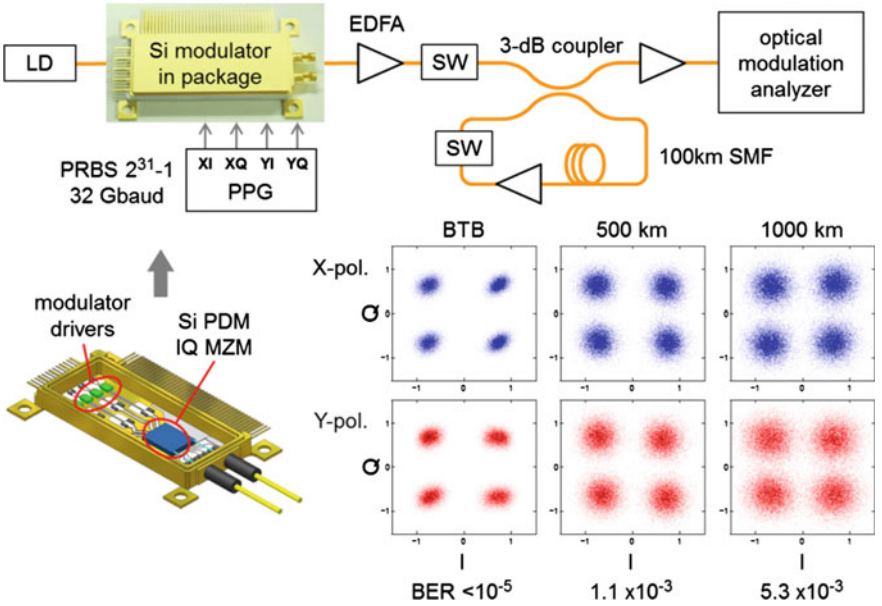

Fig. 16.18 Block diagram of the 128-Gb/s digital coherent transmission experiment based on a 100-km SMF loop link (*upper*), perspective illustration of the silicon DP-QPSK modulator module, and constellation diagrams in X and Y polarization states in transmission up to 1000-km SMF

modulator module and it was amplified to ±3.25 V in a low-power driver amplifier in the module. The LD output was 14 dBm at a wavelength of 1540 nm. A further reduction in the drive voltage will be achieved by design refinement of the rib-waveguide phase shifters for a reduction in power consumption.

Long-haul transmission measurements were performed using a 100-km SMF loop link [69]. Two optical switches (SWs) allowed synchronized burst-mode loop transmission in 50 and 100 loop turns to reach 500 and 1000-km total spans, respectively. The transmitted optical signals were detected with a coherent receiver and demodulated with an offline digital signal processor (DSP) to obtain constellation diagrams in the two orthogonal linear polarization states [19, 20].

As another example of a monolithic silicon modulator for digital coherent communication has been reported [71]; a 112-Gb/s DP-QPSK using a monolithic Si PDM IQ modulator, in which a strip-loaded Si waveguide as a PR was integrated with Si MZI IQ modulators. A silicon-nitride tapered strip was loaded on the Si core of the PR with a SiO_2 spacer layer between the Si_3N_4 strip and the Si core. An integrated small-footprint transceiver using a monolithic silicon PDM IQ modulator in a CFP package was reported [72]. Monolithic silicon optical modulators continue to progress for applications to high-capacity optical networks in various modulation formats.

16.5 Conclusion

Monolithically integrated silicon optical modulators are reviewed in the light of small-footprint high-speed optical modulators operating in various modulation formats in high-capacity optical networks. Free carriers interacting with the optical field allow the optical modulation to be insensitive to the ambient temperature, and thereby TEC-free operation is expected for the small-footprint low-cost optical modulators designed and fabricated on a silicon photonics platform. The nonresonant optical response of free carriers has the advantage of zero-chirp modulation in a push-pull drive toward high-speed optical transmission with high-spectral efficiency. Low-profile compact packaging technology has been developed concurrently with the progress of silicon modulator chips. The integrated silicon optical modulators are suitable for small-footprint optical transceivers in energy-efficient high-capacity optical networks.

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Chapter 17
Silicon Photonics Technologies: Gaps Analysis for Datacenter Interconnects

Ryohei Urata, Hong Liu, Lieven Verslegers and Chris Johnson

Abstract We give an overview of optical interconnect requirements for large scale datacenters. We then make a comparison between silicon photonics technologies and more traditional options in meeting these requirements.

17.1 Introduction

17.1.1 The New Internet

Over the past decade, web-based applications, content streaming, and cloud computing have experienced tremendous growth. One of the key enablers for this new class of applications has been the infrastructure supporting them, the large scale datacenter [1, 2]. Starting from humble, somewhat kludgy beginnings [3], Google's compute infrastructure/datacenters have been dramatically improved on all axes, from the cooling infrastructure, power infrastructure and associated efficiency (power usage effectiveness (PUE)), as well as the underlying servers, storage, and network [2]. In particular, for the network and servers/storage inside the datacenter, the trend has been to create a parallel compute architecture in both hardware and software [4]. With a largely parallel, scale-out-type datacenter network which is wide and flat (such as a fat-tree network), this network then interconnects thousands of commodity-class servers and storage devices beneath it. As shown in Figs. 17.1 and 17.2, the datacenter thus physically consists of tens and hundreds of thousands of compute nodes, with a richly interconnected, meshed network on top. In previous publications [2], this has been described as a warehouse scale computer, where the

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Topics in Applied Physics 122, DOI 10.1007/978-3-642-10503-6_17

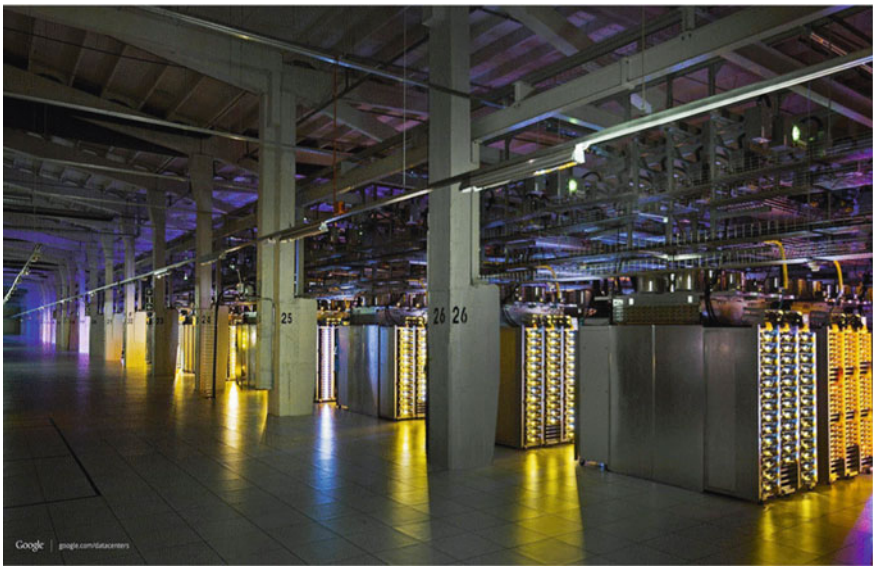

Fig. 17.1 Inside a Google datacenter, showing rows of racks, each rack housing tens of servers. Optical interconnections from the server racks can be seen above them, going to cable trays which house the fibers (http://www.google.com/about/datacenters/)

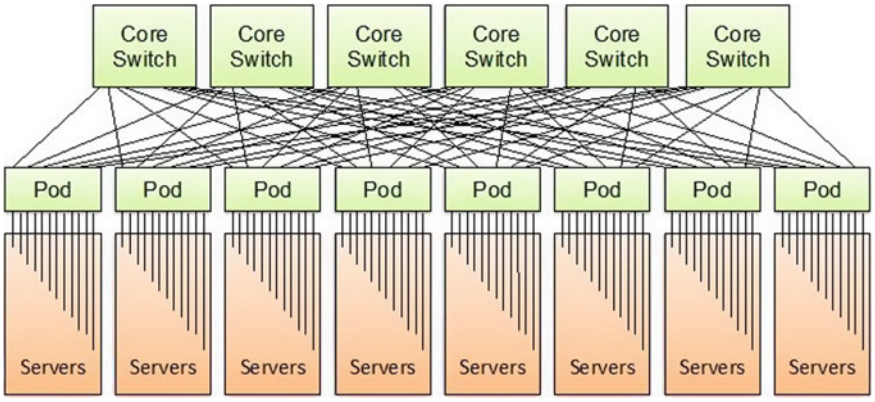

Fig. 17.2 Diagram of an example scale-out-type datacenter network. A tiered architecture is used, where fan out from lower/higher tier switches to higher/lower tier switches establishes redundant, all-to-all connections

entire datacenter building functions as a single computing entity working together in concert and running the application as one single large scale computer. In fact, taking this parallelization a step further, multiple "copies" of datacenters throughout the world are interconnected to create a global computer to deliver various services with low latency, high reliability, in a synchronized/consistent fashion.

17.1.2 Datacenter Network Architecture

A diagram of an example intra-datacenter network is shown in Fig. 17.2 [6, 7]. Machines are housed in racks (orange rectangles), which connect up to pods. The pods themselves consist of multiple switches interconnected in a tightly coupled mesh fashion to comprise a switch unit. These switches may consist of a single silicon switch application-specific-integrated-circuit (ASIC) or a meshed interconnection of ASICs. These pods then fan out to most/all switches of a second tier of switches, creating a layered/tiered network. More scale out can be derived by adding additional tiers or layers of network at the cost of more hops and delay when traversing the network. The ideal datacenter network is thus wide (to support as many end points as possible) and flat (to reduce latency and cost). The first thing that is noticeable about this intra-datacenter network is the large amount of fan out and hence, interconnect, as compared to a more traditional wide-area network (WAN), shown in Fig. 17.3. The large amount of fan out allows a wider scale out to support a large number of servers. In addition, they provide redundancy and load balancing for a robust, low latency network. Traditional WANs have low count, high value transoceanic and/or transcontinental links, thus the design direction is to maximize the capacity of these links as much as possible through higher spectral efficiency (more wavelength division multiplexing (WDM) and higher order modulation formats). This has led to the leading-edge (and usually most expensive) technologies to be first adopted at the WAN layer, specifically the end points/transceivers. Inside the datacenter, with its contrasting fan out requirement, a much larger number of transceivers and interconnect is required at lower cost, power, and density/size, at a variety of reaches, from short (tens of meters) to long (2 km or less).

Although there has been much anticipation and debate in this area, shorter, intra-rack reaches, for data rates of 1, 10, 25 Gbps, and moving forward, seem to be

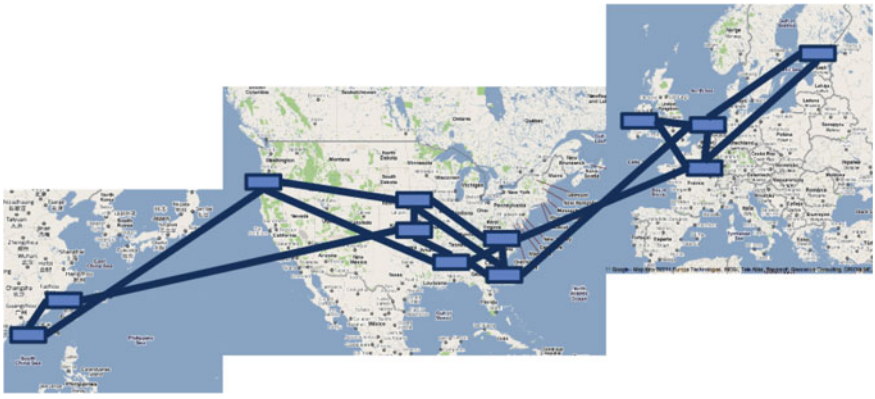

Fig. 17.3 Google's global B4 inter-datacenter wide-area-network (WAN) [5]

the domain of copper, direct attach cables, mainly driven by cost. Thus, in the following section we will cover the metrics of intra-datacenter interconnects for distances beyond intra-rack and spanning to within the datacenter (including building to building, with less than 2 km reach), where the solutions will thus be optical.

17.2 Performance Metrics for Intra-datacenter Interconnect

In addition to the aforementioned cost, power, and size characteristics, other critical metrics for the datacenter interconnects are cable efficiency, latency, serviceability, and link performance. We will review each of these items in the sections below, with comparisons between more traditional solutions versus emerging silicon photonics solutions in their ability to satisfy these requirements.

17.2.1 Cost

With the sheer number of interconnects, the overall cost of the datacenter network fabric becomes extremely sensitive to the dollar per Gbps cost of the chosen interconnect technology. When introducing new interconnect hardware then, the cost premium for this new technology, if any, must be justified by other savings at the network/switch level (dollar per port reduction with a higher bandwidth switch ASIC, as example). However, it is increasingly becoming the case that the cost of the networking fabric is dominated by the interconnect, i.e., the transceiver end points and fiber cables.

Although a variety of interconnect options exist, the traditional solutions used within the datacenter can be largely divided into vertical-cavity-surface-emitting-laser (VCSEL) with multi-mode-fiber (MMF)-based solutions, or edge-emitting-laser with single-mode-fiber (SMF)-based solutions, along with the newly emerging silicon photonics solutions. From a cost perspective, traditional SMF-based optics has been burdened by the need for a gold/ceramic box for hermetic sealing of the optoelectronic devices, in particular for applications requiring a thermoelectric cooler (i.e., dense WDM for laser wavelength accuracy) since condensate can form without hermeticity and causes reliability issues. Silicon photonic solutions have an inherent advantage here with the high-quality oxide seal provided by the CMOS process. Reliable sealing must be extended to the off-chip [8, 9] or hybrid/integrated laser [10], and novel/low-cost packaging techniques for the laser, with and without a hermetic seal, have already been demonstrated in some platforms, as shown in Fig. 17.4 [8, 11]. The need for a high power seed laser makes the reliability issue more difficult, with facet-related degradation becoming

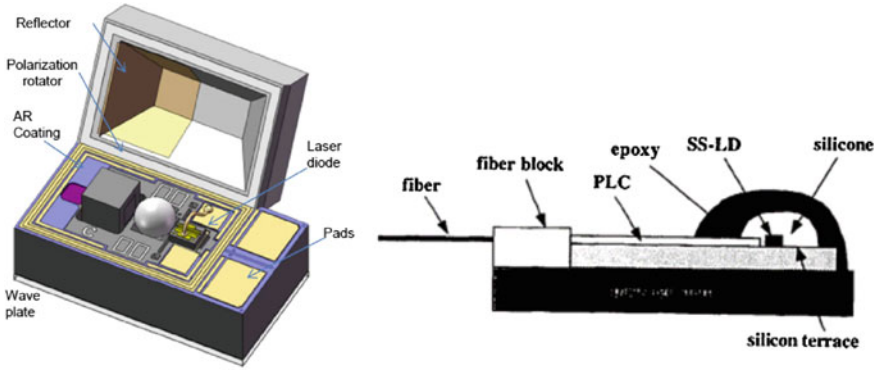

Fig. 17.4 Illustrations of low-cost packaging approaches: hermetic and non-hermetic [8, 11]

more challenging. It should be noted that a large number of these techniques to reduce cost have and will likely be extended more and more to the traditional SMF solutions employing edge-emitting lasers. VCSEL-based solutions have migrated to non-hermetic environments for quite some time now by insuring reliability at the laser/component level with the correct dielectric coatings and burn-in/screening processes [12, 13]. In addition, MMF-based solutions have gone to chip-on-board solutions where the VCSEL/photodetector (PD) chips are directly bonded to the transceiver printed circuit board (PCB), further reducing cost (Fig. 17.5). This is possible as a result of the relaxed alignment tolerances and optical components eliminated (isolator, some lenses, etc.) with a MMF-based solution.

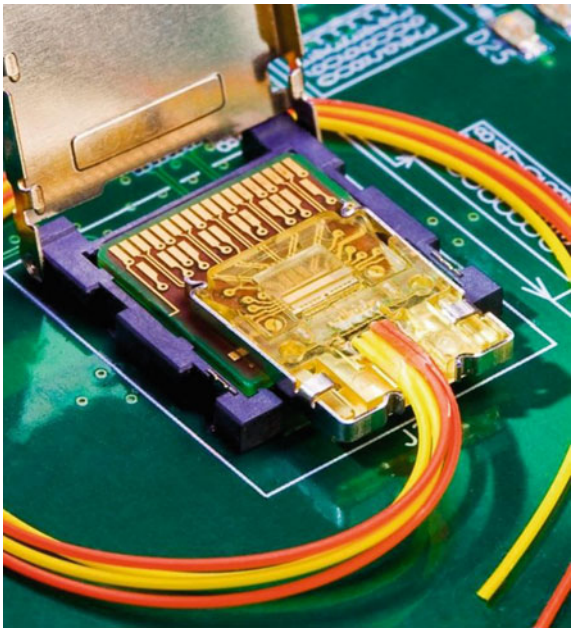

Fig. 17.5 Example of low-cost chip-on-board technology. *Source* Intel

At this point in time, in particular for lower channel count transceivers, it is thus not clear if silicon photonics has a significant advantage on cost over their traditional edge-emitting laser or VCSEL counterparts, due to the development of low-cost packaging options for traditional solutions using III–V compound materials. Higher channel count optical transceivers will require device-level integration to maintain an aggressive cost reduction roadmap, thus there may be an advantage for silicon photonics moving forward if yielded cost for multi-channel device arrays is lower than their competition. Finally, the choice of SMF versus MMF, parallel fiber versus duplex fiber technology will incur costs on the cabling, which will be covered later on, in Sect. 17.2.3.

17.2.2 Power, Density, Size

Figure 17.6 shows an example of the distribution of power consumption within a datacenter. As can be seen, the networking portion comprises only 5 % of the entire power envelope of the datacenter, of which optics is a smaller subset of that power (half or less). Thus, reduction of the networking power consumption is not effective in dramatically improving datacenter power efficiency and lowering the corresponding Cap Ex and Op Ex spend. However, reduction of the power is still important for density and overall network fabric cost.

Figure 17.7 shows a 128 port network/Ethernet switch developed at Google [5]. The switch is comprised of multiple line cards plugged into the chassis. The front panel is covered with ports/cages housing the pluggable optical transceivers. In this mode of switch design with pluggable optics covering the entire front panel, the size constraint on optics comes from the face plate width/dimensions of the line card where the aggregate bandwidth of the switch ASIC(s) sitting on the line card must be extracted within these dimensions. Figure 17.8 shows various pluggable optical transceiver standard form factors for 100 GbE and the associated power consumption of each. Obviously, with the smaller form factor solutions, more bandwidth can be brought out per linear dimension of the line card (Gbps/mm). In practice, the power consumption of the various components inside the transceiver usually limits which form factor can be used, and the actual size of the transceiver components do not.

Delving into what determines power at the component level can be quite complex as the type of device in addition to the details of the design lead to a wide range of power numbers. From a packaging perspective, a traditional approach has the electrical ICs and optoelectronic devices interconnected with wire bonds (Fig. 17.9), which adds large parasitics from both bond pads and wires, and requires additional drive and/or equalization capability within the electronics leading to additional power consumption. Silicon photonics has an inherent advantage in that it can leverage the die stacking and 3D integration technologies being developed for mainstream silicon technologies, or the ability to go monolithic: a single chip with both electronics and photonics [14]. With the reduced parasitics, the power

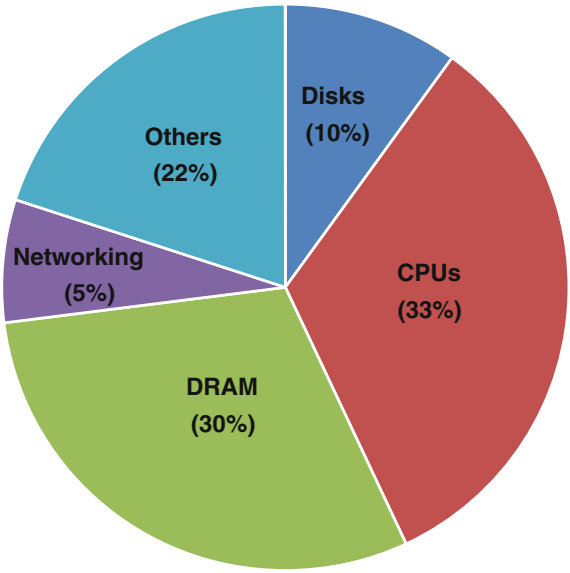

Fig. 17.6 Power consumption pie chart for a datacenter [2]. Networking (including optics) comprises only a small fraction of the entire power envelope

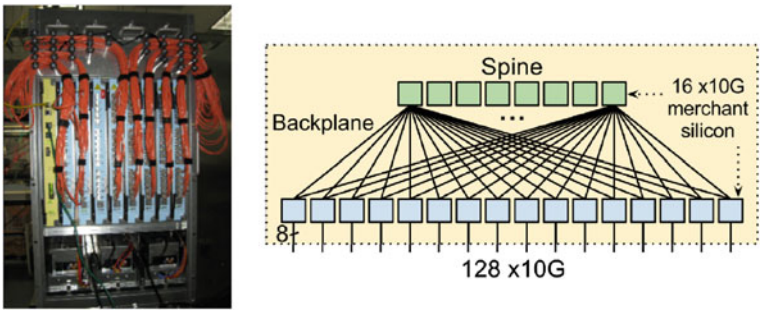

Fig. 17.7 Networking switch with multiple line cards [5]. Merchant silicon switch ASICs are used to form a 2-stage Clos topology, creating a 128 port Ethernet switch

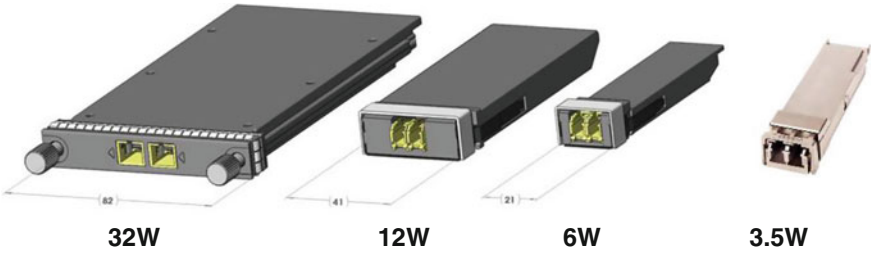

Fig. 17.8 Various form factors for 100 GbE pluggable transceivers and corresponding power envelope (www.cfp-msa.org). From *left* to *right* CFP, CFP2, CFP4, QSFP28

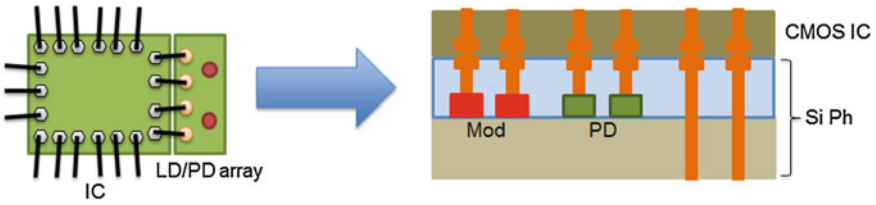

Fig. 17.9 Moving from discrete to an integrated solution will potentially enable silicon photonics to achieve a lower power solution

consumption of the driver and receiver circuits may be reduced significantly, leveraging a lumped load versus a more traditional wire bonded and/or 50 Ω terminated environment. This type of intimate integration is possible but made difficult for III–V discrete devices due to the differences in thermal expansion coefficient of the materials (III–V vs. silicon electronics) and more so by the high temperature sensitivity of lasers that would need to be placed close to the heat sources (lasers directly modulated by the IC). With silicon photonics, the laser could naturally be placed further away from the heat producing ICs.

Despite these advantages of an integrated approach, VCSEL MMF-based transceivers are at present, inherently lower power, owing to the VCSEL's low threshold current and high efficiency. As bit rates increase and higher order modulation formats become main stream moving forward [15], a large amount of signal conditioning/equalization may be needed at both the transmitter and receiver, to compensate for insufficient bandwidth of the VCSEL, in addition to more aggressive and power hungry forward error correction (FEC) needed to close the link. Silicon photonics external modulator-based solutions have demonstrated high bandwidths and good linearity to scale to the next generation of line rates [16], and this will be discussed in more detail in Sect. 17.2.6.

17.2.3 Cable Efficiency

As discussed above and shown in Fig. 17.1, network endpoints that are interconnected with fiber are done so with fiber cables going up from the racks housing the endpoints, up to cable trays above the racks. With the sheer number and aggregate volume of this cabling, datacenter deployments cannot be practically implemented with large cable volumes, making its volume efficiency an important metric. Table 17.1 compares the relative cost and volume of single-mode duplex/fiber pair (WDM), single-mode parallel (SDM), and multi-mode parallel cabling. Costs exclude termination costs (i.e., connectorizing the two ends of the fiber cable), which are significantly higher for parallel fibers. From Table 17.1, it is clear that single-mode duplex is superior in all aspects. Single-mode parallel does not scale well in cable volume and termination costs are increased, in addition to insertion

Table 17.1 Comparison of single-mode duplex (WDM), single-mode parallel (space division multiplexing (SDM)), and multi-mode parallel cable costs and physical volume for various interconnect solutions

	SMF-WDM		SMF-SDM		MMF cable	
	Cost	Volume	Cost	Volume	Cost	Volume
10G	1×	1×	1×	1×	2×	1×
40G (4 × 10 Gb/s)	1×	1×	3×	2.25×	6×	2.25×
100G (4 × 25 Gb/s)	1×	1×	3×	2.25×	12×	2.25×
400G (16 × 25 Gb/s)	1×	1×	10×	4×	30×	4×

loss increase due to the array nature of the connectors and transceiver components (i.e., alignment to a linear array is harder than a single element). Multi-mode parallel does not scale well in either cable volume or cost. The latter is owing to difficulty in dealing with inherent modal dispersion, which necessitates newer fibers with increased fiber bandwidth. It should be noted that this further burdens the cost of MMF-based solutions as fiber may need to be replaced for every new, higher speed data rate interconnect to maintain a given interconnect reach (for example: OM3 to OM4 for 100 GbE at 100 m reach), whereas SMF with WDM-based solutions may leverage parallelism in wavelength and be reused over multiple generations by simply adding additional wavelengths when more bandwidth is needed. Again, termination costs are higher for parallel cables, worse for SMF parallel than MMF parallel cables.

With respect to silicon photonics in general, there is no particular technological fit for a particular fiber cable type. In general, the devices themselves are for the most part, inherently single mode, but can be used for either with the right peripheral design. However, particular components such as bandwidth-limited grating couplers [17] and polarization-dependent WDM demuxes/muxes [18] which have been developed for silicon photonics do not lend themselves well to WDM and will need to migrate to more WDM/single-mode duplex compatible approaches.

As for additional ways of achieving single-mode duplex, there has been recent increased interest in multilevel, discrete multitone (DMT), and various other advanced modulation formats [15]. Silicon photonics does have promise in terms of achieving the higher bandwidth and linearity required to implement many of these approaches. In addition, silicon photonics may facilitate integration for WDM, with hybrid laser arrays [10], simple high yield gain blocks with gratings on silicon to form laser arrays, and high yielding high-bandwidth modulator arrays.

17.2.4 Latency

When executing specific applications or jobs within a warehouse scale computer, the communication packet in some/many cases may traverse the network from

server to server multiple times, going through a large number of network hops across switches and switch silicon. Low latency communication from endpoint to endpoint is thus needed to deliver low latency, high performance services.

The inherent latency from propagation across the fiber is 0.5 μs for a 100 m length of single-mode fiber (1 m in length ≡ 5 ns of latency). Recent IEEE and MSA standards for 100 GbE [19] have adopted forward error correction (FEC), which adds roughly tens to one hundred nanoseconds of latency. This is still a small portion of the total latency when dealing with link lengths of one hundred to several hundred meters. However, with higher order modulation and higher channel speeds straining performance and link margin, stronger (and correspondingly higher latency) FEC has been suggested for future implementations. As an extreme example, typical latencies for soft-decision-based FEC [20] for long haul optical links can be several microseconds long, and would likely be noticeable for latency sensitive applications (as well as significantly more power consumed). In particular, FEC has been adopted already for some initial silicon photonics solutions coming onto the market, to compensate for low link budget margins. This gap in performance will be discussed in more detail in the last section.

17.2.5 Serviceability: Pluggable Versus Embedded Transceivers

On the left of Fig. 17.10, an example of a "traditional" network line card is shown, with switch silicon ASIC on the board, a clock-and-data-recovery (CDR) circuit for regeneration potentially needed depending on the capabilities of the ASIC I/O circuits and electrical connector performance, and the pluggable transceivers (such as those shown in Fig. 17.8) populating the front panel edge of the line card. This has been the preferred approach for datacenter network switches, as having pluggable optics allows easy replacement and servicing of defective optics in either manufacturing test or deployment in the field, and is thus the preferred approach from a manufacturability and serviceability standpoint. The other major benefit is that one flavor of line card can accommodate multiple interconnect length solutions (copper, multimode or single mode can use the same line card). This design approach can be sustained as a result of two points. First, the ability of the host ASIC to deliver its output bandwidth and drive/receive signal on the copper trace/interconnect to/from the front panel (and beyond) within a given power/thermal constraint has not been an issue to this point in technology. In addition, the density of the optical solution has been sufficient to extract all of the ASIC bandwidth within the given linear dimension. Figure 17.11 illustrates this point, with the front panel bandwidth and ASIC bandwidth tracking each other [21]. It also predicts that the former may be the first to constrain this model of pluggable optics at the front panel, due to the power density limitation of the optical transceiver.

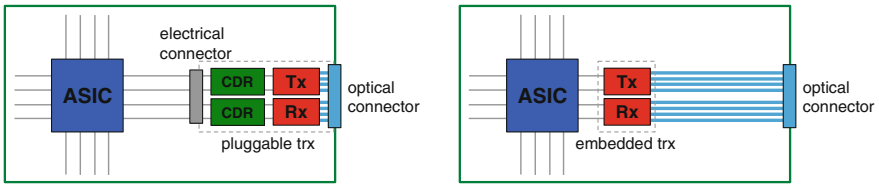

Fig. 17.10 *Left* Line card design with pluggable optical transceivers with CDRs at the edge of the line card (*front panel*), enabling easy optical module access and serviceability. *Right* Line card design with on-board optical transceivers, placed close to the switch ASIC, eliminating the need for CDRs and reducing power consumption but not allowing serviceability at per-module granularity

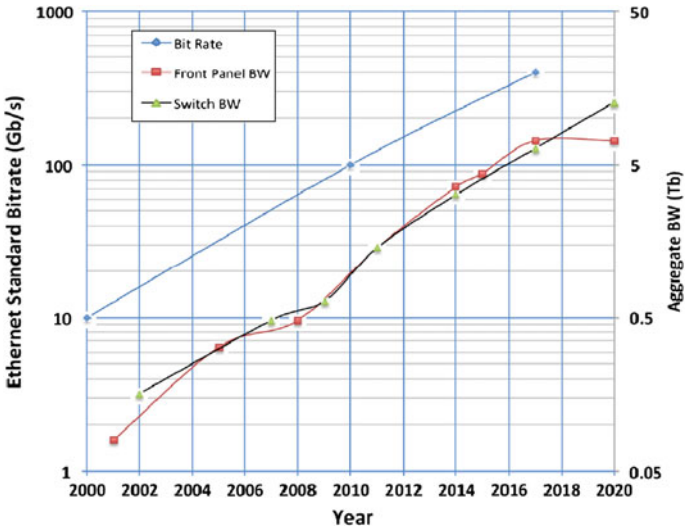

Fig. 17.11 Past and future trend in (1) channel bit rate, (2) front panel bandwidth, and (3) switch ASIC bandwidth [21]

One approach to overcome this limitation is the use of embedded optics, which places the optical transceiver close to the ASIC, either with a socketed or soldered transceiver (right, Fig. 17.10). An optical connection is then made from the module to the front panel with an optical jumper, where a dense optical connector technology can then be leveraged. In addition to overcoming the front panel density limit, additional benefits include the ability to remove the CDR and alleviate the requirement on the ASIC I/O to save power. However, as stated above, the embedded modules make manufacturing difficult, as the line card yield is dictated by a large number of modules, not just the ASIC and peripheral electrical components on the board. In addition, when one module stops functioning, the corresponding bandwidth loss of the network cannot be recovered until the entire line card is swapped. Thus, in order to obtain similar values of sustained network

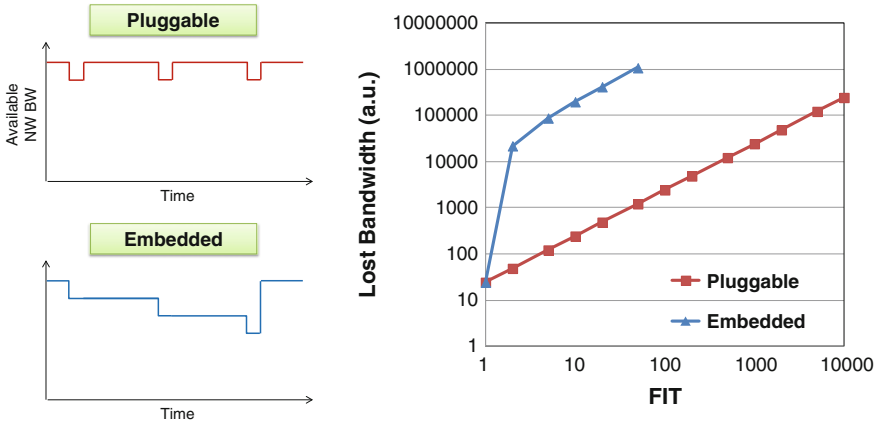

Fig. 17.12 *Left* Aggregate bandwidth change in a datacenter network with pluggable versus embedded optical transceivers. *Right* Lost bandwidth due to defective/failed transceivers versus the corresponding required FIT value needed, for both pluggable versus embedded optical transceivers

bandwidth, the reliability of the embedded module must be much higher than the pluggable one. This reliability requirement is further challenged by the placement of the module closer to the ASIC, which serves as a huge source of heat, causing the module to likely operate at a much higher temperature than the pluggable modules at the edge of the line card.

Figure 17.12 illustrates and shows the results of a simple, comparative study done between the pluggable versus the embedded approach with respect to reliability requirements [22]. Assumptions are an example datacenter network fabric with several thousand transceiver ports, with these ports split across a large number of line cards. The figure on the left shows the aggregate bandwidth of this network as a function of time, and the dips in the figure represent a module/port failure. In the case of the line card with pluggable modules, the transceiver can be immediately replaced and the bandwidth recovers within a given service time (assume 24 h). In case of the embedded module, one would likely wait until some percentage of intolerable bandwidth loss occurs on the line card, after which the entire line card would need to be replaced. In order to sustain the same level of aggregate network bandwidth on average over time, the failure-in-time (FIT) rate of the transceivers needs to be different for the pluggable versus embedded module. On the right figure, the FIT needed for a given amount of bandwidth loss is shown. Although the assumptions are simplified, it can be seen that the FIT of the embedded module would need to be several orders of magnitude better than its pluggable counterpart.

Clearly, the above analysis is independent of the transceiver technology implemented, but it points to the need for a roadmap towards sufficiently low FIT rates if the front panel bandwidth truly becomes an issue. Considering that the highest FIT component is usually the laser source, and that the silicon photonics

approaches use III–V based lasers or gain blocks, in general, it seems there is no clear advantage with the currently available silicon photonics based approaches. The approaches that utilize a hybrid/integrated laser [10] may have additional concerns with reliability due to the mismatch in material properties (thermal expansion coefficient) of the III–V gain block with the silicon substrate which affects the laser from within the laser cavity. Initial reliability studies thus far have shown promising results [23].

If/when the embedded solution becomes insufficient for bandwidth density, silicon photonics does have advantages in taking density to the extreme, as it can be monolithically integrated with the CMOS electronics [14]. However, this approach is several steps removed from commercial implementation, with a number of technical factors (power efficiency, yield, thermal stress, integration with leading-edge CMOS) as well as economic factors still to be overcome.

17.2.6 Performance

Although there are many details and subtleties involved in the design of datacenter links, from a performance aspect, the most important parameters are link budget (how much optical loss or equivalent loss due to signal impairments can be tolerated before the link cannot close to some bit-error-rate (BER)/link quality specification) and link distance. A high link budget is important for robust performance of the link, which facilitates large rollouts of the technology without issues. In addition, it also enables flexibility in network design and architecture, from both a physical and logical standpoint. As an example of the former, the datacenter architecture of Fig. 17.2 may span multiple geographic locations, across multiple buildings, which requires structured cabling and links passing through a number of patch panels/connectors with a corresponding increase in link loss. Link distance is obviously important for scale, and the datacenter networks being deployed in general are getting physically larger, not smaller.

For link budget, the lasers traditionally used for SMF-based links (distributed feedback lasers (DFBs) or Fabry-Perot lasers) are in general, superior to that of VCSELs, due to the smaller active volume of the VCSEL constraining output optical power. For silicon photonics, achieving high link budgets can also be a challenge due to the inherent need to couple light into and out of the silicon chip resulting in significant additional losses or to achieve a high gain/mode overlap integral with the hybrid/integrated laser approach, which affects laser output power. In addition, the waveguides for some silicon photonics platforms can be quite small. Mode matching this waveguide mode to the fiber or laser mode can be difficult without mode shaping elements (creates additional loss). If an external modulator is used, that can add additional loss, whereas a direct laser modulation approach eliminates the modulator at the expense of having a laser bandwidth/bias current tradeoff. Many silicon photonic modulators also exhibit higher loss than their III–V counterparts, in part due to a weak electro-optic effect.

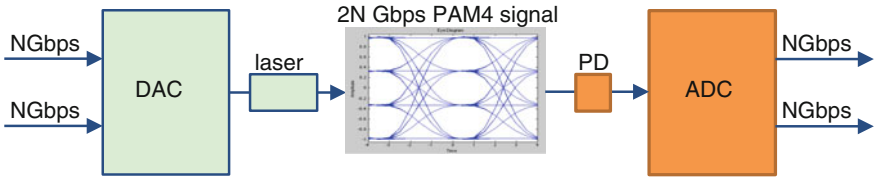

Fig. 17.13 Pulse-amplitude-modulation-based link (specifically PAM4, four level). Leveraging of technology development for the line side (long haul), in the form of high-speed ADC and DAC design, allows increase of bandwidth with the same baud rate and number of optical components

Although optical amplification could in theory be used within a datacenter link, the need for an additional element, as well as the cost increase, makes it somewhat impractical. An integrated amplifier, such as a semiconductor optical amplifier (SOA) or avalanche photodetector (APD) [24, 25] may be more realistic, but difficulties remain with the complexity in implementing and/or reliability of these elements within a silicon photonics solution.

Conversely, silicon photonics does have potentially high yielding, high bandwidth external modulators [16] and waveguide-based photodetectors, which could perhaps enhance the link budget overall if the additional bandwidth is more valuable than the power lost in going through the modulator. Mach–Zehnder structures are often adopted for the modulator, which would allow comparable linearity performance with coherent transceiver technologies. These advantages will likely become more critical as baud rates continue to increase and the modulation formats that are adopted become more complex, as shown in the pulse-amplitude-modulation (PAM)-based link of Fig. 17.13 and described in [15].

For the link distance metric, SMF-based silicon photonics has advantages over VCSEL/MMF-based links, due to the lack of modal dispersion. There is no advantage over traditional edge-emitting-laser-based SMF links, although the amount of fiber dispersion penalty can vary slightly based on the laser technology chosen (direct modulation vs. external modulation).

17.3 Conclusion

With key advantages of integration capability and high yielding high-bandwidth components, it is clear that silicon photonic technologies hold great potential for meeting the ever growing demands of datacenter interconnects. As evidence of this, the first deployments and use of silicon photonics based interconnect technology within the datacenter are likely to happen over the next few years. However, it is also clear that silicon photonics must contend with more traditional interconnect technologies and approaches that continue to evolve from both a device and packaging perspective.

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Chapter 18
VLSI Photonics for High-Performance Data Centers

Di Liang, Marco Fiorentino and Raymond G. Beausoleil

Abstract After over four decades of technology development and commercial application, photonics proves to be the best information carrier for long-haul communications. A huge effort has been taking and is still increasing to miniaturize such a photonic communication system to serve the same purpose when conventional metal interconnect in CMOS comes to its physics and practical limit. Along the road to *siliconize* photonics up to a much larger scale in order to design, fabricate, and test photonic links based on advanced CMOS technology, new architectures and device geometries are created and explored. In this chapter, we reviewed the development in architecture design, CMOS transceivers, and hybrid III–V-on-Si transceivers, particularly progress in HP, to unfold a technology roadmap of VLSI photonics application for data center from an industrial perspective.

For decades, both Moore's Law and Dennard scaling enabled exponentially higher computing and data communication performance for a given cost at lower power per function [1]. Nevertheless, demand for traditional high-performance computing installations and large-scale "cloud" computing services—relying heavily on massive data centers—have grown even more rapidly. In addition, voltage scaling, a key requirement for Dennard scaling, has plateaued, and power dissipation is becoming an ever larger problem for high-performance systems. Recent studies and initiatives from the US DOE have set an aspirational goal of 20 MW for an exascale system capable of 10^{18} computational operations per second. This is 25 times more energy efficient than the current most energy-efficient high-performance computing systems as listed in the Green 500 [2]. To even approach this ambitious goal, many significant advances will be required across the entire computer system, including

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processors, memory, storage, interconnects, and system software. For interconnects, the power required to communicate a bit across many distance scales (rooms, racks, boards, and chips) must be lowered dramatically as requirements for bandwidths per link increase. Photonics will play a key role in meeting power goals at all levels of granularity in future high-performance computing (HPC) and data centers.

In response to bandwidth, power, and signal integrity issues on long-haul networks, the telecommunications industry developed high-capacity fiber-optic technology and wavelength division multiplexing (WDM) based on narrow-linewidth lasers operating near 1550 nm [3]. As similar constraints have overtaken large-scale computer performance, active optical cables using vertical-cavity surface-emitting lasers (VCSELs) have been appearing in data centers and supercomputers. But as interconnect bandwidth requirements scale to 10 Terabits/s (Tb/s) per socket and beyond, higher levels of integration will be required to increase bandwidth per optical connector at significantly reduced cost. Over the last decade, remarkable progress has been made in research on low-power silicon photonic devices for interconnect applications, and complementary metal-oxide semiconductor (CMOS) fabrication technologies promise a "Moore's Law for photonics" [4].

Unlike the highly parallel nature of the processing done by a supercomputer, data center traffic is highly random and will require interconnect bandwidths at least as high as that of a supercomputing system. Historically, data center networks have been sized to support the relatively low bandwidth available from disk-based storage. The radically higher bandwidth available from new solid stage storage technologies will require a proportionate increase in network bandwidth, and the ability to continue to scale with future improvements in memory bandwidth. Current commercially available silicon photonics technology supports 1–4 wavelength channel(s) in each on-die waveguide and in each optical fiber core, and will require new optical "plumbing" in next-generation servers (e.g., single-mode fiber) to provide reliable operation at low cost and low power. Once this approach has been adopted for a new product line, the number of optomechanical connectors and the number of optical fibers are fixed so that operators can amortize their total cost of ownership over 10-year timescales. Therefore, the most promising way to improve performance across the entire installation is to provide higher bandwidths through the installed infrastructure. Using CMOS DWDM photonics co-packaged with processors, switches, and future systems-on-chip (SOCs), we can increase the bandwidth to all nodes and endpoints in the datacenter without *any* changes to the racks or boards—and without requiring more fiber connections to chips.

18.1 Photonic-Interconnected Data Center Architectures

HPC systems and datacenters have quite similar architectures: a large number of many-core processing nodes are connected by scalable interconnect networks. Recent trends in datacenter consolidation—as well as the growth of cloud-based computation and storage—have resulted in datacenters with node counts that

exceed that of most supercomputer systems [5]. But HPC systems are usually dedicated to a single application at a time, while data centers typically run a large number of concurrent applications. As a result, a key difference between HPC systems and commercial datacenters is the utilization of the interconnect networks: as data centers make less use of fine-grain distributed processing, they can require less network bandwidth to support a given amount of processing power. Additionally, as datacenter applications are usually limited to a small fraction of the total available resources of the installation, it is not necessary to maintain full bisection bandwidth (the ability for any arbitrary set of pairs of nodes to concurrently communicate) across the entire network. Message latency across the network has been of greater importance for HPC systems, where many processing nodes work together on single task, compared to data centers, where job throughput is of greater concern. However, emerging requirements of data center virtualization will require lower latencies and higher aggregate network bandwidth [6], creating an opportunity for the convergence of data center and HPC networking technology.

By 2020, deployment of exascale systems with as many as 100,000–1,000,000 nodes is expected to be underway. By that time, single-chip processors with sustained performance exceeding 10 Teraflops will be available, exploiting both high levels of thread parallelism and SIMD parallelism (similar to today's GPUs) within the floating-point units. With memory bandwidths as high as 4 Terabytes/s (TB/s), one of the most critical aspects of the node design shown in Fig. 18.1 will be providing sufficient memory bandwidth to sustain the processor within an acceptable power budget (e.g., 200 W). This will be achieved be either stacking "near" memory directly on the processor, or locating it within the processor package itself.

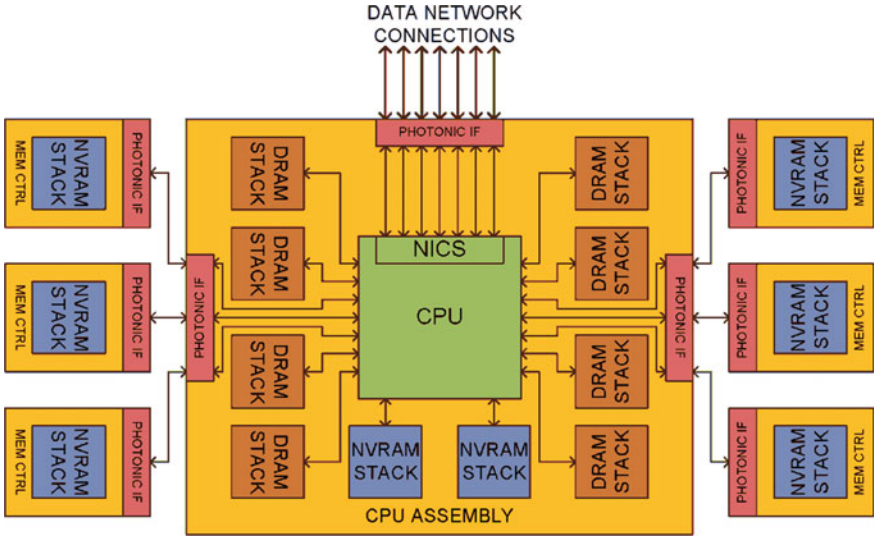

Fig. 18.1 Exascale compute node [7]

As the amount of memory that can be connected in this way is limited, additional "far" memory (provided by nonvolatile RAM) will be provided by memory modules connected to the processor through high-speed links. Distributed memory programming techniques, such as MPI message passing, are used across a network spanning 100,000 nodes with required bandwidths of at least 1 Terabyte/s per connection [7].

The networks can exploit high-radix routers connected in a HyperX topology [8] to yield a low-diameter network. As explained below, a key challenge for exascale systems will be to scale the performance of the global system interconnect to meet processor and memory requirements, while satisfying both bandwidth density requirements and power constraints. Integrated CMOS photonics based on silicon microring resonators addresses these issues by enabling compact dense wavelength division multiplexing (DWDM) transmitters and receivers to be built in standard silicon manufacturing technology [4, 7]. This technology should allow transport energies across the network approaching 200 fJ/bit, compared to the 10–20 pJ/bit of today's best optical links. An additional advantage of these links is that they have bandwidth densities as high as 640 Gbps per single-mode fiber core, assuming 64 wavelengths at 10 Gbps each. The network routers will be interconnected optically, but are likely to continue to use CMOS electronics internally for packet processing and buffering. The bandwidth density required at the periphery of these devices is so large that it is highly unlikely to be achievable using discretely packaged transceivers mounted on either the board or the chip package. Micro-solder bumps, face-to-face copper bonds, and through-silicon vias allow much finer pitches between devices, enabling arrays of closely packed transceivers to be bonded directly to the CMOS switch device. This approach significantly increases the effective edge bandwidth of the chip and supports the design of higher port count switches without reducing the port bandwidth.

Embedded high-radix routers with high port count switches and higher bandwidth per port enable direct network architectures with very low hop counts, reducing power, cost, and latency. The availability of VLSI DWDM optical interconnect technologies creates many opportunities for completely new interconnect topologies that are impractical using electronic interconnects alone. For example, optics decreases the importance of optimizing connection length in topology selection and allows simpler installation cabling, while by contrast electronics favors topologies such as meshes with larger numbers of relatively short links.

"HyperX" is a scalable network architecture (adapted from hypercube and flattened butterfly topologies) that relies on the high-radix switch implementations that large-scale integrated photonics could enable [8]. HyperX uses an adaptive routing algorithm that enables a desirable balance between performance, power, cabling complexity, and fault tolerance. This architecture can provide performance equivalent to that of folded-Clos networks, with fewer switches, and uses photonic components to enable a low-cost packaging strategy for exascale data centers. A HyperX is a direct network of switches in which each switch is connected to some fixed number T of terminals, such as compute nodes, I/O nodes, or memory or storage devices. Each switch is a point in an L-dimensional lattice. Figure 18.2

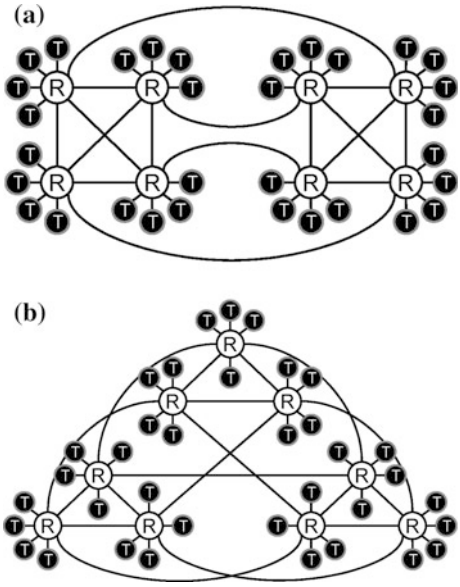

Fig. 18.2 Two examples of the HyperX topology. *Dark circles* labeled "T" are terminals, and *light circles* labeled "R" are switches [8]. **a** $L = 2$, $S_1 = 2$, $S_2 = 4$, $T = 4$, **b** $L = 2$, $S_1 = 3$, $S_2 = 3$, $T = 4$

shows two examples of a HyperX topology, each with $L = 2$ dimensions and $T = 4$ terminals connected to each switch. In Fig. 18.2a, there are $S_1 = 2$ in the first dimension, and $S_2 = 4$ in the second, supporting a total of 32 terminals. In the HyperX shown in Fig. 18.2b, each dimension comprises three switches and connects a total of 36 terminals.

Integrated CMOS nanophotonics is of greatest potential benefit where the system performance is currently constrained by the bandwidth on and off chip. Two examples of this are processor memory interfaces and switch ASICs. The distance independence of single-mode photonic interconnects is particularly attractive in this latter application. For this reason we believe that high-radix switches will be the first application of large-scale integrated CMOS photonics. Electronic switches are today designed around the power and packaging constraints of their IOs, and designers must trade the number of ports against port bandwidth. DWDM photonic interconnects will enable switch components with several hundred ports, each with hundreds of Gbps of bandwidth. Further flexibility can be achieved using passive optical multiplexors to partition the DWDM connections, allowing a single component to support either hundreds of very high-bandwidth ports, or thousands of ports at lower bandwidth.

The key component in building highly scalable networks for data centers is a high-radix photonic packet switch ASIC (PhASIC). The design of electronic router ASICs is constrained by the total chip IO bandwidth, which depends on the maximum number of pins, the data rate per pin, the total device power, and the distance between the switch and other switches and terminals. The available number of package pins has reached its practical limit and will not increase in the future, and the pin data rate is improving only relatively slowly while the reach

(a few centimeters to a meter) has not changed at all. Furthermore, the power consumed by high-speed I/Os is becoming the most significant contribution to the total router power, with more than 50 % of power being expended by the I/O components. Increasing the port count, or radix, of routers can have significant advantages in terms of reducing component count, network diameter, and system power.

Consider the three possible packet switch layouts shown in Fig. 18.3: (a) an all-electronic design; (b) an electronic switch with photonic I/O; and (c) a photonic switch core with photonic I/O [7]. In the case of the design incorporating the photonic switch core, the packets are received optically and then converted into electronic data for buffering and routing, while the core crossbar is photonic. An additional stage of electronic buffering is implemented at the outputs, before the data are converted back into the optical domain for transmission.

The results of a comparison of I/O power dissipated by each design are shown in Table 18.1 [9]. Here we have assumed that the port bandwidth will double at each new process generation to accommodate corresponding increases in processor performance. In a forced air cooling environment with a heat sink, the total power is limited in practice to around 130 W. Liquid cooling would allow a total chip power consumption as high as 200 W, but this would likely be used only in high-end supercomputers. If we assume that 50 % of the air-cooled power budget (65 W) is available for I/O, then it is clear that power considerations alone will require photonics to increase link speeds with processor performance. The I/O power reduction allowed by VLSI DWDM photonic technology is dramatic: more than 20X reduction in power could be obtained at the 22-nm processing node.

A corresponding study shows that a further 2X reduction in total package power can be achieved by incorporating a photonic crossbar within the switch core [9]. These crossbars can take several forms, depending on the application. For example, one of the first photonic crossbars, “Corona” [10], was proposed in 2008 as an architecture for a processor with 256 cores divided into 64 groups, targeted for the 22-nm CMOS technology node. The corresponding device structure had multiple stacked physical layers—each fabricated on a separate special-purpose die—for the cores (each with an integrated L1 cache), the L2 caches (shared by each group), and the global photonic interconnect. The silicon photonic layer was proposed as an all-to-all DWDM crossbar with fiber-optic I/O to DRAM, allowing high-bandwidth and low-latency communication to all memory in the system at an energy cost of approximately 290 femtojoules per bit. The design is enabled by some of the active photonic devices discussed below, such as silicon microring modulators or hybrid microring lasers, each operating at 10 Gb/s, and integrated silicon–germanium photodetectors. High-bandwidth arbitration was provided by an integrated photonic system based on the same components used in the interconnect, with a speed that is limited only by the time required for a light signal to propagate through a silicon waveguide once around the chip [10, 11]. This design reduces the latency of the entire system to only 8 clock cycles.

The extremely high degree of parallelism, 10 Terabyte/s network bandwidth, and high cache coherence provided by Corona is enabled by over provisioning the

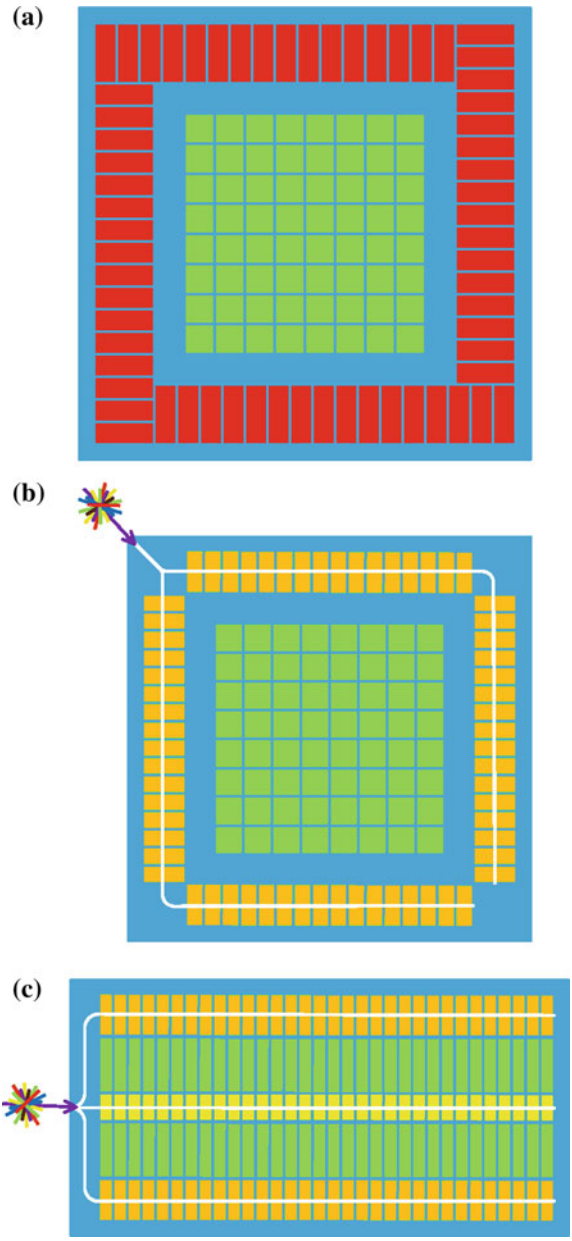

Fig. 18.3 Three possible switch architectures of **a** all-electronic switch, **b** optical I/O and electronic core and **c** optical I/O and core [7]

active photonic devices by a factor of 64 above those in use at any given time (accounting for half of the energy consumed by the photonic layer [12]), placing stringent requirements on the quality of the fabrication and integration technologies used to build the chip. In 2014, a much more energy-efficient architecture,

Table 18.1 Router I/O power scaling for switches with 64, 100, and 144 ports

Generation (nm)	Port BW (Gb/s)	I/O type	Energy (fJ/b)	64 (W)	100 (W)	144 (W)
45	80	Electronic	7000	35.8	56.0	80.6
		Optical	451	2.3	3.6	5.2
35	160	Electronic	5048	51.7	80.8	116.3
		Optical	284	2.9	4.5	6.5
22	320	Electronic	4049	82.9	129.6	186.6
		Optical	191	3.9	6.1	8.8

"LumiNOC," [13] was proposed for nanophotonic network-on-chip. This architecture partitions the crossbar into subnets to improve performance per unit power, and uses a purely photonic distributed arbitration scheme. In addition, a channel-sharing scheme allows the same waveguides and wavelengths employed for data transmission to be reused for arbitration. In a 64-node crossbar under synthetic traffic, simulations of LumiNOC predicted that it could deliver 50 % lower latency at low loads 40 % higher throughput per unit power than Corona and other published photonic networks.

VLSI DWDM photonic architecture with such complexity and scale, which will be controlled by CMOS drivers, requires enormously integrated photonic circuits. Si photonics emerges to be the best candidate to provide huge advantages in design, fabrication process control, and on-chip testing: a path paved by CMOS industry development in the past half century.

18.2 Si Microring-Based Transceivers

Si microring-based transceivers provide the means to transmit digital information over optical channels. A transceiver comprises a transmitter and a receiver. In Si photonics transmitters, typically, a continuous-wave (cw) laser is modulated by an external Si photonics modulator. This choice is typically due to the fact that it is not easy to build a laser on Si that can be modulated at high speed. The next section will focus on a very successful way to implement a hybrid Si photonics laser; in this section we will focus on transceivers based on externally modulated lasers.

Modulation in Si devices can be achieved by exploiting the plasma dispersion effect, whereas changing the carrier concentration changes the real and imaginary parts of the index of refraction [14]. In a recent review article Reed and co-workers [15] have individuated three possible configurations for electrically driven silicon modulators. These configurations are schematically shown in Fig. 18.4. In a carrier injection modulator, carriers are injected by forward biasing a p-i-n junction. This type of modulator is limited in speed by the recombination rate of the carriers and has relatively high power consumption. On the positive side, carrier injection

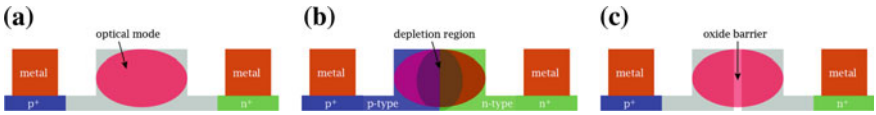

Fig. 18.4 Optical modulation schemes: **a** injection, **b** depletion, and **c** accumulation [15]

allows large changes in the carrier density and therefore a high modulation depth. A second method of modulation is carrier depletion. In this case the modulation in the carrier density is obtained by depleting a p–n junction. Carrier depletion is fast and consumes low power as little current flows in the junction during operation. Because of the need to overlap the p–n junction and the optical field, this method, in general, creates modulators that have large insertion losses and low modulation depth. A third modulation scheme is the charge accumulation. Here a MOS capacitor is used to accumulate charges in the optical waveguide. Like charge depletion this method leads to fast and low-power modulation. Because of the need to create an oxide barrier in the middle of the modulator waveguide, however, charge accumulation modulators are hard to fabricate.

Two main Si modulator topologies have been used. Mach–Zehnder interefer-ometers (MZIs) are the simplest and most robust type of modulators and for these reasons have been adopted in many Si photonic products. An MZI modulator is relatively immune to thermal drifts and fabrication imperfections. MZIs are also relatively large (with typical areas of 1000 s of μm^2), have high power consumption, and require a complex RF electrode design to achieve high speeds. Green et al. [16] reported a 10 Gbps injection-based MZI modulator with a total area of $\sim 100 \times 200\ \mu m^2$ and a power consumption of 5 pJ/bit.

Resonant microring modulators were first introduced as modulators by Xu and co-workers [17] and have several advantages over MZIs. Because they are resonant devices, microrings lend themselves to be used in wavelength multiplexing schemes; in addition, they are much smaller than MZIs (with typical areas of 10 s of μm^2) and consume much less power. On the negative side microrings are extremely sensitive to thermal shifts and fabrication imperfections. Xu et al. used charge injection for modulation where depletion disks [18] and depletion ring modulators [19] have been demonstrated as well. Charge injection has the advantage of allowing large shifts in the refractive index of the rings' waveguides and therefore a large modulation of their resonant frequencies. On the flip side the modulation speed in charge injected devices is limited by the diffusion speed of minority carriers in Si that have a characteristic time around 1 ns. To enhance the speed of such devices up to a few tens of Gbps, pre-emphasis techniques need to be applied [20]. Depletion-mode devices have much larger operating frequencies as they rely on the much faster majority carrier dynamics but the tuning range is limited by initial doping level of the ring waveguide. High doping levels result in higher losses in the ring. Usually, the rings are designed to trade-off modulation depth and tuning range and have lower modulation depth than injection-mode rings.

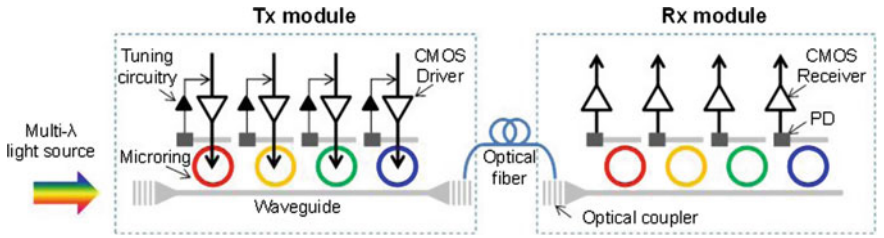

Fig. 18.5 Microring-based optical transceiver schematic

Cascaded microring modulator is a promising method to create multiple independently modulated data streams at different wavelengths for short-reach dense wavelength division multiplexing (DWDM). A typical system configuration is shown in Fig. 18.5. Such a system is compact in size and does not require additional multiplexers and demultiplexers compared to conventional DWDM modulators. To bring this vision to reality a number of engineering challenges need to be met. The first challenge is to build a suitable DWDM source. One has also to build a control system to lock the rings' resonant frequency to the laser frequency and track any changes in the environment. An energy-efficient modulation circuit is also needed, in particular for injection-mode rings where complex pre-emphasis needs to be applied. Energy-efficient receivers are also needed to transform the signal received by the photodiode back to levels appropriate for CMOS logic. Once these various components are demonstrated packaging issues will need to be addressed to make this solution viable for deployment in a cost-effective way at scale.

The multiwavelength DWDM spectrum for ring-based transceivers can be generated by either an array of single-wavelength lasers [21] or a single comb laser. Innovations in quantum dot (QD) multiwavelength lasers with Si photonic microring resonators [22] may lead to low-cost and scalable DWDM solutions avoiding the temperature control, wavelength tracking, and complicated packaging issues that make laser arrays impractical at a large scale. As shown in Fig. 18.6 a single diode comb laser based on QDs provides multiple narrow-spectrum and low-noise laser tones, each corresponding to a longitudinal cavity mode [23]. The QD comb laser can therefore enable simpler and more compact interface design, and therefore enable nanophotonic interconnects with lower power consumption when compared to an equivalent design with multiple discrete lasers and components. Recently, concurrent multichannel transmission at 10 Gbps per channel of a DWDM Si photonic transmitter based on a single quantum dot comb laser and an array of microring resonator-based modulators has been demonstrated [24].

Si ring resonators' resonant frequencies are sensitive to temperature variations and fabrication tolerances. Poor extinction ratio results when the modulator's resonance is not aligned with the input continuous-wave laser wavelength. A closed-loop adaptation scheme is necessary to stabilize the ring's resonance to match the input laser. Thermal tuning schemes with closely integrated heating resistors [19], which red-shift the resonance wavelength as the device is heated up,

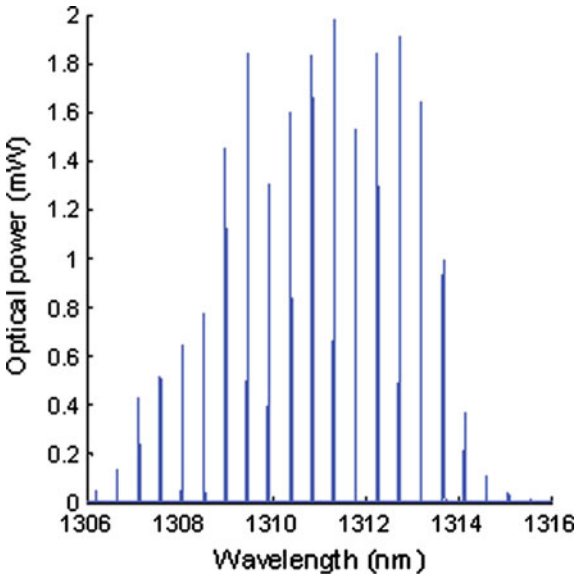

Fig. 18.6 Optical spectrum of a multiline quantum dot comb laser. Spectrum taken at a temperature of 25 °C and current of 150 mA

are commonly proposed for tuning. However, thermal time constants in the millisecond range limit the speed of this tuning approach. Another important consideration is the tuning power efficiency, which varies for thermal tuning depending on the fabrication. Doping a section of the ring waveguide differently to realize a thermal resistor is relatively simple, but this has been shown to have a relatively poor 42 μW/GHz tuning efficiency [19]. Improved efficiencies close to 10–15 μW/GHz have been demonstrated using approaches such as substrate removal and transfer for an SOI process [25] and deep trench isolation for a bulk CMOS process [26]. Finally, superior efficiencies in the 1.7–2.9 μW/GHz range have been achieved with localized substrate removal or undercutting [27], but this comes at the cost of complex processing steps. Compared with thermal tuning, bias-based tuning uses charge injection to tune the resonance of a ring resonator [28]. This approach allows efficiencies on the order of 6.8 μW/GHz efficiency without additional fabrication steps. Combining the two tuning mechanisms can help further improve the efficiency and agility of the tuning mechanism [29].

An efficient driver for a microring modulator is a key component of a transceiver. Injection microrings require pre-emphasized driving signals to achieve data rates in excess of 10 Gbps that are required for modern links [20]. The pre-emphasis signal is used to achieve fast loading of the injected charges into the ring structure but avoid excessive charge accumulation [28]. The balance can be achieved by tuning the pre-emphasis duration and amplitude. Drivers built in a 65-nm process have been shown to allow one to build both a 4 V_{PP} architecture and a 2 V_{PP} architecture with data rates of 4 and 9 Gbps, respectively, and sub pJ/bit power consumption [28]. Depletion-mode microrings allow for faster (25 Gbps) modulation at higher voltage (4.4 V_{PP}) [30].

The receiver architecture is also critical for power performance. Typical CMOS-based receivers consist of a trans-impedance amplifier (TIA) followed by a bank of comparators. A receiver has to work for the worst-case scenario of link loss budget and therefore have high power consumption. Adaptive schemes can help reduce power consumption without compromising performance. One such scheme using eye-opening monitors and active control of the TIA power supply has demonstrated power savings up to 40 % [28].

The main open question to bring a microring-based transceiver to market is the ability to package the transceivers in a stable and cost-effective way. While there are examples of products in the market that package Si photonics components, we believe that there is space for innovation in many aspects of packaging related to Si photonics transceivers. Enabling full 3D integration by the use of through-Si vias (TSVs) would greatly enhance the technology viability and reach. Development of reflowable fiber attachment methods would also simplify assembly.

18.3 Hybrid III–V-on-Si Transceivers

Si, as the most mature semiconductor material particularly for microelectronics in the past half century, has been explored intensively in the past 15 years to be the platform for photonics as well. In addition to advanced complementary metal-oxide semiconductor (CMOS) technology, Si material itself embraces desirable features like lower optical loss, better thermal and mechanical properties, etc., compared to other semiconductor materials. Enormous progress has been achieved to demonstrate high-performance Si modulators [31], photodetectors [32–34], and a variety of passive components [35, 36]. The progress discussed in the previous section is an excellent example of Si photonics. However, Si's indirect bandgap characteristic still poses a great challenge to make Si an efficient light-emitting material after decades of research.

In order to integrate a direct-bandgap material or light source device on Si, monolithic growth and hybrid approach are two typical venues. The traditional approach to hybrid integration, also the first successful commercialization, is to take prefabricated III–V lasers and amplifiers and die bond (i.e., flip chip bond) these elements onto a passive planar lightwave circuit (PLC), e.g., silica-based PLC initially and shifting to CMOS Si PLC right now [37, 38]. This solution provides an optical carrier with high power capability and state-of-the-art performance with low threshold current, low relative intensity noise (RIN), and high wall-plug efficiency [39, 40]. It also relies on mature devices and allows the prescreening of the lasers before assembly to ensure good reliability. Therefore, it has been the mainstream approach for photonic interconnect products in the current market. Luxtera is the leader of this technology. Luxtera's 40 Gbps Si CMOS photonics chip shows a DFB laser module flip chip bonded on a Si CMOS photonic chip to provide a cw light source [41]. The cw laser output is sent into the CMOS photonic chip through near-vertical couplers based on diffraction gratings, and split into four streams to

feed four independent MZI modulators. The company's newest 4 × 26 Gbps transceiver module still employs similar architecture as previous 4 × 10 and 4 × 14 Gbps products, showing data handling expandability [39, 42].

In addition to grating couplers, edge coupling via a spot size converter is another popular approach. Though it takes more fabrication effort to make a spot-size converter than a grating coupler, it has the advantage of much larger optical bandwidth over a grating coupler. Figure 18.7 shows the schematic of a III–V diode

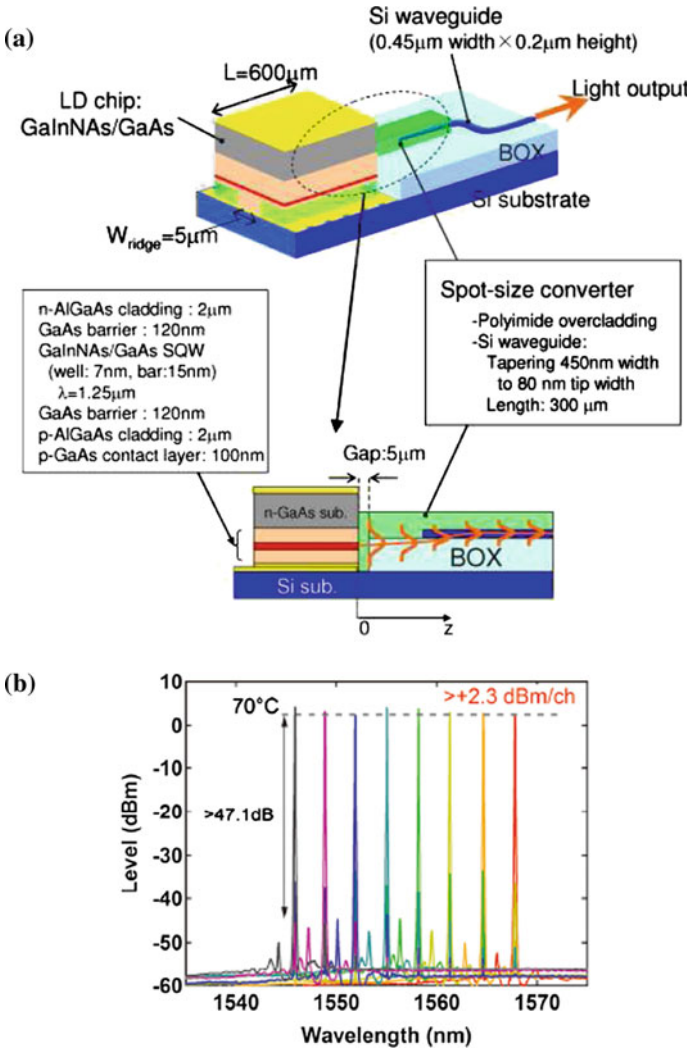

Fig. 18.7 **a** Schematic illustration of laser diode chip integrated on Si waveguide with spot-size converter [43]. **b** 8-λ superimposed spectrum of flip-bonded AlGaInAs DFB laser array under 100 mA × 8 channel simultaneous operation at 70 °C [44]

laser die flip chip bonded to the Si substrate of a SOI wafer and output aligned with a spot-size converter in the Si waveguide [43]. The 600-μm-long Fabry–Perot (FP) laser cavity is defined by two as-cleaved facets. This integration scheme also gains another advantage in better thermal management. As reported in the literature and to be discussed in more detail later in this section [45, 46], heat dissipation in III–V-on-SOI structure is a serious problem to device performance and can pose reliability issues as well. The thick BOX layer blocks the heat from the III–V junction, so TEC cooling at the Si substrate is of very little use. By partially removing the top Si layer and BOX layer, the III–V die can directly contact with Si substrate through a thin AuSn layer to ensure efficient heat dissipation. An impressive characteristic temperature (T_0) of 132 K was thus obtained from a GaInNAs-based QW structure at 1250 nm [43]. Very recently, an 8-channel multiwavelength hybrid laser array was also demonstrated in the same platform (Fig. 18.7) [47]. Benefiting from high-performance InAlGaAs-based DFB laser arrays, the lasing wavelength is pushed to a 1550 nm window and the hybrid chip shows excellent spectral characteristic even at 70 °C. Another similar design is to use the III–V part only as a SOA to provide optical gain and Si waveguide components are involved in defining the laser cavity [48, 49]. Thus advanced CMOS fabrication gives more freedom to define Si-based low-loss, compact distributed Bragg reflector (DBR) or microring resonators to realize more functionalities.

The primary challenge in this traditional hybrid integration approach, however, is optical coupling between parties. The resultant alignment inaccuracy and low throughput, mode mismatch, and back reflection all contribute to high link power budget and total chip cost. To keep the excess loss within 1 dB, normally the alignment accuracy has to be sub-μm. The reported throughput of the above approach is about 60 chips/h [43]. The relatively large III–V footprint and the difficulty to fabricate the multiple wavelength light source in a cost-effective fashion also drive the industry to look for more integrated solution.

Two new similar III–V-on-Si integrated approaches were developed recently to enable a more advanced and seamless integration. Figure 18.8a, b shows their schematic structures which were developed by a joint effort of Intel and the University of California, Santa Barbara [50, 51], and Ghent University [52, 53],

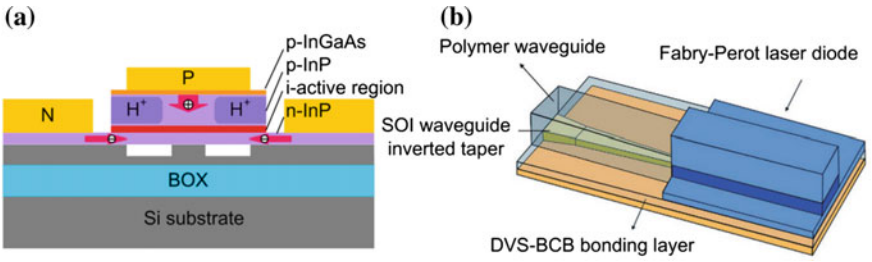

Fig. 18.8 Schematic structure of **a** hybrid Si device platform and **b** heterogeneous integrated device platform

respectively. Both approaches start from defining the photonic waveguide circuits on a SOI wafer and then transfer the thin III–V gain material on them by wafer bonding. Upon bonding and thick III–V substrate selective removal, the typical transferred III–V thin film is in the range of 500 nm to 2 μm thick, rather than finished III–V lasers with a bulky substrate (>100 μm thick). This film normally consists of a quantum well-based active region, InP and/or InGaAs metal contact layers and cladding layer(s). Such a thin film structure allows the bonded hybrid wafer to be treated like a planar surface so the III–V device structure can be fabricated afterward using standard lithography, etching, and deposition processes.

For the structure shown in Fig. 18.8a, named a hybrid Si device platform, the III–V thin film is bonded on a patterned SOI surface using a low-temperature, O_2-assisted direct bonding process, which leads to around 15-nm-thick native Si and InP oxides at the interface. Then an III–V mesa, much larger than the Si waveguide underneath, is formed. Proton implantation can be used to create a current flow channel in the relatively thick p-InP cladding for preventing current spreading [54]. After placing the p- and n-type contacts on the corresponding contact layers, electrons and holes can be injected in and recombined to emit photons from the active region. Because of the great proximity between the Si and III–V active region, a large portion of the optical mode resides in the Si waveguide. A 3–10 % optical confinement in the quantum wells is normally enough to provide enough optical gain for laser or amplifier applications [54, 55].

For the structure shown in Fig. 18.8b, named a heterogeneous integrated device platform, the III–V epitaxial layer transfer is achieved using the thermosetting polymer divinylsiloxane-benzocyclobutene (DVS-BCB) adhesive bonding [52]. A typical DVS-BCB layer is in order of several tens to hundreds of nanometers thick with a refractive index $\sim$1.5 at λ = 1.55 μm. If the BCB layer is several hundreds of nanometers thick, photons generated in the III–V active region cannot couple into the Si waveguide instantly, as shown in Fig. 18.8a. Therefore, an optimal adiabatic inverted taper structure is employed to achieve good coupling efficiency and fabrication tolerance between the III–V waveguide and Si nanowire waveguide. As shown in Fig. 18.8b, the Si inverted taper structure is buried underneath the polymer waveguide. The inverted taper tip width has to be sufficiently small in order for the fundamental optical waveguide mode at the tip to resemble the waveguide mode of the polymer waveguide and III–V waveguide closely [52]. In the case of thin BCB bonding ($\sim$tens of nanometers), light can be more readily evanescently coupled to the Si waveguide, but most of the light is still guided by the III–V waveguide instead of the Si waveguide in the hybrid Si device structure [56, 57]. So quantum well optical confinement in the heterogeneous structure design is typically higher with less optical power output from the Si waveguide. The formation of III–V mesa and electrodes is similar to the first platform.

Since the demonstration of FP lasers on both platforms, numerous photonic devices, such as lasers (racetrack [58], microring/microdisk [59, 60], DBR [61, 62], DFB [56, 63], mode lock [58, 64], AWG [65], tunable [66, 67], etc.), amplifiers [55, 68], modulators (MZI [69], EAM [70]), and photodetectors [71–73] have been

fabricated. As the power consumption is the top priority to photonic link in a data center application, the microring resonator laser emerges as one of the promising candidates, particularly for HP's photonic interconnect roadmap [59, 74]. Figure 18.9a shows the schematic of the hybrid Si microring laser. The laser comprises an III–V ring resonator on top of a Si disk with the same diameter. The fundamental whisper-gallery mode shifts toward the resonator edge as shown by a beam propagation method (BPM) simulated mode profile in the inset of Fig. 18.9a. The III–V epitaxial structure includes five periods of InAlGaAs-based, quantum wells (λ_g = 1.51 μm) plus a p-doped 50-nm-thick InAlGaAs separate confinement heterostructure (SCH) layer that are sandwiched by a 110-nm-thick n-doped InP contact layer and a p-doped 1.5-μm-thick InP cladding layer. This structure is bonded on top of a SOI wafer with a 350-nm-thick Si device layer, resulting in confinement factors of 15.2 and 51.7 % in the active region and Si, respectively. A SOI bus waveguide is s = 50–500 nm away from the resonator, which determines the coupling coefficient from microring laser to the bus waveguide. The SOI waveguide is then connected to two integrated photodetectors to capture the laser output power. The detailed fabrication procedure can be found in [59].

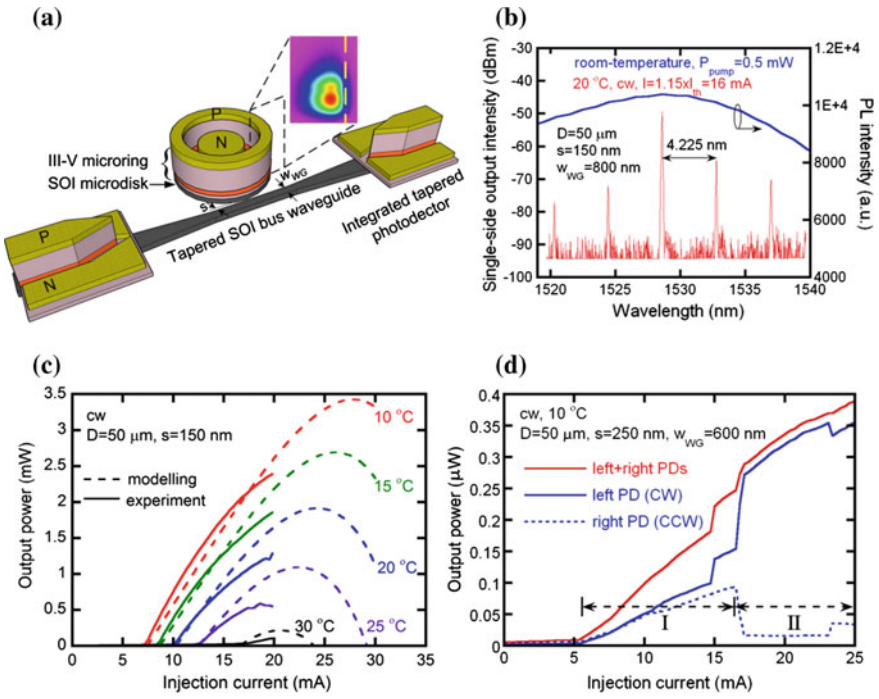

Fig. 18.9 **a** Schematic structure of a hybrid Si microring laser with two integrated hybrid Si photodetectors and a simulated BPM mode profile, **b** measured PL response and lasing spectrum [59], and typical device LI characteristic for **c** strongly coupled and **b** weakly coupled situations. The lasing temperature dependence is shown in (**c**) and bidirectional lasing is also shown in (**d**)

Figure 18.9c, d shows the typical cw, temperature-dependent light–current (LI) characteristic of devices with 150 and 250 nm coupling gaps, respectively. Devices with the III–V junction side up sit on a copper stage whose temperature is actively controlled. For a coupling gap s = 150 and 250 nm, the minimum threshold currents are 8.4 and 5.2 mA at 10 °C, respectively. The higher threshold in Fig. 18.9c results from a larger coupling coefficient with a narrower coupling gap, which also leads to much higher output with over 2 mW maximum power. The typical broadband spectrum in Fig. 18.9b shows that multiple longitudinal cavity modes lase when the device is driven at 1.15 × I_{th} at room temperature. The primary lasing peak is aligned with the photoluminescence maximum at 1528.57 nm. The free spectral range (FSR) is 4.2 ± 0.05 nm, which agrees with the calculated value of 4.3 nm [59].

Theoretically, a shorter cavity length can result in a smaller threshold current and subsequently a small power consumption. However, device size reduction can increase the device thermal impedance and subsequently the device self-heating effect. High temperature degrades the device performance (e.g., higher threshold and lower efficiency), shifts the lasing wavelength, and limits the direct modulation bandwidth. The model in Fig. 18.9c indicates thermal rollover in laser output power if the injected current continues going up. Joule heating is even more obvious in those active devices built on this hybrid Si platform, because of the thick (typically 800 nm) buried oxide layer (BOX) as previously explained. While SiO_2 is 100× worse in thermal conductivity than Si, an 800 nm or thicker BOX layer is necessary to prevent optical leakage into the Si substrate. So it becomes an intrinsic thermal bottleneck to all SOI-based active devices. Figure 18.10 presents the simulated temperature rise in the heterogeneous microring laser active region at threshold and corresponding thermal impedance values as a function of microring diameter [74].

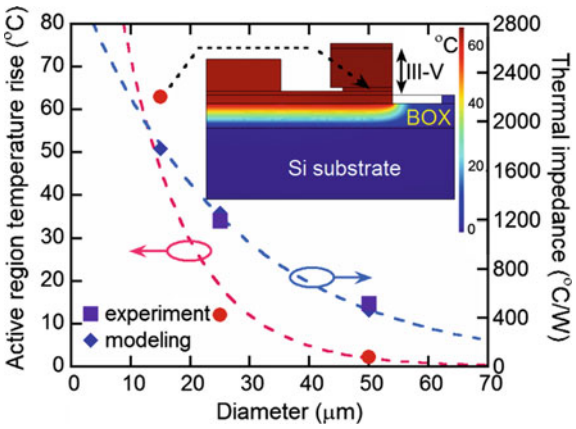

Fig. 18.10 Calculated active region temperature rise at threshold and experimental and modeling thermal impedance as a function of device dimension. (*Inset*) FEM modeling of a D = 15 μm device temperature profile at the threshold of 9.4 mA [74]

A finite element method was employed, but the simulation is based on the experimental device series resistance and threshold. The predicted temperature increase in the active region is 2.5 °C for a D = 50 μm device and grows exponentially to 63 °C for D = 15 μm, which makes it extremely challenging to scale down the device size [74].

An effective thermal shunt approach was recently developed to get away from the heat blocking in the BOX layer [75, 76]. The idea is to etch some trenches through the top Si layer and BOX layer within or around the III–V mesa, and then fill the trench with highly thermal conductive materials. Figure 18.11a shows the 3D schematic of a heterogeneous microring laser whose p-type contact and III–V-on-Si mesa are mostly surrounded by a layer of Au, and this Au shunt extends and contacts with the Si substrate after locally removing the top Si and BOX layers. The N-type contact inside the mesa also connects to the Si substrate through another Au thermal shunt. This double metal shunt design enables the joule heat from the III–V mesa to be effectively "grounded" to the Si substrate through Au shunts [76]. Figure 18.11b, c shows the stage temperature-dependent LI curves for D = 50 μm

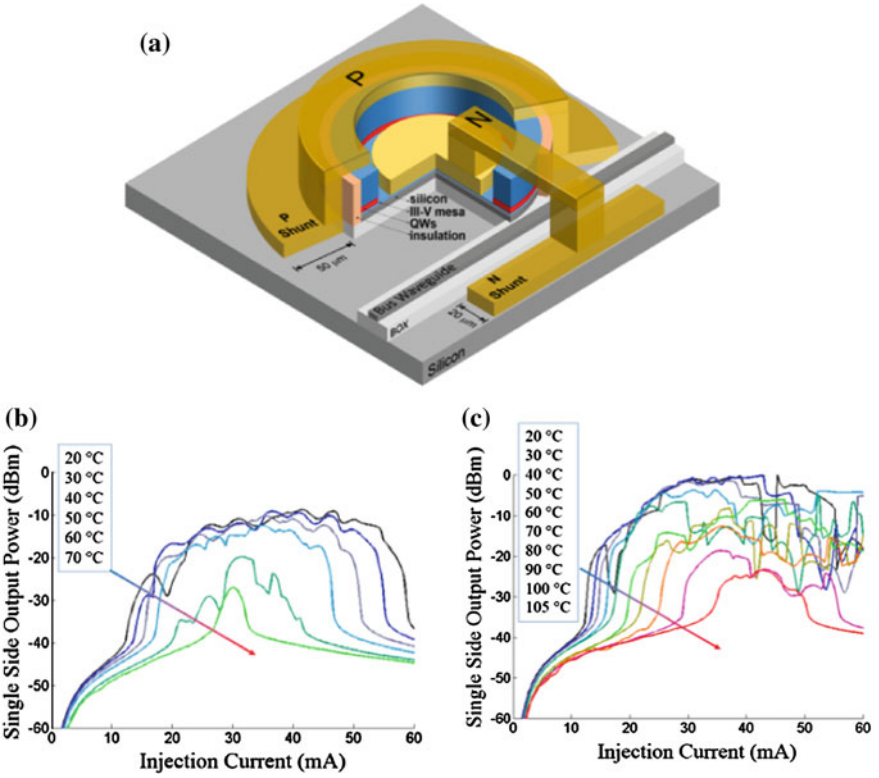

Fig. 18.11 **a** Illustration of heterogeneous Si ring laser with thermal shunts, and LI curve of 50 μm in diameter heterogeneous Si microring lasers **b** without and **c** thermal shunt design [76]

devices with and without thermal shunts, respectively. When the stage temperature was at 20 °C, both devices shared the same threshold current around 12.3 mA. The device without the thermal shunt had an earlier thermal rollover in the output power in the LI curves, and its maximum CW lasing temperature was about 70 °C. The device with double thermal shunts, in contrast, was able to lase cw up to 105 °C. The LI curves show a slower thermal rollover at the same stage temperature with the output power 8–10 dB higher. With the help of this thermal shunt design, the measured thermal impedance for devices in 50, 30, and 20 μm diameters is reduced from 580, 1031, and 1591 °C/W to 364, 652, and 1105 °C/W, respectively. Clearly, a 30–40 % improvement in thermal impedance was achieved on the devices with thermal shunts designs, where the maximum cw lasing temperatures were raised by over 35 °C [76]. Cu, instead of Au, can also be used and may lead to better results due to its higher thermal conductivity than Au and preferred CMOS compatibility.

In addition to integrating thermal shunts with heterogeneous devices to reduce the BOX layer-induced thermal barrier issue, a more advanced approach is to replace the entire BOX layer with another material that can conduct heat much better, and has the proper optical properties (e.g., refractive index, absorption coefficient, etc.). Diamond is a good candidate because of possessing the highest thermal conductivity among bulk materials in nature, and excellent optical properties, plus CMOS compatibility [77–79]. A recent demonstration of Si-on-diamond (SOD) substrate fabrication and low-loss SOD waveguide provides a promising answer here [80]. However, issues associated with diamond growth and wafer bonding and device fabrication require additional study.

With the help of reduced device heating from efficient thermal shunt design, devices now can operate at higher direct modulation bandwidths. Figure 18.12a shows a comparison of small-signal direct modulation response for two devices with the same dimension of D = 50 μm, same injection current of 25 mA, and similar output power [81]. The one with a thermal shunt shows a 3 dB bandwidth of 5.5 GHz, while bandwidth for the other one without a shunt is only 3 GHz. Figure 18.12b shows the same measurement on the device with a thermal shunt at different injection currents. Higher injection current, corresponding to higher output power (before thermal rollover), leads to larger bandwidth, which is expected. A maximum bandwidth of 7.8 GHz is observed at 35 mA injection current. Figure 18.12b inset shows a plot of resonance frequency versus square root of DC injection current, showing the expected linear dependence. The slope is 0.81 GHz/mA$^{1/2}$, 3X better than with previously demonstrated hybrid Si DBR lasers [62]. Figure 18.12c shows the measured open eye diagram at 12.5 Gbps with a7.9 dB extinction ratio. It corresponds to the power consumption of 5.28 pJ/bit. The noise at a "1" level is mainly from the stage temperature fluctuation between 25 and 27 °C, because the thermal electrical controller which was used for the temperature-dependent LI measurement in Fig. 18.11 was not available at the moment of dynamic measurement here. Furthermore, the 1 nm optical filter bandwidth is not narrow enough to filter out most of the ASE noise, which also contributes to the noise in the eye diagram [81].

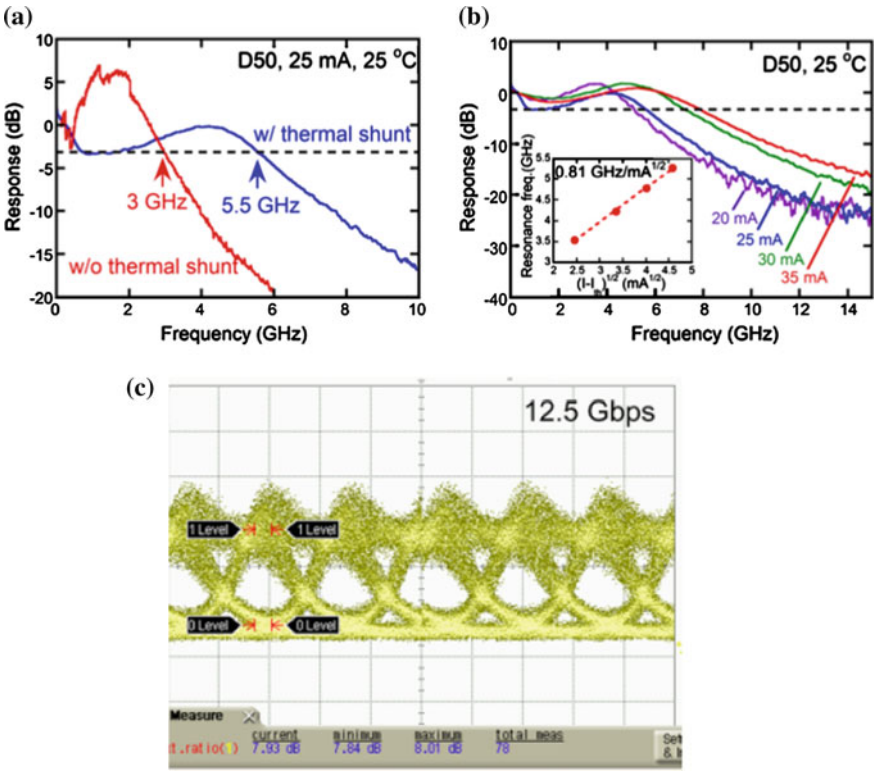

Fig. 18.12 **a** Measured small-signal responses for $D = 50$ μm devices at 25 mA injection current with and without thermal shunt design, and **b** small-signal response for thermal shunt ring at 20–35 mA injection current. *Inset* Resonance frequency as a function of square root of dc injection current, **c** measured open eye diagrams for a $D = 50$ μm device at 12.5 Gbps modulation rate [81]

Directional bistability, the ability of a laser to operate either in the clock-wise (CW) or counter-clock-wise (CCW) mode, is a unique characteristic of ring lasers [82]. Bistability has been used to demonstrate optical switching and logic applications [83, 84] in III–V microring lasers. This feature has also been observed in Fig. 18.9d where bidirectional lasing exists in the low current injection zone (I) and lasing at one direction can dominate in the high current injection zone (II). While useful for some applications [83], bistability is undesirable for microring lasers used in optical interconnects. Different devices of the same design can lase in different directions or switch lasing direction depending on the injection current and temperature.

A number of approaches have been demonstrated to achieve stable unidirectional lasing. "S-shape" ring resonator cavities are designed to introduce asymmetric round-trip loss/gain [85], but the modified resonator structure can add additional round-trip optical loss. Optical pulse injection from an external laser or light-emitting diode (LED) has also been used to increase the net modal gain in one

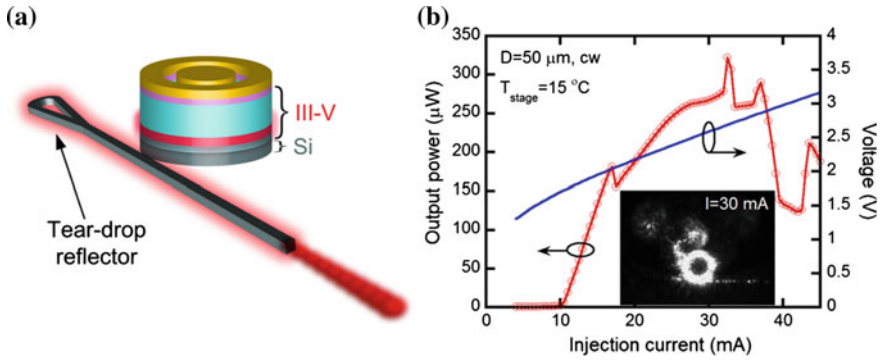

Fig. 18.13 **a** Schematic of a ring laser with an external reflector integrated on the bus waveguide. **b** LIV characteristic of a D = 50 μm device. *Inset* IR image of the device at 30 mA current injection [88]

direction [82, 86, 87]. The expense is increased chip complexity and total power consumption. A new design without sacrificing laser performance and energy cost is shown schematically in Fig. 18.13a, in which an optical reflector (a tear-drop reflector design in this case) at one end of the bus waveguide induces the laser to emit light toward the other end [88]. In this structure, light emitted in the CW mode is partially coupled back to the CCW mode. The power circled back into the cavity leads to a photon density increase and unidirectional lasing in the desired direction (CCW here) [88].

Figure 18.13b shows the LI–voltage (LIV) characteristic of a 50-μm-diameter laser, where the output power was measured by single integrated photodetector at one side of the bus waveguide. The inset shows an infrared (IR) image of the unidirectional laser at 30 mA injection current. No power sudden jump/drop seen in Fig. 18.13b is realized from lasing up to 38 mA injection current, indicating stable unidirectional lasing. The dip around 40 mA is attributed to the interference of the laser CCW mode and the back-reflected light from tear-drop reflector, which is a function of the phase of the reflected light. When a reflector is added the light from the CW and CCW light will interfere at the coupler. Depending on the phase of the reflected light, constructive or destructive interference will occur. Constructive interference will maximize the laser CCW output. Destructive interference reduces the feedback to the point that the laser goes back to its free-running, bistable operation. A short distance between the laser-bus waveguide coupling point and the reflector is therefore desirable to minimize the phase difference for this design [88].

A similar unidirectional design using a DBR rather than a tear-drop reflector has been realized on the heterogeneous integrated microdisk laser, which shows sub-mA threshold [89]. A microdisk laser-based optical flip-flop [90] and multi-wavelength laser array [91] have also been demonstrated with impressive performance. More and more hybrid/heterogeneous integrated lasers [92] are being

fabricated that show a variety of robust functionalities and are becoming practical for commercialization.

On the other hand, photodetectors are another critical component to enable a high-quality photonic link as discussed previously. Due to the Ge growth temperature [93], it is challenging to integrate hybrid/heterogeneous III–V-on-Si lasers with Ge-based photodetectors. It is, thus, more realistic to build III–V-on-Si photodetectors [72] along with the laser counterparts. The detector design is shown as a top-view and a cross-sectional view in Fig. 18.14a, b, respectively. The III–V epitaxial layers consist of an intrinsic InGaAs absorption layer sandwiched between p- and n-InGaAs contact layers that are 100 and 200 nm thick, respectively. Light is launched into a Si rib waveguide and a blunt taper transitions, the optical mode from a pure Si mode to the hybrid mode, where most of the light is confined in the absorption layer. A key III–V epitaxial design feature is to find an optimal absorber thickness to maximize the responsivity, while it is not unnecessarily thick and thus resulting in a long carrier transition time and increased fabrication complexity.

Device performance also directly depends on the device dimension, the device length in particular. A good trade-off between responsivity and high-speed bandwidth is found with a device 4 μm wide and 30 μm long. Figure 18.15 shows the performance of the fabricated devices. A good responsivity of 1.18 A/W, corresponding to 95 % quantum efficiency, is achieved. An extremely low dark current of 10 nA is typical at −3 V. At this bias, an over 30 GHz 3 dB bandwidth and open eye diagram at 25 Gbps are measured, showing a promising perspective to integrate with lasers and passive Si photonic circuits to complete a hybrid transceiver.

The roadmap of the microelectronics industry development indicates that Si is unlikely to be replaced by other materials. The urgent need to break the “brick wall” of interconnect bandwidth and power consumption in the microprocessor

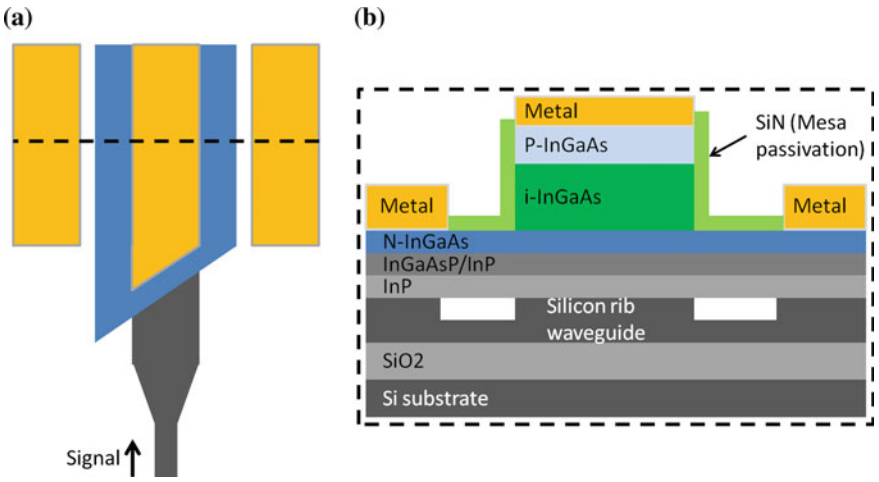

Fig. 18.14 **a** Top-down and **b** cross-sectional diagram of the hybrid Si detector

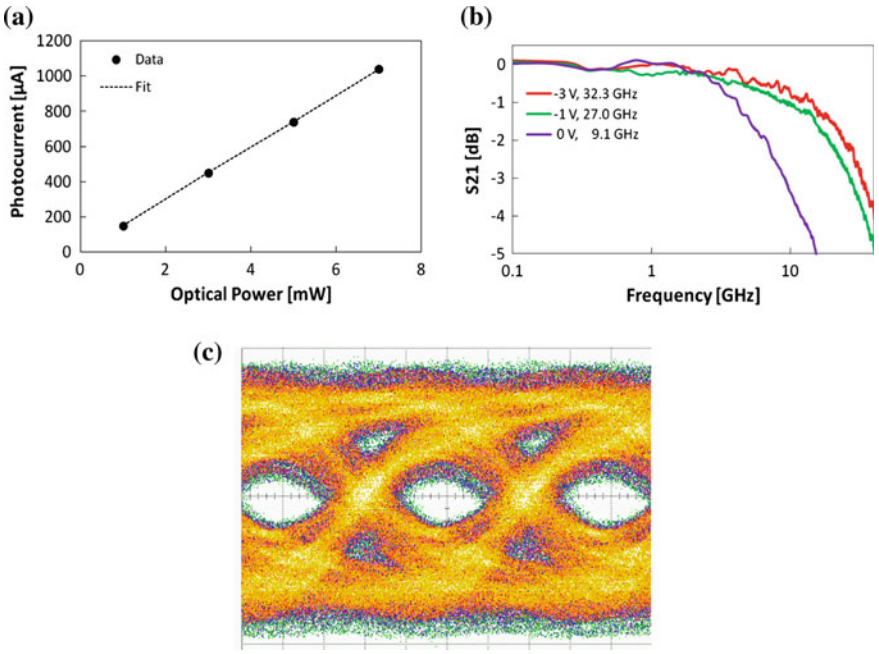

Fig. 18.15 **a** Measured photocurrent versus injected optical power, showing a responsivity of 1.18 A/W, **b** 3 dB bandwidth measurement at different bias and **c** measured eye diagram at 25 Gbps

application, particularly the data center application, and other emerging applications is a compelling force to make Si the primary host material for photonic integrated circuits as well. Equipped with the recently developed Si photonics, and hybrid/heterogeneous lasers, photodetectors, plus advanced CMOS drivers, sophisticated Si PICs will serve as the backbone for new architecture to bring the next generation of data centers to the world soon.

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Index

A
Abstracted, 158
Abstractions, 176
Accidental coincidence, 60
Accumulated dispersion, 463–465
Active optical cable, 33, 349
Active phase shifters, 149
Adiabatic coupling, 250
Advanced CMOS node, 358
Advanced modulation, 403
A generic integrated technology platform, 197
Aggregator, 269
Alignment marks, 251
Alignment tolerance, 226
Alpha- and Beta runs, 203
AMPLE, 120
Analog-to-digital converters (ADC), 164
Analog integrated circuit design, 102, 121, 130, 147
An edge-coupling, 220
An error-free data link, 18
Application program interface (API), 177
Applications, 162
Arbitration, 169
Architecture, 161, 167
ArF immersion lithography, 32
Arrayed laser diode, 4
Arrayed waveguide grating (AWG), 32, 103, 161, 379, 400
ASIC, 100
Aside on a rack, 241
Athermal, 21, 84, 97
Athermal AWG, 87
Athermal condition, 96
Athermal design, 92
Athermal MZI, 96
Automation, 241

B
Back-end integration, 5
Balanced-photo-diode, 331
Ball-lens, 227
Bandwidth, 318, 320
Bandwidth density, 2
Beat frequency, 335
Bending radius, 399
Bias voltage, 116
Binary phase-shift keying (BPSK), 449, 462, 464, 465
Birefringence, 399
Bit error rate (BER), 113, 462–465
Bit rate per channel, 407
Bragg grating, 138, 148
Bragg reflector, 303, 304
Bragg resonance, 328
Bragg wavelength, 328
Built-in self-test, 367
Burn-in, 258
Burst mode transmission, 169
Business model, 269
Butt-coupled lasers, 7
Butterfly package, 391

C
CAD Framework Initiative, Inc. (CFI), 150
Carrier, 496
Carrier density, 144
Carrier depletion, 497
Carrier depletion PN junction, 309
Carrier dispersion modulators, 139
Carrier injection PIN diode, 309
Carrier-suppressed double-sideband (CS-DSB) condition, 341
Cascaded-MZIs-based bandpass filter, 324
Cascaded microring modulators, 498

L. Pavesi and D.J. Lockwood (eds.), *Silicon Photonics III*,
Topics in Applied Physics 122, DOI 10.1007/978-3-642-10503-6

CEA-Leti, 139
Central arbiter, 181
Centralized arbitration, 180
Charge accumulation, 497
Chemical–mechanical polish analysis (CMPA), 124
Chemical vapor deposition, 353
Chiplets, 378
Chip-scale, 159
Chip-to-chip communications, 278
Chip-to-chip interconnects, 312
Chip-to-memory interface, 312
Circuit, 170
Circuit replacement, 175
Circuit simulator, 101, 151
Clock and data recovery (CDR), 173, 367
Closed-loop control, 164
Cloud data centers, 403
CMOS, 123, 124, 128, 133, 135, 138–141, 147, 448, 449, 451, 465
CMOS compatible, 93, 96, 97
CMOS photonics, 422
Coherent detection, 466
Collimated beams, 254
Colorless, directionless, contentionless (CDC) ROADM, 435
Communication, 160
Compact models, 101, 103, 104, 110, 113–115, 138, 146, 147, 149, 150
Complete library, 379
Compound semiconductors, 35
Computer-aided design (CAD), 100, 102, 104–108, 117, 119, 140, 147, 149
Computing, 157
Connection, 160
Constant bias-current condition, 25
Constraints, 105, 107, 108, 122, 124, 131
Consumer cables, 275
Continuous-wave illumination, 116
Control, 157
Coplanar waveguide, 450, 451
Corner lots, 265
Corners, 361
Correct-by-construction (CBC), 104, 111
Coupler
  directional, 141
  fiber, 139
  fiber chip, 121
  grating, 103
Coupling, 159
Critical dimension, 194
Cross-phase modulation, 57
Crosstalk, 169
Cross two-photon absorption, 60
Crystal dislocation defects, 352
Custom integrated circuit design, 153

D
Data center (DC), 182, 278, 297, 375, 403, 441, 490
Datacenter applications, 350
Datacenter interconnects, 476
Datacenter network fabric, 476
Data center virtualization, 491
Data-centric computing, 2
Data explosion, 1
Data farm, 266
Data traffic forecast, 267
Deep-rib (DRIB) waveguide, 307
Deep UV lithography, 141
Delay, 110, 119, 140
DEMUX, 103
Dennard scaling, 489
Depletion region, 449, 455, 457
Deposition, 93
Deserialization, 177
Design for manufacturing (DFM), 105, 124
Design for test (DFT), 105
Design houses, 272
Design kit, 280, 294, 296
Design rule check (DRC), 103, 124–130, 148
Detectors, 109, 149
Device self-heating effect, 505
Device thermal impedance, 505
Device-under-test, 274
Dielectric thin film materials, 102
Digital coherent communication, 449, 468
Digital delays, 364
Digital integrated circuit design, 102, 147
Digital-to-analog converters (DAC), 164
2.5 D integration, 350
Directional bistability, 508
Directional couplers, 323
Disaggregation, 2
Dispersion penalty, 463
Dispersion tolerance, 449, 463, 465
Distributed arbitration, 181
Distributed feedback lasers (DFBs), 485
2.5D or 3D SiP packaging technology, 377
Double ring network, 427
Down-converter, 317
Drude theory, 459
Dual-polarization quadrature phase-shift keying (DP-QPSK), 449, 457
Dynamic service, 404

E
E-beam lithography, 140–142
Edge-coupling, 222
Edge emitting, 254
Edge emitting lasers, 7
Effective index, 85
Efractive index difference, 221
EIT-like effect, the, 328
Electro-absorption modulator, 381
Electromagnetically induced transparency (EIT)-like effect, 327
Electronic design automation (EDA), 100, 123–126, 129, 134, 142, 145–147, 150, 151, 153, 361
Electronic integration, 75
Embedded optics, 483
Encapsulated, 158
Entanglement, 68
Epitaxy, 139
Epoxy, 245
Equation-based DRC (eqDRC), 125, 127, 128
Erbium-doped fiber amplifier, 324
Error-free data links, 26, 29
Etch, 129, 135, 136, 138–140, 149
Ethernet switch, 478
Evanescent coupler, 51, 226, 399
Extended industrial temperature range, 28
Extinction ratio, 309, 498
Eye diagram, 113, 114, 116, 118, 381

F
Fabless, 262
Fabless silicon photonics, 192
Failure-in-time (FIT), 484
Faraday rotator, 369
FDTD, 114, 146, 151
Feedback control, 164
Fiber-arrays, 224, 240
Fiber-to-the-home (FTTH) systems, 388
Field-programmable gate array (FPGA), 28, 162
Figure of merit, 454
FinFET, 282
Firmware-based logical control, 176
Flip chip, 120, 143, 229, 250, 387
Flip-chip bonding, 5
Fock basis, 51
Force sensor, 245
Forward error correction (FEC), 466
Four-wave mixing (FWM), 143
Free-carrier absorption, 458, 459, 461
Free-carrier plasma dispersion, 448, 453, 458, 459, 461
Free spectral range, 318
Frequency chirping, 449, 454, 458, 459
Front-end integration, 5
Fronthaul and backhaul transport, 422
Full bisection bandwidth, 491

G
100-Gb/s channel rate transponders, 403
GDSII, 101, 119, 124, 126, 130, 132, 133, 135, 141, 146–148, 150
Germanium, 139, 287, 352
Germanium photodetector, 4, 412
Gold/tin solder, 257
Graphenes, 35
Grating-coupler, 206, 220, 222, 223, 239, 290, 354, 384, 501
Gripper, 242
Group velocity dispersion, 58

H
Hamiltonian
of vacuum, 56
Hard-mask, 307
Hardware logic, 168
Hardware–software integration, 158, 162
Heat-sinking, 231
Heralding, 54
Heralding efficiency, 67
Hermetic environments, 391
Heterogeneous 2-D/3-D IC integration, 408
Heterogeneous integration, 376, 401
Heterogeneously integrated lasers, 384
Heterogeneous systems-in-package (SiP), 390
High bandwidth density, 20
High density optical connector, 253
High heat dissipation, 14
High index contrast, 354, 398
High output power, 14
High-performance computing, 186
High precision stages, 247
High-radix photonic packet switch ASIC (PhASIC), 493
High-speed phase modulator, 355
Hong–Ou–Mandel interference, *See* quantum interference
Hybrid/heterogeneous integration, 220
Hybrid integration, 357, 500
Hybrid integration with compound semiconductor lasers, 7
HyperX, 492

I
Imaging, 247
IMEC, 139
Immersion lithography, 141

In-band synchronization, 171
Indistinguishability, 47
Industrialize, 279
Industrial processes, 254
Industry roadmap, 392
Infrared, 109, 119
Initialization, 175
Injection modulator, 496
InP material, 377
Insertion-loss, 223, 226, 227, 304
Inspection, 244
Integrated circuits, 100, 123, 124, 127, 128, 130, 138, 145, 147, 150, 153
Integrated heater, 164
Integrated lasers, 376
Integrated photonic circuit, 100
Integrated photonics chips, 145
Integrated references, 386
Integrated signal processors, 318
Integration, 159
Integration technologies, 478
Intensity modulation, 449, 452, 454, 455, 461
Inter-channel crosstalk, 18
Inter-chip interconnects, 2
Interconnect, 112, 120, 124, 134, 152, 157
Interconnect bandwidth requirements, 490
Interfaces, 162
Interferometer, 449, 450, 464, 467
Interleaver, 342
Intermodulation, 169
Internet protocol (IP) routers, 404
Intradyne coherent techniques, 404
Inverted Si nanotaper, 198
IPKISS, 120

J
Joint Spectrum, 68

K
Known good die (KGD), 289, 360

L
Large index contrast, 400
Laser, 109, 115, 120, 135
Laser integration, 239
Laser-pill, 247
Laser source, 245
Laser-welding, 226
Latency, 173
Layout versus schematic (LVS), 103, 117, 124, 130, 132–136, 138, 148, 152
Layout-versus-schematic checking, 361
Light coupling, 197
Linear optical quantum circuits, 49
Linear optical quantum computation, 43, 45, 75
Line card, 482
Linewidth, 140, 141
Link budget, 485
LISEL, 257
Lithography effects, 146
Lithography process verification, 124
Lithography simulation, 136
Loop waveguide, 244
Low-volume access, 263
Luceda, 120, 153
Lumerical Solutions, 153

M
Mach–Zehnder intereferometer (MZI), 14, 52, 86, 95, 101, 103, 106, 108, 120, 318, 497
Mach–Zehnder modulator (MZM), 115, 116, 161, 292, 362, 381, 400
Manhattan Geometry, 119, 127, 134, 138
Manufacturing, 158
Manufacturing design rules, 101
Manufacturing rule check, 272
Many-core processors, 2
Markovian transition matrix, 174
Mass production, 252
MATLAB, 101, 110
Maximum junction temperatures, 27
Mechanical arc, 242
Mechanical tools, 242
Medical diagnostic, 268
Megafabs, 261
Memory bandwidths, 491
MEMS, 368
Mentor graphics, 120, 150–153
Message latency, 491
Metallic interconnects, 287
M factor, 107
Micro-bumps, 230
Microlens arrays, 252
Micro-optical isolator, 227
Microring, 161
Micro-ring resonators, 326, 425
Microring switch, 167
Microsecond-scale, 163
Micro-solder bumps, 492
Microwave photonics, 317
300-mm SOI wafer process, 32
Mode size converters, 399
Modulation, 161, 164
Modulation formats, 486
Modulator, 379
  electro-optical, 113, 115
  optical phase, 114, 115

quadrature amplitude, 114
Monolithic integration, 357
Moore's Law, 281, 408, 489
More than Moore roadmap, 376
MT/MPO connector, 240
Multi-chip module, 2
Multi-core processor architectures, 408
Multi-mode fiber, 34
Multi-mode interference coupler, 51
Multi-project wafer (MPW), 159, 193, 263
Multi-project wafer runs, 139
Multicasting, 184
Multidirectional ROADMs, 429
Multimode interference (MMI), 101
Multimode parallel interconnects, 407
Multimode waveguide, 291
Multiphoton-pair emission, 62
Multiple parallel transmitter devices, 410
Multistage MZIs, 319

N
Nanowires, 250
Narrow channel pitch, 10
Negative TOC, 84
Netlist, 105, 107, 108, 117, 130, 134, 135
Network architecture, 177
Network bandwidth, 491
Nonlinear, 168
Nonlinear sideband, 332
Notch bands, 330

O
OASIS, 124, 135, 141, 146, 150
Occupation number basis, *See* Fock basis
On board assembly, 254
On-board data center, 32
On-board optical transceivers, 483
On-chip light sources, 6
On-chip server, 3
On-off keying (OOK), 449, 457, 460, 462, 464
Openaccess, 144, 150, 263
OpenMatrices, 144, 151, 152
Optical amplifiers, 376
Optical circuit switching (OCS), 35, 441
Optical components, 114, 149
Optical coupling, 502
Optical interconnect technology, 408
Optical interconnection, 3, 239
Optical interface, 393
Optical I/O core, 33
Optical link, 168
Optical modulation amplitude, 364
Optical modulator, 449, 460
Optical network interface card (ONIC), 178
Optical packaging, 401
Optical path, 251
Optical signal processor, 317
Optical signal-to-noise ratio (OSNR), 451, 463, 465
Optical signal-to-noise ratio (OSNR) penalties, 413
Optical technologies, 423
Optical transport networks, 432
Optical wafer sorting, 285, 289
Optimal reflectivity spectrum, 303
OptoDesigner, 120, 122, 138, 148, 153
Ordinary differential equation (ODE), 115
ORMOCER, 253
ORMOCOMP, 253
Out-of-band synchronization, 171
OWTNM, 102
Oxide mode size converto, 198

P
Packaged-level reliability tests, 210
Packaging, 158, 159, 387, 500
Packaging automation, 238
Packaging silicon photonics, 376
Parasitic capacitance, 365
Parasitic extraction (PEX), 124, 134
Parasitics, 357
Partially etched, 222
Passive alignment, 247
Passive alignment technique, 12
Path penalty, 465
Pattern dependence, 169
Peaking routine, 245
Performance benefits, 163
Performance dependencies, 163
Phase modulation, 448, 452, 457
PhoeniX Software, 102, 120, 122, 152, 153
Photodetector, 139, 144, 510
Photodetector responsivity, 116
Photodiode responsivities, 289
Photon indistinguishability, 51
Photon loss, 46, 48
PhotonDesign, 102, 152
Photonic building blocks, 101
Photonic chip, 241
Photonic coupling, 247
Photonic crossbars, 494
Photonic crystals, 35
Photonic integrated circuit (PIC), 102–104, 109, 113, 121, 129, 130, 135, 140, 375
Photonic integration, 425
Photonic interconnect roadmap, 504
Photonic links, 160
Photonic packaging, 217

Photonic packaging solutions, 232
Photonics design automation (PDA), 102, 153
Photonics-electronics convergence system, 3
Photonics node, 282
Photonic system on chip (PSoC), 422
Physical verification (PV), 117, 122, 124, 129, 132, 146, 361
Pigtailing, 237
Pigtailing bench, 240
PIN-PDs, 15
Planar lightwave circuit (PLC), 102
Plasma dispersion effect, 363
Plasmonics, 35
Pluggable, 248
Pluggable optical transceiver, 478
PN-junction, 448, 450, 452, 455–457, 461, 462, 465, 466
Polarization beam splitters/combiners, 401
Polarization diversity, 384, 401
Polarization-diversity WDM receiver chip, 413
Polarization-division multiplexing, 467
Polarization-insensitive WDM receivers, 412
Polarization rotators, 412
Polarization splitter, 334
Polarization splitting grating couplers, 304, 354, 365
Pole–zero diagram, 320
Polymer cladding, 86, 88, 89, 92
Polymer ribbon, 251
Polymers, 399
Positioning accuracy, 359
Power consumption, 278
Power efficiency, 34
Power equalization, 182
Power usage effectiveness, 406
Prealignment, 247
Primitives, 177
Probe-card, 359
Process, 274
Process design kit (PDK), 102–106, 115, 130, 131, 138, 139, 145–150, 152, 153, 265, 361
Processing power, 491
Process modifications, 194
Process modules, 285
Process monitoring, 312
Process repeatability, 248
Process speed, 247
Production, 266
Programmable cell (pcell), 104, 117
Propagation
  bidirectional, 109, 113
  multichannel, 109
  multimode, 109
Propagation constant, 140
Propagation loss, 9, 135, 400
Propagation simulators, 101, 102
Protocol, 173
Push-pull, 448, 461, 462, 464
Push–pull mode, 293
Pyxis, 120, 152, 153

Q
Quadrature phase-shift keying (QPSK), 114, 449, 457, 465, 466, 468
Qualification process, 209
Quality factor, 63
Quantum algorithms, 46
Quantum dot LDs, 21
Quantum entanglement, 44
Quantum information, 43
Quantum interference, 47, 50, 52
  phase-doubled fringe, 53
Quantum state, 49
Quantum technology, 75
Quaternary phase-shift keying (QPSK) signals, 343
Qubit
  operations on, 45

R
Racks, 266
Radio access network (RAN), 422
Radio-frequency (RF) operating signals, 229
Receive, 167
Receiver, 500
Refractive index, 139, 140
Resonance frequency, 310
Resonant microring modulators, 497
Response time, 297
Responsivity, 297, 356
Reticle, 273
RF oscillator, 317
Ribbon cable, 240
Rib waveguide, 449–451, 453, 455
Ring modulator-based transceivers, 310
Ring network, 423
Ring resonances, 328
Ring resonator, 62, 67, 89, 105, 108, 130, 325
  optimal coupling for photon pair generation, 65
Ring-resonator-based OMs, 31
ROADM, 425
Robot, 240

Roughness, 400
Rule decks, 103, 147

S
Scalable interconnect networks, 490
Scale out, 475
Scatter matrix, 101, 111–115, 151
Scheduling algorithm, 178
Schematic capture, 101, 106–108, 130, 134
Schematic-driven layout (SDL), 104, 105, 117, 119, 122, 152
Schmidt decomposition, 68
Scientific applications, 175
Self-phase modulation, 57
Semiconductor amplifiers, 227
III-V semiconductors, 399
Serialization, 177
Seven zeros programmable analog signal processor, 322
Side-wall gratings, 15
SiGe, 352
SiGe detectors, 194
Signal, 107
  bidirectional, 112
  multichannel, 113
  optical, 103, 109, 110, 113, 143
Signal integrity, 113, 114
Signal propagation, 109
Silica AWGs, 86
Silica waveguide, 87
Silicon etching, 250
Silicon integrated wavelength selective switch (SI-WSS), 429
Silicon microring resonators, 492
Silicon nitride, 287, 399, 410
Silicon-on-insulator (SOI), 139, 351, 449, 451, 465
Silicon-on-insulator (SOI) wafer, 378
Silicon optical interposer, 8
Silicon optical modulator, 4, 292
Silicon oxynitride, 399
Silicon patterning, 306
Silicon patterning process, 302
Silicon photonic, 157
Silicon photonic interconnection, 170
Silicon photonics, 3, 87, 422
Silicon photonics foundry model, 204
Silicon photonics MPW services, 199
Silicon photonics optical interconnects, 203
Silicon photonics start-ups, 212
Silicon photonics transceiver, 384
Silicon photonics transceiver chips, 193
Silicon photonic switching, 163
Silicon quantum photonics, 75
Silicon waveguide, 139, 140, 399
Single-mode-fiber, 476
Single-photon detection, 48, 69
Single-photon source, 46
Si_3N_4 microring optical, 341
SiOB, 258
Si ring multiplexers (MUX), 103, 194
Slot waveguide, 89, 92
Smallest bandwidth, 336
Small-scale integration (SSI), 100
Software, 157
Software interfaces, 168
Solder bumps, 256
Soldering, 257
Space division multiplexing, 306
Spatial switching, 161
Spontaneous four-wave mixing, 46, 54
  phase matching, 57, 63
Spot-size converters, 11
Spurious free dynamic range (SFDR), 332
Squeezed state, 62
  two-mode squeezed vacuum, 62
Standard interfaces, 186
Statistical process control (SPC), 203
Substrate, 196
Subsystems, 158
Supercomputers, 403
Supercomputing, 182
Surface grating coupling, 198
Switching, 161, 164
Symmetric MZI-based OMs, 23
Synchronization, 169, 170
System in package (SIP), 2, 143, 145
System on chips (SoCs), 100, 138, 376
Systems, 157

T
Tape-out, 270
Taper, 119, 124, 127, 131, 135
TDWS, 85, 91
TEC, 460
Technology, 258
Technology platform, 280
Telecommunication applications, 403
TE mode, 89
Temperature-dependent wavelength shift, 83, 84
Temperature sensitive, 391
Temporal locality, 174
Testbed, 177
Test chip strategy, 285
Test-site, 271
Thermal fluctuations, 163
Thermal impedance, 384

Thermal initialization latencies, 173
Thermal management, 218, 229
Thermal shunt approach, 506
Thermal stabilization, 165
Thermal-stresses, 221
Thermal tuning schemes, 498
Thermo-electric cooler TEC, 460
The time to failure, 209
Three-dimensional (3-D) packaging, 2
Through glass vias, 33
Through-silicon vias, 492
Tiling, 272
Titania, 86, 93, 95
Titania cladding, 95
TM mode, 89
TO-cans, 368
TO coefficient (TOC), 84, 85, 93, 95
TO material, 86
Transceiver, 114, 116, 144, 162
Transceiver microsystem, 377
Transfer function, 319
Transfer response, 342
Trans-impedance amplifier (TIA), 28, 364, 500
Transmission losses, 384
Transmit, 167
Transponder aggregators (TPAs), 435
Trident, 11
Two-photon absorption laser lithography technology, 253
Two-tone test signals, 332

U
Uncooled photonic circuits, 385
Using diffraction via gratings, 239

V
Validation, 158
Verilog-A, 101, 109, 112
Vertical-cavity surface-emitting lasers (VCSEL), 120, 350
Vertically coupling, 399
Very large-scale integration (VLSI), 100

W
Wafer, 269
Wafer acceptance test, 359
Wafer level, 248
Wafer-level optical testing, 289
Wafer-level testing, 205, 399
Wall plug efficiency, 10, 379
Warehouse scale computer, 474
Waveguide photodetector, 356
Wavelength division multiplexing (WDM), 32, 106, 158, 161, 425, 490
Wavelength filters, 83
Wavelength locking, 164
Wavelength profiles, 184
Wavelength routing, 164
Wavelength selective routing, 161
Wavelength selective switches, 35
Wavelength selectivity, 163
WDM ring networks, 423
Wirebonding, 160
Wiring parasitic loading, 408

Y
Yield, 273