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Ahmed G. Radwan
Mohammed E. Fouda

On the Mathematical Modeling of Memristor, Memcapacitor, and Meminductor

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To my beloved parents, my professor (A.M. Soliman), my wife, and my children Yousef, Yasmin & Nada

—Ahmed G. Radwan

To my beloved parents, brother and sisters for their love, endless support, and encouragement

—Mohammed E. Fouda

Foreword

Among the numerous books and monographs published so far on the memristor, memcapacitor, and meminductor, the Radwan-Fouda book stands out as the most comprehensive, scholarly, and timely. The book has both depth and breadth—it covers practically all aspects of memory circuit elements that have been published in the literature, including important contributions from the authors themselves. Each chapter is carefully organized, well-illustrated, and written pedagogically so even the uninitiated will find it to be eminently readable. The references are comprehensive and surprisingly up-to-date, including some obscure papers, and several future papers that have not yet seen the light of day. Every serious researcher on memristors, memcapacitor, and meminductors will find this book indispensable.

USA Leon Chua
February 2015

Preface

Due to the huge challenges in the continuous scaling of technology, there is a need to search for alternatives that are compatible with CMOS and can provide high performance in nanoscale dimension, especially in memories due to the enormous data storage required for many applications. Memristor-based technology offers a feasible solution for post-CMOS memories and reconfigurable analog modules, which are essential in modern electronics and systems-on-chip (SOC). The history of memristor goes back to 1971 and 1976 when L. Chua, the father of nonlinear circuits, postulated the existence of passive circuit elements and their promising applications. Recently in 2008, HP Lab recognized practically the first memristor based on nanoscale titanium dioxide films though their Nature paper. Thus, mem-elements such as memristor, memcapacitor, and meminductor have become very vital components in many applications, due to their unique behaviors which cannot be obtained using other conventional elements, so modeling of these elements has become necessary.

This book tries to study the modeling and analysis of these elements in analog and digital designs as well as their new fundamentals in the circuit theory. The literature survey includes the main properties of memristor, mathematical representations (ideal, generic, and extended), physical models, types, and some applications. A generalized mathematical class of mem-elements are discussed and validated through different emulator circuits with experimental results. The concept of fractional-order elements have been extended to cover the memristor model with its basic characteristics such as step and sinusoidal responses.

Memristor-based oscillators are considered one of the nonlinear analog blocks required for many applications such as chaotic memristor oscillators and artificial neuron networks. Realizations of memristor-based oscillators have been discussed via replacing resistors with memristors to achieve oscillation, or by replacing capacitors with memristors to construct relaxation reactance-less oscillators. The advantages of such oscillators are related to low frequency, nanoscale, and simple designs and can be used in neuromorphic systems. Different topologies of memristor-based relaxation oscillators have been discussed, either symmetric or asymmetric types, with analytical formulas of oscillation frequency and conditions for

oscillations derived. The analyses of these oscillators are introduced with their numerical simulations, and verified using PSPICE circuit simulations showing great matching. Moreover, many fundamentals are also discussed such as the effect of boundary dynamics, series and parallel connections, as well as power analysis in memristor-based circuits.

Recently, there are huge concerns regarding memristors in digital signal processing (DSP) circuits to enhance the performance and realize very high density nonvolatile memories in neural networks. This can be achieved by mapping the high/low logic into the memristors' high/low resistances. Recently, the potential to divide the memristance levels to build multilevel digital circuits, such as ternary and redundant circuits, are discussed. The concepts have been initiated by designing a half-ternary adder based on the memristor, then the concept is generalized for redundant half adder, full adder, and N-bit adder circuits. The advantages of such circuits is that the speed is independent on the operand, and parallel processing can be handled efficiently. Moreover, a general approach to build digital functions using mixed memristor-transistor circuits are investigated, such as multipliers.

Similarly, the basic definitions of memcapacitor and meminductor are introduced with their step response with the settling time formulas, sinusoidal response, power and energy calculations, and the effect of boundary dynamics. Then, the boundary dynamics under sinusoidal excitations are used as bases to analyze any periodic signal by Fourier series expansion. Moreover, the analytical analyses of series and parallel connections as well as resistive-less memcapacitor-based relaxation oscillator are discussed with closed-form expressions for oscillation frequency and conditions for oscillation. Different memcapacitor and meminductor emulators are summarized with their mathematical modeling, numerical simulation, and verified using PSPICE simulations.

Giza
February 2015

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Mohammed E. Fouda

Acknowledgment

The authors thank Prof. Leon Chua (the father of nonlinear circuit theory) for his kindness and for his useful and fruitful comments on the book.

Contents

Authors Biography

Ahmed G. Radwan (M'96–SM'12) received the B.Sc. degree in Electronics, and the M.Sc. and Ph.D. degrees in Eng. Mathematics from Cairo University, Egypt, in 1997, 2002, and 2006, respectively. He is an Associate Professor, Faculty of Engineering, Cairo University, and also with the Nanoelectronics Integrated Systems Center, Nile University, Egypt. From 2008 to 2009, he was a Visiting Professor in the ECE Dept., McMaster University, Canada. From 2009 to 2012, he was with King Abdullah University of Science and Technology (KAUST), Saudi Arabia. His research interests include chaotic, fractional order, and memristor-based systems. He is the author of more than 140 international papers, six US patents, three books, two chapters, and h-index=19.

Dr. Radwan was awarded the Egyptian Government first-class medal for achievements in the field of Mathematical Sciences in 2012, the Cairo University achievements award for research in the Engineering Sciences in 2013, and the Physical Sciences award in the 2013 International Publishing Competition by Misr El-Khair Institution. He won the best paper awards in many international conferences as well as the best thesis award from the Faculty of Engineering, Cairo University. He was selected to be among the first scientific council of Egyptian Young Academy of Sciences (EYAS) in 2014, and also the first scientific council of the Egyptian Center for the Advancement of Science, Technology and Innovation (ECASTI) in 2014.

Mohammed E. Fouda received the B.Sc. degree (honors), in Electronics and Electrical Communications Engineering and the M.Sc in Engineering Mathematics from Faculty of Engineering, Cairo University, Giza, Egypt in 2011 and 2014 respectively. He is an assistant lecturer, Faculty of Engineering, Cairo University, Egypt. His research interests include Mem-element-based Circuits and Analog Circuits. He has authored and co-authored more than 20 journal and conference papers. Fouda won the physical sciences award from Misr El-Khair Institution for international publishing in 2013. Also, He won the best paper award in ICM 2013 in Lebanon.

Acronyms

φ	Flux
ω	Angular frequency
BIBO	Bounded Input Bounded Output
C	Capacitor
CCCS	Current-Controlled Current Source
CCII	Second Generation Current Conveyor
CCVS	Current-Controlled Voltage Source
CLA	Carry-Look-Ahead Adder
CMOS	Complementary Metal–Oxide Semiconductor
CPPLL	Charge Pump Phase Locked Loop
CSDC	Canonic Signed Digit Code
CSDRBA	Canonic Signed Digital Redundant Binary Adder
DDCC	Differential Difference Current Conveyor
f	Frequency
FERAM	Ferroelectric Random Access memory
FF	Flip Flop
FOC	Fractional-order Capacitor
FOI	Fractional-order Inductor
FOM	Fractional-order Memristor
FOMC	Fractional-order Memcapacitor
FOMI	Fractional-order Meminductor
FPGA	Field Programmable Gate Array
G_m	Transconductance
GIC	General Impedance Converter
HP	Hewlett-Packard
i	Current
IMP	Imply
KCL	Kirchhoffs Current Law
KVL	Kirchhoffs Voltage Law
L	Inductor or Coil
LDR	Light-Dependent Resistor
LUT	Look Up Table

M	Memristor
MC	Memcapacitor
ML	Meminductor
MOS	Metal–Oxide Semiconductor
MRAM	Magnetic Random Access memory
p	Power
PFD	Phase Frequency Detector
PPL	Phase Locked Loop
PSPICE	Personal Computer Simulation Program with Integrated Circuit Emphasis
PWL	Piece-Wise Linear
PWM	Pulse-Width Modulation
q	Charge
R	Resistor
R/W	Read/Write
RCA	Ripple-Carry Adder
RRAM	Resistive Random Access Memory
SDC	Signed Digit Code
SRAM	Static Random Access Memory
STDP	Spike-timing-dependent plasticity
TSMC	Taiwan Semiconductor Manufacturing Company
U	Energy
v	Voltage
V_{th}	Threshold Voltage
VCCS	Voltage-Controlled Current Source
VCO	Voltage Controlled Oscillator
VCR	Voltage Controlled Resistor
VCVS	Voltage-Controlled Voltage Source

Chapter 1
Introduction

Before 1971, Only nine types of two-terminal (five passive and four active) elements were required to model any electrical component or circuit. Each element was defined by a relation between the state variables of the network: current I, voltage V, charge Q, and flux φ. Although there is another classification depending on linearity of the element, in reality, all circuit components are nonlinear and can only be approximated to linear within a certain range. In this chapter, we present a brief review of linear one-port passive elements followed by a presentation of the layout for this book.

1.1 Review of Basic Linear Circuit Elements

There are two types of elements found in electric circuits: passive elements and active elements. An active element is capable of generating energy, while a passive element is not. Examples of passive elements are resistor, capacitor, inductor, transformer, and gyrator. Examples of typical active elements are VCVS, VCCS, CCCS, and CCVS. In the following sections a brief introduction to passive elements is given, but for more details, see [1].

1.1.1 Resistor

Materials in general have a characteristic behavior of resisting the flow of electric charge. This physical property, or the ability to resist current, is known as resistance and is represented by the symbol R which is the proportionality constant between voltage and current. Georg Simon Ohm (1787–1854), a German physicist, is credited with finding the relationship between current and voltage for a resistor. This relationship is known as Ohm's law.

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$$v = iR. \tag{1.1}$$

The resistance R can be measured in the lab as follows:

$$R = \rho \frac{L}{A}, \tag{1.2}$$

where ρ is known as the resistivity of the material in ohm-meters, A is the cross-sectional area, and L is the length. The power consumption on the resistance is given as

$$P = iv = i^2 R = v^2/R. \tag{1.3}$$

1.1.2 Capacitor

A capacitor is a passive element designed to store energy in its electric field. Capacitors are used extensively in electronics, communications, computers, and power systems. They are used in the tuning circuits of radio receivers and as dynamic memory elements in computer systems.

When a voltage source is connected to the capacitor, the source deposits a positive charge q on one plate and a negative charge on the other. The capacitor is said to store the electric charge. The amount of charge stored, represented as q, is directly proportional to the applied voltage by:

$$q = Cv, \tag{1.4}$$

where C, the constant of proportionality, is known as the capacitance of the capacitor. The unit of capacitance is the Farad (F), in honor of the English physicist Michael Faraday (1791–1867). Although the capacitance C of a capacitor is the ratio of the charge q per plate to the applied voltage v, it does not depend on q or v. The capacitance depends on the physical dimensions of the capacitor and is given as

$$C = \frac{\varepsilon A}{d}, \tag{1.5}$$

where A is the surface area of each plate, d is the distance between the plates, and ε is the permittivity of the dielectric material between the plates. The current–voltage relation of the capacitor is given as

$$i = C \frac{dv}{dt}. \tag{1.6}$$

The instantaneous power delivered to the capacitor is calculated as

$$p = iv = Cv\frac{dv}{dt}. \tag{1.7}$$

Therefore, the energy stored in the capacitor is given as

$$w(t) = \int_{-\infty}^{t} p(\tau)d\tau = \frac{1}{2}C\Big(v^2(t) - v^2(-\infty)\Big). \tag{1.8}$$

We note that $v(-\infty) = 0$, because the capacitor was uncharged at $t = -\infty$. Thus,

$$U(t) = \frac{1}{2}Cv^2(t) = \frac{q^2}{2C}. \tag{1.9}$$

1.1.3 Inductor

An inductor is a passive element designed to store energy in its magnetic field. Inductors find numerous applications in electronic and power systems. They are used in power supplies, transformers, radios, TVs, radars, and electric motors.

The voltage across the inductor is linearly proportional to the rate of change of current as

$$v = L\frac{di}{dt}, \tag{1.10}$$

where L is the constant of proportionality called the inductance of the inductor. The unit of inductance is the henry (H), named in honor of the American inventor Joseph Henry (1797–1878).

The inductance of an inductor depends on its physical dimension and construction. Formulas for calculating the inductance of inductors of different shapes are derived from the electromagnetic theory and can be found in standard electrical engineering handbooks. For example, the inductance of al solenoid is calculated as

$$L = \frac{N^2\mu A}{l}, \tag{1.11}$$

where N is the number of turns, l is the length, A is the cross-sectional area, and μ is the permeability of the core. The current–voltage relationship is obtained as

$$i = \frac{1}{L}\int_{-\infty}^{t} v(\tau)d\tau. \tag{1.12}$$

The inductor is designed to store energy in its magnetic field. The power delivered on the inductor as a function of the current is

$$p = vi = \left(L\frac{di}{dt}\right)i. \tag{1.13}$$

Therefore, the energy stored is given as

$$U = L\int_{i(-\infty)}^{i}(t)idi = \frac{1}{2}Li^2(t) - \frac{1}{2}Li^2(-\infty). \tag{1.14}$$

which will tend to $w = \frac{1}{2}Li^2(t)$ since $i(-\infty) = 0$.

1.1.4 Fractional-Order Elements

Integer calculus is considered as a very narrow subset of the fractional-order calculus. Therefore, the integer elements were also extended to the fractional-order elements for better modeling and interpretations of many physical phenomena. For example, the integer capacitor has 90° phase difference between the voltage and the current, while the fractional-order capacitor has $90\alpha°$ phase difference. It is clear that at the special case $\alpha = 1$, the fractional-order capacitor acts as an integer capacitor. Therefore, the extra degree of freedom α in the fractional-order capacitor increases the design flexibility and enhances the system's design. A brief introduction to the basic definition, realizations, and some applications of the fractional-order elements are discussed in the following sections.

1.1.4.1 Fractional Calculus and Its Applications

The history of fractional calculus dates back to 1695 with the work of scientists such as L'Hospital and Leibniz, though the first logic definitions were proposed by Liouville in 1834, Riemann in 1847, and Grunwald in 1867 [2, 3]. Fractional calculus can be considered as a superset of integer-order calculus, which has the potential to accomplish what integer-order calculus cannot. The first approximation of the fractional-order derivative in terms of a complicated system of integer orders was proposed in 1964 [4], but this approximation was good only in a certain band of frequencies. Furthermore, different realizations of the fractional elements were introduced during the past few years [5–8] using different techniques. The theory of fractional-order elements comes from the frequency-dependent losses in the conventional elements as proved recently in [9, 10]. Many books and researches during the past three decades have aimed to increase the accessibility of fractional calculus for remodeling most of the existing applications and analyzing new models in basic natural sciences. For example, many papers recently have tried to model the

electrical impedance of vegetables and fruits into simple electrical circuit connections using a single fractional capacitor [11, 12]. Generally, the fingerprints of the applied fractional calculus could be built up to include many physical phenomena based on differentiation and integration [13]. Various numerical techniques were introduced to solve linear and nonlinear fractional-order differential equations (FODEs) [14, 15], which model different physical problems.

Fractional calculus depends on the history of the function, which is more realistic and suitable for modeling, analyzing, and synthesizing and for solving many problems in bioengineering [16–18]. Thus different biomedical models can be represented by simple connections of fractional circuit elements [19]. The existence of an extra degree of freedom in the fractional order makes its performance always superior to that of the traditional integer calculus, which can be used to describe the behavior of complex systems and materials. Moreover, modeling with fractional calculus is used to extract more generalized information and fundamentals [20–23]. In addition, the output can be optimized to be closer to the experimental results by adjusting the extra parameters and using a suitable optimization technique.

From the circuit perspective, the general theorems related to linear oscillators have been recently generalized to the fractional-order case, beginning with mathematical proofs, through circuit simulations, and ending with experimental results [24, 25]. A main basis in most of these generalizations is that the frequency of oscillation for using fractional elements of order α, is proportional to $\omega_{o1}^{1/\alpha}$ where ω_{o1} is the frequency of oscillation in the case of integer elements and if $\alpha = 0.5$ (order one half), the oscillation frequency increases by a power of 2, which is required for many high frequency applications. Also, the generalizations of filter theorems are studied for one or two fractional elements of the same orders showing new fundamentals and features rather than those of known filters [26–28].

1.1.4.2 Basic Definition of Fractional Capacitor

The most important definition of the fractional derivative was introduced by Caputo [3] which is denoted by (1.15). If $\alpha = 1.2$, then $m = 2$, so the fractional derivative of order 1.2 is equivalent to an integer derivative of order 2 followed by a fractional integral of order 0.8.

$$ {}_aD_t^{\alpha} f(t) := \begin{cases} \frac{1}{\Gamma(m-a)} \int_a^t \frac{f^{(m)}(\tau)}{(t-\tau)^{\alpha+1-m}} d\tau & (m-1) < \alpha < m \\ \frac{d^m}{dt^m} f(t) & \alpha = m \end{cases} \tag{1.15} $$

There are many numerical approximations for the above definition; the most important one is driven as in (1.16) by Grünwald-Letnikov [29]. In this definition Γ and h are the gamma function and the step size, respectively. It is clear that the summation takes into account all previous values of $f(t)$ which cover all the historical background of the function. When $\alpha = 1$, all items inside the summation will be zero except for $m = 0, 1$, which will be reduced to the traditional backward difference formula

$$ {}_aD_t^{\alpha} f(t) = \lim_{h \to 0} \frac{1}{h^{\alpha} \Gamma(-\alpha)} \sum_{m=0}^{\frac{t-a}{h}} \frac{\Gamma(m-\alpha)}{m!} f(t-mh) \tag{1.16} $$

Another advantage of the fractional derivative comes from the Laplace transform of the fractional derivative, for example, $L\{{}_aD_t^{\alpha} f(t)\} = F(s)/s^{\alpha}$, which is equivalent to the relation between the current and voltage across the fractional-order capacitor $V(s) = I(s)/(C_f s^{\alpha})$, where C_f is the value of the fractional capacitor. Then the phase difference between the current and voltage will be $\alpha\pi/2$. In the case of integer order of the capacitor ($\alpha = 1$), the general case returns to the well-known phase difference $\pi/2$.

1.1.4.3 Realization of Fractional Elements

The modeling of fractional-order systems (e.g., the fractional capacitor) was discussed during the previous three decades from different points of view. The mathematical approximation of the equivalent transfer function (1/s) to higher integer order within a certain region of frequencies, passing through its realization using many branches of resistors and capacitors whose values are related to certain factors, where $0 < \alpha < 1$, is shown in Fig. 1.1a [8], or a tree shape of equal values can be used to realize the half-order fractional element as shown in Fig. 1.1b [30]. Other realizations of fractional elements using chemical reactions between different materials are discussed in [30–32]. All these realizations were a good approximation for the fractional element within a certain range of frequencies. Moreover, a new half-order capacitor based on fractal structures was introduced in [33, 34].

In the near future, if scientists are able to realize a wide band fractional capacitor of order α where $0 < \alpha < 1$ only, this will be enough to obtain the full range of α as follows:

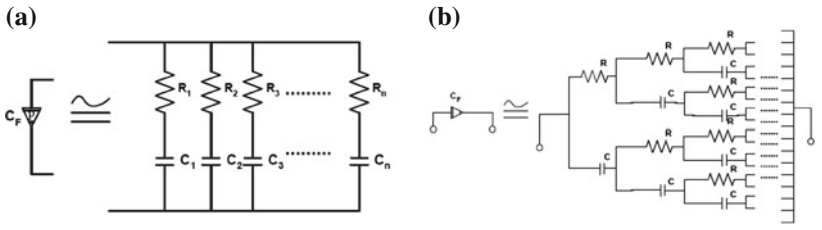

Fig. 1.1 Floating fractional-order capacitor realizations

- A fractional capacitor of order $1 < \alpha \leq 2$ can be obtained through the use of a general impedance converter (GIC) whose input impedance is given by $Z_{in} = Z_1 Z_2 Z_3/(Z_4 Z_5)$.
- A fractional inductor of order $0 < \beta \leq 2$ can be realized by using the well-known gyrator circuit whose input impedance is inversely proportional to Z_L. So if Z_L is a fractional capacitor of order β, the input impedance of the gyrator acts as a fractional inductor of the same order.

1.2 Memristor

Professor Leon Chua noted that there are four different mathematical relations connecting pairs of the four fundamental circuit variables current i, voltage v, charge q, and flux φ. The relation between these variables is deduced from Faraday's law of induction. A resistor is defined by the relationship between voltage v and current i ($dv = Rdi$), the capacitor is defined by the relationship between charge q and voltage v ($dq = Cdv$), and the inductor is defined by the relationship between flux φ and current i ($d\varphi = Ldi$). In addition, the current i is defined as the time derivative of the charge q and according to Faraday's law, the voltage v is defined as the time derivative of the flux φ. This relation is shown in Fig. 1.2a.

Leon Chua compared the above model to that of Aristotle's theory of matter. According to this theory all matter consists of earth, water, air, and fire. Each of these elements exhibits two of the four fundamental properties of moistness, dryness, coldness, and hotness. This is shown in Fig. 1.2b [35]. Thus, depending on the above theory he saw a striking resemblance and predicted the existence of the fourth kind of element and called it memristor.

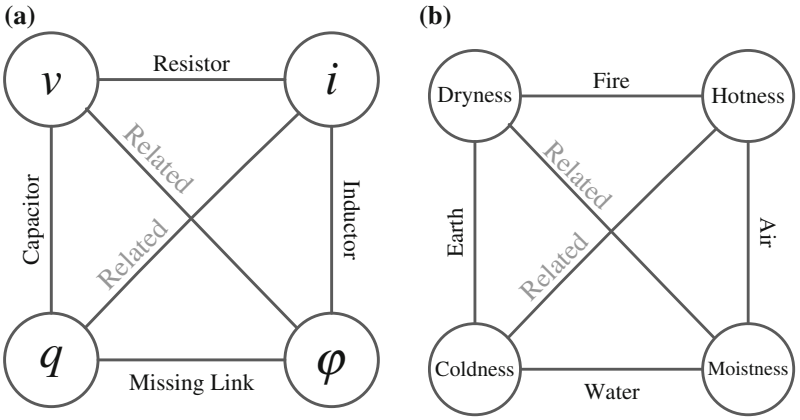

Fig. 1.2 **a** The relation between the circuit elements, and **b** Aristotle's theory of matter

1.3 Historical Background of the Mem-Element

The hypothesis of the presence of a resistor with memory concept existed even before Prof. Chua postulated its existence in a seminal paper in 1971 [36]. Indeed, the first man-made memristor dates back to 1801 [37].

In 1960, Prof. Bernard Widrow of Stanford University developed a new circuit element called the memistor. The memistor was a three-terminal device for which the conductance between two of the terminals was controlled by the time-integral of the current into the third terminal. Thus, the resistance of the memistor was controlled by charge. Memistors formed the basic components of the neural-network architecture called ADALINE (ADAptive LInear NEuron) [38]. Later, it was proved that the memistor and memristor are different devices [39]. In fact, Widrow's memistor is a gadget, not a circuit element.

In 1968, F. Argall published a paper, "Switching phenomena in titanium oxide thin films" [40], which shows results similar to that of the memristor model proposed by Stanley Williams and his team later on.

In 1971, Leon Chua mathematically predicted [36] that there is a fourth fundamental circuit element characterized by a relationship between charge and flux linkage.

In 1976, Leon Chua and Sung Mo Kang published a paper entitled "Memristive devices and systems" [41], generalizing the theory of memristors and memristive systems, including a property of zero crossing in the Lissajous curve characterizing current versus voltage behavior.

In 1980, Chua generalized his theory to higher-order nonlinear elements and presented two basic approches to device modeling [42]. Moreover, Chua introduced the general element which can represent the circuit elements.

In 1990, S. Thakoor et al. demonstrated a tungsten-oxide variable-resistance device that is electrically reprogrammable [43].

Four years later, in 1994, Buot and Rajgopal published an article entitled "Binary information storage at zero bias in quantum-well diodes" [44]. The article described current voltage characteristics similar to that of the memristor in AlAs/GaAs/AlAs quantum-well diodes.

In 2000, Beck et al. of IBMs Zurich Research Laboratory, described reproducible resistance switching effects in thin oxide films [45]. The hysteretic features of these switches are similar to those of the memristor.

Apart from the devices mentioned above, it is interesting to note that between 1994 and 2008 there were many other devices developed with behavior similar to that of the memristor, but only the HP scientists were successful in finding a link between their work and the memristor postulated by Chua.

In 2007, two U.S. patents were issued. It described implementations of two-terminal resistance switches similar to memristors in reconfigurable computing architectures, signal processing, and pattern recognition.

In 2008, the memristor in device form was developed by Stanley Williams and his group in the Information and Quantum Systems (IQS) Lab at HP. Dmitri Strukov, Gregory Snider, Duncan Stewart, and Stanley Williams, of HP Labs, published an article identifying a link between the two-terminal resistance switching behavior found in nanoscale systems and Leon Chua's memristor [46]. However, Victor Erokhin and M.P. Fontana claimed to have developed a polymeric memristor before the titanium-dioxide memristor developed by Stanley Williams' group [47]. In April 2008, a U.S. patent including basic claims to a nanoscale two-terminal resistance switch crossbar array formed as a neural network [48] was issued, and in August, a U.S. patent including claims covering the device described in the Nature article [49] was issued. Moreover, in October, the U.S. patent including basic claims to a tunable nanoscale two-terminal resistance switch [50] was issued.

Since the announcement of the breakthrough by Stanley Williams' group, numerous papers with the aim to analyze the elementary attributes of the memristor have been published as shown in Fig. 1.3. Moreover, different publications introduce memristor fabrication, models, and applications as will be discussed in the next section.

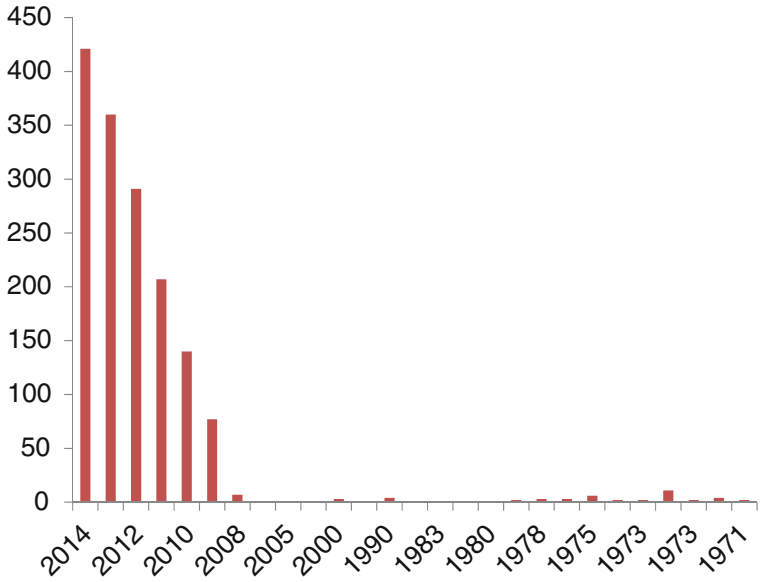

Fig. 1.3 Memristor and memristive publications adopted from Engineering Village (December 2014)

1.4 Organization of the Book

This book includes seven chapters and is organized as follows:

Chapter 2 gives a review of the memristor: theory, mathematical representations, phyiscal models, and applications.

Chapter 3 investigates two models for double-loop hysteresis behavior of the mem-elements which are based on very simple dimensionless equations and then show how physical voltage- and current-controlled memristor models can be derived. Moreover, the HP model is generalized to the fractional-order domain. The effect of the added fractional-order parameter on the memristor characteristics and output behavior are introduced. Due to the lack of memristor samples, the emulators are very useful to be used instead of memristor samples. The incremental/decremental, positive/negative, and memristance/memductance are introduced and their tunable circuit emulators are presented which are capable of emulating these devices. Moreover, their mathematical models are derived. Experimental results are given.

Chapter 4 introduces memristive oscillators which are a novel topic in nonlinear circuit theory, where the behavior of the reactive elements is emulated by the memristor. The mathematical analyses of different memristor-based reactance-less oscillators are introduced, for example, a memristor-based voltage-controlled oscillator is introduced with two different topologies in addition to the effect of the boundary of the memristor on this oscillator. New symmetric and asymmetric memristive two-gate relaxation oscillators are introduced. The generalized analysis for the proposed memristive two-gate oscillator is introduced, and four special cases for different mismatching of the memristors are introduced. The oscillation frequency, duty cycle, and condition for oscillations expressions are derived for all proposed oscillator circuits. These circuits are verified using PSPICE and numerical simulations showing great matching. In addition, the power consumption in two series memristor is calculated to assist in calculating the power consumed in the oscillators.

Chapter 5 highlights the potential of memristor in binary and multilevel digital circuits. First, a ternary half adder circuit is introduced to address the concept of multilevel circuit based on the memristor. Then, a complete case study for redundant half adder, full adder, and N-bit adder circuit based on the memristor analyzed to build an adder that has speed independent on the operand showing the potential of this element in arithmetic circuit is given. Moreover, a new approach to build digital circuit using the memristor is introduced based on replacing the complete pull-down network with one memristor to work as calculating/saving element to decreasing the number of transistors. An example to implement redundant multiplier circuit based on this approach is then introduced. All these circuits are verified using PSPICE simulations.

Chapter 6 discusses the boundary dynamics of charge controlled memcapacitor for Joglekar's window function, which describes the nonlinearities of the memcapacitor's boundaries. The derived formulas are used to predict the behavior of the memcapacitor under different voltage excitation sources showing great matching with the circuit simulations. The boundary dynamics under sinusoidal excitation

are used as bases to analyze any periodic signal by Fourier series. Moreover, the analytical analysis of two memcapacitors connected in series and in parallel taking into consideration the effect of mismatch in mobility factor and polarity of each one is given. Also, a new memcapacitor emulator without using any memristor is introduced with its mathematical modeling and numerical simulation, and verified using PSPICE simulations. In addition, the power and energy in memcapacitor is calculated.

Chapter 7 introduces different applications based on memcapacitor. Focusing on two main applications; (1) resistive-less memcapacitor-based relaxation oscillator where closed-form expressions for oscillation frequency and conditions for oscillation are derived and two special cases are discussed in detail. Moreover, the effect of boundary on the relaxation oscillator is introduced. (2) Memcapacitor-based synapse circuit is discussed. All the results have been verified using PSPICE simulations showing good matching.

Chapter 8 analyzes the current controlled meminductor under different current excitation signals: DC, sinusoidal, and periodic current signals. The proposed analysis offers closed-form expressions for the meminductance for each case. A general closed-form expression for the meminductance is derived under any periodic waveform and this formula has been validated by applying a square wave as an example. The power and energy of meminductor are also calculated. Furthermore, meminductor emulators are developed to fit the obtained formulas, which are built using commercial off-the-shelf components.

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Chapter 2
Memristor: Models, Types, and Applications

2.1 The Missing Element History

The first concept and realization of memory resistor device was proposed by Widrow in 1960 [1]. It was named memistor and had three terminals. The resistance of this memistor was variable and could be controlled and sensed using the control (DC current) and sensing (AC current) terminals. The significant difference between the transistor and the memistor is that the memistor resistance is controlled by the instantaneous time integral of the control current, which is the accumulated charge passing through the memistor. However, the memistor was not linked to the fundamentals of circuit theory because it is an "ill-posed" element, a 3-terminal device is said to be well posed if it has sufficient information to predict the current and voltage associated with all the three terminals when the device is connected to an arbitrary external circuit [2]. Moreover, in 1968, through the Electromagnetic theory, Fano et al. listed that there are four fundamental circuit elements: resistor, capacitor, inductor, and an unknown element [3].

However, the first practical mathematical concept and realization was introduced by the father of nonlinear circuits, Prof. Leon Chua, in 1971 in his seminal paper [4]. It is well known that the four main fundamental circuit variables are current, i, voltage, V, charge, q, and flux, φ. For linear elements, $f(V, i) = 0$, $f(V, q) = 0$ where $i = dq/dt$, and $f(\varphi, i) = 0$ where $V = d\varphi/dt$, which represent the linear resistor ($v = iR$), the capacitor ($q = CV$), and the inductor ($\varphi = Li$), respectively. Chua predicted mathematically that there is a device representing the missing relation characterized by $g(\varphi, q) = 0$ which he named the memristor. Moreover, he presented an electromagnetic interpretation of the memristor characteristics [4]. Also Chua defined two types of memristors; charge-controlled and flux-controlled based on their memristance relation. They are called charge-controlled and flux-controlled memristor, when the memristance relation is a single-valued function of the charge

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q or flux linkage φ, respectively. The voltage across a charge-controlled memristor is given by:

$$v(t) = M(q(t))i(t) \tag{2.1a}$$
$$M(q) = d\varphi(q)/dq \tag{2.1b}$$

Similarly, the current of a flux-controlled memristor is given by:

$$i(t) = W(\varphi(t))v(t) \tag{2.2a}$$
$$W(\varphi) = dq(\varphi)/d\varphi \tag{2.2b}$$

where $M(q)$ and $W(q)$ have units of resistance (Ω) and conductance ($\mho$). The instantaneous power dissipated by the memristor is given by

$$p(t) = M(q(t))i^2(t) \quad \text{or} \quad p(t) = W(\varphi(t))v^2(t) \tag{2.3}$$

Five years after the Chua's first paper on the memristor, Chua and his student, at this time, Kang published a paper and defined a wider class of systems called memristive systems in 1976 [5]. In this paper, they proposed a generic equation to describe the memristive devices and systems. This equation is

$$y = g(x, u, t)u \tag{2.4a}$$
$$\frac{dx}{dt} = f(x, u, t) \tag{2.4b}$$

where x is the state variable, u and y are the input and the output of the system, respectively, f is a continuous n-dimensional function and g is a continuous scalar function. This special structure was proposed to distinguish between memristive systems and dynamical systems.

2.2 HP Memristor

Since Chua postulated the existence of the memristor, scientists were observing pinched hysteresis characteristics in different materials and structures besides reporting the current–voltage characteristics. Until 2008, when HP Labs announced that they found the missing element and published their findings in Nature [6]. In addition, the HP team introduced the first basic model of memristor which is governed by the mathematical formulation of Chua's memristive systems [5, 6].

The HP memristor was built based on titanium dioxide, which is a stable compound. The memristor structure is composed of two chemically different layers; TiO_2

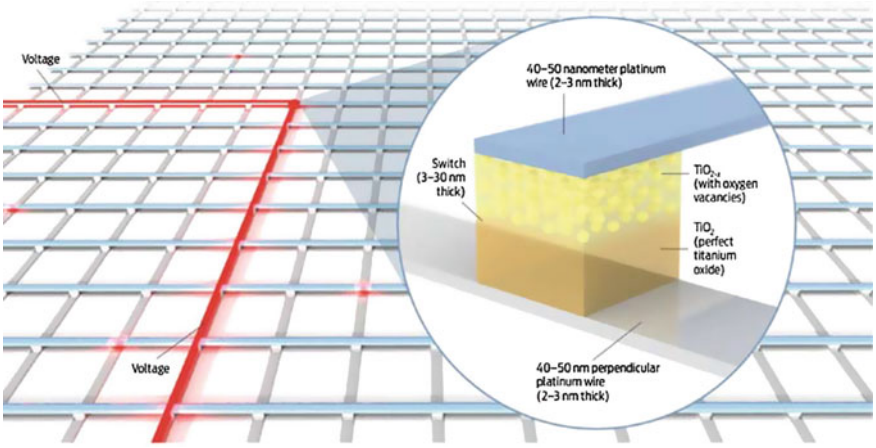


Fig. 2.1 How HP memristor works (adopted from [8])

(high impedance) adjacent to the molecules, and closer to the top platinum electrode, the titanium dioxide was missing around 2.5 % of its oxygen which is called oxygen-deficient titanium dioxide TiO_2 (conductive) [7, 8]. The oxygen vacancies are donors of electrons, so the vacancies are positively charged as shown in Fig. 2.1. When applying a positive voltage to the top electrode of the device, it will repel the oxygen vacancies in the TiO_2 layer (doped region) down into the pure TiO_2 layer (undoped region). Transferring the oxygen vacancies from the TiO_{2-x} layer to TiO_2 layer which increases the width of TiO_{2-x} layer and decreases the width of TiO_2. But, applying a negative voltage has the opposite effect where the oxygen vacancies are attracted to the electrode making the undoped layer wider and decreases the doped layer.

According to the previous description, the HP team presented a mathematical model for their memristor. This model is based on two series resistors R_{on} and R_{off} where R_{on} and R_{off} are the doped and the undoped region resistances. It is assumed that the physical device is of width, D, and the doped region of width, w, as shown in Fig. 2.2. Note that the doped region with width, w, is the state variable which changes depending on the charge [6].

$$M(t) = R_{on}\frac{w(t)}{D} + R_{off}\left(1 - \frac{w(t)}{D}\right) \tag{2.5a}$$

$$\frac{dw}{dt} = \frac{\mu_v R_{on}}{D} i(t) \tag{2.5b}$$

where μ_v is the average ion mobility.

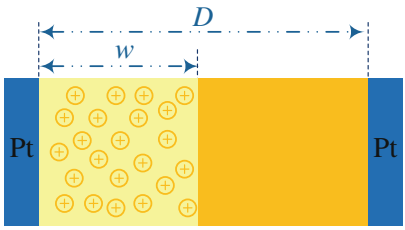


Fig. 2.2 HP memristor model

2.3 Basic Memristor Fingerprints

There are three characteristic fingerprints, memristors should exhibit [9, 10]:

- The device must exhibit a pinched hysteresis loop in the voltage–current plane for any bipolar periodic signal excitation as Chua said "If it is pinched, it is a memristor" [11].
- The pinched hysteresis lobe area should decrease monotonically as the excitation frequency increases.
- The pinched hysteresis loop should shrink to a single-valued function when the frequency tends to infinity.

2.4 Memristor Models

This element is very important due to its potential in life applications, thus it should be properly modeled in order to be used in the analysis, design, and simulation of memristor-based circuits. In 2008, the first practical model was described by HP Labs in [6], then later several models were proposed. In this section a brief summary is presented.

2.4.1 Linear Ion Drift Model

The year 2008 witnessed the solid-state memristor existence by the HP Labs team [6]. Strukov et al. published their results that described the memristor device in which the pinched hysteresis existed between the current and the voltage, described as illustrated in the second row of Table 2.1. The actual memristance is dependent on the ratio between the value of the dynamic state variable $w(t)$, representing the thickness of the oxygen-deficient titanium dioxide layer (TiO_{2x}) and the device thickness D. Strukov et al. included some basic equations for an ideal model of the memristor, where this model assumes that the vacancies have freedom to move around the entire length of the device. But it is not true, since vacancies slow down a lot at the boundary because if they move through the entire device, it means that there will be no physical

Table 2.1 Mathematical equations of memristor's models

Model	Current–voltage relation	State variable derivative
Linear ion drift	$v(t) = \left(R_{on}\frac{w(t)}{D} + R_{off}(1 - \frac{w(t)}{D})\right) i(t)$	$\frac{dw(t)}{dt} = \frac{\mu_v R_{on}}{D} i(t)$
Nonlinear ion drift	$i(t) = w^n(t)\beta sinh(\alpha v(t)) + \chi[exp(\gamma v(t)) - 1]$	$\frac{dw(t)}{dt} = a v^m(t) f(w)$
Simmons tunneling barrier	$i(t) = \tilde{A}(x, v_g)\phi_1(v_g, x) \times exp\left(-B(v_g, x) \cdot \phi_1^{0.5}(v_g, x)\right) - \tilde{A}(x, v_g)\left(\phi_1(v_g, x) + e\lvert v_g\rvert\right) \times exp(B(v_g, x)(\phi_1(v_g, x) + e v_g)^{0.5})$ $v_g = v - i(t)R_s$	$\frac{dx(t)}{dt} =$ $\begin{cases} c_{off} sinh(\frac{i}{i_{off}}) exp[-exp(\frac{x - a_{off}}{w_c} - \frac{\lvert i\rvert}{b}) - \frac{x}{w_c}] & i > 0 \\ c_{on} sinh(\frac{i}{i_{on}}) exp[-exp(\frac{x - a_{on}}{w_c} - \frac{\lvert i\rvert}{b}) - \frac{x}{w_c}] & i < 0 \end{cases}$
TEAM	$v(t) = [R_{on} + \frac{R_{OFF} - R_{ON}}{x_{off} - x_{on}}(x - x_{on})].i(t)$ or $v(t) = R_{ON}.exp(\frac{\lambda}{x_{off} - x_{on}}(x - x_{on})).i(t)$	$\frac{dx(t)}{dt} = \begin{cases} k_{off}(\frac{i(t)}{i_{off}} - 1)^{\alpha_{off}}.f_{off}(x) & 0 < i_{off} < i \\ 0 & i_{on} < i < i_{off} \\ k_{on}(\frac{i(t)}{i_{on}} - 1)^{\alpha_{on}}.f_{on}(x) & i < i_{on} < 0 \end{cases}$

oxygen vacancies in the device and the length of the doped region is zero, which does not make sense. Similarly, the doped region cannot take up all the device length; since it will leave no undoped region and the device will not work. In order to overcome the boundary problem, a window function ($f(w)$ or $f(x)$) is adopted and added to the state variable derivative.

2.4.2 Nonlinear Ion Drift Model

The linear drift model produces the hysteresis characteristics of the memristor, but it also has some limitations regarding basic electrodynamics. Studies and experiments have proved that the behavior of the implemented memristors are quite nonlinear and the linear ion drift model is not accurate enough. This model assumes that the memristor is a voltage-controlled element having nonlinear dependency between the voltage and the state derivative. Moreover, asymmetric switching behavior is considered. Lehtonen et al. [12] proposed a model based on the results of [13]. The current–voltage relationship and state variable derivative of this model are described in the third row of Table 2.1 where α, β, γ, χ, a and m are experimental fitting parameters, and n determines how the state variable can affect the current. Here, the state variable w is normalized within the interval [0, 1]. This model shows asymmetric switching behavior where during the ON state, the I–V curve follows a tunneling process (sinh part). But, during the OFF state, the I–V curve behaves similar to a PN junction (the exponential part). The exponential model presents a more reasonable description of a functional memristive device. The fact that this model is more sensitive to voltage levels gives it the flexibility to reconcile stable reading with fast writing. A low voltage level can be used during the read process which will lead to a very long switching time that translates into a more stable device. On the other hand, a higher voltage level can be used for writing the memristor in much smaller time intervals.

2.4.3 Simmons Tunnel Barrier Model

A more accurate physical model was proposed by [14] where this device is modeled as a resistor in series with an electron tunnel barrier. But in the previous models, the device is modeled as two series resistors for doped and undoped oxide regions. This model assumes nonlinear and asymmetric switching behavior due to an exponential dependence of the movement of the ionized dopants. Besides, this model exhibits nonlinear and asymmetric switching characteristics. The width of Simmons tunnel barrier is the state variable x [15]. The relationship between the current and the voltage is shown as an implicit equation based on the Simmons tunneling model [14]. Fourth row in Table 2.1 shows the state variable derivative relation where C_{off}, C_{on}, a_{off}, a_{on}, i_{off}, i_{on}, and b are fitting parameters. C_{on} is an order

of magnitude larger than C_{off}, and they both have an effect on the magnitude of the change of x. i_{on} and i_{off} confine the current threshold in an effective way. These current thresholds are useful in digital applications. The values of a_{off} and a_{on} force the upper and the lower bound for x, respectively, so there is no need for a window function. This model is the most accurate model for the memristor but it suffers some problems; (1) it is complicated, (2) the relationship between current and voltage is not explicit, and (3) it is not a generic model, since it describes a specific type of memristor. A complicated SPICE model of Simmons tunnel barrier is proposed in [16].

2.4.4 Threshold Adaptive Memristor Model

In Kvatinsky et al. [17], introduced a simple and a generic model which fits the aforementioned models even the physical model with acceptable error. This simple model is built based on a couple of assumptions for analysis simplification and computational efficiency; (1) no change in the state variable below a certain threshold, and (2) instead of exponential dependence, there is a polynomial dependence involved between the memristor current and the internal state drift derivative. The dependence of the internal state derivative on current and the state variable itself is modeled by multiplying two degenerate functions: one is a function of current and the other is dependent on state variable x as obvious in the fifth row in Table 2.1. Where $k_{off}, k_{on}, \alpha_{off}$, and α_{on} are constants ($k_{off} > 0, k_{on} < 0$). i_{off} and i_{on} are current thresholds and x is the internal state variable. The functions $f_{off}(x)$ and $f_{on}(x)$ act as the window functions, constraining x to the bounds $[x_{on}, x_{off}]$. Moreover, two current–voltage relationships to fit the previous models (written in Table 2.1). In the first relation, the memristance is linearly proportional to the state variable x which fits the first two models. However, the second relation is built to fit Simmons tunnel barrier where the memristance is exponentially proportional to the state variable x where λ is a fitting parameter and should satisfy $\lambda = ln(R_{OFF}/R_{ON})$. R_{ON} and R_{OFF} are effective memristances at bounds x_{on} and x_{off}, respectively.

As stated in [17], the TEAM model is accurate enough with a mean error of 0.2 % and can boost the simulation runtime by 47.5 %. It also satisfies the convergence conditions, computational efficiency required by simulation engines and also the requirements of a memristive system. The conditions for the previous model induction is introduced in details in [17]. A comparison between the different memristive device models is listed in Table 2.2.

2.4.5 Window Functions

Each model has a certain region which can work entirely. For example, the linear ion drift model can work only in the interval of $[0, D]$. So to prevent the state variable from getting out of the bound, and also to add more nonlinear behavior close to the

Table 2.2 Comparison of different memristor adopted from [17]

Model	Linear ion drift	Nonlinear ion drift	Simmons tunneling barrier	TEAM
State variable	$0 \leq w \leq D$	$0 \leq x \leq 1$	$a_{off} \leq x \leq a_{on}$	$x_{on} \leq x \leq x_{off}$
Control mechanism	Current	Voltage	Current	Current
I–V relation	Explicit	Explicit	Ambiguous	Explicit
Memristance relation	Explicit	Ambiguous	Ambiguous	Explicit
Generic	No	No	No	Yes
Accuracy	Lowest	Low accuracy	Highest	Sufficient
Threshold exists	No	No	Yes	Yes

bounds, the derivative of the state variable is multiplied by a window function. So, the window functions should give two things; (1) a state variable working interval, and (2) the nonlinearity near boundaries to force it to reach zero when the state variable is at the bounds. In the following, some of the window functions that have been proposed are introduced in the next sections. Moreover, a comparison between different window functions is listed in Table 2.3.

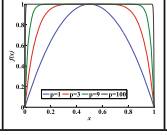
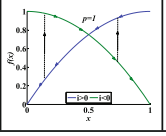
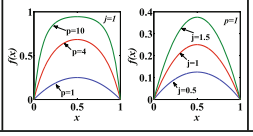
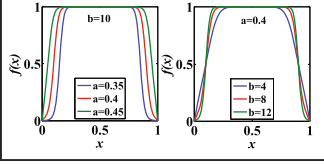
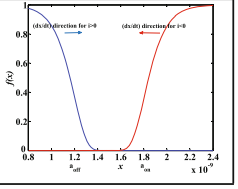
2.4.5.1 HP

In Strukov et al. [6, 18], proposed a simple window function $f(w)$ that reaches its maximum at the center of the device, $w = 0.5D$, and decreases toward the boundaries where it will reach zero speed at the terminal states $w = 0$ or $w = D$. This simple function $f(w)$ is $w(D - w)/D^2, 0 < w < D$ in which the boundary conditions are $f(0) = f(D) = 0$. This function has a symmetric behavior which does not describe the real nonlinearities of the memristor. All the properties of this window function are shown in Table 2.3.

2.4.5.2 Joglekar

Joglekar and Wolf have developed a generic symmetric window function [19]. The authors added a control parameter to control the nonlinearity of the function, which is $f(x) = 1(2x1)^{2p}$ in which p is a positive control parameter and $x = w/D$. The function looks similar to the rectangular window function when p increases, and the nonlinear drift phenomenon decreases. Moreover, the boundary conditions are simple as $f(0) = f(1) = 0$. Also, the state variable function will approximate the linear drift assumption $f(0 < x < 1) \approx 1$ when $p \leq 5$ [19, 20]. On the other hand, the main disadvantage of HP's and Joglekar's window function is at the boundaries

Table 2.3 Comparison of available window functions

	Joglekar[65]	Biolek [67]	Prodromakis[69]	Piecewise[70]	TEAM [63]
$f(x)$	$1-(2x-1)^{2p}$	$1-(x-stp(-i))^{2p}$	$j\left(1-\left[(x-0.5)^2+0.75\right]^p\right)$	$\begin{cases}(1+(\frac{x-0.5}{a})^{2b})^{-1} & x_o \le x \le 1-x_o \\ kx(1-x) & otherwise\end{cases}$	$exp\left[-exp\left(\frac{\lvert x-x_{on,off}\rvert}{w_c}\right)\right]$
Symmetry	Yes	Yes	Yes	Yes	Not necessarily
Resolve boundary conditions	No	Discontinuities	Practically yes	Practically yes	Practically yes
Impose nonlinear drift	Partially	Partially	Partially	Partially	Yes
Scalable factor $f_{max} \le 1$	No	No	Yes	Yes	No
Fits memristor model	Linear/ nonlinear ion drift/ TEAM	Linear/ nonlinear ion drift/ TEAM	Linear/ nonlinear ion drift/ TEAM	Linear/ nonlinear ion drift/ TEAM	TEAM for Simmons tunneling barrier fitting
					

where the state variable may cling at the boundary and it becomes difficult to change due to the zero value of the window function at either boundary.

2.4.5.3 Biolek

Biolek et al. introduced a window function with a solution for the modeling inaccuracy of Joglekar's window function and introduced the first PSPICE model for the memristor in [21]. This SPICE model is most commonly used to simulate the memristor in analog and digital circuits ideas. The presented window function is $f(x) = 1(x - sgn(-i))^{2p}$ where p is a positive integer, i is the memristor current and $sgn(i) = 1$ when $i \leq 0$ and $sgn(i) = 0$ when $i < 0$. Biolek et al. introduced this model to overcome the problem of Joglekar's window function (stuck at the boundary). Biolek's function is designed to resolve this problem by using $sgn(-i)$ which gives different values for approaching and receding the boundaries. But, this raises another problem which is the continuity condition at the boundaries. Also, It should be noted that Biolek's window function is a multivalued function which hardens the analysis of the memristor-based circuits [22].

2.4.5.4 Prodromakis

In Prodromakis et al. [23], handled a problem in the aforementioned window functions which is the scalability. The authors designed this window function to be scalable and include HP's window function. This window function is $f(x) = j\left(1 - [(x - 0.5)^2 + 0.75]^p\right)$ where p is a control parameter and is a positive real number unlike the constraint of the control parameter being an integer in the Joglekar's and Biolek's functions. Also, when $p = 1$, this model is reduced to HP's window function. The scalable factor j is used to adjust the maximum value of the window function f_{max}. The properties of this window function are shown in Table 2.3.

2.4.5.5 Piecewise

In [24], the piecewise window function is presented. This window function is continuously differentiable and consists of three nonlinear pieces. Also, a single-valued function between the memristance and the charge can be obtained. This window function is shown in Table 2.3 where $a \in (0, 0.5)$, $b \in \mathbb{Z}^+$, and $x_0, k \in \mathbb{R}^+$. But, there are certain conditions to ensure the continuous differentiability of this window function as given in [24].

2.4.5.6 TEAM

This window function is designed to fit the behavior of Simmon tunnel model barrier [17]. There are two functions for ON and OFF switching and do not have to be equal like the Simmons tunnel barrier model where the dependence on x is asymmetric. The parameters x_{on}, x_{off}, and w_c are fitting parameters. More details about this window can be found in [17].

2.5 Mathematical Modeling of HP Memristor

The transient response under any voltage supply $v_s(t)$ on the memristor based on the linear dopant HP's memristor model was discussed before in [20, 25, 26]. Assuming that the memristance value R_m is at an initial value R_i, then the current passing through the memristor is given by:

$$i(t) = \frac{v_i(t)}{R_m(t)} = \frac{1}{\eta k}\frac{dx}{dt} = \frac{-1}{\eta k R_d}\frac{dR_m(t)}{dt}, \tag{2.6}$$

where η reflects the memristor polarity, $k = \mu_n R_{on}/D^2$, and $R_d = R_{off} - R_{on}$. Therefore

$$R_{mc}^2(t) = R_i^2 - 2\eta k R_d \varphi(t),\ R_m(t) = min(max(R_{mc}(t), R_{on}), R_{off}), \tag{2.7}$$

where $\varphi(t)$ is the flux at time t, $R_{mc}(t)$ is the calculated memristance, $R_m(t)$ is the final memristance value after the clipping conditions to make sure that $R_m(t) \in [R_{on}, R_{off}]$. Based on the HP's paper [6], let us assume that $R_{on} = 100\,\Omega$, $R_{off} = 16{,}000\,\Omega$, $\mu_n = 10^{-14}$, $D = 10\,\text{nm}$ for the upcoming examples. For example, if $v_s(t) = V_o$ (DC supply), the value of the memristance is given by [20]:

$$R_m(t) = \sqrt{R_i^2 - 2k\eta R_d V_o t},\ R_m \in [R_{on}, R_{off}], \tag{2.8}$$

Figure 2.3 illustrates the changes of the memristance value versus time, initial value R_i and also versus the voltage amplitude V_o. However, if $v_s(t) = t$, then the memristance value can be obtained as: $R_m(t) = \sqrt{R_i^2 - k\eta R_d t^2}$, $R_m \in [R_{on}, R_{off}]$ as shown in Fig. 2.4 where the memristance reaches its minimum value R_{on} at different times based on the initial value.

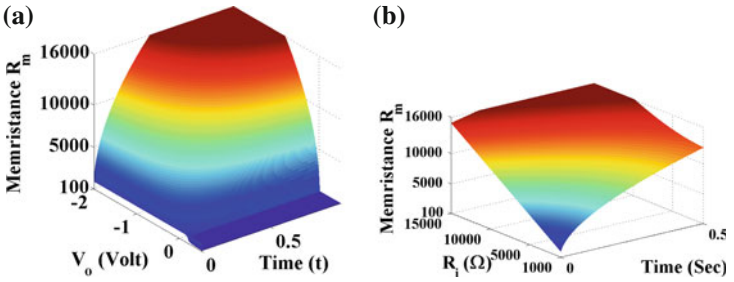


Fig. 2.3 The memristance value in case of step input voltage $v_s(t) = V_o$, $\eta = +1$ versus **a** *time* $- V_o$ plane when $R_i = 1000\,\Omega$, and **b** *time* $- R_i$ plane when $V_o = -1\,\mathrm{V}$

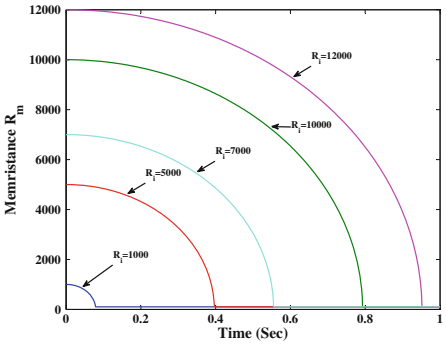


Fig. 2.4 The transient response of the memristance value under ramp input source $v_s(t) = t\,\mathrm{V}$, when $\eta = +1$ for different values of $R_i = 1, 5, 7, 10, 12\,\mathrm{k}\Omega$

As discussed before, the basic characteristics of the memristor appear under sinusoidal input $v_s(t) = V_o sin(\omega t + \theta)$, where the memristance value can be calculated as [25]:

$$R_m(t) = \sqrt{R_i^2 - \frac{2k\eta R_d V_o}{\omega}(cos(\theta) - cos(\omega t + \theta))},\ R_m \in [R_{on}, R_{off}], \qquad (2.9)$$

Figure 2.5 shows the input voltage and memristance for two different frequencies $f = 0.5\,\mathrm{Hz}$ and $f = 1\,\mathrm{Hz}$ where the memristance reaches its maximum in the first case as the flux increases unlike the second case. Moreover, the effect of the angle θ is shown in Fig. 2.6. Figure 2.7 presents the time waveforms of the input voltage, current as well as the $i - v$ and $R - v$ characteristics for two different frequencies where the range of R_m decreases as the frequency increases. Also, Fig. 2.8 shows the rotation effect of the $i - v$ characteristic versus frequencies until the memristance effect disappeared at high frequency. The upper limit of the memristance versus the $V_o - f$ is shown in Fig. 2.9a which illustrates the resistance range for many case. From the previous discussion, the hysteresis loop should decrease as the frequency

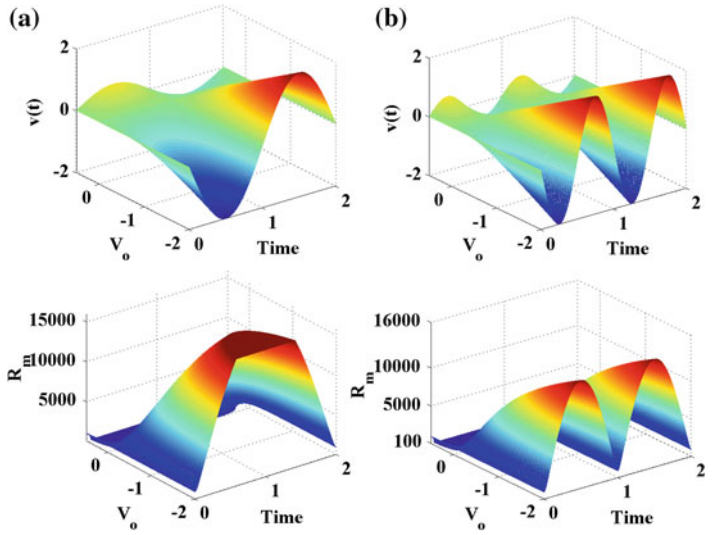


Fig. 2.5 The input voltage and the memristance value versus the $V_o - time$ plane when the input voltage is $v_s(t) = V_o sin(2ft + \theta)$ when $R_i = 1\,\text{k}\Omega$ for two different frequencies; **a** $f = 0.5\,\text{Hz}$, and **b** $f = 1\,\text{Hz}$

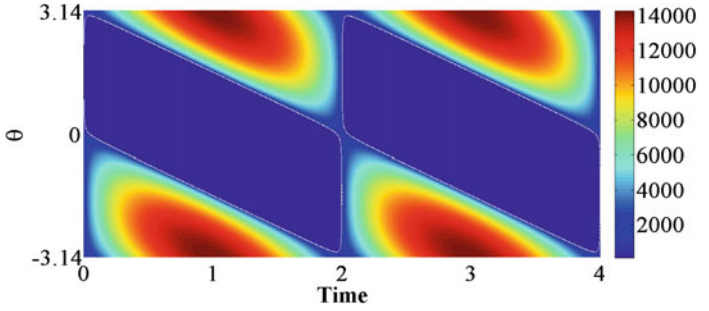


Fig. 2.6 The memristance contours versus $time - \theta$ plane when the input voltage is $v_s(t) = V_o sin(2ft + \theta)$, $R_i = 1\,\text{k}\Omega$, and $f = 0.5\,\text{Hz}$

increases. Figure 2.9b shows the upper loop where A_1 and A_2 are the areas when the voltage increases and decreases, respectively. The area enclosing the $i - v$ hysteresis is inversely proportional to the frequency f which validates the previous figures. Moreover, the relationship between the charge and flux can be obtained by:

$$q = \int_0^t i(\tau)d\tau = \int_0^t \frac{v(\tau)}{\sqrt{R_i^2 - 2k\eta R_d \varphi(\tau)}} d(\tau) = \frac{\sqrt{R_i^2 - 2k\eta R_d \varphi} - R_i}{\eta k R_d}. \quad (2.10)$$

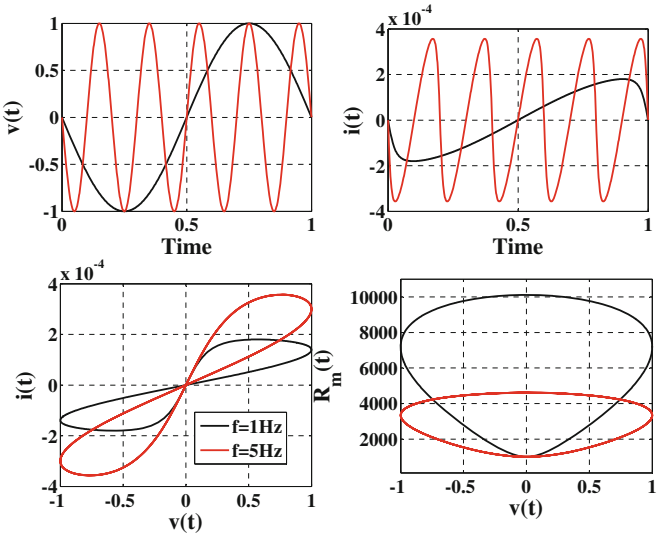


Fig. 2.7 The input voltage, current, $i-v$, and R_m-v responses when the input voltage is $v_s(t) = -sin(2\pi ft+\theta)$, $R_i = 1\,\text{k}\Omega, \theta = 0$, and for two different frequencies $f = 1$ and $5\,\text{Hz}$

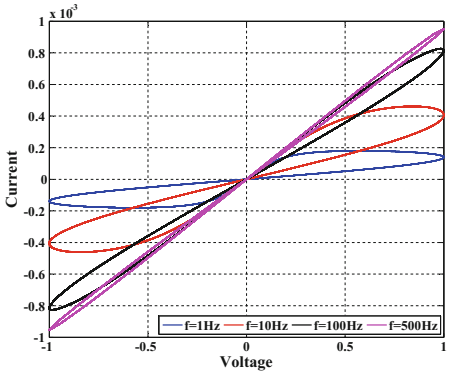


Fig. 2.8 The $i-v$ characteristics for sinusoidal input with $R_i = 1\,\text{k}\Omega, \theta = 0$, $V_o = -1\,\text{V}$ for four different frequencies $f = 1, 10, 100, 500\,\text{Hz}$

The flux–charge relationship is represented by a parabola centered at $(\varphi,\ q) = (\frac{R_i^2}{2\eta k R_d}, \frac{R_i}{\eta k R_d})$. More discussion about the periodic responses and sensitivity analysis of the flux were presented in [25].

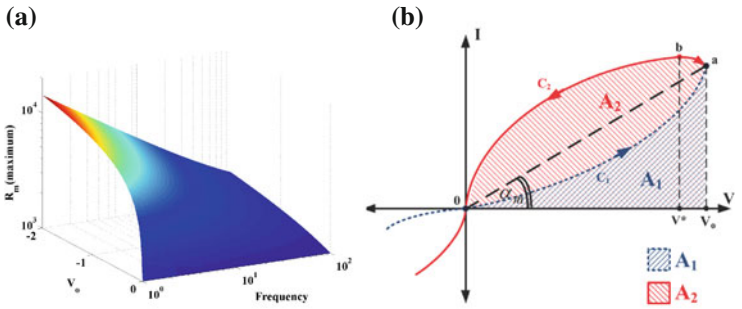


Fig. 2.9 **a** The upper limit of the memristance under sinusoidal input with $R_i = 1\,\text{k}\Omega$, $\theta = 0$ versus the $V_o -$ *frequency* plan, and **b** the area inside the $i - v$ hysteresis loop

2.6 Mathematical Representations of Time-Invariant Memristor

In 2014 Chua [27], introduced three mathematical representations of time-invariant memristors, each one has two forms depending on whether the input signal is a current source (current-controlled memristor) or a voltage source (voltage-controlled memristor). In the following sections, we will present these three representations as follows:

2.6.1 Extended Memristor

An extended memristor is defined as:

- Current-controlled extended memristor

$$v = R(x, i)i, \tag{2.11a}$$

$$\frac{dx}{dt} = f(x, i), \tag{2.11b}$$

  where $\lim_{i \to 0} R(x, i) \neq \infty$.
- Voltage-controlled extended memristor

$$i = G(x, i)v, \tag{2.12a}$$

$$\frac{dx}{dt} = g(x, v), \tag{2.12b}$$

  where $\lim_{v \to 0} G(x, v) \neq \infty$.

For example [27], let us consider an extended memristor which is defined by the following equations:

$$v = R(x, i)i = 0.01x^2 i^3, \tag{2.13a}$$

$$\frac{dx}{dt} = f(x, i) = -x^3 - 2x^2 + (3 + t^2)x. \tag{2.13b}$$

When $i = I$, the DC $V - I$ curve can be obtained by solving the DC equilibrium equation $\frac{dx}{dt} = 0$, then $f(x, I) = 0 = x(I^2 - (x - 1)(x - 3))$. Therefore, $x = 0$ is an equilibrium state independent of the value of I. The other two states are given by $x = -1 \pm \sqrt{4 + I^2}$.

Although there are three $V - I$ branches are $V = 0$ and $V = 0.01(-1 \pm \sqrt{4 + I^2})^2 I^3$ as shown in Fig. 2.10a but the first curve ($V = 0$) is unstable, while the other two curves are stable [27]. The pinched $i - v$ pinched characteristic when $i = 10sin(2\pi ft)$ for two different frequencies $f = 5$ and 20 Hz are also shown in Fig. 2.10b.

It should be noted that satisfying (2.11) and (2.12) is not enough to obtain an extended memristor model. For example [27], let us assume the following system:

$$v = R(x, i)i, \quad R(x, i) = \frac{\alpha x}{i} \tag{2.14a}$$

$$\frac{dx}{dt} = \beta i. \tag{2.14b}$$

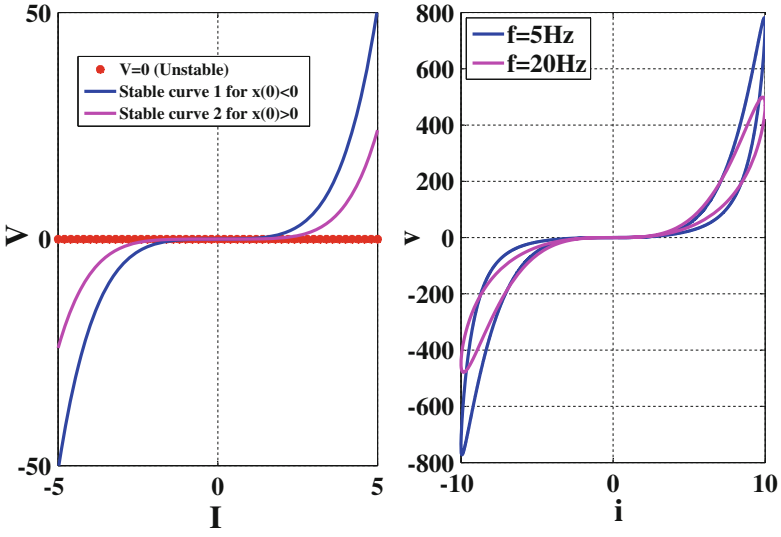


Fig. 2.10 **a** The $I - V$ DC curves, and **b** the $i - v$ characteristics for sinusoidal input

where α and β are constants. Let us apply current source, $i(t) = cos(t)$, across this memristor. Thus, the state variable is $x(t) = x(0) + \beta \int_0^t sin(\tau)d\tau = sin(t)$ assuming zero initial conditions. Substituting into (2.14), we obtain $v = \alpha\beta sin(t)$ so $i^2 + v^2 = cos^2(t) + (\alpha\beta sin(t))^2 = 1$ for $\beta = 1/\alpha$. This means that Lissajous figure in the $v - i$ plane is the unit circle which is not pinched at the origin $(v, i) = (0, 0)$. The previous system defines 1 *Farad capacitor*. So, we can reach a remark which is

$$If\, v - i\ plane\ isn't\ pinched,\ it's\ not\ a\ memristor.$$

2.6.2 Generic Memristor

A generic memristor is defined in

- Current-controlled generic memristor

$$v = R(x)i, \tag{2.15a}$$

$$\frac{dx}{dt} = f(x, i), \tag{2.15b}$$

- Voltage-controlled generic memristor

$$i = G(x)v, \tag{2.16a}$$

$$\frac{dx}{dt} = g(x, v). \tag{2.16b}$$

2.6.3 Ideal Memristor

An ideal memristor is defined as

- Current-controlled ideal memristor

$$\varphi = \varphi_1(q). \tag{2.17}$$

Or

$$v = R(q)i, \tag{2.18a}$$

$$\frac{dq}{dt} = i, \tag{2.18b}$$

where $R(q) = \frac{d\varphi_1(q)}{dq}$ is called memristance in Ohm (Ω). The constitutive relation of current-controlled ideal memristor can be recovered to $\varphi_1(q) = \varphi_0 + \int_0^t R(q)dq$ where φ_0 is an arbitrary constant.

- Voltage-controlled ideal memristor

$$q = q_1(\varphi). \tag{2.19}$$

Or

$$i = G(\varphi)v, \tag{2.20a}$$

$$\frac{d\varphi}{dt} = v, \tag{2.20b}$$

where $G(\varphi) = \frac{dq_1(\varphi)}{d\varphi}$ is called memductance in Siemens(S). The constitutive relation of voltage-controlled ideal memristor can be recovered to $q_1(\varphi) = q_0 + \int_0^t G(\varphi)d\varphi$ where q_0 is an arbitrary constant.

2.6.3.1 Memristor Siblings

Every ideal memristor can be recast into a generic memristor with a scalar state variable x defined via a differentiable one-to-one function in the following steps:

For a given constitutive relation between y and u

$$y = y_1(u). \tag{2.21}$$

1. Choose any differentiable one-to-one function

$$x = x_1(u), \tag{2.22}$$

and calculate its inverse function as

$$u = x_1^{-1}(x). \tag{2.23}$$

2. Differentiate (2.21) relative to u then substitute by (2.23) to calculate $\frac{y}{u} = Z$ as follows:

$$Z(x) = \frac{dy_1(u)}{du}|_{u=x_1^{-1}(x)}. \tag{2.24}$$

3. The relation between the state derivative $\frac{dx}{dt}$ and u is calculated by:

$$f(x, \frac{du}{dt}) = f_1(x)\frac{du}{dt}, \tag{2.25}$$

where

$$f_1(x) = \frac{dx_1(u)}{du}|_{u=x_1^{-1}(x)}. \tag{2.26}$$

4. Define the memristor sibling as follows:

$$y = Z(x)u, \tag{2.27a}$$

$$\frac{dx}{dt} = f_1(x)u, \tag{2.27b}$$

The aforementioned are applicable for current- or voltage-controlled memristor siblings by setting (φ, q) or (q, φ) instead of (y, u), respectively. Thus, $Z(.)$ become $R(.)$ or $G(.)$ for current or voltage-controlled memristor.

Since the function $x = x_1(u)$ can be chosen to be any differentiable one-to-one function, it follows that every ideal memristor has an uncountable number of memristor siblings that would give the same voltage response to a given input current $i(t)$ (the same current response to a given input voltage v(t)). So as Chua said "Indeed, every Ideal Memristor is the mother of an infinite family of equivalent Generic Memristors" [27].

2.6.3.2 Ideal Generic Memristor

This is a small subclass of generic memristor where $F(x) = \int \frac{dx}{f_1(x)}$ is one-to-one function.

An example of creating an ideal generic memristor sibling [27] is given by assuming that the constitutive relation between (y, u) is

$$y = u + u^3/3 \tag{2.28}$$

by following the previous steps;

Step 1: the arbitrary differentiable one-to-one function is $x = u^3 = x_1(u)$. So the inverse relation is given by $u = x^{\frac{1}{3}} = x_1^{-1}(x)$.

Step 2: $Z(x) = \frac{dy_1(u)}{du}|_{u=x^{\frac{1}{3}}} = 1 + x^{\frac{2}{3}}$.

Step 3: $f_1(x) = \frac{dx_1(u)}{du}|_{u=x^{\frac{1}{3}}} = 3x^{\frac{2}{3}}$.

Step 4: The memristor sibling is given as follows:

$$y = (1 + x^{\frac{2}{3}})u, \tag{2.29a}$$

$$\frac{dx}{dt} = 3x^{\frac{2}{3}}u. \tag{2.29b}$$

In case of current-controlled ideal generic memristor sibling is given by:

$$v = (1 + x^{\frac{2}{3}})i, \tag{2.30a}$$

$$\frac{dx}{dt} = 3x^{\frac{2}{3}}i. \tag{2.30b}$$

But for current-controlled ideal generic memristor sibling is given by:

$$i = (1 + x^{\frac{2}{3}})v, \tag{2.31a}$$

$$\frac{dx}{dt} = 3x^{\frac{2}{3}}v. \tag{2.31b}$$

It is worth to be noted that HP memristor is the trivial ideal generic Memristor [6] as proved in [27].

2.7 Memristor Implementation Types

This section describe briefly some recent implementations of the memristor based on different materials. Till now there is no data sheet for the memristor because it is not being available commercially. Since the hysteresis is an indicator of the memristive properties for any material, there are huge efforts using different materials for implementations where experimental results are obtained.

- Titanium dioxide memristor
  The resistive switching characteristics of titanium dioxide were originally described in 1960 [28]. Then, around 300 papers were published on titanium dioxide until 2008 [8]. For example, IBM published an article in 2000 regarding structures similar to that described by HP [29], also Samsung has a U.S. patent for oxide-vacancy-based switches [30]. In 2008, HP reported that the memristor can be obtained based on the titanium dioxide [6] and published a U.S. patent application related to the memristor construction [31].
- Polymeric (ionic) memristor
  Different realizations of a polymeric memristor have been published even before the HP memristor. For instance, in 2004, Krieger et al. proposed a structure of a passive layer between electrode and active thin films, which enhanced the extraction of ions from the electrode to create functioning nonvolatile memory cells [32]. Also in 2008, Erokhin and Fontana developed a polymeric memristor [33]. Then in 2009, Berzina et al. reported results on the improved performance of electrochemically controlled polymeric memristors [34].
- Ferroelectric memristor
  The first ferroelectric memristor was proposed in 1963 [35] where the basic idea of this device is to perform the function of memory in ferroelectric material, and to control the field-effect conductance of a semiconductor by the permanent

polarization of the ferroelectric material. But in 2012, the ferroelectric memristor was proposed in [36] based on a thin ferroelectric barrier sandwiched between two metallic electrodes. Switching the polarization of the ferroelectric material by applying a positive or negative voltage across the junction can lead to two orders of magnitude resistance variation: $R_{OFF} >> R_{ON}$ (an effect called Tunnel Electro-Resistance). In general, the polarization does not switch abruptly. The reversal occurs gradually through the nucleation and growth of ferroelectric domains with opposite polarization. During this process, the resistance is neither R_{ON} or R_{OFF}, but in between. When the voltage is cycled, the ferroelectric domain configuration evolves, allowing a fine-tuning of the resistance value. The ferroelectric memristor's main advantages are that the ferroelectric domain dynamics can be tuned, offering a way to engineer the memristor response, and that the resistance variations are due to a purely electronic phenomena, and aiding device reliability as no deep change to the material structure is involved.

- Resonant-tunneling diode memristors
  Memristive properties have appeared in certain types of quantum well diodes with special doping designs of the spacer layers between the source and drain regions [37, 38].
- Graphene Oxide memristors
  Choi and his team have made flexible memristors using thin graphene oxide films [39]. They use a similar design, swapping titanium dioxide for graphene oxide. After depositing 50-micrometer-wide aluminum wires on a 6.5 cm^2 piece of plastic, they spin a solution containing suspended graphene oxide flakes onto the surface. This forms a thin film of overlapping graphene oxide flakes over which the researchers deposit the top aluminum wire array. This results in 25 memristors, each 50 μm wide. Also, in 2012, Williams and his team in Hewlett-Packard Development Company introduced a patent about fabricating the defective graphene-based memristor [40]. A graphene-based memristor includes a first electrode, a defective graphene layer adjacent to the first electrode, a memristive material that includes a number of ions adjacent to the defective graphene layer, a second electrode adjacent to the memristive material, and a voltage source that generates an electric field between the first and the second electrodes. Under the influence of the electric field ions in the memristive material form an ion conducting channel between the second electrode and the defective graphene layer is formed.
- Silicon Oxide memristors
  In 2010, researchers developed silicon oxide memristive substrates that show promise for transitioning much of the worlds current fab and production infrastructure to memristor production [41]. Mehonic et al. reported a study of resistive switching in a silicon-based memristor device in which the active layer is silicon-rich silica. The resistive switching phenomenon is an intrinsic property of the silicon-rich oxide layer and does not depend on the diffusion of metallic ions to form conductive paths. Switching exhibits the pinched hysteresis I/V loop characteristic of memristive systems, and on/off resistance ratios of 104:1 or higher can be easily achieved. Scanning tunneling microscopy suggests that switchable

conductive pathways are 10 nm in diameter or smaller. Programming currents can be as low as 2 μA, and transition times are on the nanosecond scale [41].

- Spin memristive systems
  Spin-based memristive systems, as opposed to molecular and ionic nanostructure-based systems, rely on the property of degree of freedom in electron spin. In these types of systems, electron spin polarization is altered, usually through the movement of a magnetic domain wall separating polarities, allowing for hysteresis-like behaviors to occur.
  In 2009, Wang et al. described three examples of possible spintronic memristors [42]. These examples are based upon spin-torque-induced magnetization switching and magnetic domain wall motion. Also, they proved that the spintronic device can be designed to explore and memorize the continuum state of current and voltage based on interactions of electron and spin transport. Moreover, in 2011, an experimental proof of the spintronic memristor based on domain wall motion by spin currents in a magnetic tunnel junction was introduced [43].
  Certain types of semiconductor spintronic structures exhibit memristive behavior [44]. The mechanism of the memristive behavior in such structures is based entirely on the electron spin degree of freedom which allows for a more convenient control than the ionic transport in nanostructures. When the external excitation is changed, the adjustment of electron spin polarization is delayed because of the diffusion and relaxation processes causing hysteresis.

2.8 Memristor-Based Applications

After HP invented the passive model of the memristor, researchers from all over the world have started significant experiments to demonstrate the applications of the memristor. Memristors have been proposed for a wide range of applications such as nonlinear analog circuit design, chaotic systems, nonvolatile memory, and neuromorphic systems as will be briefly discussed in this section.

2.8.1 Analog Circuits

2.8.1.1 Memristor-Based Sinusoidal Oscillators

The idea of memristor-based sinusoidal oscillators has been introduced in many recent publications [45–47] which depends on the replacement of some or all resistors with memristors in the most common oscillator circuits and investigating the response. For example, the four Wien oscillators family have been tested using memristors where sustained oscillations were reported and an approximated oscillation frequency is obtained in [46]. Figure 2.11 shows the four different Wien oscillators with the replacement of R_1 with memristor $R_m(t)$. These four cases have been

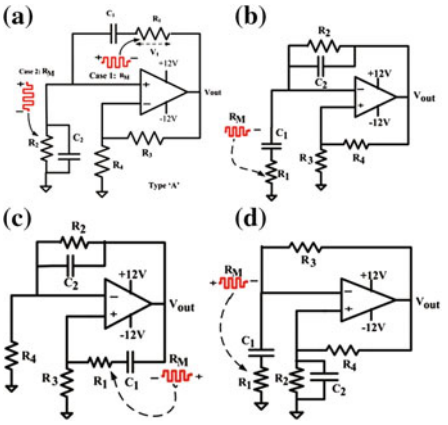


Fig. 2.11 Schematics of other members of Wien oscillator family. **a** Type A, **b** Type B, **c** Type C, and **d** Type D

discussed using PSPICE circuit simulations and Fig. 2.12a shows the output response and the memristance value for each case.

It is important to note that the sustained oscillation is achieved although the memristance value oscillates, which reflects the time-dependent oscillating poles as shown in Fig. 2.12b as a good example for parametric oscillation. The effect of the initial resistance R_i on the oscillation frequency using numerical and PSPICE simulations is also discussed in [48] as shown Fig. 2.14. Other circuits that validate the same concept for third-order oscillators were introduced in [49]. Moreover, a complete resistorless oscillator where all resistors are replaced with memristors was discussed as shown in Fig. 2.13 [50] where six resistors have been replaced with memristors and sustained oscillation has been achieved.

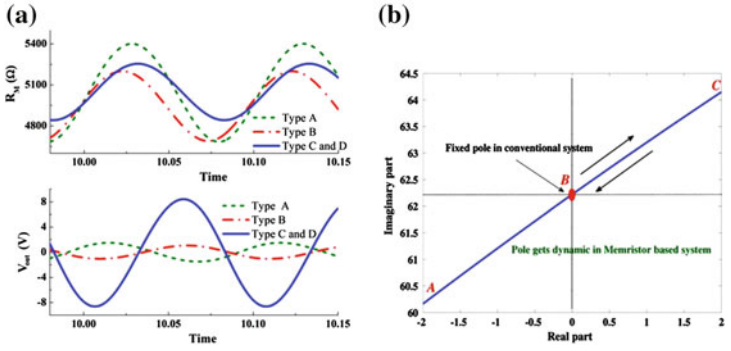


Fig. 2.12 **a** Transient response for the four Wien oscillator family and **b** oscillating poles in the s-plane of type "A"

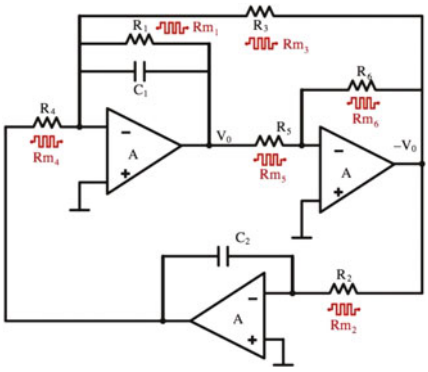


Fig. 2.13 Resistorless memristor-based oscillator

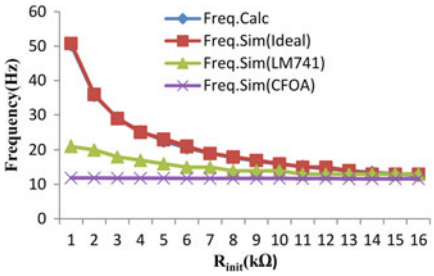


Fig. 2.14 Effect of R_i on the oscillation frequency

2.8.1.2 Programmable Analog Circuits

In many analog circuits such as amplifiers and filters, resistors need to be programmed for adaptation to particular applications or for compensation of PVT (Process, Voltage, and Temperature) variations. The programmable resistor with fine resolution and small parasitics is very useful in many analog and RF range differential circuits. By using the programmable resistance, it can be adopted for programmable attenuators, programmable gain amplifiers and programmable filters, among others.

The most popularly used method to realize programmable resistors takes the form of switch-controlled resistors composed of an array of weighted resistors and switches. However, it has a critical drawback due to the fact that these switches, typically MOS switches, introduce large parasitic capacitances and resistances. Furthermore, the parasitic values are dependent on the switch state. The state-dependent large parasitics limit the resolution and the number of bits of switching resistors. In particular, programming and control of the amount of charge on the floating gate require high voltages for the tunneling and injection to allow electrons with sufficient energy to tunnel through the insulating oxide from/to the floating gate, and thus leads to long-term reliability problems. Another problem with floating-gate devices is that the long-term charge storage capabilities are unreliable. The charge stored on the floating gate may slowly leak away with time and this problem will get worse, as the process scales down with reduced oxide thickness.

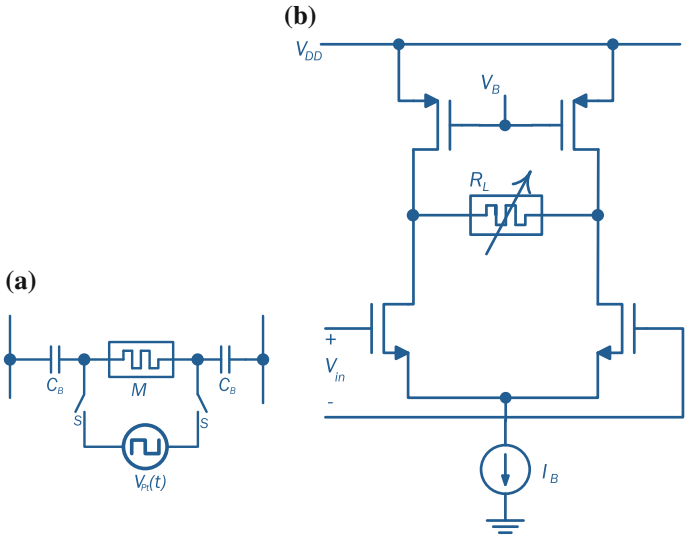


Fig. 2.15 Circuit schematic of **a** programmable resistor using memristor and **b** programmable gain amplifier using the programmable resistor [51, 52]

The authors in [51, 52] introduced a programmable resistor with fine resolution which is built using a memristor as shown in Fig. 2.15a. This programmable resistor consists of a floating memristor, simple series switches (S), provides very high impedances (R_{OFF}) during the normal mode operation and low impedances (R_{ON}) for the programming duration, and two blocking capacitors C_B to block DC mismatch or even order mismatches, which can cause unbalanced flux between the differential signals where this circuit suffers from any unbalanced flux amount across the memristor. Any kind of odd order mismatches will not hurt the differential balance by its nature. Even for the capacitor mismatch, it does not even contribute to the voltage imbalance, unlike the case of the differential gain. In order to ease the programming and controllability operations, they proposed a pulse-coded memristor programming method where the memristance is programmed by patterning the pulse waveform. In case of a voltage-controlled memristor, the flux can be linearly controlled by determining the number of pulses (N_{PULSE}), duty ratio, pulse amplitude (V_{PT}), and pulse frequency (ω_{PT}). In this circuit, the memristance decreases or increases depending on the accumulated flux of the memristor as discussed in Sect. 2.5.

The authors used this idea of programmable resistor to build a programmable gain amplifier, shown in Fig. 2.15b, where the *ac* voltage gain is $A_v = g_m(r_o//R_L)$ where g_m is the differential transconductance of M_1 and M_2, r_o is the amplifier's output impedance formed M_1 and M_2 and R_L is the load resistance. Therefore, the *ac* gain is a function of R_L so by controlling R_L, we can control the *ac* gain of the amplifier. Thus, the gain decreases or increases depending on the accumulated flux due to pulse source. This memristor-loaded amplifier circuit shows a fine gain resolution over the

wide tuning range under low-voltage programming pulses, other performances such as linearity and speed are exactly the same, as those of the cases with linear load resistors. This circuit becomes more advantageous when the application frequency is in the RF range, since the blocking capacitors can be integrated together with CMOS active devices for higher input frequencies.

Another programmable memristor circuit is proposed by Pershin and Di Ventra in 2010 [53]. This memristor-based circuit works as a digital-controlled potentiometer which consists of a memristor and a couple of FETs. Two external control signals are used to program the memristance R_m between two limiting values R_1 and R_2. Furthermore, several programmable analog circuits have been introduced such as a programmable threshold comparator, a programmable gain amplifier and a programmable relaxation oscillator.

Several other papers have been published for introducing different variable gain amplifier (VGA) topology utilizing titanium dioxide (TiO_2) memristors [54–56]. The TiO_2 solid-state memristor was employed in the feedback branch of an inverting voltage amplifier and was programmed externally so the typical circuit gain is M/R_1 followed by a low-pass filter to remove the DC voltage. In [54], the circuit was analyzed based on charge-controlled and voltage-controlled memristor models. Furthermore, in [56], the circuit was experimentally tested using a solid-state memristor. The experimental results show overall good performance of the memristor as a gain setting element in the op-amp feedback branch, where modifying the resistance of the memristor shunts the output impedance of the voltage amplifier, achieving distinct multiple gain levels.

2.8.1.3 Adaptive Filters

In Driscoll et al. [57], introduced the memristive adaptive filters where the memristive properties of vanadium dioxide are used. The authors experimentally demonstrated the adaptive filter functionality by constructing a simple R_{mLC} band-pass filter shown in Fig. 2.16 by adding a VO_2 memristive device R_m in series with an external capacitor C and inductor L. The inset shows an optical photograph of the two-terminal device used, a 5 μm × 20 μm VO_2 region lithographically defined by gold contacts.

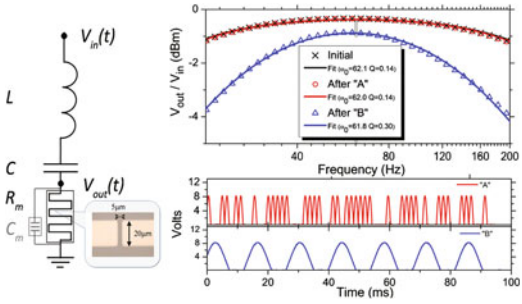


Fig. 2.16 Schematic for R_{mLC} adaptive filter, small-signal transfer function (V_{out}/V_{in}), and time series of the off-resonance "A" sequence of pulses and on-resonance "B" sequence of pulses [57, 58]

Moreover, the adaptive filter transfer function (V_{out}/V_{in}) plotted before and after off-resonance A and on-resonance B pulses and solid lines are RLC band-pass filters fit to data, which generates the ω_o and Q values in the legend showing in Fig. 2.16.

However, in [59], another memristor model is used to obtain first- and second-order low-pass filter. This memristor is based on fabricated zinc oxide (ZnO) nanowires grown on the copper layer of a printed circuit board which shows similar characteristics as memristive metal/oxide/metal structures. The ZnO device is used with a capacitor and an inductor to form a low-pass adaptive filter where the memristor reacts to different input voltage bias and changes its resistance accordingly. Also, the gain, damping, and Q-factor of the low-pass filters are observed to vary with small input voltages.

2.8.1.4 Loop Filter of Phase-Locked Loop

In communication systems, charge-pump phase-locked loop (CPPLL) is extensively used in frequency synthesis and clock recovery. Figure 2.17a shows a schematic diagram of CPPLL, which consists of a phase and frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and a divider ($\div N$). In Zhao et al. [60], proposed a memristor-based controlled proportional-integral (PI) controller to design the loop filter in the charge-pump phase-locked loop (CPPLL). The low-pass PI controller is based on a monotonic increasing piecewise linear (PWL) memristor where a periodic rectangular pulse current source is applied as the input. The proportionality constant of the PI controller is controlled by the width of the pulse, i.e., the amount of charge passing through the memristor, which effectively controls the bandwidth of the controller. This circuit is very useful for fast locking when CPPLL is in the unlocked state, and to lower phase noise when CPPLL is in the locked state. In addition, the loop filter is passive and easy to design compared to other implementations such as adaptive bandwidth phase-locked loops (PLLs).

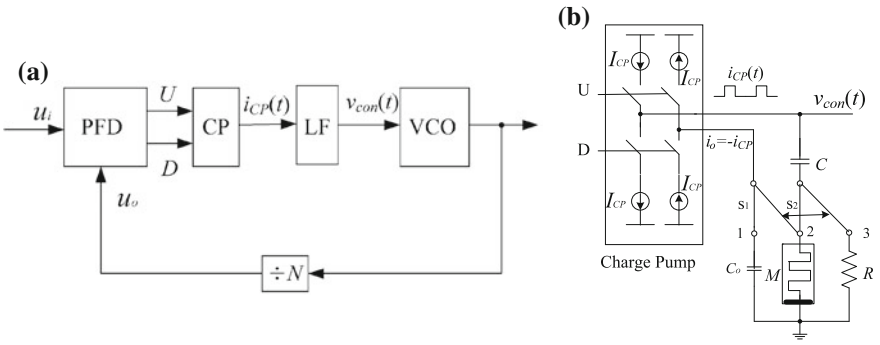


Fig. 2.17 **a** Schematic diagram of CPPLL and **b** memristor-based filter circuit [60]

2.8.2 Neuromorphic Circuits

A neuromorphic system is a mixed mode analog–digital system mimicking neural architecture to pattern neurons by real-time computation, simulation, and emulating the nervous system. But to simulate neural networks in electronic regime neurons and synapses (connections between neurons), this requires an implementation with very low power consumption. Electronic synapses are more difficult to engineer as they require being flexible as well as dynamic with memory capability. Scientists have simulated brains of small animals (cat, rat, and spider) [61–64] but associating computer memory more than terabytes (e.g., Blue Gene/P of IBM). Thus, the memristor plays a significant role to perform as a synapse with negligible power thrust [65, 66]. In Pershin et al. [66] have designed a memristor emulator which shows associative memory function with three electronic neurons connected by two memristor–emulator synapses. Also, S.H. Jo made a memristor with a Ag and Si active layer forming a highly conductive Ag-rich region and a less conductive Ag-poor region (Fig. 2.18). This hybrid system is capable of spike timing dependent plasticity (STDP) [67, 68] which is an important synaptic function. If the synapse update rate is 1 Hz, then this system can continue synaptic operation for around 5 years. The basic idea of STDP in memristive devices was proposed before [69] and a practical implementation of circuit learning was demonstrated by patterning the learning of an amoeba-like cell into a memristive system [64].

2.8.3 Chaotic System

Because of the random nature of chaotic systems, the memristor as a nonlinear element is well applicable for encryption and random number generation. The memristor makes it possible for better control and simpler versions of chaotic systems. Chua modeled the memristor to produce a chaotic attractor with negative conductance

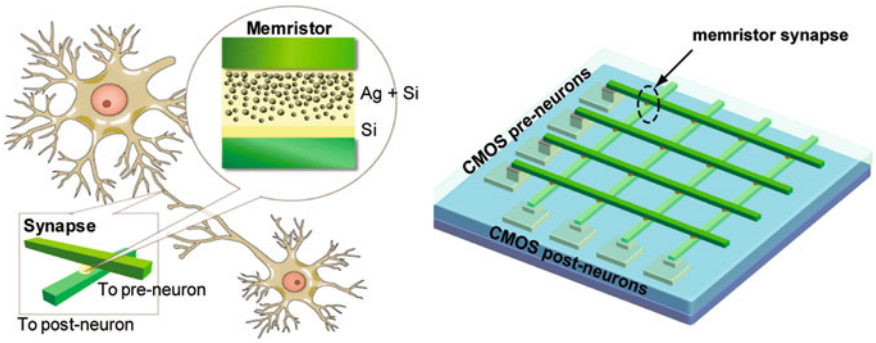


Fig. 2.18 Schematic illustration of using memristors as synapses between neurons [58, 64]

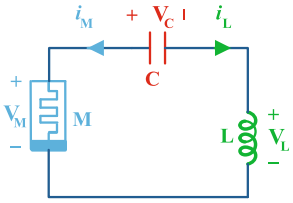


Fig. 2.19 Schematic of the proposed circuit [71]

and capacitor [70]. Though it was merely simulation based but the simplicity and functionality initiated memristor-based chaotic systems. Recently Muthuswamy and Chua demonstrated the simplest chaotic oscillator [71] where they used an inductor–capacitor–memristor series circuit as shown in Fig. 2.19. Though, the memristor was actively realized, and the pinched hysteresis loop was shown by both experimental and theoretical simulation where the memristance function is $R(x) = \beta(x^2 - 1)$ and $\dot{x} = i_M - \alpha x - i_M x$. The nonlinearity of the memristor adds up to the third state variables along with the inductor and the capacitor and the simplest system is also BIBO stable. Around the same time, Muthuswamy has shown another simpler practical implementation [72, 73] of the memristor in generating chaos. The difference between the two circuits is that in [72] the memristor is flux controlled, whereas in [71] it is charge controlled but both realizations look similar.

On the other hand, Cheng has demonstrated a memristor oscillator which gives periodic orbits of chaos from a 2-scroll transient chaos [74]. In another paper [75], a similar transition is observed but with more complicated dynamical behavior of the memristor where the initial condition plays the major role in generating periodic chaos. The effect of the initial condition on chaotic behavior is well studied in [76] where both the piecewise linear model and cubic model of the memristor are shown capable of periodic orbits somewhat similar to Hopf bifurcation. The theoretical study of generating chaos has also appeared in [77] with a cubic model of a flux-controlled memristor.

Recently, a chaotic circuit based on HP memristor was published in [78]. The circuit makes use of two HP memristors in an antiparallel connection as shown in Fig. 2.20a. The circuit is based on the topology of the canonical Chua's oscillator with the Chua's diode substituted by two HP memristors in antiparallel connection. The circuit consists of one negative resistor, two capacitors, an inductor, and two memristors. Numerical results of chaotic behavior are reported in Fig. 2.20, which shows the attractor obtained where three different bi-dimensional projections are also shown.

In order to increase chaos order, the memristive chaos circuits are extended to the fractional order as discussed in [79] where the fractional order is added to a memristor-based Chua's circuit for the first time. Moreover, a numerical solution of the fractional-order memristor-based Chua's equations was derived including dynamical behavior and stability analysis. In [80], the authors extended the simple chaotic circuit (shown in Fig. 2.19) to the fractional-order domain where the numerical solution was given using a predictorcorrector method and stability analysis of the system

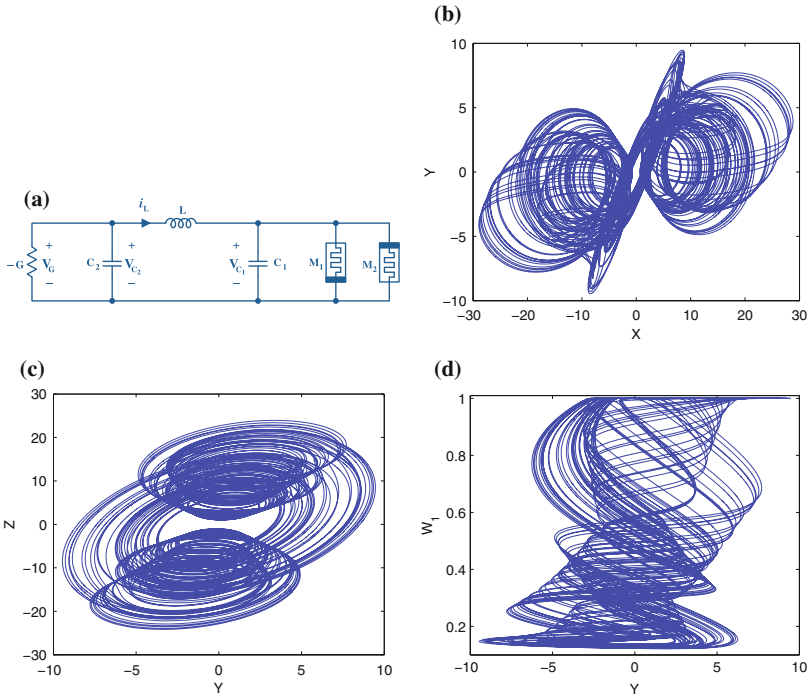


Fig. 2.20 Chaotic circuit and the attractors **a** circuit based on two HP memristors in antiparallel, **b** x-y phase plane, **c** y-z phase plane, and **d** y-w_1 phase plane [78]

equilibria are carried out, with the aim to show that chaos can be found when the order of the derivative is 0.965.

The most common application for chaotic systems is building secure communication systems but the main problem is how to sync between the receiver and transmitter [81]. A novel kind of compound synchronization among four chaotic systems was investigated in [82], where a sufficient condition is obtained to ensure compound synchronization among four memristor chaotic oscillator systems based on the adaptive technique. Moreover, a secure communication scheme via adaptive compound synchronization of four memristor chaotic oscillator systems was introduced. The authors derive the corresponding theoretical proofs and numerical simulations to demonstrate the validity and feasibility of the proposed control technique. Also, in [83], another chaotic oscillator was introduced which depends on the Van der Pol oscillator coupled to a linear circuit (VDPCL). This circuit has a very special stability property, exhibits interesting spectral characteristics, which makes it suitable for chaos-based secure communication applications.

Another category of chaotic oscillators is introduced in [84] which is inductance free. This circuit is composed of a twin-T oscillator, a passive RC network, and a flux-controlled memristor. The circuit exhibits complicated chaotic behavior of double periodicity.

2.8.4 Digital Applications

2.8.4.1 Memrories

Resistive Random Access Memory (RRAM) is a two-terminal device where the switching medium is sandwiched between top and bottom electrodes and the resistance of the switching medium can be modulated by applying electrical signal (current or voltage) to the electrodes. Even though large electrical nonvolatile resistance changes are also observed in ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and phase change of material states RAM (PRAM).

One simple approach to integrate RRAM cells with conventional CMOS circuitry is 1T1R (1 transistor + 1 resistance switching element) structure [85, 86]. The select transistor controls the location of the switching element to be accessed. The 1T1R approach can be integrated with CMOS. However, since each switching element requires one transistor in this approach, the storage density will still be limited by transistor scaling and the advantages of the simple two-terminal RRAM devices have not been fully utilized.

Generally, the memristor essentially shows resistive switching behavior as it has metal–insulator–metal configuration. Before the physical evolution of the memristor, researchers have demonstrated high density memory applications of resistive switching [85–87] where the insulating layer works as a storage medium. Though the memristive characteristics were not realized, and the results held the memristor as a promising candidate as a nonvolatile memory. In [88] Chen assumed a Pt/MgZnO/Pt device as a memristor and showed its resistive switching characteristics which are reversible and steady, leading toward nonvolatile memory. Recently as a nonvolatile memory the density of the memristor is reported to be 100 Gbits/cm^2 in [89] which requires very low energy compared to the existing flash memory.

HP lab experimentally demonstrated the nonvolatility of the memristor which is CMOS compatible, fast in response, and requires very low power [13, 14, 90]. The nonvolatile memristor latch in [90] is shown to have high endurance of 104 write cycles. In [13], 1 × 17 cross point arrays of the Pt/TiO2/Pt memristor was fabricated to show the nonvolatility where the oxygen vacancies were engineered for controlling polarity and resistance of switching. The mathematical explanation of resistive switching of Pt/TiO2/Pt memristor revealed that with higher applied current the switching time reduces sharply to decrease the input energy exponentially [14]. A comprehensive mathematical illustration of the memristor as nonvolatile

memory has been reported in [91] which will help to design a memristive system for memory applications. The nonvolatile memory capability of the memristor will turn on computers without rebooting them and hopefully in the future no physical RAM will be required separately.

In [92], The authors introduced a study of a memristor-based nonvolatile SRAM (or memristor latch) cell to achieve fast bit-to-bit parallel store/restore operations, low store/restore energy consumption, and a compact cell area which is suitable for low power mobile applications. This memristive nonvolatile 8T2R (Rnv8T) cell includes two fast-write memristor (RRAM) devices vertically stacked over the 8T, and a novel 2T memristor switch, which provides both memristor control and SRAM write-assist functions. The write-assist feature enables the Rnv8T cell to use read favored transistor sizing to prevent read/write failure at lower V_{DDS}. Moreover, the authors also fabricated the first macro-level memristor-based nonvolatile SRAM. This 16 Kb Rnv8T macro achieved the lowest store energy and R/W $V_{DD_{min}}$(0.45V) of any nonvolatile SRAM or two-macro solution.

Field programmable gate arrays (FPGAs) offer programmability at relatively low development cost and good performance. The common FPGA architecture consists of a regular, flexible and programmable two-dimensional array of configurable logic blocks (CLBs). Usually, a CLB consists of-lookup tables (LUTs), multiplexers and flip-flops (FFs). LUTs are used to implement combinational logic circuits. All configurable resources (inclusive of the LUTs) are controlled by the configuration bits stored in a static random access memory cell (SRAM). However, an SRAM is unable to retain the configuration bits should either a malfunction occur at the power supply, or the power is turned off. A possible solution consists of storing the configuration bits in a nonvolatile flash memory; thus the flash memory is integrated into the FPGA. This leads to issues such as a larger silicon area, increase in cost and most importantly very slow data retrieving time. Moreover, as technology enters the very deep submicron and nanoscales, a substantial increase of leakage current is encountered when the FPGA is in standby mode, hence causing additional power dissipation. Thus an alternative nonvolatile memory block (as a LUT) based on the memristor as a storage device was proposed in [93] to overcome the above mentioned issues.

2.8.4.2 Logic Implementation

One exciting application of memristors is using them as the basic building block of a logic gate. In [94] a memristor-based logic gate—the IMPLY gate is implemented. The IMPLY gate can be used to implement all binary operations of two variables.

Borghetti et al. [94] used memristors to realize material implication, and then realized all the fundamental Boolean operations using material implication. The basic implication gate/latch circuit is shown in Fig. 2.21b. Two memristors, P and Q, are connected using a common horizontal nanowire to a load resistance, R_G, which is connected to the ground. The states of P and Q are represented by logic values p and q, respectively. The vertical nanowires cross over the horizontal nanowires and a layer of memristive switching material forming P and Q. Each memristive

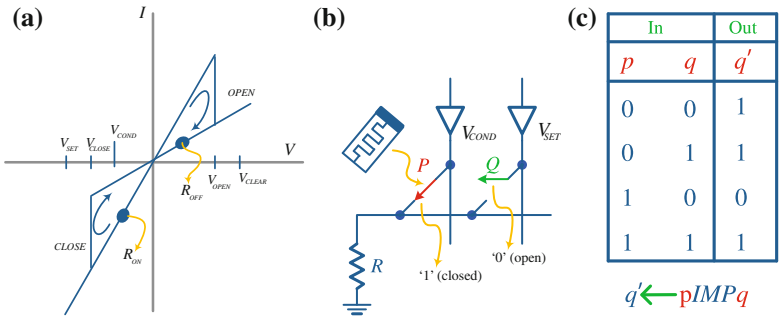


Fig. 2.21 **a** Idealized memristive electrical characteristics, **b** basic implication circuit, and **c** truth table for IMP operation [94, 95]

device can be assigned to logic 1 or logic 0 by using the tri-state drivers. When applying a negative voltage, V_{SET} a device is assigned logic 1 set (operation TRUE). Also when applying a positive voltage, V_{CLEAR} a device is assigned logic 0 clear (operation FALSE), and hence a high memristance is considered as logic 0 and a low memristance is considered as logic 1. V_{COND} is defined as a negative voltage with a magnitude smaller than V_{SET} which does not change the state of the driven device. The notation $p \leftarrow x$ indicates that the state of switch P (the logic value p) is changed to x the next time P is pulsed by V_{CLEAR}, V_{SET} or V_{COND}.

The memristive IMP operation q ← pIMPq is implemented by applying V_{SET} to Q and V_{COND} to P simultaneously, in order for the two pulses and the load resistor R_G to change the states of p and q depending on their previous states. When P is in a high memristance state (logic 0), the applied voltage on Q is roughly V_{SET} and Q is turned on (q = 1) and p stays unchanged. On the other hand when P is in a low memristance state (logic 1) the voltage on the common terminal becomes V_{COND} and the voltage across memristor Q is roughly $V_{SET} - V_{COND}$ and both P and Q stay unchanged. Figure 2.21c shows the truth table for operation q ← pIMPq.

Using material implication the 16 binary operations of two variables were realized in the supplementary information of [94]. By using these functions any arithmetic circuit can be realized. The delay can be calculated by calculating how many IMPLY operations are performed in each gate as shown in Table 2.4 [96].

Using these logic gates, any combinational logic can be designed. In Shaltoot and Madian [97], introduced two different memristor-based architectures of carry lookahead adder. The first one is based on conventional carry lookahead adder based on implication. And the second one is simplified carry lookahead adder based on IMPLY gate. Moreover, their proposed circuits gave better results comparable to the conventional carry lookahead adder for increasing the number of bits. As a result, many circuits can be built using the full adder circuit such as multipliers [98].

Table 2.4 Boolean operations implemented via material implication

Operation	Implementation	Devices area
p NAND q	$=p$ IMP (q IMP 0)	3
p AND q	$=(p$ IMP (q IMP 0)) IMP 0	4
p NOR q	$=((p$ IMP 0) IMPq) IMP 0	4
p OR q	$=(p$ IMP 0) IMP q	3
p XOR q	$=(p$ IMP q) IMP((q IMPp)IMP 0)	3
NOT p	$=p$ IMP 0	2

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Chapter 3
Memristor Mathematical Models and Emulators

Recently, different mathematical models describing the generic memristors have been introduced [1–3]. But, the first model of the memristor was introduced by HP in [4], where the memristor current voltage relationship was described by

$$v(t) = [x_d(t)R_{on} + (1 - x_d(t))R_{off}]i(t), \tag{3.1}$$

where $i(t)$ represents the current through the memristor, $v(t)$ is the voltage across the memristor, R_{on} and R_{off} are the minimum and maximum achievable resistances of the memristor, respectively. The memristor resistance depends on state variable $x_d(t)$ which is the ratio between the doped region length and the full length D of the memristor and is given by

$$\frac{dx_d}{dt} = \eta k i(t). \tag{3.2}$$

Integrating (3.2) and substituting in (3.1); assuming zero initial condition for the current, the memristance R_m can then be given by (3.3)

$$R_m = R_{in} - \eta k q(t), \tag{3.3}$$

where $\eta \in -1, 1$ represents the memristor polarity, $k = \frac{\mu_v R_{on}(R_{off} - R_{on})}{D^2} \Omega/\mathrm{C}$; μ_v is the ion mobility, and R_{in} is the initial resistance of the memristor.

A.G. Radwan and M.E. Fouda, *On the Mathematical Modeling of Memristor, Memcapacitor, and Meminductor*, Studies in Systems, Decision and Control 26,
DOI 10.1007/978-3-319-17491-4_3

3.1 Continuous Symmetrical Model

A simple symmetrical double-loop hysteresis behavior model describing an ideal generic model can be written as [1]:

$$k(t) = \frac{y(t)}{x(t)} = \left(a + b \int_0^t x(\tau) d\tau \right), \tag{3.4}$$

When $x(t) = sin(\omega t)$, then $\int_0^t x(\tau)d\tau$ will be always positive then $k(t)$ (either memristance or transmemristance) can be rewritten as $k(t) = a + \frac{b}{\omega}(1 - cos(\omega t))$. Therefore, $k(t) \in [a, a + \frac{2b}{\omega}]$ which has an average of $(a - \Delta k)$ and amplitude Δk where $\Delta k = \frac{b}{\omega}$. It is clear that the value of $k(t)$ is inversely proportional to the frequency, and Δk decays as frequency increases toward the value a as ω tends to infinity. Then, let us define f_{th} at which the maximum value of $k(t)$ is equal to 1 % above a, i.e., $2\Delta k = 0.01a$. Then, if $f > f_{th}$, the values of $k(t)$ can be approximately fixed and equals to a. Then the value of f_{th} can be given by $f_{th} = \frac{100b}{\pi a}$ Hz.

When $x(t) = cos(\omega t)$, then $\int_0^t x(\tau)d\tau$ may be positive or negative and $k(t)$ can be rewritten as $k(t) = a + \frac{b}{\omega} sin(\omega t)$. Therefore, $k(t) \in [a - \frac{b}{\omega}, a + \frac{b}{\omega}]$ with an average of a and amplitude Δk where $\Delta k = \frac{b}{\omega}$. Similarly, $k(t)$ approaches the value a as ω tends infinity. Then, the value f_{th}, is given by $f_{th} = \frac{50b}{\pi a}$ Hz. As a result of the above analysis, $k(t)$ will expand in both directions which reflects that $y = \pm x$ will be a symmetry line of such hysteresis. The polarity of a which determines the operating quadrant are shown in Fig. 3.1 as well as four different cases.

There are two different implementations of the previous model where $x(t)$ is represented by a current (voltage) and $y(t)$ is represented by a voltage (current) which is called current (voltage)-controlled memristive device, respectively. It is

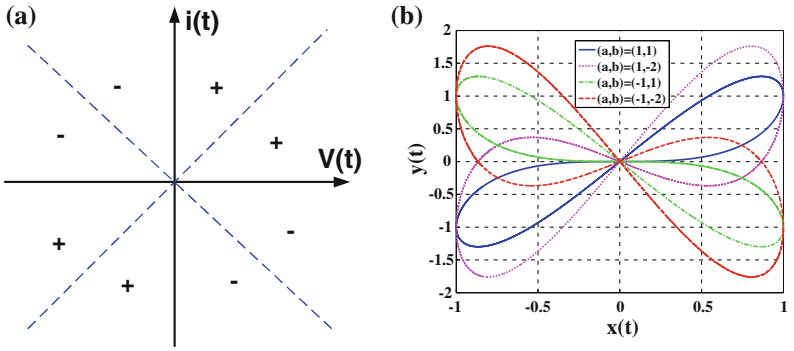

Fig. 3.1 Regions where the hysteresis appears when $x(t) = cos(\omega t)$, **a** polarity of a, and **b** four different cases of hysteresis

worth noting that the authors of [5] have recently proposed conditions for symmetric pinched hysteresis. The above model satisfies these conditions and is simpler than the one in [5].

3.1.1 Current-Controlled Memristor

Assuming $x(t) = \frac{i(t)}{I_{ref}}$, $y(t) = \frac{v(t)}{I_{ref} R_s}$, where I_{ref} is an arbitrary reference current and R_s is an arbitrary resistance. By substituting into (3.12), the current-controlled memristor equation and the memristance $R_m = v(t)/i(t)$ are given by ($a = b = \pm 1$) [1]:

$$v(t) = \pm i(t) R_s \pm \frac{i(t) R_s}{I_{ref}} \int_0^t i(\tau) d\tau = \pm i(t) R_s \pm \frac{i(t) R_s}{I_{ref}} q(t), \tag{3.5a}$$

$$R_m = \pm R_s \pm \frac{R_s}{I_{ref}} q(t). \tag{3.5b}$$

It is seen here that R_m is a function of the accumulated current which is essentially the charge $q(t)$; similar to (3.3). Note that there are four different possibilities for R_m, which are $(+, +)$, $(+, -)$, $(-, +)$, and $(-, -)$ they, respectively, represent incremental/decremental R_m and incremental/decremental negative R_m. The first subplot of Fig. 3.2 shows the I–V characteristics for three different frequencies with sinusoidal input current $i(t)$ with $I_{ref} = 1\,\mu\text{A}$ and $R_s = 10\,\text{k}\Omega$. The effect of I_{ref} is also illustrated for fixed frequency in the second plot where the hysteresis loop rotates and shrinks. The range of the memristance (the maximum and minimum values of R_m) for sine and cosine inputs and versus different frequencies and I_{ref} are shown, respectively in Fig. 3.3. It is clear that the memristive effect appears strongly in the lower frequencies and also for smaller values of I_{ref}.

3.1.2 Voltage-Controlled Memristor

Setting $x(t) = \frac{v(t)}{V_{ref}}$, $y(t) = \frac{i(t)}{V_{ref} G_s}$, where V_{ref} is an arbitrary reference voltage and G_s is an arbitrary transconductance. By substituting into (3.12), the voltage-controlled memristor equation and its transmemristance G_m are given by

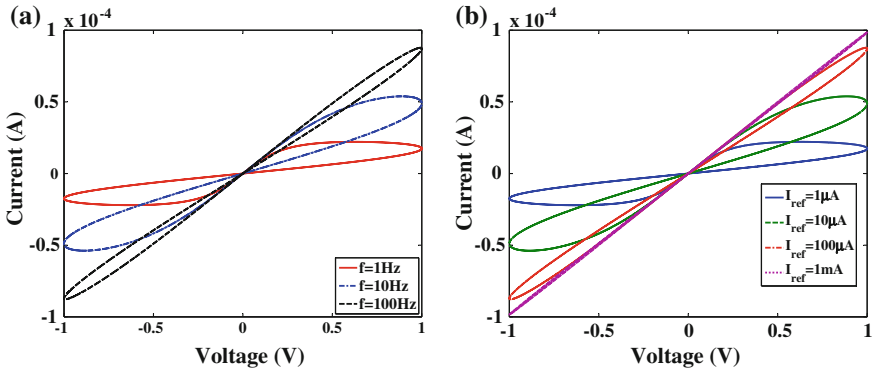

Fig. 3.2 I–V characteristics of an incremental R_m with $R_s = 10\,\mathrm{k}\Omega$, **a** for different frequency when $I_{ref} = 1\,\mu\mathrm{A}$, and **b** for different I_{ref} when $f = 1\,\mathrm{Hz}$

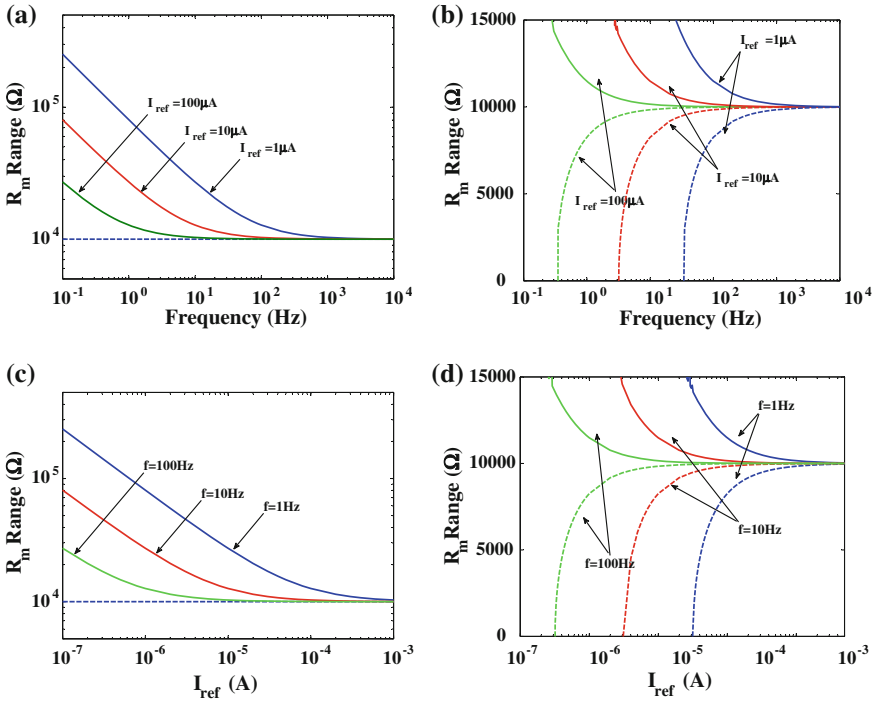

Fig. 3.3 Maximum and minimum incremental R_m when $R_s = 10\,\mathrm{k}\Omega$, **a** for different I_{ref} under Sine input, **b** for different I_{ref} under Cosine input, **c** for different frequencies under Sine input, and **d** for different frequencies under Cosine input

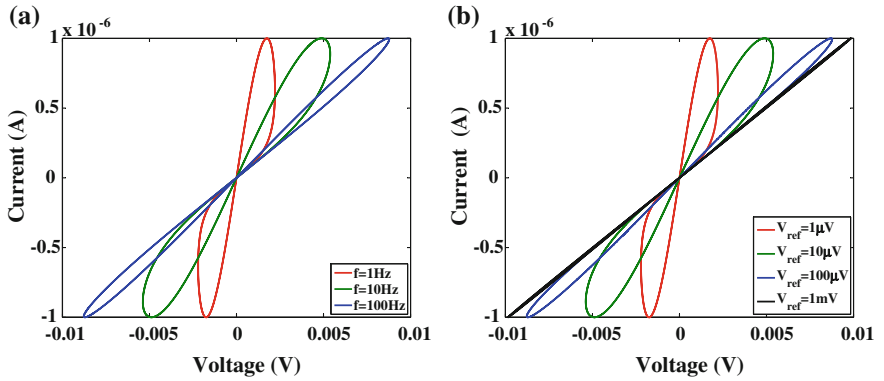

Fig. 3.4 I–V characteristics **a** versus frequency when $V_{ref} = 1\,\mu\text{A}$, and **b** versus V_{ref} when $f = 1\,\text{Hz}$

$$i(t) = \pm v(t)G_s \pm G_s \frac{v(t)}{V_{ref}} \int_0^t v(\tau)d\tau = \pm v(t)G_s \pm G_s \frac{v(t)}{V_{ref}} \varphi(t), \tag{3.6}$$

$$G_m = \pm G_s \pm \frac{G_s}{V_{ref}} \varphi(t). \tag{3.7}$$

where $\varphi(t)$ is the accumulated flux. Similarly, there are four different possibilities representing incremental/decremental G_m and incremental/decremental negative G_m, respectively. Figure 3.4 shows the effect of V_{ref} and frequency on the I–V characteristics for different cases.

3.1.3 Circuit Emulators

To validate the previous discussion and due to the absence of physical commercially memristors, this section discusses two different emulator circuits followed by circuit simulations. The first emulator is based on the current-controlled memristor and the other for the voltage-controlled memristor discussed above as shown in Figs. 3.5 and 3.6 where two current conveyor (CCII) devices (built using the commercial AD844 current feedback op amps), a voltage multiplier (built using the commercial AD633 multiplier), and a noninverting or inverting buffer (built using a general purpose op amp such as the TL082) are needed. Analysis of Fig. 3.5 reveals that the input current is given by [1]:

$$i_{in}(t) = \frac{V_{in} - V_{fb}}{R_s}, \tag{3.8}$$

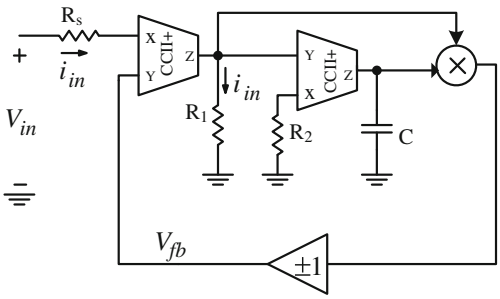

Fig. 3.5 Current-controlled decremental/incremental memristor emulator

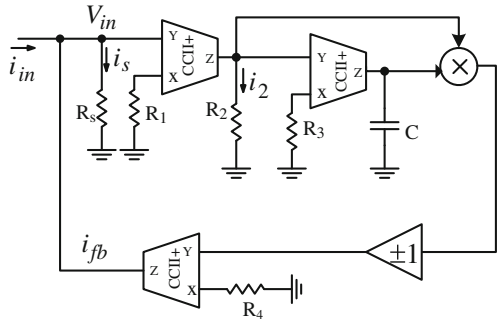

Fig. 3.6 Voltage-controlled decremental/incremental memristor emulator

where V_{in} is the applied voltage and V_{fb} is the feedback voltage given by

$$V_{fb} = K\eta \frac{R_1^2}{R_2 C} i_{in}(t) \int_0^t i_{in}(\tau) d\tau = K\eta \frac{R_1^2}{R_2 C} i_{in}(t) q_{in}(t) \tag{3.9}$$

The incremental/decremental memristor can be achieved by the buffer operation where η is either 1 or -1, respectively. The memristance is thus given by

$$R_m(t) = R_s + K\eta \frac{R_1^2}{R_2 C} q_{in}(t), \tag{3.10}$$

which is similar to (3.3) if $\frac{R_s}{I_{ref}} = K \frac{R_1^2}{R_2 C}$ where $K = 1/10$ for the AD633.

Similarly, for the voltage-controlled memristor (Fig. 3.6), the transmemristance can be obtained by:

$$G_m(t) = G_s - K\eta \frac{R_2^2}{R_1^2 R_3 R_4 C} \varphi(t). \tag{3.11}$$

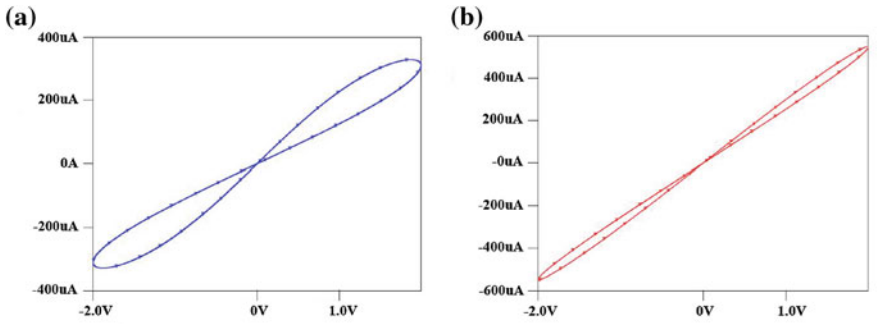

Fig. 3.7 I–V characteristics, **a** incremental memristor I_{ref}, C, $R_s = 1, 1\,\mu\text{F}, 4\,\text{k}\Omega$, and **b** decremental memristor I_{ref}, C, $R_s = 1, 0.1\,\mu\text{F}, 4\,\text{k}\Omega$

Figure 3.7 shows the PSPICE simulation results for the incremental and decremental memristors. The advantage of these emulators that they can be implemented easily using any of the available CMOS designs for current conveyors [6] and four quadrant multipliers [7].

3.2 Continuous Nonsymmetrical Model

In order to modify the previous model to obtain a nonsymmetric I–V hysteresis, a new term will be added as follows [1]:

$$y(t) = x(t)\left(a + c\int_0^t x(\tau)d\tau\right) + b\frac{dx(t)}{dt}, \tag{3.12}$$

When $x(t) = sin(\omega t)$, the relationship between $x(t)$ and $y(t)$ is given by:

$$y(t) = \left(a + \frac{c}{\omega}\right)x(t) \pm \left(b\omega - \frac{c}{\omega}x(t)\right)\sqrt{1 - x^2(t)}. \tag{3.13}$$

Generally for each value of x there are two values of y except at the pinched point (x_p, y_p) which can be calculated by

$$x_p = \frac{b\omega^2}{c}, y_p = \left(a + \frac{c}{\omega}\right)x_p, \quad x_p \leq 1, \tag{3.14}$$

and the line $y = (a + \frac{c}{\omega})x(t)$ is the symmetry line. Moreover, the hysteresis is always passing by the points $(1, a + \frac{c}{\omega})$, $(0, y_o = \pm b\omega)$, and $(-1, -a - \frac{c}{\omega})$. For fixed values of a, b, and ω and different c, the outer boundary points are fixed. The pinched point x_p and the intersection with the vertical axis increase as b increases

as shown in Fig. 3.8a. The effect of c for fixed a, b, and ω is shown in Fig. 3.8b where the intersection points of the hysteresis with the vertical axis are fixed, but the pinched and boundary points are affected. Similarly, the effect of the parameter a is shown in Fig. 3.8c with the same pinched point. Note that if $x_p = \frac{b\omega^2}{c} > 1$, then there is no pinched point and the hysteresis consists of a single loop as shown in Fig. 3.8d. To illustrate the symmetry of the hysteresis, Fig. 3.9 shows the 3D pinched hysteresis versus the parameter c where the symmetry line rotates as c increases from negative to positive values.

When $x(t) = cos(\omega t)$, the line $y = ax(t)$ is the symmetry line and the pinched point is given by $x_p = \frac{b\omega^2}{c}$, $y_p = \frac{ab\omega^2}{c}$, $x_p \leq 1$. Moreover, the hysteresis is always passing by the points $(1, a)$, $(0, y_o = \pm b\omega)$, and $(-1, -a)$ as shown in Fig. 3.10a. The existence of pinched and single loop can be controlled through the parameter b as shown in Fig. 3.10b. More cases are summarized in Fig. 3.11.

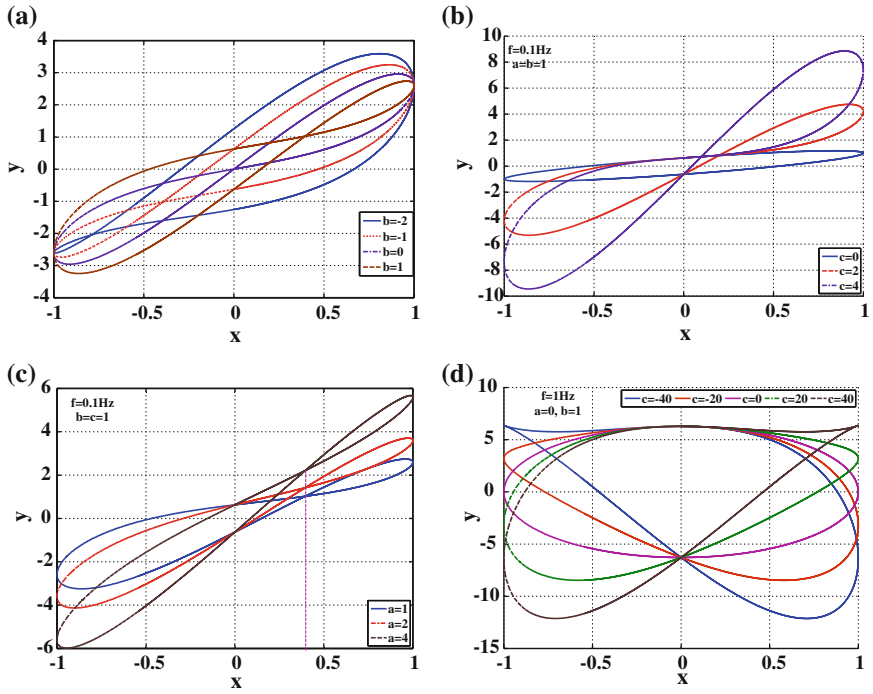

Fig. 3.8 x–y projection for the nonsymmetrical model

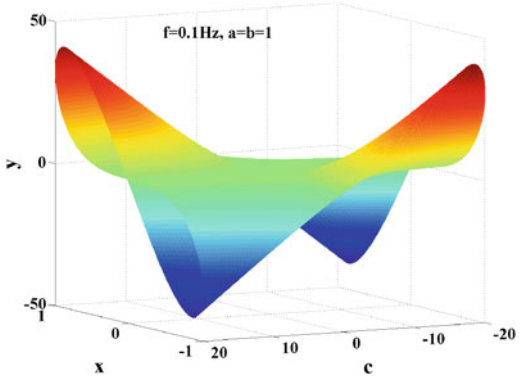

Fig. 3.9 The x–y projection rotation versus c when $x(t) = sin(\omega t)$

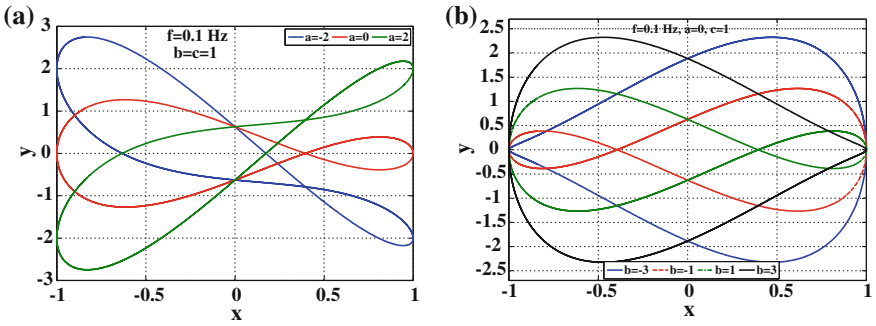

Fig. 3.10 The x–y projection when $x(t) = cos(\omega t)$

3.2.1 Experimental Results

The circuit of Fig. 3.5 was practically implemented as shown in Fig. 3.12a with $R_s = R_1 = 1\,\text{k}\Omega$ and with R_2 set as a $500\,\Omega$ variable resistor. The buffer sign was chosen to be $+1$ enabling a direct connection of the multiplier output to the noninverting input of U_1. The observed double-loop hysteresis is shown in Fig. 3.12b when $C = 1\,\mu\text{F}$ and the sinusoidal input voltage has a frequency $f = 150\,\text{Hz}$.

Note that the Y-axis in Fig. 3.12b is the voltage V_{out1} of the op amp U_1, which is also equal $-i_{in}R_1$. Similar double-loops were observed for ($C = 0.1\,\mu\text{F}$, $f = 2\,\text{kHz}$) and ($C = 2.2\,\text{nF}$, $f = 100\,\text{kHz}$) which confirm the persistence of the behavior over a wide range of input frequencies.

Figure 3.12c shows the experimentally observed nonsymmetrical loop after connecting the differentiator circuit, shown in a box within Fig. 3.12a, between the points labeled X and Y (i.e., across R_s). The selected values for the differentiator were $C_d = 10\,\mu\text{F}$, $R_{d1} = 200\,\Omega$, and $R_{d2} = 5\,\text{k}\Omega$.

Case		System	(x_p, y_p)	Boundary points	Symmetry line	Example ($\omega = 0.1$, $\varphi = \frac{\pi}{3}$)
1	$b = 0$ $d = 0$ $e = 0$	$y = ax + cx\int_0^t x(\tau)\,d\tau$	(0,0)	$(0,0)$, $\left(k, k\left(a + \frac{\cos(\phi)ck}{\omega}\right)\right)$ $\left(-k, -k\left(a + \frac{\cos(\phi)ck}{\omega}\right)\right)$	Odd symmetry $y = \left(a + \frac{ck\cos(\phi)}{\omega}\right)x$ $\Delta\left(\frac{y}{x}\right)_{max} = \frac{ck}{\omega}$	
2	$b = 0$ $c = 0$ $d = 0$	$y = ax + ex\frac{dx}{dt}$	(0,0)	$(0,0)$, (k, ak), $(-k, -ak)$	Odd symmetry $y = ax$ $\Delta\left(\frac{y}{x}\right)_{max} = e\omega k$	
3	$b = 0$ $d = 0$	$y = ax + cx\int_0^t x(\tau)\,d\tau + ex\frac{dx}{dt}$	(0,0)	$(0,0)$, $\left(k, k\left(a + \frac{\cos(\phi)ck}{\omega}\right)\right)$ $\left(-k, -k\left(a + \frac{\cos(\phi)ck}{\omega}\right)\right)$	Odd symmetry $y = \left(a + \frac{ck\cos(\phi)}{\omega}\right)x$ $\Delta\left(\frac{y}{x}\right)_{max} = k\left(e\omega - \frac{c}{\omega}\right)$	
4	$d = 0$ $e = 0$	$y = ax + b\frac{dx}{dt} + cx\int_0^t x(\tau)\,d\tau$	$x_p = \frac{b\omega^2}{c}$ $y_p = ax_p + \frac{\cos(\phi)dk}{\omega}$	$(0, \pm kb\omega)$, $\left(k, k\left(a + \frac{\cos(\phi)ck}{\omega}\right)\right)$ $\left(-k, -k\left(a + \frac{\cos(\phi)ck}{\omega}\right)\right)$	Non-symmetry $y \cong \left(a + \frac{ck\cos(\phi)}{\omega}\right)x$	
5	$c = 0$ $e = 0$	$y = ax + b\frac{dx}{dt} + d\int_0^t x(\tau)\,d\tau$	*No*	$\left(0, \frac{dk\cos(\phi)}{\omega} \pm k\left(b\omega - \frac{d}{\omega}\right)\right)$, $\left(k, k\left(a + \frac{d\cos(\phi)}{\omega}\right)\right)$, $\left(-k, -k\left(a - \frac{d\cos(\phi)}{\omega}\right)\right)$	Single loop $y \cong \frac{dk\cos(\phi)}{\omega} + ax$	
6	$b = 0$ $c = 0$	$y = ax + d\int_0^t x(\tau)\,d\tau + ex\frac{dx}{dt}$	$x_p = \frac{d}{e\omega^2}$ $y_p = ax_p + \frac{\cos(\phi)dk}{\omega}$	$\left(0, \frac{dk\cos(\phi)}{\omega} \pm k\frac{d}{\omega}\right)$, $\left(k, k\left(a + \frac{d\cos(\phi)}{\omega}\right)\right)$ $\left(-k, -k\left(a - \frac{d\cos(\phi)}{\omega}\right)\right)$	Non-symmetry $y \cong \frac{dk\cos(\phi)}{\omega} + ax$	

Fig. 3.11 Different cases for the model $y(t) = x(t)\left(a + c\int_0^t x(\tau)d\tau\right) + d\frac{dx(t)}{dt} + ex(t)\frac{dx(t)}{dt}$

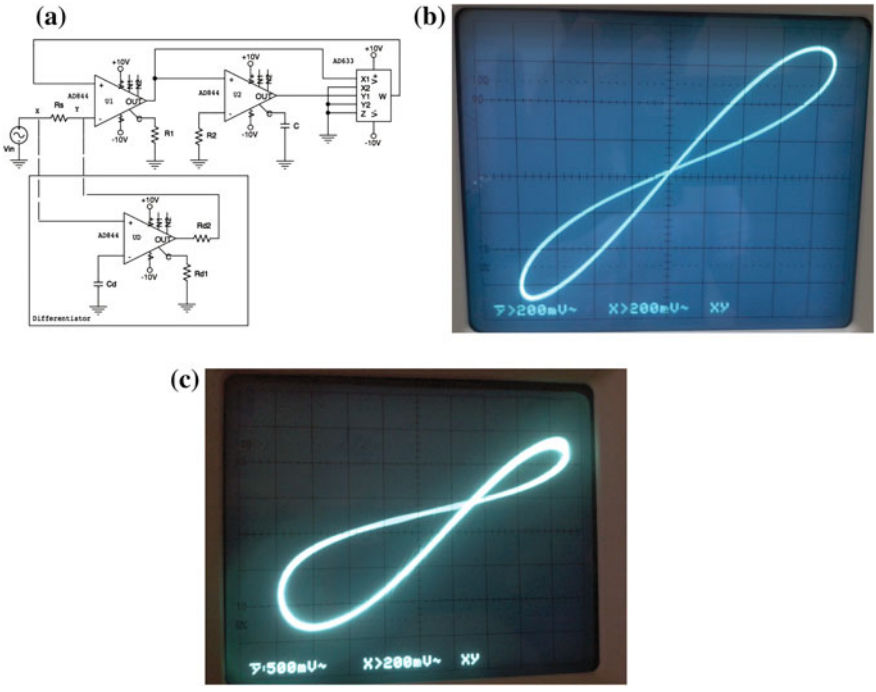

Fig. 3.12 Experimental results of a current-controlled memristor; **a** implemented circuit, **b** $V_{in} - V_{out1}$ showing a symmetrical-loop at $R_2 = 270\,\Omega$ and **c** $V_{in} - V_{out1}$ showing a nonsymmetrical loop after adding the differentiator subcircuit

3.3 Switching Model

From a circuit design perspective, reducing the complexity of implementing (3.12) requires finding an alternative to the analog multiplier block. A technique previously introduced in [8] implies replacing the multiplication function by a bipolar nonlinear switching function. Applying this technique to (3.12) yields the following model

$$y(t) = \pm a x(t) \pm b \begin{cases} x(t) & \int_0^t x(\tau)d\tau > c \\ -x(t) & \int_0^t x(\tau)d\tau \leq c \end{cases}. \tag{3.15}$$

The hysteresis loop is confined between the two lines $y = (\pm a \pm b)x$ and $y = (\pm a \mp b)x$. For memristive behavior, the condition $|b| < 1$ must hold. Figure 3.13 shows four different cases of (a, b) while Fig. 3.14 illustrates the effect of the phases ϕ on the x–y projection when the input $x(t) = sin(\omega t + \phi)$.

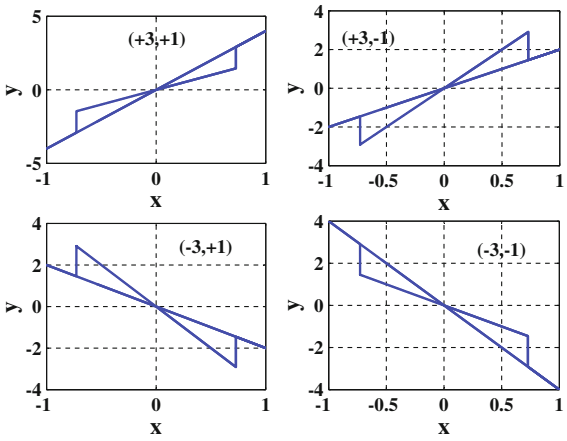

Fig. 3.13 The projection x–y for different values (a, b) with $c = 0.1$, $x(t) = sin(\omega t)$, and $\omega = 0.5$ rad/s

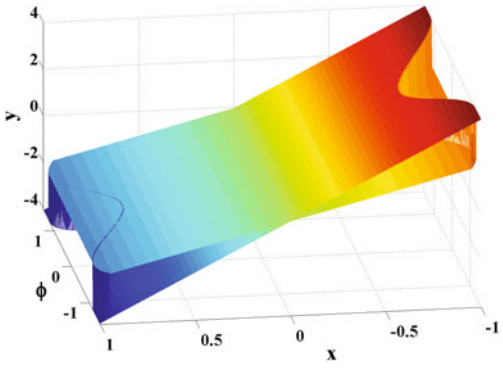

Fig. 3.14 The projection x–y versus ϕ with $c = 0.1$, $x(t) = sin(\omega t + \phi)$, and $\omega = 0.5$ rad/s

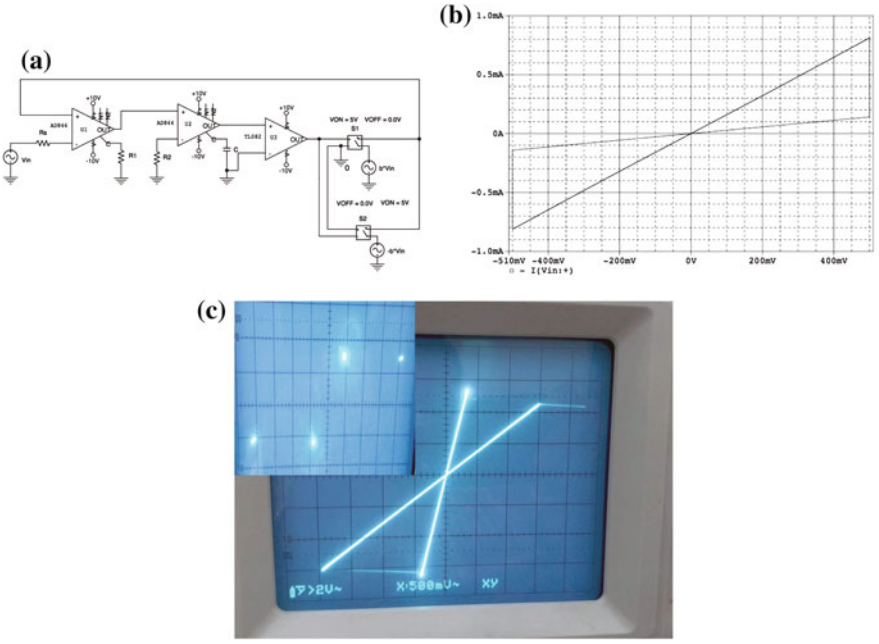

Fig. 3.15 Circuit realization of the double-loop switching model with Spice and experimental results

Figure 3.15a shows a circuit implementation using a comparator (op amp U_3) and two ideal switches (S_1 and S_2). A Spice simulation is shown in Fig. 3.15b with $R_s = R_1 = 1\,\text{k}\Omega$, $R_2 = 270\,\Omega$, $C = 1\,\mu\text{F}$, and $b = 0.7$. The experimentally observed loop is shown in Fig. 3.15c for the same component values, $R_2 = 100\,\Omega$ and the frequency of the sinusoid V_{in} set to 100 Hz. The switches were realized, respectively, with NMOS and PMOS transistors from an LM4007 chip while the two sources $\pm bV_{in}$ in Fig. 3.15a where obtained from V_{in} through simple inverting and noninverting op amp amplifiers. It is worth noting that these emulator circuits show nonvolatility so long as they are excited. This is experimentally verified through exciting Fig. 3.15a with a square wave input instead of the sinusoid. A typical 4-corner hysteresis loop (shown in the corner of Fig. 3.15a) is observed. With no excitation, the charge stored on the capacitor eventually disappears through the op amp output resistance and other leakage paths.

3.4 Fractional-Order Model

Modeling using the concept of fractional calculus penetrates the basic fundamentals of many applications due to its advantages and also since the conventional integer-order modeling is only a narrow subset of the fractional calculus. The main advantages of fractional-order modeling are its long memory dependency and also the ability to increase the degrees of freedom for the system through the added fractional-order parameters. Many ground rules in many applications have been generalized in the fractional-order sense such as in the control theory [9–11], circuit theory [12–15], special filters [16], synchronization [17], neuron systems [18], resonance [19], stability analysis [20–22], and in the fractional-order Smith chart [23, 24]. In the circuit theory, the fractional-order element (FOE) is considered as a generalized element that covers the conventional three passive elements which are inductor, resistor, and capacitor when the fractional-order parameter equals -1, 0, and 1 respectively. One of the realizations of the half-order capacitor can be obtained by dipping a capacitive-type probe, coated with a porous film of polymer of particular thickness, into a polarizable medium [25].

3.4.1 Fractional-Order Elements Relations

The fractional-order elements or constant phase elements (CFE) (like fractional-order capacitor (FOC) and fractional-order inductor (FOI)), which model the practical elements (frequency dependent losses), were introduced [26, 27]. Recently, fractional calculus is generalized and a mathematical paradigm is provided for describing the behavior of mem-elements with memory. Ohm's law is generalized and proved in case of fractional mem-element which is called memfractance [28].

The conventional elements are linked as shown in Fig. 3.16a where links (1), (2), and (3) represent R, L, and C; moreover, link (4) represents the memristor.

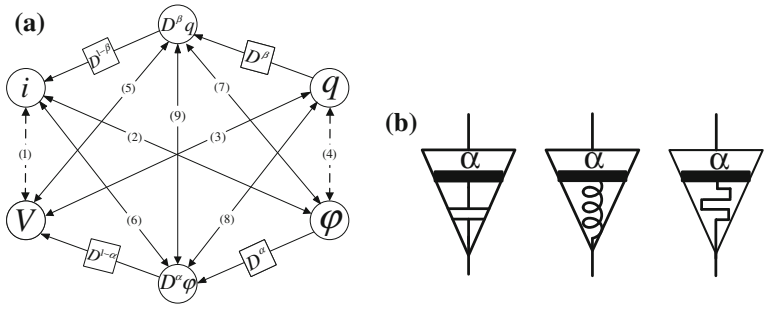

Fig. 3.16 **a** Fractional-order element relations, and **b** fractional-order capacitor, inductor symbol, and memristor symbols, respectively

The fractional-order capacitor (*FOC*) relates between the fractional derivative of the charge and the voltage which is represented in link (5) and link (8) with fractional-order $1-\alpha$ and α, respectively. Also, the fractional-order inductor (*FOI*) relates between the fractional derivative of the flux and the current which is represented in link (6) and link (8) with fractional-order $1-\alpha$ and α, respectively. So, the missing link is between the fractional-order derivative of charge and the fractional-order derivative of flux (link (9)) representing the fractional-order memristor (*FOM*). All the links are linear elements except link (4) and link (9) which are nonlinear elements.

Generally, the relation between any fractional-order derivative of charge $D^{\alpha}q$ and any fractional-order derivative of flux $D^{\beta}\varphi$ represents one of the elements R, L, C, M, *FoC*, *FOI*, and *FOM* depending on the resulting order and linearity between the elements. Also, this relation could be generalized to include memcapacitor and meminductor in addition to fractional-order memcapacitor (FOMC) and fractional-order meminductor (FOMI).

3.4.2 Fractional-Order Memristor Model

The fractional differential equation of memristor state [29, 30] can be given by

$$\frac{d^{\alpha}x}{dt^{\alpha}} = \pm k i(t) f(x). \tag{3.16}$$

By differentiating the memristance R_m, then

$$\frac{d^{\alpha}R_m}{dt^{\alpha}} = -R_d \frac{d^{\alpha}x}{dt^{\alpha}}. \tag{3.17}$$

Substituting by (3.17) into (3.16)

$$\frac{d^{\alpha}R_m}{dt^{\alpha}} = \mp k R_d i(t) f(x), \tag{3.18}$$

where R_d is the difference between R_{off} and R_{on}. For linear window function $f(x) = 1$ and substituting in (3.1)

$$R_m d^{\alpha} R_m = \mp k R_d v(t) dt^{\alpha}. \tag{3.19}$$

By integrating both sides,

$$J^{\alpha} R_m d^{\alpha} R_m = \mp k R_d J^{\alpha} v(t) dt^{\alpha}. \tag{3.20}$$

Using the basic definition of the fractional integral introduced by Riemann–Liouville [31], which was given by

$$J^{\alpha} f(t) = \frac{1}{\Gamma(\alpha)} \int_0^t (t-\tau)^{\alpha-1} f(\tau) d\tau. \tag{3.21}$$

Therefore, the left-hand side of (3.21) can be calculated by parts as follows:

$$\begin{aligned} L.H.S = J^{\alpha} R_m d^{\alpha} R_m &= \frac{1}{\Gamma(\alpha)} \int_{R_i}^{R_m} (R_m - R_i)^{\alpha-1} R dR \\ &= \frac{(R_m - R_i)^{\alpha}}{\Gamma(\alpha+1)} \left(R_i + \frac{Rm - R_i}{\alpha+1} \right). \end{aligned} \tag{3.22}$$

Substituting by (3.21) and (3.22) into (3.20), then the memristance is given by solving

$$(R_m + \alpha R_i)(R_m - R_i)^{\alpha} = \mp \alpha(\alpha+1) k R_d \int_o^t (t-\tau)^{\alpha-1} v(\tau) d\tau. \tag{3.23}$$

When the fractional-order memristor becomes a conventional memristor at $\alpha = 1$, then

$$R_m^2 = R_{in}^2 \mp 2k R_d \int_0^t v(\tau) d\tau = R_{in}^2 \mp 2k R_d \varphi(t), \tag{3.24}$$

where $\varphi(t)$ represents the flux. It is clear that the above equation gives the same results which are proposed in [32, 33]. In the next section, the step response of the memristor resistance will be discussed as follows:

3.4.3 Step Input Voltage

In case of applying step input voltage across the memristor the input signal is defined by

$$v(t) = V_{DC} u(t), \tag{3.25}$$

where $u(t)$ is the unit step function. By substituting from (3.25) into (3.24), then the resistance of the memristor is given by

$$(R_m + \alpha R_i)(R_m - R_i)^{\alpha} = \mp(\alpha+1) k R_d V_{DC} t^{\alpha}. \tag{3.26}$$

The positive or negative sign in (3.26) discusses the polarity effect for both the memristor and the applied voltage V_{DC}; consequently, two cases will be discussed in the following subsections.

The memristor circuit is connected as shown in Fig. 3.17 where the positive of the supply is connected to the negative of the memristor then the resistance of the memristor is given by:

$$(R_m + \alpha R_i)(R_m - R_i)^{\alpha} = (\alpha + 1) k R_d V_{DC} t^{\alpha}. \tag{3.27}$$

It is clear from the previous equation that the resistance of the memristor increases from the initial value until it reaches its maximum R_{off} in a certain time period which is called the saturation time t_{sat}. Figure 3.18a shows the memristor behavior when the applied step input voltage and the memristor parameters μ_v, D, V_{DC}, R_{off}, R_{on} are equal to $10^{-10}\,\mathrm{cm^2\,s^{-1}\,V^{-1}}$, 10 nm, 1 V, 38 kΩ, 100 Ω, respectively, for different values of α. From Fig. 3.17b, the saturation time depends on the value of the fractional-order α where the saturation time increases as α increases for certain V_{DC}.

The general formula of the saturation time t_{sat} in the fractional-order case at which the memristor resistance increases from its initial value R_{in} up to R_{off} is given by:

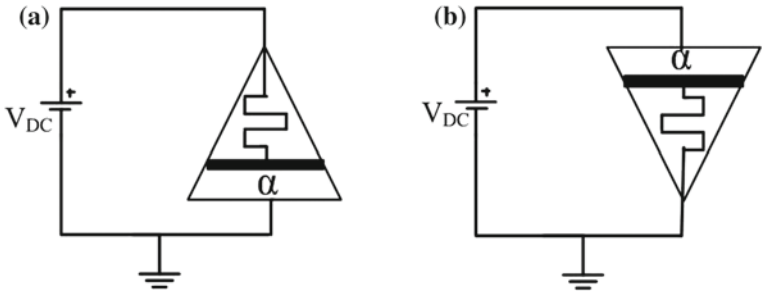

Fig. 3.17 Memristor configurations with the input voltage

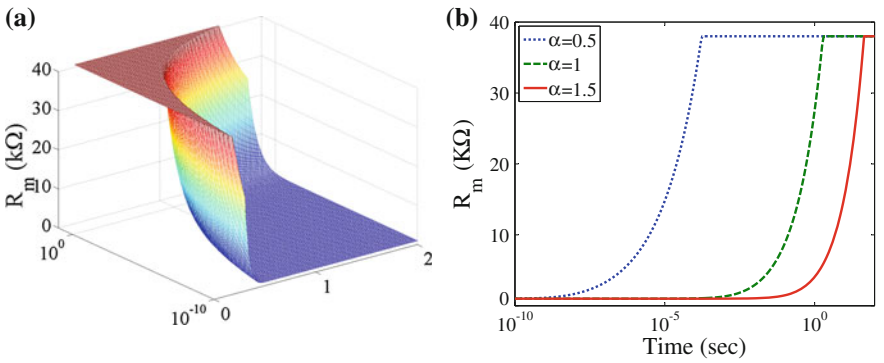

Fig. 3.18 **a** Memristor resistance versus α and time, and **b** memristance versus time for different α

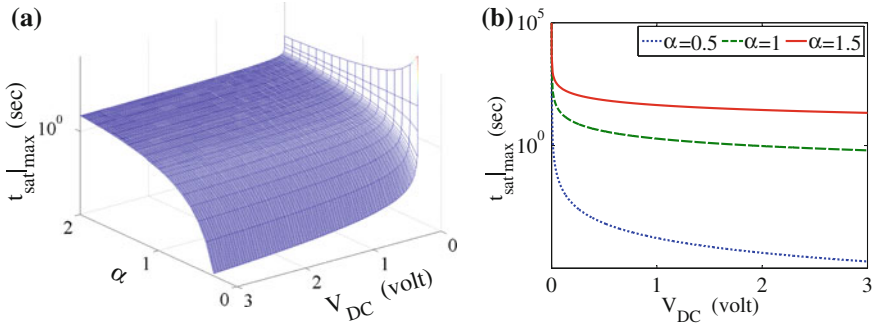

Fig. 3.19 **a** Saturation time versus α and V_{DC}, and **b** saturation time versus V_{DC} for different α

$$t_{sat} = (R_{off} - R_i)\left(\frac{R_{off} + \alpha R_i}{(\alpha + 1)k R_d V_{DC}}\right)^{1/\alpha}. \tag{3.28}$$

The maximum saturation time can be obtained when $R_{in} = R_{on}$ as follows:

$$t_{sat_{max}} = R_d\left(\frac{R_{off} + \alpha R_{on}}{(\alpha + 1)k R_d V_{DC}}\right)^{1/\alpha}. \tag{3.29}$$

For the conventional model of the memristor $\alpha = 1$, the saturation time will be reduced to the formula given in [32, 33].

The saturation time surface as a function of the $\alpha - V_{DC}$ plane and three different cases of $\alpha = 0.5$, 1, and 1.5 are shown in Fig. 3.19a, b, respectively. It is clear from the above response that the saturation time can be controlled through the fractional-order where it can be less than 1 sec when $\alpha < 0.5$ up to higher values when $\alpha > 0.5$. It is worthy to note that the memristor will act as a linear resistor as α tends to 0 with resistance R_{in}.

3.4.4 Sinusoidal Input

The applied voltage to any circuit can be represented by sinusoidal signals using Fourier series. For a single sinusoidal input which is given by $v(t) = V_o sin(2\pi f t)$ or $v(t) = V_o cos(2\pi f t)$ for $t > 0$. The fractional integration of sinusoidals is given by

$$J^{\alpha} sin(2\pi f t) = \frac{2\pi f t^{\alpha+1}\,{}_1F_2\left[1; 1 + \frac{\alpha}{2}, \frac{3+\alpha}{2}; -\pi^2 f^2 t^2\right]}{\Gamma(\alpha + 2)}, \tag{3.30a}$$

$$J^{\alpha} cos(2\pi f t) = \frac{t^{\alpha}\,{}_1F_2\left[1; \frac{1+\alpha}{2}, 1 + \frac{\alpha}{2}; -\pi^2 f^2 t^2\right]}{\Gamma(\alpha + 1)}. \tag{3.30b}$$

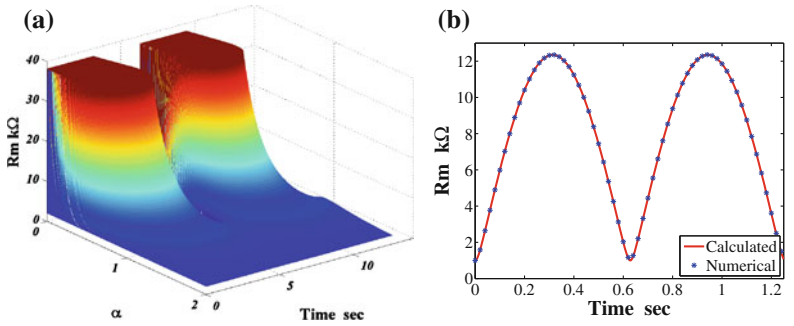

Fig. 3.20 **a** Numerical transient simulation for changing α, and **b** matching with conventional case $\alpha = 1$

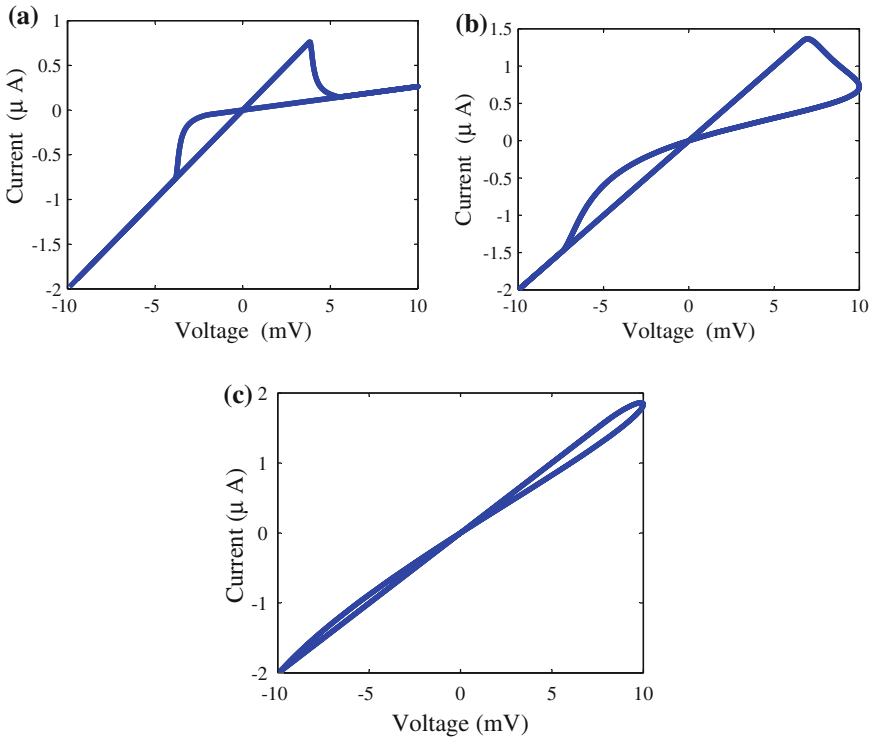

Fig. 3.21 Numerical simulation of I–V hysteresis at **a** $\alpha = 0.25$, **b** $\alpha = 0.5$, and **c** $\alpha = 0.7$

The memristance should be enclosed between the minimum resistance R_{on} and the maximum resistance R_{off}, so for $v(t) = V_o sin(2\pi f t)$, the memristance is given by

$$(R_m + \alpha R_i)(R_m - R_i)^{\alpha} = \mp 2\pi k f R_d V_o t^{\alpha+1}{}_1F_2\left[1; \frac{\alpha+2}{2}, \frac{\alpha+3}{2}; -\pi^2 f^2 t^2\right], \tag{3.31}$$

For the integer case at $\alpha = 1$, which gives the same results as in [33]. The resistance of the memristor is given by

$$R_m = \sqrt{R_{in}^2 \pm 4k R_d \frac{V_o}{\omega_o} \sin^2\left(\frac{\omega_o t}{2}\right)}. \tag{3.32}$$

Figure 3.20a shows a numerical simulation for changing fractional-order α for sinusoidal input $v_{in} = 0.1sin(t)$. Moreover, Fig. 3.20b shows matching between the general case and the conventional case for $\alpha = 1$ for $v_{in} = sin(10t)$. The effect of changing the fractional-order is clear as depicted in Fig. 3.21 for $V_o = 10mV$, $f = 1\text{Hz}$, $k = 10^4$, $R_{on} = 100\Omega$ and $R_{off} = 38k\Omega$.

3.5 Memristor Emulation Circuits for Analog Applications

Due to the lack of memristor samples, researchers tend to use emulators which emulate the behavior of the mem-elements. The previous emulators depend on the commercial off-shelf components which are implemented using op amps, multipliers, NMOS, and PMOS transistors [1, 34].

3.5.1 Simple COTS Realization of Floating Memristor

3.5.1.1 Memductor Model

The current-controlled memristor model was discussed in [4] where the constitutive relationship between the charge q, flux-linkage φ, and the memristance is a function of the state variable, current, and time. In contrast, the model of the memductor was discussed in [35] where memductance is a function of flux φ and the change rate of memductance G_m is given as follows:

$$\dot{G}_m(\varphi) = \alpha H(\varphi) v_m, \tag{3.33}$$

where $H(\varphi)$ is considered as a normalized window function having the nonidealities of the memductance change rate. For the sake of simplicity, let us assume that $H(\varphi) = 1$ representing the linear model of the memductor as discussedin [36]. By integrating

both sides relative to time, the memductance is given by

$$G_m = G_{mo} + \alpha\varphi(t), \tag{3.34}$$

where G_{mo} is the initial memductance. The memductance is linearly proportional to the flux. Moreover, in [1], the authors introduced a simple model for a double hysteresis model for the mem-elements where the voltage-controlled memductor equation is given by

$$i_m = G_s v_m + \frac{G_s v_m}{T V_{ref}}\varphi(t), \tag{3.35}$$

where G_s is the initial transconductance, T is the integration factor, and V_{ref} is an arbitrary reference. So the memductance is given by

$$G_m = G_s + \frac{G_s}{T V_{ref}}\varphi(t). \tag{3.36}$$

As is obvious, both models give the same modeling equation for the memductor where $\alpha = G_s/(T V_{ref})$.

Numerical simulations upon changing different parameters of the memductor are shown in Figs. 3.22 and 3.23 of the sinusoidal input voltage $v(t)$ with 1 V amplitude. Figure 3.22a shows the IV characteristics of the memductor for three different frequencies where the area inside the hysteresis loops decreases by increasing the input frequency. Moreover, Fig. 3.22b shows the IV characteristics for three different values of α. Also, the hysteresis loop sizes are dependent on the value of α, where upon decreasing α, the hysteresis loops decrease until α tends to zero and the memductance tends to its initial value G_{mo}. The maximum obtained memductance G_m where the memductance changes from G_{mo} to maximum G_m, shown in Fig. 3.23, plotted for the range of α spanning from 0.001 to 0.1 and for the frequency range from 0.01 to 100 Hz of the input signal.

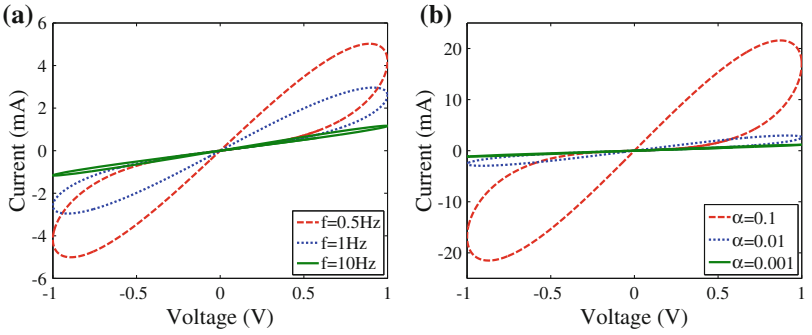

Fig. 3.22 I–V hysteresis of the memductor for $G_{mo} = 1\,\text{m}\mho$ for different **a** frequencies at $\alpha = 0.01$, and **b** α at 1 Hz frequency

In order to implement the memductor whose memductance varies and is controlled by the flux linkage. Therefore, a voltage-controlled transconductance is needed in addition to a differential voltage integrator to integrate the voltage across the transconductance and generate the flux which controls the transconductance as shown in Fig. 3.24.

Moreover, the nonideal model of the memductor can be implemented by adding a window function $H(\varphi)$ after the integrator to reshape the control voltage and boundary effect to the model.

3.5.1.2 Circuit Realization

The voltage-controlled transconductance is implemented using LM13700 [37] which is connected as shown in Fig. 3.25 to implement a floating voltage-controlled transconductance G_m which is proportional to the control voltage V_c and its transconductance is given by

$$G_m = 9.6\, I_{ABC} \frac{R_A}{R}, \tag{3.37}$$

where I_{ABC} represents the transconductance amplifier bias current. From the PSPICE simulation, it is found that I_{ABC} is linearly proportional to the control voltage ($I_{ABC} = aV_c + I_o$) where a represents the reciprocal of the control resistance R_c and I_o is the initial current. The data sheet of the transconductance [37] states that it is recommended to use $R_c = 15\,\text{k}\Omega$ and as a result the corresponding initial current $I_o = 905.057\,\mu\text{A}$. Substituting I_{ABC} into (3.37), the transconductance G_m is given by

$$G_m = \frac{0.64 R_A}{R} V_c + 8.6885 \frac{R_A}{R}\ (\text{m}\mho). \tag{3.38}$$

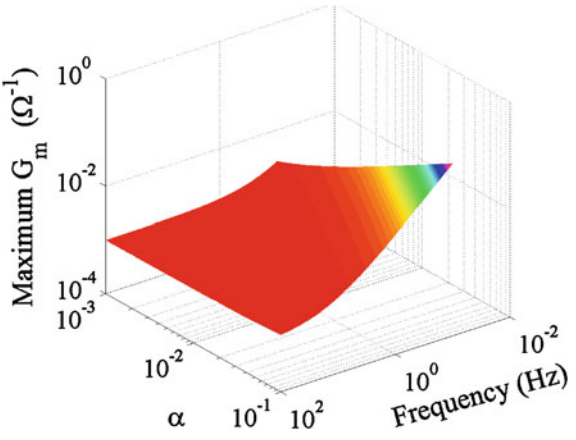

Fig. 3.23 The maximum memductance for different frequencies and α

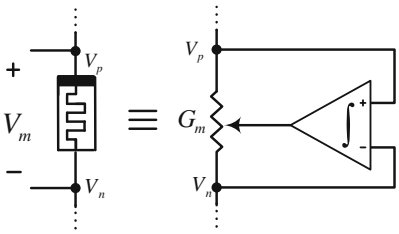

Fig. 3.24 Behavioral model of linear memductor

By comparing (3.34) and (3.34), the control voltage V_c should represent the flux linkage of the memductor. The flux linkage can be obtained by integrating the difference voltage of the memductor terminals (V_p, V_n) and is given as follows:

$$V_c = \frac{1}{R_1 C_1} \int_{-\infty}^{t} (V_p - V_n) d\tau = \frac{1}{R_1 C_1} \varphi_{pn}(t) \tag{3.39}$$

The integrator circuit is built as shown in Fig. 3.26, where an inverting integrator is used and two buffer amplifiers to prevent the loading effect of the integrator on the transconductance circuit. By substituting into G_m, the transconductance is given by

$$G_m = 0.64 \frac{R_A}{R R_1 C_1} \varphi(t) + 8.6885 \frac{R_A}{R} \text{ (m℧)}. \tag{3.40}$$

The previous equation emulates the memductors equation where $G_{mo} = 8.6885 \frac{R_A}{R}$ (m℧) and $\alpha = 0.64 \frac{R_A}{R R_1 C_1}$ (m).

3.5.1.3 Experimental Results

The circuit is practically assembled on a printed circuit board using LM13700 and TL084 (Opamp) shown in Fig. 3.27 where C_1, R_1, R, and R_A equal 1 μF, 1 kΩ,

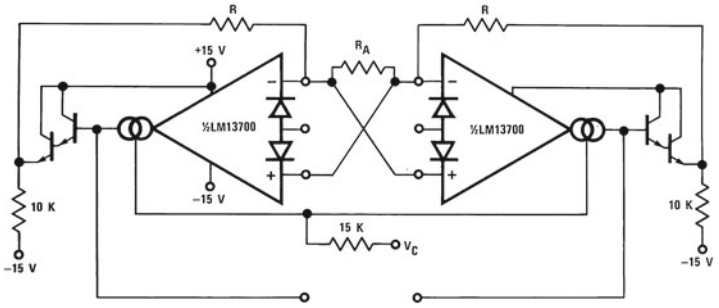

Fig. 3.25 Floating voltage-controlled transconductance implementation using LM13700

100 kΩ, and 10 kΩ, respectively. The emulator is tested using NI ELVIS Kit and the voltage results are taken to MATLAB to plot current–voltage hysteresis (as NI ELVIS does not plot hysteresis curves X-Y). In order to obtain the input current to the emulator, series resistor is connected where the input current is proportional to the voltage difference across it with gains equal to the inverse of this resistor; so in the following results, a 1 kΩ resistor is used.

In case of the memductor series with a resistor R, the voltage across the memductor $v_m = V_{in}/(1+G_m R)$ where v_{in} is the input voltage, and G_m is the memductance. By substituting into (3.34), integrating both sides, and simplifying the resulting equation. The memductance is given as follows:

$$G_m = -\frac{1}{R} + \sqrt{\left(\frac{1}{R} + G_{mo}\right)^2 + \frac{2\alpha}{R}\varphi(t)}. \tag{3.41}$$

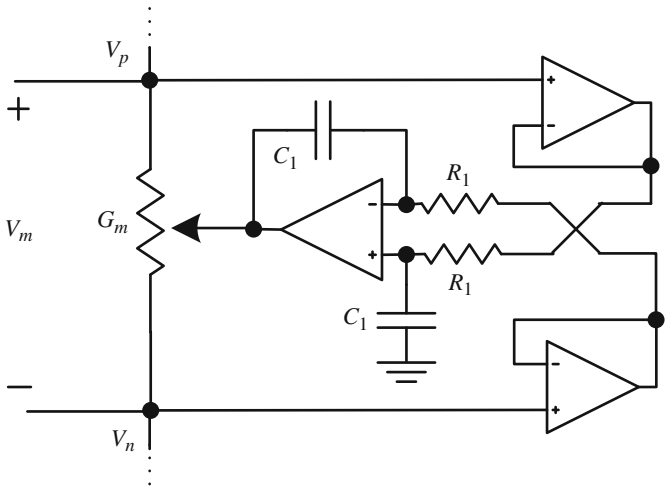

Fig. 3.26 Generation of the flux control circuit of the memductor

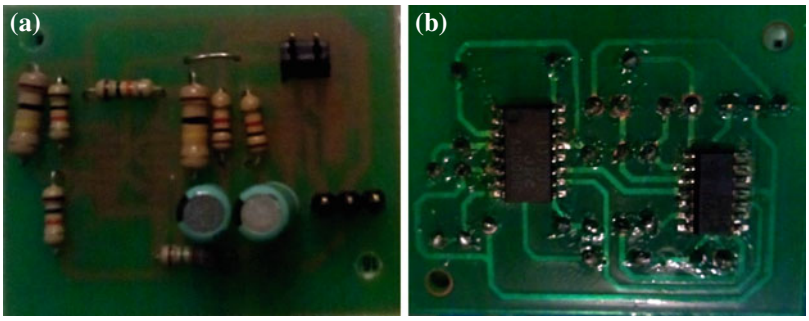

Fig. 3.27 Printed circuit board of voltage-controlled memristor emulator

In case of applying a sinusoidal signal $v(t) = A_o \sin(\omega t)$, the flux is given by

$$\varphi(t) = \frac{2A_o}{\omega} \sin^2\left(\frac{\omega}{2}t\right) + \varphi_o. \tag{3.42}$$

Moreover, in the case of square signal with A_1 amplitude for positive half cycle, A_2 amplitude for negative half cycle and zero DC term, the flux is given by

$$\varphi(t) = \varphi_o + \begin{cases} A_1\tau & \tau \leq T_h \\ (A_1 + A_2)\tau - A_2 T_h & T_h < \tau \leq T \end{cases} \tag{3.43}$$

where $\tau = mod(t, T)$. These equations gives similar results to the experimental results using appropriate values of G_{mo} and α.

This emulator was tested using different voltage excitation signals [36]: sinusoidal signal with frequency 10 and 50 Hz, square wave signal with frequency 10 Hz and triangular wave signal with frequency 10 Hz. Figure 3.28a, b show the transient voltage (blue line) and current (green line) of the emulator for sinusoidal signal with amplitude 1 V, also Fig. 3.28c, d show the corresponding double-loop pinched I–V hysteresis of the memductor which decreases with increasing the input frequency. Also a square wave signal with amplitude ±0.5 V with 10 Hz frequency is applied

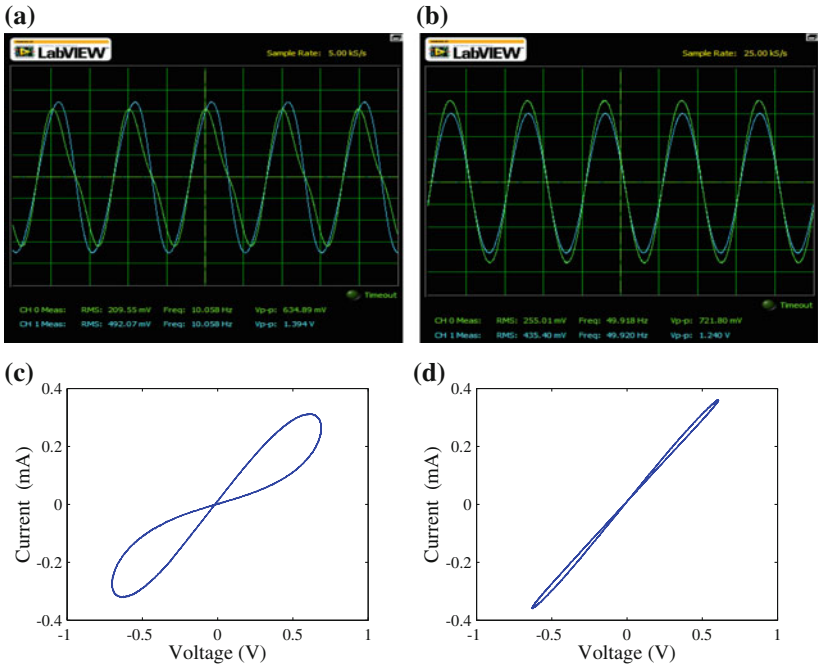

Fig. 3.28 Emulator response under sinusoidal signal at frequency 10 and 50 Hz

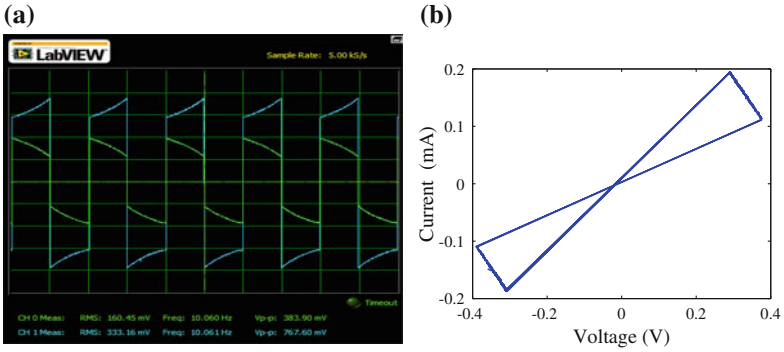

Fig. 3.29 Emulator response under square wave signal at frequency 10 Hz, **a** transient voltage and current, and **b** I–V hysteresis

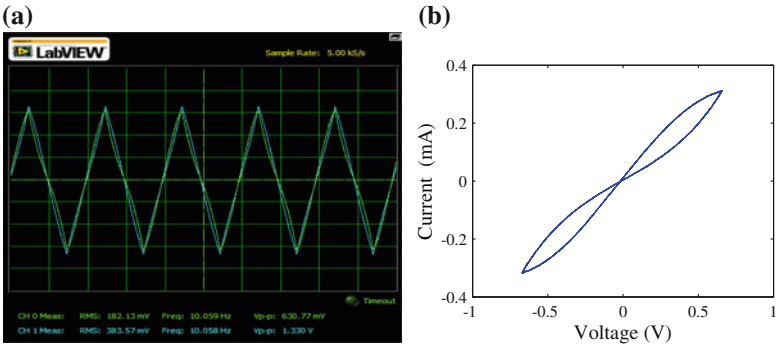

Fig. 3.30 Emulator response under triangular wave signal at frequency 10 Hz, **a** transient voltage and current, and **b** I–V hysteresis

and the transient voltage (blue line) and current (green line) shown in Fig. 3.29 which a high functionality of the emulator to be used in a memristor-based relaxation oscillator. The voltage across the memductor increases for positive pulse and decreases for negative pulse so the memductance decreases and increases for positive and negative pulses, respectively. Moreover, Fig. 3.30 shows the response of the triangular wave excitation with amplitude ± 1 V with 10 Hz frequency and I–V hysteresis in case of triangular excitation.

3.5.2 MOS Realization of Memristor Emulator

Although, the MOS realization of the memristor is discussed in [38], it was implemented by four differential difference current conveyors (DDCC) as an integrator, squarer, multiplier, and summer. This subsection discusses a recent emulator

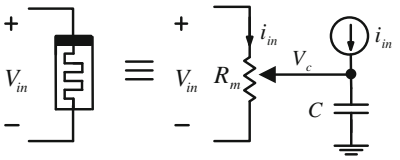

Fig. 3.31 The idea of the memristor emulator

which is implemented using only a voltage-controlled resistor (VCR) and one second generation current conveyor (CCII) which has a smaller size and is more reliable [39].

3.5.2.1 Mathematical Model

Different modeling equations of the memristor were introduced in [40]. In HP's lab model, the rate of change in the memristance was given by

$$\frac{dR_m}{dt} = k_m i(t). \tag{3.44}$$

By integrating both sides, the memristance is given by:

$$R_m(t) = R_o + k_m q(t), \tag{3.45}$$

where R_o is the initial memristance. According to the previous equation, the memristor can be defined as a variable resistor and its value depends on the charge passing through it so it can be emulated by a voltage-controlled resistor (VCR) where the control voltage is proportional to the passing charge. The control voltage V_c is generated by mirroring the current passing through VCR and imposing it into a capacitor so the voltage across the capacitor is the required control voltage $V_c = q_{in}/C$ as shown in Fig. 3.31.

For the practical realization of VCR, it can be realized using a MOS transistor working in the triode region where transconductance is proportional to gate voltage. Moreover, a simple model of double-loop hysteresis of a memristive element is discussed in [1] which is applied for memristance and transconductance which is given by

$$G_m(t) = G_o + k'_m q(t), \tag{3.46}$$

where G_o is the initial transconductance and k'_m ($\Omega^{-1}\,\mathrm{C}^{-1}$) is the transconductance mobility constant.

3.5.2.2 Mos Realization

This emulator was implemented using VCR and CCII+ which is used to mirror the current passing through the VCR to create the control voltage V_c as shown in

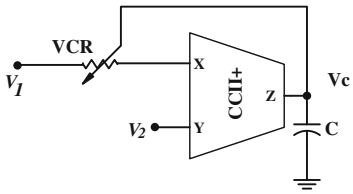

Fig. 3.32 The emulator circuit

Fig. 3.32. In the following subsections, the realization of VCR and CCII will be discussed and used in the memristor emulator.

CCII Implementation

The second generation current conveyor is a three-terminal active circuit (X, Y, Z). The input–output relation of CCII could be described by the following equation.

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \tag{3.47}$$

The relation between the current of the X terminal and the Z terminal depends on the type of CCII, where a positive sign is related to the noninverting type (CCII+), and a negative sign is related to the inverting type (CCII−).

Several literatures have been published in this topic to enhance current and voltage transfer accuracy, increase output current capability, or implement a rail-to-rail

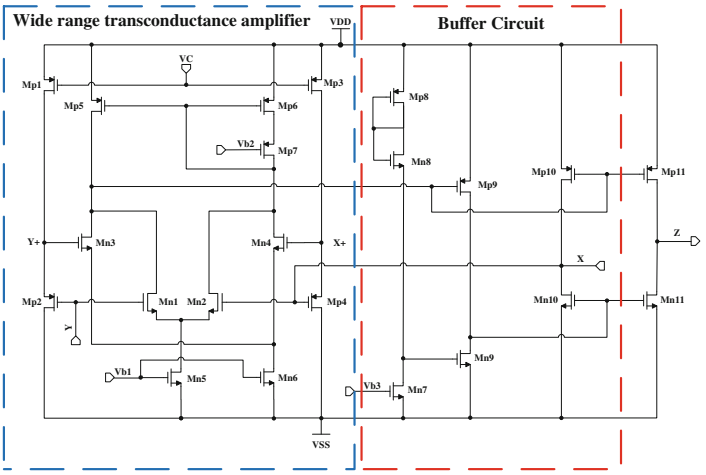

Fig. 3.33 Wide range CCII+ implementation

Table 3.1 Transistors aspect ratios of CCII+

Transistors	W (μm)	L (μm)
Mn1–Mn4	20	1
Mn5–Mn6	30	2
Mn7–Mn9	4	0.5
Mn10–Mn11	120	1.5
Mp1–Mp4	3	0.5
Mp5–Mp6	90	2
Mp7	90	0.35
Mp8–Mp10–Mp11	140	2
Mp9	4	0.5

CCII using complementary differential pairs [41]. Nevertheless, the previous architectures suffer from some drawbacks such as increasing power consumption and large transconductance variation. A modified structure has been proposed in [42] and used in the implementation of this circuit to overcome the aforementioned drawbacks. In addition, the presented structure can operate under a minimum supply voltage and reduce offset voltage between X and Y terminals.

The complete MOS realization of CCII+ is shown in Fig. 3.33, the input stage is a wide range differential input transconductance amplifier (Mn1–Mn6), (Mp1–Mp7) to extend the region of operation up to rail-to-rail, and to improve bandwidth of input stage [42]. Moreover, the buffering circuit (Mn7–Mn10), (Mp8–Mp10) was used to ensure low input impedance at the X terminal and to provide rail-to-rail swing capability.

Using the circuit analysis presented in [42], it was proven that $V_X = V_Y$ and $I_X = I_Z$ such that a current follower stage (Mn11, Mp11) has been added to convey the current pass through the X terminal to Z terminal.

CCII+ was implemented using TSMC 0.13 μm technology; the aspect ratios of transistors are given in Table 3.1; it was selected to enhance linearity performance and to alleviate the offset in voltage and current results from channel length modulation effect.

VCR Implementation

Variable resistor, especially voltage control resistor (VCR), is an essential element in different electronic circuits such as the variable gain amplifier and signal generators. A floating voltage control resistor is implemented using the circuit proposed in [43] to ameliorate linearity and dynamic range of VCR. As shown in Fig. 3.34, VCR consists of two operational amplifiers, six resistors (100 kΩ), two capacitors, and an NMOS transistor that operates in the triode region. The drain current of enhancement-type NMOS transistor (MN1) which operates in the triode region is $I_{ds} = \beta(V_{gs} - V_{th} - \frac{V_{ds}}{2})V_{ds}$ where $\beta = \mu_n C_{ox} \frac{W}{L}$, μ_n is the mobility of electrons; C_{ox} is the oxide

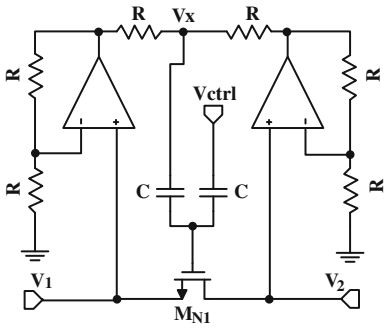

Fig. 3.34 Implementation of floating voltage-controlled resistor

capacitance per unit area; V_{th} is the threshold voltage of NMOS transistor; and W and L are width and length of the bypass transistor respectively.

From the analysis of the VCR circuit, $V_x = V_1 + V_2 = V_{ds}|_{MN1} + 2V_s|_{MN1}$. Moreover, by adding two capacitors with the same value ($C_1 = C_2 = C = 2pF$), a floating gate technique can be implemented [43]. The gate voltage of bypass transistor $V_g = 0.5(V_x + V_{ctrl})$ where V_{ctrl} is the control voltage. As a result, the gate source voltage of bypass transistor (M_{N1}) is

$$V_{gs} = \frac{1}{2}(V_{ds} + V_{ctrl}). \tag{3.48}$$

By substituting into the drain current's equation, the drain current of bypass transistor can be calculated as follows:

$$I_{ds} = \beta\left(\frac{V_{ctrl}}{2} - V_{th}\right)(V_1 - V_2). \tag{3.49}$$

The current passing through bypass transistor is linearly proportional to the applied voltage. Furthermore, the equivalent resistance of bypass transistor $R_{VCR} = 2/\beta(V_{ctrl} - 2V_{th})$. The equivalent resistance is independent on the input voltage or the output voltage; moreover, it is proportional to the control voltage. However, to ensure the linearity of the VCR, the bypass transistor should operate in the triode region so $V_{ctrl} \geq V_{ds} + 2V_{th}$. This condition can be satisfied by choosing appropriate values for the aspect ratio.

Mathematical Model

Using the designed VCR and CCII to implement the emulator shown in Fig. 3.32. The current passing through VCR is given by:

$$I = \beta\left(\frac{V_{ctrl}}{2} - V_{th}\right)(V_1 - V_2). \tag{3.50}$$

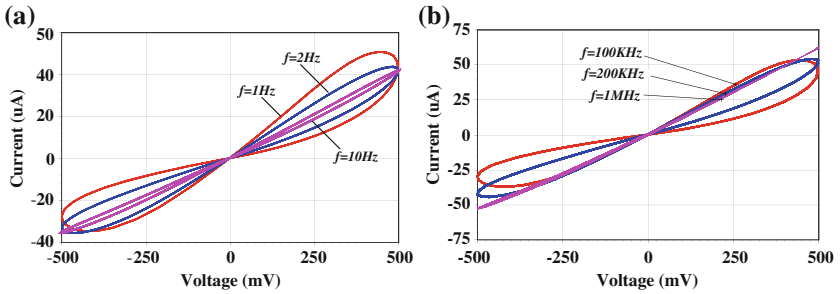

Fig. 3.35 I–V pinched hysteresis of the emulator: **a** $C = 10\,\text{uF}$, and **b** $C = 100\,\text{pF}$

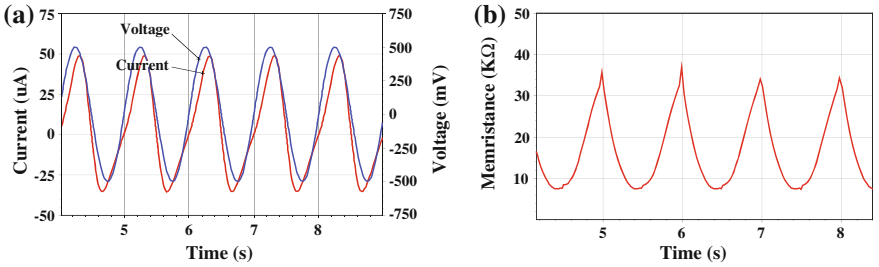

Fig. 3.36 Transient response of the emulator for sinusoidal input at 1 Hz. **a** Instantaneous current passing through memristor, and **b** Instantaneous memristance

The control voltage $V_{ctrl}(t) = q(t)/C$ where $q(t)$ is the time integral of the passing current through VCR. So the transconductance of VCR is given as follows:

$$G_m = \frac{\beta q(t)}{2C} - G_{mo}, \tag{3.51}$$

where G_{mo} is the initial transconductance and is given by $G_{mo} = \beta V_{th}$. The rate of change in the transconductance is proportional to the passing current and is given by

$$\frac{dG_m}{dt} = \frac{\beta}{2C} i(t) = k'_m i(t). \tag{3.52}$$

This circuit is designed using TSMC 0.13 µm technology with dual supply ±1.5 V. Figure 3.35a, b shows I–V pinched hysteresis of the designed emulator for $\beta = 138.74\,\mu\text{A/V}^2$ for $C = 10\,\mu\text{F}$ and $C = 100\,\text{PF}$, respectively. From (3.52), the speed of this emulator is controlled by the aspect ratio of the bypass transistor and integrating capacitor value C. The working frequency range is scaled by the same scaling factoras that of the capacitor as shown in Fig. 3.35. Also, a variable capacitor can be used to tune the emulator to work in any desirable frequency range.

Figure 3.36a, b shows the instantaneous memristance and current passing through the circuit for applied voltage $v(t) = 0.5\sin(2\pi t)$ V where the memristance changes from around 7–35 kΩ.

3.5.2.3 Testing Applications

One of the recent applications of the memristor is to design relaxation oscillators by replacing the capacitor with memristors as discussed in [44, 45] which can also be used as a voltage-controlled oscillator [46, 47]. The memristor is used to emulate the effect of charging and discharging of capacitor voltage where memristance increases or decreases depending on the polarity of the applied voltage. The previous emulator is used in the relaxation oscillator, shown in Fig. 3.37, instead of solid-state memristor.

Using the same procedure used in [44] to derive expressions for oscillation frequency and conditions for oscillation, the current passing through memristor $i(t) = G_m(V_o - V_{ref})/(G_m R_a + 1)$. By substituting into (3.52) and integrating from G_{mn} to G_{mp} which are the transconductances corresponding to V_n and V_p, respectively, during the positive time half cycle T_h is given by

$$T_h = \frac{R_a(G_{mp} - G_{mn}) + \ln(\frac{G_{mp}}{G_{mn}})}{k'_m(V_{oh} - V_{ref})}, \tag{3.53}$$

where G_{mp} and G_{mn} are given by

$$G_{mp} = \frac{1}{R_a}\frac{V_{oh} - V_p}{V_p - V_{ref}}, G_{mn} = \frac{1}{R_a}\frac{V_n - V_{ol}}{V_{ref} - V_n}. \tag{3.54}$$

A similar expression can be obtained for negative time half cycle T_l so the oscillation frequency $f_o = D/T_h$ where $D = (V_{oh} - V_{ol})/(V_{ref} - V_{ol})$. The condition for oscillation is obtained from $G_{mp} > G_{mn}$ and is given by

$$V_{ref} > \frac{V_{oh}V_n - V_{ol}V_p}{V_{oh} - V_p - V_{ol} + V_n}. \tag{3.55}$$

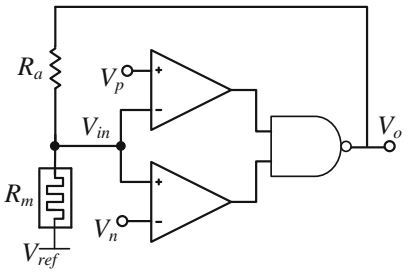

Fig. 3.37 Memristor-based voltage-controlled relaxation oscillator

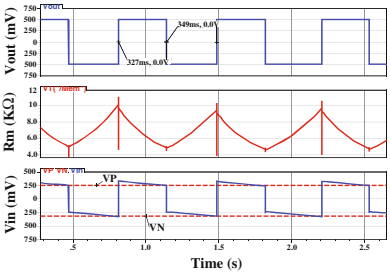

Fig. 3.38 Transient simulation results for V_o (*upper*), R_m (*middle*), and V_{in} (*lower*)

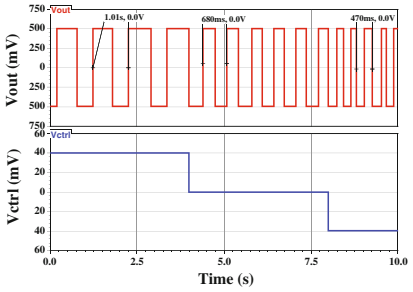

Fig. 3.39 Transient simulation of voltage-controlled oscillator

Figure 3.38 shows the transient simulation of relaxation oscillator using this emulator for V_p, V_n, V_{oh}, V_{ol}, V_{ref}, and R_a equal 0.25 V, −0.325 V, 0.5 V, −0.5 V, 0 V, and 5 kΩ where the emulator is designed using $C = 10\,\mu$F and $\beta = 138.74\,\mu\text{A/V}^2$. The time of positive half cycle equals 327 ms with relative error to the calculated value equals 4.9759 percent due to nonlinearity of VCR. The circuits oscillate with the frequency equal 1.47 Hz and the memristance changes from 5 to 9.2857 kΩ.

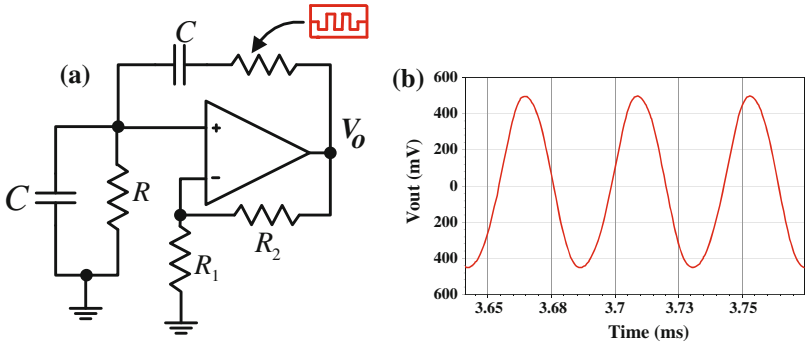

Fig. 3.40 **a** Memristor-based Wien oscillator circuit, and **b** Transient output of Wien oscillator

By controlling V_{ref} of memristor-based relaxation oscillator, the frequency changes depending on the value of V_{ref}. As obvious from Fig. 3.39, the oscillator output frequencies are 0.99, 1.47, and 2.127651 Hz for $V_{ref} = 40\,\text{mV}, 0\,\text{V}$ and $-40\,\text{mV}$ using the same aforementioned parameter values.

Also the emulator is tested in Wien oscillator where the feedback resistor is replaced with a memristor as discussed in [48–50] and shown in Fig. 3.40a. The circuit oscillates with a frequency equal to 22.6757 kHz for C, R, R_1, and R_2 equal to 1 nF, 10 kΩ, 1 kΩ, and 2 kΩ, respectively. Moreover, the memristance changes from 4.416 to 6.458 kΩ as shown in Fig. 3.40b.

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Chapter 4
Memristor-Based Relaxation Oscillator Circuits

Oscillators are the key component in electronic systems since there is always a need for a repetitive signal with a given frequency and waveform for timing, modulation, and test and measurement applications [1]. Oscillators circuits are designed to produce a repetitive, oscillating signal, often a sine wave or a square wave. The two main types of oscillators are sinusoidal and relaxation oscillators. Sinusoidal oscillators are based on positive feedback, where a frequency selective network is used to determine the frequency of oscillation of the sinusoidal output. Relaxation oscillators are used to produce square waves, pulses, and triangular waves. Square waves are one of the most important signals in digital applications. Relaxation oscillator is basically an astable multivibrator which is an electronic circuit that operates between two quasi-stable states (on and off states) at a certain frequency and whose period depends on the charging and discharging of a storing element which is conventionally a capacitor. This chapter discusses some relaxation oscillators which generate square waveform without using any reactive element.

4.1 Introduction

Recently, the first memristor-based oscillator without the use of any capacitors or inductors was introduced in [2–4]. The increase/decrease of memristor resistance according to the applied voltage resembles the charging/discharging of a reactive element. The inherent delay in the memristor response is exploited to realize the oscillator function. The resistance-storage property of the memristor eliminates the need for an energy-storing reactive element, i.e., capacitor or inductor. It should be noted that even ring oscillators are formed of delay stages, which depend on the charging/discharging of intrinsic and extrinsic capacitances. Figure 4.1a shows the oscillator circuit based on a voltage divider between a resistor and a memristor, and a feedback function ($F(Vi)$), which is similar to the conventional relaxation oscillator [1].

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DOI 10.1007/978-3-319-17491-4_4

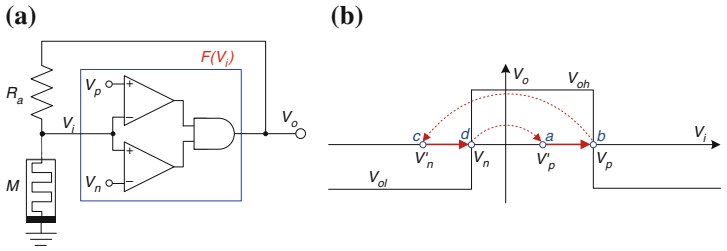

Fig. 4.1 **a** First memristor-based oscillator circuit, **b** transfer function of $F(Vi)$ showing transition between different operating points [2]

The memristor is connected in a polarity such that the memristance R_m increases for positive V_i and decreases for negative V_i. The threshold voltages V_p and V_n should be selected such that $V_n, 0, V_p$. A simple implementation of $F(V_i)$ using two comparators and an AND gate is shown in Fig. 4.1a. The oscillator is traced as shown in Fig. 4.1b, assuming that we start at point 'a'.

$a \rightarrow b$: At 'a' a positive voltage is applied to the memristor since $V_o = V_{oh}$. The memristor resistance will increase, and so will V_i until the operating point reaches 'b'.

$b \rightarrow c$: At b' the value of V_i will just pass V_p, thus V_o will switch to V_{ol}, and the operating point will jump to 'c'.

$c \rightarrow d$: At 'c' a negative voltage is applied to the memristor. The memristor resistance will decrease, and so will $|V_i|$ until the operating point reaches 'd'.

$d \rightarrow a$: At 'd' the value of V_i will just pass V_n, thus V_o will switch to V_{oh}, and the operating point will jump to 'a'.

The general expressions for the oscillation conditions and the oscillation frequency are obtained as well as the circuit realization which is suitable for low power applications and biomedical applications.

4.2 Voltage Controlled Oscillators

In general, the oscillator circuit consists of a single memristor M, resistor R_a, and control circuit $F(V_i)$ to control the resistance swing of the memristor to keep it within the required resistance range [5]. Another circuit could be obtained if the memristor M is exchanged with the resistor R_a, but the control circuit $F(V_i)$ in this case will be changed as shown in Fig. 4.2 [5].

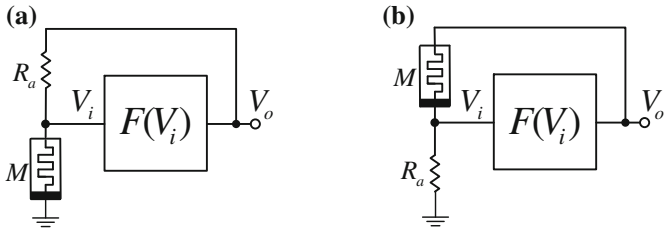

Fig. 4.2 Basic arrangements of relaxation oscillator: **a** R-M reactance-less oscillator, and **b** M-R reactance-less oscillator

4.2.1 R-M Relaxation Oscillator

The control circuit $F(V_i)$ of this arrangement basically consists of two comparators ANDed together as shown in Fig. 4.3a and its output is given as

$$F(V_i) = \begin{cases} V_{oh} & V_p' \leq V_i < V_p \\ V_{ol} & otherwise \end{cases} \tag{4.1}$$

where $V_p' = V_{ref} + V_n - V_{ol}$, and V_{oh}, V_{ol}, V_p and V_n are maximum supply voltage, minimum supply voltage, and the threshold voltages which control the maximum and minimum resistances of the memristor respectively. The resistance of the memristor using the linear model, which was proposed in [6, 7], is given as

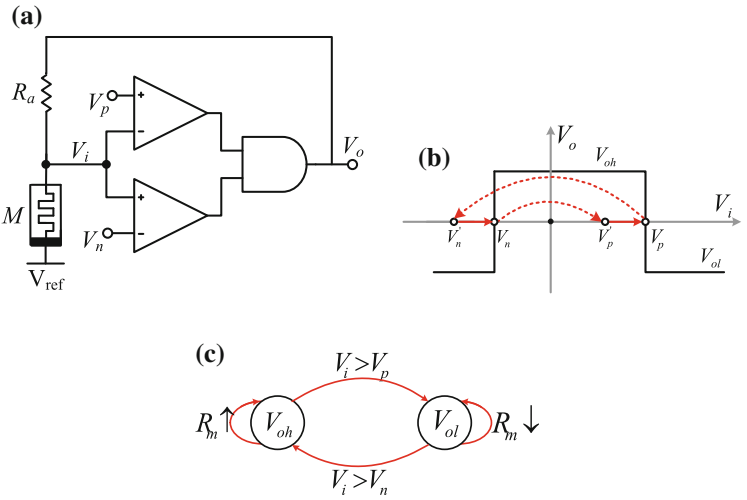

Fig. 4.3 **a** R-M reactance-less oscillator, **b** hysteresis loop of $F(V_i)$, and **c** the corresponding state diagram of the control circuit

$$R_m^2(t) = R_{in}^2 + 2k' \int_0^t V_m(t)dt. \tag{4.2}$$

By differentiating the previous equation with respect to time

$$R_m dR_m = k' V_m(t)\, dt = k' \left(\frac{V_o(t)\, R_m}{R_m + R_a} \right) dt, \tag{4.3}$$

where $k' = \mu_v R_{on}(R_{off} - R_{on})/D^2$ which depends on the mobility factor μ_v ($m^2\, s^{-1}\, V^{-1}$), minimum resistance R_{on}, maximum resistance R_{off}, and memristor length D(m).

Previously, the explanation for the hysteresis of relaxation oscillators in electronic circuits was discussed in [8]. In this circuit, the concept of oscillation of the R-M oscillator can be traced as shown in Fig. 4.3b, c. Assuming the start point to be $V_i \in [V_p',\ V_p]$, the output voltage is V_{oh} which means that the rate of the change of the memristance is positive as in (4.3) as a result of which the memristance increases, then V_i increases until it reaches V_p. When V_i increases a little more than V_p, the control circuit $F(V_i)$ will be equal to V_{ol}, which means that the rate of change of the memristance is negative. Consequently, the resistance decreases, also V_i decreases until it reaches V_n. When V_i increases a little more than V_n, the control circuit $F(V_i)$ will be equal to V_{oh} and since $V_i = V_p'$, the memristance will increase and so on as shown in the state diagram in Fig. 4.3c.

As charges pass through the memristor, the memristance value will change within the range $R_m \in (R_{on},\ R_{off})$. But if this memristance reaches one of its boundaries R_{on} or R_{off}, it will be constant as long as the direction of current does not change. Therefore for a sustained oscillation, R_m should not reach one of its boundaries. In case of reaching one of the boundaries, the input voltage V_i becomes saturated which results in constant output voltage. Thus, the use of two comparators to control the transition operation using two reference voltages V_p and V_n, where the condition for oscillation is given as

$$R_{on} < R_{mn} < R_{mp} < R_{off}, \tag{4.4}$$

where R_{mp} and R_{mn} are the memristances at which V_i reaches V_p and V_n and the output voltage is V_{oh} and V_{ol} respectively. The values of R_{mn} and R_{mp} as a function V_{ref} are given as

$$R_{mn} = \frac{R_a\left(V_n - V_{ref}\right)}{V_{ol} - V_n}, \quad R_{mp} = \frac{R_a\left(V_p - V_{ref}\right)}{V_{oh} - V_p}. \tag{4.5}$$

Therefore, the necessary and sufficient condition for oscillation for V_{ref} and R_a can be obtained. From (4.4) and (4.5) where the first condition for oscillation is given as

$$\left(\frac{V_n - V_{ol}}{V_{ref} - V_n}\right) R_{on} < R_a < \left(\frac{V_{oh} - V_p}{V_p - V_{ref}}\right) R_{off}. \tag{4.6}$$

The voltage across the memristor must be within the range of V_n and V_p to keep the memristance within the range of R_{mn} and R_{mp}, which means that R_{mn} must be less than R_{mp} as given by (4.7a) and R_a must satisfy the condition in (4.6) as given by (4.7b). The final oscillation condition for V_{ref} is given by the intersection range between (4.7a) and (4.7b), which can be summarized in (4.7c).

$$V_{ref} < \min\left(V_p, \frac{(V_{oh}V_n - V_pV_{ol})}{V_{oh} - V_{ol} - V_p + V_n}\right), \tag{4.7a}$$

$$\max\left(\frac{V_n\left(R_{on} + R_a\right) - R_{on}V_{ol}}{R_a}, \frac{V_p\left(R_{off} + R_a\right) - R_{off}V_{oh}}{R_a}\right) < V_{ref}, \tag{4.7b}$$

$$\begin{aligned}\max\left(\frac{V_n\left(R_{on} + R_a\right) - R_{on}V_{ol}}{R_a}, \frac{V_p\left(R_{off} + R_a\right) - R_{off}V_{oh}}{R_a}\right) < V_{ref} \\ < \min\left(V_p, \frac{(V_{oh}V_n - V_pV_{ol})}{V_{oh} - V_{ol} - V_p + V_n}\right).\end{aligned} \tag{4.7c}$$

Figure 4.4 identifies the region of existence of oscillatory behavior, where the working R_a range is plotted versus the reference voltage V_{ref} where this range increases as V_{ref} increases. When $V_{ref} = 0$, the working R_a range is from $100\,\Omega$ to $12.66\,\text{k}\Omega$ and when V_{ref} is maximum, the working R_a range becomes between $60\,\Omega$ and $22.79\,\text{k}\Omega$. Also at $R_a = 3\,\text{k}\Omega$, the circuit will oscillate where V_{ref} is in the range $(-0.4833, 1/3)$.

Using the same procedure proposed in [2] taking into consideration the reference voltage and by integrating (4.3) from R_{mn} to R_{mp} through time T_H where $V_o = V_{oh}$, the time of positive half cycle T_H is given as

$$T_H = \frac{\left(R_{mp} - R_{mn}\right)\left(R_{mp} + R_{mn} + 2R_a\right)}{2k'\left(V_{oh} - V_{ref}\right)}. \tag{4.8}$$

The time of negative half cycle T_L and the duty cycle D are

$$T_L = T_H\frac{\left(V_{oh} - V_{ref}\right)}{\left(V_{ref} - V_{ol}\right)}, \qquad D = \frac{V_{ref} - V_{ol}}{V_{oh} - V_{ol}}. \tag{4.9}$$

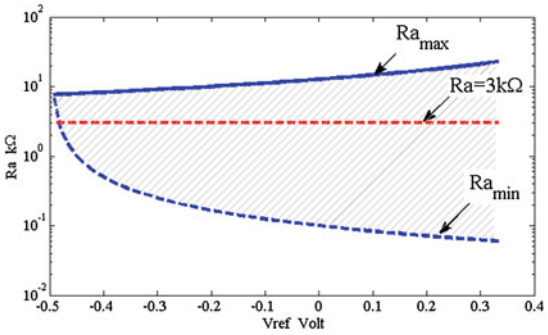

Fig. 4.4 R_a versus V_{ref} for $\{R_{off}, R_{on}, V_{oh}, V_{ol}, V_p, V_n\} = \{38\,\text{k}\Omega, 100\,\Omega, 1\text{V}, -1\,\text{V}, 0.75\,\text{V}, -0.5\,\text{V}\}$

The frequency of oscillation is given as

$$f_o = \frac{1}{T_H}\frac{\left(V_{ref} - V_{ol}\right)}{\left(V_{oh} - V_{ol}\right)}, \tag{4.10a}$$

$$f_o = \frac{2k'D\left(V_{oh} - V_{ref}\right)\left(V_{oh} - V_p\right)^2\left(V_n - V_{ol}\right)^2}{R_a^2\left(V_{ref}\left(V_{ol} + V_p - V_{oh} - V_n\right) + V_{oh}V_n - V_{ol}V_p\right)\left(V_{ref}\left(V_{ol} + V_{oh} - V_p - V_n\right) + V_{oh}V_n + V_{ol}V_p - 2V_{oh}V_{ol}\right)}. \tag{4.10b}$$

As is clear from (4.10) the frequency of oscillation can be controlled by different means such as by changing R_a since f_o is inversely proportional to R_a^2 or by changing V_{ref}. When V_{ref} increases within the range specified by (4.7), the values of R_{mn} and R_{mp} decrease and hence the frequency of oscillation will increase as shown in Fig. 4.5a. When $V_{ref} = 0$, the previous equations will be reduced to their special cases, introduced in [2]. As an example, let the memristor parameters be $\left\{R_{on},\ R_{off},\ d,\ \mu_v\right\} = \left\{100\,\Omega, 38\,\text{k}\Omega, 10\,\text{nm}, 10^{-10}\,\text{cm}^2\,\text{s}^{-1}\,\text{V}^{-1}\right\}$ and the other circuit parameters be $\{V_{ol},\ V_{oh},\ V_n,\ V_p\} = \{-1\,\text{V}, 1\,\text{V},\ -0.5\,\text{V},\ 0.75\,\text{V}\}$. Using the previous data, the range of oscillation frequency changes as V_{ref} changes. For the lower bound of the memristor resistance $R_{mn} = R_{on}$ then $R_{a_{min}} = \frac{R_{on}}{2V_{ref}+1}$ and $R_{mp} = R_{on}\left(\frac{3-4V_{ref}}{2V_{ref}+1}\right)$. The frequency of oscillation in this case from (4.10) is equal to

$$f_o = \frac{37900\left(1 - V_{ref}^2\right)\left(2V_{ref} + 1\right)^2}{(2 - 6V_{ref})(6 - 2V_{ref})}. \tag{4.11}$$

For the upper memristance bound where $R_{mp} = R_{off}$, the $R_{a_{max}} = \frac{R_{off}}{3-4V_{ref}}$, therefore $R_{mn} = R_{off}\left(\frac{2V_{ref}+1}{3-4V_{ref}}\right)$, and the frequency of oscillation are obtained as

$$f_o = \frac{37900\left(1 - V_{ref}^2\right)\left(3 - 4V_{ref}\right)^2}{(380)^2(2 - 6V_{ref})(6 - 2V_{ref})}. \tag{4.12}$$

The maximum range of V_{ref} for oscillation from (4.7) and (4.10) is $-0.4935 < V_{ref} < (1/3)$ where the minimum value of V_{ref} comes from the intersection of the $R_{a_{min}}$ and the $R_{a_{max}}$ curves. From (4.6) and Fig. 4.5a, the valid range of R_a increases with increasing V_{ref}, which enhances the flexibility of the relaxation oscillator. Moreover, the oscillation frequency range is [0.1969 Hz–3.158 kHz] and [25.78 Hz–3 MHz) when $V_{ref} = 0$ and $V_{ref} = V_{ref_{max}} = 1/3$ V respectively. Another advantage of using V_{ref} is that the circuit can operate under all positive or negative voltages as long as $V_{oh} > V_p > V_{ref} > V_n > V_{ol}$ as shown in Fig. 4.5b.

Using the PSPICE model proposed in [9], the output oscillations for three different values of $V_{ref} = \{-0.3,\ 0,\ 0.3\}$ for $\{R_a, R_{off},\ R_{on},\ V_{oh}, V_{ol}, V_p, V_n\} = \{3\,\text{k}, 38\,\text{k}, 100, 1,\ -1,\ 0.75,\ -0.5\}$ are shown in Fig. 4.6a. It is clear from the figure that the big change in the oscillation frequency is by changing V_{ref}. Figure 4.6b shows the output response when all voltage parameters are positive such that R_a, R_{off}, R_{on}, V_{oh}, V_{ol}, V_p, V_n and V_{ref} equal 3 kΩ, 38 kΩ, 100 Ω, 3 V, 1 V, 2.6 V, 1.5 V and 2 V respectively. The frequency of oscillation from (4.10) equals 18.716 Hz which matches the frequency obtained from the PSPICE simulation.

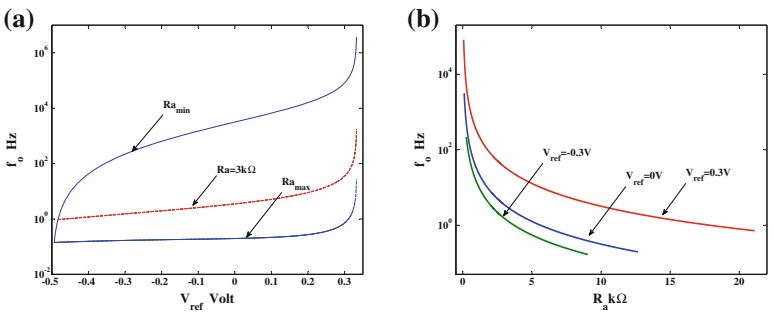

Fig. 4.5 **a** Oscillation frequency versus V_{ref}, and **b** oscillation frequency versus R_a for different V_{ref}

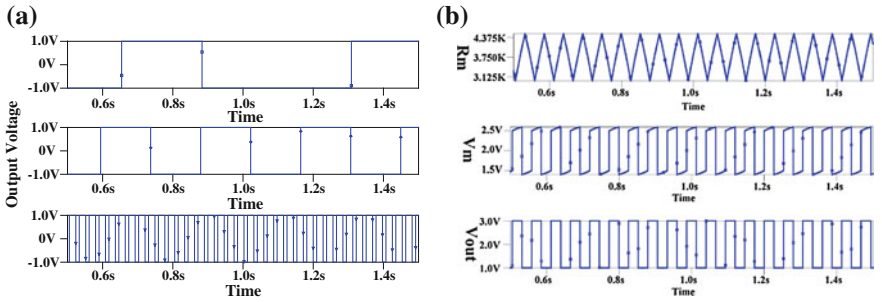

Fig. 4.6 **a** PSPICE transient simulation of the output voltage V_{out} for different V_{ref}, $V_{ref} = -0.3$ V (*upper*), $V_{ref} = 0$ V (*middle*) and $V_{ref} = 0.3$ V (*lower*), and **b** PSPICE transient simulation results of linear dopant model for R_m (*upper*), V_i (*middle*) and V_o (*lower*)

4.2.2 M-R Based Oscillator

In this section, another arrangement where the memristor is replaced with a resistor is discussed. The control circuit of the R-M oscillator is different since $V_i \in [V_n,\ V_p]$, the output voltage is V_{oh} and so the memristance increases. Then, the voltage V_i decreases until the memristance reaches its minimum resistance R_{on} and the memristor becomes saturated so that no oscillation occurs if an AND gate is used in the control circuit. Therefore, to get an oscillation the AND should be replaced by a NAND as shown in Fig. 4.7a. Then, the control function $F(V_i)$ is given as

$$F\,(V_i) = \begin{cases} V_{oh} & V_p < V_i < V_p' \\ V_{ol} & otherwise \end{cases} \tag{4.13}$$

Using the hysteresis loop of the oscillator, shown in Fig. 4.7b, the concept of oscillation is discussed as follows: assume $V_i \in [V_p,\ V_p']$ which means that $V_o = V_{oh}$ so that the memristance increases and V_i decreases until V_i reaches less than V_p; then the output voltage V_o will be changed to V_{ol} and also V_i will be changed to V_n' and so the memristance decreases and V_i increases until it reaches more than V_n; then V_o will be changed to V_{oh} and V_i will be changed to V_p' and also the memristance increases and so on as shown in the state diagram in Fig. 4.7b.

In this case, the value of R_{mn} and R_{mp} is given as

$$R_{mn} = R_a \frac{V_n - V_{ol}}{V_{ref} - V_n}, \quad R_{mp} = R_a \frac{V_{oh} - V_p}{V_p - V_{ref}}. \tag{4.14}$$

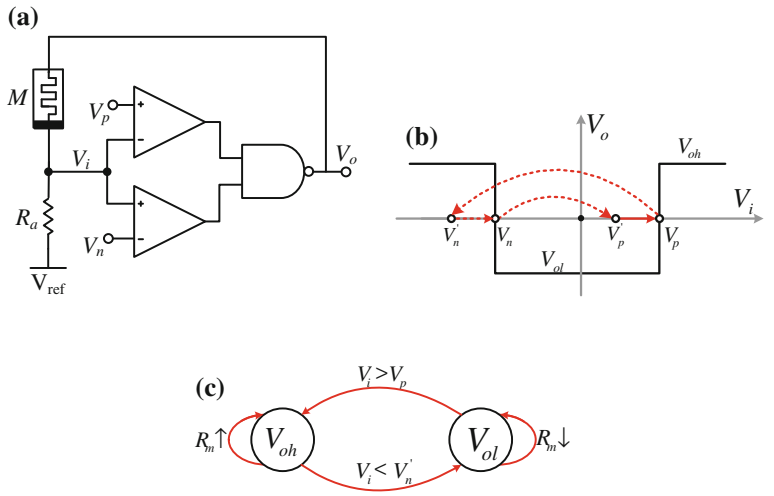

Fig. 4.7 **a** M-R reactance-less oscillator, **b** hysteresis loop of $F(V_i)$, and **c** the corresponding state diagram of the control circuit

Therefore, the necessary and sufficient condition for oscillation on V_{ref} and R_a can be obtained as

$$R_{on}\frac{V_{ref}-V_n}{V_n-V_{ol}} < R_a < R_{off}\frac{V_p-V_{ref}}{V_{oh}-V_p}. \tag{4.15}$$

The value of the reference voltage V_{ref} should ensure that the memristance does not leave the range $[R_{mn}, R_{mp}]$. Therefore, the condition on V_{ref} for oscillation is given as

$$\begin{aligned} max\left(Vn, \frac{(V_{oh}V_n - V_pV_{ol})}{(V_{oh}-V_{ol}-V_p+V_n)}\right) &< V_{ref} \\ < min\left(\frac{V_p\left(R_a+R_{off}\right)-R_aV_{oh}}{R_{off}}, \frac{V_n\left(R_a+R_{on}\right)-R_aV_{ol}}{R_{on}}\right). \end{aligned} \tag{4.16}$$

For $R_a = 3\,\text{k}\Omega$, the circuit will oscillate when V_{ref} is in the range $(-0.7484, 0.466)$. Figure 4.8 determines the working range of R_a versus the reference voltage V_{ref} of the M-R oscillator, where the working R_a range decreases as V_{ref} increases. When $V_{ref} = 0$, and -0.7484 (the minimum value), the working R_a changes from $[300\,\Omega$–$38\,\text{k}\Omega]$ to $[0.65\,\Omega$–$94.88\,\text{k}\Omega]$ respectively.

Using the same previous procedure, the voltage across the memristor V_m is given as

$$V_m(t) = \frac{\left(V_o(t) - V_{ref}\right)R_m}{R_m + R_a} \tag{4.17}$$

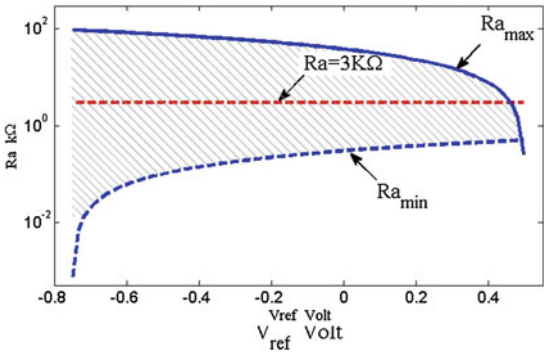

Fig. 4.8 Working R_a range versus V_{ref} for $\{R_{off}, R_{on}, V_{oh}, V_{ol}, V_p, V_n\} = \{38\,\text{k}\Omega, 100\,\Omega, 1\,\text{V}, -1\,\text{V}, 0.5\,\text{V}, -0.75\,\text{V}\}$

Using the value of $V_m(t)$ in (4.3), then

$$R_m dR_m = k'\left(\frac{\left(V_o(t) - V_{ref}\right) R_m}{R_m + R_a}\right) dt. \tag{4.18}$$

By integrating (4.18) from R_{mp} to R_{mn} through T_H, the time of positive half cycle is given by (4.8). The time of negative half cycle and the duty cycle are given by (4.9) but here in this case the M-R oscillator, R_{mn} and R_{mp} are different from the R-M oscillator so that the frequency of oscillation is given as

$$f_o = \frac{2k'D\left(V_{oh} - V_{ref}\right)\left(V_p - V_{ref}\right)^2\left(V_{ref} - V_n\right)^2}{{R_a}^2\left(V_{ref}\left(V_{oh} + V_n - V_p - V_{ol}\right) - V_{oh}V_n + V_{ol}V_p\right)\left(V_{ref}\left(V_{oh} + V_n + V_p + V_{ol} - 2V_{ref}\right) - V_{oh}V_n - V_{ol}V_p\right)}. \tag{4.19}$$

The frequency range changes as V_{ref} changes as shown in Fig. 4.9a for $\{R_{off}, R_{on}, V_{oh}, V_{ol}, V_p, V_n\} = \{38\,\text{k}\Omega, 100\,\Omega, 1\,\text{V}, -1\,\text{V}, 0.5\,\text{V}, -0.75\,\text{V}\}$, respectively. Figure 4.9b shows the obtained oscillation frequency versus the change in R_a for three different values of $V_{ref} = \{-0.3, 0, 0.3\}\,\text{V}$.

It is clear from the figure that there is a big change in the oscillation frequency by changing V_{ref}, which is also shown in Fig. 4.10a for $\{R_a, R_{off}, R_{on}, V_{oh}, V_{ol}, V_p, V_n\} = \{3\,\text{k}, 38\,\text{k}, 100, 1, -1, 0.5, -0.75\}$ respectively. Figure 4.10b shows the output response when all voltage parameters are positive such that R_a, R_{off}, R_{on}, V_{oh}, V_{ol}, V_p, V_n and V_{ref} equal $3\,\text{k}\Omega$, $38\,\text{k}\Omega$, $100\,\Omega$, $3\,\text{V}$, $1\,\text{V}$, $2.5\,\text{V}$, $1.4\,\text{V}$ and $2\,\text{V}$ respectively. The frequency of oscillation from (4.19) equals 34.45 Hz, which matches the frequency obtained from the PSPICE simulation in Fig. 4.10b.

The special case of the M-R oscillator is at grounded V_{ref}, which simplifies the previous equations. The oscillation conditions are given as

$$R_{on}\frac{|V_n|}{|V_{ol}| - |V_n|} < R_a < R_{off}\frac{V_p}{V_{oh} - V_p}, \quad \frac{R_a}{R_a + R_{off}} < \frac{V_p}{V_{oh}} < \frac{V_n}{V_{ol}} < \frac{R_a}{R_a + R_{on}}. \tag{4.20}$$

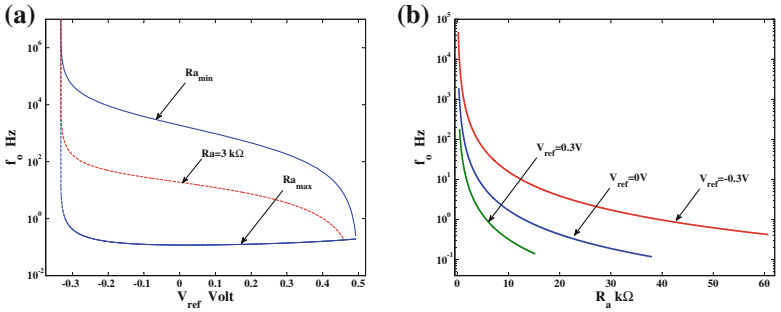

Fig. 4.9 **a** Oscillation frequency versus V_{ref}, and **b** oscillation frequency versus R_a for different V_{ref}

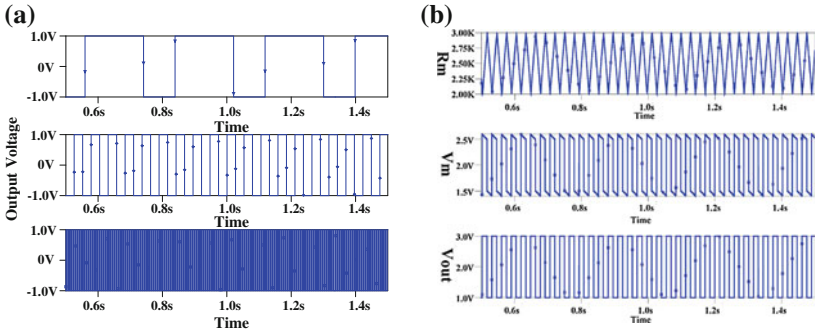

Fig. 4.10 **a** PSPICE transient simulation of the output voltage V_{out} for different V_{ref}, where $V_{ref} = 0.3$ V (*upper*), $V_{ref} = 0$ V (*middle*) and $V_{ref} = -0.3$ V (*lower*), and **b** PSPICE transient simulation results for R_m (*upper*), V_i (*middle*) and V_o (*lower*)

The frequency of oscillation f_o and the frequency range are given as

$$f_o = \frac{2k' \left|V_{ol}\right| V_{oh} {V_p}^2 {V_n}^2}{{R_a}^2 \left({V_{oh}}^2 {V_n}^2 - {V_{ol}}^2 {V_p}^2\right)\left(V_{oh} - V_{ol}\right)} = \frac{X}{{R_a}^2}, \tag{4.21}$$

where X is a variable and function of k', V_{oh}, V_{ol}, V_p and V_n, the maximum and minimum frequencies which could be obtained are given by the following closed form:

$$\frac{X\left(\frac{V_{oh}}{V_p} - 1\right)^2}{{R_{off}}^2} < f_o < \frac{X\left(\frac{V_{ol}}{V_n} - 1\right)^2}{{R_{on}}^2}. \tag{4.22}$$

From (4.10) and (4.19), the oscillation frequency is linearly proportional to the dopant drift mobility μ_v which is a physical property of the memristor material. Therefore, for higher oscillation frequencies, highly dopant material should be used.

4.2.3 Memristor-Based VCO

In the above discussion of the circuits, the duty cycle D is linearly proportional to the reference voltage V_{ref}, which means that the reference voltage controls the frequency and the duty cycle. As a result these circuits can be used as modulator circuits; the modulated signal will be proportional to the signal applied to the modulator. Using the above circuits, this modulator can be used as a digital/analog modulator if the input signal is a digital/analog signal as shown in Fig. 4.11.

For sustained oscillation, the necessary and sufficient conditions for oscillation must be satisfied and the amplitude of the input signal must be a subset from the range of V_{ref}, which is $(-0.4935, 1/3)\ V$ in the R-M circuit. From (4.12) and (4.19), it is clear that the frequency depends on V_{ref} as shown in Figs. 4.5a and 4.9a and thus this circuit can be used as a VCO. In case of the R-M oscillator, Fig. 4.5a shows that the oscillation frequency increases with increasing V_{ref} but in case of the M-R oscillator, Fig. 4.9b shows that the oscillation frequency decreases with increasing V_{ref}. For example in the R-M circuit, Fig. 4.11a shows the VCO output response which has different frequencies where a multi-level input is applied with amplitudes $\{-0.3\,\text{V},\ 0\,\text{V},\ 0.3\,\text{V}\}$. A small delay exists in the output response due to the small dopant mobility and the sudden change in V_{ref} where the memristor needs time to change its state between the maximum and minimum resistances R_{mp} and R_{mn}. Figure 4.11b shows the output voltage for applying a sinusoidal input with 0.3 v amplitude and 1 Hz frequency.

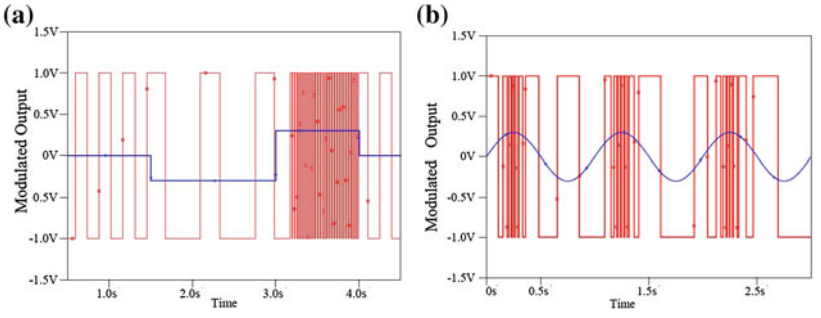

Fig. 4.11 PSPICE transient simulation of R-M oscillator using the same parameters for **a** multilevel input and **b** sinusoidal input

The nonlinear oscillation frequency of the R-M oscillator can be linearized for a certain range of V_{ref} by neglecting higher order terms

$$f_{app} \approx \gamma \left((ac\,(V_{oh} + V_{ol}) + (ad + cb)\,V_{oh}V_{ol})\,V_{ref} - acV_{oh}V_{ol} \right), \tag{4.23a}$$

$$\gamma = \frac{2k'\left(V_{oh} - V_p\right)^2 (V_n - V_{ol})^2}{R_a^2\,(V_{oh} - V_{ol})\,(ac)^2}, \quad a = V_{oh}V_n - V_{ol}V_p, \quad b = V_{ol} + V_p - V_{oh} - V_n, \tag{4.23b}$$

$$c = V_{oh}V_n + V_{ol}V_p - 2V_{oh}V_{ol}, \quad d = V_{ol} + V_{oh} - V_p - V_n. \tag{4.23c}$$

For the same data in the R-M oscillator, the percentage error between the exact and the approximated formulas is less than 2 % when $V_{ref} \in [-0.05,\ 0.05]$.

One of the advantages of this VCO is the use of the memristor to emulate the effect of the charging and discharging of the reactive elements which are commonly used in the conventional VCO. Moreover, the size of this circuit is very small due to the nanosize of the memristor compared to the size of the conventional VCOs which contain capacitors or inductors. However, the oscillation frequency of this VCO is nonlinear with the reference voltage V_{ref} but could be approximated to be linear as discussed before at small ranges of V_{ref}.

4.2.4 Discussion and Comparison

The modified circuits can operate with all voltage supplies either positive or negative but the necessary and sufficient conditions for oscillation should be satisfied. Furthermore, by changing V_{ref} the oscillation frequency can be controlled for both cases. The oscillation frequency in both oscillators is linearly proportional to the dopant mobility which depends on the used material. Table 4.1 shows a numerical comparison between the two reactance-less oscillators for three different values of $V_{ref} = \{-0.3,\ 0,\ 0.3\}$ when $\{R_{off},\ R_{on},\ V_{oh}, V_{ol}\} = \{38\,\mathrm{k\Omega}, 100\,\Omega, 1\,\mathrm{V}, -1\,\mathrm{V}\}$, and $\{V_p, V_n\}$ equal to $\{0.75\,\mathrm{V},\ -0.5\,\mathrm{V}\}$ and $\{0.5\,\mathrm{V},\ -0.75\,\mathrm{V}\}$ for the R-M and the M-R oscillators respectively. It is clear from this table that by changing the value of V_{ref} between -0.3 and 3.0 V and using the same circuit parameters, the maximum oscillation frequency is scaled to be in the range of [7 %, 2588 %] and [2543 %, 10 %] of $f_{omax}(V_{ref} = 0)$ for the R-M and the M-R relaxation oscillator respectively. In addition, the ratio (f_{omax}/f_{omin}) equals 1309, 16,040, 1,14,099 Hz for the R-M oscillator and 1,14,096, 16,059, 1421 Hz for the M-R oscillator when V_{ref} equals -0.3, 0, 0.3 V, respectively, which illustrates how the reference voltage affects the controllability of these oscillators.

Table 4.1 The oscillation parameters of the R-M and M-R oscillators for three different cases of V_{ref}

	R-M Oscillator			M-R Oscillator		
V_{ref} (V)	−0.3	0	0.3	−0.3	0	0.3
R_{amin} (Ω)	250	100	62.5	180	300	420
R_{amax} (kΩ)	9.0476	12.667	21.11	60.8	38	15.2
f_{omin} (Hz)	0.168	0.1969	0.7165	0.4224	0.118	0.139
f_{omax} (Hz)	220.025	3158.33	81751.7	48194	1895	197.53
$f_{o_{R_a=3k\Omega}}$ (Hz)	1.5279	3.50926	35.4825	173.776	18.95	3.5759

4.3 Effect of Boundary on R-M Oscillator

In this section, we will discuss the effect of changing Joglekar's window function $f(x) = 1 - (2x-1)^{2p}$ for linear ion drift model [10]. The effect of changing the dopant value p is discussed for nonlinear $p = 1$ and linear $p = \infty$ as shown in Fig. 4.12 on R-M oscillator, which can similarly done for M-R oscillator [11].

4.3.1 Mathematical Analysis

The values of R_{mp} and R_{mn} are given by the same relations in (4.5), also the necessary and sufficient condition for oscillation on V_{ref} and R_a can be obtained as in (4.6) and (4.7). As known, the rate of change of the parameter x for the HP memristor [12] which represents the ratio between the doped length to the total length of the memristor is

$$\frac{dx}{dt} = -ki(t)\, f(x) = -k\frac{V_o - V_{ref}}{R_m + R_a} f(x), \tag{4.24}$$

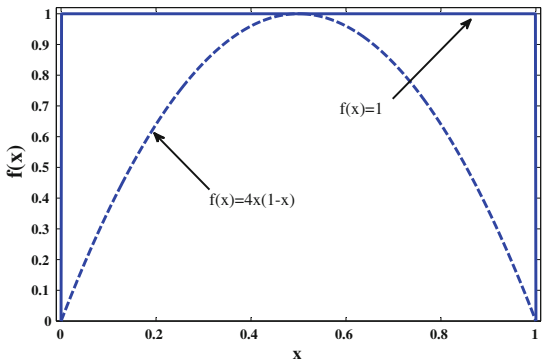

Fig. 4.12 Window function for linear and nonlinear drift model

$$\frac{dR_m}{dt} = k' \frac{(V_o - V_{ref}) f(x)}{R_m + R_a}, \tag{4.25}$$

where the function $f(x)$ represents the nonlinear dopant drift of the memristor behavior. In case of $f(x) = 1$, the system has a linear draft dopant which leads to the previous case. However at $p = 1$, the window function $f(x) = 4x(1 - x)$ so the rate of change is

$$\frac{dx}{dt} = -k(V_o - V_{ref}) \frac{4x(1 - x)}{R_{off} + R_a - (R_{off} - R_{on})x}. \tag{4.26}$$

Therefore,

$$\int_{x_{mn}}^{x_{mp}} \left(\frac{R_{off} + R_a}{x} + \frac{R_{on} + R_a}{1 - x} \right) dx = \int_0^{T_H} 4k \left(V_{ref} - V_o \right) dt, \tag{4.27}$$

where x_{mn} and x_{mp} correspond to the state variable values of the memristance R_{mn} and R_{mp} respectively. After integration and performing some simplifications, the time of positive half cycle T_H is given as

$$T_H = \frac{\left(R_{off} + R_a\right) \ln\left(\frac{R_{off} - R_{mn}}{R_{off} - R_{mp}}\right) + \left(R_{on} + R_a\right) \ln\left(\frac{R_{mp} - R_{on}}{R_{mn} - R_{on}}\right)}{4k(V_{oh} - V_{ref})}. \tag{4.28}$$

The time of negative half cycle is calculated by the same formula in (4.9) and the frequency of oscillation is given as

$$f_o = \frac{1}{T_H} \frac{(V_{ref} - V_{ol})}{(V_{oh} - V_{ref})}, \tag{4.29}$$

and the duty cycle is given by (4.9). Figure 4.13 shows that the range of memristance R_m changes from 3 to 4.5 kΩ and the oscillation frequency equals 6.476 Hz, which matches the frequency and R_m range in (4.6) and (4.29) respectively.

In case of grounded V_{ref}, the time of positive half cycle is

$$T_H = \frac{\left(R_{off} + R_a\right) \ln\left(\frac{R_{off} - R_{mn}}{R_{off} - R_{mp}}\right) + \left(R_{on} + R_a\right) \ln\left(\frac{R_{mp} - R_{on}}{R_{mn} - R_{on}}\right)}{4kV_{oh}}, \tag{4.30}$$

and the time of negative half cycle is given as

$$T_L = T_H \frac{V_{oh}}{|V_{ol}|}. \tag{4.31}$$

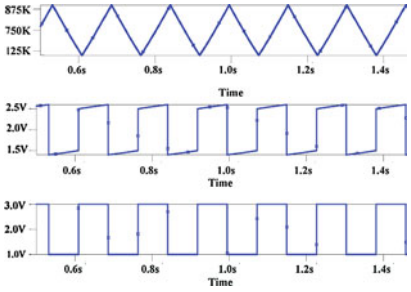

Fig. 4.13 Transient simulation results of nonlinear dopant model for R_m (*upper*), V_i (*middle*) and V_o (*lower*) for R_a, R_{off}, R_{on}, V_{oh}, V_{ol}, V_p, V_n, and V_{ref} equal 3 kΩ, 38 kΩ, 100 Ω, 3 V, 1 V, 2.6 V, 1.5 V, and 2 V respectively

Therefore, the duty-cycle and the periodic time are $D = \frac{|V_{ol}|}{V_{oh}-V_{ol}}$, and $T = T_H\left(1-\frac{V_{oh}}{V_{ol}}\right)$ (same as linear case), respectively, and the necessary and sufficient conditions for oscillation are still the same as in (4.6); however, (4.7c) is simplified to (4.32) which matches the linear model at $V_{ref} = 0$ [2].

$$V_p > V_n \frac{V_{oh}}{V_{ol}}. \tag{4.32}$$

When the memristance R_m reaches one of the boundaries R_{on} or R_{off}, the oscillation frequency becomes zero as expected. For example, let R_a, R_{off}, R_{on}, V_{oh}, V_{ol}, V_p, and V_n equal 3 kΩ, 38 kΩ, 100 Ω, 1 V, −1 V, 0.75 V and −0.5 V respectively. The oscillation frequency will be equal to 1.788 Hz and the memristance R_m changes from 3 to 9 kΩ.

Figure 4.14 shows that the curves of the oscillation frequency for different R_a are not enclosed between R_{amax} and R_{amin} curves as in the case of the linear dopant model shown in Fig. 4.5a, due to the nonlinearity of the model which appears in the oscillation frequency equations (4.30) and (4.31).

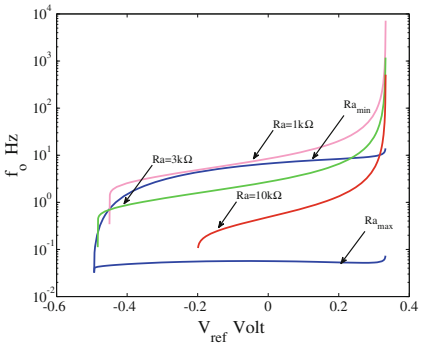

Fig. 4.14 The oscillation frequency versus V_{ref} for different cases of R_a

4.3.2 Discussion and Comparison

Due to the behavior of the nonlinear model of the memristor, when the memristor clings to one of its boundaries R_{on} or R_{off}, the oscillation frequency will be zero as shown in Fig. 4.15a. But in the case of the linear model, the memristor would not cling to its boundary due to the discontinuity of the model as shown in Fig. 4.15b. It is clear that the maximum frequency f_{omax} equals 290.1, 31.34, and 8.242 Hz when $(R_a,\ V_{ref})$ is equal to $(129.5\,\Omega,\ 0.3\,\text{V})$, $(148\,\Omega,\ 0\,\text{V})$, and $(305\,\Omega,\ -0.3\,\text{V})$, respectively, for the nonlinear dopant drift model. However, there is no maximum in the linear model due to the windowing discontinuity effect of the model.

Actually the dopant value is unknown due to the variations in the fabrication process but its value is enclosed between nonlinear dopant $p = 1$ and linear dopant $p = \infty$. For designing a good memristor-based oscillator, the frequency variation range should be very narrow as shown in Fig. 4.15 where it is better to design the oscillator between the first and the second intersections of linear and nonlinear dopant curves from $R_a = 4.037$ to $R_a = 12.348\,\text{k}\Omega$ in the case $V_{ref} = 0\,\text{V}$ curve where the maximum change in the frequency is $\triangle f = 0.2963\,\text{Hz}$.

From Eqs. (4.10) and (4.30), the oscillation frequency is linearly proportional to the dopant drift mobility μ_v, which is a physical property of the memristor material so in case of need for higher frequencies, highly dopant material should be used. A summary table of all the needed equations for designing a memristor-based reactanceless oscillator is introduced in Table 4.2.

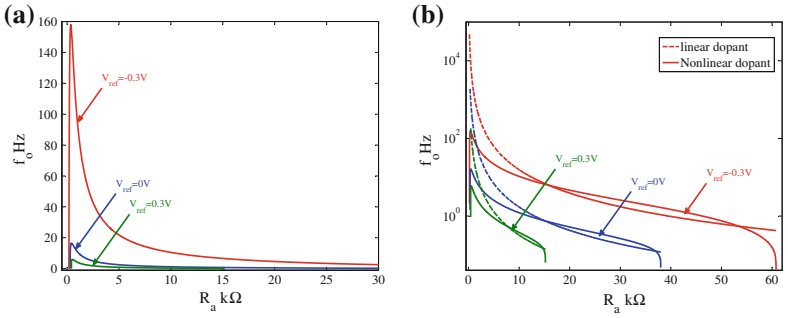

Fig. 4.15 Oscillation frequency versus R_a for different models and different $V_{ref} = 0.3\,\text{V}$ (*upper*), $V_{ref} = 0\,\text{V}$ (*middle*) and $V_{ref} = -0.3\,\text{V}$ (*lower*)

Table 4.2 Controlled reactance-less oscillator summary

	Linear window	Nonlinear window
T_H	$\frac{(R_{mp}-R_{mn})(R_{mp}+R_{mn}+2R_a)}{2k'(V_{oh}-V_{ref})}$	$\frac{(R_{off}+R_a)ln\left(\frac{R_{off}-R_{mn}}{R_{off}-R_{mp}}\right)+(R_{on}+R_a)ln\left(\frac{R_{mp}-R_{on}}{R_{mn}-R_{on}}\right)}{4k(V_{oh}-V_{ref})}$
Duty cycle	$\frac{V_{ref}-V_{ol}}{V_{oh}-V_{ol}}$	
R_a range	$R_{on}\frac{V_n-V_{ol}}{V_{ref}-V_n} < R_a < R_{off}\frac{V_{oh}-V_p}{V_p-V_{ref}}$	
R_m range	$R_a\frac{V_n-V_{ref}}{V_{ol}-V_n} < R_m < R_a\frac{V_p-V_{ref}}{V_{oh}-V_p}$	
Condition of oscillation	$\max\left(\frac{V_n(R_{on}+R_a)-R_{on}V_{ol}}{R_a}, \frac{V_p(R_{off}+R_a)-R_{off}V_{oh}}{R_a}\right) < V_{ref} < \min\left(V_p, \frac{(V_{oh}V_n-V_pV_{ol})}{(V_{oh}-V_{ol}-V_p+V_n)}\right)$	

4.4 Two-Series Memristors Analysis

Generally, there are four different connections for two memristors in series as shown in Fig. 4.16, where the output is the common node between the two memristors [13]. The instantaneous memristance of each memristor and the rate of change in its state are given as

$$R_m(t) = R_{in} - R_d x(t), \tag{4.33a}$$

$$\frac{dx}{dt} = \eta k i_{in}(t), \tag{4.33b}$$

where R_{off}, R_{on}, R_d and x represent the maximum and minimum achievable resistances of the memristor, their difference, the state variable of the memristor, respectively, and η represents the polarity of the memristor, where the wide black line of the memristor's symbol refers to the positive terminal and vice versa.

Substituting by (4.33b) into the derivative of (4.33a), the rate of change in the memristance is

$$\frac{dR_m}{dt} = \mp k R_d i_{in}(t), \tag{4.34}$$

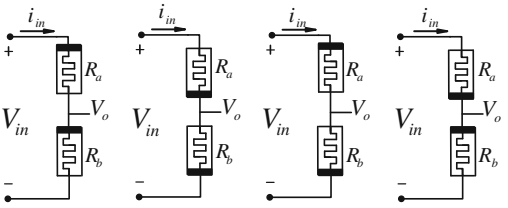

Fig. 4.16 Different configurations of two series memristors

The rates of change in the resistance of the two memristors are given as

$$\frac{dR_a}{dt} = k'_a i_{in}(t), \quad \frac{dR_b}{dt} = k'_b i_{in}(t), \tag{4.35}$$

where $k'_a = -\eta k_a R_d$, and $k'_b = -\eta k_b R_d$ ($\Omega^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$).

The current through the memristors is the same so the rate of change in the first memristance R_a is a fraction of the rate of change in the other memristance R_b

$$\frac{dR_a}{dt} = \alpha \frac{dR_b}{dt}, \tag{4.36}$$

where the mismatch factor $\alpha = k'_a/k'_b$. By integrating both sides of (4.36) with respect to time, the relation between the two memristances R_a and R_b is given as

$$R_a(t) = \alpha R_b(t) + R_{in_d}, \tag{4.37}$$

where $R_{in_d} = R_{in_a} - \alpha R_{in_b}$, R_{in_a} and R_{in_b} are the initial memristances of the first memristor R_a, and second memristor R_b respectively. The output voltage V_o is a voltage divider across the two series memristances; assuming grounded reference voltage, and after substituting by the relation between the two memristances (4.37), the output voltage can be obtained as

$$V_o = V_{in} \frac{R_b(t)}{(\alpha + 1) R_b(t) + R_{in_d}}. \tag{4.38}$$

The output voltage V_o is a function of the initial memristances R_{in_a}, R_{in_b} and the instantaneous value of R_b so the instantaneous value of R_b should be calculated first. From (4.34) and (4.35), the rate of change of the memristance of R_b is given by (4.39a). Substituting by the value of R_a from (4.37) and integrating from R_{in_b} to R_b, the expression of the memristance R_b is given as (4.39b)

$$\frac{dR_b}{dt} = -k'_b \frac{V_{in}}{R_b(t) + R_a(t)}, \tag{4.39a}$$

$$\left(R_b(t) - R_{in_b}\right)\left[(\alpha + 1)\left(R_b(t) + R_{in_b}\right) + 2R_{in_d}\right] = -2k'_b \varphi(t), \tag{4.39b}$$

where $\varphi(t)$ represents the flux, assuming zero initial flux. Using the PSPICE memristor model proposed in [9], with Joglekar's window function and high doping factor $p = 100$, Fig. 4.17 shows the memristances R_a and R_b for $\alpha = 2$ when applying a square wave input of ± 1 v and 2 Hz frequency where the maximum memristances reached at transition from positive to negative voltages equals $R_b = 13.663\,\mathrm{k}\Omega$ and $R_a = 17.365\,\mathrm{k}\Omega$, matching the calculation results with a relative error around 0.32 % due to the nonlinearity of the window function of the model.

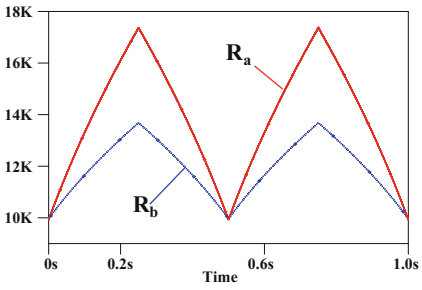

Fig. 4.17 PSPICE simulation of the memristances R_a and R_b for $\alpha = 2$, $R_{ina} = R_{in_b} = 10\,\text{k}\Omega$, $k'_a = 2\,k'_b = 758\,\text{M}\Omega^2\,\text{V}^{-1}\,\text{s}^{-1}$

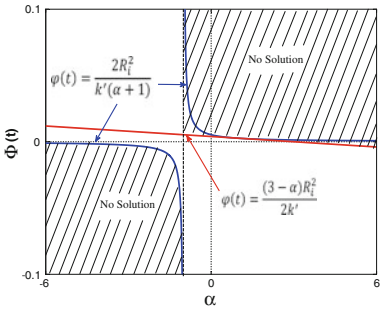

Fig. 4.18 The solution existence region for $R_{ina} = R_{in_b} = 1\,\text{k}\Omega$ and $k'_b = 379\,\text{M}\Omega^2\,\text{V}^{-1}\,\text{s}^{-1}$

The memristance R_b must be real and positive so by solving the second order equation (4.39b) using quadratic formula, there is a solution at a certain range as shown in Fig. 4.18 for equal initial memristance. The hashed region shows that no solution could be obtained for the corresponding α and φ.

The memristance R_b is a function of α, R_{in_a}, R_{in_b}, and k'_b. Figure 4.19 shows the change in the memristance R_b due to the change in $\varphi(t)$ and α. It is clear from Fig. 4.19a that the memristance R_b increases with increase in the negative α; also, the solution is valid for positive φ only which matches the existence region in Fig. 4.18. Furthermore, for $\alpha > -1$ in Fig. 4.19b, the memristance decreases with increasing

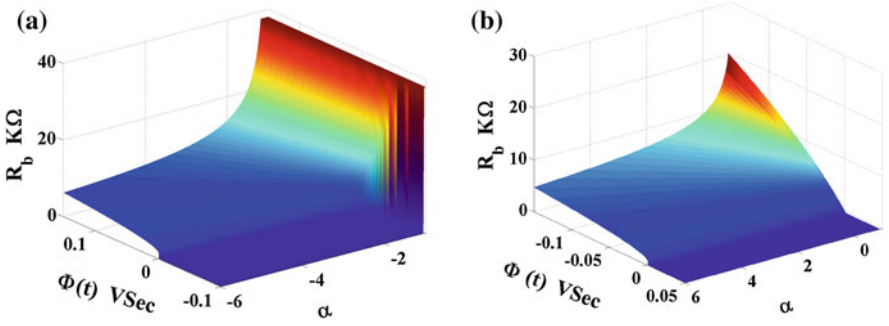

Fig. 4.19 The memristance behavior for $R_{ina} = R_{in_b} = 1\,\text{k}\Omega$

α and negative φ and there is no solution for positive φ, which matches the existence region in Fig. 4.18.

Four special cases based on α can be studied as follows:

1. $k'_a = 0$, which means that R_a is a resistor in series with the memristor R_b so $\alpha = 0$, then (4.39b) becomes

$$\left(R_b(t) - R_{in_b}\right)\left[R_b(t) + R_{in_b} + 2R_a\right] = -2k'_b\varphi(t)\,. \tag{4.40}$$

   Here, two subcases are available, where k'_b may be positive or negative depending on the polarity of the memristor which will control the change of the memristance either by decreasing or increasing the memristance respectively. Figure 4.20a shows PSPICE simulation of the instantaneous memristance R_b and the output voltage V_o for square wave input with amplitude $= \pm 1$ v, frequency $= 2$ Hz and positive k'_b where maximum $R_b = 12.848\,\text{k}\Omega$ which matches the calculations from formula (4.40).
2. $k'_b = 0$, which means that R_b is a resistor in series with the memristor R_a so $\alpha = \infty$. By replacing the value of R_b by its value from (4.37), the general expression is given as

$$\left(\frac{R_{in_a} - R_a(t)}{\alpha}\right)\left[(\alpha+1)\left(\frac{R_a(t) - R_{in_a}}{\alpha} + 2R_{in_b}\right) + 2R_{in_d}\right] = 2k'_b\varphi(t)\,. \tag{4.41}$$

   By multiplying both sides by α and taking limit when α tends to ∞, the memristance expression is given as

$$\left(R_a(t) - R_{in_a}\right)\left[R_a(t) + R_{in_a} + 2R_b\right] = -2k'_a\varphi(t)\,. \tag{4.42}$$

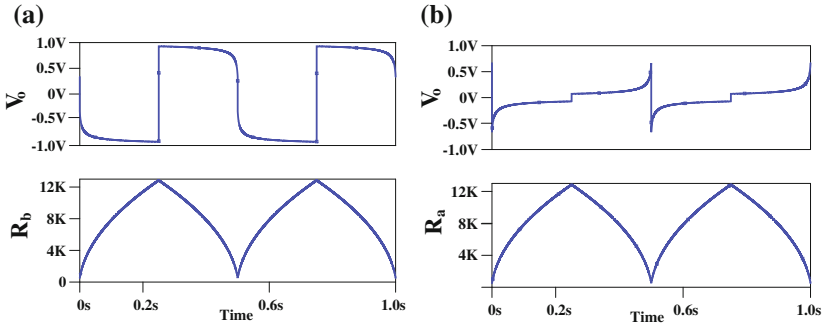

Fig. 4.20 PSPICE simulation of memristance and V_o for **a** case 1: memristance R_b for $R_{in_b} = 1\,\text{k}\Omega$, $R_a = 1\,\text{k}\Omega$ and $k'_b = 379\,\text{M}\Omega^2\,\text{V}^{-1}\,\text{s}^{-1}$, and **b** case 2: memristance R_a for $R_b = 1\,\text{k}\Omega$, $R_{ina} = 1\,\text{k}\Omega$ and $k'_a = 379\,\text{M}\Omega^2\,\text{V}^{-1}\,\text{s}^{-1}$

The previous expression is similar to the first case as is obvious from Fig. 4.20b, where the memristance R_a increases until the input voltage V_{in} changes its state, where R_a reaches 12.848 kΩ for square wave input with amplitude =1 v, frequency = 2 Hz and positive k'_a.

3. $k'_a = k'_b = k'_{ab}$, which means that R_a and R_b are memristors having the same polarities so $\alpha = 1$ as shown in Fig. 4.16a, b. The memristance R_b can be given from

$$\left(R_b(t) - R_{in_b}\right)\left(R_b(t) + R_{in_a}\right) = -k'_{ab}\varphi(t)\,. \tag{4.43}$$

The two memristances R_a and R_b will increase or decrease together depending on the sign of k'_{ab} as $R_a(t) = R_b(t) + R_{in_d}$. Figure 4.21a shows a PSPICE transient simulation of the memristances when applying square wave input, where the maximum $R_b = 10.305\,\text{k}\Omega$, matching the analytic results obtained from (4.43) with relative error = 0.4237 %. Also, the difference between R_b and R_a curves is constant as shown in the figure and is equal to 1 kΩ. In the special case of the previous expression, where $R_{in_b} = R_{in_a} = R_{in}$, the memristance R_b is given as

$$R_b^2(t) = R_{in}^2 - k'_{ab}\varphi(t)\,, \tag{4.44}$$

which is the same expression as the memristance of a single memristor but in the single memristor $k'_{ab} = 2k'$ where $k' = \mp k R_d$. The applied flux is distributed on the two memristors equally (see Fig. 4.16a, b) which makes sense because the voltage is divided across the two memristances as shown in Fig. 4.21a.

4. $k'_a = -k'_b$, which means that R_a and R_b are memristors but with opposite polarities so $\alpha = -1$ (see Fig. 4.16c, d) and $R_a + R_b = R_{in_a} + R_{in_b} =$ constant

$$R_b(t) = R_{in_b} - \frac{k'_b}{R_{in_a} + R_{in_b}}\varphi(t)\,. \tag{4.45}$$

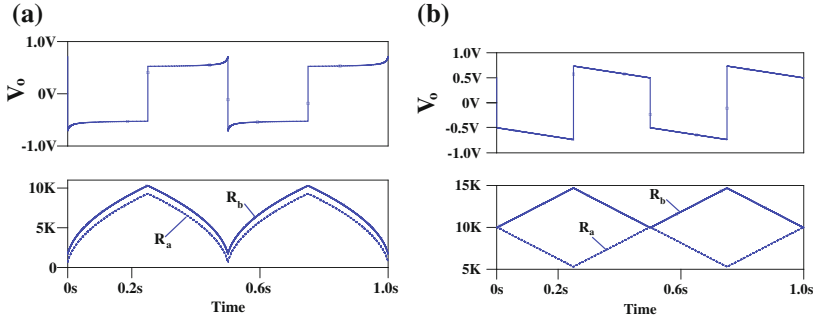

Fig. 4.21 PSPICE transient simulation of the memristances R_a and R_b, and the output voltage for $k'_{ab} = 379\,\text{M}\Omega^2\,\text{V}^{-1}\,\text{s}^{-1}$: **a** at $\alpha = 1$, $R_{in_b} = 2\,\text{k}\Omega$ and $R_{in_a} = 1\,\text{k}\Omega$, **b** $\alpha = -1$, $R_{in_b} = R_{in_a} = 10\,\text{k}\Omega$

The memristance R_b is linear with the applied flux. Moreover, the negative sign of α may result from k'_a or k'_b, thus two cases are available; the first case when k'_a is negative which means that the first memristor is reversed. The memristance R_a increases, and the memristance R_b decreases for positive applied voltage, on the other hand, when k'_b is negative the memristance R_b increases and the memristance R_a decreases if the applied flux is positive and vice versa. Figure 4.21b shows the PSPICE simulation of the memristance in case of $\alpha = -1$, where k'_a is negative and k'_b is positive so the memristance R_a decreases and R_b increases in case of negative applied voltage and vice versa.

4.5 Symmetric Memristive Two-Gate Oscillator

The symmetric memristor-based oscillator circuit consists of two memristors, an inverter and two comparators whose outputs are connected to the NAND gate. The two comparators are used to make sure that the memristor resistance always varies between two limits to achieve the oscillation function at the output of the NAND gate [14]. The two memristors are connected instead of the relaxation RC circuit to emulate the behavior of the charging and the discharging of the capacitor as shown in Fig. 4.22.

4.5.1 Oscillation Concept

The voltage across the two memristors is equal to $V_{o1} - V_o$ due to the structure of the circuit. So the two memristances increase or decrease with a value depending on the memristor polarities and the applied voltage sign until the voltage V_{in} reaches to V_p or V_n, then due to the logic gates, V_o will be inverted and the two memristances change their direction by (decreasing or increasing) with a value until V_{in} reaches V_n or V_p, respectively, as discussed in the previous section when applying a square wave input.

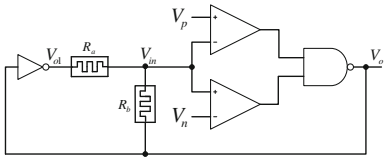

Fig. 4.22 The symmetric memristive two-gate circuit

4.5.2 Mathematical Analysis

The input voltage V_{in} of the two comparators is given as

$$V_{in} = \frac{V_{o1} R_b + V_o R_a}{R_a + R_b}. \tag{4.46}$$

By substituting from (4.37) by the value of R_a into (4.46), we obtain:

$$V_{in} = \frac{(V_{o1} + \alpha V_o) R_b + V_o R_{in_d}}{R_a + R_b}. \tag{4.47}$$

In order to obtain the maximum and minimum resistances which can be achieved by the memristance R_b at $V_{in} = V_p$, R_b will be R_{bp} at $V_o = V_{oh}$, and $V_{o1} = V_{ol}$. Then

$$R_{bp} = \frac{\left(V_{oh} - V_p\right) R_{in_d}}{(\alpha + 1) V_p - (V_{ol} + \alpha V_{oh})}. \tag{4.48}$$

Similarly by replacing V_p, V_{oh} and V_{ol} by V_n, V_{ol} and V_{oh}, respectively,

$$R_{bn} = \frac{(V_n - V_{ol}) R_{in_d}}{(V_{oh} + \alpha V_{ol}) - (\alpha + 1) V_n}. \tag{4.49}$$

For sustainable oscillation, some conditions must be satisfied which are $R_{on} < R_{bn} < R_{bp} < R_{off}$, first for $R_{bn} < R_{bp}$, then

$$\left(V_p + V_n\right) R_{in_d} < (V_{oh} + V_{ol}) R_{in_d}. \tag{4.50}$$

But R_{in_d} may be positive or negative so the condition will be $\left(V_p + V_n\right) < (V_{oh} + V_{ol})$ for positive R_{in_d} but for negative R_{in_d} the condition will be $\left(V_p + V_n\right) > (V_{oh} + V_{ol})$. The other conditions come from $R_{on} < R_{bn}$ and $R_{bp} < R_{off}$ as follows:

$$R_{on} \frac{(V_{oh} + \alpha V_{ol}) - (\alpha + 1) V_n}{V_n - V_{ol}} < R_{in_d} < R_{off} \frac{(\alpha + 1) V_p - (V_{ol} + \alpha V_{oh})}{V_{oh} - V_p}. \tag{4.51}$$

Consequently, another condition on V_p, and V_n should be obtained as

$$\frac{R_{off}}{R_{on}} > \frac{((\alpha + 1) V_n - (V_{oh} + \alpha V_{ol})) (V_{oh} - V_p)}{((\alpha + 1) V_p - (V_{ol} + \alpha V_{oh})) (V_{ol} - V_n)}. \tag{4.52}$$

Note that the greater-than ">" sign for positive R_{in_d} will be reversed in case of negative R_{in_d}. To derive an expression for the oscillation frequency and the duty cycle, the resistance will change from R_{bn} to R_{bp} through the time of a half cycle (T_{hC}). So by integrating (4.39b) from R_{bn} to R_{bp}, where the applied input voltage is constant and $(V_{o1} - V_o) = (V_{oh} - V_{ol})$. T_{hC} is given as

$$T_{hC} = \frac{\left|R_{bp} - R_{bn}\right| \left((\alpha + 1)\left(R_{bp} + R_{bn}\right) + 2R_{in_d}\right)}{2k'_b \left|V_{o1} - V_o\right|}. \tag{4.53}$$

The circuit is symmetric for T_h and T_L because the time for the memristance to change from R_{bn} to R_{bp} is equal to the time to change from R_{bp} to R_{bn}; so the duty cycle = 50 % and the oscillation frequency f is given as

$$f = \frac{k'_b \left(V_{oh} - V_{ol}\right)}{\left|R_{bp} - R_{bn}\right| \left((\alpha + 1)\left(R_{bp} + R_{bn}\right) + 2R_{in_d}\right)}, \tag{4.54a}$$

$$f = \left| \frac{k'_b \left((\alpha + 1) V_p - V_{ol} - \alpha V_{oh}\right)^2}{R^2_{in_d} \left(V_{oh} - V_{ol}\right)\left(V_{oh} + V_{ol} - V_p - V_n\right)} \frac{\left((\alpha + 1) V_n - V_{oh} - \alpha V_{ol}\right)^2}{\left((\alpha + 1)\left(V_p - V_n\right) - (\alpha - 1)\left(V_{oh} - V_{ol}\right)\right)} \right|. \tag{4.54b}$$

As discussed in the previous section α has four special values:

1. $\alpha = 0$, (i.e. $k'_a = 0$) the maximum and minimum memristances are given by (4.55a) and the oscillation frequency is given by (4.55a) as follows:

$$R_{bp} = R_a \frac{V_{oh} - V_p}{V_p - V_{ol}}, \qquad R_{bn} = R_a \frac{V_n - V_{ol}}{V_{oh} - V_n}, \tag{4.55a}$$

$$f_o = \frac{k'_b \left(V_p - V_{ol}\right)^2 \left(V_n - V_{oh}\right)^2}{R^2_a \left(V_{oh} - V_{ol}\right)\left(V_{oh} + V_{ol} - V_p - V_n\right)\left(V_p - V_n + V_{oh} - V_{ol}\right)}. \tag{4.55b}$$

The conditions for oscillation are given as

$$V_p + V_n < V_{oh} + V_{ol}, \tag{4.56a}$$

$$R_{on} \frac{V_{oh} - V_n}{V_n - V_{ol}} < R_a < R_{off} \frac{V_p - V_{ol}}{V_{oh} - V_p}, \tag{4.56b}$$

2. $\alpha = \infty$, (i.e., $k'_b = 0$) which means that R_b is a resistor and R_a is a memristor so R_a will change its state such that the maximum and minimum resistances R_{ap} and R_{an} should be calculated by substituting from (4.48) and (4.49) into (4.37) and are given as

$$R_{ap} = R_{in_d} \frac{V_p - V_{ol}}{(\alpha + 1) V_p - V_{ol} - \alpha V_{oh}}, \tag{4.57a}$$

$$R_{an} = R_{in_d} \frac{V_{oh} - V_n}{V_{oh} + \alpha V_{ol} - (\alpha + 1) V_n}. \tag{4.57b}$$

By taking limits to (4.57) when α tends to ∞, the memristances, corresponding to V_p and V_n are given as

$$R_{ap} = R_b \frac{V_p - V_{ol}}{V_{oh} - V_p}, \quad R_{an} = R_b \frac{V_{oh} - V_n}{V_n - V_{ol}}. \tag{4.58}$$

By dividing the denominator and numerator of (4.54) by α^3, taking limits at α tends to ∞ and using $\alpha k'_b = k'_a$. The oscillation frequency is given as

$$f_o = \frac{k'_a \left(V_p - V_{oh}\right)^2 (V_n - V_{ol})^2}{R_b^2 \left(V_{oh} - V_{ol}\right) \left(V_{oh} + V_{ol} - V_p - V_n\right) \left(V_{oh} - V_{ol} - V_p + V_n\right)}, \tag{4.59}$$

and the oscillation conditions are given as

$$V_p + V_n < V_{oh} + V_{ol}, \tag{4.60a}$$

$$R_{on} \frac{V_{oh} - V_p}{V_p - V_{ol}} < R_b < R_{off} \frac{V_n - V_{ol}}{V_{oh} - V_n}. \tag{4.60b}$$

3. $\alpha = 1$, (i.e., $k'_a = k'_b$) the maximum and minimum memristances are given as

$$R_{bp} = (R_{in_a} - R_{in_b}) \frac{V_{oh} - V_p}{2V_p - V_{ol} - V_{oh}}, \tag{4.61a}$$

$$R_{bn} = (R_{in_a} - R_{in_b}) \frac{V_n - V_{ol}}{V_{oh} + V_{ol} - 2V_n}, \tag{4.61b}$$

and $R_a = R_b + R_{in_a} - R_{in_b}$. The oscillation frequency

$$f_o = \frac{k'_b \left(2V_p - V_{oh} - V_{ol}\right)^2 (2V_n - V_{ol} - V_{oh})^2}{2 \left(R_{in_a} - R_{in_b}\right)^2 \left(V_{oh} - V_{ol}\right) \left(V_{oh} + V_{ol} - V_p - V_n\right) \left(V_p - V_n\right)}. \tag{4.62}$$

The oscillation frequency is inversely proportional to the difference of the initial memristances R_{in_a} and R_{in_b}, so in case of $R_{in_a} = R_{in_b}$, no oscillation will be obtained which makes sense where V_{in} is always constant, so the output will be constant. But for different initial memristances, R_{in_d} has two cases: positive or negative, for the positive case the conditions for oscillation are given by (4.63), otherwise the conditions for oscillation will be given by changing the less-than sign "<" to the greater than sign ">".

$$V_p + V_n < V_{oh} + V_{ol}, \tag{4.63a}$$

$$R_{on}\frac{V_{oh}+V_{ol}-2V_n}{V_n-V_{ol}} < R_{in_d} < min\left(R_{off}\frac{2V_p-V_{ol}-V_{oh}}{V_{oh}-V_p},\ R_d\right). \quad (4.63b)$$

4. $\alpha = -1$, (i.e., $k'_a = -k'_b$) the maximum and minimum memristances are given as

$$R_{bp} = (R_{in_a} + R_{in_b})\frac{V_{oh}-V_p}{V_{oh}-V_{ol}}, \quad (4.64a)$$

$$R_{bn} = (R_{in_a} + R_{in_b})\frac{V_n-V_{ol}}{V_{oh}-V_{ol}}, \quad (4.64b)$$

and $R_a = -R_b + R_{in_a} + R_{in_b}$. The oscillation frequency is

$$f_o = \frac{k'_b\ (V_{oh}-V_{ol})^2}{2\left(R_{in_a}+R_{in_b}\right)^2\left(V_{oh}+V_{ol}-V_p-V_n\right)}. \quad (4.65)$$

The oscillation frequency is inversely proportional to the sum of the initial memristances R_{in_a} and R_{in_b} and the oscillation conditions are given as

$$V_p + V_n < V_{oh} + V_{ol}, \quad (4.66a)$$

$$\max\left(2R_{on},\ R_{on}\frac{V_{oh}-V_{ol}}{V_n-V_{ol}}\right) < R_{in_d} < \min\left(R_{off}\frac{V_{oh}-V_{ol}}{V_{oh}-V_p},\ 2R_{off}\right). \quad (4.66b)$$

4.5.3 Circuit Validation

In the following circuit simulations, the spice model of the memristor, introduced in [9], is used with Joglekar's window function and doping coefficient $p = 100$. The global setting transient simulation is done using PSPICE simulator for the four special cases, which were introduced in the previous subsection, for the circuit parameters $\{V_{ol},\ V_{oh},\ V_p,\ V_n\} = \{-1\,\text{V},\ 1\,\text{V},\ 0.5\,\text{V},\ -0.75\,\text{V}\}$, and $\left|k'_a\right| = \left|k'_b\right| = 379\,\text{M}\Omega^2\,\text{V}^{-1}\,\text{s}^{-1}$.

Figure 4.23a shows PSPICE transient simulation for $\alpha = 0$ at $R_a = 3\,\text{k}\Omega$ and $R_{b_{in}} = 1\,\text{k}\Omega$ where R_b changes from $R_{bn} = 428.57\,\Omega$ to $R_{bp} = 1\,\text{k}\Omega$. The output voltage V_o oscillates with a frequency of 178.56 Hz giving an excellent matching with the values of the calculated results from (4.54) and (4.55). Also, when α tends to ∞, Fig. 4.23b shows the transient simulation of the memristance R_a which changes from 9 to 21 kΩ and for $R_b = 3\,\text{k}\Omega$ where the oscillation frequency equals 1.7546 Hz which matches the calculated values from (4.58) and (4.59), where k'_a is negative. Similarly, Fig. 4.23c shows the transient simulation of the memristances R_a and R_b for $\alpha = 1$. The memristances R_a and R_b change from 2.3343 to 2.9996 kΩ and

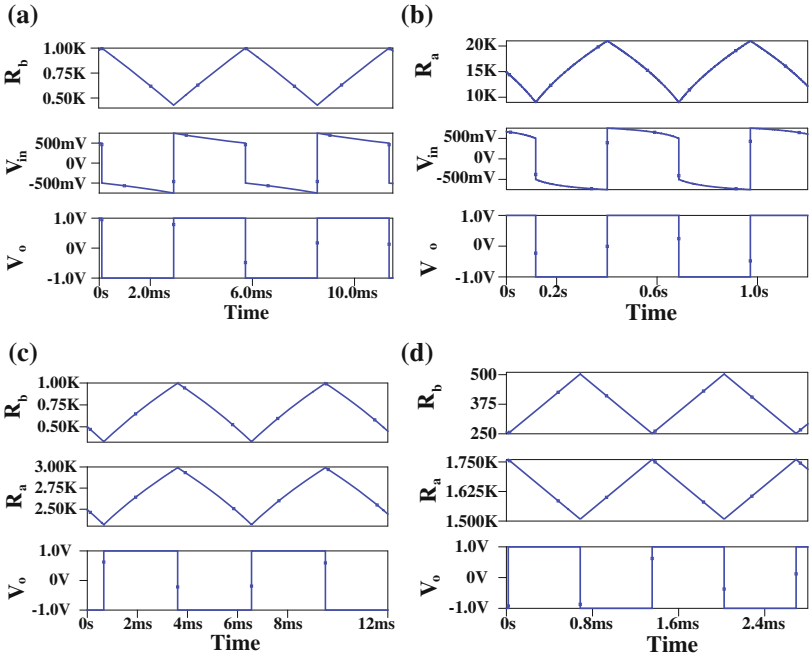

Fig. 4.23 PSPICE transient simulation for **a** $\alpha = 0$, **b** $\alpha = \infty$, **c** $\alpha = 1$, **d** $\alpha = -1$

from 334.423 to 999.6 Ω, respectively, for $\{R_{in_b},\ R_{in_a}\} = \{1\,\text{k}\Omega,\ 3\,\text{k}\Omega\}$ showing a relative error of 0.3269 % with the calculated values, and the oscillation frequency equals 170.52 Hz which matches the calculated frequency value where k'_a and k'_b are positive. Finally, at $\alpha = -1$, Fig. 4.23d shows the transient simulation of the memristances R_a and R_b which change from 1.5087 to 1.7537 kΩ and from 251.751 to 502.216 Ω, respectively, for $\{R_{in_b},\ R_{in_a}\} = \{1\,\text{k}\Omega,\ 1\,\text{k}\Omega\}$ with maximum relative error with the calculated values, showing an error equal to 0.4432 %, and the simulated oscillation frequency equals 745.39 Hz with 1.66 % relative error where k'_a is negative and k'_b is positive.

4.6 Asymmetric Memristive Two-Gate Oscillator

In the previous section, we discussed several special cases of the two-gate memristor-based relaxation oscillator showing the oscillation frequencies and oscillation conditions with a duty cycle of 50 %. This property comes from the symmetric circuit structure. In this section, an asymmetric oscillator will be introduced for one of the special cases which is at $\alpha = 0$ [13]. The conventional way to build an asymmetric oscillator from a symmetric one is by adding a diode in the path of the signal which

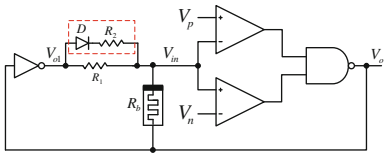

Fig. 4.24 Asymmetric two-gate memristor-based oscillator circuit

will result in an asymmetric circuit due to its behavior by adding a parallel branch to the resistor that consists of a resistor and diode as shown in Fig. 4.24.

4.6.1 Mathematical Analysis

The mathematical analysis of the asymmetric oscillator will be the same as the symmetric one where R_a depends on the current flow direction. When $V_o = V_{ol}$, the diode will be ON by assuming ideal diode (diode will be short circuit) so R_a will be replaced by $R_1//R_2$, otherwise at $V_o = V_{oh}$, $R_a = R_1$. The value of R_a affects the change rate of the memristor's resistance so the time of the positive half cycle will be unequal to the time of the negative half cycle. The resistances R_{mp} and R_{mn} which are corresponding to V_p and V_n are given as

$$R_{mp} = R_1 \frac{V_{oh} - V_p}{V_p - V_{ol}}, \quad R_{mn} = (R_1//R_2) \frac{V_n - V_{ol}}{V_{oh} - V_n}. \tag{4.67}$$

The time of positive and negative half cycle are given as

$$T_h = \frac{(R_{mp} - R_{mn})(2R_1 + R_{mp} + R_{mn})}{2k'(V_{oh} - V_{ol})}, \tag{4.68a}$$

$$T_l = \frac{(R_{mp} - R_{mn})(2R_1//R_2 + R_{mp} + R_{mn})}{2k'(V_{oh} - V_{ol})}. \tag{4.68b}$$

So the oscillation frequency and the duty cycle are given as

$$f_o = \frac{k'(V_{oh} - V_{ol})}{(R_{mp} - R_{mn})(R_1//R_2 + R_1 + R_{mp} + R_{mn})}, \tag{4.69a}$$

$$D = 0.5 \frac{2R_1 + R_{mp} + R_{mn}}{R_1//R_2 + R_1 + R_{mp} + R_{mn}}. \tag{4.69b}$$

The asymmetric oscillator has higher oscillation frequency than the symmetric one due to the parallel branch which reduces the resistance, where $2R_1$ becomes

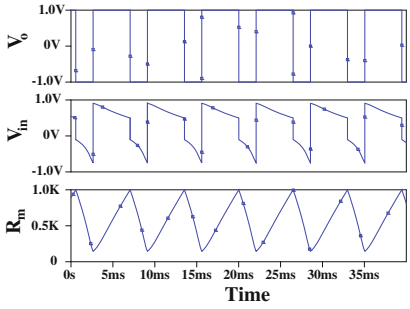

Fig. 4.25 PSPICE transient simulation of asymmetric oscillator

$R_1//R_2 + R_1$. Furthermore, the oscillation frequency and the duty cycle are a function of R_1, R_2, V_p, V_n, V_{ol} and V_{oh} so we have a lot of parameters to satisfy the required behavior. The duty cycle is always larger than 50 % (T_h is larger than T_L) where $R_1//R_2$ is less than R_1. Figure 4.25 shows the PSPICE simulation of the asymmetric oscillator at V_p, V_n, R_1, R_2, V_{oh} and V_{ol} equal to 0.5 V, -0.75 V, 1 kΩ, 3 kΩ, 1 V and -1 V respectively.

The simulated oscillation frequency and duty cycle are equal to 154.27 Hz and 0.6813, respectively, with relative errors equal to 11.737 and 6.875 %, respectively, of the calculated values due to the nonideality of the diode where the simulation is done using D1N4148.

The idea of using a diode to get the asymmetric oscillator could be used in case of $\alpha = \infty$, where R_a is a memristor and R_b is a resistor parallel to a diode and series resistor and a similar expression for the asymmetric oscillator could be obtained.

4.6.2 Discussion and Comparison

In this subsection, comparison between the different cases of α for symmetric topology is made. Figure 4.26 shows the change in oscillation frequency at V_{oh}, V_{ol}, V_n, V_p, k'_a, k'_b, R_{in_a}, R_{in_b} equal to 1 V, -1 V, -0.75 V, 0.5 V, 379 $\mathrm{M\Omega^2\,V^{-1}\,s^{-1}}$, 379 $\mathrm{M\Omega^2\,V^{-1}\,s^{-1}}$, 1 kΩ, 1 kΩ, respectively, for different values of the mismatch factor α. The derived expressions of the oscillation frequency are inversely proportional to the square of the series resistance R_a, and R_b as in case of $\alpha = 0, \infty$ respectively. As shown in Fig. 4.26a, the oscillation frequency at $\alpha = 0$ is higher than at $\alpha = \infty$ for the same parameters in the same common range; also the $\alpha = 0$ case has a wider range of series resistance which means that the oscillation frequency has less sensitivity to change in the series resistance than the $\alpha = \infty$ case. Similarly, in Fig. 4.26b, the oscillation frequency in case of $\alpha = -1$ is higher than the oscillation frequency in the case of $\alpha = 1$ with a wider range relative to the resistance. The maximum or minimum frequencies of the different cases are calculated at minimum or maximum R_{in_d}, respectively, where the oscillation frequency is inversely proportional to R_{in_d}.

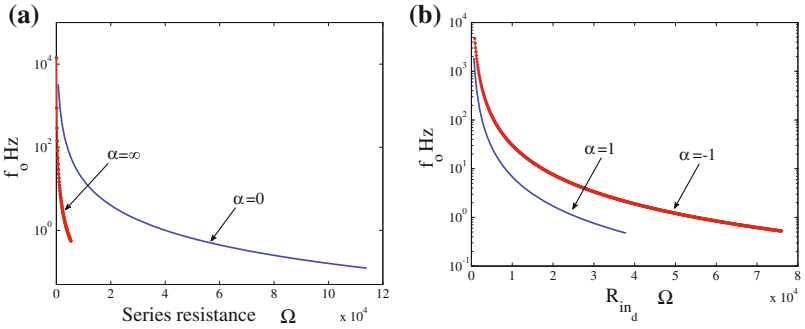

Fig. 4.26 **a** The oscillation frequency versus change of the series resistor for $\alpha = 0,\ \infty$, and **b** the oscillation frequency versus change of the initial memristance R_{in_d} for $\alpha = 1,\ -1$

The oscillation frequency in the cases of $\alpha = 1$ and $\alpha = -1$ depends on the initial state of the memristor R_{in_a} and R_{in_b} according to (4.62) and (4.65) respectively. The oscillation frequency in case of $\alpha = 1$ is inversely proportional to the square of the difference between R_{in_a} and R_{in_b}, so no oscillation can be obtained at $R_{in_a} = R_{in_b}$. On the other hand, the oscillation frequency in case of $\alpha = -1$ is inversely proportional to the square of the sum of R_{in_a} and R_{in_b}. Moreover, the oscillation frequency in the cases of $\alpha = 0$ and $\alpha = \infty$ is independent of the memristor initial state according to (4.55b) and (4.59), which is inversely proportional to the square of the resistances R_a and R_b respectively.

The generalized oscillation frequency (4.54) is proportional to k' which is linearly proportional to the mobility factor of the memristor material, so to get a higher oscillation frequency range a high mobility material should be used.

4.7 Power Consumption of Two Series Memristors

In Sect. 4.4, the analysis of memristance of each memristor was introduced for four different connections. In this section we used these modeling equations in order to calculate the power consumption in each memristor or resistor. As is well known, the power consumed in the two series memristor is given as

$$p(t) = \frac{V_{in}^2}{R_a + R_b} \tag{4.70}$$

and the power consumed in the memristances R_a and R_b are given as

$$p(t) = \frac{V_{in}^2}{R_a + R_b} \tag{4.71}$$

$$p_a(t) = \frac{V_{in}^2 R_a}{(R_a + R_b)^2} \tag{4.72a}$$

$$p_b(t) = \frac{V_{in}^2 R_b}{(R_a + R_b)^2} \tag{4.72b}$$

So the power consumed in the four aforementioned special cases can be studied as follows:

1. $k_a' = 0 (\alpha = 0)$, where memristance R_b is reduced to

$$R_b(t) = -R_a + \sqrt{(R_a + R_{in_b})^2 - 2k_b' \varphi(t)} \tag{4.73}$$

by substituting into (4.71) and (4.72), the consumed power by R_a and the total power consumption are given as

$$p_a(t) = \frac{V_{in}^2 R_a}{(R_a + R_{in_b})^2 - 2k_b' \varphi(t)} \tag{4.74a}$$

$$p(t) = \frac{V_{in}^2}{\sqrt{(R_a + R_{in_b})^2 - 2k_b' \varphi(t)}} \tag{4.74b}$$

Figure 4.27 shows a plot of power consumption of sinusoidal input $v(t) = sin(2\pi f t)$ for $R_a = R_{in_b} = 1\,\text{k}\Omega$, $k_b' = 379\,\text{M}\Omega^2\,\text{V}^{-1}\,\text{s}^{-1}$, and $f = 100\,\text{Hz}$. Figure 4.27b shows the power consumption versus applied voltage where a pinched hysteresis exists even for the power consumption in the resistor R_a.

2. $k_b' = 0 (\alpha = \pm\infty)$, where the memristance R_a reveals

$$R_a(t) = -R_b + \sqrt{(R_b + R_{in_a})^2 - 2k_a' \varphi(t)} \tag{4.75}$$

by substituting into (4.71), the total consumed power is

$$p(t) = \frac{V_{in}^2}{\sqrt{(R_b + R_{in_a})^2 - 2k_a' \varphi(t)}} \tag{4.76}$$

Figure 4.28 shows a plot of power consumption for $R_a = R_{in_b} = 1\,\text{k}\Omega$, $k_a' = -379\,\text{M}\Omega^2\,\text{V}^{-1}\,\text{s}^{-1}$, and $f = 100\,\text{Hz}$. Figure 4.27b shows the power

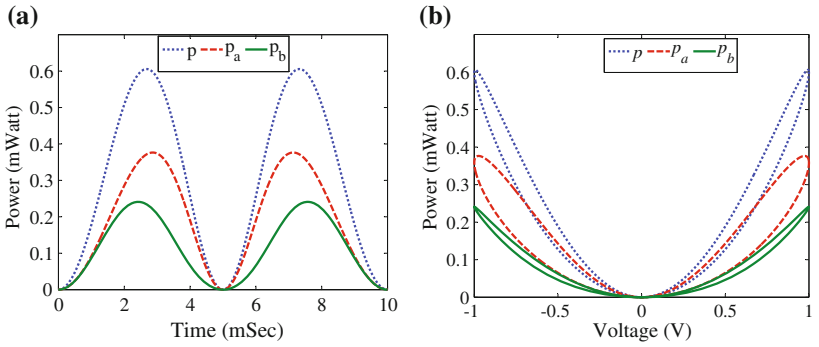

Fig. 4.27 Plot of power consumption in R_a and R_b for $\alpha = 0$

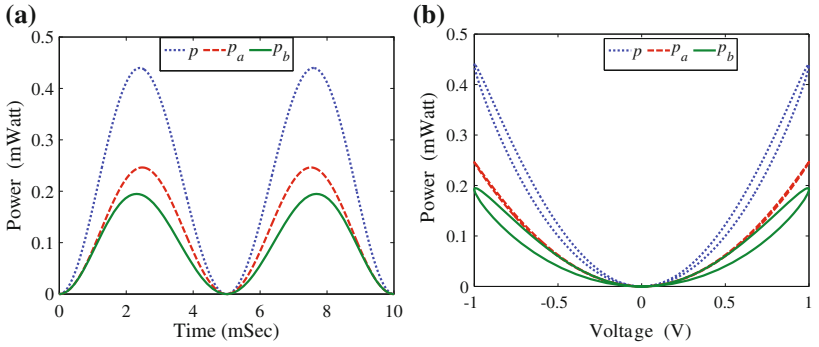

Fig. 4.28 Plot of power consumption in R_a and R_b for $\alpha = \pm\infty$

consumption versus applied voltage where a pinched hysteresis exists even for the power consumption in the resistor R_b.

3. $k'_a = k'_b = k'_{ab} (\alpha = 1)$, the memristances R_a and R_b are

$$R_a(t) = 0.5(R_{in_a} - R_{in_b}) + 0.5\sqrt{(R_{in_b} + R_{in_a})^2 - 4k'_{ab}\varphi(t)} \tag{4.77a}$$

$$R_b(t) = 0.5(R_{in_b} - R_{in_a}) + 0.5\sqrt{(R_{in_b} + R_{in_a})^2 - 4k'_{ab}\varphi(t)} \tag{4.77b}$$

and the consumed power is

$$p(t) = \frac{V_{in}^2}{\sqrt{(R_{in_b} + R_{in_a})^2 - 4k'_{ab}\varphi(t)}} \tag{4.78}$$

Figure 4.29 shows a plot of power consumption for $R_{in_b} = 2R_{in_a} = 2\,\mathrm{k}\Omega$, $k'_{ab} = -379\,\mathrm{M}\Omega^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$, and $f = 100\,\mathrm{Hz}$. Figure 4.27b shows the pinched hysteresis

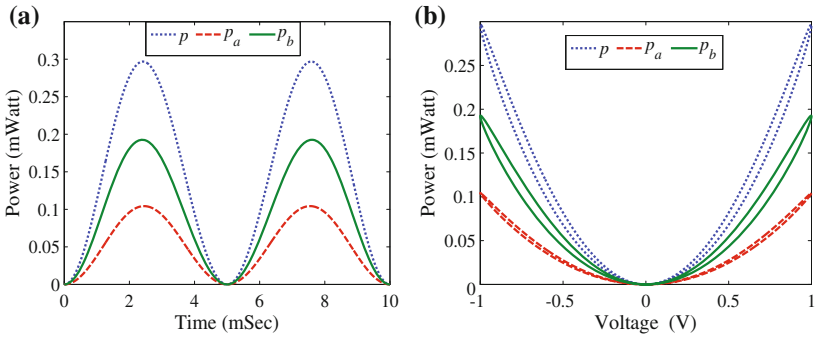

Fig. 4.29 Plot of power consumption in R_a and R_b for $\alpha = 1$

between power consumption and applied voltage where the power consumption in each memristor is pinched and total is pinched.

4. $k'_a = -k'_b (\alpha = -1)$, where the memristance R_a is

$$R_a(t) = R_{in_a} - \frac{k'_a}{R_{in_a} + R_{in_b}} \varphi(t) \tag{4.79}$$

and the consumed power is

$$p(t) = \frac{V_{in}^2}{R_{in_a} + R_{in_b}} \tag{4.80}$$

Figure 4.30 shows a plot of power consumption for $R_{in_a} = R_{in_b} = 1\,\text{k}\Omega$, $k'_a = -k'_b = -379\,\text{M}\Omega^2\,\text{V}^{-1}\,\text{s}^{-1}$, and $f = 100\,\text{Hz}$. It worth to note that the power consumption is pinched for each memristor but the total power consumption is not pinched, since the power consumed in the anti-connected memristances is proportional to the square of the applied voltage. However, in the other three cases, the power consumed has nonlinear pinched relation with the applied voltage.

The power consumption in the memristor-based relaxation oscillators can be calculated using the aforementioned formulas where V_{in} is square wave with amplitude $\pm V_{DD}$ and period T. So we can assume that the power consumption is governed by $p(t) = V_{in}^2 \sqrt{a + b\varphi}$ where $a = (R_{in_a} + R_{in_b})^2$ for all cases and $b = -2k'$ for $\alpha = 0$ and $\pm\infty$ or $b = -4k'$ for $\alpha = 1$ or $b = 0$ for $\alpha = -1$. Therefore, the average power consumption for symmetric oscillator is given as

$$p_{avg} = \frac{1}{T} \int_0^T p(\tau) d\tau = \frac{4}{bT} \sqrt{a + \frac{bV_{DD}T}{2}} \tag{4.81}$$

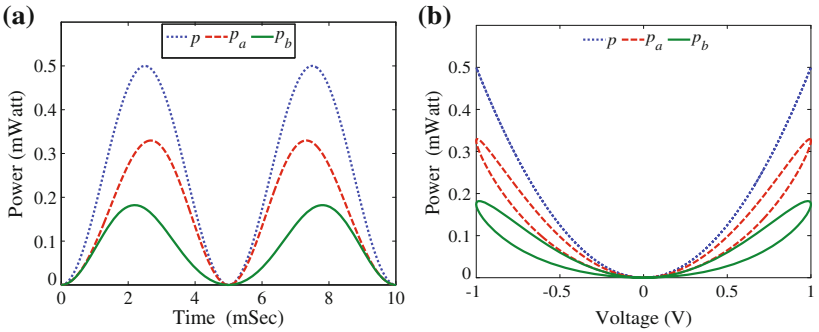

Fig. 4.30 Plot of power consumption in R_a and R_b for $\alpha = -1$

But as previously discussed that the case of $\alpha = 1$ would not oscillate, so there are only three special cases. Also, the initial memristance will be replaced by either R_{mn} or R_{mp}.

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Chapter 5
Memristor-Based Multilevel Digital Systems

5.1 Number Systems

A number system is defined as a writing system for expressing numbers or a mathematical representation of numbers. This system covers a given set of numbers such as integers and rational numbers as shown in Table 5.1.

Mainly, the most famous two types of number systems are as follows:

1. A conventional number system that is positional weighted, nonredundant, and a unique system.
2. A redundant number system in which each number of this system could be represented in more than one way.

where each system has its own advantages and disadvantages [1].

5.1.1 The Conventional Number Systems

The internal representation of numeric values in digital systems such as computers and calculators is called the computer number format where numbers are stored as binary digits. This representation consists of a stream of bits where each bit is capable to save either 1 or 0. This limitation comes from the fact that the hardware realization of each bit is based on transistors which have two levels *ON* or *Off* states. There are many positional systems such as ternary, octal, decimal, and hexadecimal systems whose bases are 3, 8, 10, and 16, respectively. Table 5.2 shows a comparison between different positional systems, and an example of six digits for each of them with its equivalent decimal value. It is clear that the number of digits required to represent any decimal number d is very big in binary and decreases as the base increases from the formula $N_{digits} = int\left(\log_a d\right) + 1$ where the $int(.)$ gives the integer value, a is the base.

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DOI 10.1007/978-3-319-17491-4_5

Table 5.1 Main categories of the number systems

$\mathbb{N}$	Natural numbers	x such that $x \in \{0, 1, 2, 3, \ldots\ldots\ldots\ldots\}$
$\mathbb{Z}$	Integer numbers	x such that $x \in \{\ldots\ldots -3, -2, -1, 0, 1, 2, 3, \ldots\ldots\ldots\}$
$\mathbb{Q}$	Rational number	$\frac{x}{y}$ such that x and $y \in \mathbb{N}$, $y \neq 0$
$\mathbb{R}$	Real number	x such that $x \in (-\infty, \infty)$
$\mathbb{C}$	Complex number	$(x + iy)$ such that x and $y \in \mathbb{R}$, $i = \sqrt{-1}$

Table 5.2 A comparison between binary, ternary, octal, decimal, and hexadecimal systems

System	Base	Set of digits	Example	Decimal value
Binary	2	{0, 1}	1011010	90
Ternary	3	{0, 1, 2}	2101102	1739
Octal	8	{0, 1, 2, 3, 4, 5, 6, 7}	7625423	2,042,643
Decimal	10	{0, 1, 2, 3, 4, 5, 6, 7, 8, 9}	9652863	9,652,863
Hexadecimal	16	{0, 1, 2, 3, 4, 5, 6, 7, 8, 9, *A*, *B*, *C*, *D*, *E*, *F*}	*FA*8*B*59	16,419,673

A number X is represented in this system as follows:

$$X = \sum_{i=0}^{W_d - 1} x_i w_i \tag{5.1}$$

where x_i is the digit value in the ith location which satisfies $(0 \leq x_i \leq r - 1)$, r is the system base, W_d is the word length, and w_i is the weight associated with location i which is equal to r^i. The conventional number system can be represented using different types of representations such as using signed magnitude, complement representation, or binary offset representation. The most widely used number system is the binary number system, with radix 2, numbers in binary domain have different representations using signed magnitude; one's and two's complement.

5.1.1.1 Signed Magnitude Representation

For the binary system, this is the simplest method where the magnitude of the number in binary is written first, then the sign is added at the most left digit; 1 or 0 in case of negative or positive, respectively. An W_d-bits number can be only represented from 0 to $(2^{W_d} - 1)$ for unsigned numbers and from $-(2^{W_d - 1} - 1)$ to $(2^{W_d - 1} - 1)$ in the signed magnitude representations.

5.1.1.2 Complement Representation

Addition and subtraction are performed without the sign of the operand, this is the main advantage of this representation. Positive number is represented normally like

the previous system but the negative number representation is a little bit different,

$$-X = R - X \tag{5.2}$$

where R is selected to be r^k, where k is the number of the digits of that number. So in order to subtract two numbers X *and* Y, the equation is converted from,

$$X - Y \tag{5.3}$$

$$X + (R - Y) \rightarrow R - (Y - X) \tag{5.4}$$

If $Y > X$ then the result does not need any more modifications but if $X > Y$ the result needs a correction to remove the R term which is discarded if $R = r^k$ [2].

There are two alternatives of complement representations which are:

1. Radix complement which is called two's complement in the binary system.
2. Diminished radix complement (which is called one's complement in the binary system.

5.1.1.3 Binary Offset Representation

The representation is exactly like the two's complement except for the sign bit which is complemented. Table 5.3 shows the four different realizations of the decimal values between -7 and 7 using signed magnitude, one's complement, two's complement, and the binary offset representations using 4 bits.

5.1.1.4 Ternary Number System

In 1840 an English inventor, Thomas Fowler introduced for the first time a new method of performing math using ternary base system [3]. Following his lead, in 1958 two Russian inventors Sergei Sobolev and Nikolay Brusentsov developed a ternary electronic machine named Setun [4]. Donald E. Knuth wrote in his book Art of Computer Programming, "Perhaps the prettiest number system of all, is the balanced ternary notation" [4]. It also differs from the normal ternary representation as it uses different set $(-1, 0, 1)$ rather than $(0, 1, 2)$. Each digit location in balanced ternary represents either adding or subtracting a power of 3. Fractional numbers work in a similar way but in this case the digits after the decimal point are represented as a power of 3^{-1}. A given example of a balanced ternary number is the decimal number 21 which can be represented in balanced notation: $1\bar{1}10$, this numeral is interpreted as: $1x3^3 - 1x3^2 + 1x3^1 + 0x3^0$, or $27 - 9 + 3 - 0$, in decimal notation. Balanced ternary has a lot of advantages such as the $\pm$ consistency cuts down the carry-in multiplication process, and the addition table has only two symmetric carries instead of three. Moreover, the negative notation makes the system more efficient in all arithmetic

Table 5.3 A comparison between the four different realizations using 4 bits

Decimal	Signed Magnitude				One's complement				Two's complement				Binary offset representation			
-8	-	-	-	-	-	-	-	-	1	0	0	0	0	0	0	0
-7	1	1	1	1	1	0	0	0	1	0	0	1	0	0	0	1
-6	1	1	1	0	1	0	0	1	1	0	1	0	0	0	1	0
-5	1	1	0	1	1	0	1	0	1	0	1	1	0	0	1	1
-4	1	1	0	0	1	0	1	1	1	1	0	0	0	1	0	0
-3	1	0	1	1	1	1	0	0	1	1	0	1	0	1	0	1
-2	1	0	1	0	1	1	0	1	1	1	1	0	0	1	1	0
-1	1	0	0	1	1	1	1	0	1	1	1	1	0	1	1	1
0	1 0	0 0	0 0	0 0	1 0	1 0	1 0	1 0	0	0	0	0	1	0	0	0
1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	1
2	0	0	1	0	0	0	1	0	0	0	1	0	1	0	1	0
3	0	0	1	1	0	0	1	1	0	0	1	1	1	0	1	1
4	0	1	0	0	0	1	0	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	1	0	1	0	1	1	1	0	1
6	0	1	1	0	0	1	1	0	0	1	1	0	1	1	1	0
7	0	1	1	1	0	1	1	1	0	1	1	1	1	1	1	1

operations, so no need for an extra bit for the sign. Brian Hayes claims that the ternary-based system is the most efficient economical radix of all integer systems [5]. Nowadays, many applications like sigma-delta modulated processor [6] and ternary optical computers [7] use ternary adders due to the advantages mentioned before.

Table 5.4 shows the normal ternary system or using three digits where the last digit represents the sign digits which are either 0 or 2 for positive and negative values. The two's complement of these values are listed in the second columns where the new digits (except the sign digit) can be obtained by subtracting each digit from 2. Three's complement is the same as the two's complement after adding 1 in the negative values as discussed before. The last column illustrates the balanced ternary representation without sign digit as the negative and positive numbers use same digits as discussed before.

Table 5.4 Normal, complement, and balanced ternary system

Decimal	Normal Ternary			Two's complement			Three's complement			Balanced Ternary		
-8	2	2	2	2	0	0	2	0	1	$\bar{1}$	0	1
-5	2	1	2	2	1	0	2	1	1	$\bar{1}$	1	1
-3	2	1	0	2	1	2	2	2	0	0	$\bar{1}$	0
-1	2	0	1	2	2	1	2	2	2	0	0	$\bar{1}$
0	2 0	0 0	0 0	2 0	2 0	2 0	0	0	0	0	0	0
1	0	0	1	0	0	1	0	0	1	0	0	1
2	0	0	2	0	0	2	0	0	2	0	1	$\bar{1}$
3	0	1	0	0	1	0	0	1	0	0	1	0
6	0	2	0	0	2	0	0	2	0	1	$\bar{1}$	0

5.1.2 Redundant Number Systems

From the previous discussion, the conventional radix r systems use $\{0, 1, 2, \ldots, r-1\}$ set and any number can be written in a unique representation. However in the redundant number systems, more than r digits are used to represent any number in radix r system, for example, the ternary system with base 3 can be represented using the digit set $s_1 = \{0, 1, 2, 3\}$ or $s_2 = \{-2, -1, 0, 1, 2\}$. Therefore, the number $10)_{Decimal}$ can be written as $31)_{s_1}$ and $101)_{s_1}$ based on the set s_1 and similarly for other cases. The extra digits increase the representation flexibility which means that any number can be represented by different ways (not a unique representation). It is clear that as the extra degrees of freedom increase the alternative representations increase for the same number. One of the main advantages of the redundant number system is its speed in the arithmetic operations by eliminating the carry from rippling (carry-free addition) [8–10]. The next section gives a brief introduction about two different types of redundant number systems.

5.1.2.1 Signed Digit Code

Signed Digit Code (SDC) is a redundant number system similar to the binary representation except that each digit x can take more than one of two values '0' or '1', it takes one of three values '−1', '0,' or '1'. By using this representation, the addition can be performed without any carry propagation delay, i.e., carry-free addition and subtraction, which leads to another improvement in multiplication units of this system as discussed in [2].

5.1.2.2 Canonic Signed Digit Code (CSDC)

Canonic Signed Digit Code (CSDC) is a special case of the signed digit code where it is not possible to have two nonzero consecutive digits; i.e., $x_i x_{i+1} = 0,\ 0 \leq i \leq W_d - 2$. The conversion is accomplished by converting any string of consecutive 1's to a series of zeroes between 1 and $\overline{1}$ while the series of $\overline{1}$ is converted to a series of zeroes between $\overline{1}$ and 1. For example, 1110_{SDC} is equivalent to $100\overline{1}0_{CSDC}$ and $\overline{111}_{SDC}$ is equivalent to $\overline{1}001_{CSDC}$. Removing consecutive nonzero digits will remove any carry propagation which will speed up the arithmetic operations. Figure 5.1 shows a comparison between the addition of two numbers 10_d and 2_d using the traditional binary method and also based on the CSDC method.

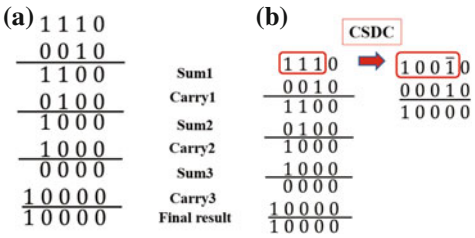


Fig. 5.1 The addition of two numbers using **a** conventional binary system and **b** CSDC method

5.2 Addition and Subtraction Circuits

There are many types of adders these days but most of them face problems with speed as they all are dependent on the size of the operands that are added or subtracted. Creating an adder that is independent on operand length is impossible under conventional number systems so investigating unconventional number systems like the redundant base system leads to overcome the problem of rippling carry. Other adders that are working under conventional systems introduce reasonable comparison between complexity and speed, the next section highlights some of the famous adder/subtract circuits built in the conventional systems, the main difference between addition and subtraction circuits is that the negative value is needed to be converted to two's complement representation before the addition is completed.

5.2.1 Ripple-Carry Adder (RCA)

The ripple-carry adder possesses the simplest architecture of all adders [2], the main building block for this adder is the full adder. It consists of three XORed inputs that represent the sum of the block, and majority circuit that represents the carry, the block diagram of the full adder is shown in Fig. 5.2a. By cascading full adder blocks, a larger adder could be created as seen in Fig. 5.2b. Size and speed of the adder is dependent on the input operand. Two inputs X, Y with length W_d could be added by connecting blocks of full adder with its carry-out connected to the next adder carry-in. The sum and carry can be calculated sequentially starting from least significant bit (LSB) rippling the carry through all adders till it reaches the MSB.

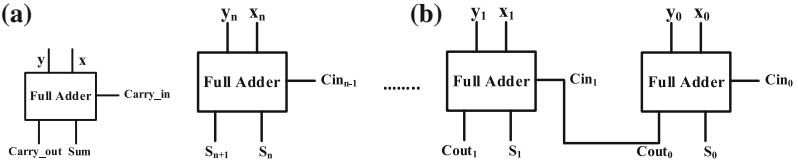


Fig. 5.2 **a** Full adder block diagram. **b** Ripple-carry adder architecture

The speed of the RCA can be determined by the propagation time of the carry which is in the order of W_d.

5.2.2 Carry-Lookahead Adder (CLA)

The Carry-Lookahead Adder (CLA) was introduced for the first time by Weinberger and Smith [11] as a tree-like circuit in order to compute the carry [12, 13]. Reducing the time for the propagation of the carry to $(log_2(W_d))$ [2] can be achieved by writing the equation of the carry in a recursive way based on propagating and generating signals. Propagated and generated signals are two signals coming from direct observation of the truth table of the full adder circuit as shown in Table 5.5.

There are three different cases for the carry: "killed" which means that the output carry is equal to "0" independent of C_{in}, "generated" which means that the output carry is equal to "1" independent of C_{in}, or "propagate" which depends on the XORing between X and Y. Therefore, the carry equation of a general block K can be written as:

$$C_{0,k} = G_K + P_K C_{0,k-1} \tag{5.5}$$

Then by using a recursive method the output carry could be rewritten as a function of all previous carries as follows:

$$C_{0,k} = G_K + P_K(G_{K-1} + P_{K-1}(\cdots + P_1(G_0 + P_0 C_{i,0}))) \tag{5.6}$$

5.2.3 Carry-Select Adder

The carry-select adder is a way to speed up the addition process by replicating the hardware and selecting the result via a multiplexer after calculating the actual carry of each stage in a parallel way [14]. There are two types of adders based on this concept linear carry-select adder and the square root carry-select adder. The difference is

Table 5.5 Full adder truth table

X	Y	C_{in}	Sum	C_o	Carry case
0	0	0	0	0	Kill
0	0	1	1	0	Kill
0	1	0	1	0	Propagate 'P'
0	1	1	0	1	Propagate 'P'
1	0	0	1	0	Propagate 'P'
1	0	1	0	1	Propagate 'P'
1	1	0	0	1	Generate 'G'
1	1	1	1	1	Generate 'G'

based on how each stage is sized, the square root carry-select is much faster than the normal linear one.

5.2.4 Carry-Skip Adder

The carry-skip adder consists of partitions; each partition is simply an RCA block with a skipping pass for the carry [15]. The ANDing of the propagate signals $p_i = a_i \oplus b_i$ is used as a selection of the multiplexer shown in Fig. 5.3 where the input carry has a direct path. This method reduces the time for the propagation of the carry to the order $\sqrt{W_d}$ by dividing the adder into smaller adders where the carry is generated, propagated, or killed depending on the input to these adders [2].

The comparison of the ripple, linear select, and square root select adders were presented in [15] where the delay versus the number of bits is large in case of ripple select adder, then decreases in the linear select adder case and is smallest in the square root adder architecture. Moreover, the advantages of the Canonic Signed Digit Code (CSDC) in the speed relative to other number systems are detected due to the cancelation of carry propagation which means that the addition of two numbers independent of their size can be carried out in two steps as discussed before.

The question now is what is the best radix from the economical prospective? The answer of this question was presented in [5] where the author introduced a measure for the economical radix, this definition was based on the product of the fractional radix R and the number of digits (width) W to represent a number X. So, the optimized function can be written as $E\,(R, X) = R * \log_R X$ assuming that the radix is a real number $R \in R$. For example, $E\,(10, 100) = 10 \times 3 = 30$, and $E\,(2, 100) = 13.288$. The optimum value of the radix for a fixed X is evaluated by $\frac{\partial E}{\partial R} = 0$ which tends to $R_{optimum} = e$ as proved by [5]. Figure 5.4a shows the function $E(R, X)$ versus $R - X$ plane when $R \in [1.5,\ 10]$ and $X \in [10,\ 10^6]$ where the minimum occurs at $R = e$. Figure 5.4b shows the projection $E - R$ in case of $R \in [1, 10]$ where the minimum curve represents the function at $X = 10$ and the maximum curve when $X = 10^6$. In all cases, the minimum exists when the radix becomes $e \simeq 2.718$. However, the radix should be an integer for real implementation, so this chapter will focus on $R = 3$ which is the closest integer value to the optimum radix.

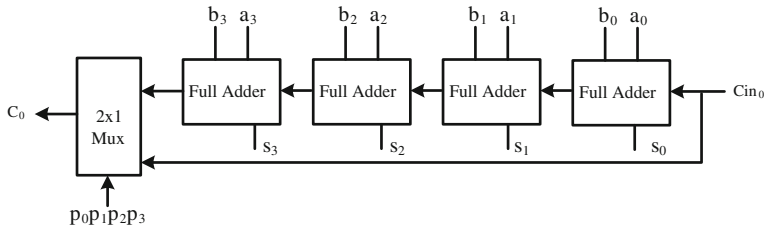


Fig. 5.3 4-bits Carry-skip adder

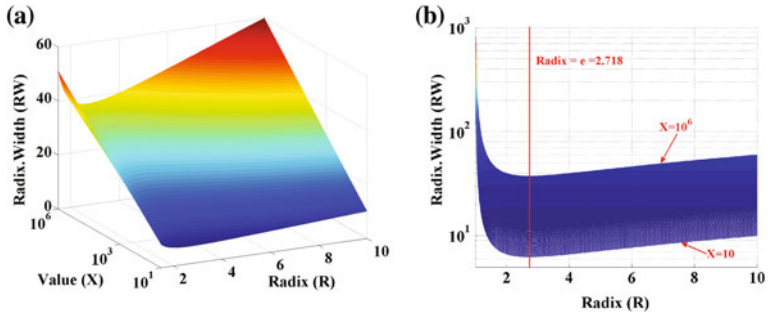


Fig. 5.4 **a** The function $E\,(R, X)$ versus the plane $R - X$, and **b** the $E - R$ projection

The binary system was a mandatory choice since all the hardware implementations are based on the transistor level which has two digital states ON and OFF which represent "1" and "0," respectively. Therefore, there was a need for a device which can handle more than two states. The idea of this chapter is to make use of the Memristor properties to have any number of levels that will help us in the realization of any radix system.

5.3 Memristor-Based Digital Circuits

Recently, many research papers have investigated the use of the memristor in arithmetic-based circuits either by different architectures and/or different concepts. The basic arithmetic operations which are addition, subtraction, and multiplication are discussed in this chapter using the memristor as a supporting element like a switch to build circuits that perform these operations. The advantages of using the memristor are related to the advantages of different radix, nanoscale device, power consumption, and area. Theoretically, any number of states can be designed using the memristor by mapping the memristance range into discrete ranges as required. So, multilevel memories and multilevel arithmetic units can be available in the near future based on memristors.

5.3.1 Memristor Quantization

The quantization concept of the memristance into N equally spaced ranges with guarding gaps has been investigated recently in [16–19]. The memristance continuous range varies between two parameters R_{on} and R_{off}, which defines the minimum (R_{on}) and the maximum (R_{off}) resistance values of the memristor. That range of resistance can be divided into N levels where each level represents a certain value

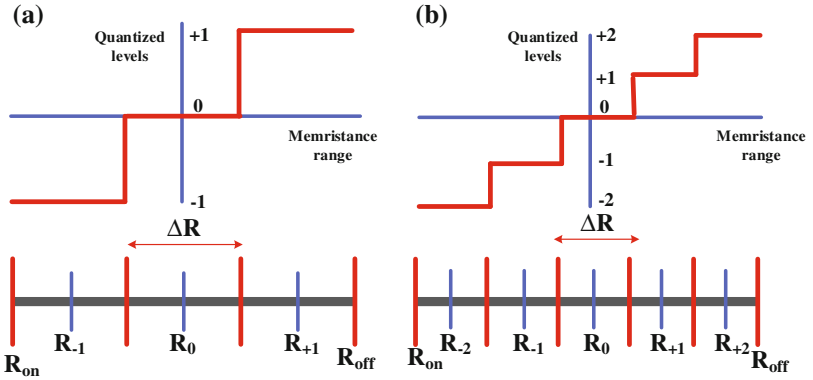


Fig. 5.5 Memristor quantization **a** three levels, and **b** five levels

(nominal value). Each nominal value has a range of resistances ΔR around it, which is considered to be the margin of this level. Figure 5.5 shows how the memristance range could be divided in case of three levels as shown in Fig. 5.5a and five levels as in Fig. 5.5b where the margin for each range ΔR is reduced as the number of levels increases.

Simply for equispaced levels, the memristance range with each level is given by:

$$\Delta R = (R_{off} - R_{on})/N \tag{5.7}$$

The nominal value of each region is defined as:

$$R_{center,n} = R_{on} + (2n-1)\frac{\Delta R}{2} \; where \; n = 1, 2, \ldots N \tag{5.8}$$

For example, if the number of levels is three then $\Delta R = (R_{off} - R_{on})/3$. Using HP nominal values [20] for both $R_{on} = 100\,\Omega$ and $R_{off} = 16\,k\Omega$, their center values are $\{R_{-1},\ R_0, R_1\} \approx \{2.5\,k\Omega, 7.5\,k\Omega, 12.5\,k\Omega\}$ with margins from $\{100\,\Omega, 5\,k\Omega, 10\,k\Omega\}$ to $\{5\,k\Omega, 10\,k\Omega, 16\,k\Omega\}$, respectively. It has been suggested to use a guarding gap between each two regions to prevent false detection of the region [16] especially with small N. It can be easily noticed that if the number of levels increases, the size of each region ΔR becomes smaller which raises the difficulty of detecting the region with good accuracy. Also sometimes it could be a better idea to divide the region in an unequal way based on the probability of occurrence.

5.3.2 One Memristor One Transistor Circuit

In [21], the authors used a passive memristor, a switch and a pulse generator to perform logic operations as shown in Fig. 5.6a and its equivalent memristor-based cell in Fig. 5.6b, where the signal $P(t)$ is the reading signal, and $I(t)$ is the input signal. If the input is "1" then the current flow inside the memristor and the memristance increases however "0" means hold status. After that the reading signal $P(t)$ is applied to extract the internal memristance value and to activate a path from the memristor to the output signal $y(t)$. It is worth mentioning that after the reading phase, the inverse of the input signals should be applied to return the memristor back to its initial value which is called the resetting mechanism.

5.3.3 Doublet Generator Circuit

The doublet generator circuit [22] shown in Fig. 5.7 consists of one memristor, four switches (from T_1 to T_4), and a current source. If T_1 (T_2) and T_4 (T_3) are *on*, the direction of the current source will feed the negative (positive) terminal, and the other terminal will be connected to the ground as shown in Fig. 5.8a, b. Otherwise,

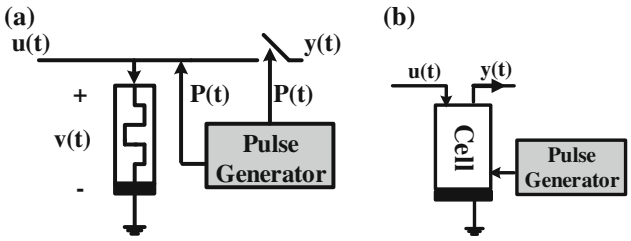
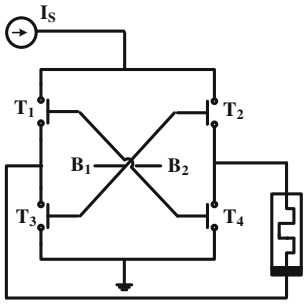


Fig. 5.6 **a** Memristor-based cell, and **b** equivalent cell

Fig. 5.7 Doublet generator memristor-based circuit



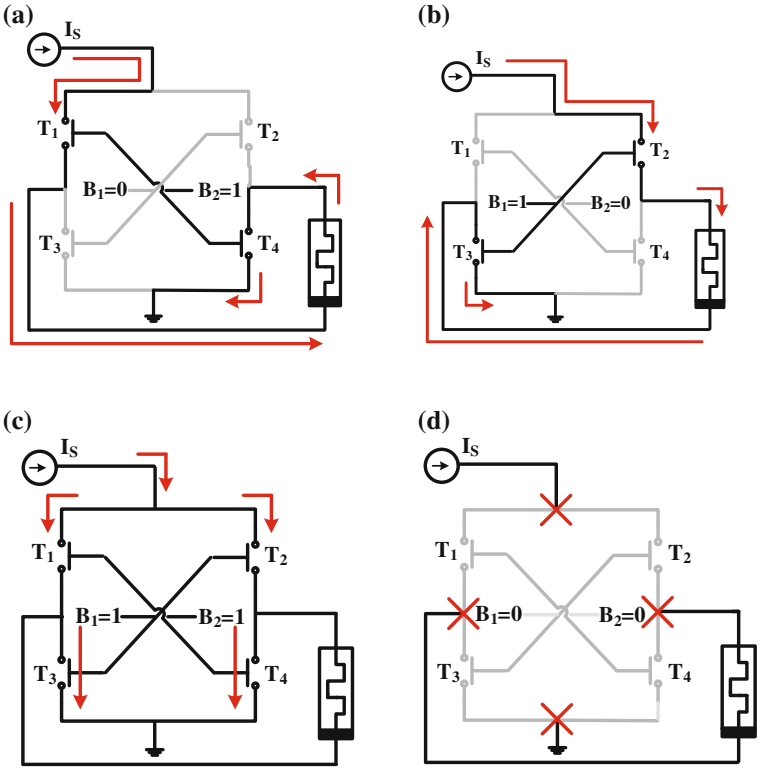


Fig. 5.8 Doublet generator memristor-based different cases **a** $T1$ and $T4$ are *on*, **b** $T2$ and $T3$ are *on*, **c** all switches are *on*, **d** all switches are *off*

if all switches are off (or on) at the same time, the current source will no longer feed the memristor as shown in Fig. 5.8c, d.

Assuming a linear dopant memristor [20], the memristance is given by:

$$R_m(t) = R_{off} - \left(R_{off} - R_{on}\right) x(t), \quad \frac{dx(t)}{dt} = \pm k i(t) \tag{5.9}$$

Since the current is constant in the double generator circuit, then the change in the memristance can be written as:

$$\Delta R_m(\Delta t) = \left| k\, I_s \left(R_{off} - R_{on}\right) \Delta t \right| \tag{5.10}$$

where "I_s" is the current source and "Δt" is the width of the input signals "$B_2 B_1$." The pulse width could be calculated to change the memristance value from one state to another. So, the value of ΔR_m can be controlled via k, I_s, $\left(R_{off} - R_{on}\right)$, *or* Δt. Let the memristor parameters k, R_{off}, *and* R_{on} be as in the HP paper [20], the current

$I_s = 0.5\,\text{mA}$, then the pulse width can be calculated to change the memristance change ΔR_m based on the required number of levels.

Since the memristor memorizes the current that is passed through it and its final memristance depends on the input signals, so there is a need to reset the memristor to its initial value (original state) by reversing the current which is the resetting mechanism. For the doublet generator circuit, if the input is "10" which means that $B_2 = 1$ and $B_1 = 0$, then after reading the memristor there is a need to apply the resetting to return back the memristor to its initial state. This can be achieved by applying the reverse polarity of the input $B_2 = 0$ and $B_1 = 1$ which is equivalent to reversing the current passing through the memristor. Another resetting technique can be applied as introduced in [19].

5.4 Memristor-Based Adder/Subtraction Circuits

5.4.1 Memristor-Based Ternary Half Adder Circuit

The first ternary half adder/subtraction circuit was presented in [23] using balanced ternary notation $\{\bar{1}, 0, 1\}$ which has many advantages as follows:

1. Better for the representation of positive and negative numbers
2. No sign bit is needed
3. Easier in the addition/subtraction process.

The truth table of the half adder ternary circuit is shown in Table 5.6, where X and Y are the inputs of the half adder circuit, Sum and Carry are the outputs of the half adder. Therefore, there are five different states of the output as shown in Fig. 5.9a.

By observing these states it can be noticed that the memristance continuous range should be divided into five regions. These regions (states) are not divided equally as they have different probabilities. For example, the state R_0 is the result of three different input cases; $\{0, 0\}$, $\{1, -1\}$ or $\{-1, 1\}$ while the state R_{-2} is the result of adding two negative ones together $\{-1, -1\}$ which is one case only. Figure 5.9b shows how the memristance range is divided between these five regions. Note that for cascading purposes, it is required to resolve the output into sum and carry where each of them

Table 5.6 Balanced ternary half adder truth table

X	$\bar{1}$	$\bar{1}$	$\bar{1}$	0	0	0	1	1	1
Y	$\bar{1}$	0	1	$\bar{1}$	0	1	$\bar{1}$	0	1
$\text{Sum})_{decimal}$	-2	-1	0	-1	0	1	0	1	2
Sum	1	$\bar{1}$	0	$\bar{1}$	0	1	0	1	$\bar{1}$
Carry	$\bar{1}$	0	0	0	0	0	0	0	1
State	R_{-2}	R_{-1}	R_0	R_{-1}	R_0	R_1	R_0	R_1	R_2

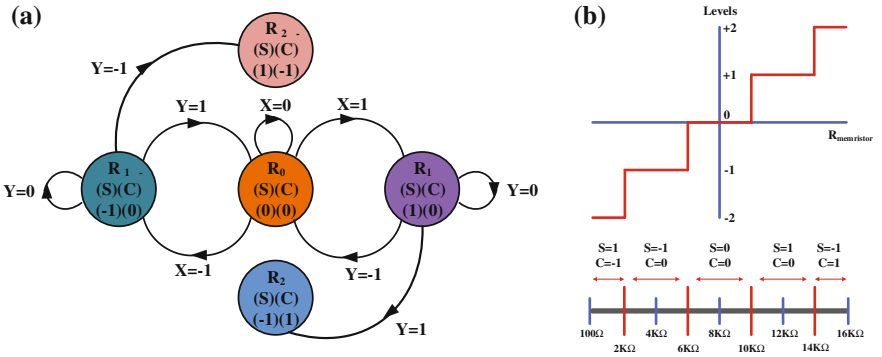


Fig. 5.9 **a** Balanced ternary half adder output distinct states, and **b** memristor-balanced ternary quantization levels

Table 5.7 Balanced ternary memristance regions

Region	From	To (kΩ)	Average (kΩ)
R_{+2}	100 Ω	2	1
R_{+1}	2 kΩ	6	4
R_0	6 kΩ	10	8
R_{-1}	10 kΩ	14	12
R_{-2}	14 kΩ	16	15

has three levels as the balanced ternary system. The previous state is summarized in Table 5.7, the pulse width is calculated to give jump on the memristance equal to 4 kΩ.

Figure 5.10 depicts the expected result of adding two bits together using one memristor and one transistor cell in a serial way where I_{ij} is the normalized input current. After the inputs enter, the reading signal $P(t)$ will be applied, followed by a reverse version of previously entered signals to reset the memristor to its initial state again. For the first addition process as an example, two positive ones are added together, after that a reading signal $P(t)$ is used to read the memristance followed by two negative ones to reset the memrsitor. The memristance starts to increase with the applied input current then it increases again under the applied $P(t)$ at this moment the memristance is laid in the upper region. Sum_M is the voltage across the memristor after rescaling to have the range from -2 to 2 under the applied reading signal $P(t)$, the last two subfigures are the normalized sum and carry of the actual result that is needed. The glitch that appears is due to the reading pulse which increases the memristance in the first half cycle and decreases it in the second part of the reading pulse. To convert the five levels into a balanced ternary system, the extreme cases R_{+2} and R_{-2} are somehow needed to be converted into "1" and "-1," respectively, in the carry as shown from Table 5.6. So, Fig. 5.11 shows a modified architecture of the adder circuit which consists of four memristors M_1, M_2, and M_3 for the Sum part

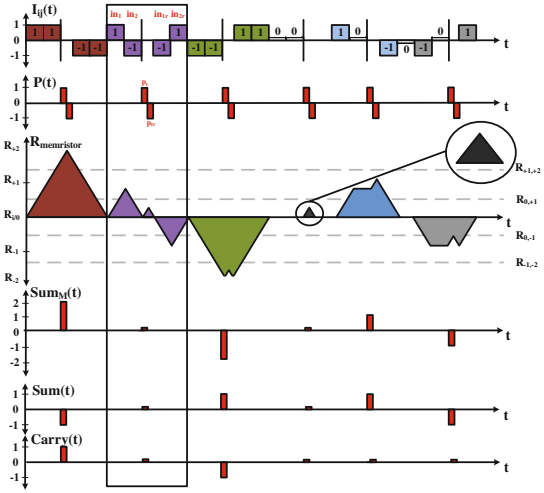


Fig. 5.10 Sequence of adding two values using 1M1T

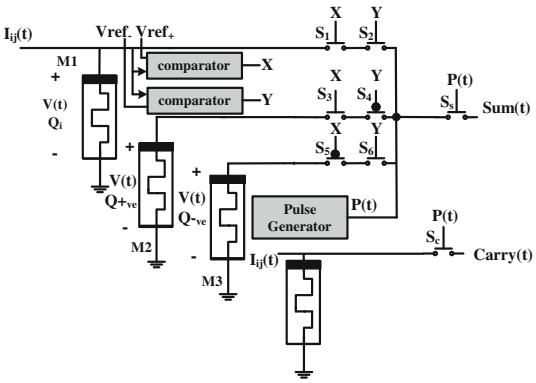


Fig. 5.11 Ternary half adder circuit

Table 5.8 Comparator output in different regions

Region	X	Y
$R_m > R_{+1,+2}$	0	1
$R_{-1,-2} < R_m < R_{+1,+2}$	1	1
$R_{-1,-2} > R_m$	1	0

and M_4 for the carry part, two comparators, a pulse generator, and some switches. The first memristor M_1 works exactly as the $1T1M$ logic cell, the memristance equivalent value corresponding to the polarity of the input signal is calculated and then compared using the two comparators. The purpose of the comparators is to detect if the memristance is located in the two outer regions as shown in Table 5.8. The output of these comparators X and Y are then used to feed six switches that control the multiplexer [23].

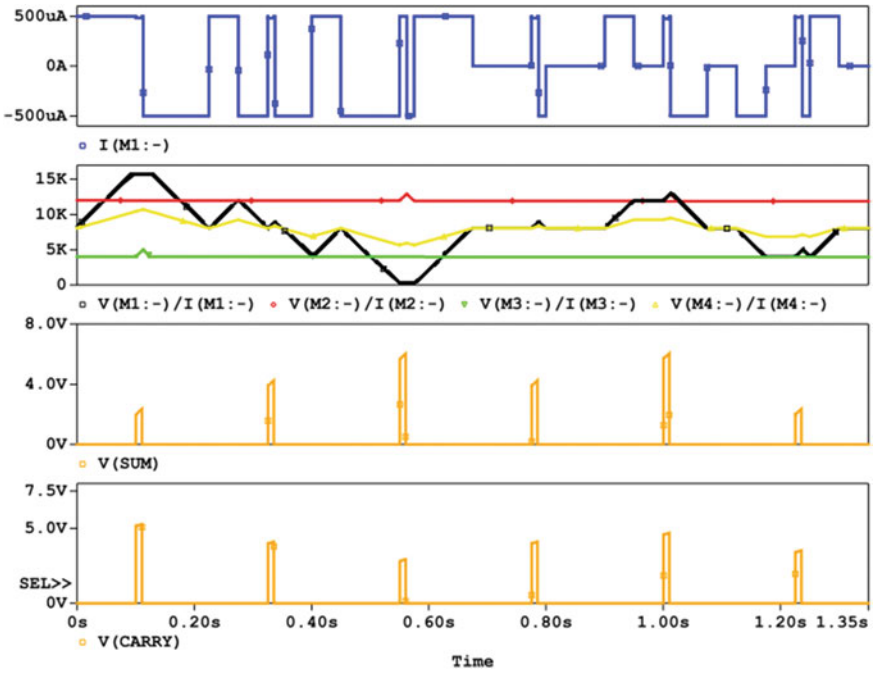


Fig. 5.12 Simulation result for half adder memristor-based circuit

Figure 5.12 shows the simulation results for the previous circuit using OrCad. The memristor model used is based on the Biolek model [24], with $p = 10$, $u_v = 10f$, $R_{on} = 100\ \Omega$, and $R_{off} = 16\,\text{k}\Omega$, all switches are idea switches with $V_{on} = 1\,\text{V}$ and $V_{off} = 0\,\text{V}$. The first subfigure is the applied input in current form I. For example, assume two positive ones are added together, two inputs with 0.5 mA are applied with pulse width 50 ms for the input and 12.5 ms for the reading pulse. The second subfigure illustrates the change in the memristances and the final two subfigures are the sum and the carry.

5.4.2 Memristor-Based Redundant Half Adder Circuit

As discussed before, the Canonic Signed Digit Code (CSDC) is a special case of Signed Digit Code (SDC), where any two consecutive digits must include at least a "0," so converting from SDC to CSDC can be done by transforming every $[011\ldots1]$ and $\left[01\overline{1}\ldots\overline{1}\right]$ to a series of zeroes between "1" and "−1" $[100\ldots\overline{1}]$ and $[\overline{1}00\ldots1]$, respectively.

Table 5.9 shows the truth table of the CSD redundant binary full adder, where only unique cases are represented as inputs X, Y and Z, while the repeated ones

Table 5.9 Truth table of the redundant full adder

X	-1	-1	-1	-1	-1	0	1	1	1	1
Y	-1	-1	-1	0	1	0	0	1	1	1
Z	-1	0	1	0	0	0	0	-1	0	1
Sum	1	0	-1	-1	0	0	1	1	0	-1
Carry	-1	-1	0	0	0	0	0	0	1	1
Decimal value	-3	-2	-1	-1	0	0	1	1	2	3
Sum 2-bits	01	00	10	10	00	00	01	01	00	10
Carry 2-bits	10	10	00	00	00	00	00	00	01	01

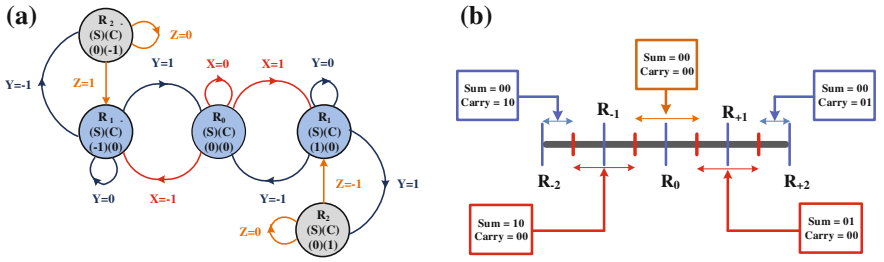


Fig. 5.13 **a** Full adder graph representation, and **b** sum and carry output extraction

are omitted. The two red columns are forbidden cases in the CSD as the appearance of three positive ones or three negative ones are not allowed in this representation. Therefore, five different states from "R_{-2}" to "R_{+2}" are needed where each state represents different values for the sum and the carry as shown in Fig. 5.13a. To represent the CSD into two bits representation to implement a Canonic Signed Digital Redundant Binary Adder (CSDRBA), assume "−1, 0, 1" are mapped into "10, 00, 01," respectively, as shown in the last two rows of Table 5.9. Also, Fig. 5.13b shows the values of the sum and the carry of the redundant adder mapped onto each region of the quantized memristor [25].

$$\begin{array}{r} x_{n-1}\ x_{n-2}\ \ldots\ x_1\ x_0 \\ y_{n-1}\ y_{n-2}\ \ldots\ y_1\ y_0 \\ \hline s_{n-1}\ s_{n-2}\ \ldots\ s_1\ s_0 \\ c_{n-1}\ c_{n-2}\ c_{n-3}\ \ldots\ c_0 \\ \hline z_n\ z_{n-1}\ z_{n-2}\ \ldots\ z_1\ z_0 \end{array} \tag{5.11}$$

The CSDC addition can be always free of the carry propagation by generating the sum value and the carry value in parallel, then adding the carry to the sum, which can also be done in parallel. For example, the addition of $(X = 35)$ and $(Y = -11)$ as in Eq. (5.12); the result equals "24" as expected in two steps where each two bits are being added by a single full adder unit. By speeding up the arithmetic addition

without the carry propagation, the multiplication process could be improved due to the reduction in the number of addition and subtraction cycles. Recently, the concept of canonic signed digit is used in many applications like digital filters [26, 27] and high speed multipliers [28].

$$\begin{array}{r} 100101\bar{1} \\ 0\bar{1}0101 \\ \hline 1\bar{1}0000 \\ 001000 \\ \hline 01\bar{1}1000 \end{array} \tag{5.12}$$

Adding Stage

Figure 5.14 shows the complete schematic of the adding circuit, which consists of a single doublet generator circuit, four comparators, inverters, AND gates, and switches [25, 29]. Two current sources are used, where (I_S) is used for writing on the memristor, and the other ($I_S/1000$) is used for reading. The comparators and the AND gates are used to extract the output sum. The sequence of the adding stage is explained in the flowchart shown in Fig. 5.15.

Figure 5.16 shows the relationship between the voltages of the comparators inside the adding circuit, where the first two comparators (comp1 and comp 2) are used to make "S_1" equal to "1" if the output is in the region "R_{+1}"; while the other two comparators (comp3 and comp4) are used to make "S_2" equal "1" in the region "R_{-1}"; otherwise, the sum should be zero. Note that the output of each comparator will be "1", if the result of multiplying the reading current and the memristance was larger than its reference value.

Moreover, the write and the read signals are used with different current sources in order to have a less destructive effect on the memristance. The current source values

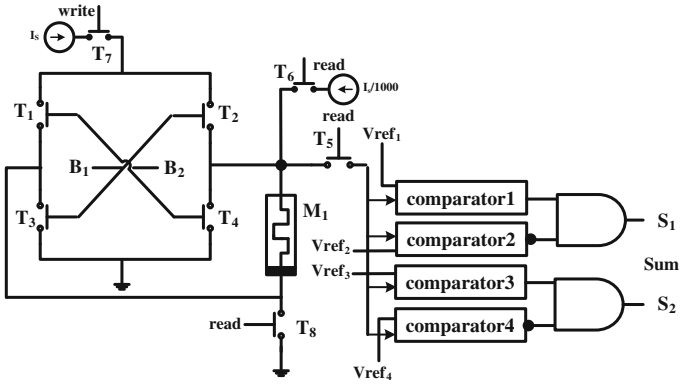


Fig. 5.14 Architecture of the adding stage

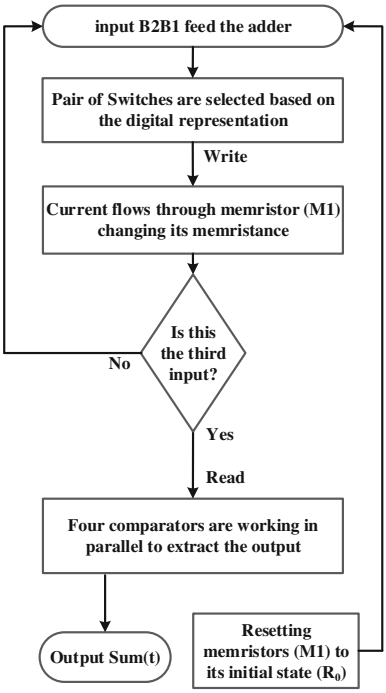


Fig. 5.15 Flow chart of the addition process

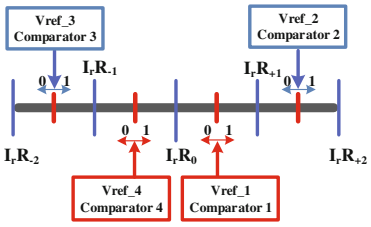


Fig. 5.16 Adding circuit reference voltages

and the pulse width of the input signal are calculated to change the memristance from one nominal value to another on the writing cycle. The comparators' reference voltage values are shown in Fig. 5.16, where "I_r" (the reading current value) is equal to (I_s/1000). Figure 5.17a shows an example of how the addition process is achieved and how the input sequence {00, 00, and 01} affects the memristance value. The write signal is high while the inputs enter the doublet generator in series. The read signal is then activated by connecting the memristor to the reading current pulse of the comparator to extract the output as shown in Fig. 5.17b. Note that all the above sequences assume that the memristor value is pre-initialized to its middle range [29].

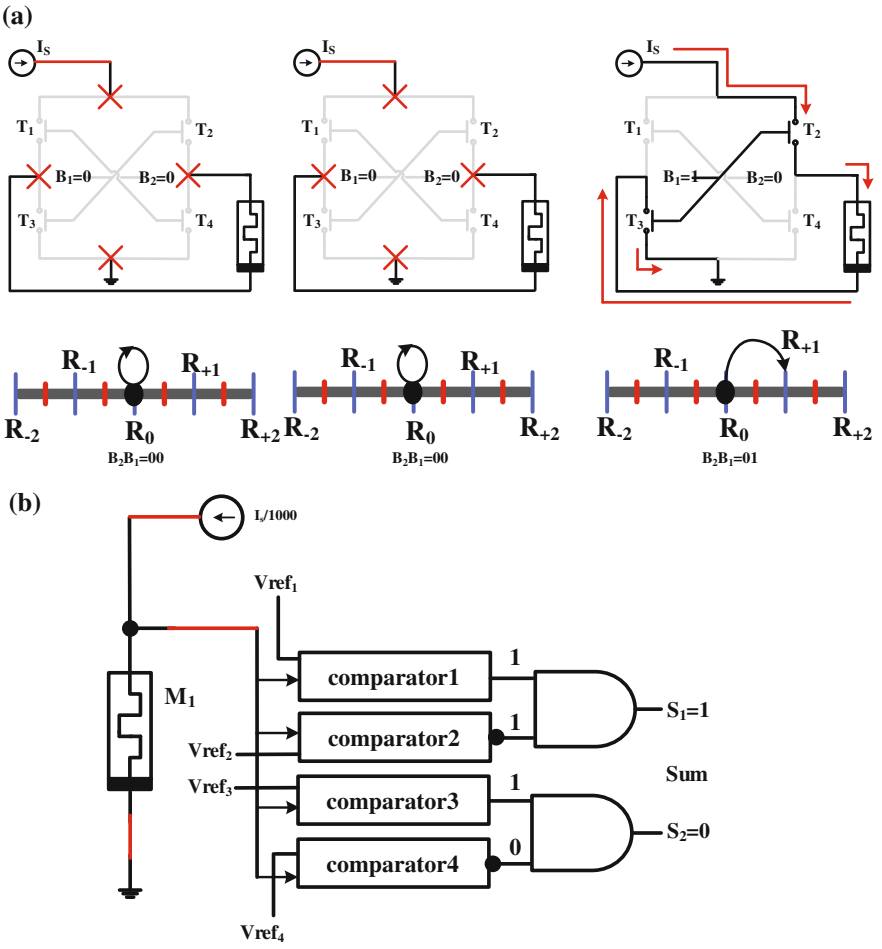


Fig. 5.17 Example of adding {00, 00, 10} **a** writing phase, **b** reading phase

Carry Propagating Stage

Figure 5.18 shows the carry circuit, which has similar architecture to the adding stage except for the comparator part. The least significant bit of the carry will be equal to "1," if the memristance was larger than "V_{ref_2}," then the most significant bit will be equal to "1" if the memristance was less than "V_{ref_3}," and "0" elsewhere. It is worth mentioning that the carry circuit can be removed by using the same circuit of the sum stage to extract the carry directly, but it will prevent cascading the full adder blocks, to build an N-bit adder as will be explained in the next section.

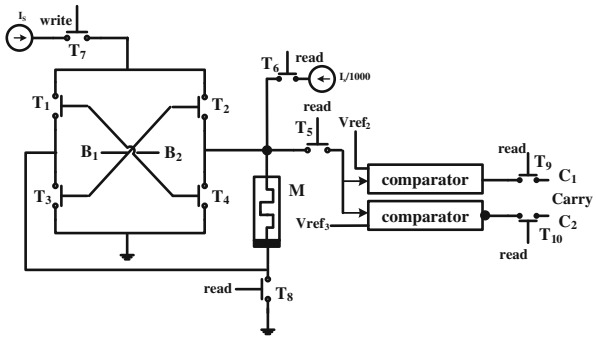


Fig. 5.18 Architecture of the propagating stage

5.4.3 N-Bits CSD Redundant Binary Adder

The block diagram of the full adder is shown in Fig. 5.19a, where "$B_{n2}B_{n1}$" are the inputs of stage "n," which is connected internally to the adding and carry stage switches; "P_{ts}" and "P_{tc}" are the $write/\overline{read}$ signals of the adding and carry stages, respectively, while "$S_{n2}S_{n1}$" and "$C_{n2}C_{n1}$" are the output sum and carry of the full adder [29]. Figure 5.19b shows the architecture of the N-bits Canonic Signed Digital Redundant Binary Adder (CSDRBA). The N-bit adder consists of "N" full adder blocks, two switches for each input and two switches between each stage.

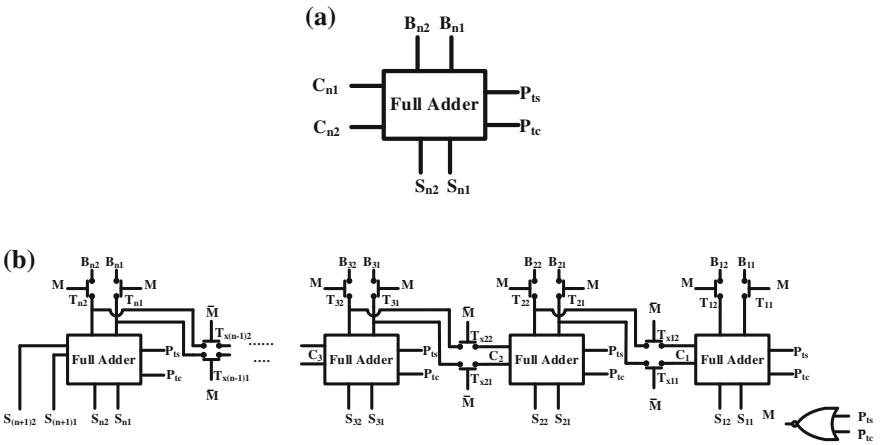


Fig. 5.19 **a** Full adder block diagram, and **b** N-bits CSDRBA

Figure 5.20 shows the signal diagram that explains the addition process sequence as follows:

1. The first two cycles (adding two inputs serially and generating the sum and carry for them):
   a. "M" signal is high for two clock cycles, so all switches from (T_{11}, T_{12}) to (T_{n1}, T_{n2}), which are connected to the input, are *on,* and all switches from (T_{x11}, T_{x12}) to ($T_{x(n-1)1}$, $T_{x(n-1)2}$) between stages are *off*.
   b. Two pairs of input digits enter the full adder serially.
   c. "P_{ts}" and "P_{tc}" are high, which means that writing on the memristors takes place.
2. The third cycle (the carry result propagates to the second stage):
   a. The "M" signal becomes low for one clock cycle, which means that all input switches are *off,* and all switches between stages are *on* (carry propagation).
   b. The "P_{tc}" signal becomes too low to read from the carry stage, while "P_{ts}" remains high, which means that writing is taking place in the adding stage (reading the carry and adding it to the next stage).
3. The fourth cycle (output extraction): "P_{tc}" and "P_{ts}" signals are set low to read the output of the adding block and the carry of the last block, which gives us the final output.

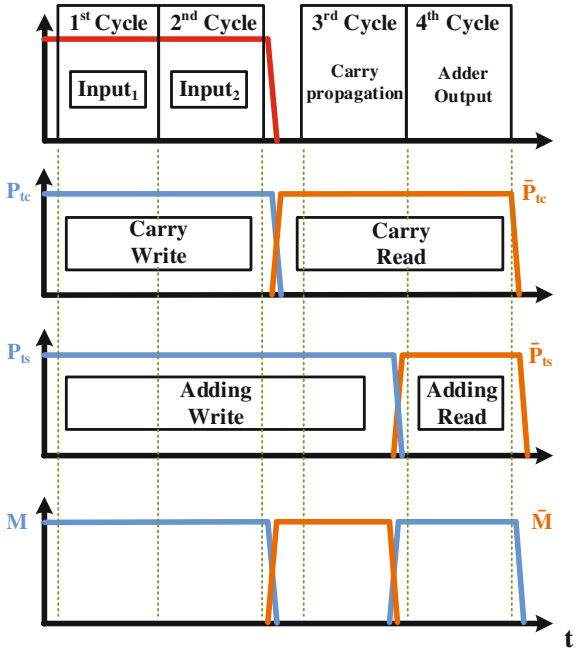


Fig. 5.20 Input and control signals sequence

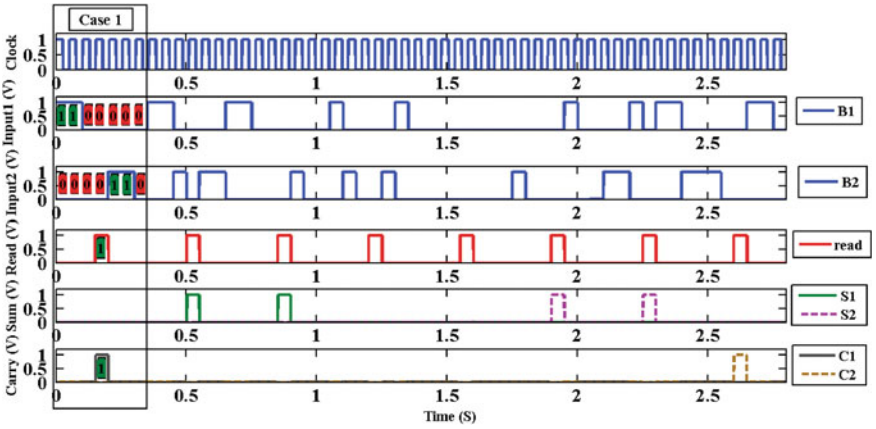


Fig. 5.21 Simulation result of the CSDRBA

5.4.3.1 Simulation Results

Figure 5.21 shows the result of the full adder; "$v(B2)$" and "$v(B1)$" are the most and the least significant bits of the input signal, respectively, following the truth table. "Read" is the reading pulse signal. "Case 1" is an example of the addition process; three inputs {01, 01, 00} are added, followed by a reading signal, then a resetting mechanism should be applied by reversing all previously entered currents {10, 10, 00}. The output is extracted with the reading pulse, leading to sum = 00 and carry = 01; the result exactly matches the truth table. It can be noticed that the input is entered serially, with 50 ms pulse width and a level of 1 V. Each output consists of two bits, representing one of the three states of the redundant digit. Therefore, addition and subtraction of multilevel digital systems can be achieved using memristor-based circuits which have been verified by many examples presented in [29]. Moreover, the next section will address how to build any combinational relationships based on mixed MOS-memristor design circuits.

5.5 Memristor-Based Redundant Multiplier

5.5.1 CMOS Architecture

In CMOS technology any function could be implemented as a network of switches organized into a pull-up network and a pull-down network as shown in Fig. 5.22a. The pull-up network is used to pull the output up to v_{dd} by opening a path from v_{dd} to the output. While the pull-down network is used to pull down the output to the ground. The pull-up network is a combination of PMOS switches connected in

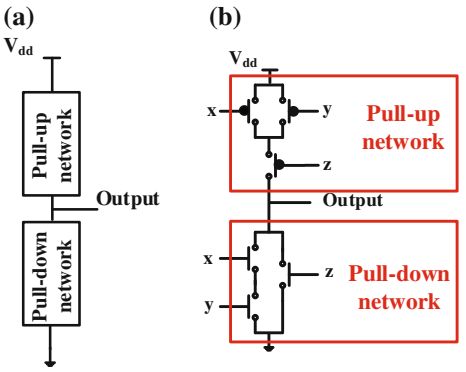


Fig. 5.22 CMOS implementation **a** general architecture, **b** implementation of $F = x \cdot y + z$

series, parallel, or a combination of both that represent the function F. Similarly, the pull-down network is a combination of NMOS switches. To implement a function F using CMOS we build the pull-down network then complement the topology to build the pull-up network, for example if the following function $F(x, y, z)$ is needed to be implemented, $F = x \cdot y + z$ where x, y, and z are the inputs of the function, "." means ANDing the inputs which is converted to series connection in the pull-down network while "+" means ORing the inputs which is converted to parallel connection in the pull-down network. Complement topology means converting each series\parallel connection in pull-down to parallel\series connection in pull-up as shown in Fig. 5.22b.

5.5.2 *Memristor-Based Digital Circuit*

The general implementation of any function using the memristor-based architecture is similar to the CMOS circuit, the pull-down network is replaced with one memristor and a comparator circuit while the pull-up network is built using ideal switches as shown in Fig. 5.23a with current source I_s connected to the memristor via the pull-up

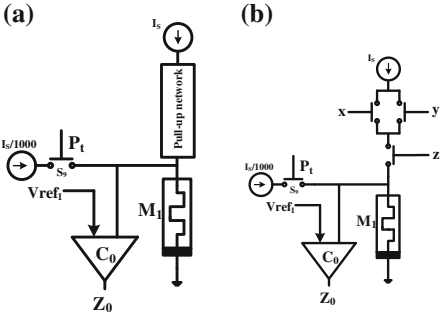


Fig. 5.23 Memristor implementation **a** general architecture, and **b** implementation of $F = x \cdot y + z$

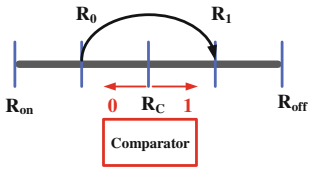


Fig. 5.24 Memristance to bit representation

network [30]. So, when the pull-up network is on, it creates a path from the current source to the memristor. That current will flow and change the memristance then by using a reading signal the memristor will be connected to another current source with lower value to read the memristance then it is compared to the reference V_{ref1}. The memristance changes its value depending on the level of current used I_s and how much time switches in the pull-up network remain open. The output of the circuit is stored as a change in the memristance.

The concept behind building any function is similar to the concept of CMOS circuit, by using the pull-up network to pass the current to the memristor to change its memristance from one state to another then using a comparator to detect that change as shown in the following Fig. 5.24 R_0 is the initial value of the memristance and if the inputs do not create an open path from the current source, no change will happen to the memristance, by using the comparator to compare the memristance to R_C, zero will be detected. On the other hand, if the inputs create an open path for the current source the memristance value will change from R_0 to R_1 crossing the value R_C then by using the comparator the value of the memristance will be greater than the comparing value R_C leading to an output one. In order to build a circuit that drives the same previous function F using the memristor (see Fig. 5.23b), it is achieved by replacing the complete pull-down network with one memristor and a comparator. Note that, inputs are applied in parallel then a reading signal is applied in the next cycle to read the change of the memristance till applying a resetting mechanism to the circuit [30].

Figure 5.25 shows the simulation results of the previous circuit, where the first three subfigures are the inputs x, y, and z, while the fourth and fifth subfigures are the reading signal and the output, respectively. The input enters the circuit in the first cycle followed by a reading phase then a resetting phase thus the sequence will be (write-read-reset). All input combinations have been verified.

5.5.3 Redundant Multiplier

5.5.3.1 Two-Bit Redundant Multiplier Cell

The inputs of the redundant multiplier are in the form of one of three values $\{-1,\ 0\ or\ 1\}$, this representation for the redundant system could be converted to a two-bit representation so the inputs will be $\{10,\ 00,\ and\ 01\}$, respectively. The

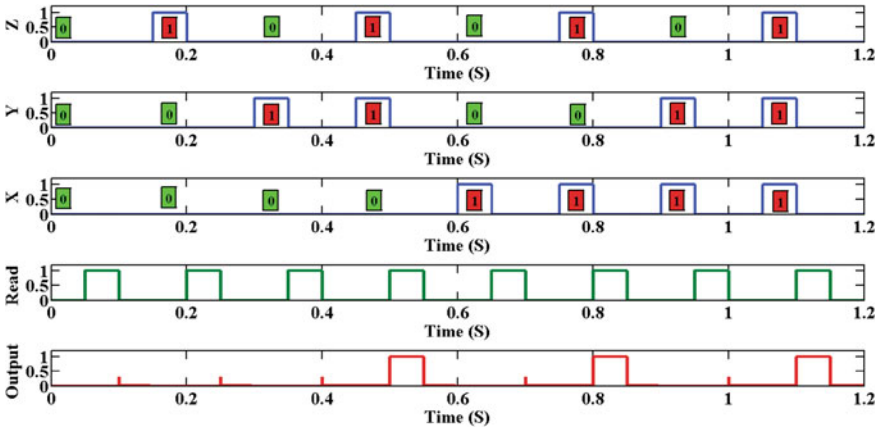


Fig. 5.25 Simulation results for function $F = x \cdot y + z$

Table 5.10 Truth table of the redundant multiplier

A	b	C	A (a1a0)	b (b1b0)	c (c1c0)	AB
0	0	0	00	00	00	0
0	1	0	00	01	00	1
0	−1	0	00	10	00	2
1	0	0	01	00	00	4
1	1	1	01	01	01	5
1	−1	−1	01	10	10	6
−1	0	0	10	00	00	8
−1	1	−1	10	01	10	9
−1	−1	1	10	10	01	10

Table 5.11 Karnaugh map for output c1

			b1			
			b0			
			00	01	11	10
a1	a0	00	0	0	X	0
		01	0	0	X	1
		10	X	X	X	X
		11	0	1	X	0

c1 = a1b0 + a0b1

multiplication table of the redundant multiplier is as follows in Table 5.10, where a, b are the inputs, while c is the multiplier output. $\{a1a0,\ b1b0$, and $c1c0\}$ are the two-bit equivalent representation for a, b, and c, respectively. Using Karnaugh, the Boolean expression of $c1$ and $c0$ could be easily calculated as a function of four inputs $a1a0b1b0$ as shown in Tables 5.11 and 5.12. The implementation of the

Table 5.12 Karnaugh map for output c1

			b1			
			b0			
			00	01	11	10
a1	a0	00	0	0	X	0
		01	0	1	X	0
		10	X	X	X	X
		11	0	0	X	1
c1 = a0b0 + a1b1						

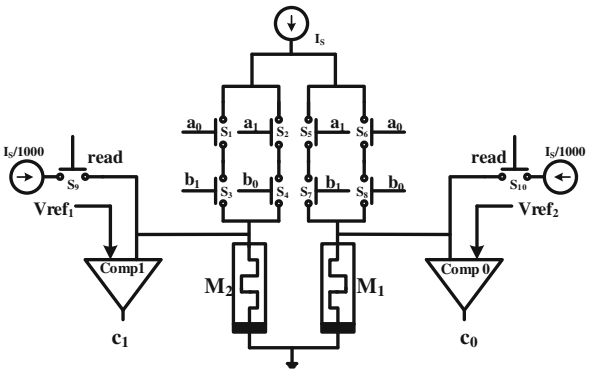


Fig. 5.26 Two-bit multiplier circuit

two-bit redundant multiplier is done using the explained idea where each one of the outputs is a function in four inputs. The switches ($S1$ *to* $S4$) are used to implement function $c0$ while switches ($S5$ *to* $S8$) are used to implement function $c1$. Then the outputs are extracted using two comparators $comp_0$ for function $c0$ and $comp\_1$ for function $c1$ as shown in Fig. 5.26. The simulation result for the two-bit multiplier is shown in Fig. 5.27 where each input consists of two bits that represent three cases, the inputs were ordered in the same order shown in the truth table and the outputs follow the desired response.

5.5.3.2 N×N Memristor-Based Tree Redundant Multiplier

In 1964 Wallace showed an efficient way to implement a multiplier based on a tree-like structure [31]. The implementation is simply based on multiplier cells and full adder circuits as shown in Fig. 5.28 where a 3×3 multiplier of two numbers $X = \{X3X2X1\}$ and $Y = \{Y3Y2Y1\}$ (where each digit can take one of three values $\{-1,\ 0,\ 1\}$), the result of multiplication is then added together generating the output of the multiplier. The multiplier consists of 9 multiplier cells M_C, three redundant binary adders (*RBA*), and some switches. The redundant binary full adder is used to add three pairs of digits and an output pair of digits that represent sum and another pair for the carry. The input to *RBA* is entered in a serial way and it has two control

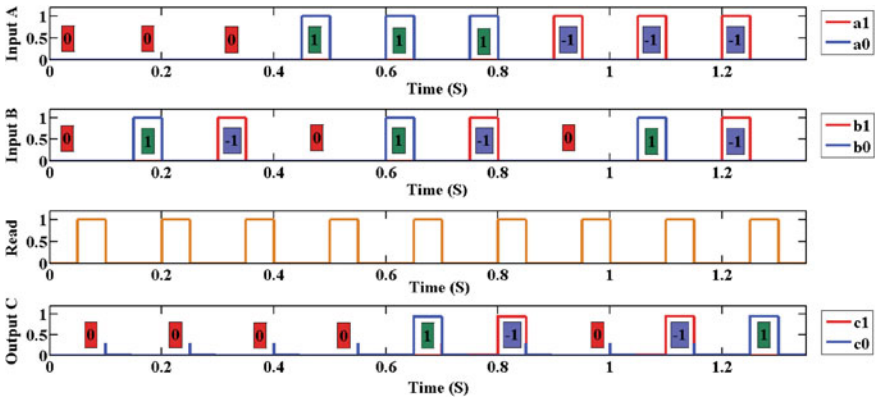


Fig. 5.27 Simulation results for two-bit multiplier circuit

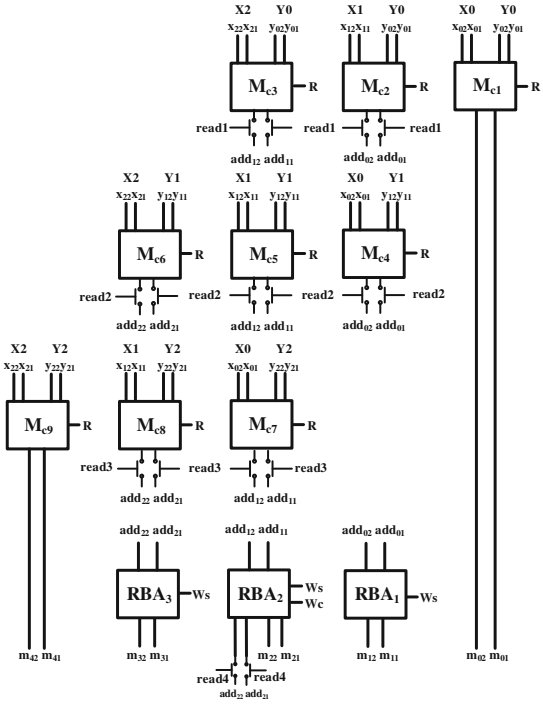


Fig. 5.28 Implementation of 3×3 multiplier

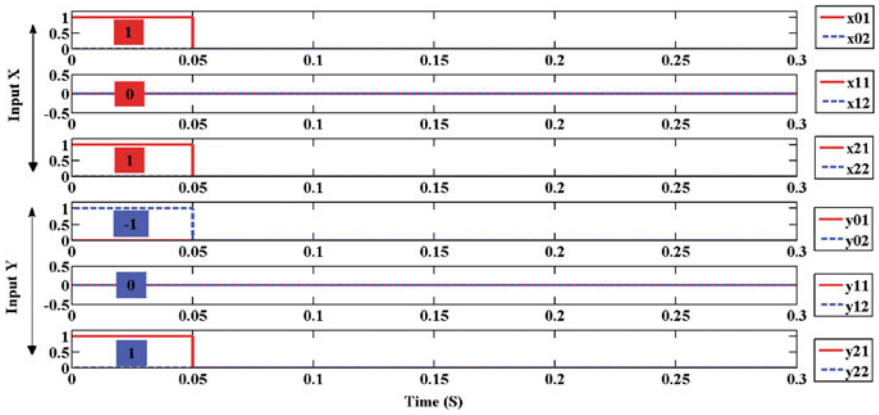


Fig. 5.29 Inputs X and Y of the 3 × 3 multiplier

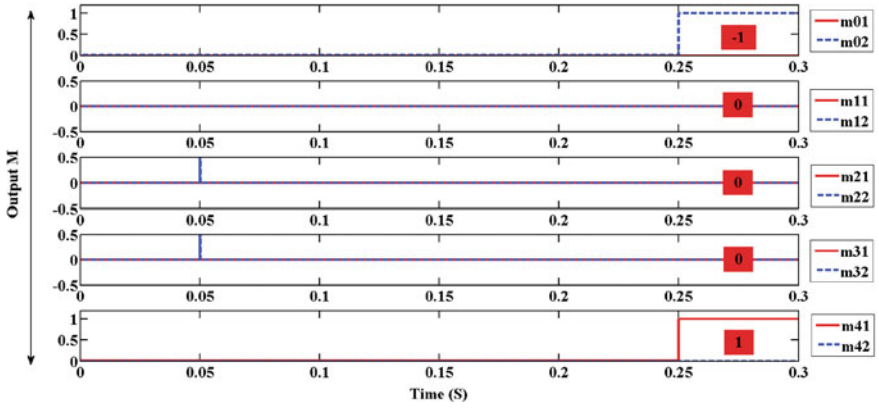


Fig. 5.30 Output M of the 3 × 3 multiplier

signals W_s and W_c which stand to write to the sum and carry stages, respectively. The multiplier works as follows [30]:

1. The inputs enter in pairs to the multiplier cells for one clock cycle
2. First read signal (*read*1) is activated to feed the *RBA* with first level inputs
3. Second read signal (*read*2) is activated to feed the *RBA* with second level inputs
4. Third read signal (*read*3) is activated to feed the *RBA* with third level inputs
5. Fourth read signal (*read*4) is activated to feed the *RBA* with the carry
6. Global read to $Mc1$, $Mc9$, and *RBA* is activated.

To validate the previous procedure, the simulation results for the multiplier circuit are shown in Figs. 5.29 and 5.30, where the input to the multiplier circuit is shown in pairs {10, 00, 01} which represent {−1, 0, 1} where this simulation shows the multiplication when $X = 5$ and $Y = 3$ [30].

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Chapter 6
Memcapacitor: Modeling, Analysis, and Emulators

6.1 Introduction

In 1980, Chua generalized the definition of the axiomatic approach of 2-terminal elements to define an infinite variety of higher order basic circuit elements. Moreover, Chua defined a new general element and named it as the $v^{(\alpha)} - i^{(\beta)}$ *element* [1]. This element has a constitutive relation involving only the 2 variables $v^{(\alpha)}$ and $i^{(\beta)}$ and has a symbol shown in Fig. 6.1. Chua visualized these new elements as a circuit element array shown in Fig. 6.2 where each dot with integer coordinates (α, β) represents a $v^{(\alpha)} - i^{(\beta)}$ element. Hence, the 4 dots with coordinates $(0, 0)$, $(-1, 0)$, $(0, -1)$, and $(-1, -1)$ correspond to a Resistor, Inductor, Capacitor, and Memristor, respectively.

Chua's elementary circuit element quadrangle was extended to include higher order elements: memcapacitor and meminductor as shown in Fig. 6.3 [2]. The two elements, memcapacitor and meminductor, were first postulated at the openingm lecture of the First Memristor and Memristive Systems Symposium held at UC Berkeley in 2008 [3]. The memcapacitance C_m links between the magnetic flux φ and the time integral of the charge σ, while the meminductance L_m provides a relationship between the charge q and the time integral of flux ρ. Figure 6.4 shows the number of publications related to the memcapacitor during the last six years. Note that circuit elements with even higher order dynamics are yet to be defined.

6.1.1 Memcapacitive Systems

In 2009, Di ventra, Pershin, and Chua defined a generalized model for the memcapacitive systems [4], where nth-order voltage-controlled memcapacitive system is defined by

A.G. Radwan and M.E. Fouda, *On the Mathematical Modeling of Memristor, Memcapacitor, and Meminductor*, Studies in Systems, Decision and Control 26,
DOI 10.1007/978-3-319-17491-4_6

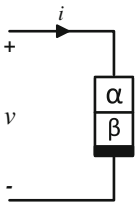

Fig. 6.1 Symbol for a $v^{(\alpha)} - i^{(\beta)}$ element [1]

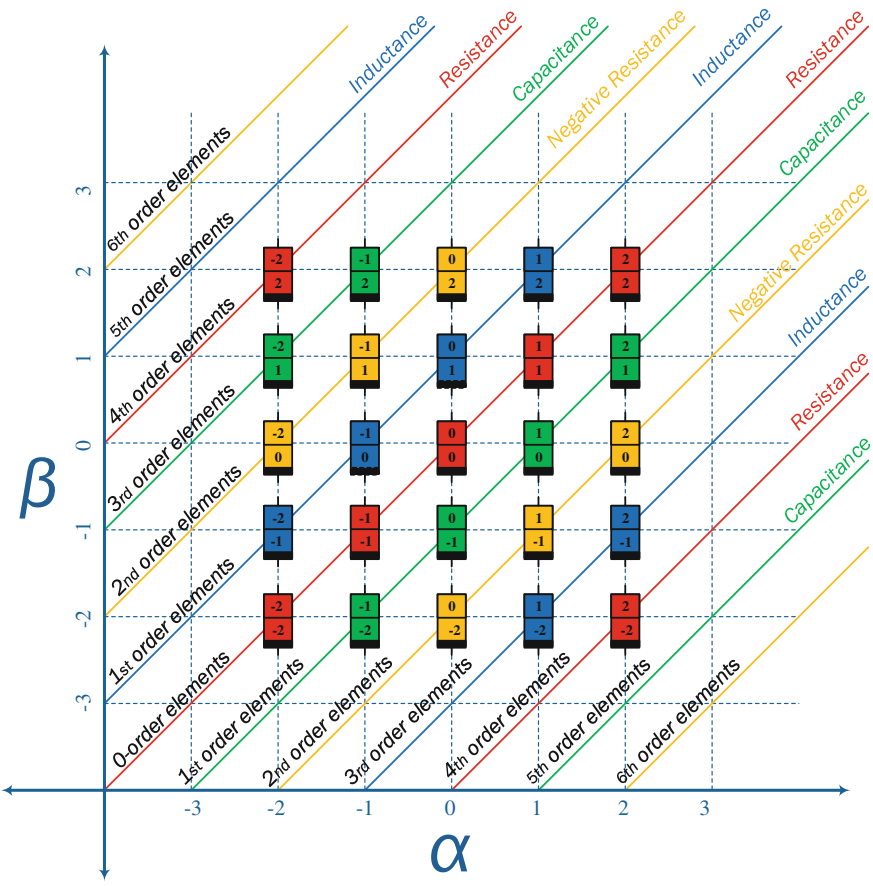

Fig. 6.2 Circuit element array: each *dot* with coordinates (α, β) denotes a $v^{(\alpha)} - i^{(\beta)}$ element [1]

$$q(t) = C(x, V_c, t)V_c(t), \tag{6.1a}$$

$$\dot{x} = f(x, V_c, t), \tag{6.1b}$$

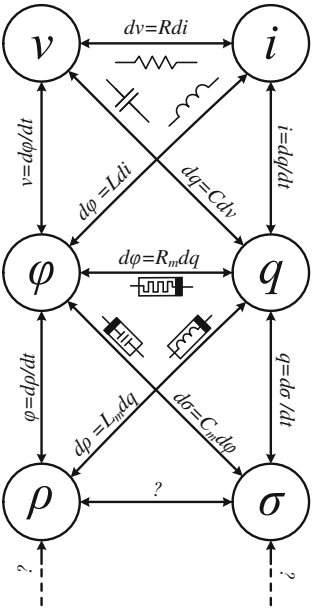

Fig. 6.3 Extension of fundamental passive elements

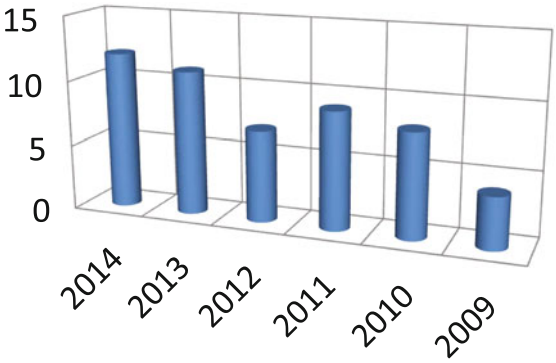

Fig. 6.4 Number of publications during the last 6 years using engineering village database (December 2014)

where $q(t)$ is the charge on the capacitor at time t, $V_c(t)$ is the corresponding voltage, and C is the memcapacitance (for memory capacitance), which depends on the state of the system. Similarly, they defined an nth-order charge-controlled memcapacitive system as

$$V_c(t) = C^{-1}(x, q, t)q(t), \tag{6.2a}$$

$$\dot{x} = f(x, q, t), \tag{6.2b}$$

where C^{-1} is an inverse memcapacitance.

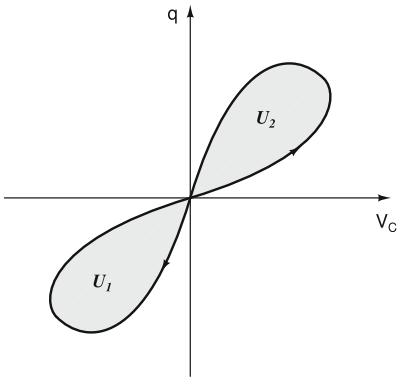

Fig. 6.5 Schematics of a pinched hysteresis loop of a memcapacitive system [4, 5]

They defined a subclass of the memcapacitive devices by deducing the voltage-controlled memcapacitive systems equation to (6.3) to represent the voltage-controlled memcapacitor.

$$q(t) = C\left[\int_{t_o}^{t} V_c(\tau)d\tau\right]V_c(t), \tag{6.3}$$

and the charge-controlled memcapacitive systems equation to (6.4) to represent the nth charge-controlled memcapacitor.

$$V_c(t) = C^{-1}\left[\int_{t_o}^{t} q(\tau)d\tau\right]q(t). \tag{6.4}$$

By the basic definition of the classical circuit theory, every capacitor must be "lossless," i.e., NOT dissipative. So, the memcapacitor should also be a lossless element. Besides, the previous systems should have a pinched hysteresis in the $q - v$ plane at the origin $(q, v) = (0, 0)$ to represent memcapacitor.

Moreover, Di ventra et al. defined the energy stored in the system as

$$P_c = V_c(t)I(t) \tag{6.5a}$$

$$U_c(t) = \int_{t_o}^{t} V_c(\tau)I(\tau)d\tau. \tag{6.5b}$$

Note that the energy of a passive memcapacitive system cannot exceed the amount of previously added energy so $U_c \geq 0$. They defined the energy added to/removed from the system ($\int V_c(q)dq$) as the area between the curve and the q-axis. The areas of shaded regions U_1 and U_2 give the amount of added/removed energy in each half-period. The signs of U_1 and U_2 are determined by the direction on the loop. For the direction shown in Fig. 6.5, U_2 is positive and U_1 is negative. The system is passive if $U_1 + U_2 = 0$, dissipative if $U_1 + U_2 > 0$, and active if $U_1 + U_2 < 0$.

6.1.2 Mathematical Representations of Time-Invariant Memcapacitor

Similar to Chua's representations of the memristor, discussed in Chap. 2, three mathematical representations of time-invariant memcapacitors are defined. Each representation has two forms; charge-controlled memcapacitor or voltage-controlled memcapacitor. These three representations can be breifly presented as follows:

6.1.2.1 Extended Memcapacitor

An extended memcapacitor is defined as

- Charge-controlled extended memcapacitor

$$v = C^{-1}(x, q)q = D(x, q)q, \tag{6.6a}$$

$$\frac{dx}{dt} = f(x, q), \tag{6.6b}$$

  where $\lim_{q\to 0} D(x, q) \neq \infty$.
- Voltage-controlled extended memcapacitor

$$q = C(x, v)v, \tag{6.7a}$$

$$\frac{dx}{dt} = g(x, v), \tag{6.7b}$$

  where $\lim_{v\to 0} C(x, v) \neq \infty$.

These extended memristor is the same to Di ventra's definition, discussed in the previous section, but with adding a condition on the constitutive relation.

6.1.2.2 Generic Memcapacitor

A generic memcapacitor is defined in

- Charge-controlled generic memcapacitor

$$v = D(x)i, \tag{6.8a}$$

$$\frac{dx}{dt} = f(x, i), \tag{6.8b}$$

- Voltage-controlled generic memcapacitor

$$q = C(x)v, \tag{6.9a}$$

$$\frac{dx}{dt} = g(x, v), \tag{6.9b}$$

6.1.2.3 Ideal Memcapacitor

An ideal memcapacitor is defined as

- Charge-controlled ideal memcapacitor

$$\varphi = \varphi_1(q). \tag{6.10}$$

Or

$$v = D(\sigma)q, \tag{6.11a}$$

$$\frac{d\sigma}{dt} = q, \tag{6.11b}$$

where $D(\sigma) = \frac{d\varphi_1(\sigma)}{d\sigma}$ is called memelastance in inverse Farad (F^{-1}). The constitutive relation of charge-controlled ideal memcapacitor can be recovered to $\varphi_1(\sigma) = \varphi_0 + \int_0^t D(\sigma)d\sigma$ where φ_0 is an arbitrary constant.

- Voltage-controlled ideal memcapacitor

$$\sigma = \sigma_1(\varphi). \tag{6.12}$$

Or

$$q = C(\varphi)v, \tag{6.13a}$$

$$\frac{d\varphi}{dt} = v, \tag{6.13b}$$

where $G(\varphi) = \frac{d\sigma_1(\varphi)}{d\varphi}$ is called memcapacitance in Farad (F). The constitutive relation of voltage-controlled ideal memcapacitor can be recovered to $\sigma_1(\varphi) = \sigma_0 + \int_0^t C(\varphi)d\varphi$ where σ_0 is an arbitrary constant.

6.1.3 Physical Realizations

A lot of prospective research on the realization of the solid-state memcapacitor has been started [6–9]. In 2009, Bratkovski et al. introduced a realization for a memcapacitor device which included two electrodes and a memcapacitive matrix interposed between them [6]. The mobile dopants are contained within the memcapacitive matrix and are repositioned within the memcapacitive matrix by applying the programming voltage across the two electrodes to change the capacitance of the memcapacitor. Also, another memcapacitor device includes a memcapacitive matrix interposed between two electrodes where the capacitance of the memcapacitor device depends upon an initial voltage applied across the memcapacitive matrix and gives results similar to the analysis introduced in the coming sections [10].

In 2009, Martinez et al. suggested a possible realization of a solid-state memcapacitive system [7]. Their approach relied on the slow polarization rate of a medium between plates of a regular capacitor. The multilayer structure is formed by metallic layers separated by an insulator so that tunneling between the layers can occur as shown in Fig. 6.6 [7]. Where a metamaterial medium consisting of N metal layers embedded into an insulator is inserted between the plates of a regular capacitor. It is assumed that the electron transfer between the external plates of the capacitor (with charge $\pm q$) and internal metal layers (with charges Q_k) is negligible. Therefore, the internal charges Q_k can only be redistributed between the internal layers creating a medium polarization. The suggested memcapacitor shows the pinched hysteresis in charge–voltage and capacitance–voltage curves, and both negative and diverging capacitance within certain ranges of the field. Their proposal can be easily realized experimentally and indicates the possibility of information storage in memcapacitive devices. The authors derived an expression for the capacitance of the whole structure which is given as

$$C = \frac{q}{V_c} = \frac{2C_o}{2 + \sum_{i=1}^{N} [\Delta - 2\Delta_{i-1}] \frac{Q_i}{q}}, \tag{6.14}$$

where $\Delta = \delta/d, \Delta_i = \sum_{j=1}^{i} \delta_j/d$ for $i = 1, 2, \ldots, N-1, \Delta_o = 0$ and $C_o = \varepsilon_o \varepsilon_r S/d$ is the capacitance without internal metal layers. As obvious from the previous equation, the memcapacitance is a function of the charge q.

Martinez et al. proposed a realization of a bistable nonvolatile memcapacitor in 2011 [11]. Its design utilizes a strained elastic membrane as one plate of the parallel-

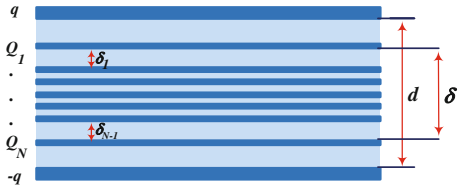

Fig. 6.6 Multilayer structure of solid-state memcapacitor [7]

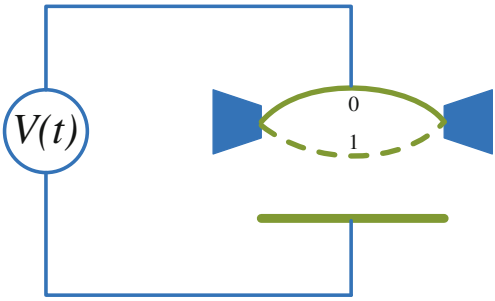

Fig. 6.7 Schematic of the bistable nonvolatile elastic membrane memcapacitor connected to the voltage source $V(t)$ [11]

plate capacitor as shown in Fig. 6.7. The top plate of a regular parallel plate capacitor is replaced by a flexible strained membrane. Because of two equilibrium positions of the membrane (represented by a double-well potential sketched on the right-hand side of the figure), stable high and low capacitance configurations are possible in such a system. A voltage pulse of an appropriate amplitude can be used to reliably switch the memcapacitor into the desired capacitance state. Moreover, charge–voltage and capacitance–voltage curves of such a system demonstrate hysteresis.

Moreover, there have been other realizations for the memcapacitive devices observed in nanopores [8], certain diode structures [12], and ferroelectric materials such as $Pb(Zr_{1x}Ti_x)O_3$ or $BaTiO_3$. The ferroelectric capacitor has a structure of a metal–insulator–metal (MIM) capacitor, in which the insulating layer is formed by ferroelectric material [13].

6.1.4 First-Order Memcapacitor Model

The nonlinear mathematical model of the memcapacitor is very important since it describes the real behavior of the memcapacitor near to the boundary which affects the response of the memcapacitor. The first nonlinear model of mem-element systems was proposed by Joglekar [14] which represents a symmetric window function and gives single-valued characteristics under any excitation source. The Joglekar's window function decreases as the boundary approaches until it reaches the boundary where it tends to zero as shown in Fig. 6.8. The second common nonlinear model was proposed by Biolek [15] where the window function depends on a discontinuous window decreasing toward zero as the boundary layer approaches any of the two ends and sharp discontinuity transitions when the excitation source reverses its polarity. Biolek's window function may allow for multivalued characteristics under the sign-varying of the excitation source. This analysis is built depending on Joglekar's window function which is more suitable for most mem-elements due to its single-valued characteristics.

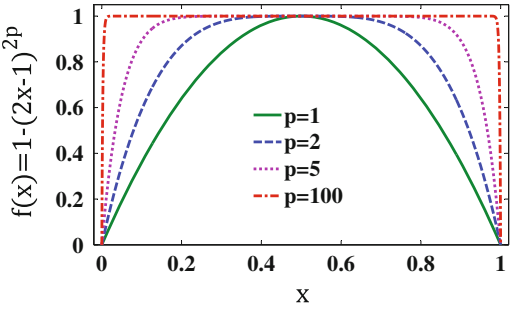

Fig. 6.8 Joglekar's window function f(x) for different p = 1, 2, 5, and 100

The charge-controlled model of the memcapacitor is introduced in [16] based on the general model of the memcapacitor [4]. The reciprocal of the capacitance D is given as

$$D(t) = D_{max} + x(t)(D_{min} - D_{max}),\ D \in (D_{max}, D_{min}), \tag{6.15}$$

where $x(t)$ represents the state variable of the memcapacitor, D_{max} and D_{min} are the reciprocal of the boundaries of the memcapacitance C_{max} and C_{min}, respectively. This definition is an analogy to the definition of HPs memristor which was presented in 2008 [14]. The state equation of the memcapacitance was defined as

$$\frac{dx}{dt} = kf(x)q(t) = kf(x)\frac{d\sigma}{dt}, \tag{6.16}$$

where $\sigma(t)$ is the time integral of the charge $q(t)$. The rate of change of the state variable is directly proportional to the mobility factor k and the window function which is modeled by Joglekar's window function [14] which is given as $f(x) = 1 - (2x - 1)^{2p}$, where p represents the doping factor of the memcapacitor which affects the rate of change in memcapacitor state variable as shown in Fig. 6.8. The pinched hysteresis relation of charge-controlled memcapacitor is given from

$$q(t) = C(t, x, q)v(t)\ or\ v(t) = D(t, x, q)q(t). \tag{6.17}$$

6.2 Mathematical Modeling of Memcapacitor

The memcapacitor is modeled using the charge passing through it as given as (6.15) and is a function of the state variable x. In order to obtain an implicit relation of memcapacitance, (6.16) is substituted in the derivative of (6.15) so

$$\frac{dD}{dt} = \eta k(D_{min} - D_{max})q(t). \tag{6.18}$$

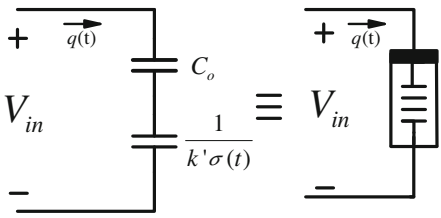

Fig. 6.9 Memcapacitor model

The rate of change of charge in the memcapacitance is proportional to the charge passing through the memcapacitor. By integrating (6.18) relative to time assuming zero initial current, if the current exists, it vanishes with time and produces an initial capacitance C_o. The memcapacitance is given as (6.19) so the circuit model of this equation is represented by two series capacitors; the first one has a capacitance C_o and the other one is $1/k'\sigma(t)$ where $\sigma(t)$ is the time integral of the charge passing through C_o as shown in Fig. 6.9.

$$D = D_{in} + \eta k'\sigma(t), \tag{6.19}$$

where $k' = k(D_{min} - D_{max})$, D_{in} represents the inverse of the initial memcapacitance, and $\frac{D_{max}-D_o}{k'} < \sigma(t) < \frac{D_{min}-D_o}{k'}$. The main parameters that affect the memcapacitances are C_o and k'. The input voltage can be written as follows:

$$v(t) = D(t)q(t) = \left(D_{in} + \eta k'\sigma(t)\right)\frac{d\sigma}{dt}. \tag{6.20}$$

By integrating both sides relative to time assuming zero initial condition, the input time integral of charge is given as

$$\sigma(t) = \frac{-D_{in} + \sqrt{D_{in}^2 + 2\eta k'\varphi(t)}}{\eta k'}, \tag{6.21}$$

where $\varphi(t)$ is the flux (time integral of the voltage). The input charge is given as

$$q(t) = \frac{v(t)}{\sqrt{D_{in}^2 + 2\eta k'\varphi(t)}}. \tag{6.22}$$

Hence, the memcapacitance is equal to

$$D^2(t) = D_{in}^2 + 2\eta k'\varphi(t). \tag{6.23}$$

As it is clear the change in the reciprocal of the memcapacitance square is directly proportional to the flux $\varphi(t)$. Moreover, the initial voltage on the memcapacitor leads to a change in its initial memcapacitance C_{in1} into C_{in2} so it can be assumed that

$\varphi(0) = 0$. In addition, Eqs. (6.19) and (6.23) represent two equivalent expressions for the memcapacitance so any one of them can be used to model the memcapacitor depending on which model makes the analysis easier. Also, it is worth noting that this linear model analysis can be considered a good approximation for the highly doped nonlinear model where $p > 10$.

The input current is the rate of change in the charge passing through the memcapacitor so $I(t) = \frac{dC}{dt}V_c(t) + C(t)\frac{dV_c}{dt}$. The time derivative of the memcapacitance is given as:

$$\frac{dC(t)}{dt} = -\frac{\eta k' C_o^3 v(t)}{(1 + 2\eta C_o^2 k' \varphi(t))^{3/2}} = -\eta k' C^3(t) v(t) \tag{6.24}$$

Hence, the current passing through memcapacitor is

$$i(t) = \frac{d(C(t)v(t))}{dt} = C(t)\frac{dv(t)}{dt} - \eta k' C^3(t)v^2(t) = C(t)\Big(\frac{dv(t)}{dt} - \eta k' C^2(t)v^2(t)\Big) \tag{6.25}$$

Thus, the stored energy is given as

$$U_c(t) = \int_{t_o}^{t} C(\tau)\Big(v(\tau)\frac{dv(\tau)}{dt} - \eta k' C^2(\tau)v^3(\tau)\Big)d\tau. \tag{6.26}$$

6.3 Boundary Dynamics of Memcapacitor

In this section; solution of nonlinear models is derived using the memcapacitance which is given as (6.15) [17]. The modeling equations of the memcapacitor can be represented as a space state representation which describes the memcapacitor behavior and are given from (6.16) and (6.17) as follows:

$$\begin{pmatrix} \frac{d\sigma}{dt} \\ \frac{dx}{dt} \end{pmatrix} = \frac{1}{D(t)} \begin{pmatrix} 1 & 0 \\ kf(x) & -D(t) \end{pmatrix} \begin{pmatrix} v(t) \\ 0 \end{pmatrix} \tag{6.27}$$

The rate of change of the memcapacitance state variable $x(t)$ is given as

$$\frac{dx}{dt} = \frac{kf(x)}{D(t)}v(t), \tag{6.28}$$

by integrating both sides relative to time where the state variable changes from x_{in} to $x(t)$

$$\int_{xin}^{x} \frac{D_{max} + xD_d}{f(x)}dx = \int_{0}^{t} kv(t)dt, \tag{6.29}$$

where $x(t) = (D(t) - D_{max})/D_d$, $x_{in} = (D_{in} - D_{max})/D_d$, $D_d = D_{min} - D_{max}$ and $D_s = D_{min} + D_{max}$.

The nonlinear dopant model of memcapacitor is $f(x) = 1 - (2x - 1)^{2p}$ and by substituting by $f(x)$ into (6.29) and by letting $y = 1 - 2x$ so $dx = -dy/2$, the integral equation (6.29) can be written as follows:

$$\int_{y_{in}}^{y} \frac{D_s - yD_d}{1 - y^{2p}} dy = \int_{0}^{t} -4kv\,(t)\,dt, \tag{6.30}$$

where y and y_{in} are given as $(D_s - 2D\,(t))\,/D_d$ and $(D_s - 2D_{in})\,/D_d$, respectively. The time integral of the right-hand side equals $-4k\varphi\,(t)$ but the left-hand side part is divided into two integrations and are given as follows:

$$I_1 = \int \frac{1}{1 - y^{2p}} dy = \sum_{r=0}^{\infty} \frac{y^{2pr+1}}{2pr + 1} + c, \tag{6.31a}$$

$$I_2 = \int \frac{y}{1 - y^{2p}} dy = \sum_{r=0}^{\infty} \frac{y^{2pr+2}}{2pr + 2} + c. \tag{6.31b}$$

From (6.30) and (6.31), the left-hand side L.H.S. is $D_s\ I_1|_{y_{in}}^{y} - D_d\ I_2|_{yin}^{y}$ so let $h(D(t),\, p) = D_s\ I_1 - D_d\ I_2$ hence L.H.S. $= h(D(t),\, p) - h(D_{in},\, p)$. By substituting by (6.30) into L.H.S. we get:

$$h(D(t),\, p) = \sum_{r=0}^{\infty} y^{2pr+1} \left(\frac{(2pr + 2)D_s - (2pr + 1)D_d\ y}{(2pr + 1)(2pr + 2)} \right),$$

$$= \sum_{r=0}^{\infty} \left(\frac{D_s - 2D(t)}{D_d} \right)^{2pr+1} \left(\frac{D_s + 2(2pr + 1)D(t)}{(2pr + 1)(2pr + 2)} \right). \tag{6.32}$$

The implicit relation of the memcapacitance for any dopant drift window function having any arbitrary p is given as follows:

$$\sum_{r=0}^{\infty} \left(\frac{2D\,(t) - D_s}{D_d} \right)^{2pr+1} \left(\frac{D_s + 2\,(2pr + 1)\,D\,(t)}{(2pr + 1)\,(2pr + 2)} \right) =$$

$$\sum_{r=0}^{\infty} \left(\frac{2D_{in} - D_s}{D_d} \right)^{2pr+1} \left(\frac{D_s + 2\,(2pr + 1)\,D_{in}}{(2pr + 1)\,(2pr + 2)} \right) + 4k\varphi\,(t) \tag{6.33}$$

This relation can be used for dopant drift model even when p tends to infinity where (6.33) will be deduced to (6.23) by taking limits when p tends to infinity. Although it is not easy to get a closed form expression for each p but in case of the minimum

window function $p = 1$, it easy to prove that the memcapacitance can be given as follows:

$$\left(\frac{C(t)}{C_{in}}\right)^{D_d}\left(\frac{C_{max}-C(t)}{C_{max}-C_{in}}\right)^{D_{max}}\left(\frac{C_{in}-C_{min}}{C(t)-C_{min}}\right)^{D_{min}} = e^{4k\varphi(t)} \tag{6.34}$$

Equation (6.33) gives a closed form solution for instantaneous memcapacitance for any voltage excitations but in order to use this closed form, it is needed to prove that this function is a bijective function (one-to-one function); by differentiating flux $\varphi(t)$ relative to $D(t)$ and checking that this function is a monotonic function across the working region (D_{max}, D_{min}) which means that it does not change its derivative sign across this region as is previously discussed in [18].

Figure 6.10a shows the change of memcapacitance due to change in flux for different doping factors p = 1, 2, 5, and 100 where C_{in}, C_{min}, C_{max}, and k are equal to 1 μF, 10 nF, 10 μF and 10 $MC^{-1}s^{-1}$, respectively. Moreover, Fig. 6.10b shows the relative error in memcapacitance in reference to the memcapacitance of the linear model which is defined as $\left(C_p - C_\infty\right)/C_\infty$. As obvious for $p > 10$; the behavior of higher value p is similar to the linear model $p = \infty$.

In the following section, the memcapacitor response with its closed form expressions will be derived for different input voltage signals: DC, sinusoidal, and periodic signals which will be analyzed for linear and nonlinear dopant drift models [17, 19].

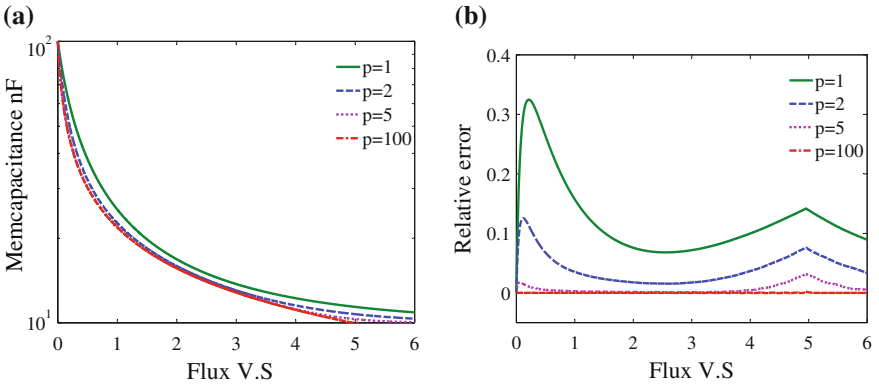

Fig. 6.10 **a** Memcapacitance–flux characteristics, and **b** relative error in capacitance–flux for different p of Joglekar's window for $\{k, C_{min}, C_{max}, C_{in}\} = 10\,M, 10\,nF, 10\,\mu F, 100\,nF$

6.4 Memcapacitor Response Under Voltage Excitations

6.4.1 Step Response

Step response is important to characterize any system where step voltage $v(t) = v_{DC}u(t)$, where $u(t)$ is a unit step function, and v_{DC} is the amplitude which may be positive or negative. To obtain an expression for the memcapacitance, the flux $\varphi(t)$ should be calculated which is the time integration of the excitation voltage. In this case the flux of step input is equal to $V_{DC}t$ so the memcapacitance for the linear case is given as

$$C(t) = \frac{C_{in}}{\sqrt{1 + 2C_{in}^2 k' V_{DC} t}}, \; C(t) \in (C_{min}, C_{max}). \tag{6.35}$$

The current and the instantaneous power can be calculated by:

$$i_c(t) = i_{c1}(t) + i_{c2}(t) = C_o v_{DC}\delta(t) + v_{DC}\frac{dC(t)}{dt} \tag{6.36a}$$

$$P_c(t) = P_{c1}(t) + P_{c2}(t) = C_o v_{DC}^2 u(t)\frac{du(t)}{dt} + v_{DC}^2\frac{dC(t)}{dt} \tag{6.36b}$$

Hence, the stored energy is given as

$$U_c(t) = U_{c1}(t) + U_{c2}(t) = \int_{t_o}^{t} P_{c1}(\tau)d\tau + \int_{t_o}^{t} P_{c2}(\tau)d\tau, \tag{6.37a}$$

$$U_{c1}(t) = \frac{1}{2}C_o(v_{DC}^2 - v_o^2), \tag{6.37b}$$

$$U_{c2}(t) = \int_{t_o}^{t} v_{DC}^2\frac{dC(t)}{dt}dt = v_{DC}^2(C(t) - C_o), \tag{6.37c}$$

$$U_c(t) = \frac{1}{2}(2C(t) - C_o)v_{DC}^2 - \frac{1}{2}C_o v_o^2. \tag{6.37d}$$

where v_o is the initial voltage on the memcapacitor. The terms $P_{c1}(t)$ and $U_{c1}(t)$ are the instantaneous power and energy due to the voltage rate of change which is identical to the conventional capacitor, however, the terms $P_{c2}(t)$ and $U_{c2}(t)$ are the instantaneous power and energy due to the memcapacitance rate of change which does not exist in the conventional capacitor. Under zero initial condition $v_o = 0$, the total energy will be positive (charging phase) and negative (discharging phase) when $C(t) > 0.5C_o$ and $C(t) < 0.5C_o$, respectively. The stored energy in the memcapacitor increases or decreases until the memcapacitor reaches one of its boundaries where there is a zero rate of change in the memcapacitor and the energy saturates. Also as obvious, the stored energy has the same profile of the memcapacitance $C(t)$,

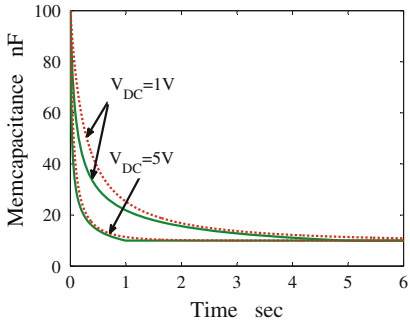

Fig. 6.11 Transient memcapacitance for different positive applied voltage at doping factor $p = 1$ (*dotted line*) and $p = \infty$ (*solid line*) for $\{k, C_{min}, C_{max}, C_{in}\} = \{10\,\text{Meg}, 10\,\text{nF}, 10\,\text{F}, 100\,\text{nF}\}$

but with gain equals v_{DC}^2. The maximum and minimum stored energy are given as $(C_{max} - 0.5C_{min})v_{DC}^2$ and $(C_{min} - 0.5C_{max})v_{DC}^2$, respectively.

But for the nonlinear case the memcapacitance is given as follows:

$$\left(\frac{C(t)}{C_{in}}\right)^{D_d}\left(\frac{C_{max} - C(t)}{C_{max} - C_{in}}\right)^{D_{max}}\left(\frac{C_{in} - C_{min}}{C(t) - C_{min}}\right)^{D_{min}} = e^{4kV_{DC}t}. \tag{6.38}$$

The expression of the memcapacitance could be expanded to $C(t) = C_{in} - C_{in}^3 k' v_{DC} t$ using the binomial theory for $C_{in}^2 k' V_{DC} t < 0.5$ so when the step voltage increases the memcapacitance decreases in case V_{DC} is positive as shown in Fig. 6.11 where the initial memcapacitance is 100 nF and the rate of decrease in the memcapacitance depends on the amplitude of the applied voltage until the memcapacitance reaches its minimum C_{min}. As obvious that the rate of change in the nonlinear model is slower than the linear case so the time to reach its boundary is larger. Moreover in case of negative applied voltage, the memcapacitance increases as the absolute of the applied voltage increases until the memcapacitance reaches its maximum C_{max}.

From the previous discussion, there is a certain time duration in which the memcapacitance reaches its boundary either maximum or minimum depending on the sign of the input voltage which is called the saturation time t_{sat} which is calculated from:

$$t_{sat} = \frac{C_{in}^2 - C_{bd}^2}{2C_{in}^2 C_{bd}^2 k' V_{DC}}, \tag{6.39}$$

where C_{bd} represents the boundary memcapacitance which is either C_{max} or C_{min}. Moreover, the saturation time for nonlinear case is given as

$$t_{sat} = \frac{1}{4kV_{DC}} ln\left(\left(\frac{C_{bd}}{C_{in}}\right)^{D_d}\left(\frac{C_{max} - C_{bd}}{C_{max} - C_{in}}\right)^{D_{max}}\left(\frac{C_{in} - C_{min}}{C_{bd} - C_{min}}\right)^{D_{min}}\right), \tag{6.40}$$

The previous expression shows that the memcapacitor will reach its boundary at infinity since it would not cling to its boundary. The maximum saturation time for the

linear model is reached when the memcapacitor changes its state from the minimum to maximum values or vice versa. Therefore, this maximum saturation time is given as:

$$t_{sat}|_{max_{p=\infty}} = \frac{C_{max} + C_{min}}{2C_{max}C_{min}k|V_{DC}|}, \tag{6.41}$$

which is a function of the applied voltage and the mobility factor k. But for the nonlinear model $p = 1$, the maximum saturation time is infinite so a new definition for maximum saturation time was defined [17, 19] where it can be assumed that the memcapacitor is saturated if the state variable reaches x_{on} or x_{off} which correspond to $D_{sat_{min}}$ and $D_{sat_{max}}$ respectively and are given as follows:

$$D_{sat_{min}} = D_{max}\,(1 - x_{on}) + x_{on}D_{min}, \tag{6.42a}$$

$$D_{sat_{max}} = D_{max}\,\left(1 - x_{off}\right) + x_{off}D_{min}. \tag{6.42b}$$

So to reach the maximum saturation time from $D_{sat_{min}}$ to $D_{sat_{max}}$ or vice versa is defined by substituting in (6.40) as follows:

$$t_{sat}|_{\substack{max \\ p=1}} = \frac{1}{4k\,|V_{DC}|} ln\left(\left(\frac{x_{off}}{x_{on}}\right)^{D_{max}}\left(\frac{1 - x_{on}}{1 - x_{off}}\right)^{D_{min}}\right). \tag{6.43}$$

But Joglekar's window function $f\,(x) = 1 - (2x - 1)^{2p}$ is symmetric so $x_{off} = 1 - x_{on}$, as a result the previous equation becomes:

$$t_{sat}|_{\substack{max \\ p=1}} = \frac{C_{max} + C_{min}}{4C_{max}C_{min}k\,|V_{DC}|} ln\left(\frac{x_{off}}{x_{on}}\right), \tag{6.44}$$

which is similar to the linear model relation but is larger by a scaling factor $\alpha = \frac{1}{2} ln\left(\frac{x_{off}}{x_{on}}\right)$. The maximum saturation time depends on the capacitance boundaries and the applied voltage where it is linearly inversely proportional to the applied voltage. Figure 6.12a shows the maximum saturation time for linear and nonlinear models where case I shows the saturation time when x_{on} and x_{off} are 0.1 and 0.9, respectively, where $\alpha = 1.0986$ which is approximately equal to the linear case, moreover case II shows the saturation time when x_{on} and x_{off} are 0.01 and 0.99, respectively, where $\alpha = 2.2976$. As obvious from Fig. 6.12b α is a decreasing function relative to x_{on} where it reaches zero when $x_{on} = x_{off} = 0.5$ and tends to ∞ when x_{on} tends to zero which matches Eq. (6.40).

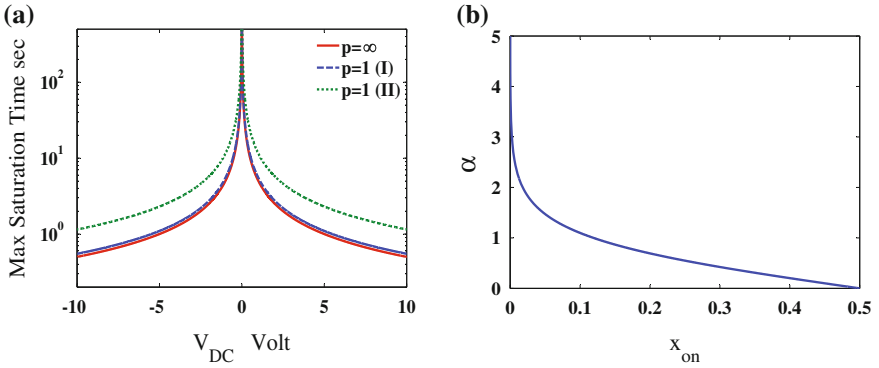

Fig. 6.12 Maximum saturation time versus voltage amplitude for $\{k, C_{min}, C_{max}\} = \{10\,\text{Meg}, 10\,\text{nF}, 10\,\text{uF}\}$

6.4.2 Sinusoidal Response

One of the main important responses which should be obtained is the sinusoidal response where a single tone signal is applied to the memcapacitor. For the capacitor, the I–V curve is a circle, but in case of the memcapacitor, the I–V curve is deformed as shown in Fig. 6.13a for different frequencies due to the memory effect. Moreover, when the frequency increases, this curve becomes more circular and tends to act more like the capacitor at very high frequencies. The pinched $q - v$ hysteresis of the simulated memcapacitor is shown in Fig. 6.13b for different input frequencies using the spice model which is proposed in [20]. Also when the frequency increases, the area inside the $q - v$ hysteresis decreases and the curve becomes more linear. If the $q - v$ characteristic is pinched, this element represents a memcapacitor which is similar to the $i - v$ characteristic in the memristor [4].

Assuming a single tone voltage is applied to the memcapacitor given as $v(t) = V_o sin(\omega_0 t)$, then by substituting into (6.23), the memcapacitance of linear model can be given as

$$D^2(t) = D_{in}^2 + \frac{4k'V_o}{\omega_o} sin^2\left(\frac{\omega_o t}{2}\right) \tag{6.45}$$

The current passing through the memcapacitor is given as

$$I = \frac{C_o V_o\left(\omega_o cos(\omega_o t) - 4\eta C_o^2 k' V_o sin^4(\omega_o t/2)\right)}{\left(1 + \frac{4\eta C_o^2 k' V_o sin^2(\omega_o t/2)}{\omega_o)}\right)^{3/2}} \tag{6.46}$$

For $\omega_o \gg 4C_o^2 k' V_o$, the current relation is reduced to $I = C_o V_o \omega_o cos(\omega_o t)$. The stored energy in the memcapacitor through sinusoidal excitation is shown in

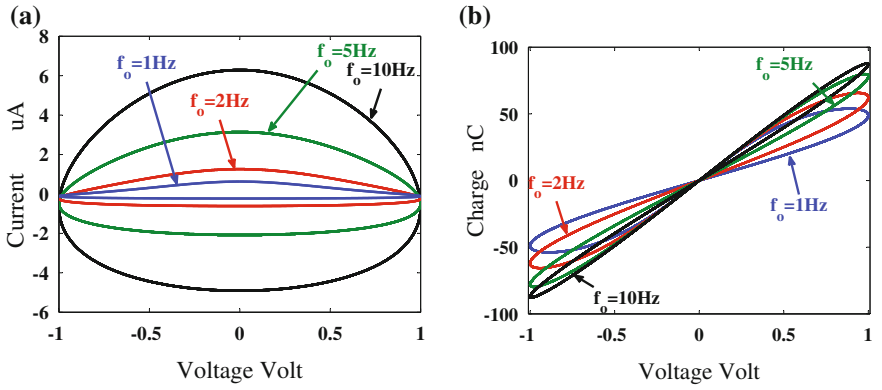

Fig. 6.13 PSPICE simulation of linear model: **a** I-V characteristics of the memcapacitor, and **b** $q - V$ hysteresis for $k, C_{min}, C_{max} = 10\,\text{Meg}, 10\,\text{nF}, 10\,\mu\text{F}$

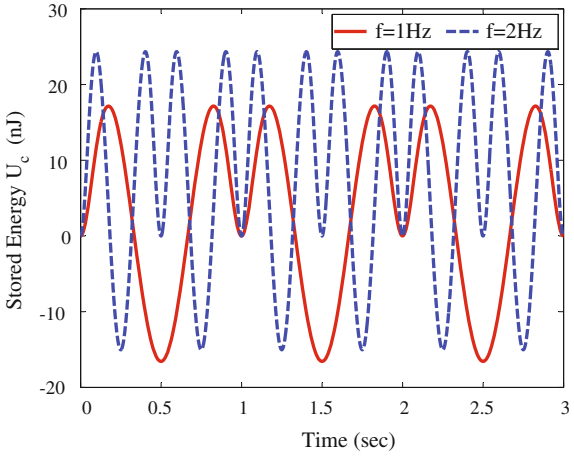

Fig. 6.14 Energy stored in memcapacitor under sinusoidal excitation

Fig. 6.14 for sinusoidal input at $V_o, \eta, k, C_{min}, C_{max}$ and C_o are equal to 1 V, 1, $10\,\text{MC}^{-1} \cdot \text{s}^{-1}$, 10 nF, 10 μF and 100 nF respectively for different frequencies. As obvious, the stored energy becomes zero after an integer number of periods which means that this memcapacitor is balanced and the average consumption power is zero.

However, in the nonlinear case, the memcapacitance is given as

$$\left(\left(\frac{C_{bd}}{C_{in}}\right)^{D_d}\left(\frac{C_{max}-C_{bd}}{C_{max}-C_{in}}\right)^{D_{max}}\left(\frac{C_{in}-C_{min}}{C_{bd}-C_{min}}\right)^{D_{min}}\right) = exp\left(\frac{8kV_o}{\omega_o}sin^2\left(\frac{\omega_o t}{2}\right)\right) \tag{6.47}$$

It is clear from (6.45) and (6.47) that the memcapacitance relation is a function of the input amplitude and the frequency where the memcapacitance decreases by increasing the frequency, moreover the area inside the hysteresis curve decreases as shown in Fig. 6.13b. The verification of the memcapacitance Eq. (6.45) compared to the spice simulation of the memcapacitor is as shown in Fig. 6.15b and Fig. 6.15a for the linear model and the nonlinear model, respectively.

When the frequency increases, the memcapacitance tends to be the initial memcapacitance C_{in}. Figure 6.16a shows the effect of changing the frequency on the transient simulation of the memcapacitance where the range of the memcapacitance decreases by increasing the frequency. Moreover, Fig. 6.16b shows the 3D surface of the pinched $q - v$ characteristic versus the frequency where the curve rotates when increasing the frequency until the effect of the memory vanishes which means that there is a linear relation between the charge and the voltage.

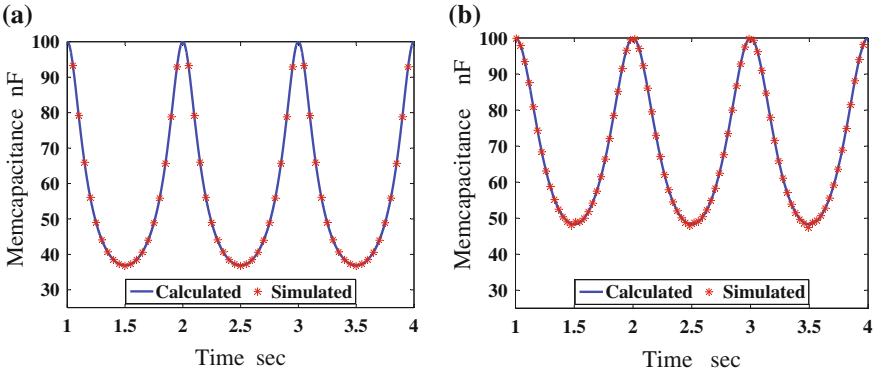

Fig. 6.15 PSPICE transient simulation of the memcapacitance: **a** $p = \infty$, and **b** $p = 1$ for $\{V_o, k, C_{min}, C_{max}, C_{in}, f_o\} = \{1\,\text{V}, 10\,\text{M}, 10\,\text{nF}, 10\,\mu\text{F}, 100\,\text{nF}, 1\,\text{Hz}\}$

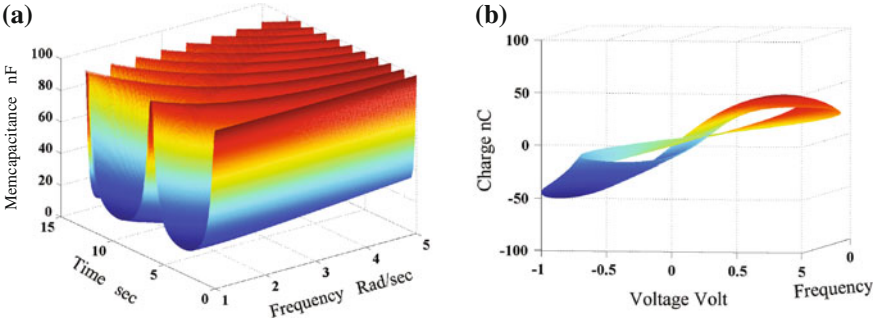

Fig. 6.16 **a** Memcapacitance for sinusoidal input voltage and **b** 3D $q - v$ pinched hysteresis of memcapacitance versus frequency

6.4.3 General Periodic Excitation Response

Any periodic signal could be expanded using Fourier series expansion as a composite of the summation of the DC signal and the sinusoidal signals

$$v(t) = a_o + \sum_{n=1}^{\infty} a_n \cos(n\omega_o t) + b_n \sin(n\omega_o t), \tag{6.48}$$

where a_o represents the DC component in the applied signal and a_n and b_n represent the amplitudes of cosine and sine terms of the nth harmonic component of the signal. By substituting by (6.48) into (6.23), the instantaneous memcapacitance for linear model is given as

$$D^2(t) = D_{in}^2 + 2k' \left(a_o t + \sum_{n=1}^{\infty} \frac{1}{n\omega_o} \left(a_n \sin(n\omega_o t) - b_n (\cos(n\omega_o t) - 1) \right) \right). \tag{6.49}$$

A similar expression can be obtained for nonlinear model by substituting by (6.48) into (6.34) which describes the nonlinear behavior of the applied periodic signals.

Any periodic signals having a DC component ($a_o \neq 0$) lead the memcapacitor to saturate, since the average of (6.49) increases or decreases with time depending on the sign of a_o, thus a condition on the periodic signal for zero, net DC component should be obtained which comes from $a_o = 0$. But in case of nonzero a_o, the memcapacitor reaches one of its boundaries after the time given in (6.23) where $V_{DC} = a_o$.

6.4.3.1 Square Wave Signal Response

As an example of periodic signal; the memcapacitor is biased by a square wave signal which is defined by

$$v(t) = \begin{cases} V_{o1} & 0 < \tau < \alpha T \\ V_{o2} & \alpha T < \tau < T \end{cases}, 0 < \alpha < 1, \tau = mod(t) \tag{6.50}$$

The applied signal alternates with sharp transitions between two different voltages that can be: (a) both are positive; (b) both are negative; or (c) one is positive and the other is negative. Therefore, the previous step response can be used periodically using the last value as the initial value of the next step. So the memcapacitance changes up and down as the voltage changes periodically. By applying Fourier series expansion to the input signal, the coefficients are given as $a_o = \alpha V_{o1} + (1 - \alpha) V_{o2}$, $a_n = \frac{(V_{o1} - V_{o2})}{n\pi} \sin(2\alpha n\pi)$ and $b_n = \frac{(V_{o1} - V_{o2})}{n\pi} (1 - \cos(2\alpha n\pi))$.

As obvious from (6.49), there is a DC term (a_o) which leads to saturation so the square wave signal has two cases:

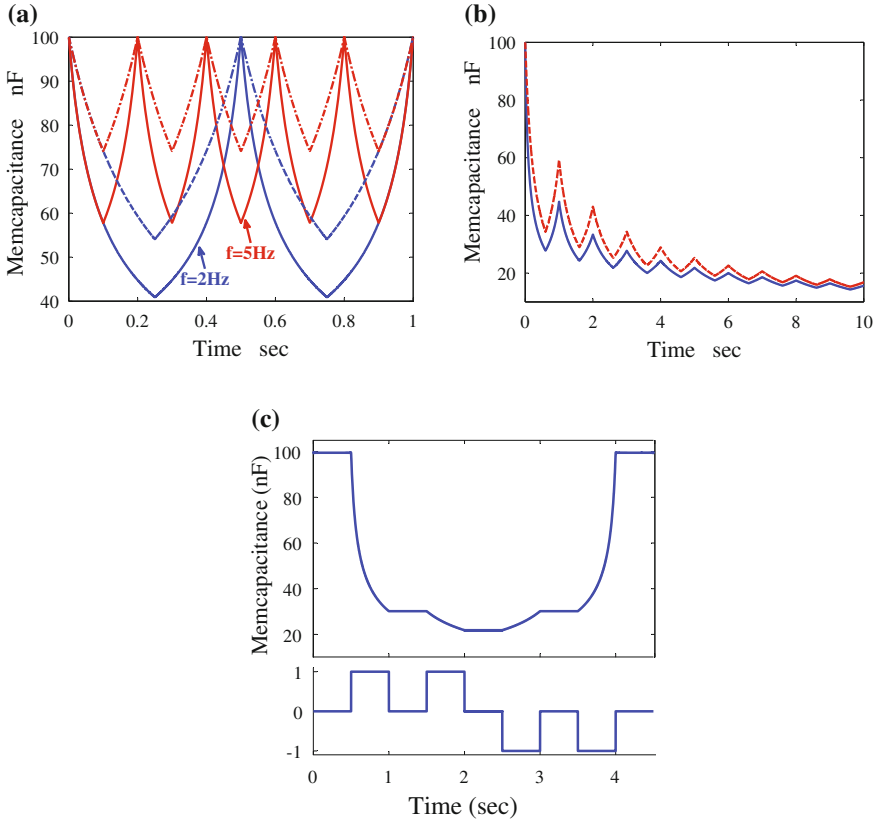

Fig. 6.17 Transient capacitance for square wave signal input at $p = 1$ (*dotted line*) and $p = \infty$ (*solid line*) **a** without DC component, **b** with DC component = 0.2 V, and **c** two successive positive and negative pulses

1. Zero DC component: which means that the accumulated voltage (i.e., net flux = 0) after N periods is zero so $\frac{V_{o1}}{V_{o2}} = \frac{\alpha-1}{\alpha}$ should be satisfied then the instantaneous memcapacitance will be a function of the summation of some sinusoidal waveforms as shown in (6.49). Figure 6.17a shows the instantaneous memcapacitance under square wave input with V_{o1}, V_{o2}, and α equal 1, −1, and 0.5 V, respectively, since the memcapacitance increases and decreases depending on the sign of the applied voltage with nonlinear curves where the change in the square of inverse memcapacitance is directly proportional to the instantaneous net voltage which is a function of V_{o1} and V_{o2}. Moreover, the range of the memcapacitance decreases by increasing the input frequency.
   The instantaneous memcapacitance expression could be written by using the behavior of the square signal which is given during any period by

$$\frac{1}{C^2(t)} = \begin{cases} \frac{1}{C_o^2} + 2\eta k' V_{o1}\tau & 0 < \tau < \alpha T \\ \frac{1}{C_o^2} + 2\eta k' \left(\alpha T \left(V_{o1} - V_{o2}\right) + V_{o2}\tau\right) & \alpha T < \tau < T \end{cases} \tag{6.51}$$

2. Non Zero DC component: where the accumulated voltage leads the memcapacitor to saturate. Figure 6.17b shows that the instantaneous memcapacitance decreases with time due to the DC component in the input signal where V_{o1}, V_{o2} and α equal 1, −1 and 0.7 V, respectively. The memcapacitance reaches saturation after a number of periods given as:

$$n_{sat} = \frac{C_{min} + C_{max}}{2kC_{min}C_{max}\, a_o T} \tag{6.52}$$

In case of applying successive positive and negative pulses, the memcapacitance decreases/increases depending on the sign of the DC component. For instance, Fig. 6.17c shows two positive successive pulses followed by two positive successive pulses where the memcapacitance decreases starting from 100 nF for positive pulses and increases for negative pulses till it reaches its ordinal value 100 nF.

Similarly, this analysis can be done for any periodic signals that can be expanded using Fourier series by substituting in the general expression of the instantaneous memcapacitance in (6.49).

6.5 Detailed Analysis of Two Series Memcapacitors

6.5.1 Mathematical Analysis

The memcapacitor is modeled by a first-order differential equation where the rate of change in each memcapacitor is given as:

$$\frac{1}{C_a^2}\frac{dC_a}{dt} = -\eta_a k'_a q_a(t), \tag{6.53a}$$

$$\frac{1}{C_b^2}\frac{dC_b}{dt} = -\eta_b k'_b q_b(t). \tag{6.53b}$$

If the charge passing through them is the same, then

$$\frac{1}{C_a^2}\frac{dC_a}{dt} = \frac{\eta_a k'_a}{\eta_b k'_b}\frac{1}{C_b^2}\frac{dC_b}{dt}, \tag{6.54}$$

Let $\alpha = \frac{(\eta_a k'_a)}{(\eta_b k'_b)}$ representing the mismatch between the two memcapacitors, by integrating both sides, the instantaneous memcapacitance C_a is given as

$$\frac{1}{C_a} = \frac{\alpha}{C_b} + \frac{1}{C_{ina}} - \frac{\alpha}{C_{inb}}, \tag{6.55}$$

where C_{ina} and C_{inb} represent the initial memcapacitance of the memcapacitors C_a and C_b, respectively. The equivalent memcapacitance of two series memcapacitors is given as

$$\frac{1}{C_{eq}} = \frac{\alpha + 1}{C_b} + \frac{1}{C_{ina}} - \frac{\alpha}{C_{inb}} \tag{6.56}$$

As shown in (6.56), the equivalent input memcapacitance can be written as a function in C_b only, thus this analysis focuses on C_b. The charge passing through the memcapacitor $q(t) = \frac{(C_a C_b)}{(C_a + C_b)} V_{in}(t)$, and V_{in} is the applied voltage thus by substituting by (6.55), $q(t) = \frac{C_b C_{ind}}{C_b + (\alpha+1) C_{ind}} V_{in}(t)$, where $\frac{1}{C_{ind}} = \frac{1}{C_{ina}} - \frac{\alpha}{C_{inb}}$. The rate of change in memcapacitor C_b is independent on C_a and is equal to:

$$\left(\frac{\alpha + 1}{C_b^3} + \frac{1}{C_b^2 C_{ind}} \right) \frac{dC_b}{dt} = -\eta_b k_b' V_{in}(t) \tag{6.57}$$

By integrating both sides relative to time, where the memcapacitance C_b changes from C_{inb} to $C_b(t)$, and the left-hand side represents a time integral of voltage which is flux $\varphi(t)$. The memcapacitance is given as:

$$\frac{\alpha + 1}{C_b^2} + \frac{2}{C_{ind}} \frac{1}{C_b} - \left(\frac{\alpha + 1}{C_{inb}^2} + \frac{2}{C_{inb} C_{ind}} + 2\eta_b k_b' \varphi(t) \right) = 0. \tag{6.58}$$

By solving this equation by quadratic formula; $\frac{1}{C_b} = (-b \pm \sqrt{b^2 - 4ac})/2a$, where $a = \alpha + 1, b = \frac{2}{C_{ind}}$, and $c = \frac{(\alpha-1)C_{ina} - 2C_{inb}}{C_{inb}^2 C_{ina}} - 2\eta_b k_b' \varphi(t)$. The instantaneous memcapacitance C_b is given as

$$\frac{1}{C_b} = \frac{-1}{\alpha + 1} \left(\frac{1}{C_{ind}} \mp \sqrt{\left(\frac{1}{C_{ina}} + \frac{1}{C_{inb}} \right)^2 + 2(\alpha + 1)\eta_b k_b' \varphi(t)} \right). \tag{6.59}$$

A similar expression can be obtained for memcapacitance C_a using (6.55) [21].

The memcapacitance C_b should be real and positive and in between the maximum and minimum achievable memcapacitances so by equating (6.59) by maximum and minimum memcapacitances, the following conditions on flux are obtained:

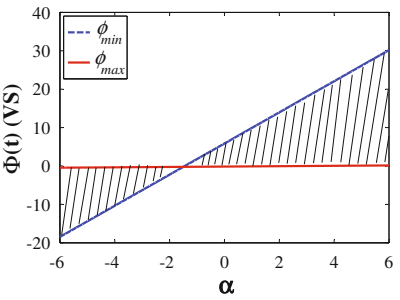

Fig. 6.18 The valid solution region of two series memcapacitors

$$\varphi_{min} = \frac{(C_{inb} - C_{bmin})(\alpha(C_{inb} - C_{bmin}) + C_{inb} + 3C_{bmin})}{2\eta_b k_b' C_{inb}^2 C_{bmin}^2}, \tag{6.60a}$$

$$\varphi_{max} = \frac{(C_{inb} - C_{bmax})(\alpha(C_{inb} - C_{bmax}) + C_{inb} + 3C_{bmax})}{2\eta_b k_b' C_{inb}^2 C_{bmax}^2}. \tag{6.60b}$$

The hashed region, in Fig. 6.18, shows the valid solution of equation (6.59) for the corresponding α and φ. As obvious there is a point of intersection where memcapacitance C_b does not change its values. This intersection point α_c is given as

$$\alpha_c = -\frac{(C_{inb}(C_{bmin} + C_{bmax}) + 2C_{bmin}C_{bmax})}{(C_{inb}(C_{bmin} + C_{bmax}) - 2C_{bmin}C_{bmax})}. \tag{6.61}$$

Figure 6.18 is plotted for the following parameters: $(C_{max}, C_{inb}, k, \eta_b) = (10\,\mu\text{F}, 10\,\text{nF}, 100\,\text{nF}, 10\,\text{M}, 1)$ and the intersection point (α_c, φ_c) equals $(-1.4994, -0.227)$.

6.5.2 Practical Cases

In general, there are four different special cases which are very important to study, shown in Fig. 6.19, where the output is the common node between the two memcapacitors.

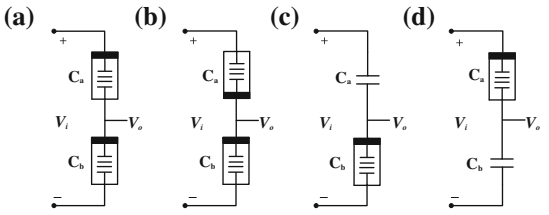

Fig. 6.19 Different configurations of memcapacitors in series connections

The memcapacitance C_b is a function of α, C_{ina}, C_{inb}, C_{ind}, and k'_b. There are four special cases based on α that can be studied as follows:

1. Both C_a and C_b are two memcapacitors with the same mobility factors ($k'_a = k'_b$) and with the same polarities so $\alpha = 1$ as shown in Fig. 6.19a. The instantaneous memcapacitance C_b is given as

$$\frac{1}{C_b} = \frac{-1}{2C_{ind}} + \sqrt{\frac{1}{4}\left(\frac{1}{C_{ina}} + \frac{1}{C_{inb}}\right)^2 + \eta_b k'_b \varphi(t)}. \tag{6.62}$$

2. Both C_a and C_b are two memcapacitors with the same mobility factors ($k'_a = k'_b$) and with different polarities so $\alpha = -1$ as shown in Fig. 6.19b. The sum of the reciprocal of the two memcapacitances is constant from (6.55). The instantaneous memcapacitance C_b is given as

$$\frac{1}{C_b} = \frac{1}{C_{inb}} + \eta_b k'_b \varphi(t) \frac{C_{ina} C_{inb}}{C_{ina} + C_{inb}}. \tag{6.63}$$

3. C_a is a capacitor and C_b is a memcapacitor, so by putting $k'_a = 0$, the effect of memcapacitor C_a is eliminated, so $\alpha = 0$ as shown in Fig. 6.19c. The instantaneous memcapacitance C_b is given as

$$\frac{1}{C_b} = \frac{-1}{C_{ina}} + \sqrt{\left(\frac{1}{C_{ina}} + \frac{1}{C_{inb}}\right)^2 + 2\eta_b k'_b \varphi(t)}. \tag{6.64}$$

4. The last case when C_b is a capacitor and C_a is a memcapacitor thus $k'_b = 0$ and $\alpha = \infty$ as shown in Fig. 6.19d. The instantaneous memcapacitance C_a is given as

$$\frac{1}{C_a} = \frac{-1}{C_{inb}} + \sqrt{\left(\frac{1}{C_{ina}} + \frac{1}{C_{inb}}\right)^2 + 2\eta_a k'_a \varphi(t)}. \tag{6.65}$$

6.5.3 Circuit Simulation and Validation

Due to the lack of memcapacitor samples which are not commonly available for experimental realization, the SPICE model of memcapacitor proposed by Z. Biolek et al. [16] is used with the following parameters: (C_{max}, C_{min}, C_{ina}, C_{inb}, K, p) = (10 μF, 10 nF, 100 nF, 150 nF, 10 M, 100) respectively and applying a sinusoidal voltage source with amplitude of 1 V and frequency of 1 Hz.

As discussed in the previous subsection, four cases exist, in the case of $\alpha = 1$, where the two memcapacitors have the same mobility and same polarities; the instantaneous expression of the memcapacitance as a function of the flux is given as (6.62)

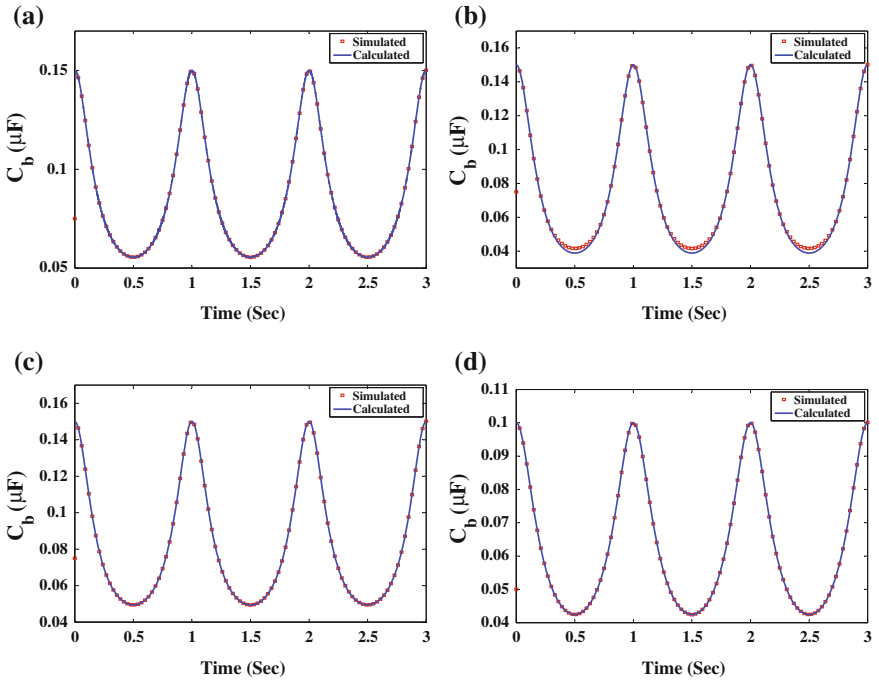

Fig. 6.20 Instantaneous memcapacitance for series case : **a** $\alpha = 1$, **b** $\alpha = -1$, **c** $\alpha = 0$, and **d** $\alpha = \infty$

which matches the PSPICE simulation as obvious from Fig. 6.20a where the maximum and minimum capacitances of C_b are 150 and 55.5 nF, respectively, which matches numerical simulation in (6.60) for the same parameters.

In the case of $\alpha = -1$ where the two memcapacitors have opposite polarities and the same mobility factor; the memcapacitance is given as (6.63) which matches the numerical simulation as shown in Fig. 6.20b, where the maximum and the minimum capacitances of C_b are 150 and 41.15 nF, respectively, with maximum relative error with calculated expression from (6.63) is equal to 5.94 % due to the effect of the dopant ratio, as the linear doping case p is infinite where the sum of the reciprocal of the two capacitances is constant.

In the case of $\alpha = 0$, the capacitance of C_b is given as (6.64) which matches the PSPICE simulation as shown in Fig. 6.20c where the maximum and minimum memcapacitance of C_b are equal to 150 and 49.44 nF, respectively.

Finally, the last case: $\alpha = \infty$, where C_b is a capacitor with constant memcapacitance equal to 150 nF, and C_a is a memcapacitor and its capacitance is given as (6.65) which matches PSPICE simulation results where the maximum and minimum capacitances are equal to 100 and 42.44 nF, respectively.

6.6 Detailed Analysis of Two Parallel Memcapacitors

6.6.1 Mathematical Analysis

As we discussed the series connections of two memcapacitors connected in parallel is discussed as shown in Fig. 6.21, where the voltage across the memcapacitors is the same so the input memcapacitance for each one could be given as in (6.23).

$$\frac{1}{C^2(t)} = \frac{1}{C_{in}^2} + 2\eta k'\varphi(t). \tag{6.66}$$

Due to the parallel connection the input charge is the sum of input charge to each branch so the input charges is given as:

$$q_{in}(t) = v(t)\left(\frac{1}{\sqrt{\frac{1}{C_{ina}^2} + 2\eta_a k'_a \varphi(t)}} + \frac{1}{\sqrt{\frac{1}{C_{inb}^2} + 2\eta_b k'_b \varphi(t)}}\right). \tag{6.67}$$

Thus the equivalent input memcapacitance is given as

$$C_{eq}(t) = \sum_{j=1}^{2} \frac{C_{inj}}{\sqrt{1 + 2C_{inj}^2 \eta_j k'_j \varphi(t)}}. \tag{6.68}$$

As discussed before, there are four special cases as shown in Fig. 6.21 where Fig. 6.21a represents the case of $\alpha = 1$ and $\eta_a = \eta_b = 1$, Fig. 6.21b represents the case $\alpha = -1$ and $\eta_a = -\eta_b = 1$, Fig. 6.21c represent the case $\alpha = 0$ and $\eta_b = 1$ and finally, Fig. 6.21d represents $\alpha = \infty$ and $\eta_a = 1$.

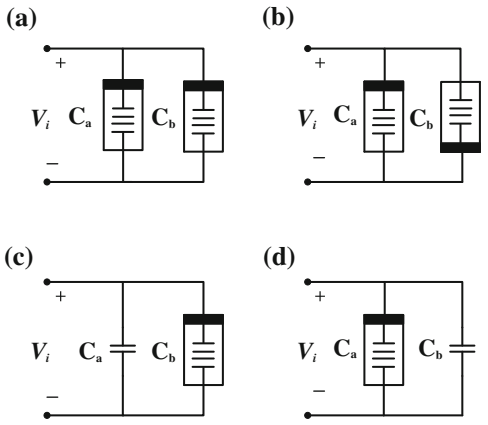

Fig. 6.21 Different configurations of memcapacitors in parallel connections: **a** $\alpha = 1$, **b** $\alpha = -1$, **c** $\alpha = 0$, and **d** $\alpha = \infty$

6.6.2 Circuit Simulation and Validation

In parallel memcapacitors simulations, the following parameters are used: $(C_{max}, C_{min}, C_{ina}, C_{inb}, K, p) = (10\,\mu\text{F}, 10\,\text{nF}, 50\,\text{nF}, 100\,\text{nF}, 10\,\text{M}, 100)$ respectively and applying a sinusoidal voltage source with amplitude of 0.5 V and with 1 Hz frequency.

In the case of $\alpha = 1$, the instantaneous expression of the equivalent memcapacitance as a function of the flux is given as (6.68) which matches the PSPICE simulation as obvious from Fig. 6.22a where the maximum and minimum capacitances of C_b are 150 and 86 nF respectively matching numerical simulation in (6.68) for the same parameters with maximum relative error with calculated expression equals 1.2176 %. In the case of $\alpha = -1$, the equivalent memcapacitance is given as (6.68) which matches the PSPICE simulation as shown in Fig. 6.22a, where the maximum and the minimum memcapacitances of C_b are 160 and 126.5 nF, respectively, with maximum relative error equal to 0.3766 %. For the case of $\alpha = 0$, the equivalent memcapacitance which matches the PSPICE simulation as shown in Fig. 6.22c where the maximum and minimum capacitance of C_b are 150 and 98.9 nF, respectively, with maximum relative error equals 0.202 %. Moreover, the last case: $\alpha = \infty$, the equivalent memcapacitance matches the PSPICE simulation where the maximum and

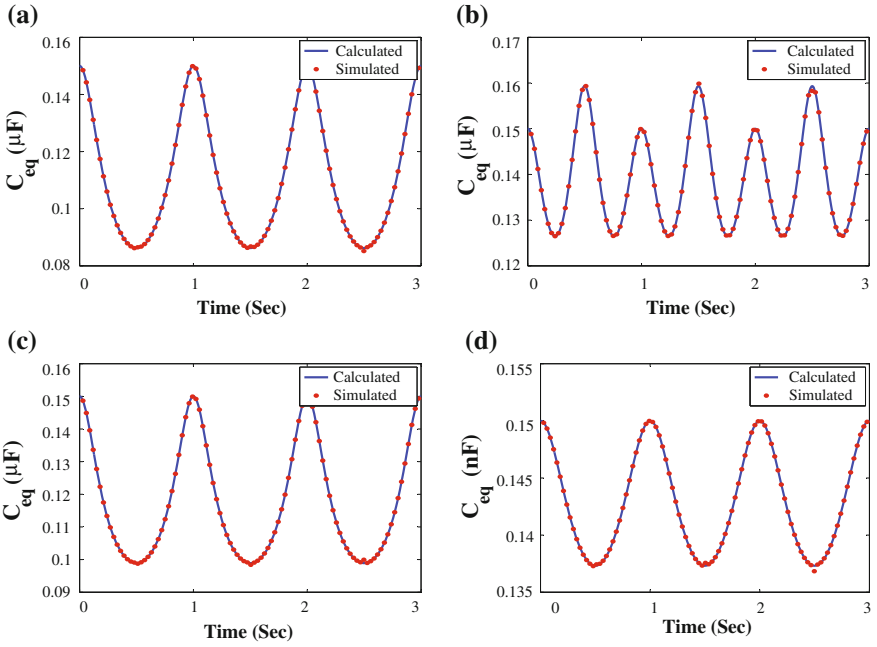

Fig. 6.22 Instantaneous memcapacitance in parallel case: **a** $\alpha = 1$, **b** $\alpha = -1$, **c** $\alpha = 0$, and **d** $\alpha = \infty$

minimum capacitances are 150 and 137.6 nF, respectively, with maximum relative error equals 0.218 %.

6.7 General Analysis of Series and Parallel Memcapacitors

In general the memcapacitors may not match so let us assume that each memcapacitor has αk where α represents the matching factor and its polarity relative to the standard memcapacitor (so α may be positive or negative). As a result, each memcapacitor can be characterized by initial memcapacitance C_o and mismatch factor α.

6.7.1 Series Memcapacitors

N series memcapacitors can be modeled using the σ-controlled memcapacitor model, see Fig. 6.9. In the series case, the charge passing through the memcapacitors is equal so they have the same time integral of charge $\sigma(t)$. The inverse of the equivalent memcapacitance is given as follows:

$$\frac{1}{C_{eq}} = \sum_{j=1}^{N} \left(\frac{1}{C_{oj}} + \alpha_j k' \sigma(t) \right) \tag{6.69}$$

Let $\frac{1}{C_{o_t}} = \sum_{j=1}^{N} \frac{1}{C_{o_j}}$ and $k'_t = k' \sum_{j=1}^{N} \alpha_j$. So $\frac{1}{C_{eq}} = \frac{1}{C_{o_t}} + k'_t \sigma(t)$. The equivalent memcapacitor has parameters (C_{o_t}, k'_t). For identical memcapacitors having the same C_o and α, the equivalent memcapacitor has $C_{o_t} = C_o/N$ and $k'_t = Nk'$.

Figure 6.23 shows perfect matching of the derived expressions with simulations for $N = 3, 5$, and 10 series identical memcapacitors under sinusoidal excitation $v(t) = sin(2\pi t)$. As obvious in Fig. 6.23, the memcapacitance starts from $C_{o_t} = C_o/N$ and behaves according to the derived formula. Furthermore, the slope of the hysteresis depends on C_{o_t} and the area inside the loops decreases by increasing N.

In case of existing opposite polarities (anti-series) in N series identical memcapacitors, where α_j is either 1 or -1, the inverse of the equivalent memcapacitance is given as:

$$\frac{1}{C_{eq}} = \sum_{j=1}^{N} \left(\frac{1}{C_{oj}} \right) + (m - n) k' \sigma(t), \tag{6.70}$$

where m and n are the number of forward- and reverse-connected memcapacitors, respectively. So, the equivalent memcapacitor has $C_{o_{eq}} = \sum_{j=1}^{N} \frac{1}{C_{o_j}}$ and $k'_t = (m - n)k'$. It is worth noting that for $m = n$, the equivalent memcapacitance is

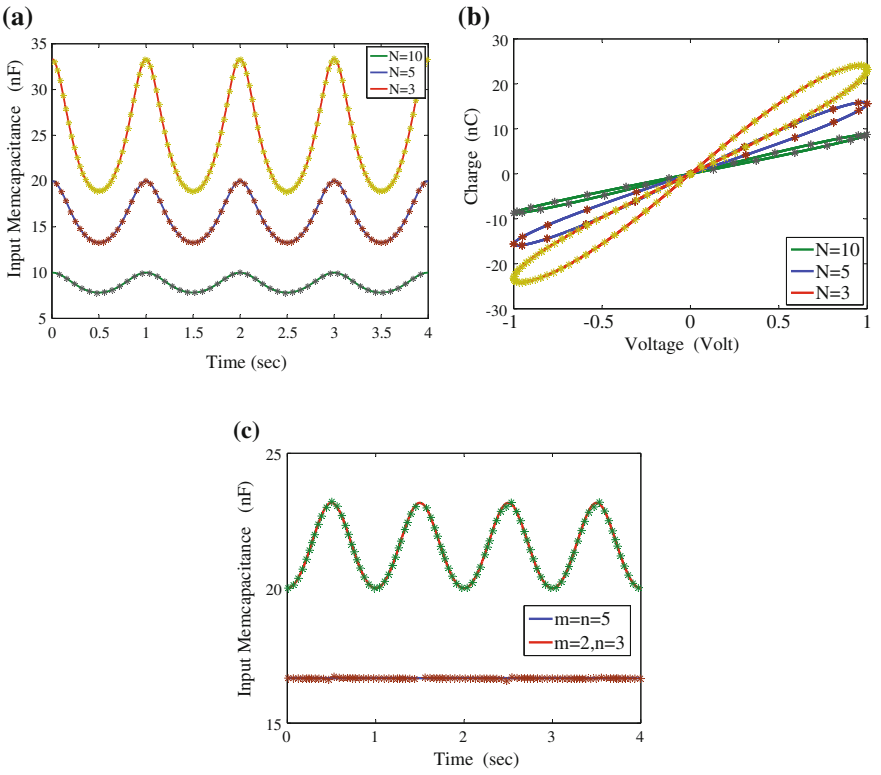

Fig. 6.23 Validation of PSPICE simulation (*stars*) and calculated expressions (*solid lines*) of series memcapacitors for **a** transient equivalent memcapacitance, **b** corresponding charge–voltage hysteresis, and **c** equivalent memcapacitance for anti-series memcapacitors for $\{k, \eta, C_{min}, C_{max}, C_o\} = \{10\,\text{MC}^{-1} \cdot \text{s}^{-1}, 1, 10\,\text{nF}, 10\,\mu\,\text{F}, \ 100\,\text{nF}\}$, respectively

constant and equals to the sum of inverse initial memcapacitances. As it is clear from Fig. 6.23c there is perfect matching between analytic expressions and the PSPICE simulations for anti-series memcapacitors where at $m = n = 3$, the equivalent memcapacitance is constant and equals $\frac{C_o}{6} = 16.7\,\text{nF}$. But in case of $m = 2$ and $n = 3$ the equivalent memcapacitor has $C_{o_{eq}} = 20\,\text{nF}$ and $k'_t = -k'$.

6.7.2 Parallel Memcapacitors

In case of N parallel memcapacitors, the voltage across the memcapacitors is equal so the flux-controlled model makes the analysis easier in this case. The input charge will be the sum of charges passing through every memcapacitor which is given as follows:

$$q(t) = \sum_{j=1}^{N} \frac{v(t)}{\sqrt{\frac{1}{C_{o_j}^2} + 2\alpha_j k' \varphi(t)}} \tag{6.71}$$

hence, the input memcapacitance is equal to

$$C_{eq}(t) = \sum_{j=1}^{N} \frac{C_{o_j}}{\sqrt{1 + 2\alpha_j k' C_{o_j}^2 \varphi(t)}} \tag{6.72}$$

For identical memcapacitors with the same initial memcapacitance C_o and polarities,

$$C_{eq}(t) = \frac{NC_o}{\sqrt{1 + 2\alpha k' C_o^2 \varphi(t)}} \tag{6.73}$$

Thus, the equivalent memcapacitor has $C_{o_t} = NC_o$ and $k'_t = k'/N^2$.

Figure 6.24 shows perfect matching of the derived expressions with spice simulation for $N = 3, 5$, and 10 parallel identical memcapacitors under sinusoidal excitation $v(t) = sin(2\pi t)$ for $\{k, C_{min}, C_{max}, C_o\} = \{10\,\text{MC}^{-1} \cdot \text{s}^{-1},\ 10\,\text{nF},\ 10\,\mu\text{F},\ 100\,\text{nF}\}$ respectively. As obvious in Fig. 6.24, the input memcapacitance starts from $C_{o_t} = NC_o$ and the hysteresis loops area increases by increasing N when the slope of the hysteresis equals C_{o_t}.

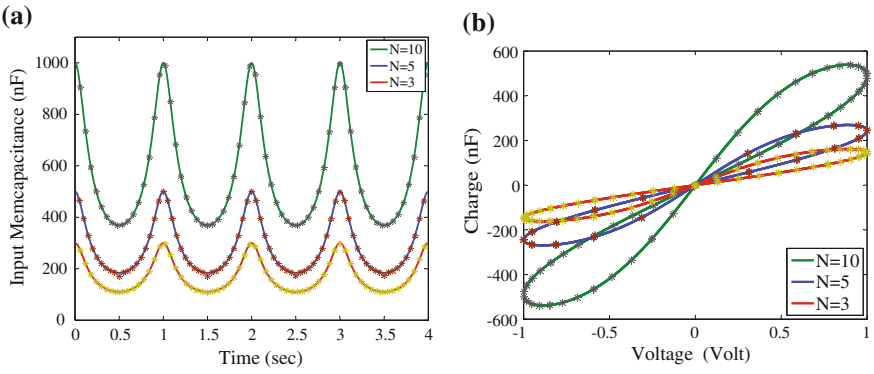

Fig. 6.24 Validation of PSPICE simulation (*stars*) and calculated expressions of parallel memcapacitors (*solid lines*) for **a** transient input memcapacitance, and **b** charge–voltage hysteresis

6.8 Charge-Controlled Memristor-Less Memcapacitor Emulator

The memcapacitor is not commercially available for experimental research, so a lot of emulators are introduced to emulate the behavior of the memcapacitor. There are two different ways to emulate the memcapacitor. The first one by transforming the memristor to memcapacitor using a $R-C$ mutator where the resistor R is replaced by the memristor to obtain memcapacitor. Thus, emulators are implemented using CCII and memristor [22–24] which is not easily available or implemented with memristor model using a light-dependent resistor (LDR) [25]. The alternative is building a memcapacitor without using any other mem-elements as proposed in this section [26].

In case of linear window function $f(x) = 1$. By integrating (6.16), the state variable is given as

$$x = x_0 + k \int_0^t q(\tau) d\tau, \tag{6.74}$$

where x_0 represents the initial state of the memcapacitor which corresponds to the initial capacitance C_0. By substituting (6.74) into (6.15), the instantaneous capacitance of the memcapacitor is given as

$$\frac{1}{C(t)} = \frac{1}{C_0} + k' \int_0^t q(\tau) d\tau, \; k' = k\left(\frac{1}{C_{min}} - \frac{1}{C_{max}}\right). \tag{6.75}$$

When applying positive voltage to the memcapacitor, the charge sign is positive then the capacitance increases so this is called incremental memcapacitor configuration and if a negative voltage is applied to the memcapacitor, the charge is negative so the capacitance decreases so this configuration is called decremental memcapacitor.

In Fig. 6.25, the $q - v$ pinched hysteresis loop of the memcapacitor shrinks and rotates decreasing the applied frequency because the capacitance is inversely proportional to the integration of charge which is a function of the frequency.

Recently, a memristor emulator was introduced which emulates the behavior of the memristor using off the shelf components to use it in memristive circuits [27]. By using a similar analogy between current and charge for the resistance and the capacitor respectively, the model is developed.

The emulator can be designed to emulate the change of capacitor by changing the applied voltage difference as shown in Fig. 6.26a. In Fig. 6.26b, the input current across the capacitor is given as

$$i_{in} = c_0 \frac{d(v_{in} - v_{FB})}{dt}. \tag{6.76}$$

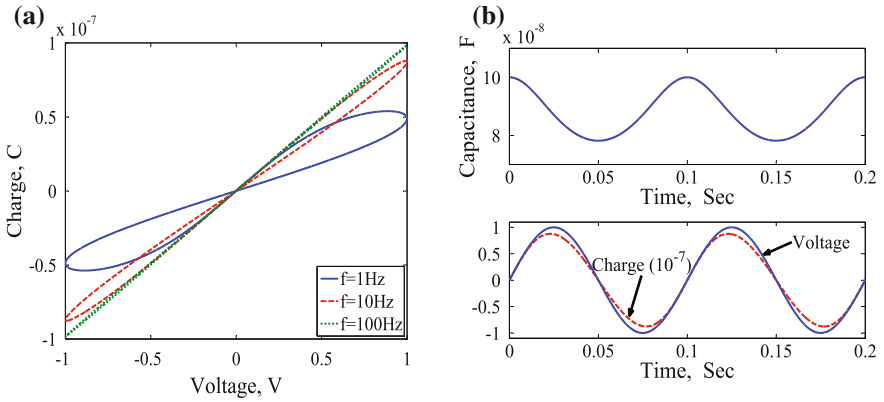

Fig. 6.25 Numerical simulation of memcapacitor for k', C_0 and V_0 are $10^{15}\,\Omega/\mathrm{C}, 100\,\mathrm{nF}$ and 1 V, respectively. **a** Charge voltage pinched hysteresis for sinusoidal input, and **b** instantaneous capacitance and charge of the memcapacitor at 10 Hz

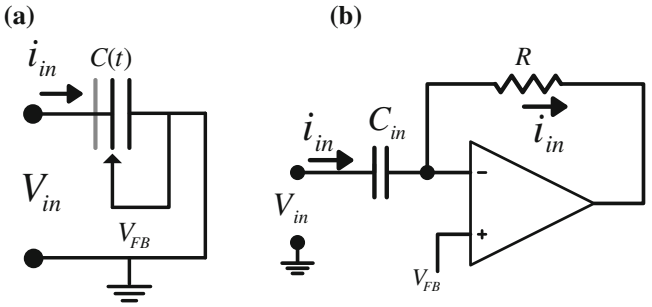

Fig. 6.26 The incremental configuration of the memcapacitor emulator **a** simplified circuit, and **b** memcapacitor symbol

This relation could be rewritten as a function of charge and by comparing it with (6.75) to get the required behavior:

$$v_{in} = \frac{q(t)}{C_{in}} + v_{FB} = \frac{q(t)}{C_0} + k'q(t)\int_0^t q(\tau)d\tau. \tag{6.77}$$

Thus we need to implement the v_{FB} term so we need a copy of the input current to be integrated and then multiplied by its integration. In Fig. 6.27, the voltage across the capacitor C_1 is the integration of the mirrored input current then this voltage is buffered to reduce the loading effect, a copy of V_{C_1} is integrated again by the active integrator then multiplied by V_{C_1} to obtain V_{FB}. Also the implementation needs an inverting buffer because of the inversion of the active integrator. The feedback voltage is given as:

$$v_{FB} = \frac{q(t)}{C_1^2}\frac{1}{RC_2}\int_0^t q(\tau)d\tau. \tag{6.78}$$

In Fig. 6.27, the incremental memcapacitor is emulated using a single multiplier, four opamps, resistors, capacitors, and a current controlled current source which could be implemented using the same circuit in [27]. Furthermore, the decremental memcapacitor could be implemented in the same way but without using the inverting buffer in the feedback as there is a required inversion from the active integrator. The previous circuit emulates the behavior of a charge-controlled memcapacitor where $k' = \frac{1}{RC_1^2C_2}$.

Figure 6.28 shows PSPICE pinched hysteresis at frequency 10 Hz which gives a great matching with the numerical simulation for the same parameters.

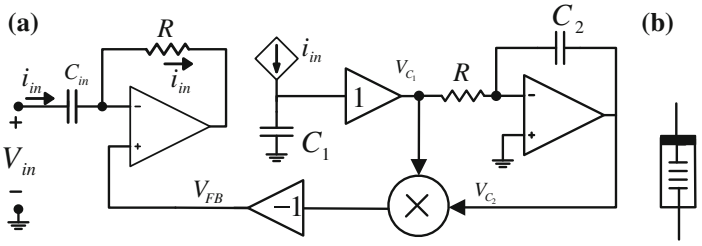

Fig. 6.27 Concept of the memcapacitor emulator. **a** Input capacitance as function of V_{FB}, and **b** emulating circuit

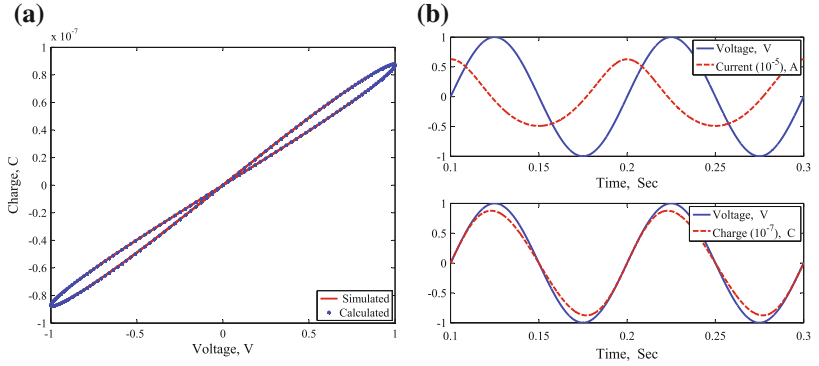

Fig. 6.28 PSPICE simulation of the memcapacitor for R, C_1, C_2, C_0, and V_0 are 1 kΩ, 1 μF, 1 μF, 100 nF, and 1 V respectively at frequency = 10 Hz. **a** Charge–voltage pinched hysteresis for sinusoidal input, and **b** instantaneous current, charge, and voltage of the simulated memcapacitor

Recently, more practical emulators have been introduced in [28, 29]. In these emulation circuits, a memristive circuit, built by analog components, is transformed into a memcapacitor emulator. In addition, these emulators are theoretically analyzed and experimentally tested.

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Chapter 7
Memcapacitor Based Applications

7.1 Introduction

There are many applications based on the mem-elements such as in the chaotic systems due to their nonlinearities. A third-order passive circuit with a voltage-controlled memcapacitor was proposed in [1] to generate chaotic oscillation. Moreover, another circuit consists of conventional R, C, L and one with charge-controlled memcapacitor to generate a chaotic oscillation was introduced in [2]. Recently, in [3] an emulation for the memcapacitor is introduced using Field-Programmable Gate Arrays (FPGAs) to realize two-element chaotic and hyperchaotic circuits.

The second application of the memcapacitor is modeling the neural networks. In [4, 5], the authors proposed a CNN cell structure implementing the basic McCulloch-Pitts neuron model, shown in Fig. 7.1a where the output (Y) is activated whenever the sum of W_i weighted input signals in_i exceeds the applied threshold Th. The cell structure is shown in Fig. 7.1b [4] where each synapse cell consists of a single memcapacitance C_M and three switches. The switch controlled by the template coefficient $AB_{i,j}$ is used to enable the given synapse to influence the cell state V_X, while the start signal initiates the processing. Switches $pr\_s_{i,j}$ are used for connecting the memcapacitor to the programming voltages V_{pr1} and V_{pr2}. Since higher amplitude pulses are usually required for programming, it is necessary to separate the memcapacitors from the rest of circuitry during the programming phase. The $AB_{i,j}$ and the start-driven switches can serve this purpose. Since the output voltage V_Y is provided by the cell output buffer (a relatively strong driver) it can be used directly for the neighborhood inputs. This enables the synapse to have either a positive $V_Y = V_{DD}$ or a negative $V_Y = 0$ contribution to the cell state.

In this chapter, two main applications are discussed. The first one is the memcapacitor-based relaxation oscillators where the expressions for sustained oscillation and oscillation frequency are introduced for linear and nonlinear models. In addition, the memcapacitor-based bridge synapses is introduced with a mathematical modeling of the bridge.

A.G. Radwan and M.E. Fouda, *On the Mathematical Modeling of Memristor, Memcapacitor, and Meminductor*, Studies in Systems, Decision and Control 26,
DOI 10.1007/978-3-319-17491-4_7

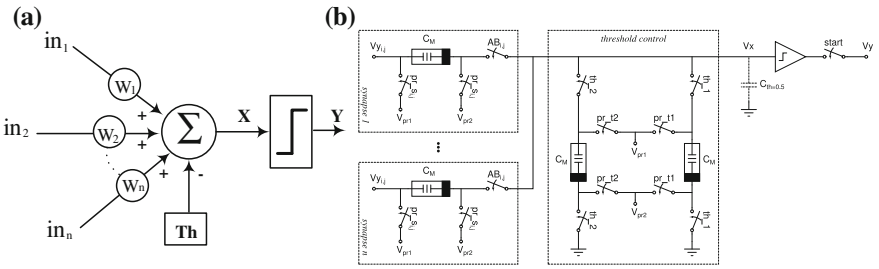

Fig. 7.1 **a** McCulloch and Pitts neuron model, and **b** memcapacitor-based cell structure [5]

7.2 Resistive-Less Memcapacitor-Based Oscillator

The memristor-based reactance-less oscillator in addition to the oscillation concept where the memristor replaces the capacitor in the relaxation oscillator was introduced in [6], but the memristor and resistor are heavily power-consuming elements which are not suitable for low-power applications such as biomedical applications and system wake-up [7, 8]. So here, the resistor and the memristor will be replaced by two memcapacitors in general as shown in Fig. 7.2a [9]. Four different cases can be extracted from this generalized circuit depending on whether each element is a capacitor or memcapacitor. The first case when two capacitors are used (where a capacitor is a special case of memcapacitor at $k = 0$), the circuit cannot oscillate since there no dynamic state may be defined where the voltage V_i is constant. The other three cases have at least one memcapacitor where nonlinear dynamics is able to change the system states.

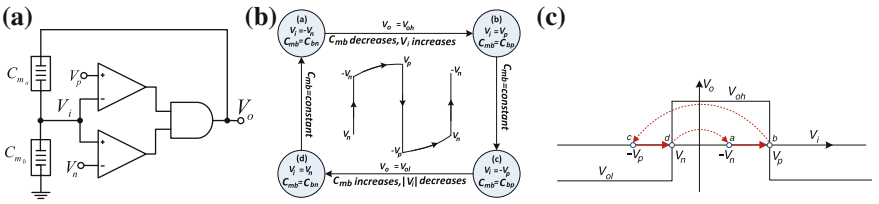

Fig. 7.2 Resistive-less memcapacitor-based relaxation oscillator **a** circuit diagram, **b** state diagram of the oscillator, and **c** transfer function of the two comparators and AND gate

7.2.1 Mathematical Analysis

The following analysis assumes two memcapacitors are used which is the general case as will be discussed later. In case of two series memcapacitors C_{ma} and C_{mb}, the rate of change in the reciprocal of memcapacitances are

$$\frac{1}{C_{m_a}^2}\frac{dC_{ma}}{dt} = -\eta_a k'_a q_a(t), \tag{7.1a}$$

$$\frac{1}{C_{m_b}^2}\frac{dC_{mb}}{dt} = -\eta_b k'_b q_b(t), \tag{7.1b}$$

where C_{ma} and C_{mb} are the memcapacitances C_a and C_b, respectively, and $k' = k(1/C_{min} - 1/C_{max})$. The charge passing through them is the same so $\frac{1}{C_{m_a}^2}\frac{dC_{ma}}{dt} = \alpha\frac{1}{C_{m_b}^2}\frac{dC_{mb}}{dt}$ where the proportionality constant α equals $(\eta_a\, k'_a)/(\eta_b\, k'_b)$ and represents the mismatch between the two memcapacitors. By integrating both sides, the instantaneous memcapacitance C_{ma} is given by:

$$\frac{1}{C_{ma}} = \frac{\alpha}{C_{mb}} + \frac{1}{C_{ind}}, \tag{7.2}$$

where $1/C_{ind} = 1/C_{ina} - \alpha/C_{inb}$, C_{ina}, and C_{inb} represent the initial memcapacitance of the memcapacitors C_a and C_b, respectively. The charge passing through the memcapacitors is the same $q_a(t) = q_b(t)$ so $C_{ma}(V_o - V_{in}) = C_{mb}V_{in}$ and substituting by (7.2), the input voltage to the comparators can be calculated as follows:

$$V_i = V_o\frac{C_{ind}}{(\alpha+1)\,C_{ind} + C_{mb}}. \tag{7.3}$$

At the critical values where $V_i = V_p$ or V_n, the memcapacitance of C_{mb} is given by C_{bp} or C_{bn}, respectively, where

$$C_{bp} = C_{ind}\left(\frac{V_{oh} - (\alpha+1)\,V_p}{V_p}\right), \tag{7.4a}$$

$$C_{bn} = C_{ind}\left(\frac{V_{ol} - (\alpha+1)\,V_n}{V_n}\right). \tag{7.4b}$$

where V_{ol} and V_{oh} are the minimum and maximum output voltages, respectively.

Starting from $V_o = V_{oh}$ (between points (a) and (b) shown in Fig. 7.2b, c), $\frac{dC_{m_b}}{dt}$ is negative (for $\eta_b = 1$) which means that the C_{mb} decreases and V_{in} increases until reaches to V_p (point (b)), the upper comparator would change its output to be V_{ol} and the output of the lower comparator is still V_{oh}. Therefore, the output of the AND gate is V_{ol} and V_i inverted to $-V_p$ (point (c)). So the output of upper comparator changes to V_{oh}, lower comparator changes to V_{ol} and V_o is still V_{ol}. As a result

of that the memcapacitance C_{m_b} increases and $|V_i|$ decreases until reaches to $|V_n|$ (point (d)), which is negative, such that the lower comparator output is V_{oh} and the upper comparator is still V_{oh} so the output of the AND gate will be V_{oh} and V_i will change to $|V_n|$ (point (a)) and so on.

By increasing the input positive voltage V_i, the memcapacitance C_{m_b} decreases (the change in C_{m_a} is proportional to the change in C_{m_b} depending on α) so for $V_p > |V_n|$, $C_{m_b} < C_{m_n}$. Therefore, the necessary and sufficient condition for oscillation is obtained from the restriction on the memcapacitance's value C_{m_b} which should be within its boundary $C_{min} < C_{bp} < C_{m_b} < C_{bn} < C_{max}$. So the conditions for oscillation are given by

$$\frac{V_p C_{min}}{V_{oh} - (\alpha + 1)\, V_p} < C_{ind} < \frac{V_n C_{max}}{V_{ol} - (\alpha + 1)\, V_n}, \tag{7.5a}$$

$$C_{ind} \frac{V_{oh} - (\alpha + 1)\, V_p}{V_p} < C_{ind} \frac{V_{ol} - (\alpha\ + 1)\, V_n}{V_n}. \tag{7.5b}$$

The charge passing through the memcapacitor $q(t) = (C_a\, C_b)/\,(C_a + C_b\,)\, V_o(t)$ and substituting by (7.2), this charge can be written as:

$$q\,(t) = \frac{C_{mb} C_{ind}}{C_{m_b} + (\alpha + 1)\, C_{ind}}\, V_o\,(t)\,. \tag{7.6}$$

Then, from (7.1), the rate of change in memcapacitance C_{m_b}, which is not an implicit function C_{ma}, is

$$-\left(\frac{\alpha + 1}{C_{m_b}^3} + \frac{1}{C_{m_b}^2 C_{ind}}\right)\frac{dC_b}{dt} = \eta_b k_b' V_o(t). \tag{7.7}$$

By integrating both sides relative to time, where the memcapacitance C_b changes from C_{bn} to C_{bp} through T_h.

$$\int_{C_{b_n}}^{C_{b_p}} \left(\frac{\alpha + 1}{C_{m_b}^3} + \frac{1}{C_{m_b}^2 C_{ind}}\right) dC_b = -\eta_b k_b' \int_0^{T_h} V_o(t) dt. \tag{7.8}$$

The time of positive half cycle T_h is given by

$$T_h = \frac{1}{2\eta_b k_b' V_{oh}} \left(\frac{1}{C_{bn}} - \frac{1}{C_{bp}}\right)\left((\alpha\ + 1)\left(\frac{1}{C_{bn}} + \frac{1}{C_{bp}}\right) + \frac{2}{C_{ind}}\right). \tag{7.9}$$

A similar expression can be obtained for the time of negative half cycle T_L, for $V_o = V_{ol}$. So the oscillation frequency is

$$f_o = \frac{2D\eta_b k_b' V_{oh}}{\left(\frac{1}{C_{bp}} - \frac{1}{C_{bn}}\right)\left((\alpha + 1)\left(\frac{1}{C_{bn}} + \frac{1}{C_{bp}}\right) + \frac{2}{C_{ind}}\right)}, \tag{7.10}$$

where $D = |V_{ol}| / (V_{oh} + |V_{ol}|)$ representing the duty cycle of the oscillator. Substituting by (7.4), the oscillation frequency is

$$f_o = \frac{2D\eta_b\, k_b'\, V_{oh} C_{ind}^2 \left(V_{oh} - (\alpha + 1)\, V_p\right)^2 \left(V_{ol} - (\alpha + 1)\, V_n\right)^2}{\left(-(\alpha + 1)\left(V_{oh} V_n + V_{ol} V_p\right) + 2V_{oh} V_{ol}\right)\left(V_{ol} V_p - V_{oh} V_n\right)}. \tag{7.11}$$

The oscillation frequency is linearly proportional to the mobility factor k of the memcapacitor; so to obtain higher ranges of oscillation frequency, a high mobility factor memcapacitor should be used. Moreover, the oscillation frequency is proportional to C_{ind}^2 which can be controlled via the initial values of the memcapacitances and the parameter α. Moreover, this oscillator can give low oscillation frequencies where there are many parameters to control the frequency instead of an RC oscillator which requires high capacitor and resistor values.

7.2.2 Special Cases

There are four cases similar to the mentioned cases in series memcapacitors, but here we are interested in two cases only which are $\alpha = 0$, and $\alpha = \infty$.

7.2.2.1 *C-MC* Oscillator Configuration

In this case $k_a = 0$ so C_a is a capacitor and C_{m_b} is a memcapacitor with $\eta_b = 1$ which should be positive such that the oscillation frequency is positive as shown in Fig. 7.3a. The conditions for oscillation and the oscillation frequency are reduced to

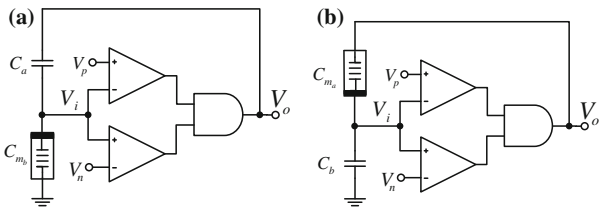

Fig. 7.3 Oscillator topologies **a** $\alpha = 0$, and **b** $\alpha = \infty$

$$C_{min}\frac{V_p}{V_{oh}-V_p} < C_a < C_{max}\frac{V_n}{V_{ol}-V_n}, \qquad V_p > V_n\frac{V_{oh}}{V_{ol}}. \tag{7.12a}$$

$$f_o = \frac{2Dk_b' V_{oh}C_a^2\left(V_{oh}-V_p\right)^2\left(V_{ol}-V_n\right)^2}{\left(V_p V_{ol}-V_n V_{oh}\right)\left(2V_{oh}V_{ol}-V_{oh}V_n-V_{ol}V_p\right)}. \tag{7.12b}$$

The maximum and minimum oscillation frequencies can be obtained from (7.12) by replacing C_a with its minimum and minimum value. They are given by

$$f_{omax} = \frac{2Dk_b' V_{oh}C_{max}^2 V_n^2\left(V_{oh}-V_p\right)^2}{\left(V_p V_{ol}-V_n V_{oh}\right)\left(2V_{oh}V_{ol}-V_{oh}V_n-V_{ol}V_p\right)}, \tag{7.13a}$$

$$f_{omin} = \frac{2Dk_b' V_{oh}C_{min}^2 V_p^2\left(V_{ol}-V_n\right)^2}{\left(V_p V_{ol}-V_n V_{oh}\right)\left(2V_{oh}V_{ol}-V_{oh}V_n-V_{ol}V_p\right)}. \tag{7.13b}$$

7.2.2.2 *MC-C* Oscillator Configuration

This case is the opposite of the previous case where $k_b' = 0$ so C_b is a capacitor and C_{m_a} is a memcapacitor with $\eta_a = -1$ as shown in Fig. 7.3b. The memcapacitance C_{m_a} increases for increasing the input voltage V_i so for $V_p > V_n$, $C_{a_p} > C_{a_n}$. Substituting by C_{ind}, $\eta_b k_b' = \eta_a k_a'/\alpha$ in (7.6) and (7.12) and by taking the limit at α tends to ∞. The condition for oscillation and oscillation frequency are given as follows:

$$C_{min}\frac{V_{ol}-V_n}{V_n} < C_b < C_{max}\frac{V_{oh}-V_p}{V_p}, V_p > V_n\frac{V_{oh}}{V_{ol}}. \tag{7.14a}$$

$$f_o = \frac{2Dk_a' V_{oh}C_b^2 V_p^2 V_n^2}{\left(V_p^2 V_{ol}^2 - V_n^2 V_{oh}^2\right)}, \tag{7.14b}$$

where the maximum and minimum oscillation frequencies are

$$f_{omax} = \frac{2Dk_b' V_{oh}C_{max}^2 V_n^2\left(V_{oh}-V_p\right)^2}{\left(V_p^2 V_{ol}^2 - V_n^2 V_{oh}^2\right)}, \tag{7.15a}$$

$$f_{omin} = \frac{2Dk_a' V_{oh}C_{min}^2 V_p^2\left(V_{ol}-V_n\right)^2}{\left(V_p^2 V_{ol}^2 - V_n^2 V_{oh}^2\right)}. \tag{7.15b}$$

Figure 7.4 shows the maximum and minimum obtained oscillation frequency for the two cases $\alpha = 0$ and $\alpha = \infty$ where the memcapacitor parameters C_{min}, C_{max} and k are 10 nF, 10 μF and 10 $MC^{-1}s^{-1}$, respectively. Figure 7.4a, b show the effect of changing V_p and V_n for $V_n = -0.5$ V and $V_p = 0.75$ V, respectively, where $C_a = 1\,\mu F$ for $\alpha = 0$ and $C_b = 1\,\mu F$ for $\alpha = \infty$. The oscillation frequency

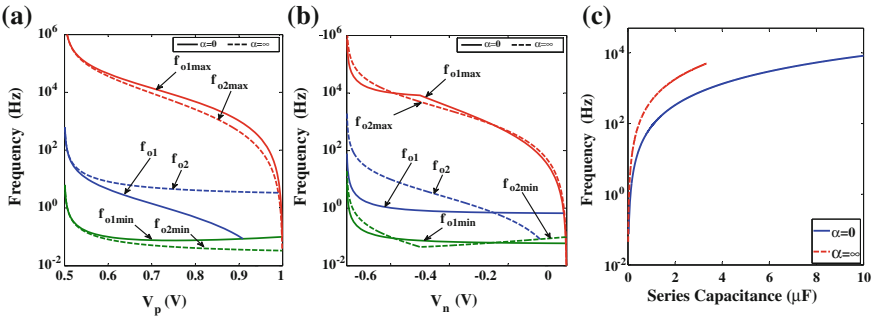

Fig. 7.4 Numerical simulation for $\alpha = 0$ and $\alpha = \infty$ for V_{oh} and V_{ol} are 1 V and −1 V

increases for increasing series capacitance (C_a for $\alpha = 0$ and C_b for $\alpha = \infty$) when using the same parameters. The oscillation frequency in case of $\alpha = \infty$ is higher than in case of $\alpha = 0$ for the same working region given from conditions for oscillation as shown in Fig. 7.4c.

7.2.3 Simulation Verification

Due to the lack of memcapacitor samples and the fact that they are not commercially available, the SPICE model of the memcapacitor is used which was proposed in [10]. The simulation was performed for the two different cases where memcapacitor parameters C_{min}, C_{max} and k are 10 nF, 10 μF and $10^7\,\mathrm{C}^{-1}\mathrm{s}^{-1}$, respectively. The oscillator is designed to satisfy the conditions for oscillation where V_{ol}, V_{oh}, V_n and V_p are −1, 1, −0.5 and 0.75 V, respectively.

The solid curve of Fig. 7.5 shows the transient response of this oscillator for $\alpha = 0$ where the oscillation frequency $f_o = 0.8325$ Hz for $C_a = 0.1$ μF matching the calculated frequency from (7.13). The memcapacitance C_{mb} changes from 0.0333

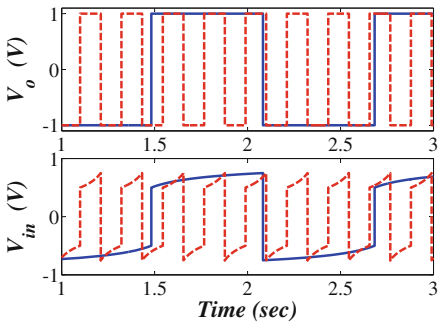

Fig. 7.5 Transient response of output voltage for $\alpha = 0$ (*solid line*) and $\alpha = \infty$ (*dotted line*)

to 0.1 μF. Moreover, the dotted curve in Fig. 7.5 shows the transient response for $\alpha = 8$ where the oscillation frequency = 4.496 Hz for $C_b = 0.1\,\mu$F matching that calculated from (7.15). The memcapacitance C_{ma} changes from 0.1 to 0.3 μF.

7.2.4 Stored Energy

The energy stored in the memcapacitor is discussed in [11], which is defined as

$$U = \int_{t_o}^{t} IV d\tau, \tag{7.16}$$

and the current $I = d(CV)/dt = \dot{C}V + C\dot{V}$, where C is the total capacitance $((C_a C_b)/(C_a + C_b))$, so

$$U = \int_{t_o}^{t} (\dot{C}V^2 + CV\dot{V}) d\tau = U_1 + U_2. \tag{7.17}$$

In order to get the energy stored by cycle, let $t = T + t_o$. Across period T, the voltage is $V_o h$ for $t_o < t < t_o + T_h$ so the memcapacitance C_{m_b} changes from C_{b_n} to C_{b_p} as discussed in the manuscript. And, when $t_o + T_h < t < t_o + T$, the output voltage is V_{ol} and memcapacitance C_{m_b} changes from C_{bp} to C_{bn}, so

$$U_1 = \int_{t_o}^{t} (\dot{C}V_o^2) d\tau = V_o^2 \int_{t_o}^{t} \frac{dC}{d\tau} d\tau = V_o^2 \int_{C_1}^{C_2} dC. \tag{7.18}$$

Therefore,

$$\begin{aligned} U_1 &= V_{oh}^2 \int_{C_{pos_{edge}}}^{C_{neg_{edge}}} dC + V_{ol}^2 \int_{C_{neg_{edge}}}^{C_{pos_{edge}}} dC \\ &= V_{oh}^2 \left(C_{neg_{edge}} - C_{pos_{edge}} \right) + V_{ol}^2 \left(C_{pos_{edge}} - C_{neg_{edge}} \right), \end{aligned} \tag{7.19}$$

where $C_{neg_{edge}}$ and $C_{pos_{edge}}$ are the negative edge and positive edge transition capacitances. The negative edge and positive edge transition capacitances

$$C_{neg_{edge}} = \frac{C_{bp} C_{ind}}{C_{bp} + (\alpha + 1) C_{ind}}, \qquad C_{pos_{edge}} = \frac{C_{bn} C_{ind}}{C_{bn} + (\alpha + 1) C_{ind}}. \tag{7.20}$$

Here, in the used oscillator topology $V_{oh} = -V_{ol}$ so $U_1 = 0$ but for U_2, the derivative of the output voltage is impulses so

$$U_2 = \int_{t_o}^{t} CV\dot{V}d\tau = C_{neg_{edge}}(V_{oh} - V_{ol})V_{oh} + C_{pos_{edge}}(V_{ol} - V_{oh})V_{ol}. \quad (7.21)$$

The total capacitance is given by

$$C(t) = \frac{C_{mb}C_{ind}}{C_{mb} + (\alpha + 1)C_{ind}}. \quad (7.22)$$

So the total stored energy is given by

$$U = U_2 = \frac{C_{bp}C_{ind}}{C_{bp} + (\alpha + 1)C_{ind}}(V_{oh} - V_{ol})V_{oh} + \frac{C_{bn}C_{ind}}{C_{bn} + (\alpha + 1)C_{ind}}(V_{ol} - V_{oh})V_{ol}. \quad (7.23)$$

For $V_{ol} = -V_{oh}$,

$$U = 2C_{ind}V_{oh}^2\left(\frac{C_{bp}}{C_{bp} + (\alpha + 1)C_{ind}} + \frac{C_{bn}}{C_{bn} + (\alpha + 1)C_{ind}}\right) = Const. \quad (7.24)$$

7.3 Boundary Effect on Memcapacitor-Based Oscillator

In this subsection, the effect of the nonlinear model ($p = 1$) on the oscillation frequency where $f(x) = 4x(1 - x)$ is discussed.

7.3.1 C-MC Oscillator Configuration

In this case, the oscillation concept is traced as was discussed in Sect. 7.2.2.1, where the values of C_{mp} and C_{mn} are given by the same relations in (7.4). The necessary and sufficient conditions for oscillation are obtained as in (7.12). Besides, the rate of change of the parameter x is

$$\frac{dx}{dt} = -k\frac{V_o}{D_m + D_a}f(x) = -4kx(1 - x)\frac{V_o}{D_m + D_a}, \quad (7.25)$$

where $D_a = C_a^{-1}$ and $D_m = C_m^{-1}$. Substituting by D_m, then

$$\left(\frac{D_{max} + D_a}{x} + \frac{D_{min} + D_a}{1 - x}\right)\frac{dx}{dt} = -4kV_o. \quad (7.26)$$

By integrating the left-hand side term from x_{mn} (corresponding to C_{mn}) to x_{mp} (corresponding to C_{mp})and the right-hand side term from 0 to T_H. After integration and performing some simplifications, the time of positive half cycle T_H is given by

$$T_H = \frac{(D_{max} + D_a)ln\left(\frac{x_{mp}}{x_{mn}}\right) - (D_{min} + D_a)ln\left(\frac{1-x_{mp}}{1-x_{mn}}\right)}{4kV_{oh}}. \tag{7.27}$$

Substituting by x_{mn} and x_{mp}. The oscillation frequency is given as follows:

$$f_o = \frac{2kV_{oh}}{(D_{max} + D_a)ln\left(\frac{D_{mp}-D_{max}}{D_{mn}-D_{max}}\right) + (D_{min} + D_a)ln\left(\frac{D_{min}-D_{mn}}{D_{min}-D_{mp}}\right)}, \tag{7.28}$$

where $D_{mn} = C_{mn}^{-1}$ and $D_{mp} = C_{mp}^{-1}$.

7.3.2 MC-C Oscillator Configuration

Moreover, in this case, the necessary and sufficient conditions for oscillation also obtained as in (7.14). By doing the same aforementioned steps, the oscillation frequency in case of nonlinear dopant model ($p = 1$) is given by

$$f_o = \frac{2kV_{oh}}{(D_{max} + D_b)ln\left(\frac{D_{mn}-D_{max}}{D_{mp}-D_{max}}\right) + (D_{min} + D_b)ln\left(\frac{D_{min}-D_{mp}}{D_{min}-D_{mn}}\right)}. \tag{7.29}$$

7.3.3 Results and Discussion

In the aforementioned expressions, the oscillation frequency is always linearly proportional to the doping factor k of the memcapacitor; so for more higher ranges of oscillation frequency, more high doping factor memcapacitors should be used. Also, as clear from (7.28) and (7.29), the oscillation frequency in linear case is proportional to the square of series capacitance C_a or C_b that are bounded by $C_{a_{min}}$ and $C_{a_{max}}$ or $C_{b_{min}}$ and $C_{b_{max}}$ obtained from (7.12) and (7.14), respectively. However, in case of nonlinear model, the oscillation frequency tends to zero at minimum and maximum series capacitance as shown in Fig. 7.6 and has peaking in at certain series capacitance. Figure 7.6 is plotted for $C_{min}, C_{max}, k, V_{ol}, V_{oh}, V_n$, and V_p equal to 10 nF, 10 µF, 10 $MC^{-1}S^{-1}$, −1, 1, 0.5, and 0.75 V, respectively. Moreover, MC-C configuration gives higher frequency than C-MC configuration for linear and nonlinear models in the common region $[C_{a_{min}}, C_{b_{max}}]$ except a narrow region in nonlinear case as shown in Fig. 7.6.

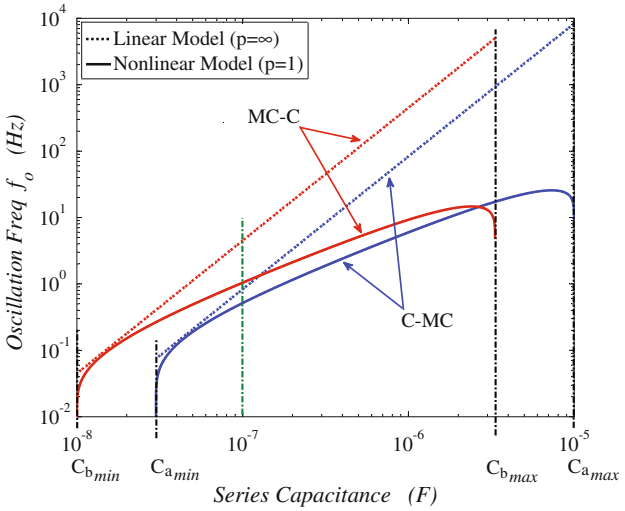

Fig. 7.6 Obtained oscillation frequency versus series capacitance for both models and both configurations

In case of using 100 nF series capacitance, the oscillation frequency in case of MC-C configuration is higher than in case of C-MC configuration as clear in Fig. 7.6. Figure 7.7a shows the transient response for nonlinear dopant drift model ($p = 1$) where the oscillation frequency = 0.512 Hz matching that calculated from (7.28) where the memcapacitance C_m changes from 0.0333 to 0.1 μF. Moreover, in MC-C oscillator configuration, the obtained oscillation frequency is 1.0437 Hz matching the calculated from (7.29) as shown in Fig. 7.7b. But here, memcapacitance C_m changes from 0.1 to 0.3 μF.

It is worth to be noted that the memcapacitor behavior differs from memristor behavior where the memristor decreases with positive applied voltage but memcapacitor increases so the conditions for oscillations are reversed. Also expression for the

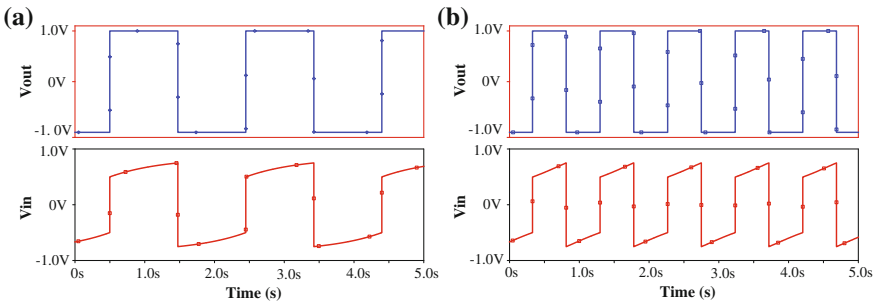

Fig. 7.7 PSPICE simulation of nonlinear model ($p = 1$). **a** C-MC oscillator and **b** MC-C oscillator

oscillation frequency is the near the same but replace R with $1/C$ in memristor-based oscillator expression to get memcapacitor-based oscillator. Moreover, no power consumption in memcapacitor makes the memcapacitor-based oscillators suitable for low-power applications.

7.4 Memcapacitor Bridge Synapses

The idea of memcapacitor-based synapses was introduced in [12, 13] which is similar to the memristor synaptic circuit proposed in [14]. The synaptic bridge circuit consists from four memcapacitors connected in two parallel branches; each branch has two series memcapacitors connected with reversed polarity as shown in Fig. 7.8. The two parallel branches are connected between excitation source and ground. This bridge has two identical memcapacitors for instance; D_{m1} and D_{m4} are identical having the same initial memcapacitance and same polarity also D_{m2} and D_{m3} are identical. In case of exciting the bridge, the memcapacitance of each pair of memcapacitors (e.g., (D_{m1}, D_{m3})) increases or decreases depending on the sign of the applied signal with the same rate but the other pair decreases or increases, respectively. The midpoint voltage (V_p or V_n) in a branch changes inversely with the midpoint voltage (V_n or V_p) of the other branch; for example, V_p increases, V_n decreases, and vice versa. These point voltages with respective to the input are given by

$$V_p = \frac{D_{m2}}{D_{m1} + D_{m2}} V_{in} \tag{7.30a}$$

$$V_n = \frac{D_{m4}}{D_{m3} + D_{m4}} V_{in} \tag{7.30b}$$

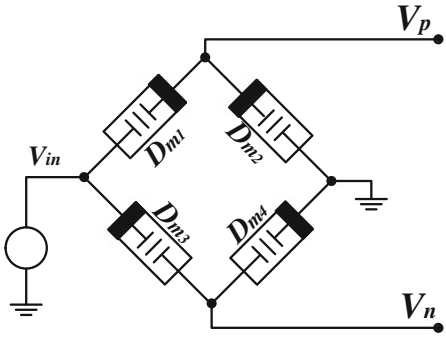

Fig. 7.8 Memcapacitor bridge circuit [12, 13]

The differential output voltage of the bridge is the difference between V_p and V_n and is given by

$$V_{out} = V_p - V_n = \left[\frac{D_{m2}}{D_{m1} + D_{m2}} - \frac{D_{m4}}{D_{m3} + D_{m4}}\right] V_{in} \tag{7.31}$$

which can be rewritten as a relationship $V_{out} = \psi V_{in}$, where ψ represents the synaptic weight and is given by

$$\psi = \frac{D_{m2}}{D_{m1} + D_{m2}} - \frac{D_{m4}}{D_{m3} + D_{m4}} \tag{7.32}$$

The positive/negative synaptic weight is represented if the previous equation is greater/less than zero, respectively. As discussed before when the memelastances D_{m1} and D_{m4} are equal and also D_{m2} and D_{m3} are equal, then the input elastance of each branch are equal so $D_{m1} + D_{m2} = D_{m3} + D_{m4}$. Applying a current pulse as an input, the input charge $q(t)$ is divided equally to the two branches and the input voltage is $V_{in} = (D_{m1} + D_{m2})q(t)/2$ and the midpoint voltages are $V_p = 0.5D_{m2}q(t)$, and $V_n = 0.5D_{m4}q(t)$. Consequently, the synaptic weight is given by

$$\psi = \frac{V_p - V_n}{V_{in}} = \frac{D_a - D_b}{D_a + D_b} \tag{7.33}$$

where $D_a = D_{m2} = D_{m3}$ and $D_b = D_{m1} = D_{m4}$. The memcapacitor bridge circuit is connected to the differential amplifier with three transistors as shown in Fig. 7.9 to implement the complete synaptic circuit where the differential amplifier performs the voltage-to-current conversion.

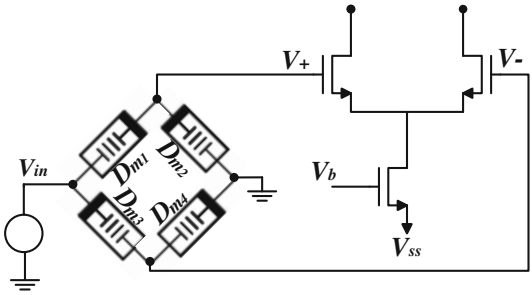

Fig. 7.9 Memcapacitor bridge synaptic circuit [12, 13]

7.4.1 Mathematical Analysis of Memcapacitor Bridge

The used model of the current-controlled memcapacitor was introduced by Biolek et. al [10] where the reciprocal of the memcapacitance $D(t)$ is given by

$$D(t) = D_{min} + x(t)(D_{max} - D_{min}),\ D \in [D_{max}, D_{min}] \tag{7.34a}$$

$$\frac{dx}{dt} = \eta k q(t) f(x) \tag{7.34b}$$

where $x(t)$ represents the state variable of the memcapacitor, D_{max} and D_{min} are the inverse memcapacitances of C_{min} and C_{max}, respectively. The parameter k is the mobility factor and the window function $f(x)$ is given by $f(x) = 1 - (2x - 1)^{2p}$ based on Joglekar's window function [10], and η represents the polarity of the memcapacitor. The analyses of series and parallel memcapacitors were discussed in details in the previous section for voltage excitation and for linear memcapacitor model $p = \infty$. However, the analysis in [13] was based on the highest nonlinear case when $p = 1$, therefore, $f(x) = 4x(1 - x)$.

7.4.1.1 Two Anti-Series Memcapacitor Analysis

In order to simplify the analysis, the solution of the memcapacitance is performed on the state variable and then transformed to the memcapacitance using (7.34). The state variables of the two memcapacitors are given by

$$\frac{dx_a}{dt} = 4\eta_a k q_a(t) x_a (1 - x_a) \tag{7.35a}$$

$$\frac{dx_b}{dt} = 4\eta_b k q_b(t) x_b (1 - x_b) \tag{7.35b}$$

In case of series memcapacitors, $q_a(t) = q_b(t) = q(t)$ where $q(t) = \int_0^t i(\tau) d\tau$. By separating the variables and integrating both sides of (7.35a) relative to time

$$\int_{x_{o_a}}^{x_a} \left(\frac{1}{x_a} + \frac{1}{1 - x_a} \right) dx_a = 4\eta_a k \int_0^t q(\tau) d\tau \tag{7.36}$$

where x_{o_a} is the initial state of D_a. After performing previous integrations and doing some simplifications, the state variable of D_a is given by

$$x_a = \frac{x_{o_a}}{x_{o_a} + (1 - x_{o_a}) e^{-4\eta_a k \sigma(t)}},\ x_a \in [0, 1] \tag{7.37}$$

where $\sigma(t)$ is the time integral of the charge passing through memcapacitor. Similarly, the state variable of D_b is given by

$$x_b = \frac{x_{o_b}}{x_{o_b} + (1 - x_{o_b})e^{-4\eta_b k\sigma(t)}},\ x_b \in [0, 1] \tag{7.38}$$

where x_{o_b} is the initial state of D_b. The initial state variables are given by

$$x_{o_a} = \frac{D_{o_a} - D_{min}}{D_d}, \quad x_{o_b} = \frac{D_{o_a} - D_{min}}{D_d} \tag{7.39}$$

where D_{o_a} and D_{o_b} are the initial memelastances of D_a and D_b, respectively. Substituting by x_a and x_b to get D_a and D_b

$$D_a(t) = D_{min} + \frac{D_d(D_{o_a} - D_{min})}{D_{o_a} - D_{min} + (D_{max} - D_{o_a})e^{-4\eta_a k\sigma(t)}} \tag{7.40a}$$

$$D_b(t) = D_{min} + \frac{D_d(D_{o_b} - D_{min})}{D_{o_b} - D_{min} + (D_{max} - D_{o_b})e^{-4\eta_b k\sigma(t)}} \tag{7.40b}$$

where $D_d = D_{max} - D_{min}$. The voltage across the two memcapacitors due to the excitation current is $V(t) = (D_a + D_b)q(t)$. The difference and sum of memelastances are given as follows:

$$D_a - D_b = D_d(x_a - x_b) \tag{7.41a}$$

$$D_a + D_b = 2D_{min} + D_d(x_a + x_b) \tag{7.41b}$$

In order to obtain maximize the linear region, a symmetric behavior should be obtained. So the initial state variables are related together by $x_{o_b} = 1 - x_{o_a}$. Also, the polarities of memcapacitor are reversed so $\eta_b = -\eta_a = \eta$. The weight function $\psi(t)$ is given by

$$\psi(t) = \frac{D_d\left[(D_{oa} - D_{min})^2 e^{-4\eta k\sigma(t)} - (D_{max} - D_{oa})^2 e^{4\eta k\sigma(t)}\right]}{2[D_{min} + D_{max}][D_{oa} - D_{min}][D_{max} - D_{oa}] + (D_{max} - D_{oa})^2(3D_{min} - D_{max})e^{4\eta k\sigma(t)} + (D_{o_a} - D_{min})^2(D_{min} + D_{max})e^{-4\eta k\sigma(t)}} \tag{7.42}$$

Practically, the memcapacitor has an initial capacitance depending on fabrication so to ensure the linear region, the memcapacitance should be changed to the middle point. The circuit published in [15] can be used to do this operation. Moreover, it is clear that applying a pulse to the bridge will change the initial memcapacitances so this pulse should be repeated with the opposite polarity to remove the effect of the initial pulse. Doublet generator circuit can be used to do this rule [16] which will prevent memcapacitor variations. This doublet circuit gives high speed and similar area between the positive and the negative cycles.

7.4.1.2 Maximum Pulse Period

It is required to apply a strong pulse such that the memcapacitance changes its state. From (7.37), the time integral of charge $\sigma(t)$ for one memcapacitor, as function of the state variable, is given by

$$\sigma(t) = \frac{1}{4\eta k} \ln\left(\frac{x(1-x_o)}{x_o(1-x)}\right) \tag{7.43}$$

where x_o is the initial state variable and η memcapacitor polarity. As obvious from the previous equation that x_o should not equal either 0 or 1 where the memcapacitor cling to one of its boundaries where an infinite σ is required to change this state which is not practical. Therefore, let us assume that minimum and maximum state values are 0.01 and 0.99. The needed σ equal $2.298\eta k(C.S)$. In case of applying a unit pulse current with period T and amplitude I_o as input to synaptic bridge circuit. The current is divided equally into the two branches. So, the current passing through each memcapacitor is mathematically defined as $i(t) = 0.5I_o(u(t) - u(t-T))$ so the time integral of the charge is given by

$$\sigma(t) = \frac{I_o}{4}t^2, \quad t \in [0, T] \tag{7.44}$$

Thus, the maximum σ equals $I_o T^2/4$. The required pulse period T_p is needed such that the memcapacitor changes its state completely as function of initial memelastance

$$T_p = \sqrt{\frac{1}{k|I_o|} \ln\left(\frac{(D - D_{min})(D_{max} - D_o)}{(D_o - D_{min})(D_{max} - D)}\right)} \tag{7.45}$$

Figure 7.10 shows the pulse width T_p as a function of the theoretical maximum memelastance divided by the maximum memelastance when $k = 10\,\mathrm{M(CS)}^{-1}$ and $I_o = 1\mu\mathrm{A}$. It is obvious that the time increases as the theoretical maximum memelastance increases, and the pulse width tends to ∞ at $D_{th}/D_{max} = 1$.

7.4.2 Weight Programming

Equation (7.33) defines the synaptic weighting operation in the memcapacitor bridge. The synaptic weight processing was performed with very small or narrow pulses so that their effect on the change in the memcapacitor was negligible. By contrast, the pulses for synaptic weight programming must be strong enough to change the charge operating point of the memcapacitor. If the synaptic weight ψ is larger than 0, then it is called positive synaptic weight and its condition is

$$D_a > D_b \tag{7.46}$$

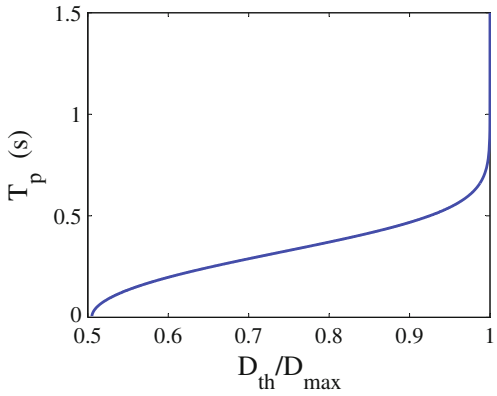

Fig. 7.10 Pulse width versus changing the initial memelastance

By substituting (7.40) and simplifying the expression at the same discussed conditions ($\eta_b = -\eta_a = \eta$ and $x_{o_a} = 1 - x_{o_b}$), the condition of positive synaptic weight is reduced to

$$\sigma(t) < \frac{1}{4\eta k} \ln\left(\frac{D_{o_a} - D_{min}}{D_{max} - D_{o_a}}\right) \tag{7.47}$$

Similarly, the conditions for negative weight or zero synaptic weight are $D_a < D_b$ and $D_a = D_b$, respectively, and can be reduced to

$$\sigma(t) > \frac{1}{4\eta k} \ln\left(\frac{D_{o_a} - D_{min}}{D_{max} - D_{o_a}}\right) \tag{7.48}$$

and

$$\sigma(t) = \frac{1}{4\eta k} \ln\left(\frac{D_{o_a} - D_{min}}{D_{max} - D_{o_a}}\right), \tag{7.49}$$

respectively.

Figure 7.11 shows the regions in which the synaptic weight is either positive, negative, or zero for $k = 10\,\mathrm{M(CS)}^{-1}$, $C_{min} = 100\,\mathrm{nF}$, and $C_{max} = 10\,\mu\mathrm{F}$. The linearity of the memcapacitor bridge circuit was discussed in detail in [12] and is discussed briefly in the next section.

7.4.3 SPICE Validation

Simulations were performed using memcapacitor SPICE model, proposed in [10] with the following parameters $k = 10\,\mathrm{M(CS)}^{-1}$, $C_{max} = 10\,\mu\mathrm{F}$, and $C_{min} = 100\,\mathrm{nF}$. Moreover, the initial state variable is assumed to be either 0.01 or 0.99 where the

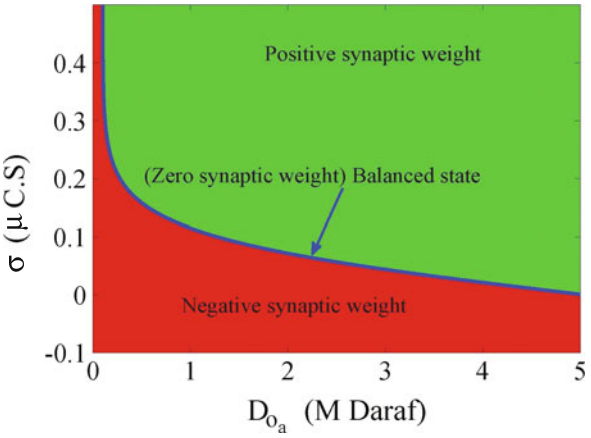

Fig. 7.11 Synaptic weight regions

corresponding initial memcapacitances are 9.99 μF and 100 nF. And, the excitation source is current pulse signal with amplitude $I_o = 1\,\mu A$ and pulse width $T_p = 2\,S$.

Mathematical analysis of memcapacitor bridge circuit is verified using SPICE simulations as shown in Fig. 7.12 for $p = 1$ showing a perfect matching. As obvious

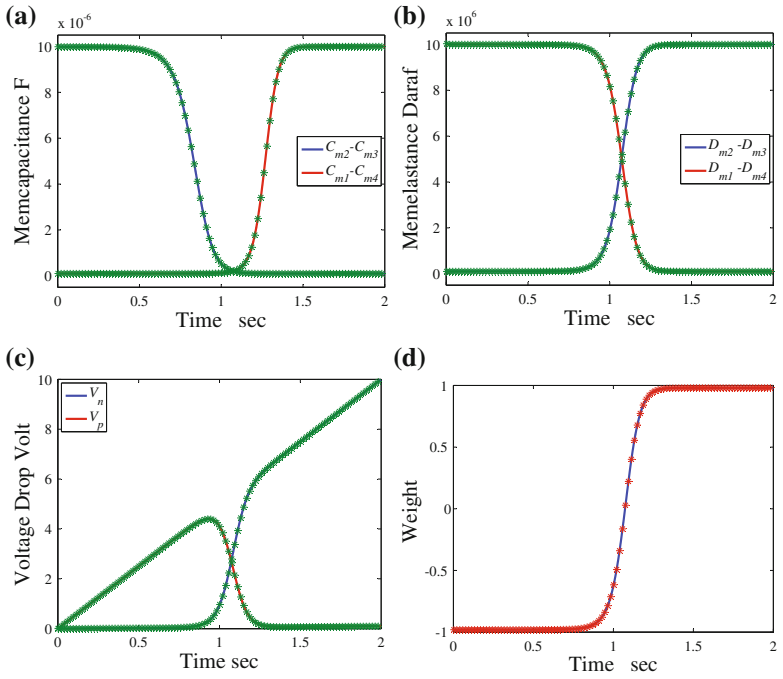

Fig. 7.12 PSPICE verification for memcapacitances, voltage drop across memcapacitors, and the synaptic weight

in Fig. 7.12d, the linearity of the synaptic weight in three regions, beginning area, center area, and ending area, where the weight is almost constant at the beginning and ending areas and increases in the center area.

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Chapter 8
Meminductor: Modeling, Analysis, and Emulators

8.1 Introduction

The third mem-element is the meminductor (short for memory + inductor), which was postulated for the first time in [1] as one of the higher order elements. Then, Chua presented at the opening lecture of the First Memristor and Memristive Symposium held at UC Berkeley in 2008 [2]. The meminductor represents the link between charge $q(t)$ and time integral of the flux $\rho(t)$. Figure 8.1 shows the number of publications based on the meminductor versus the last six years. In 2009, Di ventra, Pershin and Chua defined the general models for the meminductive systems in [3] which described the nth-order current-controlled meminductive system

$$\varphi(t) = L_m(x, i, t)i(t), \tag{8.1a}$$

$$\dot{x} = f(x, i, t). \tag{8.1b}$$

where L_m is the meminductance and the nth-order flux-controlled meminductive system is defined as follows:

$$I(t) = L^{-1}(x, \varphi, t)\varphi(t), \tag{8.2a}$$

$$\dot{x} = f(x, \varphi, t). \tag{8.2b}$$

with L^{-1} being the inverse meminductance. A subclass of current-controlled meminductor can be defined by reducing (8.1) to

$$\varphi(t) = L\left[\int_{t_o}^{t} I(\tau)d\tau\right] I(t), \tag{8.3}$$

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DOI 10.1007/978-3-319-17491-4_8

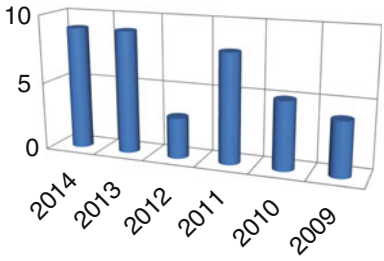

Fig. 8.1 Number of publications versus the last six years based on the engineering village database (December 2014)

and a flux-controlled meminductor subclass by reducing (8.2)

$$I(t) = L^{-1}\left[\int_{t_o}^{t} \varphi(\tau)d\tau\right]\varphi(t). \tag{8.4}$$

The power and the stored energy in the meminductive systems [3] are given by

$$P_L = V_L(t)I_L(t) \tag{8.5a}$$

$$U_L = \int_{t_o}^{t} V_L(\tau)I_L(\tau)d\tau \tag{8.5b}$$

V_L and I_L are the voltage across the meminductive system and input current, respectively.

Recently, a realization for meminductor is introduced in [4]. The authors demonstrate pinched hysteretic magnetic flux–current signals at room temperature. This device is built based on the spin hall magnetoresistance effect in several nanometer-thick thin films, exhibiting the nonvolatile memorizing property and magnetic energy storage ability of the meminductor.

But, the first theoretical meminductor model is build by Biolek et al. based on the idea of a simple electromechanical system [5], shown in Fig. 8.2. The coil has two terminal; one fixed (on the left) and one sliding terminal, which can be moved within limits defined by distances l_{min} and l_{max} from the fixed terminal. The slider positions l_{min} and l_{max} determine the limiting values of the coil inductances L_{min} and L_{max}. So, the state variable x, which enclosed between 0 and 1, is defined as

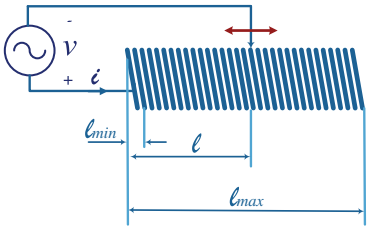

Fig. 8.2 Electromechanical model of the meminductor [5]

$$x = \frac{l - l_{min}}{l_{max} - l_{min}}. \tag{8.6}$$

The coil inductance L is, roughly speaking, proportional to the square of the number of turns N. So, the meminductance introduced by Biolek's L_m is enclosed between minimum meminductance L_{min} and maximum meminductance L_{max} which is given as follows:

$$L_m(t) \approx \left(\sqrt{L_{min}} + x(t)(\sqrt{L_{max}} - \sqrt{L_{min}})\right)^2, \tag{8.7}$$

where the rate of change in the state variable $x(t)$ is given by

$$\frac{dx}{dt} = K_L i(t), \tag{8.8}$$

which is directly proportional to the mobility factor K_L. The Spice model of the mem-elements is introduced in [6, 7] and can be found in Appendix A.

Mathematical modeling of mem-elements is essential to study their behavior in order to easily implement them in circuits where different current and voltage signals are applied. These analyses were introduced for the memristor in [8] and more definitions were defined for mem-elements like saturation time and mem-element range in [9].

8.2 Mathematical Representations of Time-Invariant Meminductor

Three mathematical representations of time-invariant meminductors can be defined. Each representation has two forms; current-controlled meminductor or flux-controlled meminductor. These three representations can be briefly presented as follows:

8.2.1 Extended Meminductor

An extended meminductor is defined as

- Current-controlled extended meminductor

$$\varphi = L(x, i)i, \tag{8.9a}$$

$$\frac{dx}{dt} = f(x, i), \tag{8.9b}$$

where $\lim_{i \to 0} L(x, i) \neq \infty$.

- Flux-controlled extended meminductor

$$i = L^{-1}(x, \varphi)\varphi, \tag{8.10a}$$

$$\frac{dx}{dt} = g(x, \varphi), \tag{8.10b}$$

where $\lim_{\varphi \to 0} L^{-1}(x, \varphi) \neq \infty$.

8.2.2 Generic Meminductor

A generic meminductor is defined in

- Current-controlled generic meminductor

$$\varphi = L(x)i, \tag{8.11a}$$

$$\frac{dx}{dt} = f(x, i), \tag{8.11b}$$

- Flux-controlled generic meminductor

$$i = L^{-1}(x)\varphi, \tag{8.12a}$$

$$\frac{dx}{dt} = g(x, \varphi), \tag{8.12b}$$

8.2.3 Ideal Meminductor

An ideal meminductor is defined as

- Current-controlled ideal meminductor

$$\rho = \rho_1(q). \tag{8.13}$$

Or

$$\varphi = L(q)i, \tag{8.14a}$$

$$\frac{dq}{dt} = i, \tag{8.14b}$$

where $L(q) = \frac{d\rho_1(q)}{dq}$ is called meminductance in Henry (H). The constitutive relation of current-controlled ideal meminductor can be recovered to $\rho_1(q) = \rho_0 + \int_0^t L(q)dq$ where ρ_0 is an arbitrary constant.
As obvious that Biolek's meminductor model, presented in the previous section, belongs to the ideal model representation.

- Flux-controlled ideal meminductor

$$q = q_1(\rho). \tag{8.15}$$

Or

$$q = L^{-1}(\rho)v, \tag{8.16a}$$

$$\frac{d\rho}{dt} = v, \tag{8.16b}$$

where $G(\rho) = \frac{dq_1(\rho)}{d\rho}$ is called inverse meminductance in inverse Henry (H^{-1}). The constitutive relation of flux-controlled ideal meminductor can be recovered to $q_1(\rho) = q_0 + \int_0^t C(\rho)d\rho$ where q_0 is an arbitrary constant.

8.3 Mathematical Model of Meminductor

In the linear circuit theory, the voltage across the conventional inductor is proportional to the rate of change of the current passing through the inductor and the proportional constant is the known inductance. However, the inductance of the meminductor was given by (8.7), and it is a function of the state variable x [9]. Therefore, the implicit relation between the meminductance and the current can be obtained by differentiating (8.7) with respect to time and substituting (8.8)

$$\frac{1}{2\sqrt{L_m(t)}}\frac{dL_m(t)}{dt} = K_L(\sqrt{L_{max}} - \sqrt{L_{min}})i(t). \tag{8.17}$$

By integrating both sides with respect to time, the meminductance is given by

$$L_m(t) = \left(\sqrt{L_o} + K'_L q(t)\right)^2, \tag{8.18}$$

where K'_L=$K_L(\sqrt{L_{max}} - \sqrt{L_{min}})$, $q(t) = \int_{-\infty}^t i(\tau)d\tau$ and L_o represents the initial meminductance. The instantaneous meminductance is a quadratic equation of the charge $q(t)$. The voltage can be defined as the rate of change of the flux, so the voltage across the meminductor is given by:

$$V_L(t) = \frac{d\varphi(t)}{dt} = \frac{d}{dt}(L(t)i_L(t)) = L(t)\frac{di_L(t)}{dt} + i_L(t)\frac{dL(t)}{dt}. \tag{8.19}$$

Then the voltage is given by:

$$V_L(t) = 2K'_L\sqrt{L(t)}i_L^2(t) + L(t)\frac{di_L(t)}{dt}. \tag{8.20}$$

By substituting into (8.6), the power and energy are given by:

$$P_L(t) = 2K'_L\sqrt{L(t)}i_L^3(t) + L(t)i_L(t)\frac{di_L(t)}{dt} \tag{8.21a}$$

$$U_L(t) = \int_{t_o}^{t}\left(2K'_L\sqrt{L(\tau)}i_L^3(\tau) + L(\tau)i_L(\tau)\frac{di_L(\tau)}{d\tau}\right)d\tau \tag{8.21b}$$

8.4 Meminductor Response Under Current Excitations

In this section, we investigate the response of the meminductor under step (DC), sinusoidal, and periodic current signals. In addition some fundamentals were introduced such as saturation time, power, and energy [9].

8.4.1 Step Response

A DC current is mathematically defined by the step current $i(t) = i_{DC}u(t)$, where $u(t)$ is the unit step function and the amplitude i_{DC} may be positive or negative [10]. By substituting into (8.18), the meminductance is given by

$$L_m(t) = \left(\sqrt{L_o} + K'_L i_{DC}t\right)^2. \tag{8.22}$$

The meminductance increases when i_{DC} is positive until the meminductance reaches its maximum L_{max}. However in case of negative i_{DC}, the meminductance decreases until it reaches its minimum L_{min} as shown in Fig. 8.3a, b for L_{min}, L_{max}, L_o and K_L are equal to 0.1, 10, 1 mH, and 10 $\mathrm{A^{-1}s^{-1}}$, respectively (these values are used throughout the chapter).

From the previous discussion, there is a certain time duration in which the meminductance reaches its boundary either maximum or minimum depending on the sign of the input voltage so the saturation time should be calculated. The saturation time is given by

$$t_{sat} = \frac{\sqrt{L_{bd}} - \sqrt{L_o}}{K'_L i_{DC}}, \tag{8.23}$$

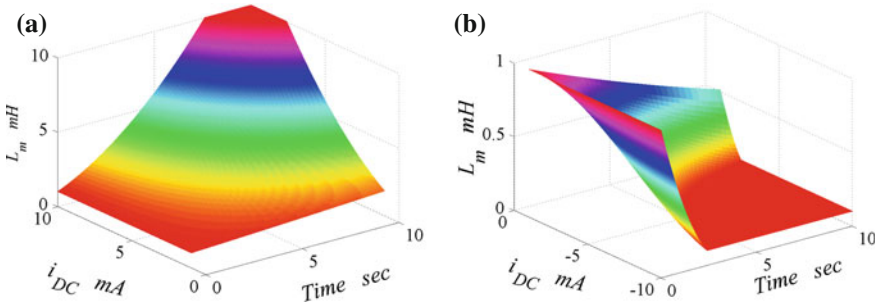

Fig. 8.3 Step response of meminductor due to DC current excitation for **a** positive current, and **b** negative current

where L_{bd} represents the boundary meminductance at either L_{max} or L_{min} depending on the polarity of the applied current. The maximum saturation time is reached when the meminductor changes its state from the minimum to maximum values or vice versa. Therefore, the maximum saturation time is

$$t_{sat_{max}} = \frac{\sqrt{L_{max}} - \sqrt{L_{min}}}{K'_L |i_{DC}|} = \frac{1}{K_L |i_{DC}|}, \tag{8.24}$$

where the maximum saturation time is inversely proportional to the amplitude and mobility factor of the meminductor.

The time derivative of the current step signal is impulse signal with amplitude i_{DC}. Hence, the voltage across the meminductor is

$$V_L(t) = V_{L1}(t) + V_{L2}(t) = L_o i_{DC} \delta(t) + i_{DC} \frac{dL(t)}{dt}, \tag{8.25}$$

where $V_{L1}(t)$ and $V_{L2}(t)$ are the voltage across the meminductor due to the change of current and meminductance, respectively. So the power and energy for $L_{min} < L < L_{max}$ are given by

$$P_L(t) = P_{L1}(t) + P_{L2}(t) = L_o i_{DC}^2 u(t) \frac{du(t)}{dt} + i_{DC}^2 \frac{dL(t)}{dt} \tag{8.26a}$$

$$U_L(t) = \int_{t_o}^{t} P_{L1}(\tau) d\tau + \int_{t_o}^{t} P_{L2}(\tau) d\tau = U_{L1}(t) + U_{L2}(t) \tag{8.26b}$$

$$U_{L1}(t) = \frac{1}{2} L_o (i_{DC}^2 - i_o^2) \tag{8.26c}$$

$$U_{L2}(t) = i_{DC}^2 (L(t) - L_o) \tag{8.26d}$$

$$U_L(t) = \frac{1}{2} i_{DC}^2 (2L(t) - L_o) - \frac{1}{2} i_o^2 L_o, \tag{8.26e}$$

where i_o is the initial current in the meminductor. The terms $P_{L1}(t)$ and $U_{L1}(t)$ are the instantaneous power and energy due to the current rate of change which is identical to the conventional inductor, however the terms $P_{L2}(t)$ and $U_{L2}(t)$ are the instantaneous power and energy due to the meminductance rate of change which is the added part in the meminductor. Under zero initial current $i_o = 0$, the total energy will be positive (charging stage) and negative (discharging stage) when $L(t) > 0.5L_o$ and $L(t) < 0.5L_o$, respectively. The energy stored in the meminductor increases/decreases for positive/negative input step until meminductance reaches to L_{max} or L_{min}, respectively.

8.4.2 Sinusoidal Response

The inductor has a linear relation between flux $\varphi(t)$ and current $i(t)$ and a circular relation between voltage $V(t)$ and current $i(t)$. But, the meminductor has a pinched hysteresis between flux $\varphi(t)$ and current $i(t)$ as shown in Fig. 8.4a and a nonlinear persimmon-shaped relation between voltage $V(t)$ and current $i(t)$ as shown in Fig. 8.4b. The pinched hysteresis shrinks until it becomes linear by increasing the applied frequency and the elliptic relation expands till it becomes circular as shown in Fig. 8.4a, b, respectively. As obvious from Fig. 8.4b, the I–V hysteresis have an even symmetry around the voltage axis.

Assuming that a single tone current is applied on the meminductor given by $i(t) = i_o sin(\omega_o t)$, and then by substituting into (8.18), the meminductance is given by

$$L_m(t) = \left(\sqrt{L_o} + 2K'_L \frac{i_0}{\omega_o} sin^2\left(\frac{\omega_o t}{2}\right)\right)^2. \tag{8.27}$$

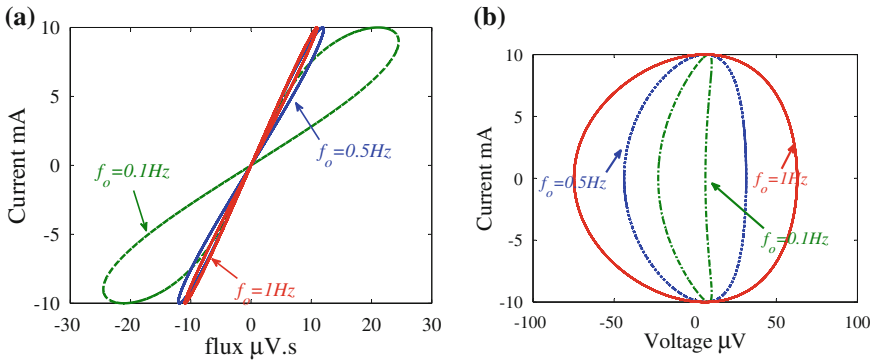

Fig. 8.4 Sinusoidal response of meminductor for different frequencies **a** flux–current hysteresis, and **b** current–voltage hysteresis

The meminductance range decreases until it reaches a value of zero where the meminductance will not change its initial value L_o by increasing the applied frequency as shown in Fig. 8.5 at $L_o = 1\,\text{mH}$ for positive or negative applied current.

Substituting into (8.20), the voltage across the meminductor is given by:

$$V_L(t) = 2K'_L i_o^2 \left(\sqrt{L_o} + \frac{2K'_L i_o}{\omega_o} sin^2\left(\frac{\omega_o t}{2}\right)\right) sin^2(\omega_o t) + i_o \left(\sqrt{L_o} + \frac{2K'_L i_o}{\omega_o} sin^2\left(\frac{\omega_o t}{2}\right)\right)^2 cos(\omega_o t) \tag{8.28}$$

when ω_o tends to infinity, the meminductor voltage equation tends to $V_L(t) = \omega_o L_o i_o cos(\omega_o t)$. Figure 8.6 shows the transient power and stored energy into the meminductor for sinusoidal input with amplitude $i_o = 10\,\text{mA}$ and frequency $f_o = 0.1\,\text{Hz}$. It is obvious that the instantaneous stored energy equals zero after a complete period which means that the average consumed power is zero.

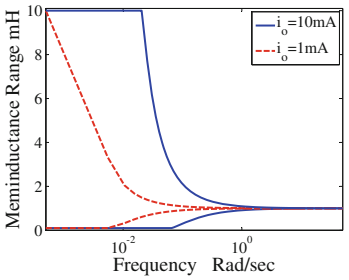

Fig. 8.5 Meminductance range versus applied frequency

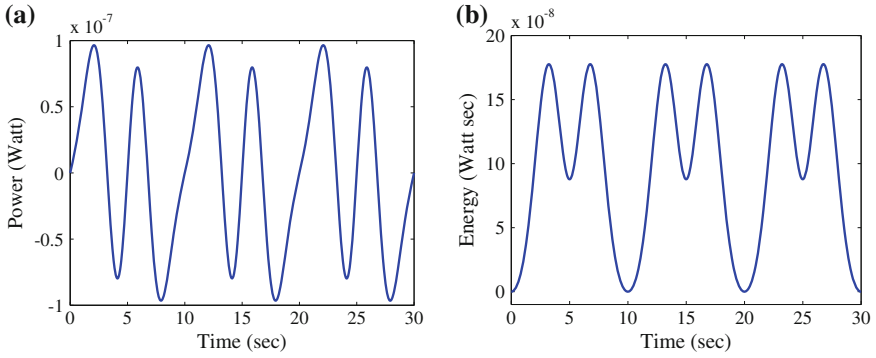

Fig. 8.6 Transient numerical simulation for power and energy of meminductor under sinusoidal excitation

8.4.3 Periodic Signals Response

Any periodic signal can be expanded using Fourier series expansion as a composite of summation of DC signal and sinusoidal signals (sines and cosines)

$$i(t) = a_o + \sum_{n=1}^{\infty} a_n \cos(n\omega_o t) \; + b_n sin(n\omega_o t), \tag{8.29}$$

where a_o represents the average of the applied signal (DC component) and a_n and b_n represent the amplitude of the sinusoidal signals with multiple frequencies. Substituting by (8.29) into (8.18), the instantaneous meminductance is given by

$$L_m(t) = \left(\sqrt{L_o} + k'_L\left(a_o t + \sum_{n=1}^{\infty} \frac{1}{n\omega_o}\left(a_n sin(n\omega_o t) + 2b_n sin^2\left(\frac{n\omega_o t}{2}\right)\right)\right)\right)^2. \tag{8.30}$$

The DC component is represented by a_o which causes the meminductor to saturate reaching one of its boundaries so the average number of periods where the meminductor saturates is given by:

$$N_{s1} = \frac{\sqrt{L_{bd}} - \sqrt{L_o}}{K'_L a_o T}. \tag{8.31}$$

where N_{sat} is the least integer function of N_{s1}. For example, we will apply this concept to the square wave signal in the following subsection.

8.4.3.1 Square Wave Signal Response

The meminductor is biased by a square wave signal which is defined by

$$i(t) = \begin{cases} i_{o1} & 0 < \tau < \alpha T \\ i_{o2} & \alpha T < \tau < T \end{cases}, \quad 0 < \alpha < 1 \tag{8.32}$$

where $\tau = t \mod(T)$, the applied signal alternates between positive and negative voltages with sharp transitions. By applying Fourier series expansion to the input signal, the coefficients are given by

$$a_o = \alpha i_{o1} + (1 - \alpha) i_{o2}, \tag{8.33a}$$

$$a_n = \frac{(i_{o1} - i_{o2})}{n\pi} \sin(2\alpha n\pi), \tag{8.33b}$$

$$b_n = \frac{(i_{o1} - i_{o2})}{n\pi}(1 - \cos(2\alpha n\pi)). \tag{8.33c}$$

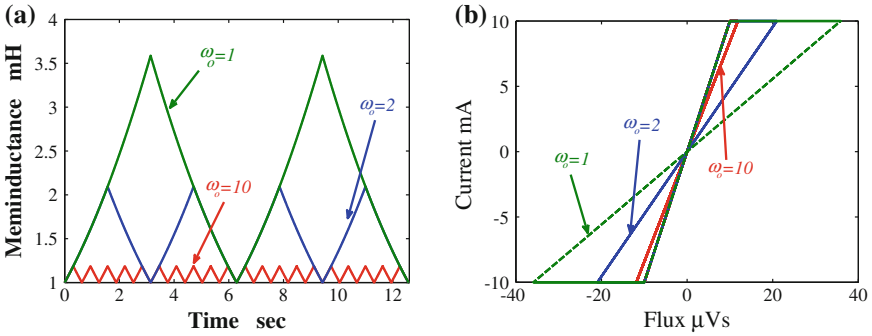

Fig. 8.7 Square wave response for different frequencies **a** instantaneous meminductance and **b** flux–current hysteresis

As obvious from (8.30), the DC term (a_o) leads to the saturation so the square wave signal shows two cases:

1. Zero DC component: which means that the accumulated charge after each period is zero so $\frac{i_{o1}}{i_{o2}} = \frac{\alpha-1}{\alpha}$ should be satisfied. Figure 8.7a shows the instantaneous meminductance under square wave input with i_{o1}, i_{o2} and α equal to 10 mA, −10 mA, and 0.5, respectively, where the meminductance increases and decreases depending on the sign of the applied current with nonlinear curves. Also its hysteresis curve is shown in Fig. 8.7b. The instantaneous meminductance expression can be written by using the behavior of the square signal where the discussed step response can be used periodically using the last value as the initial value of the next step. So the meminductance changes up and down as the current changes periodically which is given during any period by:

$$L_m(t) = \begin{cases} \left(\sqrt{L_o} + K'_L i_{o1}\tau\right)^2 & 0 < \tau < \alpha T \\ \left(\sqrt{L_o} + K'_L\left(i_{o1}\alpha T + i_{o2}(\tau - \alpha T)\right)\right)^2 & \alpha T < \tau < T \end{cases}. \tag{8.34}$$

2. Nonzero DC component: the accumulated charge, due to DC components, leads the meminductor to be saturated. Figure 8.8 shows that the instantaneous meminductance increases with time until it reaches the maximum meminductance L_{max} wherei_{o1}, i_{o2}, and α equal 10 mA, −10 mA, and 0.6, respectively. The meminductance reaches saturation after an average number of periods which is given by

$$N_{sat} = \frac{\sqrt{L_{bd}} - \sqrt{L_o}}{K'_L T(\alpha i_{o1} + (1-\alpha) i_{o2})}. \tag{8.35}$$

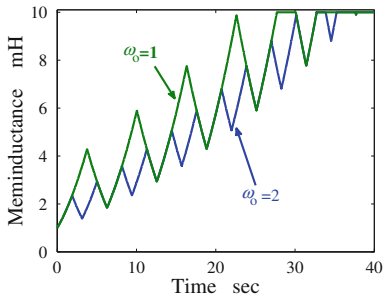

Fig. 8.8 Instantaneous meminductance for different frequencies under square wave signal with DC component

8.5 Memristor-Based Meminductor Emulator

Recently, many research articles are focused on the emulators as discussed in the previous sections. But, there is no significant research in the area of the meminductor emulator circuits. In this section, the meminductor emulator is built using a memristor and mutator to transform the memristor into a meminductor as shown in Fig. 8.9 [9, 11–13]. The relations of MR and ML are accomplished by linear transformation which is given by the following matrix:

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} sk_x & 0 \\ 0 & k_y \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \tag{8.36}$$

where k_x and k_y are real constants and their values depend on the mutator implementation. This linear transformation transforms (φ, q) into (ρ, q) which represents the constitutive relation of the meminductor. Such that the meminductance is given by

$$L_m = \frac{k_x}{k_y} R_m. \tag{8.37}$$

Since the memristor samples are not commercially available yet, thus we will use a memristor emulator instead of a solid-state memristor. Also this model is different than the previous emulator models so the emulator should be modified to fit this model. Recently, different memristor emulators were introduced showing good behavior [14, 15], however, the most practical one was introduced in [16] where the authors implemented and tested the emulator experimentally. Despite the fact that

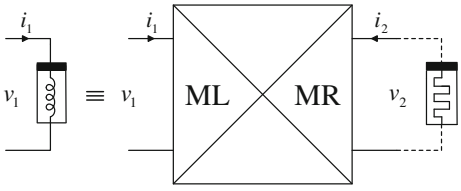

Fig. 8.9 Meminductor emulator block diagram

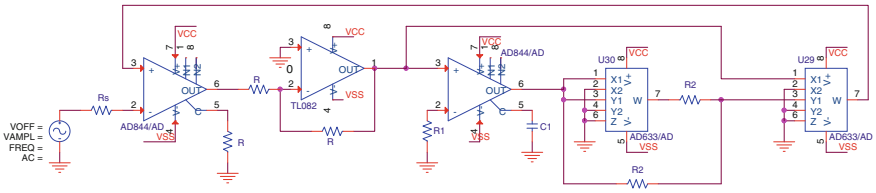

Fig. 8.10 Modified memristor emulator

this emulator is designed to model the memristance $R_m = R_s + kq(t)$, it should be modified to fit this model. To build a meminductor having the same discussed meminductance according to the previous equation, we need to build a memristor in which memristance is given by $R_m = \frac{k_y}{k_x} L_m$. Then by substituting with (8.18), the memristance should be

$$R_m = \frac{k_y}{k_x}\left(L_o + 2K'_L\sqrt{L_o}q(t) + K'^2_L q^2(t)\right). \tag{8.38}$$

Figure 8.10 shows the modified memristor emulator where the input current of the memristor i_{mr} is given by

$$i_{mr} = \frac{V_{mr} - V_{fb}}{R_s}. \tag{8.39}$$

The feedback voltage V_{fb} is given by

$$V_{fb} = \left(\frac{R^2}{20R_1C_1}q_{mr}(t) + \frac{R^3}{200R_1^2C_1^2}q^2_{mr}(t)\right)i_{mr} \tag{8.40}$$

By substituting into (8.39), the input voltage of the memristor V_{mr} is given by

$$V_{mr} = \left(R_s + \frac{R^2}{20R_1C_1}q_{mr}(t) + \frac{R^3}{200R_1^2C_1^2}q^2_{mr}(t)\right)i_{mr} \tag{8.41}$$

so the input memristance is

$$R_m = \left(R_s + \frac{R^2}{20R_1C_1}q_{mr}(t) + \frac{R^3}{200R_1^2C_1^2}q^2_{mr}(t)\right) \tag{8.42}$$

By comparing the coefficients in (8.42) and (8.38), the emulator parameters can be obtained where $R_s = \frac{k_y}{k_x}L_o$, $R = 8\frac{k_y}{k_x}L_o$ and $R_1C_1 = \frac{1.6L_o^{3/2}}{K'_L}$. Figure 8.11 shows the transient input current and input voltage; and I–V hysteresis of the memristor emulator under current excitation with $i(t) = 0.5\sin(200\pi t)$ mA where the circuit parameters are $R_s = 1\,\text{K}\Omega$, $R = 2\,\text{K}\Omega$, $R_1 = 0.5\,\text{K}\Omega$, $C_1 = 1\,\mu\text{F}$ and $R_2 = 1\,\text{K}\Omega$.

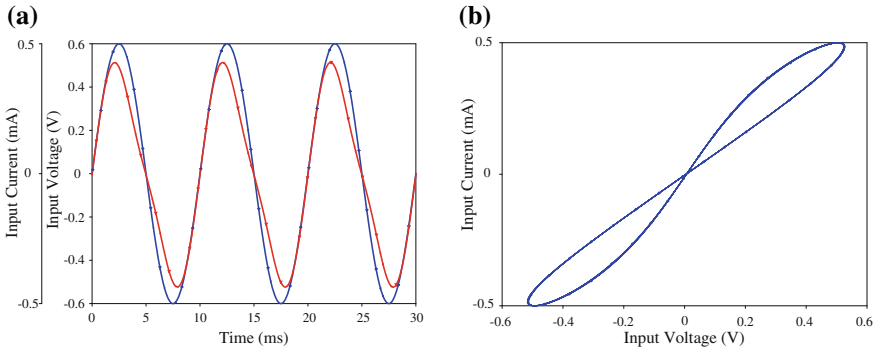

Fig. 8.11 Circuit model simulation of modified memristor's emulator **a** transient input current and voltage and **b** current–voltage hysteresis

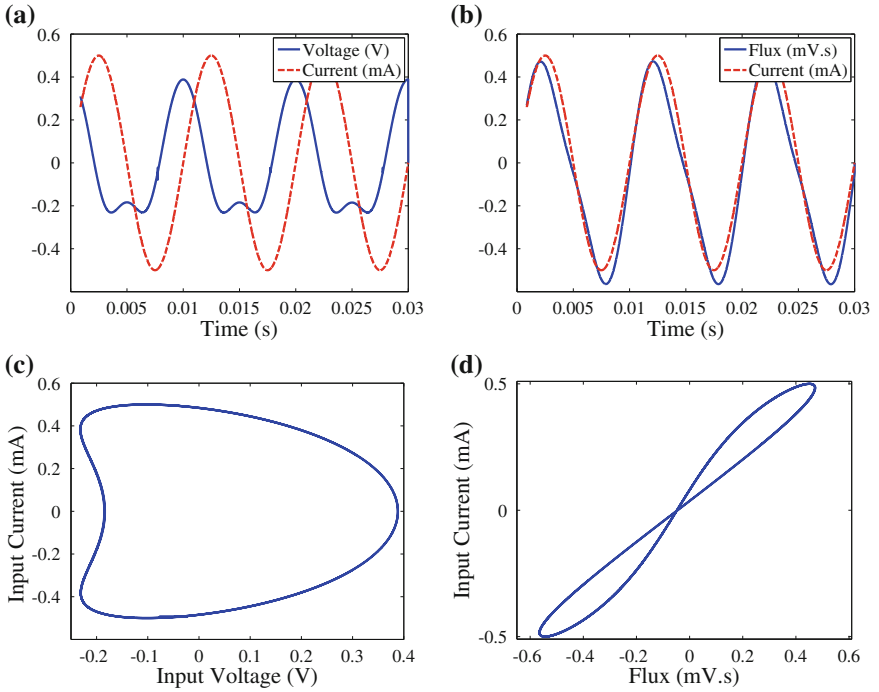

Fig. 8.12 Transient simulation results of meminductor emulator

The designed memristor emulator is connected to the mutator to obtain the complete realization of meminductor emulator where k_x and k_y are equal to 0.001 and 1, respectively. Figure 8.12a, b show a transient simulation of the meminductor current I_{ml}, Voltage V_{ml}, and flux φ_{ml}, moreover, Fig.8.12c, d show I–V hysteresis and I–φ hysteresis, respectively.

8.6 Memristor-Less Meminductor Emulators

Recently, a simple symmetrical double-loop hysteresis behavior of mem-elements can be obtained with the following modeling equation, proposed in [16].

$$Y(t) = X(t)\left(a + k\int_0^t X(\tau)d\tau\right), \tag{8.43}$$

where $X(t)$ is the normalized control signal, $Y(t)$ is the normalized dependent signal, a and k are scaling constants.

Figure 8.13 shows the hysteric relation between X and Y for $a = k = 1$ and $X(t) = sin(2\pi ft)$. It is obvious that the hysteresis loop shrinks with increasing the frequency and the slope tends to the initial value a which is the main property in the mem-elements (for more details review Chap. 3). In case of the meminductor, a pinched hysteresis should exist between flux and current as discussed in (8.1) and (8.2). Therefore in current-controlled meminductor, $X(t)$ and $Y(t)$ represent the current and the flux, respectively. So, (8.1) is reduced to:

$$\varphi(t) = \left(a + k\int_{t_o}^t i(\tau)d\tau\right)i(t) \tag{8.44}$$

Therefore, the meminductance L_m can be written as

$$L_m = a + k\int_0^t i(\tau)d\tau = a + kq(t) \tag{8.45}$$

where a represents the initial meminductance (L_o) assuming zero initial charge ($q(0) = 0$). The previous equation represents a first-order model of current-controlled meminductor which can be generalized to higher order model by adding higher order terms of charge $q(t)$. Figure 8.14 shows the hystereses of the current-controlled meminductor with $a = 1\,\text{mH}$ and $k = 100\,\text{H/C}$ for applying sinusoidal

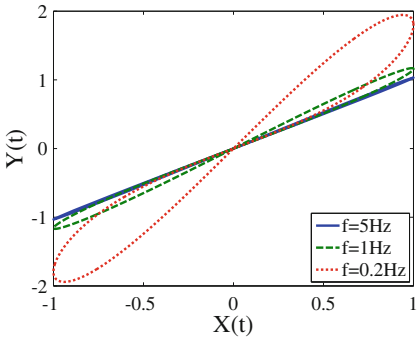

Fig. 8.13 Hysteresis relation between X–Y for different frequencies

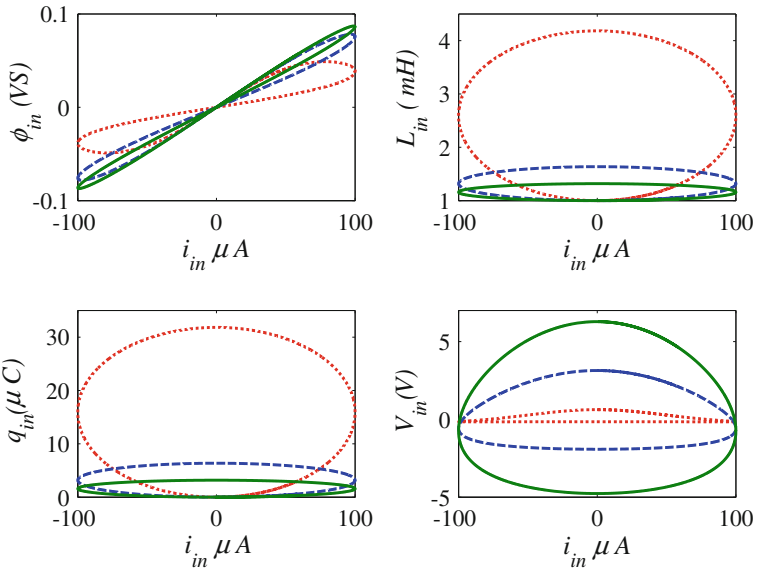

Fig. 8.14 Numerical simulation of current-controlled meminductor.

current input with amplitude 100 μA and frequencies 1 Hz(*Red*), 5 Hz(*Blue*), and 10 Hz(*Green*), where the hysteresis loops shrink by increasing the applied frequency. Therefore, the I–V is not a circle for low frequencies due to the nonlinear relation. But for the high frequencies, the I–V plot becomes a circle.

In case of applying a sinusoidal signal to the meminductor, the meminductance spans between two values: maximum and minimum achievable meminductances and the difference is inversely proportional to the applied frequency. Figure 8.15 shows

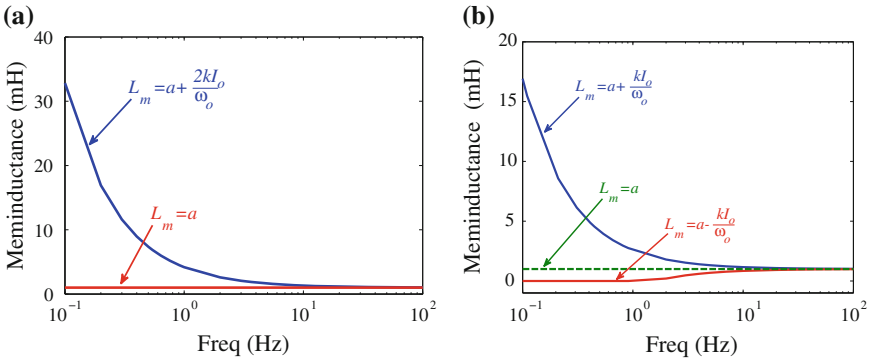

Fig. 8.15 Maximum and minimum achievable meminductance for **a** sin input signal and **b** cos input signal

the maximum and minimum for the meminductance for $a = 1\,\text{mH}$, $k = 100\,\text{H/C}$, and $I_o = 100\,\mu\text{A}$, where the meminductance changes between $[a, a + 2kI_o/\omega]$ and $[a + 2kI_o/\omega, a + 2kI_o/\omega]$ in case of *sin* and *cos*, respectively.

Similarly, the flux-controlled meminductor model can be deduced by setting $X(t) = \varphi(t)$ and $Y(t) = i(t)$. So the current–flux relation and inverse meminductance are given by:

$$i(t) = \left(a + k\int_{t_o}^{t} \varphi(\tau)d\tau\right)\varphi(t) \tag{8.46a}$$

$$L_m^{-1} = a + k\int_{0}^{t} \varphi(\tau)d\tau = a + k\rho(t) \tag{8.46b}$$

where ρ represents the time integral of the flux assuming zero initial conditions. Figure 8.16 shows the hystereses of the flux-controlled meminductor with $a = 1000\,\text{H}^{-1}$ and $k = 10\,\text{G H}^{-1}\text{V}^{-1}\text{S}^{-1}$ by applying sinusoidal current input with amplitude $100\,\mu\text{A}$ and frequencies $1\,\text{Hz}$(*Red*), $5\,\text{Hz}$(*Blue*), and $10\,\text{Hz}$(*Green*).

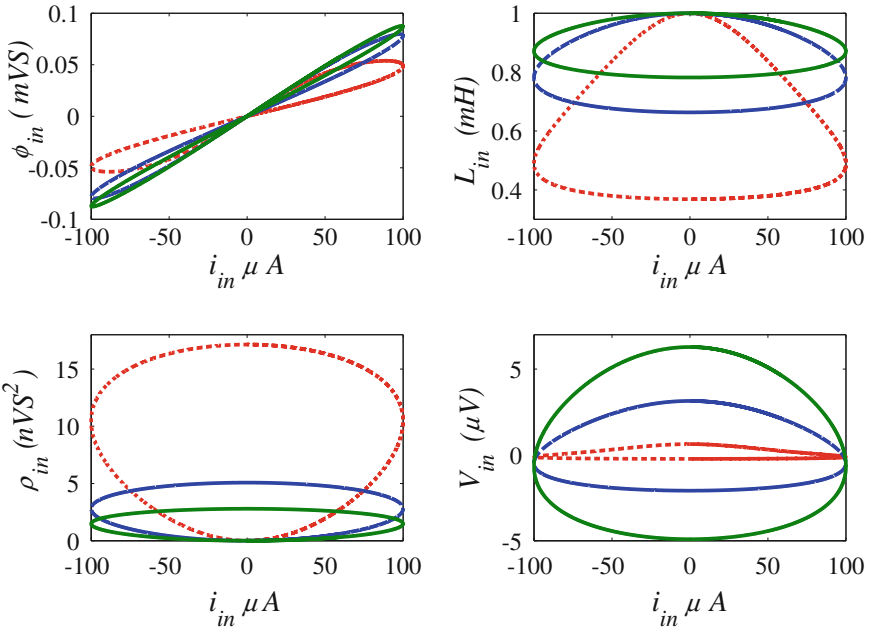

Fig. 8.16 Numerical simulation of flux-controlled meminductor

8.6.1 Circuit Realization of Meminductor Emulator

In order to realize the implicit relation between the flux and the current of current-controlled meminductor given in (8.44), a voltage–current relation should exist to make it easier for implementation. The implicit relation of flux–current which should be realized is given by:

$$\varphi(t) = (L_o + kq(t))i(t) \tag{8.47}$$

As known, the voltage is the time derivative of the flux so the voltage–current implicit relation is given as

$$V_{in}(t) = \frac{d}{dt}\left(\Big(L_o + kq(t)\Big)i(t)\right) \tag{8.48}$$

As obvious from the previous equation, we need to calculate the charge and then multiply it with the current. Therefore, the input current is mirrored and imposed in R (through CCII+) creating $V_x = i_{in}R$ which is integrated with gain $1/(R_1C_1)$ and multiplied by V_x as shown in Fig. 8.17. The output voltage is summed with V_x creating V_y which is given by:

$$V_y = \left(1 + \frac{\alpha}{R_1C_1}\int_0^t V_x(\tau)d\tau\right)V_x \tag{8.49}$$

where α is the multiplier gain. The voltage V_y is differentiated creating the feedback voltage V_{fb} which is mirrored to terminal X of the CCII+ creating the input voltage $V_{in} = V_{fb}$ which is given by

$$V_{in} = R_2C_2\frac{d}{dt}\left(\left(R + \frac{\alpha R^2}{R_1C_1}q(t)\right)i_{in}\right) \tag{8.50}$$

By comparing the previous equation with (8.48), $L_o = RR_2C_2$ and $k = \alpha\frac{R_2C_2}{R_1C_1}R^2$.

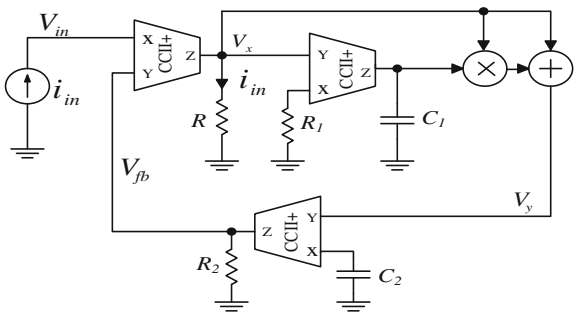

Fig. 8.17 Circuit schematic of current-controlled meminductor emulator

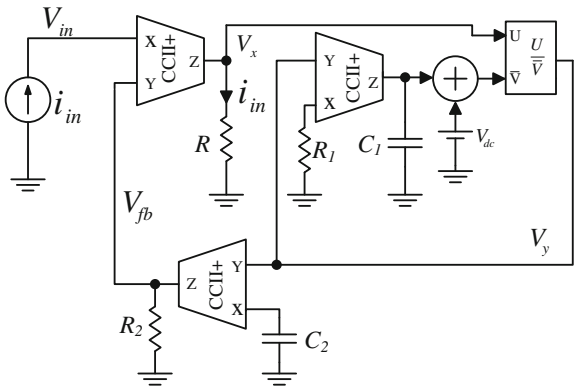

Fig. 8.18 Circuit schematic of voltage-controlled meminductor emulator

Similarly, for the voltage-controlled meminductor, the voltage–current relation is given as follows:

$$V_{in}(t) = \frac{d}{dt}\left(\frac{i(t)}{a + k\rho(t)}\right) \tag{8.51}$$

As in the flux-controlled case, the input current is mirrored and imposed in R creating $V_x = i_{in}R$. Then V_x is divided by a voltage V_y which is obtained from summing a constant voltage V_{DC} and the time integral of V_y such that

$$V_y(t) = \frac{V_x(t)}{a + k\int_0^t V_y(\tau)d\tau} \tag{8.52}$$

where V_y represents the accumulated flux which is differentiated to generate the input voltage V_{in}. Figure 8.18 shows the circuit which emulates the behavior of the voltage-controlled meminductor and then the voltage–current relation is given by:

$$V_{in}(t) = R_2C_2\frac{d}{dt}\left(\beta\frac{i(t)R}{V_{dc} + \frac{1}{R_1C_1}\rho(t)}\right) \tag{8.53}$$

where β is the divider gain. By comparing the previous two equations, $a = V_{dc}/(\beta RR_2C_2)$ and $k = 1/(\beta RR_1R_2C_1C_2)$.

8.6.2 Circuit Validation

The current-controlled meminductor emulator is assembled using AD844 as CCII+ and AD633 as a multiplier with gain $\alpha = 0.1$ and summer with $R = 500\Omega$, $R_1 = R_2 = 1\,\mathrm{K}\Omega$, $C_1 = C_2 = 100\,\mathrm{nF}$ and sinusoidal current input with amplitude $100\,\mu\mathrm{A}$

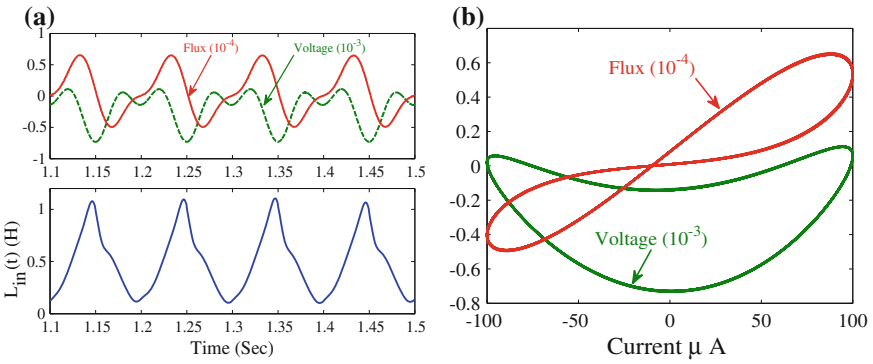

Fig. 8.19 PSPICE simulations of current-controlled emulator **a** flux, voltage, and meminductance; and **b** V–I and ϕ–I hystereses

and frequency 10 Hz. Figure 8.19a shows the transient input voltage V_{in}, flux φ, and the input meminductance L_{in}. Figure 8.19b shows the current–voltage and current–flux hysteresis of the current-controlled meminductor showing the pinched double loops hysteresis. Due to the nonidealities of the used integrated circuits (ICs), the hysteresis loops are not full symmetric.

Similarly, the flux-controlled meminductor emulator is verified using SIMULINK which gives similar simulation results as Fig. 8.16 which can be assembled using AD844 and AD734 as a divider.

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Appendix A
Memristor, Memcapacitor, and Meminductor

A.1 Memristor

The first SPICE model of the memristor was proposed by Biolek et al. [1] where the effect of boundary is taken into consideration using Joglekar and Biolek window functions [2].

```
.SUBCKT memristor Plus Minus PARAMS:
+ Ron=1K Roff=100K Rinit=80K D=10N uv=10F p=1
**********************************************
* DIFFERENTIAL EQUATION MODELING *
**********************************************
Gx 0 x value={ I(Emem) *uv*Ron/D^2*f (V (x) ,p) }
Cx x 0 1 IC={(Roff-Rinit) / (Roff-Ron) }
Raux x 0 1T
* RESISTIVE PORT OF THE MEMRISTOR *
******************************
Emem plus aux value={-I (Emem) * V (x) * (Roff-Ron) }
Roff aux minus {Roff}
**********************************************
*Flux computation*
**********************************************
Eflux flux 0 value={SDT (V(plus,minus) ) }
**********************************************
*Charge computation*
**********************************************
Echarge charge 0 value={SDT (I (Emem) ) }
**********************************************
* WINDOW FUNCTIONS
* FOR NONLINEAR DRIFT MODELING *
**********************************************
*window function, according to Joglekar
.func f(x,p)={1-(2*x-1)^(2*p)}
*proposed window function
;.func f(x,i,p)={1-(x-stp(-i) )^(2*p) }
.ENDS memristor
```


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DOI 10.1007/978-3-319-17491-4

A.2 Memcapacitor

SPICE model of the memcapacitor was introduced in [3]

```
.SUBCKT memC Plus Minus PARAMS:
+ Cmin=10nF Cmax=10uF Cinit=100nF k=10meg p=1 IC=0
**********************************************
* Input port *
**********************************************
Emc Plus Minus value={DM(v (x)) (v(charge)  +  ICCinit)}
**********************************************
* Charge computation.
**********************************************
Gq 0 charge value={I(Emc)}
Cq charge 0 1
Rq charge 0 1G
**********************************************
* State-space equation
**********************************************
.param xinit {(1/Cinit-1/Cmax) / (1/Cmin-1/Cmax)}
Gx 0 x value={v (charge) kwindow (v (x) ,p)};
Cx x 0 1 IC={xinit}
Rx x 0 1G
.func DM(x)={1/Cmax + (1/Cmin-1/Cmax) *x};
.func window (x,p)={1-(2*x-1)**(2*p)}; window function
.ENDS memC
```

A.3 Meminductor

The only SPICE model of the meminductor was introduced by Biolek et al. [4]

```
.SUBCKT memL Plus Minus PARAMS:
+ Lmin=1mH Lmax=20mH Linit=5mH k=10 p=10 IC=0
**********************************************
* Input port *
**********************************************
Vsense Plus + 0 V; sensing of the meminductor current
Gml + Minus value={(V(flux)+IC*Linit)/LM(V(x))};
**********************************************
*Flux computation via time-domain integration of meminductor voltage*
**********************************************
Gflux 0 flux value={V(plus,minus)}
Cflux flux 0 1
Rflux flux 0 1G
.param xinit {(sqrt(Linit)-sqrt(Lmin))/(sqrt(Lmax)-sqrt(Lmin))}
Gx 0 x value={I(Vsense)*k*windowJ(V(x),p)}; Joglekar window,
;Gx 0 x value={I(Vsense)*k*windowB(V(x),I(Vsense),p)}; Biolek window
Cx x 0 1 IC={xinit}
Rx x 0 1G
**********************************************
*Functions for defining meminductance and boundary effects
**********************************************
```

```
.func LM(x)={(sqrt(Lmin)+x*(sqrt(Lmax)-sqrt(Lmin)))^2};
.func windowJ(x,p)={1-(2*x-1)^(2*p)}; Joglekar window,
.func windowB(x,xd,p)={1-(x-stp(-xd))^(2*p)}; Biolek window
*******************************************
*Computing charge and time-domain integral of flux (TIF)
*******************************************
Gcharge 0 0 value={SDT(I(Vsense))}
Gintflux 0 0 value={SDT(V(flux))}
.ENDS memL
```

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