S. D. Brotherton

Introduction to Thin Film Transistors

Physics and Technology of TFTs

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Preface

Thin film transistors, TFTs, are now fundamental electronic components in virtually all consumer and professional display products, from smart phones to large diagonal, flat panel TVs. The commercial application of TFTs has been driven by the use of hydrogenated amorphous silicon, a-Si:H, which is the workhorse of the industry. However, a greater range of TFT materials, such as polycrystalline silicon, amorphous oxide semiconductors and organic semiconductors, are now commanding interest, and this book has been written as an accessible introduction to the field. Whilst there are a number excellent books aimed at the specialist working with these individual materials, this book was conceived to meet the needs of a less specialist audience. The book was written for a target audience including undergraduate and postgraduate students taking display-related courses, postgraduate and new researchers to the field, engineers supplying equipment to the flat panel display industry, researchers in one specialist TFT field looking for an overview of another and technical managers within the FPD industry.

Whilst some familiarity with the background physics of semiconductor device operation has been assumed, the book is intended to be self-contained, with introductory chapters covering the device physics concepts needed to follow the later chapters on the TFTs themselves. These introductory chapters deal with band bending effects at semiconductor surfaces, electron-hole pair generation and recombination and the operation of classical MOSFET devices. A further chapter covers the operation of active matrix displays.

This book has grown principally out of a series of lectures on TFT technologies given to an Italian research consortium, and which incorporated material from specialist lectures on active matrix displays and TFTs presented in Masters courses at Southampton and Dundee Universities.

It is a pleasure to acknowledge the contribution made by the referees with their insightful and helpful comments, and these have undoubtedly improved the book. In addition, colleagues and other contacts within the research community have generously responded to my requests for background information and access to published material. These have included Dr. G. Fortunato (CNR-IMM, Rome),

Prof. G. J. Parker (Southampton University), Dr. J. R. Ayres, Dr. N. D. Young and Dr. M. J. Trainor (Philips Research), Prof. J. M. Shannon and Dr. R. Sporea (Sussex University), Dr. Wen-yi Lin (AU Optronics Corp), Prof. R. B. Wehrspohn (Fraunhofer Institute for Mechanics of Materials), Dr. R. Paetzel (Coherent GmbH) and Prof. M.-K. Han (Seoul National University). I am also indebted to Tom Spicer of Springer for his help and guidance during the preparation of the book.

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Biographical Information

Dr. Stan D. Brotherton started his research career at the GEC Hirst Research Laboratory, England, before taking a post-doctoral Research Fellowship at Southampton University in 1971. From there he moved to the Philips Research Laboratory, Redhill, England, where he was a Senior Principal Scientist, and he now works as an independent TFT Consultant.

He has led a wide range of research projects investigating semiconductor devices, and related materials issues, particularly the influence of deep level defects on the performance of Si devices. The devices studied have included MOSFETs and CCDs, power devices, and IR imaging devices. His most recent field of activity was thin film transistors, within which he initiated the Philips research programme on poly-Si TFTs. Activity within this field has continued with consultancy contracts from a number of international organisations.

He has published $\sim$120 papers on the physics and technology of silicon devices, and in 1989 was awarded a DSc by London University for published work on deep level defects in silicon. Amongst the later publications, $\sim$65 have been on poly-Si TFTs. He also contributed a chapter on this topic to the Springer Handbook of Visual Display Technology, and was a member of the Editorial Board for that book. He has presented numerous invited and contributed papers at major international conferences, and has been a contributor of specialist TFT lectures on the DisplayMasters course at Dundee University.

Chapter 1
Introduction

This book reviews the operation, technology and application of the main classes of thin film transistor (TFT), which are of current interest in the field of large area electronics. The major application area is flat panel, active matrix liquid crystal displays, AMLCDs, and, with the range of screen diagonals currently available, this is the most ubiquitous and successful display technology to date. Screen sizes from 1 inch to more than 100 inches dominate applications in most areas of life, from small, portable mobile phone displays, through medium-sized tablets, net-books and lap-tops, to large-screen monitors and HD televisions.

In the 1960s, there was early work into a variety TFT materials and applications, and an engaging and personal account of that work has been given by Brody [1, 2], who was a pioneer of both TFTs and active matrix displays. However, the present interest in thin film transistors can be dated back to the research of Spear and Le Comber [3, 4] in the mid-1970s. They showed that glow discharge hydrogenated amorphous silicon, a-Si:H, had a low enough trap state density that it could be doped, and used in thin film transistor structures. This stimulated world-wide research and development of the a-Si:H TFT, and led to its application in active matrix liquid crystal displays.

From the first, small scale AMLCD production facilities in the late 1980s, processing A4-sized glass plates, to the current 10th generation plant, processing $2.85 \times 3.05\ m^2$ glass plates, the panel industry has grown, on average, by more than 10 % per year to a turn-over of approximately $B86 in late 2011 [5]. Whilst AMLCDs continue to dominate the current product range in terms of volume, other display media are now appearing. These are electro-phoretic displays, EPDs, for e-readers, and organic light emitting diode, OLED, displays for smart phones, and which are predicted to be of longer-term interest for TV.

To cover this field, and to make it accessible to students and new researchers, the layout of this book is organised into three sections: Part I—Background, Part II—TFTs, and Part III—Novel Substrates and Devices. The contents of these sections progress from basic semiconductor physics to speculative new materials and device structures. In the introductory Part I, Chaps. 2 and 3 contain the background device physics to TFT operation, and Chap. 4 describes the operation

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of active matrix displays. Part II, containing Chaps. 5–10, describes the technology and device physics of the major classes of TFT, which are of current interest in the field of large area electronics. These are:

- Hydrogenated amorphous silicon (a-Si:H), which forms the basis of the AM-LCD industry,
- Poly-crystalline silicon (poly-Si), which facilitates the integration of electronic circuits into flat panel displays. Cost considerations limit this application to small diagonal LCDs, whilst the high drive current of these devices favours their application to small AMOLED displays,
- Transparent amorphous oxide semiconductors, of which indium-gallium-zinc oxide is the most studied example. These newer materials are attracting much interest as they have considerably higher carrier mobility than a-Si:H, but, due to their amorphous nature, are expected to have comparable excellent uniformity. Their projected applications are to large diagonal, high resolution AM-LCD TVs [6], and, in the longer term, to AMOLED TVs [6],
- Organic semiconductors. In the preferred implementation, these TFTs contain organic materials for both the semiconductor and the gate dielectric layers. They are currently low carrier mobility devices, but can be produced by low temperature solution-processing, including printing, and are seen as a cost-effective route to flexible electronics on polymer substrates.

The majority of TFT production is based upon the use of rigid, glass substrates, and, in Part III, Chap. 11 reviews the properties and constraints of polymer substrates, and gives an overview of the strategies used to fabricate TFTs on flexible materials. Finally, Chap. 12 introduces a new type of TFT, the source-gated transistor, SGT. This has markedly different characteristics from conventional TFTs, and may be an interesting vehicle for achieving improved performance from low-mobility disordered materials, including organic semiconductors.

Irrespective of the display medium (whether it is LCD, EPD or OLED), the operation of the display itself is dependent upon the presence of an active matrix of TFTs to address and drive the individual pixels in the display. The TFTs are field effect transistors, FETs, whose operation is akin to the semiconductor industry metal–oxide–semiconductor transistor, the MOSFET. Hence, as an introduction to the TFT field, Chaps. 2 and 3 deal with the fundamentals of FET operation. In particular, Chap. 2 introduces some basic semiconductor physics topics, which underpin the operation of TFTs. This includes the bending of the semiconductor energy bands, and the change in free carrier concentration at the semiconductor surface, in response to an orthogonally applied electric field. The relationships are derived analytically for a single crystal substrate, and these expressions are then used as reference points in later chapters to clarify the changes needed to describe TFT behaviour. The other topic covered is electron–hole pair recombination and generation, and these are processes governing non-thermal equilibrium effects in TFTs, such as photoconductivity and leakage currents. Whilst most practical TFT analysis makes use of 2-D numerical modelling packages, an analytical approach is used here in order to illustrate the underlying physics. However, the relevant

equations for device simulation are summarised, so that the reader has a better appreciation of the background to the many publications reporting 2-D device simulation results.

Chapter 3 takes a similar analytical approach in describing the operation of the simple, long-channel MOSFET, with the aim of demonstrating the basic physics behind its operation. Again, these analytical concepts are used in the later chapters dealing with TFTs, as the fundamental physics are the same, and the equations are universally used to extract key performance parameters from all classes of TFT. The equations have the merit of simplicity and ease of use, and their limitations are discussed in the individual TFT chapters.

Chapter 4 describes the basic operation of active matrix displays, and, in particular, the role of the TFT as a switch and storage element within each pixel of the display. There is also a discussion of pixel layout considerations, and of their impact upon display performance. Although the emphasis in this chapter is on liquid crystal displays, an overview of the operation of electro-phoretic and OLED displays is also included.

The most widely employed transistor throughout the industry, and across the application range, is the hydrogenated amorphous silicon, a-Si:H, TFT, whose technology and performance details are described in Chaps. 5 and 6, respectively. Chapter 5 describes the architecture and fabrication of a-Si:H TFTs, whilst Chap. 6 deals with some of the performance issues of these devices. Of these, one extensively studied topic is gate bias stress instability, which is a fundamental effect related to the meta-stability of the defect concentration within the material. The chapter also includes a brief discussion of two other meta-stability effects in a-Si:H, which are associated with impurity doping and optical illumination.

At the time of writing, the only other TFT material in mass production is poly-Si, and Chaps. 7 and 8 deal with the technology and performance of these devices, respectively. In Chap. 7, the fabrication processes for poly-Si are reviewed, and the currently preferred process of laser crystallisation is discussed in more detail. These devices have a coplanar, self-aligned architecture, which is quite different from the other TFTs, and is much more similar to single crystal silicon devices. The characteristics of poly-Si TFTs are discussed in Chap. 8, and, indeed, the performance of high quality poly-Si devices is also closer to crystalline Si MOSFETs than to the alternative, contemporary TFTs. This chapter includes a review of device performance issues, many of which are related to the high electrostatic field at the drain junction, resulting in field-enhanced leakage currents and hot carrier instabilities.

Chapters 9 and 10 cover the emerging TFT technologies of transparent amorphous oxide semiconductors, and organic semiconductors, respectively. These are not yet in mass production, although initial products, employing each of these device types, have been predicted to appear in 2012 [6–8]. Both chapters discuss the fabrication and performance of devices made in these two types of material, although the content in Chap. 10, on organic materials, is notably different from the preceding chapters. Whereas the other chapters have focussed on one material, there is a plethora of different organic compounds, which have been engineered for

application to both the semiconductor layer and to the gate dielectric layer. In addition to the variety of materials, in many cases there is also a variety of alternative deposition procedures, ranging from vacuum deposition to solution processing, and printing. At the moment, there is not a consensus on the most favoured organic semiconductor materials, and the situation is further complicated by a trade-off between device performance and the ease of material deposition. Chapter 10 contains an overview of the materials of current interest, together with their different deposition procedures, and reviews the performance issues of these devices.

Chapter 11 discusses the challenges in changing from a rigid, glass substrate technology to one utilising a flexible substrate, which, ideally, would be a low cost polymer material. These materials present many handling issues, including reduced temperature processing, dimensional instability, and have coefficients of thermal expansion which are a poor match to the materials used in the inorganic TFT technologies. However, given the maturity of the a-Si:H and poly-Si fabrication technologies, a variety of routes has been explored in order to integrate them into a flexible substrate process. These approaches, including the impact of substrate bending on device characteristics, are reviewed for both the inorganic and the organic TFT technologies.

A new device structure, the source-gated transistor, SGT, is presented in Chap. 12. This is a thin-film FET, having an inverted staggered TFT architecture, but with an injection barrier at the source junction. The height of this barrier is controlled by the gate and drain biases, and the reported device characteristics are remarkably different from those of conventional TFTs. In particular, the SGT has a reduced saturation voltage, higher output impedance, reduced short channel effects, and the drain current is insensitive to modest variations in the source-drain separation. The physics of its operation are presented, and its behaviour is compared with staggered organic TFTs, which have the closest equivalent architecture. As a relatively new device, the detailed understanding of its operation was still developing at the time of writing, and further refinements may emerge in due course.

The TFT field continues to be characterised by burgeoning activities in both research and product development. New display media, such as OLEDs, are expected to become more widespread, and the pixels may well be driven by new TFT technologies, such as amorphous oxide semiconductors [8]. In addition, new products, such as flexible displays, are forecast to appear in the near-future, and organic TFTs are expected to play a major role in this area. These developments will broaden and extend the current technology range, and will further enhance the ubiquity of flat panel display products.

This introductory book on TFTs is complementary to the established books in the field, where a particular TFT technology (which is covered by just one or two chapters here) warrants a book in itself, and is aimed at the specialists in that field. In contrast, this book is designed to be an accessible introduction to TFTs, and is aimed at undergraduate teaching courses, post-graduate and new researchers to the

field, engineers supplying equipment to the flat panel display industry, researchers in one specialist TFT field looking for an overview of another, and technical managers within the FPD industry.

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Part I
Background

Chapter 2
Semiconductor Device Physics for TFTs

Abstract Two device physics topics are discussed in this chapter, namely, surface band bending and surface charges in the metal–insulator–semiconductor, MIS, structure, and electron-hole pair recombination/generation processes. The treatment of the MIS structure covers the relationship between the voltage on the metal gate, the induced surface charge in the semiconductor and the resulting surface potential. This is treated analytically, using single crystal equations, and the relationships are fundamental to the understanding of IGFET operation. Equally, the concepts are widely employed in analysing TFT behaviour. The electron-hole pair generation process underlies the leakage current behaviour of many semiconductor devices, and can be applied to the analysis of TFT off-state behaviour. The recombination process determines steady state carrier concentrations under injection conditions, such as optical illumination. Finally, there is a brief discussion of carrier flow in semiconductor devices, including the equations used in numerical simulation packages.

2.1 Introduction

In this chapter, device physics topics are introduced, which are relevant to TFTs, and for following the discussion in later chapters. The emphasis is on background understanding of basic device physics principles, and an analytical approach is followed, using single crystal semiconductor equations. These concepts and equations are modified in later chapters for the more complex situation of the non-single crystal TFT materials.

The first topic presented deals with semiconductor surface physics, focussing on band bending and surface charge in the metal–insulator–semiconductor, MIS, system. This underlies the relationship between the voltage on the metal gate and the induced charge in the semiconductor surface, and introduces the concepts of the flat band voltage and the threshold voltage for surface inversion. The most widely studied semiconductor/insulator interface is the c-Si/SiO_2 interface, and the numerical examples given are based upon this system, although the equations

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themselves are quite general. In Chap. 6, these surface space charge equations are re-formulated to include the U-shaped density of states functions found in a-Si:H and other TFT materials, and the influence of these extra states is compared to the simpler situation discussed in this chapter.

The second topic is electron-hole pair generation and recombination. These are basic processes underlying both leakage current effects, and steady state carrier densities in devices under injection conditions, such as optical illumination. Finally, there is a brief discussion of carrier flow and the coupled field/space charge equations, which need to be solved in order to calculate the current–voltage characteristics of a device.

Much current research into device behaviour makes use of commercial device simulators to solve these latter equations. These simulation packages give a deeper insight into device behaviour by relating its current–voltage characteristics to internal field and carrier distributions. However, in published work, the fundamental equations are rarely listed. In the final Sect. 2.4, of this chapter, those equations are presented, and they are built up from the material in the preceding sections of the chapter (but, the numerical techniques used for the solution of the equations go beyond the scope of this book).

As is apparent, the range of device physics topics covered here is limited, and, for a broader coverage of this field, there are many excellent books available, such as Sze and Ng [1]. Examples of device simulation packages can be found in Refs. [2, 3], as well as a discussion of the numerical solution techniques in [2].

Some of the key simplified equations, from Sects. 2.2 and 2.3, are listed in the Appendix. These are useful for cross-reference purposes in later chapters, and also for direct, analytical calculations.

2.2 Semiconductor Surface Physics

2.2.1 Ideal MIS Capacitor and Surface Band Bending

Figure 2.1a shows the band diagram of an ideal MIS capacitor, on a p-type substrate, in which the Fermi levels in the metal and in the semiconductor perfectly align, such that there is no induced band bending within the structure (In Sect. 2.2.3, a more realistic situation will be discussed, in which there are work function differences between the metal and the semiconductor, and the semiconductor interface contains interface trapping states). In the treatment below, the following conventions will be used: the Fermi potential, V_F, will be measured from the bulk intrinsic level, E_i, and will be taken as positive beneath E_i and negative above it. Similarly, the band bending, V_s, will be measured from the bulk intrinsic level, and the polarity convention will be the same as used for V_F.

When a positive charge, Q_G, is placed on the metal gate, it will induce an equal and opposite negative charge in the semiconductor, Q_s, and this negative charge

will consist of an increase in the electron density and a decrease in the free hole density, thereby, leaving behind immobile, ionised acceptor centres, N_a. In order to accommodate these changes in free carrier density, the bands within the semiconductor will have to bend downwards near its surface, as shown in Fig. 2.1b. It will also be seen that the positive charge on the gate results from a positive bias being applied to the gate relative to the semiconductor. Following the convention discussed above, the Fermi level in the metal is moved downwards in response to the positive gate bias, V_G, and the semiconductor surface potential is $+V_s$. The situation shown in this diagram is for a small positive potential on the gate, such that the surface electron density, n_s, is small compared with N_a, and the surface is said to be *depleted* (of free holes). For a larger positive gate bias, the situation shown in Fig. 2.1c occurs. In this case, there is a corresponding increase in band bending, V_s, and the free electron concentration at the surface is larger than N_a: the surface is now said to be *inverted.* Between these two situations, when the band bending, $V_s = V_F$, the surface will be intrinsic, and $n_s = p_s = n_i$. Further positive

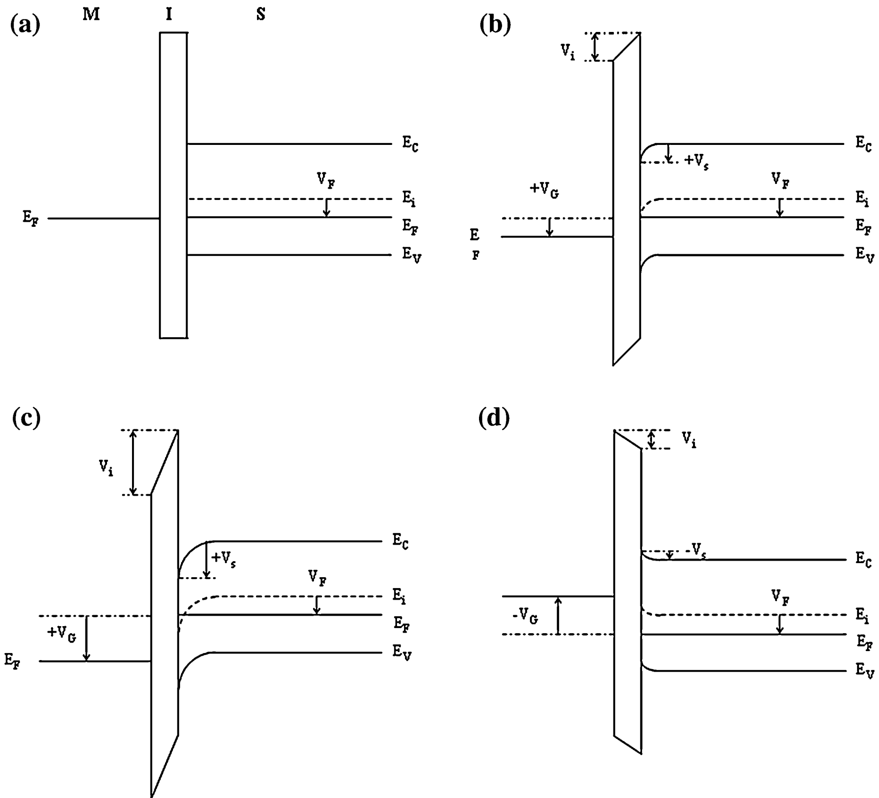

Fig. 2.1 Ideal metal–insulator–semiconductor, MIS, band diagrams, showing different surface charge conditions for a p-type substrate: **a** flat bands, **b** hole depletion, **c** electron inversion, and **d** hole accumulation

band bending beyond this point will lead to $n_s > p_s$. Finally, as shown in Fig. 2.1d, with a negative bias applied to the gate, there is an increase in positive charge induced in the semiconductor, due to an increase in the free hole density. This is associated with the bands bending upwards by an amount $-V_s$. In this case, the surface is said to be *accumulated*. With an n-type substrate, the opposite situation occurs, in that a negative gate bias will cause the surface to be depleted/inverted rather than accumulated, and a positive bias will cause surface accumulation.

To establish the relationship between V_s, and Q_s and V_G, it is necessary to solve Poisson's equation, where:

$$\frac{d^2V}{dx^2} = -\frac{q\rho(x)}{\varepsilon_0\varepsilon_s} \tag{2.1}$$

ε_0 is the permittivity of free space, ε_s is the dielectric constant of the semiconductor, and the space charge density, ρ(x) is:

$$\rho(x) = p(x) - n(x) - N_a \tag{2.2}$$

The free carrier densities are defined by the intrinsic carrier concentration, n_i, and the separation of the Fermi level from the intrinsic level, i.e.:

$$\begin{aligned} p(x) &= n_i \exp\frac{q(V_F - V)}{kT} \\ n(x) &= n_i \exp\frac{-q(V_F - V)}{kT} \end{aligned} \tag{2.3}$$

$$p(x) - n(x) = 2n_i shq(V_F - V)/kT \tag{2.4}$$

Where T is the temperature, and k is Boltzmann's constant. At the surface, $V = V_s$, and in the bulk, where $V = 0$:

$$p_0 = n_i \exp\frac{qV_F}{kT} \text{ and } n_0 = n_i \exp\frac{-qV_F}{kT}$$

From charge neutrality,[1]

$$p_0 - n_0 = N_a = 2n_i shqV_F/kT \tag{2.5}$$

$$\frac{d^2V}{dx^2} = -\frac{2n_iq}{\varepsilon_0\varepsilon_s}\left[sh\frac{q(V_F - V)}{kT} - sh\frac{qV_F}{kT}\right] \tag{2.6}$$

Using $\frac{d^2V}{dx^2} = \frac{1}{2}\frac{d}{dV}\left(\frac{dV}{dx}\right)^2$, and integrating Eq. 2.6 from the bulk ($V = 0$, and $dV/dx = 0$) to the surface ($V = V_s$, and $dV/dx = -F_s$):

[1] $V_F = (kT/q)\ln(N_a/n_i)$.

Table 2.1 Polarity relationship between band bending, surface field and space charge in an MIS structure

V_s	F_s	Q_s	Free carrier conditions
+ve	+ve	−ve	Reduction of holes and/or increase of electrons
−ve	−ve	+ve	Reduction of electrons and/or increase of holes

$$\left(\frac{dV}{dx}\right)^2_{V=V_s} \equiv F_s^2 = \frac{4n_i q}{\varepsilon_0 \varepsilon_s}\left[\frac{kT}{q} ch \frac{q(V_F - V_s)}{kT} - \frac{kT}{q} ch \frac{qV_F}{kT} + V_s sh \frac{qV_F}{kT}\right] \tag{2.7}$$

From Gauss' Law, the surface field, F_s, is related to the total areal charge, Q_s, contained within the surface by:

$$Q_s = -\varepsilon_0 \varepsilon_s F_s \tag{2.8}$$

Hence, the relationship between Q_s and V_s is given by:

$$Q_s = \pm\sqrt{4n_i q \varepsilon_0 \varepsilon_s} G(V_s, V_F) \tag{2.9}$$

where $G(V_s, V_F)$ is given by:

$$G(V_s, V_F) = \mp\sqrt{\left[\frac{kT}{q} ch \frac{q(V_F - V_s)}{kT} - \frac{kT}{q} ch \frac{qV_F}{kT} + V_s sh \frac{qV_F}{kT}\right]} \tag{2.10}$$

Given the positive and negative values of Q_s in Eq. 2.9, the appropriate signs of V_s, F_s and Q_s are given in Table 2.1, and the correct value of Q_s is given by:

$$Q_s = -\frac{V_s}{|V_s|}|Q_s| \tag{2.11}$$

Equation 2.9 has been evaluated for a crystalline Si substrate doped with 10^{15} acceptors/cm^3, and the key features in the relationship between Q_s and V_s are shown in Fig. 2.2.[2] The three previously discussed regimes of accumulation, depletion and inversion are indicated, and, for accumulation and inversion, Q_s increases exponentially with V_s. In these two regimes, the main contributors to Q_s are the free carriers, so that the hole and electron densities increase exponentially with V_s in accumulation and inversion, respectively. In the third regime of majority carrier depletion, Q_s increases with $\sqrt{V_s}$, and extrapolating the inversion arm of the curve back into this regime shows that the ionised acceptor charge dominates Q_s. Hence, in the three regimes, either free carriers or fixed space charge constitutes the major part of Q_s. As will be seen in Chap. 6, this is not necessarily the case with TFT materials, in which trapping states in the forbidden

[2] Note that in evaluating Eq. 2.10, if the units of Boltzmann's constant, k, are in eV/K, then q has the value of unity. If SI units are used, then q has its usual value of 1.602×10^{-19} C.

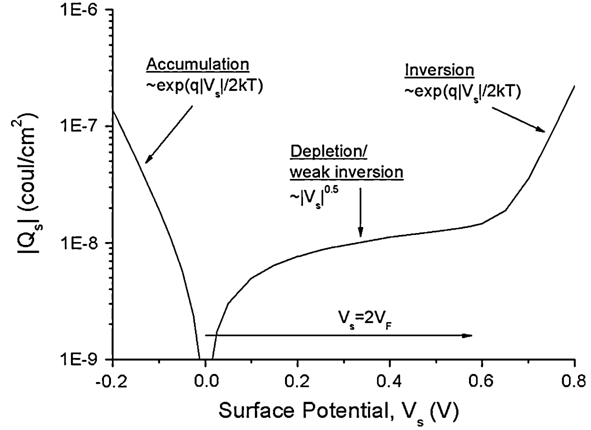

Fig. 2.2 Calculated variation of surface charge density with surface potential (substrate doping density is 1×10^{15} acceptors/cm^3)

band gap can continue to make a major contribution to Q_s even when the surface has enough free carriers to support substantial conduction.

For the calculation in Fig. 2.2, the value of qV_F was 0.288 eV below E_i, and the electron concentration in inversion starts to dominate Q_s at $V_s > \sim 2V_F$. In fact, the conventional definition of the threshold for *strong surface inversion* is at $V_s = 2V_F$, where the volume concentration of free electrons at the surface, n_s, is equal to the volume concentration of acceptors, N_a. When $V_s = V_F$, the surface is intrinsic ($n_s = p_s = n_i$), and the band bending regime beyond this, and up to strong inversion, is referred to as *weak inversion* ($p_s < n_s < N_a$).

In the depletion/inversion regime, the band bending, V_s, is positive, and for V_s, and $V_F > kT/q$, i.e., more than kT from the flat band position, Eq. 2.9 can be simplified to:

$$Q_s \cong -\sqrt{2q\varepsilon_0\varepsilon_s}\left[n_i\frac{kT}{q}exp\frac{q(V_s - V_F)}{kT} + N_aV_s\right]^{0.5} \tag{2.12}$$

The first term in the brackets relates to the free electron concentration, and the second term to the ionised acceptor space charge density, and the dependence of those terms on V_s shows the exponential and quadratic forms, respectively, discussed above. This simplified expression, with the physically obvious terms, provides a good approximation to the full Eq. 2.9, as seen by the calculations in Fig. 2.3. The calculations used two different substrate doping levels, and, for the more heavily doped substrate, with 10^{16} acceptors/cm^3, the value of qV_F is 0.348 eV below E_i, and this correspondingly increases the value of V_s at which strong inversion occurs. Also, the increase in Q_s, for the more heavily doped substrate, at a given value of V_s in depletion, is ~ 3 times more than for the less heavily doped substrate, as expected from the $\sqrt{N_a}$ dependence in Eq. 2.12.

Between flat bands and inversion, when the ionised acceptor space charge dominates, Eq. 2.12 can be further reduced to:

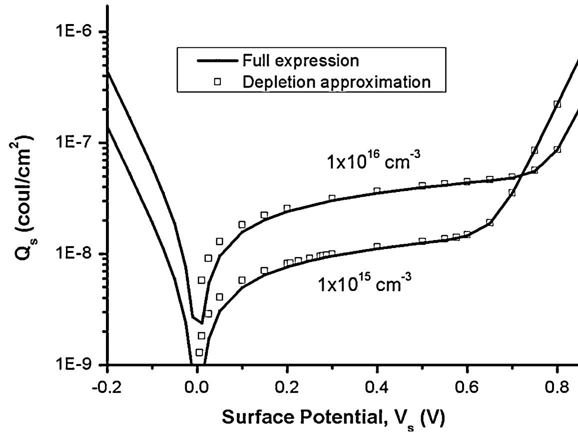

Fig. 2.3 Comparison of surface charge density calculations using the full (*solid line*) and approximate (*symbols*) expressions from Eqs. 2.9 and 2.12, respectively. (Substrate doping densities of 1×10^{15} acceptors/cm^3, and 1×10^{16} acceptors/cm^3)

$$Q_s \cong -\sqrt{2q\varepsilon_0\varepsilon_s N_a V_s} \equiv Q_b \tag{2.13}$$

Where Q_b is the areal acceptor space charge density. Equation 2.13 is the same as directly calculated from Poisson's equation using the depletion approximation, i.e. from:

$$\frac{d^2V}{dx^2} = \frac{qN_a}{\varepsilon_0\varepsilon_s} \tag{2.14}$$

and integrating this with respect to V. Alternatively, if Eq. 2.14 is integrated with respect to x, then:

$$Q_s = -qN_a x_d \tag{2.15}$$

where x_d is the width of the space charge depletion region at V_s. At inversion, when $V_s = 2V_F$, further increases in band bending cause such large increases in Q_s, due to the exponentially increasing free electron density, that, to a first approximation, the fixed space charge can be regarded as having reached a limiting maximum value, Q_{bmax}. This can be obtained by substituting $V_s = 2V_F$ into Eq. 2.13:

$$Q_{b\max} = -\sqrt{2q\varepsilon_0\varepsilon_s N_a 2V_F} \tag{2.16}$$

and from Eq. 2.15,

$$Q_{b\max} = -qN_a x_{d\max} \tag{2.17}$$

where x_{dmax} is the maximum width of the depletion region, and, from Eqs. 2.16 and 2.17, x_{dmax} is given by:

$$x_{d\max} = \sqrt{\frac{2\varepsilon_0\varepsilon_s 2V_F}{qN_a}} \tag{2.18}$$

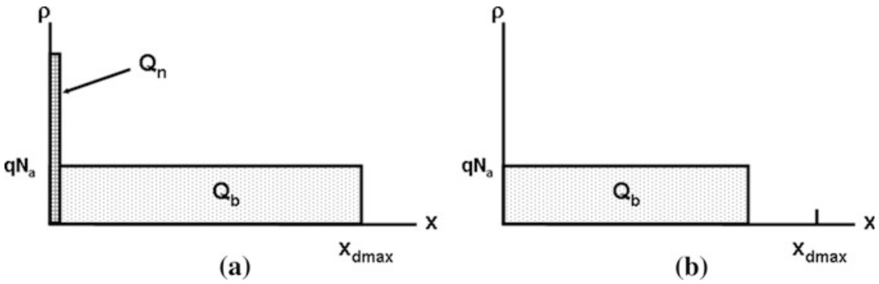

Fig. 2.4 Illustration of bulk depletion layer, Q_b, and inversion layer, Q_n, charge densities in: **a** inversion, and **b** depletion

Q_s in Eq. 2.12 can be represented by the sum:

$$Q_s = Q_n + Q_b \tag{2.19}$$

Where Q_b is the extended depletion layer charge, and Q_n is the areal density of inversion layer electrons. These will be confined close to the semiconductor surface, by virtue of the electrons being in a parabolic potential well of depth V_s. The terms in Eq. 2.19 are pictorially represented in Fig. 2.4a for inversion ($V_s > 2V_F$), and by Fig. 2.4b for depletion ($V_s < 2V_F$). The variation of x_{dmax} with N_a can be calculated from Eq. 2.18, and is shown in Fig. 2.5. From a TFT point of view, assuming a certain equivalence between N_a and the TFT trap state density, a curve of this type can be used to determine whether a thin film is fully depleted or not at inversion. For instance, the maximum equilibrium space charge width, at inversion, for a substrate doped with 10^{17} acceptors/cm^3 is 100 nm; therefore, a thin film of 100 nm, with an equivalent volume trapped charge density of $<10^{17}$ cm^{-3}, will be fully depleted before $V_s = 2V_F$. As a result of this, the threshold of inversion will occur at a lower value of band bending than for a thicker film having the same trap state density. This is discussed further in Chap. 3

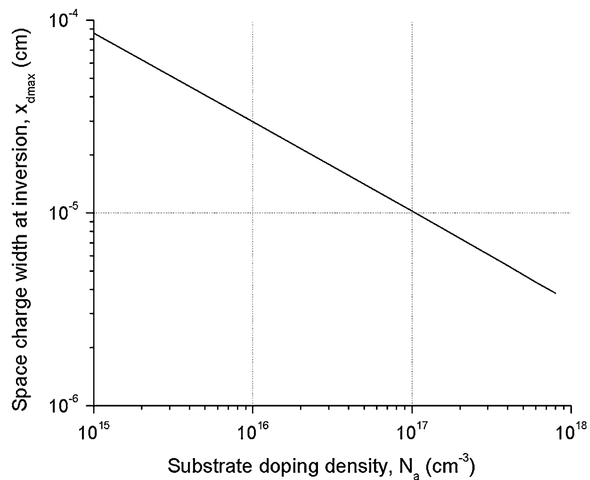

Fig. 2.5 Variation of maximum depletion layer width at inversion, x_{dmax}, with substrate doping level

2.2.2 Gate Bias and Threshold Voltage

Referring to Fig. 2.1, the voltage on the gate, V_G, is dropped partially across the dielectric, V_i, and partially across the semiconductor, V_s, so that:

$$V_G = V_i + V_s \tag{2.20}$$

And, for charge neutrality, the charge on the gate, Q_G, equals the charge in the semiconductor, Q_s, and

$$Q_G = \varepsilon_0\varepsilon_i F_i = \varepsilon_0\varepsilon_i V_i/d_i = C_i V_i = -Q_s \tag{2.21}$$

Where F_i is the field in the gate dielectric, and C_i is the capacitance/unit area of the gate dielectric. Hence,

$$V_G = V_s - Q_s/C_i \tag{2.22}$$

Equation 2.22 can be used to relate the voltage on the gate of an MIS capacitor to the induced charge density in the semiconductor, Q_s, and to the associated band bending, V_s. It can also be used to calculate the threshold voltage, V_T, of the structure, i.e. the gate voltage necessary to induce band bending of $2V_F$ at the semiconductor surface:

$$V_T = 2V_F + \frac{\sqrt{2q\varepsilon_0\varepsilon_s N_a 2V_F}}{C_i} \tag{2.23}$$

Figure 2.6 shows the calculated variation of V_G with V_s for the two substrate doping levels used in Fig. 2.3, and for a 150 nm thick gate dielectric of SiO_2. The more heavily doped substrate requires a larger gate bias to achieve a given degree of band bending in depletion, and, equally, has a larger value of V_T, as shown by Eq. 2.23. Once the surface has gone into strong inversion, the free electron density, Q_n, dominates Q_s, and Q_n is given by:

$$Q_n = C_i(V_G - V_T) \tag{2.24}$$

As will be seen in Chap. 3, this is a widely used expression for the calculation of channel currents in MOSFET devices above threshold. It is equally widely used for similar calculations in TFTs. Hence, the threshold voltage is a key parameter in determining on-state device characteristics, and the dependence of threshold voltage on substrate doping level is shown in Fig. 2.7.

2.2.3 Real MIS Structures

In contrast to the idealised MIS structure shown in Fig. 2.1, real structures may have work function differences between the gate metal and the semiconductor,

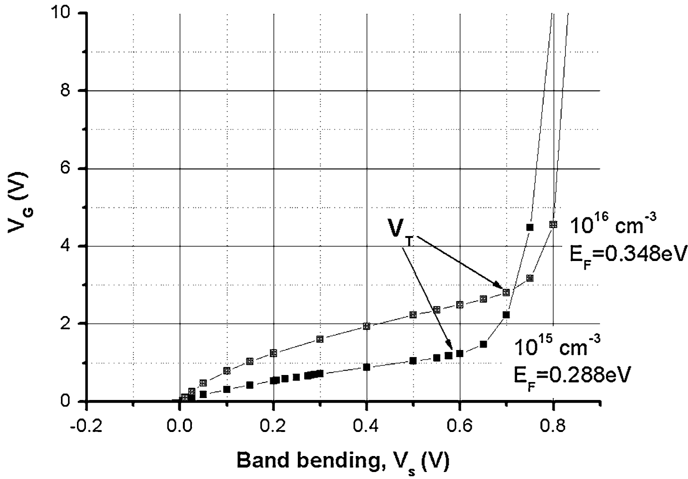

Fig. 2.6 Calculated variation of surface potential, V_s, with gate bias, V_G, in an ideal MIS structure, and showing the threshold voltage points. (Dielectric layer of 150 nm of SiO_2, and p-type substrate doping of 1×10^{15} cm^{-3}, and 1×10^{16} cm^{-3})

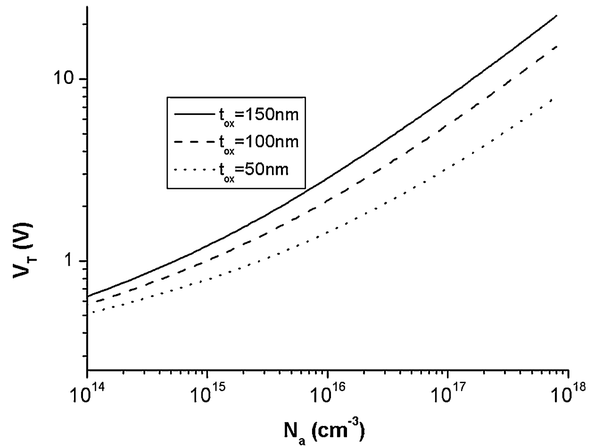

Fig. 2.7 Calculated variation of threshold voltage with substrate doping level, and thickness of SiO_2 gate dielectric

fixed charges in the oxide, and interface trapping states at the dielectric/semiconductor interface. These will change the zero-gate-bias band bending, and affect the relationship between V_G and V_s and Q_s.

2.2.3.1 Work Function Differences

In general, the Fermi level position in a free metal will be different from the Fermi level in a free semiconductor. These differences are usually expressed in terms of a work function difference, where the work function is the energy required to remove

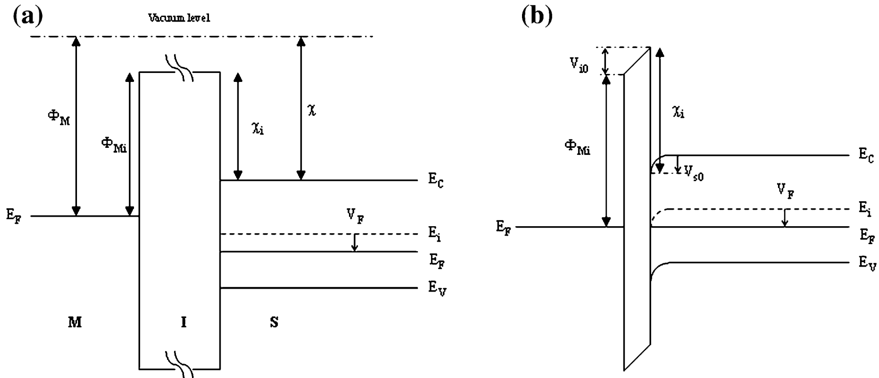

Fig. 2.8 MIS energy band diagrams in the presence of metal–semiconductor work function differences: **a** separated metal–insulator and insulator–semiconductor, **b** MIS system in thermal equilibrium

an electron from the Fermi level to the vacuum level. When the two materials are connected, and in thermal equilibrium, the Fermi levels need to be coincident, and there will be a flow of electrons from one material to the other, resulting in an interfacial dipole, which establishes this equilibrium. In the semiconductor, this will result in surface band bending, the extent of which will be much greater than in the metal due to the short screening length of the latter's high electron density.

In an MIS structure, it is conventional to reference the Fermi levels to the dielectric's conduction band edge [4] (rather than to the vacuum level), so that the quoted barriers, Φ_{Mi} and χ_i, are the energies needed to remove an electron to the dielectric conduction band (as shown in Fig. 2.8, and χ is the electro-negativity of the semiconductor). For the Si/SiO_2 system, these barrier energies were experimentally established by photo-emission measurements from the metal gate or the semiconductor into the oxide conduction band, and were 0.5–1 eV less than the respective vacuum values [5]. Figure 2.8a schematically shows the metal and the semiconductor separated, and Fig. 2.8b shows them connected in thermal equilibrium. In this case, electrons have flowed from the metal to the semiconductor to bring the Fermi levels into coincidence. As a result of this, the bands in the semiconductor have bent downwards by V_{s0}, with a corresponding voltage drop across the dielectric of V_{i0}. Equating the potentials either side of the high point in the insulator conduction band:

$$\Phi_{Mi} + V_{i0} = \chi_i + E_i/q + V_F - V_{s0} \tag{2.25}$$

The metal–semiconductor work function difference, Φ_{MS}, is, therefore, given by:

$$\Phi_{MS} = \Phi_{Mi} - (\chi_i + E_i/q + V_F) = -(V_{i0} + V_{s0}) \tag{2.26}$$

Thus, to remove the zero gate bias band bending in the system, and to restore flat band conditions, the gate voltage needs to be made more negative to induce

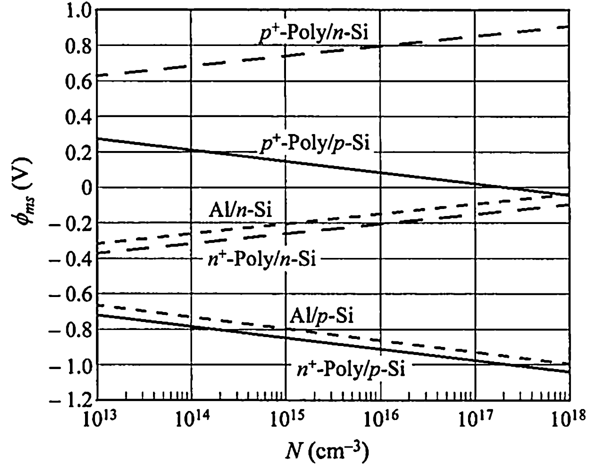

Fig. 2.9 Experimentally determined MOS work-function differences, Φ_{MS}, as a function of Si-substrate doping level, for different gate contact materials. (Reproduced from [1] with permission of John Wiley & Sons, Inc)

more positive charge in the semiconductor surface. The gate voltage at flat bands, V_{FB}, is given by:

$$V_{FB} = \Phi_{MS} = -(\mathrm{V_{i0}} + \mathrm{V_{s0}}) = -\left(\frac{\sqrt{2q\varepsilon_0\varepsilon_s N_a \mathrm{V_{s0}}}}{C_i} + \mathrm{V_{s0}}\right) \tag{2.27}$$

Equally, the gate voltage required to achieve a given degree of band bending, including the threshold for inversion, will be modified by the metal–semiconductor work function difference, so that the expression for the threshold voltage now becomes:

$$V_T = V_{FB} + \frac{\sqrt{2q\varepsilon_0\varepsilon_s N_a 2V_F}}{C_i} + 2V_F \tag{2.28}$$

As indicated in Eq. 2.26, the work function difference will be a function both of the gate metal, and of the doping level in the semiconductor substrate, as shown in Fig. 2.9 for Al and doped poly-Si gates [1]. Due to its refractory properties, doped poly-Si has been extensively employed as the gate electrode in MOSFET technology, and, with appropriate doping, it can be tailored to produce the required sign of flat band voltage.

2.2.3.2 Oxide Charges and Interface States

Many gate dielectrics, including SiO_2, are characterised by charged centres in the oxide, which induce an opposite charge in the semiconductor surface. If the charged centres, Q_i, are located at a distance x from the dielectric-semiconductor interface in an MIS capacitor, the charge induced in the semiconductor, Q_s, is:

$$\mathrm{Q_s} = \mathrm{Q_i}(\mathrm{d}-\mathrm{x})/\mathrm{d} \tag{2.29}$$

Hence, for charges at the dielectric/semiconductor interface, the induced charge is equal to the charge, Q_i, in the dielectric, whilst those at the metal interface have no effect. In many cases, the location of the charges may not be known, and an effective charge density, Q_{ieff}, will be determined, as though it were located at the dielectric/semiconductor interface.

As with the work function difference, this will result in a non-zero flat band voltage, given by:

$$V_{FB} = -Q_{ieff}/C_i \tag{2.30}$$

Positive charges are commonly found in SiO_2 films on Si, and are referred to as 'fixed' charges, as their effect is not dependent upon the surface potential in the semiconductor. In other words, they have a constant effect, irrespective of the bias conditions, and present a fixed density.

In real crystalline semiconductor surfaces, the termination of the regular, periodic bulk potential introduces allowed states into the forbidden band gap, usually referred to as surface states. These are intrinsic states at the surface, and, in addition to these, there may be extrinsic states due to impurities. The densities of intrinsic states can be up to $\sim 10^{15}$ cm^{-2} on an atomically clean surface, but, in a well-passivated surface, such as the Si/SiO_2 interface produced by thermal oxidation of Si, these can be reduced to $<1\text{–}5 \times 10^{12}$ cm^{-2}. The reduction is due to the SiO_2 network providing oxygen pairing atoms for the Si dangling bonds, and further passivation with hydrogen typically reduces the overall density to $\sim 10^{10}$ cm^{-2} or less. This combination of thermal oxidation and hydrogen passivation has generated one of the best-controlled semiconductor interfaces, and provided the basis for the Si semiconductor device industry.

Surface or interface states are generally distributed in energy across the forbidden band gap, and, in the case of the Si/SiO_2 interface, the distribution is U-shaped between the valence and conduction band edges. In contrast to the fixed charge, the charge in interface states will be determined both by their distribution across the band gap, and by the position of the Fermi level at the surface. Using the zero Kelvin approximation, those states beneath the Fermi level can be regarded as filled with electrons, whilst those above will be empty. Take, for example, a constant density, $N_{ss}(E)$, across the band gap, with acceptor levels in the upper half of the band gap, and donor levels in the lower half, and with a neutral level, E_0, at mid-gap. This distribution will have zero net charge in the interface states when the surface Fermi level is at mid-gap. However, if this distribution were added to the MIS band diagram used in Fig. 2.1a, where the Fermi level is below mid-gap, there would be a flow of electrons from the interface states below E_0, leading to positively charged, empty donor states at the surface, and an equal negative charge density in the semiconductor surface. Hence, the semiconductor bands at the surface will be bent down by an amount V_{s0} to ensure charge neutrality between the interface and the bulk, as shown in Fig. 2.10. In this example, the block of donor states between E_F and E_0 would be empty of electrons, and have a positive charge, Q_{ss}, balanced by the negative semiconductor surface charge, Q_s.

In general, the electron occupancy, F(E), of a surface state at energy E is given by the Fermi–Dirac distribution function:

$$F(E) = \frac{1}{1 + \exp(qV_F - qV_S - E)/kT} \tag{2.31}$$

Using the polarity convention of the earlier sections, E will have a negative value for centres above E_0 (which is at mid-gap), and a positive value for those below. Hence, the total negative charge in the surface states, Q_{ss}^-, with band bending $V_s > V_F$ is:

$$Q_{ss}^-(V_s) = -\int_{E_0}^{E_C} qN_{ss}(E)F(E)dE \approx -\int_{E_0}^{E_0+q(V_s-V_F)} qN_{ss}(E)dE \tag{2.32}$$

In Eq. 2.32, the full integral expression, which includes the Fermi–Dirac function, can be reduced to the simpler analytical form by using the zero Kelvin approximation, in which the acceptor states are negatively charged between the neutral level and the surface Fermi level, and neutral above the Fermi level. For a uniform distribution of acceptor states, N_{ss} can be brought outside the integral, and the density of negatively charged states, when $V_s > V_F$, is:

$$Q_{ss}^-(A) = -qN_{ss}q(V_s - V_F) \tag{2.33}$$

Similarly, for $V_s < V_F$ (as shown in Fig. 2.10), the density of positively charged donor states is:

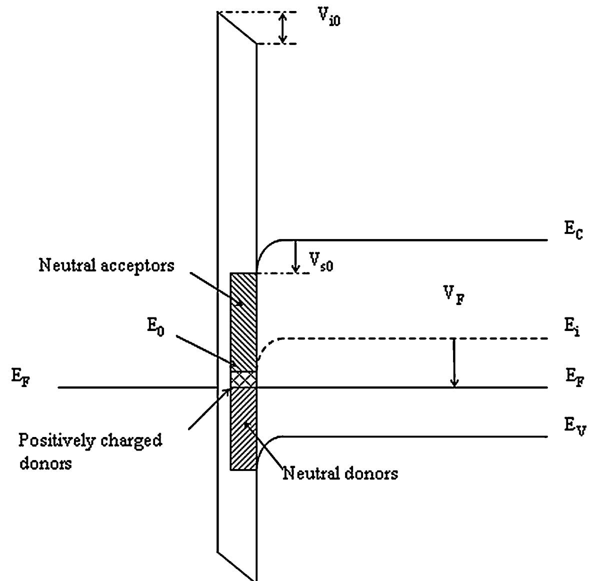

Fig. 2.10 Zero gate-bias MIS band diagram with a uniform distribution of interface states across the band gap, and with the cross-hatched region showing the charged states. (Donor and acceptor states in the lower and upper halves of the band-gap, respectively, and with the neutral level at mid-gap)

$$Q_{ss}^{+}(D) = qN_{ss}q(V_F - V_s) \tag{2.34}$$

For a constant distribution of surface states, the zero Kelvin approximation is a useful simplification. However, for trapping state distributions where the density varies significantly over an energy interval of kT, it is less accurate, and a numerical evaluation of the full integral in Eq. 2.32 would be required. This issue is discussed further in Sect. 6.2.3, where the volume trap density in a-Si:H varies exponentially with position from the band edge.

As with the work function difference and the fixed oxide charge, a bias, V_{FB}, will need to be applied to the gate to establish the flat band condition in the semiconductor, where V_{FB} is given by:

$$V_{FB} = -\frac{Q_{ss}(D)(V_s = 0)}{C_i} = -\frac{qN_{ss}qV_F}{C_i} \tag{2.35}$$

However, in contrast to the fixed oxide charge, the presence of interface states will give more than just a constant shift in the relationship between V_G and V_s and Q_s. In particular, as V_s is increased, not only does the gate bias need to induce the increasing value of Q_s, but it must also supply the increasing charge going into the interface states. The relationship between V_G and V_s from Eq. 2.22 is modified to be:

$$V_G = V_s - \frac{Q_s}{C_i} - \frac{Q_{ss}^{+}(D)}{C_i} - \frac{Q_{ss}^{-}(A)}{C_i} \tag{2.36}$$

and, for the example being used, $Q_{ss}(A) = 0$ for $V_s < V_F$, and $Q_{ss}(D) = 0$ for $V_s > V_F$, and the non-zero values of $Q_{ss}(A)$ and $Q_{ss}(D)$ are negative and positive, respectively.

Figure 2.11a compares the relationship, between V_G and V_s, for an ideal trap-free interface ($N_{ss} = 0$) and an interface containing a range of N_{ss} densities from 1×10^{10} cm^{-2} eV^{-1} to 1×10^{13} cm^{-2} eV^{-1}. The lowest interface state density of 10^{10} cm^{-2} eV^{-1} is so low that the V_G–V_s relationship is indistinguishable from the trap-free case. However, for the higher densities, increasingly large values of V_G are required to achieve a given amount of band-bending due to the charge going into the interface states. The curves have a common crossing point at $V_s = 0.288$ V, when the surface Fermi level is at mid-gap. This corresponds to the neutral level of the interface states, so that all the interface state distributions have the same zero charge in them. The flat band voltages can also be directly read from the curves by the values of V_G corresponding to $V_s = 0$ V.

The other parameter which can be extracted from these curves is the value of V_s when $V_G = 0$, which is the equilibrium zero-gate-bias bend banding, V_{s0}, and these values, together with the corresponding values of Q_{ss} (at V_{s0}), are shown in Fig. 2.11b. The 'S'-shaped curves demonstrate some simple physical principles of charge trapping over the range of N_{ss} values used. For low N_{ss} values, such as 10^{10} cm^{-2} eV^{-1}, the Fermi level position at the surface is dominated by the substrate doping level, and the surface states have almost no effect. In this case, the N_{ss}-

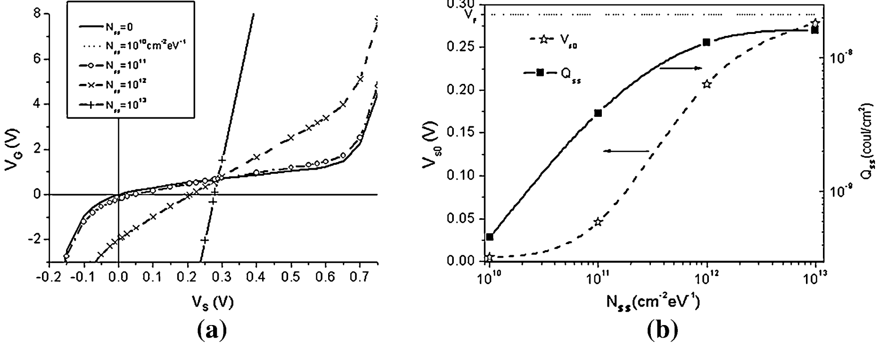

Fig. 2.11 Calculations using the uniform interface state distribution shown in Fig. 2.10 **a** variation of gate bias with surface potential, V_s, for different values of N_{ss}, and **b** variation of zero gate bias band bending, V_{s0}, and Q_{ss} (at V_{s0}) with N_{ss}. (Substrate acceptor density, $N_a = 10^{15}\ cm^{-3}$, $qV_F = 0.288$ eV, $t_{ox} = 150$ nm, and interface state density, $N_{ss} = 10^{10}$–$10^{13}\ cm^{-2}\ eV^{-1}$)

induced band bending tends towards zero, and the interface states are ionised almost down to the position of the bulk Fermi level, and $Q_{ss} \sim qN_{ss}qV_F$. Although a substantial fraction of the states are ionised, the charge in them is so low, that negligible band bending is required to produce an approximately equal amount of charge in the substrate. In contrast, for high N_{ss} values, such as $10^{13}\ cm^{-2}\ eV^{-1}$, the band-bending is dominated by the charge in the surface states, and the Fermi level tends towards being pinned at the surface state neutral level, i.e. $V_{s0} \Rightarrow V_F$. In this case, $V_F - V_{s0} = 0.01$ V, and the surface state neutral level is just 100 meV above the Fermi level. However, with the large surface state density, this still corresponds to a substantial charge, Q_{ss}, in the fractionally ionised donor surface states. For intermediate values of N_{ss} between 10^{11} and $10^{12}\ cm^{-2}\ eV^{-1}$, there is a progressive increase in V_{s0} with N_{ss}, and Q_{ss} is given by $qN_{ss}q(V_F - V_{s0})$.

Equation 2.36 also shows that the charge going into surface states has to be allowed for in calculating the gate threshold voltage for surface inversion. The surface potential at which this occurs is still $2V_F$, but the gate bias, in excess of the flat band voltage, to achieve this surface potential is increased to:

$$V_T = V_{FB} + \frac{\sqrt{2q\varepsilon_0\varepsilon_s N_a 2V_F}}{C_i} + 2V_F + \frac{Q_{ss}(V_s = 2V_F)}{C_i} \tag{2.37}$$

and, as $Q_{ss}(D) = 0$ for $V_s > V_F$, only charge in the acceptor states will contribute, and from Eq. 2.33, $Q_{ss}(A)$ at inversion is given by:

$$Q_{ss}(A) = qN_{ss}q(2V_F - V_F) = qN_{ss}qV_F \tag{2.38a}$$

Finally, the effects of the work function difference, the dielectric charge and the charge in interface states are all independent and additive, so that, in the presence of all three, the flat band voltage is given by:

$$V_{FB} = \Phi_{MS} - Q_{ieff}/C_i - Q_{ss}(V_s = 0)/C_i \tag{2.38b}$$

2.2.4 Evaluation of Surface Potential

From Eq. 2.9, the surface potential, V_s, uniquely defines the space charge density, Q_s, and Eqs. 2.22 and 2.36 define the gate bias, V_G, needed to achieve that potential, with and without surface states, respectively. Therefore, the measurement of V_s facilitates a quantitative insight into the state of a semiconductor surface. A common technique for establishing V_s is through the small signal capacitance-voltage measurement of an MIS diode, where the capacitance is given by:

$$\begin{aligned} &C = \frac{dQ_G}{dV_G} = -\frac{dQ_s}{dV_G} = -\frac{dV_s}{dV_G}\frac{dQ_s}{dV_s} \\ &\frac{dV_G}{dV_s} = 1 - \frac{1}{C_i}\frac{dQ_s}{dV_s} \text{ and } \frac{dQ_s}{dV_s} = -C_s \\ &\therefore C = 1/(1/C_i + 1/C_s) \end{aligned} \tag{2.39}$$

In other words, the capacitance of the MIS diode is the series combination of the capacitance of the dielectric, C_i, and of the semiconductor surface, C_s, where C_s is given by the differentiation of Eq. 2.9:

$$C_s = \frac{\sqrt{n_i q \varepsilon_0 \varepsilon_s}\left[\mathrm{sh}q(V_s - V_F)/kT + \mathrm{sh}qV_F/kT\right]}{G(V_s, V_F)} \tag{2.40}$$

and $G(V_s, V_F)$ is given by Eq. 2.10. The normalised C–V curves resulting from the evaluation of Eq. 2.40, for a silicon substrate doped with 10^{15} and 10^{16} acceptors/cm^3, and a gate oxide thickness of 150 nm, are shown by the solid lines in

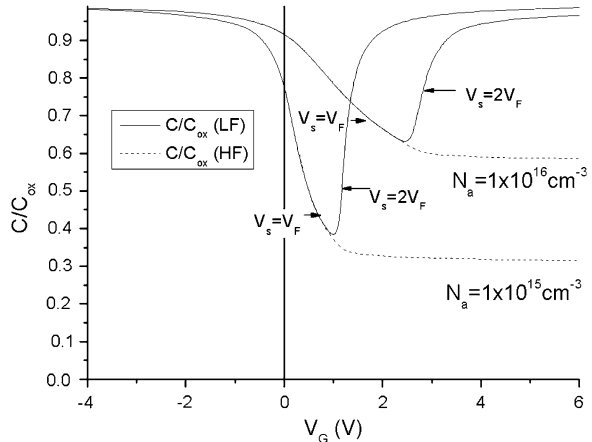

Fig. 2.12 Normalised high and low frequency MIS C–V curves (calculated for 150 nm thick SiO_2 gate dielectric)

Table 2.2 Relationship between normalised flat band capacitance, minimum C–V capacitance and substrate doping level (for 150 nm SiO_2 gate dielectric)

N_a (cm^{-3})	C_{FB}/C_i	$C_{min(LF)}/C_i$	$C_{min(HF)}/C_i$
1×10^{15}	0.77	0.38	0.32
1×10^{16}	0.91	0.63	0.59

Fig. 2.12. These curves have a characteristic 'V' shape, with the capacitance at negative V_G values tending towards the capacitance of the gate dielectric, due to the large capacitance of the hole accumulation layer. With increasing positive V_G, the capacitance falls due to the growth of the hole depletion region at the surface, which progressively reduces the surface capacitance. Finally, the curves start to rise as the surface becomes strongly inverted, and the large free electron concentration screens the underlying depletion layer, with the total capacitance once again tending towards the value of the gate dielectric.

As these curves have been calculated for an ideal MIS diode, the energy bands will be flat at $V_G = 0$, and, hence, the normalised capacitance at flat bands can be directly obtained from the curves. Given the unique relationship between surface potential and capacitance, the flat band voltage can, in principle, be directly obtained from any experimental C–V measurement using Eq. 2.40, assuming that the substrate doping level is known. Moreover, the minimum capacitance is also a unique function of doping level and dielectric capacitance, so that the doping level can be extracted from the minimum of the experimental C–V curve. The normalised flat band and minimum capacitance values from Fig. 2.12 are listed in Table 2.2, and they have also been extensively tabulated by Sze and Ng [1]. Also marked on the curves in Fig. 2.12 are the capacitance values at which the band bending gives an intrinsic surface ($V_s = V_F$), and the threshold for an inverted surface ($V_s = 2V_F$).

The solid line calculations assume thermal equilibrium, and the increase in capacitance in inversion will only be observed experimentally if the free electrons in the inversion layer can follow the a.c. measuring signal. In a high quality Si/SiO_2 capacitor, the inversion layer response time can be of the order of seconds, or more [6], as it depends upon a thermal generation process within the surface space charge region. Hence, the calculated curves are only likely to be replicated with a low frequency measurement, and the solid line curves in Fig. 2.12 are often referred to as low frequency C–V curves. Moreover, in the presence of interface states, there can be a further complication in the interpretation of the experimental low frequency curves. This will arise if the occupancy of the interface states at the Fermi level can follow the measuring signal, and, hence, contribute an interface state capacitance, C_{ss}, in parallel with the semiconductor surface capacitance C_s. The surface state capacitance, C_{ss}, is given by:

$$C_{ss} = -\frac{dQ_{ss}}{dV_s} \sim qN_{ss} \tag{2.41}$$

where, as discussed in the previous section, Q_{ss} can be approximated by $qN_{ss}q(V_s-V_F)$ for constant (or slowly varying) surface state densities. The presence of C_{ss} in an experimental C–V measurement means that Eq. 2.40 can no longer be used to give a unique relationship between measured capacitance and band bending, V_s. By implication, a high frequency measurement can be used to minimise the capacitive contributions of the surface states, and will also suppress the free electron capacitance in strong inversion. Hence, to interpret the high frequency C–V curves, a high frequency version of Eq. 2.40 is required. This essentially means suppressing the electron response in inversion, and this can be accomplished by expanding the cosh and sinh terms containing V_s, and setting to zero those of the form $\exp q(V_s-V_F)/kT$, since, in inversion, $V_s > V_F$ and those terms will govern the electron contribution to the surface capacitance. Hence the high frequency expression, $C_{s(HF)}$ is given by:

$$C_s = \frac{\sqrt{n_i q \varepsilon_0 \varepsilon_s}[-0.5 \exp -q(V_s - V_F)/kT + \mathrm{sh} q\mathrm{V_F}/\mathrm{kT}]}{G'(V_s, V_F)} \tag{2.42}$$

and $G'(V_s,V_F)$ is given by:

$$G'(V_s, V_F) = \mp\sqrt{\left[0.5\frac{kT}{q}\exp\frac{q(V_F - V_s)}{kT} - \frac{kT}{q}ch\frac{qV_F}{kT} + V_s \mathrm{sh}\frac{\mathrm{qV_F}}{\mathrm{kT}}\right]} \tag{2.43}$$

The high frequency C–V curve, calculated from Eq. 2.42, for $qV_s > 3kT$, is shown by the dotted lines in Fig. 2.12. The inversion layer response has been suppressed, and the surface capacitance in inversion tends to a constant value, approximately given by:

$$C_{s(HF)} = \frac{\varepsilon_0 \varepsilon_s}{x_{d(\max)}} \tag{2.44}$$

Where $x_{d(max)}$ is the limiting maximum thickness of the surface depletion region, as discussed in Sect. 2.2.1, and is given by Eq. 2.18. As with the minimum capacitance value of the low frequency curves, the minimum value of the high frequency curves is also a unique function of doping level, and can be used to establish the doping level in experimental samples. These values are also shown in Table 2.2. More importantly, any horizontal displacement, ΔV_G, of an experimental C–V curve from the theoretical C–V curve can be used to establish Q_{ss}, as a function of V_s, from:

$$\mathrm{Q_{ss}(V_s)} = \Delta \mathrm{V_G/C_i} \tag{2.45}$$

and N_{ss} can then be derived from dQ_{ss}/dV_s.

Whilst the emphasis in this section has been on high frequency measurements, and the use of the measured MISC capacitance to establish surface potential, there is also a low frequency procedure, called the quasi-static C–V measurement, which uses the change in capacitance, at a given value of V_G, to determine N_{ss} [7, 8]. Finally, to complete this section, one other well-established technique for the

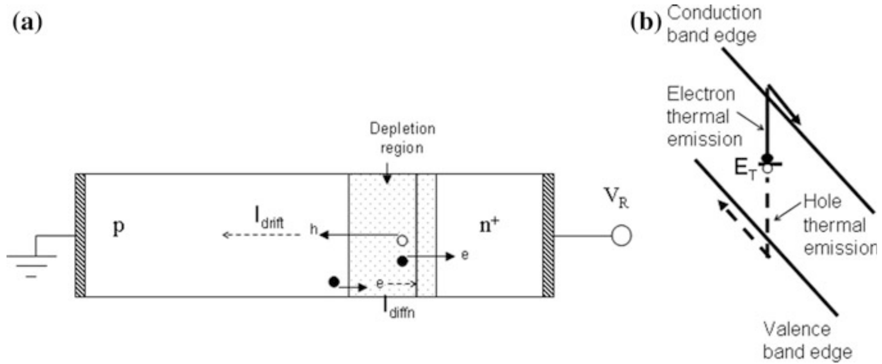

Fig. 2.13 Illustration of **a** reverse biased n^+-p junction, showing generation and diffusion leakage currents, and **b** e–h pair thermal generation process

evaluation of surface state densities should be mentioned, and this is the a.c conductance measurement of MISCs [9]. A detailed overview of these procedures can be found in Sze and Ng [1].

2.3 Electron-Hole Pair Generation and Recombination

Electron-hole pair generation and recombination are fundamental semiconductor processes relevant to both off-state leakage currents and to steady-state photo-currents in TFTs.

Two sources of leakage current in semiconductor devices are by ohmic conduction in lightly conducting and/or low generation lifetime material, or by electron-hole pair generation and/or diffusion current flow in reverse biased junctions. The latter processes are illustrated in Fig. 2.13a for a reverse biased n^+p junction. Due to the field within the space charge region, the holes generated within this region are swept into the p-type substrate, where they constitute an ohmic (drift) hole current to the substrate contact, I_{drift}. Equally, the electrons generated in the space charge layer are swept into the n^+ region, where they flow to the n^+ contact. For current continuity, there will be equal hole and electron currents, and these are referred to as generation currents. The electron-hole pair generation process, from a deep lying centre within the forbidden band gap, is shown schematically in Fig. 2.13b. In addition to the direct generation process, there is also a diffusion current, I_{diffn}, of minority carrier electrons from the neutral p-type substrate into the adjacent depletion region.

The role of electron-hole pair generation on leakage currents, including the diffusion current, is discussed in Sect. 2.3.3, and the recombination processes are presented in Sect. 2.3.4.

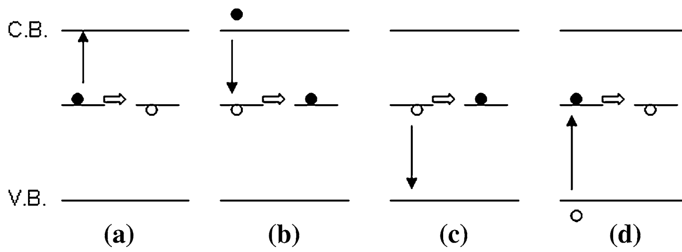

Fig. 2.14 Carrier emission and capture processes from a deep level centre in the forbidden band gap: **a** electron emission, **b** electron capture, **c** hole emission **d** hole capture. The *horizontal block arrow* shows the state's occupancy after the transition

In order to develop the expressions for electron-hole pair generation and recombination, it is necessary to consider the basic processes of carrier emission and carrier capture by a deep level centre, based upon the Shockley, Read, Hall (SRH) recombination statistics [10, 11], and the extension of this analysis to p–n junction characteristics [12].

The term deep level centre refers to intrinsic or extrinsic defects having energy levels within the forbidden band gap of the semiconductor, and which are usually further from the band edges than the shallow level dopant impurities. A deep level centre can behave as a trap, or as a generation centre, or as a recombination centre, depending upon its environment. For instance, in thermal equilibrium, a deep level acceptor in n-type material can capture electrons, thereby, reducing the free carrier density, and is acting as trap.[3] In a reverse biased space charge region, it can act as a generation centre, sequentially emitting electrons and holes, resulting in a reverse bias leakage current. Or, in material subject to electron-hole pair injection, it can act as a recombination centre, where the sequential electron and hole capture process establishes the steady-state free carrier density under the injection conditions. Hence, all three terms are often used interchangeably to refer to the same deep level centre, and, for brevity, the term trap is used as the generic term for the centre in this section.

2.3.1 Thermal Equilibrium

For a deep level centre within the semiconductor's forbidden band gap, four carrier transitions can be identified, as shown in Fig. 2.14. If the trap is an acceptor level, it has two charge states, one of which is negatively charged when it is occupied by an electron, and the other is neutral when it is empty of the electron (These two charge states can be equivalently described in terms of hole occupancy, which are empty

[3] The Fermi level position and the free electron concentration can be obtained from the numerical solution of the charge neutrality equation: $n + N_T^- = N_d^+$.

and filled, respectively. The same transitions will occur from a deep donor centre, the only difference being that it is positively charged when empty of an electron and neutral when occupied by an electron). Hence, there is a pair of possible carrier transitions from each of the two charge states, as shown in Fig. 2.14. From the negatively charged acceptor centre, these are either (a): electron emission to the conduction band, by a thermally stimulated process, or (d): hole capture from the valence band, and the release of phonon energy back to the lattice. Both leave behind the neutral centre. From the neutral centre, the two possible transitions are (b): electron capture from the conduction band, or (c): thermally stimulated hole emission to the valence band (which is equivalent to electron emission from the valence band). Both leave behind the negatively charged centre.

If the density of traps/generation/recombination centres is N_T, and if the centre and the Fermi level are positioned at E_T and E_F, respectively, above the valence band edge, then the trap occupancy is defined by the Fermi–Dirac distribution function, and from this the carrier transition rates can be calculated. These rates are determined by the number of free carriers and the appropriate occupancy of the centre, for the capture process, or just by the occupancy of the centre for the emission process (where it is implicitly assumed that there are sufficient empty states in the bands to accommodate the emitted carriers). In thermal equilibrium, the fractional electron occupancy of the trap, $F_D(E_T, E_F)$, is given by the Fermi–Dirac distribution function:

$$F_D = \frac{1}{1 + \exp(E_T - E_F)/kT} \tag{2.46}$$

The free carrier densities, n_0 and p_0, in n-type material doped with N_d donors, are given by[4]:

$$n_0 + N_T^- = N_d = N_C \exp -(E_C - E_F)/kT, p_0 = N_V \exp -E_F/kT \tag{2.47}$$

$$\text{and } n_0 p_0 = n_i^2 \tag{2.48}$$

The electron emission rate, R_{ee} is:

$$R_{ee} = e_n N_T^- = e_n N_T F_D \tag{2.49}$$

where e_n is the electron emission rate constant. Similarly, the rate of hole emission, R_{he}, is:

$$R_{he} = e_p N_T^0 = e_p N_T (1 - F_D) \tag{2.50}$$

where e_p is the hole emission rate constant. The rates of electron capture, R_{ec}, and hole capture, R_{hc}, are:

$$R_{ec} = c_n n_0 N_T^0 = \sigma_n v_{th} n_0 N_T (1 - F_D) \tag{2.51}$$

[4] From 2.47, if $N_T \ll N_d$, $E_F = kT \ln(N_d N_V / n_i^2)$.

$$R_{hc} = c_p p_0 N_T^- = \sigma_p v_{th} p_0 N_T F_D \quad (2.52)$$

where the electron and hole capture rate constants, c_n and c_p, are given by the product of the trap's capture cross section, σ_n and σ_p, respectively, and the carrier's thermal velocity, v_{th}. The thermal velocity is $\sqrt{(3kT/qm^*)}$, where m* is the effective mass, so that the thermal velocities for holes and electrons are different from each other. However, for simplicity in this analysis, they are taken to be the same.

In thermal equilibrium, the rate of electron capture must equal the rate of electron emission, and the equivalent equality must also exist for the hole transitions. Hence,

$$e_n N_T F_D = \sigma_n v_{th} n_0 N_T (1 - F_D) \quad (2.53)$$

And substituting for F_D and n_0, using Eqs. 2.46 and 2.47, respectively:

$$e_n = \sigma_n v_{th} N_C \exp -(E_C - E_T)/kT \quad (2.54)$$

Similarly, for the hole transitions:

$$e_p = \sigma_p v_{th} N_V \exp -E_T/kT \quad (2.55)$$

Hence, the thermal emission rate constants, e_n and e_p, are fundamental properties of the trap itself, and not dependent on the local concentrations of carriers. Moreover, their values are exponentially dependent upon the separation of the trap from the band edges.

2.3.2 Non-equilibrium, Steady State

Under steady state, non-thermal equilibrium conditions (where $np \neq n_i^2$), the trap will achieve a new occupancy, described by its quasi-Fermi level, and determined by the equality of the net electron transition rate and the net hole transition rate,[5] i.e.

$$\frac{dN_T^-}{dt} = R_{ec} - R_{ee} + R_{he} - R_{hc} = 0 \quad (2.56)$$

In contrast to the thermal equilibrium situation, the rates of electron emission and electron capture will not be equal. This is the situation in which there will be a net recombination or a net generation process, depending upon the divergence of the carrier concentrations from their thermal equilibrium values. Substituting the rate constants into Eq. 2.56 gives:

$$n c_n N_T^0 - e_n N_T^- = p c_p N_T^- - e_p N_T^0 \quad (2.57)$$

[5] If these rates are not equal, then the trap occupancy will change with time.

From Eq. 2.57, and using $N_T^0 = N_T - N_T^-$, the hole occupancy is:

$$N_T^0 = \frac{N_T(e_n + pc_p)}{nc_n + pc_p + e_n + e_p} \tag{2.58}$$

This can be used to calculate the net local electron generation/recombination rate, R_{GR}, which, in steady state, will also be equal to the net hole recombination/generation rate, i.e.:

$$R_{GR} = R_{ee} - R_{ec} = N_T^- e_n - nc_n N_T^0 \tag{2.59}$$

Substituting for the trap occupancy terms:

$$R_{GR} = \frac{N_T(e_n e_p - npc_n c_p)}{nc_n + pc_p + e_n + e_p} \tag{2.60}$$

$$R_{GR} = \frac{\sigma_n \sigma_p v_{th} N_T[\{N_C.N_V \exp -(E_C - E_T)/kT.\exp -E_T/kT\} - np]}{\sigma_n(n + N_C \exp -(E_C - E_T)/kT) + \sigma_p(p + N_V \exp -E_T/kT)} \tag{2.61}$$

Eliminating the exponential terms in E_T in the numerator, and replacing the remaining exponential term by n_i^2, gives the following expression:

$$R_{GR} = \frac{\sigma_n \sigma_p v_{th} N_T[n_i^2 - np]}{\sigma_n(n + N_C \exp -(E_C - E_T)/kT) + \sigma_p(p + N_V \exp -E_T/kT)} \tag{2.62}$$

The numerator shows that the rate of recombination/generation is proportional to the term $(n_i^2 - np)$, which expresses the deviation of the carrier population from thermal equilibrium. For $np > n_i^2$, the free carrier excess stimulates a net recombination process, where the carrier excess could result, for example, from optical illumination of the device, the forward biasing of a p–n junction or avalanche generation at a reverse biased p-n junction. For $np < n_i^2$, the free carrier deficit gives rise to net generation, and the free carrier deficit is most commonly encountered in the depletion region of a reverse biased p–n junction. In thermal equilibrium, the net rates of recombination or generation are zero.

Equation 2.60 (or its equivalents 2.61 or 2.62) would be typically used in device simulation packages to calculate the local rates of recombination or generation, but, for analytical work, a simplified version of this expression is often used by making the simplifying assumption that $\sigma_n = \sigma_p = \sigma$, and:

$$R_{GR} = \frac{\sigma v_{th} N_T[n_i^2 - np]}{n + p + 2n_i cosh(E_T - E_i)kT} \tag{2.63}$$

where the following substitutions have been used for N_C and N_V in the denominator:

$$n_i = N_C \exp -(E_C - E_i)/kT = N_V \exp -E_i/kT \tag{2.64}$$

2.3.3 Generation Currents

As mentioned above, the general treatment of generation or recombination is fully specified by the use of Eq. 2.60, and, in this section, an approximate, but more accessible, analytical treatment is presented for describing generation currents. For instance, in the space charge layer of a reverse biased junction, as shown in Fig. 2.13a, the free carrier concentrations can be taken as zero, so that there are no carrier capture processes, and Eq. 2.60 reduces to an expression for the local, steady state generation rate, R_G:

$$R_G = \frac{N_T e_n e_p}{e_n + e_p} \tag{2.65}$$

The steady state leakage current, J_R, due electron-hole pair generation, in a reverse biased p-n junction depletion layer of width W is:

$$J_R = q\int_0^W R_G dx = qR_G W = qWN_T \frac{e_n e_p}{e_n + e_p} \tag{2.66}$$

Where it is assumed that R_G is constant across W, and, in analogy with Eq. 2.18, W is given by:

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_s(V_R + V_0)}{qN_a}} \tag{2.67}$$

V_R is the reverse bias, and V_0 is the built-in p–n junction potential.

Returning to Eq. 2.66, the ratio $e_n e_p/(e_n + e_p)$ is a maximum when the denominator is a minimum, which will occur when $e_n = e_p$, and the traps are sited close to mid-gap. As E_T moves away from mid-gap either e_n or e_p will increase exponentially, as will the sum $e_n + e_p$, whilst the product $e_n e_p$ will be invariant. Hence, any centres located at mid-gap are likely to be the most efficient generation centres, and will dominate the device leakage current, J_R. For mid-gap centres, with equal capture cross sections, σ:

$$e_n = e_p = \sigma v_{th} N_C \exp -E_i/kT = \sigma v_{th} n_i \tag{2.68}$$

$$\therefore J_R = qR_G W = 0.5qn_i W\sigma v_{th} N_T \tag{2.69}$$

The *generation lifetime*, τ_g, is a figure of merit for the leakage current, and is defined by the following relationship:

$$J_R \equiv qn_i W/\tau_g \tag{2.70}$$

Hence, for mid-gap centres, the generation lifetime is:

$$\tau_g = 1/(0.5 N_T \sigma v_{th}) \tag{2.71a}$$

If the capture cross-sections are not equal:

$$\tau_g = 1/(N_T\sigma_n v_{th}) + 1/(N_T\sigma_p v_{th}) \quad (2.71b)$$

Equation 2.71b explicitly shows that the rate of the two-stage generation process is determined by the sequential emission of holes and electrons, and, if one capture cross-section is larger than the other, then the overall generation process will be rate limited by carrier emission from the charge state of the centre having the smaller cross-section. In experimental samples, this difference in capture cross-sections is likely to be found. For example, if the trap is an acceptor, then it will be neutral before capturing an electron, and negatively charged before capturing a hole. The Coulombic attraction between the hole and the negatively charged centre will result in the hole capture cross-section being larger than the neutral cross-section for electron capture [13]. As an example of this, one of the most widely studied deep level centres in silicon is gold, which has a near mid-gap acceptor level at 0.54 eV below the conduction band edge, and its capture cross-sections are 1.5×10^{-14} cm^2 and 9×10^{-17} cm^2, for holes and electrons, respectively [14]. In this case, Eq. 2.71b would be more appropriate than 2.71a for calculating the generation lifetime. In both cases, the generation lifetime is inversely proportional to the number of generation centres, and, as would be expected, the leakage current is proportional to this density.

However, if the only deep level centres are off mid-gap by more than a few kT, then, for those in the upper half of the band gap, $e_n \gg e_p$ (and $e_n \ll e_p$ if they are in the lower half). Taking, for example, a centre in the upper half of the band-gap, Eq. 2.66 reduces to:

$$J_R = qWN_T e_p \quad (2.72)$$

and the leakage current is limited by just the smaller of the two emission rate constants (in this case e_p), because, once the hole has been emitted, the following step of electron emission is so much faster that it has a negligible impact upon the overall two stage emission process. Expanding e_p:

$$J_R = qWN_T\sigma_p v_{th} n_i \exp -(E_T - E_i)/kT \quad (2.73)$$

$$\therefore \tau_g = 1/N_T\sigma_p v_{th} \exp -(E_T - E_i)/kT = 1/N_{T(eff)}\sigma_p v_{th} \quad (2.74)$$

$N_{T(eff)} = N_T \exp -(E_T - E_i)/kT$, and is the equivalent number of mid-gap centres, which would give the same leakage current. Hence, the shift in position of a generation centre from mid-gap increases the generation lifetime by $\exp(E_T - E_i)/kT$, and decreases the leakage current by the same amount.

In summary, the reverse bias p–n junction leakage current is characterised by the generation lifetime, τ_g, which is related to the physical characteristics of the deep level generation centres themselves.

The other contribution to junction leakage current is the flow of minority carriers, into the reverse biased space region, from the adjacent neutral material. In an n^+p junction, this will be electrons from the p-type substrate, and those adjacent to the space charge region will be swept through it, and into the n^+-region. This leaves a deficit of electrons at the depletion region edge, which establishes a local minority carrier concentration profile, thereby, driving a *diffusion current*, J_{diffn}. As the ohmic contact to the p-type substrate cannot readily supply electrons, they need to be generated within the material by thermal generation, and the diffusion current is determined by the generation lifetime, and is given by [4]:

$$J_{diffn} = qn_p\sqrt{D_n/\tau_g} \tag{2.75}$$

Where n_p is the equilibrium electron concentration in the p-type substrate $(=p_0/n_i^2)$, and D_n is the electron diffusion coefficient $(=kT\mu_n/q)$. A significant difference between the diffusion current and the generation current (Eq. 2.70) is that the diffusion current is not a function of the reverse bias voltage.

The treatment in this section has been limited to basic thermal emission processes, and these are directly used in the discussion of TFT leakage currents in Sect. 8.4. In Sect. 8.5.3, the treatment is extended to include field-enhanced emission processes.

2.3.4 Recombination Processes

Recombination will occur in response to a steady state carrier injection process (such as above band-gap optical illumination), where the injection results in an increase of the free carrier concentration above the thermal equilibrium values. The steady state carrier concentrations are given by the equality:

$$R_{inj} = R_R \tag{2.76}$$

Where R_{inj} is the injection rate, and R_R is the recombination rate given by Eq. 2.60 (or the equivalent Eqs. 2.61 and 2.62). As with the generation process, it is useful to simplify these equations to more physically meaningful forms. For charge neutrality, the injection process will result in an equality of the change in trap occupancy, and in the steady state excess densities of both holes and electrons, given by Δp and Δn, respectively. Where $p = p_0 + \Delta p$, and $n = n_0 + \Delta n$, and p_0 and n_0 are the thermal equilibrium carrier densities, and $n_0 p_0 = n_i^2$.

As with the discussion in the preceding sections, an n-type substrate is assumed, and, depending upon the relative values of Δp and n_0, two different injection conditions are identified. When $\Delta p \ll n_0$, this is regarded as *low-level injection*, and when $\Delta p \geq n_0$ this is defined as *high-level injection*.

2.3.4.1 Low-Level Injection

Consider an n-type substrate, with low-level injection, meaning that $\Delta p \ll n_0$, so that $n \sim n_0$. The *low-level recombination lifetime*, τ_R, is defined by:

$$R_R \equiv \Delta p/\tau_R \tag{2.77}$$

An examination of the physical recombination process will illustrate how Eq. 2.60 can be simplified to yield a more tractable expression for the recombination lifetime. Under low-level injection, the change in the free electron concentration is so small that the equilibrium Fermi level can still be used to describe the electron concentration. Hence, all trap levels beneath the Fermi level are filled with electrons, and ready to trap a hole as the first stage in the two-stage recombination process. Having captured a hole, with the rate constant $c_p(p_0 + \Delta p)$, the subsequent electron capture will proceed with the rate constant $c_n n_0$, which, given that $n_0 \gg (p_0 + \Delta p)$, will be a much faster process, and will not rate limit the overall recombination process. The only other consideration is whether the hole could be thermally emitted back into the valence band before the electron capture process has been completed. For the electron capture rate to exceed the hole emission rate, we need $c_n n_0 > e_p$, i.e.:

$$c_n N_C \exp -(E_C - E_F)/kT > c_p N_V \exp -E_T/kT \tag{2.78}$$

$$\text{i.e. } E_T > (E_C - E_F) + kT \ln(c_p N_V / c_n N_C) \tag{2.79}$$

Taking the logarithmic term in Eq. 2.79 to be smaller than $E_C - E_F$, Eq. 2.79 simply shows that, for efficient electron capture, the trap level must be further from the valence band edge than the Fermi level is from the conduction band edge. In other words, providing the trap level, E_T, is positioned somewhere between the Fermi level and an equivalent distance from the valence band edge, the recombination process will be limited just by hole capture. Replacing n and p in Eq. 2.62:

$$R_R = \frac{-\sigma_n \sigma_p v_{th}^2 N_T n_0 \Delta p}{c_n n_0 + e_n + c_p(p_0 + \Delta p) + e_p} \tag{2.80}$$

From the above discussion, for $E_F > E_T > E_C - E_F$, then $c_n n_o > e_n$, e_p, and $c_p(p_0 + \Delta p)$, and Eq. 2.80 reduces to:

$$R_R = -\sigma_p v_{th} N_T \Delta p \equiv \Delta p/\tau_R \tag{2.81}$$

$$\text{and } \tau_R = 1/\sigma_p v_{th} N_T \tag{2.82}$$

In other words, the recombination lifetime is a function of the trap state density, N_T, and the hole capture cross-section, and is independent of the trap energy level over a substantial fraction of the band gap (as defined above). Equation 2.82 is similar to the generation lifetime for a mid-gap generation centre (Eq. 2.71), but, in contrast to the recombination lifetime, once E_T is more than a few kT from mid-

gap, the generation lifetime increases substantially (as shown by Eq. 2.74). Therefore, except in the special case of a mid-gap centre, the steady state generation and recombination lifetimes can be substantially different.

When E_T lies outside the range prescribed for Eq. 2.81, the recombination lifetime will increase. If $E_T > E_F$, then the traps will be largely empty of electrons, and the number of traps available for hole capture will be low. In this situation, $e_n > c_n n_0$, and Eq. 2.80 becomes:

$$R_R \approx \frac{-\sigma_n \sigma_p v_{th}^2 N_T n_0 \Delta p}{e_n} = -\sigma_p v_{th} N_T \Delta p \exp(E_F - E_T)/kT \tag{2.83}$$

$$\text{and } \tau_R = \exp\{(E_T - E_F)/kT\}/\sigma_p v_{th} N_T \qquad (\text{for } E_T > E_F) \tag{2.84}$$

Hence, as E_T rises above E_F, the lifetime is larger than that given by Eq. 2.82, and it increases exponentially with increasing values of E_T.

Similarly, if the separation of E_T from the valence band edge is smaller than the value of $(E_C - E_F)$, then e_p will exceed $c_n n_0$, and, from Eq. 2.80, the recombination lifetime will be:

$$\tau_R = \frac{N_V \exp(E_C - E_F - E_T)/kT}{N_C \sigma_n v_{th} N_T} \qquad (\text{for } E_T \le E_C - E_F) \tag{2.85}$$

In other words, as the trap level gets closer to the valence band edge, and E_T reduces, the lifetime exponentially increases, but is now controlled by the capture cross section for electrons, rather than for holes, as it has been in the previous cases.

2.3.4.2 High-Level Injection

As with low-level injection, the recombination process is described by the general Eq. 2.60 (or its equivalents), and to reduce these to a simpler form, the high-level injection situation of $\Delta p \gg n_0$ is considered. In this case, if $\Delta p \gg N_T$, then charge neutrality will be determined just by equality in the excess free carrier densities, i.e. $n = p = \Delta p = \Delta n$, and the equilibrium Fermi level splits into separate quasi-Fermi levels, E_{Fp} and E_{Fn}, for holes and electrons, respectively, where the quasi-Fermi levels are given by:

$$p = N_V \exp - E_{Fp}/kT \quad \text{and} \quad n = N_C \exp - (E_C - E_{Fn})/kT \tag{2.86}$$

If the recombination centre is sited between the quasi-Fermi levels, such that $E_{Fp} < E_T < E_{Fn}$, then $nc_n > e_n$ and $pc_p > e_p$, and the steady state recombination centre occupancy can be obtained from Eq. 2.58:

$$N_T^0 = \frac{N_T \sigma_p}{\sigma_n + \sigma_p} \equiv N_T(1 - F_D) \tag{2.87}$$

F_D is the centre's Fermi-Dirac function, given by Eq. 2.46, in which the equilibrium Fermi level, E_F, is replaced by the quasi-Fermi level for the recombination centre, E_{FT}. For the special case of equal capture cross sections, $F_D = 0.5$, and the quasi-Fermi level for the recombination centre is located at E_T.

For the recombination centre located between the hole and electron quasi-Fermi levels, the recombination lifetime, τ_R, can be calculated from Eqs. 2.60 and 2.77:

$$R_R = \frac{N_T(e_n e_p - npc_n c_p)}{nc_n + pc_p + e_n + e_p} \approx -\frac{N_T \Delta p^2 c_n c_p}{\Delta pc_n + \Delta pc_p} \equiv \frac{\Delta p}{\tau_R} \tag{2.88}$$

and

$$\tau_R = 1/\sigma_p v_{th} N_T + 1/\sigma_n v_{th} N_T \tag{2.89}$$

Hence, the difference between the low-injection and high-injection lifetimes is that, at high-injection, the lifetime explicitly accounts for the two-stage electron and hole capture process, and the lifetime is correspondingly longer. This is due to the equal densities of holes and electrons. In contrast, the low-injection lifetime was determined just by hole capture, due to the more rapid electron capture process resulting from the much higher majority carrier density of electrons.[6]

As with low-level injection, once the recombination level is outside the energy interval bracketed by the carrier quasi-Fermi levels, the lifetime will increase exponentially with this separation.

2.4 Current Flow Equations

The purpose of this section is to introduce the concepts underlying the modelling of current flow in semiconductor devices, so that the reader has an appreciation of the equations used in device simulation packages. As explained in the introduction, the numerical techniques used to solve these equations are beyond the scope of this book, and further information on device simulation can be found in Refs. [2] and [3].

To establish the basic equations, one-dimensional flow will be considered initially, and then extended to show the form used in 2-D or 3-D simulation programmes.

For current flow by carrier drift and diffusion, the total current density, J_T, is given by the sum of the electron, J_n, and hole, J_p, drift/diffusion currents [1]:

$$J_T = J_n + J_p \tag{2.90}$$

[6] The situation described in Sects. 2.3.4.1 and 2.3.4.2 is for n-type substrates, and, for injection into p-type substrates, the low-level lifetime will be determined by electron capture.

$$J_n = q\mu_n nF + qD_n \frac{\partial n}{\partial x} \quad (2.91)$$

$$J_p = q\mu_p pF - qD_p \frac{\partial p}{\partial x} \quad (2.92)$$

Where F is the field, μ is the carrier mobility, n and p are the free carrier densities, and D is the diffusion coefficient. These are essentially low field equations, because, as discussed below, at high fields, carrier velocity saturation can occur [15], requiring the μF product to be replaced by the appropriate high field velocity. In Eqs. 2.91 and 2.92, the first term describes the flow of carriers under the influence of an internal field, which would result from an externally applied bias, and the second term is the carrier flow by diffusion resulting from a non-uniform carrier distribution.

The continuity equation links these equations to local generation and recombination processes by:

$$\frac{\partial n}{\partial t} = G_n - R_{GR} + \frac{\partial J_n}{q\partial x} \quad (2.93)$$

$$\frac{\partial p}{\partial t} = G_p - R_{GR} - \frac{\partial J_p}{q\partial x} \quad (2.94)$$

These equations show that the local rate of change of carrier concentration, within a given volume of material, is determined by the difference in the external carrier generation rate, G, and the internal recombination rate, R_{GR}, plus the difference in the carrier flow into and out of the volume. In *steady state*, the local carrier concentrations are constant, and Eqs. 2.93 and 2.94 are equal to zero. The internal recombination/generation rate, R_{GR}, is given by Eq. 2.60 from Sect. 2.3.2, and the external generation rate, G, could be due to optical absorption of above band-gap light. In this case, the local optical generation rate, G_O is:

$$G_o(z) = \alpha\Phi(1 - R)\exp -\alpha z \quad (2.95)$$

Where α is the optical absorption coefficient, Φ is the incident photon flux, R is the surface reflectivity, and z is the distance in the material perpendicular to the illuminated surface.[7]

Another potential source of carrier generation is high-field generation of electron-hole pairs by impact ionisation. This is also referred to as avalanche generation, since the generated carriers will also be accelerated by the field, and produce further carriers by impact ionisation themselves. This is most likely to occur with high carrier mobility semiconductors, and in high field regions of devices, such as reverse biased junctions. Where the carrier mobility is low, due to short mean free paths and efficient scattering, the carrier is unlikely to gain enough energy from the field. However, where the mean free path is large, the carriers can

[7] For a 1-D treatment, we require $\alpha < z$ for uniform carrier generation.

be efficiently accelerated and heated by the field. If the carriers attain sufficient energy, then lattice collisions can lead to electron-hole pair generation. The impact ionisation generation rate, G_{II}, is given by [1]:

$$G_{II} = nv_n\alpha_n + pv_p\alpha_p \tag{2.96}$$

Where v_n (v_p) is the electron (hole) drift velocity, α_n (α_p) is the electron (hole) ionisation coefficient, and:

$$\alpha_{n,p} = \frac{qF}{E_I}\exp - \frac{F_C}{F} \tag{2.97}$$

F_C is the critical field, F is the field parallel to current flow, and E_I is the carrier ionisation energy (for Si this is 3.6 eV for electrons and 5.0 eV for holes). A simpler expression [16] has also been used in simulations of TFTs [17], where the ionisation coefficient is:

$$\alpha_{n,p} = \alpha_{n,p}^{\infty} \exp - \frac{F_C}{F} \tag{2.98}$$

and α^{∞} is a constant, which is determined, together with F_C, from simulation fits.

The carrier velocity, in Eq. 2.96, at low fields, is given by μ_0F, where μ_0 is the low field mobility. At high fields, velocity saturation occurs, and the following relationship between velocity and field was found to provide a good fit to the experimental c-Si data shown in Fig. 2.15 [15]:

$$v_{n,p} = \frac{\mu_0 F}{\left[1 + (\mu_0 F/v_S)^{\beta}\right]^{1/\beta}} \tag{2.99}$$

Where v_S is the saturated velocity ($\sim 10^7$ cm/s for holes and electrons in Si), and β is a constant (~ 2 for electrons and ~ 1 for holes in Si).

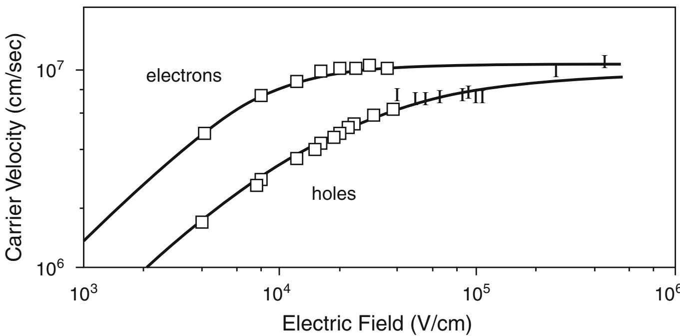

Fig. 2.15 Carrier velocity measurements as a function of the electric field in silicon. The *solid line* is the empirical fit to Eq. 2.99 (Reprinted from [15] with permission of IEEE)

Equations 2.90–2.94 contain the electrostatic field, F, which is the local gradient of the potential, dV/dx, and this has to be established in a self-consistent fashion by the simultaneous solution of Poisson's equation:

$$\frac{d^2V}{dx^2} = -\frac{q\rho(x)}{\varepsilon_0\varepsilon_s} \tag{2.100}$$

$$\text{and } \rho = p - n + N_d - N_a + N_{Td}^{+} - N_{Ta}^{-} \tag{2.101}$$

where N_d and N_a are shallow donor and acceptor dopants, and N_{Ta} and N_{Td} are deep acceptor and donor defects, respectively. For a TFT, the deep levels could equally well refer to a distribution of defect levels across the band-gap.

The above equations have been presented, for simplicity, in a 1-D format, but, for accurate device simulation, these equations need to be solved in two or three dimensions. In that case, the coupled equations in steady state are [18]:

$$\begin{aligned} \nabla.\nabla V &= -q\rho/\varepsilon_0\varepsilon_s \\ \nabla.J_n &= -q(G_n - R_{GR}) \\ \nabla.J_p &= q(G_p - R_{GR}) \\ J_n &= -qn\mu_n\nabla V + qD_n\nabla n \\ J_p &= -qp\mu_p\nabla V - qD_p\nabla p \end{aligned} \tag{2.102}$$

These are solved subject to a set of boundary conditions determined by the biases applied to the device terminals, the field continuity conditions across internal material boundaries (such as the semiconductor/dielectric interface), and the conditions at the external boundaries of the device, where, for instance, the field may be clamped at zero.

In the commercial simulators used for Si-based TFTs, the internal recombination/generation rate, R_{GR}, includes additional processes to those considered in Sect. 2.3. In particular, the treatment of carrier emission is extended to include field-enhanced emission processes from traps, as well as band-to-band tunnelling. Those mechanisms are discussed further in Sect. 8.5.3.

2.5 Summary

Some analytical device physics concepts, using single crystal equations, have been introduced as a background topic to later chapters. These simple concepts are widely used in interpreting TFT behaviour, and they provide a solid basis for appreciating the assumptions and approximations used in that work.

The topics in this chapter have been restricted to those of most relevance to TFTs, and have focussed, firstly, on aspects of semiconductor surface physics,

which describe the relationship between gate bias, surface space charge, and band bending in MIS structures. This topic underpins the understanding of IGFET behaviour, which will be the subject of Chap. 3. The second topic is electron-hole pair recombination and generation processes through deep level centres in the forbidden band gap. These processes play a role in establishing steady-state carrier concentrations under injection processes, and determine reverse bias leakage currents from junction depletion regions. Finally, there is a brief overview of the current flow processes, which are incorporated in device simulation packages.

Appendix: Summary of Key Equations

A number of the simplified equations from the text, which can be used in basic analytical calculations, are reproduced below. The equation numbers are retained for quick reference back to the original derivations.

A.1 Semiconductor Surface Band Bending

Relationships between surface potential, V_s, space charge density, Q_s, gate voltage, V_G, and threshold voltage, V_T.

(a) Depletion and Inversion Space Charge Density

$$Q_s \cong -\sqrt{2q\varepsilon_0\varepsilon_s}\left[n_i\frac{kT}{q}exp\frac{q(V_s-V_F)}{kT}+N_aV_s\right]^{0.5} \tag{2.12}$$

(b) Depletion Space Charge Density

$$Q_s \cong -\sqrt{2q\varepsilon_0\varepsilon_s N_a V_s} \tag{2.13}$$

(c) Gate Voltage, Surface Potential and Space Charge Density

$$V_G = V_s - Q_s/C_i \tag{2.22}$$

(d) Gate Threshold Voltage

$$V_T = V_{FB} + \frac{\sqrt{2q\varepsilon_0\varepsilon_s N_a 2V_F}}{C_i} + 2V_F \tag{2.28}$$

and, from Eq. 2.5, $V_F = (kT/q)\ln(N_a/n_i)$

(e) Depletion Layer Thickness at Inversion

$$x_{d\max} = \sqrt{\frac{2\varepsilon_0\varepsilon_s 2V_F}{qN_a}} \tag{2.18}$$

(f) Flat-Band Voltage

$$\mathrm{V_{FB}} = \Phi_{\mathrm{MS}} - \mathrm{Q_{ieff}}/\mathrm{C_i} - \mathrm{Q_{ss}}/\mathrm{C_i}$$

A.2 Carrier Recombination and Generation

Relationships between trap density, N_T, and capture cross section, σ, and the carrier generation/recombination rates.

(a) General Recombination and Generation Rate Expression

$$R_{GR} = \frac{\sigma v_{th} N_T [n_i^2 - np]}{n + p + 2n_i cosh(E_T - E_i)kT} \tag{2.63}$$

(b) Generation Leakage Current

$$J_R \equiv qn_i W/\tau_g \tag{2.70}$$

(c) Generation Lifetime, τ_g

$$\tau_g = 1/(0.5 N_T \sigma v_{th}) \tag{2.71a}$$

(d) Carrier Recombination Rate, and Recombination Lifetime, τ_R

$$R_R = -\sigma_p v_{th} N_T \Delta p \equiv \Delta p/\tau_R \tag{2.81}$$

(e) Recombination Lifetime (Low Injection Level)

$$\tau_R = 1/\sigma_p v_{th} N_T \tag{2.82}$$

(f) Recombination Lifetime (High Injection Level)

$$\tau_R = 1/\sigma_p v_{th} N_T + 1/\sigma_n v_{th} N_T \tag{2.89}$$

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Chapter 3
Insulated Gate Field Effect Transistors, IGFETs

Abstract The metal-oxide-semiconductor field effect transistor, MOSFET, is the most widely studied and understood IGFET, and is used here to describe key aspects of IGFET behaviour. The topic is introduced by a physical description of MOSFET operation, which identifies the linear and saturation operating regimes. A simple analytical model is developed from this, yielding expressions for important parameters such as threshold voltage, saturation voltage and carrier mobility. These are extensively used in TFT analysis. A more rigorous analysis is presented to explicitly include the role of substrate doping, and its effect upon saturation voltage. These descriptions are valid for the on-state regime, in which the gate bias, V_G, is greater than the threshold voltage, V_T. A further operating regime is described for $V_G < V_T$, which is referred to as the sub-threshold regime. In this regime, the current increases exponentially with gate bias, and is characterised by the sub-threshold slope. This is another concept, and parameter, which is widely used in the analysis of TFT behaviour. Finally, the role of film thickness, in thin film devices, in modifying the standard expressions for threshold voltage and saturation voltage is presented.

3.1 Introduction

This chapter will follow the convention of Chap. 2, and use single crystal equations to deal analytically with IGFET operation. The analysis will be based upon the most widely studied IGFET, the c-Si metal-oxide-semiconductor, MOSFET, whose concepts are widely invoked in analysing TFT behaviour. The basic device equations, and underlying assumptions, are extensively used to extract parameters, such as the threshold voltage, V_T, the saturation voltage, $V_{D(sat)}$, and the carrier's field effect mobility, from TFT measurements.

In Sect. 3.2, the basic MOSFET behaviour is described in terms of the dependence of the channel current, I_d, on gate and drain bias, which leads to the definition of the linear and saturation current regimes. The three terminal current-

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voltage equations are developed in the classical, simplified form in Sect. 3.3.1, and then extended to take account of substrate doping effects in Sect. 3.3.2. These two sections deal with the on-state behaviour of the device, when the gate voltage, V_G, is larger than the threshold voltage, V_T.

In Sect. 3.4, the current flow equations are considered for the regime where $V_G < V_T$, which is defined as the sub-threshold regime. Operation in this regime is characterised by the sub-threshold slope, S, which is given by $dV_G/d\log(I_d)$. Finally, in Sect. 3.5, the way in which the MOSFET concepts need to be modified, to take account of the limited film thickness in thin film devices, is discussed.

Some of the key equations from this chapter are listed in the appendix for future reference.

3.2 MOSFET Operation

A schematic diagram of an n-channel MOSFET is shown in Fig. 3.1, in which there are n^+ doped source and drain regions, separated by a distance L, which defines the channel length. In this particular case, the edges of the source and drain regions are coincident with the gate edges, which is the standard MOSFET architecture. This architecture is referred to as *self-aligned*, and is achieved by using the gate electrode as a mask for doping the source and drain regions by ion implantation. The width of the channel, in the z-direction (which is perpendicular to the page), is W. Surface band bending, perpendicular to the Si/SiO_2 interface, is in the x-direction.

In the on-state, positive biases V_D and V_G are applied to the drain and gate terminals, respectively, with respect to the earthed source terminal. There is a fourth terminal in a MOSFET, which is the p-type substrate connection, which, under reverse bias, will increase the transistor's threshold voltage, but, for the following discussion, it will be taken as earthed, and will have no direct effect upon the device's behaviour. For TFTs, this connection to the device layer will generally not be available.

The device model to be described is the long/gradual channel model, in which the field along the channel (driving the on-current) is much smaller than the vertical field (determining the inversion layer concentration), and the two are effectively decoupled, so that fundamental 2-D phenomena, such as short channel effects, are not incorporated. The band bending and energy level conventions are those used in Sect. 2.2, i.e. all energies and potentials in the semiconductor are measured from the intrinsic level, and are positive for levels beneath the intrinsic level (see Fig. 2.1 for further details).

Consider first the situation shown in Fig. 3.2a, in which there is an inversion layer induced by the gate bias, V_G (which is larger than the threshold voltage, V_T), and, at zero drain bias, the inversion layer will be uniform along the channel. As discussed in Chap. 2 (Eqs. 2.17–2.19), the areal charge densities within an inverted surface can be represented by the free electron inversion charge density, Q_n, and the underlying ionised acceptor space charge density, Q_b, where Q_n, Q_b, and V_T are given by:

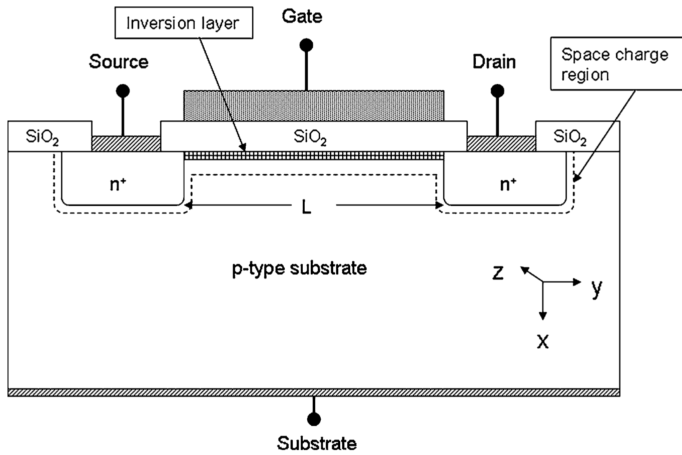

Fig. 3.1 Schematic cross section of a MOSFET, with the gate voltage larger than the threshold voltage, and showing the surface inversion and depletion layers. The channel length is L, and the width, W, is perpendicular to the page

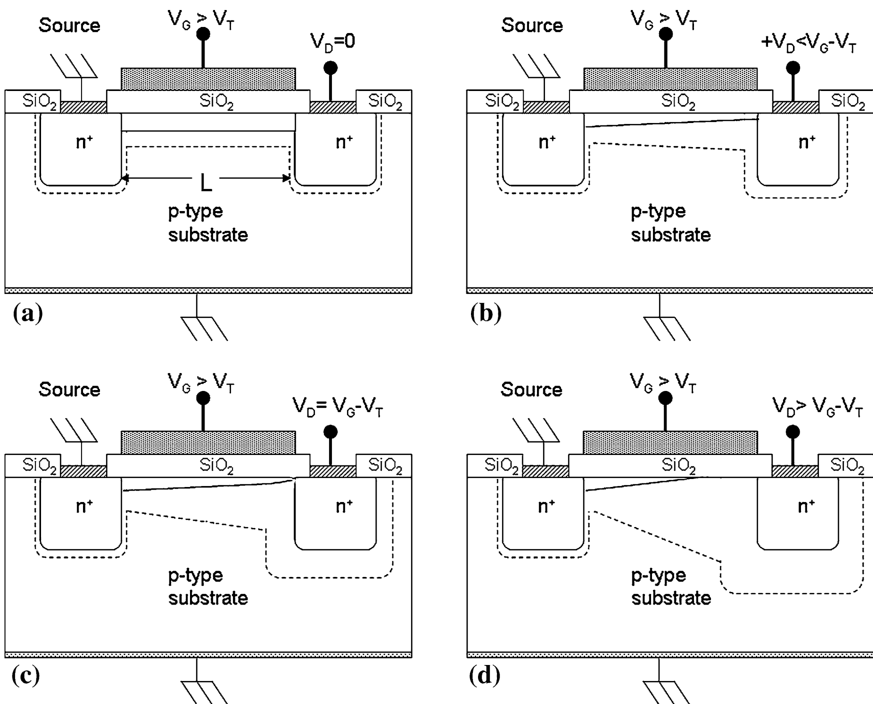

Fig. 3.2 Cross-section of MOSFET, in the on-state, for different values of drain bias, V_D: **a** $V_D = 0$, **b** $V_D < V_G - V_T$, **c** at pinch-off, with $V_D = V_G - V_T = V_{D(sat)}$, and **d** $V_D > V_{D(sat)}$, showing channel shortening. (Gate and drain biases are applied with respect to the grounded source terminal)

$$Q_n = C_i(V_G - V_T) \tag{3.1a}$$

$$Q_b = qN_a x_{dmax} = \sqrt{(2q\varepsilon_0\varepsilon_s N_a 2V_F)} \tag{3.1b}$$

$$V_T = 2V_F + \sqrt{(2q\varepsilon_0\varepsilon_s N_a 2V_F)}/C_i \tag{3.1c}$$

C_i is the capacitance of the gate dielectric, N_a is the substrate doping concentration, x_{dmax} is the maximum width of the equilibrium surface depletion layer at inversion, and qV_F is the Fermi level position relative to the intrinsic level in the semiconductor substrate.

Positive bias, $+V_D$, applied to the drain terminal will reverse bias the n^+ drain region with respect to the p-type substrate, and the current flow between the two is limited to the leakage current of the junction. In high quality structures, this leakage current will be negligible. In contrast to this low current, the drain bias will also promote the flow of an electron drift current, in the electron rich inversion layer, between the sources and drain terminals. At the drain end of the channel, the electrons will be swept through the reverse biased drain space charge region into the drain junction.

When the drain bias, V_D, is low (and significantly less than $V_G - V_T$), then V_D will be uniformly dropped along the channel inversion layer, resulting in both a constant field V_D/L and the flow of an ohmic electron current, I_d, between the source and drain contacts. (Due to the n^+ doping of these regions, it is assumed that there is negligible voltage drop within these regions themselves). This is defined as the *linear regime* of device behaviour.

As V_D is increased, the ohmic channel current increases, and, eventually, V_D reaches a value where, although it is still less than $V_G - V_T$, it is of the same order (e.g. $> \sim 5$–10%). As this happens, the potential at the drain end of the channel needs to be taken into account when computing the inversion charge density along the channel. For instance, at the drain end of the channel, the voltage drop across the oxide between the inversion layer and the gate electrode is now $V_G - V_T - V_D$, whereas it remains at $V_G - V_T$ at the source end of the channel. Hence, there is a progressive reduction in Q_n along the channel, and, to maintain current continuity, there will be corresponding field redistribution along the channel, with it increasing more at the drain than at the source as V_D is increased. The current now no longer increases linearly with V_D, but becomes sub-linear, and the device behaviour moves from the linear regime. This situation is illustrated in Fig. 3.2b. Moreover, in order to maintain charge neutrality between the charge on the gate, Q_G, and the charge in the semiconductor, the reduction in Q_n will be balanced by an increase in Q_b, such that the thickness of the ionised acceptor space charge layer increases beyond the thermal equilibrium value of x_{dmax} (Eqs. 3.1b, and 2.18). This is shown qualitatively, in Fig. 3.2b, by the progressive widening of the space charge region beneath the channel. As shown by Eqs 3.1b and 2.18, the value of x_{dmax} is given by:

$$x_{d\max} = \sqrt{\frac{2\varepsilon_0\varepsilon_s 2V_F}{qN_a}} \tag{3.2}$$

Hence, for the depletion width to increase beyond this value, the amount of band bending has to increase beyond $2V_F$, and it progressively increases along the channel from $2V_F$ at the source to $2V_F + V_D$ at the drain. The qualitative changes in the charge distributions and the band bending, at the source and drain ends of the channel, are shown in Fig. 3.3a–d. As shown in Fig. 3.3d, the bias at the drain results in a non-thermal equilibrium situation, with the thermal equilibrium Fermi level splitting into separate hole and electron quasi Fermi levels, E_{Fp} and E_{Fn}, respectively, which are separated by V_D. Hence, this diagram shows physically why the band bending, V_s, has to be increased to $2V_F + V_D$ at the drain: it is to bring the intrinsic level at the surface to qV_F below the electron quasi-Fermi level at the drain [1, 2]. This is the condition required to invert the p-type surface of a reverse-biased gated n^+-p diode [2], and is the direct analogue of the thermal equilibrium situation (discussed in Sect. 2.2), in which inversion occurs when the intrinsic level is qV_F below the equilibrium Fermi level.

Finally, as shown in Fig. 3.2c, when $V_D = V_G - V_T$, Q_n is reduced to zero at the drain, and channel is *pinched-off*. However, as all electrons arriving at the edge of the drain space charge region are swept through it into the drain, this does not pinch-off the current, but causes it to saturate, and the device operation moves into the *saturation regime*. The voltage at which this happens is the *saturation voltage*, $V_{D(sat)}$. The current saturation occurs because, in principle, the maximum possible potential difference, $V_{D(sat)}$, has been dropped along the channel, and the pinch-off voltage remains at $V_{D(sat)}$ even when V_D is increased. However, in reality, as V_D is increased, the drain space charge region grows, and the pinch-off point moves towards the source. Hence, even though the total voltage drop along the channel remains at $V_{D(sat)}$, the effective channel length shortens, and the mean channel field increases. This is shown in Fig. 3.2d, and this increase in field leads to a corresponding increase in the saturation current. Since pinch-off occurs at $V_D = V_{D(sat)} = V_G - V_T$, increasing V_G leads to a corresponding increase in $V_{D(sat)}$. This causes the saturation current to increase as $(V_G - V_T)^2$, due to the correlation of $V_{D(sat)}$ with V_G. The detailed voltage dependence of the current is discussed in the following section.

The experimental MOSFET output characteristics [1] in Fig. 3.4 illustrate the key features described above: in particular, the linear and saturation regimes, the increasing values of the saturation voltage, $V_{D(sat)}$, with increasing V_G, and the finite output impedance in saturation.

3.3 Current-Voltage Equations

3.3.1 Simplified Format

With reference to Fig. 3.2b–d, the current density, J_D, at any point x, y in the channel is given by:

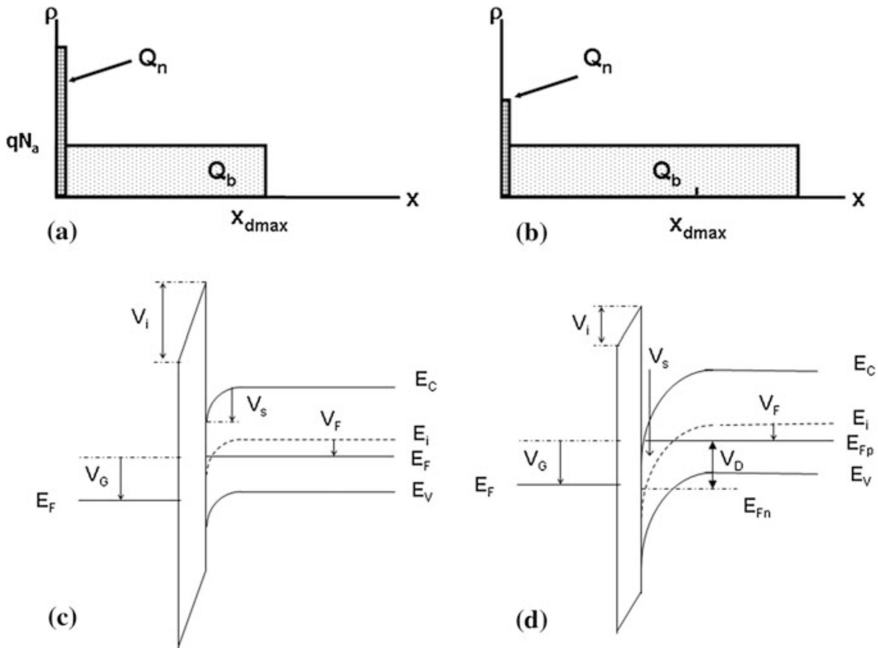

Fig. 3.3 Inversion, Q_n, and depletion layer, Q_b, charge densities at different positions in the channel, for V_D less than, but of the same order as, $V_G - V_T$: **a** at the source, **b** at the drain. Corresponding band bending diagrams at (**c**) the source, and (**d**) drain ends of the channel

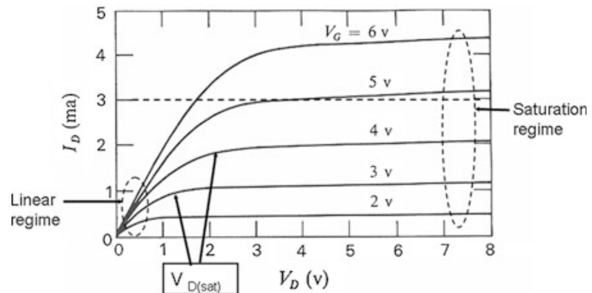

Fig. 3.4 Experimental MOSFET output characteristics showing the linear and saturation operating regimes, as well as the finite output impedance (W/L = 25). (Reproduced from [1] with permission of John Wiley & Sons, Inc)

$$J_D = \sigma_n(x, y)F(y) \tag{3.3}$$

where y is the direction of current flow, x is the direction perpendicular to the Si/ SiO_2 interface, σ_n is the local electron conductivity, and F is the local field in the direction of current flow. The conductivity, σ_n, is given by:

$$\sigma_n(x, y) = q\mu_n n(x, y) \tag{3.4}$$

The current $I_d(y)$, at position y, is given by integrating the electron density, n, over the depth of the channel (from the Si/SiO_2 interface to the point x_i at which $n = n_i$), and across the width of the channel, W, i.e.

$$I_d(y) = W\int_0^{x_i} \sigma(x,y)F(y)dx = -W\int_0^{x_i} q\mu_n n(x,y)\frac{dV(y)}{dy}dx$$
$$I_d(y) = -q\mu_n W\frac{dV(y)}{dy}\int_0^{x_i} n(x,y)dx \tag{3.5}$$

where it is assumed that the electron mobility is independent of the field in both the x and y directions, and V(y) is the potential in the channel at point y. As discussed in Sect. 2.2, for an inverted surface, the areal charge in the inversion layer can be represented by Q_n, where Q_n is the integral of the volume electron concentration through the depth of the channel, i.e.

$$q\int_0^{x_i} n(x,y)dx = Q_n(y) \tag{3.6}$$

and Q_n is related to the gate bias, V_G, by:

$$Q_n(y) = -C_i[V_G - V_T - V(y)] \tag{3.7}$$

Substituting Eqs. 3.6 and 3.7 into Eq. 3.5 gives:

$$I_d = -\mu_n W\frac{dV}{dy}Q_n(y) = \mu_n WC_i\frac{dV}{dy}[V_G - V_T - V(y)] \tag{3.8}$$

Integrating y along the channel from 0 to L, and V(y) from 0 to V_D:

$$\int_0^L I_d \mathrm{d}y = \mu_n WC_i\int_0^{V_D} [V_G - V_T - V(y)]\mathrm{d}v \tag{3.9}$$

For current continuity, I_d is independent of position within the channel, hence:

$$I_d = \frac{\mu_n WC_i}{L}\left[(V_G - V_T)V_D - 0.5V_D^2\right] \tag{3.10}$$

This is the classical, simplified MOSFET equation, which is widely used to interpret TFT behaviour, and, in particular, to extract the carrier mobility, as discussed below.

3.3.1.1 Linear Regime

For $V_D \ll V_G - V_T$, Eq 3.10 reduces to:

$$I_d = \frac{\mu_n W C_i (V_G - V_T) V_D}{L} \tag{3.11}$$

Equation 3.11 describes the current-voltage characteristics in the *linear regime* (in which the current increases linearly with V_D), and the electron mobility is derived from the slope of an experimentally measured $I_d - V_G$ transfer characteristic, using:

$$\mu_n = \frac{L}{W C_i V_D} \frac{dI_d}{dV_G} \tag{3.12}$$

An example of a linear regime plot is shown in Fig. 3.5, in which a straight line has been put through the data points having the maximum slope, from which the mobility can be obtained. The extrapolation of this line onto the x-axis gives the threshold voltage, V_T, and this procedure is widely used in extracting these two parameter values from TFT transfer characteristics.

The transconductance of the device, g_m, is given by:

$$g_m \equiv \frac{dI_d}{dV_G} = \frac{\mu_n W C_i V_D}{L} \tag{3.13}$$

and the channel conductance, g_d, is:

$$g_d \equiv \frac{dI_d}{dV_D} = \frac{\mu_n W C_i (V_G - V_T)}{L} \tag{3.14}$$

The mobility derived from Eq. 3.12 is the *field effect mobility*, and the above analysis implicitly assumes that all the charge induced in the semiconductor surface by the gate bias, V_G, is composed entirely of free electrons, which contribute

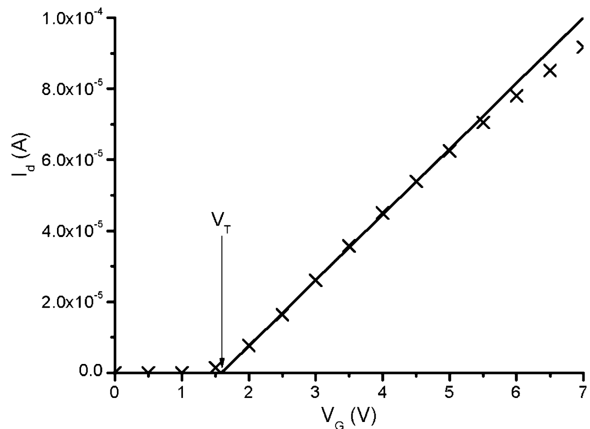

Fig. 3.5 Experimental, linear regime transfer characteristic, showing the best fit straight line (from which the carrier mobility can be calculated), and the extrapolation of the line onto the x-axis to give V_T

to the current as specified by Eq. 3.8. However, using Eq. 2.22, the general relationship between V_G and the charge in the semiconductor surface is:

$$V_G = V_s - Q_s/C_i = 2V_F - (Q_n + Q_b)/C_i \tag{3.15}$$

and differentiating by V_G gives:

$$\frac{dQ_n}{dV_G} = -\left(C_i - \frac{dQ_b}{dV_G}\right) \tag{3.16}$$

Hence, if dQ_b/dV_G is zero, then all the induced charge is, indeed, free inversion layer charge (as assumed above for a MOSFET). But, as will be discussed in the TFT chapters, the TFTs are usually found to have a distribution of trapping states across the band gap, such that there may be continuous partitioning of the induced charge between free carriers and carriers being trapped in the band-gap states. In this case, dQ_b/dV_G is not zero, and $dQ_n/dV_G < C_i$, which means that the *field effect mobility* (derived from Eq. 3.12, by assuming that all the induced surface charge is free charge) will be less than the actual free carrier mobility. This is discussed further in Chap. 6

3.3.1.2 Saturation Regime

For $V_D = V_G - V_T = V_{D(sat)}$, the current saturates at $I_{d(sat)}$, and Eq. 3.10 reduces to:

$$I_{d(sat)} = \frac{\mu_n W C_i (V_G - V_T)^2}{2L} \equiv \frac{\mu_n W C_i V_{D(sat)}^2}{2L} \tag{3.17}$$

Hence, in saturation, the current increases quadratically with $V_G - V_T$ because the inversion charge increases by this amount, as does the maximum potential drop along the channel. As in the linear regime, the field effect mobility may be obtained from experimental $I_d - V_G$ data in saturation (such as measurements at $V_D = 5$ V for the data in Fig. 3.4, for example), by taking the slope of the $\sqrt{I_d} - V_G$ plot, and using the relationship in Eq. 3.17 to give:

$$\mu_n = \frac{2L}{WC_i}\left(\frac{d\sqrt{I_d}}{dV_G}\right)^2 \tag{3.18}$$

The carrier mobility is once again the field effect mobility, and the same qualifications, as discussed in the linear regime, apply to the mobility extracted in the saturation regime. Also, as in the linear regime, the intercept with the x-axis of the line used to calculate the mobility gives the threshold voltage.

The saturation regime transconductance is:

$$g_{m(sat)} = \frac{\mu_n W C_i (V_G - V_T)}{L} \tag{3.19}$$

3.3.2 Full MOSFET Equation

In Eq. 3.7, the role of the substrate doping density was implicitly ignored in relating the channel potential to the gate bias, which is equivalent to taking the substrate doping density as zero. For a realistically doped substrate, the doping density needs to be taken into account, and Eq. 3.7 should be rewritten as:

$$Q_n(y) = Q_s(y) - Q_b(y) \tag{3.20}$$

Where, from Eq. 2.13, $Q_b(y)$ is

$$Q_b(y) = -\sqrt{2q\varepsilon_0\varepsilon_s N_a V_s(y)} \tag{3.21}$$

From Eq. 2.22, the relationship between the gate voltage and the surface potential, V_s, is:

$$V_G = V_s(y) - Q_s(y)/C_i \tag{3.22}$$

For $V_G > V_T$, at any point in the channel, $V_s(y)$ is given by:

$$V_s(y) = 2V_F + V(y) \tag{3.23}$$

Substituting Eqs. 3.21–3.23 into Eq. 3.20:

$$Q_n(y) = -\Big(C_i(V_G - \{2V_F + V(y)\}) - [2q\varepsilon_s\varepsilon_0 N_a(2V_F + V(y))]^{0.5}\Big) \tag{3.24}$$

Substituting this into the channel current Eq. 3.8, and integrating y from 0 to L, and V(y) from 0 to V_D gives:

$$I_d L = \mu_n W \int_0^{V_D} \Big\{C_i(V_G - \{2V_F + V(y)\}) - [2q\varepsilon_s\varepsilon_0 N_a(2V_F + V(y))]^{0.5}\Big\} \mathrm{d}V \tag{3.25}$$

$$I_d = \frac{\mu_n W C_i}{L}\left\{\left[V_G - \left\{2V_F + \frac{V_D}{2}\right\}\right] V_D - \frac{2}{3}\frac{[2q\varepsilon_s\varepsilon_0 N_a]^{0.5}}{C_i}\left[(V_D + 2V_F)^{1.5} - (2V_F)^{1.5}\right]\right\} \tag{3.26}$$

3.3.2.1 Linear Regime

For $V_D \ll V_G - V_T$, and expanding $(V_D + 2V_F)^{1.5}$ as a power series, in which quadratic and higher powers of V_D are ignored:

$$(V_D + 2V_F)^{1.5} \cong (2V_F)^{1.5} + 3/2 V_D (2V_F)^{0.5} \tag{3.27}$$

and Eq. 3.26 reduces to:

$$I_d = \frac{\mu_n W C_i}{L}(V_G - V_T)V_D - 0.5V_D^2 \cong \frac{\mu_n W C_i}{L}(V_G - V_T)V_D \tag{3.28}$$

In other words, in the linear regime, Eq. 3.26 becomes the same as the simple expression 3.11, and Eq. 3.28 is equally valid for extracting the linear regime field effect mobility. The commonality of Eqs. 3.11 and 3.28 is not surprising given that it has been argued that the effects of the substrate doping level only become significant when V_D is comparable to $V_G - V_T$, causing the value of Q_b to start to increase along the channel.

3.3.2.2 Saturation Regime

The saturation voltage can be determined from Eq. 3.24 by putting $Q_n(L) = 0$ when $V(L) = V_{D(sat)}$ [1]. This directly gives the following expression for $V_{D(sat)}$:

$$V_{D(sat)} = V_G - 2V_F - \frac{\sqrt{2q\varepsilon_s\varepsilon_0 N_a\left(V_{D(sat)} + 2V_F\right)}}{C_i} \tag{3.29}$$

Re-arranging Eq. 3.29, and solving for $V_{D(sat)}$ gives:

$$V_{D(sat)} = V_G - 2V_F + K^2\left(1 - \sqrt{1 + 2V_G/K^2}\right) \tag{3.30}$$

where,

$$K = \frac{\sqrt{q\varepsilon_s\varepsilon_0 N_a}}{C_i} \tag{3.31}$$

Equation 3.29 shows that $V_{D(sat)}$ is smaller than $V_G - V_T$ due to the inclusion of $V_{D(sat)}$ itself in the square root term (without this inclusion, $V_{D(sat)}$ would just be equal to $V_G - V_T$). A direct consequence of the reduction in $V_{D(sat)}$ is that the saturation current, at a given value of $V_G - V_T$, will be smaller than the value given by Eq. 3.17 using the simple analysis.

The physical meaning of Eq. 3.29 can be more easily understood by re-arranging it in terms of the value of the gate bias, $V_{G(sat)}$, at which the channel will just be pinched off at a given value of V_D (for V_G greater than this value, the channel will not be pinched off) i.e:

$$V_{G(sat)} = 2V_F + V_D + \frac{\sqrt{2q\varepsilon_s\varepsilon_0 N_a(V_D + 2V_F)}}{C_i} \tag{3.32}$$

In other words, $V_{G(sat)}$ is the gate threshold voltage for inverting the p-type surface adjacent to an n^+ p junction, which is reverse biased with a potential V_D. This also shows that the larger the value of N_a, the greater $V_{G(sat)}$ is for a given

value of V_D (and conversely, the smaller $V_{D(sat)}$ is for a given value of V_G). This is just an extension of the thermal equilibrium threshold voltage condition discussed in Sect. 2.2.2, in which the threshold voltage increased with $\sqrt{N_a}$. What has been added here is that, in the presence of a reverse biased junction, the band bending for inversion is no longer just $2V_F$ but $2V_F + V_D$.

The quantitative impact of the substrate doping level, N_a, on $V_{D(sat)}$ is shown in Fig. 3.6, in which $V_{D(sat)}$ is plotted as a function of $V_G - V_T$ for different dopant concentrations (and for a gate oxide thickness of 40 nm). A line of unity slope ($V_{D(sat)} = V_G - V_T$) has been plotted in order to indicate the displacement of $V_{D(sat)}$ from the simple condition of $V_G - V_T$, and only the substrate doped with 10^{15} acceptors/cm^3 is a close fit. In contrast, for a substrate doped with 10^{17} acceptors/cm^3, $V_{D(sat)}$ is only 4.9 V when $V_G - V_T$ is 8 V; hence, there is a substantial reduction in the saturation voltage at this substrate doping level, and a corresponding reduction in the saturation current, as shown in Fig. 3.7. This figure plots the saturation currents, calculated from Eqs. 3.26 and 3.30, for substrates doped with 10^{15} and 10^{17} acceptors/cm^3, in which the more heavily doped substrate shows a smaller saturation current at any given value of V_G. Part of this difference is due to the higher threshold voltage in the 10^{17} cm^{-3} doped substrate, but, even after allowing for this, the current is still 38 % less at $V_G - V_T$=10 V. However, the quadratic dependence of $I_{d(sat)}$ on V_G is still maintained, as shown by the plots of $\sqrt{I_{d(sat)}}$, due to the continued scaling of $V_{D(sat)}$ with V_G, albeit at a lower rate as N_a increases. This is apparent from the reducing slopes of the $\sqrt{I_{d(sat)}} - V_G$ plots in Fig. 3.7, and, if Eq. 3.18 is used to extract the field effect mobility from these plots, the apparent mobility decreases with increasing substrate doping. (For the curves in Fig. 3.7, a mobility of 500 cm^2/Vs was used to calculate the saturation currents, but the extracted values were 469 and 316 cm^2/Vs for the 10^{15} and 10^{17} cm^{-3} doped substrates, respectively). Hence, the simple analysis underlying Eq. 3.18 is likely to underestimate the carrier mobility in saturation.

As shown diagrammatically in Sect. 3.2, the space charge region beneath the conducting channel significantly widens between the source and the drain ends of the channel under drain saturation conditions. Equation 3.2 can be modified to include the influence of the drain saturation voltage on the space charge width, x_{dD}, at the drain end of the channel, which is given by:

$$x_{dD} = \sqrt{\frac{2\varepsilon_0\varepsilon_s\left(2V_F + V_{D(sat)}\right)}{qN_a}} \tag{3.31}$$

Figure 3.8 is a plot of x_{dD} as a function of $V_{D(sat)}$ for different substrate doping levels (where the zero bias value of x_{dD} is also the space charge width at the source end of the channel). For $N_a < 10^{17}$ cm^{-3}, the surface space charge width at the drain is greater than 100 nm, which is significant for TFTs with film thickness values less than this, as discussed in Sect. 3.5.

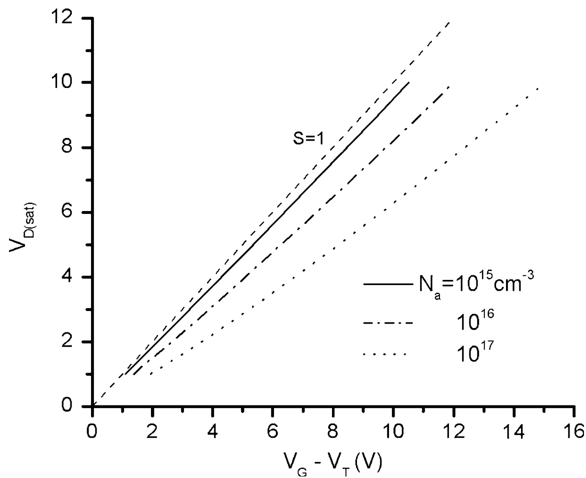

Fig. 3.6 Calculated values of the drain saturation voltage, $V_{D(sat)}$, as a function of $V_G - V_T$, for different substrate doping levels, and for a gate oxide thickness of 40 nm. (The line of slope S=1 illustrates the divergence of $V_{D(sat)}$ from the simple relationship $V_{D(sat)} = V_G - V_T$)

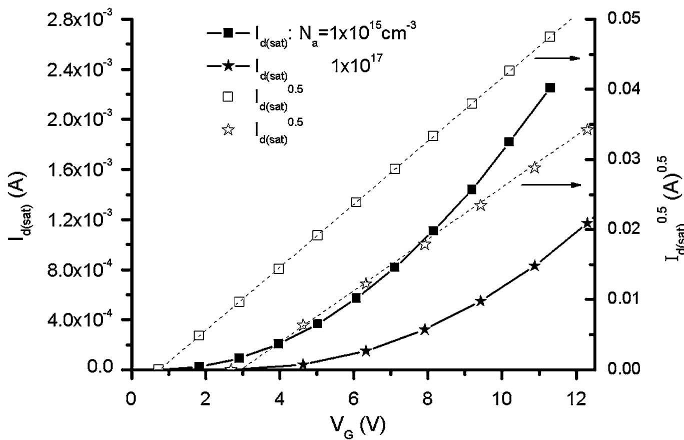

Fig. 3.7 Calculated saturation regime $I_{d(sat)} - V_G$ characteristics, for different substrate doping levels, and the associated plots of $\sqrt{I_{d(sat)}}$ vs. V_G (W/L = 1, t_{ox} = 40 nm)

3.3.3 Non-ideal MOSFET Behaviour

The preceding discussions have assumed that the threshold voltage is determined just by the substrate doping level, so that its numerical value is positive for n-channel TFTs and negative for p-channel TFTs. That is to say both channel types are in the off-state at zero gate bias. This type of transistor is referred to as an *enhancement device*. However, as discussed in Sect. 2.2.3, real MIS structures will have some, or

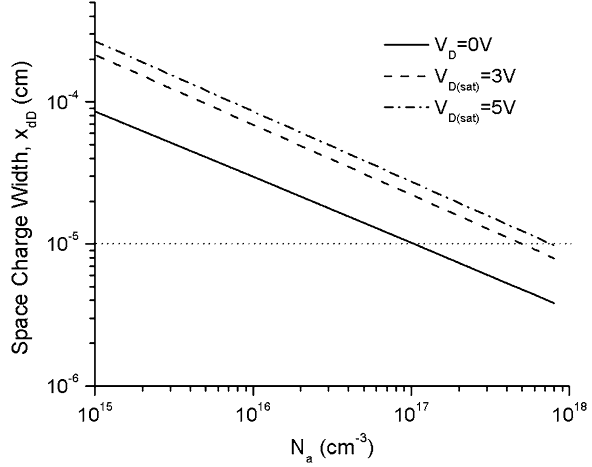

Fig. 3.8 Surface depletion layer thickness, x_{dD}, at the threshold of surface inversion, as a function of substrate doping level, and at different values of $V_{D(sat)}$

all, of the following artefacts: work function differences, Φ_{MS}, between the metal gate and the semiconductor, fixed charges in the dielectric, Q_{ieff}, and charges, $Q_{ss}(V_s)$, in the interface states, $N_{ss}(E)$, at the semiconductor/dielectric interface. These will produce a non-zero flat band voltage, V_{FB}, given by Eq. 2.38b:

$$V_{FB} = \Phi_{MS} - Q_{ieff}/C_i - Q_{ss}(V_s = 0)/C_i \tag{3.32}$$

which needs to be accounted for in the calculation of the device's threshold voltage, given by Eq. 2.28:

$$V_T = V_{FB} + \frac{\sqrt{2q\varepsilon_0\varepsilon_s N_a 2V_F}}{C_i} + 2V_F \tag{3.33}$$

If V_{FB} is sufficiently negative (due, for instance, to a large positive fixed charge density in the dielectric), and larger than the other two terms in Eq. 3.33, then the threshold voltage for an n-channel device, will be negative, and the device will be in the on-state at zero gate bias. This is referred to as a *depletion device*. (A *depletion p-channel device* would have a positive threshold voltage).

The threshold voltage shift due to the work function difference and the fixed oxide charge will both simply displace the MOSFET on-state $I_d - V_G$ characteristic along the gate voltage axis without changing its shape. In addition, for fixed charge alone, the shift will be the same for both n- and p-channel transistors. However, for interface states, whose occupancy changes with band bending, and, hence, with gate bias above V_T, their effect will be to reduce the slope of the linear $I_d - V_G$ characteristics for both channel types, so that they are displaced away from each other. The analysis of those curves using Eq. 3.12 will show an apparent reduction in carrier mobility, due to the violation of the underlying assumption in this equation that all charge induced by the gate voltage above V_T is free charge in the channel. (In the presence of interface states, the induced charge is partitioned

between the free carriers in the channel and carriers trapped up to the Fermi level in the interface states).

3.4 Sub-Threshold Currents

The MOSFET equations developed above have been derived for gate voltages in excess of the threshold voltage, which has been defined to occur at a band bending value of $2V_F$ (where the volume concentration of minority carriers at the surface is equal to the volume concentration of the majority carriers in the bulk). In addition, for band bending greater than $2V_F$, the surface charge is dominated by the free carriers, whereas, for band bending less than this, the surface charge is dominated by the ionised dopant space charge. However, within this latter regime, the minority free carrier density at the surface is increasing exponentially with band bending by several orders of magnitude from n_i^2/N_a, at flat bands, to N_a at the threshold voltage (assuming an n-channel device, with the substrate doped with an acceptor density N_a). The sub-threshold regime describes the contribution of these carriers to current flow in the device for gate voltages less than the threshold voltage.

To a first order in the gradual channel approximation, the gate-bias-induced fixed space charge screens the free carriers from the drain field, so that the drift current is assumed to be zero. However, free electrons adjacent to the positively biased drain region will be swept through the drain space charge region, and into the drain. If the drain space charge region is regarded as a perfect electron sink, then the volume surface electron concentration, n_s, at the drain will be approximately zero, and independent of V_D for $V_D > 3kT/q$ [3, 4]. At the source, it will be n_i^2/p_s, where $p_s = N_a \exp - V_s/kT$, and V_s is the surface band bending. Hence, there will be a carrier gradient along the channel, driving a sub-threshold diffusion current, I_d, which, for current continuity, requires the gradient to be constant. The diffusion current, I_d, is given by [3]:

$$I_d = qQ_{sn}WD_n/L \tag{3.34}$$

where Q_{sn} is the areal electron concentration at the source end of the device, and D_n is the electron diffusion coefficient, which is given by the Einstein relationship as $\mu_n kT/q$. The areal electron concentration, Q_{sn}, is the integral (in the x-direction) of the electron concentration through the depletion region, i.e.:

$$Q_{sn} = \int_0^{x_d} n(x)\mathrm{d}x = \int_{V_s}^{0} n(V)\frac{\mathrm{d}x}{\mathrm{d}V}\mathrm{d}V \tag{3.35}$$

Due to the band bending, V(x), within the depletion region, the electron concentration rises exponentially from its value n_i^2/N_a at the edge of the space charge region ($x = x_d$ and $V = 0$) to the following value at any point x in the space charge region, where the band bending is V(x):

$$n(V) = (n_i^2/N_a)\exp qV(x)/kT \tag{3.36}$$

The field, dV/dx, can be derived from Eq. 2.13 as:

$$\frac{dV}{dx} = \sqrt{\frac{2qN_aV}{\varepsilon_0\varepsilon_s}} \tag{3.37}$$

Hence, substituting Eqs. 3.36 and 3.37 into 3.35:

$$Q_{sn} = \frac{n_i^2}{N_a}\sqrt{\frac{\varepsilon_0\varepsilon_s}{2qN_a}}\int_{V_s}^{0}\left(V^{-0.5}\exp qV/kT\right)\mathrm{d}V \tag{3.38}$$

For $2V_F > V_s > kT$, an approximate analytical solution to Eq. 3.38 has been obtained by integrating just the dominant exponential term, and evaluating $V^{-0.5}$ at the integration limits [4], giving:

$$Q_{sn} \approx \frac{kTn_i^2}{qN_a}\sqrt{\frac{\varepsilon_0\varepsilon_s}{2qN_aV_s}}\exp\frac{qV_s}{kT} \tag{3.39}$$

Substituting Eq. 3.39 into 3.34 gives the sub-threshold current:

$$I_d \approx \frac{q\mu_nW}{L}\left(\frac{kT}{q}\right)^2\frac{n_i^2}{N_a}\sqrt{\frac{\varepsilon_0\varepsilon_s}{2qN_aV_s}}\exp\frac{qV_s}{kT} \tag{3.40}$$

This can be related to the gate bias, V_G, by Eqs. 2.13 and 2.22:

$$V_G = V_s + \frac{\sqrt{2q\varepsilon_0\varepsilon_sN_aV_s}}{C_i} \tag{3.41}$$

Equations 3.40 and 3.41 can be evaluated as a function of V_s, and the resulting $I_d - V_G$ characteristics rise exponentially with V_G [3, 4] as shown in Fig. 3.9. The results in this figure were calculated for different values of N_a, and display two important features. Firstly, that the currents rise with an approximately constant slope over several orders of magnitude, and, secondly, that this slope decreases with increased substrate doping level. Given these features, the sub-threshold regime is characterised by the inverse slope, S, of the log I_d − linear V_G plot, which has the units of volts/decade, and is the number of volts required to change the current by one decade. This procedure is widely used in the characterisation of TFTs, and, for a given value of the gate capacitance, C_i, the higher the device quality, the smaller is S.

The physical significance of this measurement can be seen by differentiating Eq. 3.40 by V_G:

$$\frac{d\log I_d}{dV_G} = \frac{d\log I_d}{dV_s}\cdot\frac{dV_s}{dV_G} \tag{3.42}$$

where, from Eq. 3.41:

$$\frac{dV_G}{dV_s} = 1 + \frac{1}{C_i}\sqrt{\frac{q\varepsilon_0\varepsilon_s N_a}{2V_s}} \tag{3.43}$$

The capacitance of the depletion layer, C_s, is given by:

$$C_s = \frac{\varepsilon_0\varepsilon_s}{x_d} = \sqrt{\frac{q\varepsilon_0\varepsilon_s N_a}{2V_s}} \tag{3.44}$$

Hence,

$$\frac{dV_G}{dV_s} = 1 + \frac{C_s}{C_i} \tag{3.45}$$

From Eq. 3.40:

$$\log I_d \approx \frac{q\mu_n W}{L}\left(\frac{kT}{q}\right)^2 \frac{n_i^2}{N_a}\sqrt{\frac{\varepsilon_0\varepsilon_s}{2qN_a}} - 0.5\log V_s + \frac{qV_s}{kT}\log_{10} e \tag{3.46}$$

$$\frac{d\log I_d}{dV_G} \approx \frac{q}{kT}\frac{1}{\ln 10}\cdot\left(1 + \frac{C_s}{C_i}\right)^{-1} \tag{3.47}$$

where the logV_s term has been ignored in differentiating Eq. 3.46, and $\log_{10}e$ has been replaced by 1/ln10 in Eq. 3.47. The inverse slope, S, is:

$$S \equiv \frac{dV_G}{d\log I_d} \approx \frac{kT}{q}\left(1 + \frac{C_s}{C_i}\right)\ln 10 \tag{3.48}$$

From Eq. 3.48, the inverse slope, S, will increase with C_s, and, hence, with N_a, as seen in Fig. 3.9. It will decrease with increasing C_i, and, hence, with reducing dielectric thickness, reaching a limiting minimum value of 59.5 mV/dec when $C_i \gg C_s$. Conversely, for $C_i \ll C_s$, such that $S \gg 59.5$ mV/dec, S can be approximated by:

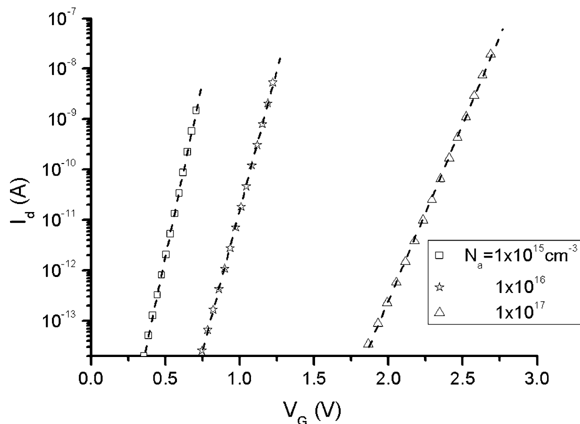

Fig. 3.9 Calculated values of the sub-threshold current, I_d, as a function of gate bias, for different substrate doping levels, and for a gate oxide thickness of 40 nm. The dashed lines are linear fits over the plotted data ranges, from which the S values are 72, 90 and 143 mV/dec for $N_a=10^{15}$, 10^{16} and 10^{17} cm^{-3}, respectively. (W/L=1)

$$S \approx \frac{kT}{q}\frac{C_s}{C_i}\ln 10 \tag{3.49}$$

and S will scale with $\sqrt{N_a}$. With high quality MOSFETs, Eq. 3.48 is likely to be the most appropriate expression, but, with the lower quality TFTs, containing a bulk distribution of trapping states across the band gap, Eq. 3.49 is a useful approximation. In this case, the value of C_s itself will be determined by the occupancy of trapping states within the forbidden band gap, and can be considered analogous to the fixed space charge density responsible for C_s in Eq. 3.44. However, in contrast to the situation with the substrate dopant, N_a, in MOSFETs (which gives a constant space charge density through the depletion region), the local density of trapped charge in a TFT will be a function of potential within the surface space charge region. Because of this, the trapping state density cannot be as readily extracted from measured values of S, but, nevertheless, the measured values of S are widely quoted as figures of merit for the TFT. The smaller S is, the higher the TFT quality is. Needless to say, in making any such comparison across different devices, the S values will need to be normalised by any differences in the dielectric capacitance between these devices.

The sub-threshold slope is also affected by interface states. In the sub-threshold regime, the surface potential V_s is changing from ~ 0 to $\sim 2V_F$, and, in the presence of interface states, $N_{ss}(E)$, their charge occupancy will also be changing over this voltage range, as they are moved below the Fermi level. Hence, for a given change in V_G, part of the induced surface charge will be trapped by the interface states, leaving a reduced amount of free charge, and concomitantly reduced band bending. The reduced amount of free charge will reduce the sub-threshold current, and S will increase. This can be seen when the influence of interface states is included in Eq. 3.48. The charging of interface states was discussed in Sect. 2.2.4, where it was shown that the interface states contribute a capacitance, C_{ss}, in parallel with the space charge capacitance. This capacitance was given by Eq 2.41:

$$C_{ss} = -\frac{dQ_{ss}}{dV_s} \sim qN_{ss} \tag{3.50}$$

Hence, in the presence of interface states, Eq. 3.48 changes to:

$$S \equiv \frac{dV_G}{d\log I_d} \approx \frac{kT}{q}\left(1 + \frac{C_s + C_{ss}}{C_i}\right)\ln 10 \tag{3.51}$$

This equation shows how S will increase with increasing interface state density, and, providing the other parameter values are known, N_{ss} can be extracted from S.

3.5 Thin Film Considerations

The MOSFET discussion in the previous sections has implicitly assumed that the substrate is sufficiently thick that there is no constraint on the thickness of the surface depletion regions. In this section, we will consider the constraints imposed by the

finite film thickness in a TFT on the device threshold voltage and saturation voltage. In using the preceding analytical equations to examine the TFT behaviour, an analogy will be drawn between the shallow dopant impurity in the MOSFET and the defect states distributed across the band gap in the TFTs. However, it should be emphasised that there is not a precise equivalence because the shallow dopant in the MOSFET is fully ionised throughout the surface space charge region, and the space charge density is simply equal to the dopant density. In contrast, the space charge density in the TFT is determined by the position of the Fermi level within the defect state distribution, and, hence, by the local band bending, V(x). In this case, the space charge density is a function of depth, x, and cannot be specified by a single value, in contrast to the dopant density, N_a, used with the MOSFET. Nevertheless, the simplicity of the analytical equations makes them useful in providing a physical insight into the broad effects of the finite film thickness in TFTs. (A more rigorous discussion of the detailed nature and impact of the TFT trapping states is presented in Chap. 6).

3.5.1 Threshold Voltage

For the thick substrate devices, the threshold voltage is defined by Eq. 3.1c:

$$V_T = 2V_F + \sqrt{(2q\varepsilon_0\varepsilon_s N_a 2V_F)}/C_i \tag{3.52}$$

Where the equilibrium depletion layer thickness beneath the channel is:

$$x_{d\max} = \sqrt{\frac{2\varepsilon_0\varepsilon_s 2V_F}{qN_a}} \tag{3.53}$$

The dependence of x_{dmax} on N_a is shown in Fig. 3.8, by the line marked $V_D = 0$ V, from which it will be seen that x_{dmax} is greater than 100 nm for substrate doping densities less than $1 \times 10^{17}\text{cm}^{-3}$. Bearing in mind the qualifications concerning precise parallels between the space charge densities in MOSFETs and TFTs, some broad conclusions can, nevertheless, be drawn for an effective space charge density, N_{TFT} (such as could be extracted from the sub-threshold slope of TFTs).

For TFTs made in films thinner than 100 nm, and with effective charge densities, N_{TFT}, less than 10^{17} cm^{-3}, the film will not be thick enough to accommodate the equilibrium space charge thickness defined by Eq. 3.53. Given that the maximum space charge width cannot exceed the film thickness, the band bending will be less than that conventionally used to define threshold voltage in Eq. 3.52. To a first approximation, the threshold voltage will be determined by the gate voltage required to fully deplete the film, and any further increase in gate bias will induce free carriers rather than increasing the depth of the space charge region (although some of these carriers may continue to be trapped). With this assumption, the modified threshold voltage, for a film of thickness T_s, will be given by:

$$V_T = qN_{TFT}T_s^2/(2\varepsilon_0\varepsilon_s) + qN_{TFT}T_s/C_i \tag{3.54}$$

where, for $T_s < x_{dmax}$, the first term is the band bending required to fully deplete the film, and the numerator in the second term is the space charge density in the fully depleted film. If the film is not fully depleted at inversion, then the normal threshold voltage expression, 3.52, can be applied.

Hence, for thin enough films, V_T is a linear function of N_{TFT}, as opposed to the $\sqrt{N_a}$ dependence found for MOSFETs, and is also a direct function of the film thickness.

3.5.2 Saturation Voltage, $V_{D(sat)}$

As discussed in Sect. 3.3.2.2, the depletion layer thickness at the drain end of the channel increases with V_D, as shown in Fig. 3.8. Clearly, if $T_s < x_{dmax}$, at the threshold of inversion, then the space charge layer thickness will be unable to grow with increasing V_D as required by Eq. 3.31 (and as qualitatively shown in Fig. 3.2). Equation 3.29 can be re-arranged to read:

$$V_G = V_{D(sat)} + 2V_F + \frac{\sqrt{2q\varepsilon_s\varepsilon_0 N_a\left(V_{D(sat)} + 2V_F\right)}}{C_i} \tag{3.55}$$

which can be put into the more general form:

$$V_G = V_{D(sat)} + V_s(V_D = 0) + \frac{Q_s}{C_i} \tag{3.56}$$

However, in the fully depleted film, the maximum areal space charge density, Q_s, is determined by the film thickness, and:

$Q_s = qN_{TFT}T_s$, and $V_s(V_D{=}0) = qN_{TFT}T_s^2/(2\varepsilon_0\varepsilon_s)$. Substituting these into Eq. 3.56 gives:

$$V_G = V_{D(sat)} + \frac{qN_{TFT}T_s^2}{2\varepsilon_0\varepsilon_s} + \frac{qN_{TFT}T}{C_i} \tag{3.57}$$

The last two terms on the right hand side of Eq. 3.57 are equal to V_T (see Eq. 3.54), and, therefore:

$$V_G = V_{D(sat)} + V_T$$

or

$$V_{D(sat)} = V_G - V_T \tag{3.58}$$

Hence, in TFTs, in which the film thickness is less than the equilibrium depletion layer thickness for surface inversion, x_{dmax}, the saturation voltage is equal to the simple, classical MOSFET value of $V_G - V_T$. This is quite different from the detailed analysis of realistically doped MOSFETs (where $V_{D(sat)} < V_G - V_T$). The simpler expression for TFTs is a consequence of the limited areal space charge density, which can be developed within the thin film, even in the presence of a high volume space charge density. Indeed, the near equality of $V_{D(sat)}$ and $V_G - V_T$ is widely observed across the range of different types of TFT, including a-Si:H [5], poly-Si [6], organic TFTs [7] and amorphous oxide TFTs [8]. The most obvious example of $V_{D(sat)} < V_G - V_T$ occurs in source-gated transistors, SGTs, [9], due to their fundamentally different mode of operation, and this is discussed in Chap. 12.

3.6 Summary

The published analyses of TFT behaviour frequently make use of simple, analytical MOSFET concepts, and, in this chapter, those concepts are explained, and the key equations developed. The physical description of MOSFET operation was used to introduce the linear and saturation operating regimes. A simple analytical model was developed from this, and contained expressions for parameters such as threshold voltage, saturation voltage, and carrier mobility, which are extensively used in analysing TFT behaviour. This simple analysis ignores the implicit effects of the substrate doping level on the saturation voltage, and a more rigorous analysis was presented to quantify this effect. This demonstrated that the saturation voltage is generally less than the value of $V_G - V_T$, which is predicted in the simple model.

The above models are valid for the on-state regime, in which the gate bias, V_G, is greater than the threshold voltage, V_T. A further operating regime is described in which $V_G < V_T$, and this is known as the sub-threshold regime. This is a low current regime, but one in which the channel current increases exponentially with gate bias (in contrast to the linear increase in the high-current, linear regime). Device operation in this regime is characterised by the sub-threshold slope, S, and this is commonly used as a figure of merit for TFT operation.

The standard MOSFET analysis implicitly assumes an infinitely thick substrate, and some of the conclusions from that analysis need to be modified in the presence of the finite film thicknesses in TFTs. The key parameter determining this is whether the film is thinner than the expected equilibrium space charge width at the point of surface inversion. When this occurs, the film thickness modifies the usual expression for threshold voltage, and the saturation voltage reduces to the simple MOSFET expression of $V_G - V_T$, as widely observed in most TFTs.

Appendix: Summary of Key Equations

A number of the simplified equations from the text, which can be used in basic analytical calculations, are reproduced below. The equation numbers are retained for quick reference back to the original derivations.

A.1 Simplified MOSFET On-State Analysis

Relationships between the drain current, and the gate and drain biases.
(a) drain current as a function of terminal biases

$$I_d = \frac{\mu_n W C_i}{L}\left[(V_G - V_T)V_D - 0.5V_D^2\right] \tag{3.10}$$

(b) threshold voltage

$$\mathrm{V_T} = 2\mathrm{V_F} + \sqrt{}(2\mathrm{q}\varepsilon_0\varepsilon_s\mathrm{N_a}2\mathrm{V_F})/\mathrm{C_i} \tag{3.1c}$$

(c) linear regime current

$$I_d = \frac{\mu_n W C_i (V_G - V_T)\, V_D}{L} \tag{3.11}$$

(d) linear regime mobility

$$\mu_n = \frac{L}{W C_i V_D}\frac{dI_d}{dV_G} \tag{3.12}$$

(e) linear regime transconductance

$$g_m \equiv \frac{dI_d}{dV_G} = \frac{\mu_n W C_i V_D}{L} \tag{3.13}$$

(f) saturation regime current

$$I_{d(sat)} = \frac{\mu_n W C_i (V_G - V_T)^2}{2L} \equiv \frac{\mu_n W C_i V_{D(sat)}^2}{2L} \tag{3.17}$$

(g) saturation regime mobility

$$\mu_n = \frac{2L}{W C_i}\left(\frac{d\sqrt{I_d}}{dV_G}\right)^2 \tag{3.18}$$

(h) saturation regime transconductance

$$g_{m(sat)} = \frac{\mu_n W C_i (V_G - V_T)}{L} \tag{3.19}$$

A.2 Simplified MOSFET Sub-Threshold Analysis

(a) sub-threshold current

$$I_d \approx \frac{q\mu_n W}{L}\left(\frac{kT}{q}\right)^2 \frac{n_i^2}{N_a}\sqrt{\frac{\varepsilon_0\varepsilon_s}{2qN_aV_s}}\exp\frac{qV_s}{kT} \tag{3.40}$$

(b) relationship between surface potential, V_s, and gate bias

$$V_G = V_s + \frac{\sqrt{2q\varepsilon_0\varepsilon_s N_a V_s}}{C_i} \tag{3.41}$$

(c) sub-threshold slope, S

$$S \equiv \frac{dV_G}{d\log I_d} \approx \frac{kT}{q}\left(1 + \frac{C_s}{C_i}\right)\ln 10 \tag{3.48}$$

(d) sub-threshold slope with interface states

$$S \equiv \frac{dV_G}{d\log I_d} \approx \frac{kT}{q}\left(1 + \frac{C_s + C_{ss}}{C_i}\right)\ln 10 \tag{3.51}$$

(e) interface state capacitance

$$C_{ss} = -\frac{dQ_{ss}}{dV_s} \sim qN_{ss} \tag{3.50}$$

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Chapter 4
Active Matrix Flat Panel Displays

Abstract The currently dominant flat panel display technology is based upon the use of liquid crystal materials to produce active matrix liquid crystal displays, AMLCDs. Other display effects, which are now appearing in commercial products, are electrophoretic displays, EPDs, in e-readers, and organic light emitting diodes, OLEDs, in some small diagonal, portable displays. The operation of all three types of display are described, although prominence is given to discussion of the operating principles of AMLCDs. The topics covered are LC effects, active matrix addressing, pixel layout and a brief overview of display performance artefacts. The treatment of EPDs and OLEDs also covers their operating principles, aspects of pixel layout and performance issues.

4.1 Introduction

This chapter deals with the operation and addressing of active matrix flat panel displays, AMFPDs, and will primarily focus on liquid crystal displays. The active matrix LCD is currently the most commercially significant display technology, offering products across the size range from $\sim 1''$ portable displays through to $100''$ TVs, as illustrated in Fig. 4.1. The annual revenue of the AMLCD industry in late 2011 was $\sim$\$B86 [1], with a long-term annual growth rate of ~ 10 %. Within this market, ~ 85 % of the revenue came from larger diagonal displays for the notebook, monitor and TV markets, and the remaining 15 % from the small and medium diagonal display market, for portable products such as cell phones, portable media players, net-books and tablets [1]. The growth of this industry has been facilitated by the manufacturability of high quality thin film transistors for display addressing, and, equally, the development of the industry has stimulated the worldwide interest and research into TFTs. Among the different TFT technologies, amorphous Si TFTs dominate the current product range, although,

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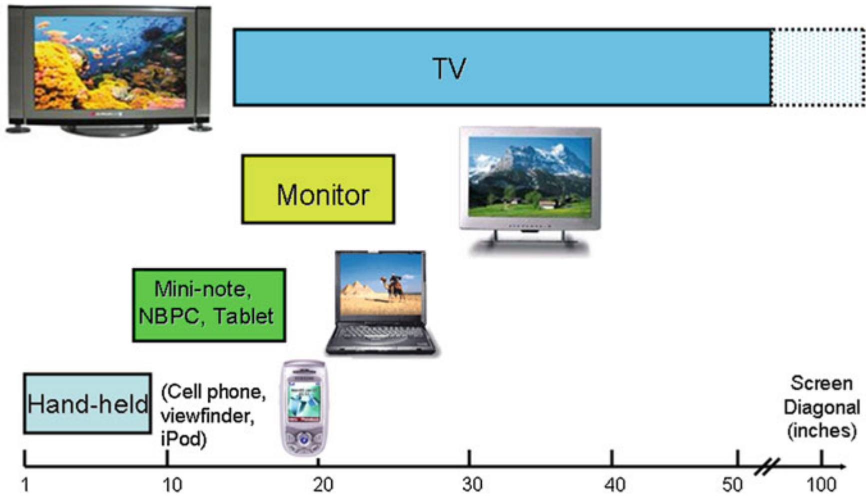

Fig. 4.1 AMLCD product applications grouped by display diagonal (the *dotted box* for LCTV illustrates the larger diagonal TVs demonstrated at electronics shows)

poly-Si TFTs are found in some of the small and medium-sized products. Also, within this latter size range, two other display technologies are emerging, in particular, electrophoretic displays, EPDs [2, 3], and organic light emitting diode displays, OLEDs [4]. The EPDs are reflective displays, with low power consumption, and are of particular relevance to e-reader devices. The current addressing devices are primarily a-Si TFTs [5], although the e-reader has also been identified as an appropriate vehicle for flexible displays, and for the use of organic addressing TFTs [6]. The OLED displays demand a higher drive current than LCDs, and the current manufacture of AMOLEDs, for products like cell-phones, has focussed on the use poly-Si TFTs for the addressing transistors [7]. There has also been strong research interest in using amorphous oxide TFTs (such as indium-gallium-zinc-oxide), rather than poly-Si TFTs, for addressing large diagonal AMOLEDs [8]. The motivation here has been the recognition that AMOLED displays are more sensitive to TFT drive current non-uniformities than AMLCDs, and the amorphous nature of the oxide TFTs is perceived as offering better uniformity than the laser crystallised poly-Si TFTs. In view of the emergence of these alternative display technologies, the operating principles of AMEPDs and AMOLEDs are also covered in this chapter.

Liquid crystal displays can operate in either the transmissive mode (illuminated by a back-light), or the reflective mode (relying upon the reflection of ambient light), or the transflective mode, where the latter is a mixture of the other two. The transmissive mode is used in the majority of applications, particularly for notebooks, monitors and TVs, whereas the other modes are more frequently employed in smaller portable displays, where power consumption and battery life are important issues. The discussion in this chapter is limited to the more wide-spread

transmissive mode. The basic operation of the LC cell is described in Sect. 4.2, and the principles of active matrix addressing (as applied to LCDs) is covered in Sect. 4.3. This is followed by a discussion of pixel layout issues in Sect. 4.4, and the principle fabrication stages of the AMLCD module are summarised in Sect. 4.5. Finally, Sect. 4.6 describes the operating principles of EPDs and AMOLEDs.

4.2 Liquid Crystal Cells

4.2.1 LC Material

A liquid crystal material is one in which there is a temperature dependent phase, which exhibits the structural organisation of a crystal, and the viscosity of a liquid. The former property results in an anisotropic refractive index and birefringence, and the latter enables the material to rapidly respond to an external influence, such as a change in an applied field. Liquid crystal materials come in a variety of forms and phases, and the type of specific interest for AMLCDs is composed of long-chain molecules, as shown in Fig. 4.2a, and by the space-filling molecular model in Fig. 4.2b [9]. This material is 4′-n-pentyl-4-cyano-biphenyl, which has a rigid biphenyl head, to give orientational order, and a flexible hydrocarbon tail which promotes the formation of a liquid crystal phase between the solid and liquid phases [9]. The length and diameter of this rod-like molecule are ~2 and 0.5 nm, respectively, giving an aspect ratio of ~4, which is typical for many LC materials. A large number of different liquid crystal structures have been engineered for

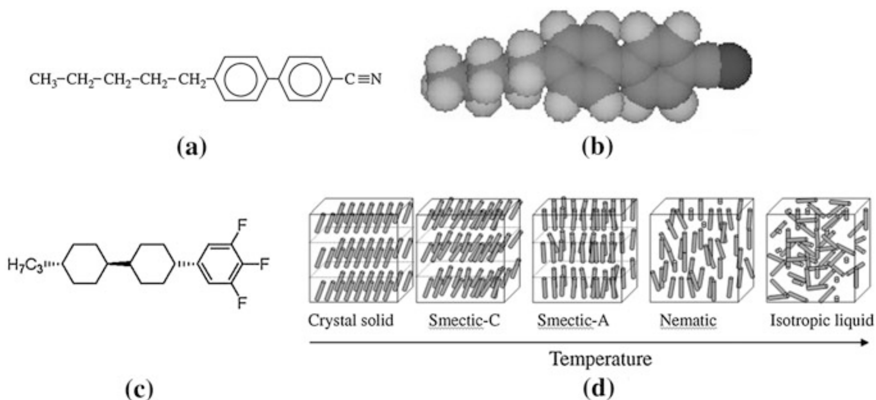

Fig. 4.2 **a** 4′-n-pentyl-4-cyano-biphenyl (5CB) LC molecule, **b** space filling model of 5CB, **c** 1,2,3 trifluorobenzene derivative molecule developed for TNLCs, and **d** temperature dependent phases of rod-like LC molecules (**a**, **b** and **d** Reproduced from [9] with permission of John Wiley & Sons, Inc, and **c** Reprinted from [10] with permission of SID)

ALMCD applications [10], and those currently favoured for AMLCDs contain fluorinated polar end groups, as shown in Fig. 4.2c [10].

Figure 4.2d schematically shows the changes of phase with temperature of rod-like LC molecules [9], from an isotropic liquid at the highest temperature, down to a crystalline solid at the lowest temperature. Between these two phase extremes, intermediate liquid crystal phases are shown, with the nematic phase being the highest temperature one, and the clearing point of the material is defined as the temperature at which the isotropic liquid forms. In the nematic phase, the molecules have orientational order, but no positional order. In other words, the long axis of the molecules is aligned predominantly in the same direction, which is called the liquid crystal director, but there is no further ordering within this direction. At a lower temperature, the smectic-A phase can arise, where the orientational ordering of the nematic phase is preserved, but there is now some positional ordering of the aligned molecules into layers, although there is no further positional ordering within the layers themselves. For this phase, the liquid crystal director is perpendicular to the layers. Some materials display further ordering into the smectic-C phase, in which the director is now at an angle to the layer. The nematic phase has lower viscosity than the grease-like smectic phases, and is the preferred material for LCDs, although it should be added that the nematic materials are synthesized compounds containing a number of constituent mixtures rather than being a single, simple LC material. Indeed, for a given application, the constituent parts are used to optimise the properties of the material, such as clearing point, speed of response or reduced driving voltages etc. [10]. For the practical application of these materials in AMLCDs, the nematic LC phase needs to be stable from ~ -40 °C to ~ 100 °C, have high resistivity, fast response times, specific dielectric properties, and excellent chemical stability [10].

The directional alignment of the LC molecules in Fig. 4.2d makes the material dielectrically and optically anisotropic [9], and, in this case, the optical axis is parallel to the direction of the LC director. Due to the anisotropy, the material has different dielectric constants for electric fields parallel and perpendicular to the director, and the difference in dielectric constants, $\Delta\varepsilon$, is given by $\Delta\varepsilon = \varepsilon_{//} - \varepsilon_{\perp}$. The dielectric anisotropy is necessary for the LC director to change direction with electric field, which is an essential aspect of the operation of the LC cell. For the materials of interest in AMLCDs, $\varepsilon_{//}$ and $\varepsilon_{\perp}$ are of the order ~ 10 and ~ 4, respectively. Similarly, there are different refractive indices for light polarised parallel to the optical axis, $n_{//}$, and perpendicular to it, $n_{\perp}$. Material with this optical property is known as birefringent, and the birefringence, Δn, is given by $\Delta n = n_{//} - n_{\perp}$ [9]. Depending upon the relative sizes of the two refractive indices, Δn can be positive or negative, and, for the nematic materials of interest to AMLCDs, positive Δn materials are more generally used. Birefringent materials change the polarisation state of polarised beams of light passing through them, when the angle of incidence is between 0° and 90° with respect to the direction of the LC director (the optical axis). This change of polarisation is exploited in AMLCDs, using a particular form of nematic cell structure, known as a *twisted nematic cell* [11].

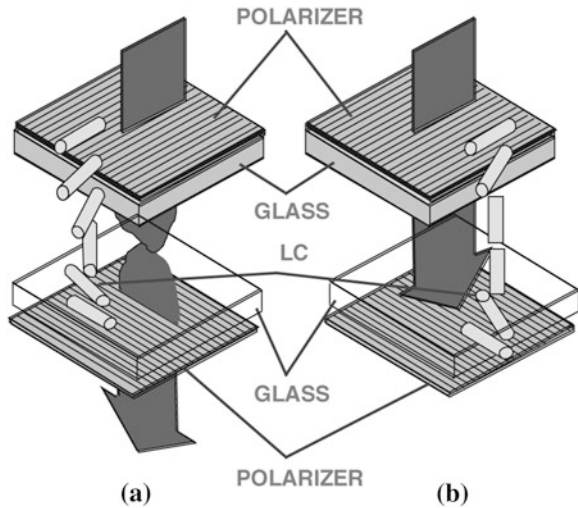

Fig. 4.3 TN LC cell structure (**a**) transmitting state, with zero applied bias across LC, and (**b**) black state, due to LC bias voltage (Reproduced from [9] with permission of John Wiley & Sons, Inc)

4.2.2 Twisted Nematic LC Cell Structure

The structure of a twisted nematic, TN, cell is shown in Fig. 4.3, which consists of a 4–6 μm thick liquid crystal layer sandwiched between two glass plates. The inner surfaces of the plates are coated with a transparent metal conductor, such as indium tin oxide, ITO, so that an electrical bias can be applied across the liquid crystal. In addition, the outer surface of each ITO layer is coated with an LC alignment layer, such as polyimide, which is textured by rubbing, in order to anchor the rod-like nematic LC molecules to the surface in a predetermined fashion. The outer surfaces of the glass plates are sandwiched between two crossed, linear polariser plates, and the LC cell is illuminated with white light from one side of the stack, and viewed through the polariser on the other side. Hence, the light entering the cell is plane polarised, and, in the absence of the LC material, there would be no optical transmission through the cell due to the action of the crossed polarisers. However, as shown in Fig. 4.3a, the alignment layers are fabricated so that the LC directors of the molecules in immediate contact with the plates are parallel to the polarisation directions, but, because the two directions are perpendicular to each other, a 90° twist is induced in the orientation of the LC director through the cell. This induces a 90° rotation in the plane of polarisation of the light passing through the cell, so that the light is transmitted by the crossed polariser on the exiting surface of the cell, and the cell appears bright. Referring to Fig. 4.3b, when a suitable voltage is applied across the liquid crystal, the LC directors line up with the field, and the 90° twist is removed from the LC. In this case, there is no longer a rotation in the plane of polarisation of the light passing through the cell, and the light is not transmitted by the crossed polariser on the opposite face: the cell now appears dark. When the voltage is reduced back to zero, the LC molecules relax back to the 90° twist shown in Fig. 4.3a, and the speed of

this relaxation is a function of the molecular form of the LC and the cell thickness, d. For a given liquid crystal material, with a birefringence Δn, the required cell thickness, to give the 90° twist to the light in the unbiased state, is determined by the Gooch-Tarry condition [9]:

$$d\Delta n = \lambda\sqrt{\left(m^2 - 1/4\right)} \tag{4.1}$$

where m is an integer, and the thinnest cell is given by $m = 1$, so that dΔn is ~480 nm for $\lambda = 550$ nm. Thus, for d ~5 μm, the LC material needs to be engineered to have a Δn value of ~0.1.

From the above discussion of the bright and dark states, it is clear that the TN cell acts as a voltage controlled, monochromatic light valve. Moreover, intermediate voltages determine the particular value of the LC twist between 0° and 90°, and, thereby, control the detailed optical transmission of the cell, as shown by the voltage/transmission curve in Fig. 4.4. A cell having this transmission curve is referred to as *normally white* (whilst with parallel polarisers, it would be *normally black*). In this curve, the *threshold voltage* is the minimum voltage required to induce a measurable reduction in bright state transmission, and the *saturation voltage* is the minimum voltage to achieve the black state. The contrast ratio is given by the ratio of the maximum and minimum transmission values, and would typically be ~250 or more. The transmission curve in Fig. 4.4 is shown only for positive drive voltages, but it is symmetric about the y-axis for both negative and positive drive voltages. In fact, a.c. drive is always used with these LCs to avoid the electro-chemical damage to the material, which would arise from d.c. driving.

Given the monochromatic nature of the TN cell, coloured displays are achieved by passing the light from the cell through red, green and blue (RGB) coloured filters. The cell structure shown in Fig. 4.3 should be regarded as a single pixel, and a display can consist of more than a million pixels, each of which need to be individually addressed to ensure that each has the correct voltage applied to achieve the required optical transmission. In principle, this can be achieved with

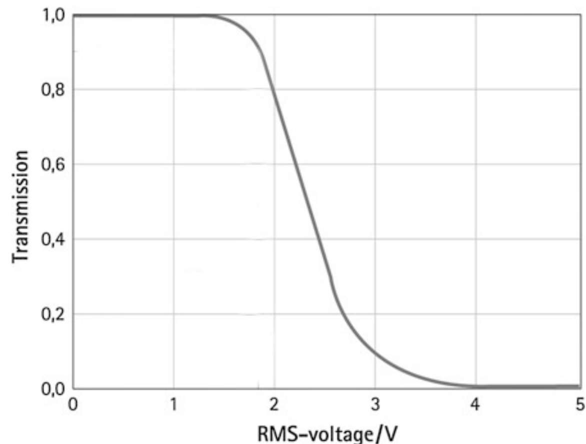

Fig. 4.4 Transmission versus voltage curve of normally white TN LC (Reprinted from [12], © Merck KGaA, Darmstadt, Germany)

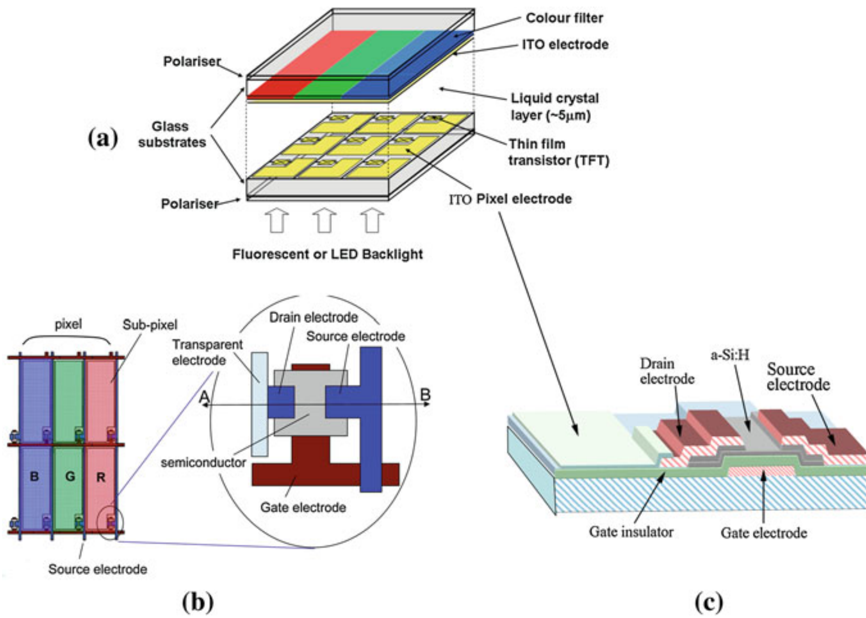

Fig. 4.5 **a** Illustration of AMLCD cell, **b** detail of pixel layout, showing TFT, **c** schematic cross-section of a-Si:H TFT (**b** and **c** reprinted with permission from [19])

'cross-wire' addressing, in which a matrix of patterned ITO addressing lines are used on one side of the display together with an orthogonal set on the other side of the display, and the combined voltage at any point will determine the optical transparency at that point. This is known as *passive matrix addressing*, but is only used in low resolution and low quality displays, because, as the number of pixels increases, the addressing time of each pixel decreases, and the image loses brightness and contrast. All present day high quality displays use *active matrix addressing*, in which there is a transistor in each pixel, as illustrated in Fig. 4.5a. This schematically shows the definition of the ITO on the bottom plate into a matrix of individual pixel areas, each of which has an addressing transistor. The ITO on the upper glass plate is unpatterned, and is often referred to as the common electrode. The coloured filters are also shown on the top plate, where they have been fabricated in a stripe arrangement (although other arrangements are also possible). In fact, each of the three pixels associated with the triad of coloured filters can be thought of as sub-pixels of the display, which is usually shown in the notation for the number of horizontal pixels in a display as N(×3), where N is related to the resolution of a display. For example, in a coloured VGA display, with a resolution of 640 × 480 pixels, there is an array of 640(×3) horizontal pixels and 480 vertical pixels. Other common display formats are listed in Table 4.1. The transistors in each pixel are used as switching devices to set the voltage across the pixel in a short addressing time, and to store it until the next refresh signal is obtained, as described in the following section.

Table 4.1 Common display formats, listing the number of rows and columns (for coloured displays)

Format	# Columns	# Rows	# Pixels	R address time (s)
VGA	640(×3)	480	921,600	3.47E−05
SVGA	800(×3)	600	1,440,000	2.78E−05
XGA	1,024(×3)	768	2,359,296	2.17E−05
WXGA	1,280(×3)	800	3,072,000	2.08E−05
SXGA	1,280(×3)	1024	3,932,160	1.63E−05
UXGA	1,600(×3)	1200	5,760,000	1.39E−05
HDTV	1,920(×3)	1080	6,220,800	1.54E−05
WUXGA	1,920(×3)	1200	6,912,000	1.39E−05
QXGA	2,048(×3)	1536	9,437,184	1.09E−05
QSXGA	2,560(×3)	2048	15,728,640	8.14E−06
QUXGA	3,200(×3)	2400	23,040,000	6.94E−06

4.3 Active Matrix Addressing

Active matrix addressing is shown schematically in Fig. 4.5a, in which the plate is patterned into an array of pixels, each one of which is addressed by its own transistor. The most widely used addressing transistor is an a-Si:H TFT: this is shown in the pixel layout in Fig. 4.5b, and in cross-section in Fig. 4.5c. Although this is a field effect transistor, like the MOSFET discussed in Chap. 3, its architecture is quite different, being a bottom-gated *inverted staggered structure*, rather than a top-gated coplanar structure. Moreover, the source and drain connections are not self-aligned to the gate electrode, but overlap it. This overlap results in a parasitic capacitance, C_{GD}, between the gate and the drain terminals, which can induce display performance artefacts, as discussed in Sect. 4.4.2.1. Further details on the design, fabrication and performance of a-Si:H TFTs are contained in Chaps. 5 and 6.

As illustrated in Fig. 4.6a, the matrix of TFTs is connected in rows and columns, with a common connection to the gate electrodes in each row, and a common connection to the source terminals in each column. The row lines carry the TFT addressing signals, and the column lines carry the data signals, V_s. The drain of each TFT is connected to its ITO pixel electrode, and the timing of the row and column voltages are shown in Fig. 4.6b and c, respectively. The high resistivity LC material is represented by a capacitor, which is charged up to the appropriate signal voltage, V_s, through its TFT. This is achieved by *line-at-a-time addressing*, during which the data signal is fed into the display in a serial row-by-row process, by sequentially switching on each row ($V_G = V_{G(on)}$), whilst holding the others in the off-state ($V_G = V_{G(off)}$). If the addressing TFTs are made from a-Si:H, they will be n-channel devices, and the row select voltages, $V_{G(on)}$, will be positive, whilst the row de-select voltages, $V_{G(off)}$, will be negative. The timing signals are related to the a.c. mains frequency, such that the display is refreshed every frame time, T_f, which will be 16.7 ms for a 60 Hz frame rate. If there are M

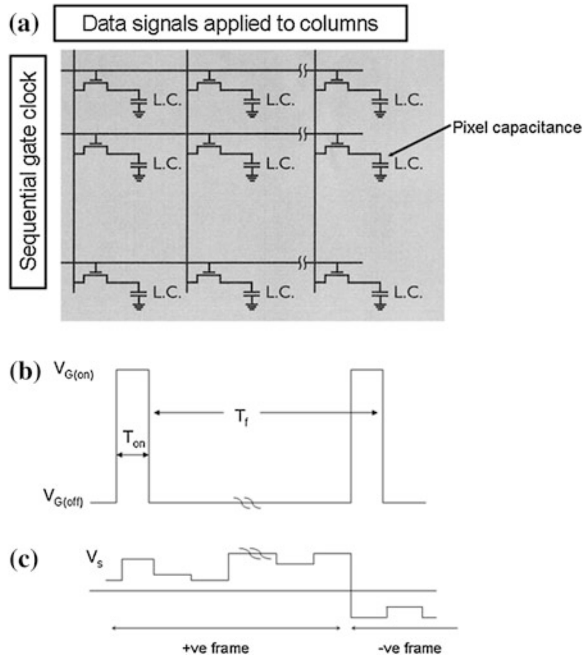

Fig. 4.6 **a** Active matrix array layout, **b** Gate line timing signal for row m, and **c** data signal waveform for column n, showing positive and negative frames

rows and N columns in the display, then the time available, T_{on}, to charge the TFTs in a given row is given by T_f/M, and this will be a function of the display format. Table 4.1 lists the row addressing times, which vary from ~35 to ~7 μs, across the range of display formats. During this interval, the signal voltages on the column electrodes of the display are applied in parallel to the common sources of the TFTs, but will charge only the one row of LC capacitors connected to the row of TFTs, which has been turned on. The on-current of the TFTs must be large enough to charge the capacitors in the time available. The maximum charge will be when the voltage is changing from +black to −black, i.e. $+V_{sat}$ to $-V_{sat}$ (or vice versa), and an approximate value of the required current is given by:

$$I_{on} > 5 \times 2V_{sat}C_{LC}/T_{on} \rightarrow (\text{for example, } I_{on} \geq 3.6 \times 10^{-7}\text{A for } C_{LC} = 0.25\text{pF}) \quad (4.2)$$

where C_{LC} is the capacitance of the LC, and the factor 5 is to ensure the full charging of the pixel. However, the charging rates for the positive and negative charging cycles are not the same, due to the influence of the data signal polarity on the source-gate bias, V_{GS}, of the TFT. For instance, when the data signal, V_s, is negative, the effective value of V_{GS} in determining the channel resistance is $V_G - V_T + V_s$, and this more negative terminal acts as the source of the n-channel TFT during the charging cycle. Conversely, for the charging cycle to a positive value of the data signal, the TFT terminal connected to the LC is now the most negative terminal, and, therefore, acts as the source. In this case, as the pixel capacitance

charges, its voltage, V_{LC}, changes from $-V_s$ to $+V_s$, which effectively reduces V_{GS}, so that, at the end of the charging cycle, V_{GS} is $V_G - V_T - V_s$. Hence, the positive charging cycle is slower than the negative charging cycle, because V_{GS} is fixed at $V_G - V_T + V_s$ during the negative charging cycle, but reduces from $V_G - V_T + V_s$ to $V_G - V_T - V_s$ during the positive charging cycle. The charging of the LC capacitor is analogous to the charging of an RC circuit, but there are some important differences, due to the non-linear nature of the TFT $I_d - V_D$ relationship (using the MOSFET Eq. 3.10), and the changing channel resistance during the charging cycle. The charging transient can be calculated from:

$$\frac{dV_{LC}}{dt} = \frac{1}{C_{LC}}\frac{dQ_{LC}}{dt} = \frac{I_d}{C_{LC}} \tag{4.3}$$

The charging current, I_d, through the TFT is given by modifying Eq. 3.10 to allow for the changing voltage, $V_s - V_{LC}$, between the source and drain terminals, and for the changing voltage, $V_G - V_T - V_{LC}$, between the source and gate terminals:

$$I_d = \frac{\mu_n W C_i}{L}\left[(V_G - V_T - V_{LC})(V_s - V_{LC}) - 0.5(V_s - V_{LC})^2\right] \tag{4.4}$$

$$\int_{V_1}^{V_{LC}} \frac{dV_{LC}}{(V_G - V_T - V_{LC})(V_s - V_{LC}) - 0.5(V_s - V_{LC})^2} = \frac{\mu_n W C_i}{C_{LC} L}\int_0^t dt \tag{4.5}$$

where V_1 is the value of V_{LC} at $t = 0$, and the solution of this equation is:

$$V_{LC} = \frac{V_s[V_1 + V_s - 2(V_G - V_T)] + [V_s - 2(V_G - V_T)](V_1 - V_s)\exp -t/\tau}{V_1 + V_s - 2(V_G - V_T) - (V_1 - V_s)\exp -t/\tau} \tag{4.6}$$

where,

$$\tau = \frac{C_{LC} L}{\mu_n W C_i (V_G - V_T - V_s)} \tag{4.7}$$

Although Eq. 4.6 has more terms than the simple RC charging expression, it still has a recognisable, effective time constant term, given by Eq. 4.7. This expression is the product of the LC capacitance, C_{LC}, and the TFT on-resistance at the end of the charging cycle, when the value of V_{GS} is $V_G - V_T - V_s$. As mentioned above, for the negative charging cycle, V_s is negative, and V_{GS} is numerically larger than it is for the positive charging cycle; hence, the time constant for the negative cycle is smaller. This is illustrated in Fig. 4.7a, in which the positive and negative switching transients are shown for $V_1 = -3$ V and $V_s = 3$ V, and $V_1 = 3$ V and $V_s = -3$ V, respectively, and the slower tail on the positive cycle is apparent. This is more clearly seen in the logarithmic plot in Fig. 4.7b, in which both transients start at the same rate, because V_{GS} is initially the same at $V_G - V_T - V_s$ for the negative transient (and $V_s = -3$ V), and is $V_G - V_T - V_{LC}$ for

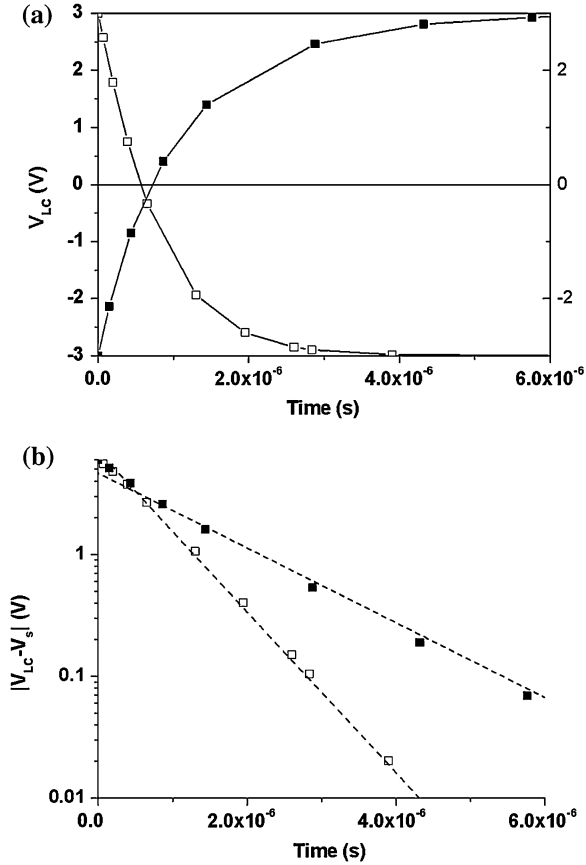

Fig. 4.7 Calculated values of LC voltage, V_{LC}, during pixel charging following data signal, V_s, inversion (*open symbols*: $V_1 = 3$ V, $V_s = -3$ V, and *closed symbols*: $V_1 = -3$ V, $V_s = 3$ V). **a** V_{LC} vs time, and **b** Logarithmic plot of absolute values of $V_{LC}-V_s$ vs time, in which the lines are best linear fits to the data. (The illustrative calculations were for a 15.4" WXGA pixel, and used the following parameter values: $V_G-V_T = 8$ V, $W/L = 5$, $\mu = 0.5$ cm^2/Vs, $t_i = 0.3$ μm, and $C_{LC} = 0.25$ pF)

the positive transient (where, at t = 0, $V_{LC} = V_1 = -3$ V). However, as V_{LC} becomes more positive, $V_G-V_T-V_{LC}$ becomes numerically smaller, and the instantaneous channel resistance increases. The time constants extracted from the slopes of the lines in Fig. 4.7b agree with the values given by Eq. 4.7, noting that, for the positive transient, the line has been fitted to the slow tail.

At the end of the row on-time, that row is deselected (by switching the gate bias to a negative value), and the adjacent row is switched on, and the process described above is repeated. Hence, the display information is loaded row by row during a frame time, and, at the end of this period, the whole process is repeated with the next 'field' of information. However, between the loading of the data signals onto a given row of TFTs, and its updating a frame-time later, it is important that the original signal voltages are maintained across the LC capacitors. During this interval, the sources of the de-selected TFTs will experience a variety of different voltages, which will be different from the voltage, V_{LC}, on the drain terminals, and, depending upon the TFT leakage current, this potential difference acts as a driving force to reset the voltage on the drain. To ensure that this effect is

minimised, the maximum tolerable leakage current, I_{off}, is constrained to be below a certain maximum value, to give, for instance, less than 1 % discharge of the pixel voltage, so that:

$$I_{off} < 10^{-2} C_{LC} V_{max}/T_f \ (\leq 4.5 \times 10^{-13} A \ \text{for} \ C_{LC} = 0.25pF) \tag{4.8}$$

Hence, with line-at-a-time addressing, the TFT is acting as a high quality switch, with a minimum on:off current ratio given by Eqs. 4.2 and 4.8:

$$I_{on}/I_{off} > 500M > 5 \times 10^5 \ \text{for a display with} \sim 1000 \ \text{rows} \tag{4.9}$$

The other potential leakage current path is through the LC itself, but its resistivity is typically $\sim 1 \times 10^{12}$ Ωcm, and, although this is not negligible, the associated leakage will be less than the TFT leakage.

The discussion of the positive and negative biases applied to the LC cell has implied that the polarity of the signal voltages is changed in a uniform fashion across the whole field between frames. This is illustrated in Fig. 4.8a, and is known as *frame inversion*. From a display performance point of view, this has well documented drawbacks, such as increased flicker, as discussed in Sect. 4.2.2.1, and increased vertical cross talk due to different rows in the display experiencing opposite polarity source and drain voltages in the off-state for different lengths of time. In fact, there are several alternative inversion schemes, such as *row inversion* (the polarity of each row of data alternates within one frame), or *column inversion* (the polarity of each column

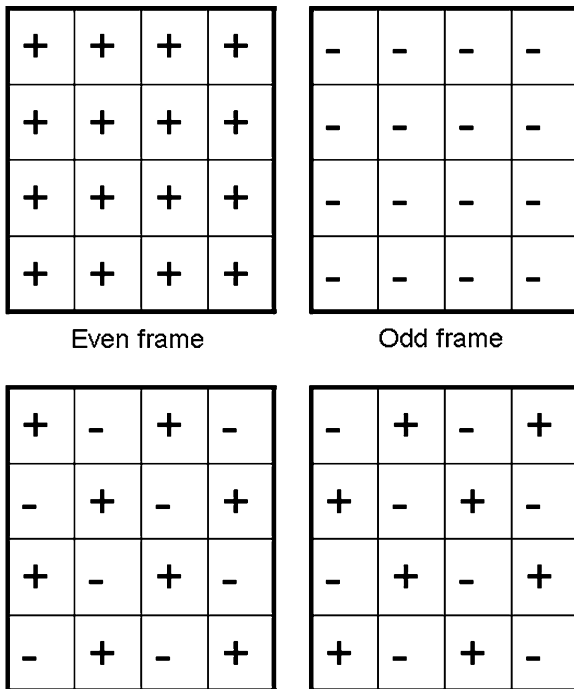

Fig. 4.8 AMLCD data signal drive inversion schemes, showing the signal polarity in consecutive frames with (**a**) frame inversion, and (**b**) dot inversion

of data alternates within one frame), or *dot inversion*, as shown in Fig. 4.8b. This is a mixture of row and column inversion, in which the polarity of every other pixel alternates, and gives the lowest values of cross-talk and flicker. In all these schemes, the polarity pattern within one frame is reversed in the next frame, so that each LC pixel experiences alternating positive and negative biases.

The foregoing description of active matrix addressing of LCDs is somewhat simplified and idealised, and there are important behavioural artefacts associated with parasitic capacitances within the pixel, such as cross talk and pixel off-set voltages. The magnitude of these effects is determined by the detailed pixel layout, and these effects are discussed in the next section. It should also be mentioned that additional capacitance is frequently introduced in parallel with the pixel capacitance, by means of a *storage capacitor*, which is also discussed in Sect. 4.4.

Finally, the viewing angle dependence of brightness and contrast in the simple TN cell is limited, and, although it is acceptable in smaller displays up to notebook size, it was necessary to improve it in the larger monitor and TV displays. In the TN cell, at mid-grey levels, the LC director is changing direction from horizontal towards vertical in the middle of the cell, and, at different viewing angles, this variable direction changes the transmittance of the cell. To improve the viewing angle, modified cell architectures have been developed, of which the two most widely used are the in-plane switching mode (IPS) [13], and the multi-domain vertical alignment mode (VA) [14, 15].

The operation of the IPS cell, with crossed polarisers, is shown in the off and on states in Fig. 4.9a and b [10], respectively. In both cases, the LC director is parallel to the plane of the glass plates (and, in Fig. 4.9a, the director is perpendicular to

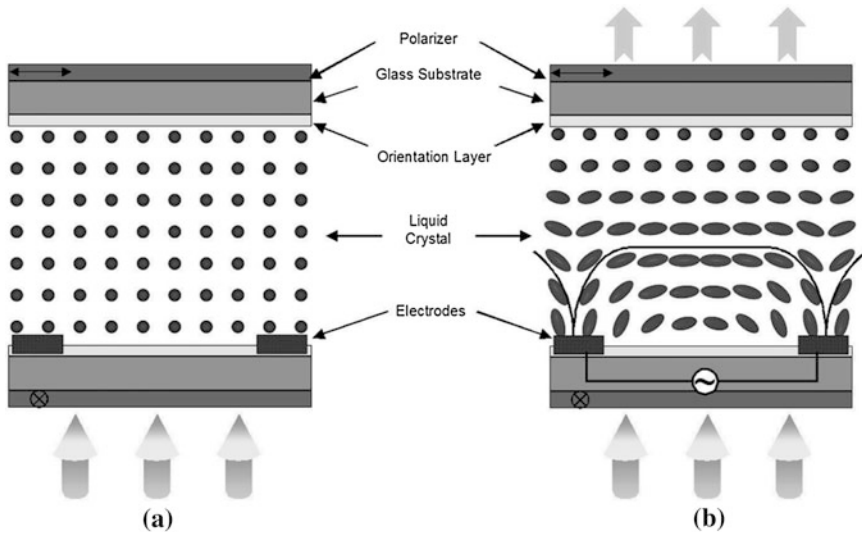

Fig. 4.9 Illustration of the normally black, IPS mode of LC cell switching. **a** Zero bias dark-state. **b** Biased bright-state (Reprinted from [10] with permission of SID)

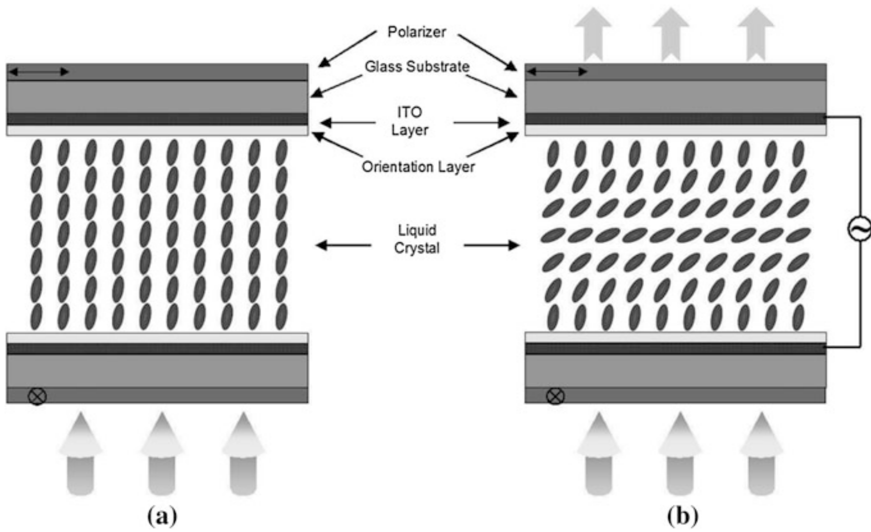

Fig. 4.10 Illustration of the normally black, VA mode of LC cell switching. **a** Zero bias dark-state. **b** Biased bright-state (Reprinted from [10] with permission of SID)

the page). The major difference from the simple TN cell, is that the switching electrodes are on the TFT plate, so that, when a bias is applied between these electrodes (Fig. 4.9b), the molecules rotate about their short axis, and the director aligns with the field. This puts a twist into the column of liquid crystal molecules, and the plane of polarisation of the light is similarly rotated. The improved viewing angle arises from the long axis of the molecules always remaining parallel to the plane of the cell. However, the trade-off with IPS is a reduced aperture ratio due to the inclusion of the switching electrodes within the pixel [13].

The operation of the VA cell, with crossed polarisers, is shown in the off and on-states in Fig. 4.10a and b [10], respectively. The molecules are vertically aligned at zero bias, and, as the LC mixture is engineered to have a negative dielectric anisotropy, when a bias is applied between the top and bottom plates, the molecules rotate in order to align their short axis with the field. With the short axis vertically aligned, the long axis of the molecule is free to rotate within the horizontal plane, and, by sub-dividing and texturing the pixel surface [15], the long axis is constrained to lie in different directions within the sub-divided pixel. Hence, in a pixel containing four sub-pixel domains, the same molecular orientation is seen from different angles, which greatly improves the viewing angle performance of the VA cell compared with the conventional TN cell.

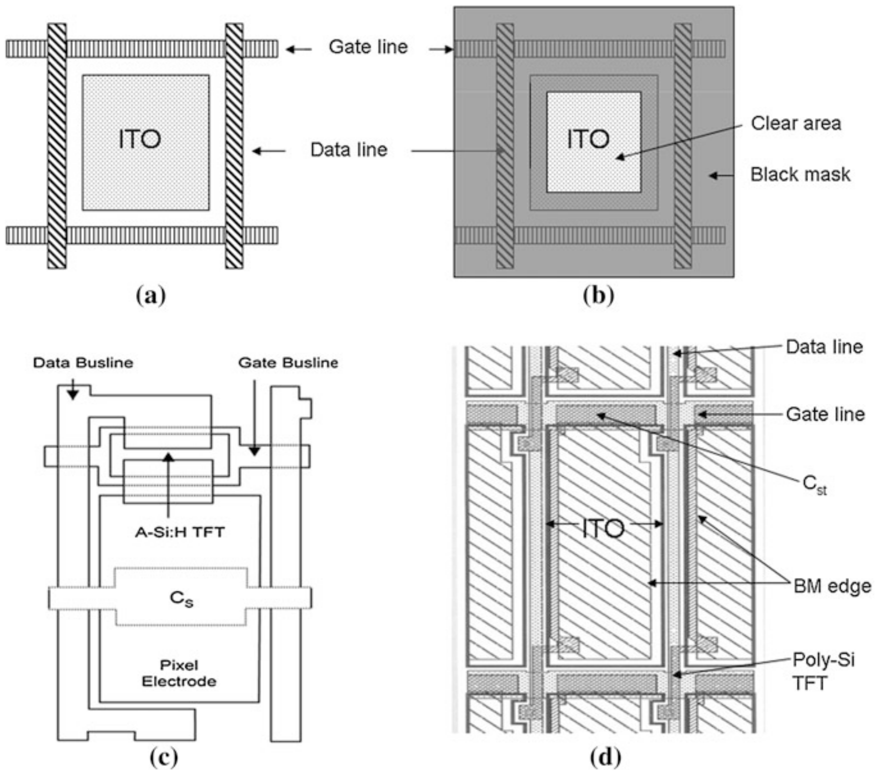

Fig. 4.11 Pixel layout considerations **a** effect of bus bars and ITO clearance margin on aperture ratio, **b** effect of black mask, BM, on aperture ratio, **c** illustrative a-Si pixel with storage capacitor (Reprinted from [20] with permission of SID), and **d** poly-Si pixel with storage capacitor

4.4 Pixel Layout Considerations

4.4.1 General

The pixel layout will consist of the addressing TFT, the ITO pixel pad, the row and column bus bars, various interconnections, including contact windows through insulating layers, and possibly a storage capacitor. These will be designed in compliance with the design rules of the fabrication process, which will specify the minimum feature sizes, and the gaps between different layers. In a conventionally designed pixel, these minimum gaps between different layers will result, for instance, in a gap between the bus bars and the ITO pixel pad, within which the optical transmission will be un-modulated, as shown in the schematic pixel layout in Fig. 4.11a (for clarity, the TFT has been omitted from this diagram). If these regions are left clear, they will permit residual optical transmission when the ITO pixel area is turned off, and the contrast ratio of the display will be seriously

degraded. In order to ensure a high contrast ratio, these clear areas must be overlaid with an occluding layer, which is normally a black masking pattern, fabricated on the upper, colour filter, CF, plate. The design of this feature will be in accordance with the alignment tolerances between the TFT and CF plates, and the black mask area, BM, may be shown superimposed on the pixel layout, so that the aperture ratio can be visualised. The BM pattern is shown in Fig. 4.11b, and the area within its inner edges will be the final transmitting area of the pixel, A_T. This will determine the aperture ratio of the pixel, which is given by the ratio of this area to the total pixel area, A_P. For example, taking a 15.4" WXGA (16:10) display, having $87 \times 259\ \mu m^2$ pixels (where $A_P = 2.24 \times 10^{-4}\ cm^2$), with 5 μm bus bars, 3 μm gaps between the ITO pad and the bus bars, and a 5 μm alignment tolerance between the TFT and CF plates, the value of A_T is $1.57 \times 10^{-4}\ \mu m^2$, giving an aperture ratio of 70 %. Hence, there can be considerable loss of aperture just due to the bus bars and the black mask, even before the TFT and storage capacitor areas are subtracted. The process design rules will be independent of the pixel size, so that the above fractional losses may increase as the pixel size decreases. Hence, for some high resolution [16] or small pixel geometry displays [17, 18], where the conventional BM will seriously reduce the aperture ratio, its inclusion on the TFT plate has been investigated, using either the bus bars themselves [16, 17], or a separate, earthed metal track [18]. Except for the latter architecture, the trade-off for a larger aperture is potentially higher cross-talk in the display, due to the parasitic capacitances between the bus-bars and the overlapping ITO layer. However, these are usually minimised by using thick inter-layer dielectrics (ideally, with a low dielectric constant). (Where a separate earthed track is used [18], this is to minimise the parasitic capacitance between the pixel pad and the signal lines). For the majority of current displays, however, the BM is conventionally fabricated on the CF plate [19].

As mentioned above, the pixel may include a storage capacitor, C_{st}, in parallel with the LC pixel capacitor, which will reduce the effects of parasitic coupling, as well as increasing the tolerance of the structure to TFT leakage currents between refresh signals. In this case, Eq. 4.8 is modified to read:

$$I_{off} < 10^{-2}(C_{LC} + C_{st})V_{max}/T_f\,(\leq 4.5 \times 10^{-13}(1 + C_{st}/C_{LC})A \text{ for } C_{LC} = 0.25pF) \tag{4.10}$$

The off-state leakage current in poly-Si TFTs is generally larger than in a-Si:H TFTs (as discussed in Chaps. 6 and 8, respectively), and, in these displays, $C_{st}/C_{LC} \sim 2$–5, whereas, in a-Si:H displays, it is more common to find that $C_{st}/C_{LC} \sim 1$. The two favoured techniques for building a storage capacitor into a pixel are either to use the previous gate line, or to introduce a separate metal track into the pixel as one plate of the capacitor, with the ITO or TFT drain pad being the other plate. An illustrative a-Si:H TFT pixel layout [20] is shown in Fig. 4.11c, and, in this case, a separate metal track over the ITO pad has been used to form the storage capacitor. Figure 4.11d shows a poly-Si pixel design [21], in which the alternative strategy, of using the previous gate line, has been employed. The other

detailed difference between Fig. 4.11c and d is that, in the latter case, an extension to the doped poly-Si drain has been used as the lower plate of the storage capacitor rather than the ITO pixel pad itself. (Forming the capacitor with the drain extension is electrically equivalent to using the ITO pad, as the two are connected to each other. However, by using the drain extension, a higher capacitance/unit area can be achieved, due to the thinner gate oxide separating the poly-Si layer from the gate electrode, whereas thicker interlayer dielectrics would generally separate the ITO from the gate line).

Whilst Fig. 4.11c and d cannot be quantitatively compared with each other in terms of aperture ratio, it is generally the case that the storage capacitor formed from the adjacent gate line is the more area efficient, as the gate bus bar has to be present in any case. However, as shown in Fig. 4.11d, its width was greater than the column lines in order to give the required storage capacitance, and to provide for the alignment tolerances within the process.

4.4.2 *Performance Artefacts*

This section describes aspects of the layout/processing conditions, which can lead to performance artefacts in the display. These can result from parasitic capacitive coupling between the drain and gate terminals, parasitic coupling between the source and drain terminals, and the effects of the resistance of the gate row lines. The first leads to a voltage resetting of the pixel voltage when the row select voltage is changed to deselect, the second gives cross-talk, and the third can lead to incomplete pixel charging in long rows.

4.4.2.1 Voltage Kick-Back

As shown in Fig. 4.5b and c, the drain terminal overlaps the gate electrode, leading to a parasitic capacitance, C_{GD}, between the two terminals. This is included, together with a storage capacitor, C_{st}, in the pixel equivalent circuit in Fig. 4.12a. As a result of this coupling, the capacitor, C_{GD}, acts as a voltage divider for changes in the gate voltage, ΔV_G, leading to changes in the pixel voltage, ΔV_{LC}, given by:

$$\Delta V_{LC} = \Delta V_G C_{GD}/(C_{GD} + C_{LC} + C_{st}) \quad (4.11)$$

This occurs at the end of the pixel charging period, when the gate voltage is switched from the positive select value, $+V_{G(on)}$, to the negative de-select value, $-V_{G(off)}$, causing the pixel voltage to be reset by a negative amount, ΔV_{LC}, as shown in Fig. 4.12b. This voltage reset is referred to as the *kick-back voltage*, and, as it is always negative, it reduces V_{LC} during the positive phase, and increases it during the negative phase, of the pixel charging sequence. In addition to this parasitic

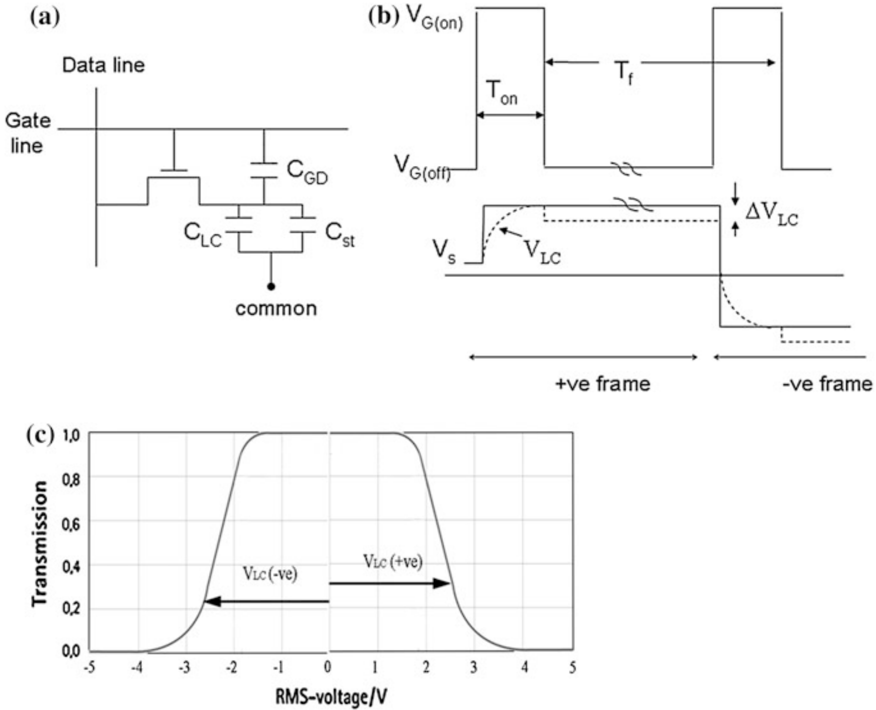

Fig. 4.12 **a** Pixel equivalent circuit, including storage capacitor, **b** row addressing waveform, column data voltage, V_s, LC voltage, V_{LC}, and kick-back voltage, ΔV_{LC}, and **c** effect of ΔV_{LC} on LC transmission-voltage curve, where $| V_{LC}(-ve) | > | V_{LC}(+ve) |$

capacitive coupling, when the TFT is switched off, the channel charge is ejected and ~50 % leaves by each of the two TFT terminals, leading to extra negative charge being added to the LC capacitor, given by:

$$\Delta Q_{LC} = 0.5WLC_i(V_G - V_T - V_s) \tag{4.12}$$

where W and L are the channel width and length of the TFT, respectively, and C_i is the gate insulator capacitance/unit area. This charge leads to a further change in the stored pixel voltage, which varies with the size and polarity of V_s.

These changes in pixel voltage cause the optical transmittance of the pixel to be different in the negative and positive charging phases (even though the signal voltage, V_s, is numerically the same, and differs only in its polarity). The difference in transmission in the positive and negative frames is shown in Fig. 4.12c, and this can lead to the appearance of flicker in the display. The flicker can be reduced by using the minimum design rule values of overlap in the pixel design, and by the presence of the storage capacitor, C_{st}. In principle, the voltage kick-back effect is constant, and could be compensated for by making the common electrode voltage on the CF plate more negative. However, due to the dielectric

anisotropy of the LC, its capacitance is a function of the bias across it, so that the voltage division is not constant, and full compensation cannot be achieved this way. Nevertheless, off-setting the common electrode voltage from zero can reduce the flicker. In addition, the presence of a storage capacitor reduces the dependence of the total capacitance on pixel voltage, and, therefore, reduces the variability in kick-back voltage. A further technique to reduce the perception of flicker is to use dot inversion, rather than frame inversion (see Fig. 4.8), so that adjacent pixels experience alternating positive and negative biases, which visually averages out the perception of frame-to-frame changes in overall brightness.

4.4.2.2 Vertical Cross-Talk

Vertical cross talk occurs when the signal voltage, V_s, being applied to a particular row of TFTs, affects the transmittance of pixels in other rows, and this can result from a parasitic capacitance, C_{DS}, between the pixel pad and the adjacent column lines. The capacitance can arise from 2-D coupling of the adjacent lines and pads, the direct overlap of the ITO pixel electrode, or the overlap of the drain terminal of the TFT with the source line. A particular example of the latter is shown in the pixel layout in Fig. 4.11d. The change in pixel voltage due to C_{DS} is given by:

$$\Delta V_{LC} = V_s C_{DS}/(C_{DS} + C_{LC} + C_{st}) \tag{4.13}$$

As with the kick-back voltage, the magnitude of this effect is reduced by the presence of a storage capacitor, and the value of C_{DS} itself is minimised by using thick dielectric layers, ideally with a low dielectric constant, between the column lines and the pixel pads.

4.4.2.3 Row Resistance Effects

As AMLCDs increase in size, the length of the addressing lines gets longer, and, in the absence of any changes in the structure of the lines, their total line resistance increases. Similarly, as the resolution of displays increases, the number of pixels increases, and the capacitive loading of the addressing lines increases (due to the greater number of pixel TFTs and of row/column crossovers). Hence, the RC charging times of the rows is likely to increase whilst, at the same time, the increased resolution will reduce the row on-time. As a consequence of this, if the RC charging time constant is too long, there is a potential problem of inadequate pixel charging in larger and higher resolution displays. In fact, because the unit cell resistance and capacitive loading of each pixel is repeated along the line, the charging of the line is best described as a distributed RC network, in which the pixel furthest from the point at which the gate switching signal is applied will receive the most delayed signal. This effect is demonstrated in Fig. 4.13a and b, in which the gate voltage and pixel charging waveforms have been simulated for the

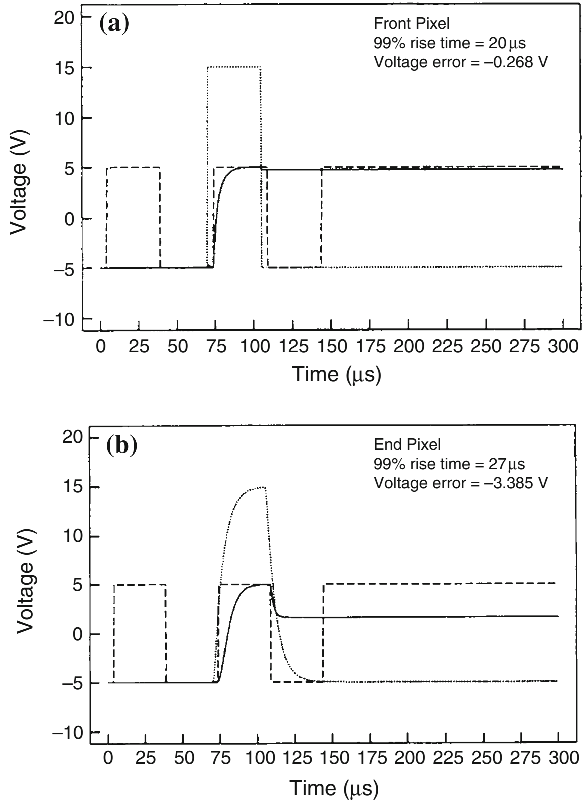

Fig. 4.13 Pixel charging waveforms (**a**) 1st pixel, and (**b**) last pixel in row, where the *dotted line* is the gate voltage, the *dashed line* is the data signal, and the *solid line* is the pixel voltage (Reprinted from [22] with permission of SID)

first and last pixels, respectively, in a row addressed by a line whose resistance is too high [22]. As this diagram shows, the pixel charging occurs accurately for the first pixel, but the distortion in the gate voltage waveform at the last pixel leads to a large error in the pixel voltage, which, in this particular example, was due to the slow turn-off of the gate pulse. Hence, the resistance of the gate lines has to be low enough to meet the requirements of the display, in terms of its size and resolution. The size is usually defined by the display diagonal, D, or its horizontal width, L_H and vertical height, L_V. The resolution can be defined by the number of rows, M, and columns, N, which can also be expressed as the pixel resolution/unit length, r, given by N/L_H.

The total row resistance, R_R, is given by:

$$R_R = \rho L_H / t_G W_R \equiv R_{SG} L_H / W_R \tag{4.14}$$

where ρ is the resistivity of the gate material, t_G is its thickness, W_R is the width of the row line, and R_{SG} is the sheet resistance of the metal.

The total row capacitance, C_R, is given by:

$$C_R = NC_{GTFT} + NC_X + NC_{st(par)} \tag{4.15}$$

where the TFT gate capacitance, $C_{GTFT} = A_{GTFT}\varepsilon_0\varepsilon_i/t_i$ (t_i is the thickness of the gate dielectric), and the other capacitance terms are parasitic ones due to: the row/column cross-overs, $C_X = W_R W_C \varepsilon_0 \varepsilon_d / t_d$ (t_d is the thickness of the cross-over dielectric, and W_C is the width of the column line), and the storage capacitor, $C_{st(par)}$, assuming that the gate is being used as the storage capacitor for the TFT in the adjacent row. In this case, the parasitic capacitance will be the series combination of C_{st} and C_{LC} through the pixel in the adjacent row, i.e. $C_{st(par)} = C_{st}C_{LC}/(C_{st} + C_{LC})$. If the gate-line storage capacitor is absent, this term can be ignored. Other potential parasitic capacitances would need to be assessed from the detailed pixel layout, and could include the capacitance of the gate line to the common electrode on the CF plate.

To ensure full charging of the furthest pixel in the row, the RC time-constant of the row line will need to be less than a small fraction, α, of the row on-time, T_{on} ($= T_f/M$) [22], i.e.:

$$R_R C_R < \alpha T_f / M \tag{4.16}$$

$$\rho < \alpha T_f t_G W_R / L_H M N \{ C_{GTFT} + C_X + C_{st(par)} \} \tag{4.17}$$

Hence, the required resistivity of the row metal will scale inversely with the size and resolution of the display, but can be traded-off against the thickness and width of the line. However, this trade-off will be limited by the process design rules, which may specify a maximum film thickness (to ensure good step coverage by subsequent layers) or a maximum line width to ensure an acceptable aperture ratio. Figure 4.14 [22] is an example of the calculated trade-off in resolution (defined in pixels/mm) and display diagonal, which can be met by metals of different resistivity. (In this calculation, the aperture ratio was kept constant, and the metal film thickness, t_G, was held at 300 nm). In order to put these values into the context of specific displays, the dotted lines show different display formats,

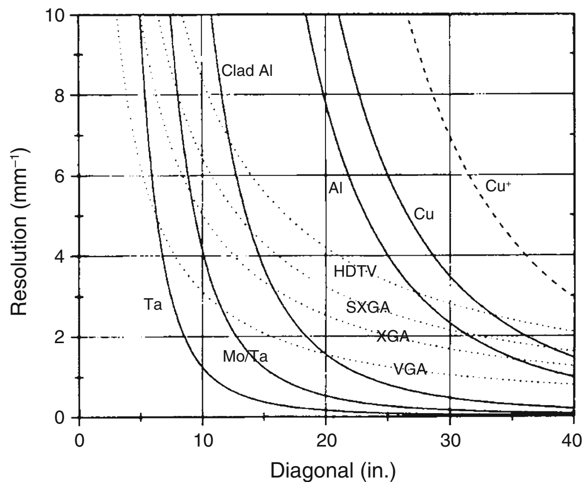

Fig. 4.14 Calculated trade-off between a-Si:H AMLCD resolution and display diagonal, for different display formats (*dotted lines*) and different gate metals (*solid lines*) (Reprinted from [22] with permission of SID)

defined in terms of the pixel count shown in Table 4.1, and only those displays which fall to the left of a particular metal can be satisfactorily driven by it. The number of display formats in this figure is limited, and a subsequent publication extended the range up to QUXGA [16]. As illustrated by Fig. 4.14, lower resistivity metals are needed to drive displays of increasing size and resolution, and the evolution in preferred gate metal can be observed in the change from Cr gate lines ($\rho = 20$ µΩ cm), in the earliest displays, through Mo ($\rho = 13$ µΩ cm), and AlNd ($\rho = 7$ µΩ cm), to Al ($\rho = 4$ µΩ cm) or Cu ($\rho = 2.5$ µΩ cm) [23] in contemporary ones.

The above discussion has focussed on the resistance requirements of the gate lines, and has included the option of using the TFT gates, in adjacent rows, as storage capacitors. Where separate, non-gate lines are used as storage capacitors, the loading of the row lines will be reduced, and the resistance of the storage capacitor lines will need to be separately considered, to ensure that it is low enough to charge the storage capacitors during the row on-time. Finally, there are similar calculations to establish the maximum acceptable resistance for the column lines, but these usually have lower capacitive loading than the row lines, and, therefore, the preferred row metal should be suitable for the column lines as well.

4.5 AMLCD Fabrication

This section provides a brief overview of AMLCD fabrication [19], and describes the major stages of this process, consisting of the TFT and colour filter plate fabrication, the LC cell construction, and the assembly of the final display module.

4.5.1 TFT Plate

Most commercial AMLCD manufacturers use a-Si:H TFTs, and the fabrication of these devices is described in Chap. 5. By and large, the basic a-Si:H TFT fabrication schedule is used for the active TFT plate, but with the addition of a final dielectric layer (by plasma enhanced chemical vapour deposition, PECVD, of a-SiN_x:H for a-Si:H TFTs), as an interlayer dielectric to electrically separate the ITO film from the source and drain metallisation. Contact windows are photolithographically patterned down to the drain contact pads, and then ITO is sputter deposited at ~200 °C, and defined into the individual pixel pads. Figure 4.15a shows a plan-view and cross-sectional diagram of a pixel, including a storage capacitor, on the finished plate.

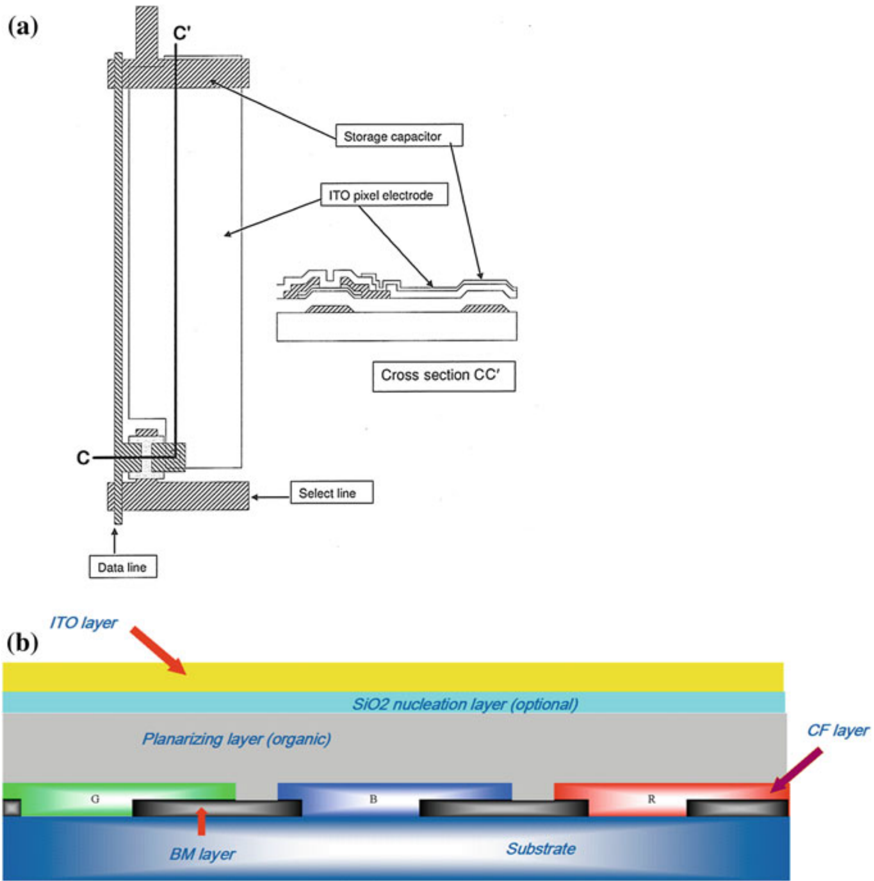

Fig. 4.15 **a** Plan and cross-section of AMLCD pixel, and **b** cross-section of colour filter plate (**a** Reprinted from [52]. Copyright (2005), with permission from Elsevier, and **b** Reprinted with permission from [24])

4.5.2 Colour Filter, CF, Plate

The cross section of a completed CF plate is shown in Fig. 4.15b [24], and the first stage in its fabrication process is the deposition and definition of the black mask material. This is a resin containing black particles so that the final film, which is photo-lithographically defined, has a high optical density and low reflectivity. The next stages deposit and define the three different colour filter layers within the apertures in the black mask pattern. The colour filter films are spin-on photo-resist layers containing pigments to give the required red, blue and green colours, and, as the films are photosensitive, they are directly defined by photo-lithography. Following the formation of the colour filters, the plate is covered by a planarising film,

and then sputter coated with the transparent conductor, ITO, at ~200 °C, to form the common electrode. The ITO film thickness is thicker than on the TFT plate, as it has to have a greater conductivity.

4.5.3 LC Cell

The LC cell is the aligned and sealed combination of the TFT and CF plates, with the LC material sandwiched between them. The first stage in the cell assembly process is the coating of the active side of both plates by a polyimide alignment layer, which is then passed beneath a fine-haired, velvet-coated cylindrical roller in order to micro-groove the surface. This pattern establishes the subsequent alignment direction of the LC molecules [19, 25]. For control of the final cell thickness, photoresist pillars, ~4–6 μm high, are defined on the CF plate, outside the coloured areas, so as to avoid a reduction in the display's aperture ratio.

The LC filling of the cell, and its alignment and sealing, are accomplished in a vacuum chamber by the 'one drop fill', ODF, technique [26]. This is a major improvement in time and LC material usage compared with the earlier technique in which the assembled, but empty, cell was evacuated in a vacuum chamber, lowered into a vessel of LC material, and then the pressure in the chamber was increased so that the pressure difference, plus capillary action, forced the LC material through a gap in the seal line into the evacuated space between the plates. As cell size increased, this became an increasingly inefficient process [26]. With the ODF process, a sealant (or glue) line is dispensed/printed onto one plate, and a precisely monitored quantity of LC material, which will be sufficient to fill the cell, is dropped onto the plate. Both plates are then loaded into a vacuum chamber, where they are aligned, and the chamber pressure increased to disperse the LC, and to make the initial seal, after which UV exposure and thermal curing complete the sealing process. At this point in the process, the mother glass plate, containing several individual displays is still intact, and the final fabrication step is the scribing and breaking of the plate into the separate LC cells.

4.5.4 Display Module

The display module is the completed working unit, which is housed in a rigid, protective case, and consists of the LC cell, the polariser plates, the back light and the external drive circuits. The polariser plates are laminated to the cell, together with any other films for cell protection or viewing performance enhancement.

The external drive circuits control the data and clocking signals sent to the display, and, with a-Si:H displays, will need to make contact to each row and column in the display. This high density of connections is facilitated on the TFT plate by a metallisation fan-out pattern, which is fabricated during the row and

column metallisation stages. The drive circuits themselves are crystalline Si ICs, designed for generating the clock signals to drive the rows, or to supply the column data signals, together with their appropriate timing signals. These chips are connected to the metallisation fan-outs at the side and top of the display, respectively, using either a chip-on-glass, COG, process, or a tape automated bonding, TAB, process (which is also referred to as chip-on-film, COF) [19]. The COG process mounts the chips upside-down, directly on the TFT substrate, whereas, with the TAB process, the chips are mounted on a flexible foil substrate, which is then bonded to the fan-out on the TFT plate. The TAB material contains a photolithographically defined wiring pattern, with bond pad areas to which the ICs are fixed, and a second set of bond pad areas, with which connection is made to the lead-out pattern on the TFT plate. For both COG and TAB processes, the bonding is accomplished with an anisotropic conducting film, ACF, which is, essentially, an anisotropic glue. The anisotropy arises because the glue is a non-conducting matrix containing small metallised spheres, which, when compressed between two vertically aligned bonding pads, makes metallic contact with the pads. The absence of a continuous, horizontal conducting path in the material avoids lateral short circuits between adjacent pads on the plates. The COG approach is more commonly used in smaller displays, as it is a more area-efficient connection scheme.

The final stage of the assembly process is the attachment of the back-light. This is either a cold cathode fluorescent light, or an LED array [27] (although it should be emphasised that these inorganic LEDs are quite different from the organic LEDs used in AMOLEDs, where the OLEDs are used instead of the LCD film). Depending upon the application, the illumination source can be either side-mounted with an appropriate light guide and diffuser to give uniform illumination of the display, or directly mounted at the back of the display with just the diffuser plate. LED back-lights are now increasingly applied to medium and large sized display products, with $\sim$50 % of AMLCD panels currently incorporating them [28].

4.6 Other Display Technologies

4.6.1 Active Matrix Electrophoretic Displays

Electrophoretic displays [2, 3] are now commercially used in a variety of e-reader/e-book products. Their primary advantage over AMLCDs is that they are low power, reflective products, which operate well in bright environments, so that a power-consuming back-light is not required, and, furthermore, the display medium can operate with very low refresh rates, and even in a bi-stable mode. In addition, the reflected image is ‘paper-like’ [2], so that the EPDs are well suited to low power, portable ‘electronic-paper’ products. Given the e-reader application, which does not require fast response times and short addressing periods, they can be addressed by low carrier mobility TFTs. This includes not just the industry

standard a-Si:H TFTs [5], but organic TFTs on flexible substrates [6] as well. Conversely, their slow response, and, until recently, black/white nature has meant that they do not compete in the conventional AMLCD product market.

As the name implies, EPDs rely upon electrophoresis, which is the field-driven movement of charged particles suspended in a fluid medium. In the current EPDs, there are micro-encapsulated black and white charged particles, and the micro-capsules, in a polymeric binder, are deposited as a 100 µm thick layer onto an ITO coated polyester film [3, 29]. The completed electrophoretic foil, attached to a rear electrode, is illustrated in Fig. 4.16a, together with a close-up of a micro-capsule [30]. The principle of image formation is shown in Fig. 4.16b, in which the negatively charged, black particles have been driven to the upper surface with a negative bias on the rear electrode. Conversely, the positively charged, white, titanium oxide particles will be pushed to the surface with a positive bias. As the white particles reflect the ambient light, and the black particles absorb it, a black

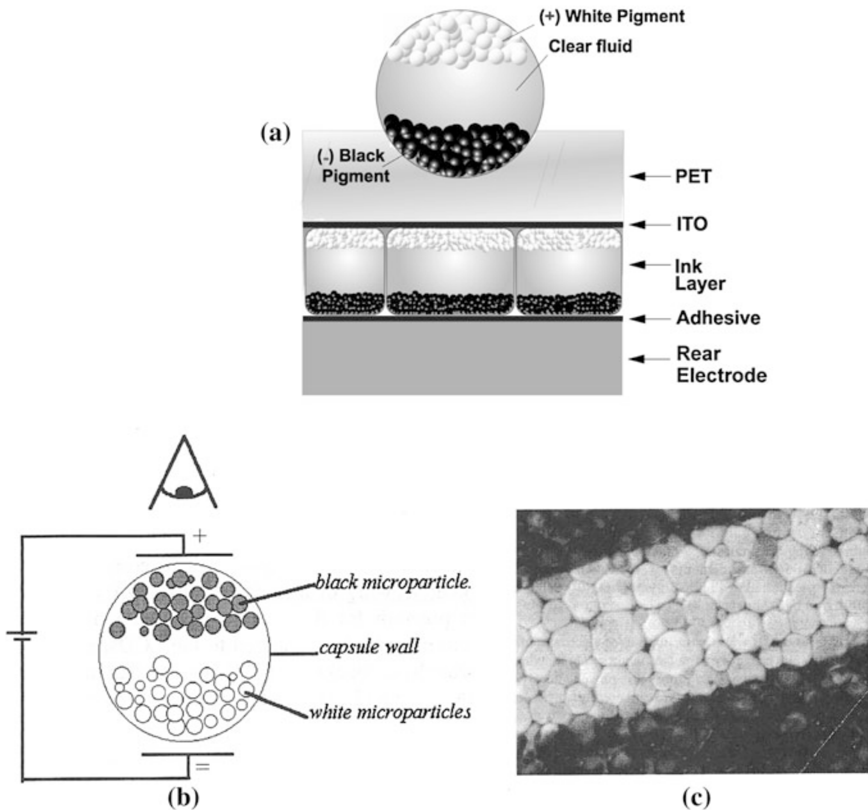

Fig. 4.16 **a** EPD foil attached to a bottom electrode (Reprinted from [30] with permission of SID), **b** schematic illustration of micro-encapsulated EP behaviour, and **c** image of an 'e-ink' line (Reprinted from [3] with permission of SID)

and white image is readily formed, and a magnified image of a well-defined 200 dpi white line, formed from 70 μm micro-capsules, is shown in Fig. 4.16c.

To form a high density image, the EPD foil is laminated onto an active matrix TFT plate, and Fig. 4.17a shows an a-Si:H TFT pixel layout [31], and Fig. 4.17b illustrates its cross-section [5]. The pixel has many common features with AM-LCD pixels, including the ITO pixel pad and a storage capacitor. However, one particular feature of the EPD pixel is the *field-shielded pixel* design, in which the ITO pixel pad extends over the row and column bus bars, and over the TFT, and is separated from them by a thick, low dielectric constant insulator layer to reduce parasitic capacitances. This design has two primary objectives: firstly, to give a large effective optical aperture, by applying the pixel voltage to the largest possible area of EPD film, and, secondly, to screen the EPD film from the voltages appearing on the bus bars and the TFT, which could cause local areas of unwanted contrast switching [31].

The AMEPD is addressed line-at-a-time, with typical pixel voltages of ±15 V for the saturated black and white states, and row select voltages of +22 V and −20 V [32, 33]. In view of the larger pixel voltages compared with AMLCDs, two TFTs are used in series (in the pixel shown in Fig. 4.17) in order to reduce the leakage current, and the storage capacitor also contributes to minimising the discharge of the pixel capacitance through the EPD film [31]. Grey scale can be achieved either by reducing the pixel voltage, or by pulse width modulation [30], and coloured displays are being realised with coloured filters [34], arranged in a quartet of sub-pixels of red, green, blue, and B/W [35].

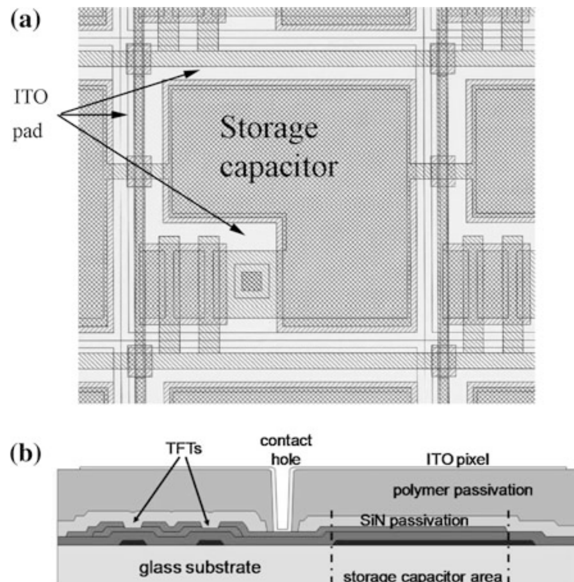

Fig. 4.17 AMEPD pixel structure, showing TFT, storage capacitor and ITO pixel; **a** pixel layout (reprinted from [31] with permission of SID), and **b** cross section (reprinted from [5] with permission of SID)

4.6.2 Active Matrix Organic Light Emitting Diode Displays

OLEDs are electroluminescent devices, in which the emission of light is due to the passage of an electric current through the material, promoting radiative electron–hole pair recombination. Hence, AMOLEDs are emissive displays, and, unlike AMLCDs, do not need a backlight, nor coloured filters, as they can be fabricated to yield the required RGB spectrum. This offers the prospect of lower power, thinner, lighter and cheaper displays, and, as they are emissive (and not dependent upon the passage of light through a layer of molecularly twisted liquid crystal) they also have a much wider viewing angle. In addition, the response time is faster than LCDs, and OLEDs are perceived to be more compatible with flexible substrates, as there is not the requirement to maintain a well controlled cell gap. However, being current driven devices, the detailed addressing process differs from both AMLCDs and AMEPDs (in which the TFTs are essentially voltage switching devices), as the TFTs in AMOLEDs are operating in an analogue current mode. Therefore, the uniformity of the TFTs is of greater importance, and this is reflected in a more complex pixel layout, and also places a premium on the uniformity of the chosen TFT technology. In addition, OLEDs, and their cathode materials, are very sensitive to contamination by oxygen and water vapour, and the whole structure needs to be hermetically encapsulated to ensure an acceptable operational lifetime.

In Sect. 4.6.2.1, the basic operation of OLEDs is described, and AMOLED pixel issues are discussed in Sect. 4.6.2.2.

4.6.2.1 OLED Operation

Two classes of organic LED have been investigated for AMOLED applications, and these are small molecule organic LEDs (SMOLEDs) and polymer LEDs (PLEDs). The SMOLEDs are generally prepared by vacuum thermal evaporation, VTE, whilst the PLEDs can be solution processed and printed [36]. However, solution processed SMOLEDs have more recently been reported, albeit with reduced performance compared with the VTE devices [36, 37]. Much of the current AMOLED activity is focussed on SMOLEDs, and the following discussion is limited to these materials. In view of this, the shortened term OLEDs will be used to refer just to SMOLEDs in the rest of this section.

The initial interest in OLEDs was stimulated by the observation of electroluminescence in a thin double layer structure of 75 nm of diamine covered by 60 nm of 8-hydroxyquinoline aluminium, Alq_3 [38]. A low work function cathode of Mg/Ag was deposited on the Alq_3, which served as the electron injector, and the hole injecting anode was an ITO layer on glass. The injected electrons and holes formed bound-pairs, or excitons, on the Alq_3 side of the organic materials' interface, where they recombined in a fluorescent, radiative decay process, emitting light at 550 nm. The luminescent efficiency was 1.5 lm/W, and, following this initial work, subsequent

developments in materials and OLED design have increased this efficiency to a peak value of ~70 lm/W at 550 nm [39].

One factor contributing to increased emission efficiency has been an engineered change in the mechanism of the radiative recombination process itself, so that the internal quantum efficiency, IQE, was improved [40–42]. The exciton population is distributed between singlet and triplet states, but, due to spin conservation rules, only the singlet state, with a spin of zero, participates in the fluorescent decay process. As the singlet states comprise only ~25 % of the exciton population, it was believed to restrict the IQE to ~25 % [40], although later observations of higher than expected IQE have shown that triplet–triplet annihilation can also give emission in fluorescent materials [43]. However, by adding guest molecules of a phosphorescent dye to the host emission material, the 75 % triplet population can directly participate, via an intersystem crossing process, in a phosphorescent radiative decay process, and offers the opportunity for 100 % IQE [42]. This modified class of OLEDs is referred to as phosphorescent OLEDs, or PHOLEDs. The photon energy from phosphorescent decay will necessarily be less than the fluorescent energy of the host, and, therefore, the host and dye materials need to be matched to obtain the required emission spectra from RGB PHOLEDs.

In addition to the improvement in IQE, the OLED construction has been modified, from the original bi-layer structure of diamine and Alq_3, to a multi-layer device. These structures have been engineered to improve the injection and transport of carriers to the recombination layer, within which they are confined for radiative recombination. This has been achieved by appropriately matching the highest occupied molecular orbitals, HOMOs, of the organic material carrying holes, to the work function of the anode, and similarly matching the lowest unoccupied molecular orbitals, LUMOs, of the electron carrying materials, to the work function of the cathode. Equally, the barriers either side of the recombination layer have been designed to confine the electrons and holes within this region, and to prevent their direct flow to the anode and cathode, respectively. Also, to exploit the higher potential IQE with PHOLEDs, it is also necessary to confine the longer lived excitons to the phophorescent dyed layer [44]. Hence, the diodes typically consisting of some, or all, of the following sequentially grown layers: hole injection, HIL, and hole transport, HTL, layers, an electron blocking layer, EBL, the emissive layer, EL, a hole blocking layer, HBL, and electron transport, ETL, and injection, EIL, layers. In addition to these organic layers, the diodes are capped by the anode and cathode materials. An example structure [44] is shown in Fig. 4.18, in which the schematic energy level diagram is illustrated in Fig. 4.18a, and the chemical structure of the layers is shown in Fig. 4.18b. In this particular example, hole and electron injecting layers were absent, because the small HOMO barrier for hole injection from the anode, and the small LUMO barrier for electron injection from the cathode, obviated the need for specifically low-barrier carrier injection layers. Where injection layers are used, they are to bridge larger gaps between the metal work function and the band edge of the carrier transport layer. Equally, for carrier blocking layers, if the HOMO of the electron transport layer is significantly below the HOMO of the recombination layer, this will block hole transport and avoid the need for a separate hole blocking layer (and

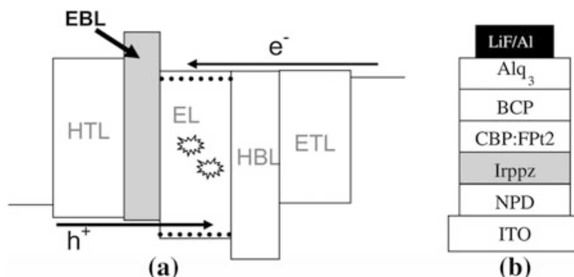

Fig. 4.18 Illustration of a PHOLED stack containing hole and electron blocking layers (**a**) HOMO and LUMO equivalent band structure, and (**b**) material stack. (a-NPD = 4,4'-bis[N-(1-napthyl)-N-phenyl-amino] biphenyl; Irppz = fac-tris(1-phenylpyrazolato,N,C2')iridium(III); CBP = 4,4'-N,N'-dicarbazolebiphenyl; FPt2 = platinum(II)(2-(4,6-difluorophenyl)pyridinato-N,$C^{2'}$)β-diketonate complex; BCP = bathocuproine) (Reprinted from [44] Copyright (2003), with permission from Elsevier)

similar arguments hold for EBLs) [44]. However, this condition was not met with the layers in Fig. 4.18, and the HBL and EBL were introduced. This discussion has focussed on carrier blocking, and similar arguments apply to exciton triplet blocking, so that they too are confined within the doped electroluminescent layer [44], as schematically shown by the star-burst icons in Fig. 4.18a.

Finally, being current driven devices, the improvement in emission efficiency has reduced the drive current needed to achieve acceptable levels of brightness in AMOLEDs, and facilitated the use of low carrier mobility semiconductors, such as a-Si:H [45] and organic TFTs, to address these displays. In addition, the lower drive currents have also increased the operating lifetimes of the OLEDs themselves [46]. The primary lifetime issue with OLEDs of all types [47], and with blue emitting structures in particular [37], is a reduction in the luminescent intensity during device operation. OLEDs are subject to a number of extrinsic and intrinsic aging processes, where the former include moisture absorption, and contamination within the materials themselves [48], and the intrinsic processes cover internal defect centre formation leading to non-radiative recombination pathways [47]. Detailed discussion of OLED instability is beyond the scope of this book, apart from noting that effective device encapsulation is routinely employed to suppress moisture and oxygen contamination, and improved materials synthesis is an on-going activity [48]. In addition, a comprehensive understanding of the nature and role of internal defect formation continues to be the subject of research. Notwithstanding the incomplete understanding of the internal degradation processes, there is considerable empirical activity to identify and use specific OLED layer compositions, which give enhanced operating lifetimes [49–51].

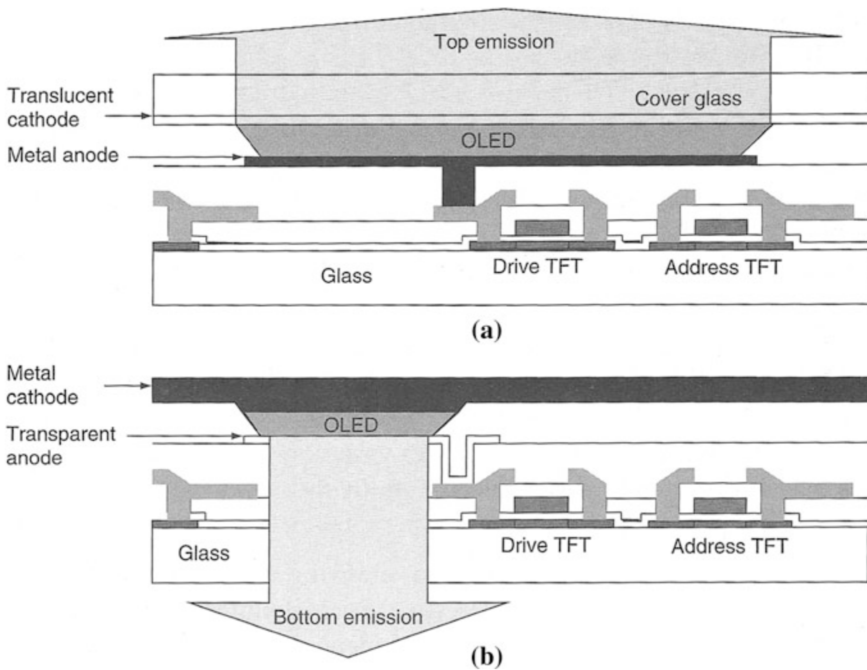

Fig. 4.19 Schematic cross-section of an AMOLED pixel showing **a** top-emitting, and **b** bottom-emitting architectures (Reprinted from [52]. Copyright (2005), with permission from Elsevier)

4.6.2.2 AMOLED Pixels

The two topics to be addressed in this section are the in-pixel addressing circuits, and top-side or bottom-side OLED emission. The test structures referred to in the previous section all had ITO anodes on glass, and were, by implication, bottom-side emitting structures. Whilst this does not present a problem in basic materials work, a bottom-side emitter will have a smaller pixel aperture ratio than a top side emitter, due to the occluding effects of the bus bars and the addressing TFTs, as shown schematically in Fig. 4.19 [52]. Hence, to build a top-side emitter, either a (semi-)transparent cathode and reflecting anode is needed [53], as shown, or the structure needs to be built with the normally transparent anode on top [54]. Also, to realise the potential benefits of the larger aperture ratio, it is necessary to optimise the optical coupling within the structure containing the semi-transparent cathode, so that there is maximum light emission, with minimum colour distortion, through the top surface [53]. This structure is referred to as a micro-cavity, and its internal reflectance characteristics need to be carefully controlled [56]. Examples of engineered semi-transparent cathodes are a thin Mg:Ag layer capped by an 80 nm ITO layer of optimum thickness [55], and, in another case, a 0.5 nm LiF/ 1 nm Al/20 nm Ag layer capped by a 40 nm dielectric film of TeO_2 [56]. These materials were optically matched to the rest of the OLED stack, and, whilst there

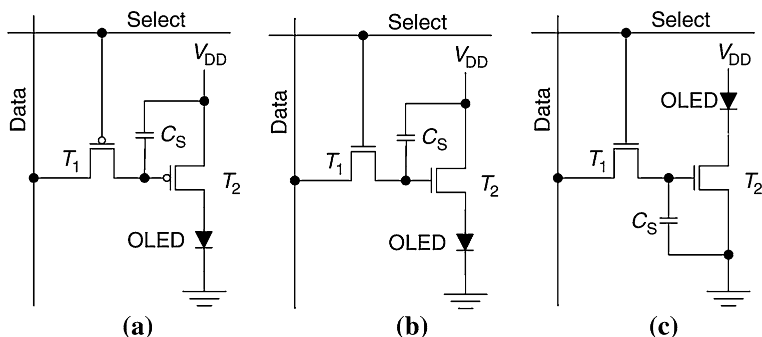

Fig. 4.20 AMOLED drive circuits **a** p-channel 2T1C (anode on drain), **b** n-channel 2T1C (anode on source), and **c** n-channel 2T1C (cathode on drain). (Reproduced from [57] with permission of John Wiley & Sons, Inc)

are numerous publications on top emitter AMOLEDs, details on the choice of cathode materials and optimisation of the structure generally remain proprietary.

The simplest pixel driving circuit consists of two TFTs and a capacitor, as shown in Fig. 4.20a [57], and is frequently referred to as a 2T1C pixel. This shows two p-channel TFTs, where T_1 is the addressing transistor, and T_2 is the drive TFT, which is connected to the anode of the OLED. As the anode is biased more positively than the cathode in the emitting state, this means that the OLED is connected to the drain of T_2. The source of T_2 is connected to the OLED power line, V_{DD}, and the OLED cathode is connected to a common terminal, which may be earthed. Hence, when T_1 is switched on, during the row-select period, the signal voltage, V_s, on the data line is passed through T_I to charge the gate of T_2, and the storage capacitor, C_s (connected between the gate and source of T_2) up to V_s. As with other line-at-a-time addressing schemes, at the end of the row-select time, T_1 is switched off, and the combination of T_2's gate capacitance and C_s retains V_s on the gate of T_2 for the frame period. When comparing this pixel addressing scheme with AMLCD pixels, it will be noted that, in addition to the extra TFT, there is also an extra bus-bar to carry the OLED power line. These extra features, in this most basic pixel design, will reduce the pixel aperture ratio, and contributes to the interest in top-side emitting OLEDs, where the aperture ratio is largely independent of the pixel layout.

The p-channel circuit, illustrated in Fig. 4.20a, can be directly implemented with p-channel TFTs fabricated with poly-Si or organic TFTs. However, with n-channel drive TFTs (a-Si:H or amorphous oxide semiconductor, AOS, TFTs) connected to the OLED anode, as shown in Fig. 4.20b, the OLED is now on the source side of T_2, so that the voltage drop across the OLED, V_{OL}, will change the gate-source bias, V_{GS}, and, hence, change the drive current delivered by this TFT (for a given value of V_s). An alternative configuration with n-channel TFTs is the inverted OLED structure, in which the cathode is connected to the drain of T_2, as shown in Fig. 4.20c.

The data signal, V_s, on the gate of T_2 determines its on-current, and, hence, controls the current flowing through the OLED, which then determines the voltage drop, V_{OL}, across the OLED. Transistor T_2 would normally be operated in saturation, so that, using the MOSFET Eq. (3.17), the channel current $I_{d(sat)}$ is given by:

$$I_{d(\text{sat})} = \frac{\mu W C_i (V_{GS} - V_T)^2}{2L} \tag{4.17}$$

For p-channel TFTs, V_{GS} is the gate-source bias, which, in this case is equal to $V_s - V_{DD}$, but, for n-channel TFTs (using the circuit shown in Fig. 4.20b), V_{GS} is equal to $V_s - V_{OL}$, and, if V_{OL} varies across the display or changes due to aging, this will cause non-uniformities in the display [58, 59]. In spite of this, the simplicity of this circuit is its main attraction, and it continues to be used for a range of demonstrator AMOLEDs, including those addressed by AOS TFTs [8], and OTFTs [60].

However, inspection of the terms in Eq. 4.17 illustrates some of the limitations in this driving circuit, where the required ±1 % accuracy in setting OLED brightness may not be met:

- The current is very dependent upon V_T, and, to a lesser extent, the carrier mobility, μ, and local non-uniformities in these values will appear as brightness variations in the display.
- Changes in these values during display operation (due to TFT lifetime effects) will similarly affect display performance. This is particularly true of the threshold voltage in a-Si:H TFTs, where, in contrast to the low duty cycle in AMLCDs, the drive transistor will be on for most of the time. This will usually increase V_T, and, to compensate for this, the signal voltage will need to increase. (Gate bias instabilities in a-Si:H TFTs are discussed in Chap. 6, and a comparison of the gate bias stability of the major TFT technologies for the AMOLED application is shown in Fig. 9.25 (in Sect. 9.4.3.3).
- Equation 4.17 assumes infinite output impedance, such that the drain saturation current is not dependent upon the particular value of drain bias across the TFT. In reality, this will not be achieved, although some technologies, such as a-Si:H, have better output characteristics than others, such as poly-Si.
- The sheet resistance of the OLED power lines must be low enough that the voltage drop along these lines is not large enough to significantly reduce the value of V_{DD} at any particular pixel.
- Lifetime issues in the OLEDs themselves will ultimately reduce their brightness at a given current level, leading to the requirement for increased drive currents. Given the sensitivity of the eye to small local variations in brightness, the often quoted OLED lifetime to 50 % reduction in brightness overestimates the life of the display.

In order to address these issues, many different designs of pixel drive circuit have been explored [58, 59, 61], with TFT numbers as high as ten/pixel [61]. These include two classes of pixel circuit design, which can be classified as

'compensated', and 'current mode' pixels [61]. In the 'compensated' pixels, the pixel circuit detects and corrects for V_T and/or V_{OL} changes [55, 59], whilst, with the 'current mode' pixels, current mirror circuits are used to directly set the desired OLED current, during the select interval, and this setting is stored as a voltage on the gate of the driver TFT [61].

An alternative approach to dealing with these non-uniformity effects, particularly in a-Si:H and poly-Si AMOLEDs, has been to use an a-Si:H photo-TFT in the pixel. This senses the optical output from the OLED, and sets the gate voltage on the drive TFT to ensure the correct LED luminescence [62]. This 5T2C circuit automatically compensates for both TFT and OLED instabilities.

Further reference to the AMOLED application can be found in Sects. 7.6 and 9.4.3.3, dealing with poly-Si and AOS TFTs, respectively. However, more detailed discussion of the various AMOLED pixel circuits is beyond the scope of this book, but further information on this topic can be gained from the cited references, and the topic is a regular feature in the annual SID Conference Digests.

4.7 Summary

Active matrix liquid crystal displays, AMLCDs, are today's most ubiquitous flat panel display product, and cover the complete range of display sizes and applications from small portable products, like cell phones, to the largest LCTV displays. As the name suggests, these are based upon the use of LC materials, and the basic twisted nematic LC material concepts are covered in sufficient detail to enable the reader to understand the operating principle of LCDs. In order to be used in high quality displays, the LC pixels are addressed by a matrix of thin film transistors, and the principles of active matrix addressing have been presented, together with the key considerations of pixel design. During the development of today's high quality displays, many performance artefacts of AMLCDs have been identified and rectified, and a number of these have been reviewed, including viewing angle limitations, effects underlying flicker and cross-talk, and the importance of bus bar resistances.

Whilst AMLCDs are the dominant display technology, other display products, based upon different principles, have emerged in recent years. The two most prominent are electrophoretic displays, EPDs, for e-reader products, and organic light emitting diodes, OLEDs, for some portable products. As with AMLCDs, these are also driven by an active matrix of thin film transistors, but their basic image generation processes are different, and their operating principles have been described.

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Part II
TFTs

Chapter 5
Hydrogenated Amorphous Silicon TFT Technology and Architecture

Abstract Hydrogenated amorphous silicon TFTs are the work-horse of the active matrix flat panel display industry, and the architecture and fabrication processes of these devices are described in this chapter. The properties of a-Si:H, including its meta-stability, are briefly summarised as background to later sections, which include a description of the inverted staggered device architecture, and a consideration of TFT layout issues. The semiconductor and dielectric layers in the TFT are deposited by plasma enhanced chemical vapour deposition, PECVD, and the current implementation and understanding of these processes are presented. Finally, some novel a-Si:H TFT structures are described, including self-aligned and short channel TFTs, as well as high stability devices deposited under conditions of enhanced hydrogen dilution of the PECVD reactant gases.

5.1 Introduction

Hydrogenated amorphous silicon TFTs dominate the current flat panel display industry, particularly for active matrix LCDs and for active matrix electrophoretic displays. The technology of these devices is presented in this chapter, and their performance and device physics issues are presented in Chap. 6.

In order to provide some technical background to the later sections, Sect. 5.2 contains a brief overview of the material properties of hydrogenated amorphous silicon, a-Si:H, and these are discussed in greater detail in Chap. 6. The device architecture is described in Sect. 5.3, and this is followed by a discussion of TFT layout issues in Sect. 5.4. These issues apply not only to a-Si:H TFTs, but to the other TFT technologies as well.

Device quality a-Si:H is an alloy of Si with $\sim 10\ \%$ hydrogen. The hydrogen plays a key role in defect passivation within the material, by reducing the dangling bond density from $\sim 10^{20}\ \mathrm{cm}^{-3}$, in H-free a-Si, to $\sim 10^{16}\ \mathrm{cm}^{-3}$ in current device material [1]. The performance characteristics of a-Si:H TFTs are determined by the deposition conditions of the material itself, and the preferred process for this is large area, low temperature plasma enhanced chemical vapour deposition,

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PECVD. The process of RF glow discharge deposition was identified, in the pioneering work on a-Si [2, 3], as delivering material with a low trap state density, whose surface potential could be controlled in an insulated gate, field effect structure, and which could also be doped (although later work showed that the doping efficiency was very low [4]). In this early work, uniform a-Si:H deposition was achieved over areas of ~ 10 cm $\times$ 10 cm [5], and subsequent industrial development has led to the present-day commercial PECVD reactors, which can handle substrates in excess of 2 m $\times$ 2 m [6]. The present understanding of the PECVD deposition process is described in Sect. 5.5, and covers the deposition of both undoped and doped a-Si:H, as well as the gate dielectric a-SiN_x:H.

The TFT structures and deposition processes described in Sects. 5.3 and 5.5 deal with the standard a-Si:H TFT of the FPD industry, and Sect. 5.6 reviews some alternative structures and processes which have been investigated to address some of the limitations of the current device. However, it should be noted that none of these alternative processes has yet been industrialised.

5.2 a-Si:H Material

In order to introduce some of the concepts used in Sect. 5.5, a brief overview of the properties of a-Si:H follows. A comprehensive treatment of the properties of a-Si:H is contained in Ref. [7].

As an amorphous material, a-Si has short range order, given by the preferred four-fold coordination of silicon, but no long range order, due to the variety of bond angles and bond lengths, which can be accommodated in the material. Compared with crystalline silicon, which has a bond length and tetrahedral bonding angle of 2.35Å and 109.5°, respectively [7, 8], the rms deviation from these values in a-Si:H are ~ 2 % and ~ 9–10 %, respectively [1, 8]. This disorder leads to a corresponding distribution of bond energies, and the occurrence of weak bonds (WBs) within the material, which play an important role in its defect structure. In general, the silicon atoms will be four-fold coordinated, with coordination defects occurring where the local inter-atom strain breaks a weak bond. This is illustrated by the bonding network diagram in Fig. 5.1, showing both dangling bond (DB) defects, and a hydrogen-passivated dangling bond. Hydrogen plays a key role in a-Si:H, which is an alloy of Si with ~ 10 % hydrogen, and, in high quality, hydrogenated amorphous silicon, the DB density is reduced to $\sim 10^{16}$ cm^{-3}, due to the presence of hydrogen forming the passivating Si–H bonds at the DBs.

The dangling bond states are amphoteric, in that the neutral state, containing one unpaired electron, can trap a further electron and become negatively charged, or release the unpaired electron and become positively charged. Hence, these defects have three charge states of positively charged, neutral, or negatively charged with zero, one or two electrons, respectively. For defects with a positive correlation energy, such as the dangling bond in a-Si:H [7] (and many deep level

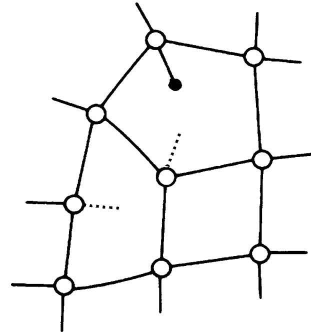


Fig. 5.1 Illustration of the four-fold-coordinated amorphous silicon random network, containing dangling bond defects (*dashed line*), and a hydrogen passivated dangling bond (*solid circle*)

defects in c-Si), the doubly occupied centre is above the singly occupied centre in the band-gap, and the three charge states are shown as a function of the Fermi level position in Fig. 5.2. The defect is negatively charged when the Fermi level is above the upper level, positively charged when it is beneath the lower level, and neutral when it is between the two levels. Moreover, the two electron level does not exist until the DB centre already has at least one electron in it. As with the Si–Si bonds themselves, the uncoordinated Si bonds have a range of carrier binding energies, so that the dangling bonds give rise to a double distribution of deep-lying centres in the forbidden band gap.

In addition, the lack of a long range regular atomic potential (in contrast to that found in single crystal Si) results in localised, as well as extended, electron states. The localised states are characterised by a distribution of band tail states in a-Si:H, extending from both the conduction and valence bands into the forbidden band gap, defining a 'mobility gap' of 1.85 eV [7] (which is significantly larger than the room temperature band gap of 1.12 eV for c-Si). In poor quality material, with high defect densities within the mobility gap, extended state conduction is negligible, and carrier conduction is by localised inter-trap hopping. For device quality material, conduction is by excitation of trapped carriers into extended states, but, as only a small fraction of the total trapped charge is thermally released from the traps, this contributes to the low carrier mobility values measured in a-Si:H. In fact, due to the high density of band tail states, it has not been possible to raise the Fermi level above the mobility edge, and pure extended state

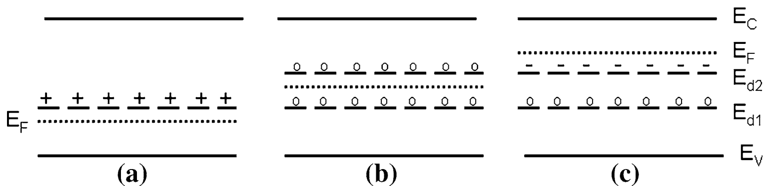


Fig. 5.2 Illustration of the electron occupancy and charge state of an amphoteric dangling bond, as a function of the Fermi level position (**a**) unoccupied centre, and positively charged *lower level*, E_{d1} (**b**) singly occupied centre, and neutral *lower* and *upper levels*, and (**c**) doubly occupied *centre*, and negatively charged *upper level*, E_{d2}

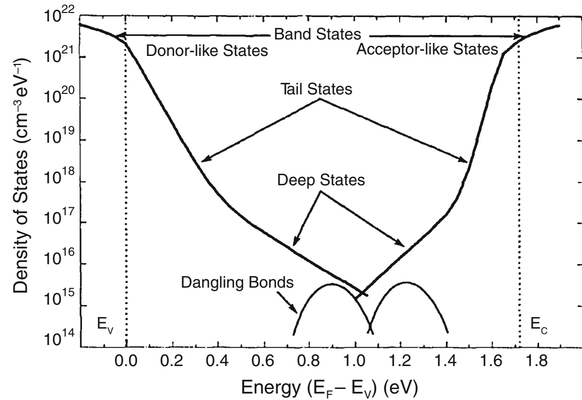


Fig. 5.3 Density of states distribution of a-Si:H (Reprinted from [9] with permission of IEEE)

conduction has not been observed. The density of states distribution in a-Si:H is shown in Fig. 5.3 [9], illustrating both the band tail states and deep states, the density of which is given by the summation of the dangling bond densities. The influence of the mobility gap states on carrier mobility in a-Si:H is discussed further in Sect. 6.2.1.

Hence, the major defects in a-Si:H are dangling bonds and weak bond states, and hydrogen-mediated equilibration occurs between the larger number of weak bonds, and the smaller density of dangling bond and hydrogen passivated states [11]. The details of this interaction are described by the defect pool model [10]. The interaction between hydrogen, the DBs and the WBs after growth determines the DB density under a given set of conditions, although the a-Si:H deposition conditions determine the background WB density [11]. The material is defined as meta-stable as the defect structure is frozen-in, at ~500 K, during cooling from the growth temperature, although the precise freeze-in temperature will depend upon the cooling rate. Moreover, given enough time at lower temperatures, a new equilibrium defect density will develop during a thermally activated relaxation process. This has an activation energy of ~1.0–1.5 eV [7, 12], and the temperature dependent equilibrium defect densities have an activation energy of ~0.2 eV [12]. The defect density within the material also equilibrates in response to other stimuli, such as changes in doping level [4], electron–hole pair recombination induced by optical illumination (the Staebler-Wronski effect) [13–15], and changes in the free carrier density in the TFT channel (induced by the gate bias). This latter dependence underlies the well established bias-stress instability displayed by a-Si:H TFTs [10, 16]. A fuller discussion of these meta-stability effects, and of the density of states in the material, is presented in Chap. 6.

5.3 a-Si:H TFT Architecture

Figure 5.4a shows the most common architecture of a-Si:H TFTs, which is an *inverted staggered* structure, and consists of a bottom metal gate, a non-stoichiometric silicon nitride, a-SiN$_x$:H, gate dielectric layer, and the undoped a-Si:H transistor body on top of this. The contacts to the TFT are n$^+$ doped a-Si:H source and drain regions, which, in turn, are contacted by lower resistance metal pads. The device structure is 'inverted' in that the gate is beneath the channel, and it is 'staggered' in that the source and drain contact regions are not coplanar with the electron channel at the a-Si:H/a-SiN$_x$:H interface, but on the opposite side of the film. Hence, the channel current will need to flow through the thickness of the a-Si:H layer to give current continuity between the source and drain electrodes. Whilst the structure is fundamentally that of an IGFET (metal/insulator/semiconductor structure), it is superficially quite different from the c-Si MOSFET architecture (discussed in Chap. 3), which is top-gated, and coplanar (with the source and drain contact regions on the same level as the channel). However, the architecture, which has been developed for the a-Si:H TFT, is a reflection of the optimised structure which can be fabricated with acceptable performance, within the constraints of a high throughput, low temperature process on large area glass substrates (< 350 °C and > 2 m × 2 m, respectively). Two other major differences from MOSFETs (which are used in p- and n-channel complementary, CMOS, circuits), are that, firstly, only n-channel a-Si:H TFTs are used in commercial applications. This is due to the poorer performance of p-channel devices, which is discussed further in Chap. 6. Secondly, the source and drain regions are not self-aligned to the gate edges, but require a photolithographic alignment stage, giving significant parasitic capacitance between the gate and the source and drain terminals. This latter effect has been discussed in Chap. 4, and contributes to AMLCD performance artefacts.

As mentioned above, a key aspect of the a-Si:H TFT process is its high manufacturing throughput. This is due, in part, to the low mask count, of four or less photolithography stages, needed to fabricate it, and with an extra mask needed for

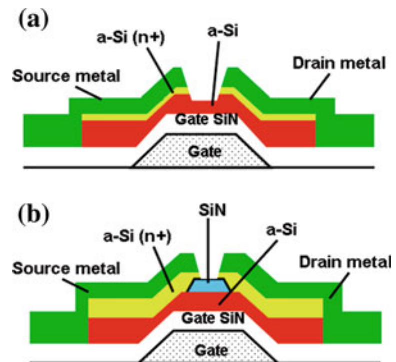


Fig. 5.4 Cross sectional diagrams of inverted staggered a-Si:H TFT structures: (**a**) back-channel-etched, BCE, and (**b**) etch-stop, ES, architectures

an AMLCD. (In contrast, a sophisticated c-Si CMOS circuit can use 12 or more mask stages).

There are two slightly different TFT architectures shown in Fig. 5.4, which differ by the presence of an a-SiN_x:H layer on top of the TFT in Fig. 5.4b. These two architectures have different fabrication schedules, and the industry standard, shown in Fig. 5.4a, is referred to as a *back-channel-etched*, BCE, structure, whilst that in 5.4b is an *etch-stop*, ES, structure. The fabrication of the BCE and ES structures are described below, and, following this, the differences between them are discussed.

5.3.1 Back-Channel-Etched TFT Fabrication

The fabrication of the a-Si:H TFT consists of a sequence of material deposition stages, each followed by patterning of the layers into the desired structures. The process used for film patterning consists of photolithography [17] and etching [18–20] stages, which are described further in Sect. 5.4.1.

Figure 5.5 shows the main process steps in fabricating an inverted staggered BCE a-Si:H TFT. The first stage is the sputter deposition, and photolithographic definition, of the metal gate electrode, by mask stage M1. The gate electrodes are then coated by a stack of three consecutively deposited films of a-SiN_x:H, undoped a-Si:H, and n^+ a-Si:H, in a plasma enhanced chemical vapour deposition reactor [6] (described in Sect. 5.5). The film thicknesses for commercial TFTs are typically 300 nm a-SiN_x:H, 200 nm a-Si:H, and 50 nm n^+ a-Si:H [6]. In the second patterning stage, M2, the triple stack is defined into the individual TFT islands. The next two stages consist of the deposition of the source and drain contact metals, and their definition into tracks and contact pads by mask stage M3. This metallisation pattern is then used as an etch mask to selectively remove the n^+ layer from those areas of the TFT island stack where it is not protected by the metal. The etching of the n^+ region removes what would otherwise be a channel-shorting layer between the source and drain contacts. The TFT fabrication process is completed by the deposition of a final capping/passivation layer of a-SiN_x:H (not shown), which is patterned by mask M4 into contact holes down to the source, drain and gate pads.

A critical stage in this process is the etch removal of the n^+ layer between the source and drain contacts. As the etch selectivity between the n^+ layer and the undoped a-Si:H is minimal [19], a well controlled etching process is required. This is a precisely timed etch to ensure that the n^+ layer is completely removed, whilst the necessary over-etching into the underlying undoped a-Si:H is well controlled and reproducible between plates. In order to accommodate the over-etching into the undoped a-Si:H layer, a relatively thick layer of $\sim$200 nm is used. The n^+ etching stage defines the channel length, L, of the TFT, which is given by the separation between the edges of the source and drain n^+ regions.

1. Deposition and definition of metal gate (**M1**)
2. Sequential deposition of SiN gate dielectric, i a-Si:H, and n^+ a-Si:H
3. Definition of a-Si TFT island (**M2**)
4. Deposition and definition of metal S, D contacts (**M3**)
5. Etch back of exposed n^+ a-Si:H (over-etch necessary to ensure clearance)
6. Deposition of final passivation layer and contact window opening to S, D and G metals (**M4**)

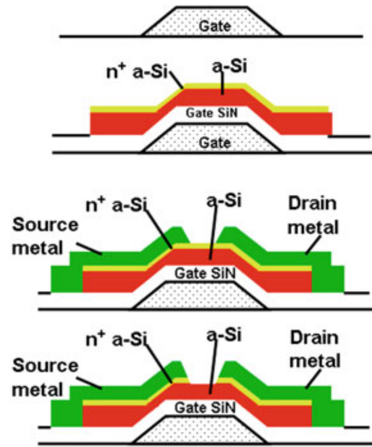


Fig. 5.5 Illustration of the back-channel-etched TFT fabrication steps (stage 6 is not shown)

In summary, the BCE process consists of four mask stages, two PECVD depositions, and two metal sputter deposition stages.

5.3.2 Etch-Stop TFT Fabrication

Comparison of the BCE and ES architectures in Fig. 5.4 shows that the ES structure differs mainly by the presence of an a-SiN_x:H pad beneath the edges of the n^+ regions. This is to give greater etch selectivity [19] between the etching of the n^+ regions and the underlying a-SiN_x:H, and, thereby, avoid the need to use a critical timed etch. However, the cost of this is a more complex fabrication schedule, as shown in Fig. 5.6. Following the first mask stage, M1, to define the gate electrodes, a triple layer deposition of a-SiN_x:H, a-Si:H and a-SiN_x:H is carried out, and the a-SiN_x:H on top of the stack is defined into the etch stop pads by mask M2. This is then followed by the separate deposition of the n^+ layer, and the definition of the device islands by mask stage M3. The source and drain contact metals are deposited, and defined using mask M4, and, as with the BCE process, the unwanted n^+ material is removed using the metal pads as an etch mask. However, in contrast to the timed BCE etch, the a-SiN_x:H pad acts as a more selective etch stop layer. This is, in principle, a more easily controlled process, and permits the use of thinner a-Si:H layers (typically down to 100 nm). The final process is the deposition of a capping layer of a-SiN_x:H (not shown), and mask M5 is used to open contact windows down to the source, drain and gate contact pads.

1. Deposition and definition of metal gate (**M1**)
2. Sequential deposition of SiN gate dielectric, i a-Si:H and SiN etch stop layer
3. Definition of SiN etch stop pad (**M2**)
4. Deposition of n⁺ a-Si:H
5. Definition of TFT island (**M3**)
6. Deposition and definition of metal S, D contacts (**M4**) and removal of n⁺ a-Si:H
7. Deposition of final passivation layer and contact window opening to S, D and G metals (**M5**)

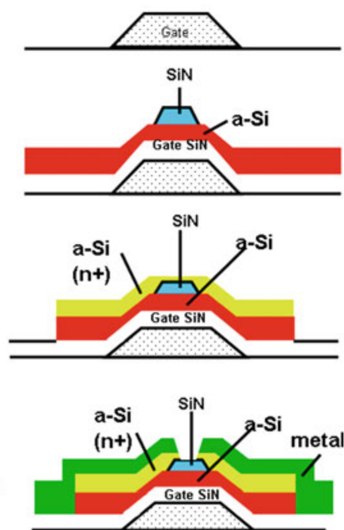


Fig. 5.6 Illustration of the etch-stop TFT fabrication steps (stage 7 is not shown)

In the ES process, the size of the a-SiN_x:H etch-stop island determines the separation of those parts of the n^+ source and drain regions which are in contact with the TFT body, and, hence, defines the TFT channel length, L.

In summary, the ES process involves five mask stages, and three PECVD depositions, but avoids a critical etching stage, whilst also delivering a potentially better back-face passivation layer (in the first triple layer deposition) [21]. However, when comparing the process details with the BCE process in Table 5.1, it is clear that, providing the back channel etch is well controlled, the BCE process is simpler, with fewer steps. Hence, it can deliver higher manufacturing throughput and lower overall plate cost, and is extensively implemented in production facilities. For many research laboratories, the ES process is preferred for basic device studies, as it is more easily implemented and controlled with less sophisticated facilities than in production units.

Table 5.1 Comparison of back-channel-etched (BCE), and etch-stop (ES) a-Si:H TFT processing stages

Process	BCE	ES
Photolithography	4-mask	5-mask
PECVD	2	3
n^+ a-Si:H removal	Timed etch into i a-Si:H	Differential etching with respect to SiN_x:H
Final passivation layer	Possible sensitivity	Screened by 1st SiN_x:H layer

In this book, the two a-Si:H TFT architectures are referred to as BCE and ES, but it should be noted that an alternative naming convention exists in the literature, in which the BCE and ES architectures are referred to as 'bi-layer' and 'tri-layer' structures, respectively [19]. In this nomenclature, reference is made to the number of layers deposited, and no distinction is made between the deposition of the i-a-Si:H and the n^+ a-Si:H layers in the BCE structure, so that the 'bi-layer' device refers to the two types of material deposited: a-SiN_x and a-Si:H. In the ES structure, the sequential deposition of a-SiN_x, a-Si:H, and a-SiN_x is counted as a tri(ple)-layer deposition.

5.4 TFT Layout Considerations

This section will discuss some general TFT layout considerations, which are not restricted to a-Si:H TFTs, but relevant to TFTs in general. However, as the different TFT technologies use different device architectures, the specific diagrams will not necessarily apply to all technologies, but the broad points will.

5.4.1 Photolithography Process

Photolithography is the process whereby the different layers in the TFT are aligned and patterned [17] in order to make the final TFT structure. This is accomplished by optically imaging a pattern from a mask firstly onto a layer of photo-sensitive material, the photo-resist, and then using this as an etching mask to selectively remove the unprotected areas of the film by an etching process. The overall procedure [17] consists of applying a thin layer of photo-resist to the plate, by centrifugal spinning or by slit coating through a linear nozzle, and then exposing it to UV light, which has been passed through the mask pattern. For negative photo-resist, the resist will be hardened where it is exposed to the light, and for positive resist it will be softened in these areas. Once the photo-resist layer has been exposed, it is then developed to remove those areas of the film which have not been hardened. Finally, the plate containing the developed photo-resist pattern is exposed to an etching process, which can use either wet chemicals [18] or a dry plasma etchant [19, 20]. Those areas of the film covered by the photo-resist will be protected from the etchant, and the film will be removed elsewhere. Once the etching process is complete, the photo-resist pattern will be removed from the plate using a suitable solvent. In addition to the processing stages listed above, it is conventional to bake the photo-resist layers at temperatures around 100 °C after the resist application, and after the development stage to further harden it. The pattern defined in the film will be a direct image of the dark areas on the mask when positive photo-resist is used, or a negative image with negative photo-resist.

The performance of a given TFT, such as its on-state and off-state currents, will be determined both by its material properties and by its channel width and length. These latter parameters, together with the process layout and design rules, will determine the overall TFT appearance and size. The design rules will specify the minimum overlaps between different layers, and also the minimum feature sizes within a layer, including the contact window dimensions. The overlap dimensions will be determined by both the photolithographic alignment tolerances, and by the overall critical dimensional control of the lithography process, including the etching stage. Equally, the final feature sizes will be determined both by the resolution of the photolithography process, and also by the etchant characteristics of the pattern definition stage.

The photolithographic aligners, which are used for TFT fabrication within the FPD industry, have alignment and resolution specifications of typically ±0.6 μm and 3.0–3.5 μm, respectively [22]. Based upon these figures, the minimum feature size will be 3.0–3.5 μm, and, when the alignment accuracy and the tolerances in the overall photolithographic process, including the etching stages, are taken into account, the typical gate/drain overlap will be 2.0–3.0 μm.

A detailed description of the photolithography process [17], and of the wet [18], and dry etching [19, 20] stages for commercial TFT fabrication can be found in the cited references.

5.4.2 TFT Layout Issues

Figure 5.7a shows the layout of an inverted staggered TFT, such as a-Si:H, where the source and drain contact pads are used to define the edges of the n^+ regions. Figure 5.7b shows the layout of a different TFT architecture, in this case a top-gated coplanar structure, such as a non-self-aligned poly-Si TFT (see Chap. 7), in which the TFT body is covered with a dielectric layer, and contact windows are needed for the source and drain metals to make contact with the underlying doped regions. Also, as the gate electrode, and the source and drain electrodes are at the same level in this example, there will be a minimum clearance gap specified between these electrodes. As with the layout in Fig. 5.7a, a clear overlap is shown between the gate metal and the doped source and drain regions. Taking, for example, a TFT with a 5 μm long channel, the minimum gate length in both layouts will be 11 μm to ensure 3 μm overlap with the doped regions. Whilst the design rules will specify minimum dimensions, in many cases the actual dimensions will exceed these minimum values, due, for instance, to TFT performance requirements demanding a channel width or length greater than the minimum allowed.

If the minimum layout tolerances are not adhered to, the situation depicted in Fig. 5.7c can arise, in which the gate does not overlap the doped region, but leaves a portion of the TFT channel area, which is not controlled by the gate electrode. This will result in a high channel resistance, giving reduced on-currents, and possibly asymmetric TFT characteristics, depending upon which electrode is used as the source or drain terminal.

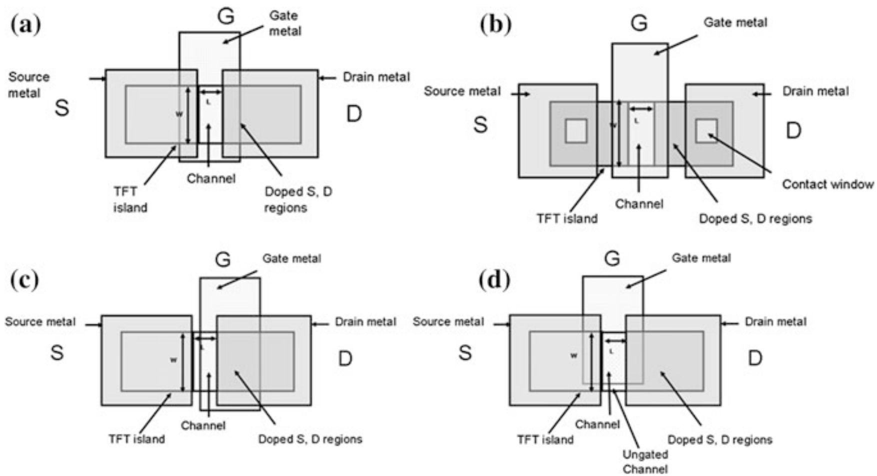


Fig. 5.7 Illustrative TFT layouts showing: (**a**) an inverted staggered TFT, e.g. a-Si:H (**b**) a top gated coplanar TFT, e.g. poly-Si (**c**) source-gate misalignment, and (**d**) channel-gate misalignment

Another common feature to the layouts in Fig. 5.7a and b, is the extension of the gate electrode beyond the width of the TFT island. This is to ensure that the designed channel width, W, determines the device characteristics, and that the gate electrode fully controls the currents flowing through the channel. An example of misalignment in this direction is shown in Fig. 5.7d, in which the gate does not completely overlap the TFT island. In this case, the on-current will be less than expected for a channel width of W, and, in the off-state, the current in the un-modulated part of the channel may be higher than the minimum current measured in a correctly processed TFT. (This will be the case for a TFT in which a non-zero gate voltage is needed to achieve the minimum off-state current). A comparable situation can also arise if the semiconductor layer itself is not patterned, and extends over an area larger than the gate electrode. In this case, not only will the off-state currents be larger than expected, but fringing fields from the gate, source and drain electrodes may also draw a larger than expected on-state current, for the given values of W and L. This will result in an overestimate of the carrier's field effect mobility, if it is calculated using Eqs. 3.12 or 3.18.

5.5 Plasma Enhanced Chemical Vapour Deposition, PECVD

PECVD is used for the deposition of the key non-metallic layers in the TFT: namely, the a-SiN_x:H gate insulator, the undoped a-Si:H for the transistor body, and the phosphorus doped n^+ a-Si:H for the source and drain regions. These layers

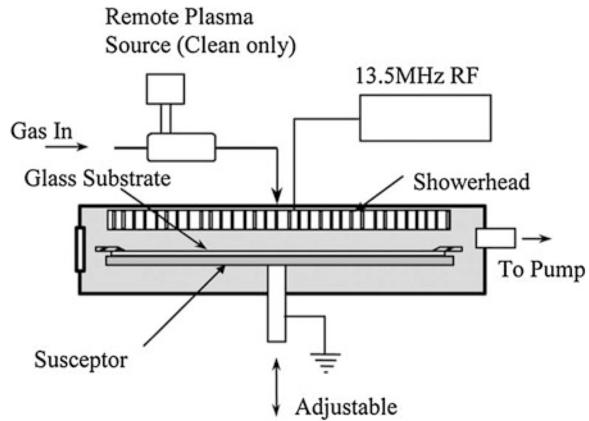


Fig. 5.8 Schematic drawing of AKT PECVD processing chamber (Reprinted from [6] with permission of IEEE)

are deposited as a sequential stack in the BCE structure, without breaking the system vacuum, in order to minimise the growth of unwanted interfacial films between layers, and to suppress ambient contamination. Also, to suppress cross-contamination, these deposition processes are carried out in separate chambers, with robotic plate transfer between chambers, and the equipment is usually configured as a cluster tool in current manufacturing systems [6]. Apart from depositing material of the desired quality, the other requirements of the deposition system are that the depositions can be carried out with a high level of uniformity over large areas (which are currently in excess of 2 m × 2 m), and at low enough temperatures (≤350 °C) to be compatible with the use of glass substrates.

A PECVD deposition chamber is illustrated in Fig. 5.8 [6]. This is a parallel plate reactor, housed in a vacuum chamber, and consists of an earthed, heated substrate holder (the susceptor), a gas shower head, which has been engineered in such a way that the reactant gas distribution leads to uniform material growth over the plate area, and the shower head is powered by a 13.56 MHz RF generator. The basic reactant gas is silane, SiH_4, for the deposition of intrinsic a-Si:H; phosphine is added to this for the deposition of n^+ a-Si:H, and ammonia is added for the a-SiN_x:H deposition. In addition to these basic gases, it is often common to run the deposition process with dilutant carrier gases such as hydrogen [23–26], helium [24, 26], argon [24], or nitrogen [26]. However, due to the key role played by hydrogen both in the a-Si:H material, and in the deposition process itself [11, 27], hydrogen is the most common dilutant for the deposition of the amorphous silicon layer.

The optimisation of the deposition process is a complex multi-parameter task, in which the variables display inter-dependent behaviour, and where the variables are the substrate temperature, the RF power, the parallel plate spacing, the gas pressure and mixture, and the gas residence time [28]. Some of the key features affecting this optimisation are presented in the following subsections.

The final feature shown in Fig. 5.8 is the in-situ plasma cleaning process to remove deposition products from the chamber walls, and to suppress the build-up of particulates in the chamber.

5.5.1 Undoped a-Si:H

The processes involved in the RF PECVD deposition of a-Si:H can be broken down into the gas phase processes within the plasma, which determine the dissociation products of the silane reactant gas, their transport and interaction with the substrate surface, and their eventual incorporation into the growing film [11, 16, 28]. The plasma consists of the fractionally ionised gas and free electrons, and collisions between the energetic electrons and the gas molecules dissociate the silane into reactive radicals such as SiH_3, SiH_2, and hydrogen, as well as ions, all of which may be involved in film growth. The radical formation products can be represented by [7]:

$$SiH_4 \Longrightarrow SiH_3 + H \tag{5.1}$$

$$SiH_4 \Longrightarrow SiH_2 + H_2 \tag{5.2}$$

Under high power, or high pressure conditions, larger molecules can also form, such as [7]:

$$SiH_4 + SiH_2 \Longrightarrow Si_2H_6 \tag{5.3}$$

$$Si_2H_6 + SiH_2 \Longrightarrow Si_3H_8 \tag{5.4}$$

Although the bulk of the plasma is neutral, containing equal numbers of ions and electrons, there is depletion of the highly mobile electrons close to the electrodes, leading to the creation of a positive space charge region. This positively charged region is referred to as the plasma sheath region, and, as a result of this, the plasma sits at a positive potential with respect to the earthed susceptor. Ions will be accelerated across the sheath region, and the effect of this acceleration is determined by the gas pressure and the resulting mean free path. At low gas pressures, there will be large mean free paths, leading to ion bombardment of the substrate. For high gas pressures, there will be many particle collisions in the sheath region, and the energy gained by the ions in the field will be largely dissipated [16]. These two gas pressure regimes are referred to as the α- and γ-regimes, respectively, and are discussed further below.

The plasma deposition processes are schematically shown in Fig. 5.9 [28], where the type of gas-phase process in the plasma is determined by the operating conditions. For low pressures and low RF powers, the primary plasma products are SiH_3 and H radicals and ions. Moreover, the long mean free paths in the low pressure environment support an appreciable ion flux, as well as the neutral radical flux, to the substrate surface. However, in this regime, the power is poorly coupled

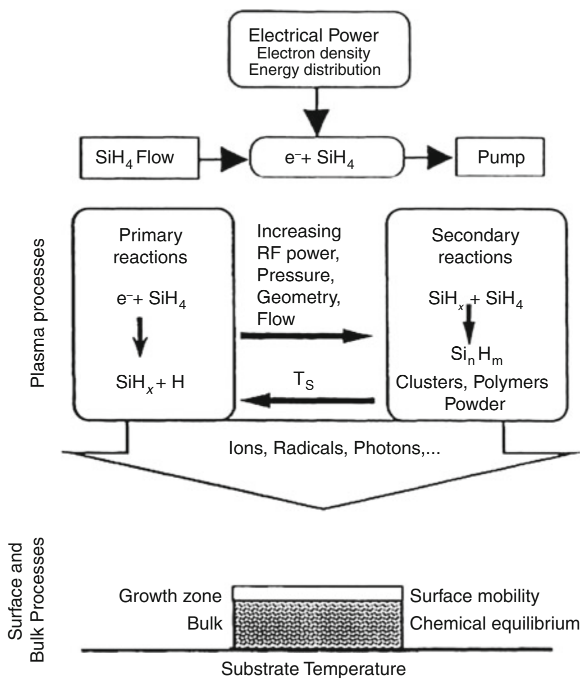


Fig. 5.9 Illustration of the processes involved in the PECVD deposition of a-Si:H (Reprinted from [28] with permission of the IET)

into the plasma, and this, in combination with low dissociation rates, leads to low deposition rates. In contrast, at higher pressures and/or higher RF powers, the power is more efficiently coupled into the plasma, and the silane dissociation rate is increased, leading to higher deposition rates. At the same time, secondary plasma products are formed, such as the higher order Si_nH_m molecules and polymers, and gas phase reactions are stimulated, leading to what are referred to as 'dusty' plasmas. Under well controlled conditions, the negatively charged 'powder' particles are electro-statically contained within the plasma, and high quality, faster depositions can be obtained within this regime [28]. Also, the reduced mean free path at these higher pressures reduces the ion flux to the substrate surface.

The dependence of the film growth rate on the total gas pressure, and the hydrogen:silane dilution ratio, is shown in Fig. 5.10 [23, 25], and two regimes have been identified in this data set. The first regime is the α-regime, giving low growth rates (<100 Å/min), which varied linearly with pressure, and the second regime is the γ-regime giving the higher growth rates, and is associated with 'dusty' plasma conditions. The approximate boundary between the two regimes was at $\sim$130 Å/min. The device and material characteristics were found to depend upon the growth regime, and were most clearly correlated using samples grown either in the α-regime, or in the saturated γ-regime (the transition regime gave variable results) [23]. The influence of the hydrogen dilution ratio was to increase the α-γ transition point to higher gas pressures, and to reduce the deposition rate. In this context, the hydrogen can be regarded as an 'etchant' [29],

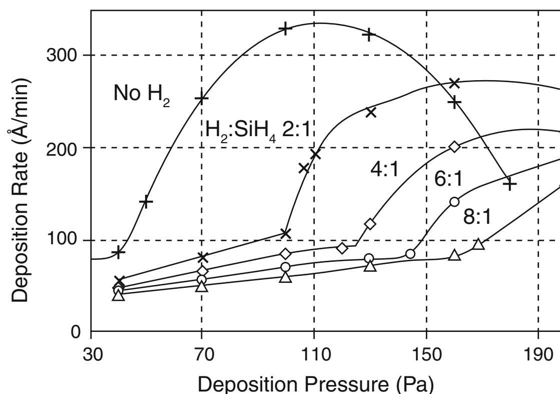


Fig. 5.10 Measured variation of the a-Si:H deposition rate, at 240 °C, as a function of the deposition pressure and the hydrogen: silane dilution ratio (Reproduced with permission from [23])

which selectively breaks weak Si–Si bonds to form volatile silicon hydrides [29, 30], and, under conditions of strong hydrogen dilution (>95 %), leads to the formation of micro-crystalline Si [29]. The α- and γ-growth regimes can be associated with the primary and secondary reaction plasma regimes, respectively [23].

As mentioned above, the two different deposition regimes influenced the performance of TFTs made in these materials, as shown by the carrier mobility and threshold voltage stability results in Fig. 5.11a and b, respectively [23]. These parameters are shown as a function of deposition temperature, with the gas pressure/deposition regime as the independent variable. The figures showed that the α-regime gave the higher electron mobility below ~300 °C, but the two

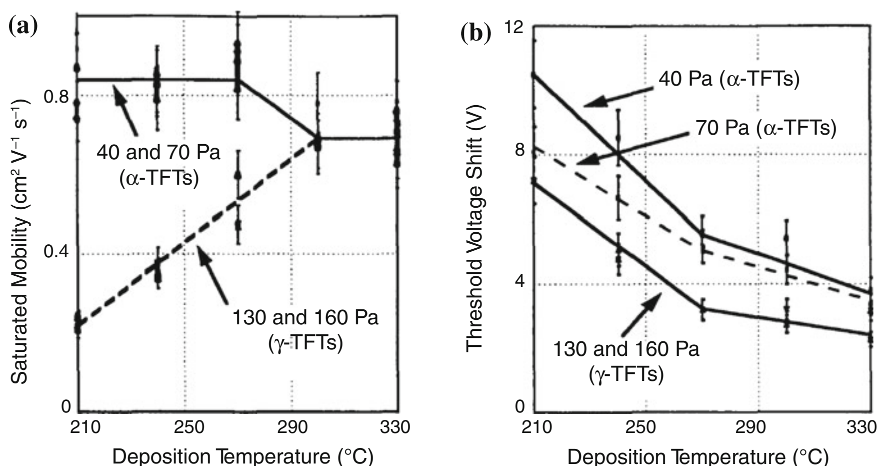


Fig. 5.11 Variation of device properties with deposition temperature and pressure, for depositions with a H_2:SiH_4 dilution ratio of 2:1 (**a**) saturation regime electron mobility, and (**b**) change in threshold voltage after a gate bias stress of 30 V for 1,000 s (Reproduced with permission from [23])

regimes were comparable above this temperature. In contrast, the γ-regime TFTs showed better gate-bias stability, although for both regimes device stability improved with increasing deposition temperature. The optimisation of deposition conditions for device fabrication is to maximise electron mobility, whilst minimising device instability. However, for commercial devices, priority is usually given to stability considerations, in view of its role in determining product lifetime. Hence, the γ-regime deposition at $\sim$300–330 °C is favoured for the industrial fabrication of a-Si:H TFTs. The other constraining factor in commercial depositions is the plate throughput rate, which places a premium on higher deposition rates. In order to optimise both device performance and deposition rate, it is common practice to deposit the a-Si:H film at two different deposition rates [6]. For instance, for a 200 nm thick intrinsic layer in the standard back-channel-etched TFT, the first 50 nm (containing the channel region) are deposited at a slower rate than the final 150 nm [6].

The plots in Fig. 5.11 also illustrate the issues which arise with lower temperature depositions, particularly the reduced gate-bias stability. These effects are discussed further in Sect. 11.4, dealing with a-Si:H TFT processing on low temperature, plastic substrates.

In addition to the dependence of the key device parameters on the deposition regime and temperature, the a-Si:H material itself also shows a variation in its hydrogen bonding pattern. This is usually assessed by infra-red spectroscopy, where the different silicon-hydrogen bonding states are identified by their characteristic vibrational absorption spectra. An illustration of the different bonds, and their vibrational modes, are shown in Fig. 5.12 [31]. The 'SiH' bond represents the $\equiv$Si–H bonding configuration, in which the H is passivating a silicon dangling bond, and its stretching mode has an absorption peak at a wave-number of 2000 cm^{-1}. The poly-hydride 'SiH_2' and 'SiH_3' bonds represent the $= Si = H_2$ and -Si$\equiv H_3$ bonding configurations, respectively, which are more prevalent under high hydrogen concentrations, and have been associated with void formation in the a-Si [7].

FTIR absorption spectra of the α- and γ-regime depositions over the temperature range 210–270 °C are shown in Fig. 5.13 [23]. For the α-regime, the spectra were dominated by the SiH stretching mode at 2,000 cm^{-1}, whereas, in the γ-regime, there were contributions from the stretching modes of both the SiH and SiH_2 bonds at 2,000 and 2,090 cm^{-1}, respectively, plus the 840–880 cm^{-1} doublet. In addition, the SiH_2 bond density decreased with increasing deposition temperature. This reduction in SiH_2 density was accompanied by a reduction in the total chemical concentration of hydrogen within the γ-regime films [23]. For depositions at 300 °C and above, the FTIR spectra for both deposition regimes were the same, showing just the SiH peaks, plus a reduced concentration of the 840–880 cm^{-1} peaks [23]. When comparing the bond configuration results with the TFT results in Fig. 5.11, a link was established between the deposition regime, the specific hydrogen bonding structure, and the TFT performance, at least in terms of electron mobility. However, the device stability appeared to be controlled by factors other than the type of Si/H bonds identified by the FTIR absorption

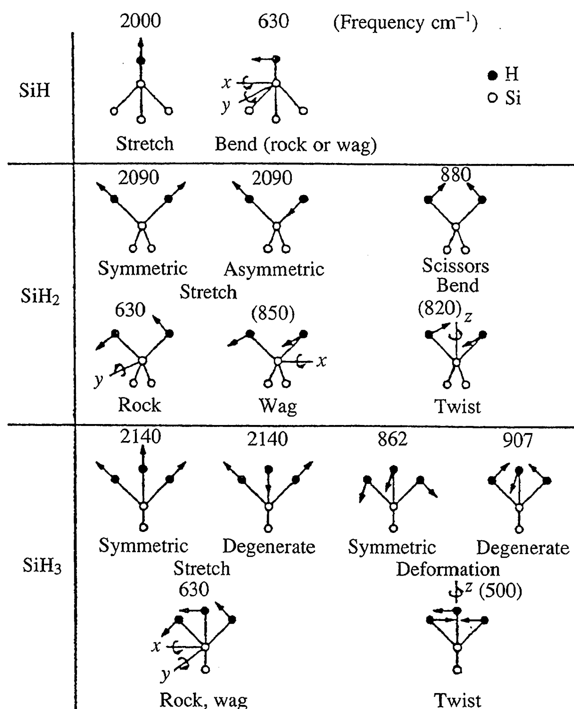


Fig. 5.12 Schematic illustration of the SiH_n vibrational modes, and their associated frequencies, for different SiH bonding configurations (Reprinted with permission from [31]. Copyright (1979) by the American Physical Society)

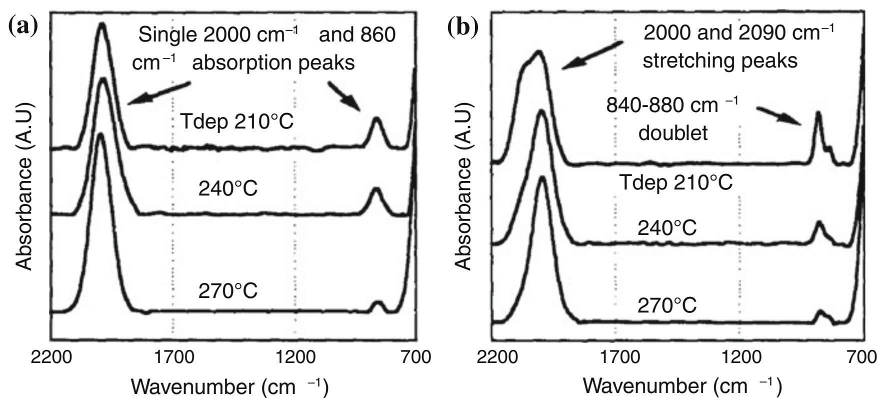


Fig. 5.13 FTIR absorption spectra from a-Si:H layers deposited over the temperature range 210–270 °C, and with a H_2/SiH_4 dilution ratio of 2:1. Depositions in: (**a**) the α-regime at 40 Pa, and (**b**) the γ-regime at 130 Pa. (Reproduced with permission from [23])

peaks [23, 25]. For example, the films deposited in the α-regime displayed increasing levels of intrinsic compressive strain as the deposition temperature reduced (which was attributed to the ion flux in this regime), and this was associated with the increased gate bias instability [25].

In more general terms, a high relative density of SiH bonds has been widely used as a figure of merit for high quality a-Si:H films [7], and the maximisation of the SiH:(SiH_2 + SiH) bond ratio has been empirically used to optimise the deposition conditions, particularly under non-standard conditions, such as at reduced temperatures [24, 26].

So far as the growth process itself is concerned, one of the objectives in understanding the mechanism has been to explain the relatively low concentration of ~10 % hydrogen in the final film, compared with the 75 % hydrogen concentration in the SiH_3 growth radical [32], and how the growth process influences the final defect density within the film [11]. In order to account for this, the growth models have made a distinction between the hydrogen-rich surface layer of the a-Si:H, and the low hydrogen-content of the deeper film, with the mobile SiH_3 radical playing a role in both abstracting hydrogen from the surface, as well as bonding to it [11, 27, 28, 32]. This is illustrated by the atomistic model in Fig. 5.14, in which the SiH_3 radical is shown interacting with the hydrogen-terminated surface in a variety of ways [11]. The primary reaction is physisorption of the SiH_3 radical onto the hydrogenated surface, forming a weak Si–H-Si bond, which permits the radical to diffuse between adjacent sites until it encounters a silicon dangling bond, where a more permanent Si–Si bond is formed. Alternatively, the radical can abstract a hydrogen atom, and be released back into the gas phase as a SiH_4 molecule, thereby creating another silicon dangling bond. With increasing temperature, hydrogen can also be thermally desorbed from the surface creating more dangling bonds, and, hence, increasing the growth rate. Although

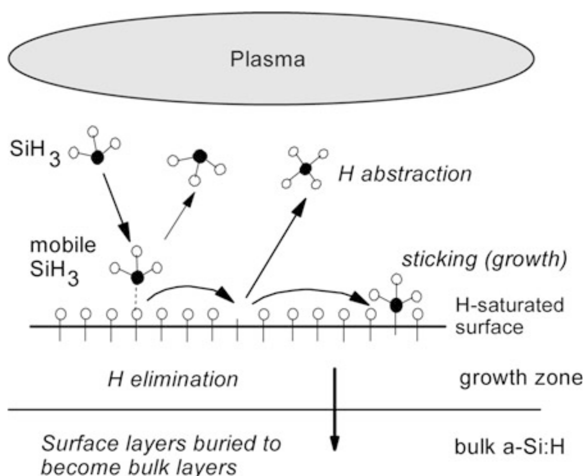


Fig. 5.14 Illustrative diagram of surface processes during the PECVD growth of a-Si:H (the open and solid circles represent H and Si atoms, respectively). (Reproduced with permission from [11])

desorption of the radical from the surface is also shown, this is assumed to be at a negligible rate compared to the other processes [11].

The hydrogen reduction mechanism, when comparing its concentration in the bulk and in the surface layers, occurs by two parallel processes, driven by the substrate temperature and by the plasma conditions (at least over the temperature range of 250 to 400 °C) [11]. The thermal process is one in which the hydrogen concentration is driven down to its equilibrium solubility value of several percent by an out-diffusion process of atomic hydrogen from a sub-surface layer to the surface, where it is released as a H_2 molecule. Even though this requires the hydrogen to diffuse up a concentration gradient, it is diffusing down a chemical potential gradient. The physical explanation of this is that the hydrogen release involves the breaking of Si–H bonds, and it is argued that Si–Si plus H–H bonds are more stable than two Si–H bonds [11].

The plasma component of the hydrogen release process invokes the role of H atoms and ions, particularly in low pressure or hydrogen diluted plasmas. The atoms can abstract hydrogen from the surface and the subsurface regions to form H_2 molecules which effuse from the surface. The H-ions can break sub-surface Si–H bonds by ion impact displacement, and again H_2 diffuses back up to the surface [11]. Hence, ions have a beneficial effect on overall film quality, although they can also contribute to undesirable compressive strain within the films [25], as mentioned above.

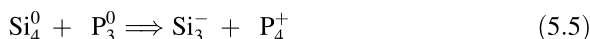
5.5.2 *Doped a-Si:H*

In order to produce the source and drain contact regions, the deposition of doped layers is an important stage in the TFT fabrication process. These layers are produced by introducing phosphine (for n^+ regions), or diborane (for p^+ regions), into the silane pre-cursor gas in the same type of PECVD reactor as used for the undoped layers [33]. Whilst the deposition process itself has not been studied as closely as the deposition process for the undoped layers, there is, nevertheless, extensive information available on the effect of the plasma deposition conditions, as well as the dopant flow rates, on the deposition rate [33]. However, in addition to the characterisation of the deposition process, considerable attention has also been focussed on the doping mechanism.

The early work [3] on doped layer deposition showed that substitutional doping could be observed with both p- and n-type dopants, albeit at a rather low level. For instance, with 1 % phosphine in the PECVD gas mixture, the resistivity of the phosphorus doped region was $\sim 100\ \Omega$cm. Whilst this should not be directly compared with c-Si with 1 % phosphorus doping, which has a resistivity of $\sim 2 \times 10^{-4}\ \Omega$cm, the several orders of magnitude difference between the two materials (which cannot be accounted for by carrier mobility differences alone) suggests very different doping mechanisms.

However, in one sense, what was surprising about these results was that doping was observed at all. The incorporation of impurities into amorphous materials was thought to be governed by Mott's "N, 8-N bonding rule" [4, 7, 34], which describes the preferred bonding coordination leading to the optimum number of covalent bonds. N is the number of valence electrons in the outer shell of the impurity, and the rule states that for $N < 4$, the coordination number will be N, and for $N > 4$, the coordination number will be 8-N. Hence, both group III boron and group V phosphorus atoms would both be expected to have a coordination number of 3 in the a-Si network, and these would be non-dopant sites. In contrast, to achieve the substitutional doping observed in c-Si, they both directly replace Si atoms, and have a coordination number of 4. In the case of the amorphous network, the bonding of the impurity into the relatively flexible network is determined by the valence requirements of the impurity itself, whereas, in the more rigid crystalline lattice, the bonding arrangements are constrained by the lattice [4, 7].

However, given that doping was observed in a-Si:H, it was clear that the '8-N' rule needed modification, and a key proposal was that it should be applied to configurations of both the dopant and host atoms [4]. In particular, the positively charged P_4^+ atom in a dopant site would have the same configuration as neutral four-fold coordinated Si_4^0, and the Si dangling bond state Si_3^- would have the same three-fold coordination as the non-bonding P_3^0 state. Hence, the modified '8-N' rule was applied to the phosphorus/dangling bond defect configuration [4]:



$$Si_4^0 + P_3^0 \Longrightarrow Si_3^- + P_4^+ \tag{5.5}$$

In which the interaction of a three-fold coordinated P-atom with a weak Si–Si bond led to the formation of an ionised P-dopant atom, and a compensating negatively charged dangling bond defect. With increasing P-concentration, the increased occupancy of the negatively charged dangling bond states shifted the Fermi level towards the conduction band edge. This increased the electron occupancy of the tail states, thereby increasing the conductivity of the material (even though most of the P-donated electrons were trapped in the compensating dangling bonds). The model was supported by the experimental observation that the dangling bond density increased with the dopant concentration in the material [4]. Although phosphorus has been used as an example to illustrate the process, the same arguments can also be used for other dopant atoms.

The dopant/defect model successfully describes the doping of both a-Si:H and a-Ge:H with the most commonly used substitutional dopants, as shown by Fig. 5.15. This demonstrates a unique relationship between the total doping efficiency of the materials and the dopant concentration in the plasma gas phase [4, 7]. The figure shows that high doping efficiency was only achieved at very low gas dopant ratios. Thereafter, the efficiency decreased with the square root of the gas dopant concentration, such that, with 1 % dopant in the gas phase, less than 1 % of the dopant in the material was electrically active. This is quite different from the doping of c-Si, in which the dopant displays ~100 % activity. Moreover,

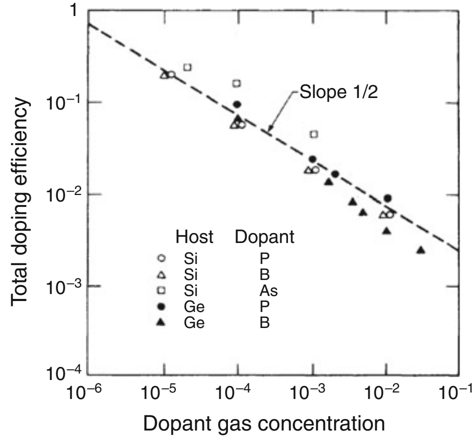


Fig. 5.15 Total doping efficiency of group III and group V impurities in a-Si:H and a-Ge:H, as a function of the gas phase concentration of dopants. (Reprinted with permission from [4]. Copyright (1987) by the American Physical Society)

the common curve, embracing all data points, was only found when relating the doping efficiency to the gas phase dopant concentration, rather than to the more intuitively obvious solid phase dopant concentration [4, 7], as discussed below.

The total doping efficiency, η_T, is defined as the product of the solid phase doping efficiency, η_{sol}, and the incorporation efficiency, η_{inc}, of the dopant from the gas phase into the material. Where these two terms are given by:

$$\eta_{sol} = \frac{N_4}{N_3 + N_4} \tag{5.6}$$

$$\eta_{inc} = \frac{N_3 + N_4}{N_{Si} C_g} \tag{5.7}$$

N_3 and N_4 are the concentrations of P_3^0 and P_4^+, respectively, N_{Si} is the silicon concentration within the film, and C_g is the ratio of the dopant gas concentration to the silane concentration in the plasma chamber. Hence, the total doping efficiency, η_T, is given by:

$$\eta_T \equiv \eta_{sol}\eta_{inc} = \frac{N_4}{N_{Si} C_g} \tag{5.8}$$

and N_4 was experimentally determined from the number of band tail electrons plus the number of dangling bond states resulting from the dopant incorporation [4, 7].

The use of the total, or gas phase, doping efficiency, rather than the solid phase doping efficiency to characterise the doping process, was a reflection of the importance of the plasma deposition process itself. This determined the film growth conditions, the incorporation of the dopant, and the density of weak Si–Si bonds, which participated in the formation of the electrically active doping centres.

5.5.3 a-SiN$_x$:H Gate Insulator

The universally preferred gate dielectric for commercial, inverted staggered a-Si:H TFTs is a form of silicon nitride represented by the expression a-SiN$_x$:H. This indicates that it is both H-rich (20–40 %, depending upon deposition conditions [35, 40]), and does not have the same as stoichiometry as Si_3N_4, which is typically deposited at higher temperatures in the semiconductor device industry. The a-SiN$_x$:H films are deposited by low temperature PECVD, in the same deposition systems used for the a-Si:H active layers, with silane and ammonia as the reactant gases (plus the possible addition of a dilutant gas such as hydrogen [35, 36] or helium [24]). As with the a-Si:H deposition, there is a potentially complex optimisation process involving the gas mixture ratio of NH_3:SiH_4, the gas pressure and flow rates, RF power, and deposition temperature etc. [35], with the aim of tailoring the nitride film's properties to meet the needs of the TFT. These will include minimising the trap state density within the nitride to maximise device stability, controlling its charge density to meet the TFT's threshold voltage requirements [43], as well as controlling the intrinsic stress within the film, all of which need to be achieved in a manner consistent with a commercially acceptable deposition rate. Indeed, as with the a-Si:H deposition, the commercial deposition of 300 nm of gate dielectric a-SiN$_x$:H usually consists of fast growth for the first 250 nm at 200 nm/min, followed by slower growth of the final 50 nm (which is adjacent to the TFT channel) at 100 nm/min [6].

The value of the N:Si ratio, x, in a-SiN$_x$:H films can be established by Auger electron spectroscopy [36] or by Rutherford back-scattering [37, 38], and some early results illustrated the variation of electron mobility and threshold voltage stability with x. The range of x varied from 0.85–1.25, and was achieved by varying the NH_3:SiH_4 gas flow ratio from 1:1 to 4:1 [36]. This work reported better TFT characteristics at x $\sim$1.0–1.1 [36], which, when compared with a stoichiometric value of 1.33, would make these films Si-rich. However, it is now more generally accepted that the preferred a-SiN$_x$:H films are N-rich, with x up to $\sim$1.6–1.7. This is particularly so for films deposited in the aminosilane regime, using large NH_3:SiH_4 gas flow ratios of >12:1 [35, 37–41]. The aminosilane deposition regime is discussed further below.

In much reported work, the N:Si ratio, x, is not quoted, instead, the deposition conditions and device properties are correlated with alternative material parameters, such as the wet-etch rate [38], the refractive index [38], and the optical bandgap [35, 36] of the film, and cross-correlated with the internal bonding structure of the film, as revealed by FTIR absorption peaks due to Si–N, N–H, H–N–H, and Si–H bonds [24, 35, 38, 39]. From these studies, it is recognised that the best a-SiN$_x$:H gate dielectric films are not just slightly N-rich, but also dense, due to a low H-content, and have a low wet-etching rate, a refractive index of $\sim$1.9, and a low Si–H bond density compared with the N–H density.

Whilst a lot of the optimisation of the deposition process was empirical, the examination of the SiH_4/NH_3 plasma chemistry [40, 41] has contributed to the

overall understanding of the deposition process, and, by identifying its critical features, eased the task of transferring a process from one reactor to another [39]. The work identified the tri-aminosilane radical, $Si(NH_2)_3$, as the key plasma species for the deposition of high quality a-SiN_x:H films, and, for a given NH_3:SiH_4 ratio, empirically specified the ratio of RF power to SiH_4 flow rate, which ensured that it was the dominant radical species [39–41]. Amongst the most important deposition conditions was an excess of NH_3 relative to SiH_4 (typically between 12 and 25 times greater [35, 39–41]), together with an adequate gas residence time [39]. This ensured that the NH_n radical density exceeded the SiH_n radical density, and was able to fully aminate the silane, yielding tetra-aminosilane, $Si(NH_2)_4$, and the tri-aminosilane radical, $Si(NH_2)_3$, as the dominant precursor plasma species [40, 41]. These conditions also minimised both the SiH radical density in the plasma, and the Si–H bond density in the film, where a low Si–H bond density has been correlated with a low trap density film [42]. Thus, the well controlled aminosilane plasma was demonstrated to remove Si–H bonds from the a-SiN_x:H films, leaving just Si–N, N–H and H–N–H bonds [39–41], whilst further work, using hydrogen-dilution, demonstrated that the hydrogen incorporation in the film could be further controlled with the removal of H–N–H bonds, resulting in an increase in the film's density and its optical band gap [35]—all of which are indicators of improved film quality.

The preference for a-SiN_x:H, as the gate dielectric in a-Si:H TFTs, is in contrast to the use of SiO_2 as the preferred dielectric in most other Si-based devices, especially c-Si MOSFETs and poly-Si TFTs. The issue with the use of SiO_2 in a-Si:H TFTs is discussed further in Chap. 6, where it is shown that the choice of dielectric is determined not just by the intrinsic properties of the dielectric itself, but by the impact of those properties on the meta-stable defect density in the a-Si:H film [43, 44].

5.6 Novel a-Si:H TFTs

5.6.1 Self-Aligned TFTs

In spite of the commercial dominance of the conventional, inverted staggered BCE structure, a number of investigations have been reported into the fabrication of self-aligned structures, in which the edges of the source and drain regions were automatically aligned to the edges of the gate. The principal reasons for interest in this structure are to remove a critical alignment stage, to reduce the parasitic overlap capacitance between the gate and the source/drain terminals, and as a route to shorter channel length TFTs [45–51]. The majority of these structures were inverted staggered devices [45–49], in which a back-face photolithography stage used the bottom gate to define a pattern in positive photo-resist, on top of the device stack, for subsequent alignment of the source and drain regions. Within this

approach, there were significant differences in the way in which the source and drain regions were actually defined. The other technique used a top-gated structure [50, 51], and the back-face exposure process was avoided. However, this technique used ion-doping to form the n^+ doped regions, either side of the previously defined top-gate (similarly to self-aligned poly-Si TFT fabrication—see Chap. 7), and ion-doping is not a standard stage in a-Si:H TFT fabrication.

One example of the more conventional approach is shown in Fig. 5.16 [48], in which the back exposure of the gate is used to form an etch-stop, ES, TFT, and this architecture has been more widely investigated for self-aligned TFTs [46, 48, 49] than has the self-aligned, back-channel-etched, BCE, architecture [45]. Part of the preference for the ES architecture is that it can be implemented with a thin a-Si:H layer, and this is advantageous for the transmission of the UV lithography radiation through the absorbing a-Si film. The particular process shown in Fig. 5.16 consists of the conventional metal gate definition, followed by the deposition of the a-SiN_x:H/a-Si:H/a-SiN_x:H triple layer stack. Positive photo-resist was used for back illumination lithography, because the areas not exposed to the UV light were retained after the exposure and development of the resist. Hence, the residual resist pattern on the plate surface replicated the gate area, as shown in Fig. 5.16a, and was used as an etch mask in defining the etch-stop a-SiN_x:H layer. In this example, a small amount of resist undercutting was implemented in order to ensure a degree

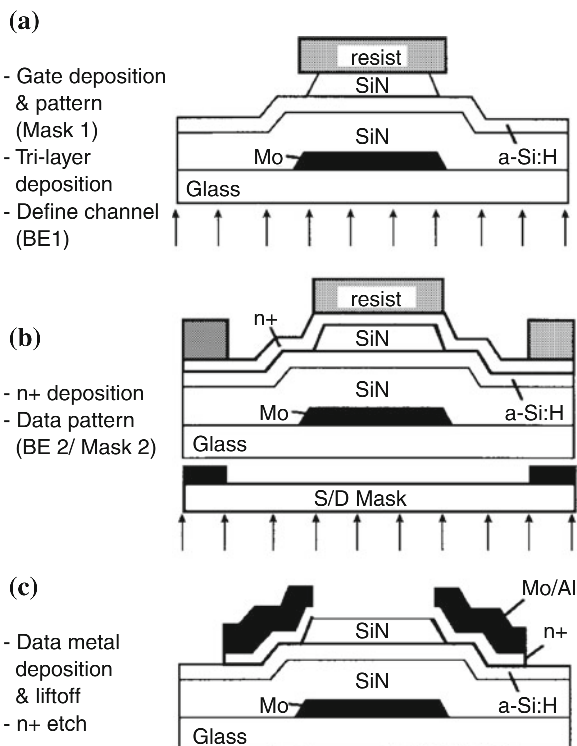


Fig. 5.16 Process steps in the fabrication of a self-aligned, etch-stop a-Si:H TFT, where 'BE' refers to a back-face exposure stage (Reprinted from [48] with permission of IEEE)

of positive overlap of the contacts over the gate. After definition of the etch stop layer, the photo-resist was removed, and the n^+ layer deposited. A second back-face lithography stage, shown in Fig. 5.16b as 'BE 2', used a mask, and defined a new photo-resist pattern, consisting of a self-aligned resist pad over the gate, plus pads each side of it. The whole structure was then coated with the final metallisation material, and immersed in photo-resist solvent, which dissolved the resist, and, in so-doing, removed the metal where it had been directly on top of the resist pads. This is usually referred to as a 'float-off', or a 'lift-off' process. The lift-off process defined the metallisation pattern, which was then used as an etch mask for the subsequent removal of the n^+ a-Si:H layer on the ES pad, and for the removal of the undoped a-Si:H outside the TFT areas, leaving behind a self-aligned ES TFT, as shown in Fig. 5.16c [48].

Other variants on this process have used a single back-face exposure to define the etch-stop pad, and then used an alignment stage to define the edges of the source and drain metal contacts on top of the ES pad [46, 49], with the metal acting as the etch mask for the removal of the n^+ a-Si:H layer, as in the conventional ES process. Hence, this process resulted in a greater overlap of the metal contacts and the ES pad than in the lift-off process, and would be less suitable for short channel devices.

A lift-off process has also been used to form self-aligned BCE TFTs [45], in which only one back-face lithography stage was used to define a photo-resist pad on top of the a-SiN_x:H/a-Si:H/n^+ a-Si:H stack. The top metal was deposited on top of this residual photo-resist pattern, and the metal was selectively removed in a lift-off process. This left a space between the edges of the source and drain metal pads, which was aligned to the gate. The normal back-channel etch was then used to clear the n^+ a-Si:H from this region.

In spite of the variety of processes demonstrated for self-aligned structures, none has been adopted for a-Si:H TFT manufacturing. This is because the standard BCE process is well enough controlled to give the required display performance, and the self-aligned processes introduce greater processing complexity, and, hence, higher manufacturing cost.

5.6.2 Short Channel TFTs

There has been relatively limited interest in short channel a-Si:H TFTs, although device characteristics have been published for channel lengths down to ~1 μm and less [45, 52–56]. These devices have employed some novel architectures, including the self-aligned BCE structure [45], described in Sect. 5.6.1, to achieve 0.4 μm channel lengths, as well as the vertical TFT structure shown in Fig. 5.17 [52]. With this device, the channel length was determined by the thickness of the horizontal layer of a-SiN_x:H, separating the two vertically stacked n^+ source and drain regions, rather than by a photolithographic process. A conventional BCE process has been used for gate lengths down to ~1 μm [54], and a high resolution

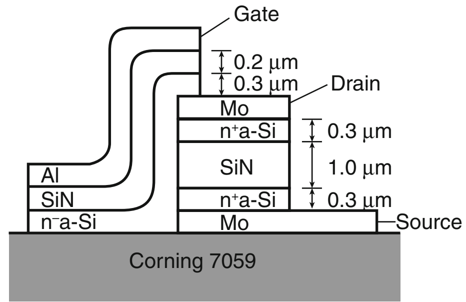


Fig. 5.17 Cross-sectional diagram of a short channel, vertical a-Si:H TFT (Reprinted from [52] with permission of IEEE)

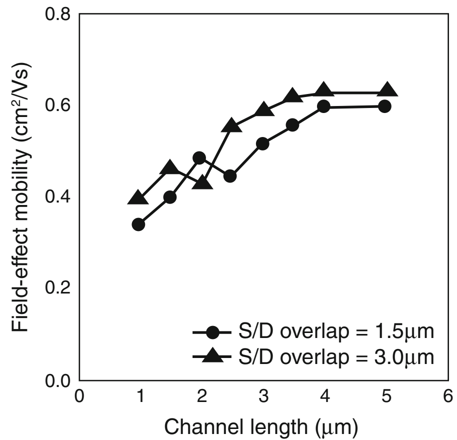


Fig. 5.18 Variation of electron mobility with TFT channel length (Reprinted with permission from [54])

electron beam lithography process, together with metal lift-off, has been used to reduce them to 0.2 μm [55, 56]. A common observation with short channel TFTs was that the on-current did not scale with 1/L [45, 52–55], as shown by the electron mobility results in Fig. 5.18 [54], and this was attributed to series resistance effects in the doped contact regions. In one instance [55], the change of contact metal from Cr to Al gave mobility values which were independent of channel length, and this was attributed to reduced contact resistance due to the diffusion of Al through the contact regions and into the underlying bulk a-Si:H.

The other feature noted in short channel a-Si:H TFTs was an increase in off-state current with reducing channel length for a given source-drain bias [45, 52–56]. This was attributed to space charge limited currents [45], or to field assisted carrier emission processes [56]. However, when devices were measured at a constant channel field (fixed V_d/L), the off-state current dependence on channel length reduced [45, 53, 54], and, in some cases, its value increased with increasing channel length [53, 54]. The latter effect was ascribed to the influence of the increasingly large drain bias itself (rather than the channel field), particularly with the longer channel length TFTs.

5.6.3 Hydrogen-Diluted TFT Depositions

The stimulus for this work [30, 57–59] was the interest in using a-Si:H TFTs for active matrix OLED addressing. As discussed in Chap. 4, the duty cycle of the drive TFTs in an AMOLED display is 100 %, whereas, in AMLCDs, the duty cycle of the addressing TFT is ~0.1 % or less. Given that a-Si:H TFTs are subject to gate bias instabilities [10, 60] (to be discussed in more detail in Chap. 6), the much greater duty cycle in AMOLED displays requires a more stable TFT than those used in AMLCDs. Hence, although the standard a-Si:H TFTs fabricated for AMLCD applications have sufficient stability for that application, an improvement in stability of up to ~1000 times is required for the AMOLED application. This is to ensure that the overall AMOLED display lifetime is not limited by the TFT stability, but that the TFT lifetime at least matches the green phosphorescent OLED lifetime of ~250,000 h (which is defined to be the time for a 50 % drop in brightness) [57, 58].

As mentioned in Sect. 5.5.1, the presence of hydrogen in the a-Si:H deposition plasma can be regarded as a surface etchant species [29], which selectively breaks weak Si–Si bonds, and this effect can be enhanced by increasing the H_2:SiH_4 dilution ratio. Low-field, gate bias instability in a-Si:H TFTs is associated with an adjustment in the number of weak bonds and dangling bonds in response to a change in the Fermi level, or free carrier density, within the device [10]. Consequently, it is argued that by reducing the weak bond density during a-Si:H growth, device stability can be enhanced [30, 57–59]. In this work, the a-Si:H, for ES

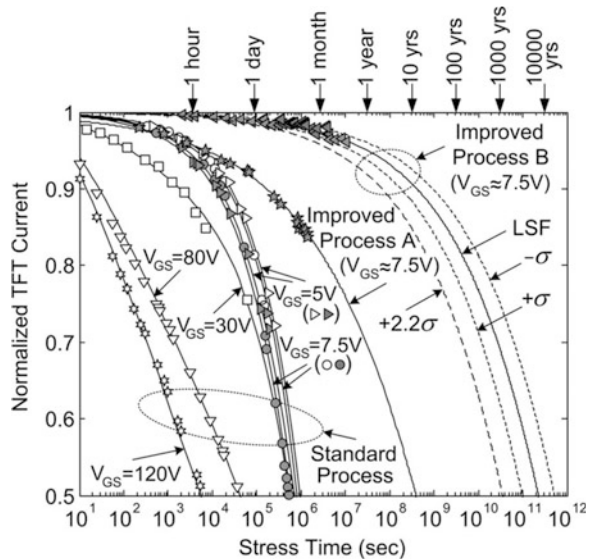


Fig. 5.19 Comparison of normalised TFT channel currents with stress time, for 'standard' and 'improved' a-Si:H TFTs. (The open and closed symbols are for the linear and saturation stress regimes, respectively). (Reprinted with permission from [59]. Copyright (2009) American Institute of Physics)

TFTs, was deposited at 300 °C with a H_2:SiH_4 flow rate of 10:1 [57, 58], and the improvement in device stability is shown by the curve labelled 'Process A' in Fig. 5.19 [59]. These results show the fractional change in channel current with stress time, and were measured under low gate bias and drain saturation conditions (V_G = 7.5 V, and V_D = 15 V) in order to reflect the typical TFT operating conditions in an AMOLED display [58]. However, TFT instability, due to gate bias stress, is usually measured in terms of the change in threshold voltage, $\Delta V_T(t)$, with time. In order to normalise the standard TFT instability results to an equivalent change in drain current at a fixed gate bias, the linear and saturation regime MOSFET device Eqs. 3.11 and 3.17, respectively, were used, i.e.:

$$I_{d(\text{lin})}(t) = \frac{\mu_n W C_i \left(V_G - V_{T0} - \Delta V_{T(\text{lin})}(t)\right) V_D}{L} \tag{5.9}$$

$$I_{d(\text{sat})}(t) = \frac{\mu_n W C_i \left(V_G - V_{T0} - \Delta V_{T(\text{sat})}(t)\right)^2}{2L} \tag{5.10}$$

where V_{T0} is the pre-stress value of the threshold voltage.

The extrapolations of the experimental Process A data in Fig. 5.19 were based upon the measured time dependence of the ΔV_T values, which, in the low gate field regime, have a power law dependence given by [59]:

$$\Delta V_{T(\text{lin})} \approx (V_G - V_{T0})(t/\tau_0)^\beta \tag{5.11}$$

The values of τ_0 and β were determined by fits to the experimental time dependence of the $\Delta V_{T(\text{lin})}$ (t) data, and, in saturation, the following relationship was used:

$$\Delta V_{T(\text{sat})} \approx 2/3 \Delta V_{T(\text{lin})} \tag{5.12}$$

where the 2/3 multiplicative factor was introduced to account for the smaller average free carrier density in the channel of a device operating in saturation [61].

The TFTs labelled 'Process A' in Fig. 5.19, had a standard silane/ammonia a-SiN_x:H layer deposited at 300 °C. A further improvement in device stability, to the curve labelled 'Process B', was obtained with H_2 dilution of the a-SiN_x:H reactant gases, and deposition at 350 °C [59]. It is generally accepted that nitride-limited instability occurs at high gate fields [60], and is caused by carrier tunnelling into nitride traps. However, it was argued here that the change in a-SiN_x:H properties had affected the low-field stability of the subsequently deposited a-Si:H, and this was ascribed to an improvement in its quality close to its interface with the a-SiN_x:H layer [30, 59]. The predicted 'half life' of these TFTs [59] greatly exceeded that of the green phosphorescent OLEDs, and a reduced deposition temperature of 300 °C, for the improved a-SiN_x:H layer, gave a predicted TFT 'half-life' of 8×10^5 h, which was still in excess of the OLED's [30].

Hence, the use of enhanced H_2-dilution for the deposition of both the a-Si:H and the a-SiN_x:H films produced up to five orders of magnitude improvement in

the time to 50 % current degradation in these TFTs, compared with the 'standard' a-Si:H TFTs.

5.7 Summary

The current active matrix flat panel display, AMFPD, industry is built around the ubiquitous hydrogenated amorphous silicon thin film transistor, and this chapter contains an overview of the structure and fabrication processes for these TFTs.

Hydrogenated amorphous silicon is an alloy of silicon with ~10 % hydrogen, in which the hydrogen plays a key role both in passivating dangling bond defects, and in the a-Si:H deposition process itself. The emphasis in this chapter is on the commonly used structures and processes employed in the AMFPD industry, and discussion of the device architecture is largely limited to the inverted staggered TFT. The two variants of this are the back-channel-etched, BCE, TFT, which is widely used in manufacturing, and the etch-stop, ES, TFT, which is often used in research. Both structures consist of an a-SiN_x:H gate dielectric layer, and n^+-doped a-Si:H contacts to the intrinsic a-Si:H transistor body. The BCE configuration is preferred for manufacturing because, in spite of it requiring a well controlled etching procedure to remove the n^+ a-Si:H from the channel area, it has a simpler processing schedule, with fewer deposition and lithography stages. In addition to the details on device architecture, there is also a brief discussion of the issues underlying the design and layout of TFTs.

The formation of the principal device layers, namely the intrinsic and doped a-Si:H, as well as the a-SiN_x:H gate dielectric, is by plasma enhanced chemical vapour deposition, PECVD, in a parallel plate reaction chamber, which is normally driven by a 13.56 MHz RF generator. Silane gas is used for the deposition of all layers, with the addition of phosphine and ammonia for the deposition of the n^+ a-Si:H and a-SiN_x:H layers, respectively. In addition to these primary reactant gases, hydrogen dilution is also used both to control the deposition process, and to influence the bonding structure and electrical properties of the layers themselves.

Whilst the focus has been mainly on the inverted staggered TFT, some novel device structures are briefly reviewed. These include self-aligned and short channel TFTs, as well as high stability TFTs fabricated using enhanced hydrogen-dilution of the PECVD reactant gases.

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Chapter 6
Hydrogenated Amorphous Silicon TFT Performance

Abstract As the dominant device for active matrix flat panel displays, a-Si:H TFTs have been extensively studied, and many of their properties linked to the meta-stability of the defect structure in the material. The topics covered in this chapter include a review of the electronic structure and the material properties of a-Si:H, which are largely determined by the density of states, DOS. The DOS consists of band tail states, due to weak Si–Si bonds, and deeper dangling bond states. Their influence on the threshold voltage and field effect mobility of the TFT is discussed in a semi-analytical fashion, by using an exponential approximation to the DOS. The factors controlling the on-state and off-state characteristics are reviewed, which, apart from the field effect mobility and threshold voltage, include series resistance effects and front channel hole conduction, respectively. Gate bias stress induces threshold voltage instability, due to both defect formation in the a-Si:H layer and carrier trapping in the a-SiN_x:H gate dielectric. The modification of these effects by pulsed bias stressing, and combined gate and drain bias stressing are also reviewed. Finally, a brief overview of defect instability under optical illumination, known as the Staebler–Wronski effect, is presented.

6.1 Introduction

Chapter 5 focussed on the technology of a-Si:H TFTs, and, in this chapter, their performance and device physics will be described. Much of their performance is determined by the material properties and defect structure of a-Si:H, which is discussed in Sect. 6.2, starting with a review of the basic material properties. This introduces the dangling bond and band tail state distributions, and focuses on the meta-stability of the material, which is driven by the hydrogen-mediated equilibration processes between these two types of defects. For practical device modelling, the defect distributions are frequently approximated to by exponential density of states, DOS, distributions across the band-gap. These approximations are used, in a semi-analytical fashion, to examine the impact of the DOS on the relationship between surface band-bending and the equilibrium surface charge density. This

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facilitates a direct comparison with the band bending in c-Si (presented in Chap. 2), and highlights the role of the a-Si:H DOS in controlling threshold voltage and the carrier's field effect mobility. Finally, in Sect. 6.2.5, the role of band bending in defect equilibration in thin films is discussed, and the resulting DOS explains the choice of a-SiN_x:H, rather than SiO_2, as the preferred gate dielectric. It also contributes, together with the wider valence band tail state distribution, to the poorer performance of p-channel TFTs compared with n-channel TFTs.

Section 6.3 deals with more practical, architectural issues of device performance, in particular, the sources of series resistance in the device, and their effect upon the on-state current, and, secondly, the role of the front and back channels on the off-state leakage currents. Section 6.4 reviews the gate bias instability phenomenon in a-Si:H TFTs, which is a major performance limitation in the application of these devices. The intensive study of this effect has led to an improved understanding of the hydrogen-mediated defect formation processes in the material. Finally, Sect. 6.5 contains a brief overview of another meta-stability effect, known as the Staebler–Wronski effect, which results from intense, long duration illumination of the material. This is a more important issue for the long-term performance of a-Si:H solar cells, rather than for TFTs, but is included in the chapter for completeness.

6.2 Defect Structure and a-Si:H Density of States

6.2.1 Basic Material Properties

As briefly discussed in Chap. 5, a-Si:H can be represented by a band diagram, which, in spite of the absence of long range order, is similar to that used for crystalline silicon. This is because with the bond length and bond angle deviations from crystallinity of ~ 2 % and ~ 10 %, respectively, these distortions in the network only correspond to an energy disorder of ~ 0.1 eV relative to the Si–Si bond strength of 2.5 eV [p 62 in 1]. This means that the same molecular orbital considerations can be used to calculate the energy bands (as for the crystalline Si phase), and these are shown schematically in Fig. 6.1. The isolated Si atom has four valence electrons, which are equally divided between the 3s and 3p states, and, to bond tetrahedrally to four other Si atoms, four hybrid sp^3 orbitals are formed containing these four electrons. Each of these can accept another electron from the four surrounding atoms, and the bonding interaction between these lowers the energy of the state, and leads to the splitting of the sp^3 level into the bonding and anti-bonding states, which correspond to the valence and conduction bands, respectively [1, 2]. As shown in the figure, there are s-like states at the bottom of the conduction band and p-like states at the top of the valence band. The p-like states are more affected by bond angle disorder, leading to greater disorder energy, and to the broader tail state distribution adjacent to the valence band mobility edge [p 83 in 1].

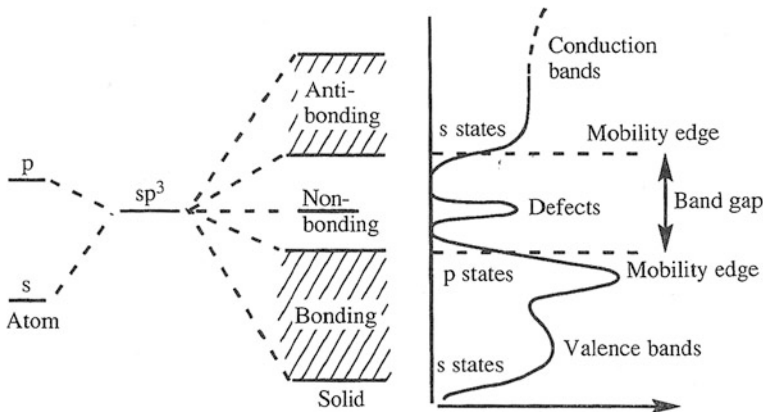


Fig. 6.1 Schematic molecular orbital model of a-Si:H, and its density of states distribution. (From [1], Copyright Cambridge University Press 1991, reproduced with permission)

A broader valence band tail is characteristically found in a-Si:H, and its width is an indicator of the disorder in the material. The band tail width can be extracted from TFT measurements, but it is also common to measure it as a basic material parameter using optical absorption [2, 3]. This assessment of the valence band tail width measures the exponential dependence of the optical absorption coefficient, α, on the photon energy just below the mobility edge. The data was modelled by the following expression:

$$\alpha(E) = \alpha_0 \exp(E - E_1)/E_0 \tag{6.1}$$

which was valid over the absorption coefficient range $2 \times 10^2 < \alpha < 5 \times 10^3$ cm^{-1}, and where the constants $\alpha_0 = 1.5 \times 10^6$ cm^{-1}, $E_1 = 2.2$ eV were obtained from data fitting [3]. The characteristic width of the distribution, E_0, is the Urbach energy [3]. At these near band edge photon energies, the electron transitions are from the valence band tail states to the conduction band. Over a broad set of samples, some of which had been deliberately dehydrogenated to increase the defect density, the Urbach energy was found to lie in the range 50–100 meV [3]. The Urbach energy is a measure of the disorder in the material [2, 3], as demonstrated in Fig. 6.2 by the correlation between the Urbach energy and the dangling bond density in a-Si:H [4]. This data set spanned a wide range of defect densities, and good quality device material sits at the lower end of this range with an Urbach energy of ~50 meV [5]. From a device point of view, the TFTs of most interest are n-channel, whilst the valence band tail states will only affect p-channel TFTs. However, it has been demonstrated that the conduction band tail width scales with the Urbach energy, with it increasing from 19 to 34 meV, as the Urbach energy increased from 45 to 57 meV [6]. Given this correlation, the Urbach energy is widely used as a figure of merit for the material.

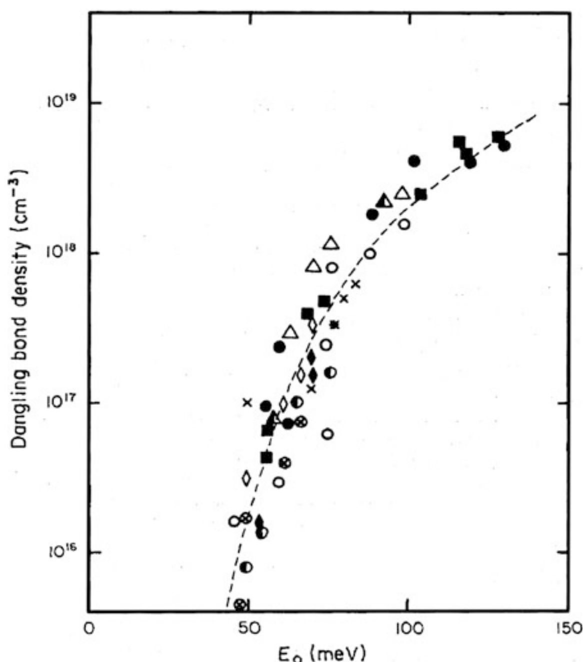


Fig. 6.2 Correlation between the Urbach energy, E_0, and the dangling bond density measured in various types of a-Si:H. (Reprinted from [4] with permission of Taylor and Francis Ltd (http://www.tandfonline.com))

Where there are no bonding interactions, such as at a dangling bond, the sp^3 level remains un-split, and gives the dangling bond, DB, defect energy level near the middle of the band gap.

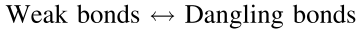
As discussed in Sect. 5.2, the absence of long range periodic order means that electrons occupying the tail states are localised, and give rise to the mobility gap. The size of this gap is defined by the mobility edges, where the extended states begin. However, even in the extended states, the carrier scattering length is of the order of the inter-atomic spacing, giving band mobilities, μ_0, for free electrons and holes of ~10–20 cm^2/Vs, and 1–10 cm^2/Vs, respectively [pp 238–240 in 1, 7]. For carriers confined predominantly in the localised states, the drift mobility, μ_d, recorded in photo-conductivity time-of-flight measurements is defined by [p 73 in 1]:

$$\mu_d = \mu_0 \tau_{free} / (\tau_{free} + \tau_{trap}) \quad (6.2)$$

Hence, the drift mobility is reduced from the band mobility by the ratio of the time, which a thermally excited carrier spends in an extended state, τ_{free}, to its time in a localised state, τ_{trap}. The time-of-flight measurements have shown that, even for high quality a-Si:H, this ratio is <0.1 for electrons, and it is even smaller for holes, due to the broader tail state distribution near the valence band edge. Hence, $\tau_{free} << \tau_{trap}$. A full analytical treatment of this effect for the band tail states [pp 238–240 in 1] is beyond the scope of this discussion, but an appreciation of the physical arguments can be obtained from the carrier capture and thermal emission rate expressions in Sect. 2.3.1. For carriers in deep traps of density N_T, and at an

energy E_T below the conduction band edge, the carrier emission time constant (to release the carrier to the band) is $(c_n N_c \exp\text{-}E_T/kT)^{-1}$, and the capture time constant of the emitted free carrier is $(c_n N_T^0)^{-1}$. (N_T^0 is the density of empty traps, N_c is the effective density of states at the conduction band edge, and c_n is the product of the trap capture cross section and the carrier's thermal velocity). These time constants can be regarded as indicative of the intervals spent by the carrier in the localised and extended states, respectively. Hence, the deeper the trap, the greater the emission time constant, with the residence time of the carrier in the trap increasing exponentially with E_T. For a trap density, which is large compared with the free carrier density, $N_T^0 \sim N_T$, and the capture time constant is independent of E_T. Hence, the ratio of τ_{free} to τ_{trap} will decrease exponentially with increasing E_T. Similar considerations of the fractional division of carriers between the localised and extended states also applies to the field effect mobility, and this is discussed in Sect. 6.2.4.

With the 10 % hydrogen concentration in device grade a-Si:H, the majority of it is contained in Si–H bonds, with two hydrogen atoms being accommodated into the lattice per broken Si–Si bond [8], giving a structure variously designated by SiHHSi or SiHSiH or the H_2^* complex [9]. The latter designations reflect the location of the two passivating hydrogen atoms on the bond-centred (BC) and adjacent tetrahedral (T_d) sites [8]. The hydrogen incorporation relieves the strain in the lattice, but the incorporation itself leaves a residual strain, with the result that, once a minimum strain has been achieved, there remains a steady state density of weak bonds of $\sim 10^{19}$ cm^{-3} [8, 10]. The residual unpassivated dangling bond density of $\sim 10^{16}$ cm^{-3} is formed by the breaking of these weak bonds in the reaction:


Weak bonds ↔ Dangling bonds

The dangling bonds affect the electrical performance of TFTs, as discussed below, and their density can be inferred from measurements of TFT characteristics. In addition, the neutral dangling bond is a paramagnetic centre, with a g-value of 2.0055, which can be detected by electron spin resonance, ESR, measurements [11]. These measurements enable the direct monitoring of the DB density during modification of the material, but are essentially bulk measurements, requiring the use of a sufficient volume of material to yield measurable ESR signals above the detection limit of $\sim 6 \times 10^{11}$ DBs at room temperature. This usually requires stacked films, or films of sufficient thickness, and, in the following work, films in the range 20–90 μm were used, not merely to yield a large enough ESR signal, but also to ensure that the bulk signal dominated any surface signal [11]. a-Si:H is described as meta-stable, as its defect characteristics are frozen-in at $\sim$450–500 K, during cooling from the growth temperature, but, if annealed long enough at lower temperatures, the material will tend to reach a new equilibrium. This equilibration is illustrated in Fig. 6.3 [11], in which the normalised concentration of dangling bonds is shown as a function of annealing time and temperature, and the equilibrium densities are shown as a function of temperature in Fig. 6.3a, b, respectively. Prior to these anneals, the samples were held at 290 °C for 10 min, which was long enough to set the defect density to its equilibrium value at that temperature. These equilibration effects can be represented on the configuration coordinate diagram in Fig. 6.4a, in which the defect formation

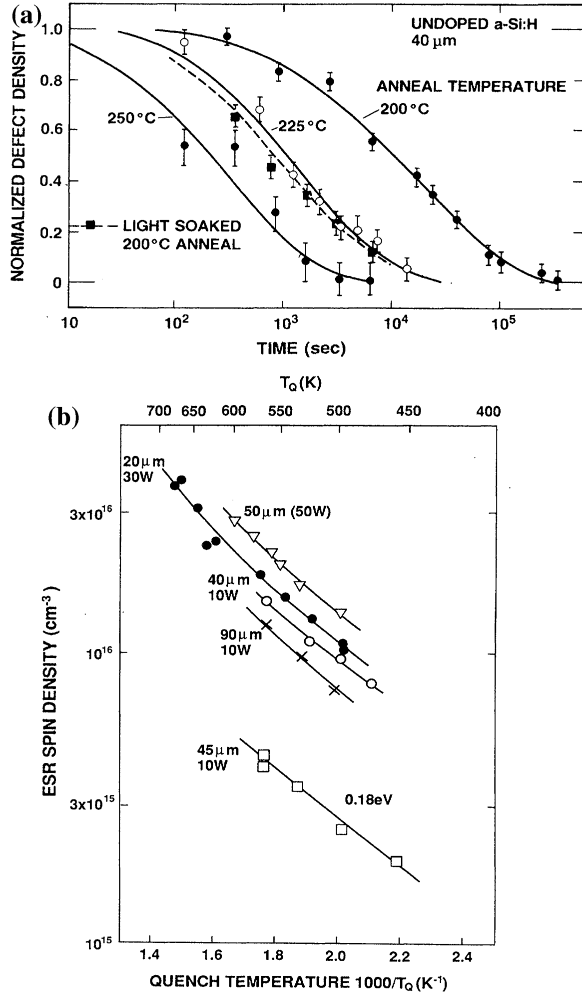


Fig. 6.3 Equilibration of the dangling bond density in a-Si:H after quenching at 290 °C: **a** time dependence at different anneal temperatures (40 μm film deposited at 40 W), and **b** equilibrium density at different temperatures (for different deposition conditions). (Reprinted with permission from [11]. Copyright (1989) by the American Physical Society)

energy, U_d, is the energy difference between the ground state and the defect state, and this determines the equilibrium defect density, N_{de}. In its most generalised form, the relationship between the equilibrium defect density, N_{de}, and the equilibrium weak bond density, N_{WBe}, is given by the law of mass action, where:

$$N_{de} = N_{WBe}\exp - U_d/kT \tag{6.3}$$

(the sum of these two concentrations equals the total weak bond density, N_{WBT}) and, from Fig. 6.3b, $U_d \sim 0.18$ eV [11]. In this simplified discussion, the neutral defect formation energy, U_d, is given by the difference in electron energies of the singly occupied dangling bond state, E_d^0, at 0.6 eV above the valence band

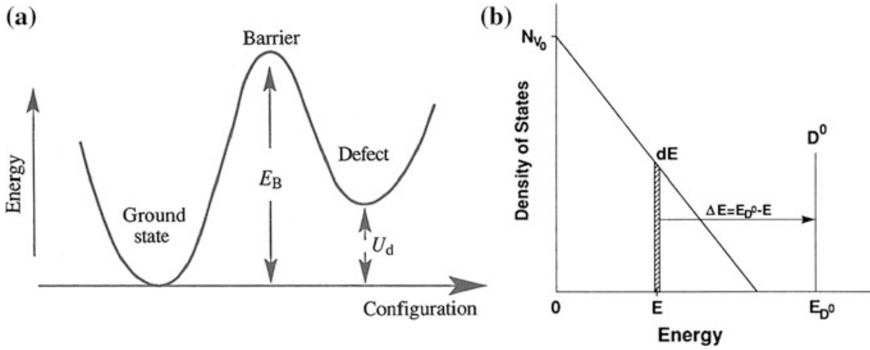


Fig. 6.4 **a** Configuration coordinate diagram showing the barrier between two defect equilibrium states (From [1], Copyright Cambridge University Press 1991, reproduced with permission), **b** schematic density of states diagram illustrating the energy required to create a dangling bond, at E_D^0, from the distribution of weak bond energies (Reprinted with permission from [10]. Copyright (1990) by the American Physical Society)

mobility edge, and the energy of the weak bond, E_{WB}, in the valence band tail state, from which it was formed [11]:

$$U_d = E_d^0 - E_{WB} \tag{6.4}$$

However, for realistic modelling of the process, the number of defects is calculated by integrating the law of mass action over the range of weak bond energies in the valence band tail [10, 11], as illustrated in Fig. 6.4b, where the formation energy at E is:

$$U_d(E) = \Delta E = E_d^0 - E \tag{6.5}$$

and the weak bond density at E is given by:

$$N_{WB}(E) = N_{v0} \exp - E/E_{v0} \tag{6.6}$$

where E_{v0} is the width of the valence band tail state distribution. Hence, the equilibrium dangling bond density, N_{de}, is then given by integrating the law of mass action over all band tail states [10], and:

$$N_{de} = 0.5 \int_0^{\infty} \frac{N_{v0} \exp(-E/E_{v0}) dE}{1 + \exp\{(E - E_d^0)/kT\}} \tag{6.7}$$

Referring back to Fig. 6.4a, the reaction rate for the defect creation process is expected to be thermally activated, with an activation energy given by the defect formation barrier, E_B. The experimental relaxation rate data in Fig. 6.3a showed a temperature dependent equilibration regime, which had a stretched exponential time dependence given by:

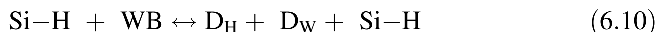
$$\Delta N = \Delta N_0 \exp\left[-(t/\tau)^{\beta}\right] \tag{6.8}$$

and where the time constant, τ, was thermally activated:

$$\tau = \tau_0 \exp E_\tau / kT \tag{6.9}$$

The activation energy, E_τ, corresponds to the defect formation barrier, E_B, shown in Fig. 6.4a. In these samples, the value of E_τ was $\sim$1.5 eV, and β was $\sim$0.6 at 200 °C [11]. The use of a stretched exponential, rather than a single exponential, is indicative of a range of barrier heights, as can be expected from the disordered material, and the value of 1.5 eV can be interpreted as the mean barrier height. The equilibration processes are reversible in response to changes in the annealing temperature. Hence, the formation and removal of the DBs is reversible, as the defect density achieves a new equilibrium value with respect to the weak bond density at different temperatures.

From a study of the reaction kinetics and defect densities, various bonding models have been examined. The simplest is the breaking of a weak bond to yield two dangling bonds; however, it is argued that these two nearby DBs on the same weak bond site would not be paramagnetic, and would not give an ESR signal [11]. The alternative would be for the dangling bonds to separate, but such mobile defects have not been identified [11]. These problems can be resolved by involving mobile hydrogen in defect formation, and two possible models are shown in Fig. 6.5a and b, in which the downward and upward arrows describe defect formation and removal, respectively. The reaction equations are [11]:



$$Si{-}H + WB \leftrightarrow D_H + D_W + Si{-}H \tag{6.10}$$

$$2Si{-}H + WB \leftrightarrow Si{-}HH{-}Si + 2D_H \tag{6.11}$$

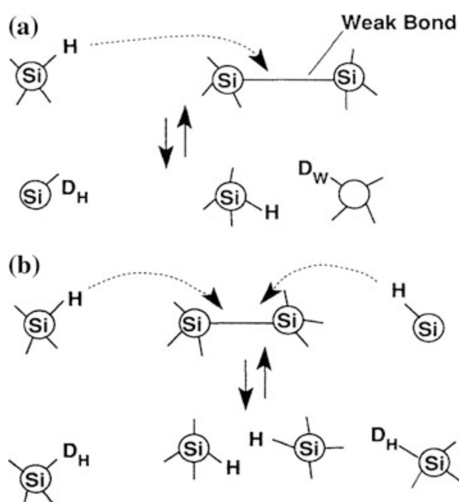


Fig. 6.5 Illustration of two hydrogen-mediated weak bond ↔ dangling bond creation and removal processes. (Reprinted with permission from [11]. Copyright (1989) by the American Physical Society)

Both models show the involvement of hydrogen in the dangling bond formation process. From a thermodynamic point of view, a distinction is made between the isolated dangling bonds, D_H, and those broken bonds on the weak bond site, D_W, which remain adjacent to the nearby hydrogen passivated bond (although these two types of DB may have the same electrical behaviour) [11]. From a comparison of the model predictions with the experimental data, the model shown in Fig. 6.5a was favoured. Clearly, hydrogen is believed to be intimately involved not just in defect passivation, but in the detailed mechanism of defect formation and annealing [9–11].

The above discussions are illustrative of some of the physical considerations employed in analysing the defect formation process. When taking into account specific defect reactions, such as the hydrogen-mediated bond breaking, this more detailed treatment of the topic goes beyond the scope of this book. Furthermore, the above discussion was limited to the formation of the neutral dangling bond, whilst the formation of the charged dangling bond requires further considerations. These include the influence of the different charge states on the defect formation energy, and the changed energy level of the defect itself in the band gap. The latter effect is a direct consequence of the defect not being a discrete level, but having a distribution of energies [9–11], and this topic is briefly reviewed in Sect. 6.2.5. In spite of the limited coverage here, it should be noted that there is an extensive literature on this subject, some examples of which are contained in Refs. [1, 4, 9–11] and the citations therein.

6.2.2 a-Si:H Density of States, DOS

Figure 6.1 showed a molecular orbital model of the a-Si density of states, and many authors have confirmed its general features, as shown by the measured DOS in Fig. 6.6 [12, 13]. The details of the trap distribution were derived by fitting the model to experimental TFT $I_d(V_G, V_d)$ data [13]. The figure shows both the deep state and the tail state distributions, which, from an analytical point of view, can be adequately represented by exponential functions, decaying from the band edges with characteristic energy widths [13–15]. The states in the upper half of the band gap are acceptor-like (which are neutral when empty, and become negatively charged when occupied by electrons), whilst those in the lower half of the band gap are donor-like. As discussed previously, and as shown by Fig. 6.6, the distributions are asymmetric, with a greater density in the lower half of the band gap, such that the Fermi level in undoped material is in the upper half of the band gap [14]. This location also defines the neutral level of the trapping state distribution, where the net charge density is zero. The tail and deep state densities can be approximated by the following exponential distributions:

$$N_{ta}(E) = N_{t0}\exp - (E_c - E)/E_{ta} \tag{6.12}$$

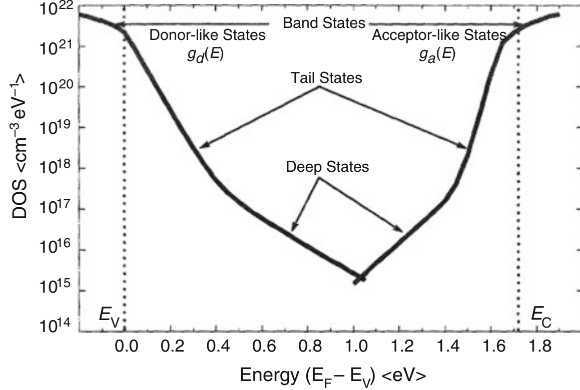


Fig. 6.6 Approximation to the a-Si:H DOS, using different exponential distributions for the tail states and deep states. (Reprinted with permission from [12]. Copyright (1988) American Institute of Physics)

$$N_{da}(E) = N_{d0}\exp - (E_c - E)/E_{da} \tag{6.13}$$

for the acceptor-like tail state and deep states, respectively. Comparable expressions exist for the donor-like states. The values of the parameters N_{t0}, N_{d0}, E_{ta} and E_{da} vary with the sample, but E_{ta} is of the order of 20–30 meV [13, 14], and E_{da} is $\sim$3 times larger. The values quoted for N_{t0} have varied from 2×10^{20} cm^{-3} eV^{-1} to 5×10^{22} cm^{-3} eV^{-1} [13, 14]. Part of this difference is due to the way in which the tail state distribution has been terminated at the conduction band mobility edge, either by using a linear distribution over the intermediate 0.1 eV between the exponential distribution and the band edge [13], or by specifying N_{t0} directly at the band edge [14]. The deep state density, N_{d0}, has been quoted in the range $5 \times 10^{18} - 1 \times 10^{19}$ cm^{-3} eV^{-1} [13, 14]. As an alternative to the exponential approximation for the distribution of deep states, some authors have represented them by a pair of Gaussian distributions [16].

6.2.3 Band Bending and Surface Space Charge

When an a-Si:H TFT is switched on, the surface banding bending, induced by a positive gate bias, will sweep some (or all) of the deep states and tail states through the bulk Fermi level. This means that in order to induce a free electron density, to support on-state conduction, the occupancy of the DOS will change as well. These changes are normally calculated numerically [12–16], but, with some simplifications, it is possible to examine the key features at an analytical level, as discussed below.

For a trapping state distribution given by:

$$N_T(E) = N_{T0}\exp - (E_c - E)/E_T \tag{6.14}$$

the total trap occupancy, with the Fermi level at a position E_F in the upper half of the band gap, is given by:

$$N_T^- = \int_0^{E_C} \frac{N_{T0} \exp -(E_C - E)/E_T}{1 + \exp -(E_F - E)/kT} dE \tag{6.15}$$

This equation is not analytically soluble [15], but, by using the zero Kelvin approximation (in which the states are occupied up to E_F and empty above it), Eq. 6.15 reduces to 6.16. (The limitations in using this approximation are discussed further below).

$$N_T^- = \int_0^{E_F} N_{T0} \exp -(E_C - E)/E_T dE \tag{6.16}$$

from which,

$$N_T^- = N_{T0} E_T \exp - \frac{E_C}{E_T} \left\{ \exp\left(\frac{E_F}{E_T}\right) - 1 \right\} \tag{6.17}$$

With appropriate modification, Eq. 6.17 can be used to describe the local trap occupancy in a surface space charge region, where the band bending is V. This is shown schematically in the MIS band bending diagram in Fig. 6.7a, b, at flat bands and at a positive value of gate bias, V_G, respectively. For simplicity, a symmetric exponential DOS is shown in this figure, with its neutral level at mid-gap, which is where the bulk Fermi level is also located. The DOS is shown only at the a-Si/a-SiN_x:H interface, but it is continuous throughout the bulk of the a-Si, and the acceptor-like state occupancy changes with position in the region within which the bands are bent. The same convention is used as in Chap. 2, in which the potentials are measured from the intrinsic level, so that the local trap occupancy at position x from the surface, where the band bending is V, is given by:

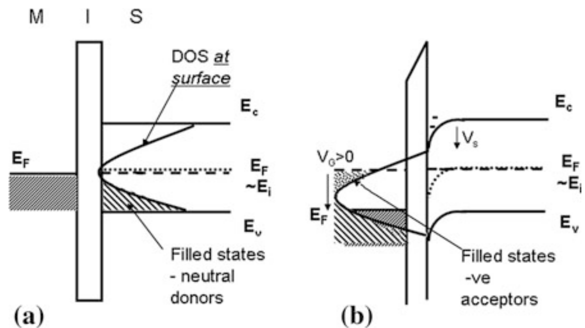


Fig. 6.7 Schematic MIS band bending diagram for a-Si:H, showing trap occupancy: **a** at flat bands—$V_G = 0$ V, and **b** with electron accumulation—+ve V_G. (The traps are spatially distributed in the a-Si:H, but, for illustration purposes, the diagram shows them only at the a-Si:H/a-SiN_x:H interface)

$$N_T^-(x) = N_{T0}E_T \exp - \frac{E_C}{E_T}\left\{\exp\frac{qV}{E_T} - 1\right\} \tag{6.18}$$

and, by referencing all levels to mid-gap, the numerical value of E_C in Eq. 6.18 is half the mobility gap, $E_G/2$.

To establish the relationship between the surface potential, V_s, and Q_s, it is necessary to solve Poisson's equation, where:

$$\frac{d^2V}{dx^2} = -\frac{q\rho(x)}{\varepsilon_0\varepsilon_s} \tag{6.19}$$

ε_0 is the permittivity of free space, ε_s is the dielectric constant of the semiconductor, and the space charge density, $\rho(x)$, for positive gate bias, is:

$$\rho(x) = -n(x) - N_T^-(x) \tag{6.20}$$

$$n(x) = n_i \exp\frac{qV}{kT} \tag{6.21}$$

Substituting Eqs. 6.18 and 6.21 into Poisson's equation, and using the solution procedure of Chap. 2 to obtain the surface space charge density, Q_s, as a function of the surface potential, V_s {i.e. using $\frac{d^2V}{dx^2} = \frac{1}{2}\frac{d}{dV}\left(\frac{dV}{dx}\right)^2$, and integrating Eq. 6.19 from the bulk (V = 0, and dV/dx = 0) to the surface ($V = V_s$, and $dV/dx = -F_s$)}:

$$Q_s \cong -\sqrt{2q\varepsilon_0\varepsilon_s}\left[n_i\frac{kT}{q}exp\frac{qV_s}{kT} + N_{T0}E_T\exp\frac{-E_C}{E_T}\left\{E_T\left(\exp\frac{qV_s}{E_T} - 1\right) - V_s\right\}\right]^{0.5} \tag{6.22}$$

for $V_s > kT$. For comparison, the corresponding expression from Chap. 2 for the c-Si substrate is:

$$Q_s \cong -\sqrt{2q\varepsilon_0\varepsilon_s}\left[n_i\frac{kT}{q}exp\frac{q(V_s - V_F)}{kT} + N_aV_s\right]^{0.5} \tag{6.23}$$

It will be seen that these two expressions have a similar form:

$$Q_s = A[B(V_s) + C(V_s)]^{0.5} \tag{6.24}$$

The first term in Eq. 6.24 relates to the free carrier contribution, and it has a comparable form in both equations, differing only by the non-zero value of V_F in Eq. 6.23 due to the p-type doping of the c-Si substrate. The second term in Eq. 6.24 relates to the immobile space charge. This is due to the ionised acceptor density, N_a, in the c-Si, whilst, in a-Si:H, it is due to the carriers trapped in the DOS. However, these terms have a different form in the two materials, with the N_a term being linear in V_s, whereas the DOS term varies exponentially with V_s. As seen for the c-Si substrate in Chap. 2, the exponential rise of the free carrier term in Eq. 6.23 ultimately led to the free carrier density dominating the surface space

charge density at large enough values of V_s (see Fig. 2.2). In contrast, the fixed space charge term in Eq. 6.22, which increases exponentially with V_s, can increase at a comparable rate to the free carrier term if the value of E_T is of the order of kT. As discussed in Sect. 6.2.2, the width of the tail state distribution beneath the conduction band edge is ~20–30 meV, which is in the same range as the room temperature value of kT. Hence, due to the tail states, there may not be a clear cut situation in which the surface space charge density is dominated by the free carrier density. As will be discussed in Sect. 6.2.4, this has implications for the measurement of the carrier's field effect mobility.

Some illustrative calculations of Q_s as a function of V_s (using Eq. 6.22) are shown in Fig. 6.8a, b. (In performing these calculations, the mobility gap has been taken to be 1.7 eV [12], and the associated intrinsic carrier concentration estimated to be 1.2×10^5 cm^{-3}). In Fig. 6.8a, only a deep level distribution has been used, with $N_{T0} = N_{d0} = 1 \times 10^{18}$ cm^{-3} eV^{-1} and $E_T = E_{da} = 0.1$ eV, and, in addition to the data points for Q_s, the dashed and dotted lines represent the evaluation of Eq. 6.22 using just the free charge or the fixed charge terms, respectively. When one curve or the other is approximately equal to Q_s, this is indicative of that term dominating Q_s. As will be seen in Fig. 6.8a, over most of the surface potential range, Q_s is determined by the trapped charge density, except at the largest values of V_s where the increased rise in Q_s is due to the free carrier charge. If the distribution of deep traps were the only defects in the material, then the device threshold voltage would be where the free carrier density starts to dominate Q_s. However, in practical devices, there is not just a deep level trap distribution, but the tail states are present as well, and this is shown in Fig. 6.8b. In this example, a sum of two exponential trap distributions has been used in Eq. 6.22: the deep level distribution used in Fig. 6.8a, plus a tail state distribution given by $N_{t0} = 2 \times 10^{21}$ cm^{-3} eV^{-1} and $E_{ta} = 0.03$ eV. The curve in Fig. 6.8b looks superficially like the one in Fig. 6.8a, but the important difference is shown by the dashed and dotted curves, which demonstrate that the increase in Q_s, at the larger values of V_s, is mainly due to the charge going into the tail states, and not due to the free carrier density. Indeed, the free carrier density remains a minor contributor to Q_s. The significance of this on the field effect mobility is discussed further in Sect. 6.2.4.

As with the c-Si situation, the gate voltage required to achieve a given surface potential, V_s, is given by Eq. 2.22 from Chap. 2:

$$V_G = V_s - Q_s/C_i \tag{6.25}$$

Hence, as Q_s increases, due to the presence of trapping states, so the value of V_G needed to attain a particular value of surface potential V_s increases accordingly.

The above discussion, and the use of Eq. 6.22, has been introduced to give an analytical appreciation of the effect of the exponential distributions of the mobility gap states on the way in which the surface space charge density is largely determined by these densities, with the free carrier density playing a minor role.

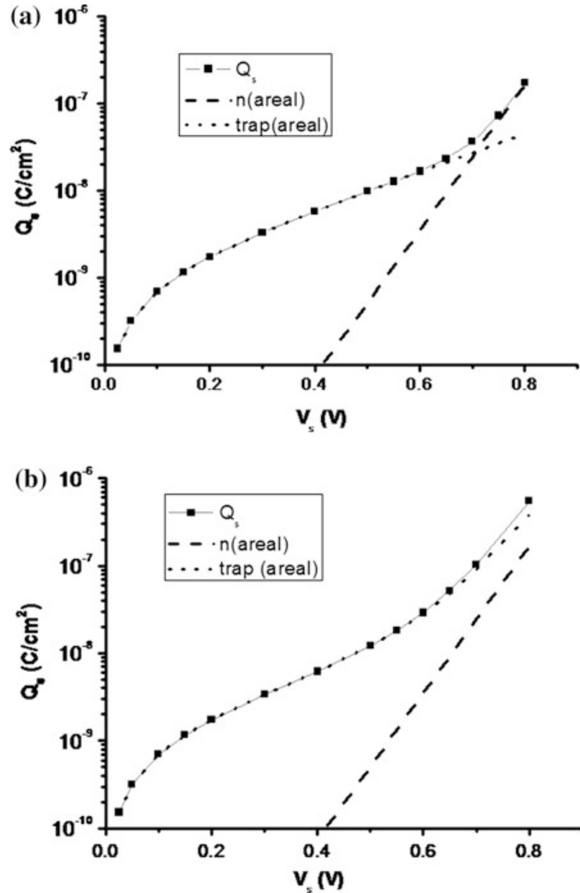


Fig. 6.8 Calculated variation of surface space charge, Q_s, with surface band bending, V_s, (using the analytical approximation in Eq. 6.22): **a** deep level defects only: $N_{da} = 1 \times 10^{18}$ cm^{-3} eV^{-1}, $E_{da} = 0.1$ eV, **b** deep level + band tail defects: N_{da}, E_{da} as above; $N_{ta} = 2 \times 10^{21}$ cm^{-3} eV^{-1}, $E_{ta} = 0.03$ eV. (Q_s—*points* and *solid lines*; trapped charge—*dotted line*; free carrier term—*dashed line*)

However, it should be emphasised that Eq. 6.22 has been derived by using the zero Kelvin approximation, and, particularly for the narrow distribution of the tail states, where $E_{ta} \sim kT$, this approximation cannot be used for a reliable, quantitative calculation of Q_s—it merely gives a qualitative indication of the trends. An accurate calculation requires the use of the Fermi–Dirac function to determine the occupancy of the trapping states (i.e. Eq. 6.15), and an example of the numerically calculated free and trapped charge densities (for the double exponential DOS in Fig. 6.6) is shown in Fig. 6.9 [13]. This is a plot of the free and trapped carrier densities at the a-Si:H surface as a function of the Fermi level at the surface (measured from the valence band edge), where the neutral level is at 1.0 eV (see Fig. 6.6). Hence, the x-axis in Fig. 6.9 is displaced by 1.0 eV compared with the calculations in Fig. 6.8, but, apart from this, there is a clear qualitative similarity between these two figures, including the change in slope of the trapped carrier density, as the Fermi level moved from the deep states into the band tail states. The filling of the deep states, and the movement of the Fermi level into the tail states,

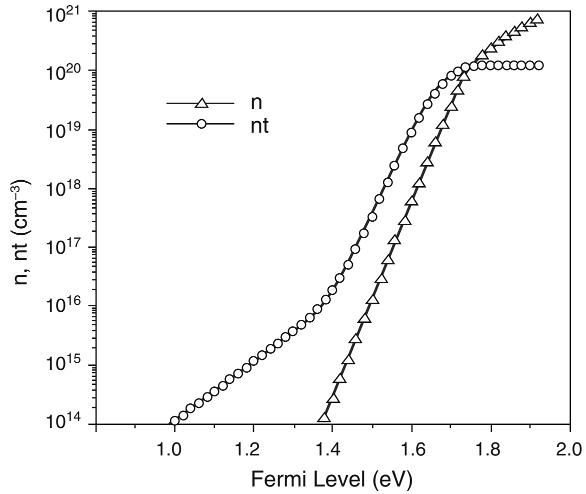


Fig. 6.9 Numerically calculated free and trapped electron densities as a function of the surface Fermi level position, using the DOS in Fig. 6.6. (Reprinted with permission from [13]. Copyright (1989) American Institute of Physics)

has been empirically identified as the threshold for on-state behaviour in a TFT [13, 17, 18], such that the value of the deep state density will determine the TFT threshold voltage through Eq. 6.25. Figure 6.9 also shows that the free carrier density remains below the trapped charge density, over much of the band bending range, and the effect of this on the field effect mobility is discussed in the next section. Finally, at the larger values of E_F in Fig. 6.9, the Fermi level is above the conduction band edge, leading to a 'crystalline-like' regime of operation at very high gate voltages, where the band mobility for electrons would be attained. However, this regime has not been achieved in practical devices [19, 20].

Only the surface carrier densities are shown in Fig. 6.9, and similar calculations to those in the figure have examined the spatial distribution of trapped and free carriers within the bulk of the surface band bending region [19]. For representative values of band bending below and above threshold, such as 0.4 and 0.6 eV, respectively (equivalent to $E_F = 1.4$ and 1.6 eV in Fig. 6.9), the relative densities in the bulk closely followed the ratios at the surface.

6.2.4 Field Effect Mobility

As discussed in Sect. 3.3.1, the carrier mobility can be extracted from the experimental relationship between the drain current, I_d, and gate bias, V_G, in either the linear or the saturation regimes of the TFT on-state characteristic. The following discussion uses the linear regime characteristics as an example, but the principle applies to both regimes. From Eq. 3.11 in Sect. 3.3.1, the I_d–V_G relationship (for small V_D) is given by:

$$I_d = \frac{\mu_n W C_i (V_G - V_T) V_D}{L} \tag{6.26}$$

and the electron field effect mobility, μ_{FE}, is derived from the slope of the I_d–V_G curve above V_T, using:

$$\mu_{FE} = \frac{L}{W C_i V_D} \frac{dI_d}{dV_G} \tag{6.27}$$

Implicit in this relationship is the assumption that, for $V_G > V_T$, all the charge induced in the surface by the gate voltage is free charge. In other words, the areal free charge density, Q_n, is given by:

$$Q_n = C_i(V_G - V_T) \approx Q_s \tag{6.28}$$

This means that Q_n is approximately equal to the total charge density, Q_s. This was clearly the case for the Q_s calculations shown in Fig. 2.2 for $V_s > 2V_F$, and is approximately the case for the large V_s values in Fig. 6.8a, but is not the case in either Figs. 6.8b or 6.9 where a realistic tail state distribution was used in the a-Si:H DOS. In these latter cases, it is necessary to modify Eq. 6.27 to take account of the division of induced charge between free carriers and trapped carriers. Writing Eq. 6.27 as:

$$\mu_{FE} = \frac{L}{W C_i V_D} \frac{\Delta I_d}{\Delta V_G} \tag{6.29}$$

Where, from Eq. 6.26:

$$\Delta I_d = \frac{\mu_n W V_D \Delta Q_n}{L} \tag{6.30}$$

$$\Delta V_G = \frac{\Delta Q_s}{C_i} \tag{6.31}$$

$$\Delta Q_s = \Delta Q_n + \Delta Q_t \tag{6.32}$$

and ΔQ_t is the fixed space charge in traps. Substituting Eqs. 6.30 and 6.31 into 6.29 establishes the relationship between the field effect mobility and the band mobility, μ_n:

$$\mu_{FE} = \mu_n \frac{\Delta Q_n}{\Delta Q_s} \tag{6.33}$$

Hence, when the free carrier density dominates the surface space charge (and $\Delta Q_n \sim \Delta Q_s$) $\mu_{FE} \sim \mu_n$ (as is the case for c-Si devices). However, for a-Si:H TFTs with band tail states, $\Delta Q_n < \Delta Q_s$, and consequently $\mu_{FE} < \mu_n$. For a quantitative evaluation of this effect, a numerical integration of the free and trapped charge through the film is required. This is shown in Fig. 6.10 [12], in which the calculated ratio of the electron field effect mobility to the band mobility has been

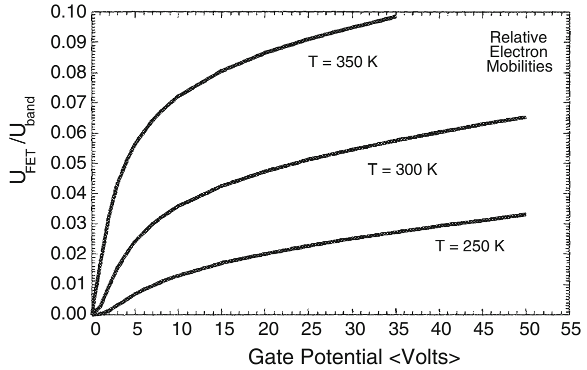


Fig. 6.10 Calculated ratio of electron field effect mobility to electron band mobility, using the DOS in Fig. 6.6 (thickness of a-SiN_x:H was 300 nm). (Reprinted with permission from [12], Copyright (1988) American Institute of Physics)

evaluated for the DOS in Fig. 6.6. This figure shows that the ratio increases both with gate bias, due to differential trap and band occupancy, and with temperature due to increased thermal occupancy of the conduction band. At $V_G = 15$ V, the room temperature ratio is ~0.04, which, for a band mobility of 10–20 cm^2/Vs, gives a field effect mobility of ~0.4–0.8 cm^2/Vs. This is consistent with the electron field effect mobility of ~0.4–1.0 cm^2/Vs measured in a-Si:H TFTs [21], an example of which is shown in Fig. 6.11. This back-channel-etched TFT had a-Si:H and a-SiN_x:H film thicknesses of 200 and 400 nm, respectively, and a threshold voltage and field effect mobility of ~3 V and 0.60 cm^2/Vs, respectively.

Equation 6.33 shows that the field effect mobility is equal to the band mobility reduced by the ratio of the free carrier density to those trapped in band tail states, and this is essentially the same as the drift mobility, which is also of the order of 1 cm^2/Vs for electrons [7].

Whilst this section has focussed on a-Si:H TFTs, other TFT technologies have also been characterised with a distribution of trapping states across the band gap, and similarly show differences between the field effect and the band mobilities. Therefore, the discussion in this section is broadly applicable, although the

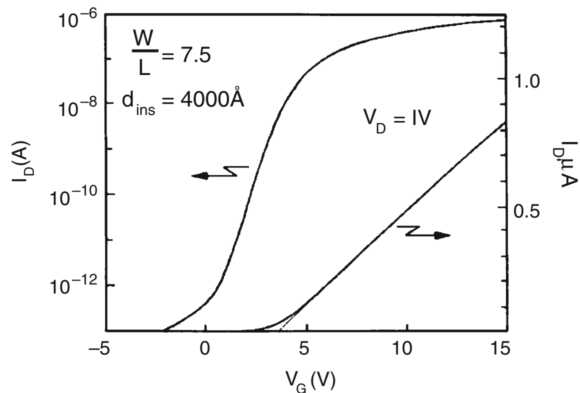


Fig. 6.11 Experimental, linear regime transfer characteristics of a back channel etched a-Si:H TFT. (Reprinted from [21] with permission of IEEE)

particular mobility ratio will depend upon the detailed trapping state distribution within the material. For instance, the analysis of large grain, high mobility poly-Si TFTs has identified a μ_{FE}:μ_n ratio of 0.55 [22].

6.2.5 Equilibration in Thin Films

The effects to be discussed in this section are not specific to thin films, but the thin films used in TFTs make them particularly sensitive to the influence of surface band bending during device fabrication. The background to the process of dangling bond equilibration was introduced in Sect. 6.2.1, in which the monitoring of the bulk equilibration process used ESR measurements on undoped samples up to 90 μm thick [11]. In the layer thickness range suitable for TFTs (i.e. <0.5 μm), the surfaces play a relatively much greater role in determining the detailed electronic properties of the resulting material. These electronic effects are controlled by the Fermi level position during equilibration, and this ultimately determines the choice of gate dielectric material, and the preferred channel type, as discussed in the following two sub-sections. Not only is the equilibrium defect density determined by the Fermi level position during equilibration, but it also influences the position of the DB states within the mobility band gap. The reason why these effects are so important in thin films is because the Fermi level at the surface is determined by the surface band bending, which in turn is controlled by the charges in the gate dielectric during the cooling of the TFT stack from its deposition temperature to the freeze-in temperature. As discussed in Sect. 5.2, the dangling bond is a positive-U amphoteric centre, with an acceptor level at E_{d2}, and a donor level at E_{d1} (see Fig. 5.2). Hence, if there is positive charge in the gate dielectric, the bands will be bent down, and the surface Fermi level will be positioned closer to the conduction band edge, such that, if it is above the acceptor level of the defect state at E_{d2}, the state will be negatively charged. Conversely, if the dielectric layer has a net negative charge, the bands will be bent upwards, and the dangling bond will be positively charged if the surface Fermi level is below the donor level at E_{d1}. The movement of the surface Fermi level towards either of the band edges has two effects: it changes the defect formation energy of the charged states compared with the uncharged state, and, as the defect levels are distributed in energy, the resulting DB energy levels are also shifted from the levels formed in near-intrinsic material [Chap. 6 in 1, 9–11]. The formation energies are changed due to the change in electron energies associated with the charged defect states. In the simplified presentation in Sect. 6.2.1, the defect formation energy for the neutral state, was given by Eq. 6.4:

$$U_d\left(D^0\right) = E_{d1} - E_{WB} \tag{6.34}$$

Continuing with the same simplified formalism for the charged states, the formation energy for the negatively charged state, at E_{d2}, becomes [p 195 in 1]:

$$U_d(D^-) = E_{d1} - E_{WB} - (E_F - E_{d2}) \tag{6.35}$$

The formation energy is reduced by $E_F - E_{d2}$, which is the gain in energy due to an electron falling from the Fermi level, E_F, down to the upper level of the dangling bond at E_{d2}. For the positively charged state, with E_{d1} above the Fermi level:

$$U_d(D^+) = E_{d1} - E_{WB} - (E_{d1} - E_F) \tag{6.36}$$

In this case, the defect itself is empty of electrons, and the formation energy of the neutral defect is reduced by the electron dropping from the defect level down to E_F. From the law of mass action, these changes in defect formation energies will change the equilibrium defect densities, compared with the density produced in intrinsic material.

As mentioned in Sect. 6.2.1, the above analysis is simplified by the assumption of a single weak bond defect level at E_{WB}, whereas, in reality, the calculation of the equilibrium number of charged defects will require the law of mass action to be integrated over the valence band tail state distribution [10, 11].

Finally, as the defect levels are distributed in energy, the defect formation process will naturally select those states with the lowest formation energy, and, for a Gaussian distribution of defect energies with a width σ_D, the change in defect energy level, ΔE, for each added electron during the formation process is given by [p 196 in 1]:

$$\Delta E = -\sigma_D^2 / E_{v0} \tag{6.37}$$

where E_{v0} is the width of the valence band tail state distribution. The shifts in the equilibrated defect energy levels with the position of the Fermi level during DB formation are illustrated in Fig. 6.12, in which, for $\sigma \sim 0.1$ eV, $\Delta E \sim 0.2$ eV [p 196 in 1]. It will be seen that, with the Fermi level in the lower half of the band gap, the positively charged, empty defect centre is formed at a high position in the band gap. With higher Fermi level positions during defect formation, the addition of each electron to form either the neutral or negatively charged levels causes those levels to be formed progressively lower in the band gap. For each Fermi

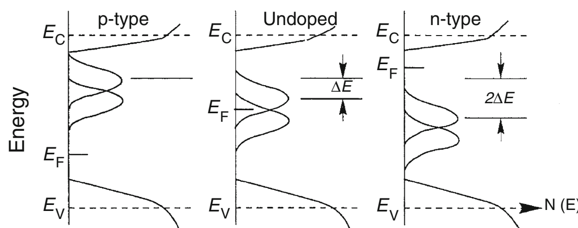


Fig. 6.12 Illustration of the a-Si:H DOS, showing the dependence of the dangling bond energy levels on the position of the Fermi level during defect formation. (From [1], Copyright Cambridge University Press 1991, reproduced with permission)

level position during defect formation, the associated donor and acceptor energy locations are shown in Fig. 6.12, and it should be emphasised that these energy levels are frozen-in during cooling from growth. At room temperature, the frozen-in distribution will not change, but the room temperature Fermi level can be moved through the distribution, by surface band bending, thereby changing the occupancy of the frozen-in centre.

As with the discussion of the neutral defect in Sect. 6.2.1, the presentation above is highly simplified, in order to bring out the underlying physical arguments, and for a more comprehensive overview and treatment the reader is referred to Ref. [9].

6.2.5.1 Gate Dielectric

The preferred gate dielectric for a-Si:H TFTs is a-SiN_x:H, which has a large density of positive charge in the dielectric, and this might be expected to lead to depletion devices with large negative threshold voltages [23]. However, this intuitive expectation does not happen, as discussed below. On the other hand, SiO_2 is preferred in c-Si MOSFETs, and has a much lower charge density, which might be expected to lead to a threshold voltage closer to zero volts. Again, this does not happen in practice. To examine the impact of the intrinsic dielectric charge on the equilibrated defect density in a-Si:H TFTs, devices were annealed at 240 °C for 10 min with different biases on the gate electrode to simulate the effect of different charge densities in the dielectric during sample preparation. To avoid charge trapping effects in the normal a-SiN_x:H gate dielectric, it was replaced by a thermally grown layer of SiO_2 on a heavily doped Si substrate, which also acted as the gate electrode [24, 25]. The impact of differently biased equilibration regimes on n- and p-channel TFT characteristics are shown in Fig. 6.13a, and simulated results are shown in Fig. 6.13b. These are normalised transfer characteristics, showing the channel sheet conductance versus the total charge density induced by the gate measurement bias. Also, by using both p- and n-channel TFTs, the defect distribution in both halves of the band gap could be assessed [24]. For the n-channel TFTs in Fig. 6.13a, the devices with the lowest density of states in the upper half of the band gap had the sharpest sub-threshold slopes, and were obtained with a positive gate bias anneal (placing the Fermi level close to the conduction band at the surface). Conversely, those with the highest defect density had the lowest sub-threshold slope, and were obtained with a negative bias anneal. The devices annealed at zero bias are representative of the native charge density in the oxide films, and gave intermediate results in terms of n-channel behaviour. Given the correlation between the sub-threshold slope and the defect density in the upper half of the band gap, these results showed that superior n-channel performance was obtained when the Fermi level was in the upper half of the band gap during the equilibration process. Conversely, this equilibration condition degraded p-channel performance.

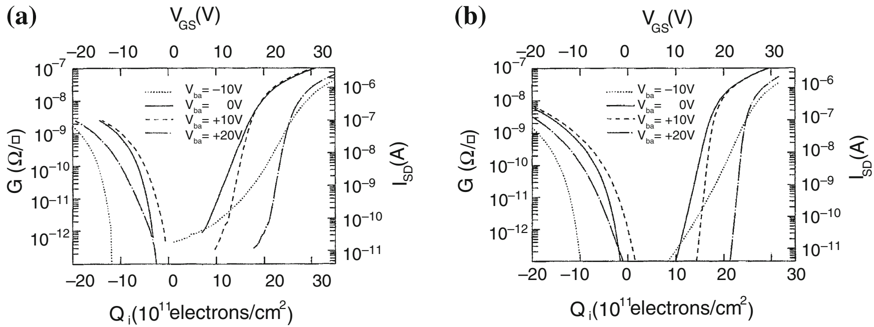


Fig. 6.13 Transfer characteristics of n- and p-channel a-Si:H TFTs with an SiO_2 gate dielectric, in which the dangling bond density was equilibrated with different gate biases, V_{ba}: **a** measured after equilibration at 240 °C, and **b** simulations. (Reprinted with permission from [24]. Copyright (1993) American Institute of Physics)

The simulations in Fig. 6.13b included constant band tail state densities and a spatially varying DB density, where the densities at the a-Si:H/SiO_2 interface, and in the bulk, are shown in Fig. 6.14. They demonstrate that a positive bias anneal positions the minimum of the surface defect distribution above mid-gap (leading to the enhanced n-channel performance), and causes the peak of the defect distribution to be located below mid-gap (thereby degrading the p-channel performance). The opposite effects are seen with the negative bias anneal. As will be appreciated, the positioning of the peaks in the defect distributions at the surface correlate with the surface Fermi level position during bias equilibration, and are consistent with the Fermi level effects illustrated in Fig. 6.12. A related feature in Fig. 6.14 is the difference between the surface DB densities and those in the bulk, illustrating that the defect density is spatially varying, and is due to the spatial variation in the separation of the Fermi level and the band edges within the band bending region. Moreover, the defect distribution in the neutral bulk is more

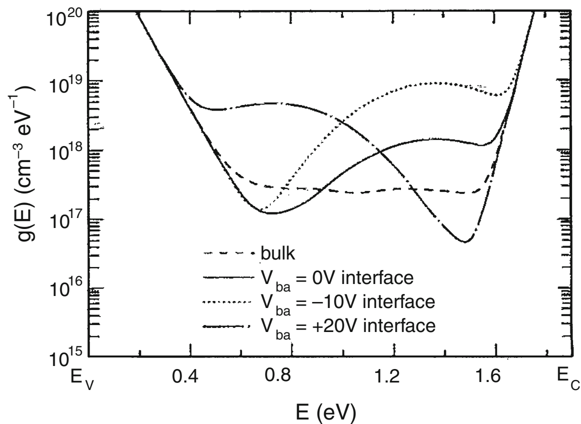


Fig. 6.14 Spatially varying DOS used in the defect equilibration simulations in Fig. 6.13b. (Reprinted with permission from [24]. Copyright (1993) American Institute of Physics)

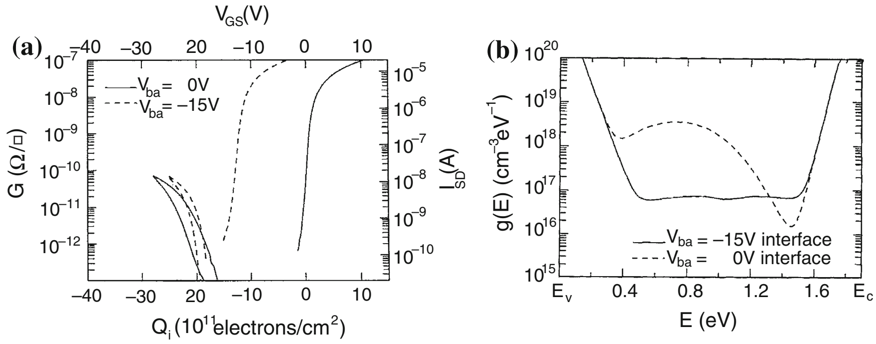


Fig. 6.15 **a** Transfer characteristics of n- and p-channel a-Si:H TFTs, with an a-SiN_x:H gate dielectric, in which the dangling bond density was equilibrated with different gate biases, and **b** interfacial values of the spatially varying DOS used to simulate the results in (**a**). (Reprinted with permission from [24]. Copyright (1993) American Institute of Physics)

evenly distributed across the middle of the band-gap, as expected when the Fermi level is near mid-gap. In summary, the changes in the density and energy location of the defects frozen-in after the equilibration anneals are consistent with the Fermi level effects discussed in the preceding section, and are a key feature of the defect pool model of defect formation in a-Si:H [24].

In support of the conclusions drawn from Fig. 6.13a, the transfer characteristics of a conventional a-Si:H TFT, with an a-SiN_x:H gate dielectric, containing a fixed positive charge density of 11.1×10^{11} cm^{-2} have also been studied [24]. To reduce the effects of charge injection into the dielectric, the bias annealing conditions were limited to 0 V and −15 V. The measured characteristics are shown in Fig. 6.15a, and the defect distribution used to simulate them is shown in Fig. 6.15b [24]. The device annealed at zero bias had near ideal characteristics, and the simulated defect distribution, in Fig. 6.15b, had the same minimum defect density in the upper half of the band gap (and a peak in the lower half of the band gap) as the oxide samples annealed with positive gate bias. Moreover, if the zero bias annealed SiO_2 sample is compared with the zero biased a-SiN_x:H sample, it is clear that the large positive fixed charge density in the latter gave superior TFT performance, and explains the universal preference for the a-SiN_x:H gate dielectric. In addition, the high defect density in the lower half of the band gap reduces hole conduction at negative gate biases in the off-state of n-channel TFTs [23, 24].

6.2.5.2 n- and p-Channel TFTs

From the density of states distribution shown for the conventional a-Si:H TFT in Fig. 6.15b, it is clear that the fabrication process which delivers a low dangling bond defect density in the upper half of the band gap, also delivers a density which is ~100 times greater in the lower half. As discussed in Sect. 6.2.3, this high

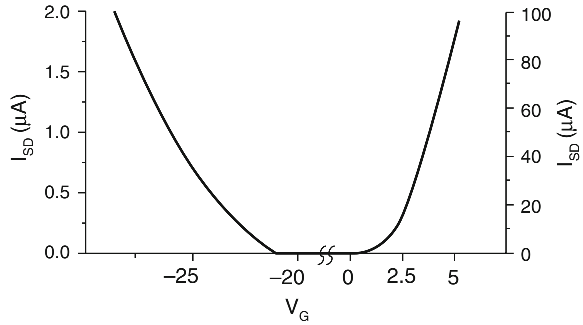


Fig. 6.16 Transfer characteristics measured on n- and p-channel ambipolar TFTs. (Reprinted with permission from [26]. Copyright (1987) American Institute of Physics)

defect density will have a direct impact upon the threshold voltage of p-channel TFTs, by making it more negative. This is apparent in the transfer characteristics shown in Fig. 6.15a, and is more directly shown in the comparison of the n- and p-channel linear regime characteristics in Fig. 6.16 [26]. These show that the threshold voltage of the p-channel TFT was ~−23 V compared with ~2.5 V for the n-channel TFT. In addition, the greater density of valence band tail states, compared with the conduction band tail states, will further reduce the hole field effect mobility from its band value. The field effect mobility is usually calculated from Eq. 6.27; however, for devices with identical geometries, Eq. 6.26 shows that the simple ratio of their on-currents is indicative of the ratio of their field effect mobilities. From an inspection of the current scales in Fig. 6.16, it is clear that the hole field effect mobility is ~50–100 times less than the electron field effect mobility. Hence, this data set indicates a hole field effect mobility of ~0.005–0.01 cm^2/Vs. This is of the same order as the hole drift mobility of 0.003 cm^2/Vs [7], and, as discussed in Sect. 6.2.4, these two measurements are essentially measuring the same quantity, which is the band mobility reduced by the ratio of carriers in extended states to localised band tail states.

In summary, the large threshold voltage and the very low field effect mobility of p-channel a-Si:H TFTs explain the universal preference for n-channel TFTs in commercial applications.

6.3 TFT Characteristics

6.3.1 On-State

The on-state characteristics are determined, to a first order, by the threshold voltage and the field effect mobility. As discussed in Sects. 6.2.3 and 6.2.4, the threshold voltage is determined by the deep state density, and the field effect mobility is determined by the tail state density. Both device parameters are usually extracted from the experimental transfer characteristics, in either the linear or saturation regime, using the simple IGFET Eqs. 3.11 and 3.17, respectively, from

Chap. 3. In particular, the field effect mobility is calculated from the slope of the I_d-V_G or $\sqrt{I_{d(sat)}}$–V_G curves, using Eqs. 3.12 or 3.18, respectively, and the threshold voltage is obtained from the extrapolated intercept of the curve with the V_G axis at $I_d = 0$, as illustrated in Fig. 6.11.

Although these simple equations are used for basic parameter extraction, for more accurate representation of the characteristics in compact circuit modelling packages, such as SPICE, account needs to be taken of detailed aspects of device behaviour including the distribution of carriers in the band tail states, and the finite output impedance using the following expression [15, 27]:

$$I_d = \frac{\mu W C_i^{\alpha-1} \xi}{\alpha L}[(V_G - V_T)^\alpha - (V_G - V_T - V_D)^\alpha][1 + \lambda(V_D - V_{Dsat})] \quad (6.38)$$

.

Where α and ξ are related to the tail state energy width, E_t, and the carrier density trapped in the tail states, N_t, by:

$$\alpha = 2E_t/kT \quad (6.39)$$

$$\xi = \frac{(q\varepsilon_s\varepsilon_0 \alpha kTN_t)^{1-\alpha/2}}{\alpha - 1} \quad (6.40)$$

For the conduction band tail states, when $E_t \sim kT$, then $\alpha \sim 2$ and $\xi \sim 1$, and the first part of Eq. 6.38 reduces to the basic IGFET Eq. 3.10:

$$I_d = \frac{\mu_n W C_i}{L}\left[(V_G - V_T)V_D - 0.5V_D^2\right] \quad (6.41)$$

The final term in Eq. 6.38 contains the channel shortening parameter, λ, which allows for the finite output impedance of the I_d–V_D characteristic in saturation.

A further modification to Eq. 6.38 (and, indeed, to Eqs. 3.10 and 3.26) is required when there is series resistance in the TFT structure [27, 28]. This can arise for several reasons, including contact resistance between the metal source and drain electrodes and the n^+ regions, the limited conductivity of the n^+ regions themselves, the thickness (or bulk resistance) of the a-Si:H film through which carriers flow from the channel to the n^+ regions, and the overlap of the gate and the source/drain contacts [28]. For a fixed ohmic resistance, R_s and R_d, at the source and drain contacts, there will be voltage drops I_dR_s and I_dR_d, respectively, which will change the effective values of the gate-source voltage, V_{GS}, and source-drain voltage, V_{DS}, from the externally applied voltages V_G and V_D, respectively, to:

$$V_{GS} = V_G - I_dR_s \quad (6.42)$$

$$V_{DS} = V_D - I_d(R_s + R_d) \quad (6.43)$$

Hence, V_G and V_D in Eq. 6.38 (and in Eqs. 3.10 and 3.26) need to be replaced by the expressions for V_{GS} and V_{DS}, respectively. However, the series resistance has to be of the same order as the channel resistance for it to have a significant

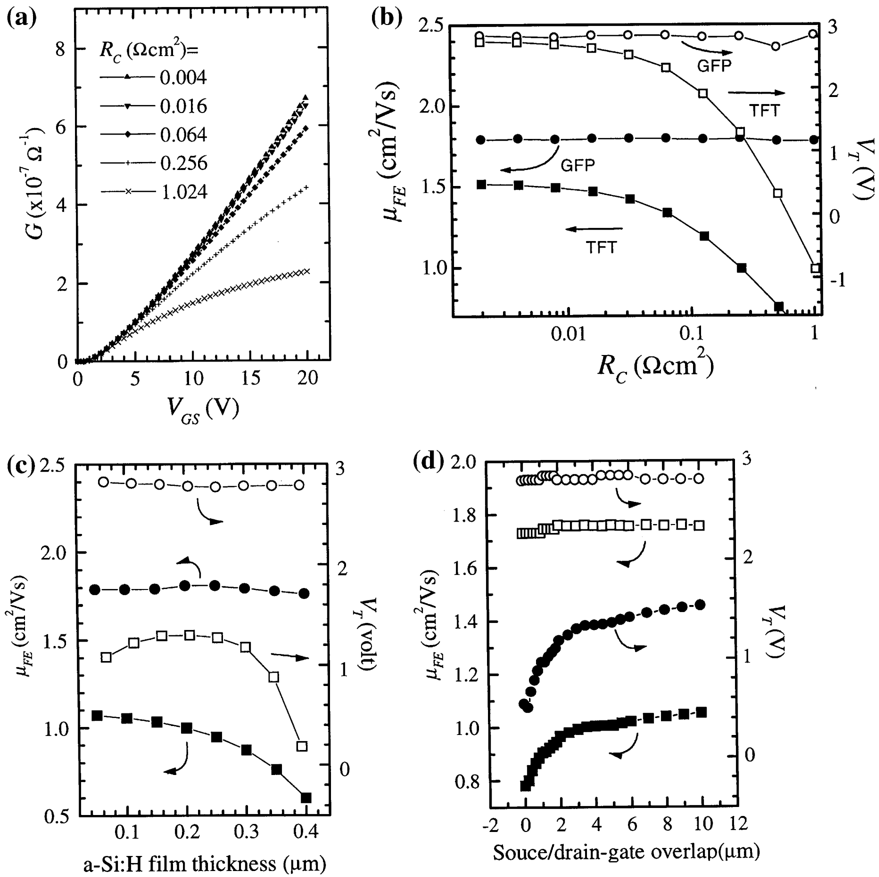


Fig. 6.17 2-D simulations of series resistance effects in BCE and FGP TFTs. **a** The variation of the TFT on-state conductance with specific contact resistance. The effects on the mobility and threshold voltage of **b** the specific contact resistance, **c** the a-Si:H film thickness, and **d** the overlap of the gate and source/drain electrodes. (The square and circular symbols represent the TFT and FGP data, respectively). (Reprinted from [28]. Copyright (1998), with permission from Elsevier)

effect. If the series resistance is non-ohmic, then its effective resistance value will be a function of the potential across it, and the detail of this will depend upon the current flow mechanism. For instance, the current flow through the thickness of the a-Si:H film is a space charge limited current [29], in which $I \propto V^2$.

The calculated effect of the specific contact resistivity is shown in Fig. 6.17a by the normalised channel conductance plots of a conventional BCE TFT [28], where the conductance, G, in the linear regime, can be calculated from Eq. 6.26, using:

$$G = \frac{I_d L}{V_D W} = \mu_n C_i (V_G - V_T) \tag{6.44}$$

With increasing values of the specific contact resistance, the roll-off in G with increasing V_G was due to the reducing channel resistance becoming increasingly comparable to the fixed series resistance.

Similar calculations were made for a modified TFT structure, containing two extra electrodes contacting the channel (labelled as a gated 4-probe, GFP, TFT) [28]. These two electrodes sense the channel potential without drawing any current, and, therefore, were not affected by the contact resistance. The calculated GFP TFT conductance (not shown) was quite different, since, in the absence of series resistance effects, its G curve was independent of the contact resistance and did not roll off with increasing V_G values. Figure 6.17b compares the extracted values of μ_{FE} and V_T for the two TFT architectures, and, as expected, μ_{FE} in the normal TFT architecture fell with increasing contact resistance, as did V_T, whilst those of the GFP TFT remained constant. (The mobility is evaluated at the point of maximum slope of the $I_d - V_G$ curve, and this tangent to the curve is also used to extract V_T, which, to a certain extent, is an artefact of the extraction procedure).

Two-dimensional device simulations were also used to quantify the effects, on the channel conductance, of the film thickness and of the overlap of the gate and the source/drain electrodes [28]. Their impact upon the extracted field effect mobility and threshold voltage are shown in Fig. 6.17c, d, respectively. In the simulations, unless the specified parameter was the variable, the intrinsic (resistance-free) field effect mobility was 1.78 cm^2/Vs, the specific contact resistivity was 0.25 $\Omega\ cm^2$, the gate-source/drain overlap was 3 μm, the a-Si:H film thickness was 200 nm, and its dark resistivity was 3.8×10^{10} Ωcm [28, 30]. These values corresponded to experimental TFT and GFP structures, which displayed characteristics comparable to the simulations [28, 30]. As will be seen in Fig. 6.17, each parameter reduced both the apparent field effect mobility and the threshold voltage. However, the spreading resistance due to the gate-source/drain overlap was not significant for overlaps of 3 μm or more, which is the typical value for conventional a-Si:H TFTs. Equally, the effect of a 200 nm, or thinner, a-Si:H film was marginal compared with much thicker films, while the measured specific contact resistivity of 0.25 $\Omega\ cm^2$ had the largest overall effect.

The contact resistance effects simulated in Fig. 6.17a were for constant resistances, but bad contacts can also give voltage dependent resistance values. These can lead to poor output characteristics, displaying low drain bias *current crowding* effects, as shown in Fig. 6.18a [31]. For comparison, a TFT with a more ideal output characteristic, and no current crowding effects, is shown in Fig. 6.18b [30]. High quality TFTs will not show current crowding effects [21], but, where it does occur, the field effect mobility cannot be meaningfully evaluated in the linear regime, and, for this reason, it is common practice for the mobility to be evaluated in the saturation regime. It should also be noted that current crowding effects are not limited to a-Si:H TFTs, but are observed with other TFT materials as well, and, for the same reason, the saturation regime mobility is also frequently quoted for those devices.

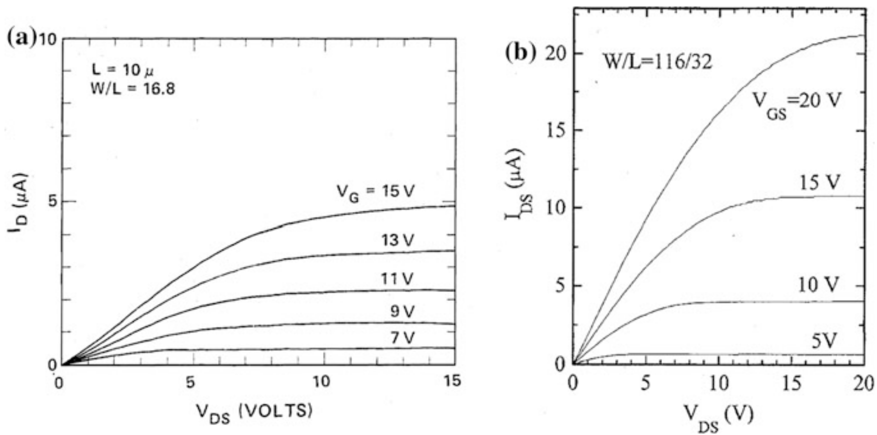


Fig. 6.18 Output characteristics from two different TFTs showing **a** current crowding at low drain bias (Reprinted from [31] with permission of IEEE), and **b** good quality contacts (Reprinted from [30] with permission of IEEE)

6.3.2 *Off-State*

The off-state characteristics of the n-channel a-Si:H TFT define its leakage current behaviour under negative gate bias, and several leakage current mechanisms have been identified. These include leakage through the a-SiN_x:H gate dielectric, bulk conduction through the a-Si:H film itself, back channel electron conduction, and front channel hole conduction [32–34]. The magnitude of the current is a function of the following parameters: the applied gate and drain biases, the a-Si:H film thickness (which will determine its bulk conductance, and the coupling of the gate to the back channel), the gate/drain overlap, and the overall fabrication process, which will determine, among other things, the back-face passivation [32, 35]. An example of an extensively studied set of characteristics is shown in Fig. 6.19a, b, which were taken from an etch-stop TFT, with 50 and 250 nm thick a-Si:H and a-SiN_x:H layers, respectively [33]. Two of the significant negative gate bias features of these curves are the exponential increase in current with gate and drain bias at large negative gate bias, and the change from inverse channel length dependence to channel length independence with increasing negative gate bias. This latter change highlights a difference in the leakage current mechanism, where the channel length independence is indicative of a current limited by generation processes at the drain terminal, whereas the channel length dependence is more consistent with an ohmic-like current flow.

Of the four leakage current processes listed above, the bulk leakage through the a-Si:H and a-SiN_x:H layers are the limiting minimum currents [33], and, in practical devices, the processes of back channel electron conduction and front channel hole conduction were found to dominate [34]. The back channel conduction is due to a weak electron accumulation layer at the back interface, and is

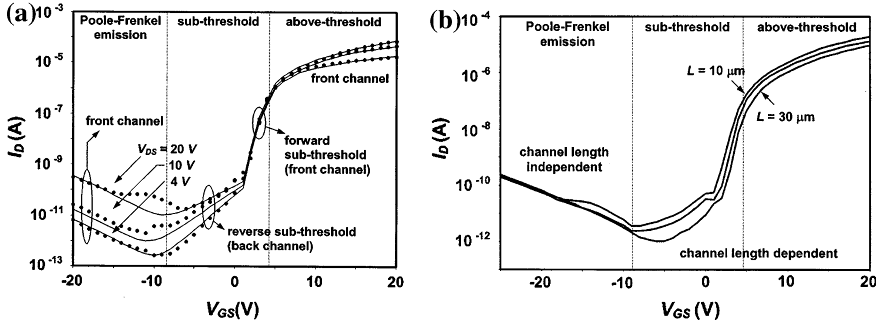


Fig. 6.19 Experimental TFT transfer characteristics, showing the leakage current as a function of (**a**) drain bias (W = 50 µm, L = 20 µm; the *solid line* is a simulation), and (**b**) channel length. (Reprinted from [33] with permission of IEEE)

determined by the top passivation layer. This can be depleted by the front gate, if the a-Si:H layer is thin enough to permit front gate/back channel coupling. This mechanism is shown by the fitted curve to the experimental data in the reverse sub-threshold regime in Fig. 6.19a. The reverse sub-threshold slope in this region is a function of both the deep trap density at the back of the film [33], and the strength of the gate coupling, which is diminished by the electrostatic screening of a hole accumulation layer at the front interface [34]. Hence, the depletion of the back channel current is strongest in thinner films [32]. This mechanism dominates at low negative gate voltages.

At large negative gate voltages, a hole accumulation layer is formed at the front interface, which can support hole current flow, but, given the non-hole-injecting nature of the n^+ contacts, it is limited by the internal hole generation rate. Holes are thermally generated from the deep traps in a-Si:H by sequential electron-hole emission, and, in the presence of large gate and drain biases, this process can be enhanced by the Poole–Frenkel effect [32–34], which lowers the emission barrier (E_T) for carrier generation by ΔE_T. This field-enhanced emission process takes place in the high field region of the device in the vicinity of the gate/drain overlap, where the Poole–Frenkel generation rate, $e_{PF}(F)$, is given by [36]:

$$e_{PF}(F) = e_0 \exp(\Delta E_T/kT) \tag{6.45}$$

e_0 is the field-free thermal generation rate (see Sect. 2.3.1 and Eqs. 2.54 and 2.55 for further details), and:

$$\Delta E_T = \sqrt{(qF/\pi\varepsilon_s\varepsilon_0)} \tag{6.46}$$

In this process, the generated electrons are swept into the drain, and the holes flow to the front interface, where they accumulate as a steady state hole accumulation layer. This transports the hole generation current, which flows from the drain area and is injected into the forward biased source junction. From Eqs. 6.45 and 6.46, the carrier generation rate increases exponentially with the square root of

the field, F, and this model provided a good fit to the large negative gate bias data in Fig. 6.19a, where the leakage current rose exponentially with gate and drain bias.

In many respects, this process is similar to the field enhanced leakage currents observed in poly-Si TFTs [33], with one notable difference being the coplanar architecture of the latter giving stronger 2-D coupling of the gate and drain fields. Further details on the basic electron and hole generation processes can be found in Sect. 2.3, and the application of this process to TFT off-state currents is described more fully in Sect. 8.4, together with a broader discussion of the field enhancement mechanisms in Sect. 8.5.3.

6.4 Bias-Stress Instability

6.4.1 Gate Bias

The major instability in a-Si:H TFTs is a shift in threshold voltage after the application of a gate bias stress, V_{Gst}, and this has been extensively studied over many years. Two principle instability mechanisms have been identified, which are carrier trapping in the a-SiN_x:H gate dielectric, and dangling bond formation in the a-Si:H itself. These two effects were distinguished in ambipolar [26, 37] and optically illuminated n-channel [38] a-Si:H TFTs, in which the effects of gate bias could be observed in both the electron and hole conduction branches of the same TFT. For carrier trapping in the gate dielectric, both characteristics were expected to shift in the same direction (e.g., in a positive direction for positive gate bias giving electron trapping), and in opposite directions for amphoteric deep state creation, in which electron filling of the acceptor (0/−) level would increase the n-channel TFT threshold voltage, and hole filling of the donor (0/+) level would increase the p-channel threshold voltage. These effects were seen in the ambipolar TFT measurements shown in Fig. 6.20a, b [21], in which low and high gate bias stresses, of +25 and +55 V, caused the characteristics to either move apart or to both shift in the same direction, respectively. Hence, the low positive bias stress caused deep state formation, but which was overwhelmed by the effects of electron injection into the a-SiN_x:H at large gate biases.

With negative bias stress of −25 V, positive charge injection dominated, although there was also some defect formation in the a-Si:H, but less than under positive bias stress [26, 37].

The positive stress bias, at which carrier injection starts to dominate, is determined by the quality of the a-SiN_x:H layer, and this is a function of the deposition conditions, including the SiH_4/NH_3 gas ratio [39]. The quality of the a-SiN_x:H layer has been correlated with the value of its optical band gap, and the greater the band gap, the higher was the threshold for the onset of the trapping instability, with a field of ~2MV/cm required for injection into the best quality

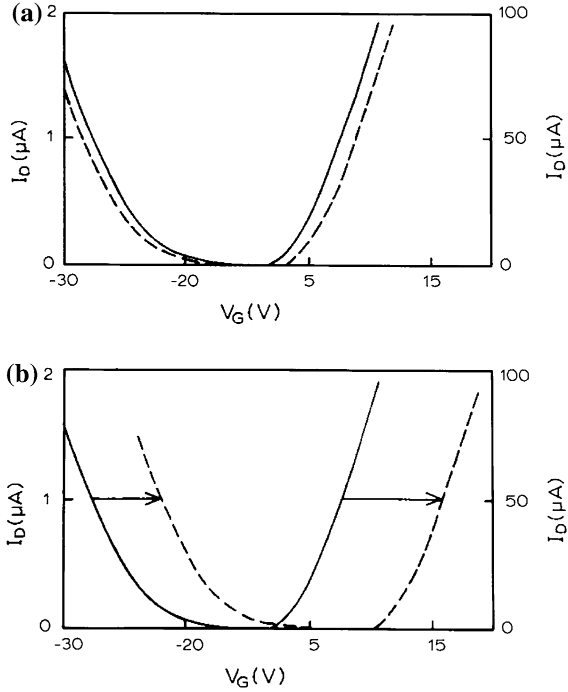


Fig. 6.20 The effect of gate bias stress (*broken lines*) on the transfer characteristics of ambipolar TFTs: **a** +25 V stress for 4 h, and **b** +55 V stress for 10^3 s. (Reprinted from [21], with permission of IEEE)

nitride layers with a 5.0 eV band gap [39]. In contrast, differently prepared samples showed a mixture of both instabilities under all positive bias stress conditions [37]. Hence, depending upon the fabrication procedures, the resulting devices may display varying relative amounts of carrier injection into the nitride and trap generation in the a-Si:H, under a given set of bias conditions [26, 37].

In addition to the different stress voltage dependence of the two instability mechanisms, there was also a different time dependence, as shown in Fig. 6.21a [21]. In this plot, the bias stress at 100 V caused the carrier injection instability to dominate, and the change in threshold voltage, ΔV_T, had an approximately logarithmic time dependence, given by [40]:

$$\Delta V_T(t) = A\log(1 + t/t_0) \tag{6.47}$$

where $\Delta V_T(t) = V_T(t) - V_{T0}$ ($V_{T0} = V_T$ at $t = 0$), A is a constant, and t_0 is a characteristic time. The logarithmic time dependence of this instability has been explained by the exponential dependence of the tunnelling injection current on the injecting field, and the field decreases with carrier trapping due to the screening effect of the trapped carriers [40]. The injection instability also had very weak temperature dependence [40].

The instability caused by the 25 V bias stress, shown in Fig. 6. 21b on a log–log plot, was due to deep state creation in the a-Si:H, and has been described by a power law [40]:

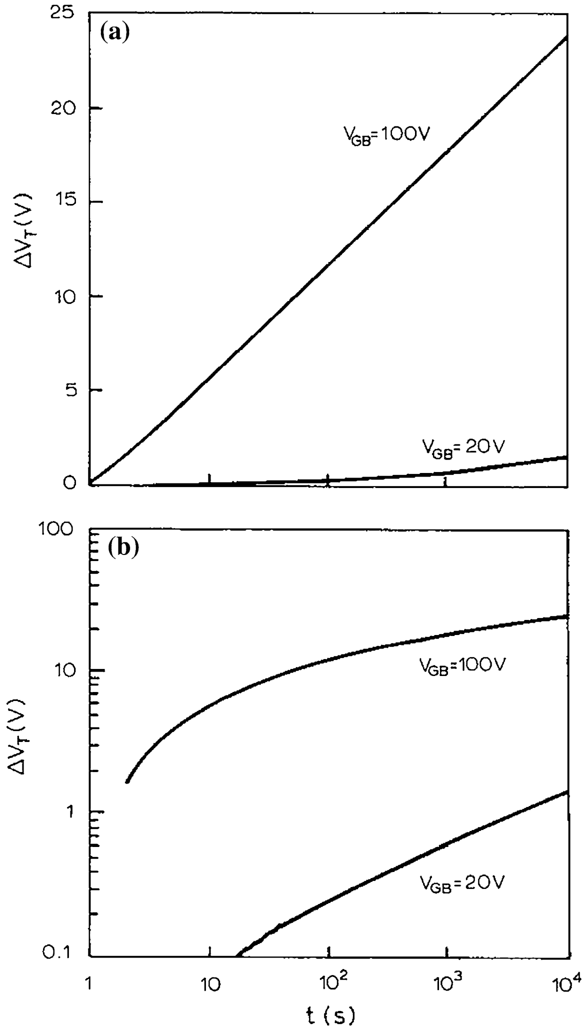


Fig. 6.21 Time dependence of gate bias stress instability (**a**) log-linear plot, and (**b**) log–log plot. (Reprinted from [21], with permission of IEEE)

$$\Delta V_T(t) = \Delta V_T(\infty)(t/\tau)^{\beta} \quad (6.48)$$

Other authors have empirically fitted the change in threshold voltage (due to deep state generation) with a stretched exponential [38], which has been widely used, and, in some cases, fitted to all the instability results [37, 41], where:

$$\Delta V_T(t) = \Delta V_T(\infty)\left[1 - \exp - (t/\tau)^{\beta}\right] \quad (6.49)$$

in which $\Delta V_T(\infty) = V_{Gst} - V_{T0}$ [37, 40–42], β is weakly temperature dependent, and the characteristic defect formation time constant, τ, is given by:

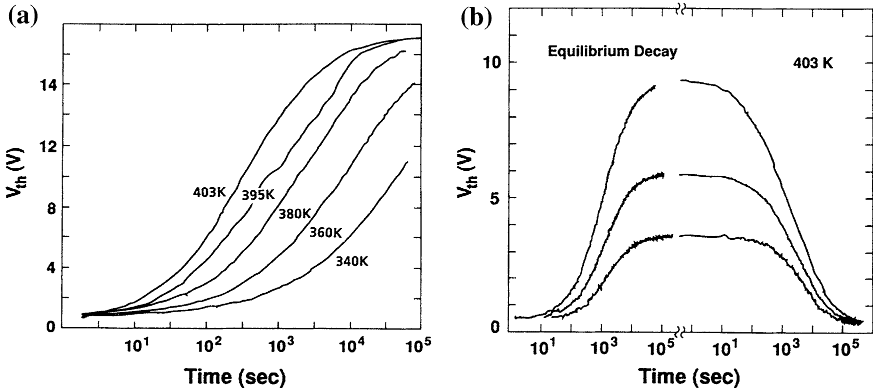


Fig. 6.22 Time dependent threshold voltage as a function of: **a** bias temperature for $V_G = +20$ V, and **b** different gate bias stress values at 403 K (on the *left* hand side), and relaxation data, at $V_G = 0$ V, after gate bias stressing (on the *right* hand side). (Reprinted with permission from [43] Copyright (1990) by the American Physical Society)

$$\tau = \tau_0 \exp(E_A/kT) \tag{6.50}$$

For times short compared with τ, Eq. 6.49 reduces to the power dependent form given by Eq. 6.48 [37, 40].

Equations 6.49 and 6.50 describe a process which is thermally activated, and which saturates after several time constants with a threshold voltage shift of $\Delta V_t(\infty)$. These features are displayed in the time dependent threshold voltage data in Fig. 6.22a [43], in which the samples were stressed at $V_{Gst} = 20$ V at different temperatures. Figure 6.22b shows the dependence of the threshold voltage shift on the stress bias, V_{Gst}, and also demonstrates that the shift could be annealed back to zero after bias removal, if the sample was held for long enough at the stressing temperature.

The features in Fig. 6.22 are similar to the effects discussed in Sects. 6.2.1 and 6.2.5, on defect generation and equilibration in a-Si:H, and these non-injection effects of gate bias stress are similarly interpreted in terms of hydrogen-mediated weak bond breaking and dangling bond formation. The driving force for bond breaking is the increased carrier density in the band-tail states, and the associated movement of the Fermi level towards the band edges by the gate bias, which induces a re-equilibration process in the material. The effects have been interpreted in terms of specific defect reaction kinetics, using the defect pool concepts [42], to replace the empirical stretched exponential fit with a more fundamental model. In particular, the model needed to account for the poor stretched exponential fit for $t > \tau$ [38, 44], and also to incorporate the power dependence of ΔV_T on $V_{Gst}-V_{T0}$ [37, 42], which is shown in Fig. 6.23a [42]. By accounting for the forward and backward defect formation and annihilation rates, and the dependence of the formation energy of charged defects on the Fermi level position, as shown in Fig. 6.23b, a defect reaction model was established which fitted the data better

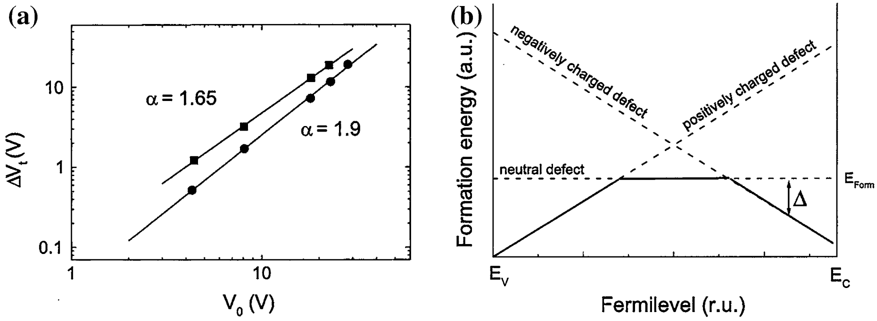


Fig. 6.23 **a** Intermediate time (t = 1000 s) threshold voltage shift as a function of stress bias, V_0 ($V_0 = V_{Gst} - V_{T0}$), for constant current stressing of low and high mobility TFTs, and **b** charged defect formation energy as a function of the Fermi level position. (Reprinted with permission from [42] Copyright (2003) American Institute of Physics)

than the stretched exponential [42]. It also yielded a value of $\alpha = 1.5$, in agreement with the power dependence of ΔV_T shown in Fig. 6.23a [42]. Whilst these results were derived from the numerical solution of the reaction rate equations, the solution for $\alpha = 1.5$ was well approximated to by a stretched hyperbola of the form [5, 44]:

$$\Delta V_T(t) \propto \left\{1 - \left[(t/\tau)^{\beta} + 1\right]^{-2}\right\} \tag{6.51}$$

In common with the stretched exponential, the above expression accounts for the fact that the defect formation rate cannot be represented by a single reaction time constant, and this is interpreted as being due to the presence of a range of reaction barrier heights, rather than the single one shown in Fig. 6.4a. For quantitative evaluation of defect formation rates between different samples and stress temperatures, it was useful to replace t in Eq. 6.51 with a thermalisation energy [42, 44, 45], E_{th}. This is the reaction barrier height below which all defects will be formed in a time t, where the relationship between t and E_{th} is given by:

$$E_{th} = kT\ln(\nu t) \tag{6.52}$$

ν is the attempt to escape frequency, which was found by curve fitting to be 10^9 Hz for defect creation [45]. For a mean barrier height E_A, and a barrier height distribution width of kT_0, the stretched hyperbola is reformulated as [45]:

$$\Delta V_T(E_{th}) = (V_{Gst} - V_{T0})\left\{1 - \left[\exp\left(\frac{E_{th} - E_A}{kT_0}\right) + 1\right]^{-2}\right\} \tag{6.53}$$

Depending upon the deposition conditions, E_A was found to be 0.93–0.98 eV and kT_0 was 54–69 meV for defect creation, whereas, for the defect annihilation, ν was calculated to be 5.7×10^{13} Hz for the Si–H bond stretching mode, E_A was ~1.55 eV and kT_0 was ~41 meV [45]. The defect creation results have been

interpreted in terms of the breaking of a weak Si bond in the vicinity of a doubly hydrogenated centre, which triggered a rearrangement of the hydrogen atoms to give two nearby defect complexes, both consisting of a dangling bond adjacent to a hydrogenated bond [45]:

$$\mathrm{Si{-}Si} + \mathrm{SiHHSi} \rightarrow 2\mathrm{SiD} + \mathrm{SiHHSi} \rightarrow 2\mathrm{SiHD} \tag{6.54}$$

The larger value of E_A for defect removal (when v is taken to be the Si–H bond vibration frequency) is similar to the activation energy for hydrogen diffusion, suggesting that defect annihilation is limited by the release and movement of hydrogen to a dangling bond site [45].

6.4.2 *Pulsed Bias Stress*

The discussion above focussed on DC gate bias stress instability, but, in active matrix displays, the pixel TFT experiences a low duty cycle of positive gate bias during the row on-time, followed by a longer period of negative gate bias for the rest of the frame time. Hence, a pixel TFT experiences alternating positive and negative pulsed gate bias stress, but with quite different duty cycles, and it has been demonstrated that the effects of negative pulsed bias stress are quantitatively different from DC gate bias stress [37]. Figure 6.24 compares the threshold voltage shift for the DC and pulsed bias stress conditions, for both stress polarities, as a function of the integrated time during which the pulsed stress was applied. For positive pulse bias stress, ΔV_T was slightly smaller than DC stress, and this was attributed to partial relaxation of the deep trap density during the pulse off period. Hence, by taking into account the pulse bias duty cycle, the DC and pulsed results were very similar. For negative pulse bias stress, there was a strong pulse width dependence, in which ΔV_T decreased with reduced pulse width. This was attributed to the instability process being driven by the hole density in the channel, and, due to the n^+ source and drain contacts, there was not a ready supply of holes. In other words, the hole density could not respond rapidly to the changes in negative gate bias, but was limited by the supply process for the holes. The experimental dependence of ΔV_T on the pulse width was empirically modelled by an RC circuit, in which the ‘resistance’ element of the time constant represented the supply of holes to charge the gate dielectric capacitor at the a-Si:H/a-SiN_x:H interface [37].

Due to the difference between the DC and pulsed stressing, it was demonstrated that, in order to estimate the projected lifetime of an AMLCD, the calculation needed to be based upon the pulsed bias instability results rather than the DC results, and that the summation of the separate positive and negative pulse bias stress results accurately reflected an alternating positive/negative pulse bias stress. Hence, the net effect of alternating stress, $\Delta V_T^{\pm}$, could be calculated from [37]:

$$\Delta V_T^{\pm}(t) = \Delta V_T^{+}(t) + \Delta V_T^{-}(t) \tag{6.55}$$

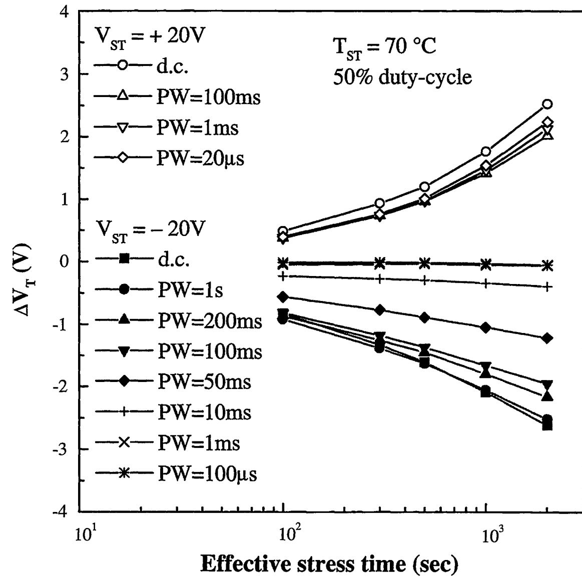


Fig. 6.24 Comparison of threshold voltage instability due to DC and pulsed bias stressing. (Reprinted with permission from [37]. Copyright (1998) The Japan Society of Applied Physics)

and,

$$\Delta V_T^+(t) = A\left(V_G^+ - V_{T0}\right)^{\alpha+}(tT_{on}/T_{fr})^{\beta+} \tag{6.56}$$

$$\Delta V_T^-(t) = B\left(V_{T0} - V_G^-\right)^{\alpha-}(t\{1 - T_{on}/T_{fr}\})^{\beta-}F_{PW} \tag{6.57}$$

Where Eqs. 6.56 and 6.57 are based upon the power law Eq. 6.48 (which is an acceptable approximation for ΔV_T values far from saturation), and they also include the power dependence of the bias conditions (the first term) to reflect the experimental data shown in Fig. 6.23a. The parameters A, B, α and β were empirically fitted constants to the DC bias results, the effects of which were modified by the duty cycle, given by the ratio of the row on-time, T_{on}, to the frame time, T_{fr}, and F_{PW} was a further weighting factor (determined from the RC charging model), to represent the specific pulse width dependence of the negative bias pulse instability. These equations were shown to approximate well to experimental alternating pulse data, and were used to predict the long term ΔV_T values for a pixel TFT in an SXGA AMLCD. This is shown in Fig. 6.25, and indicates that, for a maximum tolerable threshold voltage shift of 3 V, the display would have an acceptable operating life of ~10 years at 70 °C [37]. The initial, negative values of ΔV_T were due to the longer duty cycle of the negative gate bias, but, eventually, the stronger cumulative effect of the positive bias stress dominated the overall shift. This was due to the larger value of $\beta+$ compared with $\beta-$ in Eqs. 6.56 and 6.57 [37].

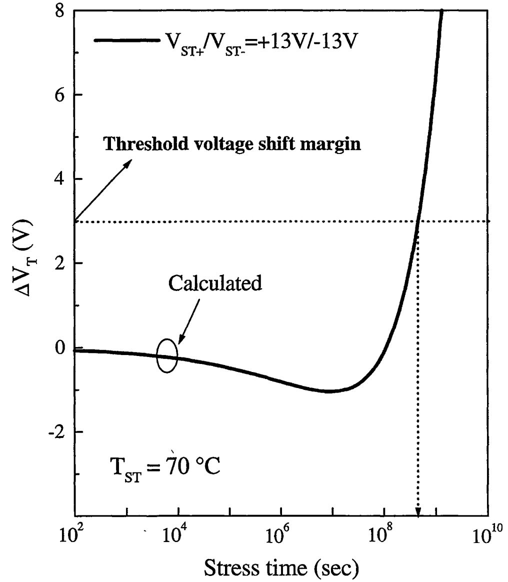


Fig. 6.25 Predicted pixel TFT lifetime in an SXGA AMLCD. (Reprinted with permission from [37]. Copyright (1998) The Japan Society of Applied Physics)

6.4.3 Gate and Drain Bias Stress Effects

In early work studying the combined effects of gate and drain bias stress [46], very little influence of the drain bias (or the level of channel current) was seen on the threshold voltage instability, which was determined mainly by the magnitude of the gate bias. In subsequent work, in both the low (<15 V) [47] and higher gate bias (≥20 V) regimes [48], where the dominant instability processes were defect state generation in the a-Si:H and charge injection into the a-SiN_x:H, respectively, a drain bias dependence was demonstrated, which, at most, had the effect of reducing the normal gate bias instability. This is shown in Fig. 6.26a, for various combinations of gate-source bias, V_{GS}, and source-drain bias, V_{DS}, in which, at constant $V_{GS} = 15$ V, the largest values of ΔV_T occurred for $V_{DS} = 0$ V, and the smallest values for $V_{DS} = 15$ and 30 V [47]. The latter results indicate that the ameliorating effect of the drain bias saturated at the drain saturation voltage. For defect formation in the a-Si:H, which is driven by the gate induced electron concentration in the band-tail states, the results were interpreted in terms of the average charge density, Q_G, in the channel. In the linear regime at low V_{DS}, this is given by:

$$Q_{G0} = C_i WL(V_{GS} - V_T) \qquad (6.58)$$

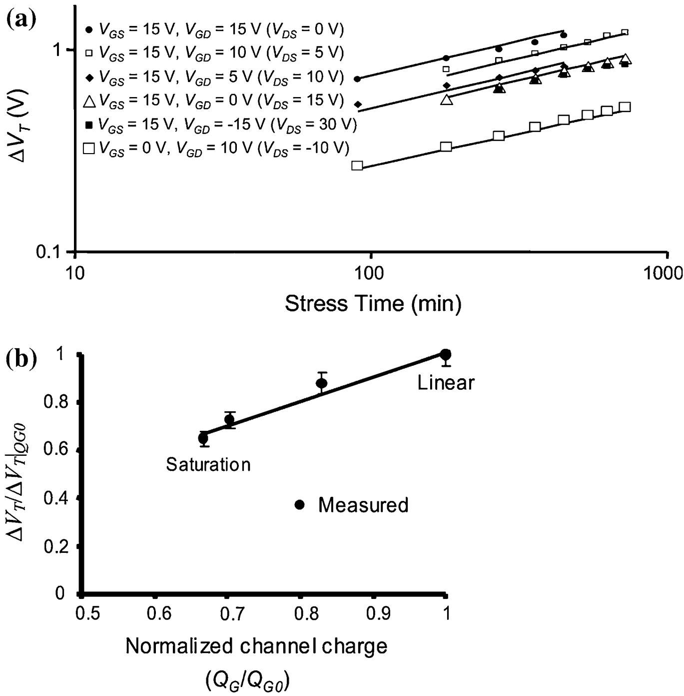


Fig. 6.26 **a** Threshold voltage instability measured after different gate and drain bias stress combinations (*solid lines* modeled using Eq. 6.60), and **b** measured and modeled normalized threshold voltage shift as a function of normalized channel charge. (Reprinted from [47] with permission of IEEE)

However, when V_{GS} and V_{DS} are of the same order (and $V_{GD} = V_{GS}-V_{DS}$), the gate and channel charge are given by [47]:

$$Q_G = \frac{2}{3} C_i WL \frac{(V_{GS} - V_T)^3 - (V_{GD} - V_T)^3}{(V_{GS} - V_T)^2 - (V_{GD} - V_T)^2} \tag{6.59}$$

For small V_{DS}, Eq. 6.59 tends towards 6.58, and, for $V_{GD} \sim V_T$ (i.e.$V_{DS} \sim V_{GS}-V_T$) Eq. 6.59 tends towards $2/3Q_{G0}$. From the power law Eq. 6.48, together with Eqs. 6.58 and 6.59, ΔV_T can be represented by the normalised channel charge [47]:

$$\Delta V_T(t) = (Q_G/Q_{G0})A(V_{GS} - V_{T0})t^{\beta} \tag{6.60}$$

Using Eq. 6.60, the threshold voltage shift, normalised to the maximum shift at $V_{DS} = 0$, is plotted against the normalised channel charge in Fig. 6.26b, and the solid lines in Fig. 6.26a were also calculated using Eq. 6.60 [47]. Similar arguments, in terms of the reduced gate field at the drain, were also used for the

reduction in carrier injection into the gate dielectric under combined gate and drain bias stress [48].

6.5 Other Meta-Stability Effects

Meta-stable defect formation induced by gate bias stressing and film doping were discussed in Sects. 6.4 and 5.5.2, respectively, and a further situation, under which there is meta-stable defect production, is when a-Si:H is exposed to high, absorbed light intensities for prolonged periods of time. This is known as the Staebler–Wronski effect [49], and was first observed as a reduction in the photoconductivity and dark conductivity of illuminated material. This was attributed to an increased recombination centre density, and is a major degradation mechanism in a-Si:H solar cells. It reduces the carrier recombination lifetime, and hence the cell's quantum efficiency. Although this is less of an issue for TFTs, for completeness, a brief overview of this effect is presented below.

6.5.1 Staebler Wronski Effect

The Staebler–Wronski effect has been extensively studied for many years [49–53], and one outcome of this has been the recognition that there are a number of light induced defect generation processes. These depend upon the illumination temperature, the growth procedure, and the quality, hydrogen content and doping content of the material [50, 51, 53]. In view of this, there is still discussion over the detailed mechanisms and processes [53], and the over-view in this section is restricted to defect generation in undoped a-Si:H near room temperature, which illustrates the essential features of the classical Staebler–Wronski effect.

Figure 6.27a shows the change in concentration, with illumination time and intensity at 310 K, of the a-Si:H $g = 2.0055$ paramagnetic centre defect, which has been associated with the neutral Si dangling bond [52]. The photon energy was 1.9 eV, although, after normalising for the carrier generation rates at different photon energies (determined by the optical absorption coefficients and the incident photon flux), similar defect generation rates were seen over the energy range 1.2–2.1 eV [52]. The density increased with time, and, for the longer times, increased with a power time dependence of $t^{1/3}$, whilst the insert shows that the dependence on the illumination intensity, I, was $I^{0.6}$. The process was also very weakly temperature dependent, with an activation energy of 0.04 eV. The absence of a linear dependence on time and intensity showed that the defect generation process was not simply cumulative with illumination time due to direct photo-dissociation. The data was interpreted as a self-limiting defect generation process, in which dangling bonds were formed by non-radiative recombination of the photo-generated electron-hole pairs.

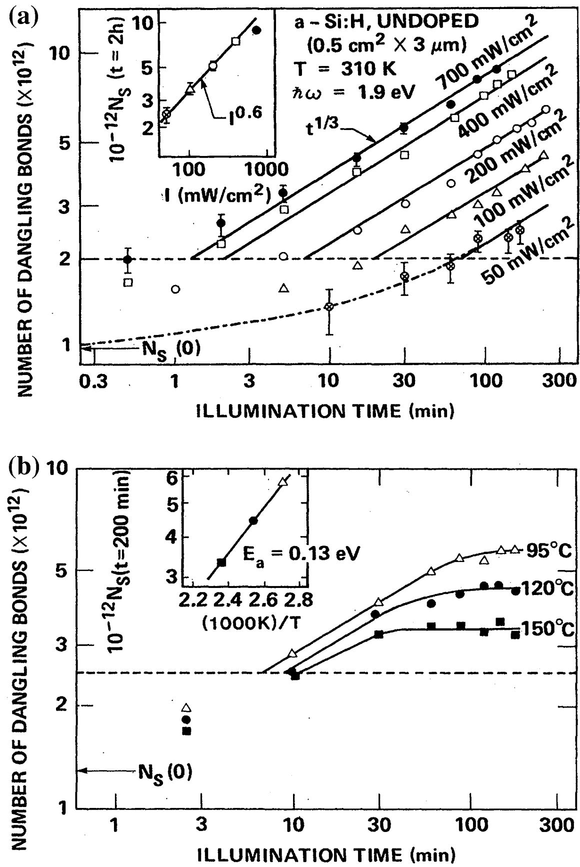


Fig. 6.27 Time dependent defect generation due to optical illumination at (**a**) 310 K, and (**b**) above 90 °C. (Reprinted with permission from [52]. Copyright (1985) by the American Physical Society)

For photon energies above band-gap, the photo-generated electrons and holes were assumed to rapidly thermalise from extended states to shallow band-tail states before recombining. (This is consistent with photo-luminescence studies, where the emitted photon energy was ~1.2–1.3 eV, and was independent of the energy of the stimulating photons [52]). For sub-band gap illumination over the energy range down to 1.2 eV, the carrier excitation was directly from the valence band-tail states, as in the Urbach edge measurement discussed in Sect. 6.2.1. However, in all cases, the recombination event leading to defect generation was assumed to be non-radiative between band-tail states. The dangling bond creation energy was ~1 eV, and, at photon energies greater than ~1.2 eV, the subsequent non-radiative carrier recombination released sufficient phonon energy back to the lattice to break weak silicon bonds, and form dangling bonds. Once near mid-gap states, such as the neutral dangling bond, have been created, non-radiative recombination can proceed through them by sequential electron and hole capture. The phonon energy released after each carrier capture stage is less than half band gap energy, and is insufficient to break more weak Si–Si bonds. Hence, the

increasing concentration of dangling bonds provided an increasing number of alternative, two-stage recombination paths, and this reduced the rate of dangling bond generation by the direct band-tail to band-tail recombination [52]. This model contained the essential features of the experimental data, where, in a simplified version, the defect generation rate is proportional to the recombining free carrier concentrations, and is given by:

$$dN_{DB}/dt = Anp \quad (6.61)$$

where N_{DB} is the DB concentration, A is a constant, and n and p are the steady state electron and hole concentrations produced by the illumination, and are given by:

$$n = G/BN_{DB} \text{ and } p = G/CN_{DB} \quad (6.62)$$

The electron-hole pair generation rate, G, is proportional to the illumination intensity, and the denominators are the inverse of recombination lifetime-like factors, which are proportional to the number of dangling bond recombination centres (see Chap. 2 for a fuller discussion of the electron-hole pair generation and recombination processes). Substitution of Eq. 6.62 into 6.61, and the integration of this equation gives [52]:

$$N_{DB}^3 - N_{DB0}^3 = 3(A/BC)G^2t \quad (6.63)$$

When $N_{DB}(t)$ is more than twice the initial concentration, N_{DB0}, the latter term can be ignored, and Eq. 6.63 reduces to:

$$N_{DB} = \{3(A/BC)\}^{1/3}G^{2/3}t^{1/3} \quad (6.64)$$

Equation 6.64 shows the same dangling bond density dependence on I and t as displayed in Fig. 6.27a. For temperatures above 90 °C, the defect density deviated from the $t^{1/3}$ dependence, and saturated with the temperature dependent density shown in Fig. 6.27b [52]. Some authors have fitted the saturating curve with a stretched exponential time dependence [51]. As with the defects formed during gate bias stress, the light induced defect concentration could be reduced back to its original value by annealing at elevated temperatures, with a distribution of activation energies between 0.9 and 1.3 eV [52]. The temperature dependence of the equilibrium densities, in the insert in Fig. 6.27b, has been attributed to the balance between defect production and the increased annealing rates at higher temperatures [51].

The defect generation and annealing features of optically stressed samples share many qualitative similarities with other metastable defect generation processes in a-Si:H, and all are thought to involve a hydrogen-mediated weak bond breaking process. This brief overview of the Staebler–Wronski effect has concentrated on defect production in intrinsic material near room temperature, and a contemporary review of further features of this effect can be found in Ref. [53].

6.6 Summary

As the dominant addressing device in active matrix flat panel displays, a-Si:H TFTs have been extensively studied, and many of their properties linked to the defect structure of the basic material. In particular, the electronic properties of a-Si:H are strongly influenced by the defect states distributed across the mobility gap. These consist of band-tail states due to weak Si–Si bonds in the disordered Si network, and dangling bonds, DBs, arising from three-fold coordinated Si atoms. The presence of high concentrations of hydrogen (~ 10 %) in the material reduce the DB density to $\sim 10^{16}$ cm^{-3}. However, the defect density is frozen-in at ~ 500 K, during the cooling of the material from its growth temperature, and the density will tend to relax to a new value in response to changes in external stimuli, such as prolonged exposure to temperatures above room temperature, increases in carrier concentration, and exposure to optical illumination.

The electronic defect state density is described by the density of states, DOS, distribution, and the inter-relationship between the surface potential and the resulting surface space charge density was treated in a semi-analytical fashion, by using an exponential approximation to the DOS. This permitted a direct comparison with defect free c-Si, and highlighted the role of the band tail states in continuously partitioning the induced charge density between free and trapped electrons, and giving an electron field effect mobility more than ten times smaller than the band mobility. The other contributor to the space charge density was the DBs, which determined the TFT threshold voltage.

The position of the DB energy level within the mobility gap is determined by its charge occupancy during the growth of the material, and the large positive charge density in the a-SiN_x:H gate dielectric layer causes the DB distribution to be formed in the lower half of the band gap. This minimises its impact upon the sub-threshold slope of n-channel TFTs, and illustrates why a-SiN_x:H is the preferred gate dielectric for n-channel TFTs; conversely, because of this DB location, it also gives rise to poor p-channel TFT performance.

The other factors controlling the on-state characteristics, apart from the field effect mobility and threshold voltage, are series resistance effects due to contact resistance, the a-Si:H film thickness, and the spreading resistance associated with the overlap of the gate electrode and the source and drain contacts. For conventional TFT geometries, with a-Si:H film thicknesses less than 200 nm and G-S,D overlaps of ~ 3 µm, 2-D device simulations showed that the typical specific contact resistance of 0.25 Ω cm^2 was the major cause of series resistance effects.

Contributory factors to the TFT leakage current characteristics are bulk conduction through both the a-Si:H and the a-SiN_x:H layers, electron conduction at the back interface and hole conduction at the front interface. For practical TFTs, the latter two effects dominate, and, at large drain and large negative gate biases, field-enhanced electron-hole pair generation rates give exponentially increasing leakage currents supported by front interface hole conduction.

Gate bias stressing leads to long-term threshold voltage instability in TFTs, due to carrier trapping in the a-SiN_x:H dielectric and DB formation in the a-Si:H layer. The trapping instability usually dominates with both negative gate bias stress and with large positive gate bias stress, whilst DB formation is more significant with smaller positive gate biases. However, the balance between the two is determined by the quality of the a-SiN_x:H layer, and other device processing features. The DB formation is another aspect of the meta-stability of the a-Si:H defect structure, and is driven by the increased free carrier concentration in the band tail states. Considerable attention has been given to understanding the bias, time and temperature dependence of this effect, and it has been similarly attributed to hydrogen-mediated weak bond breaking. In clarifying the instability mechanisms, most attention has been given to DC gate bias stressing, but, to extend those results to TFT operation in AMFPDs, the study of pulsed bias stressing has demonstrated that the negative gate bias instability is very pulse width dependent. This is due to the slow generation rate of holes in n-channel TFTs. By modifying the DC results to account for the duty cycle and for pulse width dependences, the effects of active matrix drive conditions on the TFT stability were well modelled. Combined gate and drain bias were shown to reduce the magnitude of the gate bias instability, particularly in saturation, due to the reduction in free carrier density and vertical field along the channel. Finally, a brief overview of defect instability under optical illumination, known as the Staebler–Wronski effect, was presented.

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Chapter 7
Poly-Si TFT Technology and Architecture

Abstract This chapter discusses the fabrication of high quality poly-Si films, by the industry standard technique of excimer laser crystallisation of a-Si:H precursor films. Alternative crystallisation procedures are also reviewed, including metal-induced solid phase crystallisation, as well as advanced procedures for achieving large grain and high mobility TFTs, using green solid-state lasers in addition to modified excimer laser techniques. The architecture of poly-Si TFTs is top-gated with a silicon dioxide gate dielectric, and issues with the implementation of self-aligned and non-self-aligned architectures are discussed, and illustrative processing schedules are listed. Finally, a simple qualitative cost model is presented, illustrating why the major commercial application of poly-Si TFTs is in the small-diagonal, portable display market.

7.1 Introduction

The interest in poly-Si, as an alternative TFT material, started soon after a-Si:H TFTs became recognised as the most promising technology for the large scale production of AMLCDs. The low carrier mobility of a-Si:H TFTs (<1 cm^2/Vs) is perfectly adequate for the addressing TFTs within each pixel, but is inadequate for the faster switching circuits needed for addressing the rows and columns in the display itself. In contrast to the carrier mobility in a-Si:H, which has remained within the range 0.5–1.0 cm^2/Vs over the last 20 years or so, the electron mobility in poly-Si has increased, over the same period, from <5 to $\sim$120 cm^2/Vs with routine processing, and up to $\sim$900 cm^2/Vs with innovative techniques yielding quasi-single-crystal large-grain material [1]. The higher carrier mobility offered by the more crystallographically-ordered polycrystalline silicon was seen as leading to a second generation AMLCD technology, with addressing circuitry and other circuit functions integrated onto the AMLCD plate. Whilst this has been achieved, and

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highly integrated poly-Si displays [2, 3] are now in mass production for small/medium diagonal, portable active matrix flat panel displays, AMFPDs, a-Si:H remains the dominant AMLCD technology, particularly for the larger sized notebook, monitor and TV displays. Hence, the current application of poly-Si is directed towards small/medium diagonal displays, where it accounts for $\sim$36 % of that segment of the AMLCD market [4]. In addition, it has virtually 100 % of the rapidly growing small diagonal AMOLED market, particularly for smart phones [5].

The study of poly-crystalline silicon, as a semiconductor device material, has a long history, and predates the present interest in the low temperature fabrication of TFTs on glass or flexible substrates. Traditionally, its major application has been as a heavily doped layer for the gate electrode in MOSFETs [6], because, as a refractory material, it can withstand high temperature integrated circuit processing. As MOSFET circuit speeds increased, its conductivity was enhanced by combining it with a refractory metal to form a low resistivity metal-silicide. In addition to this, poly-Si resistors have also been used in VLSI circuits [7], leading to detailed studies of conduction in the material [8]. Finally, in the mid-1980s poly-Si TFTs on quartz substrates were fabricated, using a high temperature VLSI-like process, for use in projection AMLCDs [9]. Much of this work formed a useful background to the research and development of low temperature poly-Si TFTs on glass, which is the subject of this chapter and of Chap. 8. A particular example of this information infrastructure is the analytical model of conduction in polycrystalline silicon [8], which is still used to provide a simple numerical and pictorial description of carrier flow over grain boundaries. More sophisticated treatments have now been adopted, but, in view of the continued use of this model, it will be presented in Chap. 8, together with its analytical extension to carrier flow over grain boundaries in TFTs [10].

As mentioned above, highly integrated poly-Si AMLCDs are in mass production, with the level of integration expected to increase as more circuit functionality is added to the panel: the objective being a System-on-Glass, SOG [2, 3, 11]. In order to achieve the higher circuit speeds needed to replace external MOSFET circuits, the performance of the poly-Si TFTs has been leveraged by way of higher carrier mobility and shorter channel lengths. Both of which have been achieved within the constraints of a glass-compatible process.

In Sect. 7.2, the more conventional processing of poly-Si TFTs is presented; in particular, the formation of poly-Si thin films by laser crystallisation. It will be shown that the thin film formation technique determines grain size and structure, and this has a fundamental impact upon carrier mobility and other basic device parameters, such as threshold voltage and leakage current. These performance parameters can also be affected by the gate dielectric and the device architecture, and those topics, together with the process flow for TFT and AMLCD fabrication, are presented in Sects. 7.3 and 7.4, respectively. Advanced crystallisation processes, leading to large grain and high carrier mobility material, are reviewed in Sect. 7.5. Finally, Sect. 7.6 contains a brief overview of the issues underlying the application of poly-Si TFTs to AMFPDs, including the factors favouring it for small/medium sized displays.

In summary, this chapter focuses on poly-Si material preparation, and TFT design and fabrication. The discussion of the performance of these devices is presented in Chap. 8. Throughout these two chapters, parallels are drawn, where appropriate, between the physics and technology of poly-Si TFTs and IC MOSFETs, from which it will be seen that poly-Si TFTs share more similarities with these devices than with the other TFT technologies discussed in this book.

7.2 Poly-Si Preparation

As mentioned above, the electron mobility in poly-Si has increased from <5 [12] to ~900 cm^2/Vs [1] over the last 20 years or so. These increases are due to several evolutionary changes in the preparation of the material, which are the subject of this section and of Sect. 7.5. At the upper end, the mobility is comparable to the low field value of long-channel SOI MOSFETs [1], although, in poly-Si, these are field effect mobility values, which are degraded from the band mobility values by the presence of band gap states near the conduction band edge. The nature and distribution of these states, together with their impact on carrier mobility is discussed in Chap. 8.

In discussing poly-Si performance, the electron mobility is frequently quoted as a figure of merit, and this approach is also used in this chapter. However, it should be appreciated that a large mobility alone is not sufficient for the device to have a useful application in the display-addressing field: it must also be accompanied by a low leakage current and a low threshold voltage. Moreover, these parameters need to be achieved with a glass-compatible process, within which the maximum process temperature is, ideally, kept below ~450 °C. Even this modest temperature requires a harder glass than that used in the lower temperature a-Si:H process, and a brief overview of glass plate issues is presented in Sect. 7.2.1. Finally, the overall complexity of the process needs to borne in mind, as, the more complex the process, the more expensive the final product will be.

7.2.1 Background

Before proceeding to a detailed discussion of the laser crystallisation process, it is worth briefly reviewing the preceding technologies from which the laser process was ultimately identified as the most commercially attractive.

The first generation technology was based upon a well-established LPCVD process, which was employed in the semiconductor industry for the fabrication of MOSFET gate layers. This was the direct deposition of a poly-Si layer at ~620 °C, but which had a small grain size of ~100 nm and yielded an electron field effect mobility of ~5–7 cm^2/Vs [12, 13]. This was a demanding process for glass substrates, as the deposition process approached the substrate's softening temperature, and could lead to warping and distortion of the substrate. In addition,

the finished TFTs required exposure to atomic hydrogen, for several hours at ~350 °C in an RF plasma, in order to passivate defects in the film. The long plasma exposure time was because the hydrogen diffused laterally through the gate oxide before entering the poly-Si. The consequence of this lateral diffusion process was that TFTs, with increasing channel length, required increasingly long exposure times for the defects in the centre of the channel to be passivated [12, 13].

The direct deposition process was superseded by a second generation process, using a precursor film of a-Si. This could be deposited either by LPCVD at 550–600 °C [13–15], or by PECVD (using an a-Si:H reactor) at 350 °C [15], or the standard, small grain LPCVD films could be amorphised by high dose silicon ion implantation [16]. In all cases, the objective was to use pre-cursor films, which were essentially amorphous. These films then underwent a phase transformation into a polycrystalline form by a process of solid phase crystallisation (SPC) [13–16], which relied upon a sparse distribution of incipient seeds or random nucleation within the film, to seed grain growth. For seed-free films, this was a two-stage process consisting of the growth of stable nuclei, which then seeded grain growth. Both of these processes are thermally activated, and the overall activation energy of the SPC process has been found to be within the range 3.1–3.9 eV, depending upon the film preparation technique [16]. The thermal budget for this process was up to tens of hours in the temperature range 580–630 °C [16], and the resulting films had large, faulted dendritic grains, up to 1μm long [14, 16]. These larger grains gave TFTs with electron field effect mobilities up to ~40 cm^2/Vs [13, 15].

Even more than with the direct deposition process, the longer exposure times to high temperatures were particularly demanding on the glass substrate, and the dimensional instability of the glass became an issue. The mechanical properties of glass are determined by its manufacturing process, and, in particular, its cooling rate from the melt determines the temperature at which it solidified. Only at this temperature is the glass in thermal equilibrium, and, at lower temperatures, it will tend to relax to a new equilibrium state. For the glasses used for TFTs, this will be such a slow process at room temperature that it can be ignored, and should be distinguished from reversible dimensional changes governed by its coefficient of thermal expansion. However, at the temperatures used for SPC, the irreversible dimensional changes become significant, as shown by the results in Fig. 7.1 [15]. The results in Fig. 7.1a are normalised measurements of shrinkage (usually referred to as compaction), in a hardened glass substrate, as a function at exposure time to the range of temperatures used for SPC. It will be seen that the compaction is a thermally activated process to an equilibrium state, which, as expected, is temperature dependent. In summary, the higher the annealing temperature, the smaller was the dimensional change, and the faster it occurred. For photolithography, it is essential that the substrate is dimensionally stable through all mask alignment stages, and the required degree of stability is determined by the mask alignment tolerances and the size of the substrate. For instance, with a 30 cm substrate and a 3 μm alignment tolerance, the substrate will need to maintain a dimensional stability of 10 ppm from the first to the last alignment stage. As seen from Fig. 7.1a, the overall dimensional stability of glass was far worse than this,

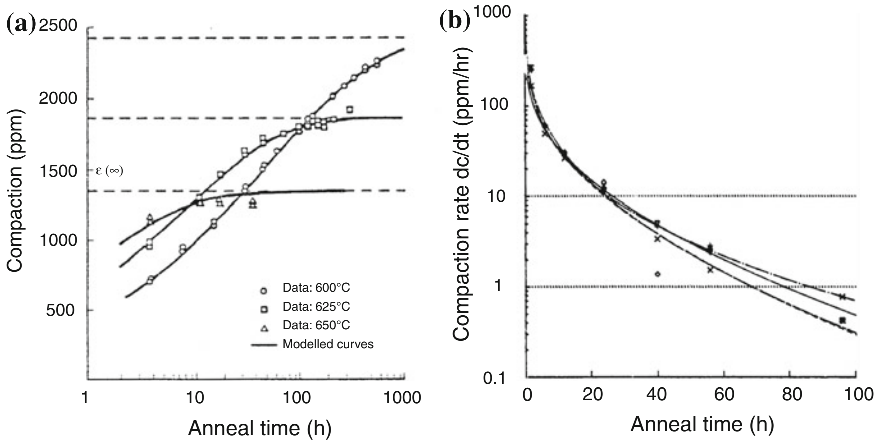

Fig. 7.1 **a** Normalised compaction measurements, on 'hardened' glass plates, as a function of annealing time at 600–650 °C (Reprinted from [15] with permission of SID), and **b** normalised compaction rate measurements at 625 °C

and it was necessary to pre-shrink the glass prior to the first alignment stage. Furthermore, as the equilibrium compaction was a function of the anneal temperature, the substrate needed to be pre-compacted at the temperature at which the SPC process was carried out. The easiest way to determine the required pre-compaction time was from a plot of the differential of the data in Fig. 7.1a, and, as an example, the compaction rate at 625 °C, as a function of the anneal time, is shown in Fig. 7.1b. Hence, if, for example, a 10 h SPC process was used, then a compaction rate, prior to processing, of 1 ppm/h was needed to ensure that <10 ppm compaction occurred during the SPC process, and this required a pre-compaction anneal of ~ 80 h.

As with the direct deposition process, prolonged exposure to atomic hydrogen in an RF plasma was required to passivate the defects in the large, but highly faulted, SPC grains. Nevertheless, demonstration displays, with integrated drive circuits, were fabricated on glass substrates by this process [13, 15]. However, the thermal budgets, the issues with glass, and the plasma hydrogenation process did not make SPC an attractive process for industrialisation. Most of these issues were resolved with the third generation process, which used excimer laser crystallisation, and this is now the industry standard process. A more extensive review of the SPC process can be found in Ref. [17].

The current industry standard crystallisation procedure of excimer laser annealing, ELA, is discussed in Sect. 7.2.2, and in Sect. 7.2.3 other laser techniques are briefly considered, although a more detailed discussion of them is contained in Sect. 7.5, which deals with advanced crystallisation techniques for large grain material. Finally, in Sect. 7.2.4, a variant of the SPC process is presented, which uses metal silicide-mediated crystallisation to reduce the thermal budget of the SPC process.

7.2.2 Excimer Laser Crystallisation

7.2.2.1 Introduction

Excimer lasers are gas lasers operating in the ultra-violet wavelength range, from 193 to 351 nm depending upon the gas mixture chosen. For crystallisation of a-Si, the preferred gas mixture is XeCl, giving a wavelength of 308 nm; similar crystallisation results have been obtained from KrF excimer lasers at 248 nm, but the 308 nm laser is preferred for industrialisation, as the longer wavelength is less damaging to the optical components in the beam path. These are pulsed lasers, with a typical pulse duration of ~30 ns, a maximum repetition frequency of 600 Hz, and can deliver up to 0.9 J/pulse [18]. The raw pulse shape is semi-Gaussian, with dimensions of ~1 cm × 1 cm, but, for crystallisation, a pencil shaped beam is preferred, and beam shaping optics are used to produce a highly elongated line-beam, whose dimensions can be up to 465 mm in the long axis and down to 350 μm for the short axis [18]. The steep edges in the short axis profile have led to the beam shape being referred to as a 'top-hat' beam, and all the line-beam irradiations discussed in this section will be assumed to have this shape, unless specified otherwise. Measurements of an industrial line-beam profile are shown in Fig. 7.2a, and a schematic illustration of an ELA crystallisation system is shown in Fig. 7.2b, where the key components are an attenuator for controlling beam intensity, the homogeniser and beam shaper to produce the line-beam, and a condensing lens to focus the beam on the underlying plate. The plate is mechanically swept through the short axis of the beam at a rate, which delivers a multi-shot process, of typically 10–30 shots per point for commercial processing, so that the plate translation distance between shots is typically in the range 12–50 μm for short axis lengths of 350–500 μm.

7.2.2.2 Crystallisation Process

At 248 nm and 308 nm wavelengths, the optical absorption depth in a-Si is 5.7 nm and 7.6 nm, respectively, so that the incident energy is strongly absorbed in the silicon film, resulting in intense heating. If the incident energy density is high enough, this will heat the film to its melting point, T_m, of 1420 K, where the optical and thermal constants for a-Si [19] and c-Si [20] are shown in Table 7.1. The required energy density, E_{th}, to cause surface melting can be calculated from the solution of the heat diffusion equation, which yields the following approximate analytical solution [21] (provided the optical absorption depth of the film, $1/\alpha$, is less than the thermal diffusion length, $\sqrt{(D\tau)}$, where $D = k/\rho C_p$):

$$E_{th} = \frac{(T_m - T_0)\sqrt{\pi}\rho C_p \sqrt{D\tau}}{2(1-R)} + \frac{H\Delta z}{\rho(1-R)} \qquad (7.1)$$

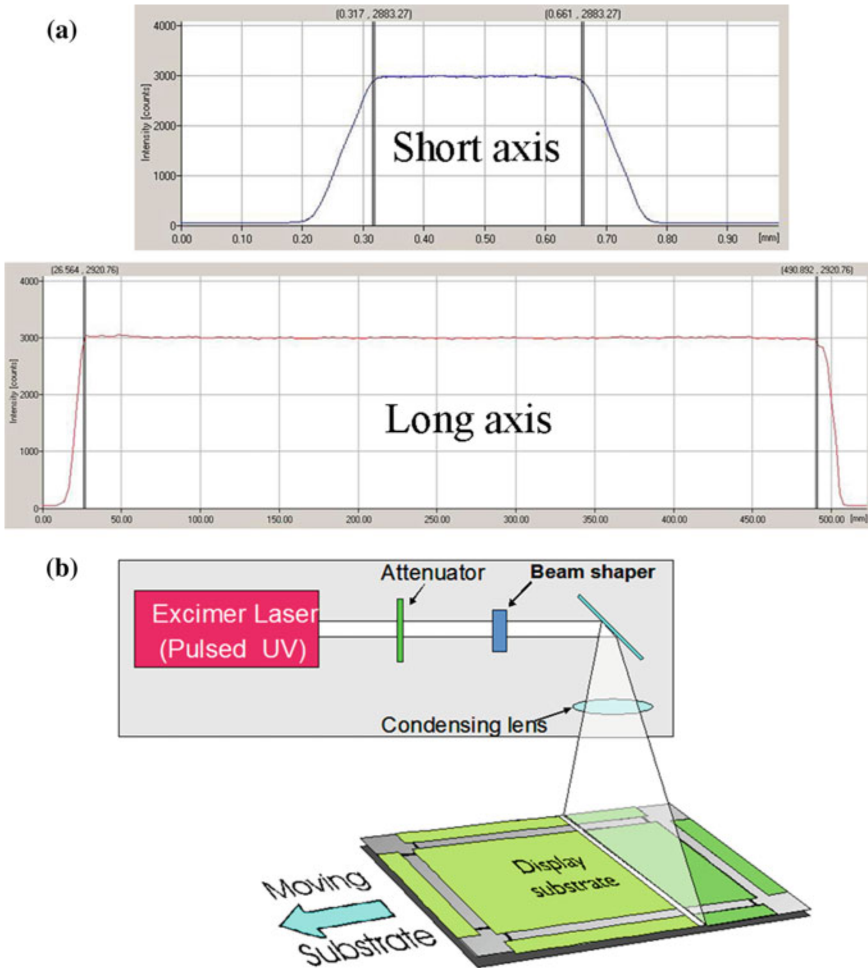

Fig. 7.2 **a** Laser intensity profiles from a 464 mm × 340 μm line-beam excimer laser annealing, ELA, system (data supplied by Coherent GmbH), **b** schematic illustration of an ELA system

The first term in Eq. 7.1 is the intensity to bring the surface of the film up to the melting temperature, and the second term accounts for the latent heat required to melt a thin film of thickness Δz. (T_0 is initial film temperature, ρ is the density of a-Si, C_p is its specific heat, D its diffusion coefficient, τ is the heating time, H is the latent heat of melting, and R is reflectivity).

Evaluation of Eq. 7.1, using the optical and thermal coefficients listed in Table 7.1, predicts a melt threshold energy density of ~75 mJ/cm^2 for a-Si, which agrees well both with full numerical simulations giving 70–90 mJ/cm^2 [22], and experimental data in the range 70–100 mJ/cm^2 [23, 24]. The thermal diffusion length in a-Si, for a 30 ns pulse, is 120 nm, so that we can readily expect films up

Table 7.1 Optical and thermal constants for amorphous, crystalline, and liquid Si [19, 20, 22]

Material	$1/\alpha$ (at 308 nm)(nm)	R (at 308 nm)	$1/\alpha$ (at 248 nm)(nm)	T_m (K)	ρ (gcm^{-3})	C_p $Jg^{-1}K^{-1}$	k ($Wcm^{-1}K^{-1}$)	H (Jg^{-1})
a-Si	7.6	0.57	5.7	1418	2.26	1.1	1.3×10^{-2}	1282
c-Si	6.9	0.66	5.5	1687	2.31	1.0	0.23	1800
Liquid Si	6.9	0.69	6.4		2.52	1.1	0.51	

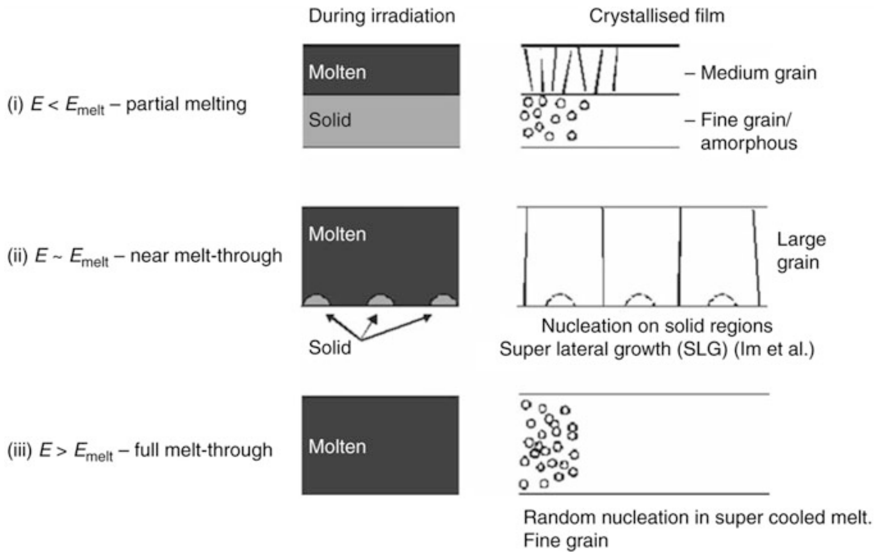

Fig. 7.3 Schematic illustration of a-Si melting regimes during excimer laser irradiation, and the resulting poly-Si grain structure

to at least this thickness to be melted at high enough incident energy densities. Indeed, experimental data have shown the melt depth increasing linearly with energy density up to 145 nm [25], and simulations have predicted the same dependence for melt depths up to at least 300 nm [26].

In fact, current understanding of the crystallisation mechanism of a-Si, has shown that the melt depth of the film is a crucial factor in determining the outcome of the process [27–30]. This is shown schematically in Fig. 7.3, where three melting regimes are identified. Following partial film melting, the crystallised film has a vertically stratified appearance, as shown in Fig. 7.4a, with mid-sized grains (~100 nm) within the previously melted region, and either a fine grain or amorphous region beneath it. Fig. 7.3b shows the film almost fully melted, with small solid islands remaining at the back of the film, seeding the growth of large (~300 nm) high quality grains, as the film cools. These columnar grains extend through the entire thickness of the film, which no longer shows vertical stratification. This process was identified by Im et al. [27, 28], and given the name super-lateral growth (SLG). As will be shown below, this is the crystallisation regime, which yields high quality TFTs. Finally, for the fully melted film in Fig. 7.3c, the seeding centres responsible for the SLG growth are lost, and crystallisation of the film relies upon random nucleation in a super-cooled melt, resulting in a fine grain film [27].

From the above scenario, it is apparent that the optimum energy range is that which results in the SLG regime: energy densities above and below this result in smaller grain poly-Si. However, as shown by the grain size results in Fig. 7.4b, the SLG regime occurred over a very limited energy density range of ~45 mJ/cm^2

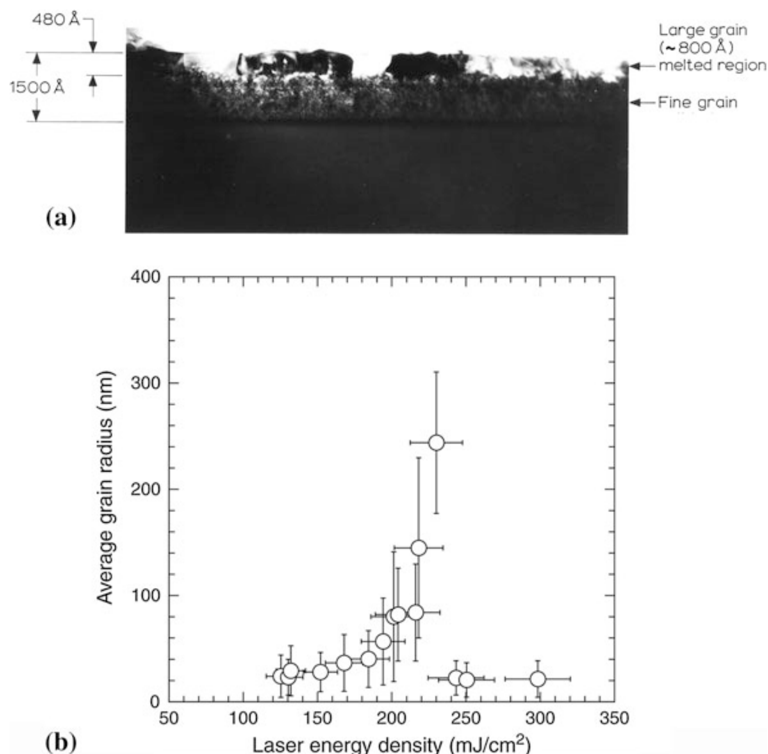

Fig. 7.4 **a** Cross-sectional TEM micrograph of a partially melted 150 nm thick a-Si film, showing the resulting vertically stratified grain structure (Reprinted from [23] with permission of IEEE), and **b** variation of average grain radius with laser energy density for excimer laser crystallized a-Si films (100 nm thick films capped with 50 nm SiO_2). (Reprinted with permission from [27]. Copyright (1993) American Institute of Physics)

from ~195 to ~240 mJ/cm^2 [27]. These particular results were from single shot irradiations [27], and qualitatively identical results were obtained from multi-shot irradiations [30], apart from a growth in SLG grain size with increasing shot number. As discussed below, the limited size of the SLG window has major implications for the implementation of the crystallisation process to produce high performance TFTs.

The essential features of the above process are fully demonstrated in the correlation of TFT behaviour with the energy density used to crystallise the film. This can be most easily seen with static irradiations of a 40 nm thick a-Si film, using the raw, semi-Gaussian excimer laser beam, as shown in Fig. 7.5a–c [25]. It should be emphasised that this mode of irradiation is not the conventional TFT crystallisation procedure (which involves swept, line-beam irradiations), but was used purely as an experimental tool. Figure 7.5a shows a profile of electron mobility measurements made on a line of non-self-aligned TFTs, with a W/L ratio of 50/6 μm, and with a spatial pitch of 220 μm. The profile through the approximately Gaussian distribution

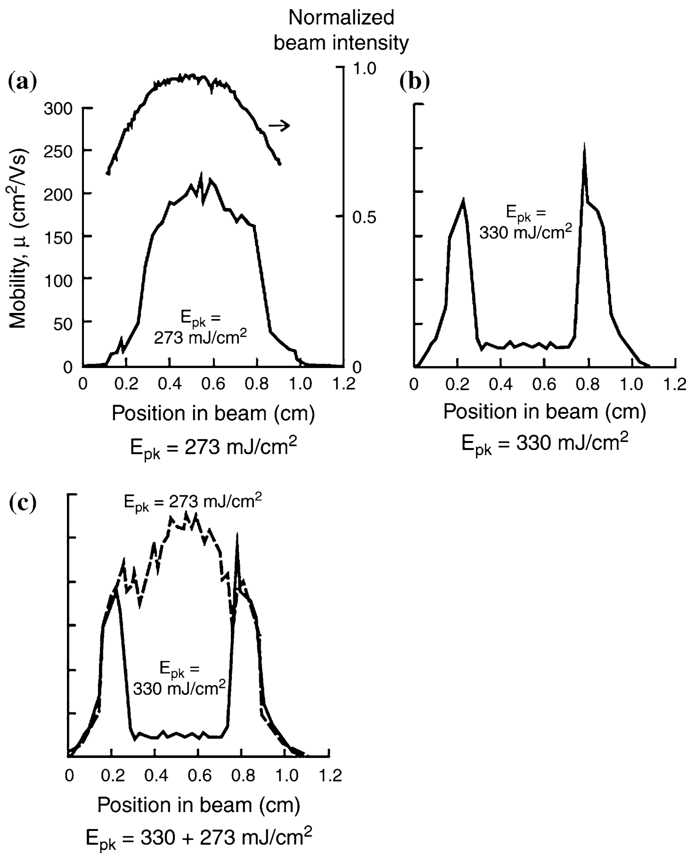

Fig. 7.5 Electron mobility as a function of position in stationary KrF excimer laser beam, measured after irradiations at the following peak intensities: **a** 273 mJ/cm^2, **b** 330 mJ/cm^2, **c** 330 mJ/cm^2 followed by 273 mJ/cm^2. (Reproduced with permission from [34])

of energy densities within the beam facilitates a precise mapping of electron mobility (and other device parameters) against incident energy density [25]. The maximum beam intensity had been set to ~270 mJ/cm^2, which was a value in the SLG regime, and a progressive increase in mobility from zero to ~200 cm^2/Vs is seen as the crystallisation energy increased from zero to its maximum. Also of note are the rapid changes in mobility at the x-axis locations of 0.3 and 0.8 cm, which corresponded to the positions within the beam at which the threshold energy density occurred for the SLG regime (~225 mJ/cm^2). In Fig. 7.5b, the maximum energy density was increased to 330 mJ/cm^2, which was large enough to induce full melting of the film over the central portion of the beam. The ensuing fine grain material [27] resulted in a reduction of electron mobility, within the centre of the irradiated region, from ~200 to ~25 cm^2/Vs, whilst the edge regions, irradiated at lower energy densities, retained the appearance seen in Fig. 7.5a. The abrupt decrease in mobility

gave an SLG window size of ~45 mJ/cm^2, which is much the same as the energy window in the TEM data of Im et al. [27]. Finally, Fig. 7.5c shows the result of re-irradiating the material from Fig. 7.5b using lower intensity conditions, which corresponded to the SLG regime. This converted the previously fine grain material back into larger grain SLG material, with a consequent recovery in electron mobility. Hence, the material can be cycled in and out of the SLG regime, depending upon the final energy density used to crystallise the film. This has particular implications for the uniformity and process window size of the conventional swept beam process, as discussed in the following section.

7.2.2.3 TFT Crystallisation

An overview of TFT results from swept beam processing is shown in Fig. 7.6 [25, 31]. This figure shows the dependence of electron mobility, in n-channel TFTs, on the irradiation energy density, with the a-Si precursor film thickness as an independent parameter. Figure 7.6a contains results from LPCVD precursor a-Si, crystallised by a 248 nm KrF semi-gaussian beam, and the data in Fig. 7.6b are from the more commonly used PECVD pre-cursor a-Si:H, crystallised by a 308 nm XeCl line beam. The two sets of curves demonstrate the same essential

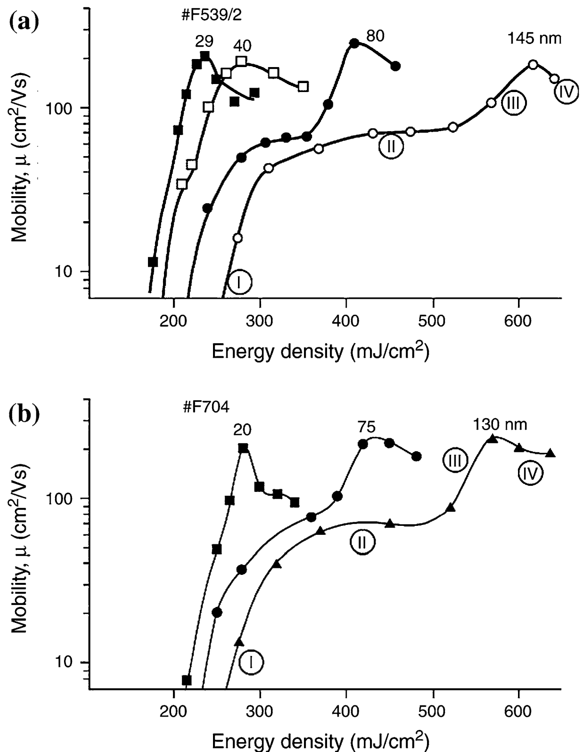

Fig. 7.6 Electron mobility as a function of excimer laser energy density for a-Si precursor films of different thickness (**a**) 248 nm (KrF) irradiation of LPCVD a-Si, (**b**) 308 nm (XeCl) irradiation of PECVD a-Si:H. (Reprinted from [31] with permission of SID)

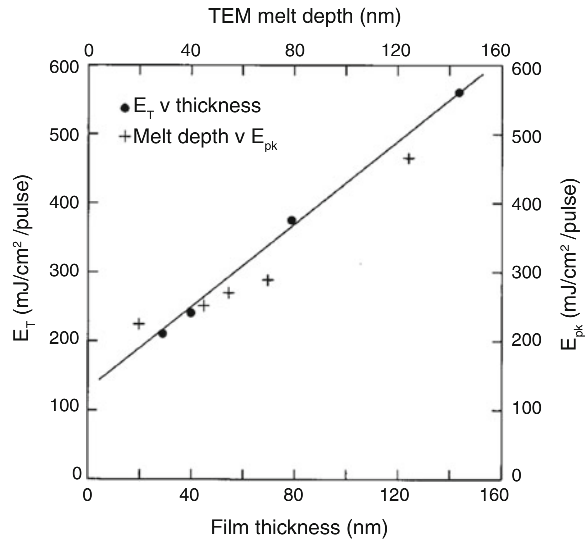

Fig. 7.7 Cross sectional TEM measurements of the melt depth in a 150 nm thick film with crystallization energy density (+ symbol, *top* and *right axes*). Variation of the threshold laser energy density for high mobility TFTs as a function of film thickness (• symbol, *left* and *bottom axes*) (from the TFT measurements in Fig. 7.6a). (Reprinted with permission from [25]. Copyright (1997) American Institute of Physics)

features of the crystallisation process, which were independent of the laser wavelength, the type of precursor material, and the beam shape details. The two most obvious features in these curves are, firstly, that the outcome of the crystallisation process was a strong function of film thickness. In fact, the energy densities required to achieve maximum carrier mobility scaled approximately linearly with film thickness, as shown in Fig. 7.7 [25]. Secondly, the crystallisation process was not a simple monotonic function of energy density. The results in Fig. 7.6 only show electron mobility, and the other key device parameters of sub-threshold slope and threshold voltage showed a corresponding dependence on crystallisation energy density, and qualitatively identical results were also obtained from p-channel TFTs [25]. Figure 7.8 shows the variation of leakage current with laser intensity, and this displays more complex behaviour than the mobility results, insofar as the leakage current initially increased and then decreased. From the dependence of leakage current on channel length, the initial increase in leakage current was ascribed to a resistive, drift current, which scaled with increasing mobility. The current at higher energy density was a generation current, and this decreased as the improving material quality increased the electron–hole pair generation lifetime [25]. The detailed analysis of this data is discussed in Chap. 8.

Figures 7.6 and 7.8 have focussed on specific parameter values, and Fig. 7.9 shows the overall transfer characteristics of high quality, non-self-aligned n- and p-channel TFTs obtained from this process. They illustrate the attainment of low leakage currents, small sub-threshold slopes, as well as high on-currents.

The crystallisation regimes in Fig. 7.6 can be broken down into four phases, which are most clearly seen in the thicker films, but can also be discerned by points of inflection in the thinner films. The four phases were an initial increase in mobility (I), a plateau region (II), a second rise in mobility (III), and, finally,

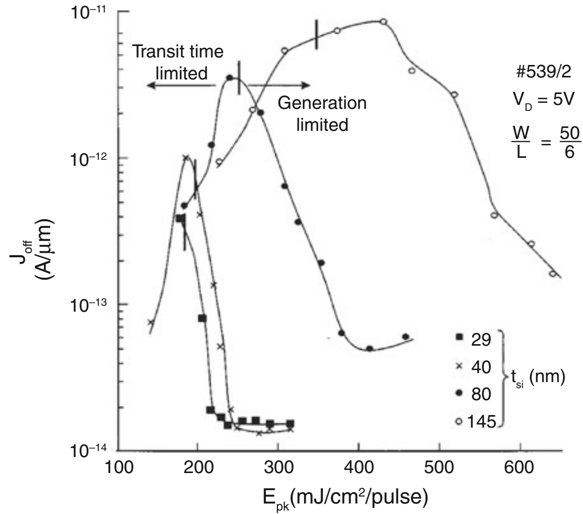

Fig. 7.8 TFT leakage current as a function of excimer laser energy density for a-Si precursor films of different thickness crystallized by swept beam 248 nm (KrF) irradiation. (Reprinted with permission from [25]. Copyright (1997) American Institute of Physics)

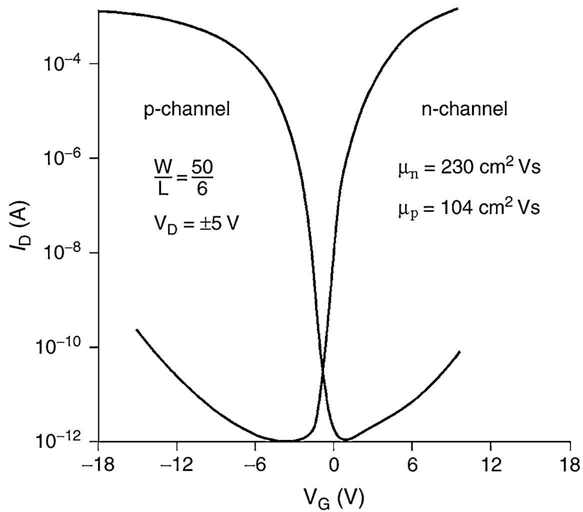

Fig. 7.9 Transfer characteristics of n- and p-channel excimer laser crystallized non-self-aligned TFTs. (Reprinted with permission from [72]. Copyright (1998), The Electrochemical Society)

a decrease in mobility (IV). The initial increase in mobility occurred above the melt threshold energy, as the surface of the film was converted into a poly-crystalline form. When the thickness of this region was less than the equilibrium band bending thickness at inversion, the band bending extended into the under-lying fine grain/amorphous silicon, as shown schematically in Fig. 7.10a (and this vertical stratification is clearly visible in the TEM micrograph in Fig. 7.4a). As discussed in Sect. 6.2.4, when there is a high trap density within the band bending region, the partition of induced carriers between trapped and free states results in a diminished value of field effect mobility. Moreover, the fewer trapping states there

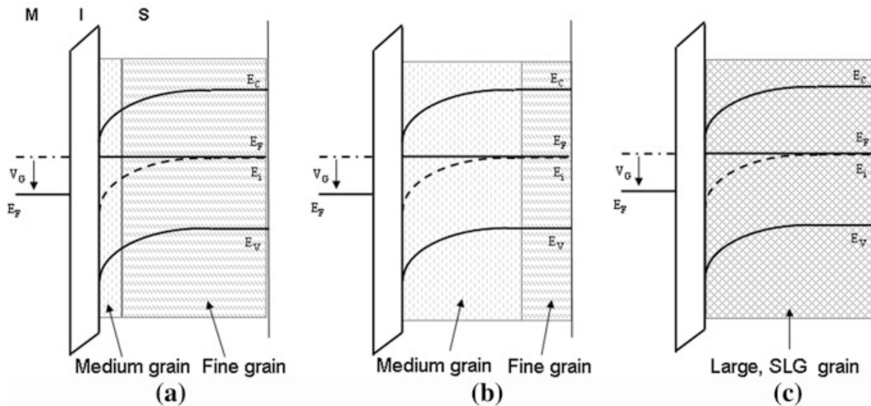

Fig. 7.10 Schematic illustration of band bending diagrams superimposed upon the grain structure regime in the laser crystallized films (**a**) regime I, (**b**) regime II, and (**c**) regime III. (For simplicity, constant values of gate bias and band bending are shown in each diagram)

are in this region, the higher the field effect mobility will be. Figure 7.7 shows that the melt depth increased with increasing crystallisation energy, and, as the thickness of this crystallised region increased, the electron field effect mobility similarly increased (due to the reduced number of carriers going into the fine grain, high trap density material at the bottom of the space charge region). This mobility increase continued until the band bending was contained entirely within the crystallised region, as shown schematically in Fig. 7.10b. When this occurred, regime II was entered, and further increases in crystallisation depth had a minimal effect upon the carrier mobility. The regime II plateau was resolved most unambiguously in the thicker films in Fig. 7.6, and Fig. 7.11a shows a TEM micrograph of the mid-sized grain structure in the upper portion of the partially melted film. Figure 7.6a shows that the threshold energy density for regime II with the 145 nm film was $\sim$300 mJ/cm^2, and, from Fig. 7.7, the melt depth at this energy density was $\sim$50 nm. Hence, the depletion depth for surface inversion was comparable to 50 nm at this energy density, and illustrates why regime II was also seen in the 80 nm film, but was not resolved in the 40 nm film.

Ultimately, with increasing incident energy density, the melt depth increased until the film was almost fully melted, and the SLG regime was initiated. This is depicted in the band bending diagram shown in Fig. 7.10c, and the SLG grain structure is shown in Fig. 7.11b. The increase in grain size and quality, compared with regime II grains (Fig. 7.11a), was responsible for the abrupt increase in electron mobility in regime III, and Figs. 7.6 and 7.7 demonstrate how the energy density for this regime scaled with film thickness [25]. Hence, to obtain maximum carrier mobility, the crystallisation energy density must be matched to the film thickness.

Finally, at the highest energy densities, the electron mobility started to decrease in regime IV, due to the incipient formation of fine grain material. However, the

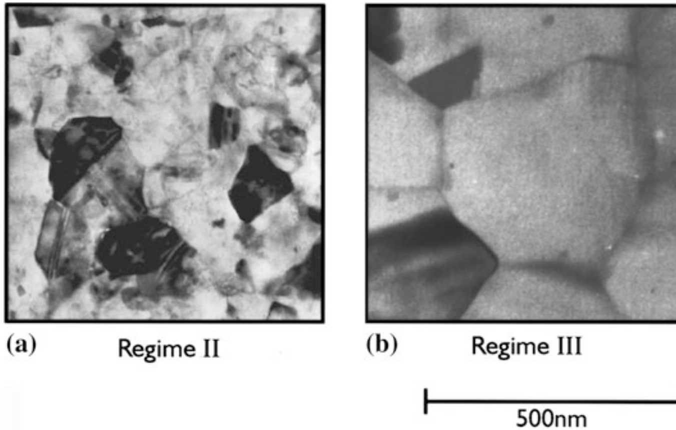

Fig. 7.11 Plan-view TEM micrographs showing the grain structure in ELA poly-Si, crystallised in (**a**) regime II (partial melting) and (**b**) regime III (SLG). (Reprinted with permission from [25]. Copyright (1997) American Institute of Physics)

decrease in mobility was much smaller than seen with the stationary beam process of Fig. 7.5b. This was because, in the swept beam process, subsequent lower intensity pulses, in the trailing edge of the beam, can reset the material back into the SLG regime. As discussed in the next section, the resetting of the material back into the SLG regime is a function of beam shape and shot number, and has implications for the overall trade-off between plate throughput and device parameters.

7.2.2.4 ELA Process Control Issues

As shown by the results in Fig. 7.6, to obtain high carrier mobility devices, the film needs to be crystallised within the SLG regime, and, ideally, at the energy density, E_m, giving the maximum mobility. But, there is limited accuracy in the precise setting of the laser energy density, and, moreover, the pulse-to-pulse fluctuations in energy density [32] mean that samples will occasionally be exposed to higher intensity irradiations, and, where this causes full melt-through, can lead to a consequent degradation in device parameters. Comparison of Figs. 7.5b and 7.6b shows that the magnitude of this degradation is determined by the opportunity, within the process, to re-irradiate the fine grain material, and to convert it back to large grain SLG material. The static irradiations in Fig. 7.5b can be regarded as a zero pulse overlap process (giving gross mobility non-uniformity when full melt-through occurred), whereas the 100-shot, swept beam process in Fig. 7.6b can be regarded as a 99 % pulse overlap process (giving greatly improved uniformity, even after full melt-through). This latter point can be understood by recognising that when an anomalously high intensity pulse has fully melted the stripe of

material exposed to it, the next pulse will overlap most of this poorly crystallised region, and the fine grain material will be re-melted, and converted back to the large grain SLG material. Nevertheless, there will be a thin strip of material (equal to the plate translation distance), which will not be fully overlapped by the top-hat region of the next pulse, but, at best, by its trailing edge. The recovery of this thin strip will then depend upon the relative size of the plate translation step, Δx, and the spatial width of the SLG window on the trailing edge of the beam, X_{SLG}, as illustrated in Fig. 7.12a [33]. Only if the SLG width on the beam edge, X_{SLG}, is greater than the translation step, Δx, will good recovery occur. (Where $\Delta x = W/N$, and W is the beam width, and N is the number of shots in the process).

Hence, the practical issue of plate processing is the trade-off between higher plate throughput (and reduced pulse overlap) and acceptable uniformity within a realistic process window.

This trade-off can be best illustrated within a quantified framework: for example, an acceptable laser process window, ΔE, could be defined as one within which the average carrier mobility, μ_{av}, varies by $<\pm 10$ %, or within which the maximum scatter in mobility ($\mu_{max}-\mu_{min}/\mu_{av}$) is $<\pm 10$ %. (The smaller of these two windows

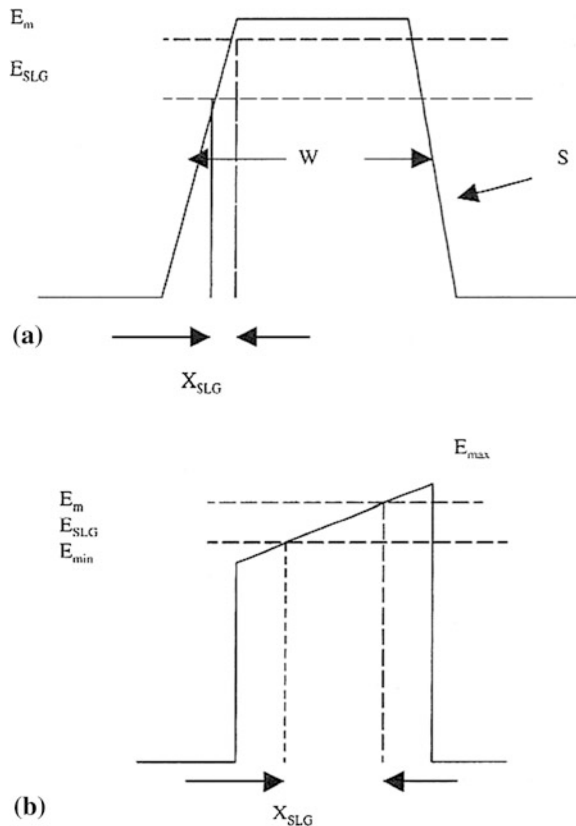

Fig. 7.12 Schematic illustrations of excimer line-beam pulse shape, showing the width of the SLG recovery regions, X_{SLG}, with: **a** top hat pulse, and **b** ramped pulse (where E_{SLG} is the threshold energy for the SLG regime, and E_m is full melt-through energy). (Reprinted with permission from [33]. Copyright (2004) The Japan Society of Applied Physics)

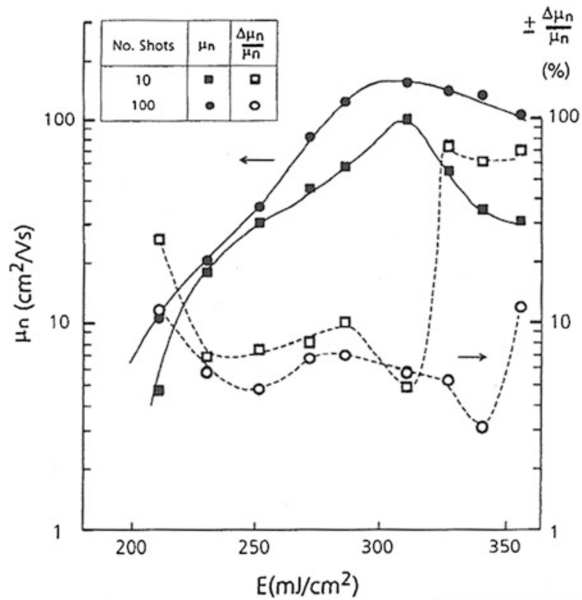

Fig. 7.13 Comparison of electron mobility values, and the maximum scatter in those values, for 100-shot and 10-shot top-hat ELA line-beam processing. (Reprinted with permission from [72]. Copyright (1998), The Electrochemical Society)

would be the relevant one.) Given that the fundamental issue is the tolerance of the process to random fluctuations in laser intensity, which cause full melt-through, this can be examined by deliberately irradiating the sample into this regime, and examining the size of the process window, ΔE, as a function of pulse overlap. This is illustrated in Fig. 7.13, in which crystallisation energy densities above the full-melt threshold are used to compare a 100-shot process (99 % overlap) with a 10-shot process (90 % overlap). The 100-shot process yielded an average mobility of 145 ± 15 cm^2/Vs, within a broad process window, ΔE, of 53 mJ/cm^2, due to good recovery of the full-melt material by the trailing edge of the beam [33, 34]. In addition, the mobility scatter remained well below ± 10 % over this energy range. The 10-shot process resulted in a lower average mobility of 90 ± 10 cm^2/Vs (due to a smaller SLG grain size [30, 31]), and a much stronger fall-off in average electron mobility at the higher energies, giving a significantly smaller process window, ΔE, of 20 mJ/cm^2. In both cases, this window was centred about the optimum intensity, E_{opt}, of 310 mJ/cm^2, which gave the maximum mobility. Hence, for the 10-shot process, the size of the energy window was just ± 3.3 % of the target intensity, E_m, so that random variations in pulse intensity greater than this will cause unacceptable uniformity variations. Associated with the lower average mobility at higher laser intensities, in the 10-shot sample, was also a sharp increase in mobility scatter once the full melt through regime was triggered. This was due to incomplete and variable recovery of the fine grain material by the trailing edge of the pulse, and was consistent with SEM observations of a periodic grain size variation, from small grain to large grain, at the pitch of the plate movement through the laser beam [33]. One way to improve the trailing edge recovery process

is to simply broaden the trailing edge; however, the energy within the pulse can be used more efficiently by ramping the top of the beam instead, as illustrated in Fig. 7.12b. With this beam shape, the size of the energy process window can be increased by a factor of ~2 for a 10-shot process [33].

In view of the uniformity issues with a high throughput and low shot number process, typical plate processing uses a 20-shot process, yielding an electron mobility of ~120 cm^2/Vs, within an energy window of ~30–40 mJ/cm^2. However, the major contributory factor to improved control and uniformity of the ELA process for poly-Si AMLCDs has been improvements in peak-to-peak pulse energy stability [18, 32] to 3 % over ± 3 sigma. Moreover, when this is combined with a technique to randomise intensity variations along the beam length, the more stringent uniformity requirements for AMOLED displays may also be met [18].

7.2.3 Other Laser Techniques

Whilst excimer laser annealing is the currently preferred technique for the commercial crystallisation of poly-Si, other lasers have been examined as alternatives in order to address some of the ELA issues themselves. These include pulse-to-pulse stability, and the cost of ownership, which includes frequent gas refills, window cleaning, and general downtime for tube and system maintenance. In particular, diode pumped solid state lasers have been advocated to address both the pulse stability and cost of ownership issues, with neodymium-doped yttrium aluminium garnet, Nd:YAG, lasers being the most commonly studied [35–37]. These can be operated either in continuous wave, CW, mode, or in Q-switched mode, delivering short duration pulses (≥10 ns) of 800 mJ/cm^2, with a repetition frequency of 4 kHz and an output power of 200 W at 532 nm [35]. The fundamental output wavelength of these lasers is 1064 nm, which is in the infrared, and radiation at this wavelength would not be efficiently absorbed in thin silicon films. Hence, for crystallisation of a-Si, the Nd:YAG lasers are usually operated in the frequency-doubled mode at a wavelength of 532 nm. This is in the visible radiation band, and these Nd:YAG-based systems are frequently referred to as green laser annealing systems. For CW use, although Nd:YAG lasers have been used [38], Nd:YVO_4 lasers are preferred for high power applications. These are also frequency doubled, and can emit 10 W of radiation at 532 nm [39–42].

Both the pulsed and CW approaches can produce material with comparable properties to the ELA process, but they are also able to produce large grain, high quality material with electron mobilities up to 250 cm^2/Vs [36] and 566 cm^2/Vs [39], respectively. In view of the large grain options with these solid state lasers, it is more appropriate to discuss them in detail in Sect. 7.5, where they can be compared with the large grain processing procedures available with modified excimer laser crystallisation.

7.2.4 Metal Induced Crystallisation

Metal induced crystallisation (MIC) is a solid phase crystallisation (SPC) process, in which the presence of the metal can enhance the crystallisation rate of a-Si into poly-Si. This process has been viewed as a potentially simpler, cheaper and more uniform alternative to ELA. Equally, by accelerating the SPC process, so that it could be implemented at lower temperatures and with shorter crystallisation times, it was seen as a more production-worthy alternative to conventional SPC. However, the resulting TFTs have had persistently high leakage currents, which has limited the commercial application of the technique, although these can be minimised by combining it with ELA.

A large number of different metals have been found to promote MIC [43], some of which act in the elemental state, such as In, whilst others, including several transition metals, as well as Pd and Pt, act via the metal silicide. This latter process is sometimes referred to as silicide-mediated crystallisation (SMC). For the application of MIC to poly-Si TFTs, the metal of greatest interest has been Ni, because one of its silicides is a very good lattice match to crystalline Si. The role of Ni in the enhanced crystallisation rate of a-Si is discussed in Sect. 7.2.4.1 and the use of this procedure to fabricate poly-Si TFTs is reviewed in Sect. 7.2.4.2

7.2.4.1 Ni Mediated Crystallisation of a-Si

When thin films of Ni, or high concentrations of Ni are introduced into c-Si, a number of different nickel silicides readily form upon subsequent low temperature annealing. At ~200 °C, Ni_2Si is formed, this is converted into NiSi at ~240–390 °C, and the thermodynamically favoured final phase of nickel disilicide, $NiSi_2$, is formed at ~325–480 °C [43, 44]. $NiSi_2$ is a good lattice match to Si, having the same cubic lattice, and a lattice constant of 5.406 Å, which is within 0.4 % of the Si lattice constant of 5.430 Å. In Ni-doped a-Si films, crystallisation proceeded via a three-stage process of $NiSi_2$ precipitate formation, the nucleation of Si on the precipitates, and the subsequent migration of the precipitates, leaving trails of crystallised Si behind them [44]. In particular, regular octahedral precipitates of $NiSi_2$ formed at ~400 °C, and the good lattice match of $NiSi_2$ to Si made it an effective seed for the crystallisation of a-Si from the {111} faces of the precipitates [44]. Using 95 nm thick a-Si films implanted with Ni, both in situ TEM observation of crystallisation at 660 °C, and TEM examination of 500 °C furnace crystallised samples showed that the crystallisation process produced needle-like grains of Si. These grains propagated in the $<111>$ directions from the {111} precipitate faces, and were preferentially orientated in the $<110>$ direction to the sample surface. This was the precipitate orientation, which permitted maximum growth within the plane of the film [44]. A TEM micrograph of the needle-like grains is shown in Fig. 7.14 [45].

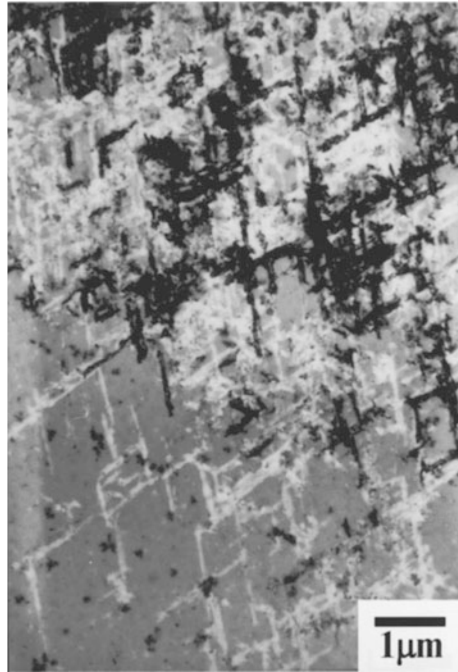

Fig. 7.14 Plan-view TEM micrograph of needle-like grains in $NiSi_2$-mediated crystallisation of a-Si, induced by 20 h annealing at 500 °C. (Reprinted with permission from [45]. Copyright (1997) American Institute of Physics)

The grain propagation took place by the movement of the precipitate through the a-Si, which consumed a-Si at its head and left the thin c-Si grain in its wake [44]. This process is shown schematically in Fig. 7.15a-c, in which the precipitate migrates towards the right, in the direction of the arrow. The overall process was driven by the reduction in free energy due to the conversion of a-Si to c-Si, which occurred with the nucleation of c-Si on one face of the $NiSi_2$ precipitate. In addition, the chemical potential of Ni was lower at the $NiSi_2$/a-Si interface than at the $NiSi_2$/c-Si interface, and the opposite was true of the Si atoms, i.e. the Si chemical potential was lowest at the $NiSi_2$/c-Si interface. It was proposed that the crystallisation process was driven by one of two alternative mechanisms [44]. In the first model, the $NiSi_2$ dissociated at the $NiSi_2$/c-Si interface, with the Si being incorporated into the growing grain, and the Ni diffusing down the chemical potential gradient to the head of the precipitate. On reaching the $NiSi_2$/a-Si interface, the Ni reacted with a-Si to form $NiSi_2$, and propagated the grain forward. This was referred to as the dissociative Ni diffusion process. The alternative mechanism was the non-dissociative diffusion of Si directly from the $NiSi_2$/a-Si interface to the $NiSi_2$/c-Si interface to sustain the migrating-precipitate/crystallisation process. In both cases, the rate limiting process was atomic diffusion within the precipitate, and, although the specific process was not positively identified, it was tentatively ascribed to dissociative Ni diffusion [44].

Given the controlling role played by Ni (or Si) diffusion through the precipitate, faster crystallisation rates were found with thinner precipitates, and crystallite

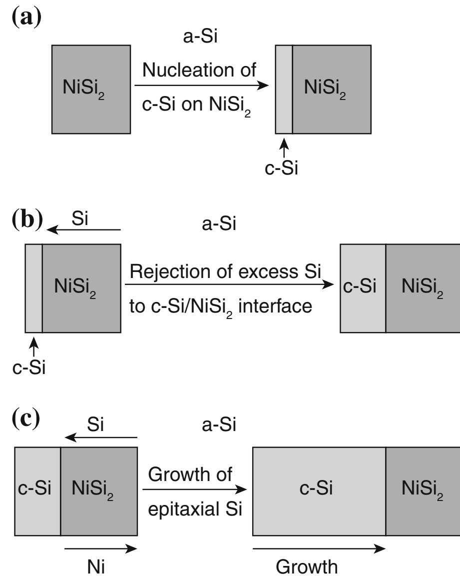

Fig. 7.15 Schematic representation of $NiSi_2$-mediated growth of c-Si grains. (Reprinted with permission from [44]. Copyright (1993) American Institute of Physics)

growth rates of 5 Å/s were measured at ~507 °C for a 50 Å thick precipitate. Progressive crystallisation of large areas occurred due to the migration, and ultimately, intersection of numerous crystalline needles from a multiplicity of seeds, and the complete crystallisation of a film doped with a dose of 5×10^{15} Ni/cm^2 occurred within 5 min at 569 °C [44]. However, the local crystallisation process was essentially one-dimensional along the extending length of the needle-like grains, and with much slower lateral growth of the crystallite width, driven by SPC alone. A UV reflectance study of the change in crystallinity of a Ni doped, 40 nm thick a-Si film, following annealing at 550 °C, showed a two-stage process, in which ~85 % crystallinity was rapidly achieved in ~4–5 h by the SMC process, but a further 100 h was needed to achieve 99 % crystallinity [46]. This slow, second stage of the process was attributed to the solid phase crystallisation of residual a-Si regions, which had remained between the needle-like grains. The activation energy of this latter process was 3.0 eV, which is consistent with the SPC process [16]. In contrast to the high activation energy for the SPC process, the activation energy for the Ni MIC process has been quoted to be 1.5–1.75 eV [43].

A variety of techniques have been used to introduce Ni into a-Si films, and these have included thin metal film deposition, co-sputtering of Ni and Si, ion implantation of nickel [46], and spin-coating of a nickel-containing pre-cursor solution [47], or localised ink-jet printing of Ni containing droplets [48]. By and large, these samples were then used for low temperature SMC over the temperature range 500–600 °C. However, one feature consistently seen in MIC TFTs was a high leakage current, which was initially attributed to Ni contamination of the poly-Si. The qualitative relationship between poly-Si quality and Ni contamination

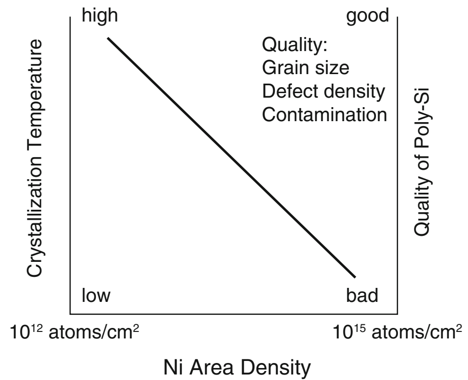

Fig. 7.16 Illustration of the relationship between Ni areal density, MIC crystallisation temperature and the resulting poly-Si quality. (Reprinted from [43] with permission of Springer SBM)

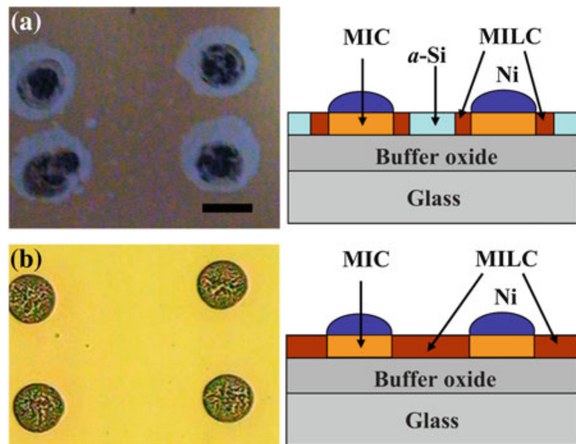

Fig. 7.17 MILC of a-Si using ink-jet printed Ni *dots* (**a**) partial inter-dot crystallisation after 2 h at 580 °C, and (**b**) full crystallisation after 6 h at 580 °C. (Reprinted with permission from [48]. Copyright (2009) American Institute of Physics)

is summarised by the plot in Fig. 7.16, which also illustrates the dependence of the crystallisation temperature on the concentration of nickel [43].

In view of the issue of Ni contamination in MIC material, there has been considerable interest in metal induced lateral crystallisation, MILC, in which the $NiSi_2$ precipitates migrate from localised Ni-doped areas into the adjacent, undoped material and crystallise this [47–51]. Optical photographs of this process are shown in Fig. 7.17a and b, in which a matrix of 80 μm diameter nickel nitrate dots had been ink-jet printed onto an a-Si film and heated at 580 °C for 2 and 6 h, respectively [48]. The lighter area around the Ni dots in Fig. 7.17a shows the extent of the lateral crystallisation beyond the dots after 2 h, and complete crystallisation after 6 h is shown in Fig. 7.17b. The two situations are illustrated schematically in the accompanying line drawings. Although lateral crystallisation can be used to reduce the level of direct Ni contamination in the poly-Si, it does not eliminate it completely. SIMS measurements have shown a 100-times reduction of the Ni concentrations in MILC areas compared with the MIC areas, but only a 10-times reduction in the precipitate areas at the head of the crystallisation front [50].

7.2.4.2 SMC Poly-Si TFTs

A survey of MIC and MILC poly-Si TFTs, fabricated within the temperature range 500–600 °C, showed that the majority of devices had electron field effect mobilities between ~70 and ~100 cm^2/Vs [43], which is higher than achieved with conventional SPC, but lower than with ELA. Also, the leakage currents of the SMC TFTs were higher than in good quality ELA material, typically being within the range of 1–100 × 10^{-12} A/μm (of channel width) for SMC TFTs, but ~2 × 10^{-14} A/μm for ELA TFTs (when measured at 5–10 V drain bias) [52]. However, direct comparisons between different publications are not straightforward due to the use of different measurement biases and different gate oxide thicknesses. Both of these parameters determine the drain field, and, as discussed in Chap. 8, the TFT leakage current, at high drain fields, is exponentially dependent upon the electrostatic field at the drain. Hence, the most useful comparisons are those made in the same publication. Nevertheless, the figure of ~2 × 10^{-14} A/μm quoted for ELA TFTs makes a good reference point when assessing SMC TFTs. The role of Ni contamination was highlighted when comparing MIC and MILC TFTs, with values of 8.8 × 10^{-12} A/µm and 3.6 × 10^{-13} A/μm, respectively, measured at 1 V drain bias [49]. Although the MILC device had ~20 times lower leakage current than the MIC device, it was still more than 10 times higher than an ELA device. However, for Ni concentrations below ~2.5 × 10^{19} cm^{-3}, in MIC devices, the leakage current of ~2 × 10^{-12} A/μm was independent of the Ni doping level [46], suggesting contributory factors, other than metal contamination, to the leakage current, including the crystal structure.

Other authors have clarified the role of the local grain and grain boundary structures in MILC TFTs, where a continuous grain boundary has been identified at the MIC/MILC boundary, as shown in Fig. 7.18a, and a further major grain boundary has been identified when two MILC fronts meet [51]. Where these boundaries are perpendicular to current flow, and are located in the channel or at the source or drain junctions, they can be expected to degrade device behaviour. There are, thus, a variety of device configurations, with respect to these grain boundaries, determined by their relative locations, as shown in Fig. 7.18b. The device location represented by '111' encompasses all three boundaries (where the MIC regions have also been used for the source and drain regions), and '000' encompasses just the MILC material itself. Figure 7.19 shows the device structures used to engineer these two situations, where, in Fig. 7.19a, the Ni seeding region was offset from the ultimate location of the source junction, and MILC growth was unidirectional in the channel area. In Fig. 7.19b, the MIC/MILC junctions were coincident with the source and drain junctions, and the bi-directional MILC fronts met in the centre of the channel. The resulting n-channel TFT characteristics are shown in Fig. 7.20, and, interestingly, the mid-channel continuous GB had only a minor effect upon the electron mobility, by reducing it from 78 to 70 cm^2/Vs, whereas the minimum leakage current, at $V_d = 5$ V, for the '111' TFT was 3 × 10^{-11} A/μm compared with 2 × 10^{-12} A/μm for the '000' TFT [51]. Hence, the continuous GBs at the junction boundaries had a strong

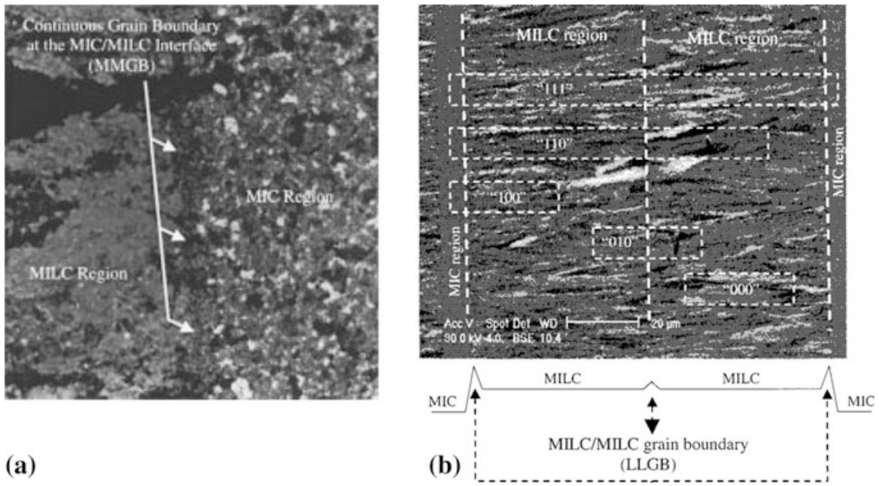

Fig. 7.18 **a** Plan-view TEM micrograph showing the continuous grain boundary at the MIC/MILC boundary, and **b** optical micrograph of MIC and MILC regions, where the numbered areas show the device locations within the material. (Reprinted from [51] with permission of IEEE)

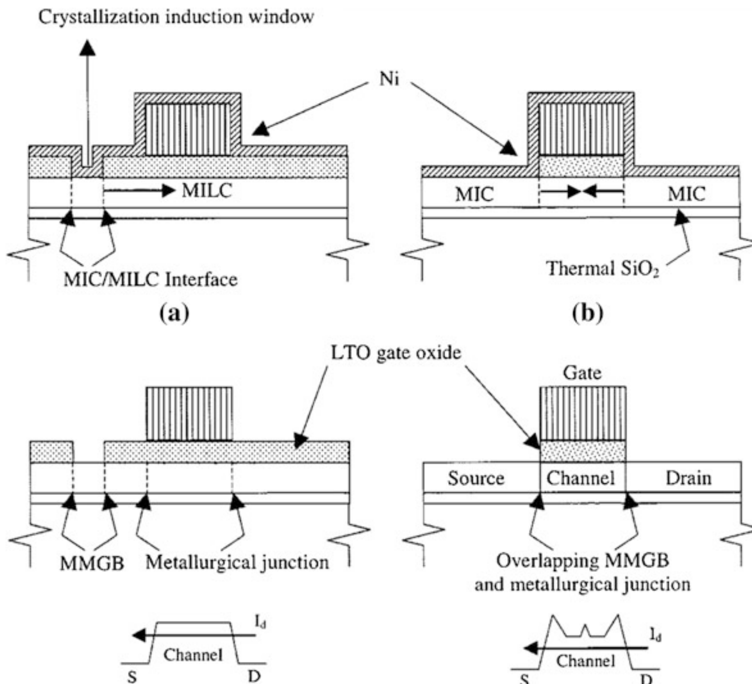

Fig. 7.19 Illustration of device and grain boundary locations within (**a**) a unilateral MILC TFT and (**b**) a MIC/MILC TFT. (Reprinted from [51] with permission of IEEE)

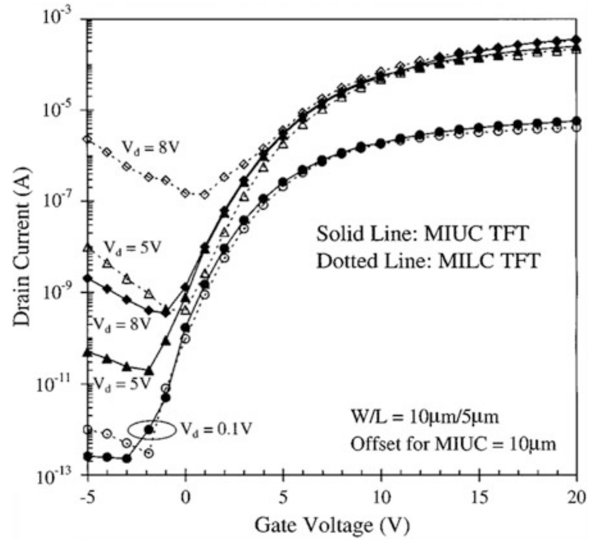

Fig. 7.20 Transfer characteristics obtained from unilateral MILC (MIUC) and MIC/MILC TFTs (see Fig. 7.19a and b, respectively). (Reprinted from [51] with permission of IEEE)

degrading effect upon the leakage current, but, even in their absence, the leakage current still remained high in the '000' device compared with ELA TFTs.

This again points to fundamental aspects of the grain structure, and not just Ni contamination or continuous grain boundaries, being responsible for high leakage currents in SMC TFTs. In confirmation of this, the only SMC devices with substantially lowered leakage currents were those in which the crystal structure was changed by a further process, such as excimer laser annealing. One example of this was with a process referred to as L-MIC [53], in which the samples used for post-MIC ELA had originally been implanted with 5×10^{13} Ni/cm^2, and then annealed at 550 °C to achieve >90 % crystallinity. These samples had typical MIC characteristics, with an electron mobility of ~85 cm^2/Vs, and a minimum leakage current at $V_d = 5$ V of 2.5×10^{-12} A/μm. Following a subsequent 7-shot ELA process, the changes in electron mobility and leakage current are shown in Fig. 7.21, from which it will be seen that the minimum leakage current density was reduced to 2.5×10^{-14} A/μm, and the electron mobility increased to ~210 cm^2/Vs [53]. In addition, the electron mobility results were obtained within an energy density window of ~70 mJ/cm^2, which is much larger than obtained from the conventional ELA process (see Fig. 7.13 for a comparison with a conventional 10-shot ELA process), and the low leakage current could be obtained with as few as two shots with L-MIC process. The explanation for these results was that in the near-melt-through SLG regime, un-melted MIC grains at the bottom of the film seeded the re-growth, and this process also crystallised any residual a-Si regions, which had remained between the MIC grains [53].

Other groups have also employed a process comparable to L-MIC, to produce high performance TFTs, using a process referred to as continuous-grain-silicon (or CGS) [54, 55]. This implemented a MIC process in 45 nm thick films of a-Si,

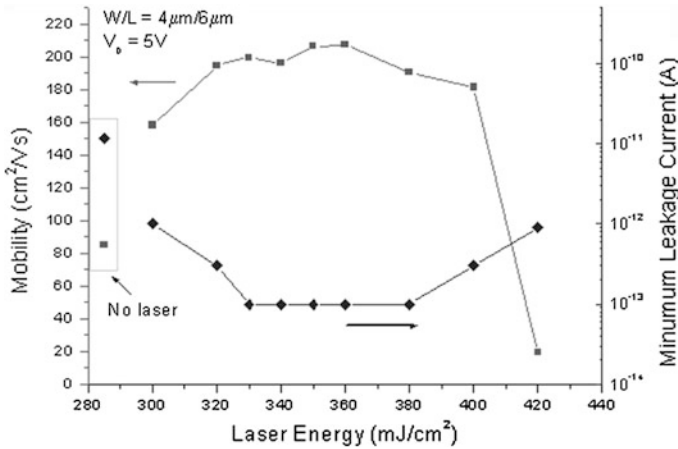

Fig. 7.21 Changes in electron mobility and TFT leakage current as a function of post-MIC ELA, using a 7-shot process. (Reprinted from [53] with permission of IEEE)

using a spin-on solution of Ni in acetic acid, and a crystallisation stage, which was carried out below 550 °C. Following the Ni-mediated crystallisation, the samples were passed through an ELA process to improve the crystal quality of the layer, and self-aligned TFTs were then made using thermally activated boron and phosphorus ion doping for the source and drain regions of p- and n-channel poly-Si TFTs, respectively. (A general discussion of poly-Si architecture and processing can be found in Sect. 7.4). The thermal activation of the phosphorus-doped regions was also described as a gettering process, which reduced the Ni content in the TFT channels. These devices were compared with ELA TFTs, in which the MIC stage had been omitted, and the CGS and ELA TFTs showed electron mobilities of 320 and 115 cm^2/Vs, respectively, and identical, low leakage currents of 5×10^{-14} A/μm (at $V_d = 1$ V) [55].

These results are comparable to the L-MIC work [53], in which the electron mobilities were higher than in conventional ELA TFTs. To clarify the differences between CGS and ELA material, the grain structures were compared by electron backscatter diffraction pattern (EBSP) analysis and by transmission electron microscopy [55]. The EBSP measurements for CGS material, within 10 μm $\times$ 20 μm sampling areas, showed that, at a pitch of 200 nm, the point-to-point changes in mis-orientation angles were just a few degrees. Whereas for a 2 μm $\times$ 2 μm area of ELA material, 30 nm point-to-point measurements gave abrupt changes of mis-orientation angle by 30–60° between grains, but was nearly zero within the grains. The absence of these large changes in the CGS material led to the identification of 7–15 μm sized ‘domains’, within which the misorientations were <5°. No such domains were identified in the ELA material, just individual grains in the size range 0.2–0.5 μm. In the CGS material, [111] planes dominated the crystal orientation normal to the sample surface, which was consistent with the $< 111 >$ preferred crystallisation direction of the $NiSi_2$ precipitates.

TEM analysis confirmed the sharp grain boundaries between the ELA grains, but, for the CGS material, the grains were larger than 1 μm, and were frequently separated by low angle grain boundaries. These fundamental differences between the grain structure of CGS and ELA material, with the large CGS 'domains' containing only low-angle grain boundaries, suggest reduced grain boundary scattering, explaining the higher carrier mobilities. It is also clear that the crystallographic nature of this material, even after the ELA treatment, contains a grain structure strongly influenced by the original Ni-mediated crystallisation process.

In summary, the SMC process was originally investigated as a low cost, and simpler, alternative to conventional ELA, but, for reasons still not fully clarified, the resulting poly-Si TFTs suffered from unacceptably high leakage currents. However, when combined with an ELA process, the leakage current issues were resolved, and higher performance TFTs, than from ELA alone, were fabricated [52–55]. Moreover, as shown in some of this work [53], this could be achieved with a low-shot ELA process and a large process window.

7.3 Gate Dielectrics

The preferred gate dielectric for poly-Si TFTs is silicon dioxide, as it is for single crystal Si devices, in contrast to the use of silicon nitride, which is preferred for a-Si:H TFTs. As discussed in Chap. 5, the preference for a-SiN_x:H in a-Si:H TFTs is determined by the meta-stability of this material and the reduced DOS resulting from the positive charge in the nitride. For poly-Si, these meta-stability considerations do not apply, and the positive charges in the nitride cause unnecessarily large negative shifts in threshold voltage; in addition, the nitride itself is also susceptible to gate bias induced trapping instabilities. These reasons also militate against the use of Si_3N_4 in MOSFET devices. In the following section, the use of SiO_2 as a gate dielectric is discussed, and there is a brief review of alternative dielectrics in Sect. 7.3.2.

7.3.1 Silicon Dioxide

The quality of the gate oxide in a TFT is crucial to the performance of the device, and the oxide needs to have low leakage current, low densities of fixed charges and interface states, high breakdown field, low pin-hole density, and good bias-stress stability. Moreover, for the low temperature TFTs of interest in this book, the oxide deposition process must be implementable below the glass softening point, and, for practical purposes in commercial processing, this means below $\sim$450 °C, and, finally, over large areas with good uniformity. The temperature constraint rules out the thermally grown oxide, which has underpinned the crystalline silicon integrated circuit industry. Nevertheless, the properties of thermal oxides have

been widely used as a benchmark against which to measure TFT oxides, and the closer these properties have matched the better has been the performance of the low temperature oxides. The correlation of electrical properties, such as the density of states at the Si/SiO_2 interface, can be readily understood, but even mechanical properties such as the etch rate in hydrofluoric acid is a good indicator of the density of the film [56], and this density has been correlated with the films porosity and its propensity to absorb water [57]. Furthermore, this porosity has been associated with gate-bias-stress induced threshold voltage instability in the TFT, due to the motion of adsorbed H^+ and OH^- ions in the oxide [58]. Hence, a number of simple measurements have been used to screen potential oxide candidates.

A powerful technique for the assessment of the porosity of the film, and its water content, has been thermal desorption spectroscopy (TDS), [57], in which, as the temperature of the film is steadily raised, the desorbed gases from the film are analysed in a mass spectrometer, set to atomic mass 18, to detect water. The TDS plots in Fig. 7.22 were obtained from films deposited by PECVD from TEOS (tetraethylorthosilicate) and O_2 in helium carrier gas, and show three characteristic water desorption peaks obtained from SiO_2 films. The two low temperature peaks at 100–200 and 150–300 °C have been associated with adsorbed water at room temperature in porous films. This was confirmed by noting that the heights of these peaks could be increased by prolonged air exposure at room temperature, and decreased by vacuum annealing at elevated temperatures. Hence, dense, low porosity films should show minimal desorption peaks at these two temperatures. The high temperature peak at 350–650 °C was associated with isolated silanol, Si–OH, bonds formed during film growth, and, unlike the lower temperature peaks, was seen in all high quality oxides. As will also be seen from Fig. 7.22, the overall peak heights were determined by the TEOS + He/O_2 flow ratios, and the highest oxygen dilution ratio led to the densest and least porous film.

In addition to the use of TEOS and O_2 gas mixtures in PECVD reactors [57, 59], SiO_2 depositions can also be obtained from SiH_4 and N_2O gas mixtures [42, 60, 61].

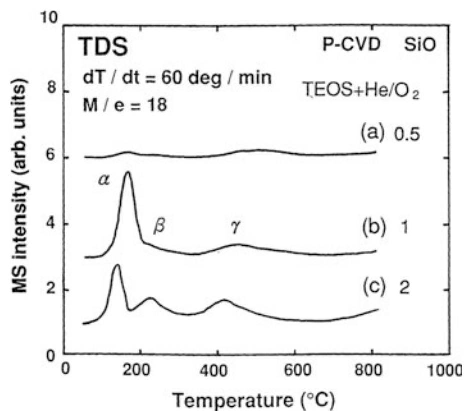

Fig. 7.22 Thermal desorption spectra (TDS) measured on PECVD TEOS films of SiO_2, deposited with different levels of TEOS + He:O_2 dilution. (Reprinted with permission from [57]. Copyright (1993) The Japan Society of Applied Physics)

These PECVD depositions at 300–400 °C are typically carried out in parallel plate reactors operating at 13.56 MHz, or 27 MHz, and, given the large area capabilities of these reactors [59], PECVD deposition is the mainstream technique used for the deposition of high quality gate oxides for poly-Si TFTs. As mentioned above, the highest quality oxides have been obtained at low growth rates, which were achieved by a large dilution of the silicon bearing gases by using high volumes of either oxygen or helium carrier gas [56, 57, 60, 61].

Other oxides, which have been examined as possible gate dielectrics in poly-Si TFTs, have included deposition by:

- APCVD from SiH_4, and O_2 [58],
- remote plasma, RPCVD, from SiH_4, O_2 and He at 300–350 °C [62],
- ECR-CVD at 2.45 GHz from SiH_4, O_2 and He at 25–270 °C [63, 64].

Comparative TDS measurements from some of these low temperature oxides are shown in Fig. 23a [61] and b [65], and it will be seen from Fig. 7.23a that only the helium-diluted SiH_4/N_2O films deposited at 250–300 °C showed low porosity, which also correlated well with an etch rate comparable to thermal SiO_2 [60]. Hence, the minimum deposition temperature for this oxide is above 250 °C, which is not a problem for TFTs on glass, but is an issue for TFTs on low-temperature polymer substrates. However, low-deposition-temperature ECR oxides were of high density and low porosity, and are possible candidates for poly-Si TFTs on polymer substrates [64]. This topic is discussed further in Chap. 11. The TEOS oxides in Fig. 7.23b were deposited above 300 °C with high O_2 dilution ratios, and compare well, in terms of low porosity, with the helium diluted SiH_4/N_2O reference sample, and are widely used in state-of-the-art TFT processing. The APCVD oxides in Fig. 7.23a show large, low temperature desorption peaks, which, as mentioned above, have been correlated with gate bias instability in TFTs [58], and these oxides are not compatible with high quality TFTs.

The other essential treatment in producing a device quality oxide is a post-deposition anneal in the temperature range 300–400 °C to reduce both the fixed oxide charge in the film and the interface state density [56, 60, 63, 64]. This is the same as the low temperature hydrogen passivation anneal, used with thermal oxides in MOSFET technology, to reduce both of the above states. Hydrogen containing ambients, such as forming gas, or wet-N_2, are used, and the treatment is frequently carried out after final metallisation, and may be referred to as a post-metal anneal. In the latter case, reducing gate metals, such as aluminium, can react with hydroxyls in the film releasing hydrogen even in an inert annealing ambient such as N_2. In order to avoid the problem of separating interface trapping states from trapping states in the poly-Si film itself, the assessment of this treatment is usually carried out by C–V measurements of the film deposited onto a lightly doped silicon substrate. Figure 7.24 demonstrates the effectiveness of a forming gas anneal at 400 °C on a dense, helium diluted SiH_4/N_2O oxide deposited at 350 °C, in which the positive charge density in the oxide was reduced from $\sim 8 \times 10^{11}$ to $\sim 2.5 \times 10^{11}$ cm^{-2}, and the near-mid-gap interface density was reduced from $\sim 1 \times 10^{12}$ to $\sim 4 \times 10^{10}$ cm^{-2}eV^{-1} [56].

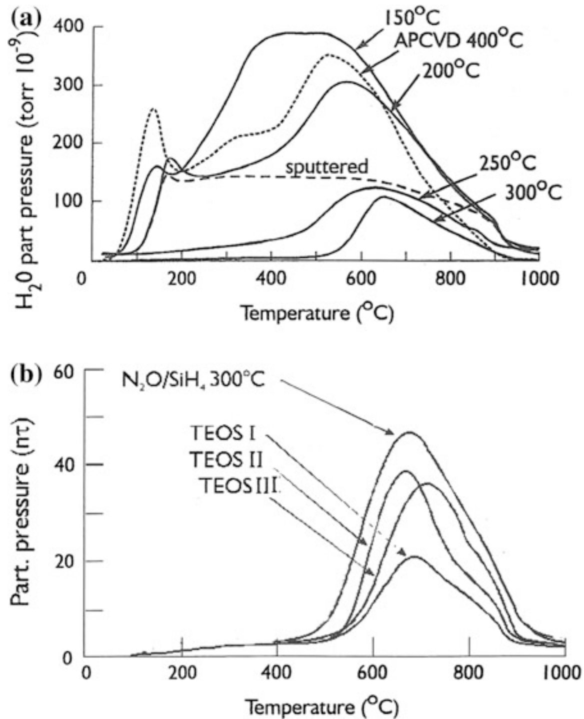

Fig. 7.23 TDS spectra of SiO_2 films (**a**) by PECVD deposition using He-diluted SiH_4/N_2O gases at different temperatures, plus an APCVD film and a sputtered film (Reprinted from [61] with permission of SID), and (**b**) various PECVD O_2-diluted TEOS films together with a reference He-diluted SiH_4/N_2O film (unpublished data from Dr N D Young of Philips Research)

Whilst the above post-deposition anneal is extensively used, various other post-deposition annealing regimes have been reported as leading to an improvement in oxide quality, such as an excimer laser anneal, at an energy below the silicon melt-threshold, which led to improvements in carrier mobility, oxide charge density and gate bias and drain bias stress stability [66]. Another procedure giving similar results was a high-pressure water vapour anneal at 1.3 Mpa and 260 °C [67]. However, it is not clear that these, or other techniques, have achieved widespread

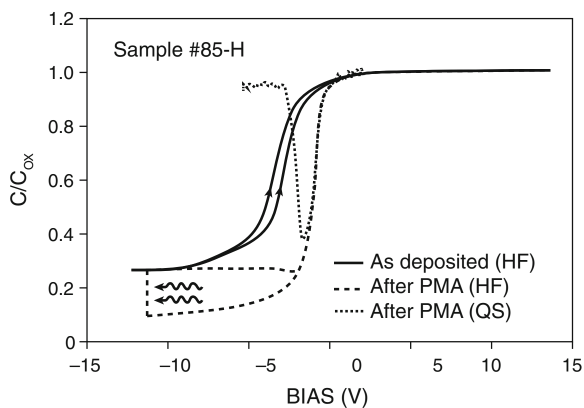

Fig. 7.24 MOS high frequency and quasi-static C–V measurements on a 350 °C PECVD He-diluted SiH_4/N_2O SiO_2 film, before and after a post-metallisation anneal, PMA, at 400 °C for 30 min. (Reprinted with permission from [56]. Copyright (1986) American Institute of Physics)

application. Moreover, there is always a cost consideration in implementing a more complex processing schedule, which needs to be balanced against the level of improvements which might be achieved when applied to the current state-of-the-art high performance TFT process.

In terms of basic dielectric properties, the dense, helium diluted SiH_4/N_2O oxides display a high breakdown field of ~8 MV/cm, as shown by the large area (5.2×10^{-3} cm^2) capacitor results obtained from single crystal Si substrates [56], and by the large area poly-Si TFTs (W = L = 100 μm) in Fig. 25a and b, respectively. The latter results demonstrate a thickness independent breakdown field, which is important for short channel TFTs, where the gate oxide thickness needs to be scaled down with reducing channel length in order to suppress short channel effects. The use of SiO_2 films down to 20 nm thickness is demonstrated in this data, but at 10 nm thickness premature breakdown was observed, indicating the current limit of oxide thickness scaling. This probably results from a combination of the rough poly-Si surface, giving poor film integrity at this thickness, as well as step coverage problems over the edges of the poly-Si islands. In the following section, some alternative dielectric strategies are discussed for thin oxides.

In addition to the gate dielectric application, high quality oxides are also needed for interlayer dielectrics separating different levels of metallisation, such as the gate and drain layers, and also for capping the glass substrates. The capping layer has the double purpose of providing an electronically well-controlled layer at the back interface of the TFT, as well as acting as a diffusion barrier to alkali ions

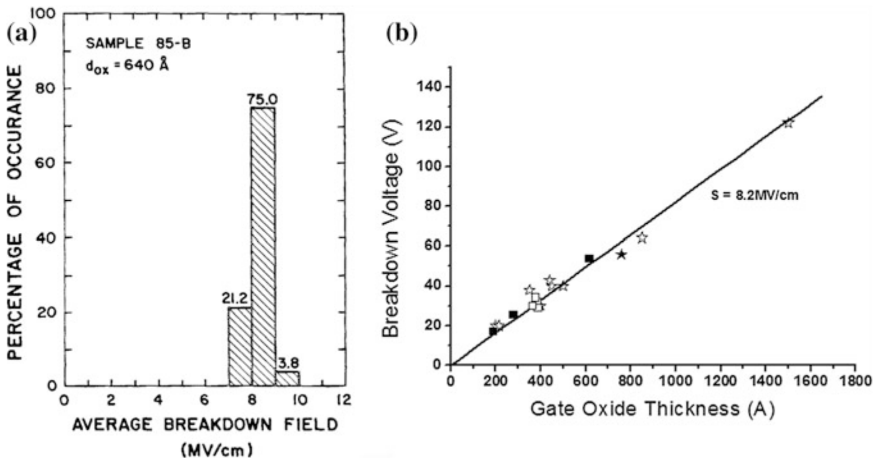

Fig. 7.25 Electro-static breakdown measurements on He-diluted SiH_4/N_2O SiO_2 films (**a**) breakdown field of large area capacitors of 64 nm thick films on c-Si substrates (Reprinted with permission from [56]. Copyright (1986) American Institute of Physics), and (**b**) breakdown voltage measurements as a function of SiO_2 film thickness in poly-Si TFTs (Reprinted from [76] with permission of SID)

from the substrate. In fact, for the latter purpose, it is common to deposit SiN directly onto the glass surfaces, as it is a better diffusion barrier than SiO_2, and then to cap this with SiO_2. Typical thicknesses for these two layers are 100 nm SiN and 400 nm SiO_2.

7.3.2 Alternative Dielectrics

In sub-0.1micron channel length MOSFETs, the scaling of gate oxide thickness has resulted in ultra thin SiO_2 films of <15 Å, where leakage current and reliability concerns have become important issues. This has led to the study of high-k dielectrics [68] as a way to use thicker films, whilst still maintaining the same equivalent oxide thickness, EOT, and, hence, the same g_m. There have not been the same fundamental issues with the SiO_2 layers used in poly-Si TFTs, but, as discussed in the previous section, a limit has been identified in the minimum thickness of SiO_2, which can be reliably used, and some investigations have been reported on the use of higher-k dielectrics for this TFT application. The dielectric constant of SiO_2 is 3.9, and the two alternative dielectrics were PECVD a-SiN_x:H ($k = 6.5$) [69] and sputtered Ta_2O_5 ($k = 11$–25) [70]. (The dielectric constant for bulk Ta_2O_5 is 25, but the thin film layers only gave a value of 11.) In both cases, a dual dielectric approach was followed, in which a thin layer of SiO_2 was used as an interfacial layer between the poly-Si and the high-k dielectric. This process was adopted in order to maintain the electronic quality of the poly-Si/SiO_2 interface.

For the dual dielectric system, the EOT is given by:

$$EOT = t_{SiO_2} + \frac{3.9t_2}{k_2}$$

where t_2 and k_2 are the thickness and dielectric constant of the high-k layer, respectively.

The p- and n-channel devices made with the a-SiN_x:H/SiO_2 dielectric contained either 5 nm or 10 nm thick layers of SiO_2, and gave good TFT characteristics down to an EOT of 9.8 nm. The device parameters such as mobility, breakdown field and drain bias stability were largely independent of the SiO_2 layer thickness [69], and this dielectric combination is a plausible route to thin oxide TFTs with an EOT at least down to 10 nm.

The TFTs with the SiO_2/Ta_2O_5 gate dielectric had a minimum EOT of 46 nm, and needed several hours post-metallisation annealing, at 350 °C in mixed gas, to achieve low threshold voltages and high carrier mobilities [70], indicating the need for further optimisation of this higher-k system in order to achieve an acceptable combination of TFT performance and processing schedule.

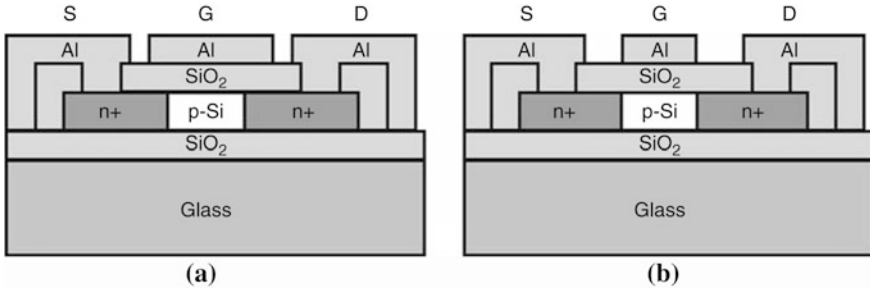

Fig. 7.26 Schematic cross-sections of n-channel, top-gated poly-Si TFTs (**a**) non-self-aligned architecture, and (**b**) self-aligned

7.4 Poly-Si TFT Architecture and Fabrication

7.4.1 Architecture

Poly-Si TFTs are most commonly implemented as top-gated structures, as shown in Fig. 7.26a and b for non-self-aligned (NSA) and self-aligned (SA) devices, respectively. As will be seen, this is a different architecture from the inverted staggered architecture of a-Si:H TFTs (see Chap. 5), and is much more similar to the architecture of single crystal silicon-on-insulator (SOI) MOSFETs. Further points of similarity with the SOI MOSFETs, and distinction from a-Si:H TFTs and emerging TFT processes in organic or amorphous oxide materials, are that both n-channel and p-channel poly-Si TFTs, with comparable performance, can be fabricated with a common process. Secondly, the source and drain doping is usually accomplished using ion shower doping of boron for p-channel TFTs and phosphorus for n-channel TFTs. This process has a number of similarities to ion implantation for MOSFETs, in that both involve the high-dose implantation of selected ions. In other words, the architecture and a key fabrication stage of poly-Si TFTs are closer to MOSFETs than to devices fabricated in other thin film materials. However, this high-dose ion doping process is potentially damaging to the crystallographic order of the poly-Si film, particularly for the heavier phosphorus ion compared with boron. The degree of damage will be determined by the ion dose, ion energy and substrate temperature, and, it has been shown that, for high enough doses into single crystal silicon, the damage can be sufficient to cause complete amorphisation of the implanted layer [71]. This is also an issue in poly-Si, and is discussed further in Sect. 7.4.1.1.

The essential difference between the two architectures in Fig. 7.26 relates to the formation of the source and drain regions, and this determines the overlap of the gate electrode across these regions. For the NSA structure, with significant overlap, the source and drain regions can be ion doped prior to the crystallisation of the film, and the dopants in these regions will then be activated during film crystallisation. This process can be implemented with direct ion doping into bare a-Si,

and results in a high level of dopant activation, with minimal residual ion damage. A doping process employing a phosphorus dose of 1×10^{15} cm^2 at 10 keV, typically gives a doped region sheet resistance of $\sim$300 ohms/square. Subsequent to this stage, the gate dielectric is deposited and defined, followed by gate, drain and source metal deposition and definition. The overlap between the gate metal and the doped source and drain regions is determined by the alignment rules for the process, and is likely to be up to $\sim 3\mu$m. This is a simple and robust fabrication procedure, and is well suited to the basic study of material parameters (as described in Sect. 7.2), but the architecture suffers from larger parasitic gate-drain capacitance, which will degrade high frequency transistor performance. In addition, it is not well suited to the fabrication of shorter channel devices ($L < 3\mu$m) due to alignment issues, and the possibility of uncontrolled channel shortening due to lateral diffusion of the source and drain dopant during the laser crystallisation stage.

The above limitations are removed with the SA architecture, but, in several respects, it results in a more complex fabrication process, primarily associated with the source and drain doping stage, which is discussed in the following section.

7.4.1.1 Self Aligned Source and Drain Doping

The self-alignment between the edges of the gate and the edges of the source and drain regions is achieved by using the gate electrode as an ion doping mask during the doping stage, which means that the dopants are implanted through the gate dielectric. In order to penetrate this layer, the doses and energies will be larger than those used for the NSA TFTs. Furthermore, as the doping occurs after the transistor channel layer has been crystallised, a further processing stage has to be introduced to activate the dopant: this can be either a second pass through the laser or a thermal activation process in a furnace, or by rapid thermal annealing, RTA. For the furnace process, the constraints imposed by the glass substrate dictate a low thermal budget, such as a few hours at a maximum temperature of 450 °C, and relies upon the re-growth of the ion-damaged film being seeded by an undamaged poly-Si layer at the bottom of the film. Hence, to ensure this seeding, full film amorphisation must be avoided, otherwise the thermal budget will increase to the values quoted in Sect. 7.2.1 for the SPC process. As mentioned above, amorphisation is a more serious issue with the heavy phosphorus ions, and the effects discussed below were not seen with boron doping for p-channel TFTs. Figure 7.27 shows the variation of poly-Si sheet resistance as a function of phosphorus ion dose, and compares laser and furnace activation. With laser activation, the sheet resistance varied inversely with phosphorus dose, as would be expected, but, with furnace activation at 450 °C, this was only seen at the lower doses. At the higher doses, the sheet resistance began to increase with dose and, at the highest dose, it was above the measurement limit of 1×10^6 ohm/square. A broader data set showed that there was a critical combination of ion energies and doses [72], above which thermal activation at 450 °C was ineffective. This was confirmed to be due

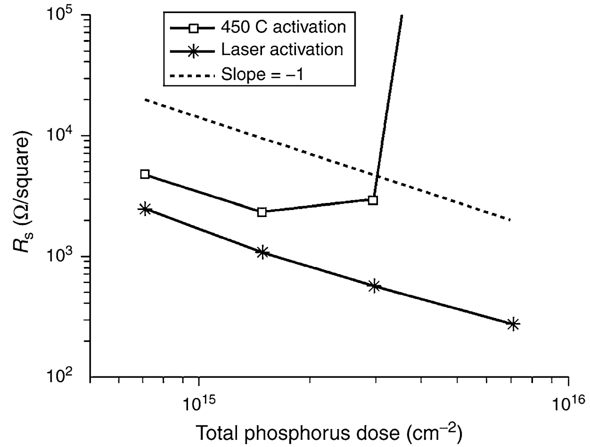

Fig. 7.27 Variation of sheet resistance of phosphorus implanted poly-Si as a function of dose and activation method (80 keV implant through 145 nm of SiO_2)

to film amorphisation, since doses, which could not be activated in 40 nm thick films, could be activated in 80 nm thick films. Finally, it should be noted that even where furnace activation was achieved, it resulted in a higher sheet resistance than obtained with laser activation. This is likely to be due to lower dopant solubility at the lower temperature. Hence, from the standpoint of comparing phosphorus activation, the 450 °C process resulted in higher sheet resistance and a smaller useable dose range than laser activation. A similar difference in the sheet resistance between laser activated and thermally activated regions was also found when higher temperature rapid thermal annealing was used instead of a 450 °C furnace process [73].

Further issues in the SA doping process are revealed when the resulting TFT transfer characteristics, processed with furnace or laser activation, are compared in Fig. 7.28 [72]. One obvious feature in these curves, and in other publications [74, 75], is the higher minimum leakage current in the laser-activated n-channel TFTs, which is due to residual ion-doping damage at the edge of the drain junction [72, 75]. Cross-sectional TEM of a more heavily phosphorus-implanted sample showed a 200 nm wide residual amorphous region, located in the doped region near the gate edge, and also extending beneath the gate [34] (due to lateral end-of-range damage not exposed to the laser). Very similar results have been reported in arsenic doped n-channel TFTs, where the leakage current and TEM-imaged crystallographic damage in the exposed silicon near the gate edge have been correlated with diffraction of the laser beam by the gate edge [75].

Another feature in Fig. 7.28 is the lower on-current in the furnace activated n-channel TFT, due to this activation process giving higher sheet resistance in the source and drain regions, as shown in Fig. 7.27. Finally, the field effect mobility extracted from laser crystallised n-channel TFTs was less than from identically crystallised NSA TFTs [72]. As with the leakage current, this has also been seen in arsenic doped TFTs, and, again, associated with the diffraction-induced residual damage effects at the gate edge [75]. This damage can also have a significant

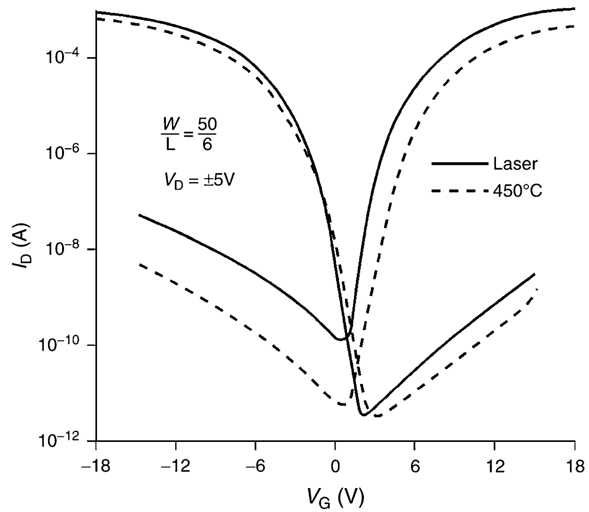

Fig. 7.28 Transfer characteristics of self-aligned n- and p-channel poly-Si TFTs, showing the influence of laser or furnace dopant activation. (Reprinted with permission from [72]. Copyright (1998), The Electrochemical Society)

impact upon the operation of short channel TFTs [75–77], as shown by the field effect mobility results in Fig. 7.29 [76]. The mobility values in this figure were corrected for the series resistance in the doped regions themselves, and were used to calculate the parasitic resistance specifically induced by the phosphorus ion doping process.

Various techniques have been reported for minimising the general ion doping damage effects in SA n-channel TFTs, including a careful control of ion dose and energy [72]. For the laser activation process, in particular, oblique-incidence laser irradiation has been shown to minimise the gate-edge diffraction [78], and, thereby, reduce the associated damage effects on leakage current and carrier mobility. A technique producing comparable results is the use of an off-set gate, in which the gate length is reduced by lateral etching after ion doping, so that the diffraction and masking effects at the gate edge no longer interfered with the full

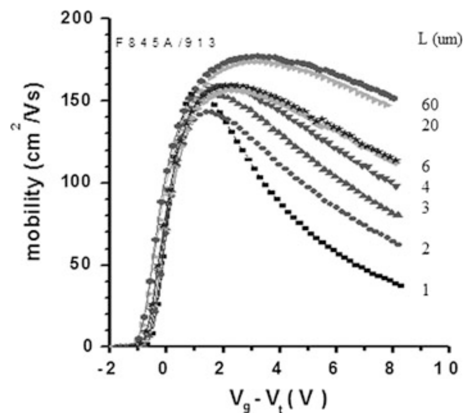

Fig. 7.29 Dependence of electron field effect mobility measurements on channel length, for SA aligned n-channel poly-Si TFTs. (Reprinted from [76] with permission of SID)

melting of the doped region. This can lead to complete damage removal, as shown in Fig. 7.30 by the TFT characteristics of a device with a 0.5 μm off-set gate [34]. The off-set gate is also one of a number of techniques, to be discussed in Sect. 7.4.1.2, for reducing the field at the drain edge, which are used to improve the drain-bias-stress stability of poly-Si TFTs. Finally, laser activation, followed by furnace activation, can be used to reduce the leakage current to the lower value seen in furnace activated TFTs.

As is apparent from the above discussion, the process for fabricating SA TFTs, with minimal performance artefacts, is considerably more complex than the NSA TFT process, and this is the reason for favouring the use of NSA TFTs for basic poly-Si materials studies, such as those presented in Sect. 7.2. However, the potentially superior performance of SA TFTs, due to lower parasitic capacitances, and their better compatibility with sub-micron channel length TFTs makes them the preferred choice for many poly-Si applications.

7.4.1.2 Drain Field Relief

When poly-Si TFTs are exposed to a drain-bias stress, there can be a critical fall-off in performance, as illustrated by the results in Fig. 7.31. The exposure of the device, to a 13 V drain bias for 60 s, led to an increase in off-state current and a reduction in on-state current, as well as a major change in the shape of the output characteristics [79]. This phenomenon has been widely ascribed to hot electron damage [80, 81], and the physics of this process are discussed in Chap. 8, where it is shown that an alteration in device architecture is needed to suppress this instability. The architectural change is one in which the field at the drain/channel

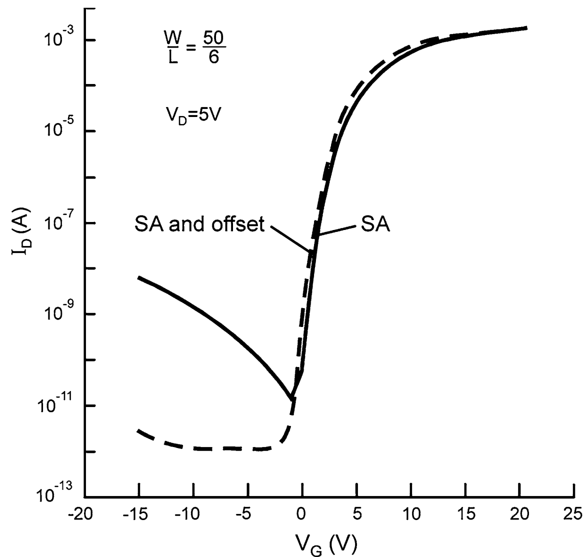

Fig. 7.30 Effect of gate offset in removing the residual ion doping damage from laser activated n-channel SA poly-Si TFTs. (Reproduced with permission from [34])

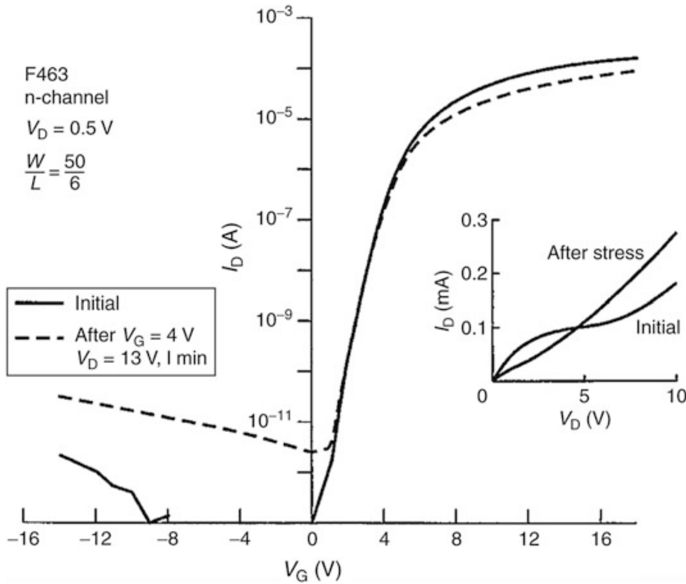

Fig. 7.31 Influence of drain bias stress of 13 V for 60 s on NSA TFT transfer characteristic. The insert shows its effect upon the output characteristic. (Reprinted with permission from [79]. Copyright (1998) The Japan Society of Applied Physics)

junction is reduced, and this is most easily accomplished by the use of lightly doped drain (LDD) regions, as shown schematically in Fig. 7.32a and b. These two figures illustrate two LDD variants, where the lightly doped region is either external to the gate, or is overlapped by the gate (GOLDD). In both cases, an extra masking and processing step is involved to form this region, and, as with the drain region itself, the LDD region is formed by phosphorus ion doping, but with a lower dose in the poly-Si. (It is typically in the range $5 \times 10^{12} – 5 \times 10^{13}$ cm^{-2}, in contrast to the fully doped drain region where the dose is likely to be in the range $5 \times 10^{14} – 1 \times 10^{15}$ cm^{-2}). When the region is defined photo-lithographically, its size will be determined by the process design rules, and is likely to be of the order of 1–3 μm.

The qualitative trade-off with dose is that lower doses will give more field relief, and hence, better stability, but a larger series resistance, and hence, lower on-current. This trade-off is minimised with GOLDD, where the gate modulates the conductivity of the GOLDD region, and it also gives better device stability (see Chap. 8). However, as with the NSA architecture, GOLDD gives greater parasitic capacitances, and is less compatible with short channel length devices.

To obtain sub-micron LDD regions, a non-lithographic definition procedure is required, such as the lateral etch-back of the gate, as used to form the off-set gate. With this technique, the gap can be left undoped, with reliance upon the lateral diffusion of the drain dopant, during a laser activation stage, to dope the LDD region. Alternatively, a low dose implant can be used to deliberately dope the

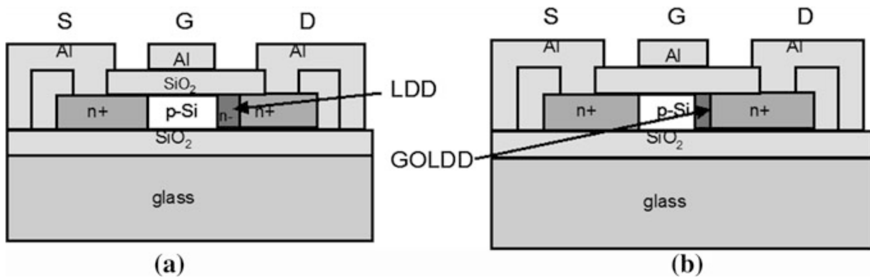

Fig. 7.32 Cross-sectional diagrams of SA poly-Si TFTs showing LDD regions (**a**) conventional LDD, and (**b**) gate overlapped LDD, GOLDD

region [82]. This procedure requires good control of the lateral etching process, because too large a gap will give increasingly large series resistance in the on-state.

A potentially more controllable sub-micron process is to use a sidewall spacer on the gate to define either an undoped off-set gate [83], or a doped LDD region, which can be a GOLDD region if the spacer itself is conducting [84].

7.4.1.3 Other TFT Architectures

Although the top-gated structures discussed above are the most widely used, bottom gated NSA TFTs have been implemented [85]. SA bottom gate TFTs have also been demonstrated by using backside exposure of photoresist on the top of the plate, where the bottom gate acts as an in situ mask to define the channel length [86].

It is also possible to fabricate NSA top-gated TFTs, without using ion doping, by sequentially depositing intrinsic a-Si and n^+ doped a-Si, and removing the n^+ a-Si from the channel region [87]. This is similar to the back-channel-etch process in a-Si:H TFTs (see Sect. 5.3.1). Following the clearance of the channel region, laser crystallisation is used in the normal way on both channel and doped regions, and is followed by gate oxide deposition, contact window opening, and metallisation to complete the TFT fabrication process.

7.4.2 Fabrication Process

Two examples of the poly-Si TFT fabrication process are shown in Figs. 7.33 and 7.34, and these list both the major processing steps and the photolithography stages. The fabrication of a simple NSA n-channel TFT (whose cross-section is in Fig. 7.26a) is listed in Fig. 7.33, and it is a 4-mask process involving the definition of the poly-Si island, the source and drain doping locations, contact window opening through the gate oxide, and definition of the metal contact areas. The SA

1.	Glass plate capping by SiN and SiO_2	
2.	a-Si:H deposition by PECVD	
3.	De-hydrogenation at 400-450°C in N_2	
4.	Poly-Si island definition	M1
5.	Low dose B^+ ion doping	
6.	Source and drain definition, and P^+ ion doping	M2
7.	Laser crystallisation	
8.	Gate oxide deposition by PECVD	
9.	Contact window definition	M3
10.	Source, drain and gate metal deposition and definition	M4
11.	Anneal at 350°C in N_2/H_2 to sinter contacts	

Fig. 7.33 Fabrication stages for non-self-aligned poly-Si n-channel TFTs

n-channel TFT (see Fig. 7.26b) is also a 4-mask process, with island definition, gate metal definition, contact window opening, and source and drain metal definition. These 4-mask process flows are the minimum number of mask stages needed to fabricate a device without field relief. For the fabrication of an AMLCD, with CMOS drive circuits and stable n-channel TFTs, an increase in the number of depositions and mask stages is needed, and a 9-mask process is shown in Fig. 7.34. Compared with the single channel TFTs, the extra stages are separate photolithographic definitions for the source and drain areas for the n- and p-channel TFTs, definition of the LDD area for the n-channel TFTs, contact windows for the ITO pixel electrodes, and the ITO patterning itself.

For both architectures, two other stages are frequently necessary, namely, de-hydrogenation, and low dose B^+ doping, in steps 3 and 5, respectively. The a-Si:H pre-cursor film typically contains ~ 10 % hydrogen, and, if this film is exposed to a top-hat laser beam, there will be an explosive release of hydrogen, causing severe blistering of the film. A low temperature thermal anneal at 400–450 °C is used to reduce the hydrogen content to ~ 1 % or less, at which level the film can be exposed to a top-hat beam without risk of mechanical damage. An alternative to this process is higher temperature deposition of a-Si, giving a lower H-content, or multi-shot irradiations at increasing energy density, to progressively heat the film leading to controlled out-diffusion of the hydrogen [88]. The same effect can also be achieved with a shaped laser beam, in which the leading edge is much less sharp than in the top-hat beam [89]. This leads to more gradual heating of the film over several incrementally higher intensities, giving controlled exo-diffusion of hydrogen before the film is ultimately exposed to the maximum laser beam intensity.

The low dose boron ion doping is used to compensate for an intrinsic electron richness in the crystallised poly-Si film, which is due to a combination of positive charges in the oxides above and below the film, and/or the neutral level of the poly-Si band-gap states being above mid-gap. The net effect of these centres is to shift the threshold voltage of the TFTs in a negative direction. Boron doping is

1.	Glass plate capping by SiN and SiO_2	
2.	a-Si:H deposition by PECVD	
3.	De-hydrogenation at 400-450°C in N_2	
4.	Poly-Si island definition	M1
5.	Low dose B^+ ion doping	
6.	Laser crystallisation	
7.	Gate oxide deposition by PECVD	
8.	Gate metal deposition and definition	M2
9.	LDD definition & P^+ ion doping (n-channel only)	M3
10.	Definition of n-ch source, drain, and P^+ ion doping	M4
11.	Definition of p-ch source, drain, and B^+ ion doping	M5
12.	Dopant activation (laser or furnace)	
13.	Capping oxide deposition	
14.	Contact window definition	M6
15.	Source and drain metal deposition, and definition	M7
16.	Anneal at 350°C in N_2/H_2 to sinter contacts	
17.	Capping oxide deposition	
18.	Contact window definition	M8
19.	ITO deposition and definition	M9

Fig. 7.34 Fabrication stages for a poly-Si AMLCD, containing complementary self-aligned TFTs, and with LDD field relief for the n-channel TFTs

used to compensate this shift, and to achieve symmetrically positioned transfer characteristics of p- and n-channel TFTs either side of $V_G = 0$ V (as seen with the characteristics in Figs. 7.9 and 7.28).

Much of the processing of poly-Si TFTs and AMLCDs can be accomplished with the equipment used for the fabrication of a-Si:H AMLCDs, and this would include plate cleaning, photolithography and etching stages, as well as the deposition of various metals such as aluminium and ITO. Also, the PECVD deposition of the gate oxide and a-Si:H precursor films can be deposited in standard, large area PECVD reactors, using the same deposition conditions as for the a-Si:H TFT films. However, there are also large area PECVD reactors, which can deposit a-Si at temperatures up to ~400–450 °C, and incorporate an in-situ de-hydrogenation anneal, so that the films are ready for laser crystallisation without any further treatment [90]. The additional items of equipment needed for poly-Si TFTs are a laser crystallisation system [18], and a large area ion doping system [91]. The ion doping system will deliver a rectangular (or ribbon-shaped) beam of ions, through which the substrate plates are scanned in a direction parallel to the short axis of the beam. The beam will not have the high-resolution mass-separation of a semiconductor industry ion implanter, but will have sufficient ion mass filtering to ensure that hydrogen is excluded from the beam, that phosphorus and boron cross-contamination is avoided, and that for a phosphorus doping stage, say, only P^+ ions are selected, whilst other species such as P_2^+ are removed. (The original ion doping systems lacked these refinements.) The other item of equipment, which

might be employed, is a high-resolution photolithography station, if short channel TFTs are used for the addressing circuits. These will need higher resolution than the 3μm typically available with the large area LCD-industry aligners.

7.5 Advanced Processing

7.5.1 Large Grain Poly-Si

As discussed above, the conventional ELA technique produces devices with limited electron mobility (<200 cm^2/Vs), limited throughput and a small laser processing energy window. Various techniques have been explored to address some of these problems, with one aim also being larger grain poly-Si, giving higher carrier mobility. These techniques have included both solid state green lasers, as well as modified excimer laser crystallisation procedures. The modified excimer laser procedures include sequential lateral solidification (SLS) [29, 92–94], phase modulated excimer laser annealing, PMELA [1, 95–97], and a micro-Czochralski process, μ-Cz, for location controlled single grain growth [98, 99]. In all these cases, a technique has been developed to control and extend lateral grain growth during the SLG process, rather than relying upon the random process, which occurs during conventional ELA. These techniques are discussed in Sect. 7.5.2.

As briefly discussed in Sect. 7.2.3, solid state green lasers have been advocated to overcome some of the technical and cost of ownership issues with ELA, as well as being able to produce large grain material [35–42], and these approaches are presented in Sect. 7.5.3. Finally, a comparison is made between the excimer and green laser approaches in Sect. 7.5.4.

7.5.2 Modified Excimer Laser Crystallisation

The SLS and PMELA techniques are conceptually similar in that both procedures expose the substrate to a spatial intensity fluctuation, varying from a below-melt-threshold intensity to a value high enough to fully melt the silicon film. At the boundary between these two regions, there will be a portion of material which will experience near-melt-through conditions, where the normal SLG process will occur. Those grains seed lateral growth into the adjacent fully molten regimes, giving grain growth of a few microns or more. SLS directly achieves the intensity fluctuation by passing the laser beam through a projection mask, containing alternate clear and occluded regions. With PMELA, the laser beam is passed through a phase shifting mask, so that optical interference in the emergent beam produces the required intensity fluctuation. However, the implementation is different, with SLS using a multi-shot scanning procedure to promote grain

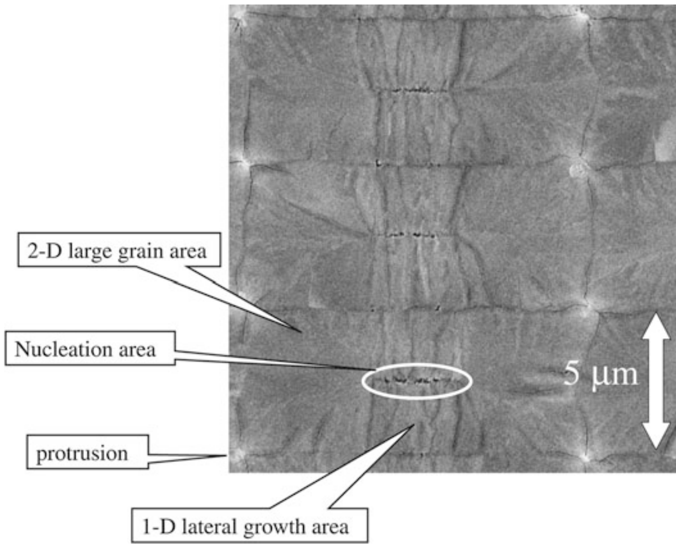

Fig. 7.35 SEM micrograph of location-controlled large grain arrays grown by PMELA. (Reprinted with permission from [96]. Copyright (2008) The Japan Society of Applied Physics)

propagation, whereas PMELA uses a single shot technique to produce an array of location controlled large-grain (or single crystal) areas, typically 5 μm square, as shown in Fig. 7.35 [96]. The SEM micrograph shows a combination of large grain areas, lateral growth areas plus the nucleation area. To achieve this well defined, location-controlled grain structure, with a robust fabrication process, the phase shift mask has evolved from its original, simple form, of etched depressions in a quartz plate [95], to a complex matrix of variably sized pits and humps on the quartz plate, which is referred to as a 2-dimensional bipolar phase modulator plate, 2-D BPM [96, 97].

The large grains from the SLS and PMELA processes yielded high electron mobility values of up to ~600 cm^2/Vs [93] and ~900 cm^2/Vs [1], respectively. For the PMELA assessment, TFTs with W = 2 μm and L = 1 μm were used, so that they were entirely contained within the 5 μm × 5 μm large-grain areas. In ~10 % of these grains, both p- and n-channel PMELA TFTs matched the performance of single crystal SOI MOSFETs, which were identically processed (apart from the crystallisation stage). These high performance TFTs were located in regions of {100} pseudo-single-crystal (PSX) material; however, as the PSX regions accounted for only 10 % of the crystallised areas, techniques still need to be established to improve uniformity by generating this orientation in all crystallised regions [1].

In contrast, to the above two techniques, the μ-Cz technique [98] requires the Si film to be patterned rather than modulating the incident laser beam. This is achieved photo-lithographically, by etching shallow, small diameter (<100 nm) holes into a layer of SiO_2 which is subsequently coated with a-Si. The a-Si film

fills the holes, so that the Si film thickness at these points is greater than on the surrounding surface, and, when exposed to a laser intensity sufficient to melt the surrounding film, the film remains solid at the bottom of the hole. Hence, there will be a transition region in the hole, within which the normal ELA process will form some crystallites, and these will seed lateral grain growth into the surrounding molten Si, as shown schematically in Fig. 7.36a [99]. By controlling the diameter of this hole, it can act as a grain filter and reduce the number of seeding crystallites to unity, with the objective of producing single crystal areas. As with the PMELA technique, this procedure has been implemented to produce an array of square, abutting grains, whose sides are ~6 µm in length, with the seeding region sited in the centre of these grains. The grain structure is shown in Fig. 7.36b, and electrical assessment of the material was carried out with small channel TFTs (W and L ~2 µm), which were able to fit within the individual grains [99]. Figure 7.36b illustrates different TFT positioning within the grains, and those sited directly over the grain filter, such as 'C', had the worst characteristics. For those TFTs horizontally or vertically displaced from this location, such as 'X' or 'Y', the device

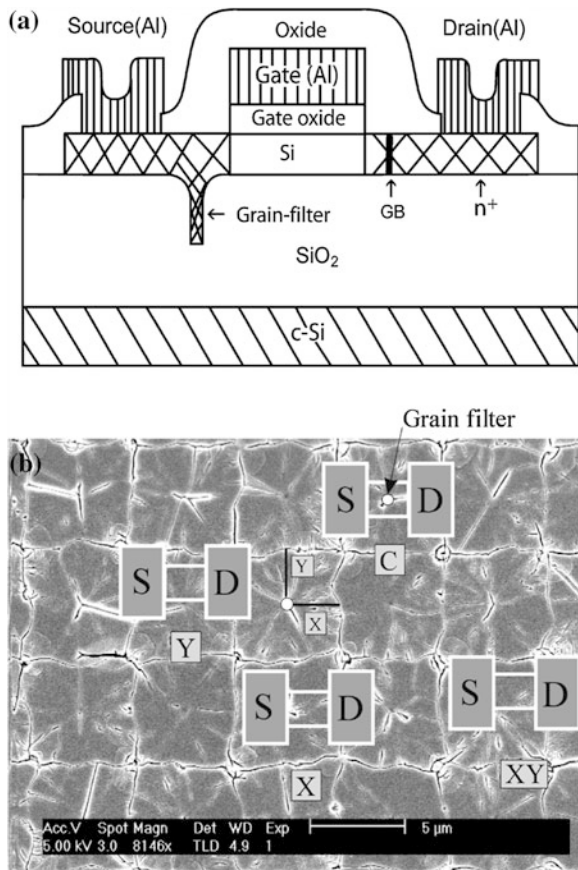

Fig. 7.36 **a** Cross-sectional diagram of μ-Cz process and c-Si TFT channel sited within a single grain, and **b** SEM micrograph of an array of location controlled grains grown by the μ-Cz technique. Superimposed on this image are TFT locations with respect to the grain filter positions. (Reprinted from [99] with permission of IEEE)

characteristics were much better, with electron mobilities up to ~600 cm^2/Vs. However, the standard deviation in these values was ±100 cm^2/Vs [99], and it is likely that uniformity improvements will be needed for routine implementation of this process.

Both the PMELA and μ-Cz processes have been implemented with single shot crystallisation, whilst the minimum shot number in SLS is two, and all processes use beam intensities sufficient to cause full melt-through. Hence, these techniques offer the potential for higher throughput and a larger energy density processing window than conventional ELA (in addition to the improved TFT performance through higher carrier mobility). At the moment, the SLS technique appears to be the closest to commercial implementation [100], and it will be described in more detail in the following section.

7.5.2.1 Sequential Lateral Solidification

As mentioned above, SLS uses a spatially varying beam intensity, which consists of a number of beamlets, just a few micrometers wide in one direction and several millimetres in the other. The beamlets are produced by projecting the homogenised excimer laser beam through a mask having alternate clear and occluded stripes [29, 32], and the ensuing crystallisation process is shown schematically in Fig. 7.37a–c. Within the high intensity beamlet areas, full film melting takes place and, at the edge of these regions, there will be an SLG region, which seeds the lateral growth into the molten region. Following single shot irradiation, two scenarios are shown, depending upon the relative widths of the beam, W_B, and of the seeded lateral growth distances, L_{lat}. For $L_{lat} < W_B/2$, the centre of the molten region undergoes random nucleation before the lateral growth front reaches this region, and results in fine grain material in the centre of each exposed stripe. To avoid this happening, the beamlet size needs to be $<\sim 5\ \mu m$ (in contrast to the conventional line beam ELA, in which the beam is ~350–500 μm wide), resulting in the situation shown in Fig. 7.37c. In this case, the two lateral growth fronts meet in the centre of the previously melted region, and produce a collision-front grain boundary. In the orthogonal direction, there are low angle sub-grain boundaries running parallel to the lateral growth direction.

Following this first shot, the material consists of alternating stripes of a-Si and poly-Si, and further irradiations are required to complete the crystallisation process, as shown schematically in Fig. 7.38a and b. In Fig. 7.38a, the plate is moved a distance Δx prior to the next irradiation, where $\Delta x < W_B/2$, such that the original melt-front-collision GB is melted by the second pulse, and the remaining polycrystalline material seeds further lateral growth, propagating the grain to the right. With an appropriate projection mask design, this process can be indefinitely repeated to produce grains tens or hundreds of micrometres long. The main constraint with this implementation of the process is the throughput, which will inversely scale with the number of grain-propagating laser shots.

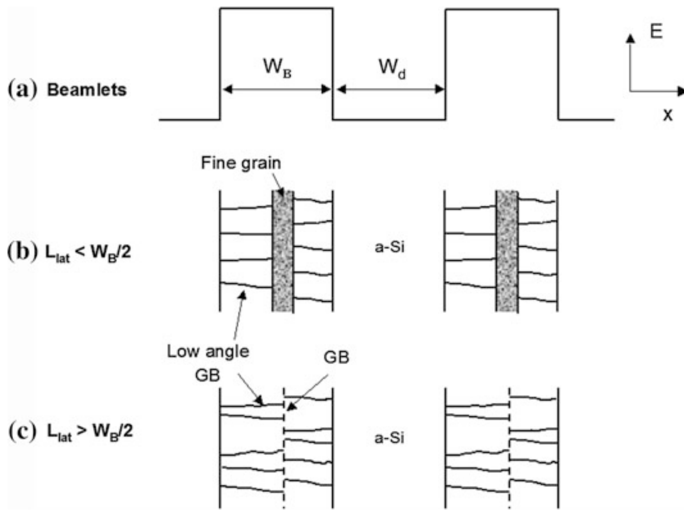

Fig. 7.37 Schematic illustration of the SLS process: **a** micro-beamlets of width W_B, separated by gap W_d, **b** lateral grain growth, and random nucleation when W_B is too large, and **c** complete crystallisation of the melted area when W_B is less than the ateral growth limit

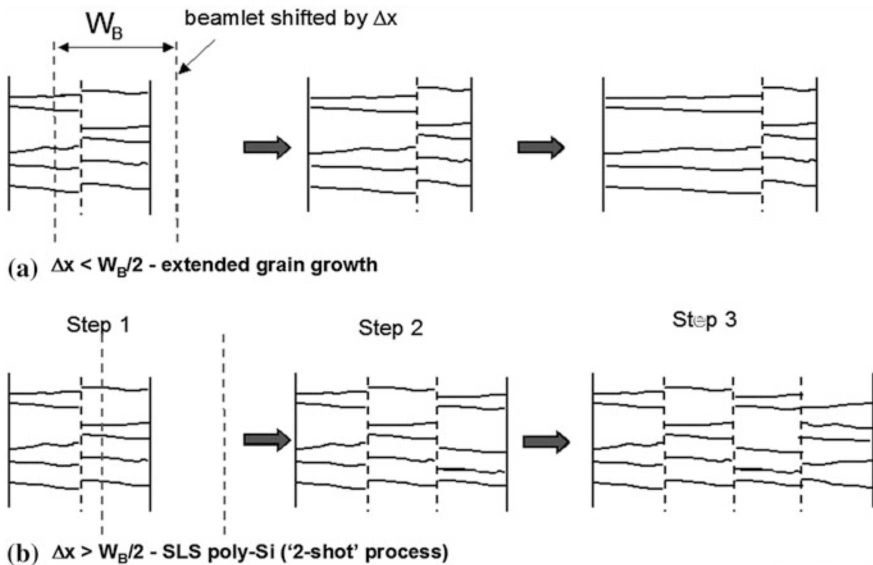

Fig. 7.38 Illustration of the SLS grain propagation process: **a** generation of extended grain material, where the beamlet stepping interval, $\Delta x < W_B/2$, and **b** repeating array of poly-Si grains, where $\Delta x > W_B/2$

When $\Delta x > W_B/2$, the situation shown in Fig. 7.38b is produced, and the original collision-front grain boundary is retained, and a similar grain structure is generated by the second irradiation. With an appropriate mask design, this process can be implemented as a 2-shot process, giving the highest throughput obtainable with SLS. The grain structures resulting from these two SLS implementations are shown in Fig. 7.39a and b, respectively [100]. Figure 7.39a is an SEM micrograph of the multi-shot grain propagation process, giving grains >15 μm long, with closely spaced sub-grain boundaries running parallel to the propagation direction. The spacing of these sub-grain boundaries increases with increasing film thickness [101], and, with increasing grain propagation, there is grain filtering and a tendency for the low-angle sub-grain boundaries to become high-angle [102]. The micrograph in Fig. 7.39b is of the 2-shot SLS process, showing the regularly spaced collision-front grain boundaries, as well as the low-angle sub-grain boundaries.

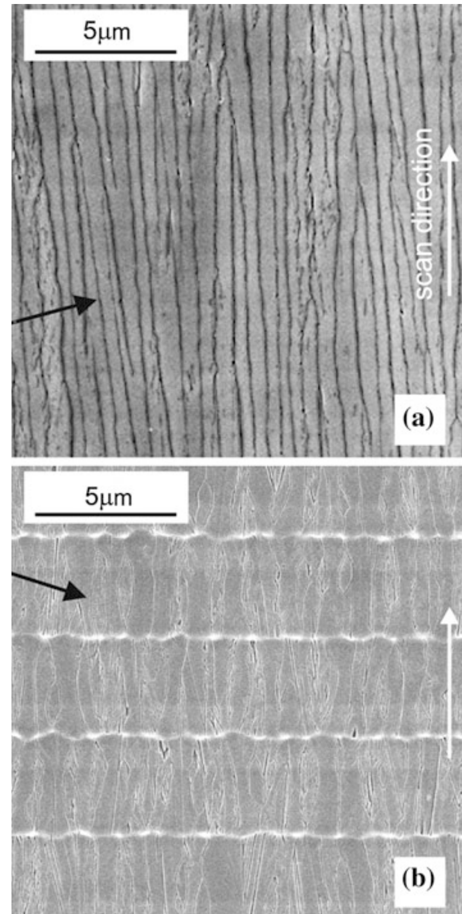

Fig. 7.39 SEM micrographs of SLS Si: **a** extended grain material, and **b** '2-shot' SLS poly-Si. (Reprinted from [100] with permission of ITC'07)

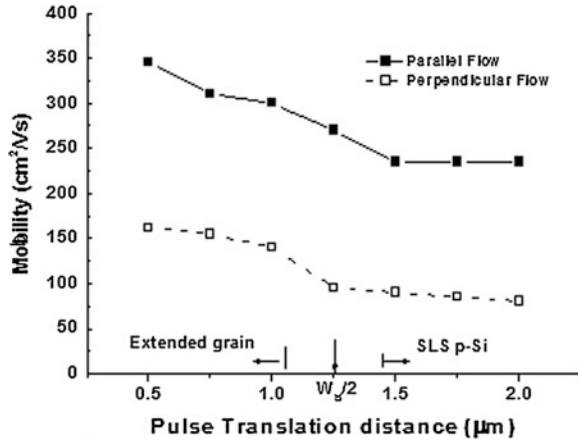

Fig. 7.40 Variation of electron mobility with pulse translation distance, Δx, in SLS material, for carrier flow parallel and perpendicular to the low angle grain boundaries. The demarcation line between extended grain and '2-shot' SLS poly-Si is shown at $\Delta x = W_B/2$ ($W_B = 2.5$ μm, $t_{Si} = 100$ nm)

Some of the characteristic features of SLS material are shown by the TFT results in Fig. 7.40 [103]. The electron mobility is plotted as function of the substrate translation distance between pulses, Δx, and results are shown for carrier flow parallel and perpendicular to the sub-grain boundaries. These results were taken from 100 nm thick poly-Si films, with a sub-GB spacing of 0.37 μm. The two major features in this plot are, firstly, the reduction in mobility for carrier flow perpendicular to the sub-grain boundaries, due to the GB anisotropy giving greater carrier scattering in this direction of current flow. Secondly, for parallel flow, the reduction in electron mobility from ~300–350 cm^2/Vs to ~240 cm^2/Vs, with increasing plate translation distance, is due to the change in material from the extended grain form ($\Delta x < W_B/2$) to '2-shot SLS' material containing regularly spaced collision-front grain boundaries ($\Delta x > W_B/2$). Qualitatively identical results have also been obtained for the hole mobility in p-channel TFTs. Within the two specific types of material, extended grain and '2-shot SLS', the process was able to yield good mobility uniformity of ±6–7 %, and ±2–3 %, respectively [103]. The better uniformity of the '2-shot' material was most likely due to better averaging of grain properties over those much smaller grains. In other work, optimisation of the high throughput, '2-shot SLS' process has given electron mobility values up to 350 cm^2/Vs [94].

The above discussion has focussed on the formation of 'directional' material by scanning line-beamlets. The technique can also be implemented to give localised single crystal regions by the use of chevron shaped beamlets [29], or by implementing the 2-shot process in two orthogonal directions [104]. However, 'single crystal' SLS material has not been electrically characterised as intensively as the PMELA and μ-Cz materials.

7.5.3 Green Laser Crystallisation

Diode pumped solid state lasers have been advocated to address both the pulse stability and cost of ownership issues associated with ELA, and Q-switched Nd:YAG and CW Nd:YVO_4 lasers have been the most widely used solid state lasers [35–42]. The fundamental output wavelength from both lasers is 1064 nm, and, in order to achieve efficient absorption into thin a-Si films, the second harmonic phase at 532 nm has been utilised, where the absorption depth in a-Si and poly-Si is 100 nm and 125 nm, respectively [24]. This is $\sim$10 times greater than the absorption depth of 308 nm radiation, so that the coupling efficiency is smaller, although the authors of the green laser work argue that the greater absorption depth gives a more uniform temperature profile in the silicon, which is discussed further below.

7.5.3.1 Pulsed Nd:YAG Lasers

In the Q-switched mode at 532 nm, Nd:YAG lasers can deliver short duration pulses ($\geq$10 ns) of 800 mJ/cm^2, with a repetition frequency of 4 kHz and an output power of 200 W [35]. The basic beam shape from a Nd:YAG laser is circular, with a Gaussian distribution of energies across its diameter, and an a-Si crystallisation system has been developed in which this shape has been optically converted into a line-beam [35]. In this system, the length of the line beam, which had a top-hat profile, was 105 mm, whilst, in the short direction, the Gaussian shape was retained, with a full width at half maximum of 40 μm, as shown in Fig. 7.41. For crystallisation, the plate scanning direction was parallel to the short axis, with typical translation stage movements of 1–5 μm between pulses [35–37], giving a multi-shot process of 40–8 shots, respectively. The pre-cursor a-Si films were typically in the thickness range 50–100 nm, and, when crystallised into poly-Si, three energy

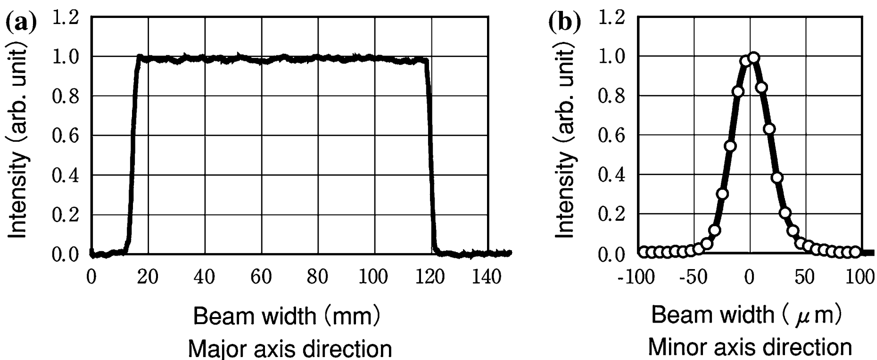

Fig. 7.41 Beam profile measured in 532 nm, Q-switched Nd-YAG laser crystallisation system. (Reprinted from [35], with permission of Ulvac)

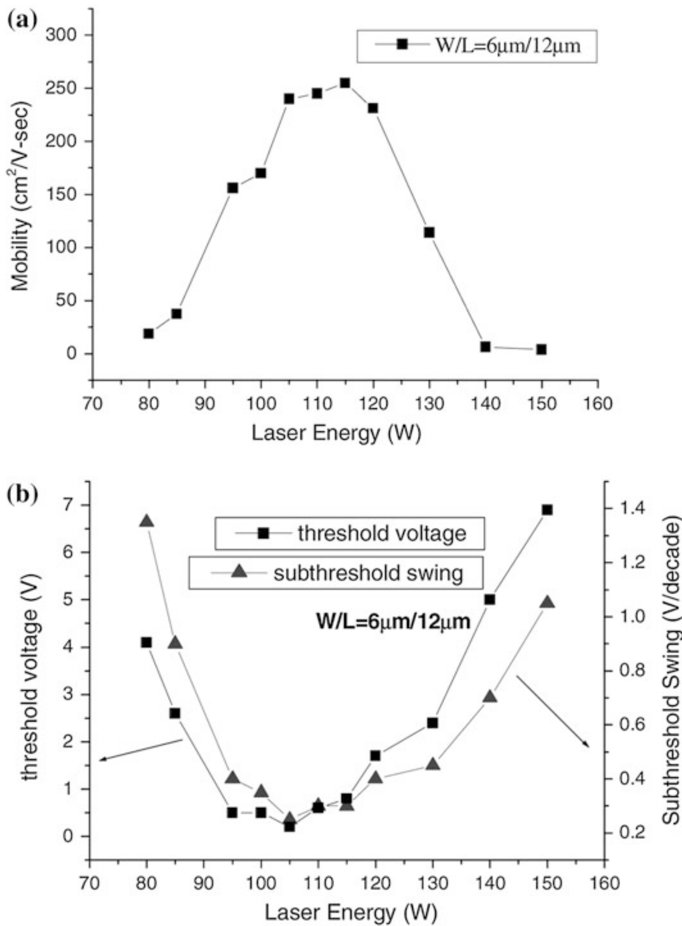

Fig. 7.42 Dependence of TFT characteristics on Q-switched 532 nm Nd:YAG laser power (**a**) electron mobility, and (**b**) threshold voltage and sub-threshold slope. (Reproduced with permission from [36])

density regimes were identified [36]: the first, at low energies (85–95 W laser power), was referred to as vertical crystallisation, and gave grains of ~100 nm, or more, in partially melted films. The second regime (105–120 W) was named SLG, which occurred when the film had fully melted and yielded larger grains, and the third regime (above 130 W) yielded fine grain material. When the TFT device parameters were measured as a function of laser power, as shown in Fig. 7.42, they showed a good correlation with the power-dependent grain structure, and gave a maximum electron mobility of 250 cm^2/Vs over the optimum laser power range of ~105–120 W for a 20 shot process [36]. As will be apparent, these regimes, and the associated device properties, are similar to the regimes identified with ELA. However, the authors argue that there is a fundamental difference due to the ~10 times

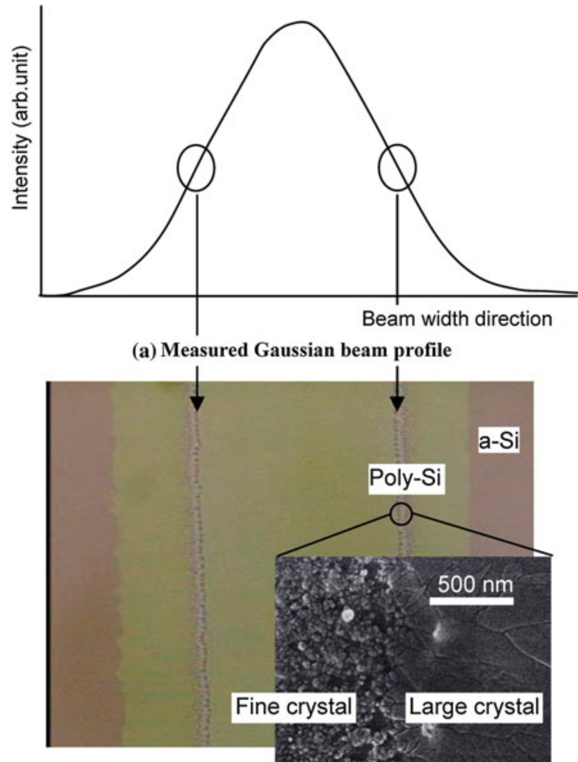

Fig. 7.43 Relationship between Q-switched 532 nm Nd:YAG laser beam profile and local poly-Si grain morphology. (Reprinted from [37] with permission of SID)

larger absorption depth of the green laser [35–37], which produces a more uniform temperature distribution through the depth of the film. As a result of this, the SLG process does not start from the bottom interface, but from the edges of the melted area [35–37]. In support of this argument, the micrographs in Fig. 7.43 show fine grain silicon in an area fully melted by the Nd:YAG beam, with large grain silicon appearing at a specific energy density on the edge of the irradiated area. Moreover, it was shown that this laterally seeded large grain region could be laterally propagated as the plate is stepped through the beam, leading to a larger processing window and larger grains than with the standard ELA process. The process comparison, in terms of the range of energy densities over which high carrier mobility TFTs can be produced, is shown in Fig. 7.44 [37].

However, this Nd:YAG process appears to be similar to the SLS process [29], discussed in Sect. 7.5.2.1, which also operates in full melt-through, relying upon seeded crystallisation from the edges of the melted areas, and uses small plate stepping intervals of 2–3 μm to propagate large sized grains. In view of these similarities between Nd;YAG irradiations and excimer SLS, the features of the Nd:YAG process cannot be uniquely attributed to the greater optical absorption depth of 532 nm radiation in a-Si. Indeed, as discussed above, in Sect. 7.2.2.2, the

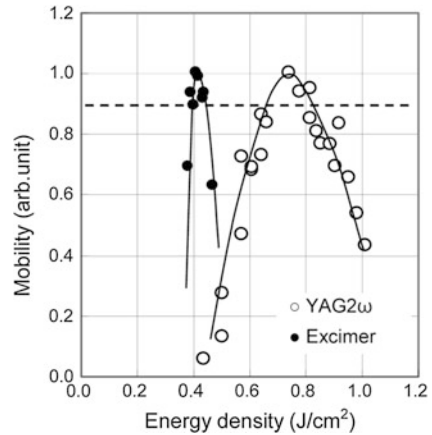

Fig. 7.44 Comparison of electron mobility and processing window sizes for ELA and Q-switched Nd-YAG crystallisations. (Reprinted from [37] with permission of SID)

large thermal diffusion length in a-Si leads to full melting of excimer laser irradiated thin films up to at least ~200 nm.

In summary, pulsed Nd:YAG crystallisation can lead to a larger process window, and potentially higher performance devices than conventional ELA, together with good pulse-to-pulse stability and lower cost of ownership. However, SLS also offers a larger processing window, and better device performance than conventional ELA. From a manufacturing perspective, system throughput and complexity are also important considerations, and these are compared in Sect. 7.5.4.

7.5.3.2 CW Nd:YVO_4 Lasers

For CW crystallisation, Nd:YVO_4 lasers are preferred to Nd:YAG lasers, as they operate with higher power and can deliver 10 W at 532 nm, with a power stability of better than 1 %. However, the conditions for successful crystallisation, using the high power CW laser, were more restrictive than for pulsed lasers, with the major problems being de-lamination of the a-Si film and damage to the glass substrate. To avoid these problems, the a-Si film was pre-patterned into discrete islands, rather than left undefined, and the preferred patterning was into close-packed 50 μm × 200 μm lozenge-shaped areas, with an inter-island spacing of 5 μm [39, 40]. These areas were large enough to accommodate 1–2 TFTs with W = 3 μm and L = 5 μm. Secondly, crystallisation of films thicker than 300 nm damaged the glass substrate, and, to avoid this, the a-Si thickness range was restricted to 50–150 nm, and, thirdly, high speed scanning at more than 20 cm/s was required. All these measures served to limit both the amount of energy absorbed by the film and coupled into the substrate, although clearly the power setting of the laser played a role as well.

The laser spot size was 200 μm × 20 μm, which was scanned in a direction parallel to the short axis along the length of the pre-defined a-Si islands. The resulting crystal structure displayed a strong interdependence on scan speed and

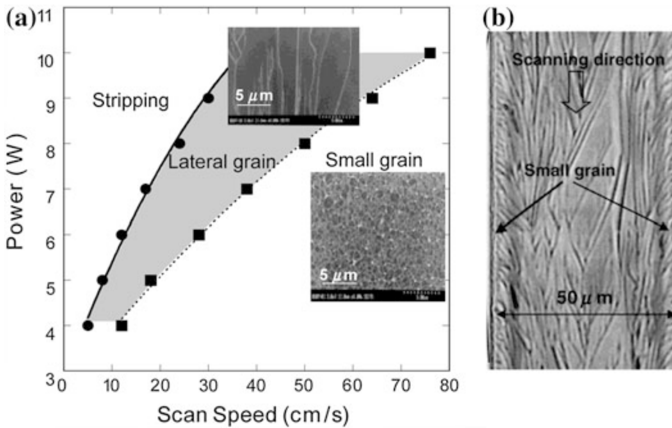

Fig. 7.45 CW Nd:YVO_4 laser crystallisation of poly-Si at 532 nm: **a** dependence of grain size and structure on laser power and scan speed, and **b** optical micrograph of pre-defined Si island, showing the Secco-etched large grain poly-Si in the centre of the island. (Reprinted with permission from [40]. Copyright (2002) The Japan Society of Applied Physics)

laser power setting, as shown by the results for 150 nm thick films in Fig. 7.45a [40]. Three crystallisation regimes were identified: at low power or high scanning speeds, small grain silicon was formed, whose appearance (as shown by the insert), at 10 W and 100 cm/s, was comparable to the SLG grains in ELA processing, whilst at 200 cm/s the grain structure was more consistent with solid phase crystallisation [39]. At higher powers and/or slower scan speeds, large laterally propagated grains were formed (see insert), whose dimensions were $\sim 3\ \mu m \times 20\ \mu m$, with the grain boundaries running parallel to the beam scanning direction. At the slowest scan speeds and highest powers the film and substrate were damaged.

The large grains were formed preferentially in the central regions of the pre-defined Si islands, because faster cooling rates along the edges of the islands resulted in smaller grains there, as shown in Fig. 7.45b. The transfer characteristics from high performance p- and n-channel TFTs, formed in a 150 nm thick film crystallised with 6 W, at a scan speed of 20 cm/s, are shown in Fig. 7.46. The high carrier mobility was attributed both to the large grain size and to the (100) surface orientation of these grains (although 100 nm thick films had a mixture of (110) and (111) oriented grains). The more general dependence of electron mobility on plate scan speed is shown in Fig. 7.47, together with the associated grain structures. The TFT transfer characteristics in Fig. 7.46 were for carrier flow parallel to the grain boundaries, and the data in Fig. 7.47 are for carrier flow both parallel and perpendicular to the grain boundaries. For perpendicular flow in the large grain material, the mobility was considerably lower than for parallel flow, which is similar to the situation with SLS silicon, due to the scattering effect of the grain boundaries. For the smaller grain, ELA-like material, the grains were equi-axed and there was no anisotropy in electron mobility.

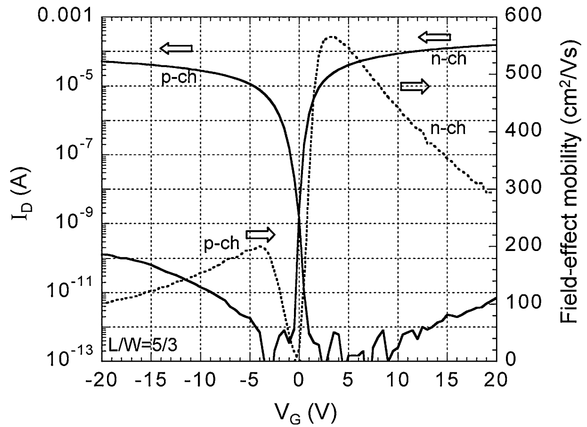

Fig. 7.46 Transfer characteristics of n- and p-channel large grain TFTs crystallised by CW Nd:YVO_4 laser at 532 nm. (Reprinted with permission from [40]. Copyright (2002) The Japan Society of Applied Physics)

The uniformity of device characteristics has not been published [39, 40]. However, in view of the spatial variation in grain structure across the width of the crystallised islands (shown in Fig. 7.45b), there must be some concern, although earlier work on unpatterned films showed better uniformity than ELA [41].

There is clearly a trade-off in scan speed and material quality with this process, and this issue is compared with SLS and pulsed Nd:YAG crystallisation in the next section.

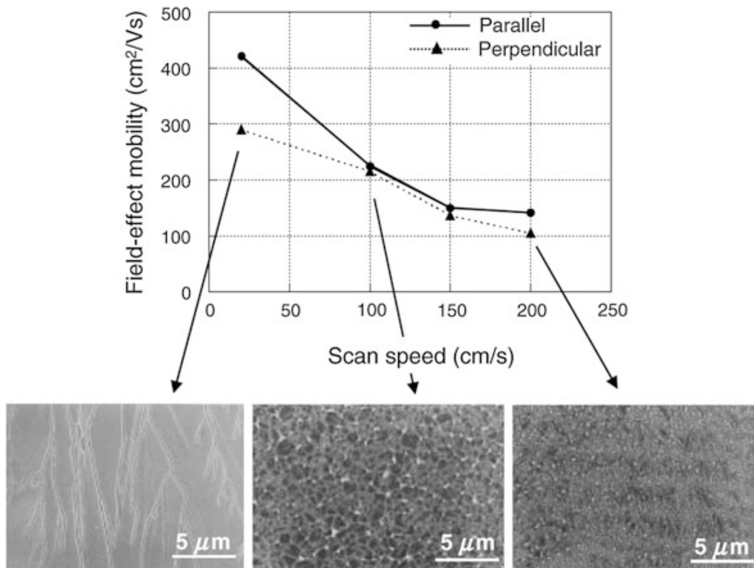

Fig. 7.47 Electron field effect mobility (for parallel and perpendicular current flow) and grain structure as a function CW Nd:YVO_4 laser scan speed. (Reprinted with permission from [39]. Copyright (2002) The Japan Society of Applied Physics)

7.5.4 Comparison of Large Grain Crystallisation Systems

All the crystallisation systems considered in this section can produce large grain, high quality TFT material, as well as being revealing tools with which to investigate the crystallisation process itself. Where a direct comparison can be made, they also offer a solution to some of the technical issues with conventional ELA, such as the size of the processing window and the associated pulse stability problem, and, in the case of the solid state lasers, they offer lower cost of ownership. These latter points are largely manufacturing issues, and a key consideration in this industrial context is plate throughput. To a large extent, throughput will scale with both the power of the system, which will determine the beam area and shot frequency, and with the efficiency of the usage of this power, which will also embrace the number of shots in the process. Taking these simple considerations into account, the crystallisation rate, R, can be calculated using: $R = \frac{A_b f}{N}$ for pulsed lasers, and $R = \frac{A_b v}{L_{\min}}$ for the CW laser. Where A_b is the beam area on the plate, f is the pulse frequency, N is the number of shots in the process, v is the plate scan velocity, and L_{min} is the small axis beam dimension.

The key features of the ELA [18], SLS [32, 94], pulsed Nd:YAG [35] and CW Nd:YVO_4 [39] systems are compared in Table 7.2, where a first order estimate of throughput is provided by the crystallisation rate, R. It should be emphasised that this is only a first order estimate as it does not account for the deceleration period of the plate translation stage at the end of each scan, and its movement and acceleration intervals for the next scan. In addition, the smaller the beam dimensions, the more scans will be needed to crystallise a whole plate, and the more significant the scan interruptions will be.

From this table, it is clear that the throughput of the Nd:YAG system is significantly lower than the ELA system, although it offers a larger process window, better pulse stability and lower cost of ownership. To what extent these beneficial features offset its lower throughput would need to be determined in a manufacturing environment. However, the overall system costs will play a role, as these determine whether it is economic to have a larger number of Nd:YAG systems as a way of maintaining the required plate processing capacity. It is also interesting to

Table 7.2 Comparison of crystallization rates in different laser annealing systems

Laser system	Power (W)	Beam size (cm × cm)	Freq (Hz)	Shot no.	Step size (μm)	Scan vel (cm/s)	Crystn rate (cm^2/s)
ELA [18]	600	$46.5 \times 3.5 \times 10^{-2}$	600	20	17.5		48.8
SLS [32, 100]	315	2.5×0.15	300	2	2.5		56.3
Nd:YAG [35]	200	$10.5 \times 4.0 \times 10^{-3}$	4000	20	2		8.4
Nd:YVO4 [39]	10	$4.0 \times 10^{-2} \times 2.0 \times 10^{-3}$	CW			50	2

note that the crystallisation rate figures for these two systems do not simply scale with system power (for the same shot number), as there is a further discrepancy by a factor of two when normalising R by power. Whilst, the overall optical efficiency of the two beam shaping systems will play a role here, there is also reduced coupling efficiency of the 532 nm radiation into the thin film because of its larger absorption depth. Hence, if a given absorbed energy density is required to melt a film of a given thickness, a higher incident density will be required with the 532 nm laser. For a given maximum output pulse energy, the incident energy density will be determined by the final beam dimensions, A_b, on the plate, and this directly controls R.

Given the sub-optimal absorption from green lasers, the use of a solid state, 445 nm blue laser has been reported [105]. The radiation at this wavelength will be more strongly absorbed, but this is an undeveloped process, with no device results reported to date.

The CW Nd:YVO4 system produces large grain material comparable to the 2-shot SLS process, and avoids the SLS system complexity of projection masks and the high resolution optical system required to produce 4–5 μm beamlets. However, its crystallisation rate is ~25 times lower than the SLS system. In recognition of this low basic crystallisation rate, a high throughput system has been designed [41], in which a number of laser sub-beams were used to simultaneously, and selectively, irradiate just the TFT areas of a display plate. This is shown in Fig. 7.48, and a crystallisation rate of 48 cm^2/s was calculated using sixteen 30–50 μm sub-beams, scanned at 2 m/s, in order to crystallise pixel TFTs at a pitch of 148 μm [41]. At this high scan speed, the electron mobility was ~150 cm^2/Vs (see Fig. 7.47), which is perfectly adequate for pixel TFTs. The peripheral driver TFTs occupy a much smaller area than the display area, but a higher carrier mobility is beneficial. For these areas, four 150 μm sub-beams were scanned at 50 cm/s, delivering a crystallisation rate of 2.4 cm^2/s, and produced TFTs with an electron mobility of 400–600 cm^2/Vs.

At the time of writing, in spite of these solid-state laser alternatives, ELA continues to be the dominant crystallisation process for poly-Si TFTs.

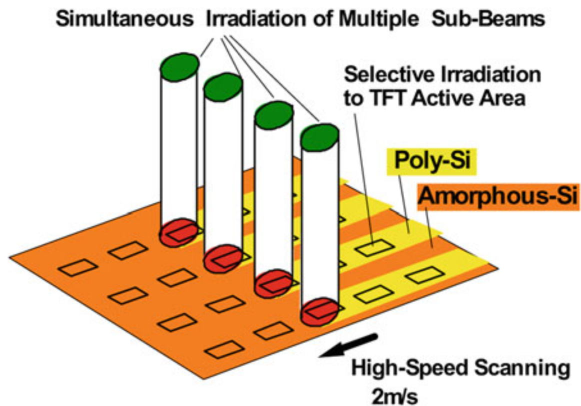

Fig. 7.48 Illustration of multiple sub-beam CW Nd:YVO_4 laser system for high throughput crystallisation. (Reprinted from [41] with permission of SID)

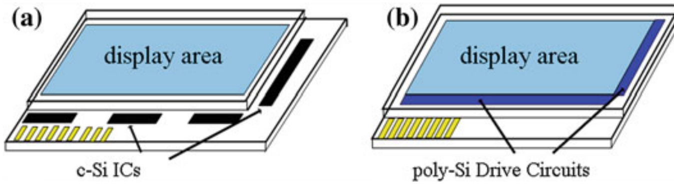

Fig. 7.49 Illustration of active matrix display cells showing drive circuits: **a** a-Si:H TFT display with externally mounted c-Si ICs, and **b** poly-Si TFT display with monolithically integrated poly-Si drive circuits

7.6 Poly-Si Applications

In order to deliver the appropriate signals to the pixels in an AMLCD (or AM-OLED display), using line-at-a-time addressing (see Chap. 4 for a detailed discussion of active matrix display operation) it is necessary to apply appropriate drive signals to the rows and columns of a display. For an a-Si:H display, where the switching speed of the a-Si:H TFTs is too slow to perform these functions, it is necessary to mount external silicon ICs around the edge of the display, as shown schematically in Fig. 7.49a. These circuits may be directly attached to the plate, or connected to the plate by flexible foils, upon which the ICs are mounted (as discussed in Sect. 4.5.4). The number of these ICs will be determined by the resolution of the display, i.e. the number of rows and columns to be addressed, and this will feed through into the cost of the display module in terms of the direct chip costs plus their mounting costs. The higher carrier mobility in poly-Si enables the direct fabrication of these addressing circuits on the active plate, as illustrated in Fig. 7.49b, and thereby reduce the module cost.

However, the cost saving due to the integration of the drive circuitry needs to be balanced against the increased cost of manufacturing the poly-Si active matrix plate. This is due to the greater number of masking and deposition stages (typically 9-mask stages, as shown in Sect. 7.4.2), as opposed to the 5-mask process for a-Si:H AMLCDs (see Sect. 5.3). In addition, there is the specific extra capital equipment needed to make poly-Si TFTs, principally the laser crystallisation and the ion doping systems (as discussed in Sect. 7.4.2), as well as extra aligners and deposition systems to give a balanced manufacturing process with the higher mask and deposition process count. Finally, there is a possible difference in yield in the more complex poly-Si process, where yield modelling is handled by assuming that the yield, Y, is given by a Poisson distribution of random defects, of density D, in a defect-sensitive area, A [106]:

$$Y = \exp -DA$$

and D is given by Nd, where d is the defect density per photolithographic step, and N is the number of steps. Hence, more mask stages can be expected to reduce process yield and add to unit costs.

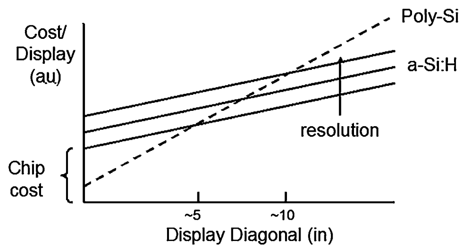

Fig. 7.50 Comparison of qualitative cost models, for a-Si:H displays with external drive circuits, and poly-Si displays with integrated drive circuits

Whilst detailed a detailed cost model, based on the evaluation of the above factors, is beyond the scope of this book, a qualitative model can give insight into the essential features of the price comparison, and this is shown in Fig. 7.50. In this figure, the cost of an individual display is plotted as function of the display diagonal, where it is assumed that there is a fixed cost for processing a glass plate of a given size, using either the poly-Si or the a-Si:H process. As shown, the smaller the display diagonal, the more displays there will be per glass plate, and, hence, the cost per display scales with its size. The slopes of the lines represent the different plate manufacturing costs for the low mask-count a-Si:H process and the higher mask-count poly-Si process. The intercept of these lines on the y-axis is determined by the number and cost of the externally added ICs, which is governed by the display resolution rather than by the display diagonal. Hence, these circuits represent a higher relative fixed cost as the display diagonal reduces, and these considerations demonstrate that poly-Si AMLCDs are most cost effective for small display diagonals. A cost cross-over point at 8-10 inch diagonals is shown as an approximate representation of the current situation, but this will vary with future IC costs and changes in the economics of plate manufacturing.

Thus, the major current application for poly-Si AMLCDs is in the high volume, 'mobile' display market (mobile/smart phones, digital camera view-finders, personal media players etc.), where circuit integration offers further advantages over and above the cost benefit. For instance, these portable displays need to be rugged, light-weight, and compact, and the poly-Si integrated circuits eliminate the risks of IC chip de-lamination due to mechanical shock. They also reduce the size of the glass module itself by reducing the space reserved for chip bonding. Finally, for higher resolution, small diagonal displays, the reduced pixel pitch can become a limiting factor for aligning and bonding the external ICs, but can be more easily met with the integrated drivers.

The poly-Si TFT CMOS circuits currently integrated into poly-Si displays include the row and column shift registers, level shifting circuits, 6-bit D/A converters for the column drivers, charge pumps and control logic [2, 11, 107, 108]. In contrast to these n- and p-channel CMOS circuits, which require the high mask count discussed above, it has been suggested that a lower level of circuit integration could be achieved at a lower processing cost, by using just p-channel TFTs [109]. This would reduce the mask count by three masks, by eliminating the separate masking stages for the n- and p-channel dopant locations, since the gate

electrode alone is sufficient to define the source and drain regions in single channel SA TFTs. In addition, the LDD mask can be removed as the superior drain bias stability of p-channel TFTs obviates the need for drain field relief. These process simplifications can lead to a more cost competitive technology compared with a-Si:H for large diagonal displays, albeit at the expense of reduced circuit performance. This is because single channel inverters conventionally have a greater power dissipation, smaller dynamic range and slower switching speed than CMOS inverters, but various single channel circuit alternatives have been proposed to reduce these performance limitations [110].

The other emerging application for poly-Si TFTs is in small/medium diagonal AMOLED displays, particularly for smart phones. At the moment, poly-Si is the preferred pixel transistor in these commercial displays, as it can provide the higher drive currents needed for OLEDs. Moreover, this application requires a high duty cycle on-current, and, under these conditions, poly-Si TFTs also have better bias stability than a-Si:H TFTs. However, amorphous oxide semiconductor, AOS, TFTs, using, for instance, a-indium-gallium-zinc-oxide, have also been identified as potential candidates for commercial AMOLED products [111], and a comparison of the stability of the major TFT technologies for this application is shown in Fig. 9.25 (in Sect. 9.4.3.3). For a fuller discussion of the background issues associated with AMOLED pixel design, see Sect. 4.6.2.2.

7.7 Summary

Poly-Si TFTs are now in mass production, particularly for small/medium diagonal, portable displays, containing integrated drive circuits. The circuit integration is facilitated by the high carrier mobility, and this has been achieved through a number of technology evolutions. The current, commercial fabrication process relies upon excimer laser crystallisation of a-Si:H pre-cursor layers, where the preferred excimer laser wavelength is 308 nm, which is obtained from a XeCl gas mixture. These are pulsed lasers, with a pulse duration of $\sim$30 ns, and the combination of UV wavelength and short pulse duration enables the a-Si film to be melted without undue heat transmission into the underlying glass substrate. The resulting grain structure displays a complex dependence upon the fractional melting of the film, where the optimum grain structure, and device performance, results from almost full melting of the a-Si films. Under these conditions, high quality $\sim$300 nm sized grains are formed, and the resulting electron field effect mobility lies between $\sim$100 cm^2/Vs and $\sim$250 cm^2/Vs, depending upon the number of laser shots in the process. The most uniform films, giving the highest performance devices, result from high shot number processing, but this gives the lowest throughput. Hence there is a trade-off between uniformity, performance and throughput, with typical manufacturing processes employing 20–30 shot processing.

In view of these well understood issues, alternative lasers and crystallisation procedures have been reported, including green solid-state lasers, as well as modified excimer laser technologies. These have all been able to produce larger grain material, with increased electron mobility values, which, in some cases, approach single crystal values. In addition to these laser-based techniques, there has also been interest in enhanced SPC procedures, using a metal catalyst to increase the speed of this inherently slow process. This is fundamentally a homogeneous large area process, which offers improved large area uniformity in contrast to the laser techniques. With a laser, the beam area itself is always far smaller than the substrate plate, and, therefore, beam uniformity, pulse-to-pulse energy fluctuations and pulse overlap effects all need to be carefully controlled to produce acceptable uniformity. The favoured metal for the enhanced SPC process is nickel, because it has a silicide phase, which is well lattice-matched to Si. This seeds the crystallisation of a-Si by a process variously referred to as silicide-mediated crystallisation (SMC) or metal-induced crystallisation (MIC). TFTs produced using this process have tended to have high off-state leakage currents, which have limited their practical application. However, it has been established that a subsequent excimer laser crystallisation stage can resolve that problem, and produce high performance TFTs. Nevertheless, in spite of these widely investigated alternatives, the current industrial production of poly-Si TFTs is still largely based upon excimer laser crystallisation.

The prevailing architecture of poly-Si TFTs is top-gated, and self-aligned (SA), with an SiO_2 gate dielectric, all of which are more similar to the semiconductor industry's silicon-on-insulator MOSFETs, rather than to the AMLCD industry's inverted staggered a-Si:H TFTs. In addition, this structure is implemented using ion doping for the source and drain dopants. However, the use of high-energy phosphorus ions, for the n-channel TFTs, is potentially damaging to the lattice within the doped regions. This damage needs to be carefully controlled to minimise device performance artefacts, namely increased leakage current and reduced on-state currents. For some purposes, particularly for basic materials investigation, a non-self-aligned structure (which is also top-gated and ion doped) offers a simpler process, and avoids the ion damage issues of the SA process. However, the SA process is necessary for short channel TFTs, and is the standard industry architecture. The other architectural feature specific to n-channel poly-Si TFTs is a lightly n^--doped region adjacent to the drain junction, which is needed to reduce the drain field, and, thereby, suppress drain-bias-stress induced hot carrier instabilities. It also diminishes other performance artefacts associated with a high field at the drain, in particular field enhanced leakage currents and poor current saturation of the output characteristics. These latter device performance issues are discussed in detail in Chap. 8.

Single channel TFTs of either architecture can be produced using a four-mask process. However, for a poly-Si AMLCD, with integrated complementary TFT drive circuits, a higher mask count than for a-Si:H AMLCDs is necessary, and a nine-mask process is illustrated. This higher mask count, and a more complex process, influences the commercial application of poly-Si TFTs, and a simple,

qualitative cost model illustrates why the current application is limited to small/ medium diagonal displays.

In summary, poly-Si TFTs are now in mass-production, particularly for small/ medium diagonal displays, where the integration of drive circuitry can give both cost and performance benefits. The circuit integration is facilitated by the high carrier mobility in poly-Si, and this can be achieved in both p- and n-channel TFTs, which enables complementary TFT circuit design. Within the small/medium display market, poly-Si accounts for $\sim$40 % of the AMLCD product revenues, and dominates the current smart phone AMOLED market.

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Chapter 8
Poly-Si TFT Performance

Abstract This chapter deals with the electrical characterisation, and related performance issues, of poly-Si TFTs. The subjects covered include an analytical model for conduction in poly-crystalline material, issues with the measurement of the poly-Si DOS, low field and high field leakage current behaviour, and an overview of the bias stress instability mechanisms in these devices. Finally, there is a discussion of short channel effects, including the role of parasitic bipolar transistor action caused by floating body effects.

8.1 Introduction

Chapter 7 dealt with the preparation of poly-Si material, as well as describing the architecture and fabrication process of poly-Si TFTs. In this chapter, the characterisation and performance of these devices is dealt with in greater detail. Poly-Si is a polycrystalline material, consisting of small grains separated by grain boundaries, and the understanding of this composite material, which is spatially inhomogeneous, is important both in establishing a basic understanding of device behaviour, and in recognising the limitations of some of the assumptions made in analysing its behaviour. Hence, Sect. 8.2 introduces a classical model of conduction in poly-Si [1]. This could be regarded as a model covering polycrystalline material in general, within which grain boundary states play an important role in trapping free carriers. This is a simple analytical model, which establishes some basic physics and concepts in a readily accessible fashion, even though the simplifications in this model have been superseded by more complex numerical models. This point is developed in Sect. 8.3, which discusses the measurement of the density of states, DOS, in poly-Si, and highlights the issues of distinguishing trapping states within the grains from those in the grain boundary regions.

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Section 8.4 describes the low field leakage current behaviour in TFTs from the standpoint of a classical carrier flow and electron–hole pair generation rate model, and relates this to the quality of the poly-Si.

Section 8.5 discusses other performance issues with poly-Si TFTs, in particular, the effects associated with a high electrostatic field at the drain junction. Firstly, it is demonstrated that this is a two dimensional field, which is controlled by both the voltage on the drain and the gate field. The high field is responsible for hot carrier instabilities, and field enhanced leakage currents, in high quality poly-Si TFTs. The high fields are essentially a device architecture issue, rather than a material quality issue, and the solution to this is found in the relief of the drain field by lightly doped drain regions (LDD), as discussed in Sect. 7.4.1.2. Although the hot carrier damage, discussed in Sect. 8.5.2, is a major reliability issue in n-channel TFTs, there are other instability mechanisms in poly-Si TFTs, which are displayed in other biasing regimes, and these are briefly discussed in Sect. 8.6.

Finally, the current understanding of the performance of short channel TFTs is reviewed in Sect. 8.7, which also deals with the issue of floating body effects in the TFTs.

The understanding of the issues discussed in this chapter has been crucial to their resolution, and, as discussed in Chap. 7, this has facilitated the mass-production of stable, high quality poly-Si TFTs for flat panel display applications.

8.2 Electrical Conduction in Poly-Si

8.2.1 Analytical Bulk Conduction Model

As is readily apparent from electron microscopy images of poly-Si, it is a polycrystalline material, consisting of discrete grains, of variable crystallographic orientation, separated by inter-grain regions. These regions need to accommodate the changes in crystallographic orientation in going from one grain to the next, and, rather like the surfaces of crystalline regions, the interruption to the periodic lattice structure of the grain can be expected to introduce defects states into the forbidden band gap at its surface. In addition, there may also be impurity defect states here. Hence, the grain boundary regions will be regions of structural disorder, and will contain deep level trapping states within the forbidden band-gap. Indeed, many aspects of the performance of poly-Si have been ascribed to carrier trapping effects at the grain boundaries, and the resistivity of doped poly-Si is a good example of this.

Figure 8.1a shows the variation of resistivity with boron concentration in p-type poly-Si, for two different grain sizes, and compares it with single crystal Si [2]. There a number of striking differences between the two types of material. Firstly, in single crystal silicon, the resistivity varies almost inversely with boron concentration, and this is only seen at the higher doping levels in poly-Si, where the

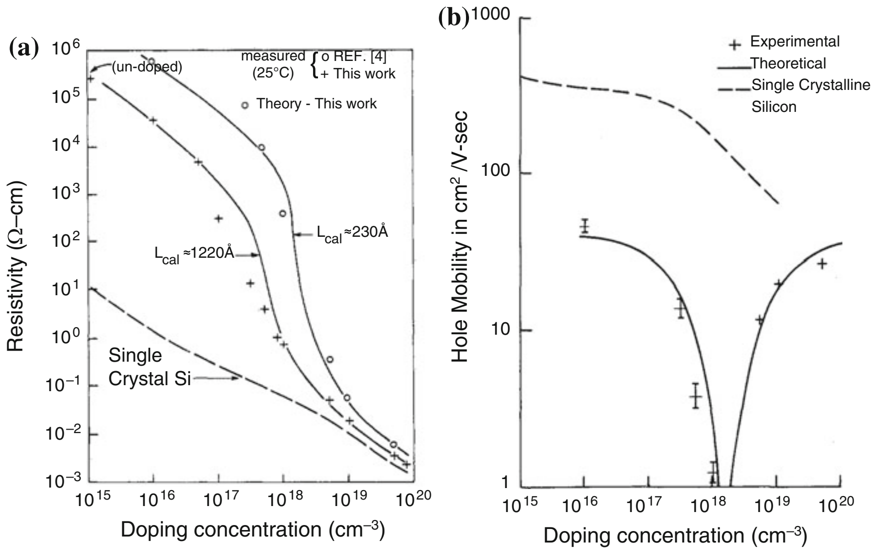

Fig. 8.1 Comparison of parameter dependence on boron doping concentration in poly-Si and c-Si **a** resistivity for two different poly-Si grain sizes (Reprinted from [2] with permission of IEEE), and **b** hole mobility (Reprinted with permission from [1]. Copyright (1975) American Institute of Physics)

resistivity approaches that of c-Si. Secondly, at very low concentrations, the poly-Si resistivity is several orders of magnitude higher than c-Si, and, thirdly, over a narrow range of doping levels, the poly-Si resistivity drops very abruptly. There are also clear differences in the behaviour of the Hall mobility in the two material types, as shown in Fig. 8.1b [1]. Whereas the hole mobility in crystalline Si shows a gradual decrease with increasing doping level, due to increased charged impurity scattering, the Hall-effect hole mobility in poly-Si shows a completely different behaviour, with the mobility falling to a very low value at moderate doping levels, before rising back to a value comparable to c-Si at higher doping levels.

The characteristic behaviour of poly-Si, as shown in Fig. 8.1, has been attributed to carrier trapping in the grain boundaries, GBs, and has been quantitatively described using a simple, analytical model [1]. In this, the material is represented by a combination of trap-free single crystal grain regions, doped with a boron acceptor density N, and separated by planar grain boundary regions containing an areal density, Q_T, of deep donor trapping levels at E_T-E_V, as illustrated in Fig. 8.2. Figure 8.2a shows a single crystal grain of length L, which is separated from the adjacent grains by the grain boundaries. Figure 8.2b shows the charge distribution between the GBs, where the GBs have trapped free holes from the grain. For charge neutrality, the positive trapped charge in the GBs will be balanced by the negative space charge in the regions of length *l* within the grains, where the ionised boron acceptors have lost their holes to the GBs. Hence, to maintain the overall space charge neutrality, the positive charge in the GBs, Q_T^+, will be equal to the

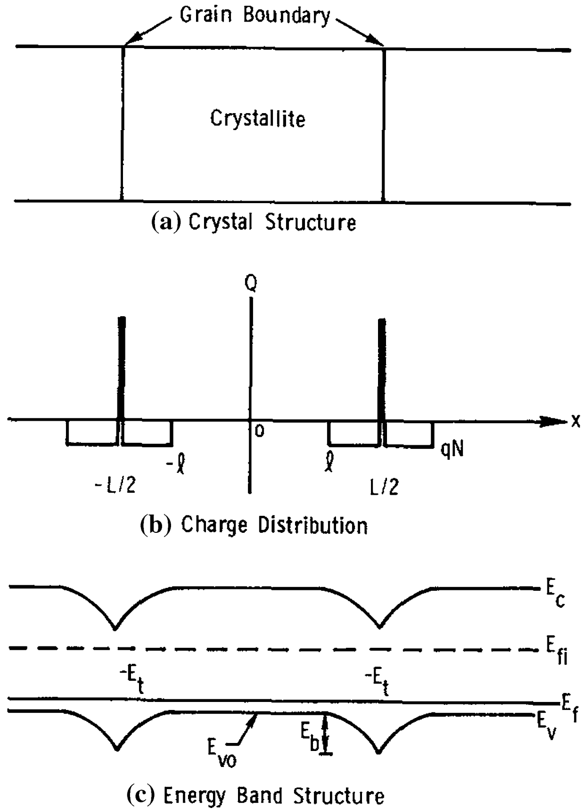

Fig. 8.2 Analytical model for grain boundary effects in poly-Si **a** GB model, **b** space charge distribution, and **c** band diagram, showing band bending (Reprinted with permission from [1]. Copyright (1975) American Institute of Physics)

negative charge, N*l*, in the two space charge regions either side of the GB. The band bending, in Fig. 8.2c, is shown for a particular situation, in which the Fermi level is close to the valence band edge, and beneath the GB trapping level, E_T. This represents a heavily doped grain, and fully occupied hole traps. There is a potential barrier at the GB due to the charge Q_T on the traps, and the compensating depletion region extending partially into the grain by the distance *l*. The band bending in this region can be calculated from Poisson's equation:

$$\frac{d^2V}{dx^2} = \frac{qN}{\varepsilon_0 \varepsilon_s} \tag{8.1}$$

Integrating this twice, and assuming that dV/dx = 0 at *l*, the potential distribution in the grain is:

$$V = \frac{qNx^2}{2\varepsilon_0 \varepsilon_s} \tag{8.2}$$

and the potential barrier height at the GB is:

$$V_b = \frac{qNl^2}{2\varepsilon_0\varepsilon_s} \tag{8.3}$$

For charge neutrality (and using the depletion approximation and zero Kelvin Fermi–Dirac statistics):

$Nl = 0.5Q_T$, and, therefore, the barrier height, V_b, can be expressed as:

$$V_b = \frac{qQ_T^2}{8\varepsilon_0\varepsilon_s N} \tag{8.4}$$

In other words, for partially depleted grains, and fully occupied traps, where $Nl = 0.5Q_T$, the GB barrier height, V_b, diminishes as the grain doping level increases.

However, in the alternative situation, where $Nl < 0.5Q_T$, all the holes are trapped in the partially occupied GB traps, and the grain is fully depleted, giving rise to the high resistivities seen at low doping levels in Fig. 8.1a. In this fully depleted case, $l = L/2$, the Fermi level will be above the trapping level, E_T, and Eq. 8.3 becomes:

$$V_b = \frac{qNL^2}{8\varepsilon_0\varepsilon_s} \tag{8.5}$$

and, for the fully depleted grains, the GB barrier height increases with grain doping level. For very lightly doped grains, V_b is close to zero, and it increases linearly with doping concentration up to a maximum value, $V_{b(max)}$, of:

$$V_{b(\max)} = \frac{qN^*L^2}{8\varepsilon_0\varepsilon_s} \tag{8.6}$$

at the critical doping concentration, N^*, where $N^*L = Q_T$. Hence, $V_{b(max)}$ is a function of both grain size and GB trap state density, and an example of the V_b and $V_{b(max)}$ dependences on N and Q_T is shown, for mid-gap traps, in Fig. 8.3 [3]. It will be appreciated that increments in doping concentration, above the critical dopant level, N*, now start to add an almost equal number of free carriers within the grain, and this, combined with the reducing barrier height, leads to the steep reduction in resistivity, seen in Fig. 8.1a.

An analytical expression for the conductivity of the material [1] was developed by assuming that, when a bias was applied to the poly-Si material, current flow was limited by the motion of carriers over the potential boundary at the GB, rather than by current flow within the grain itself. The maximum carrier flow over the potential barrier is given by thermionic emission, which is independent of the shape of the potential barrier and is determined only by its height. For simplicity, this mechanism was assumed, where the current density, J_{th}, is given by the number of carriers moving towards the GB with energies sufficient to overcome the potential barrier [4], and a general expression for the thermionic emission current over a barrier of height Φ_b is:

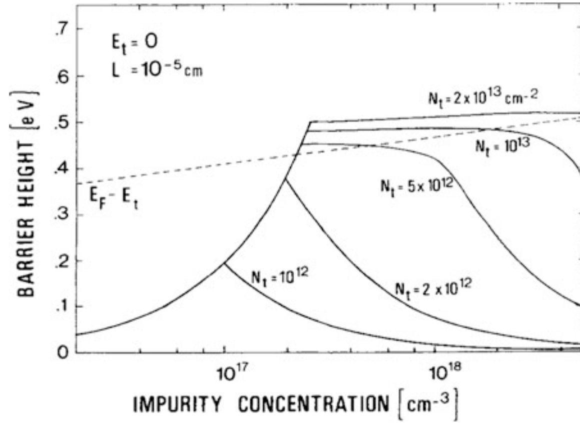

Fig. 8.3 Calculated variation, with doping concentration, of the potential barrier height at a grain boundary. The calculations are for different concentrations, N_t, of a discrete grain boundary trap at mid-gap (Reprinted with permission from [3]. Copyright (1978) American Institute of Physics)

$$J_{th} = qnv \exp\left(-\frac{q\Phi_b}{kT}\right)\left(\exp\frac{qV_a}{kT} - 1\right) \tag{8.7}$$

where, v is the carrier's thermal collection velocity (= $\{kT/2\pi m^*\}^{0.5}$) [5], n is the carrier concentration at the bottom of the barrier, m* is its effective mass, and V_a is the potential drop across the barrier.

In using this expression, the carrier density employed by Seto [1] was the average number, P_a, in the grain, which was calculated by integrating the free hole distribution, p(x), across the grain, and dividing it by L. For a fully depleted grain, p(x) is given by:

$$p(x) = N_V \exp\left[-\left\{qV(x) - E_f\right\}/kT\right] \tag{8.8}$$

and P_a is:

$$P_a = \frac{n_i}{Lq}\left(\frac{2\pi\varepsilon_s\varepsilon_0 kT}{N}\right)^{1/2} \exp\left(\frac{E_b + E_f}{kT}\right) erf\left[\frac{qL}{2}\left(\frac{N}{2\varepsilon_s\varepsilon_0 kT}\right)^{1/2}\right] \tag{8.9}$$

where $E_b = qV_b$, and n_i is the intrinsic carrier concentration. The Fermi level, E_f, is determined by the following equality:

$$NL = \frac{Q_T}{1 + 2\exp\left[\left(E_T - E_f\right)/kT\right]} \tag{8.10}$$

For partially depleted grains, the carrier concentration, p_b, in the undepleted region is approximately equal to N in non-degenerate samples, and is related to the Fermi level by:

$$p_b = N_V \exp -\left(E_f/kT\right) \tag{8.11}$$

The average concentration, P_a, of the un-depleted and fully depleted regions is [1]:

$$P_a = p_b \left\{ \left(1 - \frac{Q_T}{LN}\right) + \frac{1}{qL}\left(\frac{2\pi\varepsilon_s\varepsilon_0 kT}{N}\right)^{1/2} erf\left[\frac{qQ_T}{2}\left(\frac{1}{2\varepsilon_s\varepsilon_0 kTN}\right)^{1/2}\right]\right\} \quad (8.12)$$

From Eq. 8.7, the thermionic emission current, J_{th}, for a voltage V_a applied across a grain boundary, and where $V_b > kT$, is [1]:

$$J_{th} = qP_a\left(\frac{kT}{2\pi m^*}\right)^{1/2} \exp\left(-\frac{qV_b}{kT}\right)\left[\exp\left(\frac{qV_a}{kT}\right) - 1\right] \quad (8.13)$$

and, if $qV_a \ll kT$, Eq. 8.13 reduces to:

$$J_{th} = q^2 P_a\left(\frac{1}{2\pi m^* kT}\right)^{1/2} \exp\left(-\frac{qV_b}{kT}\right) V_a \quad (8.14)$$

The conductivity, σ, of a material is related to the current density, J, and the electric field, E, by $J = \sigma E$, so, the poly-Si conductivity can be evaluated from Eq. 8.14 together with Eqs. 8.9 or 8.12:

$$\sigma = Lq^2 P_a\left(\frac{1}{2\pi m^* kT}\right)^{1/2} \exp\left(-\frac{qV_b}{kT}\right) \quad (8.15)$$

and from $\sigma = qp\mu$, the effective carrier mobility, μ_{eff}, is given by:

$$\mu_{eff} = Lq\left(\frac{1}{2\pi m^* kT}\right)^{1/2} \exp\left(-\frac{qV_b}{kT}\right) \quad (8.16)$$

Hence, as V_b goes through a maximum with doping level, the effective mobility goes through a minimum, as shown in Fig. 8.1b. A generic version of this equation,

$$\mu_{eff} = \mu_0 \exp\left(-\frac{qV_b}{kT}\right) \quad (8.17)$$

is also often used to relate the poly-Si field effect mobility to an assumed GB barrier height in the TFT channel [5, 6].

Using Eqs. 8.15 and 8.16 (together with some scaling parameters), the model was successfully fitted to the resistivity and Hall-effect mobility data by Seto [1]. Examples of these fits by Lu et al. [2] and Seto [1] are shown by the solid lines in Fig. 8.1a and b, respectively. (The scaling parameters are discussed in Sect. 8.2.3). Hence, this simple analytical model, based upon local carrier trapping at grain boundaries, and the associated potential barriers in the valence band, encompassed the essential features of the experimental data. It offered an explanation for the high resistivity of lightly doped poly-Si, the sharp fall in resistivity at a critical

doping level, the asymptotic approach to c-Si data at high doping levels, and the anomalous behaviour of the Hall-effect hole mobility.

The above analysis has been based upon p-type doping of poly-Si, together with GB-associated deep donor traps, and the induced potential barriers in the valence band edge. The essential features of the model have been shown to apply equally well to n-type doped poly-Si, in which potential barriers arise in the conduction band edge due to electron trapping at deep acceptor levels in the upper half of the band gap [3].

8.2.2 Analytical Model of TFT Conduction

The key features of the bulk conduction model have also been used to produce an analytical model for conduction in poly-Si TFTs, in which the dependence of the barrier height on doping level has been replaced by an equivalent dependence upon the carrier density induced in the channel by the gate voltage [5]. In the same way as in the Seto model, this model also assumed discrete trapping levels for the GBs, and thermionic emission over the potential barriers at the band edges. An expression was derived for the channel current as a function of gate voltage, in which the gate voltage controlled the carrier density in the channel, and, hence, the height of the potential barriers at the GBs [5]:

$$I_d = \frac{\mu_0 W C_{ox} V_G V_d}{L} \exp - \left(\frac{q^3 Q_T^2 t_i}{8 \varepsilon_s \varepsilon_0 k T C_{ox} V_G} \right) \tag{8.18}$$

W, L are TFT channel width and length, respectively, V_G and V_d are gate and drain biases, respectively, C_{ox} is the gate oxide capacitance, and t_i is the inversion layer thickness (giving the equivalent volume charge density in the channel from $C_{ox}V_G/t_i$). The barrier height term in Eq. 8.18 corresponds to Eq. 8.4, which described the potential barrier at a GB in a partially depleted grain. Also, in this expression, the mobility term, μ_0, was given by qLv/kT (where v was the carrier's thermal collection velocity), and this retained the thermionic emission criterion.

Equation 8.18 can be used to analyse experimental TFT transfer characteristics, by plotting $\ln(I_d/V_G)$ versus $1/V_G$, as shown by the inset in Fig. 8.4, from which, the slope gives Q_T, and the intercept gives μ_0. This plot is from a 2-D simulation of TFT transfer characteristics, with 0.5 μm long grains, and mid-gap traps at the GBs [7], and similar experimental data plots have been published by Levinson et al. [5], and by many other authors. The range of V_G values (within which the plot was linear) was from ~4.5 to 7 V, which corresponded to the sub-threshold/near-threshold current regime, where the increase in channel current was ascribed, by the model, to the reduction in GB-barrier height. For this particular simulation, Q_T could be correctly calculated to be 2×10^{12} cm^{-2}, by taking the inversion layer thickness, t_i, to be 34 nm [7]. However, this value will generally not be

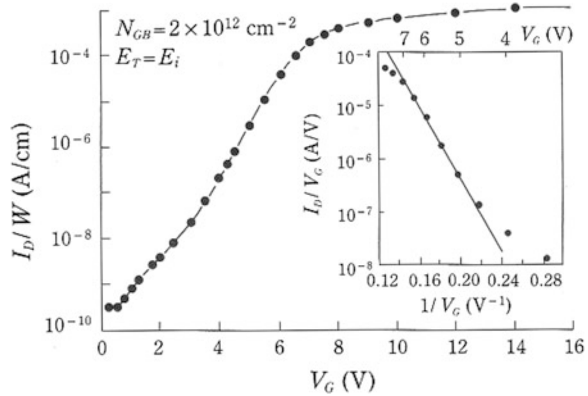

Fig. 8.4 Calculated transfer characteristic of a TFT containing 0.5 μm long grains, with a mid-gap trap at the GB. The inset is a Levinson plot of $\ln(I_d/V_G)$ versus $1/V_G$. (Reprinted from [7])

known experimentally, and this introduces an unavoidable numerical uncertainty in using this technique.

8.2.3 Limitations of Analytical Model

As will be shown in Sect. 8.3, contemporary evaluations of the density of states, DOS, in poly-Si TFTs show a continuous distribution of trapping states across the band gap. Hence, the assumption of just a discrete trapping level is a major simplification, which fails to reflect the true nature of poly-Si, and the value of Q_T extracted from the analytical TFT analysis [5] will be an artefact of this assumption. However, as shown by Fig. 8.5, one of the key features of the model is retained with a distributed DOS [3], namely, the initial increase in GB barrier height with increasing doping level, and then a reduction in height once a critical doping level was exceeded. In this case, the critical doping density, N^*, occurred,

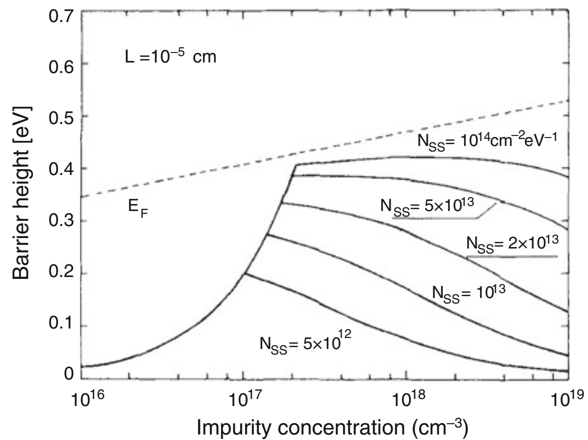

Fig. 8.5 Calculated variation, with doping concentration, of the potential barrier height at a grain boundary. The calculations are for different concentrations of GB traps uniformly distributed across the band-gap. (Reprinted with permission from [3]. Copyright (1978) American Institute of Physics)

for a uniform trap distribution, $N_{GB}(E)$, when the total space charge in the grain, N*L, was equal to the integral of the trapped charge in the distributed GB states, and this equality could be expressed as [3]:

$$N^* = \left(\frac{N_{GB}}{L}\right)\left(1 + \frac{q^2 N_{GB} L}{8\varepsilon_s \varepsilon_0}\right)^{-1} kT \ln\left(\frac{N^*}{n_i}\right) \tag{8.19}$$

which needs to be solved iteratively for N^*.

The other simplifications have been, firstly, the assumption of thermionic emission, as opposed to drift/diffusion carrier transport, and, secondly, the nature of the GB region itself, and whether it is adequately represented by a planar boundary [8]. These issues were raised, in part, by the scaling factors used to fit Eq. 8.15 to the experimental data [1, 8]. The added scaling factors were a pre-exponential term, f, and an ideality factor, n, giving the modified conductivity equation:

$$\sigma = fLq^2 P_a \left(\frac{1}{2\pi m^* kT}\right)^{1/2} \exp\left(-\frac{qV_b}{nkT}\right) \tag{8.20}$$

where f was 0.12 and n was 6.49. It was shown in this later work [8] that, by treating the GB region as an a-Si-like region of ~1–2.5 nm width, with band-tail and deep states, there was trap-limited conduction in this region. Hence, the material's conductivity was not merely limited by transport both within the grains and across the potential barriers at the GBs, but account also had to be taken of transport within finite width grain boundary regions themselves. By adding these further considerations, including drift/diffusion flow over the potential barriers, it was possible to fit the experimental data in Fig. 8.1a, without the arbitrary fitting factors, f and n, used in the earlier work [8].

In spite of these detailed qualifications to the bulk conduction model of Seto [1], its TFT equivalent, Eq. 8.18 [5], has continued to be widely used in many publications to analyse the poly-Si TFT characteristics, and to extract a GB trapping state density, Q_T. In view of the above limitations in the basic model, and the particular problem of knowing the inversion layer thickness, t_i, in Eq. 8.18, the extracted Q_T values should be taken more as a figure of merit for the TFT, rather than as an accurate estimate of the trapping state density associated with the GB region.

8.3 Poly-Si Density of States, DOS

Section 8.2 introduced the role of GB trapping states in explaining the behaviour of bulk poly-Si resistors, and briefly discussed the extension of a simple analytical model [1] to analysing TFT behaviour [5]. This section continues that discussion by looking, more broadly, at the evaluation of the poly-Si DOS, but without the limitations imposed by the simplifications in the analytical model. In general

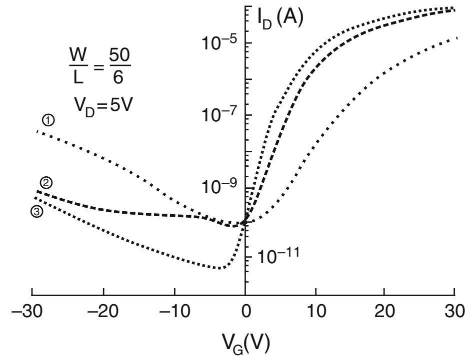

Fig. 8.6 Small grain poly-Si TFT transfer characteristics measured after different exposures times to a hydrogen plasma: (*1*) 0 h, (*2*) 0.5 h, (*3*) 4 h. The increasing exposure times produced reducing densities of states across the band-gap. (Reprinted from [9] Copyright (1991), with permission from Elsevier)

terms, the overall performance of poly-Si TFTs is affected by states within the forbidden band-gap: those near the centre contributing to leakage current, whilst those close to the band-edge will reduce the field effect mobility from the band value, and states in between will determine the sub-threshold slope and threshold voltage. These dependences are illustrated in Fig. 8.6, for a set of poly-Si TFTs, whose different DOS levels were determined by different exposure times to an atomic hydrogen passivation process [9]. Comparing the TFT with zero exposure time (and high DOS) to the device with 4 h exposure (and low DOS), the latter had a higher on-current, lower off-current, lower threshold voltage and smaller sub-threshold slope. The Levinson analysis [5] showed a reduction in effective GB trapping state density from 2.7×10^{12} cm^{-2} to 1.0×10^{12} cm^{-2}, although, as discussed in Sect. 8.2.2, these absolute values are subject to some numerical uncertainty, but the relative change is a more reliable indicator of the overall change in DOS.

Given the limitations of the Levinson analysis, many authors have used a variety of more sophisticated techniques to analyse the TFT characteristics, in order to extract the distribution of trapping states [10–15]. In these analyses, it has also been recognised that certain forms of poly-Si, such as the large faulted grain material produced by the SPC process, are likely to have defects states within the grains themselves, and not merely at the grain boundaries [10, 14]. In addition, the assumption of mono-energetic trapping states was relaxed, and the DOS was evaluated across the back-gap. The techniques have included 1-D analysis of the field-effect conductance, obtained from the TFT transfer characteristic [10], the measurement of the temperature dependent emission of electrons from the traps, using deep level transient spectroscopy [11], or, more commonly, 2-D numerical simulations to reproduce the transfer characteristic [12–15]. From this work, there is a general consensus that there is a continuous distribution of trapping states across the band-gap [10–15], as shown in Fig. 8.7 [12], and this is frequently represented by a double exponential distribution of states in each half of the band-gap:

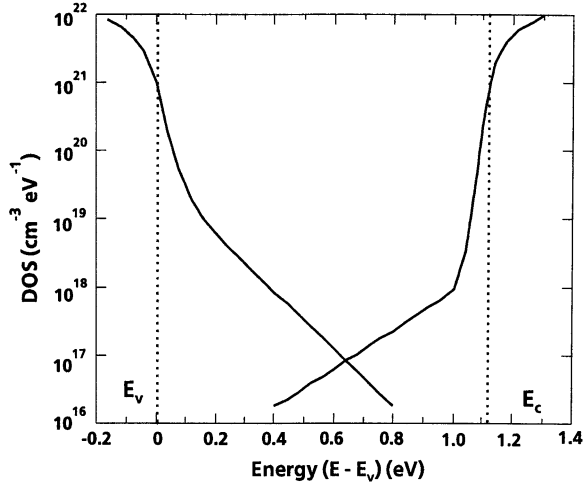

Fig. 8.7 Calculated poly-Si DOS, obtained from a 2-D simulator fit to experimental transfer characteristics (Reprinted with permission from [12]. Copyright (1990) The Japan Society of Applied Physics)

$$N(E) = N_T \exp -\frac{E}{E_T} + N_D \exp -\frac{E}{E_D} \tag{8.21}$$

where N_T and N_D are the band-edge concentrations of tail and deep states, respectively, and E_T and E_D are the characteristic energy widths of these states. The same expression is used for both the acceptor states in the upper half of the band-gap and the donor states in the lower half of the band-gap, although the individual parameter values are usually different in the two halves of the band-gap. The total densities, integrated across the band-gap, are given by N_TE_T and N_DE_D, for the tail-states and deep states, respectively.

However, a persistent problem in uniquely determining the DOS in poly-Si has been the difficulty in distinguishing between trapping states within the grains and trapping states at the grain boundaries. This is because the conventional poly-Si grain size is smaller than the typical TFT channel dimensions, and device measurements always yield an effective trapping state density per unit gate area, which can be attributed to an equivalent density of charges trapped in the grains and/or in the GBs. Some authors have attempted to partition the distribution between these two sites [14, 15], whilst others have used a spatially uniform effective density of states [12, 13] (which is also more computationally efficient, as it requires fewer mesh lines within the model). In all these cases, justification for the assumed distributions was based upon demonstrating a good fit of the model to experimental transfer characteristic data. However, with the large number of adjustable parameters in these simulations, and the different underlying assumptions, the question of an unambiguous characterisation of inter-grain and intra-grain defects remained unresolved.

As with the poly-Si resistor analysis, a further problem is the appropriate representation of the grain boundary itself, either as a planar, 2-D distribution of defects, or as a thin disordered, 3-D region of defects between the grains.

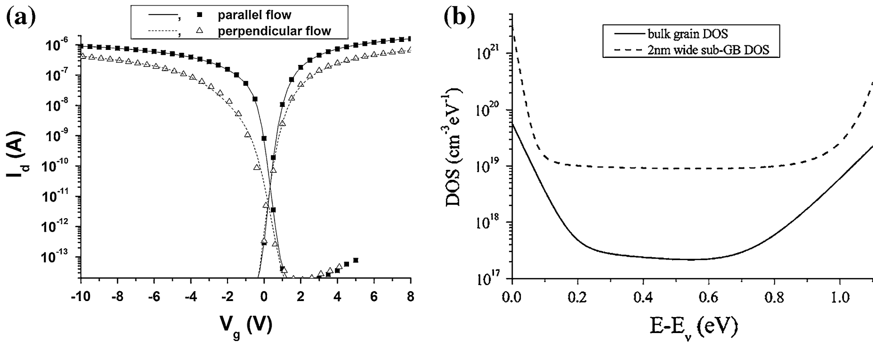

Fig. 8.8 **a** Experimental (*symbols*) and fitted (*lines*) data to SLS poly-Si transfer characteristics, for carrier flow parallel and perpendicular to the sub-GBs in the SLS material, **b** in-grain and GB DOS extracted from the SLS material (Reprinted with permission from [16]. Copyright (2007) American Institute of Physics)

Recent work using long-grain SLS poly-Si has addressed these problems, by exploiting the anisotropic nature of this material (as discussed in Sect. 7.5.2.1), in which the grain size in one direction exceeded the channel length [16]. In that work, the carrier flow parallel to the sub-GBs ($\mu_n = 218$ cm^2/Vs) was assumed to be controlled only by states within the grains, whereas carrier flow orthogonal to the sub-GBs ($\mu_n = 76$ cm^2/Vs) was assumed to be controlled by both the in-grain states as well as by the GB states. Hence, by using data from orthogonal TFTs, the in-grain DOS could be separated from the GB DOS. The temperature dependent transfer characteristics were measured in these two directions, and 2-D simulations of the transfer characteristics and their activation energies were used to establish the DOS for the intra-grain and inter-grain states [16]. The fitted characteristics, measured at 324 K, are shown in Fig. 8.8a, and, to obtain a consistent fit across the range of measurement temperatures, the GB states could not be treated as a 2-D planar distribution of defects, but had to be treated as a 2 nm wide, thin disordered region. This was because, in spite of the mobility differences for parallel and perpendicular flow remaining constant into strong inversion, the activation energy for perpendicular flow was close to zero. Such a small activation energy was not consistent with a GB barrier height large enough to produce the observed mobility difference (Eq. 8.17 predicted a barrier height of 27 meV at 295 K). Within the narrow GB region, the fitted DOS determined the carrier density, and, hence, the resistive current flowing through that region. This resistive current flow was the limiting transport mechanism in the TFT, and was also characterised by a near-zero activation energy, in agreement with the experimental data. The resulting DOS distributions for the in-grain and the GB states are shown in Fig. 8.8b. As with the earlier evaluations, such as in Fig. 8.7, the distribution of both types of states was continuous across the band-gap, with an exponential-like distribution near the band-edges. The results in Fig. 8.8b also demonstrated that there was a much higher integrated volume density of traps within the GB region than in the

grains themselves: for the band-tail states, in the upper half of the band gap, the densities were 7.7×10^{18} cm^{-3} and 1.7×10^{18} cm^{-3} respectively, and the deep state densities were ~50 times larger in the GBs. However, the 2 nm width of the GB region, L_{GB}, compared with the 300 nm grain size, L_G, meant that the total density of GB states per unit surface area of the film (3.4×10^{11} cm^{-2}) was only ~5 % of the equivalent density within the grains (7.2×10^{12} cm^{-2}), where the density per unit surface area, N_{SA}, of GB states, N_{GB}, is given by:

$$N_{SA} = \frac{N_{GB} t_f L_{GB}}{L_{GB} + L_G} \tag{8.22}$$

and t_f is the film thickness.

The detailed analysis of the sub-GB defects in the SLS poly-Si TFTs was consistent with the analysis of conduction in poly-Si resistors [8], which avoided the use of fitting factors, and demonstrated that the results could be most satisfactorily explained by assuming that the GB region was a narrow disordered region, rather than a 2-D plane of defects. Thus, the transport of carriers within this region determined the overall conductivity of the material, rather than the emission of carriers over the potential barrier at the GBs.

In some TFT simulation work [16, 17], the temperature and field dependence of the carrier mobility has been incorporated into the 2-D models by using functions developed for c-Si simulations such as the Canali [18] and Lombardi [19] formulations. In particular instances, such as the simulation of long channel length TFTs [17], the incorporation of the transverse field dependence of the mobility has been essential for the accurate reproduction of the mobility variation with gate bias at large gate biases.

8.4 TFT Off-State Currents

The basic electron–hole pair generation process has been discussed in Chap. 2, and this process, plus the transport of the generated carriers to the contacts, will be used to examine the leakage current behaviour observed in poly-Si TFTs. Experimentally, the leakage current is found to be very dependent upon the magnitude of the field at the drain junction, and low field and high field regimes can be readily distinguished. The former is governed by the field-independent generation processes described in Chap. 2, whilst the latter is determined by field-enhanced emission processes. The low-field generation process will be described in this section, using a simple analytical model to give physical insight into the process, and the high field process will be covered in Sect. 8.5.3, which groups together other drain field dependent processes.

The transfer characteristics, from a range of different channel length TFTs, are shown in Fig. 8.9a–c for different DOS levels. From a leakage current perspective,

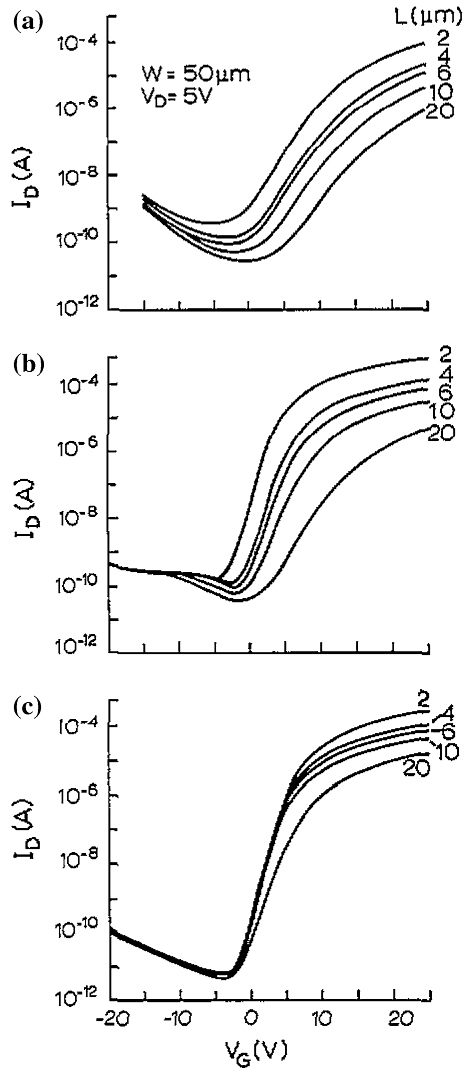

Fig. 8.9 Channel length dependent transfer characteristics for poly-Si TFTs with different DOS levels, after varying degrees of plasma hydrogenation **a** zero, **b** partial, and **c** full hydrogenation (Reprinted from [20], with permission from IOP Publishing Ltd)

the major difference between curves Fig. 8.9a and c, apart from the absolute values of current, is that the leakage current was channel length dependent in the high DOS case, whereas, in the low DOS case, the leakage current was independent of channel length [20]. The corresponding I_D-V_D leakage current curves, for different values of V_G, are shown in Fig. 8.10a–c, for 10μm or 6μm channel length TFTs. For the high DOS devices in Fig. 8.10a, the minimum current varied inversely with channel length [9], and the I_D-V_D curve was linear, suggesting a resistive, or a drift-limited, current flowing through a non-rectifying contact. For the medium DOS device in Fig. 8.10b there was resistive current flow at low V_D, which saturated into a quadratic current at higher V_D, and the applied voltage, at which

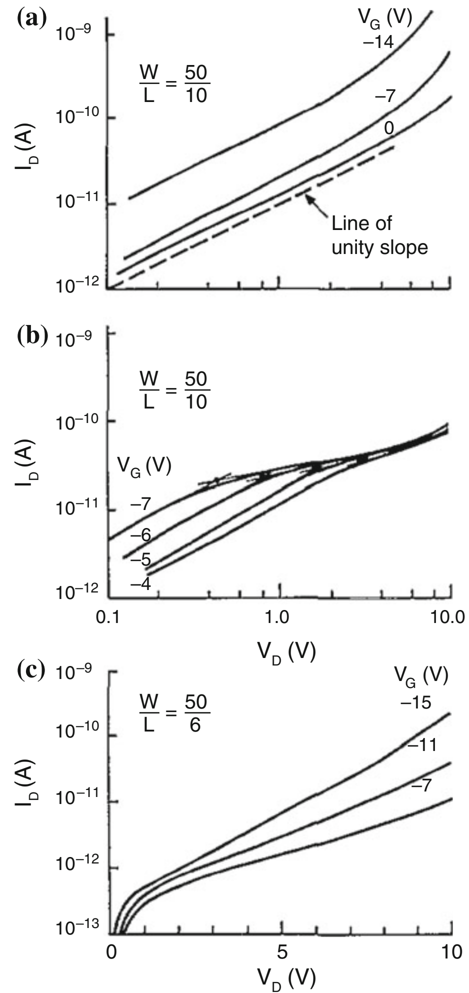

Fig. 8.10 Gate and drain bias dependent leakage current characteristics for poly-Si TFTs with different DOS levels, after varying degrees of plasma hydrogenation **a** zero, **b** partial, and **c** full hydrogenation. (Reprinted from [20], with permission from IOP Publishing Ltd)

this occurred, reduced with increasing negative gate bias. Finally, for the lowest DOS device in Figs. 8.9c and 8.10c, the channel length independence and the exponential increase in current with both V_G and V_D indicates a field enhanced generation current. The leakage current mechanism, displayed in Fig. 8.10a and b, is described below by a simple analytical n^+p junction model [9], and the field enhanced current is analysed in Sect. 8.5.3.

The model used for the low-field currents in Fig. 8.10a and b is shown in Fig. 8.11, in which there is electron–hole pair generation in the drain space charge region, supported by the voltage dropped across this region, V_{gen}, and resistive hole flow to the source junction, causing a voltage drop, V_R, across the neutral

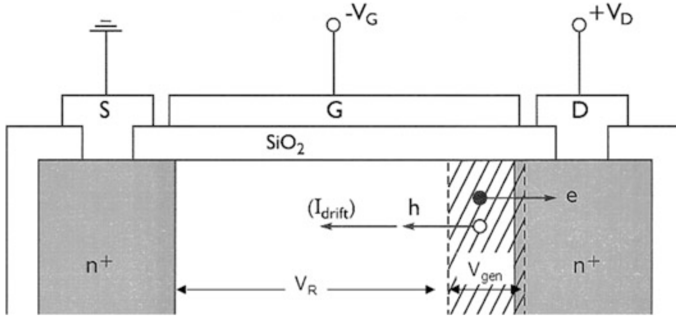

Fig. 8.11 Cross sectional diagram of TFT, showing carrier generation, voltage distribution, and leakage current paths

portion of the transistor body. From Chap. 2, the generation current, J_{gen}, is given by:

$$J_{gen} = \frac{qn_i x_D}{\tau} \tag{8.23}$$

and the drift current, J_R, is given by:

$$J_R = q(n\mu_n + p\mu_p)F \approx q\alpha p_i \mu_p F \tag{8.24}$$

assuming that $p = \alpha p_i = \alpha n_i$ and that $\alpha > 1$ for negative gate biases, where there will be surface accumulation of holes (n_i and p_i are the intrinsic carrier concentrations). The field, F, in the transistor body is given by:

$$F = \frac{V_R}{L - x_D} \tag{8.25}$$

where, from Chap. 2, the space charge width, x_D, is:

$$x_D = \sqrt{\frac{2\varepsilon_s \varepsilon_0 V_{gen}}{qN_T}} \tag{8.26}$$

$$V_D = V_{gen} + V_R \tag{8.27}$$

$$J_{gen} = J_R = J_D \tag{8.28}$$

Therefore,

$$J_D = \frac{-L + \sqrt{L^2 + 4qn_i\alpha\mu_p V_D\left(\frac{N_T\alpha\mu_p\tau^2}{2\varepsilon_s\varepsilon_0 n_i} - \frac{\tau}{qn_i}\right)}}{2\left(\frac{N_T\alpha\mu_p\tau^2}{2\varepsilon_s\varepsilon_0 n_i} - \frac{\tau}{qn_i}\right)} \tag{8.29}$$

Whilst Eq. 8.29 has been fitted to experimental data [9], it is more instructive to look at the predictions of this equation, and to compare it to the general form of the

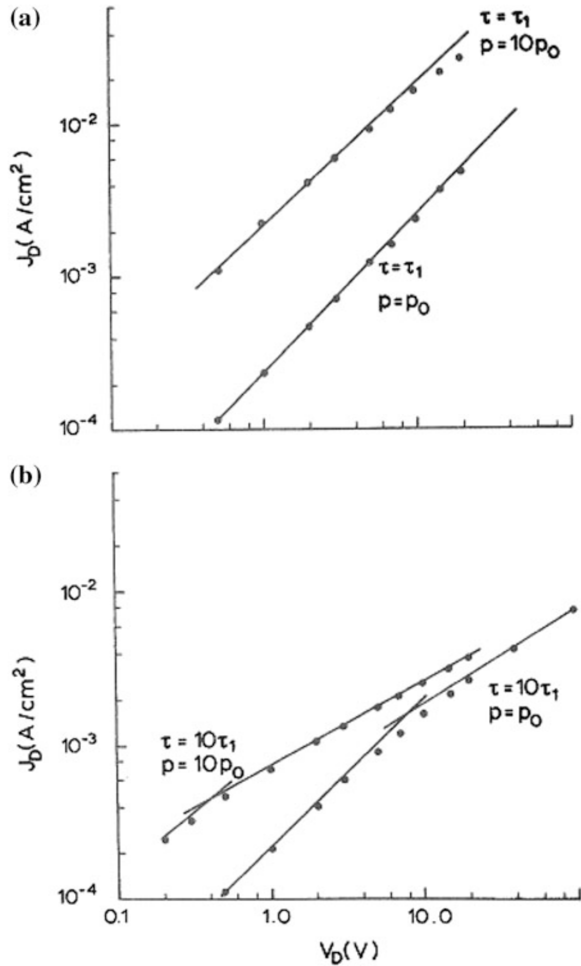

Fig. 8.12 Calculated leakage current curves, J_D-V_D, using Eq. 8.29 **a** low generation lifetime case, $\tau_1 = 10^{-11}$s, and **b** higher lifetime, $\tau = 10\tau_1$ (Reprinted from [9] Copyright (1991), with permission from Elsevier)

data in Fig. 8.10a and b. Some representative calculations are shown in Fig. 8.12a and b, using the parameter values shown in the figure caption. The curves in Fig. 8.12a have been calculated with a low value of the carrier generation lifetime, corresponding to a high DOS near mid-gap, and for two different values of the hole concentration, corresponding to two different degrees of hole accumulation. Under these conditions, the I_D-V_D characteristics are linear, and increasing the hole concentration by a factor of ten increases the current by the same amount. These curves are similar to the experimental ones in Fig. 8.10a. In this case, the junction is not rectifying because the potential electron–hole pair generation rate is so high, that the current flow through the device is not limited by this generation process, but by the transport of holes to the source junction (where it is implicitly assumed that they recombine with electrons). Hence, there is drift-limited conduction, and the resistive current is simply determined by the hole concentration in the film.

In contrast, the curves in Fig. 8.12b were calculated with a ten times higher generation lifetime, and showed the same general form as the experimental data in Fig. 8.10b. The curves had a linear I_D-V_D characteristic only at low values of V_D, and, eventually, the slope reduced to 0.5, when the current became generation rate limited. The slope of 0.5 occurred because the increase in size of the space charge region, within which generation took place, increased only with the square root of V_D, as shown in Eq. 8.26. In this case, the higher lifetime reduced the carrier generation rate, and, as V_D increased, the holes were swept away at an increasing rate, until the generation rate at the drain could not sustain this current flow. When this happened, the current became limited by the generation rate at the drain. It will also be seen that when the hole concentration increased by a factor of ten, the transition from a drift-limited to a generation-limited current occurred at a lower value of V_D. This is because, with the higher hole concentration, there was initially a 10 times higher drift current, which had to be sustained by the generation rate at the drain; but, as V_D increased, the generation rate quickly became insufficient to supply this increasingly large current, and the process became generation rate limited at the lower value of V_D.

As seen above, the simple analytical model in Eq. 8.29 provides physical insight into the low-field leakage current behaviour of poly-Si TFTs, and it can be used to explain the bell-shaped leakage current curves of ELA poly-Si TFTs, as discussed in Sect. 7.2.2.3 and shown in Fig. 7.8. The leakage current curves, as a function of ELA energy density, for L = 6 μm and L = 60 μm TFTs, from a 40 nm thick film [21], are shown in Fig. 8.13. These display the bell-shape already referred to, and, at low ELA energies, the currents scaled inversely with channel length, but were almost independent of channel length at high laser energies. This indicates that, at low energies, and high DOS, the leakage currents were drift-limited, and at high energies, and low DOS, became generation rate limited. In order to model this transition with Eq. 8.29, it is necessary to use the changing

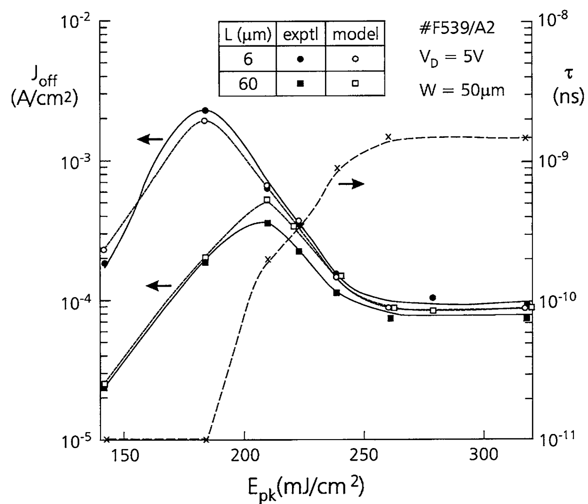

Fig. 8.13 Experimental and modelled (Eq. 8.29) leakage current characteristics, as a function of TFT channel length and ELA energy density, using the generation lifetime, τ, as the adjustable parameter (Reprinted from [21] Copyright (1999), with permission from Elsevier)

values of measured hole mobility as the ELA energy density increased, and this was done in the fitted curve in Fig. 8.13. In fitting this curve to the data, the generation lifetime, τ, was an adjustable parameter, and the values plotted against the right hand axis show, as expected, a monotonically increasing lifetime with increasing ELA energy density. Hence, the initial rise in leakage current with energy density was due to the increasing carrier mobility in the drift-limited arm of the curve, but, at the same time, the generation lifetime was increasing with energy density, leading eventually to a transition to generation-limited currents. Once the current became generation rate limited, it fell with increasing energy density as the lifetime increased due to the reduced DOS in the high quality, optimally crystallised material.

8.5 Performance Artefacts and Drain Field

Three major performance artefacts have been identified even in low DOS, high quality poly-Si TFTs, and these have been associated with high drain fields in the devices. Firstly, the off-state current increases exponentially with both gate and drain bias, as seen in Figs. 8.9c and 8.10c, respectively. Secondly, n-channel TFTs are subject to drain bias stress instability, as shown in Fig. 8.14, and, finally, the output characteristics show poor current saturation, as seen by the insert in

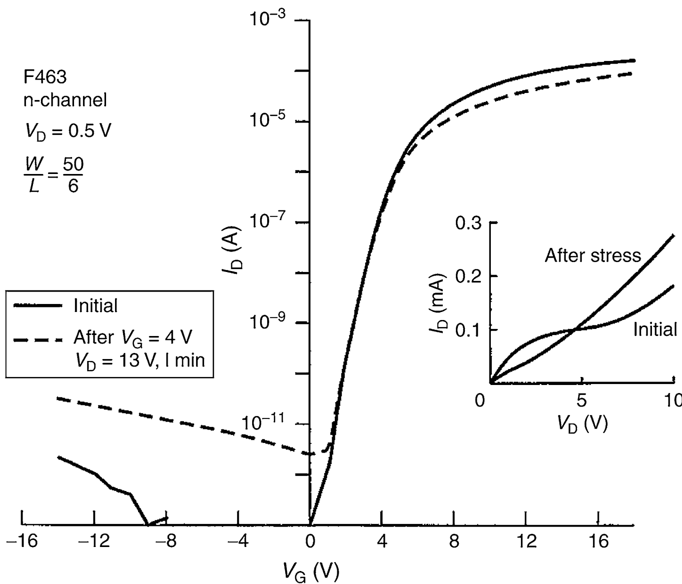

Fig. 8.14 Influence of drain bias stress of 13 V for 60 s on NSA TFT transfer characteristic. The insert shows its effect upon the output characteristic (Reprinted with permission from [24]. Copyright (1998) The Japan Society of Applied Physics)

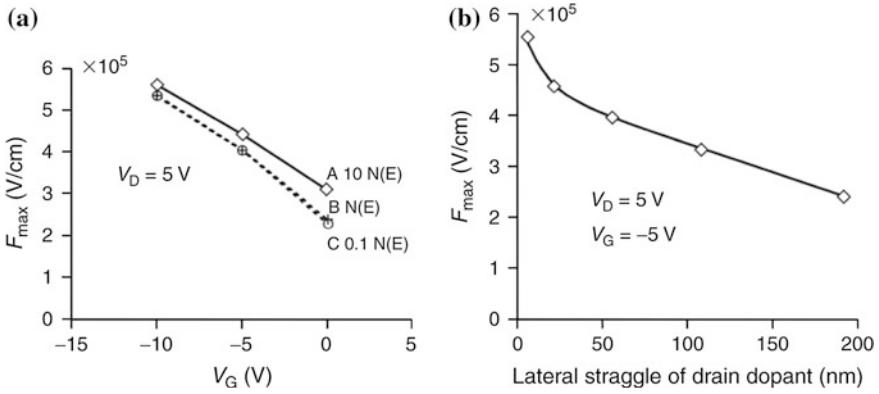

Fig. 8.15 Simulations of the maximum field at the drain/channel junction as a function of **a** gate bias and poly-Si DOS (56 nm lateral dopant spread), and **b** lateral spread of drain dopant. (The DOS, N(E), gave a TFT with a sub-threshold slope, S, of 1 V/dec). (Reprinted with permission from [22]. Copyright (1996) American Institute of Physics)

Fig. 8.14. The details of the instability process and the leakage current effects are discussed further in Sects. 8.5.2 and 8.5.3, respectively, whilst the electrostatic drain field itself is discussed in Sect. 8.5.1.

8.5.1 Electrostatic Drain Field, F

The 2-D electrostatic field in the space charge region of a semiconductor junction is given by Poisson's equation, which relates the space charge density, N_{sc}, and field, F:

$$\frac{\partial F_x}{\partial x} + \frac{\partial F_y}{\partial y} = -\frac{qN_{sc}}{\varepsilon_s \varepsilon_0} \tag{8.30}$$

Using a 2-D simulator, evaluation of this expression, for poly-Si TFTs, showed that the differential terms were opposite in sign, and both were much larger than the space charge term on the right side, such that their difference was only ~10–20 % of their absolute values [22]. Thus, the internal electrostatic field was not controlled by the poly-Si density of states, DOS, as it would be in a 1-D analysis. This is shown in Fig. 8.15a, in which the maximum drain field was calculated as a function of gate bias, with the poly-Si DOS as a scaled independent parameter [22]. In this diagram, the different DOS values produced sub-threshold slopes of 3.0, 1.0 and 0.3 V/dec in the simulated TFT transfer characteristics (for a gate oxide thickness, t_{ox}, of 0.15μm). To put those slopes into context, a high quality poly-Si TFT would have a sub-threshold slope of 0.4 V/decade for this oxide thickness. Therefore, for TFTs of practical interest, with a sub-threshold

slope of < 1 V/dec, the DOS would have no significant effect upon the drain field in the off-state and sub-threshold regime, although there was a weak dependence of drain field on trap state density at large positive V_G, when the device was turned on [24]. However, as shown in the next section, the on-state hot carrier degradation was, nevertheless, greater in the low DOS device.

The simulations showed that the drain field was a 2-D effect, and was determined primarily by the combined effects of the drain and gate biases, the oxide thickness, and the lateral distribution of the drain dopant at its edge [22, 24]. This latter point is shown in Fig. 8.15b, demonstrating that the more abrupt the junction is, the greater is the peak field. The 2-D dependence upon gate bias and oxide thickness meant that, as the transverse gate field increased, so did the lateral drain field, so that, for example, reducing the oxide thickness will increase the drain field.

Because of the significance of the lateral dopant distribution, the drain field in NSA TFTs decreases with increasing ELA shots (due to lateral diffusion of the drain dopant) [23], and, equally, the drain field in SA TFTs is likely to be larger than in NSA TFTs (due to reduced lateral diffusion in the former).

As the poly-Si quality itself had little effect upon the magnitude of the drain field, a change in architecture was required to produce a greater lateral dopant spread, and this is most readily accomplished through the use of lightly doped drain (LDD) regions, the fabrication of which was discussed in Sect. 7.4.1.2. It is worth noting that similar high drain field effects occur in MOSFETs, and these also routinely incorporate LDD regions for field relief.

8.5.2 Hot Carrier Damage and LDD

The high drain field, combined with the high electron mobility, leads to carrier heating and the generation of additional electron–hole pairs by impact ionisation. These additional carriers contribute to the poor saturation of the output characteristics of poly-Si TFTs, and to the so-called 'kink' effect when the impact ionisation-induced avalanche currents ultimately dominate the current flow [25, 26]. The impact ionisation, underlying the 'kink' effect, is enhanced by parasitic bipolar transistor (PBT) action in the floating body of the TFT [25], and this effect increases with reducing channel length [27]. Further discussion of PBT action is presented in Sect. 8.7, dealing with short channel effects.

The impact of hot carrier damage (HCD) on n-channel TFT transfer characteristics has already been shown in Fig. 8.14, and the changes in both on-state and off-state currents are attributed to the creation of localised electron trapping centres near the drain junction. Also shown by the inset is the change in output characteristics as a result of the HCD: at low drain bias, there is reduced drain current (compared with the unstressed sample) due to the high resistance of the channel near the drain, and, at large drain bias, there is a higher drain current due to the negatively charged trapping states increasing the drain field, and, hence,

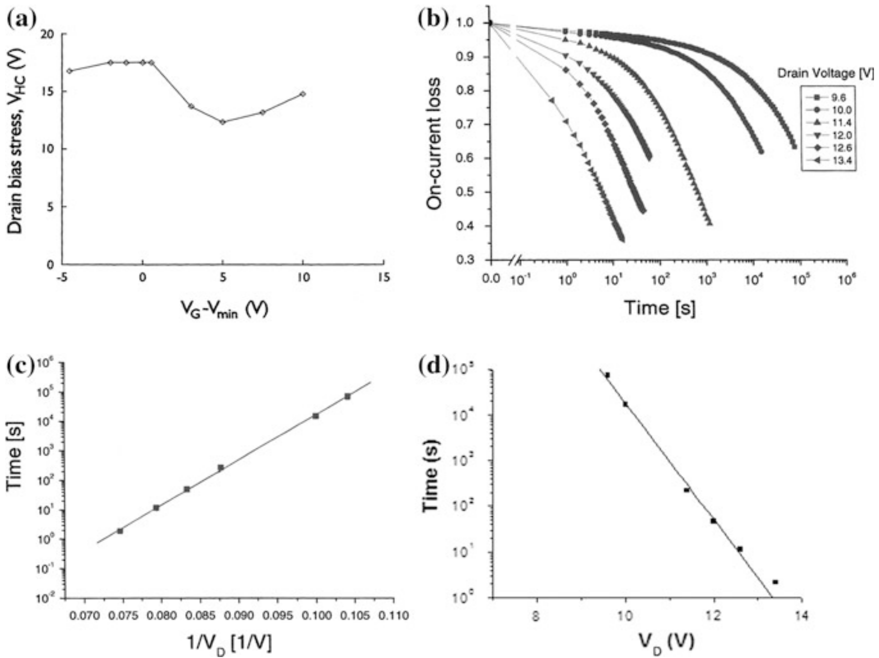

Fig. 8.16 Hot carrier instability effects in NSA TFTs **a** inter-dependence of gate and drain biases for a 30 % reduction in on-current after 60 s stress (L = 6 μm and t_{ox} = 150 nm), **b** variation of on-current degradation with drain bias and stress time (L = 4 μm and t_{ox} = 40 nm), **c** device lifetime (for 30 % on-current loss) versus 1/V_D, and **d** device lifetime versus V_D. (**a** Reprinted with permission from [24]. Copyright (1998) The Japan Society of Applied Physics)

increasing the avalanche generation rate [28]. Some typical examples of the dependence of the hot carrier instability on gate and drain bias, and stress time, are shown in Fig. 8.16a–d. The 'spoon-shaped' gate and drain bias dependence in Fig. 8.16a is characteristic of the hot-carrier instability, and is discussed further below. The change in on-current in Fig. 8.16b can be used to empirically determine device lifetime, where unacceptable performance can be defined to occur at a given reduction in on-current, such as 30 % [26]. As will be seen in this figure, the stress time needed for a given loss of on-current reduced logarithmically as the drain bias increased. This strong dependence essentially occurred once the drain bias caused the device to go into weak avalanching, and, within this regime, there was an approximately exponential relationship between device lifetime and drain bias. Indeed, from Eq. 8.33 below, the logarithm of this time should scale with reciprocal drain bias, as seen in Fig. 8.16c, and the plot can be extrapolated to determine the maximum drain bias to achieve a given device lifetime. An approximately linear plot can also be obtained directly against drain bias [26], as shown in Fig. 8.16d, and the 0.78 V/dec slope of the fitted line is an empirical measure of the relationship between lifetime and drain bias. This indicated that for each 0.78 V increment in drain bias, the device lifetime decreased by one decade.

The value is specific to this NSA device (L = 4 μm, t_{ox} = 50 nm), and it will change with device geometry and architecture, so that, for instance, SA devices, with more abrupt junctions, will typically have greater slopes, demonstrating a stronger dependence of lifetime on drain bias. For example, 1μm channel length SA TFTs, with 50 nm thick gate oxides, had a drain bias dependent lifetime of 0.32 V/dec.

Hot carrier damage has been extensively studied in c-MOSFETs, and the damage centres were identified as acceptor states at the Si/SiO_2 interface, as well as positively charged states in the gate oxide itself. From the dependence of these densities upon the gate bias, during drain bias stress, it was concluded that both hot-electron and hot-hole injection into the oxide had to take place, and that the generation of interface traps resulted from a two-stage process of hole capture at oxide traps near the interface and subsequent recombination with injected electrons [29]. It is likely that the recombination energy released by electron capture could break weak interface bonds. There is injection of both carrier types because, under the normal bias-stress conditions of $V_D > V_G$, there is field reversal in the oxide near the drain junction, which promotes hole injection. In spite of this field reversal, significant electron injection can also take place against the field if the hot electron is within a scattering distance of the Si/SiO_2 interface [29].

In analogy with these HCD effects in MOSFETs, the poly-Si damage centres have been widely attributed to states at the poly-Si/SiO_2 interface [24, 26, 28, 30], or, in analogy with defect creation in a-SiH TFTs, attributed to bulk states in the poly-Si [31]. In both cases, good fits were obtained between simulation models and the experimental characteristics, but the latter conclusion was based partly upon the observation of damage at the back of the film. However, subsequent simulation work showed that, even with top gated devices, damage centres are produced at both the front and back interfaces [28, 32].

As mentioned in Sect. 7.4.1.2, the problem of hot carrier damage can be reduced by the use of field relief regions, such as lightly doped drain, LDD, and gate-overlapped lightly doped drain, GOLDD (shown in cross-section in Fig. 7.32), and, by and large, lower doping levels give better field relief. However, dose optimisation for field relief using LDD structures involves a compromise with series resistance and reduced on-current [32]. In contrast, optimisation of dopant concentration in GOLDD structures involves almost no compromise with series resistance in the on-state, although there will be some current reduction due to the increased channel length to accommodate the GOLDD region. Less obviously, the GOLDD structure also gave significantly better field relief, as shown by the comparison of the bias-stress results in Fig. 8.17a–d. In the GOLDD device (Fig. 8.17c), there was almost no reduction in the drain current after a 30 V drain bias stress, compared with the 10–100 times reduction in the LDD device after 10 V stress. There was also no degradation in the output characteristic at low V_d, and the characteristic second saturation regime in the GOLDD TFTs was reduced by the stress [32].

These differences have been explained by applying the MOSFET HCD model to poly-Si TFTs [32], in which the simulated carrier densities and fields in the TFT

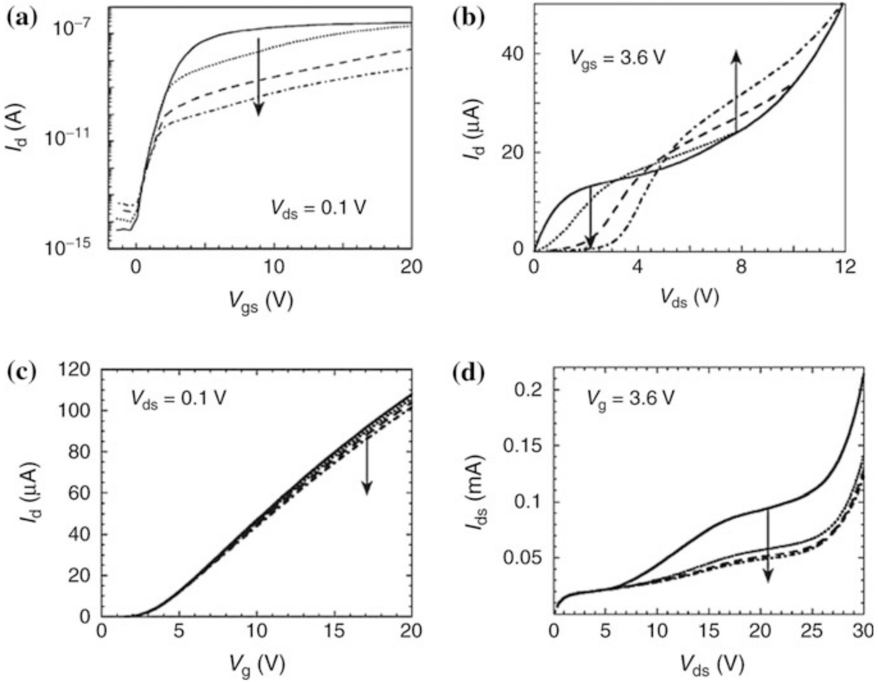

Fig. 8.17 Experimental measurements before and after drain bias stress—*arrows* indicate direction of changes **a** transfer characteristic, and **b** output characteristics of LDD TFTs after drain bias stress at 8, 10 and 12 V for 5,000 s (LDD dose = $1\text{x}10^{13}$ P/cm^2), **c** linear transfer characteristics, and **d** output characteristics of GOLDD TFTs after drain bias stress at 30 V for 75, 1,270 and 10,000 s (GOLDD dose = 5×10^{12} P/cm^2). (Reprinted from [32] with permission of IEEE)

were used to model the hot-carrier injection currents into both the top and bottom oxide layers by using the 'lucky electron' model [33]. The hot-electron injection current is given by [32]:

$$J_e(x) = A \int n(x, y) P_e(y) dy \tag{8.31}$$

and the electron injection probability, $P_e(y)$, is given by [33]:

$$P_e(y) \propto \exp - \frac{y}{\lambda} . \exp - \frac{\Phi_b}{F_x \lambda} \tag{8.32}$$

(The x direction is parallel to the semiconductor/insulator interface, and y is perpendicular to it). Φ_b is the zero field oxide barrier height, and λ is the electron mean free path. The first term in Eq. 8.32 describes the probability of an electron, at depth y in the poly-Si, travelling to the interface without an inelastic collision, and the second term is the probability of the hot-electron having enough energy to

surmount the barrier Φ_b. A similar expression holds for hole injection, and the barrier height for electrons (holes) is 3.1 eV (4.7 eV), and the electron (hole) mean free path is 6.5 nm (4.7 nm).

The 'lucky electron' model has also been used to empirically predict device lifetime, τ, [34], by arguing that the device degradation will be determined by the flux of injected hot carriers, which will be proportional to the normalised channel current, I_D/W and the hot carrier injection probability. The expression for τ was given by [34]:

$$\tau = C\frac{W}{I_D}\exp\frac{\Phi_b}{F_x\lambda} \tag{8.33}$$

where C is a constant. Using device simulation, this expression has been evaluated to investigate the gate bias and trap state density dependence of the device lifetime in poly-Si TFTs [24]. The calculated lifetime, as a function of gate bias (with $V_D = 15$ V), is shown in Fig. 8.18, for two values of trap state density. It will be seen that this expression predicts the 'spoon-shaped' dependence on gate bias, as seen in the experimental data in Fig. 8.16a, where the worst-case stress condition is approximately at $V_G = V_T$. The simple physical explanation for this effect is that, up to this gate voltage, the electron surface density (and current) has been increasing exponentially with gate bias, which more than compensates for the reducing drain field. For gate bias values greater than V_T, the electron concentration only increases linearly with gate bias in inversion, and the corresponding, linearly increasing current is not sufficient to compensate for the reducing drain field due to the increasing value of $V_{D(sat)}$. Secondly, it will be seen that the worst-case lifetime is slightly worse in the low DOS device, further reinforcing the earlier argument that improvements in basic poly-Si material quality will not reduce HCD effects.

Using Eq. 8.32, within a 2-D simulator, the device characteristics in Fig. 8.17 have been reproduced [32]. From the calculated hot-carrier injection currents, and

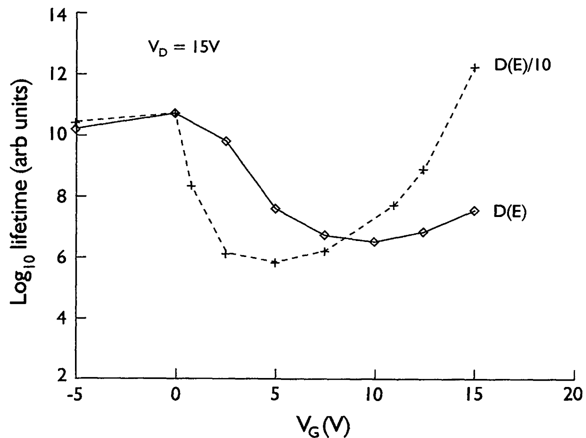

Fig. 8.18 Calculated dependence of relative hot-carrier device lifetime on gate bias, using a 2-D simulator to evaluate Eq. 8.33 (drain bias was 15 V). (Reprinted with permission from [24]. Copyright (1998) The Japan Society of Applied Physics)

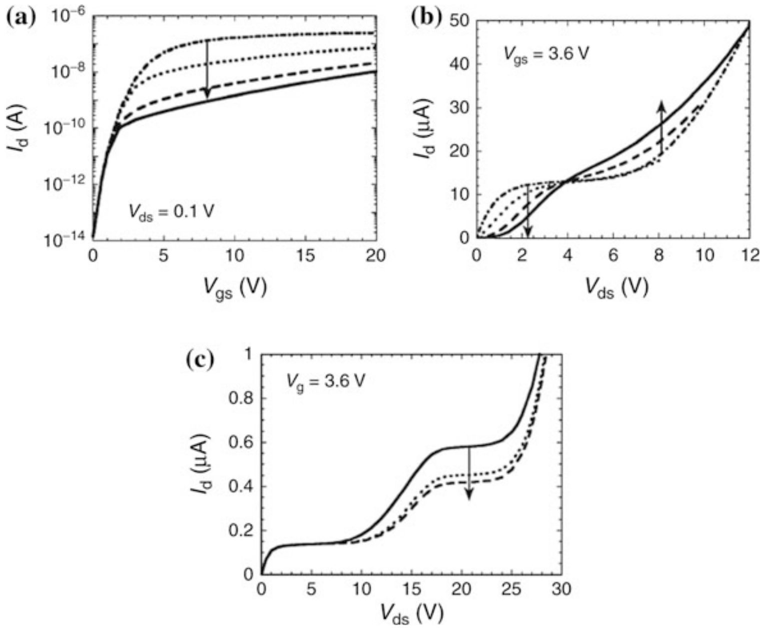

Fig. 8.19 Simulated characteristics before and after drain bias stress—arrows show direction of changes from un-stressed states **a** transfer characteristic, and **b** output characteristics of LDD TFTs following stress at 8 V, 10 V and 12 V for 5,000 s (LDD dose = 1×10^{13} P/cm^2), **c** output characteristics of GOLDD TFT following 23 V stress for 323 and 10,000 s (GOLDD dose = 5×10^{12} P/cm^2). (Reprinted from [32] with permission of IEEE)

the ensuing two stage carrier recombination process within the oxide, the positive charge density (due to trapped holes in the oxide) and the negative charge in interface states was calculated iteratively with time, so that, as these charges built up, their effect upon the field and current distribution in the poly-Si was re-calculated, which then altered the trap generation rates [32].

Figures 8.19a and b show the simulated I_d-V_G and I_d-V_{ds} plots for the LDD devices, and Fig. 8.19c shows the I_d-V_{ds} plot for the GOLDD device. In all cases, these results accurately reflect the experimental data in Fig. 8.17. For the LDD structure, acceptor trap generation started at the channel/LDD interface, where the field was at a maximum. With increasing time and V_{ds}-stress, the trap generation spread into the adjacent channel and LDD regions, at both the top and bottom poly-Si/SiO_2 interfaces. The positive trapped charge started in the same location, but finished up as a bi-modal distribution either side of the high field point. The negative charge in the interface states dominated, and constricted the electron channel current near the drain into the centre of the film. This formed a resistive bottleneck, which was responsible for the loss of on-current [32]. For the GOLDD structure, the generated interface state densities were lower than in the LDD structure, and the positive trapped charge was largely generated near the top Si/SiO_2 interface. This partially compensated the negatively charged interface

states charges at this interface, and resulted in the uncompensated negatively charged traps at the back interface having the greatest net effect. As a consequence of this distribution, the effect of the hot carrier damage on the low V_{ds} on-current near the top interface was minimal. At large V_{ds}, the current was deflected away from the top interface, but the large negative charge density at the back interface maintained the current flow more centrally within the film [32], and this reduced the impact ionisation rate in the second plateau region of the GOLDD TFTs, as seen in Figs. 17d and 19c [32, 35].

As shown, the GOLDD architecture gives significantly better hot carrier stability than the simpler LDD region, but, as with the non-self-aligned architecture, it increases the parasitic capacitance between gate and drain, and the choice of LDD architecture will be dictated by the trade-off in speed and high voltage stability requirements. As discussed in Sect. 7.4.1.2, a sub-micron GOLDD region would be needed for short channel devices, and this has been demonstrated with a conducting spacer technology [36].

P-channel TFTs, in common with p-channel MOSFETs, are far less susceptible to HCD [24, 26], and both MOSFET [37] and TFT [38] results have been successfully modelled with only electron injection. In view of this, there does not seem to be a unified HCD model using the same injection conditions for both n- and p-channel TFTs.

Other instability effects in poly-Si TFTs, over and above HCD, are discussed in Sect. 8.6.

8.5.3 Field-Enhanced Leakage Currents

High quality poly-Si TFTs, when biased in the off-state, show a leakage current characteristic, which is channel length independent, as shown in Fig. 8.9c, and which increases exponentially with both gate and drain bias, as seen in Figs. 8.9c and 8.10c, respectively [20]. The channel length independence indicates a current, which is limited by electron–hole pair generation processes at the drain, rather by resistive flow through the body of the device (which would scale inversely with channel length). However, normal thermal generation processes would produce currents, which have only a square root dependence on drain bias, and an even weaker dependence on gate bias. Hence, these anomalously large currents are described as field-enhanced currents, and Fig. 8.20 schematically shows the range of electron emission processes, which can be expected in the space charge region of a reverse biased junction. As discussed in Chap. 2, the basic leakage current mechanism is controlled by sequential electron and hole emission from deep traps near the centre of the band-gap, and, for simplicity, Fig. 8.20 shows only the electron emission processes to the conduction band. There will be equivalent hole emission processes to the valence band.

At low fields and high temperatures, simple thermal emission (with no field dependence) will dominate, giving drain current activation energies of $\sim E_G/2$. At

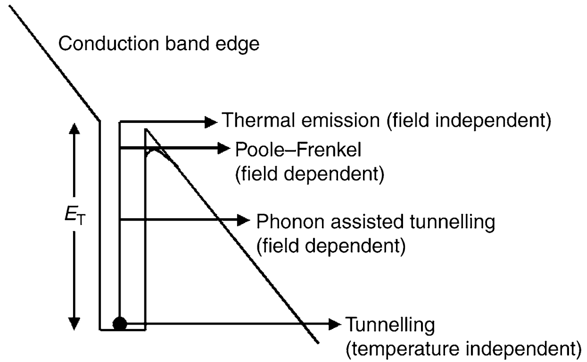

Fig. 8.20 Schematic illustration of electron emission processes into the conduction band from a trap at depth E_T. The trap is located within a reverse biased space charge region

high fields and low temperatures, tunnelling will dominate giving near-zero activation energies. Between these two extremes, two further processes are shown, which are the field-induced lowering of the emission barrier for a Coulombic centre (the Poole–Frenkel effect), and thermal emission to a virtual state followed by tunnelling (phonon assisted tunnelling), both of which are field dependent.

Experimental results, near room temperature, showing thermal activation energies decreasing from $\sim E_G/2$ with increasing V_D [22] and V_G [39] rule out pure tunnelling, and the best fits to the data have been with phonon assisted tunnelling [7, 22, 39–41], although, at the highest biases, band-to-band tunnelling is also significant [40, 41]. The phonon assisted tunnelling can be represented as a field dependent enhancement, $e_n(F)$, of the low-field electron thermal emission rate, e_{n0}, by:

$$e_n(F) = e_{n0}\gamma(F) \tag{8.34}$$

The field enhancement factor, $\gamma(F)$, for a discrete Coulomb centre at E_T, is given by [42]:

$$\gamma(F) = \exp\frac{\Delta E_T}{kT} + \frac{q}{kT}\int_{\Delta E_T}^{E_T} \exp\left\{\frac{E}{kT} - \frac{4E^{1.5}(2m^*q)^{0.5}}{3\hbar F}\right\}\left\{1 - \left(\frac{\Delta E_T}{E}\right)^{5/3}\right\}dE \tag{8.35}$$

where, ΔE_T is the emission barrier lowering due to the Poole–Frenkel effect, and this will be zero for a Dirac centre.

The simplified expression for a Dirac centre can be approximated by [42]:

$$\gamma(F) \approx \frac{2\pi^{0.5}q\hbar F}{(kT)^{1.5}2(2m^*)^{0.5}}\exp\left\{\frac{1}{3(kT)^3}\left(\frac{q\hbar F}{2(2m^*)^{0.5}}\right)^2\right\} \tag{8.36}$$

The exponential term in the above expression is quadratic in F, and the depletion approximation relates the maximum field to the drain bias by $F_{\max} \propto$

$V_d^{0.5}$, so that this simplified expression correctly predicts the observed exponential dependence of leakage current on drain bias.

The field-free thermal emission rate, e_{n0}, is given in Chap. 2 by:

$$e_{n0} = v\sigma_n N_C \exp - \frac{E_T}{kT} \tag{8.37}$$

where σ is the electron capture cross section, v is the electron thermal velocity and N_c is the effective density of conduction band states.

Equivalent expressions for $e_p(F)$ and e_{p0} can also be formulated for the hole emission rates, and the leakage current density is given by integration across the drain space charge region, of width d:

$$J = qN_T \int_0^d \frac{e_n e_p}{e_n + e_p} dx \tag{8.38}$$

Although the preceding expressions are for a discrete trap, and the poly-Si DOS is distributed across the band-gap, current generation processes, via electron–hole pair emission, are localised on near-mid-gap centres. This is in order to minimise the sum $e_n + e_p$, and this process can be reasonably accurately represented by discrete near-mid-gap states. In numerical simulations of the leakage current process, the full trap distribution was used [40, 41], and the results remain consistent with the above qualitative considerations, although it has been shown that, at high fields, the most efficient generation centres can be up to 50 meV off mid-gap [43] due to the Poole–Frenkel effect. An interesting aspect of those calculations was the observation that, for distributed traps, the current can be limited by emission from the Coulomb state of the centre, located slightly deeper than $E_G/2$, whereas, for a discrete trap at $E_G/2$, the current would normally be limited by the slower emission from the Dirac state of the centre.

As with the hot carrier instability, the field enhanced leakage currents are a direct consequence of the high drain fields in poly-Si TFTs, and field relief at the drain, using LDD or GOLDD regions, will also reduce these field-enhanced currents [24, 41]. Although the DOS values in high quality TFTs will not influence the drain field itself, the magnitude of the currents will scale with the trap density near mid-gap, and, hence, with the DOS values near mid-gap. Also, in common with the hot carrier instability, field enhanced leakage currents are observed in MOSFETs [44], and are not specific to poly-Si TFTs.

8.6 Other Bias-Stress Instabilities

Section 8.5.2 dealt with hot carrier induced instability, which is at a maximum when high drain-bias-stress is combined with a low gate-bias setting approximately equal to the threshold voltage [23, 24]. Other important bias-stress

combinations are high gate bias without drain bias, and combined high gate and high drain bias.

8.6.1 Gate Bias Stress

8.6.1.1 Ionic Instability

In common with MOSFET technology, alkali ion contamination, particularly sodium, has to be avoided, as, under the influence of positive gate bias-temperature stress, negative threshold voltage shifts occur in poly-Si TFTs. The specific ion contaminant can be identified from its characteristic ion current signature observed during a gate bias sweep at 250 °C [45].

Gate bias stress can also result in threshold voltage shifts, due to charged ion movement, in porous, poor quality gate oxides [46]. As discussed in Sect. 7.3.1, the absorption of water in these films has been identified by characteristic thermal desorption spectroscopy peaks at 100–200° C [47], and the presence of H^+ and OH^- ions in the oxide has led to both negative and positive threshold voltage shifts after positive and negative bias-stressing, respectively [46]. However, current state-of-the-art gate oxide films, formed by PECVD deposition from either oxygen-diluted tetraethylorthosilicate, TEOS [47], or helium-diluted silane and nitrous oxide [48, 49] have deliberately employed dilution conditions to reduce the oxide deposition rate, and to deposit dense, low porosity oxides, which are free from water-induced instabilities.

8.6.1.2 Negative Bias-Temperature Instability

NBTI has been widely studied in MOSFET devices, where it is particularly seen in p-channel transistors stressed with negative gate bias (< 6MV/cm) at elevated temperatures of 100–250 °C [50]. The stress causes an increase in the absolute magnitude of threshold voltage, as well as degradation of sub-threshold slope and g_m. These changes are negligible under comparable positive bias-stress conditions, and also negligible with both positive and negative gate bias-stress in n-channel MOSFETs. The changes in device characteristics have been attributed to a combined increase in trapping states at the Si/SiO_2 interface, as well as positive charge in the gate oxide. The physical model for the trapping state change is the de-hydrogenation of previously passivated Si dangling bonds at the interface, although the detailed process whereby this occurs, together with the increase in oxide charge, is still a matter of discussion, with different models invoking the role of mobile hydrogen ions or holes [50].

Similar instabilities have been reported in a wide range of p-channel poly-Si TFTs, made from directly deposited LPCVD poly-Si, solid phase crystallised [51, 52] and excimer laser crystallised material [53–55]. In most of this work [51–53],

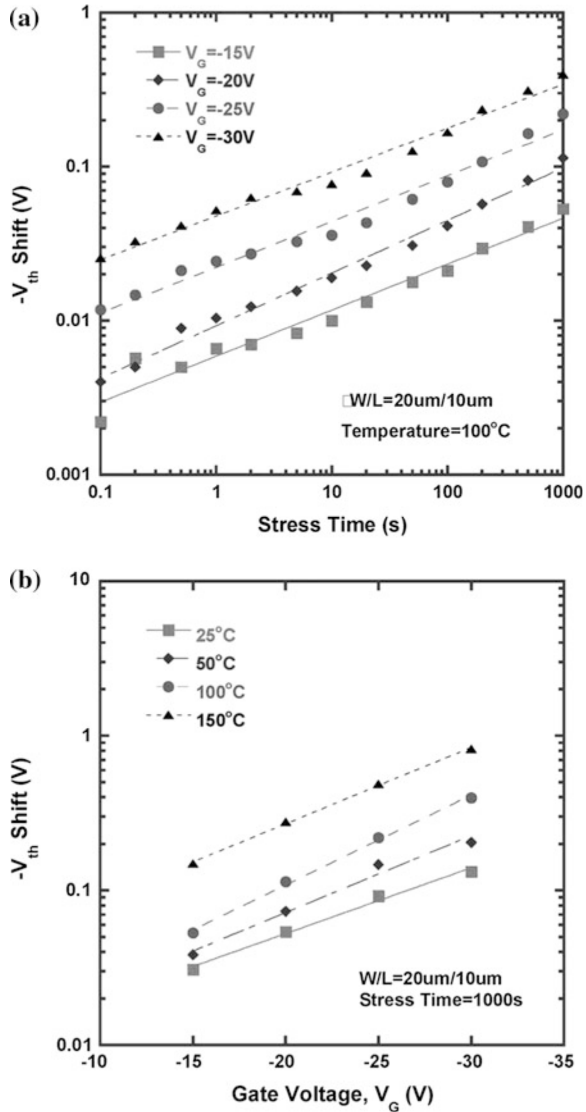

Fig. 8.21 Threshold voltage instability of p-channel poly-Si TFTs with negative gate bias temperature stress (NBTI) **a** time dependence at different gate biases, **b** gate bias dependence at different temperatures (Reprinted from [53] with permission of IEEE)

the increase in threshold voltage was thermally activated over the temperature range 297–430 K, with a power dependence on stress time, and an exponential dependence on gate bias stress, as shown in Fig. 8.21 [53]. This dependence was empirically represented by:

$$\Delta V_T \propto t^n \exp(-E_a/kT)\exp(C|V_G|) \tag{8.39}$$

where n was 0.28–0.34, E_a was $\sim$0.14 eV, and C was a fitting parameter whose value was $\sim$0.1–0.13. The power time dependence was qualitatively similar to

that reported in MOSFETs [50], although the gate bias dependence differed between authors. In the MOSFET work, there was a power dependence of $E_{ox}^{1.5}$ (where $E_{ox} = \{V_G\text{-}V_{FB}\text{-}\Psi s\}/t_{ox}$), rather than an exponential dependence. In other TFT work, there was a linear dependence of ΔV_T on E_{ox} above a critical oxide field of 0.5MV/cm [54, 55].

Notwithstanding some of the differences with the MOSFET data, the TFT results have been broadly interpreted in the same way: namely, by an increase in positive oxide charge, and an increase in trapping state density [55]. In one case [53], the change in sub-threshold slope of the I_d-V_G characteristic was attributed to interface state generation, and the near-threshold part of the characteristic was analysed using the Levinson method [5], and identified an increase in the GB trapping state density. However, as discussed in Sect. 8.3, all trapping states can be represented by an effective density per unit surface area, and identifying the specific physical location of the traps can be difficult. In other work on NSA TFTs [54], numerical simulation of the characteristics after NBTI could satisfactorily account for the NBTI changes by the introduction of an exponential distribution of Si/SiO_2 interface states, $N_{ss}(E)$, without any increase in positive oxide charge. In contrast, SA TFTs showed linear increases in both N_{ss} and oxide charge with E_{ox} [55].

In summary, NBTI is a well documented instability process in p-channel poly-Si TFTs, which has been interpreted in terms of an increase in trapping states in the material, where the state location has been attributed to both Si/SiO_2 interface states as well GB states, and the change in oxide charge seems to be sample dependent.

8.6.2 Combined Gate and Drain Bias Stress

The combination of high gate and high drain bias-stress results in a large current flow through the device, and this can lead to self-heating induced instabilities [55–61], in which the modulus of the threshold voltage of both n-channel and p-channel TFTs increased with increasing bias stress. In addition to the increase in threshold voltage, a decrease in on-current, an increase in off-current, and a degradation in sub-threshold slope have also been observed [56].

As might be expected, the self-heating effects, induced by different combinations of gate bias and drain bias, were best represented by the stress-power dissipation (= $I_d \times V_d$) within the device, and, for a given device geometry, the bias-stress threshold voltage shifts could be uniquely correlated with this power dissipation, as shown in Fig. 8.22 [56]. The self-heating effects have been confirmed by both direct infra-red detector measurements of the surface temperature of the device [56, 58], as well as by numerical simulations of Joule heating within the TFT [56, 57, 59, 61]. The measurements showed surface temperatures from ~100 °C up to ~250 °C, depending upon the specific device geometry and bias conditions [56, 58], and the magnitude of the bias-stress instability has been

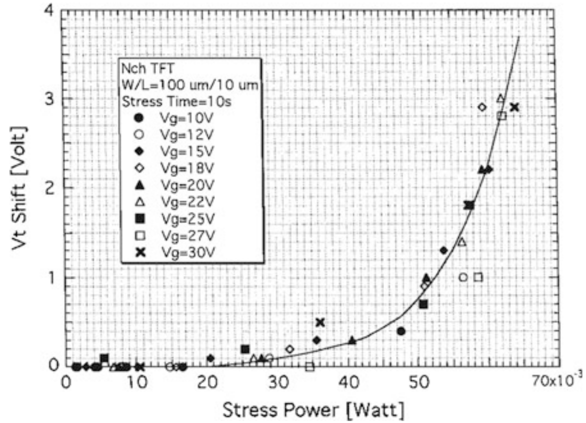

Fig. 8.22 Dependence of threshold voltage shift on stress power, where V_d was varied between 5 and 30 V, and V_G determined the drain current. Stress time was 10 s (Reprinted with permission from [56]. Copyright (2002) The Japan Society of Applied Physics)

correlated with the measured temperature of the device [56, 58], as shown in Fig. 8.23 [58]. The TFTs used for this data set had different grain sizes, resulting in increasing electron mobility with grain size. The mobility differences gave different on-currents for the same bias conditions, and the large grain devices showed the largest threshold voltage shifts after stress. However, when the results were normalised with respect to the measured device temperatures, the results, for different device geometries as well as grain size, fell upon the common curve shown in Fig. 8.23.

The device geometry was identified as a key parameter in determining the internal temperature distribution. This was because the low thermal conductivity of the glass substrate (~ 1.3 W/m/K) made it an inefficient route for the dissipation of heat from the TFT channel, resulting in the device edges and its top surface becoming significant channels for heat dissipation. Hence, the size of the device, and particularly the width of the channel (for a given channel length), played an important role in determining its temperature, with wider devices displaying both higher temperatures and greater stress-induced threshold voltage shifts [56, 58, 61], as shown in Fig. 8.24 [56].

In agreement with the experimental measurements, the simulations also predicted channel temperatures of ~ 120 to ~ 300 °C [56, 57, 59, 61], depending

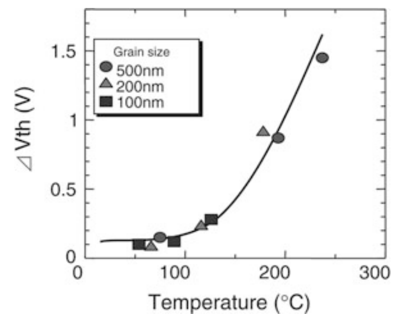

Fig. 8.23 Correlation of self-heating threshold voltage shift with device temperature for TFTs of different grain size and different channel widths (Reprinted with permission from [58]. Copyright (2005) The Japan Society of Applied Physics)

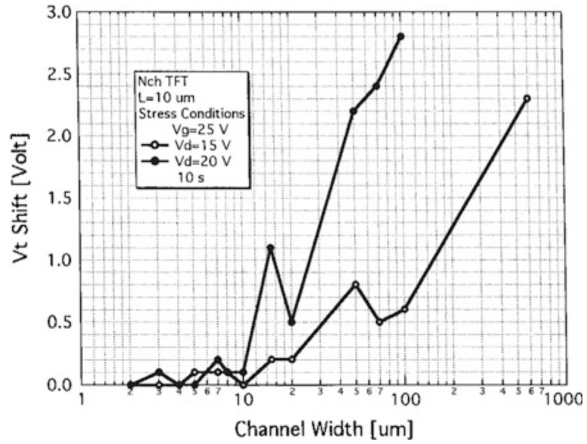

Fig. 8.24 Influence of channel width on self-heating threshold voltage shifts (Reprinted with permission from [56]. Copyright (2002) The Japan Society of Applied Physics)

upon the biasing conditions and the device geometry. In addition, the simulations demonstrated that, even when the temperature rise was not sufficient to cause bias-stress instability, it was sufficient to induce a negative output conductance in high mobility TFTs, due to increased phonon scattering of the channel electrons [59].

The threshold voltage instability has been correlated with an increase in the trapping state density either near the middle of the poly-Si band-gap [56], or at the Si/SiO_2 interface [61], and attributed to thermally-induced Si–H bond breaking either in the poly-Si grain boundaries [56] or at the interface [61]. Other workers have suggested electron injection into the gate oxide [57, 58], in analogy with hot carrier defect generation [57]. However, some of the results have been obtained at drain bias values less than the saturation voltage [56], which would keep the drain field low, and militate against hot carrier injection in those cases.

For p-channel TFTs, there is a similarity with the NBTI effects described in the preceding section, in which the drain-bias-induced self-heating plays the role of the deliberate temperature increase used to observe NBTI. Some authors have correlated the two effects, and argued that the self-heating instability is a manifestation of NBTI, in which the threshold voltage shift was found to be proportional to the oxide field, E_{ox} [54, 55] (see the discussion of Eq. 8.39). Hence, the only difference between the two effects was that, with the self-heating instability, the varying channel potential, due to the drain bias, caused a variation of oxide field, E_{ox}, along the channel, resulting in spatially non-uniform interface state and positive oxide charge creation. The device characteristics after self-heating stress were successfully simulated using the calculated values of the oxide field, E_{ox}, to fit a spatially varying interface state density and oxide charge density to the experimental characteristics [55]. The experimental and simulated transfer characteristics, before and after self-heating bias-stress, are shown in Fig. 8.25a, and, for the 10,000s stressed sample, the calculated interface state density at the source end of the channel was five times higher than at the drain end, due to the larger value of E_{ox} at the source. This spatial asymmetry in the interface state density also

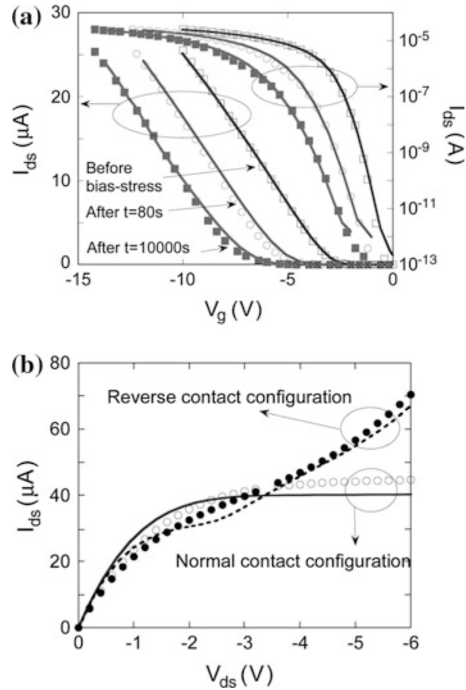

Fig. 8.25 Experimental (*symbols*) and simulated (*lines*) results of self-heating bias stress **a** transfer characteristics before and after stressing at $V_G = -15$ V and $V_d = -9$ V, and **b** output characteristics after 10,000 s stress with normal and reversed source/drain contacts (Reprinted from [55] with permission of IEEE)

successfully explained the change in output characteristics when the source and drain terminals were reversed, as shown in Fig. 8.25b. When the source terminal, with the higher interface state density was used as the drain, this higher density increased the drain field, causing a stronger avalanche current, as seen in the figure.

Whilst self-heating effects have been well established as a reliability issue in poly-Si TFTs on glass, they are a bigger issue with TFTs on flexible, polymer substrates [60, 61], where the thermal conductivity is even lower at ~0.2 W/m/K. Some common solutions have been suggested for both types of substrate, such as multi-fingered devices to avoid large W values, as well as overall device scaling to reduce both device area and drain biases, whilst retaining the required levels of channel current at lower power levels [60]. Alternatively, reduced self-heating effects have been demonstrated with thermally conducting flexible substrates, such as copper [57] or stainless steel [61] foils. The use of thin foils is discussed further in Chap. 11, which reviews the field of flexible substrate technologies for TFTs.

8.7 Short Channel Effects

Short channel effects (SCEs) have been well established, and widely studied, in c-Si MOSFETs [62], and they refer to a range of phenomena for which the

classical long channel model, described in Chap. 3, no longer applies. As channel length, L, is reduced, examples of this behaviour are a drain current, which rises more strongly than 1/L, threshold voltage, which reduces with channel length, sub-threshold currents which increase with drain bias, V_{ds}, and poor saturation in the output characteristics. These are a consequence of a number of inter-related phenomena, such as the size of the source and drain space charge regions becoming comparable to the channel length. This reduces the amount of charge needed on the gate to invert the channel surface, and decreases the threshold voltage with reducing channel length. Also, when the drain space charge region is comparable to channel length, such that the source and drain space charge regions start to overlap, increased drain bias can reduce the potential barrier between the source and the channel (drain-induced barrier lowering, DIBL), giving drain-bias-dependent sub-threshold currents and poor current saturation in the output characteristic. Strategies have been developed to minimise these effects, from simply reducing the gate oxide thickness and/or increasing the substrate doping level. Both of these changes increase the field at the drain (for a given drain bias), as discussed in Sect. 8.5.1, and reduce the spread of the space charge regions along the channel. More sophisticated changes include modifications in device design to tailor the doping level to optimise overall device performance, through to the use of field relief structures [62].

Whilst the gate length in deep sub-micron MOSFETs has been progressively shrunk to the current production values of ~50 nm [63], channel length reduction in poly-Si TFTs has been more modest, with the minimum reported dimension being ~0.5 μm [64–66]. Nevertheless, a variety of short channel effects have been seen in poly-Si TFTs having a channel length of 2–3 μm or less, with the effects becoming stronger as the channel length reduced. The results in the following sub-sections have been taken from SA n-channel, laser crystallised TFTs made in 40 nm thick layers of poly-Si. Some of the effects seen are classical short channel effects, such as a gate length dependent threshold voltage [67], and poor output impedance, as shown in Fig. 8.26a and b, respectively, and both can be mitigated by using a reduced oxide thickness. The threshold voltage measurements in Fig. 8.26a were made at a low drain bias of 0.1 V, and at normalised channel currents of $W/Lx10^{-7}$A, both of which were chosen to minimise other short channel effects to be discussed further below. The solid lines are simulation results derived from a double exponential DOS whose parameters were adjusted in order to give the best fit to the I_d-V_G characteristics across the range of channel lengths [67]. Both the experimental data and the simulations confirm the reduction in SCEs due to a reduced gate oxide thickness. The comparison of the I_d-V_D characteristics in Fig. 8.26b were made using different gate voltages for the two oxide thicknesses in order to normalise the measurements to common values of low field channel conductance. The TFTs with the thicker gate oxide showed very poor current saturation, compared with the thinner gate oxide samples. To quantify the effect of the thinner gate oxide, the current in saturation can be represented by [68]:

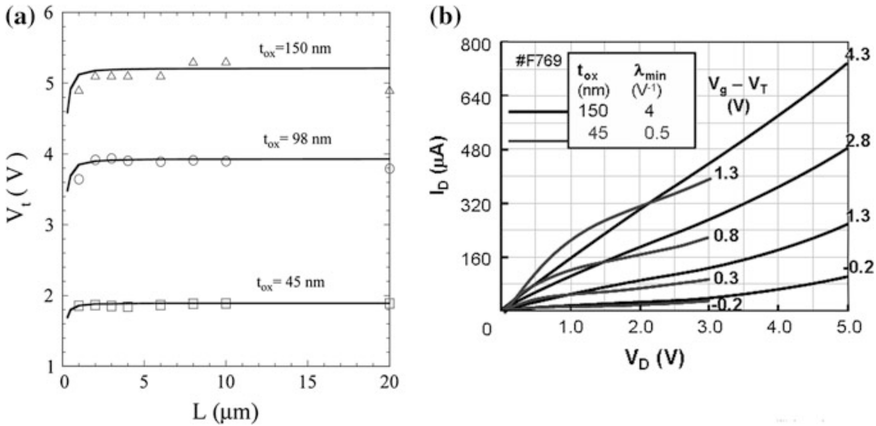

Fig. 8.26 Classical short channel effects in 1μm channel length SA poly-Si TFTs **a** variation of threshold voltage with L and gate oxide thickness (Reprinted from [67] Copyright (2005), with permission from Elsevier), and **b** comparison of output characteristics for two different gate oxide thicknesses

$$I_d = I_{do}(1 + \lambda V_d) \tag{8.40}$$

for $V_d > V_{d(sat)}$, where λ is commonly used in circuit modelling as an output characteristic quality factor, whose value is zero for devices with perfect saturation characteristics. The values for λ are shown in Fig. 8.26b, and they display an 8-fold improvement with the thinner gate oxide.

In addition to these classical effects, a number of other performance artefacts have been reported in short channel poly-Si TFTs, which have included the presence of parasitic contact resistance [65, 67, 69], the 'kink' effect in the output characteristics at high drain bias [27], and drain bias dependent sub-threshold characteristics [72]. The latter two effects are related to floating body effects in the TFTs, and will be discussed separately below. As will be apparent in that section, the floating body related SCEs have features, which are also observed in floating body SOI MOSFETs.

8.7.1 *Parasitic Resistance Effects*

When the linear regime channel current, in variable length TFTs, is normalised by channel length, a common curve would be expected as a function of gate bias. In contrast, the normalised currents, measured in SA n-channel TFTs, decreased with decreasing channel length, as shown in Fig. 8.27a [69]. This figure demonstrates that only the longest channel device had an approximately linear dependence of current on gate bias, and that, with reducing channel length, the expected linearity deteriorated as the currents failed to scale with 1/L. These results, together with the

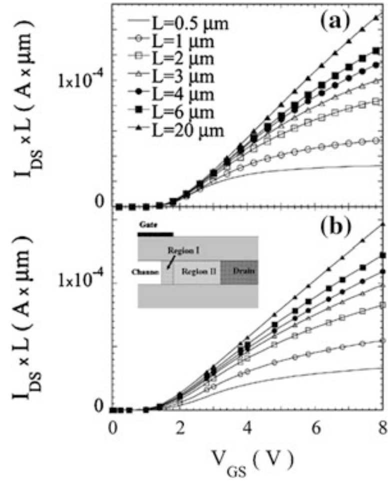

Fig. 8.27 TFT transfer characteristics, normalised by channel length **a** experimental data, and **b** simulations (also shown in the insert is the location of the ion-damaged regions in the simulation model) (Reprinted from [69] with permission of IEEE)

almost saturated nature of the L = 0.5 μm characteristic, are indicative of a parasitic resistance, R_p, in the channel. The total resistance of the device, R_{meas}, will be given by the sum of the channel resistance/unit length, R_{ch}, the doped source and drain resistance, R_n, as well as R_p, i.e.

$$R_{meas} = V_d/I_d = R_{ch}L + R_n + R_p \tag{8.41}$$

and, from a plots of $1/I_d$ versus L, at different values of V_G, the channel resistance can be calculated from the slope, and the average value of R_p across the different channel lengths can be extracted from the intercept (where R_n can be calculated from the sheet resistance of the source/drain dopant and the geometry of these doped regions). The carrier mobility can be derived from the normalised channel resistance, using the linear regime expression for TFT channel current,

$$R_{ch} = 1/\{\mu W C_{ox}(V_G - V_t)\} \tag{8.42}$$

For the TFTs in Fig. 8.27a, this analysis yielded a value of R_p which was ~600ohms [69]. For gate voltages > 6.5 V, this was more than the channel resistance of TFTs with channel lengths < 1 μm, and was responsible for the almost V_G–independent channel currents seen in the L = 0.5 μm TFTs in Fig. 8.27a.

It is significant that this effect was seen only with SA n-channel TFTs, and not with NSA n-channel TFTs nor with SA p-channel TFTs, and, as discussed in Sect. 7.4.1.1, it has been physically associated with residual phosphorus ion doping damage in the poly-Si near the edges of the gate. As also discussed in that section, the magnitude of this damage was determined by the process details, and, in modelling this effect [69], for both high and low values of R_p, it has been found appropriate to represent this damaged area by two adjacent high DOS regions, one, ~50 nm wide, immediately beneath the gate, and the other, ~200 nm wide, extending from the gate edge into the doped regions. Using this model, with DOS

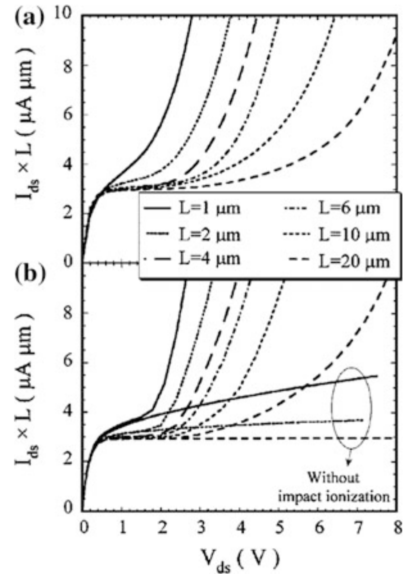

Fig. 8.28 Output characteristics for different channel length TFTs (normalised by channel length) **a** experimental data, and **b** simulations, with and without impact ionisation switched on (Reprinted with permission from [27]. Copyright (2004) American Institute of Physics)

values in region II ~10 times higher than in the channel, it was successfully fitted to the experimental data as shown in Fig. 8.27b.

As is apparent, this SCE is quite different from the classical effects seen in MOSFETs, and is a consequence of the particular processing schedule favoured for SA n-channel poly-Si TFTs.

8.7.2 Floating Body Effects

8.7.2.1 Kink Effect

Figure 8.28a shows measurements of the output characteristics for a range of TFT channel lengths from L = 20 μm to L = 1 μm [27], where the characteristics have been measured at a low enough value of gate bias to avoid the parasitic resistance effects discussed in the preceding section. In this case, the linear regime currents showed good scaling with L, but the saturation currents showed a strong L dependence, with increasingly large non-saturating currents appearing at successively lower values of drain bias. In analogy with SOI MOSFETs, it is these anomalous currents, which have been referred to as the kink effect. However, in non-fully depleted SOI devices, the kink is seen as a step in the saturation current in the output characteristic [70], rather than the continuously increasing current seen in Fig. 8.28a. These latter characteristics are much more similar to the behaviour of fully-depleted SOI devices [71], in which there is not so much a step

in the saturation current, but more of a continuous increase, which has been compared to the open-base breakdown voltage in a bipolar transistor [73].

2-D simulations were used to analyse the results in Fig. 8.28a, where a double exponential DOS was established by fitting to the low V_{ds} transfer characteristics of a long channel length device, and optimised impact ionisation parameters were used to establish a fit to the high V_{ds} output characteristics. The impact ionisation generation rate, G_{II}, was given by [72]:

$$G_{II} = nv_n\alpha_n + pv_p\alpha_p \tag{8.43}$$

where v_n (v_p) is the electron (hole) velocity, and α_n (α_p) is the electron (hole) ionisation coefficient, which is given by the Chynoweth law:

$$\alpha_{n,p} = \alpha_{n,p}^{\infty} \exp - \left(\frac{F_C}{F_{ll}} \right) \tag{8.44}$$

and F_C is the critical electric field and F_{ll} is the field parallel to the current flow. The simulated characteristics are shown in Fig. 8.28b, where $F_C = 2.9 \times 10^6$ V/cm and $\alpha_n = 5 \times 10^5 \text{cm}^{-1}$ [27].

The model was used to examine the relative roles of DIBL and avalanching in the kink effect by comparing simulations with and without the impact ionisation effect switched on. As seen in Fig. 8.28b, impact ionisation was needed to simulate the results. During impact ionisation, electron-hole pairs are produced in the high field region near the drain junction, and the electrons are swept into the drain by this field. In the floating body of the TFT, the holes have to flow through the poly-Si layer towards the source junction, and a steady state concentration of holes will be stored in the layer. This forward biases the junction, permitting a hole injection current into the source. The forward biased source junction will also inject further electrons into the channel, thereby generating parasitic bipolar transistor, PBT, action. The PBT contribution to the overall current, I_{ds}, can be analysed in the following way [27]:

$$I_{ds} = M(I_{ch} + I_e) = I_{ch} + I_e + I_b \tag{8.45}$$

Where M is a multiplication factor, I_{ch} is the channel current in the absence of avalanching, and I_e is the emitter current due to the PBT action. I_b is the base current, given by the flow of holes generated by impact ionisation at the drain (which was calculated from the integral of the impact ionisation rate). The emitter current gain, β, is given by:

$$\beta = (I_e - I_b)/I_b \tag{8.46}$$

and the excess device current, ΔI, due to impact ionisation and the PBT is:

$$\Delta I = I_{ds} - I_{ch} = I_e + I_b \tag{8.47}$$

$$\Delta I/I_{ds} = (\beta + 2)(M - 1)/M \tag{8.48}$$

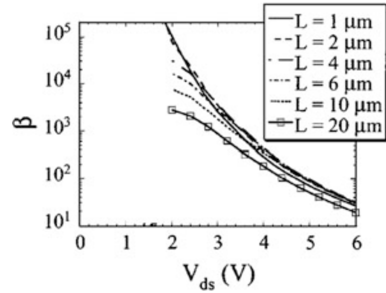

Fig. 8.29 Simulated results showing the emitter current gain, β, as a function of drain bias, for different channel length TFTs (Reprinted with permission from [27]. Copyright (2004) American Institute of Physics)

Hence, the normalised excess current is a function of M and β. The calculated values of M-1 varied with drain bias from $\sim 10^{-8}$ to 10^{-2}, and the corresponding β values are shown in Fig. 8.29. It will be seen that β is greatest, and displays the strongest L dependence, at low values of V_{ds}, where the hole injection is weakest, and the junction injection efficiency is greatest. With increasing V_{ds}, the avalanche rate and I_b increase, which causes a progressive lowering of the source barrier, such that each increment in hole current produced a reduced relative increment in electron current due to the lower barrier height. Nevertheless, the values of β range from $>10^5$, at low V_{ds}, to >10, at large V_{ds}, and demonstrate that the basic avalanche current, I_b, is significantly magnified by the PBT effect. In other words, whilst the kink effect is initiated by impact ionisation in the high drain field, the majority of the current flowing through the device is the result of current amplification due to parasitic transistor action in the floating 'base' of the device. This is analogous to the amplification of the collector–base leakage current in an open-base bipolar transistor [73]. The contribution of the injected current, I_e, as a function of channel length, L, (at $V_{ds} = 4$ V, where $\beta > 100$), is illustrated by the current component comparison in Fig. 8.30 [27]. This figure shows the low values of I_b compared to I_{ds} at all values of L, but, at L = 1 μm, the major component of the total current was due to I_e and the PBT effect. In contrast, for L = 20 μm, the PBT effect was much weaker, and the current was essentially a pre-kink, basic channel current.

These TFT results, including the dependence of β and M-1 on V_{ds}, are similar to those reported in fully depleted SOI MOSFET devices [71].

8.7.2.2 Sub-Threshold and Threshold Voltage Effects

This section deals with the drain bias dependence of both sub-threshold currents and of threshold voltage. Whilst these are essentially classical MOSFET short channel effects, the involvement of floating body effects in poly-Si TFTs [72] warrants further discussion.

Figure 8.31 compares the drain bias, V_{ds}, dependent characteristics of short (L = 0.4 μm) and long (L = 20 μm) channel TFTs, in which the L = 20 μm TFT displays classical long channel behaviour, with the sub-threshold currents being

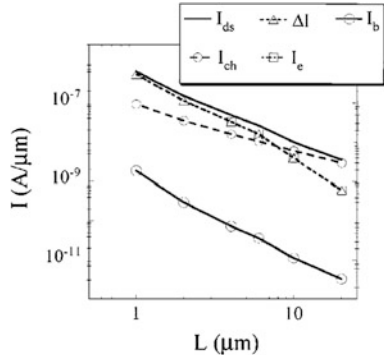

Fig. 8.30 Simulated results showing the different current components of I_{ds} as a function of channel length (at $V_{ds} = 4$ V) (Reprinted with permission from [27]. Copyright (2004) American Institute of Physics)

independent of V_{ds}, while the L = 0.4 μm TFT displays a strong V_{ds} dependence [72]. This dependence will also manifest itself as a V_{ds}-dependent threshold voltage, as shown in Fig. 8.32, where the threshold voltage was measured at $I_d = 10^{-7}$W/L A to minimise series resistance effects. Also shown by the solid lines in this figure are fitted simulation results obtained from optimised DOS and impact ionisation parameters [72], as discussed in the previous section. As will be seen, the influence of drain bias on V_T was much stronger in the short channel TFTs, and is ostensibly similar to a classical short channel DIBL effect.

However, given the presence of impact ionisation in the simulated results, the relative contributions of the direct DIBL and the PBT effects, which will also lower the source-channel barrier, have been clarified [72]. Figure 8.33 shows the simulations of V_T, with and without drain avalanching turned on. At low V_{ds}, the DIBL was primarily responsible for the barrier lowering, but the effect of hole accumulation, via the PBT effect, reduced the barrier at higher values of V_{ds}. As would be expected from Fig. 8.31, both effects increased as the channel length decreased. These barrier-lowering effects were also directly seen in simulations of

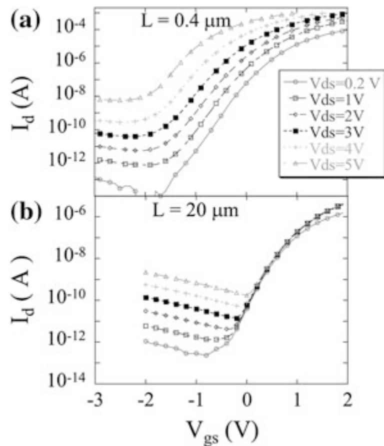

Fig. 8.31 TFT transfer characteristics measured as a function of drain bias **a** L = 0.4 μm, and **b** L = 20 μm (Reprinted with permission from [72]. Copyright (2010) American Institute of Physics)

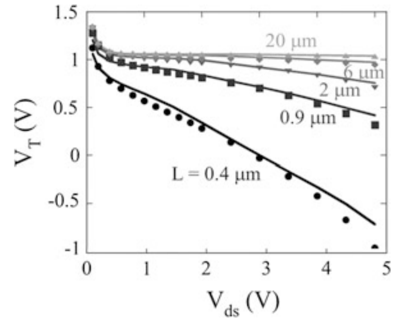

Fig. 8.32 Variation of measured (*symbols*) and simulated (*lines*) threshold voltage as a function of drain bias for different channel length TFTs (Reprinted with permission from [72]. Copyright (2010) American Institute of Physics)

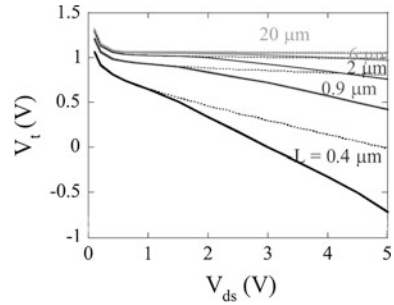

Fig. 8.33 Simulated values of threshold voltage as a function of drain bias, with (*solid lines*) and without (*broken lines*) impact ionisation switched on (Reprinted with permission from [72]. Copyright (2010) American Institute of Physics)

the source barrier height itself [72], with the influence of PBT lowering being much smaller in the longer channel devices.

As can be appreciated, the kink effect discussed in the previous section, and the V_T effects in this section, are related phenomena. Both are caused by the generation of impact ionisation holes at the drain junction, leading to PBT action in the floating body of the TFT. The kink effect discussion introduced these concepts, and focussed on the current gain within the device, and its impact on the total current flow. This section has looked in more detail at the relative contributions of DIBL and the PBT effect to the source barrier height in short channel TFTs.

8.8 Summary

In this chapter, various aspects of the characterisation and performance of poly-Si TFTs have been considered. Whilst much current analysis of poly-Si TFTs is based upon the use of 2-D numerical simulators, a simple analytical model of grain boundary conduction was introduced in Sect. 8.2, as this embodies some key physical considerations of carrier transport through poly-crystalline material. The limitations of this model were discussed, and, in Sect. 8.3, the DOS in poly-Si was shown to be continuous across the band-gap, rather than based upon a discrete trapping level (as assumed in the analytical model). It was found that the DOS

could be well represented by a pair exponentials, which could be related to band edge states and deep states.

In Sect. 8.4, the low-field TFT leakage currents were characterised by an analytical carrier generation rate and transport model, which encompassed all the key features of the drain voltage and channel length dependences of the leakage current in TFTs containing both high and low DOS values. In addition to this classical low field phenomenon, poly-Si TFTs display a number of undesirable artefacts, such as low output impedance, drain bias stress instability and field enhanced leakage currents, which are associated with a large electrostatic field at the drain junction. The drain field, in high quality TFTs, is essentially determined by the 2-D architecture of the device, rather than by the DOS level, and the mechanisms of hot carrier instability and field enhanced leakage currents were described in Sect. 8.5. Other bias instability processes in poly-Si TFTs, including ionic drift under gate bias stress, threshold voltage instability under elevated temperature negative gate stress, and self-heating instabilities under combined gate and drain bias stress were discussed in Sect. 8.6.

Short channel effects, SCEs, were presented in Sect. 8.7, where it was shown that some of these effects were comparable to the well-established SCEs in MOSFETs. However, others, such as parasitic channel resistance effects, are specific to certain types of n-channel TFT technology. A further class of SCEs was enhanced by parasitic bipolar transistor action due to floating body effects in the devices, and are comparable to similar phenomena in silicon-on-insulator MOSFETs.

The extensive investigation of poly-Si TFTs has identified the performance artefacts discussed in this chapter, and the understanding and control of these effects has enabled the mass production of stable, high performance poly-Si TFTs for a variety of flat-panel display applications. As discussed in Chap. 7, these have focussed on the small/medium diagonal display market, and include both AM-LCDs and AMOLEDs.

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Chapter 9
Transparent Amorphous Oxide Semiconductor TFTs

Abstract Transparent amorphous oxide semiconductors, especially a-InGaZnO, are the most recent TFT materials of interest for driving active matrix displays. The high level of activity on these devices is because, even though the material is amorphous, it can offer a carrier mobility of 10 cm^2/Vs, or more. This is 10–20 times greater than a-Si:H, and the higher mobility is advantageous for driving organic light emitting diode, OLED, displays. Also, due to the amorphous nature of the material, it may have better uniformity than poly-Si, which is the currently preferred TFT technology for commercial, hand-held AMOLED displays. In this chapter, the material and electronic properties of AOS materials are reviewed, paying particular attention to a-InGaZnO TFTs. Other topics include device architecture and fabrication, the DOS and conduction mechanisms within the material, overall device performance, and bias stability issues.

9.1 Introduction

The current interest in transparent amorphous oxide semiconductor, AOS, TFTs was stimulated by the publication, in 2004, of the operation of amorphous indium-gallium-zinc oxide, a-IGZO, TFTs on low temperature, flexible, polymer substrates [1]. Since that time, the work in the AOS area has rapidly developed, with a-IGZO TFT addressed active matrix displays being demonstrated for LCDs [2], OLEDs [3], and electrophoretic e-readers [4]. This interest is due to the particular properties of AOS TFTs, which make them well suited to the FPD application. Firstly, this amorphous material has Hall-effect and field-effect electron mobilities of $\sim$10 cm^2/Vs, or more, which is >10 times higher than a-Si:H [5]. This makes the material more appropriate than a-Si:H for driving AMOLED displays, and it is even relevant for addressing 120 Hz, high resolution AMLCDs, where a carrier mobility of $\sim$2 cm^2/Vs is required for display diagonals >90 inches [5, 6]. Indeed, the mass-production of large size, high resolution AMLCD TVs with AOS pixel TFTs has been forecast to begin in 2012 [7]. In addition, its amorphous nature should mean that it will have better uniformity than poly-crystalline

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materials [5]. Hence, there is interest in AOS TFTs for large diagonal AMOLED TVs, where poly-Si (which is presently used in small diagonal AMOLED displays) is perceived to be too non-uniform for this application [3]. However, this argument is not yet proven, and, as discussed in Sect. 7.2.2.4, advanced crystallisation techniques have improved the uniformity of laser crystallised poly-Si [8].

In addition to the higher electron mobility compared with a-Si:H, a-IGZO TFTs also have a better overall performance, with state-of-the-art devices having a sub-threshold slope of 0.12 V/dec [10], compared with 0.4 V/dec in a high quality a-Si:H TFT [11]. Both these mobility and sub-threshold slope differences are indicative of a lower density of trapping states near the conduction band edge in a-IGZO [5].

From a device fabrication point of view, the material can be deposited by sputtering at temperatures down to room temperature, and a further attractive feature of a-IGZO TFTs is that they can be fabricated with a simple contact metallisation scheme, without doped contacts, and a wide range of gate dielectrics have given acceptable performance [5].

These features of AOS TFTs are discussed in the following sections, starting with the background material properties in Sect. 9.2, and the device architecture and fabrication processes in Sect. 9.3. Device performance, including the DOS assessment, series resistance, and bias stability effects, are discussed in Sect. 9.4. Finally, the issues of complementary p-channel TFTs, and driver circuit integration in demonstrator displays are briefly reviewed in Sect. 9.5.

9.2 Material Properties

One of the key features of the AOS materials is their large carrier mobility, even in the amorphous state, where the mobility may be 50 % or more of the crystalline mobility. This is very different from the a-Si:H/c-Si comparison, and the key to understanding this difference lies in the difference between the covalent bonding of Si and the ionic bonding of the AOS materials [5]. As discussed in Sect. 6.2, the conduction and valence bands of Si are formed from hybridised sp^3 states, and, in the amorphous Si network, strained and broken Si–Si bonds lead to localised band tail states and deep gap states, respectively. The band tail states reduce the field effect mobility by >10 times, compared with the band mobility, which itself is very low due to the carrier scattering distance in the extended states being of the order of the inter-atomic spacing. In the ionic bonding configuration of AOS materials, due to charge exchange between the metal cation and the oxide anion (in, for instance, ZnO), the outer s-states of the metal ion are empty, and the outer p-states of the oxygen ion are filled. The charge exchange results in a Madelung potential, which separates the metal and oxygen ion orbitals, with the empty s-states of the metal cation predominantly forming the conduction band minimum, and the filled p-states of the oxygen anion mainly forming the valence band

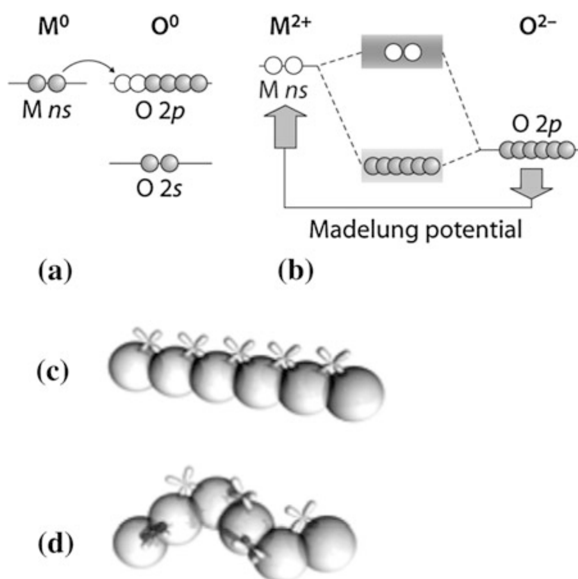


Fig. 9.1 Schematic diagram of (**a**) charge transfer and (**b**) band gap formation process in an ionic oxide semiconductor. Molecular orbital representation of the conduction band bottom, showing carrier conduction pathways in (**c**) crystalline and (**d**) amorphous oxide semiconductor (**a** and **b**: Reprinted by permission from Macmillan Publishers Ltd: NPG Asia Materials [5], copyright (2010); **c** and **d**: Reprinted from [12] with permission of IEEE)

maximum, as shown in Fig. 9.1a, b [5, 12]. The separation between these band edges was ~3 eV in the original pulsed laser deposited a-IGZO material [1] (giving these amorphous oxide materials their optical transparency), although more recent, sputter deposited a-IGZO layers have given Tauc optical gaps up to 3.7 eV [13]. For metal oxides, the spatial spread of the spherically symmetric metal s-state orbital is determined by the principal quantum number, n, of the metal ion [14]. For post-transition metals with $n \geq 5$, such as In, Ga and Sn, it is sufficiently large that there is an overlap between adjacent cations, as shown in Fig. 9.1c [12]. This leads to small electron effective masses and high electron mobilities, as found, for instance, in the transparent conducting oxide ITO. The illustration in Fig. 9.1c shows the s-state overlap for a crystalline lattice, and this overlap is still maintained in the disordered amorphous structure shown in Fig. 9.1d. Hence, these spatially extensive s-state orbitals, in the post-transition metal oxides, explain the relatively high carrier mobilities found in the transparent amorphous oxide semiconductors [5, 12].

The AOS material can be doped, but, due to the flexibility of the ionic bond, this is not achieved by introducing different valence atoms (as is standard with group IV semiconductors), but most commonly occurs via the oxygen vacancy. The vacancy results in a non-bonded metal cation producing a shallow donor level [5]. The vacancy concentration is determined by the oxygen partial pressure during deposition, and, for a low partial pressure, the interrelationship between the composition of the ternary structure In_2O_3-Ga_2O_3-ZnO, the Hall mobility and the as-grown doping level is shown in Fig. 9.2a [5]. Over most of this compositional space, the material is amorphous, although it tends to be crystalline within ~10 % of either pure ZnO or pure In_2O_3. However, as will be seen along the base of the triangle, this structural difference had little effect upon the Hall mobility, whereas increasing the

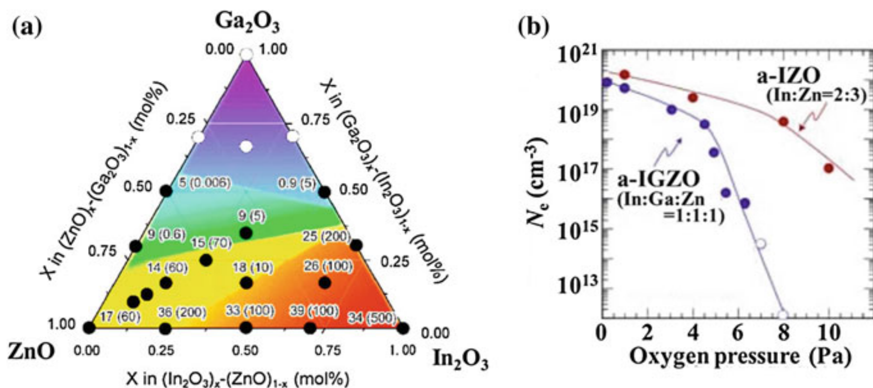


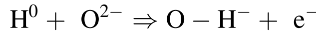
Fig. 9.2 **a** Compositional dependence of Hall effect mobility and free carrier density (in parentheses, with units of 10^{18} cm^{-3}) in the In_2O_3-Ga_2O_3-ZnO system, and **b** dependence of free carrier density on the O_2 partial pressure during deposition of a-IGZO and a-IZO films. (Reprinted from [12] with permission of IEEE)

Ga content reduced both the mobility and the free carrier density. A low free carrier density is required in TFT material to ensure a low off-current, and Ga plays an important role in this respect, because its strong Ga-O bond reduces the O-vacancy density [5]. In addition, the free carrier concentration can be further reduced by increasing the oxygen partial pressure during deposition, as shown in Fig. 9.2b. This also compares a-IGZO with IZO, and demonstrates the importance of Ga incorporation in the material [12]. For this reason, $InGaZnO_4$ (IGZO) is the preferred composition for TFTs, even though it is not the highest mobility material [12].

The oxygen vacancy has been referred to as forming a shallow donor level in IGZO material; however, the vacancy is a negative U-centre, with the fully occupied, neutral level in the lower half of the band-gap [5, 15]. This level occurs within a relatively un-relaxed, 'stoichiometric' lattice, whereas the formation of the charged centre is accompanied by an inward relaxation of the metal ions around the oxygen vacancy location [15, 16]. Given the lattice relaxation necessary to form the ionised donor level, it is more likely to be formed during film growth (under low oxygen partial pressure) [15, 16], although an increased free carrier density has also been found in material subjected to prolonged vacuum exposure [17]. This was attributed to donor formation by effusion of oxygen from the material, and the process was reversible by re-exposing the sample to an oxygen ambient. Both types of oxygen vacancy may be found in a-IGZO films, and the instability caused by negative bias illumination stress, NBIS, discussed in Sect. 9.4.3.2, is believed to be due to photo-ionisation of the deep lying neutral oxygen vacancy [18]. More work is currently required for a fuller understanding of NBIS, and of the conditions determining the relative concentrations of neutral and ionised oxygen vacancies in as-prepared thin films of a-IGZO.

Low temperature annealing in a H_2-N_2 gas mixture has also been found to increase the free electron concentration in a-IGZO [12], and calculations of the electronic properties of various point defects in c-IGZO have shown that

interstitial hydrogen bonds to an oxygen ion, forming a donor level above the conduction band edge [19]. A similar interaction has been found from bonding calculations in a-IGZO [12], with H always forming an O–H bond. It is suggested that the donor activity results from the following reaction [12]:



$$H^0 + O^{2-} \Rightarrow O - H^- + e^-$$

This reaction is believed to underlie the susceptibility of unpassivated a-IGZO TFTs to ambient moisture effects, in which water immersion [20] shifted the TFT threshold voltage in a negative direction. As with the vacuum/oxygen exposure results discussed above, the effect of water immersion was also reversible, in this case by baking the sample in vacuum to break the O–H bonds and to effuse the water molecules [20].

Finally, the Hall mobility was found to increase with increasing carrier density, and was attributed to percolation limited transport around potential barriers within the conduction band [12, 21]. A schematic illustration of the a-IGZO density of states, DOS, is shown in Fig. 9.3, and includes the percolation barriers, which are indicated by their average height, E_{center}, and distribution, ΔE. Also shown in this figure is the location of the shallow donor levels, and a low density band-tail at the conduction band edge. As the valence band edge is composed of p-type states, these do not have the overlapping orbitals of the conduction band states, and there is a large density of localised states, as well as deep states above the valence band mobility edge [12], which inhibit useful p-channel TFT behaviour. The a-IGZO DOS and electron conduction mechanisms are discussed further in Sect. 9.4.2.

9.3 TFT Architecture and Fabrication

Unlike a-Si:H and poly-Si TFTs, AOS TFT technology is still developing, and there is not an established process around which a consensus has emerged,

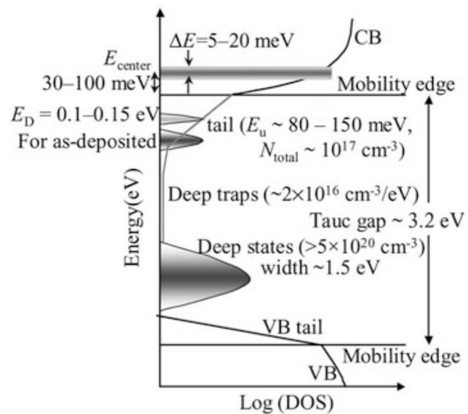


Fig. 9.3 Illustrative a-IGZO density of states distribution, DOS, showing band edges, band-gap states and distribution of percolation potentials in the conduction band. (Reprinted from [12] with permission of IEEE)

leading to a well-defined manufacturing technology. However, there are clearly emerging trends, and these are reviewed below, with a particular focus on the TFT architecture and processes used to fabricate high quality demonstration displays [2, 3, 6, 13].

9.3.1 Architecture

Although the original demonstration a-IGZO TFT was a top-gated, coplanar structure [1], the presently preferred configuration for demonstration displays is bottom gated, with either staggered [3, 13, 22] or coplanar [2, 23] source and drain electrodes, as illustrated in Fig. 9.4a and b, respectively [3, 23]. The inverted staggered structure is more widely used, but, predominantly, with the etch–stop configuration shown in Fig. 9.4a [3]. The two principal inverted staggered TFT architectures, of back-channel etched (BCE) and etch-stop (ES), were discussed in Sect. 5.3, in the context of a-Si:H TFTs, where it was shown that the BCE architecture was preferred for mass production. However, for the a-IGZO TFTs, the preference is for the ES architecture because of the sensitivity of the back channel to ambient effects, and also to damage and donor formation during the deposition and etching of the source and drain metals [24]. This was demonstrated in a direct comparison of BCE and ES TFTs, in which the ES TFTs had an SiO_x etch-stop layer deposited by PECVD, and both device types had sputter deposited and dry etched MoW source and drain metals. With a 200 nm thick PECVD SiN_x gate dielectric, the sub-threshold slopes and electron mobilities of the BCE and ES TFTs were 3.5 V/dec and 0.59 V/dec, and 5.0 cm^2/Vs and 35.8 cm^2/Vs, respectively [24]. Hence, the damage to the unprotected back surface of the a-IGZO film in the BCE TFT resulted in almost an order of magnitude degradation in device performance. The choice of ES layer was also crucial in obtaining high performance. For a-Si:H TFTs, a-SiN_x:H is usually used in the ES structure, but, when PECVD SiN_x was used in the a-IGZO TFTs, the gate modulation of the channel current was lost, and the devices became simple resistors due to a large free carrier concentration of $\sim 4 \times 10^{19}$ cm^{-3} in the material [24]. This was attributed to hydrogen entering the a-IGZO film from the SiN_x layer, and either acting as a donor [25], or reducing the a-IGZO and introducing oxygen donor vacancies. To avoid these effects, SiO_x is the preferred ES/passivation layer in many publications [2, 3, 13, 22–24], with some groups evaluating both PECVD and sputter deposition, given the latter's lower H-content [26]. The SiO_x has also been used as the uppermost film in a double layer passivation process [13, 22], with an alternative material placed in direct contact with the back face of the a-IGZO. For instance, a DC sputter deposited layer of Al_2O_3 gave excellent bias stability results, as well as good passivation [22]. In another case, the lower film of Ti, from a sputtered double layer of Ti and Mo for the source/drain metallisation, was exposed to an oxygen plasma to convert it to an insulating TiO_x passivation layer, as depicted in Fig. 9.5 [13]. After the definition of the metallisation pattern, a final capping layer

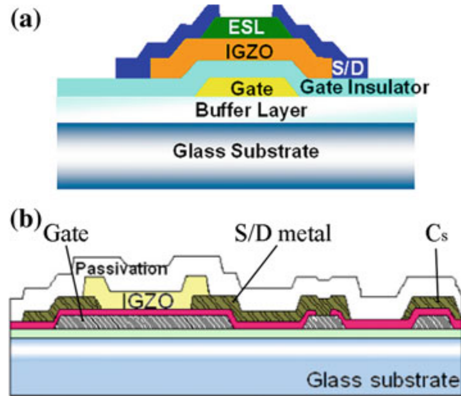


Fig. 9.4 Cross-sections of a-IGZO TFT structures **a** inverted staggered etch-stop (Reprinted from [3] with permission of SID), and **b** inverted coplanar (Reprinted with permission from [23]. Copyright (2010) The Japan Society of Applied Physics)

of PECVD SiO_x was added to this structure. This approach had the additional benefit of a reduced number of deposition stages, as the passivation layer was directly formed from the source/drain metallisation.

As discussed in Sect. 5.3, the inverted staggered, rather than the inverted coplanar structure, is exclusively used with a-Si:H TFTs in order to position the n^+ layer on the top of the device stack, so that it could be selectively etched to form the source and drain contact regions during final patterning. As doped contact regions have not been routinely implemented with the a-IGZO TFTs, this constraint is removed, and the source and drain metal regions, in the coplanar structure, can be deposited, and defined, before the deposition of the a-IGZO layer itself, as illustrated in Fig. 9.4b [23]. This architecture also has the advantage that the a-IGZO layer is not exposed to the deposition and etching processes required for the source/drain metallisation, and requires one less mask than the ES process [6], as discussed further in Sect. 9.3.2.4. However, the structure still incorporated a SiO_x passivation film on top of the completed device structure [6, 23], in order to protect it against moisture in the ambient, and from damage during subsequent display processing.

In addition to these conventional architectures, there is interest in self-aligned structures to reduce the overlap capacitance in pixel TFTs, and also as a route to future channel length reduction [27, 28]. A bottom gated self-aligned structure has been demonstrated, in which the transparency of the a-IGZO layer has been exploited to use the bottom gate as a UV exposure mask for the definition of the etch-stop layer by back-face illumination [27]. This process reduced the total mask

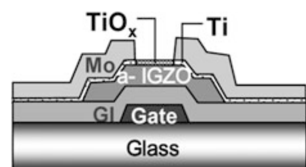


Fig. 9.5 Cross section of inverted staggered etch-stop TFT, showing the local conversion of Ti source/drain metal to a TiO_x passivation/ ES layer. (Reprinted from [13] with permission of SID)

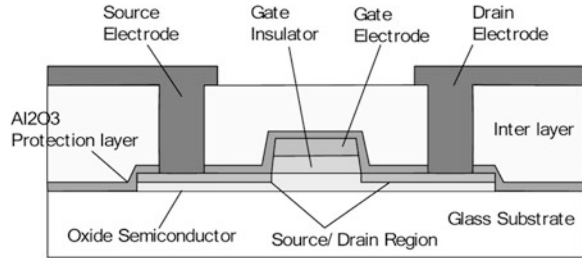


Fig. 9.6 Cross-section of a self-aligned top-gated TFT. (Reprinted from [28] with permission of SID)

count for the ES process by one, as well as reducing the gate/drain overlap to 2μm. A more novel process has been used to produce the self-aligned top-gated TFT, shown in Fig. 9.6 [28], in which the total overlap of the gate and source/drain regions was reduced to 0.8 μm or less. This structure incorporated low resistance contacts to the a-IGZO layer, which were self-aligned to the gate. In order to form them, after the definition of the gate electrode and the removal of the gate dielectric around it, the structure was coated in a thin film of Al, and annealed at 300 °C in oxygen. During this process, the lower surface of the Al reacted with the a-IGZO to form a low resistance contact, whilst the upper surface of the Al was oxidised to form an insulating layer of Al_2O_3. The self-aligned, low resistance source and drain regions were contacted by the top metallisation pattern through windows in the interlayer dielectric. TFTs with a minimum channel length of 4 μm were fabricated by this process, and high quality transfer characteristics, as well as good gate bias stability, were reported [28].

9.3.2 Fabrication Processes

9.3.2.1 a-IGZO Layer

The active a-IGZO layer is typically ~30−60 nm thick in the FPD demonstrator TFTs, and is usually deposited at room temperature by DC sputtering [2, 3, 6, 13, 26]. The sputter targets had a compositional ratio of In_2O_3:Ga_2O_3:ZnO in the range 1:1:0.5 to 1:1:1, and the sputtering gas was an Ar/O_2 mixture. Whilst other techniques, including pulsed laser deposition [1] and RF sputtering [24], have also been used, the advantages of DC magnetron sputtering are that it is widely used for ITO deposition in AMLCDs [29], and the equipment is readily available for large area depositions.

9.3.2.2 Gate Dielectric

In the demonstration displays, the gate dielectric was 200 nm thick, and was most commonly SiO_x deposited by PECVD [3, 6, 22], although in some cases PECVD

SiN_x [30] and SiO_xN_y [23] were also used. Where SiN_x was used, there was no apparent effect on threshold voltage, in spite of the high density of positive charge which is customarily found in a-SiN_x:H layers. A fuller discussion of the PECVD deposition of a-SiN_x:H and SiO_x layers can be found in Sects. 5.5.3 and 7.3.1, respectively.

In view of the bottom gate structure, and the absence of Fermi level dependent meta-stability effects (such as seen in a-Si:H), the particular gate dielectric and its deposition procedure have, in principle, little impact upon the subsequently deposited a-IGZO layers, thereby affording a broad choice of gate dielectric. This is apparent from the successful use of a-SiN_x:H, SiO_x and SiO_xN_y as cited above; however, these high quality PECVD dielectrics require a deposition temperature of ~300 °C, or higher, and are more suited to glass than flexible, polymer substrates. Indeed, the original paper reporting a-IGZO TFTs on low temperature, flexible PET films used room temperature deposition of Y_2O_3 as the gate dielectric [1]. Hence, there is continuing interest in alternative gate dielectrics, and in reduced deposition temperatures compared with conventional PECVD depositions. As part of this broad investigation, a range of low temperature, high-k dielectrics has been examined, in which it is agued that the high dielectric constant can compensate for a poorer interface compared with the higher quality PECVD films [31]. Amongst the dielectrics examined have been Ta_2O_5 ($k = 29$) [32], ZrO_2 ($k = 25$) [33] and HfLaO ($k = 25$) [34], all of which were deposited by room temperature sputtering, with a film thickness in the range 200−300 nm (i.e. comparable to the PECVD dielectrics). However, only HfLaO gave a notably low value of sub-threshold slope, S, of 0.076 V/dec, whereas Ta_2O_5 and ZrO_2 were ~0.6 V/dec (compared with 0.29 V/dec for a PECVD SiO_x dielectric [3]), suggesting that these two high-k dielectrics were, indeed, producing a poor quality interface. In addition, the TFT with a Ta_20_5 dielectric had a high gate leakage current, and a channel current on:off ratio of 10^5, compared with $> 10^8$ in the SiO_x device [3]. The other two dielectrics had on:off ratios of $1\text{-}5 \times 10^7$, and the particularly low value for Ta_2O_5 [31, 32] has been attributed to its small band gap, and small conduction band offset with respect to the a-IGZO layer [31, 35]. A compromise approach has been a room temperature sputtered composite high-k and SiO_2 dielectric, such as Ta_2O_5–SiO_2, and HfO_2-SiO_2, or even a tri-layer stack of SiO_2/HfO_2-SiO_2/SiO_2, leading, in the first case, to an improved on:off ratio of 3×10^6, and 2×10^7 for the triple stack [31].

From the above discussion, it is clear that there is on-going research to identify the optimum gate dielectric for AOS TFT fabrication on low temperature, flexible substrates. In addition to the impact of the gate dielectric layer on the static TFT characteristics, it also needs to be evaluated in terms of the bias stability of the device, and this topic is reviewed in Sect. 9.4.3.

9.3.2.3 Post Deposition Annealing

Post-deposition annealing of the a-IGZO TFT structure is commonly used, and it has been shown to lead to a major improvement in device performance and uniformity [10]. In that study, the effects of 400 °C annealing, in dry and wet oxygen, were investigated using inverted staggered TFTs fabricated on thermally oxidised n^+ silicon substrates, and the a-IGZO layers were produced by pulsed laser deposition at two different oxygen partial pressures. This difference in deposition conditions led to threshold voltage differences of 6 V, as shown by the transfer characteristics in Fig. 9.7a. However, the dry annealing removed this difference, and gave a common threshold voltage of ~ -1 V, and a reduction in S values from 0.4–0.5 V/dec to a common value of $\sim$0.25 V/dec [10]. Wet oxygen annealing had a similar effect, in terms of removing the built-in differences due to different oxygen partial pressures during deposition, and the overall effect was a function of the water partial pressure, as shown in Fig. 9.7b. At the optimum water partial pressure of $\sim$20 %, the wet annealing was more effective than the dry annealing, and normalised the threshold voltage to $\sim$1 V and S to $\sim$0.12 V/dec [10]. In addition, both dry and wet annealing improved the overall uniformity of a given set of TFTs, and, once again, the wet annealing was the most effective in this respect. Hence, the post-deposition annealing of a-IGZO, especially in a wet

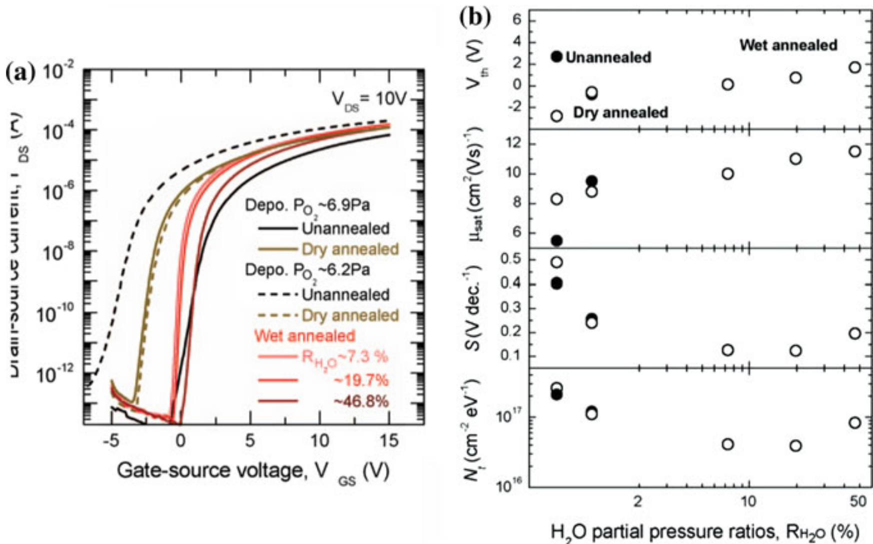


Fig. 9.7 **a** The influence of deposition partial pressure of O_2, and post-deposition annealing on TFT transfer characteristics, and **b** effect of water partial pressure during post-deposition annealing on TFT parameters {open (closed) circles 6.2 Pa (6.9 Pa) O_2 partial pressure during deposition}. (Reprinted with permission from [10]. Copyright (2008) American Institute of Physics)

oxygen ambient, improved device performance, and uniformity, and reduced the dependence of the device characteristics on the initial layer deposition conditions.

To stabilise the a-IGZO film, post-deposition annealing is routinely applied to the TFTs used for demonstrator displays [3, 6, 13, 22, 23], and is typically 1–2 h in the temperature range 250–350 °C, although the ambient is rarely specified.

9.3.2.4 Metallisation

The choice of gate and source/drain metals is determined by considerations of line resistance, processability (to include deposition by sputtering), and experience within the LCD industry. Accordingly, in some instances, Mo [3, 22] or Ti/Mo [13] has been used for the metallisation in inverted staggered devices, and, as discussed in Sect. 9.3.1, the Mo was etched away over the channel region, in the latter case, to selectively expose Ti to an oxygen plasma, which formed a dual-purpose TiO_x passivation and etch-stop layer [13].

A combined Ti/Al/Ti layer was used in some inverted coplanar TFT structures [23], and, as a consequence of the a-IGZO post-deposition anneal, the Ti reduced the a-IGZO adjacent to it to produce a layer of electron-rich, high conductivity material, thereby reducing the contact resistance between the metallisation and the channel [23].

9.3.2.5 Process Flow

The 4-mask process flow for the inverted coplanar TFT is shown in Fig. 9.8 [6], in which the mask definition stages are the definition of the gate metal (M1), the

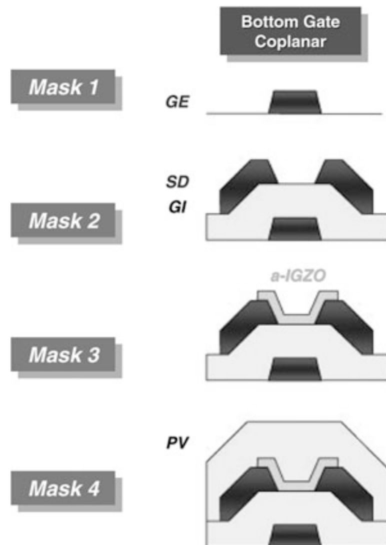


Fig. 9.8 Inverted coplanar TFT process flow. (Reprinted with permission from [6]. Copyright (2011) The Japan Society of Applied Physics)

source/drain metal (M2), the a-IGZO layer (M3) and the contact holes (M4) through the top passivation layer (not shown). For the inverted staggered etch-stop TFT, shown in Fig. 9.4a, the comparable stages are deposition and definition (M1) of the gate metal, deposition of the gate dielectric, deposition of the a-IGZO and etch-stop layers, definition of the etch-stop pad (M2), definition of the a-IGZO layer (M3), deposition and definition of the source/drain metallisation (M4), and deposition of the final capping/passivation layer and contact window opening (M5). Hence, the inverted staggered ES architecture requires one more mask than the inverted coplanar process.

9.4 a-IGZO TFT Performance

9.4.1 n-Channel Characteristics

The transfer characteristics of a high quality, inverted staggered etch-stop a-IGZO TFT, with W = 25 μm and L = 10 μm, are shown in Fig. 9.9a. This device, with a 200 nm thick SiO_x PECVD gate dielectric, had a field effect mobility of 21 cm^2/Vs, a sub-threshold slope of 0.29 V/dec and an on:off ratio of $>10^8$ [3]. Typical output characteristics [12], of an a-IGZO TFT with a saturation mobility of 11.8 cm^2/Vs, are shown in Fig. 9.9b, and the device displayed good current saturation at large V_D, and an absence of current crowding at low V_D.

However, even though current crowding is not an issue in high quality a-IGZO TFTs, the absence of a doped contact to the material has led to the investigation of series resistance effects in these devices [36–38], and its impact upon the field effect mobility as channel length is reduced [24]. If an ohmic resistance, R_s and R_d,

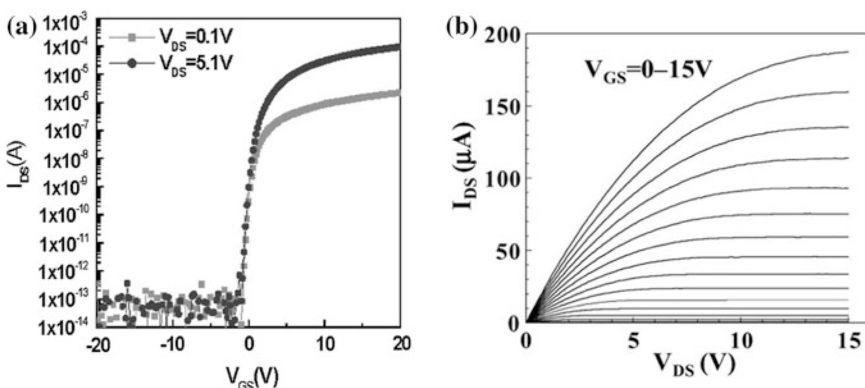


Fig. 9.9 High quality a-IGZO TFT characteristics (**a**) transfer characteristic of ES TFT (Reprinted from [3] with permission of SID, and (**b**) output characteristics (Reprinted from [12] with permission of IEEE)

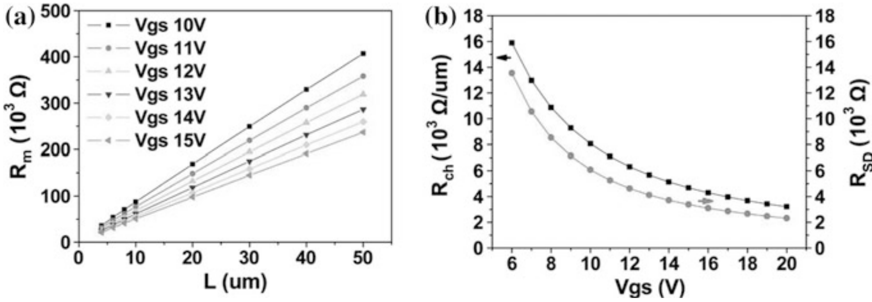


Fig. 9.10 **a** Total TFT resistance measured as a function of L and V_G, and **b** variation of channel resistance, R_{ch}, and series resistance, R_{SD}, with V_G. (Reprinted from [36] with permission of IEEE)

is present at the source and drain terminals, respectively, then the total measured device resistance, R_m, is

$$R_m = R_{ch} + R_s + R_d = R_{ch} + R_{SD} \tag{9.1}$$

where $R_{SD} = R_s + R_d$, and the channel resistance, R_{ch}, in the linear regime, can be obtained from Eq. 3.11 as:

$$R_{ch} = \frac{L}{\mu_n W C_i (V_G - V_T)} \tag{9.2}$$

Hence, for gate-bias-independent R_{SD}, a plot of R_m vs L, for any value of $V_G - V_T$, will give R_{SD} where the line intersects the R_m axis, and its slope will give the channel resistance per unit length at that gate voltage. An example of this measurement is shown for BCE inverted staggered a-IGZO TFTs in Fig. 9.10a, and the two extracted resistance parameters are shown in Fig. 9.10b [36]. There was not a common intersection point of the data sets, and the measurement yielded an approximate evaluation of the series resistance, R_{SD}, which was gate-bias-dependent. The background, and limitations, to this measurement procedure are briefly discussed below.

This resistance technique was originally developed for MOSFETs, and, with different values of $V_G - V_T$, it was found that the individual lines may have a common intersection point at a positive value of L, ΔL, rather than at L = 0 [39]. This was interpreted as channel shortening during processing, such that the effective channel length, L_{eff}, differed from the mask value by ΔL, and the value of R_{SD} was taken at this common intersection point (and not on the R_m axis). The technique has also been used with a-Si:H inverted staggered ES TFTs [40, 41], where a common intersection point was found at negative values of L, indicating an increase in the effective channel length due to current collection spreading along the n^+ doped regions. Using the above procedure, the identification of the common intersection point, and the related evaluation of the effective channel length, relies upon the series resistance being independent of gate bias, whereas,

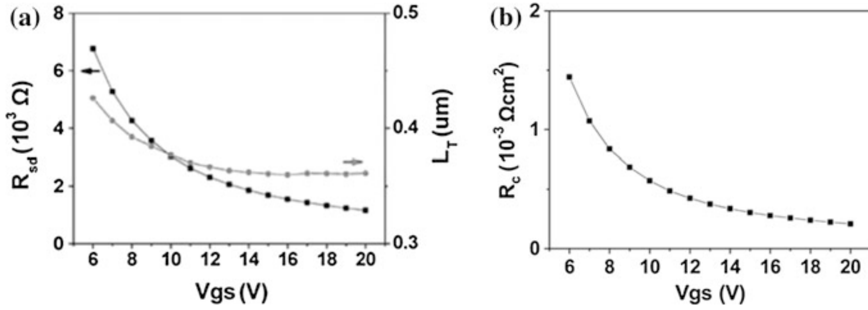


Fig. 9.11 Gate bias dependence of (**a**) change in effective channel length, L_T, and (**b**) specific resistivity of source and drain contacts (Reprinted from [36] with permission of IEEE)

for the a-IGZO TFTs in Fig. 9.10 this was not the case. A modified version of the common intersection measurement procedure was developed to handle this situation for MOSFETs, and, for each value of gate bias, V_G, a common intersection point was measured at closely paired values of V_G at $V_G \pm \Delta V_G$, where ΔV_G may be ~0.25 V. The technique was referred to as the 'paired V_G method' [42]. However, this procedure was not used with the above a-IGZO data set; instead, the intersection of each line with the x-axis in Fig. 9.10a was used as an expedient measure of the change in channel length, ΔL. This is shown as 'L_T' in Fig. 9.11a [36], demonstrating that the effective channel length was weakly gate bias dependent, and ~0.4 μm longer than the mask length. This was attributed to current spreading beneath the metal source and drain contacts.

Figure 9.10b showed that the total series resistance and the normalised channel resistance were comparable, and, therefore, for a device, with a channel length of 5 μm, the series resistance would be ~20 % of the channel resistance, and have an appreciable effect upon the on-current (although its impact would diminish as the channel length increased).

The gate bias dependent values of R_{SD} were attributed to the influence of the gate bias on the semiconductor/Mo contact on the top of the a-IGZO film. The values of R_{SD} in Fig. 9.10b were specific to the technology and geometry of the particular TFTs used, and these values may be corrected to remove the geometric effects either by normalising for the channel width (i.e. $R_{SD}W$ Ωcm), where this makes no assumption about the current distribution in the contact, or by normalising by contact area, A_c, to give the specific contact resistivity, R_c (i.e. $R_{SD}A_c$ Ωcm^2). This requires knowledge of the contact area, and the specific contact resistivity is usually measured in simple vertical contact structures of known area [43], rather than in TFTs. In the measurements here, it was assumed that the channel length extension of ~0.4 μm was an effective measure of the contact length, from which the specific contact resistance at each end of the channel was given by [36]:

$$R_c = \frac{WR_{SD}}{2}\frac{\Delta L}{2} \tag{9.3}$$

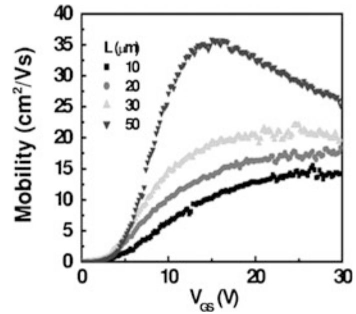


Fig. 9.12 Variation of field effect mobility with gate bias and channel length. (Reprinted with permission from [24]. Copyright (2007) American Institute of Physics)

The two factors of 2 in the denominator account for the measurements of R_{SD} and ΔL being the sum their effects at both ends of the channel. The dependence of R_c on the gate bias is shown in Fig. 9.11b, and, as with R_{SD}, it reduced with increasing gate bias.

In this study [36], the electron mobility was calculated from the slope of the inverse channel resistance/unit length against gate bias, and the intercept with the x-axis gave V_T. Thus, this procedure did not explicitly use the channel length to calculate mobility, but, in contrast, the more widely used field effect mobility calculation does, and, to give an accurate value of mobility, that would require both the use of the effective channel length, and the series resistance. However, by using long channel length TFTs to measure the field effect mobility, both of these corrections are minimised.

It can be assumed that the series resistance effects noted in this paper [36] are common, although the specific values will vary with the detailed processing conditions. A common example of a series resistance artefact is the reduction in field effect mobility with increasing gate bias and reducing channel length, as shown in Fig. 9.12, for an ES inverted staggered a-IGZO TFT [24]. From plots of total resistance as a function of gate length, the series resistance was again shown to be gate bias dependent. The gate width normalised resistance, WR_{SD}, at $V_G = 20$ V was $\sim$250 Ωcm, whereas the comparable figure for the data shown in Fig. 9.10a was $\sim$12.5 Ωcm, illustrating the variability between differently prepared samples. Indeed, some very short channel length TFTs, with L = 50 nm, have been reported with a field effect mobility of 8.2 cm^2/Vs, and good output characteristics, up to a drain bias of 10 V, as seen in Fig. 9.13 [44]. These were BCE inverted staggered TFTs, with a PECVD SiN_x gate dielectric, which was $\sim$40 nm thick, as was the a-IGZO layer. The device displayed very few short channel effects, including minimal drain induced barrier lowering, as is apparent from the tightly clustered transfer characteristics in the sub-threshold regime, and from the high impedance of the output characteristics. No doubt the thin SiN_x layer contributed to the suppression of short channel effects, but the device still had remarkably good characteristics given its channel length. (Short channel effects are discussed in greater detail in Sect. 8.7).

The detailed channel resistance measurements discussed above were for an inverted staggered BCE TFT [36], and a comparable study has been made of ES

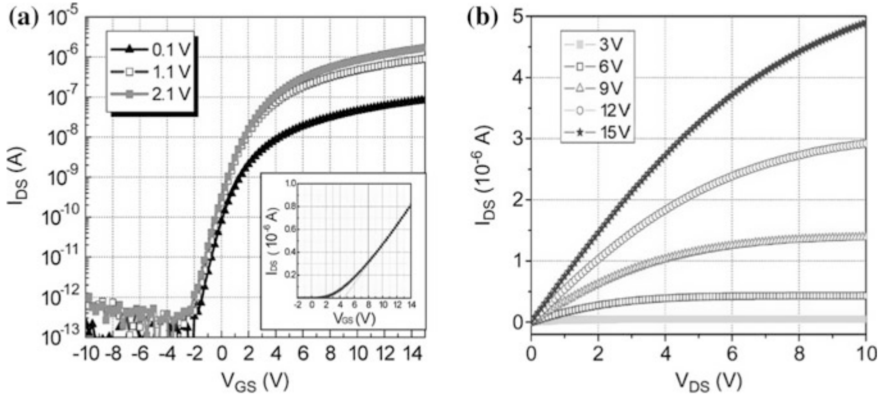


Fig. 9.13 I–V characteristics of short channel TFTs with dimensions W/L = 200/50 nm (**a**) transfer, and (**b**) output characteristics. (Reprinted from [44] with permission of IEEE)

TFTs [37], in which the defined channel length, determined by the width of the ES layer, had less control over the channel current than the separation of the source and drain contacts on top of the ES layer. The device structure is shown in Fig. 9.14a, and the conventional channel length, defined by the width of the etch stop layer, ESL, is given by L_{cnt}, and the separation of the source and drain contacts on ESL is given by L_{mask}. In this structure, the metals were MoW, the 200 nm SiN_x gate dielectric and the SiO_x etch-stop layer were both deposited by PECVD, and the 50 nm thick a-IGZO layer was deposited by RF sputtering [24, 37]. Figure 9.14b shows that the channel current was independent of the width of ESL, L_{cnt}, over the range 10–16 μm, whereas Fig. 9.14c shows that the current varied with the magnitude of L_{mask} over the range 4–10 μm [37]. In broad terms, these results suggest a channel current dominated by contact resistance effects, in which the contact resistance was determined by the magnitude of the overlap of the source and drain pads on ESL. Using the source/drain pad separation, L_{mask}, as the reference channel length, the dependence of R_m and ΔL on V_G were evaluated using the 'paired V_G method' [42], and the results are shown in Fig. 9.15. This demonstrated that, as V_G increased, the effective channel length, L_{eff}, increased beneath the overlap region towards the metal contacts at the edge of ESL (i.e. L_{eff} tended towards L_{cnt}) [37]. At the same time, the total series resistance, R_{ext}, decreased with V_G, where, from Fig. 9.14a:

$$R_{ext} = R_S + R_D + R_{ovS} + R_{ovD} = R_{SD} + R_{ovlp} \tag{9.4}$$

Further analysis of this data, including the separation of R_{SD} and R_{ovlp}, showed that both resistances reduced with increasing V_G, but R_{ovlp} was ~10 times less than R_{SD}, which itself was ~10 times less than the channel resistance. The width normalised series resistance was ~30 Ωcm at V_G-V_T = 10 V [37], which is of the same order as

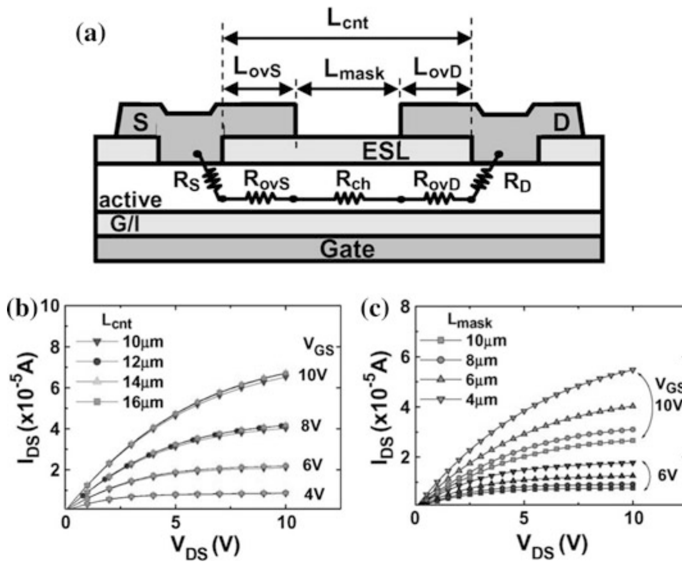


Fig. 9.14 **a** TFT structure, and definition of layout dimensions L_{cnt} and L_{mask}, **b** variation of output characteristics with channel length, L_{cnt}, for $L_{mask} = 4\mu m$, and **c** variation of output characteristics with L_{mask}, with constant channel length, $L_{cnt} = 16\mu m$. (Reprinted from [37] with permission of IEEE)

the value of 12.5 Ωcm measured at 20 V in the BCE device, shown in Fig. 9.10b [36]. A full explanation of these anomalous ES TFT results [37], which are not consistent with conventional MOSFET theory, has not been given, beyond noting that it appeared to be related to the accumulation of electrons beneath the overlap region as the device was turned-on more strongly. However, if this effect is common in a-IGZO TFTs with the ES architecture, then the conventional use of L_{cnt} to calculate the field effect mobility will overestimate its value (because L_{cnt} overestimates the effective channel length).

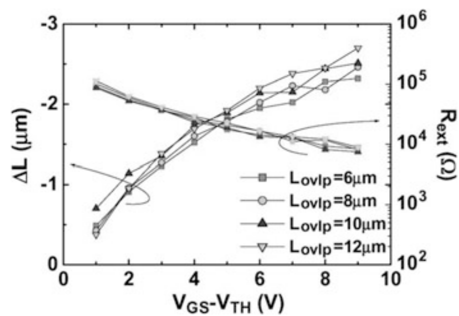


Fig. 9.15 Gate bias dependence of the change in effective channel length, ΔL, and the contact resistance, R_{ext}, for different values of the source/drain metallisation pad overlap on the etch stop layer. (Reprinted from [37] with permission of IEEE)

9.4.2 Conduction Process and Density of States Distribution, DOS

9.4.2.1 Conduction Process

Some of the characteristic features of the conduction process in a-IGZO films have been obtained from Hall effect measurements of doped films [12, 45, 46], such as those shown in Fig. 9.16. Among the key features was the increase in the Hall mobility with the doping density, in Fig. 9.16a. This is opposite to the behaviour seen in c-Si, where the mobility reduces due to increased charged impurity and electron–electron scattering. In Fig. 9.16b, the carrier density was temperature independent for densities above 10^{17}cm^{-3}, indicating that the material was degenerate, with the Fermi level above the conduction band edge [12]. This is also quite different from the behaviour of a-Si:H, where the band tail density was sufficiently great that the Fermi level never entered the conduction band. At the other end of the dopant range in Fig. 9.16b, the lightly doped material displayed a low temperature activation energy of 0.11 eV, as the material 'froze-out' with the electrons trapped on the donor level. Figure 9.16c showed that, in contrast to the temperature independent carrier density at moderate doping levels, the mobility continued to be thermally activated, until much higher carrier concentrations in excess of 2×10^{18}cm^{-3}, when it also became temperature independent [12]. Finally, Fig. 9.16d shows the electrical conductivity, σ, which is the product of the carrier density and mobility, and this was thermally activated at doping levels below 3×10^{19} cm^{-3}, but, only at the lowest carrier concentration was there a unique activation energy. At the intermediate doping levels, where there was not a simple Arrhenius plot, ln(σ) was shown to vary as $T^{-1/4}$ [46]. These results have been interpreted both in terms of a low DOS near the conduction band edge, which permitted the material to become degenerate, and a distribution of potential barriers within the conduction band, which are schematically illustrated in Fig. 9.17a [45, 46]. As indicated, electron transport around these barriers was by percolation, where there was assumed to be a Gaussian distribution of barrier heights, g(E), given by [46]:

$$g(E) = \exp[-(E - \phi_0)^2/(2\sigma_\phi^2)] \tag{9.5}$$

and ϕ_0 is the average barrier height, and σ_ϕ is the energy distribution width, as shown in the simplified diagram in Fig. 9.17b. In this work, the carrier mobility, μ, was related to the band mobility, μ_0, by the following percolation model expression [47]:

$$\mu = \mu_0 \exp\left[-\frac{q\phi_0}{kT} + \frac{(q\sigma_\phi)^2}{2(kT)^2}\right] \tag{9.6}$$

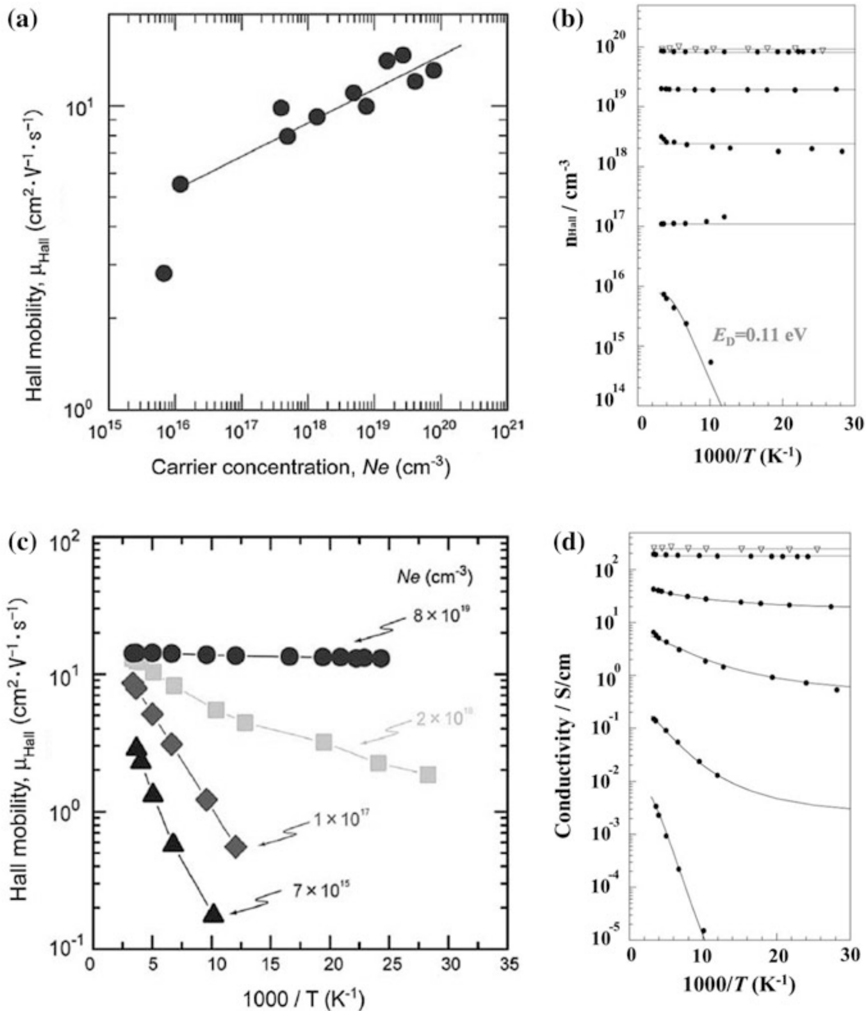


Fig. 9.16 Hall effect data from doped a-IGZO samples (**a**) variation of mobility with electron concentration. Temperature dependence of (**b**) electron density, (**c**) electron Hall mobility, and (**d**) conductivity. (**a** and **c**: Reprinted from [45] Copyright (2006), with permission from Elsevier; **b** and **d**: Reprinted from [12] with permission of IEEE)

The percolation process gave a direct physical explanation for the thermally activated mobility, and its eventual temperature independence at high enough carrier concentrations, when the Fermi level was above the maximum barrier height. The model also gave a good fit to the detailed experimental carrier concentration and conductivity data, as shown by the solid lines in Fig. 9.16b, d respectively [12, 46]. It also followed the $T^{-1/4}$ temperature dependence of the conductivity data (not shown) [46]. In establishing the data fits in Fig. 9.16b, d the

potential barrier height distribution was found to be dependent upon the background doping level, as shown by Fig. 9.17c [46], in which the average barrier height, ϕ_0, was 40–120 meV above the conduction band mobility edge, E_m, and the distribution width, σ_ϕ, was 20–30 meV.

9.4.2.2 Density of States Distribution, DOS

Given the dependence of the Hall mobility on the electron density, some caution is required in using device simulation to establish the DOS in TFTs, particularly when it is done by fitting a calculated transfer characteristic to a measured characteristic [48]. This is because, if the carrier-dependent mobility is ignored, then a field-effect mobility extracted at large V_G will overestimate its value at lower V_G values, with a corresponding overestimate of the DOS [49] (as discussed further below). Equally, the gate-voltage-dependent field-effect mobility itself cannot be

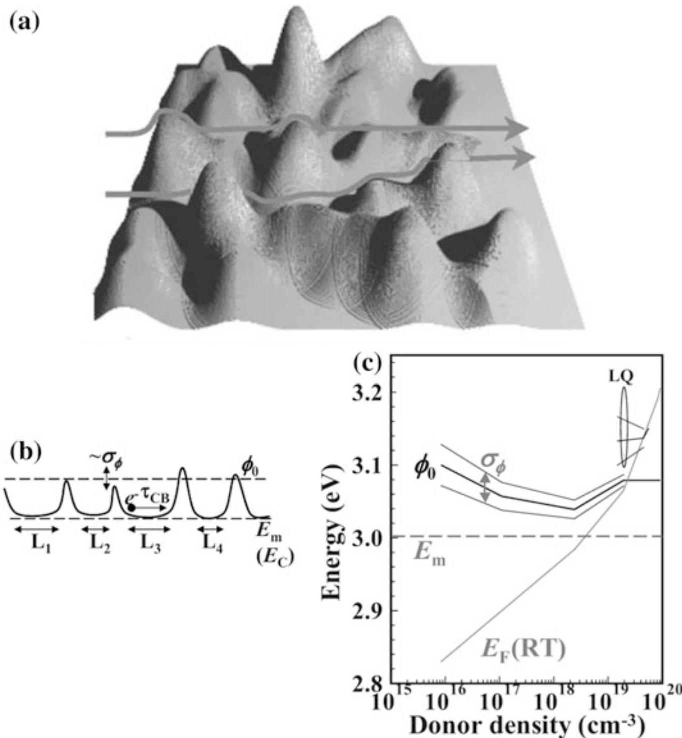


Fig. 9.17 **a** Schematic illustration of potential barriers in the conduction band, and percolation transport of electrons, **b** idealised potential barrier model used in calculations, and **c** variation of fitted barrier parameters with doping density. (**a**: Reprinted from [45] Copyright (2006), with permission from Elsevier; **b** and **c**: Reprinted with permission from [46]. Copyright (2010) American Institute of Physics)

used in the simulation, as this parameter is an artefact of carrier trapping in the DOS, as well as being affected by percolation effects. Indeed, the separation of carrier trapping and percolation phenomena on the field effect mobility should be done by explicitly analysing it for these two effects [21], as discussed below.

In view of these concerns, some authors have used C–V measurements on TFTs [48–50] (rather than I_d-V_G measurements) to determine the trap occupancy as a function of gate bias, because the electron trapping effects will be independent of the electron mobility [48–50]. The DOS thus established was then used to simulate the I_d-V_G characteristics, with the mobility as an adjustable parameter [50]. This yielded an average mobility at each value of gate bias, whereas a more detailed analysis extracted the mobility as a function of free carrier density [49], which could be directly compared with the carrier-dependent Hall-effect mobility.

The C–V measurements [51, 52] made use of the capacitor formed by the gate and the source/drain contact regions in BCE TFTs [48, 49], and the resulting C-V_G and I_d-V_G curves are shown in Fig. 9.18. The C-V_G curve was measured at a low enough frequency that the electrons could follow the frequency of the measuring signal. Using the band bending notation from Chap. 2, the surface potential, V_s, was extracted from the measured C-V_G curve by using [48, 51]:

$$Q_s = C_i(V_G - V_s) \tag{9.7}$$

$$dV_s/dV_G = 1 - (C_i)^{-1} dQ_s/dV_G = 1 - C_m/C_i \tag{9.8}$$

where C_i is the dielectric capacitance (measured at large positive gate bias), C_m is the measured capacitance, and V_s is calculated as a function of V_G by integrating Eq. 9.8:

$$V_s = \int_{V_{FB}}^{V_G} (1 - C_m/C_i) dV_G \tag{9.9}$$

From Gauss Law, the surface field, F_s, is related to the total surface charge, Q_s, by:

$$Q_s = -\varepsilon_0 \varepsilon_s F_s \tag{9.10}$$

Hence, the surface field can be calculated using Eqs. 9.7 and 9.10, together with the numerically calculated values of V_s from Eq. 9.9. The surface field is also related to the space charge density, ρ, by Poisson's equation:

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\varepsilon_0 \varepsilon_s} \tag{9.11}$$

and, for space charge densities dominated by trapped carriers:

$$\rho(x) = -q \int_0^V N dV \tag{9.12}$$

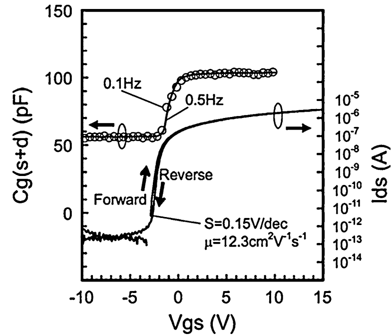


Fig. 9.18 C–V and I-V measurements on a BCE a-IGZO TFT. (Reprinted with permission from [48]. Copyright (2008) American Institute of Physics)

The trap density, N, was used iteratively, as an adjustable parameter, in Eqs. 9.11 and 9.12 to ensure that the values of V_s and F_s from those equations matched those established in Eqs. 9.9 and 9.10. The DOS measured by this procedure is shown by the solid lines in Fig. 9.19a [49], and illustrates the reduction in DOS produced by the post-deposition annealing in wet and dry oxygen, as discussed in Sect. 9.3.2.3. The decrease in the DOS was attributed to the reduction in oxygen deficiencies and structural relaxation as a result of the oxygen annealing procedure [49].

Having established the DOS and the relationship between V_s and V_G, the electron concentration could be calculated through the film at any given value of V_G. This carrier profile was then used in a computational procedure which stratified the a-IGZO film parallel to the dielectric interface, and progressively built up a mobility profile such that the integral of the vertical mobility and carrier concentration profiles accurately simulated the transfer characteristic [49], with the resulting dependence of mobility on electron concentration shown in Fig. 9.19b. This figure showed that the post-deposition annealing treatments primarily affected the DOS rather than the mobility, and also demonstrated that, for a given carrier concentration in the TFT, the electron mobility was lower than the Hall mobility in the doped samples. As indicated, the percolation model was fitted to the field-effect mobility data, and the mobility difference from the Hall samples was attributed to the doping reducing the mean percolation barrier height in the latter, as is apparent in Fig. 9.17c. Hence, this procedure separated the components of electron conduction in the a-IGZO TFTs due to trap limited conduction, determined by the DOS, and percolation conduction in the extended states.

The DOS values represented by the broken lines in Fig. 9.19a were obtained by simply fitting simulated transfer characteristics to measured ones [53], in which the electron mobility, in the simulations, was fixed at the conventionally measured field effect mobility at large gate bias. The overestimate in the DOS, over a substantial fraction of the band-gap, was attributed to the field effect mobility overestimating the correct, carrier-dependent mobility [49].

An alternative C-V_G technique was based upon the use of optical illumination during the measurement to increase the frequency response of the trapped carriers

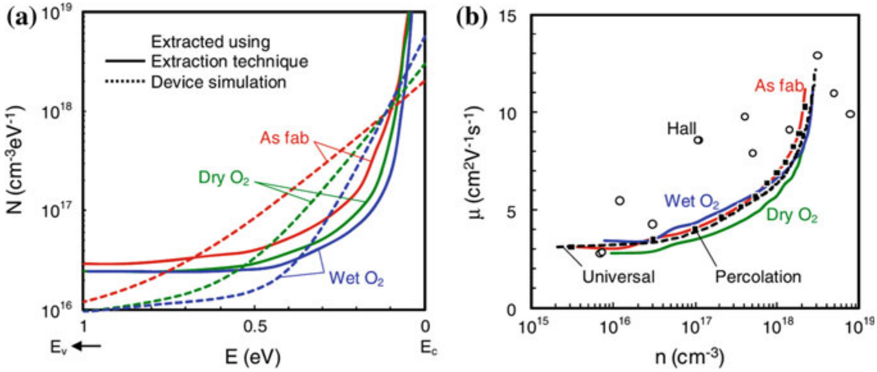


Fig. 9.19 **a** a-IGZO DOS measured by C-V technique (*solid lines*), and DOS measured by conventional TFT simulation (*broken lines*), and **b** extracted electron mobility as a function of the free electron concentration in TFTs (*solid lines*), average mobility (*broken line*), percolation model (*squares*), and Hall mobility in doped films (*open circles*). (Reprinted with permission from [49]. Copyright (2010) American Institute of Physics)

[50], and resulted in a DOS, which was qualitatively similar to that shown in Fig. 9.19a, but with a lower band edge density. The distribution, N(E), was represented by a double exponential of tail and deep states given by:

$$N(E) = 1.2 \times 10^{18} \exp - (E_c - E)/0.125 + 9.5 \times 10^{16} \exp - (E_c - E)/1.4 \tag{9.13}$$

in which the first term represented the tail state density [50].

As mentioned above, the field effect mobility itself has also been analysed in order to separate the DOS responsible for carrier trapping from the potential barrier distribution in the conduction band, controlling the percolation effects [21]. This was done by fitting the data to a model containing percolation-modulated trapping effects when the Fermi level was below the conduction band edge, and percolation transport alone when it was within the band. To account for the effect of the DOS on the mobility, the modified MOSFET equation was used [21, 54]. This was introduced in Chap. 6 (Eq. 6.27) in the discussion of on-state currents in a-Si:H TFTs, and the drain current expression is:

$$I_d = \frac{\mu_0 W C_i^{\alpha-1} \xi}{\alpha L} \left[(V_G - V_T)^{\alpha} - (V_G - V_T - V_d)^{\alpha} \right] \tag{9.14}$$

where μ_0 is the band mobility, and α and ξ are related to the tail state energy width, E_t, and the carrier density trapped in the tail states, N_t, by [54]:

$$\alpha = 2E_t/kT \tag{9.15}$$

$$\xi = \frac{(q\varepsilon_s \varepsilon_0 \alpha k T N_t)^{1-\alpha/2}}{\alpha - 1} \tag{9.16}$$

A Taylor expansion of Eq. 9.14 in the linear regime gives [54]:

$$I_d = \frac{\mu_0 W C_i^{\alpha-1}\xi}{L}\left[(V_G - V_T)^{\alpha-1}V_d\right] \tag{9.17}$$

And from Eq. 9.17, the field effect mobility is given by:

$$\mu_{FE} = \mu_0 C_i^{\alpha-2}\xi(\alpha-1)(V_G - V_T)^{\alpha-2} = \mu_0 A(V_G - V_T)^{2(E_{t/kT}-1)} \tag{9.18}$$

However, the band mobility, μ_0, must be modified to include the influence of percolation, so that, using Eq. 9.6, Eq. 9.18 becomes:

$$\mu_{FE} = \mu_0 \exp\left[-\frac{q\phi_0}{kT} + \frac{(q\sigma_\varphi)^2}{2(kT)^2}\right] A(V_G - V_T)^{2(E_{t/kT}-1)} \tag{9.19}$$

In summary, Eq. 9.19 describes the situation in which the Fermi level is below the conduction band edge, and transport is limited by both carrier trapping and percolation effects.

At a gate bias in excess of V_P, which is the threshold voltage for percolation, and occurs when the Fermi level is positioned at the conduction band edge, the mobility is controlled only by percolation, and the field effect mobility is given by [21]:

$$\mu_{FE} = \mu_0 \exp\left[-\frac{q\phi_0}{kT} + \frac{(q\sigma_\phi)^2}{2(kT)^2}\right] \exp\frac{q\Delta V_s}{kT} \tag{9.20}$$

Equation 9.20 is valid for Fermi level positions between the band edge and the maximum barrier height, ϕ_M, and ΔV_s corresponds to the change in Fermi level position within the band due to a change in band bending ΔV_s. By developing an approximate analytical expression for the free carrier density as a function of V_s, a relationship was established between ΔV_s and ΔV_G, from which the following expression was derived [21]:

$$\mu_{FE} = \mu_0 \exp\left[-\frac{q\phi_0}{kT} + \frac{(q\sigma_\phi)^2}{2(kT)^2}\right] B(V_G - V_P)^{4S} \tag{9.21}$$

where S is the ratio, $(D_B\text{-}W_B)/D_B$, of the percolation barrier width, W_B, and the inter-barrier spacing, D_B. Hence, both equations 9.19 and 9.21 show that the field effect mobility has a power law dependence on V_G of the form:

$$\mu_{FE} = K(V_G - V_{T,P})^\gamma \tag{9.22}$$

The values of K and γ were extracted from the solid line fits of the model to the experimental field effect mobility data shown in Fig. 9.20a (for a bi-layer a-IZO/a-IGZO TFT). These fits yielded a band mobility of 70 cm^2/Vs, values of ϕ_0, and σ_ϕ of 50 meV and 45 meV, respectively, and a band tail DOS given by:

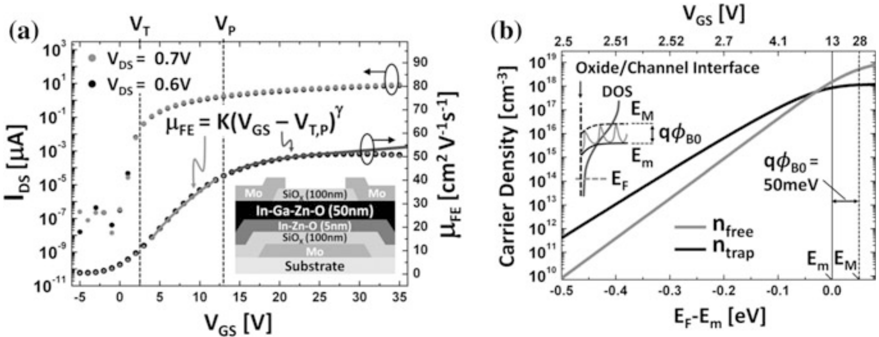


Fig. 9.20 **a** Measured values (data points) of I_{ds}, and μ_{FE} in an a-IZO/a-IGZO TFT, and the fitted expressions (*solid lines*) from equations 9.19 and 9.21, and **b** calculated variation of free and trapped electron densities with Fermi level position. (Reprinted with permission from [21]. Copyright (2011) American Institute of Physics)

$$N(E) = 4 \times 10^{19} \exp - (E_c - E)/0.035 \tag{9.23}$$

Using the extracted DOS parameters, Fig. 9.20b shows the calculated free and trapped carrier densities as a function of Fermi level position, and identifies the threshold voltage, V_P, for percolation limited conduction at 13 V [21]. This figure also illustrates the greater concentration of trapped charge, compared with free charge, when the Fermi level was more than ~0.05 eV below the conduction band edge, and confirms the trap limited conduction within this gate voltage range [21].

It is apparent that accurate DOS and percolation parameter assessment in AOS TFTs present a number of challenges, and different techniques are being explored. Also, whilst the currently published DOS values show some variability with device processing and layer composition, it is equally clear that the field effect mobility and tail state DOS values are consistently superior to those found in a-Si:H TFTs.

9.4.3 Bias Stress Instability

Due to its different bonding configuration, the meta-stable weak bond breaking observed in a-Si:H is predicted not to occur in AOS devices [55], but, even without this mechanism, both positive [53, 56–58] and negative [57, 58] gate bias instabilities have been widely reported in a-IGZO TFTs. The instability is predominantly a positive threshold voltage shift with positive gate bias stress, and is accompanied by minimal changes in mobility or sub-threshold slope. The shift is indicative of electron trapping at/near the AOS/dielectric interface, and is driven by the electron accumulation within the film. For negative bias stress, the threshold voltage shifts negatively, and is consistent with hole trapping. In addition, optical illumination

during bias stress results in a further instability process, which greatly increases the magnitude of the negative bias instability [57, 59], and reduces the positive bias stress shift [60], or even produces a net negative shift [61]. The optically enhanced instability has been attributed to photo-ionisation of the oxygen vacancy [18, 59, 61–63], and has also been correlated with persistent photoconductivity in the a-IGZO layer after the removal of the illumination [61–63]. Similar gate bias instability effects have also been reported in a wide range of other AOS TFT materials (including HfInZnO, AlSnInZnO, ZnInSnO, ZnInO, ZnSnO and ZnO) [62, 64, 65], and the a-IGZO results reviewed below can be taken to be broadly representative of the instabilities observed in other AOS materials of interest.

9.4.3.1 Gate Bias Instability

Typical examples, and artefacts, of positive gate bias instabilities are shown in Fig. 9.21a–d [53, 56]. These results were obtained after constant current stress (with positive gate and drain bias), from differently prepared inverted staggered TFTs. Figure 9.21a and b compare the shift in the transfer characteristics of an unannealed device with one given a post-deposition wet anneal at 400 °C [53]. As discussed in Sect. 9.3.2.3, anneals of this type are essential to improve the basic device characteristics, and they similarly reduce the magnitude of the gate bias instability, resulting in a small parallel shift of the transfer characteristics. From simulations [53], and a-IGZO film thickness dependent stability results [57], it was concluded that the defects were electron traps at the a-IGZO/dielectric interface in the annealed TFTs. A further aspect of device processing was identified by the results in Fig. 9.21c and d, in which an organic photoacryl and an inorganic, PECVD SiO_x passivation layer were compared in etch-stop TFTs [56]. The SiO_x layer was found to result in a smaller and more parallel shift of the transfer characteristics, and, indeed, the magnitude of the instability was found to be critically dependent upon the type of passivation layer used. The best results were obtained with a dense SiO_x layer, which suppressed the gate bias instability, and this was attributed to it providing an impervious barrier to the ingress of ambient oxygen and moisture into the top surface of the a-IGZO film, where these impurities led to trap generation within the film. Further work has directly correlated the instability of unpassivated, bottom gate devices with the relative humidity of the ambient during bias stressing [66], and also to water vapour exposure prior to the stress measurement [58]. A high quality passivation layer is, therefore, needed to minimise this contribution to positive gate bias instability, where the residual instability is associated with trapping at the dielectric/semiconductor interface.

A high quality dielectric layer is also necessary to reduce trapping within the layer itself [58, 67], and, for top-gate TFTs, the dielectric deposition process itself needs careful control to avoid damage to the underlying AOS layer [64]. For bottom gate TFTs, superior stability was obtained with a PECVD SiO_x gate dielectric compared with PECVD SiN_x [67], and the difference was attributed to a higher hydrogen content in the latter giving a larger trap state density.

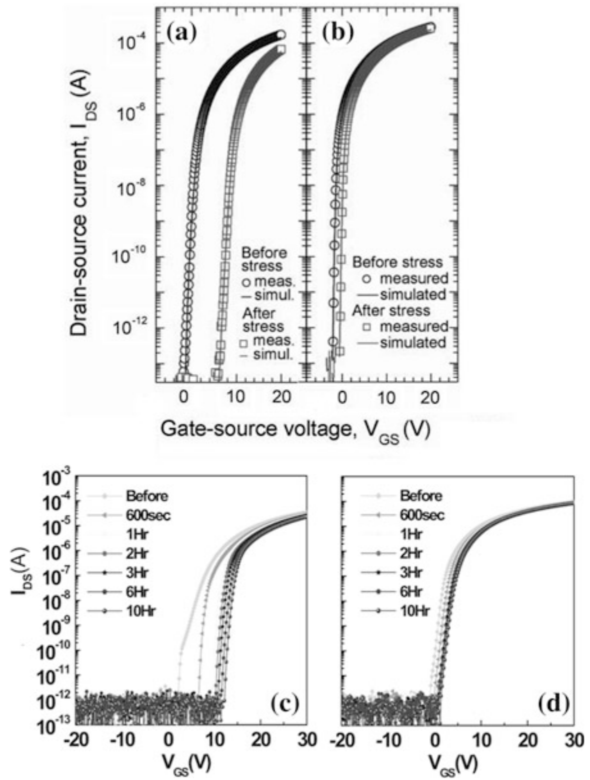


Fig. 9.21 Positive gate bias instabilities induced by constant current stress in a-IGZO TFTs (**a**) unannealed, and (**b**) with post-deposition wet anneal of a-IGZO at 400 °C (50 h stress at 5μA) (Reprinted with permission from [53]. Copyright (2009) American Institute of Physics). Time dependent stress at 10μA with (**c**) organic photo-acryl, and (**d**) inorganic PECVD SiO_x passivation layers. (Reprinted with permission from [56]. Copyright (2008) American Institute of Physics)

The time dependence of the positive gate bias instability was thermally activated, and followed a stretched exponential [57, 58, 60, 65] of the form:

$$\Delta V_T = (V_{GSt} - V_{T0})\left\{1 - \exp - \left(\frac{t}{\tau}\right)^{\beta}\right\} \tag{9.24}$$

where V_{GSt} is the stress bias, V_{T0} is the pre-stress threshold voltage, $\beta = T/T_0$, and the thermally activated time constant, τ, is given by:

$$\tau = v \exp\left(\frac{E_A}{kT}\right) \tag{9.25}$$

This process describes time dependent trapping into an exponential distribution of trapping states, with a characteristic width T_0. It is apparent that the kinetics of the instability process can be empirically modelled using the same formalism as used to describe gate bias instabilities in a-Si:H TFTs (see Sect. 6.4.1), although the physical mechanisms underlying the instabilities are quite different. Depending upon the details of sample fabrication, and the measurement conditions, activation energies, E_A, have been reported over the range 0.4 eV [60] to 0.7 eV [58].

The bias stress induced threshold voltage shifts were reversible after the removal of the gate bias, and the recovery characteristics also displayed a stretched exponential time dependence, but with a different activation energy compared with the initial instability results [58, 60].

As is apparent from the above discussion, careful device processing is required to minimise the positive gate bias instability, where important details include the choice of gate dielectric, defect removal in the AOS film by post-deposition annealing, and the implementation of a suitable passivation process over the device structure. With such processing, the negative gate bias instability is usually smaller than any residual positive gate bias instability. However, if negative gate bias stressing occurs under conditions of optical illumination, large negative threshold voltage shifts can occur [57, 59], even for devices showing good negative bias stability in the dark, as discussed in the following section.

9.4.3.2 Negative Bias Illumination Stress (NBIS)

Due to the transparency of the AOS materials, and the frequent use of transparent gate metals, there may be no natural light screening of the TFT when it is used for active matrix addressing of LCDs and OLEDs. As this will be a photon rich environment, the optical response of the TFTs, and the impact of optical illumination on their bias stability, have been widely studied [18, 57, 59, 61–63]. The NBIS instability is a negative shift in threshold voltage, and this occurs for both band-gap illumination ($E > 3.0$ eV), as well as for sub-band-gap illumination, as shown by the representative results in Fig. 9.22 [57]. These results were obtained from wet-annealed inverted staggered a-IGZO TFTs, and similar results have been obtained from top-gated TFTs [59], as well as from bottom-gated a-HfInZnO [62], and bi-layer a-InZnO/a-IGZO [61] TFTs passivated with SiO_x. The results in Fig. 9.22a showed that the devices were stable with negative gate bias stress in the

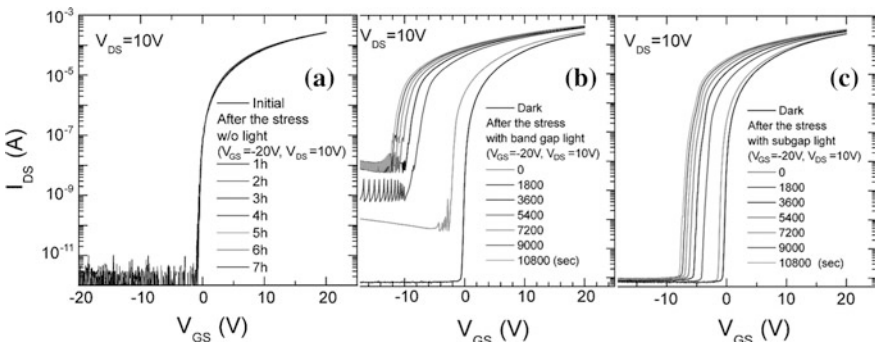


Fig. 9.22 Time dependent negative bias stress effects (V_G = -20 V) on TFT transfer characteristics (**a**) dark, (**b**) illumination at E = 3.4 eV, and (**c**) illumination at E = 2.7 eV. (Reprinted from [57] with permission of SID)

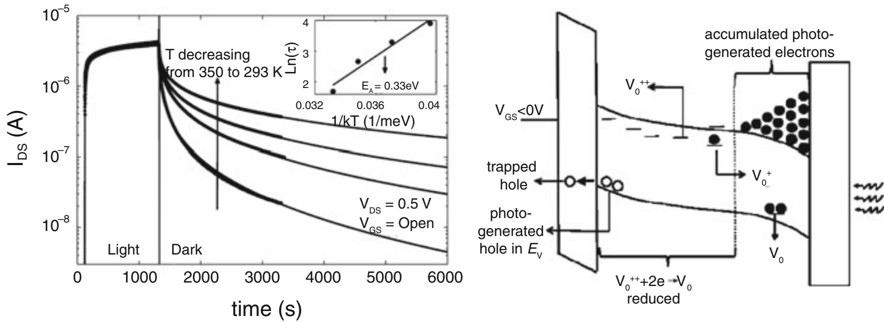


Fig. 9.23 **a** Time and temperature dependent dark relaxation of channel current after illumination (Reprinted with permission from [62]. Copyright (2010) American Institute of Physics), and **b** TFT band bending diagram during NBIS, showing shallow donor formation at the front of the film, and electron accumulation at the back of the film. (Reprinted from [61] with permission of SID)

dark, but, with both 3.4 eV (365 nm) band-gap illumination and with 2.7 eV (460 nm) sub-band visible illumination (in Fig. 9.22b and c, respectively), the threshold voltage was negatively shifted, and there was an associated time-dependent deterioration in the sub-threshold slope and the mobility values as well [57]. The shift in the transfer characteristics, and the increase in sub-threshold slope, are indicative of NBIS-induced positive charge trapping and trap generation in the upper half of the band-gap, respectively. Although the effects were greatest with band-gap light, more attention has been paid to the sub-band light, as this is the wavelength range experienced by the addressing TFTs in active matrix displays. Even without a negative gate bias, optical illumination alone shifted the threshold voltage negatively, as shown by the zero stress time results in Fig. 9.22b, c.

Following the termination of the NBIS tests, and the removal of the illumination and gate bias, there was a slow and thermally activated relaxation of the characteristics over a period of many hours, irrespective of whether bias had been applied or not. An example of the relaxation of the channel current (at $V_G = 0$ V), following illumination alone, is shown in Fig. 9.23a, where the data has been fitted by a stretched exponential, and the insert shows the relaxation activation energy. The illumination-induced threshold voltage shift (both without and without bias [61]), leading to the large, dark channel currents, is referred to as persistent photoconductivity [61, 62].

The above effects have been attributed to photo-ionisation of the neutral oxygen vacancy, V_0 [18, 59, 61, 62]. This vacancy level is in the lower half of the band gap, and, by virtue of its usual neutral charge state and its position below the Fermi level, it does not usually influence the operation of n-channel TFTs. However, under negative gate bias it is raised towards the Fermi level at the surface, and sub-band white light can photo-ionise it by exciting electrons to the conduction band, producing positively charged V_0^+ and V_0^{++} centres. As the oxygen vacancy is a

negative-U centre [18, 62], the ionised levels are above the neutral level, in the upper half of the band gap, and the V_0^{++} level is expected to be close to the conduction band edge [18]. For the centre to have this negative-U behaviour, it is necessary for the lattice to relax, by the movement of adjacent metal ions, when the centre is ionised, and this results in a potential barrier between the ionised and neutral states, which must be overcome for the centre to relax back to its neutral state when the illumination is switched off [62]. This is consistent with the thermally activated relaxation process, shown in Fig. 9.23a, where the measured activation energy is of the same order as calculations of the thermal barrier height [62]. The effects described above are summarised in the illustrative band diagram in Fig. 9.23b [61] of the TFT under NBIS. This shows the upward bending of the bands at the surface, and the localised presence of the V_0^{++} centres, whilst, at the back of the film, the bands are bent downwards to accommodate the photo-generated electrons, and, in this region, the oxygen vacancy is occupied by electrons and is neutral. The band bending will separate the photo-generated holes and electrons, with the field sweeping the holes to the front surface of the film, where they are trapped in the gate dielectric or in interface states.

Although the role of the oxygen vacancy has been widely invoked in the NBIS instability mechanism, there are also results linking the instability to inadequate passivation of the back surface of the film, and AlO_x [68] and Y_2O_3 [69] passivated structures have been shown to have much better stability than unpassivated ones. From the a-IGZO film thickness dependence of the instability, it was also shown that the photo-ionisable defects in the lower half of the band-gap, which underlie the instability in the unpassivated films, were generated on the top (exposed) surface of the film [69]. The greater instability in the unpassivated films has been attributed to the introduction of water molecules or the desorption of O^- ions [68], or possibly due to proton movement from absorbed hydrogen [69].

Whilst improved control of the NBIS instability has been demonstrated, the precise mechanism, as the above review indicates, is still open to debate, and it continues to be the subject of widespread research.

9.4.3.3 Stability Considerations for Active Matrix Addressing TFTs

For active matrix applications, the addressing TFT will experience an alternating combination of positive and negative gate biases, and, in assessing the long-term lifetime of the TFT, it is useful to determine whether this pulsed AC stress produces the same instability as the DC stress discussed above. Figure 9.24 compares the effect of DC stress with both single polarity and bipolarity pulsed bias stress (in an inverted staggered a-IGZO TFT passivated with an SiO_x layer) [70]. In these particular devices, the threshold voltage shifts were comparable for both negative and positive bias DC stresses, but they were reduced almost to zero for pulsed negative bias stress, and halved for pulsed positive bias stress. These pulsed results were for a 50 % duty cycle with a 5 ms pulse width. For this duty cycle, the negative pulse bias results were independent of the absolute pulse width (with ΔV_T

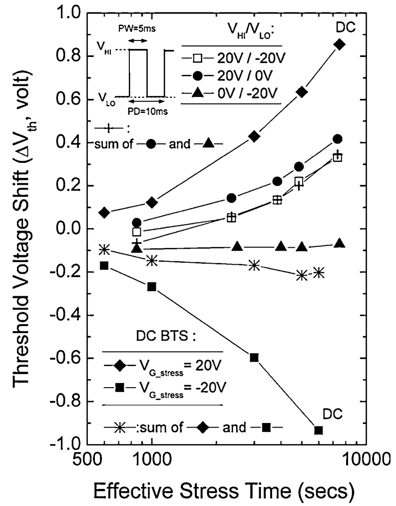


Fig. 9.24 Comparison of the threshold voltage shifts after pulsed bias and DC bias stress of a-IGZO TFTs. (Reprinted from [70] with permission of SID)

remaining close to zero), whilst, for positive pulse bias, ΔV_T increased with increasing pulse width, and tended towards the DC values. The small ΔV_T noted with the negative pulse bias stress was attributed to the slow hole accumulation processes within the material, and the consequent reduction in hole trapping at the surface compared with the DC results [70]. Due to the minimal effect of the negative pulse stressing, the bipolar pulse stressing in Fig. 9.24 (open square symbols) was almost entirely dominated by the positive pulse bias results, and were well approximated by the summation of the negative and positive pulse bias results. In contrast, the summation of the DC results did not predict the effect of bipolar pulse stressing. This investigation did not include negative pulsed bias stress under illumination, which, for DC stressing, produces a much larger ΔV_T. However, this effect has been examined, in a-HfInZnO TFTs [71], as a function of duty cycle and frequency, with a square wave pulse oscillating between +20 V and −20 V. In agreement with the dark, negative pulse bias results of Fig. 9.24, the negative threshold voltage shift with illumination was suppressed for duty cycles greater than ~1 % (positive bias), and the net shift was determined almost entirely by the positive bias stress cycle. Hence, these results indicate that, under pulsed operation conditions, the NBIS instability may be considerably less than observed with DC measurements.

Notwithstanding the above comments, all instability processes should be reduced as much as possible for TFTs used in commercial applications. The interaction of processing procedures and instability effects were discussed in Sect. 9.4.3.1, and improved stability can be achieved by post-deposition annealing of the a-IGZO, the use of a high quality gate dielectric, and effective passivation of the back surface to prevent moisture and oxygen ingress into the TFT. The sequential layer depositions must also be carried out in a way which minimises

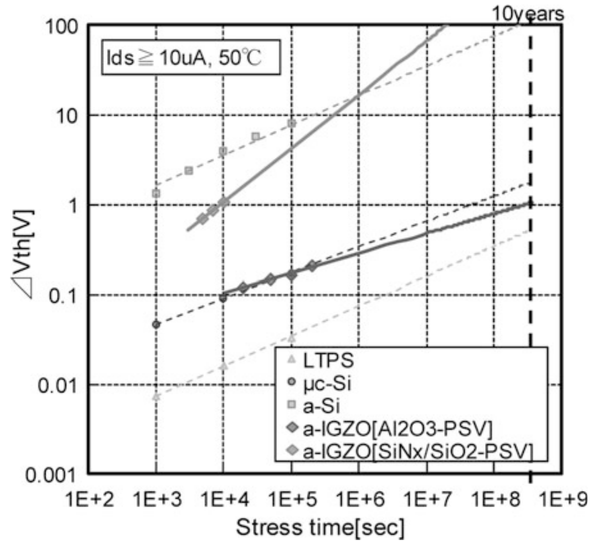


Fig. 9.25 Constant current stress instability of Al_2O_3 and SiO_x/SiN_x passivated a-IGZO TFTs compared with a-Si:H, poly-Si, and micro-crystalline Si TFTs. (Reprinted from [73] with permission of SID)

damage to the underlying films, whilst also being consistent with large area, high-throughput manufacturing. As indicated in Sect. 9.1, there are many examples of demonstrator displays being fabricated with a-IGZO addressing TFTs [2–4, 6, 13], several of which report high stability devices. One example of this [72, 73] was an inverted staggered etch-stop TFT, employing a dual layer gate dielectric of PECVD SiN_x and SiO_x (with the latter uppermost and adjacent to the DC-sputtered a-IGZO), an SiO_x etch-stop layer, Mo source/drain contacts covering the a-IGZO island edges, and a final passivation layer of DC-sputtered Al_2O_3. From positive gate bias stress measurements at 50 °C, an operating life of 10 years was predicted with an extrapolated threshold voltage shift of <1 V. In addition, after 10^4s NBIS at -20 V, using a white light source emitting in the range 380−720 nm, the threshold voltage shift was only −0.2 V, and this was attributed to excellent back-face passivation by the DC-sputtered Al_2O_3 film [72]. With the above measures, the long-term stability of these passivated a-IGZO TFTs for AMOLED displays is expected to exceed that of a-Si:H TFTs, be comparable to micro-crystalline Si, and to approach poly-Si, as shown by the constant current stress data in Fig. 9.25 [73].

9.5 AOS TFT Circuits

In view of the use of AOS material for the pixel driving TFT in demonstrator FPDs, there is widespread interest in exploiting the high carrier mobility to integrate driver circuits into these displays. From considerations of power consumption in digital logic circuits, it is preferable to use a complementary (p- and n-channel) device

technology. As discussed in Sect. 9.2, the AOS materials, including a-IGZO, used for the high electron mobility devices, have a large density of states in the lower half of the band-gap, giving very poor p-channel behaviour [12]. However, by careful choice of the constituent materials, good p-channel TFT operation has been achieved in SnO, due to the valence band edge being made up of spatially spread s-orbitals from the Sn^{2+} ion [74]. The hole mobility was 1.3 cm^2/Vs, but the n-channel TFTs in this material had a field effect mobility of only 1.5×10^{-4} cm^2/Vs [75]. Hence, as yet, there is not a monolithic AOS technology capable of delivering well-matched complementary pairs of TFTs in the same material, and most of the activity in this area has focussed on circuit implementation using the single channel n-type a-IGZO TFTs.

Given these limitations, alternative inverter circuit architectures (compared with the conventional two complementary TFTs) have been investigated to obtain good voltage switching, ideally with low power consumption. One option is to use a depletion device as the load TFT, and this has been engineered by using a double-gated load TFT to give a more negative threshold voltage than the drive TFT [76]. This gave a large output voltage swing, but power consumption was high. An alternative approach used a cross-coupled inverter design, containing six TFTs, to achieve a high output voltage swing, and ~ 70 % lower power consumption than a conventional 2-stage, single channel inverter [77]. In addition to these specific circuit studies, a range of driver circuits have already been integrated into a-IGZO demonstrator displays, including row driver circuits [78, 79] for AMOLEDs, row and column drivers for an LCD [23], as well as an LCD driver circuit [80] incorporating a common electrode inversion circuit to reduce the overall power consumption (compared with the more common dot inversion technique [81]). (AMLCD drive inversion schemes are briefly reviewed in Sect. 4.3).

9.6 Summary

Transparent amorphous oxide semiconductor materials, and in particular a-InGaZnO (a-IGZO), are attracting increasing attention as an alternative TFT material to a-Si:H and poly-Si, especially for large sized AMOLED displays. This is because the material has an electron mobility ~ 10 times higher than a-Si:H, and is, therefore, more easily able to deliver the larger drive currents needed for OLEDs. Although the mobility is still an order less than poly-Si, it may have better uniformity by being an amorphous material, and promises a simpler processing schedule. However, the current TFTs are only n-channel, and integrated logic circuits made in this material will be slower and consume more power than the complementary pair circuits available with poly-Si TFTs. Nevertheless, there are now examples of driver circuits integrated into a-IGZO demonstration displays, and attention is being given to the design of low power, single channel circuits.

The high electron mobility in this amorphous material is a consequence of its ionic bonding structure, which also delivers a low density of trapping states near the

conduction band edge. Hence, the TFTs have a sharper turn-on than a-Si:H TFTs, and state-of-the-art devices also display better gate bias stability, which is another important issue for the AMOLED application. However, there still are stability issues with AOS TFTS, especially with negative bias stress under illumination conditions. This instability has been associated with photo-ionisation of the oxygen vacancy, and this is an on-going research topic. From an application point of view, the instability is reduced under pulsed bias conditions, and good passivation of the device has been demonstrated to significantly diminish the effect.

Due to the low DOS, the Fermi level can be moved into the conduction band, where the conduction process in a-IGZO is controlled by percolation. This results in a carrier density dependent mobility, which has to be taken into account when measuring the DOS. In particular, the conventional iterative fit of a device model to the transfer characteristics will over-estimate the DOS if the on-state field-effect mobility is simply used. To avoid these problems, C-V techniques have been established for the DOS measurement, and, by using these DOS values, the carrier-dependent mobility can be extracted from the transfer characteristics.

The device structure is typically either inverted staggered etch-stop or inverted coplanar, which can be made with a 5 or 4 mask process, respectively. In principle, this is a low temperature process, including the deposition of a-IGZO by DC sputtering at room temperature, although post-deposition anneals are required to stabilise the material. Nevertheless, the potential for low temperature processing also makes it attractive for flexible substrate applications. Many current devices are fabricated with metal source and drain contacts directly on the a-IGZO, and attention is being directed towards series resistance issues, with some processing schedules incorporating a metal sinter stage to reduce the contact resistance between the metal and the semiconductor. Device performance is sensitive to ambient oxygen and water, and effective passivation of the structure is essential for the fabrication of high quality TFTs with stable long-term operation.

In summary, AOS TFTs are commanding widespread application interest, with numerous demonstrations of a-IGZO addressed displays. This is supported by a substantial research activity into the details of device behaviour, and further improvements in device physics and TFT performance can be anticipated. In addition, commercial applications to AMOLED displays, and to large, high resolution AMLCDs have been forecast.

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Chapter 10
Organic TFTs

Abstract A large number of organic TFT materials now display carrier mobility values approaching, or exceeding, those of a-Si:H, and this has stimulated considerable interest in using them for low cost, flexible substrate applications, such as RFID tags, and e-reader displays. This chapter reviews work in this field, and starts by introducing some of the key organic chemistry concepts, which underpin the semiconducting behaviour of these materials. Other topics include molecular ordering, carrier transport, TFT architecture, and the deposition of both semiconductor and dielectric materials, together with their properties. These are linked to device behaviour, with a focus on the key material and design issues, which currently limit TFT performance, such as metal/organic contacts, and ambient and bias stability effects.

10.1 Introduction

The commercial interest in organic TFTs, OTFTs, for display applications started in the early-1990s, when the carrier mobility in small molecule material, particularly pentacene, exceeded 0.1 cm^2/Vs, and began to approach the values of 0.5–1.0 cm^2/Vs obtained in a-Si:H. Since that time, the performance of organic materials has continued to improve, and, when viewed on a 20 year timescale, increases in carrier mobility of several orders of magnitude have been achieved, with the highest values now in excess of 10 cm^2/Vs, as shown in Fig. 10.1 [1]. Four classes of material are labelled in this diagram, but these include sub-divisions of the two main families, which are small molecule (sometimes referred to as oligomer) and long molecule (normally referred to as polymer) conjugated semiconductors. The further sub-division is amongst the small molecule types, where they are specified as vacuum deposited, solution processed and single crystal. (The interest in single crystal organic semiconductors has largely been to

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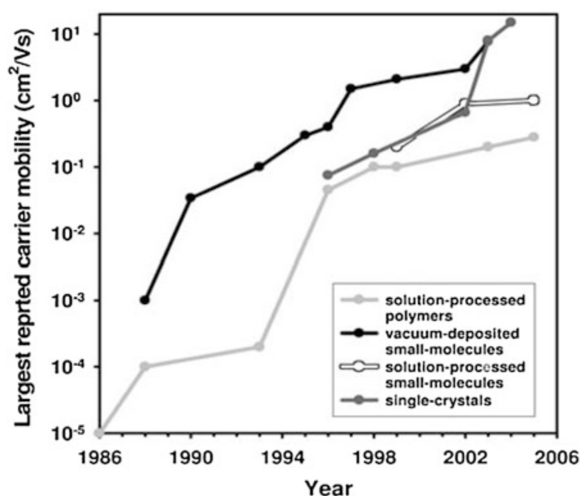


Fig. 10.1 Changes in carrier mobility in organic TFTs between 1986 and 2006. (Reproduced from [1] with permission of John Wiley & Sons, Inc)

identify ultimate performance limits. This type of material has been recently reviewed [2], and will not be discussed further here). The polymer samples are usually solution processed, which means that their deposition is from a liquid phase by printing, casting or spin-coating. This is expected to be the most cost-effective approach to film formation, and underlies the interest in polymers in spite of their lower mobility, as seen in Fig. 10.1.

Although the attainment of a useful mobility is essential for the currently envisaged commercial applications, the mobility alone is not sufficient for organic materials to be seen as potential replacements for a-Si:H. Indeed, there is no likelihood of them challenging the mainstream technology of a-Si:H TFTs on glass in the near future. Rather, the interest in them lies in their compatibility with a flexible substrate technology, using inexpensive polymer substrates, in order to produce light-weight, portable displays, which can be contoured, folded or rolled. Commonly used plastic substrates in this work are polyethylene naphthalate (PEN), and polyethylene terephthalate (PET), which, in their heat stabilised forms, have maximum handling temperatures of 200 °C and 150 °C, respectively. Further properties of these, and other polymer substrates, are shown in Table 11.1. In addition, the challenges in using flexible substrates are discussed in Sect. 11.2, in which it is shown that the issues of maximum processing temperature, the mismatch in coefficients of thermal expansion between the substrate and the layers on them, and general substrate flexing are more acute with the inorganic TFT technologies. Thus, these topics are expected to be more easily manageable with a TFT technology which uses the less rigid, and better physically matched, organic TFT materials. For example, suitably capped OTFT samples, which placed the TFTs in the neutral strain plane, have been reported with a minimum bending radius of 0.5 mm [3], and working displays have been demonstrated with a bending radius of 4 mm [4], as shown in Fig. 10.2.

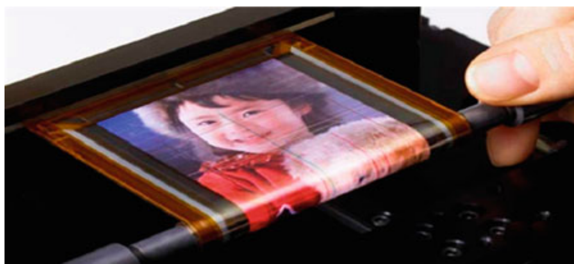


Fig. 10.2 Photograph of a flexible AMOLED display, driven by OTFTs, rolled around a 4 mm radius cylinder. (Reprinted from [4] with permission of SID)

There are now plentiful examples of OTFT research demonstrator displays on flexible substrates, using LCD [5], electro-phoretic, EPD [6–8], and OLED [4, 9, 10] media, as well as demonstration logic circuits [11–13]. The most obvious first application of OTFTs is in low cost RFID tags, and in AMEPDs (due to the reduced pixel drive current requirements). Some e-reader proto-products have been presented [6, 8], in which the ultimate aim is a compact device containing a rollable/foldable screen [8], and the first product, a rigid-framed e-reader for educational use, was announced in late 2011 [14].

In common with other TFT technologies, a mature technology should deliver not merely basic device performance, with an acceptable carrier mobility, leakage current and threshold voltage, but also good device uniformity and reliability. These properties should be delivered in a cost-effective, reproducible process, and offer the prospect of increased device/function integration. Of all the TFT technologies, the OTFT technology is currently the most immature in these respects, with no clear consensus on the preferred organic material, gate dielectric and process flow, but it is driven by the prospect of a low-cost, flexible substrate technology, with laboratory demonstrators and the first product highlighting the potential of this approach.

In another important respect, the activity covered in this chapter is different from the preceding TFT chapters, in that they dealt with just one semiconductor material for the TFT channel. In contrast, the research programmes into OTFTs have investigated an extensive range of different organic materials, both for the TFT channel, and, to a lesser extent, for the gate dielectric and contact metals. Moreover, continued development of new and improved molecular structures is an on-going activity, and recent reviews [15–17] have given a detailed overview of the range of materials examined. Similar specialist coverage of different materials is less appropriate for this book. Instead, the following sections of this chapter will focus on the broader background concepts and issues in using organic materials to fabricate TFTs, and with examples drawn from the polymer and oligomer materials of current interest.

Sections 10.2.1 and 10.2.2 are an elementary introduction to some of the background organic chemistry concepts routinely employed in the study of organic materials for TFTs, and cover the role of the molecular and orbital structure of the material in determining its semiconductor behaviour. Section 10.2.3 reviews the role of structural organisation in optimising TFT performance, including the

growth of ordered domains and poly-crystalline regions. Organic semiconductors are usually prepared undoped, and n- and p-channel behaviour is partially determined by the particular metal used for the contacts, and, specifically, by the alignment of the metal work function and the carrier bands in the semiconductor. Metal/organic contacts have been widely studied, and an overview of the key issues for TFTs is presented in Sect. 10.2.4. Finally, Sect. 10.2.5 reviews the current understanding of the carrier transport mechanisms in these materials.

Section 10.3 discusses the architecture of OTFTs, and Sect. 10.4 deals with the materials and processing procedures used in TFT fabrication. The materials coverage includes sub-sections on the semiconductors, the gate dielectrics and the metallisation options. There is also a sub-section on novel processing schemes, which exploit the self-organising properties of these materials. These techniques differ radically from the more conventional TFT fabrication process of layer-by-layer definition by photo-lithography and etching.

The electrical characteristics of OTFTs are discussed in Sect. 10.5, with an overview of the performance parameters from a range of common semiconductors, but with a more detailed focus on contact and series resistance effects, which play a major role in determining overall TFT behaviour. Finally, the ambient and bias stability issues of OTFTs are reviewed in Sect. 10.6.

10.2 Background and Materials

10.2.1 Conjugated Molecular Systems

The materials used in OTFTs are conjugated molecular systems, which means that they have alternating single and double carbon–carbon bonds, and their molecular π-bonding orbitals are responsible for the ability of the material to transport charge. A simple example of a conjugated molecule is the benzene ring shown in Fig. 10.3a [18], which is a building block for a number of important OTFT compounds. The figure shows the chemical structure of benzene, C_6H_6, which is a planar ring with the alternating double bonds between the carbon atoms. Also shown are the two commonly employed symbols, which are used to represent the benzene ring in more complex molecules, such as those shown in Fig. 10.3b, c. Figure 10.3b is an acene structure, which consists of a number of linearly fused benzene rings, giving a rod-like molecular structure, and the subscript n, in the diagram, refers to the number of repeating units of the bracketed ring structure. A specific example of this structure is the pentacene molecule, consists of five rings, as shown in Fig. 10.3c, and this is the most widely studied small molecule material, yielding high mobility p-channel TFTs.

A similar planar ring structure molecule is thiophene, C_4H_4S, which is shown in Fig. 10.3d, together with its symbolic representation. Thiophene is a building block of another group of OTFT materials, consisting of both small molecule

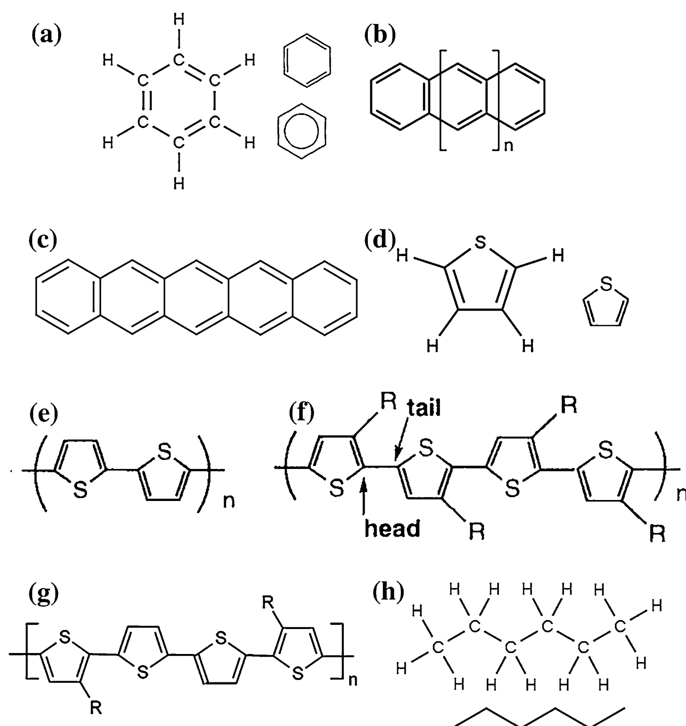


Fig. 10.3 Chemical structure of **a** benzene ring, and its symbolic representations, **b** acene molecule, **c** pentacene, **d** thiophene, and its symbolic representation, **e** polythiophene, **f** regio-regular poly(3-hexylthiophene), P3HT, **g** poly(3,3″ dialkylquaterthiophene), PQT-12, and **h** hexane linear chain molecule, and its symbolic representation. (**f** Reproduced from [22] with permission of John Wiley & Sons, Inc, and **g** Reprinted with permission from [21]. Copyright (2004) American Chemical Society)

oligothiophenes [19], as well as the polymers polythiopene and its derivatives poly(3-hexylthiophene), P3HT [20], and poly(3,3‴ dialkylquaterthiophene), PQT-12 [21], shown in Fig. 10.3e–g, respectively. The substituted side chains, R, on the basic thiophene molecule are alkyls, C_nH_{2n+1}, which are radicals of the alkane group, C_nH_{2n+2}.These are single-bond chains of carbon and hydrogen, and the six carbon molecule, hexane, C_6H_{14}, is illustrated in Fig. 10.3h. (This figure also shows its conventional symbolic representation, although a simple straight line, plus the symbol R, is also widely used for this and other substituents, as in Fig. 10.3f, g). For solution processing of the polymers, alkanes with six or more carbon atoms are favoured for the substituting alkyl groups on polythiophene [21, 22], as seen by the use of hexyl, C_6H_{13}, in P3HT, and dodecyl, $C_{12}H_{25}$, in PQT-12.

The long-range organisation of the molecular structures is essential to give good TFT performance, and this is discussed in Sect. 10.2.3.

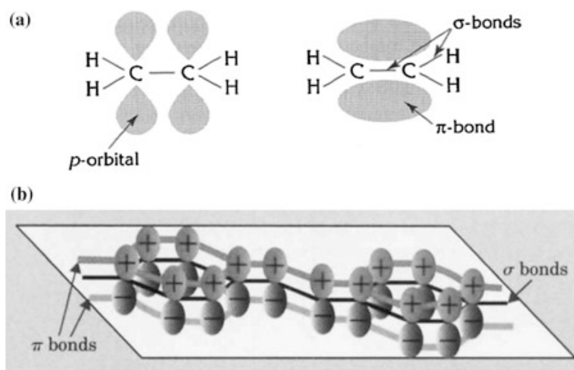


Fig. 10.4 **a** pi molecular orbital formation in an ethene molecule (Reproduced by permission of Hodder Education from [18], copyright (2003)), and **b** schematic illustration of the extended pi-orbitals in a conjugated molecular system (Reprinted with permission from [23]. Copyright (2005) American Institute of Physics)

10.2.2 Molecular Bonding

The isolated carbon atom has two electrons in the 2s orbital and two distributed in the three 2p orbitals, and, when carbon atoms are brought together to form a molecule containing a *double bond*, these four atomic orbitals are converted into three hybrid sp^2 orbitals, leaving one remaining 2p orbital. The three hybrid sp^2 orbitals form covalent bonds with the adjacent atoms, defined by the molecular σ bonding-orbital in the plane of the atoms, and with the 2p atomic orbitals perpendicular to this plane. The overlapping 2p-orbitals, on adjacent atoms in the molecule, form a molecular π-orbital [18], as shown for the simple double bond molecule, ethene, C_2H_4, in Fig. 10.4a. The π-orbital only forms where there is a σ-orbital, and double bonds are composed of σ and π orbitals. For a conjugated molecule, the π-orbital delocalises its electrons within the molecule, or along a conjugated polymer backbone, as shown schematically in Fig. 10.4b [23]. Hence, the π-orbitals support the flow of charge carriers within the material, and, in a solid, the filled π-bonding orbitals form the highest occupied molecular orbital, HOMO, and the empty π-anti-bonding orbitals form the lowest unoccupied molecular orbital, LUMO [23]. These can be thought of as corresponding to the valence and conduction bands in conventional inorganic semiconductors, and are used in the same way to represent the band off-sets between the different constituents of a TFT structure [24].

10.2.3 Molecular Organisation

It has been widely demonstrated that there needs to be a high degree of structural order within the material, together with strong electronic coupling between adjacent molecules, to achieve effective charge transport and high performance TFTs. Hence, as discussed below, the favoured materials show regions of, at least, micro-crystallinity if not poly-crystallinity, in contrast with less favoured, low

mobility amorphous materials [28]. Whilst this structural distinction is widely observed, it would appear not to be universal, as high performance n-channel TFTs have been reported in amorphous material [25]. Although there is a strong theoretical framework underpinning molecular engineering and materials development [26], it is apparent that a full understanding of the correlation between material structure and device performance has not yet been achieved [2]. In the remainder of this section, examples are given of the structural order engineered into both oligomer and polymer materials.

High performance P3HT OTFTs [27, 28] have been achieved with regio-regular molecules, in which there is predominantly head-tail, HT, coupling of the adjacent thiophene rings (at the 2 and 5 positions), with the hexyl substituent, R, in the number 3 position on the ring [22]. This is illustrated in Fig. 10.3f. The HT coupling produces molecules with a torsional twist of $<10°$, indicating good co-planarity, which is required for efficient π-orbital coupling between adjacent molecules. Alternative couplings, such as head-head (the 2, 2 positions), can lead to severe twisting of the molecule by up to 40°, and degraded π-orbital conduction [22]. Detailed discussion of the chemical synthesis of thiophene polymers can be found in Ref. [22], but the topic itself is beyond the scope of this book.

The regio-regular P3HT molecules, with a high HT content, self-organise into micro-crystalline domains containing close packed lamellae, which are vertically aligned to the substrate surface, as shown in Fig. 10.5a [28]. In contrast, in films with a low concentration of HT coupling, the lamellae are oriented parallel to the substrate surface. When these structures were used in OTFTs, the field effect mobility was up to 10^3 times higher in the high HT-content films, as illustrated, in Fig. 10.5b, by the dependence of the field effect mobility on the percentage of HT coupling [27]. This work also demonstrated the large anisotropy in mobility within these films, with the most effective carrier transport being by inter-chain, π–π coupling in these π-stacked materials. Hence, not only is molecular ordering within the film important, but as significant is the orientation of the molecular stacking with respect to the direction of channel current flow. It has also been demonstrated that the formation of vertically aligned molecules can be enhanced by the prior deposition of self-assembled mono-layers, SAMs, onto the substrate surface [29]. As will be seen in Sect. 10.4, the use of SAMs is a widely employed technique for controlling the orientation of organic semiconductor molecules, and can be regarded as comparable to the use of alignment layers in LCD cells to control the alignment of the LC molecules [30].

Another thiophene based molecule, regio-regular PQT-12 (see Fig. 10.3g), has also been demonstrated to self-assemble in an ordered vertical lamellar structure, which is similar to the P3HT discussed above. The stacking is shown schematically in Fig. 10.5c [21], and, for TFT samples, the gate oxide surface was coated with a film of octyltrichlorosilane, OTS, before spin coating with the polymer. X-ray diffraction of the as-spun films showed a loosely packed lamellar structure, but, after annealing at 135 °C, a more highly ordered lamellar stack was observed, oriented perpendicular to the substrate surface. TEM examination of these films showed an inter-stack spacing of 3.7 Å [21]. The hole mobility was 0.14 cm^2/Vs,

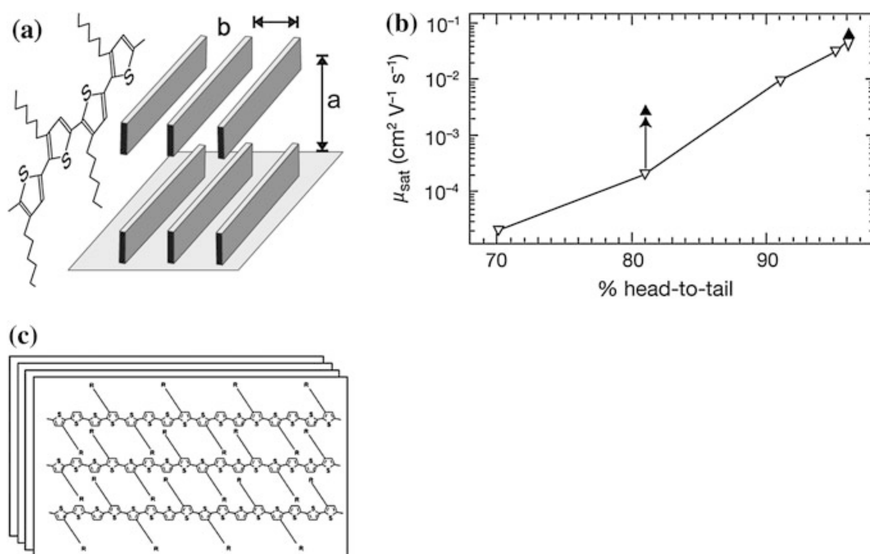


Fig. 10.5 **a** Lamellar molecular ordering of regio-regular P3HT (Reproduced from [28] with permission of John Wiley & Sons, Inc). **b** variation of hole mobility with fractional head–tail coupling in P3HT (Reprinted by permission from Macmillan Publishers Ltd: Nature [27], copyright (1999)), and **c** lamellar molecular ordering of PQT-12 (Reprinted with permission from [21]. Copyright (2004) American Chemical Society)

which is comparable to well ordered P3HT films, but the PQT-12 samples showed much less hysteresis during measurements, and much better long-term ambient stability. This was attributed to the larger ionisation potential of PQT-12, which reduced its susceptibility to oxidation. Device performance issues are discussed in greater detail in Sects. 10.4, 10.5 and 10.6.

The most widely studied small molecule material is pentacene [26], which, under well controlled vacuum evaporation conditions, forms a polycrystalline film on the substrate surface. The grain structure is triclinic, with the (001) plane parallel to the substrate surface [15], and the molecular alignment follows an edge-to-face (‘herringbone’), intermolecular stacking pattern. This is one of the characteristic structures for acenes [26], and is shown in Fig. 10.6 [31]. Figure 10.6a shows that the rigid pentacene molecules are arranged in vertically stacked layers, with a pitch of ~15.4 Å, and, within each layer, the molecules are at an angle of ~84 ± 0.5° to the substrate surface, depending upon the termination of the surface [32]. The inter-molecular ‘herringbone’ pattern, within each layer, is more clearly seen in the image in Fig. 10.6b, which is viewed parallel to the long-axis of the molecule. Given the near vertical alignment of the molecules on the substrate surface, the structure is often schematically illustrated in TFT cross-sections, as shown by Fig. 10.6c. Although single crystal pentacene has been studied, the material is usually poly-crystalline in its thin film form, and an example of the role of grain size on carrier mobility is shown in Fig. 10.6d [33].

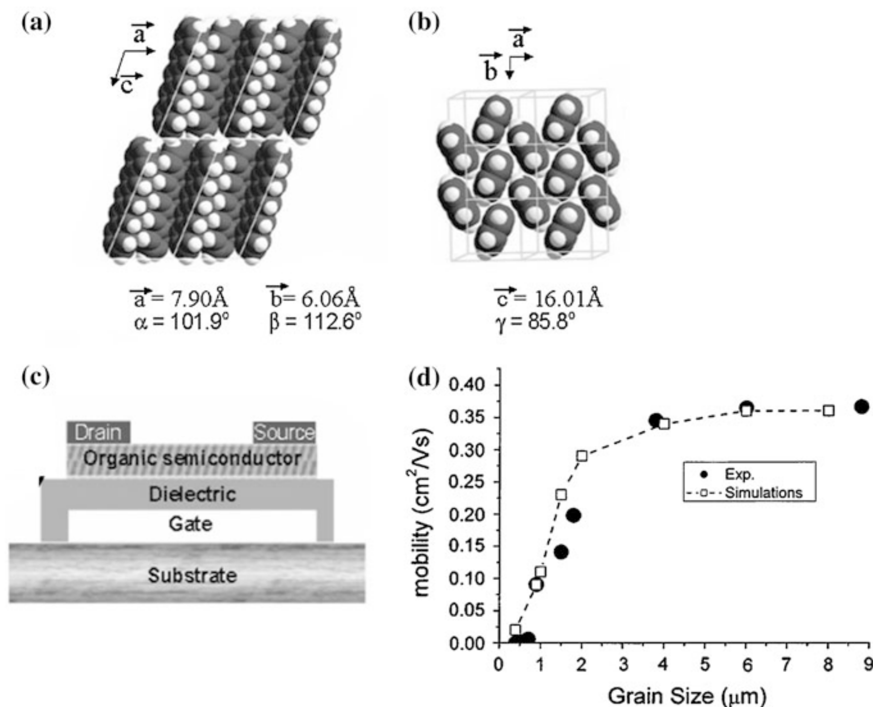


Fig. 10.6 Crystalline structure of pentacene, viewed **a** along, and **b** perpendicular to the plane of the substrate surface. **c** Schematic TFT representation showing the vertically stacked planes of near-vertically aligned molecules (Reprinted with permission from [31]. Copyright (2003) by the American Physical Society), and **d** variation of field effect mobility with pentacene grain size, where the *dashed line* is from a 2-D device model with grain-boundary trapping. (Reprinted with permission from [33]. Copyright (2005) American Institute of Physics)

In his work, the grain size was controlled by varying the pentacene evaporation rate, and was assessed by atomic force microscopy. The TFT geometry was inverted staggered with an SiO_2 gate dielectric layer, and the hole field effect mobility was found to increase with increasing grain size (up to a maximum value of 0.35 cm^2/Vs). The influence of grain size was attributed to grain boundary trapping effects, as shown by the GB modelling of the data [33]. As with the polythiophenes, the carrier transport process in pentacene films is also essentially two-dimensional, by virtue of the better electronic coupling between molecules within a layer, rather than between layers [34].

10.2.4 Metal/Organic Contacts

The organic channel materials are undoped, and the distinction between n-channel and p-channel devices is determined by which carrier is injected from the source

contact. In other words, if the work function of the source metal is close to the LUMO level, electrons will be more easily injected (giving n-channel operation), and, conversely, if it is closer to the HOMO level, holes will be preferentially injected, giving p-channel behaviour. Hence, a key consideration in matching the metal to the organic semiconductor, to achieve n- or p-channel operation, is the relative displacement of the metal work function from the HOMO or the LUMO levels. However, it should be noted that whilst a good injecting contact is necessary for both p- and n-channel device operation, it alone is not sufficient to produce high performance, stable devices, where impurities and carrier trapping will be additional determinants of device behaviour [35]. Indeed, the fabrication of high quality n-channel devices has proven to be more difficult to achieve than for p-channel devices [25, 35], particularly due to electron trapping effects when SiO_2 was used as the gate dielectric [36]. Because of this, well matched complementary p- and n-channel TFTs, for low-power digital circuits, have not been available until relatively recently [25, 37]. The issues with the development of high performance n-channel TFTs are discussed further in Sect. 10.4.3.

In view of the importance of the metal/organic semiconductor contact, it has been extensively studied [24, 38–40]. The HOMO/LUMO energy band representation of the material is particularly useful in considering the contact, as illustrated in Fig. 10.7a, b [39]. Figure 10.7a shows the simple alignment of the metal and the semiconductor vacuum levels in the Schottky-Mott limit. The hole injection barrier, ϕ_h, is then given by the difference between the metal work function, Φ_M, and the semiconductor ionisation energy, IE, and the electron injection barrier, ϕ_e, by the difference between Φ_M and the electron affinity, EA. With knowledge of these values, an appropriate choice of metal may, in principle, be made. Unfortunately, practical systems rarely accord with this simple diagram, irrespective of whether the materials are prepared in UHV [39], or under more realistic conditions, such as air exposure of the metal prior to the deposition of the organic material [24, 38]. Usually, a dipole barrier, Δ, is found at the metal/organic, MO, interface, as shown in Fig. 10.7b, and this may be either positive or negative, resulting in an offset of the work function from the location predicted by the direct alignment of the vacuum levels. In the example shown, the effect of the dipole barrier is to change the metal from a hole injector to an electron injector. Moreover, the metal work function itself is sensitive to its environment, and care is needed in using the text book values. For example, gold is widely used as a contact metal in OTFTs, and its work function is conventionally quoted as $\sim$5.1–5.2 eV [41], and this value is confirmed in the UHV cited work here [39]. However, exposing a gold film to air, or rinsing it in an organic solvent, produced a dipole barrier of 0.7 eV, giving an effective Au work function (the energy gap between the gold Fermi level and the polymer vacuum level) of $\sim$4.5 eV, whereas ozone exposure increased it back to 5.2–5.5 eV [24]. The effective work function of $\sim$4.5 eV was also found following both the deposition of several different π-conjugated polymers onto gold, and UHV gold deposition onto pre-deposited films of the same polymers [24]. The dipole barrier found in this work, of

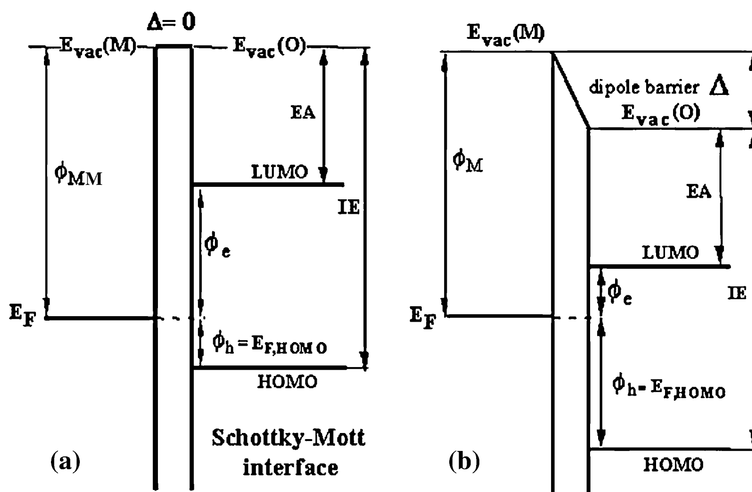


Fig. 10.7 HOMO and LUMO band diagram of an organic semiconductor showing the band offset with respect to a metal contact **a** in the Schottky–Mott limit, and **b** with the formation of a surface dipole layer. (Reproduced from [39] with permission of John Wiley & Sons, Inc)

~0.7 eV, is well established [38], although values as high as 1.08 eV have been quoted for the UHV deposition of pentacene onto gold [39].

The work function, ionisation energy and dipole barrier values quoted above were derived from ultraviolet photoelectron spectroscopy, UPS, measurements [24, 38, 39]. Most metals have been found to have a non-zero dipole barrier when in contact with organic materials, where the values recorded may be a function of the preparation and handling of the material [24]. Hence, the band diagram shown in Fig. 10.7b is the more appropriate representation of the contact than Fig. 10.7a.

Several models have been invoked to explain the dipole barriers [24, 38–40], including Fermi level pinning at interface states, charge exchange between the materials, and molecular mixing effects. The gold results, cited above, were explained by a more fundamental 'push-back' effect [24], in which the electron density from a clean metal surface decreases exponentially for a few angstroms beyond the surface, and charge neutrality is maintained by the corresponding deficit of negative charge within the material close to the surface. The electron tail produces a surface dipole, and a corresponding dipole potential energy, with which the work function scales. The larger the dipole potential energy (and the work function), the more polarisable the surface is, and the greater the effect of physisorbed layers pushing the electron tail back, and reducing the surface dipole (and the associated work function). Thus, metals like gold, with a large work function, are more sensitive to adsorbed films than low work function metals like Ca [24].

10.2.5 Carrier Transport

Carrier transport in OTFTs, as measured by the field effect mobility, is a function of several parameters [34]. The intrinsic factors include the molecular structure of the material, its ordering to promote good inter-molecular π–π coupling, and the molecular alignment on the substrate surface so that the high conduction direction is parallel to the plane of the TFT channel. The extrinsic factors include some or all of the following: the sample temperature, the lateral electric field, the free carrier density, and the carrier injection efficiency of the source and drain contact materials. The precise details of the charge transfer process, and the resultant mobility values, are still the subject of on-going theoretical study [34, 42]. However, the experimentally measured field effect mobility values are usually described as being limited by an inter-trap hopping process, in highly disordered material [43], or by multiple trapping and release, MTR, from localised defect states, in more ordered material [34, 42] (a process which was discussed in detail in Sect. 6.2.4), or by trapping effects at grain boundaries [33].

Hopping and MTR are thermally activated processes, and the field effect mobility, μ_{FE}, can be described by the generic equation:

$$\mu_{FE} = \mu_0 A \exp -(E_A/kT) \tag{10.1}$$

where μ_0 is the trap-free mobility for hopping, and, for MTR, it is the band mobility, with A proportional to the fractional division of carriers between those in traps and those in the band. As seen for inorganic semiconductors, such as a-Si:H and IGZO (Chaps. 6 and 9, respectively), the increase in trap filling with increasing gate bias leads to a greater relative increase in the free carrier density, and, thereby, increases the field effect mobility. The same has been observed with organic materials, whereby the mobility frequently displays a dependence on the carrier density, and, hence, on the gate bias above threshold. This has been empirically characterised as [44]:

$$\mu(V_G) = \mu_0 \left(\frac{V_G - V_T}{V_{AA}} \right)^{\gamma} \tag{10.2}$$

where the mobility enhancement factor, γ (>0), and V_{AA} were extracted from data fits. A similar power dependence on gate bias has also been theoretically demonstrated for both the MTR model and for hopping in more disordered materials [45]. The influence of this gate-bias-dependent mobility on the TFT current-voltage equations is discussed further in Sect. 10.5.1.

In addition, under lateral fields greater than $\sim 10^4$ V/cm, the mobility may be enhanced by the lateral field, and is attributed to emission barrier height lowering by the Poole-Frenkel effect [34, 46]:

$$\mu(F) \propto \mu_{F0}(T) \exp \beta(T) \sqrt{F} \tag{10.3}$$

where F is the lateral electric field, μ_{F0} is the zero field mobility, and the parameter β is proportional to 1/T. The mechanism of field enhancement is also temperature dependent, and, at cryogenic temperatures, it has been found to change from the thermally activated Poole-Frenkel process to a temperature-independent field emission process [46].

Some, or all, of these effects are seen in many OTFTs. For instance, Eq. 10.1 describes an increase in mobility with increasing temperature, which has been widely reported. Reference [42], for example, reviewed and confirmed this behaviour in more than a dozen oligomer and polymer materials, including both p- and n-channel TFTs, with room temperature carrier mobilities ranging from 0.02 to 0.42 cm^2/Vs. The thermal activation energy, E_A, showed an inverse correlation with the measured mobility, and was 20–30 meV and 40–70 meV for the higher and lower mobility devices, respectively [42]. When using the E_A values to extract μ_0, the μ_0 values were found to be quite similar, within the range 0.2–0.8 cm^2/Vs, and much closer than the wider spread in measured μ_{FE} values, which supported the MTR model of conduction. This thermal excitation of carriers from trapping states is a typical feature of most OTFTs, and distinguishes them from single crystal organic devices. For example, the mobility in crystalline rubrene TFTs had the opposite temperature dependence, and was found to decrease from $\sim$30 to 20 cm^2/Vs as the temperature was increased from 150 K to 300 K, due to increased phonon scattering [47].

In contrast to the widely observed thermal activation of the mobility in OTFTs, its lateral electric field enhancement appears to be less frequently reported, and this is most likely because the strength of the lateral field dependence decreases with the amount of order in the material [34]. For instance, the Poole-Frenkel effect has been reported at room temperature in small-grain pentacene TFTs (with a mobility of 3.3×10^{-3} cm^2/Vs) [48], in P3HT TFTs (with a mobility of 4.6×10^{-2} cm^2/Vs) [47], and in TIPS-pentacene TFTs (with a mobility of 1.1×10^{-4} cm^2/Vs) [47]. However, in other samples of TIPS-pentacene (with a room temperature mobility of $\sim$1.2 cm^2/Vs), the mobility was independent of the lateral field at temperatures above $\sim$200 K [49], and, at high fields, the mobility increased with reducing temperature. Hence, these high mobility TFTs displayed quite different temperature and field dependent behaviour compared with their more disordered and lower mobility counterparts.

10.3 OTFT Architecture

The device architectures which have been used in OTFTs are all non-self-aligned, and are broadly the same as those used for a-Si:H and AOS TFTs, although there is no sign of one particular architecture being identified as the optimum choice for OTFTs. Whereas the a-Si:H TFTs are almost always inverted staggered, both top and bottom gate architectures have been used in OTFTs. The three widely used device configurations are shown in Fig. 10.8 [15], and the nomenclature used is

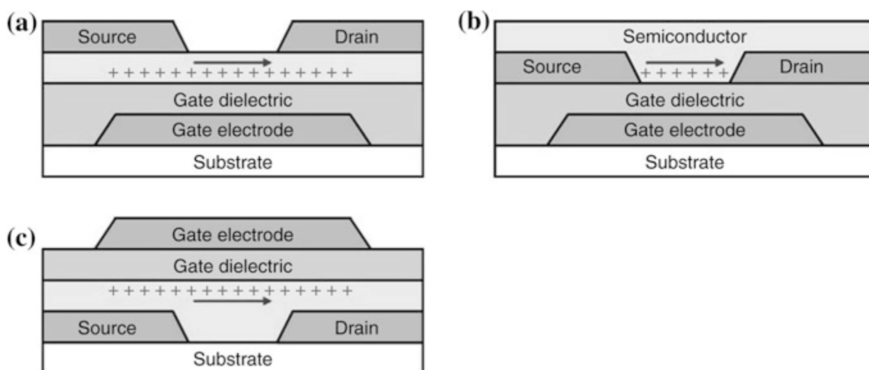


Fig. 10.8 OTFT architecture **a** *bottom* gate, *top* contact, BG/TC. **b** *bottom* gate, *bottom* contact, BG/BC, and **c** *top* gate, *bottom* contact TG/BC. (Reprinted with permission from [15])

slightly different from the inorganic TFTs, in that they are more often labelled bottom gate/top contact (BG/TC) rather than inverted staggered etc.

For much of the simple investigative work into the organic semiconductor layer itself, widespread use has been made of the bottom gated structure formed by using a doped silicon substrate as the gate electrode, and with its thermal oxide layer as the gate dielectric. The choice of the thermal oxide was implicitly assumed to provide a stable, high quality dielectric, such that all performance artefacts in the TFTs could be ascribed to the organic semiconductor itself. However, as will be seen in Sect. 10.4.3, SiO_2 films caused their own artefacts with respect to the performance of n-channel TFTs. Nevertheless, with the simple Si/SiO_2 structure, the main architectural choice is between top or bottom source/drain contacts, together with the issues related to the deposition and patterning of the source/drain contacts themselves. With bottom contacts, the metal can be deposited, and then defined using standard lithography techniques. This has the benefit that small channel lengths can be readily achieved, but the presence of the metal can interfere with the molecular alignment of the organic channel layer in the boundary region between the SiO_2 gate dielectric layer and the metal. Moreover, due to the large difference in conductivity of the OTFT channel and the metal contacts, the current flow from the channel to the contacts will be preferentially through the edge of the metal electrode in these BC structures [50]. In addition, molecular orientation discontinuities at this edge lead to contact resistance problems, as observed in pentacene TFTs with gold contacts [50, 51]. This effect is shown schematically in Fig. 10.9a [1], where the near vertically aligned molecules on the polar SiO_2 layer lose their order on the non-polar metal surface [50], and is responsible for the bright line at the SiO_2/Au boundary in the AFM image in Fig. 10.9b. The use of self-assembled mono-layers, SAMs, has been demonstrated to be effective in changing surface polarity, and increasing the overall polarity of the coated metal surface. This helps to maintain the same molecular ordering on the metal as on the SiO_2, giving the improved contrast uniformity at the SiO_2/Au

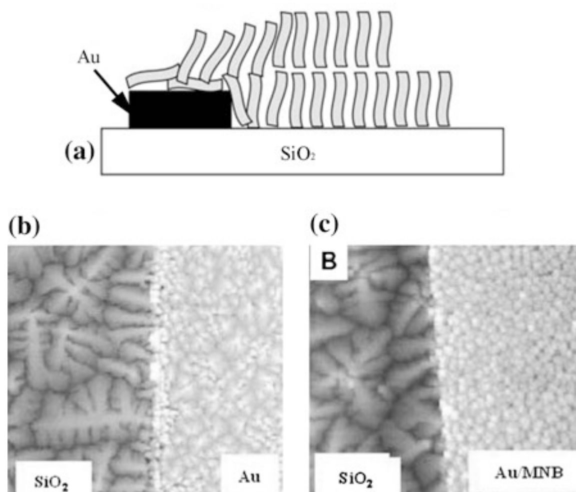


Fig. 10.9 **a** Illustration of pentacene misalignment at SiO_2/Au edges in BC TFTs, and AFM images of pentacene on SiO_2 and at the edge of the Au electrodes on **b** untreated surfaces, and **c** surfaces coated with a SAM. (Reproduced from [1] with permission of John Wiley & Sons, Inc)

edge in the AFM micrograph in Fig. 10.9c. Similar effects have been reported with 8 nm thick PMMA buffer layers [51]. The use of these layers has also been demonstrated to reduce contact resistance effects in BC TFTs [50, 51], and, because of the self-limiting thickness of SAMs, their direct contribution to series resistance is small [50].

For the simple process top-contact (BG/TC) OTFTs, a particular issue is potential damage to the organic layer both during the metal deposition, and in patterning it using conventional lithography, where the chemicals (photoresist, developer, etchant and solvent) may attack the organic layer [52]. To avoid these problems, it is common practice to use shadow-mask evaporation for the top contacts, thereby avoiding on-plate patterning. The major limitation with this approach is the minimum achievable channel length, which is likely to be of the order of ∼10–20 μm. Hence, this approach is not appropriate for devices with a channel length of just a few microns. Without the use of SAMs in BC devices, TC devices have usually given higher performance [50], but this difference has been substantially removed with SAMs in BC structures. One of the residual differences is then the additional series resistance in the BG/TC device due to the flow of current through the vertical thickness of the film from the channel at the bottom of the film to the contacts on the top of the film [53]. The impact on device performance of these architectural differences in BC and TC devices is discussed in greater detail in Sect. 10.5.3.

Another issue with the simplified device technology, irrespective of the contact position, is the patterning of the organic film itself. The patterning is to ensure that the channel width is sufficiently well defined to avoid the TFT performance artefacts discussed in Sect. 5.4.2, such as high leakage currents and erroneously large field effect mobility values. Given the problems associated with the lithography chemicals, active device area definition has been achieved, in some

instances, by simple scratch-isolation to form a trench around the device [19], or by shadow mask depositions [54]. However, more precise techniques have been implemented, which use lithography, but protect the organic film from direct chemical exposure. One example of this approach is to coat the structure with an organic solvent barrier, such as parylene [54], define it photolithographically, and use this film as a dry etch mask to pattern the organic layer beneath it. (This process is discussed further in Sect. 10.4.6). It has also been argued that some polymer semiconductors, such as poly(9,9-dioctylfluorene co-bithiophene), F8T2, do not need patterning, as its inherent conductivity is very low [55], but, further published work showed that island definition was used in high-quality demonstrator displays in order to obtain low-enough off-currents in the pixel TFTs [57].

The above non-lithographic techniques, using doped silicon substrates as a BG, have the merit of simplicity, and do not require extensive fabrication facilities, but are clearly only suitable for basic test devices, and are not appropriate for sophisticated demonstrator displays, nor for manufacturing. Nevertheless, these investigations have provided the background understanding of many materials, which have been incorporated into the range of contemporary demonstration displays, and which employ both top and bottom gates. An important consideration when comparing the processing of top and bottom gate structures, particularly with solution processing, is the solubility of the first deposited layer in the second, and this needs to be avoided by using orthogonal solvents for the different layers. Finally, a potential advantage of a TG structure, compared with a BG, is the automatic encapsulation of the active layer by the gate dielectric in the TG structures, and this can be used to suppress the ambient instability shown by many organic materials [56]. With BG structures, an encapsulant will need to be incorporated into the process if the channel material is susceptible to air-instabilities.

All three principal architectures have been used in demonstrators, as illustrated by the following examples: for oligomer-based displays, one group has implemented the BG/TC architecture for flexible AMOLED [4] and AMEPD [7] displays, whilst another group has used BG/BC for an AMOLED display [10]. For polymer materials, AMEPDs have been made with a TG/BC architecture [57], and high mobility, n-channel TFTs have been reported with the same TG/BC architecture [25, 58]. The processing conditions used to fabricate these devices are discussed in Sect. 10.4.6. The one architecture which has been little used is the TG/TC, almost certainly due to carrier injection problems.

10.4 Materials and Fabrication Processes

Sections 10.4.2–10.4.5 contain details of the materials used for the different device layers in OTFTs, in particular, the organic semiconductor, the gate dielectric and the metallisation layers, with the focus on the more widely studied materials, and those of current interest. The details include an overview of the deposition

procedures, and, as background to this, Sect. 10.4.1 briefly reviews solution processing techniques.

The most widely studied OS materials give p-channel TFT behaviour, and these are presented in Sect. 10.4.2, and, for clarity, the n-channel materials are discussed separately in Sect. 10.4.3. Examples of illustrative process flows for TFTs used in display demonstrators are shown in Sect. 10.4.6, and less conventional printing-based fabrication processes are reviewed in Sect. 10.4.7.

10.4.1 Solution Processing Techniques

One of the attractive features of OTFTs is the potential for low cost manufacturing by solution processing. Several techniques have been reported to implement this, including spin-coating, drop-casting, zone-casting, and printing, which are briefly reviewed below.

10.4.1.1 Spin-Coating

This process is commonplace for photo-resist application in conventional photolithography, and the controlling parameters to achieve a film of the required thickness are the volume of liquid deposited on the plate, the spin speed and the spin duration. The substrate temperature, or the post-spin anneal temperature, are also important for organic semiconductor films in order to control the solvent evaporation rate and the crystallisation of the film. In some cases, the polycrystalline film is formed directly after spin-coating on SAM coated substrates [59], whilst for other materials post-deposition baking [60] or solvent annealing was required [61]. Hence, the details of the required preparation procedure are very much material dependent.

10.4.1.2 Drop-Casting

Drop casting has been demonstrated for the deposition of triisopropylsilylethynyl pentacene (TIPS-pentacene) [62], which is a solution processable derivative of pentacene. The drop casting technique is illustrated in Fig. 10.10a [63], in which a solution of TIPS-pentacene in toluene was dropped from a capillary needle onto the TFT substrate tilted at 3.5° in a sealed jar, and allowed to evaporate. The process can also be implemented with horizontal substrates [64], but, with the tilted substrate, the lower drop line spread down the substrate, whilst its upper contact line remained pinned. Nucleation started at this upper line, and the crystallite stacking axis grew down the substrate, giving ribbon-shaped grains 200–800 nm thick, 20–80 μm wide, and 200 μm–5 mm long [63].

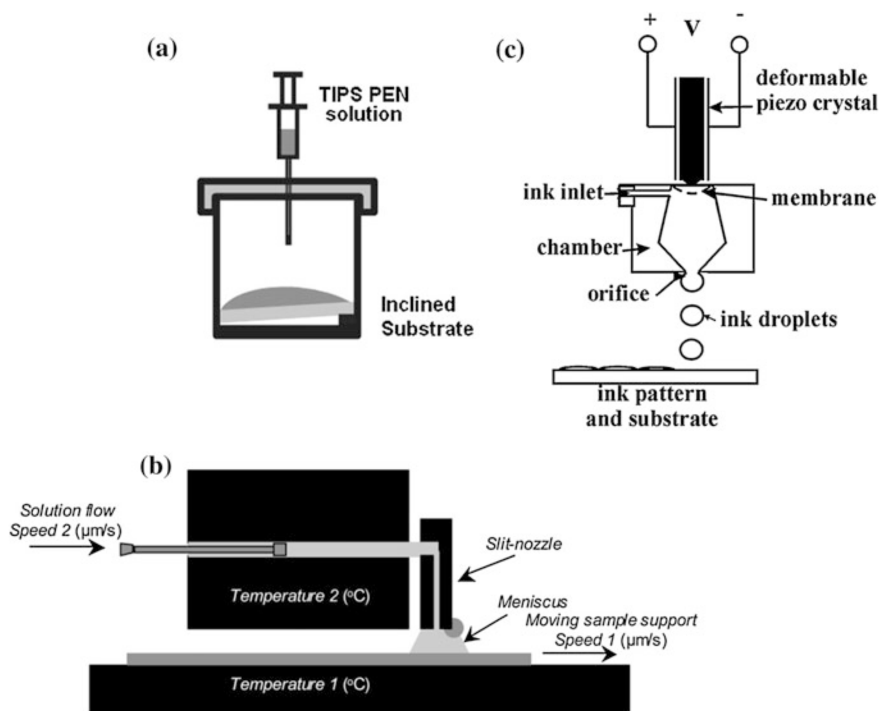


Fig. 10.10 Semiconductor layer deposition by **a** drop-casting (Reprinted with permission from [63]. Copyright (2007) American Institute of Physics). **b** Zone-casting (Reprinted with permission from [65]. Copyright (2008) American Chemical Society), and (c) inkjet printing (Reprinted from [71] with permission of IEEE)

10.4.1.3 Zone-Casting

Zone casting is a deposition technique in which the solubilized organic material is delivered to a moving substrate through a slit-like nozzle, as illustrated in Fig. 10.10b [65], and has been demonstrated with pentacene films derived from a solution of pentacene in an anhydrous chlorinated solvent. Grain size and quality was controlled by the temperature of both the liquid and the substrate, as well as by the substrate scanning speed and the flow rate of the liquid [65]. Under conditions optimised to obtain stationary film solidification, long grains were produced, with a width of 10–100 μm, and a length extending to millimetres in the substrate scanning direction. With this particular implementation using pentacene, the choice of substrate surface (which would be the gate dielectric in a BG TFT) was critical, and the best results were obtained with a BCB (divinylsiloxane-bis-benzocyclobutene resin) buffer layer on top of SiO_2. This gave extended grain growth, whereas bare SiO_2 resulted in cracks across the width of the grains [65].

10.4.1.4 Printing

Film deposition by printing has the major benefit of in-built pattern definition, as it delivers material only to those locations where it is needed. Hence, conventional lithography can be avoided, and, moreover, some of printing's unique features, such as sensitivity to substrate surface energy, can be exploited to deliver novel processing schemes [66], as discussed in Sect. 10.4.7. However, printing has a number of specific material requirements, such as the availability of appropriate inks for the printing of conductors, semiconductors, dielectrics, and of solvents for via hole opening. In addition, the inks need to have the correct viscosities and evaporation rates. The printing technique also has its own inherent limitations with respect to feature size, resolution, film thickness and plate throughput. Several different printing processes are available, including screen, offset, gravure and inkjet, which have quite different characteristics in terms of these parameters, and are reviewed in references [67, 68]. Although there are examples of all-printed TFTs and circuits using offset [69], and screen printing [70], more attention has been directed towards inkjet printing. Compared with the other printing techniques, inkjet can achieve relatively high resolution and alignment accuracy, although throughput is lower [67]. The preferred implementation of this technique is by piezo-electric drop-on-demand (rather than by continuous droplet delivery), and a schematic diagram of the print head is shown in Fig. 10.10c. A signal to the piezo crystal causes it to expand against a membrane, thereby increasing the pressure in the ink chamber, and ejecting an ink droplet [71]. Large area systems, with piezo-electric control of the printing nozzles, have been designed to release droplet volumes in the range 1–10 pL, with a positional accuracy of ± 5 μm [72]. Controlling the droplet size is crucial to line width control and positioning, and this will determine one of the most critical TFT dimensions, which is its channel length. For both top and bottom contact TFTs, this will be determined by the separation of the source and drain contacts. For example, 1 pL nozzles have been demonstrated to give 25 μm wide metallic tracks, using a silver ink [73], although repeated printing was necessary to produce lines of sufficient thickness to give an acceptable line resistance of 0.36 $\Omega/\square$. All other layers were also inkjet printed in this work, including the silver gate, the PVP gate dielectric, and the TIPS-pentacene active layer. As the dimensions of these layers were greater than those of the source/drain contacts, a 10 pL nozzle was used for faster printing. The finished device was a BG/BC structure with $W/L = 150/11$ μm, and had a field effect mobility of 0.05 cm^2/Vs [73]. For smaller channel lengths, down to 1 μm, a sub-femtolitre inkjet printing process has been demonstrated, using an ink containing silver nano-particles for the critically dimensioned source/drain contacts. In this case, n- and p-channel BG/TC OTFTs were fabricated, with the slow, but high-resolution, sub-femtolitre inkjet printing process used just for the source/drain contacts [74]. An alternative approach has been to use surface energy conditioning of the substrate to control its wetting properties, and to confine the droplet within these appropriately conditioned regions [55, 66, 67]. This process is discussed further in Sect. 10.4.7.

10.4.2 Organic Semiconductor Layers for p-Channel TFTs

10.4.2.1 Vacuum Thermal Evaporation

Pentacene is one of the most widely studied small molecule materials, largely because of its high performance, with mobility values equalling or exceeding those of a-Si:H. It has been extensively prepared from a purified source by vacuum evaporation at 10^{-4}–10^{-5} Pa, where the deposition rate has a strong influence on the grain size. This is seen in Fig. 10.11a–c by the AFM images from 60 nm thick films grown at different deposition rates on a SiO_2-coated substrate. All films showed a granular surface structure, where the largest grains were in films grown at 0.12 nm/min, and the smallest at 12 nm/min [75]. Very similar results have also been obtained for depositions onto PVP and PMMA coated substrates. The hole mobility directly correlated with increasing grain size, as shown in Fig. 10.11d, with the maximum mobility value approaching 2 cm^2/Vs for the largest grains [75]. In view of this result (and similar ones in Fig. 10.6d), evaporated pentacene is usually deposited at a rate of ~0.1 nm/min at room temperature. Higher substrate temperatures may be used, but there is a tendency for the evaporated film to contain an increasing fraction of the bulk pentacene crystalline form, rather than the 'thin-film' form, which would lead to reduced TFT performance.

In spite of its large mobility, one of the limitations of pentacene is its sensitivity to oxidising reactions, which, in unencapsulated devices, leads to device instability during ageing under ambient conditions [13, 76]. The instability is a reduction in hole mobility, which has been attributed to shallow state formation near the HOMO level [77]. Oxidation is a chemical reaction which involves electron transfer from pentacene to the oxidising agent, and the susceptibility of material to oxidation can be reduced by changing the molecular structure to one with a greater ionisation energy, and, hence, a deeper HOMO level [13, 76]. In principle, this would have the effect of increasing the injection barrier height for preferred contacts, such as gold, and, thereby, increasing the contact resistance [76]. However, whilst there is evidence for this effect [76], it does not appear to be universally present, and examples exist in which the molecular structure has been changed from pentacene to alternative molecules [13, 78], with a HOMO ~0.4 eV deeper, in which there was improved ambient stability, and only a small increase in the measured contact resistance [78]. The explanation for this variability in contact resistance between different samples is most likely due to the influence of different interfacial dipole layers. These more stable materials, shown in Fig. 10.12a, b, were di(phenylvinyl)anthracene (DVAnt) [78], and dinaphtho-[2, 3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) [13], with ionisation energies of 5.4 eV (compared with 5.0 eV for pentacene). Both were vacuum evaporated onto substrates held at 60 °C, and had similar TFT characteristics to pentacene, with hole mobilities of 0.3 and 0.6 cm^2/Vs, respectively. There is greater contemporary interest in DNTT due to its better air stability and mobility [15].

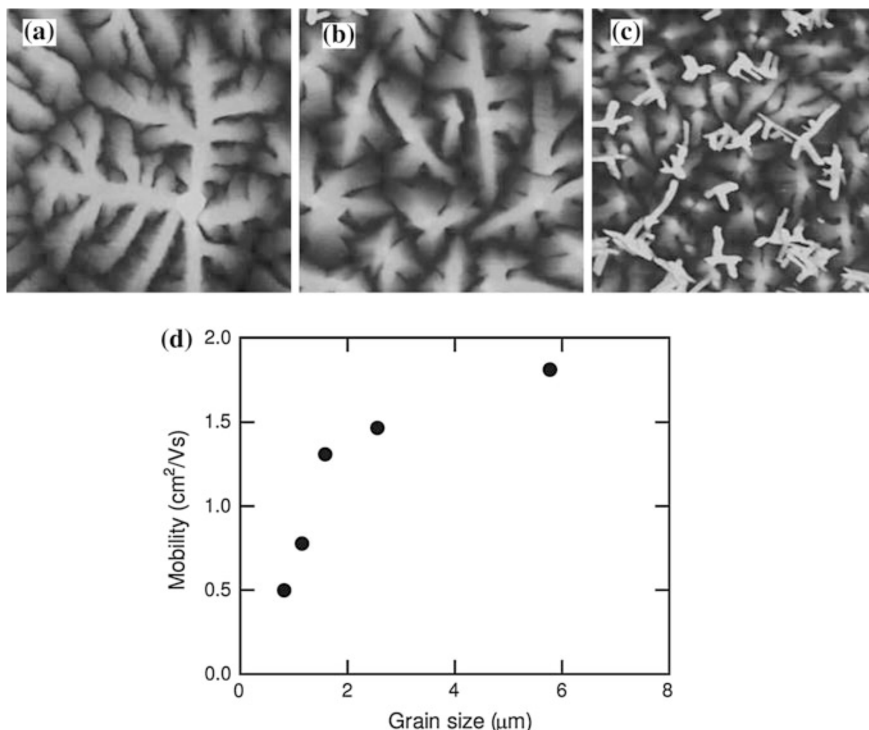


Fig. 10.11 AFM images of pentacene grains grown at deposition rates of **a** 0.12 nm/min, **b** 1.2 nm/min, and **c** 12 nm/min. The AFM image size is 5 μm × 5 μm. **d** variation of mobility with pentacene grain size (Reprinted from [75], with permission from IOP Publishing Ltd)

Although DVAnt and DNTT showed improved air-stability as a result of increased ionisation energies (which were achieved without a significant impact upon the effective height of the source injection barrier), there is a limit to the extent to which the ionisation energy can be increased without injection becoming a problem. An alternative approach has been to engineer the molecule so that it is inherently less reactive with oxygen, without increasing its HOMO, by adding substituents on the periphery of the molecule [79]. An example of this is vacuum-deposited 3,9-diphenyl-peri-xanthenoxanthene (Ph-PXX) (see Fig. 10.12c, with the H substituent). This is a derivative of peri-xanthenoxanthene, PXX [4, 79], and has an ionisation energy of 5.1 eV (i.e. similar to pentacene), but it displayed much better air-stability. The molecular packing structure was face-to-face, as opposed to the herringbone arrangement of pentacene, although the long molecular axis was similarly stacked perpendicular to the substrate surface. This material has been used in a 4.1in wide rollable AMOLED display, where the measured hole mobility of $\sim$0.4 cm^2/Vs was $\sim$4 times larger than pentacene prepared under identical conditions [4].

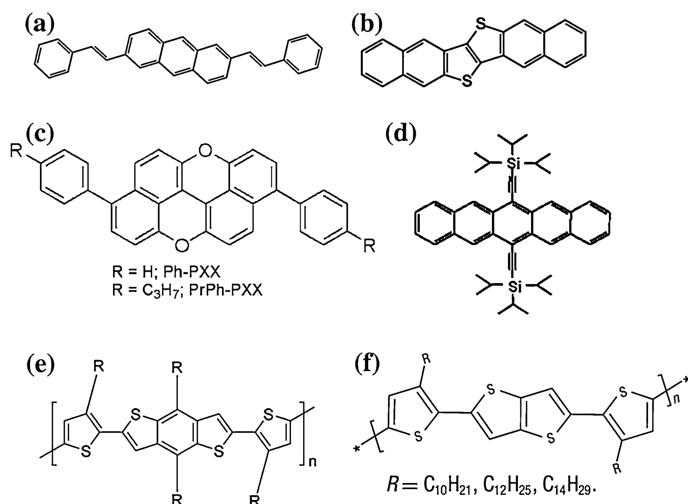


Fig. 10.12 Vacuum deposited small molecule semiconductors **a** di(phenylvinyl)anthracene, (DVAnt) (Reproduced from [78] with permission of John Wiley & Sons, Inc). **b** Dinaphtho-[2, 3-b:2',3'-f]thieno[3,2-b]thiophene, (DNTT) (Reproduced from [13] with permission of John Wiley & Sons, Inc), and **c** peri-xanthenoxanthene derivatives, Ph-PXX and PrPh-PXX (Reprinted with permission from [79]. Copyright (2009) American Chemical Society). Solution processed materials **d** triisopropylsilylethynyl pentacene, (TIPS-pentacene) (Reprinted with permission from [63]. Copyright (2007) American Institute of Physics). **e** poly(4,8-dialkyl-2,6-bis(3-alkylthiophen-2-yl)benzo[1,2-b:4,5-b']dithiophene), R = hexyl (Reprinted with permission from [87]. Copyright (2007) American Chemical Society), and **f** poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b] thiophene) (PBTTT) (Reprinted by permission from Macmillan Publishers Ltd: Nature Materials [60], copyright (2006))

10.4.2.2 Solution Processing

As discussed previously, solution processing is regarded as a more cost effective deposition technique than vacuum thermal evaporation, and has traditionally been used with polymer materials. Although much of the early work on pentacene used vacuum evaporation, there are now solubilised examples of pentacene and its derivatives, as well as of the PXX molecule discussed above. The oligomer and polymer materials are reviewed in the following two sub-sections.

Small Molecule Materials

Soluble pentacene pre-cursors have been used to deposit films of pentacene from solution, by, for instance, spin-coating a soluble derivative in chloroform solution, and then converting it into pentacene by annealing between 130 and 200 °C for 25 or 1.5 min, respectively [80]. A more extensive investigation compared spin-coating, drop-casting and zone-casting from a solution of pentacene in an anhydrous chlorinated solvent [65]. Under optimised deposition conditions, zone-casting was found

to give the best, and most continuous, long range grain structure, and the resulting TFTs had mobilities within the range 0.4–0.7 cm^2/Vs (which compared well with vacuum deposited pentacene films) [65]. Pentacene TFTs have also been printed, but with a non-conventional printing technique, using organic vapour jet printing, which was solvent free, and has been compared to thermal evaporation [81]. As with other solution based processing procedures, the performance of the printed TFTs compared well with TFTs made using vacuum deposited films.

Another solution processable material is triisopropylsilylethynyl pentacene, TIPS-pentacene, which is a functionalised derivative of pentacene with tri-iso-propylsilylethynyl substituents (the molecular structure is shown in Fig. 10.12d). It self-assembles in the solid-state with co-facial π–π stacking, rather than the herringbone stacking of pentacene, leading to closer packing of the pentacene molecules, and is also expected to be more oxidative stable than pentacene [83]. It has been widely investigated for solution processing using drop-casting [63], spin-coating [82], and, in another publication, optimised spin, dip, and drop-casting were compared [83]. In that work, when comparing both the structural organisation of the films, and the hole mobility in the TFTs, the drop-casting was found to give the best results, and spin-coating the worst. The spin and drop-cast films had mobilities of 0.05–0.2 and 0.2–1.8 cm^2/Vs, respectively. The mobility differences correlated with the differences in structural organisation, and were attributed to slower solvent release and slower film growth in the drop-cast films [83]. Compared with these high mobility TFTs, ink-jet printed TIPS-pentacene TFTs only had a mobility of 0.05 cm^2/Vs, which was associated with contact resistance effects to the ink-jet printed silver source/drain electrodes [73].

Another derivative of the molecule peri-xanthenoxanthene, PXX (which was discussed in Sect. 10.4.2.1 as having improved air-stability compared to pentacene) has been developed for solution processing. This is 3,9-bis(p-propylphenyl)-peri-xanthenoxanthene (PrPh-PXX) [7, 79], which differs from Ph-PXX by the replacement of hydrogen by the propanyl substituent on the phenyl end groups (see Fig. 10.12c). It has a HOMO level comparable to Ph-PXX. Films of PrPh-PXX were prepared by spin-coating a solution of it onto a PVP gate dielectric, which was then cured in air at 120 °C to remove the solvent and to crystallise the film. The resulting BG/TC TFTs had a hole mobility of ~ 0.5 cm^2/Vs, and were used in a 13.3in UXGA flexible AMEPD demonstrator [7]. The same material was also used to make a smaller, ink-jet printed 4.8in VGA AMEPD [84].

As is apparent from the above overview, high-performance solution-processed small molecule TFTs have been obtained using a number of different molecular materials and preparation techniques, but these procedures mainly produced undefined, large area films, which then needed patterning for TFT applications. Hence, while there are some examples of ink-jet printing of small molecule materials, it would appear that there is a need for the printing technologies to be further developed for widespread application to these materials.

Polymer Materials

Two extensively studied regio-regular polymers are P3HT [27, 85, 86] and PQT-12 [21] (see Fig. 10.3f, g), where the PQT-12 molecule has been engineered to give better air-stability then P3HT [21]. Solution processing has dispensed the purified material in a suitable solvent using spin-coating, dip-coating or drop-casting. For P3HT dissolved in chloroform, dip-coating gave the best results, and further improvement was obtained after annealing at 160 °C for 3 min in N_2, giving a mobility of 0.11 cm^2/Vs [86]. Spin-coating has, however, been successfully used with the solvent 1,2,4-trichlorobenzene [85], which has a higher boiling point than chloroform. This led to much slower drying of the films (compared with the chloroform solvent), and, following vacuum annealing at 100 °C, resulted in better controlled development of the characteristic crystalline domain structure discussed in Sect. 10.2.3, and shown in Fig. 10.5a. The hole mobility in these devices was 0.12 cm^2/Vs, which was 100 times greater than films spin-coated using a chloroform solvent. Similarly, PQT-12 has been applied by spin-coating, and post-deposition annealing at 120–140 °C improved both the lamellar packing and the hole mobility from 0.02–0.05 to 0.07–0.12 cm^2/Vs [21].

Other solution processable polymers have been reported, which have improved behaviour compared with P3HT and PQT-12, such as poly(4,8-dialkyl-2,6-bis (3-alkylthiophen-2-yl)benzo[1,2-b:4,5-b′]dithiophene) [87] (see Fig. 10.12e for its molecular formula). This was spin-coated from a 1,2-dichlorobenzene solution onto an OTS coated substrate, where it directly formed a well organised lamellar structure without post-deposition annealing. It solidified into $\sim 1 \times 1$ μm domains, giving a hole mobility of ~ 0.2 cm^2/Vs, and displayed improved air-stability compared with P3HT and PQT-12. Another polymer was poly(2,5-bis (3-alkylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTTT) (see Fig. 10.12f), which was a higher mobility polymer, with better air-stability [60]. The films were formed by spin-coating a solution of PBTTT in 1,2-dichlorobenzene, and annealing at 120–160 °C for 10–15 min. With the C14 alkyl substituents, this gave 200 nm grains, and a hole mobility of 0.6 cm^2/Vs. This mobility is larger than usually found with polymers, and is comparable to the better small molecule materials. PBTTT has a liquid crystal phase, which was established during the post-deposition annealing, and the high mobility was attributed to the organised assembly of the molecular chains in the LC phase, and their retention, as the structure crystallised [60].

As discussed in the previous section, the preferred deposition technique for low cost TFT fabrication is by printing. Amongst the polymers, P3HT has been deposited by inkjet printing, and TG/BC TFTs prepared by this process compared well with spin-coated TFTs, where the hole mobilities were ~ 0.08 and ~ 0.09 cm^2/Vs, respectively [88]. An inkjet printed proprietary p-channel polymer had better TFT characteristics, with a mobility of ~ 0.25 cm^2/Vs, whilst the mobility of its spin-coated control was 0.6 cm^2/Vs [88]. Although PQT-12 has also been ink-jet printed, its performance was poor, with a mobility of 1×10^{-4} cm^2/Vs, which was attributed to non-optimised preparation conditions [89]. The polymer poly(9,

9-dioctylfluoreneco-bithiophene), F8T2 [55], and other polyfluorene-based materials [57, 90], have been inkjet printed in demonstration displays. These materials had low mobilities of $\sim$0.03 cm^2/Vs [57], but were, nevertheless, good enough for AMEPDs.

10.4.3 Organic Semiconductor Layers for n-Channel TFTs

The development of high-performance OTFTs has traditionally been much easier with p-channel TFTs than with n-channel TFTs. A 2004 review paper [35] identified several issues with the operation of n-channel TFTs, including the high injection barrier with large work function metals and the ambient instability of low work function metals, low electron mobilities (in many cases $\ll$0.1 cm^2/Vs), the instability of these devices due to electron trap formation in the presence of oxygen and water vapour, and high threshold voltages with some high mobility materials [35]. Indeed, the question was raised whether there were fundamental reasons preventing the carrier mobility in n-channel TFTs from matching that in p-channel TFTs [36]. As mentioned above, a simple practical issue was the mismatch of the work function of the commonly used gold source/drain material with the LUMO level of the organic semiconductor. To resolve this injection problem, the LUMO had to be deeper, or a lower work function metal, such as Ca, had to be used. Neither approach solved the problem of poor n-channel performance. However, as discussed in Sect. 10.3, much of the basic materials work on OTFTs used a thermally oxidised Si substrate as a combined gate dielectric and gate electrode, and one of the key observations with n-channel operation was that hydroxyl molecules on the surface of the SiO_2 gate dielectric formed silanol, SiOH, electron traps at the dielectric/channel interface [36]. The trapping mechanism is shown in Fig. 10.13a, and the trapped electrons result in negatively charged defects, which compensate the gate field, and can result in very high threshold voltages. Although the silanol coverage of high quality SiO_2 surfaces is very small, at <10 % of a monolayer, this equates to a potential areal trap density of 3 to 7 $\times$ 10^{13} cm^{-2}, which is more than an order of magnitude greater than the electron densities induced by the gate bias. Hence, with an SiO_2 gate dielectric, a large fraction of the induced electrons were trapped at interface defects, and similar trapping effects were also observed with some other commonly used dielectrics including poly(vinyl phenol), PVP, and polyimide, both of which contain hydroxyl groups [36]. Using the poly-fluorene based semiconductor poly(9,9-dioctylfluorene-alt-benzothiadiazole), F8BT, the influence of the gate dielectric is shown in Fig. 10.13b. There was no TFT behaviour with the F8BT directly deposited onto a bare SiO_2 layer, but, after spin-coating the SiO_2 with a layer of polyethylene, good TFT operation was displayed, and the on-current increased by several orders of magnitude. Intermediate results were obtained with several SAMs, none of which was able to completely eliminate electron trapping at SiOH groups. These devices showed initial n-channel behaviour, but this was

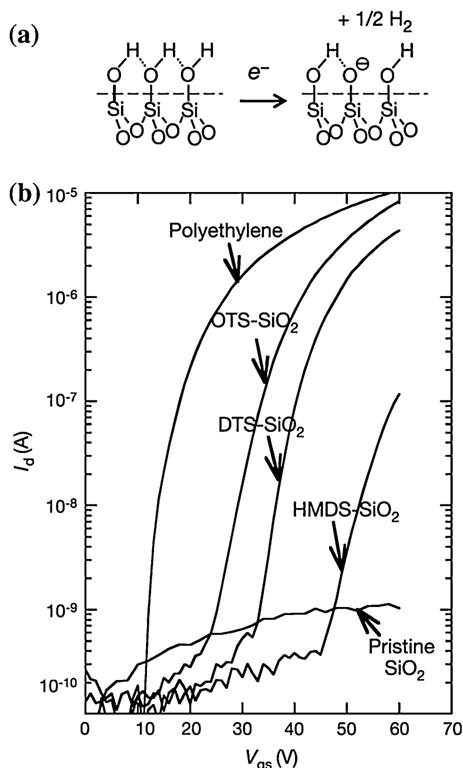


Fig. 10.13 **a** Silanol electron trapping mechanism at the semiconductor/SiO2 interface, and **b** transfer characteristics of F8BT n-channel TFTs with different gate dielectrics and SAMs (OTS, DTS and HMDS). (Reprinted by permission from Macmillan Publishers Ltd: Nature [36], copyright (2005))

quenched by strong air-instability effects [36]. It was also noted that the sensitivity to silanol trapping reduced with increasing depth of the LUMO level.

Although the use of an appropriate dielectric layer can suppress electron traps associated with silanol, this will not necessarily solve the problem of air-instability. The material's susceptibility to oxidation reactions is enhanced by the presence of channel electrons at the relatively shallow LUMO level, and these are able to react with oxygen and moisture in the ambient. Ambient instability in n-channel TFTs was reviewed in a 2007 paper [91], and, to address this instability, there is a requirement for either a dense molecular structure to suppress oxidant ingress [35, 91], or a deep enough LUMO to suppress the oxidation reactions [91, 92]. For the former, fluorinated side-group substituents may act as a kinetic barrier to the diffusion of oxidising species [35], and perfluorinated copper phthalocyanine, F_{16}CuPc, (see Fig. 10.14a) is a widely studied, air-stable n-channel material [35, 91, 93]. For LUMO-controlled instability, a minimum LUMO value of 4 eV has been identified [92], and this is consistent with other reports of air-stable n-channel TFTs using materials with LUMO values of 4.8 eV and 5.05 eV [93, 94]. It is worth noting that F_{16}CuPc, with a LUMO of 4.8 eV, possesses both attributes, but has a modest mobility of $\sim$0.08 cm^2/Vs [93].

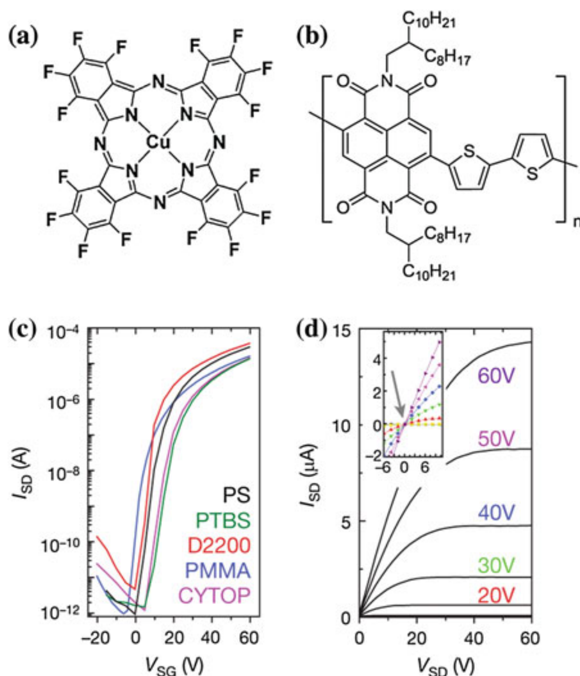


Fig. 10.14 **a** $F_{16}CuPc$ (Reprinted with permission from [91]. Copyright (2007) American Chemical Society). **b** P(NDI2OD-T2). **c** transfer characteristics of P(NDI2OD-T2) TG/BC TFTs (W/L = 1000/50) with different gate dielectrics (Cytop–(poly(perfluoroalkenylvinyl ether), k = 2.1), PTBS—(poly(t-butylstyrene), k = 2.4), PS—(polystyrene, k = 2.5), ActivInk D2200—(polyolefin-polyacrylate, k = 3.2) and PMMA—(poly(methylmethacrylate), k = 3.6), and **d** output characteristics of P(NDI2OD-T2) TFT with a PMMA gate dielectric. (Reprinted by permission from Macmillan Publishers Ltd: Nature [25], copyright (2009))

Many of the air-stable materials, with electron mobility values in the range ~0.1–0.6 cm^2/Vs, are oligomers, and are most easily deposited by vacuum evaporation [91, 93, 94], whereas an ideal n-channel material would be solution processable [37]. Such materials, which are air-stable, and have a mobility ≥0.1 cm^2/Vs, appear to be few in number [95], but, a promising candidate is the polymer poly{[N,N9-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,59-(2,29-bithiophene)}, (P(NDI2OD-T2). This has a LUMO level of ~4.0 eV, an optical band-gap of 1.45 eV, and its structure is shown in Fig. 10.14b [25]. The material is soluble in xylene and dichlorobenzene, and can be deposited by spin-coating, gravure printing or inkjet printing. It has been demonstrated in TG/BC structures, with a range of spin-coated polymer dielectrics, giving air-stable, n-channel TFTs with mobilities in the range 0.1–0.85 cm^2/Vs [25]. The highest mobilities of 0.65–0.85 cm^2/Vs were with a proprietary polyolefin-polyacrylate dielectric, D2200, but a PMMA dielectric gave the next highest mobility values in the range 0.2–0.45 cm^2/Vs. The transfer characteristics of devices made with P(NDI2OD-T2), and with a range of different spin-coated organic gate dielectrics, are shown in Fig. 10.14c. These have broadly similar characteristics, yielding high mobilities, as well as low threshold voltages, and on:off current ratios of 6–7 orders of magnitude [25]. In addition, the TFT output characteristics in Fig. 10.14d displayed good operation in both the linear and saturation regimes. Further commercial developments of P(NDI2OD-T2) have yielded a proprietary material for solution processable, air-stable n-channel TFTs

with a mobility of ~3.0 cm^2/Vs [96]. This has been demonstrated in spin-coated and inkjet printed TG/BC TFTs, using a proprietary gate dielectric, and fabricated on PET and PEN substrates. These devices displayed minimal degradation during 1400 h of accelerated bias-stress stability measurements, and this was assessed to be equivalent to an operating life of >10,000 h under typical AMOLED operating conditions [96].

One of the reasons for interest in n-channel TFTs is to enable the fabrication of low-power-dissipation complementary logic circuitry [25, 35, 37], and this was demonstrated with p- and n-channel TFT inverter circuits using P3HT and P(NDI2OD-T2) layers, respectively. These devices, with a common PMMA gate dielectric layer and Au contacts, showed inverter switching gains of 25 and 60 at supply voltages of 20 and 40 V, respectively [25]. Whilst there are many demonstrations of complementary inverter circuitry (for instance [11, 70, 88, 89, 94]), it has been argued that a simplification to the fabrication process may be achieved with a single ambipolar material, rather than with two separate materials for n-channel and p-channel operation. An important proviso for the ambipolar material is that it can deliver high performance, well-matched p- and n-channel operation using the same injecting electrodes [97]. (This necessarily requires small bandgap material, so that the injection barriers are low enough for each carrier type, and, equally, the material needs good transport properties for both holes and electrons). Ambipolar material would also ease potential compatibility issues with the dielectrics and contact materials for the two device types, as well as simplifying the definition stages for the device layers [97]. As with the more direct complementary devices, there are many reports of ambipolar material (for instance [42, 92, 95, 97–99]).

An example of ambipolar complementary device behaviour is shown in Fig. 10.15a–d [97]. The material for these devices was PSeDPPBT, which is a low bandgap polymer based upon a diketopyrrolopyrrole (DPP) core flanked with two selenophene rings (thiophene with the S replaced by Se) and a benzothiadiazole (BT) monomer. The device architecture was BC/TG with Au contacts. Both the PSeDPPBT, and the PMMA gate dielectric, were deposited by spin-coating, and, following annealing at 200 °C, saturation hole and electron mobilities of 0.46 cm^2/Vs and 0.84 cm^2/Vs, respectively, were obtained [97]. Although the material had a bandgap of 1.05 eV, current crowding, due to injection problems from the Au electrodes, is visible in the output characteristics at low drain biases. Figures 10.15a, c show the p-channel behaviour (at negative gate and drain biases), and the complementary n-channel behaviour with positive biases is seen in Fig. 10.15b, d. However, conventional p-channel and n-channel behaviour is only seen over certain voltage ranges (e.g. large negative gate and drain biases for p-channel, and the opposite conditions for n-channel). Outside these ranges, and in contrast to the usual unipolar devices, there are anomalous features in the transfer and output characteristics. For instance, for the ‘p-channel’ operation, at large negative drain bias and small positive gate bias, there is an increasing minimum off-current with increasing drain bias, which is characteristic of ambipolar device behaviour [98]. Over this voltage range, the surface adjacent to the negatively

biased 'drain' terminal becomes electron accumulated, with the terminal acting as the 'source' for n-channel conduction. Hence, the anomalous appearance of the characteristics occurs when the device is ceasing to act as a unipolar device, and is, instead, supporting ambipolar conduction. This is also responsible for the absence of saturation in the output characteristics at low gate biases in Fig. 10.15c, d. The potentially poor off-currents adversely affect the power dissipation in inverter circuits (compared with conventional complementary TFT inverters), and ambipolar inverters are also unable to fully switch the output voltage between the supply voltage and ground [97, 98]. Hence, the trade-off with ambipolar inverters is potentially simpler device processing, but with reduced inverter performance.

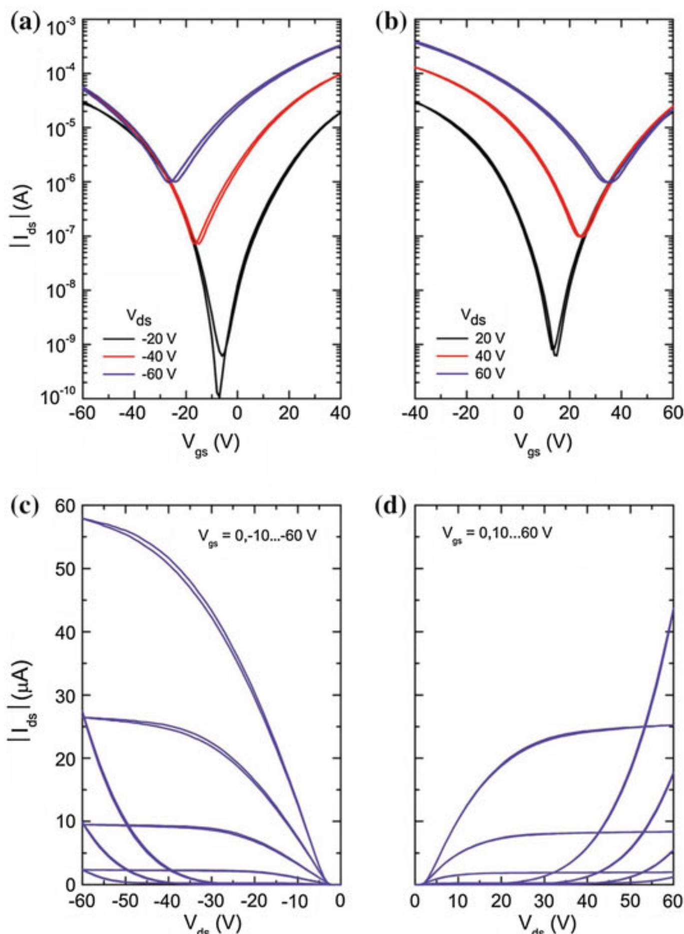


Fig. 10.15 Transfer and ouput characteristics obtained from a PSeDPPBT ambipolar device. **a** and **c** p-channel, and **b** and **d** n-channel behaviour at negative and positive gate and drain biases, respectively. (Reproduced from [97] with permission of John Wiley & Sons, Inc)

Nevertheless, there is continuing interest in this approach, and PSeDPPBT inverters (using pairs of self-aligned ambipolar TFTs) had gains of >30 and >40 at supply voltages of 10 and 20 V, respectively, and 3-stage ring oscillators operated at 182 kHz, with a small delay/stage of 0.91 μs at a supply voltage of 50 V [97].

10.4.4 Gate Dielectric

As is clear from the preceding sections, much of the simple investigative materials work has been carried out using thermally grown SiO_2 (dielectric constant, $k = 3.9$) as the gate dielectric, but this material is not relevant to low cost glass and polymer substrates, which is where the main application of OTFTs is expected to be. Moreover, as discussed in Sect. 10.4.3, SiO_2 also gave unacceptably poor n-channel TFT performance [36]. Hence, there was a clear need for alternative dielectrics to SiO_2. Nevertheless, the basic materials research using this dielectric identified the critical importance of the semiconductor/dielectric interface [100], and the key role of SAMs in tailoring the interface to promote the required ordering of the semiconductor on both the dielectric [101], and on the metal contacts in BC structures.

The dielectric material requirements for high performance OTFTs are similar to those of other TFTs, namely: a very good dielectric/semiconductor interface (which generally requires a smooth surface), low leakage currents and low pin-hole densities, and a high dielectric breakdown field in excess of several MV/cm [102]. Three broad classes of dielectric have been investigated: (a) inorganic layers, such as SiN_x and SiO_x, as well as some other inorganic materials chosen for their large dielectric constants (high-k materials), (b) organic layers, many of which have dielectric constants, k, in the range 2.0–4.5 [101], and (c) self-assembled monolayers [101–103]. As mentioned previously, SAMs are also extensively used in combination with many other dielectric layers, and two of the more common SAMs are octadecyltrichorosilane (OTS) and hexamethyldisilazane (HMDS).

There are other desirable TFT attributes, which can be enhanced by the appropriate choice of gate dielectric, such as low voltage operation, and solution processing. However, the particular material choices may be constrained in order to mitigate their effect upon other parameters. For instance, low voltage operation would, in principle, require a thin dielectric layer, but this may be incompatible with a low leakage current and low pin-hole density, and, indeed, the thickness range of organic dielectrics is ~300 nm, or more, to minimise gate leakage [102]. On the other hand, SAMs are especially thin, and have been demonstrated as gate dielectrics of potential interest [102–104]. An alternative approach to low voltage operation is the use of high-k materials, which would favour inorganic dielectrics, but these would not necessarily be compatible with solution processing. In addition, the higher dielectric constant insulators are more polar, and have been found to degrade TFT performance due to increased carrier trapping in disordered

interfacial regions [101, 105, 106]. For solution processed materials, it is also essential to use orthogonal solvents with the different layers, so that the deposition of the organic semiconductor does not dissolve the already-deposited dielectric layer in BG structures, and vice versa in TG structures. The three dielectric options listed above are briefly reviewed in the following sub-sections.

10.4.4.1 Inorganic Dielectrics

High performance OTFTs, using both solution-processed PQT-12 and pentacene, have been demonstrated using PECVD SiO_x (k $\sim$ 4.0) and SiN_x (k = 4.5–7.2) as the gate dielectric in combination with the SAMs OTS or β-phenethyltrichlorosilane (PTS) [107, 108]. It was argued that the extensive experience of these dielectrics within the inorganic TFT industry, including the availability of large area deposition equipment, makes them a low-risk route to manufacturing. However, the well-established dielectric deposition processes are at $\sim$300 °C, and pentacene TFTs with a 300 °C SiN_x dielectric had comparable performance to devices with a thermal SiO_2 gate dielectric [108]. In contrast, PQT-12 TFTs processed on plastic substrates, using SiN_x deposited at 150 °C and SiO_x at 180 °C, showed a smaller carrier mobility compared with higher temperature depositions of these materials [107]. (Details of the PECVD deposition processes for SiN_x and SiO_x can be found in Sects. 5.5.3 and 7.3.1, respectively).

Other inorganic insulators have been grown by oxidation of the gate metals Al and Ta, forming AlO_x [109] and Ta_2O_5 [10, 110], respectively. The AlO_x was grown by plasma oxidation of the Al gate, and coated with a SAM, to produce complementary TFT inverter circuits (using pentacene and $F_{16}CuPc$) on a polyimide substrate [109]. The Ta_2O_5 (k = 24) was formed by anodization of the Ta gate, and was then coated with an HMDS SAM before vacuum deposition of pentacene. These TFTs were used as drive transistors in an AMOLED display on a PEN substrate [110].

Some other high-k dielectrics, which have been used in low-voltage pentacene TFTs, were HfO_2 (k = 14.9) [111], and HfLaO (k = 10.4) [112]. The 50 nm thick HfO_2 films were deposited by atomic layer deposition at 200 °C, and its surface was modified with phosphonic acid to passivate the polar surface groups, and to improve the pentacene morphology. The resulting TFTs displayed low voltage operation with a sub-threshold slope of 120 mV/dec, a threshold voltage of −0.4 V, and a carrier mobility of 0.4 cm^2/Vs [111]. In contrast, 40 nm thick HfLaO films, deposited by RF sputtering, required annealing in NH_3 at 400 °C, and did not display such low voltage operation, with the sub-threshold slope and threshold voltage being 0.26 V/dec and −2.6 V, respectively [112]. It is clear that the differences in the TFT parameter values between these two dielectrics cannot be simply ascribed to differences in film thickness and dielectric constant. The HfLaO films did not have any surface modification beyond the NH_3 exposure, and it is possible that the polar dielectric was degrading the interface, as has been reported with other polar dielectric films [105, 106]. Indeed, by deliberately

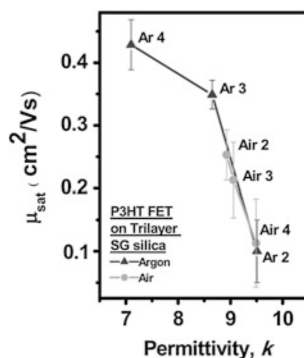


Fig. 10.16 Field effect mobility in P3HT TFTs as a function of the dielectric constant of the tri-layer sol-gel silica gate dielectric. (Reprinted with permission from [106]. Copyright (2009) American Institute of Physics)

changing the dielectric constant, k, over the range 7–10, in tri-layer sol-gel silica gate dielectric films, the carrier mobility in both pentacene and P3HT BG/TC TFTs was found to reduce as the dielectric constant was increased, as shown in Fig. 10.16 [106]. In these samples, the dielectric constant was modified by exposing the first and second surfaces in the tri-layer films to an argon or air plasma, before the deposition of the next sol-gel layer. This changed the concentration of polar OH groups in the films, and it was concluded that the polarisability of the film influenced the carrier flow in the TFT channels [106]. Parallels were drawn between this result and comparable k-dependent mobility values seen with organic dielectrics [105], as discussed in the next section.

10.4.4.2 Organic Dielectrics

The interest in organic insulators stems, in part, from their solution processability, and the characteristics of a wide range of organic dielectric films have been extensively reviewed [101, 102, 105]. Some of the more widely investigated materials (with dielectric constants comparable to, or greater than, SiO_2) are PVP (polyvinylphenol, $k = 4.5$), PMMA (polymethylmethacrylate, $k = 3.5$), and PVA (polyvinylalcohol, $k = 7.8$), and amongst the lower-k materials are Cytop ($k = 2.1$), and PPCB (polypropylene-co-butene, $k = 2.3$). The chemical structures of these materials are shown in Fig. 10.17a–e. They are usually solution processed, by, for instance, spin-coating, and then annealed to remove the solvent and also to cross-link the film. When the low-k dielectrics were used with several different TFT materials, including P3HT, F8T2, and the low-mobility amorphous polytri-arylamine semiconductor (PTAA), they were found to result in higher carrier mobilities than observed with PVP, PMMA, PVA and other high-k dielectrics [101, 105]. This is illustrated for PTAA by the dependence of mobility on dielectric constant, in Fig. 10.18a, and by the temperature dependence of the mobilities in Fig. 10.18b [105]. In Fig. 10.18b, the field effect mobility for different dielectrics is compared with the bulk mobility (evaluated by time of flight, TOF, measurements), and the reducing absolute values of field effect

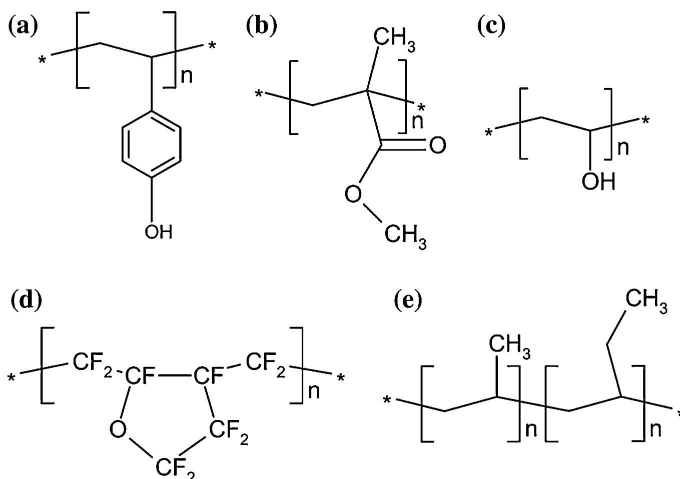


Fig. 10.17 Chemical structures of common organic gate dielectrics **a** PVP, **b** PMMA, **c** PVA, **d** Cytop, and **e** PPCB. (Reprinted with permission from [101]. Copyright (2004) American Chemical Society)

mobility, and their increasing activation energy, with increasing dielectric constant were attributed to increased carrier localisation at the semiconductor/dielectric interface. The model for this is shown in Fig. 10.18c, with a Gaussian DOS distribution in the semiconductor. The effect of the random orientation of dipoles in the high-k, polar dielectrics was to increase the energy fluctuations, and, hence, the disorder, in the semiconductor surface. This was characterised by a broadening of the DOS at the interface, leading to increased carrier trapping. It was also suggested that the use of SAMs not only improved the packing order of the organic semiconductor molecules in BG structures, but also partially screened the effects of the polar dielectric, thereby making a further contribution to increased carrier mobility [105].

The influence of the organic dielectric on pentacene film growth, and TFT performance, has been studied with the dielectrics PVP, PVA, poly(2-vinylnaphthalene) (PVN), polystyrene (PS), and poly(4-methylstyrene) (PMS) [100]. The dielectrics were selected for their differing glass transition temperatures, T_G, and surface contact angles. Polymer dielectric thicknesses of 320–360 nm were used in BG/TC structures by spin-coating them onto thermally oxidised silicon, and then vacuum baking them at 80 °C. (Uncoated SiO_2 layers, referred to as 'bare', were used as control samples). For pentacene evaporated onto substrates held near room temperature, the gate dielectric was found to influence the pentacene grain size, as shown in Fig. 10.19, but this varying grain size had little impact upon device performance and carrier mobility. The largest grains were on the PVP and 'bare' surfaces, which had the lowest contact angles, and were the most hydrophilic. This permitted greater movement of the pentacene molecules on the dielectric surface, resulting in the larger grains. The worst samples were grown on the PVA film,

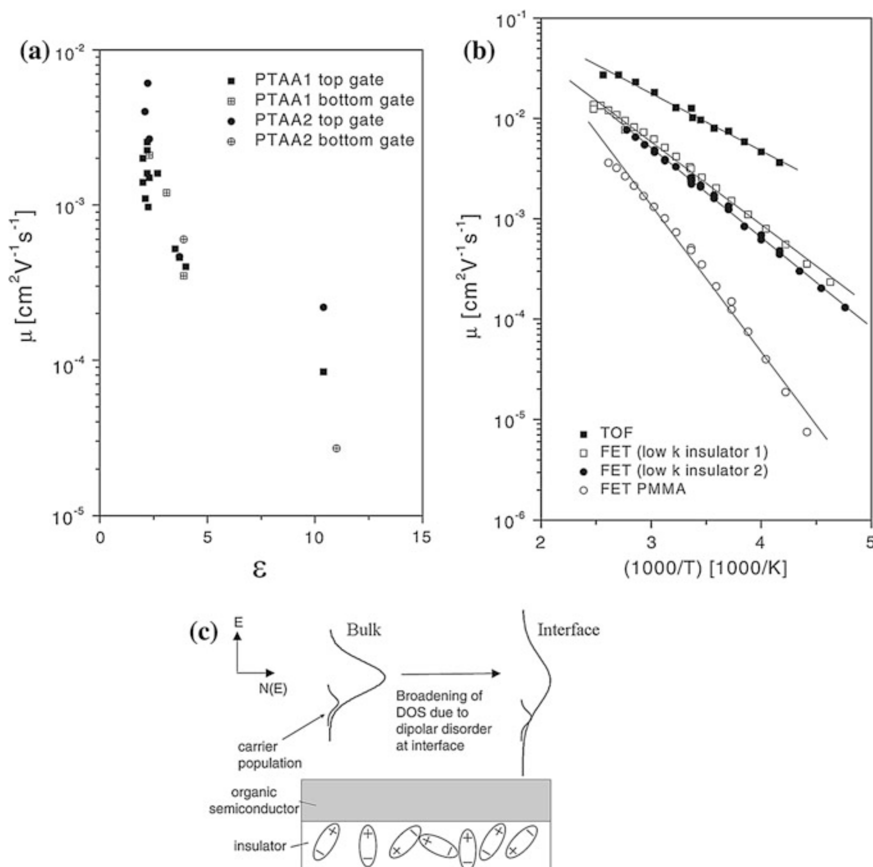


Fig. 10.18 **a** Carrier mobility measured in PTAA TFTs as a function of the dielectric constant of the gate dielectric. **b** Temperature dependence of the mobility for different gate dielectrics, and **c** schematic illustration of the effects of disorder induced in the DOS at the semiconductor surface by a polar dielectric. (Reproduced from [105] with permission of John Wiley & Sons, Inc)

which has a bulk T_G of 49 °C, whereas the others were >100 °C [100]. The small grain size with PVA was attributed to a surface T_G smaller than the bulk value, which perturbed the film during pentacene deposition, resulting in a rough interface. For the other films, it was concluded that for grain sizes above ~0.8 μm, grain boundary trapping had only a secondary effect on charge transport [100]. It was also noted that, in these samples, the dielectric constant had a smaller impact upon the carrier mobility than reported in other work. Indeed, there are examples in the literature, in which the trends with k were the opposite from those discussed above [101, 102]. Hence, the detailed understanding of the role of the dielectric in OTFTs is still incomplete.

The largest grains in Fig. 10.19 were grown on a PVP dielectric, and this material, which can be inkjet printed [73], as well as spin-coated, is widely used as

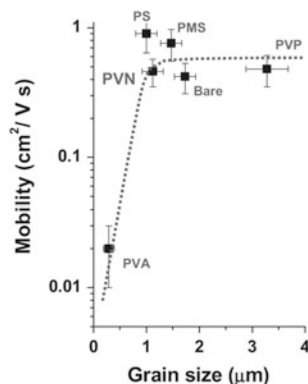


Fig. 10.19 Influence of organic gate dielectric on pentacene grain size and carrier mobility. (Reproduced from [100] with permission of John Wiley & Sons, Inc)

a polymer dielectric in TFT studies. It has also been used in demonstrator displays on flexible substrates, in which it was mixed with OTS to reduce the cross-linking anneal temperature [4, 7].

10.4.4.3 Self-Assembled Monolayers

The use of SAMs as gate dielectrics has been reviewed in Ref. [102], in which layers ~3 nm thick have displayed good dielectric properties. For instance, 2.8 nm thick OTS SAMs gave low leakage currents of 10^{-8} A/cm^2 at 5 MV/cm, and breakdown fields of 9–12 MV/cm. Improved TFT performance was achieved by adding a phenoxy end group to OTS, forming PhO-OTS (k = 2.5), which displayed closer molecular packing than OTS, and facilitated the fabrication of BG/TC pentacene TFTs [113]. (The OTS SAM alone had not functioned as an effective gate insulator with pentacene due to their intermixing). With the 2.5 nm PhO-OTS SAM insulator, the pentacene TFTs had a sub-threshold slope of 100 mV/dec, a threshold voltage of −1.3 V, and a mobility of 1 cm^2/Vs. Other SAM insulators of interest have been alkylphosphonic acid molecules, in which the length of the alkyl chain C_nH_{2n+1} was optimised for minimum gate leakage currents and good pentacene TFT performance, by using n values of 14–16 [104].

10.4.5 Metals

The metals used in TFTs are for the gate, and the source/drain contacts, and for the bus bars in displays and circuits, and, although the latter are usually the same metals as used in the TFTs, they can be different. Where the structure has a BG, it is often convenient to use evaporation or sputtering to deposit the gate metal, and lithography to define it. For TG structures, with a polymer gate dielectric, this may be less practical, and solution processing is one option. For the source/drain contacts, gold

is widely used in both experimental TFTs, as well as in demonstrator devices, but its deposition is limited to vacuum evaporation. For full solution-processing of devices, other materials have been investigated for both the TG metal and source/drain contacts. These have included inkjet printing of dispersions of inorganic metallic nano-particles [90], such as silver, which had a resistivity 8 μΩcm, and repeat printing was used to build up 200 nm thick layers, with a sheet resistance of 0.4 Ω/□ [70]. However, although Ag has very good conductivity, its work function is quite low at 4.7 eV [114], and contact resistance effects have been noted in printed TIPS-pentacene TFTs with Ag contacts [70, 114]. The use of thiol-based SAMs has been demonstrated to reduce the injection barrier at the Ag/TIPS-pentacene interface, and this improved the mobility from 0.01–0.04 cm^2/Vs to 0.04–0.17 cm^2/Vs for bare and treated Ag electrodes, respectively [114]. Source/drain contacts have also been inkjet printed using poly(ethylenedioxythiophene) doped with poly(styrene sulfonic acid) (PEDOT/PSS) [90]. This has low contact resistance into many TFT materials, but its large resistivity of 0.01 Ωcm makes it unsuitable for bus bars and gate lines [90].

10.4.6 Process Flow

Given the variety of materials used for both the organic semiconductor and for the gate dielectric, plus the various deposition options, there is not, at this moment, a consensus on the preferred choice of components, and, hence, there is not a typical device processing schedule. In view of this, the following two examples are simply illustrative of processes which have been implemented with small molecule and polymer semiconductors, and should not be regarded as representative of the industry as a whole.

The first example is of a flexible AMOLED display, addressed by BG/BC pentacene TFTs on a PEN substrate [10, 110]. Some of the key process stages in the process are illustrated in Fig. 10.20, and are listed below:

(i) RF sputter deposition of SiO_2 and SiN_x films onto the PEN substrate as barrier and adhesion layers,
(ii) RF sputter deposition of Ta, and its definition into gate electrodes by reactive ion etching,
(iii) Anodisation of Ta gate to form 170–200 nm thick Ta_2O_5 gate dielectric,
(iv) Deposition and definition of Cr/Au source/drain contacts, and ITO pixel electrode,
(v) Deposition of HMDS SAM,
(vi) Vacuum deposition of 100 nm of pentacene,
(vii) Room temperature CVD deposition of parylene (2 μm) and sputter deposition of SiO_2 (50 nm),
(viii) Photoresist application and photolithographic patterning,

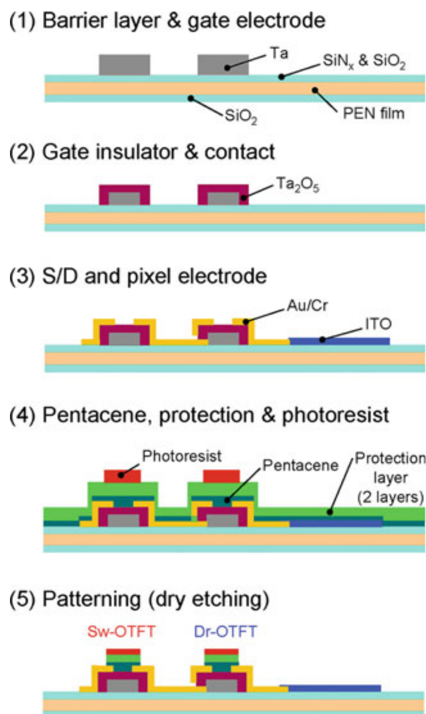


Fig. 10.20 Fabrication stages of pentacene TFTs for an AMOLED display. (Reprinted from [10] with permission of SID)

(ix) CF_4 plasma etching of SiO_2, which then acted as the etch mask for oxygen plasma etching of the parylene and pentacene layers.
(x) Final encapsulation with parylene and a photosensitive polymer.

These TFTs had a mobility of 0.05–0.1 cm^2/Vs, an on:off ratio of >10^6, and a threshold voltage of 12 V.

The second example is of a flexible AMEPD using TG/BC unpatterned polymer TFTs, and the pixel/device cross section is shown in Fig. 10.21 [115]. The processing steps were based upon direct-write solution processing and laser patterning, without the need for mask alignment. The main fabrication stages were:

(i) PET substrate planarization,
(ii) Source/drain metal deposition (unspecified procedure),
(iii) Unpatterned polyfluorene-based semiconductor deposition (unspecified procedure),
(iv) Spin-coat polymer dielectric layer,
(v) Inkjet print Ag gate electrode,
(vi) Deposition of organic dielectric passivation layer (10 μm),
(vii) Via hole opening by laser ablation,
(viii) Inkjet print PEDOT/PSS pixel electrode.

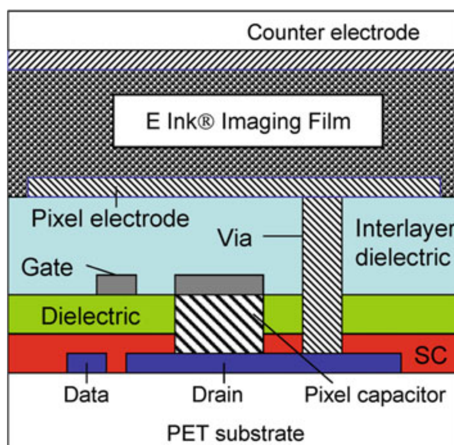


Fig. 10.21 AMEPD pixel/TFT cross section. (Reprinted from [115] with permission of SID)

These TFTs had a mobility of 0.01 cm^2/Vs, an on:off ratio of 10^4, and a threshold voltage of −5 to −10 V. The poor on:off ratio was attributed to the undefined channel layer, and, in later work, this ratio was improved to 10^5–10^6 by patterning the semiconductor [57].

10.4.7 Novel Processing

One of the challenges with inkjet printing is achieving fine lines and short channel lengths, and surface energy conditioning procedures have been demonstrated to address these issues [90], and even to facilitate sub-100 nm channel lengths [66]. The key feature in this approach was to change the wetting-angle of the sample surface, so that hydrophobic and hydrophilic regions were defined, which were then used to localise water-based conducting polymer ink drops. This procedure is shown in Fig. 10.22a, in which the surface of a hydrophobic layer was locally exposed to a laser beam to create hydrophilic regions. Because of the high resolution and positioning accuracy of the laser, gaps of a few microns were defined between the exposed regions, which became the TFT channel regions. When the water-based PEDOT/PSS inks were printed over these areas, the inks were rejected from the hydrophobic regions and retained within the hydrophilic regions. These regions formed the source and drain contacts, with a separation down to 10 μm. Then a polymer semiconductor, such as F8T2, was inkjet printed over these contacts, followed by solution deposition of a polymer gate dielectric, and inkjet printing of a 45 μm wide silver gate electrode, with a positional accuracy of ±20 μm [90]. The devices with L = 10 μm had a mobility of 8×10^{-3} cm^2/Vs and an on:off ratio of 10^5, which was comparable to more conventionally fabricated devices with photolithographically defined gold electrodes. Alternative surface conditioning procedures were also described, such as the use of an electron

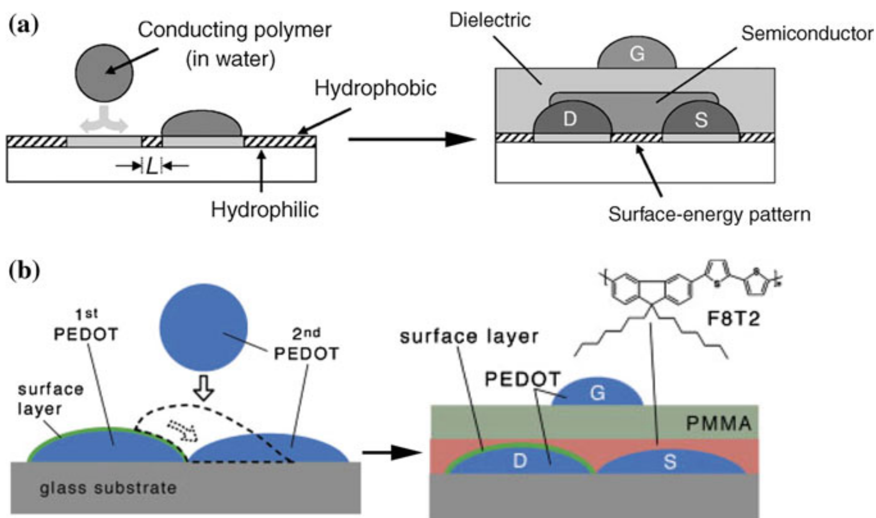


Fig. 10.22 **a** TG/BC TFT printing, using substrate surface patterning to confine the water-based droplets of PEDOT-PSS forming the source and drain regions (Reprinted from [90]. Copyright © Materials Research Society 2003), and **b** sub-100 nm channel length TFTs using self-separating source/drain regions, formed by surface modification of the first droplet. (Reproduced from [66] with permission of John Wiley & Sons, Inc)

beam to write a fine exposure pattern in a PMMA photoresist film, which had been deposited on a SiO_2 layer. These PMMA patterned areas were ultimately used as a template to localise the subsequently printed PEDOT/PSS source/drain regions, giving sub-micron channel lengths [90].

A further extension of this procedure is shown in Fig. 10.22b, and this avoided the direct surface energy patterning of the substrate itself [66]. In this case, the surface of the first droplet was modified to make it hydrophobic, such that, when the second droplet was released onto it, it slid off leaving a small gap between the two. This self-alignment of the source and drain areas did not require precise alignment of the second droplet. The surface of the first PEDOT/PPS ink droplet was made hydrophobic by either exposing it to a CF_4 plasma, which fluorinated it, and, at the same time, the exposed glass substrate surface was made hydrophilic by the etching action of the plasma. The alternative procedure was to have a suitable surfactant within the ink, which segregated to the surface on drying. Device processing was completed with the addition of solution processed layers of F8T2, a 120–130 nm thick PMMA dielectric, and the inkjet printing of the top gate. The channel length in the published device was estimated to be ~60 nm, with an on:off ratio of 10^4 for $V_d < -5$ V [66]. The devices had significant contact resistance, and displayed other short channel effects, which is understandable in a device with such a short channel and thick gate dielectric. (More detailed information on short channel effects, and their amelioration, can be found in Sect. 8.7).

10.5 OTFT Characteristics

10.5.1 General

A representative set of transfer and output characteristics for a Ph-PXX p-channel TFT, with L = 50 μm, is shown in Fig. 10.23a, b, respectively [79]. Similar curves have been published for other high quality p-channel OTFTs, and Fig. 10.14c, d show the equivalent set of characteristics for a P(NDI2OD-T2) n-channel TFT [25]. The Ph-PXX transfer characteristics measured in saturation, at a drain bias of −40 V, are shown in Fig. 10.23a, and the right hand axis is a plot of the square root of drain current versus gate bias. This shows reasonable linearity, and, as with inorganic TFTs, the simple MOSFET equations developed in Chap. 3 were used to extract the performance parameters of OTFTs from their transfer characteristics. In the saturation regime, the field effect mobility is calculated from the slope of the $\sqrt{I_d} - V_G$ plot using Eq. 3.18, i.e.

$$\mu_{FE} = \frac{2L}{WC_i}\left(\frac{d\sqrt{I_d}}{dV_G}\right)^2 \tag{10.4}$$

and the threshold voltage is given by the extrapolated intersection of this curve with the V_G axis. In the example shown, the mobility was ∼0.42 cm^2/Vs, and the threshold voltage was ∼0 V [79]. The output characteristics in Fig. 10.23b show good saturation and negligible current crowding at zero drain bias, which is indicative of good injecting contacts. With these contacts, it would be possible to extract the mobility at low drain bias in the linear regime, however, as injection problems are frequently encountered in OTFTs, the mobility is more commonly extracted in the saturation regime.

Examples of good and bad injecting contacts in TIPS-pentacene TFTs, with Ag source/drain contacts, are shown in Fig. 10.23c, d, respectively [114]. The difference between the two TFTs was in the surface treatment of the Ag electrodes by different thiophenol-based SAMs. These changed the effective work function of the Ag, which, in the good case, was a much closer match to the HOMO of the TIPS-pentacene, and gave the linear $I_d - V_d$ curves at low drain bias in Fig. 10.23c. The key characteristic of the bad contact, in Fig. 10.23d, was the non-linearity of the curves near zero drain bias, which is referred to as current crowding, and would preclude an assessment of field effect mobility in the linear regime. The series resistance associated with this injection barrier was also responsible for the order of magnitude reduction in the current in the saturation regime compared with the good sample. It is worth noting that the impact of series resistance at the injecting contact is also a function of its magnitude relative to the channel resistance, and a good injecting contact, at low gate bias and long channel length, can become a poor one as the channel resistance is decreased by either reducing the channel length and/or increasing the gate bias [53, 117]. Contact effects are discussed further in Sect. 10.5.2.

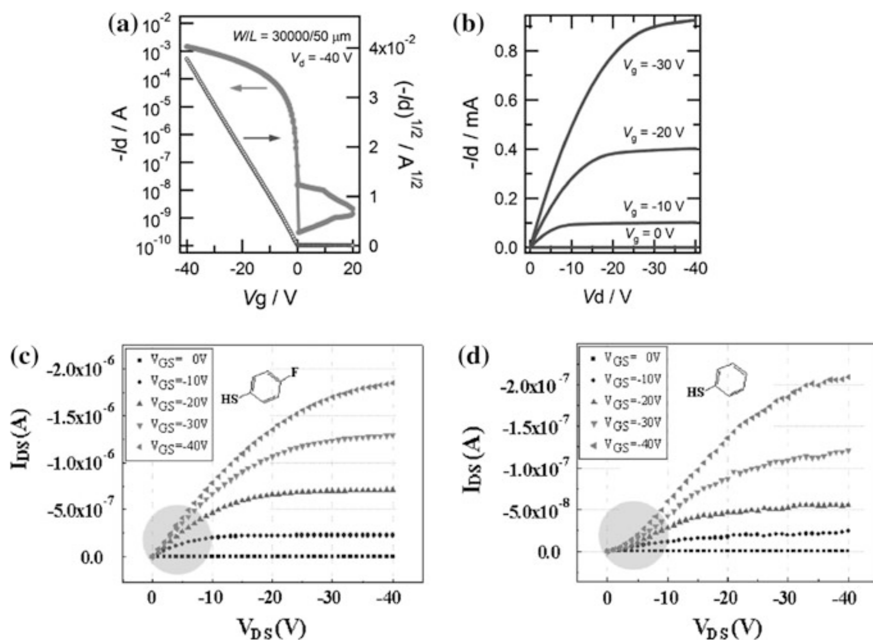


Fig. 10.23 **a** Transfer characteristics, and **b** output characteristics of a Ph-PXX TFT (Reprinted with permission from [79]. Copyright (2009) American Chemical Society). Output characteristics of TIPS-pentacene TFTs, with Ag S/D contacts covered with different thiophenol-based SAMs, showing **c** good, and **d** poor injecting contacts. (Reprinted with permission from [114]. Copyright (2008) American Institute of Physics)

Table 10.1 summarises the parameter values which have been extracted from a number of TFT materials discussed in the preceding sections. The mobility values and on:off current ratios are usually quoted in publications as simple figures of merit, and, where available, the threshold voltage, V_T, and sub-threshold slope, S, values have also been listed. However, these latter parameter values scale inversely with the gate dielectric capacitance, and this needs to be taken into account when comparing V_T and S values between different samples. Unfortunately, the dielectric film thicknesses were not always published, so it is difficult to identify meaningful differences in these parameters across the whole sample set, although the smallest sub-threshold slope of 0.1 V/dec clearly correlates with a very thin gate dielectric of just 5.3 nm [13]. Where the dielectric thicknesses have been quoted, comparisons can be made between the normalised sub-threshold slope values, S_N, in which the measured values have been normalised to a fixed dielectric capacitance of 3.45×10^{-8} Fcm^{-2} (which is equivalent to 100 nm of SiO_2). The smallest S_N value is for the TIPS-pentacene TFT, and is indicative of a lower overall density of trapping states in that material. Comparable, but slightly larger values are seen for the PXX and N3000 TFTs as well, and are also indicative of modest trap state densities, compared with the polymer p-channel materials,

Table 10.1 Summary of basic TFT performance parameters from a range of organic semiconductors

Material	Channel	Gate dielectric	Dielectric thickness (nm)	Mobility (cm^2/Vs)	Threshold voltage (V)	On:off ratio ($\log_{10}$)	S (V/dec)	S_N (V/dec)	Ref #
P3HT	p	SiO_2 + HMDS	230	0.05–0.1	–	>6	1–1.5	0.44–0.65	116
PQT-12	p	SiO_2 + OTS	100	0.14	–	>7	1.5	1.5	21
Pentacene	p	SiO_2 + OTS	–	1.00	−5	7	0.5	–	78
DVAnt	p	SiO_2 + OTS	–	1.30	−16	7	0.5	–	78
TIPS-pentacene	p	SiO_2 + HMDS	370	0.65	3.4	8	0.5	0.14	83
PXX	p	PVP/OTS	400	0.40	–	7	0.6	0.17	4, 79
Pentacene	p	AlO_x + SAM	–	0.50	–	>5	–	–	109
DNTT	p	AlO_x + SAM	5.3	0.60	–	6	0.1	–	13
$F_{16}CuPc$	n	AlO_x + SAM	–	0.01	–	>4	–	–	109
P(NDI2OD-T2)	n	PMMA	600–900	0.2–0.45	5–10	6–7	3–5	0.6–0.4	25
N3000	n	D2000	400–700	3.00	–	7	1.0	0.24–0.14	58

S_N is the normalised value of S, using a fixed dielectric capacitance of 3.45×10^{-8} Fcm^{-2}

P3HT and PQT-12. The other general points to note from this table are that the mobility values for the majority of materials are $\sim$0.4 cm^2/Vs or greater, and that the on:off current ratios are 6–7 orders of magnitude, which are sufficient for active matrix addressing.

Although there is near-universal use of the basic MOSFET equations for the simple extraction of carrier mobility and threshold voltage from OTFTs, a compact model, representing a more accurate description of device behaviour, is needed for circuit simulation [45, 118]. As with the inorganic TFTs (see Sects. 6.3.1 and 9.4.2.2), this needs to take account of non-ideal effects such as series resistance, channel length shortening and the dependence of mobility on gate bias. For example, incorporating the effects of series resistance, and the mobility enhancement factor, γ, from Eq. 10.2, the following dependence of channel current on gate and drain bias has been derived [45]:

$$I_d = \frac{W\mu_0 C_i}{L(\gamma + 2)}\left[(V_G - V_T - V_S)^{\gamma+2} - (V_G - V_T - V_D)^{\gamma+2}\right] \quad (10.5)$$

where V_S and V_D are the channel potentials adjacent to the source and drain contacts, and reflect both series resistance effects plus any voltage drops across the Schottky barrier contacts themselves. Equation 10.5 is similar to the a-Si:H TFT Eq. 6.38, in which the exponent $\gamma + 2$ is replaced by α, and, in both cases, this represents the influence of the band gap DOS in partitioning the gate-induced charge between free and trapped states. The evaluation of γ, V_S and V_D from experimental OTFT characteristics, and the good fit of the model to the data, is presented in Ref. [118].

10.5.2 Contact Effects

The source and drain metal contacts frequently have a voltage offset between the energy level of their work function and the HOMO (p-channel) or the LUMO (n-channel) levels of the semiconductor channel material. As discussed in Sect. 10.2.4, due to the presence of surface dipole layers, these offsets are often different from expectations based upon the published values of the work functions of clean metals [41]. The source junction is effectively a reverse biased Schottky barrier, and, if the barrier height is too large, severe injection problems will result. For a given choice of semiconductor and dielectric materials, if this injection barrier is too high it can dominate device performance, particularly as channel length reduces [117, 120, 121]. The contact effect may be characterised in terms of an effective series resistance, and channel width-normalised series resistance values spanning the range 10 kΩcm–10 MΩcm have been reported [117]. (To put these values into context, performance artefacts have been noted in poly-Si, AOS and a-Si:H TFTs with series resistance values of 3 Ωcm, 30–250 Ωcm, and 7.8 kΩcm, respectively—for further information on these values see Sects. 8.7.1,

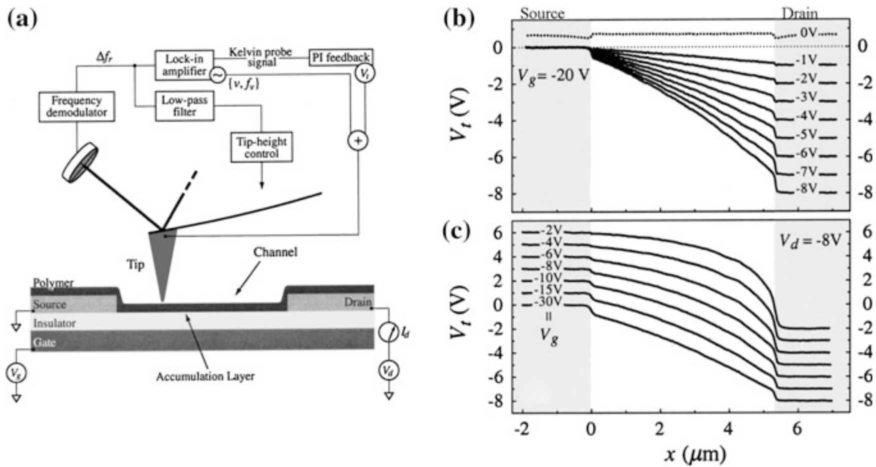


Fig. 10.24 SKPM potentiometry measurements (**a**) measurement setup using an AFM probe head. Surface potential measurements on a P3HT TFT with Au contacts (**b**) in the linear regime with different drain biases, at a fixed gate bias, and **c** different gate biases at a fixed drain bias. (Reprinted with permission from [119]. Copyright (2002) American Institute of Physics)

9.4.1 and 6.3.1, respectively). In view of the large values observed in OTFTs, considerable attention has been paid to the choice of contact materials, and to the evaluation of the injection barriers. This has been by direct barrier measurement in operating TFT structures, using scanning Kelvin probe microscopy [119], as well as by UV photo-electron spectroscopy measurements of dipole layer effects in simpler test structures [24, 38, 39]. These measurements are key contributors to the detailed understanding of the observed series resistance effects in OTFTs. In these studies, several issues were addressed, namely the effect of dipole layers on barrier heights, the injection process at the source [40] and how this translates into a measured resistance, and the influence of device architecture (TC vs BC) on the total series resistance. For instance, in the TC structure, there is vertical current flow through the body of the semiconductor, whilst in BC structures the current injection may be limited to the edge of the source contact adjacent to the channel. An overview of investigations into contact and parasitic resistance effects in OTFTs is presented below.

Non-contact, scanning Kelvin probe microscopy, SKPM, which is based upon the use of a scanning force microscope, has been used to measure the semiconductor voltage along the surface of an operating BG/BC TFT [119], and 2-D device simulations confirmed that the surface potential closely followed the channel potential [122]. The experimental set-up is shown in Fig. 10.24a, and the voltage on the conducting tip of the probe is proportional to the channel potential. Figures 10.24b, c show the potential measurements made along the surface of a P3HT TFT with gold contacts and 5.2 μm channel length [119]. In the first case, with a gate voltage of −20 V, the device continued to operate in the linear regime

as drain bias increased from −1 to −8 V, and in (c) the device went from the saturation regime to the linear regime when the gate bias increased from −2 to −30 V, with a fixed drain bias of −8 V. These profiles confirmed the applicability of the simple, first order MOSFET model, with good linear potential drops along the channel in the linear regime, and a progressive transfer of voltage to the drain end of the channel as the device moved into saturation. The steep voltage drops, ΔV, at either end of the channel in the linear regime were due to the contact resistances, R_c, which can be simply evaluated as $\Delta V/I_d$, where I_d is the channel current. In this sample, ΔV was the same at both ends of the channel, and the total series resistance was 50 kΩcm. As will be seen below, the situation in which $\Delta V_s = \Delta V_d$ is indicative of a low injection barrier, and there are many examples in which the inappropriate choice of contact metal led to significantly larger values of ΔV_s at the source end of the channel. In other measurements, the voltage drop at the drain was not observed [123], and 2-D simulations have demonstrated that this voltage drop can be associated with low mobility, disordered material adjacent to the contacts [124]. The disorder had the effect of restricting current flow at the vertical edges of the contacts, and forcing it along the horizontal surface of the contacts, where the carrier density was much lower than in the channel.

The field effect mobility, and its field dependence, was also extracted from the potential profiles using:

$$I_d = W\mu_{FE}(V_G, V(x))C_i[V_G - V(x)]dV(x)/dx \tag{10.6}$$

The SKPM procedure has been applied to a variety of materials and contact metals, including P3HT [117, 119], F8T2 [117] and pentacene [123]. Figures 10.25a, b show further measurements on P3HT with Cr-Au contacts (where Cr was used as an adhesion layer on the SiO_2 gate dielectric) and Cr contacts, respectively [117]. These measurements were made in the linear regime at $V_G = -40$ V and $V_d =$
−8 V, and the Au contact results, in Fig. 10.25a, were consistent with the comparable measurements in Fig. 10.24b, c. In particular, the values of ΔV_s and ΔV_d were very similar, whilst, for the Cr contact, $\Delta V_s > \Delta V_d$, and this was taken to be indicative of a substantial injection barrier at the Cr source contact. The value of ΔV_s at the source end of the channel is a direct measure of the reverse bias developed across the Cr Schottky barrier contact at the source, and it reduces both the effective gate-source and source-drain biases to $V_G - \Delta V_s$, and $V_d - \Delta V_s$, respectively. The consequence of this is a self-consistent reduction in channel current, for the given terminal biases V_G and V_d, as is required for current continuity through the large source barrier and the channel.

Taking the ionisation potential, IP, of P3HT to be 5.0 eV, the difference in injection barriers in Fig. 10.25a, b correlated with the different work functions, Φ_M, of Au (5.2 eV) and Cr (4.7 eV). (In this work, the dipole barrier was not measured, but it was assumed that the usual reduction in effective work function would be comparable for Au and Cr, and that Au would, therefore, give the smaller injection barrier [117], whilst the barrier would be >0.3 eV with Cr). From the values of ΔV_s

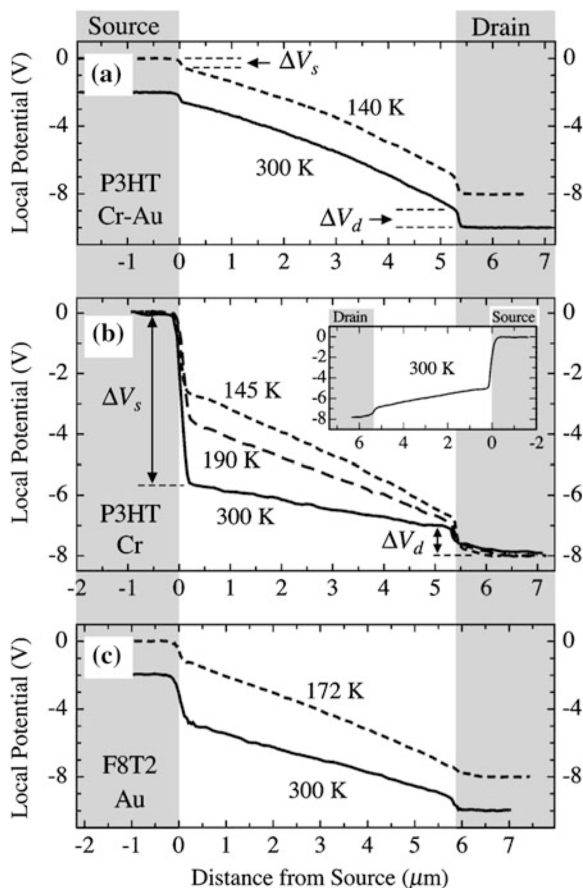


Fig. 10.25 SKPM measurements on P3HT and F8T2 TFTs with Au or Cr contact metals **a** P3HT with Cr-Au, **b** P3HT with Cr, and **c** F8T2 with Au. (Reprinted with permission from [117]. Copyright (2003) American Institute of Physics)

and ΔV_d, the total series resistance was estimated to be 5400 kΩcm for Cr and 22 kΩcm for Au. The more usual way of determining series resistance is from the channel length dependence of the drain current at fixed gate voltages, and the SPKM measurements agreed well with those measurements [117]. (For further information on the conventional series resistance measurement, the background to it was presented in Sect. 9.4.1). Finally, the difference in injection barriers identified by SKPM correlated with low-voltage current crowding in the output characteristics of the TFTs with Cr contacts, whilst it was absent with the Au contacts.

Figure 10.25c shows SKPM measurements on an F8T2 TFT with Au contacts. In contrast to the measurements of P3HT TFTs with Au contacts, F8T2, which has an IP of 5.5 eV, displayed a substantial injection barrier at the source contact, which correlated with a value of $\Phi_M - IP > 0.3$ eV [117].

Carrier flow over the barrier is often assumed to be due to thermionic emission in 2-D modelling work on OTFTs [121], but analysis of the temperature dependence of both the barrier height and the carrier mobility argued against this simple model, and favoured a thermally assisted tunnelling process [117].

As is apparent from Fig. 10.25, the forward-biased drain junction was not found to present a significant barrier to current flow in any sample. However, the small barrier at this junction did represent an element of series resistance, which was also present at the source of the Cr-Au P3HT TFT. This resistance was found to scale inversely with the carrier mobility of the material, and was attributed to carrier flow through a narrow depletion region at the edge of the drain junction. This was also assumed to be the case at the source junction in the Cr-Au P3HT TFT, where the injection barrier was estimated to be close to zero [117].

The above results were for polymer semiconductors, and broadly similar effects have been seen with pentacene TFTs. For example, measurements of SKPM and of the output characteristic of BC TFTs, with the dual-metal contacts of Pd and Pt, gave the results shown in Fig. 10.26a, b, respectively [123]. The SKPM measurement showed a near-zero injection barrier when Pt was used as the source contact (and Pd as the drain), but a substantially larger one with the contacts reversed, with Pd as the source. This correlated with the greater current crowding in the output characteristics when Pd was used as the source contact. Whilst the dipole layers on the metals were not directly measured, the injection barrier differences were consistent with the different work functions of $\sim$5.8 and 5.1 eV for Pt and Pd, respectively [41]. However, in measurements of TFTs with Pd and Ni dual-metal contacts, which have similar work functions, the use of Ni as the source contact showed a much larger injection barrier than Pd, and also worse current crowding. This was attributed to oxidation of the Ni surface during UV-ozone cleaning of the substrates prior to the pentacene deposition. The dipole layers were not measured on these samples, but these results indicate the varying sensitivities of different metal surfaces to chemical exposure, as has also been reported for Au [24]. The contact resistance values were directly evaluated from measurements of the channel length dependence of the total device resistance, as a function of gate bias, in Pd-contacted TFTs [121]. These characteristics were de-convolved (as discussed in Sect. 9.4.1) to separate the channel and parasitic resistances, and are shown in Fig. 10.26c. The resistance curves demonstrate that the parasitic resistance was comparable to, and about 3 times less than, the channel resistances in 10 μm and 30 μm channel length TFTs, respectively. Hence, the injection barrier associated with the Pd contacts had an increasing impact upon the operation of TFTs as the channel length reduced from 30 μm, and the series resistance associated with Au contacts was even higher in this work [121]. The width normalised contact resistances at $V_G = -20$ V were 6.9 kΩcm and 51 kΩcm for Pd and Au, respectively.

It is apparent from these results that the contact resistance in OTFTs consists of two separate elements: a carrier transport resistance between the channel and the source and drain contacts (which is comparable at both contacts), and, secondly, where there is a large offset between the carrier band (HOMO or LUMO) and the metal work function, an injection barrier resistance at the source electrode, which can exceed the transport resistance. Hence, the overall series resistance is sensitive to the choice of metal, and its chemical exposure, and to the choice of semiconductor, particularly its carrier mobility. In addition, the resistance is also affected by the use of SAM layers in BC TFTs to improve the molecular organisation of the

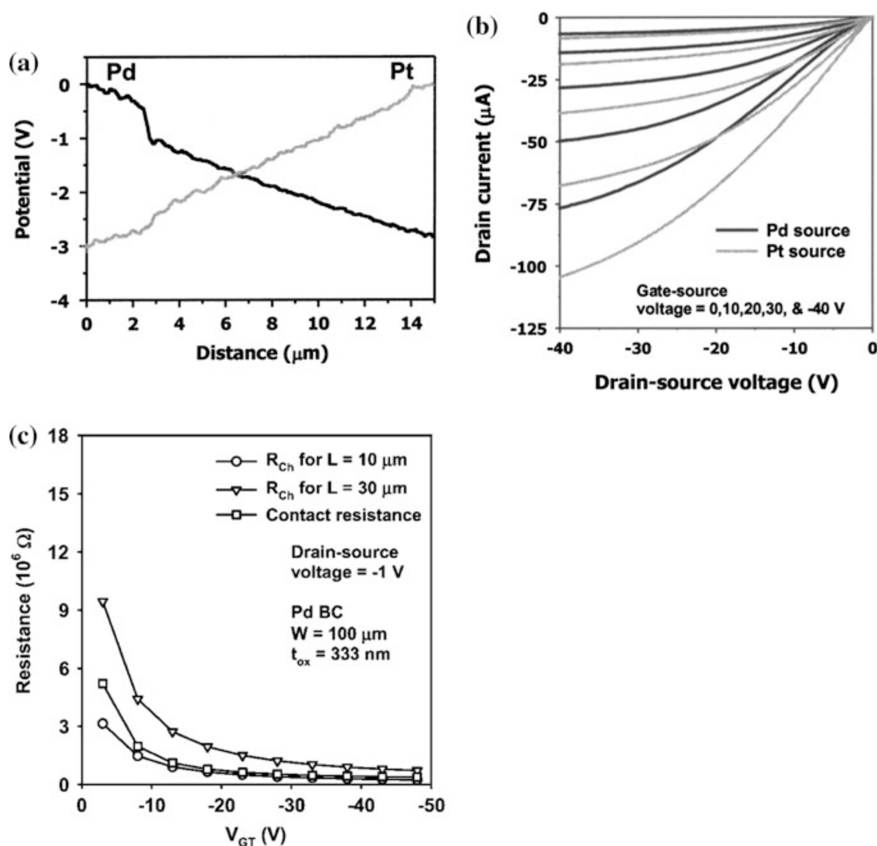


Fig. 10.26 Measurements of pentacene TFTs with reversible Pt and Pd dual-metal source/drain contacts. **a** SKPM measurements. **b** output characteristics (Reprinted with permission from [123]. Copyright (2003) American Institute of Physics). **c** Channel and series resistance values as function of V_G on Pd-contacted BG/BC pentacene TFTs. (Reprinted with permission from [121]. Copyright (2006) American Institute of Physics)

semiconductor material on the electrode itself. Improved understanding and optimisation of contact resistance is an on-going activity [40, 122, 125], and is essential for the meaningful reduction of channel length, L, in order to improve OTFT circuit speed. Indeed, speed will only scale as $1/L^2$, when the series resistance is significantly less than channel resistance.

10.5.3 Contact Architecture

Given the importance of the contact effects discussed in the preceding section, there has been much interest in whether top or bottom contact devices display different

contact limitations in their performance. For instance, with staggered BG/TC (or TG/BC) devices there is a requirement for vertical current flow through the bulk of the device, from the channel to the contacts, which is film thickness dependent [53, 126]. On the other hand, there is more opportunity in the staggered device for the channel current to be distributed along the width of the contacts, due to the overlap of the gate and contact electrodes [126], whereas, in a coplanar BG/BC structure, the current flow is limited to the contact electrode edges.

So far as TFT measurements are concerned, there are varied reports on the relative values of contact resistance in BG/BC and BG/TC TFTs. For pentacene with Au contacts, in some studies the BC TFTs were observed to have the higher contact resistance [121, 127]. In other work, whilst the lowest resistance was found with 20 nm thick pentacene films in TC structures, the resistance in the TC structures increased with film thickness, and lower contact resistance was found in the BC TFTs with 40-80 nm thick pentacene films [53]. For Pd-contacted pentacene films, the contact resistance was lowest in BC structures at low gate bias, and it then became lower in TC devices as the gate bias increased [128]. These different experimental results are no doubt related to subtle differences in device technology and processing.

A more fundamental investigation of contact effects can be obtained from 2-D device simulation, and, in these studies, TC devices have been consistently found to have lower values of contact resistance, and better performance, than BC structures [121, 122, 129]. This has been partially explained by the carrier tail from the channel extending into the substrate, and reducing the bulk resistance, and also by the spreading of the carriers along the contacts themselves. An example of the computed difference between TC and BC structures is shown in Fig. 10.27, in which the output characteristics were calculated for three different injection barrier heights of 0, 0.2 and 0.3 eV [121]. For the 0 eV barrier, the two sets of curves were identical, indicating that, in these calculations, the differences in transport resistance were negligible between the two architectures. However, as the barrier height increased, the device operation was modulated by the size of the injection barrier, and this effect was far greater in the BC TFT. In explaining these, and

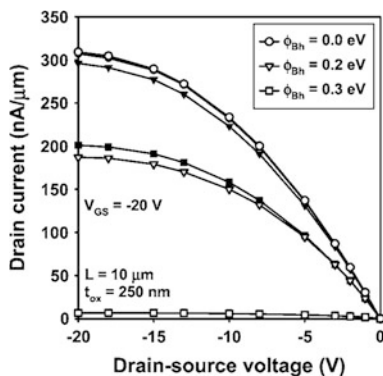


Fig. 10.27 2-D simulation of TC (filled symbols) and BC (open symbols) TFTs, with source injection barriers of 0.0, 0.2, and 0.3 eV. (Reprinted with permission from [121]. Copyright (2006) American Institute of Physics)

other TC simulations, one topic which was not reported was the capacitive coupling of the gate to the Schottky barrier source contact, and the influence of the gate bias on the injection barrier height at the TC. It has also been noted that injection barriers of <0.3 eV are needed for the efficient operation of OLEDs, whereas the operation of OTFTs seems to be tolerant of apparently much larger barriers [131]. An obvious difference between the OLED and the TFT structures is the presence of the gate in the latter, and, in subsequent work [130–132], there has been increasing recognition of the role of the gate bias in modulating the height of the reverse biased source barrier.

In one case [130], dealing with poly-crystalline material in staggered OTFTs, it was reported that the hole accumulation layer, induced by the gate bias, increased the field at the source and lowered the source barrier by the Schottky effect [133]. In another publication [131], 2-D simulation was used to compare gate-bias-induced barrier lowering in coplanar and staggered TFTs. In the coplanar TFTs, the direct Schottky effect was identified between the edge of the source contact and the adjacent hole accumulation layer, with a continuous reduction in barrier height with increased gate bias. The Schottky effect was also invoked for the staggered structure, but it was shown that the effect saturated at large gate biases. The saturation was attributed to the hole accumulation layer, on the opposite side of the film from the source, screening the source contact from further increases in the gate-induced space charge field. However, these evaluations were carried out at low values of reverse bias on the source, and did not allow for the increased field at the source once its reverse bias was increased, and started to deplete the hole accumulation layer [134]. Indeed, in a comprehensive 2-D numerical analysis of staggered OTFTs, it was shown that the field at the source was due to the combination of both the gate bias and the source reverse bias, and that gate bias alone (at low values of V_D) had only a very small impact upon the source barrier height [132]. This work demonstrated significant barrier lowering at the source contact due to the combined effects of the gate and source biases. Whilst these papers have identified the involvement of the gate in barrier height control in OTFTs, there is presently not a consensus on the precise details, and further analysis can be anticipated on the broad topic of gate-bias-controlled series resistance effects in OTFTs.

In this context, it is worth mentioning a novel form of TFT, called the Source-Gated Transistor, SGT, which has both a BG/TC structure, and a Schottky barrier source. In the SGT, it is argued that, in saturation, the height of the reverse biased source barrier is controlled by the electrostatic coupling of the gate potential, and this determines the source-drain current in injection-limited structures [134–136]. Moreover, 2-D simulations of these structures have indicated that they can enhance the performance of low mobility organic materials compared with their use in conventional TFTs [136]. The physics of SGT operation is presented in Chap. 12, where the current understanding of SGT behaviour is compared with recent analyses of source barrier effects in OTFTs.

10.6 Instability Effects

A variety of instability effects have been observed in OTFTs, and, to a certain extent, these reflect the different materials, transistor designs, and preparation techniques used with these devices [137]. Nevertheless, it is possible to define some of the more common and representative instabilities, including ambient instability, hysteresis during sample measurement, and longer-term bias stress instability. It should be noted that the specific details are likely to be a function of the particular organic semiconductor, its gate dielectric, and the conditions under which the instability is assessed. For instance, depending upon the materials, the ambient has been found to have an important effect, as demonstrated by differences observed between devices measured in vacuum, dry gases, air, and high humidity environments.

10.6.1 Air-Instability

Air-instability is related to the material's sensitivity to the presence of oxygen and water, which are able to diffuse through many semiconductor materials, and to cause an oxidising reaction. Oxidation is a process involving electron transfer from the host material to the oxidant [18], and the more tightly bound the electrons are in the host, the lower its susceptibility to this process. Hence, for a p-channel organic semiconductor, the greater its ionisation potential (or HOMO level), the more air-stable it should be. The same argument applies with respect to the LUMO level of a semiconductor under electron accumulation (i.e. for an n-channel device in the on-state), and the deeper the LUMO level is the more air-stable it should be.

As mentioned in Sect. 10.4.2, the air-instability effect most commonly observed was a reduction in carrier mobility, due to trap creation by the oxidation reactions, but changes in threshold voltage and off-current have been noted as well [76]. Amongst the more widely studied p-channel TFT materials, pentacene and P3HT were shown to be affected by air exposure, and more stable materials, such as DNTT [13], DVAnt [78], have been developed with deeper HOMO levels. An alternative approach was to change the molecular structure, such as with Ph-PXX [4, 79], in which substituents were added to the periphery of the molecule to passivate reactive sites, and thereby reduce its sensitivity to oxygen. A comparison of the air stability of pentacene and Ph-PXX is shown in Fig. 10.28a, and illustrates the much better ambient stability of Ph-PXX. Similarly, PQT-12 has a modified molecular structure compared with P3HT, which improved its oxidative stability, even though its HOMO was only 0.1 eV deeper [21].

Early n-channel materials, which were used in TFTs were made on SiO_2 gate dielectrics, were very sensitive to oxidation by silanols on the insulator surface. This reaction resulted in the formation of electron traps, which suppressed electron conduction, and also precluded ambipolar behaviour in good p-channel materials

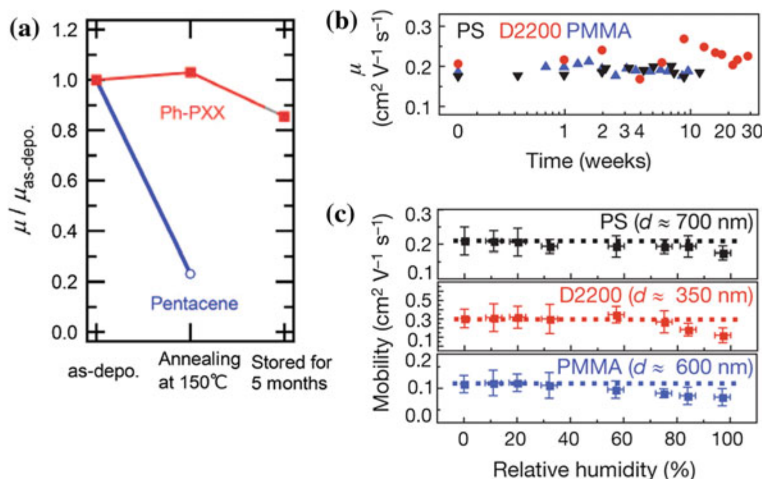


Fig. 10.28 **a** Comparison of the air-stability of pentacene and Ph-PXX TFTs (Reprinted with permission from [79]. Copyright (2009) American Chemical Society). Stability of electron mobility in n-channel P(NDI2OD-T2) TFTs with different gate dielectrics {PMMA, PS (polystyrene), and commercial D2200 (polyolefin-polyacrylate)}: **b** During ambient storage at relative humidity levels of 20–60 %, and **c** after 24 h storage at different humidity levels. (Reprinted by permission from Macmillan Publishers Ltd: Nature [25], copyright (2009))

[36]. Hydroxyl-free insulators, such as BCB, polyethylene, PMMA and parylene were demonstrated to remove/reduce this electron trapping problem, and gave good n-channel behaviour [36]. However, n-channel materials were still sensitive to air-degradation, due to the diffusion of oxygen and water through the film, and it was predicted that the LUMO level had to be deeper than ~4 eV to suppress the oxidation reaction [92]. Good air-stability was subsequently demonstrated with the n-channel materials $F_{16}CuPc$ [93], and FPTBBT [94], having LUMO levels of 4.8 eV and 5.05 eV, respectively. An alternative approach was to use a dense molecular structure to impede the ingress of oxidants, and high performance, air-stable n-channel TFTs were obtained with P(NDI2OD-T2) [25], although its LUMO level was only ~4.0 eV. The excellent air-stability of the electron mobility in P(NDI2OD-T2) TFTs, with different gate dielectrics, is shown in Fig. 10.28b, and these devices also displayed good stability at relative humidity levels up to ~60 %, as seen in Fig. 10.28c [25].

10.6.2 Gate Bias Stress Instability

Given the earlier development of high quality p-channel TFTs, a substantial body of work has been published on the bias-stress instability of these devices. By and large, the most significant instability has been under gate bias stress, with the drain bias having a relatively minor effect (as with a-Si:H TFTs). As bias stress instability is

such a fundamental aspect of device performance, most semiconductor and gate dielectric materials of interest have been routinely evaluated under gate bias stress. The most common instability was an increase in threshold voltage towards the value of the stress bias. In other words, there was a negative shift in threshold voltage with negative gate bias stress, and a positive shift with positive bias stress. This has been particularly true with the SiO_2 gate dielectric, which, in many studies, was deliberately chosen as a highly stable material, in order to focus on the instability within the organic semiconductor itself. However, it should also be noted that some TFTs with organic dielectrics, such as PVP [138, 139], have given the opposite polarity shifts, where the TFT behaviour has been dominated by instabilities within the organic dielectric material.

The typical features of gate bias stress instability include the polarity effect described above, in which the saturated shift in threshold voltage tended towards the value of the gate bias stress voltage. This direction of threshold voltage shift is also equivalent to a reduction in the on-current at a fixed value of gate bias, as can be seen in Fig. 10.29a. This figure shows the time dependent change in the transfer characteristics, due to the application of a gate bias stress of −20 V to a PTAA TFT with a thermally grown SiO_2 gate dielectric [140]. The change, which is characteristic of this type of instability, was initially rapid (and could be observed on a time scale of seconds), but it progressively slowed down, and continued over periods of hours or more. In view of the extensive time scale of the effect, it is frequently represented on a logarithmic time axis, as shown in Fig. 10.29c. Moreover, given the initially fast rate of change, the threshold instability may also be observed as hysteresis in a transfer characteristic between the outward and return gate voltage sweeps. The time dependence can be empirically fitted with a stretched exponential [137, 140–142], as shown by the dashed line in Fig. 10.29c [140]. The trends shown for the PTAA TFT in Fig. 10.29 have also been found in similarly prepared devices containing the following alternative channel materials: pentacene, P3HT, F8T2, PTV (polythienylene-vinylene), and 3-BuT5 (3-butyl-quinquethiophene) [140, 141]. Similar results have also been measured in single crystal rubrene, TIPS-pentacene, and tetracene TFTs on parylene dielectric layers [142].

The stretched exponential fitted to the data in Fig. 10.29c has the form:

$$\Delta V_T = V_0\{1 - \exp -(t/\tau)^{\beta}\} \tag{10.7}$$

where $V_0 \sim V_{Gstress}$, the exponent β was weakly temperature dependent, with a value in the range 0–1, and the characteristic relaxation time, τ, was thermally activated, and given by:

$$\tau = \tau_0 \exp(E_A/kT) \tag{10.8}$$

For the device shown in Fig. 10.29c, which was measured in air at 30 °C, the fitted parameter values were $V_0 = 19$ V, $\beta = 0.43$, $\tau = 10^4$ s, and the activation energy, E_A, was ~0.6 eV [140]. However, when stressing in vacuum, the instability was much slower, with $\tau = 10^6$s, although the other parameters remained much the same. Similar behaviour was seen with the semiconductors pentacene,

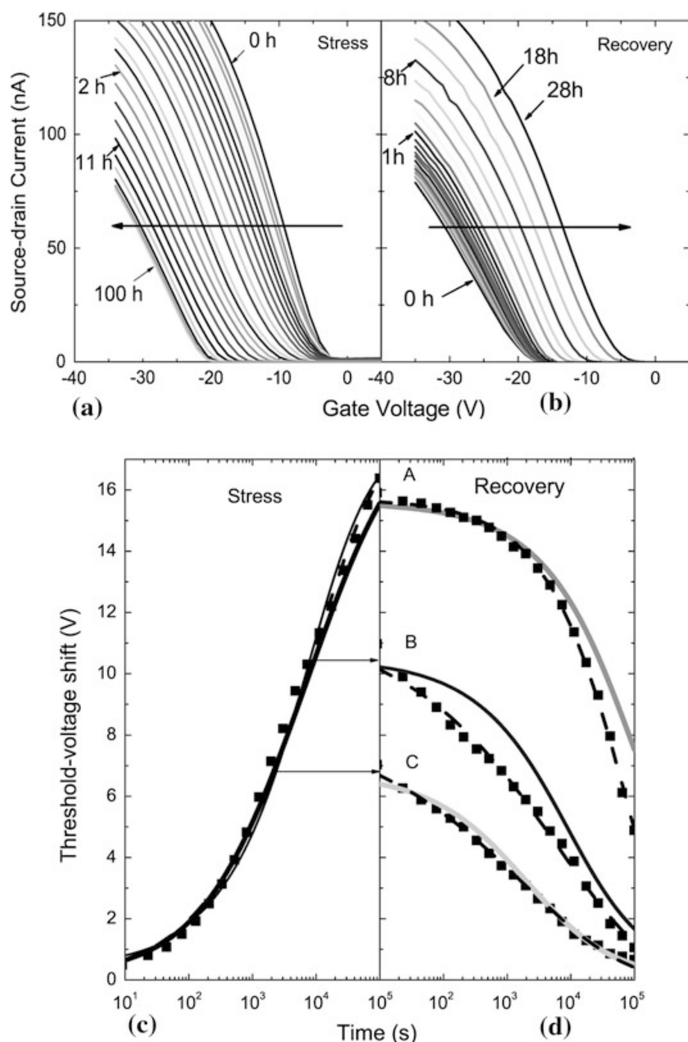


Fig. 10.29 Transfer curves measured on a PTAA TFT as a function of time in air **a** with −20 V gate bias stress, **b** recovery after removal of gate bias, **c** gate bias stress data (*symbols*), and fitted stretched exponential (*dashed line*), and **d** recovery data (*symbols*), and fitted stretched exponential (*dashed line*) (Reprinted with permission from [140]. Copyright (2010) by the American Physical Society)

P3HT, F8T2, PTV, and 3-BuT5, and, in particular, they all had comparable activation energies of ~ 0.6 eV, indicating the same underlying instability mechanism. Where they differed was in the values of their relaxation time, τ, which scaled inversely with the HOMO level of the semiconductor, as shown by the results in Fig. 10.30 (taken at 25 °C, in vacuum) [141]. In this plot, the materials with the deepest HOMO levels were the least stable. A qualitatively

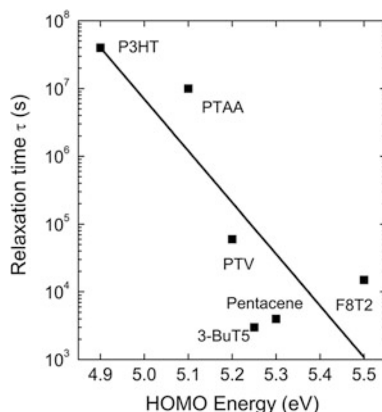


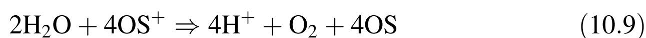
Fig. 10.30 Variation of the characteristic stress relaxation time, τ (at 25 °C in vacuum) with the HOMO level of the semiconductor. (Reprinted with permission from [141]. Copyright (2011) American Institute of Physics)

similar dependence of relaxation time on the HOMO level was also seen with the single crystal samples of rubrene, TIPS-pentacene and tetracene, albeit with a smaller slope than the data in Fig. 10.30 [142], indicating that these broad trends are quite common.

The other common features to the instability process are that it is reversible once the gate bias is removed, as shown in Fig. 10.29b, and that the time dependence could also be fitted with a stretched exponential, as shown by the dashed lines in Fig. 10.29d [140]. There are three sets of recovery data in this figure, which started at different points in the stress cycle (as indicated by the arrows from Fig. 10.29c), and one of the key features of the recovery process was that the fitted recovery time, τ, increased with the duration of the initial stress, t_s. The τ values were 7.7×10^4 s, 6.5×10^3 s, and 2×10^3 s for curves A ($t_s = 10^5$ s), B ($t_s = 10^4$ s), and C ($t_s = 2 \times 10^3$ s), respectively. Hence, the characteristic recovery time was more than 100 times longer for the stress of 10^5 s (curve A) than it was the 2×10^3 s stress (curve C). The correlation between the stress duration and the recovery speed has been reported previously in PQT-12 [143], and, in some cases, authors have noted that full recovery had not been achieved within a given recovery time [142, 143].

The type of gate bias instability seen in Fig. 10.29a has been widely observed, and attributed to carrier trapping either in the semiconductor, in the dielectric or at the interface [137]. However, in interpreting the instability effects in Fig. 10.29, account was taken of the fact that humidity has been found to strongly influence gate bias stability, and, in the cited results, there were large differences in the relaxation times between vacuum and air stressing, and that gate bias instability was greatly reduced with the hydrophobic gate insulator Cytop [140]. This indicated that water played a role in the instability, and the instability was attributed to proton generation from water at the semiconductor/SiO_2 interface, and its subsequent diffusion into the gate dielectric. One of the reasons for proposing proton participation was because its activation energy for diffusion in SiO_2 was 0.5 eV, and this was comparable to the instability activation energy of $\sim$0.6 eV [140,

144]. The detailed microscopic model involved an electrolytic reaction between free holes and water molecules at the semiconductor/SiO_2 interface, which produced protons by:



$$2H_2O + 4OS^+ \Rightarrow 4H^+ + O_2 + 4OS \quad (10.9)$$

and the reverse reaction of protons back to holes:

$$2H^+ + 2OS \Rightarrow H_2 + 2OS^+ \quad (10.10)$$

where OS^+ and OS represent holes and neutral sites in the semiconductor, respectively. Hence, the instability was triggered by the conversion of free holes into protons, and the establishment of equilibrium densities of protons across the interface. This was assumed to be a fast process, and the dynamics of the instability were governed by the diffusion of the protons away from the interface, into the gate oxide. The role played by the individual semiconductor HOMO level was in stimulating the reaction shown in Eq. 10.9, because a free hole density (equivalent to an absence of electrons) in the semiconductor can be regarded as representing the oxidised state of the material, and, the deeper the HOMO is, the less stable the oxidised state, OS^+, is [140, 141]. Hence, this carrier driven instability is the opposite of the ambient instability, in which the most unstable samples are those with the shallowest HOMO levels.

The model also accounted for the recovery behaviour of the material, since removing the gate bias removed the hole accumulation layer, and this disturbed the equilibrium between holes and protons at the interface. The absence of holes stimulated the back reaction at the interface (Eq. 10.10), and produced a reverse diffusion gradient of protons back to the interface. Hence, the longer the bias-stress period, the further the protons had diffused into the oxide, and the longer it took them to return to the interface, where they were neutralised by conversion into holes, and were then swept into the contacts. (The solid lines in Fig. 10.29 were based upon the detailed kinetics of the proton diffusion controlled instability model [140], although the generation of protons has not been confirmed by direct measurements [144]). The conclusion drawn from this work was that water had to be suppressed from the material in order to achieve good bias stress stability.

As mentioned above, the single crystal samples of rubrene, TIPS-pentacene and tetracene displayed qualitatively similar results, but a different microscopic model was advanced. In this model, the holes were captured in a distribution of tail states above the HOMO level in the parylene dielectric, and the deeper the semiconductor HOMO level, the greater the density of tail states available to it in the parylene. Once captured in the tail states of the dielectric, the holes then drifted towards the gate electrode under the influence of the gate field [142]. With the parylene and tetracene HOMO levels at $\sim$7.0, and 6.2 eV, respectively, tetracene showed much faster instability than rubrene, with its shallower HOMO at 4.2 eV. The detailed kinetics of this instability model, based upon the drift of holes in the dielectric, gave a stretched hyperbolic function, which was fitted to the data [142].

There are evidently qualitatively similar gate bias stress results across a range of organic semiconductors, with the semiconductor's HOMO level playing an important role, but no current agreement on a common microscopic model.

Finally, it is worth noting the role of the dielectric layer in qualitatively changing the type of results discussed above. In particular, those instances in which the polarity of the instability has been reversed, whereby a negative gate bias produced a positive threshold voltage shift. This is also related to ambient effects, in that it has been observed for PVP stressed in air [138, 139] and also for PVA [145], but not for PVP stressed in vacuum, where the normal polarity of threshold voltage shift was displayed [139]. The anomalous threshold voltage shift [146] has been variously attributed to electron injection from the gate electrode [138, 145], the movement of ionic impurities, or the polarization of water molecules in the dielectric, given its sensitivity to moisture in the atmosphere [147]. In most of those studies the dielectric was thermally cross-linked, and it was shown that deep UV curing of the material led to more complete cross-linking, and suppressed the instability [146]. For the above two dielectrics, ambient moisture played a role in the bias instability, as was also cited for the proton diffusion model in SiO_2 [140, 141], and better device stability has been reported with a moisture-excluding, hydrophobic dielectric, such as Cytop [148].

In summary, whilst devices with good bias-stability (comparable to a-Si:H TFTs) have been demonstrated [96, 137], there is a complex range of phenomena present in OTFTs, involving both the semiconductor and dielectric materials, as well as their sensitivity to ambient effects. In addition, there are different microscopic models for seemingly similar phenomena, and it is presently unclear whether there are, indeed, quite distinct instability mechanisms taking place in different material combinations.

10.7 Summary

A large number of organic TFT materials now display carrier mobility values approaching, or exceeding, those of the bench-mark TFT for the flat panel display industry, namely a-Si:H. This has stimulated considerable interest in using OTFTs for low cost, flexible substrate applications, such as RFID tags, and e-reader displays. Indeed, many research demonstrator displays have been presented, not just for AMEPDs, but for AMLCDs and AMOLEDs as well.

The current organic semiconductors of choice have been engineered with the appropriate molecular structure and ordering to give efficient charge transport in a TFT structure, and a wide range of both small molecule and polymer materials have been identified. Generally, better performance is obtained from vacuum-deposited small molecule materials, but polymer materials more readily lend themselves to lower-cost, solution processing. However, a range of solution-processable small molecule materials have now also been developed. Initial materials research used oxidised Si as a combined gate electrode and gate

dielectric, but this is not practical for commercial applications, and, in tandem with the semiconductor developments, considerable attention has been paid to alternative dielectrics. These have included both low temperature inorganic dielectrics, as well as a range of organic insulators, and there is continuing research to optimise the use of these materials.

The typical device architecture is a non-self-aligned structure, similar to those used for a-Si:H and amorphous oxide TFTs, although, unlike those technologies, there is not one clearly preferred architecture. Equally, the industry has not identified a particular combination of semiconductor and dielectric layers as optimum, with a range of materials continuing to be used in research demonstrator displays.

As with other TFT materials, OTFTs display various instabilities, including ambient and gate bias stress instability. The ambient instabilities have been addressed both by modifying the molecular structure of the material to reduce its sensitivity to oxygen and water, or by decreasing its permeability to these molecules. Gate bias instability most commonly results in a threshold voltage shift of the same polarity as the stress bias, and, in a number of cases, the instability time constant has been related to the depth of the semiconductor's HOMO level. However, there is not a single, accepted microscopic model for the underlying the instabilities. At a practical level, gate bias instabilities in well engineered structures have been demonstrated to match those of a-Si:H TFTs, and the appearance of a first AMEPD product has been slated for 2012.

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Part III
Novel Substrates and Devices

Chapter 11
TFTs on Flexible Substrates

Abstract The flat panel display industry has been built around TFTs on rigid glass substrates, but there are well-identified applications requiring flexible substrates. This chapter summarises the properties of common plastic substrate materials, and discusses the issues of implementing TFT fabrication schedules on them. It looks in detail at the strategies which have been developed in order to fabricate a-Si:H, poly-Si and organic TFTs on flexible substrates. These have included direct fabrication on the plastic substrates at reduced temperatures, as well as carrier plate and transfer plate processing. For carrier plate processing, the plastic substrates are temporarily bonded to glass carrier plates during processing, and, at its completion, the plastic substrate, plus its TFT layers, are detached from the glass. For the transfer process, the TFT layers themselves are detached from the glass, and bonded to a separate plastic substrate. A third approach has been to use an alternative flexible substrate, which is easier to handle, such as thin foils of stainless steel. In addition to these technological considerations, the mechanics of bending and strain in flexible substrates is summarised.

11.1 Introduction

Chapter 5 has discussed the processing of a-Si:H TFTs on glass substrates, and this is the current, dominant active matrix display technology, irrespective of whether it is for LCD, or electrophoretic e-reader displays. However, there are obvious mechanical limitations in displays made on glass, namely their rigidity and potential fragility. This is particularly true of small portable displays, where mechanical robustness is essential, and, for many of these displays, it is also desirable to minimise their weight and size. The weight reduction may be achieved through the use of thinner, lower density substrates, such as plastic, and the robustness and reduced size can be achieved with increased substrate flexibility, so

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that, for instance, the display may be rolled or folded, when not in use. There are also other applications where the display needs to be conformable to fit, for instance, the contours of a car's dashboard, or to be contoured to be worn on a wrist. These requirements can, in principle, be met with flexible substrates, providing these substrates can be used to make displays, which match the quality of the glass-based displays, and, ideally, at the same or at a reduced cost.

The same arguments can also be applied to poly-Si TFTs, particularly as their major application is in small/medium diagonal portable displays, including both AMLCDs and AMOLEDs, where the need for reduced weight, flexibility and robustness is greatest.

In view of the enormous investment in a-Si:H TFT technology, and its widespread application as the dominant active matrix display technology, it is understandable that there are strong technical and economic reasons to extend this technology, where possible, to new applications. Equally, these arguments can be applied to poly-Si technology, as it currently commands a large fraction of the small diagonal, portable display market. However, as shown in the following sections, the application of the relatively high temperature glass-based processes, to lower temperature plastic substrates, presents many challenges, which are less severe with organic TFTs. Nevertheless, the greater background understanding of the inorganic TFT technologies means that many of today's more sophisticated demonstrator displays and circuits, on flexible substrates, have been made using these devices. Hence, the emphasis in this chapter is on the implementation of these technologies on plastic substrates, with a briefer overview of the work on organic TFTs.

In this chapter, the properties and handling issues of plastic substrates are covered, before looking in detail at the implementation of a-Si:H, poly-Si and organic TFT technologies on flexible substrates. In addition, the impact of substrate flexing on the electrical performance of these TFTs is presented.

To a large extent, the current technological developments have been an extension of the glass-based technology to flexible substrates, and many of the more successful processes have used a hybrid glass/plastic approach in delivering a final plastic-based demonstrator. However, for future low-cost fabrication of flexible devices [1] it is likely that quite different processing technologies will be required, particularly where they can exploit the unique features of flexible substrates, such as roll-to-roll (R2R) processing [1–3]. Whilst aspects of R2R have been demonstrated with a-Si:H TFTs [2], it is better suited to a solution-based organic TFT technology, as this is more compatible with an all-printed process [4]. However, the implementation of an all-printed R2R technology still presents many challenges.

Section 11.2 summarises the properties of the commonly used plastic substrates, and gives an overview of the issues associated with handling them. Section 11.3 discusses the effects of strain on the deposited thin films when the flexible substrate is bent. The strategies for processing a-Si:H, poly-Si and organic TFTs on flexible substrates are described in Sects. 11.4, 11.5, and 11.6, respectively. These sections also summarise the effects of uniaxial strain on the device

characteristics. Finally, the issues of power dissipation in the TFT, leading to its self-heating, and to the subsequent heating of the plastic substrate, are briefly reviewed in Sect. 11.7.

11.2 Substrate Handling

In terms of flexibility and material cost, plastic substrates look very attractive, and have been the subject of considerable research, which has identified and addressed many of the problems involved in shifting from glass to plastic substrates. Some of the issues are related to the differences in thermal and mechanical properties between TFT materials, glass and plastics, and these are summarised in Table 11.1. This table lists key properties of many of the most widely studied plastics, and the corresponding values are also listed for the TFT materials, as well as for glass and steel foil substrates. The plastics are polyimide (PI), aromatic fluorine-containing polyarylates (PAR), polyethersulphone (PES), polyethylene naphthalate (PEN), and polyethylene terephthalate (PET) [5]. The second column lists the maximum processing temperatures for these materials, where the glass transition temperature has been used for the plastics [5], and it will be seen that, for most of the plastics, the maximum permitted processing temperature is well below that for glass substrates. This has the direct consequence that the a-Si :H and poly-Si TFT processing schedules, developed for glass substrates, cannot be directly implemented on plastic substrates, and, therefore, new lower temperature schedules were needed. The two possible exceptions to this are PI and PAR; however, PI is not transparent, and would not be suitable for a back-lit AMLCD display. Nevertheless, it could be used with reflective or emissive displays, and PI substrates are currently used in the development of flexible reflective LC, top-emitting AMOLED and electrophoretic e-reader displays. The issue with PAR is its

Table 11.1 Properties of TFT substrates and layers (*—Glass strain temperature; HS—heat stabilised; many of the figures are illustrative, and will show some variation with substrate preparation technique)

Material	Tmax (°C)	CTE, α (ppm/K)	Y (GPa)	ν	Transparency (%)	WVTR (g.m^{-2}day^{-1})
Glass	666*	3.2	71	0.23	90	0
PI (Kapton)	350	17	2.5	0.32	30–60 (yellow)	
PAR	340	53	2.9		90	
PES	223	54	2.2		90	80
PEN (HS)	150 (200)	13	6.1		>85	2
PET (HS)	80 (150)	15	5.3		>85	9
Steel	>1,000	14	200		0	0
SiN	>1,000	2.7	210	0.25		0
SiO2	>1,000	0.5	70			0
Si	>1,000	2.6	130	0.28		0

coefficient of thermal expansion, CTE, and this general issue is discussed in the next paragraph.

The third column in the table lists the coefficients of thermal expansion, α, and, for the plastics, these are all much larger than the values for glass and for the inorganic TFT materials. Following the deposition of a TFT layer at a temperature ΔT above room temperature, this mismatch between the CTEs of the TFT layers and the plastic substrates will induce room temperature strain, e_M, in the system, given by [6]:

$$e_M = (\alpha_f - \alpha_s)\Delta T \tag{11.1}$$

where the sub-scripts ‘s’ and ‘f’ refer to the parameter values for the substrate and TFT film, respectively.

The strain in the TFT layers is given by [7]:

$$\varepsilon_f = \left(\frac{(\alpha_f - \alpha_s)\Delta T}{Y_f d_f / Y_s d_s + 1} \right) \tag{11.2}$$

(where Y is Young’s modulus, and positive values of ε_f correspond to tensile strain in the film, and negative values to compressive strain). Unless $Y_s d_s \gg Y_f d_f$, the denominator is larger than unity, and the strain in the system is not concentrated just in the TFT film, but is shared with the substrate as well. This is typical for a compliant substrate with a small value of Y_s. So, for the deposition of a thin SiN layer on one side of a plastic substrate, given the CTE differences in Table 11.1, at room temperature the substrate will be constrained from shrinking as much as a free substrate would, and it will be under tensile stress, while the SiN film will be shrunk more than a free film, and it will be under compressive stress. These CTE-induced stresses will cause the structure to distort into a cylindrical shape, with the compressive film on the outer surface of the cylinder. (In contrast, with mechanically induced stress, where the structure is wrapped around a cylinder, the outer surface will be under tension). The detailed relationship between process-induced strain and the radius of the resulting cylinder is discussed further below.

For a rigid substrate, such as glass, with $Y_s d_s > Y_f d_f$, the strain is largely contained within the TFT film, and equation (11.2) reduces to:

$$\varepsilon_f = (\alpha_f - \alpha_s)\Delta T \tag{11.3}$$

The strain in equations (11.2) or (11.3) will have two possible consequences. Firstly, if the strain in the film is too high it will crack, and a rule of thumb, suggesting that the strain should be kept below 0.3 %, can further limit ΔT, and, thereby, limit the maximum processing temperature [8]. This is shown in Fig. 11.1, in which the maximum thickness of silicon nitride, before it cracks, is plotted against the nitride deposition temperature for two engineered, 300 °C plastics having CTE values of 45 ppm/K and < 10 ppm/K. As will be seen, the maximum nitride thickness, at a deposition temperature of 250 °C, was only 200 nm for the nitride on the high CTE substrate [9]. As this may be thinner than

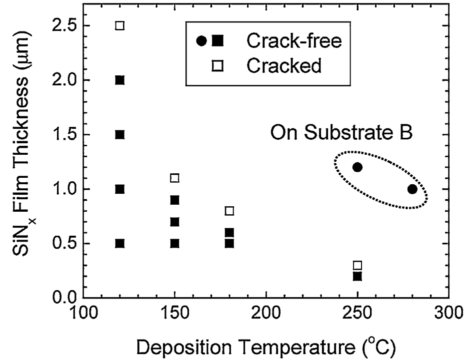

Fig. 11.1 Thickness of cracked (*square*) and crack-free (*filled square*) SiNx films deposited over a range of temperatures on engineered polymer substrates (CTE = 45 ppm/K, and <10 ppm/K for film B). (Reprinted from [9] with permission of SID)

needed for either substrate capping or for the gate insulator layer, the maximum processing temperature must be kept below this temperature if thicker films are required. PAR, with a CTE of 53 ppm/K, will be similarly constrained, and using the rule of thumb of 0.3 % maximum strain, it was recommended that the maximum processing temperature should be kept below 220 °C, which is significantly lower than its glass transition temperature of 340 °C [10].

As mentioned above, with a compliant plastic substrate, having a small Young's modulus compared with the thin film's value, the substrate will buckle into a cylindrical shape, with a radius of curvature, R, given by [6]:

$$R = \left[\frac{d_s}{6(1+v)e_M\kappa\eta}\right]\left[\frac{(1-\kappa\eta^2)^2 + 4\kappa\eta(1+\eta)^2}{1+\eta}\right] \tag{11.4}$$

where, $\eta = {}^{d_f}/_{d_s}$, $\kappa = {}^{Y_f}/_{Y_s}$ and d and Y are the thickness and Young's modulus values, respectively, of the thin film and the substrate, and v is Poisson's ratio (which is assumed to be the same for the film and the substrate). For a rigid substrate, such as glass, where $Y_f \approx Y_s$, and for $\eta < 0.1$, the above equation simplifies to the Stoney formula, giving spherical rather than cylindrical distortion [6]:

$$R = \left[\frac{d_s}{6e_M\kappa\eta}\right] \tag{11.5}$$

The normalised radius of curvature is plotted against the ratio of film thickness to substrate thickness in Fig. 11.2, for the two situations of a compliant substrate ($\kappa = 100$), and a closely matched film and substrate ($\kappa = 1$) [6]. (These two cases were chosen to represent a TFT film on plastic or on a steel substrate, respectively. As will be seen below, the use of thin steel foils is one strategy chosen for the fabrication of TFTs on flexible substrates [6]). Figure 11.2 shows that for a typical case of 1 µm thick TFT layers on 100 µm thick flexible substrates, the plastic substrate develops more than ten times greater curvature than the steel substrate. Also, if the $\kappa = 1$ curve is used as an approximate description of a 1 µm thick TFT

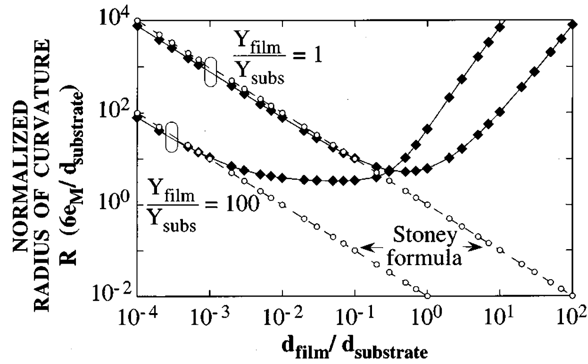

Fig. 11.2 Normalized radius of curvature calculated as a function of the film/substrate thickness ratio, using eqs. (11.4) (solid lines) and (11.5) (broken lines). (Reprinted with permission from [6]. Copyright (1999) American Institute of Physics)

layer on 500 µm thick glass substrate, the curvature of the thinner plastic substrate is ~100 times greater. The curvature in the plastic substrates will need to be handled during processing either by bonding the substrates to a rigid carrier or by using frames to flatten them [10]; either way, this will add extra complication to the processing schedule. Whilst the curvature can be minimised by coating identical capping layers on both sides of the flexible substrate, and, thereby, equalising the surface strains, it will not be practical, nor cost effective, to duplicate all TFT layers on both sides of the substrate. Hence, there will always be CTE-induced bending strain due, for instance, to the SiN_x gate dielectric layer in the TFT. In addition to the unbalanced CTE strains, there may also be residual bending strains in the as-delivered plastic substrates, as well as built-in strain in the films themselves due to the deposition processes [14], all leading to substrate handling issues due to its curvature.

To reduce the CTE mismatch problem, some proprietary, transparent plastic substrates have been developed, in which the CTE values have been engineered to be a closer match to those of the TFT layers, by being less than 10 ppm/K in one case [9], and ~14 ppm/K in another [11]. The first of these substrates also has a maximum processing temperature of ≥300 °C, so that it is also a better match to standard a-Si:H TFT processing schedules [9].

The final column in Table 11.1 lists the water vapour transmission rates, WVTR, in g/m^2/day for the plastic substrates [11], and the high values present another handling issue. This is because water absorption, as well as oxygen absorption, leads to a swelling of the plastic, which compromises its dimensional stability. For photolithography, good dimensional stability is essential for the correct registration of successive mask patterns. In addition, low WVTR values of 10^{-1}–10^{-2} g/m^2/day are needed for LCDs and considerably lower values are needed for encapsulation of AMOLEDs [11]. This problem can be addressed either through impermeable, hard surface coatings deposited by the substrate manufacturer, or by low temperature deposition of SiN_x and/or SiO_2 layers using either sputtering or PECVD. For instance, a PES film coated with a UV-cured acrylate film plus a sputter deposited SiO_x film reduced its WTVR from ~50 to 0.01 g/m^2/day [11]. The coatings also serve to protect the substrates from the potentially

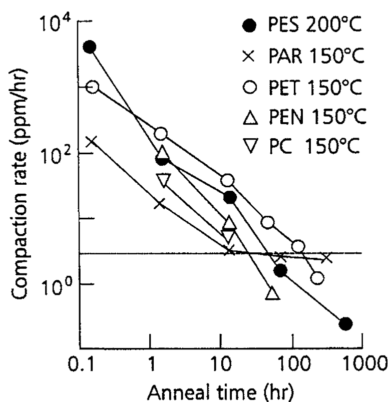

Fig. 11.3 Shrinkage rate measurements of various plastic substrates at 150 or 200 °C. (Reprinted from [12] with permission of SID)

harmful chemicals, which would be used during the device patterning processes. Given the crucial role played by these encapsulation films, they need to be of high quality and pin-hole free.

Finally, the as-delivered plastic films show a tendency to shrink at typical processing temperatures. To maintain dimensional stability throughout the TFT fabrication process, they need to be pre-shrunk, prior to device processing, by annealing them at the intended processing temperature [10, 12]. Shrinkage rate data for many of the common plastics are shown in Fig. 11.3 [12], and this rate parameter can be readily used to match the in-process shrinkage of the film to the required dimensional stability of the substrate. For instance, if a 30 × 30 cm polymer substrate is being processed, and the required alignment tolerance is 3 μm, then the shrinkage of the plate between first and last photolithography stage must be less than 3 μm, or less than 10 ppm. If the total high temperature cycle time after the first lithography stage is 2 h, then the substrate needs to be annealed until its shrinkage rate is <5 ppm/h. From the data in Fig. 11.3, those samples needed to be pre-shrunk for ~10–100 h to achieve this degree of stability.

11.3 Substrate Bending

For displays having an application dependent upon their flexibility, it is important to establish the effect of strain on the performance of the TFT, and, equally, to determine the critical strain at which the device fails. This is usually done by measuring device performance as a function of tensile and compressive strain, by bending the processed substrates around preformed cylinders of defined radius, as shown in Fig. 11.4 [13]. By varying the radius of curvature, R, the strain can be varied, where the relationship between radius and bending-induced strain at the top of the film is given by [6]:

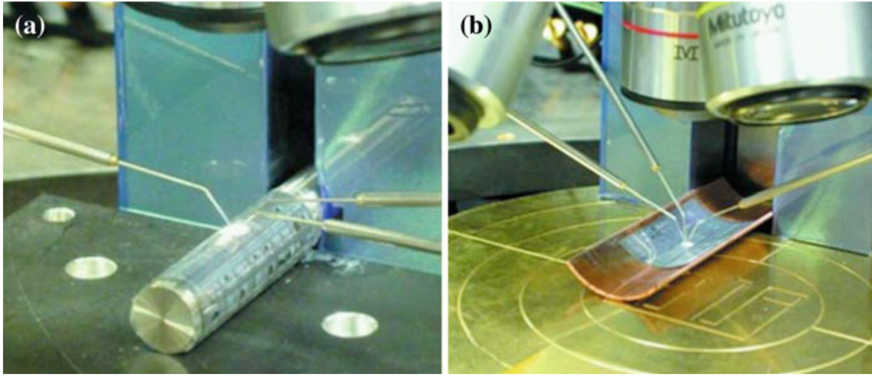

Fig. 11.4 Photographs of steel foils wrapped around cylinders to measure the effects of uniaxial strain on TFT behaviour: (**a**) tensile, and (**b**) compressive strain. (Reprinted with permission from [13]. Copyright (2009) American Institute of Physics)

$$\varepsilon_f = \left(\frac{d_f + d_s}{2R}\right)\left(\frac{1 + 2\eta + \kappa\eta^2}{(1+\eta)(1+\kappa\eta)}\right) \tag{11.6}$$

For externally applied bending strains, if the film is the outer surface of the cylindrical shape it will be under tensile strain.

The normalised surface strain is plotted in Fig. 11.5 as a function of the relative thickness of the film and substrate, for two different ratios of Young's modulus corresponding to well matched elastic properties of the film and substrate ($\kappa = 1$) and compliant ($\kappa = 100$) substrates. For the former, the unity value of the normalised strain corresponds to:

$$\varepsilon_f = \left(\frac{d_f + d_s}{2R}\right) \tag{11.7}$$

and this describes the situation in which the neutral plane is in the centre of the film-substrate bilayer, and the strain in the film increases linearly with the

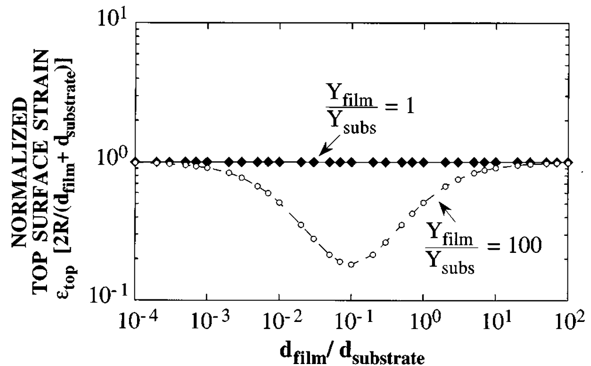

Fig. 11.5 Normalized strain in a film calculated as a function of the film/substrate thickness ratio. Two substrates are illustrated: steel (Yf/Ys $\approx$ 1) and plastic (Yf/Ys $\approx$ 100). (Reprinted with permission from [6]. Copyright (1999) American Institute of Physics)

thickness of both materials, and scales inversely with the radius of curvature. This simple situation, of the neutral plane being in the centre of the bilayer, is only approached with the compliant substrate when there is a gross mismatch in the thickness of the film and the substrate, such that $\eta < 10^{-3}$ or $\eta > 10$, and, in these two cases, one material or the other dominates the bending induced strain. For the more typical case of $\eta \sim 10^{-2}$, the neutral plane moves from the centre of the compliant substrate towards the stiffer TFT film, thereby reducing the strain in the film by approximately a factor of two compared with the $\kappa = 1$ case.

From the mechanical stressing of a-Si:H TFTs into tension and compression, the safe strain range for reversible elastic distortion was established, together with the threshold strain beyond which plastic failure occurred. This is shown in Fig. 11.6 [14], and failure under tensile strain occurred at 0.5 % due to crack propagation, whereas, under compressive strain, the failure mode was buckling and de-lamination at the higher strain of 2 %. The failure under tension has been attributed to the propagation of a crack originating at a flaw, where the propagation occurs when the driving force, G, is greater than the surface energy, Γ, of the newly formed crack [15]:

$$G = \beta \frac{(1 - v_f^2)\sigma_f^2 d_f}{Y_f} > \Gamma \tag{11.8}$$

σ_f is the stress in the film, and β is a dimensionless constant dependent upon the elastic properties of the film and substrate, and, for a compliant substrate, β is much larger than one, leading to easy crack propagation [15]. De-lamination occurs when a defective region at the film/substrate interface results in an unbonded area, which is large enough to permit the film to buckle. Once that happens, the internal stresses can propagate the unbonded area like a crack, and the critical unbonded length for buckling, l_c, is given by [15]:

$$l_c = \frac{\pi d_f}{\sqrt{3(1 - v_f^2)}} \left(-\frac{Y_f}{\sigma_f} \right)^{0.5} \tag{11.9}$$

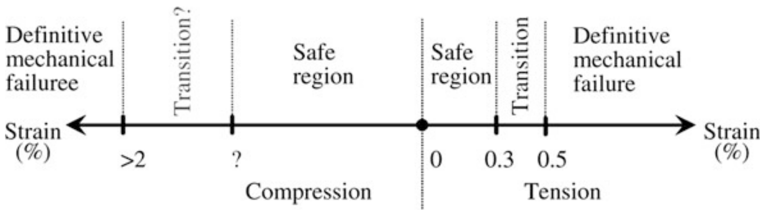

Fig. 11.6 Overview of the response of a-Si:H TFTs to mechanical strain. (Reproduced from [14] with permission of Wiley, Inc)

(where σ_f has a negative value in compression). Given that the compressive failure strain, ε_f, in the film was >2 % [14, 15], the corresponding stress can be determined, giving $l_c < 10d_f \sim 10$ µm. This is an unusually large defective area in a high quality structure, explaining why the films were so stable under compressive strain [15].

Further details of the response of a-Si:H TFTs to mechanical strain are presented in Sect. 11.4.1.1, in which the replacement of the brittle SiN_x by a more resilient hybrid layer of silicon dioxide and silicone polymer (for both substrate capping and the gate dielectric) improved the tensile and compressive failure strains to 5 and 2.5 %, respectively [16].

This discussion has focussed on the direct assessment of strain effects in TFTs on a free-standing polymer substrate. However, in a finished display, the substrate will be attached to another layer to form the display cell. If the elastic properties of this top-plane are a good match to the substrate, the TFT layer would be located near the neutral plane, and would suffer little strain when the whole structure is flexed. Whilst this will be difficult to readily achieve with the inorganic layers used in a-Si:H and poly-Si TFTs, it should be easier to achieve with organic TFTs, and it was shown that the minimum bending radius for pentacene TFTs on PI could be reduced from 5 mm, for the uncoated substrate, to 0.5 mm when it was coated with a thickness-matched parylene capping layer [17].

11.4 a-Si:H TFTs on Flexible Substrates

11.4.1 a-Si:H Fabrication Processes

Given the above discussion on the issues of using and handling the compliant plastic substrates for TFT fabrication, three different strategies have emerged to deal with these problems. The first has been to take the constraints imposed by the plastic substrates, and to develop both lower temperature TFT processing, and substrate handling procedures, in order to implement direct fabrication techniques on these substrates. The second approach is to use an alternative flexible substrate to circumvent the issues with handling plastic substrates, and the material of choice has been polished steel foils. The third strategy has been to maintain as much as possible of the well-established processing techniques used with glass substrates, and, to minimise the handling issues of plastic substrates by bonding them to glass carrier plates during processing, and then separating them from these plates at the end of processing. These three approaches are discussed in the following three sub-sections, and an embryonic, but more innovative, roll-to-roll technology is presented in Sect. 11.4.1.4.

11.4.1.1 Direct Processing on Plastic

In the direct fabrication of a-Si:H TFTs on plastic substrates, the major objectives have been stress control in the films (where the stress arises from both CTE mismatch, as well as intrinsic stress within the film), and optimisation of device performance at the reduced deposition temperatures needed when using the low temperature substrates, such as PES or PEN.

These objectives have been met by modifying the deposition procedures for the a-Si:H and the SiN_x layers. Figure 11.7 shows the variation of strain in SiN_x layers deposited at 150 °C onto 50 µm thick Kapton PI substrates, as a function of deposition power density [18]. In this diagram, the total strain in the film, ε_M, has been split into its constituent components due to CTE mismatch, ε_{th}, intrinsic deposition strain, ε_0, and humidity strain, ε_{ch}. As might be expected, only the intrinsic strain varied with deposition power, and it could be changed from tensile to compressive. Hence, by suitably controlling the deposition power density, the strain can be tuned to the processing requirements of the substrate. The deposition power has also been correlated with the gate bias instability in a-Si:H TFTs [19], in which increasing power density led to improved device stability, and the use of this control procedure is discussed below in the context of a specifically optimised process schedule [8].

As stated above, the deposition power used for the SiN_x layer can affect the gate bias stability of the TFT, and, hence, influences the electronic quality of the layer. The other deposition parameter having an influence upon the quality of the SiN_x layer, as well as upon the a-Si:H layer, is the gas dilution of the reactant gases. The deposition gases are SiH_4 for a-Si:H, and SiH_4 plus NH_3 for SiN_x. For a-Si:H, the electronic quality of the film has been correlated with a high ratio of SiH bonds to SiH_2 bonds, and the SiH bond density can be increased by diluting the SiH_4 with hydrogen [20, 21]. This has been explained mechanistically by arguing that the excess hydrogen acts as an etchant during deposition, and preferentially breaks weak Si–Si bonds to form volatile hydrides. As these weak bonds can form defect states, their removal should increase the quality and improve the bias-stress

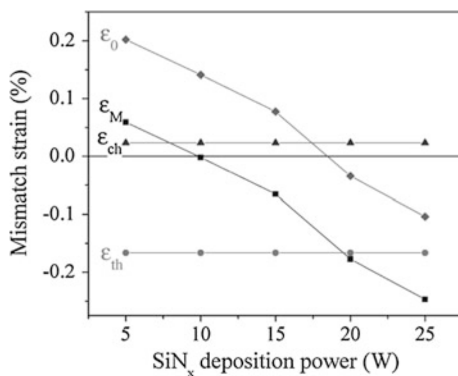

Fig. 11.7 Components of the total mismatch strain, εM, in 300 nm thick PECVD SiNx films deposited at different RF powers onto 50 µm thick Kapton 200E PI substrates at 150 °C. (Reprinted from [18] with permission of SID)

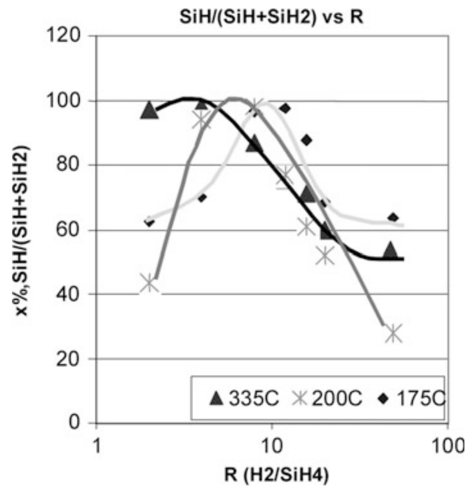

Fig. 11.8 Ratio of SiH:(SiH + SiH2) bond densities in PECVD a-Si:H films, deposited at different temperatures, as a function of the hydrogen dilution of the silane deposition gas. (Reprinted from [21] with permission of SID)

stability of the films [22]. Moreover, as shown by Fig. 11.8, the optimum dilution ratio increased as the deposition temperature reduced [21]; hence, the a-Si:H deposition conditions established for use on glass substrates needed to be re-optimised for use on lower temperature plastic substrates. Similarly, the relative density of NH and SiH bonds needed to be controlled in lower temperature SiN_x films, to prevent the SiN_x becoming either too nitrogen-rich or too silicon-rich, and this was accomplished by dilution of the reactant gases with either hydrogen, helium of argon [21]. An example of this is shown in Fig. 11.9, in which the NH/SiH ratio is plotted as a function of the dilution conditions for the three different carrier gases. Also shown on this figure is the ratio, labelled HT, achieved by conventional SiN_x deposition at 300 °C, and the data point, labelled LT, showing that the ratio was too nitrogen-rich if the same gas composition was used at 200 °C. At this lower temperature, increased gas dilution, with either argon or hydrogen, was needed to restore the film's compositional balance. Suitable

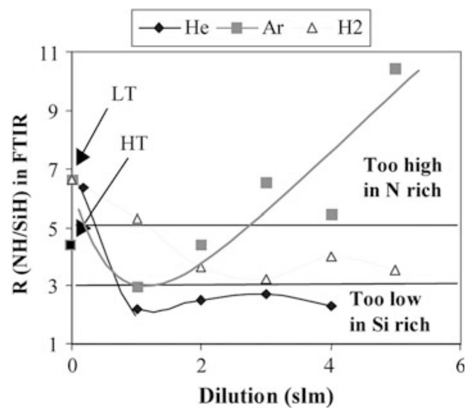

Fig. 11.9 Ratio of NH:SiH bond densities in 200 °C PECVD SiNx films as a function of the dilution of the reactant gases SiH4 and NH3 by He, Ar or H2. (Reprinted from [21] with permission of SID)

dilution ratios were identified for the deposition of the a-Si:H and SiN_x films at 200 °C to produce TFTs with electron mobility, threshold voltage, and gate bias stability comparable to those of the 300 °C control TFTs [21].

In the context of the above background considerations, it is apparent that different groups have selectively used elements of those techniques to minimise strain and to optimise the performance of a-Si:H TFTs on plastic substrates. In many cases, it has been common practice to deposit SiN_x on both sides of the substrate to equalise bending stresses, although the films themselves remained under stress. However, the combined CTE mismatch and intrinsic stresses are greatest in unpatterned films, and can lead to film de-lamination from the substrate [23]. Therefore, one approach has been to pattern the SiN_x gate insulator films into the small areas needed just for the TFTs themselves [23], but this cannot be done to a layer of SiN_x, which is also being used as a barrier film to prevent moisture absorption into the substrate. Hence, a process has been implemented to circumvent these problems [23, 25], by replacing the SiN_x barrier films with 1,200 nm thick layers of a vapour phase polymer consisting of $SiO_xC_yH_x$, and replacing most of the gate dielectric of SiN_x with a 200 nm thick layer of benzocyclobutene, BCB. As the CTE of BCB is 43 ppm/K, it is a good match to that of PES, which was the substrate used in this work. However, to ensure good electronic properties of the a-Si:H TFT, a thin 50 nm layer of SiN_x was retained as the first layer of a conventional triple stack of SiN_x, i a-Si:H (150 nm), and n^+ a-Si:H (50 nm) on top of the thicker BCB gate insulator, and all three layers in the stack were defined down to individual device islands, as shown by Fig. 11.10. The definition of the thin SiN_x gate insulator layer into individual islands led to a significant relaxation of the strain within the structure, as shown by the substrate distortion measurements in Fig. 11.11 [24]. In many respects, the TFT fabrication process was similar to the conventional back-channel-etch process, apart from the extra mask stage needed to define the SiN_x film at the bottom of the triple stack, and the use of aluminium for metal tracks due to its good ductility [25]. In addition, as the PES substrate limited processing temperatures to <220 °C, the SiN_x and a-Si:H depositions at 150 °C had to be optimised to maintain good TFT properties, and this was done by increasing the dilution of the reactant gases with helium [25]. These TFTs fabricated at 150 °C on PES compared well with conventional TFTs

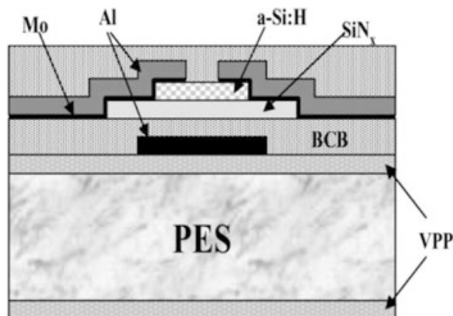

Fig. 11.10 Cross-sectional view of a back-channel-etched a-Si:H TFT with a combined SiNx/BCB gate insulator, within which the SiNx had been locally defined into an island. (Reprinted from [23] with permission of IEEE)

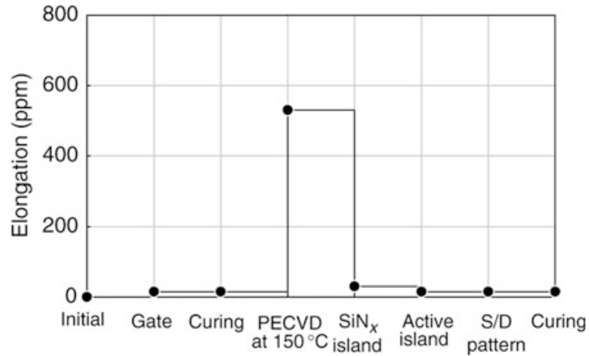

Fig. 11.11 Elongation of the substrate after each process step for an a-Si:H TFT on PES with a combined BCB/SiNx gate insulator. (Reproduced from [24] with permission of Wiley, Inc)

fabricated at 300 °C on glass, and had an electron mobility of 0.4 cm^2/Vs, a threshold voltage of 0.7 V and an insulator leakage current of $<10^{-13}$ A. The transfer characteristics are shown in Fig. 11.12.

Other groups have also looked to replace the stiff SiN_x layers, and Han et al. [16] used a homogeneous hybrid layer of SiO_2 and a silicone polymer, which was deposited at ~23 °C, for both the gate dielectric and for capping the PI substrate. As this hybrid layer was far more compliant than the usual SiN_x layers used for these purposes, the finished devices were less susceptible to cracking under tensile strain, and were able to tolerate ~5 % tensile strain, which was ten times more than the standard SiN_x-based TFTs shown in Fig. 11.6.

An alternative approach has been to use the PECVD deposition power density to engineer the strain throughout the structure, particularly within the SiN_x layers used to coat the clear plastic substrate, whilst deliberately using a high power deposition for the gate insulator SiN_x, in order to maintain good gate bias stress stability in the finished TFTs [8]. Figure 11.13 shows a cross-section of an etch-stop TFT, in which the back-face and top-face layers of SiN_x, used to cap the 75 µm thick plastic substrate, were deposited with compressive stress (at high

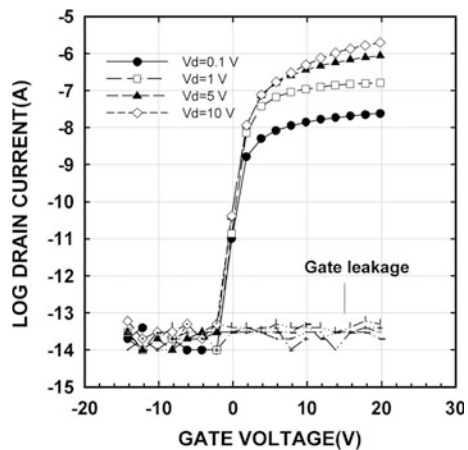

Fig. 11.12 Transfer characteristics of an a-Si:H TFT fabricated on a PES substrate at 150 °C, with a BCB/SiNx gate insulator. (Reprinted from [25] with permission of SID)

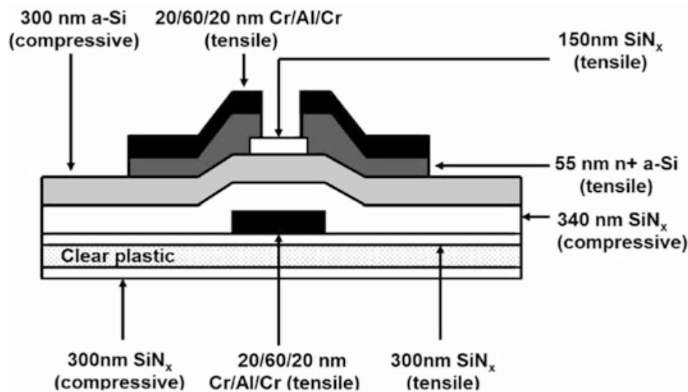

Fig. 11.13 Schematic cross-sectional view of an etch-stop a-Si:H TFT, showing the engineered stresses within each of the layers. (Reprinted from [8] with permission of IEEE)

power density) and tensile stress (at low power density), respectively. In addition, the high power density gate insulator was necessarily deposited with compressive stress, and the etch stop layer, which was deposited at lower power, was under tensile stress (see Fig. 11.7 for the relationship between strain and deposition power). The engineered substrate used for this work had a working temperature of $\geq$300 °C, a CTE of <10 ppm/K, and the depositions were carried out at 280 °C, with the substrate held flat, but not clamped, by a rigid frame. At the end of processing, the samples had a final anneal in air for 30 min [8].

The process delivered high quality TFTs, with an electron mobility of 0.96 cm^2/Vs, a threshold voltage of $\sim$3.5 V and an on/off current ratio of >10^7, which was almost identical to TFTs processed on glass at the same temperature [8]. Of particular concern to the authors was the gate bias instability of these TFTs, as they had previously demonstrated that with reducing deposition temperature there was increased instability. A comparison of the threshold voltage shifts under gate bias stress is shown in Fig. 11.14, for TFT processing at 150, 250 and 300 °C on plastic and glass substrates [8]. Both the a-Si:H and SiN_x films deposited at 150 °C had hydrogen diluted reactant gases, whereas the higher temperature films did not [19]. As expected, the higher deposition temperatures improved device stability, but was not good enough for using these devices as pixel driver TFTs in AMOLEDs [22]. In subsequent work, the authors improved device stability by using 10:1 hydrogen dilution during the a-Si:H deposition to reduce the gate-bias-induced defect generation in the a-Si:H, and further optimised the SiN_x deposition, so that the gate bias stability obtained with 300 °C processing on the low CTE, clear plastic substrate exceeded the industry standard of a-Si:H TFTs on glass [22]. These TFTs had an electron mobility of 0.8–1 cm^2/Vs, a threshold voltage of 1.5–2.5 V, and an off-state current of $\sim 10^{-13}$A, all of which were similar to control devices on glass. Figure 11.15 shows the fractional change in TFT drain current as a function of time, under combined gate (7.5 V) and drain bias (12 V) stress, with the

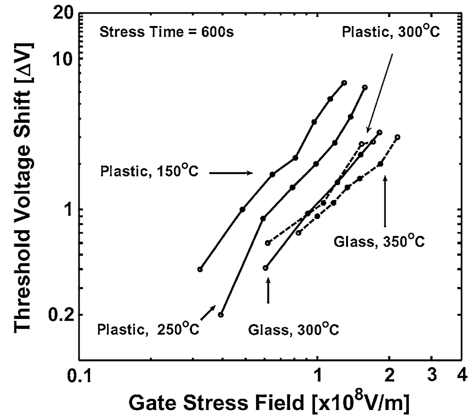

Fig. 11.14 Gate-bias stability measurements on ES a-Si:H TFTs fabricated at different temperatures on glass and plastic substrates. (Reprinted from [8] with permission of IEEE)

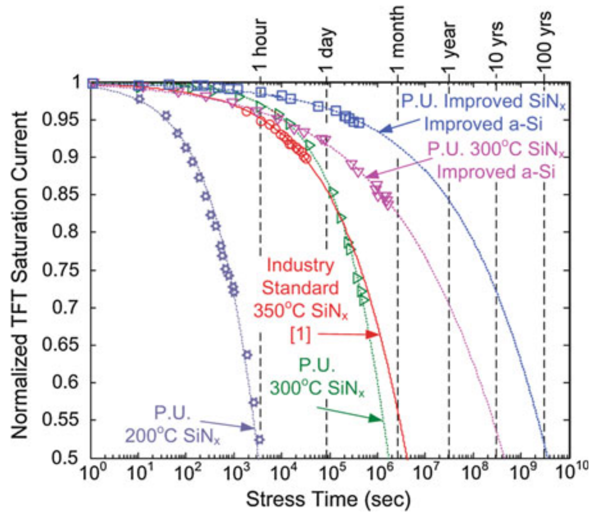

Fig. 11.15 Comparison of bias-stress stability measurements, for different a-Si:H TFT technologies, showing the reduction in normalised saturation current as a function of stress time, after stressing at Vg = 7.5 V and Vd = 12 V. (P.U. is Princeton University). (Reprinted from [22])

improved TFT lifetime exceeding that of the industry standard process, and being suitable for use in AMOLED displays [22].

11.4.1.2 Steel Foil Substrates

Steel substrates have good tolerance to high temperature processing, and, by being impermeable and stiff, they are less susceptible to the dimensional changes induced in plastic substrates by moisture absorption and the deposition of strained TFT layers with a large CTE mismatch. However, the as-delivered steel foil surface can be very rough, with greater than 1 μm peak-to-peak surface roughness reported [26], which needs to be reduced, before device processing, either by

surface polishing and/or by surface planarisation. There is also a need for a thick capping layer on the steel, in order to reduce the capacitive coupling between the TFTs and the conducting substrate [27]. Hence, the surface capping layer has a double purpose, and, in the use of steel foils to investigate pixel design for flexible AMOLEDs, 75 μm thick, 5 cm × 5 cm steel foils were coated with 1.6 μm of a spin-on glass followed by 600 nm of PECVD SiN_x deposited at 280 °C [26]. After deposition and patterning of Cr gates, a conventional triple stack of SiN_x, i a-Si:H, and n^+ a-Si:H was deposited at 280 °C (SiN_x) and 230 °C (a-Si:H). These layers were processed into back-channel-etched TFTs, yielding an electron mobility of 0.5 cm^2/Vs, a threshold voltage of 2 V, and an on:off current ratio of 10^7. The bias stress stability of these TFTs was not specified.

Other work on steel substrates has also sought to make flexible displays, but minimised the handling problems of flexible substrates by temporarily bonding them to rigid carriers during processing [28, 29]. In both cases, the temporary adhesive limited the processing temperature to 180 °C or lower. In one case [28], 100 μm thick steel foils were bonded to rigid carriers, and spin-coated with a 2 μm thick planarising film, followed by 300 nm of SiN_x deposited at 180 °C by PECVD. After Mo gate deposition and patterning, a triple stack of SiN_x (300 nm), i a-Si:H (80 nm) and SiN_x (100 nm) were deposited as the first deposition stage in an etch-stop TFT process. The finished TFTs had an electron mobility of 0.7 cm^2/Vs and a threshold voltage of 1.6 V, but the stability of these low temperature TFTs was not reported.

In the other process [29], 76 μm thick steel foils were attached to a glass carrier plate with a weak adhesive, and chemically polished before planarising them with a 3 μm thick layer of polymer resin, which was then capped with 0.4 μm of 150 °C PECVD SiN_x. The TFTs were processed through a conventional back-etch process, albeit with the PECVD depositions at 150 °C, and the resulting TFTs had an electron mobility of 0.35 cm^2/Vs and a threshold voltage of 1.47 V. Gate bias stressing at 30 V for 1000 s at 60 °C, gave a threshold voltage shift of 2.6 V, which is qualitatively consistent with the conclusions drawn in other work about the increasing degree of gate bias instability as the PECVD deposition temperature is reduced [8]. However, the authors argued that in applying these devices on steel to flexible AMOLEDs, the TFT stability problems could be mitigated by using phosphorescent OLEDs, whose increased efficiency would permit the TFTs to operate at lower values of V_G [29].

11.4.1.3 Carrier Plate Technology

As has been discussed in the preceding two sections, there are considerable problems to be overcome in the direct fabrication of TFTs on flexible substrates, which has included not just the substrate handling issues, but also the impact of reduced deposition temperatures on the bias-stress stability of the TFTs themselves. The handling issues can be minimised if all processing is carried out on the glass substrates familiar to the AMLCD industry, and device performance issues

can also be diminished if conventional processing temperatures are used. One such approach offering all these options is the EPLaR process (electronics on plastic by laser release) [30, 31].

The EPLaR process is implemented on an industry standard glass substrate, but, before processing, a 10 μm thick polyimide film is spun onto the glass and cured at 350 °C to fully polymerise the film. The PI is then coated with a PECVD layer of SiN_x to protect it against the chemicals used in the subsequent TFT process. The cured PI film can withstand processing temperatures up to 350 °C, and can, therefore, be passed through the standard a-Si:H TFT process [30]. At the end of processing, laser exposure, through the back-face of the glass plate, is used to release the PI film, and its TFT layers, from the substrate, yielding an active matrix of TFTs on a flexible plastic substrate. Moreover, as the PI film only increased the weight of the glass substrate by <1 % and its thickness by ~ 1.4 % [31], the standard robotic handling tools used in an a-Si:H TFT production facility can be used with the EPLaR substrates. This means that the EPLaR process can be introduced into a standard line with a minimum of disturbance, which sets it apart from the other technologies discussed in this and the previous sections. However, the use of non-transparent PI, as the final display substrate, prevents its use in transmissive displays, and the current application of EPLaR is for electrophoretic e-reader displays [31]. A cross-section of the back-channel-etched TFTs made with this process, prior to release from the glass substrate, is shown in Fig. 11.16, and an overview of the process flow is shown in Fig. 11.17 [30]. It has been demonstrated that the performance of the TFTs is unaffected by the laser release from the glass carrier substrate, and 9.7 inch electrophoretic displays have been made with this technology [31].

In contrast to the spin-on PI layer used in EPLaR, more conventional plastic substrates have also been used, and bonded to rigid substrates to avoid the problems of directly processing flexible substrates. Where low temperature plastics have been chosen, the maximum processing temperature is still limited by the T_{max}

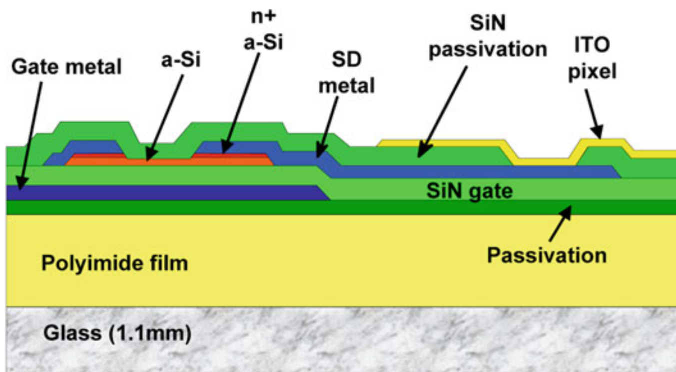

Fig. 11.16 Schematic cross-section of an EPLaR a-Si:H TFT array, shown whilst the PI film is still anchored to the glass substrate. (Reprinted from [30] with permission of SID)

Com. 1	Clean the glass substrate.
EP. 1	Spin-coat a polyimide layer on the glass substrate. Fully cure it and passivate with a thin layer of SiN.
Com. 2	Make a TFT array on the glass substrate.
Com. 3	Cut the glass substrate to form individual displays.
Com. 4	Laminate an electrophoretic foil onto the TFT array.
Com. 5	Attach driver electronics to the glass substrate.
Com. 6	Test the fully working display.
EP 2	Laser release the polyimide from the glass substrate.
Com. 7	Package the display in a display module.

Fig. 11.17 EPLaR process sequence for making flexible electrophoretic displays. (Reprinted from [30] with permission of SID)

of the plastic substrate, or by the temperature at which unacceptable stresses build up in both the films and the adhesive layer during the processing stages [32]. One example of this approach has used pre-shrunk and SiN_x barrier-coated PES [32, 33] and PEN [32, 34] substrates bonded to glass, and processed at 130 and 100 °C, respectively. The bonding, processing and plastic substrate release stages are shown schematically in Fig. 11.18, for both the TFT substrate and a colour filter top-plate on plastic for either an LC display or an electrophoretic e-reader display [35]. For the PES substrate processing, 200 μm thick layers were bonded to glass with an adhesive, which could be released at the end of processing, either thermally or by UV exposure. After bonding, a further SiN_x film was deposited at 130 °C, before the conventional triple stack was deposited, also at 130 °C, for a back-channel-etch TFT process. In order to minimise compressive strain, the layers were deposited at low plasma power [32] (in agreement with other work [8]), and this low power was also found to improve device performance, whereas other work reported that high deposition power was necessary to improve bias stress stability of the SiN_x [8]. The resulting 130 °C TFTs had an electron mobility of 0.5 cm^2/Vs, a leakage current of 10^{-13} A, and an on:off current ratio of 10^7. Gate bias stressing with $V_g = 20$ V and $V_d = 10$ V led to a threshold voltage shift of ~5 V, and ~50 % loss of on-current in 5,000 s, which is comparable to the results presented for 200 °C TFTs in Fig. 11.15. A similar process schedule was used for the 100 °C TFTs on PEN substrates, although the a-Si:H deposition was made at a reduced total gas pressure to improve the device characteristics, and a further anneal at 100 °C was made at the end of processing to reduce the contact resistance of the n^+ layer [32, 34]. These 100 °C TFTs also showed reasonable room temperature characteristics, with an electron mobility of 0.4 cm^2/Vs and an on:off current ration of 10^7. However, bias stress measurements showed a 5 V shift in threshold voltage after 3,960 s, and it is clear that these instability effects need further attention in low temperature TFTs on plastic [32]. However, in spite of the

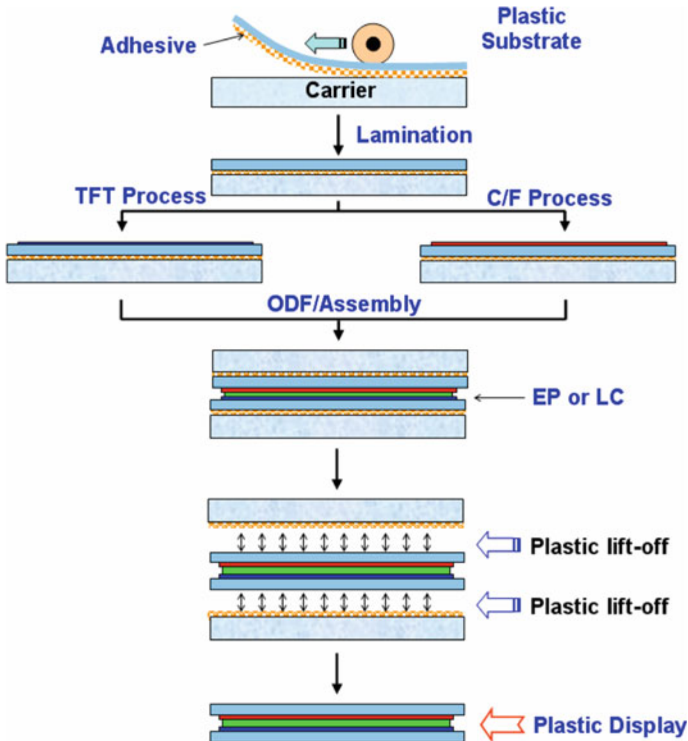

Fig. 11.18 Process sequence for flexible display fabrication using a carrier plate technology. (Reprinted from [35] with permission of SID)

device instabilities, 7 inch transmissive AMLCDs, and 14.3 inch electrophoretic displays were demonstrated on the PES and PEN substrates, respectively.

At the moment, this carrier plate technology, including EPLaR, is the favoured route for developing flexible backplanes of a-Si:H TFTs, using readily available plastic substrates, with a number of groups, in addition to those cited above, demonstrating LCD, electrophoretic and OLED displays [36].

11.4.1.4 Roll-to-Roll (R2R) Processing

Roll-to-roll processing is frequently viewed as the ultimate, low cost route to producing displays on flexible substrates [3]. The ideal R2R process would involve continuous movement of the flexible substrate from its host reel through the different layer deposition and definition stages until the final product is gathered on the collection reel [37]. A detailed discussion of the equipment required, and other R2R issues, is contained in Ref. [37], although no example is given of a particular R2R process being implemented. In this section, a recent application of these principles to the fabrication of a-Si:H TFTs is described [2, 38], using a self-

aligned imprint lithography (SAIL) process. Given the previous discussion on the dimensional instability of plastic substrates, the authors designed a self-aligned process to overcome one of the major hurdles associated with handling plastics. The process imprinted the etch mask on the substrate, so that any deformation in the plastic, causing potential misalignment between one pattern and the next, would also deform the mask by the same amount, thereby cancelling out the pattern shift. The process employed sequential deposition of all layers in the device structure [38], starting with an adhesion layer, the gate metal, the triple stack of SiN_x, i a-Si:H and n^+ micro-crystalline Si to the final metallisation layer without any intermediate pattern definition. Hence, the deposition process could be achieved without breaking the vacuum, leading to reduced contamination problems, and a smaller equipment footprint. Following this, a three-dimensional, UV-transparent elastomer etch mask, which had been wrapped around a quartz roller, was imprinted onto the surface of the device layer stack by rolling the quartz cylinder across the substrate. Whilst the roller was in contact with the sample surface, UV radiation passed through the cylinder and polymerised the imprinted material on the substrate surface. The roller plus imprint stamp is shown in Fig. 11.19a, and an SEM image of a high-aspect ratio and high-resolution imprinted pattern is shown in Fig. 11.19b. The multiple step heights in this pattern were used to define the individual layers in the device stack. In other words, the variable step heights represented the individual mask layers, which would be used in a conventional photolithography process. The use of the imprint pattern to define the device structure is illustrated in Fig. 11.20, and Fig. 11.20a shows the imprinted pattern on top of the device layer stack prior to any etching. Selective etching was used for the removal of individual layers in the stack, as well as for etching and removal of the polymer mask itself. The first etch stage is shown in Fig. 11.20b, in which the total device stack was defined, and Fig. 11.20c shows lateral undercutting of the gate metal, which removed it from narrow 'fuse' areas, such as the source and drain contact lines, assuring good isolation between the source/drain and gate metallisation layers. In Fig. 11.20d, the thinnest mask region had been completely etched away, exposing the stack of layers over the gate contact pad, and Fig. 11.20e shows the removal of those layers, down to the

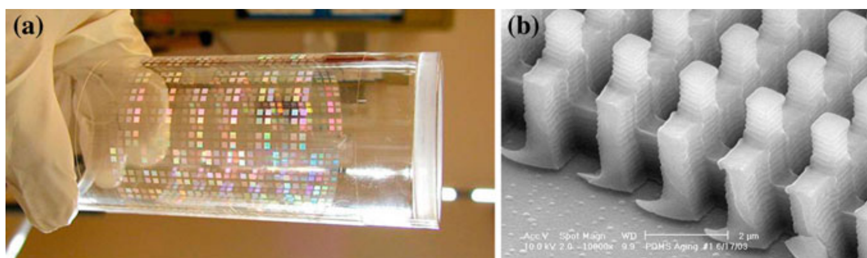

Fig. 11.19 **a** UV-transparent quartz roller with an elastomeric imprint stamp wrapped around it, and **b** SEM image of imprinted polymeric mask pattern used in the roll-to-roll SAIL process. (Reprinted from [38] with permission of SID)

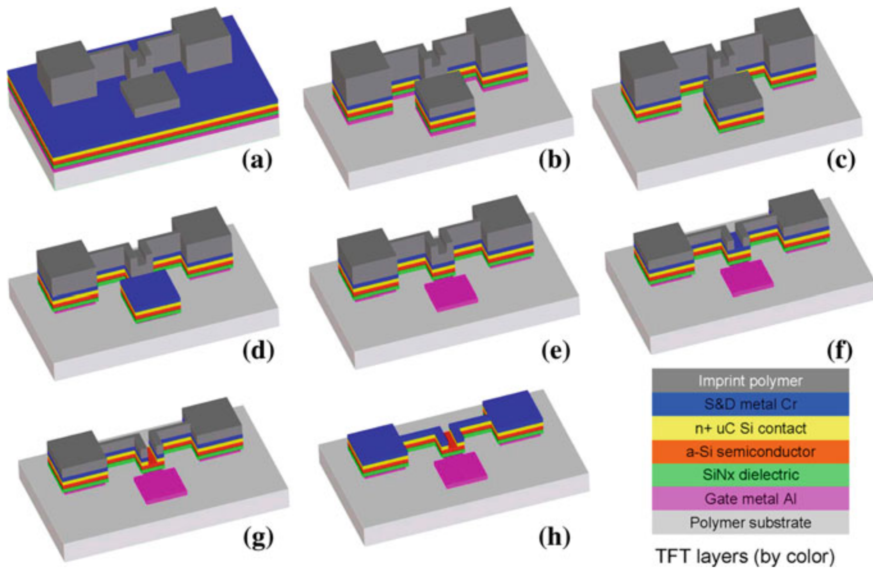

Fig. 11.20 Illustration of SAIL imprint mask and etching sequence to fabricate back-channel etched a-Si:H TFTs. (Reprinted from [38] with permission of SID)

contact pad itself. The next thinnest portion of the etch mask covered the TFT channel region, and, as shown by Figs. 11.20f and g, removal of that masking material permitted the n^+ mc-Si, and the source/drain metallisation, to be removed from the channel region, yielding a conventional back-channel-etched TFT. Figure 11.20h shows the removal of the last remaining layer of masking material, and the consequent exposure of the source/drain contact pads.

The process was implemented on a 13 inch wide and 50 μm thick web of polyimide material, with layer depositions at a maximum temperature of 250 °C, and used dry etching for the removal of the elastomer mask material and the Si-based layers, and wet etching for the metal regions.

The transfer characteristics, normalised by channel size, are shown in Fig. 11.21, and reasonable current scaling was obtained from devices with channel lengths from 100 μm down to 1 μm. The electron mobility in the short channel devices was 0.34 cm^2/Vs, and the on:off current ratio was 10^7. Small electrophoretic demonstration displays were also made using these roll-to-roll processed substrates [38].

11.4.2 Uniaxial Strain Effects on a-SiH TFTs

The effect of uniaxial strain on a-Si:H TFTs was measured by bending the samples around cylinders of different diameter, with the strain parallel to the direction of current flow in the channel. The strain was computed from the bending radius

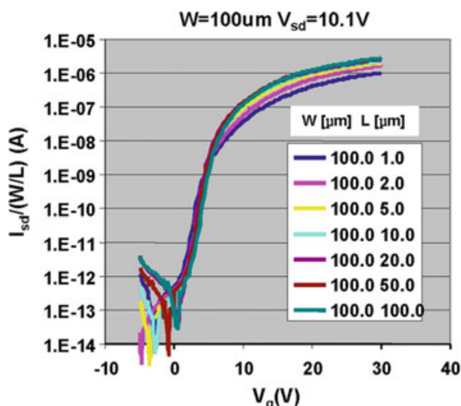

Fig. 11.21 Channel-dimension-normalised transfer characteristics of different channel length a-Si:H TFTs, fabricated by the SAIL process. (Reprinted from [38] with permission of SID)

using equation 11.6, and the samples were under tensile strain when the TFT layer was on the outer surface of a hollow cylinder, and under compressive strain when it was on the inner surface (see Fig. 11.4).

Consistent effects of strain have been reported on differently prepared samples. In one case it was measured on etch-stop TFTs prepared at 150 °C on 50 μm thick polyimide foils, which had used PECVD SiN_x layers for substrate capping and for the gate insulator [39]. In the other case, back-channel-etched TFTs were fabricated on 200 μm thick PES substrates, with an organic layer as the major portion of the gate insulator, topped by a thinner layer of SiN_x, which was defined into small device island areas in order to relieve the overall process-induced strain in the substrates [40]. The variation of electron mobility with strain is shown in Fig. 11.22 [39], where the applied strain values were established to lie within the limits of reversible elastic deformation. Beyond these limits, the samples were found to display irreversible changes in their characteristics, due to the formation of stress-induced cracks. Figure 11.22 shows a linear relationship between mobility and strain, in which compressive strain reduced the mobility and tensile strain increased it. The constant of proportionality in this data set was 26, and, in the other work, nearly identical results were found with a constant of proportionality of 28 [40]. The mobility changes occurred within the time taken to begin the TFT measurements, and there was no dependence of the changes upon the duration of the bending, up to a maximum measured duration of 40 h; and, once

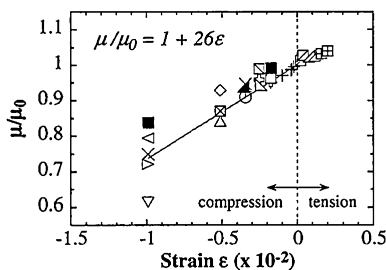

Fig. 11.22 Normalised electron mobility changes in a-Si:H TFTs as a function of uniaxial bending strain. (Reprinted with permission from [39]. Copyright (2002) American Institute of Physics)

the strain was released, the mobility reverted to its pre-strain values [39]. Uniaxial strain has been demonstrated to cause electron mobility changes in crystalline silicon [41] (which is discussed further in Sect. 11.5.2), but it was argued that those mechanisms could not apply to a-Si:H TFTs [39]. A tentative physical explanation for the a-Si:H results was given by noting that the measured electron mobility is governed by the width of the band-tail states, and that these are determined by the structural disorder in the material, which will change with strain [39, 40].

For both sets of samples, the off-state current was found to be independent of strain [39, 40], whilst the threshold voltage had no discernable dependence on strain, and the sub-threshold slope showed a small increase with compressive strain [39].

11.5 Poly-Si TFTs on Flexible Substrates

11.5.1 Fabrication Processes

The introductory section on flexible substrates applies equally to poly-Si TFTs, as to a-Si:H TFTs, and, as discussed, plastic substrates present a number of handling issues in terms of their low maximum processing temperature, dimensional instability and propensity to adopt a cylindrical shape in response to accumulated processing strains. In common with a-Si:H processing, broadly the same three strategies have been adopted in developing a flexible substrate technology for poly-Si TFTs. These are:

- A low temperature process matched to the properties of the plastic substrate,
- A higher temperature process, which could be implemented on thin steel foils,
- A transfer process, as distinct from a carrier plate process, whereby the functional TFT layer was removed from a glass substrate at the end of a conventional fabrication schedule, and transferred to a plastic substrate. This is the easiest technical option in the sense that the poly-Si on glass technology can be directly used, but is more expensive due to the additional process stages for the transfer, plus the extra substrate cost if the substrate cannot be reused.

Each of these three processing strategies is described below, followed by a further section on the response of poly-Si TFTs to bending strains. In Sect. 11.7, there is a discussion of some of the broader issues of device and circuit operation on plastic substrates, particularly for poly-Si TFTs, over and above the previously discussed handling issues.

11.5.1.1 Direct Fabrication on Plastic Substrates

Two approaches can be seen in the poly-Si work: one being to develop an ultra-low temperature process at <200 °C for use on the transparent, lower temperature substrates such as PEN, PET and PES [42, 46, 47] listed in Table 11.1, and the other to modify the established poly-Si process for the higher temperature substrates such as PI and PAR [10, 42]. In all cases, substrate preparation by drying, capping and pre-shrinking (as discussed in Sect. 11.2) was necessary to ensure dimensional stability of the substrates through successive photo-lithography stages.

The low temperature tolerance of the plastic substrates meant that only the excimer laser annealing, ELA, process was suitable for crystallisation of the precursor film, and the deposition temperature of this film, and of the gate oxide film, had to be reduced to meet the temperature constraints of the substrate. Similarly, the thermal budget for the post-metallisation anneal of the TFT, which is important for the reduction of charges and interface states, as discussed in Sect. 7.3.1, also had to be reduced.

For the precursor a-Si film, both conventional PECVD was used at 180 °C or 200 °C for PES and PI substrates, respectively [10], and sputter deposition in He was used for PES substrates [47]. The PECVD films were passed through the standard top-gated, non-self aligned, NSA, process, described in Sect. 7.3.2. The NSA architecture was chosen in preference to the SA architecture, because the latter needs a second laser pass to activate the source and drain dopants, and this could lead to potentially damaging, direct laser exposure of the plastic substrate (in regions where the poly-Si had been removed during the poly-Si island definition stage) [42]. With the NSA architecture, the source and drain dopants were implanted before crystallisation, and the unpatterned a-Si film protected the underlying plastic from direct exposure to the laser beam. Prior to ELA, the excess hydrogen had to be removed from the films, and this was done with a low intensity (230 mJ/cm^2) laser beam, which had a deliberately ramped leading edge for controlled release of the hydrogen. The film was then crystallised in the normal way with a second laser pass at 320 mJ/cm^2. After TFT island definition, the gate oxide layers were deposited at 180 °C and 250 °C for PES and PI substrates, respectively, but as these deposition temperatures were below the 300 °C normally used, the oxide quality was poorer and the interface state densities were higher than normal [10, 42]. The thermal desorption spectra, TDS, of these low temperature oxides [42] have already been discussed in Sect. 7.3.1, and, as shown in Fig. 7.23a, for depositions below 200 °C, the oxides showed high values of the undesired low temperature peaks. Figures 11.23a and b show the changes in n-channel sub-threshold slope and electron mobility, respectively, as a function of the post-metallisation anneal time and temperature [10, 12]. Even the higher quality oxides, deposited at 250 °C, required 1,000 min annealing at 250 °C for the electron mobility to reach 80 % of the standard-process mobility. Whereas, for the oxide deposited at 200 °C, and annealed at this temperature, only ~22 % of the standard-process mobility was reached in this time. This situation was also

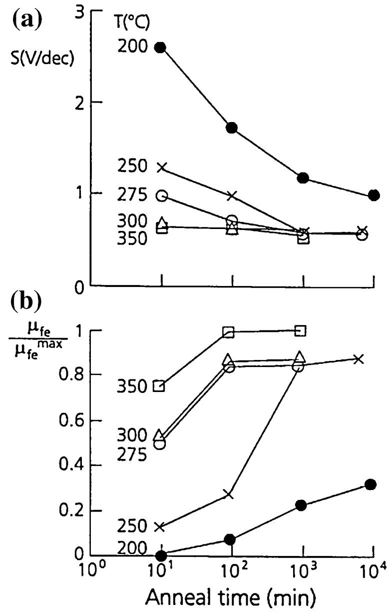

Fig. 11.23 Changes in (**a**) sub-threshold slope and (**b**) normalised electron mobility in poly-Si TFTs with post-metallisation annealing at the SiO_2 deposition temperature. (Reprinted from [12] with permission of SID)

mirrored by the sub-threshold slope results, and it was concluded that acceptable TFT performance could be achieved from a 250 °C process, with the transfer characteristics shown in Fig. 11.24. However, even at this temperature, the p–channel TFTs had larger sub-threshold slopes than the n-channel TFTs, and, at lower annealing temperatures, acceptable device performance was not obtained from p-channel TFTs. Only n-channel TFTS were obtained from a 200 °C process [10, 42, 46], and, hence, the CMOS poly-Si process was only compatible with the higher temperature PAR or PI substrates, and not with the PES substrates.

The reduced temperature oxide deposition process was identified as the processing stage limiting device performance, and, as discussed in Sect. 7.3, ECR

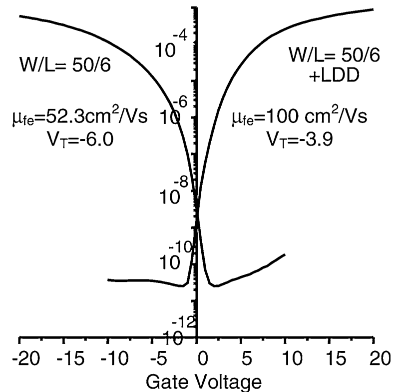

Fig. 11.24 Transfer characteristics of poly-Si TFTs fabricated on PI substrates at a maximum temperature of 250 °C. (Reproduced with permission from [10])

oxides, with good TDS spectra, have been deposited down to room temperature [44], but they have still needed post-deposition annealing above 350 °C to achieve low interface densities and useful TFT characteristics [43, 44].

For the He-sputtered precursor a-Si films on PES substrates [47], it was reported that He removal was easier than hydrogen removal, and this was accomplished with the leading edge of the crystallisation beam [47]. No details were given of the beam shape, but it must be assumed that it was closer to the raw semi-gaussian beam than to a top-hat beam. The overall processing of these samples was quite different from the work described above, and a schematic of the process flow is shown in Fig. 11.25. The gate oxide was deposited by PECVD at 110 °C, and, after gate metal definition, anisotropic plasma etching was used to remove the gate oxide from those areas not beneath the gate electrode. This enabled the exposed source and drain areas to be doped using a plasma-doping procedure in PH_3 or B_2H_6-containing gases, giving SA n- and p-channel TFTs, respectively. The dopants were subsequently activated by ELA, and it was argued that this process also led to heating of the Si/SiO_2 interface, and a consequent reduction of the interface state density. This 110 °C process on PES yielded high quality devices with an electron mobility of 250 cm^2/Vs and a sub-threshold slope of 0.16 V/decade [47]. However, many aspects of this process have not been fully revealed, such as the very low temperature PECVD oxide deposition process, and the overall quality of the resulting oxide. Nor have the details of the ELA activation process been discussed, including its possible impact upon the exposed PES substrate and its role in improving the Si/SiO_2 interface. Without these details, it is difficult to assess whether this process is readily implementable on PES, or on even lower temperature substrates, such as PEN.

11.5.1.2 Fabrication on Steel Foils

As discussed in Sect. 11.4.1.2, when compared with plastic substrates, steel foils are dimensionally stable, can be exposed to elevated temperatures, and are less susceptible to attack by a range of chemicals. Nevertheless, as-delivered steel substrates are too rough for direct use and need to be polished to achieve an acceptable level of surface roughness of a couple of nanometers, they also need to be thoroughly cleaned before use and capped with a thick enough dielectric layer to minimise parasitic capacitive coupling between the conducting substrate and the overlying TFT circuits [27, 48]. In the work quoted below, 125 μm thick polished foils of 304-type steel were used, with an average surface roughness of 3 nm. Both surfaces were coated with 3 μm of PECVD SiO_2 as both a planarising layer, and as a protective barrier to prevent metal ion diffusion into the overlying poly-Si TFTs [48]. This thickness was also necessary to minimise parasitic capacitive coupling between the conducting substrate and the TFTs [27].

The TFTs were fabricated using a SA process, similar to that described in Sect. 7.4.2 and shown in Fig. 7.34. The a-Si precursor layer was 50 nm thick, and was crystallised using an SLS process; then a 50 nm thick PECVD gate oxide was

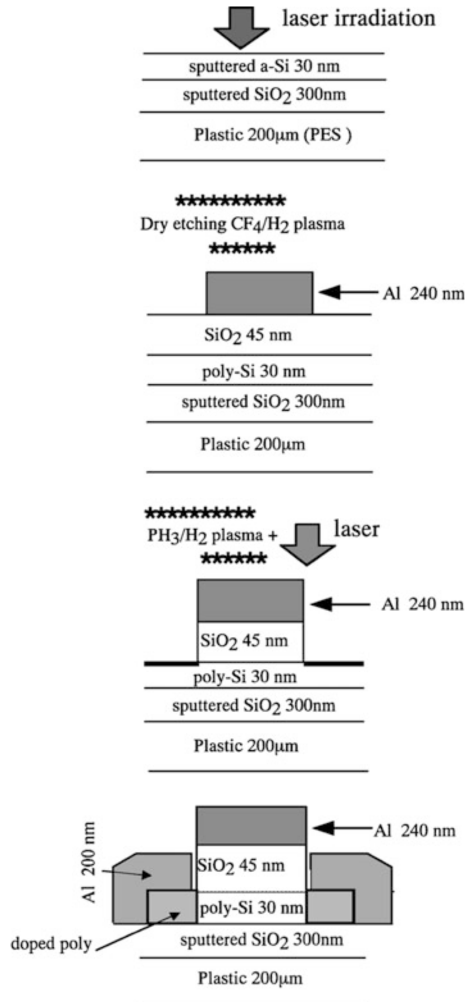

Fig. 11.25 Processing sequence of SA poly-Si TFTs on a PES plastic substrate, showing the crystallisation and plasma doping stages. (Reprinted with permission from [47]. Copyright (2000) The Japan Society of Applied Physics)

deposited from SiH_4 and N_2O, and a doped poly-Si layer was used as the gate electrode. The SA source and drain regions were ion doped and activated by thermal annealing at 650 °C. Following silicidation of the doped regions at 400 °C, the device was exposed to a hydrogen plasma at 300 °C, capped with a 300 nm SiO_2 interlayer dielectric, and, after source and drain metallisation, a final post-metallisation anneal at 300 °C completed the process [48]. Low leakage, high performance, short channel (L = 1 μm) n- and p-channel TFTs, were obtained, with sub-threshold slopes of 0.22 and 0.16 V/dec, and carrier mobilities of ~300 and ~150 cm^2/Vs, respectively.

As will be appreciated, the high processing temperatures tolerated by the steel foils permitted the fabrication of TFTs with performance comparable to conventional glass-based processing, and considerably better than has been achieved

directly on plastic substrates. In addition to the TFTs, a variety of demonstration circuits were fabricated on the foils, including ring oscillators, static shift registers with buffer output stages, decoders, sample-and-hold circuits and 5-bit digital-to-analogue converters [48]. In general, satisfactory performance was obtained from these circuits, although there was a gate-line resistance problem with the ring oscillators associated with the doped poly-Si gates. This would be resolved with lower resistance metal gates—but common metals, like aluminium, could not be used with a 650 °C dopant activation process. However, this is an issue with the specific process implemented on steel substrates in this work, rather than being a limitation imposed by the substrate choice itself. The ring oscillator circuits were fabricated with 1 μm and 2 μm channel length TFTs, and, the delay per stage was 0.88 ns and 1.0 ns, respectively. The speed should scale as $1/L^2$, and, this poor scaling with channel length suggested that the high frequency performance was being limited by parasitic effects [48]. It could be that thicker or lower-k dielectric layers may be needed for substrate capping to reduce the coupling.

11.5.1.3 Transfer Processes

With transfer processes, the basic glass-based processing schedule was retained, and, at the end of it, the TFT layers were detached from the glass and bonded to a plastic substrate. Two examples of this are, firstly, SUFTLA (surface free technology by laser annealing) [49, 50], in which a hydrogen-rich a-Si:H release layer was interposed between the glass substrate and the TFT layer, and, secondly, a glass etching procedure, in which the glass substrate was thinned to several tens of microns [51, 52] before being bonded to a plastic substrate. A third procedure used a different technique, whereby a polymer layer, which ultimately became the plastic substrate, was spun onto the glass substrate before TFT processing, and, at the end of processing, the polymer layer was released from the substrate with the TFT layers attached [53, 54]. This is conceptually similar to the EPLaR process [30, 55], described in Sect. 11.4.1.3, for the fabrication of a-Si:H TFTs on plastic substrates.

The SUFTLA process is shown schematically in Fig. 11.26a–e [50], and, in Fig. 11.26a, the fully processed TFT plate is shown with the sacrificial layer of hydrogen-rich a-Si:H, which had been deposited on the glass substrate prior to TFT processing. Before the removal of the glass substrate, the completed TFTs were mechanically protected from damage during the removal process by temporarily bonding a glass substrate to the top surface with water-soluble adhesive (Fig. 11.26b). The back surface of the original substrate was then exposed to an excimer laser, which released hydrogen from the a-Si:H layer, and detached the TFT layer from the glass substrate (Fig. 11.26c). The TFT layer was then permanently glued to a 400 μm thick plastic substrate (Fig. 11.26d) [49], after which the temporary protective substrate on top of the TFT layer was removed by dissolving the adhesive in water (Fig. 11.26e). The TFT process [49] was a conventional self-aligned fabrication schedule, using a 50 nm pre-cursor a-Si layer,

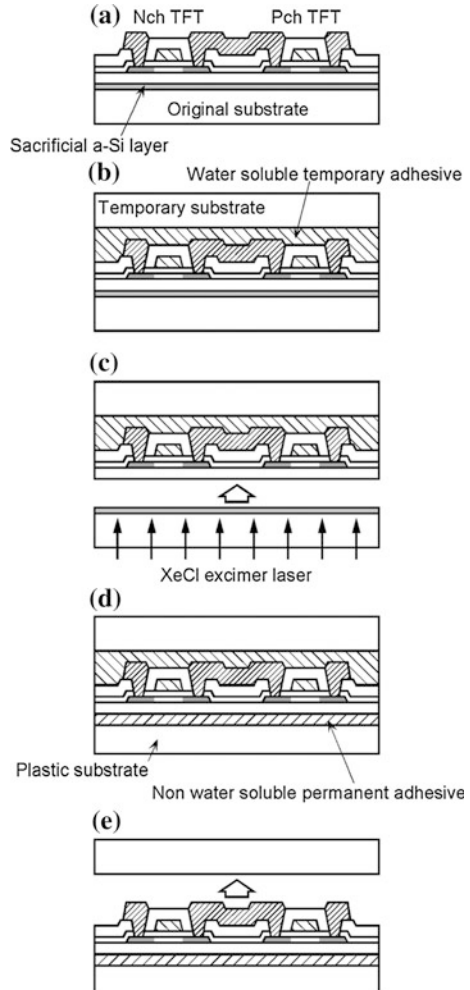

Fig. 11.26 SUFTLA process flow at the end of poly-Si device processing, showing the transfer stages from the glass substrate to the final plastic substrate. (Reprinted from [50] with permission of SID)

which was crystallised by ELA, and capped by a 120 nm gate oxide. After definition of Ta gate electrodes, the source and drain regions were ion doped, and activated at 300 °C. TEOS layers were used as interlayer dielectrics to separate the gate metallisation level from the source/drain metallisation, and also for final capping of the finished devices. Small changes in device characteristics were noted before and after the transfer process, such as electron mobility and threshold voltage changes of 119–124 cm^2/Vs and 3.3–3.9 V, respectively [49]. However, the transfer process was described as high yield, and many demonstration devices were produced with this process, including a 0.7 inch AMLCD [49], a 7.1 inch electrophoretic display, both with integrated drive circuits, and a range of other electronic circuits including an 8-bit microprocessor [50].

The glass etch transfer process was optimised for application to large 300 mm × 350 mm substrates, and the final bonding was to an engineered fibrous

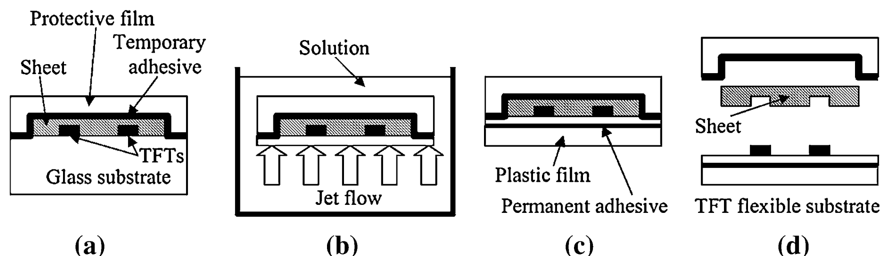

Fig. 11.27 Transfer sequence, at the end of poly-Si TFT processing, showing the thinning of the glass substrate by etching, and the subsequent adhesive-bonding to a plastic substrate. (Reprinted from [52] with permission of IEEE)

glass-reinforced plastic, FRP, substrate [11]. The substrate was designed to have a CTE of ~14 ppm/K, which is lower than most of the plastics listed in Table 11.1, and is a better match to the TFT layers. The adhesive attaching the TFT layers to the FRP substrate was also optimised to reduce de-lamination of the substrate from the TFT layer under bending strain. The transfer process is shown schematically in Fig. 11.27a–d [52], and, in common with the SUFTLA process, the fully processed TFT plate was capped with a protective film, secured by a heat-releasable adhesive, to prevent damage to the TFT layer during the transfer process (Fig. 11.27a). The glass substrate was then jet etched (Fig. 11.27b) to reduce its thickness to a few tens of microns in a uniform fashion, and this left behind a smooth etched surface. The thinned glass was then permanently bonded, using the optimised adhesive, to a 220 μm thick FRP substrate (Fig 11.27c). Finally, the top protective film was removed, by heating the structure to 110 °C for 90 s to release the temporary adhesive, and the finished TFT layer on the plastic substrate was annealed at 150 °C to complete the process. Very good reproducibility of the TFT characteristics was found before and after the transfer process, as shown by the results in Fig. 11.28.

A potentially simpler process option is one in which the TFTs are fabricated directly on a thick spun-on layer, of a suitable polymer, on a rigid substrate, and the double layer of TFTs and polymer film removed from the rigid substrate at the end of processing. In this case, the resulting TFT layer is automatically on a flexible substrate, and a separate substrate attachment stage can be avoided. The implementation of this process [53, 54] used an 8 μm thick spin-on layer of polyimide on an oxidised silicon substrate. Following thermal curing of the PI layer at 350 °C, it had a CTE of 3 ppm/K, which was much lower than the bulk PI film in Table 11.1, and was a good match to the silicon substrate. The cured PI layer was coated with a barrier stack of SiN_x and SiO_2, prior to the growth of a 70 nm thick a-Si pre-cursor layer, capped by a 25 nm thick heavily phosphorus doped a-Si layer. A channel-etched, non-self-aligned TFT process was implemented with these layers [45], but, due to the thermal constraints imposed by the underlying PI layer, the normal 450 °C thermal dehydrogenation process could not be used on the a-Si film. Instead, it was partially dehydrogenated for 18 h at

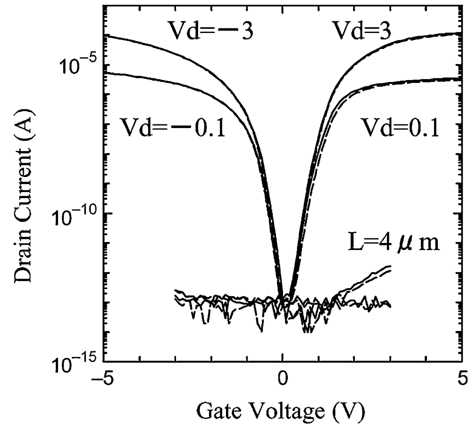

Fig. 11.28 Poly-Si TFT transfer characteristics before (*solid line*) and after (*broken line*) the glass etching transfer process. (Reprinted from [52] with permission of IEEE)

350 °C, before being crystallised with a modified excimer laser beam, having a ramped leading edge designed for the controlled release of hydrogen from the film [53]. The gate dielectric was a 150 nm thick layer of ECR-PECVD SiO_2 [44] deposited at room temperature, and, after deposition and definition of the aluminium source, drain and gate electrodes, there was a post-metallisation anneal at 350 °C. At the end of this process, the poly-Si devices on the 8 μm thick PI layer were mechanically released from the silicon substrate, although the details of the release process have not been revealed. A number of demonstration poly-Si circuits were fabricated on these flexible substrates, including logic gates, ring oscillators, and amplifiers, as well as an integrated humidity sensor [54].

EPLaR has also been used to make poly-Si TFTs [30], but with a conventional self-aligned p-channel process, which included laser activation of the source and drain dopants. However, the PI intermediate layer on the glass substrate was damaged by this direct exposure to the laser, and an unspecified shielding layer was interposed between the TFT layers and the PI to protect it. As with the a-Si TFT implementation of EPLaR, the poly-Si TFT layer on PI was released from the glass substrate by excimer laser exposure of the PI layer through the glass substrate. The TFT characteristics remained unchanged by the release process.

11.5.2 Uniaxial Strain Effects on Poly-Si TFTs

The effect of strain on poly-Si TFTs has been studied with SLS-crystallised devices, made on flexible steel substrates, using the process described in Sect. 11.5.1.2 [27, 48]. Small 20 mm × 35 mm sections of the substrates were cut from the processed foils and bent around hollow cylinders of different radius [13]. The TFTs were under tensile strain when bent around the outside of the cylinders, and under compressive strain when bent around the inner surface, and the dependence of strain on radius of curvature is given by Eq. 11.6.

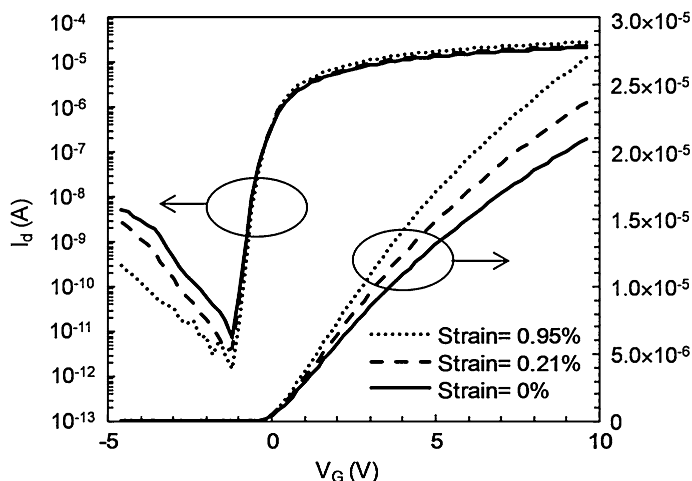

Fig. 11.29 Effect of uniaxial tensile strain on n-channel poly-Si TFTs. (Reprinted with permission from [13]. Copyright (2009) American Institute of Physics)

By measuring the TFT characteristics as a function of the bending radius, the dependence of the various device parameters on uniaxial strain was established [13]. In all measurements, the strain was parallel to the direction of current flow, which itself was parallel to the SLS-induced sub-grain boundaries, and the n-channel characteristics under tensile strain are shown in Fig. 11.29. There was decreased off-current and increased on-current with increasing strain, where the increased on-current was caused by an increase in electron mobility. The opposite trend was found for compressive strain, and the summarised carrier mobility results are shown in Fig. 11.30. This figure also includes the hole mobility results derived from p-channel TFTs; as will be seen, there were opposite trends between hole and electron mobilities. In contrast, the leakage current behaved identically in both channel types: decreasing with tensile strain and increasing with compressive strain. In single crystal silicon p-n junction diodes, the leakage current was also found to increase with compressive stress, which was attributed to stress-induced decrease of the Si band-gap at the rate of ~0.1 meV/MPa [56]; similarly, MOSFET junction leakage current was found to increase with compressive stress and to decrease with tensile stress [57]. The leakage-current in poly-Si TFTs clearly behaves in the same way as in crystalline silicon, and has been similarly attributed to stress-induced changes in the band-gap [13].

The carrier mobility changes have also been correlated [13] with similar stress-induced mobility changes in crystalline Si MOSFETs. For p-channel MOSFETs, compressive stress increased the curvature of the lowest energy valence band sub-band, reducing the hole effective mass [58], and, hence, increased the hole mobility. For n-channel MOSFETs, tensile stress led to splitting and repopulation of degenerate conduction band sub-bands, such that the population in the sub-band having the low transverse effective mass was enhanced at the expense of the

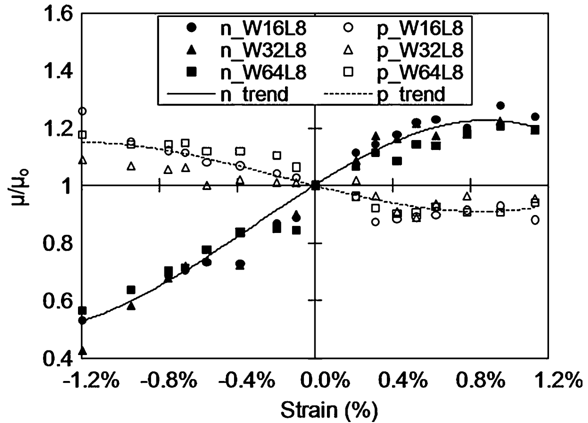

Fig. 11.30 Effect of uniaxial tensile (+) and compressive (−) strain on normalised hole and electron mobilities in poly-Si TFTs. (Reprinted with permission from [13]. Copyright (2009) American Institute of Physics)

sub-band having the higher longitudinal effective mass, thereby increasing the overall electron mobility [59].

The TFT mobility changes, discussed above, were observed in long grain SLS poly-Si, and similar changes have also been reported in metal-induced crystallised poly-Si [60]. In more conventional ELA poly-Si, on thin plastic substrates, no discernable mobility changes were detected down to a bending radius of 1.3 cm [53]. However, using Eq. 11.6, the strain in the TFT layer on the 8 μm thick compliant PI substrate is calculated to be only 0.012 %, which is considerably less than the values in Fig. 11.30, and this may be why no mobility changes were observed.

For the other device parameters, the sub-threshold slope in both channel types increased with tensile stress and decreased with compressive stress, whilst threshold voltage showed no dependence upon compressive stress, but decreased with tensile stress [13]. In contrast to the leakage current and carrier mobility changes, no simple physical models have been advanced to explain these sub-threshold slope and threshold voltage changes.

11.6 Organic TFTs on Flexible Substrates

In principle, the fabrication of organic TFTs on plastic substrates should present fewer issues than is the case with inorganic TFTs, particularly in terms of the temperature constraints imposed by the substrates. As has been discussed above, these constraints set an upper processing temperature limit, determined by the substrate's glass transition temperature, but the actual maximum temperature can be reduced below this by CTE mismatch considerations. For organic TFTs, there should be a better CTE match, and device processing itself is conventionally performed close to room temperature. However, although the upper temperature constraint is less of an issue, other attributes of plastic substrates, such as their

dimensional instability, sensitivity to chemical attack etc., still have to be controlled during processing. To deal with the dimensional instability problem, most groups pre-shrink the substrate before processing; however, details on subsequent substrate encapsulation are left unspecified in a number of publications. Also, some groups have adopted a rigid carrier plate process to reduce the handling problems of flexible substrates.

As is apparent from Chap. 10, there are a large number of organic transistor materials, device geometries, and fabrication processes, which have already been discussed, and those details will not be repeated below. Only those aspects of the process, specific to fabrication on plastic substrates, will be considered, and the reader is referred to Chap. 10 for further information.

In the following two sub-sections, the direct fabrication of OTFTs on plastic substrates, and rigid carrier plate processing are reviewed, and, finally, the impact of substrate bending on TFT performance is considered.

11.6.1 Fabrication Processes

11.6.1.1 Direct Processing

Where discrete TFTs have been fabricated on plastic substrates, particularly to examine bending effects, both PI [17] and PEN [61] substrates have been used, with evaporated gold bottom-gate and top source and drain contact layers. The gate dielectric was a spin-coated PVP (polyvinylphenol) layer, and shadow mask evaporation was used for the pentacene TFT body layer. No details were given of the handling of the substrates. In another example of pentacene TFTs on PEN substrates [62], the substrate handling was more clearly defined, and followed the procedures familiar from the discussion of a-Si and poly-Si TFT processing on plastic substrates. In particular, the substrate was initially annealed at 180 °C to degas and pre-shrink it, and it was then encapsulated with 100 nm thick SiN encapsulation layers. The bottom-gated and bottom-contacted TFTs had a spin-coated PVP gate insulator, which was cured at 180 °C, and the pentacene layer was capped with parylene and Cr/Au in order to photolithographically define it. In order to protect the pentacene from the effects of ambient water vapour and oxygen, the whole structure was encapsulated with a 1 μm thick spin-coated layer of photacryl, which was cured at 150 °C after photo-patterning.

A full-colour 2.5 inch AMOLED demonstrator was fabricated on a 200 μm thick PES substrate, which had been annealed at 180 °C to shrink it prior to processing, and an alignment accuracy of a few microns was obtained over the 4 inch substrate [63]. The evaporated pentacene TFTs were bottom-gated and bottom-contacted, using gold for both, and a 400 nm thick spin-coated organic PVP-OTS (octadecyltrichlorosilane) layer was used for the gate dielectric, which was cross-linked at 130 °C. The TFT structure was then encapsulated in organic

passivation and planarisation layers prior to the evaporation of the OLED structure. The all-organic composition of the display contributed to its satisfactory operation at a bending radius of 20 mm [63].

11.6.1.2 Carrier Plate Processing

A number of groups have used rigid carriers to reduce the handling problems of plastic substrates, where the carriers have either been glass plates (carrying PET [64] and PEN [65] films) or silicon wafers used with PI films [66]. Generally, the plastic substrates were pre-shrunk by baking for 2 h at 120 °C and at 150 °C for the 125 μm thick films of PEN and PET, respectively. Inorganic barrier films of SiN were used in both cases to prevent moisture and oxygen absorption, and, thereby, improve dimensional stability. The plastic foils were then bonded to the carrier plates using temporary adhesives. In all cases, a bottom-gated and bottom-contacted device architecture was used, with pentacene as the semiconducting TFT material. This process was used to make flexible AMOLED displays [64, 65], and electrophoretic display and shift register [66] demonstrators.

In contrast to the bottom-gated pentacene TFTs, a production facility has been established for flexible electrophoretic displays based upon a printing technology, using top-gated and bottom-contacted polyfluorene-based polymer TFTs [67, 68]. The facility can produce 10.7 inch displays by processing Gen 3.5-sized substrates ($\sim$0.62 × 0.72 m^2) of 125 μm thick PET. A major advantage of the printing process is that it can produce devices without the conventional alignment stages, and that the position of the printing head can be locally adjusted to compensate for substrate distortion [67, 68], but the substrates were, nevertheless, temporarily attached to glass carrier plates during the patterning stages [68]. To minimise dimensional instability, the substrates were pre-annealed, and a planarising layer was deposited before the metal source and drain contacts were formed. The device processing was at, or near, room temperature, using a solution-deposited polymer dielectric for both the gate insulator and the interlayer insulator (between the gate electrode and the pixel electrode).

11.6.2 Uniaxial Strain Effects on Organic TFTs

As with the inorganic TFTs, strain effects were assessed by measuring changes in the TFT characteristics as function of the externally applied bending radius, and this was then converted into a strain value using equation 11.6. Bending strain measurements made on pentacene TFTs, fabricated on 125 μm thick PEN substrates, are shown in Fig. 11.31a–d [61]. These were bottom-gated and top-contacted TFTs, with a 900 nm thick PI gate dielectric. The on-current results in Fig. 11.31a and b were obtained with the strain parallel to current flow, but the hole mobility results in Fig. 11.31c and d were obtained with the strain both

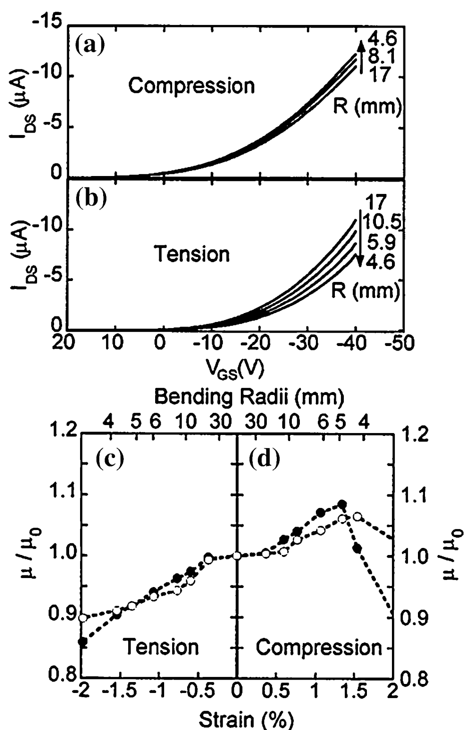

Fig. 11.31 Effect of bending strain on pentacene TFT transfer characteristics under (**a**) compression (**b**) tension, and the effect of bending strain on the hole mobility under (**c**) tension and (**d**) compression (filled and open circles were for current flow parallel and perpendicular to the strain). (Reprinted with permission from [61]. Copyright (2005) American Institute of Physics)

parallel and perpendicular to current flow. As will be seen, the on-currents and hole mobility values increased with compressive strain and decreased with tensile strain, irrespective of the strain direction. The strain effects were explained in terms of hopping transport in the TFTs, where the hopping barrier height was determined by the molecule spacing in the pentacene film, and this decreased under compressive strain and increased under tensile strain [61]. The strain isotropy was attributed to an inter-grain current flow path in which coupled grains were randomly oriented.

The authors also monitored the changes in capacitance, C, of the 900 nm thick PI gate dielectric, and found that it increased by $\sim$3 % with 1.5 % tensile strain, and decreased by $\sim$2.2 % with 1.5 % compressive strain (both of which corresponded to a 4 mm bending radius) [61]. This was explained by changes in the thickness of the gate dielectric caused by the Poisson effect (rather than by changes in dielectric permittivity), where those orthogonal changes are related to the bending radius, R, by:

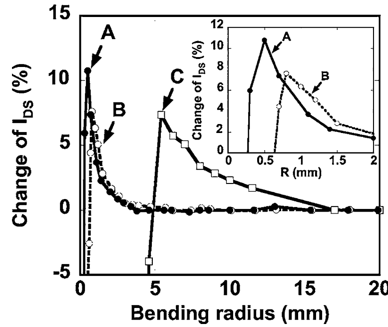

Fig. 11.32 Changes in the on-current in pentacene OTFTs, on 13 μm thick PI substrates, as a function of the bending radius. The TFTs were capped with parylene passivation layers with thicknesses of: (**a**) 13 μm (**b**) 10 μm and (**c**) 0 μm. (Reprinted with permission from [17]. Copyright (2005) American Institute of Physics)

$$1 - C/C_0 = -D/2(1 - v)R \tag{11.10}$$

C_0 is the unstrained capacitance, D is the substrate thickness, and v is Poisson's ratio, which is 0.4 for the PI film [61]. It was argued that these changes, and other dimensional changes in the TFT geometry, should be taken into account when calculating the strain-dependent carrier mobility values.

As seen in Fig. 11.31d, device failure occurred at a compressive bending radius of ~5 mm, which generated a compressive strain >1.5 %, and led to buckling of the gold electrodes [61]. These measurements were made on un-laminated substrates, in which the TFTs on the substrate surface experienced maximum strain for a given bending radius. In a practical application of TFTs on a flexible substrate, the substrate will be capped by another film, such as an electrophoretic film or OLED layer etc. This will move the TFTs towards the neutral plane, and, thereby, reduce the strain for a given bending radius. The beneficial effect of this is shown in Fig. 11.32, in which the same type of pentacene TFTs, as shown in Fig. 11.31, were fabricated on 13 μm thick PI substrates, and laminated with parylene layers of 13 μm and 10 μm thickness, and compared with an uncapped control sample (curves A, B and C, respectively) [17]. The un-laminated sample C showed the same failure, as previously, at a bending radius of 5 mm, but the well-matched sample A, with the same substrate and top-layer thicknesses of 13 μm, could be bent down to a radius of 0.5 mm before failure.

11.7 Plastic Substrate Issues

Over and above the previously discussed issues of handling and processing TFTs on plastic substrates, other concerns have been identified in their use with high-speed poly-Si devices. A particular issue has been power dissipation in the TFT, leading to self-heating, and subsequent heating of the plastic substrate [7]. Where

this is sufficient to cause a temperature rise above the glass transition temperature of the substrate, thermal deformation of the plastic can occur leading to mechanical damage to the TFT. Self-heating is also a potential problem on glass substrates [69] (where the thermal conductivity is 1.38 W/m/K), leading to threshold voltage instability under on-state stress conditions of combined gate and drain bias (see Sect. 8.6.2). Self-heating is a greater problem on plastic substrates due to their lower thermal conductivity of ~0.2 W/m/K, and, as this means that radiation from the device edges becomes the limiting mechanism for heat dissipation, the device design becomes important. In particular, devices with large values of W and L are vulnerable to self-heating, and the authors [7] recommend replacing large W devices with a number of parallel devices each having a smaller W. Also, the overall power dissipation can be reduced by reducing the drive voltages, and this can be accomplished by scaling down the TFT geometry [7], especially the channel length and the gate oxide thickness, as well as the drain bias, by a scaling factor k. This should reduce power dissipation per unit area, at fixed channel current, by the factor k, as well as increasing the operating frequency by k.

A further recommendation is to improve the energy efficiency of the circuits themselves, by using asynchronous circuits [7]. Conventional MOSFET and TFT circuits are usually termed synchronous, and global clock signals are applied to all logic blocks throughout the system. In asynchronous circuits, the clock signals are only sent to particular logic blocks when they are needed, and poly-Si asynchronous microprocessors have been found to dissipate 73 % less energy than synchronous circuits performing the same function [7].

Hence, both changes in device design and circuit design are advocated for optimising the performance of poly-Si circuits on low-temperature plastic substrates, even where the handling issues of plastic substrates have been circumvented by using a transfer process.

Self heating has also been reported in a-Si:H TFTs on PI substrates [70], in which the width-normalised drain current of TFTs with W/L = 80 μm/8 μm and 10 μm/8 μm agreed at low drain bias, but, at high gate and drain bias, the large W TFT showed a higher current than the small W TFT. In the large W TFT, the current also failed to saturate, as shown in Fig. 11.33a. Hence, the same geometric factors leading to self-heating have been identified in a-Si:H TFTs as in poly-Si TFTs. For self-heating to occur, both gate and drain bias must be applied in order to drive current through the TFT, as is the case in Fig. 11.33a. When threshold voltage stability was investigated under saturation drain bias conditions ($V_D = V_G\text{-}V_T$) at large V_D, the threshold voltage shift was found to increase with increasing channel width, as shown in Fig. 11.33b, and this shift was larger than with gate bias stress alone [70]. Device stability has been studied under combined gate and drain bias stress in conventional a-Si:H TFTs on glass [71], where the change in threshold voltage was found to be less than under gate bias stress alone. This was due to the reduced overall carrier density in a pinched-off inversion layer (see Sect. 6.4.3). Hence, the opposite effect was seen when comparing combined bias-stress effects in TFTs on glass and plastic substrates, and the larger shifts seen on the plastic substrates have been attributed to self-heating in large W TFTs [70].

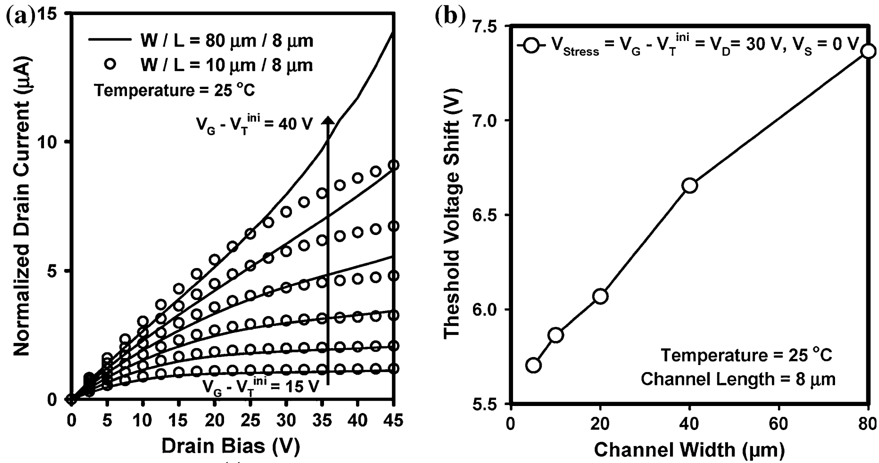

Fig. 11.33 **a** Normalised drain current in a-Si:H TFTs for W = 80 µm, and W = 8 µm, showing higher currents for W = 80 µm at large values of V_G and V_D, and **b** dependence of threshold voltage instability on channel width, W, under saturation bias-stress conditions. (Reprinted from [70] with permission of IEEE)

In addition, the self-heating-induced threshold voltage instability was further increased by bending the substrate down to a 15 mm radius of curvature [70]. Self-heating has been previously reported in short channel a-Si:H TFTs on glass [72], but neither channel width nor device stability effects were investigated in that work. In common with poly-Si TFTs, it is clear that large W TFTs can cause self heating, which, in the case of a-Si:H, exacerbates bias-stress instability effects, and attention to device design is required to minimise these effects.

11.8 Summary

The flat panel display industry has been built around a-Si:H TFTs on rigid glass substrates, but there are clearly identified applications requiring flexible substrates. This has stimulated much research investigating how the established a-Si:H, and also poly-Si, TFT technologies could be implemented on inexpensive plastic substrates. The major issues in using these readily available substrates have been their low maximum processing temperatures, thermal mismatch to the conventional device layers such as SiN_x:H, SiO_2 and Si, and also the dimensional instability of the plastic itself. In view of these problems, a number of processing strategies have emerged, including reduced temperature TFT processing directly onto the plastic substrates, and the use of non-standard plastic substrates, which have been engineered to better match the thermal properties of the TFT layers. Secondly, the use of alternative flexible substrates, principally stainless steel foils, which circumvent many of the handling problems of plastic. Thirdly, and

principally for a-Si:H TFTs, a carrier plate technology, whereby the plastic substrate is temporarily bonded to a glass substrate during processing, or a plastic film is spun onto the glass, which, at the end of processing, is released from the glass carrier plate. For poly-Si, a variant of this has emerged, which is a transfer process, whereby the TFTs and circuits are processed in the conventional way on a glass substrate, and, at the end of processing, they are removed from the glass substrate and transferred to a plastic substrate. The most sophisticated demonstrators so far have emerged from either the carrier process for a-Si:H TFTs or the transfer process for poly-Si TFTs. How economic these processes are will emerge in the longer term, but, for the moment, they are, at least, successful expedients which are able to exploit the well established glass plate technologies. The long-term aspiration in this area is for a truly plastic-based, roll-to-roll technology, which does not try to impose conventional photolithography on dimensionally unstable substrates, and some early examples of this approach have been reported for a-Si:H TFTs.

The alternative to the conventional inorganic TFTs, are organic TFTs, which should have a better match to the plastic substrate constraints of reduced processing temperatures and high coefficients of thermal expansion, although the dimensional instability of the plastic still represents a problem for pattern definition. As with the inorganic TFTs, similar strategies have been adopted, including direct substrate processing, carrier plate processing, plus a printing process, which is less sensitive to the dimensional instability of the substrate. With organic TFTs, the most sophisticated demonstrators, so far, have used the carrier plate process or the print-based process.

In addition to the discussion of device processing, the mechanics of bending and strain in flexible substrates is summarised.

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Chapter 12
Source-Gated Transistors

Abstract The source-gated transistor, SGT, is an inverted staggered thin film transistor, which has been engineered to have a barrier contact at the source, rather than the more conventional ohmic contact. Furthermore, the device geometry is designed so that current flow is barrier limited, and, in saturation, the height of this barrier is controlled by the gate voltage. As a result of these design features, the device has quite different behaviour from conventional TFTs. For example, it has a lower saturation voltage, higher output impedance, reduced short channel effects, and its current is insensitive to modest variations in the source-drain separation. The most readily formed barrier is with a Schottky contact, and these contacts have been used in SGTs fabricated in both a-Si:H and poly-Si. They have also been incorporated into the 2-D simulations of device operation, and, as a prelude to the discussion of the SGT, the operation of Schottky barrier diodes is reviewed. In addition to sections over-viewing the structure, operation and fabrication of SGTs, there is also a discussion of the differences in SGT and TFT characteristics. Finally, there is increasing recognition of the influence of the gate bias on the source barrier height in staggered organic TFTs, and analyses of the gate-source interaction in these devices are compared with the SGT analysis.

12.1 Introduction

The source-gated transistor, SGT, is an inverted staggered thin film transistor, in which the current is determined by the height of an injecting barrier at the source junction [1, 2]. Moreover, in saturation, the height of this barrier is controlled by the voltage on an insulated gate electrode. This is in contrast to the conventional TFT, which is also controlled by the voltage on the gate electrode, but, in that case, the gate bias determines the conductivity of a carrier-rich channel layer. The inverted staggered SGT and TFT structures are superficially similar in appearance, as seen in Fig. 12.1 [3]. However, they are engineered to have different properties. For instance, the source junction in a conventional TFT will usually have the lowest possible resistance, so that its value is less than the channel resistance. In a-Si:H and poly-Si TFTs this is achieved with a doped ohmic contact. In organic

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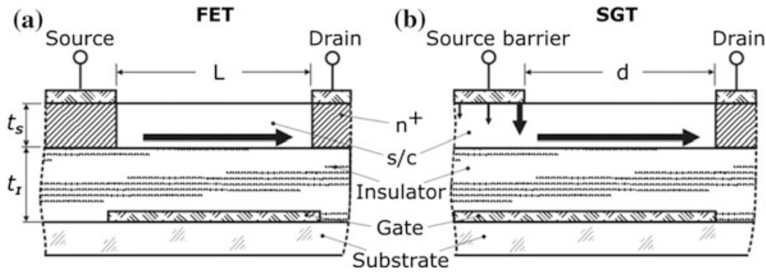

Fig. 12.1 Cross-sectional diagrams of (**a**) an inverted staggered TFT, and (**b**) an SGT. (Reprinted from [3] with permission of IEEE)

and AOS TFTs, doped contacts are not feasible, and metal Schottky barrier contacts are used, where the barrier heights will be minimised by appropriate choice of metal. In high quality devices, the contact resistance will be designed to be less than the channel resistance. Nevertheless, as discussed in Chapter 10, barrier injection problems have been identified in organic TFTs, and aspects of their behaviour may be regarded as having some qualitative commonality with SGTs. The source junction in the SGT will deliberately be a barrier structure, such that on-state operation is determined by carrier emission over and/or through this barrier, and the resistance associated with the source will be engineered to be greater than the channel resistance. This has been achieved by using short source-drain separations (channel lengths) in the SGT. Further essential features of the SGT architecture are that the semiconductor film is thin enough for it to be readily depleted by modest reverse bias values on the source electrode, and that there is adequate source-gate overlap to facilitate electrostatic coupling between these electrodes. These differences in architecture, compared with conventional inverted staggered TFTs, lead to remarkable changes in transistor behaviour, in that the SGT has a much lower saturation voltage, shows minimal short channel effects, and can be insensitive to the separation of the source/drain contacts. Moreover, in the case of a-Si: H, the SGT displays much improved gate bias stability compared with standard TFTs.

To date, operation of this device structure has been demonstrated using a-Si:H [1, 2, 4], and poly-Si [5, 6], and 2-D simulations have shown the same features as the experimental data. Simulations have also indicated that the SGT should have significant benefits when used with low mobility materials, such as disordered organic semiconductors [3, 7, 8].

Whilst most of the reported work has used a Schottky barrier diode, it is worth noting that device operation is not limited to this structure. In principle, any barrier structure could be used, providing the carrier transmission through the barrier is controllable by the local field. Other suggested barrier structures include bulk unipolar, metal-insulator-semiconductor, MIS, and space charge limited diodes [9].

Given the extensive use of Schottky barrier diodes in the published work on SGTs, Sect. 12.2 reviews the operation of these diodes, as background to the

detailed discussion on SGTs. Following this, the SGT structure and its operation are presented in Sect. 12.3, and Sect. 12.4 contains details of device fabrication, including the control of the zero-bias barrier height at the Schottky source junction in a-Si:H SGTs. Section 12.5 presents a comparison of the electrical characteristics of SGTs and conventional TFTs, and Sect. 12.6 reviews other analyses of gate/source-barrier interactions, which have been published in the organic TFT field, and contrasts them with the SGT analysis.

12.2 Schottky Barrier Diodes

The operation of the SGT relies upon the presence of an injection barrier, such as a Schottky diode, at the source junction, and the operation of reverse biased Schottky diodes is summarised below. This review also includes the use of surface doping to control the zero-bias barrier height, which has been used with the devices made to date [1, 2, 5, 6].

The band diagrams of a Schottky barrier diode, on an n-type semiconductor, at zero bias, and at a reverse bias, V_R, are shown in Fig. 12.2a, b, respectively. At zero bias, there are equal and opposite electron currents over the barrier, ϕ_B, from the metal to the semiconductor, and vice versa, giving a zero net current. Due to the built-in bias, V_{bi}, the semiconductor bands are bent upwards at the surface, and there is a small depletion region at the surface. At a reverse bias, V_R, this voltage is dropped across an increased width of semiconductor depletion region, so that the barrier to electron flow from the semiconductor is greatly increased, and the predominant current flow is just from the metal to the semiconductor. In this simplified diagram, the injection barrier from the metal is shown as unchanged by the reverse bias, but in reality there is an image-force field, the Schottky effect, which lowers the barrier in the presence of an applied electric field, E, as shown in Fig. 12.2c. The change in barrier height, $\Delta\phi$, in this example, is given by [10]:

$$\Delta\phi = \sqrt{\frac{qE}{4\pi\varepsilon_0}} \tag{12.1}$$

The diagram shows the Schottky effect on the metal work function in the presence of a constant field, E, in a vacuum. The same effect occurs when the metal contacts a semiconductor surface, as shown in Fig. 12.2d. The barrier lowering, $\Delta\phi$, is given by Eq. 12.1, except that the permittivity of free space, ε_0, is multiplied by the dielectric constant of the semiconductor, ε_s, and the relevant value of field is that at the metal surface, E_B, i.e.

$$\Delta\phi = \sqrt{\frac{qE_B}{4\pi\varepsilon_0\varepsilon_s}} \tag{12.2}$$

In a reverse biased metal-semiconductor Schottky diode, because of the presence of the semiconductor space charge in the depletion region, the internal field

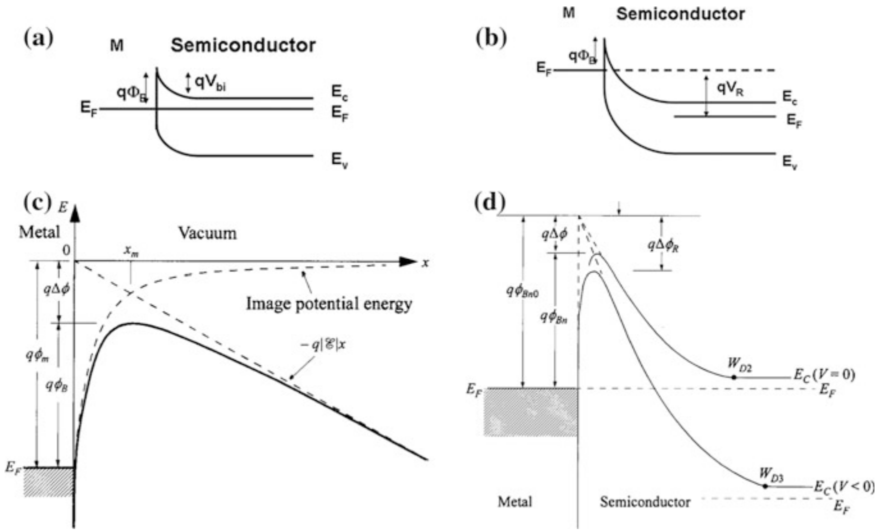

Fig. 12.2 Band diagrams for a Schottky barrier diode on an n-type semiconductor at (**a**) zero bias, (**b**) reverse bias, V_R, (**c**) reverse bias image force lowering of the injection barrier in vacuum, and (**d**) barrier lowering in a metal-semiconductor Schottky diode. [(**c**) and (**d**) reproduced from [10] with permission of John Wiley & Sons, Inc]

varies from zero at the edge of the depletion region to the maximum, E_B, at the surface. Hence, to calculate the Schottky barrier lowering, the field needs to be evaluated at the semiconductor surface.

The process of electron injection at the barrier is also field-sensitive, as shown in Fig. 12.3. The different current flow processes are qualitatively similar to those for carrier emission from a deep trap, as discussed in Sect. 8.5.3. Using the conventional terminology for Schottky barriers [10], these processes are:

- Thermionic emission, TE, of electrons directly over the top of the barrier (including barrier lowering due to the Schottky effect), which is likely to occur at high temperatures and low fields,
- Field emission, FE, by direct tunnelling of electrons at the Fermi level through the barrier, and is most likely to occur at low temperatures and high fields,
- Thermionic field emission, TFE, which is a mixture of TE and FE in that it involves the thermal excitation of electrons to a virtual state, from which they tunnel through a reduced barrier width.

Thus, by increasing the field, it is possible to change the injection mechanism from simple thermal emission, TE, to the field-enhanced process, TFE, which is the mechanism engineered into the experimental SGTs. In a doped semiconductor, the field, E_B, at the reverse biased barrier is given by:

$$E_B = \sqrt{\frac{2qN_d(V_R + V_{bi})}{\varepsilon_s \varepsilon_0}} \tag{12.3}$$

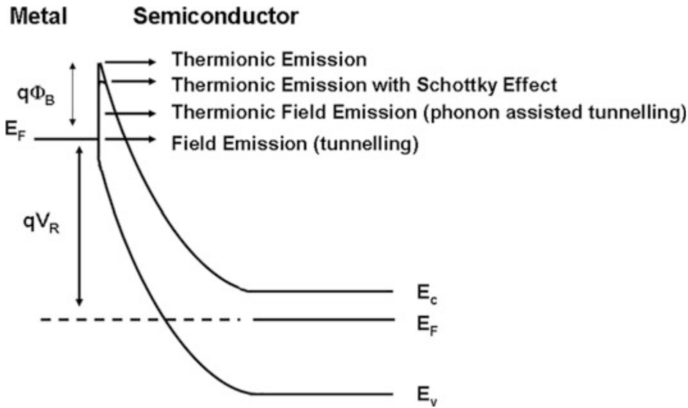

Fig. 12.3 Illustration of the current flow processes in a reverse biased Schottky diode

Equation 12.3 has been derived from Poisson's equation, using the depletion approximation (see Eq. 2.14 for more details), and it shows that the field increases with both the reverse bias, V_R, and the semiconductor doping level, N_d.

For TE, the reverse bias current density, J_R, is given by:

$$J_R = A^* T^2 \exp -q\left(\frac{\phi_B - \Delta\phi}{kT}\right)\left(1 - \exp -\frac{qV_R}{kT}\right) \tag{12.4}$$

where ϕ_B is the barrier height, and A^* is Richardson's constant, which is a function of the carrier mass, and is equal to 120 A/cm^2/K^2 for free electrons. (A correction may be applied to A^* to allow for the specific carrier effective mass of the semiconductor, and, whilst these values have been tabulated for common single crystal semiconductors [10], the basic value of 120 A/cm^2/K^2 is usually assumed for other materials). For $V_R > 3$ kT, the second parenthetic term can be ignored, although V_R still has an important influence on the current via the barrier lowering term, $\Delta\phi$ (Eqs. 12.2 and 12.3).

For high-field TFE in a-Si:H, it has been shown that for a triangular tunnelling barrier, with image-force correction, in which the current rises exponentially with field, and $V_R > 3$ kT, the current is given by [4, 11, 12]:

$$J_R = A^* T^2 \exp -q\left(\frac{\phi_B - \alpha E_B}{kT}\right) \tag{12.5}$$

where α is an effective tunnelling constant of $\sim$4 nm [11].

A further issue, particularly for a-Si:H SGTs made with the easily processable metals in common use in a-Si:H technology, is control of the zero-bias barrier height. For example, Cr on a-Si:H has a barrier of 0.91 eV, which is too high for useful operation of an SGT, and a lower barrier is needed. In single crystal Si technology, Schottky barrier heights can be readily modified by using shallow ion implantation to locally dope the Si surface [10, 13, 14], and the principles are

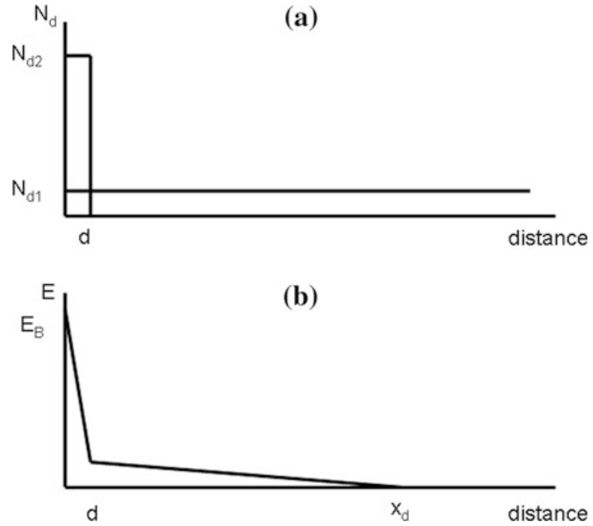

Fig. 12.4 Schottky barrier height control by shallow surface doping (**a**) idealised doping profile, and (**b**) field distribution with reverse bias, V_R

illustrated in Fig. 12.4. Figure 12.4a shows the approximate donor distribution for a shallow dose D (given by N_{d2}d), and its effect on the field distribution is shown in Fig. 12.4b. If the surface doping, N_{d2}, is much higher than the background doping, N_{d1}, then the latter can be ignored, and the maximum field, E_B, will be given by the integral of the dopant distribution within the fully depleted surface:

$$E_B \approx \frac{qN_{d2}d}{\varepsilon_s \varepsilon_0} \approx \frac{qD}{\varepsilon_s \varepsilon_0} \tag{12.6}$$

which, from Eq. 12.2, will reduce the barrier by [10]:

$$\Delta\phi \approx \frac{q}{\varepsilon_s \varepsilon_0} \sqrt{\frac{D}{4\pi}} \tag{12.7}$$

However, if the dose is large enough, the reduction in barrier height is accompanied by a reduction in barrier thickness, and this will enhance the tunnelling-based TFE process. Thus, the surface doping changes both the zero-bias barrier height, and its tunnelling transparency. For a-Si:H ion implanted with group V impurities, it was found that the empirical relationship between the ion dose and the effective reduction in Cr Schottky barrier height (calculated from the reverse bias currents) was [15]:

$$\Delta\phi \approx \frac{\alpha q D \gamma}{\varepsilon_s \varepsilon_0} \tag{12.8}$$

where α is the effective tunnelling constant, and γ was the fractional activity of the dopant, which reduced with increasing dose (in qualitative agreement with the gas phase doping of a-Si:H discussed in Sect. 5.5.2). It will be noted that Eq. 12.8 differs from Eq. 12.7, and this is partly because Eq. 12.7 gives just the direct

barrier height reduction. Whereas, the reverse bias current data, used to generate Eq. 12.8, gave an effective barrier height reduction, which implicitly included the contribution from enhanced TFE due to the barrier narrowing [15]. The practical control of barrier height in a-Si:H SGTs is discussed further in Sect. 12.4.

12.3 SGT Structure and Operation

12.3.1 Background

As is apparent from the chapters on conventional TFTs, contact resistance effects have been identified in all those structures, although their impact has been significantly larger in organic TFTs, where the contacts are Schottky diodes. Also, as mentioned in those chapters, a series resistance in the source and drain contacts influences the way in which the drain bias, V_{ds}, is distributed through the transistor structure. The voltage is divided between the channel and the contacts in a self-consistent way to ensure current continuity through these different regions. One direct consequence of this is that with a voltage drop, V_s, across the source contact, the effective gate bias at the source end of the channel is reduced to V_G-V_s. The potential drop along the channel is also reduced accordingly. In the case of the SGT, and organic TFTs with Schottky barrier contacts, the voltage drop V_s is developed as a reverse bias on the source barrier. Similarly, if there is a voltage drop, V_d, across the drain contact, this further reduces the potential drop along the channel, with its net value reduced to V_{ds}-V_s-V_d, for a drain potential V_{ds}.

Before considering the detailed analysis of SGT operation, it is useful to identify its most characteristic differences from conventional TFTs (which will simply be referred to as FETs in the rest of this chapter), and one of these is its lower saturation voltage. This is shown in Fig. 12.5 [1, 16] by the comparison of the measured output characteristics of an a-Si:H SGT and an a-Si:H FET (having the same dielectric and semiconductor film thicknesses of 300 nm and 100 nm, respectively). The FET had a threshold voltage of $\sim$4 V and a saturation voltage, $V_{D(sat)}$, of $\sim$6 V at $V_G = 10$ V (i.e. the usual dependence on V_G-V_T), whereas, at $V_G = 12$ V, the SGT had a saturation voltage of $\sim$1.5 V. Detailed analysis of these characteristics also showed that the SGT had a higher output resistance. A further difference was the lower current in the SGT, due to its barrier limited operation. In addition, the SGT had a g_m value, in saturation, which progressively increased with V_G. However, the saturation value of g_m displays a more varied dependence on V_G than indicated by this figure, and this is shown in Fig. 12.6a [4]. In the on-state, the saturation drain current increased exponentially with V_G, and this was reflected in the comparably increasing values of g_m. However, for gate biases between $\sim$5 V and $\sim$10 V, there was a small hump in g_m, and its overall value was almost constant. A schematic version of the g_m curve is shown in Fig. 12.6b, and it has been labelled to identify the different modes of operation of the SGT [17]. In particular, SGT1 represents the gate

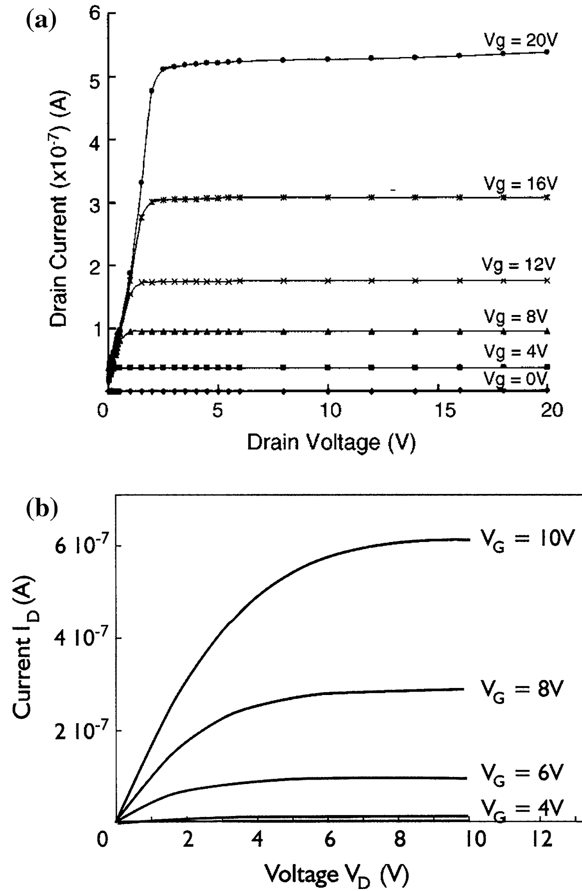

Fig. 12.5 Experimental output characteristics for a-Si:H devices (**a**) SGT, and (b) FET. [(**a**) Reprinted with permission from [16]. Copyright (2004) American Institute of Physics, and (**b**) Reprinted from [1] with permission of IEEE]

voltage range where g_m is steeply rising, and SGT2 denotes the region with the small g_m peak, around which g_m is almost constant. As will be discussed below, these represent two different modes of operation, with the SGT1 characteristics being due to gate-controlled barrier lowering of the source diode, whereas the SGT2 mode entails no barrier lowering [17]. These two operating regimes are reviewed in the following two sub-sections, starting with SGT1, which has been the focus of most of the published analyses.

12.3.2 SGT1 Mode

As stated above, this is the regime in which gate controlled lowering of the source barrier has been invoked to explain device behaviour [1–4]. The proposed mechanism is based upon a simple physical principle of using a reverse biased diode to

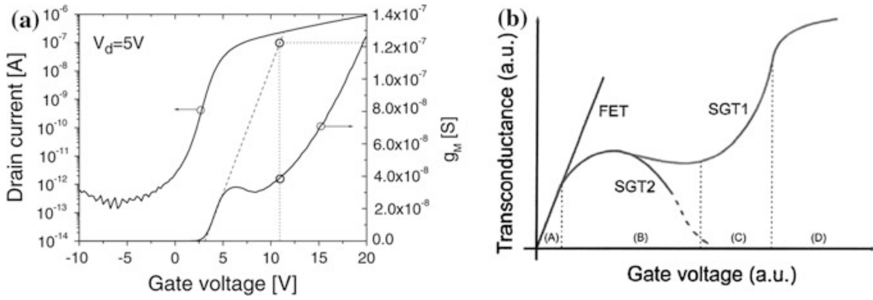

Fig. 12.6 **a** Gate bias dependence of the saturation values of drain current and g_m, measured in an a-Si:H SGT (Reprinted from [4]. Copyright (2006), with permission from Elsevier), and **b** schematic illustration of the g_m variation with gate bias. (Reprinted with permission from [17]. Copyright (2012), The Electrochemical Society)

deplete a thin layer, or sheet, of charge, Q_d, at a distance, t, from the diode. As a result of this depletion, the field at the diode increases in direct proportion to the density of depleted charge, Q_d. The most direct illustration of this is with a thin, highly doped layer in more lightly doped background material, similar to the situation shown in Fig. 12.4a, except that the highly doped region is not adjacent to the diode, but separated from it by a distance, t. Using Poisson's equation, and the depletion approximation, the reverse bias on the diode, $V_R(t)$, required to deplete just the background material doped with N_d donors to a depth t, is:

$$V_R(t) = \frac{qN_d t^2}{2\varepsilon_s \varepsilon_0} \tag{12.9}$$

And the electric field, $E_B(t)$, at the diode is:

$$E_B(t) = \frac{qN_d t}{\varepsilon_s \varepsilon_0} \tag{12.10}$$

To deplete the sheet of dopant, Q_d, at t, the increased reverse bias is:

$$V_R(t, Q_d) = \frac{qN_d t^2}{2\varepsilon_s \varepsilon_0} + \frac{qQ_d t}{\varepsilon_s \varepsilon_0} \tag{12.11}$$

And the increased electric field at the diode is:

$$E_B(t, Q_d) = \frac{qN_d t}{\varepsilon_s \varepsilon_0} + \frac{qQ_d}{\varepsilon_s \varepsilon_0} \tag{12.13}$$

Hence, for an increment in areal dopant concentration, ΔQ_d, the increase in reverse bias needed to deplete it, and the resulting increase in field at the diode, are given by the following equations:

$$\Delta V_R(t, \Delta Q_d) = \frac{q\Delta Q_d t}{\varepsilon_s \varepsilon_0} \tag{12.14}$$

$$\Delta E_B(t, \Delta Q_d) = \frac{q\Delta Q_d}{\varepsilon_s \varepsilon_0} = \Delta V_R(t, \Delta Q_d)/t \quad (12.15)$$

In the case of the SGT, the sheet of charge to be depleted is not due to a local spike in doping level, but is due to a carrier accumulation layer induced by the gate on the opposite side of the film from the diode. Hence, the operating principle of the SGT is that, for a given voltage on the gate, a particular reverse bias will be required on the source in order to deplete the accumulation layer induced by the gate. This will increase the field at the Schottky source contact, and, if the barrier height of the diode is field dependent, it will be reduced by the field, and the current over the barrier will increase. Once the drain bias is large enough for the voltage on the source to fully deplete both the film and the carrier accumulation layer beneath it, no further increase in reverse bias can be accommodated beneath the source. Hence, the device current will saturate at $V_{ds}=V_{ds1}$, and this has been described as a 'pinch-off' mechanism at the source [1–4].

Further increases in drain bias, beyond the source pinch-off voltage, V_{ds1}, will increase the film potential adjacent to the source, thereby reducing both V_G-V_s and the local carrier density in the FET channel. The reduced carrier density and higher lateral field self-consistently maintain an unchanged channel current [18]. The higher lateral field is a 2-D effect at the edge of the source adjacent to the channel, and the SGT operation relies upon the diode emission current not increasing with this lateral field. (This is discussed further below, and also in Sect. 12.6, in which the results of 2-D numerical simulations of SGTs and OTFTs are compared). Eventually, there will also be the conventional pinch-off of the FET channel at the drain, at $V_{ds}=V_{ds2}=V_G$-V_T, but this is barely visible in many output characteristics, such as those in Fig. 12.5a.

The following analysis extends the above qualitative discussion of SGT operation, and develops the relationship between the gate bias and the device saturation voltage at that gate bias [2, 4]. In this analytical treatment, the depletion approximation is used, and it is implicitly assumed that the channel resistance, for current flow between the source and the drain, is much lower than the source resistance, such that current flow is entirely controlled by the emission current over the reverse biased source diode.

The band bending, and the field distributions, below the source electrode in an a-Si:H SGT are shown in Fig. 12.7a–d, for the two situations where the drain bias is less than, and equal to the source pinch-off voltage, V_{ds1}, [1], respectively. In the former case (Fig. 12.7a, c), the centre of the film is field-free, and there is positive space charge at the top of the film, and negative space charge, plus an electron accumulation layer, at the bottom of the film. In this condition, at the insulator/semiconductor boundary:

$$\varepsilon_0 \varepsilon_i E_{i1} = \varepsilon_0 \varepsilon_s E_{s1} + Q_n \quad (12.16)$$

where Q_n is the electron accumulation layer density, E_{i1} is the field in the gate dielectric, and E_{s1} is the field in the semiconductor at the semiconductor/dielectric

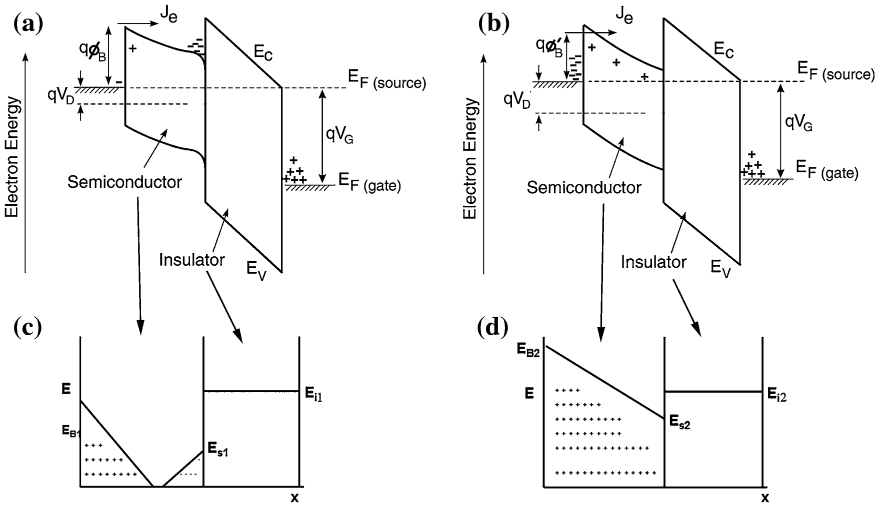

Fig. 12.7 Band bending in the SGT at (**a**) low and (**b**) saturation drain biases (Reprinted from [1] with permission of IEEE). Electrostatic field distribution in the SGT at (**c**) low and (**d**) saturation drain biases (E_{in} is the field in the dielectric, and E_{Bn}, and E_{sn} are the fields in the semiconductor at the Schottky and dielectric interfaces, respectively)

interface. When the electron accumulation layer is fully depleted by the source bias, the field-free region and the negative charge at the back surface are removed, and the condition at the insulator/semiconductor boundary becomes:

$$\varepsilon_0 \varepsilon_i E_{i2} = \varepsilon_0 \varepsilon_s E_{s2} \tag{12.17}$$

If the source is just pinched-off, and the gate bias is increased, further electrons are induced at the semiconductor/insulator interface, and the semiconductor film is no longer fully depleted. A further increase in drain bias is then needed to increase the reverse bias at the source, and to fully deplete the film. This establishes a new saturation voltage at the increased gate voltage.

With the assumption of a fully depleted film, the relationship between the gate bias and the saturation voltage can be calculated. However, the SGT situation is subtly different from that described by Eq. 12.11, in which the depletion of the free carriers left behind the ionised donor charge of density Q_d. For the SGT, the depletion of the accumulation layer (whose original density could be described by $V_G C_i$) means that the gate voltage is no longer dropped just across the dielectric, but is dropped across the series combination of the dielectric and the depleted semiconductor. Hence, by treating the series combination of the insulator and semiconductor capacitances (C_i and C_s, respectively) as a voltage divider [1, 2, 4], the change in potential across the Schottky barrier depletion layer, ΔV_s, for a change in gate bias, ΔV_G, is:

$$\Delta V_s = \Delta V_G C_i / (C_i + C_s) \tag{12.18}$$

In order to keep the film fully depleted, the increase in reverse bias, ΔV_s, across the diode is equal to the change in saturation voltage, $\Delta V_{D(sat)}=\Delta V_{ds1}=\Delta V_s$, required to deplete the charge induced by the gate. Thus, the relationship between gate bias and saturation voltage is [2, 4]:

$$\Delta V_{ds1}/\Delta V_G = C_i/(C_i + C_s) = R_V \tag{12.19}$$

This analysis is referred to as the 'dielectric model' [2].

The ratio, R_V, is a function of the insulator and semiconductor film thicknesses, and has a maximum value of unity when $C_i \gg C_s$, such that most of the voltage is dropped across the semiconductor film. In general, when $C_s > C_i$, R_V will be less than one, and can be reduced well below one by using a thin semiconductor layer compared with the insulator thickness (which is usually the case with a-Si:H TFTs). Indeed, for $C_s \gg C_i$, such that negligible voltage is dropped across the very thin and depleted semiconductor film, Eq. 12.19 becomes directly equivalent to Eq. 12.14 (and $C_i\Delta V_G = q\Delta Q_d$). In contrast to the values of $R_v < 1$ for the SGT, R_V is always ~ 1 for an FET. The measured values of R_V for two SGTs, with different a-Si:H layer thicknesses, are shown by the data points in Fig. 12.8 [2], and the lines are based upon Eq. 12.19 (with a SiN_x dielectric constant of 6.5). As shown, with a 100 nm thick a-Si:H film, a ratio of ~ 0.16 was achieved. These devices had a source-drain separation of <10 μm, and, as the results were controlled by the source barrier, rather than the channel length, the dependence on the source-drain separation within this range was minimal. However, as the source-drain separation is increased, the parasitic channel resistance increases, and the device becomes more FET-like. This is discussed further in Sect. 12.5.

From Eqs. 12.15 and 12.18, and the linear field distribution shown in Fig. 12.7d, the change in field at the source, ΔE_B, for a change in gate bias, ΔV_G, is given by [2]:

$$\Delta E_B = \Delta V_s/t_s = \Delta V_G C_i/t_s(C_i + C_s) \equiv \Delta V_{ds1}/t_s \tag{12.20}$$

where t_s is the semiconductor film thickness. Hence, for a fully depleted film, the surface field increases linearly with gate bias, and the value of E_B, at any value of gate bias, can be obtained directly from the measurement of the saturation voltage, V_{ds1}. From the current Eq. 12.5, the barrier height lowering, $\Delta\phi$, due to the gate bias can be calculated as [4]:

$$\Delta\phi = \alpha E_B = \alpha V_{ds1}/t_s \tag{12.21}$$

From Eqs. 12.5, 12.20 and 12.21, the SGT saturation current should increase exponentially with V_G due to the depletion of the charge at the semiconductor/dielectric interface by the reverse bias on the source diode. This strong dependence on V_G is shown in Fig. 12.5a. The effective tunnelling constant, α, in Eq. 12.21, will depend upon the internal field distribution, which will be determined by the details of the device fabrication process. Hence, α needs to be calculated for any given process, and it can be obtained from the slope of a plot of g_m against I_R, using the transfer characteristic measured in saturation [4]:

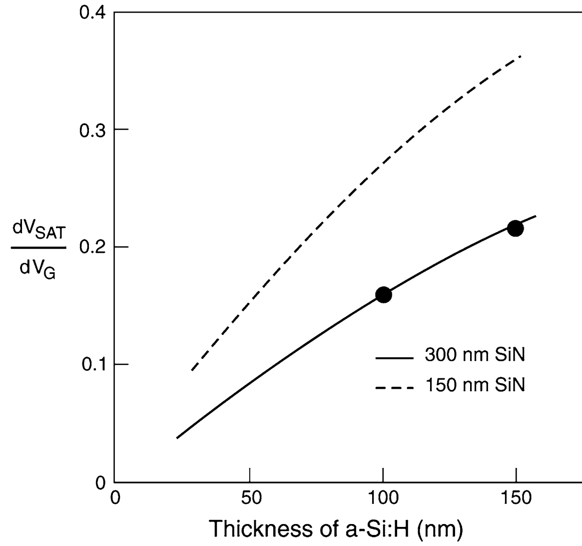

Fig. 12.8 Ratio of the differential change in SGT saturation voltage with gate voltage as a function of a-Si:H film thickness (data points). The lines are ratios calculated using Eq. 12.19. (Reprinted from [2]. Copyright (2004), with permission from Elsevier)

$$g_m = \frac{dI_R}{dV_G} = \frac{\alpha q I_R C_s C_i}{\varepsilon_0 \varepsilon_s kT(C_s + C_i)} \tag{12.22}$$

By inserting the calculated values of $\Delta\phi$ in Eq. 12.5, the zero-bias barrier height, ϕ_B, can be extracted from the effective barrier height, ϕ'_B (given by ϕ_B-αE_B) at any value of gate bias. An α value of ~2.2 nm was extracted from a set of a-Si:H SGT output characteristics, and the calculated values of ϕ_B and ϕ'_B are shown in Fig. 12.9a for a high barrier diode [4]. This figure shows a constant zero-bias barrier height of ~0.61–0.62 eV (which was determined by the fabrication process, and is discussed in Sect. 12.4), and the effective barrier height, ϕ'_B, varied linearly with gate bias, as expected from Eqs. 12.19 and 12.21.

The above analysis is based upon a 1-D analytical treatment, and would suggest that the current is uniform along the length of the source electrode. However, experimental measurements have shown that the current saturates with increasing source length, and 2-D simulations have demonstrated that this is because the current is localised towards the channel end of the source electrode [18]. The other 2-D effect, as mentioned above, is the increased lateral voltage drop at the source junction, as V_{ds} is increased above the SGT source pinch-off voltage, V_{ds1}. This continues until the conventional pinch-off occurs at the drain (at $V_{ds} = V_G$-$V_T = V_{ds2}$), after which the lateral voltage drop across the source also saturates. In spite of the increasing lateral field at the source between the V_{ds1} and V_{ds2}, the reported measurements and simulations have not shown an increase in transistor current. This is in contrast to the OTFT measurements and simulations discussed in Sect. 12.6, and the relative insensitivity of the SGT current to the field at the edge of the source is the key difference between OTFTs and SGTs. However, it should be noted that field relief architectures at the diode edge have been advocated [1], and their implementation in

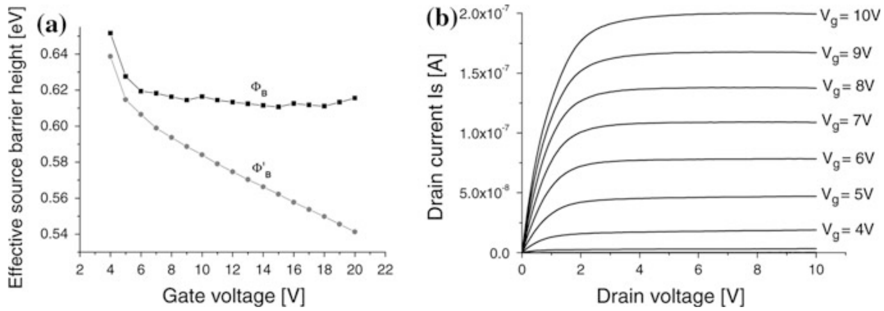

Fig. 12.9 **a** Variation of zero-bias barrier height, ϕ_B, and effective barrier height, ϕ'_B, with gate bias, calculated from experimental a-Si:H SGT characteristics, and **b** experimental a-Si:H SGT2 mode output characteristics (d = 2 μm, and 4×10^{14} P^{31}/cm^2 barrier lowering implant). (Reprinted from [4]. Copyright (2006), with permission from Elsevier)

poly-Si SGTs has been demonstrated to have a major effect upon the SGT characteristics [19]. In particular, in both experimental measurements and 2-D simulations, the field relief architecture was essential to obtain the characteristic low saturation voltage of the SGT. Without this field relief, SGT-like behaviour was lost, and the saturation voltage was at the conventional TFT value of V_G-V_T [19]. However, it is not evident that explicit field relief has been implemented in any of the measurements or simulations of a-Si:H SGTs discussed in this section. On the other hand, the doping of this material will produce different net dopant and DOS densities across the source/channel boundary. In particular, there is the shallow P^+ doping beneath the source electrode, but also B^+ doping in the channel region to compensate the local P^+ doping [2] (see Fig. 12.10 and Sect. 12.4).

As discussed in Sect. 5.5.2, the doping efficiency of heavily doped a-Si:H is low, and the active phosphorus sites result from the formation of dopant-dangling bond pairs, P^+-D^- [21]. In contrast, compensated material will have a higher doping efficiency, with the formation of P^+-B^- pairs, rather than P^+-D^- pairs, giving a lower defect density, but broader band-tails [20, 21]. The preferential formation of the P^+-B^- pairs also leads to very accurate compensation, even when the total dopant densities are not accurately matched [21]. Precisely how these differential dopant and defect densities either side of the source/channel boundary would affect the field has not been evaluated, but the lower defect density, and the accurate compensation of electrically active dopants in the channel area, should give a lower space charge density, and hence a lower field, on the channel side of the source electrode. The experimental results would indicate that the net effect is field relief on the channel side of the junction in a-Si:H SGTs. Although this argument can be made for implicit field relief in the experimental a-Si:H SGTs, it is not clear why there is not continued barrier lowering, for V_{ds} values greater than V_{ds1}, in the a-Si:H SGT simulations, where the material is treated as spatially uniform. This remains an unresolved discrepancy with respect to simulations of staggered OFETs, and is discussed further in Sect. 12.6.

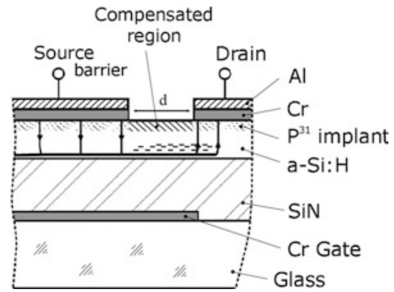

Fig. 12.10 Cross-section of an a-Si:H SGT. (Reprinted from [24])

12.3.3 SGT2 Mode

In contrast to the SGT1 mode, there is no gate-induced barrier lowering in the SGT2 mode, and the g_m value in saturation is approximately constant [4, 17]. This latter feature is a consequence of the saturation current varying linearly with gate bias, as shown in Fig. 12.9b [4]. Operation in the SGT2 mode is shown schematically in Fig. 12.6b [17], in which, at low gate bias in region A, the device operation is initially limited by the parasitic FET channel. In this regime, there is a small device current, which can be supplied by the Schottky diode operating just above zero reverse bias. However, as the gate bias increases, the FET current would linearly increase, and more current would need to be drawn from the Schottky source diode (in regime B). Thus, its reverse bias would increase by a few kT until the maximum, low-bias saturation current is drawn. The current will flow across the film and along the carrier accumulation layer at the semiconductor-dielectric interface beneath the source. This will layer act like a JFET, with saturation occurring when the layer is pinched-off at the channel edge of the source, where there is the greatest reverse bias [17]. In the absence of any further effect, the current through the structure would be limited by this low-bias diode current, and g_m would progressively fall to zero, producing the peak in the g_m curve. However, with increasing gate bias, the charge at the interface becomes sufficient to start lowering the source barrier, and the transition to SGT1 occurs [17].

The other point to note is that the absolute magnitude of the low-bias diode current is also a function of the source length, and of the diode's zero-bias barrier height. Hence, the longer the source, or the lower the barrier, the greater will be the gate voltage range over which the SGT2 mode is observed [17]. This mode has been seen experimentally, particularly where ion implantation has been used to produce low barrier devices, as shown in Fig. 12.9b [4].

The operation of constant g_m SGTs has been independently reported in other 2-D simulations, and these accurately modelled experimental characteristics similar to those shown in Fig. 12.9b [22]. The simulated carrier and potential distributions also confirmed that for drain biases above the saturation voltage, the carrier depletion was greatest towards the edge of the source contact, where the channel potential also continued to rise. As barrier lowering was not employed in these particular simulations, it was concluded that the SGT effect was simply due to a

large gate-controlled series resistance in the depletion region beneath the source contact [22]. However, as this analysis was carried out before the distinction between SGT1 and SGT2 modes was identified, the conclusion of simple gate-controlled series resistance applies, at best, to the SGT2 mode only. Moreover, recent analysis has concluded that Schottky source barriers, in any TFT structure, cannot be represented as a simple resistor, but should be represented by a more complex resistor/diode network [23], and this is discussed further in Sect. 12.6.

12.4 Fabrication Process

SGTs have been made with both a-Si:H and poly-Si, and one of the key features of the process, namely, the control of the zero-bias barrier height, was the same. In view of this, and the fact that the SGT process is of greater interest with low mobility materials [3], the process will be illustrated with a-Si:H. (Details of the conventional a-Si:H TFT technology can be found in Chap. 5).

A cross-section of an a-Si:H SGT is shown in Fig. 12.10 [24]. This is an inverted staggered structure, and its main features are the overlap length, S, of the gate and source electrodes, the separation, d, of the source and drain electrodes, the source barrier metal, and the phosphorus, P^{31}, implant used to control the zero-bias source barrier height. As discussed in Sect. 12.2, surface ion doping is a well-established technique for controlling the zero-bias barrier height of Schottky diodes, and has been used with both the a-Si:H [2, 15] and poly-Si [5, 6] SGTs. Measurements of the effective, zero-bias barrier height as a function of phosphorus dose, D, in a-Si:H with a Cr Schottky contact, are shown in Fig. 12.11 [2]. The low dose results (circles) were taken directly from Schottky diodes [15], and the higher dose results (triangles) were extracted from SGT measurements, using the procedure discussed in Sect. 12.3.2 [2]. These are referred to as effective barrier heights, as they have been derived from reverse-bias current measurements, and implicitly contain the effects of barrier thinning, as well as height reduction. In other words, although the current flow is assumed to be by TFE, the effective barrier height is the value which would be required to give a TE current of the same magnitude. Over the extensive dose range of the measurements, the barrier height was found to scale with log D, and this weak dependence facilitated accurate dose control of the barrier height [2].

The fabrication stages, for the structure shown in Fig. 12.10, initially followed a standard a-Si:H TFT process, and were [2]:

- Cr gate deposition and patterning (M1)
- PECVD deposition of SiN_x (300 nm) and a-Si:H (100–150 nm)
- Patterning of a-Si:H, and contact window opening to gate (M2, M3)
- Unmasked P^{31} ion implantation at 10 keV
- Cr source and drain deposition, and patterning (M4)
- BF_2^+ implant at 12 keV between S and D metal to compensate P^{31}
- Anneal at 250 °C for 30 min

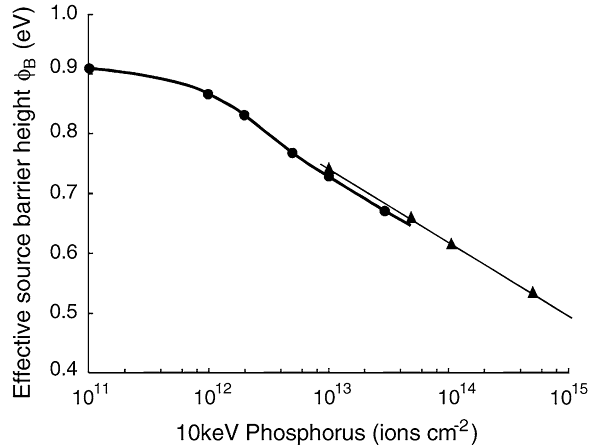

Fig. 12.11 Variation of the zero-bias barrier height, in Cr/a-Si:H Schottky contacts, with low energy P^{31} ion dose. (Reprinted from [2]. Copyright (2004), with permission from Elsevier)

This was a 4-mask process, and, in this example, the drain was a Schottky barrier diode, which was forward biased during device operation. The P^{31} implant was unmasked, and applied to the whole plate. To prevent this highly doped region from shorting the source and drain contacts, a compensating dose of BF_2^+ was implanted between them, using the Cr electrodes as an implant mask. A combined dopant activation and damage anneal stage was optimised at 250 °C [15]. The finished devices had source/drain gaps, d, of 2–10 μm, the gate/source overlap, S, was 5 μm, and the source width was 12–600 μm.

The poly-Si SGTs [5, 6] had a similar processing schedule, with one key difference being the implementation of the barrier lowering implant. For the poly-Si SGTs, the low energy P^{31} implant was through a window in a passivating SiO_2 layer on top of the device island, where the window defined the source area. As the implant was localised in the source area, this obviated the need for a compensating BF_2 implant. The source metal was subsequently defined over this window, and the size of the source metal pad was designed to ensure that it overlapped the edge of the implant window. As discussed in Sect. 12.3.2, this architecture was shown to give field relief around the edge of the source electrode [19].

From the above processing details, it is evident that SGT fabrication can be implemented within standard TFT processing facilities, providing the semiconductor film is thin enough to be depleted by modest reverse biases on the source electrode. In addition to this fundamental requirement, the other issues are the possible use of a barrier lowering implant, and a photo-lithography process capable of yielding small source-drain separations, d. With the appropriate selection of the source metal, barrier lowering implantation would not be necessary, but ion doping is, nevertheless, a routine stage in poly-Si TFT processing [25]. However, even in the absence of an ion doping stage, it is suggested that the source electrode should be overlapped onto an adjacent dielectric layer, as this would achieve the field relief architecture demonstrated with the poly-Si SGTs [19]. Higher resolution lithography is also available for the smaller plate sizes used

in poly-Si TFT fabrication [26]. Although poly-Si has been mentioned in the context of ion doping and higher resolution lithography, it should be noted that this was solely to demonstrate that equipment for these processes is readily available, and not to imply that poly-Si would be the preferred material for SGTs. Indeed, it has been argued that low mobility organic materials could benefit the most from the SGT structure [3, 28].

12.5 Comparison of SGT and FET Characteristics

Section 12.3 highlighted the differences in saturation voltage between FETs and SGTs, and, in this section, the wider differences and similarities are looked at more generally, and are illustrated with experimental examples taken from a-Si:H. In the preceding sections, it has been emphasised that SGT behaviour is observed when the injection resistance is the controlling resistance, and the parasitic channel resistance between the source and drain contacts was kept low by keeping the gap, d, between 2–10 μm. However, as the separation increases, the parasitic channel resistance increases, and this will begin to limit SGT behaviour. Ultimately, when the gap is large enough, the channel resistance will control the drain current, and the device will display FET behaviour. This transition from SGT to FET behaviour can be readily observed in the dependence of the ratio R_V ($dV_{D(sat)}/dV_G$) on the source-drain separation, d (where R_V is <1 for the SGT, and equal to one for the FET). This is seen in the variation of the measured values of R_V with d in Fig. 12.12a, with it increasing from the SGT value of ~ 0.2, at small channel lengths, to conventional FET behaviour ($R_V = 1$) at channel lengths of 100 μm [27]. The same behaviour is shown by the 2-D device simulations in Fig. 12.12b, in which R_V increased from the SGT value of ~ 0.1 (in good agreement with the capacitor ratio in the dielectric model), to the FET value over a comparable range of d. (In the simulations, the a-Si:H thickness was 60 nm, compared with 100 nm in experimental devices, which is why the capacitor ratio was lower in the simulations). Hence, as the channel resistance between the source and drain terminals increased, there was a transition from SGT to FET behaviour, at the end point of which the drain current was controlled solely by the channel resistance. Conversely, to maintain SGT behaviour, the source-drain separation must be kept small.

There are two direct implications for device operation in the SGT mode, which are that, for a given source-drain separation, the SGT current is, by definition, less than the FET current, and that, at small separations, the SGT current will be largely independent of that separation. In contrast, the current in an FET should scale inversely with channel length, and, therefore, control of channel length is a critical aspect of the FET process for ensuring good device uniformity. Both the measurements and simulations in Fig. 12.12a, b, respectively, confirmed the weak dependence of device behaviour on small values of d, and this is seen more clearly in the simulated SGT output characteristics in Fig. 12.12c [27]. The values of d were varied from 0.5 μm to 2.0 μm, and there were minimal differences in the

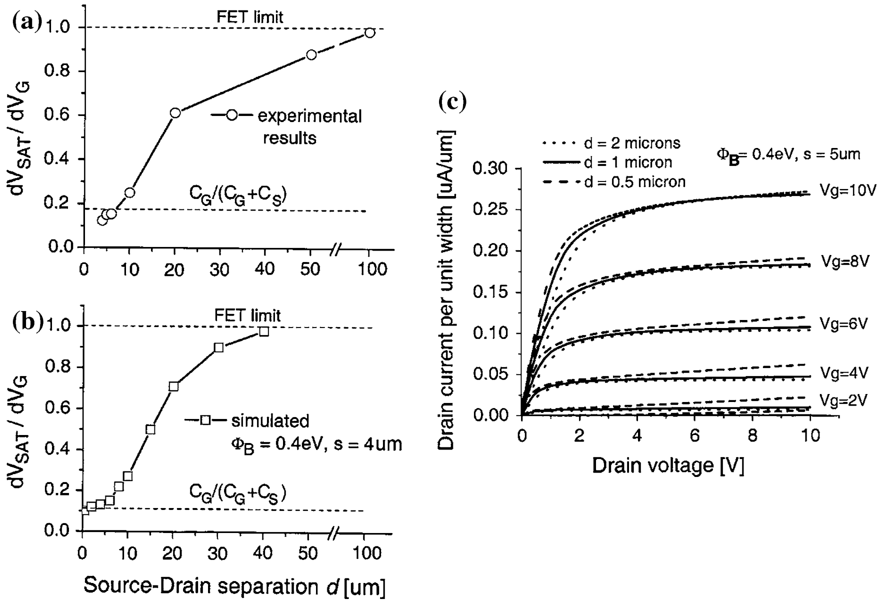

Fig. 12.12 Variation of the ratio R_V with source-drain separation: **a** experimental a-Si:H data (t_s = 100 nm, t_i = 300 nm), **b** 2-D simulations (t_s = 60 nm, t_i = 300 nm), and **c** simulated SGT output characteristics for different values of the source-drain separation, d. (Reprinted with permission from [27]. Copyright (2005) American Institute of Physics)

characteristics, including the absence of short channel effects at the smallest d value. This will not occur in an FET, due to channel shortening, and eventual drain-induced barrier lowering. These differences are illustrated in Fig. 12.13, showing simulations of the output characteristics of short channel SGTs and FETs, with d = L = 250 nm [3]. The SGT continued to show good current saturation, which was entirely absent from the FET due to strong short-channel effects. The short-channel effects in the FET, in Fig. 12.13b, were, in part, related to the thick gate dielectric of 120 nm. As discussed in Sect. 8.7, short channel effects can be reduced by scaling the dielectric layer thickness with the channel length. However, what is notable about the SGT is that this scaling is not required, and thick dielectric layers can be successfully used with small source-drain separations [3]. This can be particularly useful with low quality dielectrics, where thick layers may be needed to suppress leakage currents and pin-holes [28].

Equations 12.4 and 12.5 show that the SGT current increases exponentially with decreasing barrier height, and, to ensure adequate drain currents, the reduction of the zero-bias barrier height by ion implantation is an important part of the device design. To compare the differences in SGT and FET currents, Fig. 12.14 shows the scaling of SGT currents with ion dose, and the scaling of FET currents with channel length [2]. This indicates that the saturation current from an a-Si:H SGT, with a barrier lowering implant of 5×10^{14} P/cm^2, is the same as from an

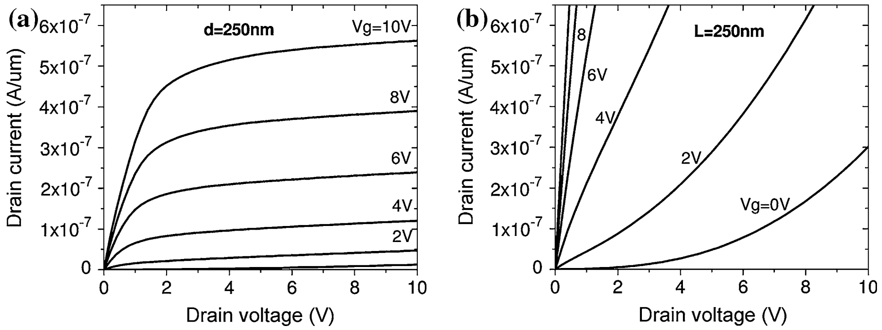

Fig. 12.13 Simulated output characteristics of short-channel a-Si:H devices (**a**) SGT, d = 250 nm (t_s = 40 nm, t_i = 120 nm, and ϕ_B = 0.35 eV), and (**b**) FET, L = 250 nm. (Reprinted from [3] with permission of IEEE)

a-Si:H FET with a 15 μm channel length. Hence, moderately high-current SGTs can be fabricated, although, as discussed in Sect. 12.3.3, these will be low zero-bias barrier devices, which will operate in the SGT2, constant g_m, mode over a broad range of V_G values.

Finally, due to the reduced free carrier concentration in the channel region beneath the source in SGTs, there should be improved gate-bias stability in those devices in which the instability is driven by Fermi level dependent trap generation, such as a-Si:H. (See Sect. 6.4.1 for a discussion of bias stability effects in a-Si:H TFTs). As already discussed, the SGT saturation voltage is determined by carrier depletion at the source, but, at drain biases greater than V_G-V_T, there is also carrier depletion at the drain. This is not only another factor improving the output impedance of the SGT [1], but it also substantially depletes the channel of carriers as well. The differences in carrier concentrations along the channel, in SGTs and FETs, are shown by the simulations in Fig. 12.15a, b, and the field distributions are shown in Fig. 12.15c, d [3]. At drain biases >7.5 V, the carrier concentration along the SGT channel is lower than in the FET, and particularly so at the source, where the concentration is highest in the FET. These differences result in superior gate-bias stability in a-Si:H SGTs compared with FETs, as shown by the bias-stress results in Fig. 12.16 [9]. For each of these measurements, the gate bias was adjusted to give the pre-stress drain current shown on the x-axis, and the drain bias was also large enough to ensure saturation. The change in drain current was then measured after 24 h combined gate and drain bias stressing. As seen in the figure, the reduction in drain current was just a few percent in the SGT, even at the highest current (and carrier densities), compared with >20 % in the FET [9].

In summary, the SGT displays markedly different behaviour from a conventional FET, providing the source-drain gap is small enough for the channel resistance to be significantly smaller than the injection resistance. However, as the channel resistance increases, the device becomes increasingly FET-like in its behaviour. When the SGT mode of operation is maintained, the device shows some clear advantages over an FET, namely:

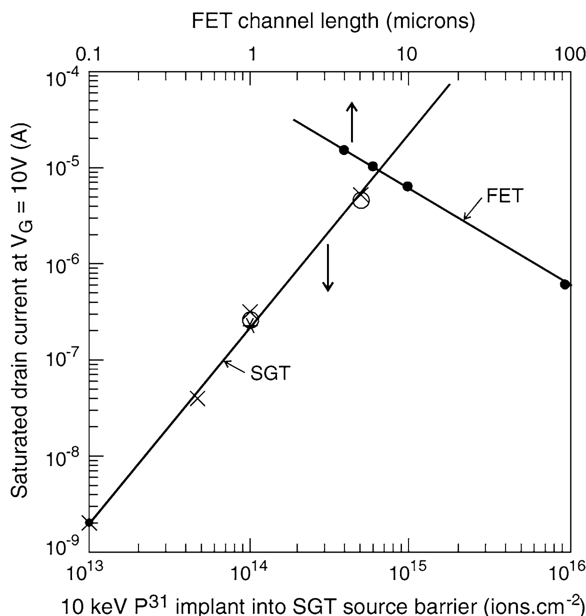

Fig. 12.14 Comparison of drain currents measured in a-Si:H SGTs and FETs as a function of barrier lowering implant dose and channel length, respectively, (V_G = 10 V, W = 600 μm). (Reprinted from [2]. Copyright (2004), with permission from Elsevier)

- Lower saturation voltage, giving lower voltage operation, and reduced power consumption in circuits.
- Higher output impedance, giving higher g_m/g_d ratios
- Reduced short channel effects
- Improved gate bias stability

When these features are considered as a package, it has been argued that they address many of the problems experienced with a-Si:H FETs driving AMOLED pixels, and that the a-Si:H SGT is better suited to this application [29]. A further proposed application is in low power, high gain analogue circuits, which would benefit from the high voltage gain offered by the large output impedance [19]. Finally, in disordered materials, such as organic semiconductors, in which carrier transport is by hopping, and the carrier mobility is a function of the lateral field [30, 31], the SGT has been predicted to offer improved on-currents and frequency response compared with FETs [3, 28].

12.6 Gate/Source-Barrier Interactions in OTFTs

As all the published work on the SGT has come from one research group, it is useful to consider how the properties and operating principles of these devices compare with analyses of other TFT structures. The nearest equivalent device structures are organic TFTs implemented with a short channel, staggered TFT architecture, and with the normal Schottky barrier contacts. Given the injection

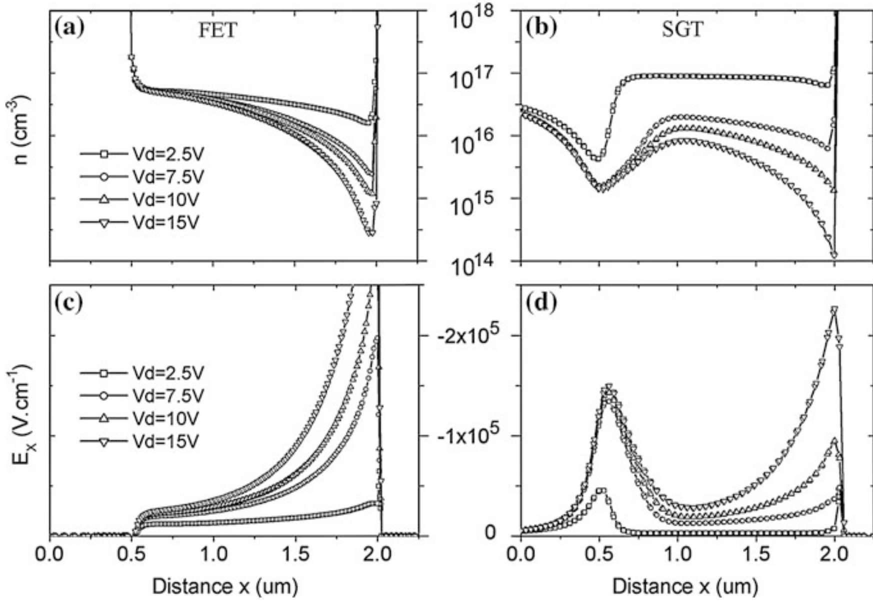

Fig. 12.15 Simulated carrier concentrations, between the source-drain regions, in (**a**) the FET, and (**b**) the SGT, and the lateral field distributions in (**c**) the FET, and (**d**) the SGT. ($S = 2$ μm, the source edge is at $x = 0.5$ μm, $L = d = 1.5$ μm, and $\phi_B = 0.45$ eV). (Reprinted from [3] with permission of IEEE)

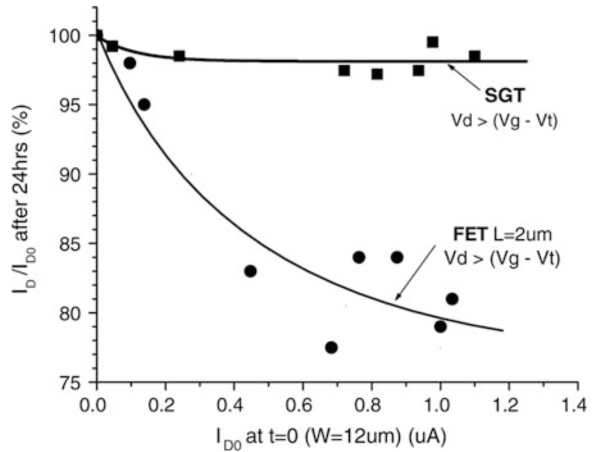

Fig. 12.16 Comparison of gate bias stress instability measurements in a-Si:H SGTs and FETs ($d = L = 2$ μm). (Reprinted from [9]. Copyright (2008), with permission from Elsevier)

problems identified with these structures, particularly as the channel length reduces, limited attention has been paid to short channel devices, and no examples of unambiguous SGT-like behaviour have been reported. Indeed, the emphasis in much of the OTFT work has been to keep the injection barrier as low as possible, so that classical TFT behaviour is observed, and barrier limited behaviour has been

avoided in the pursuit of high performance TFT structures. However, as mentioned in Sect. 10.5.3, there is now increasing recognition of the interaction between the gate bias and the barrier height in OTFTs [23, 32–35], which is the essential feature of SGT operation. All these publications have modelled the influence of the gate bias on the source barrier height, but, from the SGT perspective, the most relevant is Ref. [34] as it directly evaluated the change in injection barrier height at drain bias values large enough to ensure that the device was in saturation. In the other publications [33, 35], the drain bias was low, and many of the calculations were in the linear regime.

In order to clarify source contact effects, the characteristics of TG/BC OTFTs, with 60 nm thick, printed TIPS-pentacene films and Au contacts, were studied over the channel length range 10–200 μm [34]. The transfer characteristics of the longest channel devices showed perfect agreement with the standard MOSFET equation, whilst the shortest channel devices did not fit this simple model. This was attributed to barrier controlled operation in the $L = 10$ μm devices, and their non-standard output characteristics are shown by the data points in Fig. 12.17a. These characteristics are neither those of a classical TFT nor an SGT, and have been attributed to a device in which both the channel resistance and the barrier injection resistance play a strong role in determining the overall device behaviour. In order to interpret this behaviour, 2-D simulation was used, with a model which linked the lowering of the source barrier to the local electrostatic field, and included the Schottky effect, as well as trap and phonon assisted tunnelling [34]. The solid lines in Fig. 12.17a were the best fit to the data using a 0.46 eV Schottky barrier source, with field-induced barrier lowering. The importance of barrier lowering is shown by the broken lines, which were calculated with the barrier lowering switched off, and demonstrated that only at low drain bias could the experimental characteristics be modelled without barrier lowering. Indeed, for drain bias values above $\sim$2 V, the field-induced source barrier lowering was a key feature of the data fit. The drain bias dependence of the potential through the thickness of the TIPS-pentacene film (above the source edge, at $V_G = -44$ V), is shown in Fig. 12.17b (where the inset shows the location of the cut line). This data was also used to compute the reduction in source barrier height, which continuously fell with drain bias, with a maximum reduction of 150 meV at $V_d \geq -30$ V. In contrast, the barrier lowering at a drain bias of 0.1 V was only $\sim$2 meV, demonstrating that barrier lowering was due to the combined effects of gate and drain bias. The saturation in barrier lowering occurred when the channel at the drain pinched-off (at $V_{ds} = V_G - V_T = -30$ V), such that further increases in drain bias were localised at the drain junction, and the reverse bias on the source saturated. The simulations at $V_G = -44$ V also showed that the hole density was depleted from the semiconductor/dielectric interface above the source electrode, and that current injection was predominantly from the source edge in the vicinity of the cut-line in the insert in Fig. 12.17b [34].

The data shown in Fig. 12.17b has been interpreted in terms of a distributed diode/resistor network at the source terminal, where the resistor values were determined by the gate bias [23]. At low drain bias, the increase in TFT current

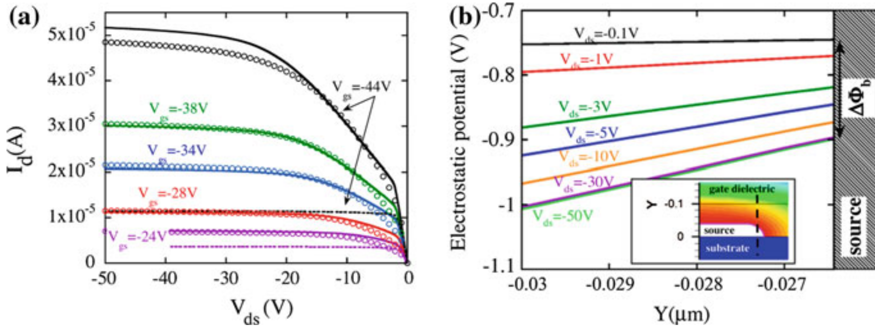

Fig. 12.17 **a** Measured (*circles*) and simulated (*lines*) output characteristics of a TIPS-pentacene TFT with L=10 μm (solid and dashed lines are with and without barrier lowering, respectively), and **b** cut lines of the electrostatic potential through the pentacene film near the edge of the source contact (as shown by the inset), and the calculated change of the source barrier height with drain bias, V_{ds}. (Reprinted from [34]. Copyright (2012), with permission from Elsevier)

with increasing gate bias (the broken lines in Fig. 12.17b) has been attributed to a spreading resistance effect along the source electrode, in which the increasing gate bias reduced the channel resistance above the source, and, thereby, extended the effective emitting length of the source diode. Hence, the gate-bias-dependent saturation currents (in the absence of barrier lowering) were due to the increasing effective source area. With barrier lowering switched on, the current increased above these saturation levels, but, under all bias conditions, the greatest potential across the diode network was at the channel end of the source electrode, and, with increasing drain bias, this point pinched-off first at V_{ds1}, giving the inflection point in the output characteristics. The pinch-off also defined the effective diode area, which did not increase with further drain bias. Following pinch-off at the source, further increases in drain bias increased the floating potential at the channel end of the source, producing a larger electrostatic field at this point. This resulted in progressive field-induced lowering of the source barrier, as shown in Fig. 12.17b, and gave the increased device current shown by the solid lines in Fig. 12.17a [23]. Once the channel pinched-off at the drain, at V_{ds2}, the reverse bias on the source saturated, and the total device current also saturated.

The OTFT data summarised above shows some features in common with the SGT model, such as the low voltage pinch-off at the edge of the source (due to reverse bias depletion of the hole accumulation layer), the field induced barrier lowering due to the combined effects of the gate and drain biases, and the saturation of the reverse bias at the source once pinch-off occurred at the drain. However, there are detailed aspects of the inverted OTFT behaviour which are quite different from the SGT data. The most important difference is the continued reduction in source barrier height for drain biases in excess of the source pinch-off voltage, V_{ds1}. It will be appreciated that for drain biases in the range $V_{ds1} < V_{ds} < V_{ds2}$, the voltage for both the OTFT and the SGT will be divided between the channel and the source diode in order to self-consistently give current

continuity through these two regions. The main difference between the two structures is that with the lower relative channel resistance in the SGT, a larger fraction of the drain voltage in excess of V_{ds1} will be dropped across its source. Hence, for both the OTFT and the SGT, the field at the channel edge of the source will continuously increase beyond V_{ds1} until the channel is pinched-off at the drain. In spite of this similarity, the current in the SGT appears to saturate at V_{ds1}, whereas it saturates at V_{ds2} in the OTFT.

Another 2-D numerical simulation of staggered OTFTs [35] showed similar results to those discussed above [34], although an effective 'contact' resistance, rather than a barrier height, was evaluated. In this case, the simulations were of a BG/TC pentacene TFT, containing a 30 nm thick film, a 5 μm channel length, a source barrier of 0.6 eV, and field-induced barrier lowering due to both the Schottky effect and direct tunnelling [35]. The simulations showed TFT-like characteristics, and a 'contact' resistance, which was a function of both the gate and drain biases, and which continuously reduced with drain bias up to the drain saturation voltage (due to the increased reverse bias at the edge of the source). The emission current was also concentrated at the channel edge of the source electrode, where the field and barrier lowering were greatest. Once again, saturation in source 'contact' resistance and device current only occurred after pinch-off at the drain.

The low saturation voltage, V_{ds1}, of the SGT is a key feature of its behaviour, and, in the published work on barrier-limited-operation of staggered OTFTs, discussed above, the saturation voltage is at the conventional TFT saturation voltage of V_G-V_T (i.e. V_{ds2}). Nevertheless, in both the SGT and the OTFT simulations, field-induced lowering of the source barrier (due to the combined action of V_G and V_{ds}) has been demonstrated, and the field at the edge of the source (adjacent to the channel) has also been shown to increase with drain bias up to the drain saturation voltage, V_{ds2}. However, barrier lowering for drain biases between V_{ds1} and V_{ds2} has only been found in the OTFT, and not in the SGT. This key difference in barrier lowering at the source edge between the SGT and the OTFT is best explained in terms of field relief around the edge of the source electrode in the SGT. Considering the experimental results for a-Si:H [2, 4] and poly-Si SGTs [19], a field relief architecture for the source electrode was explicitly identified in the poly-Si devices as essential for SGT operation. Without this field relief, there was continued reduction of the source barrier height at the channel edge for V_{ds} values between V_{s1} and V_{s2} [19]. This is in good agreement with the OTFT simulations [23, 34, 35]. For the a-Si:H SGTs, there was no direct field relief structure, but the process technology, involving a compensating implant in the channel, introduced a different DOS, as well as a net difference in dopant density, across the source/channel boundary, and is very likely giving implicit field relief. On the strength of these experimental SGT results, it is apparent that the most reliable route for obtaining SGT behaviour in any material, including organic semiconductors, is by the incorporation of a field-relief architecture into the device structure. This is not implemented in conventional organic TFTs, and is the most likely explanation for the absence of reported SGT-like behaviour in these structures.

So far as the SGT simulations are concerned, as mentioned above, the poly-Si simulations (without field relief) show good agreement with the relevant OTFT simulations. However, neither the a-Si:H [18] nor the organic SGT [28] simulations appear to incorporate explicit field relief, and do not show barrier lowering for V_{ds} values beyond V_{s1}. In both cases, an appropriate zero-bias barrier height was chosen, with a uniform DOS through the material and across the source/channel boundary. The a-Si:H simulations [18] appear to be in the SGT2 mode, where gate bias dependent barrier lowering is absent [17], but it is not clear why the device should be insensitive to the field at the edge of the source induced by the drain bias. Hence, whilst the experimental results for both a-Si:H and poly-Si SGTs, as well as the simulations of poly-Si SGTs, can be reconciled with the OTFT simulations, there remains an unexplained difference between the simulations of OTFTs and the simulations of both a-Si:H and organic SGTs.

In summary, it has been argued that, when the influence of field relief at the edge of the source electrode in experimental poly-Si and a-Si:H SGTs is taken into account, the behaviour of OTFTs and SGTs can be reconciled. Hence, by implication, in order to realise the particular features associated with the SGT-mode of behaviour, the explicit incorporation of field relief into organic semiconductor device structures appears to be necessary.

12.7 Summary

The source-gated transistor, SGT, is a type of staggered thin film transistor, which has a barrier contact at the source, rather than the more conventional ohmic contact of TFTs. The height of this barrier is controlled by the reverse bias on the source diode depleting the accumulation layer induced by the gate voltage. As a consequence of this dependence on the gate and source biases, the device has markedly different behaviour from conventional TFTs: it has a lower saturation voltage, higher output impedance, reduced short channel effects, and its current is insensitive to modest variations in the source-drain separation. The experimental implementation of the structure has been with a-Si:H and poly-Si, using Schottky barrier contacts, and the device behaviour has been investigated using 2-D simulations.

The SGT architecture is an inverted staggered structure, and, in the barrier-lowering, SGT1, mode, the analysis of device behaviour demonstrated that the overlap of the gate and source electrodes enabled the source barrier height to be controlled by the gate voltage. This meant that the device current saturated due to pinch-off at the source, when the carrier accumulation layer beneath it was fully depleted by the reverse bias on the source electrode. Current flow from the source to drain terminals was facilitated by the conducting channel between them, also induced by the gate voltage (as in a conventional TFT). However, for the observation of SGT behaviour, this parasitic channel resistance has to be less than the effective injection resistance. This places a premium on small source-drain separations, but, providing the channel resistance is small, the precise size of this gap is

unimportant. On the other hand, with an increasing gap, the device eventually tends towards conventional TFT behaviour, as the channel resistance approaches and/or exceeds the injection resistance.

The architecture of the SGT is much the same as a staggered organic TFT, which customarily has a Schottky barrier source contact. In spite of the extensive investigation of OTFTs, it should be noted that SGT-like behaviour has not been reported in these structures. Although gate-bias-dependent source barrier lowering has been identified in OTFTs, there is an important difference in the way in which the barrier lowering continues to increase with drain bias after the source has pinched-off in the OTFT. On the other hand, in the SGT, the barrier lowering saturates at source pinch-off. It should also be noted that the increase in lateral field at the source is qualitatively identical in both structures, and only saturates when the there is pinch-off at the drain. This apparent contradiction in behaviour between these two classes of similar device has been explained by the presence of field relief around the edge of the source electrode in experimental SGT structures. This is explicitly present in poly-Si SGTs, and it is argued that it implicitly arises in the ion doping technology used for fabricating a-Si:H SGTs. One conclusion that can be drawn from this is that SGT-like behaviour, in devices using organic semiconductors, is more likely to be seen if field relief is also incorporated into their source electrodes. As a corollary to this, it is suggested that the absence of such structures in conventional OTFTs is why SGT behaviour has not been reported in them.

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