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On-chip High-Voltage Generator Design

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To the memory of my father

Preface

Accordingly, as silicon technology has been advanced, more and more functionalities have been integrated into LSIs. On-chip multiple voltage generation is becoming one of big challenges on circuit and system design. Linear or series regulator is used to convert the external supply voltage into lower and more stable internal voltages. As the number of gates operating simultaneously and the operation frequency increase, AC load current of the regulators also increases. Low-voltage operation and rapid load regulation are becoming design challenges for the voltage down convertors. Another type of voltage generator is high-voltage generator or voltage multiplier whose output is higher than the input supply voltage. The voltage multipliers are categorized into two, switching convertor and switched capacitor, with respect to the components used. The former uses an inductor, switch or diode, and AC voltage source whereas the latter uses a capacitor instead of the inductor. Even though the switching convertor has been widely used with discrete chip inductor(s) and capacitor(s), there is little report on implementation of an inductor into ICs because of too low quality factor for large inductance fabricated in current silicon technology. This book aims at discussing thorough high-voltage generator design with the switched-capacitor multiplier technique.

The switched-capacitor multiplier originated with Cockcroft–Walton using serial capacitor ladders for their experiments on nuclear fission and fusion in 1932. Dickson qualitatively pointed out that the Cockcroft–Walton multiplier had too high sensitivity on parasitic capacitance to realize on-chip multipliers and then theoretically and experimentally showed that the parallel capacitor ladders realized on-chip high-voltage generation for programming Metal–Nitride–Oxide–Semiconductor (MNOS) nonvolatile memory in 1976.

After Dickson's demonstration, on-chip high-voltage generator has been implemented on Flash memories and LCD drivers and the other semiconductor devices. Accordingly, as the supply voltages of these devices become lower, it gets harder to realize small circuit area, high accuracy, fast ramp rate, and low power at a low supply voltage. This book provides various design techniques for the switched-capacitor on-chip high-voltage generator including charge pump circuits, pump regulators, level shifters, voltage references, and oscillators. The charge pump

inputs the supply voltage and a clock, which is generated by the oscillator, and outputs a voltage higher than the supply voltage or a negative voltage. The pump regulator enables the charge pump when the absolute value of the output voltage of the charge pump is lower than the target voltage on the basis of the reference voltage or disables it otherwise. The generated high or negative voltage is transferred to a load through high- or low-level shifters. Chapter 1 surveys system configuration of the on-chip high-voltage generator.

Chapter 2 discusses the charge pump. Since the charge pump was invented in 1932, various types have been proposed. After several typical types of charge pumps are reviewed, they are compared in terms of the circuit area and the power efficiency. The type that Dickson proposed is found to be the best one as an on-chip generator. Design equations and equivalent circuit models are derived for the charge pump. Using the model, optimizations are discussed to minimize the circuit area under the condition that the output current or the ramp time is given and to minimize the power dissipation under the condition that the output current is given theoretically.

Chapter 3 overviews actual charge pumps composed of capacitors and transfer transistors. Realistic design needs to take parasitic components such as parasitic capacitance at each of both terminals and threshold voltages of the transfer transistors into account. In order to decrease the pump area and to increase the current efficiency, some techniques such as threshold voltage canceling and faster clocking are presented. Since the supply current has a frequency component as high as the operating clock, noise reduction technique is another concern for pump design. In addition to design technique for individual pump, system level consideration is also important, since there are usually more than one charge pump in a chip. Area reduction can be also done for multiple charge pump system where all the pumps do not work at the same time.

Chapter 4 is devoted to individual circuit block to realize on-chip high-voltage generator. Section 4.1 presents pump regulator. The pump output voltages need to be varied to adjust them to the target voltages. This can be done with the voltage gain of the regulator or the reference voltage changed. The voltage divider which is a main component of the regulator has to have small voltage coefficient and fast transient response enough to make the controlled voltage linear to the trim and stable in time. A regulator for a negative voltage has a circuit configuration different from that for a positive voltage. State of the art is reviewed.

Section 4.2 surveys level shifters. The level shifter shifts the voltage for logic high or low of the input signal to a higher or lower voltage of the output signal. Four types of level shifters are discussed (1) high-level NMOS level shifter, (2) high-level CMOS level shifter, (3) high-voltage depletion NMOS + PMOS level shifter, and (4) low-level CMOS level shifter. The trade-offs between the first three high-voltage shifters are mentioned. The negative voltage can be switched with the low-level shifter. As the supply voltage lowers, operation margins of the level shifters decrease. As the supply voltage lowers, the switching speed becomes slower, eventually infinite, i.e., the level shifter does not work. Some design

techniques to lower the minimum supply voltage at which the level shifters are functional are shown.

Section 4.3 deals with oscillators. Without an oscillator, the charge pump never works. In order to make the pump area small, process, voltage, and temperature variations in oscillator frequency need to be minimized. There is the maximum frequency at which the output current is maximized. If the oscillator is designed to have the maximum frequency under the fastest conditions such as fast process corner, high supply voltage, and low temperature, the pump output current is minimum under the slowest condition such as slow process, low supply voltage, and high temperature. It is important to design the oscillator with small variations for squeezing the pump area.

Section 4.4 provides voltage references. Variations in regulated high voltages increase by a factor of the voltage gain of the regulators from those in the reference voltages. Reduction in the variations of the voltage references is a key to make the high generated voltages well controlled. Some innovated designs for low supply voltage operation are presented as well.

Chapter 5 provides high voltage generator system design. Multiple pumps are distributed in a die, each of which has sufficiently wide power ground bus lines. Total area including the charge pump circuits and the power bus lines needs to be paid attention for overall area reduction. Design methodology in this regard is shown using an example. Another concern on multiple high voltage generator system design is system level simulation time. Even though the switching pump models are used for the verification, simulation run time is still slow especially for Flash memory where the minimum clock period is 20–50 ns whereas the maximum erase operation period is 1–2 ms. In order to drastically reduce the simulation time, another charge pump model together with a regulator model is presented which makes all the nodes in the regulation feedback loop analogue to eliminate the hard-switching operation.

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Contents

Abbreviations

bjt	Bipolar junction transistor
BL	Bit-line
C	Capacitance of a pump capacitor
C_B	Parasitic capacitance at the bottom plate of a pump capacitor
clk	Clock
C_{OUT}	Total capacitance of pump capacitors
C_T	Parasitic capacitance at the top plate of a pump capacitor
CW	Cockcroft–Walton pump
eff	Current efficiency
FET	Field effect transistor
FIB	A type of pump whose V_{MAX} is associated with a Fibonacci number Fib(N) where N is the number of stages
G_{MAX}	Maximum voltage gain
G_V	Voltage gain
I_B	Base current
IC	Integrated circuit
I_C	Collector current
I_{DD}	Supply current
I_{DS}	Drain to source current
I_{IN}	Input current
I_L	Load current
I_{LOAD}	Load current
I_{OUT}	Output current
I_{PP}	Output current of a positive voltage pump at V_{OUT} of V_{PP}
I_{REG}	Regulator current
K(N)	4-port K-matrix of N-stage pump
LCD	Liquid crystal device
LED	Light emitting device
LIN	A type of pump whose V_{MAX} is linear to the number of stages
LSI	Large scale IC
MNOS	Metal nitride oxide semiconductor

MOS	Metal oxide semiconductor
N	Number of stages
N_{MIN}	Minimal number of stage
N_{OPT}	Optimum number of stages
opamp	Operational amplifier
P_{IN}	Input power
P_{OUT}	Output power
PVT	Process, voltage, and temperature
Q_{DD}	Total input charge
qout	Output charge per period
RFID	Radio frequency identification
R_{LOAD}	Resistance of a load circuit
R_{PMP}	Output impedance of a pump
R_{PWR}	Parasitic resistance of power and ground lines
SC	Switched-capacitor
SP	Serial-parallel
SRC	Source
T	Clock period of a pump driver clock or temperature
T_{OFF}	The period when a switch is being turned off
T_{ON}	The period when a switch is being turned on
UHF	Ultrahigh frequency
V_{BB}	Negative output voltage of a charge pump
V_{BE}	Base to emitter voltage
V_{BGR}	Band-gap reference voltage
V_{BL}	Bit-line voltage
V_{BS}	Bulk to source voltage
$V_{\mathrm{BV\_CAP}}$	Breakdown voltage of a capacitor
$V_{\mathrm{BV\_SW}}$	Breakdown voltage of a switch
V_{CAP}	Capacitor voltage
V_{D}	Drain voltage
V_{DD}	Supply voltage
$V_{\mathrm{DD\_LOCAL}}$	Supply voltage at a local interconnection node
$V_{\mathrm{DD\_MIN}}$	Minimum operating supply voltage
V_{DS}	Drain to source voltage
V_{G}	Gate voltage or voltage gain given by $V_{\mathrm{DD}} - V_{\mathrm{T}}$
V_{GS}	Gate to source voltage
V_{IN}	Input voltage
V_k	k-th nodal voltage
V_{MAX}	Maximum attainable voltage
V_{MOD}	Modulation voltage
V_{MON}	Monitored voltage
V_{OD}	Overdrive voltage
V_{OS}	Offset voltage
V_{OUT}	Output voltage

V_{PP}	Positive high output voltage of a charge pump
V_{REF}	Reference voltage
V_S	Source voltage
V_{SS_LOCAL}	Ground voltage at a local interconnection node
V_{SW}	Switching voltage
V_T	Threshold voltage or thermal voltage kT/q
V_{tD}	Threshold voltage of a depletion NMOS transistor
V_{tE}	Threshold voltage of an enhancement NMOS transistor
V_{tI}	Threshold voltage of an intrinsic NMOS transistor
V_{tP}	Threshold voltage of a PMOS transistor
WL	Word-line
α	Parameter representing a body effect of a MOS transistor
α_B	Ratio of C_B to C
α_T	Ratio of C_T to C
β	Multiplication factor of the collector current to the base current of a bipolar junction transistor
Φ_i	i-th clock phase

Chapter 1
System Overview and Key Design Considerations

Abstract This chapter describes which categories of voltage converters are covered in this book. Various applications of on-chip high-voltage generators such as memory applications for MNOS, DRAM, NAND Flash, NOR Flash, and phase-change memory, and other electronic devices for motor drivers, white LED drivers, LCD drivers, and energy harvesters are overviewed. System configuration of the on-chip high-voltage generator and key design consideration for the building circuit blocks such as charge pumps, pump regulators, oscillators, level shifters, and voltage references are surveyed.

1.1 Applications of On-Chip High-Voltage Generator

Section 1.1 starts with describing which categories of voltage converters are covered in this book. It also overviews various applications of on-chip high-voltage generators such as memory applications for MNOS, DRAM, NAND Flash, NOR Flash, and phase-change memory, and other electronic devices for motor drivers, white LED drivers, LCD drivers, and energy harvesters.

Voltage converters are categorized into two: switching converter (Erickson and Maksimovic 2001) and switched capacitor converter as classified in Table 1.1. Switching converter is composed of one or a few inductors, one or a few capacitors, and one or a few switching devices. Switched capacitor convertor is composed of one-to-many capacitors and one-to-many switching devices. The differences are with or without inductor and single or many stages. From the viewpoint of amount of power, the switching convertor can be used for applications to generate high power typically larger than 100 mW. On the other hand, switched capacitor convertor is used for applications to generate lower power than 100 mW. Presently, degree of integration is all, except for inductors, for switching converter whereas all components for switched capacitor. This is mainly because inductance that integrated inductor can have is much smaller than the value required as well as the input current noise could be much more in switching converter with a single stage. From the

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Table 1.1 Classification of voltage convertors

	Switching converter	Switched capacitor
Components	– Inductor – Capacitor – Switching device	– Capacitor – Switching device
Feature	High power and low loss	High voltage and low current or low voltage and high current
Integration	Except for inductor	Fully integrated
$G_v \equiv V_{out}/V_{in} > 1$	Boost	Charge pump/voltage multiplier
$1 > G_v > 0$	Buck	Switched capacitor voltage down convertor
$G_v < 0$	Buck–boost	Charge pump/voltage multiplier

viewpoint of voltage gain, that is, the ratio of the output voltage to the input voltage, there are three categories: greater than one, smaller than one and greater than zero, and smaller than zero. For the switching converter, these are respectively called boost converter, buck converter, and buck–boost converter. For the switched capacitor, the first and third are similarly called charge pump or voltage multiplier, and the second is called switched capacitor regulator or voltage down converter. Thus, this book covers these two categories with a voltage gain greater than one or lower than zero for fully integrated high-voltage generation among entire voltage converter system.

Following some figures show applications where on-chip voltage multipliers are used in IC's. A nonvolatile metal–nitride–oxide–semiconductor (MNOS) memory has a nitride film between the control gate and substrate where electrons or holes can trap as shown in Fig. 1.1a. Depending on the charges stored in the film, V_{GS}–I_{DS} characteristics are varied as described in Fig. 1.1b. The data in memory cells are read with V_{READ} biased to the control gate. The data is identified as "0" when the memory cell does not flow a sufficient current or as "1" when one flows. To alternate the memory data, the memory needed high voltages of 30–40 V for programming and erasing the data. To significantly reduce the system cost and complexity, an on-chip voltage multiplier was strongly desired. In 1976, Dickson theoretically and experimentally for the first time studied an on-chip high-voltage generator including a charge pump, oscillator, clock drivers, and a limiter, as shown in Fig. 1.1c. The diode is made of a MOSFET whose gate and drain terminals are connected. Dickson used two-phase clock which allowed the clock frequency as fast as possible. Using a seven-stage pump, he successfully generated 40 V from the power supply voltage of 15 V. The capacitors were also implemented using the nitride dielectric available in the MNOS process. Thus, switches and capacitors were integrated in IC's. Design parameters of 2 pF per stage, 7 stages, and 1 MHz realized an output impedance of 3.2 MΩ and a current supply of an order of 1 μA.

Figure 1.1d, e illustrate the image of how the charge pump works. For simplicity, a two-stage pump is shown. As the saying goes, a bucket, water, and the height of the surface of the water are, respectively, used as a capacitor, charge, and the capacitor voltage. V_{DD} is 2 V and V_{OUT} is 4 V. In the first half period (Fig. 1.1d), the current to the first capacitor stops when the voltage of the first capacitor reaches 2 V. The current stops flowing from the second capacitor to the output terminal

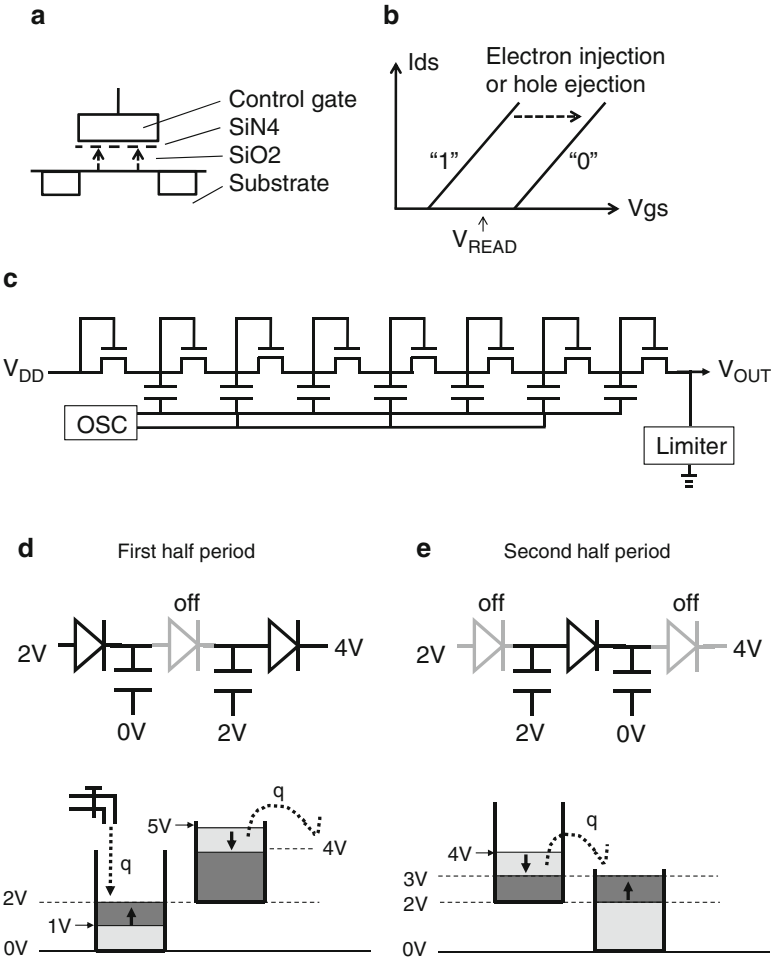

Fig. 1.1 MNOS cell structure (**a**), *I–V* curve of memory cells with data 1 and 0 (**b**), First Si verified on-chip Dickson pump (**c**), the states of the first (**d**) and second (**e**) half periods (Dickson 1976)

when the capacitor voltage reaches 4 V. At the beginning of the second half of the period (Fig. 1.1e), the capacitor voltage of the first capacitor increases to 4 V, whereas that of the second capacitor decreases to 2 V. This voltage difference between the two capacitors forces to flow the current through the second diode. When the threshold voltage of the diode is ignored, the charge transfer stops when the capacitor voltages are equalized. When the two capacitors are same size, an equilibrium state occurs when the capacitor voltages become 3 V. At the end of the second half of period, the capacitor voltages between the two terminals of the first and second capacitors are, respectively, 1 V and 3 V. At the beginning of the first half of period again, the surface potential at the top terminal becomes 1 V and 5 V,

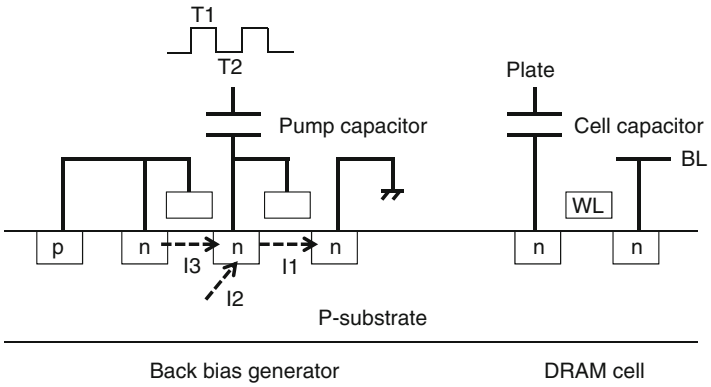

Fig. 1.2 Back bias generator for DRAM (Lee et al. 1979)

respectively. The water tap again flows until the surface potential increases to 2 V. Charge transfer from the second capacitor to the output terminal stops when the potential of the second capacitor reaches 4 V. Thus, alternate operations back and forth between the first and second half of periods result in charge transfer from the water tap to the output terminal with the same amount of charge q.

A dynamic random access memory (DRAM) cell is composed of one transistor and one capacitor as shown at the right-hand side of Fig. 1.2. The data "0" or "1" is stored as amount of charges in the cell capacitor. To read the data, a word-line (WL) is forced high. The amount of charges stored in the cell capacitor modulates the bit-line (BL) voltage, which is sensed and amplified by a sensing circuit. Thus, voltages at WLs and BLs were toggled between 0 V and 5 V during operations when the supply voltage was 5 V. Such a huge voltage swing could make PN junctions of NMOS transistors into forward bias regime locally due to capacitive coupling where it is far from body contacts if the p-type substrate is grounded. If this happens, stored charges could be flown into the substrate, resulting in degradation in data reliability. To avoid it, another negative voltage of −5 V was needed in addition to the power supply voltage of +5 V. The negative voltage was supplied to the substrate to have sufficient operation margin with such a potential localized forward biasing of junctions eliminated.

The −5 V power supply was eliminated by implementing a back bias generator allowing to reduce the system cost and complexity having the negative voltage supply, as shown at the left-hand side of Fig. 1.2. Lee and Breivogel et al. designed the generator to output −4.2 V back bias at zero substrate current and −3.5 V bias at 5 μA substrate current. The output current was needed to be higher than the impact ionization current due to the memory operation. The power dissipation was 1.5 mW. The power efficiency is estimated to be an order of 1 %. Additional advantages are known to be improving the power and speed with smaller junction capacitance at a back bias and steeping the subthreshold slope of transistors. The back bias generator has one stage. The input terminal is connected with the substrate. During T_1 where the clock is high, the capacitor node is made at about

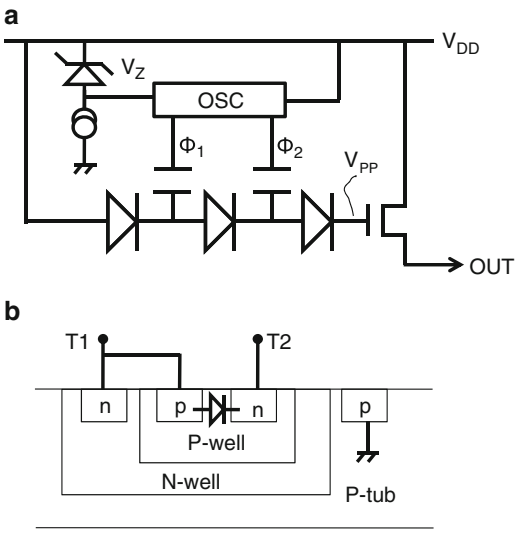

Fig. 1.3 Pump and load MOS (**a**) and diode structure (**b**) of a motor driver IC (Storti et al. 1988)

V_T of the switching transistor with the current I_1. During T_2 where the clock is low, the capacitor node is initially pulled down to about $V_T - V_{DD}$. The current I_2 or I_3 flows until the junction or the transistor turns off. Under zero substrate current, the potential of the substrate is made at the lower one of $2V_T - V_{DD}$ and $V_T + V_{BE} - V_{DD}$.

Another application of a charge pump is a motor driver IC, as shown in Fig. 1.3. Because it needs to switch a supply voltage up to 30 V with a peak current of 30 A, a power MOSFET is used. To sufficiently reduce the power dissipation, a channel resistance as low as 40 mΩ is required. A charge pump of the power IC generates an overdrive voltage for the power MOSFET. The supply voltage for the power IC is ranged in 6–30 V, whereas overdrive voltage is targeted at a voltage higher than 10 V, i.e., $V_{PP} > V_{DD} + 10$ V. The clock amplitude is regulated using a Zener diode. The switching diodes are realized by parasitic devices of isolated P-well and N-diffusion, as shown in Fig. 1.3b. The breakdown voltage of the diode is as high as 17 V. The worst case reverse bias is considered as $2V_{CLK}$ at the beginning of the pump operation, where V_{CLK} is the voltage amplitude of the driving clocks. Thus, the Zener diode with a breakdown voltage of 8 V is used to meet the requirement for $2V_{CLK} < 17$ V. Considering a sufficient operation margin under an extreme operation temperature range of −40 to 125 °C, three-stage structure is used.

Figure 1.4a, b show two typical configurations of drivers for white light emitting devices (LEDs). Figure 1.4c describes *I–V* characteristics of the structures in Fig. 1.4b, which have similar *I–V* curves as forward *I–V* curves of diodes. The current increases exponentially as the voltage across the LED increases. Thus, the operating point in the *I–V* plane could vary largely if the LED is controlled based on the voltage applied. To make the illumination or the power more stable against variations in the *I–V* characteristics per LED, the LED is controlled on a current

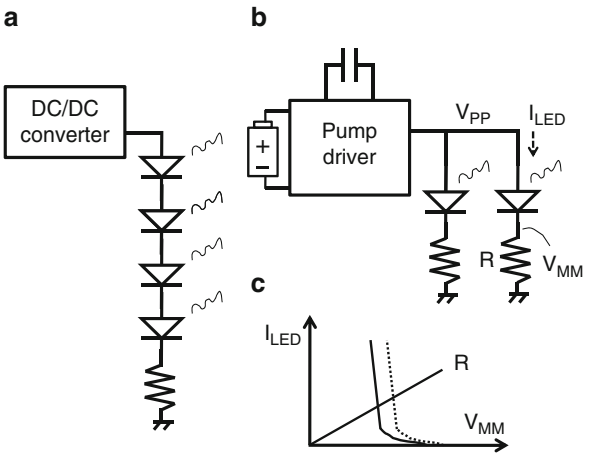

Fig. 1.4 White LED driver with (**a**) DC/DC converter (Chiu and Cheng 2007) and with (**b**) a charge pump (Wu and Chen 2009), and the operation condition of an LED (**c**)

basis. Simple addition of a resistor to an LED aims at stabilizing the operating point. Red, yellow, or green LED needs about 20 mA at 2 V, whereas white LED does at 3.2–4 V. When DC/DC converter generates 12 V, 5 red or 3 white LEDs can be connected in series in a path as shown in Fig. 1.4a. If 5 paths are needed to have 15 white LEDs in total, the converter with capability to output a current of 100 mA has to be used. For a miniature single white LED, a charge pump IC with a single Li-ion battery with an output voltage of 2.7–3.6 V can be a solution. Whether external capacitors are added or not depends on the total driver size and cost. When adding one discrete capacitor to reduce the cost of the IC with no large pump capacitor is acceptable in terms of its form factor, one could put more numbers of white LED connected in parallel in the system, as shown in Fig. 1.4b. The LED driver IC only includes components of switches and oscillator except for the capacitor. The number of white LED connected in parallel is up to the output current of the charge pump IC. In case that the driver IC outputs 100 mA, for example, one can connect 5 LEDs in parallel. If the system requires only one or a few white LEDs, all the components including the pump capacitor can be integrated.

A liquid crystal device requires two polarities of two positive voltages and two negative voltages to apply sufficiently high positive and negative voltages to each liquid crystal element aiming at improving the lifetime as shown in Fig. 1.5. Requirement for gate oxide of the transistors is sustaining a voltage of 18 V to fully turn on the pass transistors, which is half in case without generating voltages with two polarities. Otherwise, it would need a high voltage such as 36 V. A single driver IC generates these four different voltages with a supply current of an order of 10–100 μA because of no direct current to ground.

Another application using dual polarity is a NOR flash memory for erasing the data in a block, as illustrated in Fig. 1.6a. Flash cells are arranged horizontally and vertically, each of which is connected with a common source line (SRC), a bit-line (BL), and a word-line (WL). All cells in a block are placed in a common P-well. A

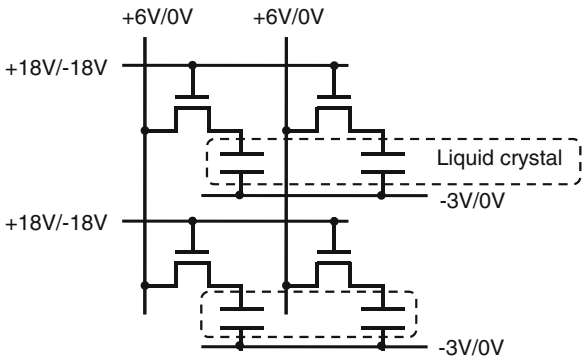

Fig. 1.5 Block diagram of a liquid crystal device (Wu and Chen 2008)

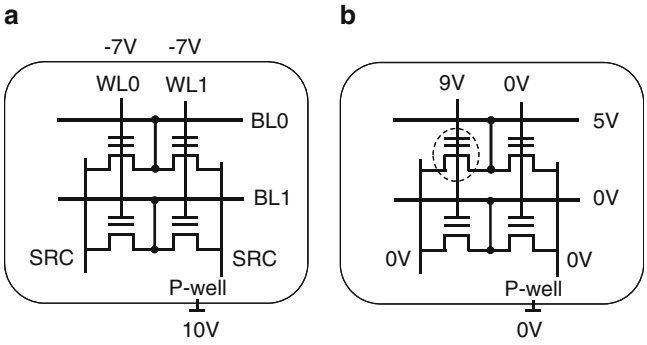

Fig. 1.6 Channel erase NOR flash memory under an erase bias condition (**a**) and under a program bias condition (**b**) (Atsumi et al. 2000)

bulk to gate voltage of 17 V needs to generate Fowler–Nordheim tunneling current flowing from the floating gate to the P-well. To allow the switching transistors for SRC and WLs to be scaled for reducing the transistor size, a high erase voltage of 17 V is divided to about half for a positive voltage of 10 V and a negative voltage of −7 V.

Figure 1.6b shows a program bias condition for the NOR flash memory. The cell enclosed by a broken line is under programming with WL and BL supplied by 9 V and 5 V, respectively. Because the scaled flash cell has a relatively low snapback voltage, the bit-line voltage (V_{BL}) has to be well controlled. The lower limit is determined by the programming speed with hot carrier injection. With too low V_{BL}, the flash cell could not have sufficient hot electrons to inject to the floating gate. The upper limit is determined by the snapback voltage. When V_{BL} is directly generated by a pump, a voltage ripple may be so large that the Flash cell can enter the snapback regime. The clamping NMOSFET can control V_{BL} with much smaller ripple voltage because the load current is determined mainly by the gate voltage as far as the load FET operates in saturation region, resulting much better stability in programming characteristics.

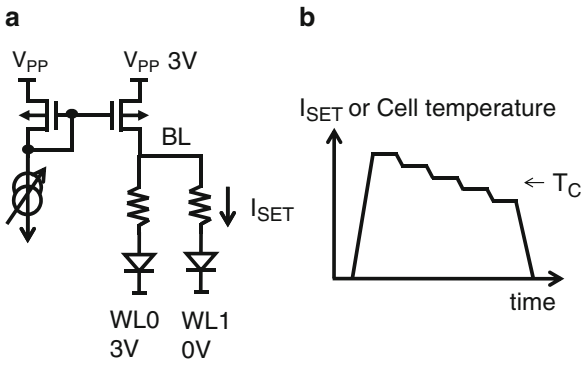

Fig. 1.7 Set voltage and current generator for phase-change memory (Lee et al. 2008)

Figure 1.7a shows phase-change memory elements described as the symbols of resistor, switching diodes, and a set current control circuit. To change into phase crystalline, the memory material needs to be heated up to a critical temperature (T_C) and to spend a required time interval at T_C. Because the memory array has quite large parasitic resistance in bit-lines (BLs) and word-lines (WLs), the input power required to individual memory element should have address dependencies. To program multiple memory cells with a few pulses for fast program operation, the set current as shown in Fig. 1.7b is supplied using a current control circuit with a variable current source. Thus, the boosted voltage V_{PP} is supplied to the memory elements with various current levels in a single set pulse.

Figure 1.8a illustrates a memory cell structure of NAND Flash memory. Because the floating gate is surrounded by insulator films, charges in the floating gate stay when the voltage difference between the control gate and silicon substrate is low enough. When there are many electrons in the floating gate of a cell, it has the data "0." When there are few electrons, it has the data "1." To program the data "0," the control gate is biased at a high voltage of 20 V while the substrate is grounded. Tunnel phenomenon under a high electric field is known as Fowler–Nordheim tunneling. When the control gate voltage (V_g) as shown in Fig. 1.8c is applied, the threshold voltage of the memory cell transistor is shifted as shown in Fig. 1.8b. The incremental step program pulse can reduce entire program time with well-controlled V_T of programmed cells using the general relation of $\Delta V_T = \Delta V_{PP}$. Due to the variation in program characteristics, cell A is programmed with two pulses, whereas cell B is done with five pulses. Once V_T of a cell becomes greater than a critical value V_C, the program pulse is no longer applied. Figure 1.8d illustrates the program pulse generator. R_1 of the resistor divider varies to vary the voltage gain G_V of V_G to V_{REF} as shown in Fig. 1.8c. Thus, the generator outputs the incremental step program pulse to control the programmed V_T's.

Energy harvesting has been paid much attention for low-power sensor and wireless applications. Figure 1.9a illustrates energy harvester gathering vibration energy. The second terminal of a capacitor is connected with a mobile plate. The displacement X is a sine waveform as shown in Fig. 1.9b. Suppose $X = 0$, $C_{VIB} = C_0$, and $V_{CAP} = V_{DD}$ at time T_0, the charge stored in the pump capacitor is $Q_0 =$

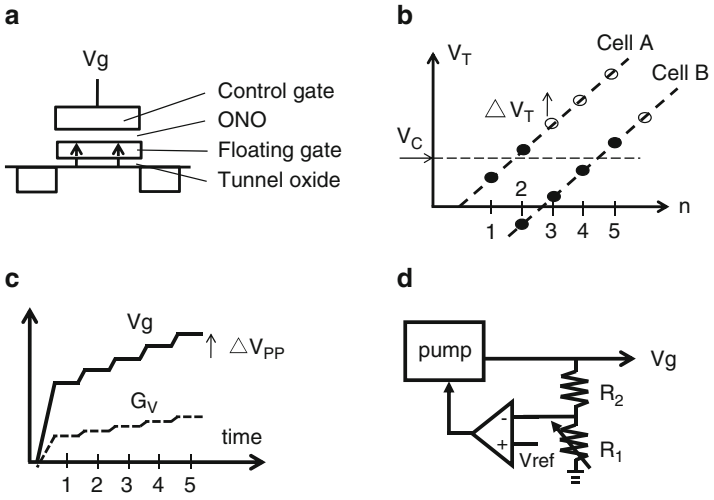

Fig. 1.8 Incremental step program pulse generation for NAND flash memory (Masuoka et al. 1987; Suh et al. 1995)

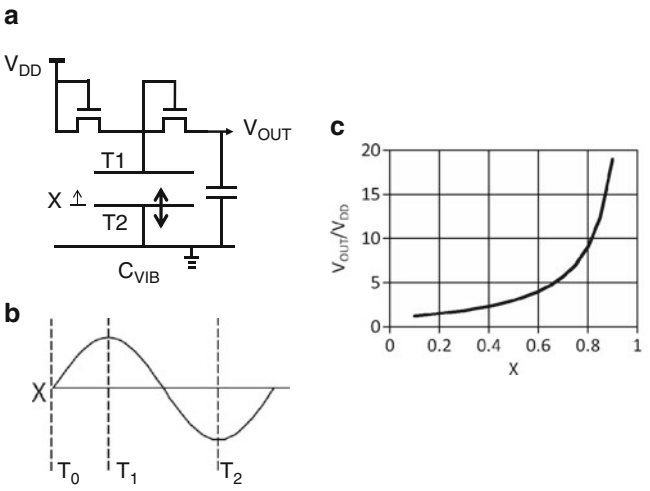

Fig. 1.9 Energy harvester IC converting from vibration energy (Yen and Lang 2006)

C_0V_{DD}. When the displacement is $+X$ at T_1, C_{VIB} is increased to $C_0/(1 - X)$. If there is no transfer transistor connected with the power supply V_{DD}, the capacitor voltage would be $Q_0 = C_0V_{DD} = C_0/(1 - X)V_{CAP}(T_1)$. Thus, $V_{CAP}(T_1)$ would be $(1 - X)V_{DD}$. With the transfer transistor, $V_{CAP}(T_1)$ is equalized to V_{DD}. Thus, the charge stored in the pump capacitor is $Q_1 = C_0/(1 - X)V_{DD}$. When the displacement is $-X$ at T_2, C_{VIB} is reduced to $C_0/(1 + X)$. If there is no transfer transistor connected with the output terminal, the capacitor voltage would be $Q_1 = C_0/(1 - X)V_{DD} =$

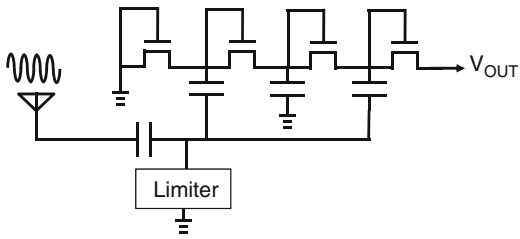

Fig. 1.10 UHF RFID IC (Jun et al. 2010)

$C_0/(1 + X)V_{CAP}(T_2)$. Thus, $V_{CAP}(T_2)$ would be $(1 + X)/(1 - X)V_{DD}$. Therefore, the maximum attainable output voltage with no current load is $(1 + X)/(1 - X)V_{DD}$. Figure 1.9c shows the factor of $(1 + X)/(1 - X)$ as a function of X.

Another energy harvester is illustrated in Fig. 1.10. Unlike that for vibrator energy as shown in Fig. 1.9, the harvester collecting the energy in a radio wave does not require any power supply voltage source. The input power from the antenna varies in a wide range. To protect capacitors and transistors from a high power input, a limiter is required. The capacitor at every even number stage is connected with the ground and that at every odd number stage is connected with the common clock line. In comparison with two-phase clock Dickson pump, the single clock pump has the maximum attainable voltage lower by half but the same output impedance, when the same number of stages and same size of capacitors are used.

In summary, design parameters of typical high-voltage generator system are as follows. The voltage gain G_V is required to be 1.5–15. The supply voltage and boosted voltage are respectively in a range of 0.5–30 V and 1–40 V. The output current is as low as an order of 1 μA especially in case of a high voltage gain and as high as an order of 10 mA especially in case of a low-voltage gain.

1.2 System and Building Block Design Consideration

Section 1.2 summarizes key design consideration for both systems and circuits, which are discussed in detail in the following chapters.

Figure. 1.11 shows on-chip high-voltage generator system and each component circuit block. The charge pump inputs the supply voltage (V_{DD}) and the clock which is generated by the oscillator, and outputs a voltage (V_{PP}) higher than the supply voltage or a negative voltage. The regulator enables the charge pump when the absolute value of the output voltage of the charge pump is lower than the target voltage on a basis of a reference voltage V_{REF}, or disables it otherwise. V_{PP} can vary in time by ΔV_{PP_DROP} due to a finite load current I_{LOAD} and by ΔV_{PP_RIPPLE} due to a finite response time in feedback loop with the pump regulator. The output voltage of the pump is determined by the reference voltage and the voltage gain of the regulator. To vary the pump output voltage, either reference voltage or voltage gain of the regulator is varied. The generated high- or negative voltage is transferred to a load through high- or low-level shifters. The level shifters are controlled

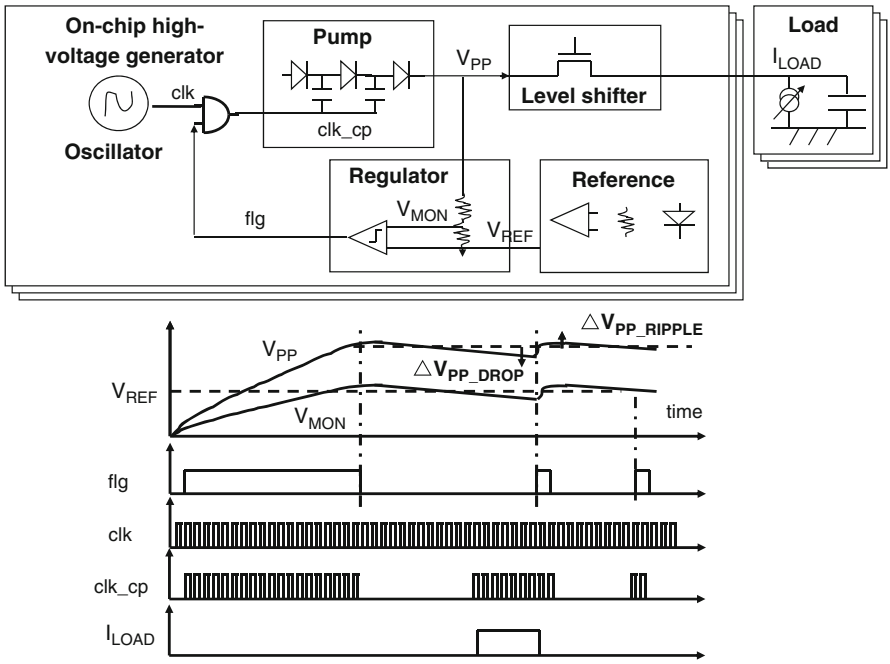

Fig. 1.11 On-chip high-voltage generator system

by the input supply voltage. The load is capacitive, resistive, or both. Optimization of the charge pump depends on the load characteristics.

According as the supply voltage decreases, the system design becomes more challenging in terms of (1) silicon area, (2) peak and average operation current, (3) ramp-up time, and (4) accuracy in the output voltage in DC and AC. The items (1)–(3) are under a trade-off relation. If the ramp-up time needs to be kept constant even with a lower supply voltage, the pump area and operation current would increase. Or, instead, if the pump area needs to remain the same, the output current would decrease, resulting in longer ramp-up time. Therefore, high-voltage generator design requires reconsideration on the entire system due to reduction in the supply voltage.

In addition, reducing the supply voltage while keeping the output voltage level means that the voltage gain is increased. Voltage variations in the reference voltage and the divided voltage of the regulator are amplified with the increased voltage gain, resulting in less accuracy in the output voltage of the generated high voltage. Moreover, IR drop in the power ground lines significantly affects the pump output current especially with lower supply voltage and with multiple high-voltage generators on a chip. Interference between different high-voltage generators occurs via the common impedance of the power ground lines. To take such considerations into design, the parasitic resistance in the power ground lines needs to be included into one of design parameters.

Table 1.2 Design considerations for each block

Circuit block	Design considerations
Charge pump	– Circuit topology choice to minimize the silicon area – Devices available as capacitors and switches in technology given – Equivalent circuit model – Design optimization for the clock to maximize the output current – Design optimizations for the number of stages to minimize the total pump area, the rise time, or the input power – Switching diode design with V_T canceling techniques – Capacitor design – Wide V_{DD} operation – Area efficient multiple pump system design with reconfiguration technique – Noise and ripple reduction design – Standby and active pump design
Pump regulator	– Resistor design – Reduction of variations in regulated voltages – Trimming capability – Response time reduction – Negative voltage detection
Oscillator	– Reduction in process, voltage, and temperature variations – Bi-stable oscillator with a high and low duty of 50 % – Four-phase clock generation
Level shifter	– Circuit topology choice according to availability of high-voltage transistors – Switching speed – Energy per switching – Minimum operating voltage – High-voltage relaxation design
Voltage reference	– Circuit topology choice according to availability of bipolar junction transistors – Reduction in process, voltage, and temperature variations – Minimum operating voltage

Because an on-chip high-voltage generator is one of the functional blocks on an LSI, simulation accuracy and run time have to be reasonable when all the blocks are simulated together with the generator. However, the high-frequency clock for driving the charge pump and the charge-transfer operation in the pump tends to make the simulations very slow. Thus, it is important to model the generator properly so that both the accuracy and simulation time are reasonable.

Table 1.2 summarizes design considerations for each block when circuit blocks composing an on-chip high-voltage generator are designed. Once the required voltage gain which is defined by the ratio of the high generated voltage to the supply voltage and the ratio of the parasitic capacitance of the pumping capacitor to the capacitance of the pumping capacitor are given for one's design, one can choose the best topology to minimize the charge pump circuit area. In case where those ratios are respectively higher than 5 and 0.03 typically, one should use the topology which Dickson experimented not only for the smallest area but also for the least power. For given transistors as switching devices in charge pumps, one can draw a graph showing the transistors can operate at how fast clock frequency. Then, using

the equivalent pump model, one can determine the design parameters such as the number of stages and capacitance per stage.

Pump regulators need to be designed with a potential variation in the output voltage of the pump considered. If it is larger than the required one, trimming capability needs to be implemented. Even if the output voltage is far from the target, trimming can adjust the output voltage closely to the target. Because the current flowing through the resistor divider needs to be small enough not to affect the net output current of the charge pump, resistance of the voltage divider tends to be relatively large. Adding switching devices for trimming can also increase RC time constant of the divider, which results in slow response from the time when the output voltage of the pump reaches the target to the time when the opamp detects it. According to the response delay, the pump operation continues to increase the output voltage, which creates the ripple in the output voltage. Therefore, the response time improvement is required to stabilize the output voltage.

Oscillators driving the charge pumps directly affect the pump output current. Higher frequency results in larger output current under a nominal condition. Thus, PVT (process, voltage, and temperature) variations in the frequency lead those both in the output and input current. If the pump is designed so that the output current at the slow condition meets the required one, the peak power is seen at the fast condition. Reduction in PVT variations in the oscillator is a key to make the pump performance stable.

Circuit topology choice due to the device availability and minimum operation voltage are common design concerns for level shifters and voltage references. In addition, level shifters need fast switching speed and robustness on high-voltage stress. One has to make sure of long-term operation under high-voltage stress.

In the following chapters, each design consideration is discussed.

References

Fundamentals of Power Converter

Erickson RW and Maksimovic D (2001) Fundamentals of power electronics. Springer, Berlin. ISBN 978-0-7923-7270-7

Applications for On-Chip High-Voltage Generator

Atsumi S, Umezawa A, Tanzawa T, Taura T, Shiga H, Takano Y, Miyaba T, Matsui M, Watanabe H, Isobe J, Kitamura S, Yamada S, Saito M, Mori S, Watanabe T (2000) A channel-erasing 1.8 V-only 32 Mb NOR flash EEPROM with a bit-line direct-sensing scheme. In: IEEE international solid-state circuits conference, Feb 2000, pp 276–277

Lee J, Breivogel J, Kunita R, Webb C (1979) A 80ns 5V-only dynamic RAM. In: IEEE international solid-state circuits conference, Feb 1979, pp 142–143

Chiu HJ, Cheng SJ (2007) LED backlight driving system for large-scale LCD panels. IEEE Trans Ind Electron 54(5):2751–2760

Dickson JF (1976) On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique. IEEE J Solid State Circuits 11(3):374–378

Jun Y, Jun Y, Law MK, Xiao LY, Lee MC, Ng KP, Gao B, Luong HC, Bermak A, Mansun C, Ki WH, Tsui CY, Yuen M (2010) A system-on-chip EPC Gen-2 passive UHF RFID tag with embedded temperature sensor. IEEE J Solid State Circuits 45(11):2404–2420

Lee KJ, Cho BH, Cho WY, Kang SB, Choi BG, Oh HR, Lee CS, Kim HJ, Park JM, Wang Q, Park MH, Ro YH, Choi JY, Kim KS, Kim YR, Shin IC, Lim KW, Cho HK, Choi CH, Chung WR, Kim DE, Yoon YJ, Yu KS, Jeong GT, Jeong HS, Kwak CK, Kim CH, Kim KN (2008) A 90 nm 1.8 V 512 Mb diode-switch PRAM with 266 MB/s read throughput. IEEE J Solid State Circuits 43(1):150–162

Masuoka F, Momodomi M, Iwata Y, Shirota R (1987) New ultra high density EPROM and flash EEPROM with NAND structure cell. In: IEEE international electron devices meeting, pp 552–555

Storti S, Consiglieri F, Paparo M (1988) A 30 A 30 V DMOS motor controller and driver. IEEE J Solid State Circuits 23(6):1394–1401

Suh KD, Suh BH, Um YH, Kim JK, Choi YJ, Koh YN, Lee SS, Kwon SC, Choi BS, Yum JS, Choi JH, Kim JR, Lim HK (1995) A 3.3 V 32 Mb NAND flash memory with incremental step pulse programming scheme. In: ISSCC, pp 128–129

Wu CH, Chen CL (2008) Multi-phase charge pump generating positive and negative high voltages for TFT-LCD gate driving. In: IEEE international symposium on electronic design, test & applications, pp 179–183

Wu CH, Chen CL (2009) High-efficiency current-regulated charge pump for a white LED driver. IEEE Trans Circuits Syst II 56(10):763–767

Yen BC, Lang JH (2006) A variable-capacitance vibration-to-electric energy harvester. IEEE Trans Circuits Syst I 53(2):288–295

Chapter 2
Charge Pump Circuit Theory

Abstract This chapter discusses circuit theory of the charge pump circuit. Since it was invented in 1932, various types have been proposed. After several typical types of charge pumps are reviewed, they are compared in terms of the circuit area and the power efficiency. The type that Dickson proposed is found to be the best one as an on-chip generator where the parasitic capacitance is 1–10% of the pump capacitor. Design equations and equivalent circuit models are derived for the charge pump. Using the model, optimizations are discussed to minimize the circuit area under various conditions that the output current, the ramp time, and the power dissipation are given theoretically.

This chapter is composed of the followings. Section 2.1 reviews several pump topologies and qualitative comparison among them. Section 2.2 presents operation analysis of each pump cell, i.e., Greinacher and Cockcroft–Walton cell, Brugler serial–parallel cell, Falkner-Dickson cell, Ueno–Fibonacci cell, and Cernea-2N cell, and then compares them quantitatively. The results suggest that Dickson cell is the best topology because of the largest voltage gain and smallest circuit area. Section 2.3 discusses Dickson pump in more detail including the equivalent circuit as well as several optimizations of the circuit with respect to circuit area and power.

2.1 Pump Topologies and Qualitative Comparison

This section begins with a brief history of several topologies of charge pump and their background on the critical characteristic parameters, i.e., the output impedance and the maximum attainable voltage. Operation of the initial topology as known as Cockcroft–Walton multiplier is discussed and the characteristic parameters are shown. Optimum design for maximizing the output power is, respectively, given under the conditions of resistive load and current load. After that, several topologies of pump are described which aim at having lower output

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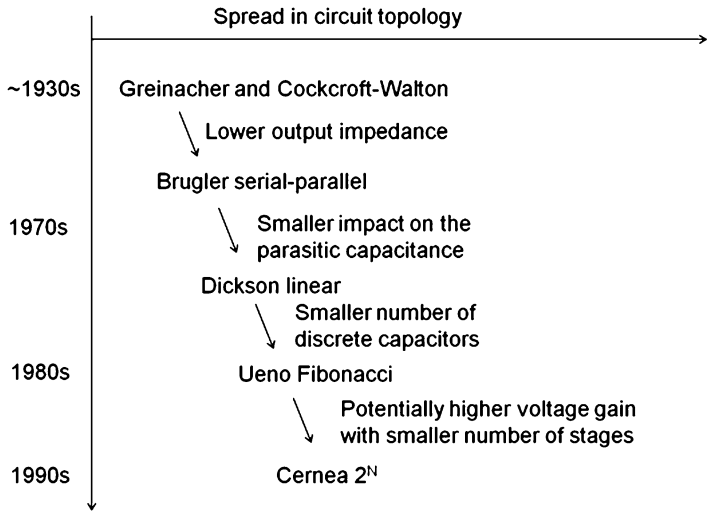


Fig. 2.1 History of two phase clock charge pump voltage multipliers

impedance for higher output current at a given output voltage. Qualitative sensitivity analysis on the parasitic capacitance of pump capacitors suggests that larger number of serially connected capacitors results in larger impact of the parasitic capacitance on the output current.

The switched-capacitor (SC) multiplier originated with Greinacher and Cockcroft–Walton (CW) using serial capacitor ladders independently. Because the CW multiplier had a relatively large output impedance with an order of N^3, where N is the number of stages, various types of multipliers with different topologies have been proposed to reduce the output impedance. By alternately switching the state from in-serial to in-parallel and vice versa, Brugler theoretically showed that the serial–parallel (SP) multiplier had lower output impedance with an order of N^1 than that of CW. Falkner suggested that parallel capacitor ladders reduced the output impedance as well. Dickson theoretically and experimentally showed that the output impedance of the parallel capacitor ladders was proportional to N^1. Another direction for improving SC performance is to increase the maximum attainable voltage gain G_{MAX}. Ueno et al. proposed the Fibonacci SC multiplier whose G_{MAX} is given by the Nth Fibonacci number of approximately 1.16exp (0.483N). The multipliers whose G_{MAX} is given by 2^N were proposed by Ueno et al. with multiphase switching clocks and by Cernea with two phase clocks. Figure 2.1 briefly summarizes the history of two phase clock charge pump voltage multiplier. Note that recent high-voltage generators are mainly based on the Dickson linear pump topology.

Performance analysis and design methodologies have also been done for the multipliers as described above. To determine an optimum multiplier topology under specific conditions, comparisons among those multipliers on circuit performance have also been made. Before advancing quantitative analysis, this chapter starts

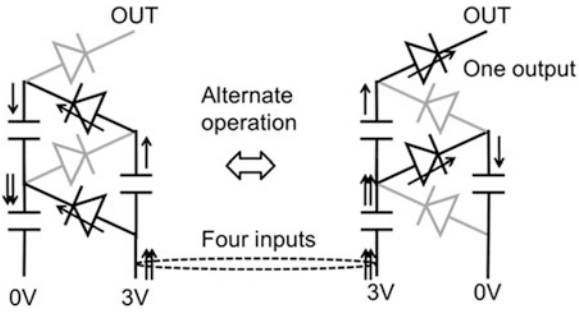


Fig. 2.2 Three stage CW in steady state (Cockcroft and Walton 1932)

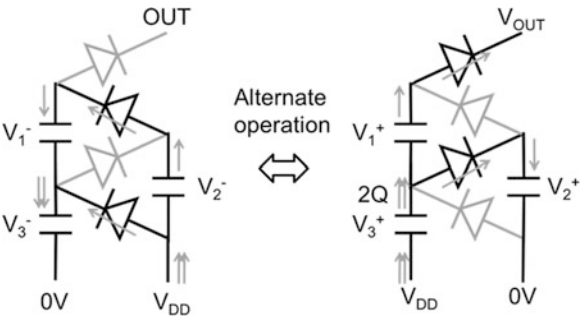


Fig. 2.3 Relation of V_3^+ and V_3^- to the other nodal voltages in steady state

with qualitative analysis on which multiplier is optimum with respect to circuit area under the condition that a given current is output at a given output voltage with a given parasitic capacitance.

Figure 2.2 shows how the CW circuit works. The number of stage is defined by the number of capacitors, i.e., three in this example. The number of diodes is four, larger by one than the number of stages. Because the CW works with two phase clock, one only needs to take care of these two half of periods. The diodes in gray are not under conduction state. One arrow indicates amount of charge Q which flows into the output terminal in a period. In the left hand side figure, a same amount of charge Q flows through each diode under a steady state. The top most two capacitors flow the same amount of Q to meet the condition that the current is continuous. Thus, the bottom most capacitor in the left branch and the power supply in the right branch flow amount of charges of $2Q$ to meet Kirchhoff's law. In the right hand side figure, both diodes and top most two capacitors, respectively, flow Q. The bottom capacitor and the power supply in the left branch flow $2Q$. As a result, one has to input $4Q$ to output $1Q$ per period. As one can easily guess, the current efficiency defined by the output current I_{OUT} over the input current I_{IN} is as shown by $I_{\mathrm{OUT}}/I_{\mathrm{IN}} = 1/(\#\mathrm{diodes}) = 1/(\#\mathrm{stages} + 1)$.

Based on Brugular's approach for theoretical steady state equation, one can calculate the relation between I_{OUT} and V_{OUT} using Figs. 2.3, 2.4, 2.5, and 2.6. V^- indicates the first half period and V^+ does the second half period. Each of $V^-{}_i$ and $V^+{}_i$ ($i = 1, 2, 3$) indicates the voltage difference between two terminals of each

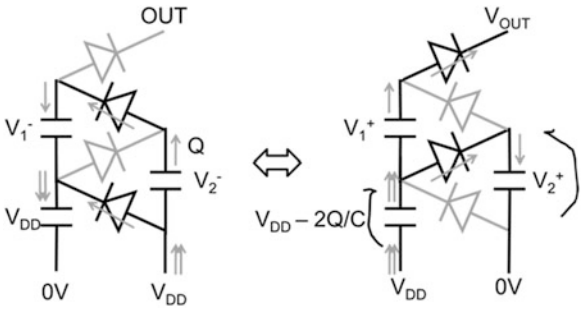


Fig. 2.4 Relation of V_2^+ and V_2^- to the other nodal voltages in steady state

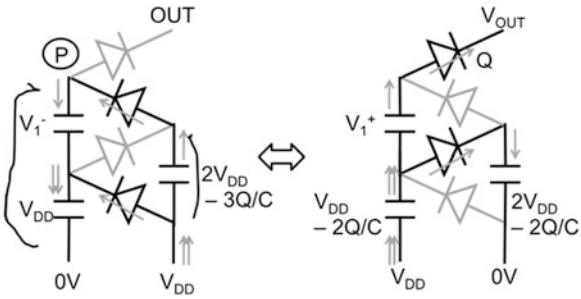


Fig. 2.5 Relation of V_1^+ and V_1^- to the other nodal voltages in steady state

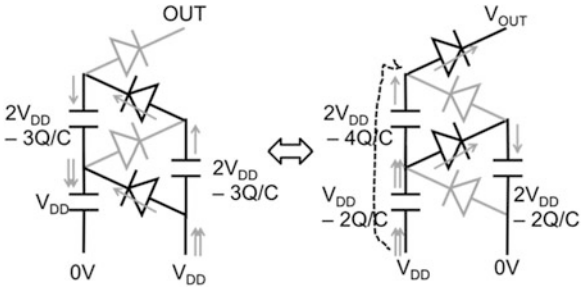


Fig. 2.6 Capacitor voltages in steady state

capacitor. The assumptions used here are that the period is too long to be able to neglect any RC time delay and that the threshold voltage of each diode is zero. Starting with Fig. 2.3, V_3^- is equalized to V_{DD}. Because V_3^+ is the voltage after amount of charges $2Q$ is transferred through the diode, it should be given by $V_3^+ = V_3^- - 2Q/C$. As a result, it is solved as $V_3^+ = V_{DD} - 2Q/C$.

$$V_3^- = V_{DD} \tag{2.1}$$

$$V_3^+ = V_3^- - 2Q/C \tag{2.2}$$

Next, Fig. 2.4 focuses on the relation of V_2^+ and V_2^- to the other nodal voltages. As shown in the right hand side, V_2^+ is equalized to V_3^+, resulting in $2V_{DD} - 2Q/$

$C = V_2^+$. As shown in the left hand side, V_2^- is lower by Q/C than V_2^+. From these two equations, V_2^- is given by $V_2^- = 2V_{\mathrm{DD}} - 3Q/C$.

$$V_2^+ = 2V_{DD} - 2Q/C \tag{2.3}$$

$$V_2^- = V_2^+ - Q/C = 2V_{DD} - 3Q/C \tag{2.4}$$

Similarly, Fig. 2.5 focuses on the relation of V_1^+ and V_1^- to the other nodal voltages. As shown in the left hand side, the potential at the point P is calculated by two ways. The first one is $V_1^- + V_{\mathrm{DD}}$ in the left path. The right path results in $V_2^- + V_{\mathrm{DD}} = (2V_{\mathrm{DD}}–3Q/C) + V_{\mathrm{DD}} = (3V_{\mathrm{DD}} –3Q/C)$. By equating these two, one has (2.5). The right hand side figure simply indicates that V_1^+ is lower by Q/C than V_1^-, thereby (2.6).

$$V_1^- = 2V_{DD} - 3Q/C \tag{2.5}$$

$$V_1^+ = 2V_{DD} - 4Q/C \tag{2.6}$$

Finally, Fig. 2.6 shows capacitor voltages. V_{OUT} is calculated with the sum of the capacitor voltages in the left path plus V_{DD} in the right hand figure.

$$V_{OUT} = (2V_{DD} - 4Q/C) + (V_{DD} - 2Q/C) + V_{DD} = 4V_{DD} - 6Q/C \tag{2.7}$$

Thus, V_{OUT} has two terms. The first term is proportional to V_{DD}. The multiplication factor of 4 is resulted from the number of capacitors that is the number of stages plus one from V_{DD} of the clock amplitude. The second term is proportional to Q. The multiplication factor is larger than the number of stages. This fact is resulted from the fact that amount of charges transferred to the next stage increases as the capacitor position gets closer to V_{OUT}. Thus, the sum of the multiplication factors tends to be higher as the number of stages increases. This means that the effective impedance of the CW multiplier rapidly increases as the number of stages increases.

What does (2.7) suggest? Introducing the cycle time T of the clock, the average output current I_{OUT} is expressed by (2.8), where V_{MAX} is the maximum attainable output voltage when I_{OUT} is zero as shown by (2.9) and R_{PMP} is the effective impedance of the pump as shown by (2.10), which will be derived in the next section.

$$I_{OUT} \equiv Q/T = (V_{MAX} - V_{OUT})/R_{PMP} \tag{2.8}$$

$$V_{MAX} = 4V_{DD} \rightarrow (N+1)V_{DD} \tag{2.9}$$

$$R_{PMP} = 6T/C \rightarrow\sim (N+1)^3/12\ T/C \tag{2.10}$$

Every topology of charge pumps has a similar I–V curve with these two characteristic parameters. The equivalent circuit is a simple voltage source and a

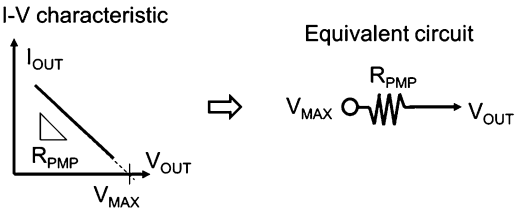


Fig. 2.7 Relation of I_{OUT} to V_{OUT} and an equivalent circuit in steady state

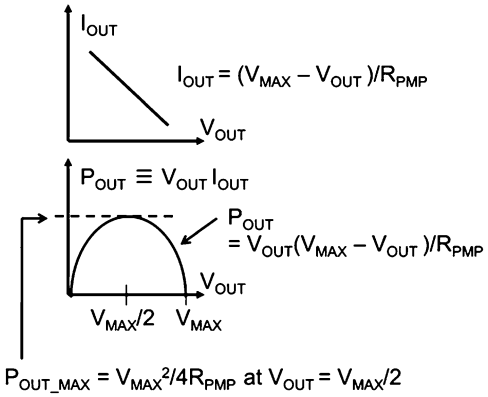


Fig. 2.8 Conditions for maximizing the output power

linear resistor as illustrated in Fig. 2.7. In this example of three stage CW pump, V_{MAX} is $4V_{\mathrm{DD}}$ and R_{PMP} is 6 T/C. One can qualitatively consider the power of three in (2.10) as follows. One comes from the amount of charges proportional to the number of stages, another one comes from kth capacitor from the bottom transferring the amount of charges proportional to k, and the last one comes from the amount of charges summed in all the capacitors in the left path. Each of those three factors is proportional to N, resulting in the power of three. More general and comprehensive discussions are done in the next section.

What else is resulted from the I–V equation is the optimum operating point where the output power is maximized as shown in Fig. 2.8. The above graph is the I_{OUT}–V_{OUT} curve. The output power is a multiple of I_{OUT} with V_{OUT}, resulting in a quadratic function. The maximum is given at a half of V_{MAX} because the X-interceptions occur at zero and V_{MAX}. The maximum power is then given by (2.11).

$$P_{OUT\_MAX} = {V_{MAX}}^2/4R_{PMP} \text{ at } V_{OUT} = V_{MAX}/2 \tag{2.11}$$

One may have different load conditions such a resistive load and a current load. No matter what the load is, the optimum operating point in terms of maximizing the output power is at a half of V_{MAX}, as shown in Fig. 2.9. In case of a resistive load, one can maximize the output power with designing R_{PMP} matched with R_{L}, which is so-called impedance match.

$$R_{PMP} = R_L \tag{2.12}$$

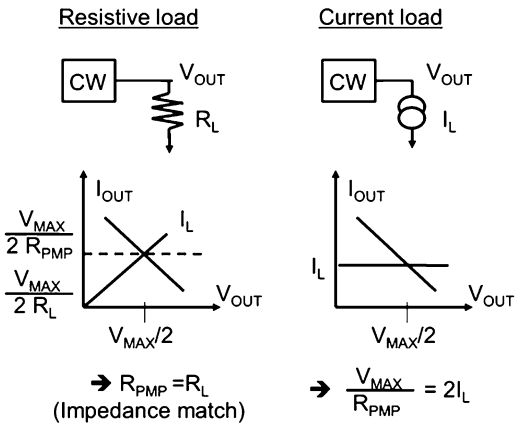


Fig. 2.9 Conditions for maximizing the output power

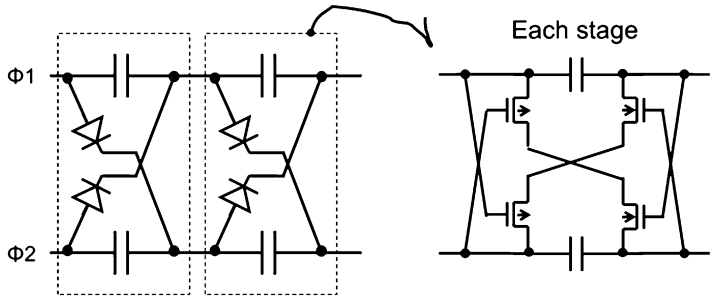


Fig. 2.10 Implementation of CW in ICs (Zhang et al. 2009)

In case of a current load, one can maximize the output power when the following relation between R_{PMP} and V_{MAX} is met.

$$V_{MAX}/R_{PMP} = 2I_L \tag{2.13}$$

Note that maximizing the output power under a given voltage of V_{PP} is equivalent to maximizing the output current at V_{PP}. Equations (2.11) to (2.13) are independent of a type of charge pump topology as far as the $I_{\mathrm{OUT}}-V_{\mathrm{OUT}}$ characteristic is the same form.

Because of quite high impedance with the CW pump with a relatively large voltage gain, there has not been lots of practice to implement the CW pump. One example implementation of CW in ICs is shown in Fig. 2.10. The key feature of the CW over the other types of pump is that every diode and capacitor sees a voltage difference of V_{DD} or less. This means that one can construct the pump with low-voltage devices, resulting in smaller circuit area with scaled devices. The circuit designers need to make sure that any device wouldn't be broken down under any

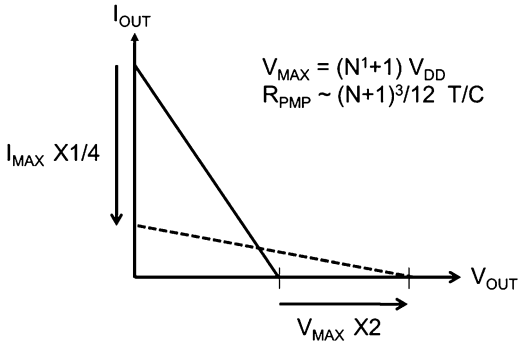


Fig. 2.11 I_{OUT}–V_{OUT} characteristic when the number of stages is doubled in CW

emergent case such as a sudden power shutdown and a sudden short of the output node to the ground. Under such circumstance, a high voltage may appear in any low-voltage device.

How significant is the power of three with respect to the number of stages in the output impedance of the CW pump? If one needs to double the number of stages to increase V_{MAX} twice, the output impedance decreases by a factor of eight. Then, the maximum output current where the output voltage is zero decreases by a factor of four, as shown in Fig. 2.11. When one designs the operating point at a half of V_{MAX}, the output current can decrease by a factor of four as well. Thus, the reduction rate in I_{OUT} over V_{OUT} is proportional to the squared number of stages. Thus, the CW multiplier may not be good for the cases where a large voltage gain is needed.

Brugler theoretically showed that there was another topology where the output impedance could be reduced as illustrated in Fig. 2.12a. Adding two more switches per stage, the capacitors can be switched from in-parallel (b) to in-series (c) alternately. All the capacitors are charged to V_{DD} in a parallel period and are connected in-series between V_{DD} and the output terminal. Hereinafter, one calls this type of pump serial–parallel or SP.

The procedure to extract the I_{OUT}–V_{OUT} equation is much easier than the case of CW using Fig. 2.13. Assuming Q is the amount of charge to be transferred to the output terminal in in-series period. Each capacitor loses the same amount of Q in this period. Thus, each capacitor needs to be charged by Q in in-parallel period. Before charging Q, each capacitor voltage should be $V_{DD} - Q/C \equiv V_{CAP}$. Thus, V_{OUT} can be related to V_{CAP} as (2.14).

$$V_{OUT} = V_{DD} + NV_{CAP} = (N+1)V_{DD} - NQ/C \tag{2.14}$$

As a result,

$$I_{OUT} \equiv Q/T = (V_{MAX} - V_{OUT})/R_{PMP} \tag{2.15a}$$

$$V_{MAX} = (N+1)V_{DD} \tag{2.15b}$$

$$R_{PMP} = N^1 T/C \tag{2.15c}$$

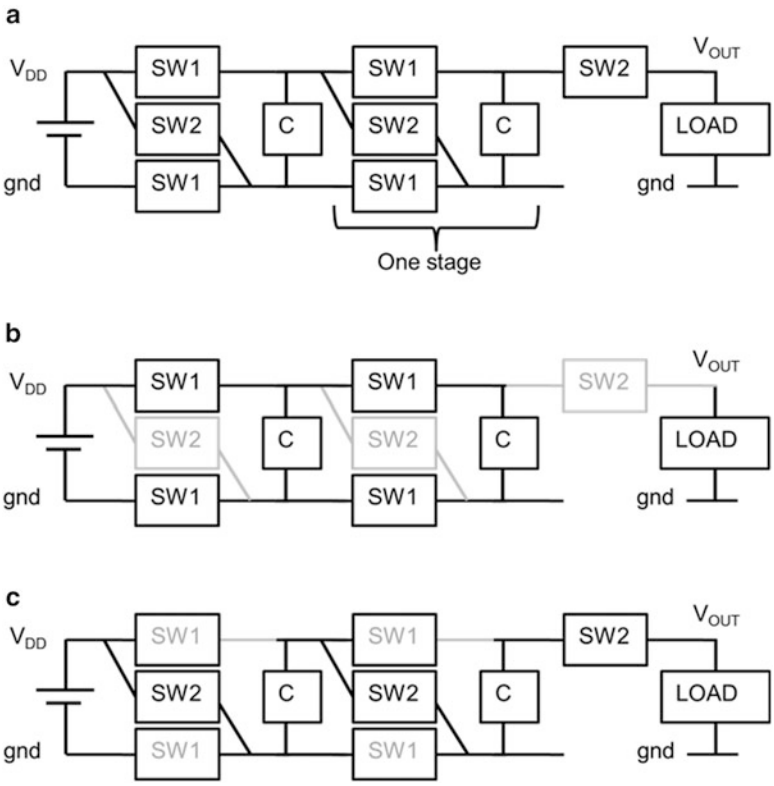


Fig. 2.12 Serial–Parallel switched capacitor with lower R_{PMP} Brugler 1971

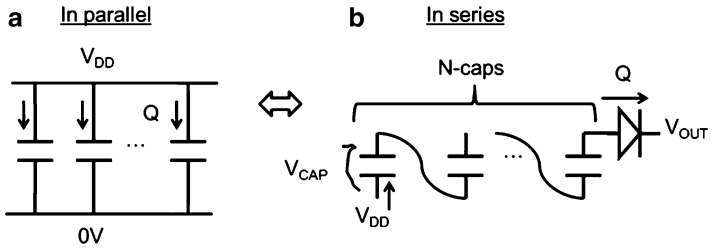


Fig. 2.13 Two phases of SP

Thus, the output impedance is proportional to N^1. To output Q in a period, each capacitor doesn't need to do extra work than getting Q from the power supply. The current efficiency defined by the total output current over the total input current is 1/(the number of capacitors + 1) as same as that of the CW. There is no advantage in the current efficiency with the serial–parallel pump.

A question here is how significant lower impedance is with the serial-–parallel pump. Figure 2.14a, b are, respectively, 5 and 10 stage pumps' *I*–*V* characteristics.

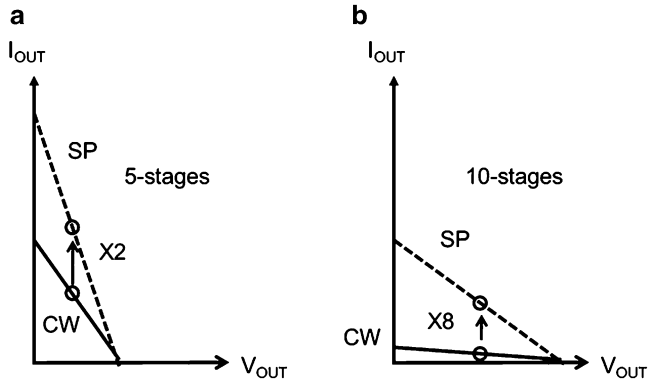


Fig. 2.14 Comparisons of 5 and 10 stage pumps' *I–V* characteristics between CW in *solid lines* and SP in *broken lines*

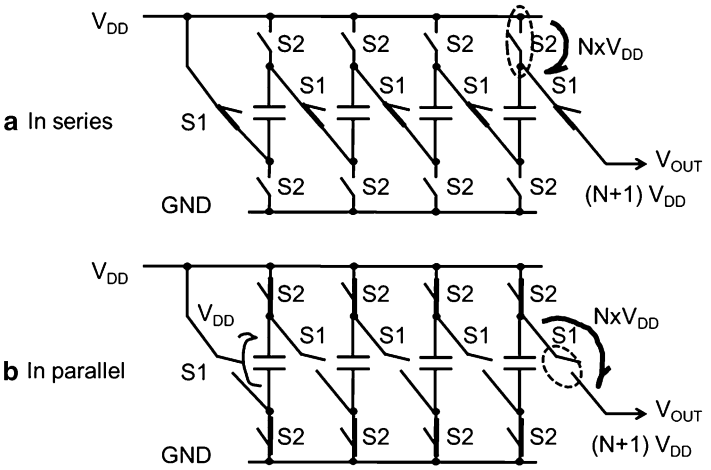


Fig. 2.15 Requirement for breakdown voltage in SP

Table 2.1 Comparison in characteristic parameters between CW and SP

	V_{MAX}	R_{PMP}	V_{BV_CAP}	V_{BV_SW}
CW	$(N+1)\ V_{DD}$	$(N+1)^3/12\ T/C$	V_{DD}	$1V_{DD}$
SP	$(N+1)\ V_{DD}$	N^1T/C	V_{DD}	NV_{DD}

The broken lines show the SP and the solid lines show CW. All the capacitors are assumed to be same. Under the condition, the SP has larger output current than the CW does especially when the number of stage is larger.

Figure 2.15 shows the requirement for breakdown voltages for the capacitors and switches used in the SP. The capacitor voltage in parallel state is equal to V_{DD} and that in serial state is lower than V_{DD} by Q/C. Therefore, the capacitor could be made of a low-voltage device, which enables to reduce the capacitor area with higher

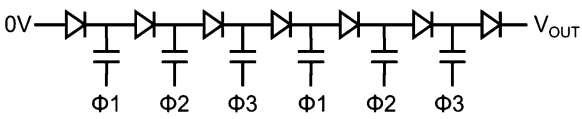


Fig. 2.16 Another proposal for lower R_{PMP} (Falkner 1973)

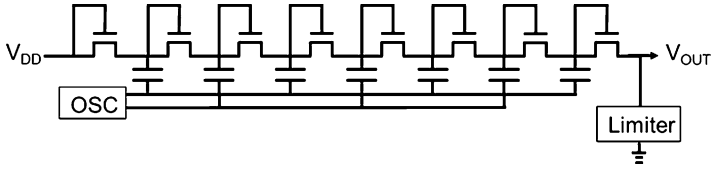


Fig. 2.17 First Si verified on-chip Dickson pump (Dickson 1976)

capacitance density. On the other hand, the switches used closely to the output terminal see N times higher than V_{DD} for both states, resulting in requirement for high-voltage switching devices.

Table 2.1 summarizes comparison of SP with CW in terms of the pump characteristics' parameters and the voltage requirements for capacitors and switches. The maximum attainable voltage V_{MAX} is no difference. The output impedance of SP is proportional to N^1, whereas that of CW is to N^3. The maximum voltage applied to a capacitor is same to be V_{DD}. The maximum voltage applied to a switch of the CW is $1V_{DD}$, whereas that of the SP is NV_{DD}. From the system view point, one needs to have high-voltage switches to connect the output terminal to a load. Thus, high-voltage devices should be available in designing the LSIs. So, requirement of high-voltage device for a switch in the SP itself shouldn't be considered as a drawback. But, the maximum operating clock frequency could be affected by the high-voltage device, because a high-voltage device is typically slower than a low-voltage device. Relation between scaling of device and operating frequency will be discussed in details in Chap. 3.

Falkner schematically showed another pump topology with a lower R_{PMP} than the CW, as shown in Fig. 2.16. The circuit has three phase clock, but it is not the essence. Key point is that each capacitor is connected with next one or two stages in parallel at a time. Unlike the CW has the state with half of stages connected in-series and the SP has that with all stages connected in-series. The numbers of switches or diodes are that of capacitors plus one, which is the same condition as the CW.

In 1976, Dickson theoretically and experimentally for the first time studied an on-chip high-voltage generator including a charge pump, oscillator, clock drivers, and a limiter, as shown in Fig. 2.17. The diode was made of a MOSFET whose gate and drain terminals are connected to play the same role as a rectifying diode. Dickson used two phase clock which allowed the clock frequency faster than the three phase clock of Fig. 2.16. Using a seven stage pump, a high voltage of 40 V was successfully generated from the power supply voltage of 15 V. The operation principle will be discussed in Chap. 3 in details.

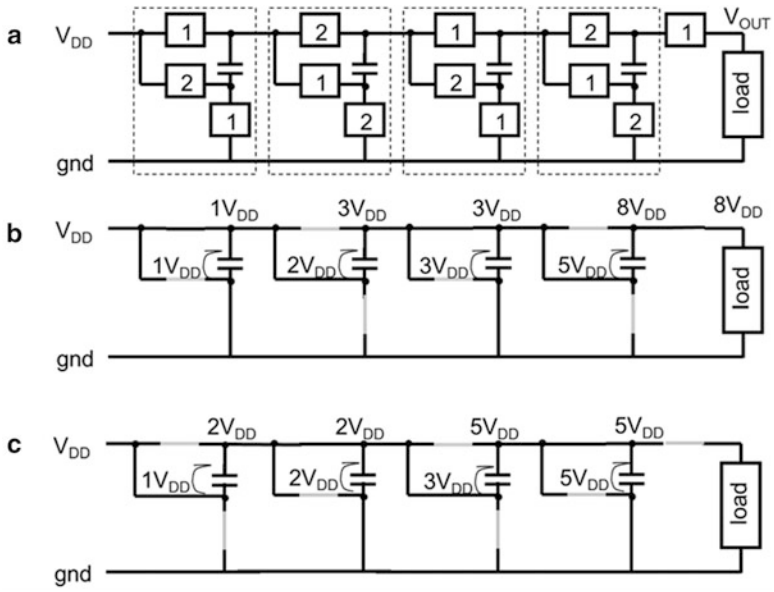


Fig. 2.18 Fibonacci type multiplier (Ueno et al. 1991)

Another type of two phase pump was proposed by Ueno et al. aiming at reducing the number of capacitors for low cost small form factor discrete applications, as shown in Fig. 2.18. The interesting characteristic is the maximum attainable voltage is given by Fibonacci number, i.e., 2, 3, 5, 8, 13, 21, and so on.

$$Fib(N) = Fib(N-1) + Fib(N-2) \tag{2.16}$$

where Fib(1) = 2, Fib(2) = 3. As the number of stages increases, the voltage gain increases more rapidly than the number of stages. For example, when one needs to have V_{MAX} of 13, one only needs five stages with Fibonacci pump, whereas 12 stages with CW, SP, or Dickson pump. Each stage has one capacitor and three switches, as shown in Fig. 2.18a. The number 1 and 2 in the boxes indicate that the switch marked as 1 turns on in a first half period and turns off in a second half of period and the switch marked as 2 turns on in the second half period and turns off in the first half of period. Figure 2.18b shows the connection states in the first half period. Even number of stages is connected in-series with the output terminal and odd number of stages is connected in parallel to the serial ones, in other word, $(2k-1)$th stage is connected with $2k$th stage in parallel. The nodal voltages shown are valid only when the output current is zero. Figure 2.18c shows the connection states in the second half period. The situations are complementary to the first half period. Thus, a half of stages are in-series and the other half of stages are in parallel, alternately.

The last one is 2^N multiplier as shown in Fig. 2.19. When the number of stages connected between the input and the output is N, the required number of capacitors

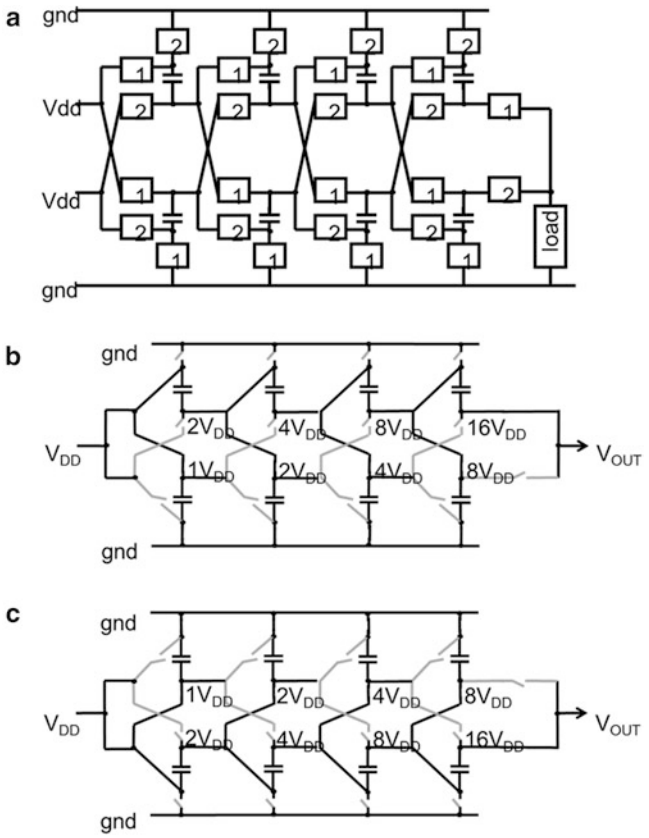


Fig. 2.19 2-Phase 2^N multiplier (Cernea 1995)

are $2N$ because two arrays are required to complete the multiplier unlike the other types of pump. Figure 2.19b shows a first half period. The upper stages are connected in-series with the output terminal, whereas the lower stages are connected in parallel with the upper stages, or in other word, kth lower stage is connected in parallel with kth upper stage. The voltage values shown in Fig. 2.19b are those in case of no load current. As a number of stages increases by one, the maximum attainable voltage increases by a factor of two in an ideal case where no parasitic capacitance is considered. One may consider the number of stages of 2^N multiplier is smaller than that of the Fibonacci pump. But, the number of capacitors of $2N$ multiplier is larger than that of the Fibonacci one because the 2^N pump needs two arrays. For example, when a maximum attainable voltage gain of 16 is required, 2^N pump needs at least eight capacitors as shown in Fig. 2.19, whereas Fibonacci pump does six capacitors.

Several topologies of two phase pump are overviewed. Now one should have a question about which topology should be selected for ICs as on-chip high-voltage

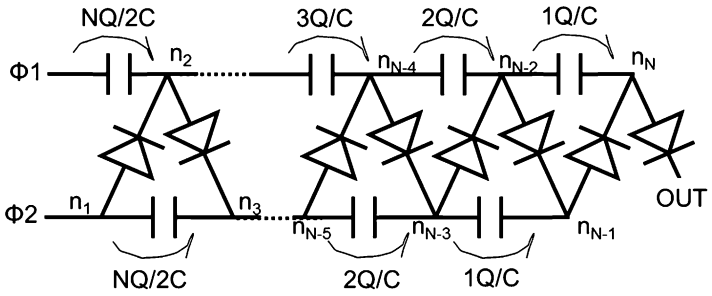


Fig. 2.20 Voltage amplitude of each capacitor in *N*-stage CW

generator. To answer the question, one has to take the two factors in terms of parasitic elements into consideration. The first one is a finite threshold voltage V_T of a real switching device. But, it simply reduces the voltage amplitude at each capacitor node from V_{DD} and doesn't affect the comparison between different topologies. Once can replace V_{DD} with $V_{DD}-V_T$. Besides, it can be mitigated with several design techniques to effectively eliminate V_T. State of the art will be overviewed in Chap. 3. The second one is a finite parasitic capacitance (C_P) of a real capacitor and switch. Unfortunately, there is no design technique to eliminate the parasitic capacitance. Therefore, sensitivity of C_P on the pump performance could determine the best topology for integration because the ratio of C_P to the integrated capacitor can be much larger than that of the discrete capacitor.

Figure 2.20 illustrates *N*-stage CW pump. The values shown are the voltage amplitude of each capacitor between two half periods of cycle, which are suggested by (2.1)–(2.6) in the case of three stages. Therefore, the voltage amplitude at the $(N-k)$th node, $(V_{N-k}^{+}-V^{-}_{N-k})$, is calculated as $f(N-k)Q/C$, where

$$f(N-k)=\sum_{i=1}^{k/2} i = k(k+2)/8 \tag{2.17}$$

Suppose that each node has the parasitic capacitance C_P. The power supply driving the clocks Φ1, 2 charges $C_P f(N-k)Q/C$ for $(N-k)$th node. Hence, the total amount of charge to C_P of all nodes, Q_P, is

$$\begin{aligned} Q_P &= C_P \sum_{k=1}^{N} k(k+2)Q/8C \\ &= [N(N+1)(2N+7)/48](C_P/C)Q \end{aligned} \tag{2.18}$$

According as the number of stages increases, Q_P increases with the cube of the number of stages. When Q_P becomes compatible to Q, the voltage at each node would decrease from the ideal cases such as (2.1)–(2.6) because the voltage

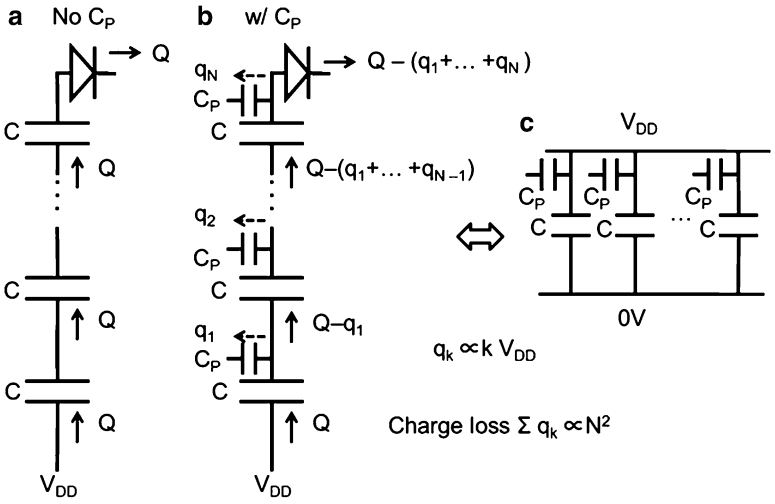


Fig. 2.21 Impact of parasitic capacitance on *I*–*V*s: SP

amplitude reduces accordingly, resulting in invalidity of (2.18). For now, one uses (2.18) as the first-order estimate.

Its worth of taking a look at the impact of parasitic capacitance on *I*–*V* of the SP. Figure 2.21 illustrates an in-series state with no C_P in ideal case (a), that with C_P in real case (b), and an in-parallel state (c). The SP works changing the state between (b) and (c), alternately. When all the capacitors are connected in parallel with the power supply, there is no impact of the parasitic capacitance on stored amount of charge in the capacitors. When the capacitors are connected in series, if the parasitic capacitance is negligibly small, each capacitor transfers a same amount of charge Q to the next capacitor, resulting in outputting Q, as shown in (a). However, if the parasitic capacitance is not negligible, the transferred charge is reduced at every node. To be worse, the charge loss at an upper node is larger than that at a lower node. Simply assuming kth capacitor reduces the charge q_k proportional to kV_{DD}, which is the voltage amplitude from in-parallel state (c) to in-series state (b), the sum of charge loss from the bottom to the top, ΣkV_{DD}, would be proportional to N^2. This means that the charge loss increases as the square of the voltage gain. The output charge Q could be eventually down to zero when the parasitic capacitance and the number of stages are large. For example, when $C_P/C = 0.1$, the charge loss of C_P/CN^2 becomes greater than 1 with N of 4. This means that one never have a voltage gain of 5 or larger. Therefore, the impact of the parasitic capacitance is very large in the SP as well as the CW.

What about the Dickson pump? Figure 2.22 illustrates three stages of a Dickson pump. The charge supplied from the power supply is Q independent of the capacitor location. Assuming each capacitor loses the charge q due to the parasitic capacitance, every capacitor can transfer $Q - q$ independent of the capacitor location unlike CW and SP. The difference from the SP is that each capacitor of the Dickson

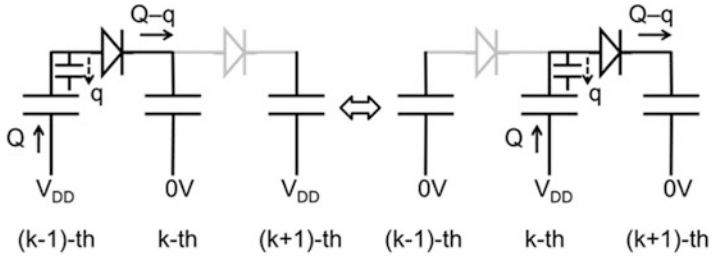


Fig. 2.22 Impact of parasitic capacitance on *I*–*V*s: Dickson

Table 2.2 Qualitative comparison between five topologies of pump

	CW	SP	FIB	2^N	Dickson
$(V_k^+–V_k^-)/V_{DD}$	$\sim k^2$	$\sim k^1$	Fib(k–2)	2^{k-1}	1
# of input terminal	2	1	1	2	$N + 1$

gains the input charge of Q and loses q. On the other hand, all the stages of the SP have only one input terminal as shown in Fig. 2.21b.

To simplify the estimates of the impact of the parasitic capacitance in Fibonacci and 2^N pumps, the special case where the output voltage is at the maximum attainable voltage is considered here. According to Fig. 2.18b, c, the voltage amplitude of kth stage between the first and second half periods in the Fibonacci pump can be expressed by Fib(k)–Fib(k–1) = Fib(k–2). Similarly, based on Fig. 2.19b, c, the 2^N pump has $(V_k^+–V_k^-)$ of $2^N–2^{N-1} = 2^{N-1}$.

Table 2.2 summarizes the comparison table among the five types of pump. Charge loss due to a parasitic capacitance is proportional to the voltage amplitude at each node in one period. This means that the larger voltage amplitude the larger charge loss. In this regard, the pumps except for the Dickson have more significant impact on the parasitic capacitance than the Dickson. The charge loss is accumulated when the number of input is small. The pumps except for Dickson have one or two inputs only. Thus, the accumulated charge loss is much larger than the Dickson. From these qualitative view points, the Dickson seems to have the least sensitivity of the parasitic capacitance. But, the next question is if its valid quantitatively too.

2.2 Circuit Analysis of Five Topologies

All the two phase charge pump multipliers discussed in this section have the same symbolical structure as shown in Fig. 2.23, using the two-port transfer matrix $\mathbf{K}(N)$ that was introduced by Harada et al., where N is the number of stages. $\mathbf{K}(N)$ connects the input and output voltages and currents as shown by (2.19), where a subscript number 1 or 2 indicates phase 1 or 2 as shown in Fig. 2.23a, b. Each stage has a similar four-port structure, as shown in Fig. 2.23c, where $\mathbf{K}_j$ is the matrix

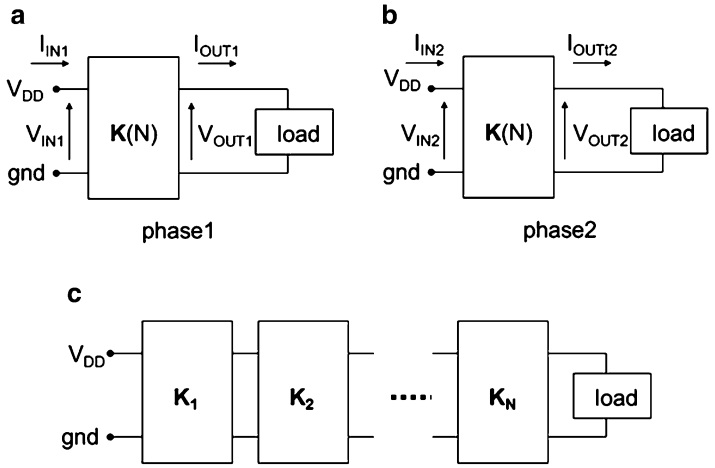


Fig. 2.23 *K*-matrix expression of a charge pump multiplier (Harada et al. 1992)

representing *j*th stage. Considering the fact that the output of *j*th stage is the input of $(j + 1)$th stage, *N* matrices are simply combined into $\mathbf{K}(N)$ as shown by (2.20).

$$[V_{IN1} \quad V_{IN2} \quad I_{IN1} \quad I_{IN2}]^T = \mathbf{K}(N)[V_{OUT1} \quad V_{OUT2} \quad I_{OUT1} \quad I_{OUT2}]^T \tag{2.19}$$

$$\mathbf{K}(N) = \mathbf{K}_1\mathbf{K}_2 \cdots \mathbf{K}_N \tag{2.20}$$

In the following section, these various types of switched capacitor multiplier are reviewed under the ideal condition where the parasitic capacitance is small enough to be ignored in the analysis, the operation frequency is so slow that internal capacitor nodes are fully charged and discharged in each half of period, and the clock amplitude is high enough to eliminate the effect of the threshold voltages of diodes or switching transistors. Then, the optimum multiplier is identified among serial–parallel, linear, Fibonacci, and 2^N multipliers where the impact of the parasitic capacitance is considered. Two-port transfer matrix for calculating an output and input voltage and current of SP, FIB, and 2^N cells with parasitic capacitance at capacitor nodes, which greatly affects the pump performance, is introduced. Numerical results on circuit area and current efficiency as a function of output voltage and parasitic capacitance are shown by using the transfer matrix. The optimum on-chip multiplier with minimum circuit area is then identified to be a Dickson charge pump.

2.2.1 Greinacher–Cockcroft–Walton (CW) Multiplier

Figure 2.24 illustrates a serial ladder multiplier proposed by Greinacher and Cockcroft–Walton. The number of stage (*N*) is defined by the number of capacitor. The number of diodes is $N + 1$. In Fig. 2.24, *N* is 6. Each half of them is serially

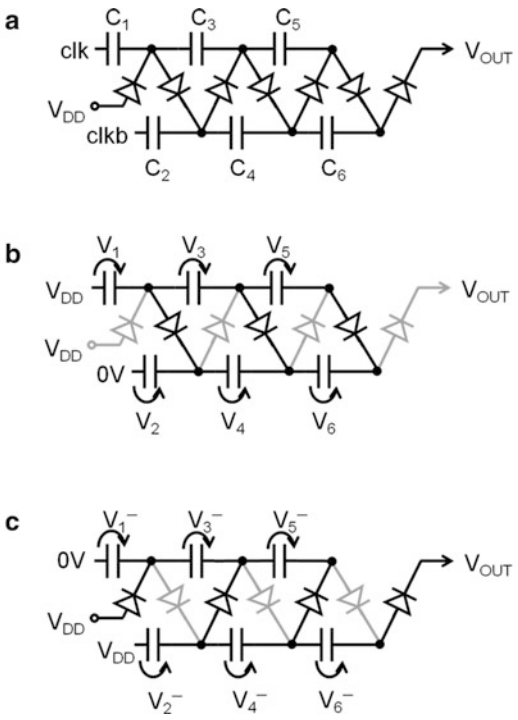


Fig. 2.24 Six-stage Greinacher–Cockcroft–Walton multiplier (Cockcroft and Walton 1932)

connected and driven by complementary clocks clk or clkb. Figure 2.24, respectively, shows the first and second half periods. The clock has two voltage states with V_{DD} and 0 V. Capacitor voltages V_k and $V_k{}^-$ ($1 \leq i \leq 6$) are defined at the end of each half period. The following equations hold.

$$V_{DD} + V_1 = V_2 \tag{2.21}$$

$$V_{DD} + V_1 + V_3 = V_2 + V_4 \tag{2.22}$$

$$V_{DD} + \sum_{i=1}^{j} V_{2i-1} = \sum_{i=1}^{j} V_{2i} \tag{2.23}$$

$$V_1{}^- = V_{DD} \tag{2.24}$$

$$V_{DD} + V_2{}^- = V_1{}^- + V_3{}^- \tag{2.25}$$

$$V_{DD} + \sum_{i=1}^{j} V_{2i}{}^- = \sum_{i=1}^{j} V_{2i-1}{}^- \tag{2.26}$$

Charge transferred through each diode in half period is same in steady state. The charge in C_1 is transferred to C_2, C_4, and C_6 in the first half period in Fig. 2.24b, in total $3q$, when each transferred charge is written as q. Similarly, the charge in C_3 is transferred to C_4, and C_6, and the charge in C_5 is transferred to C_6. Charge of $2q$ and $1q$, are respectively, discharged from C_3 and C_5. In case where the number of stage is even N, the similar consideration results in (2.27)–(2.29).

$$C_1V_1 + \frac{Nq}{2} = C_1V_1^- \tag{2.27}$$

$$C_3V_3 + \left(\frac{N}{2} - 1\right)q = C_3V_3^- \tag{2.28}$$

$$C_{2k-1}V_{2k-1} + \left(\frac{N}{2} - k + 1\right)q = C_{2k-1}V_{2k-1}^- \tag{2.29}$$

Similarly, the charge in C_2 is transferred to C_3, C_5, and the output terminal in the second half period in Fig. 2.24c, in total $3q$. Thus,

$$C_2V_2 - \frac{Nq}{2} = C_2V_2^- \tag{2.30}$$

$$C_4V_4 - \left(\frac{N}{2} - 1\right)q = C_4V_4^- \tag{2.31}$$

$$C_{2k}V_{2k} - \left(\frac{N}{2} - k + 1\right)q = C_{2k}V_{2k}^- \tag{2.32}$$

From (2.21)–(2.32), V_2^-, V_4^-, V_{2k}^- are calculated as (2.33)–(2.35).

$$V_2^- = 2V_{DD} - \frac{Nq}{2C_1} - \frac{Nq}{2C_2} \tag{2.33}$$

$$V_4^- = 2V_{DD} - \frac{Nq}{2C_1} - \frac{Nq}{2C_2} - \left(\frac{N}{2} - 1\right)\frac{q}{C_3} - \left(\frac{N}{2} - 1\right)\frac{q}{C_4} \tag{2.34}$$

$$V_{2k}^- = 2V_{DD} - \sum_{i=1}^{k}\left(\frac{N}{2} - i + 1\right)\frac{q}{C_{2i-1}} - \sum_{i=1}^{k}\left(\frac{N}{2} - i + 1\right)\frac{q}{C_{2i}} \tag{2.35}$$

The output voltage V_{OUT} is the sum of V_{DD}, V_2^-, V_4^-, …, V_N^- based on Fig. 2.24c resulting in (2.36).

$$\begin{aligned} V_{OUT} &= V_{DD} + \sum_{k=1}^{N/2} V_{2k}{}^{-} \\ &= (N+1)V_{DD} - \sum_{k=1}^{N/2} \left(\frac{N}{2} - k + 1\right)^2 \frac{q}{C_{2k-1}} \\ &\quad - \sum_{k=1}^{N/2} \left(\frac{N}{2} - k + 1\right)^2 \frac{q}{C_{2k}} \end{aligned} \tag{2.36}$$

The relation between I_{OUT} and V_{OUT} is calculated as (2.37)–(2.39), where the cycle time is assume to be one.

$$I_{OUT} \equiv q = \frac{V_{MAX} - V_{OUT}}{R_{PMP}} \tag{2.37}$$

$$V_{MAX} = (N+1)V_{DD} \tag{2.38}$$

$$R_{PMP}(C_1, C_2, \cdots, C_N) = \sum_{j=1}^{N/2} \left(\frac{N}{2} - j + 1\right)^2 \frac{1}{C_{2j-1}} + \sum_{j=1}^{N/2} \left(\frac{N}{2} - j + 1\right)^2 \frac{1}{C_{2j}} \tag{2.39}$$

In case where the capacitance of all the capacitors is same as $C_0 = C_{\mathrm{TOT}}/N$, where C_{TOT} is the total capacitance, (2.39) is rewritten as (2.40),

$$\begin{aligned} R_{PMP} &= \frac{N(N+1)(N+2)}{12} \frac{1}{C_0} \\ &= \frac{N^2(N+1)(N+2)}{12} \frac{1}{C_{TOT}} \end{aligned} \tag{2.40}$$

In case where the capacitance is weighted so that R_{OUT} is minimized under the condition that the total capacitance is constant, one can use Lagrange multiplier introducing functions f and g, and a parameter λ as follows.

$$f(C_1, C_2, \cdots, C_N) \equiv \sum_{j=1}^{N} C_j - C_{TOT} = 0 \tag{2.41a}$$

$$g(C_1, C_2, \cdots, C_N, \lambda) \equiv R_{PMP}(C_1, C_2, \cdots, C_N) - \lambda f(C_1, C_2, \cdots, C_N) \tag{2.41b}$$

$$\frac{\partial}{\partial C_{2j-1}} g(C_1, C_2, \cdots, C_N) = -\left(\frac{N}{2} - j + 1\right)^2 \frac{1}{C_{2j-1}{}^2} - \lambda = 0 \tag{2.41c}$$

$$\frac{\partial}{\partial C_{2j}} g(C_1, C_2, \cdots, C_N) = -\left(\frac{N}{2} - j + 1\right)^2 \frac{1}{{C_{2j}}^2} - \lambda = 0 \tag{2.41d}$$

Equations (2.41c) and (2.41d) hold when (2.42) holds.

$$C_1 : C_2 : C_3 : C_4 : \ldots : C_{N-1} : C_N = \frac{N}{2} : \frac{N}{2} : \left(\frac{N}{2} - 1\right) : \left(\frac{N}{2} - 1\right) : \ldots : 1 : 1 \tag{2.42}$$

Equation (2.39) results in (2.43).

$$R_{PMP} = \frac{N^2(N+2)^2}{16} \frac{1}{C_{TOT}} \tag{2.43}$$

With an effort optimizing each capacitor as (2.42), one can reduce the output resistance by a factor of about 25%.

$$\frac{R_{PMP\_unifrom\_C}}{R_{PMP\_weighted\_C}} = \frac{4}{3} \frac{N+1}{N+2} \tag{2.44}$$

Similarly, in case of odd N, (2.37) and (2.38) hold, but (2.39), (2.40), (2.43), and (2.44) are, respectively, replaced with (2.45), (2.46), (2.47), and (2.48),

$$\begin{aligned} R_{PMP}(C_1, C_2, \cdots, C_N) = & \sum_{j=1}^{(N+1)/2} \left(\frac{N+1}{2} - j + 1\right)^2 \frac{1}{C_{2j-1}} \\ & + \sum_{j=1}^{(N-1)/2} \left(\frac{N-1}{2} - j + 1\right)^2 \frac{1}{C_{2j}} \end{aligned} \tag{2.45}$$

$$\begin{aligned} R_{PMP} &= \frac{(N+1)(N^2+2N+3)}{12} \frac{1}{C_0} \\ &= \frac{N(N+1)(N^2+2N+3)}{12} \frac{1}{C_{TOT}} \end{aligned} \tag{2.46}$$

$$R_{PMP} = \frac{(N+1)^4}{16} \frac{1}{C_{TOT}} \tag{2.47}$$

$$\frac{R_{PMP\_unifrom\_C}}{R_{PMP\_weighted\_C}} = \frac{4}{3} \frac{N(N^2+2N+3)}{(N+1)^3} \tag{2.48}$$

2.2.2 *Serial–Parallel (SP) Multiplier*

Figure 2.25a shows a serial–parallel multiplier. Figure 2.25b, c shows how each capacitor is connected one another in each half period. All the capacitors are connected in parallel between the supply voltage V_{DD} and the ground in the first half period (b) and in-series between V_{DD} and the output voltage V_{OUT} in the second half period (c). The capacitor voltage between two terminals of each capacitor is V_{DD} in the first half period and $(V_{\mathrm{OUT}} - V_{\mathrm{DD}})/N$ in the second half period. When the charge transferred to the output terminal in a period is q, T is the period, and C is capacitance of each capacitor, the output current I_{OUT} is given by the following.

$$I_{OUT} = q/T = \frac{NC}{T}[(N+1)V_{DD} - V_{OUT}] \tag{2.49}$$

I_{OUT} is rewritten by

$$I_{OUT} = \frac{V_{MAX} - V_{OUT}}{R_{PMP}} \tag{2.50}$$

where

$$V_{MAX} = (N+1)V_{DD} \tag{2.51}$$

$$R_{PMP} = \frac{TN}{C} \tag{2.52}$$

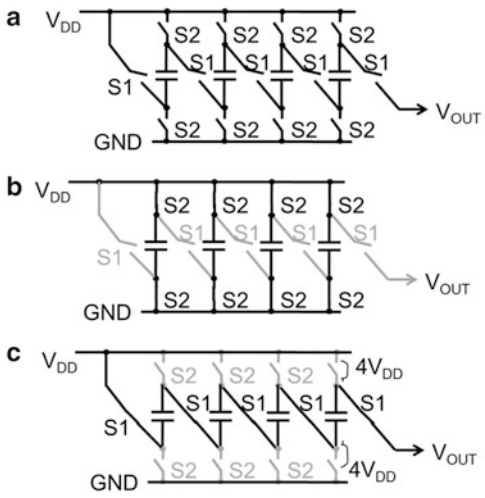


Fig. 2.25 (**a**) Serial–parallel multiplier, (**b**) in-parallel state, and (**c**) in-series state (Brugler 1971)

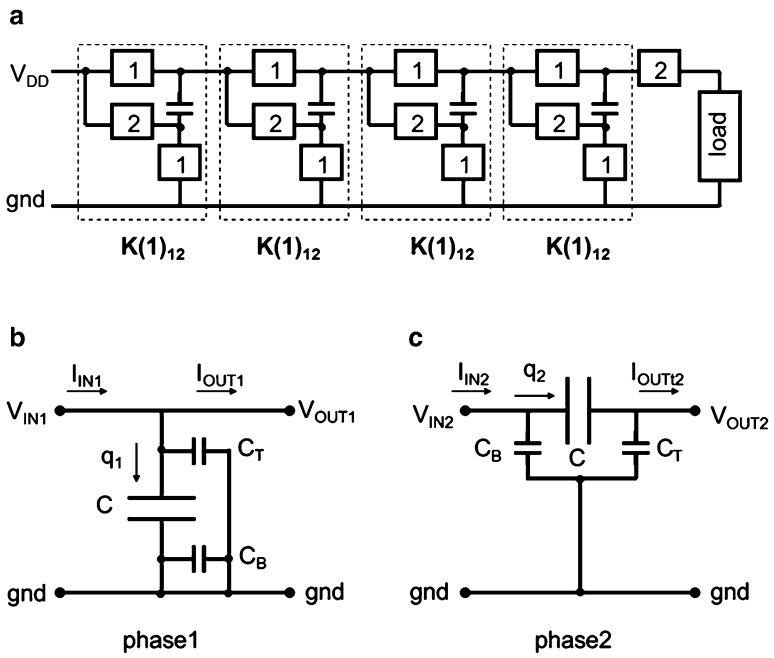


Fig. 2.26 Four-stage SP (**a**) and two alternate states (**b**), (**c**) of each stage

It is noted that the output resistance R_{PMP} is proportional to N^1 in SP which is much less dependency on N than CW with a dependency of N^3. Since each capacitor needs to be charged by the same amount of q in the first period, the input current supplied by V_{DD} is given by

$$I_{DD} = (N+1)I_{OUT} \tag{2.53}$$

When the maximum attainable voltage gain is defined by

$$G_V \equiv V_{MAX}/V_{DD} = N+1 \tag{2.54}$$

The current efficiency is given by

$$eff \equiv I_{OUT}/I_{DD} = 1/G_V \tag{2.55}$$

Next, let us take parasitic capacitance into analysis. Four stage SP pump is also expressed by Fig. 2.26a. Every stage is identical, thereby represented as $\mathbf{K}(1)_{12}$. Each stage has two operation states as shown in Fig. 2.26b, c, where C is the multiplier capacitor, C_{T} is the parasitic capacitance at one of the terminals of C, and C_{B} is the parasitic capacitance at the other terminal of C. In steady states, the following equations hold with the assumption that any parasitic resistance can be ignored.

$$V_{IN1} = V_{OUT1} \tag{2.56}$$

$$(I_{IN1} - I_{OUT1})T/2 = q_1 + C_T(V_{OUT1} - V_{OUT2}) \tag{2.57}$$

$$q_1 = C(V_{OUT1} - V_{OUT2} + V_{IN2}) \tag{2.58}$$

$$q_2 = I_{IN2}T/2 - C_B V_{IN2} = I_{OUT2}T/2 + C_T(V_{OUT2} - V_{OUT1}) \tag{2.59}$$

where q_1 and q_2 are the charge flowing into C in phase 1 and 2, respectively, and T is a cycle time. From the steady state condition of $q_1 = q_2$, the K-matrix in case of 1 stage, $\mathbf{K}(1)_{12}$, is calculated as (2.60) based on (2.56)–(2.59),

$$\mathbf{K}(1)_{12} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -(1+\alpha_T) & (1+\alpha_T) & 0 & R \\ 0 & 0 & 1 & 1 \\ -1/r_T - (1+\alpha_T)/r_B & 1/r_T + (1+\alpha_T)/r_B & 0 & (1+\alpha_B) \end{bmatrix} \tag{2.60}$$

where $\alpha_i = C_i/C$, $r_i = \mathrm{T}/2C_i$ (i = T, B), and $R = T/2C$.

As shown by (2.20), the entire K-matrix of N-stage SP multiplier is calculated by multiplying $\mathbf{K}(1)_{12}$ by N-times, resulting in (2.61).

$$\mathbf{K_{SP}}(N) = (\mathbf{K}(1)_{12})^N \tag{2.61}$$

From Fig. 2.23 and (2.19), the output current of SP multiplier I_{OUT} is $I_{\mathrm{OUT2}}/2$ since the averaged time of period for I_{OUT} is twice as long as that for I_{OUT2}, the output voltage V_{OUT} is V_{OUT2}, $I_{\mathrm{OUT1}} = 0$, and $V_{\mathrm{IN1}} = V_{\mathrm{IN2}} = V_{\mathrm{DD}}$. Thus, the following equation holds.

$$[V_{DD} \quad V_{DD} \quad I_{IN1} \quad I_{IN2}]^T = \mathbf{K_{SP}}(N)[V_{OUT1} \quad V_{OUT} \quad 0 \quad 2I_{OUT}]^T \tag{2.62}$$

The relation between V_{OUT} and I_{OUT} is calculated by the first and second row of (2.62) by eliminating V_{OUT1}. The total current consumption I_{IN} is calculated by $(I_{\mathrm{IN1}} + I_{\mathrm{IN2}})/2$ with certain values of V_{OUT} and I_{OUT}. One can easily calculate the output voltage–current characteristics and the current consumption or efficiency with the circuit parameters, such as C, C_{T}, C_{B}, T, N, given by using a simple matrix calculator (2.62).

2.2.3 *Falkner-Dickson Linear (LIN) Multiplier*

Figure 2.27 illustrates the Dickson charge pump circuit. A charge pump with an even number of stages is considered in this subsection, but a similar analysis in the case of an odd number stage charge pump can be carried out. q is defined as the

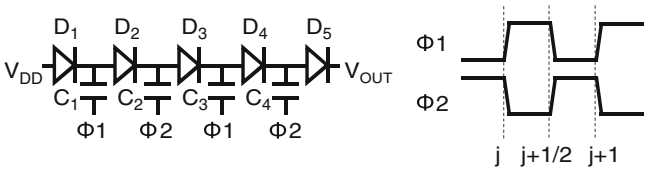


Fig. 2.27 Four-stage Dickson pump (Falkner 1973, Dickson 1978)

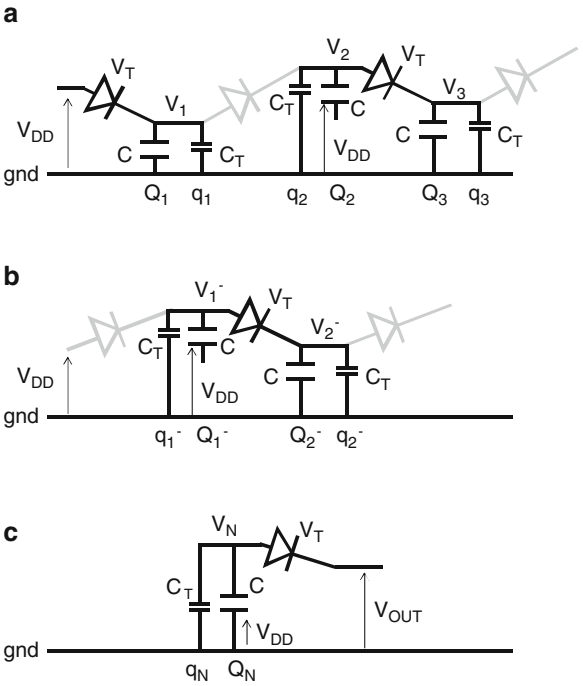


Fig. 2.28 Relations between next neighbors

charge transferred from one capacitor to the next one during one cycle, and Q_i ($1 \leq i \leq N$) are defined as the charges stored in the capacitors C_i at time j. Figure 2.28 illustrates connection of the first stage with the input terminal and connection between the second and third stages at time j (a), connection between the first and second stages at time $j + 1/2$ (b), and connection of the last stage with V_{OUT} at time j (c).

From Fig. 2.28a, the following relations hold under the condition that the diode D_1 is cut off at time j.

$$V_1 = V_{DD} - V_T \tag{2.63a}$$

$$Q_1 = C(V_{DD} - V_T) \tag{2.63b}$$

$$q_1 = C_T(V_{DD} - V_T) \tag{2.63c}$$

where V_{DD} is the supply voltage and V_T the subthreshold voltage. The difference between the total amount of charge stored in C and C_T at the first stage at time j and that at time $j + 1/2$ is q under the steady state condition.

$$(Q_1 + q_1) - ({Q_1}^- + {q_1}^-) = q \tag{2.64a}$$

$${Q_1}^- = C({V_1}^- - V_{DD}) \tag{2.64b}$$

$${q_1}^- = C_T {V_1}^- \tag{2.64c}$$

From (2.63b), (2.63c) and (2.64a), (2.64b), (2.64c),

$${V_1}^- = (V_{DD} - V_T) + \frac{V_{DD}}{1 + \alpha_T} - \frac{q}{C + C_T} \tag{2.65}$$

Similarly,

$$({Q_2}^- + {q_2}^-) - (Q_2 + q_2) = q \tag{2.66a}$$

$$V_2 = Q_2/C + V_{DD} = q_2/C_T \tag{2.66b}$$

$${V_2}^- = {Q_2}^-/C = {q_2}^-/C_T \tag{2.66c}$$

From (2.66a), (2.66b), (2.66c),

$${V_2}^- = \frac{Q_2}{C} + \frac{\alpha_T V_{DD}}{1 + \alpha_T} + \frac{q}{C + C_T} \tag{2.67}$$

From the condition (2.68) that the diode D_2 is cut off at time $j + 1/2$;

$${V_1}^- - {V_2}^- = V_T \tag{2.68}$$

and (2.65) and (2.67),

$$Q_2 = C\left(\frac{2V_{DD}}{1 + \alpha_T} - 2V_T\right) - \frac{2q}{1 + \alpha_T} \tag{2.69}$$

Similarly, from the condition that the diode D_3 is cut off at time j, and (2.66b) and (2.69),

$$Q_3 = C(\frac{2}{1+\alpha_T} + 1)V_{DD} - 3CV_T - \frac{2q}{1+\alpha_T} \tag{2.70}$$

Repeating the similar procedure, general $Q(2k-1)$ and $Q(2k)$ are calculated to be as follows.

$$Q_{2k-1} = (\frac{2(k-1)}{1+\alpha_T} + 1)CV_{DD} - (2k-1)CV_T - \frac{2(k-1)q}{1+\alpha_T} \tag{2.71a}$$

$$Q_{2k} = 2kC(\frac{V_{DD}}{1+\alpha_T} - V_T - \frac{1}{1+\alpha_T}\frac{q}{C}) \tag{2.71b}$$

From Fig. 2.28c, the following relation holds under the condition that the diode D_{N+1} is cut off at time j.

$$V_{DD} + \frac{Q_N}{C} - V_T = V_{OUT} \tag{2.72}$$

From (2.71b) and (2.72), the output voltage–current characteristic, using $2k = N$,

$$q = \frac{C + C_T}{N}[(\frac{N}{1+\alpha_T} + 1)V_{DD} - (N+1)V_T - V_{OUT}] \tag{2.73}$$

From (2.71a), (2.71b), and (2.73), the charge stored in each charge pump capacitor is represented by

$$Q_{2k-1} = \frac{2(k-1)}{N}C(V_{OUT} - V_{DD} + V_T) + C(V_{DD} - V_T) \tag{2.74a}$$

$$Q_{2k} = \frac{2k}{N}C(V_{OUT} - V_{DD} + V_T) \tag{2.74b}$$

The output current I_{OUT} is given by the following.

$$I_{OUT} \equiv \frac{q}{T} = \frac{C + C_T}{NT}[(\frac{N}{1+\alpha_T} + 1)V_{DD} - (N+1)V_T - V_{OUT}] \tag{2.75}$$

where T is the clock period. Equation (2.75) was originally derived by Dickson in 1978. I_{OUT} is rewritten by

$$I_{OUT} = \frac{V_{MAX} - V_{OUT}}{R_{PMP}} \tag{2.76}$$

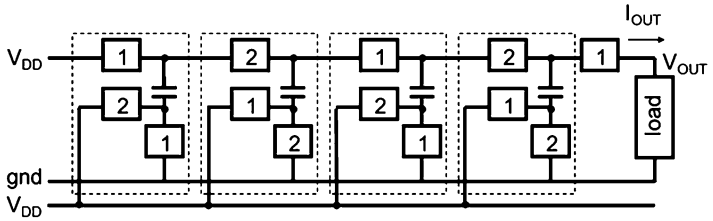


Fig. 2.29 Linear multiplier with four stages

where

$$V_{MAX} = V_{DD} + N(\frac{V_{DD}}{1+\alpha_T} - V_T) - V_T \tag{2.77}$$

$$R_{PMP} = \frac{NT}{C(1+\alpha_T)} \tag{2.78}$$

V_{MAX} is considered as the sum of the initial voltage input V_{DD}, N stages' voltage gain, each of which is $V_{\mathrm{DD}}/(1 + \alpha_{\mathrm{T}})-V_{\mathrm{T}}$, and the voltage drop in D_{N+1}. It is noted that the output resistance R_{PMP} and the maximum attainable voltage V_{MAX} are same as those of the serial–parallel pump as shown in subsection 2.2.2 in the case of $\alpha_{\mathrm{T}} = V_{\mathrm{T}} = 0$. Similar to SP, since each capacitor needs to be charged by the same amount of q in the first period, the input current supplied by V_{DD} is given by

$$I_{DD} = (N+1)I_{OUT} \tag{2.79}$$

in the ideal case where $\alpha_{\mathrm{T}} = \alpha_{\mathrm{B}} = 0$. When the maximum attainable voltage gain is defined by

$$G_V \equiv V_{MAX}/V_{DD} = N+1 \tag{2.80}$$

the current efficiency is given by

$$eff = \frac{1}{G_V} \tag{2.81}$$

Next, another procedure using K-matrix is discussed.

Figure 2.29 shows another expression of the Dickson linear multiplier with four stages. Because each stage has one input and one output in a period, as shown in Fig. 2.30, one can simply express the input and output voltages (currents) as V_{IN} and V_{OUT} (I_{IN} and I_{OUT}) without a suffix of 1 or 2. Then, the following equations hold in case of $V_{\mathrm{T}} = 0$ in phase 2:

$$I_{IN}T = q + C_T(V_{IN} - V_{OUT}) \tag{2.82}$$

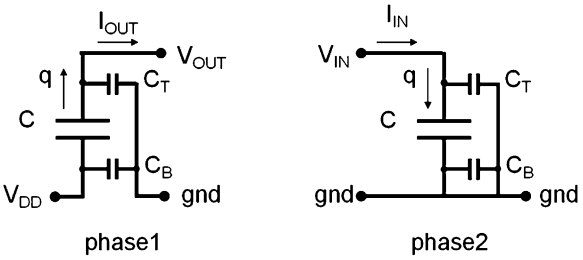


Fig. 2.30 Two alternate states of the linear multiplier

$$q = C(V_{IN} - V_{OUT} + V_{DD}) \tag{2.83}$$

and in phase 1,

$$q = I_{OUT}T + C_T(V_{OUT} - V_{IN}) \tag{2.84}$$

$$I_{DD}(1)T = I_{OUT}T + C_T(V_{OUT} - V_{IN}) + C_B V_{DD} \tag{2.85}$$

where $I_{\mathrm{DD}}(1)$ is the current supplied by V_{DD} per stage. From (2.82)–(2.84),

$$V_{OUT} - V_{IN} = \frac{V_{DD}}{1 + \alpha_T} - \frac{TI_{OUT}}{C(1 + \alpha_T)} \tag{2.86}$$

Since (2.86) represents the voltage gain per stage, the total voltage gain of N-stage multiplier is given by (2.87), which is the same as Dickson's result (2.75) in the case of $V_{\mathrm{T}} = 0$,

$$V_{OUT}(N) = (\frac{N}{1 + \alpha_T} + 1)V_{DD} - \frac{TNI_{OUT}}{C(1 + \alpha_T)} \tag{2.87}$$

The total input current from the voltage supply into N-stage multiplier, $I_{\mathrm{DD}}(N)$, is calculated with (2.85) by multiplying N and by adding one I_{IN} from the input of the first stage.

$$I_{DD}(N) = NI_{DD}(1) + I_{IN} \tag{2.88}$$

From (2.82), (2.84), and (2.85), (2.88) results in

$$\begin{aligned} I_{DD}(N) = {} & (N + 1)I_{OUT} \\ & + C_T(V_{OUT}(N) - V_{DD})/T + NC_B V_{DD}/T \end{aligned} \tag{2.89}$$

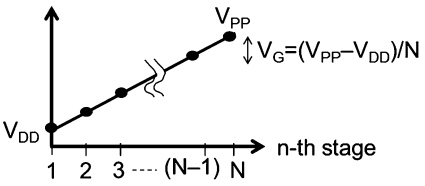


Fig. 2.31 Averaged voltage at each stage of *N*-stage Dickson pump

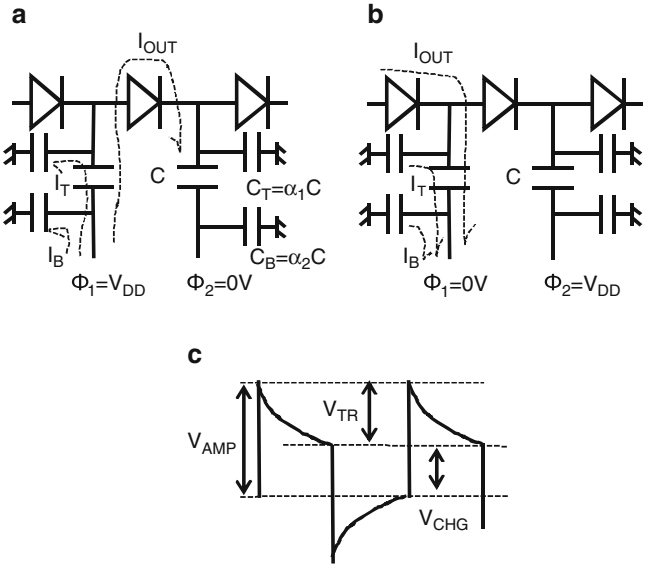


Fig. 2.32 Two neighbor stages of a charge pump in a first (**a**) and second (**b**) half period, and a voltage waveform at the top plate of a pump capacitor in a steady state (**c**)

Thus, the relationship between the output voltage and the output current and between the input and output currents of linear multiplier don't require matrix calculations, but are analytically resolved as (2.87) and (2.89), respectively.

The meaning of R_{PMP} in (2.78) is considered. Figure 2.31 illustrates the averaged voltage at each stage of *N*-stage Dickson pump. The difference voltage V_{G} between the next neighbor stages is $(V_{\mathrm{PP}} - V_{\mathrm{DD}})/N$. When V_{PP} is increased by ΔV_{PP}, V_{G} is increased by $\Delta V_{\mathrm{G}} = \Delta V_{\mathrm{PP}}/N$ and the output charge Q is decreased by ΔQ. These two are related via $\Delta Q = \mathrm{C}\Delta V_{\mathrm{G}}$. The output resistance is defined by $\Delta V_{\mathrm{PP}}/(\Delta Q/T)$, resulting in NT/C.

Three components in I_{DD} given by (2.89) can be identified as follows. Figure 2.32 shows the input current components of (1) the current from a pump capacitor to the next one which is same as the output current in steady state I_{OUT}, (2) the charging current to the parasitic capacitance at the top place ($C_{\mathrm{T}} = \alpha_{\mathrm{T}}C$) of each pump capacitor I_T, and (3) the charging current to the parasitic capacitance at the bottom

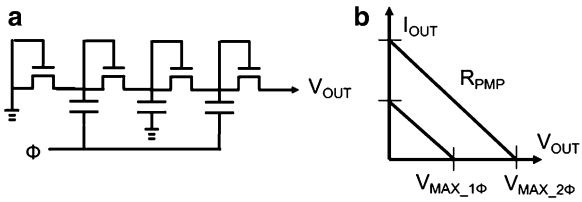


Fig. 2.33 Linear pump operating with a single phase clock (**a**) and its V_{OUT}−I_{OUT} line (**b**)

place ($C_{\mathrm{B}} = \alpha_{\mathrm{B}} C$) of each pump capacitor I_{B}, where C is the capacitance of the pump capacitor. These current components flow from the power supply V_{DD} in a half period (a) and flow to the ground in another half period (b). At the clock edge, the top plate node of each capacitor has the amplitude given by (2.90).

$$V_{AMP} = V_{DD}/(1 + \alpha_T) \tag{2.90}$$

The capacitor voltage is reduced by

$$V_{TR} = TI_{OUT}/(C + C_T) \tag{2.91}$$

due to a charge transfer of TI_{OUT}. Thus, the voltage amplitude V_{CHG} between the beginning and end of the clock high and the charging current I_{T} to the top place parasitic capacitance are given by

$$V_{CHG} = V_{AMP} - V_{TR} = (V_{PP} - V_{DD} + (N+1)V_T)/N \tag{2.92a}$$

$$I_T = C_T V_{CHG}/T \tag{2.92b}$$

where the V_{OUT}−I_{OUT} relation (2.75) is used. The current charging the bottom plate parasitic capacitance is given by (2.93).

$$I_B = C_B V_{DD}/T \tag{2.93}$$

As a result, the total input current of N-stage pump is

$$\begin{aligned} I_{DD} &= (N+1)I_{PP} + NI_T + NI_B \\ &= (N+1)I_{PP} + \alpha_T C(V_{PP} - V_{DD} + (N+1)V_T)/T \\ &\quad + N\alpha_B C_B V_{DD}/T \end{aligned} \tag{2.94}$$

Equation (2.94) in case of $V_{\mathrm{T}} = 0$ V is equivalent to (2.89)

Figure 2.33a illustrates a three stage linear pump operating with a single phase clock. Two of three stages contribute to charge pumping, resulting in a lower maximum attainable voltage than a two phase clock pump with the same number of stages, as shown by (2.95a) where $V_{\mathrm{MAX\_1\Phi}}$ is the voltage amplitude of the single clock and $V_{\mathrm{MAX\_2\Phi}}$ is the voltage amplitude of the two phase clock. However, the output impedance is the same because Fig. 2.31 is valid regardless of the number of

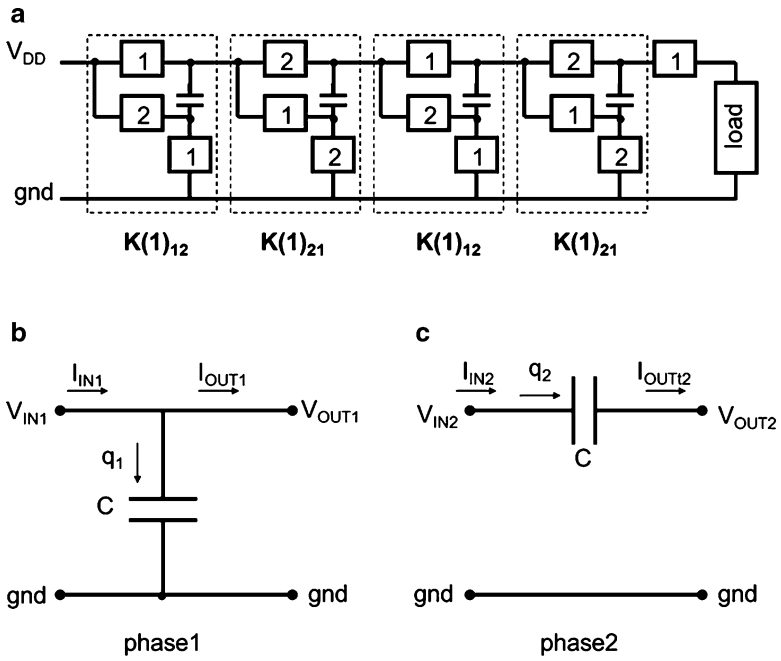


Fig. 2.34 Four-stage Fibonacci multiplier (Harada et al. 1992)

phases, as shown by (2.95b). As a result, the single phase clock pump has the $V_{\mathrm{OUT}}-I_{\mathrm{OUT}}$ line as shown in Fig. 2.33b in comparison with that of the two phase clock pump.

$$V_{MAX\_1\varphi} = V_{DD}(N+1)/2 = V_{MAX\_2\varphi}/2 \tag{2.95a}$$

$$R_{PMP} = \frac{T}{C}N \tag{2.95b}$$

2.2.4 Fibonacci (FIB) Multiplier

This subsection starts with zero parasitic capacitance and then analyzes the Fibonacci multiplier with a finite parasitic capacitance.

Figure 2.34a illustrates a Fibonacci multiplier with four stages, which work with a two-phase clock. The squares show switches, and the numbers 1 and 2 inside indicate turning on in phase 1 and 2 of the clock, respectively. The two-port transfer matrix $\mathbf{K}(N)$ is again defined by (2.96).

$$[V_{IN1} \quad V_{IN2} \quad I_{IN1} \quad I_{IN2}]^T = \mathbf{K}(N)[V_{OUT1} \quad V_{OUT2} \quad I_{OUT1} \quad I_{OUT2}]^T \tag{2.96}$$

Each stage of the multiplier has two operation states as shown in Fig. 2.34b, c, where C is the multiplier capacitor. In steady states, the following equations hold with the assumption that any parasitic resistance and capacitance can be ignored.

$$V_{IN1} = V_{OUT1} \tag{2.97}$$

$$(I_{IN1} - I_{OUT1})T/2 = q_1 \tag{2.98}$$

$$q_1 = C(V_{OUT1} - V_{OUT2} + V_{IN2}) \tag{2.99}$$

$$q_2 = I_{IN2}T/2 = I_{OUT2}T/2 \tag{2.100}$$

From the steady state condition of $q_1 = q_2$, the K-matrix in case of 1 stage, $\mathbf{K}(1)_{12}$ is calculated as (2.101),

$$\mathbf{K}(1)_{12} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -1 & 1 & 0 & R \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{2.101}$$

where $R = T/2C$. The K-matrix of Ueno Fibonacci multiplier for even stages as shown in Fig. 2.34a, $\mathbf{K}(1)_{21}$, is given by simply exchanging the suffix 1 with 2 for V_{IN} and V_{OUT} of (2.97)–(2.100).

$$\mathbf{K}(1)_{21} = \begin{bmatrix} 1 & -1 & R & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \tag{2.102}$$

As shown in Fig. 2.34a, entire K-matrix of N-stage UF multiplier is calculated by (2.103) in the case of even number of stages and by (2.104) in the case of odd number of stages, respectively.

$$\mathbf{K}_{\mathbf{UF}}(2n) = (\mathbf{K}(1)_{12}\mathbf{K}(1)_{21})^n \tag{2.103}$$

$$\mathbf{K}_{\mathbf{UF}}(2n+1) = (\mathbf{K}(1)_{12}\mathbf{K}(1)_{21})^n\mathbf{K}(1)_{12} \tag{2.104}$$

For Ueno Fibonacci multiplier with odd number of stages, the output current I_{OUT} is $I_{\mathrm{OUT2}}/2$ since the averaged time of period for I_{OUT} is twice as long as that for I_{OUT2}, the output voltage V_{OUT} is V_{OUT2}, $I_{\mathrm{OUT1}} = 0$, and $V_{\mathrm{IN1}} = V_{\mathrm{IN2}} = V_{\mathrm{DD}}$. Thus, the following equation holds for Ueno Fibonacci multiplier with odd number of stages.

Table 2.3 V_{MAX} and R_{PMP} as a function of the number of stage N

N	V_{MAX} (N)/V_{DD}	R_{PMP} (N)
1	2	$1^2/C_1$
2	3	$1^2/C_2 + 1^2/C_1$
3	5	$1^2/C_3 + 1^2/C_2 + 2^2/C_1$
4	8	$1^2/C_4 + 1^2/C_3 + 2^2/C_2 + 3^2/C_1$
n	$F(n+1)$	$\sum_{j=0}^{n-1} F(j)^2/C_{N-j}$

$$[V_{DD} \quad V_{DD} \quad I_{IN1} \quad I_{IN2}]^T = \mathbf{K_{UF}}(2n+1)[V_{OUT1} \quad V_{OUT} \quad 0 \quad 2I_{OUT}]^T \tag{2.105}$$

The relation between V_{OUT} and I_{OUT} is calculated by the first and second row of (2.105) by eliminating V_{OUT1}. The total current consumption I_{IN} is calculated by $(I_{IN1} + I_{IN2})/2$ with certain values of V_{OUT} and I_{OUT}. For the UF multiplier with even number of stages, it is valid when the conditions of $I_{OUT} = I_{OUT1}/2$, $V_{OUT} = V_{OUT1}$, and $I_{OUT2} = 0$ are used instead. Thus,

$$[V_{DD} \quad V_{DD} \quad I_{IN1} \quad I_{IN2}]^T = \mathbf{K_{UF}}(2n)[V_{OUT} \quad V_{OUT2} \quad 2I_{OUT} \quad 0]^T \tag{2.106}$$

One can easily calculate the output voltage–current characteristics and the current consumption or efficiency with the circuit parameters, such as C, T, N, given by using a simple matrix calculator (2.105) or (2.106).

$$I_{OUT} = \frac{V_{MAX} - V_{OUT}}{R_{PMP}} \tag{2.107}$$

where $V_{IN1,2}$ is V_{DD} and $F(j)$ is jth Fibonacci number and $F(0) = F(1) = 1$, $F(j+2) = F(j+1) + F(j)$. In case where the capacitance of each capacitor is not same among N capacitors, R_{PMP} is generally written as

$$R_{PMP}(N) = \sum_{j=0}^{N-1} \frac{F(j)^2}{C_{N-j}} \tag{2.108}$$

Table 2.3 summarizes the characteristic parameters of UF multipliers.

Under the condition that the total capacitor area is given, optimum distribution exists so that R_{PMP} is minimized. One can use Lagrange multiplier introducing functions f and g, and a parameter λ as follows, where C_{TOT} is the total capacitance of N capacitors.

$$f(C_1, C_2, \cdots, C_N) \equiv \sum_{j=1}^{N} C_j - C_{TOT} = 0 \tag{2.109a}$$

$$g(C_1, C_2, \cdots, C_N, \lambda) \equiv R_{PMP}(C_1, C_2, \cdots, C_N) - \lambda f(C_1, C_2, \cdots, C_N) \quad (2.109b)$$

$$\frac{\partial}{\partial C_j} g(C_1, C_2, \cdots, C_N) = -\left(\frac{F(N-j)}{C_j}\right)^2 - \lambda = 0 \quad (2.109c)$$

Equation (2.109c) holds when (2.110) holds.

$$C_1{:}C_2{:}C_3{:}C_4{:}\ldots{:}C_{N-1}{:}C_N = F(N-1){:}F(N-2){:}\ldots{:}F(0) \quad (2.110)$$

$$R_{PMP}(N) = \frac{N}{C_{TOT}} \left(\sum_{j=0}^{N-1} F(j)\right)^2 \quad (2.111)$$

When the maximum attainable voltage gain is defined by

$$G_V \equiv V_{MAX}/V_{DD} = F(N+1) \quad (2.112)$$

the current efficiency is given by

$$eff = \frac{1}{G_V} \quad (2.113)$$

$$I_{DD} = G_V I_{OUT} \quad (2.114)$$

Next, the circuit analysis is done in case where the parasitic capacitance is considered.

Each stage has two operation states as shown in Fig. 2.35b, c, where C is the multiplier capacitor, C_T is the parasitic capacitance at one of the terminals of C, and C_B is the parasitic capacitance at the other terminal of C. In steady states, the following equations hold with the assumption that any parasitic resistance can be ignored.

$$V_{IN1} = V_{OUT1} \quad (2.115)$$

$$(I_{IN1} - I_{OUT1})T/2 = q_1 + C_1(V_{OUT1} - V_{OUT2}) \quad (2.116)$$

$$q_1 = C(V_{OUT1} - V_{OUT2} + V_{IN2}) \quad (2.117)$$

$$q_2 = I_{IN2}T/2 - C_2 V_{IN2} = I_{OUT2}T/2 + C_1(V_{OUT2} - V_{OUT1}) \quad (2.118)$$

where q_1 and q_2 are the charge flowing into C in phase 1 and 2, respectively. From the steady state condition of $q_1 = q_2$, the K-matrix in case of one stage, $\mathbf{K}_P(1)_{12}$ is calculated as (2.119),

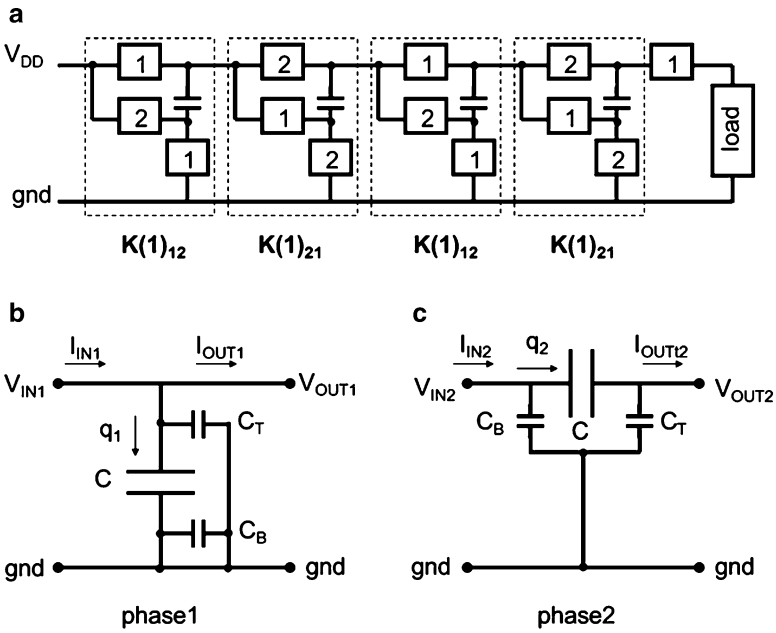


Fig. 2.35 Four-stage Fibonacci multiplier with a finite parasitic capacitance considered

$$\mathbf{K}_P(1)_{12} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -(1+\alpha_T) & (1+\alpha_T) & 0 & R \\ 0 & 0 & 1 & 1 \\ -1/r_T - (1+\alpha_T)/r_B & 1/r_T + (1+\alpha_T)/r_B & 0 & (1+\alpha_B) \end{bmatrix} \tag{2.119}$$

where $\alpha_i = C_i/C$, $r_i = T/2C_i$ $(i = T, B)$, and $R = T/2C$. The K-matrix of Fibonacci multiplier with even stages as shown in Fig. 2.35a, $\mathbf{K}_P(1)_{21}$ is given by simply exchanging the suffix 1 with 2 for V_{IN} and V_{OUT} of (2.115)–(2.118).

$$\mathbf{K}_P(1)_{21} = \begin{bmatrix} (1+\alpha_T) & -(1+\alpha_T) & R & 0 \\ 0 & 1 & 0 & 0 \\ 1/r_T + (1+\alpha_T)/r_B & -1/r_T - (1+\alpha_T)/r_B & (1+\alpha_B) & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \tag{2.120}$$

As shown in Fig. 2.35a, entire K-matrix of N-stage FIB multiplier is calculated by (2.121) in the case of even number of stages and by (2.122) in the case of odd number of stages, respectively.

$$\mathbf{K}_P(2n) = (\mathbf{K}_P(1)_{12}\mathbf{K}_P(1)_{21})^n \tag{2.121}$$

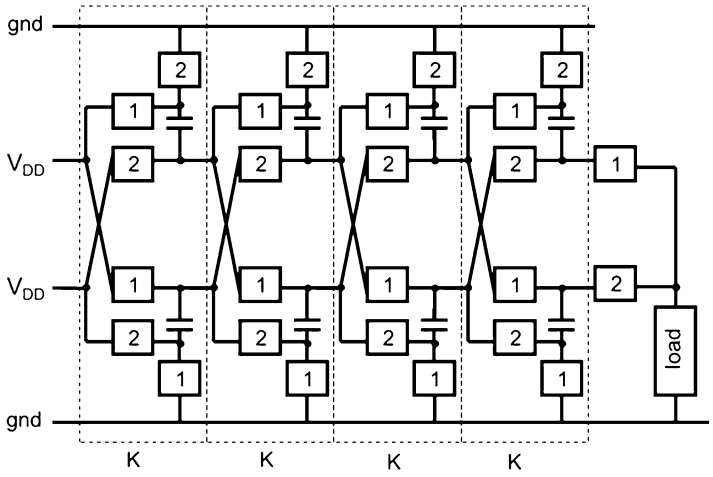


Fig. 2.36 Four-stage 2^N multiplier (Cernea 1995)

$$\mathbf{K}_P(2n+1) = (\mathbf{K}_P(1)_{12}\mathbf{K}_P(1)_{21})^n\mathbf{K}_P(1)_{12} \tag{2.122}$$

For the UF with odd number of stages, the output current I_{OUT} is $I_{\mathrm{OUT2}}/2$ since the averaged time of period for I_{OUT} is twice as long as that for I_{OUT2}, the output voltage V_{OUT} is V_{OUT2}, $I_{\mathrm{OUT1}} = 0$, and $V_{\mathrm{IN1}} = V_{\mathrm{IN2}} = V_{\mathrm{DD}}$. Thus, the following equation holds for the UF with odd number of stages.

$$[V_{DD} \quad V_{DD} \quad I_{IN1} \quad I_{IN2}]^T = \mathbf{K}_P(2n+1)[V_{OUT1} \quad V_{OUT} \quad 0 \quad 2I_{OUT}]^T \tag{2.123}$$

The relation between V_{OUT} and I_{OUT} is calculated by the first and second row of (2.123) by eliminating V_{OUT1}. The total current consumption I_{IN} is calculated by $(I_{\mathrm{IN1}} + I_{\mathrm{IN2}})/2$ with certain values of V_{OUT} and I_{OUT}. For the UF multiplier with even number of stages, it is valid when the conditions of $I_{\mathrm{OUT}} = I_{\mathrm{OUT1}}/2$, $V_{\mathrm{OUT}} = V_{\mathrm{OUT1}}$, and $I_{\mathrm{OUT2}} = 0$ are used instead. Thus,

$$[V_{DD} \quad V_{DD} \quad I_{IN1} \quad I_{IN2}]^T = \mathbf{K}_P(2n)[V_{OUT} \quad V_{OUT2} \quad 2I_{OUT} \quad 0]^T \tag{2.124}$$

2.2.5 2^{N} Multiplier

This subsection starts with zero parasitic capacitance and then analyzes the 2^N multiplier with a finite parasitic capacitance.

Figure 2.36 shows the one with four stages. Figure 2.37 illustrates two alternate states. Equations (2.125) and (2.126) hold in phase 1.

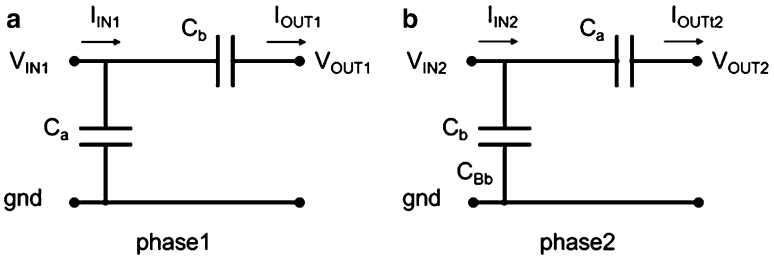


Fig. 2.37 Two phases of 2^N multiplier with no parasitic capacitance

$$I_{IN1}T/2 = C_a(V_{IN1} - V_{OUT2} + V_{IN2}) + C_b(V_{IN1} - V_{OUT1} + V_{IN2}) \tag{2.125}$$

$$I_{OUT1}T/2 = C_b(V_{IN2} - V_{OUT1} + V_{IN1}) \tag{2.126}$$

When $C_a = C_b = C/2$, phase 1 and 2 are identical. In this case, the input and output voltage (current) can be written by V_{IN} and V_{OUT} (I_{IN} and I_{OUT}) without differentiating the two states. Using this symmetry between phase 1 and 2, K-matrix can be reduced to 2×2. The matrix for jth stage is given by

$$\tilde{\mathbf{K}}(j) = \begin{bmatrix} \frac{1}{2} & R(j) \\ 0 & 2 \end{bmatrix} \tag{2.127}$$

$$R(j) = \frac{1}{2C(j)} \tag{2.128}$$

where T is assumed to be one. The matrix for n-stage pump $K(n)$ is written by

$$\mathbf{K}(n) = \mathbf{K}(n-1)\tilde{\mathbf{K}}(n) \tag{2.129}$$

$$\mathbf{K}(n) = \begin{bmatrix} a(n) & e(n) \\ b(n) & d(n) \end{bmatrix} \tag{2.130}$$

From (2.127), (2.129), and (2.130),

$$\begin{aligned} \begin{bmatrix} a(n) & e(n) \\ b(n) & d(n) \end{bmatrix} &= \begin{bmatrix} a(n-1) & e(n-1) \\ b(n-1) & d(n-1) \end{bmatrix} \begin{bmatrix} \frac{1}{2} & R(n) \\ 0 & 2 \end{bmatrix} \\ &= \begin{bmatrix} \frac{1}{2}a(n-1) & R(n)a(n-1) + 2e(n-1) \\ \frac{1}{2}b(n-1) & R(n)b(n-1) + 2d(n-1) \end{bmatrix} \end{aligned} \tag{2.131}$$

Using the initial condition,

$$\begin{bmatrix} a(1) & e(1) \\ b(1) & d(1) \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & R(1) \\ 0 & 2 \end{bmatrix} \tag{2.132}$$

The components are solved as

$$a(n) = 2^{-n} \tag{2.133}$$

$$b(n) = 0 \tag{2.134}$$

$$e(n) = 2^{-n+1}R(n) + 2e(n-1) \tag{2.135}$$

$$d(n) = 2^{n} \tag{2.136}$$

From (2.132) and (2.135), $e(n)$ is solved as

$$e(n) = \sum_{j=1}^{n} 2^{n-2j+1}R(j) \tag{2.137}$$

The output resistance of the pump is calculated as

$$R_{PMP}(N) = \frac{e(N)}{a(N)} = \sum_{j=1}^{N} 2^{2N-2j}R(j) = \sum_{j=1}^{N} \frac{2^{2N-2j}}{C(j)} \tag{2.138}$$

In case where all capacitors are equivalently divided, i.e.,

$$C(j) = \frac{C_{TOT}}{N} \tag{2.139a}$$

R_{PMP} is given by

$$R_{PMP}(N) = \frac{N}{C_{TOT}} \sum_{j=1}^{N} 2^{2N-2j} = \frac{N}{C_{TOT}} \left(\frac{2}{3}N(N-1)(2N-1) + 1\right) \tag{2.139b}$$

In case where each capacitor is weighted so that the output resistance is minimized, one can use Lagrange multiplier introducing functions f and g, and a parameter λ as follows.

$$f(C_1, C_2, \cdots, C_N) \equiv \sum_{j=1}^{N} C_j - C_{TOT} = 0 \tag{2.140a}$$

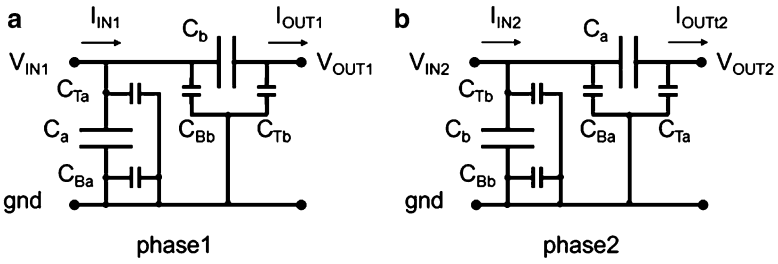


Fig. 2.38 Two phases of 2^N multiplier with a finite parasitic capacitance C_T, C_B

$$g(C_1, C_2, \cdots, C_N, \lambda) \equiv R_{PMP}(C_1, C_2, \cdots, C_N) - \lambda f(C_1, C_2, \cdots, C_N) \tag{2.140b}$$

$$\frac{\partial}{\partial C_j} g(C_1, C_2, \cdots, C_N) = -\frac{2^{2N-2j}}{{C_j}^2} - \lambda = 0 \tag{2.140c}$$

From (2.140c),

$$\frac{2^{2N-2}}{{C_1}^2} = \frac{2^{2N-4}}{{C_2}^2} = \cdots = \frac{2^0}{{C_N}^2} \tag{2.140d}$$

Therefore,

$$C(j) = C_{TOT} \frac{2^{N-j}}{2^N - 1} \tag{2.140e}$$

From (2.138) and (2.140e), R_{PMP} is given by

$$R_{PMP}(N) = \frac{(2^N - 1)^2}{C_{TOT}} \tag{2.140f}$$

Next, the 2^N pump with a finite parasitic capacitance is considered using Fig. 2.38 instead of Fig. 2.37.

Equations (2.141) and (2.142) hold in phase 1.

$$\begin{aligned} I_{IN1}T/2 = {} & C_a(V_{IN1} - V_{OUT2} + V_{IN2}) + C_{Ta}(V_{IN1} - V_{OUT2}) \\ & + C_{Bb}V_{in1} + C_b(V_{IN1} - V_{OUT1} + V_{IN2}) \end{aligned} \tag{2.141}$$

$$I_{OUT1}T/2 = C_b(V_{IN2} - V_{OUT1} + V_{IN1}) + C_{Tb}(V_{IN2} - V_{OUT1}) \tag{2.142}$$

When $C_a = C_b = C/2$, $C_{Ta} = C_{Tb} = C_T/2$, and $C_{Ba} = C_{Bb} = C_B/2$, where a factor of 2 is included for two array structure, phase 1 and 2 are identical. In this case, the input and output voltage (current) can be written by V_{IN} and V_{OUT} (I_{IN} and

I_{OUT}) without differentiating the two states. Using this symmetry between phase 1 and 2, K-matrix can be reduced to 2×2;

$$\begin{bmatrix} V_{IN} \\ I_{IN} \end{bmatrix} = \mathbf{K}_{2N}(N) \begin{bmatrix} V_{OUT} \\ I_{OUT} \end{bmatrix} \tag{2.143}$$

$$\mathbf{K}_{2N}(N) = \mathbf{K}(1)^N \tag{2.144}$$

$$\mathbf{K}(1) = \frac{1}{2+\alpha_T} \begin{bmatrix} 1+\alpha_T & 2R \\ \dfrac{\alpha_T + \alpha_B + \alpha_T\alpha_B}{2R} & 4+\alpha_T+\alpha_B \end{bmatrix} \tag{2.145}$$

where $\alpha_i = C_i/C$, $r_i = T/2C_i$ ($i = T, B$), and $R = T/2C$. The output voltage and current relation is calculated in the first row of (2.143) with $V_{\mathrm{IN}} = V_{\mathrm{DD}}$ and I_{IN} is calculated in the second row.

2.2.6 Comparison of Five Topologies

2.2.6.1 Ideal Case Where the Parasitic Capacitance Is Negligibly Small

Table 2.4 summarizes pump characteristic parameters such as the maximum attainable output voltage (V_{MAX}) in case of $V_{\mathrm{DD}} = 1$ or equivalently the voltage gain (G_{V}), the output impedance (R_{PMP}), the current efficiency, the maximum voltage applied to two terminals of a pumping capacitor (V_{CAP}), and the maximum voltage applied to a switching device (V_{SW}). Except for the serial–parallel and the liner pumps, there is an optimum weight for the pumping capacitors to make R_{PMP} minimized under the condition of a given area. The table includes both cases of non-weighted, i.e., equal sized capacitor and weighted capacitor.

2.2.6.2 Area and Current Efficiency Comparison

Next, let us compare those five topologies in more realistic case where the parasitic capacitance is not negligibly small, which is valid for on-chip high-voltage generation.

The optimum number of stages (N_{OPT}) is determined under the condition that the output current maximizes with a constant entire capacitor area $\Sigma C(i)$ using the K-matrix. This procedure is done for various output voltages and parasitic capacitance conditions for each of the multipliers. Then, the capacitor is calculated to output a certain current at a given output voltage with a given parasitic capacitance. Thus, the multipliers are designed and compared with respect to the total capacitor area. In the following figures, for simplicity, it is assumed that (1) C_i is proportional

Table 2.4 Characteristic parameters in case of negligibly small parasitic capacitance

			R_{PMP}			Current		
		V_{MAX} or G_{V}	Uniform cap	Weighted cap	Each cap $C(j)$	efficiency	V_{CAP} (Max)	V_{SW} (Max)
CW	(*N*: even)	$N+1$	$\frac{N^2(N+1)(N+2)}{12C_{TOT}}$	$\frac{N^2(N+2)^2}{16C_{TOT}}$	$C_{2\mathrm{j}-1}$ $C_{2\mathrm{j}}$ $\propto (N/2-j+1)$	$\frac{1}{G_V}$	1	1
	(*N*: odd)		$\frac{N(N+1)(N^2+2N+3)}{12C_{TOT}}$	$\frac{(N+1)^4}{16C_{TOT}}$	$\propto \left(\frac{N+1}{2}-j+1\right)$ $\propto \left(\frac{N-1}{2}-j+1\right)$			
SP			$\frac{N^2}{C_{TOT}}$	$\frac{N^2}{C_{TOT}}$	C_{TOT}/N		1	N
Dickson							N	1
Fibonacci		$F(N+1)$	$\frac{N}{C_{TOT}}\sum_{j=0}^{N-1}F(j)^2$	$\frac{N}{C_{TOT}}\left(\sum_{j=0}^{N-1}F(j)\right)^2$	$\propto F(N-j)$		$F(N-1)$	
$2N$		2^N	$\frac{N}{C_{TOT}}\left(\frac{2}{3}N(N-1)(2N-1)+1\right)$	$\frac{(2^N-1)^2}{C_{TOT}}$	$C_{TOT}\frac{2^{N-j}}{2^N-1}$		2^{N-1}	

to C so that α_i doesn't depend on C, (2) $\alpha_T = \alpha_B$ except for a special case with $\alpha_T = 0.01$ and $\alpha_B = 0.1$, (3) every stage has a same value for C except for Fibonacci case2 (FIB2) where the values for Cs are varied per stage as described later.

(*A*) *Optimum number of stages*

Figure 2.39a–e shows the optimum stages (N_{OPT}) as a function of voltage gain with a constant current load. The Fibonacci multiplier has the smallest output resistance when $C(i)$ is proportional to Fib($N-i$), where i indicates ith stage and Fib(j) is the jth Fibonacci number. SP has a linear dependency on the voltage gain (G_V) as the Dickson (LIN). On the other hand, N_{OPT} of the other multipliers has dependencies as $\log(G_V)$. Figure 2.39f, g, h compare five multipliers with $\alpha_T = \alpha_B = 0.01$ (f), $\alpha_T = 0.01$ and $\alpha_B = 0.1$ (g), and $\alpha_T = \alpha_B = 0.1$ (h). Even with

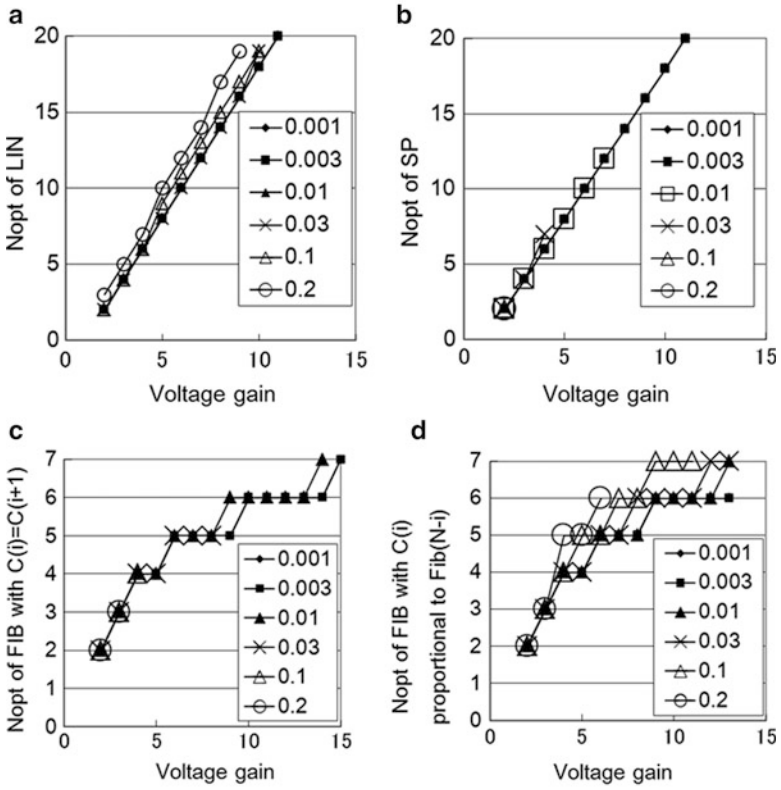


Fig. 2.39 Optimum number of stages as a function of voltage gain with various $\alpha_T = \alpha_B$ of 0.001 to 0.2 for (**a**) linear (LIN), (**b**) serial–parallel (SP), (**c**) Fibonacci with $C(i+1) = C(i)$ ($i = 1,.., N-1$) (FIB1), (**d**) Fibonacci with weighted C (FIB2), and (**e**) 2^N multipliers. Comparisons of the optimum number of stages as a function of voltage gain with $\alpha_T = \alpha_B = 0.01$ (**f**), with $\alpha_T = 0.01$, $\alpha_B = 0.1$ (**g**), and with $\alpha_T = \alpha_B = 0.1$ (**h**). Comparison of the multiplication factors as a function of $\alpha_T(j)$ and $\alpha_B(k)$ for LIN with different optimization methods

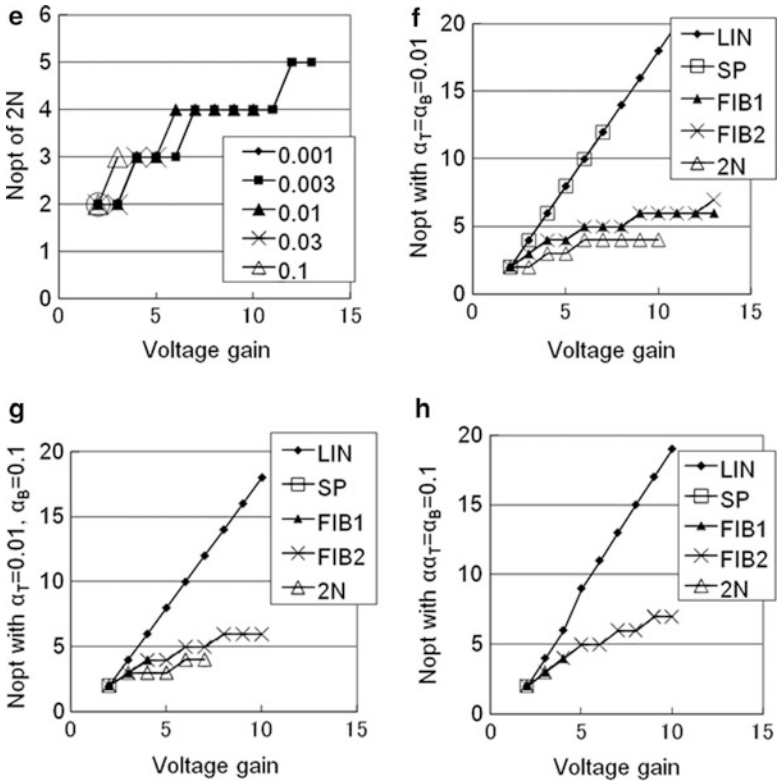


Fig. 2.39 (continued)

$\alpha_T = \alpha_B$=0.01, SP cannot generate a voltage gain higher than 7, whereas the others can generate voltage gains higher than 10 or more, as shown in Fig. 2.39f. This result shows that the parasitic capacitance decreases the output current as the number of stages in the series increases. With α_T of 0.1, which is a typical value in cases of integrated multipliers; however, only LIN and FIB2 can generate a voltage gain of 10 or more. Neither FIB1 nor 2^N can generate a voltage gain of 8 or more, as shown in Fig. 2.39g, h. With $\alpha_T = \alpha_B = 0.01$, 2^N only needs the number of stages of 4, which is less by 2 than FIB2 does in case of a voltage gain of 10 as shown in Fig. 2.39f.

(*B*) *Circuit area*

Using the values for N_{OPT} calculated, as shown in Fig. 2.39, the values for C per stage are calculated to output a specific current for each voltage gain, each α, and each multiplier. Figure 2.40 shows the circuit area, which is defined by $\Sigma C(i)$ as a measure, compared to that of LIN. As shown in Fig. 2.40a, SP can have an equivalent area as LIN does as far as both α and voltage gains are small, but SP becomes very sensitive to α higher than 0.01. FIB1, FIB2, and 2^N have smaller sensitivity than SP, as shown in Fig. 2.40b–d, but they also become very sensitive to

α higher than 0.03. Figure 2.40e–g compare the area ratios of four multipliers to LIN with $\alpha_T = \alpha_B = 0.01$ (e), $\alpha_T = 0.01$ and $\alpha_B = 0.1$ (f), and $\alpha_T = \alpha_B = 0.1$ (g). Among those four, only FIB2 has similar area as LIN in case of α_B of 0.01, but each needs much more area than LIN in case of α_B of 0.1. For example, FIB2 with a voltage gain of 10 needs an area that is five times larger than LIN in case of $\alpha_T = \alpha_B = 0.1$, as shown in Fig. 2.40g.

Thus, LIN has minimum total capacitor area among the multipliers in case of α_T and α_B of 0.1 or higher which are typical numbers in integrated circuits. In case of α_T and α_B of 0.01 or smaller, LIN and FIB2 have smaller area than the others do under the condition of a voltage gain of 10 or smaller. Such a small parasitic capacitance is realized in discrete application.

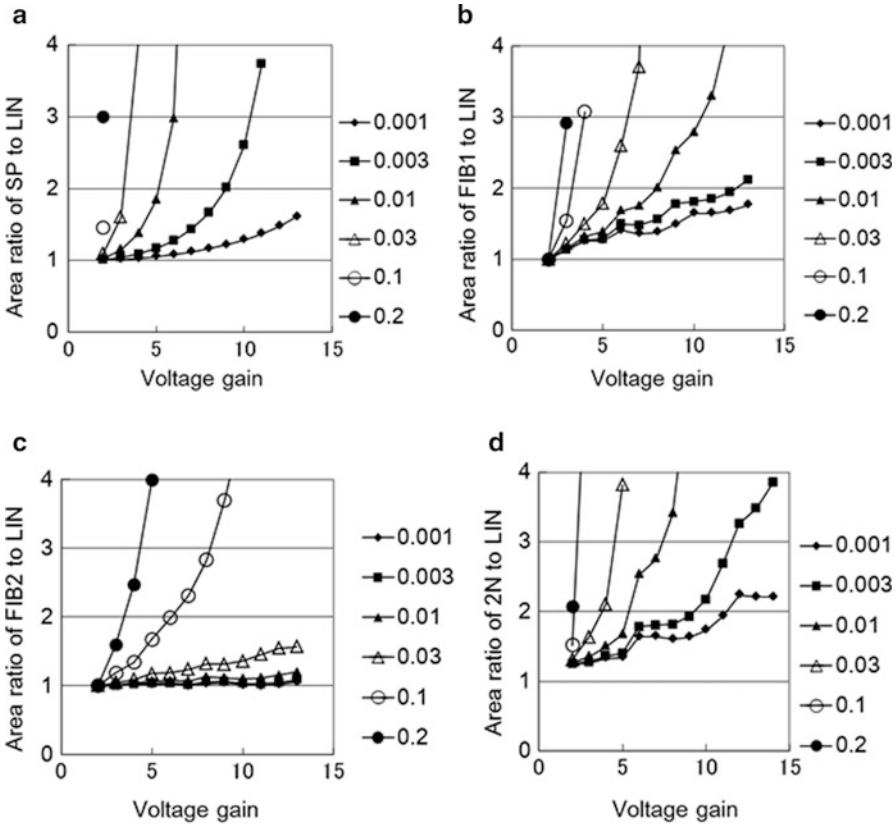


Fig. 2.40 Area ratio of (**a**) SP, (**b**) FIB1, (**c**) FIB2, (**d**) 2*N* with optimum number of stages to LIN as a function of voltage gain with various $\alpha_T = \alpha_B$ of 0.001 to 0.2. Comparisons of the area ratio as a function of voltage gain with $\alpha_T = \alpha_B = 0.01$ (**e**), with $\alpha_T = 0.01$, $\alpha_B = 0.1$ (**f**), and with $\alpha_T = \alpha_B = 0.1$ (**g**). Comparisons of the area ratio as a function of α_T (=α_B) with a voltage gain of 3 (**h**), 6 (**i**), and 10 (**j**)

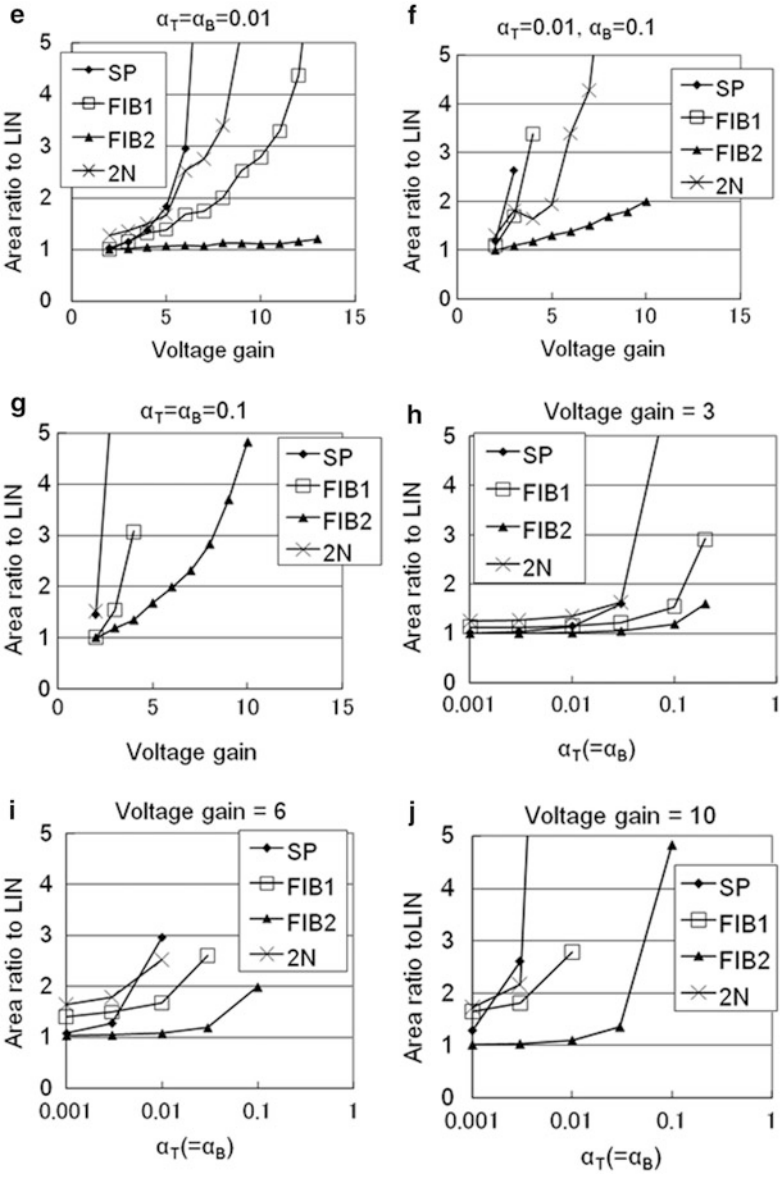


Fig. 2.40 (continued)

(*C*) *Current efficiency*

Current efficiency is defined by I_{OUT}/I_{IN}. Figure 2.41 shows ratios of the efficiency of the other four multipliers to that of LIN. Because the efficiency strongly depends on the number of stages, nonmonotinic dependencies on the

voltage gain are observed in FIB1, FIB2, and 2^N due to different dependencies of N_{OPT} on the voltage gain against LIN. In case of α_T and α_B of 0.01, FIB2 and 2^N have similar efficiencies as LIN within +/−30% up to a voltage gain of 10, as shown in Fig. 2.41e. However, in case of α of 0.1, any multiplier decreases the efficiency monotonically, as shown in Fig. 2.41f, g. The efficiency of FIB2 is degraded to about 0.3 of that of LIN at a voltage gain of 10 in case of $\alpha_T = 0.01$ and $\alpha_B = 0.1$, as shown in Fig. 2.41f.

(D) *Number of discrete capacitors*

In order to compare the number of discrete capacitor components among the multipliers for discrete applications, 2^N multiplier needs to use N_{CAP} defined by $2N_{OPT}$ rather than N_{OPT} itself as shown in Fig. 2.39e. N_{CAP} of the rest of the multipliers is same as N_{OPT}. Figure 2.42a, b is, respectively, identical to

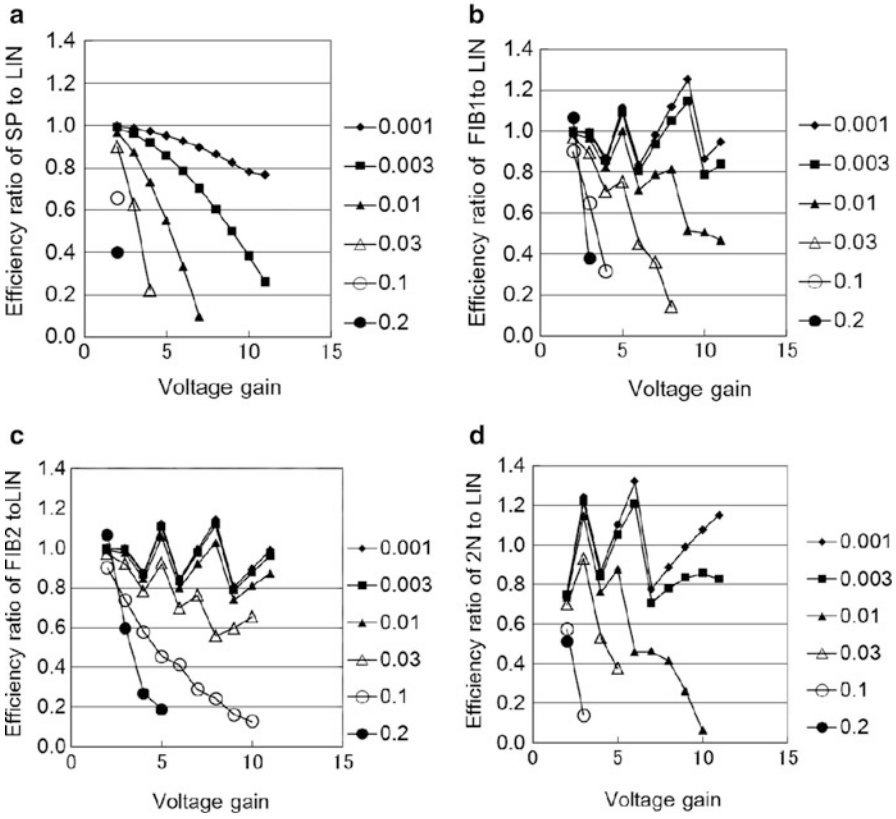


Fig. 2.41 Current efficiency ratio of (**a**) SP, (**b**) FIB1, (**c**) FUB2, (**d**) 2*N* with optimum number of stages to LIN as a function of voltage gain with various $\alpha_T = \alpha_B$ of 0.001 to 0.2. Comparison of the efficiency ratio as a function of voltage gain with $\alpha_T = \alpha_B = 0.01$ (**e**), with $\alpha_T = 0.01$, $\alpha_B = 0.1$ (**f**), and with $\alpha_T = \alpha_B = 0.1$ (**g**). Comparisons of the efficiency ratio as a function of $\alpha_T(=\alpha_B)$ with a voltage gain of 3 (**h**), 6 (**i**), and 10 (**j**)

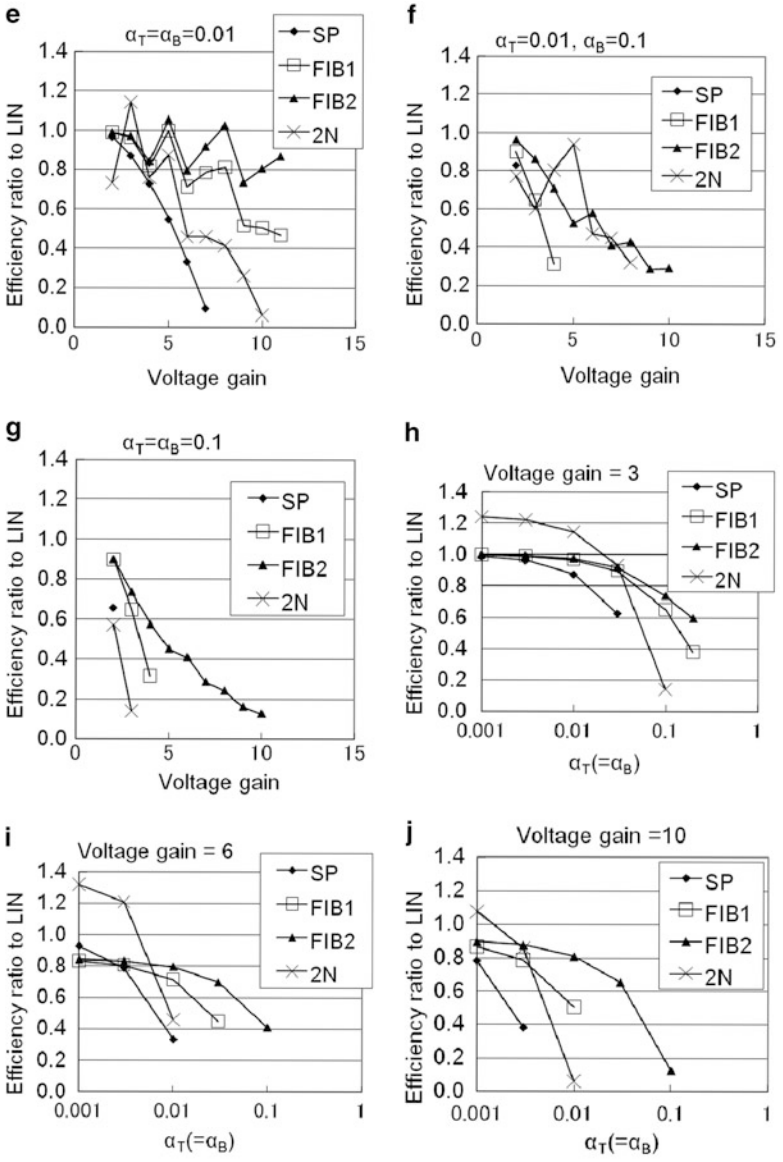


Fig. 2.41 (continued)

Fig. 2.39f, h except for the vertical axis. Figure 2.42 shows FIB has the least number of capacitors among the multipliers. For example, N_{CAP} of FIB is about one-third of that of LIN in case of a voltage gain of 10 and $\alpha_T = \alpha_B = 0.01$.

As a result, the linear Dickson cell is the best for integration because of the smallest total capacitor area and the highest current or power efficiency under

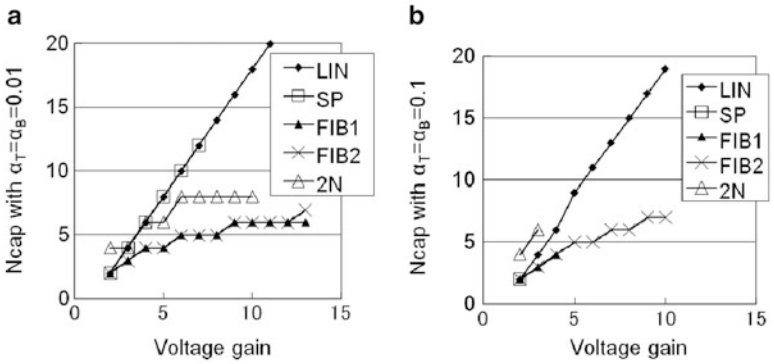


Fig. 2.42 Comparison of the number of discrete capacitors

the assumption that the parasitic capacitance is not smaller than 10% of the multiplier capacitance, and Fibonacci cell is the best for discrete application because of the minimum number of capacitor components with moderate current or power efficiency under the assumption that the parasitic capacitance is not larger than 1% of the multiplier capacitance.

2.3 Dickson Pump Design

This section discusses a dynamic behavior from the time when the pump operation starts to the time when the output voltage reaches the target voltage. The equivalent circuit is extracted from the behavioral equation. After that, several circuit optimizations are shown including optimization of the clock frequency to maximize the output current, that of the number of stages to minimize the rise time and that of the number of stages to minimize the input power.

2.3.1 Equivalent Circuit Model

(A) Dynamic behavior

This subsection discusses dynamic behavior of the Dickson charge pump and extracts the equivalent circuit model. Figure 2.43 illustrates three stage Dickson pump. ΔQ_i (i = 1–3, OUT) indicates increased amount of charges in each capacitor in the time period T_R.

In order to derive the recurrence formula of the output voltage, the total charge consumed by the charge pump during boosting is obtained by two different methods; by using the charge stored in each capacitor as shown in Fig. 2.44a, b and by using the sum of the charge consumed by the charge pump in one cycle time

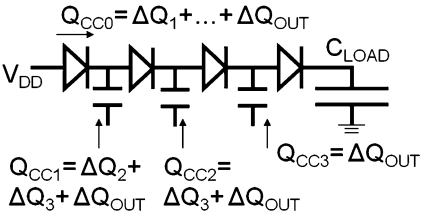


Fig. 2.43 Charges supplied by V_{DD} in T_R

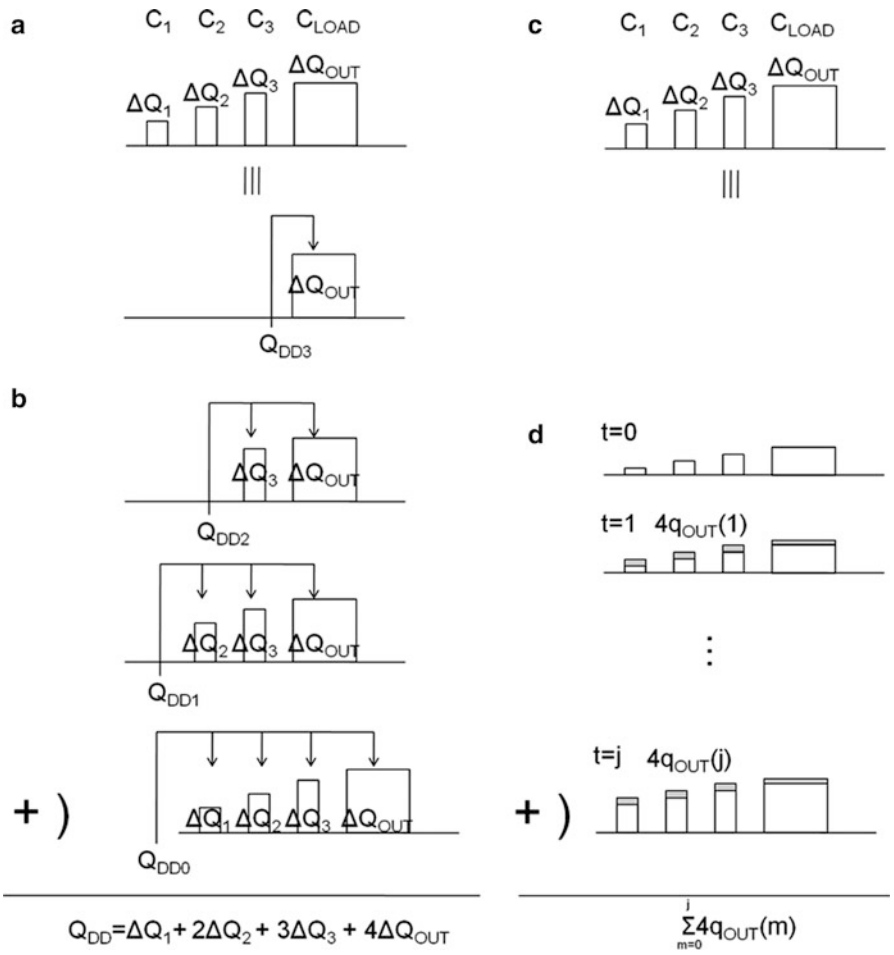


Fig. 2.44 Two methods for calculating the total input charges; method 1 with (**a**) and (**b**) and method 2 with (**c**) and (**d**)

as shown in Fig. 2.44c, d. Firstly, the total charge $Q_{\mathrm{DD}}{}^{\mathrm{d}}(j)$ consumed by the charge pump during the arbitrary time j is calculated using the charges stored in the charge pump capacitors, based on Figs. 2.43 and 2.44a, b. The total charge $Q_{\mathrm{DD}}(k,j)$ $(1 \leq k \leq N)$ consumed by the driver $I(k)$ driving the capacitor $C(k)$ during j equals the total charge transferred from the capacitor $C(k)$ to the next one $C(k+1)$ through the diode $D(k+1)$ during j, as illustrated in Fig. 2.43. Therefore, $Q_{\mathrm{DD}}(k,j)$ equals the total charge increase in the capacitors $C(k+1)$, $C(k+2)$, …, $C(N)$ and C_{LOAD} during j, where C_{LOAD} is the load capacitance of the charge pump circuit. Similarly, the total charge $Q_{\mathrm{DD}}(0,j)$ supplied by the input voltage V_{DD} at the left hand side of Fig. 2.43 equals the total charge increase in all capacitors including C_{LOAD}. Therefore, if $Q(i,j)$ and $Q_{\mathrm{LOAD}}(i)$ are the charges stored in the capacitors $C(i)$ $(1 \leq i \leq N)$ and C_{LOAD} at j, respectively, for $1 \leq k \leq N-1$.

$$Q_{DD}(k,j) = \sum_{i=k+1}^{N} [Q(i,j) - Q(i,0)] + [Q_{LOAD}(j) - Q_{LOAD}(0)] \tag{2.146}$$

and

$$Q_{DD}(N,j) = Q_{LOAD}(j) - Q_{LOAD}(0) \tag{2.147}$$

The total consumed charge $Q_{\mathrm{DD}}{}^{\mathrm{d}}(j)$ is the sum of all charges $Q_{\mathrm{DD}}(k,j)$ $1 \leq k \leq N$, so that

$$\begin{aligned} Q_{DD}{}^{d}(j) &= \sum_{k=0}^{N} Q_{DD}(k,j) \\ &= \sum_{k=1}^{N} k[Q(k,j) - Q(k,0)] + (N+1)[Q_{LOAD}(j) - Q_{LOAD}(0)] \end{aligned} \tag{2.148}$$

The following initial conditions can be assumed,

$$Q(2k,0) = 0 \tag{2.149}$$

$$Q(2k-1,0) = C(V_{DD} - V_T) \tag{2.150}$$

and

$$Q_{LOAD}(0) = C_{LOAD}(V_{DD} - V_T) \tag{2.151}$$

which satisfy (2.74a), (2.74b). Under the assumption that (2.74a), (2.74b) hold during boosting, (2.148) results in

$$Q_{DD}{}^{d}(j) = (N+1)C_{OUT}(V_{OUT}(j) - V_G) \tag{2.152}$$

$$C_{OUT} \equiv C_{LOAD} + C_{PMP} \tag{2.153}$$

$$C_{PMP} = A(N)C \tag{2.154}$$

where $A(N)$ is a function of N,

$$A(N) = \frac{4N^2 + 3N + 2}{12(N+1)} \tag{2.155}$$

$$A(N) = \frac{4N^2 - N - 3}{12N} \tag{2.156}$$

for even and odd N, respectively.

Another expression for $Q_{\mathrm{DD}}{}^{\mathrm{d}}(j)$ is derived below, based on Fig. 2.44c, d. Since the charge $q_{\mathrm{DD}}{}^{\mathrm{S}}$ supplied by the power supply in a cycle time in steady state is equal to the charge q transferred to the capacitor $C(1)$ through the diode $D(1)$ plus the charge Nq transferred from N capacitors $C(k)$ $(1 \leq k \leq N)$ to the next ones,

$$q_{DD}{}^{s} = (N+1)q \tag{2.157}$$

Like the above equation in steady state, the relation between the supplied charge $q_{\mathrm{DD}}{}^{\mathrm{d}}(j)$ and output charge increase $q_{\mathrm{OUT}}(j)$ in a cycle time from j to $j + 1$ during boosting

$$q_{DD}^{d}(j) = (N+1)q_{OUT}(j) \tag{2.158}$$

Under the assumption that (2.158) holds even during boosting, the total supplied charge during j, $Q_{\mathrm{DD}}{}^{\mathrm{d}}(j)$, is given by

$$\begin{aligned} Q_{DD}^{d}(j) &= \sum_{m=0}^{j} q_{DD}^{d}(m) \\ &= (N+1)\sum_{m=0}^{j} \frac{(1+\alpha_T)C}{N}\left[N\left(\frac{V_{DD}}{1+\alpha_T} - V_T\right) + V_{DD} - V_T - V_{OUT}(m)\right] \end{aligned} \tag{2.159}$$

where (2.73) is used. Combining (2.152) with (2.159),

$$\begin{aligned} &C_{OUT}(V_{OUT}(j) - V_{DD} - V_T) \\ &= \sum_{m=0}^{j} \frac{(1+\alpha_T)C}{N}\left[N\left(\frac{V_{DD}}{1+\alpha_T} - V_T\right) + V_{DD} - V_T - V_{OUT}(m)\right] \end{aligned} \tag{2.160}$$

Since (2.160) holds for arbitrary j, the recurrence formula for V_{OUT} holds as follow.

$$C_{OUT}(V_{OUT}(j+1) - V_{OUT}(j)) = \frac{(1+\alpha_T)C}{N}[N(\frac{V_{DD}}{1+\alpha_T} - V_T) + V_{DD} - V_T - V_{OUT}(j+1)] \tag{2.161}$$

Using the initial condition of $V_{\mathrm{OUT}}(0) = V_{\mathrm{DD}}$–$V_{\mathrm{T}}$ from(2.151), (2.161) is solved as

$$V_{OUT}(j) = N(\frac{V_{DD}}{1+\alpha_T} - V_T) + V_{DD} - V_T - N(\frac{V_{DD}}{1+\alpha_T} - V_T)\beta^j \tag{2.162}$$

$$\beta = \left(1 + \frac{(1+\alpha_T)C}{NC_{OUT}}\right)^{-1} \tag{2.163}$$

As a result, the rise time T_{R} that the output voltage $V_{\mathrm{OUT}}(j)$ rises from V_{DD}–V_{T} to V_{PP}, which satisfies $V_{\mathrm{OUT}}(\mathrm{T_R}) = V_{\mathrm{PP}}$, is solved as

$$T_R = \frac{\ln(1 - \frac{V_{PP} - V_{DD} + V_T}{N(\frac{V_{DD}}{1+\alpha_T} - V_T)})}{\ln \beta} \tag{2.164}$$

It is noted that this term should be multiplied by the cycle time of the driving clocks in practice, because (2.164) is expressed by the number of clock cycles. From (2.164), the mean current consumption $I_{\mathrm{DD}}{}^{\mathrm{d}}$ during T_{R} can be obtained as

$$I_{DD}^d \equiv Q_{DD}^d(T_R)/T_R = (N+1)C_{OUT}(V_{PP} - V_{DD} + V_T)/T_R \tag{2.165a}$$

C_{OUT} can be regarded as the total load capacitance during boosting. Therefore, it is considered that C_{PMP} represents the self-load capacitance of the charge pump itself. C_{PMP} is about one-third of the total charge pump capacitance, $NC/3$, and its error is less than 3% for even $N \geq 4$ and less than 7% for odd $N \geq 5$. When the parasitic capacitance at the bottom nodes of the pumping capacitors ($\alpha_{\mathrm{B}}C$) is taken into account for the current consumption, (2.165a) needs to be replaced with (2.165b).

$$I_{DD}^d = (N+1)C_{OUT}(V_{PP} - V_{DD} + V_T)/T_R + \alpha_B NCV_{DD}/T \tag{2.165b}$$

Although the output voltage $V_{\mathrm{OUT}}(j)$ is actually a staircase waveform, it can be regarded as a smooth function in case the rise time is sufficiently large compared with the cycle time of the driving clocks. In this case, (2.161) indicates the equivalent circuit of the charge pump as shown in Fig. 2.45. R_{PMP} represents the

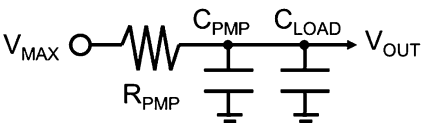


Fig. 2.45 Equivalent pump model

output series resistance of the charge pump and is given by $N/C(1 + \alpha_T)$ (as mentioned above, this is multiplied by the cycle time of the driving clocks and has the same dimension as resistor). V_{MAX} is the maximum output voltage of the charge pump, $N(V_{DD}/(1 + \alpha_T) - V_T) + V_{DD} - V_T$. C_{PMP} expressed by (2.154) indicates the self-load capacitance of the charge pump and is connected in parallel with the output load capacitance C_{LOAD}.

In order to compute the rise time and the current consumption accurately, only the cut-off condition of the transfer diodes and the charge conservation rule are used. A charge pump circuit with an even number of stages is considered. Since the charges $Q(2k-1,j)$ stored in the capacitors $C(2k-1)$ at time j are transferred to the next ones $C(2k)$ by time $j + 1/2$, the following relations hold if the charge conservation rule is assumed.

$$\begin{aligned} &Q(2k-1,j) + Q(2k,j) \\ &\quad = Q(2k-1,j+1/2) + Q(2k,j+1/2) \end{aligned} \tag{2.166}$$

Note that the charges stored in the parasitic capacitors are canceled out each other. From the condition that the diode $D(2k)$ is cut off at time $j + 1/2$,

$$\frac{Q(2k,j+1/2)}{C} - \frac{Q(2k-1,j+1/2)}{C} = \frac{V_{DD}}{1+\alpha_T} - V_T \tag{2.167}$$

Similarly, the charges $Q(2k,j + 1/2)$ stored in the capacitors $C(2k)$ at time $j + 1/2$ are transferred to the capacitors $C(2k + 1)$ by time $j + 1$.

$$\begin{aligned} &Q(2k,j+1) + Q(2k+1,j+1) \\ &\quad = Q(2k,j+1/2) + Q(2k+1,j+1/2) \end{aligned} \tag{2.168}$$

$$\frac{Q(2k+1,j+1)}{C} - \frac{Q(2k,j+1)}{C} = \frac{V_{DD}}{1+\alpha_T} - V_T \tag{2.169}$$

And also,

$$\begin{aligned} &Q_{LOAD}(j+1) + Q(N,j+1) \\ &\quad = Q_{LOAD}(j+1/2) + Q(N,j+1/2) \end{aligned} \tag{2.170}$$

$$\frac{Q_{LOAD}(j+1)}{C_{LOAD}} - \frac{Q(N,j+1)}{C} = \frac{V_{DD}}{1+\alpha_T} - V_T \tag{2.171}$$

Furthermore,

$$Q(1,j) = Q(1,j+1) = C(V_{DD} - V_T) \tag{2.172}$$

Eliminating the intermediate states at time j + 1/2, $Q(k,j + 1/2)$, and $Q_{\mathrm{LOAD}}(j + 1/2)$, from the above equations, for more than three stages,

$$\begin{aligned} Q(2,j+1) = \frac{1}{4}[&Q(2,j) + Q(3,j) + Q(4,j) \\ &- C(\frac{1-\alpha_T}{1+\alpha_T}V_{DD} - V_T)] \end{aligned} \tag{2.173}$$

$$\begin{aligned} Q(3,j+1) = \frac{1}{4}[&Q(2,j) + Q(3,j) + Q(4,j) \\ &+ C(\frac{3+\alpha_T}{1+\alpha_T}V_{DD} - 3V_T)] \end{aligned} \tag{2.174}$$

$$\begin{aligned} Q(2k,j+1) = \frac{1}{4}[&Q(2k-1,j) + Q(2k,j) + Q(2k+1,j) \\ &+ Q(2k+2,j) - 2C(\frac{V_{DD}}{1+\alpha_T} - V_T)] \end{aligned} \tag{2.175}$$

$$\begin{aligned} Q(2k+1,j+1) = \frac{1}{4}[&Q(2k-1,j) + Q(2k,j) + Q(2k+1,j) \\ &+ Q(2k+2,j) + 2C(\frac{V_{DD}}{1+\alpha_T} - V_T)] \end{aligned} \tag{2.176}$$

$$\begin{aligned} Q(N,j+1) = \frac{C}{2(C_{LOAD}+C)}[&Q(N-1,j) + Q(N,j) \\ &+ 2Q_{LOAD}(j) - (2C_{LOAD} - C)(\frac{V_{DD}}{1+\alpha_T} - V_T)] \end{aligned} \tag{2.177}$$

$$\begin{aligned} Q_{LOAD}(j+1) = \frac{C_{LOAD}}{2(C_{LOAD}+C)}[&Q(N-1,j) + Q(N,j) \\ &+ 2Q_{LOAD}(j) + 3C(\frac{V_{DD}}{1+\alpha_T} - V_T)] \end{aligned} \tag{2.178}$$

Equations (2.175) and (2.176) hold for more than five stages and $2 \le k \le N/2-1$. The stored charges $Q(k,j)$ $(1 \le k \le N)$ and $Q_{\mathrm{LOAD}}(j)$ can be iteratively computed using the initial condition of (2.149)–(2.151). The rise time can be obtained by the time that the output voltage $Q_{\mathrm{LOAD}}/C_{\mathrm{LOAD}}$ rises from the initial voltage V_{DD}–V_{T} to the final voltage V_{PP}. In case of a charge pump with one or two stages the equations like the above can be analytically solved for each $Q(k,j)$ and $Q_{\mathrm{LOAD}}(j)$, so that the rise time can be solved exactly. On the other hand, the solution

of the rise time for a charge pump with three stages can be obtained approximately rather than exactly because of the nonlinear equation for the rise time. This approximation introduces an error of only a few percent to the solution.

The charge supplied to the charge pump during one cycle from j to $j + 1$, $q_{DD}{}^{d}(j)$, is the sum of the charges supplied by the drivers $I(2k-1)$, which are the charge increases in the capacitors $C(2k)$, $(1 + \alpha_T)(Q(2k,j + 1/2)-Q(2k,j))$, the charges supplied by the drivers $I(2k)$ and $I(N)$, which are the charge increases in the capacitors $C(2k + 1)$ and C_{LOAD}, $(1 + \alpha_T)$ $(Q(2k + 1,j + 1)-Q(2k + 1,j + 1/2))$ and $Q_{LOAD}(j + 1)-Q_{LOAD}(j + 1/2)$, respectively, the charge supplied to the capacitor $C(1)$ by the input voltage, $(1 + \alpha_T)(Q(1,j + 1)-Q(1,j + 1/2))$, and the charge supplied to the parasitic capacitance at the bottom nodes of pumping capacitors, $N\alpha_B CV_{DD}$. By using (2.166)–(2.172),

$$\begin{aligned} q_{DD}^{d}(j) = {} & (1+\alpha_T)(2C(\frac{V_{DD}}{1+\alpha_T} - V_T) - Q(2,j)) \\ & - \sum_{k=2}^{N/2} (1+\alpha_T)(Q(2k,j) - CV_G) \\ & + \sum_{k=1}^{N/2-1} (1+\alpha_T)Q(2k+1,j+1) + (Q_{LOAD}(j+1) - Q_{LOAD}(j)) \\ & + \alpha_B NCV_{DD} \end{aligned} \tag{2.179}$$

Therefore, the total charge supplied to the charge pump during boosting, $Q_{DD}{}^{d}(T_R)$, can be iteratively computed by

$$Q_{DD}^{d}(T_R) = \sum_{j=0}^{T_R} q_{DD}^{d}(j) \tag{2.180}$$

As a result, the current consumption during boosting, $I_{DD}{}^{d}$, can be calculated by

$$I_{DD}^{d} = Q_{DD}^{d}(T_R)/T_R \tag{2.181}$$

The rise time and the current consumption computed have been in good agreement with the SPICE simulation results within 5%. Therefore, the verification of the analytical results is made by the comparison with the iteration method as below.

Figures 2.46, 2.47, 2.48, and 2.49, respectively, show the dependence of the rise time and the current consumption on the output load capacitance (Fig. 2.46), the number of stages (Fig. 2.47), the boosted voltage (Fig. 2.48), and the supply voltage (Fig. 2.49). As shown in Fig. 2.46a, the rise time increases proportionally to the output capacitance. The y-intersection in Fig. 2.46a indicates the rise time in case of no output load capacitance ($C_{LOAD} = 0$), and the self-load capacitance of the charge pump, which has been estimated by the analysis as about one-third of the total charge pump capacitance, is in good agreement with the iteration method. The current consumption during boosting has small dependence on the output load capacitance, as shown in Fig. 2.46b.

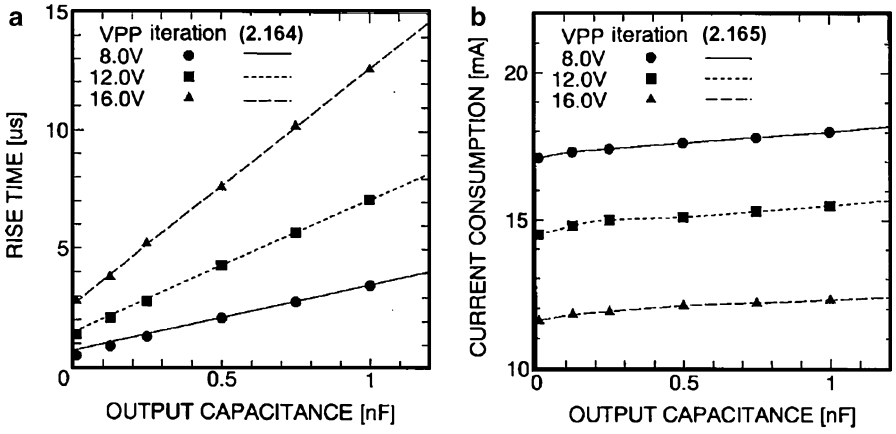


Fig. 2.46 Dependence of the rise time (**a**) and the current consumption (**b**) on the output load capacitance under the condition of $N = 8$, $V_{DD} = 3.0$ V, $V_T = 0.6$ V, $C = 100$ pF, $\alpha_T = \alpha_B = 0$, and the cycle time of driving clocks, $T = 100$ ns

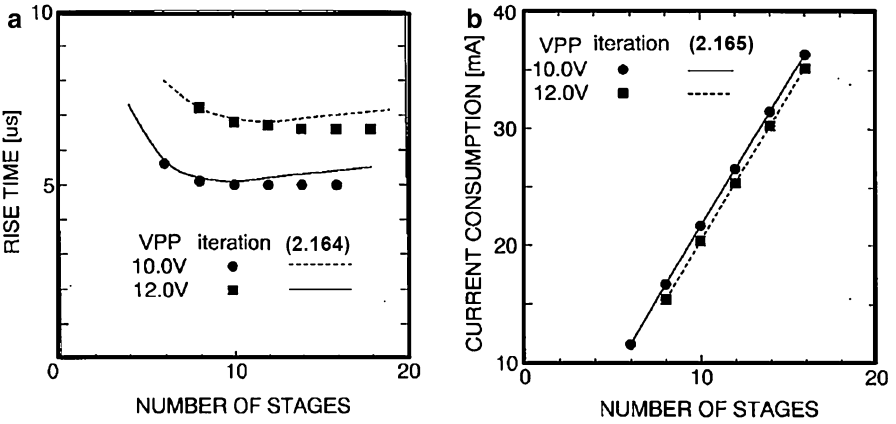


Fig. 2.47 Dependence of the rise time (**a**) and the current consumption (**b**) on the number of stages under the condition of $V_{DD} = 3.0$ V, $V_T = 0.6$ V, $C = 100$ pF, $\alpha_T = \alpha_B = 0$, $C_{LOAD} = 1$ nF and $T = 100$ ns

As shown in Fig. 2.47a, the rise time iteratively computed by (2.173)–(2.178) is constant for a large number of stages, while the rise time calculated by the analytical expression slightly increases with the number of stages because of the increasing self-load capacitance C_{PMP}. Figure 2.47a indicates the rise time doesn't depend on the excess number of stages in actual and the error of the analytical expression increases as the boosted voltage becomes much smaller than the maximum output voltage $N(V_{DD}/(1 + \alpha_T) - V_T) + V_{DD} - V_T$. This suggests the assumption that the charge pump is kept steady state even during boosting doesn't hold in such case.

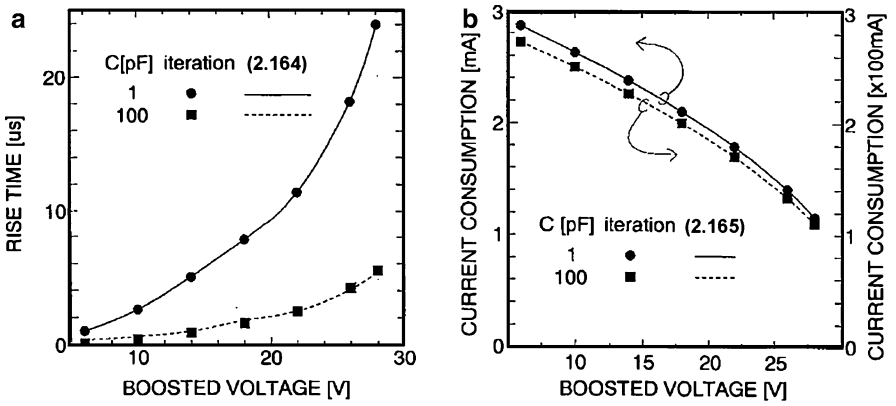


Fig. 2.48 Dependence of the rise time (**a**) and the current consumption (**b**) on the boosted voltage under the condition of $N = 8$, $V_{DD} = 4.0$ V, $V_T = 0.6$ V, $\alpha_T = \alpha_B = 0$, $C_{LOAD} = 10$ pF, and $T = 100$ ns

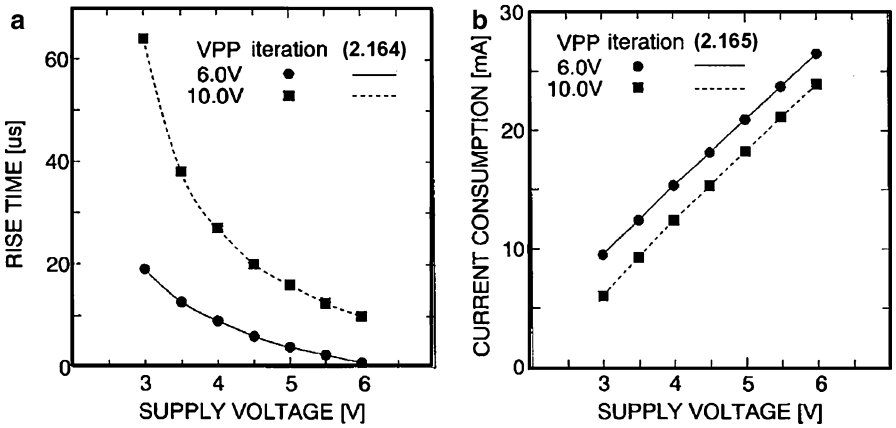


Fig. 2.49 Dependence of the rise time (**a**) and the current consumption (**b**) on the supply voltage under the condition of $N = 4$, $V_T = 0.6$ V, $\alpha_T = \alpha_B = 0$, C = 100 pF, $C_{LOAD} = 10$ nF, and $T = 100$ ns

The constant rise time and the total supplied charge proportional to the number of stages result in a current consumption that is increasing with the number of stages (Fig. 2.47b). The discrepancy between analytical and iterative results in Fig. 2.47a is attributed to the inaccuracy in the self-load capacitance C_{PMP}, while this discrepancy doesn't appear in Fig. 2.47b. This is because the discrepancy of the rise time T_R is canceled by that of the total supplied charge $Q_{DD}{}^{d}(T_R)$ in (2.165a), which is also increasing with the number of stages. The rise time and the current consumption show a large dependence on the boosted voltage (Fig. 2.48a, b) and the supply

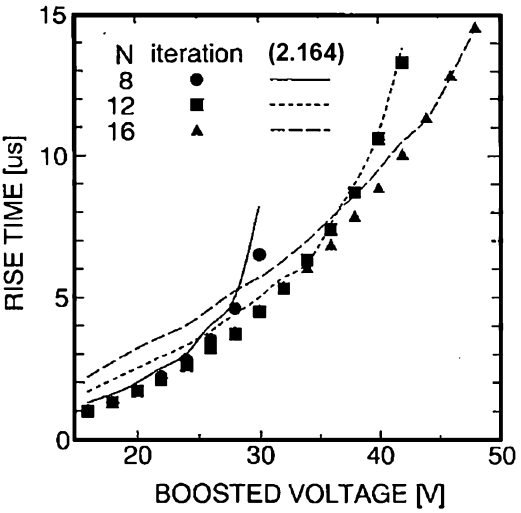


Fig. 2.50 Dependence of the rise time on the boosted voltage under the condition of $V_{DD} = 4.0$ V, $V_T = 0.6$ V, $\alpha_T = \alpha_B = 0$, $C_{LOAD} = 0$ pF, and $T = 100$ ns

voltage (Fig. 2.49a, b). Even in case that the charge pump capacitance is ten times larger than the output capacitance as shown in Fig. 2.48 (in case of $C = 100$ pF and $C_{LOAD} = 10$ pF), the analytical expression agrees with the iteration method.

Figure 2.50 shows the dependence of the rise time on the output voltage under the condition of no output load capacitance. In this case, the charge pump circuit has only a self-load capacitance. The analytical expression (2.164) in which the load capacitance C_{LOAD} is set to 0 agrees with the iteration method in case that the boosted voltage V_{PP} is not much smaller than the maximum output voltage of $N(V_{DD}/(1 + \alpha_T) - V_T) + V_{DD} - V_T$. However, in case of a small boosted voltage, the rise time given by the iteration method is independent of the number of stages. On the other hand, the rise time given by the analytical expression increases with the number of stages.

As mentioned above, the difference between the analytical expression and the iteration method increases as the boosted voltage becomes much smaller than the maximum output voltage, or in other words, the number of stages becomes excessively large compared with the number of stages necessary for the boosted voltage. In such case, the analytical results of (2.164) and (2.165a) cannot use. In a typical case that the boosted voltage is not smaller than one-fourth of the maximum output voltage, the analytical results agree with the simulation results computed by the iteration method within 10% for the rise time and within 2% for the current consumption.

(B) *Input and output power*

The power consumption P_{IN}, the output power P_{OUT}, and the power efficiency R_{PWR} during boosting are defined as

$$P_{IN} \equiv \sum_{j=0}^{T_R} q_{DD}^{d}(j) V_{DD} / T_R \tag{2.182}$$

$$P_{OUT} \equiv \sum_{j=0}^{T_R} q_{OUT}(j) V_{OUT}(j)/T_R \tag{2.183}$$

$$R_{PWR} \equiv P_{OUT}/P_{IN} \tag{2.184}$$

By using (2.162) for $V_{\mathrm{OUT}}(j)$, (2.73) for q_{OUT}, and (2.158) for $q_{\mathrm{DD}}{}^{\mathrm{d}}(j)$, these values can be calculated as

$$P_{IN} = (N+1) C_{OUT} (V_{PP} - V_G) V_{DD}/T_R \tag{2.185}$$

$$P_{OUT} = \frac{1}{2} C_{OUT} (V_{PP}^2 - V_G^2)/T_R \tag{2.186}$$

$$R_{PWR} = \frac{V_{PP} + V_G}{2(N+1)V_{DD}} \tag{2.187}$$

where V_{G} is $V_{\mathrm{DD}} - V_{\mathrm{T}}$.

(*C*) *Body effect of transfer transistors*

C_{PMP}, $V_{\mathrm{OUT}}(j)$, and T_{R} can be expanded in case where the body effect of transfer transistors should be taken into account in the cut-off condition. Following the approach that Witters et al. made, the body effect of transfer transistors is expressed by a parameter α as

$$V_S = \alpha (V_D - V_T) \tag{2.188}$$

where V_{S} is the source follower voltage, V_{D} is the voltage applied on the drain terminal which is shorted to the gate terminal, and V_{T} is the threshold voltage at no back bias. Thus, the following equations hold.

$$Q(1) = \alpha C V_G \tag{2.189}$$

$$Q(2k-1) = \sum_{i=1}^{2k-1} \alpha^i (C V_G - q_{OUT}) - \alpha^{2(k-1)} q_{OUT} \tag{2.190}$$

$$Q(2k) = \sum_{i=1}^{2k} \alpha^i (C V_G - \frac{q_{OUT}}{\alpha}) \tag{2.191}$$

$$Q(N) = C(\frac{V_{OUT}}{\alpha} - V_G) \tag{2.192}$$

Therefore, the output voltage–current characteristic with the body effect of transfer transistors is derived by

$$q_{OUT} = C(\sum_{i=1}^{N+1} \alpha^i V_G - V_{OUT}) / \sum_{i=1}^{N} \alpha^i \tag{2.193}$$

In this case, the recurrence formula for the output voltage holds as follow.

$$C_{OUT}(V_{OUT}(j+1) - V_{OUT}(j)) = C(\sum_{i=1}^{N+1} \alpha^i V_G - V_{OUT}(j+1))/\sum_{i=1}^{N} \alpha^i \tag{2.194}$$

where the self-load capacitance C_{PMP} included in the total load capacitance C_{OUT} is, respectively, expressed for even and odd N by

$$C_{PMP} = \frac{1}{(N+1)(1-\alpha^N)}\left[\frac{\alpha N^2 + (N+1)^2 - 1}{4\alpha} - \frac{1-(N+1)\alpha^N + N\alpha^{N+1}}{(1-\alpha)^2}\right]C \tag{2.195a}$$

$$C_{PMP} = \frac{1}{(N+1)(1-\alpha^N)}\left[\frac{\alpha(N+1)^2 + N^2 - 1}{4\alpha} - \frac{1-(N+1)\alpha^N + N\alpha^{N+1}}{(1-\alpha)^2}\right]C \tag{2.195b}$$

Using the initial condition of $V_{\mathrm{OUT}}(0) = V_{\mathrm{G}}$, (2.194) is solved as

$$V_{OUT}(j) = \sum_{i=1}^{N+1} \alpha^i V_G - \left(\sum_{i=1}^{N+1} \alpha^i - 1\right) V_G \beta^j \tag{2.196}$$

Therefore, the rise time that the output voltage rises from V_{G} to V_{PP} is

$$T_R = \ln[1 - (V_{PP} - V_G)/\left(\sum_{i=1}^{N+1} \alpha^i - 1\right) V_G]/\ln\beta \tag{2.197}$$

If the transistors do not suffer from the body effect, i.e., $\alpha = 1$, (2.196) and (2.197) reduce to (2.162) and (2.164) in case of $\alpha_{\mathrm{T}} = \alpha_{\mathrm{B}} = 0$, respectively.

2.3.2 Switch-Resistance-Aware Model

It has been assumed so far that all the diodes turn off at the end of a half period and all the amount of charge are transferred to the next capacitor. This subsection discusses more realistic case where this assumption is not valid to figure out an optimum clock frequency.

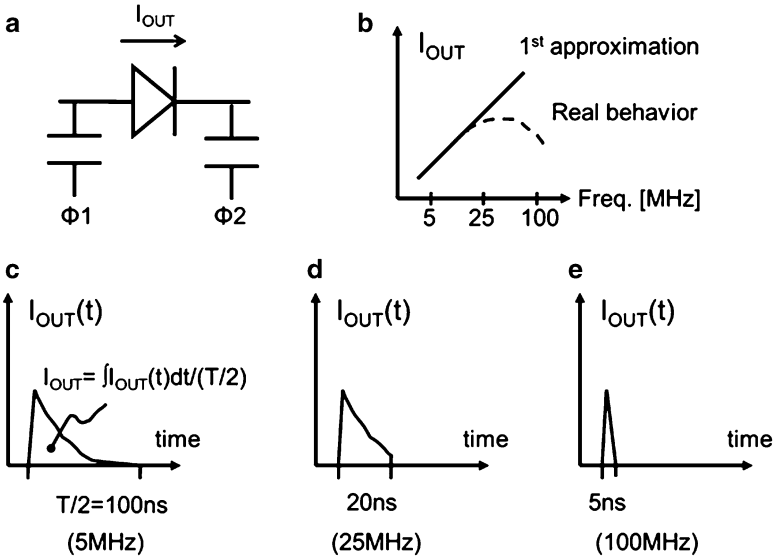


Fig. 2.51 Ideal and real frequency response to the output current

When the clock frequency is low enough, the output current is proportional to the clock frequency. Figure 2.51c indicates that the output charge per a half period is never affected when the clock frequency is slower than 5 MHz because there is no current at 100 ns. When the clock frequency increases to 25 MHz, the current at 20 ns is finite, as shown in Fig. 2.51d. One can guess that you may never gain the output current with a faster clock than 25 MHz. At 100 MHz, there may be little chance to transfer any charge, as shown in Fig. 2.51e. As a result, the frequency vs. output current curve could be a quadratic function in a real pump as shown in Fig. 2.51b.

Circuit designers have to reduce the circuit area as much as possible for a small die size. It is possible to cut the capacitor partially if one uses a fast clock. The question is how much capacitor area can cut to maintain the output current with a faster clock. Let C and C_T be the capacitance of the pump capacitor and parasitic capacitance, respectively. α_T is defined by C_T/C. Assume C is 1 pF and C_T is 0.1 pF for 50 ns clock, as shown in Fig. 2.52a. The effective voltage amplitude of the capacitor would be 10% lower than the supply voltage due to α_T of 10%. When one considers that the clock frequency increases twice, whereas the capacitor decreases half to reduce the total pump area with a faster clock and without changing the size of transfer gate, the effective clock amplitude could be reduced by 0.3 V due to an increased α_T of 20%, as shown in Fig. 2.52b. This means that this scenario is broken.

(*A*) *Switch-resistance-aware model*

Circuit analysis and modeling has been addressed in previous subsection in cases where the charges are fully transferred in every half period. To minimize the silicon

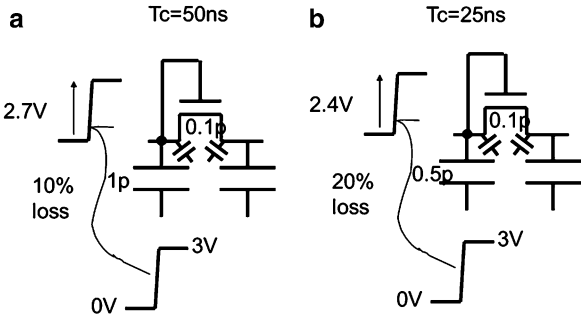


Fig. 2.52 Scalability in frequency

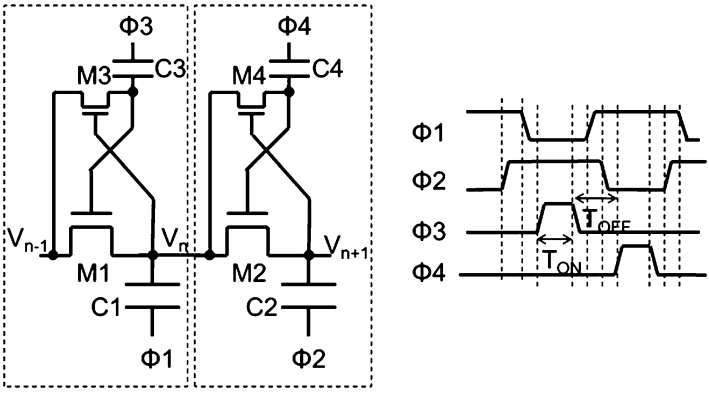


Fig. 2.53 Charge pump driven by four nonoverlapping phases

area for the pump that outputs a required current at a given output voltage, a faster clock frequency is preferred. However, the output current could decrease while the clock is running faster than a critical point at which the timing margin for four nonoverlapped clocks of the clocks is no longer negligible to the period while the switches turn on. This part discusses a switch-resistance-aware Dickson charge pump model. Equations between V_{OUT} and I_{OUT} and between the input current I_{IN} and I_{OUT} are determined in cases where the charges are not fully transferred due to the resistance of the switches (R). In addition, the impact of R on I_{OUT} is investigated and optimization of the clock frequency and the transistor size are presented to maximize I_{OUT} under a given circuit area in a given technology.

Figure 2.53 shows a Dickson charge pump circuit driven by four nonoverlapping phases whose operation is discussed in detail in Chap. 3. The capacitors C1,2 driven by Φ1,2 are main pumping capacitors, and C3,4 driven by Φ3,4 are auxiliary to eliminate the effect of the threshold voltage of the transfer gates. The transfer transistor M1(2) turns on in a triode region when Φ3(4) stays high.

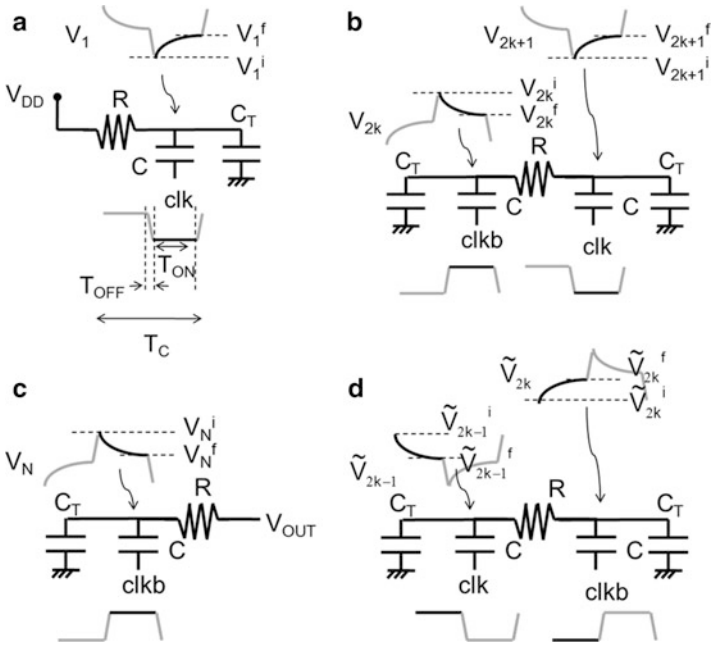


Fig. 2.54 Four representative combinations between next-neighbor capacitors. (**a**) First, (**b**) second to third, and (**c**) last stages, in the first half of period, followed by (**d**) first to second stages in the second half of the period

Figure 2.54a–d shows several combinations among the pump in steady state, where V_{DD} is the supply voltage, R the channel resistance of switches, C the main capacitor per stage, T_{ON} the period when the switch turns on, T_{OFF} the period when the switch turns off, T the period of the clock, $V_k = V_k(t)$ the voltage at node k ($1 \leqq k \leqq N$), N the number of stages, V_{ki} the initial voltage of V_k in the first half of the period, V_{kf} the final voltage of V_k in the first half of the period, $\tilde{V}_{ki(f)}$ the initial (final) voltage of V_k in the second half of the period, and V_{OUT} the output voltage. Strictly speaking, R has a voltage dependency per node, but it is assumed that the switch resistance can be treated as a constant averaged in T_{ON}. V_T is neglected below assuming V_T canceling techniques presented in the next chapter. From Fig. 2.54a–d, (2.198a)–(2.198d) hold during T_{ON}.

$$C(1+\alpha_T)\frac{dV_1}{dt} = \frac{V_{DD} - V_1}{R} \tag{2.198a}$$

$$C(1+\alpha_T)\frac{dV_{2k+1}}{dt} = -C(1+\alpha_T)\frac{dV_{2k}}{dt} = \frac{V_{2k} - V_{2k+1}}{R} \tag{2.198b}$$

$$C(1+\alpha_T)\frac{dV_{2k}}{dt} = -C(1+\alpha_T)\frac{dV_{2k-1}}{dt} = \frac{V_{2k-1} - V_{2k}}{R} \tag{2.198c}$$

$$C(1+\alpha_T)\frac{dV_N}{dt} = -\frac{V_N - V_{OUT}}{R} \tag{2.198d}$$

Where α_T is C_T/C which represents the gate overdrive loss. The initial and final voltages at each capacitor node in each half period are connected one another as follows.

$$\tilde{V}_{2k-1}{}^{f} - \frac{V_{DD}}{1+\alpha_T} = V_{2k-1}{}^{i} \tag{2.199a}$$

$$\tilde{V}_{2k-1}{}^{i} = V_{2k-1}{}^{f} + \frac{V_{DD}}{1+\alpha_T} \tag{2.199b}$$

$$\tilde{V}_{2k}{}^{f} + \frac{V_{DD}}{1+\alpha_T} = V_{2k}{}^{i} \tag{2.199c}$$

$$\tilde{V}_{2k}{}^{i} = V_{2k}{}^{f} - \frac{V_{DD}}{1+\alpha_T} \tag{2.199d}$$

Steady state indicates the following relations at each node, where q is the charge transferred to the output terminal in a period.

$$V_1{}^{i} = V_1{}^{f} - \frac{q}{C(1+\alpha_T)} \tag{2.200a}$$

$$V_{2k}{}^{i} = V_{2k}{}^{f} + \frac{q}{C(1+\alpha_T)} \tag{2.200b}$$

$$V_{2k+1}{}^{i} = V_{2k+1}{}^{f} - \frac{q}{C(1+\alpha_T)} \tag{2.200c}$$

$$V_N{}^{i} = V_N{}^{f} + \frac{q}{C(1+\alpha_T)} \tag{2.200d}$$

where N is assumed to be an even number here. However, the final results do not depend on whether N is even or odd.

From the conditions where $V_1(0) = V_{1i}$ and $V_1(T_{ON}) = V_{1f}$, (2.198a) results in (2.201).

$$V_1{}^{f} = V_{DD} - \zeta(V_{DD} - V_1{}^{i}) \tag{2.201}$$

where ζ is $\exp(-T_{ON}/RC(1+\alpha_T))$. Similarly, (2.198b) results in the following two relations.

$$V_{2k}{}^{f} = \frac{1}{2}(V_{2k}{}^{i} + V_{2k+1}{}^{i} + \zeta^2(V_{2k}{}^{i} - V_{2k+1}{}^{i})) \tag{2.202a}$$

$$V_{2k+1}{}^{f} = \frac{1}{2}(V_{2k}{}^{i} + V_{2k+1}{}^{i} - \zeta^2(V_{2k}{}^{i} - V_{2k+1}{}^{i})) \tag{2.202b}$$

Equations (2.198c) and (2.198d) also result in

$$\tilde{V}_{2k-1}{}^{f} = \frac{1}{2}(\tilde{V}_{2k-1}{}^{i} + \tilde{V}_{2k}{}^{i} + \zeta^2(\tilde{V}_{2k-1}{}^{i} - \tilde{V}_{2k}{}^{i})) \tag{2.203a}$$

$$\tilde{V}_{2k}{}^{f} = \frac{1}{2}(\tilde{V}_{2k-1}{}^{i} + \tilde{V}_{2k}{}^{i} - \zeta^2(\tilde{V}_{2k-1}{}^{i} - \tilde{V}_{2k}{}^{i})) \tag{2.203b}$$

and

$$V_{OUT} = \frac{V_N{}^{f} - \zeta V_N{}^{i}}{1-\zeta} \tag{2.204}$$

V_{1f} is calculated to be (2.205a) from (2.200a) and (2.201).

$$V_1{}^{f} = V_{DD} - \frac{q}{C(1+\alpha_T)}\frac{\zeta}{1-\zeta} \tag{2.205a}$$

From (2.199a), (2.199b), (2.199d), and (2.203a),

$$V_{2k-1}{}^{i} = \frac{1}{2}(V_{2k-1}{}^{f} + V_{2k}{}^{f} + \zeta^2(V_{2k-1}{}^{f} - V_{2k}{}^{f})) - \frac{V_{DD}}{1+\alpha_T}(1-\zeta^2) \tag{2.205b}$$

From (2.200c) and (2.205b),

$$V_{2k}{}^{f} = V_{2k-1}{}^{f} + A \tag{2.205c}$$

$$A = -\frac{2q}{C(1+\alpha_T)}\frac{1}{1-\zeta^2} + \frac{2V_{DD}}{1+\alpha_T} \tag{2.205d}$$

From (2.200b), (2.200c), and (2.202b),

$$V_{2k+1}{}^{f} = V_{2k}{}^{f} + B \tag{2.205e}$$

$$B = -\frac{2q}{C(1+\alpha_T)}\frac{\zeta^2}{1-\zeta^2} \tag{2.205f}$$

From (2.205c) and (2.205e),

$$\begin{aligned} V_2{}^f &= V_1{}^f + A \\ V_3{}^f &= V_2{}^f + B \\ V_4{}^f &= V_3{}^f + A \\ V_5{}^f &= V_4{}^f + B \\ &\vdots \\ +)V_N{}^f &= V_{N-1}{}^f + A \\ \hline V_N{}^f &= V_1{}^f + \frac{N}{2}A + (\frac{N}{2} - 1)B \end{aligned} \tag{2.205g}$$

From (2.205a), (2.205d), (2.205f), and (2.205g),

$$V_N{}^f = V_{DD}(1 + \frac{N}{1+\alpha_T}) - \frac{q}{C(1+\alpha_T)}(N\frac{1+\zeta^2}{1-\zeta^2} + \frac{\zeta}{1-\zeta^2}) \tag{2.206}$$

From (2.200d) and (2.204),

$$V_{OUT} = V_N{}^f - \frac{q}{C(1+\alpha_T)}\frac{\zeta}{1-\zeta} \tag{2.207}$$

From (2.206) and (2.207),

$$I_{OUT} \equiv \frac{q}{T} = \frac{V_{MAX} - V_{OUT}}{R_{PMP}} \tag{2.208}$$

where R_{PMP} and V_{MAX} are, respectively

$$R_{PMP} = \frac{T}{C(1+\alpha_T)}(N\frac{1+\zeta^2}{1-\zeta^2} + \frac{2\zeta}{1-\zeta^2}) \tag{2.209}$$

$$V_{MAX} = V_{DD}(1 + \frac{N}{1+\alpha_T}) \tag{2.210}$$

Using the relation of $T = 2(T_{\mathrm{ON}} + T_{\mathrm{OFF}})$, one can easily calculate I–V curves with T_{ON} and T_{OFF} instead of T and T_{ON}. Equation (2.210) is same as that of the original model which is given by (2.77) and $V_{\mathrm{T}} = 0$. (2.209) is reduced to the original model (2.78) in case where $T_{\mathrm{ON}}/RC(1 + \alpha_{\mathrm{T}})$ is much greater than 1 or ζ is much less than 1. According as $T_{\mathrm{ON}}/RC(1 + \alpha_{\mathrm{T}})$ decreases and becomes comparable to an order of 1, R_{PMP} increases, thereby I_{OUT} decreases. Since the input current is a sum of the output current multiplied by $(N + 1)$ and the charging current to another parasitic capacitor per stage at the bottom terminal of the capacitor (C_{B}), (2.89) holds.

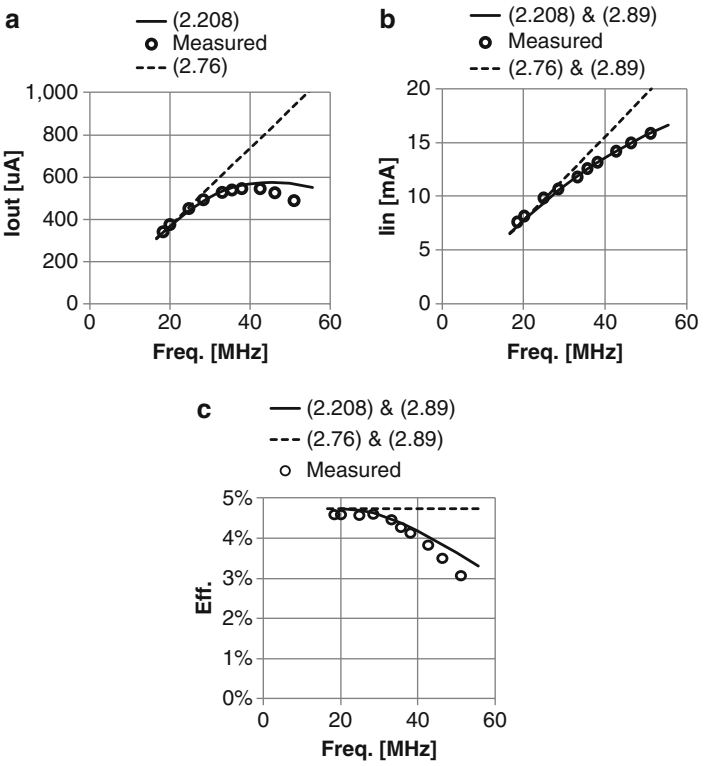


Fig. 2.55 Measured and calculated output (**a**) and input (**b**) current and efficiency (**c**) of the pump with the parameters shown in Table 2.5

Table 2.5 Design parameters used in Fig. 2.55

N	8	a.u.
C	4.0E−11	F
C_T	2.0E−12	F
C_B	1.2E−11	F
R	180	Ohm
V_{DD}	2.15	V
V_{OUT}	15	V
T_{OFF}	4.0E−09	s

Figure 2.55a, b, respectively, shows measured and modeled output and input current of the pump which has the design parameters shown in Table 2.5. The current consumption in an on-chip oscillator was subtracted from the measured input current for comparison with the models. Frequency dependencies of the input and output current of the model with (2.208), (2.209), and (2.210) are in good agreement with the measured results up to the peak frequency where the output current has the peak value. It can be considered that the effective channel resistance

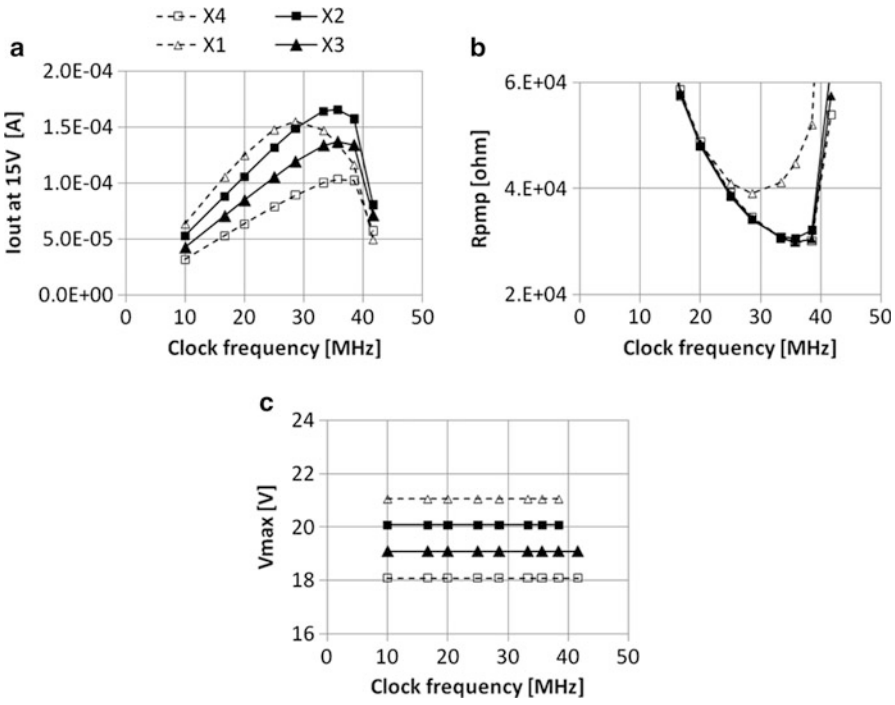


Fig. 2.56 Performance comparisons between the four design with different transistor sizes using the model with (2.209) and (2.210) and parameters in Tables 2.6 and 2.7

Table 2.6 Design parameters used in Fig. 2.56

N	10	a.u.
V_{DD}	2.0	V
T_{OFF}	1.0E−08	s

of switching transistors is no longer treated as a constant because the boosting capacitors such as C_3 and C_4 in Fig. 2.53 are not fully charged as the clock frequency increases. On the other hand, disagreement of the ideal model with (2.76), (2.77), and (2.78) with the measured currents starts at much lower clock frequency. Figure 2.55c shows the current efficiency. At a sacrifice of efficiency, the output current is maximized is about 40 MHz in this test case.

(*B*) *Optimum frequency*

The optimum operation to maximize the output current depends on the switch resistance. As the channel width of the switching transistors increases, the channel resistance R decreases. The optimum frequency can be shifted toward a faster side. With the faster clock, R_{PMP} could be reduced. However, as the transistor size is increased, the parasitic capacitance C_T is also increased. Thus, the effective voltage amplitude V_{MAX} is reduced. Therefore, given the ratio of R and C_T, one can

Table 2.7 Design parameters used in Fig. 2.56

	*X*1	*X*2	*X*3	*X*4
R [ohm]	500	250	167	125
C_T [pF]	0.5	1	1.5	2
C [pF]	10	9.4	8.8	8.2

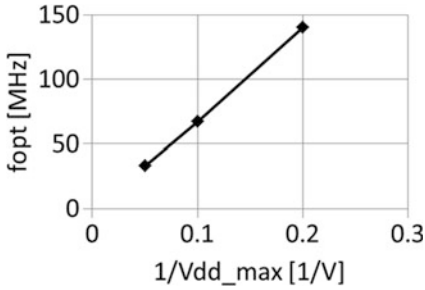


Fig. 2.57 Optimum frequency as a function of maximum drain-to-source voltages of transfer transistors

determine the optimum frequency to maximize the output current. For simplicity, it is assumed that C_T is inversely proportional to R as shown in Table 2.7. Under the condition that the total pump area is given, increase in the transistor area results in decrease in the main pumping capacitor C. Table 2.7 includes this consideration as well. Figure 2.56 compares four designs with different transistor sizes using the model with (2.209) and (2.210) and parameters in Table 2.7. As far as the clock frequency is low enough, R_{PMP} is same between the four cases, however V_{MAX} is the highest with the smallest transistors and the largest capacitors, resulting in the highest I_{OUT}. According as the frequency increases, I_{OUT} also increases until it reaches the peak. One can find the maximum I_{OUT} at the peak frequency per parameter set of R and C. Among the peak values, the optimum frequency, R, and C values are identified to have the highest output current. In Fig. 2.56, the parameter set as shown by $X2$ is the best one among the four cases to have the highest attainable output current and its optimum frequency is determined to be about 33 MHz.

The switch resistance depends on the transistors' dimensions such as channel length and gate oxide thickness which are determined by the maximum voltage applied to the transistors (V_{DD_MAX}). According as the pump output voltage required decreases, transistors used for the switches can be scaled. Figure 2.57 shows optimum frequency f_{OPT} as a function of $1/V_{DD\_MAX}$, where it is assumed that the gate oxide thickness, channel length, and channel width are scaled with a factor of $1/V_{DD\_MAX}$. Starting with f_{OPT} of 33 MHz at V_{DD_MAX} of 20 V for the case in Tables 2.6 and 2.7 and Fig. 2.56, two cases of V_{DD_MAX} of 10 and 5V are further analyzed with the method used for Fig. 2.56, which results in Fig. 2.57. Thus, the method described above can provide an initial guess for optimum frequency and switch size for detailed SPICE simulations.

In summary, steady state *I*–*V* characteristic is modeled for the pump operating with a fast frequency clock where the switch resistance cannot be negligible. Using

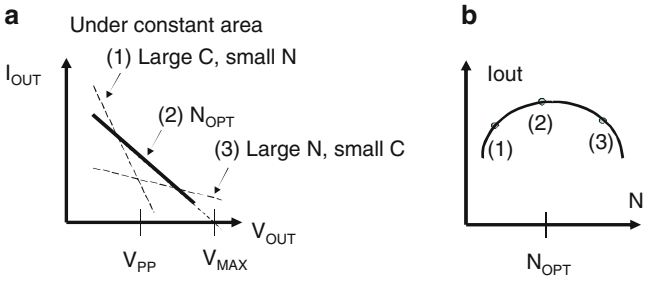


Fig. 2.58 Optimization for maximizing I_{OUT} under a given total pump capacitor area

the model, one can optimize the clock frequency where the output current is maximized. For practical design, current efficiency needs to be considered as well to make an optimization.

2.3.3 Optimization for Maximizing the Output Current

This subsection discusses optimization for maximizing the output current under a given circuit area. In order word, the optimization is equivalent to a minimum circuit area to output a given current. Because the output voltage is fixed, maximizing the output current is equivalent to maximizing the output power. Figure 2.58 shows three possible options in terms of N and C under the product NC given. Option 1 has a large pump capacitor per stage with a small number of stages, whereas option 3 has a small pump capacitor per stage with a large number of stages. Option 2 has moderate values for C and N. The question here is how to determine the option 2 whose I_{OUT} is the largest.

One can use Lagrange multiplier introducing functions f and h, and a parameter λ as follows.

$$f(C,N) \equiv \frac{C(1+\alpha_T)}{TN}\left[\left(\frac{N}{1+\alpha_T}+1\right)V_{DD} - (N+1)V_T - V_{PP}\right] - I_{PP} = 0 \quad (2.211)$$

$$h(C,N,\lambda) \equiv CN - \lambda f(C,N) \quad (2.212)$$

where (2.75) is used. One needs to minimize CN or h under the constraint where the pump has an output current of I_{PP} at an output voltage of V_{PP}. λ and I_{PP} are eliminated from (2.211) and $\partial h/\partial N = \partial h/\partial C = 0$, resulting in an optimum number of stages to minimize the area as (2.213).

$$N_{A\_OPT} = 2\frac{1 - v_T - \alpha_T v_T}{1 - v_T - 2\alpha_T v_T} N_{MIN} \quad (2.213)$$

$$N_{MIN} = \frac{(1+\alpha_T)(G_V - 1 + v_T)}{1 - v_T - \alpha_T v_T} \tag{2.214}$$

where G_V is a voltage gain of V_{PP}/V_{DD}, v_T is a relative threshold voltage of V_T/V_{DD}, and N_{MIN} is the number of stage to meet the condition of $I_{PP} = 0$. In case where V_T can be neglected, (2.213) and (2.214) are, respectively, reduced to

$$N_{A\_OPT} = 2N_{MIN} \tag{2.215}$$

$$N_{MIN} = (1+\alpha_T)(G_V - 1) \tag{2.216}$$

The condition of (2.215) and (2.216) is equivalent to (2.11).

2.3.4 Optimization for Minimizing the Rise Time

This subsection discusses another optimization for minimizing the rise time under a given circuit area. In other word, the optimization is equivalent to specifying the circuit area for a given rise time.

As discussed in subsection 2.3.1, the self-load capacitance C_{PMP} is almost constant for a given circuit area which is proportional to the total charge pump capacitance NC. The output series resistance of the charge pump, $R_{PMP} = N/C$, increases as the square of the number of stages N in case of a given circuit area because the charge pump capacitance C is inversely proportional to the number of stages. On the other hand, the maximum output voltage $V_{MAX} = (N + 1)V_G$ proportionally increases with the number of stages. As a result, there will be an optimum number of stages to minimize the rise time. If the self-load capacitance of the charge pump, C_{PMP}, is set to be just one-third of the total charge pump capacitance, $NC/3$, under the condition of a given circuit area,

$$T_R \propto x^2 \ln(1 - 1/x) \tag{2.217}$$

where x is N/N_{MIN}. N_{MIN} is $(V_{PP}/V_G - 1)$, which represents the minimum value of the number of stages necessary for a given parameter set of a supply voltage, threshold voltages of the transfer diodes and a boosted voltage. Thus, the optimum number of stages to minimize the rise time, N_{R_OPT}, is given by,

$$N_{R\_OPT} = 1.40N_{MIN} \tag{2.218}$$

Figure 2.59 shows the rise time and the current consumption under the condition of a constant circuit area. The rise time proportionally increases with the number of stages in case of a large number of stages. On the other hand, the rise time will be infinite in case of a number of stages as small as N_{MIN}. As a result, there is an

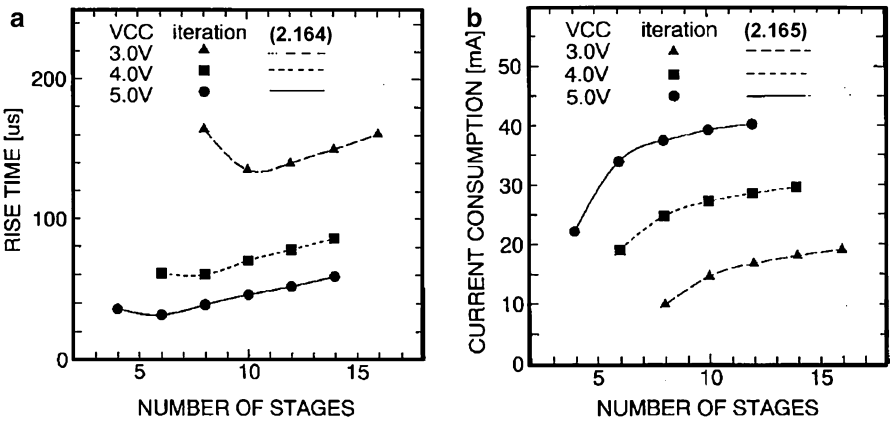


Fig. 2.59 Dependence of the (**a**) rise time and (**b**) current consumption on the number of stages under the condition of a constant circuit area $CN = 1$ nF and $V_{PP} = 20.0$ V, $V_T = 0.6$ V, $\alpha_T = \alpha_B = 0$, $T = 100$ ns, and $C_{LOAD} = 10$ nF

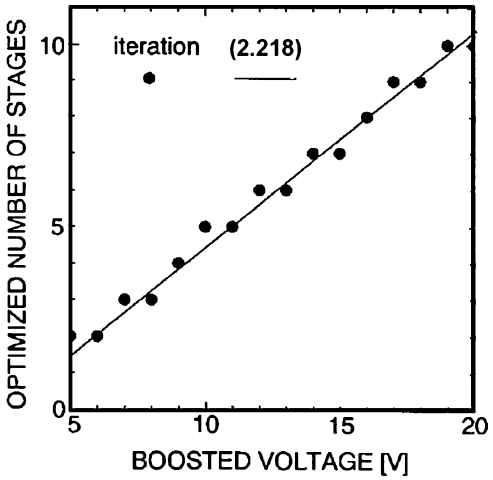


Fig. 2.60 Dependence of the optimum number of stages on the boosted voltage under the condition of a constant circuit area and $V_{DD} = 3.0$ V, $V_T = 0.6$ V, and $\alpha_T = \alpha_B = 0$

optimum number of stages in any case. The current consumption increases with the number of stages, so that a charge pump with an excessive number of stages increases not only the rise time but also the current consumption.

Figure 2.60 shows the dependence of the optimum number of stages on the boosted voltage. The analytical expression represented by the continuous line agrees with the iteration method represented by the discrete dots. The optimum number of stages proportionally increases with the boosted voltage, as represented

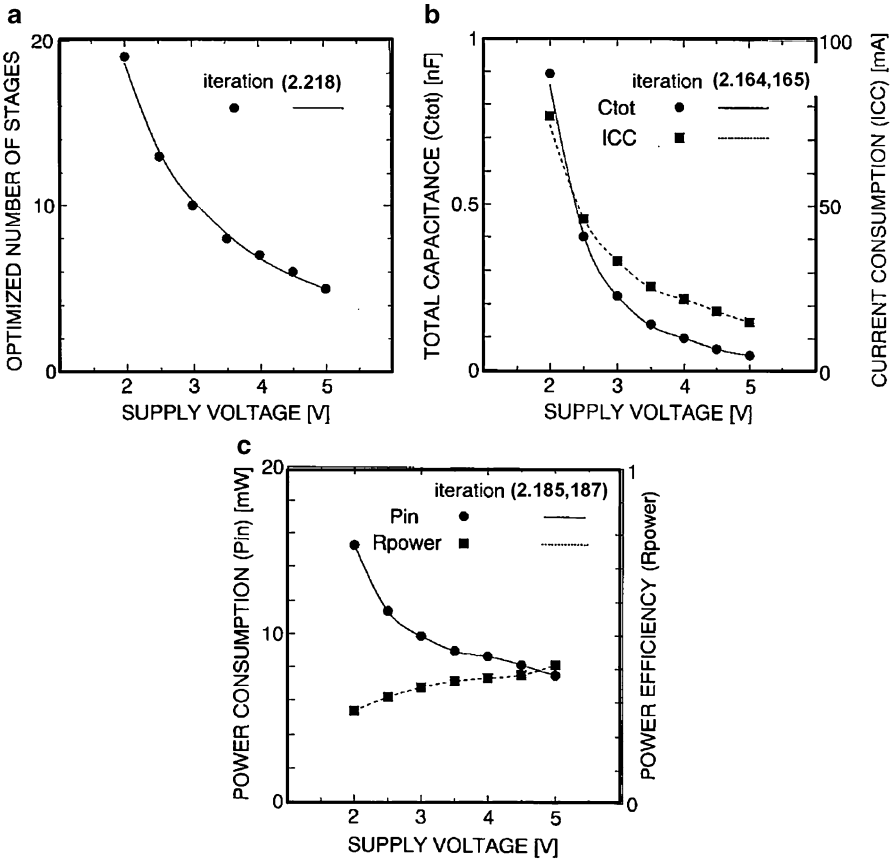


Fig. 2.61 Dependence of the optimum number of stages on the supply voltage under the condition of a constant circuit area and $V_{PP} = 20.0$ V, $V_T = 0.6$ V, $\alpha_T = \alpha_B = 0$, $T = 100$ ns (**a**). Dependence of the total capacitance, $C_{TOT} = CN$, and the current consumption on the supply voltage (**b**), and the power consumption and efficiency (**c**) under the condition that the rise time at any supply voltage is the constant value of 63 μs and $C_{OUT} = 10$ nF

by (2.218). Figure 2.61a shows dependence of the optimum number of stages on the supply voltage. The optimum number of stages increases as the supply voltage decreases. As mentioned above, an increase in the number of stages results in an increase in the current consumption. Figure 2.61b shows the total capacitance and the current consumption which are necessary for a constant rise time of 63 μs. The circuit area and the current consumption at a supply voltage of $2V$ are 17.9 and 5.1 times larger than those at $5V$, respectively. Figure 2.61c shows dependence of the power consumption and the power efficiency on the supply voltage under the same condition as Figure 2.61b. As a result, not only the circuit area but also the power consumption increase as the supply voltage decreases, unless the boosted voltage is scaled down according to the difference between the supply voltage and the threshold voltage of the transfer diode.

2.3.5 Optimization for Minimizing the Input Power

This subsection discusses an optimum design for minimizing the input power is considered under the condition that the pump outputs a given current I_{PP} at a given output voltage V_{PP}. Based on the V_{OUT}−I_{OUT} relation as shown in (2.75) and the I_{DD}−I_{OUT} relation as shown in (2.94), one can use Lagrange multiplier introducing functions f and g, and a parameter λ as follows.

$$f(C,N) \equiv \frac{C(1+\alpha_T)}{TN}\left[\left(\frac{N}{1+\alpha_T}+1\right)V_{DD} - (N+1)V_T - V_{PP}\right] - I_{PP} = 0 \tag{2.219a}$$

$$g(C,N,\lambda) \equiv I_{DD}(C,N) - \lambda f(C,N) \tag{2.219b}$$

λ and I_{PP} are eliminated from (2.219a) and $\partial g/\partial N = \partial g/\partial C = 0$, resulting in a quadratic equation in terms of N in (2.220).

$$\begin{aligned}&(1-(1+\alpha_T)v_T)(1-v_T+\alpha_B)N^2\\&\quad-2(G_V-1+v_T)(1+\alpha_T)(1+\alpha_B-v_T)N\\&\quad+(1+\alpha_T)(G_V-1+v_T)^2=0\end{aligned} \tag{2.220}$$

where G_V is a voltage gain of V_{PP}/V_{DD} and v_T is a relative threshold voltage of V_T/V_{DD}. (2.220) is accurately solved with no approximation, as shown below.

$$N_{P\_OPT} = N_{MIN}\left(1+\sqrt{\frac{\alpha_T+\alpha_B+\alpha_T\alpha_B}{(1+\alpha_T)(1+\alpha_B-v_T)}}\right) \tag{2.221a}$$

$$N_{MIN} = \frac{(1+\alpha_T)(G_V-1+v_T)}{1-v_T-\alpha_T v_T} \tag{2.221b}$$

2.3.6 Optimization with Area Power Balance

The optimum number of stages with different optimization methods such as minimizing the total pump capacitor area with (2.213), minimizing the rise time (2.218), and minimizing the power (2.221a) are summarized below. N_{OPT} is commonly expressed by

$$N_{OPT} = \varepsilon N_{MIN} \tag{2.222a}$$

where ε is a multiplication factor and is respectively given by

$$\varepsilon(A_{\_MIN}) = 2\frac{1 - v_T - \alpha_T v_T}{1 - v_T - 2\alpha_T v_T} \tag{2.222b}$$

$$\varepsilon(T_{RISE\_MIN}) = 1.40 \tag{2.222c}$$

$$\varepsilon(I_{DD\_MIN}) = 1 + \sqrt{\frac{\alpha_T + \alpha_B + \alpha_T\alpha_B}{(1 + \alpha_T)(1 + \alpha_B - v_T)}} \tag{2.222d}$$

To see how N affects the total capacitor area and input power, using the output voltage and current relation and the input current and output current relation, the following dimensionless scalable parameters, SP_{AREA} and SP_{PWR}, are calculated, respectively, where C_{TOT} is the total capacitance of the pump, i.e., NC.

$$\begin{aligned} SP_{AREA} &\equiv (1 - v_T - \alpha_T v_T)C_{TOT}V_{DD}/(TI_{PP}N_{MIN}) \\ &= \varepsilon^2/(\varepsilon - 1) \end{aligned} \tag{2.223a}$$

$$\begin{aligned} SP_{PWR} &\equiv (I_{DD}V_{DD})/(N_{MIN}I_{PP}V_{DD}) \\ &= (1 + a)\varepsilon + (1/N_{MIN} + a + b) + (a + b)/(\varepsilon - 1) \end{aligned} \tag{2.223b}$$

where a and b are the parameters defined by (2.223c) and (2.223d), respectively.

$$a = (\alpha_B + \alpha_T v_T)/(1 - v_T - \alpha_T v_T) \tag{2.223c}$$

$$b = \alpha_T/(1 + \alpha_T) \tag{2.223d}$$

SP_{AREA} shows how the total capacitor area varies when ε varies. For example, as shown in Fig. 2.62b, C_{TOT} is the minimum with ε of 2 and C_{TOT} in case of ε of 1.4 is larger by about 20% than that in case of ε of 2. Thus, SP_{AREA} can be considered as an indicator of the total capacitor area. Similarly, SP_{PWR} shows how the total input power $P_{IN} \equiv V_{DD}I_{DD}$ varies when ε varies. For example, as shown in Fig. 2.62c, P_{IN} is the minimum with ε of 1.5 in case of $N_{MIN} = 5$, $\alpha_T = 0.05$, $\alpha_B = 0.1$, $V_T = 0$ V, and P_{IN} in case of ε of 3 is larger by about 50% than that in case of ε of 1.5. Thus, SP_{PWR} can be considered as an indicator of the total input power.

Each of SP_{AREA} and SP_{PWR} as a function of ε has each own minimum point. SP_{AREA} doesn't depend on N_{MIN}, but SP_{PWR} does. The curve in Fig. 2.62b shows the relative total capacitor area given by (2.223a). The closed square point provides the minimum total capacitor area, whereas the open square point provides the minimum input power. The area overhead to minimize the input power is about 20% under the condition of $\alpha_T = 0.05$, $\alpha_B = 0.1$, and $V_T = 0$ V. Figure 2.62c shows the relative input power given by (2.223b) in cases of N_{MIN} of 5, 10, and 20. An optimum ε is 1.3–1.5 depending on N_{MIN}. At a multiplication factor ε of 2, as

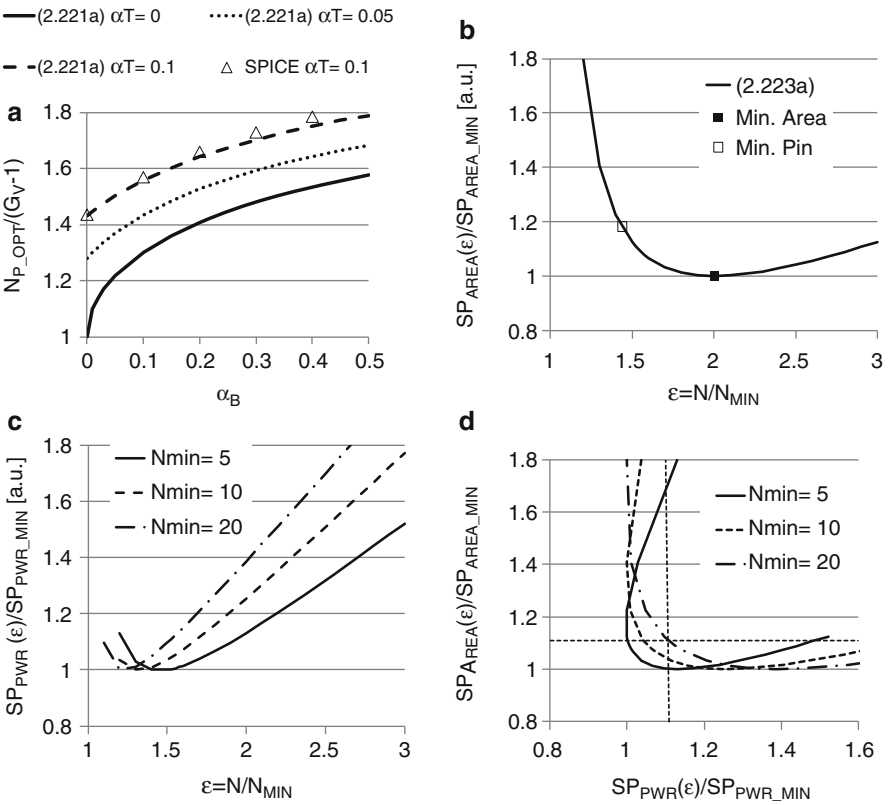


Fig. 2.62 α_B vs. N_{OPT} (**a**), ε vs. relative total area (**b**), ε vs. relative input power (**c**), relative input power vs. relative total area (**d**)

shown by (2.222b) with $v_T = 0$, where the total capacitor area is minimized, the overhead in the input power is about 10–40% depending on N_{MIN}. Therefore, an optimum ε would be selected between 1.4 and 2.0. Combining Fig. 2.62b with Fig. 2.62c, the relation of the input power and area is given by Fig. 2.62d, including a vertical and horizontal lines at $x = 1.11$ and $y = 1.11$. Figure 2.62d indicates there is a moderate design window to have both relative area and power smaller than 1.11 in the case of N_{MIN} of 20 or smaller. From Fig. 2.62b, ε of 1.5–2.7 can have the relative total area smaller than 1.11. From Fig. 2.62c, ε of 1.1–1.6 can have the relative input current smaller than 1.11 in the case of N_{MIN} of 10 or smaller. To take an operation margin into consideration, one can select a multiplication factor ε of 1.5–1.6 to provide a moderate optimum design with respect to the area and power, both of which are not higher by 11% than the minimum values.

Let us consider the back ground about a monotonic increase in N_{P_OPT} according to α_B as shown in Fig. 2.62a. Figure 2.62b shows the total capacitor area decreases

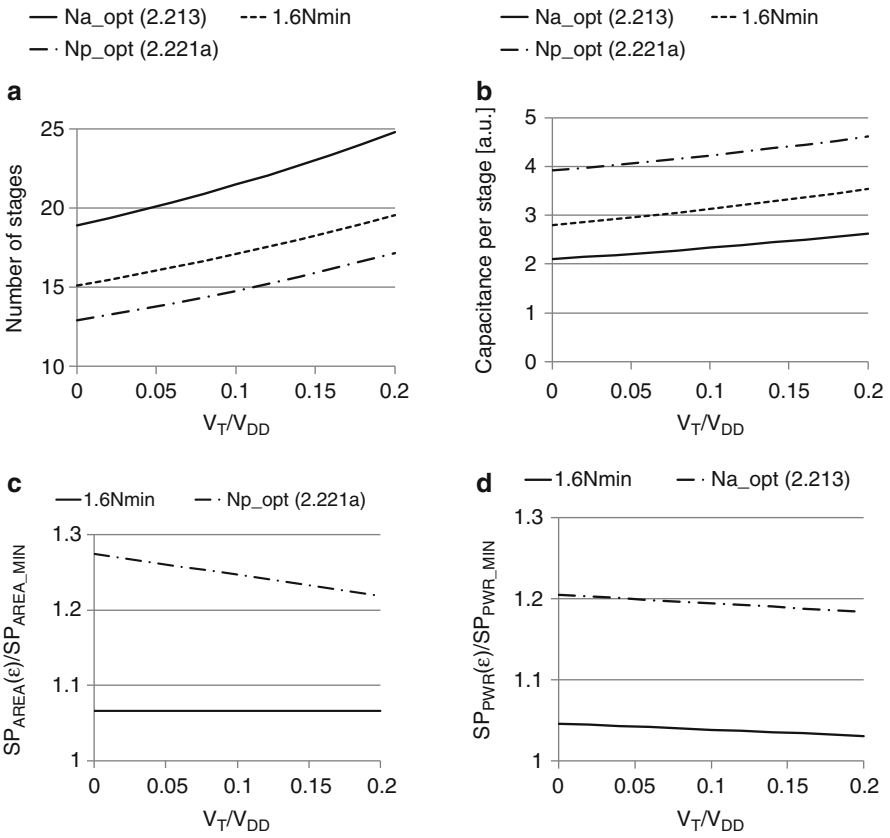


Fig. 2.63 Dependency of v_T on the number of stages (**a**) and capacitance per stage (**b**), dependency of v_T on the total area relative to the one designed by N_{A_OPT} (**c**) dependency of v_T on the input power relative to the one designed by N_{P_OPT} (**d**) under $\alpha_T = 0.05$, $\alpha_B = 0.1$

as ε increases as far as ε is smaller than 2. N and C are determined to meet (2.219a). Larger N requires smaller C. When α_B increases, the third term of (2.94) can be the main contributor. By selecting a larger N for a larger α_B, a decrease in the third term can be smaller than an increase in the first term. As a result, the total input power can be reduced with a larger N.

Figure 2.63a, b shows the impact of v_T on the number of stages given by (2.221a), (2.213), and $1.6N_{MIN}$ and on the capacitance per stage which is determined by (2.219a), respectively. All the cases increase a number of stages by about 30% and the capacitance per stage by about 20% for an increase in v_T by 0.2. To study the impact of v_T on the total capacitor area between three cases using (2.221a), (2.213) and $N = 1.6N_{MIN}$, the product NC is calculated per each v_T and is normalized by the case of using (2.213), resulting in Fig. 2.63c. The design with a number of stages calculated by $1.6N_{MIN}$ can have a moderate area overhead with an increase by about 7%. Two curves are much flatter than those of Fig. 2.63a, b.

This is because the ratios of N and C between the three cases are not strong functions of v_T. Similarly, dependencies of the input power on v_T are calculated per v_T and is normalized by the case of using (2.221a), resulting in Fig. 2.63d. The design with a number of stages calculated by $1.6N_{MIN}$ can have a moderate power overhead with an increase by about 5%.

2.3.7 Guideline for an Optimum Design

Switching transistors and capacitors are specified according to V_{PP} to have sufficient reliability in terms of time-dependent dielectric breakdown and channel hot carrier effect. The optimum operation frequency of the switching transistors fabricated in the technology given is determined by the design procedure discussed in subsection 2.3.2. The process parameters α_T, α_B, and V_T are also available once the silicon technology is selected. The optimum ratio of the capacitor area and the switching transistor area is identified using the design method in subsection 2.3.2. For the design parameters V_{DD}, V_{PP}, and I_{PP} given, one can calculate the optimum number of stages of $1.6N_{MIN}$ using (2.221b) and C using (2.219a). Because the discussions in this section are valid for any charge pumps as far as their characteristic is given by (2.219a), an optimum number of stages of εN_{MIN}, where ε is about 1.5–1.6 is applicable for the charge pumps using different switching circuit structures discussed in Chap. 3 as well as the original Dickson pump.

References

Greinacher and Cockcroft–Walton pump

Cockcroft JD, Walton ETS (1932) Experiments with high velocity positive ions.-(I) Further developments in the method of obtaining high velocity positive ions. Proc Royal Soc 136:619–30

R. Zhang, Z. Huang, Y. Inoue, "A Low Breakdown-voltage Charge Pump based on Cockcroft-Walton Structure," IEEE International Conference on ASIC Digest of Technical Papers, pp. 328–31, 2009.

Serial–Parallel pump

Brugler JS (1971) Theoretical performance of voltage multiplier circuits. IEEE J Solid-State Circuits 6(3):132–5

Mihara M, Terada Y, Yamada M (1995) Negative heap pump for low voltage operation flash memory, IEEE Symp VLSI Circuit 75–76

Linear Dickson pump

Falkner AH (1973) Generalised cockcroft-walton voltage multipliers. Elctronic Lett 9(25):585–6
Dickson JF (1976a) On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique. IEEE J Solid-State Circuits 11(3):374–378

Fibonacci pump

Ueno F, Inoue T, Oota I, Harada I (1991) Emergency power supply for small computer systems. IEEE Int Conf Circuits Systems, 1065–1068
Harada I, Ueno F, Inoue T, Oota I (1992a) Characteristics analysis of Fibonacci type SC transformer. IEICE Trans Fundamentals E75-A(6):655–62

2^N pump

Ueno F, Inoue T, Oota I (1986) Realization of a new switched-capacitor transformer with a step-up transformer ratio 2^N-1 using N capacitors. IEEE Int Conf Circuits and Systems, 805–808
Cernea RA (1995) Charge pump circuit with exponential multiplication. US Patent 5,436,587, 25 July 1995
Tsui CY, Shao H, Ki WH, Su F (2005) Ultra-low voltage power management and computation methodology for energy harvesting applications. IEEE Symp VLSI Circuit 316–319
Chang LK, Hu CH (2006) High efficiency MOS charge pumps based on Exponential-gain structure with pumping gain increase circuits. IEEE Trans Power Electronics 21(3):826–31

Circuit analysis

Dickson JF (1976b) On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique. IEEE J Solid-State Circuits 11(3):374–378
Witters JS, Groeseneken G, Maes HE (1989) Analysis and modeling of on-chip high-voltage generator circuits for use in EEPROM circuits. IEEE J Solid-State Circuits 24(5):1372–1380
Cataldo GD, Palumbo G (1996) Design of an Nth order Dickson voltage multiplier. IEEE Trans Circuits Systems I: Fundamental Theory and Applications 43(5):414–7
Tanzawa T, Tanaka T (1997a) A dynamic analysis of the Dickson charge pump circuit. IEEE J Solid-State Circuits 32(8):1231–1240
Tanzawa T, Atsumi S (1999a) Optimization of word-line booster circuits for low-voltage flash memories. IEEE J Solid-State Circuits 34(8):1091–1098
Palumbo G, Pappalardo D (2010) Charge pump circuits: an overview on design strategies and topologies. IEEE Circuits Systems Magazine 1:31–45
Makowski MS, Maksimovic D (1995) Performance limits of switched-capacitor DC-DC converters. IEEE Power Electronics Specialists Conf, 1215–1221
Gobbi L, Cabrini A, Torelli G (2007) A discussion on exponential-gain charge pump. 18th European conference on circuit theory and design, pp. 615–618, Aug. 2007
Starzyk JA, Jan YW, Qiu F (2001) A DC-DC charge pump design based on voltage doublers. IEEE Trans Circuits Systems I: Fundamental Theory and Applications 48(3):350–9

Gobbi L, Cabrini A, Torelli G (2006) Impact of parasitic elements on CMOS charge pumps: a numerical analysis. IEEE Int Conf Circuits Systems, 3125–3128
Seeman MD, Sanders SR (2008) Analysis and optimization of switched-capacitor DC-DC converters. IEEE Trans Power Electronics 23(2):841–51
Van Breussegem TM, Wens M, Geukens E, Geys D, Steyaert MSJ (2008) Area-driven optimisation of switched-capacitor DC/DC converters. Electronic Lett 44(25):1488–9
Tanzawa T (2011) A switch-resistance-aware dickson charge pump model for optimizing clock frequency. IEEE TCAS-II 58(6):336–40

Four terminal transfer matrix

Harada I, Ueno F, Inoue T, Oota I (1992b) Characteristics analysis of Fibonacci type SC transformer. IEICE Trans Fundamentals E75-A(6):655–62
Tanzawa T (2010) On two-phase switched-capacitor multipliers with minimum circuit area. IEEE TCAS-I 57(10):2602–8

Circuit optimization

Tanzawa T, Tanaka T (1997b) A dynamic analysis of the Dickson charge pump circuit. IEEE J Solid-State Circuits 32(8):1231–1240
Tanzawa T, Atsumi S (1999b) Optimization of word-line booster circuits for low-voltage flash memories. IEEE J Solid-State Circuits 34(8):1091–1098
Palumbo G, Pappalardo D, Gaibotti M (2002) Charge-pump circuits: power-consumption optimization. IEEE Trans Circuits Systems I: Fundamental Theory and Applications 49(11)

Chapter 3
Charge Pump State of the Art

Abstract This chapter discusses design techniques for implementing charge pumps in integrated circuits. Charge pumps are composed of transfer transistors and capacitors. Realistic design needs to take parasitic components such as threshold voltages of the transfer transistors and parasitic capacitance at each of both terminals into account. In order to decrease the pump area and to increase the current efficiency, some techniques such as threshold voltage canceling and faster clocking are presented. Since the supply current has a frequency component as high as the operating clock, noise reduction technique is another concern for pump design. In addition to design technique for individual pump, system level consideration is also important, since there are usually more than one charge pump in a chip. Area reduction can be also done for multiple charge pump system where all the pumps do not work at the same time. Wide supply voltage range operation and stand-by pump design are also discussed.

This chapter starts with switching diode design in Sect. 3.1 mainly focusing on how the threshold voltage of the transistor and its body effect can be mitigated to increase the output current under a given circuit area. Section 3.2 presents capacitor structures as well as design technique for reducing the top plate parasitic capacitance. Remaining sections discuss control methods for the pumps to operate stably even when the supply voltage can vary widely in Sect. 3.3, to reduce the total pump area in case where two pumps operate in different periods in Sect. 3.4, to decrease noise against the power supply and ripple in the output voltage in Sect. 3.5, and to have stability in the output voltage when stand-by and active pumps are used in Sect. 3.6.

T. Tanzawa, *On-chip High-Voltage Generator Design*, Analog Circuits and Signal Processing, DOI 10.1007/978-1-4614-3849-6_3,

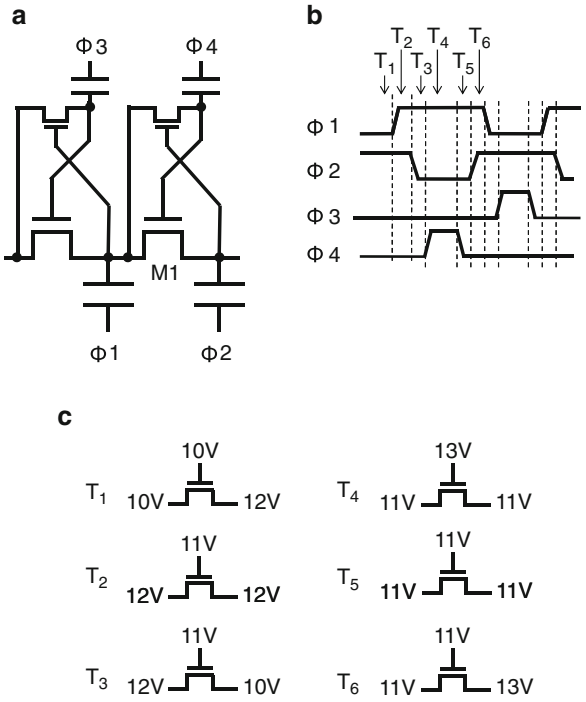


Fig. 3.1 V_T cancelation configuration (**a**) with four nonoverlapping phases (**b**) and the bias condition (**c**) (e.g., D'Arrigo et al. 1989; Umezawa et al. 1992)

3.1 Switching Diode Design

Dickson successfully generated a higher voltage on chip, but the supply voltage was much higher than the threshold voltage of the transfer transistor. According as the supply voltage of an LSI decreases for scaling the transistors and for reducing the power, the impact of the threshold voltage of the transfer transistors on the output current becomes significant. This section discusses various types of switching diode implementations to mitigate the impact of the threshold voltage and its body effect (Palumbo and Pappalardo 2010; Pan and Samaddar 2006; Kobayashi et al. 1995).

Figure 3.1a describes a positive voltage multiplier with V_T cancelation by means of four nonoverlapping phases. In order to increase the gate voltage of the transfer transistors, auxiliary capacitors driven by Φ3, 4 and transistors are added to the original devices. Figure 3.1c illustrates the bias condition of the transfer gate M1 at different timings where V_{DD} is 2 V and $V_T = 1$ V. The transfer gate M1 fully equalizes the two next neighbor capacitors at T_4 resulting in V_T cancelation whereas fully turns off at T_6. Because the timing margins between the phases are needed, the operation frequency is lower than the original Dickson pump with two phases. In case where the threshold voltages of the transfer transistors are the main contributors to limit the output current, the four nonoverlapping phases can improve the pump performance. On the other hand, if a pump running with a faster clock can output a higher current even with a finite threshold voltage, one should chose two phases.

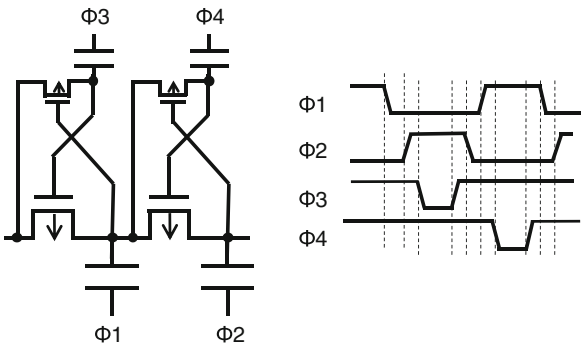


Fig. 3.2 V_T cancelation with four nonoverlapping phases for negative voltage generation (Kuriyama et al. 1990)

Which type is better depends on the threshold voltage, the supply voltage, and the frequency available in a given technology.

Figure 3.2 shows a complementary type of Fig. 3.1 outputting a negative voltage. The transfer transistors are pMOSFETs. Their N-well is connected to the supply voltage to prevent source and drain junctions from entering a forward bias regime in entire operation. If that happens, the amount of charges could flow into P-substrate, resulting in reduction in the output current.

In order to eliminate the body effect of the PMOS transfer transistors, the bodies per stage are connected to a separated N-well, as shown in Fig. 3.3a. Thus, V_{GS}, V_{DS}, and V_{BS} of every PMOS can be always limited within $2V_{DD}$. Because the N-well is connected to the capacitor node, there are several periods when the parasitic bipolar junction transistors could turn on. For instance, when Φ1 goes high while Φ2 stays low, the PN junction at the drain could enter in a forward bias regime until the potential of the effective base of the parasitic bipolar junction transistor (bjt) as shown in Fig. 3.3b is recovered after it receives a capacitive coupling of the junction capacitance. A part of the injected current flows into the P-type source and the rest flows into the P-substrate. Device design including the layout of the PMOSFETs and their N-well to reduce the P-substrate current as much as possible is a key to make the pump functional. As the supply voltage decreases, the current via the parasitic bjt decreases.

The body-effect-cancelation with P-well potential control can avoid the potential leakage current due to the parasitic bjt as shown in Fig. 3.4. Isolated P-well is connected to either one of the capacitor nodes with a lower potential. Because the transistors SW1, 2 are added, the parasitic capacitance at the upper terminal of the capacitors increases, resulting in lower boosting ratio. This is the trade-off for this method.

Figure 3.5 illustrates another topology using two phase clock to reduce the number of phases for faster clocking. To stabilize the potential of each isolated N-well, decoupling capacitors are added. The rise time can be affected, but the output current wouldn't once the pump enters a steady state because the charging current is not needed for the decoupling capacitors afterward. The transfer gates can have thin gate oxide because any voltage difference between the four terminals is smaller than

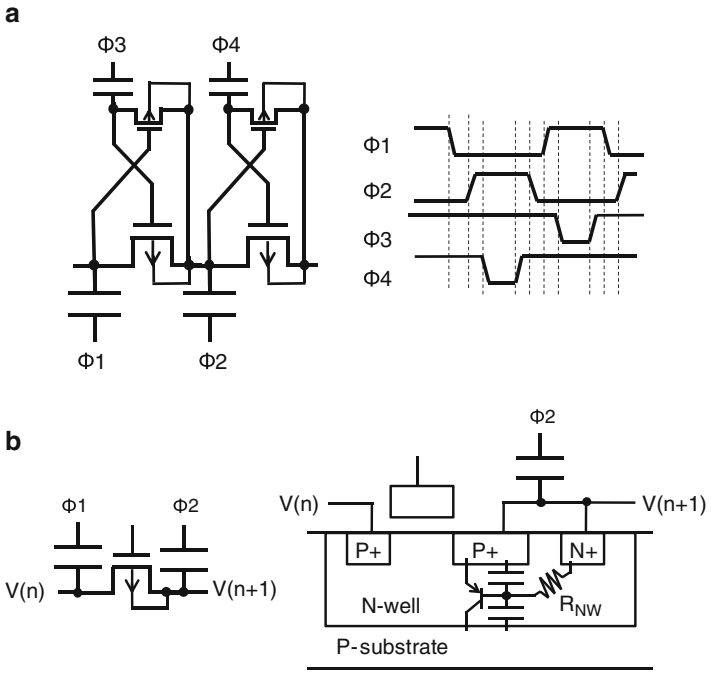


Fig. 3.3 (**a**) Body-effect-cancelation with divided N-well (Sawada et al. 1995). (**b**) Parasitic bipolar junction transistor formed in the divided N-well

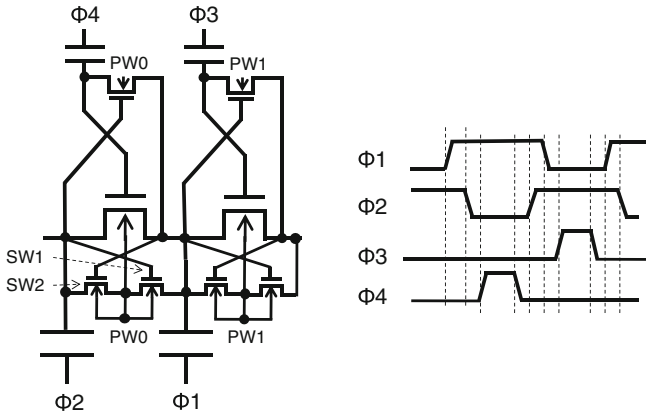


Fig. 3.4 Body-effect-cancelation with P-well potential control (Bloch et al. 1998)

$2V_{DD}$. On the other hand, the main, auxiliary, and decoupling capacitors have to have thick gate oxide because a voltage as high as V_{PP} is applied to them.

Another V_T cancelation technique was reported in Fig. 3.6. Besides a diode-connected transfer gate QN1, QN2 is connected in parallel, whose gate voltage is

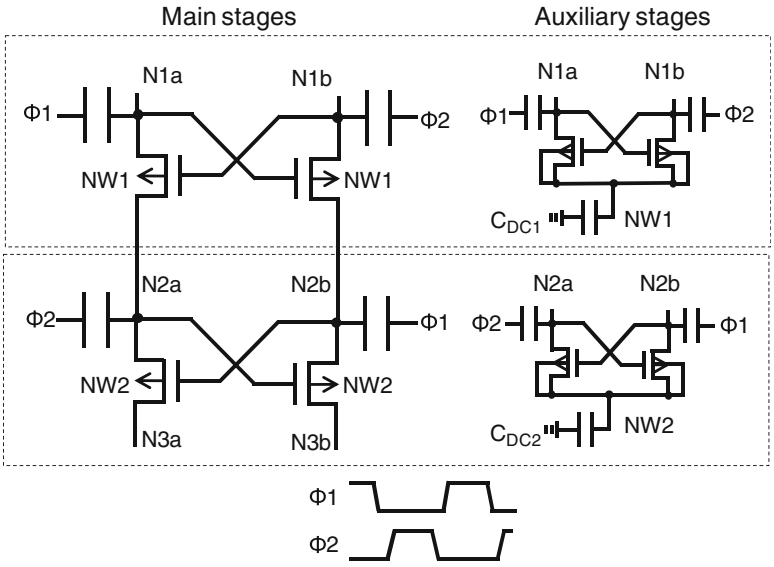


Fig. 3.5 Two phase body-effect-cancelation (Favrat et al. 1998)

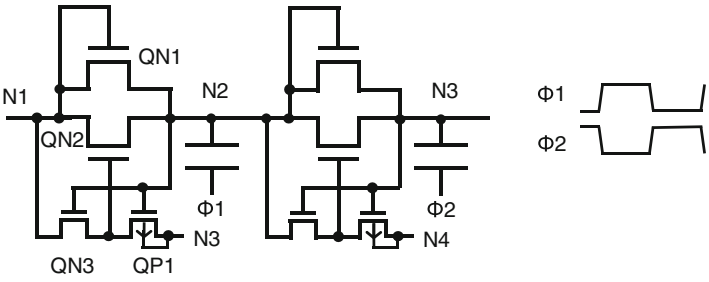


Fig. 3.6 Two phase CMOS V_T cancelation (Wu and Chang 1998)

borrowed by the capacitor node N3 of the next stage. Thus, the auxiliary capacitor is not needed. When $\Phi_1 = L$, $\Phi_2 = H$, QP1 turns on to pass the potential at N3 to the gate of QN2. When $\Phi_1 = H$, $\Phi_2 = L$, QN3 connects the potential at N1 to the gate of QN2, resulting in turning QN2 off. During the transition in Φ_1 and Φ_2, there can be the timing when both QN3 and QP1 turn on, resulting in a reverse current flowing from N3 to N1. When this happens, the output current thereby the power efficiency could be reduced. Therefore, the timing margin between Φ_1 and Φ_2 is a key design parameter.

Figure 3.7 illustrates a two phase clock pump with body effect cancelation. Because the transfer gate is connected as a diode, the threshold voltage at $V_{BS} = 0$ V, the so-called V_{T0}, does affect the transfer efficiency. However, when transistors

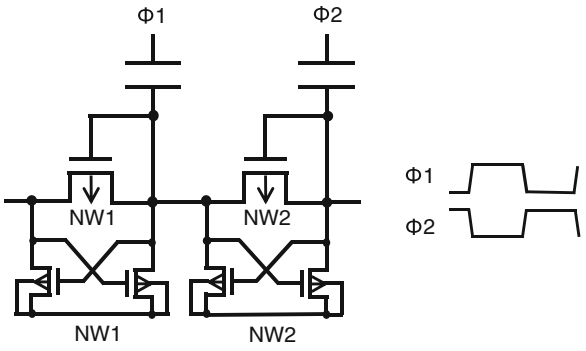


Fig. 3.7 Body-effect-cancelation with two phase clocks (Shin et al. 2000)

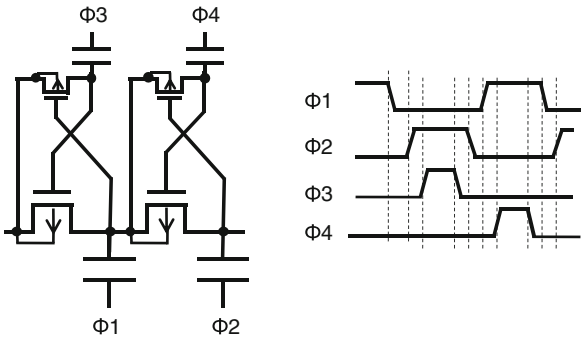


Fig. 3.8 Body-effect-cancelation with isolated P-well connected to the source of the transfer gates by stage (Javanifard et al. 2008)

with low V_{T0} is available, this topology may have a lower voltage difference between the gate and source, resulting in a lower stress on the transistor.

To reduce the parasitic capacitance in addition to body effect cancelation, the source terminals of the transfer gates are connected to the P-well by stage as proposed in Fig. 3.8. After Φ1 goes high and before Φ4 goes high, current flows through a parasitic diode composed of the P-well and the drain N+ junction. As far as the leakage current to P-substrate via the parasitic bjt is sufficiently small in comparison with the current from the pumping capacitor to the next one after Φ4 goes high, high-voltage generation is realized.

PN diode is not suffered from the body effect unlike transistor. Figure 3.9 realizes it using triple well structures. To prevent a parasitic bjt from flowing current to the substrate, N-well is connected with P-well. Sheet resistance of P-well is usually lower than that of N-well. In case where the difference is relatively large, the propagation delay from the N-well terminal to the center of N-well is longer than that from the P-well terminal to the center of P-well. If the potential difference reaches its built-in potential, the current can flow from P-well to P-substrate. Therefore, the diode size put in a single P-well needs to be small enough to be able to neglect such a difference in the propagation delay.

Using Flash memory structure, Poly-Si diode is fabricated as shown in Fig. 3.10. Second Poly-Si is used as hard mask to form P+ and N+ at source and drain.

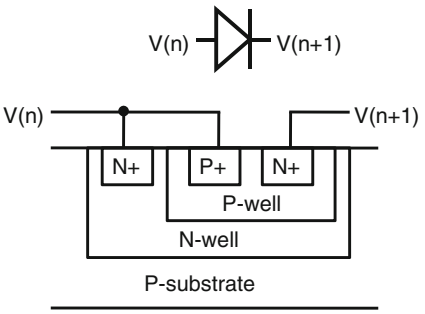


Fig. 3.9 Diode in the substrate (Storti et al. 1988)

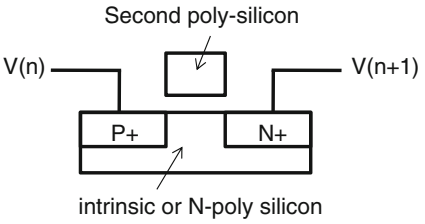


Fig. 3.10 Poly-Si diode (Mihara et al. 1999)

Because the source and drain have no connection with P-substrate, there is no parasitic bjt. On the other hand, thin-film poly-silicon devices have much lower mobility than bulk ones do. This is the trade-off for the Poly-Si diode.

3.2 Capacitor Design

This section discusses realization of capacitors. N-well capacitor may be able to be fabricated without any significant process cost, as shown in Fig. 3.11a. The N-well terminal can be driven by a clock whose voltage ranges from 0 V to V_{DD}. The gate oxide is usually thick enough to sustain a high-voltage generated by a pump. There are some parasitic capacitance components associated with the pump capacitor such as a junction capacitance between N-well and P-substrate and a fringe capacitance between the gate edge to the P-substrate. When the interconnection layers pass across the capacitor, it provides another parasitic capacitance to the gate node. When a charge pump is needed in a mixed signal LSI, metal-insulator-metal or polysilicon-insulator-polysilicon capacitor may be available, as shown in Fig. 3.11b. The maximum allowable voltage for the capacitor may restrict using the MIM/PIP capacitor. In advanced silicon technology, many interconnection layers are available. Figure 3.11c shows the cross sectional view of three interconnection layers. The top and bottom layers are routed in a direction parallel to the sheet and the middle one is routed in the direction perpendicular to the sheet. When the middle portion of the second layer is connected to a terminal of the capacitor and the surrounding portions are connected to another terminal, the capacitance between the two terminals is the sum of the four parasitic capacitors as shown in Fig. 3.11c.

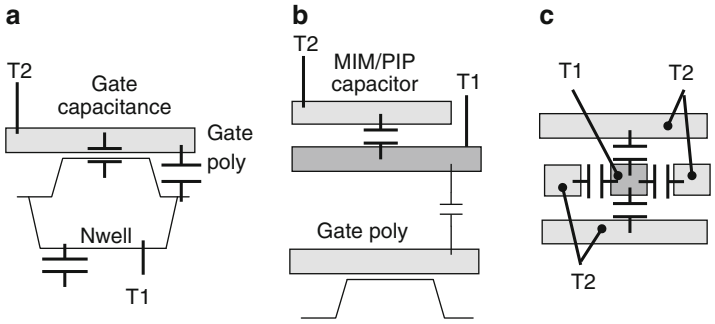


Fig. 3.11 Realization of capacitors

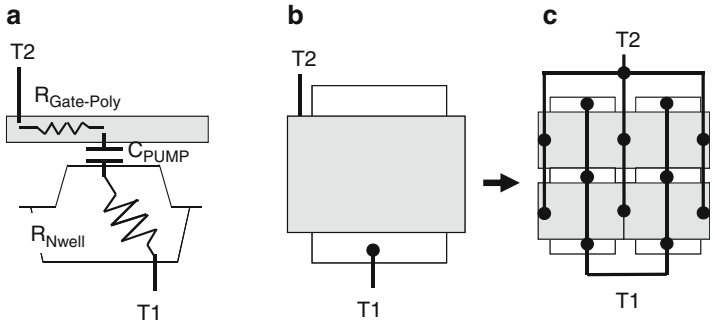


Fig. 3.12 Realization of capacitors with smaller parasitic RC time constant

One needs to make sure that the RC time constant associated with the capacitance of the pump capacitor and parasitic resistance such as gate resistance and well resistance is much smaller than the timing difference between different phases. When the single plate gate is large in terms of the RC time constant as shown in Fig. 3.12a, b, one may have to divide the capacitor into multiple small pieces to make RC time constant of each piece small enough, as shown in Fig. 3.12c.

Figure 3.13 illustrates two different routing to the two terminals of N-well capacitors. The gate is connected with a wide M1 layer in Fig. 3.13a whereas with a narrow M1 layer and another M1 layer over the gate is connected with the terminal T_1 which is connected with N-well in Fig. 3.13b. Table 3.1 compares each capacitance component of the pump capacitor C_{CP}, the parasitic capacitance at the top plate C_T, and the parasitic capacitance at the bottom plate C_B. The routing in Fig. 3.13b increases C_{CP} by C_2 and decreases C_T by C_3 at a sacrifice of increased C_B by C_3, resulting in a smaller ratio of C_T to C_{CP}, i.e., α_T, than the routing in Fig. 3.13a. This increases the effective clock amplitude and thereby the output

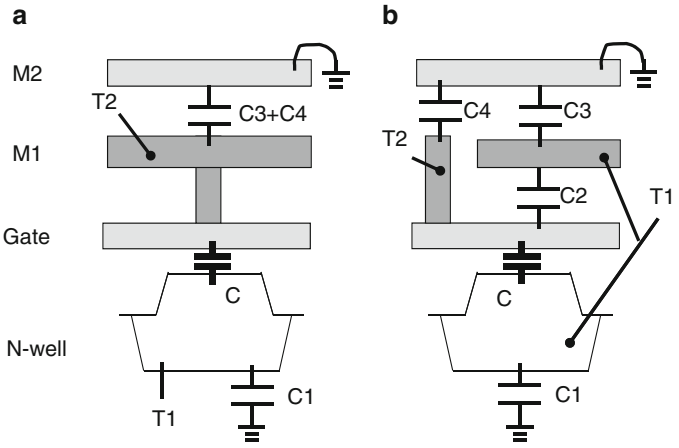


Fig. 3.13 Interconnections to pump capacitors

Table 3.1 Comparison of each capacitance of the pump capacitors of Fig. 3.13

	(a)	(b)
C_{CP}	C	$C + C_2$
C_T	$C_3 + C_4$	C_4
C_B	C_1	$C_1 + C_3$
α_T	$(C_3 + C_4)/C$	$C_4/(C + C_2)$

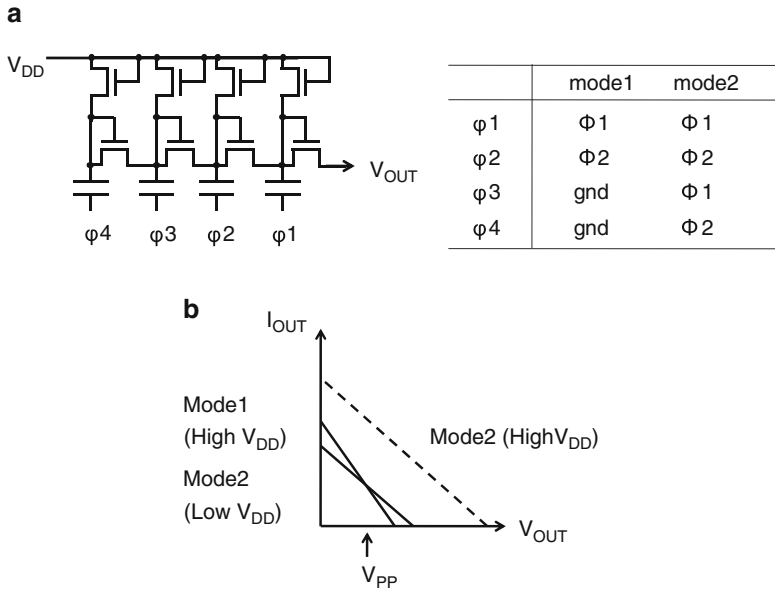
current under the same capacitor area. Because of increased C_B, the power efficiency is equivalent to the first order.

3.3 Wide V_{DD} Range Operation Design

This section investigates the impact of variation in V_{DD} on I_{OUT} and I_{DD} for applications requiring a wide V_{DD} operation. The design equations for I_{OUT} and I_{DD} are given by (2.87) and (2.89), respectively. One can extract the derivatives as follows.

$$\frac{dI_{PP}}{dV_{DD}} = \frac{C}{T}\left(1 + \frac{1+\alpha_T}{N}\right) \rightarrow \frac{C}{T} \tag{3.1}$$

$$\frac{dI_{DD}}{dV_{DD}} = \frac{C(N+1)}{T}\left(1 + \frac{1+\alpha_T}{N}\right) + \frac{NC_B - C_T}{T} \rightarrow \frac{N(C+C_B)}{T} \tag{3.2}$$



	mode1	mode2
φ1	Φ1	Φ1
φ2	Φ2	Φ2
φ3	gnd	Φ1
φ4	gnd	Φ2

Fig. 3.14 (**a**) Low noise pump design for wide V_{DD} operation with variable number of stages (Gerber et al. 1981). (**b**) Low noise pump design for wide V_{DD} operation

The arrows indicate what values are approached to when N becomes large. The dependence of V_{DD} on I_{PP} is not a strong function of N, but the smaller N the larger effect on I_{PP}. The dependence of V_{DD} on I_{DD} is a function of N^1.

Figure 3.14 shows a charge pump with two operational modes in which the number of stages is valuable. Only the last two stages operate in mode 1, whereas all the four stages do in mode 2. Figure 3.14b compares *I–V* curves in case of mode 1 at a high V_{DD}, mode 2 at a high V_{DD}, and mode 1 at a low V_{DD}. Two *I–V* curves are crossed at V_{OUT} around V_{PP}. When the number of stages is reduced as V_{DD} becomes higher than a critical voltage, the variation in I_{OUT} across the V_{DD} operating range can be significantly reduced. Furthermore, in case where the pump is required to output different currents ($I_{OUT1,2}$) at different voltages ($V_{OUT1,2}$) in different period of time, this control method can lower power consumption at $V_{OUT,1}$ ($<V_{OUT,2}$) because of smaller number of stages.

3.4 Area Efficient Multiple Pump System Design

This section discusses area efficient system design in case where all the multiple charge pumps don't operate simultaneously.

A simple method for generating two different voltages is having two different charge pumps. However, if they are not required to generate at the same time, or in

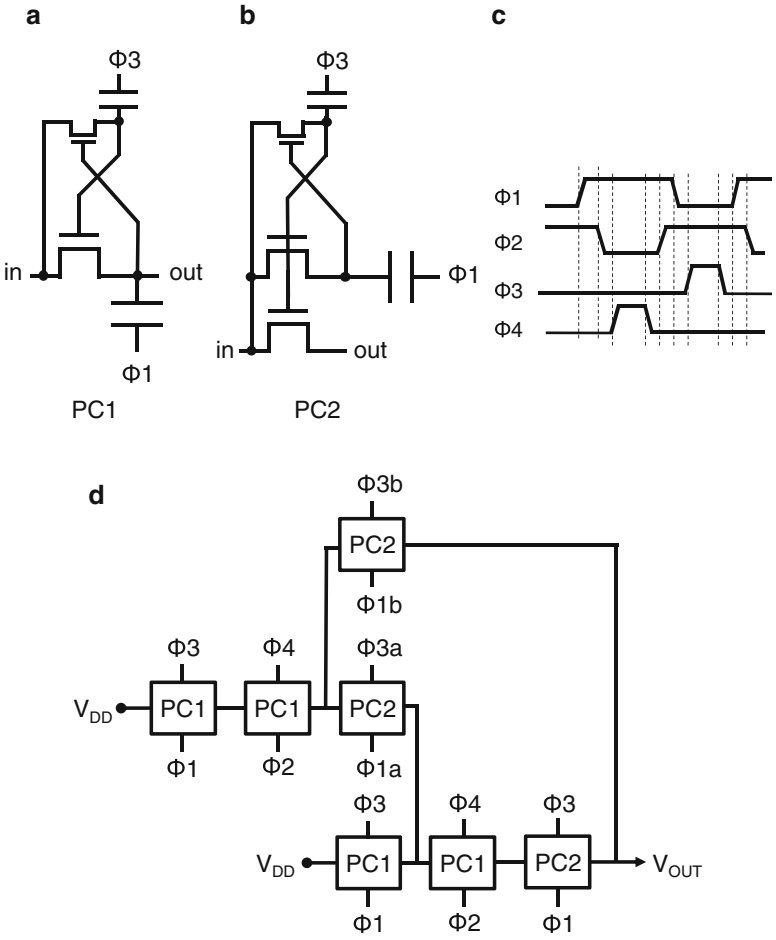


Fig. 3.15 Pump with variable number of stages and variable effective capacitance per stage (Tanzawa et al. 1997)

other word, if different high voltages are required in different periods, another method with a single charge pump having additional switches is possible as shown in Fig. 3.15. Figure 3.15a illustrates a unit pump stage cell. The switching circuit shown in Fig. 3.15b is composed of a transfer transistor and a boosting circuit with the same configuration as the unit pump cell. Because the switching circuit doesn't need to transfer large amount of charges, the capacitors used in the switching circuit can be small. Thus, the area for the switching circuit is much smaller than the unit pump cell.

Table 3.2 shows how the additional clocks are given by mode and how the pump is reconfigured. In mode 1, the upper two PC1 stages in Fig. 3.15 are connected with the output terminal in parallel to the lower two PC1 stages. Thus, the pump has a

Table 3.2 Clocks for reconfiguring the pump shown in Fig. 3.15

	Mode 1	Mode 2
Φ1a	*L*	Φ1
Φ3a	*L*	Φ3
Φ1b	Φ1	*L*
Φ3b	Φ3	*L*
# Stages	2	4
# Arrays	2	1
R_{PMP}	T/C	$4T/C$
V_{MAX}	$3V_{DD}$	$5V_{DD}$
I_{MAX}	$3CV_{DD}/T$	$1.25CV_{DD}/T$

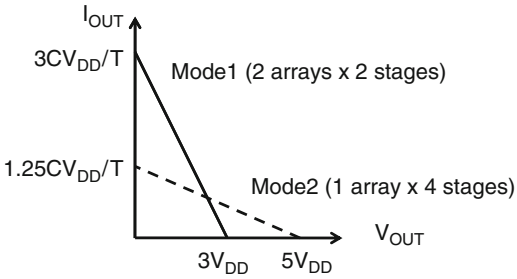


Fig. 3.16 *I–V*s in two modes of the pump of Fig. 3.15

configuration of two arrays of two stages. The output impedance R_{PMP} and the maximum attainable output V_{MAX} are respectively given by (2.78) and (2.77). The pump in mode 1 has R_{PMP} of T/C and V_{MAX} of $3V_{DD}$. I_{MAX} is defined by V_{MAX}/R_{PMP}. On the other hand, in mode 2, the upper two PC1 stages are connected with the lower two PC1 stages. Thus, the pump has a configuration of one array of four stages. The pump in mode 2 has R_{PMP} of $4T/C$ and V_{MAX} of $5V_{DD}$.

Figure 3.16 compares *I–V* curves between mode 1 and 2. If V_{PP} is set at $V_{MAX}/2$, which maximize the output power as shown in (2.11), both in mode 1 and 2, the ratio of I_{PP} of mode 1 to that of mode 2 is equal to 3/1.25. When the output current is not required to be so high, one can simply disable the upper two stages instead of enabling them. The ratio is reduced to 1.5/1.25, but it is still higher than 1. This means that this configuration is also possible when the requirement for the output current in mode 1 is not being smaller than the output current in mode 2.

3.5 Noise and Ripple Reduction Design

The pump output current I_{OUT} has a large ripple as shown in Fig. 3.17, resulting in a large ripple in the output voltage V_{OUT} and in the supply current I_{DD}. This section discusses design techniques to reduce the ripple. One approach is adding a decoupling capacitor C_{DC} to the output terminal. When the ripple in V_{OUT} is required to be ΔV_{PP}, the capacitance required for the decoupling capacitor should be

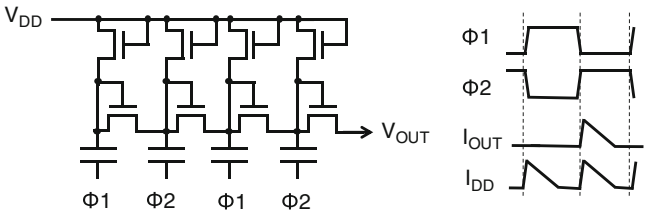


Fig. 3.17 Current profile along with pump operation

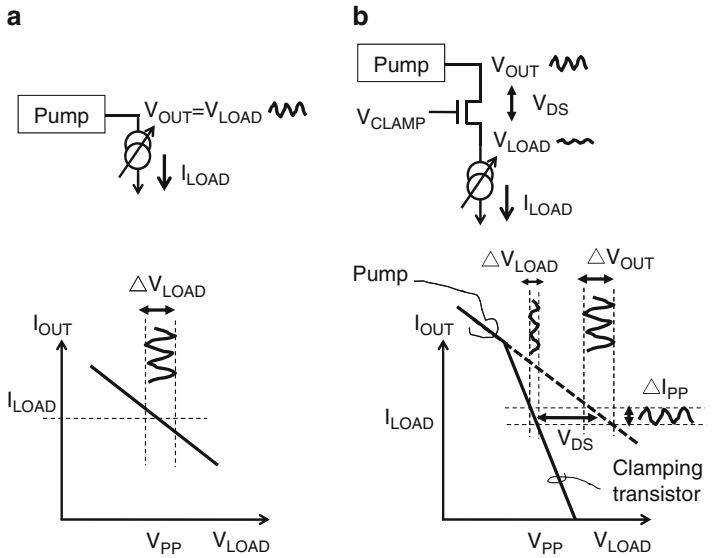


Fig. 3.18 Reduction method in the ripple in V_{LOAD}

$$C_{DC} > I_{DD} T / \Delta V_{PP} \tag{3.3}$$

The decoupling capacitor can reduce the ripple in output voltage, however, doesn't reduce the ripple in I_{DD}.

Another method for reducing the ripple in V_{PP} in case of current load is adding a clamping transistor between the pump output and the load terminals as shown in Fig. 3.18b. Compared with Fig. 3.18a without a clamping transistor, the ripple voltage at the load terminal can be reduced. As shown in the *I*–*V* graph of Fig. 3.18b, the voltage ripple ΔV_{OUT} translates into the current ripple ΔI_{PP}, and then it results in the voltage ripple ΔV_{LOAD}. Because of the steep slope in *I*–*V* with the clamping transistor, ΔV_{LOAD} can be reduced in comparison with ΔV_{OUT}. However, to keep the operation point at (V_{PP}, I_{PP}) unchanged, the pump output current needs to be increased to ($V_{\mathrm{PP}} + V_{\mathrm{DS}}$, I_{PP}), where V_{DS} is the drain to source

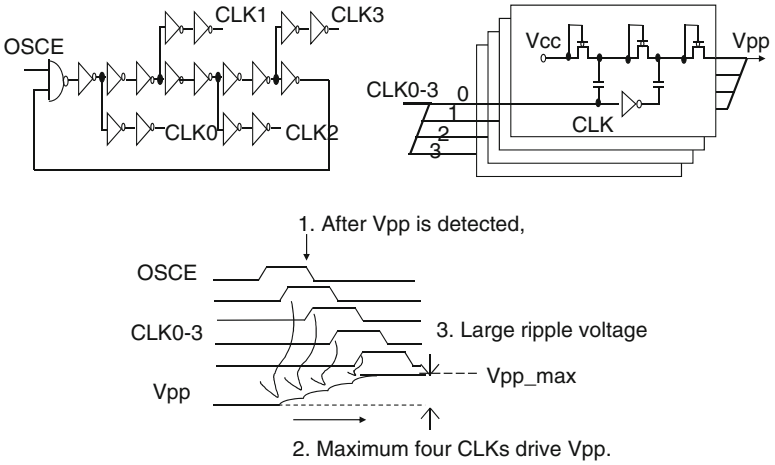


Fig. 3.19 Pump with low noise (Javanifard et al. 1994)

voltage of the clamping transistor. This requires to increase the output current at V_{PP}, resulting in a larger pump size. This technique, however, is not effective to reduce the ripple in I_{DD}.

To reduce the ripple in the supply current, another design technique is needed. Figure 3.19 describes a noise reduction method. A single pump is divided into four arrays. Every array is driven by one of four phases. Thus, both peaks in I_{OUT} and I_{DD} can be reduced by a factor of more than 2. The ripple depends on the timing when the clock enabling signal *OSCE* goes low. Figure 3.19 also shows the worst case in terms of the ripple in V_{PP}. All the four arrays operate after the oscillator enabling signal *OSCE* can go low. In this case, the ripple in V_{PP} is not reduced in comparison with a single array pump.

Figure 3.20 adds a controlled buffer for the driving signals *DRV*. As soon as *OSCE* goes low, *DRV*s stop changing their logical state and their states are latched. Thus, the ripple in V_{PP} can be minimized. After *OSCE* goes high, transferring *CLK*s to *DRV*s starts again when the logical state of *CLK*s become identical to that of *DRV*s. Thus, no simultaneous operation occurs, resulting in averaged current profile in I_{OUT} and I_{DD} as well as a low ripple in V_{PP}.

3.6 Stand-by and Active Pump Design

Some applications may need a high-voltage generated on chip with a low stand-by current condition even just after the power supply is input. In addition, the pump output current needs to be sufficient high to supply a load in an active state. When both requirements for a low current consumption in a stand-by state and a high output current in active are made simultaneously, one may have to have two pumps as shown in Fig. 3.21.

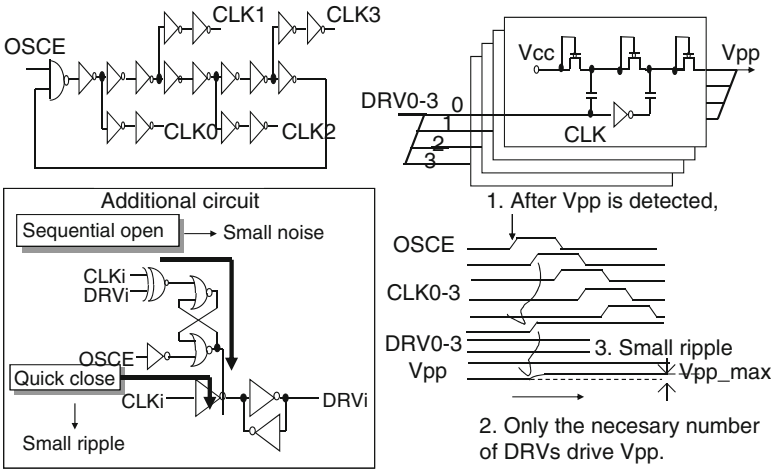


Fig. 3.20 Pump with low ripple (Tanzawa et al. 2002)

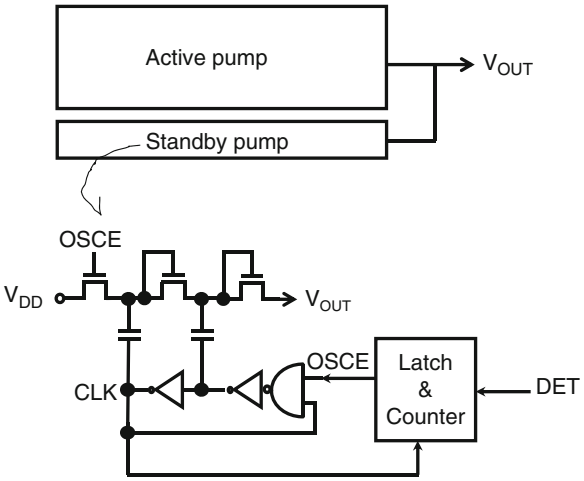


Fig. 3.21 Two pump arrays for stand-by and active states (e.g., Sato et al. 1985; Tanzawa et al. 2001)

When the leakage current at the output node is sufficiently small, the period when the stand-by pump is disabled would be quite long. During this period, all the internal capacitor nodes can be equalized to the output voltage due to the reverse subthreshold current via low-V_T transfer transistors. If the next boosting operation starts with OSCE high under such a situation, only a few clocks may be enough with relatively large pump capacitors to increase the output voltage to a target voltage and the pump operation is disabled again. Assuming the pump needs M clock cycles to output the current for recovering a reduction in the output voltage of ΔV_{PP},

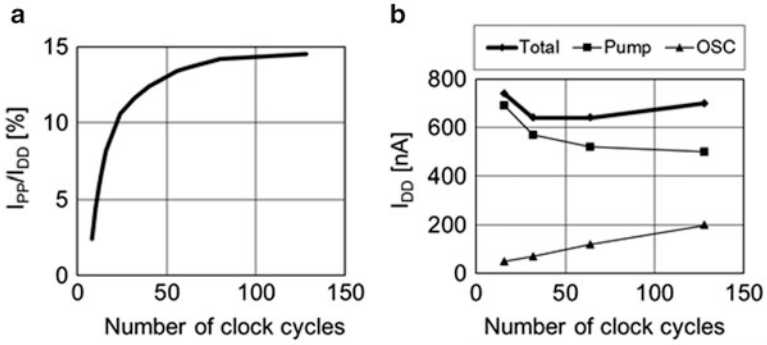


Fig. 3.22 Current efficiency I_{PP}/I_{DD} (**a**) and stand-by current I_{DD} (**b**) vs. number of clock cycles

$$\Delta V_{PP} \leq MTI_{PP}/C_{LOAD} = \alpha MC/C_{LOAD} \tag{3.4}$$

where α is a proportional coefficient $[(N + 1)V_{DD} - V_{PP}]/N$. One can simulate the amount of output charges per cycle using similar equations (2.173) to (2.178). One difference is using (3.5) instead of (2.172) because all the internal capacitor nodes are equalized to V_{PP} due to the reverse current.

$$Q(1,j) = Q(1,j+1) = CV_{PP} \tag{3.5}$$

Figure 3.22a shows simulated results under the condition of $N = 4$, $V_{DD} = 1.5$ V, and $V_{PP} = 4.5$ V. The graph suggests that one needs a number of clock cycles larger than 50 to have sufficiently high power efficiency as much as that in a steady state in this example. Figure 3.22b shows the stand-by current as a function of the number of clocks cycles. The input current to the stand-by pump decreases as the number of clocks increases because the power efficiency is improved as shown in Fig. 3.22a whereas the input current to the oscillator increases because the duty ratio of the operation time to the wait time increases thereby the averaged input current increases. Thus, the total input current has a minimum point across the number of clock cycles. In this example, M of 50–100 should be selected. For given values for ΔV_{PP}, C_{LOAD}, and α, (3.4) constrains the condition for the product MC. As a result, one can determine optimum values for M and C. The counter of Fig. 3.21 is then designed to work with the optimum M.

References

Charge Pump Design

Palumbo G, Pappalardo D (2010) Charge pump circuits: an overview on design strategies and topologies. IEEE Circ Syst Mag 10(1):31–45

Pan F, Samaddar T (2006) Charge pump circuit design, ISBN 0-07-147045-X. McGraw-Hill, New York

V_T Canceling Design

Bloch M, Lauterbauch C, Weber W (1998) High efficiency charge pump circuit for negative high voltage generation at 2 V supply voltage. In: IEEE European solid-state circuits conference, pp 100–103

D'Arrigo S, Imondi G, Santin G, Gill M, Cleavelin R, Spaglicca S, Tomassetti E, Lin S, Nguyen A, Shah P, Savarese G, McElroy D (1989) A 5 V-only 256 k bit CMOS flash EEPROM. In: ISSCC digest of technical papers, pp 132–133, Feb 1989

Favrat P, Deval P, Declercq J (1998) A high-efficiency CMOS voltage doubler. IEEE J Solid State Circ 33(3):410–416

Javanifard J, Tanadi T, Giduturi H, Loe K, Melcher RL, Khabiri S, Hendrickson NT, Proescholdt AD, Ward DA, Taylor MA (2008) A 45 nm self-aligned-contact process 1Gb NOR flash with 5 MB/s program speed. In: IEEEinternational solid-state circuits conference, pp 424–425

Kuriyama M et al (1992) A 5 V-only 0.6 μm flash EEPROM with row decoder scheme in tripple-well structure. In: ISSCC digest of technical papers, pp 152–153

Sawada K, Sugawara Y, Masui S (1995) An on-chip high-voltage generator circuit for EEPROMs with a power supply voltage below 2 V. In: Digest of technical papers, symposium on VLSI circuits, pp 75–76, June 1995

Shin J, Chung IY, Park YJ, Min HS (2000) A new charge pump without degradation in threshold voltage due to body effect. IEEE J Solid State Circ 35(8):1227–1230

Umezawa A, Atsumi S, Kuriyama M, Banba H, Imamiya K, Naruke K, Yamada S, Obi E, Shikiri MO, Suzuki T, Tanaka S (1992) A 5 V-only operation 0.6 μm flash EEPROM with row decoder scheme in triple-well structure. IEEE J Solid State Circ 27(11):1540–1546

Wu J, Chang K (1998) MOS charge pumps for low-voltage operation. IEEE J Solid State Circ 33 (4):592–597

Switching Diode Design

Kobayashi S, Mihara M, Miyawaki Y, Ishii M, Futatsuya T, Hosogane A, Ohba A, Terada Y, Ajika N, Kunori Y, Yuzuriha K, Hatanaka M, Miyoshi H, Yoshihara T, Uji Y, Matsuo A, Taniguchi Y, Kiguchi Y (1995) A 3.3 V-only 16 Mb DINOR flash memory. In: ISSCC digest of technical papers, pp 122–123, Feb 1995

Mihara M, Miyawaki Y, Ishizaki O, Hayasaka T, Kobayashi K, Omae T, Kimura H, Shimizu S, Makimoto H, Kawajiri Y, Wada N, Sonoyama H, Etoh J (1999) A 29 mm^2 1.8 V-only 16 Mb DINOR flash memory with gate-protected poly-diode charge pump. In: ISSCC digest of technical papers, pp 114–115

Storti S, Consiglieri F, Paparo M (1988) A 30 A 30 V DMOS motor controller and driver. IEEE J Solid State Circ 23(6):1394–1401

Wide V_{DD} Operation Design

Gerber B, Martin JC, Fellrath JA (1981) A 1.5 V single-supply one-transistor CMOS EEPROM. IEEE JSSC 16(3):195–200

Area Efficient Multiple Pump System Design

Tanzawa T, Tanaka T, Takeuchi K, Nakamura H (1997) Circuit technologies for a single-1.8 V flash memory. In: Symposium on VLSI circuits digest of technical papers, pp 63–64, June 1997

Low Noise Ripple Reduction Design

Javanifard J, Landgraf M, Larsen R, Leo K, Rajguru C, Sweha S, Taub M, Tedrow K, Wojciechowski K (1994), A smart auto-configuring selectable-voltage 16-Mb flash memory, 14th IEEE Non-Volatile Semiconductor Memory Workshop, Dig. Tech. Papers, vol. 5.1

Tanzawa T, Takano Y, Watanabe K, Atsumi S (2002) High-voltage transistor scaling circuit techniques for high-density negative-gate channel-erasing NOR flash memories. IEEE JSSC 37(10):1318–1325

Stand-by/Active Design

Sato K, Kawamoto H, Yanagisawa K, Matsumoto T, Shimizu S, Hori R (1985) A 20 ns static column 1 Mb DRAM in CMOS technology. In: IEEE international solid-state circuits conference, pp 254–255

Tanzawa T, Umezawa A, Kuriyama M, Taura T, Banba H, Miyaba T, Shiga H, Takano Y, Atsumi S (2001) Wordline voltage generating system for low-power low-voltage flash memories. IEEE JSSC 36(1):55–63

Chapter 4
Pump Control Circuits

Section 4.1 presents pump regulators. Some of the pump output voltages need to be varied to adjust them to the target voltages. This can be done with the voltage gain of the regulator or the reference voltage changed. The voltage divider which is a main component of the regulator has to have small voltage coefficient and fast transient response enough to make the controlled voltage linear to the trim and stable in time. A regulator for a negative voltage has a circuit configuration different from that for a positive voltage. State of the art is reviewed.

Section 4.2 deals with oscillators. Without an oscillator, the charge pump never works. In order to make the pump area small, process, voltage, and temperature variations in oscillator frequency need to be done as small as possible. There is the maximum frequency at which the output current is maximized. If the oscillator is designed to have the maximum frequency under the fastest conditions such as fast process corner, high supply voltage, and low temperature, the pump output current is minimum under the slowest conditions such as slow process, low supply voltage, and high temperature. It is important to design the oscillator with small variations for squeezing the pump area.

Section 4.3 reviews level shifters. The level shifter shifts the voltage for logic high or low of the input signal to a higher or lower voltage of the output signal. Four types of level shifters are discussed (1) high-level NMOS level shifter, (2) high-level CMOS level shifter, (3) high-voltage depletion NMOS + PMOS level shifter, and (4) low-level CMOS level shifter. The trade-offs between the first three high-voltage shifters are mentioned. The negative voltage can be switched with the low-level shifter. As the supply voltage lowers, operation margins of the level shifters decrease. As the supply voltage lowers, the switching speed becomes slower, eventually infinite, i.e., the level shifter does not work. Some design techniques to lower the minimum supply voltage at which the level shifters are functional are shown.

Section 4.4 provides voltage references. Variations in regulated high voltages increase by a factor of the voltage gain of the regulators from those in the reference voltages. Reduction in the variations in voltage references is a key to make the high voltages well controlled. Some innovated designs for low supply voltage operation are presented as well.

T. Tanzawa, *On-chip High-Voltage Generator Design*, Analog Circuits and Signal Processing, DOI 10.1007/978-1-4614-3849-6_4,

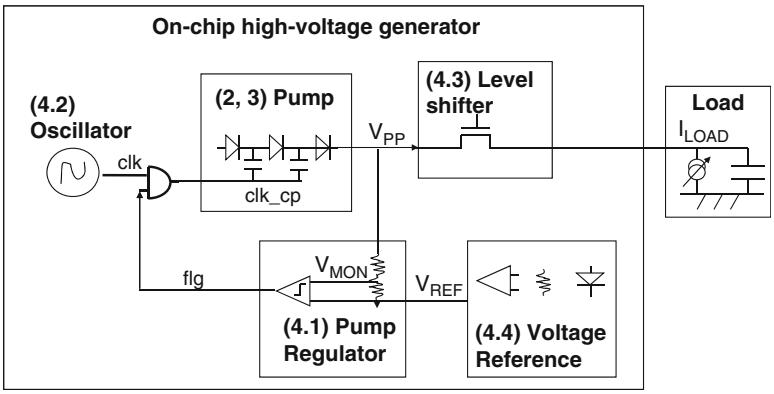


Fig. 4.1 Block diagram of on-chip high-voltage generator

Figure 4.1 shows on-chip high-voltage generator system and each component circuit block discussed in each section of this chapter. The charge pump inputs the supply voltage (V_{DD}) and the clock, which is generated by the oscillator, and outputs a voltage (V_{PP}) higher than the supply voltage or a negative voltage. The pump regulator enables the charge pump when the absolute value of the output voltage of the charge pump is lower than the target voltage on the basis of the reference voltage V_{REF}, or disables it otherwise. The output voltage of the pump is determined by the reference voltage and the voltage gain of the regulator. To vary the pump output voltage, either reference voltage or voltage gain of the regulator is varied. The generated high or negative voltage is transferred to a load through high- or low-level shifters. The level shifters are controlled by the input supply voltage. The load is capacitive, resistive, or both.

4.1 Regulator

This section presents pump regulators. Some of the pump output voltages need to be varied to adjust them to the target voltages. This can be done with the voltage gain of the regulator or the reference voltage changed. The voltage divider that is a main component of the regulator has to have small voltage coefficient and fast transient response enough to make the controlled voltage linear to the trim and stable in time. A regulator for a negative voltage has a circuit configuration different from that for a positive voltage. State of the art is reviewed.

A pump regulator shown in Fig. 4.2a detecting the output voltage of charge pump contains a voltage divider and a comparator inputting a reference voltage V_{REF}. The output signal cpen is a logic signal indicating whether the charge pump needs to operate or not. Design parameters R_1, R_2, and V_{REF} determine the target V_{PP}.

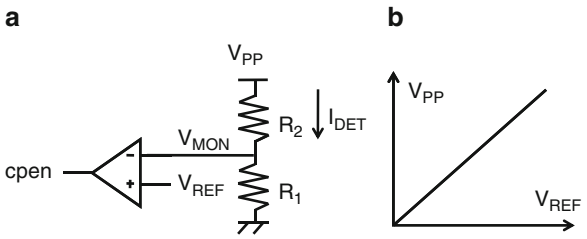


Fig. 4.2 Pump regulator for a positive high voltage V_{PP} (**a**) and ideal relation of V_{PP} to V_{REF} (**b**) (Oto et al. 1983)

$$V_{PP} = G_V V_{REF} \tag{4.1}$$

$$G_V = 1 + \frac{R_2}{R_1} \tag{4.2}$$

where G_V is the voltage gain. Practically, the output voltage can vary due to variations in each design parameter and the offset voltage V_{OS} of the comparator.

$$\begin{aligned} \delta V_{PP} &= \delta G_V V_{REF} + G_V(\delta V_{REF} + V_{OS}) \\ &= \left(\frac{\delta R_2}{R_1} - \frac{R_2 \delta R_1}{{R_1}^2}\right) V_{REF} + G_V(\delta V_{REF} + V_{OS}) \end{aligned} \tag{4.3}$$

It is assumed that each variation component is independent of one another. The standard deviation can be given by

$$\sigma {V_{PP}}^2 = \left(\frac{R_2}{R_1} V_{REF}\right)^2 \left[\left(\frac{\sigma R_1}{R_1}\right)^2 + \left(\frac{\sigma R_2}{R_2}\right)^2\right] + {G_V}^2(\sigma {V_{REF}}^2 + \sigma {V_{OS}}^2) \tag{4.4}$$

To vary V_{PP} with trimming, there are three methods. The first one is such that V_{REF} is varied whereas G_V is constant as shown in Fig. 4.2b. If the input range of the comparator is limited, the operation window would be limited in some portions in V_{REF}. The second method is such that G_V is varied whereas V_{REF} is constant. Figure 4.3a shows a trim-able resistor R_1 as shown in (4.5) using four signal input S_i $(1 \leq i \leq 4)$ to vary G_V through (4.2).

$$R_1 = \sum_{i=1}^{4} \bar{S}_i r_i \tag{4.5}$$

To reduce the impact of the transistor resistance on R_1, the transistors need to be large enough or the voltage for logic high of the signal needs to be high enough.

The third one is adding a modulation part to the resistor divider, as shown in Fig. 4.4. Suppose a current source with V_{MOD}/R_3 is connected at the V_{MON} node, V_{PP} is given by two parts of V_{REF} and V_{MOD}, as shown by (4.6). This means that V_{PP}

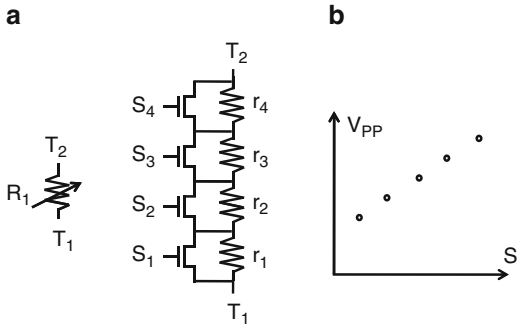


Fig. 4.3 Trim-able resistor (**a**) and ideal relation of VPP to S (**b**) (Suh et al. 1995)

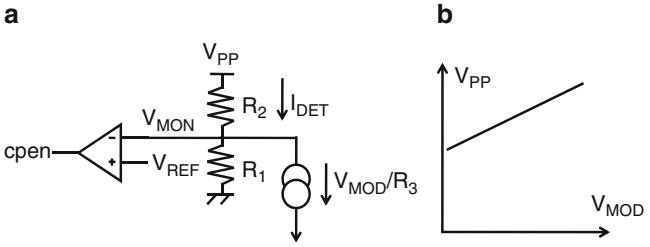


Fig. 4.4 Pump regulator with a voltage modulation path (Tanzawa and Harrington 2010)

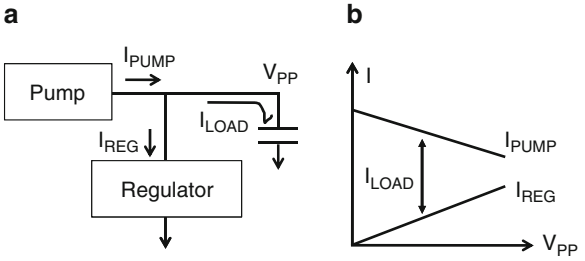


Fig. 4.5 Current components of a pump and a regulator

varies with V_{MOD} varied while V_{REF} unchanged. If one can add a modulation component into V_{MOD}, V_{PP} has the characteristic as shown in Fig. 4.4b.

$$V_{PP} = \left(1 + \frac{R_2}{R_1}\right) V_{REF} + \frac{R_2}{R_3} V_{MOD} \tag{4.6}$$

Figure 4.5a shows the current components of a pump and a regulator. As the output voltage of the pump increases, the pump output current I_{PUMP} decreases

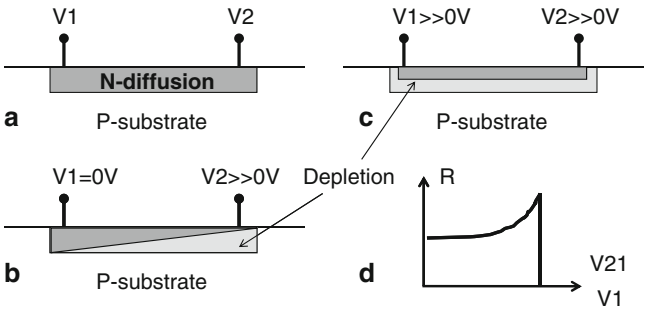


Fig. 4.6 n-diffusion resistor (**a**), two bias conditions (**b**), (**c**), resistance vs. bias relation (**d**)

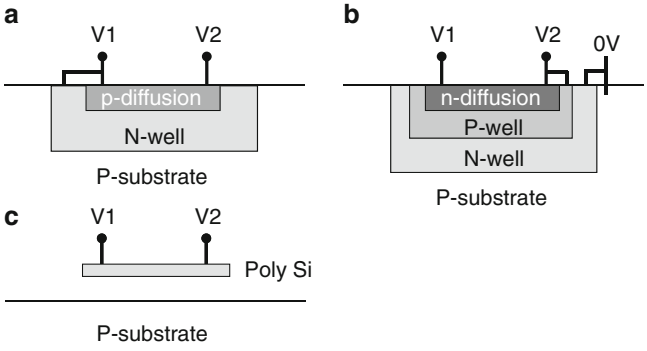


Fig. 4.7 Other types of resistors: p-diffusion resistor (**a**), n-diffusion resister in a twin well (**b**), poly silicon resister (**c**)

whereas the current to the regulator I_{REG} increases as shown in Fig. 4.5b. The effective current to charge the load, I_{LOAD}, therefore decreases as V_{PP}. Thus, the detector current needs to be made low enough not to affect I_{LOAD} much.

Figure 4.6a shows an n-diffusion resister fabricated on the p-type substrate. When a terminal of the resister is applied by a high voltage V_{PP}, depletion region width increases, resulting in higher resistivity with a thinner conduction layer as shown in Fig. 4.6b. Similar behavior is seen when both terminals are applied by high voltages as shown in Fig. 4.6c. Figure 4.6d indicates that the voltage coefficient of the resistance is small at a low voltage applied and increases as the applied voltages. Over a junction breakdown voltage, it is no longer available as a resistor.

Figure 4.7 illustrates three other types of resistors. When N-well is divided into multiple pieces and every N-well has p-diffusion layers, voltage differences between the p-diffusion layers and N-wells can be reduced to mitigate the nonlinearity of the resistance on the voltages applied in comparison with a single n-diffusion layer on the substrate. To allow a negative voltage to be detected by a pump regulator, n-diffusion layers fabricated on P-well isolated by N-well as shown in Fig. 4.7b. Poly-silicon resistor has benefits of small voltage dependency on the resistivity and of availability of both polarities.

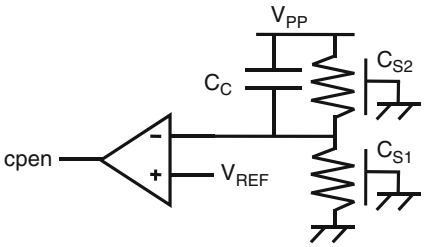


Fig. 4.8 Pump regulator with a shunt capacitor C_C

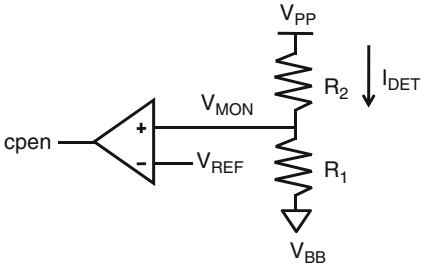


Fig. 4.9 Pump regulator for a negative voltage V_{BB}

The current used for the regulator is a part of the load current of the pump. In order to reduce the current I_{DET}, the resistor R_1 is likely high impedance. Assuming V_{REF} is 1 V and I_{DET} is 10 μA, R_1 is required to be 100 kΩ. Furthermore, when V_{PP} is 20 V, R_2 is required to be 1.9 MΩ. Parasitic capacitance of the resistor depends on the material used. In case of diffusion resistor, its parasitic capacitance per Ω is relatively large. Assuming 1 pF/MΩ, the time constant of R_2 is about 4 μs. When the rise time of V_{PP} is shorter than or compatible to 4 μs, the output of the pump can have large overshoot. To reduce the propagation delay from V_{PP} to V_{MON}, a shunt capacitor C_C is used as shown in Fig. 4.8. DC operating point is determined by the divider ratio whereas AC signal travels via C_C.

Figure 4.9 shows a negative voltage detector. The circuit requires a well-controlled regulated voltage V_{PP} to detect the negative voltage at V_{BB}, because there is an additional term in (4.8) compared with (4.1).

$$\frac{V_{PP} - V_{REF}}{R_2} = \frac{V_{REF} - V_{BB}}{R_1} \tag{4.7}$$

$$V_{BB} = \left(1 + \frac{R_1}{R_2}\right) V_{REF} - \frac{R_1}{R_2} V_{PP} \tag{4.8}$$

Sensitivity of V_{BB} on each parameter is calculated by

$$\delta V_{BB} = \left(1 + \frac{R_1}{R_2}\right)(\delta V_{REF} + V_{OS}) - \frac{R_1}{R_2}\delta V_{PP} + \left(\frac{\delta R_1}{R_2} - \frac{R_1 \delta R_2}{{R_2}^2}\right)(V_{REF} - V_{PP}) \tag{4.9}$$

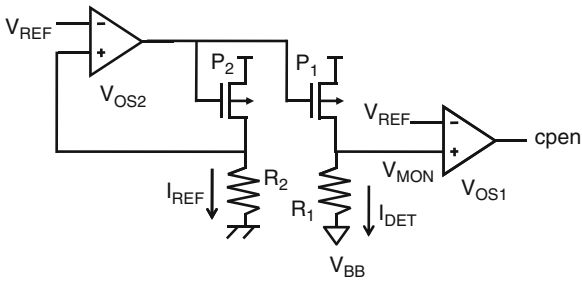


Fig. 4.10 Pump regulator for a negative voltage V_{BB} with a reduced gain against variations (Mihara et al. 1999)

The standard deviation can be given by

$$\sigma V_{BB}{}^2 = \left(\frac{R_1}{R_2}\right)^2 (V_{REF} - V_{PP})^2 \left[\left(\frac{\sigma R_1}{R_1}\right)^2 + \left(\frac{\sigma R_2}{R_2}\right)^2\right] + \left(1 + \frac{R_1}{R_2}\right)^2 (\sigma V_{REF}{}^2 + \sigma V_{OS}{}^2) + \left(\frac{R_1}{R_2}\right)^2 \sigma V_{PP}{}^2 \tag{4.10}$$

When V_{BB} is shifted by $\triangle V_{BB}$, V_{MON} is shifted by $\triangle V_{MON}$ as follows.

$$\Delta V_{MON} = \Delta V_{BB} \Big/ \left(1 + \frac{R_1}{R_2}\right) \tag{4.11}$$

The amplitude of the input signal to the comparator is scaled from that of V_{BB} by a factor of $1 + R_1/R_2$. The detector shown in Fig. 4.10 increases the input signal amplitude.

In an ideal case with no mismatch in the parameters, the following equations hold.

$$V_{MON} - V_{BB} = I_{DET} R_1 \tag{4.12}$$

$$I_{REF} = \frac{V_{REF}}{R_2} = I_{DET} \tag{4.13}$$

where it is assumed that two PMOSFETs P_1 and P_2 are identical in size. Using the steady state condition of $V_{MON} = V_{REF}$ for (4.12) and (4.13), V_{BB} can be given by

$$V_{BB} = G_V V_{REF} \tag{4.14a}$$

$$G_V = 1 + \frac{R_1}{R_2} \tag{4.14b}$$

Because I_{DET} has no V_{BB} dependence in (4.12), the sensitivity of V_{MON} on V_{BB} is given by

$$\Delta V_{MON} = \Delta V_{BB} \tag{4.15}$$

When one uses long channel *I*–*V* equations, the following relations hold.

$$I_{REF} = K(V_{GS} - V_{T2})^2 \tag{4.16a}$$

$$I_{DET} = K(V_{GS} - V_{T1})^2 \tag{4.16b}$$

where V_{GS} is the gate-to-source voltage of P_1 and P_2 and V_{T1} and V_{T2} are the threshold voltages of P_1 and P_2. When the opamps have input offset voltages of V_{OS1} and V_{OS2}, as shown in Fig. 4.10, and the device parameters are independently varied, I_{REF} varies by (4.17a).

$$\delta I_{REF} = \frac{\delta V_{REF} + V_{OS2}}{R_2} - \frac{V_{REF}\delta R_2}{{R_2}^2} \tag{4.17a}$$

From (4.16a, 4.16b) and the assumption that V_{T2} is mismatched from V_{T1} by δV_T,

$$\delta I_{DET} = \delta I_{REF} - 2\sqrt{KI_{REF}}\delta V_T \tag{4.17b}$$

In addition, from (4.12),

$$V_{OS1} - \delta V_{BB} = \delta I_{DET} R_1 + I_{DET}\delta R_1 \tag{4.17c}$$

Using (4.17a, 4.17b, 4.17c) and (4.13), overall variation is given by

$$\begin{aligned}\delta V_{BB} &= V_{OS1} - I_{DET}\delta R_1 - \delta I_{DET} R_1 \\ &= V_{OS1} - \frac{V_{REF}}{R_2}\delta R_1 - \left(\frac{\delta V_{REF} + V_{OS2}}{R_2} - \frac{V_{REF}\delta R_2}{{R_2}^2} - 2\sqrt{KI_{REF}}\delta V_T\right) R_1\end{aligned} \tag{4.18}$$

Assuming each variation component is independent, the standard deviation can be calculated by

$$\begin{aligned}{\sigma V_{BB}}^2 = {\sigma V_{OS1}}^2 &+ \left(\frac{R_1}{R_2}\right)^2 ({\sigma V_{REF}}^2 + {\sigma V_{OS2}}^2) \\ &+ \left(\frac{R_1}{R_2} V_{REF}\right)^2 \left[\left(\frac{\delta R_1}{R_1}\right)^2 + \left(\frac{\delta R_2}{R_2}\right)^2\right] + 4KI_{REF}{R_1}^2{\sigma V_T}^2\end{aligned} \tag{4.19}$$

Another interesting design technique is using a capacitor divider as shown in Fig. 4.11. It does not require a resistor, which can be applied by a negative voltage. Initially, V_{MON} is precharged to $2V_{REF}$ and then V_{MON} is made floating. Accordingly as V_{OUT} goes low, V_{MON} is also pulled down. Once V_{MON} reaches V_{REF}, the detection signal cpen goes *L*. As far as the operation time of the negative voltage generation is short enough so that the leakage current at the floating node is negligibly small, the regulator should function well.

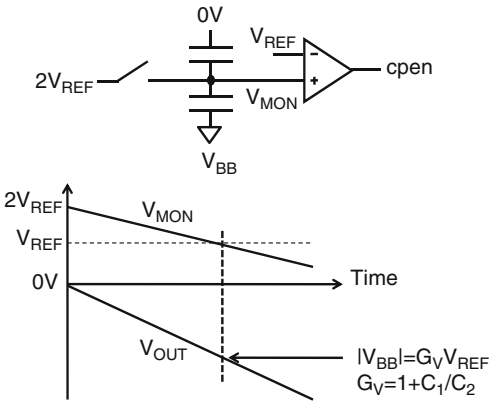


Fig. 4.11 Capacitor divider for regulating a negative voltage (Venkatesh et al. 1996)

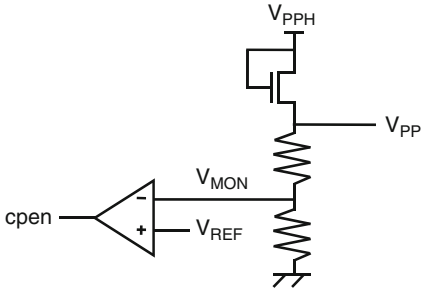


Fig. 4.12 Regulator with one diode to generate a switching voltage V_{PPH}

As will be described in Sect. 4.3 for high-voltage switching circuits, a regulator shown in Fig. 4.12 has two output terminals whose voltages are V_{PPH} and V_{PP}. A pump is connected with V_{PPH}. When V_{PPH} is supplied to the gate of a switching pass NMOS transistor, it can transfer V_{PP} without any voltage loss as shown in Fig. 4.36.

$$V_{PPH} = V_{PP} + V_T \tag{4.20a}$$

$$V_{PP} = G_V V_{REF} \tag{4.20b}$$

4.2 Oscillator

This section deals with oscillators. Without an oscillator, the charge pump never works. In order to make the pump area small, process, voltage, and temperature variations in oscillator frequency need to be done as small as possible. There is the maximum frequency at which the output current is maximized. If the oscillator is designed to have the maximum frequency under the fastest conditions such as fast process corner, high supply voltage, and low temperature, the pump output current

Table 4.1 Requirement for pump oscillator

Oscillator type	Type 1: Use of a linear regulator for V_{DD}	Type 2: No use of V_{DD} regulation
Features	– T should be insensitive to PVT – Decoupling capacitors for V_{DD} regulated is needed	– T needs to be proportional to $(N + 1)(V_{DD}–V_T)–V_{PP}$ – T should be insensitive to PT

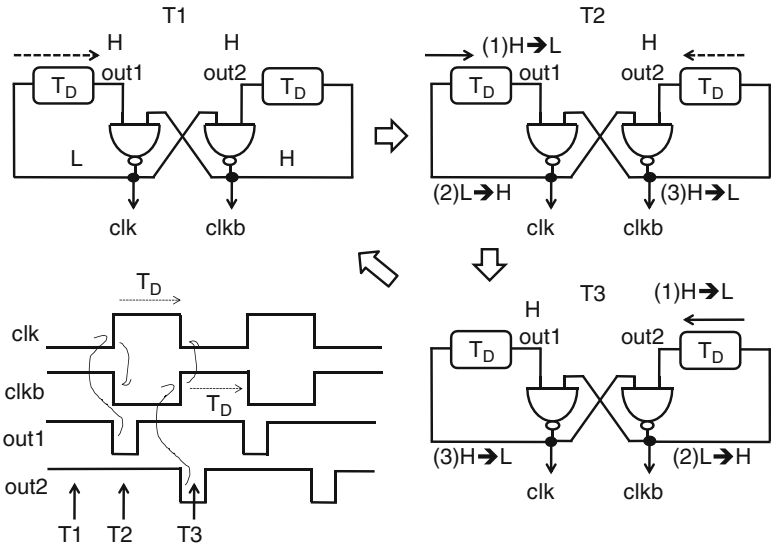


Fig. 4.13 Bi-stable oscillator generating two phase clock

is minimum under the slowest conditions such as slow process, low supply voltage, and high temperature. It is important to design the oscillator with small variations for squeezing the pump area.

The primal target for oscillators is making I_{PP} insensitive to process, voltage, and temperature (PVT) variations. What is the parameter which is not varied much? C is very accurately fabricated within a few percent errors. N is solid. V_T can be a weak function of temperature and process variation. V_{PP} is the solid target. V_{DD} may be varied a lot without an on-chip voltage regulator or quite solid with it. Thus, there are two cases, use of a linear regulator for V_{DD} or not. In the former case, all the parameters should be stable to realize the clock frequency or period insensitive to process, voltage, and temperature. To stabilize V_{DD}, you may need large decoupling capacitors. In case of no V_{DD} regulator, T would need to be proportional to the factor $(N + 1)(V_{DD} – V_T) – V_{PP}$ to make I_{PP} insensitive to PVT variation (Table 4.1).

Figure 4.13 describes a bi-stable oscillator and its operation. It is known that symmetrical bi-stable oscillator generates two phase clock with 50% high low duties. The half period time is determined by the delay element T_D. One can start

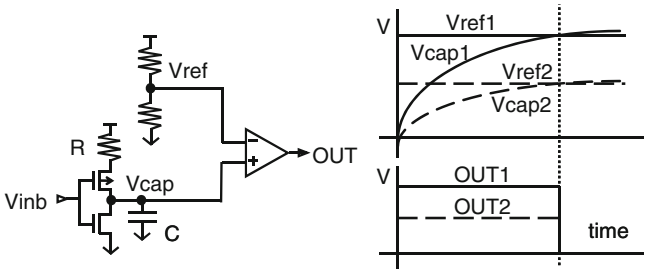


Fig. 4.14 Delay circuit with a delay time proportional to CR (Watanabe et al. 1989)

with T1 where out1 and 2 are high and clk and clkb are L and H, respectively. clk L propagates to out1 after T_D. That flips clk to H, in turn flips clkb to L. clkb L propagates to out2 after T_D. That flips clkb to H, which flips clk to L. Thus, the oscillator has two states alternately and half period is determined by T_D. This kind of oscillator is known as bi-stable oscillator. The delay circuit shown in Fig. 4.13 can be used for the delay element as described by T_D of Fig. 4.14. The clock period T_C is simply given by $2T_D$ as far as the delay of logic gates is negligibly small compared with T_D. Two delay elements alternately work to have a stable period T_C given by $2T_D$.

Oscillators are composed of multiple delay elements. To have stable oscillators against PVT variations, stable delay elements are essential. When a resistor more stable against PVT variations than channel resistance of a transistor is available, one should use it. Figure 4.14 describes a delay circuit whose delay time is basically determined by the multiple of resistance R and capacitance C.

The circuit operates as follows. When the input signal Vinb goes low, the current flows from the supply voltage V_{DD} to the capacitor node.

$$C\frac{dV_{CAP}(t)}{dt} = \frac{V_{DD} - V_{CAP}(t)}{R} \tag{4.21}$$

The reference voltage is proportional to V_{DD}, where α is a division ratio.

$$V_{REF} = \alpha V_{DD} \tag{4.22}$$

Under the initial condition where $V_{CAP}(0)$ is 0 V, $V_{CAP}(t)$ is solved to be

$$V_{CAP}(t) = V_{DD}\left(1 - e^{-\frac{t}{CR}}\right) \tag{4.23}$$

The output is flipped when V_{CAP} reaches V_{REF}. The delay time T_D is then given by

$$T_D = -CR\ln(1-\alpha) \tag{4.24}$$

Because this equation does not include V_{DD}, T_D is theoretically independent of variation in V_{DD}. "1" and "2" added to the labels of the waveform of Fig. 4.14

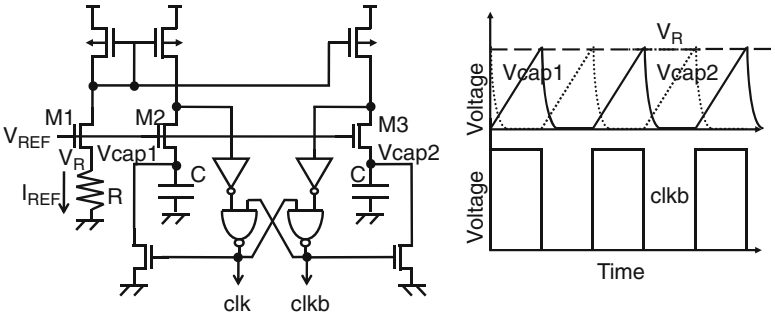


Fig. 4.15 A bi-stable oscillator (Cernea et al. 1989)

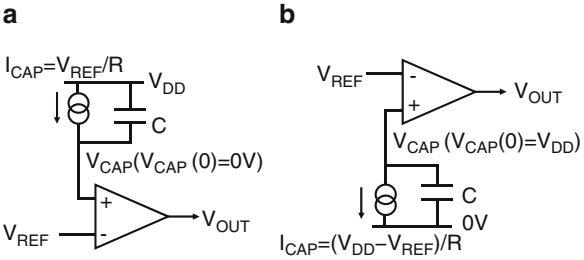


Fig. 4.16 Concept of a delay circuit (Tanzawa and Tanaka 1995)

indicate different V_{DD}. Suppose V_{REF1} is twice as large as V_{REF2} due to the variation in V_{DD}. V_{CAP1} goes high twice faster than V_{CAP2} does, resulting in the same delay in OUT1 and OUT2. Nominally the variations in R against process and temperature are smaller than those in the channel resistance of transistor R_{CH}. Therefore, overall variation can be small with R than with R_{CH}.

Figure 4.15 shows another oscillator with the period that is determined by RC, where V_R is the voltage at the upper terminal of the resistor and I_{REF} is the reference current flowing the resistor and PMOSFETs connected with the clamp NMOSFET M2, 3. The capacitor voltages $V_{CAP1,2}$ increase linearly to time with I_{REF}. After the source voltages of M2,3 reach V_R, the impedance of M2,3 rapidly increases, resulting in rapid increase in the drain voltages of M2,3. The delay time from the time when V_{CAP1} starts going up to the time when V_{CAP1} reaches V_R is given by CV_R/I_{REF}. Even though V_R and I_{REF} vary according to the threshold voltage of M1, their ratio is constant as R as given below.

$$I_{REF} = V_R/R = K(V_{REF} - V_R - V_T)^2 \tag{4.25}$$

$$T_C/2 = CV_R/I_{REF} = RC \tag{4.26}$$

Figure 4.16 illustrates the concept of another delay circuit, which has the delay time with small PVT variations. In Fig. 4.16a, the initial voltage at the capacitor

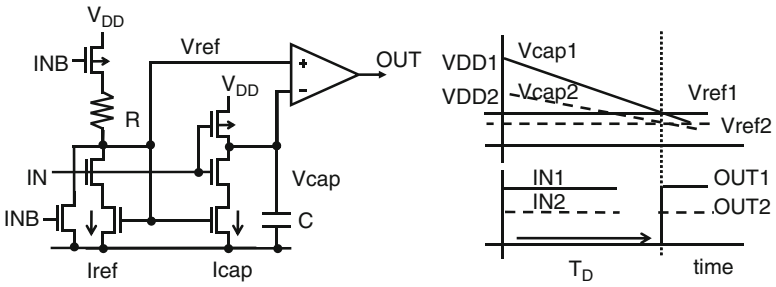


Fig. 4.17 A delay circuit (Tanzawa and Tanaka 1995)

node is set to 0 V. The charging current I_{CAP} is made to be V_{REF}/R, where V_{REF} is the reference voltage for the comparator. The delay time when V_{CAP} reaches V_{REF} is given by

$$I_{CAP} = V_{REF}/R \tag{4.27a}$$

$$T_D = CV_{REF}/I_{CAP} = RC \tag{4.28a}$$

In Fig. 4.16b, the initial voltage at the capacitor node is set to V_{DD}. The discharging current I_{CAP} is made to be $(V_{DD} - V_{REF})/R$. The delay time when V_{CAP} reaches V_{REF} is given by

$$I_{CAP} = (V_{DD} - V_{REF})/R \tag{4.27b}$$

$$T_D = C(V_{DD} - V_{REF})/I_{CAP} = RC \tag{4.28b}$$

Thus, both circuits can have the same delay time with small PVT variations.

Figure 4.17 shows a circuit realizing the concept of Fig. 4.16b. As shown by (4.27) and (4.28), the delay time is ideally independent of V_{DD} and V_T of transistors, resulting in small PVT variations. The key point here is that the voltage swing at the capacitor node V_{CAP} is proportional to the reference current I_{REF}. V_{DD} and V_T are not included in the ratio of the voltage amplitude of V_{CAP} and I_{REF}. Figure 4.18 has two sets of the delay elements of Fig. 4.17. The clock period is given by $2T_D$.

To change the type 1 oscillator into type 2, I_{REF} is made to have less V_{DD} dependency unlike the type 1, as shown in Fig. 4.19. Because the capacitor voltage has amplitude of $V_{DD} - V_R$, the clock cycle is given by

$$T_C/2 = C(V_{DD} - V_R)/I_{REF} \tag{4.29}$$

Equation (4.29) indicates the clock period increases as V_{DD}. To visualize this fact, one can compare a low V_{DD} case shown in Fig. 4.19b with a high V_{DD} case shown in Fig. 4.19c. The slopes in $V_{CAP1,2}$ during the discharging period are same. Thus, as the amplitude increases with V_{DD}, the delay time also increases.

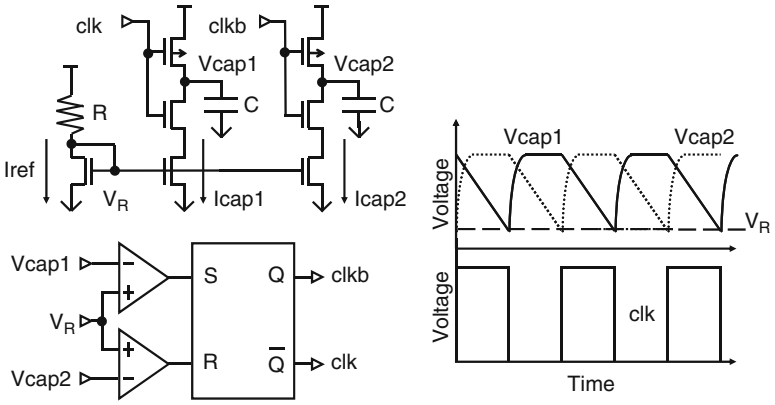


Fig. 4.18 Stable oscillator (type 1) using a delay element described in Fig. 4.17 (Tanzawa and Tanaka 1995)

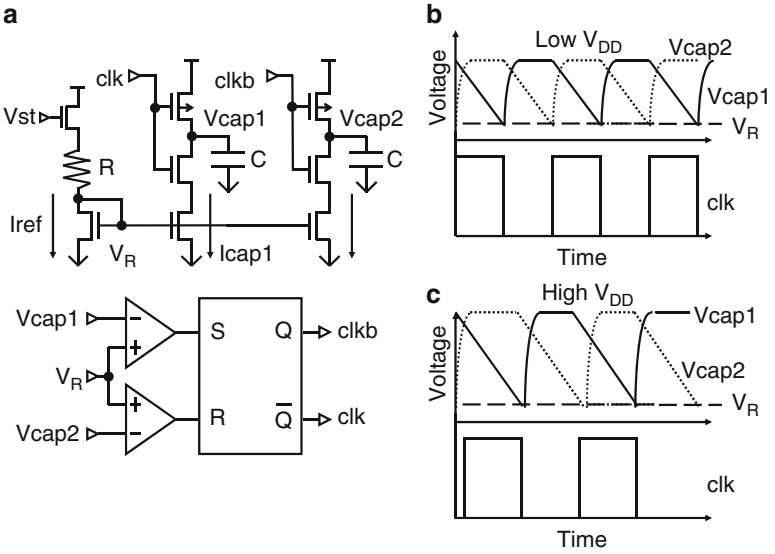


Fig. 4.19 Stable oscillator (type 2) using a delay element described in Fig. 4.17 (Tanzawa and Tanaka 1995)

Four nonoverlapping phases Φ1–4 are provided by logical addition or multiplication of clk1–4, each is the clock delayed by a same amount T_D, as shown in Fig. 4.20. It is noted that T_D also needs to be stable against PVT variations, because the effective pulse width to transfer the charges from one capacitor to the next one in the charge pump is given by $T_C/2–3T_D$.

Figure 4.21 illustrates a clock generator to output multiphase clocks. In Sect. 3.5, it was discussed that multiple arrays operating with multiple shifted phases could

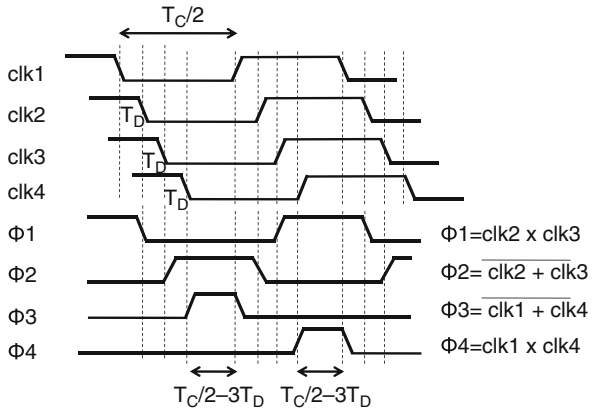


Fig. 4.20 Waveform of four nonoverlapping phases Φ1–4

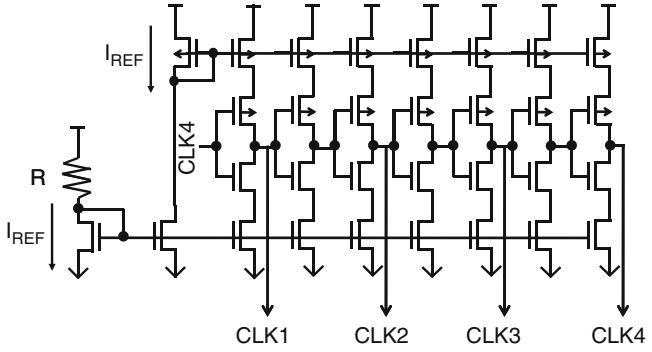


Fig. 4.21 Multiphase clock generator for peak noise reduction

reduce noise in pump current. The ring oscillator does this. Current sources are connected to both PMOS and NMOS sides to control the operating currents proportional to I_{REF}. Thus, when I_{REF} is proportional to $V_{DD} - V_T$, the clock cycle time is insensitive to PVT variations. On the other hand, when I_{REF} is independent of V_{DD}, the cycle time could be proportional to V_{DD} but insensitive to PT variation.

4.3 Level Shifter

This section reviews level shifters. The level shifter shifts the voltage for logic high or low of the input signal to a higher or lower voltage of the output signal. Four types of level shifters are discussed (1) high-level NMOS level shifter, (2) high-level CMOS level shifter, (3) high-voltage depletion NMOS + PMOS level

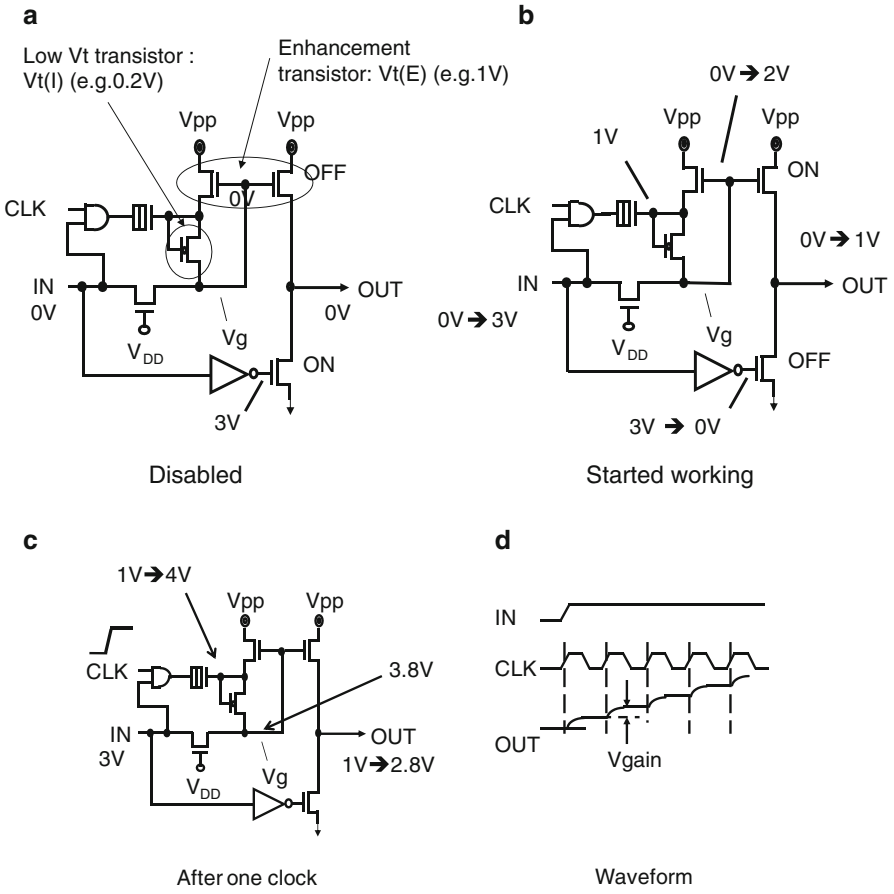


Fig. 4.22 NMOS high-level shifter (Donaldson et al. 1983, Dham et al. 1983)

shifter, and (4) low-level CMOS level shifter. The trade-offs between the first three high-voltage shifters are mentioned. The negative voltage can be switched with the low-level shifter. As the supply voltage lowers, operation margins of the level shifters decrease. As the supply voltage lowers, the switching speed becomes slower, eventually infinite, i.e., the level shifter does not work. Some design techniques to lower the minimum supply voltage at which the level shifters are functional are shown.

4.3.1 NMOS Level Shifter

Section 4.3 starts with an NMOS high-level shifter shown in Fig. 4.22. Early days electrically erasable programmable ROM had only NMOS transistor for managing high voltages. To transfer a high voltage through NMOSFET only without any

voltage drop, an overdrive voltage needs to be generated locally. To fully cut off the transfer gate when it is disabled, an enhancement transistor with a high threshold voltage V_{tE} is used. To operate the local booster at a low supply voltage, a low-Vt transistor is used. Such devices are fabricated without implanting Boron. When the input voltage is 0 V, the grounding NMOS turns on and the high-side NMOSFETs turn off with the gate grounded. When the circuit starts working, an input voltage of 3 V is transferred partially, that is, 2 V to the gates of the high-side NMOSFETs. Thus, the output voltage is 1 V. Then, the clock goes to 3 V, generating a local boosted voltage of 4 V. One diode drop of 3.8 V appears at the gate, resulting in an increase in the output voltage from 1 V to 2.8 V.

Unlike CMOS switches with large parasitic capacitance of N-well for PMOSFETs, this NMOS high-level shifter has small gate-, junction-, and wiring-capacitance, resulting in low power consumption. However, this switch also has a disadvantage in that the minimum operating supply voltage V_{DD} is mainly limited by the threshold voltage of an enhancement transistor, which prevents the leakage current from flowing in the V_{PP} switch in an inactive state. A diode-connected intrinsic transistor without channel implantation is used to improve the positive-feedback efficiency of the booster when selected for operation. The minimum operating V_{DD} is extracted.

Switching operation starts with the input signal *IN* high. After that the input clock oscillates to raise the output voltage. The source voltage of the enhancement transistor is lower by the threshold voltage V_{tE} than the gate voltage V_G with the clock *clk* high. After that, the *clk* turns to low and the gate voltage increases by $V_{DD}-V_{tE}-V_{tI}$. This is the voltage gain per cycle, V_{GAIN}. Continuing this process alternately, the gate voltage reaches $V_{PP} + V_{tE}$ and V_{PP} is output. The necessary condition that the voltage gain be positive at the gate voltage of $V_{PP} + V_{tE}$ is expressed by

$$V_{GAIN} \equiv V_{DD} - V_{tE} - V_{tI} \tag{4.30}$$

at a back bias of $V_{PP} + V_{tE}$. Therefore, the minimum operating supply voltage V_{DD_MIN} is given by

$$V_{DD\_MIN} \equiv V_{tE} + V_{tI} \tag{4.31}$$

When a V_{PP} of 18 V, V_{tE} of 1.7 V, and V_{tI} of 0.7 V at a back bias of 18 V are assumed, the minimum operating supply voltage and the maximum voltage for the switching gate are, respectively, 2.4 V and 19.7 V. Thus, V_{tE} raises the V_{DD_MIN} and the maximum V_g in the NMOS V_{PP} switch. To decrease V_{DD_MIN} for low voltage operation, V_{tE} needs to be reduced, but the leakage current flowing from V_{PP} would increase accordingly.

Figure 4.23 overcomes these two contradictory constraints, i.e., reduction of V_{DD_MIN} and elimination of the leakage current from V_{PP} at a sacrifice of a little higher I_{DD} in active mode. All of the high-voltage transistors except for the pull-down used in the switch are intrinsic ones. Instead of the enhancement transistor in

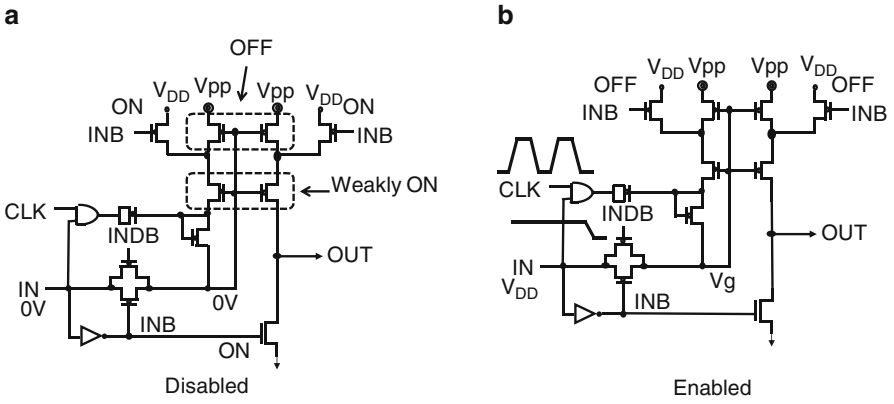


Fig. 4.23 Low voltage NMOS high-level shifter (Tanzawa et al. 1997)

the standard NMOS level shifter, three intrinsic transistors whose V_{tI} at a body bias of 0 V is around 0 V are used. In selected state, the input signal *IN* turns to high. In Fig. 4.23, the voltage gain per cycle, V_{GAIN} and the minimum operating supply voltage V_{DD_MIN} are respectively given by

$$V_{GAIN} \equiv V_{DD} - 2V_{tI} \tag{4.32}$$

$$V_{DD\_MIN} \equiv 2V_{tI} \tag{4.33}$$

As shown in Fig. 4.23a, in disabled state, the third low-Vt transistor connected between the serially connected low-Vt transistors forces the intermediate node to 1 V or higher. This bias condition creates a negative V_{GS} of the upper transistor, resulting in no leakage current flowing from V_{PP}. On the other hand, the lower transistor can flow a finite leakage current from V_{DD} even with the gate grounded, resulting in a slight increase in active current. In this example, V_{DD_MIN} can be reduced from 2.5 V to 1.5 V, as shown in Fig. 4.24. In the case of a V_{PP} of 18 V, V_{tE} of 1.7 V, and V_{tI} of 0.7 V at a back bias of 18 V, each of V_{GAIN} and V_{DD_MIN} is reduced by 1 V comparing (4.32) with (4.30) and (4.33) with (4.31).

Figure 4.25 shows another topology of NMOS level shifter. The circuit uses depletion NMOS M1–3 and enhancement NMOS M4 instead of using low-Vt or enhancement NMOS and driving clock. When the input signal *IN* is high, M4 turns on to output low. M1 biases the source terminal of M2, so that M2 is cut off to prevent the leakage current from flowing from V_{PP} at a sacrifice of an increase in I_{DD}. The depletion NMOS needs to have the conditions on $|V_t|$ as given below.

$$|V_t(V_{BS} = -V_{DD})| < V_{DD} \tag{4.34}$$

$$V_t(V_{BS} = -V_{PP}) < 0\,V \tag{4.35}$$

Equation (4.34) guarantees that M2 is off when *IN* is high. Equation (4.35) shows that the output is as high as V_{PP} without any voltage drop when *IN* is low.

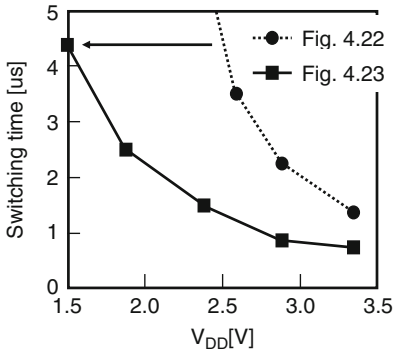


Fig. 4.24 V_{DD} vs. switching time (Tanzawa et al. 1997)

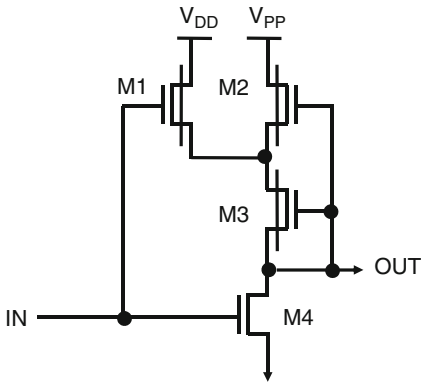


Fig. 4.25 Depletion and enhancement NMOS high-level shifter (Lucero et al. 1983a)

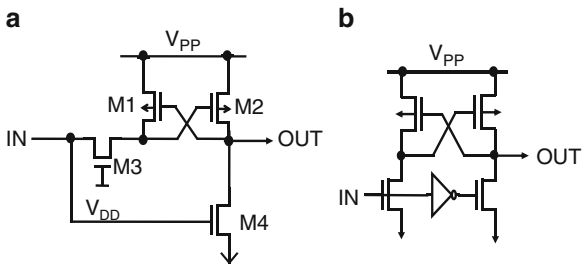


Fig. 4.26 CMOS high-level shifter (e.g., Tanaka et al. 1984; Mehrotra et al. 1984)

4.3.2 CMOS High-Level Shifter

This subsection focuses on CMOS high-level shifter with two cross-coupled PMOS and two complementary pull-down NMOS, as shown in Fig. 4.26.

Figure 4.27 shows level shifter operations. When the input goes from 0 V to V_{DD} of 2 V, the output is supposed to go from 0 V to V_{PP} (a). Thus, the high level increases V_{OUT} from V_{DD} to V_{PP}. One can divide the period into three portions (b),

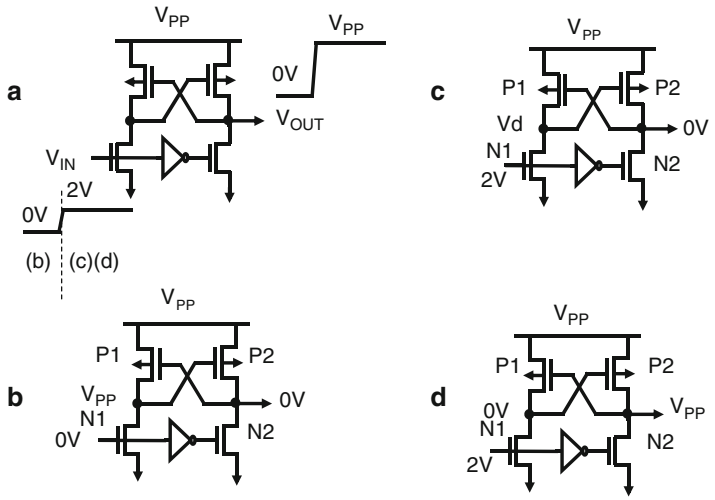


Fig. 4.27 CMOS high-level shifter

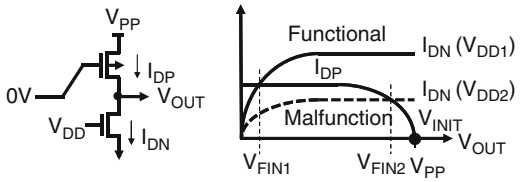


Fig. 4.28 Operating point of the CMOS high-level shifter

(c), and (d). When the input is 0 V as in (b), V_{OUT} is grounded thereby P1 turns on. Because N1 is off, the drain voltage of N1 is stable at V_{PP}, which turns off P2. As a result, all the nodes are in a latched state with no DC current flowing. When the input goes to 2 V as in (c), both N1 and P1 flow the current from V_{PP} to ground. Figure 4.28 shows the behavior in this transition. Suppose the NMOS is much stronger than PMOS as shown in the V_{OUT}–I_{DS} curves. The initial V_{OUT} is V_{PP} as shown by V_{INIT}. Because the NMOS current I_{DN} is larger than the PMOS current I_{DP}, the operating point is moving to V_{FIN1}. At this point, P2 strongly turns on and so the output node increases up to V_{PP}, which makes P1 turn off as shown in Fig. 4.27d. Thus, the drain voltage of N1 finally reaches 0 V. Because the circuit has symmetry, the same operation occurs when the input goes down to 0 V. Because V_{GS} of PMOS can be much larger than that of NMOS, the W/L ratio has to be sufficiently imbalanced. To estimate the dimensions, a long channel approximation model is used. The drain current of PMOS and NMOS transistors under the bias condition as shown in Fig. 4.28 is given by

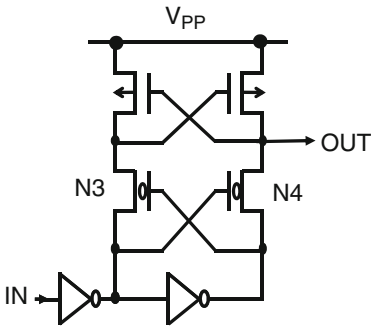


Fig. 4.29 Low V_{DD} CMOS high-level shifter with low-Vt NMOS N3, N4 (Tanzawa et al. 2001)

$$I_{DP} = \frac{\mu_h C_{OX}}{2} \frac{W_P}{L_P} (V_{PP} - |V_{tP}|)^2 \tag{4.36}$$

$$I_{DN} = \frac{\mu_e C_{OX}}{2} \frac{W_N}{L_N} (V_{DD} - V_{tN})^2 \tag{4.37}$$

where $\mu_{h(e)}$ is the mobility of hole (electron), C_{ox} is the gate capacitance per area, $W_{P(N)}$ is the channel width of P(N)MOSFET, $L_{P(N)}$ is the channel length of P(N) MOSFET, and $V_{tP(N)}$ is the threshold voltage of P(N)MOSFET. To pull down the output node enough to invert the state, the equivalent point where the NMOS current is equivalent to the PMOS current needs to be not as high as V_{FIN2} but as low as V_{FIN1} as shown in the waveform of Fig. 4.28.

Thus, the condition where the level shifter works is given by

$$I_{DN\_MIN} > I_{DP\_MAX} \tag{4.38}$$

Assuming

$$\mu_h = \mu_e/2 \tag{4.39}$$

Equations (4.36)–(4.38) are reduced to

$$A_P/A_N \equiv \frac{W_P}{L_P} \Big/ \frac{W_N}{L_N} < 2(V_{DD\_MIN} - V_{tN})^2 \Big/ (V_{PP\_MAX} - |V_{tP}|)^2 \tag{4.40}$$

In case of $V_{DD\_MIN} = 1.5$ V, $V_{PP\_MAX} = 4$ V, and $|V_{tP(N)}| = 1$ V, the aspect ratio A_P/A_N needs to be smaller than 1/18.

To allow lower voltage operation without increasing the switching delay, transistor sizes need to be kept same without I_{DN} reduced. Figure 4.29 shows a CMOS high-level shifter with low-Vt NMOS N3, N4 with $V_{tN} \sim 0$ V.

To what extent the low-Vt NMOS can reduce V_{DD_MIN}? In order to not flow a standby current, one only needs to bias the source terminal when the gate is grounded, as shown in 4.40. Thus, both PMOS and NMOS are connected as

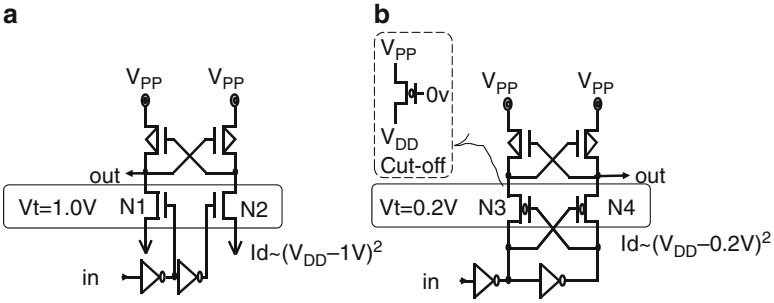


Fig. 4.30 CMOS high-level shifter with standard-Vt (**a**) and low-Vt (**b**) NMOS (Tanzawa et al. 2001)

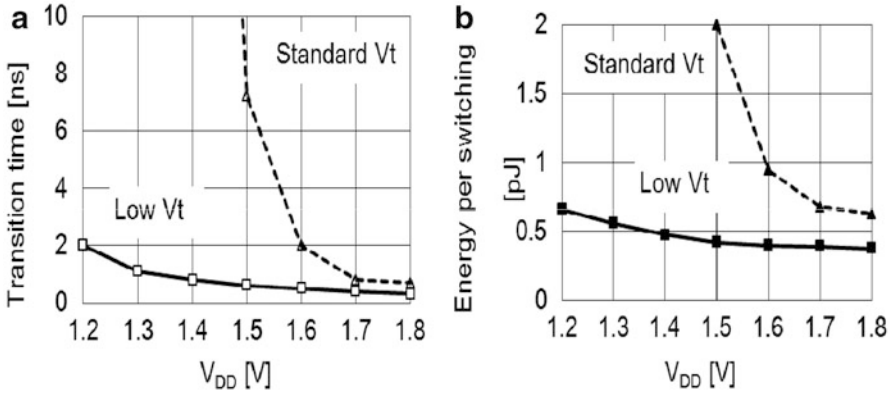


Fig. 4.31 VDD vs. switching time (**a**) and energy per switching (**b**) of the CMOS high-level shifters with standard-Vt and low-Vt NMOS (Tanzawa et al. 2001)

cross-coupled. When the NMOS needs to strongly turn on, the gate overdrive can be increased with lower Vt, resulting in lower V_{DD_MIN}, which has to meet (4.40).

Figure 4.31 shows simulation results for the switching time (a) and energy per switching (b) against V_{DD}. The low-V_{DD} high-voltage level shifter shows significant improvement in reduction in V_{DD_MIN} by about 0.5 V.

4.3.3 Depletion NMOS and Enhancement PMOS High-Level Shifter

Figure 4.32a shows another type of high-level shifter. When V_{IN} stays low, the pull down M3 forces the output node ground. M1 turns off with $V_S = |V_{tD}|$, where V_{tD} is the threshold voltage of M1, as far as M2 turns off with $V_S = |V_{tD}|$ and $V_G = V_{DD}$, as shown in Fig. 4.32b, resulting in (4.41). When V_{IN} goes high, M2 turns on as far

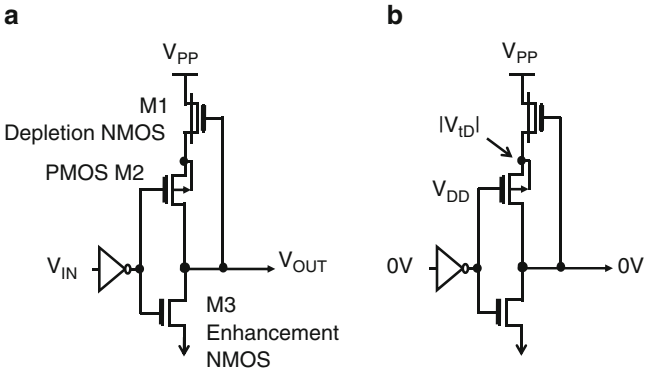


Fig. 4.32 Depletion NMOS (M1) and enhancement PMOS (M2) high-level shifter (Wada et al. 1989)

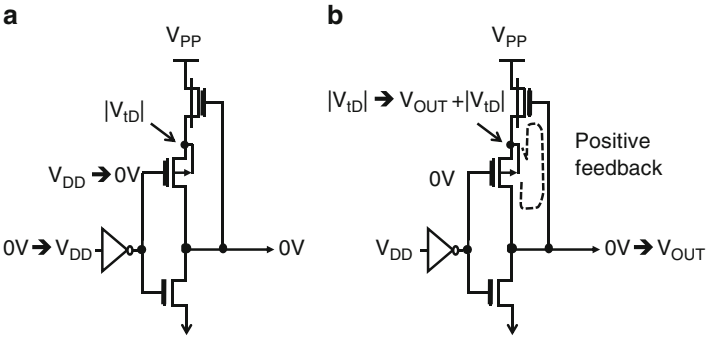


Fig. 4.33 Transient operation (Wada et al. 1989)

as $|V_{tP}|$ is lower than $|V_{tD}|$, as shown in Fig. 4.33a, resulting in (4.42). Theoretically, once the output terminal of the level shifter starts increasing, the loop composed of M1 and M2 becomes positive as shown in Fig. 4.33b. The positive feedback continues until $V_{tD}(V_{BS} = -V_{OUT})$ becomes 0 V.

Thus, it is necessary that $V_{tD}(V_{BS} = -V_{PP})$ is negative to make the level shifter functional up to V_{PP}, resulting in (4.43). Equations (4.41)–(4.43) define V_T window to make the level shifter functional under the condition where V_{DD} is given or V_{DDMIN} under the condition where V_T's are given.

$$|V_{tD}(V_{BS} = V_{tD})| - V_{DD} < |V_{tP}| \tag{4.41}$$

$$|V_{tP}| < |V_{tD}| \tag{4.42}$$

$$|V_{tD}(V_{BS} = -V_{PP})| < 0 \tag{4.43}$$

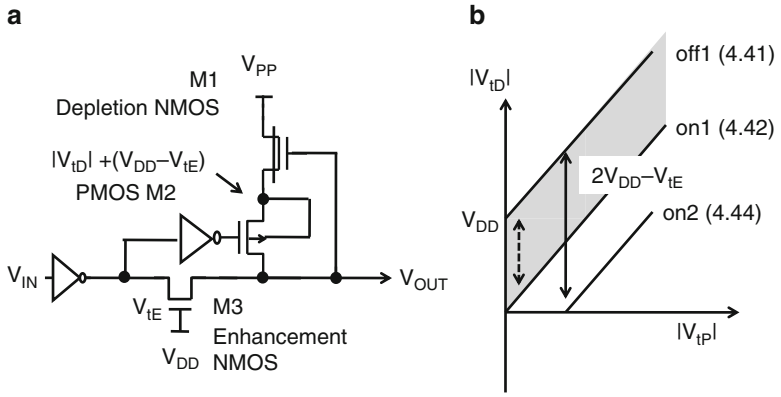


Fig. 4.34 Wider operation window D-NMOS + PMOS high-level shifter (Futatsuyama et al. 2009)

The requirement for V_{DS} of PMOS M2 is as low as $|V_{tD}|$, which can be much lower than V_{PP} in case of the CMOS level shifter. Therefore, the process cost may be lower than CMOS level shifter because of no need of specific junction process. Also, the high-voltage device counts can be smaller than CMOS level shifter.

To widen the V_T window or to reduce V_{DDMIN}, another circuit shown in Fig. 4.34a adds a precharge path to the depletion NMOS M1. Equation (4.42) is replaced with (4.44),

$$|V_{tP}|<V_{DD}-V_{tN}+|V_{tD}| \tag{4.44}$$

which is the initial condition where the PMOS becomes conductive. In case of $V_{tE} = 1$ V and $V_{DD} = 2$ V, the level shifter as shown in Fig. 4.34 relaxes the constraint for $|V_{tP}| - |V_{tD}|$ by 1 V. Figure 4.34b shows the V_T process window to have both the sufficient turn-on and cut-off conditions. The circuit of Fig. 4.32a has the V_T window between "off1" and "on1" whereas that of Fig. 4.34a has the V_T window between "off1" and "on2." Instead of widening the V_T window, one can reduce V_{DD}. Assuming that a margin of 2 V is needed between the *off* and *on* conditions, V_{DD_MIN} for the circuits of Fig. 4.32a and 4.34a has to be 2 V and 1.5 V, respectively, in case of $V_{tE} = 1$ V.

Figure 4.35a shows another high-level shifter with wider operation window. Additional depletion NMOS M4 is connected in parallel with M1, which boosts the source potential of the PMOS at the beginning of the operation. It has

$$|V_{tP}|<V_{DD}+|V_{tD}| \tag{4.45}$$

instead of (4.44). Figure 4.35b shows the window between "off1" and "on3." V_{DD_MIN} can be as low as 1 V under the same assumption as above.

Combining the level shifter of Fig. 4.34a with the regulator of Fig. 4.12, a high-voltage pass gate is obtained as shown in Fig. 4.36.

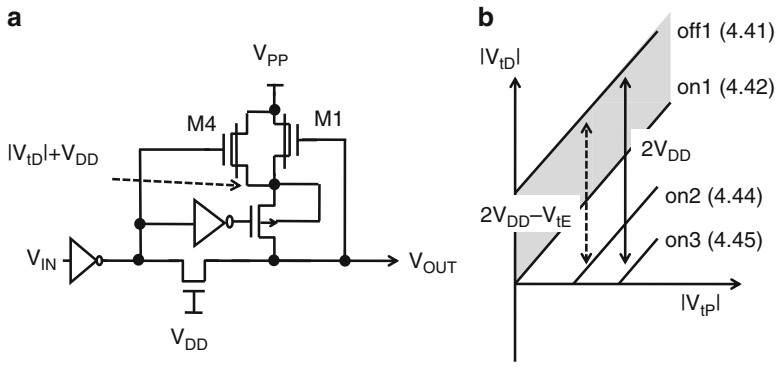


Fig. 4.35 Another wider operation window D-NMOS + PMOS high-level shifter (Tanzawa 2012)

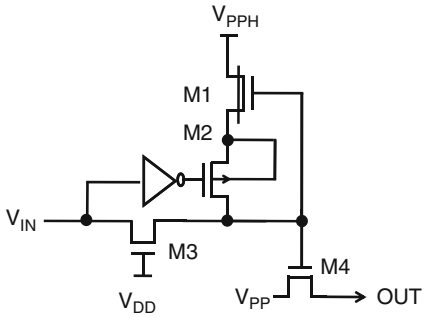


Fig. 4.36 High-voltage pass gate with V_{PPH} higher by V_{tE} than V_{PP}

Because V_{PPH} is higher by V_{tE} than V_{PP}, the pass gate can fully transfer V_{PP} with a minimal overdrive. The switching speed is determined by the output impedance of M4. When the pass gate M4 is disabled with V_{IN} low, the drain terminals of M1 and M4 are biased at the high voltages whereas the gate and source terminals are kept low. In this case, there is a gate edge stress from drain to gate. However, because the drain of HV NMOS is usually lightly doped, the voltage stress is low enough. All the terminals of the PMOS M2 are biased by low voltages as well. When the pass gate is enabled with V_{IN} high, all the terminals of M1 and M4 are biased by high voltages, but V_{GS} of M2 and M4 is much lower than the high voltages. On the other hand, the PMOS M2 is under a gate stress condition with the gate grounded and the source and drain biased with V_{PPH}. As a result, the HV oxide thickness is determined in a way that V_T of HV PMOS is not shifted by more than an acceptable amount due to such a Negative Bias Temperature Stability (NBTI) stress.

Figure 4.37 shows a level shifter with a relaxed gate stress. After transferring a part of V_{PP} to the output terminal, the gate of M2 is biased by V_{DD}, with the additional control signal/relax low. Even with an input of V_{DD} to the gate, M2 keeps on-state because the source and drain become high enough. Therefore, the gate oxide thickness

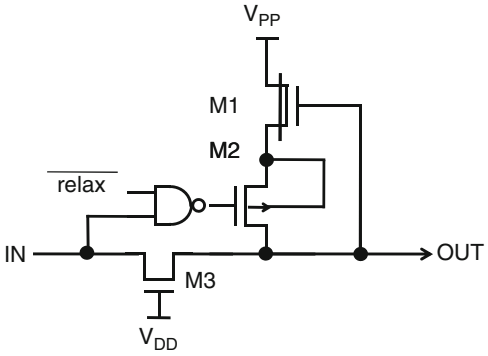


Fig. 4.37 Level shifter with a relaxed gate stress (Tanzawa 2010)

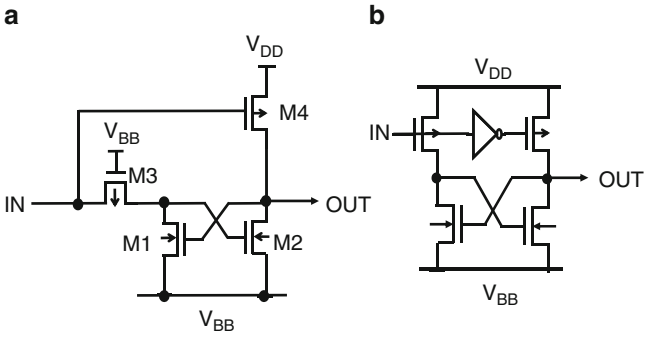


Fig. 4.38 CMOS low-level shifter

can be reduced by roughly $(V_{PP} - V_{DD})/V_{PP}$ to maintain the NBTI stress. The level shifter of Fig. 4.37 has one logic more than that of Fig. 4.34, but an increase in the area is limited because it only includes low voltage transistors. In addition, there is no timing overhead with the level shifter of Fig. 4.37 over that of Fig. 4.34, because the switching speed is limited by the impedance of the pass transistor such as M4 of Fig. 4.36. Thus, all the HV devices, including the HV capacitors, can be scaled by the ratio $(V_{PPH} - V_{DD})/V_{PPH}$ with Fig. 4.37 under the condition that the gate electric field is kept the same and the impact of the gate edge stress is still low enough with a thinner gate oxide.

4.3.4 CMOS Low-Level Shifter

Low-level shifter converts the low level of the input logic into a negative voltage whereas the high level is unchanged. The circuits of Fig. 4.38 input IN whose voltage amplitude is V_{DD} or GND and output OUT whose voltage amplitude is V_{DD}

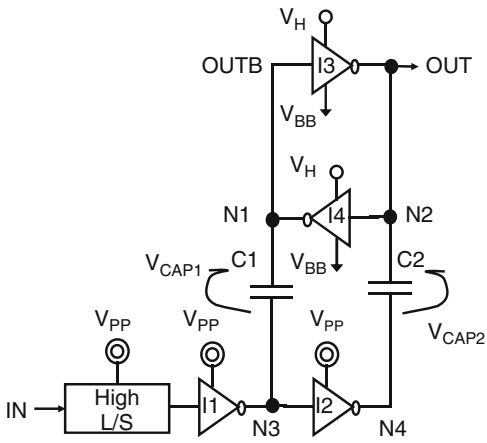


Fig. 4.39 CMOS low-level shifter using coupling capacitors (Tanzawa et al. 2002)

Table 4.2 Nodal voltages of the low-level shifter of Fig. 4.39 (Tanzawa et al. 2002)

	Initial	Transition	Final
N1	V_H	V_H–(V_{PP}–V_{SS})	V_{BB}
N2	V_{BB}	V_{BB}+(V_{PP}–V_{SS})	V_H
N3	V_{PP}	V_{SS}	V_{SS}
N4	V_{SS}	V_{PP}	V_{PP}
V_{CAP1}	$\lvert V_H - V_{PP}\rvert$	$\lvert V_H - V_{PP}\rvert$	$\lvert V_{SS} - V_{BB}\rvert$
V_{CAP2}	$\lvert V_{SS} - V_{BB}\rvert$	$\lvert V_{SS} - V_{BB}\rvert$	$\lvert V_H - V_{PP}\rvert$

or a negative voltage of V_{BB}. The topology is fully complementary to the CMOS high-level shifter of Fig. 4.26. Maximum voltage differences between two terminals of each transistor such as V_{GS}, V_{DS}, V_{DB}, and V_{SB} become $V_{DD} + |V_{BB}|$.

In case where $|V_{BB}|$ is close to V_{DD}, all the transistors except for the inverter are usually high-voltage ones whose gate oxide is thicker and whose channel length is longer than low-voltage transistors. In case where $|V_{BB}|$ becomes much larger than V_{DD}, the gate oxide needs to be much thicker. Under such a condition, reduction in V_{DD} is limited to make the PMOS strong enough to compulsorily invert the outputs. Thus, scaling the high-voltage transistor is a challenging item for the low-voltage level shifter.

To reduce the voltage for the logic high of the last stage of the low-level shifter, flipping and latching operations are separated using coupling capacitors, as shown in Fig. 4.39. The inverters *I1* and *I2* which, respectively, drive the nodes *N3* and *N4* can have sufficient driving currents to invert the latch via the coupling capacitors *C1* and *C2*. The operation voltages of the inverters are V_{PP} and V_{SS}, whereas those of the latches are V_H and V_{BB}. Table 4.2 shows the nodal voltages of the low-level shifter of Fig. 4.39.

In order to invert the latch, the condition (4.46) has to hold according to $V(N1) < V(N2)$ in the transition period.

$$V_H - V_{PP} + V_{SS} < V_{BB} + V_{PP} - V_{SS} \tag{4.46}$$

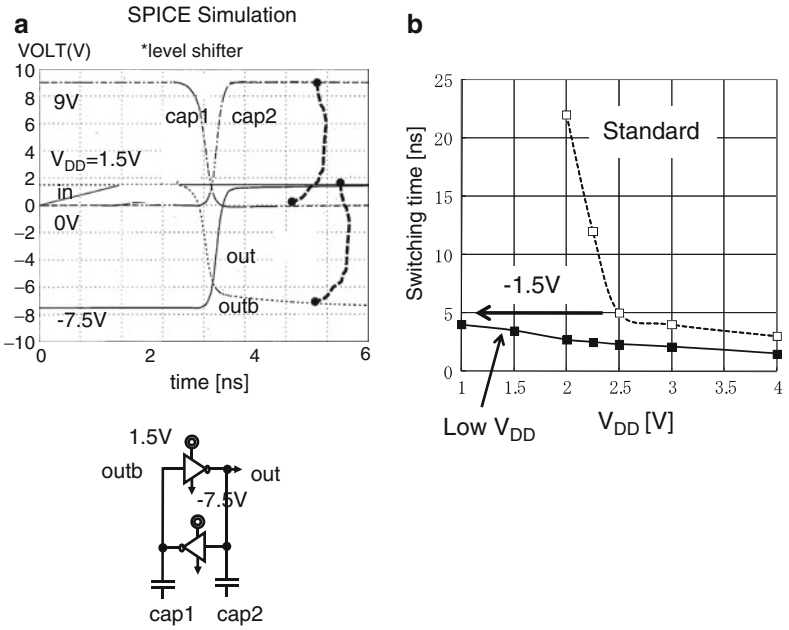


Fig. 4.40 Operation waveform (**a**) and V_{DD} vs. switching time (**b**) (Tanzawa et al. 2002)

In addition, because the capacitors have the gate oxide of the high-voltage transistors, the capacitor voltages V_{CAP1} and V_{CAP2} are equal to or less than V_{MAX}, resulting in the following conditions, respectively.

$$V_{PP} - V_H \leq V_{MAX} \tag{4.47}$$

$$V_{SS} - V_{BB} \leq V_{MAX} \tag{4.48}$$

Furthermore, the voltage difference between the logic high and low voltages of the inverters is also equal to or less than the maximum allowable voltage V_{MAX}.

$$V_{PP} - V_{SS} \leq V_{MAX} \tag{4.49}$$

Moreover, the transient voltages at the nodes $N1$ and $N2$ have to be between V_H and V_{BB}, otherwise the forward bias conditions occur. Thus, the condition should hold as follow.

$$V_{BB} \leq V_H - V_{PP} + V_{SS} \tag{4.50}$$

Figure 4.40a shows a simulation waveform of the circuit where $V_{PP} = 9$ V, $V_H = 1.5$ V, and $V_{BB} = -7.5$ V, which meet all the conditions of (4.46)–(4.50). The input has 0 V and 1.5 V as the two logic levels, which translate into 9 V via a high-voltage shifter. Then, the high amplitude cap1,2 shifts the voltage levels of out

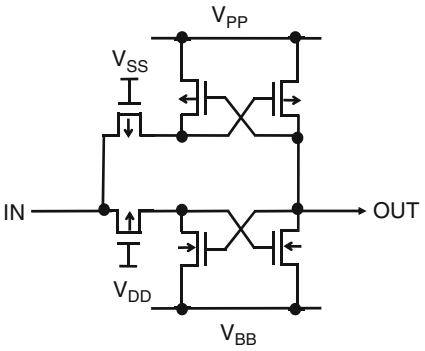


Fig. 4.41 CMOS level shifter with both high and low-level shifting (Yamagata et al. 1995)

Table 4.3 Summary: trade-offs between the level shifters

	High/Low	MOSFET	Switching speed	Power	Process cost	Circuit area	V_{DD_MIN}
1	High	NMOS	Slowest	Highest	Lowest	Large	High
2	High	CMOS	Fast	High	Highest	Small	Low/Mid
3	High	D-NMOS + PMOS	Slow	Low	High	Small	Mid
4	Low	CMOS	Fast	High	Highest	Small to Large	Low/Mid
5	High and Low	CMOS	Fast	High	Highest	Small	Low/Mid

and outb as shown without any overstress. Figure 4.40b shows the switching speed vs. V_{DD}. V_{DD_MIN} can be reduced by about 1.5 V.

In case where the high-voltage transistor is determined by another constraint, small circuit area can become the main concern to design the level shifter. Figure 4.41 has just six transistors to convert the voltage level from V_{DD} (V_{SS}) to V_{PP} (V_{BB}). Because the number of gate counts from IN to OUT is much less than the other types of level shifters, the switching delay can be the minimum with this structure.

Table 4.3 summarizes the trade-offs in switching speed, switching power, process cost, circuit area, and V_{DD_MIN}, among the level shifters discussed. When the applications need to design level shifters where the switching speed is critical, one would have to select a technology supporting high-voltage CMOS with well-controlled V_T's, even if that increases the process cost. On the other hand, when the switching speed is not a critical design parameter, one can select either NMOS or D-NMOS+PMOS level shifter depending on the total cost of the process and the die cost. If the level shifter does not affect the die size, the NMOS level shifter should have a lower total cost that the other one. Otherwise, the D-NMOS+PMOS level shifter can be the best choice. Requirement for controllability in V_T's of high-voltage depletion NMOS and high-voltage PMOS can be constraint on V_{DD_MIN}.

4.4 Voltage Reference

High-voltage generator needs to have a voltage reference to output an accurate high voltage. Bandgap reference outputs an accurate PVT insensitive voltage (Gray et al. 2001, Razavi 2000). Figure 4.42 shows the concept of bandgap reference. In (a), V_{BE} with a negative temperature coefficient is added with a thermal voltage $V_{\mathrm{T}} \equiv kT/q$ multiplied by a weight w.

$$V_{BGR} = V_{BE} + wV_T \tag{4.51}$$

Choosing an appropriate value for w in (4.51), one can have a PVT insensitive voltage as known as a bandgap voltage. In (b), two currents are summed with a single resistor R_1, resulting in another voltage reference.

$$V_{BGR} = (V_{BE} + wV_T)R_1/R_2 \tag{4.52}$$

In addition to w, one can choose another parameter R_1/R_2 to have a scaled bandgap voltage. Because R_1 and R_2 are made of same material, their ratio should have no temperature and process variations.

This section discusses deign equations, sensitivity on device mismatch, and the minimum operation voltage of four types of band-gap references: Kuijk cell, Brokaw cell, Meijer cell, and Banba cell.

4.4.1 Kuijk Cell

Figure 4.43 illustrates Kuijk cell composed of two diodes D1–2, three resistors R1–3, PMOS load, and one opamp. D2 has the junction area N times larger than D1.

$$I_1 = I_S \exp(V_{BE1}/V_T) \tag{4.53}$$

$$I_2 = NI_S \exp(V_{BE2}/V_T) \tag{4.54}$$

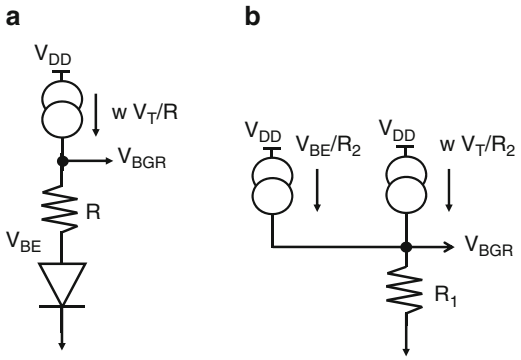


Fig. 4.42 Concept of Bandgap reference: voltage sum (Widlar 1970) (**a**) and current sum (Banba et al. 1998) (**b**)

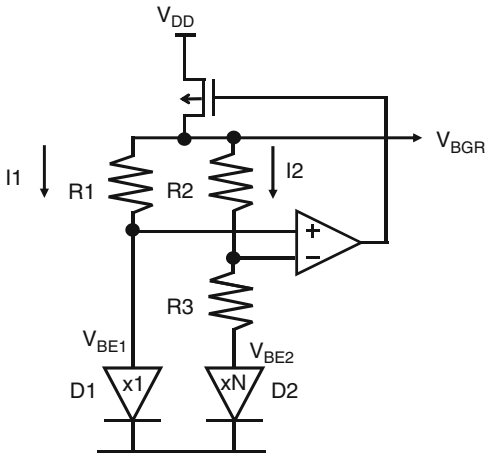


Fig. 4.43 Kuijk cell band-gap reference (Kuijk 1973)

From the fact that the two inputs of the opamp are equal,

$$R_1 I_1 = R_2 I_2 \tag{4.55}$$

Because the voltage at the upper terminal of $R3$ is given by V_{BE1} with the opamp,

$$V_{BE1} - V_{BE2} = R_3 I_2 \tag{4.56}$$

From (4.53) and (4.54),

$$I_2/I_1 = N \exp((V_{BE2} - V_{BE1})/V_T) \tag{4.57}$$

From (4.55) and (4.57),

$$V_{BE1} - V_{BE2} = V_T \ln(NR_2/R_1) \tag{4.58}$$

From (4.56) and (4.58),

$$I_2 = V_T \ln(NR_2/R_1)/R_3 \tag{4.59}$$

Therefore,

$$\begin{aligned} V_{BGR} &= V_{BE1} + R_2 I_2 \\ &= V_{BE1} + V_T R_2/R_3 \ln(NR_2/R_1) \end{aligned} \tag{4.60}$$

Assuming the ratios of R's have negligibly small temperature coefficient, the design equation to have zero temperature coefficient in V_{BGR} at T_0 to the first order is given by

$$R_2/R_3 \ln(NR_2/R_1) = -\frac{q}{k} \left. \frac{dV_{BE1}}{dT} \right|_{T=T_0} \equiv \alpha \tag{4.61}$$

Without losing generality, one can constrain the following additional equation.

$$R_1 = R_2 \tag{4.62}$$

(4.61) is then reduced to

$$R_2/R_3 = \alpha/\ln(N) \tag{4.63}$$

Next, the impact of mismatches on the reference voltage is considered as follows. In case where there is a finite input offset voltage V_{OS} of the opamp, it is assumed that the system is stable with $V_{\mathrm{BE1}} + V_{\mathrm{OS}}$ at the minus input of the opamp instead of V_{BE1} and $I_2 + \Delta I_2$ flowing through R_2 instead of I_2.

$$\Delta I_2 = V_{OS}/R_3 \tag{4.64}$$

The variation in V_{BGR} is given by

$$\Delta V_{BGR} = V_{OS} + R_2 \Delta I_2 = (1 + R_2/R_3)V_{OS} \tag{4.65}$$

From (4.65) and (4.63),

$$\Delta V_{BGR} = (1 + \alpha/\ln(N))V_{OS} \tag{4.66}$$

To reduce the variation in V_{BGR}, it is effective to have a large N. Deviation of V_{BGR}, δV_{BGR}, due to each one of the device parameters in (4.60) is expressed as follows.

$$\begin{aligned}\delta V_{BGR} = {} & \delta V_{BE1} + V_T[\delta R_2/R_3 \ln(NR_2/R_1) - \delta R_3 R_2/{R_3}^2 \ln(NR_2/R_1) \\ & + R_2/R_3(\delta N/N + \delta R_2/R_2 - \delta R_1/R_1)]\end{aligned} \tag{4.67a}$$

Assuming that there is no correlation between any two of the deviations in the device parameters, the standard deviation of V_{BGR}, σV_{BGR}, is calculated together with V_{OS}.

$$\begin{aligned}(\sigma V_{BGR})^2 = {} & (\sigma V_{BE1})^2 + {V_T}^2[(\sigma R_2)^2/{R_3}^2(\ln(NR_2/R_1))^2 \\ & + (\sigma R_3)^2 {R_2}^2/{R_3}^4(\ln(NR_2/R_1))^2 \\ & + {R_2}^2/{R_3}^2((\sigma N/N)^2 + (\sigma R_2/R_2)^2 + (\sigma R_1/R_1)^2)] \\ & + (1 + R_2/R_3)^2(\sigma V_{OS})^2\end{aligned} \tag{4.67b}$$

The minimum operating supply voltage is determined by either one of the load PMOS or the opamp. Assuming the opamp does not limit it, $V_{\mathrm{DD\_MIN}}$ is a sum of the output voltage and V_{DS} of the load PMOS, i.e.,

$$V_{DD\_MIN} = V_{BGR} + V_{DS} \tag{4.68}$$

which can be as low as about 1.5 V.

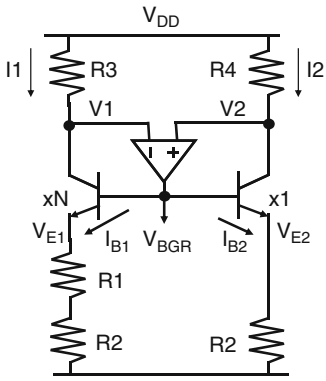


Fig. 4.44 Brokaw cell band-gap reference (Brokaw 1974)

4.4.2 *Brokaw Cell*

Figure 4.44 illustrates Brokaw cell composed of two NPN bipolar junction transistors (bjt's), four resistors R1–4, where the left bottom part is counted as one, and one opamp. From Fig. 4.44,

$$I_1 R_3 = I_2 R_4 \tag{4.69}$$

$$I_{B1} = I_1/\beta_1 = N I_S \exp(V_{BE1}/V_T) \tag{4.70}$$

$$I_{B2} = I_2/\beta_2 = I_S \exp(V_{BE2}/V_T) \tag{4.71}$$

where β_1 and β_2 are the multiplication factors of the collector currents to the base currents of the left- and right-hand side bjt, respectively, and N is the area ratio of the two bjt's. In the right-hand side branch,

$$V_{E2} = R_2 I_{b2}(\beta_2 + 1) \tag{4.72}$$

Since the difference between V_{BE1} and V_{BE2} appears at the voltage difference between both terminals of R_1,

$$V_{E1} - V_{E2} = V_{BE2} - V_{BE1} = R_1 I_{B1}(\beta_1 + 1) \tag{4.73}$$

From (4.69) to (4.71),

$$V_{BE2} - V_{BE1} = V_T \ln\left(N \frac{R_3}{R_4} \frac{\beta_1}{\beta_2}\right) \tag{4.74}$$

$$I_{B2} = I_{B1} \frac{R_3}{R_4} \frac{\beta_1}{\beta_2} \tag{4.75}$$

From (4.73) and (4.74),

$$I_{B1} = \frac{V_T \ln\left(N\frac{R_3}{R_4}\frac{\beta_1}{\beta_2}\right)}{R_1(\beta_1+1)} \tag{4.76}$$

Using (4.72), (4.75), and (4.76),

$$\begin{aligned} V_{BGR} &= V_{BE2} + V_{E2} = V_{BE2} + R_2 I_2 \\ &= V_{BE2} + V_T \frac{R_2}{R_1}\frac{R_3}{R_4}\frac{\beta_1(\beta_2+1)}{(\beta_1+1)\beta_2}\ln\left(N\frac{R_3}{R_4}\frac{\beta_1}{\beta_2}\right) \end{aligned} \tag{4.77a}$$

In case where $\beta_1 = \beta_2$, $R_3 = R_4$, (4.77a) is reduced to (4.77b).

$$V_{BGR} = V_{BE2} + \frac{R_2}{R_1} V_T \ln(N) \tag{4.77b}$$

Assuming the ratios of R's have negligibly small temperature coefficient, the design equation to have zero temperature coefficient in V_{BGR} at T_0 is given by

$$R_2/R_1 \ln(N) = -\frac{q}{k}\left.\frac{dV_{BE2}}{dT}\right|_{T=T_0} \equiv \alpha \tag{4.78}$$

Next, the impact of mismatches on the reference voltage is considered as follows. In case where there is a finite input offset voltage V_{OS} of the opamp, it is assumed that the system is stable with $V_2 - V_{\mathrm{OS}} + \Delta V_1$ at the plus input of the opamp instead of V_2, $V_1 + \Delta V_1$ at the minus input of the opamp instead of V_1, and $I_2 + \Delta I_2$ flowing through R_3 instead of I_2.

$$\Delta I_2 = V_{OS}/R_3 \tag{4.79}$$

Further assuming V_{BE2} varies by ΔV_{BE2} due to ΔI_2,

$$\Delta V_{BGR} = \Delta V_{BE2} = R_2 \Delta I_2 = V_{OS} R_2/R_3 \tag{4.80}$$

To reduce the variation in V_{BGR}, it is effective to increase the value for R_3, which is determined by $V_{\mathrm{DD\_MIN}}$.

$$V_{DD\_MIN} = V_{E2} + V_{CE2} + R_3 I_2 = V_{BGR} - V_{BE2} + V_{CE2} + R_3 I_2 \tag{4.81}$$

Using (4.77a, 4.77b) and (4.81), (4.80) is written by

$$\Delta V_{BGR} = V_{OS}\frac{V_{BGR} - V_{BE2}}{V_{DD\_MIN} - V_{BGR} + V_{BE2} - V_{CE2}}\frac{\beta_2}{\beta_2+1} \tag{4.82}$$

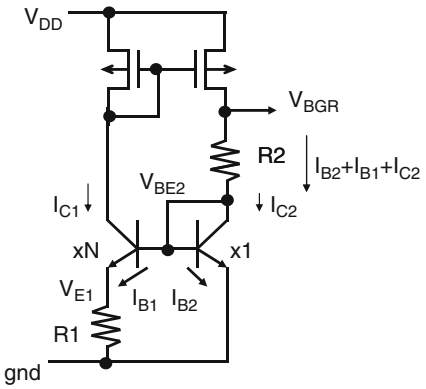


Fig. 4.45 Meijer cell band-gap reference (Meijer and Verhoeff 1976)

Even for a low supply voltage such as 1.5 V, the variation in V_{BGR} due to the input offset voltage could be close to the input offset voltage itself. (4.82) is typically much smaller than (4.66).

4.4.3 Meijer Cell

Figure 4.45 shows Meijer cell band-gap reference composed of two resistors, two bjt's, and two PMOS transistors.

$$I_{B1} = NI_S \exp((V_{BE2} - V_{E1})/V_T) \tag{4.83}$$

$$I_{B2} = I_S \exp(V_{BE2}/V_T) \tag{4.84}$$

$$V_{E1} = R_1(\beta + 1)I_{B1} \tag{4.85}$$

$$I_{C1} = \beta I_{B1} \tag{4.86}$$

$$I_{C2} = \beta I_{B2} \tag{4.87}$$

When two mirror PMOS are identical in size,

$$I_{C1} = I_{B2} + I_{B1} + I_{C2} \tag{4.88}$$

From (4.86) to (4.88),

$$I_{B2} = \frac{\beta - 1}{\beta + 1} I_{B1} \tag{4.89}$$

From (4.83), (4.84), and (4.89),

$$N \exp(-V_{E1}/V_T) = \frac{\beta + 1}{\beta - 1} \tag{4.90}$$

From (4.85) and (4.90),

$$I_{B1} = \frac{V_T \ln\left[N\frac{\beta-1}{\beta+1}\right]}{R_1(\beta+1)} \tag{4.91}$$

V_{BGR} is then

$$\begin{aligned} V_{BGR} &= V_{BE2} + R_2(I_{B2} + I_{B1} + I_{C2}) \\ &= V_{BE2} + \beta I_{B1} R_2 \\ &= V_{BE2} + \frac{R_2}{R_1} V_T \frac{\beta \ln[N(\beta-1)/(\beta+1)]}{\beta+1} \end{aligned} \tag{4.92}$$

In case where β is much larger than 1, (4.92) is reduced to

$$V_{BGR} = V_{BE2} + \frac{R_2}{R_1} V_T \ln N \tag{4.93}$$

Next, the impact of the mismatch in the mirror PMOS transistors' V_{t} on V_{BGR} is studied.

$$I_{C1} = K_P(V_{GS} - |V_t|)^2 \tag{4.94}$$

$$\Delta(I_{B1} + I_{B2} + I_{C2}) = 2\sqrt{K_P I_{C1}}\Delta V_t \tag{4.95a}$$

$$\begin{aligned} \Delta V_{BGR} &= R_2\Delta(I_{B1} + I_{B2} + I_{C2}) \\ &= 2R_2\sqrt{K_P I_{C1}}\Delta V_t \end{aligned} \tag{4.95b}$$

$V_{\mathrm{DD\_MIN}}$ is determined by either lower one of the left (4.96) or right (4.97) branch;

$$V_{DD\_MIN} = V_{E1} + V_{CE1} + V_{OD1} + |V|_t \tag{4.96}$$

$$V_{DD\_MIN} = V_{BGR} + V_{OD1} \tag{4.97}$$

where V_{CE1} is the collector-to-emitter voltage of the left BJT, and V_{OD1} is the overdrive voltage of the left PMOS.

4.4.4 Banba Cell

To reduce $V_{\mathrm{DD\_MIN}}$ for low voltage operation in advanced technology, another topology of bandgap reference with folded resistors is proposed as shown in

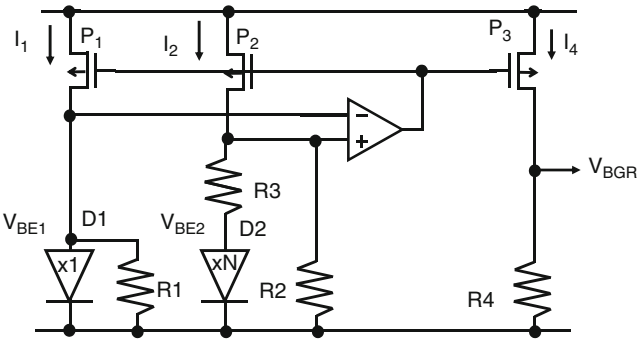


Fig. 4.46 Banba cell band-gap reference (Banba et al. 1998)

Fig. 4.46, which uses four resistors, two diodes, three load PMOS transistors, and one opamp. In the left and middle current paths,

$$I_1 = I_S \exp(V_{BE1}/V_T) + V_{BE1}/R_1 \tag{4.98}$$

$$I_2 = (V_{BE1} - V_{BE2})/R_3 + V_{BE1}/R_2 \tag{4.99}$$

(4.99) is extracted by using the fact that the two input nodes of the opamp are equal with the feedback loop. Because I_2 flows $R3$ and $D2$, the followings hold.

$$(V_{BE1} - V_{BE2})/R_3 = NI_S \exp(V_{BE2}/V_T) \tag{4.100}$$

$$V_{BGR} = I_4 R_4 \tag{4.101}$$

For simplicity, R_1 is equal to R_2 and the $P1$, $P2$, and $P3$ are identical in size. Then, from (4.98) to (4.100) and $I_1 = I_2 = I_4$,

$$V_{BE1} - V_{BE2} = V_T \ln N \tag{4.102}$$

From (4.99), (4.101), and (4.102),

$$\begin{aligned} V_{BGR} &= I_2 R_4 = R_4(V_T \ln N/R_3 + V_{BE1}/R_1) \\ &= \frac{R_4}{R_1}\left(V_{BE1} + \frac{R_1}{R_3} V_T \ln N\right) = \frac{R_4}{R_1} V_{BGR\_V} \end{aligned} \tag{4.103}$$

where V_{BGR_V} is a bandgap voltage generated by a type of bandgap references such as Kuijk, Brakow, and Meijer outputting a voltage sum.

Next, the case where the opamp has an input offset voltage of V_{OS} is considered. Assuming that the voltages at the positive and negative input nodes of the opamp are, respectively, shifted by $\Delta V_{BE1} + V_{OS}$ and ΔV_{BE1} due to V_{OS}, I_1 shifts by

Table 4.4 Comparisons in variations and minimum operation voltages

	Kuijk	Brokaw	Meijer	Banba
V_{DD_MIN}	V_{BGR} + V_{DS} ~ 1.5 V or $V_{DD\_MIN\_OPAMP}$			V_{BE} + V_{DS} ~ 1.0 V or $V_{DD\_MIN\_OPAMP}$
Sensitivity of VT mismatch (per 1 mV)	10 mV	2 mV	3 mV	10 mV
Sensitivity of β variation (10–100)	1 mV	1 mV	100 mV	1 mV
BJT or diode	Diode	BJT	BJT	Diode

$$\Delta I_1 = \Delta V_{BE1}/R_1 + \Delta I_{DIO} = \Delta V_{BE1}(1/R_1 + \ln N/R_3) \tag{4.104}$$

where the following relation is used.

$$\Delta I_{DIO} = \frac{I_S}{V_T}\exp(V_{BE1}/V_T)\Delta V_{BE1} = \ln N/R_3 \Delta V_{BE1} \tag{4.105}$$

Similarly, assuming the voltage at the lower node of $R3$ shifts by ΔV_{BE2}, I_2 shifts by

$$\Delta I_2 = (\Delta V_{BE1} + V_{OS})/R_2 + (\Delta V_{BE1} + V_{OS} - \Delta V_{BE2})/R_3 \tag{4.106}$$

From the fact that the current through $R3$ is same as that through $D2$,

$$(\Delta V_{BE1} + V_{OS} - \Delta V_{BE2})/R_3 = \Delta V_{BE2}\ln N/R_3 \tag{4.107}$$

Because the opamp controls the PMOSFETs in such as way that ΔI_1 is equal to ΔI_2, (4.104) and (4.106) lead to

$$\Delta V_{BE1} = V_{OS}\frac{\frac{R_3}{R_1} + 1 - \frac{1}{1+\ln N}}{\ln N - 1 + \frac{1}{1+\ln N}} \tag{4.108}$$

where (4.107) and the relation of $R1 = R2$ are used. The deviation in V_{BGR} is calculated by (4.101), (4.104), and (4.108) as follows:

$$\Delta V_{BGR} = \Delta I_1 R_4 = (1/R_1 + \ln N/R_3)\frac{\frac{R_3}{R_1} + 1 - \frac{1}{1+\ln N}}{\ln N - 1 + \frac{1}{1+\ln N}}V_{OS} \tag{4.109}$$

Table 4.4 summarizes characteristics of four bandgap cells. The values represent typical ones. If bjt is available in a given process, Brokaw cell would be the best among the four types of bandgaps in terms of low V_{DDMIN} and small variation, as far as the supply voltage given is higher than V_{DDMIN} of the bandgap cell. Otherwise, Banba cell would be the best one because it can have lower V_{DDMIN} than the others and similar variation as Kuijk cell does.

References:

General

Gray PR, Hurst PJ, Lewis SH, Meyer RG (2001) Analysis and design of analog integrated circuits. Wiley, New York. ISBN 0471321680

Razavi B (2000) Design of analog CMOS integrated circuits. McGraw-Hill, New York. ISBN 0072380322

Pump Regulator

Lucero EM, Challa N, Fields J (1983a) A 16 kbit smart 5 V-only EEPROM with redundancy. IEEE J Solid State Circuits 18(5):539–544

Mehrotra S, Wu TC, Chiu TL, Perlegos G (1984) A 64Kb CMOS EEROM with on-chip ECC. In: ISSCC, pp 142–143

Mihara M, Miyawaki Y, Ishizaki O, Hayasaka T, Kobayashi K, Omae T, Kimura H, Shimizu S, Makimoto H, Kawajiri Y, Wada N, Sonoyama H, Etoh J (1999) A 29mm^2 1.8 V-only 16 Mb DINOR flash memory with gate-protected poly-diode (GPPD) charge pump. In: IEEE international solid-state circuits conference, Feb 1999, pp 114–115

Oto DH, Dahm VK, Gudger KH, Reitsma MJ, Gongwer GS, Hu YW, Olund JF, Jones SJ Jr, Nieh STK (1983) High-voltage regulation and process consideration for high-density 5V-only E^{2}PROM's. IEEE J Solid State Circuits SC-18:532–537

Suh KD, Suh BH, Um YH, Kim JK, Choi YJ, Koh YN, Lee SS, Kwon SC, Choi BS, Yum JS, Choi JH, Kim JR, Lim HK (1995) A 3.3 V 32 Mb NAND flash memory with incremental step pulse programming scheme. In: ISSCC, pp 128–129

Tanaka S, Atsumi S, Momodomi M, Shinada K, Yoshikawa K, Nagakubo Y, Kanzaki K (1984) A programmable 256K CMOS EPROM with on-chip test circuits. In: ISSCC, pp 148–149

Tanzawa T, Harrington PB (2010) Adjustable voltage regulator for providing a regulated output voltage. US Patent 7764563

Venkatesh B, Chung M, Govindachar S, Santurkar V, Bill C, Gutala R, Zhou D, Yu J, Buskirk MV, Kawamura S, Kurihara K, Kawashima H, Watanabe H (1996) A 55ns 0.35μm 5V-only 16M flash memory with deep-power-down. In: IEEE international solid-state circuits conference, Feb 1996, pp 44–45

Oscillator

Cernea RA, Samachisa G, Su CS, Tsai HF, Kao YS, Wang CY, Chen YS, Renninger A, Wong T, Brennan J Jr, Haines J (1989) A 1 Mb flash EEPROM. In: IEEE international solid-state circuits conference, Feb 1989, pp 138–139

Tanzawa T, Tanaka T (1995) A stable programming pulse generator for high-speed programming single power supply voltage flash memories. In: IEEE symposium on VLSI circuits, June 1995, pp 73–74

Watanabe Y, Ohsawa T, Sakurai K, Furuyama T (1989) A new CR-delay circuit technology for high-density and high-speed DRAM's. IEEE J Solid State Circuits 24:905–910

Level Shifter

Dham V, Oto D, Gudger K, Congwer G, Hu Y, Olund J, Nieh S (1983) A 5V-only E2PROM using 1.5μ lithography. In: IEEE international solid-state circuits conference, Feb 1983, pp 166–167

Donaldson D, Honnigford E, Toth L (1983) +5V-only 32K EEPROM. In: IEEE international solid-state circuits conference, Feb 1983, pp 168–169

Futatsuyama T, Fujita N, Tokiwa N, Shindo Y, Edahiro T, Kamei T, Nasu H, Iwai M, Kato K, Fukuda Y, Kanagawa N, Abiko N, Matsumoto M, Himeno T, Hashimoto T, Liu YC, Chibvongodze H, Hori T, Sakai M, Ding H, Takeuchi Y, Shiga H, Kajimura N, Kajitani Y, Sakurai K, Yanagidaira K, Suzuki T, Namiki Y, Fujimura T, Mui M, Nguyen H, Lee SP, Mak A, Lutze J, Maruyama T, Watanabe T, Hara T, Ohshima S (2009) A 113mm^2 32Gb 3b/cell NAND flash memory. In: IEEE international solid-state circuits conference, Feb 2009, pp 242–243

Lucero EM, Challa N, Fields J (1983b) A 16 kbit smart 5 V-only EEPROM with redundancy. IEEE J Solid State Circuits 18(5):539–544

Mehrotra S, Wu TC, Chiu TL, Perlegos G (1984) A 64Kb CMOS EEROM with on-chip ECC. In: IEEE international solid-state circuits conference, Feb 1984, pp 142–143

Tanaka S, Atsumi S, Momodomi M, Shinada K, Yoshikawa K, Nagakubo Y, Kanzaki K (1984) A programmable 256K CMOS EPROM with on-chip test circuits. In: IEEE international solid-state circuits conference, Feb 1984, pp 148–149

Tanzawa T (2010) NBTI stress relaxation design for scaling high-voltage transistors in NAND Flash memories. In: IEEE international memory workshop, May 2010, pp 1–2

Tanzawa T (2012) Level shifting circuit. US Patent #8184489

Tanzawa T, Tanaka T, Takeuchi K, Nakamura H (1997) Circuit technologies for a single-1.8V flash memory. In: IEEE symposium on VLSI circuits, June 1997, pp 63–64

Tanzawa T, Umezawa A, Kuriyama M, Taura T, Banba H, Miyaba T, Shiga H, Takano Y, Atsumi S (2001) Wordline voltage generating system for low-power low-voltage flash memories. IEEE J Solid State Circuits 36(1):55–63

Tanzawa T, Takano Y, Watanabe K, Atsumi S (2002) High-voltage transistor scaling circuit techniques for high-density negative-gate channel-erasing NOR flash memories. IEEE J Solid State Circuits 37(10):1318–25

Wada Y, Maruyama T, Chida M, Takeda S, Shinada K, Sekiguchi K, Suzuki V, Kanzaki K, Wada M, Yoshizawa M (1989) A 1.7 volts operating CMOS 64K bit E^{2}PROM. In: IEEE symposium on VLSI circuits, June 1989, pp 41–42

Yamagata T, Tomishima S, Tsukude M, Tsuruda T, Hashizume Y, Arimoto K (1995) Low voltage circuit design techniques for battery-operated and/or giga-scale DRAMs. IEEE J Solid State Circuits 30(11):1183–1188

Bandgap Reference

Banba H, Shiga H, Umezawa A, Miyaba T, Tanzawa T, Atsumi S, Sakui K (1998) A CMOS bandgap reference circuit with sub 1 V operation. In: Symposium on VLSI circuits, pp 228–229

Brokaw A (1974) A simple three-terminal IC bandgap reference. In: IEEE international solid-state circuits conference, Feb 1974, pp 188–189

Kuijk KE (1973) A precision reference voltage source. IEEE J Solid State Circuits 8(3):222–226

Meijer GCM, Verhoeff JB (1976) An integrated bandgap reference. IEEE J Solid State Circuits 11(3):403–6

Widlar R (1970) New developments in IC voltage regulators. In: IEEE international solid-state circuits conference, Feb 1970, pp 158–159

Chapter 5
System Design

Abstract This chapter provides high voltage generator system design. A gate level hard switching pump model is first presented for designing a single pump block. Multiple pumps are distributed in a die, each of which has wide power ground bus lines. Total area including the charge pump circuits and the power bus lines needs to be paid attention for overall area reduction. Design methodology is shown using an example. Another concern on multiple high voltage generator system design is system level simulation time. Even though the switching pump models are used for system verification, simulation run time is still slow especially for Flash memory where the minimum clock period is 20–50 ns whereas the maximum erase operation period is 1–2 ms. In order to drastically reduce the simulation time, another charge pump model together with a regulator model is described which makes all the nodes in the regulation feedback loop analog to eliminate the hard-switching operation.

Figure 5.1 illustrates on-chip high-voltage generator system and summarizes key discussion in each section. Section 5.1 reviews a hard-switching pump model for designing a single pump cell. The pump outputs the current with an enabling signal high and disconnects the output terminal with the signal low. Thus, two logic states in the signal make the pump hardly turn on or off. The pump model can be implemented in a system together with its pump regulator for system simulation. Section 5.2 expands the model to allow the power line resistance to be included as a design parameter rather than a given condition. Thus, one can determine the power line width as well as the pump parameters such as the number of stages and the pump capacitor to minimize the entire area for the pump and the power lines. Section 5.3 then discusses a behavior model supporting to connect the power ground terminal of each pump with its local power ground lines. In case where power ground lines are shared with other pumps and with high power circuit blocks, there can be interference between one pump and the other blocks. Because lower voltage LSIs have larger sensitivity of power ground noises on performance in terms of speed and variation, the pump behavior model provides high quality on system design. Section 5.4 presents a soft-switching pump model working together with a pump regulator model to avoid a hard-switching for faster system simulation. The soft-switching

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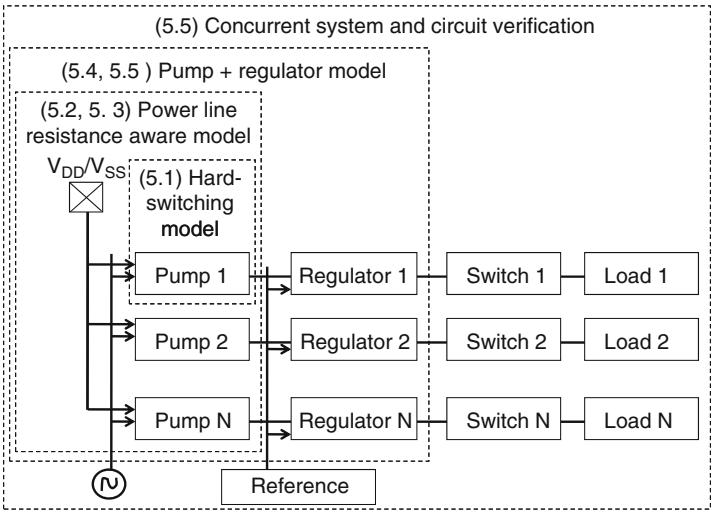

Fig. 5.1 System view and key discussion in each section

pump model includes I_{DD} calculation so that one can get the total I_{DD} waveform in entire simulation period. Section 5.5 presents system and circuit design and verification procedures using several models to meet the requirement for the system.

5.1 Hard-Switching Pump Model

Figure 5.2a shows a high-voltage generator composed of a charge pump circuit and a pump regulator. The regulator detects the output voltage of the pump, V_{PP}, to output a logical signal *flg* to the pump. When $V_{MON} < V_{REF}$, *flg* is high, where V_{MON} is a divided voltage and V_{REF} is a reference voltage, as shown in Fig. 5.2b. The charge pump outputs the current to the output terminal synchronizing with an input clock *clk_cp*. When $V_{MON} > V_{REF}$, *flg* is low to stop the clock *clk_cp*. Because the charge pump is operated with a fast continuous clock, *clk_cp*, which triggers multiple events to a simulator, it takes much time to simulate any system including a pump. A nominal clock frequency is 10 MHz to 1 GHz depending on the voltage conversion ratio or on the technology node.

To reduce the simulation time, especially for a voltage generator system, a modeled pump is used, as shown in Fig. 5.3a, where R_{PMP} is the effective output resistance of the pump as a function of the clock frequency, the number of stages, and the capacitance of the pump capacitor, C_{PMP} is the effective internal capacitance to be charged during the ramping period as a function of the number of stages, and the capacitance of the pump capacitor, V_{MAX} is the maximum attainable output voltage generated by the pump with no current load as a function of the voltage amplitude of the clock and the number of stages, and V_{SW} is a switching voltage to connect V_{MAX} to the output terminal via R_{PMP} and C_{PMP} with the enable signal

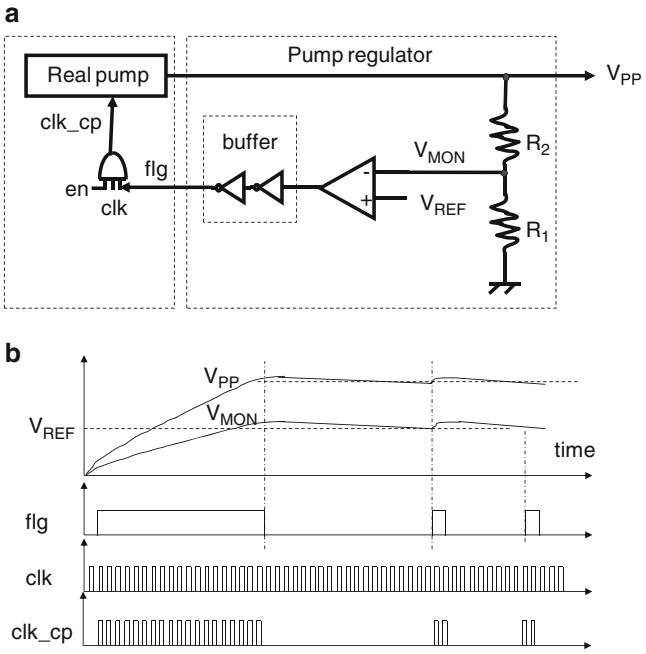

Fig. 5.2 Voltage generator composed of a pump and a pump regulator (Tanzawa (2012))

en high. The pump model is disconnected from the output terminal with en low. The level shifter used in the pump model can be a standard gate-level cell, as shown in Chap. 4. The global clock *clk* is forced to high when the model is used for system simulations. This allows to reduce the frequency of the clock *clk_cp* as low as that of *flg*, as shown in Fig. 5.3b. Even though the conventional pump model doesn't require the fast continuous clock, it still needs hard-switching to connect or to disconnect the voltage source to the load synchronized with the feedback signal *flg*. Figure 5.3c shows the relation between the output voltage and current. The current I_{REG} continuously flows in the resister divider whereas the current I_{OUT} discontinuously flows into the output terminal from the point p1 to p2 and vice versa. Thus, the simulation time is not fast enough to run the simulations for system-level verification.

5.2 Power Line Resistance Aware Pump Model for a Single Pump Cell

In this section, a finite resistance in power and ground lines is taken into account in the circuit analysis as shown in Fig. 5.4. When the effect of the resistance on the pump performance is low enough to treat it as a perturbation, the amplitude of the clocks, V_{DD}, can be replaced with V_{DD}–$2\Delta V_{DD}$, where ΔV_{DD} is the voltage drop

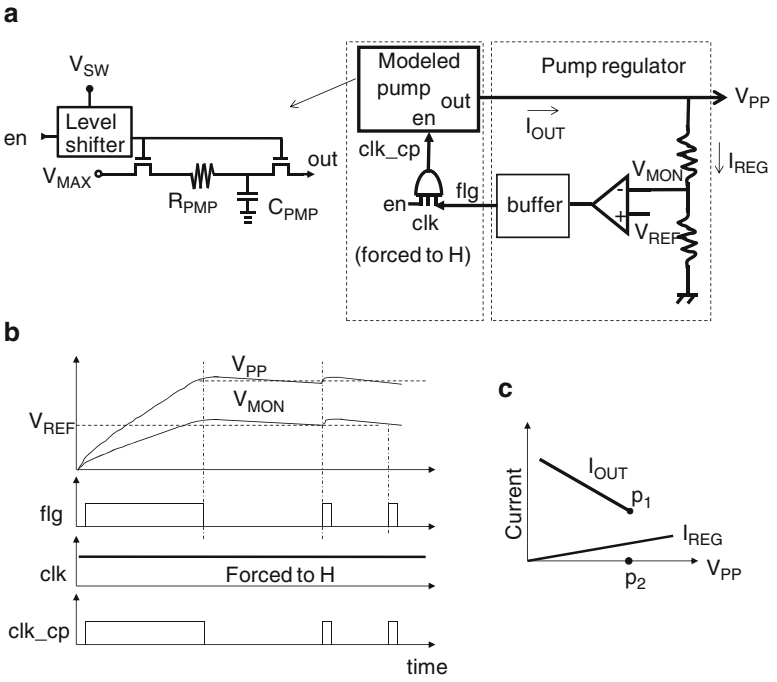

Fig. 5.3 Hard-switching pump model (Tanzawa (2012))

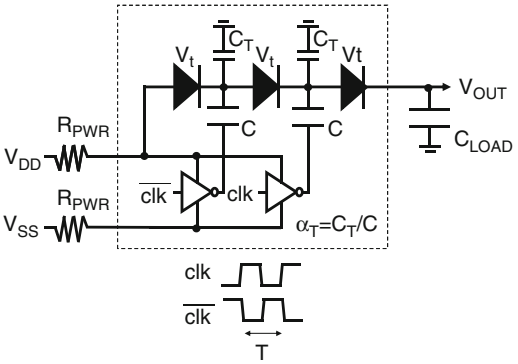

Fig. 5.4 Circuit including a pump with power line resistance

in V_{DD} line and is assumed to be same as that in ground line, resulting in a factor of 2. This voltage drop is originated from the power supply current I_{DD} and the wiring resistance R_{PWR}. Since the former is expressed by I_{OUT}/E_{FF}, where E_{FF} is the current efficiency of I_{OUT} to I_{DD}, ΔV_{DD} is expressed by $R_{PWR}I_{OUT}/E_{FF}$. Approximating a current efficiency in steady state E_{FF} with $1/(N + 1)$, the clock amplitude needs to be replaced with (5.1).

$$V_{\mathrm{DD}} \rightarrow V_{\mathrm{DD}} - 2R_{\mathrm{PWR}} I_{\mathrm{OUT}}(N+1) \tag{5.1}$$

Following the similar process in Sect. 5.2, the Dickson I-V equation and dynamic behavior of V_{OUT} are respectively modified by

$$I_{\mathrm{OUT}} = \left(1 + \frac{2C(N+1)R_{\mathrm{PWR}}}{NT}\right)^{-1} \frac{(1+\alpha_{\mathrm{T}})C}{NT} \times \left(N\left(\left(\frac{V_{\mathrm{DD}}}{1+\alpha_{\mathrm{T}}} - V_{\mathrm{T}}\right)\right) + (V_{\mathrm{DD}} - V_{\mathrm{T}}) - V_{\mathrm{OUT}}\right) \tag{5.2}$$

$$V_{\mathrm{OUT}}(j) = N\left(\frac{V_{\mathrm{DD}}}{1+\alpha_{\mathrm{T}}} - V_{\mathrm{T}}\right) + (V_{\mathrm{DD}} - V_{\mathrm{T}}) - N\left(\frac{V_{\mathrm{DD}}}{1+\alpha_{\mathrm{T}}} - V_{\mathrm{T}}\right)\gamma^{j} \tag{5.3}$$

where

$$\gamma = \left(1 + \frac{1}{1 + \frac{2C(N+1)R_{\mathrm{PWR}}}{T}} \frac{(1+\alpha_{\mathrm{T}})C}{NC_{\mathrm{T}}}\right)^{-1} \tag{5.4}$$

The rise time is modified by

$$T_{\mathrm{R}} = T \ln\left(1 - \frac{V_{\mathrm{PP}} - V_{\mathrm{DD}} + V_{\mathrm{T}}}{\frac{V_{\mathrm{DD}}}{1+\alpha_{\mathrm{T}}} - V_{\mathrm{T}}}\right) / \ln(\gamma) \tag{5.5}$$

(5.3) indicates that the equivalent circuit model parameters are respectively given by

$$V_{\mathrm{MAX}} = N\left(\frac{V_{\mathrm{DD}}}{1+\alpha_{\mathrm{T}}} - V_{\mathrm{T}}\right) + (V_{\mathrm{DD}} - V_{\mathrm{T}}) \tag{5.6}$$

$$R_{\mathrm{PMP}} = \frac{NT}{(1+\alpha_{\mathrm{T}})C_{\mathrm{EFF}}} \tag{5.7}$$

$$C_{\mathrm{EFF}} = C/\eta \tag{5.8}$$

$$\eta = 1 + \frac{2C(N+1)R_{\mathrm{PWR}}}{T} \tag{5.9}$$

$$C_{\mathrm{PMP}} = \frac{NC}{3}(1+\alpha_{\mathrm{T}}) \tag{5.10}$$

The difference in the parameters from those with no R_{PWR} is that the effective pump capacitor in R_{PMP} is reduced by a factor of η given by (5.9), resulting in an increase in R_{PMP}. On the other hand, V_{MAX} is unchanged from the case with no

Table 5.1 Design parameters of three pumps for model verification (Tanzawa (2009))

	N	C (pF)	V_{PP} (V)
Pump (a)	2	90	3.5
Pump (b)	5	17	6
Pump (c)	18	8	20

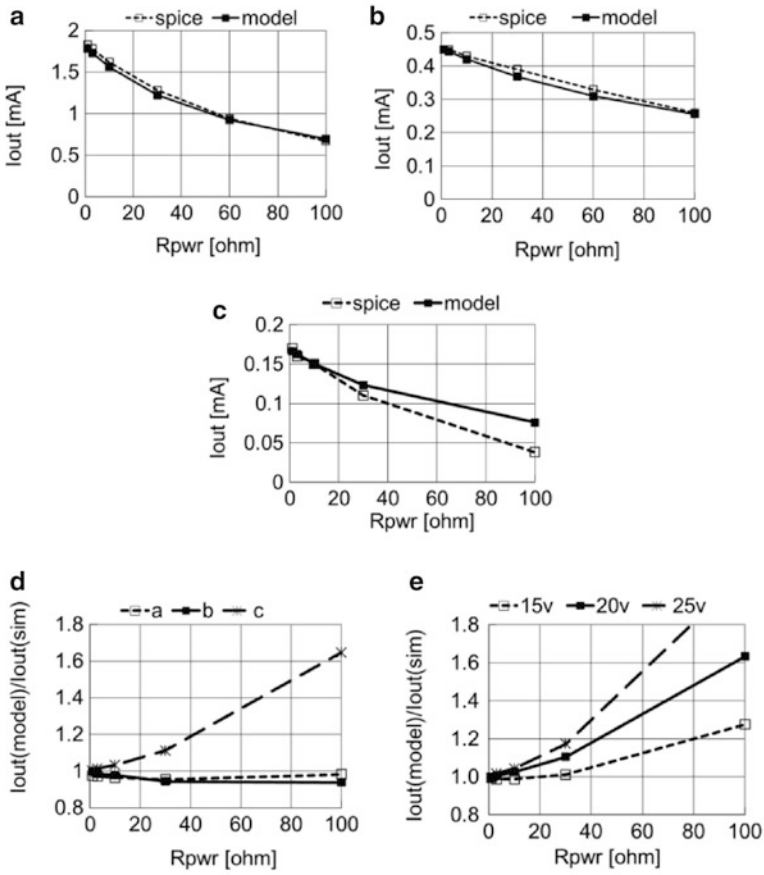

Fig. 5.5 Comparisons of the output current given by (Fig. 5.2) with the simulated results of three pumps (**a–c**) listed in Table 5.1. (**d**) Summary of the comparison results. (**e**) Errors in the output current of Pump (**c**) (Tanzawa (2009))

R_{PWR}. This means that an optimum capacitance per stage C_{OPT} needs to be increased as R_{PWR} is increased whereas an optimum number of stages N_{OPT} doesn't need to be increased no matter what optimization is done.

In order to verify the validity of the analysis, SPICE simulations for three different charge pumps shown in Table 5.1 were done under common conditions of $V_{DD} = 2.5$ V, $V_T = 0.35$ V, $\alpha_T = 0.05$, and $T = 50$ ns. Figure 5.5a–c show the comparisons of the output current given by (5.2) with the simulated results of three

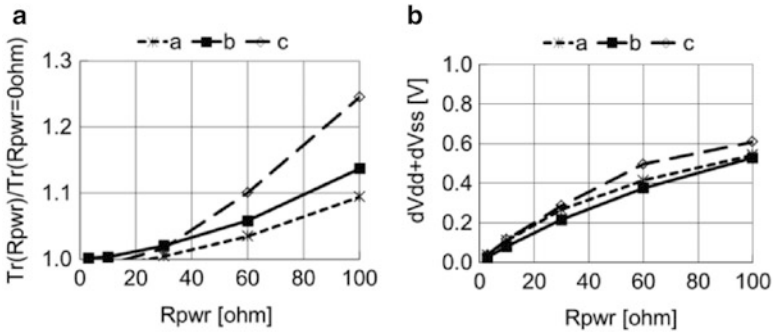

Fig. 5.6 Dependency of the rise time on R_{PWR} (**a**) and the voltage drop in the clock amplitude (**b**) under the same conditions as Fig. 5.5 (Tanzawa (2009))

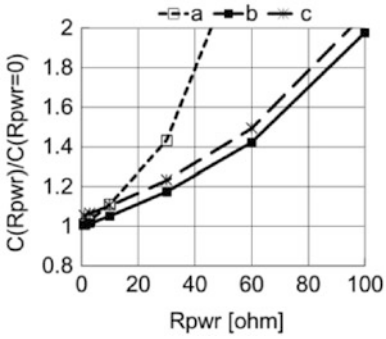

Fig. 5.7 Impact of R_{PWR} on C_{OPT} (Tanzawa (2009))

pumps listed in Table 5.1. Figure 5.5d summarizes the comparison results. Among the data points, Pump (c) with R_{PWR} of 100 Ω shows a large discrepancy between the simulated and calculated output currents. In order to investigate the discrepancy, the output current at V_{PP} of 15 and 25 V are additionally compared in Fig. 5.5e. As V_{PP} increases, the body effect of the pass transistors increases. In this case, V_T of the model needs to be increased accordingly, especially with high R_{PWR} or lower effective clock amplitude. This will determine the limitation to be able to apply the model.

Figure 5.6a illustrates the discrepancy between the calculated rise time with (5.5) and the simulated one. Figure 5.6b shows the average voltage drop of the clock amplitude. A discrepancy of 2–5% occurs at R_{PWR} of 40 Ω in Fig. 5.6a, where the voltage drop is 0.25 V or more in Fig. 5.6b. This indicates that the analysis made in this paper is in good agreement with the simulation, with less than 10% discrepancy as long as R_{PWR} drops the clock amplitude by 10% of V_{DD}.

Figure 5.7 shows the impact of R_{PWR} on C_{OPT}. As a factor $C(N + 1)$ increases, the increase rate η given by (5.9) also increases. In other words, one needs to design the charge pump circuits and/or the power line resistance so as to meet the

following equation, in order to ensure that the effect of R_{PWR} on the pump performance is negligibly small.

$$R_{PWR} \ll \frac{T}{2C(N+1)} \tag{5.11}$$

When the design violates (5.11), one needs to increase the pump capacitor by a factor of η given by (5.9) with the number of stages unchanged to meet the requirement for the design. This becomes more important especially in lower supply voltage LSIs because C and N tend to increase at lower V_{DD} conditions.

5.3 Pump Behavior Model for Multiple Pump System

This section discusses top-down charge pump circuit design with charge pump behavior models, including not only circuit parameters such as the number of stages, the capacitance per stage, and the supply voltage, but also the parasitic power wiring resistance as shown in Fig. 5.8. System designers can determine floor plan for replacement of individual charge pump, required power and ground width and length, and individual pump design parameters once the total area and power meet their design targets. Then, the charge pump circuit designers can start designing each pump with each design parameter determined.

In order to generalize the model for multiple charge pump circuits distributed in LSIs, one can start with the following equations;

$$V_{MAX} = (N/(1+\alpha_T)+1)(V_{DD\_LOCAL} - V_{SS\_LOCAL}) + V_{OS} \tag{5.12}$$

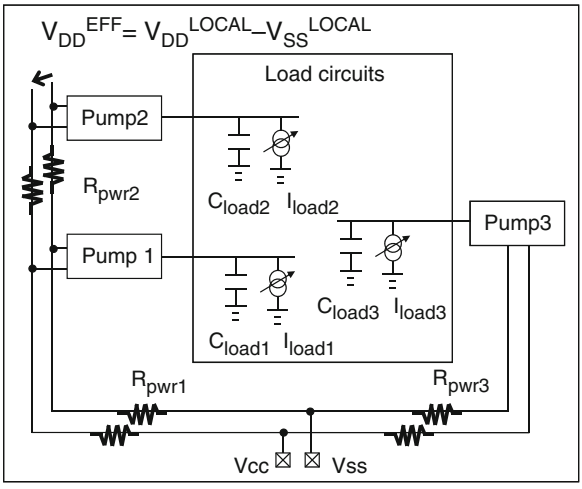

Fig. 5.8 LSI with distributed multiple charge pump circuits

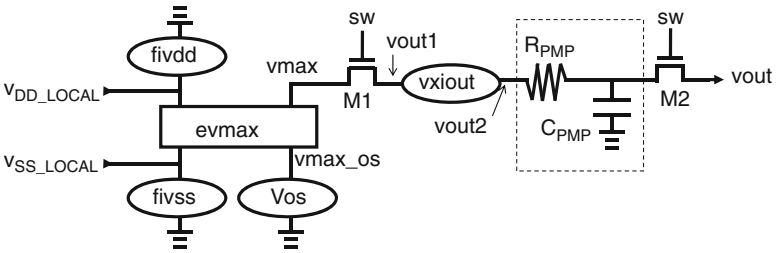

Fig. 5.9 Behavior model used in top-level design (Tanzawa (2010))

Table 5.2 Behavior model of the charge pump circuit (Tanzawa 2010)

Exvmax vmax vmax_os vdd_local vss_local $(N/(1+\alpha_T)+1)$
Fxivss gnd vss_local vxiout 1/eff
fxivcc vdd_local gnd vxiout 1/eff
vos vmax_os gnd dc $-(N+1)V_T$
vxiout vout0 vout dc 0V

$$V_{OS} = -(N+1)V_T \tag{5.13}$$

$$I_{DD} = I_{SS} = I_{OUT}/E_{FF} = (N+1)I_{OUT} \tag{5.14}$$

These equations are translated into a behavior model with several elements such as a voltage controlled voltage source (*exvmax*), current controlled current sources (*fxivcc*, *fxivss*), and voltage sources (*vos*, *vxiout*), as shown in Fig. 5.9 and in Table 5.2, where N, α_T, eff, and V_T are design parameters; respectively the number of stages, the ratio of the parasitic capacitance at the top plate to that of the pump capacitor, the current efficiency defined by the ratio of the output current to the input current, and the voltage drop via the switching diode. The voltage controlled voltage source, *exvmax*, represents the first term of (5.12) and the voltage sources, *vos*, represents the second term of (5.12). Also, the current controlled current sources, *fxivcc* and *fxivss*, and the voltage sources, *vxiout*, are related each other through (5.14). Thus, the input current, I_{DD} and I_{SS}, are calculated by monitoring the output current with *vxiout*. This behavior model is schematically expressed by each box described in Fig. 5.10.

The terminal sw of Fig. 5.9 is synchronized with an output of a regulator. The charge pump and the regulator are configured to be a feedback system to stabilize the output voltage of the pump. The switching elements M1, 2 should be so ideal that their channel resistance is much lower than an output resistance of R_{PMP}. Since every charge pump can be defined by its own behavior model, it is available in a system level simulation as shown in Fig. 5.10. When each of the terminals V_{DD_LOCAL} and V_{SS_LOCAL} is simply connected to the parasitic resistor network for power and ground lines, it is reduced to the original model. Thus, this behavior model includes the original one.

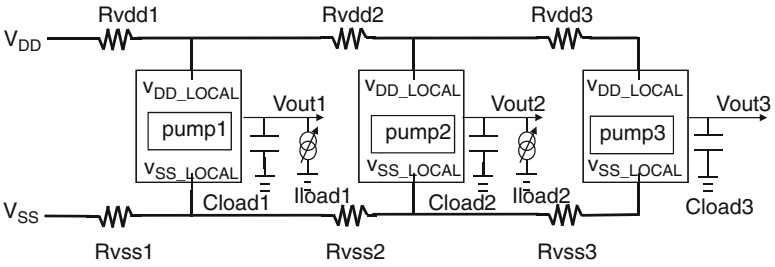

Fig. 5.10 Test bench for pump system (Tanzawa (2010))

In order to verify the behavior model and to see the impact of the common impedance of R_{PWR} on the circuit performance in the pump system described in Fig. 5.10, SPICE simulations were done together with the real pumps with gate level net list, as shown in Fig. 5.11.

The circuit parameters used in the simulations are shown in Table 5.3, where V_{MAX} is the maximum output voltage in case of no power and ground line resistance. V_{DD} and T are 2.5 V and 60 ns, respectively. Each pump is regulated so that $V_{OUT1\text{-}3}$ are stabled at 11.0, 3.3, and 7.8 V, respectively. Figure 5.11a shows the input load current waveforms. Figure 5.11b compares the modeled pumps with the real ones in the case where no power and ground wiring resistance is considered. The waveforms are in good agreement with an error of less than 3%. Figure 5.11c shows the comparison between the modeled and real pumps in the case where a finite power and ground wiring resistance is considered with the values shown in Table 5.3. Even though the simulated condition was so large that the local power and ground bounces were as high as about 0.45 V at the peak points, respectively, as shown in Fig. 5.11f, the rise time is in agreement within less than 10%. Figure 5.11d compares the waveforms between the cases with and without R_{PWR}. V_{OUT3} suffered most from the other pumps such as pump 1 and 2, which share all the power and ground lines. Figure 5.11e shows the local V_{DD} and V_{SS} at pump 3 using the real pump net list, which include high frequency components as fast as the clock frequency. The local power ground waveforms in case that the modeled pumps are used as shown in Fig. 5.11f behave filtering and averaging ones. Thus, the behavior model is shown to be accurate enough to reproduce the real pump behavior. In addition, the impact of the common impedance in power and ground lines on the pump performance was shown. The simulation time in case with the modeled pump system was reduced to less than 1/20 of that in case with the real one, in this example.

Assumed values of the worst-case V_{DD_LOCAL} and V_{SS_LOCAL} are conventionally given as the input parameters such as the clock frequency for designing individual charge pump circuits. However, since the system simulation, including all the charge pump circuits and power and ground wiring resistance, is impractical with respect to the simulation time, dynamic behavior of power and ground noises is hardly reflected to the pump performance. This kind of unknown sometimes results in over design or in larger circuit than necessary.

On the other hand, by using the behavior model, one can use the power ground resistance as parameters to minimize the total area for the power ground wirings and charge pump circuits. With the power and ground line resistance extracted from an initial floor plan for the voltage generator system and load conditions given, the initial solutions for the pump design parameters, such as the number of stages and capacitance per stage, are obtained. If the resultant total area and power don't meet the requirements, the power and ground line resistance has to be updated. Under the updated condition, the circuit parameters are reduced again and checked to be fulfilled with the target values for the total area and power. Thus, the feedback between floor plan and pump design is available to minimize the total area and power. After such a top-down procedure, an individual charge pump design can be started which takes the power and ground voltage drops due to the operation currents of itself and the rest of the circuits into consideration.

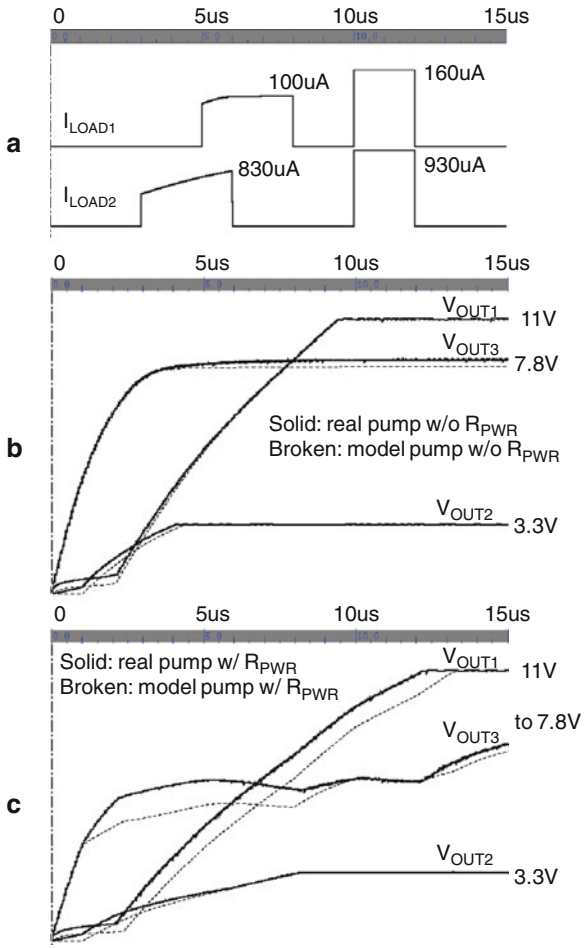

Fig. 5.11 Simulated waveform of real and modeled charge pumps with and without power ground line resistance (Tanzawa (2012))

Fig. 5.11 (continued)

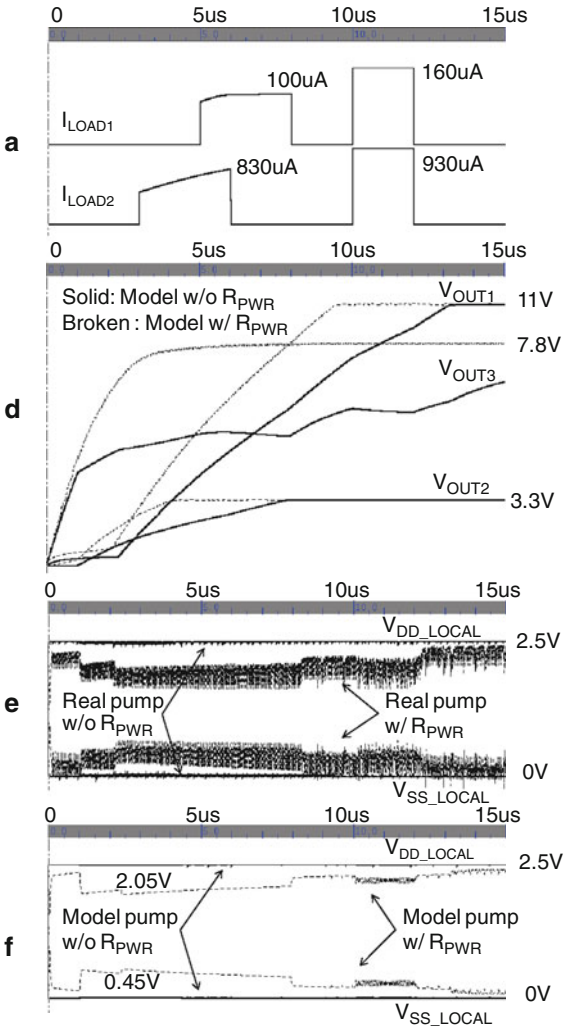

Table 5.3 Design parameters used for Fig. 5.10 (Tanzawa 2012)

	Pump1	Pump2	Pump3
N	12	2	5
C (pF)	50	150	25
α_T	0.05	0.05	0.05
V_T (V)	0.4	0	0.3
C_{LOAD}	500 pF	5 nF	10 pF
R_{VDD} (R_{VSS}) (Ω)	12	18	12
V_{MAX} (V)	36.6	7.3	13.8
R_{PMP}	13.7 kΩ	750 Ω	9.1 kΩ

5.4 Concurrent Pump and Regulator Models for Fast System Simulation

This section discusses modeling of the pump and the pump regulator to make the system simulation much faster than the pump models shown in Sects. 5.1 and 5.3.

Figure 5.12a illustrates models for pump and regulator. The voltage source V_{MAX} is connected to the resistor R_{PMP} via the current mirror. It is designed such that the output impedance is sufficiently small compared with R_{PMP} to keep the total impedance of the pump the same as the original model, i.e., to have I_{OUT1} in Fig. 5.12c as high as I_{OUT} in Fig. 5.3c.

In case that the open loop gain of the system is too high to make the pump plus regulator system unstable, a diode optionally needs to be added to reduce the gain, as shown in Fig. 5.12a, especially for a high-voltage generator system where the pole of the resister divider is not quite far from that of the pump with its load included. Thus, the AC performance of the opamp usually doesn't affect the stability of the entire system. One needs to make sure that the diode added doesn't affect I_{OUT1} especially at low output voltages, which could slightly increase the output impedance. Because the opamp is one of the circuit components which

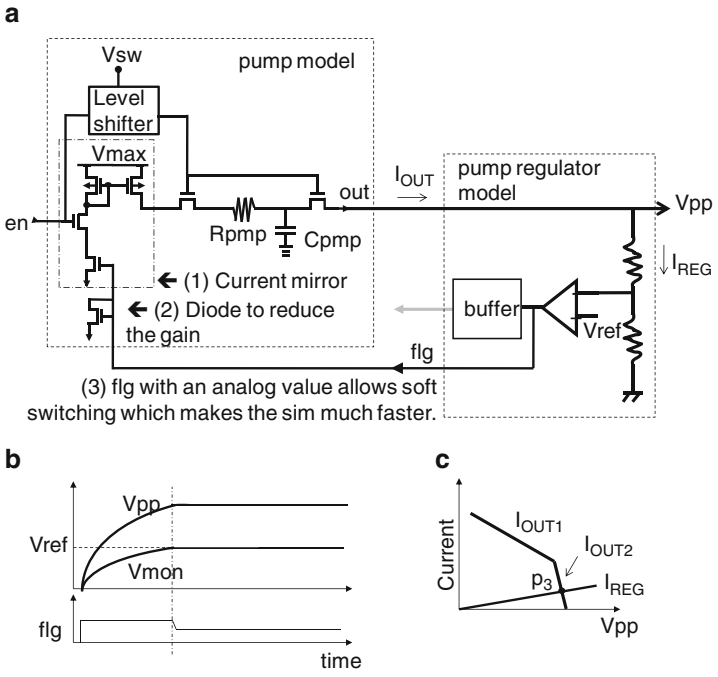

Fig. 5.12 Soft-switching pump and regulator models (Tanzawa (2012))

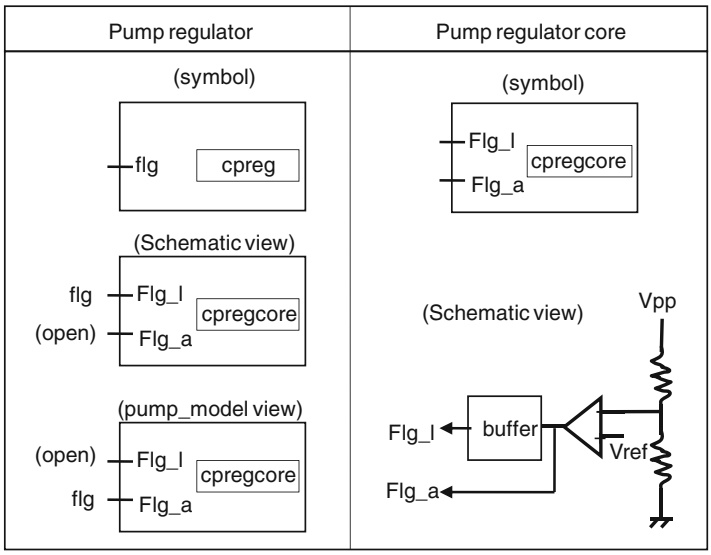

Fig. 5.13 Regulator model with *schematic* and *pump_model* views (Tanzawa (2012))

compose the entire regulator block and which cannot be changed in the model, it is only the current mirror and the diode optionally that can adjust the I-V characteristics as shown by I_{OUT1} and I_{OUT2} in Fig. 5.12c. In addition, the pump regulator is modeled to convert the logic signal *flg* to an analog one. This is done with a simple change of the terminal from the output of the buffer to that of the opamp. The buffer is required to transfer the signal with a small slew rate for a real circuit. But, it is not required for a simulation purpose in case that the wiring parasitic resistance and capacitance are not considered. Figure 5.12b shows how the feedback signal *flg* behaves. At the beginning of the operation, *flg* is higher than the level in a stable state to output the current from the pump. When V_{MON} gets close to V_{REF}, *flg* starts decreasing. *flg* becomes stable once the feedback system becomes stable unlike the conventional model. Figure 5.12c shows the regulation point P_3 at which the pump output current I_{OUT} is balanced with the regulator current I_{REG}. Thus, every node in the loop becomes analog so that hard-switching can be fully eliminated, resulting in much faster simulation time.

Figure 5.13 explains how the cell views for the regulator are implemented into the design. The pump regulator cell has two different cell views: schematic for physical design and *pump_model* for system simulation or verification. The output terminal *flg* is differently connected to an output terminal of the pump regulator core block *cpregcore*, which has two output terminals, *flg_l* and *flg_a*. Thus, *flg* is connected with *flg_l* for physical design to drive its heavy load and with *flg_a* for verification to make the feedback node analog. One can generate a gate level net list using the schematic view and a net list including the model using the *pump_model*. This approach enables us to use a single physical block for both physical design and

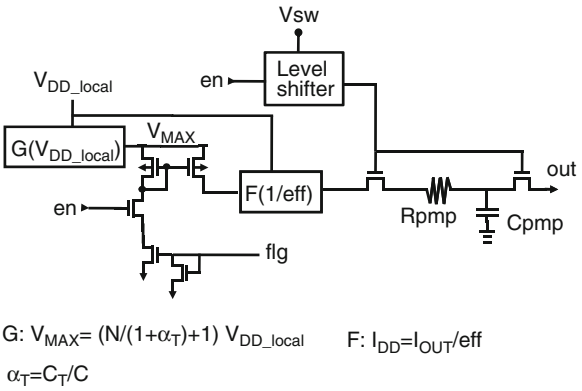

Fig. 5.14 Soft-switching pump model including I_{DD} calculation (Tanzawa (2012))

verification. Even though there is a design update in the pump regulator core, one doesn't need to update either the schematic or *pump_model* views of the pump regulator. Thus, this method has no risk of a potential mismatch between the real and model regulator. One drawback of the soft-switching pump model over the hard-switching pump model is that the soft-switching model doesn't reproduce any ripple in the output voltage unlike the real and hard-switching pump model pumps do. If concerns on the system-level simulations include the ripple, one needs to run some simulations with the hard-switching pump model additionally.

Another pump model is shown in Fig. 5.14 to take the impact of the power line resistance on the pump performance into account, which is represented by G and F. A voltage controlled voltage source G and a current controlled current source F are available in HSPICE and other simulators. These are combined into the pump model of Fig. 5.12, resulting in Fig. 5.14. V_{MAX} is actually a function of V_{DD_LOCAL}, the power supply for the pump, such as $V_{MAX} = (N/(1 + \alpha_T) + 1)$ V_{DD_LOCAL}, where N is the number of stages, α_T is the ratio of the parasitic capacitance at the top node of the pumping capacitor (C_T) to that of the pumping capacitor (C), and V_{DD_LOCAL} is the local power. Using the output current I_{OUT} and the current efficiency *eff*, the input current I_{DD} can be given by I_{OUT}/eff, as shown by F in Fig. 5.14. When the power line resistance is added to the local V_{DD} terminal for a system simulation, the IR drop in V_{DD_LOCAL} is reproduced self-consistently.

Figure 5.15 compares the V_{OUT}-I_{OUT} characteristics of a real pump and a model. Because the model shown in Fig. 5.14 includes the clock amplitude (V_{DD}) as an input parameter, the model can have the I-V curves close to the real ones under the wide V_{DD} operation conditions with an error of 5%.

Figure 5.16 shows Bode plots of the 18 V generator composed of the pump, regulator without (a) and with (b) a diode, and current load. Adding the diode, the generator system gets stable with a phase margin of 5° to 100°. Thus, the dimension of the diode can be adjusted according to the gain and output voltage range of the opamp given.

Figure 5.17 compares the waveforms for the output voltage V_{OUT} and the monitor nodal voltage V_{MON}. V_{OUT} is in good agreement each other, but V_{MON} is different.

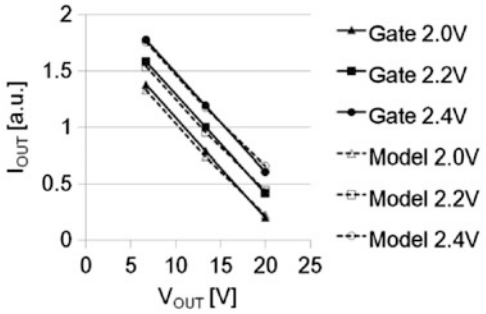

Fig. 5.15 Comparison of I-V curves between a modeled 18 V generator and a real one under various V_{DD} (Tanzawa (2012))

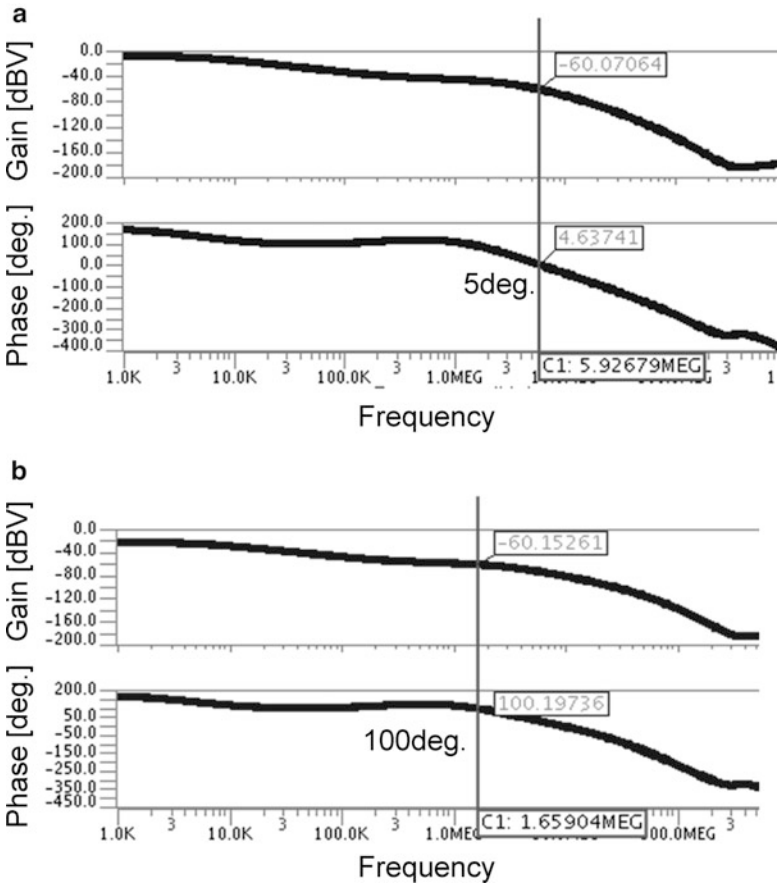

Fig. 5.16 Phase margin without (**a**) and with (**b**) a diode connected with *flg* node for the 18 V generator (Tanzawa (2012))

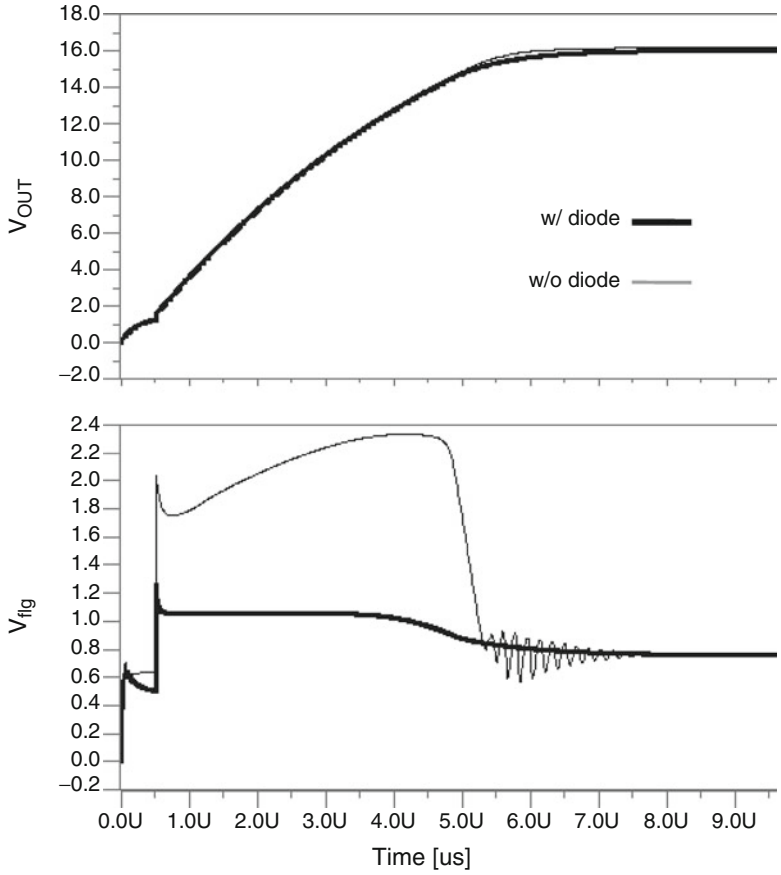

Fig. 5.17 Transient waveforms with and without the diode added to the modeled 18 V generator (Tanzawa (2012))

Because V_{MON} of the system with the diode added is much smoother than that without the diode, the former is considered to have less simulation time than the latter.

Figure 5.18 compares the waveform with a real pump and regulator with that with the modeled pump and regulator. Due to hard- and soft-switching operation with the real and modeled generator, the current waveform is sawtooth with the real one, whereas smooth with the modeled one. The generator is designed to output 18 V. The voltage waveform with the models is in good agreement with the real one in spite of the different current waveforms. The HSPICE run time with the modeled generator was 75 times shorter than that with the real one for a 10 μs transient simulation. At a sacrifice of the accuracy in high frequency components in I_{OUT} and I_{DD}, faster simulation was achieved with an error of 5% in V_{OUT}. As far as the voltage waveform is concerned, the accuracy seems to be enough. Note that

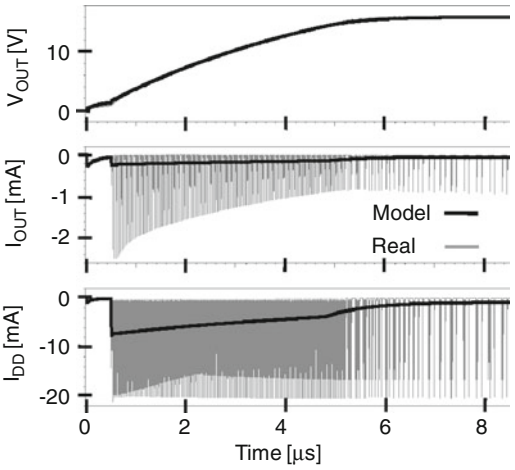

Fig. 5.18 Comparison of a modeled 18 V generator with a real one (Tanzawa (2012))

the reduction rate depends on the simulator used as well as the simulation net list and simulation period of time.

Figure 5.19 shows nine simulated waveforms of five output voltages generated by five pumps, $V_{PP1\text{-}5}$, and four regulated voltages regulated from the pump outputs, $V_{REG1\text{-}4}$, for a programming operation in 200 μs. The simulated net list includes not only voltage generators, but also switches and loads in NAND Flash memory. The number of devices in the net list is about 50 k. To validate the effectiveness of the models on the system-level simulation time, mixed-signal simulations were done.

Figure 5.20 compares the simulation time for the generator system with the number of devices at 30 k, which only includes the voltage generator, and the full-chip with the number of devices at 50 k between the cases with real generators, the hard-switching modeled ones, and the soft-switching ones. Regarding the voltage generator system, the hard-switching and soft-switching models reduced the simulation time by about 5 and 75, respectively, in comparison with the gate level net list. Regarding the full-chip, the soft-switching model reduced the simulation time by about 10 in comparison with the hard-switching model. The reduction rate depends on the simulation net list and simulation period of time, but in this example about $\times 10$ reduction in simulation time was realized with the soft-switching model compared with the hard-switching one.

5.5 System Design Methodology

Figure 5.21 shows a design flow for an on-chip high-voltage generator system. One has design requirements for the system such as the output current I_{OUT} or the rise time T_R for each voltage source and the total area and the peak and average operation current I_{DD} for entire voltage sources under the power line resistance R_{PWR} assumed (Step 1). Pump design parameters such as the clock period T, each

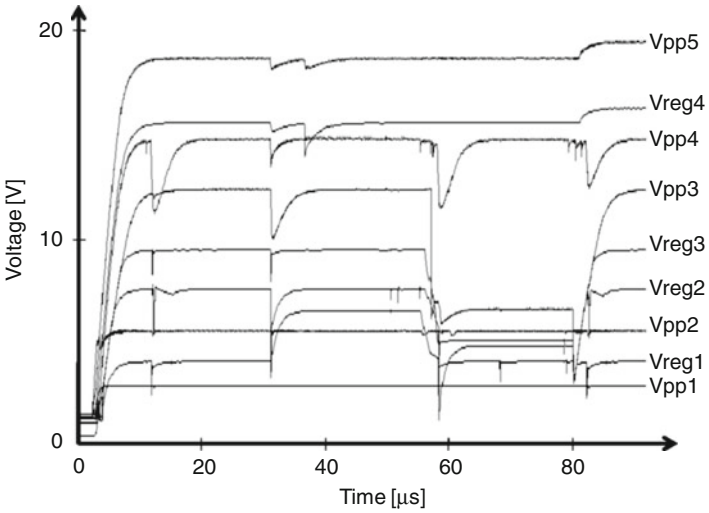

Fig. 5.19 Full-chip simulation waveforms (Tanzawa (2012))

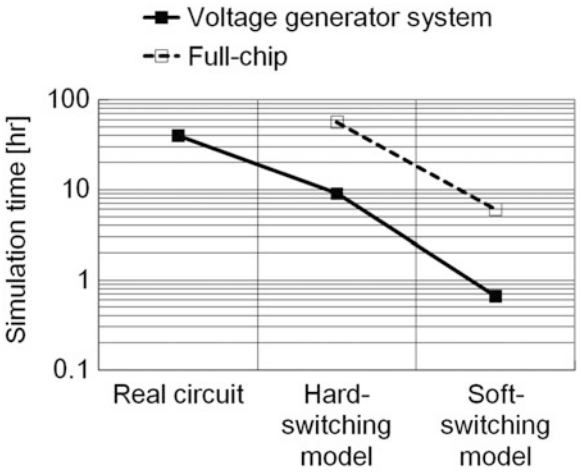

Fig. 5.20 Comparison in mixed-signal simulation time between real pumps; hard-switching models; and soft-switching models (Tanzawa (2012))

capacitor C, and the number of stages N are determined using the design formulas (Step 2). Figure 5.22 shows a flow in Step 2 of entire flow shown in Figure 5.21 in case where the power line resistance needs to be taken into consideration for low voltage ICs. In addition to the load conditions given by current, resistive, and capacitive load, the power line resistance is taken as a design parameter. Once the design parameters of the number of stages and the capacitance per stage is

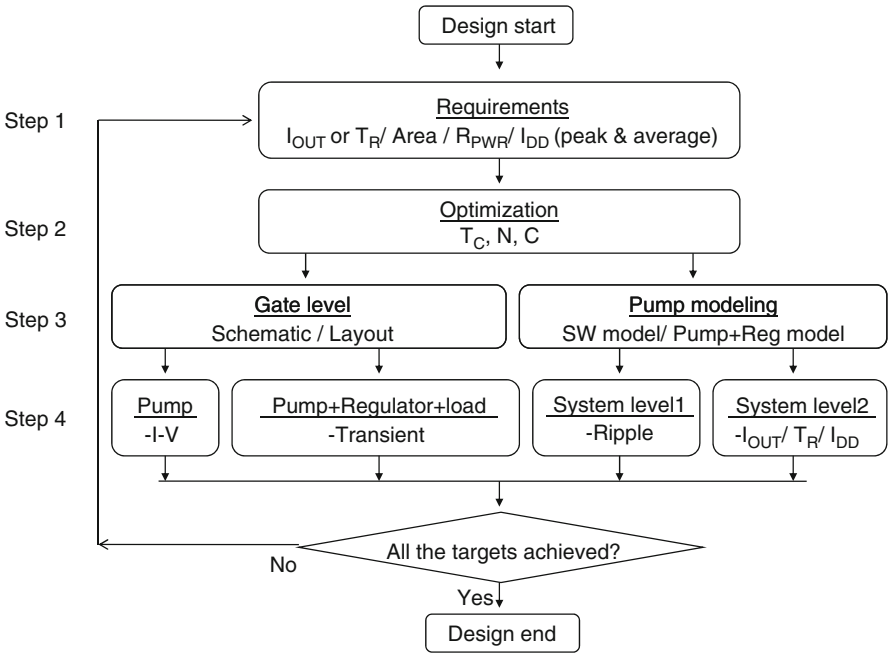

Fig. 5.21 Design and verification flow

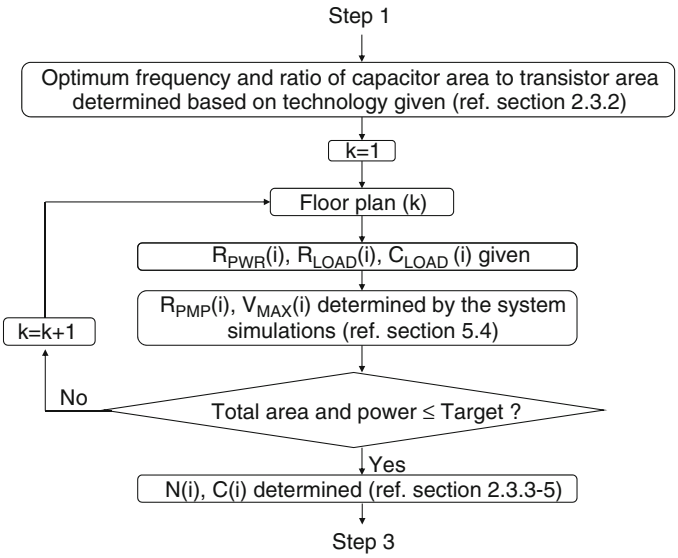

Fig. 5.22 Flow in Step 2 of Fig. 5.21 for an individual cell considering the power line resistance

determined per pump which entirely meet the area and power budget, one can proceed Step 3 of Fig. 5.21 to start physical design. At Step 3, gate level design is done with the schematic and layout for each pump and regulator. In parallel, the pumps are modeled as the hard-switching models (model 1) and the soft-switching ones (model 2). The gate level design is verified with respect to the pump I-V characteristic for each pump block and to the transient simulation for combination of each pump, regulator, and load. The system level design is verified with respect to the voltage ripple with model 1 and to the output current, the rise time, and the operation current with model 2 (Step 4).

When all the simulation results meet the original target, all the on-chip high-voltage system design and their component design are completed. Otherwise, one may need to update some of the original targets because there could be inconsistency between the design parameters. The verification categorized into "system level 2" conventionally takes more time than the rest in Step 4. Therefore, the soft-switching model can reduce the time for Step 4, resulting in faster entire design and verification periods.

References

Modeling

Tanzawa T (2009) Dickson charge pump circuit design with parasitic resistance in power lines. IEEE International Conference on Circuits and Systems, May 2009. pp 1763–1766

Tanzawa T (2010) A behavior model of a Dickson charge pump circuit for designing a multiple charge pump system distributed in LSIs. IEEE TCAS-II 57(7):527–530

Tanzawa T (2012) A Behavior Model of an On-Chip High Voltage Generator for Fast, System-Level Simulation, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 20, No. 12, pp. 2351–2355

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