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Wideband CMOS Receivers

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Miguel D. Fernandes • Luis B. Oliveira
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Editors
Miguel D. Fernandes
CTS-UNINOVA
Faculdade de Ciências e Tecnologia
Universidade Nova de Lisboa
Caparica, Portugal

Luis B. Oliveira
CTS-UNINOVA
Faculdade de Ciências e Tecnologia
Universidade Nova de Lisboa
Caparica, Portugal

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To the authors' families

Preface

Receivers that can operate in a wide range of frequencies are very desirable, due to the large number of available communication standards. Although it is possible to use multiple narrowband receivers, this configuration occupies a large area and, consequently, increases the chip cost. The solution is to employ a wideband receiver that can be easily programmable according to the system requirements. However, these receivers have many problems related to out-of-band interferers. The external filters that are usually employed at the receiver's input do not solve this problem, because they are not programmable and only work for specific frequencies, which makes it impossible to suppress all the unwanted signal components.

In this book, an overview of receiver architectures and RF blocks provides an introduction to the topic for the non-specialist. The RF key blocks: LNA and integrated filters are reviewed in depth and a general discussion of their key parameters: gain, noise and non-linearity is presented.

In modern CMOS receivers, two key problems are: (1) the use of a transformer balun at the input (to perform single-ended to differential conversion) and (2) the use of expensive and bulky external (for example: SAW—Surface Acoustic Wave) filters. In this book, we review the solutions in the literature that are used for single-ended to differential conversion using integrated balun LNAs in modern CMOS nanotechnologies; the LNA performs the conversion from single-ended to differential and has noise and distortion cancellation. In order to replace the SAW filters, high-Q BP filters based on a current-driven passive mixer have recently been proposed. In this book, an in-depth study of this type of complex filters is presented, with a detailed description of the impedance transformation involved (low-pass to band-pass).

With the solutions reviewed in this book, it is possible to obtain a wideband receiver, operating in current mode, in which the noise and non-linearity are reduced, in a low cost single chip, using standard CMOS technologies. Moreover, we present a solution to remove the transimpedance amplifier (TIA) block and connect directly the mixer's output to a passive second-order continuous-time $\Sigma\Delta$

analog to digital converter (ADC), which operates in current-mode, avoiding the use of unnecessary blocks at the analog front-end. The techniques that are reviewed in this book allow the design of a fully integrated receiver with low area. This is a low cost solution, which is useful, for example, for biomedical applications.

Caparica, Portugal Miguel D. Fernandes
Caparica, Portugal Luis B. Oliveira

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Contents

Acronyms

ADC	Analog-to-Digital Converter
AFE	Analog Front-end
BOM	Bill of Materials
BPF	Band-pass Filter
CB	Current-Buffer
CG	Common-Gate
CS	Common-Source
DFT	Discrete Fourier Transform
DVB-H	Digital Video Broadcasting—Handeld
FFT	Fast Fourier Transform
GSM	Global System for Mobile Communications
HPF	High-pass Filter
IB	In-band
IC	Integrated Circuit
IF	Intermediate Frequency
IM	Intermodulation
IP2	Second-order Intercept Point
IP3	Third-order Intercept Point
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low-pass Filter
NF	Noise Figure
OOB	Out-of-band
P1dB	1 dB Compression Point
PSD	Power Spectral Density
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
$\Sigma\Delta$	Sigma-delta
SNDR	Signal-to-noise and Distortion Ratio

SNR	Signal-to-noise Ratio
SDR	Software-defined Radio
SAW	Surface Acoustic Wave
SoC	System on Chip
TIA	Transimpedance Amplifier

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Chapter 1
Introduction

1.1 Background and Motivation

The use of wireless communications had a huge increase in the last years. These communications avoid the need of a physical connection between multiple devices, reducing the overall system cost and area occupation, which is a huge advantage comparing with traditional (wired) systems. Consequently, there is a large interest in creating compact and low power devices with low cost. Contrary to other technologies, the CMOS (Complementary Metal-Oxide-Semiconductor) technology allows the development of low cost and low power circuits that can operate at high frequencies. It also enables the circuit full integration on a single die (System on Chip (SoC)), thus, avoiding the need to match the various circuits' inputs and outputs, to allow the maximum power transfer between them, and avoiding the parasitic effects due to off-chip electrical connections at high frequencies [1, 2].

In this book the reader will learn modern techniques to implement Radio Frequency (RF) receivers using standard CMOS technologies. Moreover, this book provides guidelines to design the different receiver analog front-end blocks. In order to minimize interferers that can corrupt the desired receiver's input signal, with the possibility of saturating the LNA, new filtering techniques [3–6], based on current-driven passive mixers, have been recently employed. Since these filters are passive, they can be easily integrated in the receiver, avoiding the use of external filters that occupy a large area and have a high cost.

A wideband RF receiver, with integrated filtering that can be precisely controlled by the Local Oscillator (LO) frequency to attenuate out-of-band interferers, is analyzed in depth in this book. This receiver operates in current-mode, has small area, low power, and low cost and can be fully integrated in one chip. The key blocks of the receiver analog front-end are described. The Low-Noise Amplifier (LNA) is a widely tunable narrowband balun-LNA, which performs conversion from single-ended to differential, and has two integrated high-Q Band-pass Filters (BPFs) that filter undesired interferers at the receiver's input. This circuit is very compact and

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avoids the use of inductors and of an external balun, which occupies a large area. To convert the Intermediate Frequency (IF) current signal to the digital domain, avoiding the use of a Transimpedance Amplifier (TIA) that occupies large area and increases the receiver Noise Figure (NF), a current-mode Sigma-delta ($\Sigma\Delta$) Analog-to-Digital Converter (ADC) is directly connected to the mixer's output, thus reducing the cost of modern receivers built in standard CMOS nanotechnologies.

As an example that points to the design of future wideband receivers, we present in this book a complete wideband RF receiver (implemented in CMOS 130 nm and CMOS 65 nm technologies) that has the following main features:

- It uses integrated filters, which are desired in modern RF receivers, due to their simplicity, low area and low cost. Contrarily to traditional Surface Acoustic Wave (SAW) filters, these filters can be easily integrated in the receiver die and are very programmable, reducing the complexity of the receiver's input. The presented LNA-filters co-design has several advantages with respect to traditional approaches, since a narrowband balun-LNA that is tunable over the entire frequency band of the receiver is employed.
- The use of a TIA is avoided, at the output of the current-driven mixer, since a current-mode Sigma-delta ($\Sigma\Delta$) modulator is used to directly convert the IF signal to the digital domain, and thus the full receiver operates in current mode.

1.2 Book Organization

This book is organized in seven chapters, including this introduction, which is followed by

Chapter 2—Receiver Architectures and RF Blocks
This chapter introduces some basic concepts and definitions that are usually employed in a RF receiver. It also reviews the key receiver architectures, including the low-IF architecture, which is used later in this book.

Chapter 3—RF Blocks
This chapter presents an overview of the Key RF receiver blocks used in the front-end of a receiver (LNA, mixer, filters, oscillators, and ADC). The main characteristics of these key blocks are described in detail.

Chapter 4—Wideband Cascode Balun-LNA
The circuit studied in this chapter is a wideband cascode balun-LNA, which performs conversion from single-ended to differential. This circuit employs noise and distortion canceling techniques. To increase the voltage gain and reduce the NF, the traditional load resistors are replaced by active devices. The main purpose of the cascode stages is to allow the connection of a high-Q BPF, studied in Chap. 5. First, all the theoretical equations (input impedance, load impedance, voltage gain

and noise factor) of the LNA are derived and then the circuit is simulated using both CMOS 130 nm and CMOS 65 nm technologies. Finally, the circuits with the two technologies are compared.

Chapter 5—High-Q Bandpass Filter
In this chapter a high-Q BPF, based on a current-driven passive mixer, is reviewed. This filter performs an impedance transformation that allows to shift a baseband impedance to the RF (input) node, transforming a low-Q Low-pass Filter (LPF) into a high-Q BPF. The circuit is intended to attenuate interferers that are located outside the input signal band. This filter is developed in two versions, single-ended and differential, that will be employed in the LNA. First, the filter theoretical equations are derived in order to understand its behavior and then the circuits are simulated in order to validate the theory.

Chapter 6—Complete Receiver
In this chapter a complete RF receiver example is presented. First, the current-driven passive mixer, that also has filtering properties, is studied and then integrated in the full receiver, with an ideal TIA block connected to the mixer's output. Then, to avoid the use of a TIA, a new receiver architecture is presented. This receiver has a current-mode $\Sigma\Delta$ modulator connected to the mixer's output, to perform the direct conversion of the current IF signal to the digital domain. The interface between the mixer and the $\Sigma\Delta$ is made through a Current-Buffer (CB) that allows to amplify/attenuate the IF signal so that the $\Sigma\Delta$ can operate at maximum performance. All the circuits are validated through simulation.

Chapter 7—Conclusions
Finally, this chapter discusses the obtained results.

1.3 Main Contributions

Through this book the reader will learn techniques to implement modern RF receivers using standard CMOS technologies. This book provides guidelines to design the different receiver analog front-end blocks.

A current-mode receiver architecture, implemented on a single chip, is employed to overcome the problem created by interferers that can be located near the circuit's operating frequency. To achieve the interferers attenuation, a widely tunable narrowband balun-LNA with integrated filtering was designed, which consists of the LNA and the high-Q BPF of Chaps. 4 and 5, respectively. This avoids the use of external filters that increase the overall circuit cost and area. To convert the desired IF signal to the digital domain a current-mode $\Sigma\Delta$ modulator is used. The main advantages of this receiver are the interferers attenuation, the reduced number of blocks required in the AFE and its easy integration in one chip.

This work has originated a paper titled “A Widely Tunable Narrowband Balun-LNA with Integrated Filtering” [7], presented at 2014 Mixed Design of Integrated Circuits & Systems (MIXDES).

Chapter 2
Receiver Architectures

The main purpose of this chapter is to introduce basic concepts related with RF electronics and receiver architectures. The basic concepts are introduced and the advantages and disadvantages of different receiver architectures are described.

2.1 Basic Concepts

2.1.1 Impedance Matching

Lumped circuit analysis assumes that the physical dimensions of the network are much smaller than the electromagnetic wavelength and therefore the voltage and current do not vary significantly over the physical dimension of the elements. However, at high frequencies the network dimensions tends to be of the same order or even bigger than the wavelength (which is inverse to the frequency), and the voltage and current no longer remain spatially uniform over the network length so the transmission lines need to be treated as distributed parameter networks. A transmission line can be represented by an equivalent lumped circuit, as shown in Fig. 2.1, where R, L, G, and C are frequency-dependent parameters defined per unit length [8, 9]. The resistance R is related with the finite conductivity of the conductors, the inductance L represents the self-inductance of the wire and the mutual inductance between the two conductors, the capacitance C is due to the proximity of the two conductors and the conductance G is the electric loss in the material between the conductors.

Applying the Kirchhoff's Voltage Law (KVL) to the circuit of Fig. 2.1, and using cosine-based phasor notation for simplicity (considering steady-state sinusoidal regime), it is possible to conclude that

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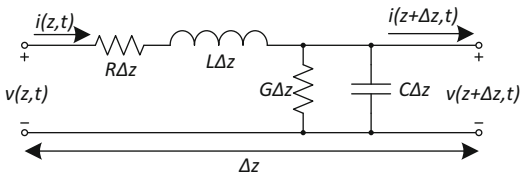


Fig. 2.1 Transmission line equivalent circuit representation

$$V(z) = (R + j\omega L)\, I(z)\, \Delta z + V(z + \Delta z) \tag{2.1}$$

and Kirchhoff's Current Law (KCL) leads to

$$I(z) = (G + j\omega C)\, V(z + \Delta z)\, \Delta z + I(z + \Delta z)\,. \tag{2.2}$$

Dividing Eqs. (2.1) and (2.2) by Δz and taking the limit as $\Delta z \to 0$ results in the following differential equations:

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{2.3}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \tag{2.4}$$

Deriving both terms of (2.3) and (2.4), and solving both equations simultaneously, the wave equations for $V(z)$ and $I(z)$ are given as follows:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{2.5}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0, \tag{2.6}$$

where

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.7}$$

is the complex propagation constant, which is frequency dependent. The solutions to these equations are two exponential functions for the voltage and for the current that are general solutions for transmission lines aligned along the z-axis, as shown in Fig. 2.1, at a specific point z [9]:

$$V(z) = V_o^+ e^{-\gamma z} + V_o^- e^{\gamma z} \tag{2.8}$$

$$I(z) = I_o^+ e^{-\gamma z} + I_o^- e^{\gamma z}, \tag{2.9}$$

where V_o^+ and I_o^+ are, respectively, the voltage and current amplitudes of the incident waves and V_o^- and I_o^- are the voltage and current amplitudes of the reflected

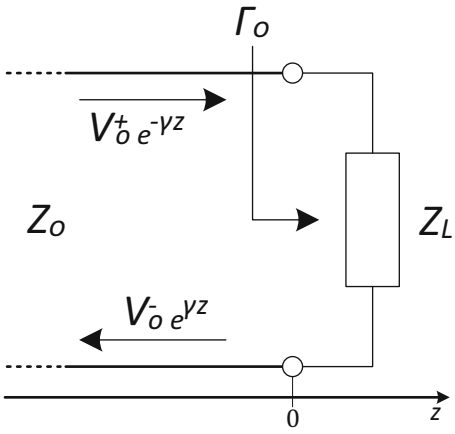


Fig. 2.2 Transmission line terminated in an arbitrary load impedance Z_L

waves. The term $e^{-\gamma z}$ represents the wave propagation in the $+z$ direction and the $e^{\gamma z}$ in the $-z$ direction. Deriving (2.8) and applying to the voltage of (2.3), the current on the line is given by

$$I(z) = \frac{\gamma}{R + j\omega L}\left(V_o^+ e^{-\gamma z} - V_o^- e^{\gamma z}\right). \tag{2.10}$$

Comparing the previous equation with (2.9) shows that the transmission line characteristic impedance Z_0 can be defined as

$$Z_0 = \frac{V_o^+}{I_o^+} = -\frac{V_o^-}{I_o^-} = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}. \tag{2.11}$$

Assuming an arbitrary load impedance Z_L located at $z = 0$, as shown in Fig. 2.2, and that an incident waveform is generated from a source at $z < 0$, from (2.8) and (2.10) is possible to define Z_L as

$$Z_L = \frac{V(0)}{I(0)} = \frac{V_o^+ + V_o^-}{V_o^+ - V_o^-} Z_0. \tag{2.12}$$

Solving the previous equation in order to V_o^-/V_o^+ shows that the voltage reflection coefficient Γ, which is the amplitude of the reflected voltage wave normalized to the amplitude of the incident voltage wave, is given by

$$\Gamma = \frac{V_o^-}{V_o^+} = \frac{Z_L - Z_0}{Z_L + Z_0}. \tag{2.13}$$

Since the time-average power that flows along a transmission line is given by Pozar [9]

$$P_{avg} = \frac{1}{2}\frac{|V_o^+|^2}{Z_0}\left(1 - |\Gamma|^2\right), \tag{2.14}$$

to achieve the maximum power transfer to the load there should not exist reflected wave in order to obtain $\Gamma = 0$, so the load impedance must be matched to the characteristic impedance of the transmission line ($Z_L = Z_0$), as stated in (2.13). RF antennas usually have an impedance of 50 Ω and consequently the first block of a receiver AFE (commonly a LNA) implemented in an Integrated Circuit (IC) must have its input impedance matched to 50 Ω. This matching can be achieved by using the transistors transconductance, as will be shown further below, or using reactive elements that are problematic due to their area occupation and bandwidth limitation. The receiver's internal blocks do not need to be matched because the distance between those blocks is so tiny that the electromagnetic wavelength is much higher than the circuit dimensions.

2.1.2 Scattering Parameters

Due to the difficulties of measuring voltage and current in an RF circuit, since these measurements usually involve the magnitude and phase of traveling or standing waves, the circuit measurements are made using the average power instead of the traditional open-circuit or short-circuit measurements [8]. The scattering parameters (S-parameters) are parameters that can be obtained through those power measurements in order to describe the network. Considering a two-port network, as shown in Fig. 2.3, with the input and output incident waves V_1^+ and V_2^+, and the corresponding reflected waves V_1^- and V_2^-, the input and output reflected waves voltages are given by Razavi [1]

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \tag{2.15}$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+, \tag{2.16}$$

where S_{mn} are the S-parameters.

Fig. 2.3 Incident and reflected waves in a two-port network

- S_{11} is the input reflection coefficient and represents the accuracy of the input matching. This parameter is the ratio of the reflected and incident waves at the input port when there is no incident wave at the output port:

$$S_{11} = \frac{V_1^-}{V_1^+}_{|V_2^+=0}$$

  If the network's input is completely adapted there is no reflected wave at the input (V_1^-) and consequently $S_{11} = 0$. Usually a $S_{11} < -10\,\text{dB}$ means that the input of the circuit is correctly matched.
- S_{12} is known as reverse voltage gain and characterizes the "reverse isolation" of the circuit. This parameter is the ratio of the reflected wave at the input port and the incident wave into the output port when the input port is matched:

$$S_{12} = \frac{V_1^-}{V_2^+}_{|V_1^+=0}$$

- S_{21} is the forward voltage gain of the network and represents the voltage gain of the circuit, as expected. This parameter is the ratio between the reflected wave at the output port and the incident wave at the input port, when the incident wave at the output is zero:

$$S_{21} = \frac{V_2^-}{V_1^+}_{|V_2^+=0}$$

- S_{22} is the output reflection coefficient and represents the accuracy of the output matching. This parameter is the ratio of the reflected and incident waves at the output port when there is no incident wave at the input port:

$$S_{22} = \frac{V_2^-}{V_2^+}_{|V_1^+=0}$$

Those values depend of the circuit's operating frequency and are usually represented in dB.

2.1.3 Gain

Nowadays the signals at a receiver's input are usually very weak, commonly in the microvolt (μV) range, so they need to be amplified in order to allow their processing by the receiver. This makes the gain a very important measure of the performance of an amplifier or a mixer because it expresses the capability of the circuit to increase the amplitude of an input signal, ideally introducing no distortion [10].

Usually, there are three different types of gain considered in electronics: voltage gain, current gain and power gain. For example, the voltage gain is defined as

$$A_v = \frac{v_{out}}{v_{in}}. \tag{2.17}$$

If $A_v > 1$ the input signal is amplified and if $A_v < 1$ the input signal is attenuated. The gain is often expressed in dB, for simplicity. It is important to note that voltage and current gains are expressed as $A_{v,i}|_{dB} = 20\log|A_{v,i}|$ and power gain is expressed as $A_p|_{dB} = 10\log|A_p|$.

2.1.4 Noise

Noise is a random process, i.e. its instantaneous value cannot be predicted at any time. It is present in all electronic circuits due to either external interference or physical phenomena related with the nature of materials. Since the noise presence is inevitable and it degrades the circuit's performance, it is important to analyze its impact, through statistical models, and create methods that allow the minimization of its effect on the circuit [2]. In this section the two main noise sources present in CMOS transistors, thermal and flicker noise, are described. The NF will also be introduced, which is the most common measure of the noise generated by a circuit.

2.1.4.1 Thermal Noise

The thermal noise in circuits is due to thermal excitation of charge carriers in a conductor. It occurs in all resistors (including semiconductors) working above absolute zero temperature and introduces fluctuations in the voltage measured across the device. This kind of noise has a white (flat) spectrum that is proportional to absolute temperature [11]. In a resistor the thermal noise can be modeled as a voltage source with a Power Spectral Density (PSD) of $\overline{V_n^2}$ in series with a noiseless resistor (Thevenin equivalent), or as a current source with a PSD of $\overline{I_n^2}$ in parallel with the same resistor (Norton equivalent) [1], as shown in Fig. 2.4. The average thermal noise power generated in a resistor is given by

$$\overline{V_n^2} = 4kTR\Delta f, \tag{2.18}$$

where k is Boltzmann's constant, T is the absolute temperature in Kelvin and Δf is the system bandwidth. Usually it is assumed that $\Delta f = 1$ Hz, for notation simplicity, which means that the noise power is expressed per unit bandwidth.

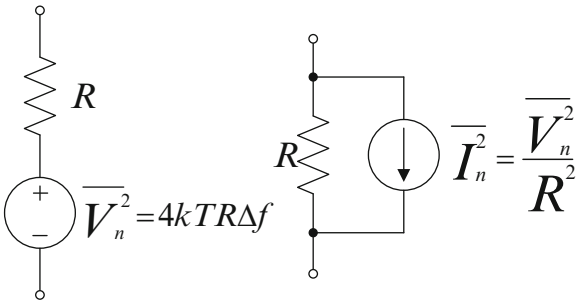


Fig. 2.4 Thevenin and Norton models of a resistor thermal noise

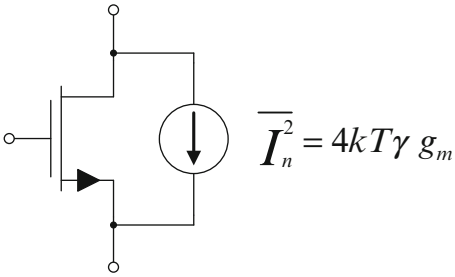


Fig. 2.5 Thermal channel noise of a MOS transistor model

The MOS transistors also exhibit thermal noise that is almost completely generated in the channel due to carrier motion, and for long-channel devices operating in saturation it can be modeled by a current source connected between the drain and source terminals [2], as shown in Fig. 2.5. In this case, the average thermal noise current generated by a MOS transistor is given by

$$\overline{I_n^2} = 4kT\gamma g_m, \tag{2.19}$$

where γ is the *excess noise factor* and has the value of 2/3 for long-channel transistors and higher values for short-channel devices [12], and g_m is the transistor's transconductance.

For the particular case of a MOS transistor operating in deep triode region, where $V_{DS} \approx 0$, it acts like a voltage-controlled resistor with V_{GS} used as control terminal, and with an on resistance given by $R_{on} \approx r_{ds} = 1/g_{ds}$. Then, as with the resistors, the generated thermal noise current is given by

$$\overline{I_n^2} = 4kTg_{d0}, \tag{2.20}$$

where g_{d0} is the transistor output conductance (g_{ds}) for $V_{DS} = 0$. It is important to note that in this operating region is assumed that $\gamma = 1$, so it is omitted in (2.20).

Another source of thermal noise in MOS transistors is related with the gate resistance. Despite being more negligible than the noise due to channel carrier motion, this effect is becoming more important for the new technologies, as the gate length is scaled down [1].

2.1.4.2 Flicker Noise

Flicker noise is present in all active devices, although it only occurs when a DC current is flowing, and has origin in a phenomenon at the interface between the gate oxide (SiO_2) and the silicon substrate (Si). As charge carriers move at the SiO_2–Si interface, some are randomly trapped and released introducing "flicker" noise in the drain current [2]. In addition to this phenomenon, other mechanisms are believed to generate flicker noise [13]. Unlike thermal noise in MOS transistors, this noise is more easily modeled as a voltage source in series with the gate and exhibits the following PSD:

$$\overline{V_{nf}^2} \approx \frac{K_f}{C_{ox} WLf}, \tag{2.21}$$

where K_f is a process dependent constant that is bias independent, C_{ox} is the gate oxide capacitance per unit area, W is the transistor channel width and L is the channel length. It is important to note that K_f is lower for p-channel devices, so PMOS transistors exhibit less flicker noise than NMOS transistors. Also, flicker noise is inverse to transistor's dimensions and to decrease the noise the device area must be increased. Since this noise is well modeled as having a $1/f$ spectral density, as shown in Fig. 2.6, it is also known as 1/f noise.

The 1/f noise corner frequency, f_c in Fig. 2.6, can be obtained by converting the flicker noise voltage (2.21) to current and equating the result to the thermal noise current expressed in (2.19) [1], resulting in

$$f_c = \frac{K_f}{WLC_{ox}} \frac{g_m}{4KT\gamma}. \tag{2.22}$$

For today's MOS technologies the corner frequency is relatively constant and falls in the range of tens or hundreds of megahertz [1].

2.1.4.3 Noise Figure

The Noise Factor (F) or Noise Figure (NF) (when expressed in dB) is the most common measure of the noise generated by a circuit and is defined as the ratio of the total available noise power at the output of the circuit to the available noise power at output due to noise from the input termination, as shown in (2.23).

$$F = \frac{N_o}{N_i G_A}, \tag{2.23}$$

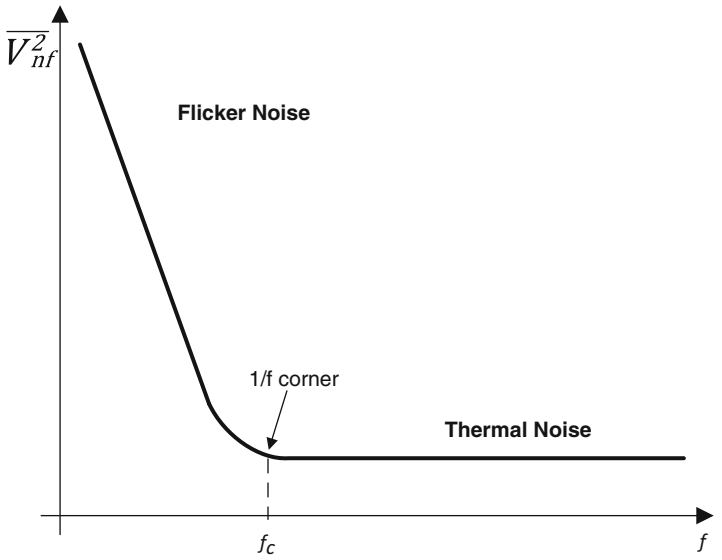


Fig. 2.6 Power spectrum of flicker and thermal noise

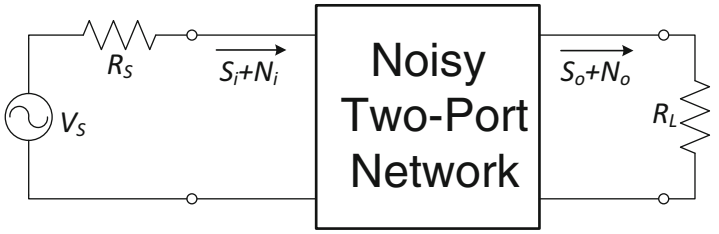


Fig. 2.7 Noisy two-port network

where N_i and N_o are, respectively, the available power noise at the circuit's input and output, and G_A is the available power gain of the circuit. By definition, N_i is the noise power resulting from a matched resistor at $T_o = 290\,\text{K}$ [9].

Assuming that the circuit is a two-port network, as shown in Fig. 2.7, with both input and output ports adapted, if a power signal S_i is applied at the input then the signal is totally transferred to the network's output (according to maximum power transfer theorem), and therefore the power gain of the circuit is expressed by

$$G_A = \frac{S_o}{S_i}. \tag{2.24}$$

By replacing (2.24) in (2.23) it is possible to conclude that

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{SNR_i}{SNR_o} \tag{2.25}$$

or, in decibels,

$$NF = 10 \log \frac{SNR_i}{SNR_o}. \tag{2.26}$$

The previous equation shows that NF is a measure of the degradation in the Signal-to-noise Ratio (SNR) between the input and output of the circuit, so if no noise is introduced by the network, $F = 1$ or $NF = 0\,\text{dB}$.

For a circuit with m cascaded stages the total NF is given by

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{G_{A1}} + \ldots + \frac{NF_m - 1}{G_{A1} \ldots G_{A(m-1)}}, \tag{2.27}$$

where NF_x and G_{Ax} are the NF and the available power gain of the stage x, respectively. This equation[1] shows that the first stages in a cascade circuit are the most critical, since the noise contribution of a stage decreases as the total power gain preceding that stage increases [1].

2.1.5 Nonlinearities Effects

Analog circuits can be approximated by a linear model for small-signal operation, modeled as a Taylor series in terms of the input signal voltage, as expressed in (2.28). However, there are no ideal linear components due to some non-linear characteristics related with noise, gain compression, etc., present in real devices like transistors. These nonlinearities may lead to signal distortion, losses, interference with other radio channels, among others [9]. Linearity is one important measurement of performance of a system and describes the impact of the nonlinearities on an output signal.

$$v_o = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \ldots \tag{2.28}$$

If a sine-wave, $v_i(t) = V_o \cos(\omega t)$, is applied to a device's input, the system response can be well described as the following third-order polynomial:

$$v_o = a_0 + a_1 V_o \cos(\omega t) + a_2 V_o^2 \cos^2(\omega t) + a_3 V_o^3 \cos^3(\omega t) \tag{2.29}$$

or

$$\begin{aligned} v_o = &\overbrace{\left(a_0 + \frac{1}{2} a_2 V_o^2\right)}^{\text{DC}} + \overbrace{\left(a_1 V_o + \frac{3}{4} a_3 V_o^3\right) \cos(\omega t)}^{\text{Fundamental Harmonic}} + \overbrace{\frac{1}{2} a_2 V_o^2 \cos(2\omega t)}^{2^{nd}\text{ Harmonic}} \\ &+ \underbrace{\frac{1}{4} a_3 V_o^3 \cos(3\omega t)}_{3^{rd}\text{ Harmonic}}. \end{aligned} \tag{2.30}$$

[1] Known as Friis' equation [14].

From this equation it is possible to conclude that a nonlinear system produces as many harmonics as the order of its nonlinearities. The even order coefficients compromise the DC component and the odd order coefficients affect the fundamental harmonic (ω) amplitude.

In this section, the 1 dB Compression Point (P1dB) and the second and third-order intermodulation products will be presented, since these parameters are very important to express the system performance related with linearity, and they usually appear in the system specifications.

2.1.5.1 Gain Compression

The 1 dB Compression Point (P1dB) quantifies the operating range of a circuit and it is defined as the input signal level that causes the gain to decrease 1 dB compared with the ideal linear characteristic, as shown in Fig. 2.8. Since the voltage gain of the signal at the fundamental harmonic frequency ω_0 is, as stated in (2.30), given by

$$A_v = \left(\frac{v_o}{v_i}\right)_{\omega_0} = a_1 + \frac{3}{4}a_3 V_o^2 \tag{2.31}$$

and typically a_3 has the opposite sign of a_1 [9], the gain of the circuit tends to be lower than the expected for large values of V_o, which causes this gain compression and consequently degrades de output signal. For an ideal linear circuit the gain would be equal to a_1.

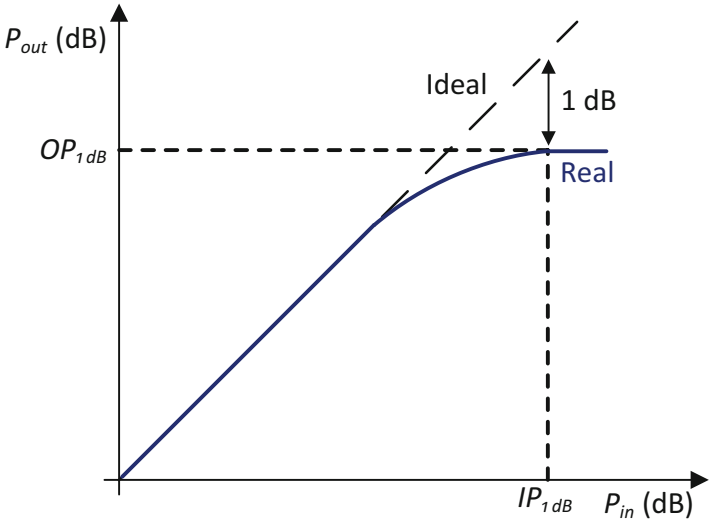


Fig. 2.8 Definition of P1dB

It is important to note that the P1dB can be referred to the input (IP1dB) or to the output (OP1dB). Typically it is given as the larger option, so for an amplifier it is usually specified as OP1dB and for a mixer as IP1dB.

2.1.5.2 Intermodulation Distortion

The previous nonlinearity considers only one signal at the system's input, which creates undesired frequency components at multiples of ω_0 that usually lie outside the passband of the circuit and do not interfere with the desired signal. If two signals are applied to the circuit, there are other nonlinear effects that do not manifest themselves in the previous situation, and can corrupt the desired signal since they produce harmonics that are not multiples of the fundamental harmonic frequency. This phenomenon is called Intermodulation (IM). For instance, assume that a signal $v_i(t) = V_{o1}\cos(\omega_1 t) + V_{o2}\cos(\omega_2 t)$ is applied to a system modeled by (2.28). Considering only the second and third terms of the Taylor series, the IM products at the output are given by

$$\begin{aligned} IM2 = {} & a_2\left[\frac{1}{2}V_o^2(1+\cos(2\omega_1 t)) + \frac{1}{2}V_o^2(1+\cos(2\omega_2 t))\right] \\ & + a_2\left[V_o^2\cos(\omega_1 t - \omega_2 t) + V_o^2\cos(\omega_1 t + \omega_2 t)\right] \end{aligned} \tag{2.32}$$

$$\begin{aligned} IM3 = {} & a_3 V_o^3\left[\frac{1}{4}\cos(3\omega_1 t) + \frac{1}{4}\cos(3\omega_2 t) + \frac{3}{4}\cos(\omega_1 t) + \frac{3}{4}\cos(\omega_2 t)\right] \\ & + a_3 V_o^3\left[\frac{3}{2}\cos(\omega_2 t) + \frac{3}{4}\cos(2\omega_1 t - \omega_2 t) + \frac{3}{4}\cos(2\omega_1 t + \omega_2 t)\right] \\ & + a_3 V_o^3\left[\frac{3}{2}\cos(\omega_1 t) + \frac{3}{4}\cos(2\omega_2 t - \omega_1 t) + \frac{3}{4}\cos(2\omega_2 t + \omega_1 t)\right]. \end{aligned} \tag{2.33}$$

These interacting signals will produce intermodulation products that originate harmonics at the sum and difference of both input signals frequencies and their multiples, as shown in Fig. 2.9.

If the two input signals frequencies, ω_1 and ω_2, are close, the second order intermodulation products can be easily filtered from the output since they are far from the input frequencies. However, the third order intermodulation products are very near the input signals, as shown in Fig. 2.9, and corrupt the desired signals because it is very difficult to filter them with a bandpass filter. From this analysis it is possible to conclude that IM3 is more problematic than IM2 and requires special attention.

To understand at which point the curves of power output of fundamental frequency and of the third-order intermodulation product would intercept if they

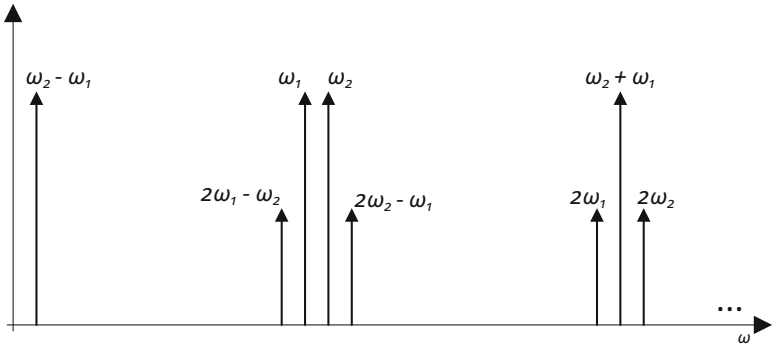


Fig. 2.9 Output spectrum of IM2 and IM3

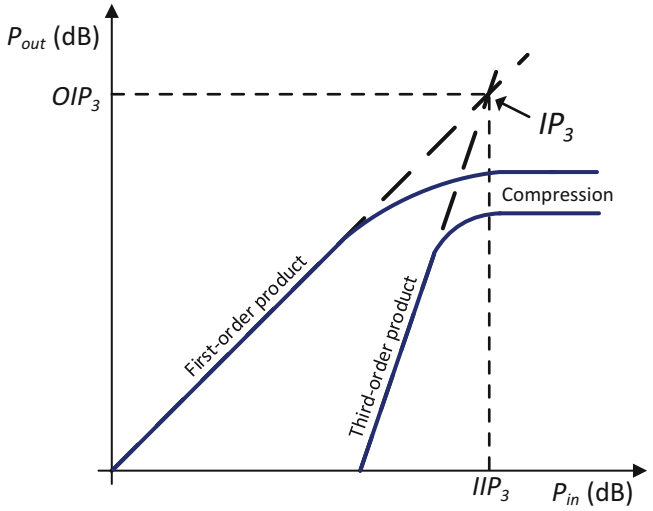


Fig. 2.10 Definition of IP3

were linear, i.e. if they did not suffer compression at high input power, the Third-order Intercept Point (IP3) was defined. As shown in Fig. 2.10, the IP3 can be input-referred (IIP3) or output-referred (OIP3) and the chosen result is typically the largest value as in the P1dB.

From Fig. 2.10 it is possible to note that the output power of the first-order product is proportional to the input power and, since the voltage associated with the third-order products increases as V_o^3, as shown in (2.33), the output power of the third-order product has a slope of 3, so they always intercept each other assuming that both are ideal (do not suffer compression). A practical rule that is usually employed is that the IP3 is 10–15 dB higher than P1dB [9].

For the second-order intermodulation product there is a similar analysis that leads to the definition of the Second-order Intercept Point (IP2).

2.2 Receiver Architectures

In a wireless system the receiver AFE is one of the most critical components since, due to the communication medium (air), the received signals are usually very weak and noisy. A wireless receiver needs to have the capability to filter the incoming signal in order to eliminate undesired interferes that can corrupt it, and detect the information present in the signal of interest. Since the signals are propagated at high frequencies, because it is possible to store more information using higher bandwidth and the antennas size is smaller, the receiver needs to convert those signals to lower frequencies. In summary, a receiver needs to filter and amplify the received signal, introducing almost no noise, and then down-convert that signal so that it can be demodulated and processed by a digital system. The main blocks of a wireless receiver are the LNA, the LO and the mixer. Receivers can be divided into three main groups: heterodyne, homodyne and low-IF, which will be presented in this section.

2.2.1 Heterodyne Receiver

The super-heterodyne receiver, also known as IF receiver, is one of the most used receiver topologies in wireless communication systems, and was proposed by Armstrong in 1917 [15]. As shown in Fig. 2.11, the down-conversion is done in two steps. First, the input signal is converted to a fixed IF, after being amplified by a LNA and filtered (by an image rejection BPF), and then that signal is filtered by a channel select BPF and down-converted to baseband. Finally, it is filtered again by a LPF. The down-conversions are made by a multiplication (mixing) of the RF signal with the signal produced by the LO. At the end the signal is converted to the digital domain by an ADC [1].

The main purpose of the image rejection filter (IR BPF) is to eliminate the image that can be produced in the down-conversion, since two input frequencies can produce the same IF, as shown in Fig. 2.12. The channel select filter (CS BPF) filters the interferers that are down-converted together with the signal and can corrupt it at

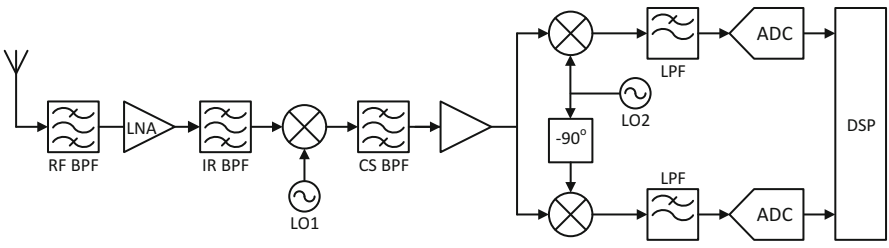


Fig. 2.11 Super-Heterodyne receiver architecture (adapted from [15])

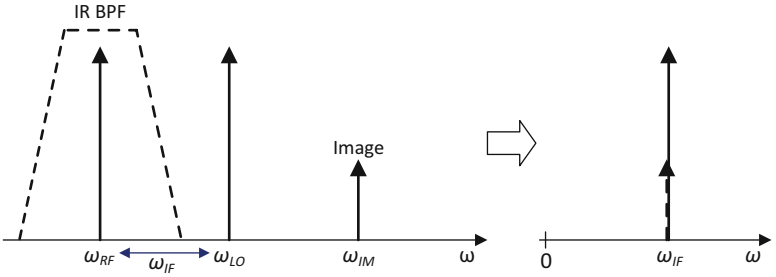


Fig. 2.12 Image rejection in super-heterodyne receiver (adapted from [15])

the next down-conversion. The choice of the IF needs to take into account that with high IF the image rejection filter is easier to design and with low IF the suppression of interferers is easier [15]. Due to the required high Q of the filters, they need to be implemented with reactive components, which is not a good solution for modern applications where a low-area and low-cost design is required. The main advantage of this kind of receivers is that it is possible to handle modern modulation schemes that require IQ (in-phase and quadrature) signals to fully recover the information.

Assuming that the receiver's input signal is a pure sine wave expressed by $v_{RF}(t) = V_{RF}\cos(\omega_{RF}t)$ and the LO produces a sine wave given by $v_{LO}(t) = V_{LO}\cos(\omega_{LO}t)$, the signal at the first mixer's output is given by

$$v_{IF}(t) = v_{RF}(t) \cdot v_{IF}(t) = \frac{1}{2} V_{RF} V_{LO} \left[\cos(\omega_{RF}t - \omega_{LO}t) + \cos(\omega_{RF}t + \omega_{LO}t)\right] \tag{2.34}$$

with $\omega_{IF} = \omega_{RF} - \omega_{LO}$.

Although the RF BPF eliminates the unwanted signals that may be present in the spectrum and are far from ω_{IF}, a major problem can occur if there is a signal $v_{IM}(t) = V_{IM}\cos(\omega_{IM}t)$ with $\omega_{IM} = 2\omega_{LO} - \omega_{RF}$ at the mixer's RF input, called image signal. After the mixing, $v_{IF}(t) = v_{IM}(t) \cdot v_{IF}(t)$, which means that the mixing originates two signals at frequencies $\omega_1 = \omega_{LO} - \omega_{RF}$ and $\omega_2 = 3\omega_{LO} - \omega_{RF}$. If no IR BPF is used, the frequency ω_1 overlaps and degrades the signal of interest, since $|\omega_1| = |\omega_{IF}|$. As shown in Fig. 2.12, this filter needs to have a high Q, mostly if ω_{IF} is low.

2.2.2 Homodyne Receiver

The homodyne receiver, also known as direct-conversion receiver or zero-IF receiver, translates the input signal to the baseband in a single down-conversion, using a LO with the same frequency as the RF signal. This avoids the use of an external image rejection filter, and only a LPF is required after the mixer to do the proper channel selection, as shown in Fig. 2.13.

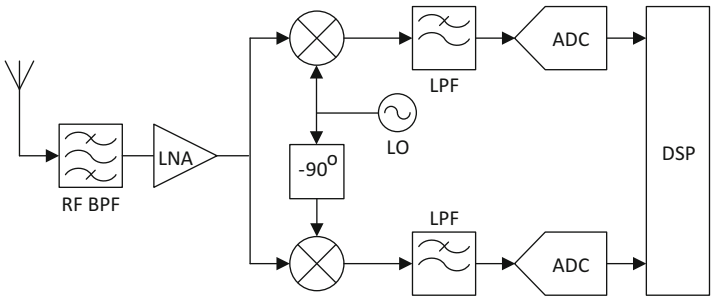


Fig. 2.13 Homodyne receiver architecture (adapted from [15])

The RF BPF before the LNA is often used to suppress the interferers outside the receiver band, so the Q requirements are not very demanding. The main advantages of this kind of receiver are the low-power, low-area and low-cost realization [15]. Despite these advantages, homodyne receivers have several disadvantages, comparing with heterodyne receivers, that prevent this architecture from being applied in more demanding applications [1, 15]:

LO leakage Due to the capacitances between the LO and RF ports of the mixer and capacitances or resistances between the LNA ports, the receiver will couple signals into the antenna that will be emitted and can interfere with other receivers using the same wireless standard. This effect can be minimized with the use of differential LO and mixer outputs to cancel common mode components.

DC offsets Due to the LO leakage, referred above, that appears at the LNA and mixer inputs, a DC component is generated at the mixer's output (this process is known as LO "self-mixing"). This signal can saturate the baseband circuits, preventing signal detection. This topology of receiver needs DC offset removal in order to avoid this kind of problems.

Channel selection The LPF must suppress the out-of-channel interferers in order to be possible to convert the desired baseband signal to the digital domain. This filter should have high linearity and low noise contributions, which makes it difficult to implement.

Flicker noise This type of noise can corrupt the baseband signals, as explained in Sect. 2.1.4.2, since their frequency is close to DC in these receivers.

Even-order distortion If two close interferers (at frequencies ω_1 and ω_2) exist near the channel of interest, after the mixing a second order term resulting of the mixing of these two signals is shifted to near the baseband (since $\omega_2 - \omega_1 \approx 0$) and appears at the output together with the down-converted signal, which leads to signal distortion. Thus, these kind of receivers must have a very high IP2. One solution to avoid this problem is use differential LNAs and mixers, in order to eliminate even-order harmonics.

I/Q mismatch Errors in the 90° phase shift circuit and mismatches between the I and Q mixers result in imbalances in the gain and phase of the baseband I and Q outputs, which can corrupt the down-converted signal constellation (e.g. in

Quadrature Amplitude Modulation (QAM)). Since modern wireless applications have different information in I and Q signals, this aspect is very critical in direct-conversion receivers because it is very difficult to implement high frequency blocks with very accurate quadrature relationship.

This kind of receiver requires very linear blocks and very precise quadrature oscillators, in order to avoid the problems described above, that are very difficult to achieve for high frequencies.

2.2.3 Low-IF Receiver

Although the heterodyne receiver has high performance and flexibility, it requires the use of external components, which does not allow the receiver full integration. On the other hand, the homodyne receiver can be totally integrated but has some problems related with flicker noise, intermodulation, etc. The low-IF receiver combines the advantages of both types of receivers, and uses a mixed approach, which consists in select a low intermediate frequency, avoiding the direct conversion problems previously indicated. To overcome the image problem related with the non-direct conversion, without the need of an image rejection filter, it is used a technique to cancel the image signal that consists in a quadrature architecture that suppresses the image by generating a negative replica. There are two main image rejection architectures, the Hartley and the Weaver [1, 15], as shown in Fig. 2.14.

The Hartley architecture [16] mixes the RF signal with the quadrature outputs of the LO and, after the LPF, one of the resulting signals is shifted 90° and subtracted to the other signal, as shown in Fig. 2.14a. For instance, consider that the signal $x(t) = V_{RF}\cos(\omega_{RF}t) + V_{Im}\cos(\omega_{Im}t)$ is placed at the receiver's input, where V_{RF} and V_{Im} are, respectively, the amplitude of the RF and of the image signals. After down-conversion and filtering,

$$x_1(t) = -\frac{V_{RF}}{2}\sin[(\omega_{RF} - \omega_{LO})t] + \frac{V_{Im}}{2}\sin[(\omega_{LO} - \omega_{Im})t] \tag{2.35}$$

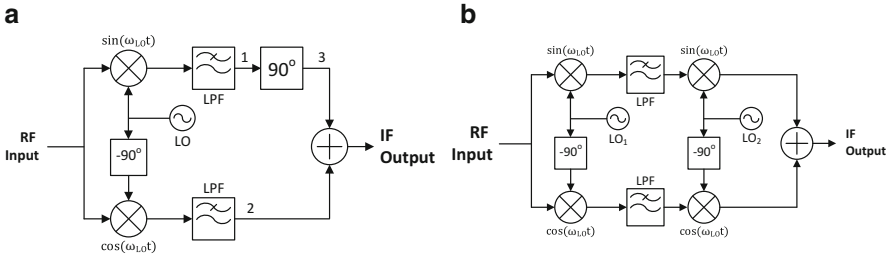


Fig. 2.14 Image rejection architectures: (**a**) Hartley (**b**) Weaver (adapted from [15])

$$x_2(t) = \frac{V_{RF}}{2}\cos[(\omega_{LO} - \omega_{RF})t] + \frac{V_{Im}}{2}\cos[(\omega_{LO} - \omega_{Im})t]. \tag{2.36}$$

Since a shift of 90° is equivalent to a change from sin to (− cos),

$$x_3(t) = \frac{V_{RF}}{2}\cos[(\omega_{RF} - \omega_{LO})t] - \frac{V_{Im}}{2}\cos[(\omega_{LO} - \omega_{Im})t]. \tag{2.37}$$

Due to 90° the phase shift, this receiver produces the same polarities for the desired signal and opposite polarities for image, in the two paths. Summing both signals, $x_2(t)$ and $x_3(t)$, results in

$$x_{IF}(t) = V_{RF}\cos[(\omega_{RF} - \omega_{LO})t] \tag{2.38}$$

Thus, the image component is canceled and the desired signal is doubled in amplitude. The main problems of this architecture are the receiver sensitivity to the local oscillator quadrature errors and the incomplete image cancellation due to the mismatches in the two signal paths.

The Weaver architecture, as shown in Fig. 2.14b, is similar to the Hartley architecture, but the 90° phase shift is performed by a second mixing operation in both signal paths. This kind of approach has the same problems of the Hartley architecture and it suffers from an image problem in the second down-conversion, if the signal is not converted to the baseband.

2.2.4 Modern Wideband Receivers

With the constant evolution of wireless communications, it is desirable to have a radio platform that is able to operate within a wide frequency band, and that supports many services, such as GSM, GPS, WiFi, among others. This avoids the use of multiple front-ends and allows to reduce the products' cost and size. The concept of Software-defined Radio (SDR), introduced by Mitola [17], specifies that "all RF and baseband received signal processing is digital, enabled by an ADC at the antenna" [18]. The main problem of this architecture, where the ADC digitizes the RF signal without previous down-conversion and filtering, is that the ADC has specifications that are impossible to fulfill nowadays [18, 19]. This problem can be solved by moving the ADC to the baseband, as shown in Fig. 2.15, such as in the architectures referred in the previous sections. However, these architectures rely on an input SAW filter to remove out-of-band interferers that can corrupt the desired signal. These filters are difficult to integrate on the receiver, are expensive, and are limited to a specific frequency range, making it impossible to cover the entire band of a wideband receiver. To overcome this problem it is necessary to have an input filter that covers the receiver working band and that can be programmed to perform filtering in a frequency defined by the LO, according to the receiver's input signal.

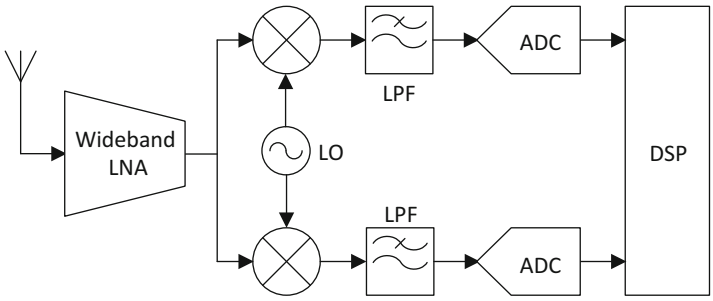


Fig. 2.15 Wideband receiver simplified architecture

Moreover, to allow the receiver's impedance matching to the antenna over its entire working band, without penalizing the noise figure, it is necessary to employ noise and distortion canceling techniques at the input stage.

In the last years, new receiver architectures—usually referred as SAW-less receivers, wideband receivers, cognitive radio receivers, multi-band receivers, and software defined receivers—have emerged, with the purpose of designing a very flexible receiver without inductors, which increase the chip area and cost [19, 20]. The more promising architectures were recently reviewed in [19, 20] and can be in voltage-mode or current-mode. Voltage-mode receivers are more power efficient, but suffer a huge penalty in linearity, which is an essential performance parameter in wideband receivers. On the other hand, current-mode receivers are more complex and have more power consumption but, since there is almost no voltage variation in the signal path, they are very linear and can tolerate large out-of-band interferers. Since the CMOS circuits' supply voltage is constantly reducing with the technologies' evolution, which limits the circuits' voltage swing; current-mode receivers are a very promising solution because they have no hard limits on the current that flows through the signal path. Thus, it is possible to deal with strong interferers without corrupting the receiver's performance [19].

Regarding current-mode receivers, the most promising architectures are based on passive mixers [20]. The main advantages of this kind of mixers are the ability to perform impedance transformation, due to the lack of reverse isolation between the baseband and RF sections, and the high linearity.

In order to improve the performance of a wideband receiver, there are three main principles that have been widely used recently [19, 20]:

- *Noise and distortion cancellation*: This technique consists of using two parallel stages. The first stage performs input impedance matching and the second stage cancels the noise contributions of the first stage [21]. This cancellation can be implemented using a CG and a CS stages. The CG stage performs the input impedance matching and the CS stage cancels the noise generated by the CG stage, since it reverses the phase of the amplified signal but not of the noise

voltage. This circuit also allows to convert a single-ended signal to differential, avoiding the use of an external balun on the receiver's chain;
- *N-Path filtering*: This technique is based in a current-driven passive mixer and allows to convert a low-pass baseband impedance into a high-Q RF band-pass impedance that is precisely controlled by the LO frequency. Thus, it is possible to attenuate out-of-band interferers at the receiver's input over its entire working band;
- *N-path mixing*: The mixer's main problem is that, due to the hard switching, it also converts interferers located at frequencies that are multiple of f_{LO} to the baseband, which can corrupt the desired signal. By performing n-path mixing and harmonic recombination, it is possible to generate a quantized sinewave, which rejects the most critical f_{LO} harmonics (especially 3rd and 5th).

These techniques have shown very promising results in modern wideband receivers during the recent years.

This book is focused on a current-mode receiver, based on a current-driven passive mixer, which employs noise cancellation and N-path filtering. The noise and distortion cancellation is performed at the wideband LNA stage, and allows to eliminate the noise contributions of the main path by using an auxiliary path, as will be demonstrated below. The out-of-band interferers filtering is also performed at the LNA stage, by two N-path high-Q BPF, and at the mixer, due to its impedance transformation properties. The receiver's input matching is performed by the LNA main path, together with the filter at the LNA input.

Chapter 3
RF Blocks

This chapter presents an overview of the RF front-end key blocks. The basic aspects of LNAs, filters, mixers, oscillators, and ADCs are reviewed in order to understand their importance and how they can be integrated in a receiver AFE.

3.1 Low-Noise Amplifiers

This section reviews some LNA topologies and addresses typical requirements for these blocks. The LNA is typically the first stage of an RF receiver so its input impedance should match the antenna's characteristic impedance in order to maximize the power transfer, as discussed in Sect. 2.1.1. The LNA should introduce a minimum noise to the system while providing enough gain, to obtain the required SNR. As expressed in (2.27), in cascaded stages the NF of the first stage (LNA) is dominant and should be very low, and the gain should be very large to reduce the noise contributions of the following stages. Regarding the circuit's linearity, in cascaded stages it is limited by the stage with the worst IP3, and the gain of the preceding stages affects negatively the IP3 of the subsequent stages, as expressed in (3.1), so there is a trade-off between noise and linearity, since a low NF demands a high gain as explained before [1].

$$\frac{1}{IP3_{tot}} = \frac{1}{IP3_{LNA}} + \frac{G_{A,LNA}}{IP3_{mixer}} + \ldots \tag{3.1}$$

Regarding the bandwidth, LNAs can be narrowband or wideband. In this section some LNA topologies will be presented and their behavior with respect to input matching, gain, and noise figure will be studied.

M.D. Fernandes, L.B. Oliveira (eds.), *Wideband CMOS Receivers*, SpringerBriefs in Electrical and Computer Engineering, DOI 10.1007/978-3-319-18920-8_3

3.1.1 Narrowband LNAs

These LNAs work with a fixed input frequency so the input matching is easier to achieve than in wideband LNAs, because the LNA only needs to be matched to the antenna's impedance for that frequency, and the matching can be performed with reactive components.

3.1.1.1 Common-Source LNA with Inductive Degeneration

The Common-Source (CS) LNA with inductive degeneration [22], represented in Fig. 3.1, is one of the most used topologies of narrowband LNAs because it allows easy input matching, high gain and low noise figure.

The input impedance of this LNA is given by

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s. \tag{3.2}$$

By choosing $L_s + L_g$ to resonate with C_{gs} it is possible to eliminate the imaginary terms of the input impedance, so the impedance will look real near the desired operating frequency. By adjusting the inductance L_s it is possible to match the antenna's impedance for that frequency. Since the inductors are ideally noiseless,

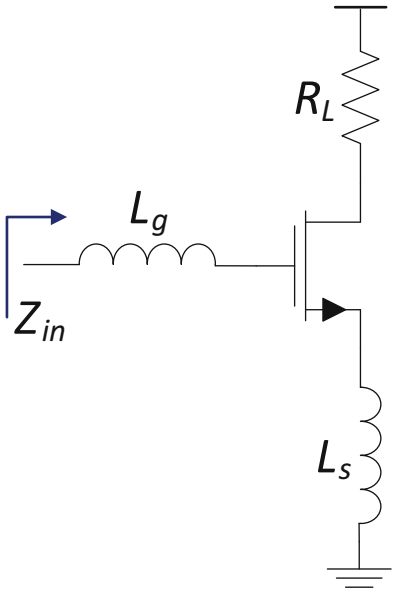


Fig. 3.1 CS LNA with inductive degeneration

they contribute with almost no noise to the LNA so it has a low noise figure. The main disadvantage of this circuit is the large die area and the special RF options needed to design high-Q inductors, which increase the production cost.

3.1.2 Wideband LNAs

This sort of LNA operates in a wide frequency range so these blocks need to match the antenna's impedance for the entire LNA working band, which is not possible to achieved through reactive components.

3.1.2.1 Common-Source Stage with Resistive Input Matching

The resistive input matching is the easiest way to obtain a stable input impedance over the LNA working band because, as shown in Fig. 3.2, the input resistor is in parallel with the transistor gate, which has infinite input impedance.

The main drawback of this configuration is that the resistor introduces a significant amount of noise. Assuming that the LNA has an available power gain G_A and output noise power P_n, and that the source has an impedance R_S (from antenna) that is matched to R_{in}, from (2.18) and (2.23) it is possible to obtain the resulting noise factor:

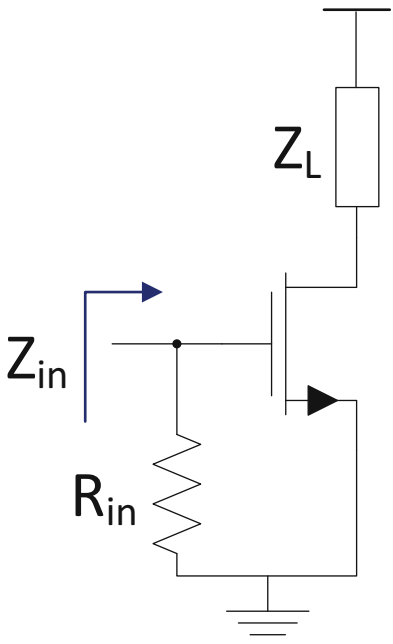
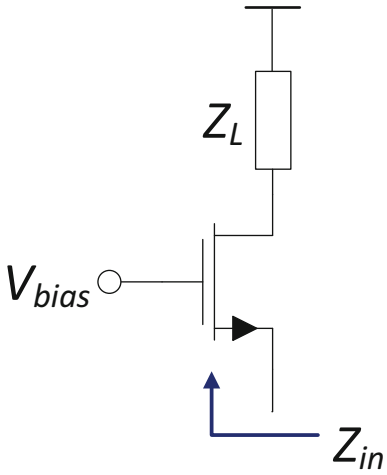


Fig. 3.2 CS LNA with resistive input matching

Fig. 3.3 Common-gate LNA



$$F = \frac{4kTR_sG_A + 4kTR_{in}G_A + P_n}{4kTR_sG_A} = 2 + \frac{P_n}{4kTR_{in}G_A} \tag{3.3}$$

that is at least 2, resulting in a noise figure greater than 3 dB.

3.1.2.2 Common-Gate Stage

The Common-Gate (CG) stage, shown in Fig. 3.3, is one of the most used topologies to implement wideband LNAs because it has an intrinsic wideband response. The LNA input impedance is approximately $1/g_m$, neglecting the channel-length modulation and body effects. Thus, the dimensions of the transistor and the bias current are chosen in order to obtain $g_m = 1/R_S = 20\,\text{mS}$ for a $50\,\Omega$ antenna.

Considering only the transistor thermal noise, and assuming that it is a long channel device, the minimum noise factor of this topology can be easily calculated through (2.23), where $N_i = \overline{I_s^2}$ and $N_o = (\overline{I_s^2} + \overline{I_d^2})G_A$.

$$F = \frac{(\overline{I_s^2} + \overline{I_d^2})G_A}{\overline{I_s^2}G_A} = 1 + \frac{\overline{I_d^2}}{\overline{I_s^2}} \tag{3.4}$$

The average thermal noise at the LNA input due to the input impedance (transistor source) is $\overline{I_s^2} = 4kT/R_S = 4kTg_m$, and the average thermal noise generated at the gate of a MOS device working in the active region, $\overline{I_d^2}$, is given by (2.19), so

$$F = 1 + \frac{4kT\gamma g_m}{4kTg_m} = 1 + \gamma. \tag{3.5}$$

Table 3.1 Comparison between Narrowband and Wideband LNAs

Narrowband	Wideband
Low NF	High NF
High gain	Low power
Large area due to the inductors	Low area
High chip cost (special RF options)	Low cost (standard CMOS)

For a long channel device operating at the active region $\gamma = 2/3$, so the minimum noise factor of a CG amplifier is about $5/3$, which corresponds to a noise figure of 2.2 dB that is lower than that of the previous topology. The main disadvantage of this LNA is the fact that the gain is given by $G_A = g_m Z_L$. Since g_m is fixed due to the impedance matching, to increase the gain it is necessary to increase Z_L, limiting the achievable gain. Usually this kind of LNA has a noise figure above 3 dB. However, there are some noise cancellation techniques to be analyzed in the next chapter that can be used to reduce the LNA noise figure.

3.1.3 Discussion

In this section it was shown that there are two major types of LNA: narrowband and wideband. Table 3.1 presents the main characteristics of both.

The LNA architectures presented in this section are single-ended, so they have only one output. In order to transform the input signal into a differential signal at the output, a balun structure can be used instead, as will be studied in the next chapter. The main drawback of this structures is the extra loss and additional noise that are introduced, since more components are required.

3.2 Mixers

The mixer is key block of an RF front-end since it is responsible for the frequency translation of an RF signal to the IF or to the baseband, in a process called down-conversion. Ideally, the output signal is a multiplication of the RF input signal by another RF signal provided by an LO, as shown in Fig. 3.4. The resulting signal has two frequency components at the difference and the sum of the input frequencies [15].

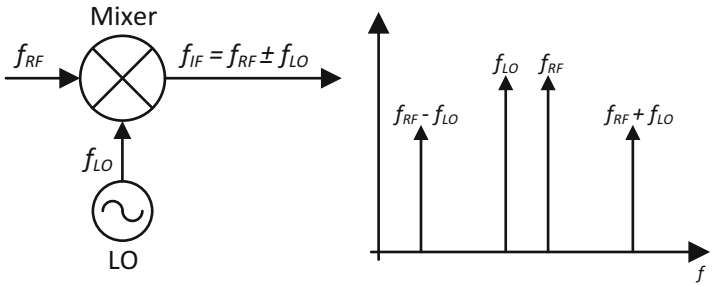


Fig. 3.4 Down-conversion mixer

Considering that the RF input signal is $v_{RF}(t) = \cos(2\pi f_{RF} t)$ and the LO signal is $v_{LO}(t) = \cos(2\pi f_{LO} t)$, the signal at the mixer's output is given by Pozar [9]

$$v_{IF}(t) = \frac{K}{2}\left[\cos(2\pi(f_{RF} - f_{LO})t) + \cos(2\pi(f_{RF} + f_{LO})t)\right], \tag{3.6}$$

where K is related to the voltage conversion loss of the mixer. For a down-conversion mixer the desired frequency component is $f_{IF} = f_{RF} - f_{LO}$, called *lower sideband* (LSB). This frequency can be easily selected by a LPF.

In this section the most important characteristics of mixers are reviewed: noise figure, intermodulation points, gain, etc., and different types of mixers (active and passive) are revisited [1, 9, 15].

3.2.1 Performance Parameters

Noise Since the mixer performs frequency translation, the noise at both sideband frequencies is also converted with the same efficiency, which means that the effects of both LNA and LO noise will appear at the mixer's output. That's why it is important to design those components to have a low NF, as explained before. Also, the input noise of the mixer is divided by the LNA gain so the NF of the mixer is very dependent of the LNA characteristics. Another important aspect is the flicker noise. If the output frequency (IF) is below the 1/f noise corner frequency (Fig. 2.6), its effect will be very pronounced at the mixer's output, so the IF selection must be done carefully.

Conversion gain The voltage conversion gain of a mixer is given by the ratio between the *rms* voltage of the IF signal and the *rms* voltage of the RF signal.

$$\text{Voltage Gain (dB)} = 20\log\left(\frac{V_{IF}}{V_{RF}}\right). \tag{3.7}$$

The conversion gain allows to distinguish between two different mixer types: passive mixers, which have conversion loss (gain lower than one), and active mixers, which have conversion gain higher than one.

Linearity Mixers perform a nonlinear operation, so the transistors behavior are nonlinear and the LO port of the mixer should also be very nonlinear due to gain and noise constraints. Due to these characteristics, there are undesirable spurious terms at the mixer's output that can affect the desired signal. In order to measure a mixer's linearity the IM (Sect. 2.1.5.2) is used. In a heterodyne receiver the third-order IM is the most important because if the two input signals are close in frequency, the third-order IM components will be close to the interesting frequency, making them very difficult to filter. In a homodyne receiver the second-order IM is more important, since the IM due to the two input signals can be close to DC and corrupt the output signal band. Larger order IM products are usually ignored because they are far from the band of interest and have lower amplitudes.

It is important to note that the IP3 of a mixer is scaled down by the LNA gain, as shown by (3.1), so there is a trade-off between the mixer's noise contributions to the receiver and the mixer's linearity.

3.2.2 Passive Mixers

These mixers have conversion gain lower than one. The easiest way to implement a mixer is by using a switch based on a MOS transistor, as shown in Fig. 3.5. Although this mixer uses an active device, it acts like a switch (operating at triode region) and consequently has no DC power consumption, has high bandwidth, high linearity and has very low flicker noise, which makes it very attractive to use in microwave circuits.

The RF signal is injected in the transistor's source and the LO signal, usually a rail-to-rail square wave,[1] is fed trough the transistor's gate. When the LO signal is at

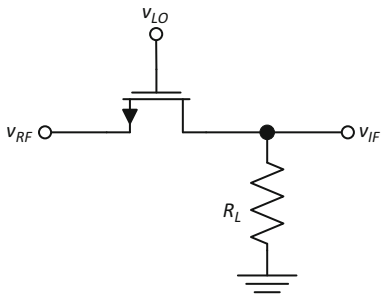


Fig. 3.5 Mixer using a MOS switch

[1]This guarantees that when the LO signal is high the transistor operates in the deep triode region.

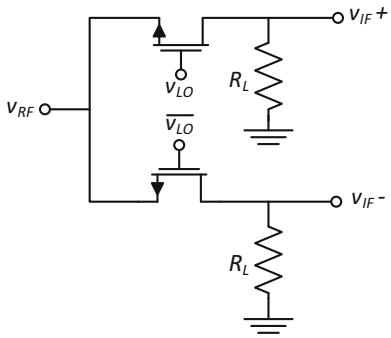


Fig. 3.6 Single-balanced passive mixer using MOS switches

high level the signal at the mixer's input is transferred to the output, since the switch is on, resulting in a frequency translation of the input signal to a frequency given by the difference of the RF and LO signals. This circuit is commonly called a *return-to-zero* mixer since the output is zero when the switch turns off. If the resistor R_L is replaced by a capacitor, the mixer operates as a sample-and-hold circuit, because the output does not fall to zero when the switch is off, resulting in a higher conversion gain. This configuration is called *non-return-to-zero* mixer.

In modern RF design, the mixers are realized as single-balanced (with a single-ended input), as shown in Fig. 3.6, or as double-balanced (with a differential input), instead of the single-ended topology of Fig. 3.5. By applying these techniques it is possible to obtain a conversion gain twice that of the *return-to-zero* mixer, because the output signal is differential. The double-balanced mixer also eliminates the LO-IF feed-through, which transfers the LO frequency to the output and can affect the mixer's performance.

Current-Driven Passive Mixers

If the LNA has high output impedance, it can be seen as a current source. Thus, the passive mixer's input is driven by a current source instead of a voltage source, and exhibit different properties (gain, noise, input impedance, etc.). Since a mixer is a *time-variant* circuit, the input impedance of a current-driven mixer is very different from a voltage-driven mixer. Considering the circuit of Fig. 3.7a, from [23] is possible to conclude that the switches mix the baseband waveforms with the LO, translating their spectrum to RF, as shown in Fig. 3.7b. Due to this effect, the input impedance around f_{LO} is a frequency-translated version of $Z_{BB}(f)$, i.e., if Z_{BB} is a low-pass impedance (e.g. a capacitor), then $Z_{in}(f)$ has a band-pass behavior. As will be studied in this work, this property can be very helpful to filter undesired components of the RF signal. Another advantage of this kind of mixer is that a device in series with a current source does not change the current that passes through it, so its noise and non-linearity contributions are much reduced.

As will be demonstrated later the mixers do not need to use a 50 % LO duty-cycle, and the use of other duty-cycle values (e.g. 25 %) can be very beneficial in terms of gain, noise figure, harmonic rejection, among others [24].

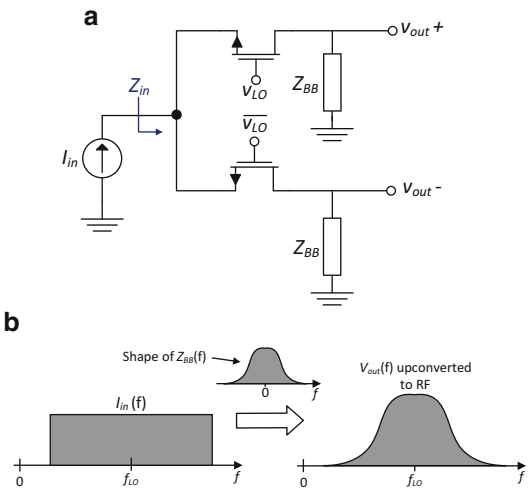


Fig. 3.7 (**a**) Current-driven passive mixer, (**b**) input frequency spectrum

3.2.3 Active Mixers

Active mixers have conversion gain higher than one, which helps to reduce the effect of the noise generated by subsequent stages, as demonstrated in Sect. 2.1.4.3. Due to this property, these mixers are very used in RF systems. The mixing operation is the same as of passive mixers but, instead of a MOS switch being used, a differential pair is used, as shown in Fig. 3.8. The transistors of the pair operate in the active region, and consequently provide current gain and have high output impedance. In this structure, known as *single-balanced active mixer*, the current source is controlled by the RF signal and the differential pair is controlled by the LO signal. This mixer converts the v_{RF} signal to a current that flows to one branch of the differential pair (where it is amplified) according to the value of v_{LO}, and it is converted back to voltage by the resistors R_D, generating the output differential voltage v_{IF}. Since it is single-balanced, this mixer only operates with a single-ended RF input.

Another very popular implementation is the Gilbert cell [25], shown in Fig. 3.9, also called *double-balanced active mixer*. Comparing with the previous topology, this mixer as higher gain, lower NF, better linearity, higher spurious rejection, higher port-to-port isolation and is less sensitive to even order distortion. The main drawbacks of this topology are the power consumption and the increased area, due to its complexity and the high number of active devices. Since it is double-balanced, this mixer needs a differential RF signal at the input to operate properly.

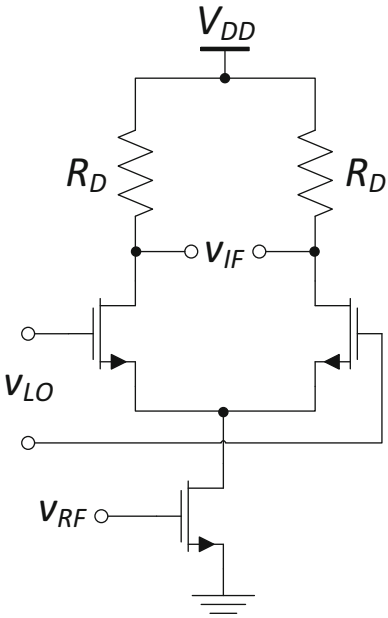


Fig. 3.8 Single-balanced active mixer

3.2.4 Discussion

In this section two main mixer types were presented: *passive* and *active*. The passive mixers do not have conversion gain but are very low power, have low noise and high linearity. Also, a passive mixer can be current-driven instead of voltage-driven, which has some advantages like baseband impedance transformation, low noise and low nonlinearity contributions. The active mixers have as main advantage the conversion gain higher than one, which helps to reduce the noise contribution of the subsequent stages of the receiver, but have more power consumption, generate more noise, have lower linearity and occupy a larger area, due to their complexity.

Regarding the mixer's inputs and outputs, the two main configurations are *single-balanced* and *double-balanced*. Both have differential outputs, which doubles the mixer gain relatively to a single-ended topology (Fig. 3.5). The single-balanced implementation needs a single-ended signal at the input while the double-balanced version needs a differential signal at the input, which sometimes requires the use of a balun, but has advantages in terms of gain, noise, linearity, port-to-port feed-through (especially LO-IF), among others. The disadvantages of double-balanced mixers with respect to single-balanced mixers are the power consumption and increased area, due to the larger number of active devices.

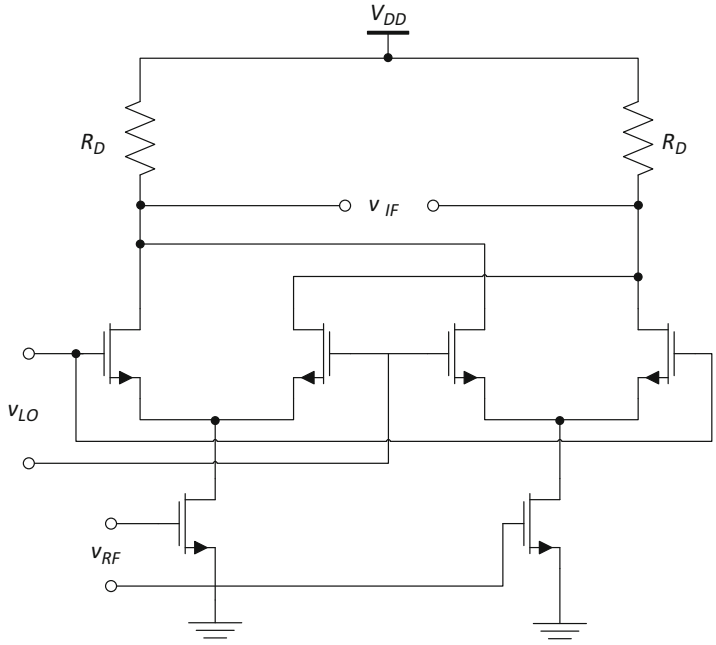


Fig. 3.9 Double-balanced active mixer

3.3 Oscillators

Oscillators are widely used in RF receivers, especially to drive the blocks that are responsible for frequency translation, such as the mixers. An oscillator should generate a periodic signal, with a frequency that can be tuned over a certain range (approximately the receiver's working range). The main limitation of an oscillator is the phase noise. This noise can be generated either inside or outside of the oscillator, and it has a large influence on the oscillator's amplitude and phase response, which can limit the receiver's immunity against interferers located near the desired signal [15]. Thus, this block should be carefully designed. Also, in a wideband CMOS receiver it is desirable to integrate the oscillator on the receiver's die to reduce the overall circuit's area and cost, which invalidates the use of LC oscillators (due to the required inductors). Therefore, this section reviews two types of RC oscillators, which can be integrated on CMOS receivers: relaxation oscillators and ring oscillators.

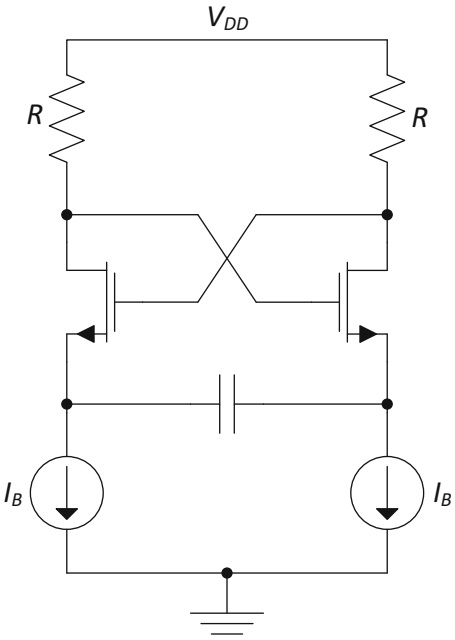


Fig. 3.10 Example of a relaxation oscillator for very high frequencies

3.3.1 Relaxation Oscillators

A relaxation oscillator is a strongly nonlinear oscillator that is widely used in integrated circuits, mainly because it does not have inductors.

This kind of oscillators is usually modeled by an integrator and by a Schmitt trigger, which is a memory element that controls the integrator. For very high frequencies, it is required a very simple circuit, as shown in Fig. 3.10. In this circuit, the integrator is implemented by a capacitor, which establishes the oscillation frequency [26]. Since the oscillator has noisy active and passive devices, such as resistors and transistors, it produces a considerable amount of phase noise, which makes it ineffective to be used in RF receivers due to the reasons explained above. It is possible to reduce the oscillator's phase noise, but this considerably increases the circuit's complexity and the chip area and cost [27].

3.3.2 Ring Oscillators

Ring oscillators, shown in Fig. 3.11, have become much used in recent years, mainly due to their simplicity, speed and easy integration in a CMOS receiver. This kind of oscillator is composed of multiple delay stages (A_N) with the output of the last stage fed back to the input of the first one. Each stage has a phase shift of π/N.

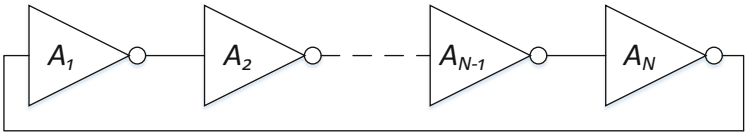


Fig. 3.11 Ring oscillator

A ring oscillator is usually composed by an odd number of identical inverter cells. The oscillation frequency is $f_{osc} = 1/(2N\tau_{inverter})$ [28], where $\tau_{inverter}$ is the time constant of each cell and is usually defined by the RC constant of the inverter. Due to this property, this oscillator is very programmable and covers a wide range of frequencies, which makes it very suitable to employ in modern wideband receivers.

3.3.3 Multi-Phase Oscillators

Modern RF receivers perform quadrature down-conversion at the mixer's stage. Although this conversion can be done by using a 4-phase 50 % duty-cycle clock, this has several associated problems, such as [29]:

- Unequal low-side and high-side conversion gains;
- Different low-side and high-side IP2 and IP3;
- Unexpected IP2 and IP3 values due to the crosstalk between channels;
- Increased receiver's noise figure due to the IQ interaction. This interaction happens because the mixer's switches of two different phases are on at the same time.

By using a 4-phase 25 % duty-cycle clock, the switches of the two quadrature channels are not on at the same time, thus avoiding interference between the two channels. Also, by using this approach, the mixer does not generate a voltage component at the image frequency, contrarily to a 50 % duty-cycle clock [29]. Thus, it is possible to minimize significantly the problems referred above.

Since in a 4-phase 25 % duty-cycle clock the waveforms are non-overlapping, when using a current-driven passive mixer to down-convert the RF signal, it is possible to perform impedance transformation, as explained in Sect. 3.2.2. Another advantage of the 25 % duty-cycle clock is that it increases the circuit's conversion gain by 3 dB, resulting in a lower overall receiver's noise figure [24].

Although a 4-phase 25 % duty-cycle oscillator can have many benefits when employed in continuous time (CT) receivers, in discrete time (DT) receivers it is necessary to oversample the RF signal at the analog front-end (AFE). This requires a high number of phases, to reduce the aliasing and consequently to reduce the BPF requirements [30]. However, the increase of the number of phases of the oscillator leads to a more complex circuit, which can limit its practicality. Recent works [30, 31] show that it is possible to design 8-phase 12.5 % duty-cycle oscillators to be employed in DT receivers.

3.4 RF Filters

With the growth of wireless communications the demand for high-performance RF (or microwave) filters has increased due to the limitations of the available frequency spectrum and the consequent growth of communication standards. The frequencies used to transmit the information are often closer to each other, which means that there are more interferers near the band of interest that need to be filtered in order to prevent the leakage of out-of-band intermodulation products and harmonics to the receiver [32]. Due to this proximity, the filters must have a high-Q factor, to suppress the nearest interferers, and low losses in the band of interest, in order to do not attenuate the desired signals.

A frequently used filter in an RF receiver's AFE is the SAW filter, placed as shown in Fig. 3.12, that attenuates the out-of-band blockers at the receiver's input and consequently prevents the LNA saturation. The major problem of this filter is that it is very expensive and bulky, and has higher insertion losses since it is usually based on resonators [3]. In a passive filter based on resonators the insertion loss is inversely proportional to its bandwidth and the resonator's Q factor, and it is proportional to the number of resonators [32]. Also, high-Q resonators are physically large. Active filters can be used to avoid this problem, since they have gain that compensates for the losses related with the resonators, but they suffer from harmonic distortion, increased NF and nonlinearities [33]. In order to save area and cost, filters based on resonators can be implemented in CMOS technologies and integrated in the receiver chip. However, unlike the off-chip filters, on-chip filters have low-Q factor, limited tuning range and the integrated coils take large chip area. There are some techniques to increase the Q factor but they degrade the filter noise and linearity [5].

To overcome the problems of resonator based filters, an old technique, called N-path filtering [34], has been used in state of the art receivers, and is adopted in this work. This solution is based on current-driven passive mixers, referred in Sect. 3.2.2, and allows the realization of a passive filter without inductors that can be precisely controlled by the LO frequency, resulting in an easily programmable filter that occupies low area. Also, these filters have high linearity, an acceptable NF

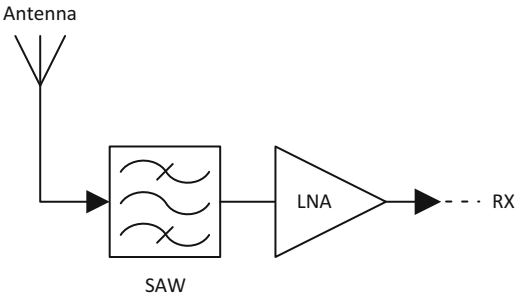


Fig. 3.12 Receiver AFE input

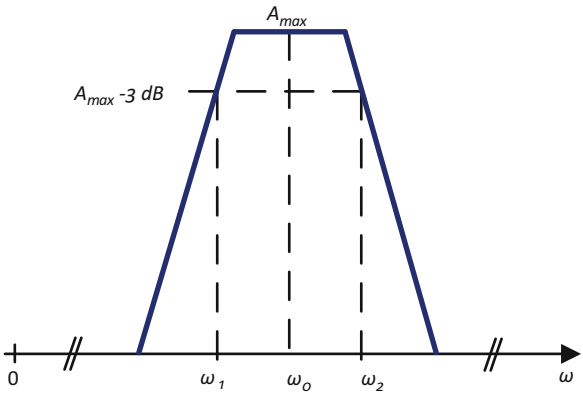


Fig. 3.13 BPF frequency response and Q factor

and high-Q factor (e.g. Q = 98 for 6.1 MHz bandwidth around 600 MHz) [3–6], as will be demonstrated below in this book. Due to its simplicity, these filters can be easily integrated in the receiver chip, avoiding the use of off-chip SAW filters. Also, since these filters do not use inductors, they can be implemented using standard CMOS technologies, avoiding the use of special RF options that are more complex and expensive.

Bandpass Filter Quality Factor

The quality factor (also referred to Q-factor) is a key parameter to measure the performance of a BPF. The definition of the Q factor is

$$Q = \frac{\omega_0}{BW}, \tag{3.8}$$

where ω_0 is the filter center frequency and BW is the filter bandwidth, which is given by $BW = \omega_2 - \omega_1$. Frequencies ω_1 and ω_2 are the frequencies at which the magnitude response of the filter drops by 3 dB relatively to its maximum value (A_{max}), as shown in Fig. 3.13.

Thus, the Q-factor is a parameter that measures the filter attenuation sharpness (or selectivity) and the higher the Q factor, the better the filter. This means that a high-Q BPF can block undesired signals that are closer to the band of interest, comparing with a low-Q BPF.

3.5 Analog-to-Digital Converters

Although the incoming signals to an RF receiver are in the analog domain, with the evolution of technology those signals began to be processed in the digital domain because digital systems are simpler, cheaper and more flexible. To make this possible it is necessary to employ an ADC, as shown in Fig. 3.14, that converts

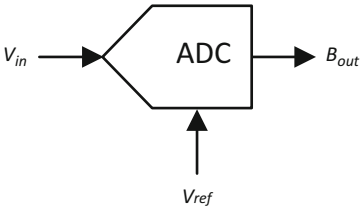


Fig. 3.14 ADC block diagram

an analog signal to the digital domain. Due to the performance requirements needed to digitize an RF signal, the ADC can not be moved towards the antenna, because a converter that fulfill these requirements would be impractical in actual CMOS technologies. One function of the AFE is to convert the RF signal to an analog signal that can be handled by the ADC.

In Fig. 3.14 B_{out} is the digital output word generated by the ADC, which depends on the analog input signal V_{in} and on the analog reference signal V_{ref}. It is important to note that the ADCs can be voltage or current-driven.

There are two main ADC types: *Nyquist-rate* and *oversampling*. The *Nyquist-rate* ADCs generate output values that have a one-to-one correspondence whit a single input value and usually operate at 1.5 to 10 times the Nyquist rate. The *oversampling* ADCs operate much faster than the input signal Nyquist rate and filter the quantization noise that is not in the desired signal's bandwidth, in order to increase the output SNR [11]. This sort of ADCs are very popular for high-resolution medium-to-low-speed applications, because they allow to relax the requirements of the analog circuitry and consequently reduce the circuit area and power consumption. Also, this type of ADCs allow the extraction of more bits of resolution than the Nyquist-rate converters, due to signal oversampling. The devices that perform this kind of conversion are usually called $\Sigma\Delta$ modulators [11].

The design of a $\Sigma\Delta$M is outside the scope of this book, so only a very short summary of this kind of converters is presented.

Chapter 4
Wideband Cascode Balun-LNA

A balun (which performs conversion from single-ended to differential) wideband LNA has been proposed [21, 35]. This topology is a good solution to implement in an RF receiver because it can be directly coupled to a differential mixer without separate balun or impedance matching networks, while performing noise and distortion cancellation. Since the LNA output is differential, it reduces harmonic distortion, improving the linearity, and rejects power supply and substrate noise. The cascode devices are used to allow the connection of a passive filter to the LNA nodes, as will be demonstrated, but they also contribute to decrease the effective input capacitance, which helps to improve the impedance matching over the working band, and to increase the LNA voltage gain. In order to improve the LNA voltage gain and NF some existing techniques can be employed [36]. This design was implemented in two different technologies, CMOS 130 nm and CMOS 65 nm. The design with the two technologies will be detailed and compared in the following sections.

This chapter is structured as follows: a theoretical analysis of the LNA is made and the main equations for its characterization are derived and validated by simulation.

4.1 Theoretical Analysis

The proposed LNA is represented in Fig. 4.1. From basic circuit analysis it is known that the CG and CS stages have approximately the same voltage gain but with opposite sign. Thus, the signal at the CG stage's output is equal to the input signal amplified, whereas the signal at the CS stage's output has the opposite phase. The LNA output signal is equal to the difference of these output signals, $v_{out} = v_{out+} - v_{out-}$. The thermal noise produced by the CG stage (modeled by $\overline{i_n}$) generates a noise voltage $\overline{v_{n,in}}$ at the input of the CS stage, since it flows into R_S. It

M.D. Fernandes, L.B. Oliveira (eds.), *Wideband CMOS Receivers*, SpringerBriefs in Electrical and Computer Engineering, DOI 10.1007/978-3-319-18920-8_4

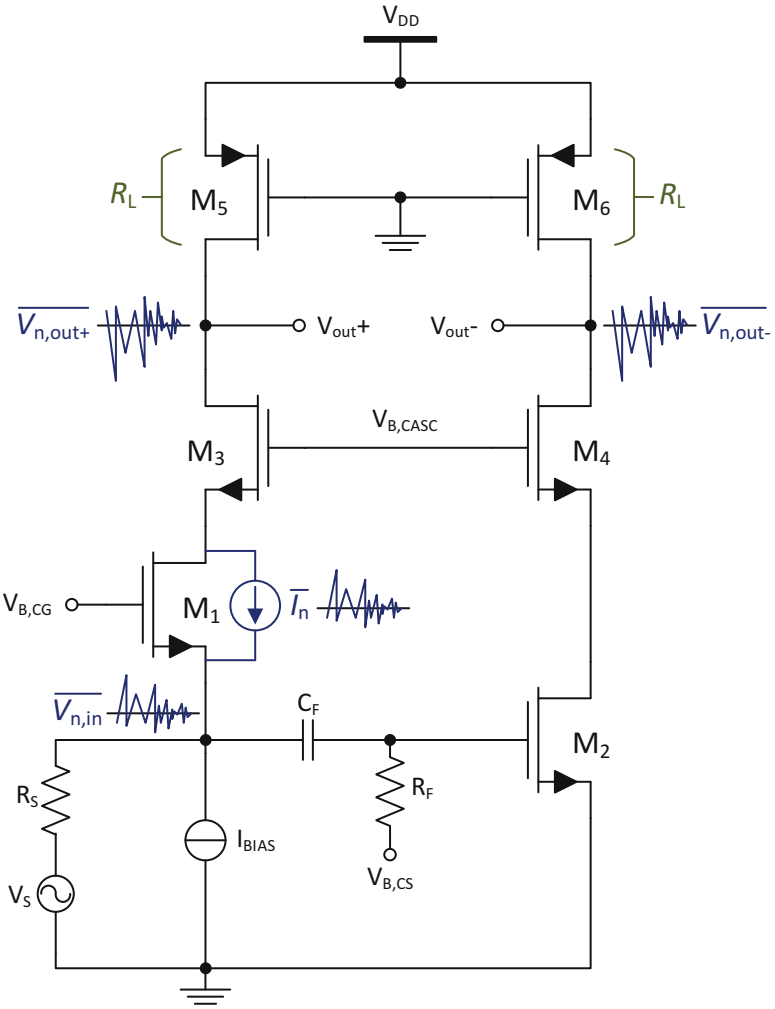


Fig. 4.1 Wideband cascode balun LNA with noise cancellation

also generates a noise voltage $\overline{v_{n,out+}}$, with opposite phase, at the CG output. Since the CS inverts the voltage phase, both noise voltages at the output of the CG and CS stages have the same signal, and are canceled at the LNA output. For a full thermal noise cancellation it is critical that the gain of both stages is matched.

In order to improve the LNA performance, the conventional load resistors were replaced by PMOS transistors (M_5 and M_6) that operate in the triode region [36]. Thus, the impedance seen at the LNA output nodes is approximately given by $R_L = r_{ds} = 1/g_{ds}$, where g_{ds} is the transistor output conductance. By employing this technique is possible to increase the incremental load resistance with the same DC

voltage drop, compared to conventional resistors, and consequently it is possible to increase the voltage gain and reduce the circuit's NF.

The following circuit equations are derived neglecting the transistors capacitive effects, the CG transistor body effect and the short-channel effects (due to the use of the minimum L allowed by the technology).

4.1.1 Input Impedance

Assuming that the biasing current-source I_{bias} has a very high output impedance, the LNA input impedance is given by the parallel of the input impedance of the CG and CS stages,

$$Z_{in} \cong Z_{in,CG} \parallel Z_{in,CS}. \tag{4.1}$$

Since the CS input is the transistor gate, which has a very high impedance, Z_{in} can be expressed by Carusone et al. [11]

$$Z_{in} \cong Z_{in,CG} \cong \frac{1}{g_{m,CG}} \left(1 + \frac{R_{casc}}{r_{ds,CG}}\right), \tag{4.2}$$

where $g_{m,CG}$ and $r_{ds,CG}$ are, respectively, the transconductance and the output resistance of the CG transistor. The R_{casc} is the impedance seen from the cascode transistor (M_3) input (source), and it is very similar to (4.2):

$$R_{casc} \cong \frac{1}{g_{m,Casc}} \left(1 + \frac{R_L}{r_{ds,Casc}}\right), \tag{4.3}$$

where $g_{m,Casc}$ and $r_{ds,Casc}$ are, respectively, the transconductance and the output resistance of the output transistor of the cascode configuration. For simplicity, considering that $r_{ds,Casc} \gg R_L$ and $r_{ds,CG} \gg R_{casc}$, then

$$Z_{in} \approx \frac{1}{g_{m,CG}}. \tag{4.4}$$

4.1.2 Voltage Gain

Given that the LNA output is differential and the input signal of both stages is the same, the voltage gain is given by Carusone et al. [11]

$$A_v = A_{v,CG} - A_{v,CS} \cong g_{m,CG} \cdot R_{out} + g_{m,CS} \cdot R_{out} \tag{4.5}$$

because the voltage gain of the CS stage and of the CG stage have opposite signals. R_{out} is the LNA output impedance seen at one node and is expressed by $R_{out} = r_{CG} \parallel R_L$ in the CG stage and $R_{out} = r_{CS} \parallel R_L$ in the CS stage, where r_{CG} and r_{CS} are the impedances seen from the cascode devices' output, and are given by $r_{Cx} \cong r_{ds,Cx} \cdot r_{ds,Casc} \cdot g_{m,Casc}$. Therefore, considering that r_{CG} and r_{CS} are very high comparing with R_L, then $R_{out} \approx R_L$ and consequently

$$A_v \approx g_{m,CG} \cdot R_L + g_{m,CS} \cdot R_L. \tag{4.6}$$

Since both stages need to have the same gain to allow the full cancellation of the CG thermal noise,

$$A_v \approx 2 \cdot g_{m,CG} \cdot R_L \tag{4.7}$$

It is important to note that the cascode configuration increases the output impedance of the stage but do not affects the voltage gain of the LNA because these impedances (r_{CG} and r_{CS}) are much higher than the resistance of the PMOS devices (R_L), as explained before, and since they are in parallel the LNA output impedance is approximately R_L. The increase of R_L has the disadvantage of reducing the LNA bandwidth, since it decreases the frequency of the output pole (which is the LNA dominant pole).

4.1.3 Noise Factor

The noise factor (F) or Noise Figure (NF) when expressed in dB, referred in Sect. 2.1.4.3, is one of the most important measurements of an LNA, because this block noise contributions have a huge impact on the receiver's total noise. Since the cascode devices don't force current into the LNA, their noise contributions are very reduced (it was verified by simulation that these transistors have a noise contribution between 3 and 5 % of the total LNA's circuit) and consequently M_3 and M_4 were ignored in this analysis, i.e. the analysis was made considering the basic CG and CS topologies. Also, only the transistors' thermal noise was considered, since flicker noise is negligible at high frequencies and the other noise sources are insignificant compared with the thermal noise.

4.1.3.1 Common-Gate Stage

The CG stage small signal noise model is presented in Fig. 4.2. There are three main noise sources that will be considered in this analysis: due to the source resistor (R_S), due to the CG transistor (M_1) and due to the load resistor (R_L). The effect of these sources will be analyzed separately and the results are added to obtain the stage's noise factor. For simplicity, it was considered that $g_{m_1} \gg g_{ds_1}$ and $r_{ds_1} \gg R_L$ in all calculations.

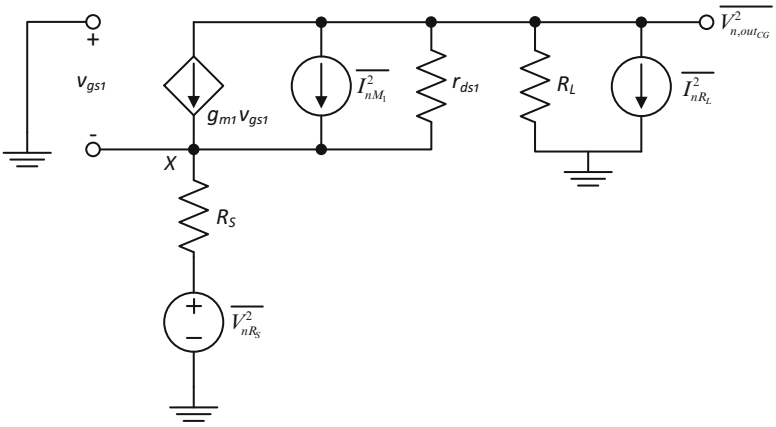


Fig. 4.2 Small signal noise model of the CG stage

Thermal noise due to R_S

Considering only the noise source of R_S, in Fig. 4.2, the output noise power is given by

$$\overline{V_{nR_S,out_{CG}}^2} = \overline{V_{nR_S}^2} A_{v,CG}^2. \tag{4.8}$$

In a CG stage, $A_{v,CG} \approx \frac{g_m R_L}{1+g_m R_S}$ [10] and, from (2.18), it is known that $\overline{V_{nR_S}^2} = 4kTR_S$, which leads to

$$\overline{V_{nR_S,out_{CG}}^2} \approx \frac{4kTR_S\,(g_{m_1}R_L)^2}{(1+g_{m_1}R_S)^2}. \tag{4.9}$$

Thermal noise due to M_1

Considering only the thermal noise source from M_1, in Fig. 4.2, and applying the KCL at node X, it is possible to obtain

$$i = \frac{I_{nM_1} - g_{ds_1} \cdot V_{nM_1,out_{CG}}}{1 + R_S(g_{m_1} + g_{ds_1})}, \tag{4.10}$$

which results in the following output noise voltage:

$$V_{nM_1,out_{CG}} = i \cdot R_L \approx I_{nM_1} \frac{R_L}{1+g_{m_1}R_S}. \tag{4.11}$$

From (2.19) it is known that $\overline{I_{nM_1}^2} = 4kT\gamma g_{m_1}$, leading to

$$\overline{V_{nM_1,out_{CG}}^2} \approx 4kT\gamma g_{m_1} \left(\frac{R_L}{1 + g_{m_1} R_S} \right)^2. \tag{4.12}$$

Thermal noise due to R_L

Considering only the noise source from R_L, in Fig. 4.2, and ignoring R_S for now (which leads to $v_{gs_1} = 0$ V),

$$V_{nR_L,out_{CG}} = I_{nR_L}(r_{ds_1} \parallel R_L) \approx I_{nR_L} R_L. \tag{4.13}$$

The noise voltage at the CG input due to R_L is equal to

$$V_{nR_L,in} = \frac{V_{nR_L,out_{CG}}}{A_{v,CG}} \approx \frac{I_{nR_L} R_L}{A_{v,CG}}. \tag{4.14}$$

However, this result does not take into account the effect of R_S. Considering the Thevenin's equivalent of the CG input, shown in Fig. 4.3, the voltage at the transistor's input is given by (4.15) [21].

$$V_{in} = \frac{Z_{in,M_1}}{Z_{in,M_1} + R_S} V_S \approx \frac{1}{1 + g_{m_1} R_S} V_S, \tag{4.15}$$

with $Z_{in,M_1} \approx 1/g_{m_1}$ as stated in (4.4). Substituting V_S by (4.14) leads to

$$V_{in} \approx \frac{1}{1 + g_{m_1} R_S} \cdot \frac{I_{nR_L} R_L}{A_{v,CG}}. \tag{4.16}$$

Considering that $\overline{V_{nR_L,out_{CG}}^2} = \overline{V_{in}^2} A_{v,CG}^2$ and $\overline{I_{nR_L}^2} = 4kT/R_L$ (from (2.18)), it is possible to obtain the following output power noise, considering R_S,

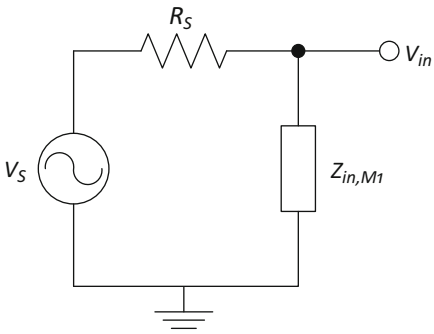


Fig. 4.3 CG Thevenin's equivalent circuit

$$\overline{V^2_{nR_L,out_{CG}}} \approx \frac{4kTR_L}{(1+g_{m_1}R_S)^2}. \tag{4.17}$$

Noise Factor
As stated in (2.23), the CG stage noise factor is given by

$$F = \frac{\overline{V^2_{n,out_{CG}}}}{\overline{V^2_{nR_S}} \cdot A^2_{v,CG}}, \tag{4.18}$$

where

$$\overline{V^2_{n,out_{CG}}} = \overline{V^2_{nR_S,out_{CG}}} + \overline{V^2_{nM_1,out_{CG}}} + \overline{V^2_{nR_L,out_{CG}}}. \tag{4.19}$$

The noise factor is

$$F \approx 1 + \frac{\gamma}{g_{m_1}R_S} + \frac{1}{g^2_{m_1}R_SR_L} \tag{4.20}$$

4.1.3.2 Common-Source Stage

The CS stage small signal noise model is presented in Fig. 4.4. As with the CG stage, there are three main noise sources: due to the source resistor (R_S), due to the CS transistor (M_2) and due to the load resistor (R_L). For simplicity, it was considered that $r_{ds_2} \gg R_L$ in all calculations.

Thermal noise due to R_S
Considering only the noise source from R_S, in Fig. 4.4, the output noise power can be written as

$$\overline{V^2_{nR_S,out_{CS}}} = \overline{V^2_{nR_S}} A^2_{v,CS}. \tag{4.21}$$

In a CS stage, $A_{v,CS} \approx -g_mR_L$ [10] and from (2.18) it is known that $\overline{V^2_{nR_S}} = 4kTR_S$, resulting in

$$\overline{V^2_{nR_S,out_{CS}}} \approx 4kTR_S(g_{m_2}R_L)^2. \tag{4.22}$$

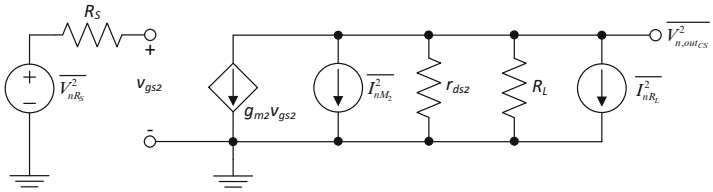


Fig. 4.4 Small signal noise model of the CS stage

Thermal noise due to M_2
Considering only the noise source from M_2, in Fig. 4.4, and knowing that in this configuration $v_{gs_2} = 0$ V,

$$V_{nM_2,out_{CS}} = I_{nM_2}(r_{ds_2} \parallel R_L) \approx I_{nM_2} R_L. \tag{4.23}$$

From (2.19) it is known that $\overline{I^2_{nM_2}} = 4kT\gamma g_{m_2}$, and consequently

$$\overline{V^2_{nM_2,out_{CS}}} \approx 4kT\gamma g_{m_2} R_L^2. \tag{4.24}$$

Thermal noise due to R_L
Finally, considering only the noise source from R_L, in Fig. 4.2, and since $v_{gs_2} = 0$ V, the output noise voltage is given by

$$V_{nR_L,out_{CS}} = I_{nR_L}(r_{ds_2} \parallel R_L) \approx I_{nR_L} R_L. \tag{4.25}$$

From (2.18) it is known that $\overline{I^2_{nR_L}} = 4kT/R_L$, which leads to

$$\overline{V^2_{nR_L,out_{CS}}} \approx 4kTR_L. \tag{4.26}$$

Noise Factor
As shown in (2.23), the CS stage noise factor is given by

$$F = \frac{\overline{V^2_{n,out_{CS}}}}{\overline{V^2_{nR_S}} \cdot A^2_{v,CS}}, \tag{4.27}$$

with

$$\overline{V^2_{n,out_{CS}}} = \overline{V^2_{nR_S,out_{CS}}} + \overline{V^2_{nM_2,out_{CS}}} + \overline{V^2_{nR_L,out_{CS}}}, \tag{4.28}$$

resulting in the following CS noise factor

$$F \approx 1 + \frac{\gamma}{g_{m_2} R_S} + \frac{1}{g^2_{m_2} R_S R_L}. \tag{4.29}$$

4.1.3.3 Complete LNA

Comparing (4.20) and (4.29) is possible to conclude that the noise factors of CG and CS stages are identical. Since the noise generated by the CG stage appears at the CS input, it is necessary to obtain the noise power generated by the CG stage that manifests at the output of the CS stage, i.e. it is necessary to divide the noise generated by the CG stage by the CG stage's gain and multiply it by the CS gain, as

shown in the following equations. Initially, the noise generated by R_S is neglected and it is added in the final equation, as with the thermal noise analysis of R_L in the CG stage. For simplicity, it is assumed that $g_{m_1} = g_{m_2}$, as explained in Sect. 4.1.2.

$$\overline{V^2_{nM_1,out_{CS}}} = \overline{V^2_{nM_1,out_{CG}}} \frac{A^2_{v_{CS}}}{A^2_{v_{CG}}} \approx 4kT\gamma g_m R_L^2 \tag{4.30}$$

$$\overline{V^2_{nR_L,out_{CS}}} = \overline{V^2_{nR_L,out_{CG}}} \frac{A^2_{v_{CS}}}{A^2_{v_{CG}}} \approx 4kTR_L \tag{4.31}$$

Obviously, the noise generated by the CS also appears at the CG output, so it is necessary to perform an identical operation for these noise contributions.

$$\overline{V^2_{nM_2,out_{CG}}} = \overline{V^2_{nM_2,out_{CS}}} \frac{A^2_{v_{CG}}}{A^2_{v_{CS}}} \approx \frac{4kT\gamma g_m R_L^2}{(1 + g_m R_S)^2} \tag{4.32}$$

$$\overline{V^2_{nR_L,out_{CG}}} = \overline{V^2_{nR_L,out_{CS}}} \frac{A^2_{v_{CG}}}{A^2_{v_{CS}}} \approx \frac{4kTR_L}{(1 + g_m R_S)^2} \tag{4.33}$$

The total noise at the LNA output is given by the sum of all the noise contributions of both stages, $\overline{V^2_{n,out_{LNA}}} = \overline{V^2_{n,out_{CG}}} + \overline{V^2_{n,out_{CS}}}$, with

$$\overline{V^2_{n,out_{CG}}} = \overline{V^2_{nM_1,out_{CG}}} + 2\overline{V^2_{nR_L,out_{CG}}} + \overline{V^2_{nM_2,out_{CG}}} \tag{4.34}$$

$$\overline{V^2_{n,out_{CS}}} = -\overline{V^2_{nM_1,out_{CS}}} + 2\overline{V^2_{nR_L,out_{CS}}} + \overline{V^2_{nM_2,out_{CS}}} \tag{4.35}$$

Since the CS inverts the signals at its input, the thermal noise generated by the CG transistor (M_1) appears at the CS output with opposite signal, as shown in (4.35), and is canceled as desired. Thus, the LNA's thermal noise depends only of M_2 and R_L. Applying the same logic as in (4.15), the LNA noise factor is given by

$$F = \frac{(1 + g_m R_S)^2(\overline{V^2_{nR_S}} A^2_{v_{LNA}} + \overline{V^2_{n,out_{LNA}}})}{(1 + g_m R_S)^2 \overline{V^2_{nR_S}} A^2_{v_{LNA}}} = 1 + \frac{\overline{V^2_{n,out_{CG}}} + \overline{V^2_{n,out_{CS}}}}{\overline{V^2_{nR_S}} A^2_{v_{LNA}}}, \tag{4.36}$$

with $A_{v_{LNA}} \approx 2 \cdot g_{m,CG} \cdot R_L$, as stated in (4.7), and $\overline{V^2_{nR_S}} = 4kTR_S$. Solving the previous equation, and assuming that in the CG stage $g_m R_S \ll 1$, for simplicity,

$$F \approx 1 + \frac{\gamma}{2g_m R_S} + \frac{1}{g_m^2 R_S R_L}. \tag{4.37}$$

As stated before, the previous equation shows that by increasing the load resistance R_L is possible to decrease the circuit's NF.

4.1.4 Load Transistors Resistance

As explained before, PMOS devices (M_5 and M_6) are used to replace the traditional load resistors. These transistors work in the triode region and behave as a voltage controlled resistor with V_{GS} used as control terminal. In this region, the current that passes through a PMOS transistor is given by Carusone et al. [11]

$$I_D = \mu_P C_{ox} \frac{W}{L} \left[\left(|V_{GS}| - |V_{tp}| \right) |V_{DS}| - \frac{V_{DS}^2}{2} \right], \tag{4.38}$$

which leads to

$$R_L = r_{ds} = \left[\frac{\partial I_D}{\partial V_{DS}} \right]^{-1} = \frac{1}{\mu_P C_{ox} \frac{W}{L} \left(|V_{GS}| - |V_{tp}| - |V_{DS}| \right)}. \tag{4.39}$$

From the previous equation is possible to conclude that if $|V_{DS}|$ (referred as V_{R_L} for simplicity) is increased, the resistance R_L also increases, and the voltage gain becomes higher, as demonstrated above. Another option to increase R_L is by decreasing $V_{DSsat} = V_{GS} - V_{tp}$. However, to keep the transistor operating at the triode region it is necessary to guarantee that $0 < |V_{DS}| < |V_{DSsat}|$, and if V_{DSsat} is reduced, this condition is more difficult to satisfy. For this work it was chosen $V_G = 0$ V, which leads to $|V_{GS}| = V_{DD}$ (because the source of the transistors is connected to V_{DD}) and guarantees that $|V_{DSsat}| > |V_{DS}|$, as desired. By changing the transistors width (W), it is possible to change V_{R_L} to the intended value and, consequently, to change R_L.

As stated in (2.19), the thermal noise generated by a MOS transistor is given by $\overline{I_{n,MOS}^2} = 4kT\gamma g_m$ and, as shown in (2.18), the thermal noise generated by a resistor is given by $\overline{I_{n,res}^2} = 4kT/R$. Considering that for a transistor operating in triode region $\gamma = 1$,

$$\frac{\overline{I_{n,MOS}^2}}{\overline{I_{n,res}^2}} = \frac{4kTg_m}{4kT/R} = g_m R. \tag{4.40}$$

For instance, to obtain a resistance of 400 Ω, in a PMOS device it is necessary $g_m \approx 1.6$ mS (for CMOS 130 nm technology) and a resistor of $R = 400$ Ω. Thus, from (4.40) it is possible to conclude that $\overline{I_n^2, MOS} \approx 0.64 \cdot \overline{I_n^2, res}$, which means that a transistor operating at the triode region generates less thermal noise than a resistor. Also, since the voltage gain of the LNA is higher, the associated NF is lower, as indicated by (2.23). Due to the high circuit operating frequencies, the flicker noise is negligible. This analysis proves that using PMOS transistors as active loads, instead of resistors, increases the overall LNA performance, increasing the voltage gain and reducing the NF.

This increase of the load resistance, compared with traditional resistors, also contributes to the increase of the LNA output impedance, since $R_{out} = r_{CG} \parallel R_L$. Since the mixer of the AFE is current-driven, as will be shown later, the LNA output impedance needs to be high in order to approximate an ideal current source and guarantee the mixer proper performance.

As disadvantages, the bandwidth of the LNA is lower due to the transistors' parasitic capacitances and to the larger output node resistance, which reduce the frequency of the LNA dominant pole. Also, the linearity suffers a penalty mainly due to the improvement of the voltage gain and the MOS transistors' intrinsic nonlinearities [36].

4.2 Circuit Implementation Using CMOS 130 nm

Since an antenna's typical impedance is 50 Ω, the LNA was designed to have this input impedance, to allow the maximum power transfer, as referred in Sect. 2.1.1. The circuit's supply voltage is $V_{DD} = 1.2$ V. The biasing current was chosen as 1.5 mA and $V_{R_L} = 600$ mV, in order to have high load resistance values while ensuring the sufficient DC voltage to keep all the transistors in the active region. The output transistors of the cascode stages were designed to have a reasonable input impedance to allow the connection of the BPF that will be studied in the next chapter. In order to be possible to achieve the desired frequencies, all the transistors have the minimum channel length (L) allowed by the CMOS 130 nm technology, which is 120 nm. Thus, the transistors' parasitic capacitances are the smallest possible, maximizing the LNA poles frequency. The capacitor $C_F = 5$ pF and the resistor $R_F = 20$ kΩ are intended to isolate the CG and CS stages at DC, allowing both stages to have independent DC operating points. They act as a High-pass Filter (HPF) with a bandwidth of approximately 1.6 MHz.

From (4.4) is possible to fix the transconductance of M_1, and consequently of M_2 (since the voltage gain of both stages needs to be equal to achieve the full noise cancellation), in 20 mS. Different $g_m - R_L$ relations have been studied in [21, 35], but they lead to more power consumption. The DC voltage $V_{B,CG}$ was chosen in order to keep the desired operation of the CG transistor and give some room to implement a bias current source with a simple current-mirror. The DC voltage $V_{B,CS}$ is used to adjust the DC current of M_2 to the desired value of 1.5 mA. Finally, $V_{B,Casc}$ was chosen equal to V_{DD} in order to allow all transistors to operate in the active region and ensure a low g_m (and consequently a high input impedance) for the cascode devices.

With respect to the transistors at the output of the cascodes stages, they were designed to have an input impedance of about 300 Ω. This impedance value was chosen considering the filter that will be connected at these devices' input, as explained in the next chapter. Since this impedance is given by (4.3), to achieve $R_{casc} \approx 300\ \Omega$ it is necessary to have $g_{m,Casc} \approx 3.3$ mS. Notice that if R_{casc} is very large, $g_{m,Casc}$ needs to be very small and, since $g_m = 2I_D/V_{DSsat}$ and I_D is fixed,

V_{DSsat} becomes very large. In order to keep all the transistors in the active region $V_{DS} > V_{DSsat}$, so if the input impedance of these transistors is very large, the V_{DS} needs also to be very large and it is more difficult to keep all the transistors in the active region, because the supply voltage is limited to 1.2 V.

Simulation Results

To verify the equations of LNA parameters, studied in the last section, simulations were made taking into account the circuit constraints that were referred above. Table 4.1 shows the transistors dimensions, used in the simulation, and the DC operating points (operating region, DC current, V_{DSsat} and g_m).

The chosen bias voltages are $V_{B,CG} = 535$ mV and $V_{B,CS} = 383$ mV. Regarding M_1 and M_2 dimensions, the difference of sizes is explained by the body effect that was ignored in the theoretical analysis and affects the CG transistor, increasing its gain. The transistors' intrinsic gain (g_m/g_{ds}) also has influence on M_2 dimensions since a large g_m leads to a lower transistor's output impedance (r_{ds}) and consequently it is necessary to have an even larger g_m in order to obtain the desired voltage gain at the CS stage, since this stage gain decreases for lower values of $r_{ds,CS}$. To compensate this limitation it is necessary to increase the CS transistor g_m in order to obtain the same voltage gain at both stages. To increase g_m, V_{DSsat} should be decreased (because g_m is inversely proportional to this voltage), which leads to a larger transistor. With respect to transistors M_3 and M_4, the high V_{DSsat} is due to the lower g_m that is needed to achieve an input impedance of about 300 Ω, as desired. Regarding the load resistance R_L (transistors M_5 and M_6), a value of approximately 724 Ω was obtained for the desired voltage drop of $V_{R_L} = 600$ mV. As expected, these transistors operate at the triode region. If passive resistors were used, $R_L = 600\,\text{mV}/1.5\,\text{mA} = 400\ \Omega$, resulting in a lower voltage gain and output impedance, and in a higher NF.

As shown in Fig. 4.5, the LNA input impedance is about 74 Ω for low frequencies and starts to decrease at higher frequencies, achieving the value of 60 Ω at 1 GHz, which is different from the target (Eq. (4.4)). This difference is mainly due to the fact that the output impedance of the CG transistor ($r_{ds,CG}$) is not much larger than the input impedance of the output transistors of the cascode stage (R_{casc}), as assumed in (4.4). This leads to an increase of the LNA input impedance, as stated in (4.2). The decrease of the LNA input impedance for higher frequencies is related

Table 4.1 LNA parameters (CMOS 130 nm)

Transistor	W (μm)	L (μm)	Region	I_D (mA)	V_{DSsat} (V)	g_m (mS)
M_1	75.2	0.12	Active	1.50	109.6	20.1
M_2	230.4	0.12	Active	1.52	77.8	27.3
M_3	5.6	0.12	Active	1.50	298.1	3.8
M_4	5.6	0.12	Active	1.52	301.2	3.7
M_5	7.2	0.12	Triode	1.50	−736.7	1.9
M_6	7.2	0.12	Triode	1.52	−737.5	1.9

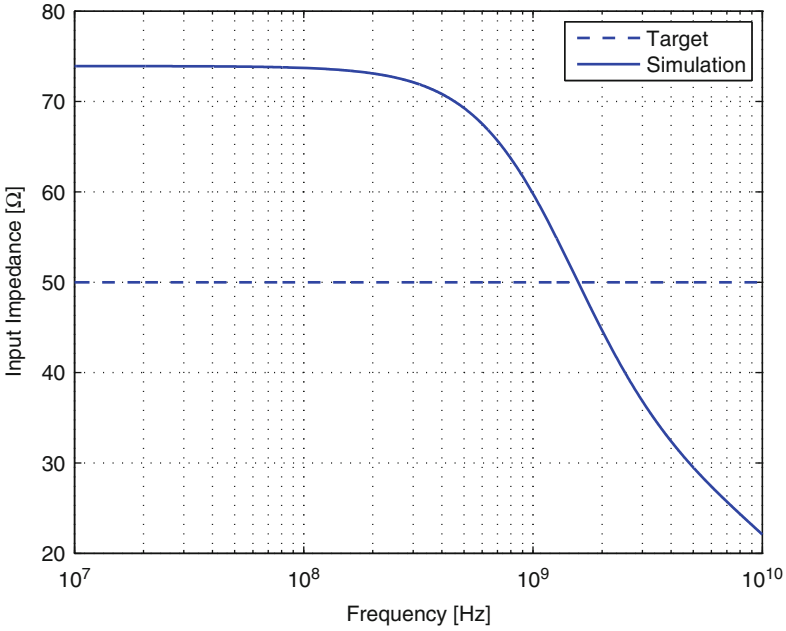


Fig. 4.5 LNA input impedance

with the parasitic capacitances of the transistors, that were neglected in Sect. 4.1.1. However, despite this deviation from the desired value, $S_{11} < -10$ dB was obtained for frequencies below 3.6 GHz, as shown in Fig. 4.6, which means that the input of the LNA is matched to the antenna's impedance for these frequencies.

The LNA voltage gain, illustrated in Fig. 4.7, is approximately 27.4 dB for low frequencies. The LNA has a bandwidth of 2.36 GHz and for this design a working band between 300 MHz (due to NF as will be explained) and 1 GHz was considered, which is the frequency where the gain begins to drop significantly.

The low bandwidth (comparing with similar designs [21, 36]) is related with the load PMOS devices, as explained before, and with the use of cascoded stages that also contribute with parasitic capacitances to the output node, decreasing the dominant pole frequency. The difference between the theoretical and simulated voltage gain is explained by the output impedance. In (4.6) it was assumed that $R_{cx} >> R_L$, which does not apply to the simulations and, as consequence, the voltage gain is reduced, because the two resistances are in parallel. Also, the parasitic capacitances of the cascode stages (ignored in the theoretical analysis) have a negative influence on the circuit's voltage gain, due to the reduction of these stages output impedance (r_{Cx}).

The LNA NF is below 1.84 dB for the working band (300 MHz–1 GHz), as shown in Fig. 4.8, which is a very acceptable value for this kind of LNA. Below 300 MHz, the NF is higher due to the effect of the flicker noise (explained in Sect. 2.1.4.2)

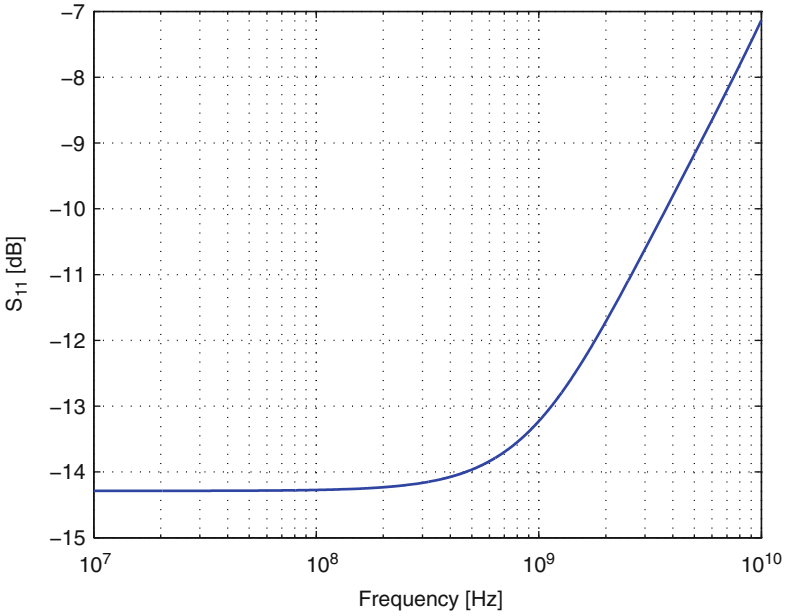


Fig. 4.6 LNA S_{11} parameter

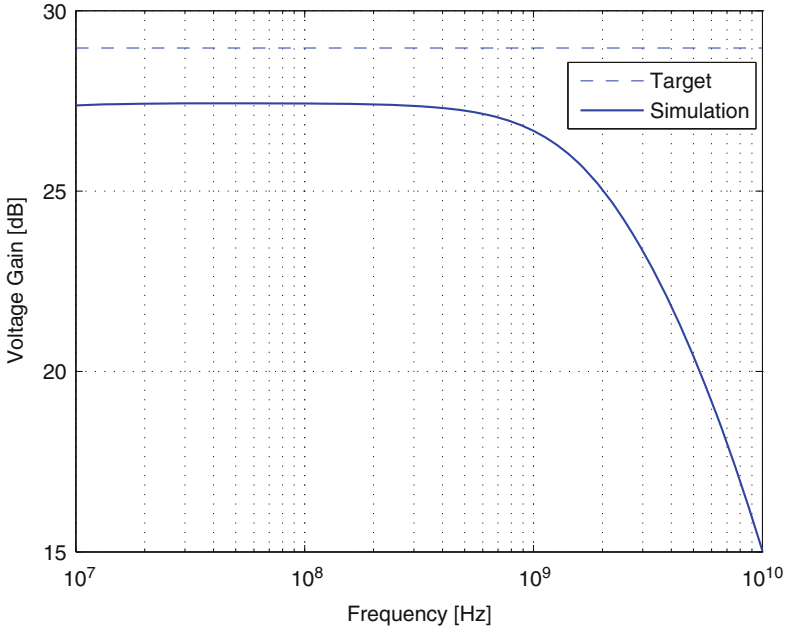


Fig. 4.7 LNA voltage gain

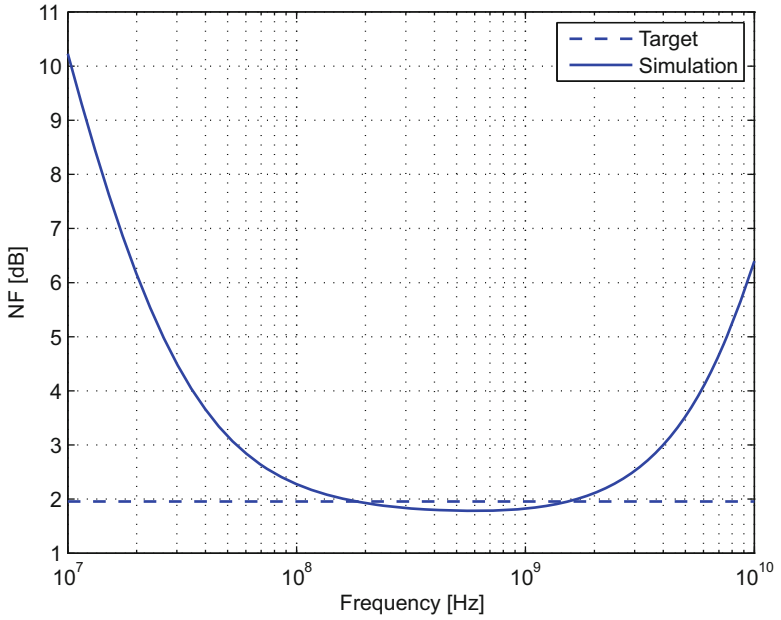


Fig. 4.8 LNA noise figure

and the filter composed by C_F and R_F. For high frequencies it increases, mainly as a consequence of the reduction of the voltage gain and because the gain of both stages becomes unbalanced. For the theoretical expression (Eq. (4.37)) the noise excess factor (γ) was considered equal to one, due to the short channel effects of transistors that are a consequence of using the minimum channel length allowed by the technology. The target (1.96 dB) and the obtained NF at the LNA working band are quite similar, which proves that the flicker noise is negligible at high frequencies, since it was not considered in the theoretical equation. The higher NF obtained in the theoretical analysis, comparing with the simulation results, is explained by the use of load PMOS devices in the simulated circuit, which decreases the LNA noise contributions as mentioned before.

Concerning linearity, the LNA has an IIP2 $= -2.2$ dBm (Fig. 4.9) and an IIP3 $= -9.6$ dBm (Fig. 4.10). To perform this simulation, two pure sinusoids were applied at the LNA input, spaced 20 MHz from each other, $f_1 = 600$ MHz and $f_2 = 620$ MHz. As expected, due to the high voltage gain, IIP2 and IIP3 are below 0 dB. Also, the nonlinearities of the active loads, referred in Sect. 4.1.4, contribute to the degradation of the LNA linearity.

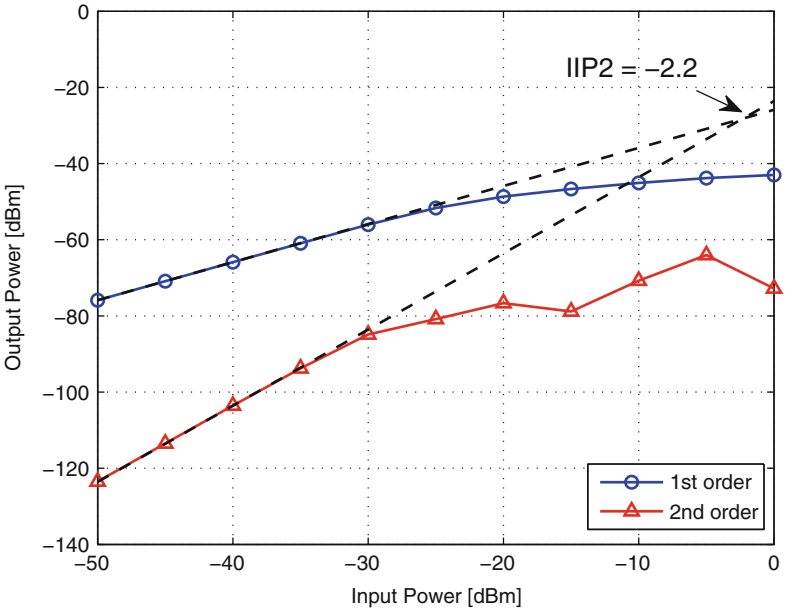


Fig. 4.9 LNA IIP2

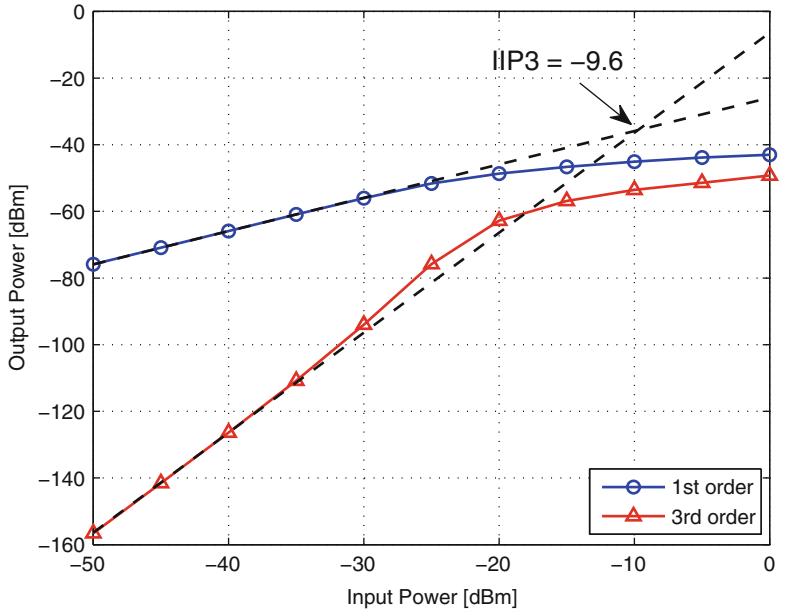


Fig. 4.10 LNA IIP3

4.3 Circuit Implementation Using CMOS 65 nm

In order to study the advantages and disadvantages of CMOS 130 nm and CMOS 65 nm technologies, comparing with each other, and since the ΣΔM that is integrated in the receiver chain was designed in CMOS 65 nm, the LNA was also designed using this technology. This circuit was dimensioned having the same constraints as of the 130 nm circuit. The only difference is the input impedance of the cascode devices that was chosen to be approximately 100 Ω, which makes the circuit easier to dimension due to the g_m constraints explained in the previous section. Also, it was chosen $V_{B,CG} = 560\,\text{mV}$, $V_{B,CS} = 347\,\text{mV}$ and $V_{B,Casc} = 980\,\text{mV}$. Obviously, these values depend on the circuit characteristics and, since the technologies are different, the bias voltages need to be different. To allow a direct comparison between the circuits of both technologies, the transistors length was chosen as 120 nm, as well as in the previous section.

Table 4.2 shows the transistors dimensions for the LNA developed in 65 nm technology and their DC operating points.

The analysis that was made in the previous section is still valid for this circuit, since the LNA response and characteristics are the same. The obtained simulation results are given in Table 4.3.

A load resistance $R_L \approx 770\,\Omega$ and a bandwidth of approximately 4.5 GHz were obtained. The bandwidth increase, comparing with the 130 nm circuit, is related with the transistors switching frequency that is much higher for the CMOS 65 nm technology due to the smaller parasitic effects and allowed channel lengths.

Table 4.2 LNA parameters (CMOS 65 nm)

Transistor	W (μm)	L (μm)	Region	I_D (mA)	V_{DSsat} (V)	g_m (mS)
M_1	86	0.12	Active	1.50	73.1	19.8
M_2	120	0.12	Active	1.51	61.0	22.1
M_3	20	0.12	Active	1.50	145.6	9.9
M_4	20	0.12	Active	1.51	146.0	9.9
M_5	5.85	0.12	Triode	1.50	−785.2	1.7
M_6	5.85	0.12	Triode	1.51	−785.3	1.7

Table 4.3 LNA simulation results (CMOS 65 nm)

Freq. (GHz)	Volt. gain (dB)	NF (dB)	S_{11} (dB)	IIP2[a] (dBm)	IIP3[a] (dBm)	Power (mW)	V_{DD} (V)	Tech. (nm)
0.3–1	28.9 ± 0.1	< 4	< -19	0	−14.1	3.6	1.2	65

[a] Simulation performed with $f_1 = 600\,\text{MHz}, f_2 = 620\,\text{MHz}$

Table 4.4 LNA simulation results

Tech. (nm)	Freq. (GHz)	Volt. gain (dB)	NF (dB)	S_{11} (dB)	IIP2[a] (dBm)	IIP3[a] (dBm)	Power (mW)	V_{DD} (V)
130	0.3–1	27.0 ± 0.4	< 1.84	< -13.2	-2.2	-9.6	3.6	1.2
65	0.3–1	28.9 ± 0.1	< 4.0	< -19	0	-14.1	3.6	1.2

[a] Simulation performed with $f_1 = 600\,\text{MHz}, f_2 = 620\,\text{MHz}$

4.4 Discussion

The equations derived in Sect. 4.1 are intended to help to dimension the circuit, but do not take into account the body effect of the CG transistor, the short-channel effects, and the parasitic capacitances of transistors, which have influence on the circuit performance. Regarding the parasitic capacitances, which have a large influence on the LNA bandwidth, they can be reduced by decreasing the transistors size, if a faster circuit is desired. For example, the largest capacitance of a MOSFET, C_{gs}, is approximately given by Carusone et al. [11]

$$C_{gs} \cong \frac{2}{3} WLC_{ox}, \tag{4.41}$$

where C_{ox} is the gate capacitance per unit area. On the other hand, to avoid short channel effects it is necessary to increase the transistor's channel length, which reduces the maximum operating frequency, since $f \propto 1/L^2$.

However, despite the differences between the theoretical and simulation results, due to the approximations, the performance of the LNA is within the expectations. A table with the LNA key parameters, for the circuits using both 130 and 65 nm CMOS technologies, is presented below (Table 4.4).

Since the 65 nm circuit's resistance R_L and the output impedance of the cascode devices are higher, the voltage gain of this LNA is higher, comparing with the LNA developed in 130 nm. The obtained NF for the 65 nm is more than the double of with the 130 nm circuit. This discrepancy is related with the technology properties and the BSIM models that were used in the Cadence simulations, which are different for the two technologies and need to be studied in order to understand this effect. Both circuits are matched to the antenna's impedance, as expected. Due to the higher gain, IIP_3 of the 65 nm circuit is poorer than that of the 130 nm circuit, as explained in Sect. 2.1.5.2. The low IIP_3 of this kind of LNA is related to the nonlinearities of the load devices and the circuit's high gain. Thus, it is possible to conclude that both circuits can accomplish the desired function but the 130 nm circuit is much better in terms of NF and IIP_3, although its voltage gain and IIP_2 are slightly lower.

Chapter 5
High-Q Bandpass Filter

In order to attenuate out-of-band interferers that can corrupt the signals at the receiver's AFE, specially by saturating the LNA, an integrated high-Q BPF, based on [3–6], is employed in this work. As referred in Sect. 3.4, this filter is based on a passive current-driven mixer (introduced in Sect. 3.2.2), which has very interesting properties related to impedance transformation. For example, if the filter's baseband impedance is a low-Q LPF, the filter will be a high-Q BPF centered at the LO frequency, ω_{LO}, as shown in Fig. 5.1.

Due to this characteristic, the resulting filter exhibits high impedance for the desired frequencies (near ω_{LO}) and offers a low impedance path to interferers that are located outside the filter's cutoff frequency [37]. This behavior makes this circuit ideal for wideband receivers in which it is desirable to have high-Q BPFs than can be precisely tuned according to the input signal's frequency.

This chapter is structured as follows: a theoretical analysis of the filter is made and the main equations for its characterization are derived and validated by simulation. Both single-ended and differential versions of the filter are presented.

5.1 Theoretical Analysis

The basic structure of the proposed high-Q BPF is shown in Fig. 5.2a. This filter is driven by a LO that produces rail-to-rail non-overlapped square waves with a frequency equal to ω_{LO} and a duty cycle of $1/M$, as shown in Fig. 5.2b, where M is the number of the filter's phases. The pulse width of each phase is equal to T_{LO}/M, where T_{LO} is the clock's period. This means that only one of the M switches is ON at a specific clock phase, i.e. the current that flows to one of the baseband impedances is equal to the RF current, if the corresponding switch is ON, or zero, if it is OFF. Usually, the impedance Z_{BB} is a capacitor (C_{BB}), as explained before. However, if

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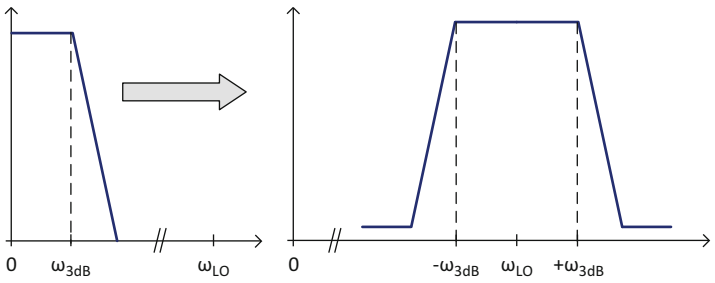

Fig. 5.1 Low-pass to band-pass transformation

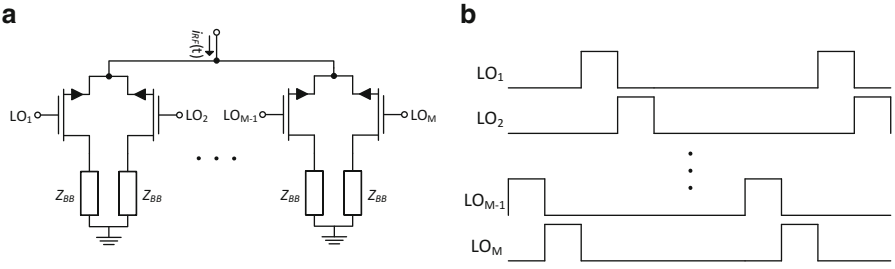

Fig. 5.2 (**a**) Single-ended N-phase High-Q BPF. (**b**) LO waveforms for a N-phase filter

higher bandwidth is required, a parallel *RC* should be used to have a lower droop in the filter response across the desired band [3].

Assuming that all the switches are ideal, with an ON resistance equal to R_{SW}, the filter's input impedance is given by Mirzaei et al. [4]

$$\begin{aligned} Z_{in}(\omega) =& R_{SW} + \frac{1}{M} Z_{BB}(\omega) + \frac{M}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) \\ & \times [Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})] \\ & + \frac{M}{4\pi^2} \sin^2\left(\frac{2\pi}{M}\right) \times [Z_{BB}(\omega - 2\omega_{LO}) + Z_{BB}(\omega + 2\omega_{LO})] \\ & + \frac{M}{9\pi^2} \sin^2\left(\frac{3\pi}{M}\right) \times [Z_{BB}(\omega - 3\omega_{LO}) + Z_{BB}(\omega + 3\omega_{LO})] + \ldots \end{aligned} \tag{5.1}$$

From the previous equation is possible to conclude that the input impedance is a translation of Z_{BB} to the integer harmonics of the LO, with a scaling factor that is inversely proportional to M, as shown in Fig. 5.3.

To simplify the filter analysis, and since the desired signals are located near ω_{LO}, the DC and high order terms can be ignored, leading to

$$Z_{in}(\omega) \cong R_{SW} + \frac{M}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) \times [Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})]\,. \tag{5.2}$$

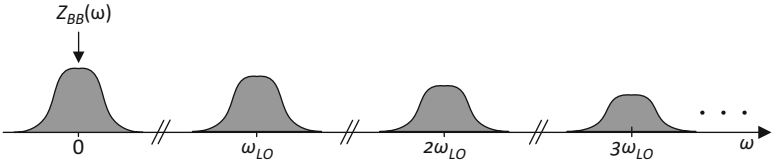

Fig. 5.3 Single-ended M-phase high-Q BPF input impedance spectrum

Given this approximation, the filter's input impedance is approximately equal to the baseband impedance Z_{BB} shifted to the LO frequency, in series with the switch resistance R_{SW}, resulting in a tunable BPF that is precisely controlled by the LO frequency, as desired. Due to this property, these kind of filters are very desirable in wideband receivers, in which the frequency of interest can vary significantly. As explained before, (5.2) shows that the low-Q baseband impedance is transferred to a high-Q RF impedance. This means that if Z_{BB} exhibits a very high impedance at DC the filter's impedance will be ideally infinite at ω_{LO} and, for frequencies far from the frequency of interest, the filter's impedance will be equal to R_{SW}, because Z_{BB} diminishes.

Regarding the number of phases, a higher M increases the filter in-band impedance, decreases the folding components gain and moves the closest folding frequency component to $(M-1)\omega_{LO}$, avoiding the folding of interferers situated in some harmonics of ω_{LO} on top of the desired signal [4]. This means that, to avoid image related problems, $M \geq 4$, otherwise the closest folding frequency will be located at ω_{LO}. The main disadvantages of using a high M are the increase of the number of switches, which increases the filter noise contributions, and the increased complexity of the LO.

Since the switches are implemented with MOSFETs, operating in deep triode region ($V_{DS} \approx 0$), the channel region behaves like a voltage controlled resistor R_{SW} that, for a NMOS device, is expressed by Carusone et al. [11]

$$R_{SW} \approx r_{ds} = \left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1}_{|V_{DS}=0} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{Tn})} \tag{5.3}$$

For a constant transistor length (L), by increasing the transistor width (W) it is possible to decrease the resistance R_{SW} and, consequently, the impedance $Z_{in}(\omega)$ also decreases for frequencies distant from ω_{LO} (at ω_{LO} the effect of R_{SW} is neglected because the filter's impedance is very high), as expressed by (5.2). Since the filter's out-of-band impedance is equal to R_{SW}, this resistance should be very low in order to obtain the maximum interferers attenuation. However, from (2.20) is possible to conclude that if R_{SW} is decreased, the thermal noise current generated by the filter increases, leading to a higher filter noise contribution. The main advantage of operating deep into the triode region is that, due to this region properties, the resulting filter is very linear.

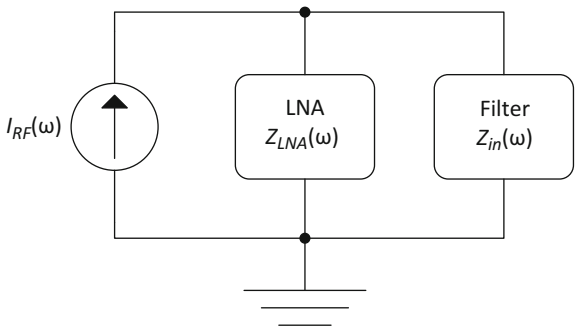

Fig. 5.4 Equivalent circuit of LNA input connected to the proposed high-Q BPF

5.1.1 Single-Ended Version

A 4-phase single-ended high-Q BPF, identical to that presented in Fig. 5.2, is proposed to be employed at the input of the LNA studied in Chap. 4. This filter was designed to filter the input signals, attenuating undesired signals located outside of the band of interest, and to contribute to the LNA input impedance matching.

Consider that the LNA has an equivalent input impedance $Z_{LNA}(\omega)$ and is in parallel with the proposed filter, as shown in Fig. 5.4. If a current $I_{RF}(\omega)$ is flowing into the circuit (Norton equivalent) the ratio between the RF voltage and the RF current is given as

$$\frac{V_{RF}(\omega)}{I_{RF}(\omega)} = Z_{LNA}(\omega) \parallel Z_{in}(\omega). \tag{5.4}$$

Substituting $Z_{in}(\omega)$ by (5.2), and for M phases,

$$\frac{V_{RF}(\omega)}{I_{RF}(\omega)} \cong Z_{LNA}(\omega) \parallel \left(R_{SW} + \frac{M}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) \times [Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})] \right). \tag{5.5}$$

This means that for frequencies near ω_{LO} the equivalent node impedance is approximately equal to $Z_{LNA}(\omega)$, because the filter impedance is very high (ideally it is infinite) as explained before, and the filter will not have much impact on the desired RF signal. For frequencies far from w_{LO} the node impedance is $Z_{LNA}(\omega) \parallel R_{SW}$, which is approximately equal to R_{SW} considering that $R_{SW} \ll Z_{LNA}(\omega)$. This small impedance attenuates undesired out-of-band interferers.

Considering a particular case where $Z_{LNA}(\omega)$ is a resistor R_{LNA} and the filter's baseband impedances are capacitors C_{BB}, (5.5) can be written as [4]

$$\frac{V_{RF}(\omega)}{I_{RF}(\omega)} \cong \frac{R_{LNA}}{R_{LNA} + R_{SW}} \times \left[R_{SW} + \frac{\frac{M^2}{\pi^2} \sin^2\left(\frac{\pi}{M}\right) R_{LNA}}{1 + jM(R_{LNA} + R_{SW}) C_{BB}(\omega - \omega_{LO})} \right]. \tag{5.6}$$

From (5.6) it is possible to verify that the resulting filter is a BPF with the equivalent LPF bandwidth given by

$$\omega_{3dB} \cong \frac{1}{M(R_{LNA} + R_{SW})C_{BB}}. \tag{5.7}$$

Considering that the filter is symmetric, as shown in Fig. 5.1, its bandwidth is equal to $2 \cdot \omega_{3dB}$ and the Q factor is $Q = \omega_{LO}/(2 \cdot \omega_{3dB})$, as referred in Sect. 3.4. By increasing M it is possible to decrease the bandwidth and increase the filter attenuation steepness (Q) by a factor M. The bandwidth also depends on the LNA input impedance and the filter's switches resistance.

For the specific case of $M = 4$, that corresponds to the filter used in this work, and considering that $R_{LNA} \gg R_{SW}$, the transfer function at ω_{LO} is

$$\frac{V_{RF}(\omega_{LO})}{I_{RF}(\omega_{LO})} \cong \frac{R_{LNA}\left(R_{SW} + \frac{8}{\pi^2}R_{LNA}\right)}{R_{LNA} + R_{SW}} \approx \frac{8}{\pi^2}R_{LNA}. \tag{5.8}$$

This means that, comparing with the LNA circuit without the BPF, the circuit gain drops by $8/\pi^2 = -1.82\,\text{dB}$ at ω_{LO}. This reduction of the gain is due to the higher harmonics effect [3], referred in (5.4), that were ignored during the filter analysis and makes the impedance seen from the filter's input finite, contrarily to the expected. If M takes a larger value, the circuit input impedance is higher, as stated in (5.6), which means that for higher M the effect of high order harmonics is less noticeable. For frequencies far from ω_{LO} the input impedance is $R_{LNA} \parallel R_{SW}$, as shown above, which means that the maximum out-of-band attenuation depends of R_{SW}. To achieve the filter maximum performance R_{SW} should be close to zero and R_{LNA} should be much larger than R_{SW}, to achieve the maximum gain at ω_{LO}, as shown by (5.8), and the maximum attenuation at undesired frequencies.

5.1.2 *Differential Version*

At the differential nodes of the LNA, a differential version of the high-Q BPF, shown in Fig. 5.5, can be employed. This filter has the same function as the single-ended version, but since it is differential, it presents the double of the input impedance. Also, since the number of switches is doubled, the filter noise contributions increase.

The input impedance of the differential filter is given by Mirzaei et al. [4]

$$\begin{aligned} Z_{in}(\omega) = {} & 2R_{SW} + \frac{2M}{\pi^2}\sin^2\left(\frac{\pi}{M}\right) \times [Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})] \\ & + \frac{2M}{9\pi^2}\sin^2\left(\frac{3\pi}{M}\right) \times [Z_{BB}(\omega - 3\omega_{LO}) + Z_{BB}(\omega + 3\omega_{LO})] \\ & + \frac{2M}{25\pi^2}\sin^2\left(\frac{5\pi}{M}\right) \times [Z_{BB}(\omega - 5\omega_{LO}) + Z_{BB}(\omega + 5\omega_{LO})] + \ldots \end{aligned} \tag{5.9}$$

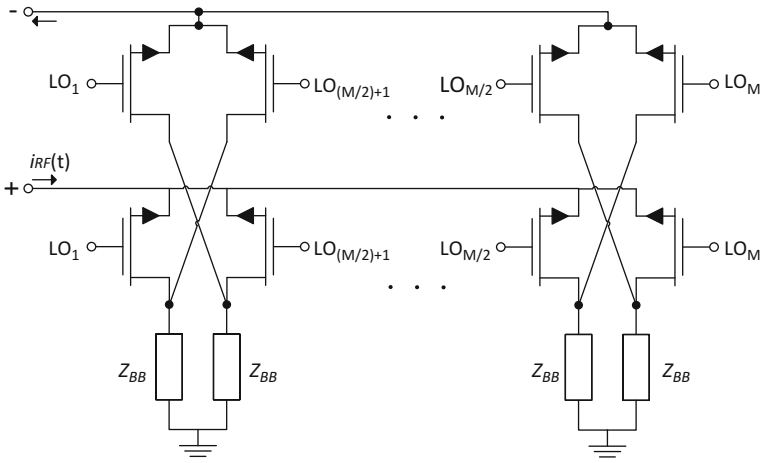

Fig. 5.5 Differential N-phase High-Q BPF

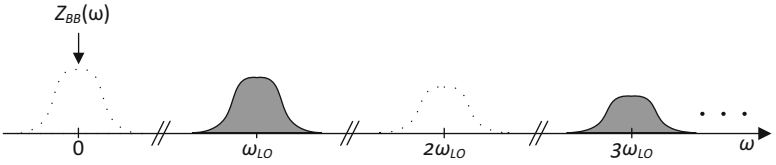

Fig. 5.6 Differential M-phase high-Q BPF input impedance amplitude response

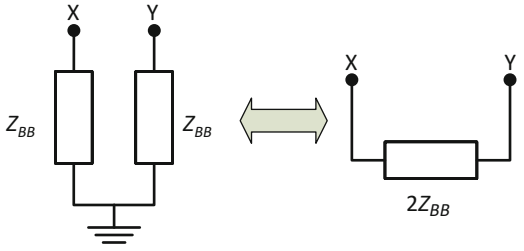

Fig. 5.7 Differential N-phase High-Q BPF with floating impedances

which means that the differential filter cancels all the even harmonics (including DC), so the impedance around these harmonics is approximately zero (assuming $R_{SW} \approx 0$). The input impedance amplitude response is shown in Fig. 5.6.

An interesting property of this filter is that the baseband impedances $Z_{BB}(\omega)$ of two inverse phases (with a phase offset of 180°) can be replaced by a floating impedance of value $2Z_{BB}(\omega)$, as shown in Fig. 5.7. This is very useful, specially if the baseband impedances are capacitors (C_{BB}) because two capacitors can be replaced by a capacitor of value $C_{BB}/2$, which results in a reduction of the capacitors area by a factor four [4].

5.2 Circuit Implementation

To verify if the filter has the expected response, a test setup with the following parameters was created: $R_{LNA} = 100\ \Omega$, $R_{SW} = 10\ \Omega$, $C_{BB} = 50$ pF, $M = 4$ and $f_{LO} = 600$ MHz. The LOs produce the waveforms[1] shown in Fig. 5.2b, with 1.2 Vpp, an offset of 600 mV and rise and fall times of 10 ps. The employed technology is CMOS 130 nm. Figure 5.8 shows the obtained results of the single-ended version of the filter, as well as the expected response, derived in Sect. 5.1.

As shown in Table 5.1, the obtained results are as expected. The differences of the simulated and expected results are mainly due to the approximations that were made in the derivation of (5.6). If a higher number of phases (M) is used, the simulated and expected results become more identical because, as referred before, for higher M, the effect of the other harmonics (including DC) is less noticeable.

From this simulation is possible to conclude that the filter exhibits a high Q, which is very difficult to achieve using conventional external filters, as stated in Sect. 3.4.

In order to understand the behavior of the studied topologies a simulation was made with the previous setup, but with $f_{LO} = 300$ MHz (Figs. 5.9 and 5.10). As

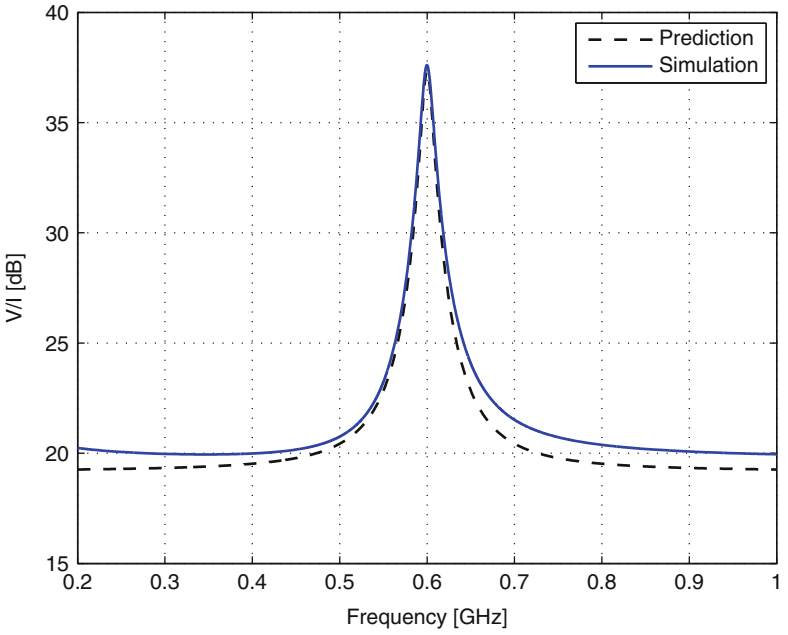

Fig. 5.8 Prediction of (5.6) *vs.* simulation results for single-ended BPF

[1] All of the LO waveforms used in this work are as shown in Fig. 5.2b with different values of f_{LO}.

Table 5.1 Single-ended high-Q BPF results

	Bandwidth (MHz)	Q	Z_{in} @ f_{LO} (Ω)	OOB Z_{in} (Ω)
Prediction	14.5	41.4	82.8	9.1
Simulation	16.1	37.3	75.9	10

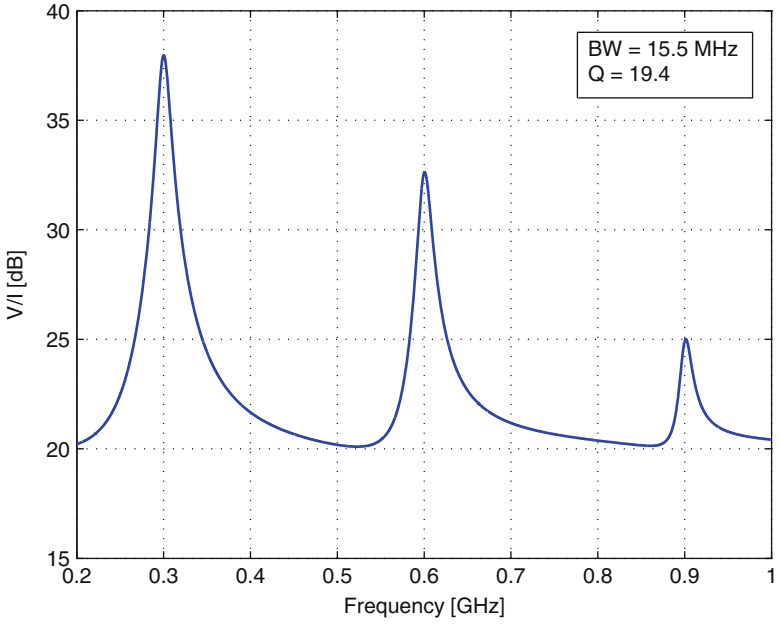

Fig. 5.9 Single-ended BPF response with $f_{LO} = 300\,\text{MHz}$

expected, the single-ended filter input impedance is similar to the presented in Fig. 5.8 and the differential filter input impedance is approximately the double of the single-ended version, as shown by (5.9). Also, the bandwidth of the differential filter is the double of the single-ended for the same input circuit, which means that the differential filter has a lower Q factor, for the same setup values.

As shown in Fig. 5.10, the differential filter cancels the even order harmonics, as referred in Sect. 5.1.2, leading to a lower degradation of the signal at the desired frequency component (f_{LO}) that occurs due to the high order harmonics effects.

5.3 Discussion

The presented high-Q BPF is a very good solution to employ in an integrated RF receiver, due to the circuit simplicity and reduced number of active devices. This circuit performs the conversion from a low-Q LPF to a high-Q BPF that is precisely

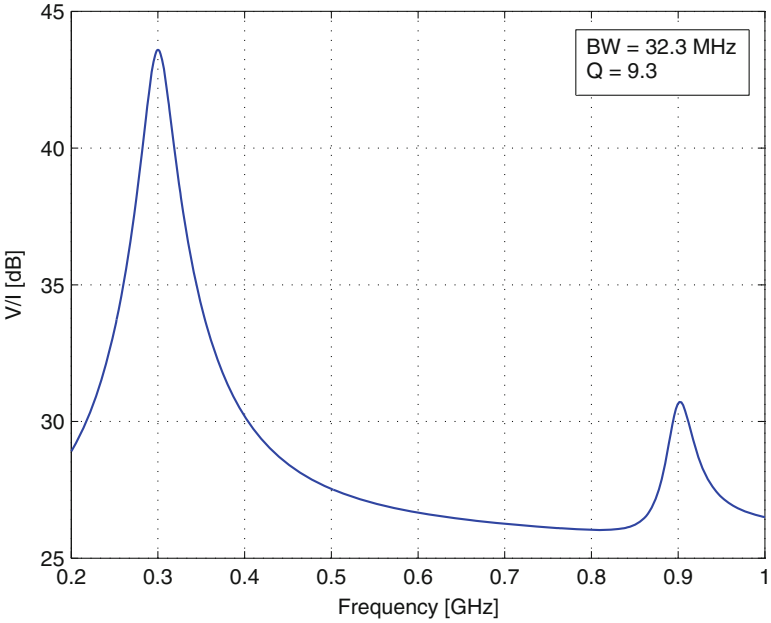

Fig. 5.10 Differential BPF response with $f_{LO} = 300\,\text{MHz}$

controlled by the LO waveform, with a minimum penalty in the overall circuit voltage gain. This allows the suppression of undesired interferers at out-of-band frequencies, avoiding the use of external filters that require an external chip that occupies more area and is more expensive. Since it is passive, this filter has almost no power consumption and no flicker noise, leading to very low noise contributions to the receiver.

For single-ended nodes of the receiver, a single-ended version of the filter should be used, and for differential nodes a differential filter is required. The main advantages of the differential filter are the full cancellation of the even order harmonics and the doubling on input impedance, compared with the single-ended version. However, since this circuit has more active devices for the same number of phases, its complexity and noise contributions are higher and the Q factor is lower.

Regarding the number of phases, increasing M increases the filter in-band impedance, decreases the folding components gain, moves the closer folding frequency component to $(M-1)\omega_{LO}$ and increases the number of filter's active devices (increasing the filter noise contributions) and the LO complexity. In this work $M = 4$ is used, which is the best compromise between the filter overall performance and complexity.

Chapter 6
Complete Receiver

As mentioned above, an RF receiver performs the conversion of an RF input signal to a signal with lower frequency (IF) that can be handled by an ADC and thereafter be processed by a digital circuit. A wideband low-IF architecture, shown in Fig. 6.1, was chosen for this work due to its simplicity and the possibility to allow its full integration in one chip, as explained in Sect. 2.2.3.

The proposed receiver consists of the LNA of Chap. 4 with integrated filtering, which amplifies the desired input signals and filters unwanted signals, a current-driven mixer that converts the amplified RF signal to a baseband signal, a end block (B) and a LO that was not studied in this work (the interested reader may refer to [15] for information on LOs). The end block can be either a TIA (studied in Sect. 6.3), which converts the current IF signal to a voltage signal, or a $\Sigma\Delta$ modulator (studied in Sect. 6.5) that directly converts the current IF signal to the digital domain. The receiver that uses the TIA was developed in CMOS 130 nm technology and produces a baseband voltage that is proportional to the RF signal. The 65 nm receiver has the same characteristics of the 130 nm circuit but instead of a TIA it uses a current-mode $\Sigma\Delta$M. Also, it uses a current buffer to perform the interface between the mixer's output and the $\Sigma\Delta$M input, as will be explained in Sect. 6.4.

This chapter is structured as follows: first, the block composed by the LNA studied in Chap. 4 and the high-Q BPF studied in Chap. 5 are reviewed and validated through simulation and then the results that were obtained for both technologies are compared. Then, the mixer and the TIA are reviewed and the complete receiver, composed by those three blocks, is reviewed. Finally, the current-buffer that performs the interface between the mixer and the $\Sigma\Delta$M is reviewed and the complete receiver using the $\Sigma\Delta$M at the receiver AFE output is analyzed.

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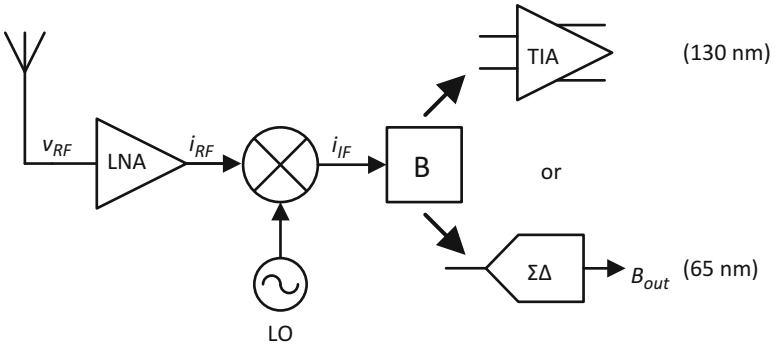

Fig. 6.1 Complete receiver

6.1 Balun-LNA with Integrated Filtering

One of the major concerns in modern RF receivers is the attenuation of undesired interferers that can saturate the LNA. To overcome this problem, two high-Q BPF are integrated in the studied LNA circuit, as shown in Fig. 6.2.

The input filter consists of a single-ended high-Q BPF (studied in Sect. 5.1.1), that also contributes to impedance matching. The filter at the input of the cascode stages is a differential high-Q BPF (studied in Sect. 5.1.2). Both filters have four phases ($M = 4$).

As explained before, this block was developed in 130 and 65 nm CMOS technologies. In the next sections both circuits will be presented, studied and compared.

6.1.1 LNA with Integrated Filtering Using CMOS 130 nm Technology

For this specific circuit both filters were designed so that the complete block has a bandwidth of approximately 6 MHz. The filters component values are described in Table 6.1, where W and L are the switches dimensions, R_{SW} is the switches ON resistance and C_{BB} is the baseband capacitances value. The filters' behavior is much influenced by the transistors dimensions, as explained in Chap. 5. For example, if the switches resistance is large, the filter noise contributions will be small, but the filter's effect is less noticeable (less amplification at ω_{LO} and less attenuation of undesired signals), comparing with lower R_{SW} values. The chosen L is 120 nm, which is the minimum size allowed by the technology. Since the transistors operate as switches (triode region), the short channel effects are negligible and this size allows the devices to operate at the maximum speed, because the maximum operating frequency varies inversely with L^2.

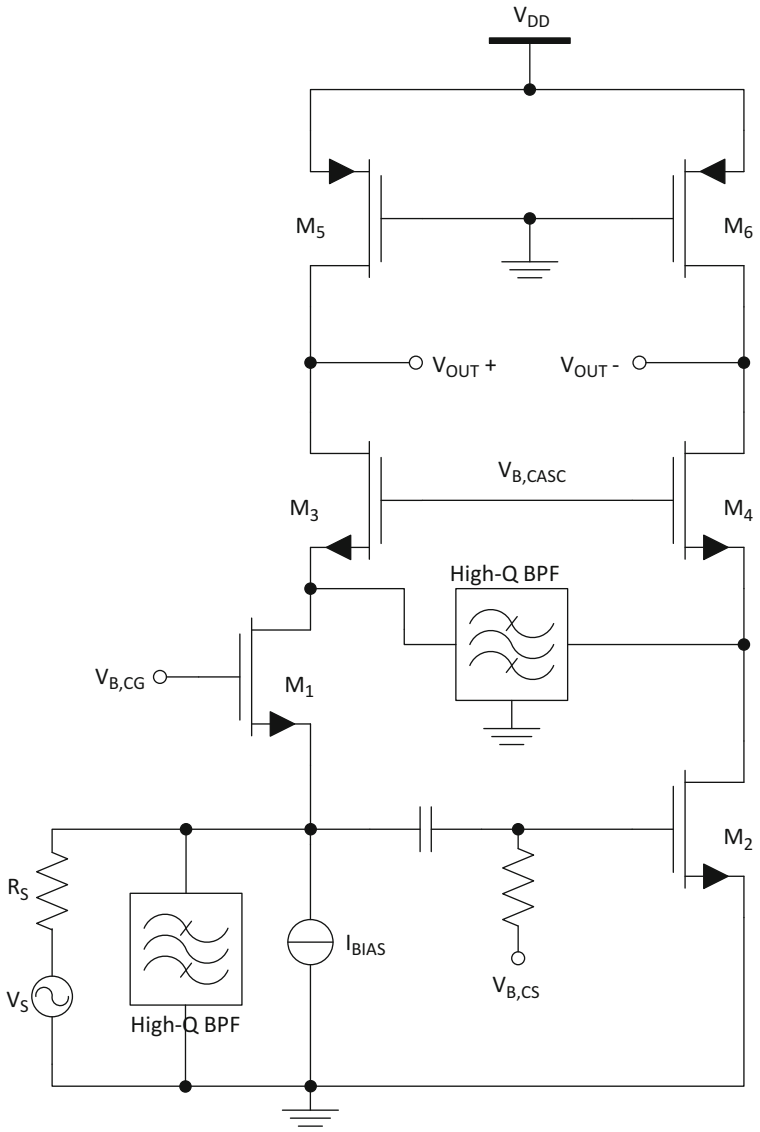

Fig. 6.2 Cascode balun-LNA with integrated filters

6.1.1.1 LNA Response

By connecting both filters to the LNA a frequency response similar to that shown in Fig. 5.8 is expected. Figure 6.3 shows the LNA voltage gain for three different LO frequencies: 300, 600 and 900 MHz. Due to the filters' properties, explained before, at frequencies near f_{LO} the input signal flows almost completely through the LNA

Table 6.1 Filters component values (CMOS 130 nm)

Filter	W (µm)	L (µm)	R_{SW} (Ω)	C_{BB} (pF)
Single-ended	16	0.12	28.6	200
Differential	8	0.12	74	55

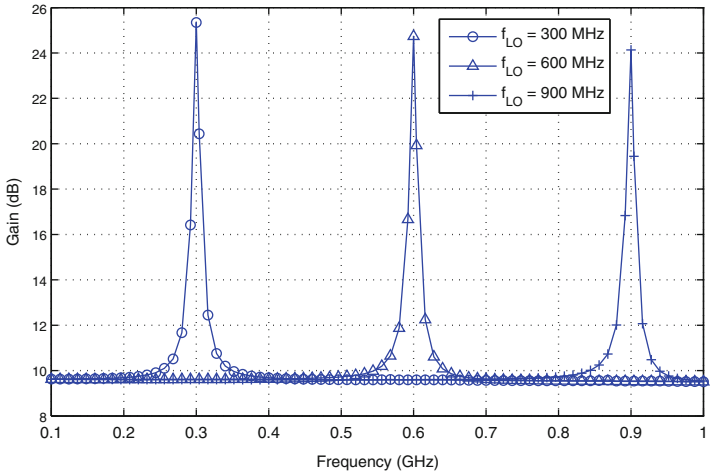

Fig. 6.3 LNA voltage gain for multiple values of f_{LO}, with both filters (CMOS 130 nm)

Table 6.2 LNA bandwidth and Q factor (CMOS 130 nm)

f_{LO} (MHz)	300	600	900
Bandwidth (MHz)	5.7	6.1	6.6
Q	52.6	98.4	136.4

transistors, since the filters' input impedance is very large. For frequencies far from f_{LO} the filters' impedance is much lower than the impedance of the LNA nodes, and consequently the signal flows almost completely through the filters, resulting in less amplification of undesired interferers. From the simulation it is possible to conclude that the LNA behaves like a BPF with a high Q factor, since it has a narrow bandwidth and is centered at a high frequency. The bandwidths and Q factors obtained are presented in Table 6.2.

As desired, the bandwidth is approximately 6 MHz for the entire LNA working band. The filter Q factor grows almost linearly with the frequency and presents high values, as expected. Since out-of-band signals are corrupted by the filters, the NF at those frequencies is very high, as shown in Fig. 6.4.

The S_{11} parameter has the same shape of NF, because for out-of-band frequencies the filters' impedance is very low (approximately R_{SW}) and, since the filters are in parallel with the LNA nodes, the equivalent input impedance is very low, resulting in a poor input matching and consequently a high S_{11}.

By using this technique is possible to employ a narrowband widely tunable balun-LNA, which means that the resulting circuit is a narrowband balun-LNA (with a

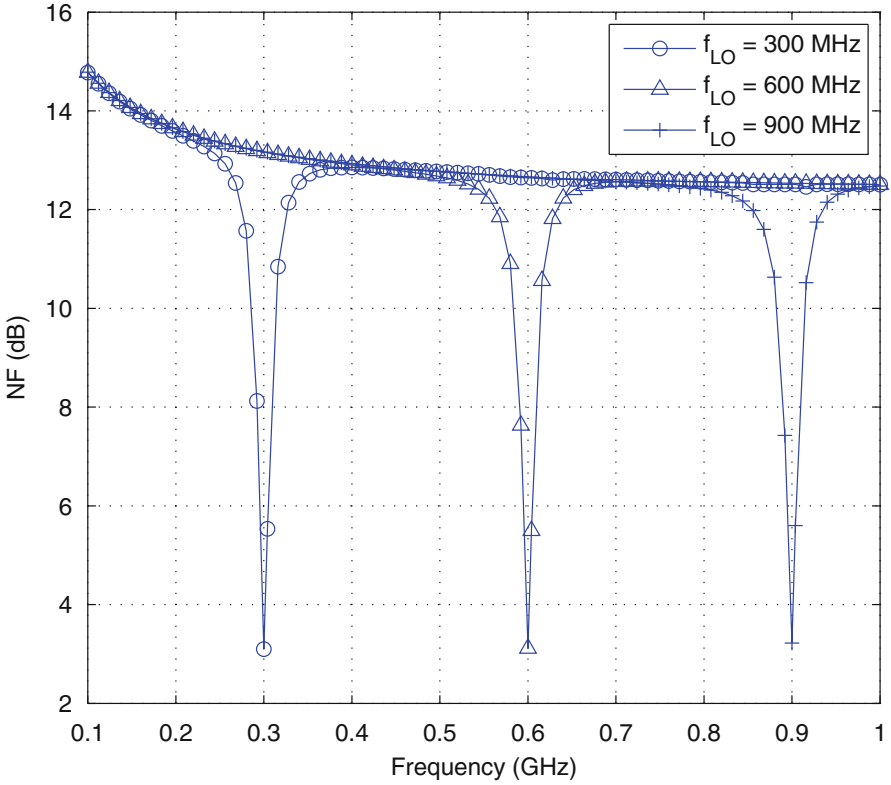

Fig. 6.4 LNA noise figure, for multiple values of f_{LO}, with both filters

bandwidth of about 6 MHz) that can be tuned to operate over the entire working band of the LNA of Chap. 4 (0.3–1 GHz), by programming the LO waveform, according to the RF input signal frequency.

6.1.1.2 LNA Frequency Sweep

In order to understand the filters' effect on the LNA response, a frequency sweep was performed, for the entire LNA working band, in order to analyze the different parameters—voltage gain, NF, S_{11}, IIP_2 and IIP_3. This frequency sweep was performed in three different configurations: using only the single-ended filter at the LNA input, using only the differential filter at the LNA cascode transistors input and using both filters.

Comparing the voltage gain at f_{LO} (Fig. 6.5) with the voltage gain of the LNA only (referred in Table 4.4) it is possible to conclude that, when both filters are used, the gain drop is about 3 dB in the worst case. This reduction of gain is related with the filter properties described in Sect. 5.1.1, i.e., due to the harmonics effect

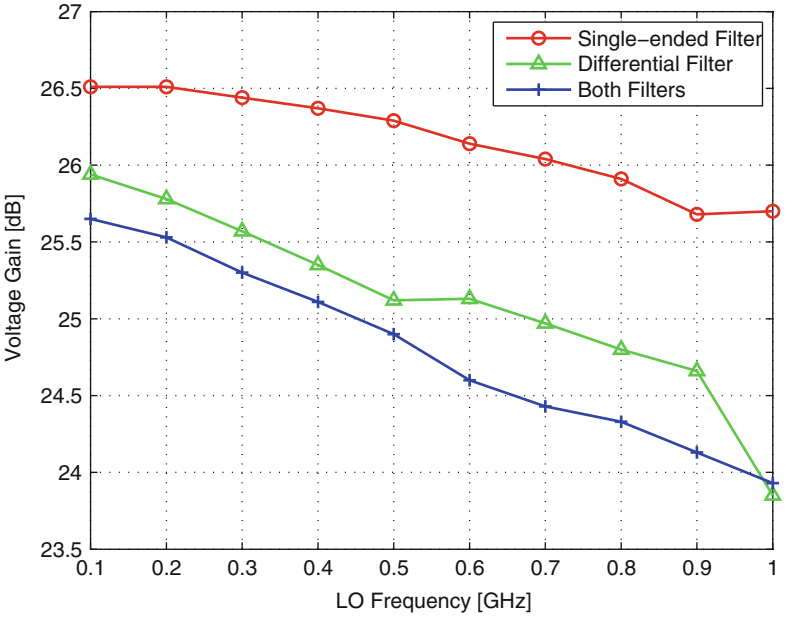

Fig. 6.5 LNA voltage gain at f_{LO}

Table 6.3 LNA out-of-band voltage gain

	Single-ended filter	Differential filter	Both filters
Voltage gain (dB)	21.5	14.7	9.6

the filters' impedance is not infinite at f_{LO}, as desired, and consequently the signal of interest does not flow completely through the LNA. Also, (5.8) neglects R_{SW} that obviously has an influence on the circuit voltage gain at this frequency. As expected, the voltage gain decreases with the increase of the number of filters. A solution to overcome this problem is to increase the number of phases of the filters, as explained before.

The out-of-band voltage gain (Table 6.3) is approximately 10 dB when both filters are used, for the entire LNA working band, which means that the undesired signals suffer an attenuation of approximately 14 dB, comparing with the signals at f_{LO}. One interesting property is that by increasing the number of filters the out-of-band gain suffers a large reduction, while the gain at f_{LO} is only slightly reduced. This means that if a higher interferers attenuation is desired, more filters can be included in the receiver's circuit, with a minor penalty in the voltage gain at the desired frequencies. As a consequence, the circuit's NF will increase.

Regarding the NF (Fig. 6.6), it is approximately 1.5 dB higher than the LNA without filters (Table 4.4), when both filters are used, and has the same shape of Fig. 4.8, due to the reasons explained before. As stated in Sect. 5.1, increasing the

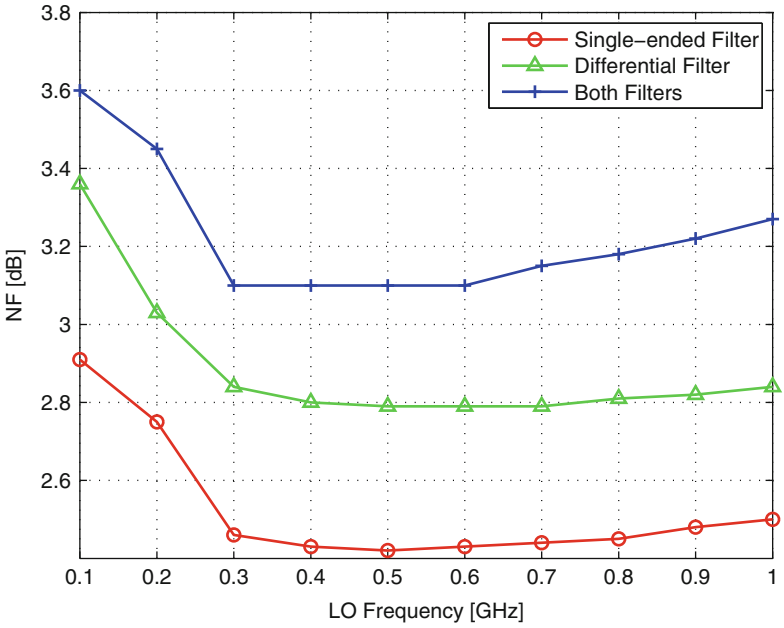

Fig. 6.6 LNA NF at f_{LO}

number of filters leads to an NF increase, due to the filters noise contributions. Also, the differential filter contributes with more noise than the single-ended filter due to the higher number of devices. The lower voltage gain (relatively to the LNA only) also increases the NF, as stated in (2.23).

Concerning the input impedance matching, Fig. 6.7 shows that the LNA is matched to the antenna's impedance for the entire working band, in the three configurations. When both filters are used $S_{11} < -17$ dB is obtained (that is 4 dB lower than the LNA alone). As shown in Fig. 6.7, the input filter improves significantly the impedance matching, as referred before, because it is in parallel with the LNA input. Thus, this filter components are limited to certain values because its impedance has a strong impact on the LNA input impedance.

In order to understand the influence of the filters on the even-order distortion and intermodulation effects, a two-tone test simulation was performed, with $f_{LO} =$ 600 MHz, to evaluate the Out-of-band (OOB) IIP2 and the OOB IIP3. For the IIP2 analysis the applied tones are at $f_1 = 700$ MHz and $f_2 = 1301$ MHz, and for the IIP3 analysis the tones are at $f_1 = 700$ and $f_2 = 799$ MHz. Thus, the intermodulation products are located at 601 MHz, i.e. 1 MHz apart from the LO frequency, which is inside the LNA bandwidth. An OOB IIP2 $= +9.4$ dBm and an OOB IIP3 $= -0.7$ dBm were obtained, which are significantly better than the values obtained for the LNA without filters (Table 4.4). These values are very acceptable for a wide number of applications like Global System for Mobile Communications (GSM) and DVB-H [38].

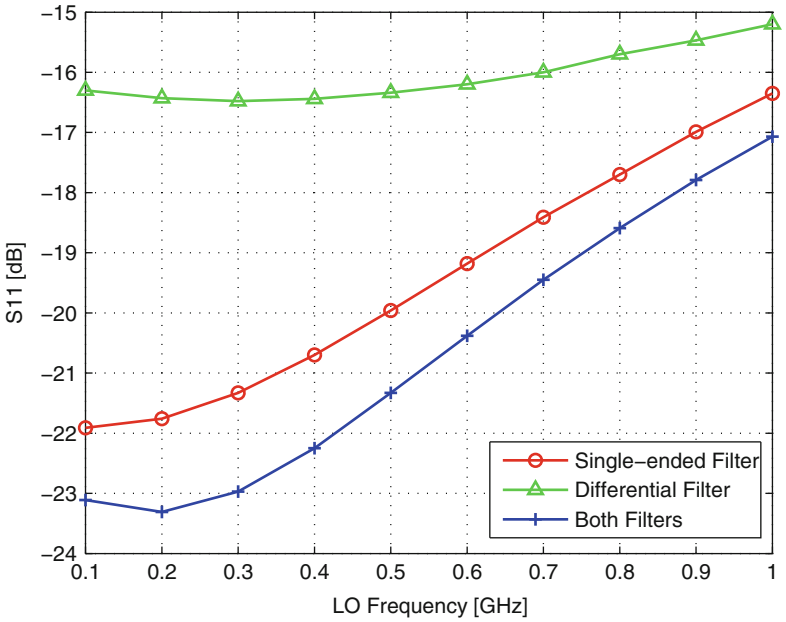

Fig. 6.7 LNA S_{11} at f_{LO}

Table 6.4 Filters component values (CMOS 65 nm)

Filter	W (µm)	L (µm)	R_{SW} (Ω)	C_{BB} (pF)
Single-ended	10	0.06	32.7	400
Differential	5	0.06	83.4	95

6.1.2 LNA with Integrated Filtering Using CMOS 65 nm

Since the technology used in the circuit of this subsection is different from the previous one, the component values need to be dimensioned again in order to achieve the desired performance and characteristics. However, the analysis that was made in the previous subsection is still valid, since the circuit is the same.

Regarding the bandwidth, a value of approximately 4.5 MHz was desired for the LNA with integrated filtering, which leads to the filters components values presented in Table 6.4.

The chosen length (L) is 60 nm, which is the minimum size allowed by the CMOS 65 nm technology. In order to verify the circuit's behavior, a simulation identical to those presented in Fig. 6.3 was made. The results are shown in Fig. 6.8.

As expected, the circuit has the same behavior as the one analyzed in the previous subsection. As referred in Sect. 4.4, the voltage gain of the 65 nm circuit is higher than the 130 nm circuit. Also, interferers suffer a lower attenuation, about 12 dB (comparing with 14 dB), because the switches impedances (R_{SW}) of this circuit are

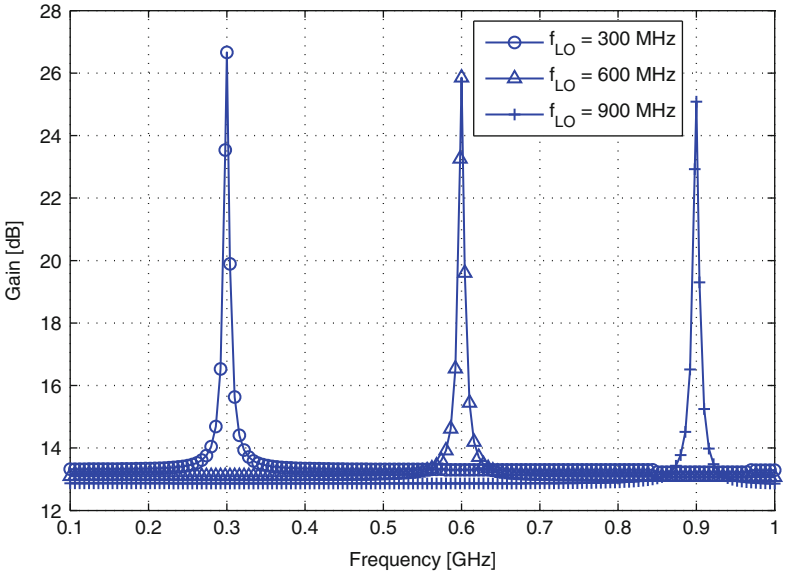

Fig. 6.8 LNA voltage gain for multiple values of f_{LO}, with both filters (CMOS 65 nm)

Table 6.5 Filtered LNA bandwidth and Q factor (CMOS 65 nm)

f_{LO} (MHz)	300	600	900
Bandwidth (MHz)	3.8	4.5	4.7
Q	79	133.3	191.5

Table 6.6 Narrowband balun-LNA simulation results (CMOS 65 nm)

Freq. (GHz)	V. gain (dB)	Atten.[a] (dB)	NF (dB)	S_{11} (dB)	OOB IIP2[b] (dBm)	OOB IIP3[c] (dBm)	Power (mW)	V_{DD} (V)
0.3–1	25.5 ± 1[d]	> 12	< 6.3[d]	< -17[d]	$+11.9$	$+6.9$	3.6	1.2

[a]Out-of-band attenuation
[b]$f_{LO} = 600\,\text{MHz}, f_1 = 700\,\text{MHz}, f_2 = 1301\,\text{MHz}$
[c]$f_{LO} = 600\,\text{MHz}, f_1 = 700\,\text{MHz}, f_2 = 799\,\text{MHz}$
[d]At f_{LO}

higher, and from (5.6) it is known that the out-of-band impedance of the studied high-Q BPF is given by $R_{LNA} \parallel R_{SW}$. Table 6.5 presents the obtained bandwidths and Q factors.

Since this circuit has a bandwidth lower than the 130 nm version, the resulting Q factor is higher, which means that the CMOS 65 nm narrowband balun-LNA is more selective and can attenuate blockers that are located closer to f_{LO}. Obviously, this property depends entirely of the filters component values and the LNA nodes impedances, and are unrelated with the used technology. In order to obtain the LNA response parameters, simulations identical to the presented in Sect. 6.1.1.2 were made. The results are shown in Table 6.6.

Table 6.7 Filtered LNAs comparison

Tech. (nm)	V. gain[a] (dB)	Atten.[b] (dB)	NF[a] (dB)	S_{11}[a] (dB)	OOB IIP2 (dBm)	OOB IIP3 (dBm)
130	> 23.8	> 14	< 3.3	< -17	$+9.4$	-0.7
65	> 24.8	> 12	< 6.3	< -17	$+11.9$	$+6.9$

[a] At f_{LO}
[b] Out-of-band attenuation

Comparing the values with the values obtained for the LNA only (Table 4.3) it is possible to verify that the voltage gain suffers a drop of about 4 dB in the worst case, the circuit's NF increases approximately 2 dB and OOB IIP2 and OOB IIP3 parameters are better. As with the 130 nm circuit, the filters can be dimensioned according to the system requirements.

6.1.3 LNAs Comparison

Table 6.7 shows a comparison of the LNAs with both filters integrated, for CMOS 130 nm and CMOS 65 nm technologies.

The operating frequency (0.3–1 GHz), $V_{DD} = 1.2$ V and power consumption are the same for both circuits. Analyzing Table 6.7 it is possible to conclude that both LNAs are identical. The 65 nm LNA has better voltage gain and a larger working band (this property was not studied in this work since both circuits were designed to operate at the same frequencies), as explained in Sect. 4.3. However, the NF of the 65 nm circuit is practically the double of the 130 nm, due to the reasons explained in Sect. 4.4. Thus, and although both circuits can achieve the desired function, the 130 nm circuit proved to be the best solution to employ in an integrated RF receiver, only because of the obtained NF. In this circuit it is possible to attenuate out-of-band interferers by at least 14 dB (comparing with the signals at f_{LO}), avoiding the use of external filters, with a minimum penalty in NF (about 1.5 dB in the worst case) and in voltage gain (about 3 dB in the worst case), comparing with the LNA of Chap. 4. The OOB IIP2 and OOB IIP3 simulations demonstrate that the interferers suffer a considerable attenuation, avoiding distortion and intermodulation problems that have a huge impact on modern RF receivers, specially in the LNA stage.

It was verified that there is a trade-off between the filters' performance and the NF of the overall circuit. Therefore, the filters' dimensions should be chosen according to the circuit specifications.

6.2 Passive Mixer and Transimpedance Amplifier

The mixer that was employed in this receiver has the same properties of the filter studied in Chap. 5, and is represented in Fig. 6.9. Since the mixer operates in current mode, its noise contributions are reduced and it is very linear, as referred in Sect. 3.2.2. Also, the use of the TIA at the mixer's output guarantees that the variation of V_{DS} of the switches is reduced, which improves the circuit's linearity.

Since the best LNA performance was achieved with the 130 nm circuit, the mixer was developed in that technology and the transistors have a channel length of 120 nm, due to the reasons explained before.

The mixer's outputs are connected to an ideal TIA with null input impedance, a gain $A_{vi} = 10\ \text{k}\Omega$ and a bandwidth of approximately 8 MHz. The mixer has quadrature outputs in order to handle modern modulation schemes, has four phases and needs to be driven by the same signal that clocks the two high-Q BPFs that are integrated in the LNA. Regarding the input, the simulations that were made in this section consider that the mixer is driven by a load equal to the studied LNA output impedance, $R_L \approx 700\ \Omega$. Since the circuit is differential, the total equivalent resistance is approximately 1.4 kΩ. The mixer input impedance is shown in Fig. 6.10.

Due to the mixer's configuration, its input presents a lower impedance for frequencies near f_{LO} and a higher impedance for frequencies far from f_{LO}. This means that the mixer behaves like a notch filter, i.e. it allows desired signals

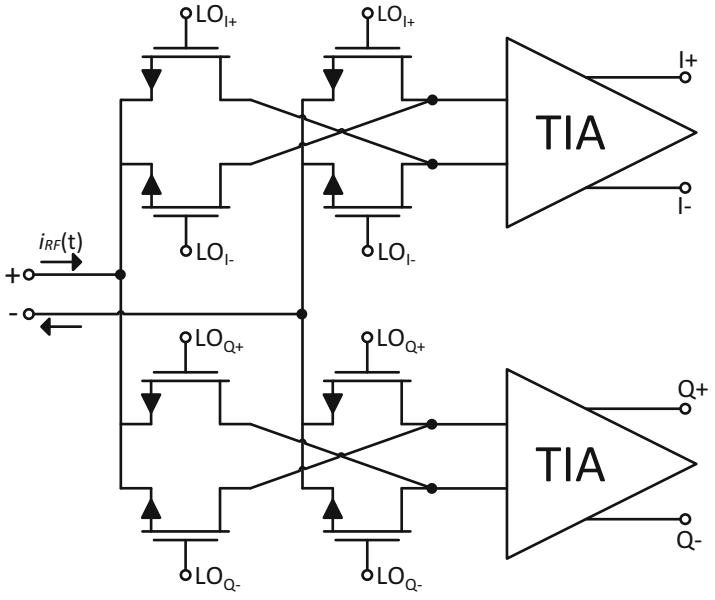

Fig. 6.9 Mixer and TIA

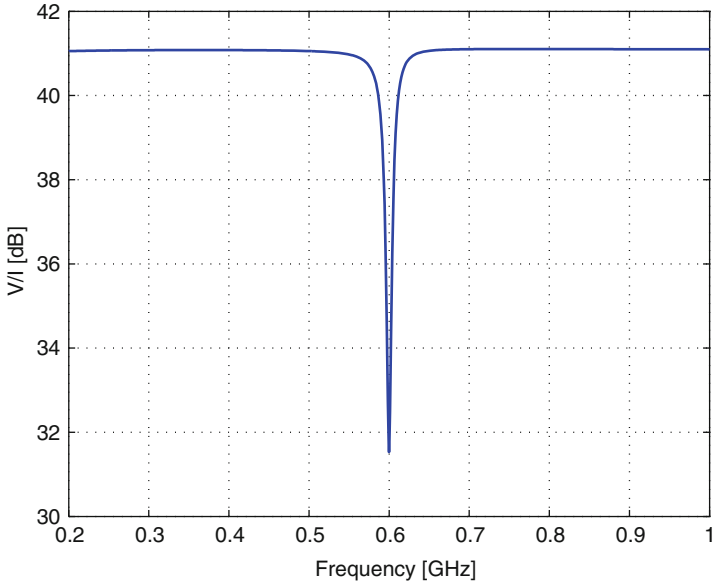

Fig. 6.10 Mixer input impedance with $f_{LO} = 600\,\text{MHz}$

(near f_{LO}) to flow to the circuit and be shifted to the IF, and attenuates the signals located at out-of-band frequencies (far from f_{LO}) due to the large input impedance. The mixer was projected to exhibit a bandwidth identical to the LNA studied in Sect. 6.1.1 and taking into account the TIA's bandwidth that was referred previously. To achieve the desired bandwidth of approximately 6 MHz, the switches dimensions were chosen to be $W = 34.4\ \mu\,\text{m}$, which leads to $R_{SW} \approx 61\,\Omega$. Also, the switches size was chosen taking into account the tradeoff between linearity and noise. Increasing the switches size reduces their ON resistance, and the circuit is more linear because it generates less voltage variation. On the other hand, larger switches have more noise contributions, as explained below, which results in a larger mixer NF.

By applying a differential current signal with $I_{in} = 10\ \mu\text{A}$ and $f_{RF} = 601\,\text{MHz}$ at the mixer's input, fed by a LO with $f_{LO} = 600\,\text{MHz}$, the signal at the TIA output can be seen in Fig. 6.11.

As expected, the I and Q signals are identical, with a difference of 90° in phase. The output signal has a value of $V_{out} = 45.4\,\text{mV}$, with a frequency $f_{RF} - f_{LO} = 1\,\text{MHz}$. This IF value was chosen taking into account that a low IF is desired in order to relax the ADC requirements. The mixer's conversion gain (CG_{mixer}) is given by

$$CG_{mixer} = 20\log\left(\frac{V_{out}}{I_{in}\cdot A_{vi}}\right) = 20\log\left(\frac{45.4m}{10\mu \times 10k}\right) = -6.86\,\text{dB} \tag{6.1}$$

Regarding the NF, it is lower than 6 dB for frequencies above 100 kHz and for all the interesting IF values (hundreds of kilohertz to few megahertz), as shown in

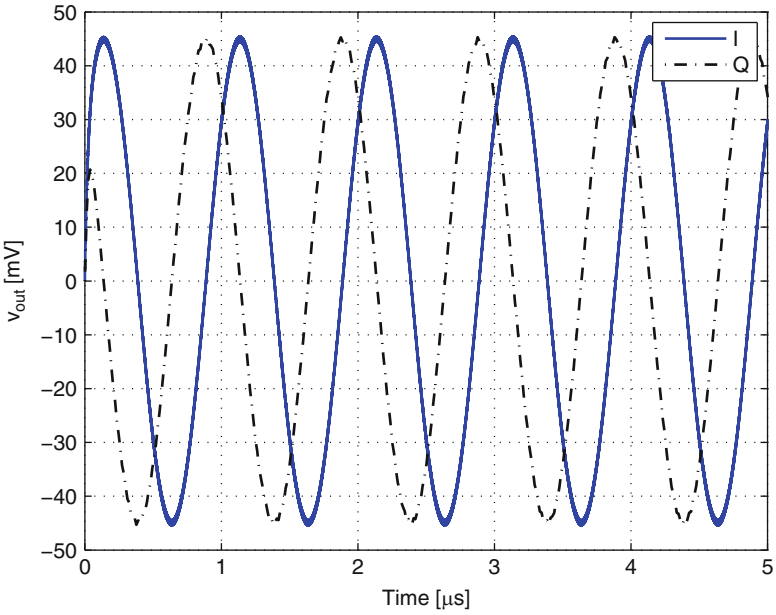

Fig. 6.11 TIA output signal

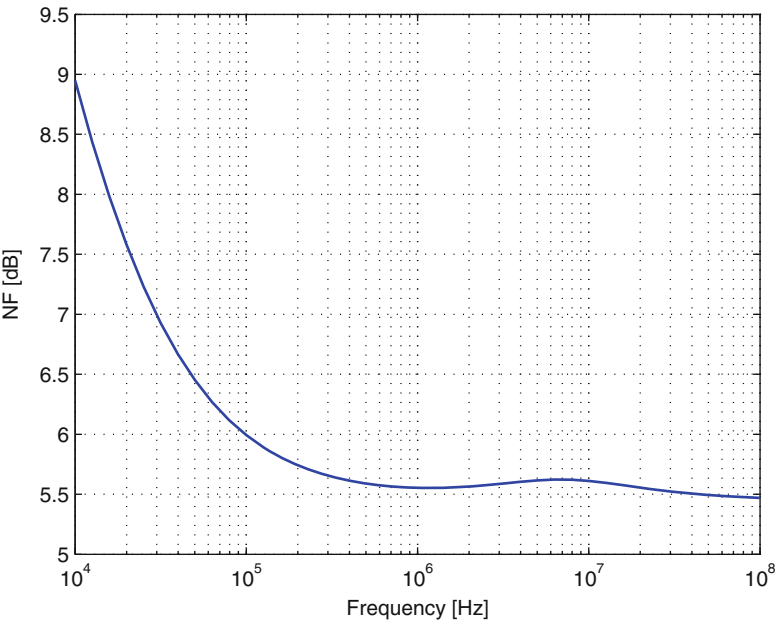

Fig. 6.12 Mixer NF with $f_{LO} = 1$ GHz

Table 6.8 Mixer parameters

CG_{mixer} (dB)	NF (dB)	OOB IIP3 (dBm)	Tech. (nm)
−6.86	< 6	+19.8	130

Fig. 6.12. For this simulation $f_{LO} = 1$ GHz was considered, which is the maximum operating frequency of the receiver and, as with the LNA (Fig. 6.6), is the working frequency where the circuit has more noise contributions, i.e. for the other f_{LO} values between 0.3 and 1 GHz, the mixer's NF is lower than the presented in this simulation. These noise contributions are mainly due to the thermal noise of the mixer's switches. Since the mixer is passive, the flicker noise is negligible (decoupling capacitors were placed between the LNA and the mixer to guarantee that there is no DC current flowing in this path). In order to reduce the NF, the transistors' size can be reduced to increase R_{SW} and consequently decrease the transistors' current thermal noise, as expressed in (2.20). However, reducing R_{SW} increases the circuit bandwidth (and reduces the Q factor) and decreases the mixer's interferers attenuation as stated in (5.8), since R_{SW} becomes closer to the LNA output impedance. It also reduces the CG_{mixer}, because the mixer's input impedance grows and consequently the RF signal flows less to the mixer's path, being more attenuated. Like the LNA, the mixer should be designed according to the system requirements.

For the IIP3 simulation, a value of +19.8 dBm was obtained, which means that the mixer can handle large interferers without corrupting the desired signal and it is very linear, as expected in a current-driven passive mixer. For this simulation two pure sine waves were placed at the mixer's input, $f_1 = 700$ MHz and $f_2 = 799$ MHz, with a LO frequency of $f_{LO} = 600$ MHz.

A summary of the mixer's parameters is presented in Table 6.8.

6.3 Complete Receiver with Transimpedance Amplifier

To check whether the developed receiver has the desired performance, the blocks that were considered in the previous sections were combined, as shown in Fig. 6.13. It is important to note that simulations were made only for the circuit designed with CMOS 130 nm technology, since the best results were achieved using this technology.

By applying a pure sinusoid with $f_{RF} = 601$ MHz and $V_{rf} = 1$ mV at the receiver's input, with $f_{LO} = 600$ MHz, the simulation result for the receiver's output signal is shown in Fig. 6.14. As expected, this signal is also a pure sine wave translated to 1 MHz with an amplitude of $v_{out} \approx 142$ mV, which means that the mixer's output current is approximately 14.2 μA.

As with the mixer (Sect. 6.2), the receiver highest NF is obtained when $f_{LO} = 1$ GHz. The simulation results obtained can be seen in Fig. 6.15.

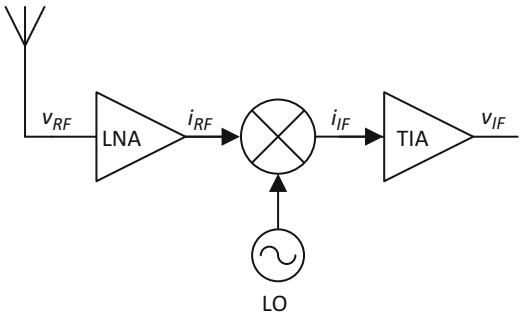

Fig. 6.13 RF receiver with TIA

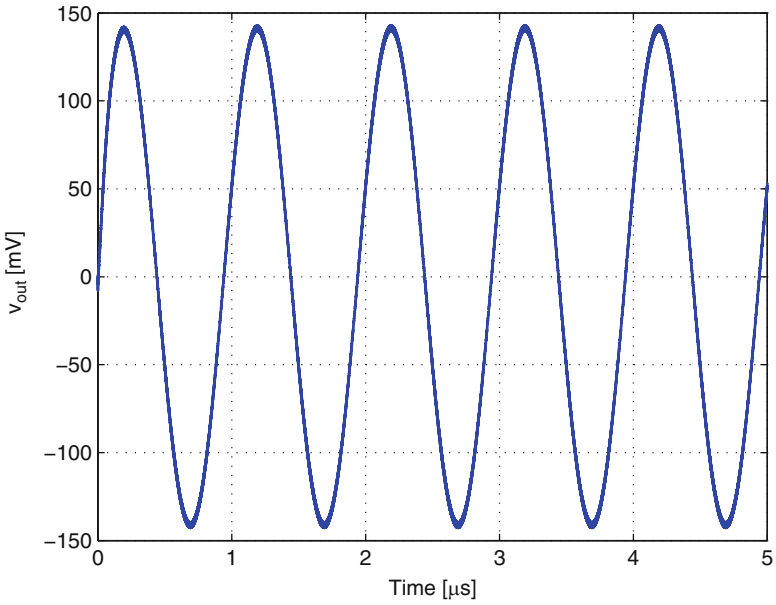

Fig. 6.14 Receiver output signal with a pure sine wave at the input

For the desired IF values (hundred of kHz to few MHz) a NF below 10 dB was obtained and for the chosen IF (1 MHz) the receiver's NF is approximately 6.9 dB. The large growth of the NF at high frequencies is mostly related with the LNA's noise contribution that, as shown in Fig. 6.4, is very large for frequencies far from f_{LO}. For lower frequencies the LNA noise contribution is reduced due to the LPF effect of the integrated filters.

To understand the interferers' effect on the receiver's performance, a simulation was carried out to observe the receiver's voltage gain and NF variations with the interferers power. Figures 6.16 and 6.17 show that for a 0 dBm blocker the voltage gain drops 7 dB and the NF degrades by 5.4 dB. This means that, due to the included filtering, the receiver can tolerate large interferers located at frequencies far from f_{LO}. Also, in order to evaluate the effect of an interferer on the receiver's

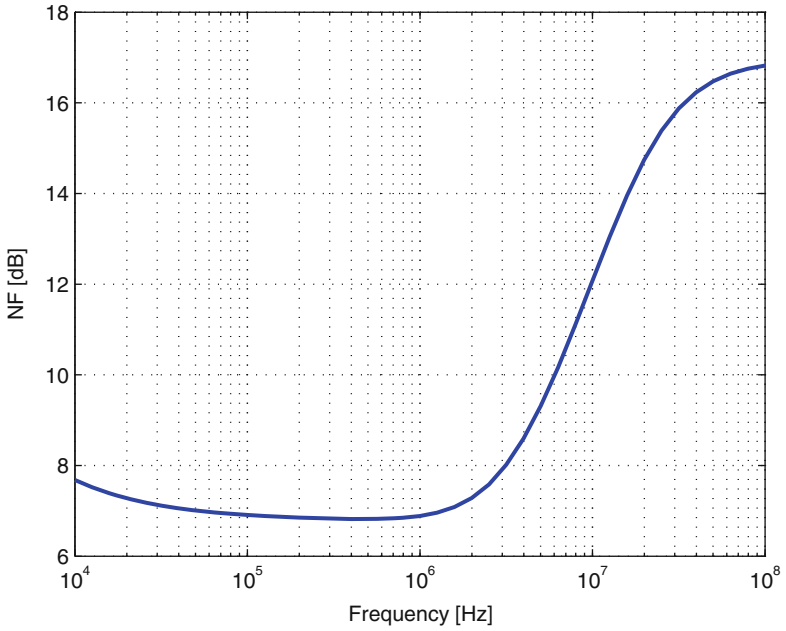

Fig. 6.15 Receiver NF with $f_{LO} = 1\,\text{GHz}$

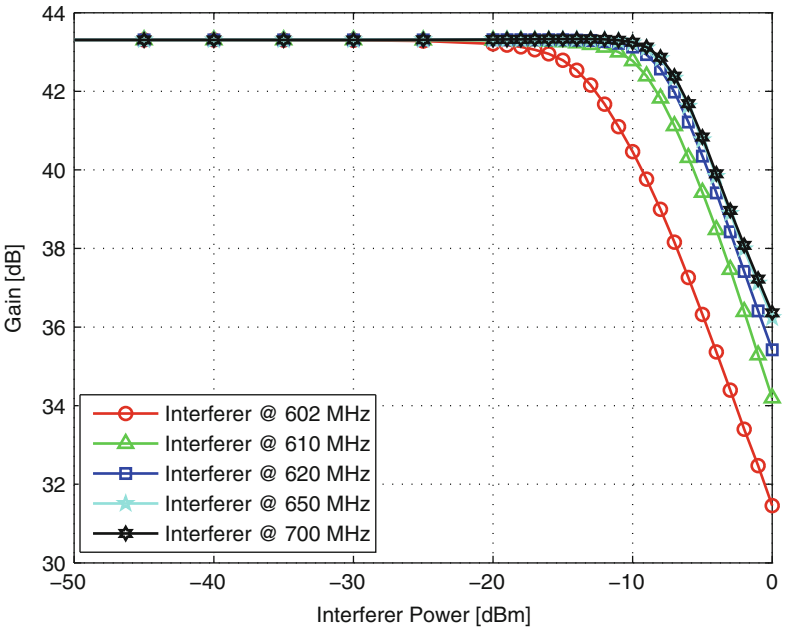

Fig. 6.16 Receiver voltage gain with $f_{LO} = 600\,\text{MHz}$, IF $= 1\,\text{MHz}$

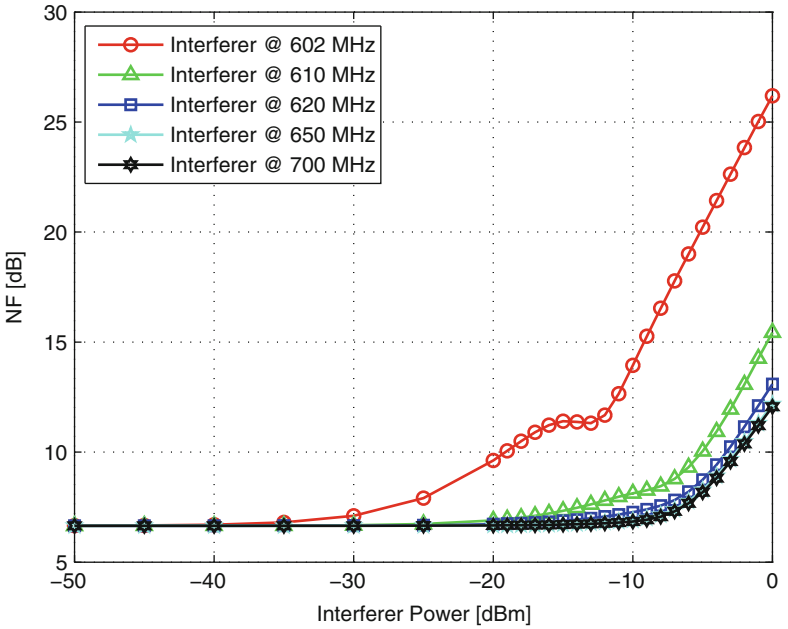

Fig. 6.17 Receiver noise figure with $f_{LO} = 600\,\text{MHz}$, IF $= 1\,\text{MHz}$

compression when a weak desired signal is injected at its input, a blocker test was performed. This simulation was carried out with the desired RF signal, with a power of $-50\,\text{dBm}$, located at 601 MHz (IF of 1 MHz since $f_{LO} = 600\,\text{MHz}$) and an interferer located at 700 MHz (OOB frequency). The obtained blocker P1dB (B1dB) is $-5\,\text{dBm}$.

Regarding the receiver's linearity, an OOB IIP3 $= 10.9\,\text{dBm}$ was obtained. This simulation was performed for $f_{LO} = 600\,\text{MHz}$ using a two-tone test with $f_1 = 700\,\text{MHz}$ and $f_2 = 799\,\text{MHz}$ (the intermodulation product is located at 601 MHz RF and 1 MHz IF).

6.4 Current-Buffer

In order to avoid the use of a TIA, to convert the IF current signal to a voltage signal before the digital part of the receiver, a current-driven $\Sigma\Delta$ modulator was used in this work, which allows to directly convert the signal at the mixer's output to the digital domain. The Current-Buffer (CB) studied in this section is intended to perform the interface between the receiver's AFE and the $\Sigma\Delta$M, as shown in Fig. 6.18. This circuit is essential to guarantee the receiver proper functioning, since both blocks (mixer and $\Sigma\Delta$M) have different impedances, which causes the second

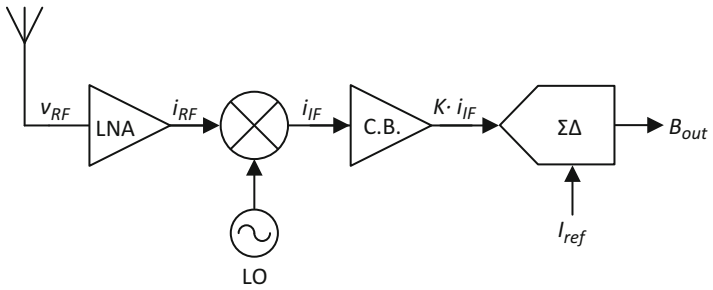

Fig. 6.18 RF receiver schematic with CB and ΣΔM

circuit to load the first one an consequently interfere with its operation. Also, this CB can provide current gain (or attenuation) to allow the tuning of both circuits and ensure that the ΣΔM operates at full-scale when the RF signal at the AFE's input is maximum.

6.4.1 Theoretical Analysis

The studied CB [39, 40], presented in Fig. 6.19, consists of a flipped voltage follower current sensor (FVFCS) that operates as a current mirror.

The transistor M_3 is in a feedback loop, with unitary gain, and does not conduct any AC current. This allows the circuit to have a very low input impedance, given by Carvajal et al. [40]

$$R_{in} \approx \frac{\frac{1}{g_{m3}}\left(1+\frac{r_{ds5}}{r_{ds3}}\right) \parallel r_{ds1}}{g_{m1}\left(r_{ds5} \parallel g_{m3} \cdot r_{ds3} \cdot r_{ds1}\right)}, \tag{6.2}$$

where g_{mi} and r_{dsi} are the transconductance and output resistance of transistor M_i, respectively. For the specific case where $r_{ds3} \approx r_{ds5}$,

$$R_{in} \approx \frac{2}{g_{m1} \cdot g_{m3} \cdot r_{ds3}}. \tag{6.3}$$

The output impedance of this configuration is given by

$$R_{out} \approx r_{ds2} \parallel r_{ds6}, \tag{6.4}$$

which is a relatively high impedance. Since an ideal current buffer has null input impedance and infinite output impedance (as an ideal current source), this circuit behaves almost like an ideal current buffer and it is expected to have a minimum interference in the AFE and ΣΔM circuits.

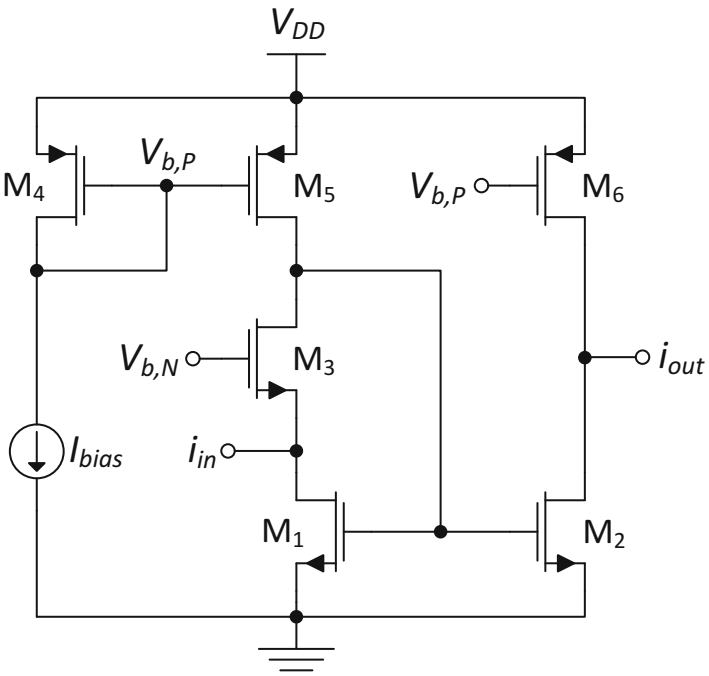

Fig. 6.19 Current-buffer schematic

By changing the bias current (I_{bias}) it is possible to modify the input and output impedances, since $g_m \cong 2I_D/V_{Dsat}$ and $r_{ds} \propto L/I_D$ [11], with $I_D = I_{bias}$ for the input stage and $I_D = I_{bias}/k$ for the output stage, where k is the CB multiplication factor. If I_{bias} increases, the input and output impedances decrease and the circuit's power consumption increases.

As explained before, this circuit has unitary gain, due to the feedback of the transistor M_3. However, the current range of the AFE circuit is usually different from the $\Sigma\Delta$M and there is the need to scale the gain of the CB. This can be achieved by changing the relation of the transistors $M_1 - M_2$ and $M_5 - M_6$. For example, if it is desired that $i_{out} = k \cdot i_{in}$, $W_{M2} = k \cdot W_{M1}$ and $W_{M6} = k \cdot W_{M5}$, where W_{Mi} is the channel width of transistor M_i . Thus, it is possible to scale the current that passes through the output stage devices by a factor of k, relatively to the current of the input stage.

Regarding the supply voltage, this circuit can operate with very low values, since the maximum V_{DD} necessary to guarantee that all transistors operate in the active region is given by the sum of the DC voltages of the input stage,

$$V_{DD,min} = V_{GS,M1} + V_{Dsat,M5} = 2V_{Dsat} + V_{Tn}. \tag{6.5}$$

A margin should be added to V_{DD} in order to guarantee that all transistors are operating in the active region ($V_{DS} > V_{Dsat}$).

Table 6.9 Current-buffer parameters

Device	W (μm)	L (μm)	I_D (μA)	V_{Dsat} (mV)	g_m (μS)
M_1	5	0.15	21.3	54	374
M_2	1.1	0.15	6.5	58	108.3
M_3	4	0.15	20	61	321.3
M_4	17	0.15	15	59	315.2
M_5	17	0.15	19.9	60	411.4
M_6	5.3	0.15	6.6	61	133.9

6.4.2 Simulation Results

Since the mixer and ΣΔM circuits are differential, two identical CBs (Fig. 6.19) were used for the interface between these two circuits. However, this analysis only considers one CB, for simplicity. This circuit was developed in CMOS 65 nm because the used ΣΔM was designed in this technology and all receiver's blocks need to use the same technology, in order to be possible to have a fully integrated RF receiver. To avoid short channel effects, and considering that this circuit operates at relatively low frequencies, all the transistors have a length of 150 nm. The dimensions and key parameters of all transistors are presented in Table 6.9.

Since the bias current is small ($I_{bias} = 15\,\mu A$), the transistors need to have a low V_{Dsat} due to channel width limitations (specially the transistor M_2 that carries lower current). A possible solution to this restriction is to increase I_{bias}, but this leads to a decrease of the output impedance and more power consumption, as previously referred.

Comparing the devices M_1 and M_2 it is possible to conclude that $k \approx 0.3$, which means that the current at the AFE output is attenuated in order to the ΣΔM reach the full-scale and does not saturate, as will be demonstrated in the next section. In order to verify if the CB operation is within the expected, a pure sinusoid with $i_{in} = 30\,\mu A$ and $f = 400\,kHz$ was injected in the circuit's input. The simulation results are shown in Fig. 6.20. By comparing the input and output signals it is possible to conclude that both signals have the same frequency and $i_{out} \approx 0.3 \cdot i_{in}$, as desired. The phase shift of the output signal is due to the CS transistor.

6.5 Complete Receiver with Sigma-Delta Modulator

The employed ΣΔ modulator consists of a current-mode passive second-order continues-time ΣΔM, which converts an analog current signal directly to the digital domain, avoiding the use of a TIA that introduces noise and increases the chip area and cost. In order to understand the circuit's behavior when it is fed by an ideal current source, an ideal sine wave was placed at its inputs, with $I_{in} = 7.5\,\mu A$ and $f_{in} = 420\,kHz$, with the ΣΔM reference current equals to $I_{ref} = 10\,\mu A$ and a supply

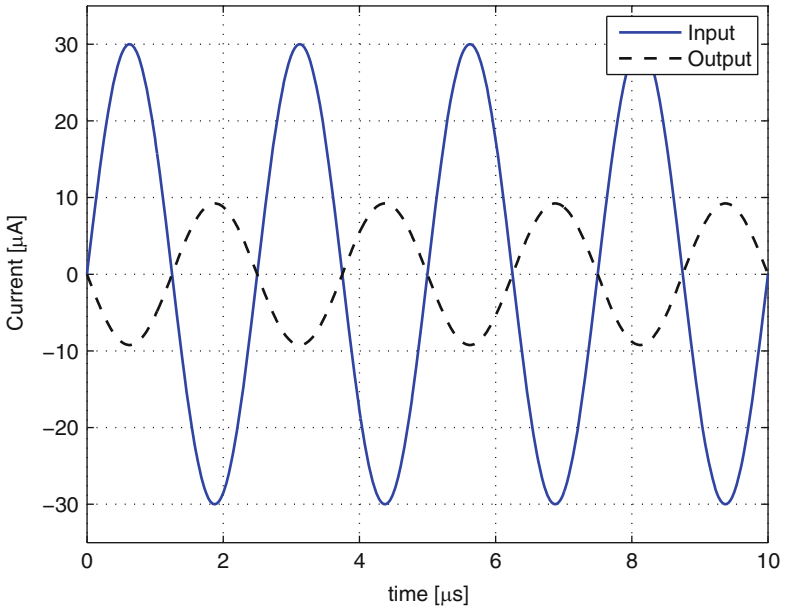

Fig. 6.20 Current-buffer time response

voltage of $V_{DD} = 1$ V. The obtained Fast Fourier Transform (FFT) is presented in Fig. 6.21. Operating at full-scale, the ΣΔM has a resolution of 9.2 bits and a Signal-to-noise and Distortion Ratio (SNDR) = 57.3 dB. These results will serve as base of comparison to the complete receiver.

As referred before, the receiver studied in this section (Fig. 6.18) is identical to the receiver studied in Sect. 6.3, without the ideal TIA block, but developed using CMOS 65 nm technology instead of CMOS 130 nm. Since both circuits have the same characteristics, the receiver of this section was not studied (except the LNA block in Sect. 6.1.2) and its only purpose is to verify if it is possible to integrate a ΣΔM at the mixer's output. For the complete receiver, shown in Fig. 6.18, which uses the studied LNA and mixer, and with a CB supply voltage of 1 V, the ΣΔM FFT shown in Fig. 6.22 was obtained. For this simulation a pure sine wave with $f_{RF} = 600.42$ MHz was placed at the receiver's input. The LO has a frequency of $f_{LO} = 600$ MHz, which leads to an IF of 420 kHz.

Comparing with Fig. 6.21, the ENOB decreases to 6.2 bits, and the SNDR decreases to 39.3 dB. This penalty in performance is expected because the AFE introduces a significant amount of noise to the desired signal and the CB has non zero input impedance and infinite output impedance, like an ideal current buffer, and consequently has influence on the circuit's behavior, comparing with an ideal current source. For this supply voltage, the CB DC power consumption (for the single-ended version) is about 42 μW.

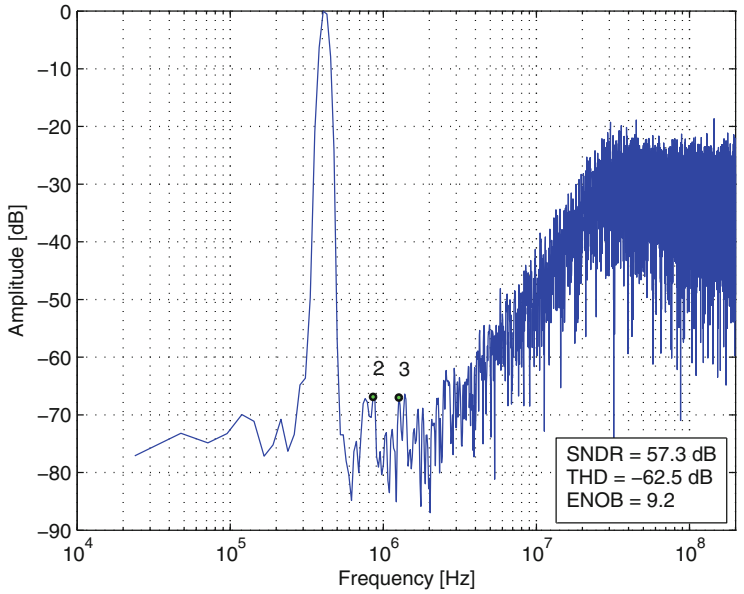

Fig. 6.21 Output spectrum of the ΣΔ modulator fed by an ideal current source (2^{14} FFT using a Blackman window)

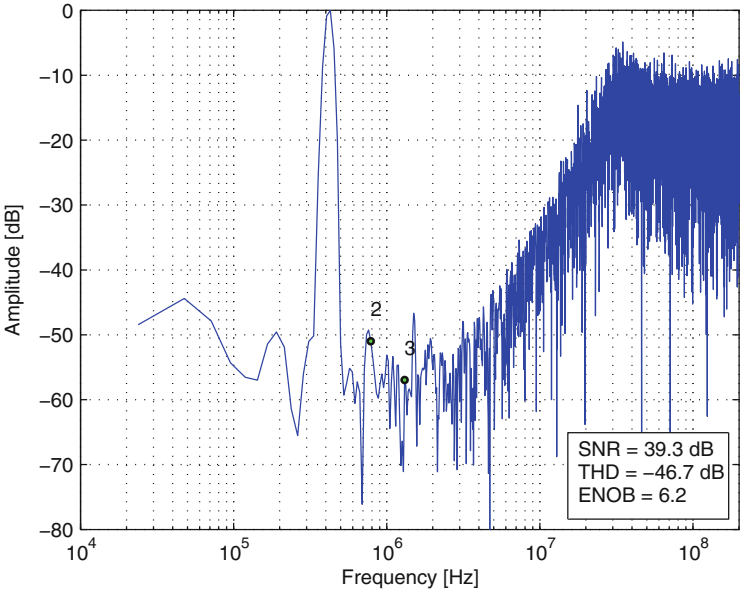

Fig. 6.22 Output spectrum of ΣΔM driven by the developed receiver AFE (2^{14} FFT using a Blackman window)

Table 6.10 ΣΔM performance parameters for sub-1V supply voltages

V_{DD} (mV)	SNDR (dB)	THD (dB)	ENOB
900	38.0	−43.8	6.0
800	38.1	−45.2	6.0
700	37.4	−42.9	5.9
600	36.4	−42.2	5.8
500	36.0	−42.1	5.7

As referred in Sect. 6.4.1, the CB can theoretically operate with very low supply voltages, of the order of milivolts. To test the minimum V_{DD} for which the CB can operate properly, the supply voltage was decreased by a 100 mV step from 1 V to 400 mV, while keeping the same transistors size. The obtained results are presented in the Table 6.10. For 400 mV it was impossible to guarantee that all the transistors operate in the active region and the resulting simulation was very poor. From 900 to 500 mV the obtained results are practically the same, with a penalty of 0.3 bits in the ENOB and 2 dB in SNDR. This means that the circuit performance does not depend of the supply voltage and it is only necessary to guarantee that all the transistors operate in the desired region.

With $V_{DD} = 500$ mV, the CB DC power consumption (for the single-ended version) is about 21 μW, which is half the value of the simulation with $V_{DD} = 1$ V.

These simulations prove that is possible to directly connect the ΣΔM at the AFE output, with a minimum penalty in the ΣΔM, avoiding the use of a TIA to convert the IF signal at the mixer's output to the voltage domain.

Chapter 7
Conclusions

This book presents a tutorial review of architectures and circuit blocks suitable for modern RF receivers implemented as CMOS integrated circuits. It is described an RF receiver, with passive high-Q bandpass filters integrated in a CMOS wideband LNA with noise and distortion cancellation, and with a current-mode $\Sigma\Delta$ ADC that converts directly the IF signal at the current-driven mixer's output to the digital domain, thus, avoiding the use of unnecessary blocks at the analog front-end. The techniques reviewed allow the design of a fully integrated receiver. This low cost solution is required, for instance, in biomedical applications.

With the increase of wireless communications, the frequency spectrum leads to more interferences. To overcome this problem it is necessary to employ filters that reject the unwanted signals at the receiver's input. However, traditional filters (e.g. SAW filters) are difficult to integrate in the receiver due to their complexity and area, which makes it impossible to employ an IC with the complete receiver, and have problems related with impedance matching and cost.

A wideband radio-frequency (RF) receiver, with integrated filtering that can be precisely controlled by the local oscillator (LO) frequency to attenuate out-of-band interferers, is analyzed in depth in this book. This receiver operates in current-mode, has small area, low power, and low cost and can be fully integrated in one chip. The key blocks of the receiver analog front-end are described. The low-noise amplifier (LNA) is a widely tunable narrowband balun-LNA, which performs conversion from single-ended to differential, and has two integrated high-Q bandpass filters (BPFs) that filter out undesired interferers at the receiver's input. This circuit is very compact and avoids the use of inductors and of an external balun, which occupies a large area. To convert the IF current signal to the digital domain, avoiding the use of a transimpedance amplifier (TIA) that occupies large area and increases the receiver noise figure (NF), a current-mode $\Sigma\Delta$ analog-to-digital converter (ADC) is directly connected to the mixer's output, reducing the cost of modern receivers built in standard CMOS nanotechnologies.

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The integration of the studied high-Q BPFs in the wideband balun-LNA allows to obtain a widely tunable narrowband balun-LNA that can attenuate out-of-band interferers of about 14 dB (for the 130 nm circuit), with respect to signals located at f_{LO}, with a minimum penalty in the circuit voltage gain and NF (3 and 1.5 dB respectively), comparing with the LNA only. Regarding distortion and nonlinearities, OOB IIP2 $= +9.4$ and OOB IIP3 $= -0.7$ dBm were obtained, which are significantly better values comparing with the LNA only and prove that the integration of the filters in the LNA increases the circuit's linearity and allows to attenuate interferers located near the frequency of interest. Since the filters are passive, the LNA power consumption remains practically the same. By employing this technique is possible to avoid the use of external filters at the LNA input/output, which require a multichip circuit that has area and cost penalty. Thus, it is possible to reduce the overall circuit area and costs, and allow the full integration of the receiver in the same chip. It was verified that a trade-off exist between the filters' performance and the NF of the LNA block, i.e. an increase of the filters' out-of- band attenuation leads to a reduction of the voltage gain at the desired frequencies and to the increase of the circuit's NF. Therefore, the filters should be designed according to the system specifications. A comparison between the used technologies (CMOS 130 nm and CMOS 65 nm) shows that both circuits have the intended operation.

Regarding the studied BPF, simulation results demonstrate that this filter is programmable and can be precisely tuned by the LO, with a penalty of about -1.82 dB in the overall circuit gain, for a filter with four phases. This filter presents a high Q factor and, since it is passive, it has almost no DC power consumption and flicker noise, leading to low noise contributions. By employing a differential version of the filter is possible to filter signals located at the LO even order harmonics and obtain the double of the filter input impedance, comparing with the single-ended filter.

Regarding the 130 nm mixer, it was obtained a conversion gain of about -6.9 dB, NF < 6 dB and OOB IIP3 $= +19.8$ dBm, which means that the mixer is very linear and can handle large out-of-band interferers without corrupting the desired signal.

Simulation results of the complete receiver AFE, using CMOS 130 nm technology, show an NF $= 6.9$ at 1 MHz IF, B1dB $= -5$ dBm and OOB IIP3 $= 10.9$ dBm, which means that the receiver can tolerate large interferers located at frequencies far from f_{LO}.

To allow the direct conversion of the current signal at the mixer's output to the digital domain, a current-mode $\Sigma\Delta$M was employed in the receiver. To perform the interface between the mixer and the $\Sigma\Delta$M, a CB with high dynamic range was developed, which prevents that the $\Sigma\Delta$M loads the mixer, due to the different impedances of both blocks, and affects its functioning. This CB also allows to scale the current at the mixer's output to allow the $\Sigma\Delta$M to operate at full-scale when the signal at the receiver's input is maximum.

The complete RF receiver, developed in 65 nm, causes a drop of 3 bits in the $\Sigma\Delta$M resolution, comparing with the $\Sigma\Delta$M driven by an ideal sine wave, being possible to achieve a resolution of 6.2 with CB and $\Sigma\Delta$M supply voltages of 1 V. Regarding the SNDR, it was obtained a value of 39.3 dB. This penalty is due to the

noise introduced by the AFE and the CB and the fact that the CB has not null input impedance and infinite output impedance, as ideally desired. This means that the receiver AFE can be directly connected to a current-mode $\Sigma\Delta$M without the use of additional blocks, like a TIA, that introduce more noise to the circuit and increase the chip area and cost.

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