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High-Ratio Voltage Conversion in CMOS for Efficient Mains-Connected Standby

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Preface

The focus of this work can be seen as making the bridge between the fields of Solid-State Integrated Circuits (IC) and Power Electronics. Multiple AC-DC and DC–DC power converters are investigated from the IC standpoint, this means a constant effort to realize converters that are fully integrated on a single chip, or have at least a very high level of integration. Moreover, it is of paramount importance to improve power conversion efficiency throughout the transport chain of energy from source (e.g., a battery, the mains) to load (i.e., the application which is the consumer). Creating new converter systems that are very efficient and integrated into chip-scale solutions enables the benefit of longer battery autonomy in portable devices, on top of enabling ever lighter and slimmer devices. In non-mobile applications, less power is required from the mains for the same functionality, and consequently, this helps to reduce emissions related to electricity generation, such as carbon dioxide, etc. To summarize this work, a few different research targets are introduced: (1) monolithic switched-capacitor DC–DC conversion for granular power delivery on-chip, (2) reduction of standby power in mains-connected devices through the addition of an efficient and compact auxiliary supply to provide power during standby mode, and (3) high-ratio DC–DC voltage conversion in a monolithic context.

Modern integrated circuits contain more and more functionality within a single chip. These are also called Systems on Chip, and examples of such systems are the Application Processing Unit chips at the heart of today's smartphones or personal computers. Because these single-chip systems house a large amount of subsystems, it is only logical that they require multiple different supply voltages to power these functions. In the past, most required voltages were generated off-chip on the printed circuit board, in the vicinity of the chip. This approach, however, is becoming less and less viable due the growing number of desired supply voltages and the associated number of interconnection pins to get the power from the off-chip power converters to the on-chip loads. Moreover, there are other negative aspects related to this approach. Therefore, a better approach is to provide the chip with one, or a few, different supply voltages, and use on-chip power converters to further provide the desired supply voltages. This requires less package pins and enables better regulation of the desired supply voltage, since the feedback loop

can now be performed locally on the chip. The goal of this work is to enable the above. To that end, an investigation of suitable fully integrated DC–DC converters is conducted. Specifically, the realization of a switched-capacitor DC–DC converter in a standard CMOS technology with a high power density was targeted. It is important to implement the converter in a standard CMOS process to enable co-integration with its loading circuits on the same chip. Secondly, a high power conversion density yields a lower chip area requirement to implement the converter. This work investigated circuit techniques to deliver top-notch specifications, given this context.

Standby power is caused by mains-connected devices in standby mode. They have a power supply that is optimized for the active mode, where power levels may be very large with respect to the low required power level of standby, a factor 100× or more. It cannot be expected that these converters are efficient both at their nominal power (active mode) and also at light-load (standby mode) condition. Therefore, the power consumption of mains-connected devices is much higher than what it could be. Since standby power on a global scale is associated to about 10 % of residential electricity consumption and 1 % of CO_2 emissions, standby power reduction could help to counter global warming. Therefore, this work aims to build the AC–DC converters that enable such reductions in standby power and prevent the associated emissions.

The research toward high-ratio voltage conversion in an integrated context is motivated by the research conclusion, of the previous work on AC–DC converters, that switched-capacitor DC–DC converters are particularly well suited for this task. Monolithic high-ratio DC–DC conversion can, for example, be used to deliver high voltages from a standard Li-ion battery in a very small and light form factor, which is particularly important for robotic insects, where high voltages are required in the drivers that power the wings. Switched-capacitor DC–DC converters do not rely on the duty cycle to set their voltage conversion ratio, as its popular inductive buck converter counterpart does, and can therefore maintain a 50 % duty cycle, regardless of the actual voltage conversion ratio. Instead, the conversion ratio is a consequence of the switched-capacitor topology. As such, it is a better candidate for high-ratio voltage conversion than the buck converter, which in this case is more affected by efficiency limiting drawbacks, due to its reliance on very low duty cycles in order to obtain high voltage conversion ratios. The research in this work explores, given the system-level choice for the SC DC–DC converter, which topology is expected to yield the best performance, considering the typical context of CMOS integration.

Contents

List of Abbreviations

AC	Alternating Current
ARG	Auxiliary Rail Generator
AVS	Adaptive Voltage Scaling
CMOS	Complementary Metal-Oxide Semiconductor
CO_2	Carbon dioxide
COTS	Commercial Off-The-Shelf
CVD	Chemical Vapor Deposition
DC	Direct Current
DFS	Dynamic Frequency Scaling
DVS	Dynamic Voltage Scaling
EEF	Efficiency Enhancement Factor
EMC	ElectroMagnetic Compatibility
ESR	Equivalent Series Resistance
FSL	Fast Switching Limit
GHG	Greenhouse gas
GO	Gate Oxide
IC	Integrated Circuit
ICR	Intrinsic Charge Recycling
IO	Input Output
IoE	Internet of Everything
IoT	Internet of Things

LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
LDO	Low-DropOut
MIM	Metal-Insulator-Metal
MIMO	Multiple-Input Multiple-Output
MOM	Metal-Oxide-Metal
NMOS	N-type MOS
PCB	Printed Circuit Board
PDN	Power Delivery Network
PFC	Power Factor Correction
PFM	Pulse-Frequency Modulation
PMIC	Power Management Integrated Circuit
PMOS	P-type MOS
PMU	Power Management Unit
PSiP	Power System-in-Package
PSoC	Power System-on-Chip
ReSC	Resonant Switched-Capacitor
SO_2	Sulfur dioxide
SoC	System on Chip
SOI	Silicon On Insulator
SOS	Silicon On Sapphire
SSL	Slow Switching Limit
VCO	Voltage-Controlled Oscillator
VCR	Voltage Conversion Ratio
VHF	Very High Frequency
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

List of Symbols

α	Ratio of C_{par} to C_{fly}
η_x	Efficiency of x
γ	Ratio of V_o to $V_{o,id}$
ΔV_{C_x}	Voltage variation on capacitor x
$a_{c,i}$	Charge flow of capacitor i to the output charge
$a_{r,i}$	Charge flow of switch i to the output charge
C_{DC}	Decoupling capacitor
C_{fly}	Flying capacitor
C_{in}	Input decoupling capacitor in DC–DC conversion context; high-voltage input-series capacitor in AC–DC conversion context
C_{out}	Output capacitor
C_{par}	Bottom-plate parasitic capacitor
f_{sw}	Switching frequency
K_c	Topology-specific flying capacitor utilization value
k_c	Topology-specific flying capacitor utilization vector
k_s	Topology-specific power switch utilization vector
M_{sw}	Swing metric of the bottom-plate capacitor loss
N	Number of converter fragments in a multi-phase time-interleaved converter
P_i ; P_{in}	Input power
P_o ; P_{out}	Output power
R_L	Load impedance
R_o ; R_{out}	Converter output impedance
R_{dyn}	Impedance to model the dynamic converter loss
R_{esr}	Equivalent series resistance
R_{fsl}	Fast switching limit converter output impedance
R_{route}	Routing impedance
R_{ssl}	Slow switching limit converter output impedance
T_{CLK}	Clock period
t_{dead}	Dead-time between non-overlapping clock phases

t_{off}	Rectifier off-time
V_{AC}	Mains amplitude
V_{C_x}	Voltage of capacitor x
V_{dd}	Nominal supply voltage
V_i ; V_{in}	Input voltage
V_{min}	Lowest allowed supply voltage value
$V_{O,eff}$	Flying capacitor voltage value at the end of a charge-transfer phase
$V_{o,id}$	Open-circuit converter output voltage
$V_{O,max}$	Theoretical maximum flying capacitor voltage value at the beginning of a charge-transfer phase
V_o ; V_{out}	Output voltage
V_{R_o}	Voltage drop over converter output impedance
V_{ref}	Reference voltage
V_{reg}	Regulated voltage
V_{supply}	Supply voltage
V_{th}	Transistor threshold voltage

Chapter 1
Introduction

The ambition of this work is, in a very broad sense, to improve the electrical energy transport between a source and its load. As this can be brought into practice in many different situation contexts, it is the electronic engineering's perspective, and more specifically the integrated circuits point of view, that is central here. The field that deals with energy conversion problems and challenges is called power management, and it is a collection of AC–AC, AC–DC, DC–AC, and DC–DC conversions that alter the voltage and/or frequency relation between input and output. The following work consists of developments in both AC–DC and DC–DC conversions. In case of the former, the application domain is providing an IC-compatible supply voltage output from a mains input. In case of the latter, on-chip converters are targeted to enable power supply granularization to address the increasingly challenging power delivery in Systems on Chip (SoC).

The introductory chapter to this work will further discuss the issues and consequences of present-day energy conversion, related to the scope of the further presented work. Afterwards, the possibilities toward improvement, in which research in the field of integrated power management can provide a beneficial impact, are introduced. Finally, an outline of the content is graphically represented to indicate the interdependence of the remaining chapters.

1.1 Standby Energy Consumption

1.1.1 Origin

Among the various ways energy is consumed, the specific issue of standby power now becomes the subject of our target focus. The core of the problem can aptly be demonstrated by the example of a microwave. Counter intuitively as it may seem,

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most microwave ovens consume more energy to display time than they use to heat food [76]. Even though the power level of microwaving its contents is much higher than what is continuously spent to power the clock, most microwave ovens are being idle for more than 99 % of the time. Consequently, the low-power level, accumulated over time, results to be the dominant part of the total consumed energy. Admittedly, the absolute amount of energy, on its own, is still negligible when considering a whole household. But there are many always-on devices in one household, and many more households on a global scale, making the phenomena a sizable problem that deserves to be looked into.

1.1.2 Quantifying Standby Power

Figure 1.1 indicates details about the costs associated with standby energy, or vampire energy. For a broad and more detailed overview on standby power in the USA, a survey held by the Lawrence Berkeley National Laboratory can be consulted online [40]. According to this survey, about 5–10 % of residential electricity in most developed countries is typically caused by devices in standby.

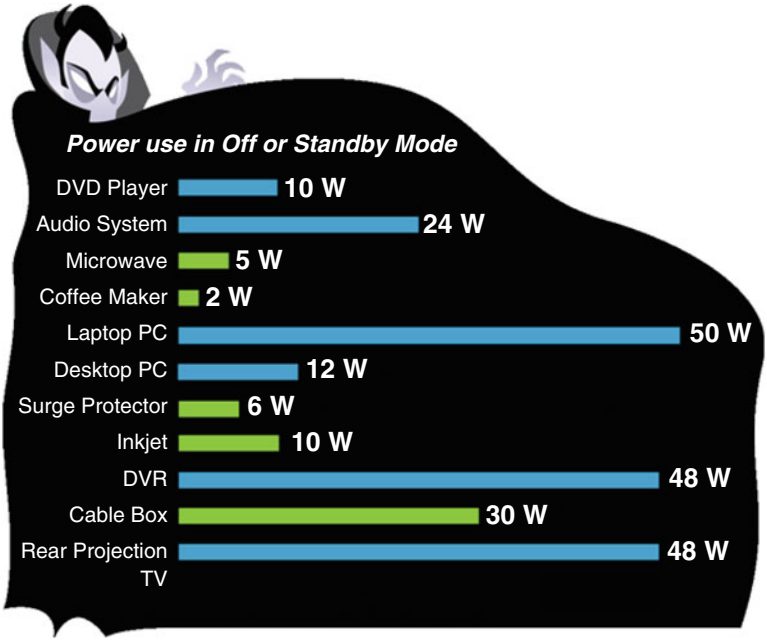

Fig. 1.1 Infographic on vampire power consumption of popular appliances, when off or in standby mode. Reported values are maximum measured values. *Source*: [20, 40]

Table 1.1 Summary of data on the US electricity production

Percentage (%)	Unit	Year
37	US CO_2	2013
31	US GHG	2013

Table 1.2 Summary of data on standby power, or vampire power

Percentage (%)	Unit	Year
5–13	Residential electricity	$\geq$2000
2.7	Global electricity	2013
1	Global CO_2	2007

In Europe, data was collected by the International Energy Agency [109]. Typical consumer culprits include TV, DVD player, set-top box, stereo, computer, kitchen appliances, external power supplies, ceiling fans, automatic garage ports, et cetera. According to the IEA, residential consumption related to standby power accounted for 7 % in France during the year 2000, 8 % in the United Kingdom, 2004, and up to 13 % in other EU member states. Consequently, the IEA data is in accordance to that of the LBL survey.

The consequences of standby power have, next to an economical impact, also an environmental impact. The latter is related to the method with which electricity is generated. When burning fossil fuels to generate electricity, sulfur dioxide (SO_2) and carbon dioxide (CO_2) are emitted. On the one hand, SO_2 is linked to acid rain and adverse effects on the respiratory system. On the other hand, CO_2 is the foremost greenhouse gas (GHG) being emitted through human activity. A study by the Environmental Protection Agency [112] connects 37 % of the total US emitted CO_2 in 2013 to electricity generation. Alternatively, a study by the IEA shows that in 2007, standby power was the cause of 1 % of global CO_2 emissions. To give a measure of magnitude, global air traffic was accountable for 3 % in that same year. From these numbers, it can be seen that standby power is roughly 2.7 % of total electricity consumption. Tables 1.1 and 1.2 combine key numbers on electricity production in the USA and vampire power, respectively.

1.1.3 Future Trend

Even though measures to increase energy efficiency are gaining more attention and are effectively supported by regulatory initiatives, it is a safe assumption to state that the number of mains-connected devices is only increasing. As such, the relative decrease of standby energy is counteracted on an absolute scale by the larger number of appliances, and it is a matter of numbers. Moreover, new evolution like the Internet of Things (IoT), which envisions to connect nearly everything to the internet, poses a large challenge in terms of energy. As an enormous amount of new devices will be always-connected and consequently always-on, the transition between standby and active more becomes less clear. In conclusion, with an ever-growing number of electrical consumers, electricity is a limited

commodity and the importance of energy efficiency, both in the active and standby mode, is increasing. To keep electricity consumption from skyrocketing, it is a necessity to consume this commodity efficiently. When hardware is free, power is expensive [104]. For those devices that are powered from the mains, it is necessary to create mains AC–DC power converters to maximize efficiency in all operational modes.

1.2 Auxiliary Low-Power Converter for High Efficiency in Standby

Section 1.1 introduced and situated the problem context of standby power. The problem originates from the finiteness in efficiency of any practical power converter in combination with the large difference between loading conditions in active and standby mode. Power supplies of electrical appliances are optimized for efficiency in their nominal condition, the active mode. To that end, a power converter is dimensioned to contain active and passive semiconductors that are rated for the voltages and currents of this nominal condition, and to perform this well. However, when in standby, only a fraction of the nominal power is required to be delivered. In this case, the converter is overdimensioned and static loss contributions, that are negligible during nominal output power, start to have a considerable impact on the system efficiency. In other words, due to the fact that the converter operation overhead loss is not fully a function of the converter power, the range of output power in which a converter surpasses a specific efficiency threshold is limited. This is illustrated in Fig. 1.2, where an inflection point in the efficiency can be observed at 20 % of the maximal output power.

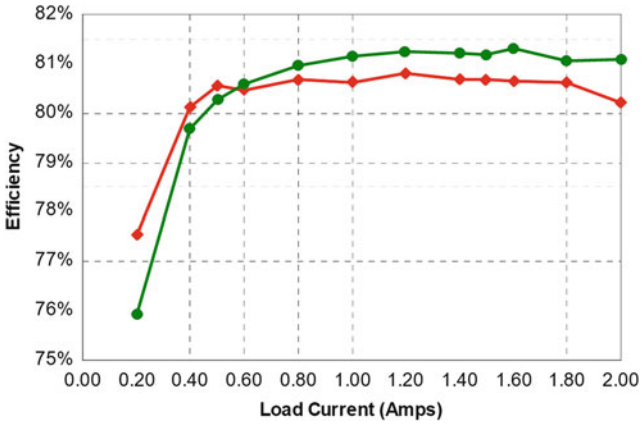

Fig. 1.2 Efficiency of a 10 W USB eco-charger for the US (*diamonds*) and EU (*circles*) mains input. *Source: TI PMP8386*

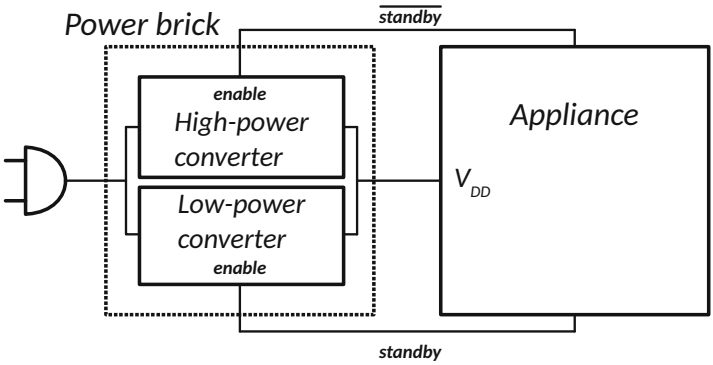

Fig. 1.3 Auxiliary power converter concept for low-loss standby

In order to extend the highly efficient operation to a broader range, this work proposes to use a compact and low-cost auxiliary converter to take over the power conversion at the light-load condition, where the main converter is no longer efficient. Since an auxiliary converter comes down to an additional system cost, a high level of integration is necessary to keep the overhead cost as low as possible. This concept is represented in Fig. 1.3, in which the low-power converter is the only active power converter during standby. It is solely intended to provide the power that is necessary to run the minimal functionality of detecting a user input, which indicates that the functionality of the active mode is once again required.

1.3 Recent Evolution of Power Management Circuits

Next to the introduction of the problem context of standby power consumption and a possible strategy to alleviate the issue, recent evolution in power management circuits is now discussed in this section to bring the problem context in relation to the current state of the art of the technology to address this issue.

A closer look on recent evolution of power management circuits clearly shows an important trend: the trend to go from discrete to fully integrated [103]. The reasons to do so are manifold, and discussed in Sect. 1.3.1. A consequential trend is to go from centralized power management to a distributed or granular power management approach. This is a logical consequence because once the step to monolithic integration is taken, the component count is no longer of importance and flexibility in layout is large. As such, a centralized power distribution approach has become obsolete.

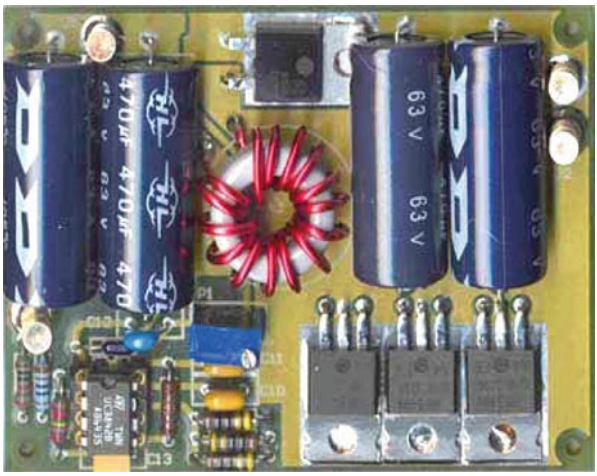

Fig. 1.4 Discrete-component power converter implementation

1.3.1 From Discrete to Fully Integrated

The trend to go from discrete to fully integrated is driven by, on the one hand, the economical advantages of doing so, and on the other hand, the combination of alleviating difficulties in the discrete approach and the performance enhancement of the integrated approach. Figure 1.4 shows a power converter consisting of discrete components. Input and output decoupling along with the magnetic energy transfer component takes up a sizable volume.

The economical benefit is enabled by the reduction of passive components. The power that can be transferred per unit of time depends on both the passive component value, which is a measure of the energy storage capability while transferring energy from input to output, and the switching frequency, which is the rate at which this transfer process takes place. Consequently, higher switching frequencies enable a reduction of the passive component, in turn yielding a cost reduction. On top of that, the power conversion density is higher, which can be marketed as a more compact solution that requires less PCB area.

It must be noted that it is very difficult for integrated passive components to reach quality factors that are common to external passives. As such, there is typically an efficiency penalty when going for an integrated solution, although there are examples with high efficiency available at low-power density [21]. But it does unlock improved performance in other specifications and on the system level, e.g., regulation, response time, power density, number of pins, lower supply voltage overhead margin, power integrity, et cetera. In high-performance digital systems, large currents need to be delivered at low voltage [7]. When the last voltage step-down conversion can be performed by an on-chip voltage regulator, less current needs to be sourced and sunk from the chip, relaxing the power pins and on-chip power grid impedance requirements. Moreover, it is not a trivial task to provide a regulated on-chip supply voltage, in the presence of sudden load steps and an inductive interconnect contribution in the Power Delivery Network (PDN) [3], in

between the power supply output and the actual integrated load. Alternatively, the combination of an on-chip controller at higher switching frequencies enables faster transient responses, due to a reduced latency between successive transfer steps and being less affected by bandwidth-limiting parasitic effects, that are otherwise more pronounced.

Integration of power converters does not always come down to full integration. For example, a mono-package solution, which contains multiple individual parts within a package, is called a Power System-in-Package (PSiP). Alternatively, when everything is integrated monolithically, a true Power System-on-Chip (PSoC) is realized. The PSiP approach is a logical step in a roadmap toward a full PSoC [54, 123], as its more compact physical form factor can decrease issues with interconnect-related parasitic effects. Secondly, using discrete components enables both actives and passives to use an optimized technology for implementation. An example of a PSiP implementation is illustrated in Fig. 1.5. An X-ray of a PSiP product reveals its internal PCB, SMD inductor, SMD capacitors, and active circuit die with bond-wire connections.

However, a Power System-in-Package, despite its compact form factor, is a separate power management integrated circuit (PMIC), with associated power delivery network issues. This is where the Power System-on-Chip approach differentiates itself, as discussed in the next section.

1.3.2 From Centralized to Granularized

As earlier introduced in Sect. 1.3.1, monolithic integration marks the end of centralized power conversion, and introduces additional degrees of freedom that enable to comply with the advanced requirements of power delivery in state-of-the-art SoCs. By having the power converter on the same die as its load, in the case of a PSoC, the PMIC can be distributed into many voltage converters, each located close to their respective load [86]. This concept is visualized in Fig. 1.6.

In order to maximize energy efficiency, many independent supply voltages are required, each optimized for a specific load functionality. For example, the digital, memory, IO, and analog circuits require different voltages, with individual specifications toward load regulation, power supply noise, and more. Within voltage islands, energy saving techniques can be applied, such as the closed-loop AVS, or alternatively, open-loop techniques like DVS and DFS. In the case of a CPU load, the minimum supply voltage V_{min} is a critical parameter to guarantee completion of an execution within the proposed clock period. Local and high-speed on-chip voltage regulators [7, 31] are excellent candidates to meet these stringent power supply requirements, while enabling a boost in energy savings.

However, there is also a cost related to the PSoCs. The drawback of the PSoC implementation approach is that on-chip realizable values of capacitance and inductance are low. This is countered by higher switching frequencies, feasible in an integrated context, but inevitably an on-chip voltage regulator consumes die area.

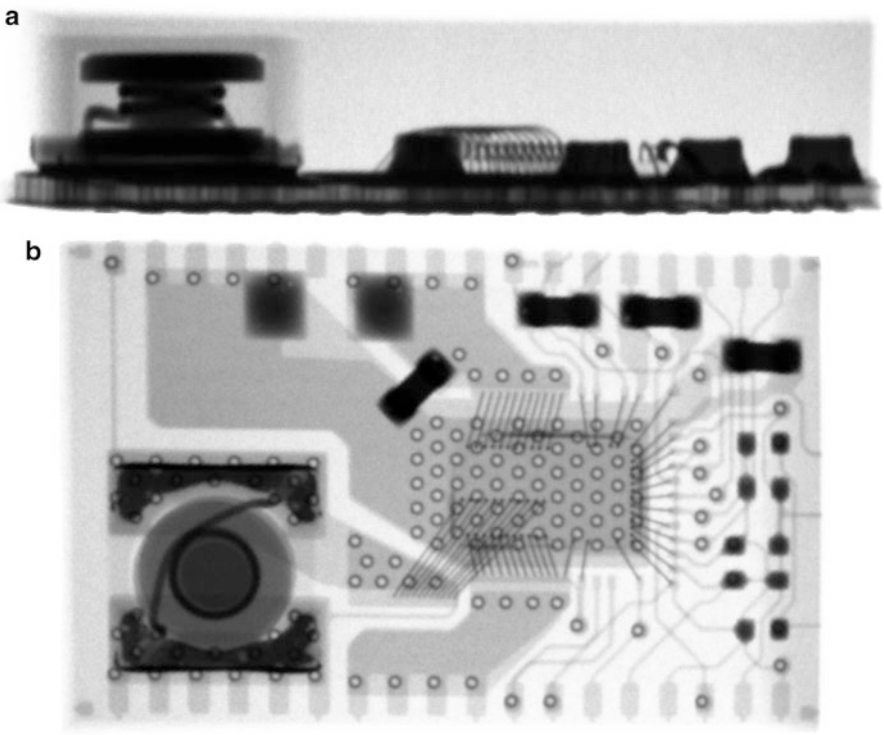

Fig. 1.5 X-ray of a PSiP product, clearly showing the individual discrete components. (**a**) Side X-ray view of a PSiP product, illustrating the inductor impact on minimal thickness. (**b**) Top X-ray view of a PSiP product, demonstrating the discrete components on PCB, but within a package

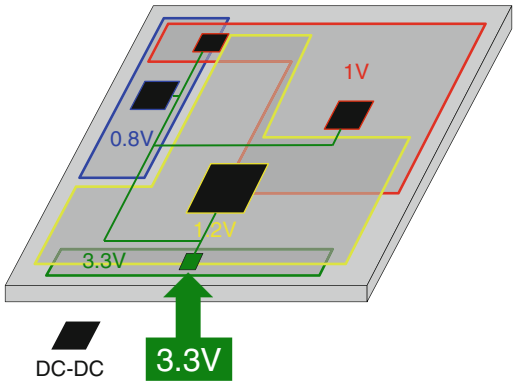

Fig. 1.6 Concept of a Power System-on-Chip approach, with multiple voltage islands and a distributed, granular power delivery

Typically, most die area is used for implementing the passive components [57], which is of course a non-ideal usage of costly nm process technology. This might be the biggest motivation why PSoCs have only mild success in the product space. In conclusion, a PSoC must deliver a sizable performance advantage, in any of its

key specifications such as efficiency, power density, regulation, or cost, to justify its implementation overhead. Whether future PMICs will be PSoC or PSiP, with 2D, 2.5D, or even 3D integration of individual chip dies, remains to be seen.

1.4 Book Outline

The remaining chapters of this revolve around integrated power converters, where full integration preferred, when allowed by the specifications.

To start off, Chap. 2 focuses on the switched-capacitor approach. Through aiming to realize an as high as possible power density, technology limits, converter implementation, and circuit techniques to maximize performance, given the context of a bulk CMOS process, are put to the test. As such, a familiarization of CMOS integrated power conversion is obtained.

Chapter 3 through Chap. 6 discuss mains AC–DC power conversion to resolve the issue of standby power, by targeting power converters that are able to provide the necessary energy to run standby functionality at high efficiency. In Chap. 3, a path toward integration of such power converters is introduced. Consequently, Chap. 4 details a single-stage monolithic AC–DC converter implementation. To continue, Chap. 5 assesses the strengths and weaknesses of this approach in light of the target specifications and moves on toward a more flexible approach, by relaxing the monolithic integration requirement. Again, a realization of the proposed approach is undertaken and Chap. 6 explores the implementation of a high efficiency switched-capacitor DC–DC converter, intended to be used in a two-stage mains AC–DC conversion system. The secondary DC–DC converter is tested together with an example, but not optimized, primary AC–DC converter in order to prove operation in real world conditions.

Whenever attempting to realize mains AC–DC conversion, large voltage conversion ratios are inevitably present. This poses a challenging research question on its own. After having realized a solution-specific, highly integrated high-ratio DC–DC converter in Chaps. 6, 7 now further explores the fundamental limits of high-ratio voltage conversion for switched-capacitor DC–DC converters in the context of monolithic integration in CMOS.

Finally, Chap. 8 concludes this work and looks ahead to future work on integrated power conversion and how it can play a role in tackling the challenges in advanced power delivery.

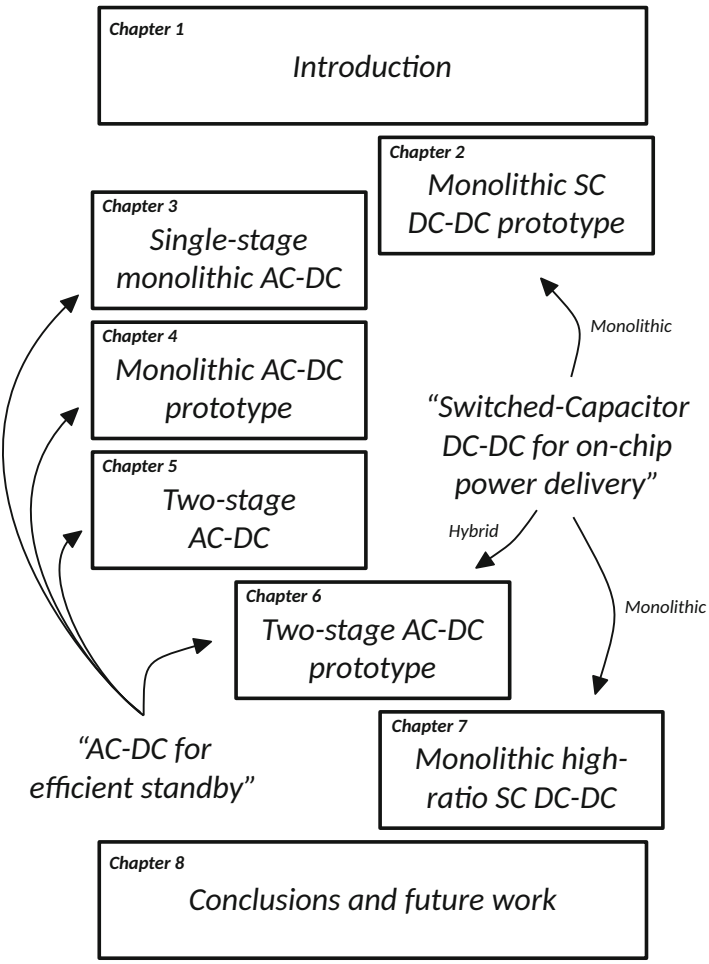

Fig. 1.7 Graphical outline of this work

Chapter 2
Switched-Capacitor DC–DC in Bulk CMOS for On-Chip Power Granularization

2.1 Introduction

Recent trends show that the power management unit (PMU) to supply System-on-Chip solutions is undergoing a transformation and is taking a leap toward monolithic integration [31, 39, 130]. This is a necessary evolution because of multiple market requirements. On the one hand, modern electronic systems are forced to be more energy efficient. This can follow from constraints on heat dissipation, where lower losses result in a lower overall dissipated heat, or to increase the battery autonomy in mobile systems. On the other hand, monolithic integration enables to reduce the form factor of power converters, saving on the required PCB board space. On top of that, the solution thickness can be reduced [122], which has become an important differentiation in modern high-end smartphones. In order to improve system efficiency and form factor reduction, these systems frequently rely on energy saving techniques, such as Adaptive Voltage Scaling (AVS), Dynamic Voltage Scaling (DVS), Dynamic Frequency Scaling (DFS), power and clock gating to realize (deep, etc.) sleep, multiple supply voltages with voltage islands and power domains, and so on. Consequently, the step toward integrated power conversion is a key enabler for the aforementioned techniques because it allows power delivery to take place via a distributed or granular concept, yielding the possibility of many voltage domains. In fact, once power converters are integrated on chip, the concept of having one centralized power converter becomes obsolete. There is no longer a reason to keep the power converter in one place besides tradition, which is not a rational motivation and leads to bad circuit design [30].

A lot of these techniques imply the real-time regulation of the supply voltage or the presence of multiple supply rails in a single application [129]. Another issue of the PMU is its output impedance in combination with the impedance of the power grid, also known as the power delivery network, that is becoming more problematic as circuit supply voltages decrease. Lower supply voltages inevitably

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require larger supply currents, hereby increasing the ohmic losses [38, 63] over the PDN. These issues can be better addressed by means of a number of distributed, high-performance integrated DC–DC converters, as opposed to multiple external converters, which require a low-impedance routing to the chip, take up printed circuit board (PCB) space and many package pins.

DC–DC converters, that intend to face this challenge, should demonstrate high efficiency compared to traditional linear regulation and have a small form factor, i.e., high power density. To obtain such a compact and compatible solution, this chapter investigates the opportunities to integrate the DC–DC converter in the same standard CMOS technology as the system to be supplied, maximizing the added value of an integrated solution [102]. This approach has the advantage that a portion of the external bulky components and their interconnections are no longer required. On top of that, once DC–DC converters are monolithically integrated, a game-changing new playing field emerges with new possibilities, but also new rules. In this context, the converters can take advantage of state-of-the-art circuit techniques, such as fragmented operation (time-interleaved multi-phase operation), which otherwise is unpractical due to a high component count [70, 71]. But as with most innovation, there is no such thing as a free lunch. This means that also the drawbacks of CMOS integration, such as parasitic capacitive coupling, must be taken into consideration.

When integrating conventional DC–DC converters—buck, boost—in a CMOS process, the quality factor of integrated inductors becomes a huge problem. The equivalent series resistance (ESR) of the inductor induces large losses, but also the parasitic capacitive coupling between the inductor and the substrate deteriorates the converter's efficiency. State-of-the-art designs in the literature prove that relatively high power densities can be achieved, but at the cost of efficiency [125, 126]. Better performance can be obtained by going toward a Power System-in-Package, which involves integrating only the active devices in an advanced nm-CMOS process, while implementing the passive components in a cheaper, high-density technology [10]. Even though additional cost is to be expected, related to having an extra die for the passives and co-packaging steps, it is noted that the area of the nm-CMOS die is significantly reduced, as the die area of monolithic power converters is typically dominated by passive components [56]. Especially with the rapidly increasing mask cost of the latest CMOS technologies, which resort to double and triple patterning for the smallest feature sizes [23], it is increasingly prohibitive to waste precious area to passive components and this approach gains all the more relevance.

Next to inductive-based DC–DC converters, capacitive-based DC–DC converters are gaining interest. In the past they were used for low-current, high-conversion-ratio applications [17]. An application example is their use in EEPROM and flash memory to generate the high-voltage levels to erase the memory cells. These switched-capacitor converters, or charge pumps, use nothing but switches and capacitors to perform a fixed voltage conversion ratio. The maximum attainable ratio is dependent on the number of capacitors in the converter topology [53]. Behavioral [90] and state-space models [28] characterize the capacitive converter's output impedance allowing straightforward design. Recently, fully integrated capacitive

converters are appearing that report both a high power density and a high efficiency using the advantages of SOI technology [42] and exploiting the capacitance density of deep trenches [13]. Although their baseline CMOS counterparts show high efficiency, they stay behind in power density [115, 119] due to typical limitations resulting from a CMOS implementation. To mitigate the drawbacks of CMOS integration, the presented converter in this chapter employs the Flying-Well and Intrinsic-Charge-Recycling techniques and demonstrates that these enhancements enable improved specifications, achieving a power density of 0.77 W/mm^2 and an efficiency of 69 % in a monolithic solution.

This chapter will discuss the operation of switched-capacitor DC–DC conversion, by means of a 2:1 step-down conversion, in Sect. 2.2. Section 2.3 introduces the technology difficulties of using a bulk CMOS process to implement SC conversion. Circuit techniques are proposed to, on the one hand, reduce the drawbacks of CMOS and, on the other hand, recycle the parasitic effects into a positive contribution. Implementation and performance validation are reported in Sects. 2.5 and 2.6, respectively.

2.2 Topology of a 2:1 Step-Down Switched-Capacitor DC–DC Converter

2.2.1 Operation

The topology of the capacitive converter's power conversion core is shown in Fig. 2.1. It consists of four switches ($M1$–$M4$) and a charge-transfer capacitor (C_{fly}) to transfer charge from input to output in a 2-phase alternated operation. For sake of simplicity, the input voltage is ideal and the output capacitor C_o is infinite. Even though this topology is intended to perform a 2:1 step-down, the effective output voltage $V_o(= V_{o,eff})$ is slightly lower than half of the input voltage V_i. This voltage drop V_{R_o} is caused by the voltage divider formed by the output impedance R_o of the converter and the load impedance R_L (Fig. 2.11) and this voltage divider ratio is in this work denoted by parameter γ. Thus, $V_o = \gamma \frac{V_i}{2} = \gamma V_{o,id}$, in which $V_{o,id}$ is the ideal output voltage when no load current is present and consequently no voltage

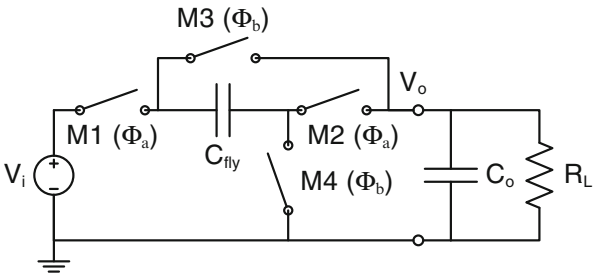

Fig. 2.1 Power conversion cell topology

drop over R_o occurs. Consequently, from a pure voltage conversion ratio perspective, which excludes the dynamic switching losses, the efficiency of an SC converter can be calculated as $V_{o,AVG}/V_{o,id}$, which equals γ under the assumption that $C_{out} = \infty$, so that $V_{o,AVG} = V_{o,DC}$. This is the equivalent of considering an SC DC–DC as a combination of a lossless DC-transformation, with the step determined by the VCR, and a subsequent lossy voltage divider, composed of the SC output impedance and the load impedance.

During phase (Φ_a) the flying capacitor is switched between the input terminal (V_i) and the output terminal (V_o) by closing switches $M1$ and $M2$. Hereby, C_{fly} is charged to a voltage $V_i - V_o$, which is $2V_{R_o}$ larger than V_o due to the non-zero output impedance as explained above. At the same time charge is delivered to the load because the flying capacitor is charged in series with the output. In the next phase (Φ_b), the charge-transfer capacitor C_{fly} is relocated between the output terminal and ground by closing $M3$ and $M4$. C_{fly} discharges into the output and again charge is delivered. Each conversion cycle C_{fly} is charged and discharged by the voltage difference $\Delta V_{C_{fly}} = 2(V_{o,id} - V_o) = 2V_{R_o}$. It is this voltage variation that is responsible for the charge transfer. Continuously alternating between these 2 phases results in an output current being supplied to the load.

This charging and discharging process is also shown in detail in Figs. 2.2 through 2.4. A view of the separate switched-capacitor topology configurations is shown in Fig. 2.2, making abstraction of the switches. Figure 2.3 provides insight in the actual flying capacitor C_{fly} state as function of time. The flying capacitor voltage levels, from which and to where (dis)charge takes place, are given. The full switching cycle consists of the following sequence: C_{fly} discharges during $\Phi_b \rightarrow$ topology reconfiguration to Φ_a by relocation of $C_{fly} \rightarrow C_{fly}$ charges during $\Phi_a \rightarrow$ topology reconfiguration to Φ_b by relocation of C_{fly}. The effect of this switched-capacitor operation, and the associated charge sharing in between C_{fly} and C_{out}, is demonstrated in Fig. 2.4. The output is assumed to be loaded with either a constant load current or either a resistive load. In case of the latter, the time constant at the output of the converter is assumed to be much larger than the switching frequency. The consequence of the output decoupling capacitor value C_{out}, or more comprehensively: the ratio of flying capacitor value to the output capacitor value, on the charge sharing and its effect on the output voltage can be noticed in the different scenarios of Fig. 2.4a through 2.4d. Each scenario depicts a different C_{out} value, and as such a C_{fly} to C_{out} ratio. It can be seen in Fig. 2.4a that, in the absence of C_{out},

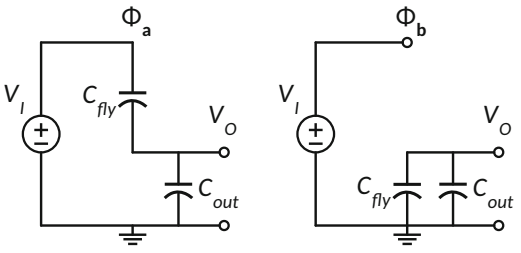

Fig. 2.2 Phase Φ_a and phase Φ_b shown separately for a 2:1 step-down converter topology

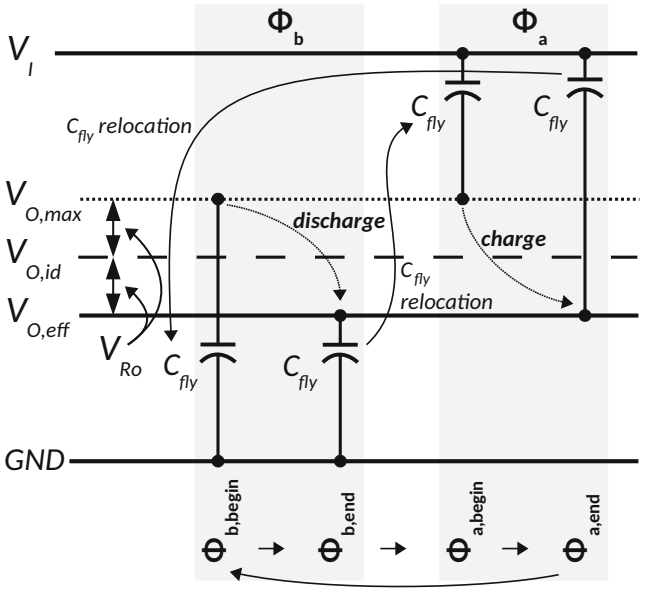

Fig. 2.3 Charging and discharging of capacitor C_{fly}, indicated over time at its most significant instants: the beginning and ending of each of the two phases

no charge sharing takes place. In this case, $v_{OUT,AVG} = V_{O,id}$ and efficiency equals 100 %, given ideal switches and ideal capacitors. But, given the fact that the output voltage $v_{OUT}(t)$ now is intended to have a voltage ripple in this mode of operation, due to the absence of an output decoupling capacitor, this circuit is no longer a DC–DC converter in its strict sense. However, DC–DC converters, those in the strict sense, also exhibit voltage ripple in realistic conditions. As such, aside from the definition of a DC–DC converter, both circuits yield a very similar output and can be categorized as DC–DC converter in the opinion of the author. Figure 2.4b, c shows the scenario of increasing the value of the output decoupling capacitor C_{out} toward a value of infinity in Fig. 2.4d. In this last case, $v_{OUT,AVG} = V_{O,eff}$ and the efficiency is set by the parameter γ, earlier introduced to denote the voltage division ratio of the output and load impedance. The modeling work of Seeman and Sanders [90], that describes the converter output impedance, assumes this condition of infinite output decoupling capacitance. In practice, the output capacitor is finite and the output impedance is more accurately described by the model of Van Breussegem and Steyaert [116], which builds further upon [90]. It can be concluded that the worst-case theoretical efficiency of a switched-capacitor DC–DC converter is set by ratio of $V_{O,eff}$ to $V_{O,id}$, when C_{out} is infinite. But in practice with a finite C_{out}, the output is not a perfect DC voltage and the efficiency is set by the ratio of $v_{OUT,AVG}$ to $V_{O,id}$. As such, there is a trade-off in between output voltage ripple and efficiency. In this trade-off, it is possible to choose for either quality of the voltage or quality of the converter performance.

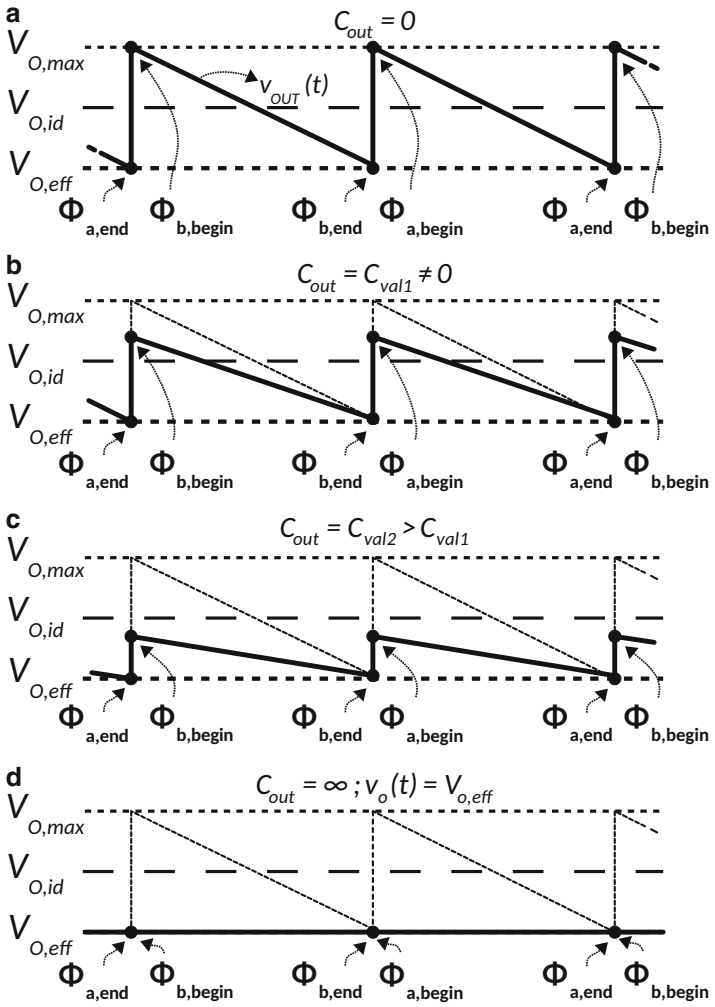

Fig. 2.4 Output voltage variation and evolution over time as result of the switched-capacitor operation, for multiple C_{out} scenarios and idealized switch conductance. (**a**) Output capacitor $C_{out} = 0$. (**b**) $C_{out} = C_{val1} \neq 0$. (**c**) $C_{out} = C_{val2} > C_{val1}$. (**d**) $C_{out} =$ infinite

2.3 Techniques

2.3.1 CMOS Integration Difficulties

Parasitic effects have a large impact on the design of CMOS integrated capacitive converters. Especially the ESR of the flying capacitor ($R_{ESR,C_{fly}}$) and the parasitic capacitor $C_{par}(= \alpha C_{fly})$ between the bottom plate and the substrate decrease efficiency and limit the maximum output power. Due to their high capacitance

density in comparison to other types of integrated capacitors, MOS-capacitors were selected for implementation. Unfortunately, these capacitors are also the ones that suffer most from the parasitic effects.

On the one hand, the conductive inversion channel plate of a MOS-capacitor imposes a substantial contribution to its equivalent series resistance $R_{ESR,C_{fly}}$. However, this can be decreased in layout by tuning the W/L ratio of the MOS-capacitor. The equivalent series resistance can be lowered by decreasing the channel length, but at the cost of a decreased capacitance density, due to fixed drain/source diffusion overhead in layout, which does not contribute to the MOS-capacitor capacitance. On the other hand, the conductive channel is closely embedded in the substrate and exhibits a high parasitic coupling α. Two techniques are proposed to provide a workaround in standard CMOS. The bottom-plate parasitic coupling parameter α in this design is reduced by means of the Flying-Well technique. The remaining bottom-plate parasitic capacitor is exploited to increase the power density by the Intrinsic-Charge-Recycling (ICR) technique.

2.3.2 *Flying-Well Technique*

The Flying-Well technique lowers the parasitic capacitive coupling to the substrate by biasing the body well such that the regular parasitic capacitance is traded in for a smaller capacitance. The regular parasitic, in case of a PMOS-capacitor according to Fig. 2.5, is mainly formed by the junction capacitance of the drain/source terminals to the n-well body of the transistor. Opposed to tying the n-well to a fixed bias voltage, for example, the input voltage, in this approach the n-well is connected to the drain/source terminals of the PMOS-capacitor as shown in Fig. 2.5. This shorts the drain/source to n-well junction capacitor, eliminating it. However, there is a new parasitic capacitance, which is the capacitor formed by the n-well to bulk junction. This junction capacitance is much smaller and thus the parasitic coupling is reduced from over 5 % of C_{fly} to $\alpha = 1.3\,\%$ as indicated by simulation results in the case of this converter.

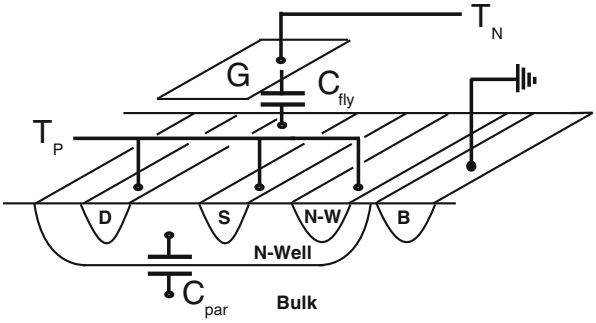

Fig. 2.5 Flying-Well biasing technique. D/S to N-well junction shorted. Bulk to N-well junction is new C_{par}

As alternative to the approach in this work, the PMOS-capacitor N-well can also be biased by a very high-ohmic connection to the input voltage, approximating the situation in which the N-well is left floating [43]. This causes both the drain-source parasitic junction capacitance and N-well-to-substrate parasitic junction capacitance to be seen in series, from the PMOS-capacitor channel to substrate point of view. Even though the technique in this work does not have the advantage of placing both parasitics in series, both approaches result in fairly similar $C_{par,tot}$ values. This is due to the fact that $C_{Nwell-to-subs} \ll C_{drain,source-to-Nwell}$, and the total capacitance in a series connection of capacitors, in which one is much smaller than the other, is only slightly smaller than the smallest of the two capacitances. Moreover, the body-to-source voltage V_{BS} in the approach of this work is zero because the N-well is shorted to the drain and source terminals, eliminating a negative effect on the channel conductance if this voltage were non-zero. The V_{BS} in [43] is non-zero as it is biased to the input voltage.

2.3.3 Intrinsic-Charge-Recycling Technique

Even though the use of the Flying-Well technique reduces the parasitic coupling considerably, the remaining parasitic effect still limits the maximum achievable efficiency of the converter in comparison to technologies such as SOI, which inherently suffer less from substrate coupling due to the presence of a thick oxide in between the circuit and the semiconductor substrate. The Intrinsic-Charge-Recycling technique aims to reverse the loss of the parasitic capacitor C_{par} into a recycled benefit. The concept is to recuperate charge that is stored on the parasitic capacitor and direct it toward the output, instead of letting it get wasted toward ground. Figure 2.6 shows the different possible scenarios: (a) the parasitic capacitor is present at the negative terminal of the charge-transfer capacitor C_{fly}, and (b), in which the parasitic capacitor is connected to the positive terminal of C_{fly}. In case (a), C_{par} is first charged during Φ_a by the output terminal, and is discharged into the ground in Φ_b, as C_{fly} is relocated between output and ground. Alternatively in case (b), when the parasitic capacitor C_{par} is present at the positive voltage terminal, C_{par} is charged by the input during Φ_a. Afterwards in Φ_b, the parasitic capacitor discharges into the output. The charge stored on the parasitic capacitor is not lost, it is delivered to the output instead. Consequently, the output power is increased, instead of reduced.

However, there is a difference in the charge transportation efficiency from input to output by C_{fly} and C_{par}. During a charge/discharge cycle the voltage difference, that the flying capacitor is subjected to, is approximately equal to twice the voltage drop over the output impedance ($\Delta V_{C_{fly}} = 2V_{R_o} = V_i - 2V_o$), which is set by voltage division ratio γ and is supposed to be small. Consequently only a small amount of energy is lost in this charge-transfer process as the flying capacitor voltage ripple is small. This leads to an efficient voltage conversion, set by parameter γ, as discussed earlier in Sect. 2.2.1. The conversion that is performed by recycling charge from the

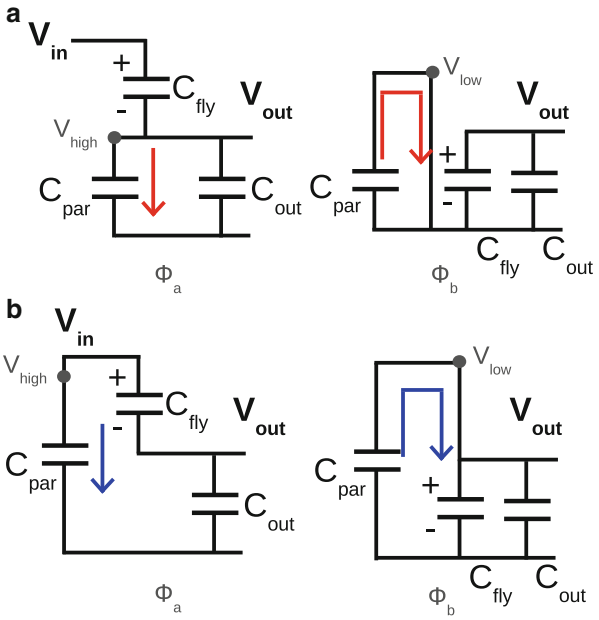

Fig. 2.6 Intrinsic-Charge-Recycling technique. (**a**) Regular case where C_{par} is connected to the negative terminal of the flying capacitor $C_{fly,-}$. (**b**) ICR case: C_{par} is connected to the positive terminal of the flying capacitor $C_{fly,+}$

parasitic capacitor is less efficient, since the voltage variation seen by this parasitic capacitor is larger and approximately equal to $(\frac{Vi}{2} + V_{R_o} = V_i - V_o)$. Hereby, the charge conversion contribution of this capacitor equals that of a switched-capacitor resistor, and the efficiency is therefore equal to that of its linear regulation equivalent. Even though the conversion associated with the recycling is less efficient than that of the actual converter operation, it is important to note that by applying Intrinsic Charge Recycling in the converter, the output impedance is decreased instead of being increased.

The performance enhancement realized by using this strategy is that for the same switching frequency, the output power can either be higher, or either that the same output power can be obtained with a lower switching frequency, which yields a higher efficiency. Simulations have shown that in the case of this prototype converter the output impedance was reduced by 5 %. Intrinsic Charge Recycling can easily be established in CMOS by implementing the flying capacitor with PMOS-capacitors, as the positive capacitor terminal is formed by the inversion channel, closely embedded in the substrate.

The location of the parasitic capacitor also has consequences from an energy point of view. Considering the ICR case, it is seen that the parasitic capacitor C_{par} in Fig. 2.6b swings with a voltage difference $\Delta V_{C_{par,ICR}} = V_{high} - V_{low}$, equal to $V_i - V_o$. The voltage difference in the regular case, of Fig. 2.6a, is $\Delta V_{C_{par,REG}} = V_o$.

Thus, $\Delta V_{C_{par,ICR}} > \Delta V_{C_{par,REG}}$ and consequently the ICR scenario is more lossy than the regular scenario. However, the ICR case offers in return the recycling benefits otherwise not present, because C_{par} is first charged by the input, after which this charge is then transferred to output. Moreover, in the regular non-ICR case, the charge with which C_{par} is being charged comes from the output, and was transferred to the output at a finite conversion efficiency.

To investigate the system performance improvement of Intrinsic Charge Recycling, the efficiencies of both scenarios are now calculated and compared. Figure 2.7 schematically represents the energy flow from input to output, and indicates where losses take place as result of lossy energy transfer steps. The ideal case of $\alpha = 0$ is demonstrated in Fig. 2.7a. During phase Φ_a, the flying capacitor C_{fly} is charged by $\Delta V_{C_{fly}}$. This charging process requires an amount of energy from the input equal to:

$$E_{in,ideal} = C_{fly} \Delta V_{C_{fly}} V_i. \tag{2.1}$$

The same charge also flows to the output, since C_{fly} is connected in series with the output, and delivers an amount of energy $E_{out,\Phi a}$ to the output:

$$E_{out,\Phi a} = C_{fly} \Delta V_{C_{fly}} V_o. \tag{2.2}$$

During the second phase, Φ_b, the flying capacitor is put in parallel to the output and now discharges into it, delivering $E_{out,\Phi b}$ to the load, given by:

$$E_{out,\Phi b} = C_{fly} \Delta V_{C_{fly}} V_o = E_{out,\Phi a}. \tag{2.3}$$

The efficiency of the ideal scenario can now be used to validate the formulas by calculating the ratio of the total output energy to the total input energy of this scenario.

$$\eta_{ideal} = \frac{E_{out,\Phi a} + E_{out,\Phi b}}{E_{in,ideal}} = \frac{2V_o}{V_i} = \gamma \tag{2.4}$$

Equation (2.4) confirms that the efficiency in this ideal scenario is set by the voltage division ratio of the output impedance to the load impedance.

The next scenario under investigation is shown in Fig. 2.7b, which is the regular, non-Intrinsic-Charge-Recycling scenario, when the parasitic coupling C_{par} is located at the negative flying capacitor terminal. Next to the energy formulas derived above, for the absence of a C_{par} coupling, there is now an additional energy loss taking place in phase Φ_a, due to the charging of C_{par} by the output:

$$E_{chargeLoss,C_{par},\Phi a} = C_{par} V_o^2. \tag{2.5}$$

Again, the efficiency of this regular scenario can now be obtained by taking the ratio of the total output energy to that of the input. The efficiency of the regular scenario is then given by the following equation:

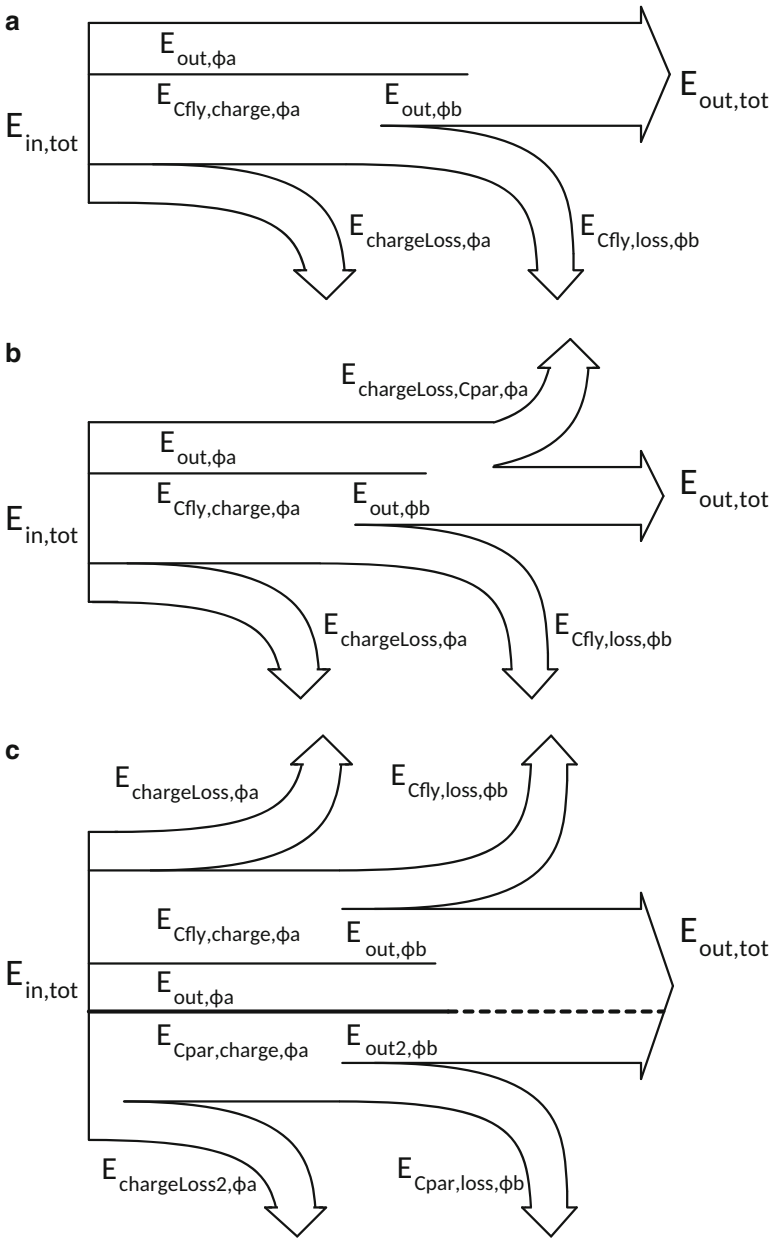

Fig. 2.7 Sankey diagrams of the energy flow in different scenarios. (**a**) Energy flow in the absence of a bottom-plate parasitic coupling C_{par}. (**b**) Energy flow in the regular non-Intrinsic-Charge-Recycling case, showing an additional loss flow at the output. (**c**) Energy flow in the Intrinsic-Charge-Recycling scenario, consisting of the energy flow of the ideal case in parallel to the energy flow as result of C_{par}

$$\eta_{REG} = \frac{E_{out,\Phi a} + E_{out,\Phi b} - E_{chargeLoss,C_{par},\Phi b}}{E_{in,ideal}}, \tag{2.6}$$

in which substitution of Eqs. (2.1)–(2.3) and (2.5) yields

$$\eta_{REG} = \frac{2C_{fly}\Delta V_{C_{fly}} V_o - C_{par} V_o^2}{C_{fly}\Delta V_{C_{fly}} V_i}, \tag{2.7}$$

and finally by substitution of $C_{par} = \alpha C_{fly}$, $V_o = \gamma V_{o,id}$, $\Delta V_{C_{fly}} = V_i - 2V_o$, and $V_i = 2V_{o,id}$:

$$\eta_{REG} = \frac{1}{4}\frac{\gamma(\alpha\gamma + 4\gamma - 4)}{\gamma - 1}. \tag{2.8}$$

Whereas the efficiency in the absence of a bottom-plate parasitic coupling is only dependent on γ, it is now a function of both γ and α.

To complete the analysis, a similar derivation of the efficiency is now repeated for the Intrinsic-Charge-Recycling scenario. As shown in Fig. 2.7c, this scenario can be interpreted as two energy conversion paths in parallel. On the one hand, there is the efficient energy conversion path of the actual switched-capacitor operation with small flying capacitor voltage ripple and the energy calculations of the ideal scenario apply. On the other hand, there is a switched-capacitor path, due to the bottom-plate parasitic coupling C_{par}, in which the capacitor voltage ripple is much larger and where the charge-transfer process is consequently much less efficient. The additional energy, during phase Φ_a, from the input to charge C_{par} equals:

$$E_{in,ICR,additional} = C_{par}\Delta V_{C_{par}} V_i. \tag{2.9}$$

During phase Φ_b, this parasitic coupling is discharged into the output and contributes to the total output energy, albeit at the conversion efficiency of its linear regulation equivalent. This energy $E_{out2,\Phi b}$, from Fig. 2.7c, is given by:

$$E_{out2,\Phi b} = C_{par}\Delta V_{C_{par}} V_o. \tag{2.10}$$

The efficiency of the Intrinsic-Charge-Recycling scenario is then obtained by:

$$\eta_{ICR} = \frac{E_{out,\Phi a} + E_{out,\Phi b} + E_{out2,\Phi b}}{E_{in,ideal} + E_{in,ICR,additional}}, \tag{2.11}$$

which in combination with (2.1)–(2.3), (2.9), and (2.10) expands to:

$$\eta_{ICR} = \frac{2C_{fly}\Delta V_{C_{fly}} V_o + C_{par}\Delta V_{C_{par}} V_o}{C_{fly}\Delta V_{C_{fly}} V_i + C_{par}\Delta V_{C_{par}} V_i}, \tag{2.12}$$

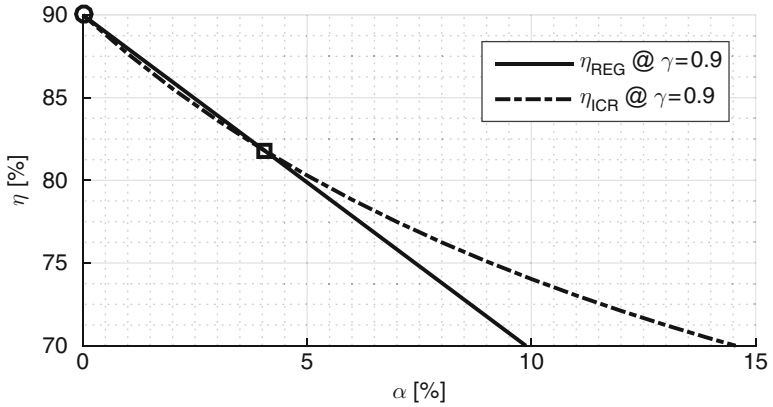

Fig. 2.8 Efficiency of both the regular as well as the Intrinsic-Charge-Recycling scenario for a $V_o/V_{o,id}$ ratio of 0.9

and results, with substitution of $C_{par} = \alpha C_{fly}, V_o = \gamma V_{o,id}, \Delta V_{C_{fly}} = V_i - 2V_o$, $\Delta V_{C_{par}} = V_i - V_o$, and $V_i = 2V_{o,id}$, into the condensed form:

$$\eta_{ICR} = \frac{1}{2}\frac{\gamma(\alpha\gamma - 2\alpha + 4\gamma - 4)}{\alpha\gamma - 2\alpha + 2\gamma - 2}. \tag{2.13}$$

Equations (2.8) and (2.13) summarize the efficiency of both scenarios as function of α and γ. Figure 2.8 plots the result for $\gamma = V_o/V_{o,id}$ ratio of 0.9. As expected, when $\alpha = 0$, both cases are coincidental and simplify to the ideal scenario efficiency γ. When the flying capacitor is not ideal and exhibits a bottom-plate parasitic coupling percentage α, it can be seen that for low coupling percentages below about 4 %, the regular scenario yields a slightly better efficiency result. A break-even between the regular and the ICR scenario takes place at 4.04 %, after which it is better to have the parasitic coupling capacitor located at the positive flying capacitor terminal.

A more general analytic solution of this trade-off can be computed by equating Eqs. (2.8) and (2.13), and solving for parameter α:

$$\alpha_{break-even} = \{0, -\frac{4(\gamma^2 - 2\gamma + 1)}{\gamma(\gamma - 2)}\} \tag{2.14}$$

Next to the trivial solution of α being zero, the break-even is now visualized in the $\alpha - \gamma$ plane in Fig. 2.9. Depending on the operation point of the converter, it is now clear which mode of operation yields the highest efficiency, given a fixed flying capacitor and not including other converter losses.

The total system performance perspective, however, exceeds the efficiency point of view. On the one hand, the power density of both non-ideal scenarios is different.

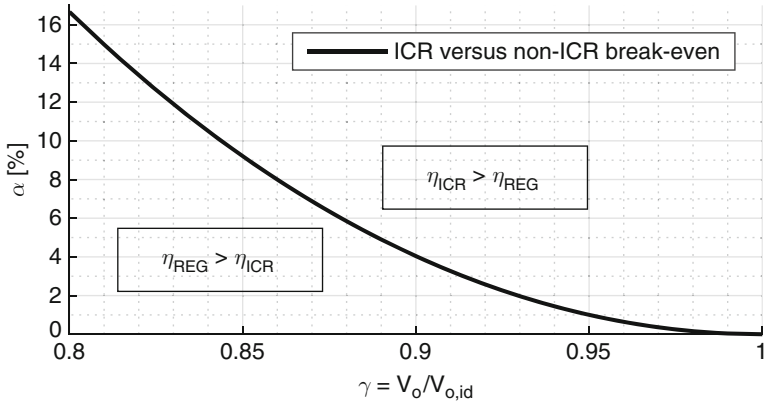

Fig. 2.9 Break-even between the ICR and the regular scenario as function of the operation point: α and γ

Where the power throughput in the ICR scenario is increased, because the intended switched-capacitor DC–DC operation is aided by an inefficient switched-capacitor linear regulation path, the power density is decreased in the regular scenario, due to the switched-capacitor resistor leakage to ground. The power density can be considered by taking the ratio of the total output energy per flying capacitor. This is a valid assumption if the flying capacitor area closely matches the total die area, which in a CMOS context is indeed the case. Consequently, the power densities of the regular and the ICR scenario are given by Eqs. (2.15) and (2.16), respectively:

$$PD_{REG} = \frac{E_{out,tot,REG}}{C_{fly}} = \gamma V_{o.id}^2(4 - \alpha\gamma - 4\gamma) \tag{2.15}$$

$$PD_{ICR} = \frac{E_{out,tot,ICR}}{C_{fly}} = \gamma V_{o.id}^2(4 - \alpha\gamma - 4\gamma + 2\alpha) \tag{2.16}$$

Not surprisingly, the power density is also a function of the output voltage. This follows from the fact that the voltage drop over the converter output impedance $V_{R_o} = V_{o,id} - \gamma V_{o,id}$, for a given $\gamma = V_o/V_{o,id}$ ratio, and is larger with increasing output voltage. Consequently, this larger allowable overdrive voltage over the converter output impedance yields a larger output current and an associated output power. Of course a lower γ also increases the output impedance overdrive voltage, but this reduces the efficiency as both the output voltage and the voltage conversion ratio deviate from their ideal, open-circuit output values.

In order to continue the comparison between the ICR and the regular scenario, the power density improvement by selecting the ICR technique is now given by the ratio of the power density with ICR to that without ICR:

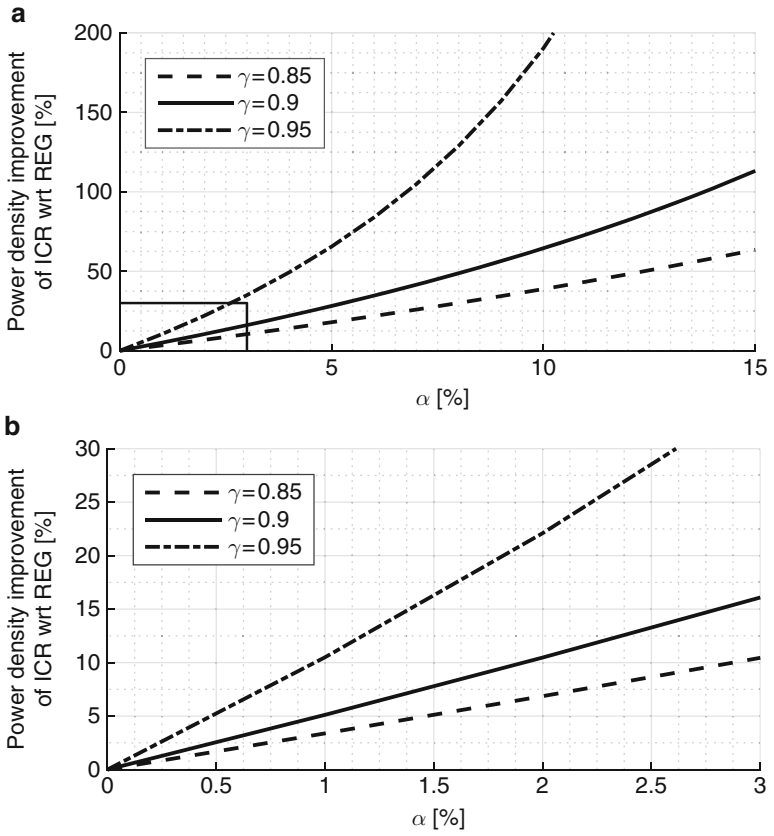

Fig. 2.10 Power density improvement of ICR with respect to the regular scenario. (**a**) Power density improvement of ICR, up to large parasitic coupling ratios. The *box* in the *lower left corner* indicates the area of the plot that is enlarged in (**b**). (**b**) Power density improvement of ICR, close-up in the case of a low parasitic coupling ratio

$$PD_{gain} = \frac{\text{Eq. (2.16)}}{\text{Eq. (2.15)}} = \frac{4 - \alpha\gamma - 4\gamma + 2\alpha}{4 - \alpha\gamma - 4\gamma}. \tag{2.17}$$

This power density gain ratio is shown in Fig. 2.10a, for capacitors with relatively high parasitic coupling ratios, and more in detail in Fig. 2.10b, for higher quality capacitors with a lower bottom-plate parasitic coupling. The results are also plotted for several γ settings, and it can be seen that even very low α coupling percentages can give rise to a large improvement in the power density, especially for high γ values. With respect to a highly efficient switched-capacitor DC–DC operation, exactly these high γ values are necessary.

When comparing the ICR scenario to the regular one, it is unfair to only consider the absolute efficiency and the resulting trade-off of Fig. 2.9. It is more fair to

compare both scenarios at equal power density. This means that the power density improvement, as given in Fig. 2.10a, is traded into a corresponding lower switching frequency. In turn, this reduces the switching associated losses and improves the conversion efficiency. The Intrinsic-Charge-Recycling technique is thus a useful technique to, given the parasitics that inevitably remain after having applied other circuit techniques in order to minimize the parasitic effects, make the best of the situation. It is noted that, as indicated by Fig. 2.8, there can be a penalty of selecting the ICR scenario over the regular one, for the lower α range of capacitors. However, this penalty is relatively small and toward higher γ values, this penalty becomes even smaller. In conclusion, considering the bigger picture involves considering the possible efficiency penalty, of selecting the ICR scenario for low α values, versus the efficiency gain that is obtained, by reducing the switching frequency in the ICR scenario to obtain an equal resulting power density for fair comparison to the regular scenario. Therefore, it can be concluded that the application of the Intrinsic-Charge-Recycling technique is highly likely to be the better option. Depending on the operation conditions α and γ, the performance improvement can turn out to be significant and can be calculated with Eqs. (2.8), (2.13), and (2.17).

2.3.4 Multi-Phase Time Interleaving

Multi-phase time interleaving is an effective technique to reduce the ripple in power converters [100, 113, 119]. The principle is to take a converter and subdivide it into N smaller fragments, which are operating in parallel, but the switching occurs on different time instants. Each fragment operates at the same base frequency as before, but fragments are activated sequentially every $T_{CLK}/2N$, where T_{CLK} is the clock period of the base switching frequency and the factor two in the denominator is caused by the two-phase operation. The benefits of this technique can be seen on multiple levels.

First, although the base switching frequency is unchanged, the output voltage ripple frequency is increased by a factor N. This relaxes the specification of the output filter, reducing the required passive component values to realize a targeted ripple attenuation. Secondly, in the case of switched-capacitor DC–DC converters, the requirement on the output decoupling capacitor is reduced because the charge transferred per converter phase configuration transition is N times smaller. Consequently, the charge sharing of the flying capacitor fragment and the output decoupling capacitor will cause a smaller positive deviation of the output voltage, since the C_{fly} to C_{out} ratio is reduced. A third aspect, which is also specific to switched-capacitor DC–DC converters, is that a dedicated decoupling capacitor is no longer necessary. The $N-1$ converter fragments, that are configured in either of the two possibilities, have their flying capacitor either in series or in parallel with the output, in case of a 2 to 1 converter. As such, this flying capacitance is adding to the decoupling of the output. Other voltage conversion ratio topologies benefit less

than that with a ratio of two, but the concept is still valid. Moreover, elimination of a dedicated output decoupling capacitor greatly enhances the power conversion density [41, 56].

Conceptually, multi-phase time interleaving can be summarized as a technique that reduces the C_{fly} to C_{out} ratio and yields all benefits that follow from doing so. From this perspective, Fig. 2.4 is also valid in this case.

2.3.5 *Avoiding Multi-Phase Time Interleaving*

Next to the many positive aspects of multi-phase time interleaving, Sect. 2.2.1 and Fig. 2.4 describe that allowing an output voltage ripple can yield a higher converter efficiency. This concept is being explored in the work of Zimmer et al. [130] to improve the system efficiency of a digital SoC. However, the earlier work of Le et al. [42] advocates to use the multi-phase interleaving to improve the system efficiency of a digital SoC. These conflicting perspectives are now discussed.

Typically, digital circuits are operated synchronously with a clock. In order to ensure that digital logic circuits function correctly, they must complete their input-to-output transition within the clock period, while respecting all setup and hold times of other logic cells they interface with. This comes down to the verification that the computation time of the slowest cell, which forms the critical path, is less than the clock period, and this in the worst-case scenario. Such a worst-case scenario involves, among many other process variation effects, the worst-case supply voltage. As the supply voltage is lower, digital circuits run slower, therefore a minimum supply voltage specification is an important part in the selection of the maximum possible clock frequency. In the static scenario, where a circuit is always operating at this frequency, any voltage surplus above this minimal specified supply voltage level is a loss. This is due to the fact that, as a higher voltage will speed up the digital computations, these computations will consume more energy associated with the charging and discharging of gate capacitors in the digital logic, given by:

$$E_{C,supply} = Q_{cap} V_{supply} = C V_{supply}^2 \tag{2.18}$$

However, the fact that a logic computation is completed in a shorter time does not yield any benefit, since the clock period is fixed, and everything remains idle until the next clock period. In this case, multi-phase time interleaving is the best approach, since it will minimize the voltage ripple excursions above the minimal output voltage. Therefore, it is better to reduce the C_{fly} to C_{out} ratio as much as possible. This can be verified by considering that, if a digital load is modeled by an equivalent resistance, the power at the input of a 2:1 switched-capacitor DC–DC converter is given by:

$$P_{in,DC-DC} = \frac{P_{load}}{\eta_{DC-DC}} = \frac{V_{load,RMS}^2}{R_{load}} \frac{V_{in}}{2V_{load,AVG}} \tag{2.19}$$

Equation (2.19) shows that a higher $V_{load,RMS}$ will increase the input power, while there is no improvement in the performance of the digital load.

The merit of not applying multi-phase time interleaving relies on the premise of being able to apply dynamic voltage scaling on a cycle-by-cycle basis, as function of the actual time-varying supply voltage. Only then, it is possible to end the clock period right after the critical path has completed its action. As such, there is no time spent idle, while waiting for the next clock period. This enables for the system to go in sleep after a job has been completed in a shorter time frame. Combined with a higher η_{DC--DC}, as discussed in Sect. 2.2.1, the non-interleaving, or rippled V_{supply}, operation can in theory provide a lower input power. It must be noted that the non-interleaving scenario will provide a higher average load voltage over the supply, resulting in an increased energy/operation. However, the input voltage of the non-interleaving converter can be reduced to make the average load voltages more similar and minimize the energy/operation difference for both scenarios. A drawback of not applying multi-phase time interleaving is that DC–DC converter input current will again be more impulsive, and the associated effects of this dI/dt over any parasitic inductance are highly undesirable.

2.4 Converter Design and Optimization

Chip area is a costly resource, for this reason it is not only the power conversion efficiency that is considered when designing an integrated converter, but also power conversion density is to be maximized. On a system level, the area allocated to each circuit block must minimize the power flow losses from input to output in the converter. Therefore it is necessary to also include the additional effects of block interconnections, that are typically not part of the converter modeling. As these resistive losses become more important, due to the high current density of power-dense converters, it is no longer possible to consider these effects as negligible.

In [90] the contribution of the flying capacitor C_{fly} and the switch on-resistances to the output impedance of the converter is modeled. In a Slow Switching Limit (SSL) case, the flying capacitor impedance is dominant [Eq. (2.20)]. The other limit is the Fast Switching Limit (FSL) case, in which the combined on-resistance of the switches dominates the flying capacitor (dis)charge time constant. The FSL resistance is given by Eq. (2.21).

$$R_{ssl} = \sum_i \frac{(a_{c,i})^2}{C_i f_{sw}} \tag{2.20}$$

$$R_{fsl} = 2 \sum_i R_i (a_{r,i})^2 \tag{2.21}$$

$$R_o = \sqrt{R_{fsl}^2 + R_{ssl}^2} \tag{2.22}$$

Parameters $a_{c,i}$ and $a_{r,i}$ are topology-specific. The output impedance is then given by Eq. (2.22). However this model does not yet include the ESR of the flying capacitor $R_{ESR,C_{fly}}$ and metal routing resistance R_{route} as shown in Fig. 2.11. Both these parasitics contribute to R_o and result in Eq. (2.23).

$$R_o = \sqrt{(R_{fsl} + R_{ESR,C_{fly}} + R_{route})^2 + R_{ssl}^2} \tag{2.23}$$

From Eq. (2.20) it can be seen that the R_{ssl} can be made small by using more capacitance C_{fly}, or by increasing the switching frequency f_{sw}. Integrating a large capacitance in CMOS consumes a large area, and thus will be the bottleneck for power density as the switching frequency cannot be chosen arbitrarily high, without compromising system efficiency. For this reason MOS-capacitors are selected to integrate C_{fly}, due to their high capacitance density of around 10 $\frac{\text{nF}}{\text{mm}^2}$ in comparison to the MIM capacitor or MOM capacitor alternative. Achieving high power density requires optimal use of the available C_{fly}, i.e., design $R_{ESR,C_{fly}}$, R_{route}, and R_{fsl} to be low in comparison with R_{ssl}, while limiting the associated impact on the area.

Additionally, the flying capacitor bottom-plate parasitic coupling can be captured by a modeling resistor in Fig. 2.11, but is not added here. In case of applying Intrinsic Charge Recycling, the coupling can be modeled by a resistor from input to output. Alternatively, the coupling causes an additional resistor in parallel to the load, in the regular scenario.

Next to the output impedance loss, Fig. 2.11 shows the dynamic losses (R_{dyn}) as result of the switched-mode operation. Resistor R_{dyn} is not a physical impedance at the location in Fig. 2.11, but intends to model the loss associated with the power switches, their drivers and level shifters. It is represented by $P_{dyn,switches}$.

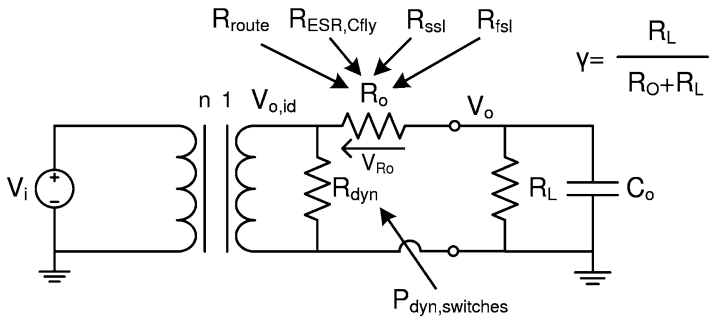

Fig. 2.11 Output impedance model for switched-capacitor DC–DC converter, extended with additional loss contributions

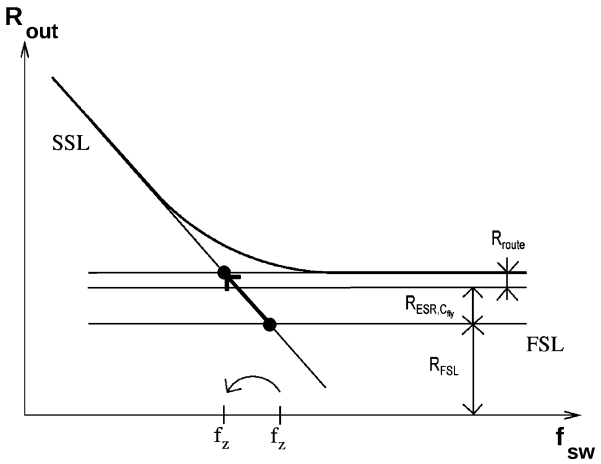

Fig. 2.12 Crossover frequency shift due to additional parasitics and the influence of R_{fsl} on total losses

Optimizing power density results in the minimizing Eq. (2.23), while targeting a desired threshold-efficiency as secondary objective. Figure 2.12 depicts the crossover frequency shift of R_o due to Eq. (2.23). Both $R_{ESR,C_{fly}}$ and R_{route} only have an area impact, but no cost in the dynamic power. Consequently, good design involves to make these values much smaller than R_{fsl} [9, 115], which contributes, on top of area, to dynamic losses. Regarding losses, the ideal value of R_{fsl} is obtained when its associated cost $P_{dyn,switches}$ is comparable to the dominant loss caused by R_o. Indeed R_{fsl} (and thus R_o) should be made smaller as long as the cost in additional dynamic power is negligible to the dominant loss. This approach is similar to the output impedance balancing described in [115] and includes the effect of $R_{ESR,C_{fly}}$ and R_{route}.

The above design considerations were combined into the automatic procedure that resulted in the proposed converter, of which the specifications are later discussed in Sect. 2.6. Given a fixed area for the flying capacitor C_{fly}, as this is the main area bottleneck, an optimal solution is searched for in the design space formed by parameters $R_{ESR,C_{fly}}$, R_{route}, R_{fsl}, f_{sw}, and γ.

2.5 Implementation

The system architecture is shown in Fig. 2.13. The converter is built up with power conversion cells, discussed in Sect. 2.2. These cells contain 2 voltage domains, each with a voltage range of V_{dd}. Voltage domain 1 ranges from V_{dd} to $2V_{dd}$ and contains transistors $M1$ and $M3$. Voltages between ground and V_{dd} form voltage domain 2 and this domain includes transistors $M2$ and $M4$. The advantage of stacking 2 voltage domains is that the standard thin-oxide transistors (V_{dd} rated) can be used, instead of the less-performing thick-oxide I/O devices ($> V_{dd}$ rated). This is because each transistor only operates within one voltage domain, and

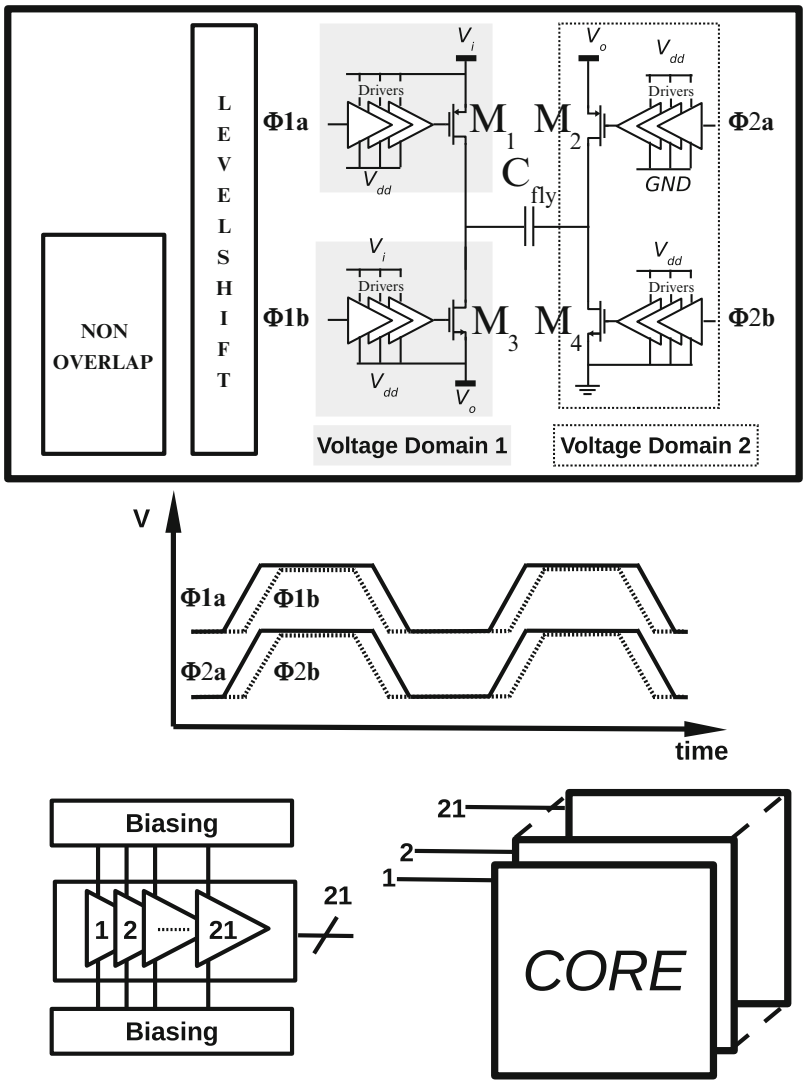

Fig. 2.13 System architecture: 21-interleaving structure composed of unity converter cells, controlled with 21-tap VCO

undergoes a maximum voltage swing of V_{dd}. Thin-oxide transistors have a better $Q_g R_{ds,on}$, hence they are preferred over the thick-oxide transistors if the topology is compatible with voltage domains. Generally, capacitive converters can exploit this very well, as demonstrated by Ng et al. [70] in a 12–1.5 V converter with extensive implementation of multiple voltage domains. Using many voltage domains also has consequences, level shifters are needed to pass clock signals in between voltage

domains and during start up special care must be taken to protect the transistors from overvoltage. In this design, an integrated linear regulator, implemented with thick-oxide devices, was included to generate an internal supply voltage of V_{dd} to ensure safe start up.

Proper operation of the power conversion cell requires the 2 phases to be non-overlapping, as shown in Fig. 2.13. A clock signal from the ring oscillator is made non-overlapping into Φ_{2a} and Φ_{2b}. Because of the voltage domain approach, these non-overlapping signals also need to be present in the V_{dd}-$2V_{dd}$ domain. To this end, a capacitively coupled level shifter is used [95]. Each core includes two level shifters to generate the level-shifted counterparts of Φ_{2a} and Φ_{2b}, Φ_{1a} and Φ_{1b}, respectively.

To decrease the ripple on the output voltage the converter is fragmented into 21 equal parts, which are operated out of phase, interleaved in time. This degree of interleaving was selected in order to obtain a specification of the ripple of the output voltage that is below 10 % of V_o. In general, interleaving has a double advantageous effect. First of all, the charge transfer is spread out over 21 smaller charge and discharge currents, yielding a decreased output voltage ripple [101, 113]. This relaxes the requirements of the output smoothing capacitor, as well as that of the input smoothing capacitor. Another advantage is that the idle converter cores help smooth the input and output. When 1 of the 21 converter cores switches between phases, 10 other converter cores are located between V_i and V_o (Φ_a) and another 10 converter cores are located between V_o and ground (Φ_b). Hereby the charge-transfer capacitors C_{fly} in the idle cores are effectively decoupling the output, with the difference that at a later time they will also contribute to the charge-transfer process. When the amount of interleaving is high, the idle cores are sufficient to smooth a switching converter core. Then it is no longer needed to have a dedicated output smoothing capacitor. Precious chip area is saved and the power conversion density is boosted. In this prototype converter, a total of 12 nF is divided over the 21 converter cores resulting in a C_{fly} of 0.57 nF per core. No dedicated output capacitor was integrated and the output voltage ripple did not exceed 8 % of the output voltage in steady state. Each converter core is provided with an out-of-phase clock signal, generated by a 21-stage voltage-controlled ring oscillator (VCO), of which the frequency is set by an external control voltage. For the interleaving approach to work well, the switching action of each core should be spread out in time with equal intervals. Small levels of phase noise in the VCO however are not a problem because the flying capacitor C_{fly} is charged/discharged with exponential decaying current pulses and thereby the interleaving sensitivity to phase noise in the VCO is low.

Capacitive converters, as opposed to their inductive counterparts, implement a fixed voltage conversion ratio (VCR) that is set by the topology of the converter. The topology of Fig. 2.1 achieves an ideal (unloaded) VCR of 0.5, but under practical conditions the VCR is lower due a non-zero output impedance [90]. The voltage drop V_{R_o} (set by γ), introduced by this output impedance, forms an upper bound for the maximum achievable efficiency. Therefore, V_{R_o} is desired to be as low as possible. From a regulation perspective this output impedance can also be used to generate intentional voltage drops as to generate voltages below the ideal output

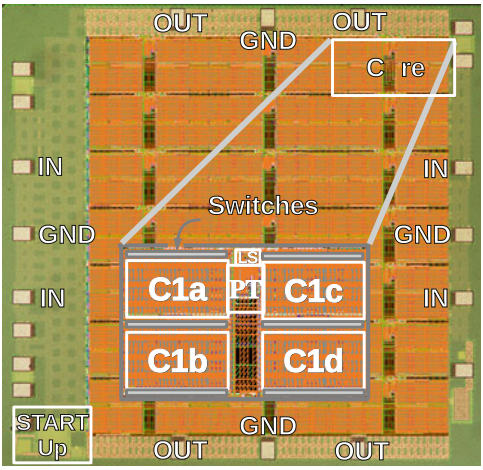

Fig. 2.14 Chip photograph

voltage of the converter topology. This is similar to adding a linear regulator in series with the ideal converter output, where a voltage drop is generated over a series pass device. Control of the output impedance of the capacitive converter can be obtained by changing the switching frequency. The efficiency of generating voltages below the ideal output voltage is thus like that of a linear regulator. However for small deviations below the ideal output voltage, this kind of regulation has only a limited efficiency impact. On top of that, the overall decrease in efficiency is being counteracted by a decrease in switching losses, associated with an output impedance increase. For a wider range of output voltage regulation, while maintaining high efficiency, it is necessary for the converter to reconfigure in a different topology with a different corresponding VCR [27, 87, 105].

The total circuit of the proposed converter prototype was implemented in a 90 nm bulk CMOS technology and measures 2.14 mm^2. The total amount of integrated flying capacitance is 12 nF. A chip micrograph is depicted in Fig. 2.14.

2.6 Experimental Verification

Figure 2.15 shows the efficiency of the converter when a constant output voltage of 1 V is delivered to a load. This measurement was conducted by sweeping the load current, while the external control voltage was adjusted to set the switching frequency in order to generate 1 V at the output. The load is varied from 250 mW up to 1050 mW and both the converter prototype efficiency as well as the efficiency of a corresponding linear regulator is shown. A peak efficiency of 65 % at a 1 W load is achieved. From Fig. 2.15, it is clear that the capacitive converter substantially improves upon the linear regulator. The Efficiency Enhancement Factor (EEF)

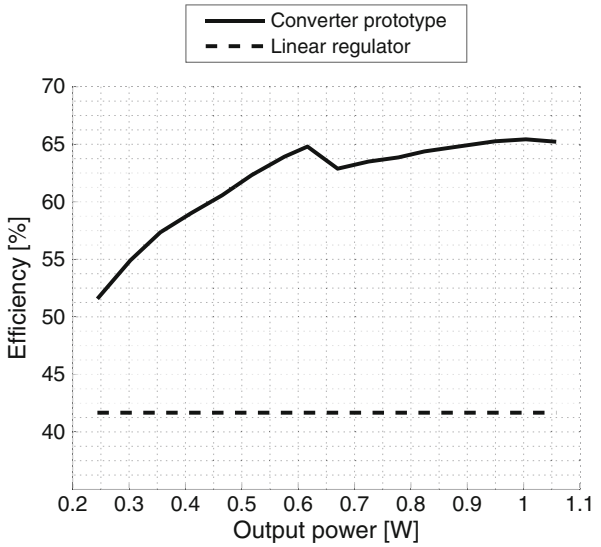

Fig. 2.15 Efficiency during a sweep of the load power P_o, at constant $V_o = 1\,\text{V}$ and $V_i = 2.4\,\text{V}$

introduced in [125] under a 1 W load is +36 %, meaning that this prototype converter can extend the battery lifetime with the same amount.

A measurement to indicate the maximum efficiency, for an output power range of 150 mW up to 1.65 W, is performed in Fig. 2.16. For each converter load power point, the converter efficiency and the corresponding output voltage are plotted. This was measured for both an input voltage of 2.4 and 2.6 V. When the converter is supplied with an input voltage of 2.4 V, the converter efficiency peaks at 69 %, while supplying 0.9 W to the output. In case 2.6 V is present at the input, the converter prototype is able to deliver a maximum output power of 1.65 W, and this at a power conversion efficiency of 60 %. Both input voltage cases lead to a performance of over 60 % in a broad load power range.

As mentioned earlier, capacitive converter topologies implement a fixed VCR, but regulating the output impedance is suitable for generating output voltages, if only a small deviation below the ideal output voltage is required. The external control voltage is used to set the frequency and hereby the output impedance can be controlled by Pulse-Frequency Modulation. Alternatively, Fig. 2.17 shows the efficiency under an input voltage decline from 2.6 V down to 2.35 V and a constant output voltage of 1.03 V, while the load current is 775 mA. Both converter efficiency as well as the efficiency of a linear regulator are plotted and the switching converter steadily maintains an efficiency of around 65 %.

The load regulation of the converter is measured in Fig. 2.18. Since the converter does not have an integrated closed control loop, the measurement represents an open-loop converter, configured to a single switching frequency. The load current is stepped between 641 and 1170 mA, represented by the lower (CH1) waveform.

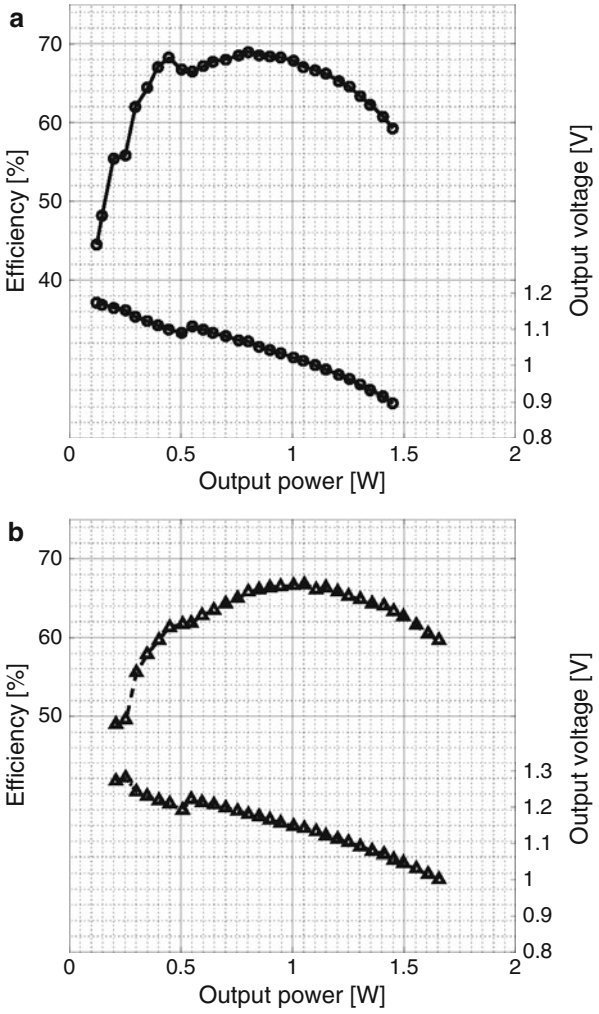

Fig. 2.16 Efficiency and corresponding V_o (open loop) during load power P_o sweep, with (**a**) $V_i = 2.4\,\mathrm{V}$ and (**b**) $V_i = 2.6\,\mathrm{V}$

The upper waveform (CH2) shows the reaction of the converter to this load variation. The applied load step causes an output voltage difference of 95 mV, which results in a load regulation of $-0.175\,\Omega$. The efficiency in both load current cases was 65 %.

A comparison to prior art is summarized in Table 2.1 and Fig. 2.19. All converters in the comparison exhibit high power density, but each has a different technology or topology background. It is shown that this work improves upon [125] and achieves a high output power on top of a power density comparable to [42], although no special technology options were used in this work and no high capacitance density feature was available, as is typical in advanced nanometer technology nodes [110].

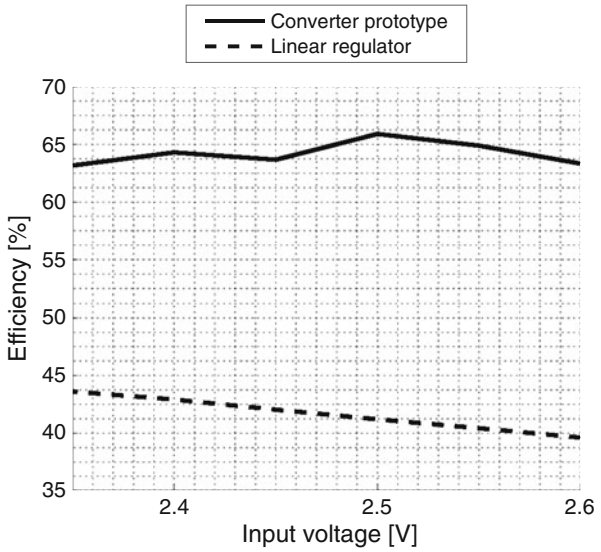

Fig. 2.17 Efficiency under an input voltage variation, but fixed $V_o = 1.03$ V and fixed load current $I_o = 775$ mA

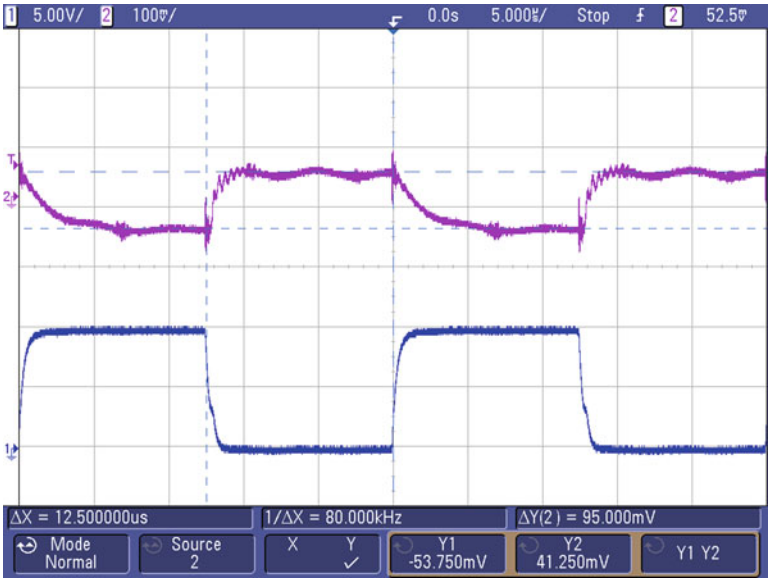

Fig. 2.18 Load regulation measurement. $\Delta i_L = 529\,\text{mA} \rightarrow \Delta V_o = -95\,\text{mV}$: load regulation $= -0.175\,\Omega$

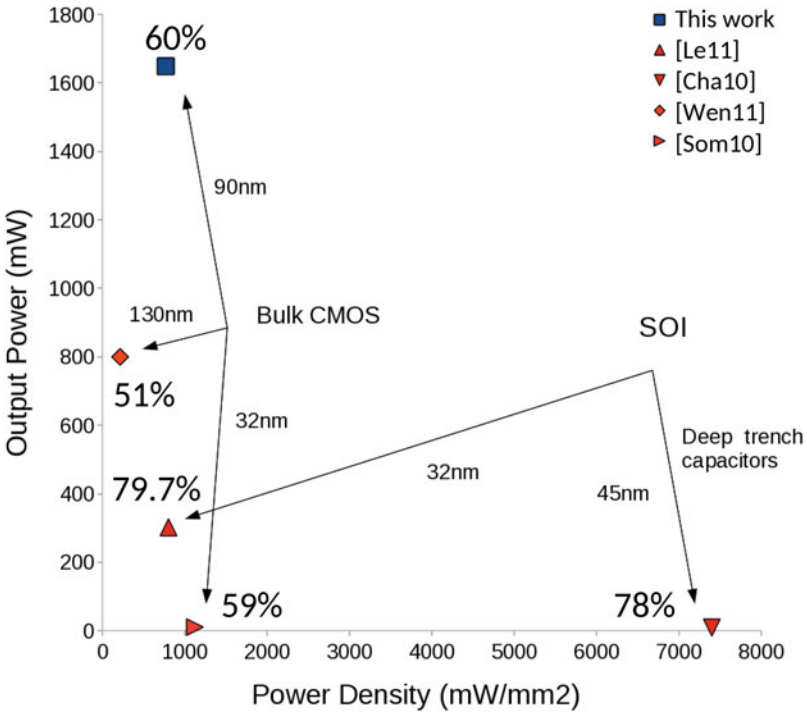

Fig. 2.19 Power versus power density of state of the art, anno 2011, at the indicated efficiency

The work in [13] achieves a very high power density, but the integrated prototype only delivers a peak output power of 8.88 mW. The high power density can be realized through the availability of a very large amount of integrated capacitance, enabled by deep-trench capacitors. While the design in [13] only realizes a low output power, issues such as heat dissipation and metal routing impedance are not expected to be very pronounced. As such, extrapolation of the power density to higher power implementations is optimistic. Nonetheless, very high power densities can be achieved by this technology.

2.7 Conclusion

The converter in this work was designed to have a maximal power density, with efficiency as secondary objective. To this end, Sect. 2.4 provides insight on the parameters and parasitic effects that affect the optimal design point. Section 2.3 introduces circuit and layout techniques to overcome the pitfalls that accompany the integration of capacitive DC–DC converters in a cheap bulk CMOS technology. The proposed Flying-Well technique and the Intrinsic-Charge-Recycling technique

Table 2.1 Specification comparison to prior art

Reference	[42]	[13]	[125]	[115]	This work
Tech node (nm)	32	45	130	90	90
Type	Capacitive	Capacitive	Inductive	Capacitive	Capacitive
Control	Open-loop PFM	Ext. frequency	SCOOT control	Hysteretic closed loop	Open-loop PFM
Power/area (max.)	0.86 $\frac{\text{W}}{\text{mm}^2}$	7.4 $\frac{\text{W}}{\text{mm}^2}$	0.213 $\frac{\text{W}}{\text{mm}^2}$	0.05 $\frac{\text{W}}{\text{mm}^2}$	0.77 $\frac{\text{W}}{\text{mm}^2}$
$P_{out,max}$	325 mW	8.88 mW	0.8 W	0.15 W	1.65 W
$\eta_{max}(\%)$	85	90	58	77	69
V_o ripple spec	Not available	Not available	$< 10\,\%V_\text{o}$	$< 5\,\%V_\text{o}$	$< 8\,\%V_\text{o}$
Tech option	SOI	SOI, deep trench	Bulk CMOS	Bulk CMOS	Bulk CMOS
		200 $\frac{\text{nF}}{\text{mm}^2}$			
# interleaving	32	1	4	10	21

offer a performance increase, along with other incorporated techniques as the use of multiple voltage domains and interleaving. This resulted in a 2.14 mm^2, 90 nm CMOS capacitive 2:1 step-down demonstrator, capable of delivering an output power of 1.65 W or 0.77 $\frac{W}{mm^2}$. Achieving these specifications, the converter prototype does not escape high temperature operation and metal routing impedance issues, that very-high-power-density converters only delivering a low output power are not impeded by. Over a broad load range, the efficiency of the proposed converter is above 60 %, which is on average a 20 % efficiency increase in comparison to a corresponding linear regulator. It is shown that bulk CMOS can be a potential vehicle for high-power, high-power-density converters at moderate efficiency. That is the performance penalty when circumventing special technology options and keeping cost down.

Chapter 3
Toward Monolithic Integration of Mains Interfaces

3.1 Introduction

This chapter is the first in a set of four chapters, to discuss and report on the main focus of this work: the investigation and realization of miniaturized transformerless power converters to interface the mains voltage, and deliver an output voltage that is compatible with the supply voltage of modern low-voltage CMOS technologies. Therefore the functionality resembles that of the traditional AC–DC converter, which has become a ubiquitous component in the household to the extent that most users no longer take notice of what a central place this common component takes up in daily life. Especially with the growing popularity of connected mobile devices and the smartphone in particular, which has an exceptional hard time to last through the day on a single battery charge, the little AC–DC adapter can be regarded as a gadget enthusiast's best friend. The integration focus of mains interfaces in this work is not to replace the current AC–DC adapters, but to extend upon the available mains converters by adding efficient and compact mains conversion at power levels below the current spectrum.

3.2 Motivation

Research toward highly integrated mains AC to low-voltage DC conversion can easily be justified. On the source side, the mains AC voltage is the predominant power distribution method toward the end user, and this on a global scale [127]. This is a logical consequence of using AC machines to generate electricity. In the early days of electrification, there was initially a proliferation toward many local frequency standards. The multitude of used frequencies caused no single standard to prevail until large companies weighed in to back a single frequency.

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In Germany, and later Europe, Allgemeine Elektricitäts-Gesellschaft (AEG) decided in 1891 to use 50 Hz, while Westinghouse in the USA adopted 60 Hz in 1890 [72]. On the electricity consumption side, voltage is required in a different form. Applications, which contain modern semiconductor integrated circuits, typically require a DC voltage to operate. The actual voltage level varies depending on the specific application, but generally more recent integrated circuits require ever lower DC supply voltages. This leads to the voltage gap, a large discrepancy in voltage specification between source and sink. Moreover, this discrepancy presents itself very often, which is proven by the multitude of AC–DC adapters, wall warts, or power bricks in a typical household.

Figure 3.1 shows the trend of volume reduction from bulky blocks to a more compact form factor. This is made possible by moving from the bulky transformer-based AC–DC adapters to switched-mode power supplies and in a later stage by transitioning to a high-frequency switched-mode power supply approach, allowing to reduce the size of passive components. Moreover, weight is also reduced due to the transition of heavy ferrite-core low-frequency transformers into their lighter high-frequency equivalents. Even though there is a positive evolution in AC–DC adapters, applications are available that do not match with the specification scope of typical adapters and are better served by other mains conversion approaches with better matching specifications. A popular output power specification for adapters is 5 V at 1 or 2 A, resulting in 5 or 10 W at the output, respectively. Below 10 % of this

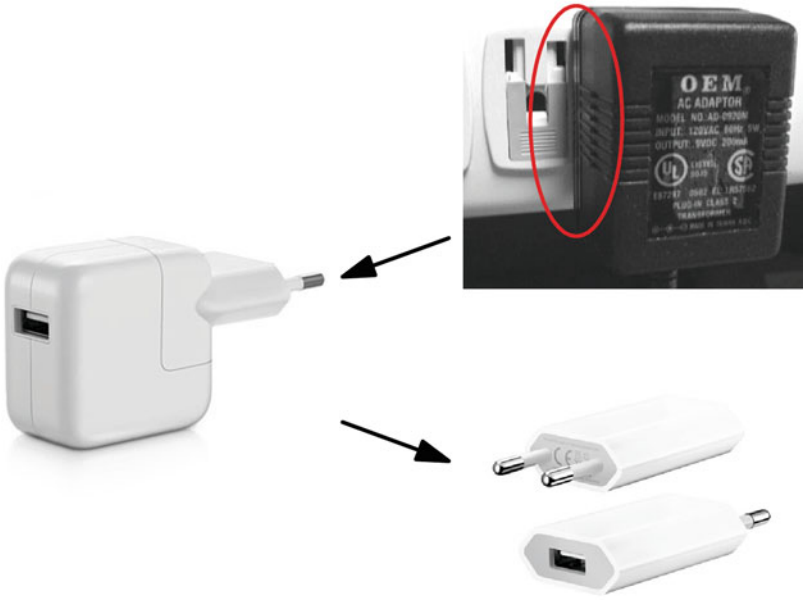

Fig. 3.1 Evolution of AC–DC adapters: from bulky transformer-based through the traditional switched-mode power supply to the recent high-frequency compact switched-mode power supply

nominal output power rating, high conversion efficiency can no longer be assumed and is also not a legal requirement, although efficiency standards are gradually becoming more strict [19]. Consequently, applications with a power consumption below this level are better supplied by other means of mains AC–DC conversion.

This motivates the search for μW-level and mW-level solutions to bridge the voltage gap between source and sink, targeting low-power applications. In the μW-range, possible application can be found in smart sensor networks, of which the terminology has evolved into the more popular and widely accepted Internet-of-Things (IoT) or Internet-of-Everything (IoE) denomination. Alternatively, efficient delivery of mW-level output power can revolutionize standby power consumption of consumer electronic appliances by adding an auxiliary power supply. In addition, mW-level power supply from the mains can also serve as a main stand-alone solution for future low-power target applications.

3.2.1 μW Level

A trend toward smart environments, as proposed by the Internet-of-Everything, is posing substantial demands on sensor nodes to become available for in-building light and climate control. To power these functions, one can aspire to use any method of energy scavenging, but the limitations in power and cost for the scavenging solutions are manifold. Alternatively, it might not be possible to rely on a battery for energy storage due to the large volume that would result or the infeasibility to recharge. Another option is to power sensor nodes from the mains, particularly relevant for applications that already have access to the mains voltage such as lighting control. Typical solutions for low-power low-voltage supplies are based on flyback topologies [81] and the cost and size are determined by the external components, such as a mains isolating transformer. For target application in this work, it is required to realize a differentiation in cost and volume. Consequently, a high level of integration is required in the solution.

3.2.2 mW Level

Many of the consumer electronics appliances in the household are permanently connected to the mains. Among these appliances, devices belonging to the category of remote-controlled devices are mostly never fully switched off by the power button, but in fact go into a form of hibernation or sleep mode. This means that, even when not actively used, the device continues to draw power from its internal mains-connected power supply. Despite the obvious lower power level required by the device in sleep, total system power consumption may be worse than initially expected as result of the inefficiency of the internal mains-connected power supply now being used at 1/10th to 1/100th of its nominal output power level. This confirms

the need to develop a high-efficiency mW-power inexpensive alternative with a small footprint to be added to the remote-controlled device to enable negligible system power consumption when operating in sleep mode. In addition, a mW-level power supply from the mains can also serve as a main stand-alone solution for future low-power target applications.

3.3 Target Functionality and Specification

After introducing and motivating the proposed research in Sects. 3.1 and 3.2, this section takes the next step in the development toward a concrete solution by translating the wanted properties into specifications. To that end, it is necessary to identify key functionality and quantify this into the system specifications that define the boundaries of the solution space. On top of that, this exploration targets an application-specific, in the sense that the output power of the converters under aim is in a suitable matching range, custom prototype to advance on previous work in terms of integration, performance, and cost.

From a high-level perspective, the target functionality is the ability to interface to the mains voltage and to efficiently deliver a regulated low-voltage power supply with sufficient output power capability to operate the applications described in Sect. 3.2. An important aspect while achieving this functionality is to eliminate the need for a transformer, in order to overcome the cost and volume bottlenecks of readily available solutions while advancing the state of the art.

The input specification of the system solution is immediately well defined because of the standardization of the mains [65], even though multiple mains standards exist. The situation with respect to the specifications on the output side is less clear. Typical IC supply voltages include the 0.9–1.2 V range, 1.8, 2.5, 3.3, 5, 12 V, etc. Their origin is found as being the nominal supply voltage ratings of CMOS technology nodes through the evolution of CMOS technology scaling and simultaneous voltage scaling. From these voltages, 3.3 V is a good compromise in between legacy technologies and the present-day high-end nanometer CMOS. It is a very commonly used power rail on printed circuit boards and is consequently a good target output voltage level. With respect to the output power, it can be concluded that only relatively low amounts of power need to be extracted from the mains in order to supply the applications mentioned in Sect. 3.2. Even though the absolute power levels are low, a power range of μW's in smart nodes up to mW's for auxiliary standby units spans three orders of magnitude. Realization of such a wide operation range is not a simple feature to accomplish [118] and typically involves multiple control parameters to vary or multiple operation modes [14], where normally one is enough. Inevitably, when an application is on the low end of this power spectrum, the power converter is operating at a very light loading condition, and is not fully taking advantage of its die area and is operating at a low actual power density in comparison to its nominal capability. Therefore, if target applications are on either end of this power spectrum and only operate at that level,

Table 3.1 Specification targets for low power from the mains

V_{IN}	$[V_{RMS}]$	85–265	
V_{OUT}	$[V_{DC}]$	3.3	
		µW-range	mW-range
$P_{Load,nom}$		$\leqslant 100\,\mu W$	$\leqslant 100\,mW$
$P_{IN,no\ load}$		N.A.	$\leqslant \frac{1}{10} P_{Load,nom}$

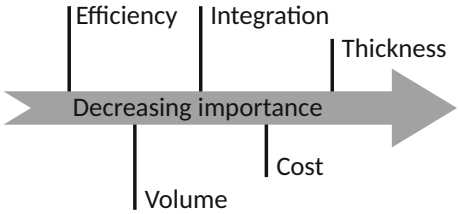

Fig. 3.2 Performance feature order of importance

wide range is not required and power-level-specific scaled implementations are more appropriate. Alternatively, this is an indication that optimized approaches for either end of this power spectrum might require fundamentally different underlying operation principles.

Next to input and output voltage specifications in combination with targets for the output power, which are functionality specifications, as they are fundamental in achieving the target functionality, other specifications of importance are system efficiency, cost, and volume. They are performance specifications as their actual value does not affect the ability to perform the target functions, but affects the quality of how these are performed. Therefore, instead of setting target values for these specifications, unless forced by system constraints, it is more sensible to sort them in their order of importance or priority. Especially since performance specifications typically yield trade-off relations between another.

Table 3.1 lists an overview of the functional specification targets and Fig. 3.2 indicates the priority order of the performance specifications.

3.4 Research Challenges

After the definition of target specifications, practical circuit techniques and implementation are necessary in order to realize the demonstrators under aim. At this point, an assessment is made of what the research challenges of this work are with respect to the available current state of the art.

A first challenge to solve when integrating mains interfaces is the handling of high voltages on a chip or within a system where not every individual component can come into direct contact with this voltage. This results in the requirement of the circuit to arrange the components such that individual components are always operated within their nominal boundaries but that the whole of components is

handling a higher than nominal voltage. The voltage range of active circuits in CMOS is generally limited due to the small feature size they are produced in and the according breakdown voltages of the process materials. Technological solutions, in the form of non-standard CMOS processes, are available with more relaxed breakdown specifications. However, even in this case the issue is not mitigated and special consideration is necessary to realize overvoltage-free and thus reliable circuit operation. Passive components on the other hand can be created with more freedom in layout and can therefore be designed accordingly so that the necessary voltage range is directly incorporated.

A second challenge is to conceive circuit topologies to perform rectification, high-ratio voltage conversion, and regulation. It is not required that the preceding steps are performed in the listed order. Both a single-stage or multi-stage system circuit approach is considered, as long as the functional and performance specifications can be met. With respect to the state-of-the-art solutions, a transformerless solution is targeted to substantially differentiate this work from available commercial off-the-shelf (COTS) components in volume and cost.

A third challenge, as with all integrated power converters, is the limited density at which capacitance and inductance can be integrated onto a chip. Hereby restricting achievable values to the first decade of the nF or nH range. In voltage conversion circuits, passives can easily become large in a trade-off to reduced switching frequency in order to achieve a high efficiency specification. At the same time, the power conversion density is a critical performance parameter and maximizing this yields the dual trade-off to reduce the passive component area and increase the switching frequency. The resulting conflict between power density and efficiency is ever present in monolithic power converters. When focusing only on the specifications of the converter itself, this trade-off yields a very subjective decision. Therefore, it is up to the designer to take into account the total system and to realize optimization from this top-level point of view. It is exactly, and only, this total perspective and its constraints that can objectively motivate specifications of each system building block, and as such, the trade-off between efficiency and power density in the case of a voltage converter.

A fourth challenge is the control of the voltage conversion in order to obtain a regulated output voltage. Despite load fluctuations in the drawn output current and line deviations of the input voltage, the target output must remain within specification. On top of that, there is a growing need for very fast transient response times to react on sudden input/output events. This follows from the evolution that if power conversion is applied more decentralized, with many individual supply nets and close to its individual load, a large shared buffer capacitance that provides inertia to the power net is no longer feasible. The decoupling per voltage net is reduced, while at the same time the dynamic range of the load current is increased. Consequently, faster transient events occur, which require a faster transient control response. In this regard, integration of the power converter is also an enabler to achieve fast control as the feedback loop can be implemented with fast CMOS circuits and the parasitics of the power delivery network [3] are low as result of short physical dimensions of the converter-load combination.

3.5 Bridging the Voltage Gap

3.5.1 Single-Stage Approach

The mains AC as input to a converter presents challenging peak input voltage specifications up to 169 and 325 V in case of the US and EU mains, respectively. The higher the intended level of CMOS integration, the more limited the options to interface such a high voltage become. This is a consequence of the limitation in voltage ratings of native CMOS integrated components, and the restriction to only use such components that yield fewer possible circuit implementations.

1. Active devices: Standard nm processes typically offer switch voltage ratings of 2.5 V/3.3 V, which are already special-purpose input–output devices with higher ratings than the regular transistors standard in nm CMOS. Techniques such as stacking devices in series [8, 94] can be used to construct switch blocks with enhanced voltage ratings, but are still limited by the finite body-to-substrate diode reverse-breakdown voltage. When larger switch blocking voltages are unavoidable, a possibility is to use a process with the option to implement laterally diffused MOS (LDMOS) devices. This enables active devices interfacing up to many tens of volts.
2. Passive components: Passive components can on the one hand be implemented with active devices in the case of a MOS-capacitor or with special process option components such as metal-insulator-metal (MIM) capacitors on the other hand. Unlike these passive components that are limited in voltage rating by the building blocks they are composed of, passive components implemented in the metal stack benefit from the freedom in layout to obtain custom-designed voltage ratings. However, larger voltage ratings require larger spatial separation of the component terminals and thus result in a lower density of the integrated passive.

Even though the implementation options for a monolithic single-stage approach are reduced, this approach will be further investigated in Chap. 4.

3.5.2 Two-Stage Approach

Next to full integration in a single stage, partitioning the mains AC–DC conversion over two cascaded stages allows increased design flexibility in each stage and enables each stage to focus more efficiently on a subset of the system challenges. This approach motivates to use external components to step-down the high-voltage mains in a coarse manner to an intermediate voltage compatible with CMOS integrated active devices, which can then implement a secondary conversion and provide fine regulation of the output. This will be later explored in Chap. 5.

3.6 Conclusions

The realization of an integrated power converter to interface the mains and deliver a low DC voltage in a compact form factor poses many challenges. As discussed in this chapter, a most prominent aspect is to enable high-voltage capability with a combination of lower-voltage building blocks. Opportunities to address the challenge consist of flexible output power specifications that target the μW levels and mW level, but are otherwise loosely defined. Alternatively, within the scope of achieving a compact and highly integrated solution that differentiates itself with a 10x improvement with regard to current available solutions, total freedom to conceive a system is available.

From the discussions in this chapter, two implementation perspectives emerge that will now be explored in detail in the upcoming chapters. On the one hand a full monolithic approach focusing on the lowest power, but in a very small form factor, is presented in Chap. 4. On the other hand, an approach with a high level of integration, using only a limited set of low-volume external components, offers more flexibility to address both higher power as well as efficiency at the cost of an increased implementation volume. The system trade-offs and an implementation are discussed in Chaps. 5 and 6, respectively.

Chapter 4
A Single-Stage Monolithic Mains Interface in 0.35 µm CMOS

4.1 Introduction

In everyday integrated circuits a DC supply voltage is assumed to be available to power the IC. But where does it come from? Commonly used power sources have their origin in either harvested power or the mains grid, as the also often-used batteries in mobile applications are of course just energy carriers and need to be recharged.

For the first option, it is possible to harvest energy from various sources that are present in the surroundings. RF radiation [59], kinetic [25], thermal [47], or photovoltaic [107] energy can be harnessed using the appropriate harvester into an electrical output. This output can then be further converted and regulated by integrated power management circuits. However, the power output of a harvester is related to the power available in its environment and therefore is subject to uncertainty. Consequently, system down times may occur, which can last for extended periods of time.

Alternatively, the mains grid proves to be a very reliable source of power with blackouts occurring, on average, less than once a year [15]. It is also widely available through an extensive infrastructure already in place. Unfortunately for integrated circuits, the mains grid distributes power in the form of a high-voltage low-frequency sine wave, specified in regional standards [127]. This generally requires converters employing costly high-voltage discrete components, such as a rectifier and a transformer [2], taking up significant PCB area.

In this chapter an integrated mains interface is proposed according to the single-stage solution perspective discussed in Chap. 3, with the goal of fully integrating it on chip. This eliminates the need for high-voltage-rated external components, drastically reducing the footprint. However, the complexity is now shifted toward the integrated circuit, creating the challenge to interface with these high voltages. The approach encompasses the monolithic integration of a capacitive step-down

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interface that separates the active circuit from the high-voltage input, enabling integrated circuits to operate straight from the mains as supply voltage. This feature opens up the mains as possible power source for new application domains, where the otherwise necessary discrete converter makes the solution unfeasible or too expensive. Possible example applications are physically small low-power systems that cannot consider the mains as power source if it requires a bulky converter and consequently are limited to battery power and/or energy scavenging operation. The mains as power source implies, in return, that the system is stationary, for example, to be used for in-building sensor applications and other applications listed in Sect. 3.2.

Previous research in this area concentrated on the feasibility of a high-voltage-input integrated power supply by using the high-voltage capability of a silicon-on-sapphire (SOS) technology [73], to implement circuits capable of interfacing the mains input. To circumvent the need for high-voltage active circuits, a capacitive division of the input voltage has been presented by Tamez et al. [106] to reduce the required voltage rating of the subsequent power management circuits. However, this capacitive division of the AC input voltage considerably lowers the total system power throughput due to limited rectifier diode on times, because the voltage division occurs before rectification, reducing the duration when the sinusoidal rectifier input is larger than its output. This work aims to combine the efficiency benefit of a capacitive step-down approach with the feature of a maximal power throughput by maximizing the rectifier diode on times. To that end, the operation of a capacitive AC–DC step-down stage is examined, offering the advantage of a decreased voltage rating for the subsequent active circuits, but with a maximal power throughput by eliminating the capacitive division before the rectification. The resulting demonstrator was measured for line input voltages from 85 V_{RMS} up to 265 V_{RMS} for both 50 and 60 Hz and was able to supply a load current of 1.93 µA and 2.87 µA at 3.3 V for the US and EU mains standards, respectively.

This chapter is organized as follows. Section 4.2 discusses the challenges of handling the mains as input voltage in an integrated circuit. The system architecture and operation are proposed in Sect. 4.3. Section 4.4 presents a compact model for an ideal capacitive AC–DC step-down converter, followed by the prototype implementation details in Sect. 4.5. Measurements results are reported in Sect. 4.6 and final conclusions are drawn in Sect. 4.7.

4.2 High-Input-Voltage Architectures

Interfacing voltages beyond the nominal rated device voltage generally requires special circuit techniques to prevent device overvoltage from occurring and consequential device destruction. Successful techniques to do so include device stacking, on the one hand, where cascoded devices each share a portion of the total voltage [8, 93], and voltage domain stacking on the other hand, in which multiple nominal voltage rails are serialized [67]. The cascoding approach is useful up to

a few times the nominal rated supply voltage as the complexity to implement these techniques increases substantially for each added level of stacking devices. Nevertheless, voltage levels up to 10 V have been reported using 0.18 µm CMOS processing [96]. The voltage domain stacking approach can be taken a step further, but is fundamentally limited by substrate-to-well diode reverse-breakdown voltage. This voltage depends on the doping concentration, where higher doping level results in a lower breakdown voltage, and lies in the 10–15 V range for modern bulk CMOS processes. Therefore, extensive voltage domain stacking requires a medium or high-voltage CMOS process, either with an additional buried layer or either through a silicon-on-insulator (SOI) approach. Where in the former the substrate-to-well diode is rated for larger voltages, there is no longer a diode in the latter. Instead, the breakdown voltage is now related to the isolation material and its thickness. The ability to stack many voltage domains does require a very regular, repetitive topology structure, such as a ladder converter. In the case of Meyvaert et al. [61], a collection of many switches and capacitors, each handling only $1\,V_{unit}$, are combined into a series-stack of 10 voltage domains. But, this is assuming that the circuit is functioning in its steady-state operation and starting up to this nominal state is not trivial, possibly requiring the temporary support of high-voltage devices that were targeted to be circumvented by the approach.

When considering the mains voltage with a nominal peak voltage of 375 V in the $265\,V_{RMS}$ case, it is clear that these techniques are inadequate and alternative approaches are needed. With the mains voltage input exceeding the rated voltage of the active circuitry by two orders of magnitude, it is required to create a voltage gap between the mains input and the active circuit. This can be achieved by placing a series impedance [73, 106] to contain a high voltage, so that the remaining voltage over the active circuitry is low and within the nominal specification. As discussed in [73], it is possible to use a resistor. Such an approach would have a very low efficiency, due to the very large resistive voltage drop, and is therefore undesirable. On the other hand, the possibility to use a capacitor is also discussed, which in the ideal case is lossless and thus a better choice.

Such a series capacitor approach is taken in the work of Tamez et al. [106] in the form of a capacitive voltage divider, as shown in Fig. 4.1a. The mains input voltage V_{AC} is divided by the combination of capacitors C_{in} and C_{div} to a safe lower value V_X, which can be handled by the rectifier and the rest of the active circuit. The divided voltage V_X is then rectified onto a smoothing capacitor C_{DC}, which supplies current to a load. The maximal operation value for V_{DC} is found to be $\sqrt{2}V_{X,RMS}$, occurring when the load current is absent. Therefore it is required that the capacitive voltage division ratio r_{div} is chosen to fulfill $r_{div}\sqrt{2}V_{AC,RMS} < V_{rated}$ in order to guarantee that no overvoltage will take place at V_{DC} at the worst-case condition when the load current is zero. Consequently, this necessary division ratio r_{div} reduces power throughput in all other lower load conditions as the rectifier diodes are only turned on when $V_X > V_{DC}$, which only occurs for a short time near the peak of V_X. When V_X decreases below V_{DC}, the rectifier diodes turn off until V_X goes below $-V_{DC}$. During this time C_{DC} buffers V_{DC}.

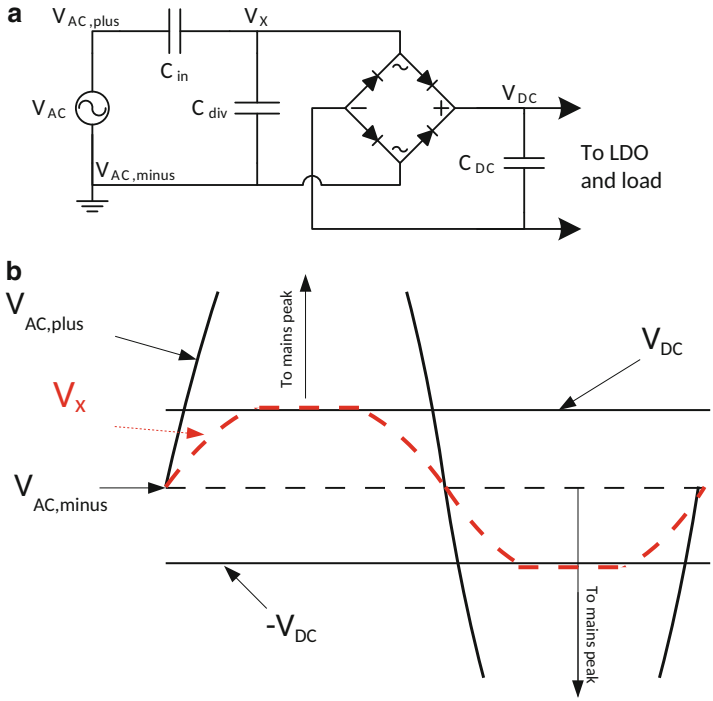

Fig. 4.1 Schematic (**a**) and associated waveforms (**b**) of a typical capacitive voltage divider

This work proposes to use a series capacitor as a capacitive step-down, interacting with the load and the power management regulation circuits located behind the rectifier, showing similarity to [73]. But other than in [73], this work targets the use of a CMOS technology by moving the high voltage toward the integrated passive components. And unlike [106], which guarantees safe operation at the worst-case load by reducing the rectifier input voltage V_X, overvoltage is avoided by providing a proper current sinking capability after rectification by a shunt regulation path. This approach maximizes the rectifier diode on-time as $V_{AC,low}$ floats at the rate of the mains when the rectifier is off, keeping t_{off} to a minimum. Hereby power throughput is nearly ideal and maximizes the input-series capacitance utilization, reducing the necessary capacitor size and cost in comparison to other approaches, such as the capacitive division. Figure 4.2a, b demonstrates the proposed concept.

4.3 Proposed System Architecture and Operation

The converter topology, shown in Fig. 4.3, combines an AC–DC step-down stage and DC post-regulation stage. The first stage consists of 2 high-voltage-rated passive components R_{in}, C_{in} and a full-wave rectifier [24], forming the capacitive step-down.

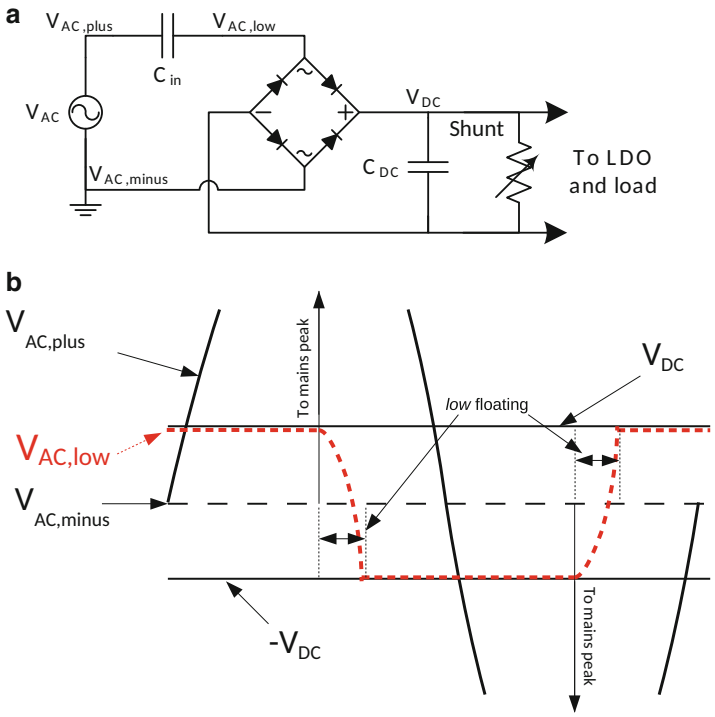

Fig. 4.2 Schematic (**a**) and associated waveforms (**b**) of the proposed capacitive step-down

The output voltage V_{DC} of the AC–DC stage is determined by the combination of the input-series capacitance current and the output load current. The active post-regulation stage is composed of a shunt path and a series regulator. While the series regulator removes any remaining ripple from V_{DC} toward the regulated output voltage V_{reg}, the shunt path via transistor M_{sh} ensures that V_{DC} is limited to a safe voltage value within specification. This is necessary when a reduction of the output current, to lower than nominal values, would otherwise push the equilibrium V_{DC} level up to destructive values.

Next to the fully integrated approach of Fig. 4.3, integrating all components on chip, Fig. 4.4 shows an alternative implementation, which does rely on external components. It is also implemented to avoid the limited availability of monolithic high-voltage passives. Circuits from the fully integrated approach are reused in a scaled-up version, with the exception that the high-voltage input impedance and DC buffer capacitor are now implemented with discrete components, as seen in Fig. 4.4. By exchanging the on-chip components for external components, larger capacitance ratings are feasible to enable the same functionality at a scaled-up throughput level.

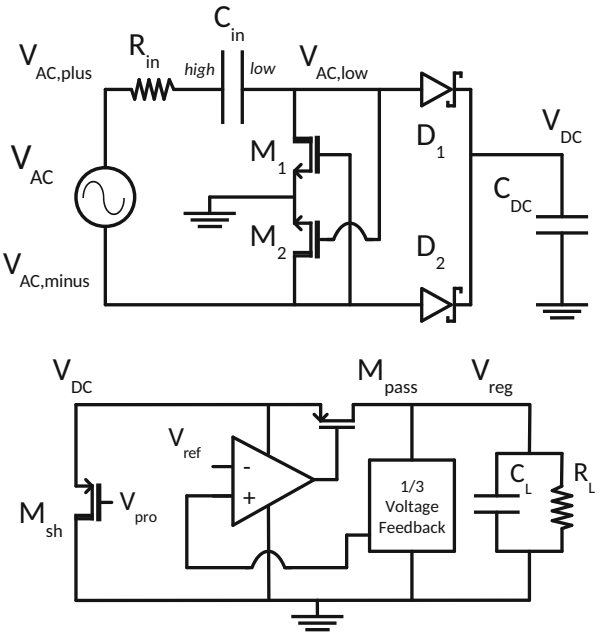

Fig. 4.3 System architecture of the proposed monolithic AC–DC converter

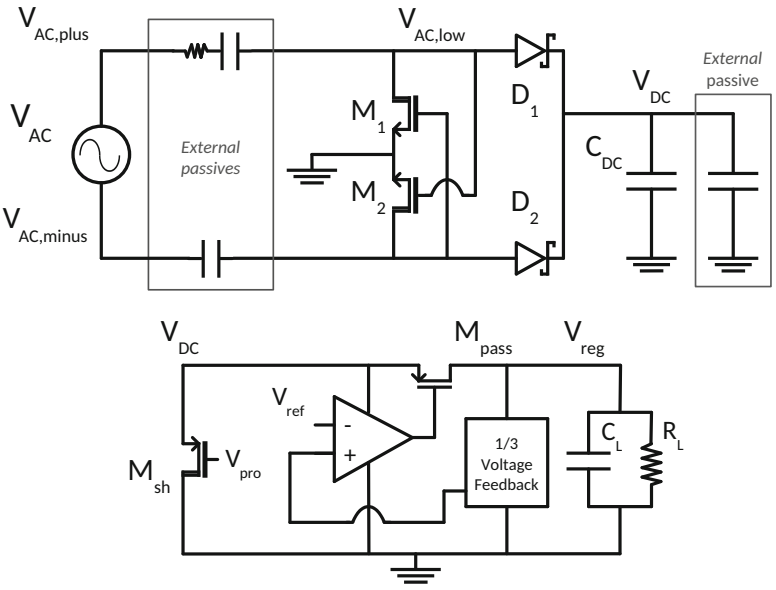

Fig. 4.4 System architecture of the proposed AC–DC converter, employing external components

4.3.1 Capacitive AC–DC Step-Down

To discuss the operation of Fig. 4.3, it is assumed for the sake of simplicity that $R_{in} = 0$, the rectifier is ideal ($V_{th,M1-M2} = 0, V_{D,D1-D2} = 0$), C_{DC} is infinite and charged to a voltage V_{DC}. A mains RMS voltage V_{AC} is considered to be present at the input terminals, as shown in Fig. 4.2b, and the initial condition of $V_{C_{in}} = 0$ is valid. In this case when $V_{AC,plus}$, referred to $V_{AC,minus}$, increases from 0 V up to V_{DC}, devices $M1$, $D1$, and $D2$ remain off while $M2$ is on. Next, for $V_{DC} \leq V_{AC,plus} \leq \sqrt{2}V_{AC}$, $D1$ turns on and current flows to C_{DC}. Immediately after the mains peak is reached, $D1$ turns off followed soon after by $M2$ since the *low* terminal of C_{in} starts to float and decreases at the same rate as $V_{AC,plus}$, until a drop of $2V_{DC}$ has taken place. At that time, $V_{AC,minus} - V_{AC,plus} = V_{DC}$ and $D2$ turns on, while $M1$ has already turned on just before, providing another current flow toward C_{DC}. This continues until the negative peak at which $D2$ turns off. The above operation continues to alternate.

Input-series capacitor C_{in} separates the active circuit from the high-input mains voltage. While the *high* terminal of C_{in} is subjected to the full mains voltage, meaning a peak-to-peak voltage $V_{ptp,high}$ of $2\sqrt{2}V_{AC}$, this is not true for the *low* terminal ($V_{AC,low}$). The *low* terminal is bound by the rectified voltage V_{DC} resulting in a $V_{ptp,low} = 2V_{DC}$. Next to the series-input capacitor C_{in}, which safeguards the active circuitry from high voltages, a series-input resistor is added, to protect the circuit against an inrush current of destructive proportion. When the system is initially connected to the mains at a time of a high voltage or peak while C_{in} is not charged, there is an instantaneous voltage difference of the input capacitor, with an exponential charging current as result. Without resistor R_{in}, a most-likely destructive current rushes in to charge C_{in}, only limited by the parasitic series resistance located between $V_{AC,plus}$ and $V_{AC,minus}$.

4.3.2 Shunt Overvoltage Protection and Series Regulation

Until now it was assumed that C_{DC} was infinite and fixed at V_{DC}, limiting $V_{AC,low}$ with respect to ground during both positive and negative mains half cycle. In practice, this cannot be assumed automatically and must be actively managed. The limitation, in this work, is guaranteed by the parallel combination of the shunt path and a low-dropout (LDO) series regulator passing the current to the load. At nominal load the shunt path is inactive and all power passing the rectifier is consumed by the load, satisfying both $< |i_{C_{in,nom}}| > = i_{load,nom}$ and $V_{DC,nom} = V_{reg}$ (aside from the minimal dropout voltage). The resulting equilibrium of $V_{DC,nom}$ is given by V_{out} of Eq. (4.7), in which $< |i_{C_{in,nom}}| >$ equals the load current $i_{load,nom}$ for that nominal case.

When load power decreases to a lower level $i_{load,low}$, V_{reg} will be kept constant by the series regulator. This is not true for V_{DC}, which will settle at a new equilibrium

$V_{DC,low}$ in order to satisfy $< |i_{C_{in,low}}| > = i_{load,low}$. From Eq. (4.7) it can be seen that, for a given set of fixed parameters V_{in}, C_{in}, and f_{mains}, this can only occur by increasing V_{out} (i.e., V_{DC}). The new $V_{DC,low}$ equilibrium can be calculated according to Eqs. (4.1) and (4.2). In conclusion, this means that for a lower than nominal load current, V_{DC} will easily exceed the safe operation voltage limit. For this reason, a shunt path was included through M_{sh} in parallel with the series regulator, in order to limit V_{DC} to a maximum of $V_{pro} + V_{th,M_{sh}}$. At less than nominal load current, the shunt path will sink current i_{shunt} to compensate for the reduction in i_{load}. Thereby, the load seen by the capacitive AC–DC step-down stage remains constant, and V_{DC} does not reach overvoltage levels.

$$\frac{< |i_{C_{in,low}}| >}{< |i_{C_{in,nom}}| >} = \frac{4 f_{mains}\ C_{in}\ (V_{AC} - V_{DC,low})}{4 f_{mains}\ C_{in}\ (V_{AC} - V_{reg})} \tag{4.1}$$

$$V_{DC,low} = V_{AC} - \frac{< |i_{C_{in,low}}| >}{< |i_{C_{in,nom}}| >} (V_{AC} - V_{reg}) \tag{4.2}$$

4.4 Converter Model

This section analyzes the power throughput of a capacitive step-down stage in the ideal case, which is depicted in Fig. 4.5, and consists of an AC voltage source which is capacitively stepped down and ideally rectified to a DC output voltage. A compact calculation model is presented in Eqs. (4.3)–(4.8).

The capacitive step-down introduces an impedance bottleneck as result of the low mains frequency and a low capacitance value for C_{in}. The latter is caused by the high-voltage nature of capacitor C_{in}, leading to a low capacitance density. Given the ideal representation in Fig. 4.5, it is now investigated what the maximum attainable power throughput is that can be expected for an ideal AC–DC step-down. The power throughput is analyzed for the following set of system parameters: the mains amplitude V_{AC}, the mains frequency f_{mains}, the amount of series input capacitance C_{in}, and the output voltage V_{out}.

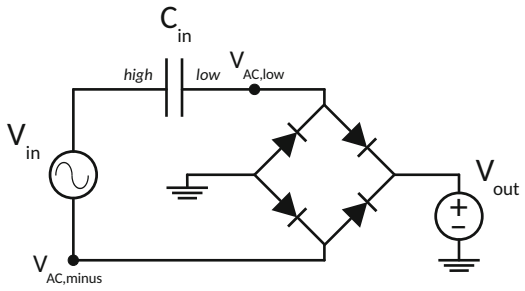

Fig. 4.5 Schematic representation of the ideal model with AC input voltage, a capacitor over which a voltage is dropped, an ideal rectification, and a DC output voltage

$$V_{in}(t) = V_{AC}\ sin(2\pi f_{mains} t) \tag{4.3}$$

$$V_{C_{in}}(t) \approx (V_{AC} - V_{out})\ sin(2\pi f_{mains} t) \tag{4.4}$$

On the one hand, Eq. (4.3) represents the input voltage as function of time present at the high terminal of the capacitor C_{in}. On the other hand, the low terminal of C_{in} exhibits a square-wave pattern with amplitude V_{DC}. As a result of these voltages present at the capacitor terminals, the voltage over C_{in} can be approximated by Eq. (4.4). The capacitor current as function of time is then given by Eqs. (4.5) and (4.6):

$$i_{C_{in}}(t) = C_{in} \frac{dV_{C_{in}}}{dt} \tag{4.5}$$

$$= C_{in}\ (V_{AC} - V_{out})\ cos(2\pi f_{mains} t)\ 2\pi f_{mains} \tag{4.6}$$

Averaging this over time consequently leads to the average capacitor current $< |i_{C_{in}}| >$ in Eq. (4.7), which can be combined with the output voltage V_{out} to calculate the output power P_{out} according to Eq. (4.8).

$$< |i_{C_{in}}| >= 4 f_{mains}\ C_{in}\ (V_{AC} - V_{out}) \tag{4.7}$$

$$P_{out} = < |i_{C_{in}}| > V_{out} \tag{4.8}$$

It can be seen in Fig. 4.2b that the proposed architecture operation constitutes voltages $V_{AC,low}$ and $V_{AC,minus}$ to exhibit block-pulse-like behavior, approaching the ideal case, i.e., an AC square-wave output of the capacitive AC–DC step-down topology that is fed into the rectifier. This is opposed to previous work [106], in which the capacitively divided voltage V_X still looks like a sine wave. A sinusoidal rectifier input results in sub-optimal power throughput due to the fact that power is only transferred when the rectifier diodes turn on ($V_X > V_{rectified}$) which is limited by the slower voltage variation of V_X. Alternatively, for this proposed architecture with its block-pulse-like rectifier input, the rectifier diode on times is significantly longer than for the sine wave rectifier input of Tamez et al. [106], hence improving power throughput. A diode on time of 91 and 93 % was achieved in this demonstrator for the US and EU mains cases, respectively.

Since the mains voltage is already standardized, both system parameters V_{AC} and f_{mains} are fixed. Figure 4.6 shows the output power capability of an ideal AC–DC stage as function of the two remaining degrees of freedom. A trade-off between input capacitance C_{in} and the output voltage V_{out} is observed. On the one hand when V_{out} is fixed, the average capacitor current $< |i_{C_{in}}| >$ of Eq. (4.7) is linearly influenced by the input capacitor C_{in} and consequently the output power given by Eq. (4.8) also scales linearly. Alternatively, when keeping the series input capacitor constant, a higher output voltage V_{out} results in a lower average input capacitor current as can be seen in Eq. (4.7). However, this effect is negligible for voltage values of V_{out} below 50 V and therefore the output power relation as function of V_{out} scales linearly in this region.

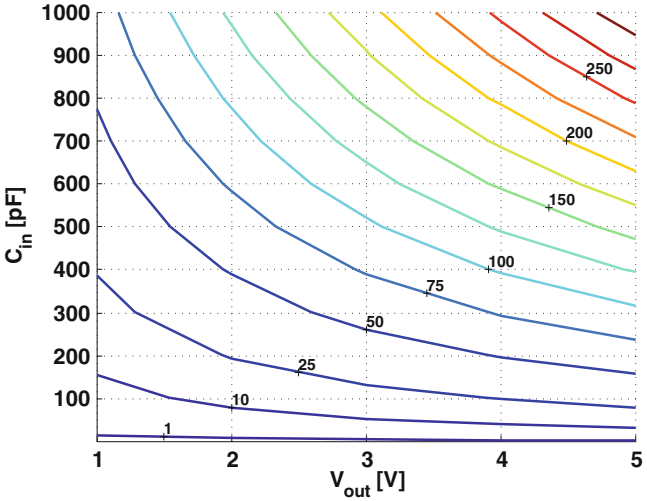

Fig. 4.6 Trade-off in achievable output power (µW) as function of parameters C_{in} and DC output voltage V_{out} for $V_{in,RMS} = 230\,\text{V}$ and $f_{mains} = 50\,\text{Hz}$

4.5 Implementation in CMOS

4.5.1 High-Voltage Passive Components

Capacitor C_{in} bridges the high-voltage gap between the high-voltage mains input and the low voltages on chip, as discussed in Sect. 4.3. While the active circuits do not come in contact with high voltage, the input capacitor C_{in} and input resistor R_{in} are subjected to a maximum voltage of V_{AC}, up to 375 V in the case of $V_{in,RMS} = 265\,\text{V}$. With the chemical-vapor-deposition (CVD) silicon oxide in the metal stack having a breakdown of at least $1\,\frac{\text{MV}}{\text{cm}}$ [111], a minimal spacing of 3.75 µm is needed to ensure breakdown will not occur. To this end the input capacitor was implemented as a metal–metal fringe capacitor with at least 4 µm of oxide between the capacitor plates. On top of that, metal corners were rounded to avoid the point effect. In Fig. 4.7 a top view of the custom layout of the capacitor is depicted and Fig. 4.8 shows a cross-section of C_{in}. The half unit cell of Fig. 4.8 must first be mirrored over its front plane. The resulting unit cell can then be expanded to obtain the total capacitor. The high-voltage plate is located solely in the top metal as to ensure sufficient spacing (>4 µm) to the low-voltage terminal and the substrate. Voids are left in this high-voltage plate through which the low-voltage plate, mainly located lower in the metal stack, rises up to the top metal. This structure was found to maximize fringing while considering metal density reliability rules. Nevertheless, capacitance density suffers from the widely spaced capacitor plates and $12.5\,\frac{\text{pF}}{\text{mm}^2}$ is achieved for this structure, resulting in a total C_{in} capacitance integration of 50 pF.

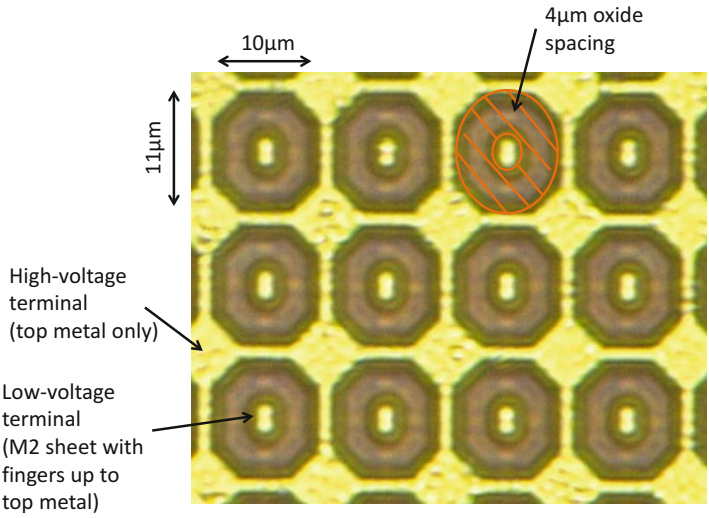

Fig. 4.7 Top view of high-voltage fringe capacitor custom layout representation

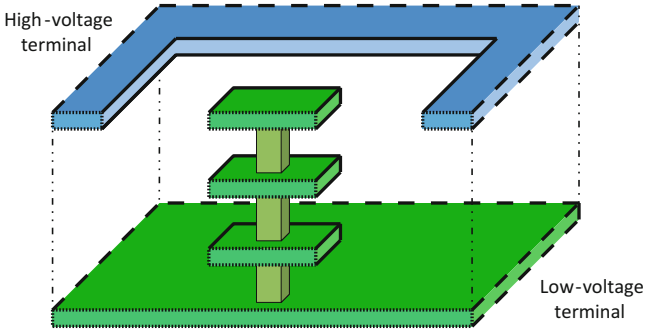

Fig. 4.8 Half unit cell of high-voltage fringe capacitor conceptual cross-section

The input resistor is implemented using a series connection of vias and the top two metals in the stack, ensuring a large spacing to the substrate (Fig. 4.9). Oxide spacing exceeds 6 µm to ground to be able to withstand even higher voltages, such as short spikes in the mains input. These result into additional inrush current events and consequently cause voltage drops across R_{in}, attenuating the voltage spike and causing a partial overvoltage relieving of C_{in}. Resistor R_{in} was designed to be 32 kΩ, with typical values after processing around 36 kΩ.

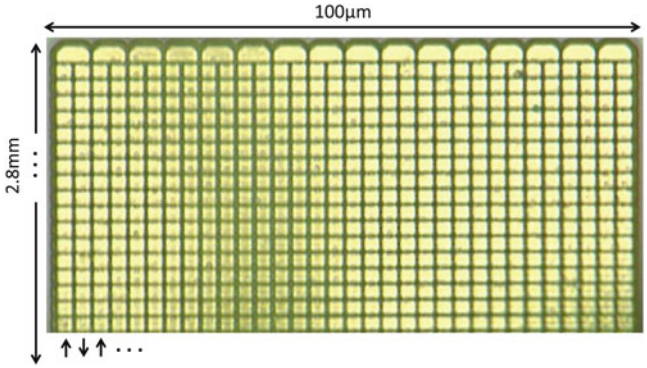

Fig. 4.9 High-voltage resistor composed of meandering top metals and vias

4.5.2 Regulation Circuits

A regulated output voltage V_{reg} of 3.3 V is desired. To this end, a regulation stage is implemented to post regulate the rectifier output. The minimum allowed value for V_{DC}, on which the regulation is performed, is found to be:

$$V_{DC} \geq V_{reg} + V_{LDOdropout,min} \tag{4.9}$$

Equation (4.9) demonstrates that V_{DC} must minimally be the regulated output voltage V_{reg} of 3.3 V, incremented with the minimal LDO dropout voltage $V_{LDOdropout,min}$. Achieving this headroom for series regulation while keeping $V_{DC,max}$ constrained to a safe operation value requires sufficient decoupling after the rectifier. The area underneath C_{in} is therefore efficiently reused to implement more than 10 nF of NMOS capacitance. Besides its necessity for safe operation, it also increases system efficiency, as less noise needs to be chopped off by the LDO, allowing the average value of V_{DC} to be decreased to a value closer to V_{reg}. For this reason, the prototype converter can optionally be decoupled with an external low-voltage 1 µF SMD capacitor. Transistors $M1$ and $M2$ are implemented with available thick-oxide LDMOS devices, as part of a set power devices rated up to 25 V available in the technology, to ensure safe rectifier operation. The Schottky diodes $D1$ and $D2$, forming the other half of the full-wave rectifier, do not cause overvoltage issues toward substrate either.

The post-regulation stage has a dual function, as previously mentioned. First, it is responsible for limiting the active circuit operation voltage V_{DC} by means of the shunt path. Secondly, a series regulator removes the noise that remains after the rectification.

Shunt Path

Transistor M_{sh} is a thick-oxide P-type LDMOS device, biased with an overvoltage protection control signal V_{pro}. When load power is decreased and V_{DC} increases above $V_{pro} + V_{th,M_{sh}}$ the P-type LDMOS will start to conduct and will limit the maximum of the rectified voltage to a safe value.

Alternatively, this shunt path can be addressed to shut down the converter. From Fig. 4.6 it follows that setting V_{DC} toward zero makes the output power P_{out} also collapse toward zero, achieving shutdown.

Low-Dropout Regulator

The LDO regulates the rectified voltage into a noise-free output voltage V_{reg}. Considering the limited power budget available at the output from the AC–DC stage, it is imperative that power consumption of this regulator is low compared to the full budget, in order to minimize the impact on system efficiency. Thus static currents in the error amplifier and feedback path were chosen to be 100 nA and 50 nA, respectively. A gain-bandwidth of 100 kHz was realized under the loading of the gate capacitance of M_{pass}, which can be sized relatively small due to the low expected current levels. The feedback path was chosen to be implemented by a diode-connected stack of 6 subthreshold-biased PMOS transistors in order to create a high-ohmic 1/3 voltage divider on a small chip area.

4.6 Chip Measurements

The converter prototype was measured for various mains voltage, frequency specifications. Figure 4.10 shows the maximum achievable output power as function of the input mains RMS voltage ranging from 85, 120, 230 up to 265 V and this for both 50 and 60 Hz cases. It can be seen that the achievable load power scales linearly with the input RMS voltage, but does not reach its full calculated potential. This is due to the limited amount of buffer capacitor C_{DC} available on chip. This causes V_{DC}, in the higher current range, to drop below the level needed to regulate the target V_{reg}. An external low-voltage SMD can optionally be used to alleviate this. When the input voltage frequency is 50 Hz, the load power scales from 3.6 µW for a 85 V input up to a maximum of 10.5 µW at 265 V. Similarly, with a 60 Hz frequency input the load power varies from 4.2 µW up to 12.7 µW. Measuring the efficiency involves quantifying the input power which, in contrast to the output power, is not a simple task. Specifically, the measurement of the input current through the $V_{AC,plus}$ terminal, from Fig. 4.3, failed. An approach with a current probe was insufficiently accurate due to the µA-range current levels to be measured. Alternatively, a voltage-based current measurement over the resistive series impedance was found to be infeasible due to the fact that the voltage drop over this impedance, which contains the

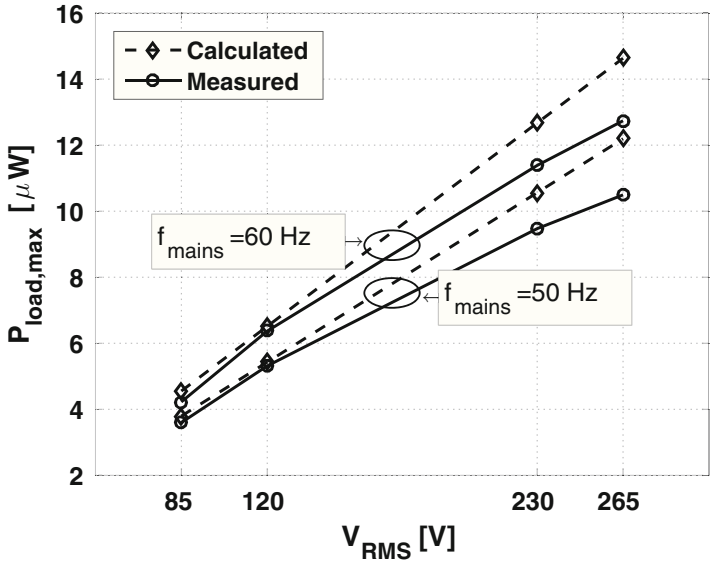

Fig. 4.10 Measured maximum output power for a regulated 3.3 V output as function of mains specification, for a C_{in} of 50 pF

information, itself is well below 1 V while it exhibits a common mode range equal to the peak-to-peak voltage of the mains. As such, it was not possible to accurately measure the input current and the efficiency, accordingly. However, simulations indicate an expected efficiency in the range of 70–75 % at nominal power.

Figure 4.11 shows the system voltage waveforms of both rectifier inputs, the rectifier output V_{DC}, and the regulated output voltage V_{reg} for the typical EU mains input case. For an input voltage and frequency of 230 V_{RMS} and 50 Hz the converter supplies 9.5 µW. After series regulation of the ripple clearly visible in V_{DC} the regulated output voltage V_{reg} exhibits a noise of less than 150 mV peak-to-peak, which is below 5 % of V_{reg}. The waveform inputs of the rectifier show the presence of a parasitic coupling in the measurement setup. Signal $V_{AC,minus}$ contributes more input current than its complementary signal $V_{AC,low}$. This imbalance is due to the fact that the generated mains signal in the test setup is not solely AC coupled as it should be, but also exhibits some DC coupling to ground. Since the proposed topology of Fig. 4.3 only employs one series capacitor, the parasitic DC coupling to ground can propagate into the measurement via the path with no series capacitor. To avoid this, another measurement was performed with 2 external 1 nF high-voltage capacitors. Both mains connections to the chip contained a 1 nF capacitor in this case, which are connected to the rectifier inputs. The according power is shown in Fig. 4.12 for the different mains input possibilities. In Fig. 4.13, it is now clear that the input power contribution of both mains half cycles is balanced, as would be expected of the topology.

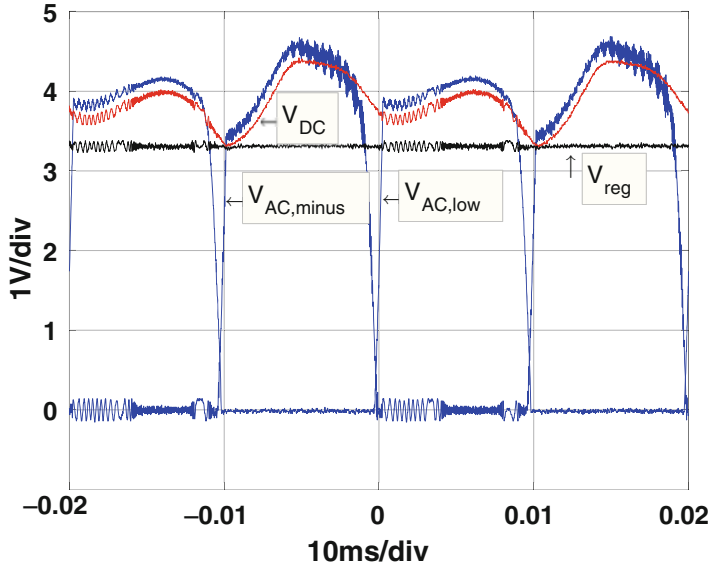

Fig. 4.11 Converter output waveforms for $V_{RMS} = 230\,\text{V}$, $f_{mains} = 50\,\text{Hz}$ input, and 3.3 V output, for a C_{in} of 50 pF

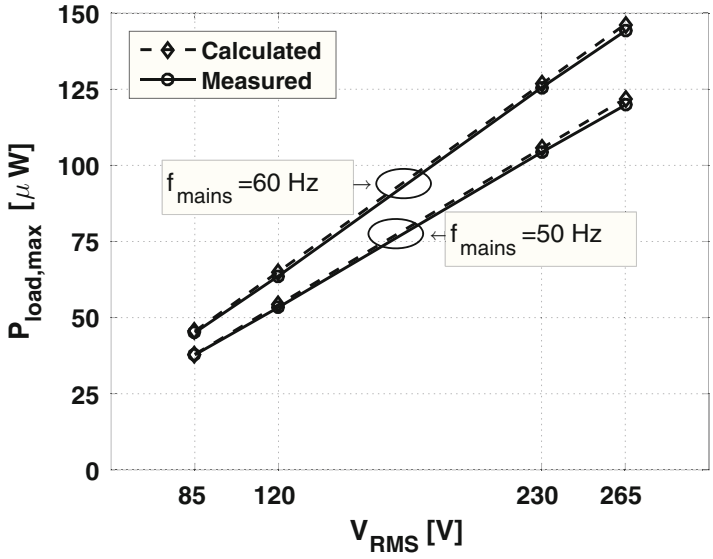

Fig. 4.12 Measured maximum output power for a regulated 3.3 V output as function of mains specification, for two external C_{in} capacitors of each 1 nF

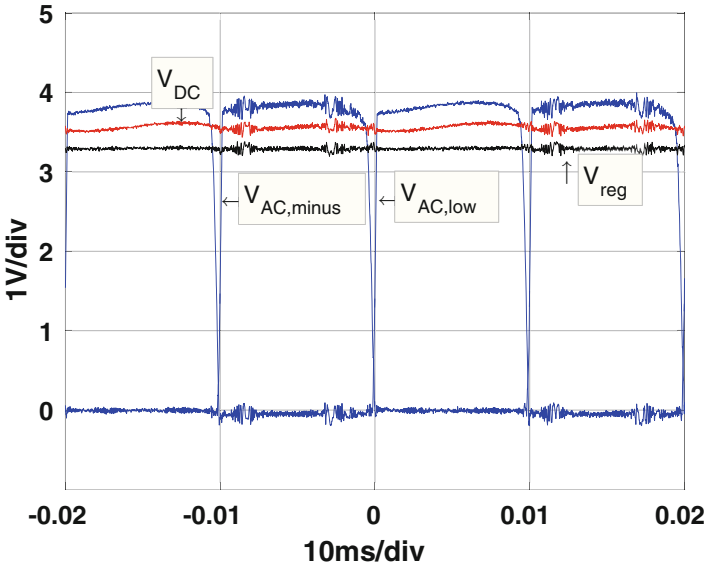

Fig. 4.13 Converter output waveforms for $V_{RMS} = 230\,\text{V}$, $f_{mains} = 50\,\text{Hz}$ input and 3.3 V output for the external C_{in} capacitors of each 1 nF

For all tested input cases, the output voltage V_{reg} can be regulated to a fixed 3.3 V over the full load power range from zero up to the maximum achievable load power P_{load} as presented in Figs. 4.10 and 4.12. This proves the functionality of the shunt path provided by M_{sh}, allowing for overvoltage free and stable operation over the full load power range, and the series LDO regulator.

A chip micrograph is shown in Fig. 4.14 and shows the die measuring 6 mm. Most of the area is occupied by the integrated high-voltage-capable passive components C_{in} and R_{in}. For area efficiency the NMOS capacitor decoupling device routed up to metal 1 is located underneath the actual high-voltage input-series capacitor C_{in}, which itself is fabricated using metals M2 and above. The stacking of these devices is possible without oxide breakdown because only the *high* terminal of C_{in} is subjected to high voltage and is confined to the top metal.

Finally a comparison of the proposed converter with a prior state-of-the-art integrated AC–DC converter is given in Table 4.1. The measurement results of this converter show increased power density, demonstrating the enhanced converter architecture proposed in this work. On top of that, the input voltage range has been extended from 120 V_{RMS} up to the maximum of 265 V_{RMS}.

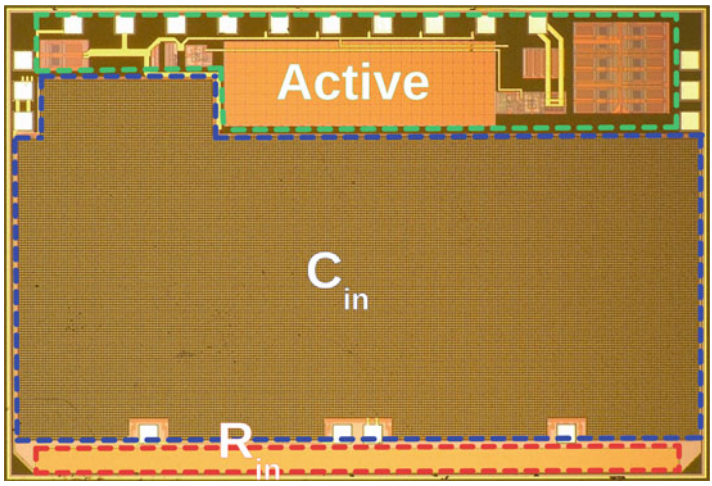

Fig. 4.14 Chip micrograph

Table 4.1 Specification comparison to prior art

Reference	[106]	This work		This work	
Tech node (µm)	0.13	0.35		0.35 + 2x 1 nF	
V_{RMS} (V)	120	120	230	120	230
f_{mains} (Hz)	60	60	50	60	50
Power/area (µW/mm^2)	0.43	1.06	1.58	–	–
V_{reg} (V)	4	3.3		3.3	
$t_{on,diode}$ (%)	48	91	93.5	91	93.5
$P_{out,max}$ (µW)	1.5	6.4	9.5	63.7	104.3

4.7 Conclusion

In this work, a high-voltage-capable capacitive AC–DC step-down interface is fully integrated in 0.35 µm CMOS, altering the external components requirement from multiple high-voltage devices to a single optional low-voltage SMD for improved performance. The presented converter architecture ensures an optimal operation because voltages $V_{AC,low}$ and $V_{AC,minus}$ approach square-wave behavior, as is the case of the ideal model, enabling maximal rectifier diode on times and hence maximal power throughput. The prototype measurements show achievable load powers of 6.4 and 9.5 µW in the most typical cases of 120 V_{RMS}, 60 Hz and 230 V_{RMS}, 50 Hz, respectively. This, while a fixed 3.3 V regulated output can be supplied with a peak-to-peak voltage ripple of less than 5 % over the full output power range.

Chapter 5
Two-Stage Approach for Compact and Efficient Low Power from the Mains

5.1 Introduction

This chapter continues the investigation of Chaps. 3 and 4, but introduces an alternative solution approach to realize the same goal of extracting relatively low amounts of power from the mains into a low DC voltage, and this at high efficiency.

Investigating a new system concept is a logic next step as the approach of Chap. 4 explored, and reached, the power throughput limits of a monolithic approach in a 0.35 µm CMOS process. Although the integration of very high voltage, over 100 V, passive components is possible within the metal stack and thus enables the ability to interface the mains, the combination of the low realizable density of the passive components, the low mains frequency, the fixed input voltage, and the required low-voltage output, resulted in µW-level output power, as indicated by Eqs. (4.7)–(4.8). Since there is little to no maneuverability in either of these contributors, a limit is reached. Therefore, another system concept is proposed, which consists of two independent voltage converters in cascade, to increase the degrees of freedom and consequently the implementation flexibility. This enhances the feasibility of simultaneously realizing all target specifications, introduced in Chap. 3.

The introduction of a solution concept that allows a high flexibility goes hand in hand with the introduction of many trade-offs, which need to be investigated and explored. This will be the main focus of this chapter. Questions such as which converter to use in each stage, the order of the converters, how to allocate the total mains conversion over these two converter stages, regulation of the whole, etc. will need to be answered.

Section 5.2 discusses the aspects and consequences of a two-stage approach. Possible implementations for the primary and secondary conversion stage are proposed. Section 5.3 provides insight in the trade-offs of switched-capacitor converter topologies, and their generation. Multiple candidates are analyzed and compared for application in the proposed two-stage system approach.

H. Meyvaert, M. Steyaert, *High-Ratio Voltage Conversion in CMOS for Efficient Mains-Connected Standby*, Analog Circuits and Signal Processing,
DOI 10.1007/978-3-319-31207-1_5

5.2 Subdivision of the Voltage Processor

5.2.1 Synergy Through Cascading

The monolithic implementation of Chap. 4 demonstrated the difficulty of combining all required voltage processing steps into a single solution. Especially the high-input-voltage level, far beyond what the active devices are rated for, limits the circuit possibilities. This section discusses the opportunity and impact of subdividing the total conversion step into two individual, cascaded steps.

Partitioning the total mains conversion step into two independent converters allows the research challenges, associated with extracting low power from the mains and discussed in Sect. 3.4, to be spread out over both converters. This spreading may consist of distributing the realization of a single specification, e.g., the total voltage conversion ratio, over both converters. At the same time, it is possible to allocate and confine a system specification, e.g., the handling of the mains input voltage, into a single converter. Thus, a two-stage approach unlocks the positive synergy of the individual building blocks by allowing each subblock to more efficiently focus on a subset of the total tasks, possibly yielding a solution with a higher end-to-end performance.

Typical off-line AC–DC power supplies with output power levels exceeding 75 W, which require them to have a limited emission of harmonics as dictated by the IEC 61000-3-2 Electromagnetic compatibility (EMC) harmonics directive, even split the problem into three individual converter stages. In this case, a first stage typically consists of a power-factor-correction (PFC) boost stage of the mains to a DC voltage in the range of 400 V, to ensure compliance with the IEC 61000-3-2 norm. Secondly, an isolated DC–DC step-down conversion covers the bulk of the very large voltage conversion ratio and has the benefit of a constant input DC voltage, regardless of the line conditions. Finally, the third and last conversion stage implements a point-of-load DC–DC converter to provide a load-specific supply voltage, conform to specifications such as voltage ripple and load regulation [18]. This division of the total voltage processing into individual specification-targeted subsystems simplifies the system as a whole. However, the end-to-end efficiency of a cascade of k subsystems is determined by the product of each of the k stages, as given in Eq. (5.1). Consequently, using the assumption that each subsystem has the same efficiency, each of the k subsystems should have an efficiency as dictated by Eq. (5.2) to reach a desired system efficiency. An end-to-end efficiency of 90 % requires to realize each subsystem stage at an efficiency of 94.7 and 96.5 % in the case of a two-stage and three-stage approach, respectively. A trade-off is observed, subdivision of a problem in a number of cascaded stages can enable a positive synergy, but too many cascaded stages will render the benefits undone.

$$\eta_{end-to-end} = \prod_{i=1}^{k} \eta_{subsystem,i} \tag{5.1}$$

$$\eta_{subsystem,i} = \sqrt[k]{\eta_{end-to-end}} \tag{5.2}$$

5.2.2 Considering the Low-Power Mains-Connected Context

The output power level in the targeted context of low power from the mains does not require compliance with IEC 61000-3-2 and consequently the development of a prototype needs no special attention toward the emission of harmonics. Therefore, it is not required to draw a continuous current from the mains, allowing full flexibility in the mains-interfacing circuit. Consequently, this investigation assumes a two-stage approach to be sufficient, unless show-stopping issues come to light during the course of the exploration, which would lead to reiteration toward a different solution approach.

Figure 5.1 schematically represents a cascade of two converters to distribute the voltage processing steps: rectification, voltage conversion, and regulation. By only cascading two stages, the impact of cascading on the efficiency from Eq. (5.1) is kept to a minimum. Considering the target specification of Chap. 3, the input voltage V_{AC}, the output voltage V_{OUT}, and current i_{out} are already defined. The remaining design choices, taking Fig. 5.1 into account, are on the one hand the topology of the first stage or primary conversion step, the second stage or secondary conversion step and the voltage V_{DC} that links them in between. On the other hand, it is up to the designer to divide or allocate the voltage processing steps to one of the two converter stages. Making the correct design choices is a key moment in the project as global optimization of the total system can only be achieved through making design decisions with the global picture in mind. Considering this perspective, the design choices are now discussed in further detail.

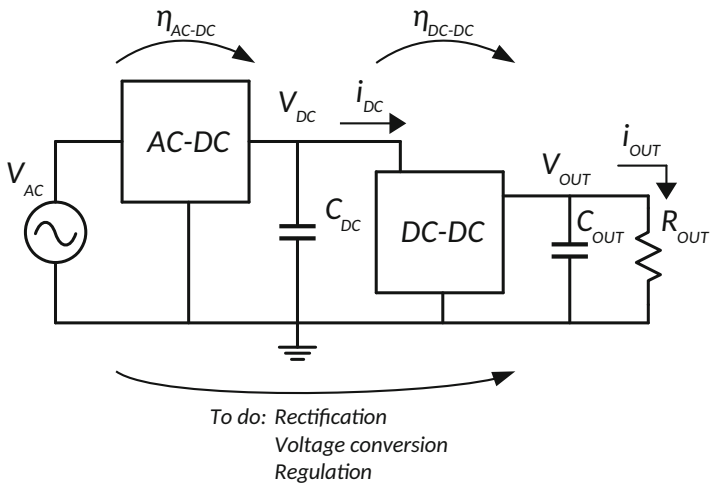

Fig. 5.1 Two-stage system concept

5.2.3 Design Choice Overview

From Fig. 5.1, it is clear that the design choices, in essence, can be reduced to selecting the DC bus voltage V_{DC} and choosing where to apply rectification and regulation. By selecting V_{DC}, the division of the total voltage conversion ratio over the converter stages is immediately set.

Bus Voltage

Increasing V_{DC}, on the one hand, reduces the voltage conversion ratio of the first stage and enables this stage to be more efficient. Moreover, a higher bus voltage will lead to lower bus currents. Inevitably, unwanted resistance is found in the bus that forms the link between the primary and secondary converter. A lower bus current consequently reduces the bus impedance loss caused by its IR drop, or similarly reduces the packaging requirements of the interconnect. Finally, a higher intermediate DC voltage has a strong impact on the energy stored in the capacitor C_{DC} as the stored energy is related to the square of the storage voltage. Consequently, the energy available from this buffer capacitor, given a specified capacitor voltage discharge, is given in Eq. (5.3):

$$\Delta E_C = \frac{1}{2} C (V_{begin}^2 - V_{end}^2) \tag{5.3}$$

Both a larger allowed voltage discharge range and a higher absolute voltage at which this range is situated result in a lower capacitance requirement for a specific amount of energy extraction. Since this investigation aims at low output power levels, this can be of particular use to buffer the required output energy during a (rectified) mains cycle of (10 ms) 20 ms. To illustrate, buffering 100 mW for a period of 20 ms, requires 2 mJ of energy storage in the buffer capacitor. This can be achieved, according to Eq. (5.3) and a 100 % efficient secondary conversion stage, by allowing a 22 µF buffer capacitor, initially charged to 50 V, to discharge by 1.85 V.

The ability to fully buffer a mains cycle enables even more flexibility in the primary conversion step. Next to not yet having specified its output voltage, it is not required to have a continuous power transfer, both from the mains input harmonics-emission perspective as well as the energy flow perspective at the output.

Decreasing V_{DC}, on the other hand, reduces the voltage conversion ratio of the second stage and enables this stage to be more efficient. When this is taken up to the point that it is required to convert an input of only a few volts, the possibility to use a low-voltage standard CMOS process technology emerges. Using such a plain-vanilla process reduces the cost of the secondary conversion step and simultaneously increases the compatibility and feasibility to co-integrate this conversion step side-by-side with its intended load.

Rectification

Rectification of the mains voltage is a simple voltage processing step, which can be implemented passively and requires in this case either two or four diodes for half-wave or full-wave rectification, respectively. Alternatively, a mains-voltage-rated switch can be inserted between the mains and the primary converter to only turn during the positive half-wave and also achieve half-wave rectification. Extending this concept can of course achieve full-wave regulation. To avoid negative voltages further upstream in the system, rectification is best implemented at the beginning of the first conversion step.

Considering the option of selecting an appropriate buffer capacitor C_{DC} and storage level V_{DC} combination, with an allowed voltage deviation, it is not explicitly required to implement full-wave rectification. Instead, an additional 1 mJ, equal to 100 mW sustained over 10 ms, should be stored to buffer the negative half-wave of the mains in the case of an ideal secondary conversion step. However, the addition of extra diodes to achieve full-wave rectification has a lower volume impact than the capacitive storage of 1 mJ. Hence, full-wave rectification is preferred from a system-level perspective.

Regulation

Regulation involves the conditioning of the output voltage to remain within its specified tolerance, regardless of the dynamics that occur, within their own specification limits, at both the line and the load. The exact conditioning requirements of the output supply voltage depend on the load circuit functionality. In digital circuits, a critical specification is the minimum supply voltage level that occurs in a worst case, because the circuit speed is related to the supply voltage. Consequently, a lower than specified supply voltage can yield slower than specified signal propagation, corrupting calculations [37]. Besides the minimum supply voltage constraint of V_{min}, digital circuits are very robust to supply noise, although all overhead voltage beyond V_{min} results in increased loss power [1, 32]. In contrast, analog circuits are more sensitive to output voltage ripple amplitude and frequency [80]. The importance of the load supply voltage on its performance motivates implementing regulation as close as possible to the load. This is confirmed in the ongoing power supply granularization, in which the power supply is distributed within the load [86, 103]. As such, the feedback path is as short as possible and hereby the impact of the interconnection parasitics on the controller performance is minimized.

Design Choice Summary

The implementation of rectification and regulation is best allocated to the primary and secondary conversion step, respectively. With respect to the division of the voltage conversion ratio over the two converter stages, the above discussion indicates

that increasing the intermediate voltage V_{DC} unlocks a system-level advantage. However, this does not yet pose any absolute voltage requirements for V_{DC}. As a result, settling on a suitable intermediate DC voltage still contains a degree of freedom. The resulting flexibility can now be exploited to select this parameter as trade-off in terms of the performance of the first and second converter stage, so that the system end-to-end efficiency in Eq. (5.1) is maximized. To this end, an implementation-oriented discussion of possible primary and secondary converters follows.

5.2.4 Primary Converter

The purpose of this section is to explore options to deliver an intermediate voltage V_{DC} with the mains as input. Within the context of a low-power supply from the mains, it is not required to have power factor correction and isolation. Instead, it is highly regarded to perform well in terms of efficiency, compactness, and cost. At this time, it is noted that the focus of this work is monolithic integrated circuit design and that it does not intend to cover the intricacies and optimization of discrete off-line power converters, which merits its own dedicated study. However, with respect to the realization of a feasible and efficient mains converter system, a brief overview of conceptual first conversion stages suffices. By doing so, the primary converter can from hereon be regarded as a black box, but with the knowledge that it can actually be realized.

Capacitive AC–DC Step-Down

The capacitive AC–DC step-down converter topology, monolithically implemented in Chap. 4, is revisited. Relieving the requirement to be fully integrated enables to increase the capacitance of the high-voltage capacitor in series with the input by implementing it with an off-chip component. This increases the input current of Eq. (4.7). Moreover, a higher output voltage out of the capacitive step-down topology, up until $\frac{1}{2}V_{AC,pk}$, results in a higher output power throughput [Eqs. (4.7) and (4.8)]. Figure 5.2 demonstrates this by showing the required input-series capacitance C_{in}, as function of the V_{DC} intermediate bus voltage, to provide a 100 mW at V_{DC}. As example, both the EU 230 V_{RMS} at 50 Hz mains as well as the US 120 V_{RMS} at 60 Hz mains data are plotted. It can be observed that the required C_{in} value rapidly decreases with increasing bus voltage, down to its minimum value of 18.9 nF, for the EU case, at $V_{DC} = \frac{1}{2}V_{AC,pk} = 162.6$ V. After this minimum, the required C_{in} increases again and can be found by mirroring the plot over the vertical $V_{DC} = 162.6$ V−axis, similar to how the US data can be mirrored across $V_{DC} = 84.9$ V. From the data in Fig. 5.2, a V_{DC} of 84.9 V fulfills the minimum C_{in} for the US mains, while the minimum EU C_{in} value is already nearly reached. However, the sensitivity of C_{in} is not strongly dependent on the exact bus DC

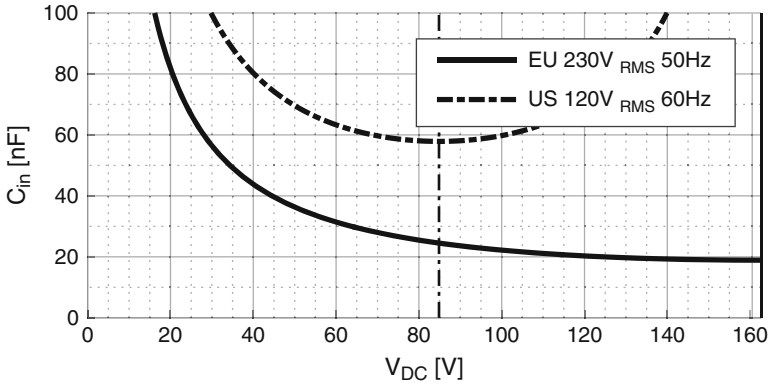

Fig. 5.2 C_{in} capacitance requirement as function of V_{DC} for 100 mW of output power

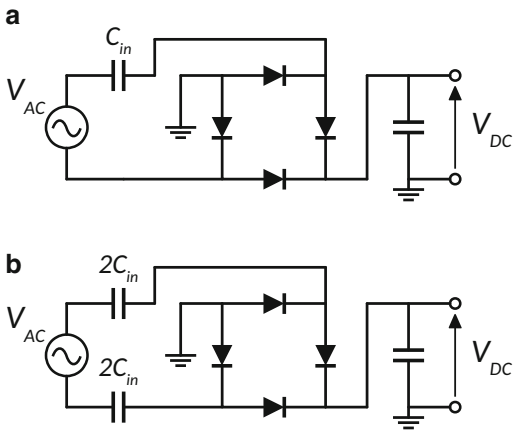

Fig. 5.3 Capacitive AC–DC step-down circuit equivalence with (**a**) one series capacitor and (**b**) two series capacitors

voltage value in this range and, with respect to the performance and feasibility of the secondary converter, can be selected to be lower for only a relatively small increase of C_{in}. As such, less is more.

Figure 5.3a, b depicts two implementation possibilities of the capacitive AC–DC step-down topology. The input capacitor C_{in} matches with that of Fig. 5.2. When comparing the two possibilities of Fig. 5.3, the option with only one series capacitor seems to be better as, in total, only a quarter of the total capacitance is necessary than in the other case. However, in this implementation, the capacitor needs to be rated for twice the voltage, which will roughly take twice as much volume. Therefore, the difference between the two implementations, regarding volume, is only a factor of two.

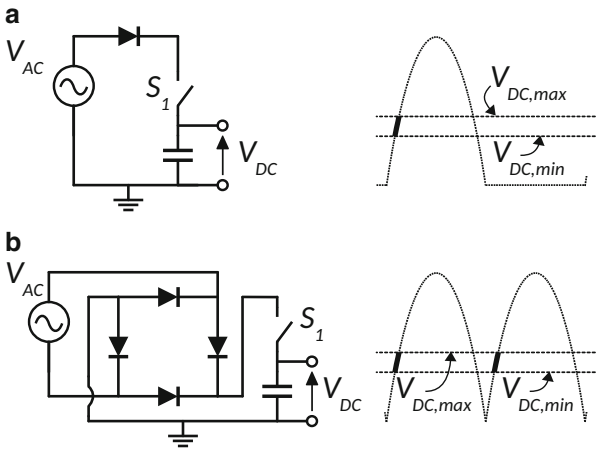

Fig. 5.4 Principle of charging the buffer direct from the mains with (**a**) half-wave rectification and (**b**) full-wave rectification

Direct Buffer Charging

An alternative approach to deliver energy to a secondary converter stage is shown in Fig. 5.4. The principle is to charge the buffer capacitor by directly connecting it to a half-wave or full-wave rectified version of the mains, as exemplified by Fig. 5.4a, b. This can be done in an efficient fashion if switch $S1$ closes to connect the capacitor C_{DC} to the rectified mains when it has voltage $V_{DC,min}$. The capacitor is then charged by the mains and once it has reached the $V_{DC,max}$ level, switch S_1 is opened. By doing so, the buffer capacitor C_{DC} can be periodically replenished, either at the mains frequency or twice the mains frequency in case of half-wave or full-wave rectification, respectively.

The consequences of this approach are that the buffer capacitor, and its allowed voltage discharge range, must be sufficiently large, as given by Eq. (5.3). Alternatively, switch S_1 has short on-time, during which it must sustain the buffer capacitor charge current. In the example of Sect. 5.2.3, where every cycle 1.85 V is required to be replenished to a 22 µF capacitor, this translates into a $S1$ on-time of 27 µs. Switch S_1 is required to sustain 1.5 A during this interval. The timing constraints related to direct charging of the buffer capacitor can be relaxed, but requires the implementation of an additional boost or non-inverting buck-boost DC–DC converter to extend the voltage window in which the mains can be used as input source to charge the buffer. The added voltage conditioning of the extra DC–DC converter increases the charging time window and consequently reduces the charge current. Alternatively, the timing related to direct charging of the buffer capacitor can also be reduced by reducing the buffer capacitor. Hereby, the buffer storage energy is reduced, limiting the output power specification of the system to a lower value. But to conclude, this can be a suitable approach if, instead of 100 mW, it is the target to realize a lower output power specification.

5.2.5 *Secondary Converter: High-Efficiency and High-Ratio DC–DC Voltage Conversion*

In subdividing an AC–DC converter system for low power from the mains, this chapter has discussed, in Sect. 5.2.3, the benefits of increasing the intermediate DC bus voltage from a system functionality point of view. However, this proposition is only valid on the premise that it is feasible to implement a highly performant DC–DC converter, which must handle a large voltage conversion ratio and regulation on the side, as secondary conversion step. This section will discuss implementation options to achieve a DC–DC converter with such specifications.

High-ratio voltage step-down conversion is typically performed by inductive synchronous buck converters. Only recently, their switched-capacitor counterparts are evolving in this direction [68, 84, 87]. Despite the widespread use of inductive converters for this application, the fundamentally different operation of SC converters shows promise to outperform inductive converters at a high voltage conversion ratio. SC topologies generally require a larger number of components than inductive converters, but still compare favorably in terms of volume due to efficient component utilization [34, 68].

An inductive buck converter is shown in Fig. 5.5a and uses only 2 switches and 1 inductor, but these need to be rated for the full input voltage and current. It depends on the Pulse-Width Modulation of its duty cycle to set the VCR. This offers the advantage to flexibly alter the VCR in a continuous way. Consequently, the inductive buck converter depends on very low duty cycles for high step-down ratios. This becomes an issue as higher switching frequencies are desirable to get a smaller inductor. A low duty cycle in combination with a high switching frequency leads to a very short on-time of the high-side power switch. Since this device handles the full input voltage and current, a significant amount of power is consumed in its high-speed (de)activation.

In contrast, the VCR of an SC DC–DC converter is mainly set by consecutive capacitor configuration transitions that make up the switched-capacitor topology. These configuration transitions are similar to those in a buck converter, but because it only contains capacitors, the voltage conversion ratio is consequently a topology-specific parameter. The maximum achievable VCR, given in Table 5.1, depends on the number of charge-transfer phases within an operation cycle and on the number of flying capacitors in the topology [52]. This enables the key advantage of fixed duty-cycle operation, regardless of the VCR. Figure 5.5b, c shows how the highest VCR can be reached by a 2-phase and a 3-phase SC topology, using two flying capacitors. The voltage conversion ratio is 3 and 4, respectively.

Besides the previously addressed popular synchronous buck converter, other approaches are emerging in research. Resonant conversion is employed in a 50 V to 5 V prototype [51]. The power density is increased through using a switching frequency in the Very High Frequency (VHF) range, which on its own is made

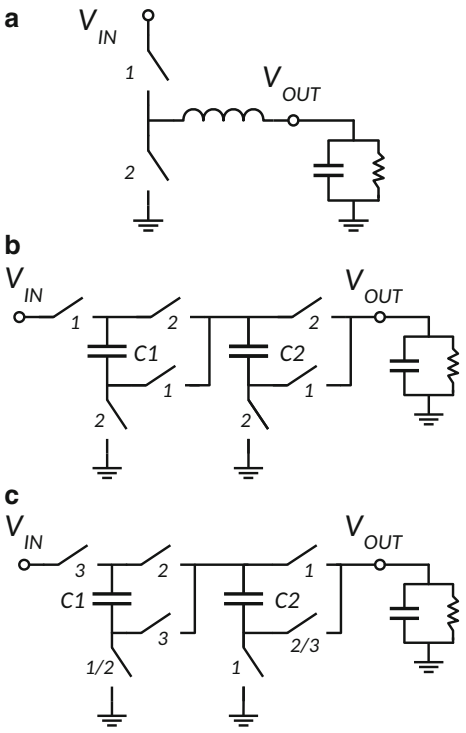

Fig. 5.5 Inductive and capacitive options for DC–DC conversion. (**a**) Switched-inductor step-down converter; (**b**) 2-phase SC DC–DC converter topology, demonstrating a VCR of 3 with only 2 capacitors; (**c**) 3-phase SC DC–DC converter topology, demonstrating a VCR of 4 with only 2 capacitors

Table 5.1 Maximum voltage conversion ratio as function of the number of flying capacitors

# Flying caps	1	2	3	4	5
2ϕ VCR_{max}	2	3	5	8	13
3ϕ VCR_{max}	2	4	7	13	24

possible by reducing the switching losses with Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) conditions. The peak efficiency of this approach is reported to be 82.9 % for a 1 W output, which is not compatible with the targeted specifications in Chap. 3.

Other hybrid capacitor–inductor converter topologies with focus on large voltage conversion ratio have been proposed as early as 1988 [64], but have only been gaining traction in the field of integrated power management more recently in the form of multilevel converters [120], soft-charging converters [46, 75, 99], and resonant switched-capacitor (ReSC) converters [35, 88]. Even though not all of these research prototypes implement large voltage conversion ratios, it is clear that the combination of capacitors and inductors yields promising results.

5.2.6 *Summary of System Considerations from Full-System Point of View*

The discussion in this section has introduced, motivated and explored benefits and trade-offs present in a two-stage approach to realize an AC–DC conversion to extract low power from the mains. The beneficial trend of increasing the intermediate bus voltage V_{DC}, to voltage values above the typical level of about 12 V, has been discussed in Sect. 5.2.3. To extract a more concrete and suitable DC bus voltage from this trend, the implementation feasibility for both the primary and secondary converters has been discussed.

From this discussion it can be concluded that from a primary converter perspective, in case of a capacitive AC–DC step-down converter as primary stage, bus voltages up to 84.9 V minimize the input-series capacitance requirement and consequently its related volume impact. However, a V_{DC} of 30 V and upwards can be seen to already offer a large reduction of C_{in}, with respect to using this topology as a single-stage mains to 3.3 V conversion. Hence, this V_{DC} range of 30 to 84.9 V can be used to optimize the trade-off between primary and secondary converter performance. In case of the direct buffer charging, it is not the absolute voltage level of V_{DC} that limits its application feasibility, but the ability to conduct a certain current during a short time window that sets the ceiling on the power throughput and consequently its useful operation range.

From the secondary converter perspective, there is growing interest in high-ratio voltage conversion DC–DC. Multiple approaches have been reported in recent research, each with benefits. As contribution to this field of exploration, Sect. 5.2.5 proposed the switched-capacitor approach for high-voltage-conversion-ratio DC–DC conversion and discussed its key differentiating features, which prompt expectations of high-performance operation. Therefore, this work selects the switched-capacitor approach to perform high-ratio voltage conversion and investigates the performance limit of these converters at a high VCR value. To that end, an in-depth discussion on switched-capacitor topologies is detailed in the next section.

5.3 Searching for Switched-Capacitor Converter Topology Candidates

5.3.1 *Topology Trends: Regularity vs Irregularity*

Even when only the minimum number of flying capacitors, as given in Table 5.1, is used in an N-phase SC topology, already multiple topology options are possible to achieve a certain VCR. Exceptionally, when the number of used capacitors equals 1, there is only one possible topology that achieves the maximum ratio condition of 2. Besides using the minimum number of flying capacitors necessary to obtain a

VCR, it is also possible to use a topology that requires many more. Consequently, the number of SC topologies that leads to a certain VCR is very large and this clearly makes the selection of an ideal topology candidate a non-trivial issue.

Having more capacitors than necessary allows the flying capacitor bias voltages, and consequently the voltage ratings, to be reduced. This leads to switched-capacitor DC–DC topologies with high regularity where not only the capacitor voltage ratings are low, but those of the switches as well. This is demonstrated by the ladder converter of Fig. 6.9, where all flying capacitors and all switches have a voltage rating requirement of one unit value, V_u. $1\,V_u$ corresponds to $1\,V_{IN}$ or $1\,V_{OUT}$, whichever is the lowest, the former in case of step-up conversion and the latter in case of a step-down conversion. Highly regular SC topologies with low switch and capacitor voltage ratings are ideal from a CMOS integration point of view as the use of many devices to reduce individual component ratings is not penalized due to monolithic integration. At the same time, the reduced component ratings are a necessary condition if the low-voltage devices of CMOS are to be used. Unfortunately, regular topologies with only low-voltage components are not among the most efficient in capacitor utilization [90], increasing the capacitance requirement to obtain a specific output impedance R_{OUT}. On top of that, CMOS integration has limitations. The relatively low capacitance densities of integrated capacitors result in a substantial die area consumption. Moreover, non-negligible parasitic capacitive coupling to the substrate makes up for an important loss contribution [60]. Therefore, a monolithic SC DC–DC converter combining high efficiency, high power density, and high VCR is currently out of reach of standard available CMOS technologies. Less common capacitor technologies, like the advanced-process deep-trench capacitors [124] and the advanced-material-property ferroelectric capacitors [82], offer increased performance at an increased production cost. As alternative to costly integrated capacitor technologies, it is also possible to sacrifice monolithic integration and use cheap commercial off-the-shelf ceramic capacitors.

The targeted combination of high efficiency, high VCR, and high-input voltage in a compact and low-cost SC converter motivates fully integrating the power switches, control logic, and auxiliary circuits, while keeping the flying capacitors external. This enables larger capacitance with lower parasitics compared to integrated capacitors, but also adds 2 pads per capacitor to the pin count. Thus, when external flying capacitors are used, it is highly desirable to use SC topologies only needing the minimum number of capacitors of Table 5.1 to keep the pin count low. Topologies with a minimal capacitor count, opposite to regular SC topologies with many more capacitors, lead to highly irregular structures. Switch and capacitor voltage ratings of individual components can vary over a large range. However, voltage ratings equal or greater than the full input voltage rating, when in step-down, are uncommon to occur due to the structural stacking nature of SC topologies.

Among SC DC–DC converters with minimal capacitor count for a specific VCR, a 3-phase approach as demonstrated by Karadi and Villar Piqué [34] can require less flying capacitors to achieve a certain VCR compared to regular 2-phase SC converters [52, 53], as stated in Table 5.1. But there is a penalty in efficiency due to a less optimal component utilization. As each phase only lasts 33 % of the period,

compared to 50 % in 2-phase operation, larger switches are necessary, which leads to an increased switching loss. Moreover, the addition of phases to a switched-capacitor topology increases the gate-drive complexity. As power switch drain and source terminal voltages are likely to change with each topology reconfiguration, so does the gate voltage and its the gate-driver requirements. Indeed, this has an impact on efficiency through its related circuit overhead. Nevertheless, limiting the number of capacitors to the strict minimum in order to keep the pin count low, inevitably, leads to higher complexity in the power-switch drivers of the selected irregular SC topology. The goal of an as high as possible efficiency, as required to realize an attractive two-stage system efficiency, in this work leads to the selection of a 2-phase SC converter.

5.3.2 Switched-Capacitor Topology Construction

In order to investigate a suitable two-phase switched-capacitor DC–DC topology, it is necessary to have insight into how one is constructed and to what rules it must adhere to. To clarify the following discussion, the naming of the elements that make up an SC topology is now defined. A switched-capacitor DC–DC topology may consist of N multiple capacitor configurations, which are sequentially activated by opening and closing the related power switches. Hence the name switched-capacitor topology. A cycle or switch cycle can be defined as the sequential activation of these N capacitor configurations. As such, a cycle consists of N phases, each representing one of the N capacitor configurations. Hence the origin of an N-phase SC topology. The capacitors transfer charge and consequently are called charge-transfer capacitors. As this charge transfer results from the relocation of these capacitors to a different absolute potential, during which their capacitor bias voltage ideally remains unchanged, they can also be called flying capacitors. Multi-phase operation, a widely popular ripple reduction technique, is not to be mistaken with the N phases of a switch cycle. Instead multi-phase operation consists of, and can be described more uniquely, by the time-interleaved operation of M converter fragments. A converter fragment is readily obtained by dividing an SC converter's switch and capacitor resources into M equal fragments.

An SC topology consists of an input voltage source, an output voltage source as load, any number of charge-transfer capacitors and switches to configure these building blocks into the capacitor configurations of each phase. For the purpose of SC topology construction, it is only required to consider the voltage sources and the flying capacitors, which are assumed to be ideal and therefore approximate a voltage source. However, they differ in the ability to source or sink charge. A real voltage source is able to source or sink charge indefinitely, i.e., only sourcing charge (input source) or only sinking charge (output load), and this during one or all of the phases of the topology cycle. In contrast, the flying capacitors cannot have an infinite capacitance, and consequently must be charged in at least one phase and discharged in at least one other phase, in order to achieve an equilibrium bias voltage

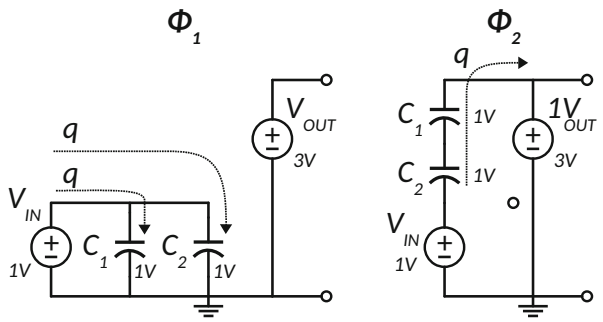

Fig. 5.6 1–3 series-parallel switched-capacitor DC–DC topology, shown without switches in its two separate phases

in steady state. In case of a two-phase converter, charging a capacitor in one phase leads to a necessary discharge during the other phase.

An example is given in Fig. 5.6 with a 1–3 step-up converter. During the first phase, the input voltage sources a charge amount of $2q$ to charge capacitors C_1 and C_2. During the second phase, the flying capacitors are reconfigured and the charge amount is now delivered to the output voltage load. Indeed, a voltage difference ΔV must be present between the steady-state capacitor bias voltage at the end of phase 1 and phase 2, in order for charge flow to occur. The voltage conversion ratio of 3, in Fig. 5.6, is idealized and consequently this ΔV is not shown. But once a non-zero current is consumed by the load, the effective output voltage will be lower than the ideal output voltage by the amount of the voltage drop that is caused by the load current over the finite converter output impedance. Each capacitor is charged during one phase and discharged during the other, resulting in an equilibrium capacitor bias voltage of 1 V in steady state.

In effect, the rules to construct a two-phase switched-capacitor DC–DC converter topology are fairly straightforward. An SC converter topology can be seen as a collection of voltage source input–outputs, switches, and capacitors, in which the steady-state capacitor bias voltages must mathematically fit in each configuration phase assembly. By switching over these phases during a switch cycle, DC–DC conversion is obtained. To avoid short-circuit currents that deteriorate efficiency, it is important that the consecutive topology phases are activated in a non-overlapping fashion.

5.3.3 Switched-Capacitor Topology Survey

In search of a suitable solution, multiple SC topologies are now explored and analyzed with respect to topology-specific performance defining parameters. These include the component voltage rating of the capacitors, the power-switch blocking

voltages, the charge transfer contribution of each component, and the required output signal swing of the power-switch drivers. Even though there is always a discrepancy from theoretical analysis to practical implementation, these parameters provide information and insight on the expected performance and implementation feasibility.

By using external flying capacitors, capacitance availability does not pose a bottleneck and parasitic capacitor coupling and its related power loss can be neglected. Consequently, the switching loss of the power switches and their drivers is focused on. As the required swing to properly drive a power switch becomes larger, the related power loss contribution is increased and robustness is simultaneously compromised. Therefore, SC topologies with the least demanding requirements regarding power switches and power-switch drivers are the target of the following topology survey. In the approach of using external capacitors, it is indeed preferred to keep their number to a strict minimum. To this end, a number of two-phase SC topologies are investigated that comply with the minimum capacitor requirement [53] to achieve a certain ratio, as given in Table 5.1. For a voltage conversion ratio up to 13, this translates into a flying capacitor count of 5. Next to this minimum requirement, it is also investigated if the power-switch gate-driver complexity is reduced in a few topologies, using one capacitor more as per minimally required. Due to the length of the survey result data, it is not included in this chapter, but instead is listed in Appendix A. Table 5.2 gives an overview of the eleven topologies under investigation, using the set of capacitor bias voltage ratings from high to low as denomination for each SC topology. With a target output voltage of 3.3 V, voltage conversion ratios in the range of 11–13 are investigated to end up with an intermediate DC bus voltage V_{DC} in the vicinity of 40 V.

As indicated in the result data, all voltage ratings in the survey are normalized to the output voltage. It can be confirmed that, as discussed in Sect. 5.3.1, the low capacitor count leads to irregular topology architectures with various possible component ratings. In general, the higher the component rating, the higher its volume/area impact. But this volume impact is linked to the discrete set of possible voltage ratings in which switches and capacitor are available. Therefore, a higher capacitor bias voltage or switch blocking voltage rating only leads to a volume

Table 5.2 Topology survey topologies overview

VCR	Capacitor bias voltages ratings	Appendix entry
11	33321	Table A.1
	65221	Table A.2
	83321	Table A.3
	44321	Table A.4
	222221	Table A.5
12	55221	Table A.6
	75221	Table A.7
	443111	Table A.8
	842211	Table A.9
	933211	Table A.10
13	85321	Table A.11

impact when it requires the component to be implemented with the next available, but higher-rated, device. The voltage impact on volume is a result from the fact that higher potential differences require larger physical terminal spacing to avoid dielectric breakdown. Although there is a continuous relation between terminal spacing and the maximum voltage before dielectric breakdown occurs, actual switches and capacitors are only available and optimized for a limited set of device ratings. Therefore, components are rarely used to their full rating and over-specification is inevitable. The lower the rating resolution in which components are available, the more over-specification is likely to occur. From the capacitor perspective, typical available component voltage ratings are 4, 6.3, 10, 16, 25, 35 V, and onwards. This gives a lot of flexibility to implement each capacitor with a COTS capacitor, with best matching voltage rating. When considering integrated switches, the number of available device voltage ratings is typically low and over-specification is common. However, switch stacking can be a solution, yet in some cases not practical, to increase the flexibility and is a good approach to better match the implemented switch voltage rating to the required functional switch blocking voltage, with as little over-design as possible.

From the data in Appendix A, it can be seen that the topology with voltage conversion ratio 11 and capacitor bias voltages 65221 is a promising candidate. It has the lowest requirement with respect to gate-driver output swing with only one driver needing a $3\,V_{OUT}$ swing, totaling 9.9 V. On top of that, the maximum switch blocking voltage is limited to $6\,V_{OUT}$, which with its 19.8 V matches with the available 20 V device rating of the available high-voltage CMOS process technology. Hereby, the need to use the next-in-line, and largely overqualified and lower-performance 40 V devices, is mitigated.

Figure 5.7 confirms these claims. Among the surveyed topologies, those with the lowest power-switch driver swing specification yield the best performance in simulation. The best candidate from this exploration is shown in Fig. A.2 and Table A.2 and is consequently selected for implementation, which will be the focus of the next chapter.

5.4 Conclusion

This chapter introduced a two-stage approach in order to increase the flexibility of an AC–DC conversion system, aimed at extracting a low power from the mains. The newly introduced design choices, as result of taking a two-stage approach, are discussed and trade-offs are highlighted. From this discussion, it is concluded that increasing the DC bus voltage to a level above the typical 12 V-level can yield a substantial benefit in the context of low power from the mains. Therefore, this chapter continued by investigating possible primary and secondary converter stages to serve in such an AC–DC converter with high intermediary bus voltage, with special focus on the possibilities to perform high-ratio voltage conversion in a highly efficient and compact fashion.

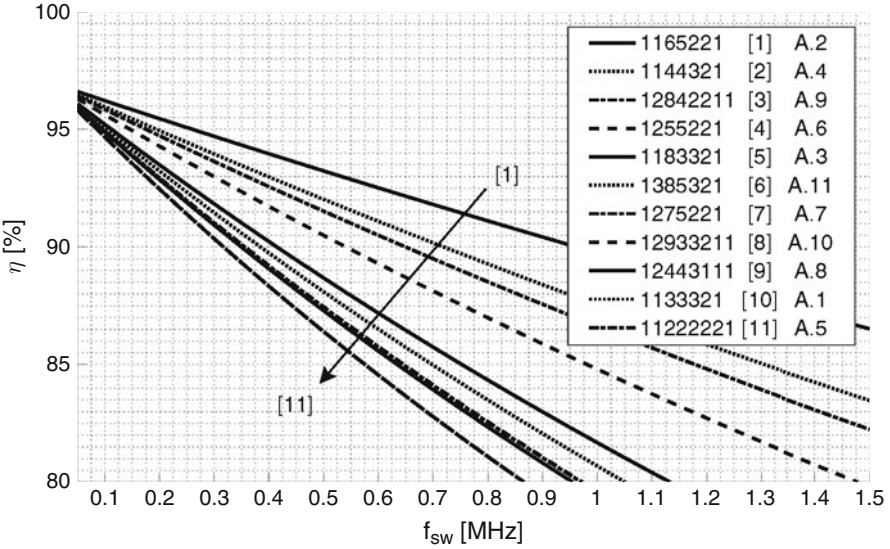

Fig. 5.7 Performance simulation of the survey topologies, for 100 mW at 3.3 V. Next to the naming of the topologies in this comparison, the corresponding appendix entry is given in the legend

Chapter 6
An 11/1 Switched-Capacitor DC–DC Converter for Low Power from the Mains

6.1 Introduction

This chapter describes the implementation of a switched-capacitor DC–DC converter to be used as second stage in the two-stage AC–DC system concept, introduced in Chap. 5. The converter is required to perform a large step-down voltage conversion ratio and this from a high-input voltage. Since this converter will be used in a two-stage system, where total efficiency is the result of subsystem efficiency multiplication, efficiency is the most important specification and is targeted to be at least 90 %. The output of the converter is expected to deliver 100 mW at 3.3 V, as provided in the project target specifications of Table 3.1. Other goals, next to the efficiency and output specification, are to obtain a compact solution that is low cost and robust. The targeted combination of high efficiency, high VCR, and high-input voltage in a small-volume SC converter motivates integration of the power switches, control logic, and auxiliary circuits, while keeping the flying capacitors external. This enables larger capacitance with lower parasitics compared to integrated capacitors, necessary to achieve the stringent efficiency specification. Since full monolithic integration is consequently infeasible, focus is shifted to keeping the number of external components to a strict minimum.

6.2 Motivation

Getting from the mains to a few volts to power electronic circuits requires a very large voltage conversion ratio since the rectified US and EU mains have DC levels of 169 and 325 V, respectively. Primary converters, such as flyback converters, use the winding ratio of the isolation transformer to achieve large step-down ratios to generate bus voltages of about 12 V. This bus voltage can supply a load system or

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be additionally down-converted, if necessary. The higher the bus voltage, the higher the efficiency of the primary converter can be and the lower the bus I^2R losses will be. This motivates the investigation of highly efficient DC–DC converters with a high-voltage conversion ratio to use as secondary converters in mains AC–DC applications.

Figure 6.1 shows a two-stage mains AC–DC system, of which the secondary DC–DC step-down conversion, and its implementation, is the focus of this chapter. Intermediate bus voltage V_{DC} is set to nearly 40 V in a trade-off between on the one hand the increased performance of the first stage, reduced I^2R losses at the bus, and a relaxed buffer capacitance specification, and on the other hand a reduced buffer capacitor voltage rating and complexity of the secondary stage. Spreading the mains AC–DC conversion over two cascaded stages allows increased design flexibility in each stage and enables each stage to focus more efficiently on a subset of the system challenges. Consequently, a two-stage approach is better suited to achieve the target specifications of this work, compared to a single-stage approach [58] in which the high-voltage constraints result in a power density limitation.

This chapter details the ratio-11 switched-capacitor DC–DC topology with capacitor bias voltage ratings 65221 and its implementation into an NXP 0.14 µm SOI BCD technology. To that end, the outline is structured as follows. A detailed overview of the proposed system architecture, its operation and implementation is given in Sect. 6.3. The need for additional circuits to support the actual main DC–DC converter automatically follows from combining the requirements of its reliable and functional operation. The main building blocks of the system are discussed in detail. To continue, measurements and performance validation follow in Sect. 6.4. Part of this validation includes the selection of appropriate COTS capacitors. Finally, key concepts and conclusions are summarized in Sect. 6.5.

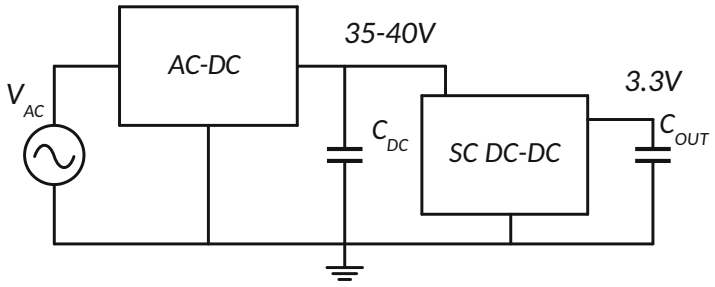

Fig. 6.1 Two-stage mains AC–DC system with high-voltage intermediate bus voltage and energy buffer C_{DC}

6.3 System Overview and Operation

6.3.1 Architecture

The system-architecture block diagram is shown in Fig. 6.2, indicating the on-chip circuits as well as the external components and reference inputs. The main 11/1 switched-capacitor power converter is located in the top-right corner and consists of 16 power switches, their drivers and 12 level shifters. It can be seen that all intermediate auxiliary DC supply voltages 0x ($0\,V_{OUT} = gnd$) up to 11x ($11\,V_{OUT} = V_{IN}$) are provided to the main converter by an auxiliary rail generator. These additional supply rails are necessary in control-signal level shifting and in the power-switch drivers. Five identical external 10 µF/25 V/0603 ceramic capacitors are used to implement the flying capacitors and the input V_{IN} and output V_{OUT} are also decoupled externally. The output voltage V_{OUT} is fed back into a lower-bound hysteretic controller, which closes the feedback loop. Figure 6.2 also shows a Multiple-Input Multiple-Output auxiliary (MIMO) rail generator and its control block on the left-hand side. This is an additional 11/1 fully integrated ladder converter, consisting of 22 switches, 21 capacitors, and 20 level shifters, to efficiently generate all intermediate auxiliary DC supply voltages.

Reference voltages and frequencies are externally supplied as this allows more flexibility during measurements. Also, their functionality is not part of the innovation goals that this work aims to demonstrate. Consequently, power consumption

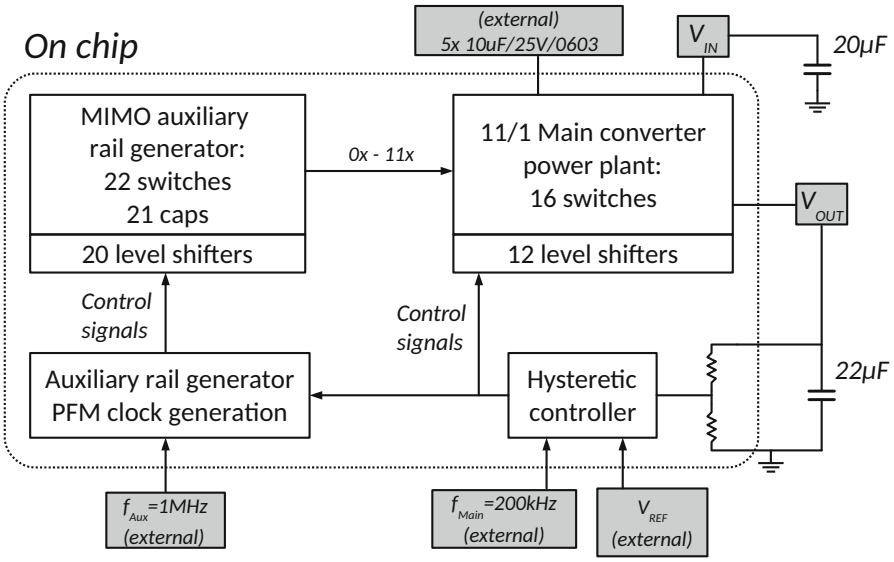

Fig. 6.2 System-architecture block diagram

related to the generation of these inputs is not included in the measured efficiency. Nonetheless, since on-chip buffering of the reference inputs takes place, power consumption due to the loading of these inputs is included in the efficiency.

6.3.2 11/1 Power Plant

Figures 6.3 and 6.4 show multiple aspects of the 11/1 switched-capacitor topology in detail. The two capacitor configuration phases are shown separately in Fig. 6.3. Switches are omitted in this representation for clarity. The capacitor structure connects to the input only during phase Φ_1, which results in the charging of capacitors $C_1 - C_3$ while $C_4 - C_5$ are simultaneously discharged. During the following phase Φ_2, the structure is reconfigured and capacitors $C_1 - C_3$ are discharged, while C_4 and C_5 are charged. Alternately charging in one phase and discharging in the other results in the steady-state capacitor bias voltages that are also shown in terms of the output voltage V_{OUT}, abbreviated in this work to $1\,V_u$ or 1x. More details on the topology-specific capacitor parameters are given in Table 6.1. Next to the capacitor bias voltages, the charge-transfer contribution per capacitor to the total output charge per cycle and the capacitors for each phase is given.

A full circuit implementation of the switched-capacitor topology, showing all capacitors and switches with their drivers, is given in Fig. 6.4. Switches S_{1-8} close in Φ_1, while S_{9-16} close in Φ_2. Switch blocking voltages, in terms of V_{OUT}, of each switch are listed in Table 6.2 and range from $1\,V_{OUT}$ up to $6\,V_{OUT} = 19.8\,V$. This maximum blocking voltage is just above half of the input voltage rating and only 1/11th of the DC output current is carried, demonstrating the reduced individual component ratings with respect to buck converters.

The converter IC has been implemented in an NXP 0.14 µm SOI BCD technology with the option of 3.3 V-IO devices as well as 20 V LDMOS devices with a 3.3 V gate oxide. Because the $Q_g R_{on}$ product of a cascade of two 3.3 V devices is lower than that of an LDMOS, S_{15} consists of two 3.3 V devices to achieve the required

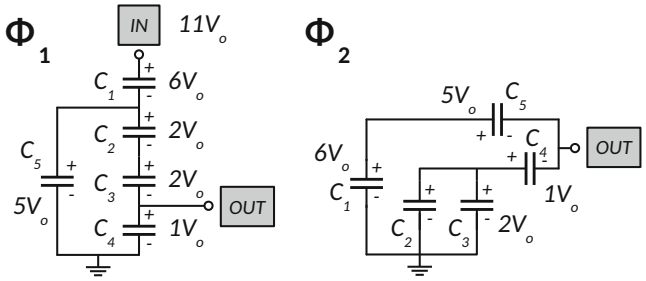

Fig. 6.3 Capacitor configuration of both phases in the 11/1 SC topology

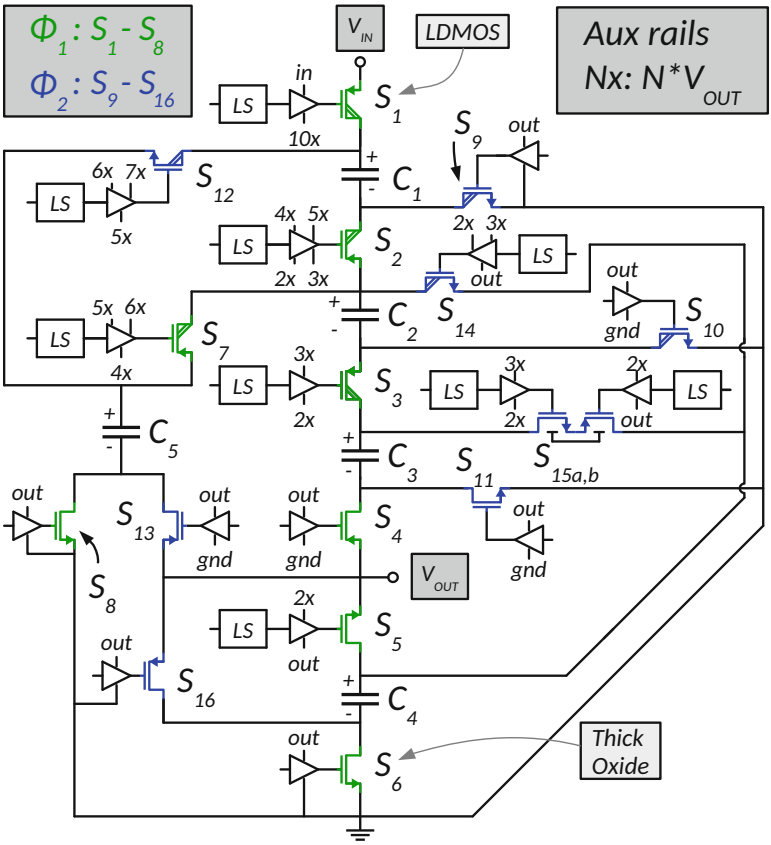

Fig. 6.4 Transistor-level converter implementation of the 11/1 SC topology, showing capacitors, switches, and driver details

Table 6.1 Topology-specific capacitor parameters: bias voltage, charge multiplier, and terminal potential per phase

C_i	$i =$	1		2		3		4		5	
$V_{Cfly,bias}$	[V_{OUT}]	6		2		2		1		5	
q_{Ci}	[$\frac{q_{OUT}}{11}$]	1		2		2		4		1	
C terminal		+	−	+	−	+	−	+	−	+	−
$V_{\Phi 1}$	[V_{OUT}]	11	5	5	3	3	1	1	0	5	0
V_{Φ_2}	[V_{OUT}]	6	0	2	0	2	0	2	1	6	1

blocking voltage of $2\,V_{OUT}$. Although S_2 and S_3 only need to block $2\,V_{OUT}$, they are implemented with an LDMOS for reliability, as drain and source terminals experience large potential variations during phase transitions. When the source potential of a switch is connected to a flying capacitor terminal, which changes with each topology phase reconfiguration, its corresponding driver must also be able to

Table 6.2 Topology-specific switch parameters: block voltage and charge multiplier

S_i	$i =$	1	2	3	4	5	6	7	8
$V_{block,i}$	[V_{OUT}]	5	2	2	1	1	1	4	1
q_{Si}	[$\frac{q_{OUT}}{11}$]	1	1	2	2	4	4	1	1
S_i	$i =$	9	10	11	12	13	14	15	16
$V_{block,i}$	[V_{OUT}]	5	3	1	6	1	4	2	1
q_{Si}	[$\frac{q_{OUT}}{11}$]	1	2	2	1	1	2	2	4

adapt accordingly. For $S_{7,12,14}$, the required drive swing remains limited to 2 V_{OUT}, but S_2 requires a 3-state drive signal with a 3 V_{OUT} swing, leading to a more complex driver needing multiple auxiliary supply rails. These necessary auxiliary supply rails are also shown in Fig. 6.4 in the schematic representation of each power-switch driver.

6.3.3 Power-Switch Driver Construction and Operation

Correct functionality of the SC converter requires proper power-switch drive signals, ensuring a strict non-overlapping of both capacitor configuration phases to prevent short-circuit paths. Due to the SC topology irregularity, discussed in Sect. 5.3, power-switch driver outputs with up to three states and a swing of up to 3 V_{OUT} can occur. This section discusses the driver requirements in detail, as well as a uniform technique to construct the necessary signals.

Since the source node of some switches is not connected to a DC-level voltage, but to a capacitor terminal that undergoes a potential variation when the capacitors in the topology are reconfigured during a phase transition, a three-state gate-drive signal is required to properly open and close a switch, and keep them as such. This is illustrated in Figs. 6.5 and 6.6. Figure 6.5 details the on-time, dead-time, and off-time of the switches, given the non-overlapping Φ_1 and Φ_2 signals. A switch that is part of the capacitor configuration of phase Φ_1 needs to close during $\Phi_{1,on}$ and needs gate potential $V\Phi_{1,on}$ to accomplish this. Then, in the subsequent dead-time in between $\Phi_{1,on}$ and $\Phi_{2,on}$, this switch needs a second gate potential $V\Phi_{1,dead}$ to open and ensure a strict non-overlapping activation of both SC topology phases. With the activation of the phase Φ_2 switches at the start of $\Phi_{2,on}$, the SC topology is reconfigured according to Fig. 6.3 and the absolute capacitor terminal potentials are changed. This causes the need for a third gate potential $V\Phi_{1,off}$ for the Φ_1 switches, with their source attached to such a capacitor terminal, in order to stay open during $\Phi_{2,on}$ and $\Phi_{2,dead}$. These three-gate potentials are represented by a gate potential coordinate in the form of ($V\Phi_{1,on}$ .. $V\Phi_{1,dead}$; $V\Phi_{1,off}$). For switch S_2, this equals (4 V_{OUT} .. 5 V_{OUT}; 2 V_{OUT}) as shown in Fig. 6.6 and requires a 3-state driver, handling a swing of 3 V_{OUT}. Figure 6.7 shows the S_2 driver to generate the desired

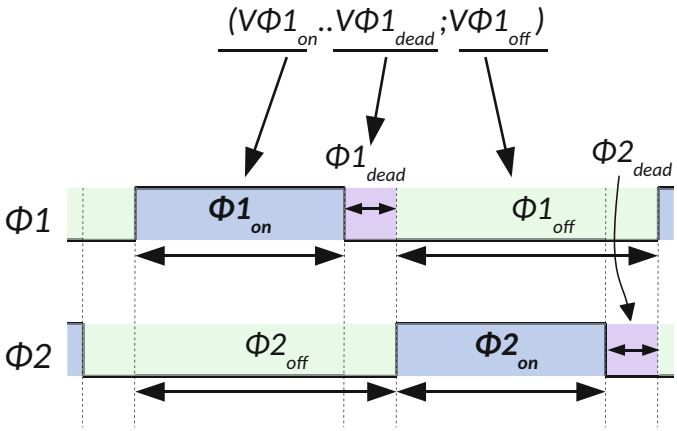

Fig. 6.5 Overview of the $\Phi_1 - \Phi_2$ clock pair and naming convention of the signals in this work

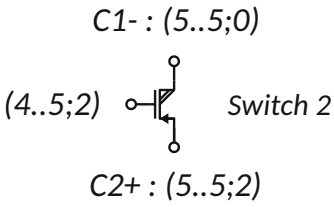

Fig. 6.6 Detailed information on the terminal potentials of switch S_2, denoted by potential coordinates

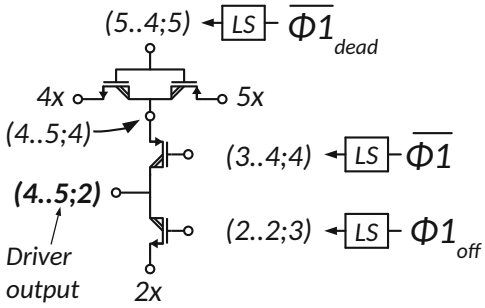

Fig. 6.7 Transistor-level implementation of the S_2 driver showing the (4..5; 2) output and additionally required auxiliary rails and input signals

output. Besides needing auxiliary DC supply rails $2xV_{OUT}$, $4xV_{OUT}$, and $5xV_{OUT}$, multiple input signals are necessary. However, these additional inputs have only two states and 1 V_{OUT} swing, which simplifies their construction to level-shifted versions of signals derived from the non-overlapping $\Phi_1 - \Phi_2$ pair. The level shifting is performed by capacitively coupled latches, shown in Fig. 6.8. Both the driver circuit and the capacitive level shifters require the auxiliary supply rails to function. Once these rails are available, this approach offers a uniform technique to generate all power-switch drive signals.

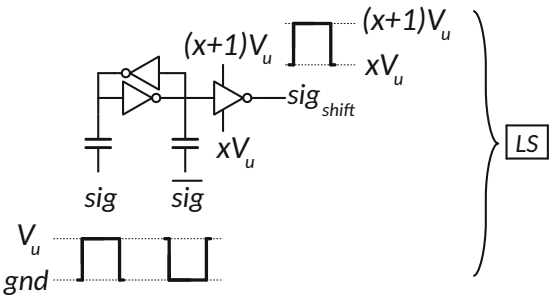

Fig. 6.8 Schematic representation of a dual-capacitor, capacitively coupled latch level shifter

6.3.4 Auxiliary Rail Generation

Section 6.3.3 confirms the necessity of the auxiliary rail generator in the proposed system to properly operate the main 11/1 converter and its drivers. Instead of adding an auxiliary DC–DC converter per additional rail [34, 43], a unified approach of generating all rails simultaneously is preferred since the required number of auxiliary rails is much higher in this converter. Moreover, stacking control voltage domains in series leads to a substantial charge recycling benefit[77, 78].

Figure 6.9 shows the Multiple-Input Multiple-Output auxiliary rail generator, generating all integer multiples of V_{OUT}. In contrast to a Single-Input Single-Output converter, where charge flows into the converter input terminal and out of the output terminal, each intermediate DC node of the MIMO rail generator is a terminal that allows for bidirectional charge flow in/out of the converter. Charge flows out of the converter if the terminal voltage level is below its steady-state value and vice versa. An 11/1 ladder topology is selected due to its high regularity, as discussed earlier in Sect. 5.3, and resulting simplicity to integrate monolithically. The converter uses 22 switches and 21 capacitors and is implemented with 2 fragments that are, instead of being time interleaved, switching in opposite phase to reduce noise on the intermediate rails. Switching a converter fragment in opposite phase reuses the already available control signals and results in a negligible implementation overhead. The active area of the ladder converter takes up 0.77 mm^2. This backbone of auxiliary supply rails now allows control signals to be transferred to any level with capacitive level shifters, enabling the uniform technique to construct drive signals, as proposed in Sect. 6.3.3.

Next to its primary function, the auxiliary rail generator is crucial to safely power up the system. The ladder converter operation continuously equalizes the voltage of its stages, causing all intermediate supply rails to simultaneously ramp up during start up with the total voltage over the converter V_{IN} shared equally over all internal voltage rails. In order to execute start up, the output voltage V_{OUT} is expected to be supplied to the converter output node by another means, such as a linear regulator. This initial voltage is then used to ramp up the intermediate supply rails, while the main converter is continuously switching to precharge the external flying capacitors to their steady-state bias voltage. While this booting process is taking place, the

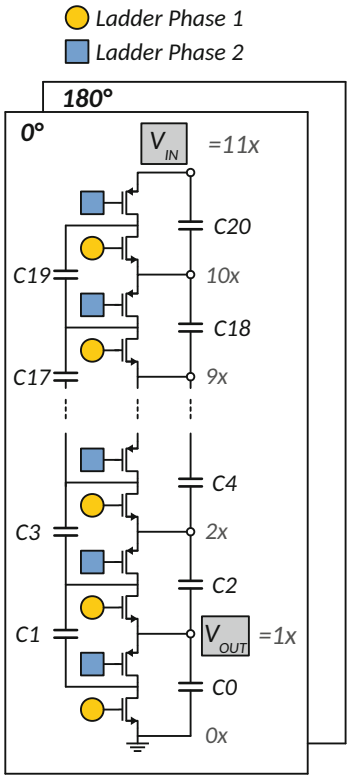

Fig. 6.9 Circuit schematic of the auxiliary MIMO ladder converter, consisting of 2 fragments in opposite phase

physical connection of the input source to the V_{IN} node can be made by either one of the following options depending on what behavior can be expected from the input source. If the source voltage needs to start up as well and ramps up to the nominal input voltage from 0 V, then it can simply be connected and fixed to the V_{IN} input node. Alternatively, if the source already is supplying its nominal voltage, a single high-voltage switch is required to disconnect the V_{IN} node from the input source until the converter booting process has completed and V_{IN} has reached a similar level to that of the input source.

When the input source turns off and its output turns high-impedance, the continued switching of the system will perform a safe ramp-down, similar to start up.

6.3.5 *Control System*

The system in this work contains two separate converters and each requires a suitable control approach. Since only the main 11/1 converter needs to provide a tightly regulated and low-noise output voltage, its control is of primary concern.

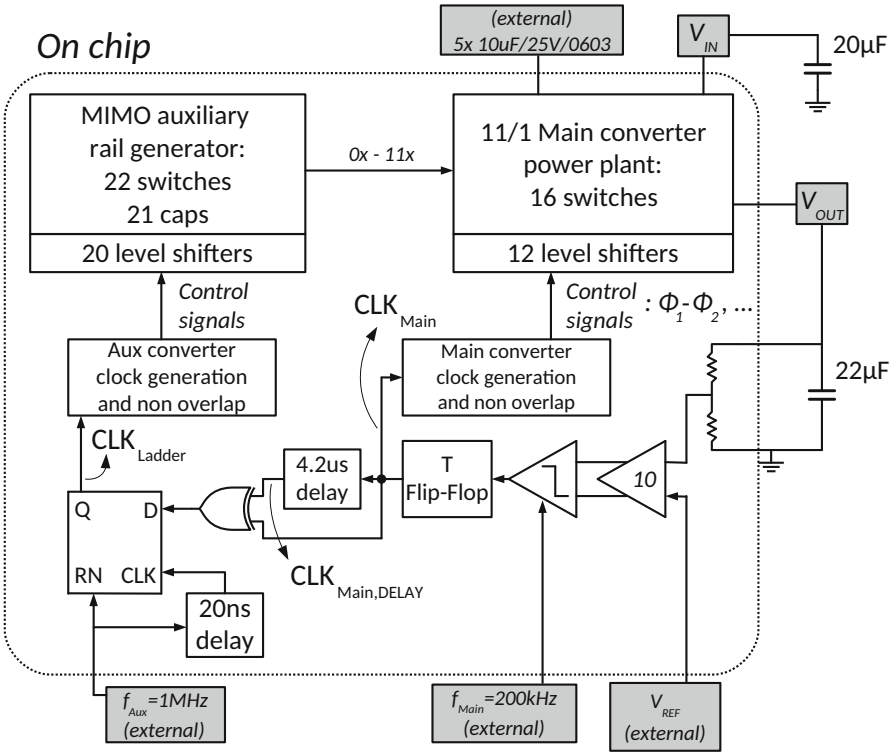

Fig. 6.10 System-architecture block diagram, showing details on the hysteretic control of the main converter and the synchronized open-loop control of the auxiliary ladder converter

The regulation and noise specification of the intermediate supply rails are much less stringent as they are only used internally. Figure 6.10 extends upon Fig. 6.2 and depicts the schematic implementation of the controllers.

Main Hysteretic Controller

A lower-bound hysteretic control approach is selected for the main converter as its digital nature offers excellent robustness and noise immunity [115] as well as fast Pulse-Frequency Modulation (PFM) [6, 7, 43]. Figure 6.10 shows the resistive divider, feeding back the divided version of the output voltage V_{OUT} to be compared with an external V_{REF}, representing the desired output voltage level. The comparator is clocked at 200 kHz and is succeeded by a Toggle Flip Flop to select only rising-edge transitions and generate the PFM control signal. Due to the frequency halving of the T-Flip Flop, CLK_{Main} is limited to a maximum frequency of 100 kHz. This operation frequency is the result of maximizing the converter efficiency, within the context of the targeted output power and the capacitance available in 0603

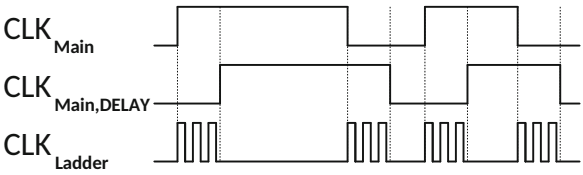

Fig. 6.11 Relevant waveforms to demonstrate the synchronization of CLK_{Ladder} to CLK_{Main}

ceramic SMD capacitors. CLK_{Main} is converted into a two-phase non-overlapping clock signal pair $\Phi_1 - \Phi_2$, and a few derivative signals in order to generate all required inputs to be buffered or level shifted into the drivers.

Auxiliary Controller

The auxiliary rail generator (ARG) does not require a very tight regulation of the intermediate supply rails and consequently its effort can be significantly reduced. In this work, the ARG is operated in open loop with a fixed switching frequency of 1 MHz. However, as the auxiliary rail generator only supplies power to the drivers and level shifters, which only consume power when the main converter goes through a phase transition, it is unnecessary for the ARG to keep equalizing the internal rails when they have already reached steady state. Therefore, in order to improve light-load efficiency, the fixed frequency clock signal of the ARG is only passed on during a window that is synchronized to the main converter switching frequency. As can be seen in Fig. 6.10, a 4.2 µs delay together with an exclusive-OR gate generates a window with equal length following each CLK_{Main} transition. A D-Flip Flop, to suppress glitches, passes along the fixed reference frequency during this time. Figure 6.11 shows the relevant waveforms to clarify the principle. This implementation allows flexibility during testing as both the delay and external reference frequency are configurable, but can be replaced with a counter and digital logic to achieve the same. The resulting CLK_{Ladder} signal is made into a non-overlapping clock signal to control the two-phase ladder ARG.

6.4 Chip Implementation and Measurements

The micrograph of the converter prototype, measuring 1.98 mm by 2.29 mm, is shown in Fig. 6.12. The main converter and its controller are located on the right-hand side, with the MIMO auxiliary rail generator to its left. The intermediate supply rails are clearly visible.

The topology-specific capacitor parameters, given in Table 6.1, show that capacitors C_1 and C_5, both having higher bias voltages, transfer less charge per cycle than $C_2 - C_4$. Nevertheless, identical 10 µF 25 V-rated 0603 ceramic capacitors are selected for the flying capacitor implementation. Selecting a capacitance larger than

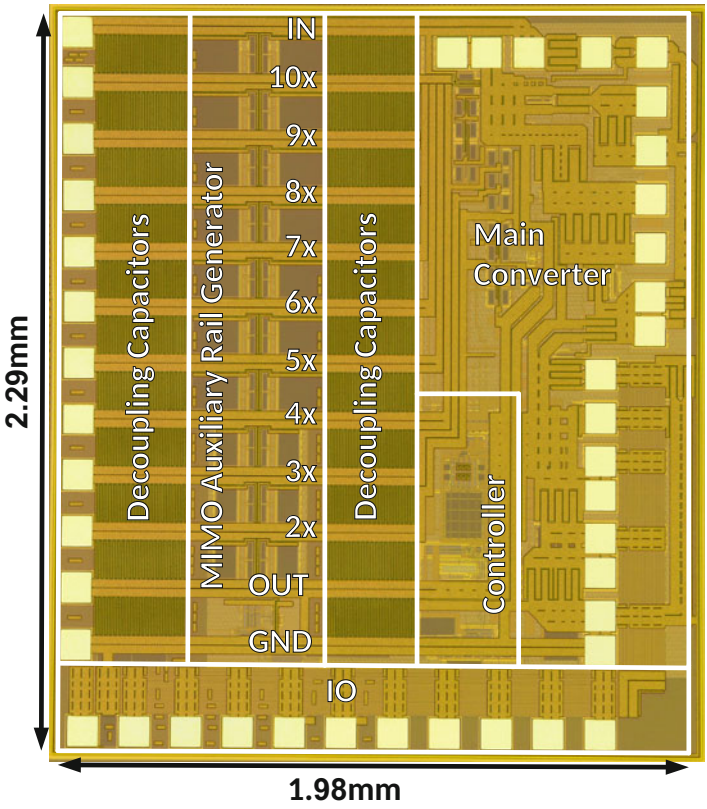

Fig. 6.12 Chip micrograph of the converter prototype, measuring 4.53 mm^2, indicating the location of the building blocks

necessary compensates for the capacitance reduction that is typical with ceramic capacitors under DC bias. This is demonstrated in Fig. 6.13 [66], showing the typical capacitance reduction of ceramic capacitors as function of their DC bias voltage. A substantial reduction from the initial value can be expected, from a 40 % decrease at only 3.3 V up to a 90 % reduction at 20 V. The choice of identical 10 µF 25 V-rated 0603 ceramic capacitors results in an actual capacitance value close to the optimal ratio, as indicated in Table 6.3.

Capacitor C_1 is the bottleneck in Table 6.3 as it is the largest actual capacitance that can be achieved in a 0603 SMD package with a 25 V rating, according to Fig. 6.13. The current overdimensioning of capacitors $C_2 - C_3$ and C_4 cannot be traded for less-overdimensioned SMD capacitors of a smaller 0402 package as the desired capacitance value at a 25 V rating is not available, and would lead to these components becoming the bottleneck. Alternately, the highest available capacitance rating is selected on purpose also for $C_2 - C_4$ within the 25 V-rated 0603 ceramic SMD capacitor series, because a higher capacitance rating yields a lower equivalent series resistance for a fixed package size.

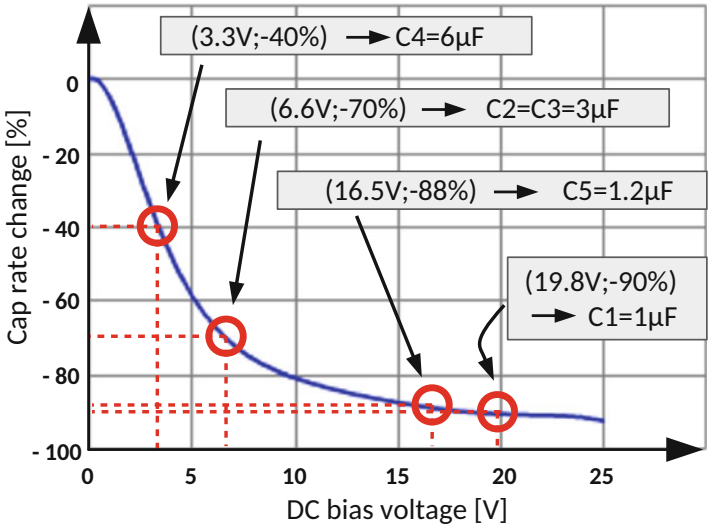

Fig. 6.13 Capacitance variation under DC bias of the 10 µF 25 V 0603 ceramic capacitor, used to implement the flying capacitors

Table 6.3 Ideal and actual achieved relative flying capacitance ratio

C_i $i=$	1	2	3	4	5
Ideal ratio w.r.t. unity	1	2	2	4	1
Actual ratio w.r.t. unity	1	3	3	6	1.2

6.4.1 Efficiency

A first performance validation is shown in Fig. 6.14. The output power P_{OUT} is varied from 0 mW up to a maximum load power of 140 mW, while the output voltage is tightly regulated to a DC level of 3.3 V with an output voltage ripple less than 5 % of V_{OUT}. Voltages have been measured without Kelvin contacts. The measurement has been repeated for multiple input voltages over a 1.6 V range. The lowest input voltage of 37.42 V represents the case with a maximum theoretical efficiency η_{max} of 97 %. The η_{max} indicates the maximum intrinsic efficiency of an SC converter when only the loss due to the output impedance is considered. η_{max} denotes the voltage division ratio of the voltage divider composed of R_{OUT} and R_{Load}, of which V_{OUT} is the output of the divider. It is thus a measure for the voltage lost over the output impedance R_{OUT}. With an output voltage V_{OUT} of 3.3 V and $\eta_{max} = 97\,\%$, the ideal output voltage of the converter, before R_{OUT}, is 3.3 V/0.97 = 3.402 V, and thus 102 mV is lost over the output impedance. The corresponding input voltage V_{IN} equals to 11 $V_{OUT,ideal}$ = 37.42 V. When the output voltage is desired to be fixed at 3.3 V and the input voltage V_{IN} is increased, a larger voltage drop over the output impedance will occur and consequently η_{max} is reduced. Input voltages 37.42 V up to 39.03 V correspond to η_{max} settings of 97 % down to 93 %.

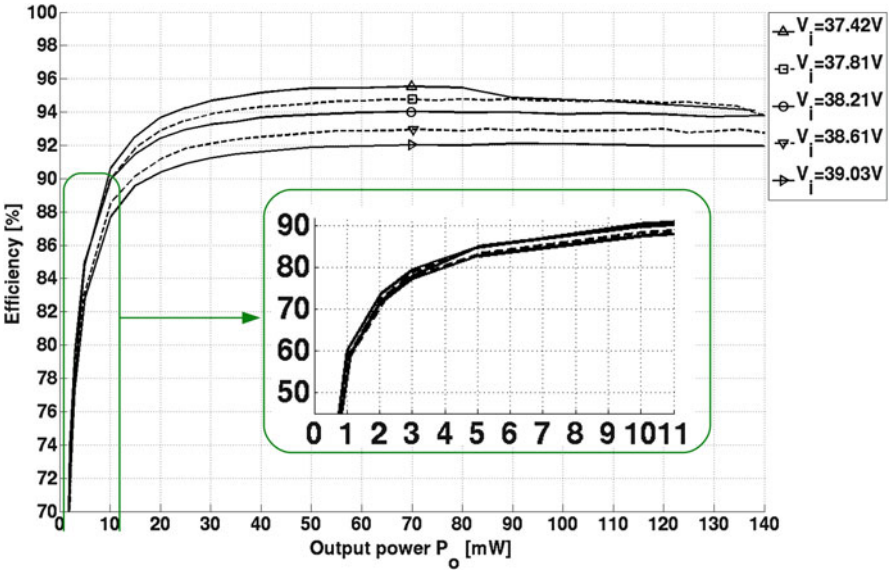

Fig. 6.14 Efficiency versus output power measurement for multiple input voltages, corresponding to a η_{max} setting of 97 % for $V_{IN} = 37.4$ V down to 93 % for $V_{IN} = 39$ V

For the measurement where η_{max} is set to 97 %, 3 % of the losses are intrinsic and the remaining extrinsic losses consist of a dynamic and a static contribution. The dynamic part is caused by the switching of the main converter switches and drivers, the loss as result of parasitic coupling of its capacitor terminals to other nodes, and the power consumed in the operation of the auxiliary rail generator. The static contribution is composed of the control circuitry power consumption. The maximum efficiency in this case is 95.5 % for an output power of 70 mW, indicating that only 1.5 % is lost because of the extrinsic losses. At higher input voltages, the output impedance is allowed to be larger and actual switching frequency can consequently be lower. Therefore, the dynamic contribution of the loss is lower than in the highest η_{max} setting and typically equals about 1 % in this converter for output power levels above 50 mW. As result, the measured efficiency is just 1 % below the η_{max} efficiency setting for a wide range of output power levels when η_{max} equals 96 % down to 93 %. The flatness of efficiency over output power variation confirms the PFM operation of the converter. As the output power is decreased, the switching losses reduce as well, resulting in a flat efficiency response. Thanks to PFM, both in the main as well as the auxiliary converter, and current reuse in the ladder auxiliary rail generator, a quiescent current of 22 µA is achieved, leading to light-load-efficient operation. This number does not yet include the power that is necessary to generate the frequency and voltage references that are provided externally in this prototype, as observed in Fig. 6.2. However, a low impact on the

efficiency is expected due to the low values of the reference frequencies and the nW-range power consumption reported in recent voltage references [26] as well as very accurate μW-range solutions [50].

Figure 6.14 also shows a steep efficiency curve for low power levels with respect to the maximum output power. At 1, 2, and 3 mW, efficiency surpasses 60, 70, and 80 %, respectively. Alternatively, this translates into an efficiency above 80 % for an output power in the wide range of 2.8 % up to 100 %$P_{OUT,max}$. From 20 %$P_{OUT,max}$ and upwards, the efficiency in Fig. 6.14 is observed to be at least 91 %.

6.4.2 *Load Regulation*

The lower-bound hysteretic controller's ability to regulate the output voltage is represented in Fig. 6.15. A worst-case scenario measurement has been performed to validate the controller to its full extent. This has been done by inducing a load step from the highest allowed output power condition toward a zero-load condition, and vice versa. Figure 6.15 shows how the converter prototype responds to a load step with a fall time of 300 ns from 140 to 0 mW. No overshoot is observed as the switching frequency is instantly decreased by a factor of nearly 2000 from its maximum switching frequency of 100 kHz to just 52 Hz. A 65 mV DC-shift is

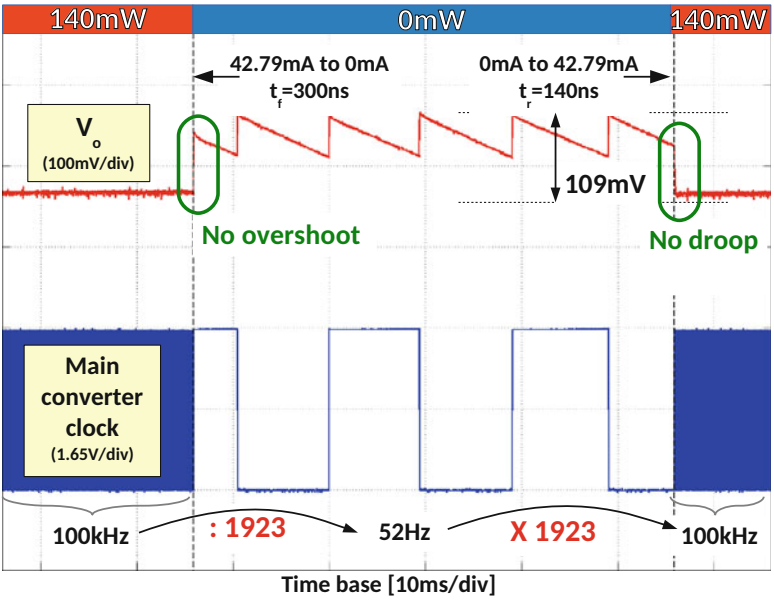

Fig. 6.15 Load transient response of full load steps, while $V_{IN} = 37.42$ V, demonstrating the instant switching frequency jumps that prevent both overshoot and undershoot

present as result of the difference between the loading conditions. Alternatively, it can be seen in Fig. 6.15 that a load increase of 0–140 mW with a rise time of 140 ns occurs without any droop. Consequently, the guard band in between the hysteretic lower bound and the minimal required system supply voltage is minimized. The combination of the 5 µs sampling period and a single 22 µF 0603 SMD ceramic capacitor suffices for the converter prototype to handle the worst-case load current step-up and step-down. Even though the minimal switching period of the converter is 10 µs, charge can be delivered to the output every 5 µs because the SC topology has two phases which both deliver charge to the output.

6.4.3 Line Regulation

Not only the output current can vary as result of an activity variation of the load. The input voltage is also subject to variation as it is the output of a preceding source, which has its own output regulation specifications and limitations thereof. The presented converter is able to maintain a regulated output voltage for any input voltage within the specified 1.6 V-range of 37.4–39 V. This has been validated with a measurement, again, of the worst-case condition.

Figure 6.16 demonstrates a DC-level input voltage step of 1.6 V with rise and fall times of 380 and 350 µs, respectively. The measurement has been performed while delivering 100 mW at 3.3 V. As the input voltage is increased, for fixed output voltage and current, the voltage drop over the output impedance of the converter is required to be larger. Given a fixed load current, the output impedance thus increases, which is achieved by operating the converter at lower switching frequency. This behavior is confirmed by Fig. 6.16 where it can be seen that when the input voltage is increased, the switching frequency inversely tracks this variation at the input. The change in switching frequency is more clearly visible in the output voltage ripple amplitude as lower switching frequency leads to a larger ripple.

Secondly, to demonstrate the presented converter can be used as second stage in a two-stage mains AC–DC system, an example AC–DC converter, shown in Fig. 6.17, has been built in order to generate a more realistic input supply voltage variation. Figure 6.18 indicates the response of the converter prototype to the input voltage variation coming from the AC–DC output. The converter maintains a regulated 3.3 V output under a 100 mW load, while the input voltage is subject to a 100 Hz variation of 472 mV. The switching frequency tracking of the input voltage variation can again be observed, both in the main converter clock signal as well as in the output voltage ripple amplitude.

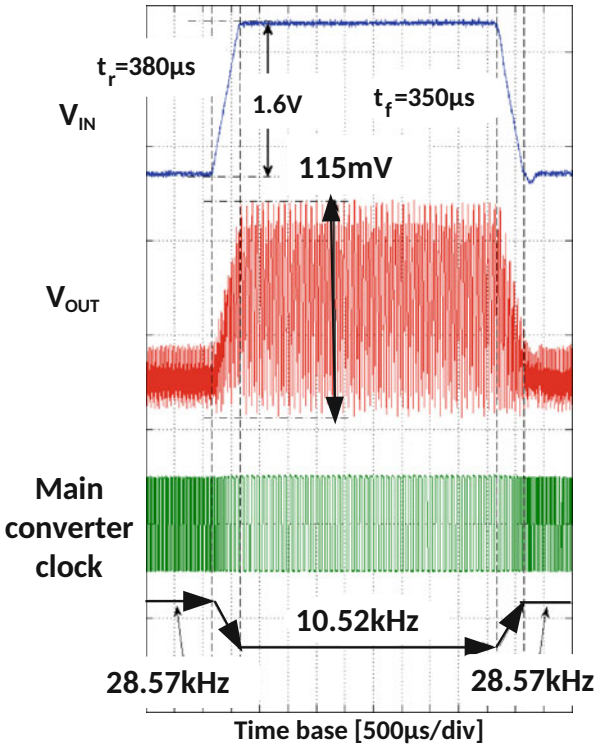

Fig. 6.16 Line-regulation response when the input is subject to a 1.6 V step-wise line variation, while supplying 100 mW

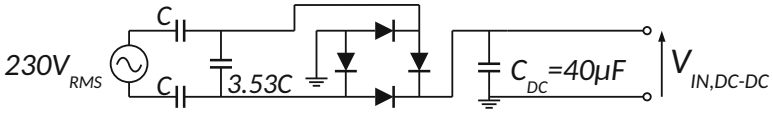

Fig. 6.17 Example implementation of a primary stage AC–DC converter to test the converter prototype with a realistic input

6.4.4 Comparison

Finally, a comparison of this work to the state of the art is plotted in Fig. 6.19 and Table 6.4. Although the switched-inductor competitors are able to handle a very large voltage conversion ratio range, Fig. 6.19 confirms the trend of their decreased efficiency toward larger voltage conversion ratios, as result of the duty-cycle asymmetry and the short on-time of the high-side switch. The proposed SC DC–DC converter topology is not affected by this issue, but is only specified to function in a smaller VCR range, and reaches very high efficiency at its intended operation point.

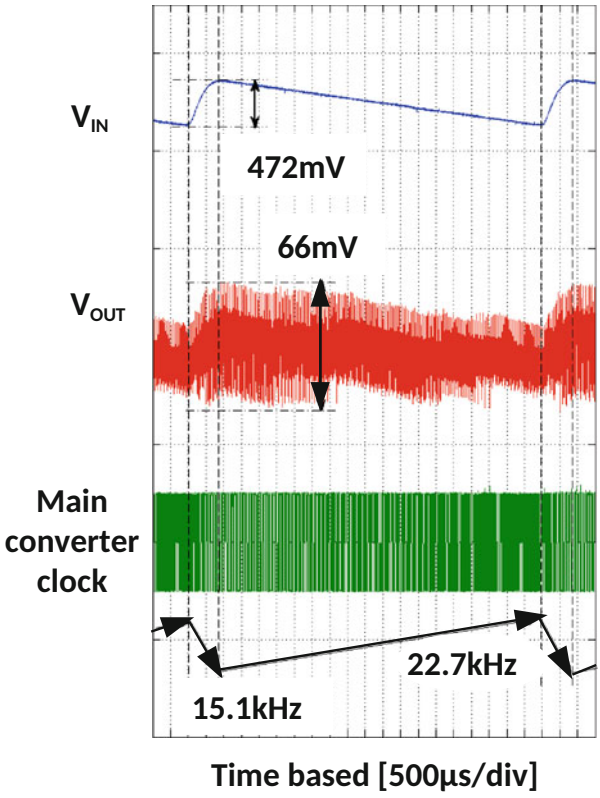

Fig. 6.18 Line-regulation response when the input is delivered by the example AC–DC stage, of Fig. 6.17, while supplying 100 mW

Table 6.4 lists a more-detailed comparison of this work to the switched-inductive converters of Fig. 6.19. All listed converters have comparable input voltage and output voltage and current specifications. Next to a higher peak efficiency, the comparison shows a significant advantage of the presented approach at light-load conditions. Moreover, despite the need for more external components, the form factor of our solution is smaller, thinner, and lighter than their switched-inductor alternatives.

6.5 Conclusion

A switched-capacitor DC–DC converter has been demonstrated to be an excellent candidate to perform a high step-down VCR of 11/1, while attaining high efficiency above 91 % over a broad output power range and interfacing high voltages in

Table 6.4 Performance summary and comparison of this work to the state of the art

	TPS54062	LTC3632	ISL85412	MAX17551	This work
Reference	[108]	[48]	[29]	[55]	[62]
V_{IN} (V)	40	36	36	36	37.42
V_{OUT} (V)	3.3	3.3	3.3	3.3	3.3
$I_{OUT,max}$ (mA)	46	20	150	50	42.2
C_{IN} (µF)	2.2	4.7	20	1	20
C_{OUT} (µF)	22	100	22	10	22
$I_{quiescent}$ (µA)	89	125	50	18.5	20
η_{peak} (%)	78.4	81	77	83	95.5
$\eta > 80\,\%$ @ *power range* ($\%P_{OUT,max}$)	n.a.	35–100	n.a.	50–100	2.8–100
η @ $20\,\%P_{OUT,max}$ (%)	55	78	64 (PFM)	76.4 (PFM)	91
Energy transfer	*Inductive*	*Inductive*	*Inductive*	*Inductive*	*Capacitive:* 5 × 0603
Component area[a] (mm^2)	46.2	36	23	23	5 × 1.28 = 6.4
Component volume[a] (mm^3)	106.4	126	66.8	66.8	5 × 1.024 = 5.1
Component mass[a] (mg)	4000	480	244	244	5 × 9.1 = 45.5

[a]Recommended in specification sheet

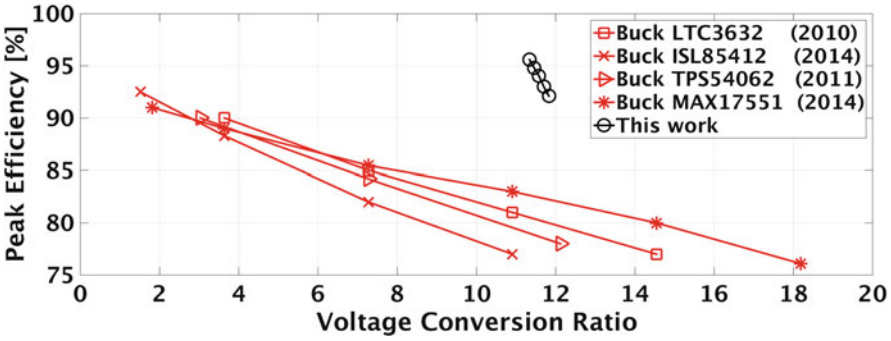

Fig. 6.19 Efficiency versus voltage conversion ratio comparison of this work to the state of the art

the 37.4 to 39 V range. The two-phase SC topology requires only 5 external 0603 ceramic flying capacitors, which is the theoretical minimum to achieve the 11/1 ratio. Even though this solution requires a larger number of discrete components with respect to switched-inductor converters, the final footprint is smaller. Moreover, the 50 %-duty-cycle SC approach can achieve beyond 91 %, and up to 95.5 %, conversion efficiency at high VCR values. This compares favorably to the efficiency of their inductive counterparts, which suffer from on-time limitation of the high-side switch as consequence of the duty-cycle asymmetry.

A fully integrated Multiple-Input Multiple-Output auxiliary rail generator concept is proposed as a single solution to simultaneously provide all intermediate auxiliary supply rails. This enables a uniform technique to reliably generate all necessary power-switch control signals, regardless of complexity.

The hysteretic control allows full load-step transient response without any undershoot or overshoot, with a single 22 µF 0603 output buffer capacitor. In addition, good line regulation with a realistic input from an example AC–DC conversion stage is shown. In comparison to state-of-the-art inductive converters with similar V_{IN}, V_{OUT}, and P_{OUT} specifications, this work achieves a higher efficiency, over a much broader load range (2.8–100 %) and in a smaller and lighter form factor.

Chapter 7
Monolithic SC DC–DC Toward Even Higher Voltage Conversion Ratios

7.1 Introduction

This chapter investigates the feasibility to achieve higher voltage conversion ratios in fully integrated DC–DC converter solutions. DC–DC conversion, however, is a very large playing field in the world of power electronics and the attention in the further discussion is focused on monolithically integrated DC–DC conversion. Consequently, the impact of CMOS process technology will be of paramount importance. Even when the scope is directed at high-ratio integrated DC–DC voltage conversion, as hinted toward by the chapter title, many implementation options still exist. To further identify the research region of interest, this chapter will study the switched-capacitor DC–DC approach.

The pursuit of a DC–DC converter that combines: (1) high-ratio voltage conversion, (2) monolithic integration, and (3) the switched-capacitor approach is of particular interest. In order to successfully realize the high-ratio voltage conversion, these three features facilitate, and also depend on, each other.

Figure 7.1 visualizes the synergy between the three earlier mentioned features. Arrow one indicates that high-ratio voltage conversion feature "benefits from" the switched-capacitor approach. This is proven by the prototype with a high-voltage conversion ratio in Chap. 6, where it was demonstrated that the switched-capacitor approach outperformed its inductive buck counterpart.

Arrow two represents the beneficial contribution of monolithic integration to the combination of a high-ratio switched-capacitor DC–DC converter. The required number of components increases along with the voltage conversion ratio [53], which can make discrete implementations infeasible due to the rising component count and the associated volume. With monolithic integration, the number of individual circuit components is no longer an issue.

H. Meyvaert, M. Steyaert, *High-Ratio Voltage Conversion in CMOS for Efficient Mains-Connected Standby*, Analog Circuits and Signal Processing,
DOI 10.1007/978-3-319-31207-1_7

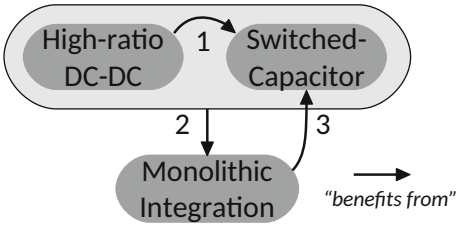

Fig. 7.1 Representation of the synergy between converter features

Finally, arrow three closes the circle and shows that monolithic integration benefits from the switched-capacitor approach as CMOS integrated capacitors generally, additional process steps not taken into account, showcase better quality factors than CMOS integrated inductors.

Coming back to the research question of how to achieve large voltage conversion ratios with an SC DC–DC converter in a monolithic solution, it is necessary to quantify the performance limits as function of the voltage conversion ratio. Consequently, the larger part of this chapter will revolve around this quantification. Next to the voltage conversion ratio, both the input and output voltage are necessary to fully determine the conversion. Clearly, a 10-to-1 V conversion will pose different implementation issues than a 100-to-10 V step-down conversion. Therefore, high-voltage conversion ratios do not necessarily lead to high voltages [83, 85], but mostly it does.

The outline of this chapter is shortly summarized. Section 7.2 creates additional background motivation for the research question and states this chapter's goal. Section 7.3 discusses the IC technology impact on DC–DC converters and, subsequently, introduces the key differentiating parameters necessary for comparison. Continuing, Sect. 7.4 uses these parameters to investigate and analyze popular switched-capacitor topologies. A note on the difference between theory and practice is discussed in Sect. 7.5. Here, the importance and influence of circuit techniques on practical prototypes are put in the spotlight. Validation by simulation is presented in Sect. 7.6, demonstrating performance and area-cost trade-offs with respect to the voltage conversion ratio. Final conclusions are listed in Sect. 7.7.

7.2 Motivation and Target

The ever-present voltage gap between a voltage source and a load requires DC–DC converters to efficiently bring source and load together. A typical voltage gap is present in hand-held systems which are battery operated. Lithium-ion batteries exhibit terminal voltages of 2.8–4.2 V while the circuit supply voltage is roughly 1 V. Alternatively, step-up conversion of the same voltage source can be required to generate the supply rail for a backlight LED driver. While the VCR of the former example remains low, the latter requires a higher VCR and deals with higher

voltages as well. Other examples that typically require even higher VCRs include LIDAR, Power over Ethernet, ultrasound transmitter drivers, piezo actuators, and drivers for MEMS applications.

Both an inductive as well as a capacitive approach is possible to implement the energy storage element, critical to a DC–DC converter's operation. Inductive DC–DC converters have the advantage over switched-capacitor DC–DC converters that they can implement a continuous VCR by means of Pulse-Width Modulation. But this also implies that the VCR is related to the PWM duty cycle and as such can become an issue toward high VCR. Even more so when taking into account that the switches in an inductive converter must be rated for the full input voltage, requiring high-voltage devices, which are more difficult to quickly turn on and off. This is in contrast to switched-capacitor DC–DC converters where the VCR is more determined by its topology, consisting of two specific capacitor configurations that are time-alternated in a two-phase operation scheme in order to perform voltage conversion. Thus duty cycle can be kept at 50 % regardless of the actual VCR. On top of that, single devices only need to block a fraction of the system rated voltage and current, leading to a better device utilization [90].

Another strength of SC converters is their suitability for monolithic integration as they only require components native to an integrated circuit (IC) technology: switches and capacitors. Hereby eliminating component count limitations which would otherwise obstruct implementation practicality and feasibility of non-fully integrated solutions.

Despite the previous motivations to select the switched-capacitor DC–DC approach for high conversion ratios and this upwards/downwards to/from high-voltage levels, they have not yet gained traction in this application field. The current state-of-the-art VCRs are limited to 8 [67–70] and many practical aspects that influence performance at high VCR are left unanswered. At this point, it must be noted that available step-up converters with a high ratio [117, 128] are not ideal comparison candidates, as these implementations rely on diodes. The use of diodes simplifies the functionality due to the absence of an otherwise required gate drive, but at the same time limits the circuit to step-up mode. This chapter aims to generalize and to discuss general bidirectional high-ratio converters, which rely on active switching to realize the switched-capacitor configurations. In addition, it is the goal of this chapter to investigate the combination of the aforementioned SC strengths into a monolithically integrated high-voltage-conversion-ratio switched-capacitor DC–DC converter. To that end, performance and cost trade-offs are analyzed for VCRs of a factor 10 and more by means of topology parameters and metrics. Different implementation options are compared and the best candidate to use in high-ratio and/or high-voltage applications is selected. Again, only monolithic solutions are considered in order to maximize cost effectiveness of the proposed solution, which has its consequences on the solution space due to technology limitations on the one hand but also possibilities on the other, related to the CMOS approach.

7.3 Impact of CMOS Integration and Topology Comparison Parameters

Fully integrating a switched-capacitor DC–DC converter can be an attractive step as external board space and components are omitted. However, also limitations arise from choosing the monolithic approach. A switched-capacitor DC–DC converter relies on capacitors to store energy in its electric field and switches to configure the capacitors into the physical topology configurations that result in a specific VCR, so the availability and specifications of these basic components are shortly summarized with respect to power conversion applications. Fortunately the nature of CMOS integration allows, within a set of process fabrication limits, a very flexible layout. This freedom is an advantage of the monolithic approach, enabling custom-designed structures, with customized component ratings, and overcoming component count limitations.

7.3.1 Integrated Capacitors

Capacitors can be integrated in CMOS in quite a few ways, each resulting in different specification parameters, of which the capacitor voltage rating $V_{C,rated}$ [V], capacitance density $C_{\square}$ [$\frac{\text{fF}}{\mu\text{m}^2}$], parasitic coupling ratio to the substrate $C_{par}/C_{netto} = \alpha$ [%], and the equivalent series resistance R_{esr} [Ω] are most crucial for application in DC–DC converters. Even though the equivalent series inductance L_{esl} [H] on its own is a property not to be omitted, the L_{esl} values of integrated capacitors are low enough that they can be neglected without consequence.

The capacitor voltage rating increases with the spacing of the capacitor plates, for a given dielectric, and therefore is inversely related to capacitance density for both planar and non-planar structures. Since α is the ratio of the parasitic substrate coupling capacitance to the net usable capacitance, it is inversely related to both the physical spacing of the capacitor structure to the substrate and to its capacitance density. Lastly, R_{esr} is set by the resistance of capacitor plates, which are heavily layout-dependent and thus a design parameter at the cost of capacitance density.

A more in-depth overview of different types of fully integrated capacitors is summarized:

Gate-Oxide Capacitors

Gate-oxide capacitors employ the planar thin or thick oxide, normally used for making transistors. Densities typically range from 3 $\frac{\text{fF}}{\mu\text{m}^2}$ to 10 $\frac{\text{fF}}{\mu\text{m}^2}$ depending on the actual oxide thickness. Consequently, these capacitor's voltage ratings coincide with the nominal voltage ratings for the thin- and thick-oxide transistors. The bottom plate is embedded in the substrate and thus subject to high substrate coupling, unless

a silicon-on-insulator process is used. Despite the relatively high substrate coupling, α can still be small if the capacitance density is high, i.e., thinner oxides. However, as gate oxides get thinner, they also become more susceptible to leakage current.

Metal-Insulator-Metal Capacitors

MIM capacitors are widely available non-standard planar structures, using a thin isolating layer with a higher dielectric constant than oxide to achieve very linear capacitors with capacitance densities typically in the range of 1.5 $\frac{\text{fF}}{\mu\text{m}^2}$ to 2.5 $\frac{\text{fF}}{\mu\text{m}^2}$. In some process technologies, it is possible get this type of capacitor in a double or triple stack. Their voltage rating $V_{C,rated}$ is about two to three times that of the gate-oxide capacitors, depending on the actual capacitor plate spacing d and the dielectric material used in the technology process. Due to their location higher up in the metal stack, they can exhibit a very low parasitic ratio α, especially if their capacitance density is doubled or tripled due to MIM capacitor stacking.

Metal-Oxide-Metal Capacitors

MOM capacitors are built within the regular metal-stack metals and possibly vias. These are typically arranged in a vertical parallel-plate structure to combine both the metal-to-metal and via-to-via parallel-plate capacitance along with metal-to-via fringing capacitance. The freedom in the spacing of the vertical plates allows for a custom-designed capacitor voltage rating, which is the most differentiating feature of this type of capacitor. Moreover, selecting the lowest level to be part of the structure allows the parasitic coupling ratio to be varied. Generally a low α can be achieved by not using all metals down to the lowest, but consequently at low capacitance densities in the range of 0.5 $\frac{\text{fF}}{\mu\text{m}^2}$ to 5 $\frac{\text{fF}}{\mu\text{m}^2}$ depending on actual number of used metals and the plate spacing.

Deep-Trench Capacitors

A non-standard limited-availability capacitor structure [5, 124] that is able to attain ultra-high capacitance densities of over 200 $\frac{\text{fF}}{\mu\text{m}^2}$, due to its vertical orientation, deeply rooted in the substrate. As such, despite being embedded in the substrate, α is virtually eliminated. Originating from embedded DRAM, these capacitors are typically optimized toward maximum capacitance density and a capacitor voltage rating high enough to reliably support embedded DRAM application, which does not need to be high.

Ferroelectric Capacitors

These capacitors are planar non-standard structures [21, 82], similar to the MIM capacitors, but much less common. The principle is similar, but a ferroelectric insulator material allows for a higher capacitance density with respect to the MIM capacitor.

Conclusions on Integrated Capacitors

Only three of the above types remain if only widely available integrated capacitor structures are considered: gate oxide (GO), metal-insulator-metal (MIM), and metal-oxide-metal (MOM) capacitors. At the same time compatibility to the majority of available CMOS processes is of paramount importance, except for niche segments, when the cost of processing comes into consideration. Therefore, it can be seen that low-loss, low-density capacitors with flexible high-voltage rating are available in the form of MOM capacitors. Alternatively, GO and MIM capacitors allow low-to-medium loss, higher-density capacitors but with a technology-fixed lower voltage rating.

7.3.2 Integrated Switches

Considering power conversion applications where switches are either fully OFF or ON, the $Q_{gate}R_{on}$ is a useful technology-specific figure of merit that demonstrates the required charge to reach a certain conductance in the ON state. In practice, a switch does not have to be composed of just a single device and it can in fact be a collection of components, which together form a "switch" with a voltage rating related to the collection of individual switch devices, as long as they are combined in a reliable way, so that no single device is subjected to overvoltage stress. This enables many switch implementation possibilities [49, 89].

The standard thin-oxide device, rated for the nominal technology supply voltage $V_{DD,nom}$ with the technology's minimal-feature-size gate length, together with a second type of Input–Output (IO) device with a thicker oxide and larger minimal gate length, to sustain higher voltages $V_{DD,IO}$, form the basic set of devices to implement a power converter. The $Q_{gate}R_{on}$ is lower for the thin-oxide devices, even if they need to be stacked in series to construct a new switch structure that can withstand higher voltages [96]. Switch stacking does come at the cost of a more complex gate-driver scheme in order to achieve reliability [92, 93], but, if properly designed, the added complexity translates into higher performance. A simple two-transistor self-biasing gate drive for the cascoded devices exists [8], but only increases the total blocking voltage with a part of the cascoded device's rated voltage, limiting the performance of this technique. Clearly, the large number of switch stacking combinations allows a lot of flexibility in custom designing

the blocking voltage. Other difficulties with extensive switch stacking include the reverse-breakdown voltage limit of the substrate-to-well junction and the need for auxiliary supply voltage rails to support the gate driver.

Laterally diffused metal-oxide semiconductor devices can block higher drain-source voltages and form an alternative if switch stacking is no longer an option, but require extra processing steps.

7.3.3 Topology Comparison Parameters

Metrics to evaluate the performance limits of SC DC–DC converters have been proposed in [91], and focus on comparing the contribution to R_{out} for a given switch V−A product and capacitor energy storage. These metrics offer an effective approach to compare idealized converter topologies and explore the fundamental limits toward a high-voltage conversion ratio. But the idealized character of the converter topologies does not capture the CMOS integrated context specifics, of which it is an absolute necessity to take them into consideration. Hence, this chapter tries to include the CMOS context into the comparison toward high-voltage conversion ratio.

An output impedance R_{out} model for SC converters is derived in [90], in which the converter output impedance is split up in two asymptotic limit approximations. Combining these approximations leads to a practical, user-friendly model, which is sufficiently accurate for initial calculations. A key feature is that the switched-capacitor topology, that is being modeled, is captured simply in a set of topology-specific parameters that describe capacitor utilization (k_c) and switch utilization (k_s). Since both influence the output impedance of the converter, these parameters are a measure for the utilization efficiency of the available capacitance and conductance. A low k_c leads to less required flying capacitance for a given R_{out} specification and consequently yields smaller parasitic coupling losses. Therefore, topologies with a low k_c vector, represented by a low K_c value, are preferential over others regarding parasitic coupling C_{par} and power density. The relation between K_c and k_c is given in Table 7.1. However, the total loss related to charging and discharging the parasitic coupling is given by Eq. (7.1), and is also a function of the parasitic capacitor voltage swing $V_{sw,par,i}$, squared.

$$E_{sw,i} = \alpha_i C_{fly,i} V_{sw,par,i}^2 \tag{7.1}$$

Consequently, another metric M_{sw}, introduced by Van Breussegem and Steyaert [114], is required to capture this influence. Metric M_{sw}, given in Eq. (7.2), quantifies the combined loss impact of each of the flying capacitor's parasitic substrate coupling.

$$M_{sw} = \sum_i k_{c,i} V_{sw,par,i}^2 \tag{7.2}$$

Table 7.1 Listing of topology-specific parameters as function of voltage conversion ratio N regarding capacitance utilization K_c and parasitic coupling metric M_{sw}, for the topologies under investigation in step-down

	Dickson Star	Series parallel	Fibonacci	Dickson Star embedded cascade	Doubler
1 Figure #	7.2a	7.2b	7.2c	7.2d	7.2e
# columns = k	$k = N - 1$	$k = N - 1$	$Fib_{k+2} = N$[a]	$k = \frac{N}{2} - 1$[b]	$k = 2log_2(N) - 1$
k_c	$[\frac{1}{N} \dots \frac{1}{N}]$	$[\frac{1}{N} \dots \frac{1}{N}]$	$[Fib_1 \dots Fib_k]$	$[\frac{1}{N} \dots \frac{1}{N}\ \frac{1}{4}\ \frac{1}{4}]$[b]	$[\frac{1}{2}\ \frac{1}{2^2}\ \frac{1}{2^2}\ \frac{1}{2^3}\ \frac{1}{2^3} \dots \frac{1}{2^N}\ \frac{1}{2^N}]$
$V_{C,rated,i}$ [V_{out}]	[1 2 3 ... N-1]	[1 ... 1]	$[Fib_2 \dots Fib_{k+1}]$	$[2\ 4\ 6 \dots (\frac{N}{2} - 1)\ 1\ 1]$[b]	$[1\ 2\ 2\ 4\ 4 \dots \frac{N}{2}\ \frac{N}{2}]$
$V_{sw,par,i}$ [V_{out}]	[1 ... 1]	[1 2 3 ... N-1]	$[Fib_1 \dots Fib_k]$	[2 ... 2 1 1][b]	$[1\ 2^1\ 0\ 2^2\ 0 \dots 2^{log_2(N)}\ 0]$
M_{sw}	$\frac{N-1}{N}$	$\frac{1}{N}\sum_{i=1}^{N-1} i^2$	$\frac{1}{N}\sum_{i=1}^{k}(Fib_i)^3$	$2.5 - \frac{4}{N}$	$\frac{1}{2} + \sum_{i=1}^{(log_2N)-1} 2^{i-1}$
$K_c = (\sum_{i=1}^{N} \lvert k_{c,i} \rvert)^2$	$(\frac{N-1}{N})^2$				$(\frac{1}{2} + \sum_{i=1}^{(log_2N)-1} 2^{-i})^2$
$K_c,\ N = \infty$	1				2.25
$M_{sw},\ N = 2$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$
$M_{sw},\ N = 4$	$\frac{3}{4}$	3.5	–	1.5	1.5
$M_{sw},\ N = 8$	$\frac{7}{8}$	17.5	4.62	2	3.5
$M_{sw},\ N = 16$	$\frac{15}{16}$	77.5	–	2.25	7.5
$M_{sw},\ N = 64$	$\frac{63}{64}$	1333.5	$N = 55 - 89$ $220.6 - 578$	2.375	31.5
$M_{sw},\ N = \infty$	1	∞	∞	2.5	∞

[a] $Fib_1 = 1, Fib_2 = 1$
[b] $N > 2$ and N even and $\frac{N}{2}$ even

The loss is quantified as function of the parasitic coupling voltage swing $V_{sw,par,i}$, inherent to two-phase topology reconfiguration, and is weighed by the utilization $k_{c,i}$ of that flying capacitor. The combination of these topology-specific metrics, K_c and M_{sw}, enables to compare topologies and to evaluate their performance prospects toward high VCR.

By selecting K_c and M_{sw} as main benchmarks for comparison, the switch-utilization efficiency is neglected. This is motivated by the fact that the capacitor is typically the bottleneck component, when integrating switched-capacitor DC–DC converters. The capacitance density of integrated capacitors heavily influences the realizable power density [5, 57, 121]. On top of that, M_{sw}-associated losses have a large impact on the system efficiency as C_{par} may be subject to very high-voltage swing [60, 114] and produce losses, as given by Eq. (7.3).

$$P_{dyn,C_{par}} = \sum_i \alpha_i C_{fly,i} V_{sw,par,i}^2 f_{sw} \tag{7.3}$$

7.4 Topology Comparison

Many options are possible to implement a certain VCR [33], e.g., a single topology or a cascade. Cascading topologies, however, are to be avoided due to increased losses as result of having the cascade of converter output impedances in series. Cascading a topology can often be avoided by embedding it directly into the original converter topology, but may require an extra capacitor to preserve correct functionality, as is the case in Fig. 7.2d.

Next to the motivation mentioned earlier, switch utilization is less important than capacitor utilization efficiency, in an integrated context, because the typical low capacitance density of an integrated capacitor leads to a much bigger impact on the total die area compared to that of switches. Therefore, Fig. 7.2 depicts topologies that are well known for their efficient capacitor usage, and consequently integration friendly. Both Fig. 7.2d and Fig. 7.2a show a 4:1 Dickson Star topology, but Fig. 7.2d demonstrates the possibility to embed an additional 2:1 ratio at, what would normally be, the output of the regular 4:1 Dickson Star topology. The advantage of the embedded approach is that the additional loss associated with converter cascading is avoided.

Table 7.1 lists the topology extracted parameters for comparison as function of voltage conversion ratio N. Vector k_c, and its condensed result K_c, shows the capacitor utilization efficiency. A low K_c indicates that a topology is capacitor efficient and more importantly it can be seen that as the VCR becomes infinity, K_c converges to a low finite value. Even though capacitor utilization efficiency in this case does not take any area cost as result of the capacitor voltage rating into account, a valid comparison of the required capacitance is obtained. For all compared topologies, except the Doubler, this is even the lowest value theoretically possible and thus ideally suited for monolithic integration.

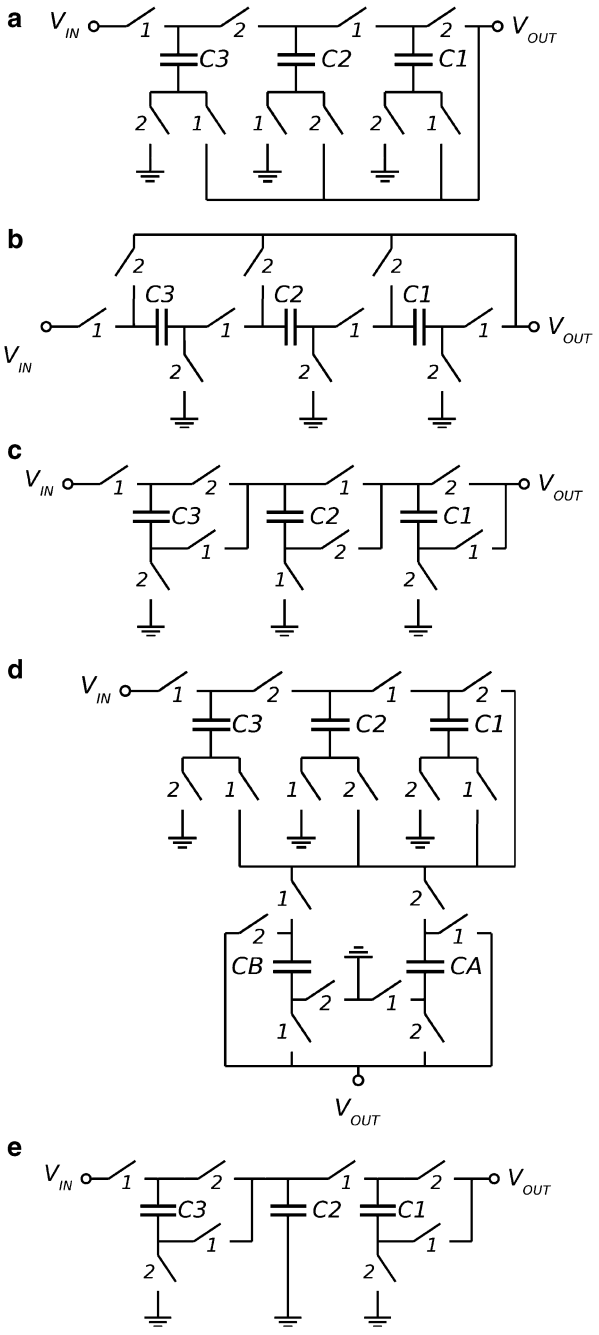

Fig. 7.2 Schematic representation of the topologies under comparison. (**a**) Dickson Star with ratio 4:1. (**b**) Series parallel with ratio 4:1. (**c**) Fibonacci with ratio 5:1. (**d**) Dickson Star embedded cascade with ratio 8:2:1. (**e**) Doubler with ratio 4:1

A more striking differentiation is shown by Table 7.1 in the parasitic swing metric M_{sw}. Topologies that structurally exhibit higher $V_{sw,par}$ values as the VCR increases suffer a lot since its associated losses are proportional to $V_{sw,par}^2$, as given by Eq. (7.1). Out of all compared topologies, the Dickson Star topology clearly outperforms all others, as its M_{sw} metric not only converges, but also does this to a very low finite value. On top of that, it is noted that this M_{sw} value for infinite VCR is only twice that of the theoretical minimum at N=2. The Dickson Star topology hereby nearly eliminates the negative influence of an increasing voltage conversion ratio on overall converter performance. Thereby minimizing the influence of the parasitic substrate coupling, inherent to the integrated circuit technology. Alternatively, IC technology is a good match for the incremental $V_{c,rated}$ rating requirement of the Dickson Star topology as layout freedom in MOM capacitors allows them to custom fit the voltage requirement.

7.5 The Difference Between Theory and Practice

A clear result from the previous section was obtained, demonstrating the low sensitivity of the loss associated with the parasitic capacitor-to-substrate coupling C_{par} to the voltage conversion ratio in the Dickson Star topology. This, where other topologies showed a stronger dependency. However, the proof of the pudding is in the eating and theory does not always coincide with practice.

The road from topology concept to a converter prototype can be winding if an appropriate driver concept for the, possibly large number of, power switches turns out to be complex. The energy cost of generating control signals, reliably level shift clock signals, properly drive power switches to a non-overlapping fashion at all times may amount up to a significant impact on the total efficiency. It is clear that the end-system prototype must meet its performance specifications and this means that in selecting the converter topology, the inclusion of these additional aspects must still allow the feasibility of the target performance. If this can no longer be achieved, it is required to select another topology.

On the other hand, circuit techniques can also reduce or mitigate topology shortcomings. Multi-phase time interleaving [100, 113] of the switched-capacitor converter enables to eliminate the need for an area-consuming dedicated decoupling capacitor. Connecting the MOS-capacitor in a particular fashion leads to a reduced parasitic capacitor coupling to the substrate [41, 56]. Charge recycling during the dead-time of the non-overlapping two-phase clock, from one parasitic capacitor to another, operated in opposite phase, decreases the resulting loss by a factor of two [4, 79]. The above techniques demonstrate that not all is lost when actually implementing a switched-capacitor DC–DC converter, and that these improvements can actually make a finished prototype perform better than estimated solely on a theoretical basis.

However, applying the previously mentioned techniques is not always possible or might require more energy overhead than benefit. When looking at the Dickson Star topology (Fig. 7.2a) in particular, it can be observed that all the parasitic capacitance

is connected to two physical nodes and always switched between the ground and the output potential, as it is located between the capacitor bottom plates and ground. Therefore, no additional level shifting is required to implement the charge recycling, allowing it to be a very simple performance boost. The only required overhead consists of the addition of a pass-gate and a clock signal indicating the dead-time. Since the parasitic capacitors of the other topologies in Fig. 7.2 are connected to more physical nodes and charged to different potentials, charge recycling is not as obvious as with the Dickson Star. Therefore, it can be concluded that the road to an implementation prototype for the Dickson Star is paved and is not expected to negatively impact performance, instead the performance expectations are increased.

7.6 Simulation Results for Dickson Star Topology

Section 7.4 demonstrated that the Dickson Star converter topology is the optimal choice for high-voltage conversion ratios in a monolithically integrated context. Simulations of such a topology are shown in Figs. 7.3 and 7.4. The efficiency of an optimized Dickson Star converter with parasitic reduction, i.e., charge recycling of the bottom-plate parasitic, and a VCR equal to 11 is shown in Fig. 7.3. The switching

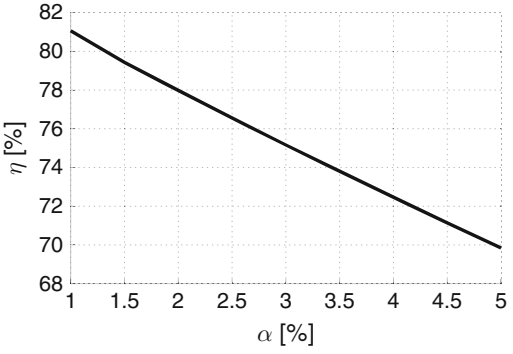

Fig. 7.3 Dickson Star topology with parasitic reduction at VCR=11, $f_{sw} =$ 10 MHz, $V_{in} = 41.7$ V, $V_{out} = 3.3$ V, $P_{out} = 40$ mW, and $C_{tot} = 2.9$ nF

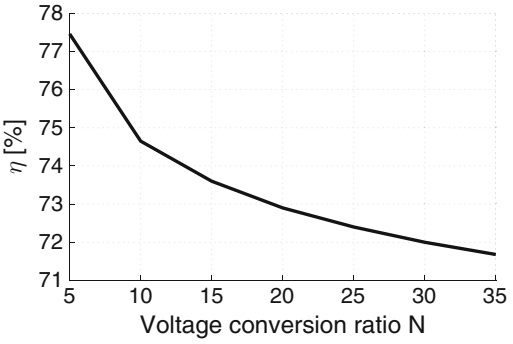

Fig. 7.4 Evolution of the converter efficiency with rising voltage conversion ratio, $f_{sw} = 10$ MHz, $\alpha =$ 3 %, $V_{out} = 2.5$ V, $P_{out} =$ 20 mW, and $C_{tot}/V_{in} =$ 1.94 nF/19 V for N=5 to 2.86 nF/100.5 V for N=35

frequency is 10 MHz and an output voltage/power of 3.3 V/40 mW is converted from a 41.7 V input. The graph shows the efficiency as function of realistic parasitic coupling ratio α values. It can be seen that a range of 4 % in α results in an efficiency decrease of 11 %, emphasizing the impact of the parasitic substrate coupling in a monolithic SC converter.

Figure 7.4 shows the simulated efficiency of a partially optimized converter as function of the voltage conversion ratio. It is optimized in the sense that the converter is implemented with two fragments in opposite phase, which enables to reduce the loss of the bottom-plate parasitic coupling by a factor of two, by shorting a charged and a discharged parasitic capacitor pair during the dead-time. As expected from Table 7.1, the efficiency tends to converge as loss contributions stabilize due to the convergence of both K_c and M_{sw}, while the VCR keeps increasing linearly. It is shown that an efficiency of above 70 % is achievable at very high-voltage conversion ratios, if an α of 3 % is reached. Designing capacitor structures to yield low parasitic coupling ratios will be a trade-off between low α and low die area, thus performance versus chip cost. Achieving low parasitic coupling is simplified in technologies such as silicon on insulator allowing higher performance per area, but at an increased base cost for the technology.

A final set of simulation results is given in Figs. 7.5, 7.6, 7.7, 7.8, showing the influence of the physical implementation consequences resulting from the flying capacitor voltage rating requirements. As the VCR increases, so do the capacitor voltage ratings of the flying capacitors related to the VCR increase. Once the average capacitor voltage rating increases beyond the fringe capacitor nominal rating, additional capacitor terminal spacing is required and both $\alpha_0 = 1.4\,\%$ and the average area density of C_{fly} are influenced, as can be seen in Figs. 7.5 and 7.6, respectively. Hereby, the efficiency of a typical Dickson Star converter with increasing VCR will not converge as in Fig. 7.4, but is shown in Fig. 7.7. Even though there is no actual convergence trend, good efficiency can be obtained at high VCR if α can be kept low. Figure 7.8 demonstrates the corresponding power density–VCR relation at $V_{out} = 1.8\,\text{V}$.

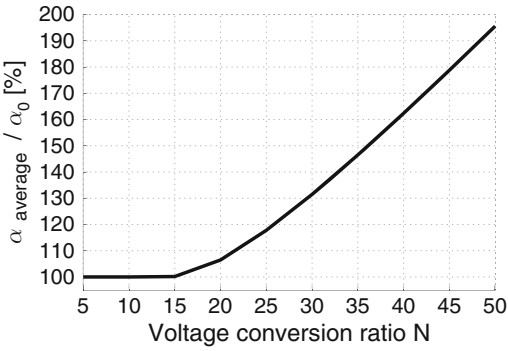

Fig. 7.5 $\alpha_{average}$, normalized to α_0, as function of the VCR for a Dickson Star topology, $f_{sw} = 15\,\text{MHz}$, $V_{out} = 1.8\,\text{V}$, and $P_{out} = 20\,\text{mW}$

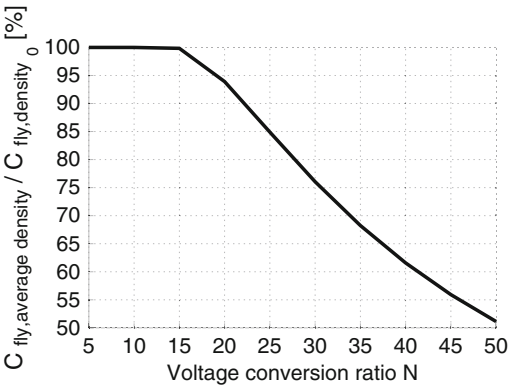

Fig. 7.6 $C_{fly,average\ density}$, normalized to $C_{fly,density_0}$, as function of the VCR for a Dickson Star topology, $f_{sw} = 15\,\text{MHz}$, $V_{out} = 1.8\,\text{V}$, and $P_{out} = 20\,\text{mW}$

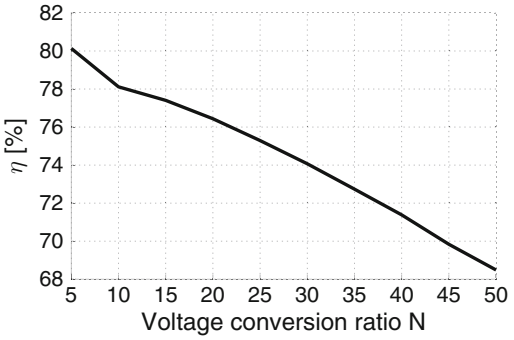

Fig. 7.7 η as function of the VCR for a Dickson Star topology, $f_{sw} = 15\,\text{MHz}$, $V_{out} = 1.8\,\text{V}$, and $P_{out} = 20\,\text{mW}$

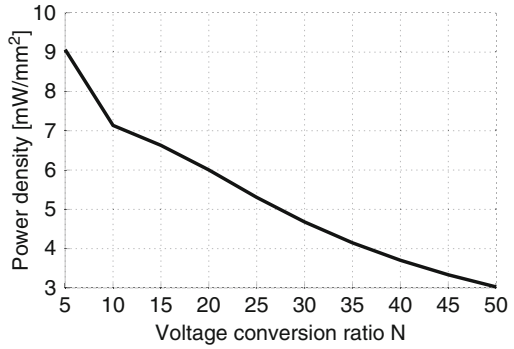

Fig. 7.8 Power density as function of the VCR for a Dickson Star topology, $f_{sw} = 15\,\text{MHz}$, $V_{out} = 1.8\,\text{V}$, and $P_{out} = 20\,\text{mW}$

7.7 Conclusions

This chapter introduces the research questions related to high-ratio DC–DC conversion in a monolithic context. After proposing, and motivating, the switched-capacitor approach as solution for this application, key parameters were introduced that enable to compare the benefits and drawbacks of topologies toward high-voltage conversion ratios. This was then applied to a set of topologies to investigate trends

and find a suitable candidate. This candidate was found in the form of the Dickson Star topology, which demonstrated to be superior to the other topologies, in an integrated context. This is mainly due to the convergence of both K_c and M_{sw} to very low values, when the VCR becomes large. Since the step from concept to practical implementation can yield issues that are not predicted by the theory, additional background on the consequences of circuit implementation was discussed. The expected performance was confirmed by simulation results and demonstrated the feasible realization of monolithic SC DC–DC converters with very high-voltage conversion ratios, while attaining attractive efficiency. Thus, it is confirmed that SC converters are indeed good candidates for high VCR applications, provided the feasibility to keep $\alpha_{average}$ low.

Chapter 8
Conclusions and Future Work

8.1 Overview and Conclusions

In the past, the trend to integrate power supplies has been driven mainly by the associated cost-reduction perspective. Indeed, pushing the operation frequency of switched-mode power supplies to higher frequencies has steadily reduced the cost and volume of the passive components. Once these values are small enough, it is possible to include them within the package (PSiP), or even on the chip (PSoC). This evolution is currently taking place.

But this is no longer the only motivation. New markets are appearing, posing new challenges in terms of power efficiency and other fields. Regardless of the buzzwords like Internet of Things or Internet of Everything, and which concepts and applications it eventually will implement, it is clear that the number of connected devices is seeing a strong growth and, more importantly, that the viability of this growth relies on successfully overcoming its main challenges: energy efficiency and security. As discussed in Chaps. 1 and 2, addressing the former challenge involves the combination of multiple circuit techniques to optimize system efficiency, which are gradually becoming less compatible with the traditional approach of a discrete, centralized, external power supply. Next to the cost-reduction perspective, integrating power management circuits is now becoming a necessity, in some cases, from the application point of view. To bring such advances into practice, this work has focused on the efficient implementation of monolithic switched-capacitor DC–DC converters, by analyzing the performance limitations in a CMOS context, and proposing techniques to reduce and overcome these challenges. In a CMOS switched-capacitor DC–DC converter, the impact of the flying capacitor bottom-plate parasitic is of paramount importance to the performance. Therefore, this effect has been modeled and exploited to implement a high power density SC DC–DC converter in CMOS.

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Besides energy efficiency improvements on a micro-scale in the field of on-chip power delivery, integrated power conversion is also a candidate to address the macro-scale challenge of reducing standby or vampire power. The discrepancy between the power level in active and standby mode renders it unlikely that a single power converter is highly efficient at both power levels. In case of the proposed solution approach, which introduces an auxiliary power supply to cover the standby power delivery, it is imperative that the overhead of an additional power converter is as low as possible. Both features, a low power level and a low overhead, in cost and volume, point toward integrated power conversion as a proper match. To this end, Chaps. 3 and 4 discuss the detailed realization of a monolithically integrated AC–DC converter that is able to deliver a μW-level output power. The interface of very high mains voltages in a CMOS process requires relying on passive components, in the metal stack, to contain a high voltage. Consequently, only low voltages are present in the active post-regulation circuit. The bottleneck of using passive components, to handle the high-voltage interface, is examined and a topology with optimized power throughput is demonstrated.

An alternative two-stage AC–DC approach is explored in Chaps. 5 and 6. Despite the relaxation of full integration to a hybrid implementation, to enable high efficiency operation in the mW-range, a significant effort is spent in keeping the overhead as low as possible. It is shown that a two-stage approach enables a larger flexibility to implement the challenge of a mains AC–DC conversion. Moreover, a two-stage system benefits from the synergy that both subsystems only need to perform a subset of the total functionality, which can be more efficient. Chapter 5 proposes to only perform a coarse step-down to a relatively high intermediate bus voltage in the primary AC–DC conversion step, as a larger set of functional requirements is likely to incur a larger energy penalty in this stage, due to the high-voltage components, than expected in the secondary. In order to combine high efficiency over a wide range and a high-ratio voltage conversion from a high intermediary voltage, while performing fine output regulation, a new switched-capacitor DC–DC converter topology was introduced, implemented, and validated in Chap. 6. It is demonstrated that SC DC–DC converters are excellent candidates for high-ratio voltage conversion. This originates from the fact that the voltage conversion ratio is a topology-dependent parameter, unlike it is a consequence of the duty cycle in the traditional inductive buck converter. As such, the switched-capacitor DC–DC converter can maintain a 50 % duty cycle, whereas the buck converter cannot, at the penalty of having a fixed voltage conversion ratio.

The promise of switched-capacitor DC–DC converters toward high-ratio voltage conversion is further elaborated in Chap. 7. Within the scope of monolithic integration in CMOS, the fundamental limitation on performance, by the inevitable parasitic effects from Chap. 2, as function of voltage conversion ratio is explored. The effect of the flying capacitor bottom-plate parasitic is found to be a dominant loss contribution toward high ratios. Consequently, topologies in which the voltage swing of this parasitic coupling is limited are found to be superior toward high-ratio voltage conversion in a monolithic context. Hence, the star-configured Dickson converter topology is best suited for monolithic integration of high-voltage

conversion ratios, since the voltage swing is constrained to 1 V_{out}, regardless of the VCR. Consequently, it is a very differentiating result to find the worst-case penalty associated with this bottom-plate parasitic effect in the Dickson Star converter is only a factor of two higher at infinite VCR than its best-case value, at a VCR of two. In contrast, the impact of the parasitic capacitor voltage swing in other topologies quickly diverges to infinity.

8.2 Main Contributions

The following list summarizes the key contributions of this work.

- Modeling of the flying capacitor bottom-plate effect, which is known to be a substantial loss contribution in monolithic switched-capacitor converters. This work demonstrates the beneficial effect of applying this inevitable parasitic into a positive charge-transfer contribution, instead of a negative one. This is demonstrated in a bulk CMOS converter prototype to achieve a high power density realization. This work reported the highest output power, at the time, for an SC DC–DC converter.
- Analysis of the power throughput bottleneck in a capacitive AC–DC step-down mains interface. Moreover, a monolithic implementation, enabled by custom-designed high-voltage-rated passive components, is demonstrated in a 0.35 µm technology. This is the first demonstrator in CMOS that is able to interface an input voltage of up to 265 V_{RMS}.
- Application of the switched-capacitor DC–DC converter approach, instead of the inductive conversion approach, to perform high-ratio voltage conversion from a high-input voltage, with a custom-designed topology that requires the theoretical minimal number of external components. This work realizes a higher voltage step-down conversion ratio, from a higher input voltage than other state-of-the-art SC DC–DC converters. Moreover, this work beats the conversion efficiency of comparable inductive converters. Additional differentiation is obtained by demonstrating highly efficient operation down to very light loading conditions, a missing feature in the comparable inductive converters.
- Application of a Multiple-Input Multiple-Output monolithically integrated converter as an encompassing solution to generate all required auxiliary power supply rails, necessary for level shifting and driving of the power switches. Additionally, this converter enables safe start up and shut down.
- The exploration of switched-capacitor DC–DC conversion toward high-ratio voltage conversion in a CMOS context, establishing the superiority of the Dickson Star topology.

8.3 Future Work

Despite the increased level of attention from the research community, the following research questions are promising candidates to deliver disruptive results. As such, these topics might deserve more focus in the future.

8.3.1 Fundamental Concepts

The following fundamental concepts concern possible approaches to innovate in power conversion when focusing on, and only on, the converter perspective.

Hybrid Capacitor–Inductor Topologies

An incredible amount of effort has been spent into the development of switched-inductor DC–DC converters. Indeed, they combine many practical attractive aspects such as a very low number of components, a flexible voltage ratio conversion through Pulse-Width Modulation and a high reliability. More recently, interest in the switched-capacitor approach has picked up because this kind of DC–DC converters rely on capacitors, which can be more efficiently integrated into CMOS [103] and have a much higher volumetric energy density than inductors [86]. The latter property creates the expectation of a higher power conversion density. However, in order to achieve highly efficient operation, only a fraction of this energy can actually be utilized to the end of power transfer. This is a result of the charge sharing loss that occurs when charging a capacitor with another capacitor. The addition of an inductor can enable either resonant or a more current-source behavior, to reduce this loss. Even though the beneficial effects of hybrid capacitor–inductor topologies have been known for a long time [64], it is only recently that the research community has picked them back up for further examination. Combining (1) the switched-capacitor strengths, such as high-ratio voltage conversion, efficient device utilization, and high capacitor energy density, (2) the strengths of the switched-inductor approach, including a flexible voltage regulation, and (3) the synergy of both approaches, yielding soft charging or resonance, sounds promising indeed. Implementation paths to combine these strengths consist of the multilevel approach [36, 120], the soft-charging approach [45, 75], and the resonant switched-capacitor approach [35, 88]. Further research in these directions is bound to deliver interesting results.

3D Packaging

Switched-mode power converters transfer energy from input to output. In order to do so, they rely on a component to temporarily store the energy. This can either be a capacitor, which stores energy in an electric field, or an inductor, which turns to the magnetic field to store its energy. Regardless of scaling down their values, through continued increase of the switching frequency, they inevitably take up costly die area. This chip area can be spent more useful on the integration of active devices, which actually require the ability of ultra-deep submicron CMOS processes to realize tiny transistors. Therefore, it is more sensible to implement passive devices in process technologies, optimized for making such components. However, resistance, inductance, and capacitive coupling of the interconnect, from actives to passives on separate dies, can hardly be tolerated, as otherwise the operation frequency cannot match the high speed that CMOS technology enables voltage converters to attain. Consequently, innovation in the packaging is required to enable a close physical spacing of the active die(s) to the passive die(s). The successful realization of such a combination might even put the PSiP approach ahead of the PSoC approach. Efforts in this direction are ongoing with the combination of an active die and a separate die for the passives [10], or with the passive component in a custom additional metal stack on top of the regular active die [12]. Alternatively, a complete mm-scale sensor node is presented in [11], even though it comprises multiple stacked dies for the subsystems. These examples demonstrate the potential of thinking outside the plane and into the box.

Passive Component Technology

As already discussed above, the energy storage capability of the passive component is one of the key parameters to attaining high power conversion density. In this regard, advancing the state of the art in voltage conversion, despite utilizing the most advanced and even future circuit techniques, is largely dependent on technological advances in capacitor and inductor technology. Especially since there is a strong motivation to go toward 3D integration of power converters, there should be no argument not to use the most optimal technologies to implement passive components in this 3D stack. Recently introduced state-of-the-art technologies, such as micro-supercapacitors [22], are an example of thin, low-cost capacitor structures. Hence, application of these devices in actual power converters should prove to be highly rewarding.

8.3.2 Application Concepts

The following application concepts suggest to expand the optimization horizon to cover the full system, enabling a synergy in the interaction between power converter and its load.

Serializing Voltage Domains

A huge challenge in power delivery are high power loads at low voltage, resulting in a large current flow. This leads to significant constraints on the power grid impedance, as well as the power converter output impedance. Instead of placing load circuits more in parallel, they should be placed more in series [44, 98]. As such, lower supply currents are traded in for a higher voltage. When perfectly balanced, no power converter is even required at all. Of course, a power converter is necessary to balance the supply voltage levels, as a perfect symmetry in load current of a series-load approach is currently not allowed to be a requirement from the converter. Moreover, the converter is not allowed to require anything. But even in this non-ideal scenario, the DC–DC converter is only required to transfer less power, worst-case scenario, than in the all-parallel voltage domain approach [78, 97]. Therefore, this is a promising research concept. After all, the ultimate DC–DC converter is not needing the converter in the first place.

Energy-Aware Computing

Although a power converter, traditionally, is not allowed to put requirements on how and when the load circuit is allowed to consume power, this master–slave relation between load and power converter should be revisited, as tradition is not a good argument when doing circuit design. Providing the power converter with ahead-of-time information on future energy consumption of upcoming executions, even in the most rudimentary on–off sense, could drastically improve energy efficiency on a system level. Moreover, awareness of the energy consumption within the computing unit and flexible allocation of executions to hardware in a series-voltage-domain approach might even virtually eliminate any imbalance of the load current [74]. Since part of such useful information is readily available in digital circuits, there should be no reason why not to distribute this also to the power converter. Also in other cases it is clear that information sharing between the load circuit and the power converter proves to be very beneficial. For example, this information can be used to reduce design margins when coping for effects such as process variation, temperature variation, and aging [16]. Therefore, it is time to consider the power converter as an integral part of the circuit, and no longer as a trivial DC voltage input to it.

Dense Energy Storage in Self-Reliant Harvesting Devices

Devices that, as consequence of their deployment in space, need to be self-reliant typically harvest incident power. This energy is stored on a capacitor, which acts as an energy buffer. Once the buffer is full, an action can be taken that consumes the stored energy. This action, that a deployed device is able to take, is limited by the energy storage capability, and as such, the combination of the buffer capacitance value and the square of the storage voltage. Consequently, it is in the general interest that the storage voltage is as high as possibly allowed by the capacitor rating to maximize the energy storage capability. Alternatively, for a fixed target action, the required capacitance value can be smaller, possibly enabling monolithic integration and an associated reduction of the system volume. At present, this maximal storage voltage is not a common design target, as even the minimally required voltage conversion is not an evident task. In case of RF radiation, the initial harvested voltage is very low, typically below the transistor threshold voltage, and passive AC–DC voltage multipliers are used to generate voltages of about 1 to 1.8 V. When more of these multiplying stages are cascaded, the mismatch of the output impedance of the harvesting antenna and the input impedance of the AC–DC multiplier increases. Consequently, the passive multiplication process is not a viable approach to go to a higher storage voltage. This is where active DC–DC conversion can make the difference. By decoupling the target storage voltage from the initial AC–DC multiplier, new degrees of freedom are enabled to realize a more efficient system from the top-level point of view. Of course, active step-up also creates the need for active step-down, but since switched-capacitor DC–DC converters work bidirectionally, this is a promising use-case scenario.

Appendix A
Topology Survey Data

Due to the in-depth extraction of topology-specific data, representation of these results becomes lengthy. For this reason, the results are listed in this appendix, instead of impeding the readability of the manuscript (Figs. A.1, A.2, A.3, A.4, A.5, A.6, A.7, A.8, A.9, A.10, and A.11 and Tables A.1, A.2, A.3, A.4, A.5, A.6, A.7, A.8, A.9, A.10, A.11).

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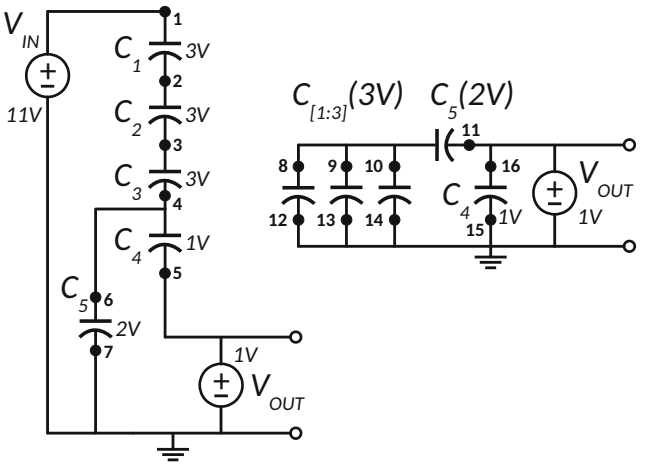

Fig. A.1 11 to 1 step-down switched-capacitor DC–DC topology with capacitor bias voltages 33321

Table A.1 11:1_33321 topology-specific capacitor and switch parameters: bias voltage, charge multiplier, blocking voltage, and gate voltage swing

C_i	$i =$	1	2	3	4	5
$V_{Cfly,bias}$	[V_{OUT}]	3	3	3	1	2
q_{Ci}	[$\frac{q_{OUT}}{11}$]	1	1	1	4	3

S_i	$i =$	1	2	3	4	5	6	7
$V_{block,i}$	[V_{OUT}]	8	3	3	1	1	2	1
q_{Si}	[$\frac{q_{OUT}}{11}$]	1	1	1	1	4	3	3
$V_{gate,sw,i}$	[V_{OUT}]	1	5	2	1	1	2	1

S_i	$i =$	8	9	10	11	12	13	14	15	16
$V_{block,i}$	[V_{OUT}]	9	6	3	1	8	6	3	1	1
q_{Si}	[$\frac{q_{OUT}}{11}$]	1	1	1	3	1	1	1	4	4
$V_{gate,sw,i}$	[V_{OUT}]	2	2	2	1	1	1	1	1	1

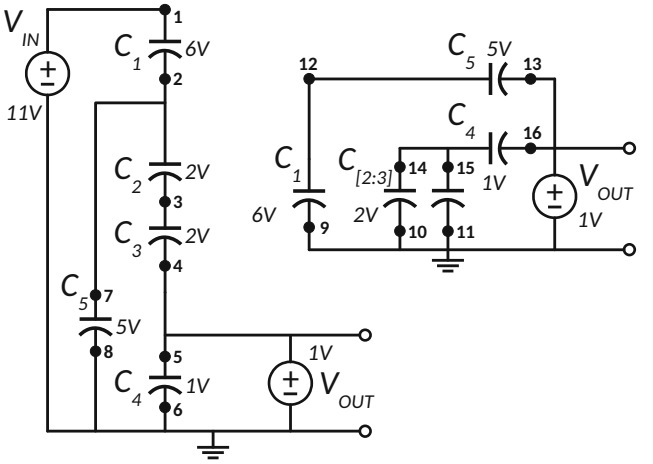

Fig. A.2 11 to 1 step-down switched-capacitor DC–DC topology with capacitor bias voltages 65221

Table A.2 11:1_65221 topology-specific capacitor and switch parameters: bias voltage, charge multiplier, blocking voltage, and gate voltage swing

C_i	$i =$	1	2	3	4	5
$V_{Cfly,bias}$	$[V_{OUT}]$	6	2	2	1	5
q_{Ci}	$[\frac{q_{OUT}}{11}]$	1	2	2	4	1

S_i	$i =$	1	2	3	4	5	6	7	8
$V_{block,i}$	$[V_{OUT}]$	5	2	2	1	1	1	4	1
q_{Si}	$[\frac{q_{OUT}}{11}]$	1	1	2	2	4	4	1	1
$V_{gate,sw,i}$	$[V_{OUT}]$	1	3	1	1	1	1	2	1
S_i	$i =$	9	10	11	12	13	14	15	16
$V_{block,i}$	$[V_{OUT}]$	5	3	1	6	1	4	2	1
q_{Si}	$[\frac{q_{OUT}}{11}]$	1	2	2	1	1	2	2	4
$V_{gate,sw,i}$	$[V_{OUT}]$	1	1	1	2	1	2	2	1

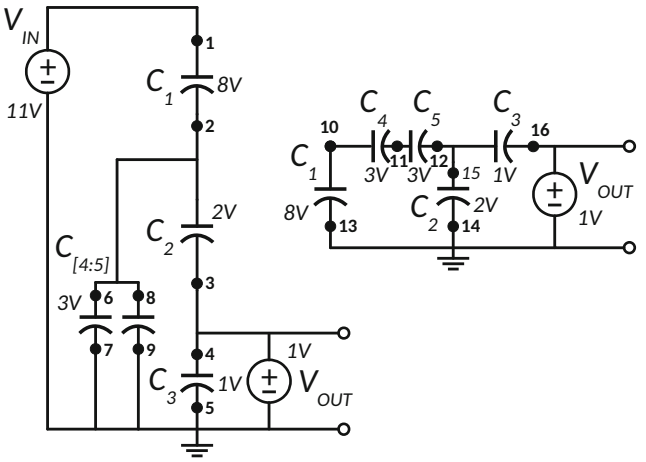

Fig. A.3 11 to 1 step-down switched-capacitor DC–DC topology with capacitor bias voltages 83321

Table A.3 11:1_44321 topology-specific capacitor and switch parameters: bias voltage, charge multiplier, blocking voltage, and gate voltage swing

C_i	$i =$	1	2	3	4	5
$V_{Cfly,bias}$	[V_{OUT}]	8	2	1	3	3
q_{Ci}	[$\frac{q_{OUT}}{11}$]	1	3	4	1	1

S_i	$i =$	1	2	3	4	5	6	7	8	9
$V_{block,i}$	[V_{OUT}]	5	2	1	1	1	6	5	3	2
q_{Si}	[$\frac{q_{OUT}}{11}$]	1	1	3	4	4	1	1	1	1
$V_{gate,sw,i}$	[V_{OUT}]	1	1	1	1	1	2	1	2	1

S_i	$i =$	10	11	12	13	14	15	16
$V_{block,i}$	[V_{OUT}]	8	3	3	3	1	2	1
q_{Si}	[$\frac{q_{OUT}}{11}$]	1	1	1	1	3	3	4
$V_{gate,sw,i}$	[V_{OUT}]	4	2	1	1	1	2	1

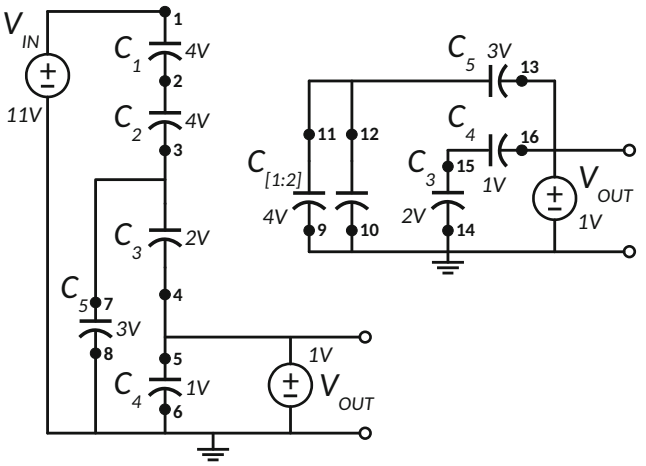

Fig. A.4 11 to 1 step-down switched-capacitor DC–DC topology with capacitor bias voltages 44321

Table A.4 11:1_44321 topology-specific capacitor and switch parameters: bias voltage, charge multiplier, blocking voltage, and gate voltage swing

C_i	$i =$	1	2	3	4	5
$V_{Cfly,bias}$	[V_{OUT}]	4	4	2	1	3
q_{Ci}	[$\frac{q_{OUT}}{11}$]	1	1	3	3	2

S_i	$i =$	1	2	3	4	5	6	7	8
$V_{block,i}$	[V_{OUT}]	8	3	2	1	1	1	2	1
q_{Si}	[$\frac{q_{OUT}}{11}$]	1	1	1	3	3	3	2	2
$V_{gate,sw,i}$	[V_{OUT}]	1	3	1	1	1	1	2	1
S_i	$i =$	9	10	11	12	13	14	15	16
$V_{block,i}$	[V_{OUT}]	7	3	8	4	1	1	2	1
q_{Si}	[$\frac{q_{OUT}}{11}$]	1	1	1	1	2	3	3	3
$V_{gate,sw,i}$	[V_{OUT}]	1	1	2	2	1	1	2	1

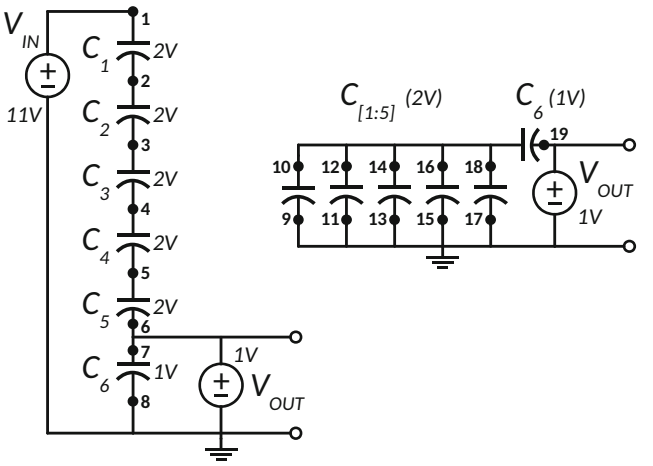

Fig. A.5 11 to 1 step-down switched-capacitor DC–DC topology with capacitor bias voltages 222221

Table A.5 11:1_222221 topology-specific capacitor and switch parameters: bias voltage, charge multiplier, blocking voltage, and gate voltage swing

C_i	$i =$	1	2	3	4	5	6
$V_{Cfly,bias}$	$[V_{OUT}]$	2	2	2	2	2	1
q_{Ci}	$[\frac{q_{OUT}}{11}]$	1	1	1	1	1	5

S_i	$i =$	1	2	3	4	5	6	7	8
$V_{block,i}$	$[V_{OUT}]$	9	2	2	2	2	1	1	1
q_{Si}	$[\frac{q_{OUT}}{11}]$	1	1	1	1	1	1	5	5
$V_{gate,sw,i}$	$[V_{OUT}]$	1	7	5	3	1	1	1	1

S_i	$i =$	9	10	11	12	13	14	15	16	17	18	19
$V_{block,i}$	$[V_{OUT}]$	9	10	7	8	5	6	3	4	1	2	1
q_{Si}	$[\frac{q_{OUT}}{11}]$	1	1	1	1	1	1	1	1	1	1	5
$V_{gate,sw,i}$	$[V_{OUT}]$	1	2	1	2	1	2	1	2	1	2	1

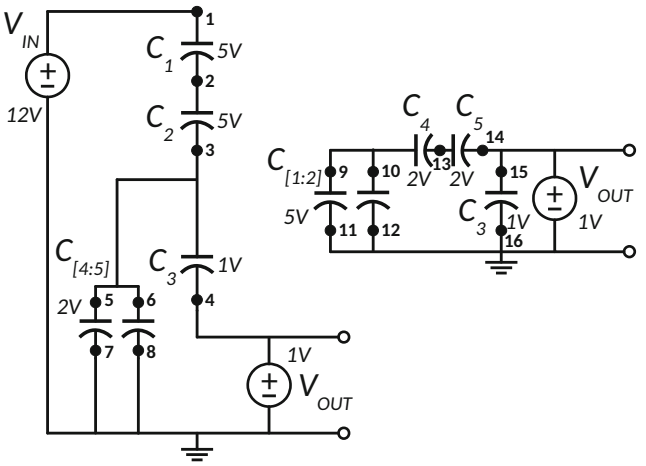

Fig. A.6 12 to 1 step-down switched-capacitor DC–DC topology with capacitor bias voltages 55221

Table A.6 12:1_55221 topology-specific capacitor and switch parameters: bias voltage, charge multiplier, blocking voltage, and gate voltage swing

C_i	$i =$	1	2	3	4	5
$V_{Cfly,bias}$	[V_{OUT}]	5	5	1	2	2
q_{Ci}	[$\frac{q_{OUT}}{12}$]	1	1	5	2	2

S_i	$i =$	1	2	3	4	5	6	7	8
$V_{block,i}$	[V_{OUT}]	7	5	1	1	4	2	3	1
q_{Si}	[$\frac{q_{OUT}}{12}$]	1	1	1	5	2	2	2	2
$V_{gate,sw,i}$	[V_{OUT}]	1	2	1	1	2	2	1	1
S_i	$i =$	9	10	11	12	13	14	15	16
$V_{block,i}$	[V_{OUT}]	10	5	7	2	2	1	1	1
q_{Si}	[$\frac{q_{OUT}}{12}$]	1	1	1	1	2	2	5	5
$V_{gate,sw,i}$	[V_{OUT}]	4	3	1	1	1	1	1	1

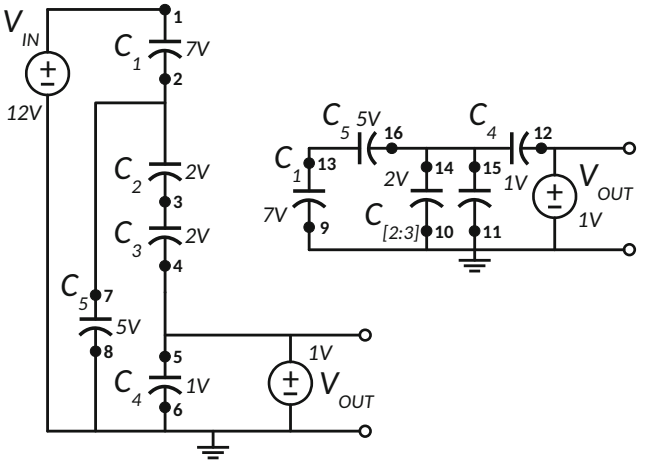

Fig. A.7 12 to 1 step-down switched-capacitor DC–DC topology with capacitor bias voltages 75221

Table A.7 12:1_75221 topology-specific capacitor and switch parameters: bias voltage, charge multiplier, blocking voltage, and gate voltage swing

C_i	$i =$	1	2	3	4	5
$V_{Cfly,bias}$	[V_{OUT}]	7	2	2	1	5
q_{Ci}	[$\frac{q_{OUT}}{12}$]	1	2	2	5	1

S_i	$i =$	1	2	3	4	5	6	7	8
$V_{block,i}$	[V_{OUT}]	7	2	2	1	1	1	7	2
q_{Si}	[$\frac{q_{OUT}}{12}$]	1	2	2	2	5	5	1	1
$V_{gate,sw,i}$	[V_{OUT}]	1	3	1	1	1	1	3	1
S_i	$i =$	9	10	11	12	13	14	15	16
$V_{block,i}$	[V_{OUT}]	5	3	1	1	7	5	3	2
q_{Si}	[$\frac{q_{OUT}}{12}$]	1	2	2	5	1	2	2	1
$V_{gate,sw,i}$	[V_{OUT}]	1	1	1	1	3	2	2	1

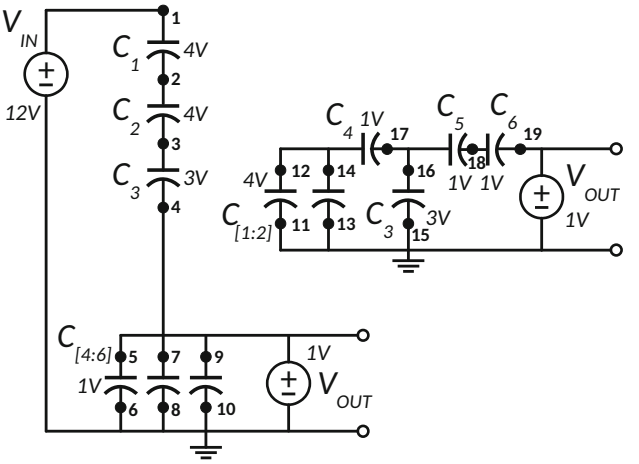

Fig. A.8 12 to 1 step-down switched-capacitor DC–DC topology with capacitor bias voltages 443111

Table A.8 12:1_443111 topology-specific capacitor and switch parameters: bias voltage, charge multiplier, blocking voltage, and gate voltage swing

C_i	$i =$	1	2	3	4	5	6
$V_{Cfly,bias}$	[V_{OUT}]	4	4	3	1	1	1
q_{Ci}	[$\frac{q_{OUT}}{12}$]	1	1	1	2	3	3

S_i	$i =$	1	2	3	4	5	6	7	8	9	10
$V_{block,i}$	[V_{OUT}]	8	4	3	1	3	3	2	2	1	1
q_{Si}	[$\frac{q_{OUT}}{12}$]	1	1	1	1	2	2	3	3	3	3
$V_{gate,sw,i}$	[V_{OUT}]	1	4	1	1	1	1	1	1	1	1

S_i	$i =$	11	12	13	14	15	16	17	18	19
$V_{block,i}$	[V_{OUT}]	8	11	4	7	1	4	4	1	1
q_{Si}	[$\frac{q_{OUT}}{12}$]	1	1	1	1	1	1	2	3	3
$V_{gate,sw,i}$	[V_{OUT}]	1	4	1	4	1	2	1	1	1

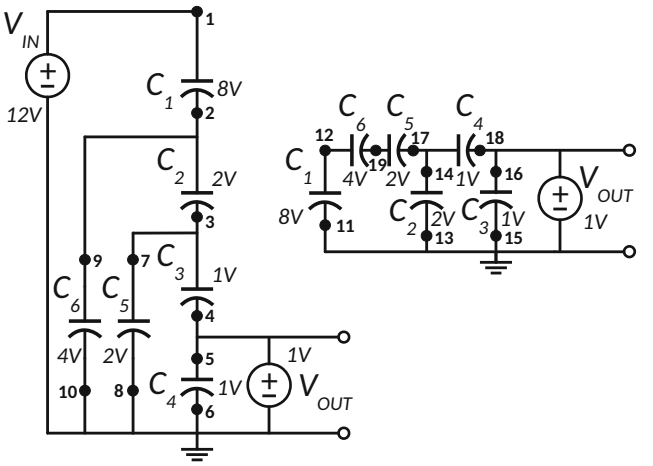

Fig. A.9 12 to 1 step-down switched-capacitor DC–DC topology with capacitor bias voltages 842211

Table A.9 12:1_842211 topology-specific capacitor and switch parameters: bias voltage, charge multiplier, blocking voltage, and gate voltage swing

C_i	$i =$	1	2	3	4	5	6
$V_{Cfly,bias}$	$[V_{OUT}]$	8	2	1	1	2	4
q_{Ci}	$[\frac{q_{OUT}}{12}]$	1	2	3	3	1	1

S_i	$i =$	1	2	3	4	5	6	7	8	9	10
$V_{block,i}$	$[V_{OUT}]$	4	2	1	1	1	1	8	2	8	4
q_{Si}	$[\frac{q_{OUT}}{12}]$	1	1	2	3	3	3	1	1	1	1
$V_{gate,sw,i}$	$[V_{OUT}]$	1	2	1	1	1	1	2	1	3	1
S_i	$i =$	11	12	13	14	15	16	17	18	19	
$V_{block,i}$	$[V_{OUT}]$	4	8	2	2	1	1	4	1	2	
q_{Si}	$[\frac{q_{OUT}}{12}]$	1	1	2	2	3	3	1	3	1	
$V_{gate,sw,i}$	$[V_{OUT}]$	1	5	1	2	1	1	1	1	2	

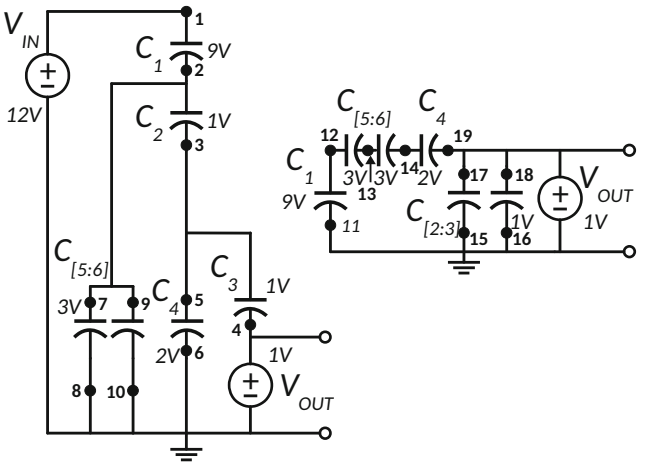

Fig. A.10 12 to 1 step-down switched-capacitor DC–DC topology with capacitor bias voltages 933211

Table A.10 12:1_933211 topology-specific capacitor and switch parameters: bias voltage, charge multiplier, blocking voltage, and gate voltage swing

C_i	$i =$	1	2	3	4	5	6
$V_{Cfly,bias}$	[V_{OUT}]	9	1	1	2	3	3
q_{Ci}	[$\frac{q_{OUT}}{12}$]	1	3	4	1	1	1

S_i	$i =$	1	2	3	4	5	6	7	8	9	10
$V_{block,i}$	[V_{OUT}]	3	1	1	1	2	1	9	6	5	3
q_{Si}	[$\frac{q_{OUT}}{12}$]	1	1	3	4	1	1	1	1	1	1
$V_{gate,sw,i}$	[V_{OUT}]	1	2	1	1	2	1	3	1	3	1

S_i	$i =$	11	12	13	14	15	16	17	18	19
$V_{block,i}$	[V_{OUT}]	3	9	3	2	2	1	2	1	1
q_{Si}	[$\frac{q_{OUT}}{12}$]	1	1	1	1	3	4	3	4	1
$V_{gate,sw,i}$	[V_{OUT}]	1	4	3	1	1	1	1	1	1

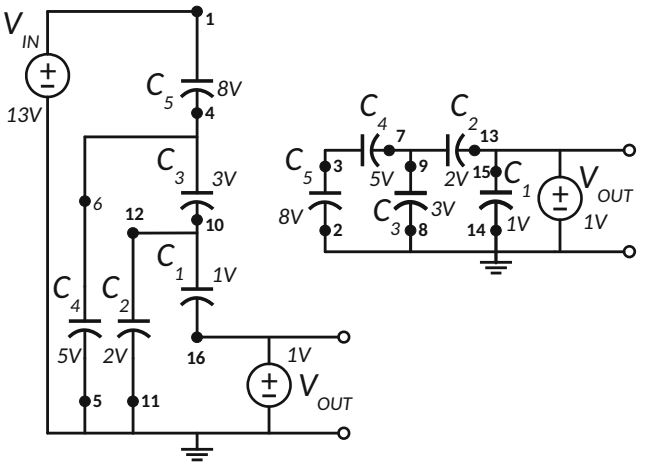

Fig. A.11 13 to 1 step-down switched-capacitor DC–DC topology with capacitor bias voltages 85321

Table A.11 13:1_85321 topology-specific capacitor and switch parameters: bias voltage, charge multiplier, blocking voltage, and gate voltage swing

C_i	$i =$	1	2	3	4	5			
$V_{Cfly,bias}$	[V_{OUT}]	1	2	3	5	8			
q_{Ci}	[$\frac{q_{OUT}}{13}$]	5	3	2	1	1			
S_i	$i =$	1	2	3	4	5	6	7	8
$V_{block,i}$	[V_{OUT}]	5	5	8	3	3	5	5	2
q_{Si}	[$\frac{q_{OUT}}{13}$]	1	1	1	1	1	1	1	2
$V_{gate,sw,i}$	[V_{OUT}]	1	2	1	1	2	1	4	1
S_i	$i =$	9	10	11	12	13	14	15	16
$V_{block,i}$	[V_{OUT}]	3	1	1	2	1	1	1	1
q_{Si}	[$\frac{q_{OUT}}{13}$]	2	2	3	3	3	5	5	5
$V_{gate,sw,i}$	[V_{OUT}]	4	3	1	1	1	1	1	1

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