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Crosstalk in Modern On-Chip Interconnects

A FDTD Approach

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A FDTD Approach

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Preface

Advancement in VLSI technology offers gigascale integrated circuits in a system on-chip. In such circuits, interconnects play a key role in determining circuit performance such as time delay and power consumption. At high operating frequencies, the closely packed interconnects produce transient crosstalk. The crosstalk noise strongly influences the signal propagation delay and also causes logic or functional failure. Therefore, it is desirable to accurately model the crosstalk effects in the on-chip interconnects.

Over the years, several mathematical models have been proposed for the analysis of CMOS-gate-driven coupled interconnect lines. However, most of these crosstalk noise models consider the nonlinear CMOS driver as a linear resistor. This approximation is not valid for on-chip interconnects because during the input and output transition states the MOSFET operates in cutoff, linear, and saturation regions. The MOSFET operating time in the saturation region is about 50 % during the transition period. Moreover, the equivalent resistance value in saturation region is much higher than the linear region. Thus, assuming that the transistor operates in the linear region during the transition state leads to severe errors in the performance estimation of the driver interconnect load system. Therefore, it is necessary to develop an accurate model that appropriately considers the nonlinear effects of CMOS driver and accurately measures the crosstalk-induced performance parameters of on-chip interconnects. This book presents an accurate and time efficient model of CMOS-gate-driven coupled interconnects for crosstalk-induced performance analysis by considering the nonlinear effects of CMOS driver.

The conventional interconnect copper material suffers due to lower reliability with downscaling of interconnect dimensions. The reliability of Cu decreases due to electromigration-induced problems such as hillock and void formations. Moreover, with highly scaled dimensions the resistivity of copper increases due to electron-surface scattering and grain-boundary scattering. Therefore, researchers are forced to find an alternative material for on-chip interconnects. Carbon nanotubes (CNTs) have been proposed as a promising interconnect material. A portion of this book is focused toward modeling of MWCNT interconnects. Based on the electrical

equivalent model, an accurate FDTD model is presented while incorporating the quantum effects of nanowire and nonlinear effects of CMOS driver. The crosstalk noise is comprehensively analyzed by examining both functional and dynamic crosstalk effects.

Graphene nanoribbon (GNR), a strip of ultrathin width graphene layer, has also been considered aggressively by researchers as a potential alternative material for realizing on-chip interconnects. Most of the physical and electrical properties of GNRs are similar to that of CNTs; however, the major advantage of GNRs over CNTs is that both transistor and interconnect can be fabricated on the same continuous graphene layer, thus avoiding the metal-graphene contact problems. This book presents an accurate model for the analysis of MLGNR interconnects using the FDTD technique. In a more realistic manner, the model incorporates the width-dependent MFP parameter that helps in accurately estimating the crosstalk-induced performance in comparison to conventional models. Moreover, a comparative analysis of crosstalk-induced performance is presented among Cu, MWCNT, and MLGNR interconnects.

The stability of the FDTD technique is constrained by the Courant-Friedrichs-Lewy (CFL) stability condition. Hence, beyond the CFL condition, the technique is unstable and within it, the technique is inefficient. The efficiency improvements in the FDTD technique can be easily addressed if the CFL stability condition is removed by implicitly deriving the transmission line equations. To improve the efficiency of the FDTD technique, an unconditionally stable FDTD (US-FDTD) technique is presented for the analysis of MLGNR interconnects.

This book provides an accurate FDTD model for on-chip interconnects, covering most recent advancements in materials and design. Furthermore, depending on the geometry and physical configurations, different electrical equivalent models for CNT and GNR-based interconnects are presented. Based on the electrical equivalent models the performance comparison among the Cu, CNT, and GNR-based interconnects are also discussed. The proposed models are validated with the HSPICE simulations. The organization of the book is as follows: Chap. 1 introduces the current research scenario in modeling of on-chip interconnects. Chapter 2 presents the structure, properties, and characteristics of graphene based on-chip interconnects. The FDTD modeling of Cu-based on-chip interconnects is presented in Chap. 3. The model considers the nonlinear effects of CMOS driver as well as the transmission line effects of interconnect line that includes coupling capacitance and mutual inductance effects. Chapter 4 introduces an equivalent single conductor (ESC) model of MWCNT interconnects. Based on the ESC model, this chapter presents an accurate FDTD model of MWCNT while incorporating the quantum effects of nanowire and nonlinear effects of CMOS driver. The modeling of MLGNR interconnects using the FDTD technique is presented in Chap. 5. In a more realistic manner, the proposed model includes the effect of width-dependent MFP of the MLGNR while taking into account the edge roughness. Finally, to

improve the efficiency of the FDTD model, an unconditionally stable FDTD technique is presented for the analysis of on-chip interconnects in Chap. 6. Moreover, the performance of Cu interconnect is compared with MWCNT and MLGNR interconnects under the influence of crosstalk.

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About the Book

The book provides accurate FDTD models for on-chip interconnects, covering most recent advancements in materials and design. Furthermore, depending on the geometry and physical configurations, different electrical equivalent models for CNT and GNR based interconnects are presented. Based on the electrical equivalent models the performance comparison among the Cu, CNT, and GNR-based interconnects are also discussed in the book. The proposed models are validated with the HSPICE simulations.

The book introduces the current research scenario in modeling of on-chip interconnects. It presents the structure, properties, and characteristics of graphene-based on-chip interconnects and the FDTD modeling of Cu-based on-chip interconnects. The model considers the nonlinear effects of CMOS driver as well as the transmission line effects of interconnect line that includes coupling capacitance and mutual inductance effects. In a more realistic manner, the proposed model includes the effect of width-dependent MFP of the MLGNR while taking into account the edge roughness.

Chapter 1
Introduction to On-Chip Interconnects and Modeling

Abstract This chapter briefs about the challenges associated with the modeling of on-chip interconnects in nanoscale technology. Copper had been used as an on-chip interconnect material for a long time. However, as device dimensions are scale down the reliability decreases due to electromigration induced problems. Therefore, researchers are forced to find an alternative solution for future high-speed global VLSI interconnects. This chapter introduces the evolution of graphene interconnect materials and the challenges associated with them. This chapter also introduces the FDTD technique for the modeling of on-chip interconnects.

Keywords Carbon nanotube (CNT) · Copper · Finite-difference time-domain (FDTD) · Graphene nanoribbon (GNR) · Interconnects · Very large scale integration (VLSI)

1.1 Introduction

Advancement of technology in the nanometer regime considers high-speed and high-density very large scale integration (VLSI) circuits. It is desirable to use multilayer interconnections in three or more levels to achieve higher packing densities and smaller footprint [1, 2]. Based on the length and cross-sectional dimensions, the on-chip interconnects can be broadly characterized into three categories: local, intermediate, and global interconnects. Local interconnects consist of very thin lines, used to connect gates and transistors in a functional block. Intermediate interconnects are wider and longer than local interconnects, provide low-resistance signal paths in a functional block. The global interconnects provide long-distance communication between the functional blocks and have a large cross-sectional area to minimize the resistance [3]. The global interconnects are placed at the higher level of the chip and can be as long as 1–2 cm in current high-performance integrated circuits [1].

In early days, the operating speed of an integrated circuit was limited by the speed of a logic gate. Interconnects between the gates were considered as ideal

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conductors, where the signal propagates instantaneously. Therefore, the interconnects had little effect on circuit operation. However, after the introduction of submicron semiconductor devices, the ideal behavior of interconnects no longer remains adequate. In fact, the performance of the chip is primarily determined by the interconnect line rather than the device [4].

At high operating frequencies, the closely packed interconnects produce transient crosstalk [5–7]. The undesired effect created on one line due to a signal transmitted on another line is defined as crosstalk. The crosstalk noise strongly influences the signal propagation delay and causes the circuit malfunction or functional failure. Based on the switching transitions in the coupled lines, crosstalk can be broadly classified into functional and dynamic crosstalks. When the victim line is quiescent, a voltage spike appearing on it due to switching in an adjacent line is referred as the functional crosstalk. Dynamic crosstalk appears when the adjacent lines are simultaneously switching either in-phase or out-phase. A change in logic value and propagation delay can be experienced under functional and dynamic crosstalks, respectively. Moreover, the crosstalk noise causes signal overshoot, undershoot and ringing effects. Therefore, accurate estimation of performance parameters, under the effect of crosstalk, gained importance for the design of high-performance on-chip interconnects.

1.2 Evolution of Interconnect Materials

Aluminum had been used for a long time to form interconnect lines because of its compatibility with silicon. However, as device dimensions scale down the reliability decreases due to increasing current density that may lead to electromigration induced problems [2]. In 1997, IBM announced plans to replace aluminum with copper, a metal with lower resistivity than aluminum [2]. Copper provides high current density (10^7 A/cm^2) leading to the electromigration effect being less significant [8]. Later on, it was realized that even Cu was not able to fulfil the demands of high-speed interconnects due to the following reasons:

(i) The reliability decreases with down scaling of interconnect dimensions due to increase in current density.
(ii) The resistivity increases at lower dimensions, due to grain-boundary scattering and surface scattering.
(iii) The resistivity increases rapidly due to Joule heating.
(iv) The conductivity reduces at high operating frequencies, due to the skin effect.

Therefore, the copper interconnect material is unable to meet the requirements of future technology needs. The widening gap between the requirements of future on-chip interconnect material and the presently used copper material has compelled researchers and designers to look out for novel material solutions. Graphene based nano interconnects have been proposed as a promising solution for the future on-chip interconnects [9–15]. Encouragingly, graphene nano interconnects

demonstrate longer mean free paths (MFPs) in the order of several micrometers, higher current densities in excess of 10^9 A/cm^2, and higher thermal stability than copper. These properties create lots of interest among researchers to use these materials as VLSI interconnects [16, 17]. Graphene nano interconnects can be classified into carbon nanotubes (CNTs) and graphene nanoribbons (GNRs).

1.2.1 Carbon Nanotubes (CNTs)

Carbon nanotubes are single layer of graphene sheets rolled up into cylinders with diameters ranging from 1 to 5 nm. The electron transport in metallic CNTs is ballistic that results in movement of electrons without scattering along the nanotube axis and enables a long MFP in the range of micrometers [18–22]. Contrastingly, the MFP of electrons in Cu is limited to a few nanometers. Due to the large MFP and small diameter, the electrons do not scatter as often in CNTs which results in low resistance. This low resistance ensures that the energy dissipated in CNTs is incredibly small. Thus, the problem of dissipated power density can be properly addressed. Moreover, the 1D structure of CNT offers many electrical properties, such as

(i) High quality CNTs have long MFP ranging from 1 to 5 μm that results in ballistic transport phenomenon.
(ii) The strong sigma bonds are useful for high mechanical strength and pi bonds are useful for high conductivity.
(iii) Higher electron mobility ($\sim 10^5$ cm^2/(Vs)) in comparison to Cu ($\sim 10^3$ cm^2/(Vs)) that results in high drift velocity.
(iv) Larger current densities (10^{10} A/cm^2) in comparison to Cu (10^6 A/cm^2) that results in lower electromigration effect.

Depending on the number of concentrically rolled up graphene sheets, CNTs are categorized as single-walled CNTs (SWCNTs) and multi-walled CNTs (MWCNTs) [23, 24]. SWCNT is a single-layer sheet of graphite rolled up into a cylinder. The primary drawback of SWCNT bundle is the non-controllability of its chirality. The metallic and semiconducting properties of CNTs are primarily dependent on their chirality. Statistically, one-third of the CNTs in a bundle are considered to be conducting (i.e., metallic) while the remaining behaves as semiconductors. Morris [25] observed that the SWCNTs with random chiralities do not show any advantage over the conventional interconnect materials. This problem can be rectified by using MWCNTs that consist of multiple layers of graphene sheets arranged in co-axial configuration with the diameters ranging from 2 nm to several tens of nanometers. Due to the large diameters, the MWCNT shells are conductive even if they are of semiconducting chirality because the energy gap is inversely proportional to the shell diameter. For a semiconducting CNT having a diameter greater than 20 nm, the gap between the conduction band and the Fermi level is observed to be smaller

Table 1.1 Electrical properties of CNTs and comparison with other materials [11]

Semiconducting properties			Metallic properties		
Parameter	Semiconducting CNT	Silicon	Parameter	Metallic CNT	Copper
Bandgap (eV)	0.9/diameter	1.12	Mean free path (nm)	10^3	40
Electron mobility (cm^2/Vs)	20×10^3	1500	Current density (A/cm^2)	10^{10}	10^6
Electron phonon mean free path (μm)	~0.07	0.0076	Resistivity (Ω-m)	$\sim 10^{-5}$	1.68×10^{-8}

than 0.0258 eV, which can be smeared by the environmental temperature [26]. Table 1.1 summarizes the unique electrical properties of metallic and semiconducting CNTs and compares them with copper and silicon.

1.2.2 Graphene Nanoribbons (GNRs)

Graphene nanoribbon, a strip of ultra-thin width graphene layer, has also been considered aggressively by the researchers as a potential alternative material for realizing on-chip interconnects [27, 28]. Most of the physical and electrical properties of GNRs are similar to that of CNTs, however, the major advantage of GNRs over CNTs is that both transistors and interconnects can be fabricated on the same graphene layer [29]. Therefore, one of the manufacturing difficulties regarding the formation of metal–nanotube contact can be avoided. Depending on the number of stacked graphene sheets, GNRs are classified as single-layer GNRs (SLGNRs) and multilayer GNRs (MLGNRs). Due to the lower resistivity and easy fabrication process, the MLGNRs are often preferred over SLGNRs as interconnect material. However, the MLGNRs fabricated till date have displayed some level of edge roughness [30, 31]. The electron scattering at the rough edges, reduces the MFP that substantially lowers the conductance of the MLGNRs. This fundamental challenge limits the performance of MLGNR interconnects.

1.3 Modeling of On-Chip Interconnects

Historically, interconnects were modeled as a lumped capacitor [1]. With the advancement of technology, the cross-sectional area of interconnects were scaled down, due to which the line resistance became significant and therefore, the interconnect line was represented as lumped resistance-capacitance (*RC*) [32]. However, later these interconnect parasitic elements were not treated as lumped

elements. To improve the accuracy, a distributed *RC* model was considered [33]. Currently, the parasitic inductance has started to play an important role in an on-chip interconnect performance due to the adoption of low resistive interconnect materials, and high operating switching frequencies. Therefore, the on-chip interconnects must be treated as distributed *RLC* lines or as transmission lines to estimate the performance accurately [34]. Agarwal et al. [4] proposed a model considering the transmission line effects of coupled on-chip interconnects driven by a linear resistor. Kaushik et al. extended this model to a nonlinear complementary metal–oxide–semiconductor (CMOS) driver using alpha-power law model and analyzed functional crosstalk effects in [35] and dynamic crosstalk effects in [36]. The models reported in [4, 35] and [36] are based on even-odd modes and hence limited to purely two coupled interconnect lines. Furthermore, the transient analysis was carried out for lossless lines, which is impractical.

The modeling of distributed *RLC* lines along with nonlinear CMOS driver suffers from frequency/time domain conversion problem. This problem arises because the transmission lines were traditionally solved in the frequency domain by using the partial differential equations, whereas the CMOS driver is modeled in the time domain. Therefore, to avoid this conversion problem, most of the researchers [4, 5, 37] replace the nonlinear CMOS driver by the linear resistive driver that severely affects the accuracy of the model. In the present research work, to avoid the conversion problem, finite-difference time-domain (FDTD) technique is used to solve the transmission line equations in the time domain. Using the FDTD method, the voltage and current values can be correctly estimated at any particular point on the interconnect line. Moreover, the FDTD model can be extended to n coupled interconnect lines with low computational cost.

In past, FDTD techniques were used to analyze the transmission lines, which are excited and terminated by resistive driver and resistive load, respectively [38–40]. Including the frequency dependent losses, Orlandi et al. [41] proposed the FDTD model for the analysis of multiconductor transmission lines terminated in arbitrary loads using the state-variable formulation. However, the models proposed in [38–40] analyze the transmission lines with resistive drivers and hence are not valid for the accurate study of on-chip interconnects performance, which are actually excited and terminated by the CMOS inverters. Based on the FDTD technique, Li et al. [42] proposed a model for the transient analysis of CMOS gate-driven distributed *RLC* interconnects. Coupled interconnects were analyzed at global interconnect length using 180 nm technology node where the nonlinear CMOS drivers were modeled by the alpha-power law model. This model is not accurate under the conditions when the technology is scaled down beyond 180 nm, due to the ignorance of the finite drain conductance parameter. Therefore, it is necessary to develop an accurate model that appropriately considers the nonlinear effects of CMOS drivers and accurately measures the crosstalk induced performance parameters of on-chip interconnects. This book presents an accurate and time-efficient model of CMOS gate-driven coupled interconnects for crosstalk induced performance analysis. The model is developed using the FDTD technique for coupled on-chip interconnects, whereas the

CMOS driver is modeled by either *n*th power law or modified alpha-power law model by considering the finite drain conductance parameter. The model is validated by comparing the results with HSPICE simulations.

1.4 Introduction to FDTD Method

FDTD is a popular computational electromagnetic modeling technique. Initially, this method was implemented to solve Maxwell's equations in the time domain. In this method, the time-dependent partial differential equations are discretized in space and time using the central difference approximations. The resulting finite difference equations are solved in a leapfrog time stepping manner for the solution of the Maxwell's equations [43]. In the present book, FDTD technique is used to solve transmission line equations, where the relative parameters are line voltage (V) and current (I) on a transmission line, that are analogous to the electrical field (E) and magnetic field (H) in Maxwell's equations, respectively.

To carry out the FDTD analysis of a transmission line model, a computational domain has to be established. The computational domain for the transmission line is modeled by resistance, inductance and capacitance (RLC) elements with relative parameters of V and I. The V and I values are determined at each point in space and time within the computational domain. The resistance (R), inductance (L), and capacitance (C) parasitics of the line must be specified for each cell in the computational domain. In case of coupled line system, the mutual inductance and the coupling capacitance should also be included within the computational domain. After establishing the computational domain, the boundary conditions have to be specified at the near-end and far-end boundaries. At the near-end boundary, the interconnect line is driven by a nonlinear CMOS inverter, whereas at the far-end boundary the interconnect line is terminated by a gate capacitance of the CMOS inverter load. After specifying the near and far-end terminals, the boundary conditions must be incorporated in the computational domain to match the FDTD solution for voltage and current at discrete time and space points. Time is implicit in the FDTD method, whereas space is explicit. Nevertheless, the FDTD method provides the exact solution if the following two conditions are satisfied: (1) spatial step (Δz) must be small enough in comparison to the wavelength (generally 10–20 steps per wavelength); (2) time step (Δt) must be small enough to satisfy the Courant condition [38–41]. The FDTD technique offers the following advantages:

(i) This technique allows the user to specify the computational domain. A wide variety of linear and nonlinear mediums can be modeled easily.
(ii) The voltage and current parameters are evaluated at any particular point on the interconnect line can be quickly and accurately obtained.
(iii) The technique requires less number of assumptions; therefore, the accuracy is very high.
(iv) The technique is able to simulate a wide range of frequencies.
(v) The model can be extended to n number of lines with low computational cost.

1.4.1 Central Difference Approximation

The FDTD method is developed based on the central difference approximation. This subsection describes the evaluation of numerical derivatives using central difference approximation. Consider a function of one variable $f(t)$. Expanding this in a Taylor series in a neighborhood of a desired point t_0 gives

$$f(t_0+\Delta t) = f(t_0)+\Delta t f'(t_0)+\frac{\Delta t^2}{2!}f''(t_0)+\frac{\Delta t^3}{3!}f'''(t_0)........ \quad (1.1)$$

where the primes denote the various derivatives with respect to the function. Solving this for the first derivative gives

$$f'(t_0) = \frac{f(t_0+\Delta t)-f(t_0)}{\Delta t}-\frac{\Delta t}{2!}f''(t_0)-\frac{\Delta t^2}{3!}f'''(t_0)........ \quad (1.2)$$

Thus first order derivative can be approximated as

$$f'(t_0) = \frac{f(t_0+\Delta t)-f(t_0)}{\Delta t}+\theta(\Delta t) \quad (1.3)$$

where $\theta(\Delta t)$ denotes that the error in truncating the series is on the order of Δt. So the first derivative may be approximated with the forward difference

$$f'(t_0) \cong \frac{f(t_0+\Delta t)-f(t_0)}{\Delta t} \quad (1.4)$$

This amounts to approximating the derivative of $f(t)$ as with its region of the desired point. If we expand the Taylor's series as

$$f(t_0-\Delta t) = f(t_0)-\Delta t f'(t_0)+\frac{\Delta t^2}{2!}f''(t_0)-\frac{\Delta t^3}{3!}f'''(t_0)........ \quad (1.5)$$

which can be approximated by

$$f'(t_0) \cong \frac{f(t_0)-f(t_0-\Delta t)}{\Delta t} \quad (1.6)$$

This gives the backward approximate equation for derivative.

Other approximations known as central differences can be found by subtracting Eq. (3.3) from Eq. (3.6) to yield the first derivative central difference approximation

$$f'(t_0) \cong \frac{f(t_0+\Delta t)-f(t_0-\Delta t)}{2\Delta t} \quad (1.7)$$

with a truncation error of Δt^2. Similarly, the second derivative central difference is obtained by adding (3.2) and (3.6) to yield

$$f''(t_0) \cong \frac{f(t_0 + \Delta t) - 2f(t_0) + f(t_0 - \Delta t)}{\Delta t^2} \quad (1.8)$$

with a truncation error on the order of Δt^2. Due to second-order error truncation in central difference approximation, FDTD termed as FDTD solution with second-order accuracy.

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Chapter 2
Interconnect Modeling, CNT and GNR Structures, Properties, and Characteristics

Abstract This chapter reviews the Cu-based on-chip interconnect modeling. The unique atomic structure and properties of carbon nanotube (CNT) and graphene nanoribbon (GNR) are discussed. The characteristics and semiconducting/metallic properties of graphene-based on-chip interconnects are presented. Depending on the physical configuration, equivalent electrical models of MWCNT and MLGNR interconnect lines are also introduced. An extensive review on performance analysis of on-chip interconnects is presented.

Keywords Electrical equivalent model · Equivalent single conductor (ESC) · Lüttinger liquid theory · Multiconductor transmission line (MTL) · Tight-binding approximation

2.1 Interconnect Modeling Approaches

In the early days of VLSI design, the crosstalk-induced signal integrity effects were negligible because of relatively low integration density and slow operating speed. However, with the introduction of technology scaling of below 0.25 μm, there were many significant changes in the structure and electrical characteristics [1, 2]. The interconnect lines started to be a dominating factor for chip performance and robustness. The line parasitic elements have a major impact on the electrical behavior of the interconnect model. These models vary from simple to very complex depending upon the effects that are being studied and the required accuracy. There are three different types of approaches available in literature for modeling Cu-based on-chip interconnects.

2.1.1 Lumped Model with CMOS Driver

This approach focuses on the CMOS gate modeling while the interconnect line is approximately considered as a lumped circuit. Alpha-power law model [3] has been

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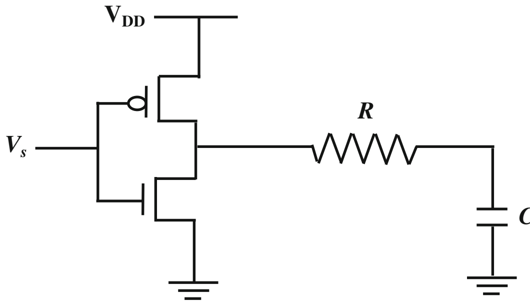

Fig. 2.1 A CMOS gate-driven *RC* load

widely used for representation of short-channel transistor that includes the velocity saturation effects. Based on the alpha-power law model, delay formulas were developed for CMOS gate-driven lumped capacitance modeled interconnect line [4, 5]. Bisdounis et al. [6] extended the model to include the influences of short-circuit current and gate-to-drain coupling capacitance. With the resistive component of interconnect becoming comparable to the gate output impedance, the line resistance *R* of interconnect line needs to be considered. Considering the line resistance, the modeling of CMOS gate-driven resistor-capacitor (*RC*) line was presented in [7–9]. The representation of CMOS gate-driven lumped *RC* load is shown in Fig. 2.1. Alder and Friedman [10] derived the delay equations for repeater insertion of a CMOS buffer design with *RC* interconnects. They developed a closed-form expression for the timing analysis of CMOS gate-driven *RC* load. They also derived an expression for the short-circuit power dissipation of the driver-interconnect-load system. However, all these approaches [3–10], lumped the total wire resistance of each segment into one single *R* and similarly combined the global capacitance into a single capacitor *C*. This lumped *RC* model is inaccurate for long interconnect wires, which are more adequately represented by a distributed *RC* model. Moreover, due to high operating frequencies and wider interconnect dimensions, interconnects exhibit inductance effects and should be included in the delay and crosstalk noise models. Hence, the analytical models that considered only *RC* were no longer accurate [3–10].

2.1.2 Distributed Model with Resistive Driver

In the distributed model with resistive driver, the driver-interconnect-load system is analyzed by simplifying the CMOS gate driver as a resistive driver [11]. Using the linear driver approximation, Elmore delay model was initially developed for *RC* lines [12] and then extended to *RLC* lines [13, 14]. The distributed *RLC* line with linear driver is shown in Fig. 2.2, where R_d and C_L represent driver resistance and load capacitance, respectively; *r*, *l* and *c* represent per-unit-length line resistance,

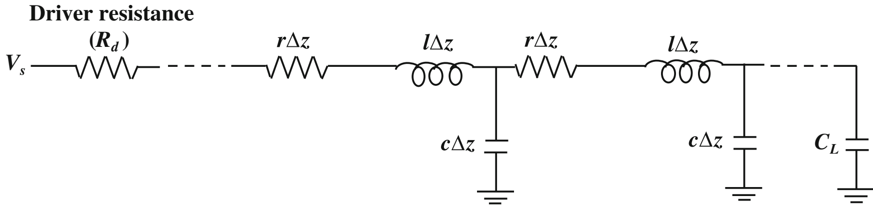

Fig. 2.2 A distributed *RLC* interconnect line driven by a resistive driver

inductance, and capacitance, respectively. Considering the nonlinearity of the driver, Bai et al. [15] improved the linear driver model by calculating the effective resistance. Davis and Meindl proposed closed-form delay expressions for the analysis of distributed *RLC* lines by considering the single transmission line effects in [16] and a crosstalk noise model of coupled transmission lines in [17].

Based on even–odd mode technique, the crosstalk noise model was developed by Agarwal et al. [18] for coupled-two lossless lines and then modified for low-loss lines to analyze crosstalk-induced noise peak voltage. They investigated that at high operating frequencies, inductive coupling effects are significant and should be included for accurate crosstalk noise analysis. Using the coupled transmission line theory, the authors developed a crosstalk noise model that is useful to guide noise-aware physical design optimizations. A closed-form analytical transient response model was derived for resistance/capacitance loads by solving semifinite transmission line equations [19]. However, all these models [11–19] consider the nonlinear CMOS driver as a linear driver that limits the accuracy of the models.

2.1.3 Distributed Model with CMOS Driver

The distributed model with CMOS driver approach co-simulates the nonlinear CMOS gate and the distributed interconnect. The CMOS gate-driven distributed *RLC* interconnect line is shown in Fig. 2.3. Based on the even–odd modes, Kaushik et al. proposed a simple analytical model for functional crosstalk analysis in [20] and dynamic crosstalk analysis in [21] of CMOS gate-driven two coupled

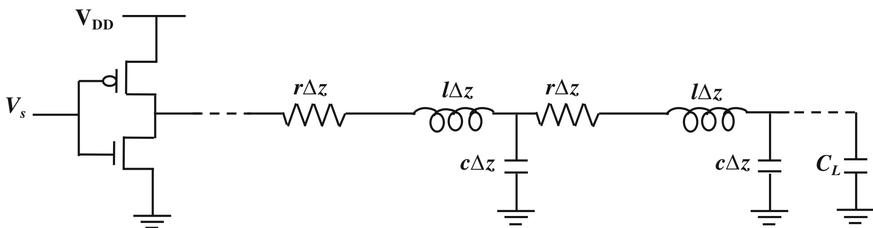

Fig. 2.3 A CMOS gate-driven distributed *RLC* interconnect line

interconnect lines. The model was developed based on the alpha-power law model of MOS transistors and transmission line theory of interconnects. There the authors have observed that the nonlinear effects of the CMOS inverter should be incorporated in a valid crosstalk noise modeling. Moreover, it was noticed that the use of resistive driver model presented a pessimistic view on the performance analysis of on-chip interconnects. However, these models [20, 21] were based on the even–odd modes and hence limited to two coupled interconnect lines. Later on, Li et al. [22] proposed an FDTD method for the transient analysis of CMOS gate-driven lossy transmission lines including frequency-dependent losses and observed the effect of functional crosstalk. However, the model ignored the finite drain conductance parameter in the modeling of CMOS driver and hence not useful for nanoscaled devices.

2.2 Carbon Nanotubes

Until mid-1980s, diamond and graphite were the only two known forms of carbon allotropes. In 1985, Kroto et al. [23] were able to synthesize new allotrope of carbon C_{60}. They used a high pulse of laser light to vaporize a sample of graphite. The vaporized graphite was sent to a mass spectrometer with the help of helium gas. The mass spectrometer detected the presence of C_{60}, a molecule consisting of 60 carbon atoms. The C_{60} had the shape of a soccer ball with 12 pentagon faces and 20 hexagonal faces. The easy synthesis of C_{60} led the group to propose the existence of another allotrope of carbon named as “buckyball” due to its soccer ball-shaped structure. The shape of the new allotrope of carbon did not end at the soccer-shaped structures and long cylindrical tube-like structures were also reported, which are known as carbon nanotubes (CNTs).

CNTs have fascinated the research world due to their extraordinary physical, electrical, and chemical properties. Many of the properties defy the conventional trends and scientists are still discovering the unique properties and constantly making efforts to understand and explain the phenomenon for such distinctive behavior. One of the remarkable physical properties of CNT is its ability to scale down its thickness to a single atomic layer. Another interesting physical property observed in CNTs is when two slightly different-structured CNTs are joined together; the resultant junction formed can be used as an electronic device. The properties of the device formed are dependent on the type of CNTs used for their formation.

2.2.1 *Basic Structure of CNTs*

A single-walled CNT can be assumed as a structure formed when a single graphene sheet is rolled into a cylindrical shape (Fig. 2.4). Depending on the shape of the

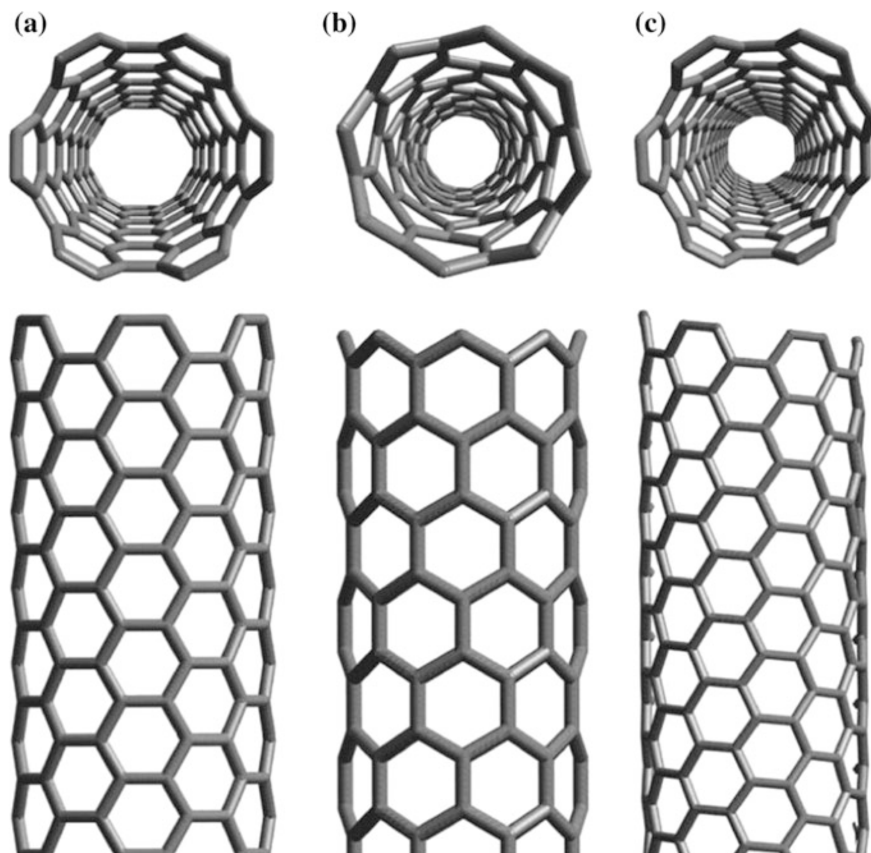

Fig. 2.4 Sketches of three different SWCNT structures: **a** armchair nanotube, **b** zigzag nanotube, and **c** chiral nanotube

circumference, CNTs can be classified as armchair (ac), zigzag (zz), or chiral CNTs as shown in Fig. 2.4a–c, respectively [24]. The terms zigzag and armchair are inspired from the pattern in which the carbon atoms are arranged at the edge of the nanotube cross section. Graphene consists of sp^2-hybridized atoms of carbon that are arranged in a hexagonal pattern. The hexagonal carbon rings should join coherently when placed in contact with adjacent carbon atoms. Accordingly, in an SWCNT tube, all the carbon atoms (except at the edges) form hexagonal rings and are therefore equally spaced from one another. Xu et al. [25] reported the fabrication of vertically grown CNT bundles with an average diameter of 50 μm and a pitch of 110 μm.

In spite of the hexagonal aromatic rings, SWCNT is considered to be more reactive than planar graphene. It is due to the fact that the hybridization in SWCNTs is not purely sp^2 and some degree of sp^3 hybridization is also present. It has been observed that with the decrease in SWCNT diameter, the degree of sp^3

hybridization increases [26]. This phenomenon causes variable overlapping of energy bands that results in SWCNTs obtaining versatile and unique electrical properties. It was studied that beyond the diameter of ≈2.5 nm, the SWCNT tube collapses into a two-layer ribbon [26]. Moreover, a CNT with smaller diameter results in higher stress on the structure, although SWCNTs of ≈0.4 nm diameter have been produced [27]. It is therefore natural to consider that a diameter of ≈1 nm is the most suitable value with regard to energy consideration of SWCNTs. Encouragingly, there are no such restrictions on the length of the SWCNTs. The length is dependent on the processes and methods used for synthesis of the SWCNTs. SWCNTs of length ranging from micrometers to millimeters can be commonly observed. Considering the diameter and length of an SWCNT, it is easy to intuitively conclude that SWCNT structures have exceptionally high aspect ratios.

A graphene sheet can be rolled in a number of different ways (see Fig. 2.4). The mathematical expression that can be used to represent the various ways of rolling graphene into the tubes is shown below [28]:

$$PX = \boldsymbol{C}_h = p\boldsymbol{b}_1 + q\boldsymbol{b}_2 \tag{2.1}$$

where $\boldsymbol{C}_h$ is chirality vector, p and q are integers. The unit vectors $\boldsymbol{b}_1$ and $\boldsymbol{b}_2$ are defined as

$$\boldsymbol{b}_1 = \frac{b\sqrt{3}}{2}\boldsymbol{x} + \frac{b}{2}\boldsymbol{y} \quad \text{and} \quad \boldsymbol{b}_2 = \frac{b\sqrt{3}}{2}\boldsymbol{x} - \frac{b}{2}\boldsymbol{y} \tag{2.2}$$

where b = 2.46 Å and $\cos\theta = \frac{2p+q}{2\sqrt{p^2+q^2+pq}}$.

The vector PX is normal to the CNT tube axis and θ is chirality angle. The diameter d of a nanotube is dependent on $\boldsymbol{C}_h$ by the following relation:

$$d = \frac{|C_h|}{\pi} = \frac{b_{\mathrm{C-C}}\sqrt{3(p^2+q^2+pq)}}{\pi} \tag{2.3}$$

where $1.41\ \text{Å(graphene)} \leq b_{\mathrm{C-C}} \leq 1.44\ \text{Å}(\mathrm{C}_{60})$.

The C–C bond length in the hexagonal ring structure of SWCNT slightly increases from the C–C bond length in graphene due to the curved structure of SWCNT. The degree of curvature in an SWCNT cannot exceed the degree of curvature in C_{60} molecule, resulting in the upper limit of C–C bond length in SWCNTs. Similarly, the degree of curvature in an SWCNT cannot be less than the curvature in a flat graphene structure, resulting in lower limit of C–C bond length in SWCNTs. Moreover, it can be observed that $\boldsymbol{C}_h$, θ, and d can be expressed in terms of p and q. Since SWCNTs can be identified by $\boldsymbol{C}_h$, θ, and d values, it is sufficient to define SWCNTs through p, q values by denoting them as (p, q). The p and q values for a particular SWCNT can be easily obtained by counting the number of hexagonal rings separating the margins of $\boldsymbol{C}_h$ vector following $\boldsymbol{b}_1$ first and then $\boldsymbol{b}_2$

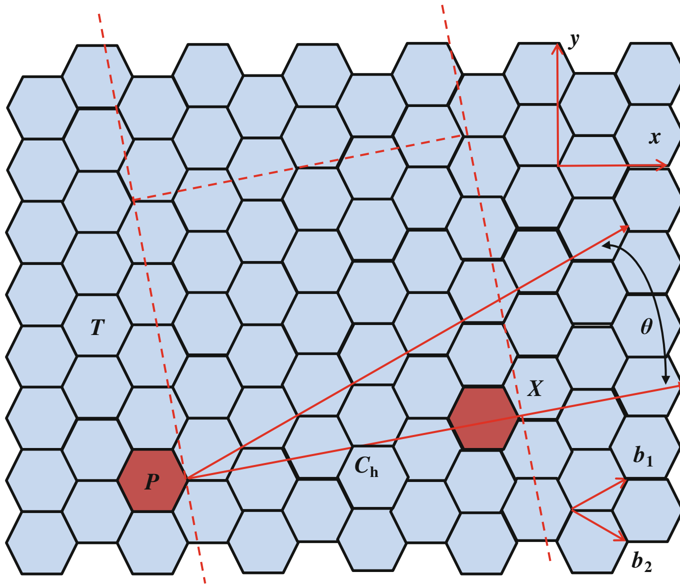

Fig. 2.5 Sketch representing the procedure to obtain a CNT, starting from a graphene sheet

[29]. Based on the (p, q) representation, zz SWCNTs can be denoted as (p, 0) and having $\theta = 0°$; ac SWCNTs can be denoted as (p, p) and having $\theta = 30°$; chiral SWCNTs can be denoted as (p, q) and having $0 < \theta < 30°$.

From Fig. 2.5, it can be observed that having $\boldsymbol{C}_h$ direction perpendicular to any carbon bond directions results in zz SWCNT ($\theta = 0°$), while having $\boldsymbol{C}_h$ direction parallel to any carbon bond directions will result in ac SWCNT ($\theta = 30°$). In chiral SWCNTs, $0 < \theta < 30°$ due to hexagonal rings in graphene sheet.

An MWCNT is a bit more intricate in structure compared to an SWCNT. Unlike a single graphene shell in an SWCNT, there are multiple graphene shells in an

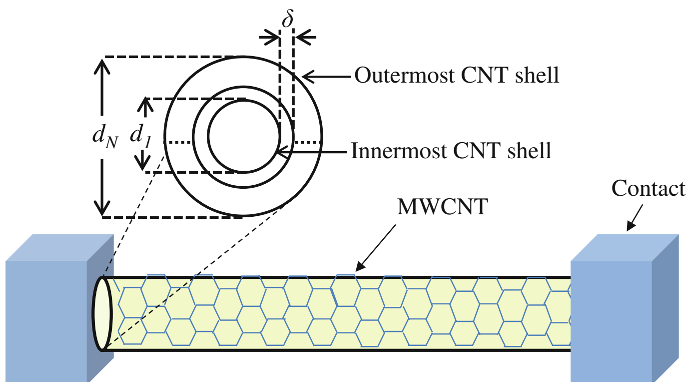

Fig. 2.6 The structure of MWCNT placed between the two contacts

MWCNT. The MWCNTs have two or more numbers of CNT shells that are concentrically rolled up. The structure of MWCNT between the two contacts is shown in Fig. 2.6, wherein the inset figure shows its cross-sectional view. The intershells are separated by the van der Waals gap, $\delta \sim 0.34$ nm. The diameter of outermost CNT shell can be varied from a few nanometers to several tens of nanometers. The diameters of outermost and innermost shells are denoted by d_N and d_1, respectively. The ratio of d_1/d_N varies in different MWCNTs, the values between 0.3 and 0.8 have been observed in [30–32]. The density of 10^6/cm^2 has been obtained in [30] with a d_1/d_N of 0.5. The current carrying capabilities of MWCNTs are similar to the SWCNT bundles, however, the MWCNTs are easier to fabricate [33]. Close et al. [34] reported the fabrication of MWCNTs with 80 shells based on a versatile method that is ideally suited for fabricating MWCNT interconnects with extensive electrical properties.

2.2.2 Semiconducting and Metallic CNTs

CNTs can act as semiconducting or metallic based on the pattern of CNT circumference. The armchair CNTs always act as metallic, whereas the zigzag CNTs act as either metallic or semiconducting depending on the chiral indices. This section presents the behavior of zz CNTs and their dual nature.

Since CNT is a rolled-up sheet of graphene, an appropriate boundary condition is required to explore the band structure. If CNT can be considered as an infinitely long cylinder, there are two wave vectors associated with it: (1) the wave vector parallel to CNT axis, $k_{||}$, that is continuous in nature due to the infinitely long length of CNTs and (2) the perpendicular wave vector, $k_{\perp}$, that is along the circumference of the CNT. These two wave vectors must satisfy a periodic boundary condition [28]

$$k_{\perp}.C_h = \pi d k_{\perp} = 2\pi m \tag{2.4a}$$

where m is an integer. The quantized values of allowed $k_{\perp}$ for CNTs are obtained from the boundary condition. The cross-sectional cutting of the energy dispersion with the allowed $k_{\perp}$ states results in the one-dimensional band structure of graphene as shown in Fig. 2.7a. This is called zone folding scheme of obtaining the band structure of CNTs. Each cross-sectional cutting gives rise to one-dimensional subband. The spacing between allowed $k_{\perp}$ states and their angles with respect to the surface Brillouin zone determine the one-dimensional band structures of CNTs. The band structure near the Fermi level is determined by allowed $k_{\perp}$ states that are close to the K points. When the allowed $k_{\perp}$ states pass directly through the K points as shown in Fig. 2.7c, the energy dispersion has two linear bands crossing at the Fermi level without a bandgap. However, if the allowed $k_{\perp}$ states miss the K points as shown in Fig. 2.7b, there would be two parabolic one-dimensional bands with an energy bandgap. Therefore, two different kinds of CNTs can be expected depending on the wrapping indices, first, the semiconducting CNTs with bandgap as in Fig. 2.7b and second, the metallic CNTs without bandgap as in Fig. 2.7c [28].

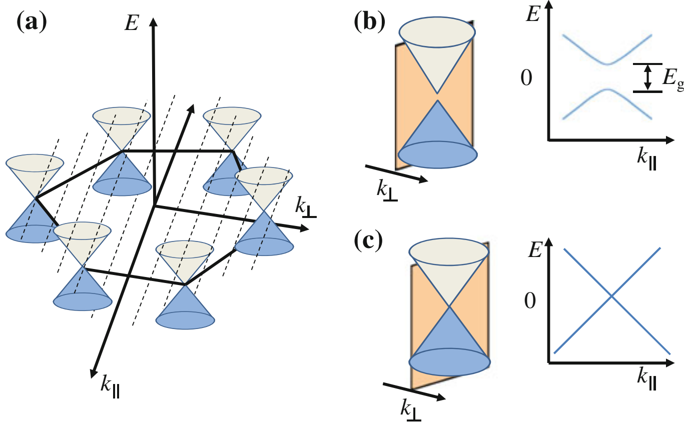

Fig. 2.7 Band structures of CNT shell **a** first Brillouin zone of graphene with conic energy dispersions at six K points. The allowed $k_\perp$ states in CNT are presented by dashed lines. The band structure of the CNT is obtained by the cross sections as indicated. Close view of the energy dispersion near one of the K points are schematically shown along with the cross sections by allowed $k_\perp$ states and resulting one-dimensional energy dispersions for **b** a semiconducting CNT and **c** a metallic CNT

Using the approach of one-dimensional subbands discussed in previous subsection, the one-dimensional subband closest to the K points for zigzag CNTs is investigated here. Based on the chiral indices, the zigzag CNTs can show metallic/semiconducting property. Since the circumference is $\bar{p} \cdot b(C_\mathrm{h} = \bar{p} \cdot b_1)$, the boundary condition in Eq. (2.4a) becomes

$$k_x \bar{p} b = 2\pi m \tag{2.4b}$$

There is an allowed k_x that coincides with K point at (0, 4π/3b). This condition arises when $\bar{p}$ has a value in multiples of 3 ($\bar{p} = 3\bar{q}$, where $\bar{q}$ is an integer). Therefore, by substitution in Eq. (2.4b) [28]

$$k_x = \frac{2\pi m}{\bar{p} b} = \frac{3Km}{2\bar{p}} = \frac{Km}{2\bar{q}} \tag{2.5}$$

There is always an integer $(m = 2\bar{q})$ that makes k_x pass through K points and these types of CNTs (with $\bar{p} = 3\bar{q}$) are always metallic without bandgap as shown in Fig. 2.7c. There are two cases when p is not a multiple of 3. If $\bar{p} = 3\bar{q} + 1$, the k_x is closest to the K point at $m = 2\bar{q} + 1$ (as in Fig. 2.7b).

$$k_x = \frac{2\pi m}{\bar{p} b} = \frac{3Km}{2\bar{p}} = \frac{3K(2\bar{q} - 1)}{2(3\bar{q} + 1)} = K + \frac{K}{2} \frac{1}{3q + 1} \tag{2.6}$$

Similarly, for $\bar{p} = 3\bar{q} - 1$, the allowed k_x closest to K is when $m = 2\bar{q} - 1$, hence

$$k_x = \frac{2\pi m}{\bar{p}b} = \frac{3Km}{2\bar{p}} = \frac{3K(2\bar{q} - 1)}{2(3\bar{q} - 1)} = K - \frac{K}{2}\frac{1}{3\bar{q} - 1} \tag{2.7}$$

In these two cases, allowed k_x misses the K point by

$$\Delta k_x = \frac{K}{2}\frac{1}{3\bar{q} \pm 1} = \frac{2}{3}\frac{\pi}{\bar{p}b} = \frac{2}{3}\frac{\pi}{\pi d} = \frac{2}{3d} \tag{2.8}$$

From Eq. (2.8), it is inferred that the smallest misalignment between an allowed k_x and a K point is inversely proportional to the diameter. Thus, from the slope of a cone near K points in Eq. (2.4a), the bandgap E_g can be expressed as

$$E_g = 2 \times \left(\frac{\partial E}{\partial k}\right) \times \frac{2}{3d} = 2\hbar v_F \left(\frac{2}{3d}\right) \approx 0.7\text{eV}/d\,(\text{nm}) \tag{2.9}$$

Therefore, semiconducting CNTs (d = 0.8–3 nm) exhibit bandgap ranging from 0.9 to 0.2 eV. Depending on the value of $\bar{p}$, where $\bar{p}$ is the remainder when p and q is divided by 3, SWCNTs [represented by (p, q)] can be of three types:

$\bar{p} = 0$; metallic with linear subbands crossing at the K points.
$\bar{p} = 1, 2$; semiconducting with a bandgap, E_g ~ 0.7 eV/d (nm).

Similar treatment can also be applied for armchair CNTs $(\bar{p}, \bar{p})$, arriving at the conclusion that they are always metallic.

2.2.3 *Properties and Characteristics of CNTs*

The atomic arrangements of carbon atoms are responsible for the unique electrical, thermal, and mechanical properties of CNTs [35, 36]. The sp^2 bonding delivers the high conductivity and mechanical strengths to the CNTs. The unique properties of CNTs are discussed below.

2.2.3.1 Strength and Elasticity

Due to the sp^2-hybridization, each carbon atom in a single sheet of graphite is connected via strong sigma bonds to three neighboring atoms. Thus, CNTs exhibit the strongest basal plane elastic modulus and hence are expected to be the ultimate high-strength fiber. The elastic modulus of CNT is much higher than steel that makes the CNT as a strongest material. Although forcing on the tip of nanotube will cause it

to bend, the nanotube returns to its original state as soon as the force is removed. This property makes CNTs extremely useful as probe tips for high-resolution scanning probe microscopy. Although, the current Young's modulus of SWCNT is about 1 TPa, but a much higher value of 1.8 TPa has also been reported [37]. For different experimental measurement techniques, the values of Young's modulus vary in the range of 1.22–1.26 TPa depending on the size and chirality of the SWCNTs [36]. It has been observed that the elastic modulus of CNTs is not strongly dependent on the diameter. Primarily, the moduli of CNTs correlate to the amount of disorder in the nanotube walls [38].

2.2.3.2 Thermal Conductivity and Expansion

CNTs can exhibit superconductivity below 20 K (−253 °C) due to the strong in-plane sigma bonds in between carbon atoms. The sigma bond provides exceptional strength and stiffness against axial strains. Moreover, the larger interplane and zero in-plane thermal expansion of SWCNTs results in high flexibility against nonaxial strains.

Due to their high thermal conductivity and large in-plane expansion, CNTs exhibit exciting prospects in nanoscale molecular electronics, sensing and actuating devices, reinforcing additive fibers in functional composite materials, etc. Recent experimental measurements suggest that the CNT-embedded matrices are stronger in comparison to bare polymer matrices [39]. Therefore, it is expected that the nanotube may also significantly improve the thermomechanical and the thermal properties of the composite materials.

2.2.3.3 Field Emission

Under the application of strong electric field, tunneling of electrons from the metal tip to vacuum results in the phenomenon of field emission. Field emission results from the high aspect ratio and small diameter of CNTs. The field emitters are suitable for the application in flat panel displays. For multiwalled CNTs, the field emission properties occur due to the emission of electrons and light. Without applied potential, the luminescence and light emission occur through the electron field emission and visible part of the spectrum, respectively.

2.2.3.4 Aspect Ratio

One of the exciting properties of CNTs is the high aspect ratio, which infers that a lower CNT load is required compared to other conductive additives to achieve

similar electrical conductivity. The high aspect ratio provides unique electrical conductivity in CNTs in comparison to the conventional additive materials such as chopped carbon fiber, carbon black, or stainless steel fiber.

2.2.3.5 Absorbent

Carbon nanotubes and CNT composites have been emerging as perspective absorbing materials due to their light weight, larger flexibility, high mechanical strength, and large surface area. Therefore, CNTs emerge out as ideal candidates for use in gas, air, and water filtration. The absorption frequency range of SWCNT–polyurethane composites broaden from 6.4–8.2 (1.8 GHz) to 7.5–10.1 (2.6 GHz) and to 12.0–15.1 GHz (3.1 GHz) [40]. A lot of research has already been carried out for replacing the activated charcoal with CNTs for certain ultra-high purity applications [41].

2.2.3.6 Conductivity

CNTs are assumed to be the most electrically conductive materials. However, it is quite difficult to control the chirality of the SWCNT shells and therefore statistically only one-third of the CNTs in a bundle is assumed to be conducting and the rest of them are semiconducting. However, because of large diameters, the CNT shells of MWCNTs would be conductive even if they are of semiconductor characteristics. The energy gap between the conduction band edge and the Fermi level of a CNT shell is defined as [30]

$$\boldsymbol{E}_g = \frac{v_0 p_{\mathrm{C-C}}}{d} \tag{2.10}$$

where d is the CNT diameter, v_0 is the nearest-neighboring tight-binding parameter, and $p_{\mathrm{C-C}}$ is the nearest neighbor C–C bond length, which is $\sim$0.142 nm. From Eq. (2.10), it can be observed that the bandgap is inversely proportional to the diameter. Therefore, the semiconducting CNT shells with larger diameter are conductive. The detailed conductivity comparison between MWCNTs and SWCNTs will be discussed in the following sections.

2.2.4 Conductivity Comparison

The performance of interconnect primarily depends on the conductivity of the interconnect filler material. The conductivity comparison among Cu, SWCNT, and MWCNT is analyzed in this section.

2.2.4.1 SWCNT Conductivity

The conductivity of SWCNT [42, 43] can be expressed as

$$\sigma_{\mathrm{SWCNT}} = \frac{4G_0 l_0 d F_m}{\sqrt{3}(d+\delta)^2} \frac{l}{(l + l_0 d)} \tag{2.11}$$

where l, d, F_m are the interconnect length, shell diameter, fraction of metallic CNTs in the bundle, respectively, l_0 is 10^3, δ is 0.34 nm, G_0 is the quantum conductance equal to $2e^2/h$, e is the charge of an electron, and h is the Planck's constant.

For $l > l_0 d$, Eq. (2.11) can be expressed as

$$\sigma_{\mathrm{SWCNT}} \approx \frac{4G_0 l_0 d F_m}{\sqrt{3}(d+\delta)^2} \tag{2.12}$$

From Eq. (2.12), it can be observed that for longer interconnects, the conductivity of SWCNT is independent of length.

2.2.4.2 MWCNT Conductivity

The conductivity of MWCNT [44] can be expressed as

$$\sigma_{\mathrm{MWCNT}} = \frac{G_0 l}{2\delta}\left[\left(1 - \frac{d_{\mathrm{min}}^2}{d_{\mathrm{max}}^2}\right)\frac{a}{2} + \left(b - \frac{l}{l_0}a\right) \times \left(\left(\frac{1}{d_{\mathrm{max}}} - \frac{d_{\mathrm{min}}}{d_{\mathrm{max}}^2}\right) - \frac{l}{d_{\mathrm{max}}^2 l_0}\ln\frac{d_{\mathrm{max}} + \frac{l}{l_0}}{d_{\mathrm{min}} + \frac{l}{l_0}}\right)\right] \tag{2.13}$$

where d_{max} and d_{min} are the outermost and the innermost shell diameters of an MWCNT, respectively; a and b are constants and the values are 0.0612 nm^{-1} and 0.425, respectively [45]. From Eq. (2.13), it can be observed that for $l > (l_0 b/a)$, the conductivity increases with an increase in d_{max}.

The conductivity comparison plot among Cu, SWCNT bundles, and MWCNT is shown in Fig. 2.8. It can be observed that for shorter interconnect length, the conductivity of SWCNT bundle is higher than MWCNT, whereas for longer lengths, MWCNTs can potentially have conductivities several times larger than that of copper or even SWCNT, which is essential for interconnect applications. It is worth noting that the best case scenario is considered for SWCNTs, wherein they were densely packed so that highest conductivity is obtained. However, in contrast to this, an average case scenario was considered for MWCNTs wherein the innermost diameter is half of the outermost shell diameter. The innermost diameters were considered as 5, 15, 35, 50 nm for respective outer diameters of 10, 30, 70, 100 nm. However, the best case scenario for MWCNTs would have been when the innermost diameter had been 1 nm. But still, for longer interconnects, the performance of the MWCNTs was better than the SWCNTs.

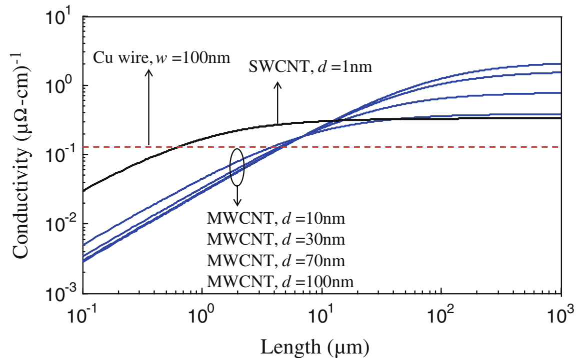

Fig. 2.8 The conductivity comparison among Cu, SWCNT, and MWCNT

2.2.5 *MWCNT Interconnect Modeling*

MWCNTs have recently acquired importance for VLSI on-chip interconnect material due to their high current carrying capabilities. For the first time, Burke [46] proposed an electrical equivalent model for the analysis of CNT interconnects based on the Lüttinger liquid theory. The model considered the quantum effects of a nanowire by including the quantum resistance, kinetic inductance, and quantum capacitance. The electrical equivalent model was further explained by Avouris et al. [47] through extensive study of electronic structure and transport properties of CNTs. Depending on the analysis, a bottom-up approach was demonstrated by Li et al. [48] to integrate MWCNTs into multilevel interconnects in silicon-integrated circuits. Ngo et al. [49] reported the mechanism of electron transport across metal–CNT interface. The authors analyzed this mechanism for two different MWCNT architectures, horizontal or side-contacted MWCNTs and vertical or end-contacted MWCNTs. Later, Miano and Villone [50] extended the fluid theory model for frequency domain to describe the electromagnetic response of three-dimensional (3D) structures formed by metallic CNTs and conductors within the framework of classical electrodynamics.

Xu and Srivastava [51] presented a semiclassical one-dimensional (1D) electron fluid model that took into account the electron–electron repulsive force. Based on the one-dimensional electron fluid theory, the authors presented a transmission line model of metallic CNT interconnects using classical electrodynamics. However, the authors neglected the inter-CNT tunneling phenomenon. Later, Li et al. [43] presented a multiconductor transmission line (MTL) model for the MWCNT. The authors considered the tunneling effect between the adjacent shells in MWCNT and neighboring CNTs in a bundle. However, using the MTL model, the analysis of MWCNT with N number of tubes leads to the solution of differential equations with the system dimensional of $2N$, which can be computationally expensive. For this reason, the equivalent single conductor (ESC) model was proposed in [52].

The ESC model is based on the assumption that voltages at an arbitrary cross section along MWCNT are the same, such that all nanotubes are connected in parallel at both ends. The accuracy of the ESC model in comparison to MTL model has been reported by several researchers [52, 53]. It was observed that the transient responses to a pulse input of MTL model and ESC model are in good agreement. The MTL and ESC models are briefly described in the next section.

2.2.5.1 MTL and ESC Models of MWCNT Interconnect

The electrical equivalent models of MWCNT interconnect are discussed in this section. The schematic cross-sectional view of MWCNT interconnect is shown in Fig. 2.9. The MWCNT bundle interconnect line is positioned over a ground plane at a distance H and placed in a dielectric medium with dielectric constant ε. The MWCNT interconnect consists of N number of tubes with intershell distance δ, inner shell diameter d_1, and outer shell diameter d_N. The total number of CNTs in an MWCNT can be expressed as

$$N = 1 + \text{int}\left[\frac{(d_N - d_1)}{2\delta}\right] \tag{2.14}$$

where int[•] represents an integer value. The number of conducting channels in a CNT can be derived by adding all the subbands contributing to the current conduction. Using Fermi function, it can be expressed as

$$N_{\text{ch},i} = \sum_{\text{subbands}} \frac{1}{\exp(|E_i - E_F|/k_B T) + 1} \tag{2.15}$$

where T is the temperature, k_B is the Boltzmann constant, and E_i is the lowest (or highest) energy for the subbands above (or below) the Fermi level E_F.

The multiconductor transmission line (MTL) model of MWCNT interconnect is described in Fig. 2.10, where $R_{MC,i}$ and $R_{Q,i}$ represent the imperfect metal contact

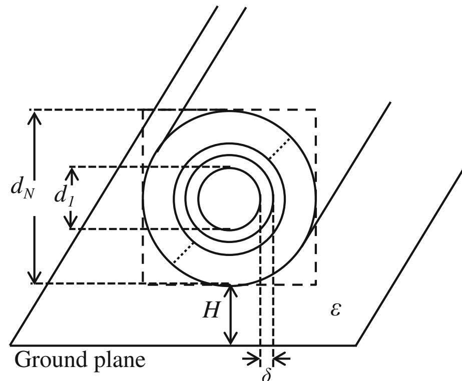

Fig. 2.9 Geometry of an MWCNT with N shells above a ground plane

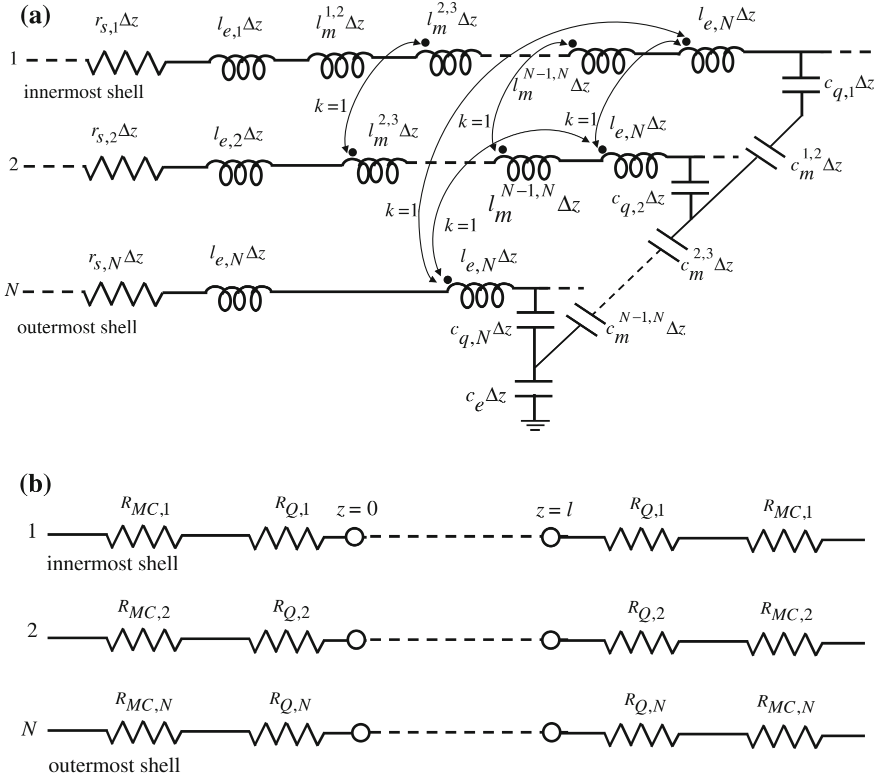

Fig. 2.10 Multiconductor transmission line model of MWCNT (**a**) section of infinitesimal length Δz, where $k = 1$ represents perfect magnetic coupling (**b**) nanotube of length l including terminal resistance

resistance and quantum resistance of ith shell, respectively; $r_{s,i}$, $l_{k,i}$, and $c_{q,i}$ represent the p.u.l. scattering resistance, kinetic inductance, and quantum capacitance, respectively. The parasitics $R_{Q,i}$, $r_{s,i}$, $l_{k,i}$, and $c_{q,i}$ can be expressed as

$$R_{Q,i} = \frac{h}{4e^2 N_{\mathrm{ch,i}}} \tag{2.16a}$$

$$r_{s,i} = \frac{h}{2e^2 \lambda_{\mathrm{mfp,i}} N_{\mathrm{ch,i}}} \tag{2.16b}$$

$$l_{k,i} = \frac{h}{4e^2 v_F N_{\mathrm{ch,i}}} \tag{2.16c}$$

$$c_{q,i} = \frac{4e^2 N_{\mathrm{ch,i}}}{h v_F} \tag{2.16d}$$

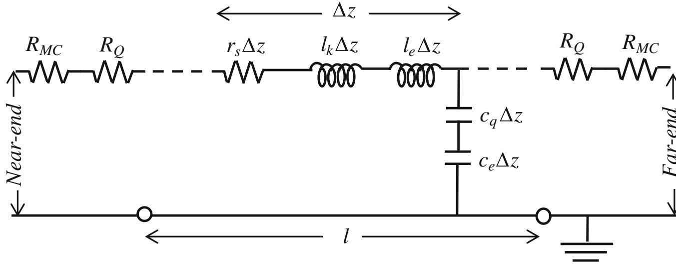

Fig. 2.11 Equivalent single conductor model of MWCNT

where h, e λ_{mfp}, and v_F represent the Planck's constant, electron charge, mean free path, and Fermi velocity, respectively.

In Fig. 2.10, $l_{e,i}$ is p.u.l. magnetic inductance of the ith shell and c_e is p.u.l. electrostatic capacitance, $c_m^{i,i+1}$ and $l_m^{i,i+1}$ are the p.u.l. coupling capacitance and mutual inductance between the shells, respectively. These parasitics can be expressed as

$$l_{e,i} = \frac{\mu_0\mu_r}{2\pi}\cosh^{-1}\left[\left(\frac{d_i + 2H}{d_i}\right)\right] \tag{2.16e}$$

$$c_e = \frac{2\pi\varepsilon_0\varepsilon_r}{\cosh^{-1}\left[\left(\frac{d_N + 2H}{d_N}\right)\right]} \tag{2.16f}$$

$$c_m^{i,i+1} = \frac{2\pi\varepsilon_0}{\ln(d_{i+1}/d_i)}, \quad i = 1, 2, \ldots, N-1 \tag{2.16g}$$

$$l_m^{i,i+1} = \frac{\mu}{2\pi}\ln(d_{i+1}/d_i), \quad i = 1, 2, \ldots, N-1 \tag{2.16h}$$

To reduce the complexity of the MTL model, a simplified ESC model was proposed in [52]. The ESC model is shown in Fig. 2.11. This model was developed based on the assumption that voltages at an arbitrary cross section along MWCNT are the same. Thus, all the scattering resistances $r_{s,i}$ are in parallel and can be replaced by an equivalent resistance ($r_{s,\mathrm{ESC}}$). The $r_{s,\mathrm{ESC}}$ can be expressed as

$$r_{s,\mathrm{ESC}} = \frac{h/e^2}{\sum_{i=1}^{N} 2N_{\mathrm{ch},i}\lambda_{\mathrm{mfp},i}} \tag{2.17a}$$

Referring to Fig. 2.12, the distributed MWCNT capacitance $c_{q,\mathrm{ESC}}$ is expressed in terms of quantum capacitance and coupling capacitance between shell to shell.

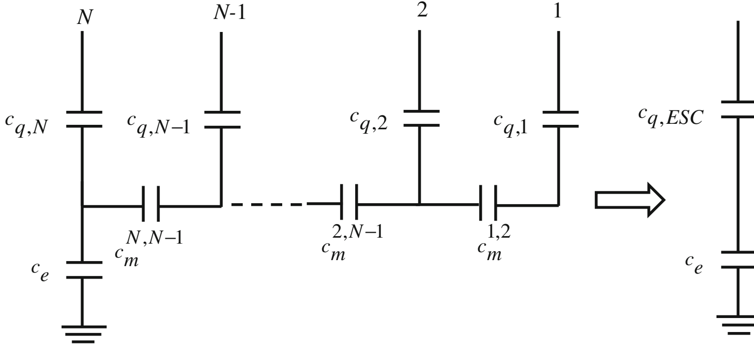

Fig. 2.12 Per unit length capacitance network of the MWCNT

$$c_{\text{equ,1}} = c_{q,1} \tag{2.17b}$$

$$c_{\text{equ,i}} = \left(\frac{1}{c_{\text{equ,i-1}}} + \frac{1}{c_m^{i-1,\text{i}}} \right)^{-1} + c_{q,\text{i}}, \quad i = 2, 3, \ldots, N \tag{2.17c}$$

$$c_{q,\text{ESC}} = c_{\text{equ,N}} \tag{2.17d}$$

The inductance equations can be written in a similar form. The ESC model of MWCNT interconnect is thoroughly discussed in Sect. 4.2.

2.2.6 MWCNT Performance Analysis

The performance analysis of MWCNT interconnects was analyzed using both the MTL and ESC models in [54]. The voltage response of two coupled MWCNT interconnects of 14 and 22 nm technologies was computed to a pulse input. It was observed that both models are in good agreement. The same agreement was achieved in the estimation of 50 % time delay as well. The validity of the ESC model was also verified experimentally in [52]. Based on the ESC model, Lamberti et al. [55] compared the performance of MWCNTs with SWCNTs. The propagation delay time was analyzed at three different technologies 15, 21, and 32 nm by means of interval analysis. It was observed that for global interconnect lengths, the time delay obtained for MWCNT interconnects is less than 1 ns for the most severe configuration, i.e., for 15 nm technology node at a length of 250 µm, whereas for SWCNTs the delay is as large as 7.87 ns.

The estimation of performance parameters under the crosstalk influence is an important design concern in modern VLSI interconnects. The crosstalk analysis of MWCNTs has been studied by several researchers. Liang et al. [56] analyzed the crosstalk noise effects with lengths ranging from 10 to 1000 µm at 22 and 14 nm

technology nodes. Moreover, the performance of MWCNTs was compared with the Cu interconnects. They observed that the MWCNT interconnects showed better performance for longer wire lengths and smaller technology nodes. Das et al. [57] analyzed the crosstalk effects in Cu, SWCNT, and MWCNT interconnects. They observed that the MWCNT-based interconnects are more suitable for VLSI interconnects. Furthermore, the authors analyzed the power supply voltage drop for Cu- and MWCNT-based interconnects in [58]. It was observed that the CNT-based interconnects have significantly less power drop in comparison to that of Cu-based interconnects for semi-global and global lengths. Based on the ESC model, Liang et al. [59] investigated the crosstalk effects in Cu and MWCNT interconnects. They reported that the crosstalk-induced time delays in MWCNT interconnects are much smaller than those in the Cu interconnects. Sahoo and Rahaman [60] developed an analytical closed-form delay expression for both Cu and MWCNT interconnects. They observed that the performance of MWCNT interconnects over copper interconnects is improved by 90 % for 200 μm long interconnect. In 2015, Tang et al. [61] proposed a fast transient simulation technique based on the ESC model for the crosstalk-induced performance analysis of MWCNT interconnects. They observed that the proposed method and HSPICE are very similar to each other with an average relative error of 1.54 %. However, most of the researchers [56, 59–61] used the resistive driver in the performance analysis of MWCNT interconnects that leads to severe errors in the performance estimation of the driver-interconnect-load (DIL) systems.

2.3 Graphene Nanoribbons

In 1996, Mitsutaka Fujita and his group provided a theoretical model of graphene nanoribbons (GNRs) to observe the edge and nanoscale dimension effect in graphene [62, 63]. Recent developments in GNRs have aroused a lot of research interest of their potential applications in the area of interconnects and field-effect transistors [64–66]. A monolithic system can be constructed using the single-layer GNR for both transistors and interconnects. For nanoscale device dimensions, Cu-based interconnects are mostly affected by grain boundaries and sidewall scatterings. It has been predicted that GNRs will outperform the Cu interconnects for smaller widths [67]. In a high-quality GNR sheet, the mean free path is ranging from 1 to 5 μm. GNRs can carry large current densities of more than 10^8 A/cm^2. They also offer high carrier mobility that can reach up to 10^5 cm^2/(Vs) [68].

2.3.1 Basic Structure of GNRs

A graphene nanoribbon is a single sheet of graphene layer, which is extremely thin and limited in width, such that it results in a one-dimensional structure [69]. As a

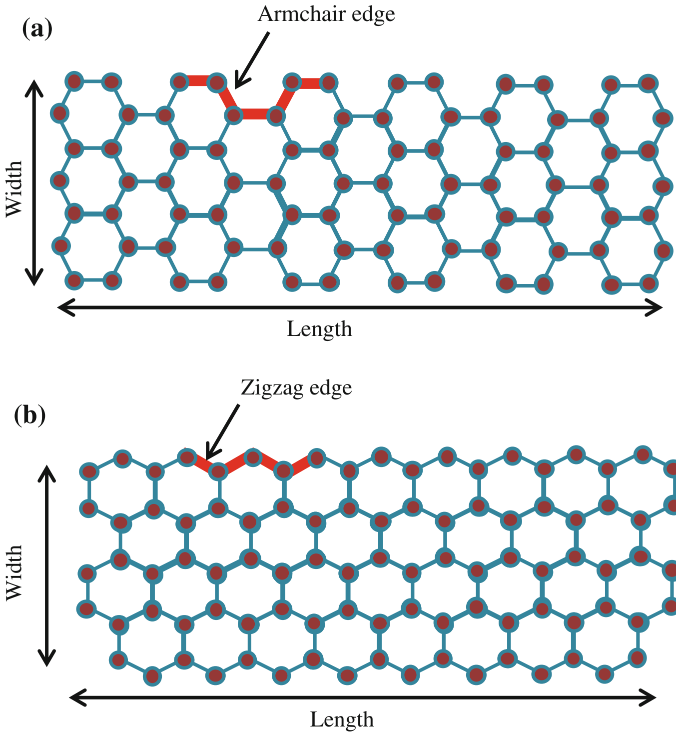

Fig. 2.13 Structure of GNR **a** armchair and **b** zigzag

result, GNRs can be considered as an unrolled version of CNTs. The electronic properties of GNRs are similar to that of CNTs. Depending on termination of their width, GNRs can be divided into chiral and nonchiral GNRs. The chiral GNRs can be further classified as armchair (ac) or zigzag (zz) GNRs as shown in Fig. 2.13a, b, respectively. It can be noted that the terms "armchair" and "zigzag" are used for both GNRs and CNTs. However, these nomenclatures are used in opposite ways. For GNRs the terms armchair and zigzag indicate the pattern of the GNR edge, whereas for CNTs the same terms indicate the CNT circumference. Therefore, the unrolled armchair CNT can be visualized as a zigzag GNR and vice versa.

Depending on the stacked graphene sheets, GNRs are classified as single-layer GNR (SLGNR) or multilayer GNR (MLGNR). The most promising interconnect solution for VLSI interconnect is MLGNR due to its higher current carrying capability than SLGNR. The geometric structure of an MLGNR is shown in Fig. 2.14. The MLGNR interconnect consists of N number of layers, with interlayer distance δ, width w, and thickness t.

From the fabrication point of view, it is evident that the growth of the GNRs can be more easily controlled than that of the CNTs because of their planar structure. This makes them compatible with the conventional lithography techniques [70].

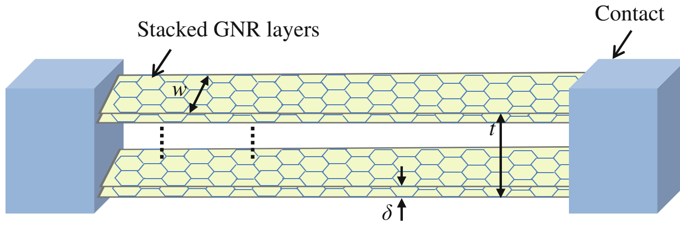

Fig. 2.14 The geometric structure of an MLGNR interconnect

Using the electron beam lithography technique, Murali et al. [71] fabricated an MLGNR interconnect with ten layers. The higher electrical conductivity in MLGNR can be obtained either by enhancing the carrier mobility or by increasing the number of carriers. The carrier mobility can be increased by intercalation doping of arsenic pentafluoride (AsF_5) vapor. Using the AsF_5 doping, the conductivity of MLGNR can be increased up to 3.2×10^5 S/cm, which is almost 1.5 times higher than the copper interconnects [72]. Additionally, the easier fabrication process of MLGNRs makes them as promising candidates for interconnect material.

2.3.2 *Semiconducting and Metallic GNRs*

GNRs can act as either semiconducting or metallic based on the pattern of the GNR edge. The zigzag edge-patterned GNR always act as metallic, whereas the armchair edge-patterned GNRs can act as either metallic or semiconducting depending on the number of carbon atoms present across the width of the GNR. This section presents the behavior of armchair GNRs and its dual nature.

The typical structure of armchair GNR is shown in Fig. 2.13a, where the number of carbon atoms across its width, $N_C = 7$. For understanding the metallic/semiconducting behavior of GNRs, it is necessary to analyze the electronic band structures. The band structures of GNRs are obtained using a tight-binding (TB) model [73]. Using the TB approach, the band structures of 23- and 24-atom wide armchair GNRs are shown in Fig. 2.15a, b, respectively. It can be observed that the metallic GNR has zero bandgap, whereas the semiconducting GNR has 0.2 eV bandgap. The ac GNR acts as metallic, if $N_C = 3a + 2$ and acts as semiconducting, if $N_C = 3a + 1$ or 3, where a is an integer. The zz GNRs are always metallic, independent of the value of N_C [73].

2.3.3 *Properties and Characteristics of GNRs*

Most of the physical and electrical properties of GNRs are similar to that of CNTs. However, compared to CNTs, the growth of the GNRs is considered to be more

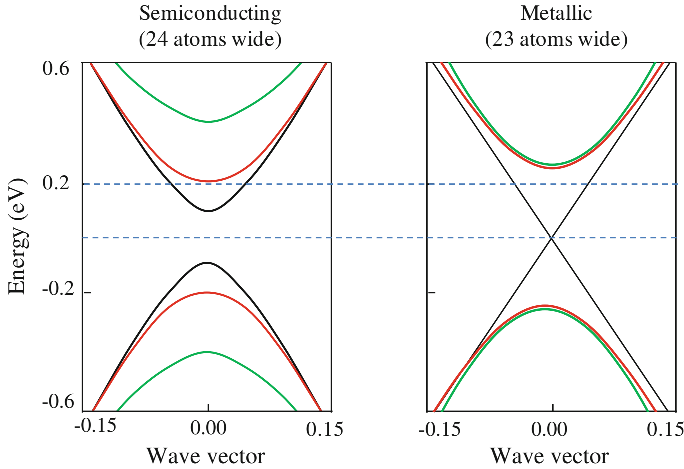

Fig. 2.15 Band structures of **a** semiconducting and **b** metallic armchair GNRs whose widths are 6.02 nm (24 atoms wide) and 5.78 nm (23 atoms wide), respectively

controllable due to their planar structure. Moreover, the major advantage of GNRs over CNTs is that both transistor and interconnect can be fabricated on the same continuous graphene layer, which unlike CNTs, are free from Stone–Wales defects [74]. Therefore, one of the manufacturing difficulties regarding the formation of metal–nanotube contact can be avoided. Due to the lower resistivity, the MLGNRs are often preferred over SLGNRs as suitable on-chip interconnect material. However, the MLGNRs fabricated till date, have displayed some level of edge roughness [70, 71]. The electron scattering at the rough edges reduces the mean free path that substantially lowers the conductance of the MLGNR. This fundamental challenge limits the performance of MLGNR-based interconnects. The value of MFP primarily depends on the level of edge roughness. The following sections discuss the effect of edge roughness on the MFP.

2.3.3.1 Mean Free Path of GNR

The effective MFP of GNR λ_{eff} depends on the scattering effects due to phonons λ_{ph}, defects λ_d, and edge roughness λ_n. Using Matthiessen's rule, the λ_{eff} can be expressed as

$$\frac{1}{\lambda_{\text{eff}}} = \frac{1}{\lambda_d} + \frac{1}{\lambda_n} + \frac{1}{\lambda_{\text{ph}}} \tag{2.18}$$

For the interconnect applications (low bias), the MFP corresponding to λ_{ph} is observed as extremely large, i.e., tens of micrometers, and therefore, its effect can

be neglected for the modeling of GNR scattering resistance [73]. Consequently, λ_d and λ_n dominate the overall value of λ_{eff}.

According to the experimental measurements reported in [75], the MFP corresponding to λ_d is about 1 μm for a single-layer GNR, which is width independent. However, in multilayer GNR, the MFP reduces due to the intersheet electron hopping [76]. The λ_d of MLGNR can be extracted by measuring the in-plane conductivity of GNR. Using the in-plane conductivity of $G_{\text{sheet}} = 0.026\ (\mu\Omega\text{-cm})^{-1}$ [77], layer spacing of 0.34 nm, and $E_F = 0$ of a neutral MLGNR, the λ_d is extracted as 419 nm by solving Eq. (2.19) [77]

$$G_{\text{sheet}} = \frac{2q^2}{h} \cdot \frac{\pi\lambda_d}{hv_f} \cdot 2k_BT \ln\left[2\cosh\left(\frac{E_F}{2k_BT}\right)\right] \tag{2.19}$$

To increase the conductivity of MLGNR, AsF_5 intercalated graphite can be used. The in-plane conductivity, $G_{\text{sheet}} = 0.63\ (\mu\Omega\text{-cm})^{-1}$ and carrier concentration, $n_p = 4.6 \times 10^{20}\ \text{cm}^{-3}$ are observed for the AsF_5 intercalated graphite [78]. Using the simplified TB model, the E_F can be expressed as

$$E_F = hv_F\left(\frac{n_p \cdot \delta}{4\pi}\right)^{1/2} \tag{2.20}$$

where $\delta = 0.575$ nm is the average layer spacing between adjacent graphene layers. Using the expressions (2.19) and (2.20), E_F and λ_d are expressed as 0.6 eV and 1.03 μm, respectively.

The MFP corresponds to diffusive scattering at the edges is a function of edge backscattering probability, P and the average distance by an electron travels along the length before hitting the edge. The mean free path for nth subband due to edge scattering can be expressed as [67]

$$\lambda_n = \frac{w}{P}\sqrt{\left(\frac{E_F/\Delta E}{n}\right)^2 - 1} \tag{2.21}$$

where ΔE is the gap between the subbands.

2.3.4 Conductivity Comparison

The performance of the interconnect line is primarily depends on the conductivity of the material. This section discusses the conductivity of various interconnect materials. Figure 2.16 shows the conductivity of Cu, SWCNT bundle, MWCNT and MLGNR interconnects. The fully specular edge MLGNR interconnects are analyzed for two different doped conditions [79]. First, the Fermi energy level of 0.3 eV is considered and second, the level of 0.6 eV is considered. The SWCNT

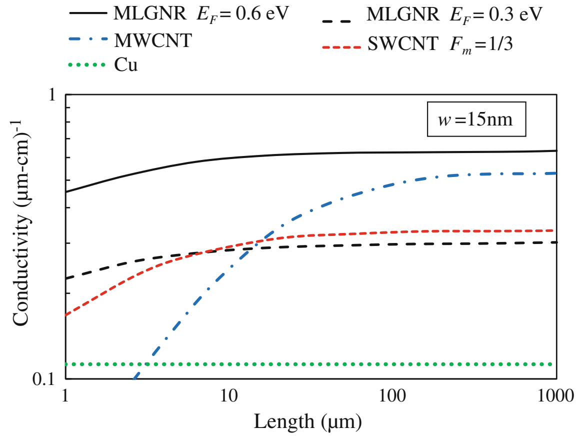

Fig. 2.16 Conductivity comparison among Cu, SWCNT bundle, MWCNT and MLGNR interconnects

diameter is chosen to be 1 nm with a metallic to semiconducting ratio (F_m) of 1/3. For MWCNTs, the outer diameter of CNT shell is considered as 15 nm. From Fig. 2.16, it can be observed that the conductivity of MLGNR increases with the Fermi energy. Moreover, at highly doped condition (E_F = 0.6 eV) the conductivity of MLGNR is observed to be higher than MWCNT interconnects.

2.3.5 MLGNR Interconnect Modeling

This section presents an electrical equivalent model of the MLGNR interconnect line. An MLGNR of width w and thickness t is placed above the ground plane at a distance H as shown in Fig. 2.17. The permittivity of the medium between the bottommost layer of MLGNR and the ground plane is represented by ε. The total number of layers (N_{layer}) can be expressed as

$$N_{\text{layer}} = 1 + \text{int}\left[\frac{t}{\delta}\right] \tag{2.22}$$

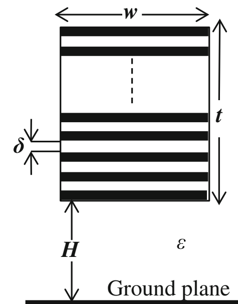

Fig. 2.17 Geometry of MLGNR above ground plane

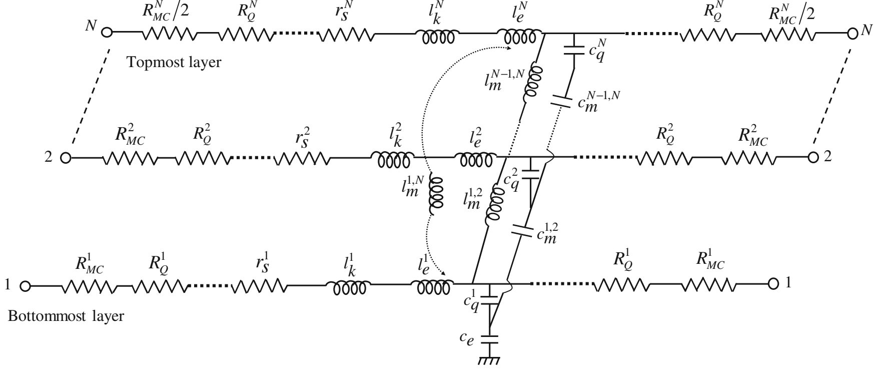

Fig. 2.18 Equivalent *RLC* model of MLGNR interconnect

The interlayer distance δ is considered to be 0.575 and 0.34 nm for doped and neutral MLGNRs [77], respectively.

The equivalent electrical model of MLGNR interconnect is presented in Fig. 2.18, wherein the parasitics are primarily dependent on the number of conducting channels (N_{ch}) of each layer in MLGNR. The N_{ch} takes into account the effect of spin and sublattice degeneracy of carbon atoms and primarily depends on the width, Fermi energy (E_F), temperature (T) and can be expressed as [80]

$$N_{\text{ch}} = \sum_{n=0}^{n_C} \left[e^{(E_i - E_F)/kT} + 1 \right]^{-1} + \sum_{n=0}^{n_V} \left[e^{(E_i + E_F)/kT} + 1 \right]^{-1} \tag{2.23}$$

where k, n_C, and n_V represent the Boltzmann constant, number of conduction and valence bands, respectively. E_i is the lowest/highest energy of ith subband in conduction/valence band [80].

Depending on the current fabrication process, the imperfect metal–MLGNR contact resistance (R_{MC}) has a typical value ranging from 1 to 20 kΩ [81]. Each layer of MLGNR exhibits lumped quantum resistance (R_Q) that is due to the quantum confinement of carriers across the interconnect width. The quantum resistance of jth layer (R_Q^j) can be expressed as

$$R_Q^j = \frac{h}{4e^2 \cdot N_{\text{ch}}} \tag{2.24}$$

For longer interconnects, scattering resistance r_s appears due to the static impurity scattering, defects, line edge roughness scattering (LER), etc. [82–84]. The r_s primarily depends on the effective MFP of electrons (λ_{eff}) and can be expressed as

$$r_s^j = \frac{h}{2e^2 \cdot N_{\text{ch}} \cdot \lambda_{\text{eff}}} \tag{2.25}$$

Using the Matthiessen's rule, the λ_{eff} of each subband can be expressed from (2.18). Each layer in MLGNR comprises of kinetic inductance (l_k) and quantum capacitance (c_q) that represent the mobile charge carrier inertia and the density of electronic states, respectively. The l_k and c_q of any layer j can be expressed as

$$l_k^j = \frac{l_{k0}}{2N_{\text{ch}}};\text{where } l_{k0} = \frac{h}{2e^2 v_F} \tag{2.26}$$

$$c_q^j = 2c_{q0} \cdot N_{\text{ch}};\text{where } c_{q0} = \frac{2e^2}{hv_F} \tag{2.27}$$

where $v_F \approx 8 \times 10^5$ m/s represents the Fermi velocity of carriers in graphene [81]. The kinetic inductance per channel is 8 nH/µm, which is verified by the experimental observations also [85]. The electrostatic capacitance (c_e) is due to the electric field coupling between the bottom most layer of MLGNR and the ground plane. Therefore, the c_e is primarily dependent on the MLGNR width (w) and the distance (H) from the ground plane. Apart from this, the magnetic inductance (l_e) of MLGNR interconnect is due to the stored energies of carriers in the magnetic field. The l_e and c_e can be expressed as

$$l_e^j = \frac{\mu_0 \mu_r H}{w} \quad \text{and} \quad c_e = \frac{\varepsilon_0 \varepsilon_r w}{H} \tag{2.28}$$

The interlayer mutual inductance (l_m) and coupling capacitance (c_m) are mainly due to the magnetic and electric field coupling between the adjacent layers. The l_m and c_m can be expressed as

$$l_m^{j-1,j} = \frac{\mu_0 \delta}{w}, \quad j = 2, 3, \ldots, N \tag{2.29a}$$

$$c_m^{j-1,j} = \frac{\varepsilon_0 w}{\delta}, \quad j = 2, 3, \ldots, N \tag{2.29b}$$

The analysis of signal propagation along an MLGNR with N_{layer} leads to the solution of a 2N-dimensional system of differential equations that can be highly time-consuming. For this reason, the equivalent *RLC* model of Fig. 2.18 is simplified to an ESC model shown in Fig. 2.19, wherein all the layers are assumed to be parallel. The value of $R_1 = (R_{MC} + R_Q)$ is equally divided between the two contacts on either side of the interconnect line. The detailed explanation of ESC model of MLGNR interconnect line is provided in Sect. 5.2.

2.3.6 MLGNR Performance Analysis

The performance of an MLGNR interconnect is generally evaluated by means of an electrical equivalent model. The equivalent model considers all the parasitic

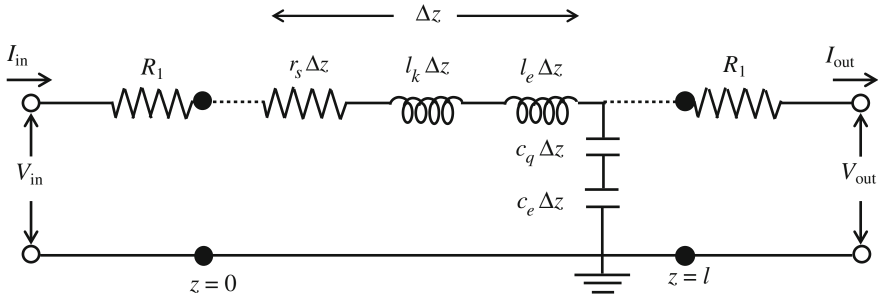

Fig. 2.19 Equivalent single conductor (ESC) model of MLGNR interconnect

parameters based on the quantum effects of the nanowire, and its electrostatic and magnetostatic characteristics. Sarto et al. proposed an electrical equivalent transmission model to represent the MLGNR interconnect [86]. They compared the performance between MWCNT and MLGNR interconnects and observed that the MLGNR interconnect has higher current carrying capability than the MWCNT interconnect. Xu et al. [77] derived the conductance model of MLGNR interconnect using the tight-binding approach and the Landauer formula. The conductance of the MLGNR is compared among Cu, W, and CNTs. They observed that the conductance of MLGNR is much higher than Cu, W, and CNTs when proper intercalation-doped MLGNRs are used. Nishad et al. [87] presented the analytical time domain models for the performance analysis of top contact and side contact MLGNR interconnects. Based on the analytical models, they designed an optimum top-contacted MLGNR interconnect that exceeds the performance of Cu and optical interconnects.

The crosstalk-induced signal transmission analysis of MLGNR interconnects was performed by Cui et al. [81] based on the transmission line model. The authors obtained the output response of driver-interconnect-load system using the transfer function. The impact of Fermi level on the signal transmission was also investigated. In 2014, Zhao et al. [79] performed the comparative study on MLGNR interconnects with SWCNT, MWCNT, and Cu interconnects. They observed that even with the maximum crosstalk impacts considered, the advantage of MLGNR interconnects over other interconnect materials can still be maintained. The impact of MLGNR line resistance variations on the crosstalk-induced performance parameters were investigated in [88]. The simulations were performed for 11 and 8 nm technology nodes for both intermediate and global interconnect lengths. They observed that irrespective of technology node, the perfectly doped fully specular MLGNR interconnects are better than Cu interconnects as far as the line resistance tolerance was concerned. However, the existing crosstalk noise models [79, 81, 88] analyzed the performance of MLGNR interconnects with resistive drivers that limits the accuracy of the models. Moreover, the authors considered the mean free path parameter independent of width by assuming perfectly smooth edges of MLGNRs.

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Chapter 3
FDTD Model for Crosstalk Analysis of CMOS Gate-Driven Coupled Copper Interconnects

Abstract This chapter deals with the modeling of Cu-based on-chip interconnects. The model considers the nonlinear effects of CMOS driver as well as the transmission line effects of interconnect line. The CMOS driver is represented by the *n*th power law model and the coupled-multiple interconnect lines are modeled by the FDTD technique. The model is validated by the industry standard HSPICE simulator. It is observed that the results of the proposed model closely match with that of HSPICE simulations. Encouragingly, the proposed model is highly time efficient than the HSPICE.

Keywords Complementary metal oxide semiconductor (CMOS) · Crosstalk · Finite-difference time-domain (FDTD) · Propagation delay · Transient response · Transmission line model

3.1 Introduction

In general, the modeling of on-chip interconnects is performed by assuming the nonlinear CMOS driver as a linear resistor [1–3]. However, this is not a valid assumption because the MOSFET operates in cutoff, linear, and saturation regions [4]. Moreover, the value of change in resistance in saturation region is much higher than the linear region. Especially, the PMOS operates in the saturation region for more than 60 % of time and in the linear region for less than 5 % of time [5]. Thus, assuming that the transistor operates in the linear region, leads to severe errors in the performance estimation of the driver-interconnect-load system.

The modeling of on-chip interconnects with nonlinear CMOS driver suffers with domain conversion problem. This problem arises because the CMOS driver elements appeared in the time domain, whereas the on-chip interconnects were solved in the frequency domain. The best way to avoid this conversion problem is the use of the FDTD technique to solve the transmission line equations of on-chip interconnects. Previously, Paul [6] analyzed the transmission line equations for the resistive driver and resistive load. In [7], Orlandi et al. extended this model by

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incorporating the frequency-dependent losses using the state-variable analysis. Additionally, several authors have also proposed FDTD-like techniques to analyze the transmission lines namely, latency insertion method [8], and alternating direction explicit-latency insertion method [9]. However, these models [6–9] analyze the transmission lines that are excited and terminated by the resistive drivers and resistive loads, respectively. Therefore, these models are not valid for the performance analysis of on-chip interconnects that are actually excited and terminated by the CMOS inverters.

In 2011, Li et al. [10] proposed a FDTD model for the analysis of on-chip interconnects by incorporating the nonlinear effects of CMOS driver. The authors analyzed the interconnect lines at global lengths for 180 nm technology node. However, they ignored the drain conductance parameter (σ), and therefore the estimated current was higher than the actual value. Moreover, the performance analysis is limited to functional crosstalk, wherein only one of the lines is in switching mode and the rest in quiet mode. In addition to the functional crosstalk analysis, the dynamic crosstalk also frequently occurs in the current technology nodes and its analysis is essential. The model presented in this chapter considers all these effects appropriately and accurately estimates the crosstalk-induced performance parameters.

This chapter presents the FDTD model for the crosstalk-induced performance analysis of on-chip interconnects. The crosstalk effects are comprehensively studied by including the dynamic and functional crosstalk analysis. The proposed model incorporates the transmission line effects of interconnect line and nonlinear effects of CMOS driver, and therefore it proves to be more accurate than the existing models. The CMOS driver is represented by the nth power law model [11], and the on-chip interconnect lines are modeled by FDTD technique.

This chapter is organized in seven sections as follows: Sect. 3.1 introduces the current research scenario on the modeling of on-chip interconnects. The motivation behind this work is described in Sect. 3.2. The FDTD model combined with nth power law model is presented in Sect. 3.3. The model is presented for two coupled interconnect lines; however, it can be extended to n coupled lines by changing the dimensions of the matrices. The model is validated with HSPICE in Sect. 3.4 for coupled-two lines and for coupled-three lines in Sect. 3.5. Finally, Sect. 3.6 presents the concluding remarks.

3.2 Motivation

In most of the analysis carried out, the CMOS gate drivers are approximately represented by a resistive drivers while performing the on-chip interconnect analysis [1–3]. The value of the equivalent resistance (R_{eq}) of driver is evaluated by averaging the values at the endpoints of the transition region. Using the Taylor expansion, R_{eq} is expressed as [4]

$$R_{eq} = \frac{3}{4}\frac{V_{\mathrm{DD}}}{I_{\mathrm{DSAT}}}\left(1 - \frac{5}{6}\sigma V_{\mathrm{DD}}\right) \tag{3.1}$$

where σ is the finite drain conductance parameter and I_{DSAT} is drain saturation current.

Figure 3.1 shows two different interconnect structures. First, Fig. 3.1 shows the interconnect lines driven by CMOS inverter and second, Fig. 3.2 shows the interconnect lines driven by resistive driver. In Fig. 3.1, R, C, and L represent per unit length (p.u.l.) line resistance, ground capacitance and line inductance, respectively, and C_{12} and L_{12} represent per unit length (p.u.l.) coupling capacitance and mutual inductance, respectively.

To justify the motivation, the transient response of Figs. 3.1 and 3.2 are compared using HSPICE. For symmetric driving capability of CMOS inverter, the width of PMOS is chosen as twice of NMOS width [4]. The time domain response is performed at 32 nm technology node at the global level interconnect length of 1 mm. The input transition time and supply voltage are considered as 10 ps and 0.9 V, respectively. The dimensions of the interconnect line are considered by the following two assumptions: (1) the space between the two interconnects is equal to the width of interconnect; and (2) the height from the ground plane is equal to the

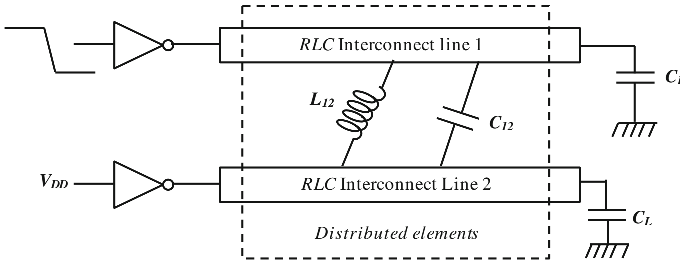

Fig. 3.1 CMOS gate-driven coupled interconnect lines

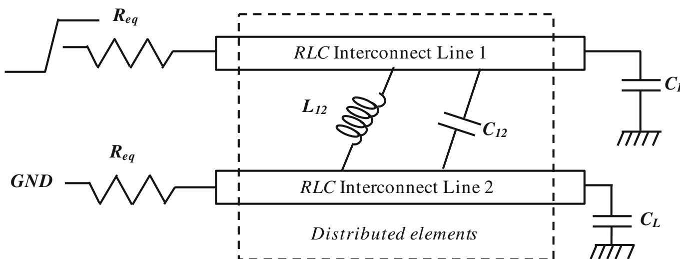

Fig. 3.2 Resistive gate-driven coupled interconnect lines

Table 3.1 Parasitic components of coupled interconnect lines

Line resistance R (kΩ/m)	Line capacitance C (pF/m)	Coupling capacitance C_{12} (pF/m)	Line inductance L (μH/m)	Mutual inductance L_{12} (μH/m)
150	15.11	98.59	1.645	1.484

thickness of the line. The resistivity of the copper material and the relative permittivity of the inter layer dielectric medium are chosen as 2.2 (μΩ-cm) and 2.2, respectively. The interconnect line width and the aspect ratio are considered as 0.22 μm and 3, respectively [12]. For the above-mentioned interconnect dimensions, the associated parasitic values are listed in Table 3.1. The load capacitance C_L is considered as 2 fF.

The transient response comparison of on-chip interconnects using the CMOS driver and the resistive drivers are shown in Figs. 3.3, 3.4, and 3.5. For comprehensive analysis the functional, dynamic in-phase, dynamic out-phase crosstalk conditions are compared and shown in Figs. 3.3, 3.4 and 3.5, respectively. From these figures, a large deviation in the timing response can be observed between the resistive and CMOS gate-driven interconnects. For more clarification, the percentage error is compared while measuring the propagation delay during the dynamic out-phase switching. This error is observed to be as large as 68 %. This corroborates the earlier observations in [5, 10, 13], that the resistive driver model presents inaccurate results for the on-chip interconnect performance.

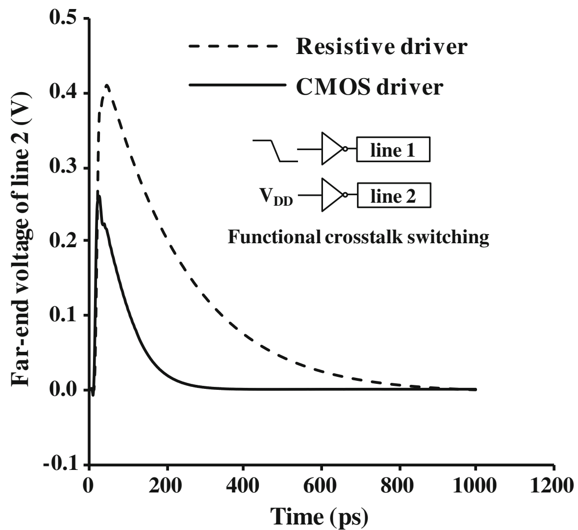

Fig. 3.3 Functional crosstalk transient response of CMOS and resistive drivers

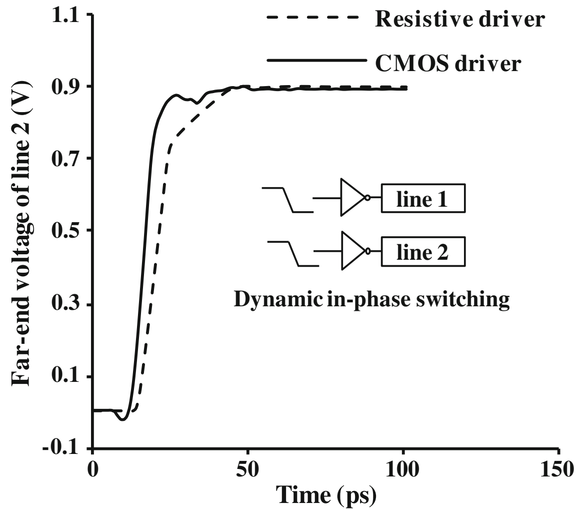

Fig. 3.4 Dynamic in-phase crosstalk transient response of CMOS and resistive drivers

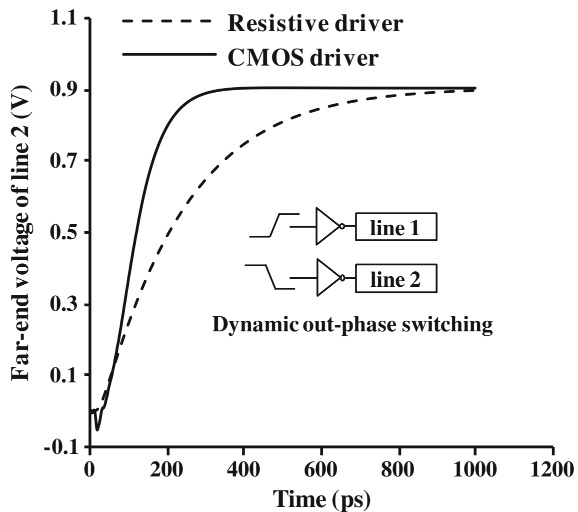

Fig. 3.5 Dynamic out-phase crosstalk transient response of CMOS and resistive drivers

3.3 FDTD Model of CMOS Gate-Driven Cu Interconnects

In this section, the FDTD model is presented for the performance analysis of two coupled interconnects. In a more accurate manner, the nonlinear CMOS driver effects are incorporated in the proposed model using the *n*th power law model. Moreover, the short-channel effects including the velocity saturation and finite drain conductance parameter are also considered in the proposed model.

3.3.1 FDTD Model of Coupled Interconnects

The coupled-two copper interconnect lines driven by CMOS driver is shown in Fig. 3.6, where R is line resistance, L is line inductance, C is line capacitance, and C_L is load capacitance, respectively. The subscripts 1 and 2 represent the parasitic values to the corresponding line 1 and line 2, respectively. All the line parasitic values are mentioned in p.u.l. The time and space along the interconnect line are represented by t and z, respectively.

Using the telegrapher's equations the coupled transmission line equations can be expressed as

$$\frac{\partial}{\partial z}V_1(z,t) + L_1\frac{\partial}{\partial t}I_1(z,t) + L_{12}\frac{\partial}{\partial t}I_2(z,t) + R_1I_1(z,t) = 0 \tag{3.2a}$$

$$\frac{\partial}{\partial z}V_2(z,t) + L_2\frac{\partial}{\partial t}I_2(z,t) + L_{12}\frac{\partial}{\partial t}I_1(z,t) + R_2I_2(z,t) = 0 \tag{3.2b}$$

$$\frac{\partial}{\partial z}I_1(z,t) + (C_1 + C_{12})\frac{\partial}{\partial t}V_1(z,t) - C_{12}\frac{\partial}{\partial t}V_2(z,t) = 0 \tag{3.2c}$$

$$\frac{\partial}{\partial z}I_2(z,t) + (C_2 + C_{12})\frac{\partial}{\partial t}V_2(z,t) - C_{12}\frac{\partial}{\partial t}V_1(z,t) = 0 \tag{3.2d}$$

Equations (3.2a)–(3.2d) can be represented in the matrix form as

$$\frac{\mathrm{d}}{\mathrm{d}z}\boldsymbol{V}(z,t) + \boldsymbol{RI}(z,t) + \boldsymbol{L}\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{I}(z,t) = 0 \tag{3.2e}$$

$$\frac{\mathrm{d}}{\mathrm{d}z}\boldsymbol{I}(z,t) + \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{CV}(z,t) = 0 \tag{3.2f}$$

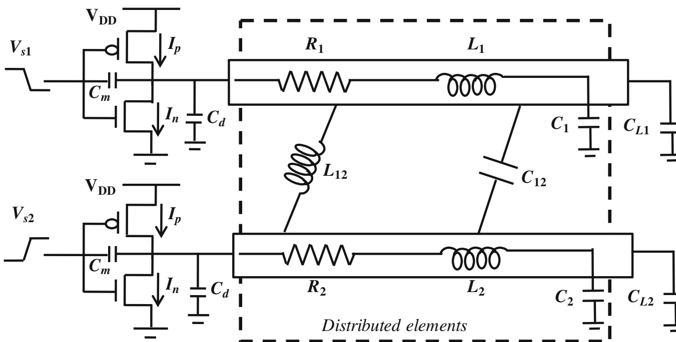

Fig. 3.6 Coupled-two interconnect lines driven by CMOS inverter

where the voltages and currents are expressed in a 2 × 1 column vectors and the line parasitic are expressed in 2 × 2 matrices as shown below

$$\boldsymbol{V} = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \ \boldsymbol{I} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \ \boldsymbol{R} = \begin{bmatrix} R_1 & 0 \\ 0 & R_2 \end{bmatrix}, \ \boldsymbol{L} = \begin{bmatrix} L_1 & L_{12} \\ L_{12} & L_2 \end{bmatrix} \text{ and}$$
$$\boldsymbol{C} = \begin{bmatrix} C_1 + C_{12} & -C_{12} \\ -C_{12} & C_2 + C_{12} \end{bmatrix}.$$

Equations (3.2e) and (3.2f) can be solved using the central difference approximation method. However, the results shows better accuracy if the $\boldsymbol{V}$ and $\boldsymbol{I}$ points are separated in space location by half of the space discretization, i.e., $\Delta z/2$. In a similar manner, the $\boldsymbol{V}$ and $\boldsymbol{I}$ points are separated in time location by half of the time discretization, i.e., $\Delta t/2$. This information can also be visualized in Fig. 3.7.

The interconnect line is driven by the nonlinear CMOS driver at the near-end boundary ($z = 0$) and terminated by a capacitive load at the far-end boundary ($z = l$). The discretized solution points of $\boldsymbol{V}$ and $\boldsymbol{I}$ along the line are shown in Fig. 3.8, where the Nz represents the number of space segments that can be derived from $Nz = l/\Delta z$.

Applying the finite-difference approximations from Fig. 3.7, Eqs. (3.2e) and (3.2f) can be solved as

$$\frac{\boldsymbol{V}_{k+1}^{n+1} - \boldsymbol{V}_k^{n+1}}{\Delta z} + \boldsymbol{L}\frac{\boldsymbol{I}_k^{n+3/2} - \boldsymbol{I}_k^{n+1/2}}{\Delta t} + \boldsymbol{R}\frac{\boldsymbol{I}_k^{n+3/2} + \boldsymbol{I}_k^{n+1/2}}{2} = 0 \tag{3.3a}$$

$$\boldsymbol{I}_k^{n+3/2} = \boldsymbol{B}\boldsymbol{D}\boldsymbol{I}_k^{n+1/2} + \boldsymbol{B}\left(\boldsymbol{V}_k^{n+1} - \boldsymbol{V}_{k+1}^{n+1}\right) \text{ for } k = 1, 2, \ldots\ldots, Nz \tag{3.3b}$$

where $\boldsymbol{B} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{L} + \frac{\Delta z}{2}\boldsymbol{R}\right]^{-1}$, $\boldsymbol{D} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{L} - \frac{\Delta z}{2}\boldsymbol{R}\right]$

$$\frac{\boldsymbol{I}_k^{n+1/2} - \boldsymbol{I}_{k-1}^{n+1/2}}{\Delta z} + \boldsymbol{C}\frac{\boldsymbol{V}_k^{n+1} - \boldsymbol{V}_k^n}{\Delta t} = 0 \tag{3.4a}$$

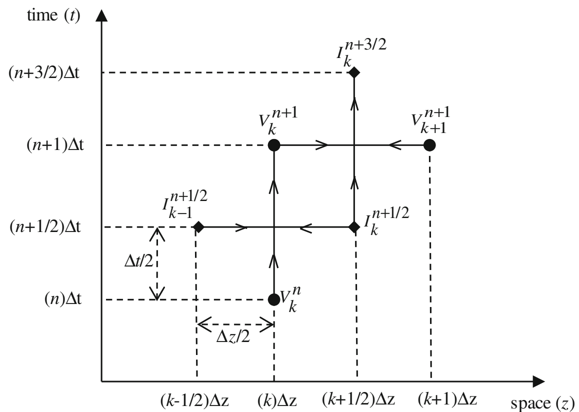

Fig. 3.7 Spatial and time discretization of FDTD technique to achieve second order accuracy

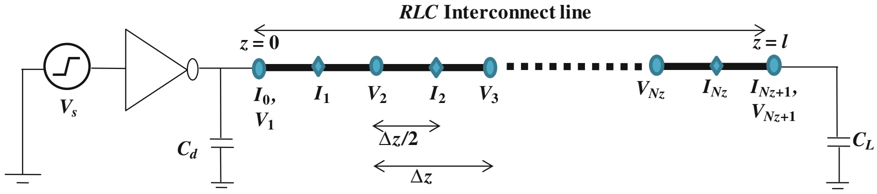

Fig. 3.8 Space discretization of FDTD technique on the interconnect line

$$\boldsymbol{V}_k^{n+1} = \boldsymbol{V}_k^n + \boldsymbol{A}\left(\boldsymbol{I}_{k-1}^{n+1/2} - \boldsymbol{I}_k^{n+1/2}\right) \quad \text{for } k = 2, 3, \ldots\ldots, Nz \tag{3.4b}$$

where $\boldsymbol{A} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{C}\right]^{-1}$.

Here, it can be noticed that the calculations are interleaved in both space and time. For example, in (3.3b) the updated value of $\boldsymbol{I}$ is calculated from the past value of $\boldsymbol{I}$ and the most recent values of $\boldsymbol{V}$. The vectors of $\boldsymbol{V}$ and $\boldsymbol{I}$ are represented as

$$\boldsymbol{V}_i^j = \boldsymbol{V}[i\Delta z,\ j\Delta t]\ ,\quad \boldsymbol{I}_i^j = \boldsymbol{I}[(i+1/2)\Delta z,\ j\Delta t] \tag{3.5}$$

3.3.2 Incorporation of Boundary Constraints

This section discusses the incorporation of nonlinear CMOS driver effects in the FDTD model. At near-end boundary, the voltage and current points are denoted by $\boldsymbol{V}_1$ and $\boldsymbol{I}_0$, respectively. From Fig. 3.8, it can be noted that the space discretization between the current values $\boldsymbol{I}_0$ and $\boldsymbol{I}_1$ is $\Delta z/2$. Therefore, at $k = 1$ Eq. (3.4b) becomes

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{V}_1^n + 2\boldsymbol{A}\left[\boldsymbol{I}_0^{n+1/2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{3.6a}$$

In Eq. (3.6a), the source current $\boldsymbol{I}_0$ at $(n + (1/2))$ time interval is obtained by averaging the values at n and $n + 1$, then the Eq. (3.6a) becomes

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{V}_1^n + 2\boldsymbol{A}\left[\frac{\boldsymbol{I}_0^{n+1} + \boldsymbol{I}_0^n}{2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{3.6b}$$

here, $\boldsymbol{I}_0$ represents the driving current of the CMOS. Using the KCL at near-end boundary, the driving current can be expressed as

$$\boldsymbol{I}_0 = \boldsymbol{C}_m\left[\frac{\mathrm{d}(\boldsymbol{V}_s - \boldsymbol{V}_1)}{\mathrm{d}t}\right] + \boldsymbol{I}_p - \boldsymbol{I}_n - \boldsymbol{C}_d\frac{\mathrm{d}\boldsymbol{V}_1}{\mathrm{d}t} \tag{3.7}$$

where $\boldsymbol{C_m}$ and $\boldsymbol{C_d}$ are the drain to gate coupling capacitance and drain diffusion capacitance, respectively. The PMOS and NMOS currents are represented by $\boldsymbol{I_p}$ and $\boldsymbol{I_n}$, respectively. These currents can be expressed using the *n*th power law model as [11]

$$\boldsymbol{I_p} = \begin{cases} 0 & \boldsymbol{V}_S \geq V_{\mathrm{DD}} - |V_{\mathrm{Tp}}| & \text{(cutoff)} \\ \boldsymbol{I}_{\mathrm{DSATp}(1+\sigma_p(V_{\mathrm{DD}}-\boldsymbol{V}_1))}\left(2 - \frac{V_{\mathrm{DD}}-\boldsymbol{V}_1}{\boldsymbol{V}_{\mathrm{DSATp}}}\right)\frac{V_{\mathrm{DD}}-\boldsymbol{V}_1}{\boldsymbol{V}_{\mathrm{DSATp}}} & \boldsymbol{V}_1 > V_{\mathrm{DD}} - \boldsymbol{V}_{\mathrm{DSATp}} & \text{(lin)} \\ \boldsymbol{I}_{\mathrm{DSATp}(1+\sigma_p(V_{\mathrm{DD}}-\boldsymbol{V}_1))} & \boldsymbol{V}_1 \leq V_{\mathrm{DD}} - \boldsymbol{V}_{\mathrm{DSATp}} & \text{(sat)} \end{cases} \tag{3.8a}$$

$$\boldsymbol{I}_n = \begin{cases} 0 & \boldsymbol{V}_S \leq V_{\mathrm{Tn}} & \text{(cutoff)} \\ \boldsymbol{I}_{\mathrm{DSATn}}(1+\sigma_n \boldsymbol{V}_1)\left(2 - \frac{\boldsymbol{V}_1}{\boldsymbol{V}_{\mathrm{DSATn}}}\right)\frac{\boldsymbol{V}_1}{\boldsymbol{V}_{\mathrm{DSATn}}} & \boldsymbol{V}_1 < \boldsymbol{V}_{\mathrm{DSATn}} & \text{(lin)} \\ \boldsymbol{I}_{\mathrm{DSATn}}(1+\sigma_n \boldsymbol{V}_1) & \boldsymbol{V}_1 \geq \boldsymbol{V}_{\mathrm{DSATn}} & \text{(sat)} \end{cases} \tag{3.8b}$$

where V_{DSAT}, V_{T}, I_{DSAT}, and σ are the drain saturation voltage, drain saturation current, threshold voltage, finite drain conductance parameter. The subscripts of *p* and *n* represent the PMOS and NMOS, respectively. The V_{DSAT} and I_{DSAT} are expressed as

$$\boldsymbol{V}_{\mathrm{DSATp}} = K_p\left(V_{\mathrm{DD}} - \boldsymbol{V}_S - |V_{\mathrm{Tp}}|\right)^{m_p} \tag{3.8c}$$

$$\boldsymbol{V}_{\mathrm{DSATn}} = K_n(\boldsymbol{V}_S - V_{\mathrm{Tn}})^{m_n} \tag{3.8d}$$

$$\boldsymbol{I}_{\mathrm{DSATp}} = \frac{W_p}{L_{\mathrm{eff}}} B_p\left(V_{\mathrm{DD}} - \boldsymbol{V}_S - |V_{\mathrm{Tp}}|\right)^{s_p} \tag{3.8e}$$

$$\boldsymbol{I}_{\mathrm{DSATn}} = \frac{W_n}{L_{\mathrm{eff}}} B_n(\boldsymbol{V}_S - V_{\mathrm{Tn}})^{s_n} \tag{3.8f}$$

The parameters *s* and *B* control the saturation region while *m* and *K* control the linear region characteristics. The width and effective channel length of MOSFET is represented by *W* and L_{eff}, respectively. Using [11], the model parameters can be computed and the values are listed in Table 3.2.

Table 3.2 MOS parameters at 32 nm technology node

Parameter	NMOS	PMOS
m	0.211	0.087
s	0.915	1.07
B	3.55×10^{-5}	0.801×10^{-5}
K	0.369	0.316
σ	0.867	3.11
V_{T}	0.36	0.366

The source current $\boldsymbol{I}_0$ can be discretized as:

$$\boldsymbol{I}_0^{n+1} = C_m \frac{\boldsymbol{V}_s^{n+1} - \boldsymbol{V}_s^n}{\Delta t} + \boldsymbol{I}_p^{n+1} - \boldsymbol{I}_n^{n+1} - (\boldsymbol{C}_m + \boldsymbol{C}_d) \frac{\boldsymbol{V}_1^{n+1} - \boldsymbol{V}_1^n}{\Delta t} \tag{3.9}$$

Using (3.9) and (3.6b)

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{V}_1^n + \boldsymbol{EA}\left[\frac{\boldsymbol{C}_m}{\Delta t}(\boldsymbol{V}_s^{n+1} - \boldsymbol{V}_s^n) + \boldsymbol{I}_0^n\right] - 2\boldsymbol{EAI}_1^{n+1/2} + \boldsymbol{EA}\left(\boldsymbol{I}_p^{n+1} - \boldsymbol{I}_n^{n+1}\right) \tag{3.10}$$

where $\boldsymbol{E} = \left[\boldsymbol{U} + \frac{\boldsymbol{A}}{\Delta t}(\boldsymbol{C_m} + \boldsymbol{C_d})\right]^{-1}$ and $\boldsymbol{U}$ is identity matrix.

At the far-end boundary, the voltage and current equations can be derived as follows:

Using Eq. (3.4b), the output voltage becomes

$$\boldsymbol{V}_{Nz+1}^{n+1} = \boldsymbol{V}_{Nz+1}^n + 2\boldsymbol{A}\left(\boldsymbol{I}_{Nz}^{n+1/2} - \frac{\boldsymbol{I}_{Nz+1}^{n+1} + \boldsymbol{I}_{Nz+1}^n}{2}\right) \tag{3.11}$$

For a capacitive load $\boldsymbol{C}_L$, the output current is expressed as

$$\boldsymbol{I}_{Nz+1} = \boldsymbol{C}_L \frac{\mathrm{d}}{\mathrm{d}t} \boldsymbol{V}_{Nz+1} \tag{3.12a}$$

Equation (3.12a) is discretized as

$$\boldsymbol{I}_{Nz+1}^{n+1} = \boldsymbol{C}_L \frac{\left(\boldsymbol{V}_{Nz+1}^{n+1} - \boldsymbol{V}_{Nz+1}^n\right)}{\Delta t} \tag{3.12b}$$

Using (3.11) and (3.12b)

$$\boldsymbol{V}_{Nz+1}^{n+1} = \boldsymbol{V}_{Nz+1}^n + 2\boldsymbol{FA}\left[\boldsymbol{I}_{Nz}^{n+1/2} - \frac{\boldsymbol{I}_{Nz+1}^n}{2}\right] \tag{3.13}$$

where $\boldsymbol{F} = \left[\boldsymbol{U} + \frac{\boldsymbol{AC}_L}{\Delta t}\right]^{-1}$.

The voltage and current expressions are evaluated in a bootstrapping fashion. First, the voltages are evaluated at a fixed time using Eqs. (3.10), (3.4b), and (3.13). Second, the currents are evaluated from (3.9), (3.3b), and (3.13). However, in order to get the stable output, the maximum value of time step must be less than $\Delta z/v$. It is worth noting that the boundary conditions are implicitly derived and interconnect line equations are explicitly derived. Therefore, there is no stability issue at the boundaries and stability of the driver-interconnect-line system is completely determined by the interconnect line. The proposed model is derived for the two coupled interconnect lines. For extended coupled interconnect lines, these equations remain

valid except the changes in the matrix dimensions. For instance, to model the coupled-three interconnect lines, the interconnect parasitic values have to be mentioned in 3 × 3 order and voltage and current values should be derived in 3 × 1 order.

3.4 Validation of the Model

The two coupled interconnect lines are considered for the validation of the proposed model. The results of the proposed are compared against the industry HSPICE simulation results. Using the similar simulation environment as described in Sect. 3.2, the following interconnect parasitic values are used in the simulations

$$R = \begin{bmatrix} 150 & 0 \\ 0 & 150 \end{bmatrix} \frac{\text{k}\Omega}{\text{m}}, \quad L = \begin{bmatrix} 1.645 & 1.484 \\ 1.484 & 1.645 \end{bmatrix} \frac{\mu\text{H}}{\text{m}}, \text{ and}$$

$$C = \begin{bmatrix} 113.7 & -98.59 \\ -98.59 & 113.7 \end{bmatrix} \frac{\text{pF}}{\text{m}}$$

For the above parasitic values, the signal mode velocities of a lossless interconnect line are $v_{m1} = 1.4 \times 10^8$ m/s and $v_{m2} = 1.7 \times 10^8$ m/s. Using the break frequency of 3.1×10^{10} Hz, the minimum space discretization is calculated as 4.5×10^{-4} m. Based on the CFL condition, the time discretization is obtained to be less than 2.67×10^{-12} s, for a larger mode velocity, v_{m2} [6]. The rise and fall transition of the input signal is assumed to be 10 ps. In the two coupled interconnect lines, line 2 is considered as victim line and accordingly all the performance parameters such as propagation delay, noise peak voltage and its timing instances are evaluated on the victim line 2.

The functional crosstalk analysis is studied by switching the aggressor line 1 and keeping the victim line 2 in quiescent mode [14]. Later on, dynamic crosstalk analysis is studied by switching both aggressor and victim lines either in in-phase or out-phase. In all these cases, the transient responses at far-end of the victim line are compared and shown in Figs. 3.9, 3.10 and 3.11. From these figures, it can be observed that the proposed model accurately captures the timing response in all switching cases, whereas the model presented in [10] is unable to capture the response accurately. This is due to the fact that the model presented in [10] ignores the drain conductance parameter and the current in saturation region is assumed to be independent of drain voltage.

To test the robustness of the proposed model, the percentage errors are calculated while measuring the crosstalk-induced peak voltage and its timing instances [15]. The percentage error is calculated with respect to the HSPICE simulation results. For comparison with the existing models, the model in [10] is also considered as a reference. The peak voltage values and timing instants are shown in Tables 3.3 and 3.4, respectively. From these tables, it has been observed that the average errors using proposed model and model in [10] are 1.5 and 14 %, respectively with respect to the HSPICE simulations.

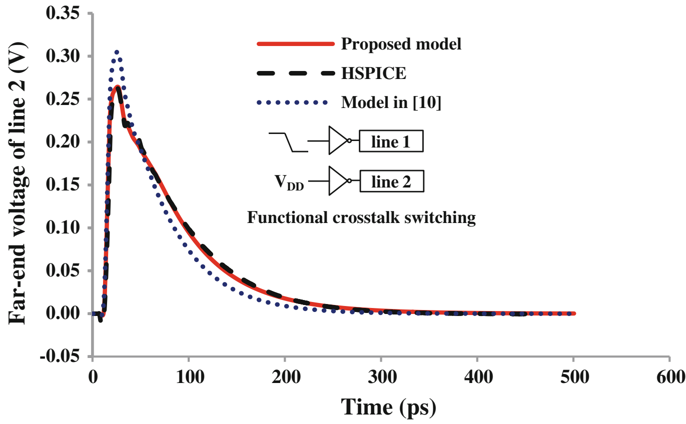

Fig. 3.9 Comparison of functional crosstalk transient response of line 2

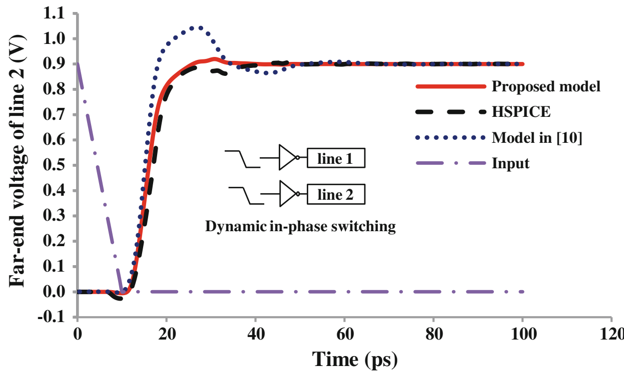

Fig. 3.10 Comparison of dynamic in-phase transient response of line 2

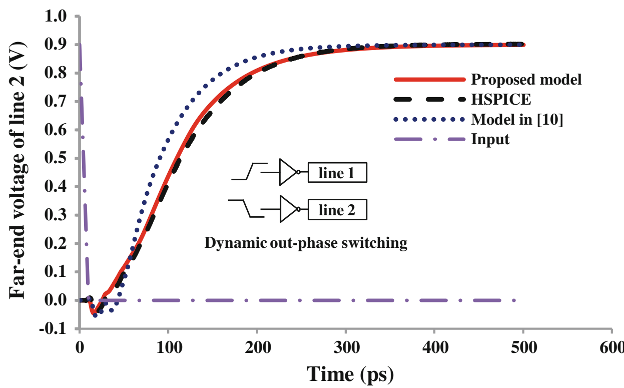

Fig. 3.11 Comparison of dynamic out-phase transient response of line 2

Table 3.3 Comparison of computational error involved in peak noise voltage using HSPICE and proposed model

Input transition time (T_r) (ps)	Peak voltage				
	Proposed model (V)	Li et al. model [10] (V)	HSPICE (V)	% error proposed model	% error [10]
10	0.26	0.30	0.26	0.0	−15.3
30	0.25	0.29	0.24	−4.1	−20.8
50	0.23	0.27	0.22	−4.5	−22.7
70	0.21	0.24	0.21	0.0	−14.2
90	0.20	0.22	0.2	0.0	−10.0

Table 3.4 Computational of computational error involved in peak voltage timing using HSPICE and proposed model

Input transition time (T_r) (ps)	Peak voltage timing				
	Proposed model (ps)	Li et al. model [10] (ps)	HSPICE (ps)	% error propoposed model	% error [10]
10	25.90	26.40	25.74	−0.6	−2.5
30	39.30	28.80	40.89	3.8	29.5
50	59.10	58.40	60.39	2.1	3.3
70	78.80	75.70	79.39	0.7	4.6
90	98.70	90.10	98.89	0.1	8.8

The propagation delay is also compared between the proposed model and the model presented in [10]. Figure 3.12 shows the propagation delay comparison for different values of input transition timings. From Fig. 3.12, it can be observed that the delay during the out-phase transition is higher than the in-phase transition delay.

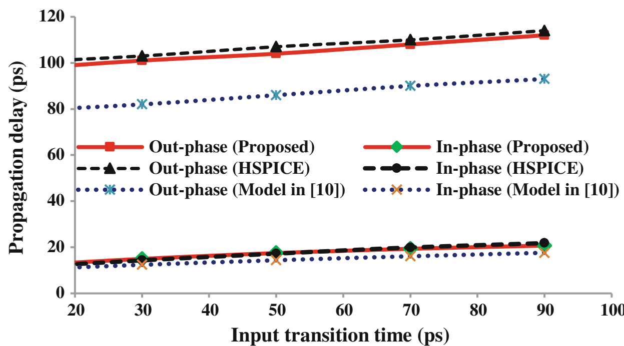

Fig. 3.12 Propagation delay variation with transition time

It is due to the effect of Miller capacitance. Moreover, it has been observed that the proposed model captures the delay accurately during both in-phase and out-phase transitions. The average error is observed to be less than 3 %, whereas using [10] the average error is as high as 17 %.

3.5 Extended Three Coupled Interconnect Lines

In this section, the three coupled interconnect lines are analyzed using the proposed model. The three coupled interconnects that are driven by the CMOS driver is shown in the Fig. 3.13. Similar to the two coupled interconnect lines, the input rise and fall transitions are considered as 10 ps and load capacitance is considered as 2 fF. The following interconnect parasitic values are used in the simulations:

$$R = \begin{bmatrix} 150 & 0 & 0 \\ 0 & 150 & 0 \\ 0 & 0 & 150 \end{bmatrix} \frac{\text{k}\Omega}{\text{m}}, \; L = \begin{bmatrix} 1.645 & 1.484 & 1.264 \\ 1.484 & 1.645 & 1.484 \\ 1.264 & 1.484 & 1.645 \end{bmatrix} \frac{\mu\text{H}}{\text{m}} \text{ and}$$

$$C = \begin{bmatrix} 113.7 & -98.59 & 0 \\ -98.59 & 212.29 & -98.59 \\ 0 & -98.59 & 113.7 \end{bmatrix} \frac{\text{pF}}{\text{m}}$$

From the values of capacitance, the coupling capacitance between the lines 1 and 3, C_{13} can be safely neglected because of the shielding of line 2 [3]. In the three coupled interconnect line system, line 1 and line 3 are considered as aggressor lines and line 2 is considered as victim line. The transient responses at the far-end terminal of the victim line are compared at different switching cases and shown in Fig. 3.14. It can be observed that in all switching cases, the proposed model provides the timing responses as accurate as that of HSPICE.

The percentage error involved while measuring the propagation delay on victim line 2 at different switching cases is shown in Table 3.5. The percentage error is calculated with reference to the HSPICE simulations. From Table 3.5, it has been

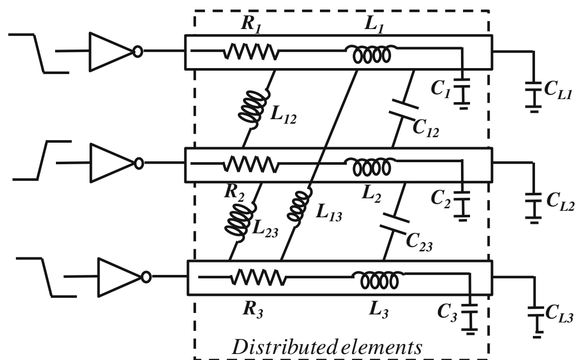

Fig. 3.13 CMOS gate-driven three coupled interconnect lines

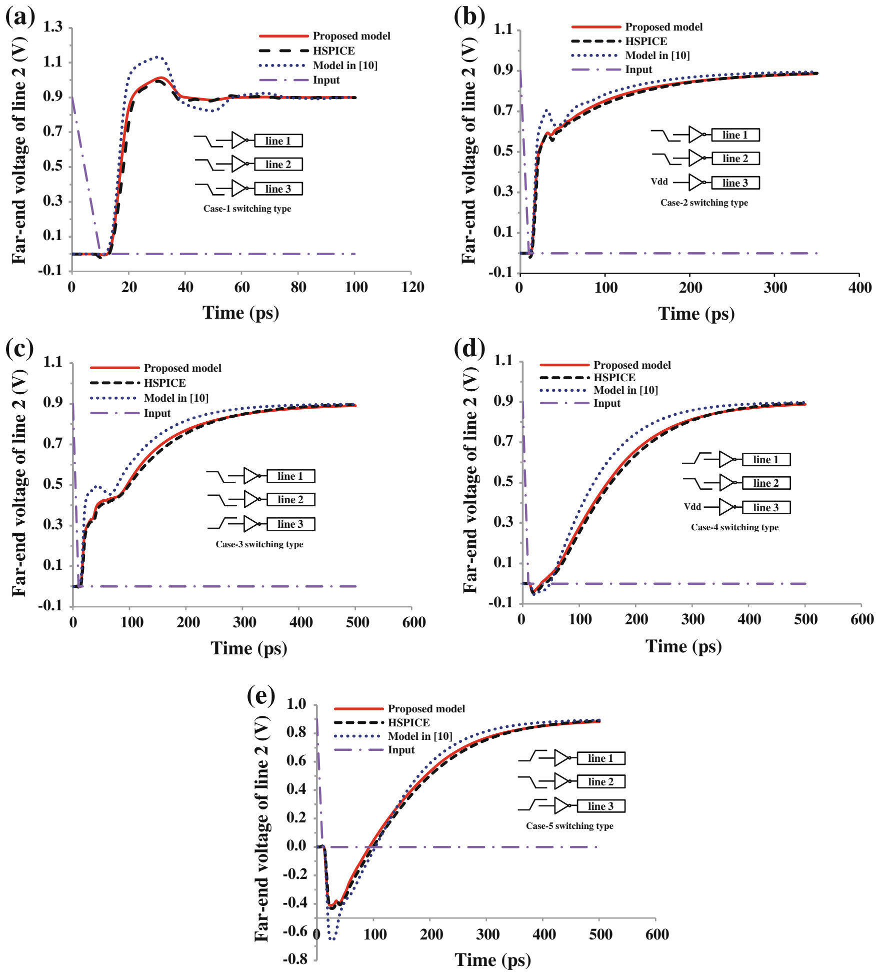

Fig. 3.14 Comparison of transient response on victim line 2 during **a** case-1, **b** case-2, **c** case-3, **d** case-4, and **e** case-5 input switching modes

Table 3.5 Comparison of percentage error involved for propagation delay on victim line 2

Input switching modes				Propagation delay on victim line 2				
Case-mode	Line 1 (agg.)	Line 2 (vic.)	Line 3 (agg.)	Proposed model (ps)	Li et al. model [10] (ps)	HSPICE (ps)	% error proposed model	% error [10]
Case-1	1 → 0	1 → 0	1 → 0	12.1	11.5	12.7	4.7	9.4
Case-2	1 → 0	1 → 0	V_{DD}	15	13.8	15.7	4.4	12.1
Case-3	1 → 0	1 → 0	0 → 1	78.1	20.9	79.6	1.8	73.7
Case-4	0 → 1	1 → 0	V_{DD}	133	111	138.4	3.9	19.8
Case-5	0 → 1	1 → 0	0 → 1	174.9	164.7	181.4	3.5	9.2

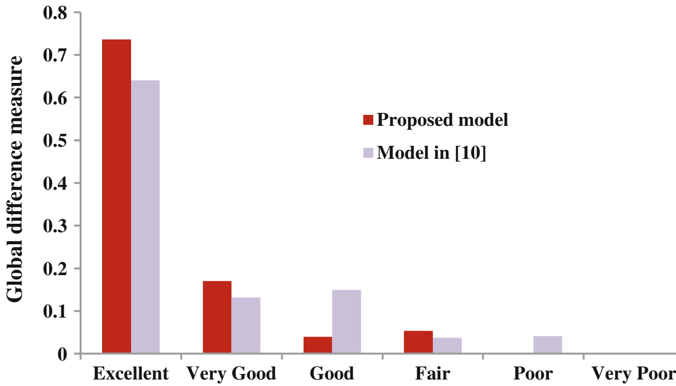

Fig. 3.15 Histogram forms the datasets of Fig. 3.14a using FSV tool

observed that the average error using the proposed model is 4 % and using the model presented in [10] is 24 %. It is also observed that the propagation delay increases with increasing the case mode. The propagation delay changes by more than one order from case-1 mode to case-5 mode switching. It is due to the Miller capacitance that highly influences the effective capacitance value when two lines are switching oppositely. Accordingly, for three coupled lines the case-5 is the worst case switching scenario, if the line 2 is considered as a victim.

Lastly, in order to make a quality of the comparison the data values of the Fig. 3.14a are changed to the natural language descriptor using the feature selective validation (FSV) tool [16–18]. Based on the global difference measure (GDM), the quality of the comparison can be of different types such as excellent, very good, good, fair, poor, and very poor. The result of the FSV tool is shown in Fig. 3.15. The result describes that the proposed model is as accurate as that of HSPICE.

3.6 Summary

This chapter presented an accurate FDTD model for the crosstalk-induced performance analysis of on-chip interconnects. In a more realistic manner, the nonlinear CMOS driver effects are incorporated in the proposed model. The finite drain conduction parameter is also incorporated to improve the accuracy. The boundary conditions at the interface are derived in an implicit manner and therefore the stability of the FDTD solution is strictly followed by the Courant condition. The results of the proposed model are compared with the HSPICE simulations. The comparison results show that the model captures the timing response, propagation delay, and peak voltage quite well. The proposed model is applicable to asymmetric drivers and line configurations as well.

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Chapter 4
FDTD Model for Crosstalk Analysis of Multiwall Carbon Nanotube (MWCNT) Interconnects

Abstract This chapter introduces an equivalent single conductor (ESC) model of MWCNT interconnects. Based on the ESC model, this chapter presents an accurate FDTD model of MWCNT while incorporating the quantum effects of nanowire and nonlinear effects of CMOS driver. To reduce the computational effort required for analyzing the CMOS driver, a simplified but accurate model is employed named as modified alpha-power law model.

Keywords Crosstalk · Equivalent *RLC* model · Kinetic inductance · Multiwall carbon nanotube (MWCNT) quantum resistance · Quantum capacitance

4.1 Introduction

The conventional interconnect copper material is unable to meet the requirements of future technology needs, since it suffers from low reliability with downscaling of interconnect dimensions. Moreover, the resistivity of copper increases, due to electron-surface scattering and grain boundary scattering with smaller dimensions. Therefore, researchers are forced to find an alternative material for global VLSI interconnects. Carbon nanotubes have been proposed to be one of the potential candidates for VLSI interconnects due to their unique physical properties, such as extraordinary mobility, large mean free path, and high current carrying capability [1, 2].

Carbon nanotubes can be classified into single-walled carbon nanotube (SWCNT) and multiwalled carbon nanotube (MWCNT) [3–6]. The promising interconnect solution for global interconnect lengths are MWCNTs due to their high current carrying capabilities than SWCNT bundles. Naeemi et al. observed that for longer interconnects, MWCNTs can have conductivities several times greater than SWCNT bundles [6]. Hence, many researchers consider the MWCNTs as a potential solution for global interconnect material. The experimental and theoretical investigations of MWCNTs as interconnect material have been presented in [7] and [8], respectively.

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The performance of an MWCNT interconnect line is generally evaluated by means of an equivalent transmission line model. Li et al. proposed a multiconductor transmission line (MTL) model to represent the MWCNT interconnect [9]. However, the analysis of MWCNT using the MTL model can be computationally expensive. For this reason, the equivalent single conductor (ESC) model was proposed in [8], using the assumption that voltage at an arbitrary cross section along MWCNT are the same, such that all nanotubes are connected in parallel at the both ends. The accuracy of the ESC model has been verified by several researchers [4, 8, 10]. They observed that the transient responses of ESC model and MTL model are in good agreement.

The FDTD technique has been used widely to analyze the transmission lines due to their better accuracy [11]. However, incorporation of different boundary conditions in the FDTD models is a challenging task. Previously, Paul [12, 13] incorporated the boundary conditions to analyze the transmission lines for resistive driver and resistive load boundaries. However, these studies were focused only on copper interconnects and hence, not suitable for next-generation graphene-based nanointerconnects. The quantum and contact resistances at the near-end and far-end terminals of a nanointerconnect line results in complex boundary conditions. For the first time, Liang et al. [14] proposed a crosstalk noise model for the analysis of MWCNT interconnects using FDTD technique. However, the authors represented the nonlinear CMOS driver by a resistive driver, thus limiting the accuracy of their model. Moreover, they did not validate their proposed model with respect to HSPICE. Therefore, a more accurate model is required that allows a better crosstalk-induced performance estimation of MWCNT interconnects.

The fabrication technique of MWCNT bundles was reported in [15], using thermal chemical vapor deposition technique. The authors have demonstrated the feasibility of growing perfectly aligned carbon nanotube bundles. Recently, Wang et al. [16] fabricated the MWCNTs arrays using microwave plasma chemical vapor deposition on Si substrate with interdigital electrodes. This method is able to control the thickness of MWCNT arrays based on the growth time. Although, the controlled growth of MWCNTs with high CNT density is realizable, the researchers are still facing some challenges in terms of large imperfect metal–nanotube contact resistance, poor control on number of shells, chirality and orientation, higher growth temperature during the fabrication process. However, efforts are underway to fabricate MWCNTs for interconnect applications.

This chapter presents an accurate numerical model for comprehensive crosstalk analysis of coupled MWCNT interconnects based on FDTD method. Using this method, the voltage and current can be accurately estimated at any particular point on the interconnect line. Since the proposed model requires less number of assumptions, the accuracy is very high. The nonlinear CMOS driver effects are incorporated using the modified alpha-power law model with suitable boundary conditions. Using the proposed FDTD method, the functional and dynamic crosstalk analysis is carried out. The results demonstrate that the proposed model has high accuracy that matches closely with the HSPICE results. In addition to this, the proposed model is highly time efficient than the HSPICE. Although, this chapter

demonstrates the crosstalk effects on two coupled interconnect lines, the model can be extended to N lines.

The rest of the chapter is organized as follows: Sect. 4.2 describes the ESC model of an MWCNT. In Sect. 4.3, the FDTD method is developed for coupled MWCNT interconnect lines. Section 4.4 is devoted to the validation of proposed model for coupled-two lines. In Sect. 4.5, the sensitivity analysis is performed to evaluate the validity of the assumptions associated with the proposed model. Finally, Sect. 4.6 concludes this chapter.

4.2 Equivalent Single Conductor Model of the MWCNT Interconnect

This section presents an equivalent *RLC* model of an MWCNT interconnect line. Consider a horizontal MWCNT bundle interconnect line positioned over a ground plane at a distance H and placed in a dielectric medium with dielectric constant ε. The geometry of an MWCNT interconnect is shown in Fig. 4.1. The coupling parasitics between the two MWCNT interconnects is shown in Fig. 4.2, where s is the spacing between the interconnect lines, and l_{12} and c_{12} represent the mutual inductance and coupling capacitance between the interconnect lines, respectively. The MWCNT interconnect consists of N number of tubes

$$N = 1 + \mathrm{int}\left[\frac{(d_N - d_1)}{2\delta}\right] \tag{4.1}$$

where δ, d_1, and d_N represent intershell distance, innermost shell diameter, and outermost shell diameter, respectively.

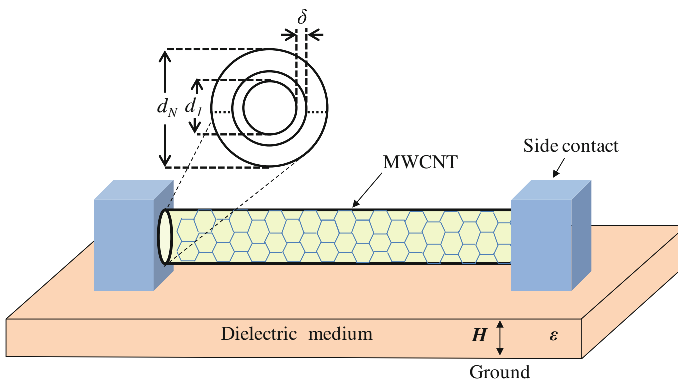

Fig. 4.1 Geometry of an MWCNT interconnect above the ground plane

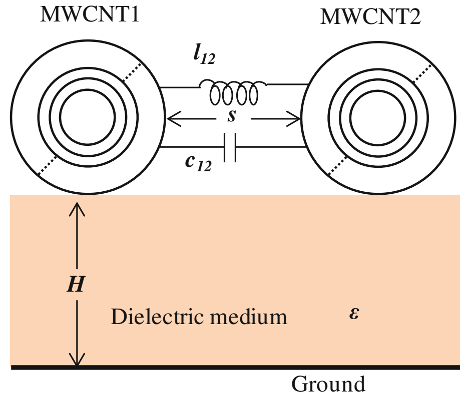

Fig. 4.2 Cross-sectional view and coupling parasitics between the MWCNT interconnects

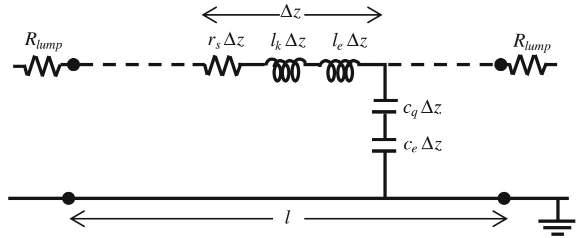

Fig. 4.3 Electrical equivalent model of an MWCNT interconnect

The MWCNT interconnect has been represented by an equivalent single conductor (ESC) model as shown in Fig. 4.3 [8]. The *RLC* parasitics of an MWCNT interconnect are primarily dependent on the number of conducting channels. The number of conducting channels in a CNT can be derived by adding all the subbands contributing to the current conduction. Using Fermi function, it can be expressed as

$$N_{\mathrm{ch},i} = \sum_{\mathrm{subbands}} \frac{1}{\exp(|E_i - E_{\mathrm{F}}|/k_{\mathrm{B}}\,T) + 1} \tag{4.2a}$$

where T is the temperature, k_{B} is the Boltzmann constant, and E_i is the lowest (or highest) energy for the subbands above (or below) the Fermi level E_{F}.

A simplified form of expression (4.2a) is [6]:

$$\begin{aligned} N_{\mathrm{ch},i} &\approx k_1 T d_i + k_2 \qquad d_i > d_{\mathrm{T}}/T \\ &\approx 2/3 \qquad\qquad\quad d_i < d_{\mathrm{T}}/T \end{aligned} \tag{4.2b}$$

where d_i represents the diameter of CNT in an MWCNT, k_1 and k_2 are curve fitted constants. The value of d_{T} (=1300 nm K) is determined by the gap between the subbands and the thermal energy of electrons. The *RLC* parasitics can be extracted a follows:

4.2.1 Resistance

Each shell in the MWCNT primarily demonstrates three different types of resistances: (1) quantum resistance (R_Q) due to the finite conductance value of quantum wire if there is no scattering along the length; (2) imperfect metal–nanotube contact resistance (R_{MC}) that exhibits a value ranging from zero to few kilo-ohms depending on the fabrication process [17–19]; and (3) scattering resistance (r_s) due to acoustic phonon scattering and optical phonon scattering that occurs when the nanotube lengths exceed the mean free path of electrons. The scattering resistance appeared as per unit length distributed resistance along the line, whereas (1) and (2) are considered as lumped resistances placed at the contacts of near-end and far-end terminals. The overall effective lumped resistance at the near-end/far-end terminals of the MWCNT can be expressed as

$$R_{\text{lump,ESC}} = \frac{1}{2}\left[\sum_{i=1}^{N}\left(\frac{R_Q}{2N_{\text{ch},i}} + R_{\text{MC},i}\right)^{-1}\right]^{-1} \quad \text{where} \quad R_Q = \frac{h}{e^2} \approx 25.8\ \text{K}\Omega \tag{4.3a}$$

The p.u.l. scattering resistance of an MWCNT can be expressed as

$$r_{\text{s,ESC}} = \frac{h/e^2}{\sum_{i=1}^{N} 2N_{\text{ch},i}\,\lambda_{\text{mfp},i}} \quad \text{where} \quad \lambda_{\text{mfp},i} = \frac{10^3 d_i}{(T/T_0) - 2},\ T_0 = 100\,\text{K} \tag{4.3b}$$

where h and e represent the Planck's constant and the charge of an electron, respectively.

4.2.2 Inductance

The MWCNT demonstrates two different types of inductances:

(1) Magnetic inductance: The magnetic inductance (l_e) is due to the magnetic field generation around a current-carrying conductor. In the presence of ground plane, the p.u.l. magnetic inductance of a CNT shell shown in Fig. 4.4 is given by [20]

$$l_e = \frac{\mu}{2\pi}\cosh^{-1}\left(\frac{d + 2H}{d}\right) \tag{4.4a}$$

where d and H represent the shell diameter and height from the ground plane, respectively. Additionally, the intershell mutual inductance (l_m) is mainly due to the magnetic field coupling between the adjacent shells in an MWCNT. The p.u.l. l_m can be expressed as [9]

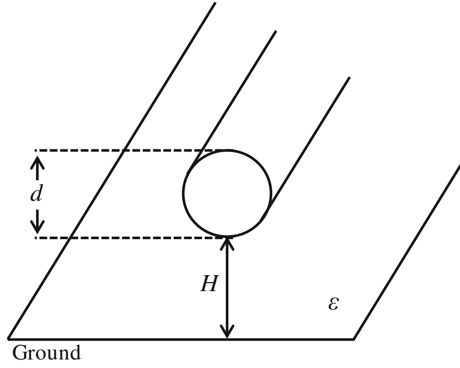

Fig. 4.4 A single CNT shell above a ground plane

$$l_m = \frac{\mu}{2\pi} \ln\left(\frac{d_i}{d_{i-1}}\right) \tag{4.4b}$$

(2) Kinetic inductance: The kinetic inductance (l_k) is mainly due to the kinetic energy of electrons. By equating kinetic energy stored in each conducting channel of a CNT shell to the effective inductance, the kinetic inductance of each conducting channel (l'_k) in a CNT can be expressed as [20]

$$l'_\mathrm{k} = \frac{h}{2e^2 v_\mathrm{F}} \tag{4.4c}$$

where v_F is the Fermi velocity ≈ 8×10^5 m/s [21].

By adopting a recursive approach proposed in [8], the equivalent inductance ($l_\mathrm{k,ESC}$) of Fig. 4.3 can be expressed as

$$l_\mathrm{equ,1} = l_\mathrm{k,1} \tag{4.4d}$$

$$l_\mathrm{equ,i} = \left(\frac{1}{l_{\mathrm{equ},\,i-1} + l_\mathrm{m}^{i-1,\mathrm{i}}} + \frac{1}{l_{\mathrm{k},\,i}}\right)^{-1}, \quad i = 2, 3, \ldots, N \tag{4.4e}$$

$$l_\mathrm{k,ESC} = l_\mathrm{equ,N} \tag{4.4f}$$

where

$$l_m^{i-1,i} = \frac{\mu}{2\pi} \ln(d_i/d_{i-1}), \quad i = 2, 3, \ldots, N \tag{4.4g}$$

$$l_{\mathrm{k},i} = \frac{1}{2N_\mathrm{ch,i}} \frac{h}{2e^2 v_\mathrm{F}} \quad 1 \le i \le N \tag{4.4h}$$

4.2.3 Capacitance

The MWCNT interconnect consists of two types of capacitances:

(1) Electrostatic capacitance: It represents the electrostatic field coupling between the CNT and the ground plane. The electrostatic capacitance (c_e) of MWCNT appears between the external shell and the ground plane, as external shell shields the internal ones. The p.u.l. c_e of a CNT shell shown in Fig. 4.4 can be expressed as [20]

$$c_e = \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{d+2H}{d}\right)} \tag{4.5a}$$

Additionally, the intershell coupling capacitance (c_m) is mainly due to the potential difference between adjacent shells in MWCNT. The p.u.l. c_m can be expressed as [9]

$$c_m = \frac{2\pi\varepsilon}{\ln\left(\frac{d_i}{d_{i-1}}\right)} \tag{4.5b}$$

(2) Quantum capacitance: It originates from the quantum electrostatic energy stored in a CNT shell when it carries current. According to the Pauli exclusion principle, it is only possible to add extra electrons into the CNT shell at an available state above the Fermi level. By equating this energy to the effective capacitance energy, the quantum capacitance of each conducting channel (c'_q) in a CNT can be expressed as

$$c'_q = \frac{2e^2}{hv_F} \tag{4.5c}$$

The distributed line capacitance $c_{q,ESC}$ is expressed in terms of quantum capacitance (c_q) and coupling capacitance (c_m) between shells

$$c_{equ,1} = c_{q,1} \tag{4.5d}$$

$$c_{equ,i} = \left(\frac{1}{c_{equ,i-1}} + \frac{1}{c_m^{i-1,i}}\right)^{-1} + c_{q,i}, \quad i = 2, 3, \ldots, N \tag{4.5e}$$

$$c_{q,ESC} = c_{equ,N} \tag{4.5f}$$

where

$$c_m^{i-1,i} = \frac{2\pi\varepsilon}{\ln(d_i/d_{i-1})}, \quad i = 2, 3, \ldots, N \tag{4.5g}$$

$$c_{\mathrm{q},i} = 2N_{\mathrm{ch},i}\frac{2e^2}{hv_{\mathrm{F}}} \quad 1 \leq i \leq N \tag{4.5h}$$

4.3 FDTD Model of MWCNT Interconnect

The FDTD method is used to model the coupled MWCNT interconnect lines. The coupled-two interconnect lines are analyzed in this section; however, the model can be extended to coupled-N lines with a low computational cost.

4.3.1 The MWCNT Interconnect Line

The coupled-two MWCNT interconnect line structure is shown in Fig. 4.5, where r_{s1}, r_{s2} are the scattering resistances; l_{k1}, l_{k2} are the kinetic inductances; l_{e1}, l_{e2} are the magnetic inductances; c_{q1}, c_{q2} are the quantum capacitances; c_{e1}, c_{e2} are the electrostatic capacitances; and C_{L1}, C_{L2} are the load capacitances of line 1 and line 2, respectively, where all these values are mentioned in p.u.l. The parameters c_{12} and l_{12} are the p.u.l. coupling capacitances and mutual inductances, respectively

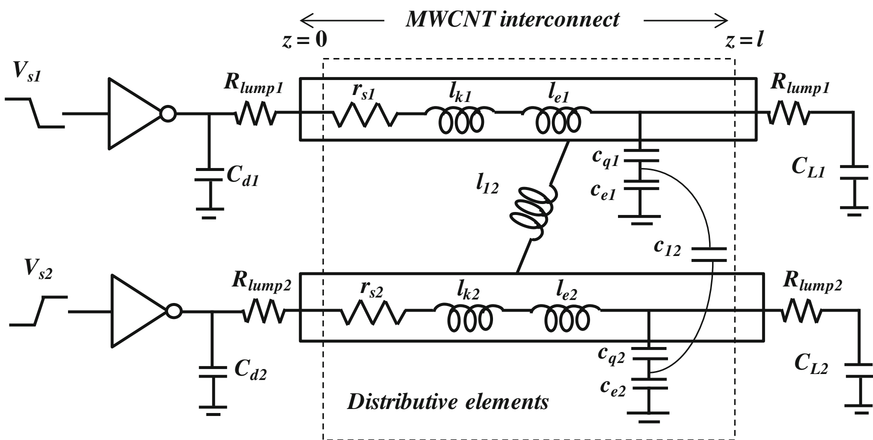

Fig. 4.5 Coupled MWCNT interconnect lines

[22–32]. The position along the interconnect line, and time are denoted as z and t, respectively.

For uniform coupled-two transmission lines the telegrapher's equations in the transverse electromagnetic (TEM) mode [11] are represented as

$$\frac{\mathrm{d}}{\mathrm{d}z}\boldsymbol{V}(z,t)+\boldsymbol{RI}(z,t)+\boldsymbol{L}\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{I}(z,t)=0 \tag{4.6a}$$

$$\frac{\mathrm{d}}{\mathrm{d}z}\boldsymbol{I}(z,t)+\boldsymbol{C}\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{V}(z,t)=0 \tag{4.6b}$$

where $\boldsymbol{V}$ and $\boldsymbol{I}$ are 2×1 column vectors of line voltages and currents, respectively. The line parasitic elements are obtained in 2×2 per unit length matrix form, i.e., $\boldsymbol{V}=\begin{bmatrix}V_1\\V_2\end{bmatrix}$, $\boldsymbol{I}=\begin{bmatrix}I_1\\I_2\end{bmatrix}$, $\boldsymbol{R}=\begin{bmatrix}r_{\mathrm{s1}} & 0\\0 & r_{\mathrm{s2}}\end{bmatrix}$, $\boldsymbol{L}=\begin{bmatrix}l_{\mathrm{k1}}+l_{e1} & l_{12}\\l_{12} & l_{\mathrm{k2}}+l_{e2}\end{bmatrix}$ and $\boldsymbol{C}=\begin{bmatrix}\left(1/c_{\mathrm{q1}}+1/c_{\mathrm{e1}}\right)^{-1}+c_{12} & -c_{12}\\-c_{12} & \left(1/c_{\mathrm{q2}}+1/c_{\mathrm{e2}}\right)^{-1}+c_{12}\end{bmatrix}$.

Central difference approximation is used to analyze the first-order differential Eqs. (4.6a) and (4.6b) by neglecting the higher order terms. This assumption results in a negligibly small loss of accuracy in the estimation of the transient response, since the value of time segment Δt is limited by CFL condition [33]. Using the FDTD method, the analysis of telegrapher's equations shows better accuracy, if the voltage and current points are chosen at the alternate space location and separated by one-half of the position discretization, i.e., $\Delta z/2$ [12]. In the same manner, the solution time for $\boldsymbol{V}$ and $\boldsymbol{I}$ should also be separated by $\Delta t/2$.

The interconnect line of length l is driven by a resistive driver at $z = 0$ and terminated by a capacitive load at $z = l$. The line is discretized into Nz uniform segments of length $\Delta z = l/Nz$. The voltage and current solution points are discretized along the line as shown in Fig. 4.6.

Applying finite difference approximations to (4.6a) results in

$$\frac{\boldsymbol{V}_{k+1}^{n+1}-\boldsymbol{V}_{k}^{n+1}}{\Delta z}+\boldsymbol{L}\frac{\boldsymbol{I}_{k}^{n+3/2}-\boldsymbol{I}_{k}^{n+1/2}}{\Delta t}+\boldsymbol{R}\frac{\boldsymbol{I}_{k}^{n+3/2}+\boldsymbol{I}_{k}^{n+1/2}}{2}=0 \tag{4.7a}$$

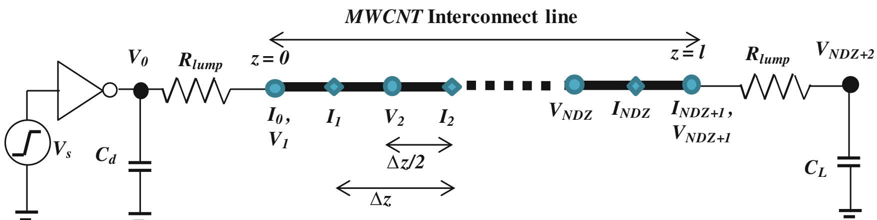

Fig. 4.6 Illustration of space discretization of line for FDTD implementation

$$\boldsymbol{I}_k^{n+3/2} = \boldsymbol{EFI}_k^{n+1/2} + \boldsymbol{E}\left[\boldsymbol{V}_k^{n+1} - \boldsymbol{V}_{k+1}^{n+1}\right] \quad \text{for } k = 1, 2, \ldots, Nz \tag{4.7b}$$

where $\boldsymbol{E} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{L} + \frac{\Delta z}{2}\boldsymbol{R}\right]^{-1}$, $\boldsymbol{F} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{L} - \frac{\Delta z}{2}\boldsymbol{R}\right]$.

Applying finite difference approximations to (4.6b) results in

$$\frac{\boldsymbol{I}_k^{n+1/2} - \boldsymbol{I}_{k-1}^{n+1/2}}{\Delta z} + \boldsymbol{C}\frac{\boldsymbol{V}_k^{n+1} - \boldsymbol{V}_k^{n}}{\Delta t} = 0 \tag{4.8a}$$

$$\boldsymbol{V}_k^{n+1} = \boldsymbol{V}_k^{n} + \boldsymbol{D}\left[\boldsymbol{I}_{k-1}^{n+1/2} - \boldsymbol{I}_k^{n+1/2}\right] \quad \text{for } k = 2, 3, \ldots, Nz \tag{4.8b}$$

where $\boldsymbol{D} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{C}\right]^{-1}$.

4.3.2 Boundary Condition at Near-End Terminal

The voltage and current points at the near-end terminal are represented by $\boldsymbol{V}_1$ and $\boldsymbol{I}_0$, respectively. As indicated in Fig. 4.6, it is observed that to apply the boundary conditions in (4.8b), Δz is replaced by $\Delta z/2$. Therefore, at $k = 1$ Eq. (4.8b) becomes

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{V}_1^{n} + 2\boldsymbol{D}\left[\boldsymbol{I}_0^{n+1/2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{4.9a}$$

The source current $\boldsymbol{I}_0$ at $(n + 1/2)$ time interval is obtained by averaging the source current at (n) and $(n + 1)$ time intervals. Then Eq. (4.9a) becomes

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{V}_1^{n} + 2\boldsymbol{D}\left[\frac{\boldsymbol{I}_0^{n+1} + \boldsymbol{I}_0^{n}}{2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{4.9b}$$

where $\boldsymbol{I}_0$ is the driver current. Applying Kirchhoff's current law (KCL) at near-end terminal, $\boldsymbol{I}_0$ can be written as

$$\boldsymbol{V}_0^{n+1} = \boldsymbol{V}_0^{n} + \boldsymbol{A}\left[\frac{\boldsymbol{C}_m}{\Delta t}\left(\boldsymbol{V}_s^{n+1} - \boldsymbol{V}_s^{n}\right) + \boldsymbol{I}_p^{n+1} - \boldsymbol{I}_n^{n+1} - \boldsymbol{I}_0^{n}\right] \tag{4.9c}$$

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{BV}_1^{n} + 2\boldsymbol{BD}\left[\frac{\boldsymbol{V}_0^{n+1}}{2\boldsymbol{R}_{\text{lump}}} + \frac{\boldsymbol{I}_0^{n}}{2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{4.9d}$$

$$\boldsymbol{I}_0^{n+1} = \frac{1}{\boldsymbol{R}_{\text{lump}}}\left[\boldsymbol{V}_0^{n+1} - \boldsymbol{V}_1^{n+1}\right] \tag{4.9e}$$

where $\boldsymbol{A} = \left[\frac{\boldsymbol{C}_m + \boldsymbol{C}_{\text{d}}}{\Delta t}\right]^{-1}, \boldsymbol{B} = \left[\boldsymbol{U} + \frac{\boldsymbol{D}}{\boldsymbol{R}_{\text{lump}}}\right]^{-1}$ $\boldsymbol{C}_m$ is the drain to gate coupling capacitance, $\boldsymbol{C}_{\text{d}}$ is the drain diffusion capacitance of CMOS inverter, $\boldsymbol{I}_p$ and $\boldsymbol{I}_n$ are the

PMOS and NMOS currents, respectively. The modified alpha-power law model that includes the drain conductance parameter is used to express the NMOS current as

$$\boldsymbol{I}_n = \begin{cases} 0 & \boldsymbol{V}_S \le V_{\text{tn}} \quad \text{(off)} \\ \boldsymbol{K}_{\text{ln}}(\boldsymbol{V}_s - \boldsymbol{V}_{\text{tn}})^{\alpha_n/2}\boldsymbol{V}_0 & \boldsymbol{V}_0 < \boldsymbol{V}_{\text{DSATn}} \quad \text{(lin)} \\ \boldsymbol{K}_{\text{sn}}(\boldsymbol{V}_s - \boldsymbol{V}_{\text{tn}})^{\alpha_n}(1 + \sigma_n\boldsymbol{V}_0) & \boldsymbol{V}_0 \ge \boldsymbol{V}_{\text{DSATn}} \quad \text{(sat)} \end{cases} \tag{4.9f}$$

where K_{ln}, K_{sn}, V_{tn}, α_n, and σ_n are the linear region transconductance parameter, saturation region transconductance parameter, threshold voltage, velocity saturation index, and drain conductance parameter of NMOS, respectively. In a similar manner, the PMOS current can be expressed as

$$\boldsymbol{I}_p = \begin{cases} 0 & \boldsymbol{V}_S \ge \boldsymbol{V}_{\text{DD}} - \left|V_{\text{tp}}\right| \quad \text{(off)} \\ \boldsymbol{K}_{\text{lp}}\left(\boldsymbol{V}_{\text{DD}} - \boldsymbol{V}_s - \left|\boldsymbol{V}_{\text{tp}}\right|\right)^{\alpha_p/2}(\boldsymbol{V}_{\text{DD}} - \boldsymbol{V}_0) & \boldsymbol{V}_0 > \boldsymbol{V}_{\text{DD}} - \boldsymbol{V}_{\text{DSATp}} \quad \text{(lin)} \\ \boldsymbol{K}_{\text{sp}}\left(\boldsymbol{V}_{\text{DD}} - \boldsymbol{V}_s - \left|\boldsymbol{V}_{\text{tp}}\right|\right)^{\alpha_p}\left(1 + \sigma_p(\boldsymbol{V}_{\text{DD}} - \boldsymbol{V}_0)\ \right) & \boldsymbol{V}_0 \le \boldsymbol{V}_{\text{DD}} - \boldsymbol{V}_{\text{DSATp}} \quad \text{(sat)} \end{cases} \tag{4.9g}$$

4.3.3 Boundary Condition at Far-End Terminal

Here the objective is to derive the voltage expression at $k = Nz + 1$ and $Nz + 2$.

At $k = Nz + 1$, Eq. (4.8b) becomes

$$\boldsymbol{V}_{Nz+1}^{n+1} = \boldsymbol{V}_{Nz+1}^{n} + 2\boldsymbol{D}\left(\boldsymbol{I}_{Nz}^{n+1/2} - \frac{\boldsymbol{I}_{Nz+1}^{n+1} + \boldsymbol{I}_{Nz+1}^{n}}{2}\right) \tag{4.10a}$$

Applying KCL at far-end terminal, the output current ($\boldsymbol{I}_{Nz+1}$) can be expressed as

$$\boldsymbol{V}_{Nz+1} - \boldsymbol{V}_{Nz+2} = \boldsymbol{R}_{\text{lump}}\boldsymbol{I}_{Nz+1} \tag{4.10b}$$

The discretized form of (4.10b) is

$$\boldsymbol{I}_{Nz+1}^{n+1} = \frac{1}{\boldsymbol{R}_{\text{lump}}}\left[\boldsymbol{V}_{Nz+1}^{n+1} - \boldsymbol{V}_{Nz+2}^{n+1}\right] \tag{4.10c}$$

Using (4.10a) and (4.10c) the far-end voltage $\boldsymbol{V}_{Nz+1}$ can be expressed as

$$\boldsymbol{V}_{Nz+1}^{n+1} = \boldsymbol{B}\boldsymbol{V}_{Nz+1}^{n} + 2\boldsymbol{B}\boldsymbol{D}\left[\frac{\boldsymbol{V}_{Nz+2}^{n+1}}{2\boldsymbol{R}_{\text{lump}}} + \boldsymbol{I}_{Nz}^{n+1/2} - \frac{\boldsymbol{I}_{Nz+1}^{n}}{2}\right] \tag{4.10d}$$

and the load voltage $\boldsymbol{V}_{Nz+2}$ is

$$\boldsymbol{V}_{Nz+2}^{n+1} = \boldsymbol{V}_{Nz+2}^{n} + \frac{\Delta t}{\boldsymbol{C}_L}\boldsymbol{I}_{Nz+1}^{n} \tag{4.10e}$$

These equations are evaluated in a bootstrapping fashion. Initially, the voltages along the line are evaluated for a specific time from Eqs. (4.9c), (4.9d), (4.8b), (4.10e), and (4.10d) in terms of the previous values of voltage and current. Thereafter, the currents are evaluated from (4.9e), (4.7b), and (4.10c) in terms of these voltages and previous current values.

4.4 Validation of the Model

The coupled MWCNT interconnects are analyzed using the actual CMOS driver. The proposed model is implemented with the MATLAB. The industry standard HSPICE simulations are used for the validation of the results. The HSPICE simulations are carried out using the subcircuit model with 50 distributed segments for interconnect and using BSIM4 technology model for MOSFET. A symmetric CMOS driver is used to drive the interconnect load. The equivalent resistance of the driver is evaluated by averaging the resistance value over an interval when the input is between V_{DD} and $V_{\mathrm{DD}}/2$ [34]. The signal integrity analysis is carried out at the global interconnect length of 1 mm for 32 nm technology and 0.9 V of V_{DD}. The interconnect dimensions are based on the ITRS data [35]. The interconnect width and height from the ground plane are 48 and 110.4 nm, respectively. The spacing between the two interconnects is 48 nm. The relative permittivity of the inter layer dielectric medium is 2.25. The load capacitance and input transition time are 2 fF and 20 ps, respectively. The following *RLC* parasitics are used in the experiments [36–43]:

$$\boldsymbol{R} = \begin{bmatrix} 653.67 & 0 \\ 0 & 653.67 \end{bmatrix} \frac{\mathrm{k\Omega}}{\mathrm{m}}, \quad \boldsymbol{L} = \begin{bmatrix} 14.83 & 0.61 \\ 0.61 & 14.83 \end{bmatrix} \frac{\mathrm{\mu H}}{\mathrm{m}} \quad \text{and}$$

$$\boldsymbol{C} = \begin{bmatrix} 93.33 & -71.50 \\ -71.50 & 93.33 \end{bmatrix} \frac{\mathrm{pF}}{\mathrm{m}}$$

In the interconnect system, lines 1 and 2 are considered as aggressor and victim lines, respectively. For the above-mentioned setup, the transient response is analyzed at the far-end terminal of the victim line using the proposed model, resistive driver-based model [14], and HSPICE simulations using CMOS driver. From Fig. 4.7, it can be observed that the model presented in [14] is unable to capture the timing waveform accurately. However, the proposed model is able to successfully capture the HSPICE waveform characteristics.

The crosstalk-induced delay is analyzed under two different cases. First case considers out-phase delay where the input signals of aggressor and victim lines are

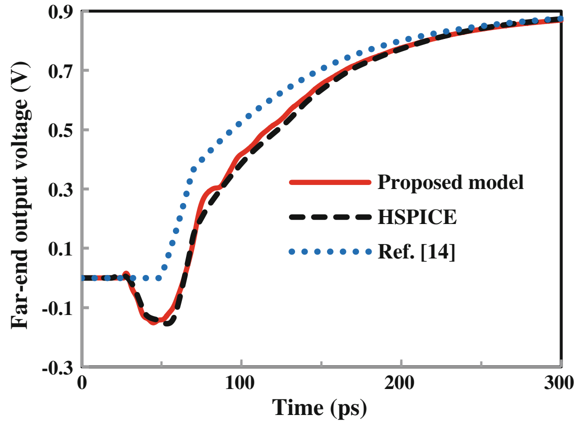

Fig. 4.7 Transient response at the far-end terminal of the victim line when the aggressor and victim lines are switched out-of-phase

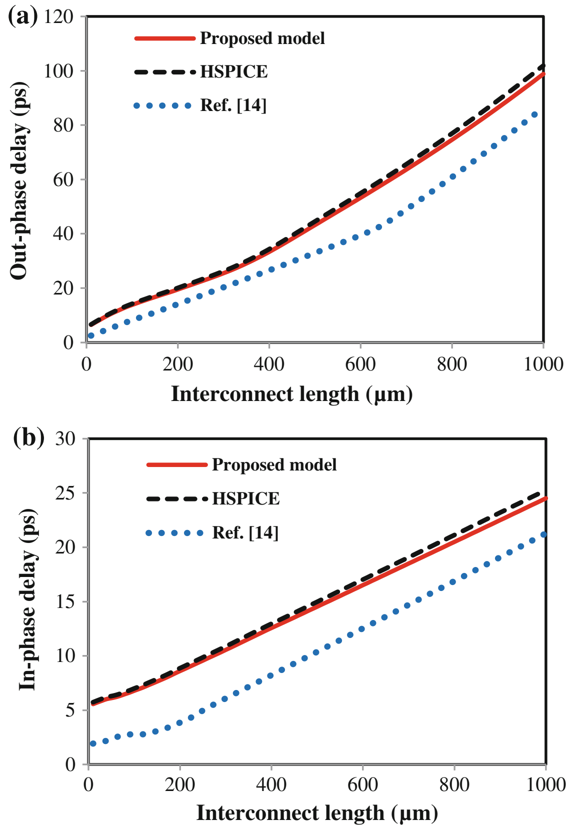

Fig. 4.8 Crosstalk-induced delay comparison **a** out-phase delay and **b** in-phase phase delay with the variation of interconnect length

switched out-of-phase. Second case considers in-phase delay where the input signals of aggressor and victim lines are switched in-phase. Figure 4.8a, b show out-phase and in-phase delay comparison, respectively, for different interconnect

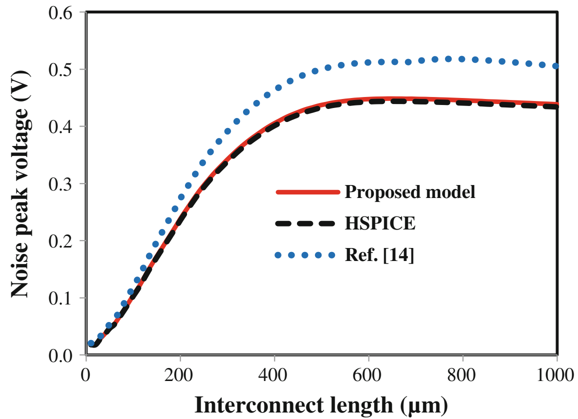

Fig. 4.9 Noise peak voltage comparison of victim line 2 with the variation of interconnect length

lengths. It can be clearly observed that the model proposed in [14], fails to estimate the crosstalk-induced delay for all interconnect lengths. The model proposed in [14] underestimates the delay for both out-phase and in-phase switching by average errors of 27.2 and 35.3 %, respectively.

The functional crosstalk noise is analyzed when the aggressor line is switched and the victim line is kept in quiescent mode. Figure 4.9 depicts the noise peak voltage comparison on the victim line. It can be observed that the resistive driver model [14] overestimates the noise peak voltage, wherein the average error is observed to be 15 %.

To test the robustness, the proposed model is examined at different input transition times. The interconnect length is considered as 500 μm. Figure 4.10 depicts the computational error involved in predicting the crosstalk-induced propagation delay. It can be observed that the proposed model accurately predicts the delay for both out-phase and in-phase transitions. The average error involved is only 1.4 and

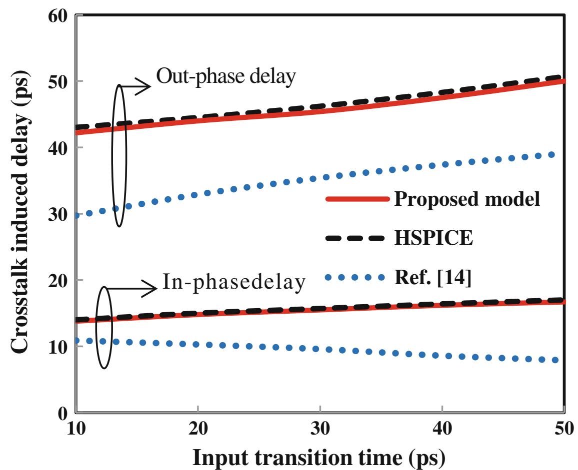

Fig. 4.10 Crosstalk-induced delay comparison on victim line 2 with the variation of input transition time

Table 4.1 CPU runtime comparison between proposed model and HSPICE with 1000 time segments

Number of space segments	HSPICE (s)	Proposed model (s)	% reduction in runtime
1	0.14	0.02	85.71
10	0.68	0.06	91.17
50	2.97	0.23	92.25
100	6.04	0.31	94.86

1.5 % during in-phase and out-phase switching, respectively. Contrastingly, with the resistive driver model [14], the average errors involved are 38.6 and 25.1 % for in-phase and out-phase switching, respectively.

Modified nodal analysis (MNA) is the core approach used in SPICE to formulate the system equations. Applying the Kirchhoff's current law and following the energy conversion principle, the MNA generates the set of matrix equations. The order of the matrix is determined by the number of nodes and unknown variables in the circuit. The unknown variables are solved after the inversion of the matrix and therefore require more computational time. However, the FDTD operator is matrix free and therefore fast and memory efficient as compared to HSPICE simulations.

The efficiency of the proposed model is examined under different test cases. The analysis is carried out by varying the space segment while keeping the time segment constant for coupled interconnects. Using a PC with Intel Dual Core CPU (2.33 GHz, 4 GB RAM), the comparison results are provided in Table 4.1. Using the proposed model, it is observed that the CPU runtime reduces by an average of 91 % in comparison to HSPICE simulations. Additionally, the proposed model is compared with the HSPICE simulations using the same modified alpha-power law model. It is observed that the average CPU runtime reduces by 88 % in comparison to HSPICE simulations.

4.5 Sensitivity Analysis

The primary assumptions made in the proposed work are for: (1) number of conducting channels and (2) contact resistance. This subsection presents the sensitivity analysis to evaluate the validity of these assumptions.

4.5.1 Sensitivity Analysis for Number of Conducting Channels

The number of conducting channels in a CNT can be obtained from expression (4.2b), which is an approximated form of (4.2a). Table 4.2 shows the variations in

Table 4.2 Variation between (4.2a) and (4.2b) on parasitics and crosstalk-induced performance parameters

Variation between (4.2a) and (4.2b)	Parasitic parameter				Performance parameter		
	Lumped resistance (Ω)	Scattering resistance (Ω)	C (fF)	L (pH)	Noise peak voltage (V)	In-phase delay (ps)	Out-phase delay (ps)
From Eq. (4.2a)	11.79	675.10	21.84	15.28	0.433	26.0	64.3
From Eq. (4.2b)	11.43	653.67	21.83	14.83	0.424	25.3	63.6
% change	3.05	3.17	0.04	2.94	2.1	2.6	1.1

parasitics and crosstalk-induced performance parameters using Eqs. (4.2a) and (4.2b). The average percentage change in parasitics and performance parameters are just 2.3 and 2 %, respectively. It can be inferred that the parasitics and crosstalk-induced performance parameters are almost insensitive to the usage of approximated expression for obtaining N_{ch} [44].

4.5.2 Sensitivity Analysis for Contact Resistance

The value of imperfect metal contact resistance can range from the best case value of zero to the worst case value of few kilo-ohms depending on the fabrication process. As reported earlier [9], the R_{MC} value is considered as 3.2 kΩ per shell. However, a sensitivity analysis on parasitic $R_{lump,ESC}$ and crosstalk-induced performance parameters for R_{MC} varying from 0 to 8 kΩ is carried out and the results are presented in Table 4.3. A maximum variation of 5 % in $R_{lump,ESC}$ and almost no change in the crosstalk performance are noticed with the change in R_{MC}. This is due to the fact that the crosstalk-induced performance parameters primarily depend on the scattering resistance and almost insensitive to the change in R_{MC}.

Table 4.3 Variation of performance parameters due to change in R_{MC}

Parasitic parameter		Performance parameter			
R_{MC} (per shell) (k Ω)	Lumped resistance ($R_{lump,ESC}$) (Ω)	Noise peak voltage (V)	Noise peak timing (ps)	In-phase delay (ps)	Out-phase delay (ps)
0	11.20	0.425	54.5	25.1	63.5
2	11.3	0.425	54.4	25.3	63.5
4	11.49	0.424	54.4	25.3	63.6
6	11.63	0.424	54.4	25.4	63.6
8	11.77	0.424	54.4	25.4	63.8

4.6 Summary

This chapter presented an accurate model to analyze the crosstalk effects in coupled MWCNT interconnect lines. The CMOS driver and the coupled MWCNT interconnect are modeled by modified alpha-power law model and FDTD method, respectively. It has been observed that the results of the proposed model exhibit a good agreement with HSPICE simulations. Over the random number of test cases, the average error in the propagation delay measurement is observed to be less than 2 %. Moreover, the sensitivity analysis is performed based on the assumptions used in the proposed model. It is observed that the percentage change in parasitic elements and performance parameters are almost negligible with respect to the assumptions associated with the model. This analysis suggests that with continuous advancements in FDTD technique the proposed model would play a significant role in performance analysis of MWCNT on-chip interconnects and would be potentially incorporated in TCAD simulators.

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Chapter 5
Crosstalk Modeling with Width Dependent MFP in MLGNR Interconnects Using FDTD Technique

Abstract This chapter analyzes the performance of coupled MLGNR interconnects using the FDTD technique. In a more realistic manner, the proposed model incorporates the width dependent MFP parameter of the MLGNR while taking into account the edge roughness. This helps in accurate estimation of the crosstalk-induced performance in comparison to the conventional models. The crosstalk noise is comprehensively analyzed by examining both functional and dynamic crosstalk effects.

Keywords Equivalent single conductor (ESC) model · In-phase and out-phase delay · Mean free path (MFP) · Multilayer graphene nanoribbon (MLGNR) · Propagation delay · Power dissipation

5.1 Introduction

In the first four decades of the semiconductor industry, system performance was entirely dependent on the transistor delay and power dissipation [1]. The technology scaling had an adverse effect on *RLC* delay of complex VLSI circuits as the resistivity increased for the small-dimensional metal interconnects made up of Cu [2]. The reduced cross-sectional area of Cu interconnects resulted in higher resistivity under the effects of enhanced grain and surface scattering. Moreover, with thinner interconnects and higher operating frequency, electromigration-induced problems gained more attention. Presently, at GHz range of frequencies, issues like skin effect, stability, operational bandwidth and crosstalk severely affect the performance of Cu interconnects [3]. Therefore, researchers are forced to find an alternative to Cu material for high-speed global VLSI interconnects [4, 5].

During the recent past, graphene nanoribbons (GNRs) have rapidly gained importance as an emerging material that potentially forms a monolithic system for field effect devices and interconnects [6, 7]. GNR is a sheet of graphite wherein carbon atoms are tightly packed in honeycomb lattice structures [8]. High-quality GNR sheets have long mean free path (MFP) ranging from 1 to 5 μm that results in

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ballistic transport phenomenon. Due to the large MFP, GNRs have higher carrier mobility of 10^5 cm^2/(V·s) and larger current densities, of 10^9 A/cm^2 in comparison to Cu [9]. Due to high intrinsic resistance of single layer GNR, researchers often prefer multilayer GNR (MLGNR) as potential interconnect material [10–12]. Moreover, intercalation doping can increase the in-plane conductivity of MLGNR up to 20 times that involves insertion of one dopant layer between each pair of adjacent graphene layers [8]. Intercalation doping can also increase the MFP due to an increase in spacing between the adjacent layers. Additionally, the easier fabrication process of MLGNR makes it a promising candidate for VLSI interconnect material. The comparison between the performance of MLGNR and Cu has been studied in [13], where the authors observed that MLGNR interconnect demonstrates the smaller propagation delay than Cu interconnect.

Using the equivalent transmission line model, the crosstalk effects of coupled MLGNR have been studied in [14], where the authors considered the MFP parameter independent of width by assuming perfectly smooth edges of MLGNR. However, in reality all GNRs exhibit edge roughness [15, 16]. Due to these rough edges, the electron scattering increases, thereby decreasing the overall MFP and increasing the resistivity [17]. At lower widths, the MFP is predominantly dependent on the edge roughness. Therefore, it is essential to incorporate width dependent MFP while modeling the performance of MLGNR-based interconnects.

This chapter accurately analyzes the performance of MLGNR interconnects based on the finite-difference time-domain (FDTD) technique. In a more realistic manner, the proposed model includes the effect of width dependent MFP of the MLGNR while taking into account the edge roughness. Moreover, a nonlinear CMOS driver is used to drive the MLGNR interconnect line. At different interconnect widths, the crosstalk-induced propagation delay is compared among proposed model, HSPICE, and the existing crosstalk noise model.

The organization of this chapter is as follows: Sect. 5.1 introduces the importance of MLGNR interconnects in current research scenario and briefs about the work carried out. Based on the multiconductor transmission line theory, an equivalent single conductor (ESC) model of MLGNR interconnects is described in Sect. 5.2. Using a driver-interconnect-load system, a comparative analysis of transient response of MTL and ESC models is also presented in this section. Section 5.3 brief the FDTD model for the MLGNR interconnects. The validation of the proposed model is discussed in Sect. 5.4 along with the performance comparison between Cu and MLGNR interconnects. Section 5.5 concludes this chapter.

5.2 Equivalent Single Conductor Model of the MLGNR Interconnect

The proposed model is developed for MLGNR interconnect line positioned over a ground plane at a distance H with a dielectric medium sandwiched between GNRs as shown in Fig. 5.1. The MLGNR consists of N number of layers

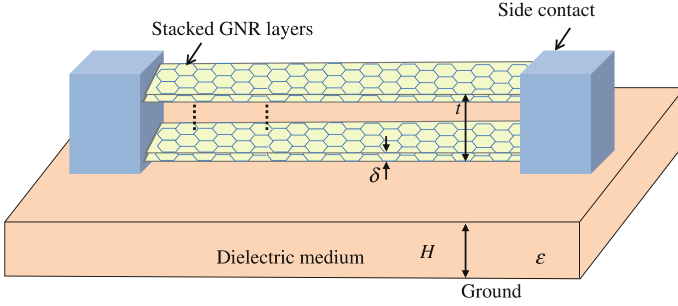

Fig. 5.1 The geometric structure of MLGNR

$$N_{\text{layer}} = 1 + \text{int}[t/\delta] \quad (5.1)$$

where w, t and δ are width, thickness, and interlayer spacing, respectively. The number of conducting channels per layer can be expressed as

$$N_{\text{ch}} = \sum_{i=0}^{n_c} \left[1 + e^{(E_i - E_F)/k_B T}\right]^{-1} + \sum_{i=0}^{n_v} \left[1 + e^{(E_i + E_F)/k_B T}\right]^{-1} \quad (5.2\text{a})$$

where the first and second summations represent the contributions of the n_c conduction subbands and n_v valence subbands, respectively, T is the temperature, k_B is the Boltzmann constant, E_F is the Fermi level, and E_i is the lowest (highest) energy of the ith conduction (valence) subband. In general, the value of E_F is set to zero for neutral GNR [8]. However, some charge usually gets trapped at the interface of graphene and the substrate. This is due to the planar structure of graphene and also due to the work function difference between the graphene and substrate. Alternatively, the number of conduction channels is also derived from the following approximated expression [18]

$$N_{\text{ch}} = \begin{cases} a_0 + a_1 w + a_2 w^2 + a_3 E_F + a_4 w E_F + a_5 E_F^2 & \text{for } E_F > 0 \\ b_0 + b_1 + b_2 w^2 & \text{for } E_F = 0 \end{cases} \quad (5.2\text{b})$$

For metallic GNR at $T = 300$ K, the fitting parameters a_0–a_6 and b_0–b_2 are given in Tables 5.1 and 5.2, respectively [18].

The typical ESC model of an MLGNR is shown in Fig. 5.2, where R_{MC}, R_Q, and r_s are the imperfect metal contact, quantum, and scattering resistances, respectively; l_k

Table 5.1 Fitting parameters (a_0–a_6) for calculating the N_{ch} of $E_F > 0$

Fitting parameters					
a_0	a_1	a_2	a_3	a_4	a_5
1.244	-1.696×10^{-2}	7.517×10^{-5}	−5.031	1.225	5.122

Table 5.2 Fitting parameters (b_0–b_3) for calculating the N_{ch} of $E_F = 0$

Fitting parameters		
b_0	b_1	b_2
1.94	2.97×10^{-4}	2.29×10^{-4}

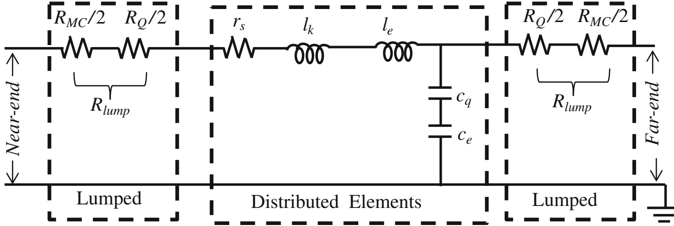

Fig. 5.2 Equivalent single conductor model of an MLGNR interconnect

and l_e are the kinetic and magnetic inductances, respectively; c_q and c_e are the quantum and electrostatic capacitances, respectively. The R_{lump} represents the average value of metal contact resistance and quantum resistance.

The resistances R_{lump} and r_s are expressed as

$$R_{\text{lump}} = \frac{1}{2}\left[\frac{h/2e^2}{N_{\text{ch}}N_{\text{layer}}} + \frac{R_{\text{MC}}}{N_{\text{layer}}}\right] \tag{5.3}$$

$$r_{s,\text{ESC}} = \left(h/2e^2 N_{\text{layer}}\right)\left(\sum_n \left(\frac{l}{\lambda_{\text{eff}_n}}\right)^{-1}\right)^{-1} \tag{5.4}$$

where h, e, N_{layer}, n, l and λ_{eff} represent the Planck's constant, electron charge, number of GNR layers, number of subbands, length, and overall effective MFP, respectively. The λ_{eff} of nth subband is expressed as

$$\frac{1}{\lambda_{\text{eff}_n}} = \frac{1}{\lambda_d} + \frac{1}{\lambda_n} \tag{5.5}$$

where λ_d and λ_n represent the MFP corresponding to the scattering effects due to defects and edge roughness, respectively. The value of λ_d is considered as 419 nm and 1.03 μm for neutral and doped MLGNRs, respectively. The λ_n for nth subband is expressed as [17]

$$\lambda_n = \frac{w}{P}\sqrt{\left(\frac{2wE_F}{nhv_F}\right)^2 - 1} \tag{5.6}$$

where P is the backscattering probability, lies in the range 0–1 and v_F is the Fermi velocity.

The quantum capacitance and kinetic inductance of an MLGNR can be expressed as

$$c_{q,\mathrm{ESC}} = N_{\mathrm{ch}} N_{\mathrm{layer}} \frac{2 \times 2q^2}{h v_F} \tag{5.7}$$

$$l_{k,\mathrm{ESC}} = \frac{1}{N_{\mathrm{ch}} N_{\mathrm{layer}}} \frac{h}{2 \times 2q^2 v_F} \tag{5.8}$$

The values of $l_{e,\mathrm{ESC}}$ and $c_{e,\mathrm{ESC}}$ can be obtained using the electromagnetic field solvers.

5.2.1 Transient Analysis of MTL and ESC Models

The ESC model of MLGNR is validated with respect to the MTL model by performing transient analysis of DIL system. The CMOS gate-driven MLGNR interconnect line is shown in Fig. 5.3. The number of stacked GNR layers is considered as 20. The interconnect line is excited and terminated by a CMOS driver and capacitive load, respectively. The symmetric CMOS inverter is used and the load capacitance is considered as 250 aF. To maintain good accuracy, the number of distributed segments is considered as 20. For different interconnect lengths ranging from 100 to 1000 μm, Fig. 5.4 shows the far-end voltage waveforms of MLGNR interconnects. It is observed that the output voltage waveforms of the ESC model are in good agreement with the MTL model for all interconnect lengths.

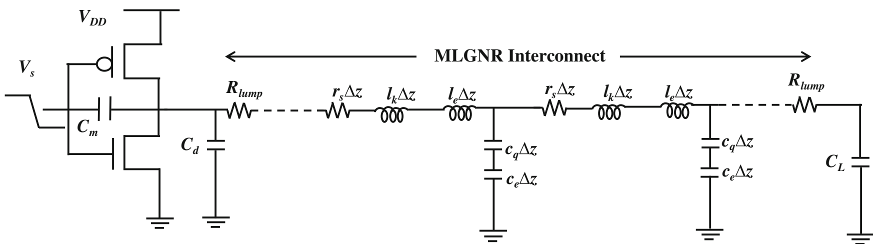

Fig. 5.3 Driver-interconnect-load (DIL) structure, wherein R_{lump} is placed at near-end and far-end terminals of the interconnect line due to the effect of quantum and imperfect contact resistances

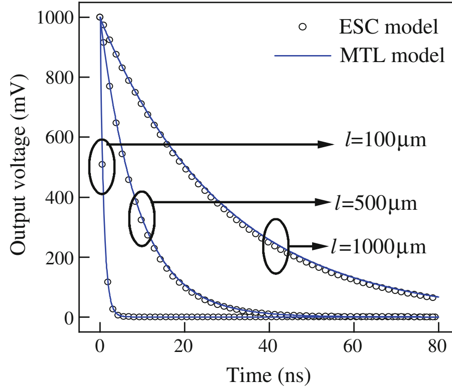

Fig. 5.4 Transient waveforms of the output voltages of MLGNR (N_{layer} = 20) interconnect

5.3 FDTD Model of the MLGNR Interconnect

The MLGNR interconnect of length l is driven by a CMOS inverter at near end and terminated by a capacitive load at far end. The total interconnect length is discretized into Nz uniform segments of space step Δz and the total simulation time is discretized into n uniform segments of time step Δt. The value of n can be determined by dividing the total simulation time by Δt. The time step, Δt is determined by the Courant stability condition. The maximum time step that can be allowed for the stable operation is $\Delta t_{\max} = \Delta z / v_{\max}$, where $v_{\max}$ is the maximum phase velocity. The voltage and current solution points are discretized along the line as shown in Fig. 5.5.

The CMOS gate-driven coupled MWCNT interconnects are shown in Fig. 5.6. The telegrapher's equations are

$$\frac{\mathrm{d}}{\mathrm{d}z}\boldsymbol{V}(z,\,t) + \boldsymbol{RI}(z,\,t) + \boldsymbol{L}\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{I}(z,\,t) = 0 \tag{5.9a}$$

$$\frac{\mathrm{d}}{\mathrm{d}z}\boldsymbol{I}(z,\,t) + \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{CV}(z,\,t) = 0 \tag{5.9b}$$

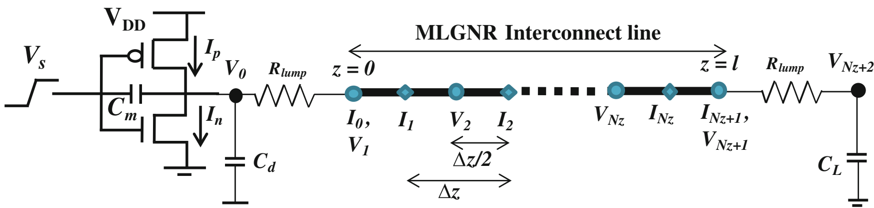

Fig. 5.5 Illustration of space discretization of line for FDTD implementation

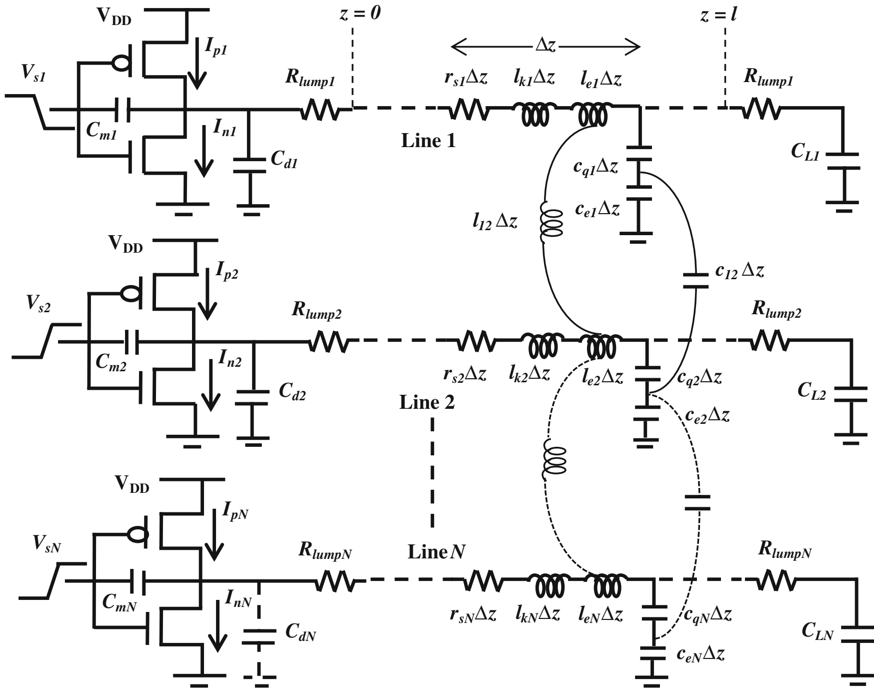

Fig. 5.6 Coupled MWCNT interconnect lines driven by CMOS inverter

where $\boldsymbol{V}$ and $\boldsymbol{I}$ are $N \times 1$ column vectors and the line parasitic elements are obtained in $N \times N$ matrix form. For instance, the voltage $\boldsymbol{V}$ is $[\,V_1 \quad V_2 \quad . \quad . \quad . \quad V_{N-1} \quad V_N\,]^T$, resistance $\boldsymbol{R}$, and inductance $\boldsymbol{L}$ matrices are $\begin{bmatrix} r_{s1} & 0 & 0 & . & . \\ 0 & r_{s2} & 0 & . & . \\ 0 & 0 & r_{s3} & . & . \\ . & . & . & . & . \\ . & . & . & 0 & r_{sN} \end{bmatrix}$ and

$\begin{bmatrix} l_{k1}+l_{e1} & l_{12} & l_{13} & . & . \\ l_{21} & l_{k2}+l_{e2} & l_{23} & . & . \\ l_{31} & l_{32} & l_{k3}+l_{e3} & . & . \\ . & . & . & . & . \\ . & . & . & l_{N-1,N} & l_{kN}+l_{eN} \end{bmatrix}$, respectively, where r_{sN} is the scattering resistance of line N, and $l_{N-1,N}$ is the mutual inductance between the lines $N-1$ and N.

Applying finite difference approximations to (5.9a) and (5.9b) the line voltages and currents can be determined, whereas using Kirchhoff's law at near-end and far-end boundaries the terminal voltage and current can be determined as

$$\boldsymbol{V}_0^{n+1} = \boldsymbol{V}_0^n + \boldsymbol{A}\left[\frac{\boldsymbol{C}_m}{\Delta t}\left(\boldsymbol{V}_s^{n+1} - \boldsymbol{V}_s^n\right) + \boldsymbol{I}_p^{n+1} - \boldsymbol{I}_n^{n+1} - \boldsymbol{I}_0^n\right] \tag{5.10}$$

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{B}\boldsymbol{V}_1^n + 2\boldsymbol{BD}\left[\frac{\boldsymbol{V}_0^{n+1}}{2\boldsymbol{R}_{\text{lump}}} + \frac{\boldsymbol{I}_0^n}{2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{5.11}$$

$$\boldsymbol{V}_k^{n+1} = \boldsymbol{V}_k^n + \boldsymbol{D}\left[\boldsymbol{I}_{k-1}^{n+1/2} - \boldsymbol{I}_k^{n+1/2}\right] \text{ for } k = 2, 3, \ldots, Nz \tag{5.12}$$

$$\boldsymbol{V}_{Nz+2}^{n+1} = \boldsymbol{V}_{Nz+2}^n + \frac{\Delta t}{\boldsymbol{C}_L}\boldsymbol{I}_{Nz+1}^n \tag{5.13}$$

$$\boldsymbol{V}_{Nz+1}^{n+1} = \boldsymbol{B}\boldsymbol{V}_{Nz+1}^n + 2\boldsymbol{BD}\left[\frac{\boldsymbol{V}_{\text{Nz}+2}^{n+1}}{2\boldsymbol{R}_{\text{lump}}} + \boldsymbol{I}_{Nz}^{n+1/2} - \frac{\boldsymbol{I}_{Nz+1}^n}{2}\right] \tag{5.14}$$

$$\boldsymbol{I}_0^{n+1} = \frac{1}{\boldsymbol{R}_{\text{lump}}}\left[\boldsymbol{V}_0^{n+1} - \boldsymbol{V}_1^{n+1}\right] \tag{5.15}$$

$$\boldsymbol{I}_k^{n+3/2} = \boldsymbol{EF}\boldsymbol{I}_k^{n+1/2} + \boldsymbol{E}\left[\boldsymbol{V}_k^{n+1} - \boldsymbol{V}_{k+1}^{n+1}\right] \quad \text{for } k = 1, 2, \ldots\ldots, Nz \tag{5.16}$$

$$\boldsymbol{I}_{Nz+1}^{n+1} = \frac{1}{\boldsymbol{R}_{\text{lump}}}\left[\boldsymbol{V}_{Nz+1}^{n+1} - \boldsymbol{V}_{Nz+2}^{n+1}\right] \tag{5.17}$$

where $\boldsymbol{A} = \left[\frac{\boldsymbol{C}_m + \boldsymbol{C}_d}{\Delta t}\right]^{-1}$, $\boldsymbol{B} = \left[\boldsymbol{U} + \frac{\boldsymbol{D}}{\boldsymbol{R}_{\text{lump}}}\right]^{-1}$, $\boldsymbol{D} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{C}\right]^{-1}$, $\boldsymbol{E} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{L} + \frac{\Delta z}{2}\boldsymbol{R}\right]^{-1}$, $\boldsymbol{F} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{L} - \frac{\Delta z}{2}\boldsymbol{R}\right]$, $\boldsymbol{C}_m$ is the drain to gate coupling capacitance, $\boldsymbol{C}_d$ is the drain diffusion capacitance of CMOS inverter, $\boldsymbol{I}_p$ and $\boldsymbol{I}_n$ are the PMOS and NMOS currents, respectively [19].

The expressions (5.10)–(5.17) are evaluated in a bootstrapping fashion. The process can be demonstrated with the flowchart shown in Fig. 5.7. The proposed model can be easily extended to bigger circuits with more number of coupled lines by changing the dimensions of the parasitic, voltage, and current matrices. To optimize the calculation time in the FDTD flow, the value of Δt must be considered as $\Delta t_{\max}$, so that the number of time steps can be minimized.

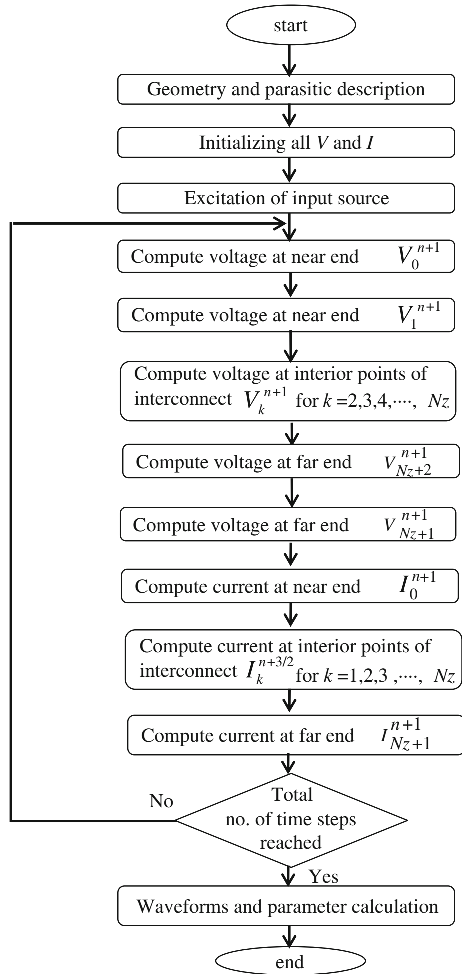

Fig. 5.7 Flowchart for evaluation of voltage and current using the proposed FDTD technique

5.4 Results and Discussion

The effective mean free path, resistance, propagation delay, and the crosstalk-induced delay of an MLGNR are analyzed by incorporating the width dependent MFP. Moreover, the performance of MLGNR interconnect is compared with Cu interconnect.

5.4.1 Analysis of Mean Free Path, Resistance, and Propagation Delay with Rough Edges

The fundamental issue in GNR is the presence of edge roughness that substantially reduces the effective MFP. For rough edges, the electrons scatter at the edges, and hence the effective MFP becomes width dependent. Therefore, width dependent MFP should be incorporated in the model of MLGNR resistance. Based on the improved model, this section demonstrates the impact of edge roughness on the performance of MLGNR interconnects.

The effective MFP, λ_{eff} is analyzed by considering the width dependent MFP for different values of edge roughness probabilities of MLGNR. The MFP due to defects and Fermi level are assumed to be 419 nm and 0.2 eV, respectively. The values of λ_{eff} are calculated using Eq. (5.5) and the results are shown in Fig. 5.8. It is observed that the edge roughness reduces the MFP by more than one order of magnitude, particularly for narrow widths. However, the reduction of MFP is highly dependent on the backscattering probability (P).

The scattering resistance of MLGNR can be expressed as

$$r_{s,\text{ESC}} = \frac{h}{2e^2 N_{\text{layer}}} \left[\sum_n \left(\frac{l}{\lambda_{\text{eff}_n}} \right)^{-1} \right]^{-1}; \; 0 < P \leq 1 \, (\text{rough edges}) \tag{5.18a}$$

$$r_{s,\text{ESC}} = \frac{h}{2e^2 N_{\text{layer}} N_{\text{ch}}} \left(\frac{l}{\lambda_d} \right); \; P = 0 \, (\text{smooth edges}) \tag{5.18b}$$

Using (5.18a) and (5.18b), the scattering resistance of MLGNR for different widths and edge roughness probabilities is shown in Fig. 5.9. The thickness and interconnect length are 56.9 nm and 100 μm, respectively. The variation in the resistance is higher at narrow widths due to the dominating effect of edge scattering.

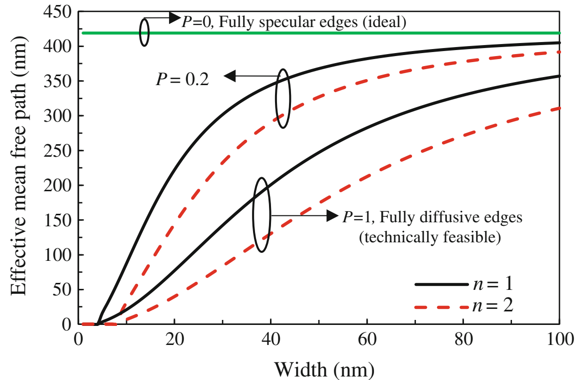

Fig. 5.8 MFP of MLGNR for first two lowest subbands at different widths

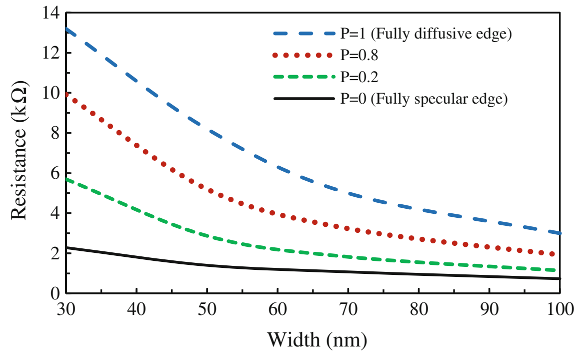

Fig. 5.9 Resistance of MLGNR for different interconnect widths

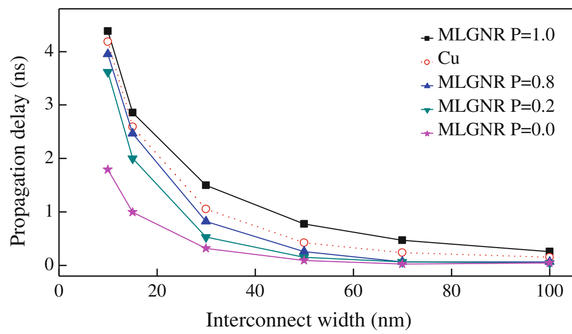

Fig. 5.10 Propagation delay of MLGNR and Cu at t = 56.9 nm and l = 100 μm

For different values of P, the propagation delay of MLGNR and Cu at different interconnect widths is shown in Fig. 5.10. It is observed that for wider MLGNR interconnects, the delay is almost constant for different edge roughness probabilities. It is due to a small variation in the scattering resistance for wider interconnects. It can also be observed that the propagation delay of MLGNR is higher than Cu for fully diffusive edge (P = 1).

5.4.2 Crosstalk-Induced Delay

The coupled MLGNR interconnects performance is analyzed using the proposed model and the outcome is compared with the previously reported model [14], where the MFP is considered as independent of width. An industry standard HSPICE simulator is used for model validation. Considering the width dependent and width independent MFPs, the variation of crosstalk-induced propagation delay with interconnect width during in-phase and out-phase transitions is shown in Fig. 5.11a, b, respectively. The dynamic crosstalk is analyzed by switching both lines in-phase and out-phase. The input signal rise and fall transition times are considered as 20 ps. For an interconnect length of 10 μm, the interconnect width is varied from 10 to 60 nm, while

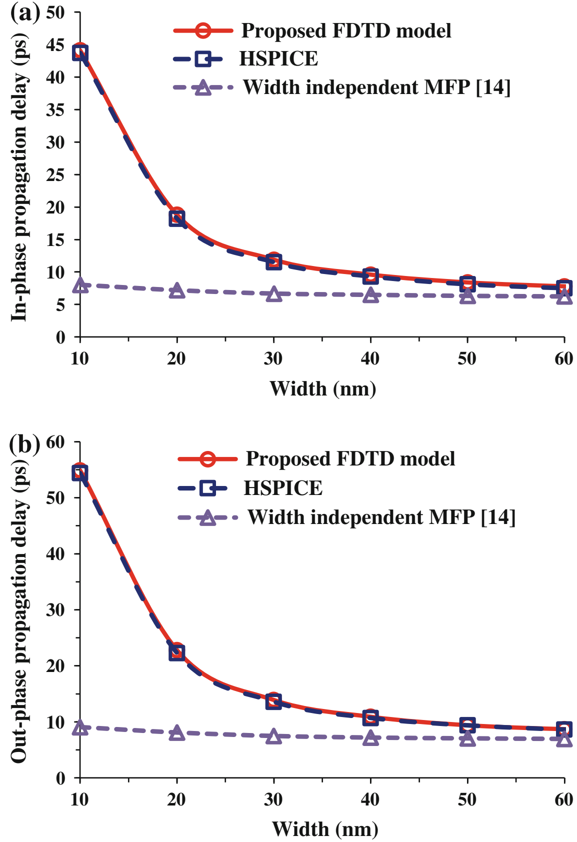

Fig. 5.11 Crosstalk-induced propagation delay performance with change in interconnect width under **a** in-phase switching, and **b** out-phase switching

keeping the thickness and spacing between the interconnect lines as 22 nm, and distance from the ground plane as 44 nm.

From Fig. 5.11, it can be observed that the width independent MFP model presented in [14] underestimates the propagation delay by 32 %. Moreover, it is observed that this margin increases substantially for technology nodes having narrower interconnect widths. This is due to the prominent effect of edge scattering at smaller dimensions. Therefore, it is strongly recommended to include width dependent MFP for accurately modeling the crosstalk noise in MLGNR interconnects.

To further verify the robustness of the proposed model, the propagation delay comparison under in-phase and out-phase transitions on victim line 2 is observed in Fig. 5.12 for different input transition times. It can be observed that the proposed model matches accurately with HSPICE simulations for all transition times. Moreover, the propagation delay during the out-phase transition is higher due to Miller capacitance effect.

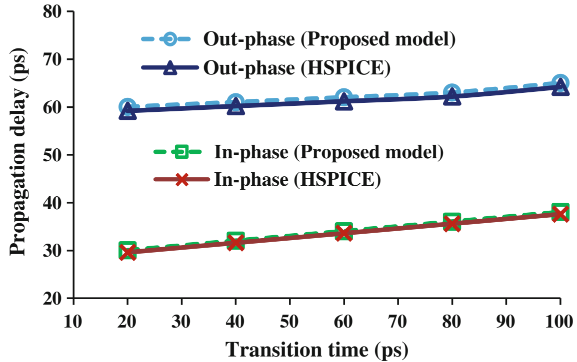

Fig. 5.12 Variation of propagation delay with respect to input transition time

Using a PC with Pentium Dual Core CPU (2.33 GHz, 4 GB RAM), the runtime of the proposed model is compared with the HSPICE simulation time. Using the proposed model, it is observed that the CPU runtime reduces by an average of 95 % in comparison to HSPICE simulations. For an interconnect length of 200 μm with 100-space and 1000-time segments, the runtime using proposed model is 0.36 s against 7.26 s using HSPICE.

5.4.3 Performance Comparison Between Cu and MLGNR Interconnects

The propagation delay and power dissipation of MLGNR (neutral and doped) and Cu are analyzed for similar interconnect length, width, and thickness. The mean free path, λ_d of neutral MLGNR is considered as 419 nm with in-plane conductivity of 0.026 $(\mu\Omega\ \text{cm})^{-1}$, whereas an AsF_5 doped MLGNR can exhibit λ_d of 1.03 μm with in-plane conductivity of 0.63 $(\mu\Omega\ \text{cm})^{-1}$ [8]. Figure 5.3 shows the DIL system wherein the interconnect line is represented by the ESC model of MLGNR. The *RLC* distributed model is used for analyzing the conventional Cu interconnects [20–22]. A CMOS driver with supply voltage of 0.9 V is used to drive the interconnect line that is terminated by a load capacitance of 10 fF. Using this setup, propagation delay and power dissipation are analyzed for different global interconnect lengths ranging from 100 to 1000 μm.

The propagation delay and power dissipation are proportional to the resistive and capacitive parasitics of interconnect. For different interconnect thicknesses, the MLGNR (neutral and doped) to Cu delay and power dissipation ratio are shown in Fig. 5.13a, b, respectively. It is observed that a thicker doped MLGNR demonstrates substantial reduction in delay and power dissipation compared to Cu interconnects. In doped MLGNR, the higher carrier concentration in each layer

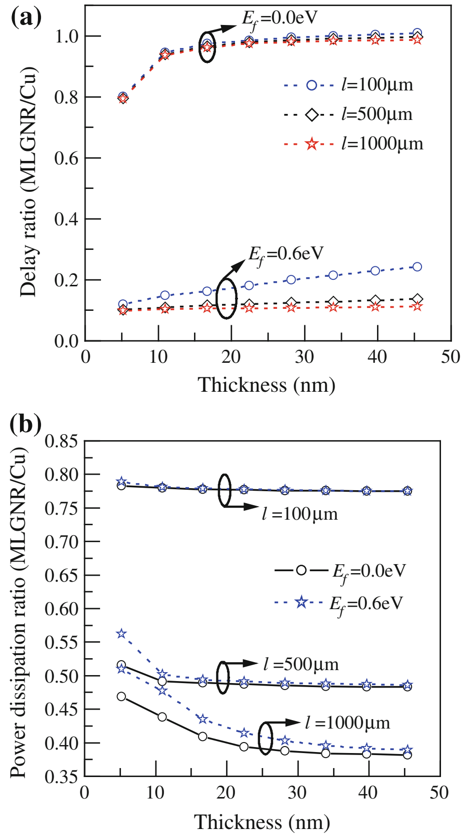

Fig. 5.13 MLGNR to Cu **a** delay and **b** power dissipation ratio at different interconnect thicknesses

substantially increases the number of conducting channels that in turn drastically reduces the resistive parasitic ($r_{s,\mathrm{ESC}}$) compared to Cu interconnects. Although, more number of conducting channels in doped MLGNR increases the quantum capacitance ($c_{q,\mathrm{ESC}}$), but the equivalent capacitance (c_{ESC}) remains almost constant due to the dominating effect of ($c_{e,\mathrm{ESC}}$) factor. Therefore, the cumulative effect of $r_{s,\mathrm{ESC}}$ and c_{ESC} of doped MLGNR reduces the overall delay and power dissipation in comparison to Cu interconnects.

Table 5.3 summarizes the percentage reduction in propagation delay and power dissipation of doped MLGNR in comparison to Cu at different interconnect lengths. The reduction is more pronounced for longer interconnects due to a comparatively higher reduction in the line resistance. The overall delay and power dissipation of doped MLGNR are reduced by 86.13 and 43.72 %, respectively, in comparison to the Cu interconnects.

Table 5.3 Percentage reduction in propagation delay and power dissipation for doped MLGNR with respect to Cu interconnects

Thickness (nm)	% reduction in propagation delay of MLGNR *w.r.t.* Cu for interconnect lengths of			% reduction in power dissipation of MLGNR *w.r.t.* Cu for interconnect lengths		
	100 μm	500 μm	1000 μm	100 μm	500 μm	1000 μm
5.75	88.01	89.79	90.11	49.39	50.61	54.04
11.50	85.13	88.97	89.61	50.93	52.98	57.17
17.25	83.78	88.44	89.42	51.12	54.17	59.14
23.00	81.91	87.98	89.27	51.32	55.82	60.61
28.75	80.05	87.53	89.15	51.47	57.31	61.21
34.50	78.46	87.10	89.04	51.57	58.02	61.57
40.25	77.11	86.67	88.92	51.66	58.99	61.72
46.00	75.76	86.25	88.82	51.69	60.13	61.81

5.5 Summary

This chapter analyzed the performance of MLGNR as a potential candidate to replace the Cu for future VLSI interconnects. Based on the multiconductor transmission line theory, the ESC model of MLGNR is presented. In a more realistic manner, the proposed model incorporates the width dependent MFP parameter that helps in accurately estimating the crosstalk induced performance in comparison to the conventional model. The proposed ESC model is validated by comparing its transient response with respect to the response of MTL model.

The FDTD model is presented to analyze the crosstalk effects in coupled MLGNR interconnect lines. The results of the proposed model closely match with that of HSPICE simulations. The average error in the propagation delay measurement is observed to be less than 2 %. Moreover, it has been noticed that the width dependent MFP should be incorporated in a valid crosstalk noise modeling. In addition, the efficiency of the proposed model has also been demonstrated. It is observed that the model requires at an average only 5 % of HSPICE simulation time. Based on the comparative study, it is observed that the MLGNR is the better suitable on-chip interconnect material than the Cu.

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Chapter 6
An Efficient US-FDTD Model for Crosstalk Analysis of On-Chip Interconnects

Abstract This chapter introduces a novel unconditionally stable FDTD (US-FDTD) model for the performance analysis of on-chip interconnects. It is observed that the stability of the proposed US-FDTD model is not constrained by the CFL condition and is therefore unconditionally stable. The accuracy of the proposed model is validated against the conventional FDTD model. It is observed that the US-FDTD model is as accurate as the conventional FDTD model while being highly time efficient. Moreover, the performance of Cu interconnect is compared with MWCNT and MLGNR interconnects under the influence of crosstalk.

Keywords Courant–Friedrichs–Lewy (CFL) · Stability condition · Finite difference time domain (FDTD) · Unconditionally stable · VLSI interconnects

6.1 Introduction

The shrinking size of the transistors has resulted in gate delays being overshadowed by larger interconnect delays [1, 2]. Therefore, the overall chip performance is primarily dependent on the interconnect performance. The close proximity of interconnects in miniaturized microelectronic devices leads to crosstalk noise. The crosstalk noise may result in logic failure, circuit malfunction, change in signal propagation and unwanted power dissipation [3]. Therefore, accurate modeling of crosstalk noise has emerged as vital design criteria in microelectronics.

The FDTD technique is widely used to solve electromagnetic wave problems. It is a fast, accurate and robust technique, which involves discretization of electromagnetic fields in both space and time domains [4–6]. Recently, the application of this versatile technique has been extended to high-speed interconnect domain [7]. However, in the FDTD technique to ensure a stable operation, the time step size (Δt) is limited by the Courant–Friedrichs–Lewy (CFL) stability condition, i.e., $\Delta t \leq \Delta t_{max}$, where $\Delta t_{max} = \Delta z / v_{max}$, the terms Δz and v_{max} represent the space step size and the maximum phase velocity, respectively [8, 9]. Consequently, the

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conventional FDTD techniques [7, 10, 11] consume large memory space and power due to the enormous number of iterations required for the analysis. Hence, beyond the CFL condition, the FDTD technique is unstable and within it, the technique is not efficient.

The improvements in FDTD technique can be easily addressed if the CFL stability condition is removed. Recently, several researchers have proposed various modified FDTD techniques to overcome the CFL stability criteria based on different algorithms, such as alternating direction implicit (ADI)-FDTD [12, 13], split-step FDTD [14, 15], Crank-Nicolson (CN)-FDTD [16, 17] and others [18–20]. All these techniques [12–20] were developed for transmission lines that are usually excited and terminated by resistive drivers and resistive loads, respectively. However, the VLSI interconnects are driven and terminated by the nonlinear CMOS drivers and capacitive loads, respectively. Therefore, the existing unconditionally stable FDTD techniques are not suitable to analyze the performance of CMOS gate driven VLSI interconnects.

In this chapter, a novel model is proposed that successfully implements an unconditionally stable FDTD (US-FDTD) technique to analyze the comprehensive crosstalk effects of coupled VLSI interconnects. The interconnect lines are driven by the nonlinear CMOS driver that are modeled by the modified Alpha power law model, which includes the drain conductance parameter. The crosstalk induced performance parameters such as noise peak voltage, noise width, and delay are analyzed. The proposed model is compared against the conventional FDTD model for accuracy, efficiency and stability.

The remaining chapter is organized as follows: Sect. 6.2 details the implementation of the US-FDTD technique for coupled interconnect lines. Moreover, the unconditional stability of the model is also scrutinized. Section 6.3 analyzes the crosstalk noise and validates the accuracy and efficiency of the proposed model. Moreover, to verify the unconditional stability of the proposed model the transient analysis is carried out at different values of time step. The performance of Cu, MWCNT and MLGNR interconnects is compared in Sect. 6.4. Finally, Sect. 6.5 concludes the chapter.

6.2 Development of Proposed US-FDTD Model

This section deals with the development of US-FDTD model for the coupled on-chip interconnects. The interconnect lines are coupled capacitively and inductively. In a more realistic manner, the CMOS drivers are considered for accurate performance analysis. The interconnect lines are terminated by capacitive loads. The schematic view of coupled interconnect lines is shown in Fig. 6.1, where the line x and the line y represent the aggressor and victim lines, respectively.

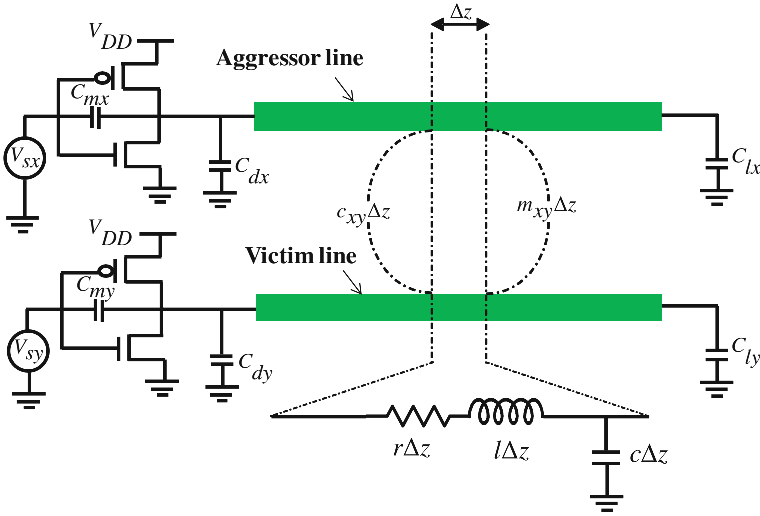

Fig. 6.1 Schematic view of coupled interconnects driven by CMOS drivers

6.2.1 Modeling of Coupled On-Chip Interconnects

The interconnect lines are represented by the transmission lines that are coupled capacitively, c_{xy} and inductively, m_{xy}. The telegrapher's equations in the transverse electromagnetic mode of coupled lines, at any point z along the line, is represented as

$$\frac{\partial v_x(z,t)}{\partial z} + r_x i_x(z,t) + l_x \frac{\partial i_x(z,t)}{\partial t} + m_{xy} \frac{\partial i_y(z,t)}{\partial t} = 0 \quad (6.1a)$$

$$\frac{\partial v_y(z,t)}{\partial z} + r_y i_y(z,t) + l_y \frac{\partial i_y(z,t)}{\partial t} + m_{xy} \frac{\partial i_x(z,t)}{\partial t} = 0 \quad (6.1b)$$

$$\frac{\partial i_x(z,t)}{\partial z} + c_x \frac{\partial v_x(z,t)}{\partial t} + c_{xy} \frac{\partial v_x(z,t)}{\partial t} - c_{xy} \frac{\partial v_y(z,t)}{\partial t} = 0 \quad (6.1c)$$

$$\frac{\partial i_y(z,t)}{\partial z} + c_y \frac{\partial v_y(z,t)}{\partial t} + c_{xy} \frac{\partial v_y(z,t)}{\partial t} - c_{xy} \frac{\partial v_x(z,t)}{\partial t} = 0 \quad (6.1d)$$

Representing Eqs. (6.1a) and (6.1b) in matrix form results in

$$\frac{\partial \boldsymbol{v}(z,t)}{\partial z} + \boldsymbol{r i}(z,t) + \boldsymbol{l} \frac{\partial \boldsymbol{i}(z,t)}{\partial t} = \mathbf{0} \quad (6.2a)$$

where v and i are evaluated in 2 × 1. Matrix form as $v = [v_x, v_y]^T$, $i = [i_x, i_y]^T$, r and l are evaluated in 2 × 2 matrix form as

$$\boldsymbol{r} = \begin{pmatrix} r_x & 0 \\ 0 & r_y \end{pmatrix}, \boldsymbol{l} = \begin{pmatrix} l_x & m_{xy} \\ m_{xy} & l_y \end{pmatrix}$$

Representing Eqs. (6.1c) and (6.1d) in matrix form results in

$$\frac{\partial \boldsymbol{i}(z,t)}{\partial z} + \boldsymbol{c}\frac{\partial \boldsymbol{v}(z,t)}{\partial t} = \boldsymbol{0} \tag{6.2b}$$

where c is evaluated in 2 × 2 matrix form as $\boldsymbol{c} = \begin{pmatrix} c_x + c_{xy} & -c_{xy} \\ -c_{xy} & c_y + c_{xy} \end{pmatrix}$.

Figure 6.2 represents the space discretization of an interconnect line. Using the forward difference approximation in space domain, Eq. (6.2a) results in

$$\frac{\boldsymbol{v}_{k+1} - \boldsymbol{v}_k}{\Delta z} = -\boldsymbol{r}\boldsymbol{i}_k - \boldsymbol{l}\frac{\partial \boldsymbol{i}_k}{\partial t} \tag{6.3a}$$

For k = 1, 2, …, N_z, Eq. (6.3a) can be rearranged as

$$\boldsymbol{v}_{k+1} - \boldsymbol{v}_k + \boldsymbol{r}\Delta z \boldsymbol{i}_k + \boldsymbol{l}\Delta z \frac{\partial \boldsymbol{i}_k}{\partial t} = \boldsymbol{0} \tag{6.3b}$$

Using the backward difference approximation in space domain, Eq. (6.2b) results in

$$\frac{\boldsymbol{i}_k - \boldsymbol{i}_{k-1}}{\Delta z} = -\boldsymbol{c}\frac{\partial \boldsymbol{v}_k}{\partial t} \tag{6.4}$$

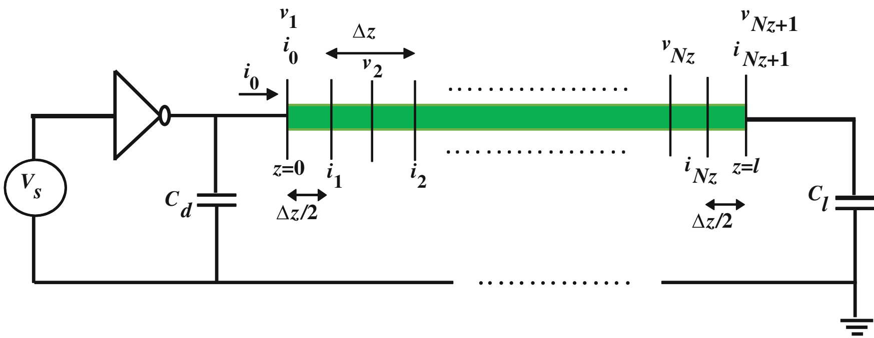

Fig. 6.2 Representation of space discretization of an interconnect line for unconditionally stable FDTD technique. The total interconnect length is divided into N_z number of sections, each with a uniform length of Δz

For $k = 1$ and $k = Nz + 1$, the space segment is replaced by $\Delta z/2$ (Fig. 6.2). For $k = 1$, Eq. (6.4) results in

$$\boldsymbol{i}_1 - \boldsymbol{i}_0 + \frac{\boldsymbol{c}\Delta z}{2}\frac{\partial \boldsymbol{v}_1}{\partial t} = \boldsymbol{0} \tag{6.5a}$$

For $k = Nz + 1$, Eq. (6.4) results in

$$\boldsymbol{i}_{Nz+1} - \boldsymbol{i}_{Nz} + \frac{\boldsymbol{c}\Delta z}{2}\frac{\partial \boldsymbol{v}_{Nz+1}}{\partial t} = \boldsymbol{0} \tag{6.5b}$$

For $k = 2, 3, \ldots, Nz$, Eq. (6.4) results in

$$\boldsymbol{i}_k - \boldsymbol{i}_{k-1} + \boldsymbol{c}\Delta z\frac{\partial \boldsymbol{v}_k}{\partial t} = \boldsymbol{0} \tag{6.5c}$$

Equations (6.5a) and (6.5b) are further modified after applying the boundary conditions, as illustrated in the following Sects. 6.2.2 and 6.2.3.

6.2.2 Modeling of CMOS Driver

The CMOS drivers are modeled by modified alpha power law model that incorporates the effect of velocity saturation along with the finite drain conductance parameter. As shown in Fig. 6.1, the parasitic capacitances C_m and C_d represent gate to drain coupling capacitance and drain diffusion capacitance, respectively. The NMOS and PMOS transistors can operate in either cutoff, linear or saturation regions depending on the input voltage signal [21] as depicted in Fig. 6.3.

The current equations of the MOS transistors are

$$\boldsymbol{I}_n = \begin{cases} \boldsymbol{0} & \text{(cutoff)} \\ \boldsymbol{M}_{\mathrm{Ln}}(\boldsymbol{V}_s - \boldsymbol{V}_{\mathrm{Tn}})^{\alpha_n/2}\boldsymbol{v}_1 & \text{(lin)} \\ \boldsymbol{M}_{\mathrm{Sn}}(\boldsymbol{V}_s - \boldsymbol{V}_{\mathrm{Tn}})^{\alpha_n}(\boldsymbol{U} + \sigma_n\boldsymbol{v}_1) & \text{(sat)} \end{cases} \tag{6.6}$$

$$\boldsymbol{I}_p = \begin{cases} \boldsymbol{0} & \text{(cutoff)} \\ \boldsymbol{M}_{\mathrm{Lp}}\left(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{V}_s - \left|\boldsymbol{V}_{\mathrm{Tp}}\right|\right)^{\alpha_p/2}(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{v}_1) & \text{(lin)} \\ \boldsymbol{M}_{\mathrm{Sp}}\left(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{V}_s - \left|\boldsymbol{V}_{\mathrm{Tp}}\right|\right)^{\alpha_p}\left(\boldsymbol{U} + \sigma_p(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{v}_1)\right) & \text{(sat)} \end{cases} \tag{6.7}$$

where $\boldsymbol{U}$ is a 2×2 identity matrix, M_{Ln} (M_{Lp}), M_{Sn} (M_{Sp}), α_n (α_p), σ_n (σ_p) and V_{Tn} (V_{Tp}) are the linear region transconductance parameter, saturation region transconductance parameter, velocity saturation index, drain conductance parameter and the threshold voltage of NMOS (PMOS), respectively. The model parameters of NMOS/PMOS transistor at 32 nm technology node are listed in Table 6.1.

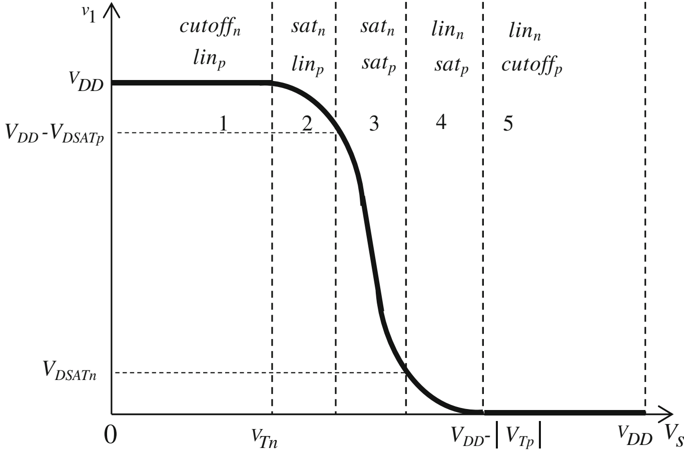

Fig. 6.3 The five regions of operation of a CMOS inverter. The subscripts *n* and *p* denote NMOS and PMOS, respectively

Table 6.1 Model parameters for 32 nm node

Parameter	PMOS	NMOS
M_L	0.006	0.007
M_S	0.875105×10^{-3}	1.944973×10^{-3}
α	1.0788	0.91503
σ	2.685	0.876
V_T	0.36	0.35

6.2.3 Modeling of Driver-Interconnect-Load

In this sub-section, the near-end and far-end interconnect terminal conditions are incorporated in the current equations. At the near-end terminal (k = 1), applying Kirchhoff's current law, the source current i_0 can be expressed as

$$\boldsymbol{i}_0 = \boldsymbol{I}_p - \boldsymbol{I}_n + \boldsymbol{C}_m\left(\frac{\mathrm{d}(\boldsymbol{V}_s - \boldsymbol{v}_1)}{\mathrm{d}t}\right) - \boldsymbol{C}_d\frac{\mathrm{d}\boldsymbol{v}_1}{\mathrm{d}t} \tag{6.8}$$

Incorporating Eq. (6.8) in Eq. (6.5a) results in

$$\boldsymbol{i}_1 - \boldsymbol{I}_p + \boldsymbol{I}_n - \boldsymbol{C}_m\left(\frac{\mathrm{d}(\boldsymbol{V}_s - \boldsymbol{v}_1)}{\mathrm{d}t}\right) + \boldsymbol{C}_d\frac{\mathrm{d}\boldsymbol{v}_1}{\mathrm{d}t} + \frac{\boldsymbol{c}\Delta z}{2}\frac{\partial \boldsymbol{v}_1}{\partial t} = \boldsymbol{0} \tag{6.9}$$

At the far-end terminal ($k = Nz + 1$), the load current i_{Nz+1} can be expressed as

$$\boldsymbol{i}_{Nz+1} = \boldsymbol{C}_l \frac{\partial \boldsymbol{v}_{Nz+1}}{\partial t} \tag{6.10}$$

Incorporating Eq. (6.10) in (6.5b) results in

$$\boldsymbol{i}_{Nz} - \left(\frac{\boldsymbol{c}\Delta z}{2} + \boldsymbol{C}_l \right) \frac{\partial \boldsymbol{v}_{Nz+1}}{\partial t} = \boldsymbol{0} \tag{6.11}$$

Representing Eqs. (6.9), (6.5c) and (6.11) together in the matrix form results in

$$\boldsymbol{PI} + \boldsymbol{GV} + \boldsymbol{C}\frac{\partial \boldsymbol{V}}{\partial t} = \boldsymbol{I}_s + \boldsymbol{X}_r \frac{\partial V_r}{\partial t} \tag{6.12}$$

where $\boldsymbol{P} = \begin{pmatrix} \boldsymbol{U} & \boldsymbol{0} & \cdots & \boldsymbol{0} & \boldsymbol{0} \\ -\boldsymbol{U} & \boldsymbol{U} & \cdots & \boldsymbol{0} & \boldsymbol{0} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \boldsymbol{0} & \boldsymbol{0} & \cdots & -\boldsymbol{U} & \boldsymbol{U} \\ \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} & -\boldsymbol{U} \end{pmatrix}_{2(Nz+1)\times 2Nz}$, $\boldsymbol{G} = \begin{pmatrix} \boldsymbol{E}_1 & \boldsymbol{0} & \cdots & \boldsymbol{0} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \ddots & \vdots & \boldsymbol{0} \\ \vdots & \ddots & \ddots & \boldsymbol{0} & \boldsymbol{0} \\ \boldsymbol{0} & \ddots & \ddots & \boldsymbol{0} & \vdots \\ \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} & \boldsymbol{0} \end{pmatrix}_{2(Nz+1)\times 2(Nz+1)}$,

$$\boldsymbol{C} = \begin{pmatrix} \frac{\boldsymbol{c}\Delta z}{2} + \boldsymbol{C}_d + \boldsymbol{C}_m & \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{c}\Delta z & \ddots & \ddots & \boldsymbol{0} \\ \vdots & \boldsymbol{0} & \ddots & \boldsymbol{0} & \vdots \\ \boldsymbol{0} & \vdots & \ddots & \boldsymbol{c}\Delta z & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} & \frac{\boldsymbol{c}\Delta z}{2} + \boldsymbol{C}_l \end{pmatrix}_{2(Nz+1)\times 2(Nz+1)}, \quad \boldsymbol{I}_s = \begin{pmatrix} \boldsymbol{E}_2 \\ \boldsymbol{0} \\ \vdots \\ \vdots \\ \boldsymbol{0} \end{pmatrix}_{2(N_z+1)\times 1},$$

$$\boldsymbol{I} = \begin{pmatrix} \boldsymbol{i}_1 \\ \boldsymbol{i}_2 \\ \vdots \\ \vdots \\ \boldsymbol{i}_{Nz} \end{pmatrix}_{2Nz\times 1}, \quad \boldsymbol{V}_r = \begin{pmatrix} \boldsymbol{V}_s \\ \boldsymbol{0} \\ \vdots \\ \vdots \\ \boldsymbol{0} \end{pmatrix}_{2(Nz+1)\times 1}, \quad \boldsymbol{V} = \begin{pmatrix} \boldsymbol{v}_1 \\ \boldsymbol{v}_2 \\ \vdots \\ \vdots \\ \boldsymbol{v}_{Nz+1} \end{pmatrix}_{2(Nz+1)\times 1},$$

$$\boldsymbol{X}_r = \begin{pmatrix} \boldsymbol{C}_m & \boldsymbol{0} & \cdots & \cdots & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \ddots & \ddots & \boldsymbol{0} \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ \vdots & \vdots & \ddots & \ddots & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} & \boldsymbol{0} \end{pmatrix}_{2(Nz+1)\times 2(Nz+1)}.$$

The values of E_1 and E_2 are dependent on the operating region of CMOS inverter and can be obtained from Table 6.2.

Representing Eq. (6.3b) in matrix form results in

$$\boldsymbol{QV} + \boldsymbol{RI} + \boldsymbol{L}\frac{\partial \boldsymbol{I}}{\partial t} = \boldsymbol{0} \tag{6.13}$$

Table 6.2 E_1 and E_2 for different regions of operation

Region	E_1	E_2
1	$\boldsymbol{M}_{\mathrm{Lp}}\left(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{V}_s - \lvert\boldsymbol{V}_{\mathrm{Tp}}\rvert\right)^{\alpha_p/2}$	$\boldsymbol{M}_{\mathrm{Lp}}\left(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{V}_s - \lvert\boldsymbol{V}_{\mathrm{Tp}}\rvert\right)^{\alpha_p/2}\boldsymbol{V}_{\mathrm{DD}}$
2	$\boldsymbol{M}_{\mathrm{Lp}}\left(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{V}_s - \lvert\boldsymbol{V}_{\mathrm{Tp}}\rvert\right)^{\alpha_p/2} + \sigma_n\boldsymbol{M}_{\mathrm{Sn}}(\boldsymbol{V}_s - \boldsymbol{V}_{\mathrm{Tn}})^{\alpha_n}$	$\boldsymbol{M}_{\mathrm{Lp}}\left(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{V}_s - \lvert\boldsymbol{V}_{\mathrm{Tp}}\rvert\right)^{\alpha_p/2}\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{M}_{\mathrm{Sn}}(\boldsymbol{V}_s - \boldsymbol{V}_{\mathrm{Tn}})^{\alpha_n}$
3	$\sigma_p\boldsymbol{M}_{\mathrm{Sp}}\left(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{V}_s - \lvert\boldsymbol{V}_{\mathrm{Tp}}\rvert\right)^{\alpha_p} + \sigma_n\boldsymbol{M}_{\mathrm{Sn}}(\boldsymbol{V}_s - \boldsymbol{V}_{\mathrm{Tn}})^{\alpha_n}$	$\boldsymbol{M}_{\mathrm{Sp}}\left(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{V}_s - \lvert\boldsymbol{V}_{\mathrm{Tp}}\rvert\right)^{\alpha_p} + \sigma_p\boldsymbol{M}_{\mathrm{Sp}}\left(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{V}_s - \lvert\boldsymbol{V}_{\mathrm{Tp}}\rvert\right)^{\alpha_p}\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{M}_{\mathrm{Sn}}(\boldsymbol{V}_s - \boldsymbol{V}_{\mathrm{Tn}})^{\alpha_n}$
4	$\boldsymbol{M}_{\mathrm{Ln}}(\boldsymbol{V}_s - \boldsymbol{V}_{\mathrm{Tn}})^{\alpha_n/2} + \sigma_p\boldsymbol{M}_{\mathrm{Sp}}\left(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{V}_s - \lvert\boldsymbol{V}_{\mathrm{Tp}}\rvert\right)^{\alpha_p}$	$\boldsymbol{M}_{\mathrm{Sp}}\left(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{V}_s - \lvert\boldsymbol{V}_{\mathrm{Tp}}\rvert\right)^{\alpha_p} + \sigma_p\boldsymbol{M}_{\mathrm{Sp}}\left(\boldsymbol{V}_{\mathrm{DD}} - \boldsymbol{V}_s - \lvert\boldsymbol{V}_{\mathrm{Tp}}\rvert\right)^{\alpha_p}\boldsymbol{V}_{\mathrm{DD}}$
5	$\boldsymbol{M}_{\mathrm{Ln}}(\boldsymbol{V}_s - \boldsymbol{V}_{\mathrm{Tn}})^{\alpha_n/2}$	0

where $\boldsymbol{Q} = \begin{pmatrix} -\boldsymbol{U} & \boldsymbol{U} & \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} \\ \boldsymbol{0} & -\boldsymbol{U} & \boldsymbol{U} & \ddots & \ddots & \boldsymbol{0} \\ \vdots & \ddots & \ddots & \ddots & \boldsymbol{0} & \vdots \\ \boldsymbol{0} & \ddots & \ddots & -\boldsymbol{U} & \boldsymbol{U} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} & -\boldsymbol{U} & \boldsymbol{U} \end{pmatrix}_{2Nz \times 2(Nz+1)}$, $\boldsymbol{R} = \begin{pmatrix} r\Delta z & \boldsymbol{0} & \cdots & \boldsymbol{0} \\ \boldsymbol{0} & r\Delta z & \ddots & \vdots \\ \vdots & \ddots & \ddots & \boldsymbol{0} \\ \boldsymbol{0} & \cdots & \boldsymbol{0} & r\Delta z \end{pmatrix}_{2Nz \times 2Nz}$,

$$\boldsymbol{L} = \begin{pmatrix} l\Delta z & \boldsymbol{0} & \cdots & \boldsymbol{0} \\ \boldsymbol{0} & l\Delta z & \ddots & \vdots \\ \vdots & \ddots & \ddots & \boldsymbol{0} \\ \boldsymbol{0} & \cdots & \boldsymbol{0} & l\Delta z \end{pmatrix}_{2Nz \times 2Nz}$$

Applying finite difference in time domain to Eqs. (6.12) and (6.13)

$$\boldsymbol{P}\frac{\boldsymbol{I}^{n+1}+\boldsymbol{I}^{n}}{2} + \boldsymbol{G}\frac{\boldsymbol{V}^{n+1}+\boldsymbol{V}^{n}}{2} + \boldsymbol{C}\frac{\boldsymbol{V}^{n+1}-\boldsymbol{V}^{n}}{\Delta t} = \frac{\boldsymbol{I}_s^{n+1}+\boldsymbol{I}_s^{n}}{2} + \boldsymbol{X}_r\frac{\boldsymbol{V}_r^{n+1}-\boldsymbol{V}_r^{n}}{\Delta t} \tag{6.14}$$

$$\boldsymbol{Q}\frac{\boldsymbol{V}^{n+1}+\boldsymbol{V}^{n}}{2} + \boldsymbol{R}\frac{\boldsymbol{I}^{n+1}+\boldsymbol{I}^{n}}{2} + \boldsymbol{L}\frac{\boldsymbol{I}^{n+1}-\boldsymbol{I}^{n}}{\Delta t} = \boldsymbol{0} \tag{6.15}$$

Solving Eqs. (6.14) and (6.15) results in

$$\boldsymbol{V}^{n+1} = \boldsymbol{K}_1\left(\frac{\boldsymbol{I}_s^{n+1}+\boldsymbol{I}_s^{n}}{2} + \boldsymbol{X}_r\frac{\boldsymbol{V}_r^{n+1}-\boldsymbol{V}_r^{n}}{\Delta t} - \boldsymbol{K}_2\boldsymbol{V}^n - \boldsymbol{K}_3\boldsymbol{I}^n\right) \tag{6.16}$$

$$\boldsymbol{I}^{n+1} = -\boldsymbol{K}_4\left(\boldsymbol{K}_5\boldsymbol{I}^n + \boldsymbol{K}_6\left(\boldsymbol{V}^{n+1}+\boldsymbol{V}^n\right)\right) \tag{6.17}$$

where $\boldsymbol{K}_1 = \left(\left(\frac{\boldsymbol{G}}{2}+\frac{\boldsymbol{C}}{\Delta t}\right) - \frac{\boldsymbol{P}}{4}\boldsymbol{K}_4\boldsymbol{Q}\right)^{-1}$, $\boldsymbol{K}_2 = \left(\left(\frac{\boldsymbol{G}}{2}-\frac{\boldsymbol{C}}{\Delta t}\right) - \frac{\boldsymbol{P}}{4}\boldsymbol{K}_4\boldsymbol{Q}\right)$, $\boldsymbol{K}_3 = \left(\frac{\boldsymbol{P}}{2} - \frac{\boldsymbol{P}}{2}\boldsymbol{K}_4\boldsymbol{K}_5\right)$, $\boldsymbol{K}_4 = \left(\frac{\boldsymbol{R}}{2}+\frac{\boldsymbol{L}}{\Delta t}\right)^{-1}$, $\boldsymbol{K}_5 = \left(\frac{\boldsymbol{R}}{2}-\frac{\boldsymbol{L}}{\Delta t}\right)$, $\boldsymbol{K}_6 = \frac{\boldsymbol{Q}}{2}$.

Initially, the voltage and current values of interconnect line are set to zero. After exciting the input voltage source, the voltages along the line are evaluated for a specific time using (6.16) in terms of the previous values of voltage and current. Thereafter, the currents are evaluated using (6.17), in terms of these voltages and previous current values. The process is continued till the final time step is reached. This procedure can be demonstrated with the flowchart shown in Fig. 6.4.

From Eqs. (6.16) and (6.17), it can be observed that these equations are in implicit form and hence free from stability condition. Moreover, the conductance parameter ($\boldsymbol{g}$) can be incorporated in the proposed model without affecting the unconditional stability criteria.

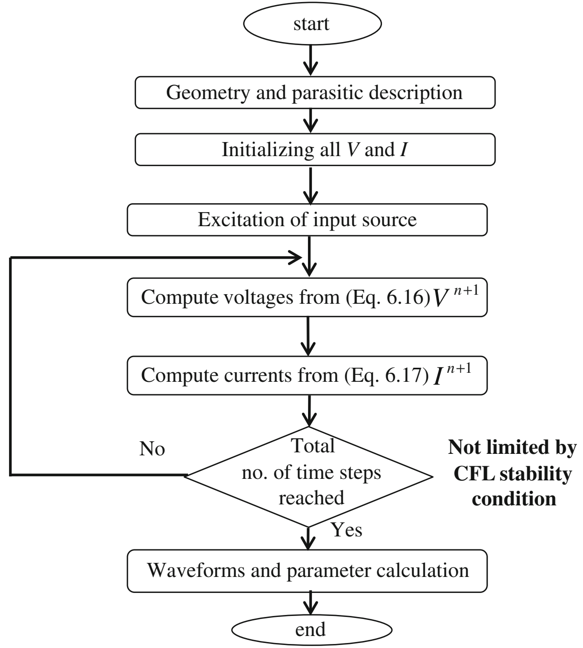

Fig. 6.4 Flowchart for evaluation of voltage and current using the proposed US-FDTD technique

6.2.4 Stability Analysis

This subsection analytically demonstrates that the proposed US-FDTD model is not limited by the CFL stability condition and is unconditionally stable. Representing Eqs. (6.12) and (6.13) together in matrix form results in

$$\boldsymbol{AM} + \boldsymbol{B}\frac{\partial \boldsymbol{M}}{\partial t} = \tilde{\boldsymbol{I}}_s + \tilde{\boldsymbol{X}}_r\frac{\partial \tilde{\boldsymbol{V}}_r}{\partial t} \tag{6.18}$$

where $\boldsymbol{A} = \begin{pmatrix} \boldsymbol{G} & \boldsymbol{P} \\ \boldsymbol{Q} & \boldsymbol{R} \end{pmatrix}$, $\boldsymbol{B} = \begin{pmatrix} \boldsymbol{C} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{L} \end{pmatrix}$, $\tilde{\boldsymbol{I}}_s = \begin{pmatrix} \boldsymbol{I}_s \\ \boldsymbol{0} \end{pmatrix}$, $\tilde{\boldsymbol{X}}_r = \begin{pmatrix} \boldsymbol{X}_r \\ \boldsymbol{0} \end{pmatrix}$, $\tilde{\boldsymbol{V}}_r = \begin{pmatrix} \boldsymbol{V}_r \\ \boldsymbol{0} \end{pmatrix}$, $\boldsymbol{M} = \begin{pmatrix} \boldsymbol{V} \\ \boldsymbol{I} \end{pmatrix}$. Performing finite difference in time domain, the Eq. (6.18) results in

$$\boldsymbol{A}\frac{\boldsymbol{M}^{n+1} + \boldsymbol{M}^n}{2} + \boldsymbol{B}\frac{\boldsymbol{M}^{n+1} - \boldsymbol{M}^n}{\Delta t} = \frac{\tilde{\boldsymbol{I}}_s^{n+1} + \tilde{\boldsymbol{I}}_s^n}{2} + \tilde{\boldsymbol{X}}_r\frac{\tilde{\boldsymbol{V}}_r^{n+1} - \tilde{\boldsymbol{V}}_r^n}{\Delta t} \tag{6.19a}$$

After rearranging, Eq. (6.19a) results in

$$\boldsymbol{M}^{n+1} = \boldsymbol{X}\boldsymbol{M}^n + \left(\frac{\boldsymbol{A}}{2} + \frac{\boldsymbol{B}}{\Delta t}\right)^{-1}\left(\frac{\tilde{\boldsymbol{I}}_s^{n+1} + \tilde{\boldsymbol{I}}_s^n}{2} + \tilde{\boldsymbol{X}}_r\frac{\tilde{\boldsymbol{V}}_r^{n+1} - \tilde{\boldsymbol{V}}_r^n}{\Delta t}\right) \tag{6.19b}$$

where $\boldsymbol{X} = \left(\frac{\boldsymbol{A}}{2} + \frac{\boldsymbol{B}}{\Delta t}\right)^{-1}\left(\frac{\boldsymbol{B}}{\Delta t} - \frac{\boldsymbol{A}}{2}\right)$.

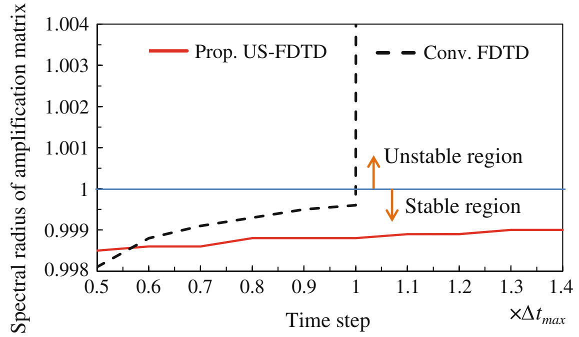

Fig. 6.5 Comparison of spectral radius of amplification matrix between proposed US-FDTD and conventional FDTD model

The matrix X is known as the amplification matrix of Eq. (6.19b). The model is stable if $\rho(X) \leq 1$, where $\rho(X)$ represents the spectral radius of X and can be expressed as [22]

$$\rho(\boldsymbol{X}) = \max(|eigen(\boldsymbol{X})|) \tag{6.20}$$

With the increase in time step size, beyond the CFL limit, the conventional FDTD techniques [7, 10, 11] results in instability. However, for the proposed model the value of (6.20) is always less than 1 for all values of time step. Considering the worst case of the time step size, tending to infinity, the amplification matrix of the proposed US-FDTD model tends to identity matrix that has spectral radius of 1. Therefore, the proposed model is stable for any value of the time step size and hence, unconditionally stable.

The stability of the proposed model is analyzed based on the value of $\rho(X)$, which is calculated from Eq. (6.20). Figure 6.5 shows the comparison of $\rho(X)$ between the proposed US-FDTD model and conventional FDTD model, at different time steps. It is observed that when Δt is greater than the CFL limit ($\Delta t_{\max}$), for the conventional FDTD model, $\rho(X) > 1$, whereas for the proposed US-FDTD model, $\rho(X) < 1$. Therefore, the proposed model is stable beyond the CFL stability condition as well [23]. The numerical example that demonstrates the unconditional stability of the proposed model is provided in Sect. 6.3.3.

6.3 Simulation Setup and Results

The proposed US-FDTD model is validated with the conventional FDTD model. Using the 32 nm technology, the width and thickness of the interconnect line are considered as 48 nm and 112.32 nm, respectively, with an aspect ratio of 2.34. The spacing between the interconnect lines and the height from the ground plane are assumed to be equal to the width and thickness, respectively. The interlevel metal

insulator dielectric constant, load capacitance and length of the line are 2.78, 2 fF and 0.5 mm, respectively. The line capacitive and inductive parasitics are extracted from the electrostatic and magnetostatic field solvers, respectively [24, 25]. The symmetric CMOS drivers are used to drive the coupled interconnect lines [26]. The input to the aggressor line is a falling ramp signal from 0.9 to 0 V with a transition time of 50 ps.

The interconnect line supports two different modes of propagation, i.e., even and odd modes in coupled lines. For given line parasitics, the corresponding even and odd mode velocities are evaluated as $v_1 = 1.49 \times 10^8$ m/s and $v_2 = 0.49 \times 10^8$ m/s, respectively. To maintain high accuracy, the line discretization value (Δz) is considered as 0.5×10^{-5} m. Based on the CFL stability condition, the maximum time step size ($\Delta t_{\max}$) while ensuring stable operation is 0.33×10^{-13} s.

6.3.1 Transient Analysis

The comprehensive crosstalk noise is analyzed at the far-end of the line 2 using proposed US-FDTD and conventional FDTD. The transient responses of functional, dynamic in-phase and dynamic out-phase crosstalk switching are shown in Figs. 6.6, 6.7 and 6.8, respectively. The input switching of interconnect lines is shown in the inset. For functional crosstalk, line 1 (aggressor) makes a transition from ground to V_{DD} while line 2 (victim) is at ground level. During dynamic in-phase crosstalk, both line 1 and line 2 switch from ground to V_{DD}. Finally, for dynamic out-phase crosstalk, line 1 and line 2 make the transition from ground to V_{DD} and from V_{DD} to ground, respectively. From Figs. 6.6, 6.7 and 6.8, it is observed that in all the three cases the proposed US-FDTD model accurately estimates the timing response with respect to the conventional FDTD model.

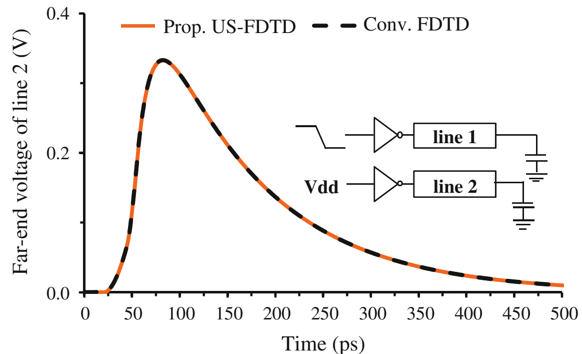

Fig. 6.6 Transient response comparison during the functional crosstalk

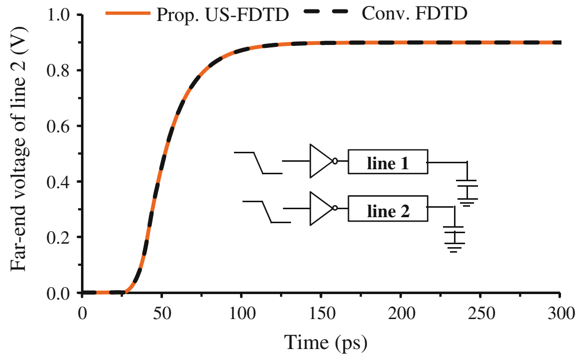

Fig. 6.7 Transient response comparison during the dynamic in-phase crosstalk

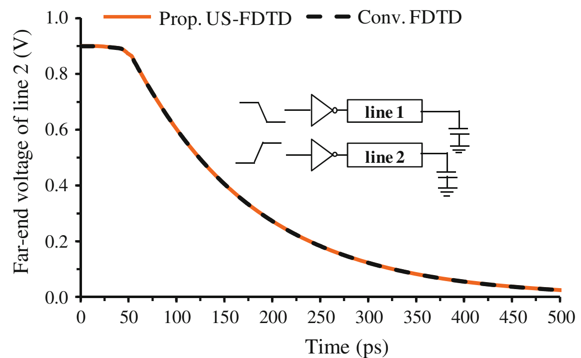

Fig. 6.8 Transient response comparison during the dynamic out-phase crosstalk

6.3.2 Crosstalk Induced Noise Peak, Width and Delay Analysis

When the generated noise has a peak voltage above the threshold voltage and attains a width above the threshold pulse width of the receiving gate, it leads to the generation of a glitch that may result in logical failure of the circuit [27]. Therefore, noise peak voltage and pulse width are the two important parameters for crosstalk noise analysis. Consequently, these parameters are estimated using the proposed US-FDTD model and conventional FDTD model. Table 6.3 shows the functional crosstalk noise peak voltage and pulse width at different load capacitances. The average percentage error is observed to be less than 1 % for noise peak voltage and noise width. It is also observed that as the load capacitance increases, the noise peak voltage decreases, whereas the noise width increases. This is because of the increase in time constant with the increase in load capacitance.

To further verify the accuracy of the proposed model, the dynamic in-phase and out-phase crosstalk induced delay are analyzed at different interconnect lengths. From Fig. 6.9, it can be observed that the proposed model accurately estimates the

Table 6.3 Noise peak voltage and noise width comparison between proposed US-FDTD and conventional FDTD simulations

Load capacitance (fF)	Peak voltage			Noise width		
	Proposed US-FDTD (V)	Conv. FDTD (V)	Error (%)	Proposed US-FDTD (ps)	Conv. FDTD (ps)	Error (%)
5	0.287	0.289	0.69	150.151	148.280	0.58
10	0.249	0.249	0	176.614	175.655	0.54
15	0.222	0.223	0.45	202.112	201.003	0.55
20	0.197	0.198	0.50	231.621	229.707	0.62

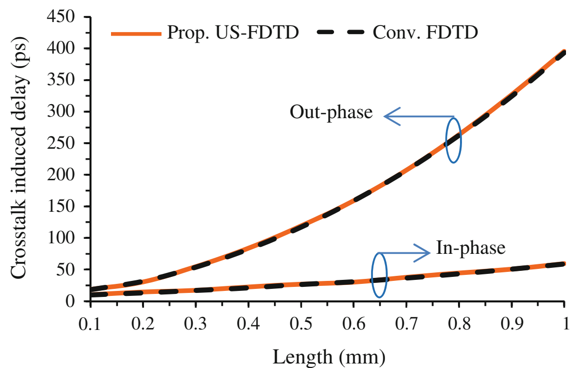

Fig. 6.9 Comparison of crosstalk induced propagation delay between proposed US-FDTD model and conventional FDTD model

crosstalk induced propagation delay for all interconnect lengths, with an average error of less than 1 %. It is also observed that the out-phase delay is higher than the in-phase delay. This is due to the fact that the Miller capacitance strongly influences the signal propagation during the out-phase switching, whereas it is ineffective during the in-phase switching.

6.3.3 Unconditional Stability of the Proposed Model

The stability of the proposed model is verified through a numerical example demonstrating the dynamic in-phase transient response. The transient response is analyzed at different time steps using both conventional and proposed US-FDTD.

The stability of the proposed model is analyzed in the following two cases:

(1) Within the CFL condition ($\Delta t = \Delta t_{max}$), from Fig. 6.10a it can be observed that both conventional FDTD and proposed US-FDTD models provide stable outputs;

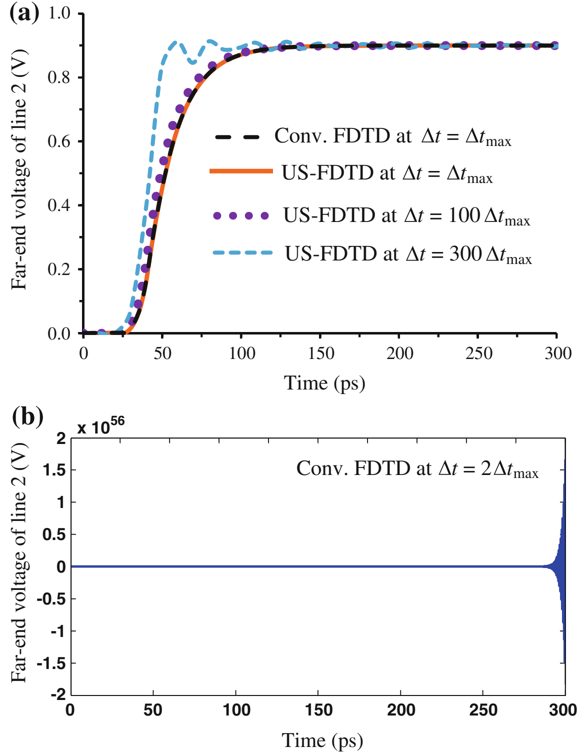

Fig. 6.10 Dynamic in-phase crosstalk analysis at different time steps **a** stable output of conventional FDTD and proposed US-FDTD and **b** unstable output of conventional FDTD due to the violation of CFL condition

(2) Beyond the CFL condition ($\Delta t > \Delta t_{max}$), from Fig. 6.10b it can be observed that the conventional FDTD model is unstable at $\Delta t = 2\Delta t_{max}$, whereas the proposed model is stable and sufficiently accurate, even when $\Delta t = 100 t_{max}$ (Fig. 6.10a). Although, at $\Delta t = 300\Delta t_{max}$ the proposed model output is stable but the accuracy reduces due to the lower resolution in temporal space. The stability of the proposed model is not limited by the CFL condition and is therefore unconditionally stable.

6.3.4 Efficiency of the Proposed Model

Using a PC with Intel Core i7 CPU (3.4 GHz, 8 GB RAM), the run-time of the proposed model is compared with the conventional FDTD. The computational effort for the transient analysis of dynamic in-phase crosstalk at different time steps is shown in Table 6.4. For $\Delta t \leq \Delta t_{max}$, the proposed US-FDTD model requires 89 %

Table 6.4 Comparison of computational efforts

Time step size, Δt	No. of iterations		CPU time (s)	
	Conventional FDTD model	Proposed US-FDTD model	Conventional FDTD model	Proposed US-FDTD model
$0.5\Delta t_{max}$	18,182	18,182	4.124	3.651
$1\Delta t_{max}$	9091	9091	2.056	1.824
$2\Delta t_{max}$	×	4545	×	0.914
$10\Delta t_{max}$	×	909	×	0.191
$50\Delta t_{max}$	×	182	×	0.037
$100\Delta t_{max}$	×	91	×	0.019

'×' represents the invalid instances since the conventional FDTD model becomes unstable for $\Delta t > \Delta t_{max}$

of the time utilized by the conventional FDTD model. It is worth noting that because the proposed model is unconditionally stable, it allows to consider larger time step, well beyond Δt_{max}. This further reduces the number of iterative steps required for analysis and consequently, reduces the computational run-time. As observed in Table 6.4, at $\Delta t = 100\Delta t_{max}$, where the conventional model results in unstable output, the proposed model requires only 0.9 % of the time required by conventional model at $\Delta t = \Delta t_{max}$. Therefore, depending on the time step size the proposed model can be up to 100 times faster than the conventional FDTD.

6.3.5 Comparison with 3D Simulations

The validity of the proposed model is further verified by the 3D simulations. Sentaurus TCAD simulator is used for the 3D simulations [28]. The interconnect width and spacing between the interconnect lines are equally considered as 48 nm, the thickness and height from the ground plane are equally considered as 112.32 nm. The interlevel metal insulator dielectric constant, load capacitance and length of the line are 2.78, 0.2 fF and 5 µm, respectively. The structure of the coupled interconnect line is shown in Fig. 6.11. The transient response at the far-end voltage of line 2 is observed during the functional crosstalk switching and shown in Fig. 6.12. It can be observed that the accuracy of the results via the proposed model is in good agreement with the 3D simulations. The average error between the proposed model and 3D simulation is less than 3 %. The CPU run-time and memory required by the proposed model are 0.02 s and 602 MB, respectively, whereas the 3D simulations require 964 s and 3066 MB, respectively.

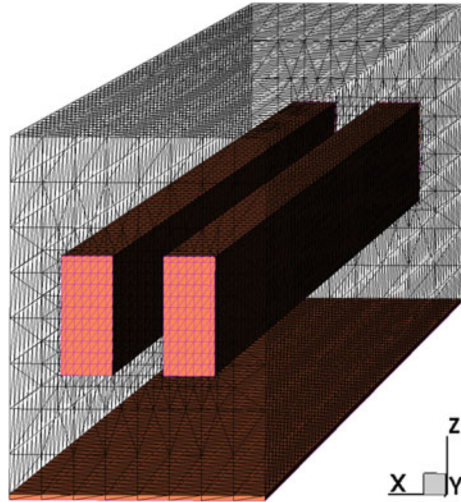

Fig. 6.11 Structure of two coupled interconnects

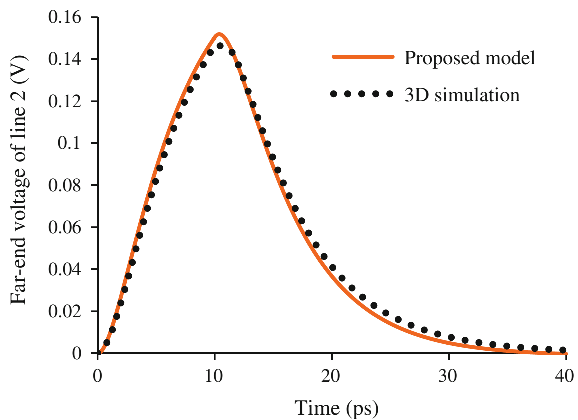

Fig. 6.12 Transient response comparison between the proposed US-FDTD model and 3D simulations at the far-end terminal of line 2 during the functional crosstalk switching

6.4 Performance Comparison of Cu, MWCNT and MLGNR Interconnects

In this sub-section, the propagation delay under the influence of crosstalk is analyzed among Cu, MWCNT and MLGNR interconnects. The simulations have been carried out using the US-FDTD method. The coupled interconnect line structures considered for the performance comparison of Cu/MWCNT/MLGNR is shown in Fig. 6.13. A CMOS driver with supply voltage V_{DD} = 0.9 V is used to drive the interconnect line. The relative permittivity of the inter layer dielectric medium is considered as 2.25. The width and spacing between coupled interconnects is equal to 48 nm and the distance from the ground plane is 86.4 nm.

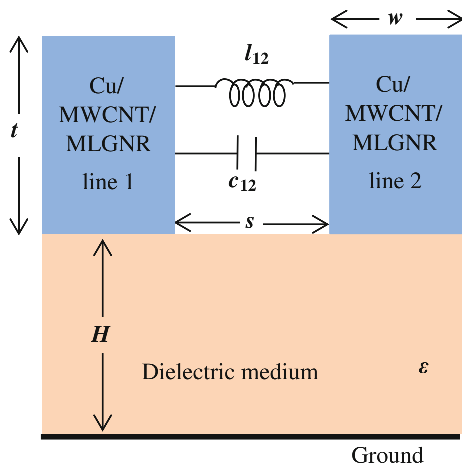

Fig. 6.13 Structure of two coupled interconnects

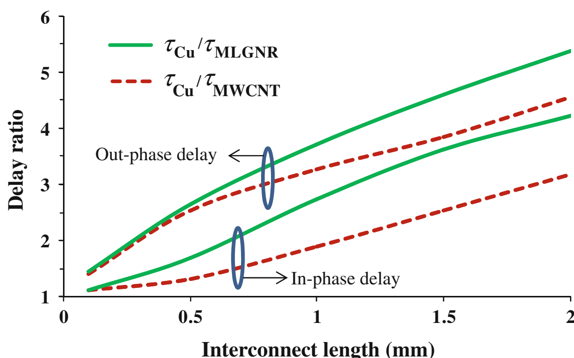

Fig. 6.14 Performance delay comparison among Cu, MWCNT and MLGNR interconnects

The crosstalk induced delay ratios of Cu to MLGNR (τ_{Cu}/τ_{MLGNR}) and MWCNT (τ_{Cu}/τ_{MWCNT}) are shown in Fig. 6.14. The AsF_5 doped MLGNR interconnect is used with intercalation doping density of E_F = 0.4 eV and back scattering probability of 0.2. The comparison plot shows that the crosstalk induced delay of MWCNT and MLGNR substantially reduces in comparison to the conventional Cu interconnect. This reduction is more prominent for out-phase switching due to the considerable reduction in coupling capacitance of MWCNT/MLGNR than Cu interconnects. Additionally, the crosstalk induced delay of MLGNR is smaller in comparison to MWCNT interconnects. The primary reason behind this reduced delay is the availability of more number of conduction channels in MLGNR than MWCNT. Therefore, the superior electrical properties and the fabrication compatibility with conventional lithography techniques make the MLGNR intrinsically more suitable material for on-chip interconnect realization. However, the intercalation doping of MLGNR with low back scattering probability is the primary challenge in designing a high performance MLGNR interconnect.

6.5 Summary

This chapter proposed a novel model based on US-FDTD technique, to analyze the crosstalk effects of coupled VLSI interconnects. It is analytically and numerically demonstrated that the proposed model is not limited by the CFL condition and is unconditionally stable. Using the proposed model, a comprehensive crosstalk analysis is performed and the results are in good agreement with the conventional FDTD model. The average percentage error is observed to be less than 1 % for the estimation of crosstalk induced performance parameters. Moreover, it is observed that the proposed model is highly time efficient than the conventional FDTD model. Depending on the time step size, the proposed model can be up to 100× faster than the conventional FDTD. Moreover, the performance comparison of Cu, MWCNT and MLGNR interconnects is also presented. It is observed that the MLGNR is the better suitable on-chip interconnect material than the Cu and MWCNT.

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