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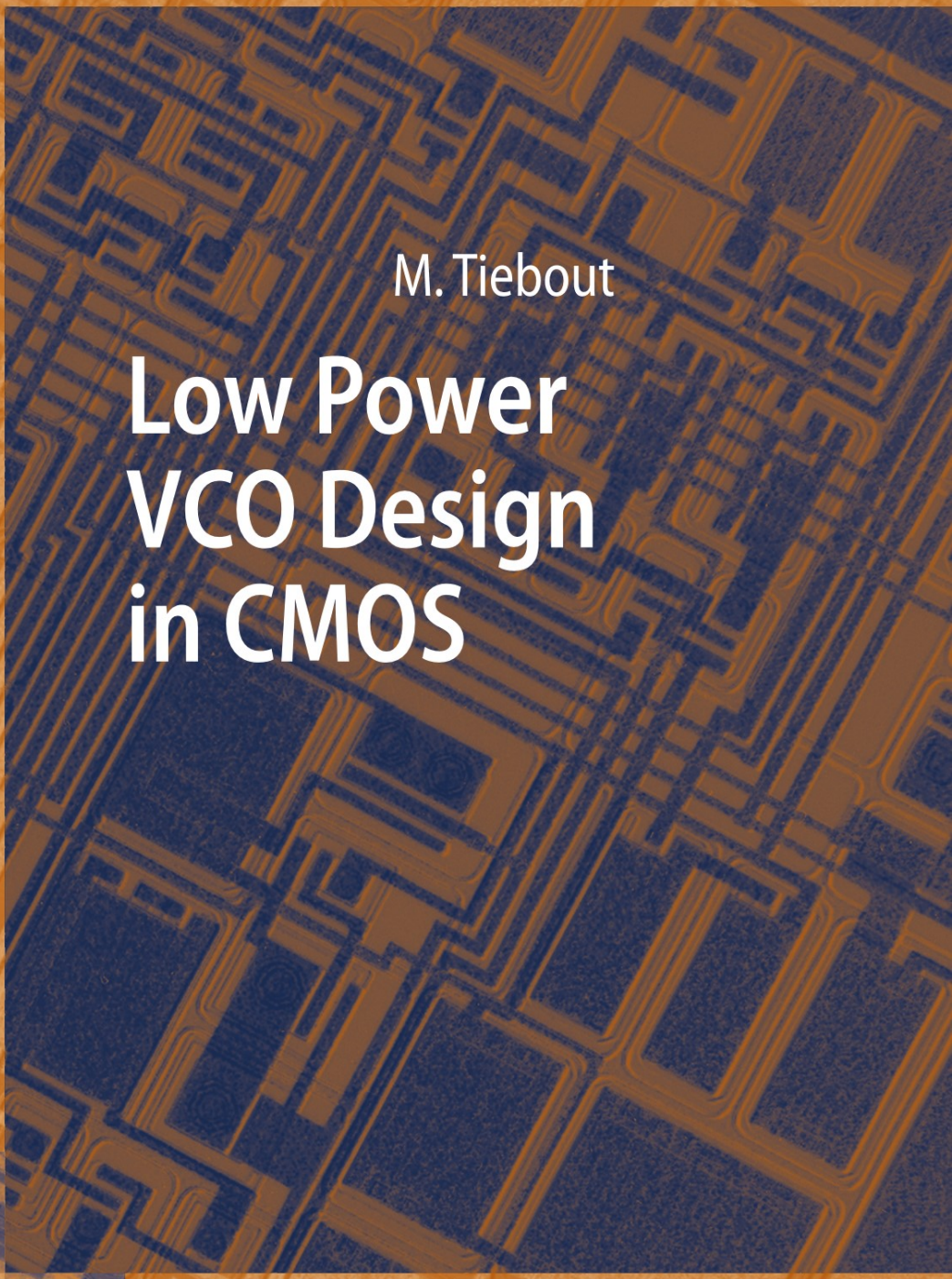

M. Tiebout

Low Power VCO Design in CMOS

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Marc Tiebout

Low Power VCO Design in CMOS

With 103 Figures

Springer

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To my grandfather Georges Smets

Preface

This work covers the design of CMOS fully integrated low power low phase noise voltage controlled oscillators for telecommunication or datacommunication systems.
The need for low power is obvious, as mobile wireless telecommunications are battery operated. As wireless telecommunication systems use oscillators in frequency synthesizers for frequency translation, the selectivity and signal to noise ratio of receivers and transmitters depend heavily on the low phase noise performance of the implemented oscillators. Datacommunication systems need low jitter, the time-domain equivalent of low phase noise, clocks for data detection and recovery. The power consumption is less critical.
The need for multi-band and multi-mode systems pushes the high-integration of telecommunication systems. This is offered by sub-micron CMOS featuring digital flexibility. The recent crisis in telecommunication clearly shows that mobile hand-sets became mass-market high-volume consumer products, where low-cost is of prime importance. This need for low-cost products enlivens tremendously research towards CMOS alternatives for the bipolar or BiCMOS solutions in use today.
Part I of this work treats VCO design. It starts with an introduction to VCO design, recapitulates various definitions and terminologies, then presents LC-VCO-phase noise theories. Energy conservation and VCO phase noise theory applied to the tank design leads to the concept of systematic high inductance LC-tank VCO design for low power low phase noise oscillator designs. In Part II the RF-properties of the active and passive devices in CMOS are revisited, from the viewpoint of the optimization guidelines formulated in the previous chapter. Especially varactors (variable capacitors) and integrated inductors are treated in detail, as their role is crucial for the VCO-performance. Finally, Part III of this work validates the proposed VCO design approach with fully integrated designs. First the guidelines of Part I and its realization based on the devices treated in Part II are summarized. A first VCO design at 1.3 GHz center frequency with a power consumption of 15 mW demonstrates the feasibility of a fully integrated CMOS oscillator for GSM. Next, as quadrature

solutions are necessary for complex modulation/demodulation, an overall low power low phase noise quadrature cross-coupled 1.8 GHz VCO design, featuring a power consumption of just 20 mW is presented. Its very low power consumption and low phase noise is mainly due the trivial but novel use of a NMOS/PMOS very digital topology without current source. The new differential MOS varactor tuning shows to be very effective in suppressing tuning common mode sensitivity and also can be used to reduce or solve the power supply sensitivity. Further potential of deep sub-micron CMOS is demonstrated with a 51 GHz low phase noise VCO in 0.13 μm CMOS, consuming only 1 mW. Finally, a tunable coil is introduced to extend the tuning range of LC-VCOs, before coming to the general conclusion in Part IV.

Munich, May 2005 *Marc Tiebout*

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Part I

VCO Design

1

VCO Basics

1.1 Definitions

1.1.1 Frequency Tuning

A general VCO can be treated as a black box with an input V_{tune} and a periodic oscillating output $V(t)$ depicted as drawn in Fig. 1.1. The VCO is

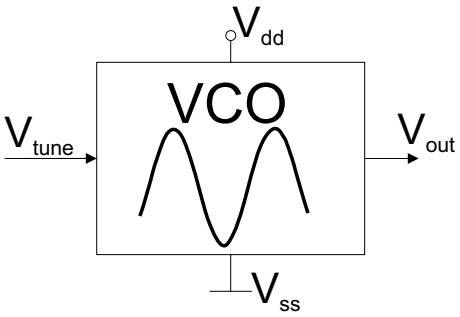

Fig. 1.1. Basic VCO

connected to the power supply through VSS and VDD. The output voltage $V_{out}(t)$, differential or single ended, is periodic:

$$V_{out}(t) = V_0 sin(\omega_c t + \varphi) \tag{1.1}$$

with phase φ, V_0 amplitude and angular carrier frequency

$$\omega_c(V_{tune}) = 2\pi f_c(V_{tune}) \tag{1.2}$$

which is dependent on the tuning voltage input V_{tune}, as a voltage controlled oscillator is needed. The frequency spectrum and time-domain output of an ideal oscillator is shown in Fig. 1.2.

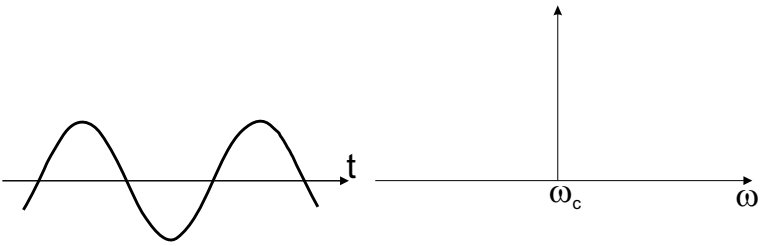

Fig. 1.2. Ideal oscillator output over time and corresponding frequency spectrum

1.1.2 VCO-Gain

VCOs are normally used in a phase locked loop (PLL) as voltage to frequency translation block. The transfer function of input voltage to output frequency

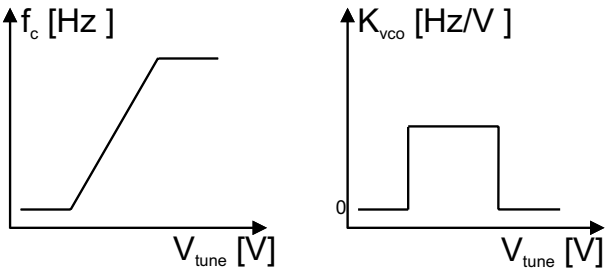

Fig. 1.3. VCO frequency transfer function

(e.g., Fig. 1.3) and its gain K_{VCO} is of main importance for PLL design (more in section 1.1.5).

$$K_{VCO} = \frac{d\,f_c}{d\,V_{tune}} \tag{1.3}$$

1.1.3 Pushing

Similarly as in the previous section, the transfer function from power supply to output frequency can be defined as:

$$K_{Vdd} = \frac{df_c}{dV_{dd}} \tag{1.4}$$

$$K_{Vss} = \frac{df_c}{dV_{ss}} \tag{1.5}$$

Unfortunately K_{Vdd} and K_{Vss} are not zero in real oscillators and can lead to severe problems if not specified at the very beginning design phase of a VCO.

1.1.4 Pulling

VCO output frequency also varies with the load attached to its output. This is called load pulling:

$$pulling = \frac{\Delta f_c}{\Delta load} \tag{1.6}$$

This parameter is mainly of concern for VCO-modules and usually defined for changing the VSWR of the load from 1 to 2 (see e.g [6]).

1.1.5 Phase Noise and Jitter

Definitions

As already stated, an ideal sinusoidal oscillator is described as

$$V_{out}(t) = V_0 cos[2\pi f_c t + \phi] \tag{1.7}$$

with constant amplitude V_0, center frequency f_c, and ϕ a fixed phase. In the frequency domain the spectrum of this oscillator consists of a Dirac-impulse at $\pm f_c$. A real oscillator is more generally given by

$$V_{out}(t) = V_0(t) y[2\pi f_c t + \phi(t)]. \tag{1.8}$$

y is a periodic function. The fluctuations introduced by $V_0(t)$ and $\phi(t)$ - now functions in time - result in sidebands close to f_c, with symmetrical distribution around f_c (Fig. 1.4) [11]. The frequency fluctuations correspond to jitter in the time-domain, which is a random perturbation of zero-crossings of a periodic signal (Fig. 1.5). Frequency fluctuations are usually characterized

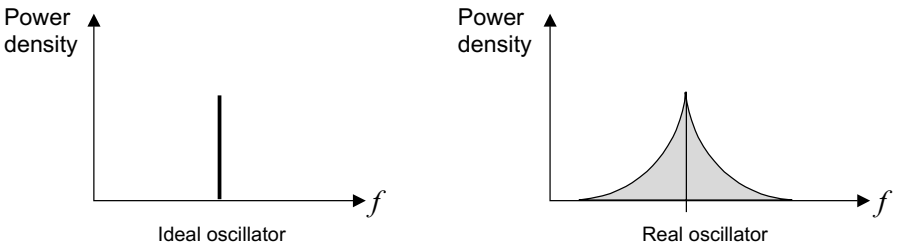

Fig. 1.4. Frequency spectrum of ideal and real oscillators

by the single sideband noise spectral density normalized to the carrier signal power (Fig. 1.4). It is defined as

$$\mathcal{L}_{total}(f_c, \Delta f) = 10 \log \left[\frac{\mathcal{P}_{sideband}(f_c + \Delta f, 1\,\mathrm{Hz})}{\mathcal{P}_{carrier}} \right] \tag{1.9}$$

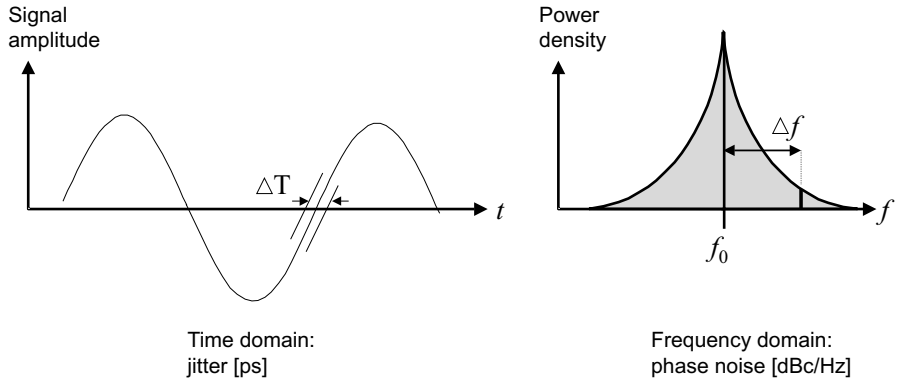

Fig. 1.5. Jitter in the time domain relates to phase noise in the frequency domain

and has units of decibels below the carrier per hertz (dBc/Hz). $\mathcal{P}_{carrier}$ is the carrier signal power at the carrier frequency f_c and $\mathcal{P}_{sideband}(f_c + \Delta f, 1\,\text{Hz})$ denotes the single sideband power at the offset Δf from the carrier f_c at a measurement bandwidth of 1 Hz.
The total phase noise $\mathcal{L}_{total}$ includes both amplitude $A(t)$ and phase $\phi(t)$ fluctuations. In practical oscillators the amplitude is limited by non-linear active devices and $\mathcal{L}_{total}(f_c, \Delta f)$ is dominated by the phase part of the phase noise [11, 55].
The time domain equivalent or jitter is characterized as the statistical distribution of the output signal period. This typically is assumed of gaussian distribution with mean value $\tau = 1/\omega_c$ and variance σ. The relation between clock jitter σ_τ and phase noise can be calculated as [11]:

$$\sigma_\tau^2 = \frac{4}{\pi {\omega_c}^2} \int_0^\infty S_\phi \omega \sin(\frac{\omega\tau}{2}) d\omega \tag{1.10}$$

with τ the clock period.

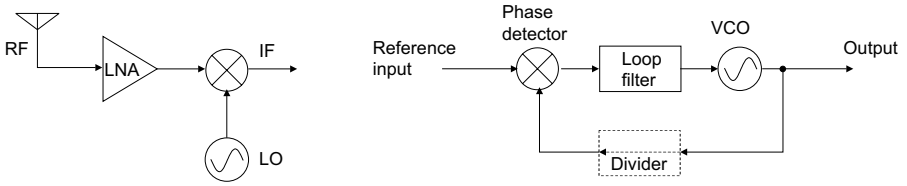

Fig. 1.6. Simplified receiver block diagram *(left)* and phase-locked loop *(right)*

Importance of Phase Noise

The front-end of a typical receiver is shown in Fig. 1.6, where a mixer and a local oscillator (LO) downconvert the incoming radio frequency (RF) signal to a lower, intermediate frequency (IF). With a LO frequency lower than the RF frequency (low-side LO) the resulting intermediate (IF) frequency is determined by: $f_{IF} = f_{RF} - f_{LO}$. To achieve absolute synchronization of the LO signals, the VCO is engaged in a phase-locked loop (PLL, Fig. 1.6). A typical PLL consists of a VCO, a frequency divider, a phase detector, a charge pump, and a low-pass loop filter. It forces the output frequency to be equal to a multiple of the input reference frequency [11, 55]. PLL design is eased significantly with a VCO offering a linear dependence between tuning voltage and frequency. To understand the importance of phase noise Fig. 1.7 depicts

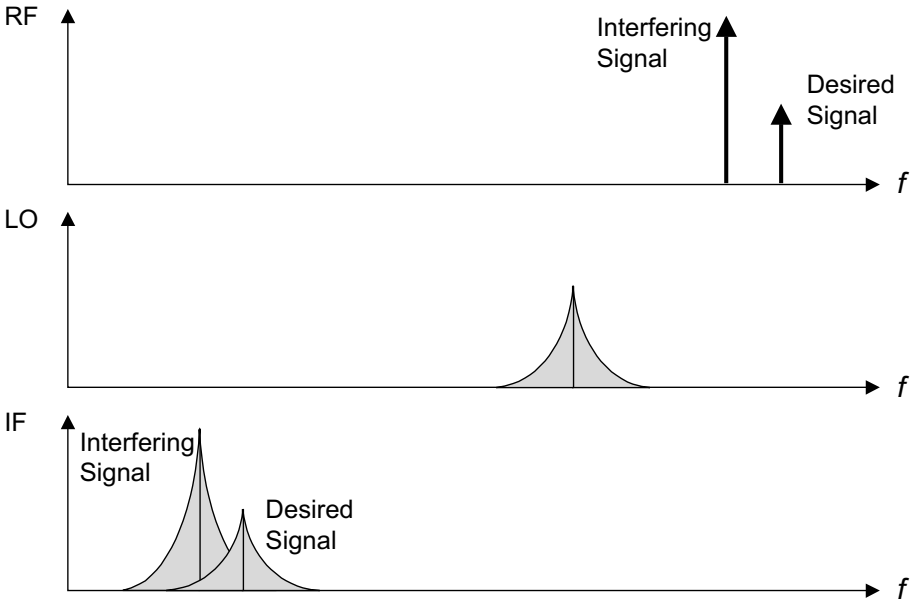

Fig. 1.7. Effect of oscillator phase noise in a receiver

the situation in a receiver. The LO signal used for downconversion has a noisy spectrum. Besides the wanted signal with small power an unwanted signal with large power is present in an adjacent channel (at a close-by frequency). After mixing with the LO the downconverted spectrum consists of two overlapping spectra. The wanted signal suffers from significant noise due to in-band signal from the downconversion of the interferer by the LO sideband: the signal-to-noise ratio is degraded [56]. In order to be able to detect the signals from

all channels while (stronger) interferers may be present stringent phase noise specifications have to be met in wireless communication systems.

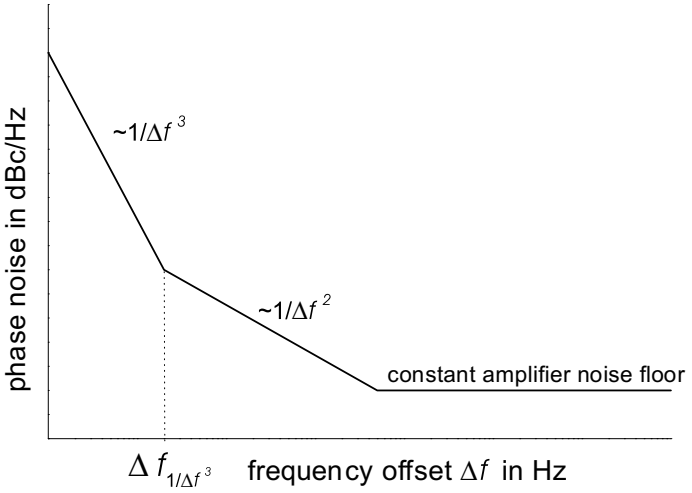

Fig. 1.8. Typical phase noise spectrum of a LC-oscillator

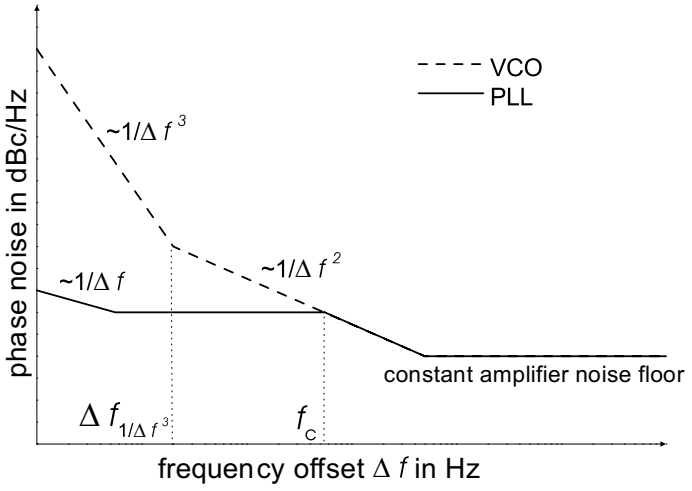

Fig. 1.9. Noise spectra of the VCO and the resulting PLL output

Phase Noise and The Impact on PLL Noise

A typical single side band phase noise spectrum is given in Fig. 1.8 [11, 55]. At low offset frequencies up to a corner frequency $\Delta f_{1/\Delta f^3}$ a $1/\Delta f^3$ behavior, also called flicker-noise behavior, is observed. For medium offset frequencies the phase noise shows a $1/\Delta f^2$-dependence, also called white-noise behavior, up to where the constant amplifier noise floor begins to dominate. PLL noise is mainly determined by noise introduced by the reference signal and the VCO. A thorough analysis of the transfer characteristic and loop response to noise signals shows that the PLL functions as high-pass for the noise from the VCO [55]. Above a cut-off frequency f_c, noise passes unattenuated. f_c is determined by the overall forward gain of the loop and the order of the divider [55]. Due to the existence of many adjacent channels specifications for the maximum PLL noise output have to be met. Figure 1.9 compares the spectra of the VCO noise and the resulting PLL noise output. Below f_c the output characteristics are dominated by the PLL transfer function. Output noise is significantly reduced compared to the "input" from the VCO. Above f_c essentially the VCO noise will be observed. Below f_c the resulting PLL noise is determined by the PLL design and the VCO phase noise, which can be exploited to suppress the flicker-noise region of VCO phase noise through adequate PLL design.

Table 1.1. VCO specification list

spec	**Unit**
Center frequency	GHz
Tuning Range	MHz
Phase noise	dBc/Hz @ offset [kHz]
Power consumption	mW
Supply voltage	V
VCO-Gain	MHz/V
Pulling	MHz/load-spec
Pushing	MHz/V
Area	μ m ^{2}
Cost	$
Operating temperature	°C
Manufacturability	
Yield	%
Lifetime	Years

1.2 Requirements

Table 1.1 summarizes the general specifications for (integrated) VCO design. Main specifications are center frequency, tuning range, power supply voltage, power consumption and phase noise specifications. But additional specifications like cost or chip area, pulling, pushing, etc. must be fulfilled aiming at products in CMOS. For instance, a reliable operation over many years can only be met when taking into account all limits of a given CMOS technology, including the maximum allowed gate oxide voltages. Especially the pushing problem is often neglected, although it easily becomes a critical problem for the performance of a fully integrated synthesizer. Very few pushing data are included in the common VCO literature. However, typical pushing behavior is clearly documented and specified for real products, e.g. VCO modules [5, 6]. Also pulling usually is not treated, but this problem is less severe and mainly concerns careful output buffer design.

1.3 Integrated VCO Circuit Options

1.3.1 Ring Oscillators

A classical oscillator circuit solution is the connection of amplifiers or inverting in a ring of amplifiers or inverters. If the phase shift over the ring is 360 °, it will oscillate. An exemplary appliction is shown in Fig. 1.10. Ring oscillators

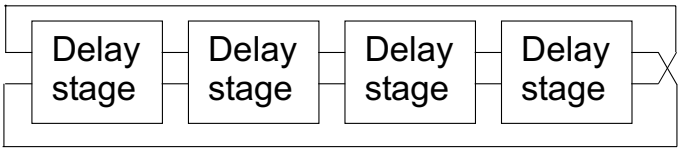

Fig. 1.10. Exemplary ring oscillator topology

have a very small area and are easy to integrate and design. They feature wide tuning ranges. Main disadvantage is their high power consumption and phase noise [21, 55, 94, 99]. Recent work, e.g. [21], show that it is possible to design low phase noise ring-oscillator's, but still at a much higher power consumption than for LC-VCOs.

1.3.2 LC Oscillators

A general LC-VCO can be symbolized as in Fig. 1.11. The oscillator consists of an inductor L and a capacitor C, building a parallel resonance tank, and an active element -R, compensating the losses of the inductor (R_L in Fig. 1.11)

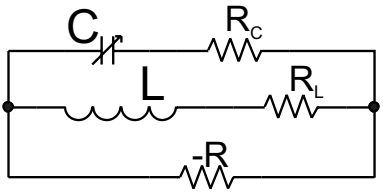

Fig. 1.11. Basic LC-VCO

and the losses of the capacitor (R_C in Fig. 1.11). The circuit results into an oscillator with angular center frequency.

$$\omega_c = \frac{1}{\sqrt{LC}} \tag{1.11}$$

As the capacitance C is proportional to the tuning voltage input V_{tune}, also ω_c is dependent on V_{tune} and the oscillator results in a voltage controlled oscillator. The capacitor C in Fig. 1.11 not only consists of a variable capacitor to tune the oscillator, but it also includes the parasitics or fixed capacitances of the inductor, the active elements, and of any load connected to the VCO (output driver, mixer, prescaler, etc.).
In comparison to ring oscillators, LC oscillators have a rather limited tuning range, but feature lower phase noise at a lower power consumption. The area of an LC oscillator with an integrated coil is much bigger than the area of a ring oscillator. This holds for designs aiming at widely spread GSM, UMTS, DCS1800, ... applications in the frequency range of 900 MHz to 2 GHz, for higher frequency upcoming applications as WLAN (5.2 GHz, 5.7 GHz, 17.2 GHz) coil area is not important any more, as the coil size decreases with higher frequencies.

1.4 VCO Figure of Merit

The performance of VCOs is difficult to compare as they feature different center frequencies, power consumption P_{supply}, and phase noise over offset-frequency. A widely accepted figure of merit has been introduced in [85]:

$$\text{FOM} = \mathcal{L}(f_0, \Delta f) + 10 \log \left(\left(\frac{f_0}{\Delta f} \right)^2 \frac{P_{supply}}{[mW]} \right). \tag{1.12}$$

where $\mathcal{L}(f_0, \Delta f)$ is the single-side-band noise at the offset frequency Δf from the carrier frequency f_0. This FOM is a direct deviation of Leesons empirical phase noise ([33], Eqn. (3.10)) expression normalized to the power consumption. For a fair comparison the worst-case measured phase noise of a VCO-design should be taken into account (unfortunately many authors tend

to calculate a best-case FOM at, e.g., zero tuning voltage input). The performance of a VCO is regarded to be better with a more negative value or higher absolute value of the figure of merit.

1.5 Summary

This chapter summarized general definitions concerning the VCO design and a long list of requirements to oscillators.
To fulfill the very tough combination of low power consumption (battery operation) and ultra-low phase noise needed for telecommunications, the remaining text limits the subject to LC-VCO circuits, as generally their phase noise performance is superior to the phase noise of, e.g., ring-oscillators.

2

Tank Properties

2.1 Introduction

As LC-VCOs are based on LC-tanks, the properties of the tank are likely very important for the VCO performance. Various tank representations and many quality factor Q definitions are in use. Not only for tanks or resonators but also for passive devices, inductive or capacitive, Q-factors have been defined. Before going into the details of the LC-VCO design for lowest power and lowest phase noise, Q definitions and notations are treated in depth, sorted and clearly defined. In electronics many Q-definitions are in use in various applications like tanks, filters, control systems, etc. but quality factors also are known from optical systems or from mechanical systems: clocks, spring-mass systems, controllers, lasers, ...

2.2 Q-Definitions

2.2.1 Energy

Probably the most general definition refers to Q as the energy stored, divided by the energy dissipated per cycle [11, 102].

$$Q_E = \frac{\omega_c E_{stored}}{P_{diss}} \tag{2.1}$$

Obviously this also can be applied to optical, mechanical, and other systems [48].

2.2.2 Reactive to Resistive Impedance

For passive components (capacitors and inductors), in analogy to the Q_E, quality factor has been generalized and is commonly defined as

$$Q_C, Q_L = \frac{reactive\,impedance}{real\,impedance} \tag{2.2}$$

This quality factor is widely used as conventional quality factor in many inductor papers [13, 25, 64]

$$Q_{CONV} = \frac{im(y11)}{re(y11)} \tag{2.3}$$

2.2.3 Bandwidth

Bandwidth quality factor Q_{BW} is defined for bandpass characteristics of filter or resonator amplitude responses as the ratio of the the center frequency to the 3 dB-bandwidth:

$$Q_{BW} = \frac{\omega_c}{\Delta\omega_{3dB}} \tag{2.4}$$

It is easily visualized in a bode plot and concerns the amplitude response (Fig. 2.3).

2.2.4 Phase Stability

The phase stability quality factor is a measure for the phase steepness of resonators or filters and is defined as

$$Q_{PS} = -\frac{\omega_c}{2}\frac{d\phi}{d\omega} \mid \omega = \omega_c \tag{2.5}$$

It is easily visualized in a bode plot and concerns the phase response (Fig. 2.3).

2.3 LC-Tank Properties

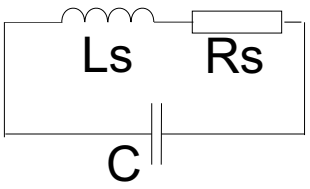

Fig. 2.1. Series resistance tank

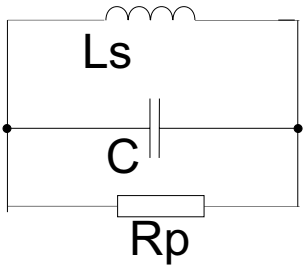

Fig. 2.2. Parallel resistance tank

2.3.1 Series and Parallel Resistance

In this work the representation of Fig. 2.1 is preferred over representation of Fig. 2.2 as it is closer to the physical losses in integrated inductors and improves the insight into optimal inductor design. The representation of Fig. 2.1 however is easily transformed to the representation of Fig. 2.2 with

$$R_p = \frac{L_s}{CR_s} \tag{2.6}$$

clearly showing that R_p is a difficult-to-handle design parameter as it is dependent on R_s, C, and L_s. With Eqn. (2.13) R_p can be rewritten as:

$$R_p = Q_{tank}^2 \, R_s \tag{2.7}$$

2.3.2 Center Frequency

An LC-tank can be treated as a bandpass filter, its center frequency is the frequency f_c (or angular frequency $\omega_c = 2\pi f_c$) where the amplitude response reaches its maximum. For the tanks of Figs 2.1 or 2.2 it is easily calculated that:

$$\omega_c = \frac{1}{\sqrt{LC}} \tag{2.8}$$

2.3.3 Tank Q

The quality factors listed above applied to LC-tanks lead to very different results.

Conventional Q

Q_{conv} equals to zero at resonance frequency, so it is useless for LC-tank considerations. Unfortunately Q_{CONV} is widely used to characterize and present integrated inductors, which can lead to improper optimization of inductors [65].

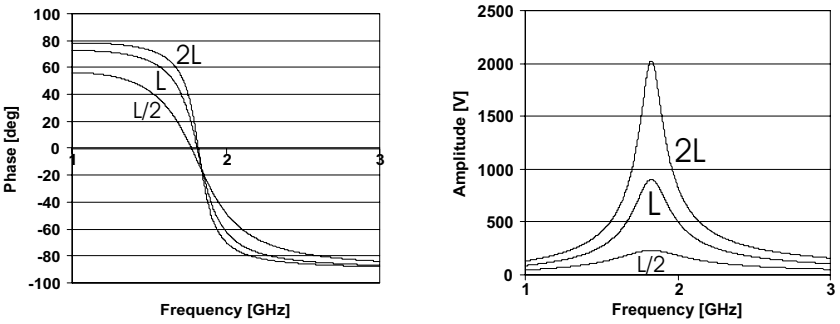

Fig. 2.3. LC-tank bode plot, constant R_s, varying L/C ratio

Energy Q

For the tank of Fig. 2.1 the energy is flowing from the inductor to the capacitor and back, and equals: $E_{stored} = L_s I^2_{max}/2$. The dissipated power is due to the current flowing through the series resistor: $P_{diss} = R_s Imax^2/2$, so Eqn. (2.1) simplifies to

$$Q_{E-tank} = \frac{\omega_c L_s}{R_s} \tag{2.9}$$

Phase Stability Q

For the LC-tank of Fig. 2.1 Q_{PS} straightforward impedance calculations lead to

$$Q_{PS-tank} = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{2.10}$$

or with Eqn. (1.11) again:

$$Q_{PS-tank} = \frac{L}{R}\,\omega_c \tag{2.11}$$

Bandwidth Q

Also Q_{BW} of Fig. 2.1 can be shown to simplify to

$$Q_{BW-tank} = \frac{\omega_c L_s}{R_s} \tag{2.12}$$

The plot in Fig. 2.3 provides a physical feeling of these equations for the circuit designer. Keeping R_s and resonance frequency constant, it shows the amplitude and phase response for the tank of Fig. 2.1 for different L/C ratios. A higher L/C ratio results in the phase domain into a steeper phase rolloff, or higher Q_{PS}. The amplitude representation shows that higher L/C-ratios correspond to more smallband bandpass filters, or to a higher Q_{BW}.

2.4 Conclusion

Starting from the most general and physical energy-based Q-definition, a long list Q-factors arising from many applications was sorted and clearly defined. Clear naming conventions Q_E, Q_{PS}, Q_{BW}, Q_L, Q_C, Q_{conv} were introduced. For the LC-tanks (Fig. 2.1, 2.2) of greatest importance for this work, it was clearly shown that

$$Q_{tank} = Q_{E-tank} = Q_{PS-tank} = Q_{BW-tank} = \frac{\omega_c L_s}{R_s} \tag{2.13}$$

So all relevant Q-factors equal to the most general Q-definition based on energy considerations. Starting from here, further references to tank quality factor Q_{tank} in this work, all refer to Eqn. (2.13).

3

VCO Design Theory

3.1 Introduction

For a specified frequency, tuning range, and maximal allowed phase noise, the design problem to be solved is the dimensioning of the few active and passive components of a typical LC-VCO (e.g. Fig. 1.11) for minimal power consumption. The design variables obviously are the inductor parameters (mainly R_s and L_s), the total tank capacitance C, the width and length of the transistors and the bias current. Unfortunately the interdependences of the design parameters are very complex, resulting in a huge number of VCO-theories, approaches, papers, and books in open literature. Although oscillators have been designed for over 50 years, in recent years, numerous "new" phase noise theories have been proposed, leading to additional insight in the upconversion of white and/or flicker noise into phase noise. The following sections first recapitulate old and widely used oscillator theories, before comparing them to the results of more recent proposals.

3.2 Barkhausen Oscillator Criteria

Barkhausen's [42, 97] 2-port model of an oscillator treats the LC-VCO as a an active element or amplifier G and a feedback network H, as presented in Fig. 3.1, where $G(V, j\omega)$ represents the transfer function of the amplifier as a function of the input amplitude and angular frequency, and $H(V, j\omega)$ the transfer function of the feedback network, also as a function of input amplitude and frequency.
Assuming a linear amplifier and a linear feedback network, $G(V, j\omega)$ reduces to $G(j\omega)$ and $H(V, j\omega)$ to $H(j\omega)$. A straightforward analysis now arrives at the well-known Barkhausen oscillator criteria. Obviously

$$V_{out} = G(j\omega)V_G \tag{3.1}$$

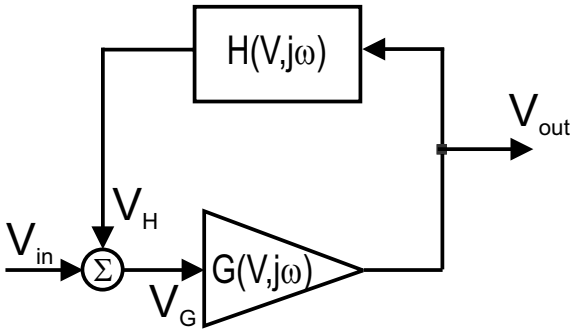

Fig. 3.1. Barkhausen 2-port model

and

$$V_H = H(j\omega)V_{out} \tag{3.2}$$

With

$$V_G = V_{in} + V_H \tag{3.3}$$

the transfer function of the complete network is calculated as:

$$\frac{V_{out}}{V_{in}} = \frac{G(j\omega)}{1 - H(j\omega)G(j\omega)} \tag{3.4}$$

which is instable if

$$|H(j\omega)||G(j\omega)| \geq 1 \tag{3.5}$$

As long as the left-hand side of the above expression > 1, oscillation amplitude will grow. Due to non-linear and saturation effects a steady-state amplitude will be reached where:

$$|H(j\omega)||G(j\omega)| = 1 \tag{3.6}$$

For the phase

$$\Phi_{G(j\omega)} + \Phi_{H(j\omega)} = 0 + 2\pi k \qquad k = 1 \ldots n \tag{3.7}$$

is valid with $\Phi_{G(j\omega)}$ and $\Phi_{H(j\omega)}$ the phase of $G(j\omega)$ and $H(j\omega)$. Equations (3.5) and (3.7) are well known as Barkhausen oscillator criteria. Assuming a zero degree phase shift over the active part $G(j\omega)$, Eqn. (3.7) reduces to

$$\Phi_{H(j\omega)} = 0 \tag{3.8}$$

Applying this criterion to the tanks of the previous chapter results in a frequency of oscillation

$$\omega_{osc} = \frac{1}{\sqrt{LC}} = \omega_c \tag{3.9}$$

3.3 Leeson's Empirical Phase Noise Expression

In 1966 Leeson [33, 67] set up the following empirical expression for the phase noise of a resonator-based VCO:

$$\mathcal{L}(\omega_c, \Delta f) = 10 \log \frac{2FkT}{P_{sig}} \underbrace{\underbrace{\left[1 + \left(\frac{\omega_c}{2Q_L \Delta\omega}\right)^2\right]}_{\frac{1}{\Delta\omega^2}} \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)}_{\frac{1}{\Delta\omega^3}}. \tag{3.10}$$

where Q_L is the loaded quality factor of the tank, $\Delta\omega = 2\pi\Delta f$ is the angular frequency offset, and F is called the device noise excess factor or simply noise factor. $\Delta\omega_{1/f^3}$ describes the flicker noise corner frequency and is not equal to the device flicker noise corner frequency. Equation (3.10) shows that one obvious way to reduce phase noise, is to increase $P_{sig} \propto {V_{peak}}^2$. For practical oscillators obviously V_{peak} is limited by the power supply voltage, or the maximal allowed power supply voltage. After Eqn. (3.10) the most effective way to lower phase noise seems to use a LC-tank with a higher Q or higher L/R_s ratio.
Neglecting the flicker-noise portion and with $Q_{tank} = \omega_c L/R_s$, $\omega_c >> \Delta\omega$ and $P_{sig} = V_{sig}^2/(2R_p) = V_{sig}^2/(2Q_{tank}^2 R_s)$ Leeson's equation simplifies to:

$$\mathcal{L}(\Delta\omega) = 10log[\frac{F\,kT\,R_s}{V_{sig}^2}\frac{\omega_c^2}{\Delta\omega^2}] \tag{3.11}$$

describing the $1/\omega^2$ portion of the phase noise.
The flicker noise is described empirically and no insight is provided into the upconversion mechanisms. But still Eqn. (3.10) shows that improving phase noise through signal swing maximization or by Q maximization will also improve the flicker noise phase noise region.

3.4 Linear Approach

The $1/f^2$ region of Eqn. (3.10) for an LC oscillator as shown in Fig. 3.2 can be explained using a simple linear approach.

The impedance of the parallel RLC-tank at offset frequency $\Delta\omega$ around its center frequency ω_c is approximated as:

$$Z(\omega + \Delta\omega) = R_p \frac{1}{1 + j2Q_{tank}\frac{\Delta\omega}{\omega_c}} \tag{3.12}$$

with R_p being its parallel resistance. For steady-state oscillation, the active part of the oscillator cancels the losses and $G_m(V).R_p = 1$ must hold (Eqn. (3.5)). So

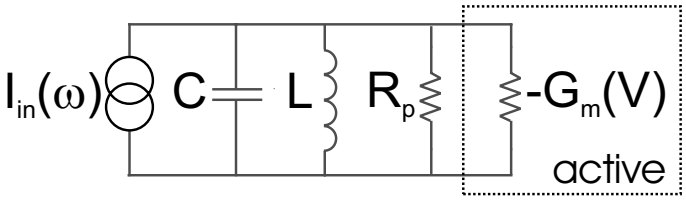

Fig. 3.2. Linear LC-VCO model

$$Z(\Delta\omega) = -jR_p \frac{\omega_c}{2Q_{tank}\Delta\omega} \tag{3.13}$$

The output noise density can be calculated as

$$S_{out}(\Delta\omega) = S_{in}(\Delta\omega).Z(\Delta\omega)^2 \tag{3.14}$$

with input noise density $S_{in}(\Delta\omega) = 4kT/R_p$ which is replaced by $S_{in}(\Delta\omega) = 4kFT/R_p$ to account for the excess noise of the active part by a noise factor F. Of course $F > 1$. Calculating

$$S_{out}(\Delta\omega) = \frac{4kTF}{R_p}\left(-jR_p \frac{\omega_c}{2Q_{tank}\Delta\omega}\right)^2 = 4kTF\,\frac{R_p\omega_c^2}{(2Q_{tank}\Delta\omega)^2} \tag{3.15}$$

This noise actually is amplified sideband noise, which can be split up into an amplitude modulation and phase modulation component [27]. A real oscillator acts like a limiter circuit and eliminates the amplitude portion of the phase noise, so phase noise is calculated as

$$\mathcal{L}(\Delta\omega) = 10log\left(\frac{\frac{1}{2}S_{out}(\Delta\omega)}{\frac{V_0^2}{2}}\right) \tag{3.16}$$

with V_0 the steady-state voltage amplitude output of the oscillator, leading to the phase noise estimation:

$$\mathcal{L}(\Delta\omega) = 10log\left[\frac{2FkTR_p}{V_0^2}\left(\frac{\omega_c}{2Q_{tank}\Delta\omega}\right)^2\right] \tag{3.17}$$

or with $P_{sig} = V_0^2/R_p$

$$\mathcal{L}(\Delta\omega) = 10log\left[\frac{2FkT}{P_{sig}}\left(\frac{\omega_c}{2Q_{tank}\Delta\omega}\right)^2\right] \tag{3.18}$$

which is identical to the Leeson expression for $\omega_c >> \Delta\omega$.

3.5 Craninckx Linear Approach

Similarly as in the previous section, in [55] Craninckx calculates the phase deviation for an LC oscillator using a linear phase model around ω_c for different noise source: tank inductor series resistance R_s, tank capacitor series resistance R_c, and tank parallel resistance R_p. The result of the analysis states:

$$\mathcal{L}(\Delta\omega) = \frac{2kT\,R_{eff}\,(1+F)(\frac{\omega_c}{\Delta\omega})^2}{{V_0}^2} \tag{3.19}$$

with F the excess noise factor, V_0 the tank voltage amplitude, and effective resistance

$$R_{eff} = R_s + R_c + \frac{1}{R_p(\omega_c C)^2} \tag{3.20}$$

The result is nearly identical to Eqn. (3.11).

3.6 Mixer Approach

Rael proposes in [57] a non-linear approach to the analysis of phase noise in oscillators. In contradiction to the two previous sections, the assumption $G(V, j\omega)$ reducing to $G(j\omega)$ is not used. The analysis is based on the NMOS only tail biased VCO-topology as presented in Fig. 3.3 and is validated against SpectreRF-simulations [24]. The large signal analysis treats the NMOS pair Ma, Mb as a mixing pair upconverting the white noise sources of the tank and of the active devices, and again comes to a Leeson-like formula:

$$\mathcal{L}(\Delta\omega) = F\frac{4FkTR_p}{{V_0}^2}(\frac{\omega_c}{2Q_{tank}\Delta\omega})^2 \tag{3.21}$$

with

$$F = 2 + \frac{8\gamma R_p I_T}{\pi V_0} + 8/9\gamma g m_{bias} R_p \tag{3.22}$$

and R_p the equivalent parallel resistance of the LC-tank, $V_0 = (4/\pi)R_p I_T$ the amplitude over the tank, I_T the tail current through transistor Mbia, and γ the thermal noise factor of a MOSFET ($\gamma \cong 2/3$).
Inserting in $R_p = Q^2 R_s$ (3.21) simplifies to

$$\mathcal{L}(\Delta\omega) = F\frac{4FkTR_s}{{V_0}^2}(\frac{\omega_c}{2\Delta\omega})^2 \tag{3.23}$$

leading to exactly the same dependence on R_s and L_s as predicted by Leeson or the linear approach of Craninkx. In contrast to Leeson and Craninckx, it gives VCO-designers valuable insight into the relation between the dimensioning of the active part and the noise factor F.

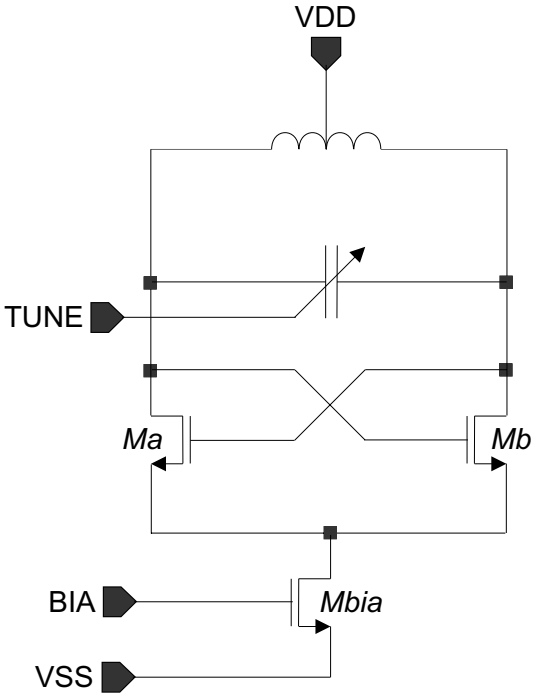

Fig. 3.3. VCO topology

3.7 Hajimiri's Linear Time Variant Approach

In [11] a time-variant phase noise model for oscillators is proposed. The basic idea behind the theory is that a current noise source injecting charges into the oscillator has a different impact on the oscillator phase over the oscillator time period. A so-called time-domain impulse sensitivity transfer function (ISF) is calculated characterizing the phase impact over the period.

$$\mathcal{L}(\Delta\omega) = \frac{{\Gamma_{rms}}^2}{q_{max}^2} \frac{\overline{i_n^2}/\Delta f}{4\Delta\omega^2} \tag{3.24}$$

with Γ_{rms} being the mean value of the ISF function and q_{max} the maximum charge across the tank capacitor. The ISF is a function that shows the sensitivity of every point of the periodic waveform to an input charge impulse. When a given perturbation causes a large phase shift, the ISF is large, while it is small in the opposite case. For the ideal oscillator of Fig. 3.4 it is zero at peak voltages and maximal at the zero crossings as shown in Fig. 3.5. The linear time variant approach is very useful to explain qualitatively the upconversion of flicker noise and the contribution of tail current sources to oscillator phase noise. For design trade-off and phase noise optimization of LC-oscillators Eqn.

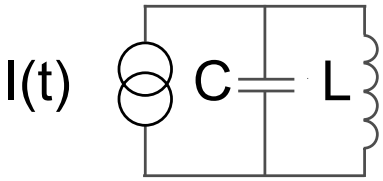

Fig. 3.4. Ideal LC-oscillator topology

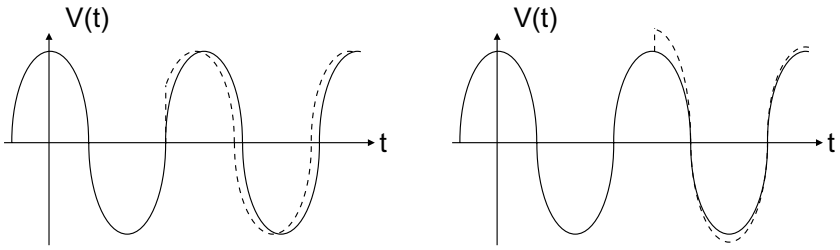

Fig. 3.5. Phase impulse response of the ideal oscillator topology

(3.24) however is not very useful as Γ_{rms} depends in a complex way on all design parameters and a spice-like simulator is needed to calculate Γ_{rms} (If a simulator is needed anyway, it can be used to simulate the phase noise instead of ISF).
Hajimiri [10, 11, 28] furthermore states that phase noise is minimized by maximizing C (or minimizing L), besides the trivial maximization of V_0.

3.8 Summary

In this chapter the main and most cited VCO-theories were recapitulated. All approaches linearize the active part and/or the tank transfer function and are able to explain the $1/\Delta\omega^2$ region of oscillator phase noise. A non-linear analytical treatment of active and passive parts has not yet been published, probably because it is simply too complex and designers must rely on simulators as SpectreRF or TITAN at design phase, especially when investigating the complex upconversion processes of flicker noise.
Due to this complexity and as flicker noise can be suppressed through adequate PLL design, the rest of this work neglects at first order the flicker noise performance of VCOs and concentrates on the optimization of the $1/\Delta\omega^2$ oscillator phase noise region and shifts the flicker noise optimization to simulator-based design.
Concerning the $1/\Delta\omega^2$ oscillator phase noise region, although starting from many different viewpoints ranging from a pure empirical approach, over a lin-

ear approach, over a mixer-based approach, most phase noise theories clearly arrive at an expression like Eqn. (3.11):

$$\mathcal{L} = (1+F)\frac{kT}{2V_{sig}^2}\frac{R_s}{\Delta\omega^2}{\omega_c}^2 \tag{3.25}$$

which will be used for systematic VCO-design in the following text.

4

Low Power Low Phase Noise VCO Design

4.1 Introduction

The oscillator and phase noise theories presented in the previous chapter give insight to phase noise in oscillators, but regarding the dimensioning of the tank and active part, it is still not clear how to obtain optimal low power low phase noise VCOs.

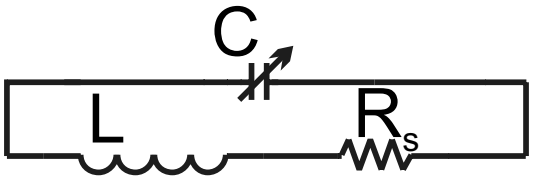

Fig. 4.1. Basic LC-resonator tank

4.2 Design for Low Power

The general LC-VCO of Fig. 1.11 is redrawn in Fig. 4.1, neglecting the capacitor losses, as the series resistance of integrated inductors largely dominates the tank losses.
Using the energy conservation theorem, the maximal energy stored in the inductor must equal the maximal energy stored in the capacitor:

$$\frac{CV_{peak}^2}{2} = \frac{LI_{peak}^2}{2} \tag{4.1}$$

with V_{peak} the peak amplitude voltage of the sinewave voltage across the capacitor and I_{peak} the peak amplitude current of the sinewave current through

the inductor. This current is flowing to the resistor R_s, so the effective loss in the tank can be calculated as:

$$P_{loss} = \frac{RI_{peak}^2}{2} = \frac{R}{2}\frac{C{V_{peak}}^2}{L} \tag{4.2}$$

or with (1.11)

$$P_{loss} = \frac{R}{2}C^2{\omega_c}^2{V_{peak}}^2 = \frac{R}{2L^2{\omega_c}^2}{V_{peak}}^2 \tag{4.3}$$

This loss must be compensated by the active part of the VCO to sustain the oscillation. P_{loss} in the above equations is the fundamental minimum for the power consumption of a LC-VCO. The equations lead to some interesting conclusions for the power consumption of any LC-VCO:
1. It is no surprise that power consumption decreases linearly for lower series resistances in the resonance tank, but these equations demonstrate that for some given unavoidable series resistance in the coil, we still have a degree of designer freedom to decrease the power consumption by increasing the tank inductance.
2. Normally the frequency of oscillation is specified. In this case Eqn. (4.3) clearly shows that power consumption decreases **quadratically** when the tank inductance is increased. The resulting guidelines for low-power VCO-design are summarized in Table 4.1, ω_c is assumed fixed.

Table 4.1. Low-power optimization summary

		Power gain	Limit
L	maximize	quadratic	chip area, tuning range, yield
$C \propto \frac{1}{L}$	minimize	quadratic	tuning range, yield
R	minimize	linear	metalization
Amplitude	minimize	quadratic	phase noise, power drain in conn. circuits

The reduction of R_S for integrated coils is strongly limited by the metalization thicknesses and eventually by skin effects. Higher inductance values come at the cost of more chip area, further limitations arise from the lower self-resonance frequency of bigger coils as it reduces VCO-tuning range and yield.

4.3 Design for Low Phase Noise

In contrast to the power consumption discussion, it is unfortunately impossible to set up a generalized black-box model for the phase noise of any LC-VCO. In chapter 3 numerous phase noise theories leading to apparently very different

design approaches were presented. After Leeson's empirical expression Q_{tank} and V_0 should be maximized. From Craninkx's and Rael's approaches R_s/V_0^2 should be minimized. These approaches were shown to be equivalent by Eqn. (3.11), although very different design approaches were applied in recent years:

- Maximize tank quality factor, i.e. maximize L/R_s [22, 30, 57, 73]
- Minimize R_s, which is mainly obtained by minimizing L_s [19, 83]

The apparent difference in both approaches, however, vanishes if the power consumption, needed to sustain the tank amplitude V_0^2, is taken into account:

$$\mathcal{L}(\Delta\omega) = 2kT(1+F)\frac{R_{eff}}{V_O^2}(\frac{\omega_c}{\Delta\omega})^2 \tag{4.4}$$

with $CV_O^2 = LI_O^2$, I_O^2 representing the tank current, transforms to:

$$\mathcal{L}(\Delta\omega) = 2kT(1+F)\frac{R_sC}{LI_O^2}(\frac{\omega_c}{\Delta\omega})^2 \tag{4.5}$$

or, with (4.2), (2.9), (1.11) and $I_{peak}^2 = 2I_O^2$ to:

$$\mathcal{L}(\Delta\omega) = 2kT(1+F)\frac{R_s^2}{L^2{\omega_c}^2P_{loss}}(\frac{\omega_c}{\Delta\omega})^2 = 2kT(1+F)\frac{1}{Q^2P_{loss}}(\frac{\omega_c}{\Delta\omega})^2 \tag{4.6}$$

A similar mathematical procedure, leading to the same result, can be applied based on the relation $V_0 = (4/\pi)R_pI_T$ ([57] or [89]). This, however, is only valid for the two referenced specific VCO topologies and only in the current limited region.
The final conclusion for the phase noise optimization is a two step design procedure. First the ${R_{eff}/V_0}^2$ equation should be used to find an upper limit for R_s. Next, for lowest phase noise at minimal power consumption $Q = \omega_cL/R_s$ must be maximized. This is summarized in Table 4.2. Obviously the

Table 4.2. Low phase noise optimization summary, ω_c fixed

		Limit
L	maximize	Chip area, tuning range
C	minimize	Tuning range
R	minimize	Metalization
Amplitude	maximize	Power consumption, reliability

same limitations for L, C, R are valid as discussed in the previous section.

Validation Against the Linear Time Variant Theory

As already stated in section 3.7, Hajimiri proposes a maximization of the tank capacitance C. However, simply stating that phase noise is minimized

by maximizing $q_{max} = CV_0$ or by maximizing V_0 is correct. No conclusion for C, however, should be drawn, as Γ_{rms} and $\overline{i_n}$ also depend on C.
This can be further clarified with Fig. 4.2. In fact, the signal swing is propor-

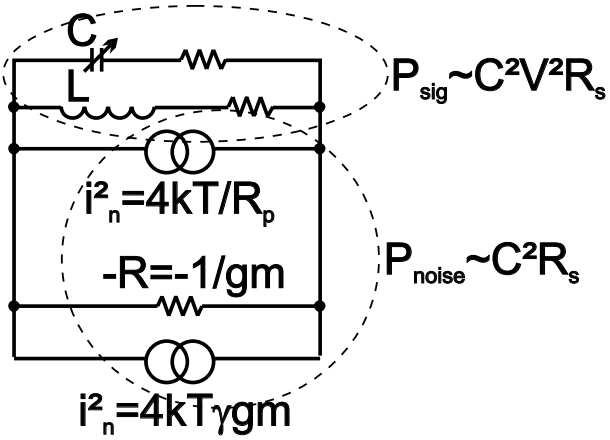

Fig. 4.2. LC-VCO signal to noise

tional to $R_s C^2 V_0^2$, but also the noise source, $4kT/R_p$ and $4kT\gamma gm$ originating from the tank equivalent parallel resistance and active part are also proportional to C^2.
This physical insight can also be provided through simple mathematics:

$$P_{sig} = \frac{V_0^2}{R_p} = \frac{V_0^2}{Q^2 R_s} \tag{4.7}$$

or with $\omega_c = 1/sqrt(LC)$

$$P_{sig} = R_s C^2 \omega_c^2 V_0^2 \tag{4.8}$$

So the signal is indeed maximized when maximizing the tank capacitance. However, having a look at the tank noise source:

$$P_{noise} = 4kT/R_p + 4kT\gamma g_m \tag{4.9}$$

Assuming $g_m = 1/R_p$ to cancel the tank losses:

$$P_{noise} = 4kT/R_p(1+\gamma) \tag{4.10}$$

which using $R_p = Q_{tank}^2 R_s$, $Q = \omega_c L/R_s$ $\omega_c = 1/sqrt(LC)$ rewrites to:

$$P_{noise} = \frac{4kT(1+\gamma)}{Q^2 R_s} = \frac{4kT(1+\gamma)R_s}{\omega_c^2 L^2} = 4kT(1+\gamma)R_s\omega_c^2 C^2 \tag{4.11}$$

So exactly as the signal swing, also noise sources are proportional to C squared. This clearly shows that a maximization of C will not lead to a better phase noise performance as the C ratios are cancelled out in the noise to carrier relation. On the contrary, assuming a constant power budget, the phase noise will deteriorate when maximizing the tank capacitance as the tank amplitude V_0 and thereby the tank signal will decrease.

4.4 Summary

The generally valid energy conservation theorem is used to derive a minimal power consumption for a given tank. The apparent disagreement between old and recent, well-known phase noise theories was shown to disappear when rewriting all theories to the tank losses. A general approach for low power low phase noise VCO is postulated, as presented in Table 4.3. The application of these guidelines from the VCO circuit level down to technology device level leads directly to power and phase noise optimized VCO-designs. The next chapter treats the detailed application of this design strategy at device level (varactor, coil). In part III of this work this is applied to specific designs aimed at commercial applications.

Table 4.3. Low power low phase noise design strategy

	Low power	**Low phase noise**
L_s/R_s	maximize	maximize
L_s/C	maximize	maximize
Amplitude	minimize	maximize

Part II

CMOS Devices for VCO Design

5

MOS Transistors

A typical cross-section of today's commonly used sub-μm CMOS technologies is presented in Fig. 5.1. On the left side, a NMOS-transistor is found, on the

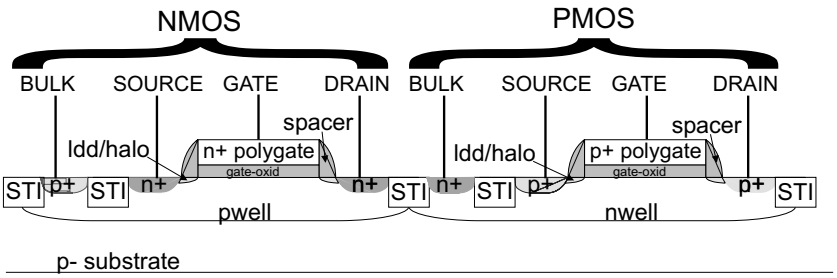

Fig. 5.1. Typical sub-μm CMOS cross-section

right side, a PMOS-transistor. For both transistors all four terminals including their back-gates (bulks) are depicted. All NMOS back-gate connections, however, are short-circuited over the substrate. Current technologies use shallow trench isolation (STI) to isolate transistors enabling a higher transistor density. All n+ and p+diffusions and polygates are salicided for a low resistance of source, drain, and gate connections. The wells, Pwell for the NMOS, Nwell for PMOS, are separately doped. Even more channel implant steps are provided to set the threshold voltage (e.g., low, regular, and high threshold voltage) according to the need towards digital high speed or digital low leakage or analog. To avoid hot electron effects, causing reliability and lifetime degeneration, a lowly doped drain extension is inserted. Further short channel device optimization is obtained through the HALO-extension.
A 0.25 μm standard CMOS transistor layout, often used in the designs of part III and optimized for RF-operation, is shown in Fig. 5.2. Instead of one single transistor with a width of 12 μm and a length of 0.25 μm, the transis-

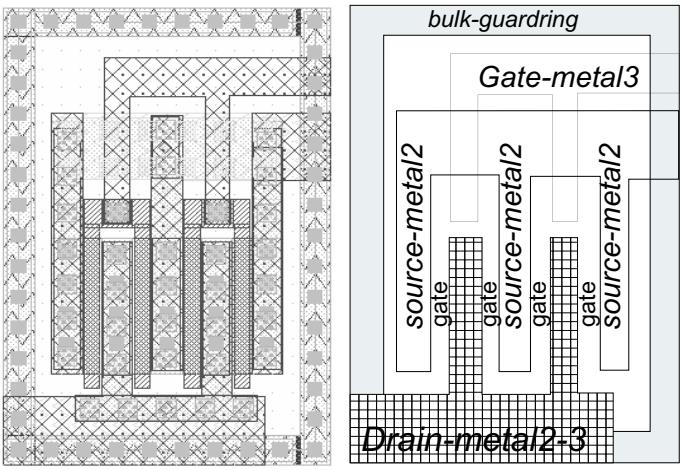

Fig. 5.2. MOS folded layout

tor consists of four parallel connected 3 μm wide transistors. This multifinger folding of the transistor reduces the drain area, and thereby its capacitance into the substrate, by a factor of two. Furthermore, the effective gate series resistance is reduced by the folding factor n squared:

$$R_{gate} = \frac{R_g/sq}{3}\frac{W}{n^2\,L} \tag{5.1}$$

with R_g/sq the sheet resistance of the gate material (for salicided polysilicon typ. 5-7 Ω/sq), and W and L transistor total width and length. The factor of three accounts for the distributed nature of the intrinsic gate [63]. For RF-simulations the subcircuit model of Fig. 5.3 is preferred over the industry-standard Berkeley BSIM [105] model. The subcircuit model is built around a MOS-transistor, modeled with a normal BSIM model, but with source and drain area set to zero. The subcircuit accurately models the external connections of the MOS-layout and is highly layout dependent. Source and drain areas are modeled through simple junction diodes with a series resistance. The series resistances to gate, source, and drain cannot be neglected at RF-frequencies, causing low-pass poles and contributing noise. They are explicitly added to the subcircuit. The model values in Fig. 5.3 were extracted from the layout and from s-parameter measurements. For physical insight and hand calculations the model is reduced to the RF small signal model shown in Fig. 5.4. The extra included elements are the channel charge resistance R_i, and external gate, drain, and source resistances R_{gate}, R_{drain} and R_{source}. The channel charging resistance models the phenomenon that the channel charge cannot instantaneously respond to changes in the gate source voltage and is proven to be $1/5\,g_m$ [104]. The small signal model subcircuit is easily extended to reflect also the noise sources of the transistor (Fig. 5.5). The external sub-

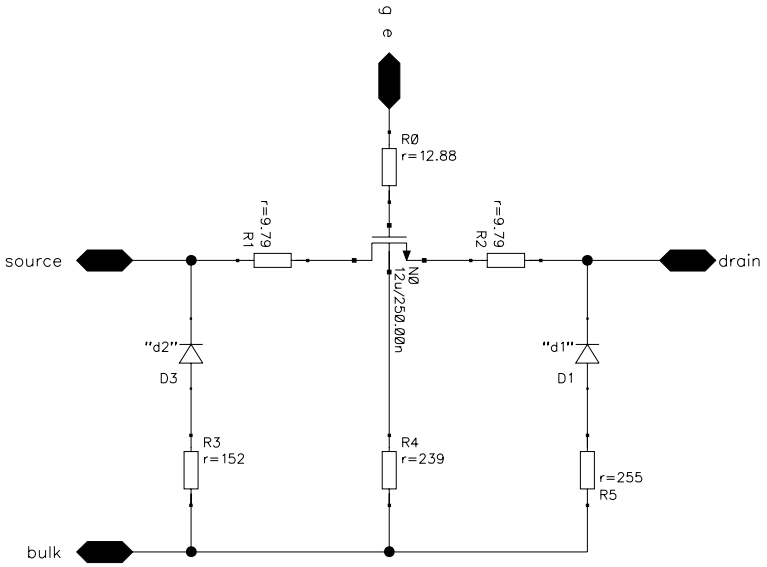

Fig. 5.3. RF-model for MOS folded layout

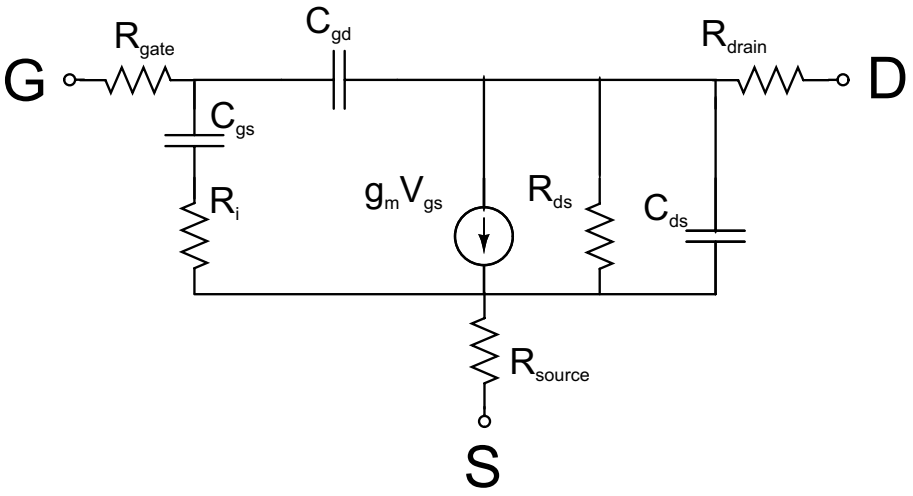

Fig. 5.4. RF small signal model of a MOSFET

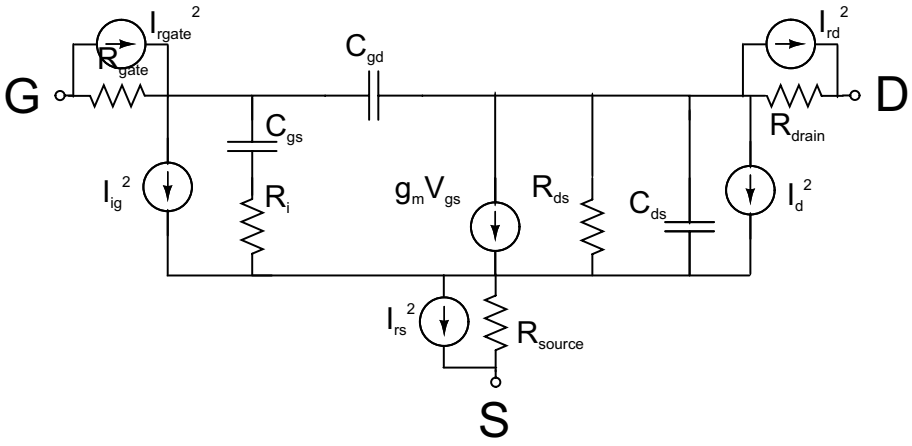

Fig. 5.5. Small signal model including the noise sources

circuit resistances obviously cause extra white noise sources, i^2_{source}, i^2_{gate}, i^2_{drain}. The drain channel noise consists of flicker noise and of thermal noise generated by the carriers in the channel. The white noise density due to the drain channel is given as:

$$i_d^2 = 4kT\gamma\, g_m \Delta f \tag{5.2}$$

where $\gamma = 2/3$ for long channel devices. In deep sub-micron processes γ might rather equal to 1.0 for relevant RF and analog operating points [91].
The induced gate noise also is originally generated in the channel standard flicker noise and coupled through the gate as a gate current. At low frequencies this gate induced noise current can be neglected. At high frequencies it must be taken account and is expressed as [104]:

$$i_{gi}^2 = 4T\delta\, g_g \Delta f \tag{5.3}$$

with $\delta = 2\gamma$ and

$$g_g = \frac{(\omega C_{GS})^2}{5 g_m} \tag{5.4}$$

Since the drain channel noise and induced gate noise arise from the same source they are correlated with a factor c [104].
Shot noise $i^2_{shot} = 2q\, I_D C \Delta f$ which is very important in bipolar devices can be fully neglected in MOS devices as the DC currents through the reverse biased junction diodes at source and drain are very close to zero.

6

Inductors

Inductors or coils can be realized in various ways. In this work external inductors or bondwire inductors are avoided for their high cost, high tolerance, and questionable manufacturability. A further very strong argument against the use of external inductors arises from CMOS ESD-protection devices, which would add huge parasitic capacitances to the VCO-nodes.

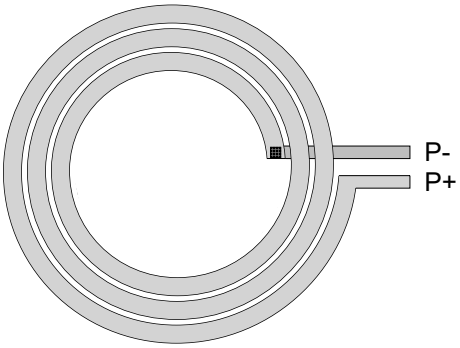

Fig. 6.1. Spiral inductor

6.1 Planar Inductors

Integrated inductors can be realized as planar inductors. Various layout structures for integrated inductors are discussed here, even more structures can be found in the relevant literature [13, 25, 64]. The planar geometrical structures are realized in integrated circuit metalization processes, either in Bipolar- or CMOS-technology. Modern IC metalization processes offer 4 to 9 metal layers which are intended for (digital) circuit wiring and can be used as inductor

design. For the conducting metal layers copper (conductivity σ=57.14 S/m) or aluminum (σ=37.7 S/m) is used. The metal layers reside on top of the substrate and are usually embedded in silicon dioxide SiO_2 (relative permittivity $\epsilon_r \approx$4). The substrate has a typical conductivity of σ=20 S/m and a relative permittivity of $\epsilon_r \approx 12$. Often two metal layers are shunt connected to reduce the series resistance using so-called VIAs or intermetallic connection layers. In older technologies VIAs are made of tungsten, more recent (starting at 0.18 μm generations) processes normally use copper. As long as VIAs consist of tungsten, it is sufficient to connect the beginning and the end of the actual turn half to the layer below and/or above. This is shown in Fig. 6.2. With

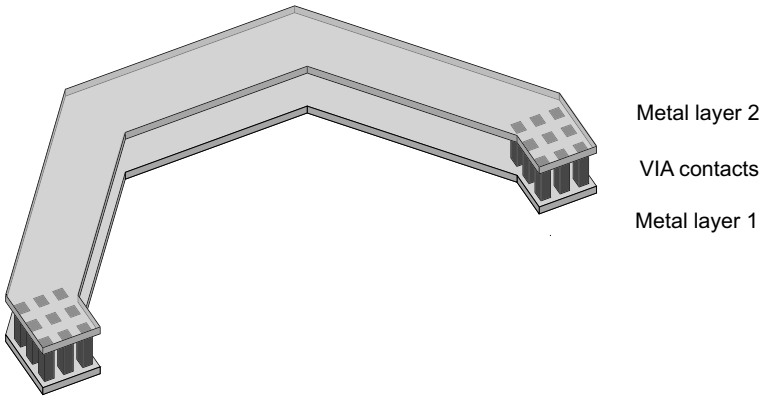

Fig. 6.2. VIA contacts

the availability of copper VIAs, Fig. 6.3 shows a better possibility to shunt connect two metal layers using VIA bars, or intermetallic stripes along the winding, thereby reducing the series resistance of the windings by 30-60%. Figure 6.1 shows an example layout for a circular integrated inductor. Practical CAD problems limit mask data preparations to allowed angles of 0, 45, or 90 degrees, so square and octagonal inductors must be used instead of circular inductors. A typical layout is presented in Fig. 6.4. An obvious asymmetry is visible from the simple planar layout and lumped model of simple spiral inductors. A nearly perfectly symmetrical layout [55] is possible using the layout and cross-section presented in Fig. 6.5. Aiming at highly integrated transceivers, the symmetrical coil layout is generally preferred for its inherently better insensitivity to substrate noise. Main disadvantage is the more complicated layout and modeling. A middle tap to the coil center is easily realized as common-mode access point or as DC biasing connection. At least two metal layers for the winding are needed for the cross area of the turns, otherwise it would be impossible to connect the turns to each other. Figure 6.5

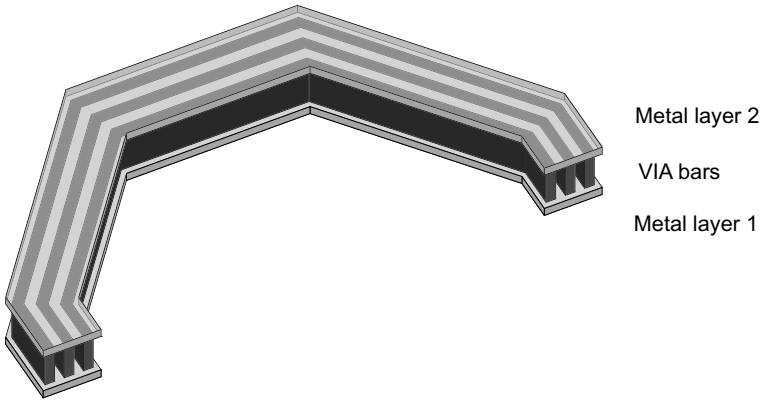

Fig. 6.3. VIA bars

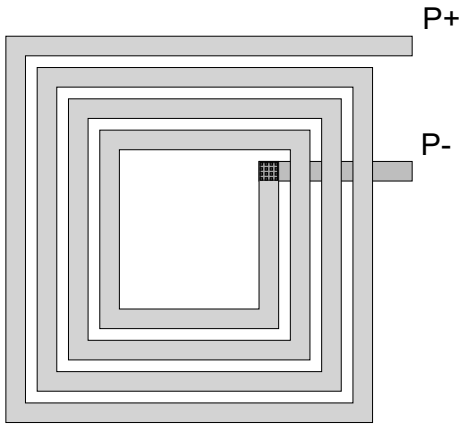

Fig. 6.4. Square-shaped spiral inductor

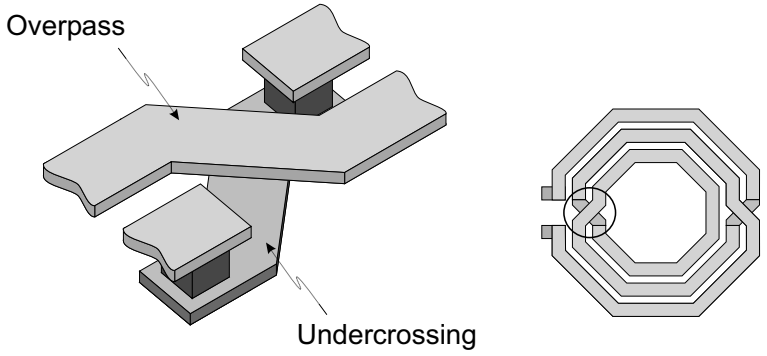

Fig. 6.5. Symmetrical inductor

shows how the crossing of the individual turns is realized via an intermetallic layer change.

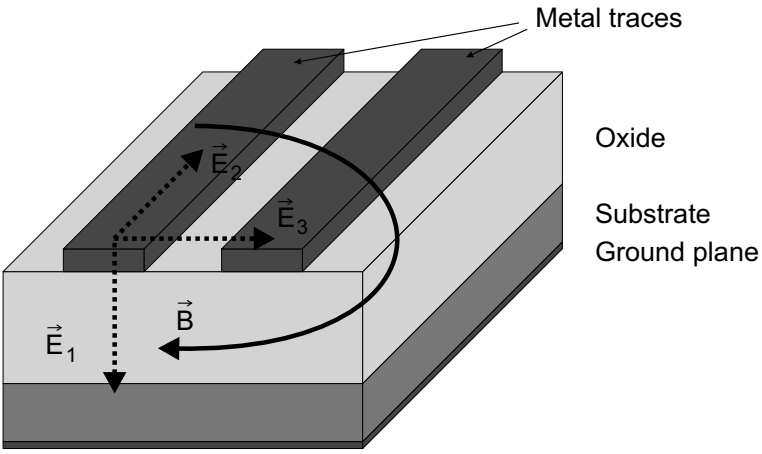

Fig. 6.6. Cross-section and electromagnetic fields

6.2 Parasitic Effects

The parasitic effects and the non-ideal behavior of the integrated inductor originate directly from the electromagnetic field building up around the metal traces. Figure 6.6 shows the cross-section of an inductor winding along with the main electromagnetic field components. The inductance, the main property of integrated inductors, is determined by the magnetic field induced by the alternating current flowing through the conducting metal layers. This magnetic field, which is characterized by the magnetic flux density $\mathbf{B}$ (see Fig. 6.6), stores the magnetic energy. A part of the overall transmitted energy is converted to heat due to the non-infinite conductivity of the metal layers and the resistive behavior of the substrate and is therefore lost. A magnetic field always delivers an orthogonal electric field which reduces the overall transmitted energy. Hence, the quality factor of the inductor is also reduced. This electric field is characterized by the electric field strengths $\mathbf{E_1}$, $\mathbf{E_2}$, and $\mathbf{E_3}$ as shown in Fig. 6.6. A voltage drop also occurs due to the electric field strengths $\mathbf{E_1}$, $\mathbf{E_2}$, and $\mathbf{E_3}$ which can be calculated along an arbitrary curve $\mathcal{C}$ for the common case as follows:

$$U(\mathcal{C}) = \int_{\mathcal{C}} \mathbf{E}\, ds \tag{6.1}$$

Skin and proximity effects occur at higher frequencies. The time-varying alternating currents flowing through the conducting metal traces produce an

electric field on their own within the conductor. This electric field counteracts the overall magnetic field of the device, as illustrated in Fig. 6.7. Due to

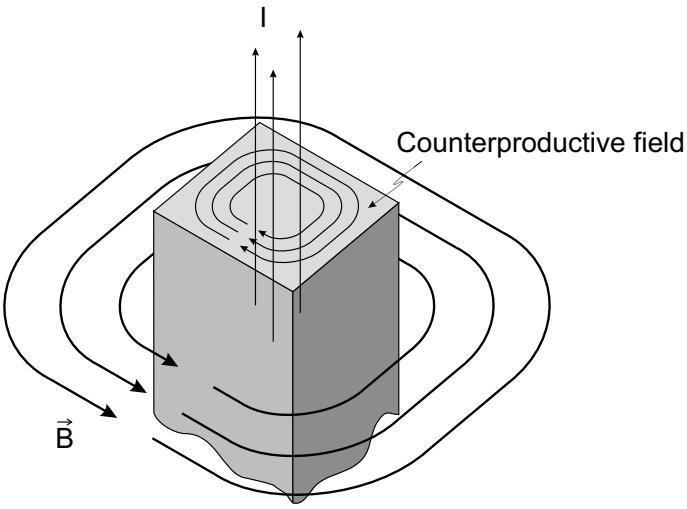

Fig. 6.7. Magnetic field inside a metal trace

this induced field within the volume of the conductor the current flowing through the winding is forced to the edge of the conducting metal traces and accumulates near the surface of the metal traces of the inductor. Hence, the overall magnetic field of the inductor can penetrate the metal traces only to a certain depth. These effects are known as *skin effect* and *current crowding*. The skin depth describes the depth of penetration:

$$\delta = \sqrt{\frac{2\rho}{\mu\omega}} \tag{6.2}$$

ρ is the resistivity [Ωm] of the material, μ [Vs/Am] is the magnetic permeability and ω [Hz] the angular frequency. Skin depth in aluminum equals to 2.6 μm at 1 GHz, 1.8 μm at 2 GHz. For copper the skin depth equals to 1.5 μm at 2GHz, 0.3 μm at 50 GHz. These skin depths are well above the thickness of typical metallizations in standard digital CMOS, so skin effect is completely negligible for the designs presented in Part III of this work.
For multiple conductors, the magnetic field of one conductor penetrates the neighboring conductors and thus also changes the current distribution. This is known as proximity effect. The substrate of an IC process is a major source of losses. We can distinguish between two different main loss mechanisms. First, displacement currents are induced because electric energy is coupled to the substrate via capacitive coupling mechanisms. This is further shown in Fig. 6.8. Second, the time-varying magnetic field of the device penetrates

the substrate and also produces time-varying electromagnetic fields within the substrate which induce substrate currents (also known as Eddy currents) . This is illustrated in Fig. 6.9. All effects mentioned above contribute to the

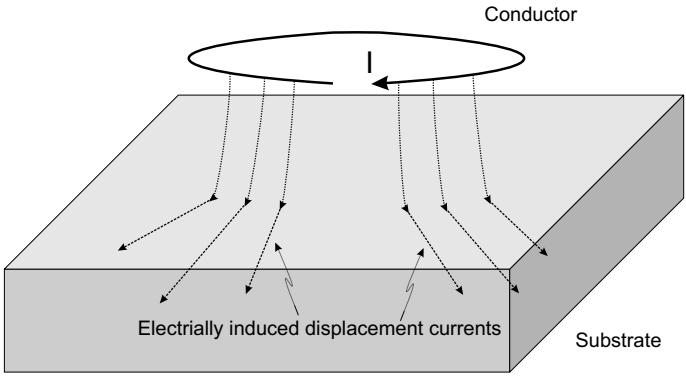

Fig. 6.8. Substrate losses due to capacitive coupling

non-ideal behavior of integrated inductors and so handling these parasitic elements is important for efficient inductor and circuit design. To counteract these problems, many IC processes provide a thick top metal layer for inductor design. Furthermore, this metal layer may reside on top of a thick insulator to minimize the resulting capacitance to the layers and substrate below. In standard CMOS, unfortunately the metal layers are rather thin, but due to the ever increasing digital wiring complexity, the number over metal layers is increasing steadily.

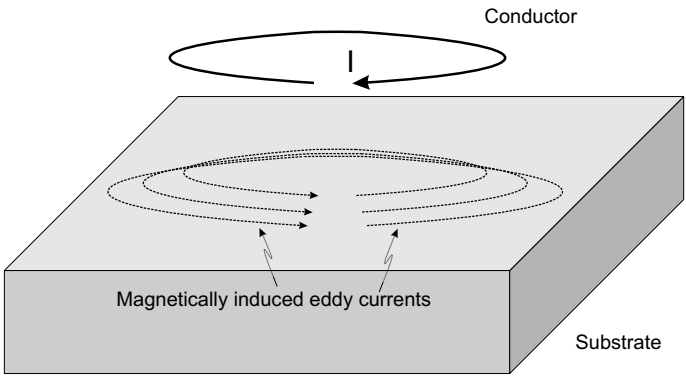

Fig. 6.9. Substrate losses due to induced electric fields

6.3 Modeling

The aim of a lumped lower order model is to characterize the integrated inductor with a minimum number of discrete components. A detailed derivation of the lumped low order model for inductors can be found in [93]. Here, only a brief insight into the modeling process is provided. Figure 6.10 shows the cross-section of an integrated inductor together with discrete elements used to model the various parasitic components. Below follows a short explanation

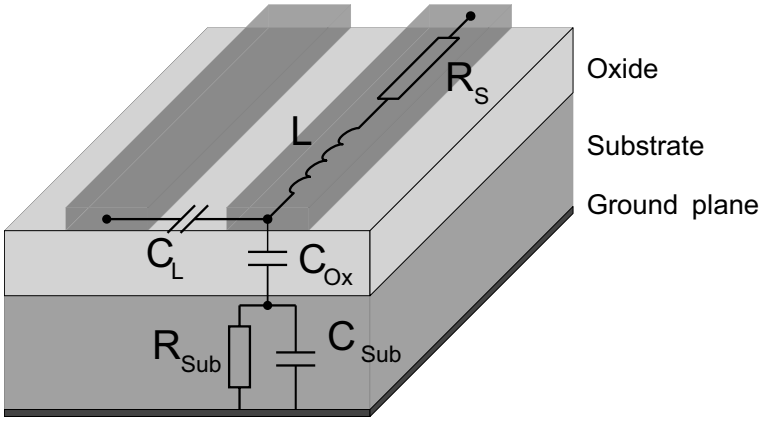

Fig. 6.10. Inductor cross-section and parasitic components

of the various components found in the lumped low order model:

- L: The inductance is caused by the magnetic flux density $\mathbf{B}$ of the electromagnetic field.
- R_{sub}: The resistance R_{sub} is used to model the ohmic losses in the substrate.
- R_s: The series resistance R_s characterizes series resistance of the metal traces with finite conductivity, as well as the previously mentioned skin effect and current crowding. For all inductors in this work, the metal series resistance is dominant due to the thin metal layers in standard CMOS and R_s equals to the DC series resistance, neglecting skin effects and current crowding.
- C_L: The capacitive coupling between the turns of the inductor is modeled with the lateral coupling capacitance C_L.
- C_{ox}: C_{ox} models the area capacitance between the inductor and substrate.
- C_{sub}: The capacitance C_{sub} is used to characterize the capacitance in the substrate. Due to the highly conductive substrates as typically used in standard CMOS processes (1 to 6 Ωcm), it can be neglected in this work.

It is important to note that the complete inductor is modeled with these components and hence a minimum number of discrete elements is used in the

modeling process. The resulting electrical circuit is now easily obtained. The use of a Π-circuit is appropriate since the inductor is a two-port device. The series branch of the Π-circuit corresponds to the winding of the inductor, so the inductance L and series resistance R_s are placed here as well as the lateral coupling capacitance C_L. Since we assume static parasitic components, the resistances and capacitances to the substrate can be split into two equal parts to complete the equivalent electrical circuit. The values are divided as follows:

$$C_{ox1} = C_{ox2} = \frac{C_{ox}}{2} \tag{6.3}$$

$$R_{sub1} = R_{sub2} = 2\ R_{sub} \tag{6.4}$$

$$C_{sub1} = C_{sub2} = \frac{C_{sub}}{2} \tag{6.5}$$

Figure 6.11 shows the resulting electrical circuit. In [29, 46, 69, 93] detailed

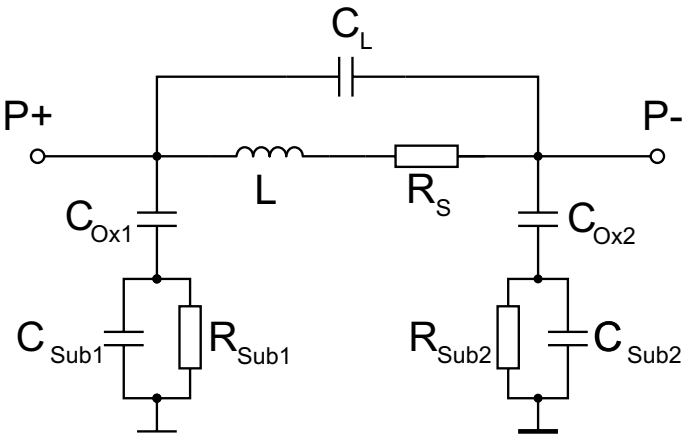

Fig. 6.11. Low-order equivalent circuit

methods and algorithms for the calculation of these lumped components can be found. For simple spiral coils C_L normally can be neglected as the voltage difference between neighboring windings is small. For symmetrical inductors (Fig. 6.5) the single Π lumped model must be extended to the double Π model as presented in Fig. 6.12. The double Π-model allows an accurate modeling of the coil, as well as in balanced mode as in single-ended operation mode. For instance, in balanced mode the capacitor at the middle node completely disappears, causing a totally different self-resonance frequency. The meaning of the model parameters is the same as for the single-pi model, only a form factor f was introduced to fit the substrate-capacitor C_{ox} according to the

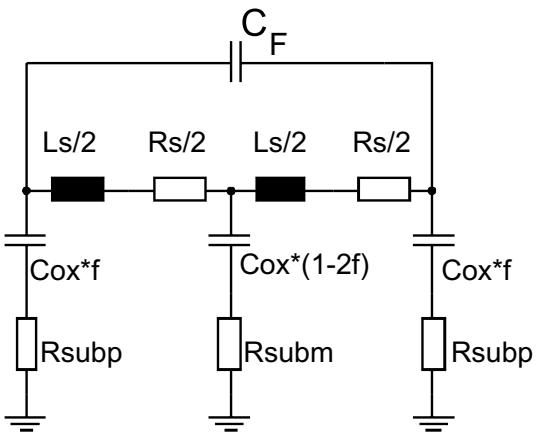

Fig. 6.12. Differential inductor lumped model

winding staggering (see next section). For coils without winding staggering $f = 0.25$. In contrast to simple spiral coils, the lateral winding to winding capacitance C_L cannot be neglected at all as the voltage difference between neighboring windings is maximal due to the differential winding scheme. The lumped models for the integrated inductors can be extracted out of measured s-parameters. This enables highly accurate models at the cost of a large testchip area and testchip time delay, which normally is provided for a limited number of inductors, provided to designers through a library including layout and model.

For insight or first-order modeling of simple planar inductors (Fig. 6.4) analytic or fitted formulas for hand calculations can be used. For instance, for a planar inductor without winding staggering the inductance value L is approximately given by [101]:

$$L = \frac{\mu_0}{2\pi} l(ln(\frac{l}{n(w+t)} + 0.2)) \tag{6.6}$$

with total length l:

$$l = (4n+1)r + (4N+1)N(w+s) \tag{6.7}$$

winding width w, winding count n, $N = integer(n)$, winding spacing s , and the thickness t of the metal. Due to the magnetic coupling from winding to winding, the inductance increases nearly quadratic with the number of turns, or equivalently inductors with many turns feature a high inductance to area ratio.

Alternatively, commercial 3D electromagnetic simulators like, e.g., HFSS [2] or Agilent MOMENTUM [1] can be used to estimate the models. These simulators unfortunately require very long simulation times of many hours and

their accuracy is not yet good enough to avoid the expensive testchip verifications. Furthermore, run-times are too long to optimize the coils. For a fast and acceptable model estimation the public domain M.I.T. simulators FASTHENRY [80] and FASTCAP [79] can be combined to provide the magnetical and electrical parts of the lumped model. This approach is described in more detail in [29]. The speed of the approach allows a qualitative optimization of integrated inductors, which is illustrated by the design presented in chapter 11.

6.4 Optimized VCO-Inductors

The design goals of Table 4.3 can be recapitulated for inductors as 1) maximize L/C the ratio of inductance to parasitic capacitance, and 2) maximize L/R, the ratio of inductance to resistance. The insight into integrated coil design of the previous sections leads to the use of the following options to overcome the traditional low Q of the integrated coils and to build highly optimized coil layouts:

- high winding count
  With n, the number of turns in a coil, the coil inductance $L \propto n^2$ and the coil series resistance $R_s \propto n$, so a higher n will improve the R/L ratio (or Q_L) by n. An upper boundary for n, comes from the fact that also the winding to winding capacitance increases with n.
- differential coil
  The use of one differential coil, instead of two single coils, exploits the coupling factor to increase the inductance per area, leading to a higher L/C ratio. As the differential coil is used in a balanced configuration, the middle capacitance of the lumped model (Fig. 6.12) is cancelled out. This very effectively increases the differential self-resonance frequency and extends the differential Q to higher frequencies.
- special coil layout
  The differential coil is further optimized through a special staggered winding coil layout as shown in Fig. 6.13. The middle tap of the coil is the outer winding in the layout, it is laid out wider to reduce the ohmic resistance of these winding, without any capacitive penalty as its capacitance is at common mode. This increases L/R largely as the outer winding is the longest one. The inner windings are thinner, this decreases the capacitive load at the RF-nodes of the oscillator increasing L/C and the differential self-resonance frequency. One more benefit of thinner inner windings is due to the crowding effects as the magnetic field is maximal in the middle of the coil. So, wider inner windings would not decrease the series resistance. To exploit the capacitive benefits of the winding staggering, coil ports must be fed to the inner windings and the winding width should increase from the inner winding to the outer winding. This is mainly due to the simple

fact that the inner winding is the shortest winding, with the smallest area capacitor into the substrate.

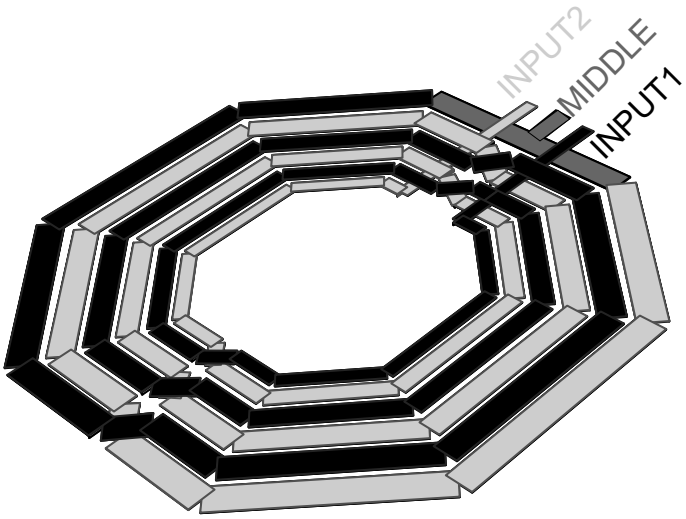

Fig. 6.13. Staggered coil layout

6.5 Inductor Scaling and Reuse

The optimized complex inductor layouts with staggered winding widths (and spacings) as presented in previous sections (example in Fig. 6.14) can accurately be modeled using a double π-model (Fig. 6.12). For first-pass single-testchip VCO-designs the models should be extracted out of hardware-based measurements, or much less accurate out of day-consuming 3D-simulations. One approach is to characterize an inductor library at an early developing stage of the technology development. An inductor library, however, is never complete and causes high testchip-, design-flow, and CAD-costs, as well as time-consuming and inflexible VCO-designs. To avoid this, a physical scaling procedure is proposed in this work to enable more flexible coil design and coil design reuse. The scaling procedure is summarized in Table 6.1 and consists of scaling rules for the layout and for the lumped model. The layout scaling consists of a simple linear geometrical size scaling in X and Y dimensions with an identical scaling factor s, which easily can be programmed in today's widely used design and layout frameworks. The scaling of the lumped model is based on the physical meaning of the lumped model parameters. The total inductance L_s of the coil scales in first order linearly with its radius, as known from magnetic field basics and confirmed by FASTHENRY simulations [80].

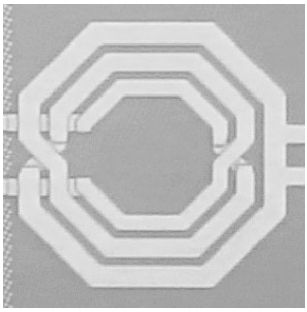

Fig. 6.14. Staggered coil layout

Table 6.1. Layout and lumped model parameter scaling algorithm

Layout	Lumped model parameter
	$L_s \rhd L_s.s$
$x \rhd x.s$	$R_s \rhd R_s$
$y \rhd y.s$	$C_f \rhd C_f$
	$C_{ox} \rhd C_{ox}.s^2$
	$f \rhd f$
	$R_{sub} \rhd R_{sub}.s^{1\cdots2}$

The series resistance R_s of the coil is caused by the series resistance of the windings. Scaling all geometries by s, increases width and length of the windings, so R_s remains constant. The coupling capacitance C_f is mainly caused by the winding to winding capacitance, due to the differential layout causing high voltage differences between neighboring windings. Scaling all geometries by s, increases the distance between the capacitor plates by s and increases the length of the capacitor plates by s, leading to C_f remaining constant. The total parasitic capacitance of the coil into the substrate C_{ox} is basically an area capacitor and scales quadratically with s when scaling all geometries with s. The distribution of C_{ox} over the three nodes of the model depends on the winding width staggering and is modeled by the form factor f, it does not depend on the geometrical size of the inductor or on s, so also f remains constant. The substrate series resistances R_{subm} and R_{subp} scale less easy. The values scale inversely proportional with the area (s^2) of C_{ox} into the substrate, but linearly (s^1)with the distance to the next substrate contact. At first order, its dependence on s can be modeled with $s^{1.5}$, if more measured coils are available, R_{sub} can be calculated from a second-order polynomial fitted to the measured values. Inductor testchips consisting of 4 and 6 windings differential coils with inductances from 2.6 nH to 13 nH verify the introduced scaling procedure. Figure 6.15 shows the chip photograph of the 0.25 μm standard CMOS coil testchip with 4 metal layers. The coil set documenting the scaling is listed in Table 6.2. The coil windings consist of a parallel connection of Metal 2, 3

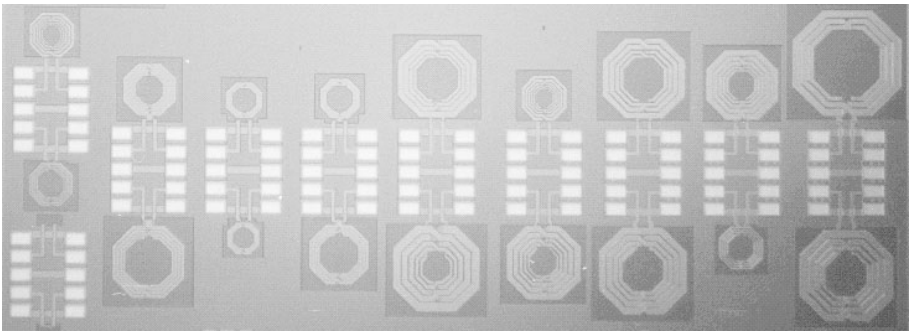

Fig. 6.15. Coil scaling testchip photograph

and 4 to decrease the series resistance. The staggered winding widths further decrease the series resistance, while conserving the differential self-resonance frequency. A comparison between measured and predicted model parameters for the 6 windings layouts is shown in Fig. 6.16,6.17,6.20,6.18,6.19,6.21. A very good fit between predicted and extracted values is obtained. The deviation for the smallest coil series resistance is due to increased via resistances at the winding crossings. Figure 6.20 furthermore reveals the limitation of the coil down-scaling. Whereas L_s scales down linearly, C_f remains constant which leads, for small s, to a coil which is self-resonance limited by the combination of L_s and C_f. Obviously, coil geometry up-scaling should be preferred over down-scaling.
The scaling procedure proposed here is very helpful at any VCO design. New designs benefit from the insight into coils. Regarding the VCO-optimization for low power and low phase noise presented in chapter 4, the scaling procedure enables a coil optimization for minimal R_s to minimize the phase noise followed by a scaling to high L at constant R_s for minimal power consumption.

Table 6.2. Extracted coil data from s-parameters

	ind4	**ind6**	**ind9**	**ind13**
$L_s[nH]$	4.2	6.2	9.6	12.9
$R_s[\Omega]$	16.7	13.8	10.7	11.3
$C_f[fF]$	16.7	13.8	10.7	11.3
$C_{ox}[fF]$	292	564	1370	2138
f	0.21	0.23	0.21	0.22
$R_{subm}[\Omega]$	144	103	82	55
$R_{subp}[\Omega]$	48	18	19	16
s	0.47	0.67	1.0	1.37
inner radius [μm]	34	49	73	100

Of course, the scaling procedure also can be applied to redesign previous VCO-designs to new applications (e.g., 51 GHz VCO to 17 GHz and 11 GHz) [76]) or to re-center a known VCO for optimal yield. Another benefit of the physical scaling is that coils with different inductance values can be compared.

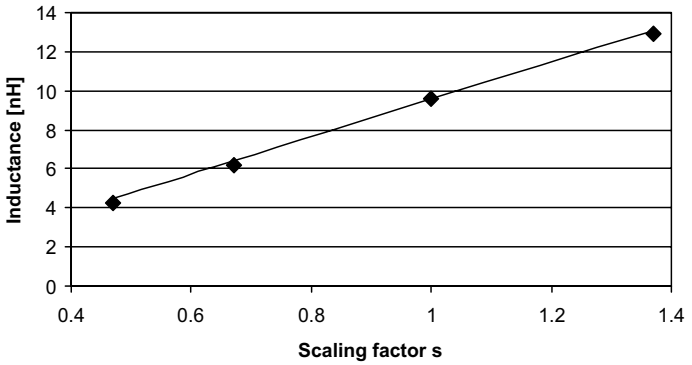

Fig. 6.16. Scaling of series inductance L_s

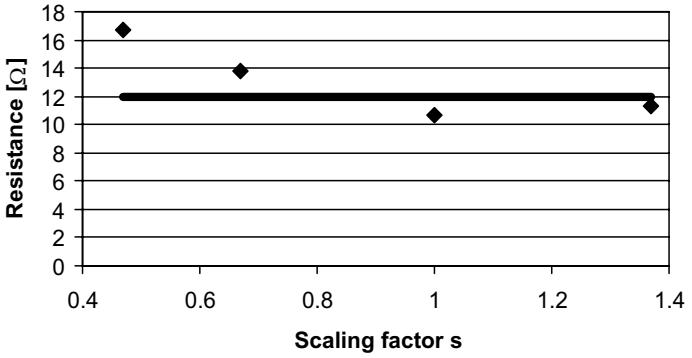

Fig. 6.17. Scaling of series resistance R_s

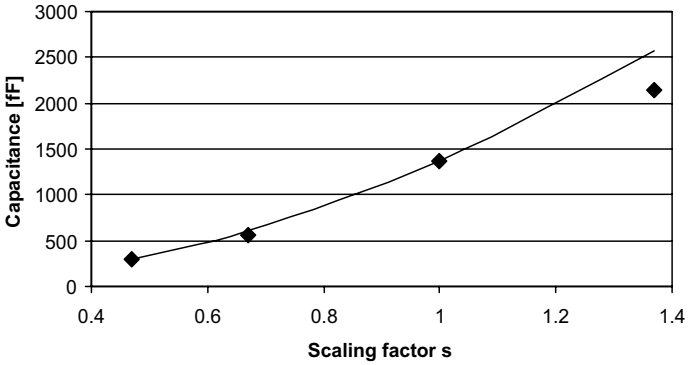

Fig. 6.18. Scaling of lumped substrate capacitance C_{ox}

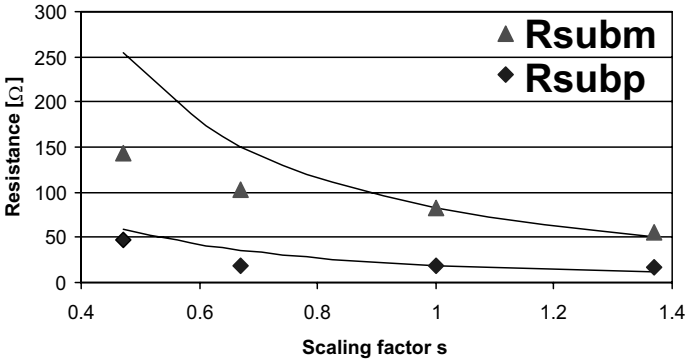

Fig. 6.19. Scaling of lumped substrate resistances R_{sub}

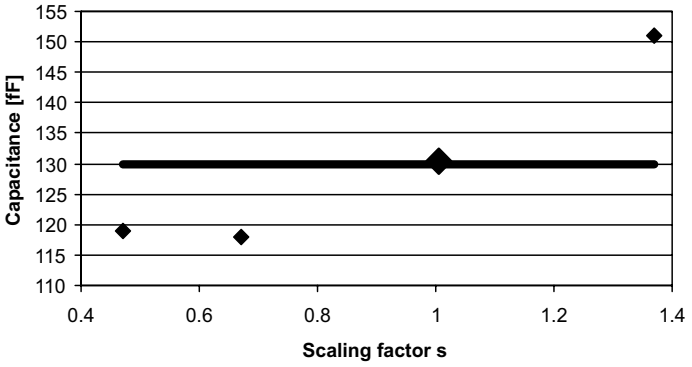

Fig. 6.20. Scaling of lumped couple capacitance C_f

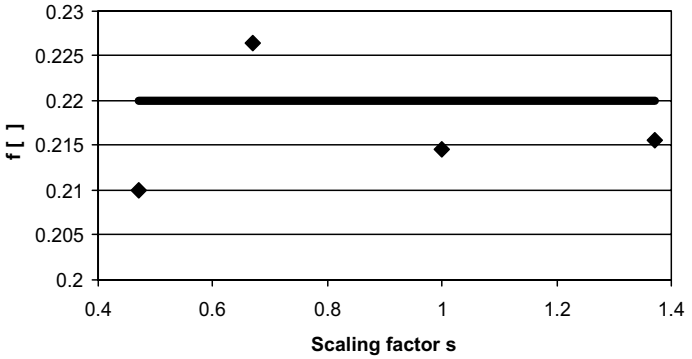

Fig. 6.21. Scaling of form factor f

7

Capacitors

7.1 Linear Capacitors

Considering highly integrated transceivers in CMOS linear capacitors are mainly needed in baseband filters and in RF building blocks as AC-coupling capacitors. A capacitor combined with a MOS-switch furthermore can be used to band switch frequencies of VCOs [12] or LNAs [43]. Most CMOS-processes

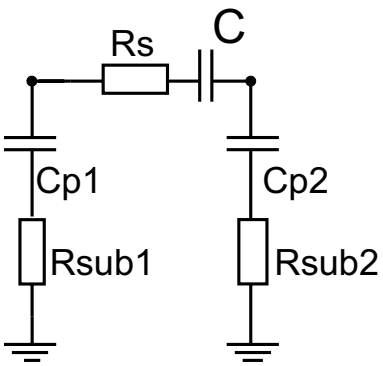

Fig. 7.1. RF-capacitor lumped model

offer, at the cost of extra masks and lower yield, nice linear capacitors in form of a poly-to-poly capacitor (PIP) or in the form of a metal-insulator-metal capacitor (MIM). Alternatively, linear capacitors can be realized with the standard metal layers available. Realizations (Fig. 7.2) exploit the area-capacitance between two or more metal layers or the fringing capacitance or a combination of both [90]. Fractal capacitor layouts [44] furthermore can be used to increase the fringing effect. Linear RF-capacitors generally can be modeled with the lumped model presented in Fig. 7.1. Of main importance

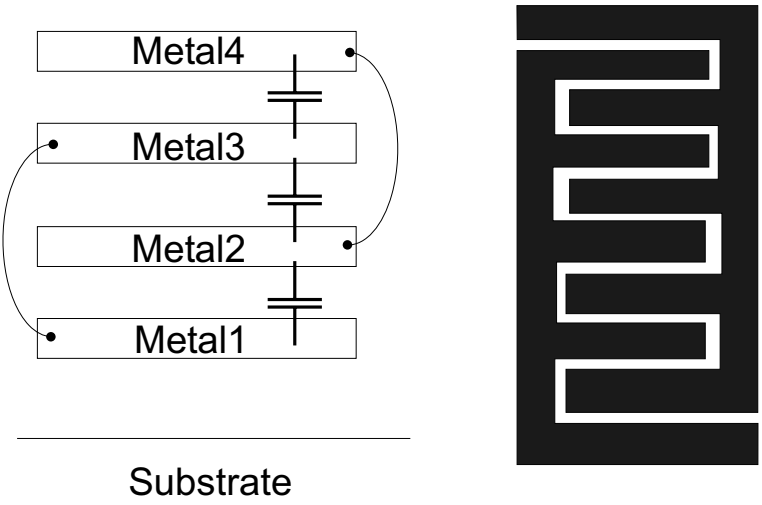

Fig. 7.2. Standard metalization linear capacitors,*left*: area capacitor cross-section,*right*: fringing cap top view

for use as RF-capacitors is the quality factor $Q_C = 1/(j\omega R_S C)$ and the ratio of the wanted capacitance to the parasitic capacitance C/C_p. This ratio is usually best for MIM-caps situated in the top metal layers (few %). Standard metal layer-based capacitors feature worse values for C/C_p of 10% to 20%.

7.2 Junction Diodes

A trivial implementation of a variable capacitor or varactor is any junction diode. In contrast to many BiCMOS technologies, in standard CMOS no separate implant is provided to realize an optimized varactor diode. Only parasitic junction diodes can be used as varactors: NMOS source/drain junctions and PMOS source/drain junctions. Also the well to substrate diode could be used, but it is not presented here due to its low tuning range and quality factor. Measured C-V characteristics and quality factors for INFINEON Technologies AG 0.25 μm standard CMOS process are shown in Figs. 7.3 and 7.5. C and Q_{var} were extracted out of deembedded S-parameters by:

$$C = -(2\pi f Im(\frac{1}{Y_{11}}))^{-1} Q_{var} = -\frac{Im(\frac{1}{Y_{11}})}{Re(\frac{1}{Y_{11}})} \tag{7.1}$$

The quality factor is mainly due to the ohmic resistance of the contacts to the diffusion regions. A Q-optimized layout, presented in Fig 7.4, was used for both diode types. The measured quality factors are more than sufficient for

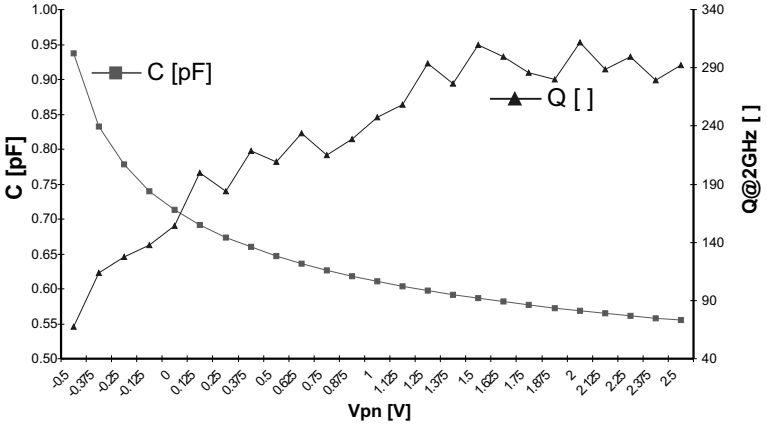

Fig. 7.3. Measured p+/nwell junction diode characteristics

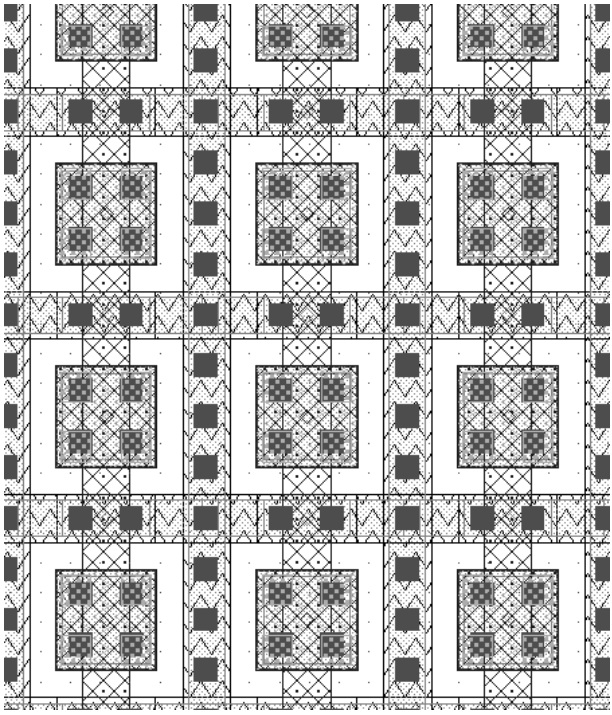

Fig. 7.4. Q-optimized junction diode layout

VCO designs in commercial application bands. The ratio of maximal to minimal capacitance is important to tune VCO-frequency. Both junction diodes unfortunately feature a small C_{max}/C_{min} over the -0.5 to 2.5 V measured voltage range, which is even smaller when limiting the tuning voltage from 0V to 2.5 V nominal supply voltage. This ratio further deteriorates from technology generation to technology generation with decreasing power supply voltages. The p+ to nwell junction diode normally is preferred over the device in the p-substrate as it is less sensitive to substrate noise.

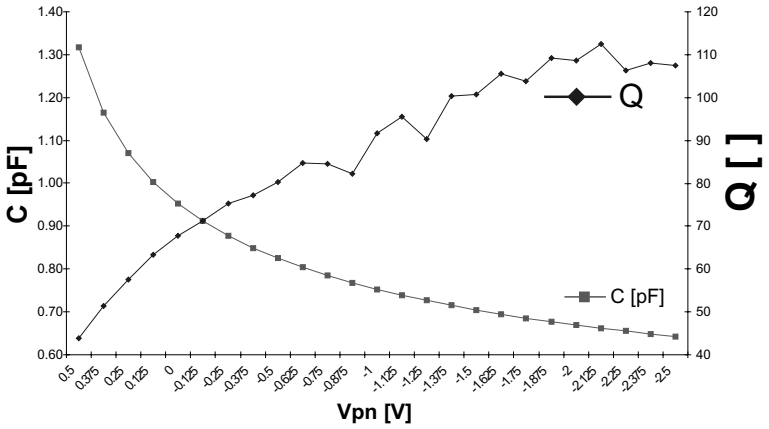

Fig. 7.5. Measured n+/psub junction diode characteristics

7.3 MOS-Varactors

MOS varactors are variable, voltage-controlled capacitors based on the MOS structure. The use of a MOS device as varactor is not new [87] and well known [17].

7.3.1 Principle of Inversion Mode Varactors

Figure 7.6 shows a cross-section of a NMOS varactor and the small-signal model generally assumed for varactors: a variable capacitance in series with a variable resistance. For the NMOS device, source and drain are n^+-doped. The substrate (or well) region between and around source and drain is of opposite doping, i.e., p^--type. Process determined the polysilicon gate is of the same doping as source and drain, i.e., n^+-type. A PMOS device is obtained when all regions have opposite doping as in the NMOS. The MOS varactor is not a four-terminal device as the transistor but a three-terminal device. The

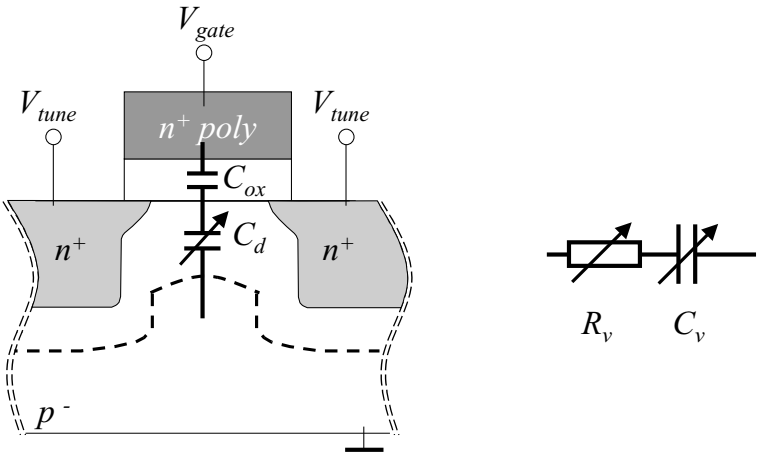

Fig. 7.6. Cross-section of a conventional NMOS varactor (in depletion; left) and the generally assumed model (right). The dashed line indicates the border of the depletion region.

source and drain regions are shorted to apply the voltage V_{tune} that tunes the variable capacitance. The p^- body is grounded and the voltage V_{gate} is applied to the gate node. The variable capacitance C_v appears between the gate node and all other nodes at AC ground. Essentially it is the series connection of the gate oxide capacitance C_{ox} and the variable depletion region capacitance C_d

$$\frac{1}{C_v} = \frac{1}{C_{ox}} + \frac{1}{C_d}. \tag{7.2}$$

Figure 7.7 depicts the small-signal capacitance of a NMOS varactor at zero tuning voltage. The corresponding charges and the relevant lumped elements in the device are included also.

Negative gate voltages result in a hole surplus at the surface of the semiconductor; the device is in accumulation. Charge variations at the gate are balanced by changes in the accumulation layer charge. A large capacitance determined by the gate oxide is effective.

At increasing gate voltage the flat-band situation is reached. The semiconductor beneath the gate is neutral and fixed oxide and interface charges balance the gate charge. The flat-band voltage V_{FB} is usually negative as especially the oxide charges are comprised of positively charged alkali-ions unintentionally introduced during processing. Further, for the value of V_{FB} the different work functions of the gate and the well have to be considered. If gate and well are of the same type of doping flat-band occurs close to 0 V. Different doping shifts V_{FB} by ca. 1 V.

Just above the flat-band voltage holes are repelled from the surface and the negatively charged ions of the fixed dopand atoms (acceptors) form a deple-

tion region. Changes in the gate charge are balanced by more or less negative dopands, i.e., by a wider or shallower depletion region. The capacitance in this situation is a series connection of the gate oxide capacitance C_{ox} and the variable depletion region capacitance C_d.

Gate voltages above a certain threshold V_{th} result in a surplus of electrons

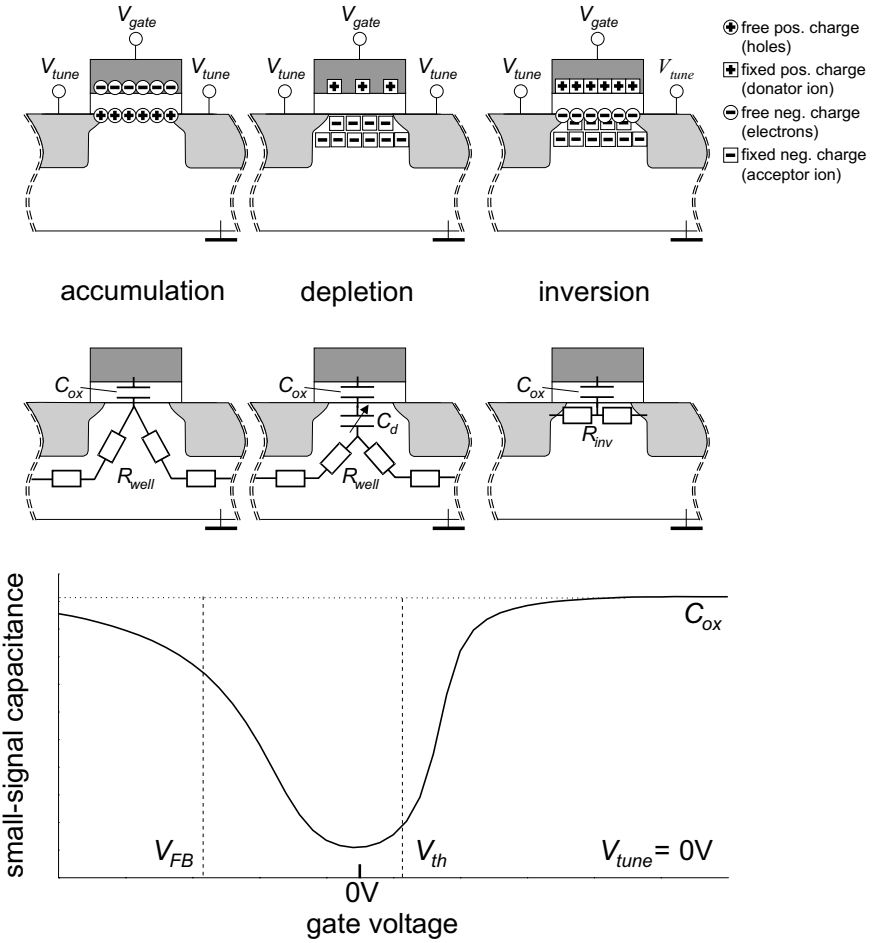

Fig. 7.7. Typical measured small-signal capacitance characteristic of a NMOS varactor *bottom*, the corresponding charges *top* and the relevant lumped elements *middle* at zero tuning voltage. Oxide, interface charges and charges at *pn* junctions are not shown

at the semiconductor surface; the device is in inversion. In this situation the depth of the depletion region remains constant and changes in the gate charge are balanced by changes in the electron inversion layer. Again the effective ca-

pacitance is determined by the gate oxide capacitance. The necessary electrons can be provided by thermal generation in the depletion region. However, at the voltages leading to inversion the electric field between the gate and the source/drain lowers the barrier between the source/drain and the semiconductor's surface considerably. Therefore, the main source of electrons are the n^+-doped source and drain regions.

Part of the resistance is always the gate resistance determined by the polysilicon line. The gate area and thus the gate width have to be large to achieve the necessary capacitance values (≈500 fF...2 pF) for VCOs in wireless communication systems. With a regular straight transistor design the corresponding gate resistance

$$R_{gate} \propto N_{\square} R_{\square} \tag{7.3}$$

is large. $N_{\square}$ and $R_{\square}$ are the number of squares and the square resistance of the gate, respectively. To avoid this large, undesired resistance RF transistors as well as varactors are laid out in so called multifinger structures (Fig. 7.8). Many short fingers (often less than 10μm) connected in parallel resemble a

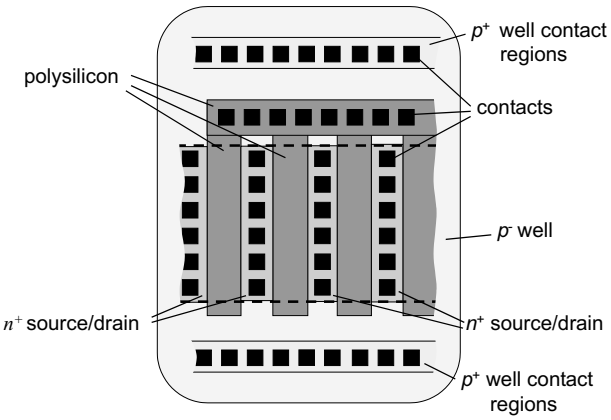

Fig. 7.8. Typical multifinger structure of RF varactors. *Dashed line* indicates area of thin oxide

device with large total gate width

$$w_g = l_f N_F \tag{7.4}$$

with N_F the number of parallel fingers and l_f the length of each finger. Thereby the gate resistance is considerably reduced to

$$R_{gate} \propto \frac{F_{\square} R_{\square}}{N_F} \tag{7.5}$$

with $F_{\square}$ the number of squares per finger. A typical value for R_{gate} is around 300 mΩ for a 600 μm wide device (at 0.25 μm gate length). Further reduction

of the gate resistance by a factor of $\frac{1}{4}$ is achieved when contacting the gate fingers at both ends.
The typical behavior of the total resistance of a NMOS varactor is shown in Fig. 7.9. In accumulation the gate resistance is in series to the resistance from

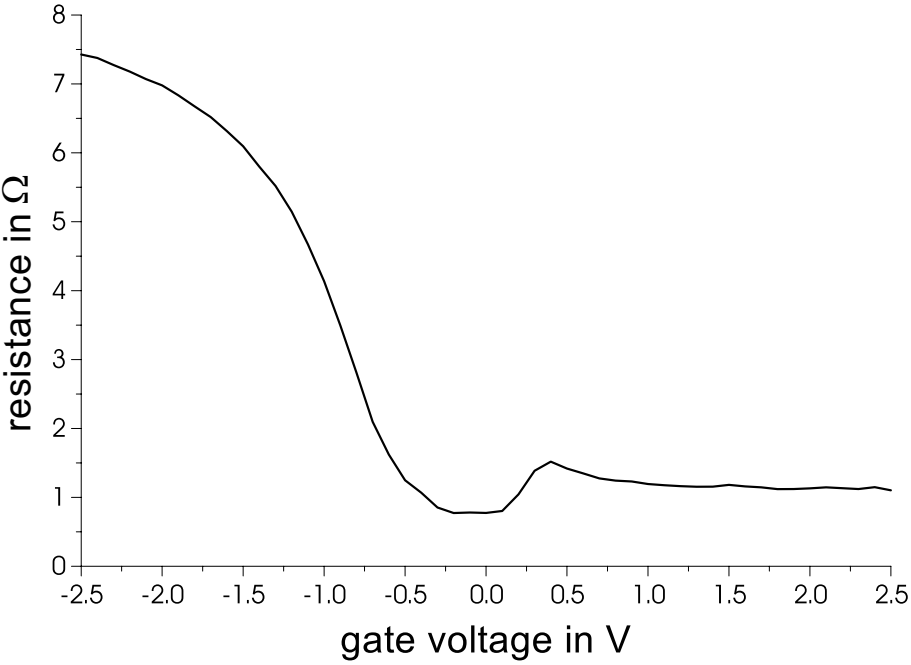

Fig. 7.9. Typical measured small-signal resistance characteristic of a NMOS varactor

the accumulation layer to substrate (well) contacts outside the device, see Fig. 7.8. This resistance is strongly layout dependent.
In depletion the resistance is usually lower than in accumulation, as the resistive path, now from the border of the depletion region to the substrate (well) contacts, is shorter. Above V_{th} the resistance is determined by the inversion layer. Thus, a peak in the resistance is observed at the onset of inversion, as the semiconductor surface is only weakly inverted with few electrons. At higher gate voltages and strong inversion the resistance drops to a relatively low value. The resistance in inversion is proportional to the gate length of the varactor.
The transition from depletion to inversion is determined by the voltage difference between gate and source/drain and the threshold voltage. Therefore, the transition voltage will be increased with increasing tuning voltage (Fig. 7.10). The threshold voltage depends on the voltage between source/drain and

substrate (bulk effect) and contributes additionally to the shift of the transition. Accumulation occurs only for gate voltages more negative than the bulk

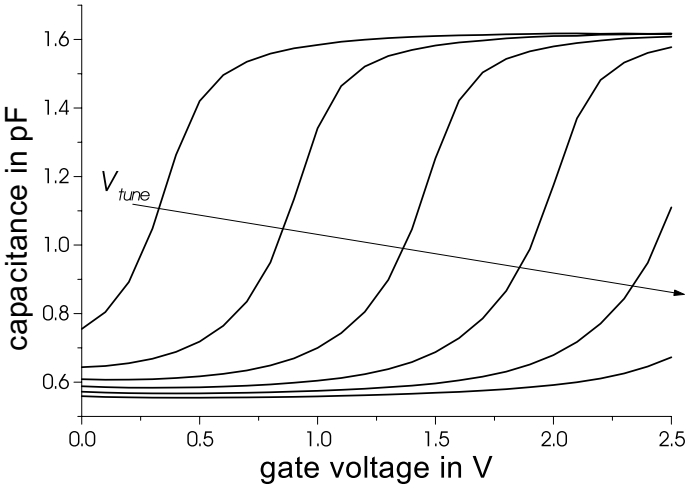

Fig. 7.10. Typical measured small-signal capacitance characteristic of a conventional NMOS varactor at various tuning voltages (0 V...2.5 V; 0.5 V steps)

(substrate) voltage. However independently of the tuning voltage the well is always at 0 V and the transition to accumulation remains at fixed voltage (<0 V) despite increasing tuning voltage. The device remains in depletion, the maximum depth of the depletion region is increased and the total capacitance slightly decreased (deep depletion).
Devices in practical circuits are operated in the positive voltage range. As NMOS and also PMOS varactors are then between depletion and inversion they are called inversion mode (I-mode) varactors. Their maximum capacitance appears in inversion, the maximum resistance at the onset of inversion.

7.3.2 Accumulation Mode Varactors

Devices that are in depletion or accumulation in the positive voltage range are called accumulation mode (A-mode) varactors. Figure 7.11 shows a cross-section of an A-mode varactor in n^- well and the small-signal capacitance characteristic. The device is derived from a PMOS varactor[1], in which the p^+ source/drain regions are replaced by n^+-well contacts. Thus, the potential of the complete well is tuned.
Due to the close similarities with a NMOS structure, the A-mode in n^- well

[1] classification by the carrier type in the inversion layer; here holes

is often called "NFET in Nwell". The flat-band voltage is close to 0 V, as gate and well are of the same doping type. First the behavior at zero tuning voltage is considered. At zero gate voltage the device is already at the onset of accumulation. A small increase of V_{gate} drives the varactor entirely into "strong accumulation". The capacitance shows a high value determined by the gate oxide. The resistance is given by the accumulation layer and the parallel well resistance, in addition to the gate resistance.
An increase in tuning voltage shifts the transition voltage (depletion to accumulation) to higher gate voltages. Contrary to the I-mode varactors this corresponds to simply shifting the capacitance characteristic. At some tuning voltage both, depletion and accumulation occur within the usable voltage range. At medium tuning voltages and low gate voltages the varactor is in depletion (a,). The capacitance is low due to the series connection of oxide and depletion capacitance. With increasing gate voltage the flat-band case for

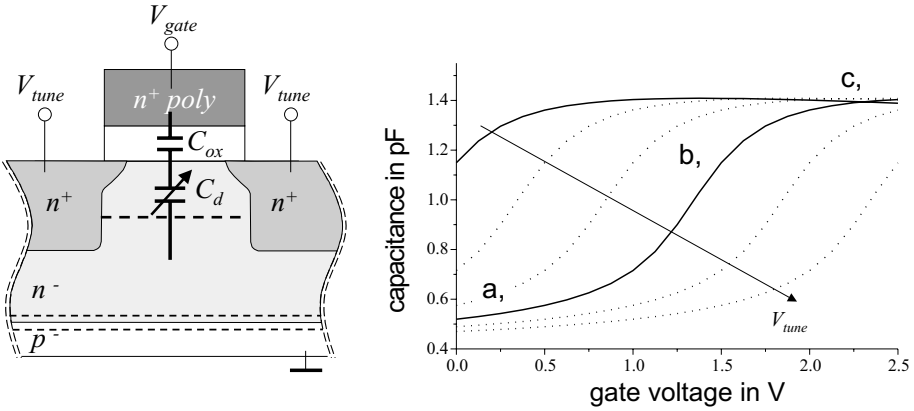

Fig. 7.11. Cross-section of an A-mode varactor in n^- well (in depletion *left*) and the measured small-signal capacitance characteristic *right* at various tuning voltages (0 V...2.5 V; 0.5 V steps). Dashed lines indicate the borders of depletion regions

the respective tuning voltage is reached (b,). Again increasing the gate voltage beyond $V_{FB}(V_{tune})$ leads to accumulation (c,), with high capacitance.
Even at high tuning and low gate voltages no capacitance increase due to inversion is observed. Without p^+ source/drain inversion can occur through thermally generated holes only. Such an inversion layer is present, however, it is electrically isolated and there is no reservoir of holes. At frequencies well above the generation rate of holes small-signal changes in the gate charge can not be balanced by changes in the inversion layer, but must be balanced by depth changes of the depletion layer. Therefore the capacitance remains low. Variation of the "DC" gate voltage, however, is very slow, and the corresponding change of gate charge is still balanced by holes. Thus, the depth of the

depletion region remains constant and the capacitance has a low value. For very low frequencies, at which holes can be generated fast enough the high capacitance due to inversion can be observed. But as the doping-dependent generation rates are on the order of milliseconds [100] and the corresponding frequencies in the hertz range, it is not expected that this phenomenon plays a role at the frequencies of interest, which are in the GHz range.

Part III

Fully Integrated VCO Designs

8

VCO Design Guide

8.1 Introduction

As shown in chapters 3 and 4, LC-VCO performance is heavily determined by the correct dimensioning of the LC-tank. This is now combined with the knowledge about CMOS devices from the previous chapter to select a set to design optimal tanks. The optimization of the tank-Q automatically leads to a different design, as when separately inductor-Q and capacitor-Q are optimized.
The inductance, of course, equals the inductance of the coil. The capacitance, in contrast, is the sum of the parasitic coil capacitances (winding to substrate and winding to winding), the varactor, the unavoidable capacitances of the active elements compensating the losses in the tank and the VCO-loads (prescaler, mixer, interstage buffers, or output buffers). The tank design goals from the previous sections can be recapitulated as 1) maximize L/C the ratio of inductance to capacitance, and 2) maximize L/R, the ratio of inductance to resistance. The first goal is limited by the systematic tuning range specified for a given (mobile) application, which has to be increased to meet the frequency specifications over component tolerances and the specified temperature range. The second goal is fundamentally limited by the given technology back-end (number and type of metals, thickness, conductivity, ...), although much can be obtained from an optimized inductor layout as proposed in Sect. 6.4.

8.2 Varactor Options

As presented in Sect. 7.1, junction diodes can be used as varactors in VCO-designs [53], or MOS-transistors can be used [88]. The junction diodes clearly suffer from their low C_{max}/C_{min} ratio, a problem that becomes even worse due to the ever decreasing power supply voltage resulting from technology downscaling.
For highest tank L/C ratio a MOS-varactor with a high C_{max}/C_{min} is clearly

preferred, as it enables the use of higher inductance values. For maximal varactor Q a minimal gate length should be preferred, but again MOS-varactor length should be chosen higher to increase C_{max}/C_{min}. As shown in Fig. 7.9, a multifingered folded layout can be used for minimal gate resistance or maximal varactor-Q, resulting in a measured Q at 2 GHz of at least 40 in standard 0.25 μm CMOS of INFINEON Technologies AG.

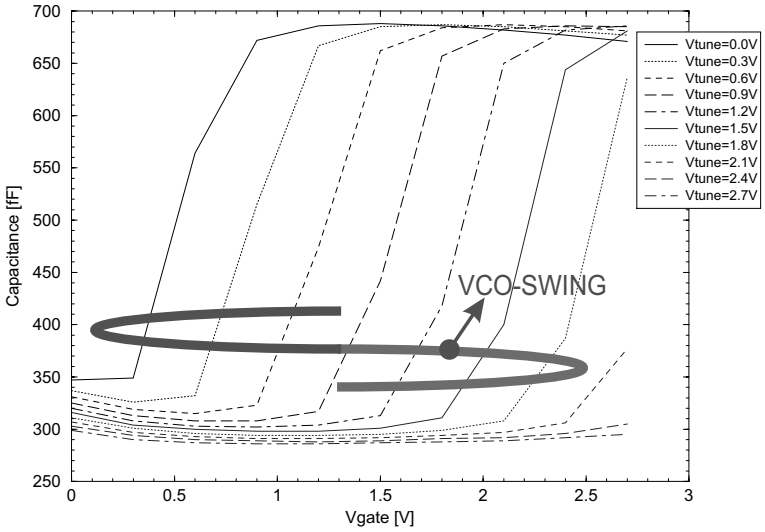

Fig. 8.1. NMOS varactor characteristic over backgate voltage

The MOS-varactors, however, have a very steep capacitance over voltage characteristic as shown in Fig. 8.1. To linearize the oscillator tuning characteristic, the varactors are directly coupled to the large signal swing over the inductor and the oscillator frequency is indirectly set through the backgate voltage V_{tune} of the MOS-transistors. As shown in Fig. 8.1, the steep curve can be shifted through the tuning voltage V_{tune} on the backgates. As the oscillator has a very large signal swing (nearly full power supply), the effective capacitance of the varactor is averaged over each VCO-period. The resulting capacitance varies linearly with V_{tune} in a range defined by the oscillation amplitude, a picture of a typical resulting frequency characteristic is given in Fig. 8.2. The capacitance variation over each oscillation period results in harmonic distortion of the oscillator sine. Although this distortion is partially rejected by the high Q of the LC-tank, it is probably a source of increased flicker noise upconversion [11].

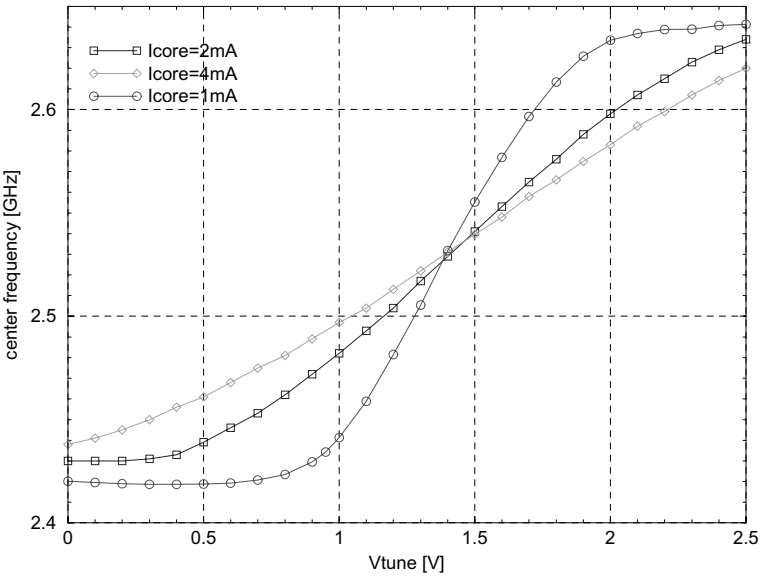

Fig. 8.2. Frequency tuning for different oscillator amplitudes

8.3 Inductor Options

External inductors [89] can provide very high quality factors. Their main drawback is found in the interface to the integrated oscillator core. The package pins, the bondwires, the pad capacitances, and the capacitances of the primary ESD-protection devices severely deteriorate the high quality factor. These interface effects aggravate with higher VCO frequencies. If the secondary ESD-protection has to be provided through series resistances, the use of external coils becomes impossible. Another drawback of the use of external inductors is the very complex coupling over the board from VCO to other inputs or outputs of the transceiver. Regarding the trend towards Zero-IF receivers [31] [40], this can be a killing point.

The option to use bondwire inductors [55] is limited by their low inductance, their inductance tolerance and the mechanical stability. Furthermore, their high volume manufacturability has not yet been proven.

A fully integrated solution suffers from low-Q on-chip coils, but avoids complex board crosstalk problems and is probably the most cost-effective, reliable and producible solution. The low Q of the integrated coils is mainly due to the thin metal layers available in standard CMOS technologies. However, considering the parasitic capacitances of integrated coils as a part of the tank capacitor and using fully-differential optimized coil layouts, it is possible to build fully integrated VCOs, competing with discrete VCOs on both phase noise **and** power consumption criteria. These optimized integrated were presented in de-

tail in Sect. 6.4. The optimization is obtained through the use of differential coil with high winding count and staggered winding widths (Fig. 8.3).

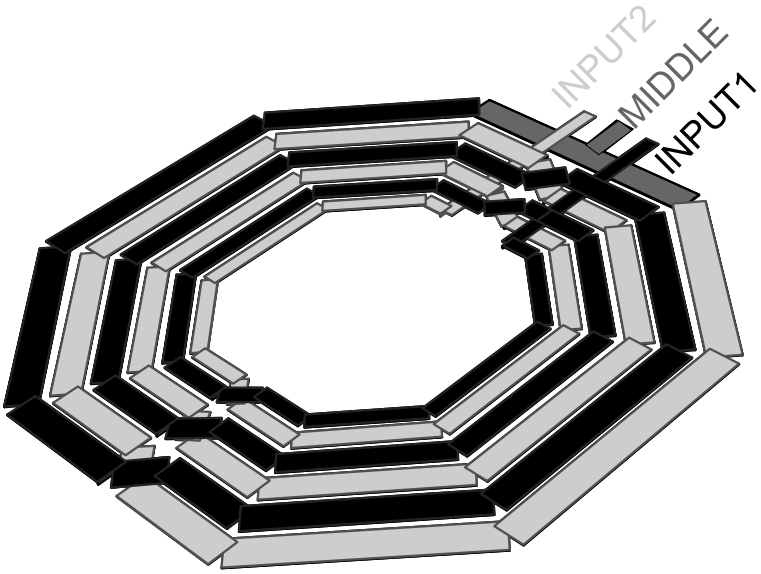

Fig. 8.3. Coil layout

8.4 VCO Topology

Many circuits options to provide the negative resistance of Fig. 1.11, to compensate for the tank losses, are available. Aiming at standard CMOS realizations, bipolar transistors are not available, but still NMOS, PMOS, or a combination of NMOS- and PMOS-transistors can be used. VCO-structures based on NMOS are presented in Fig. 8.4 [53]. The structure with the current source to ground has the smallest sensitivity to noise on the ground line, but the highest sensitivity to the power supply (pushing). This structure has a lower flicker noise upconversion than the structure with current source to the supply, due to the more symmetrical waveforms. This due to the smaller harmonic distortion caused in a MOS differential pair, if the tail node is connected to a current source instead of short-circuited to ground. Due to the inductors to the supply voltage, both structures easily have a signal swing of up to twice the power supply voltage on each node, which is a very nice feature for phase noise minimization through signal maximization, but it must be checked very carefully, if a reliable operation for the usually specified 15 years can be guaranteed, as the high signal swing will cause severe MOS-degradation

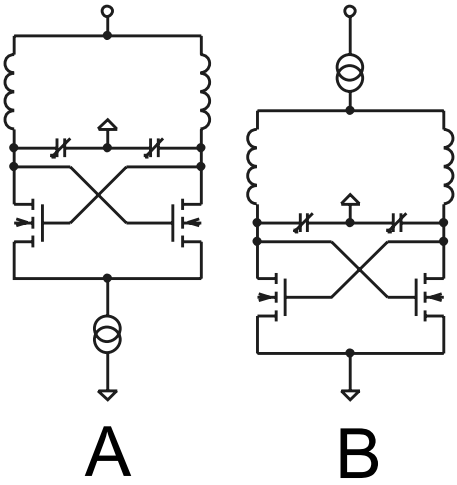

Fig. 8.4. NMOS VCO-cores, A. current source to ground, B. current source to supply

(hot electron effects) or even gate oxide breakdown. Both structures are well suited for low voltage operation, e.g., operation from one single battery, is no problem at all. Similarly, the same VCO-structures can be drawn using

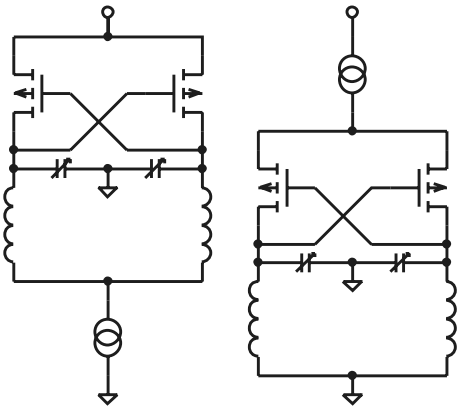

Fig. 8.5. PMOS VCO-cores

PMOS transistors, and the same discussion as for NMOS can be repeated. PMOS transistors are about half as fast as NMOS transistors and for the same transconductance per current, approximately double width is needed. Their lower flicker noise, however, or the fact that PMOS-transistors are situated in the wells, as most actual processes are of nwell/p-substrate type, can

be a strong argument to use PMOS instead of NMOS. Finally, both transistor types [11] can be combined to the structures presented in Fig. 8.6. The combination of NMOS and PMOS transistors generates a negative resistance from NMOS and PMOS, thus enabling effectively to half the power consumption for the same negative resistance. The signal swing is limited to power supply voltage, granting a reliable longtime operation within the voltage limits of the technology. The choice, whether to put the current source to ground or to power supply, will be dominated by the primary concern to minimize the sensitivity to ground or to power supply, which finally will depend on the package, the number of pads, and the application. An interesting and even

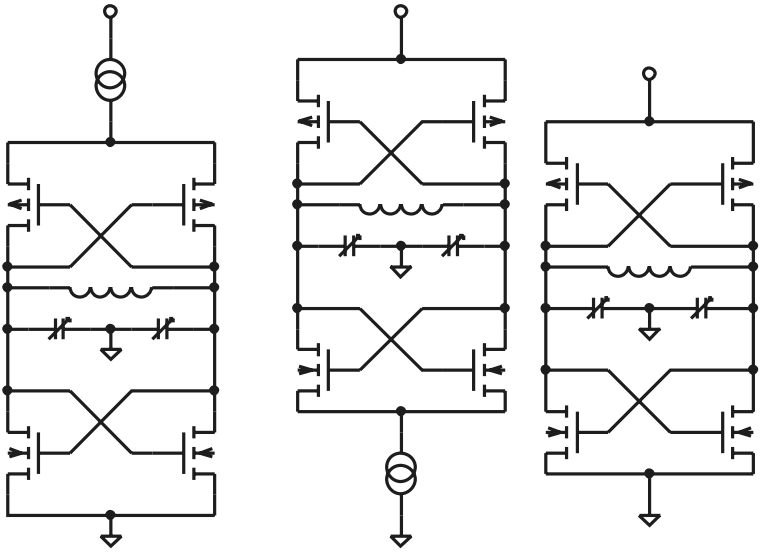

Fig. 8.6. Current reusing VCO-cores

novel VCO structure comes out if the current source is simply omitted. (Although the idea is rather trivial, an extensive literature search at IEEE Xplore and IEEE Member Digital Library [3, 4] for CMOS VCO designs showed no publication featuring this topology before its publication in [71] by the author of this work. Apparently independently [14] published the same topology one year later) The proposed structure has many advantages:

- Signal swing is maximized.
- After [11, 57] the current source is a very important phase noise source, this noise source is obviously completely eliminated.
- As all VCO-core transistors are put in a GHz-switching bias condition [37], flicker noise terms are reduced by at least 10 dB comparing measurement and simulation for several measured designs in 0.25 μm and 0.13 μm CMOS using this topology.

At first sight two disadvantages may arise from the topology without current source:

- a higher power supply sensitivity due to the lack of the current source
- a higher upconversion of flicker noise due to a higher harmonic distortion.

The differential tuning measurements of chapter 10, however, clearly show that the main source of power supply sensitivity is the varactor and not the active part of the VCO. Titan phase noise simulations for VCO designs with tank quality factors above 10 and recent publications [36, 96] show that the main source of flicker noise up-conversion should be searched in the varactor, and not in the VCO topology.

8.5 Conclusion

The guidelines for systematic low power low phase noise VCO-design of chapter 4 have been translated into clear design choices for the passive tank components presented in Part II, as well as for circuit options concerning the MOS transistors. As the high-Q tank design obtained strongly reject harmonics, the introduction of a new very digital NMOS/PMOS-topology without current source was enabled. The proposed set of LC-tank design options enables low power low phase noise VCO-design with an acceptable tuning range, and is demonstrated extensively with the designs presented in the next Part of this work.

9

1.3 GHz Fully Integrated CMOS VCO for GSM

9.1 Introduction

Many voltage controlled oscillators aiming at telecommunications systems (DECT, Bluetooth, GSM, ...) have been published [22],[53]. Phase noise requirements for DCS1800 have been achieved using fully integrated inductors or using bond wires. Assuming a minimal S/N of 9 dB for the baseband part of a GSM receiver, it is easily calculated from GSM blocking specifications, that maximum allowed VCO phase noise is -141 dBc/Hz at 3 MHz offset. The design goal for this integrated VCO is to fulfill this tough GSM phase noise upper limit **and** to consume less power than external VCO-modules currently in use, i.e. typically 15-25 mW [5, 6] . Using the systematic design of LC-VCOs, a fully integrated voltage controlled oscillator for a 900 MHz GSM heterodyne receiver with an IF at 400 MHz is to be designed. The LC-VCO is designed in low-cost 0.25 μm 4-metal standard CMOS process of INFINEON Technologies AG, using an integrated fully symmetrical coil. To the author's knowledge, even today, no standard CMOS ([57] uses BiCMOS with thick top metal layer and low resistivity substrate) fully integrated VCO featuring this phase noise at an acceptable power consumption has been reported.

9.2 Design

The VCO schematic is presented in Fig. 9.1. The coupled inductors (La, Lb, and K0 in Fig. 9.1) are laid out as one fully symmetrical coil with middle tap. The coupling factor of about 0.8 (FASTHENRY [80] simulation) nearly doubles the effective inductance. The differential layout generally makes the oscillator less sensitive to substrate noise when co-integrating it with other circuits. The symmetrical coil is operated in balanced mode and is modeled by a double π model as presented in Fig. **??**.

For the tuning of the oscillator conventional 4-terminal NMOS-transistors are used as varactors as explained in Sect. 8.2. Exactly the same varactor of

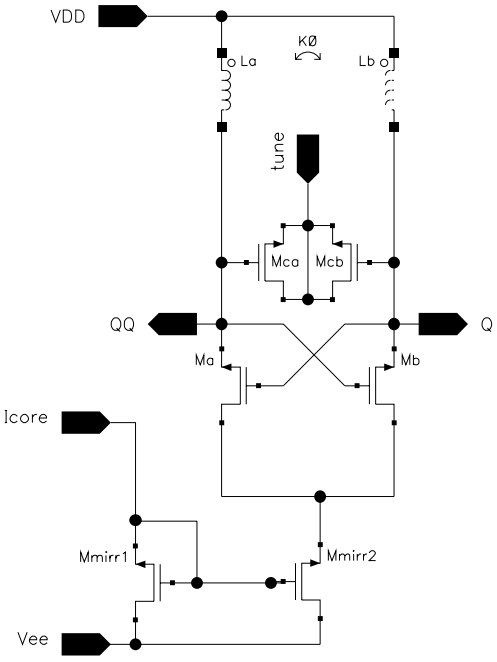

Fig. 9.1. VCO schematic, MOS-bulks are connected to Vee

Fig. 8.1 is used. A two-stage output buffer was added to drive 50 Ω loads. At the expense of a high current drain in the output buffer, no more integrated inductors were used for the buffer design to avoid magnetic coupling into the VCO core.

9.3 Measurements

The testchip photograph is shown in Fig. 9.2. Die size is 700 μm by 700 μm, coil size is 400 μm by 400 μm. The coil was separately characterized using s-parameter structures, the resulting lumped model is presented in Fig. **??**. Differential self-resonance frequency is 2 GHz, differential bandwidth Q is about 8 in the 1.3 GHz VCO frequency range. Also the MOS-varactor was characterized using s-parameter structures. Capacitance over gate-voltage can be found in Fig. 8.1. The minimum extracted varactor quality factor $Q = Im(Z)/Re(Z)$ over gate voltage at $2GHz$ is over 40. The measured and simulated tuning-characteristic of the VCO is presented in Fig. 9.4. The slope is very linear and shows the effectivity of the large signal varactor averaging. It is well suited for a frequency synthesizer realization (PLL). Unfortunately, the pushing or power supply sensitivity is as large as the sensitivity to the tuning input and

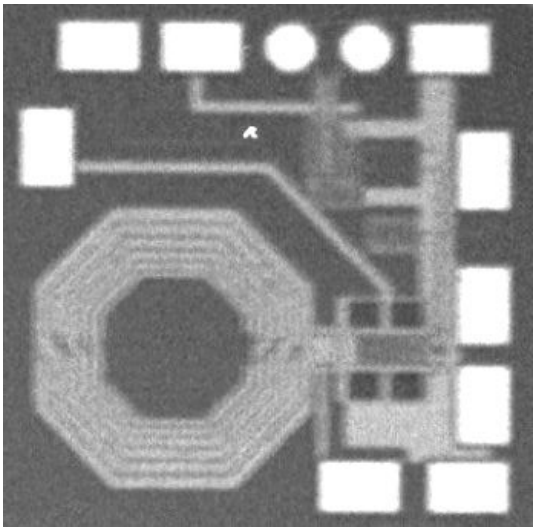

Fig. 9.2. Chip photograph of VCO

equals to a maximum of 130 MHz/V. This is directly due to the chosen VCO-topology: changing the tuning input voltage or changing the DC power supply voltage connection to the middle of the coil, both leads to exactly the same shift at the MOS-varactors, and thereby leads to the same shift in the varactor averaging over the oscillator period. Phase noise was measured using Europtest PN9000 equipment (delay line method), the result is presented in Fig. 9.3. Phase noise increases by circa 3 dBc over the tuning range. Also in Fig. 9.3 the simulated phase noise is presented. This design features a VCO figure of merit (1.12) of -182.6 dBc/Hz at 1.2 GHz or -180.9 dBc/Hz at 1.4 GHz. In appendix C recently published VCOs are listed. Table C.1 lists recent fully integrated pure CMOS VCO-designs and shows that this design has a very state-of-the-art phase noise performance with a lower power dissipation. Only a few BiCMOS designs (Table C.2) or VCOs based on external components outperform this design in terms of low power consumption and low phase noise. The measurements are summarized in Table 9.4.

9.4 Simulation Versus Measurement

MOS transistors are modeled by simple subcircuits around a standard MOS-model (BSIM3v3.2) adding gate, source, drain and bulk resistances [41]. The subcircuit values can be found in Fig. 5.3. For the coil the model in Fig. **??** is used. Also for the varactor a subcircuit around a MOS-model (BSIM3v3.2) incorporating the gate resistance is used. SpectreRF [24] of Cadence and TITAN (INFINEON Technologies AG proprietary SPICE [50]) were used.

Both simulators delivered the same results, although TITAN is completely frequency-domain harmonic balance based [9], whereas SpecteRF is time-domain based [8]. As clearly visible in Fig. 9.3 phase noise simulation and measurement match very good within 2 dB at far offset frequencies (white noise 20 dB/decade region). At lower offset frequencies a mismatch between simulated and measured flicker noise corner frequency becomes visible.

Table 9.1. Measurement summary

Frequency	1.3 GHz
Tuning range	200 MHz
Pushing	$<$ 150 MHz/V
Phase noise @3 MHz offset	-142 dBc/Hz
FOM	-180.9 dBc/Hz
Supply	2 V
Current	7 mA

9.5 Summary

A fully integrated CMOS LC-VCO at 1.3 GHz with a linear tuning range of over 200 MHz is presented. Through the optimization of the complete LC-tank, using a combination of an optimized fully symmetrical coil geometry and folded NMOS-varactors, a measured phase noise of as low as -142 dBc/Hz @ 3 MHz or -112 dBc/Hz @ 100kHz is obtained. Hereby the VCO fulfills GSM 900 MHz receive phase noise requirements at a power consumption of only 14 mW.

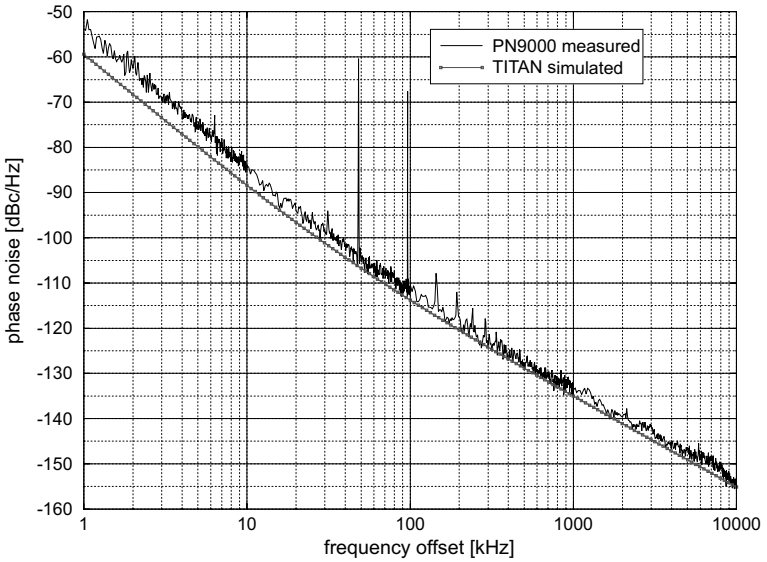

Fig. 9.3. Measured and simulated phase noise at 2 V power supply, 7 mA core current, frequency=1.21 GHz

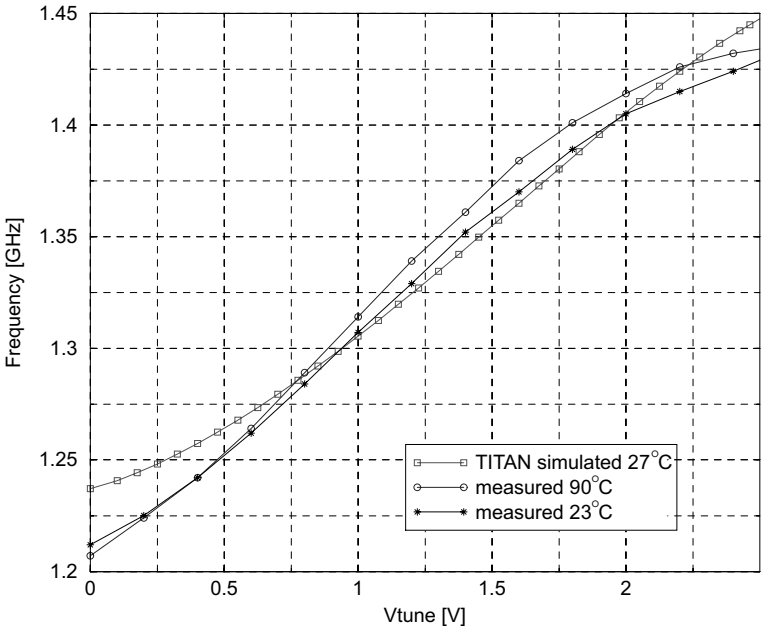

Fig. 9.4. VCO measured and simulated tuning

10

1.8 GHz Quadrature VCO Design for DCS1800 and GSM

10.1 Introduction

Aiming at highly integrated low-cost receivers in standard CMOS, it is not sufficient to integrate a low power low phase noise differential VCO, but quadrature signals (sine and cosine or 0 and 90 degree signals) should be provided for complex demodulation in zero-if or low-if systems (Fig. 10.1). Furthermore,

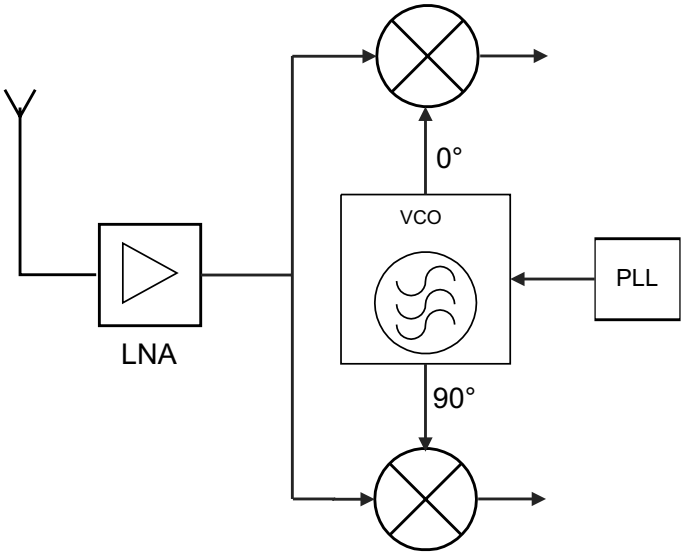

Fig. 10.1. Complex demodulation receiver path

the VCO-design should be suited for a high integration of the complete receiver including the phase locked loop (PLL). The design proposed in this

chapter aims at DCS1800, DECT, and/or GSM highly integrated low-IF receivers. To reduce on-chip PLL crosstalk a novel differential tuning concept is introduced.

10.2 Quadrature Generation

Three design options are available to generate quadrature signals:

1. Combination of VCO, polyphase-filter (or R-C C-R filter) and output buffers (or limiters) as used in e.g. [54, 68].
2. VCO at double frequency followed by master-slave flipflops.
3. Two cross-coupled VCOs as proposed in [16].

The first option needs four output buffers or limiters, consuming a lot of power. If buffers are inserted between VCO and filters even more power is needed, if the filters are directly connected to the VCO-tank, tank capacitance is increased, leading to higher power consumption (Eqn. 4.3) and worse phase noise (Eqn. 4.6). Furthermore, a lot of chip area is needed, as the filters need good matching.
The second option has the smallest area. This option needs a VCO designed at double frequency, which should not consume more power, as a higher Q_{tank} for integrated tanks at higher frequencies is achievable (inductance scales down linearly when sizing down an integrated coil, coil-capacitance scales down quadratically, so L/C improves). However, the master-slave flipflops, which have to be designed for the doubled frequency, consume too much power in the 0.25 μm CMOS technology used here. As soon as 0.18 μm or 0.13 μm technology generations are widely available, this changes rapidly. If primary design concern is low cost or small area, then this solution clearly must be preferred, as the VCO designed at double frequency features a smaller coil and the area of the master-slave flipflops in sub-μm CMOS is negligible. Also in ZERO-IF receivers, this solution should be preferred because it avoids direct parasitic coupling between VCO and receiver input.
The third option comes at the cost of double VCO-area. Option 3 outperforms the other solutions in terms of power consumption, as soon as a well designed VCO-core consumes less power than the four output buffers or limiters of option 1, or as soon as the VCO-core consumes less power than the master-slave flipflops designed for double frequency, needed to realize option 2. The 2-core solution furthermore provides a very high voltage swing, which eases the design of prescaler and mixer circuits somehow connected to the VCO. This consideration can also be extended to VCOs using external high quality inductors. When using external inductors, a lot of current must be spent to amplify the VCO-signal to drive the filters (external VCO at nominal frequency) or to drive the flipflops (external VCO at double frequency).

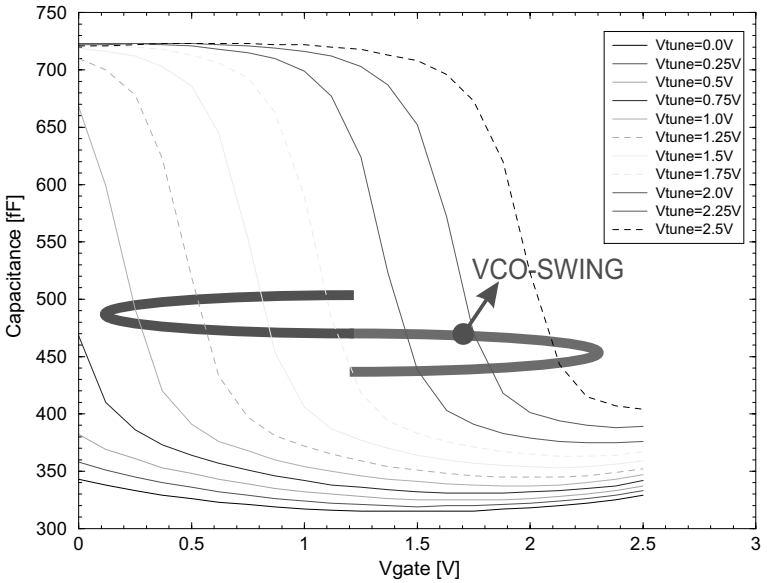

Fig. 10.2. PMOS varactor characteristic over backgate voltage

10.3 Differential Tuning Concept

Of course, as already presented in Fig. 8.1 for NMOS, also PMOS-transistors can be used as varactors (measured data in Fig. 10.2). VCO-gain (K_{vco}, [MHz/V]) and VCO-gain linear region depend on the signal swing of the oscillator and the ratio C_{min}/C_{max} of the varactor (Fig. 8.2). C_{max} is obtained in strong inversion mode and depends on the oxide thickness t_{ox} of the MOS-gates, it is identical for NMOS and PMOS, $C_{max-PMOS} = C_{max-NMOS}$. Varactor C_{min} is obtained in weak inversion mode [17], and depends on the complex channel doping profile, including LDD- and HALO-implants. In the sub-μm CMOS-process used here, the ratio $C_{min-PMOS}/C_{min-NMOS} \cong 0.85 \cong 1$ (the number is process dependent). Finally, the signal swing, of course, is identical for PMOS and NMOS varactors. So a parallel connection of NMOS and PMOS varactors enables in first order a differentially tuned VCO with equal but opposite signed gain K_{vco} to NMOS and PMOS tuning input.

10.4 Design

As, for the 0.25 μm CMOS-process available for this design, the cross-coupled quadrature VCO definitely outperforms the other quadrature solutions in terms of power consumption, it was combined with the differential tuning concept leading to the final schematic of the prototype IC, presented in Fig.

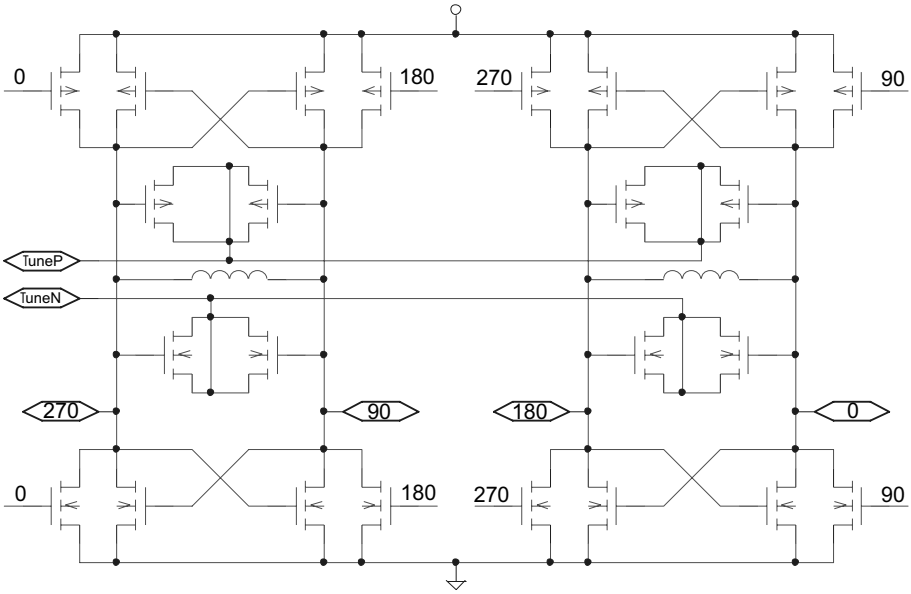

Fig. 10.3. Quadrature VCO schematic.

10.3. The highly doped substrate non-epi CMOS process offers four thin metal layers. The integrated 9 nH inductor was derived from the 13 nH inductor from the previous chapter through a physical layout and model scaling of Sect. 6.5 [76]. Again, the three top metals were put in parallel to reduce the series resistances.

For maximal speed and minimal tank capacitive load, all transistors (not including the varactors) lengths were set to minimal length of 0.25 μm. Excessive white noise [32, 62, 91, 98] could become a strong argument in more advanced sub-μm processes to choose lengths greater than minimal.
The widths of the MOS-transistors of the cores were dimensioned for maximal amplitude and for maximal symmetry of the sine waveforms, using ordinary transient simulations (At the design stage of this oscillator phase noise simulation was not yet available in TITAN, and SpectreRF did not converge). Also by means of transient simulations, optimal core cross-coupling width was set to one third of the width of core-transistors. If the cross-coupling is made to weak, a two-tone oscillation is possible, if it is made too strong, power is wasted and extra parasitics load the tanks. The chipphoto in Fig. 10.4 shows the perfectly symmetrical layout. Testchip die size is 1500 μm by 700 μm.

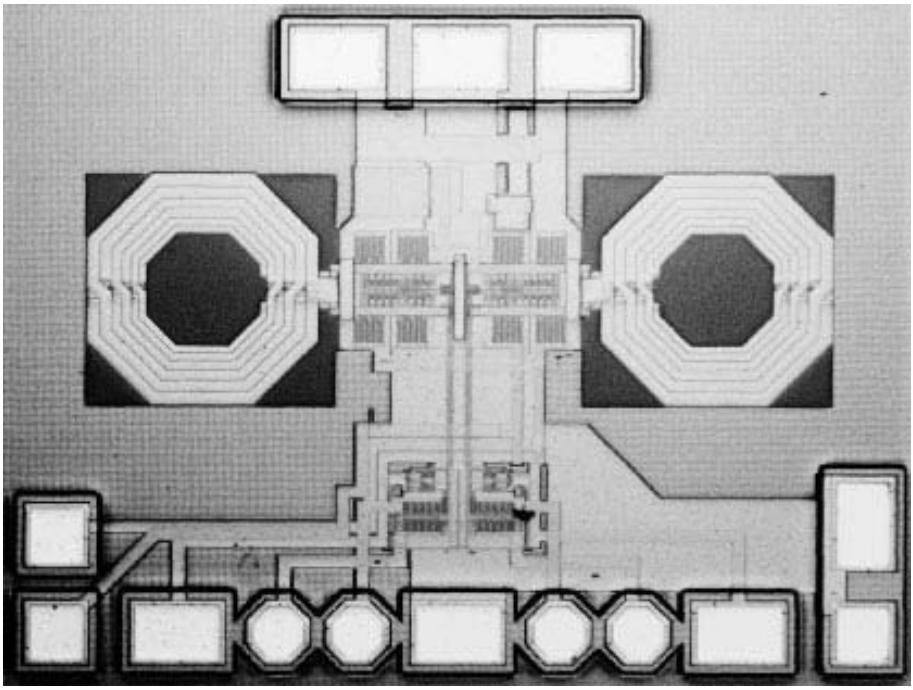

Fig. 10.4. Chip photograph of VCO

10.5 Measurements

The 3D tuning-characteristic of the VCO is presented in Figs. 10.5 and 10.6. As the slope is very linear, it is well suited for a frequency synthesizer realization (PLL). Phase noise was measured using Europtest PN9000 equipment (delay line method), the result is presented in Fig. 10.7. The power supply sensitivity also was characterized. If PMOS tuning input is referenced to VDD and NMOS tuning input is referenced to VSS, power supply sensitivity is suppressed as well as tuning common mode voltage to 2 .. 9 MHz/V. If both tuning voltages are referenced to VSS, no benefit is seen, which is easily explained through the averaging of the NMOS an PMOS varactors towards tuning and power supply connections. In that case, all bulks of the PMOS varactors should be connected to some extra voltage source referenced to VSS. In triple well processes or in SOI, an easier differential tuning, effective towards tuning common-mode and power supply, can be obtained using N-type and P-type accumulation MOS-varactors [81].
A quadrature accuracy of ca. 3° was measured. This number is mainly due to limited accuracy of the measurements. For instance a bondwire length mismatch of only 0.2 mm (≅0.2 nH) leads to ca. 1° phase mismatch. Table 10.1

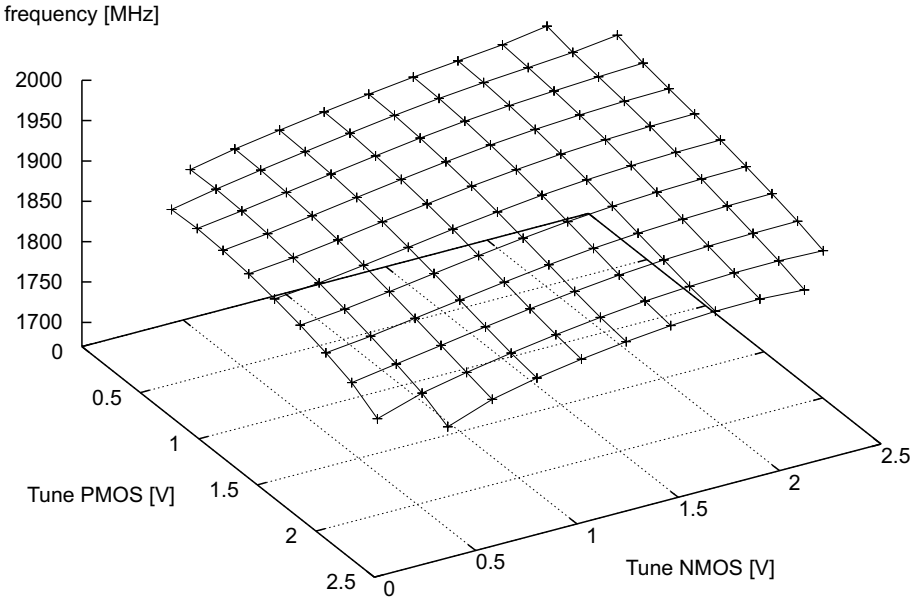

Fig. 10.5. VCO tuning range

gives a summary of the measured performance.
The normalized phase noise FOM (1.12) results in -185.5 dBc/Hz for this design. In Appendix C, Table C.3 lists most recently published quadrature VCOs. It shows that this design has a state-of-the-art phase noise performance at an extremely low power dissipation. Also comparing this design with other CMOS VCOs (Table C.1) or with BiCMOS designs (Table C.2) shows a very state-of-the-art performance in terms of low power and low phase noise.

Table 10.1. Measured quadrature VCO performance summary.

Center frequency	1.72-1.99 GHz
Tuning range	280 MHz (17%) differentially
Phase noise	¡ -143 dBc/Hz @ 3 MHz
Quadrature mismatch	¡5°
Power	20 mW (7.8 mA @ 2.5 V)
Technology	standard 0.25 μm CMOS
Area	1.1 mm^2 (incl. pads)

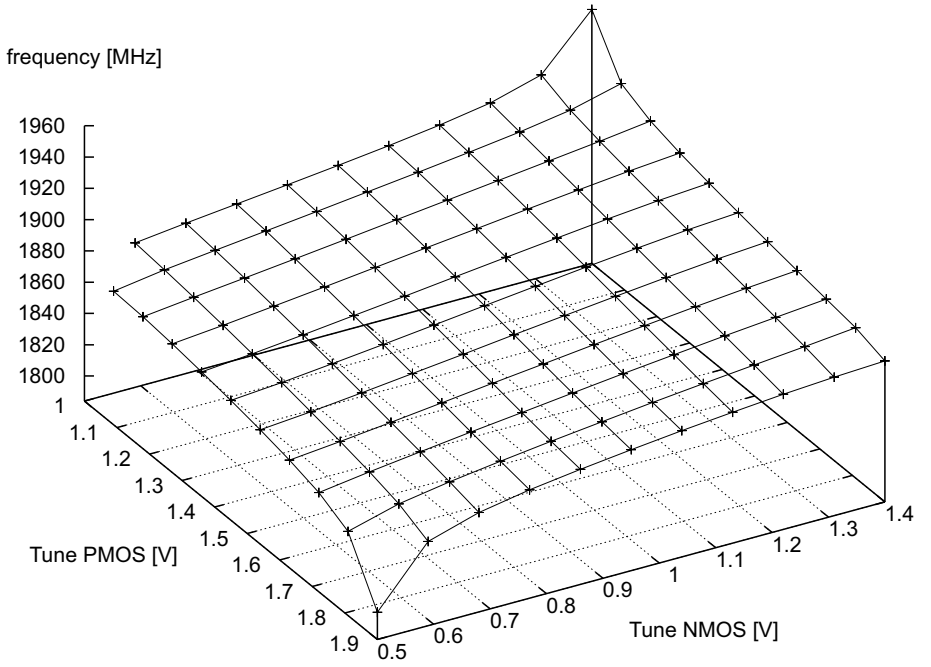

Fig. 10.6. Zoomed VCO tuning range

10.6 Summary

The design problem to minimize the overall power consumption of a VCO with quadrature outputs is solved using two cross-coupled fully integrated high-inductance VCO-cores without current source. A prototype quadrature LC-VCO for 1.8 GHz was designed in 0.25 μm standard digital CMOS. A differential tuning range of 280 MHz was obtained through the use of NMOS and PMOS varactors. Measured worst-case negligible is -143 dBc/Hz @ 3 MHz. Hereby the VCO fulfills GSM and DCS1800 receive negligible requirements at a power consumption of only 20 mW.

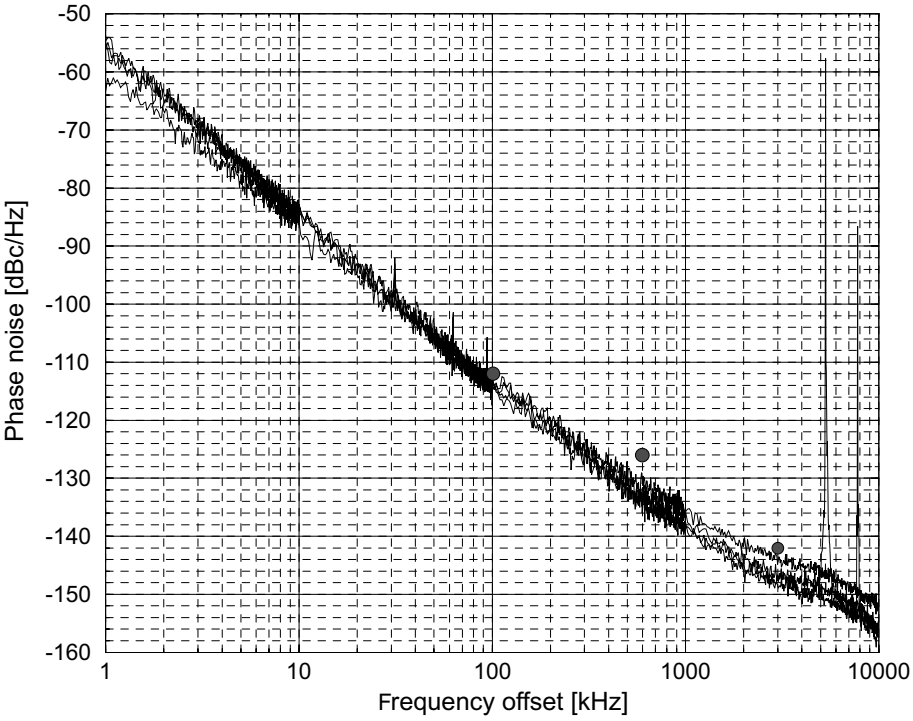

Fig. 10.7. Measured phase noise over frequency tuning at 2.5 V power supply, 7.8 mA core current. Dots indicate GSM-requirements

11

A Fully Integrated 51 GHz VCO in 0.13 μm CMOS

11.1 Introduction

Fully integrated VCOs with frequencies in the millimeter-wave bands have mainly been realized in III-V or SiGe technologies. The ongoing shrinking of CMOS technologies to deep-submicron recently enabled the design of CMOS oscillators at frequencies in the range of 10 to 50 GHz [20], [45], [49], [23]. However, up to now, designs reaching frequencies over 30 GHz are power-hungry or use non-standard options such as high-resistivity substrate, thickened top metal, SOI and buried or epi layers. This chapter presents the design of a 51 GHz low phase noise VCO in 0.13 μm standard bulk CMOS featuring a very stable oscillation at 1 V with only 1 mW of core power consumption.
This low power CMOS VCO-design was motivated by the ever increasing frequency and bandwidth demands of data-communications applications (40 Gbit and beyond). The design, furthermore, is a perfect demonstration and test of the capabilities of the 0.13 μm standard CMOS technology and serves as a modeling verification.

11.2 Design

The schematic of the oscillator is presented in Fig. 11.1. An NMOS-only topology is chosen for speed as NMOS f_T of ca. 100 GHz is much higher than PMOS f_T of ca. 50 GHz. As the voltage swing of this topology exceeds the power supply, the supply voltage is reduced from nominal 1.5 V to 1 V for a reliable operation within the technology limits. In order to optimize the circuit for highest frequencies and lowest power, a global optimization of the active core, integrated coil, and 50 Ω-output stage has been performed. Furthermore, special care in the layout is invested to keep the dimensions as small as possible to minimize the parasitics and to keep the size well below the 50 GHz wavelength enabling a design approach based on lumped models. The systematic VCO design approach from chapter 8 is applied, which means that

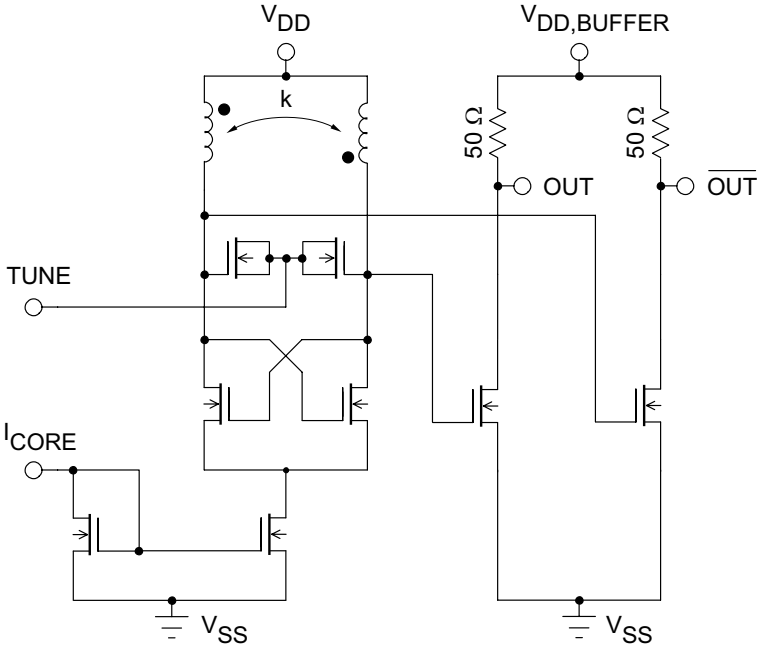

Fig. 11.1. VCO schematic

the tank inductance has to be maximized for lowest power consumption and phase noise. For a given oscillation frequency and especially at 50 GHz, the maximization of the tank inductance once more stresses the minimization of all capacitances. One fully symmetrical coil with middle tap is preferred over a two-coil solution, as the coupling factor improves the inductance per area, leading to a lower inductor to substrate capacitance. The main design parameters are the widths of the MOS transistors and the coil parameters radius, winding widths, winding spacing and winding count. To assure a very compact layout, the differential coil winding count should be odd, placing the middle connection on the other side of the coil. For a constant total inductance, higher winding counts decrease the inductor to substrate capacitance, but deteriorate the coil self-resonance frequency through an excessive winding to winding capacitance. For a fast and efficient estimation of the coil model, a combination of the FASTHENRY and FASTCAP [80] electromagnetic simulators is used by means of the approach described in [29]. Few design iterations led to the final choice of a three windings inductor with quadratic winding staggering, as presented in Fig. 11.2. The inner coil winding is 2.5 μm wide, each next winding width is 20% wider than the previous one. This winding staggering effectively improves the series resistance of the coil without a deterioration of the coil self-resonance. As shown in the cross-section presented in Fig. 11.3, a parallel shunt connection of metal 4, 5, and 6 (all copper) is chosen for the coil

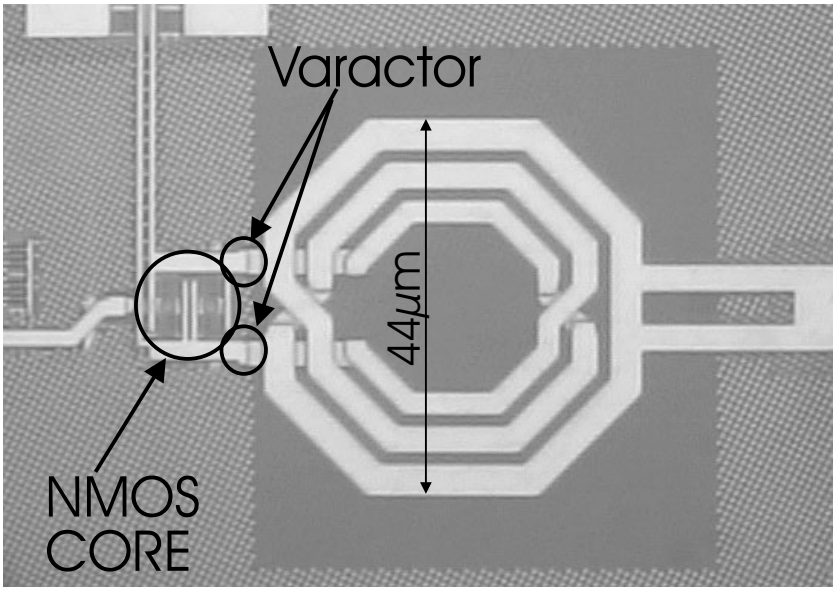

Fig. 11.2. VCO and coil layout

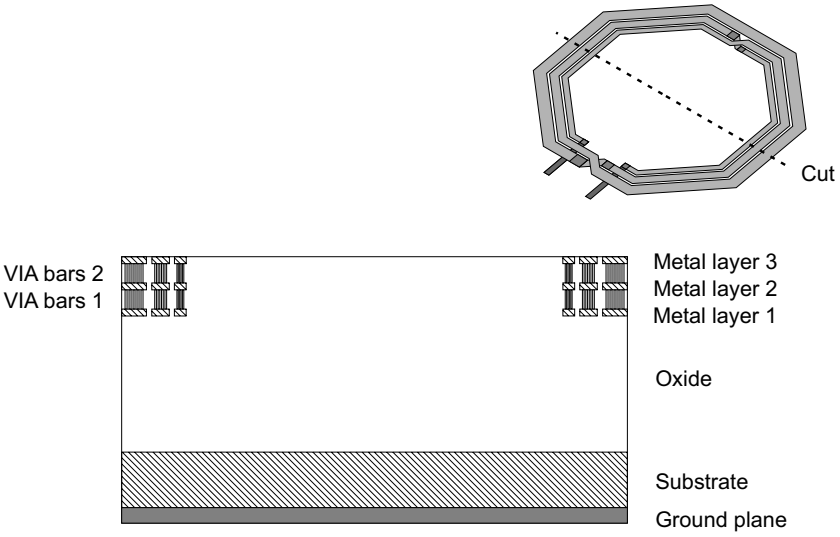

Fig. 11.3. Optimized inductor cross-section

windings as the best compromise between winding series resistance and winding parasitic capacitance to substrate. Another important series resistance improvement is obtained by the insertion of copper viabars (long-line VIAs) along the windings. The simulated coil model, used for the design simulations, is presented in Fig. 11.4. The self-resonance of the coil benefits from the SILK low-k dielectric. For the frequency tuning a normal NMOS transistor is used

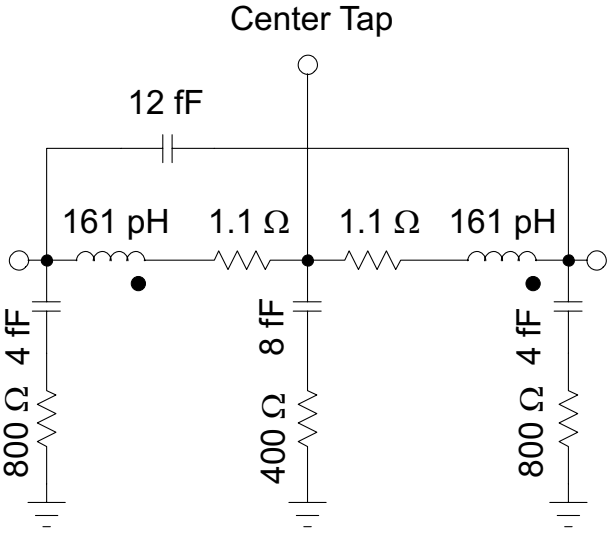

Fig. 11.4. Coil simulated model

as varactor. The varactors are laid out as a multi-finger structure to maximize the Q of the varactor. Each finger features a size of 1.5 μm/0.12 μm and is contacted on both sides, resulting in a modeled Q of about 60 for the varactor at 50 GHz (NQS-effects are neglected). The varactor is placed under the connections of the inductor to realize a very compact LC-tank layout (Fig. 11.2). The varactors are modeled using a standard BSIM3V3.2 MOS model and an external gate series resistor. Also for the MOS transistors in the VCO-core

Table 11.1. Simulation summary

Frequency	53 GHz
Tuning range	1.4 GHz coarse
	800 MHz fine
SSB phase noise	-95 dBc/Hz @ 1 MHz
Power supply voltage	1V
Core power consumption	1 mW

and in the output driver, multi-fingered layout transistors are used. Again the model is a standard BSIM3V3.2 model with an external gate series resistor. S-parameter measurements on the same transistor layout show a f_t of about 100 GHz and a f_{max} of about 60 GHz. The single-stage output buffer is terminated with on chip 50 Ω-resistances for unproblematic RF-measurements, although it reduces the expected output power to about -15 dBm per node. The buffer reuses the MOS transistor-layout of the core.

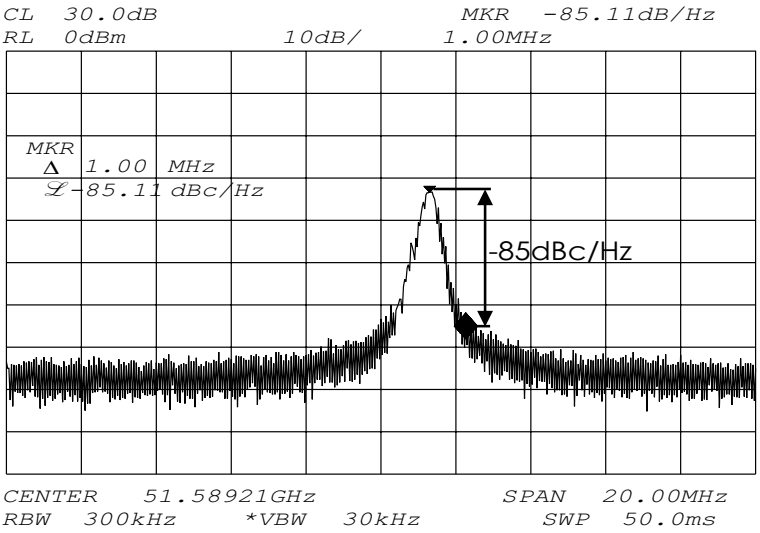

Fig. 11.5. Measured phase noise at 51.6 GHz, 1 mA core current and 1 V supply voltage

11.3 Measurements

The chip photo is presented in Fig. 11.6. Die size of 900 μm by 500 μm is dominated by the pads and power supply decoupling capacitors. The VCO-core size is only 60 μm by 40 μm. Measurements were acquired with an HP8562E spectrum analyzer and HP11974V preselected 50-75 GHz RF-section. As the imide covering the chips was too thick to contact the output pads with RF-probes, an on-wafer measurement was impossible and the chips were mounted chip-on-board on a RO4003 microwave substrate. The impedance of the bondwires and the losses in the RO4003 substrate drastically reduced the output power to ca. -30 dBm per node. The VCO starts oscillating at a bias current of 600 μA at 1 V. The output buffer draws 5.5 mA from a 1.5 V supply. For the measurements, a microwave amplifier HP83050A compensates the losses

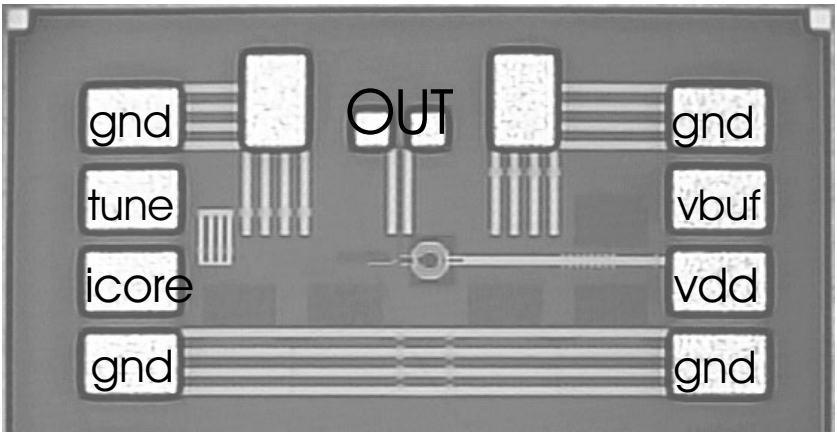

Fig. 11.6. 51 GHz testchip photograph

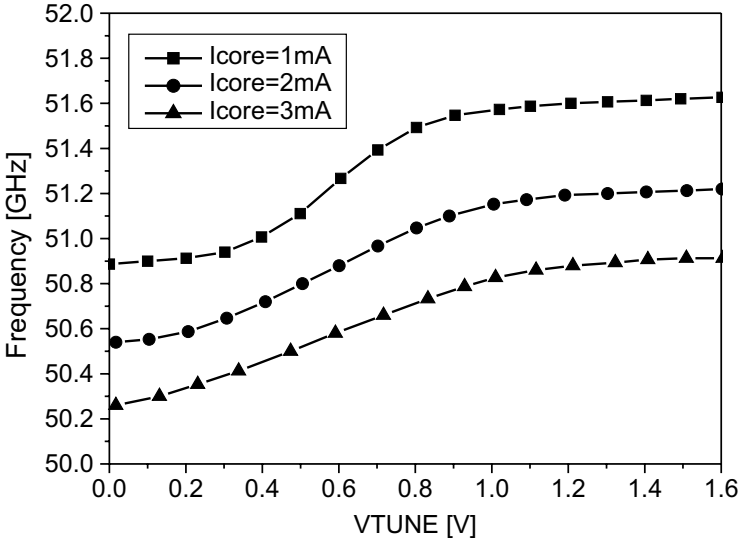

Fig. 11.7. Measured tuning range for different core currents and 1 V supply voltage

from the bondwire and the measurement setup. The resulting output spectrum and phase noise of the VCO at 1 mA bias current and maximal tuning voltage is presented in Fig. 11.5. The frequency tuning for different bias currents is shown in Fig. 11.7. Although no coil skin effect , no coil eddy current substrate losses, and no NQS-modeling were included in the design simulations, all measurements fit to the design simulations within better than 10%. With a phase noise of -85 dBc/Hz at 1 MHz offset from the 51.6 GHz carrier, this design features a VCO figure of merit ([85], Eqn. (1.12)) of -179 dBc/Hz. The results for this 1 mW fully integrated 51 GHz VCO are summarized in Table 11.2.

Table 11.2. Measurement summary.

Technology	
Metalization	6 Metals Cu
	SILK low-k dielectric
Substrate resistivity	6 ΩCm
Frequency	51 GHz
Tuning range	1.4 GHz coarse
	700 MHz fine
SSB phase noise	-85 dBc/Hz @ 1 MHz
Power supply voltage	1 V
Core power consumption	1 mW
Chip size including pads	0.5 mm x 0.9 mm

11.4 Summary & Outlook

The 51 GHz VCO design has not yet any practicable application, but clearly demonstrates the feasibility of VCO design in CMOS and once more the power of the high-inductance approach. The high inductance tank allows a very low power consumption, thereby to very small MOS transistors in the active VCO-part enabling the high operational frequency. The price paid for this design exploiting design and technology frequency limits, is the limited tuning range. Although CML-logic frequency dividers can be realized in 0.13 μ up to very high frequencies exceeding 20 GHz [47], this clearly is still far below the 51 GHz frequency of the presented oscillator. Precondition for any practical use of this oscillator is the ability to divide the signal, which leads to a new (patent submitted) divider circuit presented in [75].

12

Dual Band 1 GHz / 2 GHz VCO Design

12.1 Introduction

The examples of the previous chapters illustrate the wide use of fully integrated LC voltage controlled oscillators (VCO) for wireless telecommunication systems. Also for the implementation of clock-circuitry and frequency synthesizers in wireline systems LC-VCOs are the preferred solution. The LC-VCO implementation is normally preferred over ring-oscillator circuits for its better phase noise/jitter performance at a much lower power consumption. The remaining disadvantage of an LC-VCO is the limited tuning range. Solutions to extend the tuning range based on switched capacitor banks [12] or switching VCO-inductors [7] have been presented.
The capacitor switching solution suffers from the large switches needed for the Q of the coil. It furthermore decreases the tank-inductance to the value necessary for the specified lowest center frequency leading to higher power consumption and phase noise as described in chapter 4 or in [73, 74, 78].
Switching the inductors is severely limited by the switches. If the switches are designed for minimal series resistance in order not to deteriorate the Q of the tank, huge capacitances are introduced at the RF-nodes of the oscillator, leading again to higher power consumption and phase noise.
More generally, the systematic low power low phase noise design approach proposed in this work maximizes the tank inductance and minimizes the varactor size to the limit given by the tuning range specification. This design tradeoff problem between low power and tuning range obviously vanishes completely, if the varactor could be omitted and the VCO could be frequency controlled over its inductor, leading to the concept introduced in this chapter.

12.2 A Fully Differential Voltage Controlled Inductor

The proposed voltage controlled inductor (patent submitted) is based on the special coil layout already used and discussed in chapter 9 ([73]). The layout

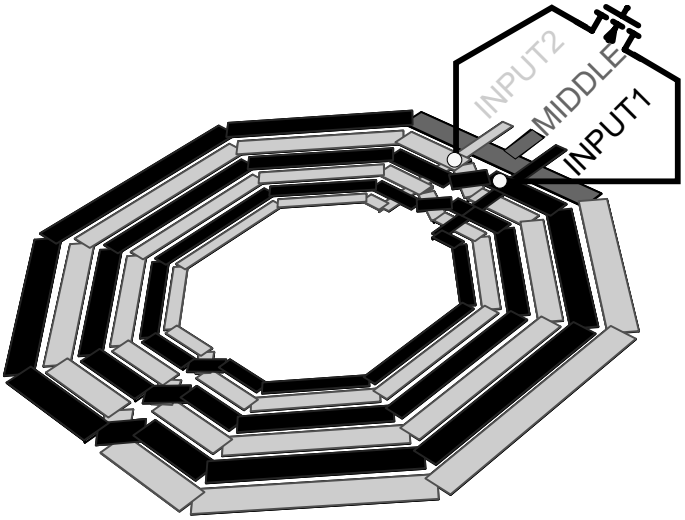

Fig. 12.1. Differential voltage-controlled coil layout

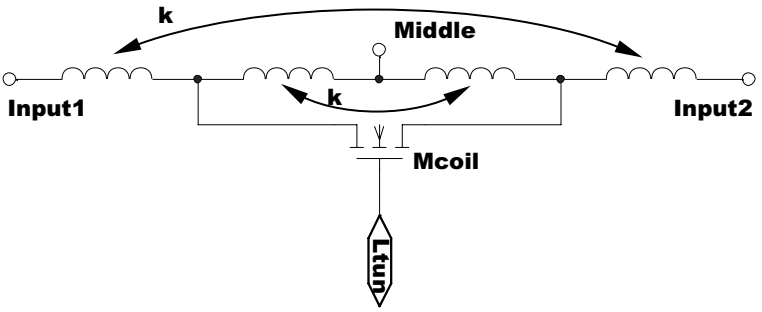

Fig. 12.2. Differential voltage-controlled coil lumped model

of the staggered winding width coil is shown in Fig. 12.1. As the RF-nodes are put at the inside of the coil, the outer winding of the coil is at common mode in differential mode and its winding width can be increased to reduce its series resistance without any disadvantage of the increased capacitance into substrate. The influence of any additional capacitance connected to the other windings is proportional to the respective differential voltage. The differential voltage across a winding is proportional to the inductance and varies quadratically with the winding number from the inside to the outside of the layout. Thus, the largest differential RF voltage swing is found at the inner windings of the coil and only a minor voltage swing occurs at the outer windings. The proposed voltage-controlled inductor exploits this effect and adds a large MOS-switch between the outer windings of the coil. The rather large parasitic capacitances

from the MOS device only marginally affect the self-resonance of the coil as they are placed at nodes with a small voltage swing. Also the series resistance of the coil is not deteriorated as the MOS-switch can be made very wide. If the MOS switch is off, the proposed inductor has an inductance and self-resonance similar to the layout without the MOS switch. If the MOS switch is on, the proposed structure is reduced to a smaller inductor consisting of the inner windings, with a smaller inductance. The differential self-resonance is clearly increased, as the short-circuited windings are at common-mode and the resulting smaller coil layout has less winding to winding and winding to substrate capacitance. If the MOS transistor is used as variable resistance, the effective inductance of the structure can be tuned continuously over its gate voltage. A simplified lumped model for this differential voltage-controlled inductor is presented in Fig. 12.2. As a fully integrated VCO is very sensitive to coil series resistance and self-resonance, the proposed tunable coil was implemented in a VCO to demonstrate its feasibility and usability. Of course, this structure is not only useful for dual band VCO-applications, but it can also be very useful to switch the gain of inductively loaded LNAs, mixers, or output drivers.

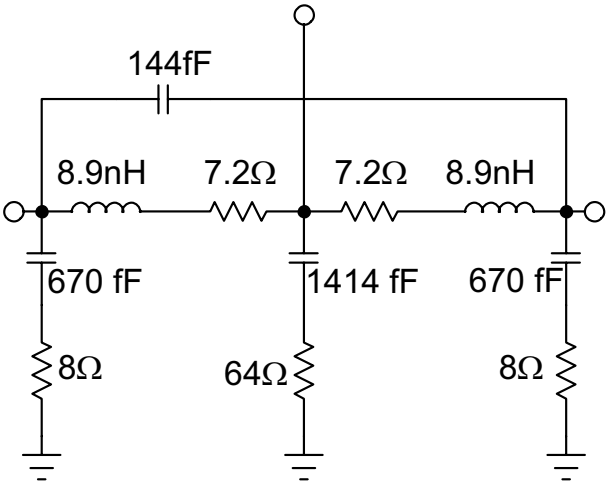

Fig. 12.3. Extracted coil lumped model without transistor *Mcoil*

12.3 Design

The VCO-design is based on the design described in chapter 9 or in [73]. Only the coil was replaced. Three more staggered windings were added to

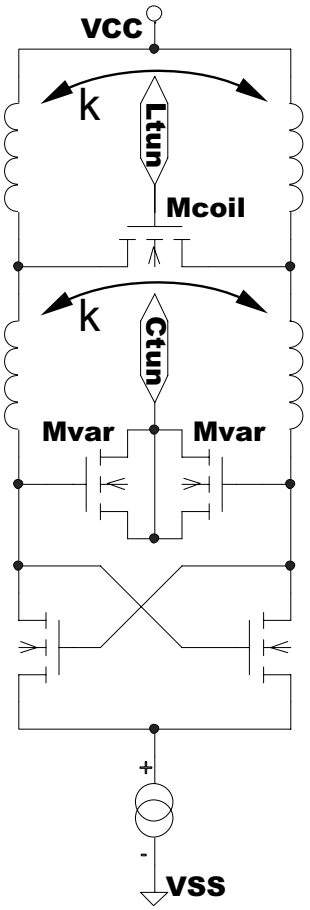

Fig. 12.4. VCO schematic, MOS-bulks are connected to VSS

its six windings coil layout, resulting in an inductance of 17.8 nH. Metal 2, 3, and 4 were put in parallel for a total thickness of 1.7 μm Al to reduce the series resistance. Total metal thickness in [7] is 4 μm. The nine windings coil, without the inductor-controlling transistor, was separately characterized using s-parameter structures, the resulting lumped model is presented in Fig. 12.3. Differential self-resonance frequency is 1.7 GHz, differential bandwidth Q is about 7 in the 1 GHz VCO frequency range. Figure 12.4 presents the VCO schematic. The VCO has two frequency control inputs. One input, $Ctun$, tunes the NMOS varactor and provides classical capacitive tuning. The second input, $Ltun$, tunes the inductance through the MOS-transistor $MCoil$. This very large NMOS transistor is clearly visible in the chip photograph of Fig. 12.5. The odd winding count of the coil is optimal for the floorplan of the

layout as the big transistor Mcoil is situated automatically at the opposite side of the RF-nodes. A 50 Ω output buffer completes the design.

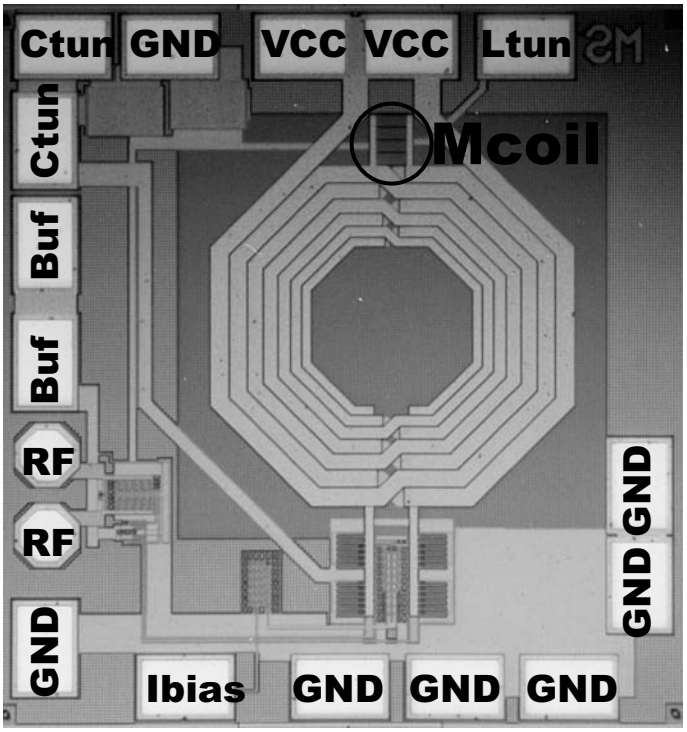

Fig. 12.5. Dual band VCO chip photograph

12.4 Measurements

The chipfoto is shown in Fig. 12.5, die size is 850 μm by 850 μm, coil size is 500 μm by 500 μm.
The capacitive dual-band tuning-characteristic of the VCO is presented in Fig. 12.8, setting the coil tuning *Ltun* at minimum and maximum value. These curves represent a typical dual-band application. The inductive tuning-characteristic of the VCO is presented in Fig. 12.9, setting the varactor tuning *Ctun* at minimum and maximum value. The steep frequency response in this mode limits severely the usability of this continuous inductance tuning.
The upper VCO frequency range of ca. 2 GHz of the VCO clearly exceeds the 1.7 GHz self-resonance of the separately measured nine windings coil from Fig. 12.3 without the inductance tuning. This clearly demonstrates the inductance

decrease and self-resonance increase as discussed in Sect. 12.2. Phase noise is measured with EUROPTEST PN9000 equipment at the respective minimal and maximal frequencies of the capacitive and inductive tuning ranges (Figs. 12.6, 12.7), corresponding to the typical frequency ranges in a dual-band application. The phase noise performance of the coil-tunable VCO is very comparable to the design [73]. This clearly shows that the coil tuning does not deteriorate the Q of the tank. The VCO-measurements are summarized in Table 12.4. The widely used VCO figure of merit of -178 dBc/Hz is very state-of-the-art, especially considering the standard CMOS process with thin metals and low-resistivity substrate used for this design.

Table 12.1. Measurement summary

	Low range	High range
Freq [MHz]	978-1160	1600-2010
Phase noise [dBc/Hz] @3 MHz offset	-138	-132
FOM [dBc/Hz]	-178 (1 GHz)	-177 (2 GHz)
Supply [V]	1.5	1.5
Current [mA]	7.5	9

12.5 Summary

A novel fully integrated voltage controlled inductor is introduced. The proposed structure is used to implement a fully integrated dual-band voltage controlled oscillator with a wide tuning range from 978 to 2010 MHz. A testchip was produced in low-cost 0.25 μm 4 metal standard CMOS process. At 1 GHz center frequency the VCO features a phase noise of -138 dBc/Hz at 3 MHz offset, at 2 GHz a phase noise of -132 dBc/Hz at 3 MHz offset. The frequency tuning above 2 GHz exceeds the self-resonance of the same inductor layout without the newly introduced tunability by 300 MHz. The phase noise and frequency tuning measurements clearly demonstrate that Q and self-resonance of voltage controlled inductor is not affected by its tunability.

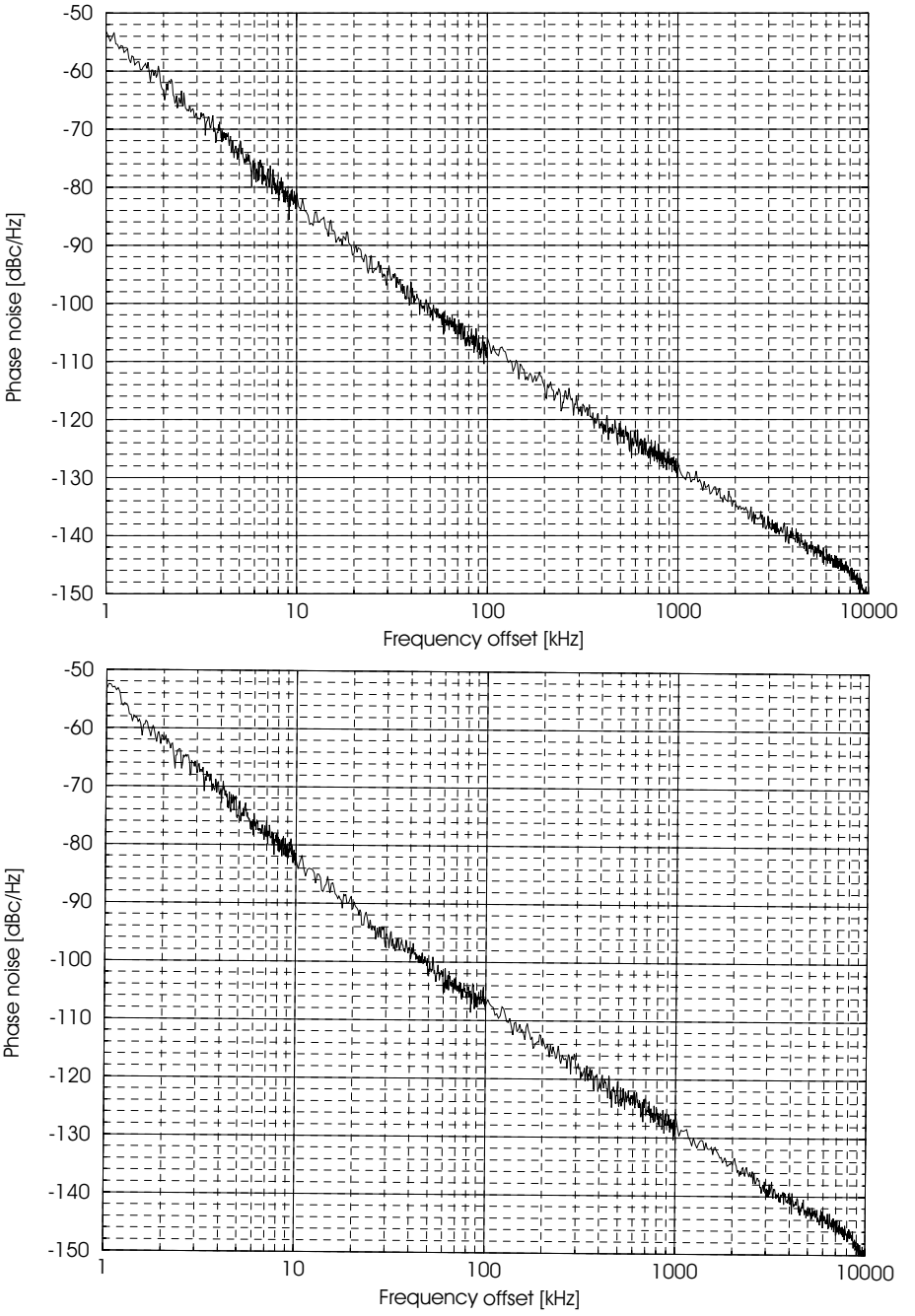

Fig. 12.6. Measured phase noise at 1.5 V power supply, 7.5 mA core current, upper graph: frequency=1 GHz, lower graph frequency=1.16 GHz

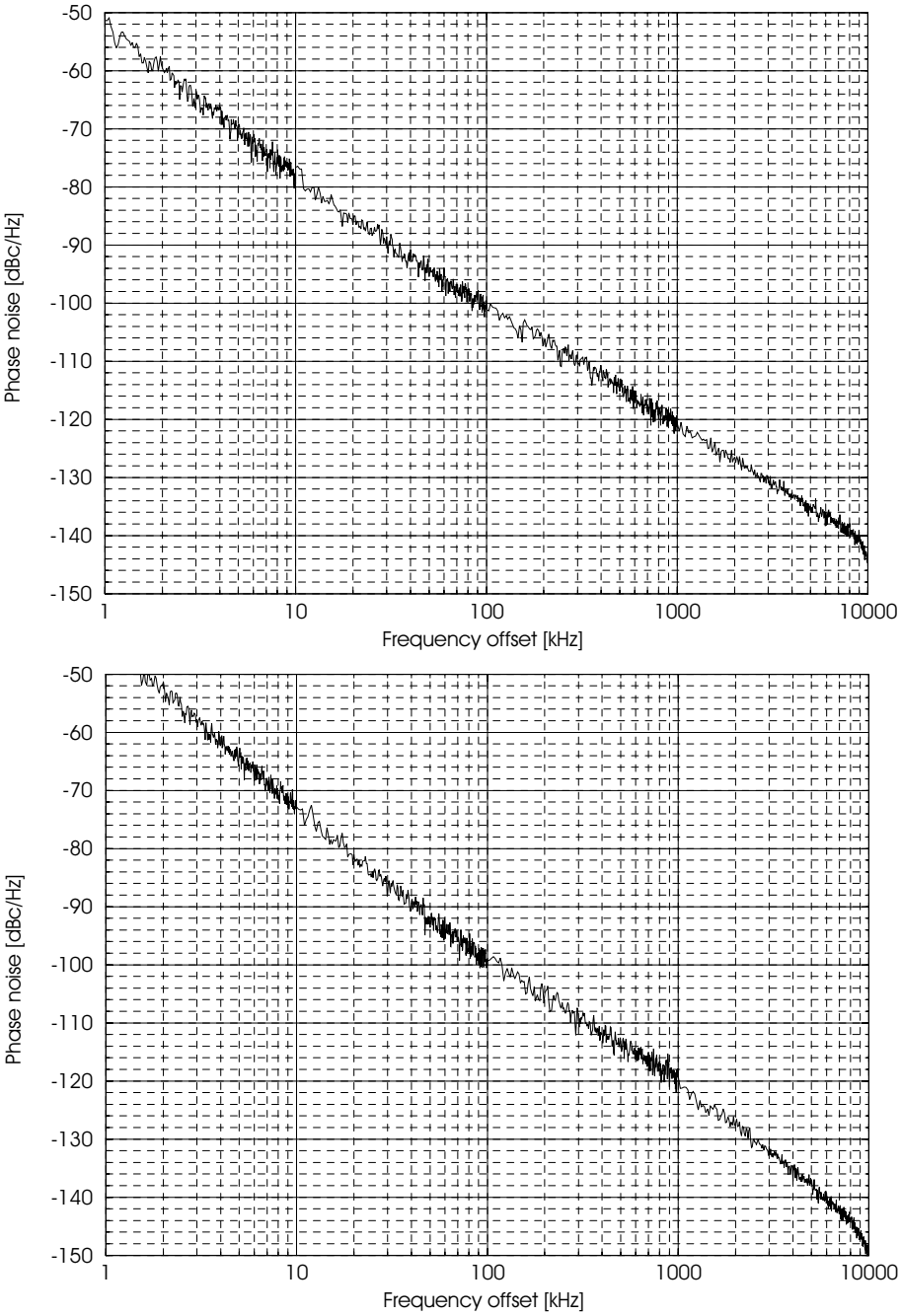

Fig. 12.7. Measured phase noise at 1.5 V power supply, 9 mA core current, upper graph: frequency=1.6 GHz, lower graph frequency=2 GHz

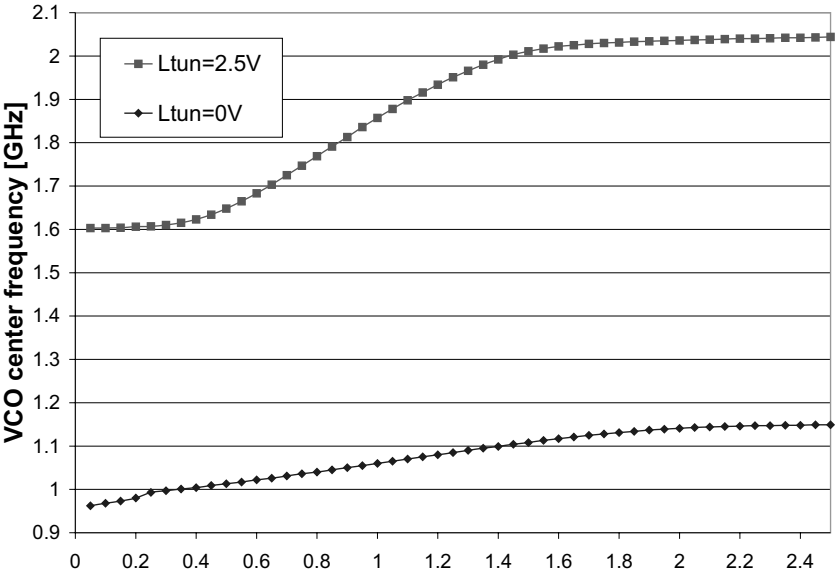

Fig. 12.8. VCO varactor tuning

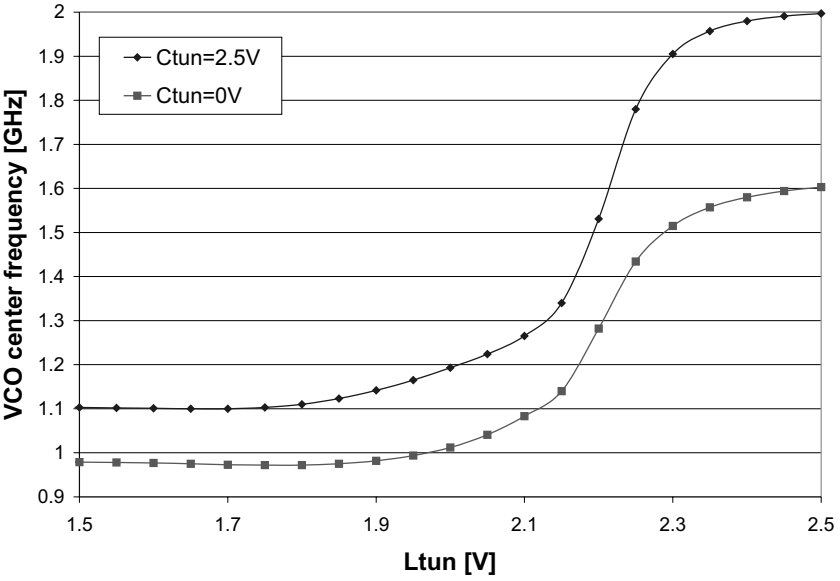

Fig. 12.9. VCO inductor tuning

Part IV

General Conclusion

13

General Conclusion

The tough VCO circuit design problem to combine low phase noise as well as low power consumption was treated in depth. A systematic high inductance approach, using optimized standard CMOS passive devices, is proposed for low power low phase noise fully integrated LC-VCO designs.
The systematic design approach was demonstrated through the integration in standard CMOS of low power low phase noise voltage controlled oscillators for mass market mobile standards like GSM or DCS1800. The presented 1.8 GHz design introduces a novel differential tuning concept and is based on a new VCO-topology without tail current source.
All presented CMOS designs attain or even outperform the performance of external VCO-modules in terms of phase noise and power consumption. Two further designs demonstrate highest frequency operation at 51 GHz combined with lowest power consumption and show how to extend the normally very limited tuning range of LC-VCOs through a tunable coil. The high inductance approach can be further exploited through an optimization of the MOS-varactors [58, 59].
As VCO power consumption is now shown to be of minor concern for SOC-RFCMOS transceivers, further research can be concentrated on other power-hungry building blocks such as prescalers [72], dividers [75], LNAs [77] or output stages [92, 103].

Part V

Appendices

A

List of Symbols

BiCMOS	bipolar and CMOS	
CMOS	complementary MOS	
GSG	ground signal ground	
GSM	globale systeme mobile	
Im	imaginary part	
LDD	lightly doped drain	
LNA	low noise amplifier	
MOS	metal oxide semiconductor	
NQS	non quasi-static	
NMOS	n-type MOS	
PMOS	p-type MOS	
PLL	phase locked loop	
Re	real part	
RF	radio frequency	
STI	shallow trench isolation	
UMTS	universal mobile transmission system	
VCO	voltage controlled oscillator	
C	capacitance	F
C_{av}	averaged capacitance	F
C_F	fringing capacitance, input to output capacitance of inductor	F
C_{max}	maximum varactor capacitance	F
C_{min}	minimum varactor capacitance	F
C_{ox}	gate oxide capacitance	F
C_p	parasitic capacitance	F

Δf	frequency offset	Hz
ϵ_0	permittivity of vacuum	F/m
ϵ_{ox}	dielectric constant of silicon dioxide	1
ϵ_{si}	dielectric constant of silicon	1
f	frequency	Hz
f_c	center frequency	Hz
F	excess noise factor	Hz
f_{res}	resonance frequency	Hz
FOM	VCO figure of merit	dBc/Hz
$\mathcal{L}$	phase noise	dBc/Hz
k	Boltzmann's constant $1.38\,10^{-23}$	J/K
K_{Vdd}	sensitivity of VCO frequency to V_{dd}	Hz/V
K_{VCO}	sensitivity of VCO frequency to V_{tune}	Hz/V
L, L_s	inductance, series inductance	H
μ_0	magnetic permeability of vacuum	Vs/(Am)
P_{loss}	power loss, power dissipation	W
P_{supply}	power supply consumption	W
P_{sig}	signal power	W
q	elementary charge	C
Q	quality factor	1
Q_{BW}	quality factor according to bandwidth definition	1
Q_{tank}	quality factor of LC-tank	1
Q_{min}	minimum quality factor	1
Q_{PS}	quality factor according to phase stability definition	1
R_s	series resistance	Ω
R_{gate},R_g	gate resistance	Ω
R_p	(equivalent) tank parallel resistance	Ω
R_{sub}	substrate resistance	Ω
T	absolute temperature	K
t_{ox}	gate oxide thickness	m
V_{dd}	supply voltage	V
V_{gate}	gate voltage	V
V_{th}	threshold voltage	V
V_{tune}	tuning voltage	V

B

Acknowledgements

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Last but not least, I would like to thank Professor Heinrich Klar for supervising this work.

C

State of The Art VCOs

Table C.1. Performance of some recently published fully integrated CMOS VCOs, FOM as defined in Eqn. (1.12)

VCO	**Tech.** [μm]	**Power** [mW]	Center freq. [GHz]	Tuning range [MHz]	Offset freq. [MHz]	**Phase noise** [dBc/Hz]	**FOM** [dBc/Hz]
[66]	0.13	14.5	10	1600	1	-95	-163.5
[53]	0.7	6	1.8	260	0.6	-116	-177.8
[83]	0.25	24			3		-174.1
[22]	0.8	66	1.24	130	3	-137	-171.1
[18]	0.25	32.4	1.8	460	3	-142	-181.5
[34]	0.25	9.3	1.2	200	3	-152	-196
[84]	0.25	50	1.8	330	3	-140	-180
[16]	1.0	30	0.9	120	0.1	-85	-180
[96]	0.25	7.25	5				-182
[86]	0.25	30	1.57	330	0.6	-132	-187
[39]	0.35	12	1.3	360	0.6	-119	-175
[76]	0.12	3.3	11	1100	1	-104	-180
[76]	0.12	3.3	17	2400	1	-108	-182
Chp. 9	0.25	**14**	1.3	220	3	**-142**	**-182.6**
[60]	0.12	1.5	4	1300	1	-115	-185
Chp. 10	0.25	**20**	1.8	270	3	**-143**	**-185.5**
Chp. 11	0.12	**1**	51	700	1	**-85**	**-179**
Chp. 12	0.25	**11.3**	1	160	3	**-138**	**-178**
Chp. 12	0.25	**13.5**	2	400	3	**-132**	**-177**
[51]	0.35	5	0.9	NONE	1	-138	-190

Table C.2. Performance of some recently published fully integrated Bipolar & BiCMOS or SOI VCOs, FOM as defined in Eqn. (1.12)

VCO	**Tech.**	**Power** [mW]	Center freq. [GHz]	Tuning range [MHz]	Offset freq. [MHz]	**Phase noise** [dBc/Hz]	**FOM** [dBc/Hz]
[61]	Bipolar	45	5.3	1100	2	-108	-160
[82]	0.13 μm SOI	8	5.7	1900	1	-112	-178
[81]	0.13 μm SOI	11.2	40	4000	1	-90	-179
[35]	0.35 μm BiCMOS	9	0.9	200	3	-148.5	-188.5
[34]	0.25 μm BiCMOS	9.3	1.2	200	3	-152	-196
[70]	0.35 μm BiCMOS	11.2	1.7	100	3	-152	-196.5

Table C.3. Performance of some recently published fully integrated quadrature VCOs, sorted by FOM, FOM as defined in Eqn. (1.12)

VCO	**Tech.** [μm]	**Power** [mW]	Center freq. [GHz]	Tuning range [MHz]	Offset freq. [MHz]	**Phase noise** [dBc/Hz]	**FOM** [dBc/Hz]
[61]	Bip	45	5.3	1100	2	-108	-160
[66]	0.13	14.5	10	1600	1	-95	-163.5
[26]	0.18	24	8	250	1	-102	-166
[16]	1.0	30	0.9	120	0.1	-85	-180
[84]	0.25	50	1.8	330	3	-140	-180
[15]	0.18	12	5	1000	1	-118	-181
[95]	0.25	22	5	6000	1	-124	-185
Chp. 10	0.25	**20**	1.8	270	3	**-143**	**-185.5**
[86]	0.25	30	1.57	330	0.6	-132	-187
[51]	0.35	5	0.9	NONE	1	-138	-190

Table C.4. Performance of state of the art VCOs using bond-wires, FOM as defined in Eqn. (1.12)

VCO	**Tech.** [μm]	**Power** [mW]	Center freq. [GHz]	Tuning range [MHz]	Offset freq. [MHz]	**Phase noise** [dBc/Hz]	**FOM** [dBc/Hz]
[52]	0.7	24	1.8	120	0.2	-115	-180
[38]	0.35	2	2.1	600	0.6	-122.5	-189.5
[30]	0.25	0.9	1	180	0.1	-111	-192

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