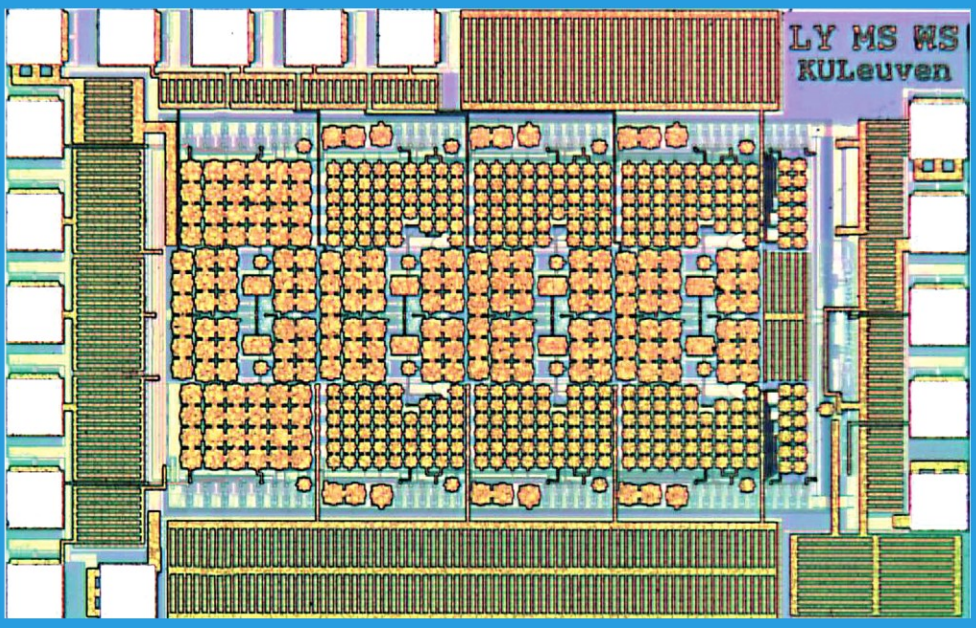
# LOW-POWER LOW-VOLTAGE SIGMA-DELTA MODULATORS IN NANOMETER CMOS

Libin Yao, Michiel Steyaert
and Willy Sansen

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# LOW-POWER LOW-VOLTAGE SIGMA-DELTA MODULATORS IN NANOMETER CMOS

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# Abstract

The evolution of the CMOS technology brings many challenges to analog designers. The scaling-down of the transistor feature size has a big impact on analog circuit design, because it considerably degrades the performance of an analog circuit. As an interface between the analog circuit and the digital circuit, the ADC is moving into nanometer CMOS technologies due to the advantages for the digital circuit. Consequently, the reduced supply voltage and the degraded device characteristic are inevitable problems in ADC design. Many efforts have been devoted to cope with these problems to make an ADC design in nanometer CMOS technologies. In this text, the circuit level approach and the system level approach are presented for low-power low-voltage $\Sigma$-$\Delta$ ADC design in nanometer CMOS technologies.

At the circuit level, specially designed circuit building blocks suitable for nanometer CMOS technologies are introduced. At the same time, low-power consumption is also addressed. Following a low-power low-voltage operational amplifier design, a low-power low-voltage $\Sigma$-$\Delta$ modulator design is presented in a 90-nm CMOS technology. The total power consumption is 140 $\mu$W under a 1.0-V power supply voltage. The modulator reaches a peak SNR of 85 dB and a dynamic range of 88 dB in a 20-kHz signal bandwidth. This design is the first $\Sigma$-$\Delta$ modulator design in a 90-nm CMOS technology and reaches a very high figure-of-merit. This design demonstrates the feasibility of designing high-performance $\Sigma$-$\Delta$ ADCs in nanometer CMOS technologies.

At the system level, a full-feedforward $\Sigma$-$\Delta$ topology suitable for the $\Sigma$-$\Delta$ ADC design in nanometer CMOS technologies is introduced. The most important feature of this topology is that the signal transfer function is unity, which is fairly independent of the building block characteristics. With careful signal scaling, signal swings inside the loop filter can be largely suppressed, which is highly desirable for low-voltage designs. A detailed analysis is presented in this text, leading to optimized loop coefficients. Behavioral simulations reveal that requirements for building blocks are quite relaxed in this topology. Implemented in a 130-nm CMOS technology, the proposed fourth-order full-feedforward $\Sigma$-$\Delta$ modulator reaches a 88-dB DR with a power dissipation of 7.4 mW in a 500-kHz signal bandwidth under a 1.0-V power supply voltage. This design is the first design using the full feedforward $\Sigma$-$\Delta$ topology and reaches the highest conversion speed among all the 1-V $\Sigma$-$\Delta$ modulators to date. This design proves that the proposed full-feedforward $\Sigma$-$\Delta$ topology is an excellent topology for low-power low-voltage $\Sigma$-$\Delta$ ADC designs in nanometer CMOS technologies.

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## Symbols

### Physical

| | |
|---|---|
| k | Boltzmann's constant ($1.38 \times 10^{-23}[J/K]$) |
| q | Electron charge ($1.60 \times 10^{-19}[C]$) |
| T | Absolute temperature |

### Definitions

| | |
|---|---|
| $\Delta$ | Quantization step size |
| $\gamma$ | Excess noise factor |
| $\omega_n$ | Natural frequency |
| $\zeta$ | Damping factor |
| $A$ | Gain of the OTA |
| $A_0$ | Nominal OTA gain |
| $A_{VT}$ | transistor threshold voltage mismatch factor |
| $B$ | Number of bits of the quantizer |
| $C_I$ | Integration capacitance |
| $C_L$ | Load capacitance |
| $C_S$ | Sampling capacitance |
| $f_s$ | Sampling frequency |
| $f_T$ | Cutoff frequency |
| $g_{DS}$ | Output conductance of a MOS transistor |
| $g_m$ | Transconductance |
| $H$ | Loop filter of a $\Sigma$-$\Delta$ modulator |
| $H_e$ | Noise transfer function of a $\Sigma$-$\Delta$ modulator |
| $H_x$ | Signal transfer function of a $\Sigma$-$\Delta$ modulator |

| | |
|---|---|
| $k$ | Quantizer gain |
| $L$ | Channel length of a MOS transistor |
| $P$ | Power consumption |
| $t_{ox}$ | Gate oxide thickness of a MOS transistor |
| $V_{GS}$ | Gate-source voltage of a MOS transistor |
| $V_{ref}$ | Reference voltage of an ADC |
| $V_T$ | Threshold voltage of a MOS transistor |
| $W$ | Channel width of a transistor |

## Abbreviations

| | |
|---|---|
| ADC | Analog to Digital Converter |
| CMFB | Common-Mode Feedback |
| CLK | Clock Signal of a $\Sigma$-$\Delta$ ADC |
| CMOS | Complimentary Metal Oxide Semiconductor |
| DAC | Digital to Analog Converter |
| DC | Direct Current |
| DEM | Dynamic Element Matching |
| DR | Dynamic Range |
| DWA | Data Weighted Averaging |
| FFT | Fast Fourier Transform |
| FOM | Figure of Merit |
| GBW | Gain Bandwidth production |
| IC | Integrated Circuit |
| ISSCC | International Solid-State Circuits Conference |
| LSB | Least Significant Bit |
| MIM | Metal Insulator Metal |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| MSB | Most Significant Bit |
| NAND | Not AND |
| NMOS | n-channel MOSFET |

| | |
|---|---|
| OL | Overload Level |
| OSR | Over Sampling Ratio |
| OTA | Operational Transconductance Amplifier |
| PMOS | p-channel MOSFET |
| PSRR | Power Supply Rejection Ratio |
| ROM | Read Only Memory |
| SC | Switched Capacitor |
| SNDR | Signal to Noise plus Distortion Ratio |
| SNR | Signal to Noise Ratio |
| SR | Slew Rate |

# Chapter 1

# Introduction

## 1.1 Motivation

Driven by the speed demand of digital circuits, the CMOS technology is continuously scaling-down. In recent years the deep-submicron CMOS technology is pacing into the 100-nano meter range. As a consequence, the power supply voltage drops below one Volt earlier than expected. On the other hand, portable electronics with low-voltage operation find big markets. All these factors have made the low-voltage circuit design a hot topic recently. The low supply voltage constraint makes the analog design challenging due to the reduced signal swing. On the other hand, the scaling-down of the CMOS technology results into the degradation of the device characteristics, making the analog IC design in nanometer CMOS technologies more challenging.

As a major building block, the ADC is widely used in mixed-signal circuits. Being an interface between the analog world to the digital circuit, the ADC is implemented with the same technology as the digital circuit. As a result, the reduction of the power supply voltage of the ADC is inevitable. The decrease of the supply voltage obviously results into a performance degradation of the ADC. Generally speaking, to maintain the same dynamic range in a system, the noise floor should be lowered while the signal swing is reduced. Moreover the distortion problem tends to be more severe with the reduction of the supply voltage reduction.

Among different ADCs, the $\Sigma$-$\Delta$ ADC is most suitable for high-resolution applications due to its high linearity feature. The high linearity of the $\Sigma$-$\Delta$ ADC is obtained by using the intrinsically linear single-bit quantizer and the oversampling technique. However, the non-ideality in the building block strongly affects the performance of the $\Sigma$-$\Delta$ ADC. To design a high-performance $\Sigma$-$\Delta$ ADC, most efforts are spent fighting the non-ideality of the building block. The movement into nanometer CMOS technologies makes the situation even worse. The reduced supply voltage limits the operation headroom for the active devices, resulting into difficulties in designing building blocks [San98]. On the other hand, a lower noise-floor is required for the same dynamic range of a ADC, which costs power and comprises the performance. Generally speaking, low-voltage operation does not necessarily result into low-power consumption for a $\Sigma$-$\Delta$ ADC. For the high-resolution $\Sigma$-$\Delta$ ADC, one of the most important parameters is the linearity of the converter. The degraded device characteristic and reduced supply voltage make the distortion problem even worse [Lee85]. To solve these problems, many efforts have been made at both the circuit level and at the system level with a lot of trade-offs and compromises.

To build a whole system on a single chip, the Σ-Δ ADC is preferred to be integrated with the digital circuit on the same chip. Therefore, the implementation of the low-voltage Σ-Δ ADCs in nanometer CMOS technologies is strongly required. In many cases, the power consumption of the Σ-Δ ADC is restricted. As a result, the low-power low-voltage Σ-Δ ADC design is highly desirable in a system. It is thus more than meaningful to investigate the low-power low-voltage Σ-Δ ADC design in nanometer CMOS technologies.

## 1.2 Outline of the Work

This work is devoted to exploration of low-power low-voltage Σ-Δ ADC design in nanometer CMOS technologies. The outline of the work is as follows:

Chapter 2 presents the evolution of the CMOS technologies and its impact to the analog circuit design, and more specifically, to the ADC design. Different design difficulties are addressed and potential solutions are suggested in this chapter.

Chapter 3 presents the basic principle of the ADC. Then the operation principle of the Σ-Δ ADC is introduced. The traditional single-loop and the cascaded Σ-Δ ADC are introduced. Optimized loop coefficients of the traditional single-loop and the cascaded Σ-Δ ADC are presented as well.

Chapter 4 presents the circuit level approach of the low-power low-voltage Σ-Δ ADC design in nanometer CMOS technologies. The low-voltage low-power OTA design is introduced firstly. A gain-enhanced current mirror OTA with high power-efficiency is described. It is meaningful to explore the possibility of implementing high performance Σ-Δ modulators in a standard digital process in nanometer technologies. In this chapter, a single-loop third-order switched-capacitor Σ-Δ modulator implemented in a standard digital 90-nm CMOS technology is demonstrated. Finally extensive measurements on the power-supply-rejection-ratio and the low-frequency noise are performed and the measurement results are interpreted.

Chapter 5 presents the system level approach of the low-power low-voltage Σ-Δ ADC design in nanometer CMOS technologies. Circuit level problems can often easily be solved at the system level. In the first section of this chapter, the full feedforward Σ-Δ ADC is introduced. The features associated with this topology are analyzed. Optimized loop coefficients for different full feedforward Σ-Δ ADCs obtained from the behavioral simulation are presented in this chapter. By introducing the novel full feedforward Σ-Δ modulator topology, several drawbacks of the traditional Σ-Δ modulators are overcome. Then the linearity of the full feedforward Σ-Δ modulator is analyzed. The circuit implementation of the full feedforward Σ-Δ modulator is introduced. Two design examples in a 180-nm and a 130-nm CMOS technologies are presented. Comparisons to the state-of-the-art works are also provided to more clearly evaluate the proposed design. Finally, a multibit full feedforward Σ-Δ modulator design is proposed.

Finally some general conclusions are drawn in the last chapter.

Chapter 2

# ADCs in Nanometer CMOS Technologies

## 2.1 Introduction

Nowadays most ICs are fabricated in nanometer CMOS technologies. This chapter addresses the trend of nanometer CMOS technologies and its impact to analog IC designs, especially for ADC designs.

Many of the analog designs during the 1960s and 1970s were done in bipolar and hybrid technologies. During the 1980s, the MOS analog designs gained with rapid evolution. The CMOS technology gained popularity in modern integrated circuits industry. In this technology, both the n-type MOSFET and p-type MOSFET are fabricated in the same wafer and it is easy to make logic gates in this technology. Soon it has become clear that the dimensions of the CMOS devices could be scaled-down more easily than other technologies. Thus in the same chip area, more devices can be fabricated and the cost of the IC decreases rapidly. According to the statistical data, more than 90% of the IC market is taken by the CMOS technologies. The CMOS technology is becoming the cheapest technology and it is suitable for mass production. It is thus worth to investigate the CMOS technology and its evolving trend.

In this chapter, the scaling-down of the CMOS technology is introduced. Then the impact of the CMOS scaling-down to analog circuits, particularly to ADCs, is analyzed.

## 2.2 Scaling-Down of CMOS Technologies

For more than three decades, the CMOS technology has been evolving continuously. The most important evolution is the scaling-down of the CMOS technology. The scaling-down of CMOS technologies is the geometry dimension reduction of the device and interconnection. By scaling-down, more devices can be fabricated into the same chip area and hence the cost is reduced. As a result, the CMOS technology dominates the IC market. The number of transistors per square inch on integrated circuits had doubled every 18 months since the integrated circuit was invented [Moo65]. This is so-called Moore's Law. Most experts, including Moore himself, expect Moore's Law to hold for at least another one decade from now.

The dimensions of the device scale as the constant field scaling. The supply voltage, Vdd, scales to have reasonable electric fields in the device. The doping levels are adjusted to have the correct depletion region widths. To limit the sub-threshold currents, the transistor threshold voltage, $V_T$, scales more slowly than the supply voltage.

Table 2.1: The technology history of the Intel processors.

| Processor Name | Year | Technology | Clock frequency | Transistors |
|---|---|---|---|---|
| 4004 | 1971 | 10 $\mu$m | 108 kHz | 2,250 |
| 8008 | 1972 | 10 $\mu$m | 500 kHz | 2,500 |
| 8080 | 1974 | 6 $\mu$m | 2 MHz | 5,000 |
| 8086 | 1978 | 3 $\mu$m | 10 MHz | 29,000 |
| 286 | 1982 | 1.5 $\mu$m | 12 MHz | 120,000 |
| Intel386 | 1985 | 1 $\mu$m | 33 MHz | 275,000 |
| Intel486 | 1989 | 0.6 $\mu$m | 100 MHz | 1,180,000 |
| Intel Pentium | 1993 | 0.35 $\mu$m | 233 MHz | 3,100,000 |
| Intel Pentium II | 1997 | 0.15 $\mu$m | 450 MHz | 7,500,000 |
| Intel Pentium III | 1999 | 0.18 $\mu$m | 1 GHz | 24,000,000 |
| Intel Pentium 4 | 2000 | 0.13 $\mu$m | 3.6 GHz | 42,000,000 |
| Intel Itanium | 2002 | 0.13 $\mu$m | 1 GHz | 220,000,000 |
| Intel Itanium 2 | 2003 | 0.13 $\mu$m | 1.6 GHz | 410,000,000 |

### 2.2.1 Driving Force of the CMOS Scaling-Down

To integrate more devices into a single chip, the device geometrical dimension must be reduced. Table. 2.1 shows the transistor numbers, minimum transistor channel length and the operation frequency of different Intel processors. The minimum transistor channel length is also called the feature size of the technology. From the 1-$\mu$m CMOS technology to the current 90-nm CMOS technology, the feature size of the transistor has been scaled-down by a factor of 10, while the device density has been increased by a factor of 100. More and more devices and function blocks are integrated into one single chip and the production cost of the system is greatly reduced.

Another driving force for the CMOS scaling-down is the speed and power demands of the digital circuits. For CMOS digital circuits, i.e. logic gates, the operating speed is solely determined by the load capacitance the logic gate sees. The load capacitance is composed by the input capacitance of the next stage and the parasitic capacitance of the interconnection. An intuitive consideration is that all these capacitances are proportional to the geometry size of the devices and the interconnections. Thus the reduction of the geometry sizes is the main way to decrease the parasitic capacitance, hence increases the speed and reduces the power consumption of the circuit. For a CMOS logic gate, e.g. an inverter, the most simple logic gate, the static and dynamic power consumption can be expressed as:

$$P_{static} = Vdd \cdot I_{leakage} \tag{2.1}$$

$$P_{dynamic} = C_L \cdot Vdd^2 \cdot f. \tag{2.2}$$

In this equation $Vdd$ is the supply voltage of the circuit, and $I_{leakage}$ is the leakage current of the inverter. $C_L$ represents the load capacitance of the inverter and $f$ is

the operating frequency of the inverter. The scaling-down of CMOS technology helps reducing the load capacitance of the logic gate. The reduction of the supply voltage is beneficial both in reducing the static and dynamic power consumption of the CMOS logic circuits. As a result, the dynamic power, the main power consumption of CMOS digital circuits, is greatly reduced by the CMOS scaling-down.

In short, the scaling-down of the CMOS technology improves the chip density, reduces the power consumption of the digital circuit and increases the operating speed. The production cost is also reduced since the scaling-down of the CMOS technology. Since the main stream of the CMOS IC market is the digital circuits, the evolving direction is in favor of the digital circuits. That is the driving force of the CMOS scaling-down.

### 2.2.2 Moving into Nanometer CMOS Technologies

For most digital ICs, currently the most popular technology is 130 nm or 90 nm, i.e. nanometer CMOS technologies. The system on chip trend has caused that the analog and mixed-signal ICs are fabricated with the digital ICs on the same wafer. That eventually requires the analog and mixed-signal ICs are fabricated in nanometer CMOS technologies to save cost. It is seen that the analog and mixed-signal ICs have moved into nanometer CMOS technologies. A lot of discussions have arisen that the analog ICs must separate from the digital ICs. However, the cost reason has pushed analog designers to get used to the digital technology and more and more analog IC designs in nanometer CMOS technologies have been published.

From the publications on the International Solid-State Circuits Conference (ISSCC) recent years one can see the trends of the analog ICs moving into nanometer CMOS technologies. Table 2.2 shows the high-performance logic technology roadmap, 2004 edition from the Semiconductor Industry Association(SIA).

Table 2.2: The high-performance logic technology roadmap 2004 edition.

| Year | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 |
|---|---|---|---|---|---|---|---|
| Feature size($nm$) | 100 | 90 | 80 | 70 | 65 | 57 | 50 |
| Supply Voltage($V$) | 1.2 | 1.2 | 1.1 | 1.1 | 1.1 | 1.0 | 1.0 |
| Threshold Voltage($V$) | 0.21 | 0.20 | 0.20 | 0.21 | 0.18 | 0.17 | 0.16 |
| Device Density($M/cm^2$) | 61 | 77 | 97 | 122 | 154 | 194 | 245 |

In 2004, the 90-nm CMOS technology has already been in mass production for digital circuits. However, for analog circuits, there is still a big time lag between digital circuits. The reason is that the analog circuit gains little from the CMOS scaling-down. Instead, several big challenges are encountered in the scaling-down of the CMOS technologies for analog designs. In the following sections the impact of the CMOS scaling-down to analog designs will be discussed in detail.

## 2.3 Impact of Moving into Nanometer CMOS to Analog Circuits

The first impression for analog designers of moving into nanometer CMOS technologies is that faster and more effective devices can be available. The transconductance from a single transistor in strong inversion region is:

$$g_m = \sqrt{2\mu C_{ox} \cdot \frac{W}{L} \cdot I_D}. \tag{2.3}$$

For a certain drain current, more transconductance can be obtained from the transistor that has higher gate oxide capacitance or has shorter channel length. It seems great beneficial to move into nanometer CMOS technologies for analog designs. However, several problems arisen and a lot of efforts have been devoted to solve these problems.

When moving to nanometer CMOS design, the analog designer faces a number of challenges. The maximum field strength inside the device and hot carrier reliability concerns limit the supply voltage of the circuit. At the same time, the threshold voltage $V_T$ of the transistor cannot be decreased due to off-state power constraints. Consequently, the analog designer is faced with a decrease in the available window for voltage swing above the overdrive voltage, $V_{GS} - V_T$. In addition, in the nanometer region the long-channel proportionality becomes less favorable, reaching a short-channel limit. These two factors reduce the voltage-controlled sensitivity that the designer can manipulate over the transistor.

On the other hand, in nanometer CMOS devices, the device characteristics become more sensitive to variations in the channel length, greatly complicating basic design tasks, as well as magnifying the effects of process variations and device mismatch. This is an undesirable and uncontrollable sensitivity. Note that the desirable sensitivity decreases while the undesirable sensitivity increases. Furthermore, nanometer CMOS device behavior is very difficult to model accurately; analytical descriptions used for circuit simulation will inevitably introduce further errors into the design. In addition, the extreme complexity of present-day analytical MOSFET descriptions that are employed for circuit simulation precludes their use in conventional analog design practice. These issues must be addressed in the development of future analytical MOSFET descriptions for circuit simulation.

### 2.3.1 Decreased Supply Voltage

The CMOS scaling-down is accompanied by the reduction of the voltage on the transistor to avoid the transistor breakdown. It is essential to maintain the electric field constant inside the transistor. These constraints restrict the voltage on the transistor and result into reduction of the supply voltage of the circuits, as can be seen in Table. 2.2. Fig. 2.1 shows the supply voltage and the threshold voltage evolution of different generations of CMOS technologies. The decreased supply voltage is the first challenge analog designers faced while moving into nanometer CMOS technologies. The direct impact to analog circuits is the reduction of the signal swing inside the circuits. For

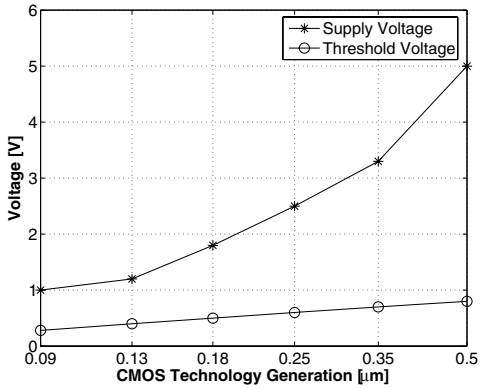



Figure 2.1: The supply voltage and transistor threshold voltage of different generations of CMOS technologies.

analog circuits, the signal swing is very important as it defines the dynamic range of the circuit.

Another problem associated with the reduced supply voltage is the limited use of the cascode configuration of the transistor, shown in Fig. 2.2. There are 5 transistors vertically cascoded in this telescopic cascode OTA. For each transistors biased at strong inversion region, there is a minimum $V_{DS}$, which equals the overdrive voltage, $V_{GS}-V_T$, of the transistor, required to stay in the saturation region. For all 5 transistors, there is a considerable voltage drop and the output swing is small. This is not tolerable if the supply voltage is limited. Consequently, the use of cascode transistors is limited in nanometer CMOS technologies. The cascode transistor is widely used in analog circuits for its high output impedance, hence a high voltage gain can be obtained. However, the reduced supply voltage makes transistor cascoding difficult. Instead, transistor cascading is more preferred in a low-voltage environment.

### 2.3.2 Impact on Transistor Intrinsic Gain

Fig. 2.3 shows the MOS transistor symbol, the actual layout and the basic gain stage of a MOS transistor. The intrinsic gain of a MOS transistor is defined as:

$$A_{intrinsic} = \frac{g_m}{g_{DS}}. \tag{2.4}$$

where $g_m$ and $g_{DS}$ are the transconductance and output conductance of the active MOS transistor, respectively. The intrinsic gain is the maximum gain a transistor can reach. It is the amplification ability of a MOS transistor. From (2.4) it can be seen that due to the channel length modulation effect, the output impedance is decreased with the channel length reduction. The intrinsic gain of a transistor is also reduced. Fig. 2.4 shows the transistor intrinsic gain and $f_T$ curve vs. channel length. It can be seen that

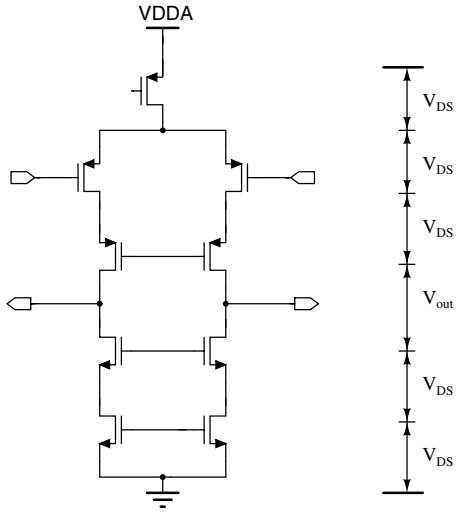



Figure 2.2: The schematic of a telescopic cascode OTA.

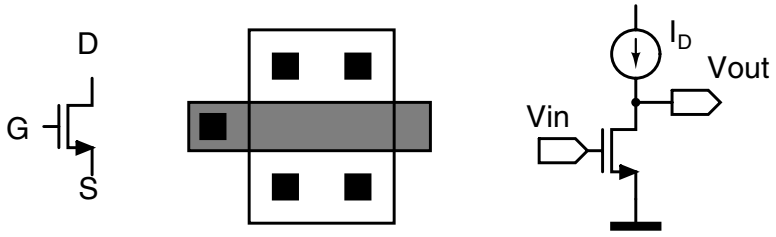



Figure 2.3: The MOS transistor symbol, the layout and the basic schematic of the MOS transistor gain stage.

if the transistor channel length is increased, then the $f_T$ decreases rapidly. A gain-speed trade-off must be made here. For analog circuits, the gain is the most important specification for an active device. To avoid the reduction of the transistor gain, the longer transistor channel length is normally used in amplifiers. Transistor cascading, i.e. multi-stage gain stages, is normally adopted in nanometer CMOS designs to obtain the required gain. However, frequency compensation is normally needed in this situation, which consumes more power and renders the circuit more complicated.

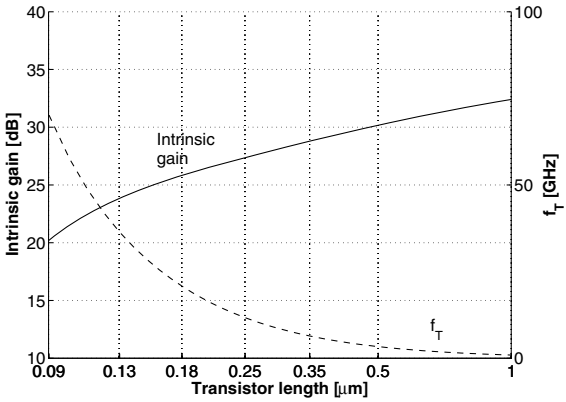



Figure 2.4: The transistor intrinsic gain and $f_T$ vs. channel length curves with $V_{GS}-V_T = 0.2\ V$ and $V_{DS} = 0.3\ V$ in a nanometer CMOS technology.

It is worth to mention that due to the tighter control from the gate, the body-effect of the transistor is reduced with the CMOS scaling-down, which is beneficial for analog designs. In analog designs, the minimum transistor size is always avoided for reasons of the lower intrinsic gain and poorer matching properties of the transistor. Although the speed of the transistor is compromised.

### 2.3.3 Impact on Device Matching

Matching of devices often dominates the analog circuit performance, as the precision of the circuit is often assigned by the matching of devices. For example, the yield of the Flash ADC is defined by offsets of the comparators. The offset is defined by the matching of the transistors. The matching performance of a certain transistor parameter P is, to first order, expressed in terms of the matching coefficient $A(P)$:

$$\sigma(P) = \frac{A(P)}{\sqrt{W \cdot L}} + P_0. \tag{2.5}$$

where $\sigma(P)$ is the standard deviation of a transistor parameter $P$. $A(P)$ is a matching coefficient related to the process and the $P_0$ is a fixed component. The matching coefficient $A(P)$ is determined by the contribution of all possible sources of transistor

variations, such as dopant fluctuations, variations in fixed charges at the silicon/oxide interface, surface roughness, etc. For MOS transistors, the most important matching parameters are the threshold voltage $V_T$ and the current factor $K$ [Lak86]. The scaling-down of the MOS transistor makes the channel better controlled due to the thinner gate oxide thickness. As a result, the technology having thinner gate oxide thickness shows better matching properties [Pel89], [Miz94]. Fig. 2.5 shows the relationship between

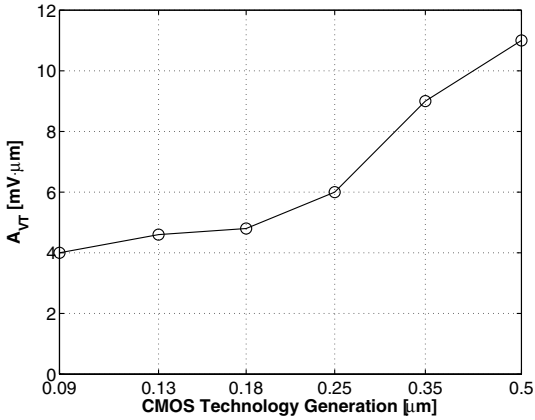



Figure 2.5: The transistor threshold voltage matching constant $A_{VT}$ of different CMOS technology generations.

the transistor threshold voltage matching constant $A_{VT}$, taken from foundry data, and different CMOS technology generations. The trend shows that the transistor threshold voltage matching constant $A_{VT}$ decreases with the scaling-down of the CMOS technologies. Equation 2.6 shows the relation between the matching constant of the transistor threshold voltage and the transistor gate oxide thickness [Bas98].

$$A_{V_T} = \frac{q \cdot t_{ox}}{\sqrt{2}\epsilon_{ox}} \sqrt{D_t} \tag{2.6}$$

where $D_t$ is the total implant dose and $t_{ox}$ is the gate oxide thickness. It is seen that the scaling-down of the CMOS technologies improves the matching properties of the transistor. It is good for analog circuits. Benefiting from the improved matching properties, circuits like Flash ADCs and current steering DACs whose performance strongly depends on the device matching properties obtain better results moving into nanometer CMOS technologies.

### 2.3.4 Impact on Device Noise

With the transistor channel length reduction, there are more side effects. Another problem with nanometer technologies is the channel noise increase while the channel length

is shrunk [Che02]. For a transistor, the power spectrum density of the thermal noise can be expressed as:

$$S_{id^2} = \gamma \cdot 4kTg_m \tag{2.7}$$

where the coefficient $\gamma$ is dependent on the technology. For long channel transistors, the coefficient $\gamma$ is 2/3. However, it will increase when the channel length is reduced, which means that in nanometer technologies, the transistor channel noise is higher than that of long channel transistors. Especially when the signal swing is reduced, the increase of the noise reduces the dynamic range of the analog circuits. So in the design of high dynamic range analog circuits, the device noise should be carefully considered. Further more, the $1/f$ noise is often not well modeled in nanometer technologies, making the design of high dynamic range analog circuits more difficult.

## 2.4 ADCs in Nanometer CMOS

As a major building block, the ADC is widely used in mixed-signal designs. As an interface between the analog world to the digital world, ADCs are implemented with the same technology as the digital circuit. Hence the power supply voltage reduction is inevitable. Fig. 2.6 shows the Nyquist ADC paper numbers published in ISSCC and the CMOS technologies used in recent years. It is clearly seen that most of the ADC designs are made in nanometer CMOS technologies. The decrease of the supply voltage obviously results into analog circuit performance degradation. Generally speaking, to maintain the same dynamic range on a system, the noise floor should be lowered while the signal swing is reduced. The cost of lowering the noise floor is increased power consumption.

In this section, ADC design difficulties of moving into nanometer technologies are addressed firstly. Among different ADCs, $\Sigma$-$\Delta$ ADCs are most suitable for high-resolution applications due to their high-linearity. The high linearity is achieved by using the intrinsically linear 1-bit quantizer and oversampling technique. These features makes the $\Sigma$-$\Delta$ ADCs suitable for high-resolution analog to digital conversion with neither stringent device matching requirement, nor trimming and calibration. However, the non-idealities in the building blocks strongly affect the ADC performance. The scaling-down of the CMOS technology makes these non-idealities more severe. To design a $\Sigma$-$\Delta$ ADC, main efforts are put on fighting with the non-idealities of building blocks. The reduced supply voltage makes these constraints even tighter. Among them, the most important one is the distortion problem in high-resolution $\Sigma$-$\Delta$ ADCs. Thus the high-resolution ADC design in nanometer CMOS technologies is getting more attention nowadays, as shown in Fig. 2.7, which is the $\Sigma$-$\Delta$ ADC paper numbers published in ISSCC and the CMOS technologies used in recent years. It is seen that most $\Sigma$-$\Delta$ ADC designs are moved into nanometer CMOS technologies recently. In the following sections the impact of moving into nanometer technologies on the ADC design is analyzed in detail.

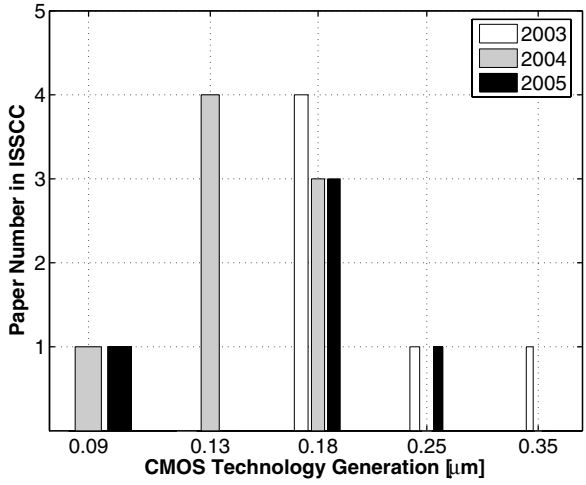



Figure 2.6: The Nyquist ADC paper numbers published in recent ISSCC and the CMOS technologies used.

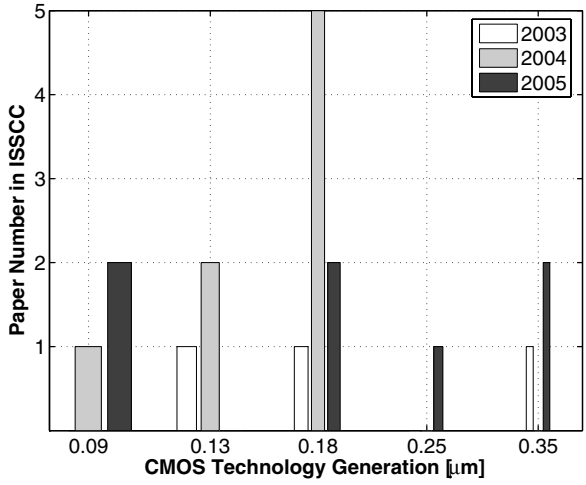



Figure 2.7: The $\Sigma$-$\Delta$ ADC paper numbers published in recent ISSCC and the CMOS technologies used.

### 2.4.1 Decreased Signal Swing

The signal swing defines the dynamic range for a system with a certain noise floor. In order to increase the dynamic range of a system, the signal swing should be maximized and the noise floor should be minimized. Unfortunately, the movement into nanometer technologies brings a restriction on the supply voltage, which leads to small signal swing of the system. For example, a thermal noise limited Σ-Δ ADC, the dynamic range can be expressed as:

$$DR = 10\,log\frac{P_s}{P_n} = 10\,log\frac{{V_{in\,max}}^2}{2P_n} \tag{2.8}$$

And the maximum input signal amplitude, $V_{in\,max}$, can be expressed as:

$$V_{in\,max} = V_{ref} \cdot OL \tag{2.9}$$

where $P_n$ is the input referred noise power, $V_{ref}$ and $OL$ is the reference voltage and overload level respectively. The overload level is the normalized input amplitude while the SNR decreases from the peak SNR by 6 dB. For a certain Σ-Δ ADC topology, the overload level, which is relative to the reference voltage, is approximately fixed. One can only increase the reference voltage to increase the maximum input signal amplitude. The reference voltage is limited by the output swing of the integrators, which is limited by the OTA output swing, and finally limited by the supply voltage. So the lower supply voltage poses difficulties to high dynamic range Σ-Δ ADC designs. Either the maximum input signal has to be increased or the noise floor has to be decreased to maintain the same dynamic range.

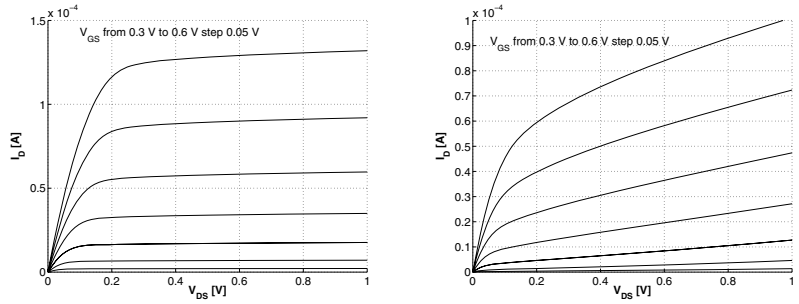
### 2.4.2 Degraded Transistor Characteristics

The transistor characteristics change with the channel length shrinking. Fig. 2.8 gives the transistor $I_D - V_{DS}$ characteristics for transistors with different channel length in the same nanometer CMOS technology.

Due to the channel length modulation, the drain-source resistance, $R_{DS}$, of a MOS transistor decreases along with the reduction of the channel length. The intrinsic gain, defined in equation (2.10), is the amplification ability of a single transistor.

$$A_{intrinsic} = \frac{g_m}{g_{DS}} = \frac{2 \cdot I_D}{V_{GS} - V_T} \cdot \frac{1}{I_D \cdot \lambda} = \frac{2}{(V_{GS} - V_T)\lambda} = \frac{2V_E \cdot L}{V_{GS} - V_T} \tag{2.10}$$

where $V_E$ is the Early voltage of the transistor. For a short channel length transistor, the intrinsic gain decreases along with the transistor channel length reduction. For example, the intrinsic gain of a transistor in a 90-nm CMOS technology with minimum channel length is less than 20 dB. The usual way to increase the output resistance, the use of a cascode, can't be used in the low-voltage environment due to the limited output swing. Thus cascading more transistors to achieve a certain gain is inevitable in nanometer technologies. However the cascading of multi-stages needs frequency compensation, which costs power and degrades the speed.




(a) Transistor $I_D - V_{DS}$ characteristics with W/L=8 $\mu$m/0.8 $\mu$m.

(b) Transistor $I_D - V_{DS}$ characteristics with W/L=0.8 $\mu$m/0.08 $\mu$m.

Figure 2.8: Transistor characteristics with different channel length in a nanometer CMOS technology.

### 2.4.3 Distortion

One of the main sources of the distortion on $\Sigma$-$\Delta$ modulators is the amplifier. In a low-voltage environment, designers are struggling to squeeze the most usable signal swing from the supply voltage. As a result, transistors are forced to work at a relatively larger output swing, especially the output devices. From Fig. 2.8 it is seen that for nanometer CMOS technologies, the drain-source resistance, $R_{DS}$ of a transistor, has a strong dependence on the source-drain voltage. The drastically changed source-drain voltage results in a big variation on the output conductance of the transistor, generating more distortion. This is inevitable for low-voltage designs, unless the signal swing can be reduced. However, the reduced signal swing requires a lower noise floor, which costs power consumption. The best solution is at the system level, i.e. reduce the output swing of the integrators [Sil01].

Another source of the distortion is the input voltage dependent on-resistance of the switch. The main way to solve this problem is making a constant on-resistance of the switch, which means a constant overdrive voltage for switch transistors. In low-voltage environment, normally clock boosting circuits are needed to do so [Abo99].

### 2.4.4 Switch Driving

Switched-capacitor circuits are widely used in analog signal processing circuits. In switched-capacitor circuits, the implementation of the switch is usually done by MOS transistors. To reduce the signal-dependent on-resistance of the switch, usually both n-type and p-type transistors are used to form a transmission gate, shown in Fig. 2.9. The switch on-resistance is determined by the overdrive voltage of the switching transistor.

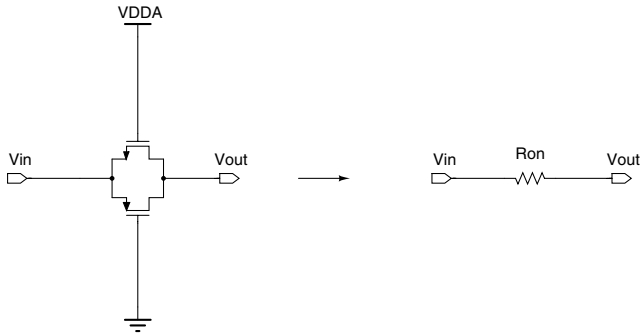



Figure 2.9: Schematic of the transmission gate.

For a single transistor, it can be expressed as:

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_T)} \tag{2.11}$$

For a transmission gate, the on-resistance is the parallel of the resistance of both n-type and p-type transistors. On the one hand, the scaling-down of the CMOS technology brings a higher gate oxide capacitance and helps to reduce the switch on-resistance. On the other hand, to reach low on-resistance of the switch, the overdrive voltage of the transistors should be as higher as possible. However, the scaling-down of the CMOS technology reduces the driving voltage for the switch, resulting into higher switch on-resistance. Fig. 2.10 shows the switch on-resistance v.s. the input voltage of the switch driven by a 1.8-V driving signal. While the driving voltage drops to 1 V, the switch on-resistance greatly increases, shown in Fig. 2.11. The reason is that the switch transistor is not sufficiently driven.

For a supply voltage smaller than $V_{Tn} + V_{Tp}$, clock-boosting circuits are employed to provide sufficient overdrive voltage, shown in Fig. 2.12 [Abo99] . The driving signal amplitude in the clock-boosting circuits is boosted on the input signal, producing a constant overdrive voltage for the switch transistor. The on-resistance of the switch is greatly reduced and is independent to the input signal. Other special techniques, e.g. switched-opamp [Ste94] or low-$V_T$ devices, can also be used to overcome the transistor-driving problem in a low-voltage environment. However, extra costs are paid, which limit the use of these circuits.

The movement to nanometer CMOS technologies results into a lower threshold voltage of the transistor. For MOS switches, it is beneficial to have a lower threshold voltage of the transistor, as a higher over-drive voltage can be reached with the same driving amplitude and, as a result, a lower on-resistance can be achieved. Though the transistor threshold voltage does not scale-down as fast as the supply voltage, there is still some room left for the transistor overdrive voltage. As long as the circuit works at the rated supply voltage, the switch can be driven sufficiently. Besides, the smaller transistor

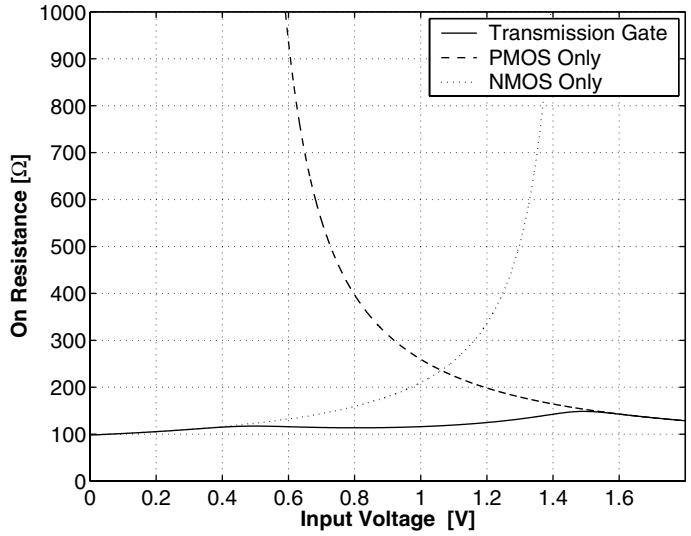



Figure 2.10: The simulated on-resistance of a transmission gate driven by an 1.8-V driving signal.

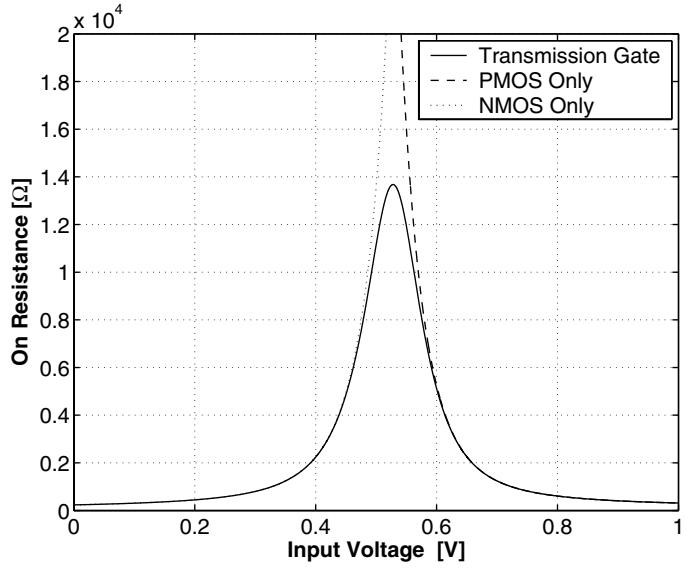
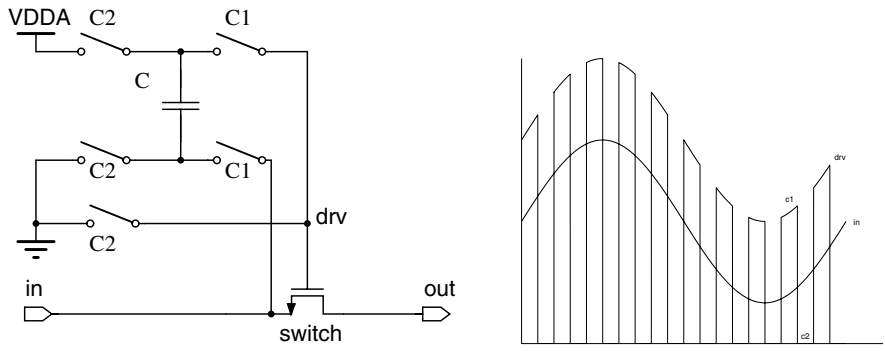



Figure 2.11: The simulated on-resistance of a transmission gate driven by an 1.0-V driving signal.




(a) The schematic of the clock boosting circuits.

(b) The driving waveform of the switch transistor.

Figure 2.12: The clock boosting circuit and its driving waveform.

sizes help to reduce the clock feed-through, charge injection and increase the operation speed of the switch.

### 2.4.5 Improved Device Matching

As described before, the matching properties are improved with the scaling-down of the CMOS technology. The device matching is a key factor on the performance of most ADCs. For example, the performance of the basic ADC, i.e. the Flash ADC, is based on the matching of the devices. For ADC designs, the better matching properties help to improve the ADC performance.

### 2.4.6 Digital Circuits Advantages

Another important advantage moving into nanometer technologies is that the power consumption of digital circuits is reduced while the speed is increased. On every ADC system, there are large amounts of digital blocks, e.g. clock generation and distribution circuits, encoders and output digital buffers, etc. The direct benefit of the scaling-down of the CMOS technology is the higher speed and lower power consumption in the digital circuits. For digital circuits, it is always beneficial to move into smaller feature sized technologies and in fact it is the main reason of the technology evolution. It is beneficial for $\Sigma$-$\Delta$ ADCs having a large digital part, i.e. digital filters and decimators.

## 2.5 Conclusion

In this chapter the scaling-down of the CMOS technology is introduced. Then the impact of the CMOS scaling-down to analog circuits is described. For analog circuits, the CMOS scaling-down brings us not only faster transistors, but also many design

difficulties. In short, in nanometer CMOS technologies, faster speed but less gain can be obtained from a single transistor, less voltage swings can be provided on the circuit, and better transistor matching can be expected.

Then the impact of the CMOS scaling-down to the most important part of the mixed-signal circuits, the ADC, is analyzed in different aspects. The most important challenge is the decreased supply voltage. As for ADCs, the direct impact is the reduced signal swing and thus the dynamic range of the ADC is compressed. The decreased supply voltage and the transistor characteristic degradation make the distortion a big challenge for high-linearity ADCs.

In the next chapter, basic ADC foundations will be introduced. The principles of the $\Sigma$-$\Delta$ modulators will be also described and different topologies of the $\Sigma$-$\Delta$ modulators will be analyzed.

Chapter 3

# Principle of Σ-Δ ADC

## 3.1 Introduction

The ADC is a fundamental building block in modern electronics systems. As a bridge between the analog to digital world, the ADC functions as a translator from an analog quantity to a digital code. There are many types of ADCs and each of them has its own advantages and shortages. Among them the Σ-Δ ADC features high resolution without requirement of high-precision devices, making it a popular choice of high-resolution ADCs in cheap CMOS technologies.

This chapter presents the principle of the ADC firstly. Then the Σ-Δ ADC is introduced and how oversampling and noise shaping are used in ADCs to improve the resolution of the ADC.

Starting with the principle of oversampling technique, the suppression of the quantization noise after the digital filtering is introduced. Then noise shaping, a more powerful mean of moving the quantization noise power out of the signal band, is explained. Linear models of Σ-Δ ADCs are introduced to analyse the Σ-Δ ADC.

The performance metrics used to characterize the Σ-Δ ADC are then introduced. Traditional single-loop single-bit and multibit Σ-Δ modulators are introduced. Then the cascaded Σ-Δ modulators are introduced.

## 3.2 Basic Analog to Digital Conversion

There are different values used in electronics. In the amplitude domain, there are discrete-amplitude values and continuous-amplitude values. In the time domain, there are continuous-time values and discrete-time values. The analog signal, the natural signal from the real world, is a continuous-time and continuous-amplitude value, as shown in Fig. 3.1. It is the physical signal that human beings can understand naturally and is the most common signal from the real world. The digital signal is defined as the discrete-time and discrete-amplitude value. It is the value that digital computers can process.

Since the digital signal is easy to store, duplicate, process and transfer, the digital signal processing dominates all electronic systems. The bridge between the analog world and the digital world, the ADC and DAC are becoming the bottlenecks of the system and getting more attention. An ADC, depicted in Fig. 3.2, is the device that converts the analog signal to the digital code. To perform the analog to digital conversion task, two

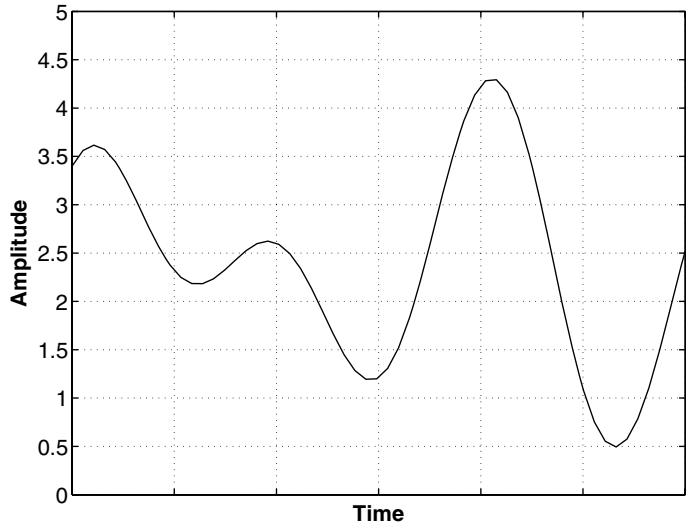



Figure 3.1: The analog signal.

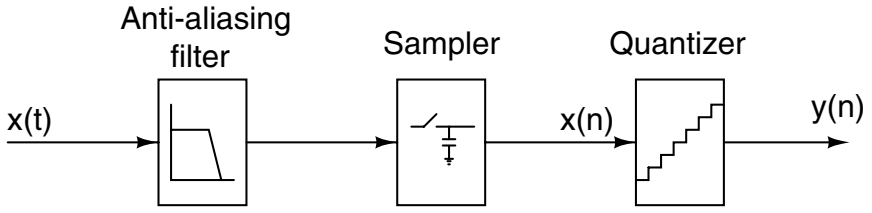



Figure 3.2: The block diagram of an ADC system.

steps should be done. The first one is the discretization in the time domain, which is called sampling. After the sample and hold, the analog signal is converted to a sampled-data signal, shown in Fig. 3.3. The second step is the discretization in the amplitude, which is called quantization. After the quantization, the sampled-data signal is converted to a digital signal, as shown in Fig. 3.4. So for every ADC, there must be a sampler and a quantizer. Mathematically, a N-bit analog to digital conversion can be expressed as [vdP94]:

$$V_{in} = \sum_{i=1}^{N} 2^{-i} b_i \cdot V_{ref} + e_q \tag{3.1}$$

where, the $V_{ref}$ refers to the reference voltage and the $b_i$ is the output bit from the ADC. The $e_q$ is so-called quantization error that is inevitable in all ADCs.

For an ADC, the most important parameters are input signal bandwidth and the resolu-

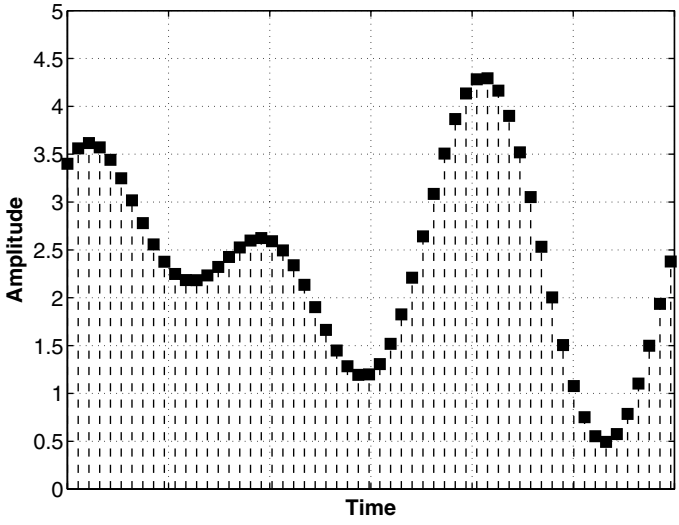



Figure 3.3: The discrete-time signal.

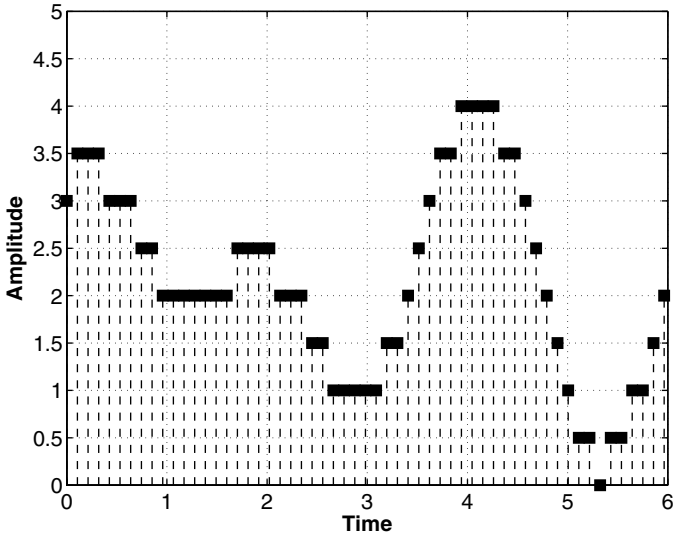



Figure 3.4: The digital signal.

tion. Illustrated in Fig. 3.5, there are many applications that need different input signal bandwidth and resolution parameters. Different types of ADCs are developed according to different requirements. Fig. 3.6 shows different types of ADCs with different input signal bandwidth and different resolution. The integrating type ADC is good at high-resolution low-speed applications such as measurement instruments and the conversion speed is normally less than a few hundred Hz. The $\Sigma$-$\Delta$ ADC is suitable for high resolution applications in the audio frequency range. For conversion speeds of 1 MHz to 100 MHz, the pipelined ADC finds its best position. For higher conversion speeds, the folding ADC is suitable and the resolution is normally around 10 bit. For conversion speed of 1 GHz and above, it is the area of the Flash ADC. There is a speed and resolution trade-off in ADC performance, which can be seen from Fig. 3.6.

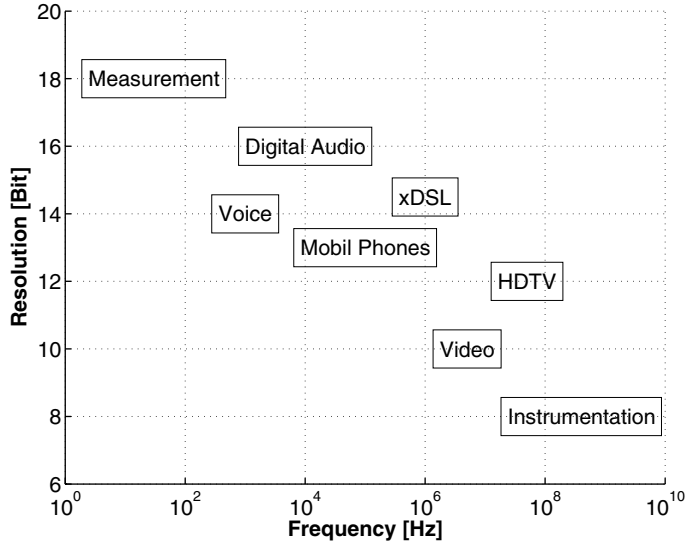



Figure 3.5: Different ADC applications.

For an ADC, there is always an error, $e_q$ in (3.1), associated with the ADC. This error is called quantization error. The higher resolution the ADC is, the smaller quantization error it has. Since the process of quantization is a classification process in amplitude, there is always a quantization error in an ADC, as shown in Fig. 3.7. The quantization error $e_q$ is smaller than the quantization step $\Delta$ of the ADC.

$$-\frac{\Delta}{2} \leq e_q \leq \frac{\Delta}{2} \tag{3.2}$$

The quantization step $\Delta$, with a value of $V_{ref}/2^N$ is called the least significant bit (LSB) of an ADC. Assuming the quantization error is uniformly distributed between

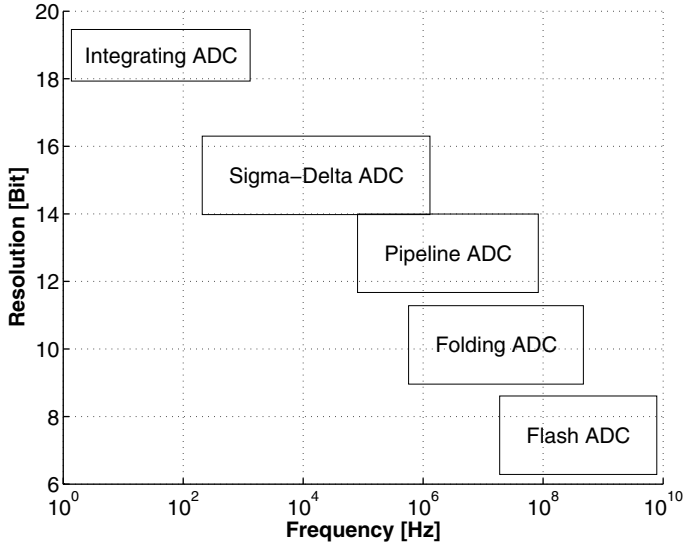



Figure 3.6: Different ADC types.

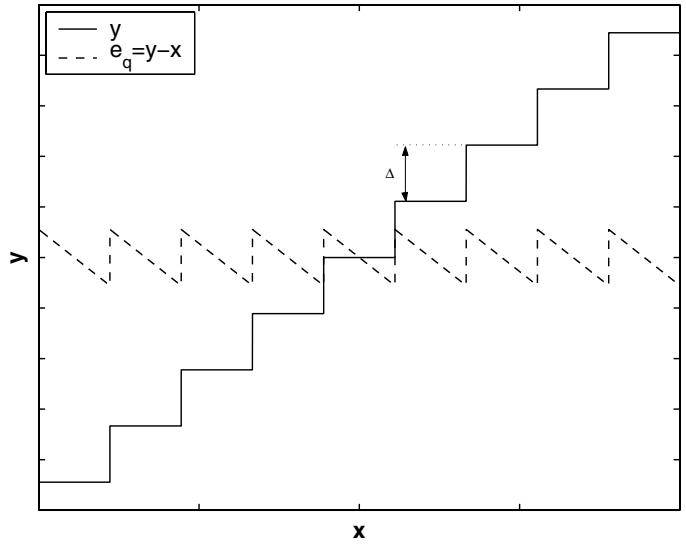



Figure 3.7: Transfer function of a nine-level quantizer and the quantization error $e_q$.

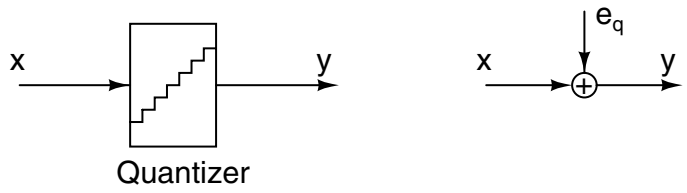



Figure 3.8: Linear model of a quantizer.

$\pm LSB/2$, the quantization error power is related to the quantization step:

$$e_q^2 = \frac{1}{LSB}\int_{-LSB/2}^{LSB/2} e_q^2 de_q = \frac{\Delta^2}{12} \tag{3.3}$$

The quantization error is dependent on the resolution of the ADC and it is often referred to as the quantization noise of an ADC. The quantizer can be modeled as a quantization noise source, shown in Fig. 3.8. From the equation (3.3), the peak SNR of an ideal N bit ADC for a sinusoidal input signal can be calculated as:

$$\begin{aligned} SNR_p &= 10log\frac{e_s^2}{e_q^2} \\ &= 10log\frac{12\cdot(\frac{V_{ref}}{2\sqrt{2}})^2}{(\frac{V_{ref}}{2^N})^2} \\ &= 10log\frac{3}{2}2^{2N} \\ &= 6.02N + 1.76\ dB \end{aligned} \tag{3.4}$$

where $e_s^2$ is the maximum input signal power. Note that equation (3.4) gives the best possible SNR for a N-bit ADC.

## 3.3 Oversampling and Noise Shaping

In the previous section, the quantization noise is introduced. It is assumed that the quantization noise is independent from the input signal. Moreover, the quantization noise power spectral density is uniformly distributed in the sampling frequency band, i.e. the quantization noise is the so-called white noise. Shown in Fig. 3.9, the power spectral density of the quantization noise, $S_e(f)$ is white and all its power is within $\pm f_s/2$, where $f_s$ is the sampling frequency. The total quantization power is $\frac{\Delta^2}{12}$, so the amplitude of the power spectral density is:

$$h_e = (\frac{\Delta^2}{12})\frac{1}{f_s} \tag{3.5}$$

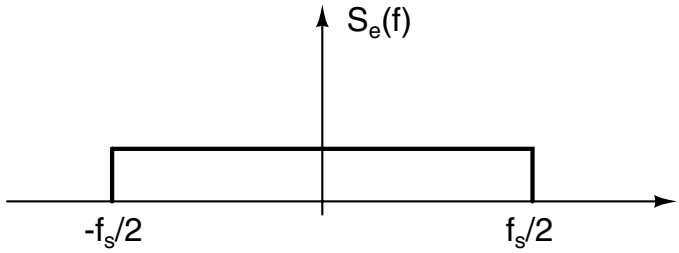



Figure 3.9: Power spectral density of quantization noise.

It can be seen in Fig. 3.9. The total power of the quantization noise is evenly distributed within $\pm f_s/2$. As the sampling frequency increases, the amplitude of the spectral density decreases, but the total quantization noise power remains the same. This property is used in oversampling converters, which will be discussed in the next session.

### 3.3.1 Oversampling

For a signal band-limited to $f_0$, the Nyquist rate is $2f_0$, which represents the minimum sampling rate without information loss. If the sampling frequency is greater than the Nyquist rate of the ADC, then it is called oversampling. The oversampling ratio is defined as:

$$OSR = \frac{f_s}{2f_0} \tag{3.6}$$

Shown in Fig. 3.10 is an oversampled ADC system. Assuming the signal frequency

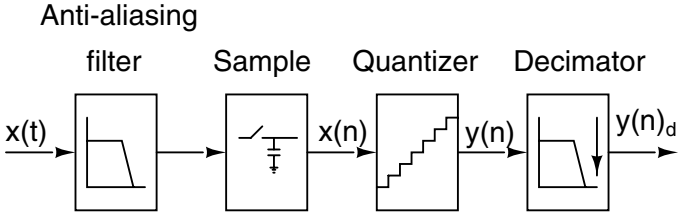



Figure 3.10: Block diagram of an oversampled ADC system.

is below $f_0$, the quantized signal then is filtered by a band-pass filter $H(f)$ whose frequency response is shown in Fig. 3.11. This filter eliminates the quantization noise whose frequency is greater than $f_0$. Then the quantization noise power is reduced to:

$$P_e = \int_{-f_s/2}^{f_s/2} S_e(f)|H(f)|^2 df = \frac{\Delta^2}{12}\left(\frac{1}{OSR}\right) \tag{3.7}$$

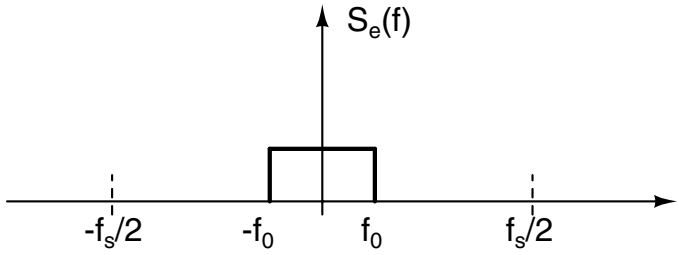



Figure 3.11: The frequency response of the filter to remove the out-of-band quantization noise power.

Therefore, by using an oversampling technique, the quantization noise power of an ADC can be reduced by a factor of $OSR$. It is an effective way to increase the SNR, hence the resolution, of an ADC system. Now the SNR formula can be revised as:

$$SNR_p = 10log\frac{e_s^2}{P_e} = 6.02N + 1.76 + 10log(OSR)\ \ dB \tag{3.8}$$

This formula clearly shows the benefit of the oversampling. For example, the peak SNR of an ADC can be increased by 3 dB by doubling the sampling frequency, i.e. the resolution of the ADC increases by 0.5 bit/octave. This gives a way to exchange the resolution with the speed for an ADC system, as long as the quantization noise is the major noise of the system. The improvement of oversampling converters over Nyquist converters costs more in practice, for example, the speed improvement of the circuit and the decimation filter. It is worth to mention that the oversampling technique also relaxes the requirement for the anti-aliasing filter.

It is possible to exploit the benefits of the oversampling technique even further by means of noise shaping.

### 3.3.2 Noise Shaping

How to increase the resolution of an ADC by oversampling is introduced before. However, the SNR gained is quite limited by using the oversampling technique alone. For example, only 0.5 bit is gained by doubling the sampling frequency in an oversampled ADC. It is clear that a more powerful method is needed. An intuitive way is introducing filtering into the ADC system to further suppress the in-band quantization noise power. However, the problem here is how to distinguish the quantization noise and the input signal.

By applying a loop filter $H(f)$ before the quantizer and introducing the feedback, shown in Fig. 3.12, a $\Sigma$-$\Delta$ modulator is built and different signal and quantization noise transfer functions is realized. After the decimation, the in-band quantization noise power is greatly suppressed. While combining with oversampling and noise shaping, a significant SNR improvement can be achieved for a $\Sigma$-$\Delta$ ADC compared

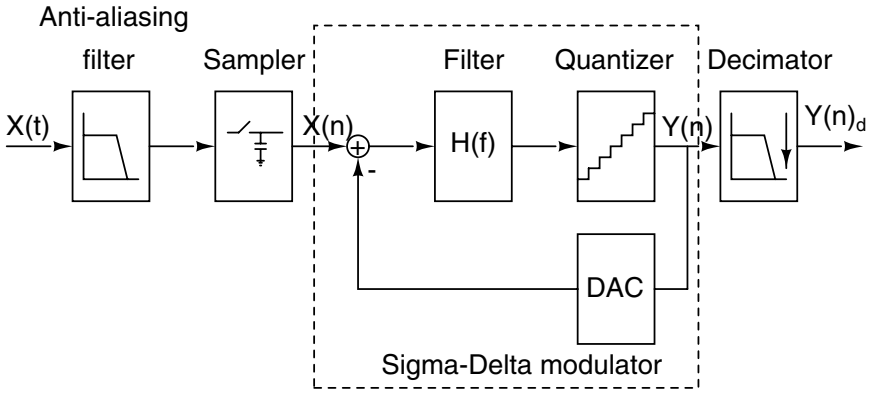



Figure 3.12: Block diagram of a noise shaping ADC system.

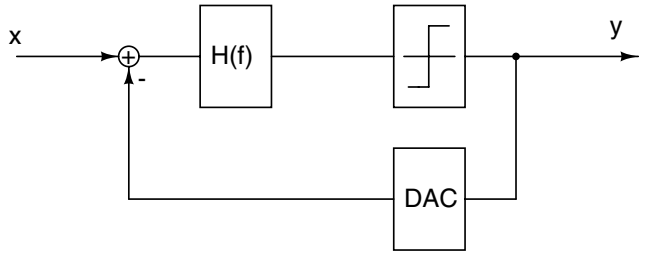



Figure 3.13: Block diagram of a Σ-Δ modulator.

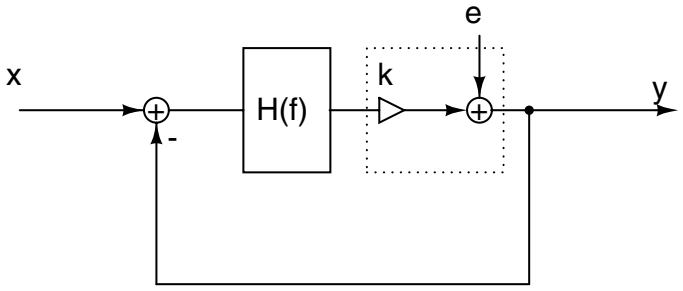



Figure 3.14: Linear model of a Σ-Δ modulator.

to the ADC with oversampling only.

The basic Σ-Δ modulator is shown in Fig. 3.13 and its linear model is shown in Fig. 3.14. The basic Σ-Δ modulator consists of a loop filter, a quantizer and a feedback loop. There should be a digital to analog converter inside the feedback loop since the output of the quantizer is a digital signal. The linear model of a Σ-Δ modulator models the quantizer with a quantization gain $k$ and a noise source. It is assumed that the DAC inside the feedback loop is an ideal one. In this system, there are two input signals, $x(n)$ and $e(n)$, and one output signal $y(n)$. The output of the Σ-Δ modulator can be expressed as:

$$Y(z) = H_x(z)X(z) + H_e(z)E(z) \tag{3.9}$$

where $H_x(z)$ represents the signal transfer function and $H_e(z)$ represents the quantization noise transfer function in the domain. The signal and noise transfer function can be calculated as:

$$H_x(z) = \frac{H(z)}{1+H(z)} \tag{3.10}$$

$$H_e(z) = \frac{1}{1+H(z)} \tag{3.11}$$

It is seen that the signal transfer function is different from the noise transfer function. By properly choosing the loop filter transfer function $H(z)$, the desired signal and noise transfer function can be obtained within a certain band of interest. If the loop filter transfer function $H(z)$ is designed to have a large gain inside the band of interest and small gain outside the band of interest, then the signal and noise transfer function become:

$$H_x(z) = 1 \tag{3.12}$$

$$H_e(z) = \frac{1}{1+H(z)} \ll 1 \tag{3.13}$$

The signal can pass the Σ-Δ modulator directly and the noise is greatly reduced inside the band of interest. This is called noise shaping.

For example, if an integrator is chosen to be the loop filter, its transfer function is:

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \tag{3.14}$$

Then the signal and noise transfer functions of the Σ-Δ modulator can be calculated as:

$$H_x(z) = z^{-1} \tag{3.15}$$

$$H_e(z) = 1 - z^{-1} \tag{3.16}$$

The loop filter transfer function, signal and noise transfer functions of the Σ-Δ modulator are shown in Fig. 3.15. It is seen the signal is passed to the output with a delay of a clock cycle, while the quantization noise is passed through a first-order low-pass filter. Combined with the oversampling, the SNR of the ADC can be improved. This is the principle of the first-order low-pass Σ-Δ modulator.

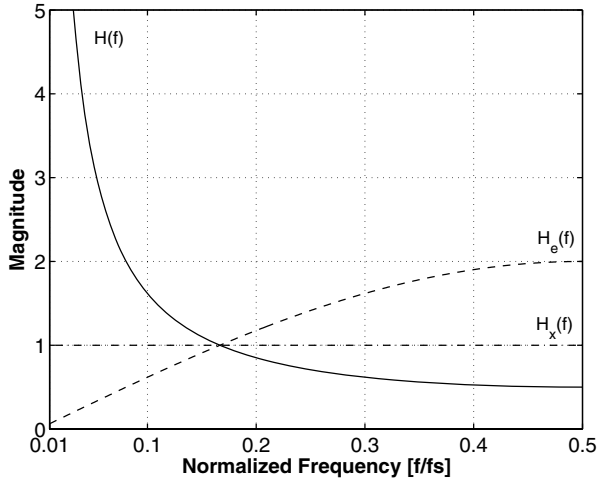



Figure 3.15: Loop filter, signal and noise transfer functions of a Σ-Δ modulator.

### 3.3.3 Σ-Δ Modulator

The Σ-Δ modulator concept is described above. Actually the Σ-Δ modulator is a feedback system. In the time-domain, the integrator integrates the difference between the input signal and the fedback output signal of the Σ-Δ modulator. The result of the integrator is then fed to the quantizer. The negative feedback tries to minimize the difference between the input signal and the output signal of the Σ-Δ modulator. As a result, the average of the output signal of the Σ-Δ modulator is tracking the input signal. This behavior is illustrated in Fig. 3.16 and Fig. 3.17.

It can be seen that the output of the Σ-Δ modulator tracks the input signal. In Fig. 3.16, a single-bit quantizer is used in the Σ-Δ modulator. The benefit of using a single-bit quantizer is that the linearity of a single-bit quantizer is assured. Since there are only two output states in the single-bit quantizer and two points define a straight line, so the single-bit quantizer is inherently linear. Therefore the single-bit quantizer is widely used in oversampled ADCs. The four-bit quantizer generates less quantization noise power compared to the single-bit quantizer, as shown in Fig. 3.17. As a result, the average value of the output tracks the input signal much closer than the single-bit one.

So far the discussion is constrained to low-pass Σ-Δ modulators. Depending on the frequency band of interest, there is another type of Σ-Δ modulator, band-pass Σ-Δ modulator, widely used in wireless transceivers. By applying different loop filters inside the Σ-Δ modulator, a high attenuation of quantization noise in a certain frequency

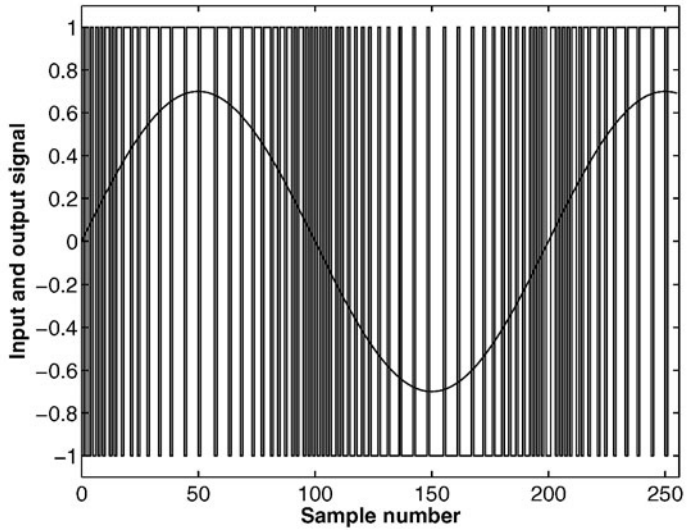



Figure 3.16: Input and output waveforms of a first-order Σ-Δ modulator with single-bit quantizer.

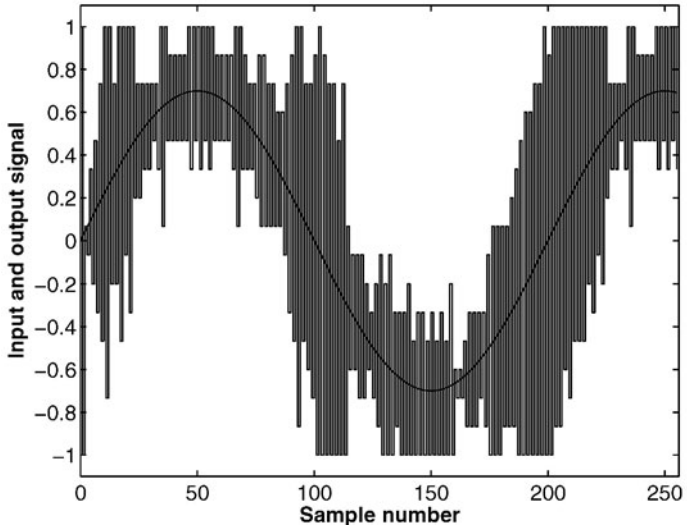



Figure 3.17: Input and output waveforms of a first-order Σ-Δ modulator with four-bit quantizer.

band can be realized. For example, when the loop filter is of second-order given by:

$$H(z) = \frac{-z^{-2}}{1+z^{-2}} \tag{3.17}$$

Then the signal and noise transfer functions of the Σ-Δ modulator is given by:

$$H_x(z) = -z^{-2} \tag{3.18}$$
$$H_e(z) = 1+z^{-2} \tag{3.19}$$

The loop filter, signal and noise transfer functions of the Σ-Δ modulator are shown in Fig. 3.18. The quantization noise is suppressed in the frequency band around $f_s/4$. This type of modulator is useful in digitizing signals within a certain frequency range and finds its applications in wireless transceivers.

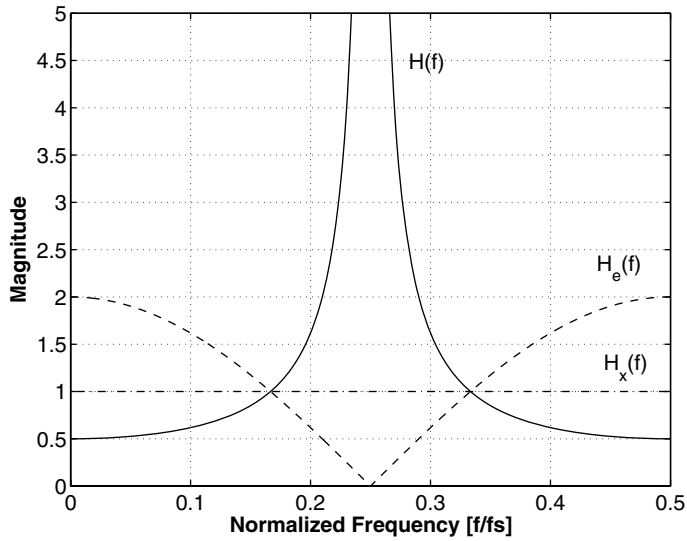



Figure 3.18: Loop filter, signal and noise transfer functions of a bandpass Σ-Δ modulator.

### 3.3.4 Performance Metrics for the Σ-Δ ADC

For oversampled ADCs, since the operation principles are different from the Nyquist ADCs, different performance metrics are used to evaluate the performance of oversampled ADCs. Some important specifications are discussed here.

- **Signal to Noise Ratio.** The SNR of a converter is the ratio of the input signal power to the noise power measured at the output of the converter. The maximum SNR of a converter can achieve is called peak signal-to-noise-ratio ($SNR_p$). The noise here should include the quantization noise and circuit noise.

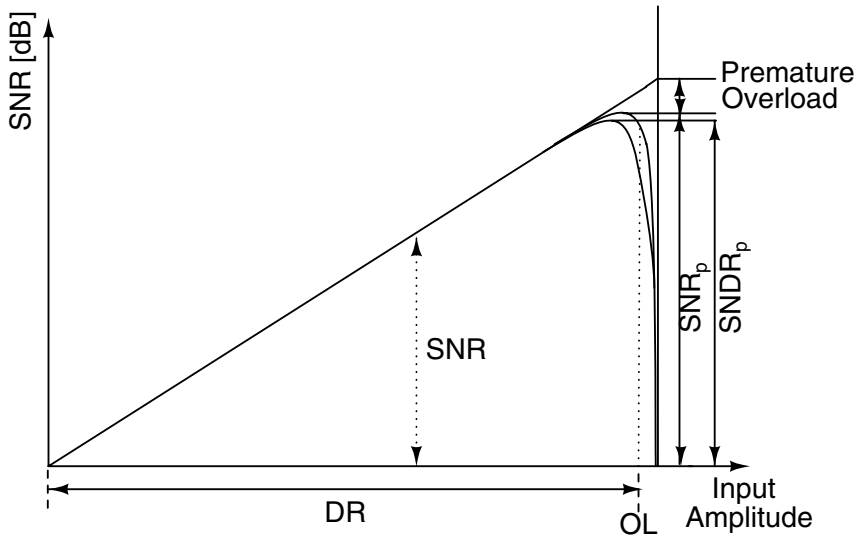



Figure 3.19: Definitions of the performance metrics used to characterize a Σ-Δ ADC.

- **Signal to Noise and Distortion Ratio.** The SNDR of a converter is the ratio of the input signal power to the power of the distortion components and noise measured at the output of the converter. The maximum SNDR of a converter can achieve is called peak signal-to-noise-and-distortion-ratio ($SNDR_p$).

- **Dynamic Range.** The DR is the ratio between the maximum input signal power can be applied to the input of the converter without significant performance degradation, and the minimum detectable input signal power. A significant performance degradation of a converter is considered as the SNR drops more than 3 dB below the peak SNR value. The minimum detectable input signal is the input power that the converter has for a SNR of 0 dB.

- **Overload Level.** The OL is the relative input amplitude where the SNR decreases by 3 dB below the peak SNR.

These specifications are illustrated in Fig. 3.19. This figure shows the SNR and SNDR of the Σ-Δ modulator versus the amplitude of the signal applied to the input of the converter. Naturally, the SNR increases linearly with the increase of the input amplitude for an ideal converter. When the input signal amplitude is small, the distortion component is immerged in the noise floor of the converter. Therefore, the SNR and SNDR curves are merged together. With the increase of the input amplitude, the distortion power becomes larger than the noise power and the SNDR starts to decrease.

The $SNDR_p$ reflects the linear performance of the converter. Due to the distortion power, the $SNDR_p$ is smaller than the $SNR_p$ for the same converter. After the converter reaches its $SNR_p$, the performance of the converter degrades drastically due to the overload of the modulator, where instability occurs. The overload is the special characteristics of the Σ-Δ modulator. The overload level of a Σ-Δ modulator defines the dynamic range of a converter. When the input amplitude is larger than a certain value, the Σ-Δ modulator loop becomes unstable and the noise shaping disappears. Large quantization power in the signal band results into a drastic decrease of the SNR. In the normal operation of the Σ-Δ modulator, overload should be avoided.

## 3.4 Traditional Σ-Δ ADC Topology

The Σ-Δ ADC trades speed with resolution by means of oversampling and noise shaping, as discussed in the previous section. In this section, the single-loop Σ-Δ modulator is introduced. The relationship between the performance and the topology parameters is also discussed in this section. Then the cascaded Σ-Δ modulator is presented. Pros and cons of different topologies are analyzed in details. To make a difference from the full feedforward topology introduced in Chapter 5, the Σ-Δ modulator topology without feedforward is called traditional topology in this text.

### 3.4.1 Single-Loop Single-Bit Σ-Δ Modulators

The single-loop Σ-Δ converter is defined as there being only one single Σ-Δ loop in the whole converter. The ability of noise shaping can be improved by increasing the order of the loop filter. Shown in Fig. 3.20 is the block diagram of a first-order single loop Σ-Δ modulator. By inserting another integrator inside the loop a second-order Σ-Δ modulator can be obtained, shown in Fig. 3.21.

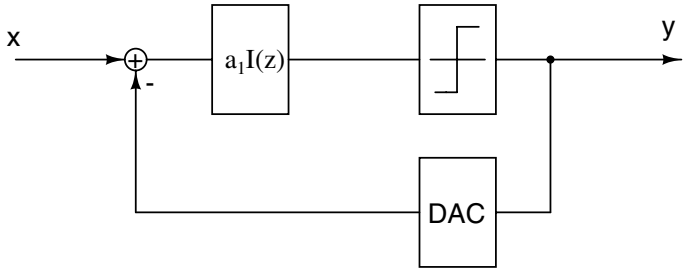



Figure 3.20: The first-order single-loop Σ-Δ modulator.

Similarly, by inserting more integrator stages inside the loop, a higher-order Σ-Δ modulator can be realized. In Fig. 3.22, a general block diagram of a n-th order single loop Σ-Δ modulator is shown. Consequently, as demonstrated in Fig. 3.23 the noise transfer functions become steeper in the signal band for higher-order Σ-Δ modulators. The

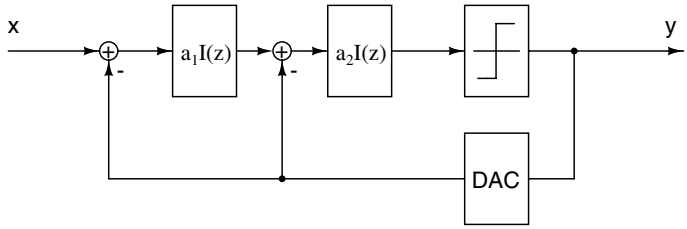



Figure 3.21: The second-order single-loop Σ-Δ modulator.

signal transfer function of an ideal n-th order Σ-Δ modulator can be expressed as:

$$H_x(z) = z^{-n} \tag{3.20}$$
$$H_e(z) = (1 - z^{-1})^n \tag{3.21}$$

The signal transfer function is only a n-th order delay and the noise transfer function is a n-th order high-pass filter. The total quantization noise power inside the signal band is:

$$\begin{aligned} P_e &= \int_{-f_s/2}^{f_s/2} S_e(f)|H(f)|^2 df \\ &= \int_{-f_b}^{f_b} S_e(f)|1 - z^{-1}|^{2n} df \\ &= \int_{-f_b}^{f_b} \frac{\Delta^2}{12 f_s} \left| \frac{j2\pi f}{f_s} \right|^{2n} df \\ &= \left(\frac{\Delta}{2}\right)^2 \cdot \frac{1}{3\pi(2n+1)} \cdot \left(\frac{\pi}{OSR}\right)^{2n+1} \end{aligned} \tag{3.22}$$

Then the $SNR_p$ of the n-th order Σ-Δ modulator can be calculated as:

$$SNR_p = \frac{3\pi}{2} \cdot (2^B - 1)^2 \cdot (2n+1) \cdot \left(\frac{OSR}{\pi}\right)^{2n+1} \tag{3.23}$$

where B is the number of bits in the quantizer. This is the theoretical performance of an ideal n-th order single-loop Σ-Δ modulator. Compared to the first-order Σ-Δ modulator, the noise shaping ability of the n-th order Σ-Δ modulator is greatly improved. However, the Σ-Δ modulator loop can be unstable when the order is greater than two [Nor96]. The reason is that the higher loop-gain of the high-order loop filter causes the overload of the quantizer. Loop coefficients, $a_1 \cdots a_i$, are introduced to ensure the stability of a high order Σ-Δ modulator. The constant $a_i$ in front of the integrator is called the loop coefficient of this stage. Then the transfer function of the

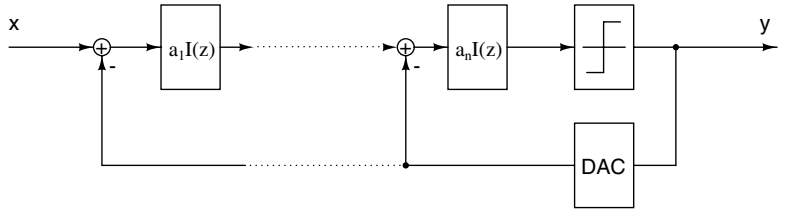



Figure 3.22: General block diagram of the n-th order single-loop Σ-Δ modulator.

quantization noise is:

$$H_e(z) = \frac{1}{1 + k \cdot \sum_{i=1}^{n} \prod_{j-i}^{n} a_j \left( \frac{z^{-1}}{1 - z^{-1}} \right)^{n-i+1}} \tag{3.24}$$

The amplitude of the noise transfer function can be approximated as:

$$|H_e(z)| \approx \frac{|1 - z^{-1}|^n}{k \cdot \sum_{i=1}^{n} a_i} \tag{3.25}$$

Then the SNR of the Σ-Δ modulator can be calculated as:

$$SNR_p = SNR_{p(ideal)} \cdot \left( k \cdot \prod_{i=1}^{n} a_i \right)^2 \tag{3.26}$$

The quantization gain $k$ is not determined in a single-bit quantizer, since it only responds to the polarity of the input signal. As a result, the gain of the last integrator is irrelevant to the operation of the Σ-Δ modulator. In other words, the last loop coefficient can be chosen to have any value without affecting the performance of the Σ-Δ modulator. For a single-bit Σ-Δ modulator, the quantization gain $k$ can be combined with the last integrator gain.

Normally the product of all coefficients is smaller than unity to reach stability. Compared to the ideal Σ-Δ modulator, the SNR degrades due to the introduction of the loop coefficients. By properly choosing the loop coefficients, the high order Σ-Δ modulator can be made stable in the whole input range. However, the steepness of the noise transfer function is more gentle than the ideal one, which means that the noise shaping ability is degraded.

According to equation (3.23) and (3.26), the noise shaping ability of aΣ-Δ modulator is determined by the following factors: oversampling ratio, order of the noise shaping, number of bits of the quantizer and loop coefficients.

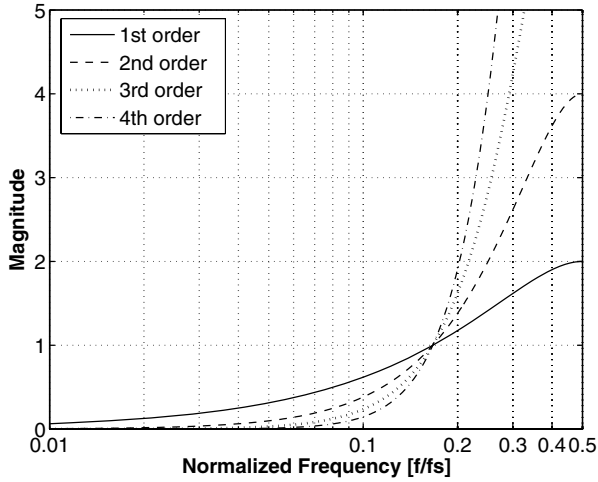



Figure 3.23: Ideal noise transfer functions of Σ-Δ modulators.

- **Oversampling ratio.** The SNR of the Σ-Δ ADC can be increased by $(2n + 1) \cdot 3\,dB$, or $n+0.5\,bits$ by doubling the oversampling ratio, where $n$ denotes the order of the loop filter. It is tempting to raise the oversampling ratio to increase the SNR of the Σ-Δ modulator. However, it is restricted by the speed limit of the circuit and the power consumption. In practice, for the same performance, it is preferred to lower the oversampling ratio. Another driving force is the ever-increasing bandwidth requirement, which also needs to lower the oversampling ratio. For high bandwidth converters, the oversampling ratio should be kept as low as possible. A lot of efforts have been made at the system level to lower the oversampling ratio and maintain the same performance.

- **Order of the loop filter.** The SNR of the converter can be increased by increasing the order of the loop filter $n$ ideally. However, while increasing the order of the loop filter, the stability problem is the prior concern. Smaller loop coefficients are then introduced to maintain the stability of the converter. Consequently, the noise shaping ability is compromised. Moreover, more circuits are also required to expand the order of the loop filter. Practically the order of the loop filter is less than fifth-order.

- **Number of bits of the quantizer.** For the intrinsic linearity of the single-bit quantizer and the single-bit DAC in the feedback loop, many Σ-ΔADCs employ the single-bit quantizer. However, increasing the number of bits in the quantizer increases the SNR of the converter significantly. For each additional bit in the quantizer, the SNR of the converter increased by 6 dB. Moreover, by employing a multibit quantizer, the loop stability can also be improved and loop coefficients can be enlarged. Thus more powerful noise shaping ability is obtained. The

linearity of the multibit DAC in the feedback loop directly affects the linearity of the converter. Since the feedback loop is connected directly to the input of the Σ-Δ modulator, any non-linearity in the DAC can not be distinguished from the input signal and will be shown in the output. Therefore, the accuracy of the DAC should be at least as good as the Σ-Δ converter in order not to degrade the performance of the Σ-Δ converter. Dynamic matching techniques are the main solution to tackle this problem [Pla76] [Pla79] [Gee02].

- **Loop coefficients.** Loop coefficients are introduced to stabilize the Σ-Δ modulator. However, they degrade the SNR of the Σ-Δ modulator. The larger coefficients are, the better noise shaping ability can be achieved, and the higher the risk is to get instability for the Σ-Δ modulator. Balance between the stability and the SNR is necessary. Optimized loop coefficients are developed for high performance Σ-Δ modulators in [Mar98].

Fig. 3.24 shows the output spectrum of single-loop single-bit Σ-Δ modulator of the first-order to the fourth-order. The loop coefficients are taken from Table 3.1 [Mar99]. In Table 3.1 the loop coefficients and the performances are presented. It is worth to mention that in the first-order Σ-Δ modulator, large idle tones are found in the spectrum of the output. Such modulators are thus better avoided.

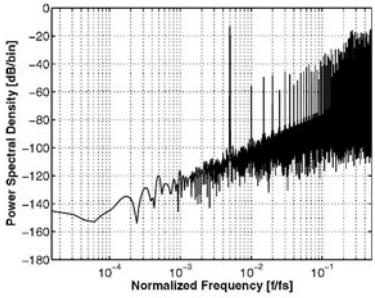
Table 3.1: Topology parameters and modulator performance for second to fourth-order single-loop single-bit Σ-Δ modulators.

| Loop Coefficients | $(a_1, a_2)$ (0.5,0.5) | | $(a_1, a_2, a_3)$ (0.2,0.5,0.5) | | $(a_1, a_2, a_3, a_4)$ (0.2,0.2,0.5,0.5) | |
|---|---|---|---|---|---|---|
| Loop order | 2 | | 3 | | 4 | |
| OSR | $SNR_p$ | OL | $SNR_p$ | OL | $SNR_p$ | OL |
| 16 | 42 | 0.7 | 43 | 0.6 | 40 | 0.6 |
| 32 | 57 | 0.7 | 65 | 0.55 | 71 | 0.6 |
| 64 | 74 | 0.7 | 86 | 0.55 | 100 | 0.55 |
| 128 | 88 | 0.65 | 108 | 0.55 | 128 | 0.55 |

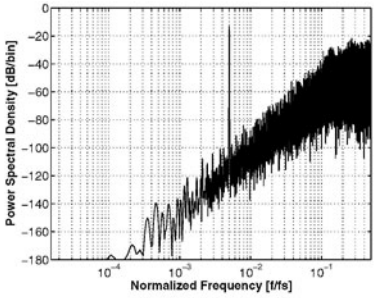
### 3.4.2 Single-Loop Multibit Σ-Δ Modulators

The above discussed Σ-Δ modulators are limited to the single-bit topology, whose quantizer is a single-bit one. The most appealing characteristic of the single-bit quantizer is the intrinsic linearity of the single-bit quantizer and the single-bit DAC in the feedback loop. The precision of the DAC in the feedback loop defines the precision of the whole Σ-Δ modulator since the DAC error can not be processed by the Σ-Δ modulator loop. Therefore, for the single bit Σ-Δ modulator, there is no linearity problem encountered and the linearity of the Σ-Δ modulator is guaranteed.

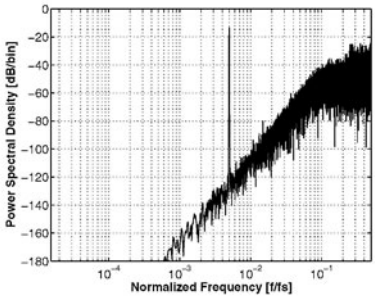
However, based on the quantization noise equation, the quantization noise power is related to the number of bits of the quantizer itself. It is a very effective way to reduce the quantization noise power by increasing the number of bits in the quantizer. Another



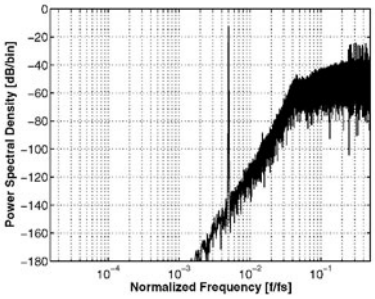

(a) Output spectrum of a first-order single-loop single-bit Σ-Δ modulator.




(b) Output spectrum of a second-order single-loop single-bit Σ-Δ modulator.




(c) Output spectrum of a third-order single-loop single-bit Σ-Δ modulator.




(d) Output spectrum of a fourth-order single-loop single-bit Σ-Δ modulator.

Figure 3.24: Figure (a) to (d): output spectrum of first-order to fourth-order single-loop single-bit Σ-Δ modulators.

benefit gained from the multibit quantizer is that the loop coefficients can be scaled-up due to the improvement of the loop stability. For example, for a fourth-order single-bit Σ-Δ modulator, the loop coefficients are $(a_1, a_2, a_3, a_4) = (0.2, 0.2, 0.5, 0.5)$, and the $SNR_p$ is 71 dB when OSR is 32. For the same fourth-order four-bit Σ-Δ modulator, the loop coefficients are $(a_1, a_2, a_3, a_4) = (0.25, 0.5, 0.75, 2.25)$, and the $SNR_p$ is 117 dB under the same condition. The use of a four-bit quantizer improves the $SNR_p$ with 24 dB, while the scaling-up of loop coefficients contributes extra 14 dB for the $SNR_p$ of the converter [Gee01]. Compared to the single-bit version, this is a great improvement on the performance. Especially for wide-band Σ-Δ modulators, it is advantageous to choose a multibit Σ-Δ modulator topology to lower the OSR. Table 3.2 summarizes the loop coefficients and the performance of the second to fourth-order single-loop 4-bit Σ-Δ modulators.

Table 3.2: Topology parameters and modulator performance for second to fourth-order single-loop 4-bit Σ-Δ modulators.

| Loop Coefficients | $(a_1, a_2)$ (0.75,2.25) | | $(a_1, a_2, a_3)$ (0.5,0.75,2.25) | | $(a_1, a_2, a_3, a_4)$ (0.25,0.5,0.75,2.25) | |
|---|---|---|---|---|---|---|
| Loop order | 2 | | 3 | | 4 | |
| OSR | $SNR_p$ | OL | $SNR_p$ | OL | $SNR_p$ | OL |
| 16 | 78 | 0.9 | 86 | 0.85 | 89 | 0.8 |
| 32 | 94 | 0.9 | 107 | 0.85 | 117 | 0.85 |
| 64 | 106 | 0.9 | 128 | 0.85 | 144 | 0.85 |
| 128 | 123 | 0.9 | 145 | 0.85 | 168 | 0.85 |

There are many ways to increase the linearity of the DAC in the feedback loop, such as digital correction [Cat89], [SN93] and dynamic element matching(DEM) [Pla76], [Pla79], [Car89], [Gee01], [Gee02]. Without additional trimming or calibration, the dynamic element matching technique is an effective way to increase the linearity of the DAC and it is widely used in the multibit Σ-Δ converters.

### 3.4.3 Cascaded Σ-Δ Modulators

Smaller loop-coefficients are used in the single-loop high-order Σ-Δ modulator due to the stability problem. Consequently, for the single-bit high-order Σ-Δ modulator, the SNR significantly degrades compared to the ideal one. This effect significantly restricts the benefit of increasing the order of the loop filter. The cascaded Σ-Δ modulator is an effective way to solve this problem.

The noise cancelling of a n-th order Σ-Δ modulator is shown in Fig. 3.25. The quantization noise of the n-th order Σ-Δ modulator is extracted by a subtracter and then fed to an ideal ADC. The digital output of the Σ-Δ modulator and the ideal ADC are then processed in the digital domain. If the transfer function of the block $H_1$ and

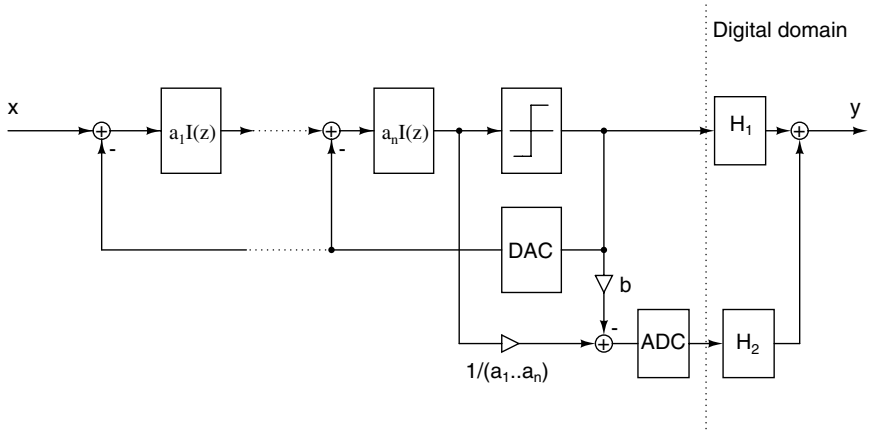



Figure 3.25: Block diagram of the noise cancelling concept.

$H_2$ is defined by:

$$\begin{aligned} H_1(z) &= 1 + (b-1)(1-z^{-1})^n \\ H_2(z) &= (1-z^{-1})^n \end{aligned} \tag{3.27}$$

Then the output of the whole system is:

$$Y(z) = z^{-1} \cdot X(z) \tag{3.28}$$

It can be seen from the above equation that the quantization noise of the n-th order Σ-Δ modulator is cancelled completely [Rib91] [Yin94a]. In practice, the matching between the two loops can introduce some errors and perfect cancellation may not be achieved. On the other hand, the quantization errors of the last ADC still can be seen in the output. Therefore, the exact noise cancellation depends on the matching of the two loops and the precision of the ADC in the cancellation loop.

By exploiting such a noise cancellation technique, a cascaded Σ-Δ modulator can be built. Normally the ADC in the noise cancelling loop is implemented by another Σ-Δ modulator. The quantization noise of the last Σ-Δ modulator is present in the output of the cascaded Σ-Δ modulator. The cascaded topology is the combination of several intrinsically stable first or second-order Σ-Δ modulators. By employing a cascaded topology, higher noise shaping can be obtained without the stability problem. Fig. 3.26 shows the block diagram of a third-order cascaded 2-1 Σ-Δ modulator topology composed by a second-order Σ-Δ modulator and a first-order Σ-Δ modulator. The cascaded Σ-Δ modulator consists of several stages of low-order Σ-Δ modulators. The quantization noise of the previous Σ-Δ modulator is fed to the next Σ-Δ modulator. Then the outputs of all Σ-Δ modulators are processed in the digital domain to cancel the quantization noise of the Σ-Δ modulators except the last stage Σ-Δ modulator. It

is seen that there is no feedback branch across different Σ-Δ modulators. Therefore, the cascaded Σ-Δ modulator is stable as long as each stage of Σ-Δ modulator is stable [Mat87], [Rib91].

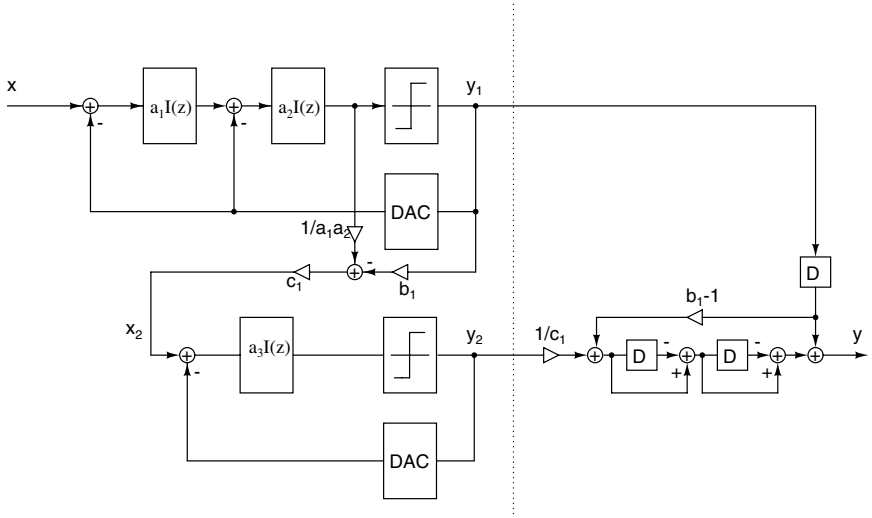



Figure 3.26: Block diagram of a third-order cascaded 2-1 Σ-Δ modulator topology.

Taking the cascaded 2-1 topology as an example, the output of the first Σ-Δ modulator can be expressed as:

$$Y_1(z) = \frac{a_1 a_2 k_1 z^{-2} X(z) + (1 - z^{-1})^2 E_1(z)}{D(z)} \tag{3.29}$$

where $D(z) = 1 + (a_2 k_1 - 2)z^{-1} + (a_1 a_2 k_1 - a_2 k_1 + 1)z^{-2}$, and $k_1$ is the quantization gain of the first Σ-Δ modulator. The output of the second Σ-Δ modulator is:

$$Y_2(z) = \frac{a_3 k_2 z^{-1} X_2(z) + (1 - z^{-1}) E_2(z)}{1 - (1 - a_3 k_2) z^{-1}} \tag{3.30}$$

The input of the second Σ-Δ modulator is:

$$X_2(Z) = \frac{Y_1(z) - E_1(z)}{a_1 a_2 k_1} - b_1 Y_1(z) \tag{3.31}$$

Then the output of the cascaded Σ-Δ modulator is:

$$Y(z) = Y_1(z) \cdot H_1(z) + Y_2(z) \cdot H_2(z) \tag{3.32}$$

The digital processing block transfer functions are:

$$H_1(z) = z^{-1}(1 + (b_1 - 1)(1 - z^{-1})^2) \tag{3.33}$$

$$H_2(z) = \frac{(1 - z^{-1})^2}{c_1} \tag{3.34}$$

Taking the assumption of:

$$a_1 a_2 k_1 = 1 \tag{3.35}$$

$$a_2 k_1 = 2 \tag{3.36}$$

$$a_3 k_2 = 1 \tag{3.37}$$

Then finally the output of the cascaded 2-1 topology is the combination of (3.32) and (3.33-3.37):

$$Y(z) = z^{-3}X(z) + \frac{(1 - z^{-1})^3}{c_1} \cdot E_2(z) \tag{3.38}$$

It is seen that the quantization noise of the first Σ-Δ modulator is completely cancelled. Only the quantization noise of the second Σ-Δ modulator, $E_2(z)$, is seen in the output. The quantization noise is noise-shaped by a third-order noise shaping function and reduced by a factor $c_1$.

In addition to the above mentioned cascaded 2-1 topology, there are other ways to cascade several Σ-Δ modulators. The performance achieved is different. For example, a fourth-order cascaded Σ-Δ modulator can be composed by a 2-2 topology or a 2-1-1 topology, shown in Fig. 3.27 and Fig. 3.28 respectively. The cascaded 2-2 topology is constructed by two second-order Σ-Δ modulators and the cascaded 2-1-1 topology is constructed by a second-order Σ-Δ modulator and two first-order Σ-Δ modulators. Tables 3.3, 3.4 and 3.5 summarize loop coefficients and the performance of the cascaded 2-1, 2-2 and 2-1-1 Σ-Δ modulators respectively [Mar98], [Mar99], [Gee99], [Gee01].

In principle any Σ-Δ modulator can be used in the cascaded Σ-Δ modulator. For stability consideration, only first and second-order Σ-Δ modulators are used in cascaded Σ-Δ modulators. Therefore, the cascaded Σ-Δ modulator maintains intrinsic stability and achieves high-order noise shaping. It should be avoided to use the first-order Σ-Δ modulator as the first stage of the cascaded Σ-Δ modulator, since large idle tones from the first stage can directly leak to the output. Normally the second-order Σ-Δ modulator is put in the first stage to avoid the idle tone problem.

Generally by applying linear analysis, the quantization noise transfer function of a cascaded Σ-Δ converter is given by [Mar99]:

$$H_e(z) \approx \frac{(1 - z^{-1})^n}{\prod_{i=1}^{m} c_i} \tag{3.39}$$

where $m$ is the number of cascaded stages and $c_i$ is the coupling coefficient between different stages. Compared to the ideal n-th order Σ-Δ modulator, the performance

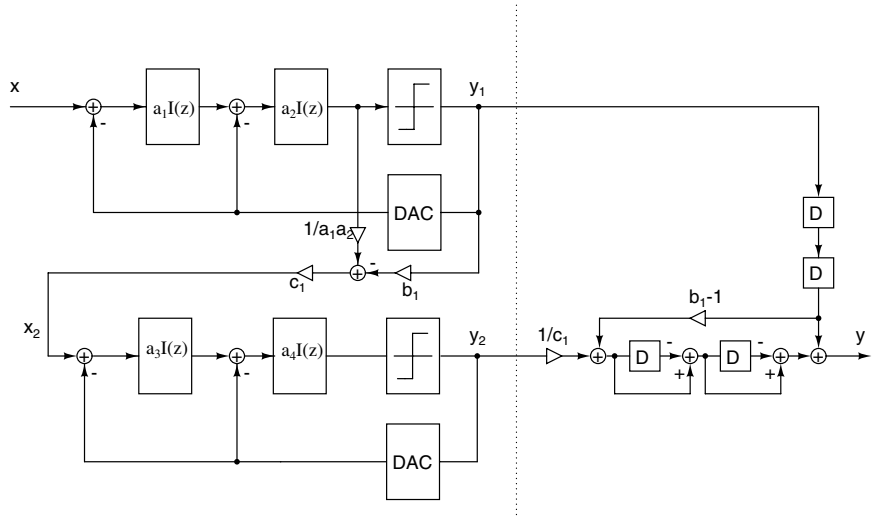



Figure 3.27: Block diagram of a fourth-order cascaded 2-2 Σ-Δ modulator topology.

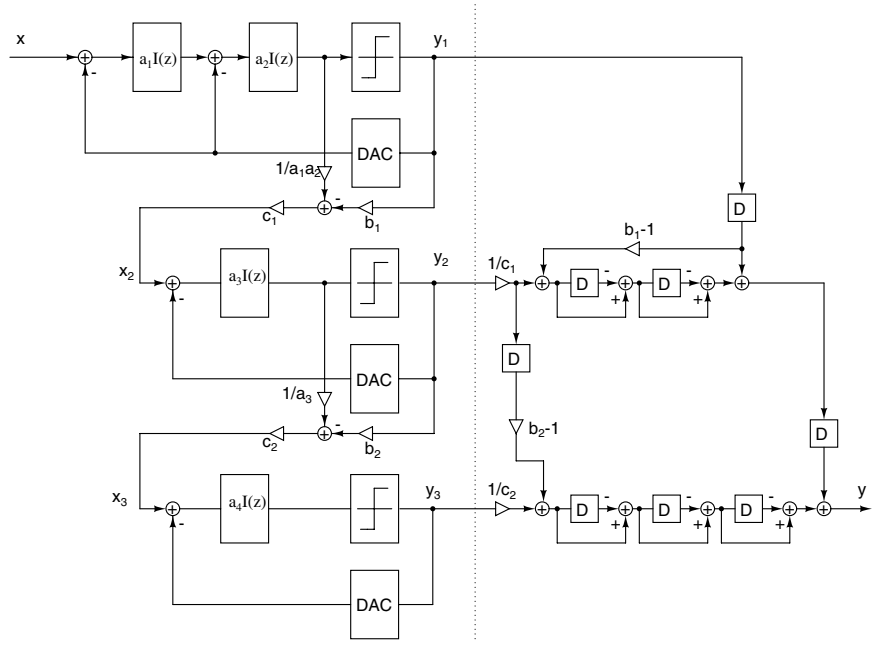



Figure 3.28: Block diagram of a fourth-order cascaded 2-1-1 Σ-Δ modulator topology.

Table 3.3: Topology parameters and modulator performance for the cascaded 2-1 Σ-Δ modulator.

| Loop Coefficients | ( $a_1$, $a_2$, $a_3$, $b_1$, $c_1$) ( 0.5, 0.5, 0.5, 2, 0.5) | |
|---|---|---|
| Topology | 2-1 | |
| OSR | $SNR_p$ | OL |
| 16 | 56 | 0.75 |
| 32 | 77 | 0.7 |
| 64 | 96 | 0.7 |
| 128 | 119 | 0.65 |

Table 3.4: Topology parameters and modulator performance for the cascaded 2-2 Σ-Δ modulator.

| Loop Coefficients | ( $a_1$, $a_2$, $a_3$, $a_4$, $b_1$, $c_1$) ( 0.5, 0.5, 0.5, 0.5, 2, 0.5) | |
|---|---|---|
| Topology | 2-2 | |
| OSR | $SNR_p$ | OL |
| 16 | 64 | 0.7 |
| 32 | 92 | 0.7 |
| 64 | 119 | 0.65 |
| 128 | 144 | 0.6 |

Table 3.5: Topology parameters and modulator performance for the cascaded 2-1-1 Σ-Δ modulator.

| Loop Coefficients | ( $a_1$, $a_2$, $a_3$, $a_4$, $b_1$, $c_1$, $b_2$, $c_2$) ( 0.5, 0.5, 0.5, 0.5, 2, 0.5, 1, 1) | |
|---|---|---|
| Topology | 2-1-1 | |
| OSR | $SNR_p$ | OL |
| 16 | 72 | 0.7 |
| 32 | 99 | 0.7 |
| 64 | 125 | 0.65 |
| 128 | 152 | 0.65 |

degradation depends on the coupling coefficients. For best noise shaping, it is preferred to increase the coupling coefficient. However, the coupling coefficient defines the input amplitude of the next stage and is restricted by circuit's characteristics. The best strategy for a cascaded Σ-Δ modulator design is to maximize the coupling coefficients without overloading the next stage to achieve a higher SNR.

The main drawback of the cascaded Σ-Δ modulator is the severe requirement of the building blocks. The noise cancellation relies on the matching of the cascaded converters. If the matching is not well controlled, then the noise cancellation is not perfect. There is a quantization noise component from the previous converter appearing in the output of the whole converter. This is called noise leakage [Rib91], [Yin94b]. In a real circuit implementation, the mismatch of the loop coefficient, the finite OTA DC gain and the settling error of the integrator are the main sources of the noise leakage of a cascaded Σ-Δ converter. From the last chapter, the non-idealities is getting more severe in nanometer CMOS technologies. The higher sensitivity to the non-idealities of the building blocks makes the implementation even more difficult in nanometer CMOS technologies.

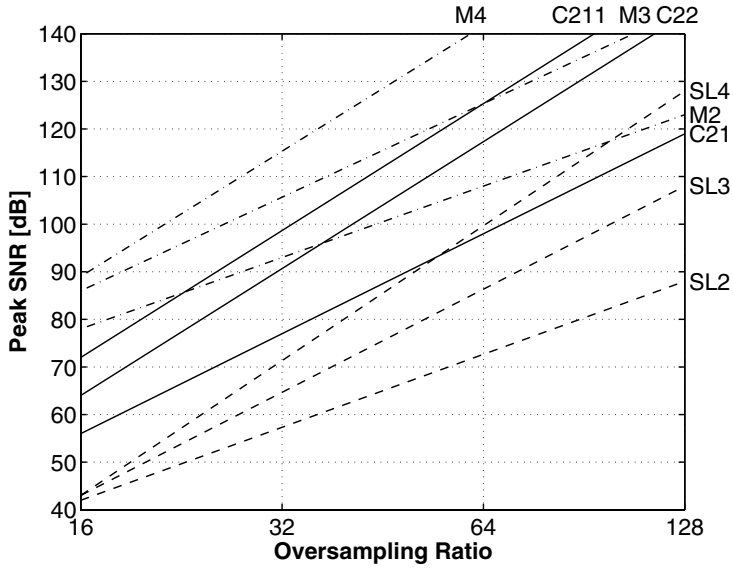



Figure 3.29: $SNR_p$ vs. oversampling ratio for different traditional Σ-Δ modulator topologies. SLi: i-th order single-loop modulator; Mi: i-th order 4-bit single-loop modulator; Cijk: Cascaded modulator i-j-k.

### 3.4.4 Performance Comparison of Traditional Σ-Δ Topologies

Fig. 3.29 shows the simulated peak SNR versus the oversampling ratio for different traditional Σ-Δ modulator topologies. Generally speaking, the multi-bit modulator offers the best performance, but suffers from the nonlinearity problem of the feedback DAC. The cascaded modulator offers good performance, but it requires high-performance building blocks. The single-loop single-bit modulator is the worst one in terms of performance, however it is not sensitive to the non-idealities of the building blocks.

## 3.5 Conclusion

Firstly, the basic principle of the ADC is introduced in this chapter. By introducing oversampling and noise-shaping concepts, the basic operation principle of the Σ-Δ ADC is presented. Then the performance metrics of the Σ-Δ ADC are explained.

A systematic study on the traditional single-loop, cascaded and multibit Σ-Δ modulator topologies has been presented in this chapter. The advantages, disadvantages and optimized parameters are also given for each topology.

In next chapter, the low-power low-voltage Σ-Δ ADC design in nanometer CMOS technologies is presented. The design of low-power low-voltage Σ-Δ ADC in nanometer CMOS technologies can be classified into two approaches: the circuit level approach and the system level approach. The circuit level approach focuses on the building block design suitable for nanometer CMOS technologies. Trade-offs are often made in this approach. The next chapter will deal with this topic.

Chapter 4

# Low-Power Low-Voltage Σ-Δ ADC Design in Nanometer CMOS: Circuit Level Approach

## 4.1 Introduction

In this chapter, the low-power low-voltage Σ-Δ ADC design in nanometer CMOS technologies by the circuit level approach is introduced. At the circuit level, the low-voltage building blocks suitable for nanometer CMOS technologies are analyzed and presented according to the requirement of nanometer CMOS technologies. At the same time, low-power is also emphasized in the design of the building blocks.

In recent years, portable electronics, such as personal wireless communication devices, digital cameras, personal audio devices, etc., find booming markets. Powered by batteries, their supply voltage is often limited. The battery lifetime is of great importance for these devices. All these factors address the requirements of low-voltage low-power system building blocks. At the same time, mainly driven by the digital circuits, the feature size of the transistors is continuously scaled-down. The operating voltage is decreased as a consequence of the shrinking size to avoid transistor breaking-down, forcing the design to work at lower supply voltage. These factors make the low-voltage low-power circuits a hot topic. However, the decreased supply voltage restricts the signal swing in circuits and brings some difficulties for analog designs [San98]. In low-voltage environments, the transistor characteristics degrade and some circuit techniques can not be used any more, rendering the low-voltage design different from the traditional circuit design technique.

As an important building block, ADCs are widely used in various systems. The movement of digital circuits into nanometer technology causes strong demands for low-voltage low-power ADCs. Among different ADC topologies, the Σ-Δ ADC efficiently trades speed for accuracy, providing an effective way to implement high resolution ADCs without stringent matching requirement or calibration in a low-voltage environment. By means of oversampling and noise-shaping, the Σ-Δ ADC transfers most of the signal processing tasks to the digital domain where the power consumption can be drastically reduced by the technology scaling-down and supply voltage decreasing. Meanwhile, the use of an intrinsically linear single-bit quantizer exempts the stringent matching requirement, which is power hungry. For high resolution ADCs, the Σ-Δ ADC is more power-effective and robust compared to other architectures.

While moving into nanometer CMOS technologies, for low-voltage low-power designs, certain advantages can be gained. On the other hand, some disadvantages are

also foreseen. Limited by the transistor breakdown voltage, the rated supply voltage is low in nanometer CMOS technologies. As a result, the threshold voltage of the transistor is low too, which is advantageous to implement low-voltage applications. Normally no specially designed low-voltage circuits are needed, which simplifies the circuits and lowers the power consumption. Many low-power low-voltage $\Sigma$-$\Delta$ ADCs reported to date are implemented in deep-submicron CMOS technologies [Rab97], [Des01]. The common point of these works is that they work on a reduced supply voltage that is lower than their rated supply voltage. To sufficiently drive the switches, clock bootstrapped driving circuits are employed. In this case, some internal node voltages might be higher than the supply voltage. Damaging the transistor or having a reliability problem is a potential risk. Low-$V_T$ technologies can also be used. However this needs extra processing steps and is expensive. Some designs [Pel98] were implemented with the switched-opamp technique [Ste94], which solves the driving problem of the sampling switches in the succeeding stage. But the first sampling switch still cannot be driven sufficiently. With nanometer technologies, the threshold voltage is reduced as the supply voltage is decreased. This makes the driving of the switches possible without bootstrapping circuits. Hence, nanometer technologies help to reduce the power consumption further in a low-voltage environment. For the digital part of the converter, the shorter the transistor length, the less power is consumed. That is the driving force of the technology scaling-down. Generally speaking, in terms of low-power low-voltage, it is advantageous indeed to move into nanometer technologies.

In this chapter, the low-voltage low-power OTA design is introduced firstly. A gain-enhanced current mirror OTA with high power-efficiency is introduced. By using this OTA topology, a low-voltage low-power $\Sigma$-$\Delta$ ADC is then designed. It is meaningful to explore the possibilities of implementing high performance $\Sigma$-$\Delta$ modulators in a standard digital process in nanometer technologies. Presented in this chapter, a single-loop third-order switched-capacitor $\Sigma$-$\Delta$ modulator implemented in a standard digital 90-nm CMOS technology is demonstrated. Finally extensive measurements on power supply rejection ratio and low-frequency noise are performed and the measurement results are discussed in this chapter.

## 4.2 Low-Voltage Low-Power OTA Design

The movement of CMOS technology into nanometer CMOS technologies is getting faster in recent years. As a consequence, the power supply voltage drops below 1 Volt earlier than expected. On the other hand, portable electronics with low-voltage operation find big markets. All these drive the supply voltage of CMOS circuits into the sub-one Volt era. However, the threshold voltage is not reduced proportionally with the supply voltage. Thus, the threshold voltage is becoming a restraint for many analog circuits. Some special techniques are used to overcome the size of the threshold voltage, e.g. floating gate transistors [RA95], bulk-driven transistors [Bla96] and low threshold transistors provided by the foundry. They suffer from several drawbacks or need special fabrication steps, which increases the cost. It is preferred to implement low-voltage circuits using a standard CMOS technology.

Being the most important building block in analog circuits, the amplifier faces another

difficulty in the low-voltage design, providing high gain and high output swing with low-power consumption. In nanometer CMOS technologies, the intrinsic gain of the transistor is usually lower than 20 dB. The usual way to boost the gain, cascoding of transistors, is not available in low-voltage design due to its output swing limitation. Alternatively, cascading transistor, i.e. the multi-stage amplifier, is adopted. However, a cascade structure, which boosts gain with more than one amplifying stage, normally increases the power consumption and needs frequency compensation. Besides, there are also other methods to enhance the OTA gain, e.g. positive feedback [See98] and a use of replica amplifier [Yu93]. Among all these methods, a rather high amount of power and chip area are used for the gain enhancement circuitry.

## 4.2.1 Gain Enhanced Current Mirror OTA Design

### 4.2.1.1 Low-Power Low-Voltage Amplifier Design Strategy

In low-voltage designs, the main consideration is to maintain the output swing as high as possible. The rail-to-rail output swing is preferred, which means no cascoding transistors can be used in the output stage. On the other hand, for minimum power consumption, the number of current branches should be minimized, and class AB operation is preferred. The multi-stage amplifier, which spends power on driving the compensation capacitances, is not competitive compared with the single-stage amplifier in terms of power efficiency. These constraints lead to the most power-efficient solution, single-stage amplifier without cascoding. The current mirror amplifier fulfills the above requirements, making it a good candidate for a low-power low-voltage amplifier.

### 4.2.1.2 Current Mirror Amplifier

As mentioned before, the current mirror OTA, shown in Fig. 4.1, is a good candidate for a low-voltage OTA topology. The minimum supply voltage of the current mirror OTA is only a transistor threshold voltage plus three times the transistor saturation voltage, as shown in equation (4.1).

$$V_{dd_{min}} = V_{GS} + 2V_{DS_{sat}} = V_T + 3V_{DS_{sat}} \tag{4.1}$$

The DC gain of the current mirror OTA is given by (4.2) below:

$$A_0 = gm_1\ B\ r_{o3} = \frac{2\ I_{D1}}{(V_{GS1} - V_T)} \frac{B}{\lambda_3\ I_{D3}} \tag{4.2}$$

where $\lambda$ is the channel length modulation coefficient and B is the current ratio (4.3) of the current mirror.

$$I_{D3} = B\ I_{D1} \tag{4.3}$$

Finally the gain of the current mirror OTA can be expressed by (4.4).

$$A_0 = \frac{2}{(V_{GS1} - V_T)\lambda_3} \tag{4.4}$$

In nanometer CMOS technology, the effect of channel length modulation becomes more significant. As a result, the output resistance is quite low and thus the DC gain of the current-mirror OTA is normally below 30 dB, which is not sufficient for most applications.

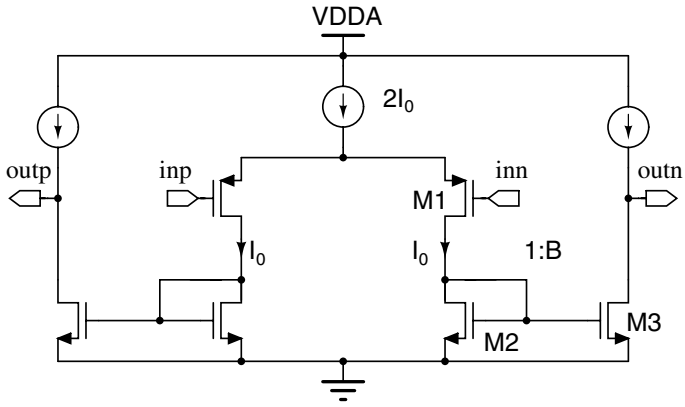



Figure 4.1: Schematic of the current mirror OTA.

#### 4.2.1.3 Gain Enhancement by Current Shunt

From equation (4.4) one can clearly see that in the current mirror amplifier, the transconductance is boosted B times; at the same time, the output resistance is reduced B times due to the amplification of the biasing current. So the overall gain of the OTA still remains unchanged, which is the same as for a single transistor.

If the biasing current of the output transistors can be made smaller and still maintain the same current transfer function, the overall gain of the OTA can be increased. This is the basic idea to enhance the gain [Ste91]. Shown in Fig. 4.2, two current sources are placed in parallel with the diode-connected transistors and shunt part of the current from the transistors. Assuming the current source carries a portion $k$ of the current of transistor M1, the gain of the OTA can be expressed as:

$$A_{en} = gm_1 \; B \; r_{o3} = \frac{2 \; I_{D1}}{(V_{GS1} - V_T)} \; \frac{B}{\lambda_3 \; I_{D3}} \tag{4.5}$$

Now the biasing current of M3 is:

$$I_{D3} = B \; (1 - k) \; I_{D1} \tag{4.6}$$

And finally the gain of the OTA is given by

$$A_{en} = \frac{1}{1 - k} \; \frac{2}{(V_{GS1} - V_T)\lambda_3} = \frac{A_0}{1 - k} \tag{4.7}$$

From equation (4.7) it can be seen that the OTA gain is enhanced $\frac{1}{1-k}$ times. The enhancement can be adjusted by changing the $k$ factor. Apparently the $k$ factor could not be bigger than 1, otherwise the total current would be drawn by it and pull the diode connecting node towards the ground.

In practice, the shunt current source can be mirrored from the differential pair tail current source. Then the gain-enhancement is completely defined.

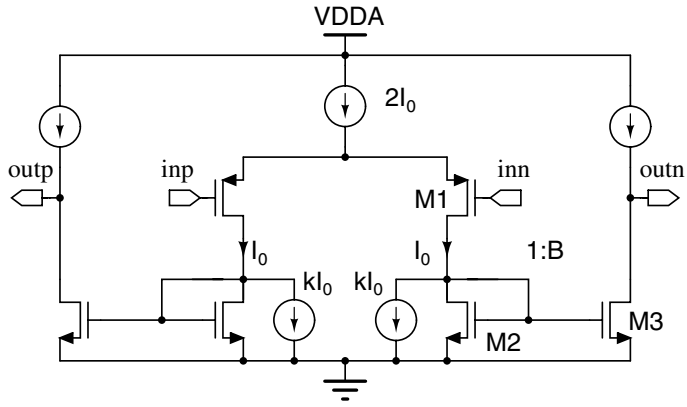



Figure 4.2: Gain enhancement by current shunting in the current mirror OTA.

#### 4.2.1.4 Practical Design Considerations

Practically, the gain enhancement is restricted by several factors.

The first concern is the frequency response problem. Using this technique will result in the increased impedance of the internal node A. The non-dominate pole frequency will be pulled down and hence the phase margin will be reduced too. Shown in Fig. 4.3, the total parasitic capacitance in node A is presented by $C_C$ and the parasitic capacitance in node OUT together with the load capacitance is presented by $C_L$. Then the non-dominate pole in node A is given by (4.8):

$$P_{nd} = \frac{gm_2}{2\pi C_C} = \frac{2(1-k)I_1}{2\pi C_C(V_{GS2} - V_T)} \tag{4.8}$$

The gain bandwidth product (GBW) of the OTA can be expressed by (4.9)

$$GBW = \frac{B\ gm_1}{2\pi C_L} = \frac{2\ B\ I_1}{2\pi C_L(V_{GS1} - V_T)} \tag{4.9}$$

To maintain a reasonably safe phase margin, the non-dominate pole has to be placed more than 3 times of the GBW [Lak94]. If the overdrive voltages of the transistors are same, then the following criteria can be drawn:

$$k \leq 1 - 3B\frac{C_C}{C_L} \tag{4.10}$$

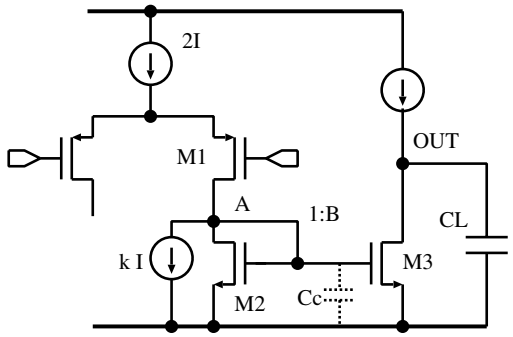



Figure 4.3: Parasitic capacitance and internal pole in the gain-enhanced current mirror OTA.

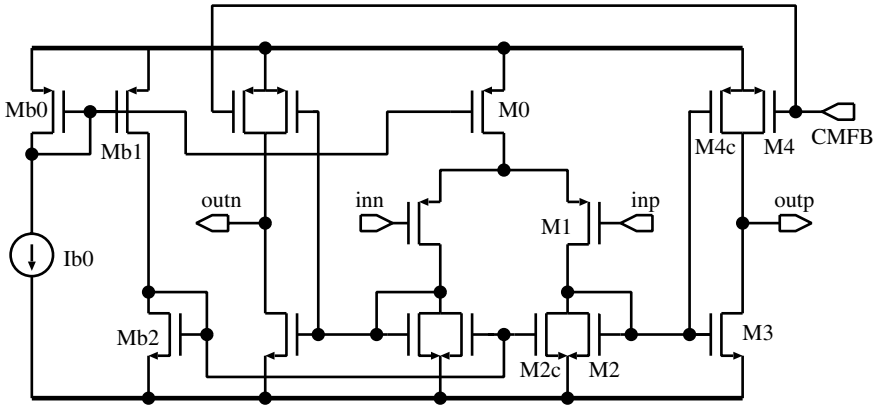



Figure 4.4: Complete circuits of the gain-enhanced current mirror OTA.

Equation (4.10) shows the maximum gain enhancement that can be achieved. The smaller $\frac{C_C}{C_L}$ ratio, the more gain enhancement can be achieved. The larger the capacitance load is, the higher gain can be reached.

Secondly, in practice the matching of current sources determines the total gain enhancement. To ensure good matching between the tail current source and shunt current source, both of them are mirrored by the same reference current source. The matching between these current mirrors determines the overall effect of gain enhancement. To ensure good matching, transistors should be properly sized. Trade-offs are normally made between the frequency response and gain enhancement here.

### 4.2.2 A Test Gain-Enhanced Current Mirror OTA

Fig. 4.4 shows the complete implementation of the gain-enhanced current mirror OTA in a 0.25-$\mu$m CMOS technology. The load capacitance is 18 pF, which is much bigger than the parasitic capacitance $C_C$. The $k$ factor can be chosen slightly smaller than one. Taking the transistor matching into consideration, the $k$ factor was set to 0.9 and B factor was 3. The shunt current source was mirrored by the main reference current source.

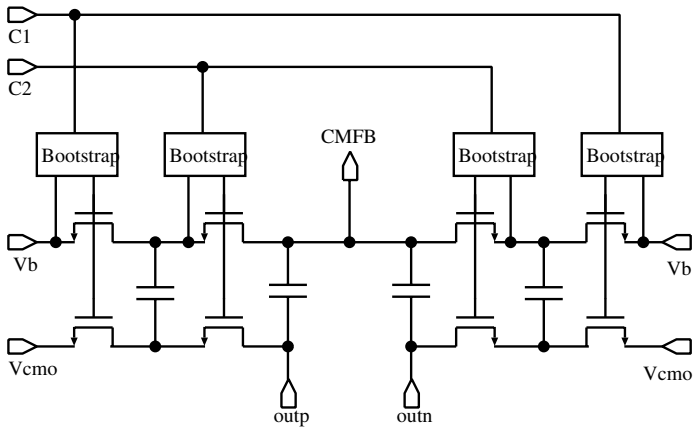



Figure 4.5: The switched-capacitor CMFB circuit.

#### 4.2.2.1 Class AB Operation

For power efficiency consideration, the class AB output stage is preferred. The class AB operation is implemented with the so-called push-pull output stage consisting of transistor M3 and M4c. Note that under small signal conditions, transistor M4c works in sub-threshold region and conducts a very small amount of current. While a large output current is demanded, M4c will turn on and source large amounts of current to drive the load capacitance hence increasing the positive slew rate.

#### 4.2.2.2 CMFB circuit

The common-mode feedback(CMFB) circuit is implemented by switched-capacitor circuits, shown in Fig. 4.5. Since the supply voltage is insufficient to operate the switch transistor, bootstrapped switches [Abo99] are used to ensure low-voltage operation, shown in Fig. 4.6. Care should be taken that the GBW of the common-mode loop should be greater than that of differential loop. This can be done by making $g_{m4}$ greater than $B \cdot g_{m1}$.

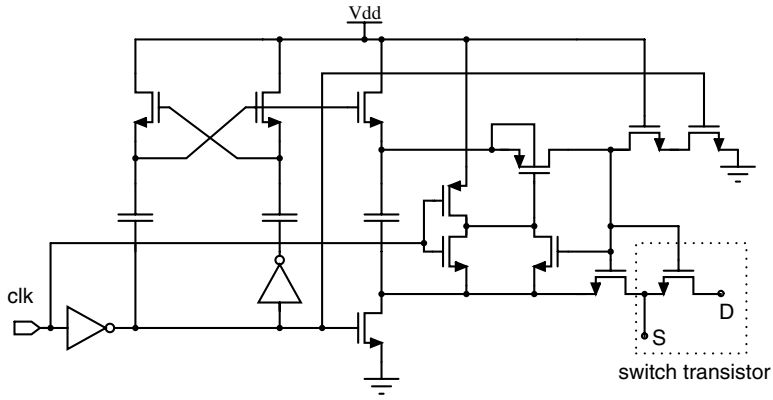



Figure 4.6: Schematic of the clock boosting circuit.

### 4.2.3 Implementation and Measurement Results

The proposed OTA topology was implemented with a standard 0.25-$\mu$m CMOS technology with $V_{Tn}$=0.54 V and $V_{Tp}$=-0.58 V. The chip micrograph is shown in Fig. 4.7. The active core area is $100 \times 60 \mu m^2$. The open-loop frequency response was measured with a 500-$\mu$V RMS input signal and a 15-pF load capacitance. An off-chip unity-gain buffer was used to buffer the output and drive the network analyzer. The input capacitance of the buffer together with the wiring capacitance was estimated to be around 3 pF. So the total load capacitance was about 18 pF. Fig. 4.8 shows the schematics for the unity-gain transient response measurement setup. The same buffer was used in the transient response measurement. All measurements were made single-endedly.

Fig. 4.9 shows the open-loop frequency response. The OTA achieves a GBW of 1.2 MHz while driving an 18-pF load and consumes about 8-$\mu$W power at a 0.8-V supply voltage. The phase margin is about 60 degrees. The power consumption of the biasing circuits and the CMFB circuits are not included in the result. The OTA stays functional while supply voltage drops to 0.7 V, but the performance is degraded considerably. Fig. 4.10 shows the transient response measurement result. The upper trace is the input signal and the one below is the output signal. The rising-time and falling-time is 2.7 $\mu$s and 2.4 $\mu$s respectively while a 600-$mV_{pp}$, 50-kHz input signal is applied.

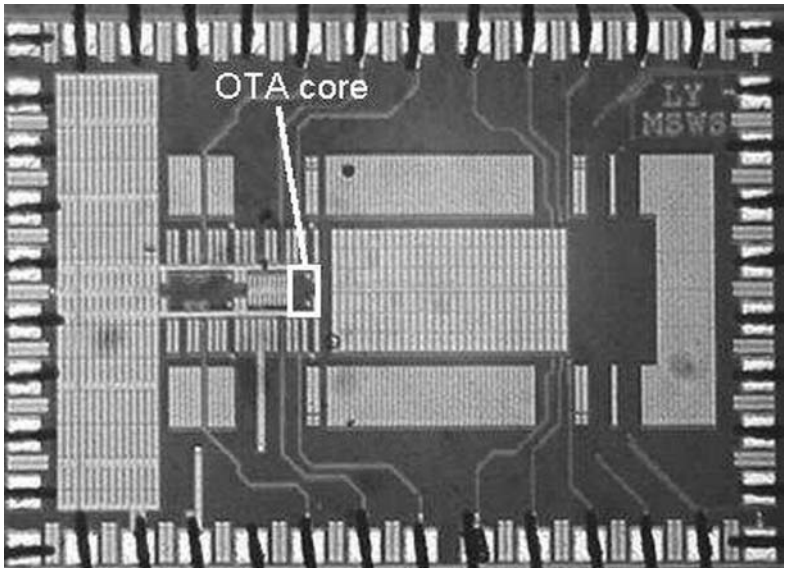



Figure 4.7: Chip micrograph of the OTA.

The supply current increases to 12 $\mu$A, which shows the class AB operation. Table 4.1 summarizes the measured OTA performance parameters.

### 4.2.4 Two-Stage OTA Design

When moving into nanometer CMOS technologies, the problem faced is the reduced signal swing and insufficient gain of the amplifiers. As mentioned in Chapter 3, these problems force designers go to cascading transistors instead of cascoding. Cascading transistors means that more than one amplifier stage are adopted in the whole amplifier. Consequently, the system is no longer a first-order system and the frequency compensation is needed. In this section, two-stage amplifiers are introduced and their settling performance, the important performance for switched-capacitor circuits, is analyzed.

Compared to the single-stage OTA, the two-stage OTA has higher gain. However, having more poles and zeros in the transfer function, the two-stage OTA shows more complex settling behavior. Two structures of two-stage OTA having good settling performance are introduced in this section. By analyzing the settling behavior of the third-order system, a set of poles and zeros parameters are extracted. A design procedure for minimum settling time of these two OTAs is described. Finally two design examples for minimum settling time are presented. These high-speed OTAs are suitable for high-speed switched-capacitor applications.

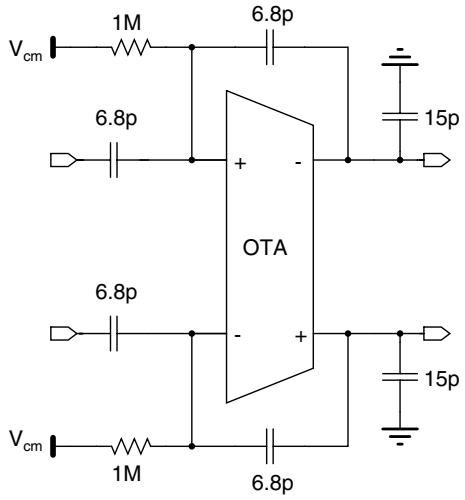



Figure 4.8: Transient response measurement setup for the gain-enhanced current mirror OTA.

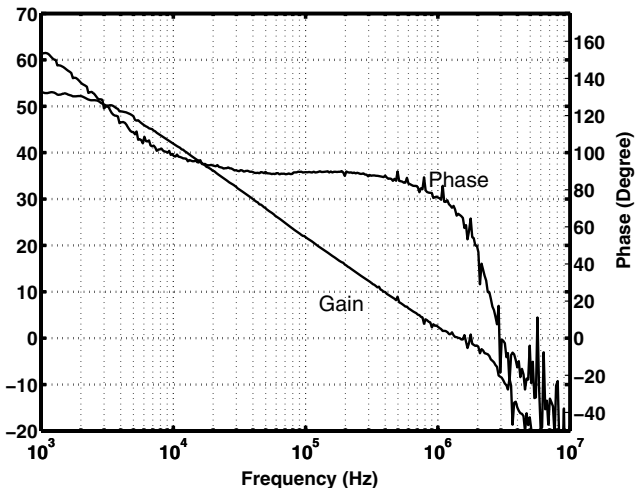



Figure 4.9: Measured frequency response of the gain-enhanced current mirror OTA.

Table 4.1: Measured OTA performance parameters.

| | | |
|---|---|---|
| Supply voltage | 0.8 | V |
| Static supply current | 9.9 | $\mu$A |
| Static power consumption | 8 | $\mu$W |
| DC gain | 52 | dB |
| Phase margin | 60 | Degree |
| GBW | 1.2 | MHz |
| Single-ended output swing | 0.6 | V |
| Slew rate | 0.2 | V/$\mu$S |
| Load capacitance | 18 | pF |
| Active die area | 0.006 | mm$^2$ |

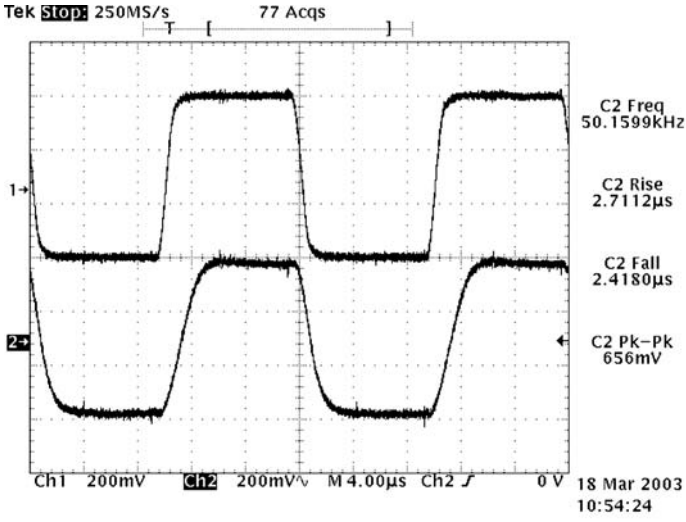



Figure 4.10: Measured transient response of the gain-enhanced current mirror OTA.

#### 4.2.4.1 Introduction of the Two-Stage OTA

Speed and accuracy are two of the most essential properties of analog circuits. For OTAs the settling time and DC gain are direct reflections of speed and accuracy. While pursuing the high specifications of analog circuits, fast settling and high DC gain of OTAs are often demanded at the same time. Especially in switched-capacitor circuits, settling performance is the most parameter of concern as the settling time determines the maximum clock frequency while the DC gain of the OTA determines the output accuracy [Yan90].

For settling performance of a system, the single-pole system has the simplest settling behavior. Therefore, the single-stage OTA, which can be regarded as a first-order system, is the simplest OTA structure compared to the multi-stage OTA in terms of settling performance. The GBW of the amplifier determines the settling time solely. However, the DC gain that one stage can reach is limited. To achieve high DC gain with a single amplifier stage, some techniques are adopted, such as cascoding, gain-boosting and negative conductance compensation. However, the gain-boosting technique suffers from the degrading of high-frequency performance and has the potential to be unstable. The negative conductance compensation heavily relies on the transistor matching. Of all these techniques, cascoding is widely used, as it doesn't degrade the settling performance.

With the semiconductor processing development, the feature size of the transistor is continuously shrinking, making it possible to reach even higher unit-gain frequencies of the transistor. However, the intrinsic gain of the transistor, $g_m \times r_o$, is also degrading. This makes the single-stage amplifier gain even lower. At the same time, the power-supply voltage is decreasing, making the output swing lower [Gul98]. For the widely used cascode structure, the output swing is limited as at least 4 transistors are in stack. These problems force the analog designer to switch to multi-stage OTAs.

The main drawback of the multi-stage OTA is that compensation is needed to avoid instability. Thus more poles and zeros are introduced and the settling time no longer depends on one pole frequency. This makes the design of the high-speed multi-stage OTA more difficult.

In the next section, the settling behavior of the third-order system is analyzed and an optimized set of system parameters is obtained. According to the obtained system parameters, a design method of optimizing the settling time is proposed. Finally, a design example is reported.

#### 4.2.4.2 Settling Behavior Analysis of Two-Stage OTA Topologies

**Ahuja style compensated OTA** The most popular two-stage OTA is the Miller compensated OTA. Moving the compensation capacitance to the source of the cascading transistor, the so-called Ahuja style compensated two-stage OTA is obtained, shown in Fig. 4.11 [Ahu83]. Since the output amplitude of the first stage is small, a telescopic cascode stage providing high voltage gain is chosen. The second stage is a common-source stage providing high output swing. The minimum supply voltage of the two-stage OTA is a transistor threshold voltage plus four times the transistor satu-

ration voltage, as shown in equation (4.11).

$$V_{dd_{min}} = V_{GS} + 3V_{DS_{sat}} = V_T + 4V_{DS_{sat}} \tag{4.11}$$

The DC gain of the OTA is:

$$A = \left(\frac{g_m}{g_{DS}}\right)^3 \tag{4.12}$$

The gain of the two-stage OTA is third-order power of the intrinsic gain of the transistor. For switched-capacitor applications, the gain is enough for most applications. Furthermore, the two-stage OTA can offer rail-to-rail output swing, which is essential for low-voltage designs. However, the dynamic behavior of the two-stage OTA, which is often important in switched-capacitor applications, is more complex as more low-frequency poles and zeros in the transfer function. Compensation is needed to ensure closed-loop stability.

Of all the nodes, only node $N_2$ and output node are high impedance nodes. The poles and zeros formed by these two nodes are much smaller than the other nodes. To simplify the analysis, only the parasitic capacitances of these two nodes are taken into consideration. In real situations, the OTA always operates in closed-loop configurations, so the following analysis is based on a closed-loop configuration.

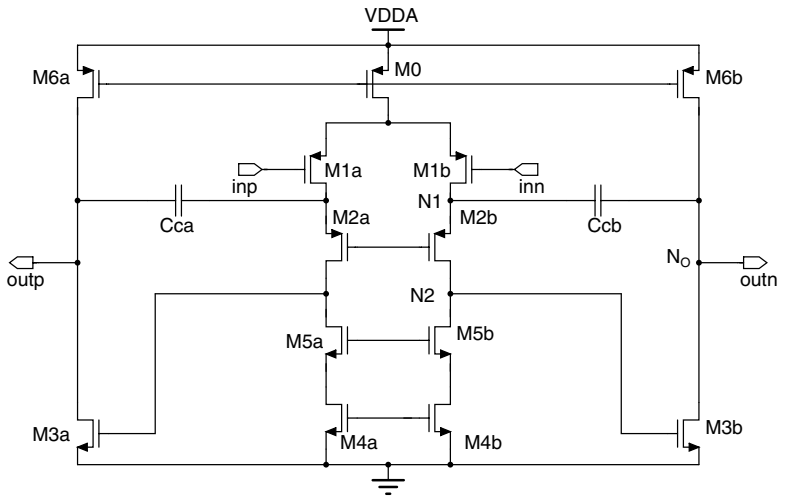



Figure 4.11: Schematic of the Ahuja style compensated two-stage OTA.

Fig. 4.12 shows the small-signal equivalent circuit for pole and zero analysis. In the equivalent circuit schematic, $C_1$ represents the parasitic capacitance of node $N_1$, $C_2$ represents the parasitic capacitance of node $N_2$ and $C_L$ represents the parasitic capacitance of node $N_o$ together with the load capacitance; $g_{m1}$, $g_{m2}$ and $g_{m3}$ represent the transconductance of transistor M1, M2 and M3 respectively; $V_1$, $V_2$ and $V_o$ represent the voltage of node $N_1$, $N_2$ and $N_o$. To simplify the expression, the bulk transconductance and output conductance of all transistors are considered as zero. The node

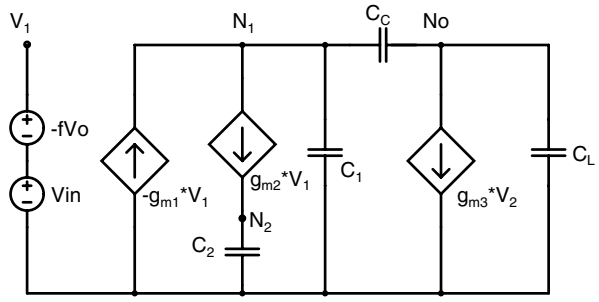



Figure 4.12: Small-signal equivalent circuit of the Ahuja style compensated two-stage OTA.

equations and the transfer function are:

$$\begin{cases} V_o s C_L + g_{m3} V_2 + (V_o - V_1) s C_C = 0 \\ (V_o - V_1) s C_C + g_{m2} V_1 + g_{m1}(V_{in} - f V_o) + V_1 s C_1 = 0 \\ V_2 s C_2 - g_{m2} V_1 = 0 \end{cases} \tag{4.13}$$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{\frac{g_{m1}}{C_2 C_T^2}(s^2 C_C C_2 - g_{m2} g_{m3})}{s^3 + \frac{g_{m2}(C_L + C_C) - f g_{m1} C_C}{C_T^2} s^2 + \frac{g_{m2} g_{m3} C_C}{C_2 C_T^2} s + \frac{f g_{m1} g_{m2} g_{m3}}{C_2 C_T^2}} \tag{4.14}$$

where $C_T^2 = C_1 C_L + C_1 C_C + C_L C_C$.

**Settling behavior of Ahuja style compensated OTA** In order to investigate the settling behavior, the transfer function of the Ahuja style OTA is converted into the following standard third-order system transfer function:

$$\begin{aligned} H_(s) &= \frac{k(z^2 - s^2)}{(s + \omega_{CL})(s^2 + 2\zeta\omega_n s + \omega_n^2)} \\ &= \frac{k(\gamma^2 \zeta^2 \omega_n^2 - s^2)}{(s + \alpha\zeta\omega_n)(s^2 + 2\zeta\omega_n s + \omega_n^2)} \end{aligned} \tag{4.15}$$

where $z = \gamma\zeta\omega_n$ and $\omega_{CL} = \alpha\zeta\omega_n$.

There are four system parameters, $\alpha$, $\gamma$, $\zeta$ and $\omega_n$ in the transfer function. The $\omega_n$ is called natural frequency and $\zeta$ is called damping factor. The physical explanation of these four parameters is found in Fig. 4.13.

Now we try to find the relationship between the settling time and these four parameters. By applying a step signal to this system, which is equivalent to multiply the transfer function by 1/s, the Laplace transform of the unit step, the response of this system in frequency domain is obtained. After taking the reverse Laplace transform, the time

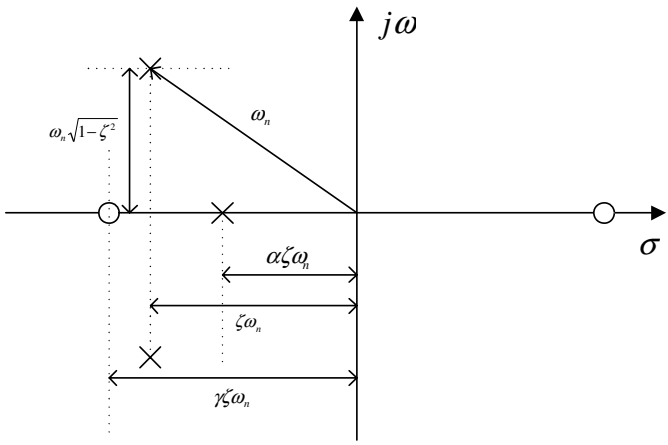



Figure 4.13: Poles and zeros plot of a third-order system.

domain step response of the system is obtained [Fel97]:

$$\begin{aligned} R(t) &= A_{CL}\Big\{1 - \frac{\gamma^2-\alpha^2}{\gamma^2(1-2\alpha\zeta^2+\alpha^2\zeta^2)}e^{-\alpha\zeta\omega_n t} - \frac{\alpha e^{-\zeta\omega_n t}}{\gamma^2(1-2\alpha\zeta^2+\alpha^2\zeta^2)} \\ &\quad \Big[(\alpha - 2\zeta^2\gamma^2 + \alpha\zeta^2\gamma^2)cos(\omega_n t\sqrt{1-\zeta^2}) \\ &\quad + \frac{(1-\alpha\zeta^2+\zeta^2\gamma^2-2\zeta^4\gamma^2+\alpha\zeta^4\gamma^2)}{\zeta\sqrt{1-\zeta^2}}sin(\omega_n t\sqrt{1-\zeta^2})\Big]\Big\} \end{aligned} \tag{4.16}$$

where $A_{CL}$ denotes the closed-loop gain.

$$E(t) = \frac{R(\infty) - R(t)}{R(\infty)} \tag{4.17}$$

is the settling error to the final value of time $t$. Then we have:

$$\begin{aligned} E(t) &= \Big\{\frac{\gamma^2-\alpha^2}{\gamma^2(1-2\alpha\zeta^2+\alpha^2\zeta^2)}e^{-\alpha\zeta\omega_n t} + \frac{\alpha e^{-\zeta\omega_n t}}{\gamma^2(1-2\alpha\zeta^2+\alpha^2\zeta^2)} \\ &\quad \Big[(\alpha - 2\zeta^2\gamma^2 + \alpha\zeta^2\gamma^2)cos(\omega_n t\sqrt{1-\zeta^2}) \\ &\quad + \frac{(1-\alpha\zeta^2+\zeta^2\gamma^2-2\zeta^4\gamma^2+\alpha\zeta^4\gamma^2)}{\zeta\sqrt{1-\zeta^2}}sin(\omega_n t\sqrt{1-\zeta^2})\Big]\Big\} \end{aligned} \tag{4.18}$$

The analytical equation of settling error and system parameters has been found. However, this equation is too complex to see the relationship clearly. So it is explored by numerical calculations. With the help of the mathematic software tool, the settling error

curves with different system parameter values can be drawn. For given settling error and time, the parameters can be found easily. All the figures are drawn versus time normalized to $\omega_n$. Fig. 4.14 shows the settling error curves of the Ahuja style OTA for

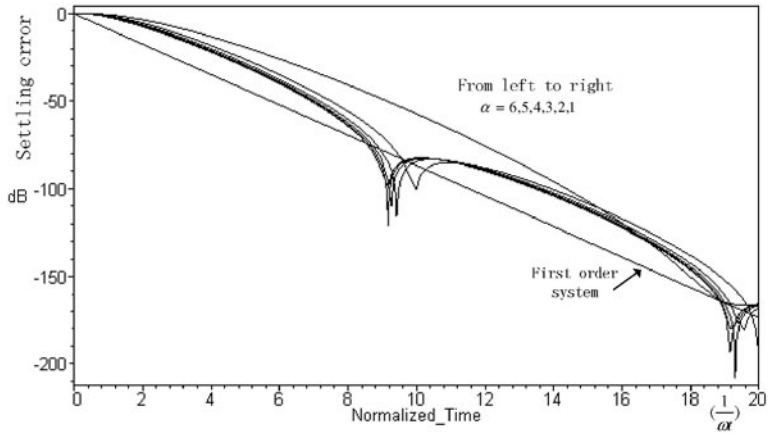



Figure 4.14: Normalized settling time of the Ahuja style OTA for different $\alpha$ value ($\zeta$=0.95 and $\gamma$=4).

different parameters. The minimum settling time is achieved when $\alpha > 2$, $\zeta = 0.95$ and $\gamma > 4$. From the curves one can clearly see that for a -80-dB settling error, the settling time of the Ahuja style OTA is about 9 times $1/\omega_n$, which is comparable to the first order system with the same $\omega_n$.

**Improved Ahuja style compensated OTA** By moving the compensation capacitance to the source of the load transistor, a new structure, the improved Ahuja style compensated two-stage OTA, is formed, shown in Fig. 4.15. The small signal equivalent circuits are shown in Fig. 4.16.

Again, we have the node equations and the transfer function:

$$\begin{cases} V_o sC_L + g_{m2}V_2 + (V_o - V_1)sC_C = 0 \\ (V_1 - V_o)sC_C + g_{m2}V_1 + V_1 sC_1 = 0 \\ V_2 sC_2 - g_{m2}V_1 + g_{m1}(V_{in} - fV_o) = 0 \end{cases} \tag{4.19}$$

Then the transfer function of the improved Ahuja style compensated two-stage OTA is:

$$\frac{V_o(s)}{V_{in}(s)} = \frac{\frac{g_{m1}g_{m3}(C_C+C_1)}{C_2C_T^2}(s + \frac{g_{m2}}{C_C+C_1})}{s^3 + \frac{g_{m2}}{C_2C_T^2}(C_2C_1 + C_2C_C)s^2 + As + \frac{f}{C_2C_T^2}g_{m1}g_{m2}g_{m3}} \tag{4.20}$$

where $C_T^2 = C_1C_L + C_1C_C + C_LC_C$ and $A = \frac{1}{C_2C_T^2}[fg_{m1}g_{m3}(C_C+C_1) + g_{m2}g_{m3}C_C]$.

It can be seen that there is only one zero in the transfer function of the improved Ahuja style OTA.

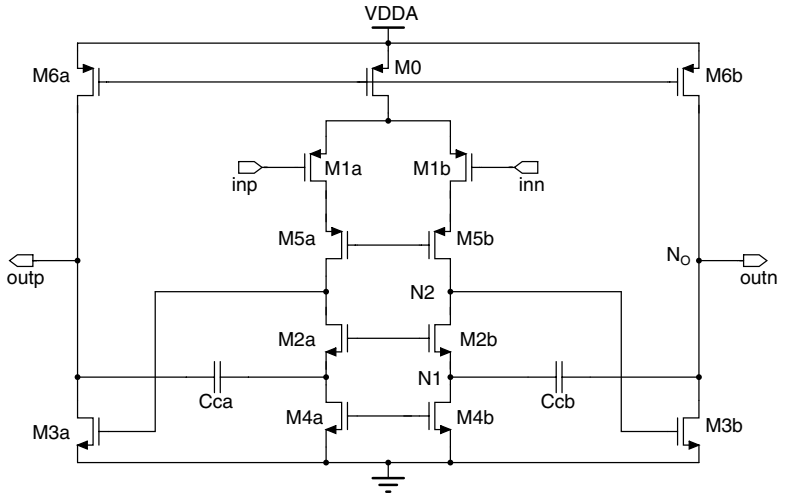



Figure 4.15: Schematic of the improved Ahuja style compensated two-stage OTA.

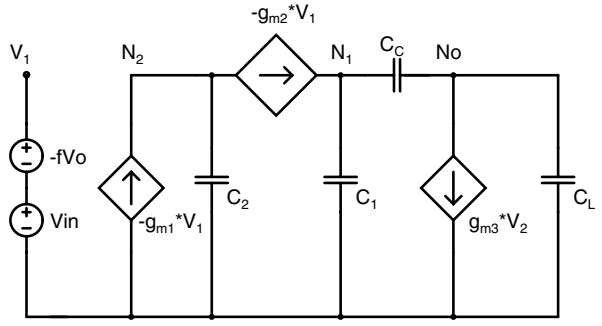



Figure 4.16: Small-signal equivalent circuit of the improved Ahuja style compensated two-stage OTA.

**Settling performance of the improved Ahuja style compensated OTA** The transfer function of the improved Ahuja style compensated OTA can be simplified as:

$$H(s) = \frac{k(s+z)}{(s+\omega_{CL})(s^2+2\zeta\omega_n s+\omega_n^2)} \tag{4.21}$$

Based on this equation, using the same method, the settling error of the improved Ahuja style compensated OTA can be calculated as:

$$\begin{aligned} E(t) \quad = \quad & \left\{ \frac{\gamma-\alpha}{\gamma(1-2\alpha\zeta^2+\alpha^2\zeta^2)} e^{-\alpha\zeta\omega_n t} - \frac{\alpha e^{-\zeta\omega_n t}}{\gamma(1-2\alpha\zeta^2+\alpha^2\zeta^2)} \right. \\ & \left[ (2\gamma\zeta^2-1-\alpha\zeta^2\gamma) cos(\omega_n t\sqrt{1-\zeta^2}) \right. \\ & \left. \left. + \frac{(2\gamma\zeta^3-\alpha\gamma\zeta^3+\alpha\zeta-\zeta-\gamma\zeta)}{\sqrt{1-\zeta^2}} sin(\omega_n t\sqrt{1-\zeta^2}) \right] \right\} \end{aligned} \tag{4.22}$$

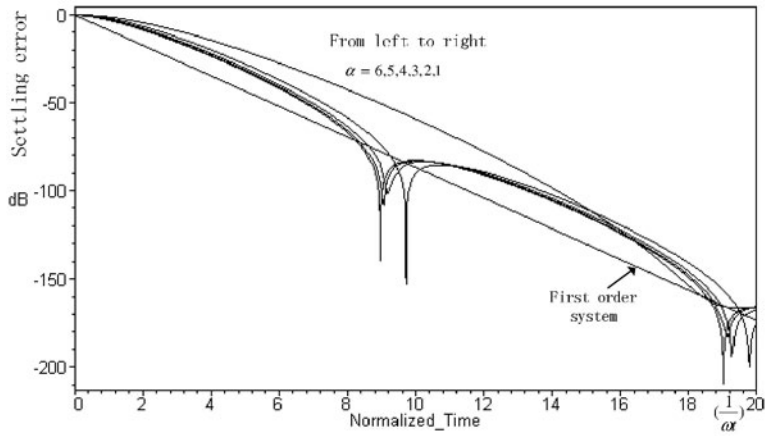



Figure 4.17: Normalized settling time of the improved Ahuja style OTA for different $\alpha$ value ($\zeta$=0.95 and $\gamma$=4).

Fig. 4.17 shows the settling error curves of the improved Ahuja style OTA for different parameters. The parameters to achieve the minimum settling time are the same as the Ahuja style OTA.

#### 4.2.4.3 Optimization for Minimum Settling Time

From the previous analysis, we already have the system parameters for desired settling time and settling error. Now the problem is how to design the physical sizes of the transistors and the biasing currents.

**Optimization procedure of the Ahuja style OTA** The optimization of the Ahuja style two-stage OTA can start from the design equations extracted by matching the

transfer function of the OTA with equation (4.15). For simplicity reason, the $\gamma$ is not included in these equations.

$$\begin{cases} (2+\alpha)\zeta\omega_n = \frac{g_{m2}(C_L+C_C)-fg_{m1}C_C}{C_1C_L+C_1C_C+C_LC_C} \\ \omega_n^2(1+2\alpha\zeta^2) = \frac{g_{m2}g_{m3}C_C}{C_2(C_1C_L+C_1C_C+C_LC_C)} \\ \alpha\zeta\omega_n^3 = \frac{fg_{m1}g_{m2}g_{m3}}{C_2(C_1C_L+C_1C_C+C_LC_C)} \end{cases} \tag{4.23}$$

These equations reveal the relationship between the device parameters and the system parameters. Among all the parameters, the system parameters $\alpha$, $\gamma$, $\zeta$, and $\omega_n$ are known. The load capacitance $C_L$ is known too. The compensation capacitance $C_C$ can also be determined before hand. The capacitances $C_1$ and $C_2$ are parasitic capacitances of the node $N_1$ and $N_2$ respectively and they can be related to the transistor sizes. So $C_1$, $C_2$ and all the transconductance can be expressed by transistor sizes. Theoretically, these equations can be solved and the sizes of the transistors can be obtained. However, practically, these equations are too complex to be solved. Again, a numerical solution is taken to find the right sizes of the transistors.

**Optimization procedure of the improved Ahuja style OTA** The design equations of the improved Ahuja style OTA can be found below:

$$\begin{cases} (2+\alpha)\zeta\omega_n = \frac{g_{m2}(C_1C_2+C_2C_C)}{C_2(C_1C_L+C_1C_C+C_LC_C)} \\ \omega_n^2(1+2\alpha\zeta^2) = \frac{fg_{m1}g_{m3}(C_C+C_1)}{C_2(C_1C_L+C_1C_C+C_LC_C)} \\ \alpha\zeta\omega_n^3 = \frac{fg_{m1}g_{m2}g_{m3}}{C_2(C_1C_L+C_1C_C+C_LC_C)} \end{cases} \tag{4.24}$$

The same design procedure is applied to the improved Ahuja style OTA.

#### 4.2.4.4 Simulation Results

By applying the optimization procedures introduced above, two designs are made to achieve good settling performance. Simulation results using 0.25-$\mu$m CMOS process model are given in Table 4.2. To ensure high slew rate, the biasing current of the output stage must be high enough. The OTAs were designed with $\alpha = 5$, $\zeta = 0.95$ and $\gamma = 5$. The supply voltage is 2.5 V, the load capacitance is $C_L = 3\ pF$ and the feedback factor $f = 0.75$. It is seen that the settling performances of two OTAs are

Table 4.2: Simulation results of two type of OTAs.

| | Ahuja OTA | Improved Ahuja OTA |
|---|---|---|
| DC gain [dB] | 66 | 72 |
| Power consumption [mW] | 30 | 25 |
| GBW [MHz] | 710 | 963 |
| Settling time + slew time [ns] (0.6-V step) | 2.1 | 2.1 |

similar. The improved Ahuja style OTA reaches higher GBW and consumes less power than the Ahuja style OTA.

#### 4.2.4.5 Comparison of Two Type of OTAs

The poles and zeros for these two OTA types achieving a certain settling performance are almost the same. The difference takes place in the implementation of the circuits. To design a fast settling OTA, the large transconductance value is inevitable for transistor M2, as it drives the compensation capacitance, which is a relatively large capacitance. In the Ahuja style OTA, M2 are PMOS transistors, which need larger current and size to achieve the wanted transconductance, resulting into more power consumption. However, in the improved Ahuja style OTA, M2 are NMOS transistors, making things easier. This is the main difference between these two types of OTAs.

In nanometer CMOS technologies, the two-stage OTA offers both high DC gain and high output swing. By careful optimization, the settling performance of the two-stage OTA is comparable to that of the single-stage OTA.

## 4.3 Low-Voltage Low-Power Σ-Δ ADC Design

### 4.3.1 Impact of Circuit Nonidealities to Σ-Δ ADC Performance

The switched-capacitor implementation of the Σ-Δ ADC is popular for its accuracy and robustness. However, the nonidealities of the circuits degrade the Σ-Δ ADC performance considerably. It is preferred to quantitatively investigate the impact on the Σ-Δ ADC performance. For Σ-Δ ADCs, the behavioral simulation is the best tool to evaluate the operation and performance of the Σ-Δ ADC.

The basic building block in a switched-capacitor Σ-Δ ADC is the switched-capacitor integrator. The switched-capacitor integrator is modeled as an OTA and sampling capacitance and integration capacitance, shown in Fig. 4.18. The main non-idealities of a

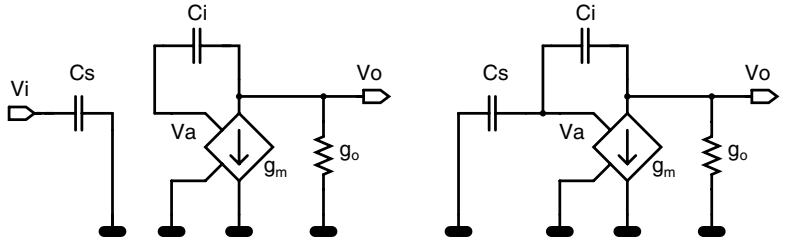



Figure 4.18: Switched-capacitor integrator modeling.

switched-capacitor integrator is the finite OTA gain and the settling error. The transfer function of the integrator is given by [Mar81], [Tem80].

$$I(z) = \frac{C_s}{C_i} \cdot \frac{\rho_2 z^{-1}}{1 - \frac{\rho_2}{\rho_1} z^{-1}} \tag{4.25}$$

where $\rho_1$ and $\rho_2$ are the closed-loop static errors determined by these equations:

$$\rho_1 = \frac{Af_{dc1}}{1 + Af_{dc1}} \tag{4.26}$$

$$\rho_2 = \frac{Af_{dc2}}{1 + Af_{dc2}} \tag{4.27}$$

where A is the OTA DC gain and $f_{dc1}$ and $f_{dc2}$ are DC feedback factors during the sampling phase and integration phase, respectively. $f_{dc1}$ and $f_{dc2}$ are given by the following equations:

$$f_{dc1} = 1 \tag{4.28}$$

$$f_{dc2} = \frac{C_i}{C_s + C_i} \tag{4.29}$$

By implementing the transfer function in the behavioral simulations, the relation between the SNR of the Σ-Δ modulator and the OTA DC gain is revealed.

The previous deviation assumes that the OTA instantaneously settles to the final value. The settling error is not taken into consideration in the above analysis. In [Mar81], [Tem80], [Fis84], [Gei82] and [Gee99], the transfer function of the integrator is given.

$$I(z) = \frac{C_s}{C_i} \cdot \frac{\rho_2(1-\delta)z^{-1}}{1 - \frac{\rho_2}{\rho_1} \cdot \left(1 - \delta\left(1 - \frac{\rho_1}{\rho_2}\right)\right)z^{-1}} \tag{4.30}$$

The parameter $\delta$ represents the settling error in the integration phase. It can be expressed as:

$$\delta = exp\left(-\frac{g_m}{C_s} \cdot \frac{\tau}{\rho_2}\right) \tag{4.31}$$

where $\tau$ is the time available for settling during the integration phase. By using the transfer function in the behavioral simulations, the relation between the SNR of the Σ-Δ modulator and the OTA DC gain and settling error can be derived.

### 4.3.2 Modulator Topology Selection

A single loop topology is preferable for low-voltage low-power designs since it is less sensitive to circuit non-idealities, e.g. OTA DC gain and switch on-resistance [Mar99]. The Σ-Δ ADC is known for its high tolerance for circuit non-idealities compared to other ADC architectures. However, in a low-voltage environment and nanometer technologies, circuit non-idealities become more severe and their impact on the ADC performance should be reconsidered. A third-order single-loop topology was chosen in this design, shown in Fig. 4.19. The loop coefficients are set to [0.2 0.3 0.4]. Compared to loop coefficients in [Mar98], the modulator with these coefficients has the same noise shaping ability but higher overload level, which is good for expanding the dynamic range in low-voltage environments. More importantly, this topology is quite tolerant to the inaccurate coefficients caused by capacitance mismatches. Fig. 4.20 shows a behavioral simulation result of the modulator. The behavioral simulation was done by setting all of the OTA gains to 40 dB and the oversampling ratio to 100.

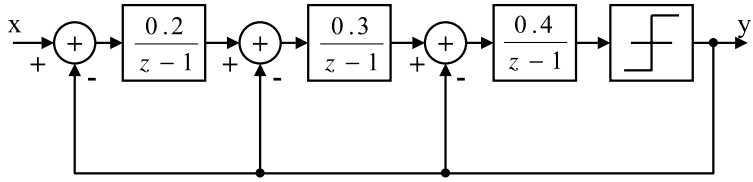



Figure 4.19: Single-loop third-order topology.

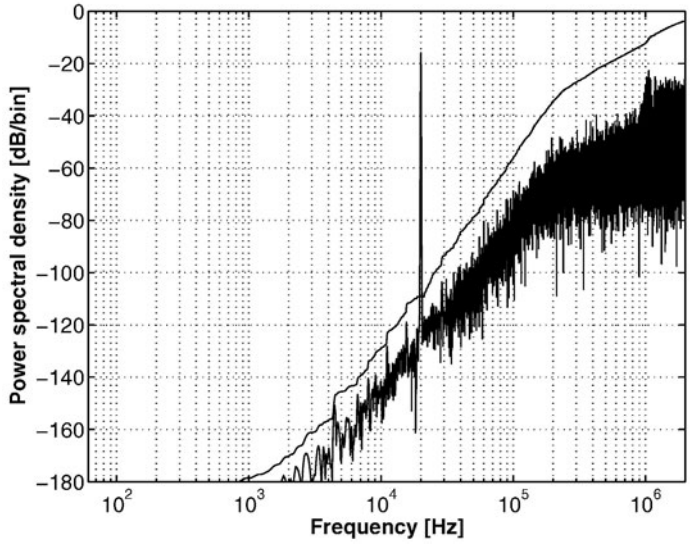



Figure 4.20: Output spectrum of the proposed topology with a 20-kHz input signal.

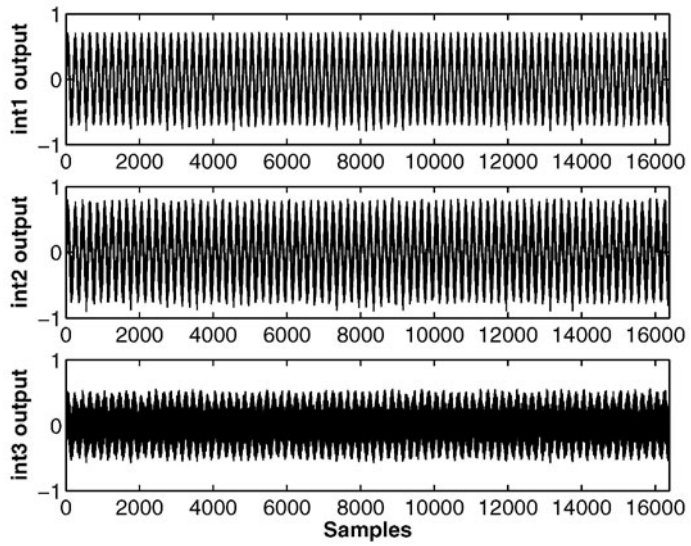



Figure 4.21: Normalized output of each integrators of the proposed topology.

Fig. 4.21 shows the output swing of each integrator of the modulator normalized to the reference voltage while feeding a -3 dB input signal. The output swings reach 80% of the reference voltage, which means that the reference voltage should be almost the same as the output swing of the integrator. If distortion performance is taken into consideration, then the reference voltage should be even smaller. Fig. 4.22 shows the simulated Σ-Δ modulator SNR vs. the OTA DC gains in the proposed topology, according to the equations derived in section 4.3.1. The minimum gain requirement for OTAs is 30 dB to ensure a 85-dB SNR of the modulator. This gain requirement is drawn only from the noise shaping consideration. However, taking the distortion into consideration, the higher the OTA gain, the better distortion performance that can be achieved.

Fig. 4.23 shows the simulated Σ-Δ modulator SNR vs. the integrator settling error. The OTA DC gain is set to 80 dB in the simulation. The single-loop topology is quite tolerant to the settling error of the integrator according to the simulation results.

### 4.3.3 OTA Topology Selection

The OTA composes the main building block of the Σ-Δ modulator. It determines the main power consumption of the modulator. The requirements for the OTA are mainly the output swing, the DC gain and the GBW. The output swing is of great importance in low-voltage designs, as mentioned before. It determines the reference voltage, hence the sampling capacitance and finally the power consumption. For a

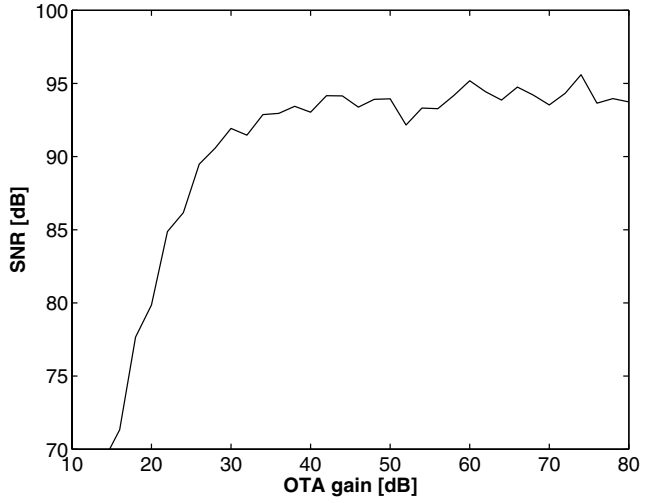



Figure 4.22: SNR vs. OTA DC gain of the third-order single-loop Σ-Δ modulator.

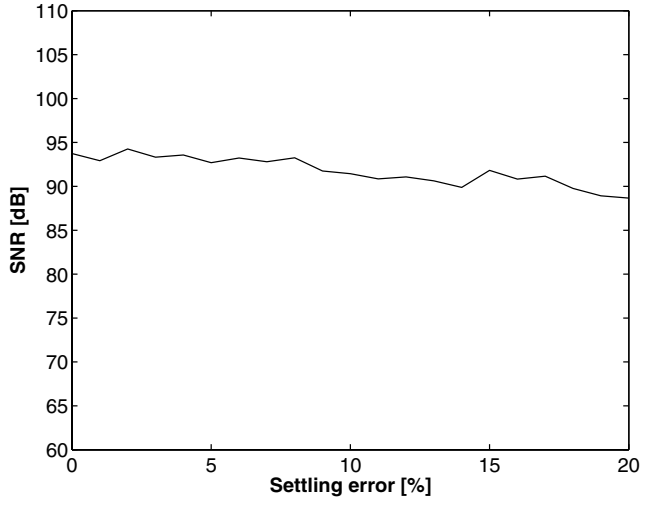



Figure 4.23: SNR vs. integrator settling error of the third-order single-loop Σ-Δ modulator.

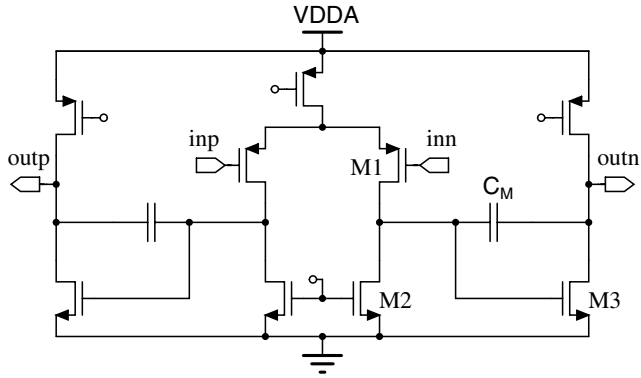



Figure 4.24: The Miller compensated two-stage OTA.

kT/C noise dominated modulator, the dynamic range can be written as:

$$DR = \frac{P_{in_{max}}}{P_{kT/c}} = \frac{V_{in_{max}}^2 \cdot OSR \cdot C_s}{2kT} \tag{4.32}$$

where $V_{in_{max}}$ is the input amplitude of the modulator while the modulator reaches the highest output output swing. $C_S$ is the sampling capacitance of the first integrator. The maximum input amplitude of a certain modulator topology is defined by the output swing of the OTA, as can be seen in Fig. 4.21. For a certain dynamic range, an increase in the output swing can result in a reduction of sampling capacitance and hence power consumption. The importance of the output swing can be clearly seen here in equation (4.32). An OTA topology that can provide rail-to-rail output swing is highly desirable in low-voltage low-power designs.

In nanometer technology, the intrinsic voltage gain of the transistor is low due to the lower output impedance. The low-voltage environment and output swing constraint prohibit the use of the cascoding transistors to increase the voltage gain. The natural solution is two-stage or multi-stage topologies. However, the two-stage OTA is not load compensated. Extra compensation capacitance is needed to ensure the closed-loop stability. For a given GBW and load capacitance $C_L$, the current drawn by a fully differential class A Miller OTA, shown in Fig. 4.24 can be calculated as:

$$\frac{g_{m1}}{C_M} = GBW \cdot 2\pi \tag{4.33}$$

where $C_M$ is the Miller compensation capacitance. Combining this with the MOSFET equation in strong inversion region

$$g_{m1} = \frac{2I_{D1}}{V_{GS1} - V_T} \tag{4.34}$$

gives

$$I_{D1} = GBW \cdot \pi \cdot (V_{GS1} - V_T) \cdot C_M \tag{4.35}$$

The non-dominant pole, which is created by the load capacitance, should be placed beyond the three times the GBW. This criteria

$$\frac{g_{m3}}{C_M + C_L} = 3 \cdot GBW \cdot 2\pi \tag{4.36}$$

gives

$$I_{D3} = GBW \cdot \pi \cdot (V_{GS3} - V_T) \cdot (3C_M + 3C_L) \tag{4.37}$$

Assuming all transistors have the same overdrive voltage, the total current of the Miller OTA is then

$$I_{Miller} = GBW \cdot \pi \cdot (V_{GS} - V_T) \cdot (8C_M + 6C_L) \tag{4.38}$$

The minimum supply voltage of the Miller OTA is a transistor threshold voltage plus three times the transistor saturation voltage, as shown in equation (4.39).

$$V_{dd_{Miller}} = V_{GS} + 2V_{DS_{sat}} = V_T + 3V_{DS_{sat}} \tag{4.39}$$

Similarly, for the same GBW and load capacitance $C_L$, the current drawn by a fully differential, class A, single-stage OTA, is calculated as follows. The current drawn by the single-stage telescopic cascode OTA is

$$I_{tc} = GBW \cdot \pi \cdot (V_{GS} - V_T) \cdot (2C_L) \tag{4.40}$$

The minimum supply voltage of the single-stage telescopic cascode OTA is a transistor threshold voltage plus three times the transistor saturation voltage, as shown in equation (4.41).

$$V_{dd_{tc}} = V_{GS} + 2V_{DS_{sat}} = V_T + 3V_{DS_{sat}} \tag{4.41}$$

For the folded cascode OTA, there are two current branches. Normally the current of both current branches are the same. The current drawn by the single-stage folded cascode OTA is

$$I_{fc} = GBW \cdot \pi \cdot (V_{GS} - V_T) \cdot (4C_L) \tag{4.42}$$

The minimum supply voltage of the folded cascode OTA is a transistor threshold voltage plus two times the transistor saturation voltage, as shown in equation (4.43).

$$V_{dd_{fc}} = V_{GS} + V_{DS_{sat}} = V_T + 2V_{DS_{sat}} \tag{4.43}$$

The current drawn by a current mirror OTA with a current ratio of $1 : B$, shown in Fig. 4.25, can be calculated as follows. For the given GBW and $C_L$, we have

$$\frac{g_{m1} \cdot B}{C_L} = GBW \cdot 2\pi \tag{4.44}$$

then

$$I_{D1} = GBW \cdot \pi \cdot (V_{GS1} - V_T) \cdot \frac{C_L}{B} \tag{4.45}$$

And for the current mirror OTA, we have

$$I_{D3} = B \cdot I_{D1} \tag{4.46}$$

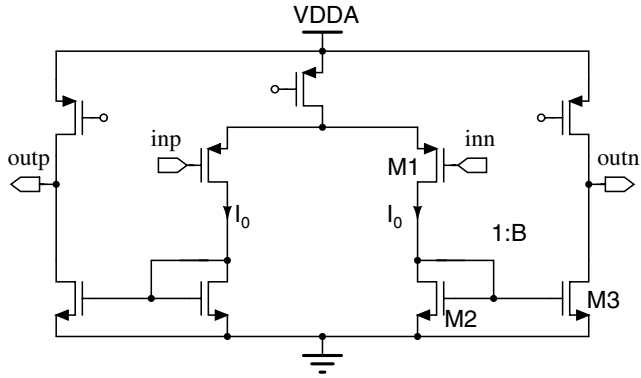



Figure 4.25: The current mirror OTA.

Then the total current of the current mirror OTA is

$$I_{cm} = GBW \cdot \pi \cdot (V_{GS} - V_T) \cdot (2C_L + \frac{2C_L}{B}) \tag{4.47}$$

The minimum supply voltage of the current mirror OTA is a transistor threshold voltage plus three times the transistor saturation voltage, as shown in equation (4.48).

$$V_{dd_{cm}} = V_{GS} + 2V_{DS_{sat}} = V_T + 3V_{DS_{sat}} \tag{4.48}$$

It is clearly seen that for the same condition, the single-stage OTA is more power-efficient than the two-stage OTA, since no power is wasted in driving the compensation capacitance in the single-stage OTA.

According to the above discussion, the single-stage OTA is preferred in terms of power-efficiency. In a low-voltage environment, the rail-to-rail output swing for the OTA is highly preferred. The only single-stage topology that can provide rail-to-rail output swing is the current mirror OTA. However, the voltage gain of the current mirror OTA is only in the order of $gm \cdot ro$, which is normally around 20-40 dB in nanometer technologies. According to behavioral simulations, the requirement of the OTA DC gain is above 40 dB. To ensure enough gain, a gain enhancement technique is used, which can enhance the gain for 10-20 dB without extra power consumption [Yao03], shown in Fig. 4.26. The design of the gain-enhanced current mirror OTA has been discussed in 4.2.2.

The class AB output stage is known to be more power-efficient than the class A output stage in SC circuits [Wan99]. Higher slew-rate can be obtained from a class AB output stage with less power consumption. To save power, a class AB output stage should be adopted in this low-voltage low-power design.

Shown in Fig. 4.27(a), the class AB operation is made by driving the PMOS transistor M4 by a floating voltage source $V_{bias}$. This is a very crude class AB output scheme.

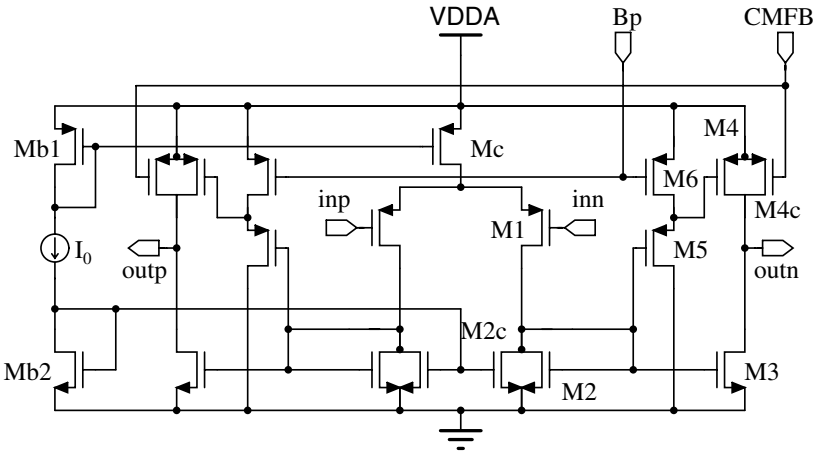
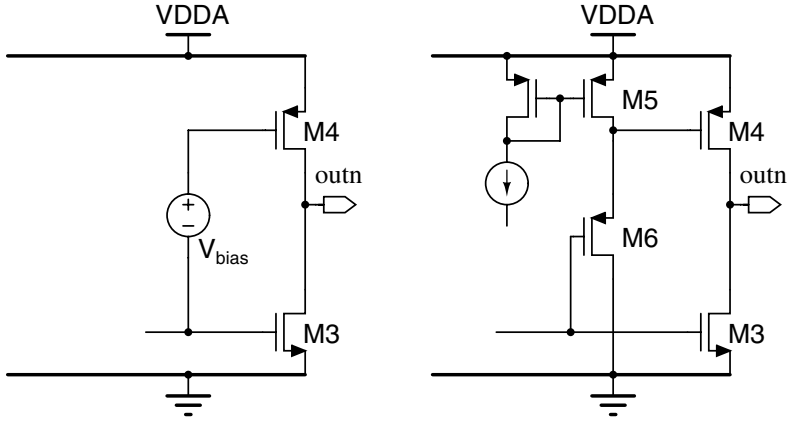



Figure 4.26: Schematic of the gain-enhanced current mirror OTA used in the Σ-Δ modulator design.




(a) Class AB biasing of the output PMOS transistor.

(b) Implementation of the class AB biasing.

Figure 4.27: The class AB operation of the output stage.

The class AB characteristics are not so good. But here in SC circuits, the high slew rate is more important than the good class AB output characteristics. As long as the output settles to the required final value, the settling procedure is not important. This class AB stage increases the current sourcing ability of the output stage. As a result, the slew rate of the OTA is increased. The floating voltage source $V_{bias}$ is implemented by a level-shifter, shown in Fig. 4.27(b). The transistors M5 and M6 are identical and have the same drain current. As a result, their gate-source voltages are identical too. By properly biasing M5, a certain $V_{bias}$ can be obtained.

Common-mode feedback is essential to fully-differential circuits. A switched-capacitor common-mode feedback is the best solution in terms of power consumption.

### 4.3.4 Transistor Biasing

The biasing of a transistor determines the most important specifications of the transistor. Generally speaking, the transistor reaches the maximum $gm/I_D$ ratio and low saturation voltage when it operates in the weak inversion region, hence the maximum power efficiency is achieved. However, the frequency response is degraded and the silicon area occupied is bigger in the weak inversion region. A compromise is made here between speed and power consumption. The specifications of the whole modulator should be taken into consideration in making tradeoffs among speed, power and area. In this design, the main transistors in OTAs are biased in moderate inversion region, e.g. $V_{GS} - V_T \approx 0.1$ V.

### 4.3.5 Scaling of Integrators

One of the most interesting properties of the $\Sigma$-$\Delta$ modulator is the noise suppression inside the loop. Utilizing this feature can result into a large amount of power saving. For a single-loop $\Sigma$-$\Delta$ modulator, the noise suppression in node k can be calculated by [Nor96]

$$F_{sup,k} = \frac{OSR^{2k+1}}{\pi^{2k}}(2k+1)\prod_{i=0}^{k} a_i^2 \tag{4.49}$$

where F is the noise suppression factor, OSR is the oversampling ratio and $a_i$ denotes the loop coefficient of the i-th stage. For the proposed topology, the noise suppression of the first, second and third stage is 41 dB, 63 dB and 86 dB, respectively. This allows the sampling capacitances of these stages to be scaled down proportionally to corresponding ratios. The only restriction is due to the matching requirements. Reducing the sampling capacitance results into a reduction of the load capacitance of the OTA and hence reduces the power consumption.

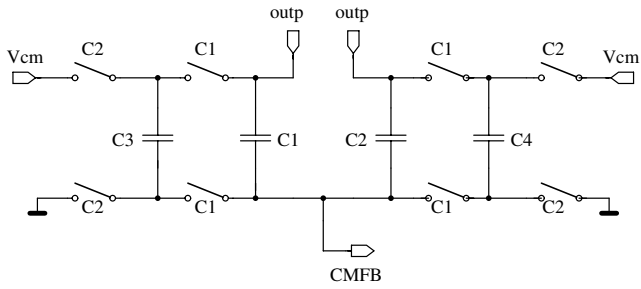



Figure 4.28: Schematic of the switched-capacitor CMFB circuit.

## 4.4 A 1-V 140-$\mu$W $\Sigma$-$\Delta$ Modulator in 90-nm CMOS

### 4.4.1 Building Block Circuits Design

#### 4.4.1.1 Low-Voltage Low-Power OTA

Depicted in Fig. 4.26, the OTA used in this design is the current mirror OTA with gain enhancement. This OTA features rail-to-rail output swing and class AB operation. And most importantly, it is a single-stage structure, which reduces the power consumption effectively.

As mentioned in section 4.2.1.4, the $k$ factor determines the gain reached and the phase margin. In this design, the $k$ factor was set to 0.8 and the current mirror ratio is 10. These ratios can be realized by sizing relevant transistors. Matching issues should be taken into consideration here. Two identical transistors M5 and M6 function as a voltage level-shifter. The shifted signal drives transistor M4, providing extra current to the load when a large signal is present. The biasing voltage Bp defines the class AB operating point of the output stage. The switched-capacitor CMFB circuit is presented in Fig. 4.28. The two pre-charged capacitor $C_1$ and $C_2$ sense the output common-mode voltage and shift the voltage to a proper level in node CMFB. Capacitor $C_3$ and $C_4$ periodically recharge the sensing capacitor to provide a constant voltage in the sensing capacitor. The main feature of this CMFB circuit is that it is very power efficient. To ensure that the speed of the common-mode loop is faster than the differential loop in the OTA, the transconductance of transistor M4c should be higher than that of transistor M1 in Fig. 4.26.

The simulated frequency response of the proposed OTA with a 6 pF load is depicted in Fig. 4.29. The gain reaches 50 dB and the GBW is 57 MHz while the phase margin is kept at 57 degrees, with a power consumption of only 80 $\mu$W.

#### 4.4.1.2 One-Bit Quantizer Circuits

The one-bit quantizer is realized with a dynamic comparator and a SR latch shown in Fig. 4.30 [Cho95]. While clock C1 is low, node P and Q are pre-charged to Vdd. While clock C1 goes high, the pre-charged parasitic capacitances of node P and Q

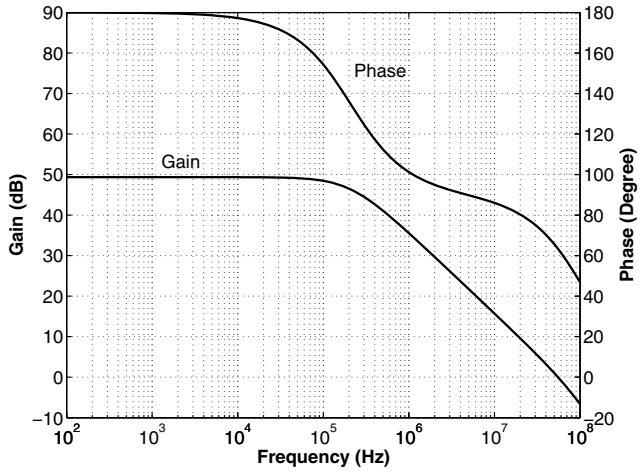



Figure 4.29: Simulated OTA frequency response.

are discharged by transistor M1a and M1b respectively. The discharge rate of each branch depends on the input voltage. When the voltage of node P or Q drops to the threshold voltage of the latch formed by two cross-coupled inverters, the regeneration process starts. Finally the voltage of node P and Q reaches the rail voltage according to the decision made. The result is then latched by the following SR latch. The whole comparator is a purely dynamic circuit, which is very power efficient. For a single-bit $\Sigma$-$\Delta$ modulator, the requirement for the quantizer is quite relaxed as non-idealities in this stage can be largely suppressed, seeing section 4.3.5. The offset voltage is mainly defined by matching of the input transistors.

#### 4.4.1.3 Switch Driving Circuits

All switches are implemented with transmission gates. As the circuit is working on its rated supply voltage, there is no need to use any clock bootstrapping circuit to boost the driving voltage. Simple inverters are employed to drive the switching transistors, shown in Fig. 4.31. The maximum driving voltage is the supply voltage. So no node inside the whole circuit is exposed to a voltage higher than Vdd or lower than Vss, which is essential for the high-reliability operation of the circuit.

#### 4.4.1.4 Other Circuits

The on-chip clock generator is shown in Fig. 4.32 [Mar98]. The external clock input signal is buffered and then two non-overlapping clock signals are generated. To avoid signal dependent charge injection, two delayed clocks, i.e. C1d and C2d are also generated [Hai83].

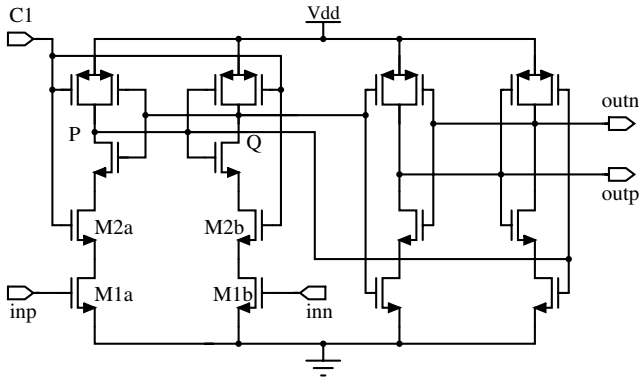



Figure 4.30: Schematic of the comparator and latch.

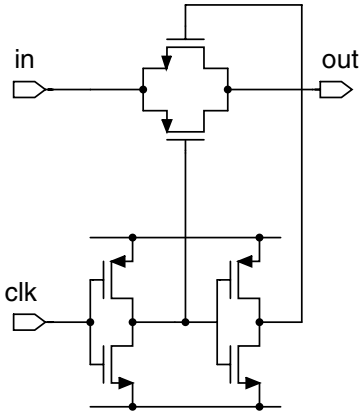



Figure 4.31: Switch implementation and the local driver.

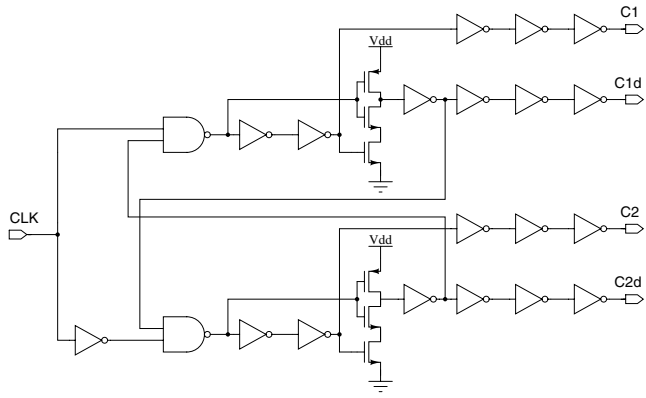



Figure 4.32: Schematic of the clock generator.

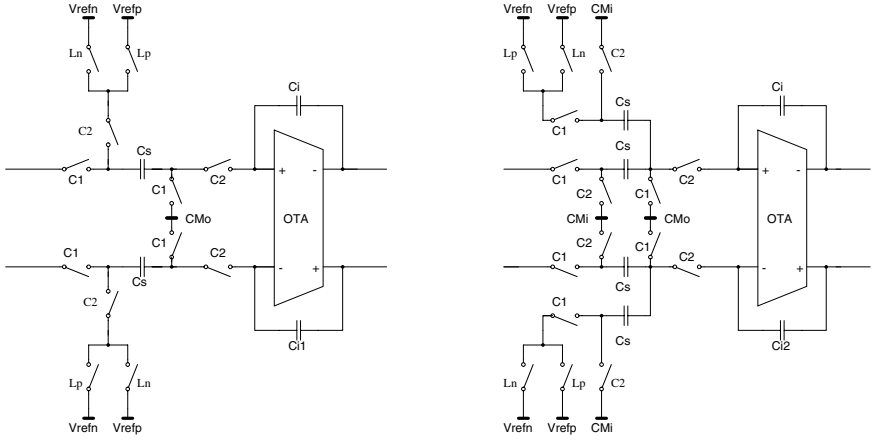



Figure 4.33: Different feedback configurations.

### 4.4.2 Implementation

The ultimate goal of this design is to reduce the power consumption as much as possible. To lower the power consumption, the main consideration is to lower the power consumption in the first integrator. In $\Sigma$-$\Delta$ modulators, the first integrator dominates the overall performance of the modulator and most of the power is consumed here. As mentioned in section 4.3.5 the second and third integrators can be scaled down to reduce the power consumption. The thermal noise level of the modulator determines the value of the first sampling capacitor, hence the power consumption of the first integrator. The value of the first sampling capacitor is 6 pF, which is sufficient to provide 95 dB peak SNR with 0.6 V reference level. Considering the matching property of the capacitors, both the second and third sampling capacitor are set to 0.4 pF.

Another practical low-power consideration is the feedback scheme of the integrator. Fig. 4.33 shows two different feedback schemes. The left one directly connects the feedback signal to one terminal of the sampling capacitor during clock period C2, i.e. the integration phase of the integrator. The right one uses two sampling capacitors to sample the input signal and feedback signal, respectively, and then sums these two signals during the integration phase of the integrator. Both of these two schemes have the same function, while the right scheme uses more capacitors and switches. On the left circuit, the sampling capacitor is discharged to either Vrefp or Vrefn during the integration phase. During the sampling phase the sampling capacitor is charged to the input voltage. During the charge and discharge cycle, the voltage change on the sampling capacitor is from either Vrefp or Vrefn to Vin, which is quite large. Most importantly, the charge current is provided by the preceding OTA. This large signal charge requires a high slew rate of the OTA and consumes power. On the right circuit, the large charge current is provided by the reference voltage. The OTA only charges the sampling capacitor from 0 to the input voltage, which is smaller. So the right circuit relaxes the requirement for the preceding OTA and consumes less power.

The common-mode input and output voltage is chosen differently in a low-voltage environment. For signal swing consideration, the output common-mode voltage is set to the middle of the supply voltage, i.e. 0.5 V. However, if the input common-mode voltage is set to the middle of the supply voltage, rail-to-rail input capability is required for the OTA, which can't be offered by the normal differential input stage. If the input common-mode voltage is set near the supply rail, the normal OTA can be used without the rail-to-rail input requirement. In this design, the common-mode input voltage is set to be 0.2 V. The whole circuit is shown in Fig. 4.34.

As the process technology used is a standard digital technology, no standard metal-insulator-metal (MIM) capacitor is available. All capacitances are implemented by metal wall structure, shown in Fig. 4.35 [Apa02]. This structure uses the lateral capacitance instead of the vertical capacitance normally used. In nanometer technologies, the lateral spaces between metal lines in the same layer are smaller than the vertical spaces between metal layers. Also the lateral spaces are well controlled. Only one metal layer is occupied for connecting, and the remaining layers can be used to build the capacitor, which means the unit capacitance can be large. Calculation shows that the unit capacitance is around 1.7 $fF/\mu m^2$ in the used technology, which is higher

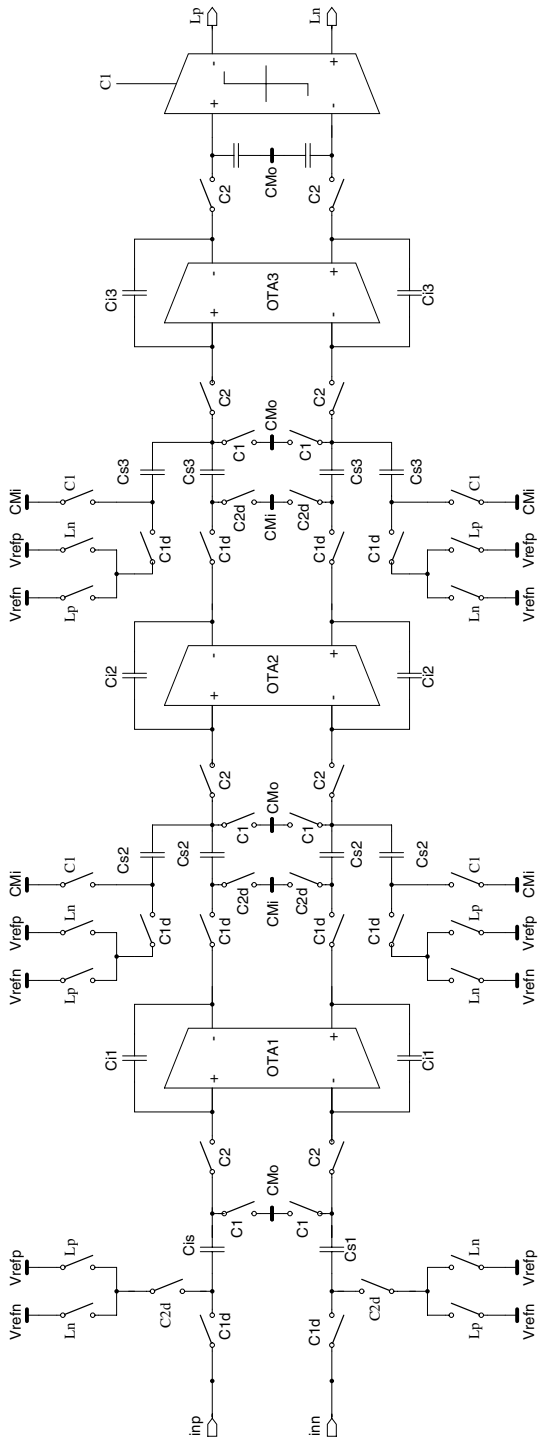



Figure 4.34: Schematic of the proposed third-order single-loop Σ-Δ modulator.

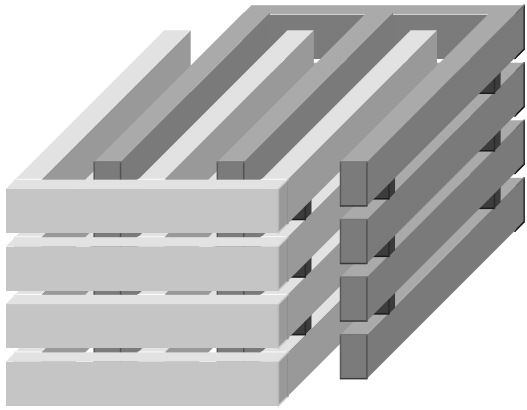


Figure 4.35: Proposed metal wall capacitance structure.

than that of the normal metal-insulator-metal (MIM) capacitor. However, the matching (0.5%) is worse than that of MIM capacitor (0.1%). As the loop coefficients are defined by the capacitance ratios, robust loop coefficients are chosen to be more tolerant to the mismatched capacitance. Besides, this kind of capacitance is widely used in this design as decoupling capacitors around the chip.

The chip was fabricated in a standard digital 90-nm CMOS technology. The power supply voltage is 1 V and the reference voltage is 0.6 V. The chip core size is $0.42\,mm \times 0.42\,mm$, as illustrated in Fig. 4.36. The analog part is separated from the digital part by guard rings. To reach the maximum common-mode rejection ratio, all the analog parts are laid out symmetrically. The surroundings of the unit capacitances are identical to ensure good matching.

### 4.4.3 Measurement Results

The schematic of the measurement setup is shown in Fig. 4.37. To shield the chip from external interferences, the chip is mounted on a thick-film ceramic substrate and then encapsulated in a copper-beryllium box, as shown in Fig. 4.38. Separate power supplies for analog, digital parts and output buffer are used in the measurement. Local decoupling capacitors are used in power supplies and biasing sources.

Clocked at 4 MHz, the output data of the modulator is captured by a logic analyzer and processed by software. Fig. 4.39 shows the measured output spectrum of an 11 kHz sinusoid signal. Fig. 4.40 shows the output spectrum with the inputs short-circuited to ground. Fig. 4.41 shows the measured SNR and SNDR vs. the input signal amplitudes normalized by reference voltage. The peak SNR reaches 85 dB while the peak SNDR

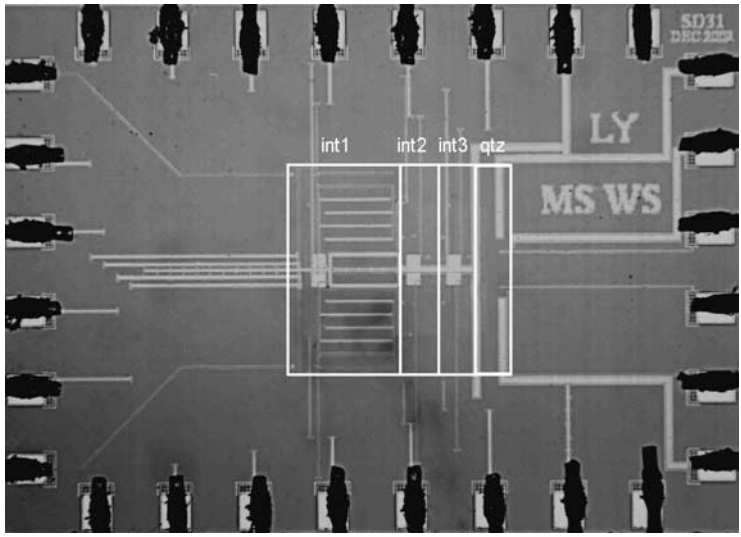



Figure 4.36: Chip micrograph of the Σ-Δ modulator in 90-nm CMOS.

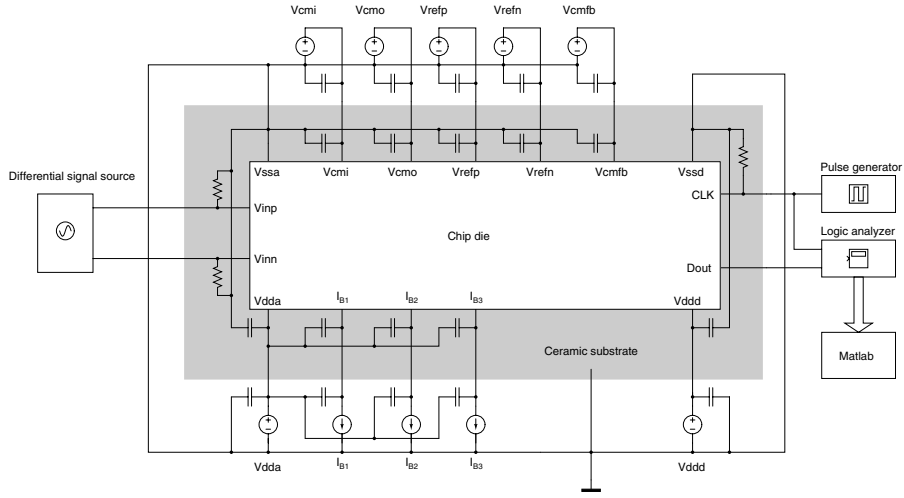



Figure 4.37: Schematic of the Σ-Δ modulator measurement setup.

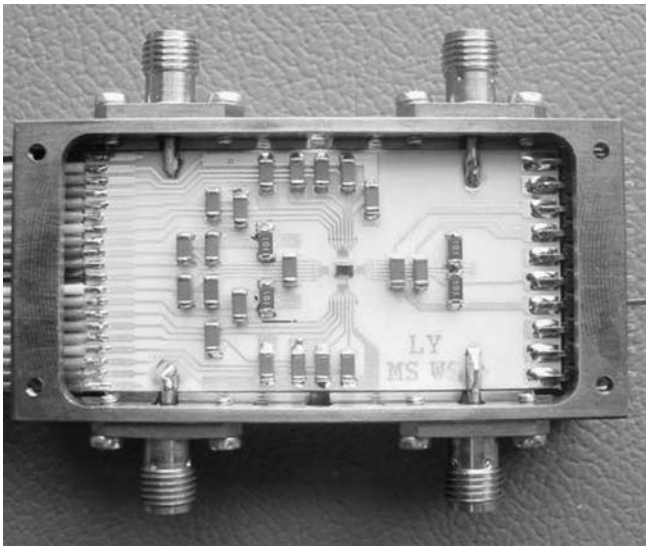


Figure 4.38: Photograph of the die mounted on the ceramic substrate and sealed inside the copper-beryllium box.

reaches 81 dB. The dynamic range is 88 dB in a 20-kHz signal bandwidth. The analog core power consumption is 130 $\mu$W. The digital power consumption is 10 $\mu$W, excluding the power consumption of the output buffer. Table 4.3 gives the summary of the performance.

Table 4.4 shows the performance comparison of recently published low-voltage low-power $\Sigma$-$\Delta$ modulators whose supply voltage is less than 1.5 V. The figure-of-merit (FOM) is defined as [Rab97]:

$$FOM = \frac{4kT \cdot f_B \cdot DR}{P} \tag{4.50}$$

where $k$ is the Boltzmann's constant; T is the absolute temperature; $f_B$ and P is the signal bandwidth and power consumption of the $\Sigma$-$\Delta$ ADC respectively. The FOM is a measure of the power efficiencies of $\Sigma$-$\Delta$ ADCs, taking signal bandwidth and dynamic range into consideration. However, the supply voltage is not taken into consideration here. To make a fair comparison, all converters should be operating at the same supply voltage. This work achieves the highest FOM among these $\Sigma$-$\Delta$ ADCs.

There are two reasons for the high power efficiency of this work. One is the specially designed building blocks, especially the class AB gain-enhanced current-mirror OTA. Another is the use of the advanced 90 nm technology, which helps to reduce the power consumption in the digital circuit. Following the low-voltage and low-power design strategies described before, the power consumption of the whole converter has been effectively decreased. For digital parts, the smaller transistor feature size helps

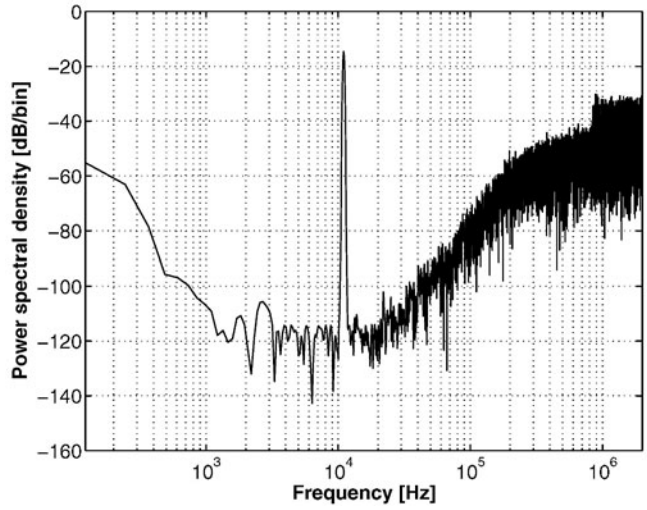



Figure 4.39: Measured output spectrum of an 11 kHz sinusoidal input.

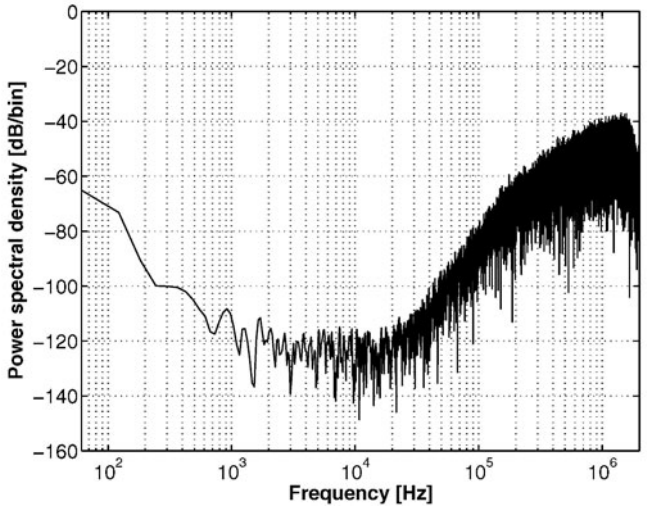



Figure 4.40: Measured noise floor of the modulator with inputs short-circuited.

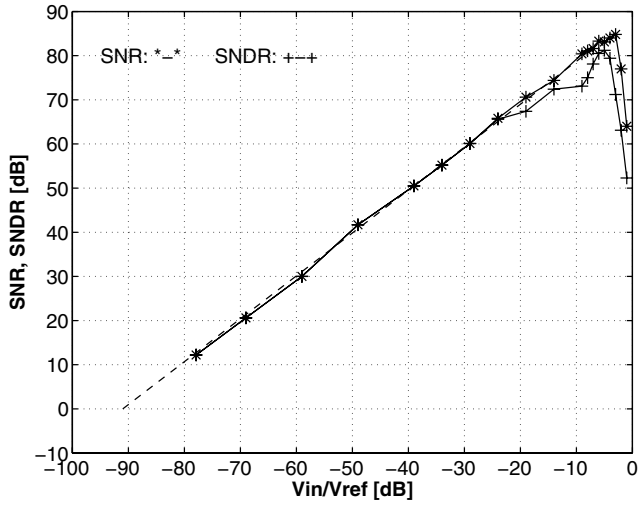



Figure 4.41: Measured SNR and SNDR vs. input amplitude.

Table 4.3: Measured performance summary.

| | | |
|---|---|---|
| Sampling frequency | 4 | MHz |
| Signal bandwidth | 20 | kHz |
| Over sampling ratio | 100 | |
| Supply voltage | 1.0 | V |
| Analog power consumption | 130 | $\mu$W |
| Digital power consumption | 10 | $\mu$W |
| Peak SNR | 85 | dB |
| Peak SNDR | 81 | dB |
| DR | 88 | dB |
| Reference voltage | 0.6 | V |
| Active die area | 0.18 | $mm^2$ |
| Technology | 90nm CMOS | |

Table 4.4: Performance comparison.

| Names and Years | Supply Voltage [V] | DR [dB] | Signal Bandwidth [kHz] | Power [$\mu$W] | FOM |
|---|---|---|---|---|---|
| Keskin,2002 [Kes02] | 1.0 | 80 | 20 | 5600 | 5.9e-6 |
| Sauerbrey,2002 [Sau02] | 0.7 | 75 | 8 | 80 | 52e-6 |
| Dessouky,2001 [Des01] | 1.0 | 88 | 25 | 950 | 275e-6 |
| Peluso,1998 [Pel98] | 0.9 | 77 | 16 | 40 | 330e-6 |
| This work | 1.0 | 88 | 20 | 140 | 1493e-6 |

to decrease the power consumption. Clocked at 4 MHz, the total digital part of this modulator consumes only 10 $\mu$W.

## 4.5 Measurements on PSRR and Low-Frequency Noise Floor

### 4.5.1 Introduction of PSRR

On the design of the 3rd-order single-loop $\Sigma$-$\Delta$ modulator, the power supply rejection ratio(PSRR) of the modulator is of concern. The class AB biasing circuit, i.e. the transistor M6 shown in Fig. 4.26, is directly connected to the power supply rail. There is a concern of coupling the disturbance on the supply rail to the input of the transistor M4, resulting into degradation of the PSRR. Actually the transistor M6 is biased in the saturation region and the output impedance is high, thus the coupling from the analog supply to the output signal is minimized. However, to test the PSRR, some special measurements are carried out.

The PSRR of an amplifier is defined as:

$$PSRR = \frac{A_{vin}}{A_{vdd}} = \frac{vout_{vin}/vin}{vout_{vdd}/vdd} \tag{4.51}$$

where $A_{vin}$ is the voltage gain from the input terminal to the output terminal of the amplifier and $A_{vdd}$ is the voltage gain from the power supply terminal to the output terminal of the amplifier. $vout_{vin}$ is the output voltage caused by the input voltage at the input terminal, $vin$, and $vout_{vdd}$ is the output voltage caused by the input voltage at the power supply terminal, $vdd$. Similarly, the PSRR of a $\Sigma$-$\Delta$ modulator can be defined as:

$$PSRR = \left(\frac{pout_{vin}/p_{vin}}{pout_{vdd}/p_{vdd}}\right)^{1/2} \tag{4.52}$$

where $pout_{vin}$ is the output power caused by the input power at the input terminal, $p_{vin}$, and $pout_{vdd}$ is the output power caused by the input power at the power supply terminal, $p_{vdd}$.

### 4.5.2 PSRR Measurement Setup

The measurement setup is shown in Fig. 4.42. The analog power supply is provided by a signal generator. A sinusoidal signal with a DC offset of 1 V functions as the analog power supply of the modulator. The 50-Ω resistor is the termination resistance of the signal source. In this way, a ripple on the analog supply is created. To measure the impact of the ripple on the analog supply to the performance of the modulator, all the off-chip decoupling capacitance must be disconnected to eliminate the attenuation from the decoupling capacitance. Therefore, there is no decoupling capacitance in the test circuits except the on-chip ones. The frequency of the power supply is fixed to 10 kHz and the input signal frequency is 15 kHz.

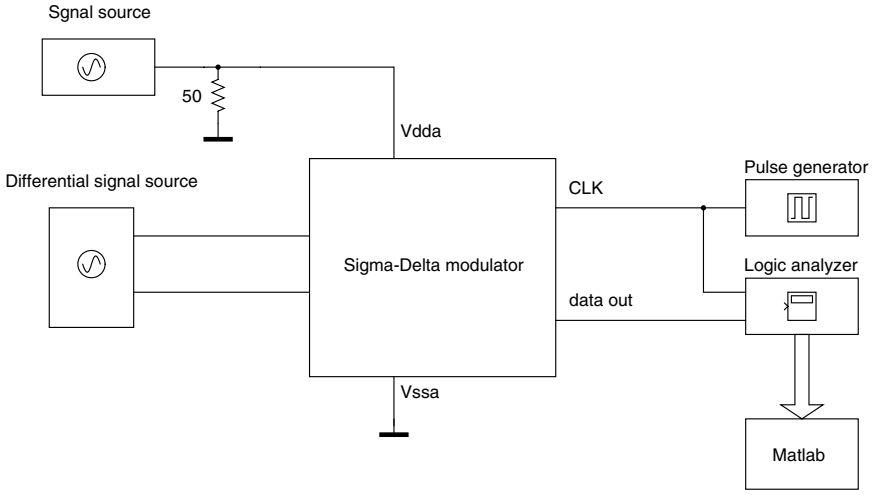
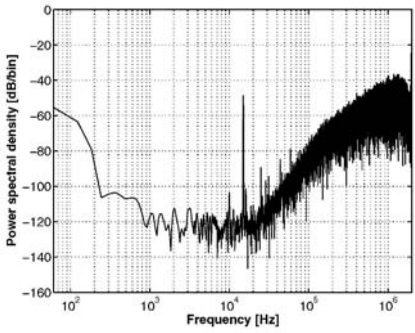



Figure 4.42: Schematic of the PSRR measurement setup.

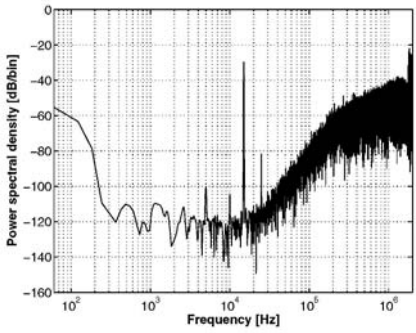
### 4.5.3 PSRR Measurement Results

#### 4.5.3.1 PSRR Measurement

First a 15-kHz, 10-m$V_{p-p}$ input signal and a 10-kHz, 10-m$V_{p-p}$ analog power supply are fed to the test circuit. Shown in Fig. 4.43(a), the measured output power of the input signal is about -48 dB and the output power of the analog supply is -103 dB. A PSRR of 55 dB is thus calculated. In Fig. 4.43(b) the input signal amplitude was increased to 100 m$V_{p-p}$. However, higher inter-modulation components at 5 kHz and 25 kHz were produced. The inter-modulation components are even higher than the power supply ripple itself. These measurement results show that the modulator has a good immunity to the ripples on the analog power supply. Due to some coupling paths from the analog power supply to the signal path, for example the biasing circuit, the ripple on the analog supply can be coupled and modulates the input signal.

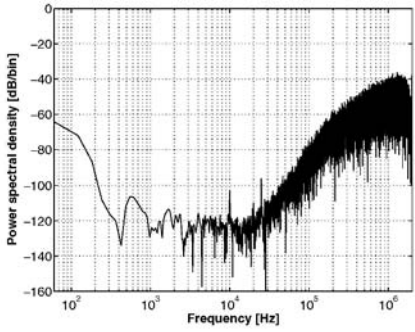



(a) Measured output spectrum with a 10-kHz, 10-m$V_{p-p}$ ripple on the analog power supply and a 15-kHz, 10-m$V_{p-p}$ signal as the input.

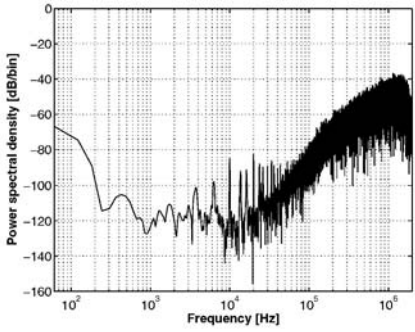



(b) Measured output spectrum with a 10-kHz, 10-m$V_{p-p}$ ripple on the analog power supply and a 15-kHz, 100-m$V_{p-p}$ signal as the input.

Figure 4.43: Measured output spectrum with a 10-kHz sinusoidal signal with a 1-V DC offset as the analog supply.




(a) Measured output spectrum with a 10-kHz, 10-m$V_{p-p}$ ripple on the analog power supply.




(b) Measured output spectrum with a 10-kHz, 50-m$V_{p-p}$ ripple on the analog power supply.

Figure 4.44: Measured output spectrum with a short-circuited input.

Fig. 4.44 shows the output spectrum of the ripple on the analog supply while the input is short-circuited to the ground. In Fig. 4.44(a) the peak of the ripple on the analog supply is under -100 dB when a 10-m$V_{p-p}$ ripple is applied to the analog supply, indicating a good immunity to the interference on the analog supply. While the ripple on the analog supply is increased to 50-m$V_{p-p}$, as shown in Fig. 4.44(b), the inter-modulation components are increased.

To test the effect of the decoupling network, a simple RC network was connected to the analog supply, shown in Fig. 4.45. The RC network is composed by a 100-Ω resistor in series and a 1-$\mu$F capacitor in parallel to the analog supply, providing a low-pass filter with a cut frequency of 1.6 kHz. A 370-m$V_{p-p}$, 19-kHz input signal and a 10-m$V_{p-p}$, 10-kHz ripple on the analog supply were applied to the modulator. The output spectrum is shown in Fig. 4.46. A PSRR of more than 70 dB can be achieved now with the decoupling network. It can be seen that the RC network effectively decouples the ripple on the analog supply. The ripple is hardly seen in the output spectrum. As the signal band is 20-kHz only, the decoupling is easily done. Thus the PSRR of the modulator can be greatly increased by using both the on-chip and off-chip decoupling capacitors.

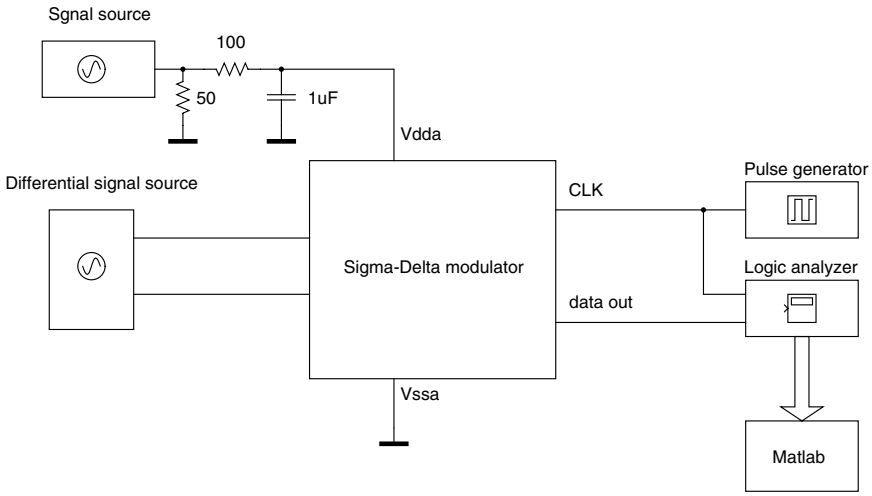
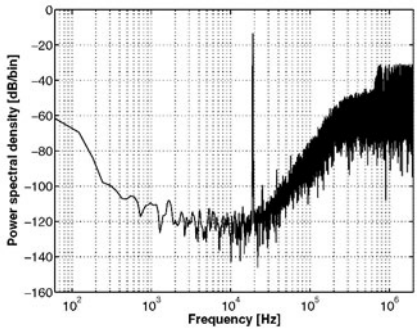


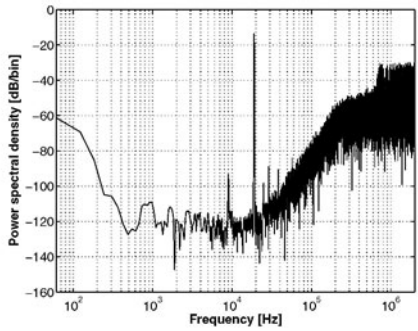

Figure 4.45: Measurement circuits with the off-chip decoupling network on the analog power supply.

### 4.5.3.2 PSRR v.s. Frequency Measurement

To investigate the frequency dependency of the PSRR, different frequencies are used in the PSRR measurements. In all the measurements, the input signal frequency is fixed to 25 kHz and the input amplitude is 370 m$V_{p-p}$. The ripple frequency on the analog power supply is changed from 1 kHz to 30 kHz and the ripple amplitude is fixed to 50 m$V_{p-p}$. All the following measurements are done without the RC decoupling




(a) Measured output spectrum with a 10-kHz, 10-m$V_{p-p}$ ripple on the analog power supply.




(b) Measured output spectrum with a 10-kHz, 100-m$V_{p-p}$ ripple on the analog power supply.

Figure 4.46: Measured output spectrum with a RC decoupling network on the analog power supply.

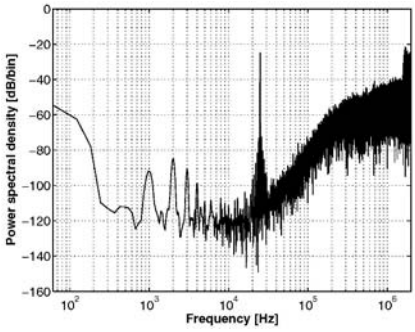
network on the analog power supply.

Fig. 4.47 shows the output spectrum of the modulator with different ripple frequencies from 1 kHz to 10 kHz and with the same amplitude. It is seen that while the frequency increases, the peak of the ripple decreases. The inter-modulation peaks decrease also. Usually the PSRR decreases with the frequency increases. However, due to the large and effective on-chip decoupling capacitances, the ripple on the analog power supply is attenuated. The attenuation is increased with the ripple frequency increases. As a result, the higher frequency the ripple is, the less impact on the performance of the modulator.

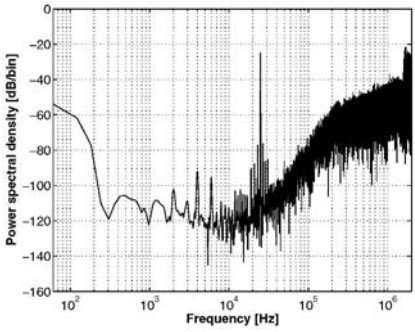
Fig. 4.48 shows the output spectrum of the modulator with different ripple frequencies from 15 kHz to 30 kHz. The same trend can be found.

If the ripple frequency is further increased beyond the input bandwidth of the modulator, the ripple component can be filtered out in the decimation filter. The only concern is the inter-modulation components. Fig. 4.49 shows the output spectrum of the modulator with different ripple frequencies from 50 kHz to 1 MHz and a larger amplitude of 200 m$V_{p-p}$. It is seen that no inter-modulation component in the signal bandwidth can be found. The ripples are buried in the quantization noise and have no impact on the performance of the modulator.

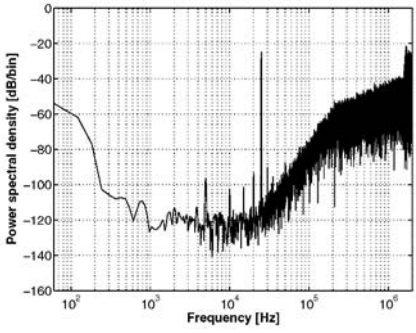
The impact of the ripple on the analog power supply rail on the performance of the 3-rd order single-loop $\Sigma$-$\Delta$ modulator was studied and the measurement results are shown. At 10-kHz, the measured PSRR of the modulator is 55 dB. Due to the local on-chip decoupling capacitances on the analog power supply rail, the ripple peak is decreased while the ripple frequency increases. Further increasing the ripple frequency results



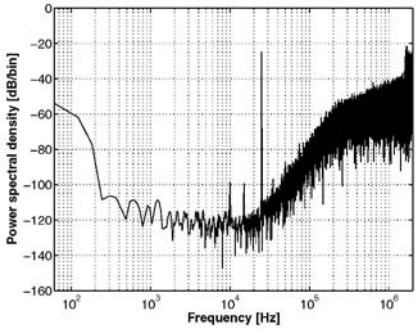

(a) Measured output spectrum with a 1-kHz, 50-m$V_{p-p}$ ripple on the analog power supply.




(b) Measured output spectrum with a 2-kHz, 50-m$V_{p-p}$ ripple on the analog power supply.

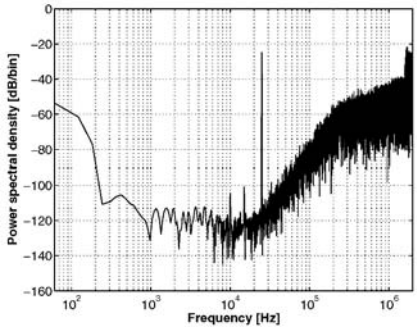



(c) Measured output spectrum with a 5-kHz, 50-m$V_{p-p}$ ripple on the analog power supply.

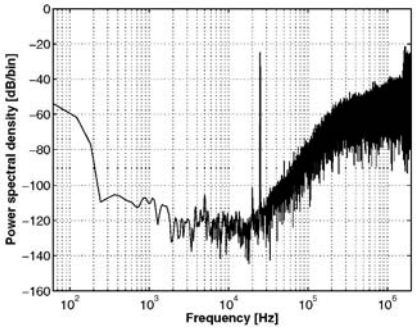



(d) Measured output spectrum with a 10-kHz, 50-m$V_{p-p}$ ripple on the analog power supply.

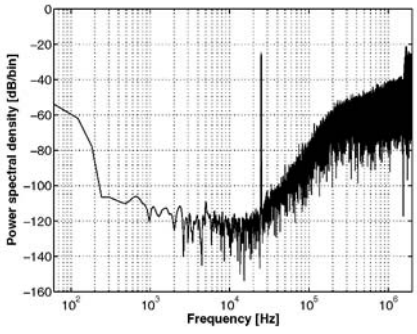
Figure 4.47: Measured output spectrum with a 50-m$V_{p-p}$ ripple and different ripple frequencies on the analog power supply.



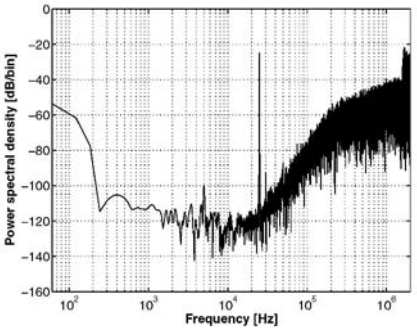

(a) Measured output spectrum with a 15-kHz, 50-m$V_{p-p}$ ripple on the analog power supply.




(b) Measured output spectrum with a 20-kHz, 50-m$V_{p-p}$ ripple on the analog power supply.

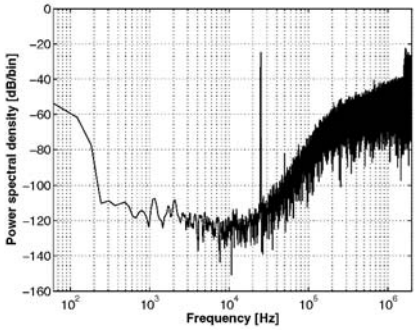



(c) Measured output spectrum with a 30-kHz, 50-m$V_{p-p}$ ripple on the analog power supply.

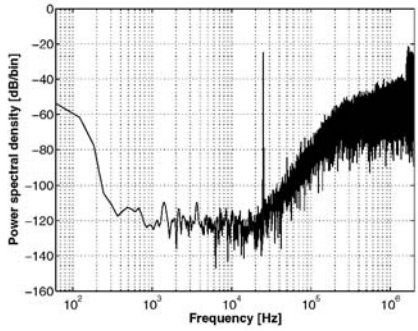



(d) Measured output spectrum with a 30-kHz, 150-m$V_{p-p}$ ripple on the analog power supply.

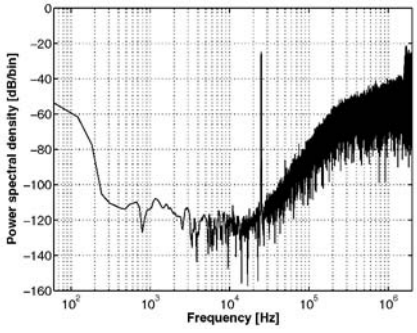
Figure 4.48: Measured output spectrum with a 150-m$V_{p-p}$ ripple and different ripple frequencies on the analog power supply.



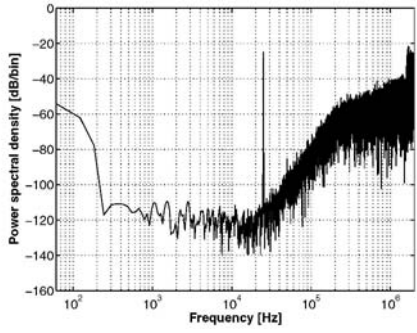

(a) Measured output spectrum with a 50-kHz, 200-m$V_{p-p}$ ripple on the analog power supply.




(b) Measured output spectrum with a 100-kHz, 200-m$V_{p-p}$ ripple on the analog power supply.




(c) Measured output spectrum with a 200-kHz, 200-m$V_{p-p}$ ripple on the analog power supply.



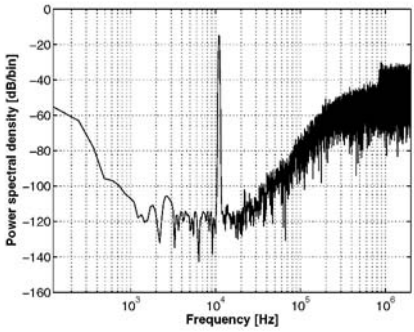

(d) Measured output spectrum with a 1-MHz, 200-m$V_{p-p}$ ripple on the analog power supply.

Figure 4.49: Measured output spectrum with a 200-m$V_{p-p}$ ripple and different ripple frequencies on the analog power supply.

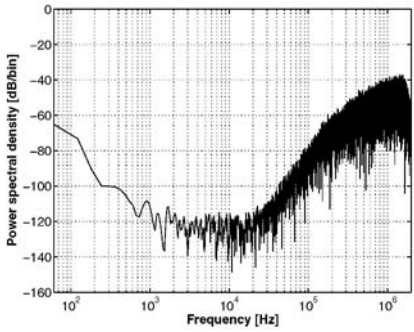
into a higher attenuation of the ripple on the analog power supply. By applying a first-order off-chip RC decoupling network in the analog power supply, the impact of the supply ripple to the modulator performances is greatly reduced. A PSRR of more than 70 dB can be achieved by using both the on-chip and off-chip decoupling capacitances.

### 4.5.4 Measurement on Low-Frequency Noise Floor

In the measurement result shown in Fig. 4.50, the low-frequency noise floor of the designed Σ-Δ modulator is not explicitly shown. The noise level at low-frequencies, i.e. few hundred Hz, is high. The question arises on what these low-frequency components are. One explanation is that they are spectral leakage from the DC component due to the limited number of FFT points. In the Σ-Δ modulator circuit, the offset of the first integrator is always present, resulting into a DC component in the output spectrum. A non-ideal window used in the FFT algorithm and a limited number of FFT points give a spectral leakage from this DC component. On the other hand, the device noise, especially the 1/f noise, is mixed with the leakage, making it difficult to determine the real circuit noise level.




(a) Measured output spectrum with an 11-kHz input signal (32768 points FFT).

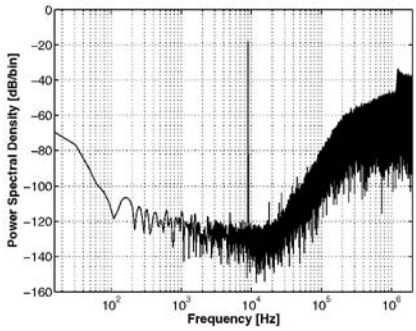



(b) Measured noise-floor (32768 points FFT).

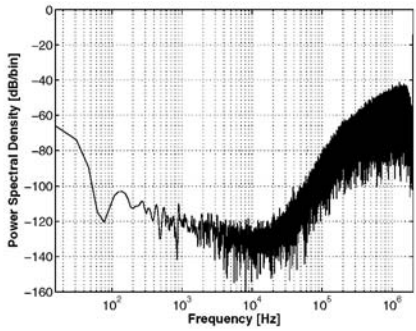
Figure 4.50: Measured output spectrum with a 4-MHz sampling frequency(32768 points FFT).

To reveal the source of these low-frequency components, some additional measurements are performed. Firstly, more FFT points are taken to increase the FFT resolution. The result shown in Fig. 4.50 is derived from 32 kb data. With some efforts, the same measurement is done with 258048 bit data, which is the maximum capacity of the equipment, shown in Fig. 4.51. It is seen that the low-frequency noise floor decreases compared to the result from 32 kb data. For instance, the noise floor below 1 kHz is decreased. However, the noise floor below 100 Hz is still high.

To separate the real circuit noise from the DC leakage, the sampling frequency has




(a) Measured output spectrum with a 9-kHz input signal (258048 points FFT).




(b) Measured noise-floor (258048 points FFT).

Figure 4.51: Measured output spectrum with a 4-MHz sampling frequency (258048 points FFT).

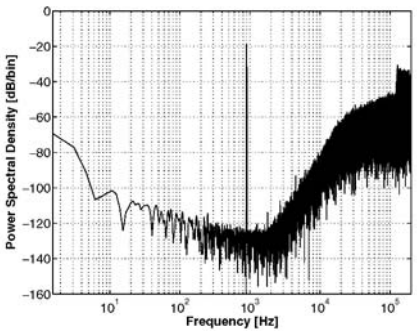
been reduced from 4 MHz to 400 kHz and the signal frequency has been reduced as well. The result is shown in Fig. 4.52. It is seen that above 10 Hz, the noise floor is kept below -100 dB. Although the DC leakage is not completely excluded from the result, at least it can be concluded that at 10 Hz a SNR of more than 80 dB has been achieved. Attempts to further reduce the sampling frequency to 40 kHz failed due to the leakage of the capacitance. Shown in Fig. 4.53, the noise shaping has been ruined by the charge leakage of the on-chip capacitors. However, the noise level between 1 Hz to 10 Hz is not larger than the noise level between 100 Hz to 1 kHz

Using the increased FFT point and reduced sampling frequency, the low-frequency noise floor of the $\Sigma$-$\Delta$ modulator in a 90-nm standard digital CMOS technology has been determined. The result shows that the low-frequency component on the output spectrum of the $\Sigma$-$\Delta$ modulator is mainly the leakage from the DC offset. For the designed $\Sigma$-$\Delta$ modulator, the measurement shows that the SNR achieves 80 dB at 10 Hz.

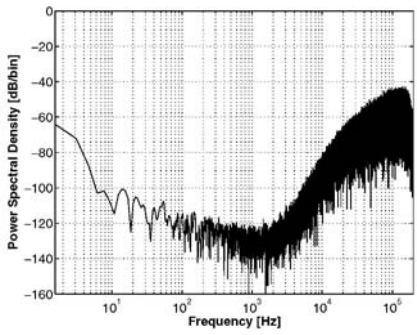
## 4.6 Conclusion

In this chapter, the circuit level approach of the low-power low-voltage $\Sigma$-$\Delta$ ADC design in nanometer CMOS is discussed. By introducing low-power low-voltage building blocks at circuit level, high-performance $\Sigma$-$\Delta$ modulators in nanometer CMOS technologies can be implemented.

Firstly, a gain-enhanced current-mirror OTA is introduced. By exploiting only the single-stage of an OTA, the gain is enhanced by using a current shunt. Rail-to-rail output swing is another feature of the OTA. Implemented with a 0.25-$\mu$m CMOS technology, the test OTA achieves a GBW of 1.2 MHz while driving an 18-pF load and




(a) Measured output spectrum with a 900-Hz input signal (258048 points FFT).




(b) Measured noise-floor (258048 points FFT).

Figure 4.52: Measured output spectrum with a 400-kHz sampling frequency (258048 points FFT).

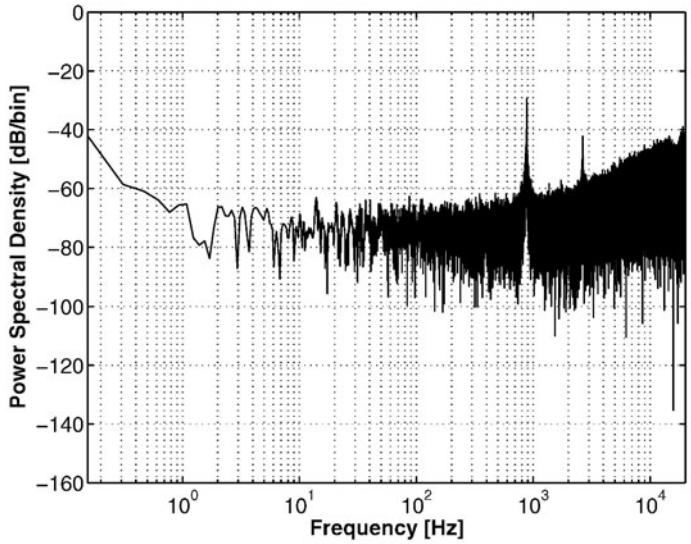



Figure 4.53: Measured output spectrum with a 900-Hz input signal and a 40-kHz sampling frequency (258048 points FFT).

consumes about 8-$\mu$W power in a 0.8-V supply voltage. Good power efficiency is achieved in this design. Two-stage OTA design is discussed as well in this chapter.

Then a low-power low-voltage switched-capacitor $\Sigma$-$\Delta$ modulator implemented in a standard 90-nm CMOS technology is presented. By proper topology selection, the modulator enables the use of single-stage OTAs with rail-to-rail output swing in a nanometer CMOS technology. A gain enhancement technique is adopted in the OTA to satisfy the distortion requirements of the modulator. A metal-wall structure is employed to implement the capacitance in this standard digital technology. This capacitance has good matching properties and higher unit capacitance, which helps to reduce chip area. Special measures are taken in the circuit design to reduce power consumption. The peak SNR reaches 85 dB and the dynamic range is 88 dB in a 20-kHz signal bandwidth. The total power consumption is 140 $\mu$W under a 1-V power supply. The results have proven the feasibility of implementing high-performance $\Sigma$-$\Delta$ ADCs in nanometer standard digital CMOS technologies. Compared to other CMOS technologies, nanometer CMOS technologies (such as a 90 nm technology) have considerable advantages in the implementation of low-power low-voltage $\Sigma$-$\Delta$ modulators.

Extensive verification of the PSRR and low-frequency noise floor are also presented in this chapter.

Chapter 5

# Low-Power Low-Voltage Σ-Δ ADC Design in Nanometer CMOS: System Level Approach

## 5.1 Introduction

Driven by the speed demand of digital circuits, in recent years the deep-submicron CMOS technology is pacing rapidly into the 100-nano meter range. As a consequence, the power supply voltage drops below 1 V earlier than expected. On the other hand, portable electronics with low-voltage operation find big markets. All these factors make the low-voltage circuits a hot topic. The low supply voltage constraint makes the analog design more challenging due to the reduced signal swing. As a major building block, the ADC is widely used in mixed-signal circuits. As an interface between the analog world to the digital circuit, the ADC is implemented with the same technology as the digital circuitry hence the power supply voltage reduction is inevitable. The decrease of the supply voltage obviously results into analog circuit performance degradation. Generally speaking, to maintain the same dynamic range on a system, the noise floor should be lowered while the signal swing is reduced. So do the distortion components. Unfortunately, as the supply voltage drops, the distortion tends to be more severe.

Among different ADCs, Σ-Δ ADCs are most suitable for high-resolution applications due to their high linearity feature. The high linearity is acquired by using the intrinsically linear 1-bit quantizer and oversampling technique. However, the non-idealities in the building blocks strongly affect the performance. To design a Σ-Δ ADC, the main effort is to fight the non-idealities of building blocks. The reduced supply voltage makes these constraints even tighter. Among them, the most important one is the distortion problem in high resolution Σ-Δ ADCs [Lee85]. Another problem with low-voltage design is that a lower noise-floor is required for the same dynamic range, which leads to difficulties to design building blocks [San98]. Many efforts have been done at the circuit level with a lot of trade-offs and compromises.

Circuit level problems can be easily solved at the system level. In this chapter, the Σ-Δ ADC design in nanometer CMOS technologies is introduced at the system level. By introducing a novel Σ-Δ modulator topology, drawbacks of the traditional Σ-Δ modulators are overcome. The topology parameters optimized to nanometer CMOS technologies are presented. The linearity of the full feedforward Σ-Δ modulator is analyzed. Then the circuit implementation of the full feedforward Σ-Δ modulator is introduced. Two design examples in a 180-nm and in a 130-nm CMOS technologies are

presented. Comparison to the state-of-the-art is also provided to evaluate the proposed design.

## 5.2 The Full Feedforward Σ-Δ ADC Topology

Feedforward is the complement of feedback in a control system. By applying feedforward in Σ-Δ modulators, a variant of Σ-Δ modulator topologies can be realized and some unique characteristics can be obtained.

Shown in Fig. 5.1, the input signal is fully fedforward to the quantizer and the Σ-Δ loop processes only the quantization noise [Sil01] in this Σ-Δ modulator. The signal and quantization noise transfer function is:

$$H_x(z) = 1 \tag{5.1}$$

$$H_e(z) = \frac{1}{1 + H(z)} \tag{5.2}$$

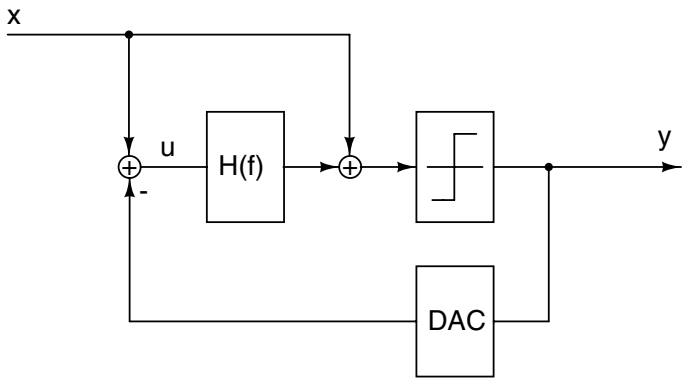



Figure 5.1: Block diagram of the full feedforward Σ-Δ modulator.

Compared to the traditional Σ-Δ modulator, shown in Fig. 3.13, the quantization noise transfer function is the same, as shown in (3.16); while the signal transfer function is ideally unity in the full feedforward Σ-Δ modulator topology. The unity signal transfer function suggests that the harmonic distortion due to nonidealities in the modulator's loop filter can be significantly reduced. In the traditional Σ-Δ modulator, the input seen by the first integrator is the error signal $u$ between the input $x$ and the output $y$. Since the output $y$ is a delayed version of $x$ in the time domain, the delay introduced by the signal transfer function causes the error signal $u$ to contain a high-pass filtered version of the input signal $x$, which is restored to its full amplitude by the integrators [Sil01]. As a result, the swings inside the filter loop are high. From equation (3.9), the transfer function of the traditional Σ-Δ modulator, the input signal $U_t(z)$ of the loop

filter is:

$$U_t(z) = X(z) - Y(z) = [1 - H_x(z)]X(z) - H_e(z)E(z) \tag{5.3}$$

It is clearly seen that for traditional Σ-Δ modulators, the input signal of the loop filter is not only the quantization noise, but also a high-pass filtered input signal $X(z)$. In the full feedforward Σ-Δ modulator, the input of the first integrator is also the error signal $u$ between the input $x$ and the output $y$. However, due to the fully fedforward input signal to the quantizer, the output $y$ is not delayed. Consequently, the signal pass through the loop filter in the full feedforward Σ-Δ modulator is the quantization noise, which is much smaller compared to the input signal in amplitude. Equation (5.3) demonstrates that due to the unity signal transfer function, the input signal $U_f(z)$ of the loop filter only contains the quantization noise:

$$U_f(z) = -H_e(z)E(z) \tag{5.4}$$

This is a very attractive characteristic since the input signal does not pass through the loop filter. Consequently, the non-linearity of the loop filter will not contaminate the signal. Moreover the quantization noise is smaller in amplitude compared to the input signal, which suggests that the harmonic distortion generated inside the loop filter can be decreased due to the smaller signal swings. The reduction of the internal signal swings also relaxes the output swing requirement for the building blocks, which is a tough requirement in low-voltage designs in nanometer CMOS technologies.

### 5.2.1 Single-Loop Single-Bit Full Feedforward Σ-Δ Modulators

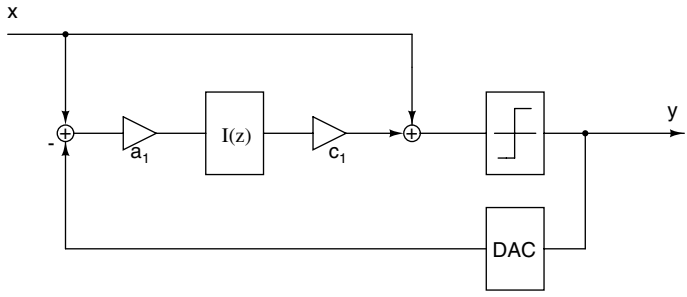



Figure 5.2: Block diagram of the first-order single-loop full feedforward Σ-Δ modulator.

In Fig. 5.2, by introducing loop coefficients into the filter loop, the first-order full feedforward Σ-Δ modulator is shown. The signal and the noise transfer function are:

$$H_x(z) = 1 \tag{5.5}$$

$$H_e(z) = \frac{1 - z^{-1}}{1 + (a_1c_1 - 1)z^{-1}} \tag{5.6}$$

The order of the loop filter in the full feedforward topology can be increased by inserting more integrators inside the loop. For each integrator stage, there is a full feedforward branch associated with it. All the full feedforward branches are summed together and passed to the quantizer. Represented in Fig. 5.3, Fig. 5.4 and Fig. 5.5 are the block diagram of the second-order, third-order and fourth-order full feedforward Σ-Δ modulators, respectively.

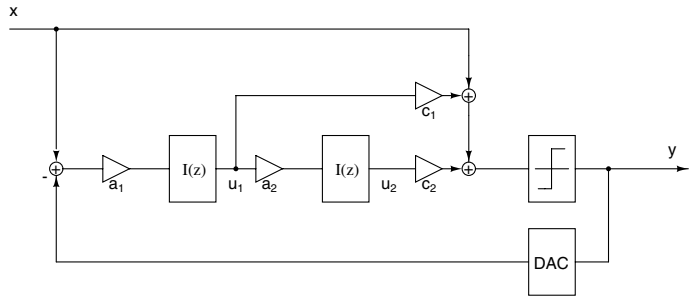



Figure 5.3: Block diagram of the second-order single-loop full feedforward Σ-Δ modulator.

The insertion of the loop coefficients does not change the signal transfer function. This is one of the characteristics of the full feedforward topology. The signal transfer function remains unity, no matter what loop coefficients are chosen. The noise transfer function is related to the loop coefficients. If $a_1c_1 = 1$ then the noise transfer function is the ideal first-order Σ-Δ modulator noise transfer function in (3.16). The full feedforward Σ-Δ modulator shows exactly the same behavior with the traditional Σ-Δ modulator. Behavioral simulations are used to determine the loop coefficients and the performance of the full feedforward Σ-Δ modulator.

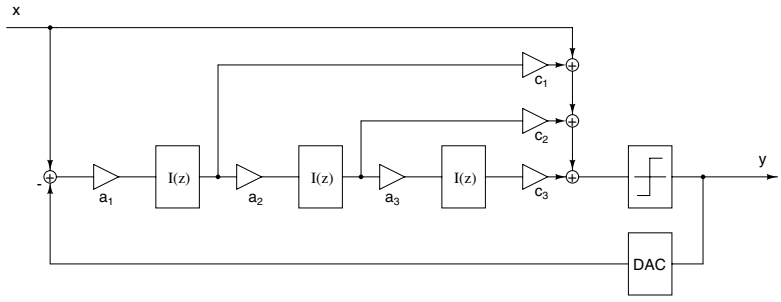



Figure 5.4: Block diagram of the third-order single-loop full feedforward Σ-Δ modulator.

Taking a closer look at the second-order full feedforward Σ-Δ modulator, the input

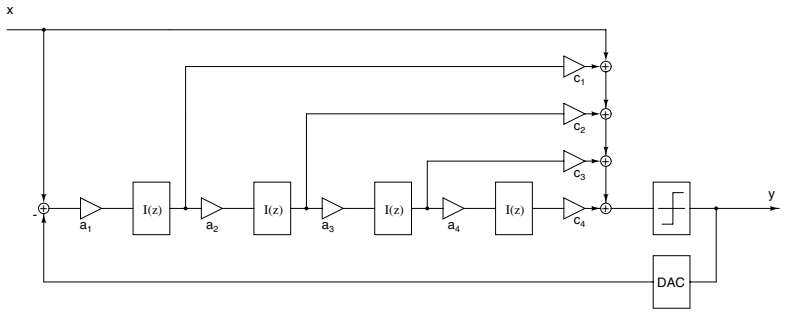



Figure 5.5: Block diagram of the fourth-order single-loop full feedforward Σ-Δ modulator.

of the first integrator is the difference of the quantizer input and the output, i.e. the quantization noise itself. The loop filter only processes the quantization noise in the ideal case. This can be seen in Fig. 5.6. It can be seen that in the full feedforward Σ-Δ modulator, the signal power inside the Σ-Δ modulator loop is suppressed significantly compared to the traditional Σ-Δ modulator. Since the quantizer is a single-bit one, the cancellation of the input signal and the output signal is not perfect due to the large quantization noise. As a result, some signal components can be seen in the integrator outputs, as shown in Fig. 5.6.

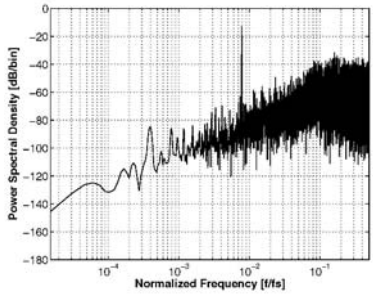
The signal transfer function and the quantization noise transfer function of the second-order full feedforward Σ-Δ modulator is:

$$H_x(z) = 1 \tag{5.7}$$

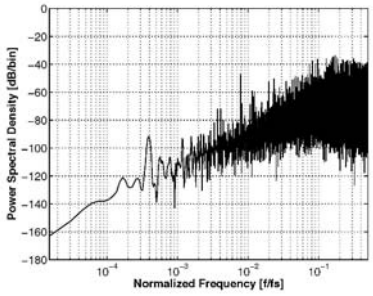
$$H_e(z) = \frac{(1-z^{-1})^2}{(a_1a_2c_1c_2 - a_1c_1 + 1)z^{-2} + (a_1c_1 - 2)z^{-1} + 1} \tag{5.8}$$

The big question is to optimize the loop coefficients for the full feedforward Σ-Δ modulators to achieve the best performance and maintain loop stability. Analytical tools are not well suitable because of the strong non-linearity of the single-bit quantizer. To optimize the loop coefficients for best SNR performance of a full feedforward Σ-Δ modulator, behavioral simulations are utilized for their simplicity and intuition. A batch of behavioral simulations is performed to select the best performance. Shown in Fig. 5.7 is the simulated SNR of a first-order single-bit full feedforward Σ-Δ modulator for different combinations of the loop coefficients a and c. It is seen that there are regions where the SNR of the modulator reaches its peak value. For the second-order full feedforward Σ-Δ modulator, since there are four loop coefficients involved in the simulation, only the simulation on coefficients a is performed while the coefficients c are fixed to [2 1]. The simulation results are presented in Fig. 5.8.

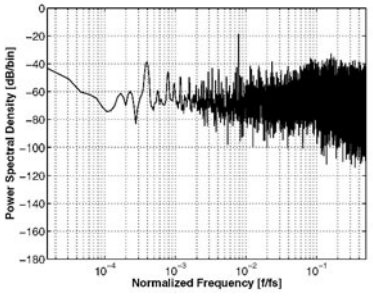
Applying the same type of simulation to the third-order and the fourth-order full feedforward Σ-Δ modulators, optimized loop coefficients are obtained. The full feedforward Σ-Δ modulator performance is summarized in Table 5.1. Compared to the



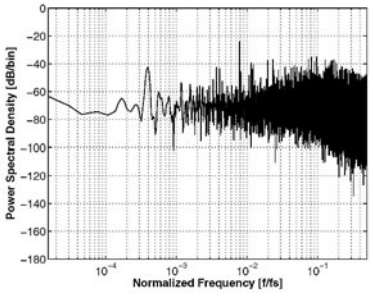

(a) Spectrum of the first integrator output in a traditional second-order Σ-Δ modulator.



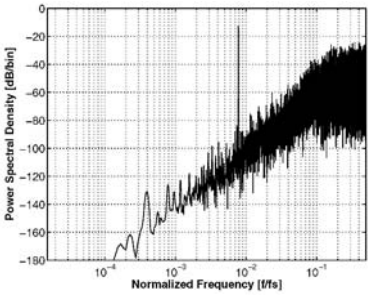

(b) Spectrum of the first integrator output in a full feedforward second-order Σ-Δ modulator.



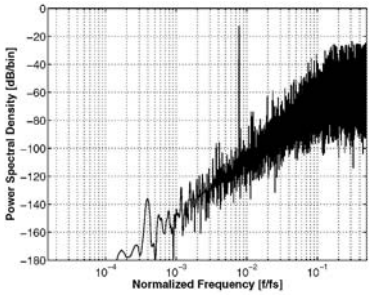

(c) Spectrum of the second integrator output in a traditional second-order Σ-Δ modulator.




(d) Spectrum of the second integrator output in a full feedforward second-order Σ-Δ modulator.

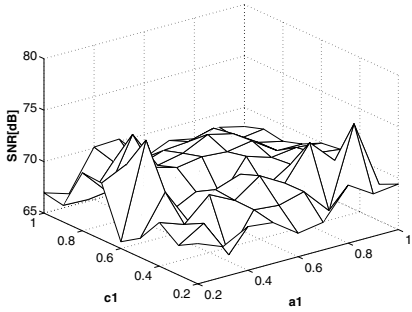



(e) Spectrum of the quantizer output in a traditional second-order Σ-Δ modulator.

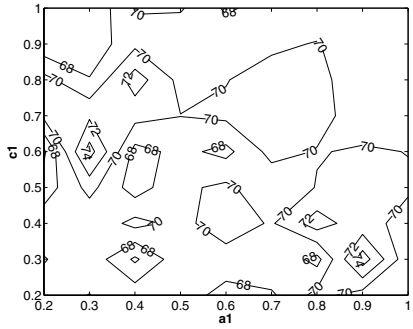



(f) Spectrum of the quantizer output in a full feedforward second-order Σ-Δ modulator.

Figure 5.6: Simulated output spectrum of the first integrator, second integrator and the quantizer for both second-order traditional Σ-Δ modulator and full feedforward Σ-Δ modulator. The oversampling-ratio is 64.

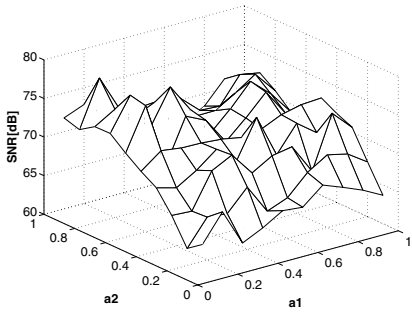



(a) Surface plot of the SNR for the first-order full feedforward Σ-Δ modulator.

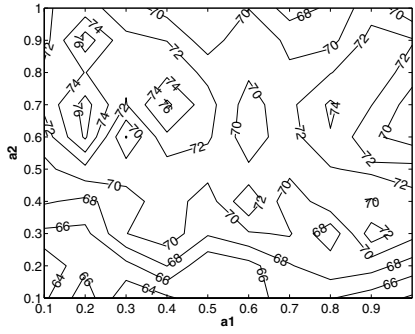



(b) Contour plot of the SNR for the first-order full feedforward Σ-Δ modulator.

Figure 5.7: Behavioral simulation to determine the coefficients of the first-order single-bit full feedforward Σ-Δ modulator. The oversampling-ratio is 64.




(a) Surface plot of the SNR for the second-order full feedforward Σ-Δ modulator.




(b) Contour plot of the SNR for the second-order full feedforward Σ-Δ modulator.

Figure 5.8: Behavioral simulation to determine the coefficients of the second-order single-bit full feedforward Σ-Δ modulator. The oversampling-ratio is 64 and coefficients c=[2 1].

Table 5.1: Loop coefficients and modulator performances for second to fourth-order single-loop single-bit full feedforward Σ-Δ modulators.

| Loop Coefficients | a=[ 0.3, 0.7 ] c=[ 2 , 1 ] | | a=[ 0.1, 0.3, 0.2 ] c=[ 1 , 1 , 1 ] | | a=[ 0.2, 0.4, 0.1, 0.1 ] c=[ 1 , 1 , 1 , 2 ] | |
|---|---|---|---|---|---|---|
| Loop order | 2 | | 3 | | 4 | |
| OSR | $SNR_p$ | OL | $SNR_p$ | OL | $SNR_p$ | OL |
| 16 | 45 | 0.95 | 41 | 0.85 | 22 | 0.9 |
| 32 | 62 | 0.9 | 63 | 0.85 | 63 | 0.85 |
| 64 | 78 | 0.9 | 86 | 0.85 | 95 | 0.75 |
| 128 | 102 | 0.9 | 109 | 0.8 | 125 | 0.75 |

performance of the traditional Σ-Δ modulator topology shown in Table 3.1, the full feedforward Σ-Δ topology offers the same SNR under the same conditions. However, the overload level is significantly increased. The explanation is that the loop processes the quantization noise, which is much smaller than the input signal itself in amplitude, in the full feedforward Σ-Δ topology. Therefore, the ability to handle larger signal is increased without overloading the quantizer.

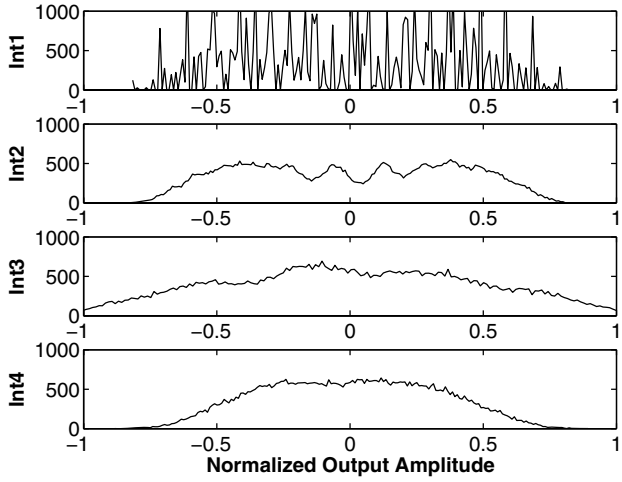



Figure 5.9: Output level histogram of the first to fourth integrators for a fourth-order single-bit traditional Σ-Δ modulator. The input level is set to 0.5 of the reference.

Fig. 5.9 gives the histogram of the output level of the different integrator stages for a fourth-order single-bit traditional Σ-Δ modulator while the input level is set to half of the reference level. As a comparison, the histogram of the output level of different

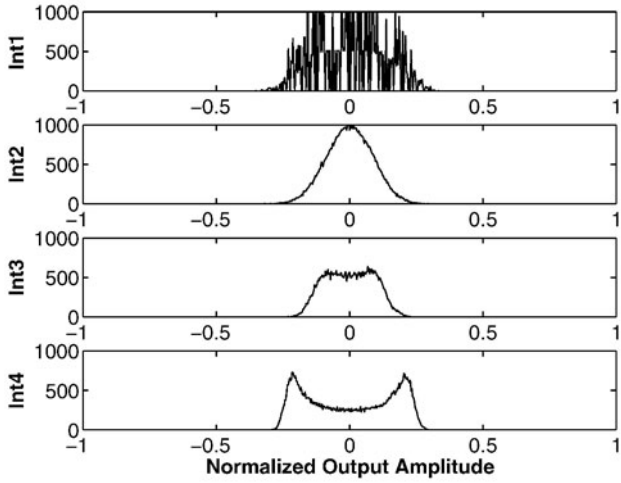



Figure 5.10: Output level histogram of the first to fourth integrators for a fourth-order single-bit full feedforward Σ-Δ modulator. The input level is set to 0.5 of the reference.

integrator stages for a fourth-order single-bit full feedforward Σ-Δ modulator under the same condition is presented in Fig. 5.10. The output level of the integrators in the full feedforward Σ-Δ modulator topology is significantly reduced compared to that in the traditional Σ-Δ modulator topology.

In summary, the advantages of the full feedforward Σ-Δ modulator over the traditional Σ-Δ modulator are described below:

- **Reduced sensitivity to the building block non-idealities.**
- **Reduced internal signal swing.**
- **Improved overload level. Hence improved dynamic range.**
- **Only one DAC feedback path.**
- **Simplicity of cascaded architectures.**

### 5.2.2 Single-Loop Multibit Full Feedforward Σ-Δ Modulators

A multibit quantizer can also be used in the full feedforward Σ-Δ topology to increase the SNR of the Σ-Δ modulator. For multibit full feedforward Σ-Δ modulators, smaller quantization noise power of the multibit quantizer reduces the signal level pass through the loop filter. As a result, internal swings inside the filter loop decrease further compared to the single-bit full feedforward Σ-Δ topology, which is helpful to reduce the

Table 5.2: Loop coefficients and modulator performances for second to fourth-order single-loop four-bit full feedforward Σ-Δ modulators.

| Loop Coefficients | a=[ 1 , 1 ] c=[ 2 , 1 ] | | a=[ 0.5, 1.0, 1.0 ] c=[ 4 , 2 , 1 ] | | a=[ 0.6, 1.0, 1.0, 0.7 ] c=[ 4 , 4 , 2 , 1 ] | |
|---|---|---|---|---|---|---|
| Loop order | 2 | | 3 | | 4 | |
| OSR | $SNR_p$ | OL | $SNR_p$ | OL | $SNR_p$ | OL |
| 16 | 77 | 1 | 82 | 0.88 | 96 | 0.9 |
| 32 | 92 | 1 | 104 | 0.92 | 124 | 0.9 |
| 64 | 113 | 1 | 126 | 0.95 | 152 | 0.88 |
| 128 | 132 | 1 | 149 | 0.92 | 182 | 0.86 |

harmonic distortion components generated inside the loop filter. The overload level is also increased compared to the traditional Σ-Δ modulator topology.

The optimized loop coefficients and performance is shown in Table 5.2. These loop coefficients are obtained by running behavioral simulations. It is interesting to see that the overload level is 1 in the second-order full feedforward Σ-Δ modulator.

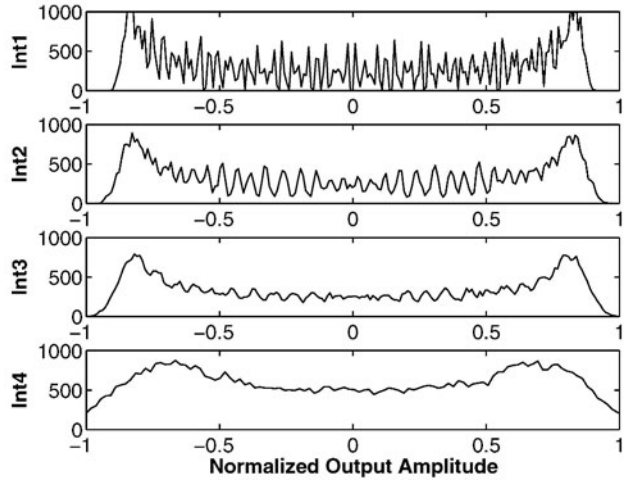



Figure 5.11: Output level histogram of the first to fourth integrators for a fourth-order 4-bit traditional Σ-Δ modulator. The input level is set to 0.85 of the reference.

Fig. 5.11 illustrates the histogram of the output level of different integrator stages for a fourth-order four-bit traditional Σ-Δ modulator while the input level is set to 0.85 of the reference level. As a comparison, the histogram of the output level of different integrator stages for a fourth-order four-bit full feedforward Σ-Δ modulator order

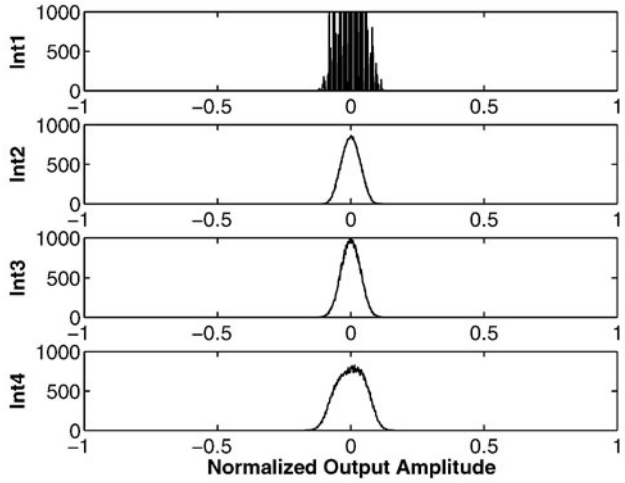



Figure 5.12: Output level histogram of the first to fourth integrators for a fourth-order 4-bit full feedforward Σ-Δ modulator. The input level is set to 0.85 of the reference.

the same condition is presented in Fig. 5.12. The output swings of the integrators in the full feedforward Σ-Δ modulator topology are significantly reduced compared to the ones in the traditional Σ-Δ modulator topology and the ones of the single-bit full feedforward Σ-Δ modulator topology. In the traditional Σ-Δ modulator, the output level is almost 100% of the reference level in all the four integrators. In the real circuit implementation, due to the output situation and output swing limitation of the integrator, such a high output level forces the reference level to be reduced. Moreover, the high output swing in the integrator generates higher distortion components, while in the full feedforward Σ-Δ modulator case, the output level is well controlled below 20% of the reference level. Consequently, the reference voltage of the full feedforward Σ-Δ modulator can be set equal to the supply voltage, utilizing the complete supply voltage and finally saving power at the system level.

The reason for the reduced output swings of the integrators is the smaller input signal of the loop filter in the multibit full feedforward Σ-Δ modulators. The use of the multibit quantizer significantly reduces the quantization noise generated. Accordingly, the input of the loop filter, which is composed by the quantization noise only in the full feedforward topology, is significantly decreased.

The nonlinearity problem in the DAC still exists in the full feedforward Σ-Δ modulator topology. As mentioned before, the dynamic element matching technique is a good remedy for this problem.

Due to the high-linearity and the reduced signal swing inside the filter loop, the multibit full feedforward Σ-Δ modulator is a promising topology for wideband Σ-Δ ADC designs in nanometer CMOS technologies.

### 5.2.3 Cascaded Full Feedforward Σ-Δ Modulators

As mentioned in Chapter 3, several low-order Σ-Δ modulators can be cascaded to achieve high-order noise shaping without the stability concern. To cascade several Σ-Δ modulators, the quantization noise should be coupled to the next stage to perform noise cancellation. In the traditional Σ-Δ modulators, additional subtracting is needed to pick the quantization noise up, which costs extra hardware, as illustrated in Fig. 3.25. The full feedforward Σ-Δ modulator is easy to be cascaded due to the simplicity of the topology [Sil04].

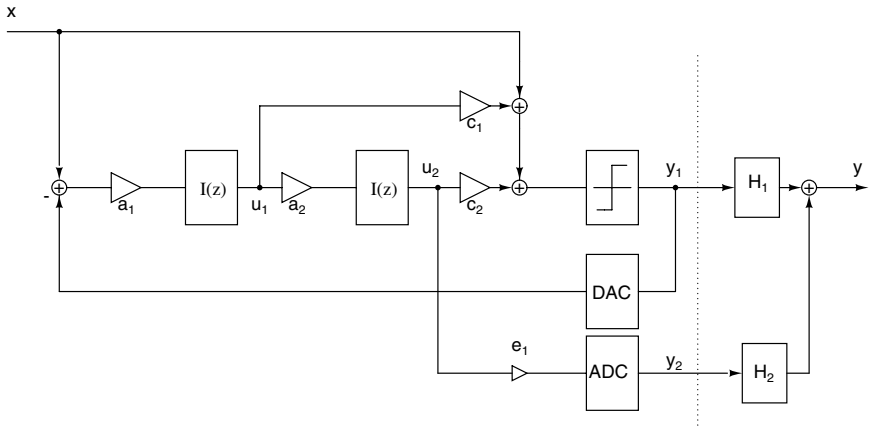



Figure 5.13: The noise cancelling diagram of the full feedforward Σ-Δ modulator.

To make a cascaded Σ-Δ modulator, the quantization noise must be extracted. In the cascaded Σ-Δ modulators, the first stage of the cascaded is normally a first-order or second-order Σ-Δ modulator for its intrinsic stability. Assuming that the gain in the quantizer is 1, for a first-order full feedforward Σ-Δ modulator, the output of the last integrator can be calculated as:

$$U(z) = \frac{-a_1 I(z) \cdot E_1(z)}{1 + a_1 c_1 I(z)} = \frac{-a_1 z^{-1} E_1(z)}{1 + (a_1 c_1 - 1) z^{-1}} \tag{5.9}$$

where $I(z)$ is the transfer function of the integrator and $E_1(z)$ is the quantization noise of the first Σ-Δ modulator. If $a_1 c_1$ is chosen to be 1, then the output of the last integrator is:

$$U(z) = a_1 z^{-1}(-E_1(z)) \tag{5.10}$$

which is a delayed version of the quantization noise. For a second-order full feedforward Σ-Δ modulator as the first stage of the cascaded topology, as depicted in Fig.

Table 5.3: Topology parameters and modulator performance for the cascaded 2-1 full feedforward Σ-Δ modulator.

| Topology | Cascaded 2-1 full feedforward Σ-Δ | | | |
|---|---|---|---|---|
| Loop Coefficients | ( $a_1$, $a_2$, $a_3$, $c_1$, $c_2$, $c_3$, $e_1$) ( 0.5, 0.25, 0.5, 4, 2, 1, 1) | | ( $a_1$, $a_2$, $a_3$, $c_1$, $c_2$, $c_3$, $e_1$) ( 0.5, 0.7, 0.5, 2, 1, 1, 1) | |
| OSR | $SNR_p$ | OL | $SNR_p$ | OL |
| 16 | 51 | 0.95 | 57 | 0.95 |
| 32 | 71 | 0.9 | 78 | 0.85 |
| 64 | 94 | 0.9 | 100 | 0.85 |
| 128 | 115 | 0.9 | 124 | 0.85 |

5.13, the output of the last integrator is:

$$U(z) = \frac{-a_1 a_2 I^2(z) \cdot E_1(z)}{1 + a_1 c_1 I(z) + a_1 a_2 c_1 c_2 I^2(z)} \tag{5.11}$$

If the loop coefficients are chosen as:

$$a_1 c_1 = 2 \tag{5.12}$$

$$a_1 a_2 c_1 c_2 = 1 \tag{5.13}$$

Then the output of the last integrator is calculated as:

$$U(z) = a_1 a_2 z^{-2}(-E_1(z)) \tag{5.14}$$

which is only a delayed version of the quantization noise. From the expression it is seen that the quantization noise is readily available at the last integrator output in a full feedforward Σ-Δ modulator, as long as some conditions are fulfilled. There is no need to subtract the quantization noise from the Σ-Δ modulator. Therefore, the output of the last integrator in the first full feedforward Σ-Δ modulator can be directly fed into the second Σ-Δ modulator to construct a full feedforward cascaded Σ-Δ modulator. Accordingly, the two transfer functions in the post processing block, presented in Fig. 5.13, are to be designed as:

$$H_1(z) = z^{-2} \tag{5.15}$$

$$H_2(z) = \frac{(1 - z^{-1})^2}{a_1 a_2 e_1} \tag{5.16}$$

Taking the cascaded 2-1 full feedforward Σ-Δ modulator as an example, shown in Fig. 5.14, the output of the first Σ-Δ modulator can be obtained from (5.7) and (5.8). Then the output of the first and second cascaded Σ-Δ modulator are:

$$Y_1(z) = X(z) + (1 - z^{-1})^2 \cdot E_1(z) \tag{5.17}$$

$$Y_2(z) = X_1(z) + (1 - z^{-1}) \cdot E_2(z) \tag{5.18}$$

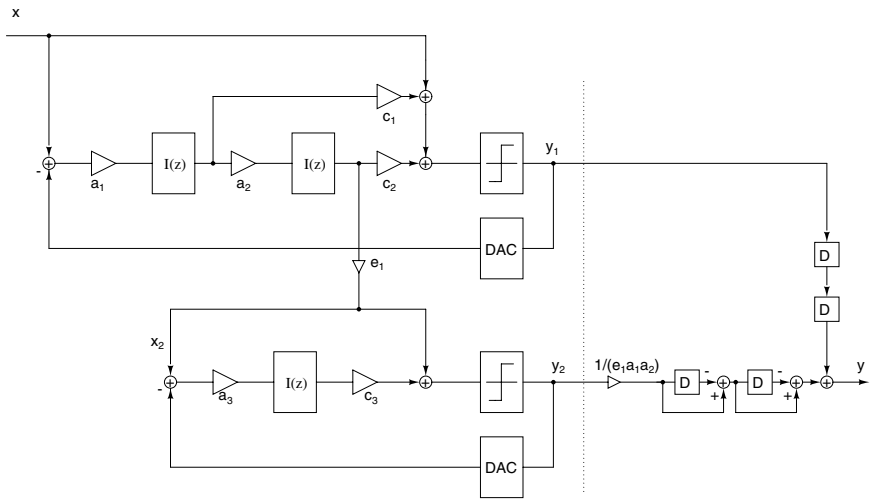



Figure 5.14: Block diagram of the third-order cascaded 2-1 full feedforward Σ-Δ modulator.

The final output of the cascaded Σ-Δ modulator is:

$$\begin{aligned} Y(z) &= H_1(z)Y_1(z) + H_2(z)Y_2(z) \\ &= X(z)\cdot z^{-2} + \frac{(1-z^{-1})^3}{a_1 a_2 e_1}E_2(z) \end{aligned} \tag{5.19}$$

There is only the quantization noise from the second Σ-Δ modulator left in the output, and it is third-order noise-shaped. The quantization noise of the first Σ-Δ modulator is completely cancelled out. The signal transfer function is a delayed version of the input signal. It is also seen that the noise-shaping ability is related to the loop coefficient $e_1$. Maximizing $e_1$ will increase the SNR of the cascaded Σ-Δ modulator, however, it is restricted by the input range of the second Σ-Δ modulator. Similar to the traditional cascaded Σ-Δ modulators, the noise cancellation is also relied on the matching between the full feedforward cascaded Σ-Δ modulators.

The principle of the cascaded full feedforward Σ-Δ modulator can be also applied to realize other cascaded topologies. Fig. 5.15 shows a fourth-order cascaded 2-2 full feedforward Σ-Δ modulator composed by two second-order full feedforward Σ-Δ modulators. Fig. 5.16 shows a fourth-order cascade 2-1-1 full feedforward Σ-Δ modulator composed by a second-order full feedforward Σ-Δ modulator and two first-order full feedforward Σ-Δ modulators.

The assumption that the quantization gain equals unity is not valid for a single-bit quantizer. Consequently, the best performance is not achieved using the above mentioned coefficients. Behavioral simulations are adopted to optimize the loop coefficients. Shown in Table 5.3, there are certain performance differences between the analyzed loop coefficients and the optimized loop coefficients. The loop coefficients

from the analysis ( $a_1$, $a_2$, $a_3$, $c_1$, $c_2$, $c_3$, $e_1$) = ( 0.5, 0.25, 0.5, 4, 2, 1, 1) fulfill the requirement in (5.12), but does not provide the best performance. The optimized loop coefficients from the behavioral simulations ( $a_1$, $a_2$, $a_3$, $c_1$, $c_2$, $c_3$, $e_1$) = ( 0.5, 0.7, 0.5, 2, 1, 1, 1) result into better performance.

Finally the optimized loop coefficients and performance are summarized in Table 5.4 and Table 5.5 for fourth-order cascaded 2-2 and 2-1-1 full feedforward Σ-Δ modulators, respectively.

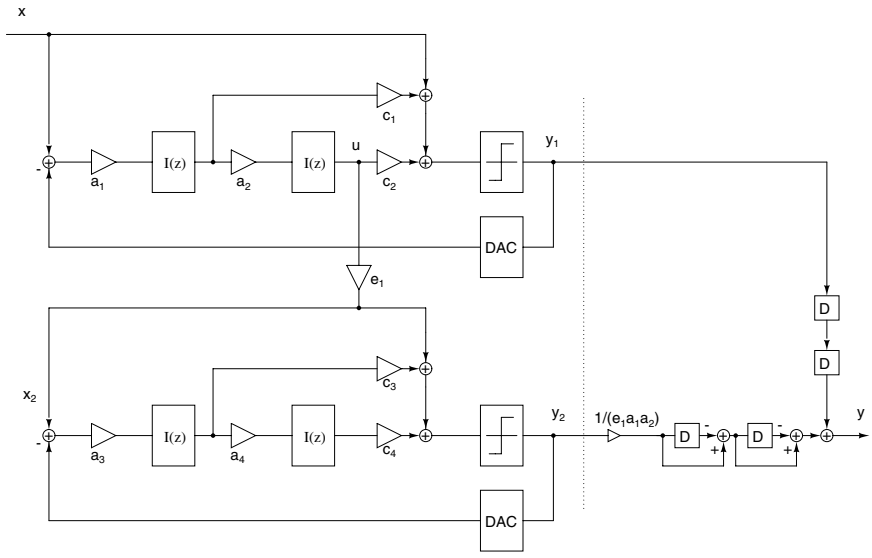



Figure 5.15: Block diagram of the fourth-order cascaded 2-2 full feedforward Σ-Δ modulator.

Table 5.4: Topology parameters and modulator performance for the cascaded 2-2 full feedforward Σ-Δ modulator.

| Topology | Cascaded 2-2 full feedforward Σ-Δ | |
|---|---|---|
| Loop Coefficients | ( $a_1$, $a_2$, $a_3$, $a_4$, $c_1$, $c_2$, $c_3$, $c_4$, $e_1$) ( 0.4, 0.8, 0.4, 0.8, 2, 1, 2, 1, 1) | |
| OSR | $SNR_p$ | OL |
| 16 | 65 | 0.95 |
| 32 | 92 | 0.89 |
| 64 | 121 | 0.88 |
| 128 | 149 | 0.85 |

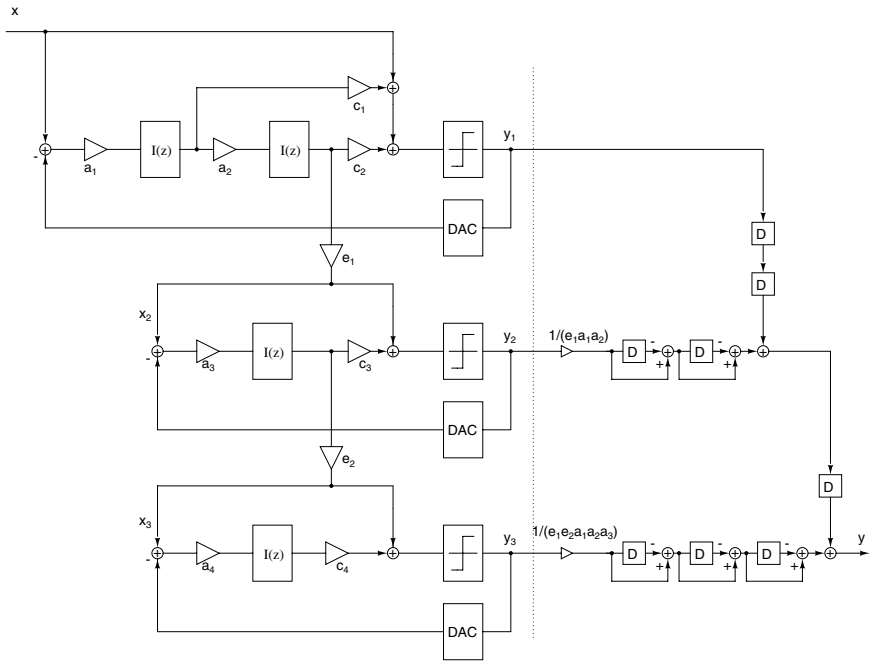



Figure 5.16: Block diagram of the fourth-order cascaded 2-1-1 full feedforward Σ-Δ modulator.

Table 5.5: Topology parameters and modulator performance for the cascaded 2-1-1 full feedforward Σ-Δ modulator.

| Topology | Cascaded 2-1-1 full feedforward Σ-Δ | |
|---|---|---|
| Loop Coefficients | ( $a_1$, $a_2$, $a_3$, $a_4$, $c_1$, $c_2$, $c_3$, $c_4$, $e_1$, $e_2$) ( 0.4, 0.8, 0.5, 0.5, 2, 1, 2, 2, 2, 2) | |
| OSR | $SNR_p$ | OL |
| 16 | 74 | 0.82 |
| 32 | 100 | 0.80 |
| 64 | 129 | 0.80 |
| 128 | 159 | 0.80 |

### 5.2.4 Performance Comparison of Full Feedforward Σ-Δ Topologies

Fig. 5.17 shows the simulated peak SNR versus the oversampling ratio for different full feedforward Σ-Δ modulator topologies. Compared to Fig. 3.29, it is seen that the full feedforward Σ-Δ modulator achieves approximately the same performance as its counterpart in traditional Σ-Δ modulator topologies.

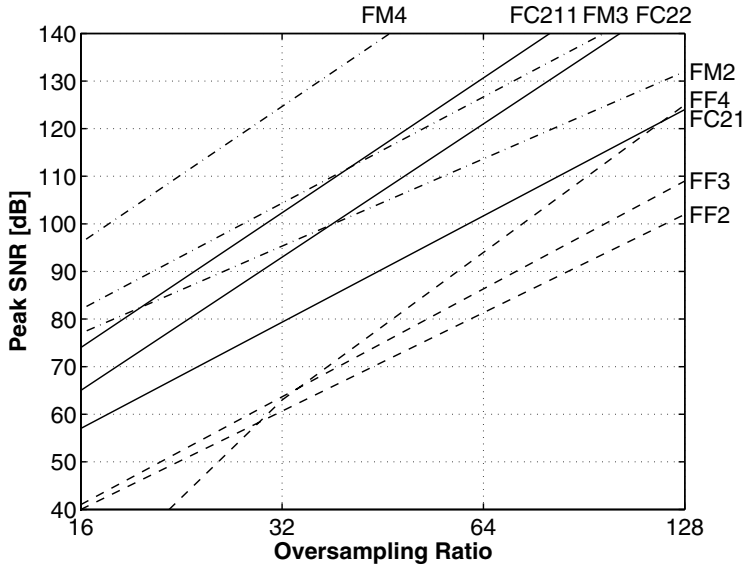



Figure 5.17: $SNR_p$ vs. oversampling ratio for different full feedforward Σ-Δ modulator topologies. FFi: i-th order single-loop full feedforward modulator; FMi: i-th order 4-bit single-loop full feedforward modulator; FCijk: Cascaded full feedforward modulator i-j-k.

## 5.3 Linearity Analysis of Σ-Δ ADC

With the evolving of the CMOS technology, the analog circuit is moving into nanometer or even nano-meter CMOS technologies. The impact nanometer technology brings to analog designers is two-fold. One is the reduction of the supply voltage and the other one is the more severe transistor characteristics degradation compared to traditional long channel transistors [San96]. The low-voltage environment forces the circuit to work under relatively large signal conditions. Hence more deviation from the biasing point and more distortion is generated. At the same time, the intrinsic gain of the MOS transistor is reduced as well, which causes more difficulties to design high-gain amplifiers.

To conclude, in nanometer CMOS technologies, it is more difficult to implement high-quality analog building blocks. Also more power should be used to achieve the same specifications, compared to traditional long-channel CMOS technologies.

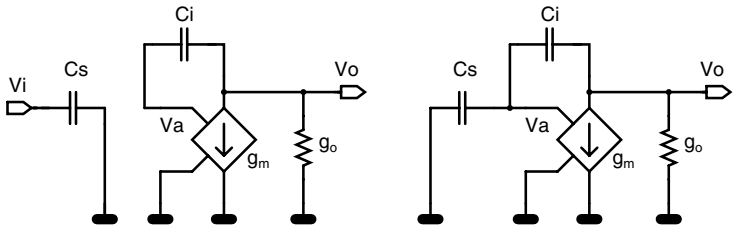



Figure 5.18: Switched capacitor integrator model using an OTA.

To gain insight in the impact of non-idealities on the switched-capacitor Σ-Δ ADC performance, behavioral simulation is used for its clarity and speed. The switched-capacitor integrator, the basic building block in switched-capacitor Σ-Δ ADCs, is the vital building block that determines the overall Σ-Δ ADC performances. For a single-ended switched-capacitor integrator, shown in Fig. 5.18, the charge balance equation can be written as

$$C_I \cdot (v_o^+ - v_a^+) = C_I \cdot (v_o^- - v_a^-) + C_S \cdot (v_i - v_a^-) \tag{5.20}$$

where $C_S$ and $C_I$ are sampling and integration capacitance respectively. Throughout this chapter, $v^+$ and $v^-$ are used to replace $v((n+1/2)T)$ and $v((n-1/2)T)$ in order to simplify the equations. The amplifier is modeled by an OTA. The input and output relationship of the OTA is

$$v_o^{\pm} = -A \cdot v_a^{\pm} \tag{5.21}$$

where A is the voltage gain of the OTA. For an ideal integrator, the gain of the OTA is infinite. The equations (5.20) and (5.21) serve as the fundamental equations of switched-capacitor integrator. Based on these equations, by adding non-idealities into them, various behavioral simulations can be carried out.

### 5.3.1 Non-Linearities Modeling in Σ-Δ ADC

There are several building block non-idealities that degrade the performance of Σ-Δ ADCs. In the switched-capacitor Σ-Δ ADCs, the main non-linearities related to distortion are the non-linear OTA gain, the non-linear capacitance and the non-linear switch. These non-linearities generate harmonics and degrade the linearity performance of the entire Σ-Δ ADC. To investigate the effects of these non-linearities, each non-linearity is modeled in the charge balance equation (5.3). Then behavior simulation is performed and final results are obtained through the simulation. In this chapter, a single bit fourth-order Σ-Δ modulator is chosen as the test vehicle to carry out all simulations and comparisons.

In modern CMOS technologies, the MIM capacitance linearity is quite good and the non-linear switch problems can be solved easily by a clock boosting technique. However, the non-linearity of the OTA is getting worse with the transistor feature size shrinking, making it the main source of non-linearity of the Σ-Δ ADCs.

### 5.3.2 Non-Linear OTA Gain Modeling in Σ-Δ ADC

The non-linearity of the OTA gain can be modeled as

$$A = A_0(1 + b_1 \cdot v_o + b_2 \cdot v_o^2) \tag{5.22}$$

where $A_O$ is the DC gain of the OTA in a small signal condition. $v_o$ is the output amplitude of the OTA and $b_1$, $b_2$ are first and second order distortion factors, respectively. According to the definition of the i-th order harmonic distortion $HD_i$ [San99], we have:

$$A = A_0(1 + 4HD_2 \cdot v_a + 12HD_3 \cdot v_a^2) \approx A_0(1 + \frac{4HD_2}{A_0}v_o + \frac{12HD_3}{A_0^2}v_o^2) \tag{5.23}$$

where $v_a$ is the input amplitude of the OTA. By comparing equation (5.23) to equation (5.22), we have:

$$b_1 = \frac{4HD_2}{A_0} \quad b_2 = \frac{12HD_3}{A_0^2} \tag{5.24}$$

Normally for a CMOS OTA, the harmonic distortion is less than 10%. Assuming the gain of the OTA is 40 dB, the coefficient $b_1$ and $b_2$ are significantly smaller than 0.1.

By replacing the gain in equation (5.21) with equation (5.22), the input-output relation of a switched-capacitor integrator can be readily obtained. By applying this relation in the behavior simulation of Σ-Δ modulators, the non-linearity of the Σ-Δ modulator can be simulated.

### 5.3.3 Linearity Performance Comparison

From the above analysis and simulations, the conclusion could be drawn that the most non-linearity source is the non-linear OTA gain. In nanometer technology, this problem is getting more severe due to the relatively large signal swing. It is difficult to completely solve this problem in the circuit level. However, this problem could be potentially solved in the Σ-Δ topology level, e.g. with the proposed full feedforward Σ-Δ modulator topology.

Fig. 5.19 shows the output spectrum of a traditional fourth-order single-loop Σ-Δ modulator with a non-linear OTA modeled with coefficient $b_1 = -0.1$ $b_2 = -0.1$. It is clear that, from Fig. 5.19, the gain non-linearity of the OTA causes large harmonic distortion in the traditional Σ-Δ modulator.

Distortion and performance simulations are performed on a fourth-order single-loop full feedforward Σ-Δ modulator topology shown in Fig. 5.5. It has some unique characteristics compared to the traditional topology. The most interesting characteristic is that the signal transfer function is unity, therefore the nonidealities in the building

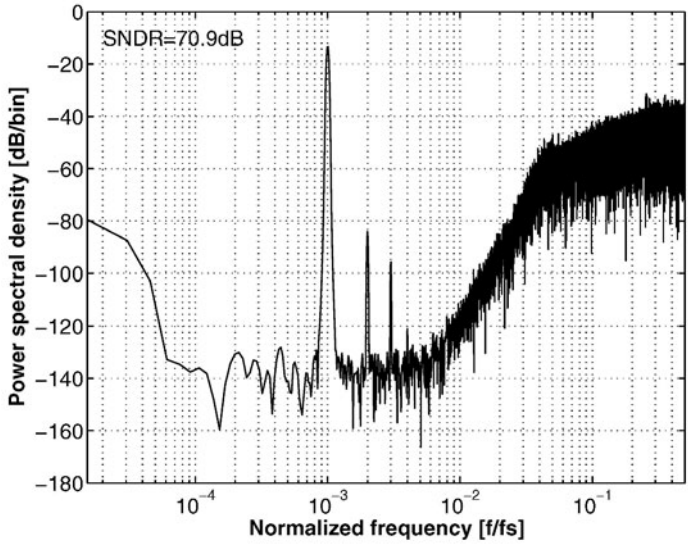



Figure 5.19: Simulated SNDR of the traditional fourth-order Σ-Δ modulator. The nonlinear OTA is modeled with $A_0 = 40\ dB, b_1 = -0.1\ and\ b_2 = -0.1$.

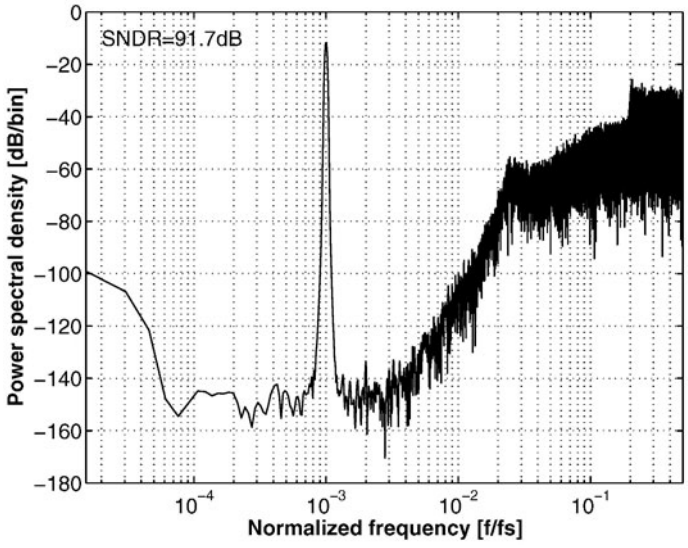



Figure 5.20: Simulated SNDR of the full feedforward fourth-order Σ-Δ modulator. The nonlinear OTA is modeled with $A_0 = 40\ dB, b_1 = -0.1\ and\ b_2 = -0.1$.

blocks will not affect the signal quality. Fig. 5.20 shows the output spectrum of a fourth-order single-loop full feedforward Σ-Δ modulator with a non-linear OTA modeled with coefficient $b_1 = -0.1$ $b_2 = -0.1$. Compared to Fig. 5.19, the same OTA non-linear gain coefficients are used, but in the full feedforward Σ-Δ modulator, the harmonic distortion is hardly visible.

Another feature associated with this topology is that the internal swing of the loop can be significantly reduced compared to traditional one. Shown in Fig. 5.22, outputs of four integrators of the full feedforward Σ-Δ modulator are all smaller than half of the reference voltage. By contrast, on the same operation condition, the outputs of four integrators of the traditional Σ-Δ modulator is shown in Fig. 5.21. It is clearly seen that the output swing of all integrators in the full feedforward Σ-Δ modulator is considerably reduced compared to the traditional Σ-Δ modulator. This simply eases the OTA design in a low-voltage environment. In a low-voltage environment, the output swing is limited by the supply voltage and the saturation voltage of the transistor. For the same output swing of the OTA, a higher reference voltage can be chosen, which eventually reduces the power consumption.

Fig. 5.23 and Fig. 5.24 show the gain requirement for the OTA used in the classic Σ-Δ modulator and full feedforward Σ-Δ modulator, respectively. It can be seen that for noise-shaping only, the OTA gain of 30 dB to 40 dB is enough for 95-dB SNR. While in a classic Σ-Δ modulator topology, much higher gain is requested to suppress the distortion caused by the non-linear OTA gain. Typically more than 60 dB gain is required [Mar99]. However, in the full feedforward Σ-Δ modulator topology, the OTA gain requirement is only determined by the noise-shaping performance, which is only 30 dB. With such relaxed requirements for the OTA, drastically scaling-down can be done to reduce the power consumption, making the proposed topology an ideal topology for low-voltage low-power Σ-Δ ADC.

Fig. 5.25 and Fig. 5.26 show the SNR of the modulator with the settling error of the integrator the traditional Σ-Δ modulator and full feedforward Σ-Δ modulator, respectively. As can be seen, the settling requirement of the full feedforward Σ-Δ modulator is similar to the traditional Σ-Δ modulator.

## 5.4 Circuit Implementation of the Full Feedforward Σ-Δ Modulator

Differently from the traditional Σ-Δ modulators, in the full feedforward Σ-Δ modulator topology, there is a summing point where all the feedforward branches signals are summed together. The summer of the full feedforward Σ-Δ modulator is implemented as a switched-capacitor network shown in Fig. 5.27. The transfer function of the summer is expressed as:

$$Y(z) = \frac{\sum_{i=1}^{n} X_i(z) \cdot C_{f_i}}{\sum_{i=1}^{n} C_{f_i}} \tag{5.25}$$

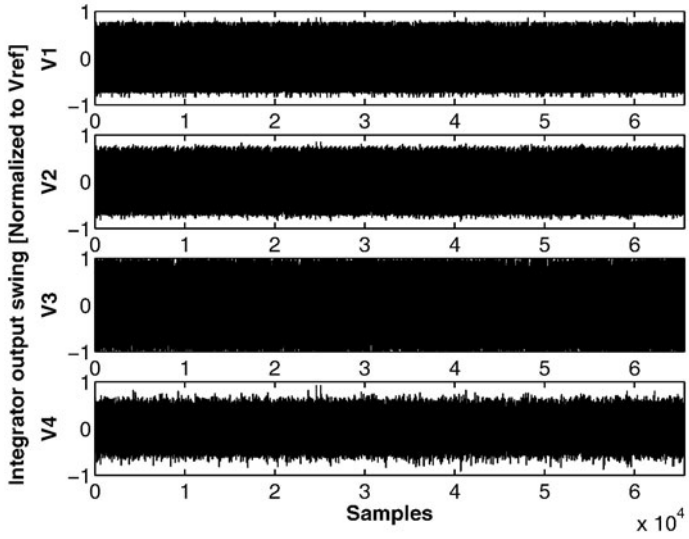



Figure 5.21: Simulated integrator output swings of a traditional fourth-order Σ-Δ modulator with a SNR=95 dB and OSR=64.

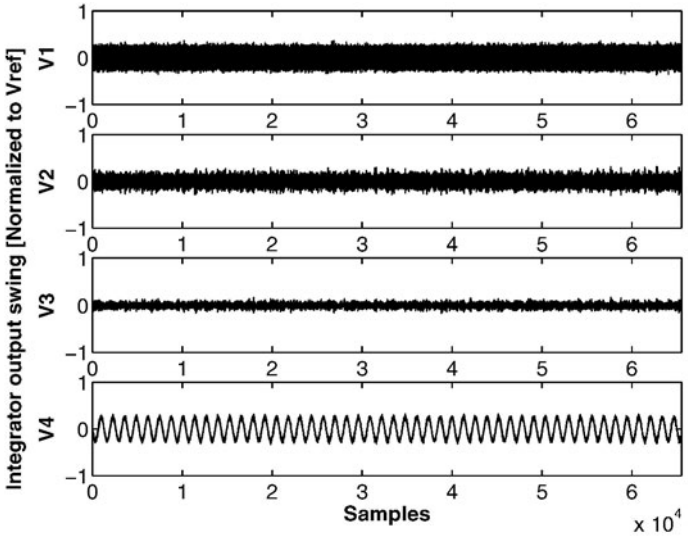



Figure 5.22: Simulated integrator output swings of a full feedforward fourth-order Σ-Δ modulator with a SNR=95 dB and OSR=64.

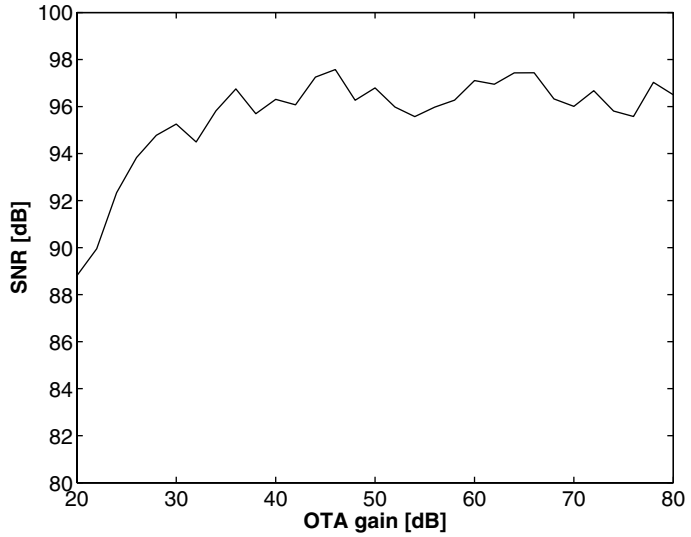



Figure 5.23: Traditional single-loop fourth-order Σ-Δ modulator SNR vs. OTA gain.

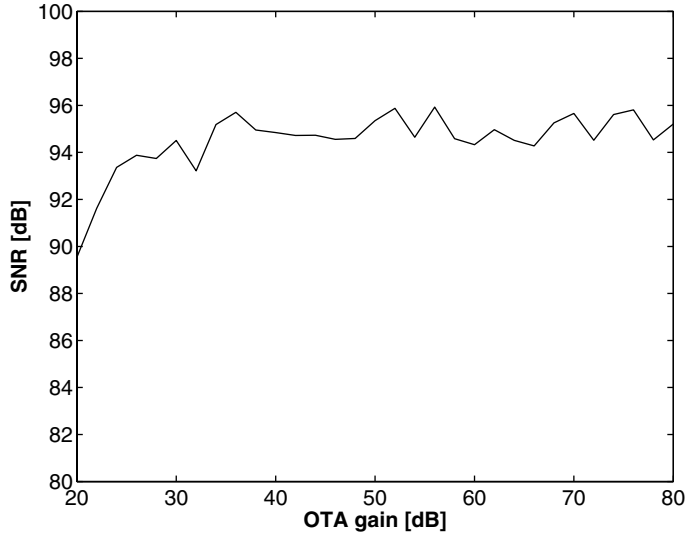



Figure 5.24: Full feedforward single-loop fourth-order Σ-Δ modulator SNR vs. OTA gain.

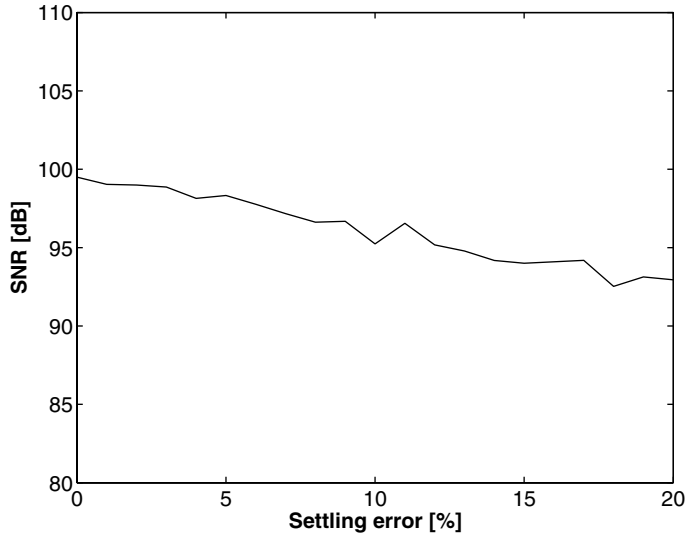



Figure 5.25: Traditional single-loop fourth-order Σ-Δ modulator SNR vs. settling error.

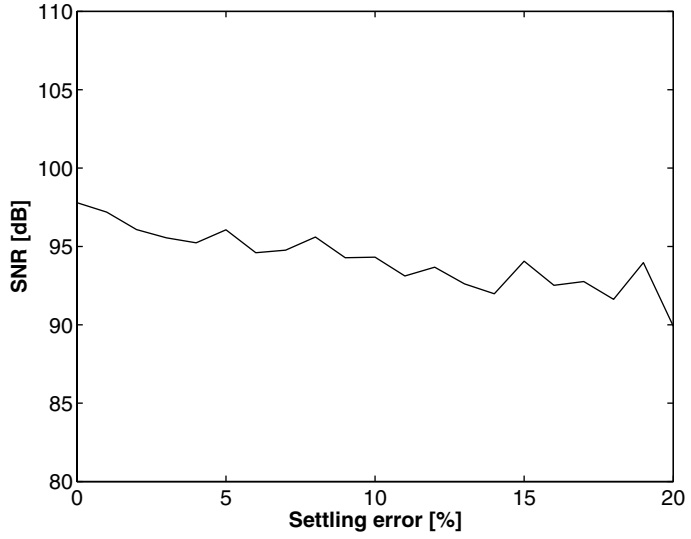



Figure 5.26: Full feedforward single-loop fourth-order Σ-Δ modulator SNR vs. settling error.

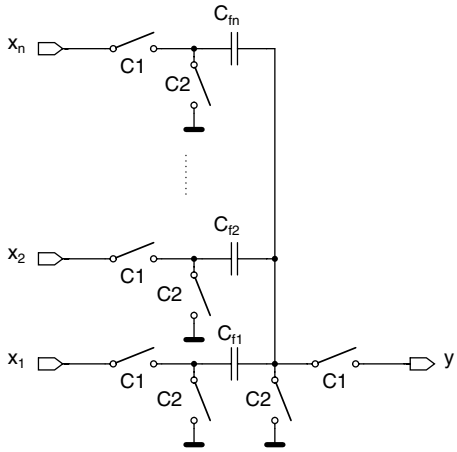



Figure 5.27: Circuit implementation of the switched-capacitor summer(single-ended).

where $C_{fi}$ is the capacitance of the i-th feedforward loop. Since the optimized loop coefficients, $c_i$, are all integers, it is possible to use unity-capacitances to realize the switched-capacitor network. By using the unity-capacitance in the feedforward branches, the transfer function is:

$$Y(z) = \frac{\sum_{i=1}^{n} X_i(z) \cdot c_i \cdot C_{unit}}{\sum_{i=1}^{n} c_i \cdot C_{unit}} = \frac{\sum_{i=1}^{n} X_i(z) \cdot c_i}{\sum_{i=1}^{n} c_i} \tag{5.26}$$

where $c_i$ is the feedforward loop coefficient of the full feedforward Σ-Δ modulator. To fulfill the requirement of the full feedforward Σ-Δ modulator, additional amplification of $\sum_{i=1}^{n} c_i$ is needed. Then the transfer function after the amplification is:

$$Y(z) = \sum_{i=1}^{n} X_i(z) \cdot c_i \tag{5.27}$$

This is the transfer function needed in the full feedforward Σ-Δ modulator to sum all the feedforward signals to the quantizer.

It is worth to mention that in a single-bit implementation, the amplitude information of the summer output is not utilized, while the sign of the output is the only important information for the single-bit quantizer. Therefore, the amplification factor of $\sum_{i=1}^{n} c_i$ in the single-bit Σ-Δ modulator can be omitted. The only impact is that the offset requirement for the single-bit quantizer is more stringent than that with the amplification factor. Since as described before, the single-loop Σ-Δ modulator is not sensitive to the

Table 5.6: Capacitor sizes of the full feedforward Σ-Δ modulator.

| Sampling capacitors | Integrating capacitors | feedforward capacitors |
|---|---|---|
| | | $C_{f0} = 0.4\ pF$ |
| $C_{s1} = 3.2\ pF$ | $C_{i1} = 16\ pF$ | $C_{f1} = 0.4\ pF$ |
| $C_{s2} = 0.8\ pF$ | $C_{i2} = 2.0\ pF$ | $C_{f2} = 0.4\ pF$ |
| $C_{s3} = 0.4\ pF$ | $C_{i3} = 4.0\ pF$ | $C_{f3} = 0.4\ pF$ |
| $C_{s4} = 0.4\ pF$ | $C_{i4} = 4.0\ pF$ | $C_{f4} = 0.8\ pF$ |

quantizer offset, there is no impact on the whole modulator performance by omitting the amplification after the summer in the single-bit implementation.

For high-resolution applications, switched-capacitor implementation is adopted for its high accuracy. The fully-differential implementation is also chosen in order to increase the signal swing and the CMRR. The circuit implementation of the fourth-order single-loop full feedforward Σ-Δ modulator is shown in Fig. 5.28.

The timing of the modulator is described below. The clock phase C1 is the sampling phase for integrators, and also the sampling phase for the quantizer. The clock phase C2 is the integration phase and feedback phase of the integrator. In order to provide the feedback signal in phase C2, the quantizer should make a decision before the phase C2. A delayed version of C1 is needed for the quantizer. In the single-bit implementation, the trigger signal of the quantizer is simply an inversion of the C1 clock, as shown in Fig. 5.28.

## 5.5 A 1.8-V 2-MS/s Σ-Δ Modulator in 180-nm CMOS

### 5.5.1 Implementation

A switched-capacitor circuit implementation of the proposed full feedforward Σ-Δ modulator topology is shown in Fig. 5.28. The feedforward signals are summed by a switched-capacitor network and then fed to the single-bit quantizer. The loop coefficient $c_4$ is two, which means that an amplification of two for the branch $c_4$ is needed. However, since a single bit quantizer is used, the only important thing is to detect the zero-crossing point of the input signal for the quantizer. The amplitude information is not used at all. So the amplification of two for the $c_4$ branch can be omitted while attenuating other branches by a factor of 0.5. That is the benefit of using the single-bit quantizer. The only thing of concern is that the offset requirement for the quantizer is two times smaller than that with amplification, as mentioned before. However, this requirement is easily fulfilled since the single loop topology is insensitive to the quantizer offset. All the capacitor sizes are summarized in Table. 5.6.

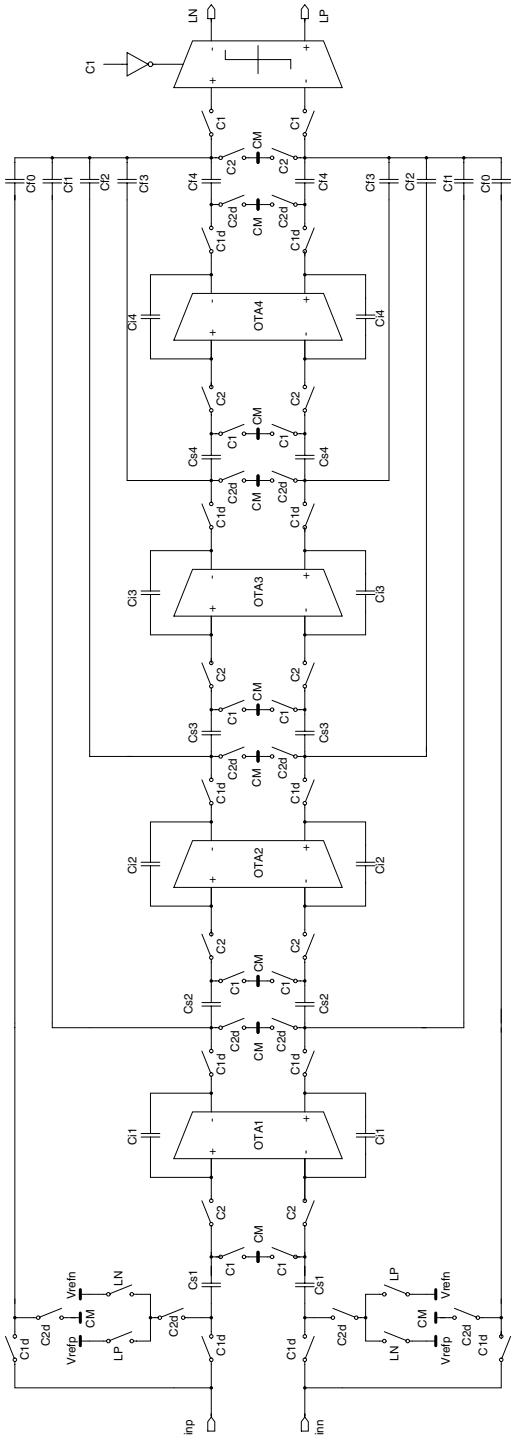



Figure 5.28: Schematics of the fourth-order single-bit full feedforward Σ-Δ modulator.

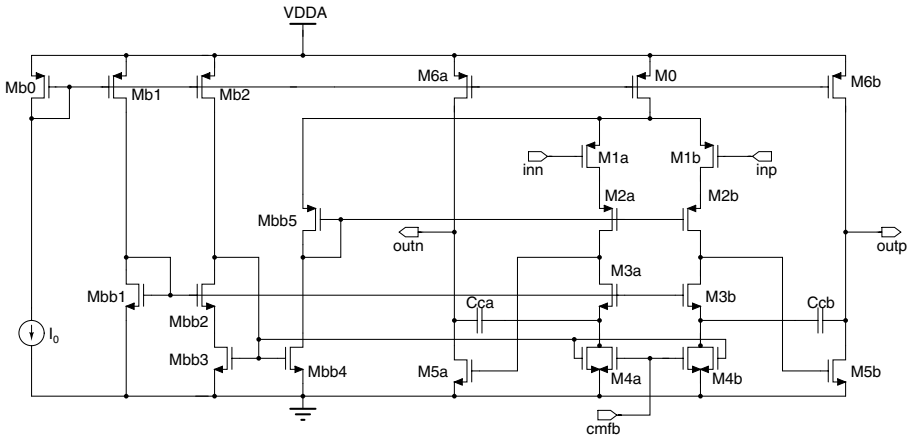



Figure 5.29: Schematic of the OTA used in the Σ-Δ modulator.

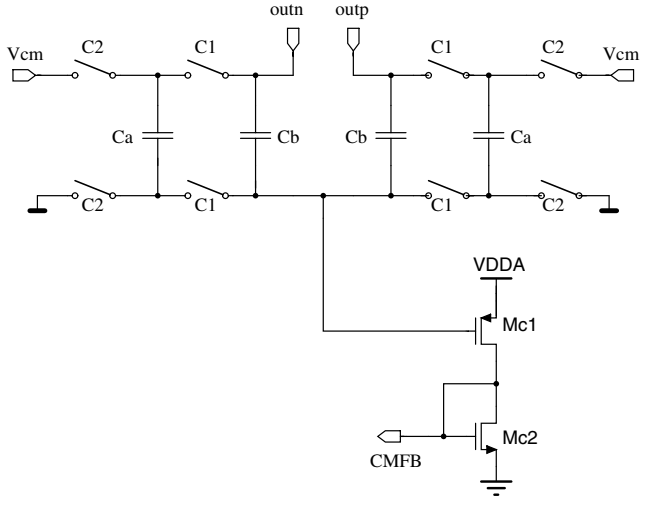



Figure 5.30: Switched-capacitor common-mode feedback circuit of the OTA.

#### 5.5.1.1 OTA Design

The most important building block in a Σ-Δ modulator is the OTA. Shown in Fig. 5.29, the OTA is implemented by a two-stage OTA with cascode compensation and optimized for best settling performance to increase the sampling frequency of the modulator, as described in section 4.2.4.2. The two-stage topology ensures that the DC gain of the OTA is sufficient for the noise shaping requirement, which normally is 30 dB for the proposed single loop topology according to the behavioral simulation. The rail-to-rail output swing of the two-stage OTA enables the full use of the supply voltage: the reference voltage can be set to 1.8 V to extend the dynamic range and reduce the power consumption on system level. By using an inverting stage, shown in Fig. 5.30, only one switched-capacitor common mode feedback circuit is used for each OTA in this design. The size of the transistors Mc1 and Mc2 are designed to ensure that the common-mode loop bandwidth is greater than the differential loop bandwidth. For low power consumption, the size of the sampling capacitors and the biasing of the OTA are scaled-down.

#### 5.5.1.2 Quantizer Design

Consisting of a dynamic comparator with a latch, shown in Fig. 5.31, the quantizer is able to work at a 1-GHz clock frequency and consumes dynamic power only. As the offset requirement for the comparator is quite relaxed, no pre-amplifier is used in front of the dynamic comparator. The output of the comparator is latched and buffered to provide the output data.

#### 5.5.1.3 Switches and Other Circuits

As illustrated in Fig. 5.32, all switches are implemented by transmission gates and driven by local drivers composed by inverters. As the conversion speed is over 100 MHz, the RC time constant formed by the switch on-resistance and the load capacitance should be taken into consideration. Transistors in the switches are properly sized to ensure a small on-resistance required by the RC constant. Non-overlapping two-phase clock signals are generated on chip from a master clock, as shown in Fig. 4.32. A delayed version of the clock is adopted to minimize the clock feed-through of the switches.

The proposed full feedforward Σ-Δ modulator was fabricated with a 1P6M 180-nm CMOS technology. All capacitances are implemented with MIM capacitance. No other features, except the MIM capacitance, are used in this design. The chip core size is 1.1 $mm \times 0.6\,mm$, as shown in Fig. 5.33. The analog part is separated from the digital part by guard rings to minimize the interference from the digital part. To reach the maximum common-mode rejection ratio, all the analog parts are laid out symmetrically. The surroundings of the unit capacitances are identical to ensure good matching.

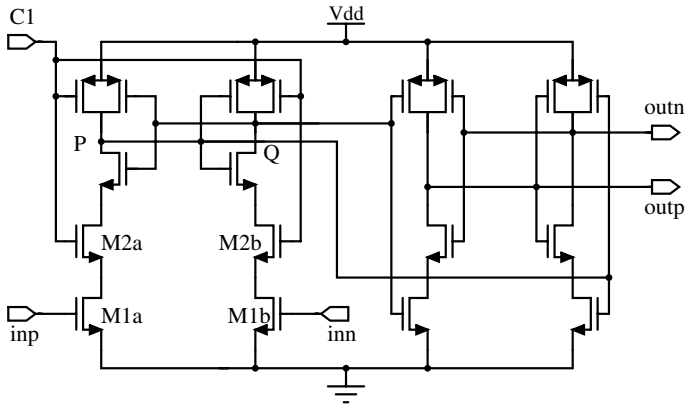



Figure 5.31: Dynamic comparator circuit of the Σ-Δ modulator.

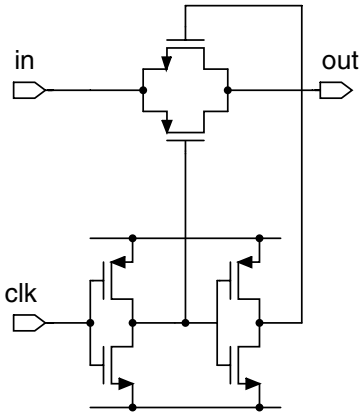



Figure 5.32: Switch implementation of the Σ-Δ modulator.

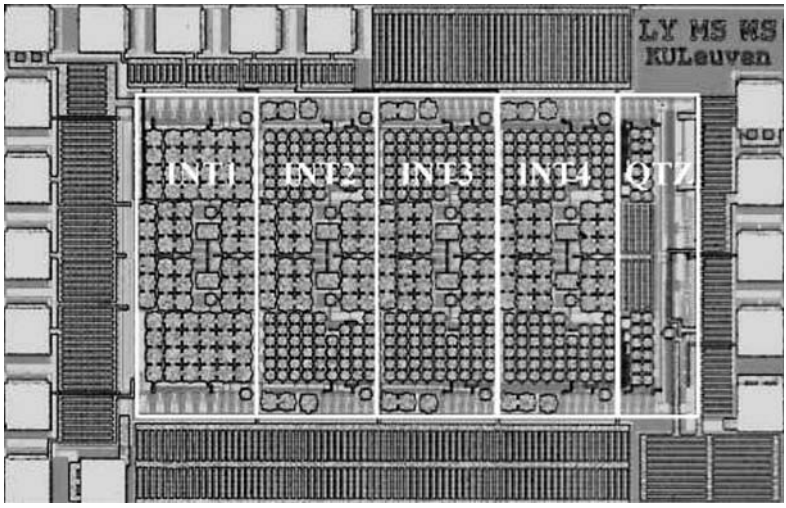



Figure 5.33: Chip micrograph of the full feedforward Σ-Δ modulator in a 180-nm CMOS.

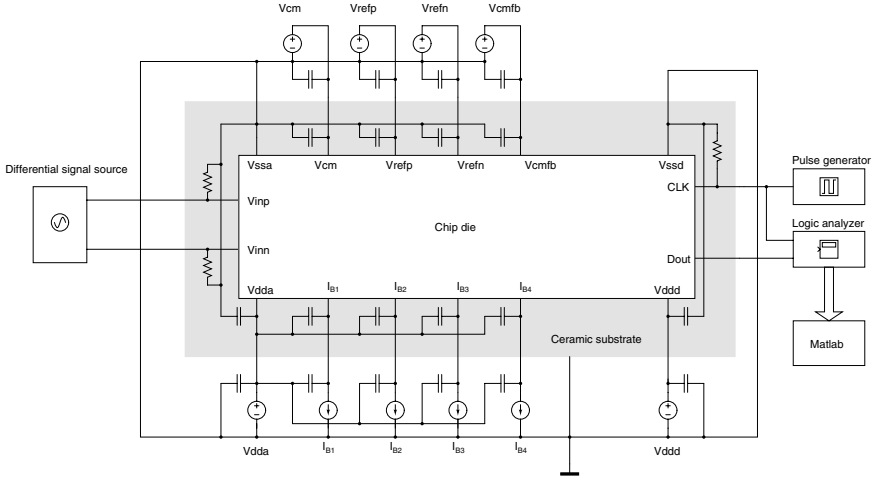



Figure 5.34: Schematic of the measurement setup.

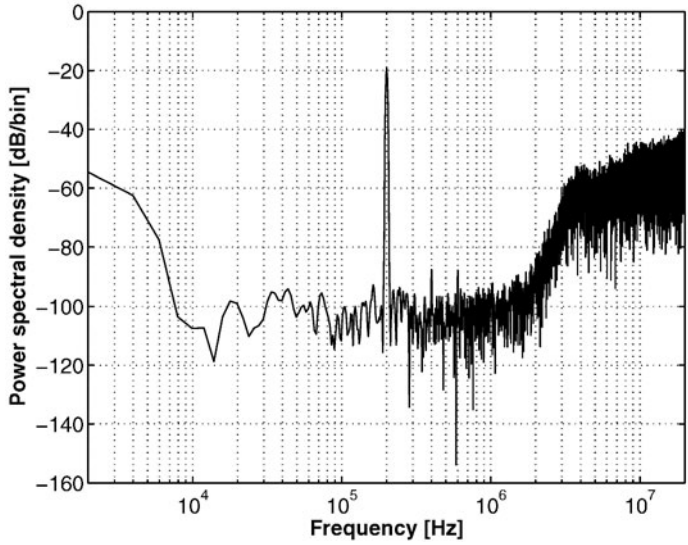



Figure 5.35: Measured output spectrum of a 200-kHz input signal.

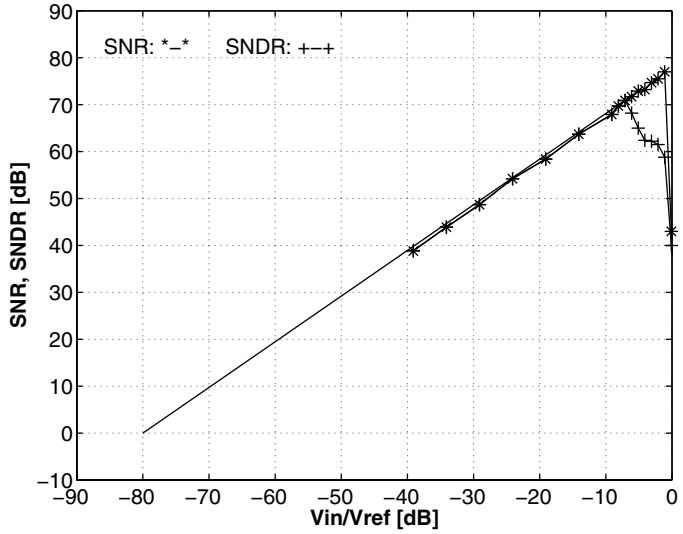



Figure 5.36: Measured dynamic range of the presented fourth-order full feed-forward Σ-Δ modulator.

### 5.5.2 Measurement results

Fig. 5.34 shows the schematic of the measurement setup. The Σ-Δ modulator chip was bonded on a ceramic substrate and then mounted in a metal box to shield from the outside interference. An ultra-low-distortion signal source was used to supply the differential input signal. The output data of the modulator is captured by a logic analyzer and processed by software. Clocked at 130 MHz, the modulator consumes 72 mW in the analog part and 15.2 mW in the digital part under 1.8-V power supply voltage. The oversampling ratio is 64. Fig. 5.35 shows the measured output spectrum of a 200-kHz sinusoid signal. A peak SNR of 77 dB has been reached in 1-MHz signal bandwidth. Fig. 5.36 shows the SNR and SNDR curves vs. the input signal amplitude. It can be seen that the modulator reaches a DR of 80 dB.

It is seen that a relatively high distortion is found from the output spectrum. According to the behavioral simulation results, the full feedforward topology is insensitive to the nonlinearity of the OTA. However, the distortion generated from the full feedforward path through the $C_{f0}$ branch shown in Fig. 5.28, directly shows in the modulator output. Since the signal swing in the full feedforward path is high, considerable distortion is generated by the switches in this path. A clock boosting circuit would certainly improve the SNDR of the modulator.

## 5.6 A 1-V 1-MS/s Σ-Δ Modulator in 130-nm CMOS

### 5.6.1 Implementation

To further explore the capability of the proposed full feedforward Σ-Δ modulator topology, a low-voltage low-power Σ-Δ modulator is implemented in a 130-nm pure digital CMOS technology. The proposed Σ-Δ modulator is implemented using fully-differential switched-capacitor circuits.

The modulator schematic is shown in Fig. 5.28. The feed forward paths are implemented by switched-capacitor networks. Due to the use of the single-bit quantizer, the amplitude information is not used at all. So the amplification of two for the $c_4$ branch can be omitted while attenuating other branches by a factor of 0.5. The output of the switched-capacitor summer is directly fed to the quantizer.

#### 5.6.1.1 OTA Design

The OTA is the main building block in a Σ-Δ modulator, as it determines most of the main performance and consumes most of the power of the modulator. Of all OTA topologies, the single-stage OTA is the most power-efficient because it does not need an additional compensation capacitance. The settling performance of the single-stage OTA is the simplest and easy to be optimized. The telescopic cascode OTA is a common single-stage OTA offering good gain and power efficiency. However, the reduced supply voltage restricts the use of the cascode OTA due to the small output swing. As mentioned before, the output swing of the integrators is successfully suppressed in the full feedforward topology, so it is possible to choose the single-stage telescopic cascode OTA in this design, shown in Fig. 5.37. The biasing circuit is optimized to ensure

that the transistor M1 and M4 are biased at the edge of the saturation region, which enables high output swings [Cho83], [Bab87]. A switched-capacitor common-mode feedback circuit is chosen in this design for its simplicity and power-efficiency.

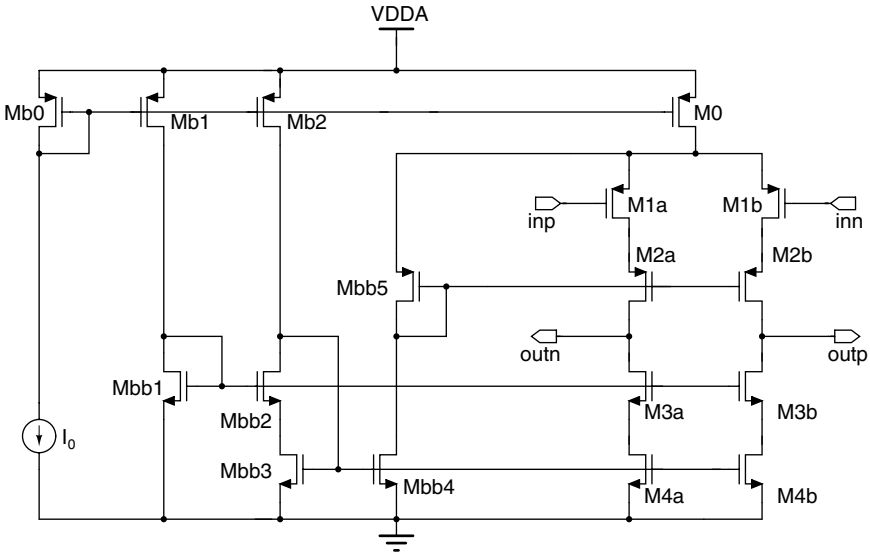



Figure 5.37: The telescopic cascode OTA used in this design.

### 5.6.1.2 Quantizer Design

The one-bit quantizer is realized with a dynamic comparator and a SR latch [Cho95], as shown in Fig. 5.31. The whole comparator is a purely dynamic circuit, which is very power efficient. The offset voltage is mainly defined by matching of the input transistors. For a single-bit Σ-Δ modulator, the offset and other requirement for the quantizer is quite relaxed.

### 5.6.1.3 Switches and Other Circuits

All switches are implemented with transmission gates, as shown in Fig. 5.32. Thanks to the relatively low threshold voltage of the transistor, there is no need to use any clock bootstrapping circuit to boost the driving voltage. Simple inverters are employed to drive switching transistors. The maximum driving voltage is the supply voltage. So no node inside the whole circuits is exposed to a voltage higher than Vdd or lower than Vss, which is essential for high-reliability operation of the circuit.

The clock signals are generated by a on-chip clock generator [Mar98], as shown in Fig. 4.32. The external clock input signal is buffered and then two non-overlapping clock signals are generated. To avoid signal dependent charge injection, two clocks with delayed falling edge, i.e. C1d and C2d are also generated to drive different switches [Hai83].

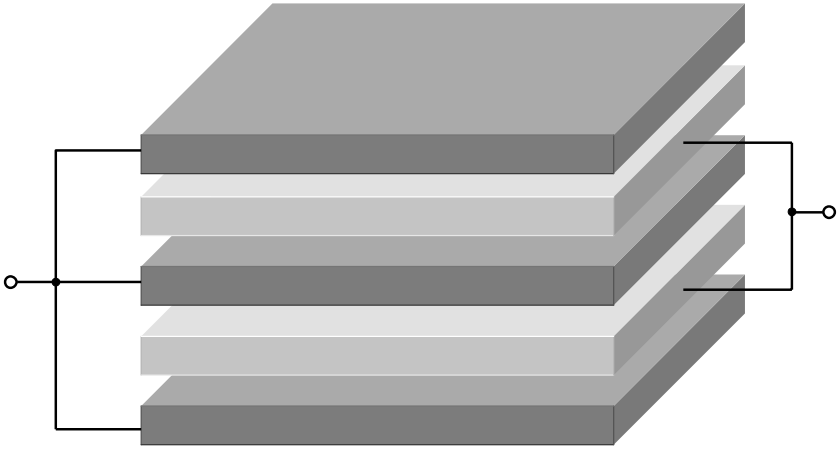


Figure 5.38: The metal layer Sandwich capacitance structure.

#### 5.6.1.4 Layout

The proposed full feedforward Σ-Δ modulator was fabricated with a 1P6M 130-nm pure digital CMOS technology. Only a standard digital process and no optional features are used in this design. All capacitances are implemented with metal Sandwich structures using 5 metal layers, as shown in Fig. 5.38. This capacitance implementation has a unit-capacitance of $0.35 fF/\mu m^2$, which is smaller than that of a standard MIM capacitance. The area occupied and parasitic capacitance associated with this Sandwich capacitance is larger than that of the MIM capacitance. All capacitances are implemented by unit capacitors of 400 fF, which ensure good matching from each other and provide accurate loop coefficients of the Σ-Δ modulator.

The chip core size is $0.94\ mm \times 0.64\ mm$, as illustrated in Fig. 5.39. The analog part is separated from the digital part by guard rings to minimize the interference from the digital part. To reach the maximum common-mode rejection ratio, all the analog parts are laid-out symmetrically. On-chip decoupling capacitances are widely used at the power supply and bias nodes.

### 5.6.2 Measurement Results

The modulator chip designed in a 130-nm CMOS technology is bonded on a ceramic substrate and then mounted in a metal box to shield the outside interference, as shown in Fig 5.40. The schematic of the measurement setup is the same as the one used in the last section, as depicted in Fig. 5.34. An ultra-low-distortion signal source is used to supply the differential input signal. The output data of the modulator is captured by a

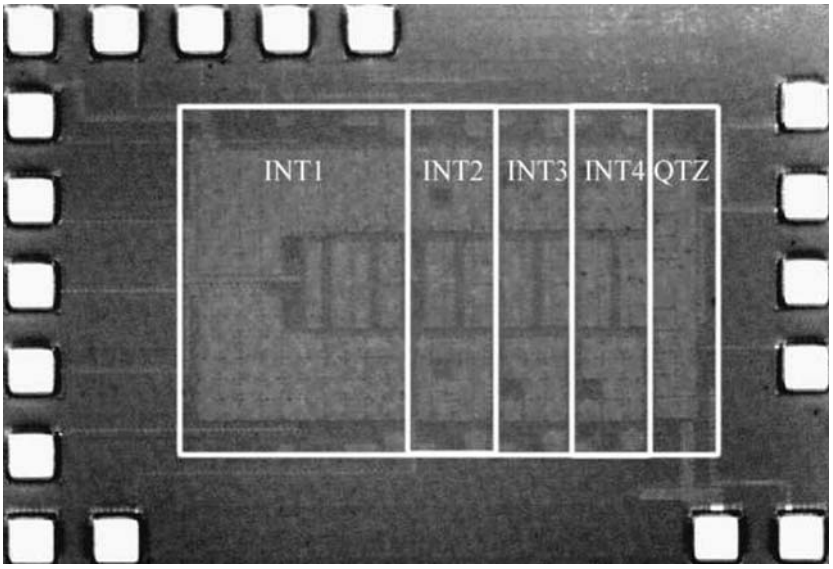



Figure 5.39: Chip micrograph of the full feedforward Σ-Δ modulator in a 130-nm CMOS.

logic analyzer and processed by software. Clocked at 64 MHz, the modulator consumes 6.1 mW in the analog part and 1.3 mW in the digital part including the output buffer, under a 1.0-V power supply voltage. The reference voltage is 0.8 V. The oversampling ratio is 64, resulting a 1 MS/s conversion speed. Fig. 5.41 shows the measured output spectrum of a 100-kHz sinusoid signal. A peak SNR of 86 dB and a peak SNDR of 75 dB have been reached in a 500-kHz signal bandwidth. Fig. 5.42 shows the SNR and SNDR vs. the input amplitude. It can be seen that the modulator reaches a DR of 88 dB. It is worth to mention that when the reference voltage is increased to 1 V, the same as the supply voltage, the modulator reaches a DR of 90 dB and SNDR of 73 dB with a higher power consumption. Experiencing a high signal swing, the switches in the full feedforward path generate a considerable amount of distortion and degrade the SNDR of the modulator. The distortion performance is not as good as expected. The reason is that the distortion generated by the full feedforward paths is directly shown in the modulator output. The signal dependent on-resistance of the switch in the full feedforward path is the main source of the distortion. The signal swing in the full feedforward path is quite high, making this problem severe. Table 5.7 gives a summary of the performance.

Table 5.8 shows the performance comparison of recently published low-power low-voltage Σ-Δ modulators whose supply voltage is less than 1.5 V. As can be seen in Table 5.8, this design largely extends the signal bandwidth of low-voltage Σ-Δ modulators and still achieves rather high FOM. Due to the use of the full feedforward topo-

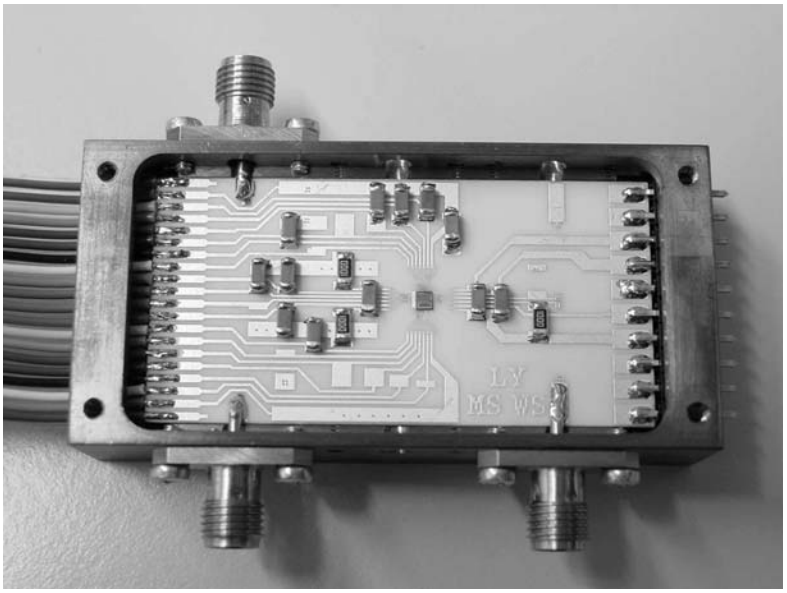


Figure 5.40: Photograph of the Σ-Δ modulator die mounted on the ceramic substrate and sealed inside the copper-beryllium box.

Table 5.7: Measured performance summary.

| | | |
|---|---|---|
| Sampling frequency | 64 | MHz |
| Signal bandwidth | 500 | kHz |
| Over sampling ratio | 64 | |
| Supply voltage | 1.0 | V |
| Analog power consumption | 6.1 | mW |
| Digital power consumption | 1.3 | mW |
| Peak SNR | 86 | dB |
| Peak SNDR | 75 | dB |
| DR | 88 | dB |
| Reference voltage | 0.8 | V |
| Active die area | 0.6 | $mm^2$ |

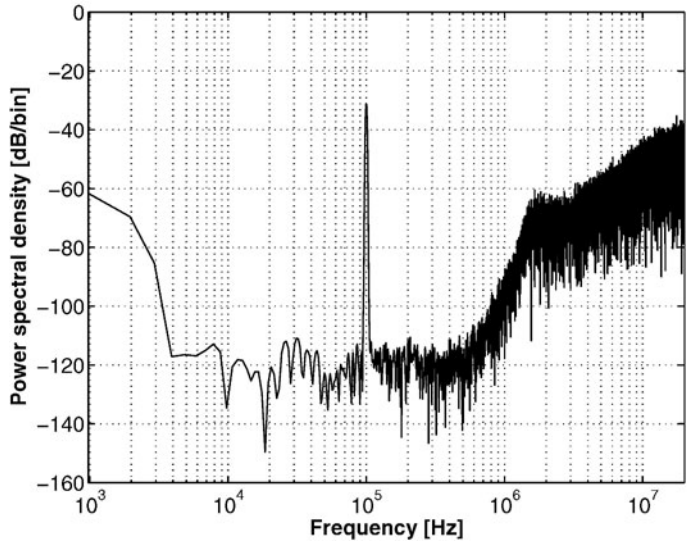



Figure 5.41: Measured output spectrum of a −30-dBFS, 100-kHz sinusoidal input signal.

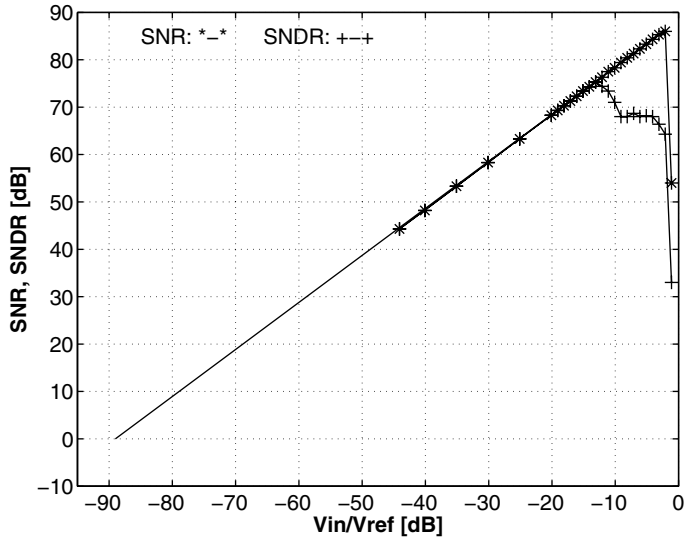



Figure 5.42: Measured SNR and SNDR vs. input amplitude.

logy, the high-speed telescopic cascode OTA can be used in low-voltage environment. This greatly increases the operation speed and maintains the high performance of the modulator.

Table 5.8: Performance comparison.

| Names Year | Supply Voltage [V] | DR [dB] | Signal BW [kHz] | Power [$\mu$W] | FOM |
|---|---|---|---|---|---|
| Peluso,1998 [Pel98] | 0.9 | 77 | 16 | 40 | 330e-6 |
| Keskin,2002 [Kes02] | 1.0 | 80 | 20 | 5600 | 5.9e-6 |
| Yao,2004 [Yao04] | 1.0 | 88 | 20 | 140 | 1493e-6 |
| Dessouky,2001 [Des01] | 1.0 | 88 | 25 | 950 | 275e-6 |
| Gaggl, 2004 [Gag04] | 1.5 | 88 | 300 | 8000 | 392e-6 |
| Das, 2005 [Das05] | 1.3 | 86 | 600 | 5400 | 732e-6 |
| This work | 1.0 | 88 | 500 | 7400 | 706e-6 |

## 5.7 Multibit Full Feedforward Σ-ΔModulator Design

The speed requirement for a high-resolution Σ-ΔADC promotes the development of the multibit Σ-ΔADC. The use of a multibit quantizer in the Σ-Δ modulator greatly reduces the quantization noise and improves the stability of the Σ-Δ modulator loop.

In this section, the performance of the multibit full feedforward Σ-Δ modulator topology is analyzed. A four-bit fourth-order Σ-Δ modulator topology and optimized loop coefficients are presented.

As described before, the distortion generated in the full feedforward Σ-Δ modulator topology is significantly reduced compared to the traditional Σ-Δ modulator topology. This feature is also inherited by the multibit full feedforward Σ-Δ modulator.

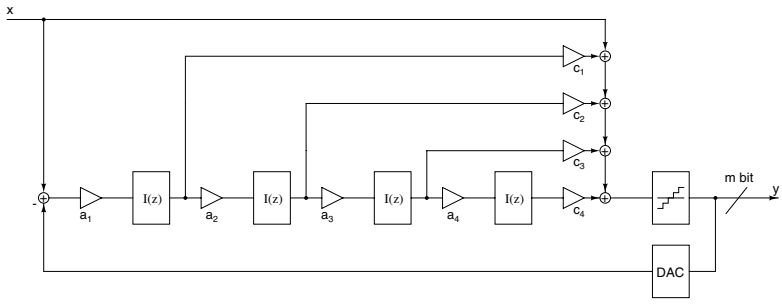



Figure 5.43: The four-bit fourth-order full feedforward Σ-Δ modulator topology.

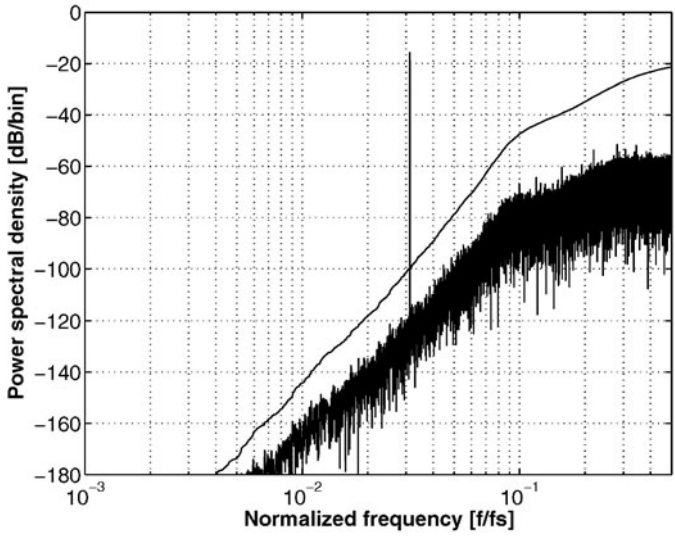



Figure 5.44: Simulated output spectrum of the proposed four-bit fourth-order full feedforward Σ-Δ modulator topology.

Table 5.9: Optimized loop coefficients of the proposed topology.

| | | | |
|---|---|---|---|
| $a_1$=0.6 | $a_2$=1 | $a_3$=0.9 | $a_4$=0.6 |
| $c_1$=4 | $c_2$=4 | $c_3$=2 | $c_4$=1 |

Another feature associated with this topology is that the internal swing of the loop can be significantly reduced without compromising the noise shaping performance, compared to the traditional Σ-Δ modulator. Shown in Fig. 5.45, all four integrators' output swings of the full feedforward Σ-Δ modulator are smaller than 20% of the reference voltage. This simply eases the OTA design in a low-voltage environment further more. Also for a certain output swing of the OTA, a higher reference voltage can be chosen, which can reduce the power consumption of the Σ-Δ ADC at the system level.

### 5.7.1 Optimized Loop Coefficients

The proposed four-bit fourth-order full feedforward Σ-Δ modulator topology is shown in Fig. 5.43. Fig. 5.44 shows the simulated output spectrum. The loop coefficients are shown in Table. 5.9. These coefficients are optimized for best noise-shaping performance with small internal swings, as can be seen in Fig. 5.45. With an oversampling ratio of 16, the proposed Σ-Δ modulator topology achieves a dynamic range of 90 dB.

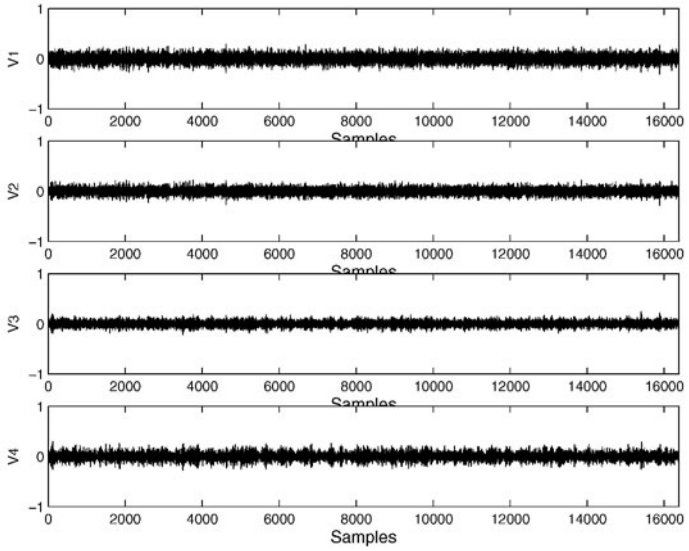



Figure 5.45: Simulated output swing (normalized to reference voltage) of each integrator of the proposed topology.

To conclude, the proposed topology greatly relaxes the requirement to the OTAs in terms of DC gain , linearity and output swing. In practice a simple, fast and robust single-stage OTA topology can be used in the proposed full feedforward $\Sigma$-$\Delta$ topology without compromise for the converter performance. With such relaxed requirements for the OTA in the full feedforward $\Sigma$-$\Delta$ modulator topology, much freedom is available in designing the OTA, making the proposed full feedforward topology a good topology for wide-band $\Sigma$-$\Delta$ ADCs in nanometer CMOS technologies.

## 5.7.2 Circuit Implementation

The full circuit implementation of the multibit full feedforward $\Sigma$-$\Delta$ modulator is shown in Fig. 5.46. The differences between the single-bit implementation and the multibit one are the multibit quantizer and the feedback DAC. A 4-bit quantizer and a 4-bit capacitive DAC are used in the proposed $\Sigma$-$\Delta$ modulator.

### 5.7.2.1 Switched-Capacitor Summer Implementation

As mentioned before, the switched-capacitor summer is used in the implementation of the full feedforward $\Sigma$-$\Delta$ modulators. In the multibit implementations, the amplitude is important, so after the passive switched-capacitor network, an amplification of $\sum_{i=1}^{n} c_i$ is needed to realize the wanted feedforward coefficients. As shown in Fig. 5.46, preceding the multibit quantizer, an amplifier is used. The requirement to the amplifier is the fixed gain and wide bandwidth. Moreover, in nanometer CMOS tech-

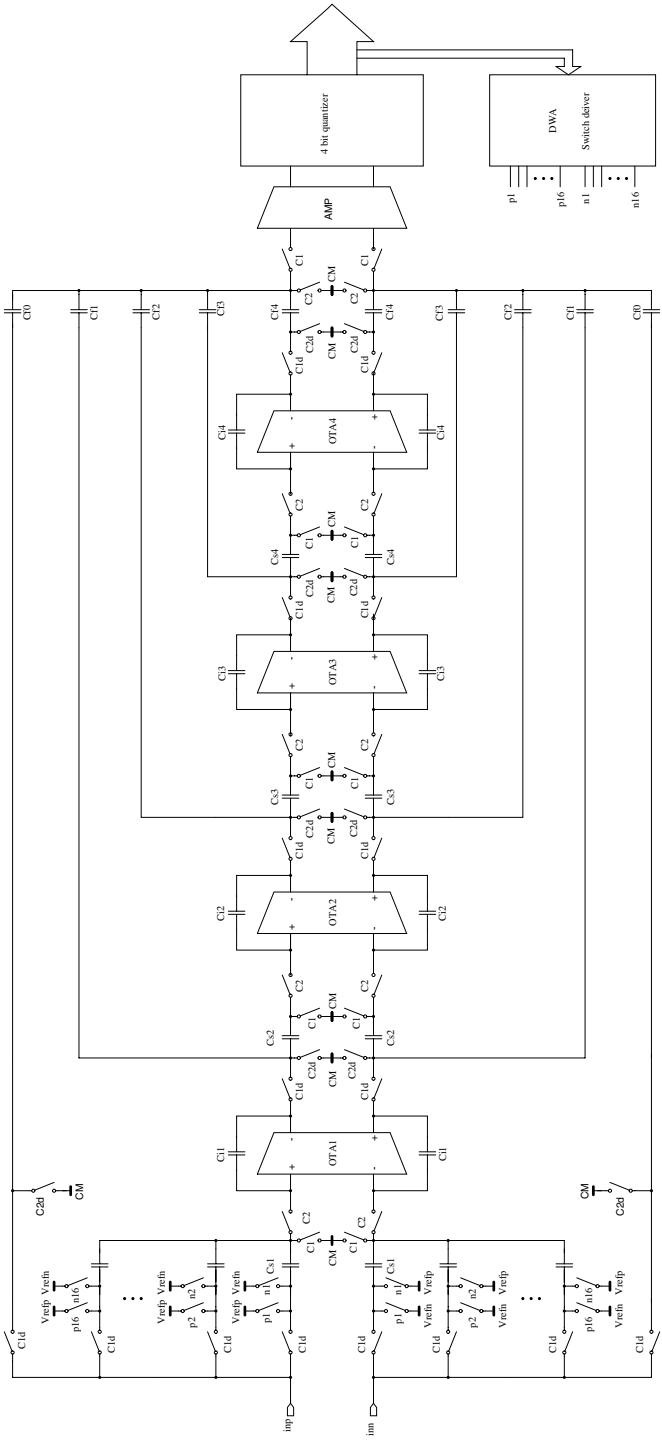



Figure 5.46: Schematic of the four-bit fourth-order full feedforward Σ-Δ modulator.

nologies, the output swing is also addressed since the signal swing here is big. At this summing point, the full input signal swing is directly coupled to this point, as can be seen from the transfer function. The gain is not required to be precise according to [Bal04]. A simple wide-band amplifier, shown in Fig. 5.47 is chosen in this case for its speed performance.

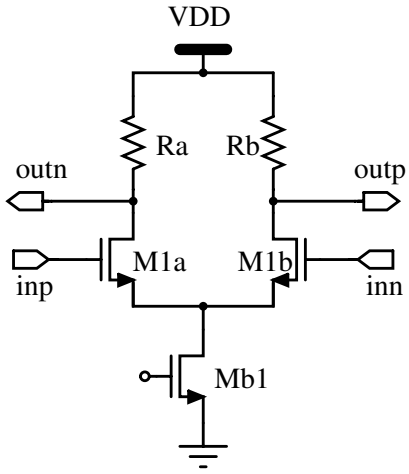



Figure 5.47: Wideband amplifier to realize the feedforward coefficients in the multibit full feedforward Σ-Δ modulators.

#### 5.7.2.2 Multibit Quantizer Implementation

The multibit quantizer in fact is a Flash ADC. The output codes of the multibit quantizer are thermometer codes to drive the unit-element feedback DAC. Binary codes are also needed to provide the output data and to perform the DWA algorithm.

In nanometer CMOS technologies, the supply voltage is reduced. At the same time, the signal range is maximized to gain better performance. These result into large signal swings inside the Σ-Δ modulator loop. In the full feedforward Σ-Δ modulator, the signal swings inside the loop are greatly suppressed. However, in the summing node, i.e. the input of the quantizer, the signal swing is high, since the full range input signal is directly coupled to this node. Consequently, a rail-to-rail input range for the multibit quantizer is required. In a low-voltage environment, this requirement results into complex circuits.

The basic building block in the multibit quantizer is the fully-differential comparator. The rail-to-rail input range of the fully-differential comparator is implemented by a switched-capacitor level shifter network shown in Fig. 5.48. The operation principle is as follows. At the clock phase C2, the reference voltage is sampled on the sampling capacitor; at the clock phase C1, the pre-charged sampling capacitor is connected to the input signal. The comparator output is decided on the polarity of the expression:

$(V_{inp} - V_{refp}) - (V_{inn} - V_{refn})$.

By using a switched-capacitor level shifter, the rail-to-rail input range requirement for the preamplifier is exempted and simplifies the overall circuit.

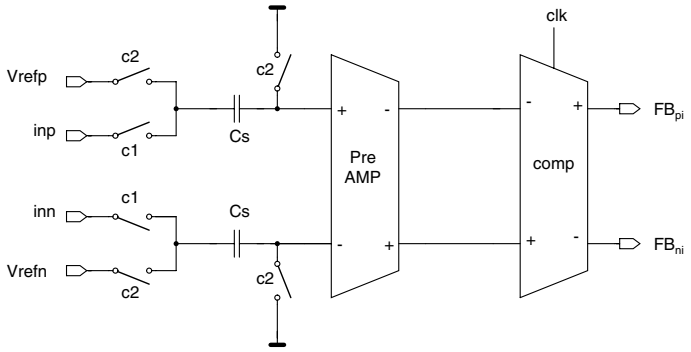



Figure 5.48: Circuit implementation of the full input swing comparator.

By a slight change of the connection of the switches in Fig. 5.48, additional offset-cancellation can be obtained. At the clock phase C2, the offsets and the reference voltages are sampled. At the clock phase C1, the input signal is connected to the input through the pre-charged sampling capacitors. The input of the pre-amplifier sees the difference of the input signal and the reference voltage. The offset voltage is automatically cancelled.

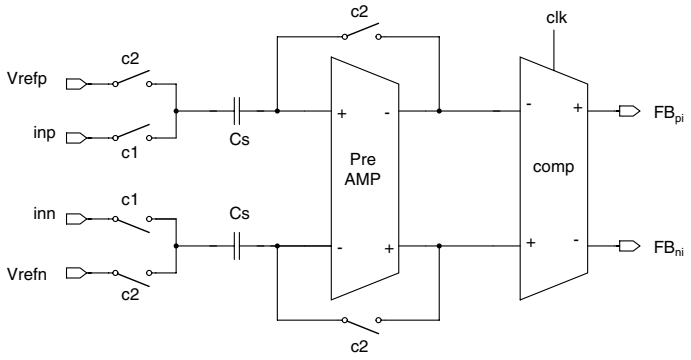



Figure 5.49: Circuit implementation of the full input swing comparator with offset cancellation.

#### 5.7.2.3 Feedback DAC Implementation

The feedback DAC is implemented with a capacitive DAC, shown in Fig. 5.50 [Gee00]. Since only one feedback branch is needed in the full feedforward topology, the DAC circuit is simplified.

#### 5.7.2.4 DWA Implementation

The nonlinearity problem of the feedback DAC can be solved by using dynamic element matching (DEM) techniques. Of all DEM techniques, the data weighted averaging (DWA) algorithm, introduced in [Bai95], [Gee01], is an effective and simple technique to realize the DEM. Using this algorithm, distortion spectra from DAC linearity errors are shaped by first-order noise shaping, resulting in a dynamic range improvement of 9 dB/octave when DAC errors dominate. The principle of the DWA algorithm is shown in Fig. 5.51. The register points to the next unused element and rotates according to the input codes. This operation ensures that all the elements are used an equal number of times in a certain period. Consequently, the errors introduced by the mismatch of the elements are averaged to zero quickly.

The DWA algorithm is implemented with an accumulator and a logarithmic shifter, as depicted in Fig. 5.52. The output data from the quantizer are thermometer codes, and then they are converted to binary codes by a ROM encoder, shown in Fig. 5.53. The binary output codes are fed to the accumulator to perform the rotation of the pointer. The accumulator functions as a pointer in the DWA algorithm. The shifter rotates the selected element according to the input codes. The whole implementation is aimed to minimize the delay in the feedback path of the $\Sigma$-$\Delta$ modulator.

The accumulator is composed by four adders and four registers, shown in Fig. 5.54. The output signal of the adder is coupled to the input again to perform the accumulation. To minimize the delay introduced by the adder, a high-performance CMOS 1-bit full-adder cell is chosen [Sha00]. The novel 16-transistor CMOS 1-bit full-adder cell uses low-power designs for the XOR and XNOR gates, pass transistors, and transmission gates. The cell offers higher speed and lower power consumption than standard implementations of the 1-bit full-adder cell. The latch used is a dynamic latch shown in Fig. 5.55.

## 5.8 Conclusion

In this chapter, a system level approach of $\Sigma$-$\Delta$ ADC design in nanometer CMOS is discussed. At the system level, by introducing the full feedforward branch to the $\Sigma$-$\Delta$ modulator, some unique features are achieved. A systematic study on the single-loop, cascaded and multibit full feedforward $\Sigma$-$\Delta$ modulator topologies is presented. Aiming at the implementation in nanometer CMOS technologies, the optimization of the full feedforward $\Sigma$-$\Delta$ modulator is done and optimized parameters are given.

Main features of the full feedforward $\Sigma$-$\Delta$ modulator topology are the unity signal transfer function and low internal swings. These features make this topology an ideal topology for low-voltage low-power $\Sigma$-$\Delta$ modulator. The distortion performance of the

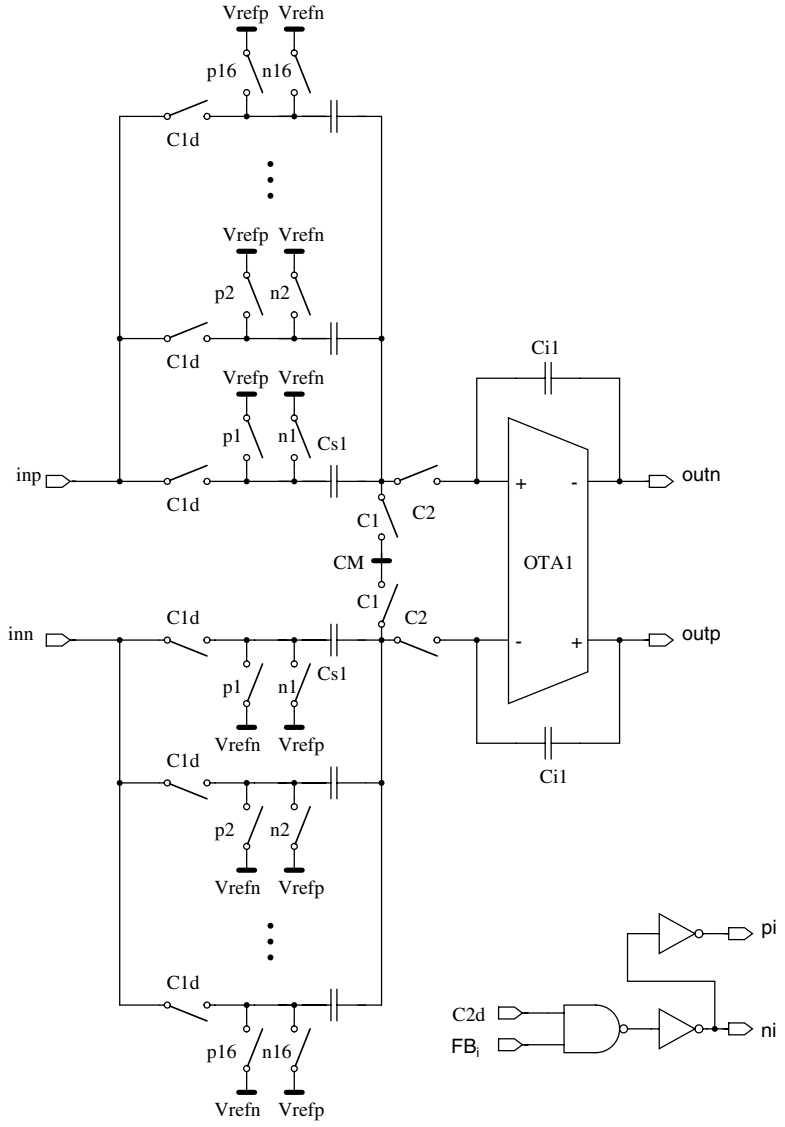



Figure 5.50: Circuit implementation of the feedback DAC for the four-bit full feedforward Σ-Δ modulator.

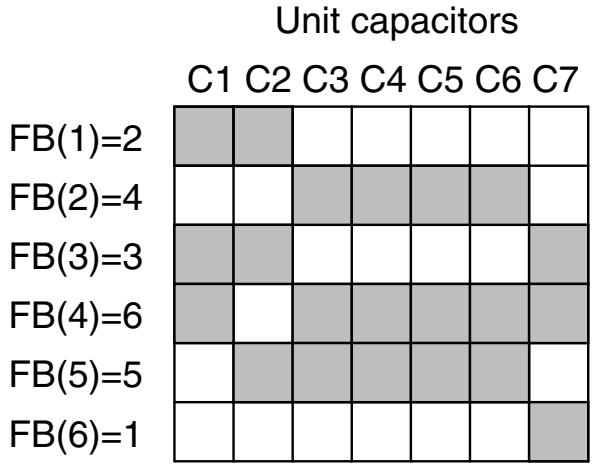



Figure 5.51: Operation principle of the DWA algorithm. The shaded boxes indicate the selected unit elements for a three-bit DAC with input codes of: 2 4 3 6 5 1.

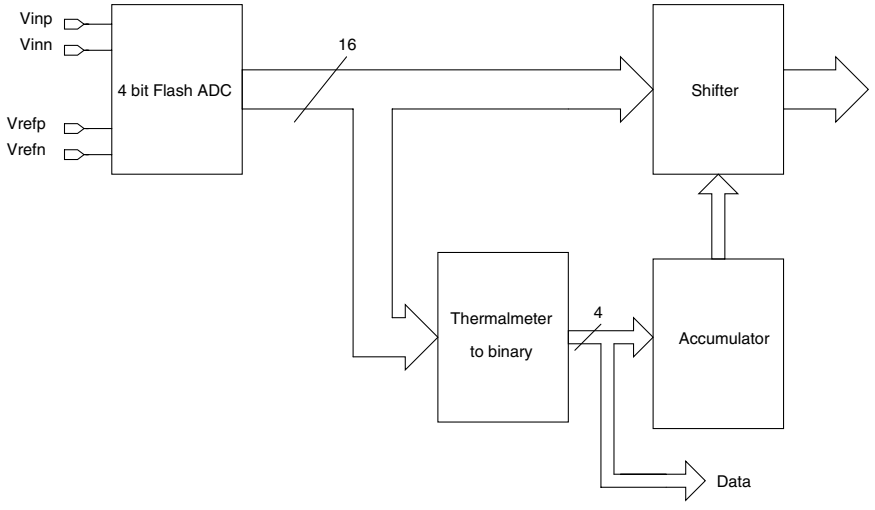



Figure 5.52: Block diagram of the DWA implementation.

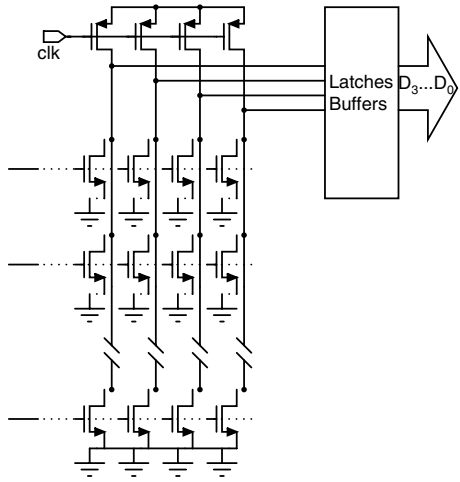



Figure 5.53: Circuit implementation of the thermometer to binary code encoder.

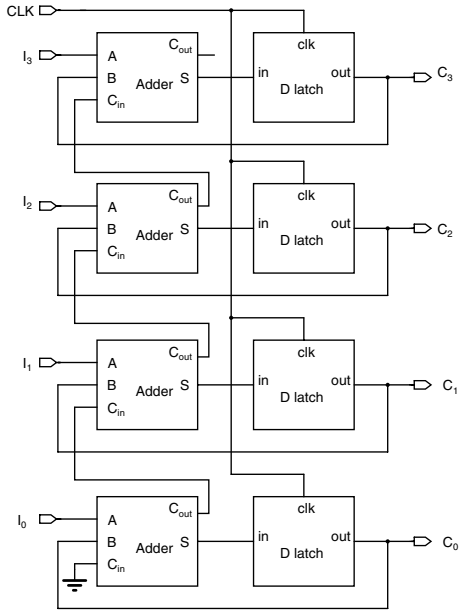



Figure 5.54: Circuit implementation of the accumulator.

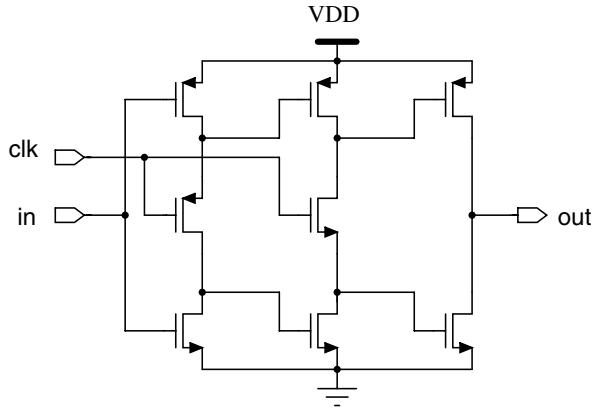



Figure 5.55: Circuit implementation of the rising edge triggered D latch.

full feedforward Σ-Δ modulator topology is analyzed. Impact of the building block nonidealities to the full feedforward Σ-Δ modulator performance is also analyzed. From the behavioral simulation results presented in this chapter, it is seen that the full feedforward Σ-Δ modulator has better linearity compared to the traditional Σ-Δ modulator. The full feedforward Σ-Δ modulator is insensitive to the gain nonlinearities of the OTA. Since the loop only processes the quantization noise, the internal swing of the full feedforward topology is greatly reduced. This swing reduction not only relaxes the output swing requirement to the OTA, but also helps to reduce the distortion generated in the OTA. The single-loop full feedforward Σ-Δ modulator is insensitive to the DC gain and the settling error.

The circuit implementation of the proposed full feedforward Σ-Δ modulator topology is introduced. The feedforward branches are implemented with a switched-capacitor network. The use of the single-bit quantizer exempts the feedforward branches from amplification.

Two test chips are designed using the proposed full feedforward Σ-Δ modulator topology. The first chip was implemented with a 180-nm CMOS technology. Clocked at 130 MHz, the modulator consumes 72 mW in the analog part and 15.2 mW in the digital part from a 1.8-V power supply voltage. A peak SNR of 77 dB and a DR of 80 dB have been reached in a 1-MHz signal bandwidth. The second chip was implemented with a 130-nm CMOS technology. Clocked at 64 MHz, the modulator consumes 7.4 mW from a 1.0-V power supply voltage. The modulator reaches a 1-MS/s conversion speed and a peak SNR of 86 dB and a DR of 88 dB. The second test chip marks a new conversion speed in 1-V Σ-Δ converters. The FOM of the modulator is good as well. These measurement results demonstrate that the proposed full feedforward Σ-Δ modulator topology is an ideal topology for low-voltage low-power Σ-Δ modulator designs and wideband Σ-Δ modulator designs in nanometer CMOS technologies.

In the final part of this chapter, a multibit full feedforward $\Sigma$-$\Delta$ modulator topology is proposed. Circuit level implementation and the DWA implementation are also introduced. By reducing the oversampling to 16, the proposed multibit full feedforward $\Sigma$-$\Delta$ modulator topology is a good candidate for wideband $\Sigma$-$\Delta$ modulator design in nanometer CMOS technologies.

# Chapter 6

# Conclusions

Recent research work on the low-power low-voltage Σ-Δ ADC design in nanometer CMOS technologies has been presented in this book. In a low-power low-voltage Σ-Δ ADC design in nanometer CMOS technologies, both approaches at the circuit level and at the system level are presented. Several presented designs have demonstrated that it is possible to implement high performance ADCs in nanometer CMOS technologies.

In Chapter 2 the scaling-down of the CMOS technology is introduced. Then the impact of the CMOS scaling-down to analog circuits is described. For the analog circuit, the CMOS scaling-down brings us not only faster transistors, but also many design challenges. The impact of the CMOS scaling-down to the ADC design is then analyzed in its different aspects.

In Chapter 3, the basic principle of the ADC is introduced. By introducing oversampling and noise-shaping, the basic operation principle of the Σ-Δ ADC is presented. Then the performance metrics of the Σ-Δ ADC is explained. A systematic study on the traditional single-loop, cascaded and multibit Σ-Δ modulator topologies is given in this chapter. Optimized parameters are also given for each topology.

In Chapter 4, the circuit level approach of the low-power low-voltage Σ-Δ ADC design in nanometer CMOS technologies is presented. A third-order single-loop Σ-Δ modulator in a 90-nm pure digital CMOS technology has been presented. Special measures are taken in the circuit design to reduce the power consumption. The peak SNR of the modulator reaches 85 dB and the dynamic range is 88 dB in a 20 kHz signal bandwidth. The total power consumption is only 140 $\mu$W under a 1-V power supply. This design is the first Σ-Δ modulator design in a 90-nm CMOS technology and reaches a very high figure-of-merit. These measurement results have proven the possibility of implementing high-performance low-power low-voltage Σ-Δ ADCs in nanometer standard digital CMOS technologies.

In Chapter 5, the system level approach of the low-power low-voltage Σ-Δ ADC design in nanometer CMOS is presented. At system level, by introducing the full feedforward branch to the traditional Σ-Δ modulator, several unique features are acquired. After the introduction of the full feedforward Σ-Δ modulator topology, a systematic study on the single-loop, cascaded and multibit full feedforward Σ-Δ modulator topologies is presented. Aiming at the implementation in nanometer CMOS technologies, the full feedforward Σ-Δ modulator is optimized. Advantages and disadvantages of each topology are analyzed. Two test chips are designed using the proposed

full feedforward Σ-Δ modulator topology. The first chip was implemented in a 180-nm CMOS technology. Clocked at 130 MHz, the modulator consumes 72 mW in the analog part and 15.2 mW in the digital part under a 1.8-V power supply voltage. A peak SNR of 77 dB and a DR of 80 dB have been reached in a 1-MHz signal bandwidth. The second chip was implemented with a 130-nm pure digital CMOS technology. The modulator consumes 7.4 mW under a 1.0-V power supply voltage. The modulator reaches a 1 MS/s conversion speed, a peak SNR of 86 dB and a DR of 88 dB. These designs are the first design using the full feedforward Σ-Δ topology. The second design reaches the highest conversion speed among the 1-V Σ-Δ modulator designs to date. These measurement results have proven that the proposed full feedforward Σ-Δ topology is an excellent topology for the high-performance low-power low-voltage Σ-Δ ADC design. In the final part of this chapter, a multibit full feedforward Σ-Δ modulator implementation is proposed. The circuit level implementation and the DWA implementation are also introduced. By reducing the oversampling to 16, the proposed multibit full feedforward Σ-Δ modulator topology is a good candidate for wideband Σ-Δ modulator design in nanometer CMOS technologies.

Both the circuit level and the system level approaches of the low-power low-voltage Σ-Δ ADC design in nanometer CMOS technologies are presented in this text. By applying these approaches to the Σ-Δ ADC design, high-performance Σ-Δ ADCs can be designed in nanometer CMOS technologies. Several test chips have proven that these two approaches are effective in implementing high-performance low-power low-voltage Σ-Δ ADCs in nanometer CMOS technologies.

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