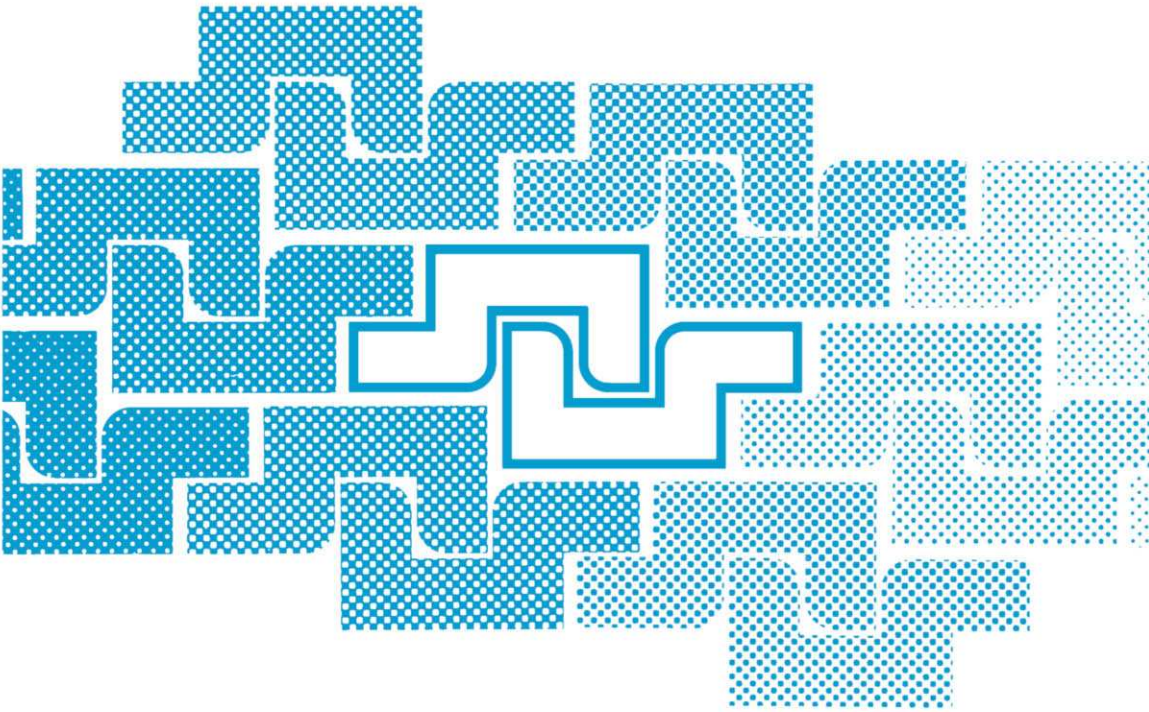


Defects in High-κ Gate Dielectric Stacks

Edited by

Evgeni Gusev

NATO Science Series

II. Mathematics, Physics and Chemistry – Vol. 220

Defects in High-κ Gate Dielectric Stacks

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Series II: Mathematics, Physics and Chemistry – Vol. 216

Defects in High-κ Gate Dielectric Stacks

Nano-Electronic Semiconductor Devices

edited by

Evgeni Gusev
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New York, NY, U.S.A.

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PREFACE

The goal of this NATO Advanced Research Workshop (ARW) entitled "Defects in Advanced High-k Dielectric Nano-electronic Semiconductor Devices", which was held in St. Petersburg, Russia, from July 11 to 14, 2005, was to examine the very complex scientific issues that pertain to the use of advanced high dielectric constant (high-k) materials in next generation semiconductor devices. The special feature of this workshop was **focus on** an important issue of **defects** in this novel class of materials.

One of the key obstacles to high-k integration into Si nano-technology are the electronic defects in high-k materials. It has been established that defects do exist in high-k dielectrics and they play an important role in device operation. However, very little is known about the nature of the defects or about possible techniques to eliminate, or at least minimize them. Given the absence of a feasible alternative in the near future, well-focused scientific research and aggressive development programs on high-k gate dielectrics and related devices must continue for semiconductor electronics to remain a competitive income producing force in the global market.

To progress towards overcoming the many fundamental obstacles blocking integration of high-k dielectrics into nano-semiconductor technology and to improve our basic knowledge of these emerging materials, more than 60 leading researchers from 16 countries around the globe gathered together at this workshop to share their recent results and thinking and to establish new collaborations with the ultimate goal to develop an atomic-scale understanding of defects in high-k and their role in devices. During this 4-day ARW, NATO country and "Eastern Block" based scientists met, tutored each other and defined directions as to where research and development should be focused over the next five years. Many of the speakers were from Europe, the U.S. and Canada. Several key speakers came from leading centers in the former USSR (Moscow, Novosibirsk, and St. Petersburg). The list of researchers represented a rather diverse group of scientists and engineers from academic, industrial and governmental labs, and included both experimental and theoretical researchers with backgrounds in basic and applied areas of physics, chemistry, electrical engineering, surface science, and materials science.

Following several introductory presentations, the first day was concentrate on processing and physical and structural properties of high-k materials (HfO_2, ZrO_2, Al_2O_3, Y_2O_3, silicates, etc) . A thorough knowledge of bulk materials properties and interfaces is required before these complex multi-component systems can hope to be understood or optimized. It was followed by a discussion of experimental and theoretical investigations of defects. The

focus of the 3rd day was electrical characterization, defects structure and effect on device performance. This day was concluded by a poster session, giving special priority to younger researchers to present and discuss their work. Finally, a review and open discussion was held to focus on both individual and collective plans for future research on defects in high-K dielectrics.

The enjoyment of the week came not only from the excellent presentations and stimulating discussions, but from the beauty of St. Petersburg amplified by gorgeous summer weather. The foreigners among us were not only delighted in the "physical" beauty of the city (architecture, Neva-river, canals, palaces, parks, etc.) but enjoyed rich cultural experiences (the Hermitage, the Palaces, opera, ballet) and the hospitality of local people.

The editor would like to thank the co-Director, Dr. V. Osipov, and the members of the International Advisory Committee, Prof. D. Buchanan, Dr. A. Dimoulas, Dr. A. Edwards, Prof. E. Garfunkel, and Prof. J. Robertson, for help in selecting participants from different countries and for their valuable comments on the scientific program. I would also like to thank all invited speakers and contributors to this book for their support and encouragement during the early planning stages of the Workshop and cooperation in meeting publication deadline. The success of the Workshop would not have been possible without the excellent planning and operation of the local team in St. Petersburg led by Dr. S. Kidalov and I. Vorobieva. It was a real pleasure to collaborate with this professional team again, after another successful NATO ARW on "Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices: Towards an Atomic-scale Understanding" in 1997. I am very grateful to Dr. V. Siklitsky for developing and maintaining the website (http://www.ioffe.ru/natoarw/2005/) and also for his help during the Workshop. I am thankful to all participants for their high-quality presentations, active participation (including peer-reviewing papers presented in this book) and fruitful discussions at the Workshop. Finally and importantly, I would like to acknowledge the hard editorial work of O. Elyukhina and D. Solnyshkov who helped us to put together presented papers into this book. The Workshop would not have been possible without financial support from the NATO Public Diplomacy Division. We also greatly appreciate financial contributions from co-sponsors, the Russian Foundation for Basic Research, the U.S. National Science Foundation (NSF), the European Office of Aerospace Research and Development (EOARD), and International SEMATECH.

August 2005
Saratoga, California Evgeni Gusev



PVD-HIGH-K GATE DIELECTRICS WITH FUSI GATE AND INFLUENCE OF PDA TREATMENT ON ON-STATE DRIVE CURRENT

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Abstract. The electrical characteristics of high-k transistors using HfO_2 and its silicate gate dielectrics are investigated. These dielectrics are formed by an oxidation of co-sputtered Hf (and Si), followed by nitridation in NH_3 gas. In case of HfSiON gate dielectrics, due to its thermal robustness, lower gate leakage with good uniformity was achieved even after higher thermal treatment. Capacitance reduction due to its lower permittivity compared to HfO_2 is compensated by introducing of Ni-FUSI electrode to reveal high on-state drive current. More highlighted is the effects of SiN capping between Ni-FUSI gate and PVD-high-k dielectric and post deposition annealing(PDA) to suppress the reaction during FUSI process. The SiN cap was found to increase the yield of transistors, however, it could not suppress the instability of drive current characteristic. The reason for this is considered to be due to the defects at the SiN capping layer caused by interfacial reaction during the NiSi formation. In addition, it is noteworthy to arouse that the replacement of poly Si with FUSI gate causes not only the elimination of poly-depletion but also the reduction of

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EOT. Hereof, by optimizing the PDA condition, as an example, stable decent electrical characteristics were obtained for the Ni-FUSI/SiN/HfO_2 stack, i.e., I_{on}(n/p) = 600/180 uA/um at I_{off} = 20 pA/um at V_{dd}=1.1V. This excellent drivability meets low stand-by power specification of the MOSFET for 45nm node.

Keywords: PVD, HfO_2, HfSiON, PDA, Ni-FUSI, SiN cap, oxygen scavenging

1. Introduction

It has been a serious challenge to compromise EOT scaling with mobility degradation for high-k gate dielectrics with a suitable Vt value. The combination of full Ni silicidation (Ni-FUSI) gate and high-k gate dielectrics is one of the most promising gate stack structures because of its high C_{inv} and EOT scaling. However, it is reported that FUSI/high-k gate stacks have worse uniformity and lower yield of transistors[1]. A systematic approach based on PVD has been employed in this work to enable optimized bi-layered gate stack by engineering the interface. In this paper, we investigate a formation of Hf-based high-k gate dielectric by PVD method and demonstrate that the instability of FUSI/high-k is caused by interfacial reaction between NiSi gate electrode and the high-k gate dielectric films.

2. Hf-based Film Formation by PVD Method

The "Hf-metal sputter + remote plasma oxidation(RPO)" technique[2] has excellent controllability to prepare HfO_2(or HfSiON) layer on the interfacial layer engineered independently in addition to its high film quality, such as less water content in the film and higher density as well as less impurity, compared to other methods. Fig. 1(a) shows a method to obtain PVD prepared HfO_2 film used in this experiment. Hf metal was first deposited on a starting surface prepared by rapid thermal oxidation(RTO). The Hf metal was successively oxidized to be HfO_2 with ~1.6 times thickness by RPO where oxygen radicals selectively oxidize the Hf at low temperature (400□). Characteristic feature of this process is oxygen scavenging during HfO_2 formation.[3] (The conventional oxygen annealing was not introduced instead of RPO to form HfO_2 film in this experiment in 4.1.) This leads to excellent thickness uniformity across the wafer. The interface was also controlled by the extended RPO time(Fig. 1(b)). It is possible to form HfO_2 film without RTO layer, however in this experiment the RTO layer was introduced to avoid the mobility degradation. By tuning the

RPO time, g_m of the FET can be easily controlled. Optimized SiN capping was used to prevent the HfO_2 from reacting with Si in the gate electrode.

3. Ni-FUSI / High-k gate stack process

In this experiment a Ni-full silicidation(Ni-FUSI) as well as conventional Poly Si(PS) were used as the gate electrode. Fig. 2 shows cross-section TEM(XTEM) image of a transistor with Ni-FUSI gate. All poly-Si gated transistors with gate lengths down to 45nm were fabricated with a conventional self-aligned process up to Ni silicidation. A standard implantation conditions as well as source/drain were tuned for the gate stack. Post deposition annealing(PDA) in the nitrogen ambient was performed after the high-k deposition. In case of nMOS transistors, the achieved V_t range is suitable for all kinds of application, however, PMOS devices exhibit high V_t even without V_t adjust implant. This implies that the poly/Hf-based high-k stacks are not suitable for the HP applications.

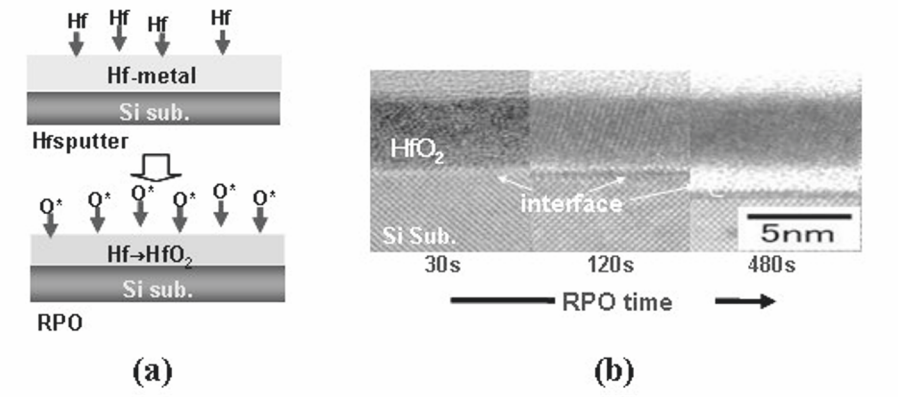


Figure 1. PVD-HfO_2 formation by means of remote plasma oxidation(RPO).

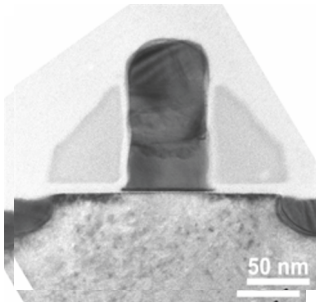


Figure 2. XTEM image of Ni-FUSI/HfO_2 gate stack. (L_g = 55nm).

Figure 3 shows the effects of poly-Si(PS) and Ni-FUSI gates on CV characteristics with respect to SiON control and PVD-HfO_2 gate dielectrics. The system of the gate stacks used are "PS, Ni-FUSI/(SiN)/1.6nm-HfO_2/1.3nm-RTO". As can be seen in the curves for SiON control, replacement of poly-Si with Ni-FUSI increases the capacitances in the accumulation(C_{acc}) for both n- and pFETs(white/black circle) by ~ 0.2 nm of EOT reduction. And from the capacitances in the inversion(C_{inv}), 0.5 nm of reduction in the CET owing to the elimination of poly Si depletion. Due to its mid-gap work function of the Ni-FUSI gate, CV curve for both n- and pFETs shift to higher V_t values. Here, it should be noted that V_t implantation condition is same for all samples except for nFET with FUSI. Under the optimized channel implantation condition, V_t for nFET with FUSI will shift further. On the other, capacitances of the PVD-HfO_2 stack with SiN capping(white/black triangle) are also increased by this gate replacement, and furthermore, 0.7 nm of EOT reduction are observed when the SiN cap is removed. When the SiN cap is removed, not only the inversion thickness,T_{inv}(CET=1.6/1.4 nm for p/nFET) but also 0.5nm of EOT reduction are obtained for the FUSI/HfO_2 stack compared with PS/SiN/HfO_2. This **implies** ***not only the elimination of poly-depletion but also reduction of EOT is induced by replacing poly Si with Ni-FUSI electrode*****.** This should be confirmed by the increasing and decreasing of the leakage current.[4] The reason for this is not yet clarified at present, however, the following possibilities are considered, 1) the interfacial reaction between HfO_2 and FUSI to consume the HfO_2, 2) Capacitance increase due to increase of the roughness between FUSI and HfO_2, 3) Band bending due to Fermi level pinning to give additional capacitance at the interface between PS and HfO_2.[5]

As for the V_t roll-off for both kinds of gate electrodes, a shift in V_t for long channel nFET is in an agreement with work function(WF) difference with poly and Ni FUSI. The V_t for pFET long channel remains, however, almost unchanged indicating that the WF did not change much as compared to the one with PS. As shown in Fig.4, when the channel implantation condition is optimized to some extent, superior I_{off}-I_{on} characteristics are obtained for the Ni-FUSI/PVD-HfO_2 compared to the best published data with poly Si gate[6] for p- and nFETs.[7] However, since pFET results scarce, further optimization in the channel implantation seems to be necessary.[8]

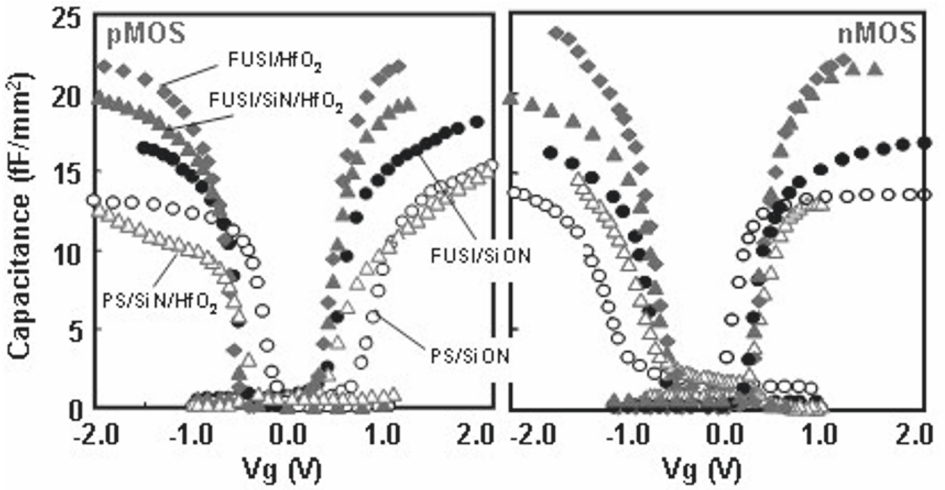


Figure 3. CV characteristics for SiON and PVD-HfO_2 dielectrics with respect to Poly Si vs Ni-FUSI gate electrode and with vs. without SiN capping.

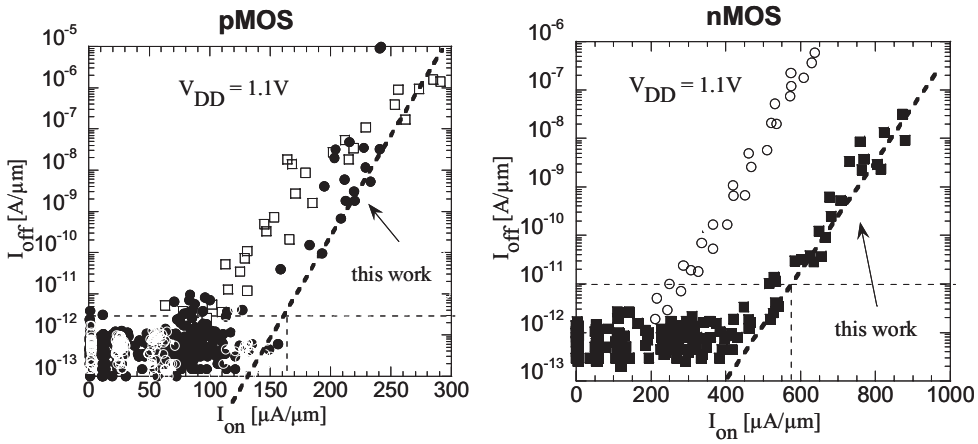


Figure 4. I_{off}-I_{on} characteristics for p- and nFETs with Ni-FUSI/PVD-HfO_2 compared to the best published data with Poly Si gate indicated by white symble[6].

4. Hf-based High-k transistor characteristics

4.1. HFSION GATE DIELECTRIC[9]

Capability of PVD-HfSiON is studied by comparison with HfO_2. The permittivity of HfSiON is smaller than that of HfO_2, however, Hf-silicate is easy to stay as amorphous and more likely to SiO_2. The film was deposited by co-sputtering by Hf and HfSi targets at room temperature followed by 1% oxidation at 500C and NH_3 nitridation at 700C. Oxidation of the sputtered Hf was performed at 500C for 30sec in 1% oxygen at atmospheric pressure for the reference HfO_2 film. Fig.5(a) shows a XTEM images for the Hf-silicate with 75, 50, 25% of Hf content after oxidation of Hf metal, where all silicates are amorphous. Concerning this, it was reported that HfSiON stays amorphous even after high temperature anneal up to 1100C.[10] Hf-rich region(darker contrast) is localized in the upper region for the smaller Hf content film. This leads to a promising Hf distribution, i.e, less Hf content at the bottom interface to reduce coulomb scattering origin. On the contrary, HfO_2 is crystallized even without any post deposition annealing (Fig.5(b)). Fig.6 shows high-frequency CV curves in the accumulation of 70x70um^2 MOS capacitors for HfO_2 and HfSiON(50% of Hf) with poly Si(PS) and Ni-FUSI gates. The results indicate higher capacitance for PS/HfO_2 than PS/HfSiON even with SiN capping layer on top of it, however, leakage current for PS/HfO_2 is higher than that for the PS/HfSiON. As described previously for the HfO_2 case, the reason why the increase of C_{acc}, i.e., EOT decreases when poly Si is replaced with FUSI is not yet clear at present. According to larger EOT and higher thermal budget, better leakage current distribution was obtained for HfSiON than HfO_2 for n/p-MOS

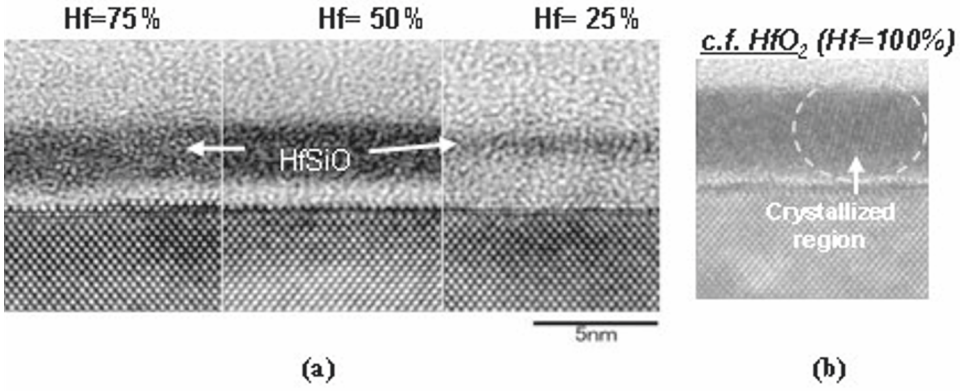


Figure 5. XTEM images for the HfSiOx with 75, 50, 25%(a) and 100%(b) of Hf content after the oxidation of pre-deposited Hf metal.

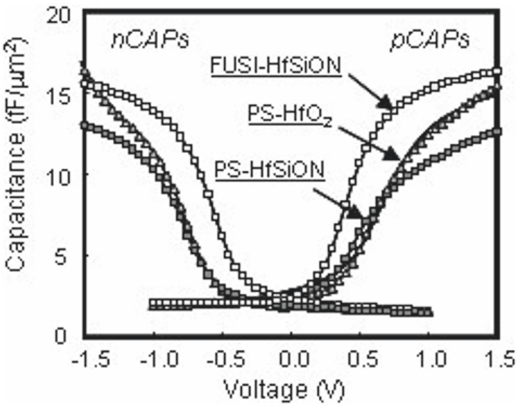


Figure 6. CV curves at accumulation regime of MOS capacitors for HfO_2 and HfSiON(50% of Hf) with poly Si(PS) and Ni-FUSI gates.

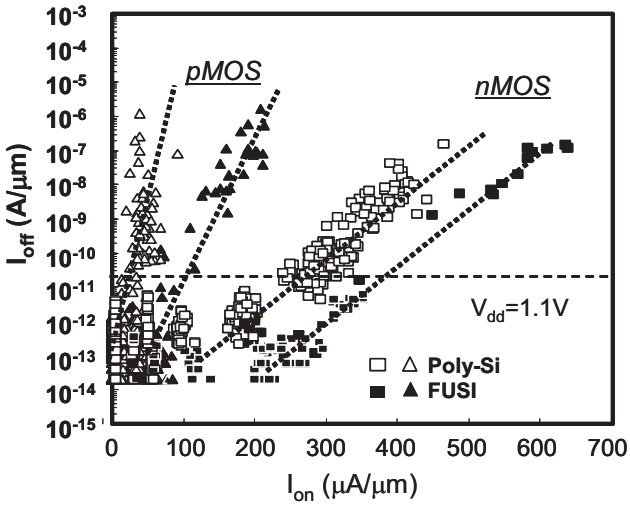


Figure 7. I_{off}-I_{on} characteristics for n/p-FETs with respect to HfSiON(50% of Hf) with poly Si(PS) and Ni-FUSI gates.

FETs(not shown here). Owing to the advantages described above, a higher on-state drive current, I_{on}(N/P) = 380/120 uA/um at I_{off} = 20 pA/um at V_{dd}=1.1V as shown in Fig.7. (Reason for the scarce data for FUSI FETs is due to imperfect optimization of the channel implant and much more data for the PS FET are plotted in this figure.)

4.2. HFO_2 GATE DIELECTRIC

Improvement of deteriorated property of the PVD-HfO_2 gate dielectric is studied focusing on the defect related phenomena at the interface. The film was formed by depositing the sputtered 1nm-Hf metal on the 1.3nm-rapid thermal oxide(RTO). Different from the previous discussion(4.1), in this case, a Hf metal was successively oxidized to be HfO_2 by RPO at 400C. The SiN cap was deposited after the post deposition anneal(PDA).

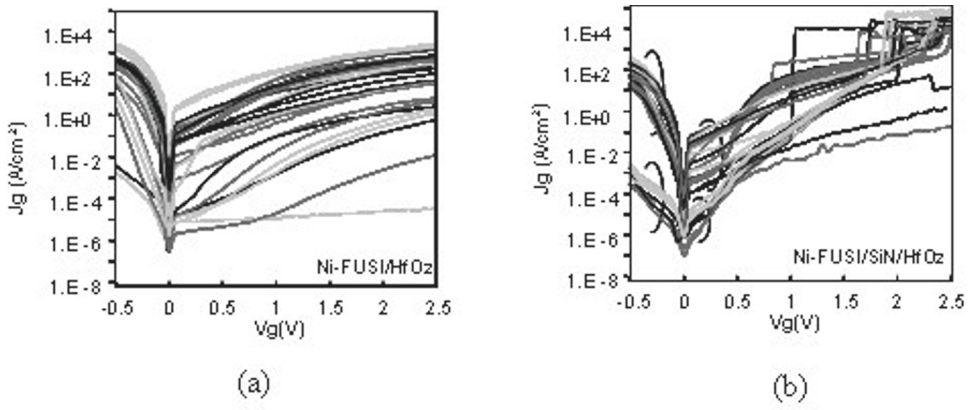


Figure 8. J_g-V_g characteristics of the Ni-FUSI/(SiN)/PVD-HfO_2 stacks with respect to without(a) and with(b) the SiN capping layer [PDA;700C].

4.2.1. *SiN Capping effect*[11]

In this section, an effect of the thin SiN capping on top of the high-k dielectric was investigated using HfO_2. The EOT value calculated from the CV curve of Ni-FUSI/HfO_2 without SiN cap is 1.0nm. The correspondent J_g-V_g characteristics indicate that J_g is scattered in a wide range with respect to without(a) and with(b) the SiN capping layer.(Fig.8) This dispersion was not observed in case of the PS/HfO_2 gate stacks, implying sort of influences of NiSi on HfO_2. When the SiN capping is introduced, the scattering in the J_g is effectively suppressed with two separated phases. The CV curves without and with SiN capping for Ni-FUSI/HfO_2 gate stacks are shown in Fig.9(a) and (b), respectively. By the capping, however, the calculated EOT increased from 1.0

to 1.2nm. Fig. 10(a) shows the comparison of I_{on}-I_{off} with respect to with and without the SiN cap. In case of w/o SiN cap, many points gather at I_{on}= 0 indicating many transistors do not work compared with the transistors with SiN caps. However, the plots in the I_{on}-I_{off} with SiN capping are still widely scattered although the corresponding V_t roll-off curves with SiN cap indicate uniform distribution compared to those w/o SiN capping.(Fig.10(b)) Split of the V_t for the devices with SiN cap in the short gate length is due to different phases in the Ni-silicide gate.[12] The above discussion implies the SiN cap can increase the yield of the transistor but it can not always provide good uniformity of electrical properties.

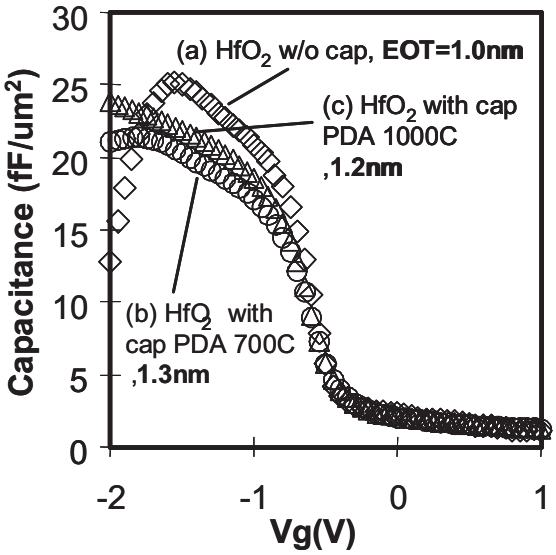


Figure 9. CV of n-MOS capacitors for FUSI/HfO_2 gate stack : (a) w/o cap, (b) with SiN cap, PDA at 700C, while (c) with SiN cap, PDA at 1000C. The respective EOT are 1.0, 1.3, and 1.2nm.

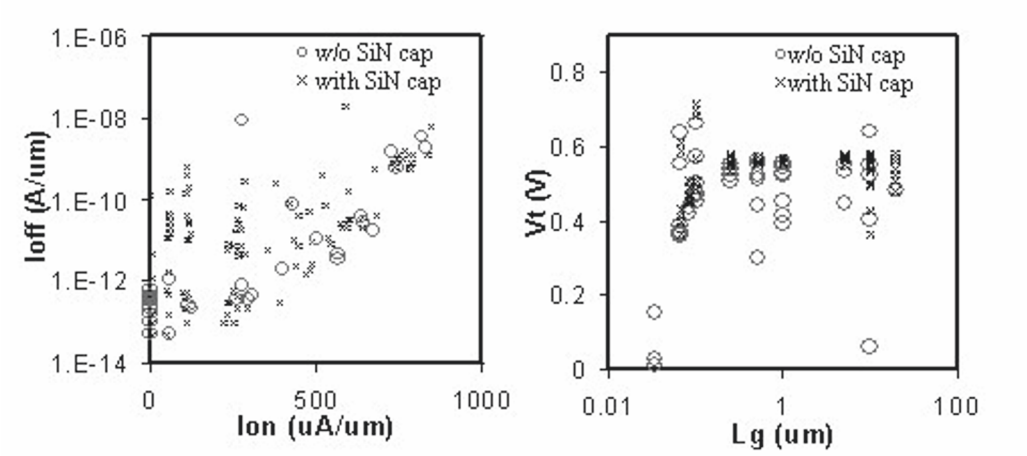


Figure 10. I_{off}-I_{on} characteristics(a) and V_t roll-off(b) of nFETs for FUSI/(SiN)/ HfO_2 gate stack. [PDA;700C] V_t split in the small L_g regime might be due to excessive Ni silicidation[12].

4.2.2. *Effect of PDA treatment – defect control*[11]

Comparison of I_{on}-I_{off} with respect to PS and Ni-FUSI/SiN/HfO_2 under PDA at 700C is shown in Fig.11. The results do not indicate scattered for the case for PS/SiN/HfO_2. Correspondingly, the J_g-V_g curves of poly-Si/SiN/HfO_2 gate stacks do not split(not shown here). This implies anomalous degradation occurs for Ni-FUSI/SiN/HfO_2 system. To explain this, we suspect that there might be some micro holes in the SiN film formed during processing. Some areas, which contain holes result in high leakage current whereas the other area without any holes exhibit less leaky behavior (Right-hand side of Fig.11). Generation of such defects in the film can be controlled by the PDA treatment to change the surface roughness as well as its film quality. And effect of the PDA is essential for the high-k gate and the electrode.[13] Fig.12 shows XTEM results with respect to conventional PDA condition performed at 700C and new condition treated at 1000C. As can be seen in this figure, it seems difficult to observe the direct evidence of the holes, however, there are some differences between them. As for the new condition, 1) an ultra thin layer indicated by bright contrast was observed at upper interface and 2) the contrast in the HfO_2 shows darker contrast compared with that for the conventional PDA case. It is possible to consider the presence of ultra-thin nitrided layer in the upper interface as for 1) and more concentrated Hf in the bulk as for 2). In addition, due to the higher temperature treatment, crystal structure seems to happen for the new PDA condition. These results may explain the above scattering phenomenon observed in the I_{on}-I_{off} and V_t plots. An ultra thin layer indicated by bright

contrast observed at upper interface is remarkable among above considerations. From this, we suspect that the interfacial reaction with NiSi causes the micro hole like deffects in the SiN film. This interfacial reaction causes not only the increase in J_g but also scatters I_{on}-I_{off} and V_t roll-off trends. The above assumption indicates that if the reaction between HfO_2 and NiSi does not occur in the whole area of the SiN film, a good uniformity of electrical properties can be obtained. Since the SiN film itself is very thin (< 0.5 nm), the film property is supposed to depend on the surface condition/roughness of the HfO_2. In this respect, we focused on HfO_2 quality by elevating the PDA temperature from 700C to 1000C. The gate leakage current is reduced and any splits in the J_g-V_g curves were not observed at all (Fig. 13(a)). Further more, scattered plots of V_t at large gate length regime are improved (Fig. 13(b)).

However, note that the split in the V_t-L_g curve at shorter gate length is caused by the excessive silicidation resulting in metal rich silicide[12] and not by the interfacial reaction. The carrier mobility decreases a little by this treatment(Fig. 14), however, as was shown in Fig.9(c), the EOT resulted in decreased value(1.2nm). This EOT reduction can compensate the mobility degradation.

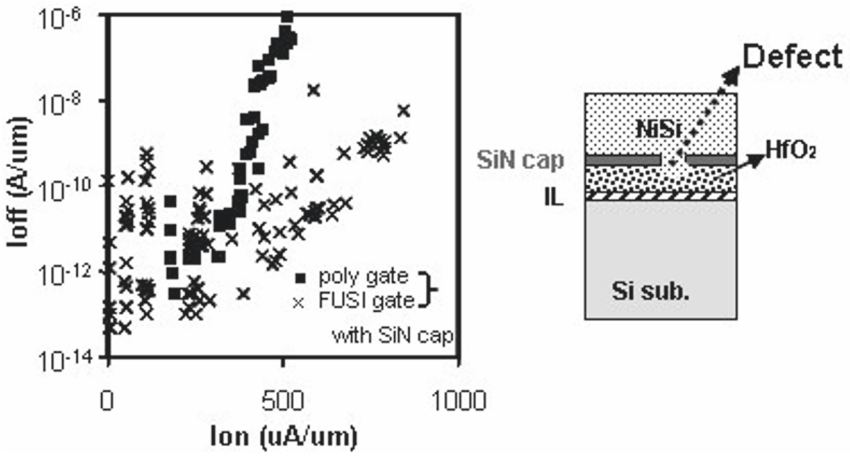


Figure 11. I_{off}-I_{on} characteristics for n-FET and with poly and FUSI gate with SiN cap and defect in the SiN capping layer. [PDA;700C].

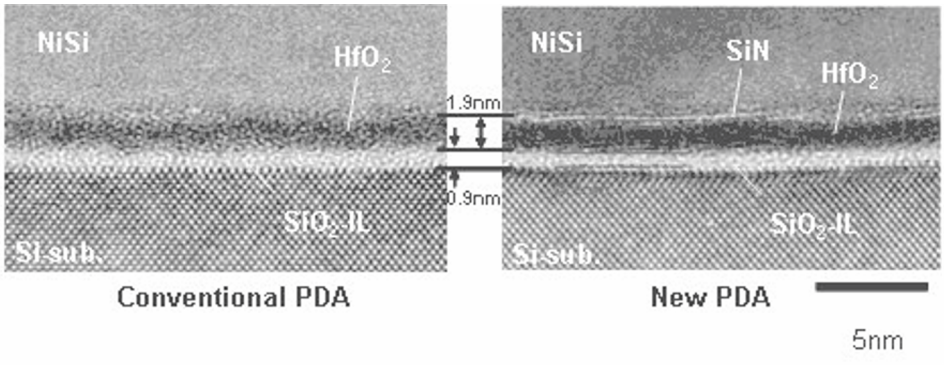


Figure 12. XTEM image with respect to conventional PDA condition(700C) and new condition treated at 1000C.

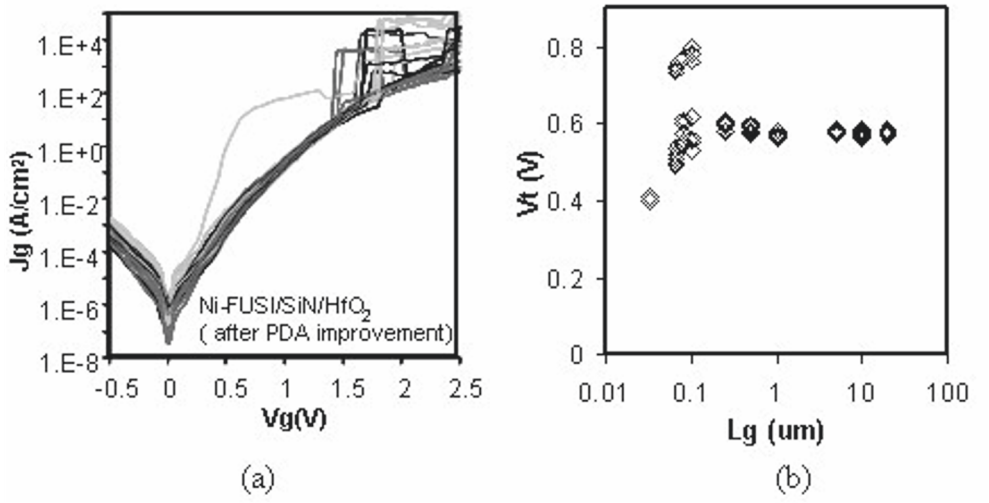


Figure 13. J_g-V_g curves(a) and V_t behavior(b) for the n-MOS transistors with Ni-FUSI/SiN/HfO_2 after PDA optimization. [PDA;1000C].

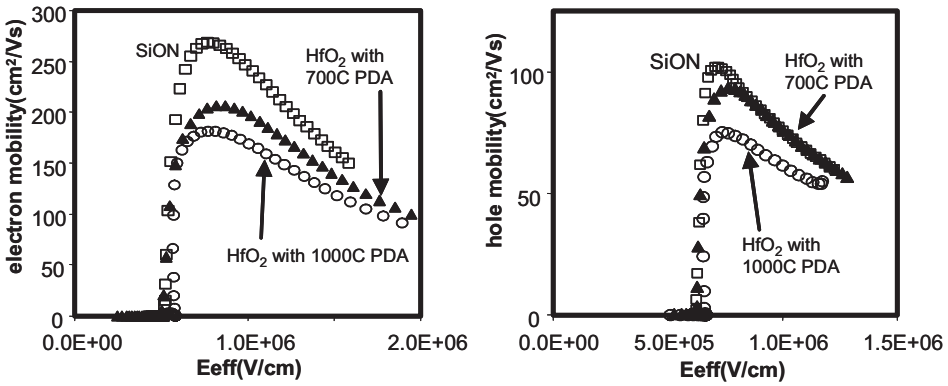


Figure 14. Electron and hole mobility extracted for SiON and HfO_2/SiN stacks with PDA performed at 700C and 1000C Mobility for HfO_2 with 1000C-PDA degrades a little.

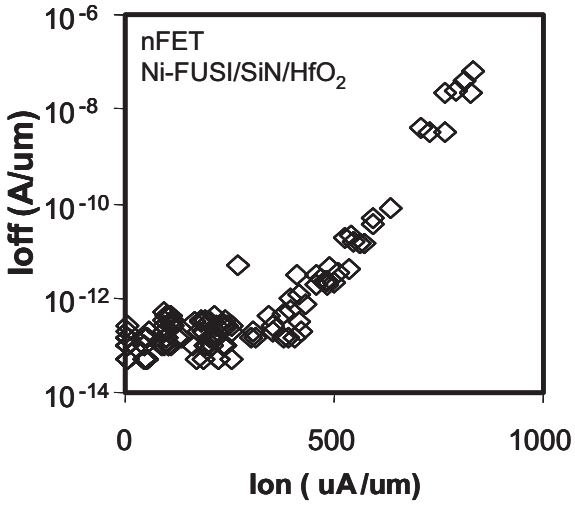


Figure 15. I_{on}-I_{off} of n-MOS transistors with improved PDA condition [PDA;1000C].

By these treatments, the I_{on}-I_{off} characteristics of nMOS transistors with Ni-FUSI/SiN/HfO_2 exhibit dramatic improvement due to the change of PDA condition and decent electrical characteristics were obtained, i.e., I_{on} (n/p) = 600/180 uA/um at I_{off} = 20 pA/um at V_{dd} = 1.1V as shown in Fig.15.

5. Conclusion

We investigated Ni-FUSI/ PVD-Hf based high-k gate stack and demonstrated that instability of electrical properties at Ni-FUSI/PVD-HfO_2 gate stacks is caused by the interfacial reaction between FUSI and high-k. This effect can be eliminated by the SiN cap on top of the HfO_2 and of PDA optimization. Important to note is not only the elimination of poly-depletion but also reduction of EOT is induced by replacing poly Si with Ni-FUSI electrode. By these treatments, decent electrical characteristics were obtained, i.e., I_{on} (n/p) = 600/180 uA/um at I_{off} = 20 pA/um at V_{dd} = 1.1V for Ni-FUSI/SiN/HfO_2 stack. In case of PVD-HfSiO(N), owing to its thermal robustness, lower gate leakage with good uniformity was achieved even after higher thermal treatment. Reduced capacitance due to its lower permittivity was compensated by introducing the FUSI gate to keep higher on-state current. These countermeasures lead to meet the low stand-by power specification for 45nm-node MOSFETs.

Acknowledgements

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EXTREMELY HIGH-DENSITY CAPACITORS WITH ALD HIGH-K DIELECTRIC LAYERS

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Abstract. This paper describes the deposition of high-*k* dielectric layers, Al_2O_3, Ta_2O_5, HfO_2, etc, in high aspect ratio pores aiming for a higher capacitance density at a given breakdown voltage. The most emerging technology to achieve this appears to be Atomic Layer Deposition, ALD. However, applying ALD to wafers with deep pores leads to additional challenges to be dealt with. Apart from e.g. roughness on the sidewalls of the pores, leading to undesired lower breakdown voltages, and native oxide layers, leading to undesired lower relative dielectric constants, carrying out ALD on wafers with a large topography needs careful consideration of the ALD process. An appropriate step coverage and proper microstructure (morphology and texture) are necessary to achieve good insulating layers, but are certainly not obvious! This paper addresses issues we ran into in our challenge to realize very high capacity densities (preferably > 200 nF/mm^2) with sufficient insulating quality.

Keywords: High-density capacitors, decoupling capacitor, passive integration, Deep Pores, ALD, High-*k*, defects, electrical characterization, PASSI, PICS

1. Introduction

In MOS technology the capacitive coupling between gate and substrate has been increased over the years by decreasing the gate-dielectric thickness down to sub 2 nm[1]. Despite the fact that this leads to higher capacitance densities,

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leakage currents through these thin layers are considerable, requiring the exploration of alternative materials. Dielectrics with a higher relative dielectric constant, so called high-*k* dielectrics like Al_2O_3, Ta_2O_5, HfO_2 are considered as serious candidates to replace SiO_2 as gate dielectric[1]. The International Technology Roadmap for Semiconductors (ITRS) even predicts imminent process integration of these high-*k* materials in the 2007-2008 timeframe[2].

Alternative dielectric materials are also considered in the field of passive components, in particular capacitors[3-7]. Besides higher capacitance values, sustainability to higher voltages is an important requirement. Theoretically, the capacitance is mathematically described by the following equation:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{t_{diel}} [F] \quad \text{or} \quad C_{diel} = \frac{\varepsilon_0 \varepsilon_r}{t_{diel}} [F/m^2] \qquad (1)$$

with A the area of the capacitor, ε_r the relative permittivity of the dielectric layer, t_{diel} the dielectric thickness and C_{diel} the capacitance density. An increased capacitance value can be obtained by:

- Decreasing the dielectric thickness, t_{diel};
- Increasing the area of the capacitor, A;
- Increasing the relative dielectric constant, ε_r.

The latter two options will be discussed in this paper. Increasing the capacitor area, A, needs to be achieved without using additional space of the silicon surface. Consequently, the third dimension, i.e. the depth of the silicon wafer, has been successfully used.

2. High-Density Decoupling Capacitors

MOS 'trench' (or pore) capacitors have been developed and implemented in Philips' PICS (Passive Integration Connective Substrate) process[3,4] to realize high-density storage capacitors. This process is a low-cost process technology including eight mask steps to integrate - with the right chip-level partitioning - passive components such as high-Q inductors, resistors, accurate planar MIM capacitors and 'trench' (or pore) MOS capacitors for e.g. supply line decoupling[8]. In this PICS process high-resistivity (1 to 5 kΩcm) Si (100) substrate wafers with a diameter of 150 mm are used. These wafers are covered with a hard mask layer of 1.0 µm thermal oxide and optionally 1.3 µm photoresist on top. The lithographic step uses a mask with a pseudo-hexagonal array of circular openings with ~1-1.5 µm diameter and 3.5 µm spacing. The wafers are etched at room temperature in an inductively coupled Reactive Ion Etching reactor using the so-called '*Bosch*' process[9], where in a time-

multiplexed way pores are anisotropically dry-etched by alternatively introducing SF_6/O_2 etching gas and C_4F_8 passivation gas into the plasma. Typical etching conditions are 12 to 16 mTorr pressure, etching and passivation time cycles of 7 and 5 s., respectively, yielding time-averaged etch rates around ~1-2 μm/min depending on pore width and depth. With this process macropore arrays are obtained with smooth pore walls and a rounded bottom, diameters of 1.5-2 μm, high aspect ratios up to ~20 and a pore depth uniformity of less than 3 %. The pore diameter is slightly larger than the mask opening due to some underetch, see Roozeboom et al.[3] for more details. Porous Si-wafers thus obtained serve as high-surface substrates for the capacitor structure.

CAPACITOR STRUCTURES

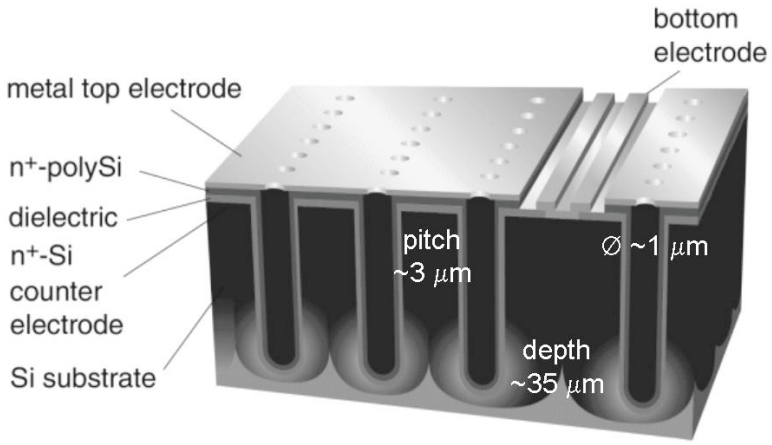


Figure 1: Schematic view of MOS capacitor scheme. The lower electrode is only for pre-testing on wafer level, enabling capacitor measurements and breakdown voltage tests. The arrays of macropores typically have a diameter of ~1.5 μm and depths up to ~30 μm.

Figure 1 illustrates the MOS capacitor with an array of cylindrical macropores containing the stack of layers composing the capacitor. The capacitors are obtained as follows. First, the pore walls of the dry-etched wafers are made highly conductive by Phosphorus diffusion into the silicon. Next, the pore arrays are filled with a nominally 30 nm 'ONO' dielectric layer stack consisting of 5 nm thermal oxide, 20 nm LPCVD nitride and a 5 nm deposited oxide layer (LPCVD-TEOS). Next, a ~0.7 μm conductive layer of n-type in situ doped poly-Si is deposited by LPCVD from SiH_4 and diluted PH_3. A furnace anneal step of 30 minutes at 1000°C renders the resistivity of the poly-Si below 1 mΩcm. The metal electrode contacts are made by deposition of a (first) Al layer and patterning after photolithographic steps.

This process yields a higher capacitance density, around 30 nF/mm^2, indicating an area enhancement by a factor of ~20. Breakdown voltages as high

as 30 V and very low leakage current densities < 1 nA/mm^2 @ 22 V have been achieved. This process has been successfully transferred to Philips Semiconductors. Higher capacitance densities, typically 90 nF/mm^2, have been achieved using thinner ONO layers[4], however, at lower breakdown voltages.

3. Atomic layer deposition in deep pores

The next step is to explore possibilities enabling a further increase of the capacitance density. For obvious reasons the integration of higher-*k* dielectric (*k* ≈ 15-25) layers in deep pores, among others Al_2O_3, Ta_2O_5, HfO_2, etc. attracts a great deal of attention, enabling a huge capacitance density increase assuming properly composed dielectric layers. The most emerging technology to achieve this seems to be Atomic Layer Deposition, ALD. In MOS technology ALD has shown already very promising results[10]. Thus, a logical question arises: can ALD be applied to wafers with high aspect ratio macro pores?

Besides the already known issues, like e.g. thermal (un)stability of many high-*k* dielectric materials[11], applying ALD in deep pores obviously leads to additional challenges to be dealt with. Apart from the roughness on the sidewalls of the pores and the immaturity of the ALD process, leading to undesired lower breakdown voltages, carrying out ALD on wafers with a large topography needs a lot of adaptation of the ALD process. An appropriate step coverage and proper microstructure (morphology and texture), necessary to achieve good insulating layers, are certainly not obvious!

ATOMIC LAYER DEPOSITION

Very briefly summarized, an ALD cycle for growing one monolayer consists of precursor 1 pulse, a nitrogen purge, precursor 2 pulse and a nitrogen purge. During each exposure step, precursor molecules react with the surface until all available surface sites are saturated. Precursor chemistries and process conditions are chosen such, that no further reaction takes place once the surface is completely saturated. This guarantees the self-limiting nature of ALD. Modern ALD processes have been primarily developed for flat wafers or wafers with minimal topography. When ALD is applied to wafers with deep pores several questions arise:

Is the amount of water enough in the pores? Is the subsequent N_2 purge sufficient to remove the water from the pores? Can the precursor enter the pores? Can it be removed during the subsequent purge? In brief, does the ALD process need any adaptation to be applied in deep pores? Since deep pores with a given aspect ratio are considered, the ALD process is taking place in the so-called Knudsen flow regime[6,12-14]. In order to find out whether the amount of

supplied gas during an ALD cycle is sufficient to adsorb one monolayer in the deep pores, the following calculation is performed.

KNUDSEN FLOW (J_K):

Let us consider the following pores:
Diameter = 2 μm (r = 1 μm)
Depth = 20 μm
From this we obtain:
Area of opening: A = $3.14*10^{-8}$ cm^2
Area of inside pore: A_{pore} = $1.2*10^{-6}$ cm^2
Volume of inside pore: V = $6.3*10^{-11}$ cm^2
For ALD the following is required:
To "grow" one monolayer on the side-wall of the pore we need:
$2*10^{15}/cm^2 \sim 2*10^{15}$ x $1.2*10^{-6} = 2.4*10^9$ mol

Through a thin orifice to vacuum:

$$J_K = w * n * \bar{c} \quad [mol/m^2 s] \qquad (2)$$

with J_K the Knudsen flow, w a constant dependent on the aspect ratio (increasing aspect ratio results in a lower w), n the gas density and $\bar{c}$ the mean velocity of the gas molecules.
For this orifice, w = 0.25; suppose the pressure is 10 mTorr:
n = $(6*10^{23}/760 * 22.4*10^{-3})*10^{-2} = 3.5*10^{20}$ mol/m^3; suppose we use SiF_4,
then: $\bar{c} = 8RT/\pi M \sim 8 * 8.31*10^3 * 300 / 3.14 * 100 = 252$ m/s
Thus,
J_K = w n c = $0.25 * 3.5*10^{20} * 252 = 2.2*10^{22}$ $mol/m^2.s$
For our pore "orifice": A = $3.14*10^{-12}$ m^2, so the quantity is:
$Q_K = 6.9*10^{10}$ mol/s
However, for a pore to vacuum: w = 2/3 r/l = 2/3 1/20 = 0.033, resulting in:
J_K = w n c = $0.033 * 3.5*10^{20} * 252 = 2.9*10^{21}$ $mol/m^2.s$
This means that for our pore (A = $3.14*10^{-12}$ m^2)
$Q_K = 9*10^9$ mol SiF_4/sec
Considering ALD: to adsorb one monolayer on the side-wall we need:
$(2*10^{15}/cm^2) \sim 2*10^{15} * 1.2*10^{-6} = 2.4*10^9$ mol
These calculations indicate that the amount of supplied gas seems to be sufficient. However, in practice there are some additional issues:

- We presume ideal (permanent) gas behavior.
- In ALD precursors there are no permanent gases. Adsorption and desorption play an important role in filling and emptying the pores[14].
- Pumping (=N_2 purge) time will be considerably longer (H_2O, HCl, ..), which is confirmed by *Figure 2*, where the pump down curve (log t – log p) is

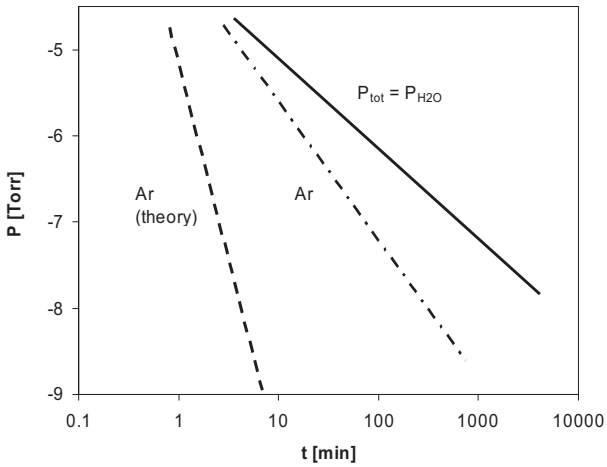


Figure 2: Pump down curve of Ar (theory) versus P_{H2O}. The pressure is plotted as a function of the time. The time to pump the permanent gasses (meeting the ideal gas law) is very short with respect to the time to pump non-permanent gases (not meeting the gas law). The pressure of water dominates the total (system) pressure.

shown for Ar (theory) versus P_{H2O} for the purpose of illustration for a given vacuum system. It is clearly observed, that the total system pressure is dominated by the pressure of H_2O (which takes much longer to remove, because of the absorbing properties of water).

What do we learn from the calculations? Deshpande et al.[15] discuss the atomic layer deposition of hafnium oxide on flat wafers. The substrate temperature is chosen between 250°C and 350°C and the reactor pressure lies between 200 and 500 mTorr. Considering the pulse/purge ratios, the following interesting phenomenon is observed:

- The H_2O pulse takes only 0.8 s., while the subsequent N_2 purge takes 12 s.!
- A similar tendency is observed for the Hf precursor. The precursor pulse takes 4 seconds, while the subsequent N_2 purge takes 8 s.

Taking our calculations into account one might expect a pulse/purge ratio close to 1. However, in practice longer purge times than pulse times are necessary to obtain good quality layers even on flat wafers, indicating that even much longer purge times will be requisite when deep pores are considered. Gutsche et al.[6] validate this: “It turns out that the time required for species transport inside high aspect ratio structures actually makes up a significant portion of the overall saturation or pulse time”.

In conclusion, applying ALD to wafers with large topography or deep pores requires a lot of adaptation of the ALD process. In first instance the N_2 purge needs to be extended to ensure complete removal of the precursors.

4. Experimental results

It is generally known that dielectric layers with a higher-*k* value exhibit a lower electrical breakdown field. Jain et al.[16] propose and explore a design space based on the experimentally established relationship between breakdown field and dielectric constant. A tradeoff between capacitance density and breakdown voltage and their variation with film thickness and dielectric constant is indicated. According to them[16], the "best can do" fit is represented by the following equation:

$$E_{BD} \approx 20/\sqrt{\varepsilon_r} \quad [MV/cm] \qquad (3)$$

This indicates that our objective- the realization of high capacitance densities at a given breakdown voltage- will certainly be compromised by this relation. We nevertheless did some first experiments in order to realize higher capacitance values, using a sandwich of different high-*k* materials.

TESTSTRUCTURES

Using the pores process as discussed in paragraph 2 some first capacitor structures have been realized, in which ALD dielectric layers were deposited. Table 1 summarizes the dielectric layers that were used.

Table 1: Dielectric layers that were used for capacitors with high-*k* ALD dielectrics. ATA stands for a sandwich of $Al_2O_3/Ta_2O_5/Al_2O_3$ and AHA stands for $Al_2O_3/HfO_2/Al_2O_3$ respectively.

Wafer ID	Al_2O_3 [nm]	HfO_2 [nm]	Ta_2O_5 [nm]	Al_2O_3 [nm]
ATA 3/12/3	3		12	3
ATA 3/6/3	3		6	3
ATA 2/6/2	2		6	2
AHA 3/10/3	3	10		3
AHA 3/5/3	3	5		3
AHA 2/5/2	2	5		2

The dielectric layers were deposited using an ALD process that is generally used on flat wafers. At a wafer temperature of 300°C the Al_2O_3, Ta_2O_5 and HfO_2 layers were deposited using TMA, PET and TEMAH as precursor, respectively. We used a sandwich of a higher *k* material that is cladded with two layers of a lower *k* material with a higher bandgap in order to reduce leakage currents as much as possible. These layers were deposited on flat wafers as well as pore array containing wafers, using the test structure shown in *Figure 3*.

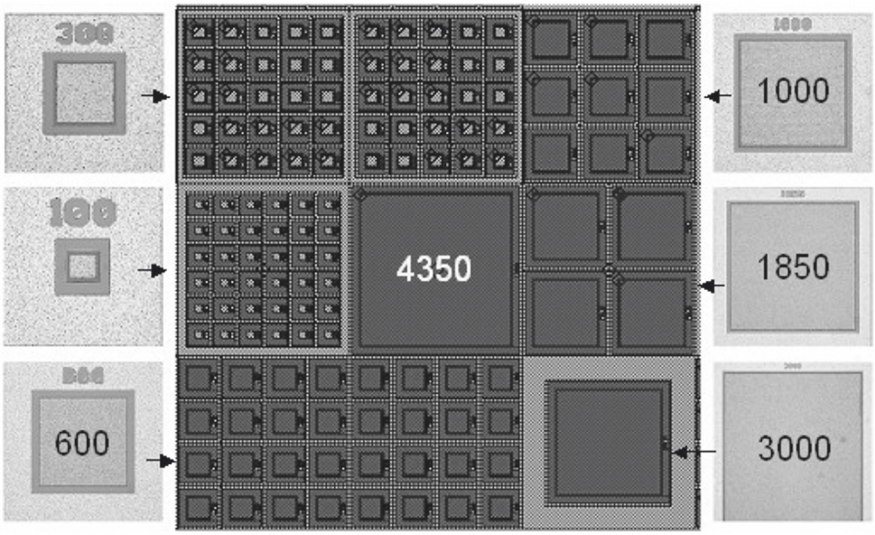


Figure 3: Layout of the capacitor test structure. The dark part in the middle is a real die on the mask. The brighter parts adjacent to the dark are top view photographs of the magnified images of different capacitor sizes under a microscope. The inner part of the test structure is the top electrode of the capacitor. The outer part forms the substrate contact.

The teststructures consist of pore capacitors with different surface areas, ranging from 100*100 μm^2 to 4350*4350 μm^2. The figure shows the mask design as well as photographs of the capacitor teststructures. Both the top electrode and the substrate can be connected from the top side of the wafer, enabling easy probing for electrical characterization.

ELECTRICAL MEASUREMENTS

After completing the technological part, the capacitors have been electrically characterized on wafer level. Capacitance (C-V) measurements, using an Agilent™4284A precision LCR meter, as well as current voltage characteristics (I-V), using an Agilent™ 4155B parameter analyser, have been carried out. To determine the capacitance value, two probes were placed on the Al top contact and the Al ring of the test capacitor, respectively. A 10 mV AC voltage was applied at a frequency f=10 kHz.

The measurement results for the capacitance value as a function of the top electrode area are plotted in *Figure 4*. It is consistently shown that the capacitance of the pore capacitors is ~20 times larger than that of the flat ones for all capacitor sizes. This is in accordance with the expected value based on the enhanced area created by the pore arrays. In order to evaluate the capacitance density performance of the high-*k* materials, the ideal capacitance was calculated for each kind of capacitor. The dielectric sandwich layers, AHA

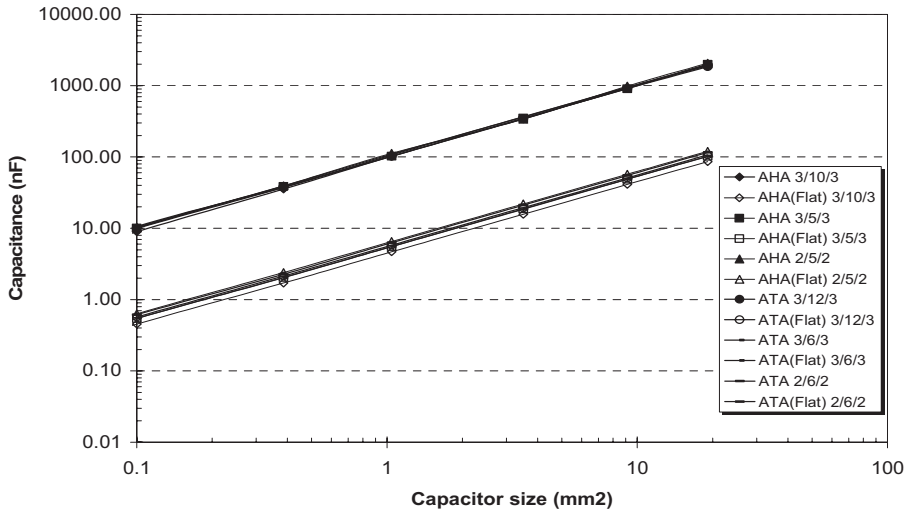


Figure 4: Capacitance vs. capacitor area for both flat capacitors and pore capacitors measured at 10 kHz.

or ATA (see Table 1), are modelled as three capacitors in series, using "ideal" k values of Al_2O_3, Ta_2O_5 and HfO_2, being 9, 26 and 25, respectively.

Figure 5 plots the measured and the calculated capacitance density. The ideal capacitance is calculated assuming of uniform layer thicknesses in the pores, a perfect microstructure (theoretical ε_r) the dielectric layers and a perfectly flat silicon surface. It can be seen that the measured capacitance density is ~100 nF/mm^2, which is already quite a good achievement. However,

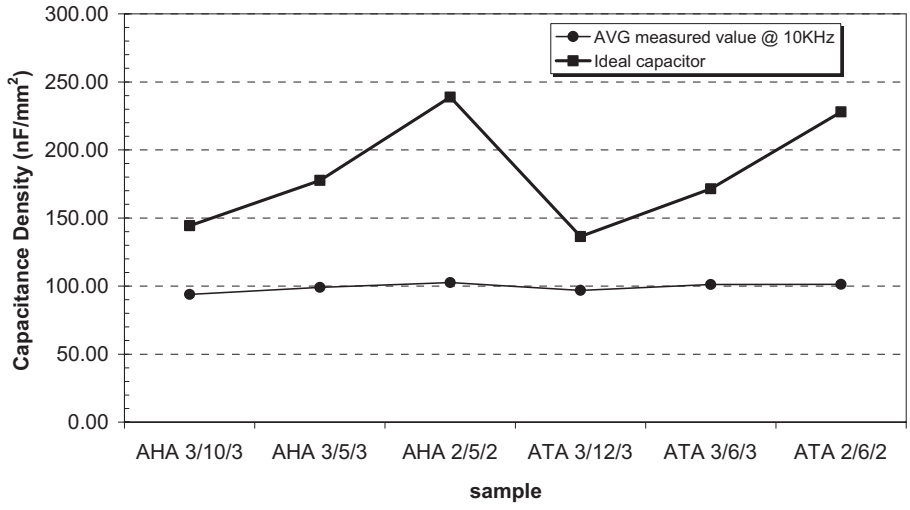


Figure 5: Measured capacitance density at 10 kHz vs. ideal (calculated) capacitance density.

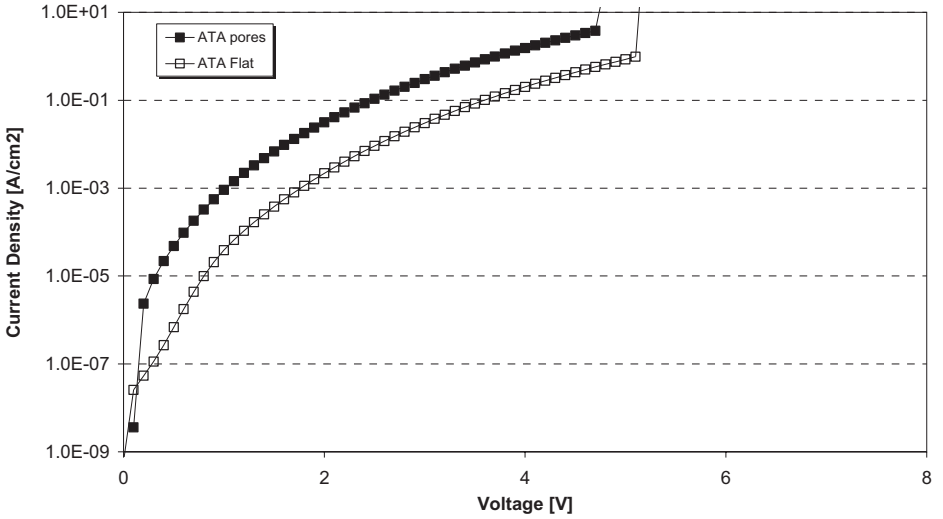
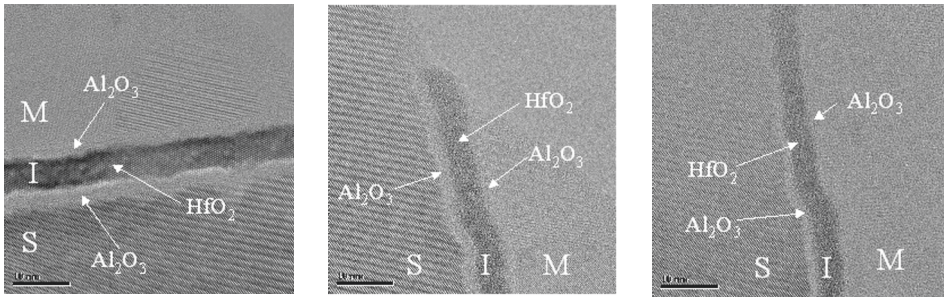


Figure 6: Current density vs. applied voltage at room temperature for the ATA 3/12/3 sample. The area of the capacitor is 100*100 μm^2.

a large deviation is observed from the ideal (calculated) capacitance density. The measured capacitance density is about 20 to 50 % lower than expected. One can think of several reasons that cause this deviation. The dielectric quality (e.g. microstructure) may be inadequate, the thickness can vary through the pore, an interfacial (native) oxide layer may be present and the interface of the etched silicon will certainly not be flat.

Figure 6 shows a typical I-V curve of an ATA capacitor structure. The current density of the pore capacitor is roughly 20 times larger than the current density for the flat capacitor, which is in agreement with the area enhancement factor. Breakdown fields seem reasonable. A value is hard to be given, since it is almost impossible to determine the exact layer thickness of the dielectric layers. In addition, the composition of the dielectric layers is not known exactly, which complicates the correct understanding of our measurements. In order to investigate the dielectric material quality, one of the AHA 2/5/2 test wafers was analyzed by TEM (Transmission Electron Microscopy). Typical cross section TEM photographs are shown in *Figure 7*. It is clearly observed that the Al_2O_3 layers are always amorphous. The HfO_2 layer is crystalline on the horizontal regions in between the pores and in shallow regions of the pores. Deeper in the pores, the crystallinity of HfO_2 seems to be less or even absent. So, ε_r will vary as a function of pore depth, causing an anomalous capacitance value. The thickness also varies, indicating imperfections of the ALD process applied to the pores. Appreciable surface roughness is observed as a result of the pore



A **B** **C**

Figure 7: High resolution TEM pictures of the high-k dielectric layer interface from AHA 2/5/2, **A** on the wafer surface, **B** at a depth of ~8 μm in a pore, **C** at a depth of ~33 μm in a pore.

etching. A native oxide (almost not visible) appeared to be present, which will decrease the capacitance density.

It goes without saying that the ALD process used was not optimal yet for wafers with pores. Despite the observed non-idealities, provoking lower capacitance values, capacitance density values up to 120 nF/mm^2 have been achieved.

5. Conclusion

This paper has shown that an Atomic Layer Deposition process needs adaptation when used for substrates with large topography or ultimately high aspect ratio macropore arrays. Timing of the cycling of the gases (including N_2 purging) needs to be optimized for additional adsorption and desorption processes of precursors. ALD high-*k* dielectrics are very promising candidates for replacing SiO_2 as a dielectric layer. Preliminary experiments have shown an increased capacitance value ≅ 120nF/mm^2, which shows the potential of this technology. Much higher capacitance densities are within reach, if ALD grows to maturity. Breakdown voltages are considerably lower than for SiO_2 layers and need much more attention. However, first results are encouraging and are challenging for more research in the near future.

Acknowledgements

Jurgen van Berkum is kindly acknowledged for the TEM analysis.

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TOWARDS UNDERSTANDING OF PROCESSING-NANOSTRUCTURE-PROPERTY INTER-RELATIONSHIPS IN HIGH-K/METAL GATE STACKS

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Abstract. This paper summarizes the challenges and opportunities that lay ahead in screening candidate metal gate electrodes and their integration in a standard CMOS process in order to replace the aging poly-Si gate electrodes. In particular, special emphasize on defects in the gate stack, its potential origin and its influence on device properties will be discussed. For example, the deleterious effects of bulk charges in high-k on effective extraction of work function of the metal gates, and influence of metal gate processing on final structure of the gate stack and its device properties is discussed in detail.

Keywords: Metal Gates, High-k, Defects, Effective Work Function

1. Introduction

The IC scaling trends (2003 ITRS) suggests that the low power applications will require high permittivity dielectrics (high-k) by the year 2006, while the high performance devices will soon require both high-k dielectrics and metal gate electrodes to eliminate poly depletion as devices scale down to the 1 nm equivalent oxide thickness (EOT)[1]. In this respect, metal gates have many important features, in particular, lower gate resistance, elimination of the B penetration from the doped poly-Si into the gate dielectric and transistor channel, and apparently smaller (compared to poly-Si) interaction of the gate

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materials and the underlying high-k films. In order to achieve appropriate threshold voltages one needs to integrate metal gates with appropriate effective work function (EWF) values, which can easily be controlled via dopants in conventional poly-Si/SiO_2 case[2]. It is noteworthy that despite several groups studying metal gates over many years, there still appears to be lack of consensus on the material systems to be used and a large disparity in reported EWF of metal gates for similar materials from different research groups[3-12]. One of the primary causes for this disparity is limited understanding of the defect structures within the gate stack and comprehension of its deleterious affects on device properties.

This paper describes and validates a novel technique to accurately extract the EWF of metal gates despite the bulk charges in the high-k. Additionally an understanding of the thermal stability and influence of metal gates on device properties is forwarded.

2. Extracting Effective Work Function of Metal Gates

The EWF of a metal gate can be extracted from the capacitor-voltage (C-V) measurements, according to equation 1. In the case of conventional SiO_2-type dielectrics, one can vary the dielectric thickness and extract ϕ_{MS} (to calculate gate work function) from the linear extrapolation of V_{fb} vs equivalent oxide thickness (EOT) plot.

$$V_{fb} = \Phi'_{ms} - \frac{Q_f * EOT}{\varepsilon_{ox}} \qquad (1)$$

The underlying assumptions of this technique is that the interface charge density, Q_f, is constant for all samples, and the dielectric exhibits minimal bulk charge. However, both these assumptions may not hold for the high-k dielectrics due to high density of fixed bulk charges in the high-k films and effects of the high-k deposition on the underlying interfacial sub-oxide layer. This is particularly true in the case of measurements on high-k gate stacks, where interfacial oxide characteristics are less well understood, and may be affected by the varying depositions of high-k films of various thicknesses. A modified equation, accounting for the various charge terms in an advanced gate stack with high-k dielectrics as shown in equation 2, needs to be used to extract ϕms.

$$V_{fb} = \Phi'_{ms} - \frac{Q_i * EOT_{HfOx}}{\varepsilon_{ox}} - \frac{\rho_b * (\varepsilon_h / \varepsilon_{ox}) * EOT_{HfOx}^2}{2 * \varepsilon_{ox}} - \frac{Q_f * EOT}{\varepsilon_{ox}} \qquad (2)$$

Here, the gate stack is modeled to consist of the high-k layer with bulk charge density ρ_b, and EOT_{HfOx}, an interfacial layer (IL), which is SiO_x like with comparably insignificant bulk charge but interface charges Q_i and Q_f for high-k/IL and IL/Si substrate respectively. Although one may be able to extract the EWF of metal gates using this complicated equation, often times, these many variables compromise the accuracy of EWF extraction.

An improved procedure, developed at SEMATECH, is to form the entire range of oxide thicknesses on a single wafer by growing a relatively thick oxide and selectively etching back regions with a benign wet etchant[13]. Evaluation of metal gate work function on high-k can be done by processing a fixed high-K thickness on the "terraced" oxide. By doing so, one can fix and minimize the high-k bulk charge contribution and demonstrate linear V_{fb}-EOT relationship. This "terrace oxide" technique has been demonstrated to exhibit excellent linear Vfb-EOT fits with minimized effect from variation in Q_f as shown in Fig 1 (2nm HfO_2). Also shown in Fig 1 is the non-linear relationship once the high-k thickness increases (on the terraced oxide) clearly demonstrating the influence of high-k bulk charges. It is important to note that one may extract very different EWF values from such non-linear V_{fb}-EOT relationships (for HfO_2 > 2nm in Fig 1), by considering just specific regions in the V_{fb}-EOT plot. This maybe one of the main reasons for such large disparity in reported EWF values of similar materials by different research groups. For high-k/metal gate systems, it is imperative to understand the effects of defects in the gate stack and often times utilize novel methodologies (unlike SiO_2 case) to extract meaningful parameters. The extracted EWF values for terraced oxide technique were also correlated to the threshold voltage from transistors with the same metal gate. Figure 2 shows the excellent 1:1 correlation further validating the effectiveness of terraced oxide technique in accurately extracting the EWF of metal gates on high-k dielectrics.

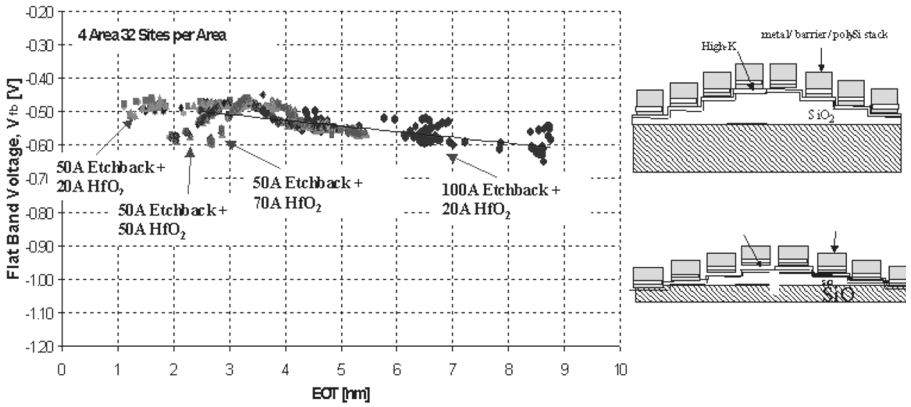


Figure 1. Schematic of the terrace oxide capacitor structure and the Vfb-EOT relationship for different stacks of high-k thickness on terraced oxide.

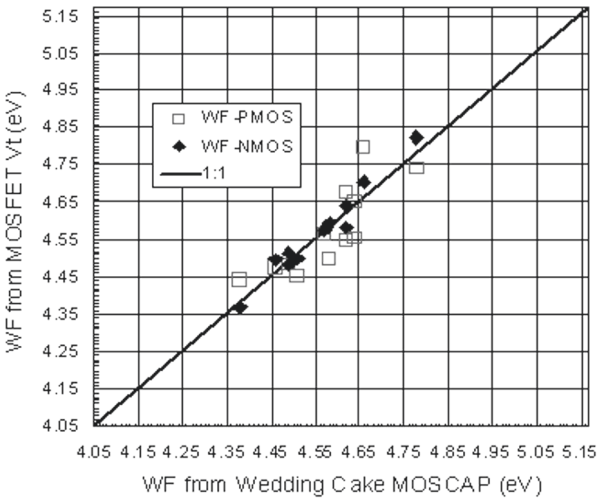


Figure 2. Correlation of EWF extracted from terraced oxide capacitor structures and threshold voltage of transistors with metal high-k stacks.

Using the novel technique the various factors that could affect the EWF of gate electrode in the advanced gate stack were studied carefully. Several hypotheses including Fermi-level pinning (FLP), metal induced gap states being formed due to the penetration of wave function from metal into the

dielectric, presence of dipoles at the metal high-k interface, have been proposed to explain commonly observed shift in the effective work function of the metal gates and its dependence on the dielectric layer[14-16]. However, data generated in this study (Fig 3) did not exhibit observable evidence of FLP, suggesting again that a comprehensive understanding, which should include the structure-property interrelationship, is still lacking.

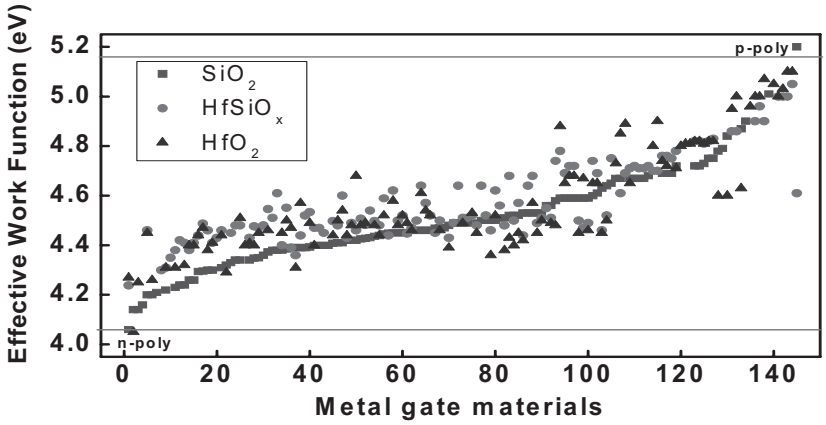


Figure 3. Summary of EWF of several metal gate materials on different dielectrics after full thermal processing (1000 ^{o}C 5 sec).

3. Metal Gates Influence on Device Properties

Considering the incorporation of high-k and metal gates in conventional gate first CMOS flow, where in high temperature source/drain activation annealing is inevitable for dopant activation, it becomes imperative for metal gate stacks to exhibit good thermal stability on high-k gate dielectrics. The stability issues include material diffusion across the layers in the gate stack and/or interfacial reactions that affect the device properties and reliability. The following sections discuss examples of these instability issues for select metal gate material systems.

3.1. DEFECTS DUE TO METAL DIFFUSION ACROSS GATE STACK (THERMAL STABILITY ISSUES)

Although, one of the primary screening parameters (based on physical properties) to down-select potential metal gate materials is the melting point,

one needs to also be cognizant of the potential defect formation due to the diffusion of these elements across the gate stack especially if they form deep level defects within the Si band-gap. Also, metal diffusion and subsequent accumulation near the substrate-dielectric interface can significantly increase the interface trap states, which in turn degrades the device performance and reliability. Figure 4 shows significantly increasing Dit with reducing gate oxide thickness for Ru electrodes suggesting instability of Ru on SiO_2 gate dielectrics. Figure 5 shows high-resolution images of a typical Ru-SiO_2.-Si stack as a function of the anneal temperature. Again, this data corroborates the electrical data suggesting that Ru is indeed unstable on SiO_2 dielectric at elevated temperatures despite its high melting point. Similar work of Ru on hafnium based high-k dielectrics (Hf-Si-O) indicated that the stability of Ru electrode increased with HfO_2 content[17].

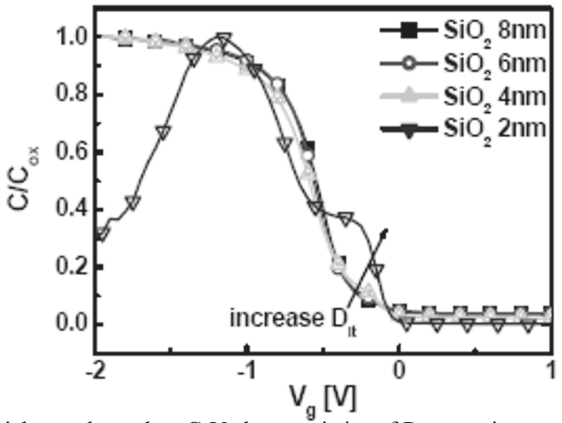


Figure 4. Thickness dependent C-V characteristics of Ru capacitor.

Typically the detection limits of electrical characterization techniques are far superior compared to physical characterization techniques to detect defects caused by such thermal instabilities. This is especially the case when small amounts (physically undetectable) of metallic elements (from gate electrode) diffuse down to the Si substrate to form deep level defect states that can participate in reduction of the minority carrier lifetime. A capacitance-based technique was recently developed at SEMATECH, to monitor degradation of minority carrier lifetime and relate it to the diffusion of metal elements across the gate stack.

Figure 6 shows the time dependence of inversion capacitance of two metal gates (TiN and Mo) on two thicknesses of SiO_2 dielectric. With reducing thickness the C/C_{final} value decreases due to direct tunneling current. When comparing the different metals in Fig. 6, there is clear indication of significant reduction in minority carrier lifetime for Mo electrode case as there is no

observable deep depletion. Note, SIMS measurement for the Mo stack on 2nm SiO_2 also exhibited Mo diffusion across the stack. However, detection of metal diffusion issues using SIMS technique becomes more complicated in highly scaled gate stacks due to matrix effects. On the other hand, this electrical technique is very sensitive (ppm levels) to metal diffusion and is an extremely valuable methodology to screen out material systems that may compromise the integrity of the gate stack during high temperature IC processing. Utilizing this technique, several material systems were evaluated carefully and it was found that, in general, nitrided metal gates exhibited high thermal stability as opposed to pure metals and/or metal alloys.

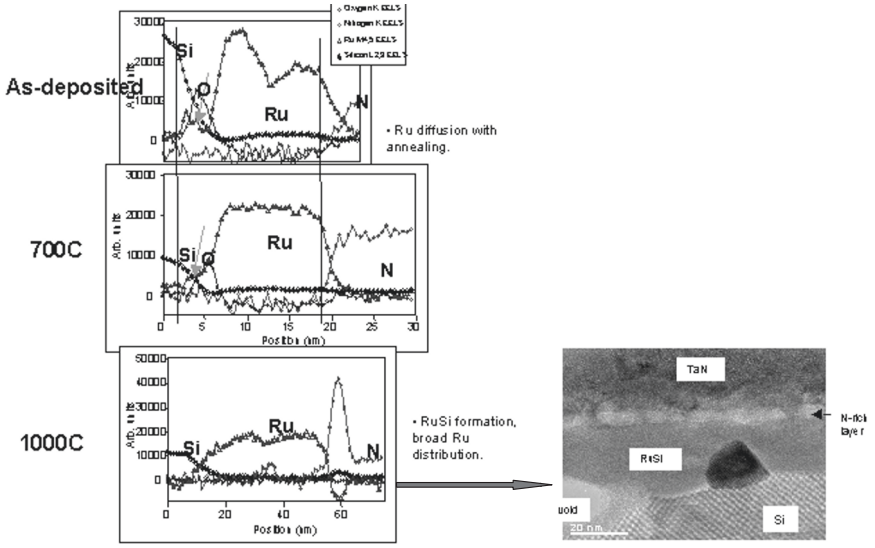


Figure 5. High resolution TEM image and chemical composition scans across a Ru/SiO_2 (2nm)/Si stack annealed at different temperatures.

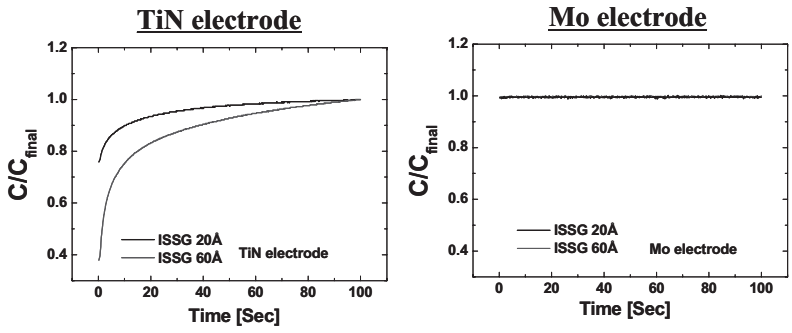


Figure 6. Capacitance-time measurements to observe deep depletion behaviour for Mo and TiN gate stacks.

3.2. DEFECT STRUCTURES IN METAL-SI-NITRIDE METAL GATE SYSTEMS

As discussed in the earlier section, thermal stability is key in identifying candidate metal gate material systems that can replace poly-Si in future generation CMOS. In this respect high temperature stable metal nitrides are attractive systems, provided the EWF is tuned to band-edge values even after high thermal processing[18]. One candidate system that has been widely studied as a potential NMOS candidate is Ta-Si-N system. Although most of the early work on this system was primarily focused on its barrier like properties for backend application and MIM capacitors, recent studies showed that the EWF of this system could be tuned by controlling the composition[19]. Additionally in certain composition regimes, the material remains amorphous making it a promising gate electrode material. However, interestingly, there have been limited reports exhibiting high performance transistors with band-edge EWF values with this system. Earlier work investigating factors that control the EWF in Ta-Si-N system showed that Si% influenced the final EWF value significantly[19]. Also, the chances of forming an amorphous like structure was high when processing along a TaN_x-SiN_x tie line in the ternary system. In this study, transistors with varying Si% in Ta-Si-N system on optimized hafnium based high-k ($HfSiO_x$) dielectrics were processed.

Figure 7 (a) shows the mobility curves for the three metal gates on 2nm of $HfSiO_x$. The EWF value of Ta-Si-N and the % of Si increased in going from process A to process C. Surprisingly, the process change for metal gate exhibited a significant influence on the electron mobility in substrate Si

channel. Note, the HfSiOx used in this study has previously been demonstrated to exhibit excellent mobility (close to universal) with TiN metal gates. Various factors including charge scattering, soft optical phonons, transient charge trapping, have been proposed to explain commonly observed mobility degradation in hafnium based high-k dielectrics[20-22]. However, the dependence on metal gate processing and material is less understood. Hence in-depth characterization (electrical and physical) of this system was carried out to correlate the physical structure to the observed electrical properties. Figure 7 (b) shows the mobility curves for these gate stacks using pulsed Id-Vg measurements. Note, by measuring Id-Vg at shorter pulse widths, one gets around the problem of transient charge trapping. This measurement clearly showed that most of the observed mobility degradation was indeed due to transient charge trapping. Figure 9, depicts this same degradation (due to transient charging) as a function of pulse width of the Id-Vg measurement. Now, in order to understand the origin of the transient charging in these stacks, the nanostructure was probed under high-resolution transmission electron microscope. The inset of Fig 8 shows an image of the stack for process C. The TaSiN in this case showed evidence of phase segregating into a TaN_x rich TaSiN and SiN_x rich TaSiN phases.

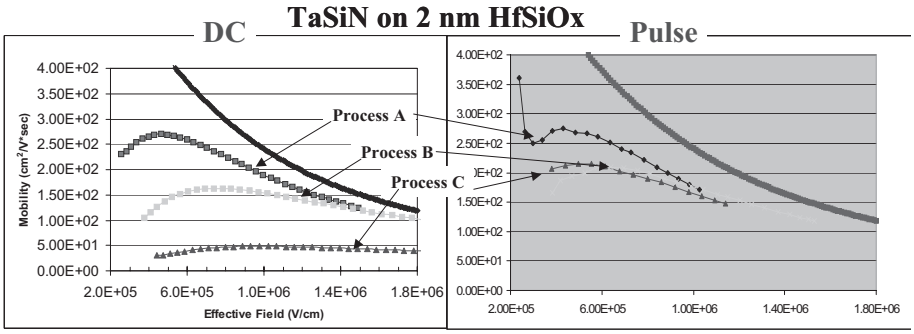


Figure 7. Influence of Ta-Si-N process conditions on transient charging (a) mobility curves extracted from DC measurements (b) mobility curves extracted from pulsed Id-Vg measurements.

All the TaSiN stacks that showed mobility degradation also exhibited phase segregation suggesting the possibility that the phase segregated structure forms electron traps and/or the process of phase segregation initiates a reaction between high-k and metal to form defects that act as electron traps. Note, given this understanding it was possible to alter the processing to deposit TaSiN films with excellent device performance by controlling the final nanostructure. These examples clearly illustrate that comprehension of the influence (device

properties) of defect structures and its potential origin (process conditions) is imperative to realize high performance metal-high-k devices.

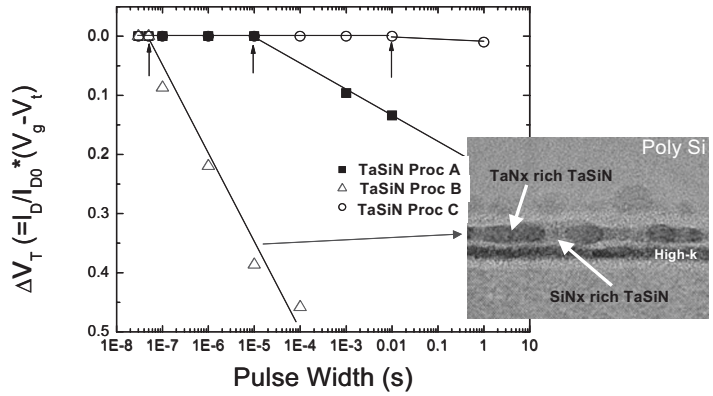


Figure 8. Normalized drift in Vt due to transient charging as a function of processing of TaSiN/HfSiOx stacks.

4. Summary

This paper summarized important challenges and opportunities of identifying and integrating candidate metal gate electrodes in a standard CMOS process. Using specific examples, the role of defects in the gate stack, its potential origin and its influence on device properties was discussed. For example, the deleterious effects of bulk charges in high-k on extraction of work function of the metal gates, and influence of metal gate processing on final structure of the gate stack and its device properties is discussed in detail. Also, a novel technique to accurately extract the effective work function of metal gates despite high bulk charges in the high-k dielectrics is forwarded and minority carrier lifetime measurement along with conductance method are introduced for the first time to investigate the interaction between metal gate and gate dielectric.

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ON THE CHARACTERIZATION OF ELECTRONICALLY ACTIVE DEFECTS IN HIGH-κ GATE DIELECTRICS

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Abstract. A number of techniques are discussed with regard the measurement of electronically active defects in high-κ gate dielectrics. Following a short review of 1st-order trapping kinetics, a discussion of its limitations, especially with respect to high-κ gate dielectrics is included. It is suggested that, due to the nature of the proposed trap modulated transport in high-κ gate dielectrics, the 1st-order trapping kinetics used historically for SiO_2, may not be applicable without significant revision. However, the measurement techniques using the standard "stress and sense" methodology, where charge is injected into the film and the effects of the charge trapping are measured with either capacitance-voltage (ΔV_{FB}) and/or current-voltage (ΔV_t) to measure the effects of the charge trapping may still be applicable if reasonable assumptions may be made. A discussion of the positioning of trapped charge (i.e. bulk vs interface) is included. Data from HfO2 using electron injection via internal photo-emission and charge centroid extraction using the "photo I-V" technique suggest that centroid of the trapped charge is within the bulk of the high-κ film independent of bias polarity and photon energy. Techniques involving transient current analysis using charge pumping in both "conventional base sweep" and "amplitude sweep" and pulsed I_{DS}-V_G are also presented. While these techniques are capable of measuring interfacial and near-interfacial trapped charge, their usefulness for obtaining a full understanding of spatial or energetic trap distributions is limited.

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1. Introduction

Scaling[1] has driven the gate dielectric, traditionally silicon dioxide, SiO_2, to less than acceptable limits (< 20Å) where the gate leakage currents are a substantial detriment to device operation[2,3]. The continued decrease of the SiO_2 thickness is no longer possible for future CMOS and therefore replacement dielectrics need to be found. The new dielectric materials must emulate as many of the good SiO_2 qualities as possible. These "new high-κ" materials, which can be made thicker to reduce the leakage current while increasing the capacitance, via a higher dielectric permittivity, $\varepsilon_{high\text{-}\kappa}$, are required and notably Al_2O_3[4-6], ZrO_2[7-10] and especially HfO_2[11-16] and its silicates[11,16], have shown some promise. Nonetheless, these new gate dielectric materials are not without problems. Fixed and trapped charge cause serious performance degradation by shifting the threshold voltage, limiting transistor mobility and reducing device lifetimes[11,17-22]. It is the nature and properties of the trapped charge; and the measurement thereof, in these new high-κ dielectrics that is the main thrust of this dissertation.

2. Characterization Techniques

The charge trapping (and de-trapping) in high-κ films, or for that matter just about any dielectric film used in the semiconductor industry, is commonly characterized using one technique to inject charge into and/or through the gate dielectric and a second technique to measure the density, and possibly the position of trapped charge either within the dielectric layer or at one of its interfaces. This is typically referred to a "stress and sense" technique. There are

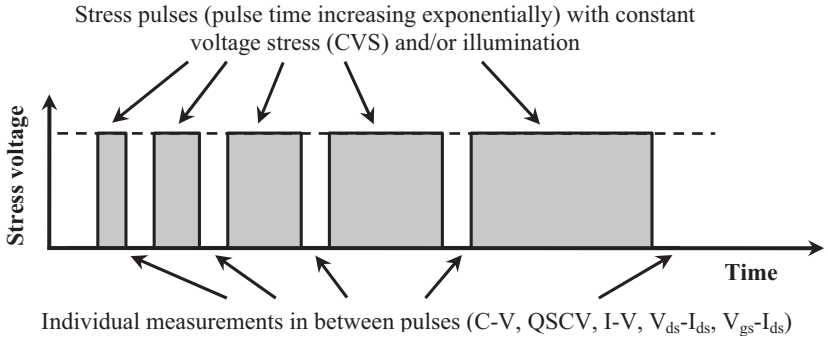


Figure 1. Constant voltage "stress and sense" technique.

numerous examples of this type of characterization dating back many decades[11,12,18,20,23-27]. This stress and sense technique can be illustrated as shown in Figure 1.

Typically, voltage pulses, (or current pulses in the case of constant current stressing) are applied to the sample often in a exponentially increasing pulse width. In between each stress pulse, a capacitance-voltage or current-voltage technique is used to sense the trapped charge density.

Capacitance-voltage techniques can be used to sense trapped charge as a result of their effect on the field within the dielectric and therefore the band-bending within the silicon substrate. This relationship may be given by [26]

$$\Delta V = \left[\frac{\int_0^d x\, n(x,t)\ dx}{\int_0^d n(x,t)\ dx} \right] \frac{q\, n(x,t)}{\varepsilon_{oxide}\ \varepsilon_o} \tag{1}$$

where

$$\bar{x} = \frac{\int_0^d x\ n(x)\ dx}{\int_0^d n(x)\ dx}, \tag{2}$$

and n(x,t) is the trapped charge distribution within the dielectric, ε_o and ε_{oxide} are the free space elative dielectric permittivity and $\bar{x}$ is the centroid of the charge distribution as measured from the gate side of the dielectric. Often this expression is simplified using $\bar{x} = t_{ox}$ for charge assumed to be at the Si/oxide interface or $\bar{x} = t_{ox}/2$ for charge uniformly distributed throughout the dielectric. For the former case, using ΔV_{FB} to measure the charge (qN_t) induced voltage shift in a capacitance-voltage curve, Equation (1) becomes

$$\Delta V_{FB} = \frac{\bar{x}\, q\ N_t}{\varepsilon_{oxide}\ \varepsilon_o}. \tag{3}$$

As an example a series of capacitance-voltage measurements are shown in Figure 2(a), for HfO_2 / SiO_2 (90/15 Å) capacitors with an area of $5x10^{-3}$ cm^2 as a function of injected charge. For these particular stressing experiments a photo-injection technique with a 3.4 eV illumination was used to inject charge into the dielectric film. The measured ΔV_{FB} as a function of injected charge, shown in Fig. 2(b), yields a positive voltage shift indicating a net negative trapped charge. A number of points should be noted with regard to the data shown in Figure 2. Although the C-V curves in Figure 2(a) shift substantially showing a large trapped charge density, ~10^{13} cm^{-2}, the curves shift in a parallel fashion indicating a small change in the interface state density, D_{it}. This is only an approximation and a measurement of the interface state density would be required to make any accurate statement regarding the true nature of the trapped

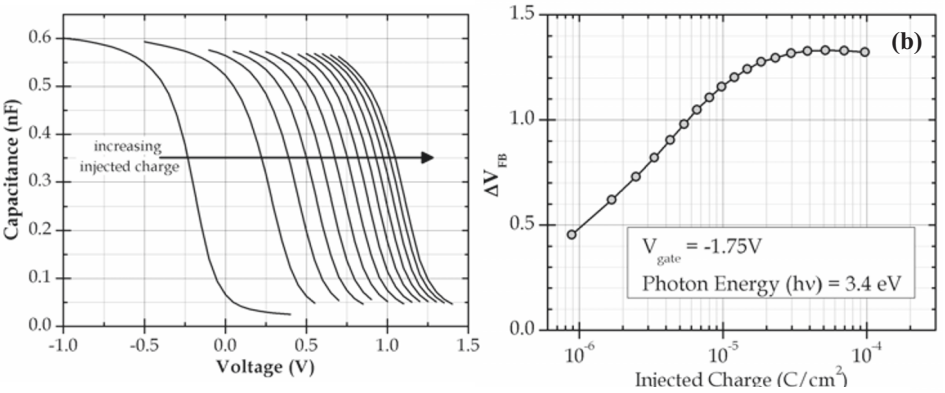


Figure 2. Capacitance-voltage curve shifts and ΔV_{FB} as a function of the injected charge.

charge. From the data shown in Figure 2(b), the trapped charge density, as determined from ΔV_{FB}, appears to be saturating if not even decreasing for large injected charge densities. Assuming that there is no "trap creation[28]", this apparent saturation could occur for a number of different reasons. If the total density of defects is fixed, at sufficiently high injected electron densities, all traps should be filled and as such ΔV_{FB} should saturate. However, de-trapping is likely also occurring, and possibly at a rate different from that for trapping. At some point, de-trapping may start to dominate and the "effective trap density" could reach a "steady state" value or even begins to decrease. To review this analysis 1st-order trapping kinetics is presented in the following section.

2.1. TRAPPING KINETICS

A simplistic, and sometimes inaccurate, fit to the data shown in Figure 2 can be obtained using 1st-order trapping kinetics[26] where the electron trapping rate is given by

$$\frac{dn_t}{dt} = k_c(N - n_t) - k_p n_t - k_t n_t \,, \tag{4}$$

and

$$k_c = n_c \, v_{th} \, \sigma_c \,, \qquad k_p = F_p \sigma_p \qquad and \qquad k_t = N_c \, v_{th} \, \sigma_c exp\left(-\frac{Et}{kT}\right),$$

where n_t is the trapped charge density, N_t is the total trap density, n_c is the conduction band electron density, v_{th} is the electron thermal velocity, σ_c is the trap capture cross section, F_p is the local photon flux, σ_p is the photo ionization cross section, N_c is the density of states at the edge of the conduction band and E_t is the electron trap depth as measured from the conduction band edge. Similar

expressions could be written for hole trapping and de-trapping. Equation (4) can be simplified and solved if some or all of the following assumptions are made. Since in this case a photo injection technique is used, either a small photon flux or a small photo-ionization cross section would be required. Experiments can be

$$\frac{dn_t}{dt} = n_c \, v_{th} \, \sigma_c (N - n_t) \tag{5}$$

and have been made to verify this assumption. If the trap were sufficiently deep, such that $E_t >> kT$ then the thermal de-trapping term could also be removed. Therefore Equation (4) would reduce to

For the transport of carriers through the films, the externally applied current density is normally given by

where v_d is the thermal drift velocity. This approximation, although valid for SiO_2, has not been shown to be the case for other films. If the transport of electrons through the dielectric film(s) of interest is dominated by some trap-

$$\frac{J}{q} = n_c \, v_d \approx n_c \, v_{th} \, , \tag{6}$$

mediated process, for example trap-assisted-tunneling[29] or Frenkel-Poole[30] hopping, this expression would have to be modified. For the sake of simplicity, and for this initial discussion, it will be assumed to be valid. Equation (5) can then be solved to yield

$$Q(t) = q \, N_t \left[1 - exp\left(-\frac{t}{\tau_c} \right) \right] \tag{7}$$

where

$$Q = q \int_0^{t_{ox}} n_t(x) \; dx \, , \qquad N_t = \int_0^{t_{ox}} N(x) \, dx \, , \qquad and \qquad \tau_c = \left(\frac{J\sigma_c}{q} \right)^{-1} .$$

Equation 7 expresses the simplest of trapping situations where there is only one type of defect with a sufficiently deep trapping level to limit thermal de-trapping and a single cross section, σ_c. For SiO_2 these assumptions have been shown to be valid, with a few exceptions, notably a field dependent capture-cross section[31] and the existence of more than one type of defect[26].

For the case of the high-κ materials, the situation is much more complicated as has been noted by many authors. For example, in ZrO_2 gate dielectrics, Houssa et al.[22,32] found that voltage dependent trap creation was evident and as such Equation (7) was modified to include a term, $\beta(V_g)\, t^{\delta}$ where β is a voltage dependent trap generation rate, V_g is the stress bias and δ is a fitted parameter. Ribes et al., in a review of high-κ reliability[33] suggested that the capture cross section has a dimensional component σ(x). The authors argue that "the transport

probability of carriers changes exponentially with distance", and the time constant $\tau(x)$, from Equation (7), can be written as $\tau_o(x) = \tau_o \exp(\alpha x)$ where α is the transport probability of carrier to reach the trap. Since current continuity demands that J be constant throughout the insulator, at least in steady-state, only the capture cross section could fulfill this spatial component. Likewise Zafar et al.[20,34] found that 1st-order trapping kinetics were insufficient to explain their results on Al_2O_3 and HfO_2. They introduced a "continuous distribution in trapping capture cross sections" and found that this leads to an expression where a threshold voltage shift may be given by

$$\Delta Vt = \frac{qN_t}{C_{ox}}\left\{1 - exp\left[-\left(\frac{J\sigma_0}{q}\right)^{\beta}\right]\right\} \tag{8}$$

where β is a constant that ranges from 0 to 1. In both the aforementioned cases[20,33], the authors were able to fit their measured data, threshold voltage shifts in FETs, as a function of injected charge to these models. However, one might ask is it reasonable to make such assumptions? What would be the physical origins to a spatial variation in the transport properties and does this not violate current continuity in the steady state? Is a continuous distribution of capture cross sections a realistic possibility in these high-κ films? To answer these questions, the origins of trapping theory need to be addressed.

Previously it was stated from 1st-order trapping kinetics that the drift velocity, and by approximation the thermal velocity, controls the transport of carriers through these films. This applies for a barrier limited process, like it is for SiO_2, where Fowler-Nordheim injection controls the injection of electrons, where trapping probabilities are relatively small. Therefore, for SiO_2, transport in the film itself is governed solely by the field and therefore the drift (and therefore, by approximation, the thermal velocity). This does not seem to be the case for the high-κ films. A number of publications have stated that transport tends to be a trap modulated process, i.e. Poole-Frenkel[30] or trap-assisted tunneling[29] and as such the approximation made in Equation 6 above, and used in the previously mentioned models, may not be appropriate. It is likely, given the variable crystallographic nature of these films, that a number of different types of electronically active defects could be present, each with their own trap energy level, E_t, capture cross section, σ_c and trap density, N_t, which may not be uniformly distributed or restricted to the interfacial region, as is normally assumed.

2.2. TRANSIENT CURRENTS: RELAXATION, TRAPPING AND DE-TRAPPING

It is evident from many published works that de-trapping or the transient behavior[33,35-38] of the measured voltage shifts (ΔV_{FB} and/or ΔV_t) also play an important role in understanding the electronic properties of these defects.

The transient nature of the current found within these high-k gate dielectrics may arise from a number of different physical mechanisms. The most basic of these would refer to the dielectric material relaxation resulting from material polarization with the application of an applied electric field. However, in a detailed study of the "relaxation currents" in Al_2O_3 and HfO_2 films, Xu[39] et al. (from the IMEC group) found that the "dielectric material polarization model"[40,41] did not fit the temperature dependence of the current transients they measured. As such, the relaxation currents were attributed to electron trapping and de-trapping in the high-κ dielectric stacks and at its interface with the substrate as opposed to dielectric polarization relaxation. It was further suggested that electron traps were located near the SiO_2/high-κ interface. This assertion was founded on the fact that similar relaxation currents were obtained for gate stacks with the same interfacial layer, but with significantly different high-κ thickness. This assertion that the trapping and de-trapping at the interfacial SiO_x/high-κ ($Al2O_3$ and HfO_2) was also made by other researchers[42] who measured the time response of a gate current in $SiOx/ZrO_2$ films. More recently a fast pulsed technique has been used[35,38] to characterize the transient currents in gate stacks containing high-κ/SiO_x gate films. This technique is discussed below.

2.2.1. *Fast transients: Pulsed V_g with I_{ds}-V_{ds} and ΔV_t*

A pulsed V_g technique[35,38] has been used where the rise and fall times, and or pulse length are varied and the shift in the FET threshold voltage shift, or I_{DS}-V_{DS} characteristic, are recorded for very short times. It was found that some defects have very fast response on the order of ~10^{-6} seconds. As stated previously, this response is likely due to defects found very close to the silicon/high-κ interface that can communicate rapidly with the silicon substrate through a tunneling mechanism. However, a similar fast response may also be the result of very energetically shallow defects distributed deeper within the gate dielectric material.

It should be noted using the ΔV_t or change in I_{DS} as a function of injected charge is similar in nature to using a ΔV_{FB} in C-V measurements in that the shifts are most strongly affected by charge trapped close to the silicon/dielectric interface. It is very difficult to ascertain the distribution of defects, $N_t(x)$, with these techniques. However, these fast, pulsed techniques have been developed to yield a "dynamic analysis of $I_{ds}(V_g)$ hysterisis on high-κ stacks, allowing the

characterization of V_t shift transients at short times" and Leroux et al[38] used this type of measurement, along with a model using Shockley-Reed-Hall (SRH) theory to describe the capture and emission of traps in the high-κ gate stacks. Although this work is likely one, if not the first, to fully model the defects in the stack, a number of assumptions and initial conditions were assumed to fit the model. For example, this type of analysis is useful for distinct and localized defects which may or may not be the case for the materials of interest. Secondly, a constant, energy independent, capture cross section is used for all defects. Finally, it is always difficult, if not impossible, from only a transient analysis alone to determine both the spatial and energetic distributions of the defects; normally another "degree of freedom" i.e. temperature (T) or illumination (hν) is required. As such, the question of trap depth levels and spatial distributions still remains a question of debate.

2.3. WHERE ARE THE DEFECTS: BULK VERSUS INTERFACIAL

Probably the biggest controversy regarding the trapping and de-trapping of electronically active defects, aside the physical origin of these defects, is their location. The aforementioned techniques are unable, without the use of many assumptions, to separate the charge that results from the trapping within the bulk of the insulator from that which occurs due to interface (or near-interfacial) states that occur between the dielectric and silicon substrate. Typically it is argued that the time dependence of transient behavior can be used to make this distinction. However, both a distribution in space as well as energy will yield very similar transients. Using the C-V (ΔV_{FB}) technique or the transient analysis mentioned above, this distinction cannot be made uniquely. Typically to separate the charge associated with interface states, N_{it} (cm^{-2}) or D_{it} (eV^{-1} cm^{-2}) from bulk charge both a capacitance-voltage and current-voltage technique need be used[28] where for the current-voltage technique electrons and/or holes that are injected into the oxide sense the effect the bulk trapped

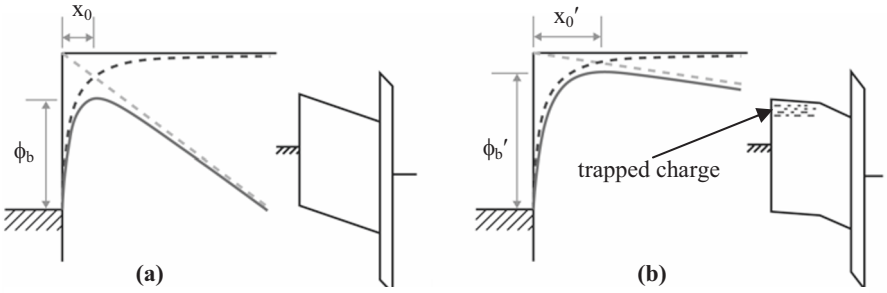


Figure 3. Injection barrier (with image force lowering) and high-κ/SiO_x/Si band diagram prior to (a) and after (b) charge trapping.

charge has on the internal field at the injecting contact. Due to the image force lowering effects at the injection contact/oxide interface, the charge right at the injecting interface is not sensed using an injecting I-V technique. This is demonstrated schematically in Figure 3. In previous work DiMaria and Stasiak[28] showed that for well behaved, energetically deep and localized defects in SiO_2, measuring ΔV_{FB} and both ΔV_g^+ and ΔV_g^- as a function of the injected charge, the density of bulk trapped charge (and it's centroid) and the interface state density can be determined independently. Even though in this work[28] they used FETs, to injected carrier from either an accumulation or inversion layer, similar results can be obtained from capacitors with semi-transparent gates using internal photo-emission to inject the carriers for both voltage polarities. With the use of both the I-V and C-V techniques, a separation of bulk and interface trapped charge can be ascertained.

2.3.1. *The measurement of bulk trapped charge*

As stated previously, the C-V technique is most sensitive to charge located near the substrate but unfortunately does not yield specific information regarding the distribution or centroid of trapped charge. Internal photo-emission[6,7] techniques, including the photo I-V (current-voltage) technique[6,8] can be used for charge centroid locating. This technique uses photons to excite electrons into the gate dielectric from either the substrate or the gate ($\pm V_{gate}$) resulting in a measurable photocurrent. The voltage shifts in the photocurrent response from both gate and substrate injection can then be related to the spatial distribution of the charge within the insulator[43]. The trapped charge shifts the effective barrier height as shown in Figure 3, and as such alters the photo I-V characteristic. Since the measured shifts in the photo current is sensitive to the change in the internal field, and therefore the barrier height at the injecting contact, comparing shifts from gate and substrate injected photo I-Vs, before and after trapping, the centroid of the charge distribution may be ascertained.

The field inside the insulator, not including the image force lowering, can be determined from Poisson's equation and as such the field at the maximum potential, x_0, is given by[43]

$$E(x_0^+) = \left(\frac{V_g^+ - \phi_{ms} - \Psi_s^+}{t_{ox}} \right) + \frac{1}{\varepsilon} \frac{\bar{x}}{t_{ox}} Q - \frac{1}{\varepsilon} \int_{x_0^+}^{t_{ox}} N_t(x) dx \qquad (9b)$$

for x_0 near the metal/oxide interface (gate injection) and

$$E(x_0^-) = \left(\frac{V_g^- - \phi_{ms} - \Psi_s^-}{t_{ox}} \right) - \frac{1}{\varepsilon} \left(1 - \frac{\bar{x}}{t_{ox}} \right) Q + \frac{1}{\varepsilon} \int_0^{x_0^-} N_t(x) dx \qquad (9a)$$

for x_0 near the oxide semiconductor interface (substrate injection) where V_g is the applied gate bias, ϕ_{ms} is the metal/semiconductor work function difference, $N_t(x)$ is the trap charge distribution, Q is the total charge density (the integral of N_t over t_{ox}), t_{ox} is the dielectric thickness, $\bar{x}$ is the charge centroid and ε is the low frequency dielectric constant. Assuming bulk trapping is occurring, the photocurrent will depend on x_0 or more accurately $E(x_0)$ and for a given photocurrent level, the field before and after charging should be identical i.e. $E(x_0)^a = E(x_0)^b$ for $I_{ph}^a = I_{ph}^b$ where superscripts a and b refer to "after" and "before" charging. This should be independent of photo current polarity. If we can assume that there is negligible charging very close to the injecting contact, then the third term in 9(a) and 9(b) goes to zero. Finally, if the band bending has not change significantly during charging then the voltage shifts can be given by

$$\begin{aligned} \Delta V_g^- &= V_g^{-b} - V_g^{-a} = \frac{1}{\varepsilon}\left(t_{ox} - \bar{x}\right)Q \\ \Delta V_g^+ &= V_g^{+b} - V_g^{+a} = -\frac{\bar{x}}{\varepsilon}Q \end{aligned} \tag{10}$$

These equations can be combined and solved for total charge density, Q, and the charge centroid, $\bar{x}$ to yield

$$\begin{aligned} Q &= \frac{\varepsilon}{t_{ox}}\left(\Delta V_g^- - \Delta V_g^+\right) \\ \frac{\bar{x}}{t_{ox}} &= \left(1 - \frac{\Delta V_g^-}{\Delta V_g^+}\right)^{-1} \end{aligned} \tag{11}$$

Table 1. Photo IV shifts & charge centroid as a function of film thickness, stress polarity and photon energy.

	Photon Energy (eV)	Stress Bias (V)	HfO_2 (Å)	ΔV_{gate} (V)	ΔVsub (V)	Centroid (x/t_{ox})
Gate injection	3.4	-1.5	50	-1.19	0.44	0.27
			90	-2.15	0.48	0.18
		-2	90	-2.47	0.63	0.2
				-1.85	0.45	0.2
			115	-1.63	0.38	0.19
	4	-1.5	50	-0.86	0.31	0.27
				-0.62	0.23	0.27
		-1.5		-1.3	0.26	0.17
		-2	90	-1.71	0.36	0.17
				-1.05	0.22	0.17
				-1.16	0.27	0.19
Substrate injection	3.4	2	90	-0.89	0.31	0.26
	4			-0.6	0.24	0.29
				-0.72	0.28	0.28
		2.5		-0.48	0.27	0.36

An example of the use of this photo I-V technique is shown in Figure 4 for a gate stack with a 90/15Å HfO_2/SiO_x. This capacitor had a semitransparent Al-gate (~150 Å) and had an area of 5×10^{-3} cm^2.

For $|V_g| > 1V$, there is a parallel shift in the photo I-V curves to higher biases, for both polarities, ΔV_{gate} and ΔV_{sub}. The shift on the gate injection side, ΔV_{gate}, negative bias, shows a much larger shift than the shift on the positive side suggesting that the defects causing these shifts are distributed closer to the

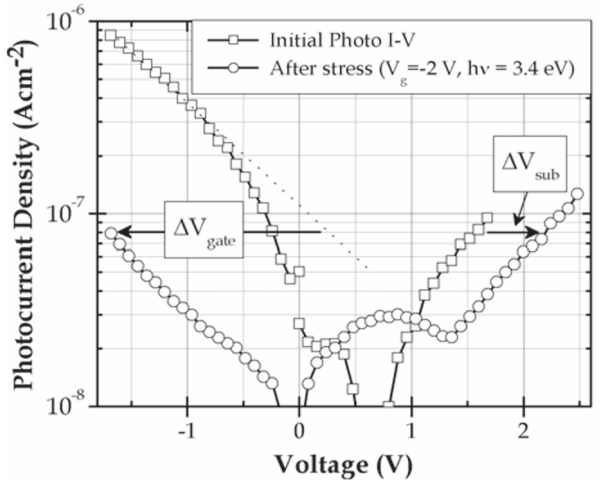
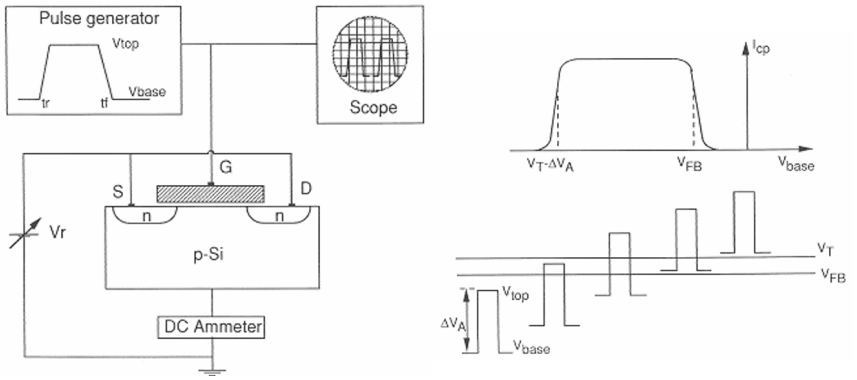


Figure 4. Photo I-V Shifts of a 90Å, HfO_2, Al-gate, 5×10^{-3} cm^2 capacitor.

gate than the substrate. In Table I, a series of calculated centroid are given for various photon energies, bias conditions, and HfO_2 thicknesses. For the gate injection on the 90Å capacitors, the centroid is found to be $\bar{x}/t_{ox}$ = 0.17-0.2 as measured from the gate. This suggests that the charge trapping seen in these measurements occurs close to the gate contact. Similar results are found for the thinner films, t_{ox} ~ 50Å where $\bar{x}/t_{ox}$ ~ 0.27 still suggesting the charge is trapped close to the gate. From these results, the charge seems to be trapped primarily, although perhaps not exclusively, in the bulk of the HfO_2 and at neither the HfO_2/SiO_2 nor the SiO_2/Si interfaces. It may be argued that the charge will be trapped closer to the injecting interface and this is the reason for the centroid appearing close to the gate contact for the gate injection case. However, as can be seen from the data for the substrate injection case, a similar, albeit slightly larger value, is obtained for the charge centroid, still suggesting that the defects or at least the centroid for the defects is located well within the HfO_2 film.

There does not seem to be a large dependence up on the photon energy used to inject the carriers (and measure the photo I-Vs) as both the 3.4 and 4.0 eV results produce similar photo I-V shifts. As such it is arguable that there is little "photo-enhanced" de-trapping which may be a result of either the low photon flux used, or a low photo-ionization cross section for these defects.

Given the previous discussion regarding the appropriateness of assumptions made to analyze the properties of these defects, and their measurement, it is prudent to discuss some of the limitations of the photo I-V technique as well. Firstly, these films do not see the same processing that current technology FETs do, (i.e. temperature cycles etc.) and as such may not be representative of the "best of breed" of the current high-κ materials. Also, the gates of these devices are semitransparent, ~150Å, Al and are likely not as stable as devices fully integrated and capped, although substantial changes in the devices properties over time have not been observed. More importantly, it should be noted that these, like most gate stacks, contain two dielectric films, not one and as such the equations (9)-(11) should be adjusted to reflect the slightly different field conditions one would see at the injection contact for gate and substrate injection. For gate injection the carriers are being injected into the HfO_2 film while for substrate injection they are injected in the interfacial SiO_2 layer (~15Å in this case) and then into the HfO_2 film. The interfacial field, which in the end determines the zero field point, and ultimately the barrier height, will not be, as assumed, identical for gate and substrate injection cases. It is arguable that this will change the effect that the trapped charge will have on the local barrier height. This is probably easiest seen in Equation 10 where the shifts are related to the charge via the dielectric constant, ε. It is assumed in this analysis that ε, especially that close to the injecting contact, is the same independent of the bias



(a) (b)

Figure 5. Charge pumping schematics of (a) measurement apparatus and (b) applied bias pulse and charge pumping current (Icp) for the base level sweep (conventional) technique.

polarity. This is obviously not the case. However, since ε for the positive bias case, i.e. substrate injection, would if anything be smaller than that for gate injection ($\varepsilon_{SiO2} < \varepsilon_{HfO2}$), for a given trapped charge density Q, the value of ΔV^+ would be even larger than that measured. In that case, the centroid would actually be even further away from the HfO_2/SiO_2 interface and even deeper into the HfO_2 film. Therefore, for these films and based upon these photo I-V measurements the trapped charge appears to be trapped in the bulk of the HfO_2 films.

2.3.2. *The measurement of "interfacial" trapped charge*

Charge-pumping using the newer amplitude sweep method (discussed below) and the previously mentioned pulsed I_D–V_G technique have recently been introduced to study fast transient charging effects in alternative gate dielectrics. Kerber et al.[12] have published a very good comparison of these two techniques in the study of charge trapping in SiO_2/HfO_2 gate dielectrics. In this section, with regard to the measurement of interfacial charge, the focus will be on charge pumping and other techniques as the pulsed Id-Vg technique has already been discussed in some detail in section 2.2.

Charge trapping in alternative gate dielectrics is commonly studied using a stress and sense as shown in Figure 1. However, it has been reported that this can underestimate the amount of charge that results from de-trapping during the sense measurement. Recent work from the IMEC group[12,39,44] have shown that using "charge pumping" and the "amplitude sweep" technique information regarding defects that trap and/or de-trap very quickly and are within close proximity to the silicon substrate, can be measured accurately. It is therefore appropriate to discuss, albeit quite briefly, the workings of this "charge

pumping" technique. In 1969, charge pumping was first reported by Brugler and Jespers[45]. They reported that, when applying periodic pulses to the gate of a FET, with the source and drain grounded, a net current was measured at the substrate. This current was found to be proportional to the frequency of the pulses and to the gate area. They referred to this current as a charge pumping current as it originated from the recombination of majority and minority carriers through defects at the Si/SiO_2 interface. A schematic for the apparatus of a typical charge pumping measurements is shown in Figure 5(a)[46]. When the gate is pulsed between inversion and accumulation conditions; i.e. above V_t and below V_{FB} a charge pumping current can be measured at the substrate that flows in the opposite direction of the normal drain and source to substrate leakage currents. When an nFET is pulsed into inversion, electrons flow from the source and drain regions into the channel region where a fraction of them are captured by the interface traps. When the surface is driven back into accumulation, the channel electrons drift back to the source and drain, but the trapped charge recombines with the majority carriers. This yields a flow of negative charge into the substrate that can be given by

$$I_{CP} = fQ_{CP} = f\ q\ A_G\ \overline{D}_{it}\ \Delta E \tag{13}$$

where q is the electron charge, A_G is the channel area of the transistor (cm^{-2}), $D_{it}(E)$ is the interface trap density at energy level E(cm^{-2} eV^{-1}) and E_f^{Inv} and $E_f^{Acc.}$ are the Fermi level positions in inversion and accumulation, respectively. For a series of repetitive pulses at a frequency, *f*, the charge recombining through the defects will give rise to a steady state current given by

$$I_{CP} = q\ A_G \int_{E_f^{Acc.}}^{E_f^{Inv.}} D_{it}(E)\, dE \tag{12}$$

Therefore, using a pulse of constant magnitude, sufficient enough to drive the FET from inversion ($<V_t$) to accumulation ($>V_{FB}$), and "moving" the pulse through the silicon gap I_{CP} can be measured as is demonstrated schematically in the "Base Level Sweep" shown in Figure 5(b) demonstrating the 5 basic regions of operation. By plotting I_{CP} as a function of the base level voltage of the pulse, a curve is obtained where the rising edge of the curve occurs at V_t-ΔV_A, the falling edge at V_{FB} and the saturation I_{CP} level is given by Equation 13 above. To first order, a change in the saturated I_{CP} level is indicative of interface state density while changes in the edge are indicative of charge that is trapped in the bulk of the film; in other words affecting the V_t and/or V_{FB} as it would for other charge sensing techniques.

However, it has been suggested[12] that conventional charge pumping measurements[46], where the base level of the gate pulse is swept from

accumulation to inversion, as in Figure 5(b)[46], provide poor control over the charge exchange while the amplitude sweep technique, as shown in Figure 6, results in complete de-trapping throughout the entire sweep range. Therefore, trapped electrons that are emitted from within the HfO_2 layer into the substrate will be able to also recombine with majority carriers and contribute to the substrate current and as such that the oxide charge can be measured.

Although great care with regard to the details of the charge pumping parameters, (i.e. rise and fall times, base and peak voltage levels, frequency etc.) was required, Kerber et al.[12] give a convincing argument that at least some knowledge of the interfacial and near-interfacial trap densities may be ascertained. However, a true distinction between energetic trap depth (or distribution) and the spatial positioning of the defects still remains illusive.

Jasckik et al[47] in a recent publication, further speculated that the trapped charge profile could be determined using charge pumping in Al_2O_3 films. In this work, they used more or less conventional base level sweep measurements with varying frequency and rise and fall time. However, their analysis once again required speculation about the nature of the defects in this case and spatial dependent capture cross section.

It is not surprising, that for either (or both) charge pumping or pulsed I_D–V_G techniques, with a well qualified time base (i.e. frequencies, rise and fall times) the charging transients associated with interfacial and near-interfacial charge can be measured. In fact substantial information can be acquired to allow for process, and device optimization. However if it is the spatial and/or energetic distributions of these defects that is of concern, neither of these techniques can independently determine this information. In all of the techniques mentioned above, some assumption was required whether that was to fix the defect energy level and/or position or an assumption regarding their capture cross sections. As such, the search continues for a better understanding of the electronic nature of these defects.

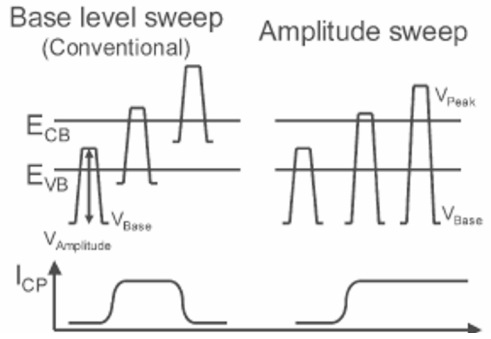


Figure 6. Charge pumping schematics applied bias pulse and charge pumping current (Icp) for the "base level sweep" (conventional) and amplitude "sweep" techniques.

3. Summary

A review of first-order trapping kinetics, especially with respect to high-κ gate dielectrics suggests that, due to the nature of a proposed trap modulated transport in high-κ gate dielectrics, the adaptation of this theory, used historically for SiO_2, may not be applicable without significant revision. However, the measurement techniques using the standard "stress and sense" methodology, where charge is injected into the film and the effects of the charge trapping are measured with either capacitance-voltage (ΔV_{FB}) and/or current-voltage (ΔV_t) to measure the effects of the charge trapping may still be applicable if reasonable assumptions (an appropriate measurements) can be made.

Data from HfO_2 using electron injection via internal photo-emission and charge centroid extraction using the "photo I-V" technique suggests that centroid of the trapped charge is within the bulk of the high-κ film independent of bias polarity and phone energy although other techniques involving transient current analysis using charge pumping in both "conventional base sweep" and "amplitude sweep" and pulsed I_{DS}-V_G suggest that the charge trapping is interfacial and/or near-interfacial.

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INELASTIC ELECTRON TUNNELLING SPECTROSCOPY (IETS) STUDY OF HIGH-K DIELECTRICS

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Abstract. Inelastic electron tunnelling spectroscopy (IETS) will be shown to be a simple and powerful technique 1 to study microstructures and defects in Metal-Insulator-Semiconductor (MIS) systems where the insulator is sufficiently thin to allow significant tunnelling current to flow through. The information that may be revealed by IETS arises from a wide variety of inelastic interactions, including interactions with phonons, various bonding vibrations, bonding defects, and impurities.

Keywords: Electron tunnelling high-k dielectrics, spectroscopy, phonons, vibrational modes, traps.

1. Introduction

High-K dielectrics are being actively pursued as a replacement for SiO_2 as the gate dielectric for future CMOS technology, but numerous issues, such as thermal instability, high densities of oxide charge and traps, and low channel mobility, must be resolved before any of them can be implemented[1]. It is very

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important to be able to have effective characterization techniques to probe the underlying mechanisms behind these challenging issues. A promising technique is inelastic electron tunnelling spectroscopy (IETS)[2-5], which probes the MOS structure by detecting the interaction between the tunnelling electrons and the energy-loss modes caused by lattice vibrations (phonons), impurities, and defects in the gate dielectrics.

The basic principle of the IETS technique is illustrated in Fig.1(a) where one can see that, without any inelastic interaction, the I-V characteristic is a smooth curve, and its 2nd derivative is zero. When the applied voltage causes the Fermi-level separation to be equal to the characteristic interaction energy of an inelastic energy loss event for the tunnelling electron (see the 2nd band diagram in Fig. 1a), then an additional conduction channel (due to inelastic tunnelling) is established, causing the slop of the I-V characteristic to increase at that voltage, and a peak in its 2nd derivative plot, where the voltage location of the peak corresponds to the characteristic energy of the inelastic interaction, and the area under the peak is proportional to the strength of the interaction.

In a typical MOS sample, there are numerous inelastic modes, as a wide variety of inelastic interactions may take place, including interactions with phonons, various bonding vibrations, bonding defects, and impurities. Therefore, Fig. 1(b) is shown to represent the typical IETS spectrum that one expects to see.

Spatial information about where the inelastic interactions occur can be revealed by considering the asymmetry of the dielectric barrier caused by the voltage bias. Qualitatively, the electrons tunnel into the barrier and interact with a mode near the negatively biased electrode (i.e., near the "emitter" electrode) will

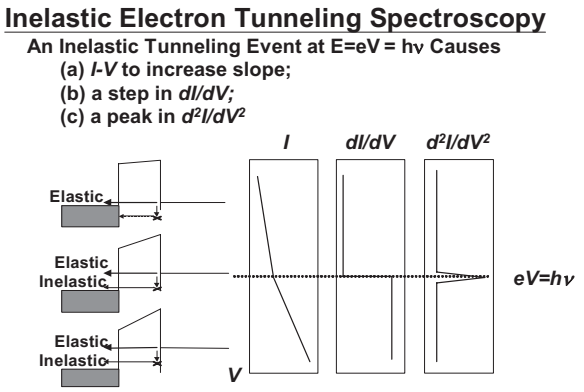
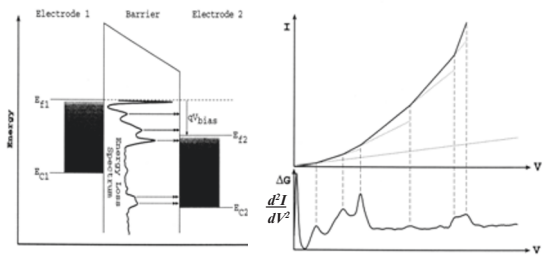


Figure 1(a). Inelastic interaction causes a slope increase of I-V, a step in dI/dV, and a peak in 2nd derivative, all occurring at the voltage corresponding to the characteristic energy.

effectively experience a higher energy barrier than those electrons interacting with same mode near the positively biased electrode (i.e., near the "collector" electrode). This is because the former electrons lose some energy shortly after they enter the barrier by the inelastic interaction, and the barrier height for those

Various Inelastic Modes in the Barrier (Left)
May Be Reflected in IETS (Bottom Right)



IETS probes phonons, bonding vibrations, impurities, and Traps

Figure 1(b). Typical IETS spectrum (lower right curve) reveals the various inelastic modes depicted in the energy diagram on the left.

electrons is effectively increased from that point forward. In contrast, the latter electrons only experience an increased barrier height through a small portion of their journey. Thus IETS can be used to probe features near either one interface or the other by switching the polarity of the voltage bias.

In this study, each IETS spectrum (proportional to the second derivative of the I-V characteristic) was measured at liquid helium temperature (4.2K) with the standard lock-in method[2]. The modulation voltage of the excitation signal for the measurements was 2 mV. A dual temperature (4.2K, 77K) technique was used to remove the elastic tunnelling background [2]. The MOS capacitors in this study were fabricated on N-type, (100) silicon substrate. Degenerate silicon wafers were used to ensure conduction at the liquid He temperature (4.2K) used during the IETS measurement. The HfO_2 and HfAlO layers under investigation were deposited by the Jet Vapor Deposition (JVD) technique at room temperature [6]. As a reference, we also made samples with thermal SiO_2 layer grown in dry O_2 at 700°C for 5 min.

2. IETS of SiO_2/Si

Figure 2 shows the IETS spectra of a sample with thermal SiO_2 tunnel barrier measured under a forward bias (gate positive). The relatively strong peaks at 18, 48, 59 mV correspond to acoustic and optical phonon modes of crystalline

silicon. The broad feature centered around 145 mV is consistent with the asymmetric stretching vibration modes of SiO_2. The broadness of the feature reveals the presence of disorder in the thin layer of amorphous SiO_2 and possible non-stoichiometry of the transition region between SiO_2 and the silicon substrate. The broad peak around 105 mV coincides with the symmetric stretching vibration mode of SiO_2, and a mode of Si-H as well. The aforementioned results are in excellent agreement with previous IETS spectra [2-5] and infrared spectroscopy[7] analysis, as noted in the references.

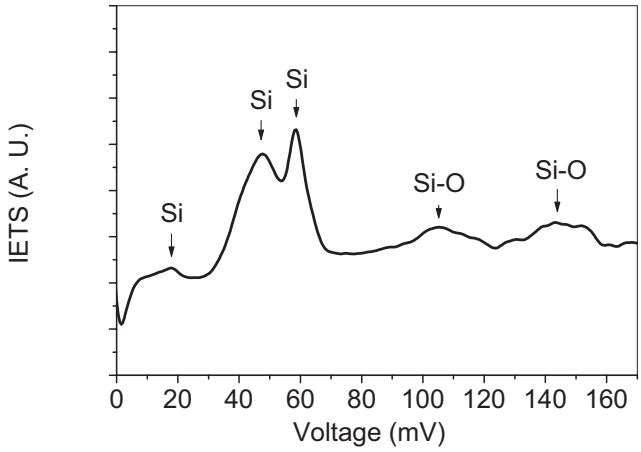


Figure 2. IETS for thermal SiO_2 on Si, with Al gate electrode.

3. IETS of HfO_2/Si

Figure 3 shows the forward and reverse biased IETS spectra of a JVD HfO_2. We first look at the forward-biased spectrum. As expected, the silicon phonon modes show up at 18, 48 and 59 mV in the spectrum. The peaks at 33mV, 70mV and 83 mV are attributed to the vibration modes of Hf-O bond. The energy levels of these peaks are consistent with the results for crystalline HfO_2 from Raman spectroscopy [8,9]. This agrees with the observed crystallization of HfO_2 upon 600 ^oC annealing in previous work [13]. The peak at 137mV in the forward-biased spectrum is attributed to the Hf-O-Si bond [10,11]. Now we look at the reverse-biased spectrum. The peak at about 155 mV is attributed to the vibration mode of the Si-O bond in the dielectrics.. The presence of the Si-O modes suggests that the 600 ^oC anneal causes SiO_2 growth. Note that there is significant difference between the forward-biased and reverse-biased spectra. Since the forward-bias signal tends to couple much more strongly with the dielectric/top electrode interface, while the reverse-bias one tends to couple much more

strongly with the dielectric/substrate interface[12], the spectra in Fig.3 further indicate significantly different microstructure near the aluminum electrode interface than that near the silicon substrate interface. Our forward-biased data clearly reveal the Hf-O bonds without much trace of the Si-O bonds, while our reverse-biased data show primarily Si-O bonds and Hf-O-Si bonds. These results suggest that the aluminum electrode interface is more HfO_2-like, while the silicon substrate interface is more SiO_2-like.

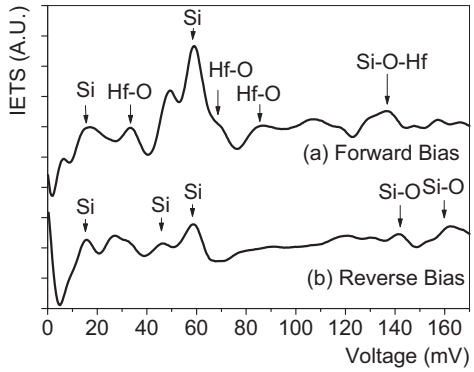


Figure 3. IETS for HfO_2 on Si under different bias polarities. (a) Forward bias (gate electrode positive), (b) Reverse bias (gate electrode negative).

Figure 4 shows the forward and reverse biased IETS spectra of an aluminum doped JVD HfO_2 (HfAlO). The atomic aluminum concentration relative to Hf is estimated to be 30%. In addition to the features identified in Fig. 3, there is a peak at 118 mV, which is attributed to the Al-O bond [13]. The presence of the Al-O mode in both Fig. 3 and Fig. 4 suggests that the aluminum gate reacts with the

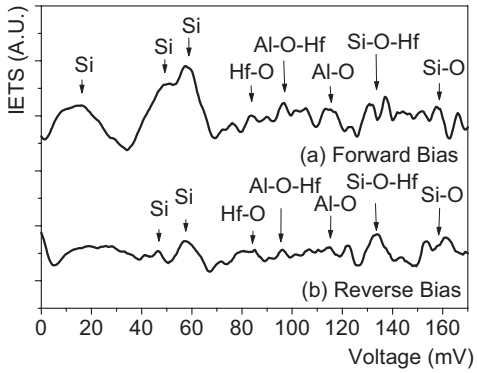


Figure 4. IETS for Al-doped HfO_2 (HfAlO) on Si under different bias polarities. (a) Forward bias (gate electrode positive), (b) Reverse bias (gate electrode negative).

dielectric during or after the aluminum thermal evaporation. The stronger presence of the Al-O mode in Fig. 4 is attributable to the deliberate addition of Al in the film. Based on infrared and Raman spectroscopy results, we attribute the peak at 95 mV to the vibration mode of the Al-O-Hf [14,15], and the feature around 83 mV to Hf-O. The absence of other Hf-O modes might be associated with the fact that the HfAlO stays in the amorphous phase after the 600 ^{o}C anneal, as a result of Al doping[16]. The broad Hf-O features associated with amorphous HfAlO are hard to resolve in IETS.

It should be noted that in both Fig. 3 and Fig. 4 there are some unidentified features. While some of them might be associated with intrinsic bonding structures yet to be determined, we believe that some are caused by the trapping/de-trapping of tunnelled electrons[17,18] due to bonding defects or impurities. The use of IETS to study traps in the gate dielectric is presented next.

4. Traps in IETS

It is well known that traps in the gate dielectric can cause at least two different kinds of adverse effects in a MOSFET: (1) trapping of carriers, which causes shifts in the threshold voltage, and (2) trap-assisted conduction, which causes increased leakage current. Figure 5 illustrates the basic difference between the aforementioned trap effects in I-V and d^2I/dV^2 - V plots. Curve (1) in Figure 5(a) shows that the I-V curve will show an increase in slope over a small range of voltage when trap-assisted conduction mechanism takes place, where the voltage at which this occurs corresponds to the condition when the tunnelling electrons have sufficient energy to tunnel into the trap, and the width of this region corresponds to the energy spread of this particular trap, including thermal spread.

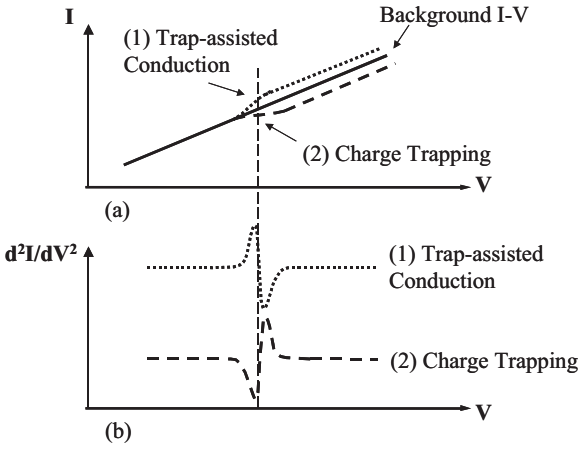


Figure 5. Illustration of two kinds of trap effects on (a) I-V, and (b) d^2I/dV^2 –V characteristics. In each case, Curve (1) represents trap-assisted conduction, and Curve (2) represents carrier trapping.

Curve (2) in Figure 5(a) shows that charge trapping effect causes a small horizontal plateau, where the width of the plateau is proportional to the trapped charge ($\Delta V = qN_t/C_{ox}$, where q is the electron charge, N_t is the areal trap density, and C_{ox} is the gate dielectric capacitance). Note that this effect is analogous to the well-known C-V shift due to charge trapping. Figure 5(b) shows the corresponding second derivative of the I-V curve; specifically, the second derivative will show a peak-followed-by-a-valley for the trap-assisted conduction mechanism (Curve 1), while a valley-followed-by-a-peak for the charge trapping mechanism (Curve 2).

In contrast to the inelastic interactions involving phonons and other bonding vibrations, the trap-assisted tunnelling process is an elastic process, and thus, strictly speaking, IETS is not an appropriate nomenclature for the trap related features. However, in this paper we will still use IETS to describe the spectra associated with traps, because the trap features are revealed in the same measurement procedure for IETS.

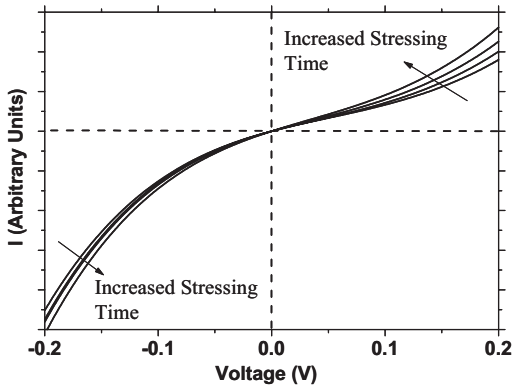


Figure 6. Current-Voltage (I-V) characteristics of a HfO_2 MOS capacitor before and after a series of constant-voltage stress at 1.2V for 200, 400, and 800 seconds.

The next two figures connect the stress-induced-leakage current (SILC) [19] with traps observed in IETS. Figure 6 shows the room temperature current-voltage curves of an Al-HfO_2-Si capacitor before and after a series of constant-voltage stresses at 1.2V at room temperature. It is apparent that the current increases noticeably as the stressing time increases. This is the SILC phenomenon that's often observed for ultra-thin gate dielectrics[19], and is believed to be related to the build-up of traps in the gate dielectric.

Figure 7 shows the corresponding IETS spectra of the device discussed above, where curve (a) was taken before the stress, and the most prominent peak at 58 mV corresponds to Si phonon vibration; other features are relatively weak, but if sufficiently amplified we could identify possible Hf-O vibration at about

80 mV, Hf-O-Si and Si-O vibration modes from 130mV to 160mV, and possible hydrogen-bonds related vibration modes at about 110mV and 255mV [2-4]. Curve (b) in Fig.7 was taken after constant-voltage stress at 1.2V for 200 seconds. Many additional features appear between 130 and 300 mV, indicating electrical stress-induced build-up of defects. Curve (c) in Fig.7 was taken after constant-voltage stress for 800 seconds, and one can see a dramatic increase in magnitude of the features between 160 and 200 mV, and between 250 mV and 290 mV. It seems that both kinds of trap effects as depicted in Fig.5 are found in Curve (c), where the feature marked (1) may be attributed to trap-assisted conduction, the feature marked (2) may be associated to trapping, while that marked (3) may also be associated with trapping. Similarly, the features between 250 mV and 290 mV also appear to contain both kinds of traps.

Next, we will demonstrate the use of IETS to determine the locations and energy levels of traps in ultra-thin gate dielectrics.

Figure 8 shows the ETS spectrum of an Al/HfO_2/Si structure where prominent trap-assisted features are revealed in both forward and reversed-bias spectrum. From such a spectrum, the energy level and the physical location of the corresponding trap in the gate dielectric can be estimated, as described below. It should be noted that the fact that the feature in the positive-bias region is much stronger than its negative-bias counterpart is due to the asymmetry of the tunnel barrier, which gives rise to a much higher tunnelling probability in the positive-bias region.

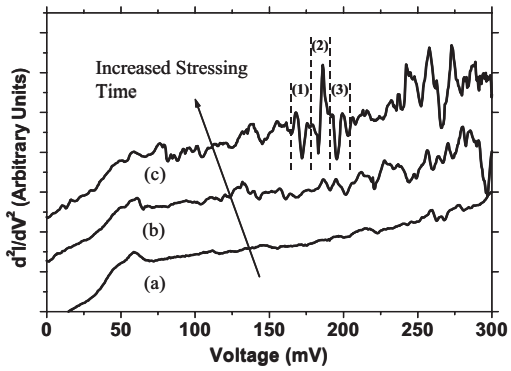


Figure 7. IETS Spectra for HfO_2-gated MOS capacitor (a) before stress, (b) after 200 seconds of constant-voltage stress at 1.2 V, and (c) after 800 seconds of constant- voltage stress at 1.2 V. Three trap-related features are highlighted on Curve (c).

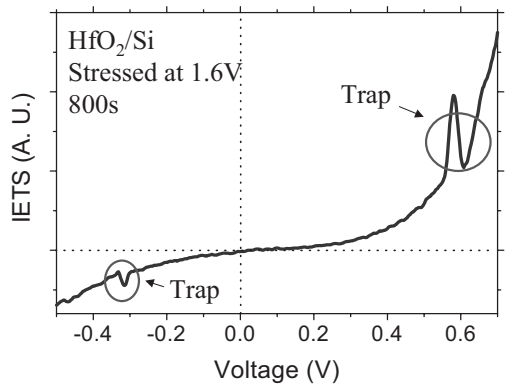


Figure 8. An ETS spectrum (2nd derivative of the tunneling I-V characteristic) of an MOS (Metal-Oxide-Silicon) structure with HfO_2 as the dielectric. Two strong trap related features appear at ~580mV in the forward-bias range and ~320mV in the reverse-bias region.

Figure 9 (a) shows the schematic of a tunnel dielectric sandwiched between two electrodes (made of metal or semiconductor) with zero bias voltage, where the Fermi energies of electrodes 1 and 2 are at the same level. The total physical thickness of the dielectric is x_0. Assume a non-uniform dielectric constant, $\varepsilon = \varepsilon(x)$, and a trap is located at x_t from the electrode-1 interface, with an energy level at eV_t, defined as the energy above the Fermi levels of the electrodes at zero bias. As the applied voltage reaches V_f, the Fermi level of the negative-biased electrode (electrode-2) reaches the energy level of the trap, as shown in Fig. 9 (b), and trap-assisted tunnelling will start to take place. Considering the electric field across the dielectric, V_f can be expressed as:

$$V_f = \int_0^{x_0} dx D_f/\varepsilon(x) \tag{1}$$

where D_f is the electric displacement, defines as the electric field E_f times the dielectric constant ε. On the other hand, V_f can be written as:

$$V_f = V_t + \int_0^{x_t} dx D_f/\varepsilon(x) \tag{2}$$

Similarly, for a reverse bias (with electrode-2 positive) of V_r, the Fermi level of the negatively biased electrode (electrod-1) reaches the energy level of the trap, as shown in Fig. 9(c), and one can write:

$$V_r = \int_0^{x_0} dx D_r/\varepsilon(x) \tag{3}$$

and

$$V_r = V_t + \int_{x_t}^{x_0} dx D_r/\varepsilon(x) \tag{4}$$

Solving Eqs. (1) – (4) by cancelling out D_f and D_r, one has the trap energy level expressed as:

$$V_t = V_f V_r /(V_f + V_r) \quad (5)$$

and the physical location of the trap expressed as:

$$d_t = d_0 V_f /(V_f + V_r) \quad (6)$$

where $d_0 = \int_0^{x_0} dx/\varepsilon(x)$ is the electrical effective thickness of the dielectric, and $d_t = \int_0^{x_t} dx/\varepsilon(x)$ is the electrical effective distance. Equations (5) and (6) imply that, by recording trap-assisted tunnelling features in both bias polarities of the ETS spectrum, one can calculate the energy level and its physical location of the trap that causes the related ETS feature.

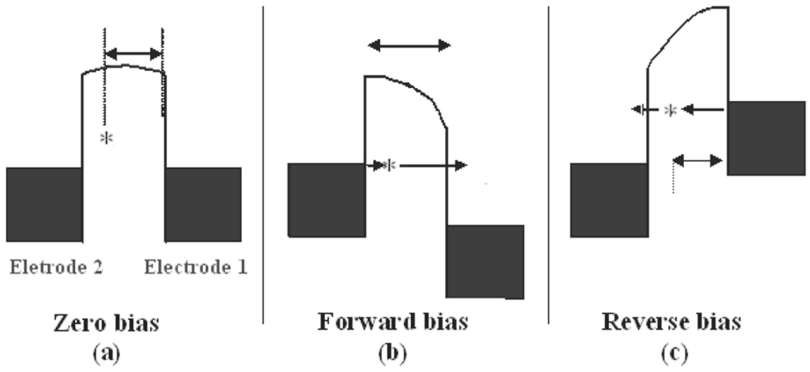


Figure 9. A tunnel dielectric surrounded by two electrodes: (a) with 0 bias voltage, (b) with a forward bias V_f such that the trap energy coincides with the Fermi level of the left electrode, (c) with a reverse bias V_r such that the trap energy coincides with the Fermi level of the right electrode.

Using the equations shown above, we estimate the trap energy level associated with the features in Fig. 8 to be about 0.2 eV above the Fermi level at zero bias. The physical location of the traps is estimated to be ~1nm from the silicon substrate, which is in close proximity to the interface between the HfO_2 and the interfacial oxide near the silicon substrate.

Figure 10 shows the IETS spectra of an Al-HfO_2-Si capacitor before and after a series of constant voltage stresses at 1.6V at room temperature. Using the method mentioned above, we are able to track the evolution of the traps during the constant voltage stress. Figure 11 shows the change of the trap energy and location (i.e., the electrical effective distance to the substrate/oxide interface, d_0-d_t) in the sample discussed above during the constant voltage stress. It is apparent that the location of this trap moves slightly toward the substrate/oxide interface during the electrical stress while the energy level of the trap remains almost unchanged.

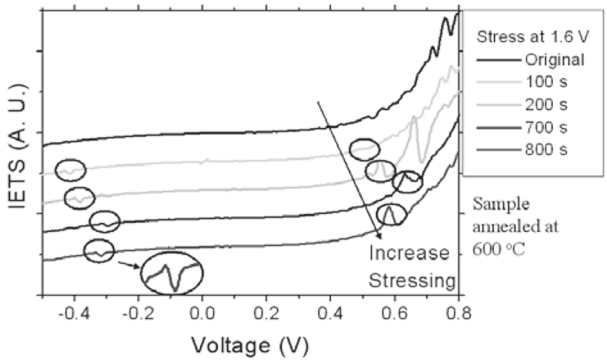


Figure 10. Evolution of the trap features in an ETS spectrum for an Al/ HfO2/ Si capacitor.

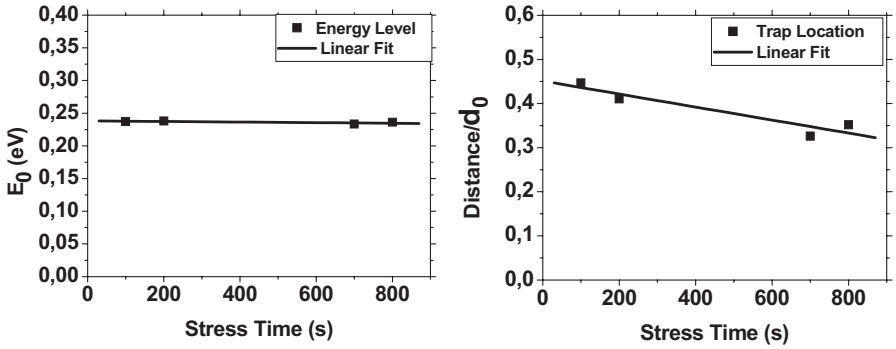


Figure 11. Calculated (a) trap energy, and (b) trap location as functions of stress time based on the data shown in Fig.3.

5. Summary

In summary, we have applied IETS to study MIS capacitors with ultra-thin gate dielectrics. The IETS spectra that we have obtained have revealed valuable information about microscopic bonding structures and chemical compositions of these high-k gate dielectrics. We have also applied the IETS technique to study electrically-active traps in ultra-thin gate dielectrics. We have shown that the IETS technique enables the identification of two different kinds of trap effects, that of carrier trapping and that of trap-assisted conduction, and it also allows the determination of the energy level as well as its spatial location of a trap. These

capabilities are very useful for studying the microscopic origins of these traps, which are not available with conventional techniques.

Acknowledgements

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CHARACTERIZATION AND MODELING OF DEFECTS IN HIGH-K LAYERS THROUGH FAST ELECTRICAL TRANSIENT MEASUREMENTS

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Abstract. An original dynamic analysis technique allows the characterization of V_T shift transients for full time range. Extensive data set versus voltage, time, temperature and operating mode is shown to fit with direct tunnel trapping-de-trapping. A model is presented explaining all the dynamic behaviors and leading to the trap characteristics and profiles inside the high-κ layer. The question of uniqueness of the trap profile determination is addressed by simulation of other possible trap profile responses.

Keywords: Hafnium oxide; HfO_2; high-k dielectric; threshold voltage instability; hysteresis; trap modeling

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1. Introduction

Hafnium-based dielectrics are major potential candidates for the nitrided silicon replacement for future CMOS technologies [1-3]. However, significant issues remain to overcome as the mobility degradation, the metal gate potential compatibility, and threshold voltage instabilities [4-6]. These aspects are all more or less related to defects, traps or charges inside the high-κ layers and it becomes important to improve our understanding of these defects. One of the major sources of threshold voltage instabilities is the hysteresis phenomena [7]. This paper will present in the second paragraph a recently developed experimental method which leads to extensive data set of threshold voltage variations versus applied voltage, time, temperature and various operating modes. It is shown why the observed data can be explained by a direct tunneling trapping/de-trapping mechanism. A possible modeling of the mechanisms is then presented in the third paragraph. This model addresses both static and dynamic responses of the devices. The profiles and physical characteristics of the traps are extracted for all the studied stacks. These results are then discussed in detailed as it is important to give a ruling about the uniqueness question of this trap profile determination. For that, several other possible trap profiles and physical characteristics are studied by simulation and their typical responses compared to experimental results.

2. Experimental data and physical mechanism

2.1. EXPERIMENT

Measurements have been performed on four stacks [3]: two ALD-HfO_2 thicknesses (3 and 4.5 nm) were deposited on a 0.7 nm oxide and annealed (PDA) under N2 ambient at 600° C or 800° CThe final equivalent interfacial oxide thicknesses were 0.8 nm (600° C) andl nm (800° C). The gate electrode is CVD TiN capped with polySi. Devices had low Dit and good reliability [3].

Hysteresis phenomena is studied by a recently proposed time resolved measurement technique allowing characterization of I_d transients and V_T shifts from short times to long times [8]. A key point is the use of a fast I-V converter which allows measurements down to a few μs after the pulse set. For this minimum time no trapping occurs for our devices and the corresponding currents and V_T are taken as a no-trapping-reference. Notice that devices with thinner interfacial oxides would need faster measurements to get the no-trapping-reference. This can be done by a commercial faster I-V converter.

Typical V_T shift variations for charging and discharging are given respectively in Fig.1 and Fig.2. For both conditions, charging and discharging extend over more than six decades of time. For time over 1s, a steady state condition is obtained. The discharging study is performed from a charge level Vg_{max} to a lower discharge level Vg_{min}. Varying these two values allows a spectroscopy of the traps energies and may help to identify various trap behaviors.

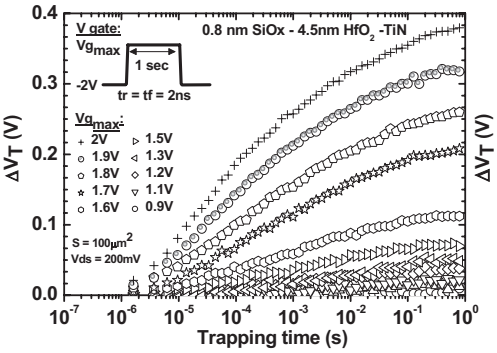


Figure 1. Typical V_T shifts versus trapping time. Pulses with different bias are applied. Each point is obtained from I_d current transients sampling at specific times.

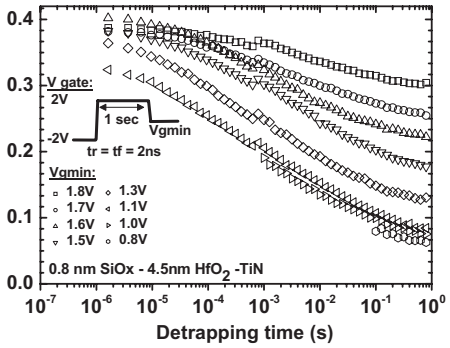


Figure 2. Typical V_T shifts decrease versus de-trapping time. Traps are filled during 1s at 2V. Various de-trapping levels Vg_{min} are studied. De-trapping process are sampled up to 1s.

2.2. TOWARD DIRECT TUNNEL TRAPPING MECHANISM

A trapping efficiency versus injected charge Ninj can be estimated from the previous ΔV_T versus time measurements (Fig.3) [9]. Ninj is calculated by multiplying the static gate current by time. This trapping efficiency appears clearly much higher than unity at small injected charges. This indicates that the gate current does not control the trapping for such devices with thin high-κ stacks, contrary to what was observed on thicker stacks. For interfacial SiO_2 thickness around the nanometer, trapping/de-trapping mechanism by tunneling from the substrate must be considered. The trapping and de-trapping processes are then modeled using a trap-like approach already proposed for non volatile memories [10]. Trapping /de-trapping will be described by Shockley-Read-Hall (SRH) statistics modulated by a tunnel transparency between silicon and traps.

Further evidences for this model are the measurements of trapping and de-trapping versus temperature. Literature data may present hysteresis data significantly increasing with T. However, plotting charging versus V_g-V_T, i.e. looking at the same traps in the gap, shows T independent results for usual operating conditions (weak V_g-V_T and T up to 400K) (Fig.4). This is fully

consistent with tunnel-SRH model once supposed that capture cross section weakly varies with T [11-13]. In the case of higher T and higher electric fields E, ΔV_T decreases due to limitations for the trapping mechanisms, activated by electric field and temperature but yet not fully identified. The synthesis of the mechanisms as understood yet are described Fig.5.

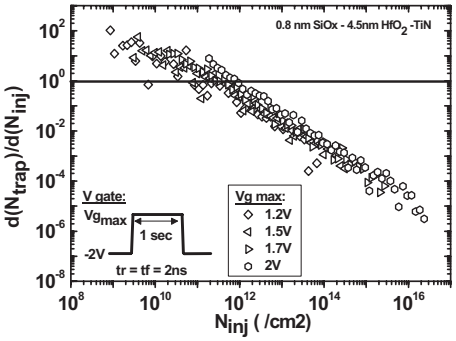


Figure 3. Trapping probability versus injected charge at various gate biases. Trapped charge is here supposed at $SiOx/HfO_2$ interface.

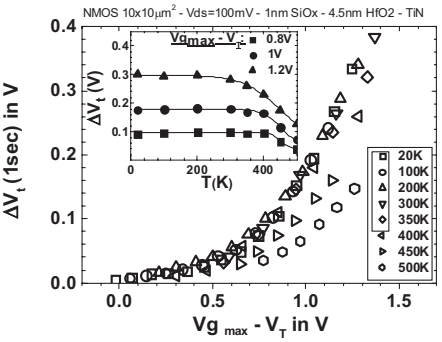


Figure 4. Evolution of maximum hysteresis at various temperatures with V_T correction.

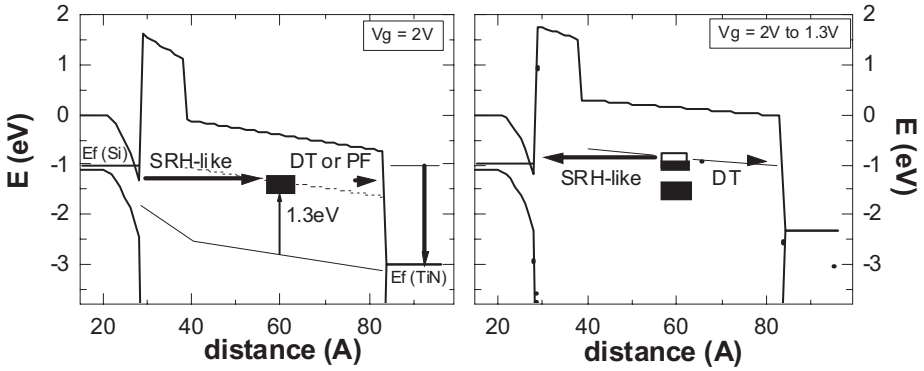


Figure 5. Exact energy band diagram for trapping and de-trapping experiments; case 4.5 nm HfO_2, 600° C N. (a) trapping at Vg=2V ; (b) De-trapping from Vg= 2V to 1.3V. Plain arrows: mechanisms physically identified; dashed arrows: mechanisms supposed but still controversial.

Trapping kinetic is shown temperature independent. This is true from low to medium temperature range (Fig.6) but also at high temperatures (Fig.7) even if, in this case, the final charging level decreases as already discussed. Moreover, as we consider the de-trapping kinetics by normalizing ΔV_T to its initial and final values (Fig.8), they appear also temperature independent. All these data are very consistent with the tunnel-SRH model.

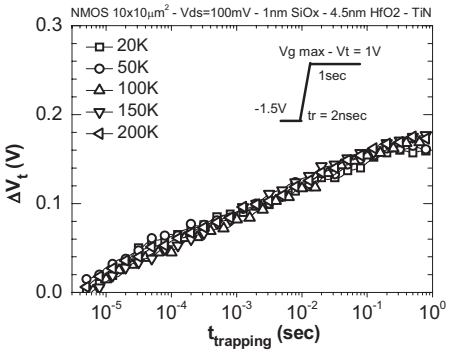


Figure 6. Trapping kinetics at low temperatures at Vg_{max}-V_T= 1V.

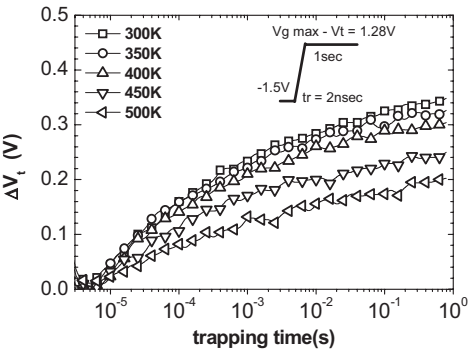


Figure 7. Trapping kinetics above 300K at Vg_{max}-V_T= 1.3 V.

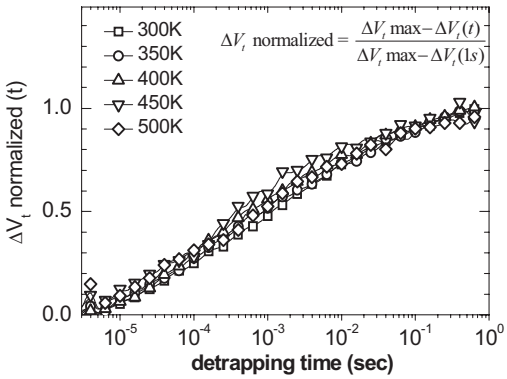


Figure 8. Normalized de-trapping V_T shift evidencing similar kinetic.

3. Traps modeling

3.1. TRAPS MODELING AND PROFILE EXTRACTION

3.1.1. *Model and trends*

For a given energy level E_t, we consider that the trap filling probability at equilibrium is determined by its position relatively to the substrate Fermi level E_F. Its evolution with time follows a Shockley-Read-Hall statistic [14] described by equation (1). The originality of this model is that capture probabilities for electrons c_n (equation 2) and for holes c_p are modulated by the tunnel transparency between silicon and traps. Electron capture probability also depends on the trap capture cross section (σ_n), interface electron density (n_s)

and thermal velocity v_{th}. Emission probabilities e_n and e_p are determined from equilibrium conditions.

$$\frac{df_t}{dt} = e_p + c_n - (e_n + c_n + e_p + c_p).f_t \quad (1)$$

$$c_n = \sigma_n.v_{th}.n_s.T_n \quad (2)$$

Emission probabilities e_n and e_p are determined from equilibrium conditions for which $f_{t,equil}$ equals $1/(1+\exp((E_t-E_F)/kT))$. It leads then to the relationship between e_n and c_n, $e_n=c_n\exp((E_t-E_F)/kT)$. Two de-trapping mechanisms are possible, electron emission e_n for E_c interaction, hole capture for E_v interaction.

The model also includes quantum effects. It allows the calculation of the carrier capture and emission times by traps located at a given position in space and energy. According to this mechanism, an exponential dependence of the time constants with trap distance from Si/SiO_2 is obtained, explaining the observed distribution of time constants. Equations can be solved versus V_g and t with any trap distribution. Results are then compared with experiments and a suitable fitting methodology leads to traps profiles and physical parameters. Actually typically the time response leads to the trap spatial position while the Vg response leads to the traps energy.

3.1.2. *Extracted profiles and full modeling*

In this part, modeling is performed on the hypothesis of simple and realistic traps characteristics. These characteristics are the following: (a) trap distribution inside the volume of the high-κ material in order to account for the time constants distribution, (b) one main kind of trap due to material structure, i.e. one energy level and one σ for the whole material; however as will be seen later, other bands of traps are necessary to explain all the results.

With these hypotheses, the self-consistent solving of the equation giving the potential in the gate stack and the trap filling probability equation (1) leads to simulations of V_T shifts with time, which account reasonably well to the obtained experimental results (Fig.9). For a given process, the modeling parameters fit the full set of charging conditions (Vg, time) but are also in good agreement with the discharging conditions (compare Fig.10 and Fig.2). The extracted trap profiles included in the simulations are presented Fig.11. The spatial profiles come from $\Delta V_T(t)$ de-convolution while Et is related to the $\Delta V_T(Vg)$ dependence.

Two bands of traps are necessary to explain the full set of results. The first band is ~1.3 eV over Ei_{Si}, Ei_{Si} being the equivalent energy of the midgap in silicon (see insert of Fig.11). The second band has a lower density and is deeper in energy, around Ei_{Si}+0.8eV. This band is necessary to model the ΔV_T

response at low Vg (Fig.9). Notice that the kinetic is correctly fitted using a common $\sigma \sim 10^{-16}/\varepsilon r^2$, the term $1/\varepsilon r^2$ allowing comparison with trap cross sections in other dielectrics.

Figure 11 shows that trap densities weakly vary inside the volume for each layer. However, a decrease is observed beginning at 2 nm from the gate. This is attributed to the increasing impact de-trapping to the gate since the traps get closer to the gate electrode. The results also show a decrease of trap density when PDA increases from 600° C to 800° C.

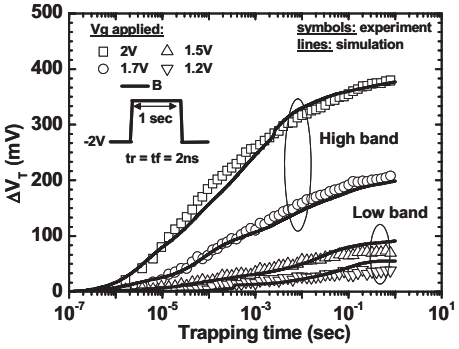


Figure 9. Experimental (symb.) and modeled (lines) V_T shift versus trapping time at different gate biases. 4.5 nm HfO_2, 600° C N. Electrical responses of high band and low band are shown.

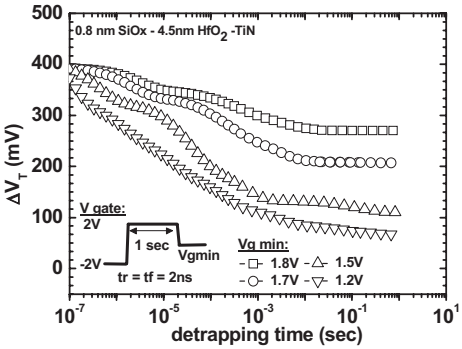


Figure 10. Modeled V_T shift decrease versus de-trapping time at different gate biases. 4.5 nm HfO_2, 600° C N.

3.1.3. *Case of full de-trapping at negative V_g*

It is well known that a negative Vg is necessary to completely de-trap charges. Fig. 12 shows electron emission times versus V_g for various trap energies: Ei_{Si}, Ei_{Si}+0.5eV, Ei_{Si}+1eV. Results suggest that for traps at high energy (~ Ei_{Si}+1eV) de-trapping transient via emission should have a dynamic similar to trapping, able to explain both trapping and de-trapping experiment in dynamic mode. However, the negative bias necessary to de-trap in quasi static experiment needs to suppose the existence of much deeper traps, near Ei_{Si}+0eV. As shown Fig.12, traps at Ei_{Si}+0.5eV would de-trap at V_g=0 in only 1s and so are too high in energy! According to the trapping experiments and modeling of paragraph 3.1.2, these traps can be filled only at Vg corresponding to higher energy (Ei_{Si}+0.8eV or Ei_{Si}+1.3eV have been found). These deep traps have a different energy for trapping and for de-trapping and could be described by a U-traps behavior [15].

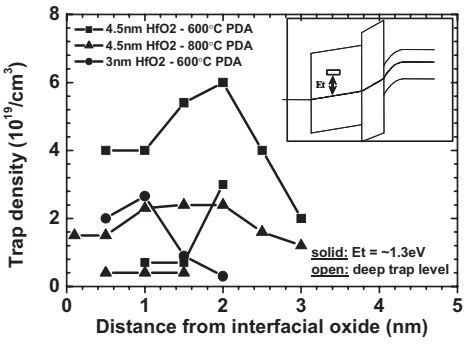


Figure 11. Summary of trap density levels used to simulate trapping and de-trapping for the studied HfO_2 stacks.

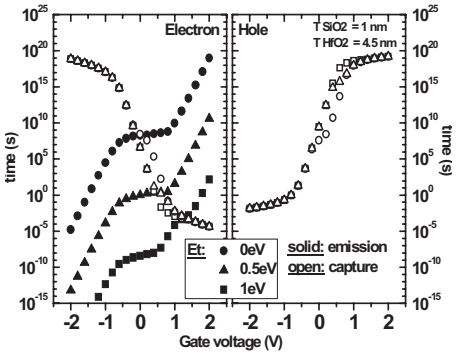


Figure 12. Electron and hole capture time and electron emission time versus biases for different trap energy levels.

3.2. DISCUSSION: IS TRAP PROFILE UNIQUE?

The previous paragraph has shown that it is possible to obtain a very consistent modeling assuming two kinds of traps, each one at a constant energy level inside the high k, with a density profile in the volume HfO_2. This density profile can be considered constant in the bulk of the HfO_2 layer but its effective density decreases near the gate (from 2nm) due to electron de-trapping. σ is taken constant for all cases and for the two trap energies.

A reasonable question is whether or not it would be possible to obtain the same quality of modeling with other trap densities, energies or physical characteristics. To try to answer at least partially to this question, we performed simulations with the proposed model of equation (1) and equation (2) but with fundamentally different trap characteristics and we compared results to experiments. The first alternative case is to suppose traps uniformly distributed in the volume of the high k, but with an energy level different than what has been previously found (1.3eV from Ei_{Si}); the second alternative is to suppose traps at a given spatial position (we study the case at the interface $SiOx/HfO_2$) and with a distribution of energy or capture cross sections. Another alternative is a distribution of energies but this case can be extrapolated from case 1.

3.2.1. *New case 1: trap density constant in volume but at another energy*

Comparison is performed on the most significant split, with highest hysteresis: 4.5 nm HfO_2, PDA 600° C. For simplicity of simulations and comparisons, only one trap level has been supposed. The trap profile (see Fig.11) has been simplified to a constant value of 6 $10^{19}cm^{-3}$ from 0.5 nm to 2 nm and a decrease at 2 nm from the gate. As discussed in the previous sections, the energy profile has a direct impact on the electrical V_g dependence. We then

compare the curve of maximum trapping $\Delta V_T(1s)(V_g)$ for the various modeling scenarios. For 1s charging, all the traps at energy under E_F are considered filled.

Fig. 13 shows the results for trap energies varying from 0.9eV to 1.8eV above Ei_{Si} and for the typical density Nst= 6 $10^{19}cm^{-3}$. It appears that the $\Delta V_T(1s)(Vg)$ curves are significantly translated when Et is shifted. The experimental curve can be clearly associated to an energy level (1.3eV) on this graph. This energy level does not depend on the trap densities: in Fig.14, the trap density is varied over two decades, from Nst/8 to Nst*32; while the shape of the curve depends on the trap density, the extrapolation to ΔV_T~0V remains unchanged. This voltage corresponds to the beginning of trapping, when the traps far from the substrate are found at E_F.

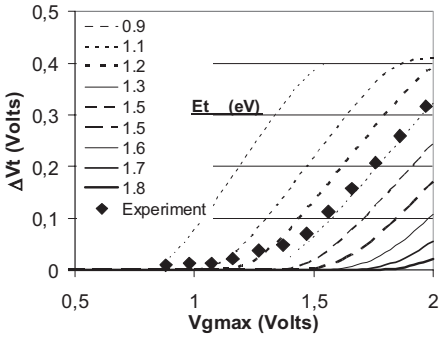


Figure 13. Simulated $\Delta V_T(1s)(Vg)$ for various trap energy levels referenced to Si mid gap. Comparison with experiment. Ntrap = 6.10^{19} cm^{-3} . 4.5 nm HfO_2, 600° C N̲.

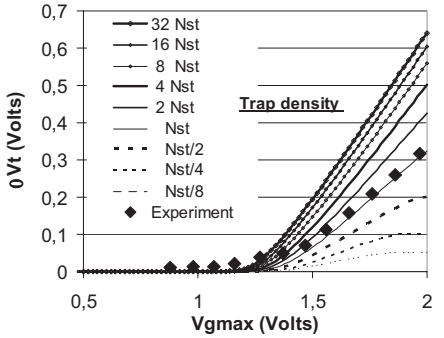


Figure 14. Simulated $\Delta V_T(1s)(Vg)$ for various trap densities and comparison with experiment. Nst is the value of Fig. 15. Et~1.3eV. 4.5 nm HfO_2, 600° C N̲.

As we have considered quasi-static V_T shift, results of Fig.13 and Fig.14 are independent of the capture cross section. However we have demonstrated that a specific cross section ($10^{-16}/\varepsilon r^2$) also leads to a good agreement with experimental transient V_T shift (Fig.9). For such a trap density profile, an increase of a factor of 10 for the cross section (from $10^{-16}/\varepsilon r^2$ to $10^{-15}/\varepsilon r^2$) would shift the modeled transient curves of a decade toward shorter transient times. A correct fit is re-obtained if we shift the trap density of 0.5 nm towards the gate.

To conclude this section, the combination of Fig.13 and Fig.14 unambiguously determines both trap energy position and trap density. The trap cross section depends on the position of trap density profile respectively to the $SiOx/HfO_2$ interface; a cross section of $10^{-16}/\varepsilon r^2$ corresponds to a trap profile starting 0.5 nm from the interface. A value of ~1.3eV above Si mid-gap agrees rather well with ab-initio simulation (1 eV above Ei_{Si} in ref. [16]) and

experimental results (1.3eV in ref. [17]) assuming a 2eV barrier height between Si and HfO_2. The involved defects could then be related to oxygen vacancies.

3.2.2. *New case 2: traps at a given spatial position and with σ distributions*

We investigate now another hypothesis, all the traps located at the interface $SiOx/HfO_2$ [18]. Experimental comparison is performed on the same split as previously. Fig. 15 shows that it is possible to fit the experimental curve with such an hypothesis. In order to fit, the energy of the traps is found at ~1.2 eV, similar to previous case (as discussed previously it is determined by the alignment of E_F with traps). In order to take into account the large range of time constants and fit the experiment on the whole range of 6 time decades (Fig.16), it is necessary to introduce a distribution of capture cross sections from $10^{-17}/\varepsilon r^2$ to $10^{-22}/\varepsilon r^2$. Of course the physical meaning of this result is questionable: while the first value is typical of neutral trap, the second value is characteristic of highly repulsive traps. Such a distribution at the same spatial and energetic position is highly unrealistic. Moreover such trap parameters lead to $\Delta V_T(t)$ curves which have a homothetic dependence with Vg (Fig.16). Experimentally, the trapping appears faster at large Vg and becomes more linear (in a time logarithmic scale) at low Vg. It evidences that the faster traps (those close to the SiOx interface in the band trap hypothesis) are only accessible at large Vg. This behavior and the need for a realistic cross section with a typical value for the involved defect lead us to reject the hypothesis of traps at the interface.

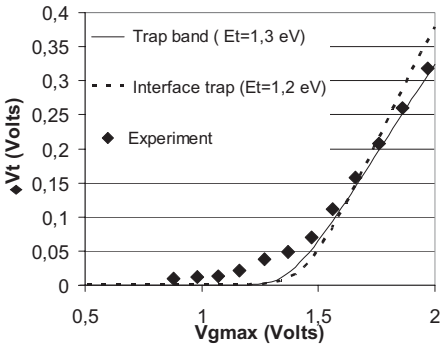


Figure 15. Simulated $\Delta V_T(1s)(Vg)$ for traps at $SiOx/HfO_2$ interface at Et=1.2eV and with σ distribution. Comparison to experiment and with "one band model". Ntrap = 6.10^{19} cm^{-3}. Case 4.5 nm HfO_2, 600° C N.

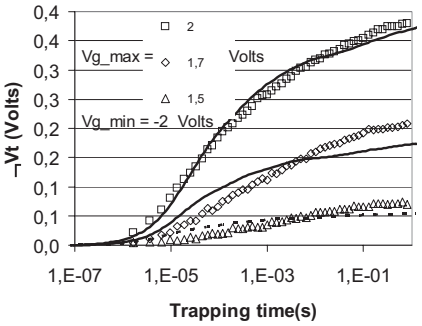


Figure 16. Simulated $\Delta V_T(t)$ traps with σ distribution (see Fig.15). Comparison with experiment.

4. Conclusion

Hysteresis phenomena has been studied through charging and discharging experiments over a wide set of conditions as time, voltage, temperature, operating modes, and on stacks with several interfacial layer and HfO_2 thicknesses. All these data have been successfully explained by a model using a trap-like approach where trapping and de-trapping are described by Shockley-Read-Hall (SRH) statistics modified by the tunneling transparency on the trapping and de-trapping probability of electrons and holes.

Measurements have been performed in a wide temperature range, from 20 K to 500K, and have been shown to validate the models once corrected from threshold voltage variations versus temperature.

Traps within two bands energy levels inside the HfO_2 are necessary to explain consistently experimental results: one around 1.3eV above the equivalent silicon midgap and one much deeper with a lower density of traps. In all cases an apparent trap density reduction is observed as the traps are less than 2 nm from the gate. This is due to the de-trapping to the gate via a field and temperature activated mechanism. This contributes to explain the decreasing impact of the hysteresis for thinner layers.

The uniqueness question of trap profile determination has been addressed. In all cases the most obvious results is the energetic position of the trap, around 1.3eV over Si mid-gap. The spatial distribution of traps with a same energy level is the most convincing hypothesis while a distribution of σ for traps all located at one interface is also possible but much more difficult to explain physically. These results and this methodology open a broad spectrum of opportunities of research, for example correlation of trap characteristics with process, correlation with ab-initio calculations and correlation with new stress generated traps.

Acknowledgements

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CHARACTERIZATION OF ELECTRICALLY ACTIVE DEFECTS IN HIGH-K GATE DIELECTRICS USING CHARGE PUMPING

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Abstract. Charge-pumping is studied and applied to the characterization of electrically active defects in high-k gate stacks. The rate equations for trap occupancy are solved to determine the energy and spatial range probed by charge-pumping. These contours are used to highlight the impact of experimental and physical parameters on the measured results. The amplitude and on/off times of the pulse are quantitatively shown to effect the depth into the dielectric probed by charge-pumping. The rise/fall times are shown to impact the energy region probed. Charge-pumping measurements were then performed on HfO_2/SiO_2 gate stacks with varying SiO_2 thickness (0.5 nm, 1.0 nm, 1.5 nm). The volume density of defects is small within the SiO_2 layer and then rise near the HfO_2/SiO_2 interface. The relative shift of the trap profile is consistent with the difference of the interfacial layer thickness indicating the reliability of the measurement.

Keywords: Charge-pumping, high-k gate dielectrics, electrically active defects, interface states

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1. Introduction

The scaling of the gate dielectric thickness in Metal Oxide Semiconductor (MOS) devices results in large leakage currents flowing through the gate dielectric. Therefore, high dielectric constant (high-κ) materials are being developed with equivalent capacitance and reduced leakage current as compared to conventional gate dielectrics.[1] However, high-κ materials typically have high densities of interfacial defects (N_{it}) near the silicon substrate.

There are several potential methods to characterize electrically active defects within the dielectric near the silicon substrate. The low-high frequency and Terman capacitance-voltage (C-V) methods have historically been the most popular.[2,3] However, even with high-κ gate stacks, leakage currents through the dielectric preclude the measurement of quasi-static C-V curves. Therefore, the low-high frequency C-V method is not possible. The Terman method is based on comparing the measured high frequency C-V data which includes stretch-out due to interface states with an ideal theoretical C-V curve with no interface states. The first problem when applying Terman to a high-κ gate stack is that the amount of shift or stretch-out caused by interface states is typically very small. For example, a defect density of 10^{12} cm^{-2} results in only a .003 V shift for a 0.62 nm equivalent dielectric. The second problem is that true high-frequency curves are typically not obtained for these thin dielectrics. Figure 1 shows a simulation[4] of C-V curves for the true high-frequency case (no interface state capacitance) and that for a frequency of 1 MHz. The difference between the curves at the gate voltage region of interest (depletion) is much greater than .003 V indicating that the Terman method would be in error. Based on the above discussion, C-V methods cannot be used to extract defect densities in advanced gate dielectrics.

The conductance technique can be applied to advanced gate dielectrics even in the presence of leakage current.[5,6] However, the technique typically involves measurement of MOS capacitors and extracts interface state density in a limited portion of the majority carrier side of the bandgap. Furthermore, there is no way to evaluate the depth dependence of defects in the insulator using conductance.

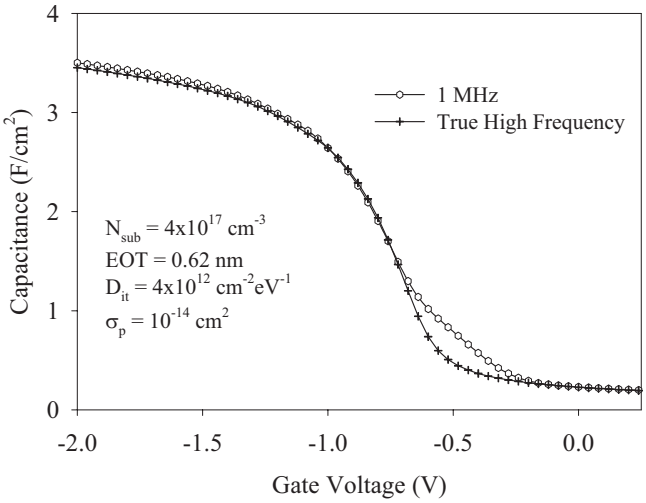


Figure 1. Simulated high- (infinite) frequency and 1 MHz C-V data.

Charge-pumping has been used to study interface traps in the Si/SiO_2 system for more than thirty years.[7-11] The distribution of Si/SiO_2 interface states in energy has been obtained using charge-pumping.[8] It has also been shown that the charge-pumping technique can provide information on the distribution of traps as a function of depth.[9-11] In this work, we first describe a comprehensive model for understanding both the depth and energy dependence of defects measured using charge-pumping. We then apply these measurements and model to HfO_2/SiO_2 stacks having various SiO_2 interface thickness. The depth dependence of the extracted defect density provides important insight into these stacks and illustrates the capability of the charge-pumping technique in the measurement of high-κ gate stacks.

2. Charge-pumping Theory and Model

In charge-pumping of n-channel transistors (mechanisms are similar for p-channel), periodic pulses are applied to the gate and drive the channel region into inversion and accumulation, with source and drain typically connected to ground. When the semiconductor surface is in accumulation, all of the interface states above the quasi-Fermi level at accumulation are filled with holes. As the gate voltage starts to increase, holes are emitted from the interface states at a rate which is governed by the rate of change of surface potential (steady state hole emission). At the flatband voltage, the surface potential begins to change at a very rapid rate and the holes can no longer emit fast enough to keep up with

the change in surface potential. Thus, the holes leave the interface states at a rate governed by hole emission (non-steady state hole emission). When the gate voltage reaches the threshold voltage, the interface states below the quasi-Fermi level at inversion are filled with holes. Thus, more holes were initially captured in the states than were emitted. When the gate voltage goes above the threshold voltage, electrons are swept into the channel from the source and drain and are trapped in interface states not yet emptied of holes (trapping of electrons). The channel is then in equilibrium with the energy bands and the interface states up to the quasi-Fermi level at inversion are filled with electrons. As the gate voltage decreases similar mechanisms are in operation (steady state electron emission, non-steady state electron emission, trapping of holes). The channel is then again in equilibrium with the energy bands and the interface states down to the quasi-Fermi level at accumulation are filled with holes. The dc charge pumping current measured at the substrate arises because more holes are captured than emitted.

If the pulse amplitude (V_a) is kept constant and the pulse base voltage (V_{base}) is swept from flat band voltage (V_{FB}) to threshold voltage (V_{th}) or vice versa, a maximum dc charge-pumping current ($I_{CP,MAX}$) will be observed. Conventionally, $I_{CP,MAX}$ is expressed as,[8]

$$I_{CP,MAX} = q\, N_{it}\, f\, A_G \tag{1}$$

where q (C) is the unit Coulombic charge, f (s^{-1}) is the frequency of the applied pulses, A_G is the effective channel area (cm^2) and N_{it} (cm^{-2}) is the total number of traps per unit area. In this expression, N_{it} is typically considered to be independent of the distance of traps from the interface. This assumption is valid in the Si/SiO_2 system for which most traps are located close to the Si/SiO_2 interface and are probed by the CP measurement at moderate frequencies.

To include the effect of the spatial distribution of traps to $I_{CP,MAX}$, equation (1) is re-written as[9-11]

$$I_{CP,MAX} = q\, f\, A_G \int_0^{x_d} \int_{E_{min}}^{E_{max}} n_T(x)\, \Delta F(x, E_t)\, dE_t\, dx \tag{2}$$

where, n_T ($cm^{-3}eV^{-1}$) is the volume and energy density of traps at a given depth and energy, ΔF indicates the probability that a trap can be probed by charge-pumping and is a function of the distance from the Si-substrate/gate-dielectric interface (x) and the trap energy (E_t). The upper and lower limits of the double integral are the energy range ($E_{max} - E_{min}$) and the maximum depth (x_d) in which traps inside can be probed. It will be shown in the following that ΔF is strongly affected by the parameters of the pulses applied to the gate during the charge

pumping measurement such as pulse on/off time (t_{on}/t_{off}) which controls the depth probed and pulse rise/fall time (t_r/t_f) which controls the energy region probed. One can also define the energy density of interface traps as

$$D_{it} = dN_{it}/dE_t \tag{3}$$

and the volume density of traps as

$$N_T = dN_{it}/dx\,. \tag{4}$$

Modeling of ΔF can be performed by considering the capture and emission processes of electrons and holes at traps described in Shockley-Read-Hall theory.[9-14] Details of these calculations can be found elsewhere.[15] The results depend strongly on the parameters chosen including electron and hole effective mass ($m_{e/h}$), barrier height for electrons and holes ($\Phi_{e/h}$), and electron and hole capture cross sections at the interface ($\sigma_{n/p}(0)$). Figure 2 shows a 3-D contour of ΔF as a function of trap energy and distance measured from the silicon interface toward the dielectric using parameters commonly accepted for pure SiO_2 ($m_{e/h}$ = 0.5/0.4 eV, $\Phi_{e/h}$ = 3.1/3.8 eV, $\sigma_{n/p}(0) = 10^{-14}/10^{-16}$ cm^{-2}).[16] Traps located inside the trapezoidal plateau with ΔF equal to approximately one have the maximum probability to be probed and contribute to $I_{CP,MAX}$ during charge-pumping. For these conditions, ΔF drops from one to zero at approximately 0.8 nm. Traps beyond this depth are not detected by charge-pumping. Therefore, the maximum depth probed by charge-pumping (x_{max}) can be defined.

Figure 3 shows a 2-D contour of $\Delta F = 0.5$ for three different conditions of t_{rise} and t_{fall}. At a given depth, the range of energy probed by charge pumping is wider than the range of energy probed at the Si/SiO_2 interface. During the pulse on (off) times, defects throughout the bandgap up to a certain depth are filled by electrons (holes). During the initial phase of the rise (fall) time, holes (electrons) are emitted from the defects at a rate independent of the silicon Fermi energy and before trapping (and recombination with) the opposite carrier can occur. The rate of emission of carriers from defects situated at a given depth from the interface is slower than that at the interface due to tunneling. Therefore, more emission occurs near the Si/SiO_2 interface as compared to a given depth from the interface explaining the range of energy probed by charge pumping. These results also show that the energy distribution of defects can potentially be probed by varying rise or fall time. The energy dependence of defects extracted from HfO_2 stacks by varying t_{rise} and t_{fall} was studied elsewhere.[17,18] The results indicate a higher density of defects in upper half of

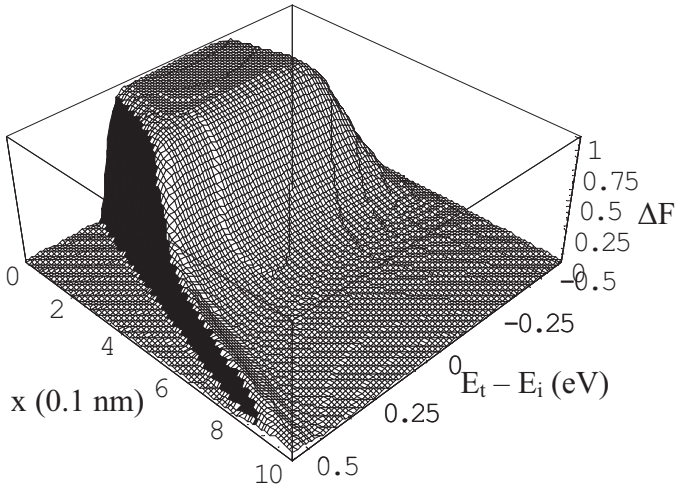


Figure 2. 3-D contour plot of ΔF as a function of trap energy and depth from the Si/SiO_2 interface.

the gap as compared to the lower half. Determining the defect density as a function of depth and energy together is possible, but is beyond the scope of this work.

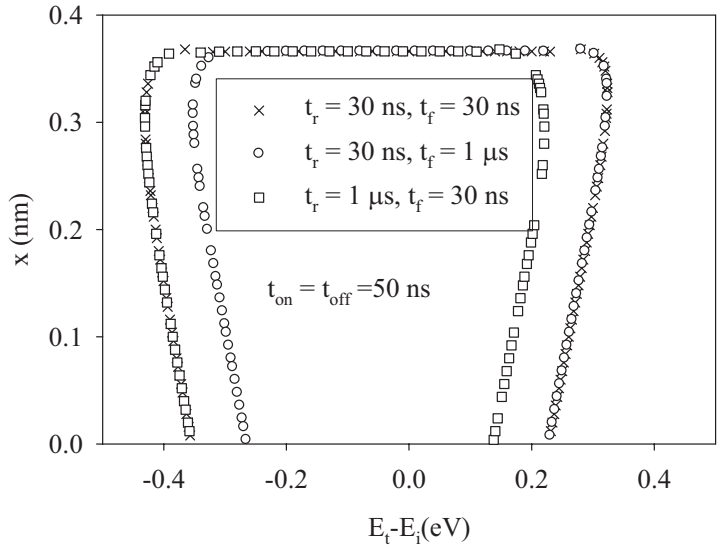


Figure 3. 2-D contour for ΔF=0.5 as a function of depth and trap energy for varying rise and fall times.

Figure 4 shows simulated x_{max} as a function of t_{on} or t_{off} using parameters for SiO_2 for three different cases: varying t_{on}=t_{off}, varying t_{on} with t_{off} = 50 ns, and varying t_{off} with t_{on} = 50 ns. In the formulation of ΔF t_{off} controls the depth at which holes are trapped by defects. t_{on} controls the depth at which electrons are trapped by defects. Recombination and, hence, charge pumping current, occurs only when both electrons and holes are trapped. Varying t_{on} (t_{off}) while keeping t_{off} (t_{on}) constant results in a saturation of x_{max} with t_{on} (t_{off}). Therefore, to continuously probe defects as a function of depth, one must vary both t_{on} and t_{off}. In the following, we will experimentally measure the depth profile of defects in HfO_2/SiO_2 stacks with varying SiO_2 interlayer thickness.

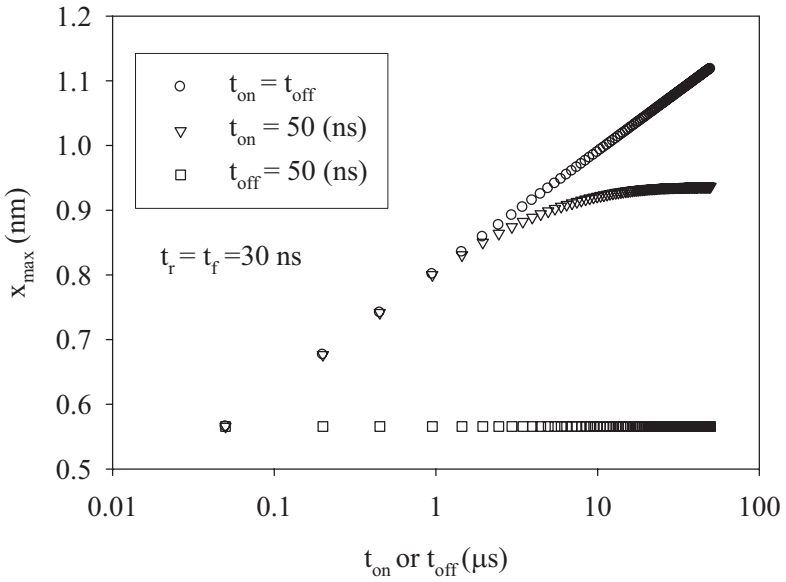


Figure 4. Maximum depth probed by charge-pumping (defined by ΔF=0.5) as a function of pulse on and off time.

3. Experimental Conditions

The devices used in this work are fully processed MOSFETs with HfO_2/SiO_2 stacked gate dielectrics. High-κ gate dielectric transistors were fabricated on 200mm p/p+ epitaxial Si <100> wafers using a standard CMOS process with 1000 °C, 10 s dopant activation anneal. The gate stacks were formed by depositing a 3 nm atomic layer deposited HfO_2 dielectric on various scaled thermal oxide interface layers (IL) created by the controlled etch-back of a 1.9 nm thermal oxide. Three IL thicknesses were tested: 1, 1.5 and 2 nm. The high-

κ film deposition was followed by a 700 ºC anneal in NH_3 ambient, after which, a gate electrode was formed by chemical vapor deposition of TiN with poly-Si cap. A control gate dielectric of 3.5 nm thermally grown SiO_2 was also studied. Charge-pumping measurements were performed by applying periodic trapezoidal pulses with fixed rise/fall time and amplitude generated by an HP8112A pulse generator to the gate. The dc electron-hole recombination current is measured from the substrate by using an HP4156B semiconductor analyzer. To probe traps at different depth in the dielectric, pulse on and off times (t_{on} and t_{off}) are kept of equal value and varied from 50 ns to 100 ms.

4. Results and Discussion

Figure 5 shows the total measured trap density per unit area (N_{it} cm^{-2}) as a function of $t_{on} = t_{off}$ for all devices. The values of N_{it} at the smallest $t_{on} = t_{off}$ (or x) for all dielectrics are very similar, which suggests that all dielectrics have approximately the same amount of traps within the SiO_2 interfacial region. These traps are attributed to the commonly observed interface traps at the Si/SiO_2 interface. The SiO_2 control shows a constant N_{it} throughout the detectable depth range. This suggests that all of the traps are located near the Si/SiO_2 interface which is expected and is consistent with observations from other groups. For the HfO_2/SiO_2 stacks, N_{it} increases with depth and N_{it} at a given depth decreases with increasing SiO_2 interfacial layer thickness. The thickest interfacial layer (2 nm) shows behavior similar to that of the control SiO_2 dielectric. This suggests that the 2 nm interfacial layer is beyond the maximum depth able to be probed by charge pumping.

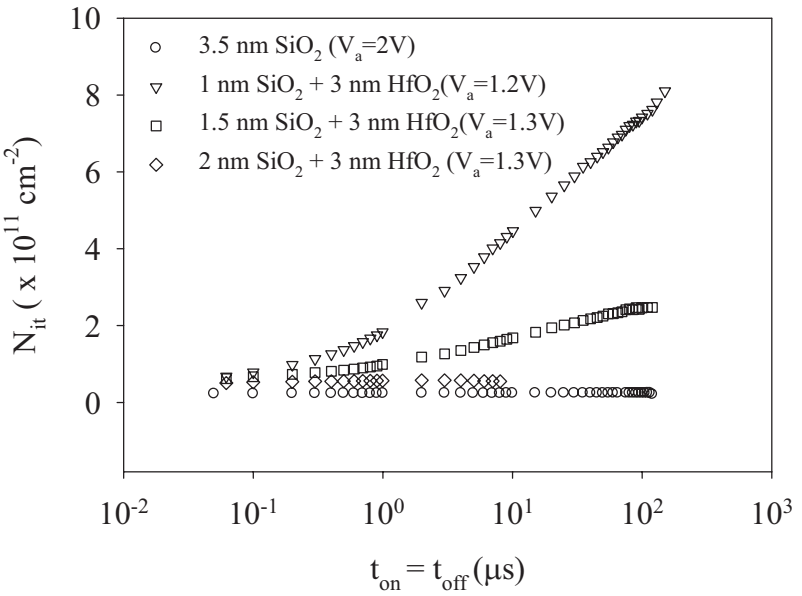


Figure 5. Measured total trap density (cm^{-2}) as a function of pulse on and off time.

The trap volume density, N_t (cm^{-3}) as a function of depth for the HfO_2/SiO_2 stacks with the two thinnest dielectrics is shown in Fig. 6. N_t is determined using two different sets of parameters, namely, those commonly assumed for SiO_2 ($m_{e/h}$ = 0.5/0.4 eV, $\Phi_{e/h}$ = 3.1/3.8 eV, $\sigma_{n/p}(0) = 10^{-14}/10^{-16}$ cm^{-2}) and those commonly estimated for HfO_2 ($m_{e/h}$ = 0.1/0.1 eV, $\Phi_{e/h}$ = 1.3/3.3 eV, $\sigma_{n/p}(0) = 10^{-14}/10^{-15}$ cm^{-2}). These estimated values indicate the range of values likely for the interfacial region. These different sets of parameters not only shift the curves along the x axis but also result in different magnitudes of N_t.

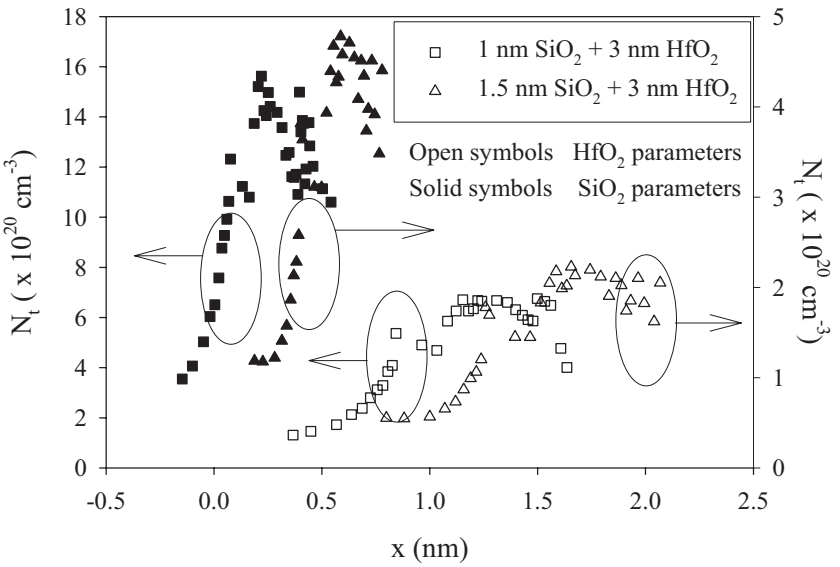


Figure 6. Extracted volume trap density (cm^{-3}) as a function of x for the high-κ stacks having 1.0 nm and 1.5 nm interfacial layer thickness. The volume trap density is determined assuming 2 different sets of parameters: those for SiO_2 and those for HfO_2.

It is clearly observed that both dielectrics show low N_t at small depth, which then increases with x and finally saturates. This result may suggest that the region probed by charge pumping moves from a SiO_2-like region, through an SiO_2/HfO_2 interfacial region and then reaches a pure HfO_2 region. The saturation of N_t in the HfO_2 region may suggest that the trap distribution within the HfO_2 is relatively uniform. Independent of the parameters chosen, it is observed that the SiO_2/HfO_2 interfacial region in these two dielectrics is different by approximately 0.4 nm, which is close to the difference between the SiO_2 interfacial layer thicknesses of these two dielectrics. This suggests that although the accurate probing depth is unknown, the relative trap spatial distribution is accurate. Furthermore, the results suggest that the deposited HfO_2 interacts with the grown SiO_2 interfacial region resulting in a SiO_2/HfO_2 interface within the original SiO_2.

5. Summary and Conclusions

A model for charge pumping was developed which provides a fundamental understanding of both the energy and spatial distribution of traps probed. Charge pumping was applied to HfO_2/SiO_2 gate stacks with varying SiO_2

interfacial layer thicknesses. Although an accurate depth position of traps cannot be determined due to unknown values of the dielectric parameters, the relative shift of the trap depth profile is consistent with the difference of the interfacial thicknesses. The results indicate the capability of charge pumping in the extraction of defect densities from high-κ gate dielectric stacks. The results suggest that the deposited HfO_2 interacts with the grown SiO_2 interfacial region resulting in a SiO_2/HfO_2 interface within the original SiO_2. Further work is required to fundamentally determine the correct parameters necessary to extract trap densities from charge pumping data and to simultaneously extract the energy and depth profiles of defects.

Acknowledgements

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IMPACT OF HIGH-K PROPERTIES ON MOSFET ELECTRICAL CHARACTERISTICS

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Abstract. The integration of high-κ dielectrics in MOSFET devices is beset by many problems. In this paper a review on the impact of defects in high-κ materials on the MOSFET electrical characteristics is presented. Beside the quality of the bulk of the dielectric itself, the interfaces between the high-κ and the interfacial oxide layer and the gate electrode are of crucial importance. When poly-Si is used as gate electrode, the defects at the poly-Si / high-κ interface control the band alignment as well as the gate depletion. The quality and thickness of the interfacial SiO_2 controls both the carrier mobility in the channel as well as the kinetics of charging and discharging of pre-existing high-κ defects. The quality of the interfacial layer has also important consequences for reliability specifications like negative bias instability and dielectric breakdown.

Keywords. high-κ defects, breakdown, internal photoemission, mobility, metal gates, transient instability, charing and discharging, HfO_2 defects

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1. Introduction

In the recent years tremendous research efforts have been focused on the investigation of so-called high-κ gate dielectrics for the potential replacement of SiO_2 in advanced CMOS technologies [1-3]. The high-κ oxides allow the further increase of the gate capacitance without paying the price of an increased leakage current (and thus dissipated power). The purpose of this article is to give an overview of the electrical properties of high-κ based MOS devices. At this time the gate dielectrics considered present several challenges, especially due to the presence of non-idealities (i.e., defects) in these layers.

This paper is organized as following. After this introduction the impact of defects in the high-κ layer will be discussed on the basis of a simple phenomenological model, which is able to capture most of the relevant physics. The quality of the interfacial layer controls the mobility as well as timing of transient charging instability. The transient charging and discharging on pre-existing defects also depends on the quality of the dielectric considered. The application of these techniques will be discussed together with the defect creation during stress and subsequent breakdown.

2. A model of defects present in the high-κ stack

Most of the electrical characteristics of Hf-based dielectrics can be better understood from the model in fig.1. In fig.1 the band diagram for the Si / SiO_2 / high-κ / gate is schematically shown along with the defects present in the layers. The interfacial SiO_2 is (so far) inevitable and limits the overall EOT scalability. The defects at the SiO_2 / HfO_2 interface limits the mobility (i.e., drivability) of these devices [4-8]. Defects in the bulk of the high-κ can also be dynamically charged and discharged during operation conditions. The transient charging of these defects leads to an unacceptable reduction in device performances. To further complicate the picture, defects at the high-κ / gate electrode interface are also important. These defects are screened by the carriers in the gate electrode thus resulting in an effective change in the gate workfunction. Furthermore in the case of degenerately doped gate electrodes (i.e., poly-Si) the defect density is usually comparable to dopant concentration and the screening effect will result in a larger poly-Si depletion (i.e., the so-called Fermi Level pinning).

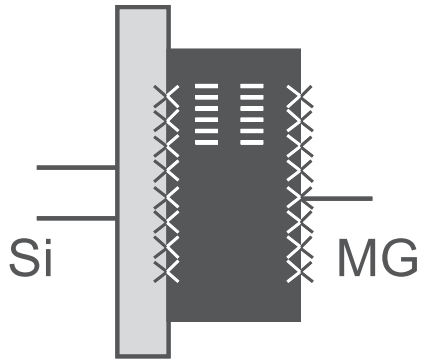


Figure 1. Band diagram of a SiO_2 / HfO_2 / metal gate (MG). In this model it is assumed that defects are present at the interface between the HfO_2 and SiO_2 and MG, respectively. A defect band is also assumed to be present in the bulk of the HfO_2. The energy position of these defects is assumed to be in the upper part of the HfO_2 bandgap.

3. Defects at the gate / dielectric interface

One of the first problems observed in the integration of high-κ layers with poly-Si gates is the control of the flat-band voltage, V_{FB}, and threshold voltage, V_{th}, of the devices. With respect to the ideal SiO_2/poly-Si reference system, shifts in V_{FB} and V_{th} are observed, as illustrated in Fig. 2. This shift is asymmetric, being positive for n^+-poly-Si and negative for p^+-poly-Si. Two possible explanations were given in the literature for this effect. Hobbs *et al.* [9] reported V_{FB} measured on several SiO_2 samples with increasing submonolayer HfO_2 concentration at the poly-Si interface. Hobbs *et al.* [9] proposed that the interaction of Hf atoms with the poly-Si layer was creating a large density of defects in the Si bandgap, capable of "pinning" the Fermi level, effectively changing the gate electrode workfunction, hence, the V_{FB}. More recently, it has been shown that a similar flat-band voltage shift is observed for undoped poly-Si layer [10,11] as well as fully-silicided gates [10]. Conversely, it was argued that the V_{FB} and V_{th} shifts could be related to the presence of fixed charge in the high-κ layer. In the model of ref. [12], the V_{th} shifts were mainly attributed to the penetration of dopants into the dielectric layer during the poly-Si activation process.

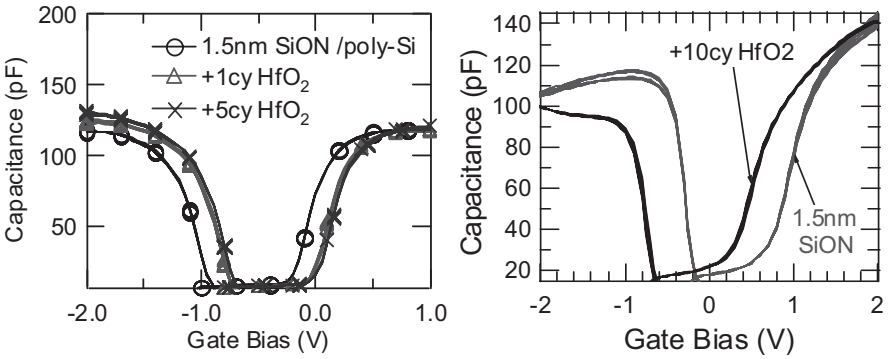


Figure 2. (a) Split capacitance-volage characteristics of SiO2/HfO2/n+poly-Si devices, with different HfO2 surface coverages. The deposition of 1 cycle (5 cycles) of HfO2 on top of SiO2 covers about 10% (50%) of the surface (island growth). (b) Same than in (a), for SiO2/HfO2/p+poly-Si devices.

Since these interpretations of V_{FB} shifts have been largely based on the extraction of V_{FB} from capacitance-voltage (C-V) measurements, it is not possible to clearly distinguish whether the observed effects originate from charge incorporation into the dielectric layer or a change in the band alignment at the gate electrode side. Furthermore both models mentioned above neglect a fundamental aspect, namely the *screening effect* due to charge carriers in the gate electrode. Free charge carriers in the poly-Si gate can screen any charged defect present in the dielectric layer near the gate/dielectric interface. As illustrated in Fig.3, it is assumed that the (charged) defect states in the Si bandgap are located at a small distance from the poly-Si surface (on the order of a few Å). The sign of the charge related to these defects depends on the poly-Si doping type. Free charge carriers in the poly-Si layer will then screen this charged defect. This charge and its image charge in the poly-Si electrode then establish an interfacial dipole. The presence of a surface dipole perturbs the electrostatic potential at the top dielectric/gate electrode interface, and has important consequences for device operation. First of all, this interfacial dipole causes V_{FB} and V_{th} shifts (see fig.2 and 4). Secondly, the built-in electric field contributes to additional Coulomb-like scattering of charge carriers in the Si (substrate) channel, as shown in [8]. Additionaly, redistribution of the carriers in the gate electrode occurs, due to the screening effect. If the defect charge density is comparable to the poly-Si dopant density, then additional poly depletion takes place. This is indeed the case, as shown in fig.2b. The large band bending (i.e., depletion) in the poly-Si layer is then very similar to the so-called Fermi-level pinning observed in Schottky barriers [13,14].

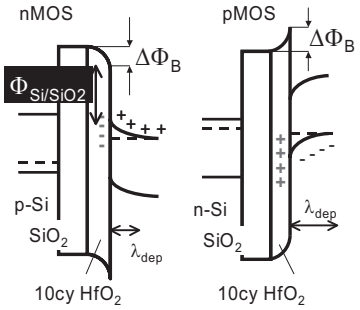


Figure 3. Schematic energy band diagram of a $Si/SiO_2/HfO_2$ structure. A surface dipole is assumed close to the HfO_2/poly-Si interface. The the poly-Si doping controls the charge-state of the defect.

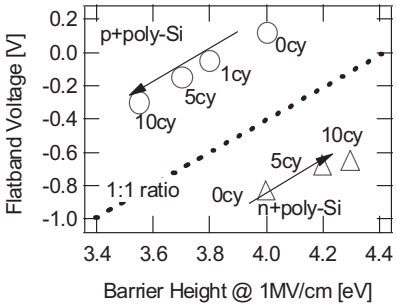


Figure 4. Flat-band voltage of SiO_2/HfO_2/poly-Si structures (from C-V characteristics), as a function of the HfO_2/poly-Si barrier height (measured directly with IPE).

A further experimental proof of the presence of a surface dipole contribution comes from the Internal Photoemission measurements (IPE). IPE measures directly [15] the barrier height Φ_B for electron and hole injection over Si/dielectric interfaces. It appears clearly that the presence of HfO_2 traces induces *an increase* in Φ_B by up to ~200mV with n^+-poly Si gates. As the HfO_2 surface coverage increases, Φ_B increases for n^+-poly-Si gates and decreases for p^+-poly-Si gates, as shown in Fig.4. A one to one correlation between Φ_B change and V_{FB} shift is also clearly observed from this figure. A more detailed analysis of the IPE results reveals the discrete nature of these charges located near or at the interface [16].

4. Transient Charging in pre-existing traps

This section describes the electrical stability and reliability issues of SiO_2/HfO_2 gate stacks. When combined with a poly-Si gate, this dielectric stack has a defect band of bulk HfO_2 traps that can very efficiently trap electrons. This causes hysteresis in the C-V curves and transistor characteristics. Furthermore, the charge trapping also affects the extraction of important transistor parameters like transconductance and threshold voltage. We evaluate different measurement methods to study the charge trapping and provide a simple empirical model for the charging kinetics. Most of the results presented in the following focus on polycrystalline HfO_2 deposited by ALD. Several other deposition techniques (MOCVD, PVD), chemical precursors, post deposition-annealing were also used for similar studies. Marginal differences were found between them, suggesting that the instability observed is a property of the

dielectric considered rather than due to chemical impurities. A recent report by Gusev *et Al.* [17] suggests that the use of the metal gate can alleviate some of these problems. Other high-κ materials (HfSiON, $LaHfO_{3.5}$) seem more stable than pure HfO_2, as recently reported by in [18, 19].

The results for HfO_2 can be easily explained if we postulate the presence of a defect band located above the Si conduction band [20] (see the band diagram in Fig. 1). The defects in this band can be very efficiently charged when a positive gate voltage (V_G) is applied. Electrons tunnel through the interface layer directly into the traps, or into the HfO_2 conduction band with subsequent trapping, as illustrated in Fig. 5 (a). The traps in the defect band are discharged at zero bias or –more efficiently – at negative gate bias, as illustrated in Fig. 5 (c). With this simple picture, one can readily understand most of the electrical instabilities observed in the capacitor and transistor characteristics as will be demonstrated in the following paragraphs.

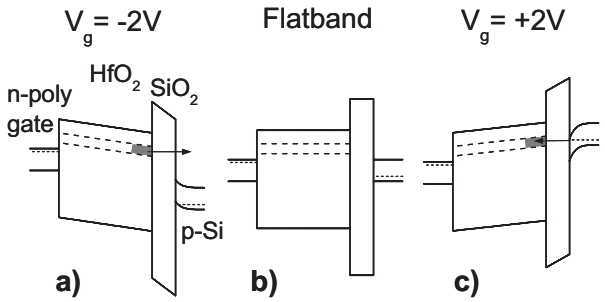


Figure 5. Schematic energy band diagram of a SiO_2/HfO_2/poly-Si gate stack containing a defect band in the HfO_2 layer at flatband condition (b), for negative (a), and for positive gate bias (c), the defects located near the SiO_2 interfacial layer move rapidly with respect to the Fermi-level in the Si substrate.

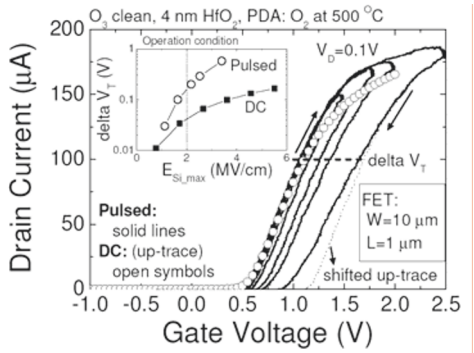


Figure 6. I_D-V_G traces measured a fast voltage ramp [24,25]. The open symbols show an uptrace measured by conventional quasi DC technique. Significantly more threshold voltage shift is measured with a fast pulse technique, demonstrating the fast charge trapping in these layers. The inset shows the V_T-shift as a function of the maximum Si-field for both measurement techniques.

In order to study the details of the charging kinetics, fast voltage transients are mandatory. In this work the drain current I_D was measured in the μs to ms time range [21]. The I_D-V_G characteristics measured are presented in Fig. 6. The open symbols show a 'quasi DC' measured trace, illustrating how in this case the charge trapping is already occuring during the voltage ramp. The V_{th}-shifts measured with fast pulses are significantly larger than with 'quasi DC' techniques as can be seen in the inset of Fig.6. In non-optimized stacks, a hysteresis of more than 1V can be observed!

The interfacial SiO_2 layer strongly influences the charge trapping by controlling the electron injection (into the traps). The influence of the interfacial layer on the bulk trapping in HfO_2 can be decoupled using a 'thick' 9 nm SiO_2 layer [22,23]. Detailed charge trapping studies were carried out varying the injection condition and the lattice temperature and it was concluded that only the electron fluence controls the trapping, while the detrapping is controlled by oxide electric field in combination with the lattice temperature.
For a given amount of injected charge, N_{inj}, the apparent trapping probability,

$$\overline{P(N_{inj})} = \bar{x} \cdot P(N_{inj}) \tag{1}$$

is proportional to the trapping probability, P, and the charge centroid, $\bar{x}$, as measured from the gate electrode . The apparent trapping probability

$$\overline{P(N_{inj})} = \Delta N_{tr} / \Delta N_{inj} \tag{2}$$

where ΔN_{tr} is the amount of trapped charge determined from the drain current decrease at stress condition (assuming that the channel electron mobility is unchanged), and ΔN_{inj} is the amount of injected carriers determined from the gate leakage current. As an alternative, the V_{FB} shift in a capacitor can also be used.

The measured apparent trapping probability, $\bar{P}$, is shown in Fig. 7a. Independent of the SiO_2 thickness, a large trapping probability (close to 0.3) is measured for $N_{inj} < 10^{12}$ cm^{-2}, and $\bar{P}$ decays with $(N_{inj})^{-1}$ at larger fluence. The fact that the value of $\bar{P}$ appears to be saturated at 0.2 - 0.3 can be explained by the charge location, $\bar{x}$. If we assume that the charge is located in the bulk of the HfO_2, a charge centroid of $\bar{x} \sim 0.3$ is estimated, suggesting that all the injected charge gets trapped initially, P≈1, providing a simple explanation for the saturation of $\bar{P}$.

Furthermore, since $\bar{P}$ is independent of the gate voltage, the trapped charge can simply be calculated by integrating $\bar{P}$ over the injected charge. As expected, this approach works well, as shown in Fig. 7b for identical HfO_2 samples with 1nm and 2nm interfacial SiO_2 respectively. The interfacial SiO_2

controls the supply of electrons that can flow to the gate, and thus the amount of charge trapped at each voltage condition.

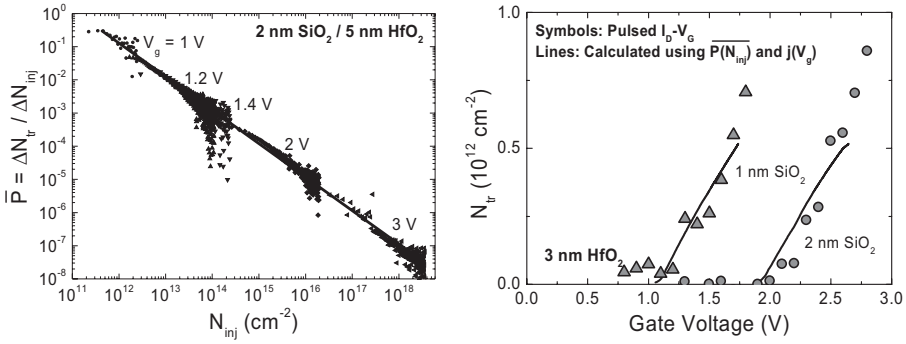


Figure 7(a). Apparent trapping probability, $\bar{P}$, as a function of electron fluence, N_{inj}, for several gate biases. Fig. 7(b). Comparison of the measured trapped charge with the calculated trapped charge (using the apparent trapping probability of Fig. 7a and gate current data) in a 3nm HfO_2 layer with 1 and 2nm thick interfacial layers, respectively.

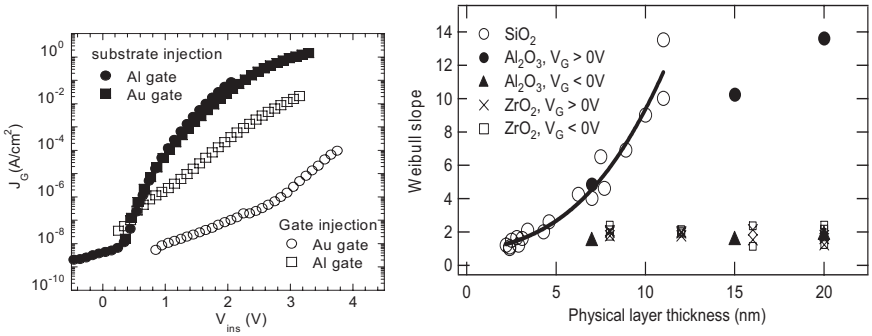


Figure 8. Gate current-voltage characteristics of SiO_x/ZrO_2 stacks under substrate (V_G>0) and gate (V_G<0) injection (right). The Weibull slope plotted as a function of the physical thickness of the high-κ layer in the stack (right). The polarity dependence of the Weibull slope for Al_2O_3 can be observed [24]. In case of ZrO_2, no polarity dependence is found. For comparison, the thickness dependence of the Weibull slope for SiO_2 layers is also shown.

5. Application: wearout and time-dependent dielectric breakdown

SiO_2/high-κ stacks systematically show a large asymmetry in the gate current vs. gate voltage characteristics, as illustrated in Fig. 8a (left). This effect is caused by i) the asymmetry of the dielectric energy band-structure and ii) the work function difference between the gate (poly-Si or metal) and the Si substrate. This asymmetry is also reflected in the reliability characteristics and, for instance, time-dependent dielectric breakdown (TDDB) distributions can have polarity-dependent Weibull slopes, as observed on SiO_2/Al_2O_3 stacks [24],

see Fig. 8b. The Weibull slope of the time-to-breakdown (t_{BD}) distribution can be used as an indicator to decide whether the interfacial SiO_2 or the high-κ layer triggers the stack breakdown. Using the t_{BD} distribution in this way is, however, an indirect approach, and it does not yield a definite answer. Only by analyzing the defect generation directly, one can gain insight into the physical mechanisms that control breakdown.

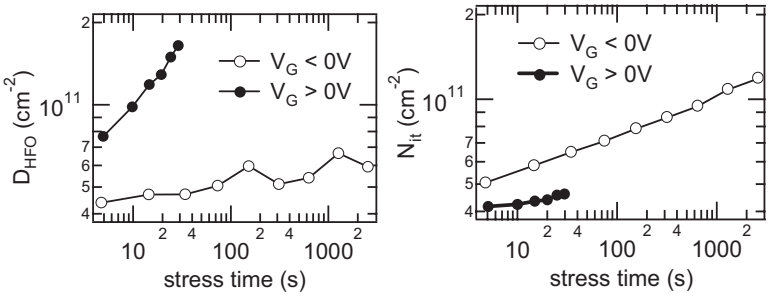


Figure 9. The increase of the bulk HfO_2 trap density D_{HFO} (left) and the Si/SiO_2 interface trap density N_{it} (right) vs. time during positive and negative gate voltage stress. Breakdown occurs after 30s for V_G>0V, while it does not occur even after 2500s for V_G<0V. For V_G>0V, the D_{it} increase is very small and substantially lower than for V_G<0V.

Charge pumping at variable frequency and amplitude is a useful technique to study defects in high-κ stacks [25]. By subtracting the charge pumped at low frequency from the charge pumped at high frequency, a measure for the trap density in the bulk of the high-κ layers can be obtained. The low frequency used in this work allows probing (i.e., charging and discharging) traps both in the HfO_2 bulk and at the SiO_2/HfO_2 interface. We applied the charge pumping method to a 1 nm SiO_2/4 nm HfO_2 stack with poly-Si gates to study the generation or buildup of defects during the electrical stress of the device [26]. Fig. 9 illustrates the polarity dependence of trap generation in the bulk of the HfO_2 layer and at the Si/SiO_2 interface after electrical stress. The large interface trap generation for negative polarity has been confirmed also on SiO_2/Al_2O_3 by capacitance-voltage measurements [24] and is related to the high energy of the electrons entering the substrate [26]. For positive stress polarity, the HfO_2 bulk trap generation is more important.

We now focus mostly on positive gate bias stress in nMOS devices. The HfO_2-bulk trap density as a function of the injected electron fluence at different stress voltages is shown in Fig. 10a. As the stress voltage decreases, the trap generation rate decreases and below 1.3 V, no significant trap generation is observed. Furthermore, the stress-induced leakage current (SILC) increases linearly with the generated HfO_2 defects (cf. Fig. 10b), like in SiO_2 layers [27].

We explain these observations in Fig. 11 by a two-component model for the current injection [28]: electrons that move through the stack by a trap-assisted

conduction mechanism arrive at the anode with low energy and cause no degradation. Electrons that tunnel directly to the anode are more energetic and therefore more effective in creating HfO_2 traps. As V_G is lowered, the decrease of the observed trap generation rate can be explained by the growing fraction of defect-related leakage current as opposed to direct tunnel current. We observed that even in an unstressed device, the leakage current at low voltage is entirely defect-related.

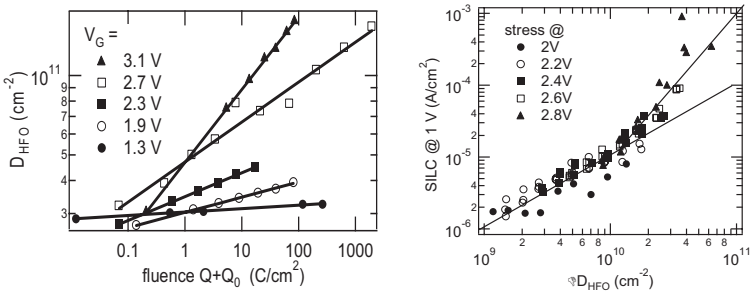


Figure 10 (a). The HfO_2 trap density D_{HFO} vs. $(Q+Q_0)$ (fluence and pre-stress fluence). The initial trap density is treated as if it were generated during a pre-stress with injected fluence Q_0. Note that only a fixed fraction of the total HfO_2 trap density is measured. Fig. 10 (b). At low trap density, the SILC (J_G @ V_G=1V)has a one-to-one relation with the electrically generated HfO_2 bulk trap density. Near breakdown, the SILC rises faster than proportionally.

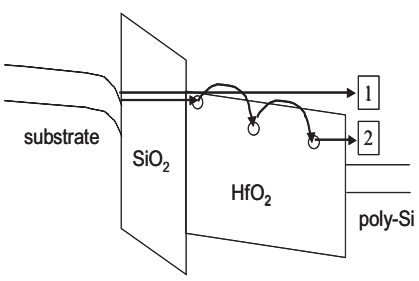


Figure 11. Two components in the leakage current are to be considered: 1) the tunneling current and 2) the trap assisted current.

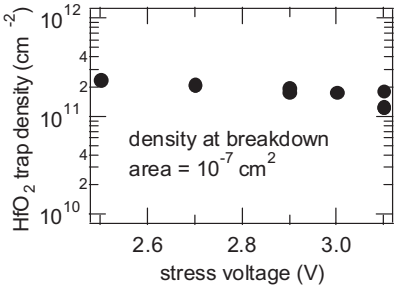


Figure 12. The bulk HfO_2 trap density at breakdown (~$2x10^{11}$ cm^{-2}) is nearly constant in the measured stress voltage range.

As illustrated in Fig. 12, the breakdown under positive gate bias stress occurs when the HfO_2 trap density reaches a critical value, independent of the gate bias polarity, suggesting that the HfO_2 layer controls the breakdown of the entire stack; hence percolation theory can be applied in this case [29]. It is worth pointing out that in large area devices, the initial trap density in this particular stack is already above the critical trap density, resulting in a large yield loss [25]. The initial defect density in HfO_2 can only be reduced with metal gates. The presence of two current components (see fig.11) complicates the extrapolations of TDDB lifetime from high voltage stress conditions (where

tunneling current dominates) to low voltage operating conditions (where defect-assisted conduction dominates). Combining the critical threshold with the trap generation behavior in Fig. 10a, a very long time-to-breakdown at operating conditions it is expected (due to the gate leakage reduction).

6. Summary and conclusion

The combination of high-κ dielectrics with metal gates appears to be a promising solution for the further scaling down of CMOS devices. However the defect density present at the interfaces and in the bulk of the high-κ have to be reduced. The interaction of the high-κ material with poly-Si resulted in the so-called "Fermi level pinning" problem, causing un-controllable shifts of the flatband and threshold voltages of the devices. Experimental results also confirmed the local change in barrier height at the poly-Si/HfO_2 interface induced by surface dipoles. This effect seems mainly driven by the high thermal budget used during the junction activation step rather than the dopant impurities in the gate electrode. V_{th} instability could be explained by the charging and discharging of a defect band present in the HfO_2 energy band-gap, located above the Si conduction band. The trapping kinetics only depended on the electron fluence, while the detrapping was controlled by oxide electric field in combination with lattice temperature. The instability seems to be related to the HfO_2 itself rather than the deposition technique or the integration scheme considered. Other dielectric materials seem more promising from that standpoint. Polarity dependent degradation and breakdown was observed. For negative stress polarity, the interface layer was severely degraded and in many cases the breakdown of this layer also determined the breakdown of the entire stack. For positive stress polarity, a clear relation between creation of traps in the high-κ bulk, leakage current, yield and breakdown was revealed. The Weibull slope values found were rather low (close to 1) suggesting that some extrinsic failure mechanism may be present in these layers. It is not clear at the moment whether these effects may be linked to the crystalline phase in HfO_2 or the presence of some residual contaminants (like Zr) or impurities (Cl, C, etc.) in the films.

Acknowledgements

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STRUCTURAL EVOLUTION AND POINT DEFECTS IN METAL OXIDE-BASED HIGH-*K* GATE DIELECTRICS

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Abstract. Processing of ultra-thin high-k metal oxide films (e.g. HfO_2) for use in semiconductor devices requires exposure of these materials to potentially-reactive solids and to both reducing and oxidizing ambients at elevated temperatures. This often results in structural changes within the high-k layer, and formation of interface defects. This paper describes the thermodynamics of point defect equilibrium in HfO_2 and related materials, including effects of oxygen partial pressure, internal interfaces, and contact with adjacent metal layers. Thermodynamic analysis is useful in predicting trends and driving forces for defect formation. Experimental results on point defect reactions and structural changes during thermal processing are reviewed. Implications for properties of MOS devices containing high-k metal oxides are discussed.

Keywords: point defects, thermodynamics, size effects, crystallization, HfO_2

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1. Introduction

Point defects form in high permittivity, metal oxide-based, dielectric films because of the ionic character of their bonding, their large cation coordination numbers[1] and their propensity to 1) contain impurity ions and 2) to equilibrate with the surrounding oxygen pressure during high temperature processing.[2] Point defects are electrically significant because they can ionize. Electrically active point defects present in high-k metal oxide films may affect the conduction band-offset of the gate metal and the fixed charge density in the gate stack. The former property alters the gate leakage current density, whereas the latter influences the threshold voltage and carrier mobilities in the channel of a MOS transistor. Ionized defects can trap electronic carriers, which adversely affects threshold voltage stability.

Processing of ultra-thin high permittivity metal oxide films in semiconductor devices results in exposure of these materials to potentially-reactive solids and to both reducing and oxidizing ambients at elevated temperatures. Point defect reactions may occur as a result. In extreme cases,[3] changes in metal:oxygen stoichiometry accompanying such processes becomes so severe that undesired interfacial chemical reactions between the high-k layer and adjacent materials will take place during device fabrication. This may result in defect-induced pinning of the potential barrier between the materials4 or decomposition of the high-k film itself.[5]

A more thorough understanding of point defect phenomena in high-k thin films that goes beyond the energetics of defect formation and encompasses electrostatic effects at crystallographic interfaces and the influence of adjacent layers is desirable. This paper reviews the thermodynamics of point defect equilibration in HfO_2 and related materials, including effects of oxygen partial pressure, proximity to interfaces, and contact with adjacent metal layers. The understanding of defect equilibria in nanocrystalline ZrO_2, CeO_2 and other fluorite-structure metal oxides that has emerged in the solid state ionics community in recent years guides much of this discussion. Although high-k film deposition and post-deposition thermal treatments may take place far from equilibrium, thermodynamic analysis is useful in predicting trends and driving forces for defect formation. Experimental results on suggestive of point defect reactions and interface structure changes are reviewed. Implications of such findings for the properties and reliability of high-k MOS devices are discussed

2. Point Defect Equilibrium in Nanocrystalline, Fluorite Structure – Based, Metal Oxides

2.1. EQUILIBRIUM FROM BULK TO INTERFACE

The bulk point defect chemistry of ZrO_2 and CeO_2 is now relatively well-understood. Although less well-studied, defect equilibrium in chemically-similar HfO_2 can be inferred from what is known of these other compounds. These are materials with a tendency toward oxygen deficiency.[6] As a result of their relatively close-packed crystal structures (especially the tetragonal and cubic forms), vacancy defects dominate. Oxygen vacancies will have much lower formation enthalpies than cation vacancies because of the oxygen ion's lower coordination in fluorite-structure metal oxides. Similarly, the migration rates of cation vacancies will, except near the melting point, be orders of magnitude less than those of oxygen vacancies. Therefore, substitutional cation impurities present in fluorite-based metal oxides can be assumed to be "frozen-in" at all temperatures of technological interest.

In large bandgap (Eg ~ 6 eV), ionic crystals such as ZrO_2 and HfO_2, impurity ions often are electrically compensated by point defects rather than by electronic carriers.[6] This is the case for acceptor impurities (subvalent metals such as Y3+ and Ca2+) which sit on Zr sites in cubic ZrO_2. Because these impurities are often highly-soluble, they can produce very large concentrations of charge-compensating oxygen vacancies. This has been exploited technologically in galvanic oxygen sensors and fuel cell membranes made from yttria-stabilized ZrO_2 (YSZ) oxygen fast ion conductors.[7]

Oxygen exchange between the vapor and the crystal is governed by the redox reaction (written in Kröger-Vink notation[7]):

$$O_O^x \leftrightarrows \tfrac{1}{2}\, O_2 + V_O^{\cdot\cdot} + 2e', \qquad (1)$$

where O_O^x is an oxygen ion present on an oxygen site and $V_O^{\cdot\cdot}$ is a doubly-ionized oxygen vacancy. Ionization of oxygen vacancies produces donor-type defects and conduction electrons. Depending on the position of the Fermi energy relative to the defect states associated with oxygen vacancies, these defects can be either neutral (V_O^x), singly-ionized ($V_O^{\cdot}$) or doubly-ionized. The ionization energies of oxygen vacancies can be estimated from electronic structure calculations on cubic ZrO_2,[8] optical absorption data from ZrO_2 films[9] and spectroscopic ellipsometric measurements of thin film HfO_2[10] to be ~ 2 eV. The free energy change for reaction (1) has been measured from the high temperature, variable-$P(O_2)$ electrical conductivity of the metal oxide, or it has been inferred from measurements of the equlibrium $P(O_2)$ above the oxide at

varying temperature. Redox reaction enthalpies are typically reported to be range 4 – 6.5 eV per oxygen ion for CeO_2 and the various phases of ZrO_2.[11-13]

Near crystallographic interfaces, such as grain boundaries and surfaces, equilibrium concentrations of point defects can vary greatly from the bulk values. In the bulk, local electroneutrality sets the concentration of the majority charged species (e.g. $[Y_{Zr}'] \cong 2[V_O^{\bullet\bullet}]$ in YSZ), whereas point defect concentrations near the interface are determined by exchange of ions between lattice and interface sites. This fact, which was apparently originally recognized by Frenkel,[14] has been the basis for many subsequent analyses of near-interface defect equilibria in ionic solids.[15-17] Equilibrium of an acceptor impurity-containing ionic crystal with a propensity to form oxygen vacancies is depicted schematically in Fig. 1. Local charge neutrality is violated near the interfaces at equilibrium, leading to a space charge region and an equilibrium electrostatic potential difference between the interface and bulk.[14] Global charge neutrality occurs because interface charge (charge trapped in interface states) balances the near-interface space charge, thus screening the "built-in" electric field produced by the space charge.

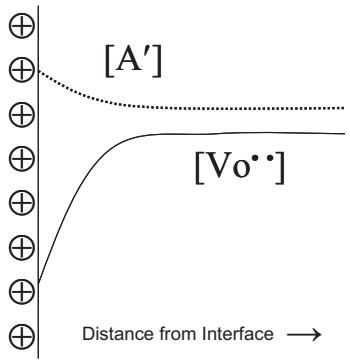


Figure 1. Schematic illustration of the (log) equilibrium oxygen vacancy and acceptor ion concentrations near a surface or grain boundary in an ionic crystal. In this sketch, it is assumed that both defect concentrations can reach equilibrium with the interface, which is unlikely for acceptor cations in MeO_2 oxides.

In Fig. 1, $[V_O^{\bullet\bullet}] << [A_{Zr}']$ at the interface because the process of oxygen ion exchange between lattice and interface,

$$O_O^x + (V_O^{\bullet\bullet})_{int} \leftrightarrows (O_O^x)_{int} + V_O^{\bullet\bullet}, \qquad (2)$$

(Fig. 2), will generally produce an equilibrium vacancy concentration that is very small relative to the impurity concentrations. Common metals in the earth's crust (e.g. Fe and Al), produce acceptor defects when they substitute on cation sites in MeO_2 oxides. Such defects can be present in concentrations of 100 ppm – 10% depending on solubility, far larger than the equilbrium near-interface value of $[V_O^{\cdot\cdot}]$. The energetics of the exchange reaction described by equation (2) and schematically illustrated in Fig. 2(b) can be estimated crudely from Me-O bond enthalpies. For example, for O^{2-} in tetragonal ZrO_2, movement from a lattice site to a surface or grain boundary kink site requires the breaking of two Zr-O bonds, an energetic penalty of ~ 5 eV. However, this simple estimation neglects next-neighbor interactions and, in particular, structural relaxation effects which appear to be significant for vacancies in these materials.[18] Considering these effects may reduce the estimated oxygen ion exchange enthalpy by 1 eV or more.

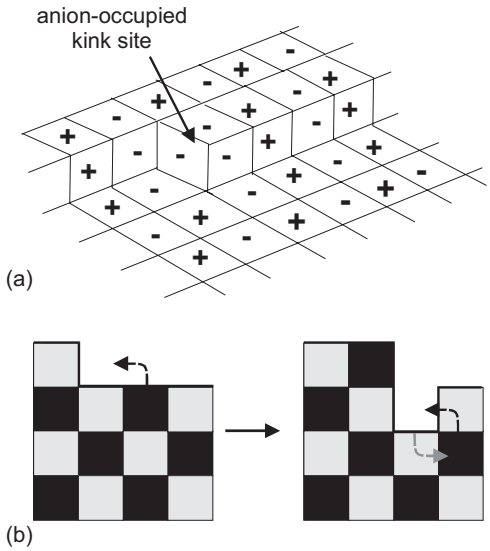


Figure 2. (a) Terrace-ledge-kink picture of an ionic crystal interface; kink sites are energetically-preferred locations for vacancy formation and annihilation. (b) Exchange of an ion from the lattice to an interface kink site produces a lattice vacancy which can diffuse into the crystal.

One can calculate the equilibrium defect and electronic carrier concentrations as a function of position with respect to the interface. Local point defect distributions and the equilibrium electrostatic potential distribution are obtained by numerical solution of the Poisson equation, where the various charged defect concentrations are related through the multiple mass action equations which

stem from the simultaneous defect equilibria (redox, ionization, ion exchange between lattice and interface, etc.). Readers interested in the details of the methodology are referred to a previous publication in which such calculations were performed for acceptor-doped $SrTiO_3$.[17]

2.1.1. *Acceptor Impurity-Containing ZrO_2*

Results of a calculation of local defect and carrier equilibrium near an interface in acceptor impurity-containing tetragonal ZrO_2 are shown in Figure 3. Input into the calculation were the free energy change of reaction (1), 5.7 eV,[12] that of reaction (2), 4 eV (estimate), and the energy change (2.5 eV[4]) for the vacancy ionization equilibrium. A constant acceptor ion fraction (fully ionized) of 100 ppm relative to the Zr-site concentration and a simulation temperature of 1000 K were also assumed. This calculation did not address the effects of the entropy of mixing of oxygen vacancies and oxygen ions in the interface.[19] Therefore, the results are only reasonable in the limit of relatively modest interface charge densities, or $[(V_O^{\bullet\bullet})_{int}]/[(O_O^{x})_{int}] \leq 0.01$, approximately. This condition is satisfied for all the simulation results described in Figures 3 and 4.

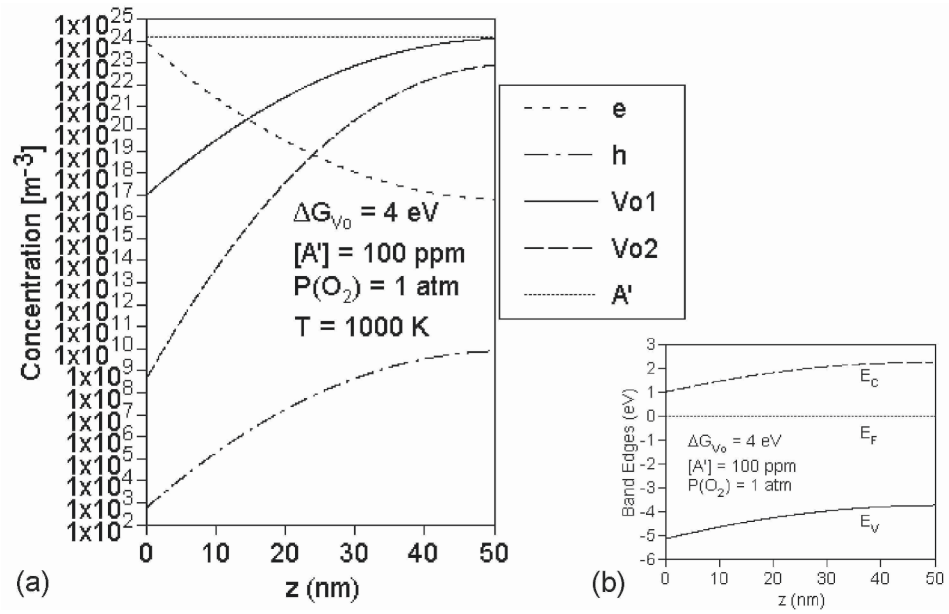


Figure 3. (a) Predicted equilibrium point defect and carrier distributions as a function of distance (z) from a crystallographic interface in *tet*-ZrO_2; *Vo1* = singly-ionized and *Vo2* = doubly ionized oxygen vacancies, respectively. (b) Corresponding band edge profiles near the interface (Fermi energy = 0).

Figure 3 indicates that a pronounced depletion of oxygen vacancies is predicted at equilibrium near grain boundaries and surfaces in acceptor-containing tetragonal ZrO_2. Given their chemical and structural similarities, a similar picture would be expected for other ZrO_2 phases and for HfO_2. Negative space charge produced near the interface by uncompensated acceptor impurities is balanced by positive charge on the interface. The varying equilibrium electrostatic potential between bulk and interface leads to a near-interface electron accummulation. Increasing the acceptor impurity concentration, increasing the simulated temperature, or decreasing the $P(O_2)$ compared to the situation in Fig. 3 tends to increase the predicted magnitude of the potential difference between interface and bulk, as well as the magnitude of the interface charge. The distance from the interface over which defect concentrations differ significantly from bulk values is ~ 50 nm for the situation simulated. This is substantially larger than the Debye length, a result[20] of the assumption of immobile A′ far below the melting point of the oxide.

The situation in Fig.3 is similar to that expected in acceptor impurity-containing nanocrystalline MeO_2 ceramics (Me = Ce, Zr). In fact, a form of this interface equilibrium simulation has been used with success recently[20] to explain the observed temperature- and $P(O_2)$-dependence of the dc electrical conductivity and ac impedance spectra[11] of nanocrystalline CeO_2.

2.1.2. *Donor Impurity-Containing ZrO_2*

Many of the impurities introduced in thin film processing are expected to have donor character in metal oxide crystals such as ZrO_2 and HfO_2. Possible examples include $Cl_O^{\bullet}$, an important impurity species in ALD-grown high-*k* films, and $H_i^{\bullet}$, hydrogen interstitial defects.[21] Figure 4 shows the results of a near-interface equilibrium calculation for donor-impurity (D*) containing *tet*-ZrO_2. The temperature, $P(O_2)$, and bulk dopant concentration are the same as for the acceptor calculation already described. Unlike the acceptor case, the donor impurity is assumed to be sufficiently mobile to reach equilibrium with the interface and the other charged species in the crystal.

For the conditions in Fig. 4, the electrostatic potential difference between bulk and interface is very small (< 0.05 V) and opposite in sign to the acceptor case shown in Fig. 3. Relatively few oxygen vacancies are predicted at equilibrium. The crystal is predicted to exhibit strongly n-type electronic conduction at all locations relative to the interface. The distance over which defect and carrier concentrations differ (slightly) from their bulk values is ~ 20 nm.

For many simulation conditions of interest, the sign of the potential difference is opposite to that shown in Fig. 4 (ie. $V_O^{\bullet}$ and $V_O^{\bullet\bullet}$ depletion rather than accummulation near the interface), but it is generally smaller in magnitude than for the acceptor case. Increasing the simulated temperature or decreasing the $P(O_2)$ compared to the situation in Fig. 4 tends to increase the predicted magnitude of the potential difference between interface and bulk, as well as the magnitude of the interface charge. It also tends to produce oxygen vacancy depletion near the interface as in Fig. 3. Increasing the donor concentration has the opposite effect because it increases the bulk electron concentration and,

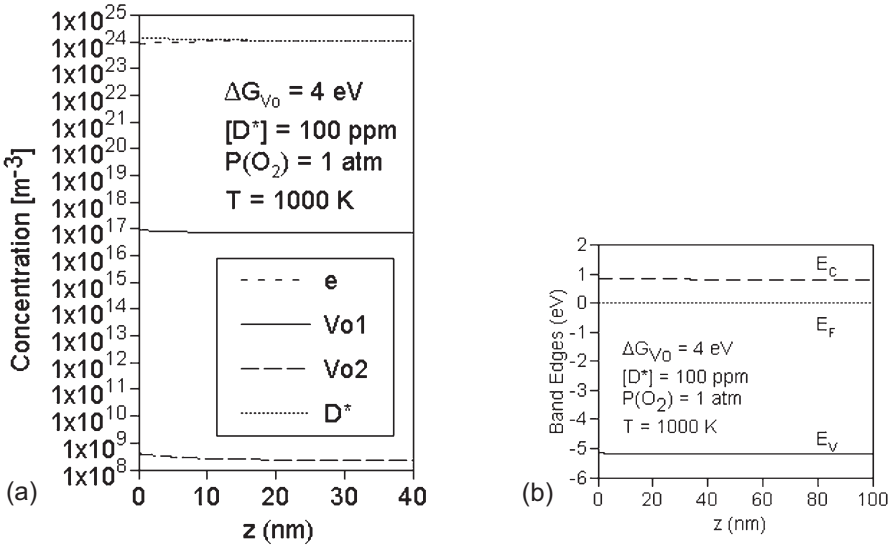


Figure 4. (a) Predicted equilibrium point defect and carrier distributions as a function of distance (z) from an interface in donor-containing *tet*-ZrO_2. (b) Corresponding band edge profiles near the interface (Fermi energy = 0).

through the mass action relation for reaction (1), reduces the bulk value of $[V_O^{\bullet\bullet}]$. This brings the simulated bulk vacancy concentration closer to the interfacial equilibrium value for reaction (2), implying a smaller value of the bulk-to-interface potential difference.

3. Implications for High-*k* Thin Films

Size scale and crystallinity are important factors which will influence the applicability of the forgoing results. High-*k* metal oxide gate dielectrics for advanced MOS devices are no more than a few nanometers in thickness. HfO_2

films, for example, are often amorphous as-deposited but are generally reported[22, 23] to crystallize into the monoclinic phase during subsequent annealing at temperatures around 800 K. These crystallites span the film thickness and have lateral sizes that may be several times the film thickness.[23] However, they are still typically much smaller than the distance scale over which pronounced interface effects on defect equilibrium are predicted. Considering the length scales depicted in Fig's 3 and 4, an equilibrated nanocrystalline high-*k* film in which acceptor impurities are predominant that is deposited on SiO_2-passivated Si would be expected to exhibit a pronounced depletion of oxygen vacancies relative to the bulk crystal. A large, positive interface charge (10^{16} – 10^{17} m^{-2} for reasonable doping levels and modest oxygen partial pressure) located along grain boundaries and the film surface, would also be expected at equilibrium. In contrast, donor doping may produce either negative or positive grain boundary/surface charge at equilibrium, depending upon the dopant concentration and other factors. Donor doping will, however, also lead to relatively low oxygen vacancy concentrations at equilibrium. One is left with the somewhat surprising conclusion that, in spite of the tendency toward oxygen deficiency of the bulk crystals, interface effects should produce relatively low oxygen vacancy concentrations (generally, $< 10^{18}$ m^{-3}) in bare and equilibrated, crystalline high-*k* films of useful thickness.

3.1. FERMI LEVEL PINNING

Pinning of the Fermi level at poly-Si/HfO_2 interfaces is a serious problem[24] for integration of high-*k* films with the currently-standard MOS gate electrode. It has been suggested[4] that formation of a high density of oxygen vacancies in HfO_2 films is responsible for this pinning effect. Given their energies in the upper portion of the HfO_2 bandgap,[8-10] a sufficiently high density of interface states associated with oxygen vacancies near the HfO_2 surface may pin E_F in the gap of the Si electrode. In fact, the calculations in Section 2 above suggest a mechanism by which such large gate /high-*k* interface state densities may form.

Poly-Si deposition is typically performed using a CVD process with silane or a related reactive Si precursor gas diluted in H_2. Such a process has a very low effective $P(O_2)$. Point defect simulations which mimick such conditions suggest that, either for acceptor or donor doping, a nanocrystalline ZrO_2 film will exhibit a large, positive surface potential relative to the bulk and a very large ($>10^{18}$ m^{-2}), positive surface charge density at equilibrium. A high density of donor-type surface states (likely, surface oxygen vacancies) would be required to achieve equilibrium between nanoscale crystallites and the surface under such reducing conditions. Complete equilibration with a CVD ambient

would note likely occur in the brief time before the film surface is coated with Si (thus blocking the film from the vapor). However, the simulations suggest that a driving force exists to modify the surface of the film in a way that is consistent with Fermi level pinning. In order to test this possibility, careful measurements of the surface potential of high-*k* films as a function of vacuum and H_2 exposure conditions would be useful.

In ref. 4, an alternative explanation for the Fermi level pinning which involves oxygen vacancies in HfO_2 is proposed. Takeuchi et al. consider the possibility that electrons generated during oxygen vacancy formation in HfO_2 may be trapped at the vacancy electronic state itself or they may be emitted into the gate metal. They argue in effect, as did Shiraishi et al. previously,[25] that the potential energy decrease for the electrons should lower the standard enthalpy of reaction (1), thus providing a driving force ($\Delta G° < 0$) for the reaction

$$Si_{(s)} + 2O_O^x \leftrightarrows SiO_{2(s)} + 2V_O^{\bullet\bullet} + 4e'. \qquad (3)$$

Their idea is inconsistent with the requirement that standard enthalpies and free energies of reaction apply for species in their standard states (e.g. conduction electrons in the conduction band of the metal oxide crystal). The state of ionization of the vacancy and the equilibrium electron concentration in a HfO_2 layer in contact with a gate metal layer will indeed be altered by the presence of an adjacent metal. These effects result from the equilibration of the chemical potential of electrons (E_F) in the system and thus will determine the equilibrium constants, but **do not** change $\Delta G°$ of reaction (1) or reaction (3). Therefore, $\Delta G°$ of reaction (3) is positive for *tet*-ZrO_2, for example.[3] It is true, however, that gate metals which have less affinity for oxygen than do Hf or Zr should be good choices on thermodynamic grounds, as Takeuchi et al. point out.[4]

3.2. FIXED CHARGE

A detailed description of fixed charge in high-*k* dielectric films should include both charges at the high-*k*/metal interface and the high-*k*/substrate interface, and how these interfaces interact with point defect populations and grain boundary states in the film. If one considers a nanocrystalline MeO_2 film in isolation, the net fixed charge in it is zero at equilibrium, as the grain boundary and surface charges will cancel the space charge within the grains.

Figure 5 compares capacitance-voltage plots obtained from ALD-HfO_2 films after *in-situ* post-deposition anneals performed in the ALD reactor at low pressure.[26] The annealing conditions did not result in any growth of the

underlying, 1.5 nm thick SiO_2 interface layer, as confirmed by transmission electron microscopy. Previously-reported,[23] *ex-situ* N_2 annealing studies on similar films indicated that anneals above 500°C produced a systematic shift of the flat band voltage, consistent with creation of positive fixed charge, and the appearance of pronounced, mono-energetic interface state prior to forming gas anneal. This is not the case for the *in situ* anneals, suggesting that an O_2 impurity in the *ex situ* anneal ambient (which was found to produce SiO_2 growth above 600°C even for 2.5 nm thick initial interface layers) was influencing those results. Instead, the *in-situ* data show no systematic effect of annealing, and, thus, the extent of HfO_2 crystallization, on fixed charge. A subsequent 400°C forming gas anneal shifts the CV curves systematically to a ~ 200 mV lower flat band voltage and reduces the CV hysteresis and stretch-out.

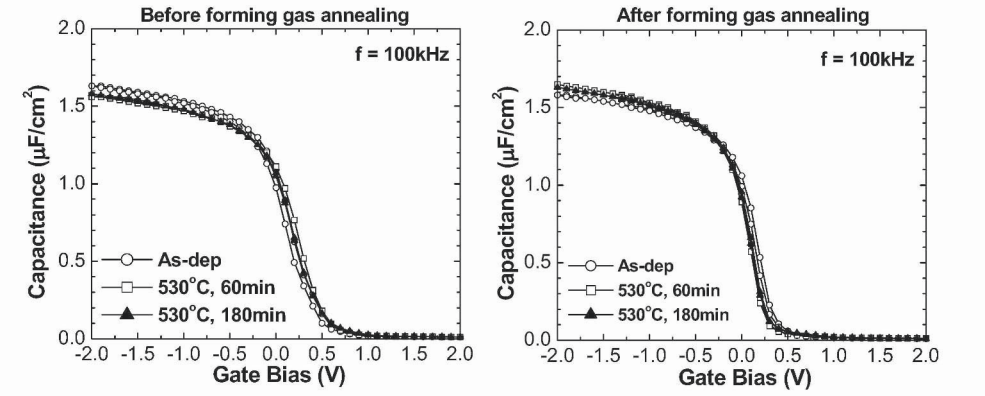


Figure 5. 4 nm ALD-HfO_2 films on 1.5 nm SiO_2/p-type Si substrates annealed *in-situ* after deposition in 1.3 Torr of N_2 before and after 1 atm H_2 4%/N_2 anneal at 400°C. Films were amorphous as-deposited, partially-crystalline after 60 min *in-situ* anneal at 530°C, and fully-crystalline after 180 min.

These data are consistent with the expectation that zero net fixed charge should accompany equilibration of defects in nanocrystalline ceramic films that are electrostatically-isolated from the substrate and have no overlying metal layer. It is not obvious that the same condition of zero net space charge after point defect equilibration will hold when a contacting gate electrode is present at high temperatures. More significantly, spatially-periodic changes in negative space charge and positive grain boundary charge in polycrystalline high-*k* films would likely enhance remote Coulomb scattering of carriers in the transistor channel.[27] Therefore, if crystalline metal oxides are required for achieving sufficiently high dielectric constants, substantial effort must be devoted to measuring and controlling their charged point defect concentrations and grain boundary states.

4. Conclusions

Point defect equilibrium in nanocrystalline films of fluorite- and related-structure (e.g. ZrO_2 and HfO_2) high-*k* metal oxides was examined quantitatively and the following conclusions can be reached:

a) Reasonable concentrations of both donor and acceptor impurities are predicted to produce a significant deficiency of oxygen vacancies within the grains of nanocrystalline films at equilibrium relative to the situation in bulk crystals.

b) For most simulation conditions of practical interest, substantial negative space charge in the grains and positive grain boundary and surface charge densities are predicted. These charges should cancel in films that are electrostatically-isolated from their surroundings, consistent with recent experimental data obtained after *in-situ* crystallization anneals of ALD-HfO_2.

c) Under the highly-reducing conditions typical of poly-Si CVD, the simulations suggest a very high density of donor-type surface states (positive interface charge) at equilibrium. These surface defects may be responsible for the reported Fermi level pinning at the poly-Si/HfO_2 interface.

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DISORDERED STRUCTURE AND DENSITY OF GAP STATES IN HIGH-PERMITTIVITY THIN SOLID FILMS

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Abstract. Metal-oxide-semiconductor structures based on high-permittivity dielectric thin films of HfO_2, ZrO_2, Al_2O_3, TiO_2, Ta_2O_5, and Nb_2O_5, were subjected to capacitance-voltage and conductance transient measurements as well as deep level transient spectroscopy studies. The measurements have revealed correspondence between film growth temperature, crystallinity, residual contamination and gap-state densities arising from structural disorder. The measurements have also revealed higher stability and lower defect densities in the group III and IV metal oxide films, compared to group V metal oxides.

Keywords: atomic layer deposition, gap states, defects, capacitance transients, conductance transients, transition metal oxides, dielectrics

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1. Introduction

SiO_2 and SiON dielectrics have been of major importance in the microelectronics, forming electronically and structurally high-quality interface in field effect transistors with silicon based channels. Alternative metal oxide dielectrics, such as HfO_2, $HfSiO_4$, $HfSiO_xN_y$, $HfAlO_x$, ZrO_2, would enable the exploitation of thicker layers without loss in capacitance density, compared to SiO_2. HfO_2 based dielectrics have been accommodated to nanoelectronic devices.[1] At the same time, the devices based on metal oxides lack of commensurate junction between silicon and insulator, and possess graded chemical and structural composition in the vicinity of the junction. Defects and related charge traps at oxide/semiconductor interfaces and inside the dielectric bulk affect the performance and reliability of gate oxides.[1,2]

Defects can be investigated by several methods such as measuring gate current transients,[3] hysteresis width of capacitance-voltage (C-V),[4] electron tunneling spectra,[5] relations between bias voltage, corresponding capacitance dependence and maximum dielectric loss,[6] transient capacitance[7] and deep level transient spectra (DLTS).[8] Not too many studies compare the defect densities in different materials obtained by the same deposition technique and/or using the same measurement technique. In some papers, interface trap densities, D_{it}, between Si substrate and HfO_2 atomic layer deposited (ALD) or chemical vapor deposited (CVD) either from $Hf[N(C_2H_5)_2]_4$ or $Hf(NO_3)_4$ have been measured using electron-spin resonance,[9,10] capacitance-voltage[9] and ac conductance spectroscopy.[10] Structural differences between films grown in these processes have not been described in detail. Instead, the choice of precursors enabling either chlorine-free or both carbon- and chlorine-free deposition routes was considered as the most relevant issue. D_{it} has increased from films grown above 300 ºC in $HfCl_4$-based ALD over $Hf[N(C_2H_5)_2]_4$-based CVD to $Hf(NO_3)_4$-based CVD.[11] It has also been shown, that interfacial Si dangling bond defects (P_{b0}, P_{b1}) affect the quality of dielectric stacks, ZrO_2 and Al_2O_3, and the ultrathin SiO_2 interlayer would be advantageous in terms of interface defect density reduction.[12]

We have estimated the density of defects both at the oxide-silicon interface and inside the ALD oxides measuring C-V curves, conductance transients, and deep level transient spectra. We have studied dielectric layers based on HfO_2, $HfSiO_x$, Ta_2O_5, Nb_2O_5, $Zr_xAl_yO_z$, TiO_2 and Al_2O_3. The rechargeable, disorder-induced, trap densities could depend on whether metal alkylamides, iodides or chlorides are used in the process carried out at comparable temperatures at 300 ºC or lower. This study, although not exhaustive, aims at the description of defective nature of these oxides and their interfaces to silicon against a) impurity level and b) structural disorder and crystallographic inhomogeneity.

2. Experimental details

2.1. FILM GROWTH

The dielectric layers were in most cases grown on etched silicon after removal of native SiO_2 1 % HF aqueous solution (20-30 s dipping time), since the SiO_2/Si(100) substrate would restrict the charge transfer between substrate and oxide due to the high-band gap SiO_2 interlayer. HfO_2 films were grown on HF-etched Si(100) using $HfCl_4$ and H_2O as precursors either in a commercial F120 type ALD reactor[13] or in an open-type ALD reactor with calibrated H_2O partial pressure.[14,15] Another halide-based route to HfO_2 has been the growth from HfI_4 and H_2O.[13] Additionally, HfO_2 films have been deposited in the F120 reactor from $Hf[N(C_2H_5)(CH_3)]_4$ and H_2O[16,17] on Si substrates covered by chemically grown SiO_2 (RCA clean). Further, mixtures and nanolaminates of HfO_2 or ZrO_2, Al_2O_3 and Nb_2O_5 have been deposited on HF-etched Si using chlorides of Hf and Zr, $Al(CH_3)_3$ and $Nb(OC_2H_5)_5$ with H_2O.[18,19] Some Al_2O_3 samples were deposited using $AlCl_3$ and H_2O. Hafnium-rich mixtures of HfO_2 and SiO_2[20] were grown as well, using the precursor chemistry based on $HfCl_4$ or HfI_4 and $Si(OC_2H_5)_4$, suitable for silicate growth.[21] Reference Ta_2O_5 and Nb_2O_5 films and their stacks were grown using $Ta(OC_2H_5)_5$, $Nb(OC_2H_5)_5$ and H_2O as precursors[18,22,23] on HF-etched Si. Finally, TiO_2 films were grown on HF-etched Si from $Ti(OC_2H_5)_4$ and H_2O.[24]

2.2. ELECTRICAL MEASUREMENTS

All the metal-oxide-semiconductor (MOS) samples were created by evaporation of nearly-ohmic Al contact on backside of Si substrates and an array of Al dot (gate) electrodes with 0.204 mm^2 surface area. Conductance transients[25] could be measured on n-type (p-type) Si substrates after applying positive (negative) bias voltage pulses sweeping MOS capacitors from deep to weak inversion. Concurrently, capturing of charge carriers by empty disorder-induced gap states (DIGS),[26] emitted from the Si conduction band, takes place. This proceeds via tunnelling and requires some characteristic time, while states closer to the interface capture electrons faster than those farther away from the interface towards bulk. The rate of charging traps in the band-gap is measured. Traps with the emission and capture rates corresponding to the measurement frequency effectively contribute to the conductance, and can be correlated to the certain energetic distance from the band edge. At the beginning of the transient process the front of tunneling electrons is close to the interface and the states capturing and releasing electrons have emission rates much higher than the frequency and do not contribute to the conductance. In general and at arbitrary

frequency, trap states will contribute to the conductance, when the traps are located at distance from interface (induced by disorder in oxide) and in suitable depth, enabling response time corresponding to the signal frequency, $\omega \pm \Delta\omega$, of the ongoing measurements. Conductance signal goes through maximum in this small frequency range and the eventual conductance value is proportional to the density of states. Since the emission rate is a function of temperature, the rate of transient changes with sample temperature. Applying the measurement temperature and frequency as parameters, it becomes possible to three-dimensionally map[27] the apparent densities of defect states as function of distance to interface in length units (Å, nm) and to semiconductor conduction or valence band edges in energy units (meV). High-frequency (1MHz) measurements are performed when the fast traps at the very interface, D_{it}, are to be detected in DLTS regime. Structural DIGS and interface trap densities, D_{it}, cause capacitance-voltage hysteresis,[26] flat-band voltage shifts,[28] band tails in optical absorption spectra,[29] and are a probable source of tunnelling and trap-assisted conduction current[23] and the related dielectric breakdown.[30]

3. Results and discussion

3.1. CAUSES OF STRUCTURAL DISORDER

The films were grown from precursors and at temperatures which have provided appreciably high density, relatively high crystallinity and/or low residual contamination level in the earlier studies. The properties of the resulting films are compromise between purity, density of structure defects, reactivity and thermal stability of the precursors. For instance, HfO_2 films grown from $HfCl_4$ and H_2O at 300 ºC contain observable amounts of residual hydrogen and chlorine (0.5-1.5 at.%) while the impurity content rapidly decreases with increasing growth temperature.[14,15] The substrate temperature 300 ºC is also within the critical range initiating crystal growth intensifying towards higher growth temperatures. Reflections from different polymorphs can be seen.[15,19] The impurity content tends to enhance at oxide/semiconductor interfaces,[31] probably due to the lattice being most distorted and open in the vicinity of interfaces as well as the impurities bonding to the substrate. Changes in structural disorder can stem from the changes in the film growth mechanism. The most conventional HfO_2 ALD mechanism is recognized as a sequence of fast exchange reactions between adsorbing $HfCl_4$ and OH-terminated Si surface.[14] At relatively low substrate temperatures (< 300-350 ºC) the density of OH-groups is high and, consequently, also the nucleation density is high. However, also the residual OH-content increases. At higher temperatures (> 300 ºC), surface dehydroxylates more efficiently during purge periods and the

fast nucleation of crystallites may occur due to OH-groups more separated from each other, assisted by surface migration also enhanced by temperature. Formation of agglomerates then precedes continuous growth. Henceforth the defective grain boundaries are formed.[32]

Al_2O_3, Ta_2O_5 and Nb_2O_5 remained completely amorphous. Al_2O_3 as more covalent material compared to HfO_2 does not demonstrate long-range ordering unless growth temperature is increased above 700-800 ºC. Ta_2O_5 and Nb_2O_5 do not crystallize when grown from alkoxides probably due to kinetic reasons. Low growth temperatures are required, because the alkoxides start do decompose intensely at 300-350 ºC. Alkoxides (ethoxides) are otherwise suitable precursors for TiO_2, Nb_2O_5 and Ta_2O_5 growth providing uniform, quite dense and chlorine-free films. By contrast, alkoxides are quite poor ALD precursors of HfO_2 and ZrO_2, resulting in nanocrystalline films with high hydrogen and carbon content in as-deposited state, demonstrating wide C-V hysteresis, distorted C-V curves due to deep interface traps, and the hysteresis direction changed from counterclockwise to clockwise likely due to mobile ion (H^+) conduction.[33] In this study, alkoxide-processed HfO_2 will not be dealt with.

3.2. HfO_2 GROWN FROM HALIDE PRECURSOR

Fig. 1 exemplifies the three-dimensional DIGS plots[34] as results obtained in studies on HfO_2 grown from $HfCl_4$ and H_2O.[35-37] DIGS are denser in as-deposited films and decrease after heat-treatment. DIGS densities have been higher in HfO_2 films on HF-etched Si,[36] compared to films on RCA cleaned Si substrates (Fig. 1). DIGS densities in the films as-deposited on SiO_2/Si and annealed on HF-etched Si have been very similar, suggesting that interface SiO_2 layer may regrow and additional densification of HfO_2 layer can take place upon annealing, increasing the electronic quality. Inhomogeneous nucleation of HfO_2 at 450-600 ºC [32] is the probable reason for the D_{it} increasing with growth temperature (Table 1). However, impurity level decreases with increasing temperature and HfO_2 is probably quite stoichiometric inside the grains or crystallites. Consequently, DIGS densities may become reduced in the films grown at higher temperatures (Table 1).[3]

Around critical temperatures at 300 ºC, where films with thicknesses not exceeding 5 nm can remain amorphous, the crystal growth can be initiated by controlling the oxygen precursor (H_2O) dose, although the film purity is not affected noticeably by H_2O pressure.[15] Table 2 indicates, that the film thickness and H_2O pressure may have a little effect on D_{it}. DIGS density may be more affected by crystallinity, thickness and also the growth temperature.[37]

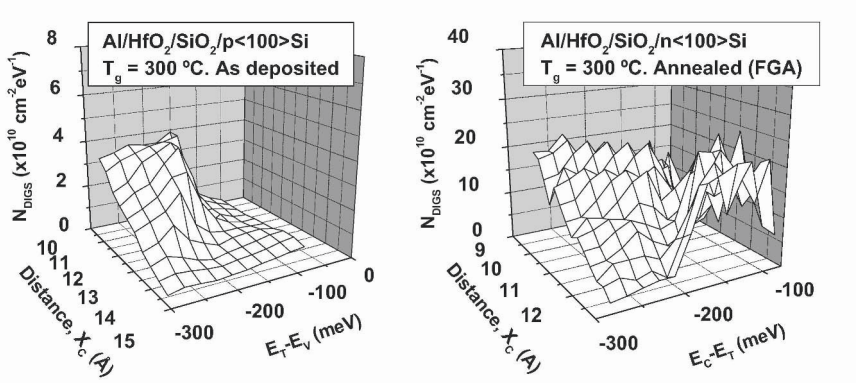


Figure 1. Three-dimensional DIGS plots of selected as-deposited and forming gas annealed (30 min at 400 ºC) HfO_2 films.

Table 1. D_{it}, and maximum DIGS density of Al/HfO_2/Si MOS structures with as-deposited HfO_2 films grown in $HfCl_4$-H_2O ALD process. HfO_2 thickness is denoted by d_{HfO2}.

T_R	d_{HfO2}	HF-etched substrate	D_{it}, $cm^{-2}eV^{-1}$	$DIGS_{max}$, $cm^{-2}eV^{-1}$
300 °C	25 nm	p-Si(100)	$0.4\text{-}0.6 \times 10^{11}$	6×10^{10}
500 °C	190 nm	p-Si(100)	$1\text{-}2 \times 10^{11}$	2.8×10^{10}
600 °C	121 nm	p-Si(100)	6×10^{12}	3.5×10^{10}

Table 2. D_{it} and maximum DIGS values in Al/HfO_2/Si MOS structures with HfO_2 films as-deposited in $HfCl_4$-H_2O ALD process on HF-etched p-Si(100) at 300 ºC. H_2O partial pressure during the growth and film thickness are denoted as p_{H2O} and d_{HfO2}, respectively.

T_R	p_{H2O}	d_{HfO2}	crystallinity	D_{it}, $cm^{-2}eV^{-1}$	$DIGS_{max}$, $cm^{-2}eV^{-1}$
300 °C	12 Pa	8.7 nm	crystalline	$3\text{-}7 \times 10^{10}$	9×10^{10}
300 °C	3 Pa	8.3 nm	crystalline	1×10^{11}	3×10^{10}
300 °C	12 Pa	4.1 nm	amorphous	1×10^{11}	not detected
300 °C	3 Pa	3.7 nm	amorphous	$1\text{-}3 \times 10^{11}$	not detected

3.3. HfO_2 GROWN FROM ALKYLAMIDE PRECURSOR

The films grown from $Hf[N(CH_3)(C_2H_5)]_4$ contained hydrogen (3-6 at.%), nitrogen (1-2 at.%) and carbon (1 at.%).[16] D_{it} most clearly correlated to the content of residual hydrogen, which in turn depends on the content of hydrogen in precursor chemicals. D_{it} values for amorphous[17] 4.6, 4.3 and 4.8 nm thick films grown on SiO_2-covered p-Si(100) from $Hf[N(CH_3)(C_2H_5)]_4$ at temperatures 205, 235 and 300 °C were 2×10^{12}, 3×10^{11}, and $1\text{-}2\times10^{12}$ $cm^{-2}eV^{-1}$, respectively. The hydrogen content in these films was correspondingly 3±1, 2±1, and 2.5±1 at.%.

Even when the films were grown on SiO_2/Si substrates with 1.2-1.8 nm thick SiO_2 chemical oxide, high hydrogen contents may affect the interface. Defect states can form due to H diffused and loosely bound to sites in the SiO_2 network at the interface.[38] Hydrogen is also able to create defect states in the high-k film bulk.[39] In such cases, hydrogen must be at least partially annealed out by post-deposition heat-treatment but the interface quality may still remain influenced by the synthesis process and sample history. In this study the effect of bulk hydrogen to the disorder induced states could not be estimated due to the presence of wide-band gap SiO_2, effectively inhibiting the exchange between substrate and oxide charge. An additional impurity detected – nitrogen – arising from alkylamide ligands[16] could probably increase interface trap densities in upper part and passivate the H-related defects in the lower part of Si band gap.[40] The effect of carbon is not quite known.

3.4. MIXTURES AND SOLID SOLUTIONS

Al_2O_3/Si structures have shown relatively low, but stable capacitance and low leakage current density. D_{it} has been comparable to that in HfO_2/Si structures, and DIGS density been even lower (Table 3). Mixing HfO_2 with Al_2O_3 has caused amorphization already in the case of low Al contents[18] and dramatically reduced leakage current density, compared to HfO_2[20] and even to $HfSiO_x$.[41] In both $ZrAl_{0.7}O_3$ and $HfAl_{0.7}O_3$, interface and oxide defect densities become lower than in HfO_2 grown from $HfCl_4$ (Table 3).[42]

3.5. OXIDES OF TANTALUM, NIOBIUM AND TITANIUM

TiO_2, Ta_2O_5, and Nb_2O_5 are recognized as materials of the highest permittivity among conventional binary oxides (25-100). Due to higher leakage currents, these materials are of lesser importance as gate dielectric, but can be suitable for memory dielectric applications.

Table 3. Defect densities in selected Al/dielectric oxide/Si MOS structures. Zr-Al-O and Hf-Al-O are with as-deposited $HfO_2(ZrO_2)$ constituent grown in $HfCl_4(ZrCl_4)$-H_2O ALD process on HF-etched p-Si(100). The content of niobium in Hf-Al-Nb-O films was ca. 10-15 at.%.

material, Hf precursors	T_R, °C	d_{ox}, nm	D_{it}, $cm^{-2}eV^{-1}$	$DIGS_{max}$, $cm^{-2}eV^{-1}$	substrate
HfO_2 from $HfCl_4$	300	9.8	$1\text{-}2\times10^{11}$	3×10^{13}	p-Si
HfO_2 from HfI_4	300	6-8	8×10^{11}	2.5×10^{11}	p-Si
$Hf_{1-x}Si_xO_4$ from HfI_4	400	9.6	4×10^{12}	1.3×10^{11}	n-Si
Al_2O_3	300	6	$8\text{-}10\times10^{11}$	12×10^{10}	n-Si
Hf-Al-O, Hf:Al=1:0.7	300	5.3	0.9×10^{10}	1.2×10^{12}	p-Si
Zr-Al-O, Zr:Al=1:0.7	300	11.7	6.0×10^{10}	2.0×10^{12}	p-Si
Hf-Al-Nb-O	300	5.4	$3\text{-}8\times10^{12}$	2.0×10^{9}	p-Si
Hf-Al-Nb-O	300	11.0	$5\text{-}8\times10^{12}$	unmeas.	p-Si
Ta_2O_5	300	7.5	6×10^{12}	1.2×10^{11}	p-Si
Nb_2O_5-Ta_2O_5-Nb_2O_5	300	1.5-7-1.5	$1\text{-}2\times10^{13}$	6×10^{11}	p-Si
TiO_2	275	20	2×10^{12}	0.6×10^{11}	n-Si

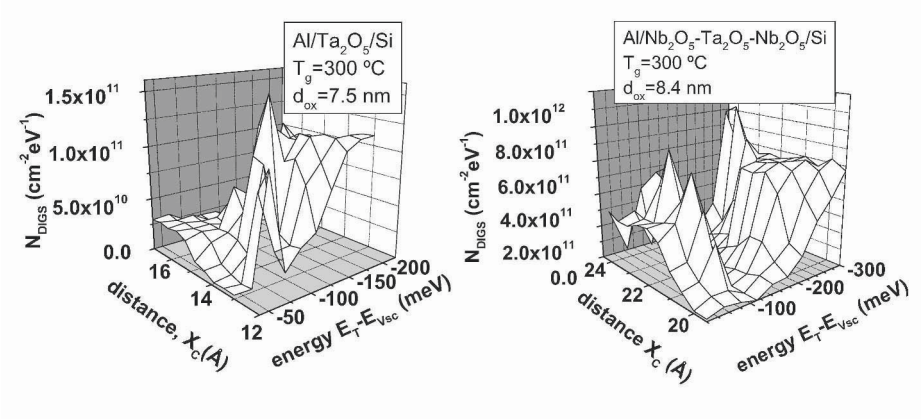


Figure 2. Three-dimensional DIGS plots of Ta_2O_5 film and Ta_2O_5-Ta_2O_5-Nb_2O_5 as-deposited on HF-etched n-Si(100) substrates.

In Ta_2O_5, both the dielectric constant and leakage currents tend to be lower than in Nb_2O_5 and thus the dielectric performance could be improved by mixing or nanolaminating these oxides.[18,23] DIGS densities[35] have been noticeably higher and deeper in Ta_2O_5-Nb_2O_5 nanolaminates compared to single Ta_2O_5 films on silicon (Fig. 2, Table 3). DIGS density has also shown dependence on the compositional homogeneity, likely increasing due to phase boundaries in the form of Ta_2O_5/Nb_2O_5 „bulk" interfaces. Mixing niobium into Hf-Al-O oxides has reduced the C-V hysteresis width,[19] but also increased the leakage and interface trap density (Table 3).

TiO_2 in as-deposited state is a truly leaky oxide, possessing space-charge determined leakage currents in the order of magnitude $1\text{-}10 \times 10^{-2}$ A/cm^2. TiO_2 films on Si have therefore all been measured after annealing at 750 °C in O_2 for 10 min. D_{it} has clearly been higher than in HfO_2 or $HfAlO_x$ films on Si, while DIGS has been comparable to that in other materials due to the densification and recrystallization (Table 3).

Summary

The defect density in various high-k materials is influenced by the choice of precursors and atomic layer deposition temperature. Disorder-induced gap-state densities tend to be lower in amorphous films and films with higher phase homogeneity. Trap density increases with residual contamination level, e.g. hydrogen content. In terms of defects affecting the leakage and conductance, Nb_2O_5, Ta_2O_5 and TiO_2 are much more sensitive materials compared to HfO_2 and Al_2O_3.

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INTERDIFFUSION STUDIES OF HIGH-K GATE DIELECTRIC STACK CONSTITUENTS

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Abstract. This paper presents a summary of recent studies of the thermal stability of various high-k gate dielectric materials. The role of film morphology and the resultant interdiffusion are also discussed.

Keywords: high-k dielectrics, metal gate, gate stack, interdiffusion, thermal stability

1. Introduction

High-k dielectric materials have been under intense investigation for the scaling of planar CMOS integrated circuits.[1] Unlike the relatively mature state of understanding of the physical and electrical properties of benchmark dielectric materials such as SiO_2 and SiO_xN_y,[2] high-k dielectric materials require further substantial materials research and development to enable their successful integration into device structures.[3,4,5] Several requirements must be met from these materials to enable successful integration, and these include permittivity and the associated band gap/alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility, as well as the resultant

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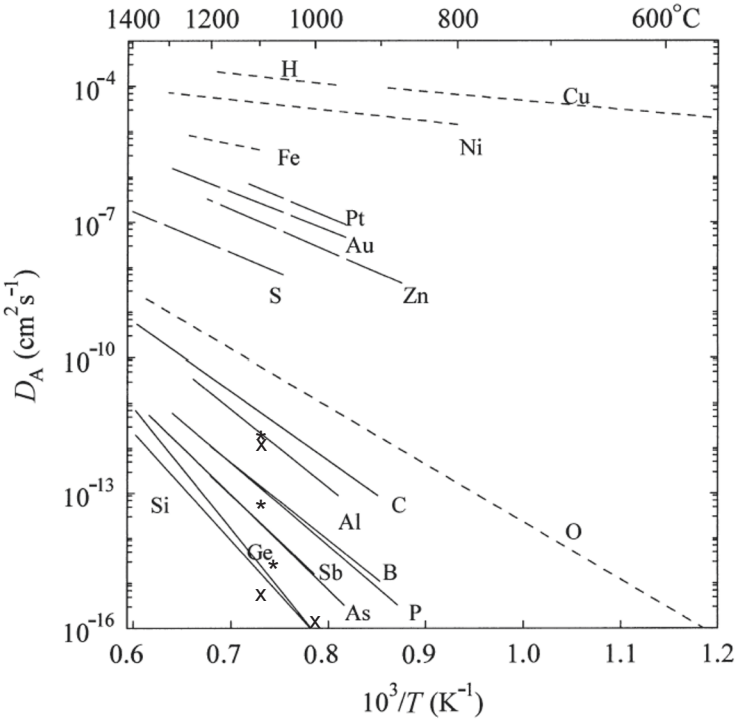


Figure 1. The temperature dependence of the diffusion coefficient for species in Si. See text for further discussion. Recent Hf (x) and Zr (*) measured diffusivities are included. After refs. 6, 14, 15.

transistor mobility and reliability. An underlying requirement is the desire for a stable material – stable in both materials properties and resultant electrical performance – to enable integration into CMOS device process flows in a cost-effective manner.

Given the extensive thermal processing required, thermal stability is a highly desirable property. Thermal stability in regard to uncontrolled interfacial reactions, as well as the prospect of uncontrolled interdiffusion between the various components of the gate stack is a concern. The thermal processing required in the fabrication of CMOS transistors results in annealing temperatures often exceeding 1000°C for several seconds to activate dopants in the source, drain and gate regions. The diffusion of gate dielectric constituents into the transistor channel from such thermal treatments is expected to result in impurities which can serve as scattering centers that deleteriously impact carrier mobility.

As shown in Figure 1, substantial mass transport is anticipated for a number of atomic species in single crystal Si.[6,7] The solid lines indicate species which

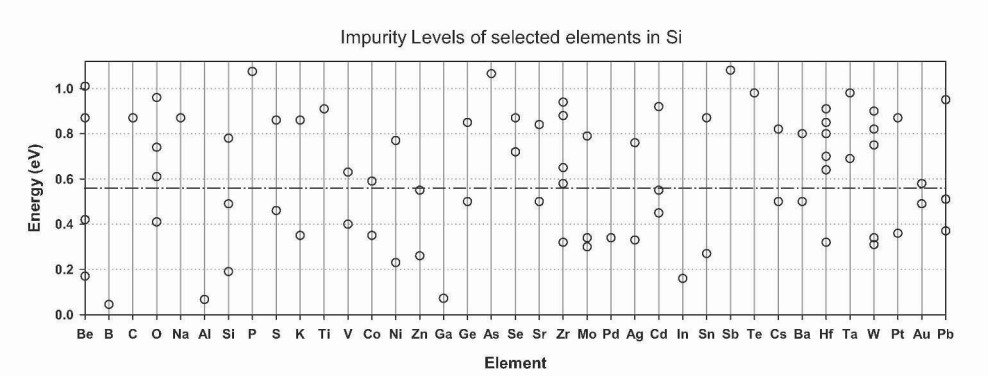


Figure 2. Energy levels of selected impurities in the band gap of Si. The dashed line indicates the midgap energy for Si. After refs. 9, 13, 14.

diffuse by vacancy or interstitialcy (indirect) defect mechanisms, where such species are dissolved mainly at substitutional lattice sites. Those with short-dashed lines correspond to species that diffuse through a direct interstitialcy mechanism, where point defects are not involved.[‡] Those species with long-dashed lines behave as hybrids that are mainly dissolved as substitutional lattice species which diffuse through interstitial-substitutional exchange mechanisms. From the data in Figure 1, it can be seen that facile diffusion of many transition metals is expected upon the annealing conditions employed for CMOS transistor fabrication. As the majority of device carrier transport in the channel occurs within a few nanometers of the gate dielectric/substrate interface, such diffusion may certainly result in enhanced scattering mechanisms and therefore mobility degradation. Such degradation effects on transistor mobility have been reported for Al interdiffusion with Si from Al_2O_3 gate dielectrics.[8] Indeed, the appearance of significant ($\geq 10^{16}/cm^3$) impurity scattering centers from the interdiffusion of gate stack constituents may well be the primary cause for the observed mobility degradation in many transistor studies incorporating high-k dielectrics (and metal gate electrodes) with mobile constituents.

Moreover, such ionized impurities may exhibit levels in the band gap of Si, resulting in the presence of defect traps for electrons or holes. As shown in Figure 2, various elements that are constituents of compounds under investigation for gate stack materials (dielectrics and metal gates) exhibit deep levels within the Si band gap.[9] Such levels are therefore available for electron or hole tunneling mechanisms, resulting in significant issues for device electrical

[‡] The slower diffusion behavior for oxygen is attributed to the requirement of additional Si-O bond scission mechanisms. See ref. 6.

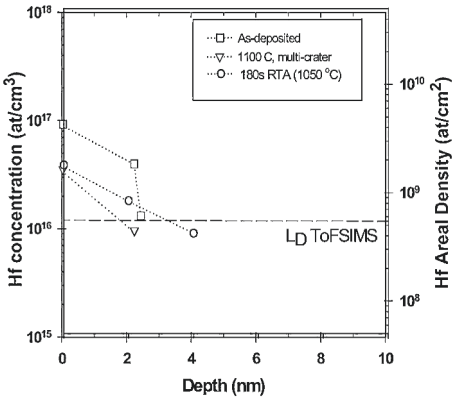


Figure 3. ToFSIMS profiles of Hf interdiffusion with the Si substrate before and after annealing in N_2. After Refs 16, 17.

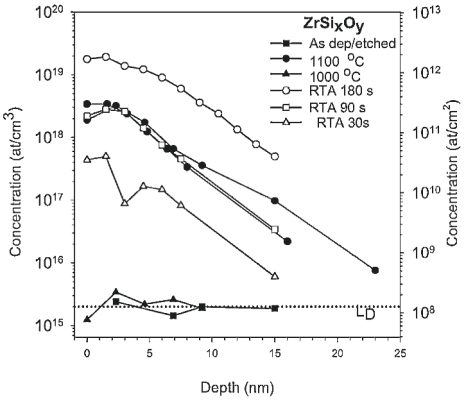


Figure 4. ToFSIMS profiles of Zr interdiffusion with the Si substrate after annealing. Filled (open) symbols correspond to furnace (RTA) treatments, unless noted. After Refs. 15, 17.

characteristic control and reliability. Recent work examining Hf and Zr interdiffusion (discussed below) is also summarized in Figure 1.

An underlying requirement is the desire for a stable material – stable in both materials properties and resultant electrical performance – to enable integration into CMOS device process flows in a cost-effective manner. This paper will review our recent thermal stability studies of several high-k dielectric candidates and the role of film morphology for interdiffusion of gate stack constituents.

2. Results and Discussion

2.1. Hf AND Zr SILICATE DIELECTRICS

Both Hf-silicate[10] and Zr-silicate[11] have been investigated for high-k gate dielectric applications.[12] The investigation of the thermal stability of these materials has resulted in an apparent substantial difference in the interdiffusion behavior of the respective transition metal, *viz.* Hf and Zr. The presence of Hf and Zr in Si has been shown to lead to deep levels like many of the transition metals shown in Figure 2,[13,14] and spreading resistance measurements of surface-diffused species indicated acceptor behavior for Hf and Zr.[14]

Surface sensitive Time-of-flight secondary ion mass spectrometry (ToFSIMS) was previously employed to examine the interdiffusion of Zr and Hf from their respective silicate thin films.[15,16,17] Figure 3 presents the

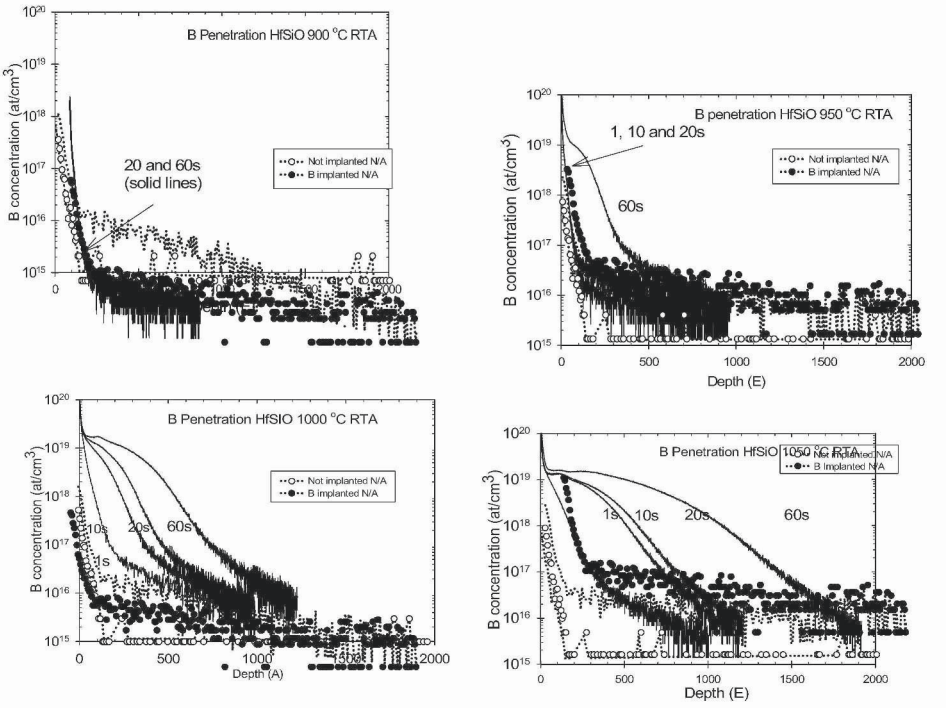


Figure 5. Dynamic SIMS profiles for B in Si from diffusion through Hf-silicate from a p+ poly-Si overlayer. Ref. 24.

ToFSIMS depth profiles obtained from a Zr-silicate thin film before and after furnace anneals to 1100°C in N_2 for 6 min as well as rapid thermal annealing (RTA) in N_2 to 1050°C. It is seen that as-deposited or samples furnace-annealed to 1000°C results in no detectible near-surface diffusion. It is also seen that furnace anneals at 1100°C (reproducibility if the depth profile after the 1100°C treatment is also shown in Fig. 3) or RTA in N_2 to 1050°C results in the incorporation of Zr into the Si substrate. Modeling the observed depth profiles assuming a semi-infinite Zr source[15,17] (*viz*., the Zr-silicate layer), results in an estimated diffusivity of $D_0 \sim 2\times10^{-15}$ cm^2/s in this high temperature regime, and appears to be consistent with independent measurements by Vyvenko, *et al.* for Zr diffusivity in Si ($\sim5\times10^{-14}$ cm^2/s at 1100°C).[14] Extrapolation of the near surface concentration of Zr with relevant process thermal budgets leads to concentrations [Zr]$\geq10^{16}$/cm^3. In contrast, the profiles shown in Figure 4 for Hf from Hf silicate thin films before and after the same annealing treatments indicate that any detectible Hf diffusion is limited to a depth of ≤1nm, due to the SIMS detection limit. The reason for the difference in the apparent diffusion behavior remains to be understood, given the comparable size of the Hf or Zr atoms. Recent work on diffusion studies of implanted Hf and Zr has indicated the presence of fast and slow diffusion mechanisms for both of these

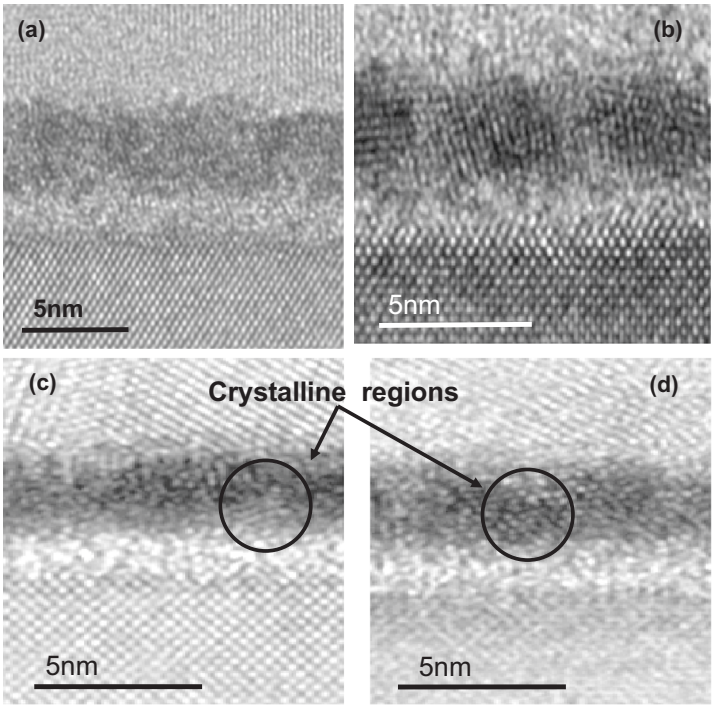


Figure 6. HRTEM results for B-doped poly-Si/HfSiO/Si films after 60s RTA at (a) 900°C , (b)1000°C , (c) and (d) 950°C showing different regions in the sample. Ref. 24.

species.[14] Other experimental evidence from spreading resistance profiles suggests comparable diffusivities (~10^{-12} cm^2/s) for either species for long anneals at 1100°C, and a hybrid diffusion mechanism is proposed.[14] Further work is required to clarify this point. Nevertheless, it appears that an enhanced thermal stability is observed for Hf-based oxides and silicates compared to their Zr-based analogs. It is also noted that mobility measurements of transistors incorporating Hf-based dielectrics, and in particular Hf-silicate dielectrics, suggest a smaller mobility degradation relative to that obtained for benchmark dielectrics (SiO_2 and SiON) is observed in contrast to other high-k dielectric materials.[4] These observations could be consistent with a dearth of Hf impurities for scattering in the channel region, as well as additional mobility degradation mechanisms.[18,19,20]

The penetration of impurities through such silicate films from an overlying, doped polycrystalline Si layer has also been investigated.[21,22,23,24] In the case of B diffusion through Hf-silicate thin films, a correlation of enhanced penetration and the formation of grain boundaries upon annealing was observed. As seen in

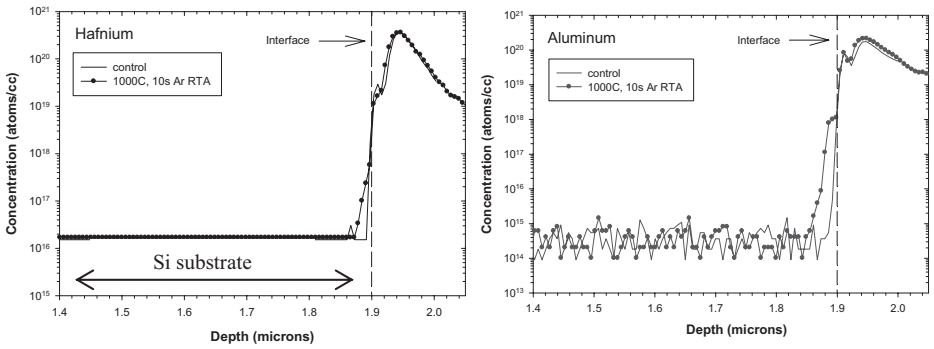


Figure 7. Backside SIMS analysis of Hf and Al diffusion from a 6nm $HfAl_2O_5$ film deposited on Si.

Figure 5, dynamic SIMS profiles of B exhibit penetration into the Si substrate upon RTA treatment at 950°C for 60s. The corresponding microstructure of the film is also observed to change significantly in the annealing temperature range of 900-1000°C, as seen in Figure 6. Nanocrystalline regions are detected using high-resolution transmission electron microscopy (HRTEM) upon 60 s RTA annealing at 950°C, and are clearly evident after annealing to 1000°C. In contrast, samples annealed at 900°C appear to present an amorphous structure for the Hf composition employed (10–12 at. % Hf, corresponding to a stoichiometry of $(HfO_2)_{1-x}(SiO_2)_x$, x=0.52). The concomitant increase in B concentration in the n-type Si substrate taken with the observed changes in Hf-silicate morphology suggest that the formation of nanocrystalline regions and their grain boundaries results in an enhanced diffusion "conduit" for B. Similar results were also obtained for P and As dopant species in poly-Si as well.[24]

The suppression of such dielectric crystallization and dopant penetration through the incorporation of N has also been considered,[25] and more recently examined where a significant reduction of B penetration and the elimination of P and As penetration is observed.[23,24] Promising device performance results have also been reported for "HfSiON" films as well.[26] The combination of the thermal stability with respect to Hf interdiffusion and the suppression of crystallization appear to be important considerations for gate dielectrics that must withstand conventional "front end" process flows.

2.2. HAFNIUM ALUMINATE DIELECTRICS

The suppression of crystallization for HfO_2 films through the incorporation of Al to result in the formation of Hf-aluminate has been reported using atomic

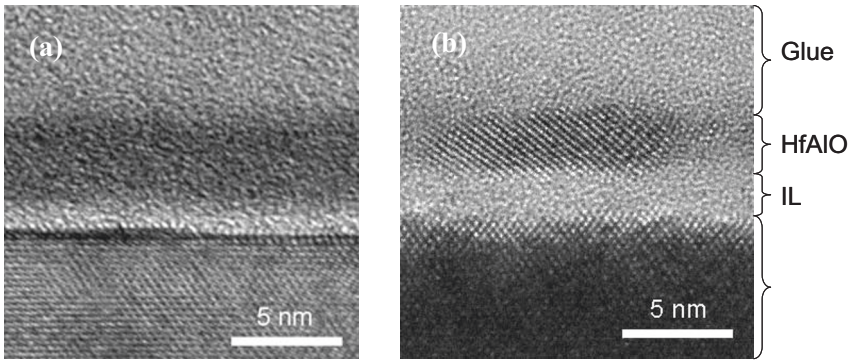


Figure 8. HRTEM image of $(HfO_2)_x(Al_2O_3)_{1-x}$; x=0.57 deposited by ALD. (a) As-deposited and (b) annealed films.

layer deposition (ALD) methods.[27] An amorphous film structure was reported for "spike" (<1s) anneals up to 1050°C for films with 75 at.% Al content. We have recently examined the thermal stability of uncapped $(HfO_2)_x(Al_2O_3)_{1-x}$ (x=0.57) thin films prepared by ALD using SIMS methods where the analysis is performed from the substrate side ("backside") of the substrate/dielectric interface. Such SIMS analysis methods attempt to minimize the ion-beam mixing ("knock-on") distortions of depth profiles in order to obtain a relatively unperturbed depth profile.

As can be seen in Figure 7, comparison of the Hf backside SIMS depth profiles for the unannealed ("control") and annealed Hf-aluminate films (RTA 1000°C, 10s in Ar) indicates that Hf diffusion appears to be at or below detectible limits, while some Al diffusion into the Si substrate is evident. HRTEM (Fig. 8) and XRD analysis (not shown) of the Hf-aluminate film indicates that crystallization is observed in these films upon the RTA treatment, and appears to be consistent with recent reports.[28] Additional growth of the interfacial layer (IL) is also noted. Again, the SIMS depth profiles are consistent with the previous evaluations of both Hf and Al thermal stability in other high-k dielectrics as far as interdiffusion is concerned. The correlation between the presence of a crystallized phase and the detection of impurities in the Si substrate (channel) is consistent with the results discussed above.

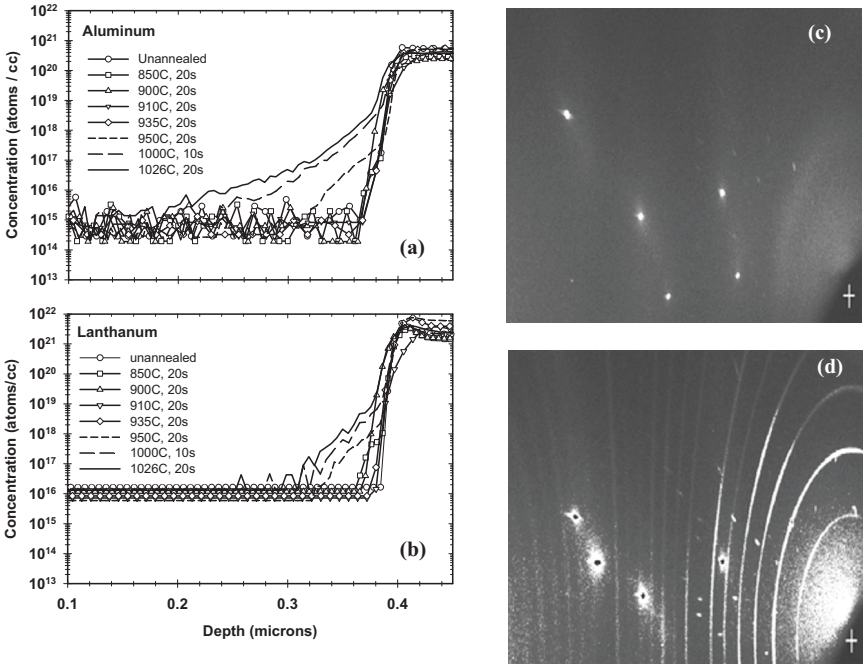


Figure 9. Backside SIMS analysis of $LaAlO_3$ with annealing treatments showing the depth profile for (a) Al and (b) La species. X-ray diffraction analysis of films annealed for 20 s at (c) 935°C and (d) 950°C. Ref. 38.

2.3. LANTHANUM ALUMINATE DIELECTRICS

The oxides, silicates and aluminates of La have been considered as high-k dielectric candidates.[1,29,30] Amorphous La aluminates have recently been the subject of considerable attention for high-k gate dielectric applications.[31,32,33,34] The thermal stability of La-aluminate films deposited by molecular beam deposition has been investigated by HRTEM, with sharp interfaces and a lack of interfacial oxide formation reported.[35] However, recent work using sputtered La-aluminate films has suggested that there exists considerable Si interdiffusion with the aluminate,[36] a prospect not predicted from bulk equilibrium thermodynamic considerations[37] and sometimes attributed to the deposition technique.[30]

We have recently examined the thermal stability of amorphous $LaAlO_3$ deposited on Si using molecular beam deposition methods.[38] As seen in Figure 9, backside SIMS analysis of annealed $LaAlO_3$ appears to result in the

interdiffusion of both Al and La with the Si substrate after RTA treatments of 950°C for 20 s in N_2. The interdiffusion of Al is consistent with the previous measurements for $HfAl_2O_5$ and Al_2O_3 described above. As can be seen in the 2-D x-ray diffraction image, annealing the $Al_2O_3/LaAlO_3/Si$ structure at 935°C for 20 s results in the detection of diffraction spots attributed to the Si substrate only. However, annealing at 950°C for 20 s in N_2 clearly results in the detection of diffraction rings which are consistent with the formation of poly-crystalline $LaAlO_3$ in the film. Again, the concomitant observation of interdiffusion and the associated grain boundary formation indicate that the suppression of crystallization is a desirable avenue to pursue as far as impurity control in the substrate.

3. Conclusions

This paper summarizes recent work examining the thermal stability of gate dielectrics in view of conventional CMOS process constraints. We find that the film morphology evolution appears to play a significant role for the interdiffusion of gate stack species into the channel region of the Si substrate. Assuming that thermal budgets will continue to require RTA treatments as high as 1000°C, these results indicate that amorphous dielectric films are preferable to control the diffusion of species into the Si channel. Of course, amorphous films would be expected to exhibit a somewhat lower permittivity than their crystalline counterparts. However, this tradeoff between film morphology and permittivity must be considered for a manufacturable solution applicable to conventional CMOS fabrication.

Acknowledgements

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XPS/LEIS STUDY OF HIGH-K RARE EARTH (LU, YB) OXIDES AND SILICATES ON SI: THE EFFECT OF ANNEALING ON MICROSTRUCTURE EVOLUTION

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Abstract. Thin Lu_2O_3 and Yb_2O_3 layers grown on Si using Atomic Layer Deposition (ALD) were studied with x-ray photoelectron spectroscopy (XPS) and low energy ion spectroscopy (LEIS). Our results show that ALD grown Lu_2O_3 and Yb_2O_3 films subsequently annealed in N_2 are polycrystalline, and that their oxygen "subsystems" are very sensitive to further heat treatments in various atmospheres. In particular, it is evident that two chemically non-equivalent oxygen states are present in the oxides at equilibrium conditions. The one with the higher binding energy ($BE_{O1s} \approx 531.8$ eV) is loosely bound, desorbs from the subsurface region upon vacuum annealing at $T>300^0$C, and re-appears upon annealing in O_2 ($T\approx500^0$C, $P_{O2}=10^{-1}$ Torr). ALD can provide a variety of Lu silicates, depending on precursor combination and growth conditions. As grown ultrathin (≤5 nm) continuous Lu_2O_3 and Yb_2O_3 films on Si exhibit an interfacial layer from ~1 to 3 nm thick and a hydroxide layer on top. Upon annealing in N_2, both components of the stacks transform into amorphous silicates. *In situ* XPS and LEIS analyses show that ultrathin Lu silicate films are further stable on Si at least up to $T=900^0$C, while for ultrathin Yb silicate layers the valence band structure appears sensitive to the annealing environment, and the Yb silicates eventually decompose and desorb from the surface upon vacuum annealing at $T=900^0$C.

Keywords: rare earth oxides, lutecium, ytterbium, x-ray photoelectron spectroscopy, low energy ion spectroscopy

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1. Introduction

Rare earth (RE) metal oxides are a high–dielectric–constant (κ) materials which may satisfy the requirements to substitute SiO_2 as insulating layer in complementary metal–oxide–semiconductor (CMOS) devices[1,2]. In particular, both Lu_2O_3 and Yb_2O_3 exhibit a relatively large band gap $E_g \approx 5$ eV[3]. At the same time, the 2:3 metal: oxygen stoichiometry ratio promotes a low charge neutrality level and hence a large conduction band offset (CBO) between the oxide and the silicon substrate[4]. Besides, both Lu_2O_3 and Yb_2O_3 have an unique oxidation state (equal to 3), which avoids mixed metal oxide stoichiometries with different electronic structures. In addition, for Lu the intrinsic high energy of the 5*d* shell and its low occupancy (only one electron) should, in principle, limit the density of interfacial traps in Lu_2O_3[5]. Recent experimental results on the electric properties of Lu_2O_3 on Si partially support optimistic predictions[6,7].

In this work, thin layers of Lu_2O_3, Yb_2O_3 and Lu silicates were grown on Si(100) substrate using atomic layer deposition (ALD), and the elemental and chemical composition for as grown samples as well as their evolution upon different heat treatments were monitored combining two analytical techniques, namely, x-ray photoelectron spectroscopy (XPS) and low energy ion spectroscopy (LEIS). While XPS probes ~5 nm subsurface region and provides information on both the elemental and chemical composition in the layer, LEIS, utilizing He^+ ions, is only sensitive to the outmost surface layer and is used to determine surface elemental composition. The combination of both techniques, exploiting *in situ* vacuum or O_2 annealing and *ex situ* rapid thermal annealing in N_2, allows a detailed characterization of the elemental versus chemical structure evolution of Lu and Yb oxides, and of Lu silicates on Si. The reaction paths in different annealing environments provide the necessary experimental basis to better understand the thermodynamics of the Lu_2O_3/Si and Yb_2O_3/Si systems.

To understand the interfacial layer formation between the RE oxide and Si, and its evolution upon heat treatments is of special importance, since the interfacial layer stability is one of the criteria ultimately defining the applicability of dielectric materials in devices. To directly probe the interfacial layer between the RE oxides and Si with XPS, and to avoid detrimental effects of Ar^+ etching on the interfacial chemical composition[8], ultrathin Lu and Yb oxide layers were grown on Si(100) and characterized with XPS (layer elemental and chemical composition) and LEIS (surface elemental composition). These ultrathin oxide layers on Si evolve to silicates upon annealing, and the stability of the latter on Si upon further heat treatments is not completely understood. The detailed characterization of the reaction paths and clues to mechanisms responsible for such evolutions could be revealed through *in situ* XPS and LEIS.

The obtained experimental data allow to better understand the thermodynamic properties of the Lu_2O_3/Si and Yb_2O_3/Si systems, and to preliminarily conclude on their applicability as candidates for microelectronic applications.

2. Experimental

This work investigates Lu and Yb oxides and Lu silicate films grown using ALD, a technique employed in microelectronics because of the smoothness, conformality, and good electrical characteristics of the deposited films. The organometallic compounds $\{[\eta^5\text{-}C_5H_4(SiMe_3)]_2LuCl\}_2$[9], and $Lu(iPrO)_3$ were used as precursors for Lu together with both H_2O and O_3 as oxygen sources (Me = CH_3). The combination of $[(Me_3Si)2N]_3Lu$ with H_2O was used for the Lu silicate layers. On the other hand, $Yb(Cp)_3$ and $Yb(thd)_3$ were used as precursors for Yb combined with respectively H_2O and O_3 the former, and with only O_3 the latter (Cp = C_5H_5, and thd = $C_{11}H_{19}O_2$). The films were deposited in an ALD F-120 ASM-Microchemistry reactor on Si(100) wafers. Some of samples were also subjected to post-deposition rapid thermal processing (RTP) in N_2 for 60 s up to 1000 °C.

The growth parameters of samples used in this work are listed in Table 1.

Table 1 ALD growth parameters for samples used in this work.

Precursor combination	Growth temperature	RE source temperature
$\{[\eta^5C_5H_4(SiMe_3)]_2LuCl\}_2$ and H_2O	360 °C	195 °C
$\{[\eta^5C_5H_4(SiMe_3)]_2LuCl\}_2$ and O_3	360 °C	195 °C
$Lu(iPrO)_3$ and H_2O	330 °C	185 °C
$Lu(iPrO)_3$ and O_3	310 °C	180 °C
$[(Me_3Si)2N]_3Lu + H_2O$	380 °C	150 °C
$Yb(Cp)_3$ and H_2O	360 °C	100 °C
$Yb(Cp)_3$ and O_3	360 °C	100 °C
$Yb(thd)_3$ and O_3	360 °C	100 °C

For XPS analysis, an XSAM-800 (Kratos) electron spectrometer was employed utilizing an MgK_α source (E=1253.6 eV) to excite the photoelectrons. The energy resolution was measured to be ΔE=0.9 eV (Au 4*f*). The fitting of the spectra was performed by setting the line as a combination of Gaussian and Lorenzian curves utilizing the Origin 6.0 software.

In situ annealing up to T=900^0C was performed either in ultra-high-vacuum (UHV, P=10^{-9} Torr) or in O_2 atmosphere (P_{O2}=$10^{-6}\div10^{-2}$ Torr) in the preparation chamber of the spectrometer, using calibrated electric current transmission directly through the Si substrate mounted on the sample holder. For *in situ* XPS calibration, few Au monolayers were deposited on top of the RE oxide layers

using the pulsed laser deposition (PLD) module installed in the preparation chamber of the spectrometer ($E_{BAu4f7/2}$ = 84.0 eV). An Ar^+ ion beam at E=2.5 keV incident at 55^0 on the sample surface was employed to etch the surface layer of the thin oxide films.

For LEIS analysis, an He^+ beam was used, instead, with an incident energy in the E_0=100÷1000 eV range. The ions backscattered at $\theta=125^0$ were analyzed with the same hemispheric analyzer of the electron spectrometer but switched to the opposite polarity.

3. Results and discussion

3.1. Lu_2O_3 (Yb_2O_3) LAYERS ON Si

XPS results on relatively thick (~ 10 nm) Lu_2O_3 layers on Si(100) are presented in Figure 1 (the data for the Yb_2O_3 films are qualitatively very similar and therefore not shown in this paper). Surface Lu 4*f* and O 1*s* core level photoemission spectra of as grown Lu_2O_3 layers (e.g., from $Lu(iPrO)_3$ and O_3) are displayed in Figure 1,a. It is noteworthy that the film is partly amorphous (as revealed by x-ray diffraction measurements). Although for our experimental conditions the spin-orbit components of the Lu 4*f* line are only partially resolved, it is clear that an additional Lu 4*f* doublet should be considered in the fittings. The same holds for the O 1*s* single line. The fitting of the spectra was performed with a pair of 3:4 peak area ratio doublets and single lines for Lu 4*f* and O 1*s*, respectively. The binding energies (BE) corresponding to pure Lu_2O_3[6] and $Lu(OH)_3$, usually present in the subsurface region[10], are given in Table 2.

From the comparison of the peak areas for ultrathin surface (hydroxide) layer and bulk oxide, the thickness of hydroxide layer turns out to be ≈ 3 nm. In fact, it is removed upon mild Ar^+ etching (Figure 1,b). However, an *additional* line in the O 1*s* spectrum at slightly lower BE is still visible. A much smaller hydroxide component is observed in the O 1*s* spectrum for the same Lu_2O_3 sample upon RTP (Figure 1,c), indicating that the hydroxide specie is removed from the surface during crystallization ("densification"), presumably according to the reaction:

$$2Lu(OH)_3 \rightarrow Lu_2O_3+3H_2O.$$

Further *in situ* annealing in vacuum ($T=300^0C$,) and in O_2 ($P_{O2}=10^{-6}$ Torr, $T=600^0C$) results in the *additional* O peak diminishing and re-emerging, respectively (Figure 1,d,e). The fact that the fraction of additional O state can be modified by the environment during annealing at moderate T indicates that the chemical structure of Lu_2O_3 is not quite stable, at least, in the film subsurface region. There might be several explanations of the origin of the O

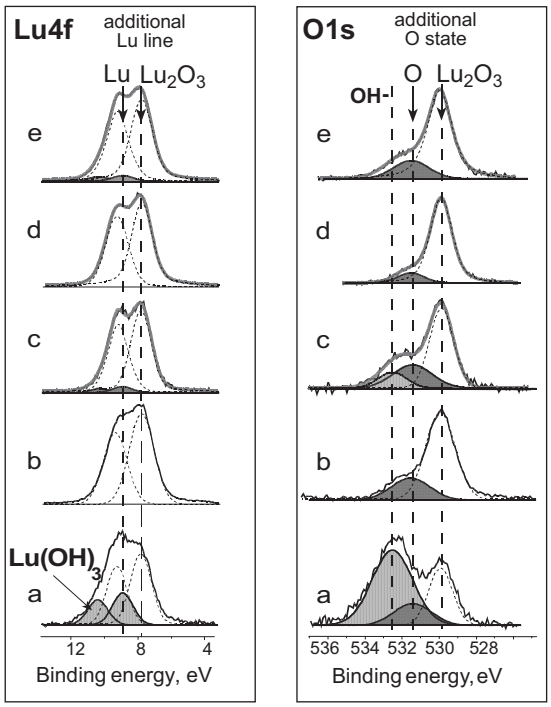


Figure 1. XPS Lu 4*f* and O 1*s* lines taken from ALD grown Lu_2O_3 layers: (a) the surface of as grown (partly amorphous) Lu_2O_3, (b) upon further Ar^+ ion etching, (c) the surface of Lu_2O_3 upon *ex situ* RTP, (d), upon further *in situ* vacuum annealing, and (e) annealing in O_2 ($P_{O2}=10^{-6}$ Torr).

chemical state which gives rise to the additional peak in the O 1*s* core level spectrum at higher BE: 1) OH^- groups, always present in subsurface layer, which, however, appear at noticeably higher BE than the observed ones (Table 2); 2) O bound to Si in the SiO_2 form, which is often observed on the surface of ALD grown oxide layers. This hypothesis is weak since the additional O state is found even when no Si is observed on the surface; 3) existence of two chemically nonequivalent O states in the Lu_2O_3 crystalline structure. This hypothesis should also be ruled out, since all O sites are equivalent in the bixbyite structure.

From the analysis of the whole set of experimental data for both as grown amorphous Lu_2O_3 and Yb_2O_3 layers, we conclude that the additional O state observed with XPS could be attributed to super-stoichiometric oxygen, which is either trapped during ALD growth or absorbed upon exposure to air at least in, the subsurface oxide layer at equilibrium conditions. An additional evidence

for this conclusion is that ultrathin RE oxide layers on Si are fully converted into silicates upon annealing in vacuum, a process that possibly requires additional oxygen (see below).

Table 2. Lu 4*f* and O 1*s* core level BE taken from the surface of an as grown *amorphous* Lu_2O_3 film and upon Ar^+ ion etching.

	BE(O 1*s*), eV	BE(Lu 4*f*), eV	
		5/2	7/2
Lu_2O_3	529.8 (531.5)	7.9	9.3
$Lu(OH)_3$	532.3	9.0	10.4

3.2. Lu SILICATE LAYERS ON Si

The combination of $[(Me_3Si)2N]_3Lu + H_2O$ in ALD produces Lu oxide layers with a large amount of silicon, homogeneously distributed in them (as revealed by a Rutherford backscattering spectrometry - RBS)[11].

In Figure 2, core level Lu4*f*, Si2*p* and O1*s* spectra of a silicate layer from $[(Me_3Si)2N]_3Lu + H_2O$ are compared with those of pure SiO_2 and Lu_2O_3 (all the spectra were carefully calibrated). Several differences are evident in the BE of the typical lines in silicates and oxides: 1) the Lu 4*f* doublet in the former compound is found at higher BE than in Lu_2O_3 films, $\Delta BE \approx 1$ eV; 2) the O 1*s* line position in silicates is between the one in SiO_2 and in Lu_2O_3, and can be fitted with one, though broad, line; 3) finally, the Si 2*p* line is found in a "suboxide" position with respect to SiO_2 (i.e. $\Delta BE_{sil.} \approx 3.1$ eV from Si^0 for the Lu silicate, and $\Delta BE_{SiO2} \approx 3.8$ eV from Si^0 for SiO_2). These differences unambiguously identify Lu silicates with XPS.

In the BE shifts for Lu, Si and O in Lu silicates with respect to pure SiO_2 and Lu_2O_3 are plotted as a function of the Lu/Si ratio measured through XPS in the silicate layers. It is evident that the BE shifts are a monotonous function of composition, which is not uniquely determined in as grown silicate layers. It is known indeed, that RE silicate layers are always amorphous, apparently because of the high barrier for the nucleation of the crystalline phase[12], which may prevent also the formation of a specific phase stoichiometry. Interestingly, unlike in RE oxide films, hydroxide formation is never observed in the surface layer of silicates.

To investigate the thermal stability of an amorphous Lu silicate layer, vacuum annealing of a thick $Lu_{0.75}Si_1O_3$ sample from $[(Me_3Si)_2N]_3Lu + H_2O$ was performed up to 900^0C in vacuum and monitored *in situ* with XPS (the heating was interrupted upon each annealing step to allow the analysis). Changes in composition as a function of the annealing temperature T derived from XPS data, are shown in . The subsurface layer composition in Lu silicates

is quite sensitive towards vacuum annealing. The corresponding Si/Lu ratio decreases as a function of T, suggesting that Si desorbs from the surface.

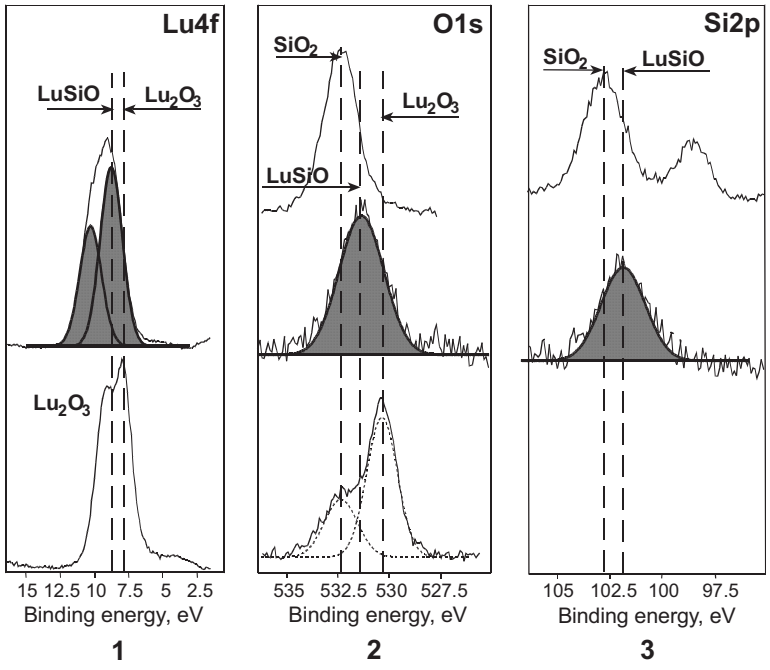


Figure 2. XPS Lu 4*f*, O 1*s*, and Si 2*p* lines taken from the bulk of an ALD grown Lu silicate layer from $[(Me_3Si)2N]_3Lu + H_2O$ compared with the lines corresponding to pure Lu_2O_3 and SiO_2.

The available data are not sufficient to establish the true mechanism of Lu silicate composition evolution, but it is reasonable to suppose that Si desorbs in the SiO form. Further annealing in O_2 (P_{O2}~10^{-1} Torr) partially restores the initial stoichiometry. This phenomenon occurs only if we assume Si outdiffusion from the deeper layers (ultimately, from the Si substrate) to the surface, and its oxidation. Generally, these results show that Lu silicates are not as robust with respect to different heat treatments as it is generally expected from the thermodynamic point of view.

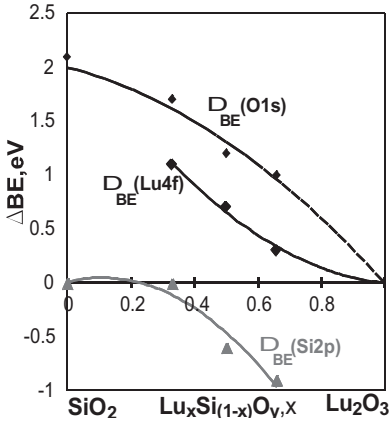


Figure 3. Binding energy shifts (ΔBEs) for Lu, Si and O in Lu silicates as a function of the Lu/Si ratios.

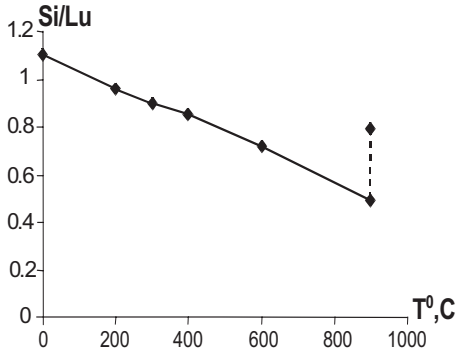


*Figure 4.*Compositional changes in Lu silicate (originally $Lu_{0.75}Si_1O_3$) upon vacuum annealing and further annealing in O_2.

3.3. ULTRATHIN Lu_2O_3 LAYERS ON Si(100)

Ultrathin oxide layers grown on single crystalline Si substrate are of special interest since they are an ultimate test for the growth technique ability to fabricate suitable stacks for, e.g. CMOS technology. On the other hand, when the oxide layer thickness is ≤ ~ 5nm, the interfacial layer with the substrate can be directly probed and characterized with XPS, for both as grown and annealed films. Lu_2O_3 layers, 3 nm thick from RBS measurements, were grown from $\{[\eta^5C_5H_4(SiMe_3)]_2LuCl\}_2$ and H_2O on Si(100). LEIS analysis was performed upon mild ($T=150^0C$) heating in vacuum to find the surface elemental composition. The spectrum taken at E_0^{He+} = 1 keV for an as grown sample is shown in Figure 5.

The fact that the only peaks observed are Lu and O, while Si is not visible allows to conclude that the Lu_2O_3 layer is continuous[14]. Upon RTP in N_2 up to 950^0C, Si emerges in the LEIS spectrum, either because of the Lu_2O_3 crystalline grains coarsening on the surface and opening Si substrate surface, or because of Lu silicate formation.

XPS was employed to assess the Lu_2O_3/Si(100) interfacial layer for as grown sample, and to monitor its evolution during heat treatments in O_2 and in vacuum. Core level Lu 4*f*, Si 2*p*, and O 1*s* spectra taken at different stages are presented in Figure 6. The O 1*s* line for an as grown ultrathin Lu_2O_3 layer on Si(100) can only be fitted with three lines, i.e. Lu hydroxide, pure Lu_2O_3, and Lu silicate (Si 2*p* Figure 6,a). The Si 2*p* line is a combination of a peak originating from the Si substrate, and of another one located in the "suboxide"

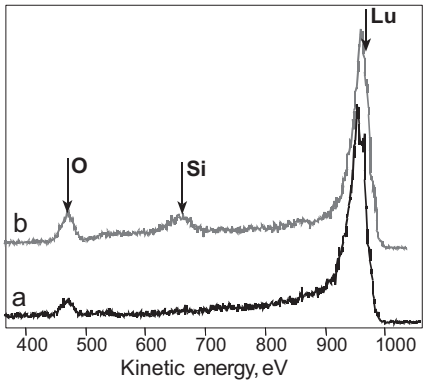


Figure 5. LEIS spectrum (E_0^{He+} = 1 keV) taken from the surface of a) as grown ultrathin Lu_2O_3 film on Si(100); b) Lu_2O_3 layer upon RTP.

region (ΔBE=3.1 eV from the Si^0 peak as compared to ΔBE=3.8 eV for SiO_2) indicative of a silicate present in the layer. (The Lu 4*f* line for the as grown sample was not fitted since at the employed resolution it was difficult to obtain an unique fit with several doublets). It is therefore reasonable to conclude that i) an about 2-3 nm thick $Lu(OH)_3$ layer is present on the surface; ii) a silicate layer is forming at the Lu_2O_3/Si(100) interfacial layer during deposition or upon exposure to the atmospheric air. Its thickness, calculated from the relative Si^0 versus $Si^{sil.+}$ peak areas, is ~ 1.2 nm. Upon vacuum annealing at T=300^0C, the $Lu(OH)_3$ layer disappears, in agreement with earlier observations on thicker Lu_2O_3 films, and the spectra consist of two components, one corresponding to Lu_2O_3 and the other one to $Lu_xSi_yO_z$ (Figure 6,b). Upon RTP at T = 950^0C, the Lu 4*f*, Si 2*p* and O 1*s* XPS lines consistently point toward a silicate as the only component in the spectra (*Figure 6*,c).

The silicate composition, estimated by comparing the relative Si 2*p* and Lu 4*f* peak areas with those in pure SiO_2 and Lu_2O_3, and taking into account the sensitivity factors for the elements, is $Lu_2Si_xO_{3+2x}$, $1.2<x<1.5$.

Therefore, according to our experimental observations, the Lu_2O_3/Si(100) interfacial layer formation and evolution upon annealing in different environments can be summarized as follows (Figure 7): 1) a few monolayer thick silicate interfacial layer presumably forms during the initial stage of Lu_2O_3 growth on a chemical oxide (SiO_2) terminated Si surface; 2) upon exposure to air, an ultrathin as grown Lu_2O_3 layer is mostly converted into an $Lu(OH)_3$ layer because amorphous Lu_2O_3 is known to be highly hydroscopic, and; 3) the $Lu(OH)_3$ layer can be transformed back to oxide by vacuum

annealing up to 300^0C; 4) annealing at higher temperatures converts the whole Lu_2O_3 layer into a Lu silicate one.

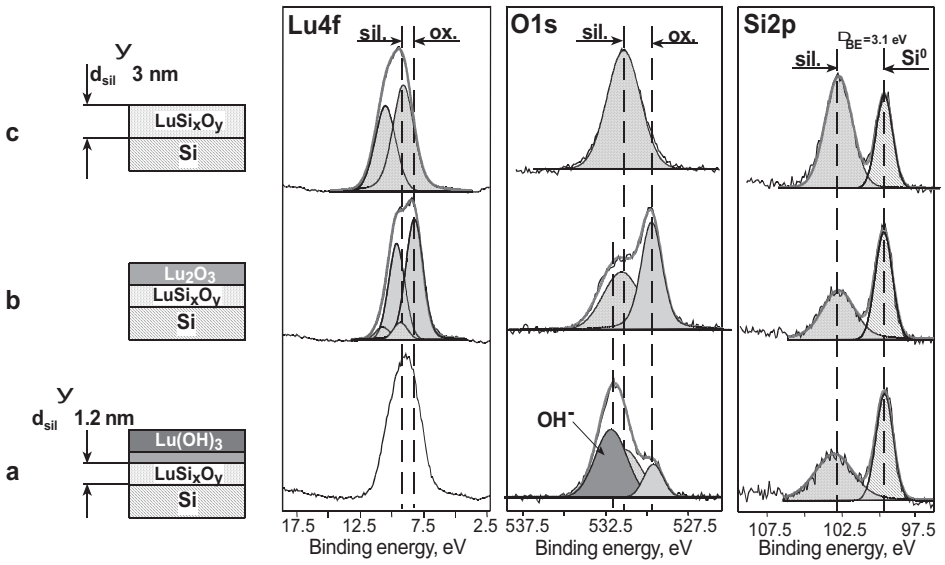


Figure 6. Lu 4*f*, O 1*s* and Si 2*p* core level lines taken from the surface of a 3 nm thick Lu_2O_3 film on Si(100): a) as grown, b) upon vacuum annealing up to 300^0C; c) upon RTP in N_2 T=950^0C.

The experimentally observed transformations are supported by thermodynamic considerations. In particular, a driving force for silicate formation exists if Lu_2O_3 is in contact with SiO_2 (Lu_2O_3+ $SiO_2 \rightarrow Lu_2SiO_5$)[13]. In fact, using the bulk thermodynamic data of Ref. [15]., and assuming the ΔH value for Lu silicate to be the same as that for Y and La silicates, one gets

$$\Delta H_{Lu2O3}\,(-20.18\ \text{eV}) + \Delta H_{SiO2}(-8.2\ \text{eV}) > \Delta H_{Lu2SiO5}(-35\ \text{eV}),$$

which is also consistent with the reaction path given in [13].

The silicate formation at the interfacial layer between RE oxide films and Si was experimentally shown[6]. It was also pointed out[13] that this phenomenon is likely due to excess oxygen incorporated into the oxide layer during growth, or to the oxygen in the annealing atmosphere. Indeed, the reaction

$$Lu_2O_3 + Si + O_2 \rightarrow Lu_2SiO_5,$$

where O_2 comes from the environment and goes through oxide layer to react with the underlying Si, is also favorable from the thermodynamical point of view [ΔH_{Lu2O3} (-20.2eV) > $\Delta H_{Lu2SiO5}$ (-35eV)][15] Our observations of the additional O state, attributed to "superstoichiometric" oxygen in the as grown

oxide layer at equilibrium conditions, supports this model and explains the observed transformation of ultrathin RE oxide layers into silicate ones even upon annealing in vacuum.

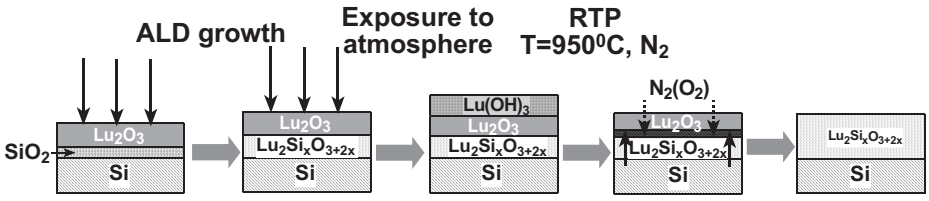


Figure 7. Interface formation and evolution for ultrathin ALD grown Lu_2O_3 layers on Si(100).

Finally, since hydroxide species are found to be a dominating ones for ultrathin "oxide" layers, suggesting the following reaction to take place:

$$2Lu(OH)_3 \rightarrow Lu_2O_3+3H_2O\uparrow$$

The alternative pathway is[13]:

$$2Lu(OH)_3 +3/2Si \rightarrow Lu_2O_3+3/2SiO_2 + 3/2H_2\uparrow,$$

and the products would eventually be converted into a silicate.

3.4. ULTRATHIN Yb_2O_3 LAYERS ON Si(100)

The interfacial layer formation and evolution upon mild (T=300^{0}C) vacuum annealing and RTP in ultrathin (~ 5 nm) Yb_2O_3 layers grown on Si(100) from $Yb(C_{11}H_{19}O_2)_3$ and O_3, is qualitatively very similar as in the Lu_2O_3/Si(100)

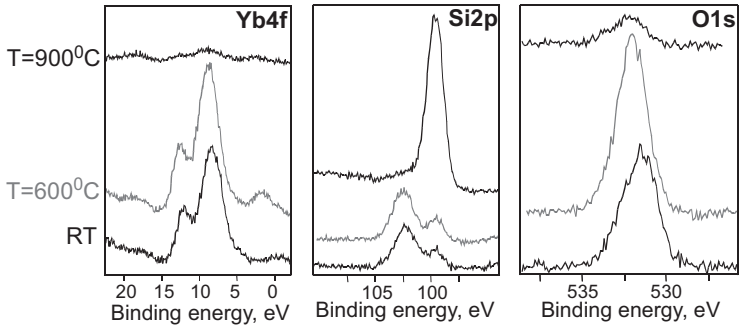


Figure 8. Yb 4f, O 1*s* and Si 2*p* lines taken from an ultrathin Yb silicate layer on Si(100): a) before annealing; b) annealed to 600^{0}C; c) annealed to 900^{0}C.

system, as revealed from XPS (spectra not shown).

The main difference is that the Yb silicate layer, initially formed at the Yb_2O_3/Si interface, is thicker ($d_{YbSiO} \approx 3$nm) than in films deposited using H_2O as oxygen source. Interesting transformations are revealed with XPS upon vacuum annealings (Figure 8) in ultrathin (1 nm) Yb silicate layers obtained from $Yb(C_5H_5)_3$ and H_2O on Si.

Unlike ultrathin $Lu_xSi_yO_z$ layers, the Yb silicate layer thus formed desorbs from the surface upon T=900^{0}C annealing. Prior to this (at T=600^{0}C), an additional peak seen in the Yb*4f* spectrum emerges in the valence band. In our opinion, this peak in the band gap close to the Fermi level (E_F) indicates defects generated in the Yb silicate layer which are forming an additional band. A more detailed picture of Yb silicate valence band evolution upon different heat treatments is shown in Figure 9. It is evident that the defects generated upon vacuum annealing are removed after annealing in O_2.

The comparison of the oxide Yb 4*f* peak in the valence band with the corresponding one of metallic Yb, indicates that indeed the defects formed upon vacuum annealing are pushing the Yb in a silicate environment to an Yb metallic-like state, which eventually results in the Yb silicate decomposition and desorption.

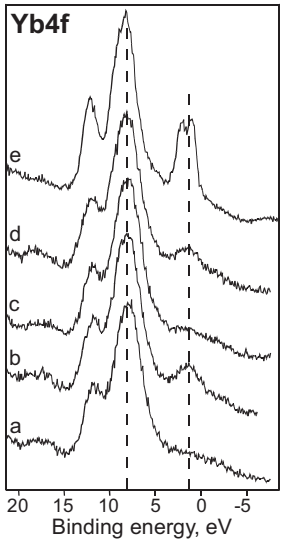


Figure 9. Valence band XPS spectra (including the Yb 4*f* line) of an ultrathin Yb silicate layer (a) as formed, and upon sequential annealings: b) T=400^{0}C in vacuum; c) T=400^{0}C in O_2 (P=10^{-2} Torr); d) T=400^{0}C in vacuum; e) reference metallic Yb with natural oxide.

The effect can be related to the established fact (particularly, for Lu) that the surface layer of RE silicates can be depleted of Si following vacuum annealing

(see above). It is worth noticing that the valence band modification upon vacuum annealing was never observed in the case of pure Yb_2O_3, i.e. it occurs only with Si present in the surface layer.

4. Conclusions

Rare earth oxides are high-κ materials which were predicted to be thermodynamically stable on Si and satisfy the main requirements to substitute SiO_2 as dielectric gate in CMOS devices. Lu_2O_3, Yb_2O_3, and Lu silicate films were grown using ALD, and the effects of annealing in different environments were studied with the combination of XPS/LEIS techniques. In agreement with other authors, it was found that both Lu_2O_3 and Yb_2O_3 are highly hydroscopic, but the ability to absorb water depends on the crystallinity of the film surface. An additional chemical state is observed for oxygen in the subsurface region of both Lu and Yb oxides, and its amount depends on sample treatment. This additional chemical state is concluded to be due to superstoichiometric O, which is loosely bound in the oxide. A variety of amorphous Lu silicates can be grown with ALD with composition depending on the growth parameters and post-deposition heat treatments. It is demonstrated that the Si/Lu ratio in the subsurface region is affected by the annealing temperature, and by the annealing environment. As grown ultrathin Lu_2O_3 and Yb_2O_3 layers on Si include an ~3 nm hydroxide layer on the surface, and a 1.2 nm (3 nm, when the film is deposited using O_3 as oxygen source) silicate layer at the interface with Si. Annealing in reduced O_2 atmosphere of these ultrathin stacks removes the hydroxide layer, but converts the oxide into a homogeneous silicate layer. The latter observation allows to conclude that, in agreement with theoretical predictions and with the experimentally observed behavior of other RE oxides, when there is no way to hinder oxygen penetration into the film, both Lu_2O_3 and Yb_2O_3 layers are not thermodynamically stable in contact with Si. Moreover, ultrathin Yb silicate layers on Si can even desorb from Si surface once annealed in vacuum to 900^0C. Prior to decomposition, a modification of the valence band is observed pushing the Yb 4*f* in a silicate environment into a metallic one. The latter effect is believed to be the result of defects generated in the silicate surface region, apparently through SiO desorption. It is therefore concluded that ultrathin Yb silicates exhibit limited stability on Si with respect to vacuum annealing, and can decompose similarly to transition metal oxides.

Acknowledgements

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TRANSIENT CHARGING EFFECTS AND ITS IMPLICATIONS TO THE RELIABILITY OF HIGH-K DIELECTRICS

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Abstract. Unlike SiO_2-based devices, various structural defects and small band gaps in high-k gate dielectrics make high-k devices susceptible to electron charging. In particular, fast transient charging in high-k devices was shown to distort the outcome of reliability tests because conventional stress and sense method cannot account for the charge decay during the delay between stress and sense. In this paper, the effect of transient charging on hot carrier stress and bias temperature instability tests of high-k devices will be examined and the technical challenges inherent in these tests will be discussed.

Keywords: Transient charging effects, high-k dielectric, hot carrier, BTI, HfO_2,

1. Introduction

During the last decade, high-k materials have undergone intensive studies with respect to their potential application as gate dielectrics. As a result, Hf-based gate dielectrics have become the materials of choice, and intensive optimizations of deposition processes have enabled impressive improvements in equivalent oxide thickness (EOT) scaling, leakage reduction, mobility, and reliability.

Several research groups have demonstrated EOT scaling below 1nm. Leakage current reduction on the order of 10^2–10^5 is also possible, providing a significant advantage over conventional SiO_2-based gate dielectrics. Mobility degradation, especially electron mobility, was one of the most serious problems of high-k dielectrics, but recent progress at SEMATECH and other companies

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has shown that the mobility of high-k gate stacks could be made comparable to SiO_2-based gate dielectrics in the same EOT range[1]. Threshold voltage (V_{th}) instability, characterized by capacitance-voltage (CV) and current-voltage (IV) hysteresis, has also improved significantly as the quality of high-k dielectrics, especially HfO_2 and HfSiON, has been improved.

As some difficulties associated with the new materials have been overcome with the recent process improvements, significant progress was made in understanding of the reliability characteristics of high-k dielectrics. The growing number of publications addressing reliability characteristics of high-k dielectrics indicates increased interest to this area. However, it is still unclear whether the test methods employed to assess the reliability of high-k devices are sufficiently accurate. Transient charging have been identified as an important factor, which may complicate interpretation of conventional DC-type electrical measurements, especially in reliability tests[2–7]. Even though optimizing high-k dielectric processes can minimize transient charging effects, high-k materials still cannot be adequately characterized using the conventional electrical techniques developed for SiO_2 gate devices. Transient characteristics of charges injected into high-k layers during conventional reliability tests can still affect the accuracy and validity of the conventional tests since even a short delay between the stress and sense measurement can result in a significant underestimation of the stress impact[8]. On the other hand, a mostly reversible shifts of parameter values caused by transient charging may add up to a stress-induced device degradation resulting in an overestimation of the reliability impact. This paper discusses recent results on the impact of transient charging on hot carrier stress and bias temperature instability of high-k devices.

2. Review of transient charging effects

High-k dielectrics are intrinsically susceptible to charge trapping due to high density of structural defects. In addition to as-grown defects, , high-k dielectrics are susceptible to defect formation caused by semiconductor processing which uses low energy plasma, in particular, in ashing and gate etching. Even though the origin of defects or the trapping process may vary, transient charge trapping in high-k dielectrics, in general, can be classified into two categories depending on the characteristic time of the trapping process: fast transient charging and slow transient charging[5].

A charge accumulation in high-k dielectrics during fast transient charging (i.e., in a matter of a few microseconds) shifts the threshold voltage of MOS devices, similar to floating body effects in silicon-on-insulator (SOI) devices [5,9]. Trap sites responsible for fast transient charging cannot hold an excess of carriers within the high-k dielectric layer, and the charges (accumulated during

device operation or reliability stress) are spontaneously emitted once the applied electric field is reduced. The accumulation and relaxation of fast transient charges affect many aspects of conventional electrical test methods developed for SiO_2 devices. Kerber et al. and Lee et al. showed that this transient charging effect could impact the drain current-gate voltage (I_d-V_g) measurement of high-k dielectrics[2,5]. As shown in Fig.1, the time of acquisition of the drain current affects the measured I_d values[5]. Young et al. showed that the ultra short pulse measurement technique could be used to quantify the amount of transient charging. The fast transient charging is shown to be proportional to the thickness of the high-k film and Hf concentration[9,10]. Additionally, after excluding transient charging effects, the intrinsic mobility of the high-k device is much higher than what has been observed with conventional measurements affected by fast transient charging.

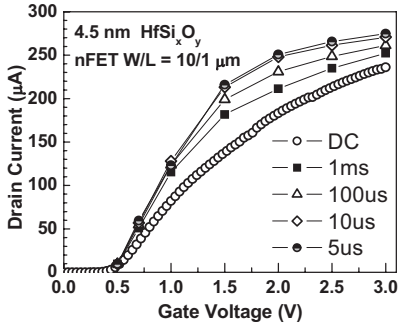


Figure 1. Drain current measured using a single pulse measurement method. Id points are averaged while applying pulses with varying amplitude to the gate. Pulse widths are varied to change the integration time. DC symbol represents conventional measurement.

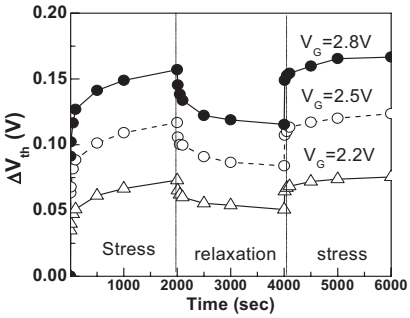


Figure 2. Charge trapping characteristics of a TiN/HfSiON NMOS. During relaxation, the stress bias was turned off.

On the other hand, slow transient charging affects the results of reliability tests, especially the long-term stress cases. Fig.2 shows a typical charge trapping and detrapping cycle. A fast initial increase in V_{th} is believed to be due to fast transient charging; a gradual V_{th} increase is due to slow transient charging. Charges accumulated during stress spontaneously decay once the stress bias is removed. A residual V_{th} shift is controlled by the stress bias and stress time. Most of the electrons accumulated during a positive bias stress can be detrapped when a small negative bias is applied, with no residual damage being generated. This behavior is different from that of SiO_2 devices, in which charge trapping causes permanent damage[11]. With negative bias stress, carrier

injection can occur from both the gate and substrate, depending on the magnitude of the electric field, and silicon-dielectric interfaces are more likely to be damaged permanently[12,13].

Note that the slow and fast transient charging processes co-exist during a given stress test. V_{th} values shown in Fig.2 are measured using a conventional I_d-V_g sweep in a reduced gate voltage range to minimize the disturbance to the trapped charge. However, in high-k devices, detrapping can occur even within a few hundred μseconds as shown in Fig.3 [14]. The V_{th} shift of HfSiON devices is reduced to a value close to the DC measurement within 250 μsec after the end of a constant voltage stress (V_g=1.65V, 100 μsec). For SiO_2 devices, there is no change. The implication of this result is that a typical delay, on the order of msecs, between the stress and V_{th} measurement may cause a significant underestimation of the stress effect in high-k devices. Thus, conventional reliability tests should be interpreted carefully, taking into account the effect of fast transient charging and its relaxation.

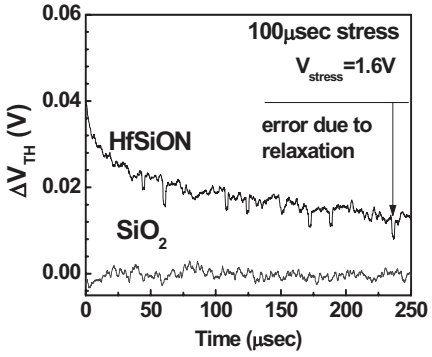


Figure 3. Drain current reduction after 100 μsec stress is measured aonverted to effective V_{th} shift. Pulse bias was +1.65 V.

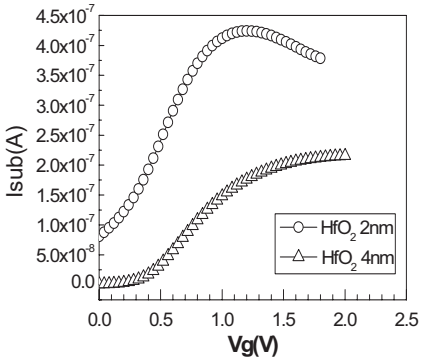


Figure 4. I_{sub}-V_g curves for films showing high level of TCE (HfO_2 4nm) and low level of TCE (HfO_2 2nm).

3. TCE and hot carrier instability

Early publications on hot carrier reliability of high-k devices used stress methods developed for SiO_2 devices such as stress at V_g=V_d/2, and 1/V_d lifetime extrapolation[15,16] without a thorough discussion on their applicability to high-k dielectrics. Interpretation of HCS still remains controversial. Several reports have shown that the charging by the channel carriers could occur concurrently with the HC changing reliability projections[18–20]. During hot

carrier stress, cold carriers from the channel region accumulate in the high-k layer and shift the device characteristics[18]. Strong Vt relaxation (see Fig.5) observed after HC stress[21] indicates that high-energy electron injection into the high-k dielectric does not generate significant permanent damage. It is difficult to separate the effect of permanent damage from that of reversible transient charging. Fig.4 shows that when a transient charging effect is significant, electrons easily accumulate within the high-k layer. Electron accumulation near the drain side of MOSFETs reduces the vertical electric field, and the peak of the substrate current moves towards the higher V_g or even totally disappears due to reduced surface scattering. Thus, in high-k dielectrics, the worst-case degradation condition is $V_g = V_d$, different from $Vg=V_d/2$ in the case of the SiO_2 gate dielectric[19]. On the other hand, when the high-k process is optimized to reduce TCE, the position of the peak of the I_{sub} curve shifts towards the conventional value $Vg=V_d/2$. However, hot carrier stress at a higher V_g using the highest I_{sub} condition increases the amount of concurrent cold carriers charging. Thus, the test conditions which would minimize the contribution to parameter shifts due to the hot electrons need to be set with taking into consideration the effect of transient charging.

Once the test conditions have been determined, the device parameters to monitor the effects of hot carrier injection should be chosen carefully because, as shown in Fig.6, hot carrier stress and constant voltage stress may result in a similar ΔV_{th} value while G_m degradation is much more severe for hot carrier stress. While the ΔV_{th} value varies over time because it includes the contribution from the concurrent reversible cold carrier charging, G_m is affected by permanent damage primarily at the interfacial layer[21]. Unfortunately, it is not clear whether lifetime extrapolations for high-k devices using a ΔG_m vs $1/V_d$ curve would be valid as G_m is not completely free from the effect of concurrent transient charging. Also, at low field stress, G_m degrades very little and is not sensitive to the electric field.

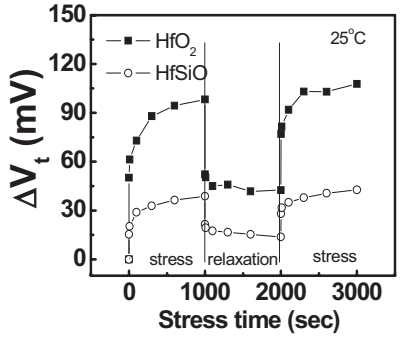


Figure 5. V_{th} shift during HCS on HfSiO/TIN and HfO_2/TIN NMOSFETS devices. HCS induced Vth shift is dissipated during relaxation.

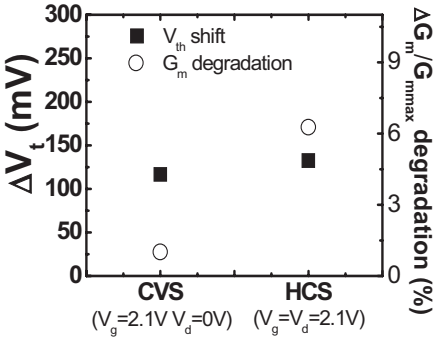


Figure 6. V_{th} shift and $\Delta G_m/G_{mmax}$ (%) degradation after 2,000sec CVS and HCS on HfSiO/TIN NMOSFETS transistor devices.

4. TCE and bias temperature instability

Negative bias temperature instability (NBTI) has been one of the most important reliability concerns for SiO_2 devices. NBTI of SiO_2 devices is believed to be due to hydrogen dissociation at the SiO_2-Si interface and subsequent hydrogen diffusion (a so-called reaction-diffusion (H°R-D) model) [22–24]. Some reports interpreted the results of BTI stress in high-k devices without differentiating high-k specific phenomena. Positive bias thermal instability (PBTI) characteristics of poly/high-k devices were studied by Onishi et al.[25], and more detailed lifetime extrapolation studies under AC and DC stress were done by Lee et al.[26]. The effects of concurrent charging and relaxation were not considered in these studies.

How the effects of transient charging, especially transient charging with longer time constant, can affect a conventional BTI mechanism remains problematic. Several groups claim that the NBTI of their high-k dielectrics show saturation behaviors similar to those of SiO_2 devices[27–30]. On the other hand, Li et al. reported that the BTI of high-k dielectrics is dominated by charge trapping at the high-k layer[31,32]. Note that the conclusions of these works came from limited sample sets, which characteristics might have been affected by non-intrinsic factors such as specifics of the dielectric deposition process, as well as of electrode materials. Krishnan et al. investigated the NBTI in HfSiON devices with a more extensive set of samples to identify the root cause of discrepancies in the literature. For SiO_2 devices, it is well known that the

exponent n of the ΔV_{th} vs time dependence is close to 0.25 in the case of neutral hydrogen species, and reaches 0.5 for H^+ under NBTI stress[23]. Fig.7 shows that the exponent extracted from thick HfSiON devices is much lower than 0.25 and approaches 0.25 as the HfSiON film becomes thinner[33]. Smaller exponent values can be interpreted as a high-k specific characteristic, which might be correlated to the stronger tunneling current components as proposed by Li et al. Since the characterization time for NBTI stress is longer than the characteristics time for fast transient charging, this result can be understood using the slow transient charging, which is also reduced as HfO_2 becomes thinner. For NBTI, both electron injection from gate electrode side and hole injection from substrate side can affect the tunneling components of V_{th} shift. For thick HfO_2 devices, the effects of slow transient charge trapping can dominate the effects of hydrogen reaction and diffusion, leading to the exponent value much lower than 0.25. For thin HfO_2 devices, the effect of the hydrogen reaction and diffusion is more pronounced than tunneling induced V_{th} shift and the exponent value is recovered towards 0.25. Note that the effect of transient charging is not fully accounted for in the ΔV_{th} measurement and PBTI cases might be underestimated than NBTI cases due to stronger relaxation.

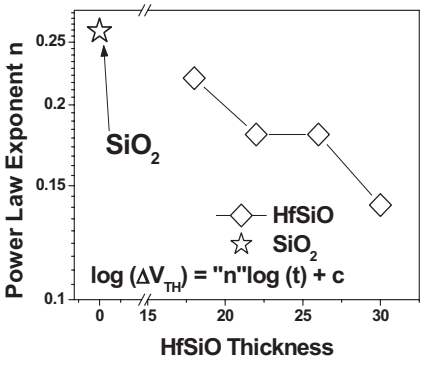


Figure 7. Power law exponent "n" for NBTI increases as the thickness of dielectric decreases.

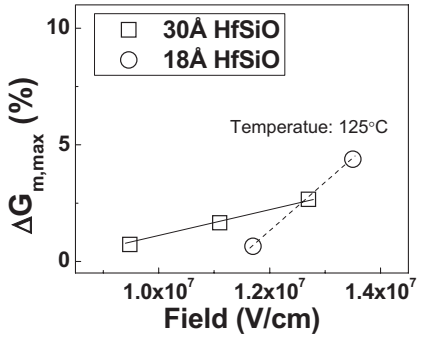


Figure 8. Temperature dependence of G_m degradation during NBTI stress.

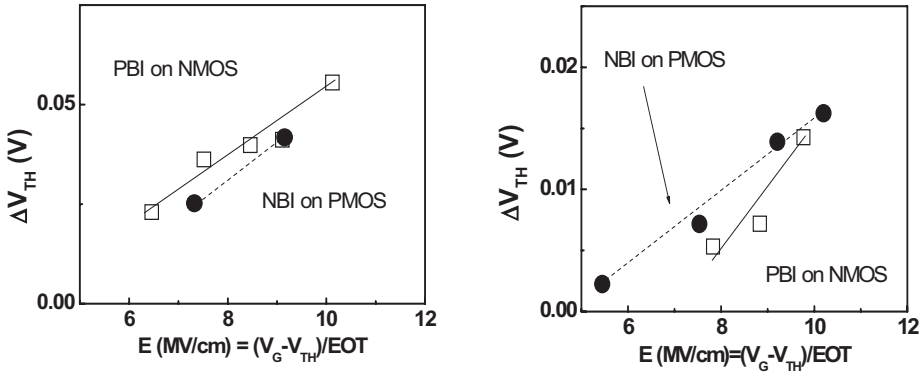


Figure 9. NBTI and PBTI of TiN/HfO_2 devices after 2000sec stress ; (a) HfO_2 3nm and (b) HfO_2 2nm. Measurement is performed at 25°C.

If the spontaneous relaxation shown in Fig.3 is taken into account, the actual exponent value will be a little lower even for thin HfSiON samples. Similar observations were made for transconductance degradation at 125°C for thin and thick HfO_2 (Fig.8). The thinner sample again showed stronger field dependence, indicating more SiO_2-like characteristics[34].

Unlike SiO_2 devices, high-k devices have demonstrated stronger BTI under a positive bias than a negative bias. A higher transient electron charging under positive bias injection conditions can explain this result[5]. However, when the transient charging is suppressed by scaling of the high-k layer thickness, this trend is reversed (see Fig.9). For 3nm HfO_2, PBI is slightly worse than NBI, with the V_{th} shift after 2,000sec stress at 10MV/cm being greater than 50mV in the former. On the other hand, for 2nm HfO_2, NBI is worse than PBI, with the base level of ΔV_{th} is less than 20mV—lower than the 3nm HfO_2 samples. These measurements were made at room temperature, but the trend remains the same at elevated temperatures (data not shown)

5. Slow transient charging and constant voltage stress (CVS)

As follows from the discussion above, V_{th} shift during CVS should be measured with taking into account both fast transient charging and relaxation effects. However, the slow transient charging effect governed by redistributing the injected charge within high-k dielectric layer further complicates CVS.

Fig.10 shows Vt relaxation characteristics after 100μsec and 2,000sec of stress. Even though the V_{th} shift after stress is similar for both cases, relaxation

characteristics are quite different[34]. The detrapping of samples stressed for 2,000sec is slower than the sample stressed for 100μsec, indicating to a smaller electric field, which drives the de-trapping process, in the former case. Smaller built-in electric field reflects more uniform distribution of the trapped charges within the high-k layer after longer stress suggesting additional electron re-distribution (relatively slow migration) across the dielectric thickness.

The temperature-dependent V_{th} shift in HfO_2 dielectrics covering a wide range of temperatures revealed that the initial Vth shift due to fast trapping is weakly dependent on temperature while slow charge trapping is strongly affected by stress temperature. Fig.11 shows that the rate of the V_{th} shift increase under long term stress is reduced at low temperatures. The charge redistribution in the high-k dielectric appears to be controlled by the temperature-activated process similar to the Pool-Frenkel process[33]. Under low temperature stress conditions, the charge re-distribution is suppressed and V_{th} shift is limited by the amount of charge initially trapped via the direct tunneling from the channel area. This points to two distinctly different charge-trapping mechanisms. Fast trapping is dominated by tunneling of channel carriers into the dielectric while slow trapping is likely due to charge diffusion between the trap sites.

The non-uniformed spatial distribution profile of the trapped charges and variable rate of charge accumulation during stress can affect the fundamental assumption of the electric field accelerated lifetime extraction methods[6], which assume a single bandgap material, monotonic defect accumulation, uniform charge distribution, and uniform electric field during a given reliability stress. When high-k devices are subjected to long stress, an electric field within the dielectric changes with changing distribution of the trapped charges resulting in preferential stressing of certain portions of the high-k dielectric. Since the special profile of the trapped charge is affected by the stress bias as implied by Fig.10, reliability test results at high stress fields cannot be directly extrapolated to low electric field cases.

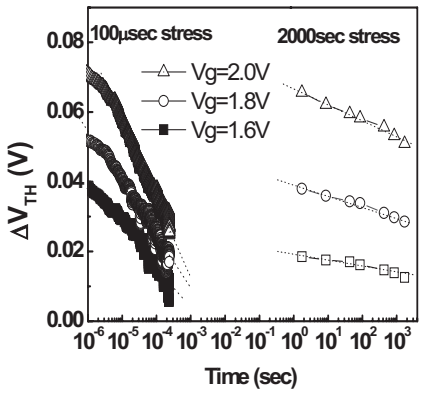


Figure 10. Relaxation measurement using on-the-fly measurement after 100μsec and 2,000sec constant voltage stress.

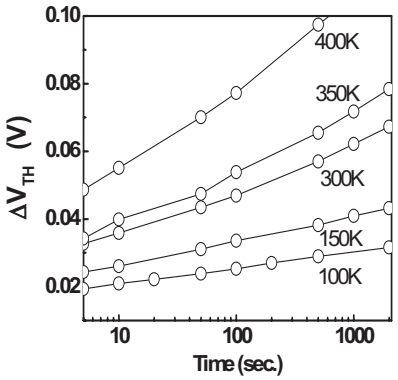


Figure 11. Temperature dependence of G_m degradation during PBTI stress.

6. Conclusion

Reliability characteristics of high-k devices are crucial factors affecting the implementation of advanced gate stack technology. Consequently, test methodologies and interpretation of test results need thorough investigation. In this paper, the effects of transient charging in high-k devices on various reliability test methods are discussed. Depending on the reliability test method used, ignoring the transient charging component may lead to either an overestimation or underestimation of device degradation. For example, the effect of fast transient charging cannot be accurately captured by a conventional stress and sensing method. Thus, any reliability test that use the V_{th} value as a measure of degradation may underestimate this degradation. On the other hand, both transient charging and damage in the interfacial oxide layer contribute to V_{th} shift during hot carrier stress. Using a V_{th} shift, that can be relaxed as soon as the stress bias is turned off, as a measure of degradation overestimate the damage caused by hot carrier stress. Even monitoring of the transconductance proposed as an alternative figure of merit for the hot carrier stress would not completely eliminate the influence of transient charging.

The nature of defects contributing to fast and slow transient charging is yet not fully understood. Intrinsic states related to a d-orbital band split at the grain boundary and oxygen vacancies are proposed as possible sources [35,36]. Nitrogen incorporation and fluorine bond formation are found to reduce the charge

trapping sites while hydrogen passivation affects only slow transient charging [36-39]. While progress in transient charging reduction may address some of the above concerns regarding conventional reliability tests, deep understanding of the transient charging effects is critical for comprehensive evaluation of high-k devices.

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DEFECT ENERGY LEVELS IN HIGH-K GATE OXIDES

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Abstract. We present calculations of the electrical energy levels of the oxygen vacancy and the oxygen interstitial in HfO_2, ZrO_2, $ZrSiO_4$ and La_2O_3. The levels are aligned to those of the Si channel using the known band offsets. In HfO_2, the oxygen vacancy gives an energy level in the Si gap or just above the gap, depending on its charge state. This is the main electrically active defect and trap. The oxygen interstitial gives levels just above the oxide valence band, and the neutral interstitial also gives a level near the Si conduction band.

1. Introduction

The scaling of complementary metal oxide semiconductor (CMOS) transistors will lead to the replacement of SiO_2 gate oxide by oxides of higher dielectric constant (κ) such as HfO_2 or ZrO_2 in order to avoid excessive gate leakage currents. Recent research has led to the choice of the best high K oxide[1-5] and provided ways to deposit closed films of HfO_2 and ZrO_2 with a much lower leakage current density than that of SiO_2. However, the performance of device s using high K gate oxides is unsatisfactory in a number of respects[5-7]. Hence, while it is clear that SiO_2 must be replaced, it is also clear that the electronic properties of the high K oxides are presently poorer than SiO_2 in that they have a higher concentration of bulk defects and a poorer interface with Si.

There are three main problems with devices using high K gate oxides. Firstly, there is a large charge trapping[7-11], which gives rise to bias instability and unreliability. Analysis by Zafar et al [8] indicates that trapping occurs into a large density of existing defects, not by creating new defects.

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Secondly, the carrier mobility is lower than in equivalent SiO_2 gate oxide devices, particularly for NMOS[5-7]. This is partly due to remote phonon scattering of carriers by soft phonons in the high K oxides[12], and partly due to Coulombic scattering by charge trapped in the gate oxide. The two effects can be separated by the dependence on the gate field and temperature[13-15]. But the fact that mobility is lower in devices with Al_2O_3 gate oxide[5], which does not have soft phonon modes, indicates that charge scattering is a problem.

The third problem is the sizeable gate threshold voltages needed to turn on transistors with high K gate oxide and poly-Si gate electrodes, compared to devices with SiO_2 gate oxide. This is partly due to an interaction between the high K oxide and the gate electrode[16].

Hence there is a need to identify the type of defects present in the oxides and their energy levels, in order to choose deposition and processing conditions to minimise the defect concentrations. Both oxygen vacancies and oxygen interstitials have been observed by electron spin resonance (ESR) in bulk samples[17,18], so it is unclear at present whether optimum conditions correspond to a high or low oxygen availability. Here we calculate the energy levels of the main point defects in HfO_2 and ZrO_2 in order to resolve these questions. We then extend these to preliminary calculations for $ZrSiO_4$ and La_2O_3.

There have been a number of previous calculations of defect energies and energy levels in HfO_2 [19-26]. The most comprehensive were by Foster et al [19,20]. They identified the oxygen vacancy and oxygen interstitial as the two most likely intrinsic defects in terms of their formation energies. The metal site defects have a higher formation energy. They also derived their energy levels. However, these calculations used the local density approximation (LDA). The LDA is well known to give good values for the total energies and structures, but to under-estimate the band gap of semiconductors and insulators by 30-50%. For bulk materials, the under-estimate can be corrected by a rigid upward shift of the conduction bands to fit the experimental gap–the so-called 'scissors operator' . However, for defects the energy levels are the heart of the problem. It is unclear in any empirical adjustment if a defect level should be moved in proportion to the gap or tied to one of the band edges. In the calculations of Foster et al [19,20], the O vacancy levels were placed below the Si band gap in the Si:HfO_2 system, but experimental trapping data[9,10] require a level just above the Si gap. Thus, either the defect level is not the O vacancy or the calculated levels are wrong.

2. Methods

Our calculations use the total energy plane wave pseudopotential code CASTEP[27]. The atoms are represented by Vanderbilt type ultra-soft pseudopotentials. The electronic exchange correlation potential is given in the

initial calculations by the PBE generalised gradient approximation (GGA) version of LDA. This has been successfully used for high K oxides and their interfaces[28-30].

The defects are created by making a periodic supercell of say 48 atoms of the original cell and removing or adding an oxygen atom. The supercell size was varied to test convergence. The structures can be relaxed to minimise their energy, for a given defect and given charge state within CASTEP. It should be noted that defect states in an ionic material such as HfO_2 are very localized so that their properties do not depend too much on the specific phase of HfO_2, only on the overall bonding. Thus calculations on the simplest phase, cubic, captures the problem.

The key problem with all LDA calculations is that they under-estimate the band gap compared to experiment. For a bulk semiconductor or insulator, it is possible to correct this band gap error approximately by the ' scissors operator' . However, for defects it is unclear in any empirical adjustment if a defect level should be moved in proportion to the gap or tied to a band edge.. Overall, existing calculations[19-24] place the O vacancy levels over a range of ~2 eV. This is not particularly useful, as the minimum information required is how the levels lie in relation to the band edges of the underlying Si.

Ideally, an ab-initio method should be used to find the defect energy levels. There are a number of methods which can give improved band gaps, such as the GW approximation[26], B3LYP[31], self-interaction correction, and screened exchange method[32-34]. The GW method is an accurate perturbative method, but it is very costly in computer time. Kralik et al[26] carried out GW calculations on the ideal neutral O vacancy in cubic ZrO_2 in a small supercell.

Another method is B3LYP. The B3LYP functional was developed to correct the over-binding of total energies of small molecules. It also happens to give reasonable band gaps for many semiconductors[31]. It does this by taking 0.7 times the exchange from Hartree-Fock plus the correlation from LDA. The LDA method underestimates the band gap, whereas Hartree-Fock with its exact exchange over-estimates the band gap. However, it is implemented for a basis set of localised orbitals, not plane waves.

Two methods that have been implemented for a plane wave basis are the screened exchange (sX) method and the weighted density approximation (WDA). The sX method [32,33] is based on Hartree-Fock, but introduces electron correlation via a simple screening term,

$$V_{sX}(r,r') = -\sum_i \frac{\psi_i(r)e^{-k|r-r'|}\psi_j^*(r)}{|r-r'|} \quad (1)$$

where V_{sX} is the non-local screened exchange potential, ψ are the Kohn-Sham orbitals and k is the Thomas-Fermi screening wavevector. The sX method has been found to give good band gaps for a number of semiconductors and

oxides[33]. However, it is still quite expensive computationally as it requires the use of norm-conserving pseudopotentials which need a higher plane wave cut-off energy than ultra-soft pseudopotentials.

In WDA, the exchange-correlation interaction is given by a Coulomb-like interaction between the electronic charge density and the exchange-correlation hole of the electrons

$$\varepsilon_{xc}(r) = \int \frac{n(r) n_{xc}(r, r')}{|r - r'|} dr' \tag{2}$$

where $\varepsilon_{\xi\chi}$ is the exchange-correlation energy density, n is the electronic charge density and n_{xc} is the exchange correlation hole which is approximated by a particular functional form [35]. The WDA method is a less well-tested functional than sX. It is faster than sX because it can use ultra-soft pseudopotentials with their lower cut-off energy. Both methods are found to give improved band gaps compared to LDA or generalised gradient approximation (GGA) methods (Table 1).

Here, we carry out calculations of the oxygen vacancy and interstitial using the GGA, sX and WDA functionals. For sX calculations, norm-conserving pseudopotentials are used with a cutoff of 600 eV. For WDA and GGA calculations ultra-soft pseudopotentials are used with a cutoff of 400 eV.

Table 1. Comparison of band gaps calculated by GGA, screened exchange and WDA, and from experiment.

Gap	GGA (eV)	sX (eV)	WDA (eV)	Experiment
Cubic ZrO_2	3.4	5.2	6.0	5.8
Cubic HfO_2	3.7	5.5	6.1	6.0
$ZrSiO_4$	4.7		7	6.7
a-$LaAlO_3$	3.1	4.4	6.7	5.6
La_2O_3	3.7	5.4	6.9	6

3. Results

The defect structures in high K oxides are the oxygen vacancies and interstitials as shown in Fig. 1. In HfO_2, due to the difference in valence between Hf and O, the cost of Hf-site defects are roughly twice that of the O-site defects. Hence, the main defects of interest are O-site defects, the O vacancy and the O interstitial.

Figure 2 compares the band structure of cubic HfO_2 obtained by GGA (with the gap opened to the experimental value) and by WDA. Fig. 3 shows the partial density of states (DOS) of a cubic HfO_2 obtained with the WDA functional. The valence band is seen to consist mainly of O p states and the

conduction band mainly of Hf d states. The conduction band is split by the crystal field into two peaks. This DOS is typical of an ionic oxide consisting of Hf^{4+} and O^{2-} ions. The GGA band gap is found to be 3.6 eV. In WDA this increases to 6.1 eV which is slightly above the experimental value of 6 eV. The sX method gives a band gap of 5.5 eV, which is a slight underestimate.

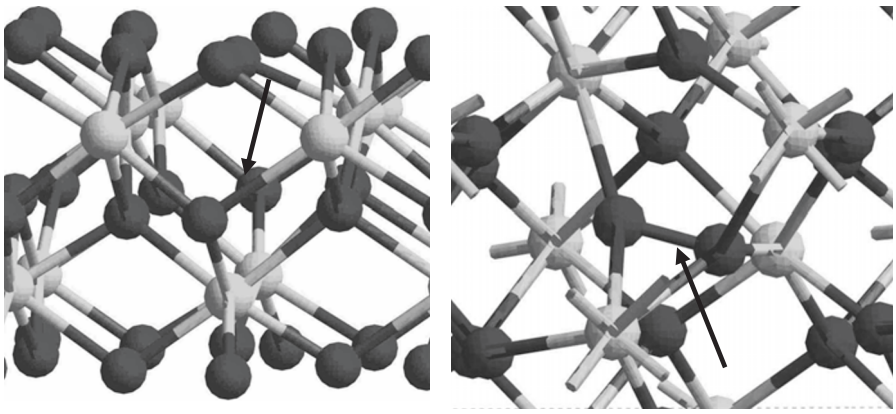


Figure 1. Oxygen vacancy and neutral interstitial in HfO_2.

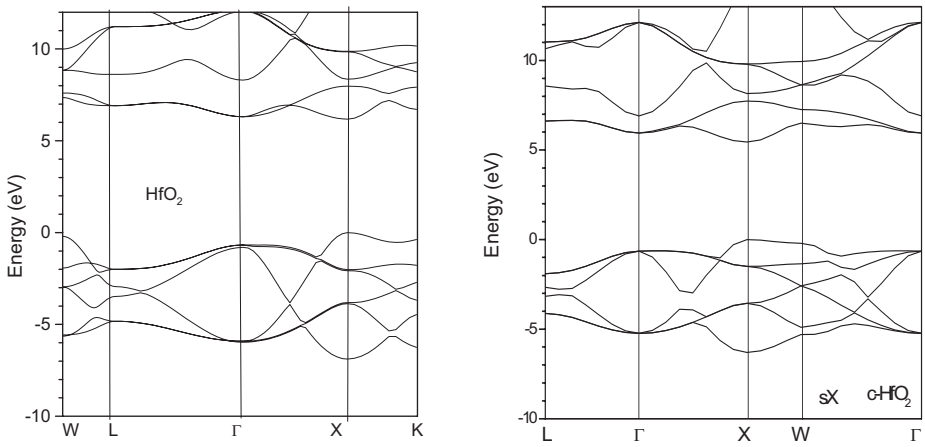


Figure 2. Band structure of cubic HfO_2 in GGA (with gap adjusted) and in screened exchange.

The structures of defects are calculated in a 48 atom BCC supercell. We first consider the ideal, unrelaxed defects and then the relaxed structures. All total energy relaxations are calculated in GGA. The oxygen vacancy creates a single gap state. This state has fully symmetric A1 symmetry and it is strongly localised on the d orbitals of the adjacent Hf ions. It is occupied by 2 electrons in the neutral vacancy. The local DOS of the Hf sites next to an ideal neutral

oxygen vacancy was calculated by GGA. The gap state lies at 3.0 eV above the oxide' s valence band (VB) maximum. The defect state eigenvalue was then calculated in the sX method. It lies at 3.75 eV. The vacancy is relaxed in GGA and Hf atoms move outwards only slightly from their ideal positions, so the Hf-Hf distance is 3.59 Å compared to 3.54 Å in bulk HfO_2. This causes the level as calculated in sX to move up by 0.05 eV to 3.8 eV. The energy levels are summarised in Fig. 4.

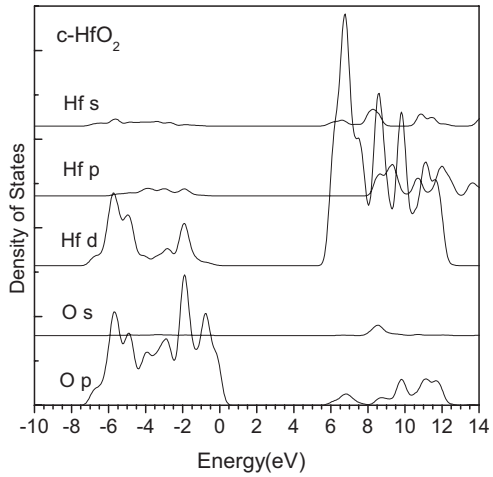


Figure 3. Calculated density of states of HfO_2.

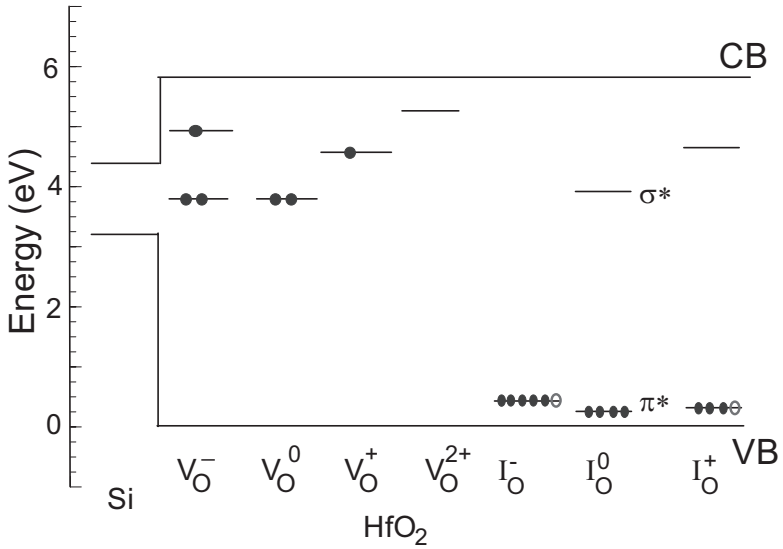


Figure 4. Summary of the energy levels of vacancy and interstitial defects in HfO_2.

The A1 defect state is singly degenerate and it is filled with 2 electrons for the neutral vacancy. For the positively charged oxygen vacancy, one electron is removed from this state. This state lies at 3.2 eV in the unrelaxed configuration. Unlike the neutral vacancy, the net positive vacancy causes the adjacent Hf ions to have a substantial outward relaxation from the vacancy site. The Hf-Hf spacing is now 3.74 Å compared to 3.54A in the bulk. This relaxation causes the defect state to move upwards from 3.2 eV to 4.7 eV, as shown in Fig 4. The amount of relaxation depends on the size of the supercell, with small cells under-estimating this. The relaxation is symmetric.

At the doubly positive vacancy, the A1 gap state is now empty. The greater positive charge causes a further outward relaxation of the Hf' s away from the vacancy so the Hf-Hf separation now increases to 3.90 Å. The gap state is now calculated to lie higher at 5.2 eV after the relaxation. A similar behaviour is found for the vacancy in the other poly-types.

We have recently found that the O vacancy also supports a negative charge state. In this case, an asymmetric relaxation brings a further state into the band gap. It is singly occupied for the V1- state. It is found to lie at about 5.0 eV, but further work is needed on this energy.

These energy levels are summarised in Fig 4. The vacancy levels lie in the upper part of the HfO_2 band gap. The levels can be aligned to the bands of the underlying Si by using the band offset of HfO_2 on Si of 3.3 eV found by photoemission by Sayan[36]. It places the neutral vacancy levels within the Si gap and the positive vacancy level just above the Si gap.

Now consider the oxygen interstitial. The O^{2-} ion forms a closed shell whose energy states all lie in the valence band. The repulsion of an extra O^{2-} ion to bulk HfO_2 will mean that it will be well spaced from the other O^{2-} ions. It will add more states to the valence band of the bulk material, with some states repelled slightly above the VB edge. We now consider other charge states of the interstitial.

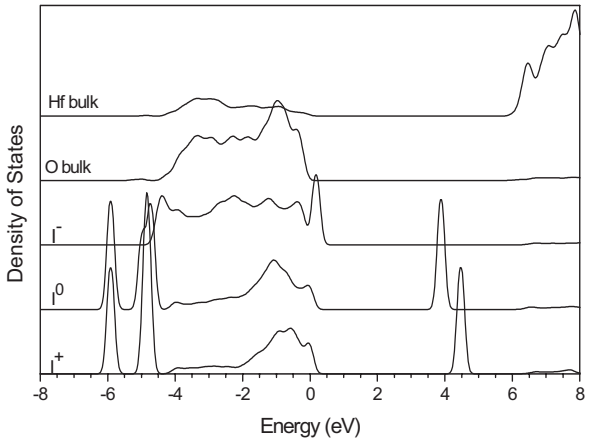


Figure 5. Calculated local density of states at the Oxygen interstitial site, for its different charge states.

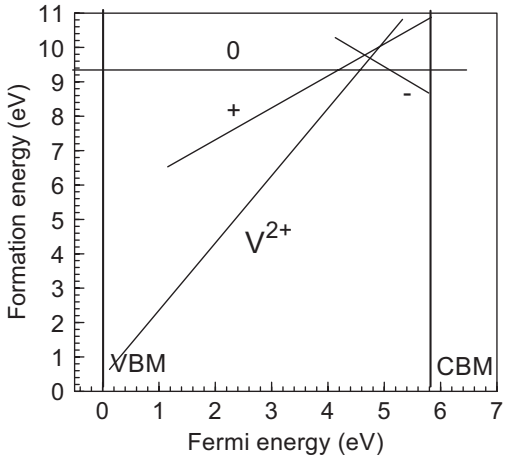


Figure 6. Formation energy of the O vacancy in HfO_2 as a function of Fermi level energy.

The O^- interstitial is similar to the O^{2-}. It is separated from the other O^{2-} ions. It now lies about 2.0 Å away from the nearest O^{2-} ion, as found by Foster et al[19]. Fig 5 shows the calculated local DOS of the O^- interstitial and on a nearby bulk O^{2-} ion. This is calculated in the spin-polarised state to allow for partial occupancy. The structure was relaxed in the GGA and the DOS was calculated in the WDA. The energy zero is referenced to the VB maximum of the bulk oxide. We see that there is now a state 1 eV above the oxide VB maximum. This is partially occupied and the Fermi level lies in this state.

Fig. 5 shows the calculated local DOS of the neutral O^0 interstitial. The structure was relaxed in the GGA and the DOS calculated in the WDA. This

configuration is shown in Fig. 1(b). There is now a clear O-O bond of bond length 1.49 Å, and the interstitial now consists of two equivalent O atoms, the original interstitial and one previously bulk O ion. It is a split interstitial with O-O axis along $\{100\}$. This structure gives rise to an empty state in the upper band gap, which lies at 4.6 eV. This arises because of the O-O bond. The empty state in Fig. 5 is in fact the antibonding or σ^* state of the O-O bond. Its bonding σ partner lies just below the main VB at - 5.5 eV. There are also filled π and π^* states lying inside the VB and just above the VB top. The empty σ^* state is a possible trap level. This configuration is sometimes called the peroxyl anion. The Fermi level in this case lies near midgap.

Next consider the positive O^+ interstitial, sometimes called the superoxy or peroxyl radical. This structure has been relaxed in GGA and the DOS calculated in the WDA. The local DOS is shown in Fig. 5. The O^+ also forms an O-O bond, but the positive charge causes the bond length to reduce to 1.39 Å. This shorter bond length leads to larger σ-σ^* splitting and repels the σ^* state towards the conduction band. The σ state falls deeper in the VB at -6.5 eV. There are still π and π^* states, and there is a hole in the π^* state above the VB. The Fermi level lies in the π^* state. It is interesting that the energy levels of these peroxyl defects are similar to those in SiO_2[37]. The states of the various interstitial configurations are summarised in Fig. 4.

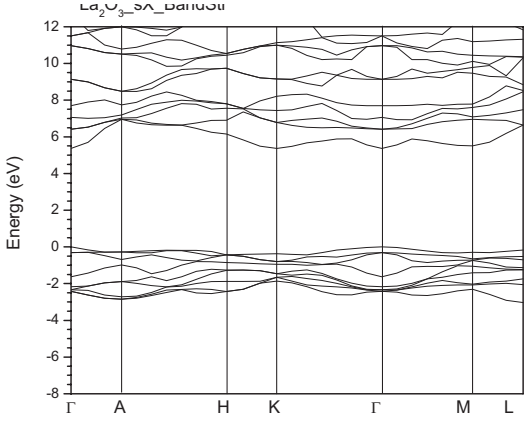


Figure 7. Band structure of La_2O_3 using screened exchange.

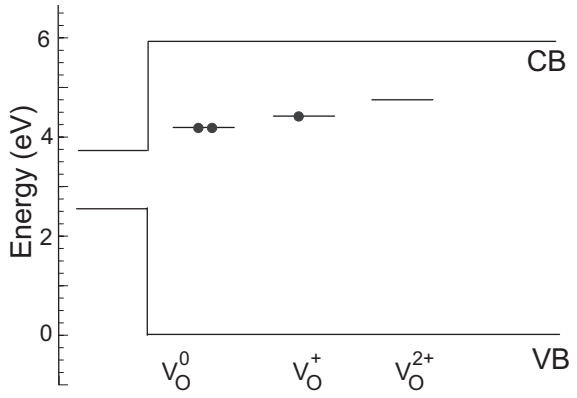


Figure 8. Calculated energy levels of the Oxygen vacancy in La_2O_3.

The silicates are other high K dielectrics which are of interest because they stay amorphous to higher temperatures. We consider defects in the crystalline phase, as a model. We use 40 atom supercells. The positive relaxed O vacancy in $ZrSiO_4$ gives a state at 4.7 eV in a gap of 6.5 eV.

Fig. 7 shows the band structure of La_2O_3 is the screened exchange method. Fig 8 shows the levels of the relaxed O vacancy in La_2O_3 calculated in sX. A 20 atoms supercell was used initially. The levels lie at 4.3 to 4.6 eV slightly above midgap, but with less variation between charge states. Howeve,r it was found that this cell did not allow adequate relaxation of the adjacent ions, for symmetry reasons. Using a larger 40 atom cell allowed proper relaxation, and the energy level now show a larger spread of energies, as in the HfO_2 case.

The energy levels can be aligned to the gap of Si using the band offsets of Hattori[38]. The CB offset of La_2O_3 on Si is larger than of HfO_2, so the levels of all charge states of La_2O_3 lie above the Si VB edge.

4. Discussion

The trapped charge in high K oxides is generally attributed to trapping in existing defect levels rather than the creation of new defects[8]. Hot carriers can create additional defects, but this is an additional effect[9]. The trapping causes hysteresis between up and down ramps of gate voltage cycles. The repeated curves follow the same cycle showing that no new defect traps are formed. Kerber et al[10] interprets this as fast trapping and de-trapping of electrons in HfO_2.

The chemical nature of all defect configurations with partly filled states can be identified by electron spin resonance (ESR). So far, most of the defects found by ESR in high K oxides are related to the Si dangling bond at the interface, called the P_b centre. Recently, Lenahan et al [17,18] identified two

paramagnetic defects in bulk films of HfO_2 subjected to corona discharge; the O vacancy and the peroxy radical. The signal at g=1.965 is assigned to the O vacancy. The three-line signal at g> 2 is assigned to the peroxy radical. The existence of a hole in a π^* state of a O-O bond of the O^+ interstitial gives rise to a very specific three-line signature in ESR. Indeed this allows this peroxyl radical to be easily recognised.

The defect levels in ZrO_2 and HfO_2 are likely to be similar. Kerber et al [10] noted that their trapping data in HfO_2 were consistent with an electrical level lying just above the Si conduction band edge. Kumar' s [9] data is not consistent with a level lying below the Si valence band edge. Takeuchi et al [39] recently used spectroscopic ellipsometry on HfO_2 films oxidised to different levels to identify an absorption band in its band gap at 4.5 eV. They attribute this to transitions from the valence band to the O vacancy, and so place the V_O level at 4.5 eV in the gap. Again, this is only consistent with levels lying in or above the Si gap. Zhang et al[40] noted that the defect is a trapped electron, meaning the V^0 to V^- transition.

The consistency of our results with trapping data implies that the O vacancy is the dominant defect in HfO_2 gate oxide films. Only the O vacancy can give an electron trap in this energy range; the interstitial gives an electron trap near the valence band. It means that conduction in HfO_2 films is by electrons, by Poole-Frenkel hopping or trap assisted tunnelling [41,42]. The trap depth is therefore of order 1 to 1.5 eV eV, that of V^- below the oxide conduction band edge.

The previous calculations of the oxygen V^+ levels in ZrO_2 and HfO_2 by Foster [19,20] placed the levels at 2.1 eV and 2.9 eV above the oxide VB edge. This places them below the Si VB edge after aligning the Si band to the oxide. The GW calculations of Kralik[26] place the vacancy levels higher, at 3.4 eV above the oxide VB, and may be a little higher if the gap is increased to the experimental value. Our results place the V^+ level in ZrO_2 much higher than Foster [19], and close to the Si CB edge. This new result is much more consistent with charge trapping data, assuming that the O vacancy is the dominant trap.

Gusev et al [43] recently found that the degree of charge trapping in HfO_2 depended on the nature of the gate electrode material. The conventional poly-Si gates cause strong trapping while tungsten gates gave much less trapping. This suggests that O vacancies are the source of traps and could be related to the faster O diffusion in HfO_2. Hf silicates are less prone to this problem.

We have also derived a formation energy diagram for the O vacancy (Fig 6). The formation energy of V^0 is taken from Foster [19], and that of the charged states from our calculated energy levels. We see that V_O possesses a large negative correlation energy or ' U' . The single positive state V^+ is unstable with respect to V^0 and V^{2+}. This was also proposed by Shen et al [22] but only on the basis of LDA calculations with their band gap error. A positive U is the normal

situation, where electrons in a defect repel each other due to their charge. A negative U is an *effective* electron-electron attraction, which arises when there is a significant electron-lattice coupling, so that the ions relax as the defect charge state changes.

Electrons are likely to be the carriers in both HfO_2 and La_2O_3.The vacancy levels lie deeper below the conduction band edge in La_2O_3 than in HfO_2. La_2O_3 also has a larger conduction band offset. This may be the reason that conduction is more by space charge limited current in La_2O_3 [44], while it is Poole-Frenkel and trap-assisted tunnelling in HfO_2.

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DEFECT-RELATED ISSUES IN HIGH-K DIELECTRICS

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Abstract. The roles of impurities and point defects are again coming to the forefront as new materials, such as high-k dielectrics, and novel device structures (e.g., double gate MOSFETs) are introduced in new generations of microelectronics. This talk covers several related issues that have been studied with a combination of first-principles theory and experiments: a) "stray" Hf atoms in Si-SiO_2-HfO_2 structures, identified by atomic-resolution Z-contrast imaging; b) the mechanism for excess point defects at the Si-dielectric interface known as negative-bias temperature instability (NBTI); c) first-principles calculations of mobilities in the presence of atomic-scale deviations from abruptness at the Si-dielectric interface; and d) first-principles calculations of Fowler-Nordheim and low-bias tunneling currents.

Keywords: hafnium oxide, NBTI, mobilities, Fowler-Nordheim

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1. Introduction

Silicon-based Complementary-Metal-Oxide-Semiconductor (CMOS) technology has already entered the nanoscale regime and faces significant challenges arising from the need to introduce new materials and novel device structures. Figure 1a shows a schematic of a MOS field effect transistor (MOSFET), which has remained in principle the same for decades, except for a scaling of feature dimensions. The main driver for a change in materials associated with the transistor gate stack is the thickness of the gate dielectric. Using the conventional material, SiO_2, the gate dielectric is currently at about 0.15 nm. In order to avoid unmanageable tunneling currents through the gate oxide, alternate dielectric materials with higher dielectric constant (high-k materials) are needed. At the same time, metal gate electrodes are being considered to replace polysilicon in order to reduce resistance, eliminate depletion of the gate electrode, and optimize the workfunction. Such a change inevitably leads to changes in the gate metal. The material of the active device, Si itself, is under pressure to change to either strained Si or SiGe to obtain enhanced mobilities. Finally, the venerable MOSFET is also under pressure for change as Silicon-On-Insulator (SOI) technology allows the fabrication of ultrathin channels and double-gate MOSFETs (Fig. 1b) and other novel structures.

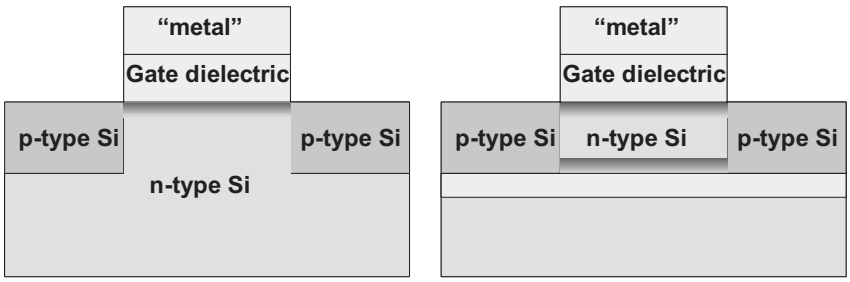


Figure 1. Schematic of a) a conventional MOSFET and b) a double-gate MOSFET (not to scale).

The inevitable material changes and novel device structures raise a number of defect-related issues. A key property of a conventional MOSFET is the low density of interface defects at the Si-SiO_2 interface. In fact, no other semiconductor-dielectric interface with comparably low interface-defect densities had ever been fabricated until recent research on high-k dielectrics has produced interfaces with defect densities that *approach* those of the conventional Si-SiO_2 interface. Control of interface defect densities leads to issues of identification of new defects, their effects on carrier densities (capture of carriers, effect on mobilities), their possible passivation, and their dynamical evolution under operating conditions (e.g., under hot-carrier stress), under radiation conditions (e.g.,

for space electronics), and under dormant aging conditions ("aging" of parts stored as long-term replacements or spares).

New materials, novel device structures, and the concomitant new defect-related issues present challenges to process and device modeling, both of which have been indispensable tools for designing manufacturable integrated circuits and systems. In particular, in device modeling, conventional methods that rely on approximations that suppress atomic-scale structure are no longer directly applicable.

This paper will give a summary of recent work by the speaker and his collaborators on defect-related issues in high-k dielectrics and novel device structures. In each of the modules, motivation for the work will be given and major results will be highlighted and discussed. Much of the work is still in progress.

2. Methods

The results reported in this paper entail a theoretical component carried out primarily in the group headed by the principal author. The primary theoretical tool is density functional theory used for total-energy calculations that allow the determination of equilibrium configurations of defect structures and related properties. These calculations are carried out in supercells, using pseudopotentials and plane-wave basis sets. In all cases, suitable convergence tests have been carried out to ensure accuracy. New theoretical developments to calculate carrier mobilities will be described in Section 5.

In one of the modules (Section 3), the theoretical work was carried out in the context of atomic-scale imaging using Z-contrast (annular dark-field) scanning transmission electron microscopy (STEM) carried out in the group headed by S. J. Pennycook at Oak Ridge National Laboratory. Images were taken using an aberration-corrected VG Microscopes HB603U dedicated STEM with 0.6-Å resolution. The intensity in the image is roughly proportional to the square of the net atomic number so that individual atoms with large Z can be observed in the background of lower-Z atoms. A novel method for three-dimensional depth-imaging was employed. Details of the method will be reported elsewhere.

In another module (Section 4), the theoretical work was carried out in the context of collaborative research with the groups headed by R. D. Schrimpf and D. M. Fleetwood at Vanderbilt University in the area of electrical measurements and device modeling. Details will be given in Section 4.

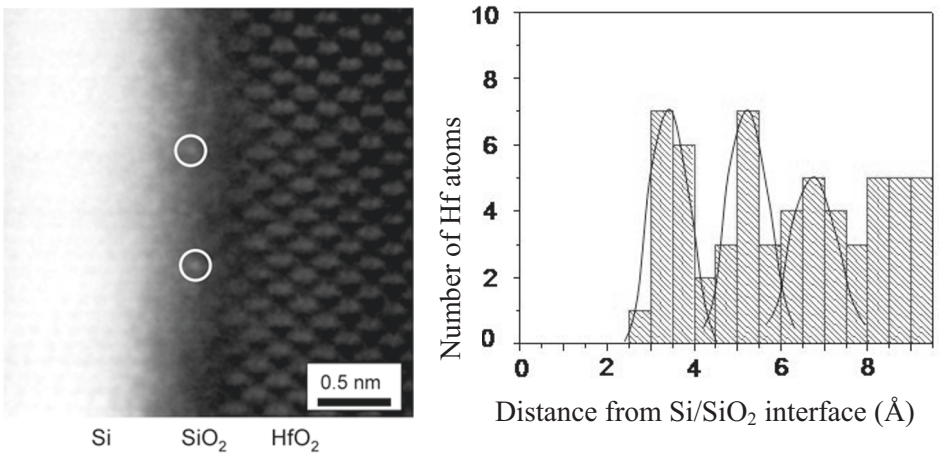


Figure 2. a) Atomic-resolution Z-contrast image of a Si-SiO_2-HfO_2 structure, showing "stray" Hf atoms in the SiO_2 interlayer; b) histogram of the distribution of the stray Hf atoms.

3. "Stray" Hf atoms in Si-SiO_2-HfO_2 structures

One of the most promising high-k alternate dielectrics is HfO_2. The latter is typically deposited on a Si substrate and some form of annealing is carried out to obtain the final structure. Typically, the annealing leads to the formation of a thin SiO_2 interlayer, resulting in a Si-SiO_2-HfO_2 structure. Thus, carriers in a MOSFET channel still travel adjacent to a Si-SiO_2 interface, which is expected to have the usual low densities of interface defects, while the gate dielectric is the combined high-k SiO_2/HfO_2. Mobilities that are roughly half of typical mobilities in conventional Si-SiO_2 structures have been reported in the literature in such Si-SiO_2-HfO_2 structures.

Figure 2a shows an atomic-resolution Z-contrast image of a Si-SiO_2-HfO_2 structure. The sample was prepared as follows. A 4-nm-thick polycrystalline HfO_2 film was deposited on a Si substrate by atomic layer deposition. The deposition was followed by a 30-second rapid thermal anneal at 950°C in N_2. Afterwards, the HfO_2 film was capped with undoped polycrystalline Si using chemical vapor deposition.

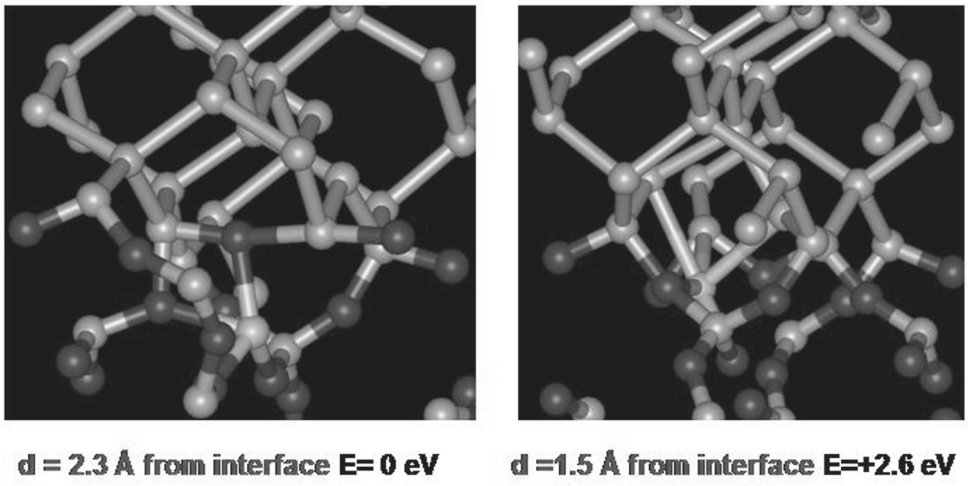


Figure 3. Schematic of Hf interstitials in SiO_2 at two different distances from a Si-SiO_2 interface. The energy of the configuration on the right is higher in energy by 2.6 eV.

In the image of Fig. 2a, the Si-SiO_2 interface is seen to be abrupt, very similar to images of high-quality conventional Si-SiO_2 interfaces. The width of the SiO_2 interlayer is about 0.8 nm. Single "stray" Hf atoms are clearly observable in the amorphous SiO_2 interlayer. By adjusting the focal point of the beam, depth profiling of the distribution of stray Hf atoms was obtained. Details will be reported elsewhere. The distances of stray Hf atoms from the nominal Si-SiO_2 interface were determined. The histogram in Fig. 2b shows that the density of stray Hf atoms peaks at 0.325, 0.525, and 0.675 nm from the nominal Si-SiO_2 interface, suggesting that the thin SiO_2 interlayer is not a completely random structure. There are no stray Hf atoms closer than about 0.25-0.30 nm from the interface.

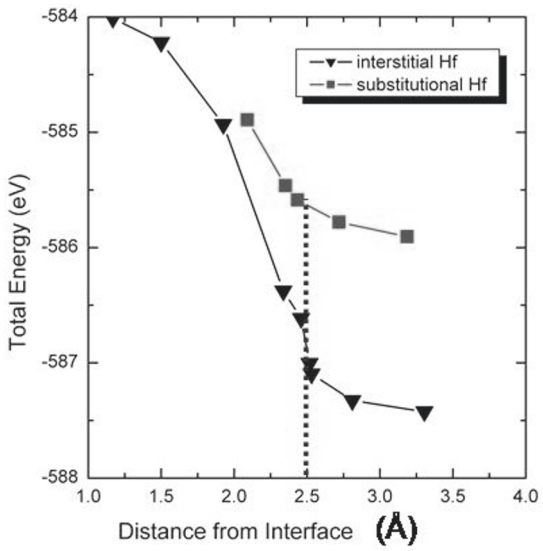


Figure 4. Total energy of single Hf atoms in the Si-SiO_2 structure as a function of nominal distance from the interface.

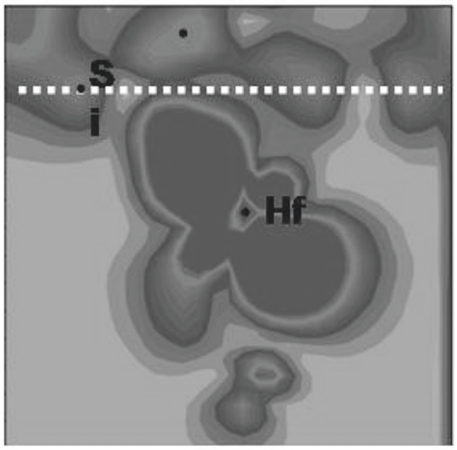


Figure 5. Wave function of the 4d localized state of a Hf atom as shown schematically in Fig. 4, plus the wave function of electrons at the bottom of the Si conduction band The dotted line is the interface. A

The possible configurations of stray Hf atoms in a Si-SiO_2 structure were probed using density-functional calculations and model atomic-scale structures. Two interstitial configurations are shown in Fig. 3a and 3b. The nominal distances from the interface are 0.23 and 0.15 nm, respectively. In the case of the Hf atom at 0.15 nm, "damage" in the Si substrate occurs, which raises the formation energy by 2.6 eV relative to that of the Hf atom at 0.23 nm. Results of such calculations at various distances are collected in Fig. 4. It is clearly seen that the energy rises rapidly if Hf atoms are taken closer than about 0.25 nm, in agreement with observations. Similar results were found for substitutional Hf. Details will be given elsewhere.

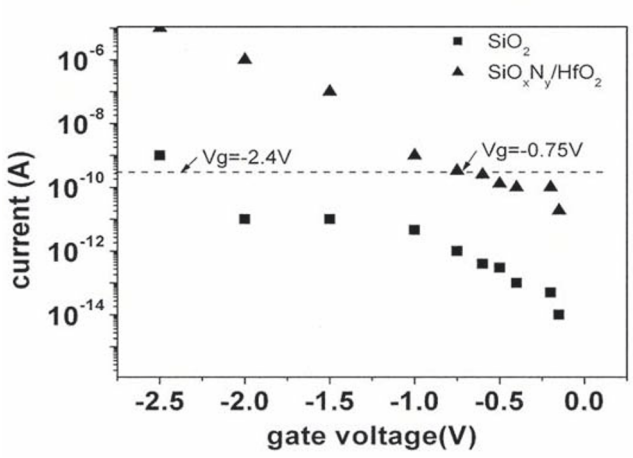


Figure 6. Leakage currents in a MOS structure with SiO_2 and in a MOS structure with SiO_xN_y/HfO_2. From Zhou et al. (Ref. 1)

The experimental images of stray Hf atoms have not so far been correlated with electrical measurements of mobilities and leakage currents. The theory, however, suggests that, when stray Hf atoms are present in the SiO_2 interlayer, they are likely to cause enhanced leakage currents. Several of the configurations that we examined have localized levels in the energy region of the Si energy gap. Figure 5 shows the wave function of such localized states (primarily Hf 4d) overlapping wavefunctions of electrons in Si substrate. It is clear that such states in the Si energy gap can be the cause of enhanced leakage currents that are typically observed in Si-SiO_2-HfO_2 structures (Fig. 6). One possibility is a percolation path through stray Hf atoms. Otherwise, individual Hf atoms can act as stepping stones for resonant tunneling.

The effects of Hf atoms on carrier mobilities are currently under investigation using the theoretical methods of Section 5. Correlation of Z-contrast images with mobility measurements and leakage-current measurements is also under way.

4. Negative-bias temperature instability

At slightly elevated temperatures (100-200º C), MOSFETs under negative bias exhibit degradation resulting from increased interface defect densities and increased positive charge trapped in the oxide. Measurements of the phenomenon in Si-SiO_2 and Si-HfO_2 structures (Fig. 7) reveal that the latter are more susceptible to NBTI degradation. In both cases, the activation energy is ~0.3 eV, suggesting that similar mechanisms are responsible for the phenomenon.

There have been several suggestions for the NBTI mechanism over the years, but a comprehensive treatment based on first-principles calculations was provided only recently by Tsetseris et al.[2] It is generally assumed that the observed activation energy, extracted from an Arrhenius plot, corresponds to the energy barrier for the "rate-limiting step" in a series of reactions. From such a perspective, the NBTI observed activation energy, ~0.3 eV, would be a puzzle. If all energy barriers are $\leq$0.3 eV, the phenomenon would occur too rapidly for measurements to be possible even at room temperature.

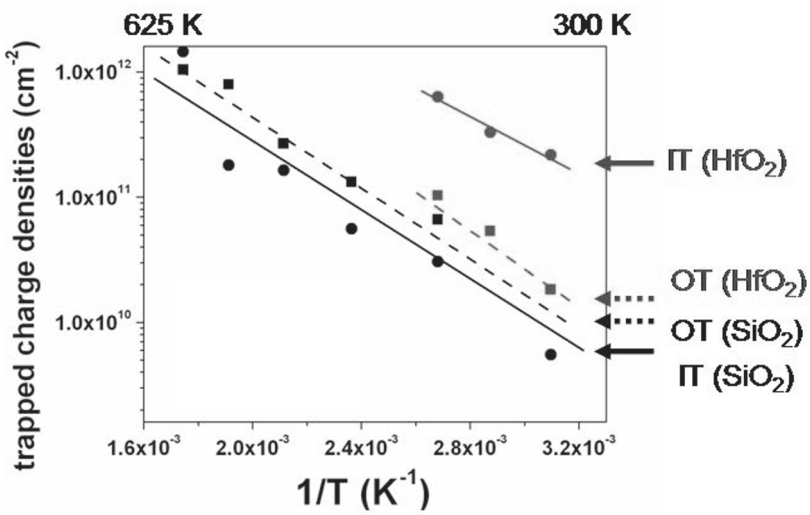


Figure 7. Increased trap density at the interface and in the bulk dielectric under NBTI conditions for SiO_2 and HfO_2 dielectrics (from Zhou et al., Ref. 1).

The theory proposed by Tsetseris et al. resolves the quandary in an elegant way as follows. Under NBTI conditions, H is released near the interface as H^+ (see below), which migrates in the area and depassivates dangling bonds, forming H_2 molecules. The latter diffuse away, but can also undergo the reverse reaction and re-passivate dangling bonds. Depending on the relative energy barriers of the various diffusion-reaction steps, a quasi-equilibrium can be achieved. In such a case, a theory developed in the 1970's by Jepson and Svensson[3] is applicable. First-principles calculations have led to the following results: Energy barrier for depassivation reaction: E_a = 1 eV; reaction energy for depassivation reaction: ΔE = 0.5 eV; migration energy for H_2: Q_{H2} = 0.45 eV; migration energy for H^+_2: Q_{H2} = 0.8 eV. According to the Jepson-Svensson theory, under quasi-equilibrium conditions, the observed activation energy for depassivation would be

$$E = \tfrac{1}{2}\Delta E + \tfrac{1}{4}Q(H_2) = 0.35 \ \text{eV},$$

in excellent agreement with observations.

The only remaining issue is the source of H^+ in the Si side of the interface. The most likely source is dopant impurities, which are known to bind H. During the annealing step that produces passivation of dangling bonds at the interface, a fraction of dopants near the interface are also likely to capture a H and be deactivated. This small fraction is adequate for NBTI because the release of H from dopants is enhanced by the presence of holes caused by the negative bias.

The enhanced NBTI degradation seen in the data of Fig. 7 may be caused by the presence of higher concentrations of passivated dangling bonds in Si-HfO_2 interfaces and also by any stray Hf atoms in the SiO_2 interlayer as discussed in Section 3 above. Such Hf atoms can also bind H atoms that can be removed by arriving H^+ ions.

5. First-principles calculations of carrier mobilities

As already noted in Section 3, stray Hf atoms in Si-SiO_2-HfO_2 structures may be responsible in part for the observed lower carrier mobilities in such structures. Inclusion of this effect in standard mobility models would be difficult because one has no simple way to construct a model scattering potential using empirical parameters.

Other effects are resulting in serious difficulties with conventional mobility modeling. The Si-SiO_2 interface has been routinely modeled as an infinite potential barrier for carriers in the channel. Thus, wave function penetration in the oxide is not taken into account. With stray Hf atoms as close as 2.5 – 3 Å to the interface, wave function penetration is clearly important. In addition, the band-offset between Si and SiO_2 is not quite a step function (Fig. 8) so that, in a very thin SiO_2 interlayer, the infinite-barrier model breaks down completely.

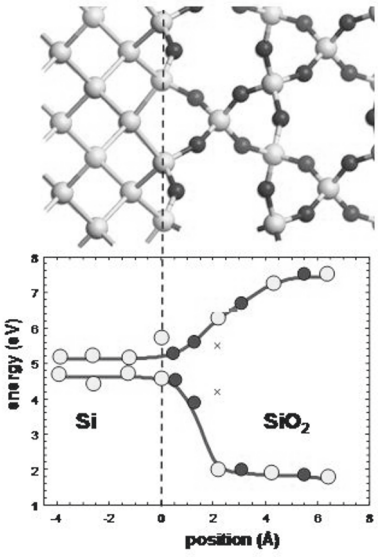


Figure 8. Band gap variation across a Si-SiO_2 interface calculated using DFT.

Ultrathin-channel double-gate devices based on SOI technology also raise questions for conventional mobility modeling. Mobilities in such structures do not track the "universal mobility curve" (Fig. 9). With ultrathin channels being as thin as 1-2 nm, suppression of atomic-scale detail is not viable. Consider for example an ideally abrupt Si-SiO_2 interface. If a single "O protrusion" is present (Si-O-Si chain on the Si side of the interface), as much as 25% of the channel is "blocked". Thus, calculations of mobilities using atomic-scale models of a MOSFET with quantum mechanical rigor are called for.

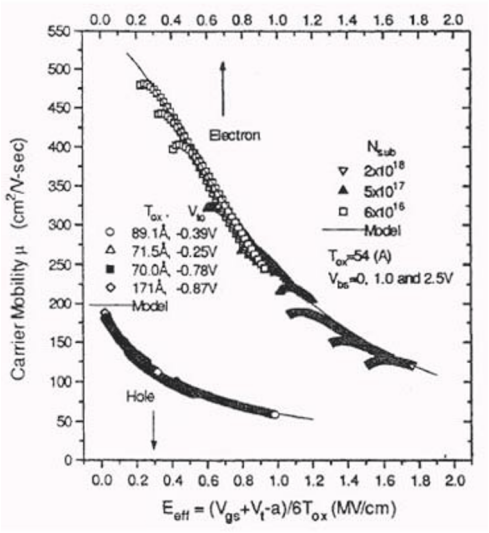


Figure 9. The universal mobility curve for electrons and holes in Si (From Ref. 6).

A method for first-principles calculations of mobilities has been developed and implemented for a double-gate MOSFET. A Si-SiO_2-Si… superlattice is used. Ideally abrupt interfaces are employed first and the self-consistent DFT potential is calculated. Single atomic-scale defects are then introduced, e.g., an O protrusion, a suboxide bond (Si-Si bond on the SiO_2 side of the interface), or a stray Hf atom is introduced and, after all relevant relaxations are allowed to occur, the self-consistent DFT potential is recalculated. The difference with the reference potential of the ideally abrupt structure is then treated as a scattering potential for electrons or holes. Mobilities are calculated using a linear approximation to the Boltzmann equation and the Born approximation for scattering rates (a higher-order theory has been developed, but is not yet implemented).

Initial results for O protrusions and suboxide bonds are shown in Fig. 10. The key point is that these defects, which constitute atomic-scale roughness, do not reduce mobilities at low-electron densities (low effective fields). Thus, they do not account for the observed deviations of mobilities in UTSOI MOSFETS from the universal mobility curve. The most likely mechanism for the observed mobility degradation at low electron densities is long-wavelength roughness (e.g., steps). Calculations of the effect of stray Hf atoms in UTSOI MOSFETs are under way.

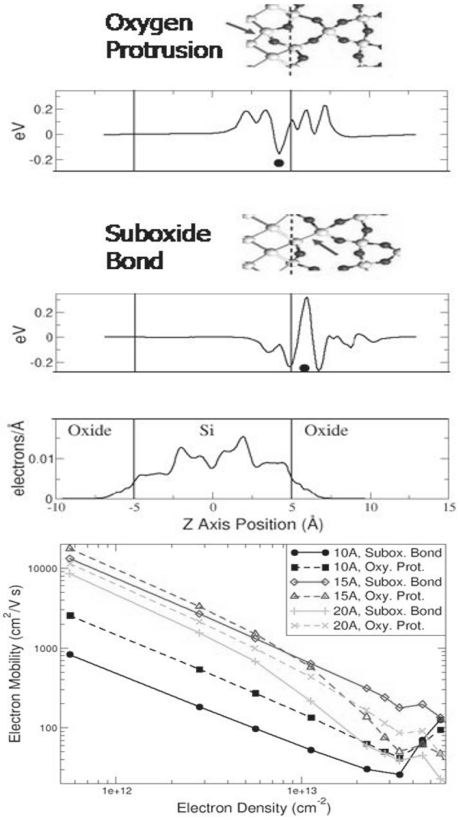


Figure 10. Top two panels: scattering potentials; third panel: electron density (note the penetration into the oxide); lower panel: calculated mobilities (solid curve: suboxide bond;dashed curve: O protrusion).

6. Fowler-Nordheim tunneling and leakage currents

At high enough voltages, tunneling through an oxide film can be modeled by tunneling through a triangular potential barrier, as first formulated by Fowler and Nordheim in 1928.[4] The theory has formed the basis of "Fowler-Nordheim tunneling" in MOSFETs. With ultrathin oxides, the usual model proves to be inadequate. The key reason is again the suppression of atomic-scale detail. Indeed, the usual FN model is based on effective mass theory and an abrupt, step-function-like band offset at the Si-SiO_2 interface (the effective mass of the carrier also changes abruptly at the interface).

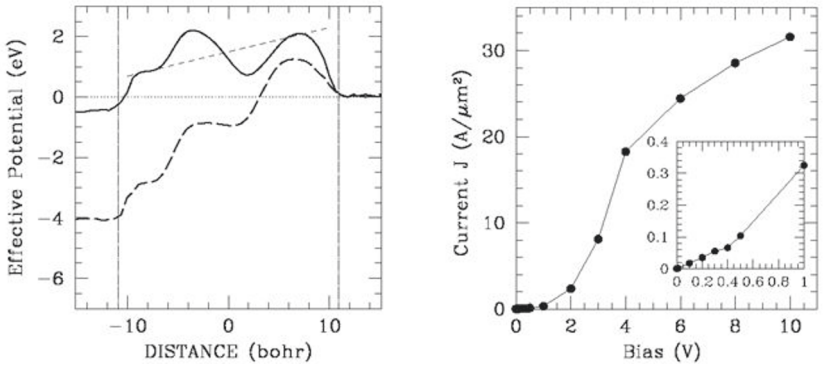


Figure 11. Left: The self-consistent potential in a metal-SiO_2-metal structure for 1 V and 4 V. Right: Current vs voltage. The Fowler-Nordheim regime is 0.5-4.5 V.

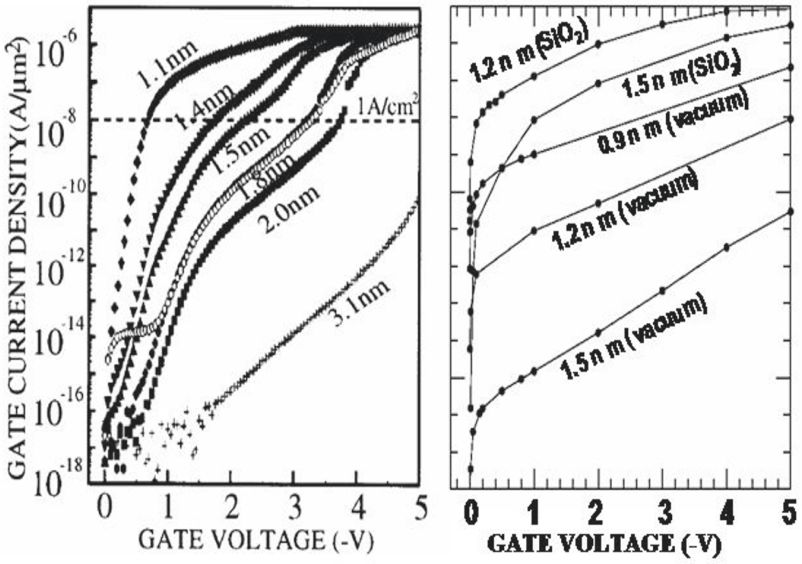


Figure 12. Current-voltage characteristics for several thicknesses of SiO_2 Left: experiment (from Timp et al, 1998); Right: theory for SiO_2 films and for vacuum "films". The theory has been scaled to correspond to experimental electron densities

In recent years, the author's group reported calculations of current-voltage characteristics of individual molecules connected to model "jellium" electrodes (homogeneous electron gas, with nuclei smeared out into a uniform positive background).[5] The Lippmann-Schwinger method was used, as first developed by Lang (see Ref. 5). The method has been extended for periodic structures and

applied to thin SiO_2 films between jellium electrodes (modeling the metal gate and doped Si, respectively). Results are shown in Fig. 11 and 12.

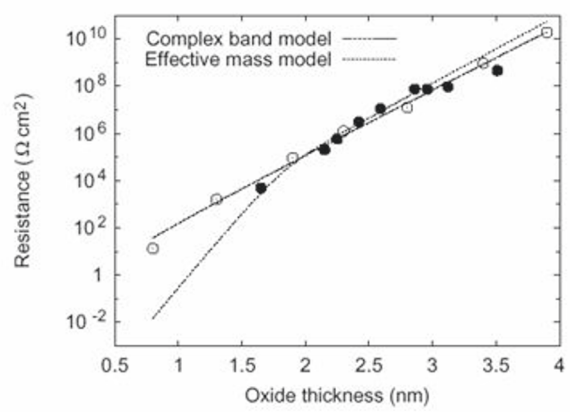


Figure 13. Resistance of ultrathin SiO_2 films as a function of thickness.

A key point of the atomic-scale calculations is that the real electrons (as opposed to effective-mass electrons) do not experience a band offset. Instead, they experience the actual atomic-scale potential, which is continuous across the interface (see Fig. 11). The point is best seen for small voltages, the regime of conventional tunneling. At infinitesimally small biases, the band offset presents a barrier of several volts that the effective-mass electron must tunnel through. On the atomic scale, however, the potential experienced by the real electron is continuous. At the Fermi energy, the current is carried by a single wave function that has a Bloch character in the "electrodes", but has evanescent character in the oxide. The evanescent solutions of the crystal Hamiltonian are normally discarded for the perfect crystal because they do not obey the pertinent boundary conditions. They are relevant in the case of a thin oxide, however, as they are connected to Bloch functions in the electrodes.

A theory based on evanescent waves in the oxide (energy bands with complex-wave vectors) has been developed and applied to tunneling current through thin oxides. The results for tunneling current as a function of thickness in the linear regime (infinitesimally small bias) are shown in Fig. 13, compared with data. A single parameter needed to capture the contact resistance, assumed to be the same in all samples) was used to normalize the theory against the data. The theory can be used to explore leakage tunneling currents in the presence of point defects such as stray Hf atoms, O vacancies, etc.

Acknowledgements

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STUDYING THE EFFECTS OF NITROGEN AND HAFNIUM INCORPORATION INTO THE SIO_2/SI(100) INTERFACE WITH REPLICA-EXCHANGE MOLECULAR DYNAMICS AND DENSITY-FUNCTIONAL-THEORY CALCULATIONS

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Abstract. By combining large-scale classical molecular dynamics simulations, the replica exchange method and *ab initio* calculations, we have studied how the incorporation of nitrogen and hafnium affects the physical and chemical properties of the silicon/silicon dioxide interface. This paper focuses on the determination of the structure of the SiO_2/Si(100) interface and on the changes induced on its microscopic characteristics by nitrogen introduced at different concentrations (in the range from 1% to 14%). Characteristic Si- and O-centered defects are observed and in particular N-centered defects—also unforeseen ones. Additional defects emerging after hydrogenation are also considered. The effects of silicon replacement with hafnium atoms at various levels in the interface region are also studied, both in the stoichiometric and substoichiometric oxide.

Keywords: silicon dioxide; silicon oxynitride; defects; high-k dielectrics

1. Introduction

The motivation for the research we present here lies in the ever growing need for a better understanding of the microscopic structure of nanoscale interfaces between silicon and oxides such as SiO_2 and SiON, currently used in CMOS devices, or HfO_2 , which is considered for application in the near future (for recent reviews, see e.g. Refs. 1,2,3). A large amount of data and knowhow has

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been accumulated over the years, both from experiment and from calculations of diverse levels of sophistication, on SiO_2 and its interfaces with silicon. However, a few outstanding questions are still open concerning the physical behavior of this material, which are related to the mechanisms responsible for the dielectric breakdown when the thickness is reduced to less than 2 nm. The investigation of microscopic changes induced by nitridation of films in the sub-nanometer scale is more recent and apparently less clearly understood. Concerning the understanding of HfO_2 /Si interfaces, progress continues to be made daily, but it is still unclear whether (or to what extent) heavy-metal atoms penetrate the silicon substrate after deposition.

Our investigation[4] is based on computer simulations of SiO_xN_y/Si(100) interfaces (with stoichiometric composition $y = 2(2-x)/3$ and also nonstoichiometric with moderate oxygen excess) for a nitrogen content $\xi = y/(x+y) = 0$ (pure SiO_2), ~1, ~3, ~6 and ~14%. Hafnium atoms were also incorporated with concentration x ranging from ~1 to ~5% in replacement of silicon atoms at various positions in the dioxide as well as in the suboxide region. The determination of the structure of the SiO_xN_y/Si(100) interfaces was made using the Molecular Dynamics (MD) driven replica exchange (RE) method[5] which greatly enhances the sampling rate of the configurations and also allows one to monitor the system behavior at different temperatures. In these MD simulations the interatomic interactions were described with DFT-derived potentials[6]. In particular, some unforeseen defect configurations are found which are N-centered and increase with N content. DFT calculations of these defect configurations and others with added hydrogen (in the neutral and positively charged states) were performed on smaller samples.

DFT calculations are also performed to characterize the changes induced by hafnium replacing silicon atoms of different oxidation states, at low concentration, and to determine the relative thermodynamic stability of the corresponding configurations as well as their electronic structure.

2. Computational scheme

2.1. METHODS

In the simulations we describe in the following sections, both *ab initio* approaches and classical potentials for molecular dynamics simulations were adopted.

The *ab initio* calculations were performed within the framework of density-functional theory using the Perdew-Burke-Ernzerhof[7] approximation for the gradient-corrected exchange-correlation energy functional, norm-conserving angular-momentum dependent pseudopotentials[8] to represent the interaction of

the valence with core electrons, and plane waves as basis set for the expansion of the wave functions up to a 80 Ry cutoff[9]. For SiON(H) systems we refer to our results on the structural and dielectric properties of bulk phases[10], which document their validity. In the case of hafnium, the validity of the pseudopotential scheme (with f-electrons considered frozen in the core) was also verified on bulk properties of Hafnia[11].

The classical potentials for Si, O, N and H—which are coordination-dependent and are based on an extension of the Tersoff potential for silicon[12] — were consistently derived from fitting to DFT-PBE results[9] that we have obtained for a relatively large set of compounds and configurations[6] via simultaneous energy and force matching[13]. In particular, an additional number of tests were made against DFT-PBE results, on structural characteristics, vibrational spectra, and the energetics of defects.

In the REMD simulations, 128 replicas, distributed over temperatures ranging from 50 to 1500 K, were explored for each system and each one for a period of time ranging from 2.5 to 3.1 nsec.

2.2. MODEL SYSTEMS

The atomistic models used to represent the interfaces consisted of 3D periodically repeated slabs in which the oxide was sandwiched between two ~8A thick silicon multilayers so as to prevent spurious truncation effects. Indeed this configuration is physically interesting because it can be considered to represent the environment of the dielectric film in MOSFET devices, where it is sandwiched between silicon and polysilicon.

In classical MD simulations, the samples contained 2088 atoms, the global thickness of the oxide corresponded to 18– 20 Å, and the periodically repeated cell had dimensions 32.54 Å × 32.54 Å × 33.70 Å. In the DFT calculations, the samples contained 522 atoms, and were obtained by cutting the original model so as to reduce the dimensions of the unit cell to 16.27 Å × 16.27 Å × 33.70 Å.

3. Results

3.1. SiO_2/Si(100)

Simulations of this interface were aimed at providing a realistic atomistic model on which one could investigate how its physical properties can be modified by the inclusion of hetero-atoms, depending on their nature and on their concentration. In previous studies, also the most advanced ones to-date[14,15], structural models of SiO_2/Si(100) were generated so as to represent some empirical data

before-hand. Clearly this type of approach does not offer the flexibility necessary for our purposes. As discussed in Sect. 2, in our search for a thermodynamically stable structure we do not enforce any constraint on the atomic coordinates and make use of the REMD method to efficiently sample the configurational space. Here we briefly review the main results of our research that are discussed in more detail in Ref. 4.

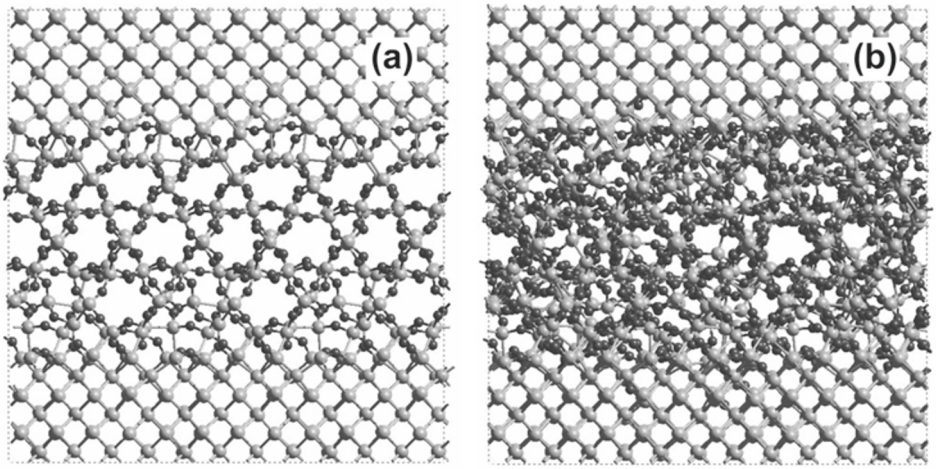


Figure 1. (a) Initial configuration (abrupt interface) and (b) snapshot of a low-temperature configuration resulting from our simulations.

Our REMD simulations start from an abrupt interface (see Fig. 1(a)) with a moderate excess of oxygen atoms randomly distributed on the silicon backbonds. The system is observed to progressively undergo a strong rearrangement as can be seen in Fig. 1(b). In particular, the distribution of the substoichiometric oxide species rapidly establishes itself. Figure 2(a) shows the time evolution of the relative concentrations of silicon atoms in oxidation states Si^{+n} with n = 1, 2, and 3, averaged over all replicas comprised in the temperature range 200– 400 K. The statistical average at room temperature corresponds to ratios Si^{+2}/Si^{+1} = 1.4 and Si^{+3}/Si^{+1} = 1.6. The values of these ratios derived from fitting to experimental data exhibit a non-negligible scattering e.g. from 1;1 [16] to 2;2 [17] to 2;3 [18,19], and seem to depend on the type of experiment as well as on a number of factors related to the sample itself, such as film thickness[17] and growth conditions[20]. The Si^{+1} atoms are generally indicated as the minority species and also the ones whose distribution is less affected by either thickness or temperature. Still comparison with experiment cannot be straightforward unless a step forward is made in the calculations and on the basis of a structural model, theoretical photoemission spectra are determined. The average

distribution of silicon atoms we calculate at room temperature is shown in Fig. 2(b) for all five oxidation states. The Si^{+1} component slightly penetrates into the substrate as a consequence of oxygen diffusion, and the Si^{+3} component protrudes into the bulk SiO_2. Indeed Si^{+3} species have been observed to have a relatively higher extension, from the earliest X-ray photoemission study[21] to more recent angle-resolved Si 2p photoemission[19]. One can try to estimate the width of the suboxide from Fig. 2(b), for example as the distance between the first maximum of the Si^{+1} distribution and the first maximum of the Si^{+4} one, which amounts to ~6 Å. A variety of measurements on films of different thickness (see e.g. Ref. 19, 22,23) indicates a value closer to 5 Å.. Again the correspondence between specific experimental observation and the outcome of a profile plot is not a one to one correspondence.

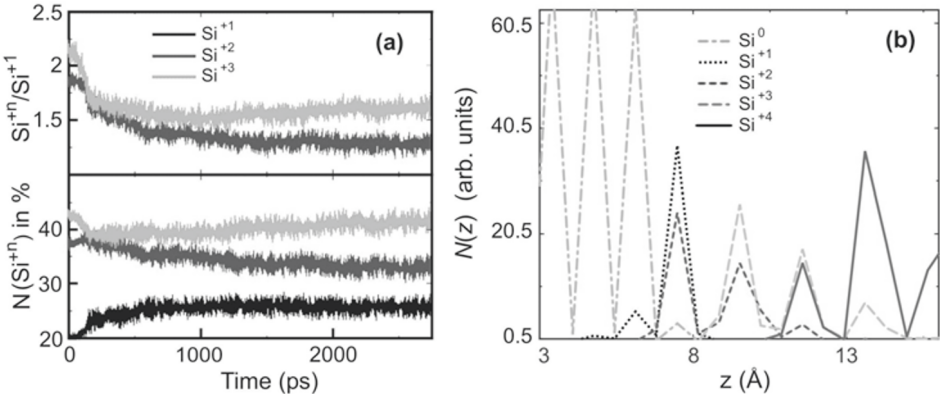


Figure 2. (a) Time variation of the distribution of silicon atoms in sub-oxidized states; and (b) Average density profile of all states calculated at room temperature (see text).

In spite of the strong rearrangement of the atomic positions, a pattern rapidly established itself on the surface layer, similar to that observed in cristobalite. This feature corresponds closely to high-resolution electron microscopy (HREM) [24] observations on very thin films and also by XRD[25] on thicker samples. The formation of this ordered cristobalite-like pattern in the proximity of the substrate drives an increase in the atom density over the transition region: on average, we calculate a 10% enhancement over 6 Å towards the Si layers. This fact is consistent with – although not directly comparable to – the observation of a "high-density layer" of 10 Å in the transition region of thicker films (40 Å)[26].

Unlike previous models that were constrained to be defect-free[15,27] our results show the presence of the characteristic defects of this system, namely, under-coordinated Si and over-coordinated O atoms, the latter having maximum concentration in the proximity of silicon. Being forcedly diamagnetic, no direct

comparison with ESR experiments can be made. As expected, their average density (taken over the 200– 600 K temperature range) is higher than what ESR indicates for real systems, namely, by a factor of 2 to 10, depending on the reference system (see e.g. Ref. 28).

While detailed comparison with experiment awaits for simulations of the processing of the material, such as to generate a structural model similar to thermally grown silicon oxide, the results here obtained provide a physically sound ground on which the effects of incorporation of heteroatoms can be studied.

3.2. SiON / Si(100)

Recently we have undertaken an extensive investigation of the interfaces of oxynitrides with silicon. For comparison with a number of previous studies (see e.g. Ref. 29, 30) we refer to Ref. 31 . In this section, we describe only our most salient and novel findings.

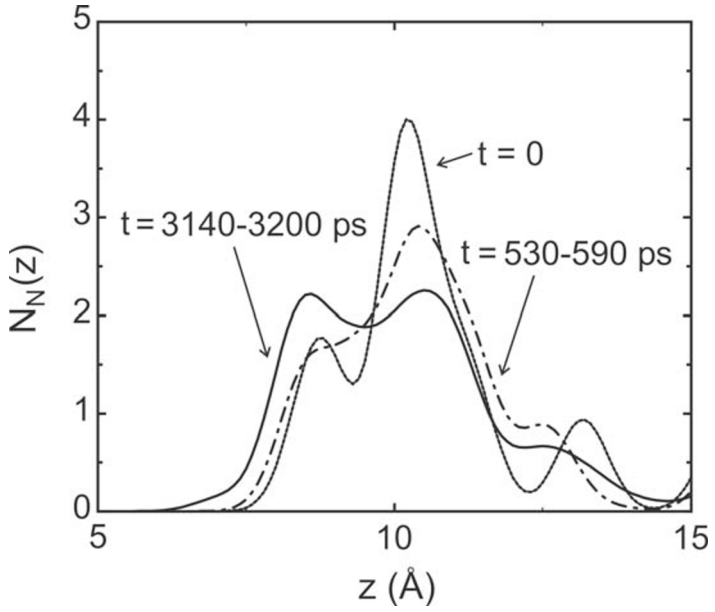


Figure 3. Nitrogen profile calculated for the ξ = 3% sample at room temperature.

Starting from a low-temperature configuration found above for the bare interface, we have incorporated nitrogen atoms for concentrations corresponding to ~1, ~3, ~6 and ~14% of nitrogen content ξ. In the initial configurations the oxygen atoms were replaced by nitrogen atoms throughout the system but

according to a given profile. However no constraint was enforced on the atomic coordinates. Figure 3 shows how the nitrogen profile changed over time for the ξ = 3% sample. The tendency of nitrogen to localize itself closer to silicon is apparent. That important changes take place during the REMD simulations is evidentiated by the transformation of the large majority of nitrogens from two- to three-fold coordinated. In Fig. 4 we have plotted the change with time of the number of defects for all the species observed in the ξ = 6% sample, which is however representative of all cases calculated. As expected three-fold coordinated nitrogen atoms (not shown in the figure) evolve so as to form the stable network of the nitridated interface at the expense of the two-folded coordinated species that dramatically decrease. This is accompanied by the manifest increase of the number of under-coordinated silicon atoms, while the amount of over-coordinated oxygen does not seem to be affected by the reconstruction of the structure. Interestingly a tiny amount of unforeseen 4-fold coordinated nitrogen (Si_4-N) emerges. With DFT calculations we have verified that this result was not an artifact of the classical potential scheme.

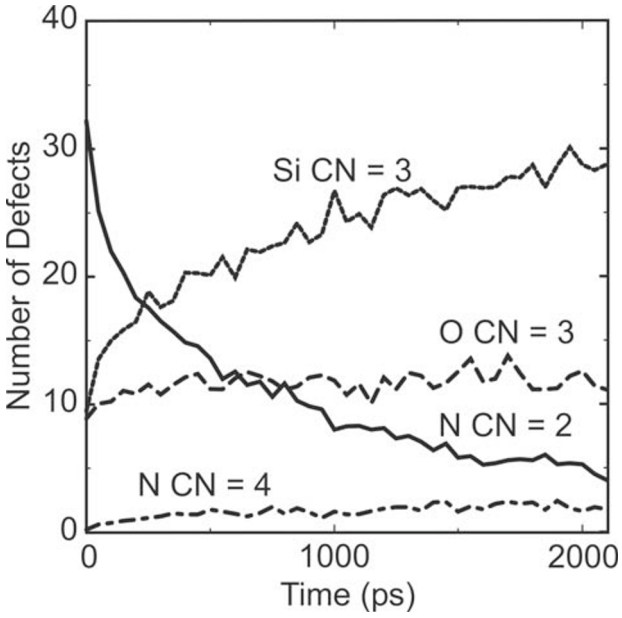


Figure 4. Time evolution of the number of the various characteristic defects observed in the ξ = 6% sample at room temperature.

With increasing nitrogen content (see Fig. 5) we observe that unlike over-coordinated oxygen atoms, the density of both nitrogen- and silicon-centered defects also increases. In particular this is true for the 4-fold coordinated nitrogen. We notice that contrary to the case of under-coordinated silicon (the

majority defect) that can be passivated by hydrogenation, over-coordinated nitrogen cannot be removed with this procedure.

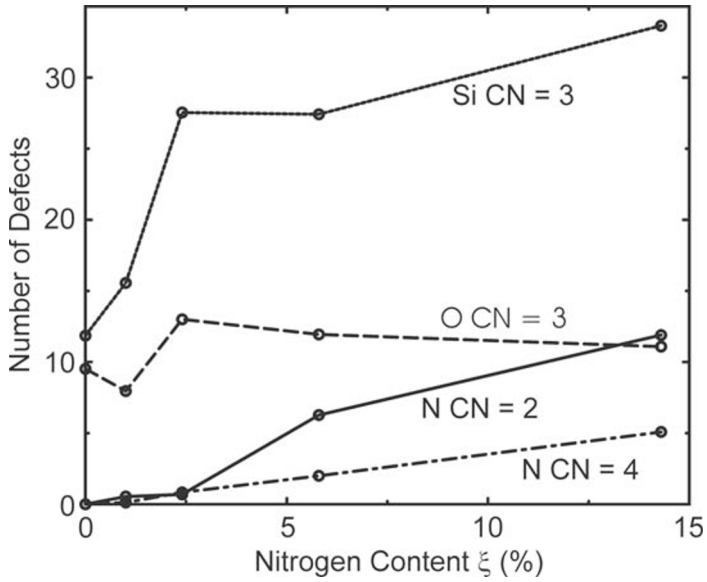


Figure 5. Number of defects as a function of nitrogen content, at room-temperature.

Given the well-known high stability of positively charged 4-fold-coordinated nitrogen (e.g. in ammonia salts), the nitrogen configurations here detected might form positively charged defects that can act either as fixed charges or electron traps. Moreover, positively charged 4-fold-coordinated nitrogen could also be generated by hydrogen sticking at network 3-fold coordinated nitrogen (Si_3-N) and also at formerly hydrogen passivated 2-fold coordinated nitrogen. DFT calculations of the binding affinity of hydrogen, both neutral and ionized, were performed. In particular binding affinities for the Si_3-N species are 1 eV for H and 4.1 eV for H^+, only slightly lower than those for Si_2-O in silica (1.1 and 4.4 eV respectively). Interestingly, the formation of Si_3-NH^+ in plasma-nitridized SiON/Si(100) systems has recently been invoked[32] as a possible ESR-inactive interface defect which can contribute to near-bias temperature stress (NBTS). A detailed investigation of N-induced defects is currently underway using first-principles calculations with the aim of determining the mechanisms by which they can contribute to negative-bias temperature instability (NBTI) and affect electron mobility.

3.3. Hf AT SiO_2/Si(100)

The effects induced by incorporation of hafnium in the SiO_2/Si(100) interface were investigated[11] for hafnium concentrations of 1% and 5%. Only configurations were studied, in which hafnium enters as a substitutional impurity. As reported in Table 1, hafnium strongly prefers to replace a silicon atom in the dioxide rather than in the suboxide region. This is consistent with the fact that hafnium-rich silicates are stable in structures with high coordination (6– 7) and in this system the tetrahedral coordination is the highest possible. The change of local environment, compared to silicon, amounts to a 0.2– 0.3 Å expansion of the bond lengths, which is a sign of localized strain. Unlike silicon-silicon distances, hafnium-silicon distances shrink with decreasing number of coordinating oxygens.

Table 1 Energy and bond lengths (in Å) of interface configurations with hafnium replacing one silicon atom of a given oxidation state (1% hafnium). Energies are referred to the lowest state that corresponds to hafnium located in the dioxide region. Si-Si and Si-O distances are calculated in the interface without hafnium.

Oxidation State	Energy (eV)	d_{av} Hf-O	d_{av} Si-O	d_{av} Hf-Si	d_{av} Si-Si
+4	0	1.92	1.64	–	–
+3	1.2	1.92	1.65	2.65	2.36
+2	2.5	1.85	1.67	2.57	2.36
+1	3.1	1.81	1.67	2.57	2.36

Although hafnium is unlikely to penetrate into the suboxide according to mere thermodynamics grounds, it is interesting to consider the modifications that such an event would involve. Our most interesting observation refers to the case of the replacement of silicon in the +1 state. An increment of the electron density at the Fermi edge emerges already for a hafnium content of 1% and is further enhanced at 5% as shown in Figure 6(b). These new states are hafnium-related states and are delocalized in the proximity of the silicon substrate, as illustrated in Figure 6(a). This scenario might be considered as the precursor of a metallic interfacial layer.

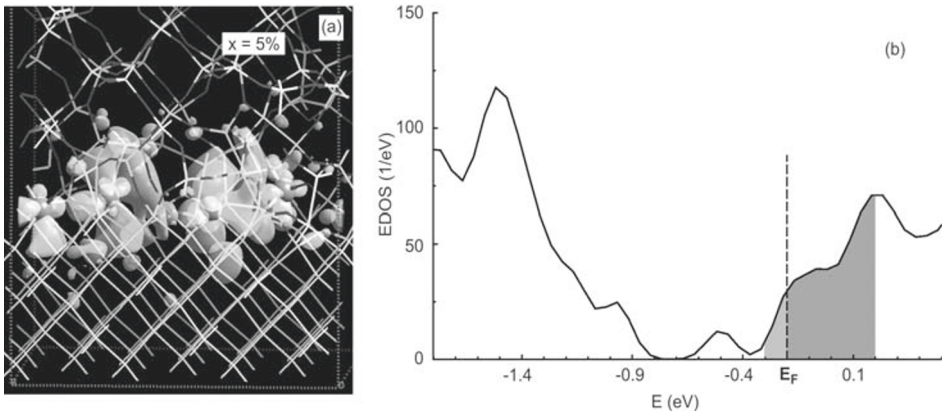


Figure 6. SiO_2/Si(100) with Hf replacing Si^{+1} atoms in the suboxide at a concentration of 5%. (a) Density of electron states around the Fermi level and (b) a representative isosurface of the corresponding probability density. Circles denote hafnium atoms.

An early attempt[33] to calculate the effects of the incorporation of hafnium on different layers of the interface also concluded that the metal atom prefers to be located in bulk-like SiO_2. However a direct comparison cannot be made with our results, because the configurations considered for the substitutional hafnium did not differ in its oxidation state. Indeed that model did not account for a substoichiometric region. The interface, whose unit cell had lateral dimentions of the silicon unit cell, was abrupt (β-quartz SiO_2 with an oxygen bridge aimed at eliminating interface states due to unsaturated bonds) so that only Si^{+2} was present as sub-oxidized species.

4. Conclusions

We believe that by combining the accuracy of the DFT method and the power of REMD simulations of large-scale systems, real progress can be made in the understanding of complex interfaces like those of SiON and high-k oxides with silicon. The results briefly surveyed above are intended to be only the beginning of a new and systematic approach to the study of their structural and electronic properties, and in particular of defects introduced during material processing .

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PROBING POINT DEFECTS AND TRAPS IN STACKS OF ULTRATHIN HAFNIUM OXIDES ON (100)SI BY ELECTRON SPIN RESONANCE: INTERFACES AND N INCORPORATION

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Abstract. The results of an electron spin resonance (ESR) analysis of (100)Si/HfO_2 entities with ultrathin layers of deposited amorphous (a)-HfO_2 are overviewed. The main ESR signals observed in the as-grown samples and after VUV irradiation were P_b-type interface defects. However, when using $Hf(NO_3)_4$ as a precursor in chemical vapor deposition (CVD), the incorporation of N is revealed after ^{60}Co γ-irradiation through the observation of NO_2 radicals. The molecules are found to be stabilized and likely homogeneously distributed in the a-HfO_2 network. Some network forming N entity is suggested as a precursor, transformed into ESR-active NO_2 upon γ-irradiation. The interesting N incorporation into the HfO_2 network appears inherent to the particular nitrato CVD process and correlates with dominant electron trapping in these hafnia layers as revealed by electrical measurements in combination with photo-generation of charge carriers. Generally, in the HfO_2 films obtained using other (N-free) CVD chemistry, hole trapping is found to dominate the oxide charging.

Keywords: point defect; high-κ dielectrics; electron spin resonance; charge traps; HfO_2; nitogen incorporation; chemical vapor deposition; MOS; C-V measurements

1. Introduction

Very resolutely, the International Technology Roadmap for Semiconductors 2003 (ITRS) predicts a reduction in gate insulator thickness to an equivalent Si

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oxide thickness (EOT) < 1 nm for the 65-nm technology node.[1] The incessant scaling, primarily at the basis of the impressive advancements achieved in of metal-oxide-silicon (MOS) based devices, will demand, among others, the introduction of new insulators of dielectric constant κ higher than that of conventional SiO_2 (κ=3.9): Conventional SiO_2 will be found failing when used at such small thickness mainly due to intolerable (tunneling) leakage currents and problems with intrinsic reliability. Obviously, the potential success of any alternative high-κ insulator in technology hinges critically on the control of charge traps, that is, structural imperfections (defects), either of intrinsic or extrinsic origin, both at critical interfaces and in the bulk of the layers. Indeed, charge trapping centers are an issue. [2, 3] As to the Si/dielectric interface, the challenge additionally implies attainment of uncontaminated interfaces of superb thermodynamic stability, smooth to carrier scattering.

Currently, HfO_2, or perhaps rather Hf-oxide based composites, such as its silicates ($HfSi_xO_y$) and nitrated silicates enjoy much attention –in fact, the materials are actually considered for use in functional devices– because of distinguishing characteristics including high-κ value (~3.9-20, depending on Hf content), good thermal and chemical stability in contact with Si,[4-7] and favorable conduction and valence band offsets with respect to Si (2.0 and 2.5 eV, respectively).[8] Furthermore, the incorporation of nitrogen (N) into high-κ-layers may potentially ensue additional beneficial properties such as improving the layer's diffusion barrier properties, thermal stability (e.g., against crystallization), electrical properties, and κ enhancement. It is then only natural to strive for insight in how N is (atomically) incorporated in the network, the concentrations typically encountered, and to find out about its stability. Such an aspect is addressed in this work for HfO_2 films deposited using a particular chemical vapor deposition (CVD) method.

In simultaneously addressing microstructure, bonding chemistry, and composition of newly composed Si/high-κ dielectric stacks, numerous material characterization tools are combined,[9,10] providing a wealth of useful and pertinent information. This research is paralleled by intense electrical study indicating the presence of, besides interface traps, substantial densities of traps in the HfO_2 layers. Moreover, their density and type (charge) turns out to depend profoundly on the applied deposition technique and modalities (e.g., chemicals).[11-14] However, when it comes to assessing the atomic nature of the structural imperfections (point defects) at the origin of these electrically active traps these techniques, superb as they are, inherently fail. Such information, in principle, can be obtained from electron spin resonance (ESR) probing. Naturally, with defects presents, a key question emerging is whether their origin would be mainly intrinsic or, rather, extrinsic –a well pertinent question as for the newly applied high-κ oxides on Si, CVD techniques are often used for oxide layer deposition:[15] These deposition techniques, such as atomic layer (AL)

CVD, may cause impurities (e.g., Cl, C) to be symptomatically incorporated on the 1 atomic % level.[10] Hence, large fluctuations over the various (CVD) techniques may result, raising a matter of concern.

The number of ESR investigations on Si/high-κ entities is still limited.[16-20] Initial K-band work[16] studied stacks of (100)Si with nm-thin ALCVD layers of ZrO_2 and Al_2O_3, and simultaneously addressed the role of SiO_x and Al_2O_3 inter-layers. The P_b-type (trivalent Si) interface defects P_{b0} and P_{b1} –the archetypal defects for the (100)Si/SiO_2 (SiO_xN_y) interfaces– are the sole defects observed in the as-grown state. Compared to Si/SiO_2 they are observed in enhanced densities. This was confirmed by electrically detected magnetic resonance[17] on ALCVD (100)Si/Al_2O_3 and (100)Si/ZrO_2 entities and a X-band ESR work[18] on ALCVD grown (100)Si/Al_2O_3. The latter additionally reported a second signal, the D center generally ascribed to unpaired Si bonds in disordered/amorphous Si, which has likely originated from Si substrate damage. Several more works addressed the Si/HfO_2 entity. A first one[19] compared (100)Si/HfO_2 entities grown by three variants of CVD (see discussion below). Also here, in the as-grown state, the P_b-type defects were reported as predominant defects. In agreement, a second X-band work[20] reported the observation of P_b defects at the interface of nominally (111)Si/HfO_2(14.5 nm) entities manufactured via ALCVD using the nitrato precursor $Hf(NO_3)_4$ (NCVD).

It thus appears that a major ESR result so far attained implies the detection of P_b-type defects (P_{bo}, P_{b1}) at the Si/insulator interfaces. Observation of signals from as-deposited dielectric films themselves appears much less successful, despite the report of the presence, in general, of substantial densities of charge traps.[11-14] This situation, however, is not much different from that of the classical Si/SiO_2 case, where, except from one EX defect,[21] ESR also fails to trace defects in the as-grown SiO_2 layer. Generally, successful application of ESR requires defect activation (charge state) by some kind of irradiation by energetic particles or charge injection.

The scope of present work concerns the ESR observation and identification of a defect, albeit extrinsic, in CVD HfO_2 films deposited on (100)Si using the $Hf(NO_3)_4$ precursor. The centers, identified as embedded NO_2 radicals, expose the inherent incorporation of N into the HfO_2 layers during deposition. From parallel electrical study, evidence is presented that the incorporation of N correlates with the occurrence of negative traps in the Hf oxide.

2. Experimental details

2.1. SAMPLES INVESTIGATED

Three types of samples were studied, obtained by depositing HfO_2 (100-110 nm thick) on (100)Si (n and p type; ~800 μm thick) in technological facilities via different CVD procedures, which include[19] (1) ALCVD at 300 °C using $HfCl_4$ and H_2O as precursors at a pressure of ~1 Torr; (2) metallo-organic (MO) CVD at 485 °C from tetrakis-diethylaminohafnium ($[(C_2H_5)_2N]_4Hf$) and O_2. To improve the initial HfO_2 nucleation, in both cases, the Si substrates were subjected to the IMEC clean followed by oxidation treatment in ozonated water leaving an Si oxide layer of about 0.7 nm thick;[22] (3) NCVD on HF-last (100)Si surfaces at 350 °C, that is, in nominally H and C free conditions,[23,24] unlike the two previous methods. After initial ESR tests, to reveal defects, separate sets of samples were subjected to either VUV ($h\nu$=8.48 eV) photons (~3×10^{17} cm^{-2}) emitted by a Xe resonant lamp or ^{60}Co γ-irradiation to a dose of 50 Mrad(Si).

For the electrical measurements the same types of samples were used, but with thicknesses of the insulating layers ranging from 3 to 110 nm. The samples were either left in the as-deposited state or subjected to post-deposition annealing (PDA) at temperatures between 500 and 1000 °C for 10 min in a mixture of N_2 + 5 % O_2. The latter treatment was carried out to trace temperature-induced effects, yet without growing a substantial $SiO_{2(x)}$ interlayer between Si and the HfO_2 insulator. After deposition and PDA, MOS capacitors were formed by thermoresistive evaporation of 0.5-mm^2 semitransparent (13-15 nm) Au metal electrodes onto the oxide without any further thermal treatment.

2.2. EXPERIMENTAL METHODS

Conventional CW absorption-derivative ESR measurements were performed at K and Q band in the temperature range T= 4.3-35 K under slow passage conditions. Applied modulation amplitude B_m (~100 kHz) of the magnetic field (**B**) and incident microwave power P_μ were sufficiently restricted to avoid signal distortion. More details can be found in Ref. 19. ESR samples were (100)Si slices of 2× 9 mm^2 area with the 9-mm edge along a [0 $\bar{1}$1] direction. Typically, an ESR sample was comprised of 12-15 slices which backside was treated in a HF-H_2O mixture immediately before each ESR observation.

A comparative study for the different oxide deposition methods has been carried out taking the approach of detection of the stable trapped charge resulting from photogeneration (PG) of carriers[25] in oxide as a function of its thickness. The PG of electron-hole pairs in the oxide was realized by

illumination through the semitransparent gate electrode with 10-eV photons emitted by a Kr resonant lamp. The density of stably trapped electrons/holes was determined from the shift of the flat band voltage (V_{fb}) on 100 kHz capacitance-voltage (C-V) curves normalized to the specific capacitance of the studied MOS structure. The charges related to the Si/oxide interface states were separated from those pertaining to the oxide defects by comparing the charging kinetics observed in the MOS structures on p- and n-type Si.

3. Experimental results and discussion

3.1. P_b-TYPE INTERFACE DEFECTS

It has been reported before[19] that the predominant ESR signals detected in the as-grown sample state or after VUV irradiation were P_b-type defects. In the AL- and MOCVD samples no clear signal could be traced from the high-κ films, not even after γ-irradiation. For the NCVD sample, however, the situation appears strongly different. Here a prominent spectrum was observed, as illustrated in Fig. 1 (a), showing a typical K-band ESR trace for **B** along the [100] sample normal **n**. Extensive measurements as a function of incident P_μ level (in the range 0.3-8 nW) and **B** direction (angular dependence) indicated the spectrum to originate from at least two different centers. As expected[19] the first one is the P_{b0} signal at g=2.0060(1) for **B**//**n**, exhibiting the expected angular dependence in terms of g, and splitting into three components for **B** rotating in the (0 $\bar{1}$1) plane away from **n** towards the (011) direction; the density is inferred as (8 ± 0.3) × 10^{12} cm^{-2}, similar to the as-grown state.[19]

3.2. NO_2 RADICALS

Interestingly, upon γ-irradiation there appears a second signal in the NCVD sample: It implies a rich multi component spectrum, which can be considered as consisting of three sets of highly-resolved asymmetric lines, behaving fully isotropic and all constituent peaks responding identically to P_μ saturation (no spectral change): the spectrum was found to be slightly more saturable than P_{b0}. Combined with the particular peak shapes these observations show that the spectrum is a powder pattern (or, perhaps a combination of several) of an anisotropic center embedded in an amorphous matrix. To be short, it became quickly evident that the spectrum could be well simulated by the powder pattern of a center characterized by the effective spin S=½ Hamiltonian comprised of the electronic Zeeman and hyperfine (hf) interaction terms

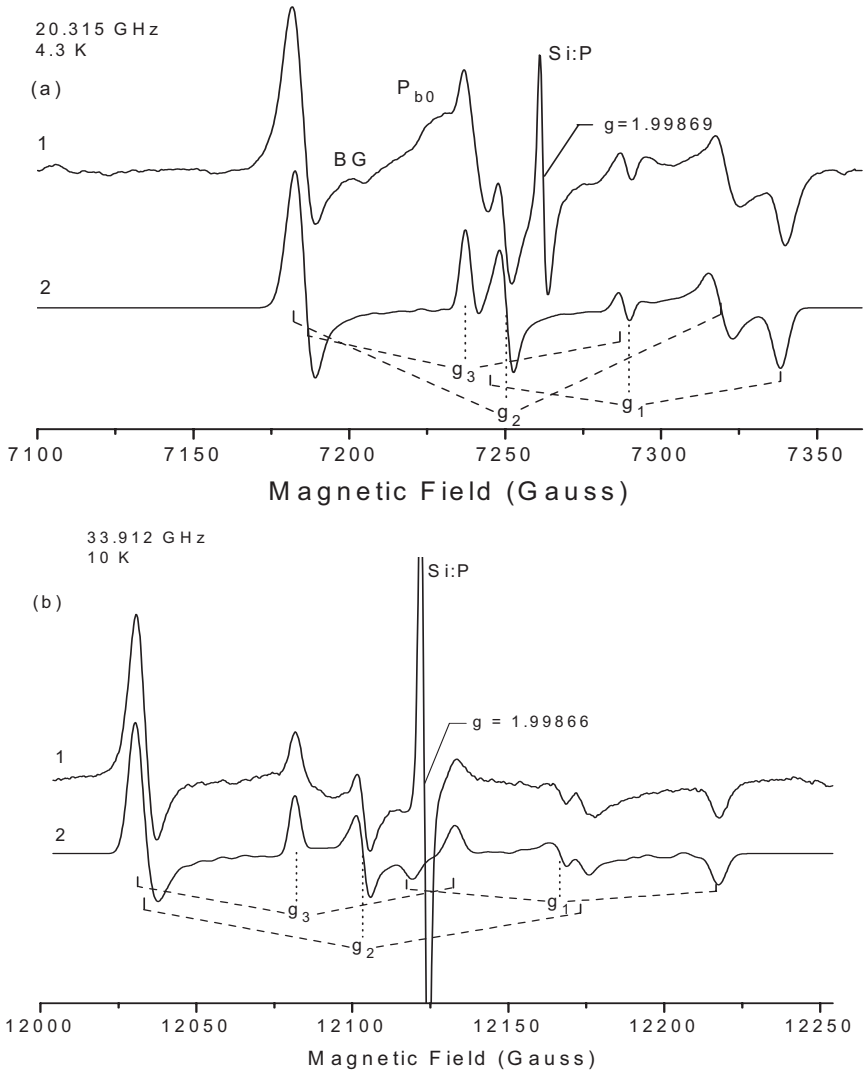


Figure 1 (a): Top curve: K-band ESR spectrum (4.3 K) observed for **B**//**n** on NCVD (100)Si/HfO_2(100 nm). The signal at g=1.99869 stems from a co-mounted marker sample, while the small feature (marked BG) at g~2.015 originates from cavity background. The applied modulation field amplitude was 0.3 G, using P_μ ~0.4 nW. Curve 2: simulation of the observed powder pattern, originating from NO_2 radicals, using, besides the parameters given in table I, an intrinsic Lorentzian broadening function of ΔB_{pp}=3.5 G and interaction with one I=1 nucleus; (b) top curve: Q-band ESR spectrum, using B_m= 0.6 G and P_μ~ 17 μW. Bottom curve: simulation using the same parameters as listed in table I; Only the microwave frequency has been adapted, and a standard distribution of spread σA=5 % in the principal A values was included.

$$H=\mu_B \mathbf{B}.\hat{g}.\mathbf{S} + \mathbf{I}_j.\hat{A}_j.\mathbf{S}, \quad (1)$$

where $\hat{g}$ is the electronic g dyadic and $\hat{A}_j$ the hf tensor for interaction of the unpaired electron with a nucleus of spin I at site j. As demonstrated by the simulated curve 2 in Fig. 1, excellent agreement is attained with the experiment using the parameters listed in table I, a Lorentzian intrinsic broadening function of peak-to-peak width ΔB_{pp}=3.5 G, and interaction with one I=1 nucleus (100 % natural abundance) with $\hat{g}$ and $\hat{A}$ having common symmetry axes. There appears no significant distribution in principal g and A values. As can be seen, all spectral features are well reproduced both in shape, relative magnitude, and width. The inferred parameters g, A, and I are reliably assigned by measurements at a significantly different microwave frequency f, where peaks of different g do shift relatively, while hf splittings remain generally unchanged, resulting in a much altered spectrum. The results of such an experiment at Q band (32.912 GHz) and its simulation are shown in Fig. 1 (b). Again, excellent agreement in spectrum simulation is attained using the same parameters listed in table I; only the microwave frequency has been altered, indicative of a consistent analysis.

In looking for a I=1 nucleus of substantial natural abundance, nitrogen (^{14}N; 99.64 % natural abundant) may be self suggestive as an 'obvious' candidate contaminant for the particular NCVD method applied. A literature search quickly resulted in identification of the spectrum:[26] In table I, the inferred spectral parameters are compared with those of NO_2 molecules,[27-29] stabilized in various matrices, leaving no doubt as to its atomic origin. In particular, the parameter values are close to those of NO_2 centers stabilized (constrained) in rf sputtered SiO_2 films;[27] there is a slight common shift (~0.0004) in principal g values, which could be due to calibration. There are of course small changes as may be expected when embedding the NO_2 centers in different matrices (environments): variations in the molecular configuration (e.g., O-N-O bond angle), reflecting in the unpaired electron sp hybrid, will result in some modification of g and A values.

The spatial location of centers was addressed by repeating K-band experiments after removal of ~50 % (determined capacitively) of the HfO_2 film in aqueous HF. This reduced the NO_2 signal by 55± 10 %, indicating the contaminant centers to reside in the HfO_2 layer, likely uniformly distributed. That is, they neither predominantly reside at the Si/insulator interface nor in a thin SiO_xN_y interlayer grown[30] during sample manufacturing. The latter is supported by the rather high density of defects observed (*vide infra*): it is unlikely that all defects are confined to only one or a few atomic layers.

From the optimized powder pattern simulations, an NO_2 areal density of $(4.7\pm1.5)\times10^{13}$ cm^{-2} is inferred, corresponding to 4.7×10^{18} cm^{-3} if assuming uniform distribution throughout the HfO_2 film (~100 nm thick), i.e., ~55 at.

ppm. However, should the applied γ-irradiation not have exhaustively (ESR) activated all NO_2 precursors present, the likely more correct statement would perhaps be that this value rather constitutes a lower bound.

K-band observations were extended up to a maximum temperature T~35 K, limited by excessive cavity loading due to growing losses in the Si substrate. Through these measurements, P_μ was maintained at ~2.5 nW to avoid extraneous saturation effects. As shown in Fig. 2, for T increasing to ~35 K, the spectrum undergoes little variation, apart from the decreasing signal intensity due to the 1/T Curie law. This would imply that up to this T, the NO_2 entities remain immobilized within the HfO_2 matrix: No substantial rotation of the NO_2 entities occurs, as this would directly reflect into the spectral features of the ESR powder pattern.[29] Rotation, if enabled, would average the g and hf tensor anisotropy to either axial symmetry if the molecules were constrained to rotation about a particular axis, or to full isotropy should the NO_2 entities be enabled to tumble randomly in the matrix. The latter case would imply that the NO_2 molecules reside in voids in the HfO_2 network.

3.3. ELECTRICAL ANALYSIS: CHARGE TRAPPING

The injection-induced V_{fb} shift observed in Au-gated p-type MOS samples and normalized to the specific oxide capacitance as a function of the generated e-h pair density is shown in Fig. 3 for 5-nm-thick HfO_2 layers deposited using different methods. We find that the charge trapping in the thin oxides is strongly sensitive to the method of deposition and PDA. The positive charging of the thin HfO_2 layers deposited using ALCVD and MOCVD clearly differs from the behavior of the NCVD layers, which exhibit net negative charging. Also, the oxidizing PDA of Si/HfO_2 entities shows a clear trend to enhance

Table 1. Parameters for NO_2 radicals stabilized in various matrices inferred from ESR studies (hyperfine A values in gauss).

Matrix	g_1	g_2	g_3	A_1	A_2	A_3
HfO_2 [1]	1.99122	2.00192	2.00555	49.0	68.5	51.0
SiO_2 rf	1.9914	2.0023	2.0059	47.0	66.0	50.0
ice (77K)[3]	1.9920	2.0022	2.0066	49.6	70.2	50.6
$NaNO_2$ [4]	1.9910	2.0015	2.0057	46.8	67.3	49.5

[1]Current results inferred from simulation of the observed powder pattern K and Q-band ESR signals. [2]Ref. 27. [3]Ref. 28. [4]Ref. 29.

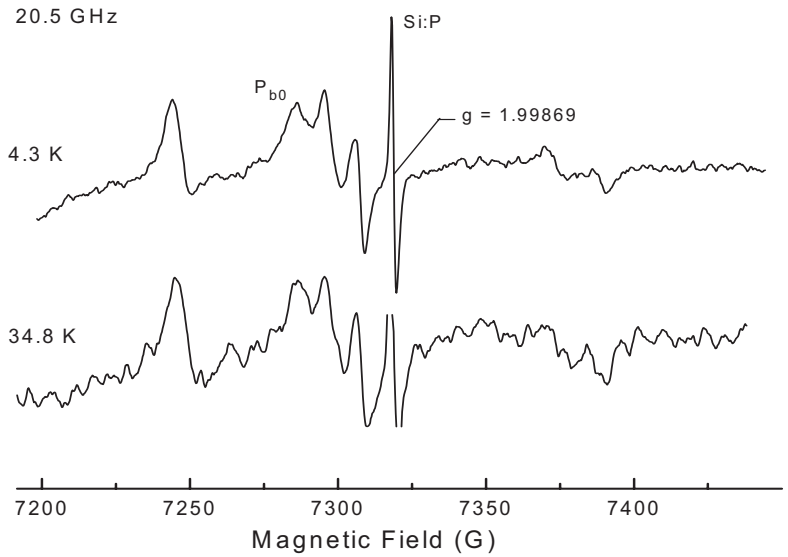
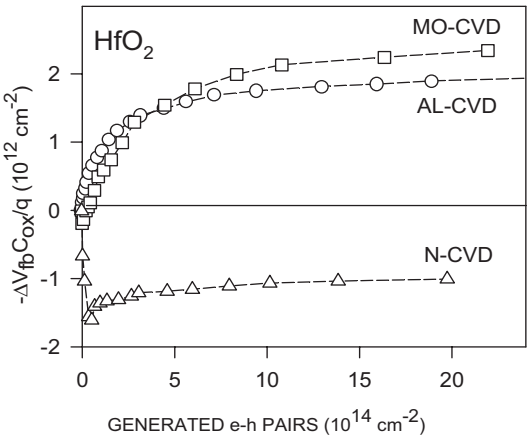


Figure 2. K-band ESR spectra observed for **B**//**n** on NCVD (100)Si/HfO_2(100 nm) for two temperatures; there is no evidence for variation in principle g values, potentially arising from rotations of the NO_2 radicals with increasing T.

positive charging, suggesting an additional contribution of the growing Si oxide interlayer to the hole trapping. As no ESR active centers possibly associated with trapped positive charge could be detected in the as-deposited samples, most of the traps in HfO_2-based insulators are likely diamagnetic. The trapped charge density appears to be nearly insensitive to the thickness of the oxide (data not shown) suggesting location of charges near the Si/insulator interface.

*Figure 3***.** Normalized shift in flatband voltage V_{fb} determined from 100-kHz C-V curves as a function of e-h pair density generated under +1.5 V bias on the Au electrode in p-type MOS capacitors with unannealed 5-nm-thick HfO_2 insulating layers deposited using ALCVD (circles), MOCVD (squares), and NCVD (triangles). Here, q is the elemental charge, and C_{ox} the specific capacitance. Curves guide the eye.



The dissimilar response of NCVD grown HfO_2 on Si to hole injection as compared to ALCVD and MOCVD layers of the same oxide indicates a strong impact of CVD residuals. In the NCVD process, N figures as the only possible contaminant of the oxide and its interlayer with Si, which is manifested by the above-presented ESR results. The N-containing centers are likely incorporated near the interface between Si and NCVD HfO_2 layers as suggested by compositional analysis of the interlayer, indicating it to be close to Si oxynitride.[30] It is then reasonable to propose the presence of N as the reason for the exposed dissimilar NCVD oxide charging behavior (cf. Fig. 3).

3.4. PRECURSOR FOR NO_2 RADICAL

It can be excluded that the detected N atoms are incorporated in the form of NO_2 radicals initially in the as-grown HfO_2, not even in an ESR-*inactive* charge state. The signal is neither observed in the as-grown state nor after substantial VUV illumination, an ionizing radiation that would readily enable appropriate charge transfer. It is also unlikely that the NO_2 radical is part of a metal $M^{\oplus}$ stabilized complex such as, e.g., the [-O-N-O-] $M^{\oplus}$ (=Hf^{+}) hole center,[31] an Hf-stabilized anionic nitrogen bridge: again, if not in the proper ESR-charge state initially, the VUV treatment would be expected to readily alter this. One could also speculate about a H-related precursor, for example the network entity O_2N-H, where one could adduce that irradiation by appropriate energetic particles might readily knock off H^0 to result in the ESR-active NO_2 radical. But also this is considered highly unlikely. First, simply because the particular applied CVD growth method using the nitrato precursor represents a nominally H (and C) free process. Second, VUV excitation is not observed to result in direct NO_2 radical formation through N-H bond breaking.

In pursuit of the correct precursor, we may thus infer that apparently the switching on by ^{60}Co γ-irradiation would indicate atomic displacement to be involved.[27] Following this line, an obvious precursor would appear the a-HfO_2 network entity $N{\equiv}(O{-}HfO_3)_3$, a three-fold coordinated N atom bonded to three a-HfO_2 network O atoms. Embedded in the a-HfO_2 network, the species may energetically reside in a less favorable structural (strained) state. Under impact of γ-rays, the creation of a vacancy at any of the three neighboring O-sites would result in the formation of an NO_2 bridge. But, obviously, the charge state may matter. Should a negatively charged O vacancy be created (O^- removal) to result in a complex composed of an ESR-active $\bullet NO_2$ entity and an adjacent $^{+}HfO_3$ center, the result would comply with experimental observations. However, in case of neutral O removal, the resulting complex would entail the additional, in principle, ESR-active center $O_3{\equiv}Hf\bullet$, i.e., the equivalent for HfO_2

of the well-known E' center (generic entity $\bullet Si{\equiv}O_3$) in SiO_2.[32] Such HfO_2 E' center is not observed by ESR, but, in objectivity, the reason could be purely spectroscopic (e.g., excessive line broadening). Obviously, the current data do not provide suitable discrimination, so we shall refrain from further speculation.

4. Conclusions

Paramagnetic defects have been studied by ESR in (100)Si/HfO_2 entities with ~100-nm thick HfO_2 films grown by three variants of CVD. The predominant centers observed in the as-grown sample state or after VUV irradiation were P_b-type defects (P_{b0}, P_{b1}). The incorporation of N atoms during deposition of thin HfO_2 films on (100)Si via NCVD using the $Hf(NO_3)_4$ precursor has been revealed through observation after ^{60}Co γ-irradiation of NO_2 radicals in the HfO_2 matrix. No such centers could be observed in (100)Si/HfO_2 entities formed by the ALCVD or MOCVD methods. The defect precursor is suggested to be the $N{\equiv}[O\text{-}HfO_3]_3$ network entity, the NO_2 defects being formed through γ-ray induced structural rearrangement.

The electrical analysis of (100)Si/HfO_2 entities showed that the hole trapping is the most efficient oxide charging process in the case of ALCVD and MOCVD, strongly depending on the oxide growth method and the applied PDA. Net negative charging is only observed in NCVD-grown structures. The trapped hole charge is found to be mostly associated with diamagnetic centers located in a thin SiO_2-based interlayer between Si and the Hf oxide. The electron traps, on the other hand, seem to reside in the high-κ oxide and their density is also found to be strongly sensitive to the deposition method and PDA treatment. Nitrogen appears correlated with enhanced electron trapping, that therefore, could be used to diminish the degrading impact of hole trapping.

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MECHANISM OF CHARGE TRAPPING REDUCTION IN SCALED HIGH-k GATE STACKS

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Abstract. Properties of the defects responsible for fast transient electron trapping phenomenon in high-k gate dielectrics were investigated. It was shown that electrons might be reversibly trapped at shallow, delocalized gap states. Ab initio calculations have indicated that Zr substitutional impurities and four-coordinated negatively charged O vacancies can fit the electrical profile of the electron traps. The relationship between trap characteristics and reduction of trapping observed in ultra-thin high-k gate stacks are discussed.

Keywords: High-k, Defects, Electron Trapping

1. Introduction

Transition metal and rare-earth oxides comprise many of the high dielectric constant (high-k) materials currently being investigated for application as gate dielectrics in highly scaled transistors. A common electronic feature of these materials is the presence of d-shell states, which leads to their structural properties being drastically different from those of the conventional SiO_2 gate dielectric[1,2]. One of the high-k dielectric properties with significant implications for their electrical characteristics is a relatively high density of as-grown

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defects, which may function as electron traps and fixed charges. Electron trapping/de-trapping in structural defects may contribute to threshold voltage (V_t) instability[3] and affect evaluation of mobility in transistors with the high-k gate stack[4]. In this work, we discuss electrical characteristics of the defects contributing to fast electron trapping process and possible structural origin of these defects.

2. Electron Trapping

2.1. ELECTRICAL PROPERTIES

The electron trapping at low stress voltages relevant to circuit operation conditions is reversible: by applying voltage of the opposite polarity, V_t can be returned to its initial pre-stress value, *Figure 1*a. The de-trapping kinetics is very similar to the trapping one (compare the slopes of the up and down V_t curves in *Figure 1*b); The V_t value after de-trapping is defined by the de-

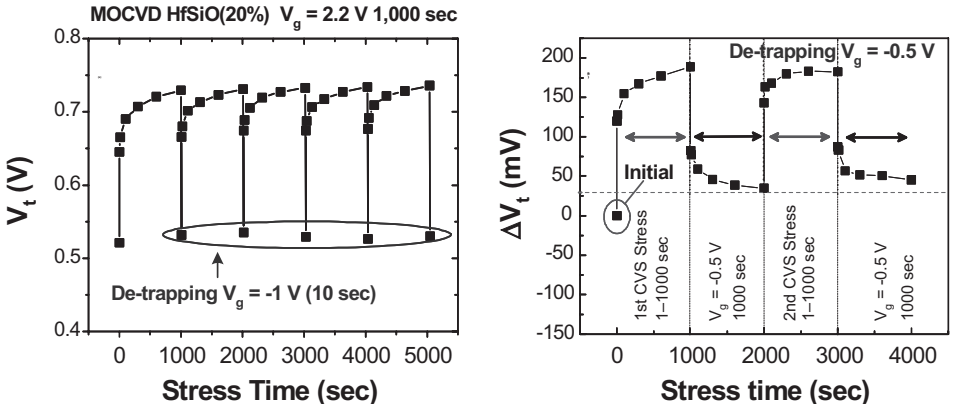


Figure 1. Variation of the HfSiO (20% SiO_2) NMOS transistor V_t during stress cycles, which include 1000 sec substrate injection stress followed by a) 10 sec and b) 1000 sec stress of the opposite bias under the specified voltage conditions. Stress cycle conditions are as labeled.

trapping voltage. The V_t dependence on the stress time does not change with each subsequent stress cycle, and there are no noticeable degradations of the interface electrical properties (transconductance and subthreshold slopes do not change). Therefore, one may conclude that the electron trapping occurs on the pre-existing ("as-grown") defects, and a low voltage electrical stress of practical importance does not generate new traps. This reversible behavior may be expected when the trapped electron resides mostly on the d-orbital, which are

de-localized over the metal ion and its nearest neighbors: in this case, no significant structural relaxation should be expected, and the electron trapping and de-trapping may not lead to structural damage.

One can identify two processes defining the V_t change during stress: initial fast increase of V_t, as can be seen in *Figure 1*a, *Figure 1*b during the first second of the constant voltage stress, followed by a slower V_t growth. To investigate the fast electron trapping, a so-called fast transient charging, a pulse I_d-V_g technique in the microsecond time range was employed[5,6]. An example of these measurements is shown in *Figure 2*a, where the drain current decrease, ΔI_d, is attributed to the effective increase of the device threshold voltage $\Delta V_t = Q/C$ due to the charge, Q, trapped in the dielectric (the trap locations with respect to the electrode define the capacitance C) during the gate voltage pulse: $\Delta I_d = (W/L)C_0\mu\Delta V_t$, where W and L are the transistor width and length, respectively, C_0 is the gate capacitance, and μ is the carrier mobility. This explains why the conventional DC current measurements are lower than the pulse currents (*Figure 2*b): the former's longer time (up to a second) results in significant electron trapping. Measured ΔI_d values can be employed for

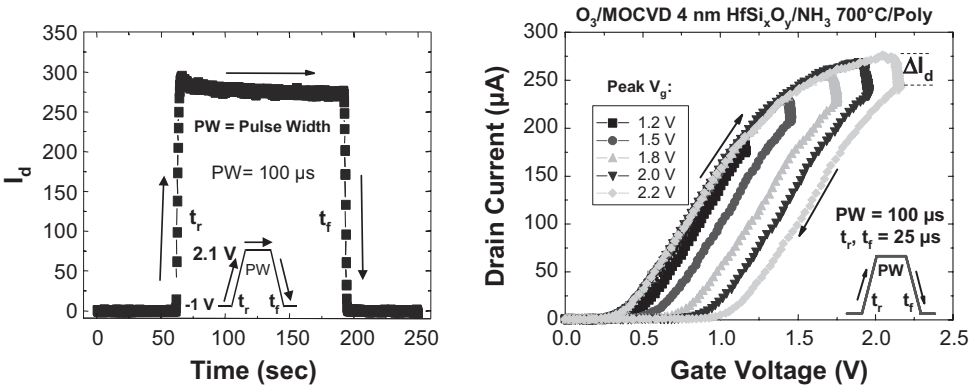


Figure 2. a) Example of the drain current change in devices fabricated using a standard transistor process (with 1000°C/10sec anneal) during the pulse of 100 µsec width. Gate stack processing details are shown in the graph. b) Variation of the drain current with the pulse voltage during the pulse rise, fall, and width times. The drain current was recorded during the gate voltage sweep to the peak value and back to the starting value (negative portion of the curve for the NMOS device is not shown)[5].

calculating the parameter ΔV_t, which can be considered a figure of merit for the fast transient charging effect and, in the case of small trapping, is described as follows[7]:

$$\Delta V_t = (\Delta I_d/I_d)(V_g - V_t) \quad (1)$$

To study fast transient charging we adopt a simplified model where trapping of each electron is independent from others and does not affect the injection current density. Under these conditions, the kinetics of fast transient electron trapping is described by:

$$\partial n/\partial t = 1/\tau(N_0 - n). \quad (2)$$

Here, n is the density of the filled traps, N_0 is the total trap density and τ is the characteristic trapping time, which is inversely proportional to the probability of a single electron trapping event: $1/\tau \equiv p = \sigma J/q$ where σ is the defect capture cross-section, and J is the injection current density. By fitting the solution,

$$n = N_0(1\text{-}e^{-t/\tau}), \quad (3)$$

to the measured time dependence of the drain current during the pulse, ΔI_d (*Figure 2*a), which reflects the time dependence of the electron trapping and accompanying increase of ΔV_t, one can obtain an estimate for the characteristic trapping time (τ) and, subsequently, σ. In the example in *Figure 2*a, $\tau \approx 20\mu s$, and $\sigma \approx 6\cdot$E-13 cm^2 (the effective cross-section value might be overestimated since some effects, like non-linearity of the trap filling process, were ignored.

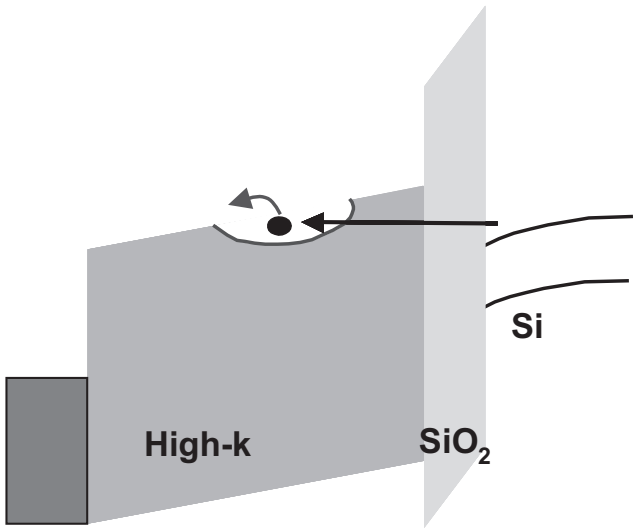


Figure 3. Schematic of the energy band diagram illustrating de-trapping of the electron captured in the direct tunneling process.

In the time scale of the fast charging process, the direct electron tunneling to the traps, which may only weakly depend on temperature, controls, the trapping (*Figure 3*). On the other hand, the electron de-trapping occurs via a temperature activated process $\propto \exp(-E_t/kT)$. From the slope of the temperature dependence of ΔV_t, which was calculated, as described above, based on the pulse measurements data[8], we have estimated the energy of the traps (E_t) to be on the order of 0.20–0.30 eV with respect to the bottom of the conduction band, which is consistent with other reports[9]. Thus, the defects participating in the fast transient charging represent shallow electron traps with extremely large capture cross-section.

2.2. DEFECT STRUCTURE

The atomic structure of the shallow defects still remains unclear and is a subject of intense theoretical studies. Neutral and positively charged oxygen vacancies are unlikely candidates for the shallow traps due to relatively deep energy levels and large relaxation energy[10]. The U-type centers represented by the negatively charge oxygen vacancies were suggested as a candidate for the shallow traps[11], although it is not clear whether this type of defect can exhibit a large effective capture cross-section value extracted from the electrical measurements. Localization of injected electrons in the d-states split off from the conduction band due to the Jahn-Teller effect and distorted at the grain boundaries was considered as a possible mechanism of electron trapping[2].

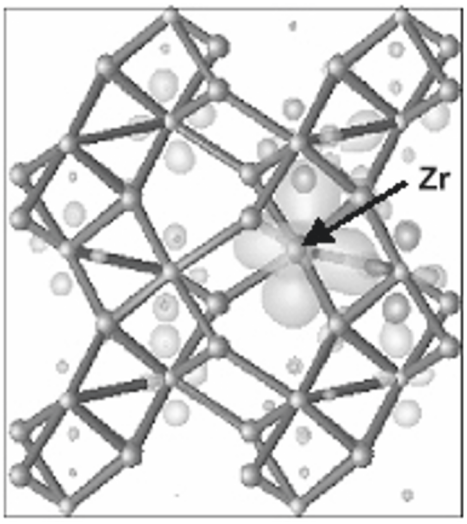


Figure 4. Spin density iso surface of the electron trapped at Zr substitution in the monoclinic HfO_2. The view is along the c-axis. Small 'blobs' around Hf atoms indicate electron density delocalization over the large area. The electron density on the cations has a distinct d-character.

transient charging. Extrinsic defects may be associated with Zr impurities usually present in hafnia within a few atomic percent. The Zr substitution in HfO_2 was calculated using plane wave density functional theory with the spin polarized generalized gradient approximation. The calculations have shown that Zr defects (*Figure 4*) represented shallow traps with the energy of ≤ 0.2 eV, and an electron trapped at this defect was distributed over a large area with a radius

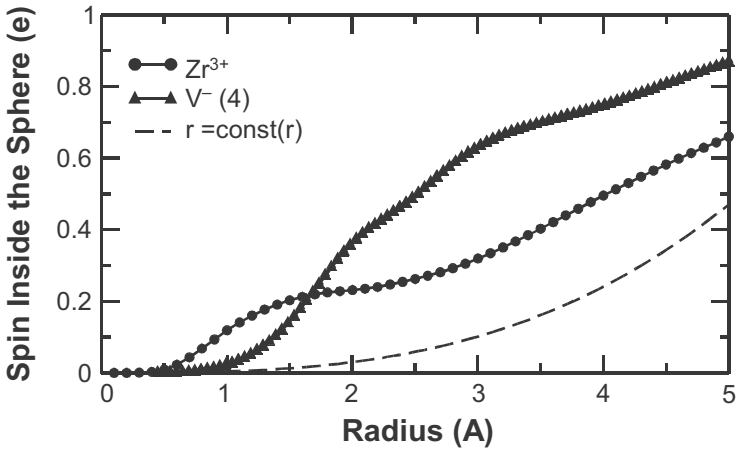


Figure 5. The spin density integrated inside the sphere as a function of its radius R, for the electron captured by the Zr impurity (circles) and four-coordinated O vacancy (triangles) in the monoclinic HfO_2. The integrated uniform spin density corresponding to 1/(supercell volume) is shown for a comparison (dashed line).

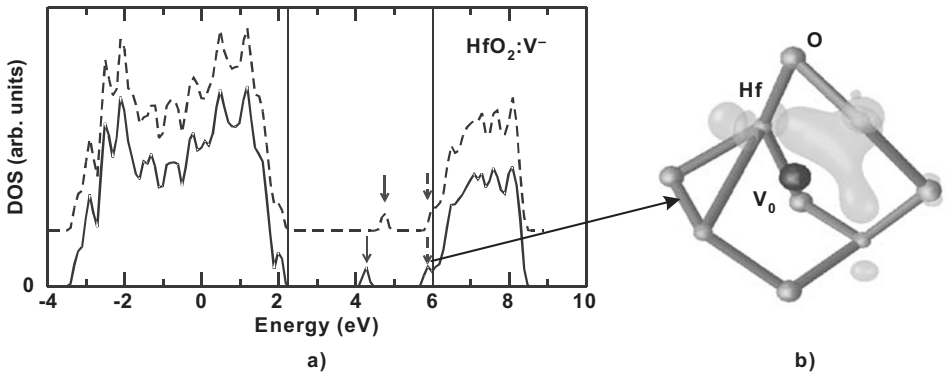


Figure 6. a) Calculated electron density of states for the monoclinic HfO_2 with 4-fold coordinated (solid line) and 3-fold coordinated (dashed line) negatively charged oxygen vacancy (V-). Solid/dashed arrows indicate doubly/singly occupied levels respectively. Thin vertical lines indicate the valence and conduction band edges in a perfect HfO_2. b) Spin density distribution of the electron trapped near the neutral four-coordinated O vacancy (large dark ball).

of more than 0.5 nm (*Figure 5*), which is qualitatively consistent with the above electrical estimates of a very large effective capture cross-section of the traps active in fast transient charging.

Oxygen vacancies in the m-HfO_2 were studied as potential intrinsic electron trapping defects. The electron density of states (DOS) for a vacancy in different charge states is shown in *Figure 6*. Calculations indicate that the positively charged vacancies are most stable in the sublattice of 3-fold coordinated oxygen, while the negatively charged vacancies are more stable in the 4-coordinated oxygen sites. The vacancies in the 4-coordinated sites are characterized by low energy with respect to the conduction band edge, about 0.1 eV, and significant electron delocalization (*Figure 5*) that fits the electron trap profile.

3. Trapping Reduction Mechanisms

Whatever the actual physical structure of the shallow traps is, their critical feature of interest for this study is a very large effective dimension, in excess of 1 nm. The ability of high dielectric film to capture injected electrons is expected to diminish when the film thickness becomes comparable to the effective size of the trap (from the standpoint of localization of the trapped electron). This effect

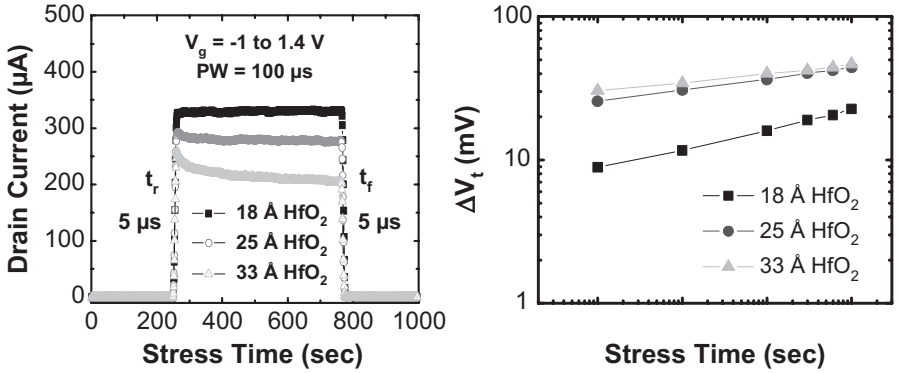


Figure 7. Electron trapping vs. a) pulse time and b) vs. DC constant voltage (V_g =1.8V) stress time in the ALD HfO_2 gate stack (O_3 pre-clean, 1000°C/10sec dopant activation anneal) of different high-k thickness with the TiN electrode.

is clearly seen in the pulse measurement data performed in a set of HfO_2 films of different thicknesses (*Figure 7*). In thinner films, more traps become unable to localize the captured electrons, which may "leak" to the gate electrode

(*Figure 8*). Therefore, aggressive scaling of the gate dielectric physical thickness may provide trap-free device electrical characteristics.

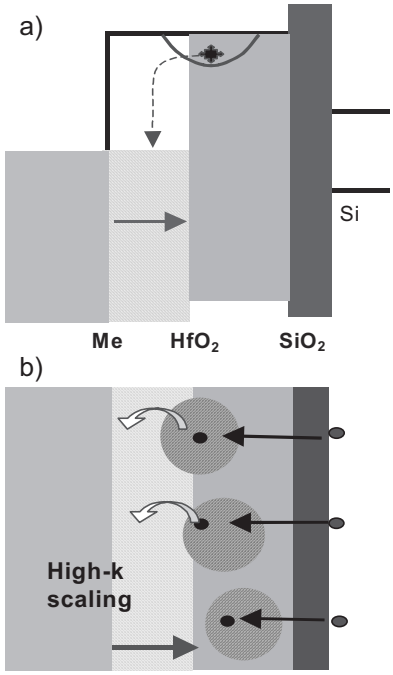


Figure 8. a) Schematic of the band diagram illustrating reduction of the barrier for electron de-trapping out of the shallow trap in HfO_2 due to scaling of the high-k film thickness. b) A corresponding top view of the high-k stack illustrating electron trapping/de-trapping with respect to the trap potion in scaled high-k film.

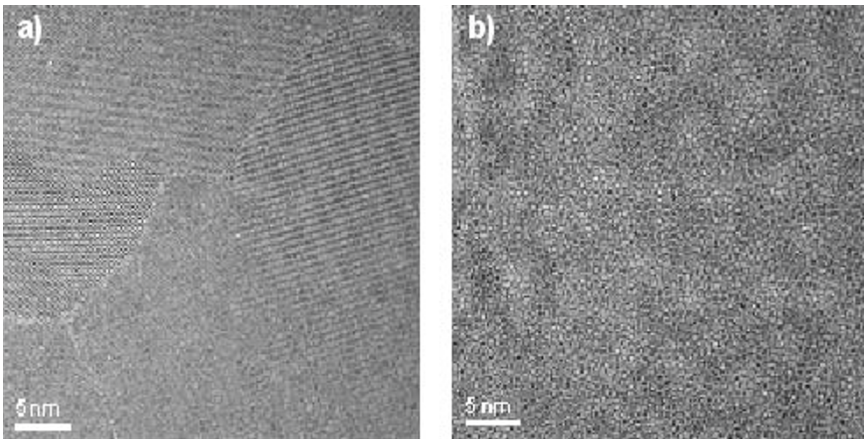


Figure 9. Top view TEM images of the a) 4 nm and b) 2 nm ALD HfO_2 films after 1000°C/10sec anneal[12]. Grain structure is not visible in thinner film.

An alternative explanation may lie with the observation that thinner HfO_2 films exhibit crystallization in a lesser degree accompanied by a correspondingly smaller density of grain boundaries (Figure 9)[12]. If electrically active defects preferentially reside at the grain boundaries, which could be the case with oxygen vacancies, scaling of the high-k film thickness may lead to less electron trapping. However, the temperature dependence of the O-K edge electron energy-loss spectroscopy (EELS) spectra of the ALD HfO_2 film indicates that, in general, the density of the oxygen defects does not scale with the density of the grain boundaries[13], leaving open the question on the relation between grain formation and electron trapping.

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ELECTRICALLY ACTIVE INTERFACE AND BULK SEMICONDUCTOR DEFECTS IN HIGH-K / GERMANIUM STRUCTURES

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Abstract. Metal insulator semiconductor field effect transistors (MOSFETs) with high-k dielectric gates fabricated on high mobility semiconductors such as germanium could be used for future high performance logic devices. In this work, the effects of electrically active defects on the electrical characteristics of Ge metal insulator semiconductor (MIS) capacitors are reviewed. It is shown that at room temperature, generation-recombination processes mediated by semiconductor mid-gap traps are responsible for the generation of minority carriers. Because of the narrow energy gap of Ge and consequently the high intrinsic carrier concentration n_i, the minority carrier density is high so that the inversion layer is built fast in response to high frequency signals at the gate. This gives rise to low frequency behavior in inversion which is characteristic of Ge devices. It is also shown in this work that rare earth oxides form good interfaces with Ge having low interface states density compared to more commonly used HfO_2/GeON gate dielectric stack. This property makes rare earth oxides good candidates for passivating layers of the Ge surface.

Keywords: Germanium MOSFET, rare earth oxides, high-k dielectrics, interface states

1. Introduction

The semiconductor and integrated circuits industry face the challenge to increase the high frequency performance of logic devices keeping at the same time the power consumption low. Strained silicon channels combined with conventional SiO_2 or SiON gate dielectrics offer a good solution for the 45 nm technology node. However, for more aggressive scaling for the 32 and 22 nm

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nodes requiring equivalent thickness (EOT) as low as 5-6 Å it may be necessary to replace SiO_2 by alternative high-k dielectrics in the gate of metal -oxide-semiconductor (MOS) transistors. Although high-k dielectrics have beneficial effects on the gate leakage current, they degrade channel mobility slowing down the speed of devices. High mobility substrates such as germanium can help overcoming mobility degradation and further increase performance. In addition, due to lower bandgap, the Ge transistors can be operated at lower threshold voltage which could reduce power consumption significantly.

The experimental evidence we have so far [1-9] shows that in general high-k dielectrics may be a better match to Ge since they are very good insulators yielding very low EOT values (well below 1 nm), as seen in Fig. 1. In addition, for the case of HfO_2, the dielectric permittivity k is found [9] to be very high, close to the bulk value of 25 and considerably higher than the values of k~15-20 typically obtained when HfO_2 is deposited on Si. These results are encouraging since they show the potential for aggressive oxide scaling.

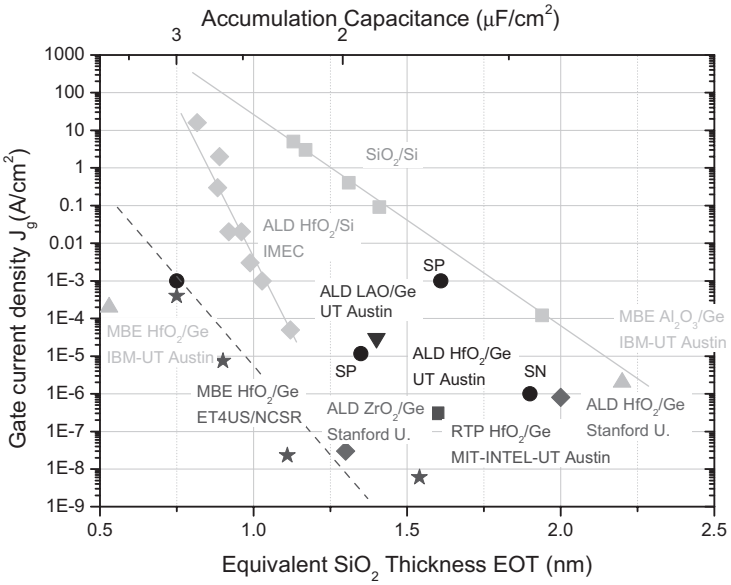


Figure 1. Summary of published results on high-k dielectrics deposited on Ge substrates. HfO_2/Si and SiO_2/Si data are also given for comparison.

Research in Ge is mainly driven by the need to obtain high mobility transistors which will show superior performance over Si-based devices. Since the pioneering work of the Stanford group [10], progress has been made by several groups demonstrating operation of Ge transistors with GeON[11,12], HfO_2[13], Al_2O_3

or $LaAlO_3$ [7] gates. However, all projections based on experimental results show that Ge MOSFETs underperform state-of-the-art Si devices. The biggest problems appear in N-MOSFETs with HfO_2 gates which are barely functional for reasons which are not fully understood at the present time. Part of the problem may be the inefficient activation and diffusion of dopants in Ge which may cause high junction leakage. On the other hand, electrically active defects may also be responsible for poor transistor performance. Bulk semiconductor defects could be generated by metal diffusion[1,2] from the high-k oxide in the underlying Ge. A high density of slow interface carrier traps[2] could also be present as a result of inefficient passivation of Ge surface. For the case of HfO_2, the most common passivating layer is GeON whose quality, however, is considered to be insufficient to ensure fabrication of high performance devices. An intense investigation of alternative passivation methodologies of the Ge surface using Si ultrathin layers [6,7], PH_3 [8] and AlN [8] is underway by several research teams. Among all alternatives, Si passivation has the advantage of being compatible with the standard CMOS processing. However, the formation of a low-k interfacial SiO_2 layer raises concerns about EOT scalability of the gate stack. Because of the difficulties with passivation it becomes increasingly clear that HfO_2 may not be the best match to Ge, so research is re-directed to other high-k candidates which could be deposited directly on a clean Ge surface without interfacial passivating layers. This is an emerging new field of research which requires a deep understanding of surface chemistry on Ge surfaces.

In this article, I will review the possible effects that electrically active defects might have in the inversion capacitance and conductance of Ge MIS capacitors with HfO_2/GeON gates. I will also attempt to elucidate the effects in the electrical behavior of Ge MIS which come from the high intrinsic concentration n_i in Ge. Finally, I will provide evidence that the interfaces of rare earth oxides with Ge have lower density of interface states which make these oxides suitable passivating layers.

2. Thin film preparation methodology and electrical measurements

Amorphous high-k oxides are mainly deposited on semiconductors by atomic layer deposition (ALD) and metal organic chemical vapor deposition (MOCVD). These methods are compatible with semiconductor manufacturing offering very good uniformity and high throughput. Physical vapor deposition methods, including molecular beam epitaxy/deposition (MBE/MBD) offer alternative possibilities. First, the native oxides of Si and Ge surfaces can be removed *in-situ* by thermal desorption under UHV conditions. Second, because there is no need to develop precursor chemistry, a large number of high-k candidates can be screened in a short time. Third, MBD offers a wide

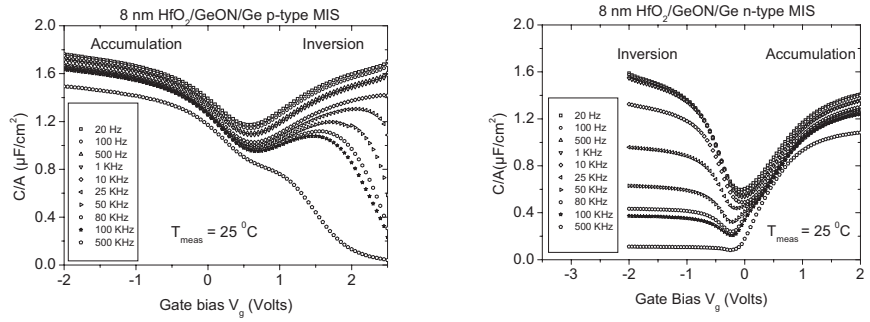
temperature window for growth, including room temperature, which is not easily accessible by CVD-based techniques. Finally, MBE offers the possibility of epitaxial growth of oxides to improve their dielectric properties (i.e., the dielectric permittivity k) and enhance their performance as gate dielectrics. MBE/MBD methodology is described in detail elsewhere [9, 14,15].

The electrically active defects are investigated by admittance spectroscopy, *C-V* and *I-V* measurements using metal-semiconductor-insulator (MIS) capacitors. The top gate contacts are made of Pt and the bottom ohmic contact is made by eutectic In-Ga alloy [15]. All reported thickness values are estimated by X-ray reflectivity.

3. Defect-driven electrical response in HfO_2/GeON/Ge MIS

3.1. FREQUENCY DEPENDENCE-LOW FREQUENCY BEHAVIOR

A common feature [1,2,8,9,15] appearing in Ge MIS devices with high-k gates is a large frequency dispersion in inversion and a low frequency behavior as shown in Fig. 2 below.



(a) (b)

Figure 2. C-V characteristics of HfO2/GeON/Ge MIS capacitors at room temperature measured at different frequencies (a) on p-type and (b) on n-type Ge substrates.

More specifically, the high frequency (>1kHz) capacitance in inversion acquires high values very close to the oxide capacitance C_{ox} as obtained normally in the low frequency (20 Hz) *C-V* curves. The transition frequency f_m which marks the transition from high frequency to low frequency behavior is in the kHz range for Ge [15]. On the other hand, in good quality SiO_2/Si, f_m is very low in the range of a few Hz or a few tens of Hz [18], while low frequency behavior does not appear very often unless the material is defective. In Germanium, inefficient surface passivation or metal diffusion [1,2] from the high-

k dielectric into the semiconductor may introduce electrically active defects which could induce this behavior. It is worth noting, that very similar behavior is obtained also [17] in La-Al-O/GeON/Ge (not shown here) and ZrO_2 MIS [2], indicating that the low-frequency behavior is independent of the specific high-k material used. To obtain a deeper understanding of the microscopic mechanisms involved, a systematic investigation with temperature is performed. The results are discussed in section 3.2 below.

3.2. TEMPERATURE DEPENDENCE

3.2.1. *Temperature dependence of capacitance and conductance*

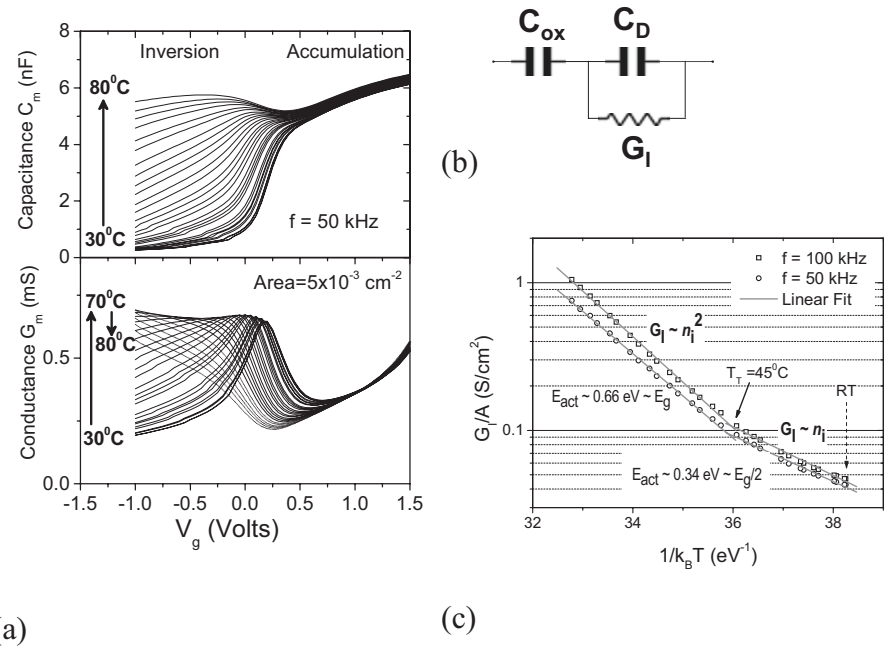


Figure 3. (a) *C-V* and *G-V* at 50 kHz measured at different temperatures in the range between 30 and 80 ^{0}C. (b) Simplified equivalent circuit in inversion. C_{ox} is the oxide capacitance, C_D is the space charge (depletion) capacitance and G_I is the inversion conductance. (c) Ahrrenius plot of G_I. (Courtesy of A. Dimoulas et al, Appl. Phys. Lett. **86** 223507 (2005)) E_g is the Ge energy gap, E_a is the activation energy and n_i is the intrinsic carrier concentration. The vertical dashed arrow marks room temperature. T_T denotes the transition temperature where the activation mechanism changes.

The temperature dependence of *C-V* and *G-V* curves is shown in Fig. 3 (a). The measured capacitance C_m and the conductance G_m show a strong variation in

inversion. Using the simplified equivalent circuit in Fig. 3 (b), the inversion capacitance G_I can be extracted [15,19] as a function of the measured C_m and G_m and then plotted as a function of $1/kT$ in Fig. 3 (c). The inversion conductance G_I shows an activation behavior with activation energies E_{act} equal to $E_g/2$ or E_g depending on whether T is below or above 45 ^{0}C, respectively. Given that the intrinsic carrier concentration varies as $n_i \propto \exp(-E_g / 2kT)$, the results shown in Fig. 3 (c) indicate that G_I is determined by n_i, varying either as n_i or as n_i^2, depending on the temperature of the measurement. G_I regulates the minority transport to the interface with the HfO_2 insulator. At high temperature n_i, and therefore G_I increases so that a high density of minority carriers reaches the interface easily building-up the inversion layer very fast in response to external fields at the gate. This explains, at least qualitatively, why the inversion capacitance at 80 ^{0}C is very high (close to C_{ox}) even at high frequencies (50 kHz).

3.2.2. *Minority carrier response time*

For a quantitative approach the minority carrier response time τ_R, needs to be estimated. This time defined [19] as the *R-C* time constant of the equivalent circuit of Fig. 3 (b), could be expressed as $\tau_R = C_D / G_I$. Using the measured G_I, τ_R is estimated to be in the 0.5-1 μsec range at room temperature, which is more than three orders of magnitude shorter than the corresponding value in the SiO_2/Si system. This is not surprising taking into account that τ_R varies inversely proportional to n_i ($\tau_R \propto 1/G_I \propto 1/n_i$) around room temperature and that, due to lower bandgap, n_i in Ge is more than three orders of magnitude higher compared to Si. The short minority carrier response time in Ge, underlies the low frequency behavior of the high frequency *C-V* observed in Fig.2. It is worth emphasizing here that τ_R is not identical to the minority generation lifetime τ which is much shorter. τ_R depends on τ but as an *R-C* time constant it is longer and it describes how fast the minority carriers move to the interface to form the inversion layer.

3.3. POSSIBLE MECHANISMS FOR THE GENERATION OF MINORITY CARRIERS

In this section we make a critical discussion of the possible mechanisms involved in the generation of minority carriers. Without loosing generality we examine here the case of an n-type Ge MIS which is shown schematically in Fig. 4.

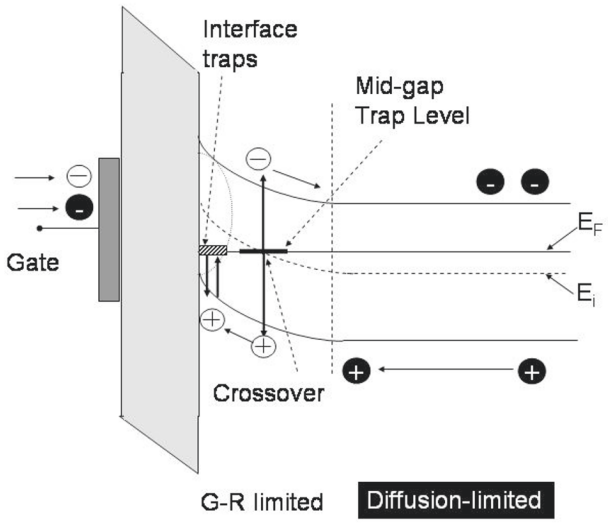


Figure 4. Band diagram of an n-type MIS biased in inversion.

3.3.1. *Generation-recombination of e-h pairs by midgap traps in depletion*

Near surface midgap traps in the depletion layer can mediate the creation of electron-hole (e-h) pairs which provide the necessary population of ninority carriers (holes) to build-up the inversion layer, when a negative bias is applied. This process is very efficient at the crossover point (Fig 4) where the electron and hole emission rates are equal. The inversion capacitance G_I varies proportional to n_i as previously observed in Si/SiO_2 capacitors and subsequently analyzed by Nicollian and Brews[19]. Based on the results in Fig. 3(c), we conclude that in the case of HfO_2/GeON/Ge and in the temperature range between room temperature and 45 ^{0}C, the experimental evidence is consistent with the e-h generation-recombination mechanism mediated by semiconductor midgap traps in depletion.

3.3.2. *Diffusion-limited processes*

In this case, minority carriers are generated in the quasi-neutral area in the bulk of the semiconductor while their response is controlled by diffusion from the quasi-neutral area to the interface. Previous studies[20] in the SiO_2/Si system showed that this processes dominate at higher temperatures where G_I varies as n_i^2. The results presented in Fig. 3 (c) show that for temperatures higher than 45^{0}C, the response of the carriers in HfO_2/GeON/Ge is dominated by

diffusion-limited processes.

3.3.3. *Generation of minority carriers mediated by interface traps*

Interface traps could also mediate e-h pair generation processes. Note however that in strong inversion the interface states which are lined-up with the Fermi level are much closer the valence band (Fig. 4) so that the probability for hole emission is much larger than the probability of electron emission[19]. This means that interface traps exchange carriers mainly with the valence band by emitting and recapturing holes. In such a case, e-h pair generation is not an efficient process. For that reason, the contribution of interface states to the generation of minority carriers and consequently to the low frequency behavior is not expected to be dominant.

3.3.4. *Formation of (permanent) inversion layer beyond (around) the gate.*

A permanent inversion layer formed beyond (around) the gate from fixed oxide charges in the dielectric could easily provide the necessary minority carriers for fast build-up of the inversion charge[19]. In such a case however, low frequency behavior is expected in one type of MIS only, which is in contradiction with the observations (see Fig. 2). This excludes the possibility of permanent inversion layer as possible source of minority carriers.

4. Rare earth oxide gate dielectrics on Germanium

Unlike the case of HfO_2 (and La-Al-O[16]), rare earth oxides do not require an interfacial GeOx or GeON layer. Acceptable MOS behavior can be obtained when rare earth oxides are deposited directly on a clean Ge surface.

4.1. GENERAL ELECTRICAL CHARACTERISTICS

The high frequency C-V and G-V spectra for two rare earth oxides are given in Fig. 5. These spectra have a common characteristic: the conductance peak in depletion and the conductance in accumulation are much lower compared to the values obtained in HfO_2/GeON gate stacks. This is indicative of a low interface state density which is confirmed also by admittance spectroscopy measurements (see section 4.2 below). CeO_2 presents an interesting case because unlike all other candidates, it gives a negligible hysteresis, and a small contribution of the interface states in capacitance associated with small frequency dispersion in depletion.

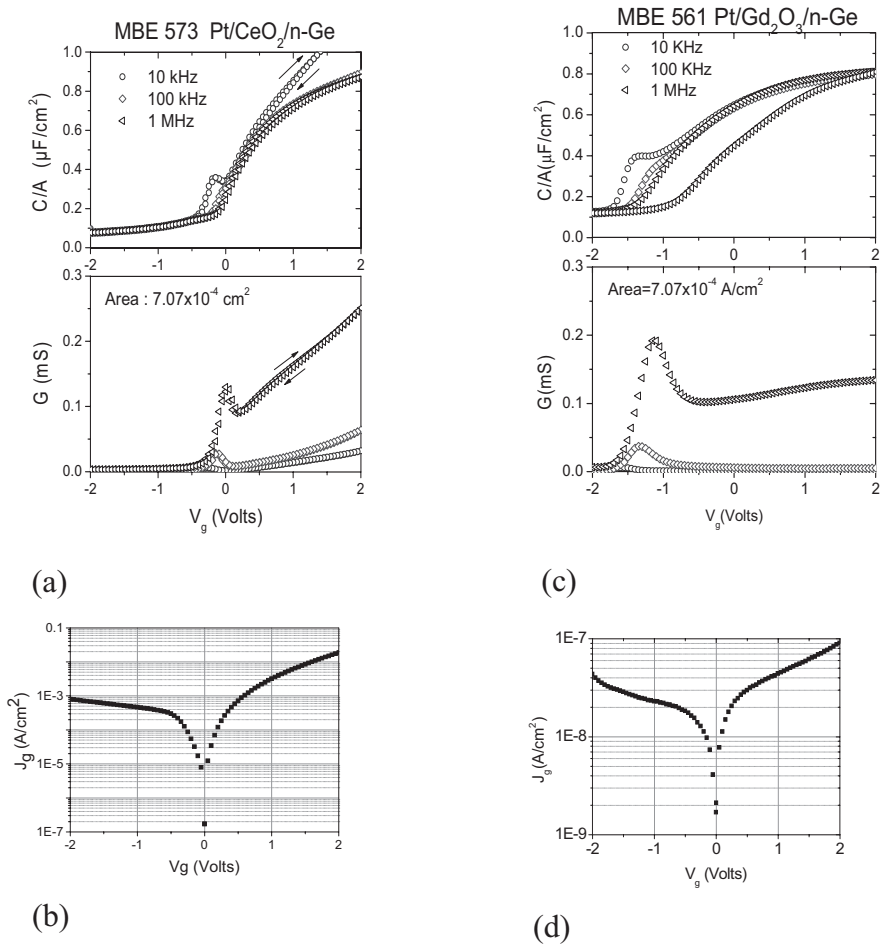


Figure 5. C-V, G-V and I-V characteristics of (a)-(b) 15 nm CeO_2/Ge n-type MIS. (c)-(d) 8 nm Gd_2O_3/Ge n-type MIS.

However, this material is leaky as can be seen from the behavior of capacitance and conductance in accumulation as well as from the *I-V* curves of Fig 5 (b), probably due to its low band gap (~ 3.3 eV) [17]. From the data in Fig. 5(a) an effective dielectric permittivity k_{eff}~ 12-13 is estimated.

On the other hand, Gd_2O_3 is very good insulator (Fig. 5 (d)), which is compatible with the higher bandgap of this material (~ 5.3 eV[17]). However, it shows large hysteresis ~ 500 mV, which is comparable to that obtained in the HfO_2/GeON system. It also shows a large shift of the flat band voltage to

negative values indicating a high density of positive fixed charges in the oxide. From Fig. 5 (c) the effective dielectric permittivity is estimated to be around 9-10. It should be emphasized that similar results were obtained [16] also for Dy_2O_3 (not shown here) indicating that rare earth oxides in general could be a better match to Ge compared to HfO_2/GeON dielectric stack.

4.2. INTERFACE DEFECT DENSITY BY ADMITTANCE SPECTROSCOPY

Admittance spectroscopy is performed on the MIS capacitors with rare earth oxides to determine the the parallel condactance G_p which represents the losses due to the interface states.

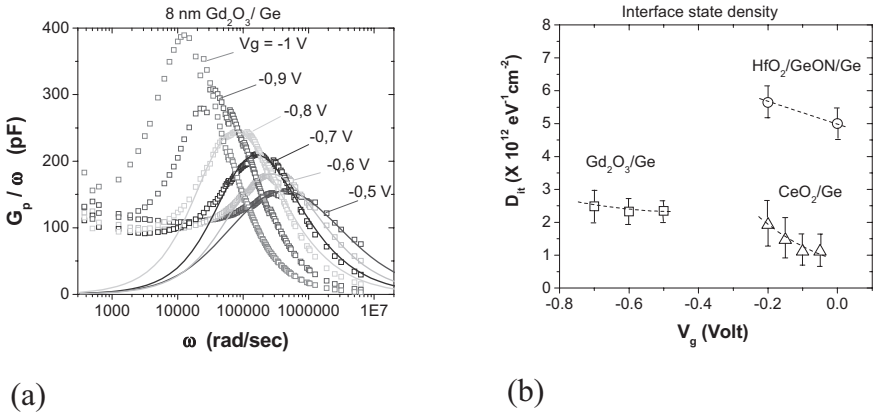


Figure 6. (a) Admittance spectroscopy of a Gd_2O_3/Ge MIS capacitor showing the parallel conductance G_p as a function of the angular frequency ω. The points are experimental data. The continuous line is a fitting curve using the statistical model. (b) The interface state density for Gd_2O_3/Ge, CeO_2/Ge and HfO_2/GeON/Ge systems as extracted from the fitting of the admittance spectroscopy data. Dashed lines are guides to the eye.

Only the spectra corresponding to Gd_2O_3/Ge are shown in Fig. 6(a). By fitting the experimental points using the statistical model, the interface state density D_{it} is extracted and plotted in Fig. 6 (b). The rare earth oxides on Ge give D_{it} values in the low 10^{12} $cm^{-2}eV^{-1}$ range which are reduced by a factor of ~3 compared to HfO_2/GeON. This makes Gd_2O_3 and CeO_2 better candidates than HfO_2/GeON in terms of the quality of interfaces. However, these rare earth oxides exhibit medium- to- low effective k values as already discussed in section 4.1 above, while CeO_2 presents in addition a high gate leakage. This make them unsuitable for agressively scaled devices. Therefore rare earth oxides may be suitable only as thin interfacial-passivating layers to be used in combination with other high-

k oxides such as HfO_2 provided that the two oxides are stable in contact with each other in the same gate dielectric stack and that the good interface properties of rare earth oxides are maintained.

5. Summary

In this work a review is presented of the electrical properties associated with bulk semiconductor or interface defects in several high-k oxides deposited on germanium substrates. HfO_2/GeON gate dielectric stacks on Ge are good insulators with high k values however they suffer from the presence of electrically active defects which produce abnormal effects such as low-frequency behavior in the inversion capacitance of MIS devices. We show that at room temperature, e-h generation-recombination process, assisted by mid-gap impurity states in the semiconductor near the interface is the dominant mechanism for the creation of minority carriers. Based on the electrical characteristics, it turns out that the HfO_2/GeON combination may not be the best match to Ge. In this work, it is shown that rare earth oxides such as CeO_2, Gd_2O_3 and Dy_2O_3 can be deposited directly on Ge with low density of interface states in the low 10^{12} $cm^{-2}eV^{-1}$ range. However, due to their low effective k values (10-13) and the high leakage current (CeO_2) they cannot be used for applications where aggressive oxide scaling is required. They can be used though as thin passivating layers for other oxides (i.e., HfO_2, $LaAlO_3$ etc.) to achieve gate dielectric stacks which combine low interface state density with low leakage and high dielectric permittivity.

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DEFECT AND COMPOSITION ANALYSIS OF AS-DEPOSITED AND NITRIDED (100)SI / SIO_2/ $HF_{1-X}SI_XO_2$ STACKS BY ELECTRON PARAMAGNETIC RESONANCE AND ION BEAM ANALYSIS

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Abstract. The defects in the as-deposited and nitrided $Si/SiO_2/Hf_{1-x}Si_xO_2$ stacks have been analysed by EPR spectroscopy. The interface defects at the Si/SiO_2 section are identical to those in the classical Si/SiO_2 case and their concentration is not influenced by the hafnium silicate layer growth. As-deposited hafnium silicate layers present in addition a defect located in the near surface region with a high concentration; it shows the characteristics of the EX center in SiO_2 including low temperature hydrogen passivation. In the nitrided samples both the interface defects and the EX center are no longer observed. Additional annealing shows this to be related to a hydrogen passivation during the nitridation. The composition of the as deposited $Hf_{1-x}Si_xO_2$ layers have been analysed by ion beam analysis. Their thermal nitridation by NH_3 has been investigated as a function of the annealing conditions. The hafnium silicate layers incoporate N up to some at% in the entire layer whereas hafnium oxide layers show no significant nitrogen incorporate into the bulk of the film.

Keywords: hafnium silicate, Pb centers, EX center, nitridation

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1. Introduction

High-k dielectric materials are an interesting alternative for the replacement of ultrathin nitrided SiO_2 layers currently used as gate oxides in MOS structures. Among the different potential candidates explored such as Al_2O_3, ZrO_2, HfO_2 the alloys $Hf_{1-x}Si_xO_2$ seem to be of particular technological interest. Hafnium oxide-based materials show a number of important properties for silicon electronics. Binary HfO_2 has a dielectric constant of ~ 20-25 (i.e. ~ 5 times larger than that of standard SiO_2 of ~ 3.9) and reasonable wide band gap ~ 5.5 eV and conduction band offset of ~ 1.8 eV. Moreover this material can be integrated with poly-Si technology due to thermal stability with silicon up to 1000°C[1,2]. However, HfO_2 is known to undergo crystallization at relatively low temperature of ~ 500-600°C, depending on film thickness[3]. Electron mobility degradation in gate stacks with HfO_2 due to remote phonon scattering is also a concern for high-performance devices[4,5]. Hafnium silicate materials ($HfSi_xO_y$) have been demonstrated as an option with even higher thermal stability and higher electron mobility[5-7]. One of the issues with $HfSi_xO_y$ pseudo-binary alloys is their moderate dielectric constant of ~ 12-16 (depending on the composition) and phase separation in HfO_2 and SiO_2 regions upon annealing at high-temperatures[8-9]. To overcome this problem, nitrided hafnium oxide and hafnium silicates have been proposed[10]. $HfSi_xO_yN_z$ materials show superior thermal stability, resistance to crystallization (at least up to 1100°C for 60 sec), reduced gate leakage, better scalability to sub-1nm EOT, reduced charge trapping, good electron mobility and reliability[1,10,11].

A limiting factor concerning the utility of such layers in microelectronics is the presence of electrically active defects at the interface with the silicon substrate and in the bulk of the dielectric layer. In the case of ultrathin SiO_2 layers nitridation has been shown to be beneficial for interface defect reduction as well as leading to an enhanced resistance to degradation of the SiO_2 layer. It thus seems interesting to study the effect of nitridation of the hafnium silicate layer. Nitrogen can be incorporated in the hafnium oxide-based materials by means of several techniques. One approach is to have nitrogen incorporated during deposition, for example by sputtering of HfN followed by reoxidation[12]. Another approach is nitrogen incorporation by post-deposition treatment of HfO_2 or $HfSi_xO_y$ layers. Post-deposition incorporation can be achieved either by plasma nitridation methods or thermal nitridation, e.g. in NH_3. One potential issue to be aware with the post-deposition nitridation, especially with ultrathin high-k layers, is to make sure the treatment is not too aggressive and doesn't result in significant interface nitridation since it may cause, in turn, reduced electron mobility. It is the purpose of this work to investigate thermal nitridation of hafnium oxide-based materials in ammonia. Specific questions

we would like to answer are as follows: (i) where nitridation takes place, *viz.* in the bulk of the high-k dielectric or at the surfaces and interfaces; (ii) how nitridation depends on high-k layer thickness and processing parameters, such as temperature, pressure and time; and (iii) relative comparison of HfO_2 *vs.* $HfSi_xO_y$ layers. Further we want to investigate how the defects at the interface and in the dielectric layer are modified by the nitridation. It is our belief that understanding these basic aspects of nitridation mechanism will also help to guide processes for gate stacks with improved device properties.

We present here the results of the study of defects in $Si/SiO_2/HfSiO_2$ stacks and their modification by nitridation with high temperature NH_3 treatments. The stacks were analyzed by (i) ion beam analysis in order to determine the composition of the high- k layers and the nitrogen incorporation by NH_3 treatments as well as by (ii) electron paramagnetic resonance spectroscopy (EPR) to assess the interface and layer defects.

Previous studies[13-16] of (100)Si / high-k stacks prepared by ALCVD and MOCVD have shown that irrespective of the surface preparation of the (100) Si substrate before deposition of the high-k layer abrupt interfaces cannot be obtained due to the apparently unavoidable growth of a thin SiO_x intermediate layer. Therefore Si/SiO_2/high-k stacks with a purposely grown SiO_x layer are generally prepared. The samples studied in this work are of such type with a 1nm thick thermal SiO_2 layer systematically grown before the deposition of the high-k layers. The presence of a controlled SiO_2 layer at the interface with Si has the advantage of disposing of a well known, low defect interface which is essentially very similar to the classical Si/SiO_2 case with thermally grown SiO_2 layer. For $(100)Si/SiO_2$ interfaces two defects, the Pb centers P_{b0} and P_{b1}, are known to be the dominant interface defects with concentrations in the $10^{11}..10^{12}cm^{-2}$ range before hydrogen passivation. Both defects are paramagnetic and their properties and concentrations have been widely studied by EPR spectroscopy. Defects in the amorphous dielectric layer can equally be studied by EPR; nevertheless, no such defects have been observed up to now in as deposited layers. It is only in layers degraded by post deposition high temperature oxidation treatments or carrier injection that paramagnetic defects have been evidenced[14-15].

2. Experimental details

HfO_2 and $HfSi_xO_y$ films used in this work have been deposited on $Si(100)/SiO_2$ by MOCVD using Hf-tert-butoxide (HTB) precursors. Nominal compositions of $x \approx 0.25$ have been targeted. The real compositions obtained by ion beam analysis (IBA) differ slightly from these values (table). High-k film thickness varied in the 4-20 nm range. Before high-k deposition, Si wafers were pre-

cleaned using standard wet chemistry treatment followed by thermal oxidation of an ultrathin (<1.5 nm) SiO_2 interlayer.

Table 1. Si(100)/SiO_2/$HfSiO_2$ stacks used in this study

sample	SiO_2 thickness	High k layer composition	thickness
J49P	1nm	-	-
IQIP	1nm	HfO_2	5nm
IT4P	1nm	$Hf_{.75}Si_{.25}0_2$	3nm
IRRP	1nm	$Hf_{.74}Si_{.26}0_2$	4nm
IQ3P	1nm	$Hf_{.75}Si_{.25}0_2$	9nm
J19P	1nm	$Hf_{.77}Si_{.23}0_2$	17.5nm
J4BP	1nm	$Hf_{.76}Si_{.24}O_2$	4nm

For the $Hf_{0.75}Si_{0.25}O_2$ compositions layers with different thickness (table 1) - 3, 4, 9 and 17.5nm - have been prepared to investigate the influence of the layer thickness on its structural and defect properties. The HfO_2 layer was of 5nm thickness. A Si/SiO_2 reference sample has equally been studied.

The nitridation treatments were performed in an UHV closed furnace. The nitrogen source was >90 % isotopially enriched $^{15}NH_3$ gas. The treatments were performed in the 600°C -800°C temperature range for pressures between 2mbar and 100mbar and a duration of 15 min. In addition, vacuum annealings - 600°C/15 min- and forming gas annealings -600°C/15min were performed on the as–prepared layers. Post deposition vacuum annealings are necessary for the EPR analysis of the layers in order to verify the presence of hydrogen passivated interface or bulk defects. The nuclear reaction analysis (NRA) measurements were performed on the SAFIR installation of the INSP laboratory.The EPR measurements were performed with an X-band (9.4GHz) spectrometer. The X-band frequency range has been proven in the past to be the most suited for interface defect studies on Si as higher frequency K-band (18GHz) and Q-band (35GHz) spectrometers do not offer any increase in spectrum resolution due to the inherent g-factor distribution of the Pb centers and are limited by the smaller sample size which can be accepted. Often microwave saturation problems, leading to distorted lineshapes, are equally encountered at these frequencies.

A typical sample size for the X-band EPR experiments is 4x10mm^2. The measurements were generally done at 4K but the 4K-20K temperature range was explored to search for the eventual presence of centers with long spin lattice relaxation times. As the interface defects are anisotropic centers the angular variation of the spectra for a rotation of the magnetic field has to be measured for a reliable analysis of the EPR spectra. A rotation in the (110) plane is the most aequate choice which allows the decomposition of the total

EPR spectrum in the P_{b0}, P_{b1} components plus additional defects from the amorphous layers. Any defect spectrum related to the amorphous layers will of course be isotropic. If adequate low microwave powers are used, symmetrical lineshapes can easily be obtained for the Pb centers and the decomposition of the total EPR spectrum is straightforward. The parameters obtained are the principal values of the g-tensors, linewidths and the absolute spin concentration. The latter is obtained by comparison with a ruby spin standard sample.

3. Experimental Results and Discussion

In the as deposited state all layers present only the EPR spectrum of the P_{b0},P_{b1} centers. As from the hydrogen rich growth environment a partial passivation of the interface defects as well as a strong passivation of the volume defects can be expected we submitted the samples systematically to a standard 600°C/15min vacuum anneal. Indeed, this depassivation anneal increased the intensity of the Pb center spectra and revealed in addition in two layers a new defect center.

We have studied by EPR four set of different samples: a Si/SiO_2 reference sample, a $Si/SiO_2/HfO_2$ sample with a 5nm thick pure HfO_2 layer, a series of $Si/SiO_2/Hf_{0.75}Si_{0.25}O_2$ samples with different high-k layer thickness (3, 4, 5, 9, 17.5 nm). The thickness of the SiO_2 layer is 1 nm in all cases. We will in the following present the results for the vacuum annealed samples.

A typical EPR spectrum corresponding to the $Si/SiO_2/HfO_2$ sample is shown in fig.1. The spectra are taken at 4K under low (μW) microwave power; the fig.1 shows the spectra for the three high symmetry orientations of the magnetic field B relative to the crystal axes B// [001], [111],[110]. As expected these spectra correspond to the interface defects P_{b0},P_{b1}. The spectra are anisotropic due to the low symmetry - C_{3v} symmetry for P_{b0} and D_{2d} symmetry for P_{b1} - of these centers. Due to the small g-factor anisotropies and the linewidth in the 3 to 5 G range at X-band the EPR spectra of the P_{b0} and P_{b1} center are partially superposed. The decompositions in the respective P_{b0} and P_{b1} components as well as a small reference line, is based on the simulteneous analysis of the complete angular variation. Due to the good signal to noise ratio and the symmetric lineshape of the components at X-band they are straightforward and the results are shown in fig.2, 3. The multiplet structure of the P_{b0} spectrum for B//[111] and B//[110] is related to the (100) orientation of the Si substrate. Let us recall that the P_{b0} center has an axial symmetry with a [111] symmetry axis. Thus, contrary to the case of (111) surfaces, where only P_{b0} centers oriented normal to the interface plane are present, different orientations of the P_{b0} center are possible at the (100)Si/SiO_2 interface and are

indeed observed experimentally. It is believed that the intensity distribution between the P_{b0} centers with different orientations is related to the atomic step distribution at the Si/SiO_2 interface.

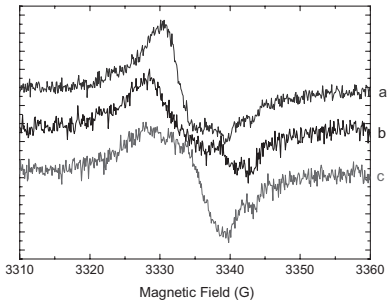


Figure 1. X-band EPR spectra of the $Si/SiO_2/HfO_2$ sample for three orientations of the magnetic field (a)//[100], (b)//[111], (c) //[110].

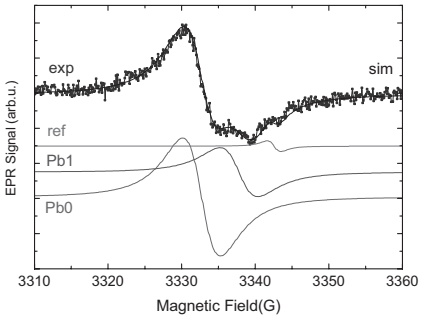


Figure 2. $Si/SiO_2/HfO_2$:Decomposition of the total EPR spectrum (a) B//[100] in the P_{b0}, P_{b1} and reference lines respectively. The sum line of the 3 components is superposed on the experimental spectrum (points).

The modifications of the P_{b0},P_{b1} center parameters (principal values of the g-tensor, linewidth, concentration) as compared to the Si/SiO_2 reference sample or when an additional $HfSiO_2$ layer is deposited, are weak: slight variations in the principal values of the centers are observed but there is no systematic behavior with the composition of the layers HfO_2/ $Hf_{0.75}Si_{0.25}O_2$, or the layer thickness.

The effective g-factors of the P_{b0} and P_{b1} centers in the different sample types are given in fig 4 for the three orientations B//[100],[111],{[110]. For the P_{b0} centers two of these values correspond directly to the principal values of the g-tensor with $g_{//}=2.0020\pm0.0002$ and $g_{\perp}=2.0075\pm0.0002$.

In fig. 5 we have superposed the EPR spectra for B//[001] for four samples. The spectra were taken under identical conditions (temperature, microwave power, field modulation. and gain. As the Pb centers are interface defects, no corrections for the different high-k layer thickness needs to be applied and the signal amplitude –assuming identical linewidth - is thus directly proportional to the respective spin concentration. We observe the highest spin concentration for the Si/SiO_2 reference layer and the lowest for the $Si/SiO_2/Hf_{0.75}Si_{0.25}O_2$ (17.5nm) layer. The relative variations in the spin concentrations are less than a factor of two.

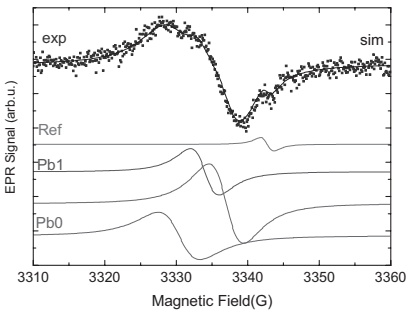


Figure 3. $Si/SiO_2/HfO_2$: Decomposition of the total EPR spectrum (c) B//[110] in the two P_{b0}, one P_{b1} and one reference lines respectively. The sum line of the 3 components is superposed on the experimental spectrum (points).

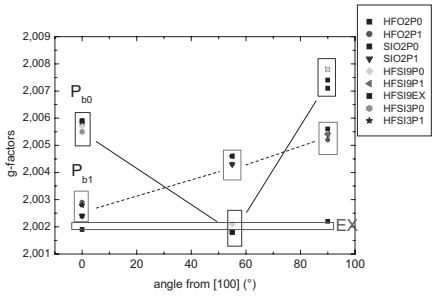


Figure 4. Overview of the effective g-factors observed for the P_{b0}, P_{b1} and EX center lines for the three principal orientations B//[100]-0°, B//[111]-55°, B//[110]-90°.

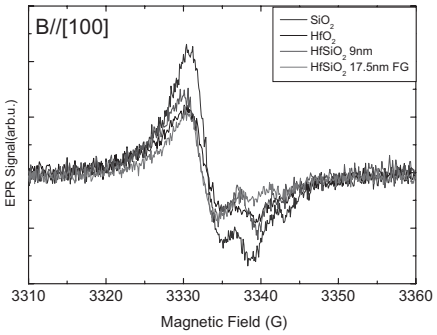


Figure 5. Comparison of the EPR spectra for B//[100] obtained for the different layers cited in table 1.

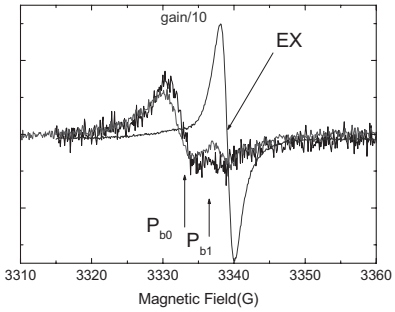


Figure 6. Comparison of the EPR spectra of the vacuum annealed $Hf_{0.75}Si_{0.25}O_2$ layers of 3nm (black), 9nm (red) and 17.5nm (blue)thickness; B//[100]; the gain of the 17.5nm sample has been divided by 10.

The comparison of the vacuum annealed $Si/SiO_2/Hf_{0.75}Si_{0.25}O_2$ layers (fig.6) shows the additional presence of a high concentration isotropic defect in the thickest (9nm,17.5nm) hafnium silicate layers. Its EPR parameters are an isotropic effective g-factor g_{iso}=2.0020 and a peak-to peak first derivative linewidth of ΔBpp=2.5G with a symmetric lineshape of (nearly) Lorentzian form. Such a symmetric lineshape indicates a low intrinsic g-factor anisotropy with $\Delta g<0.0001$. In spite of an excellent signal to noise ratio no related hyperfine spectrum could be detected (fig.7). The concentration of this defect is reduced by a factor of by ~50 passing from a thickness of 17.5 nm to a

thickness of 9nm and is below the detection limit in the 4nm and 3nm thick $Hf_{0.75}Si_{0.25}O_2$ layers (fig.8). In fig 6 the gain of the 17.5 nm layer is divided by a factor of 10! This is a surprising, exceptionally strong nonlinear dependence of the defect concentration with the layer thickness.

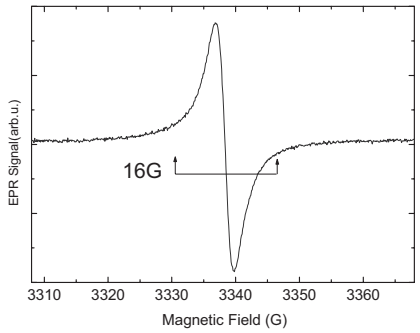


Figure 7. Large scale EPR spectrum of the EX center in $Hf_{0.75}Si_{0.25}O_2$ -17.5nm; no SHF lines are observed at B_{res}±8G.

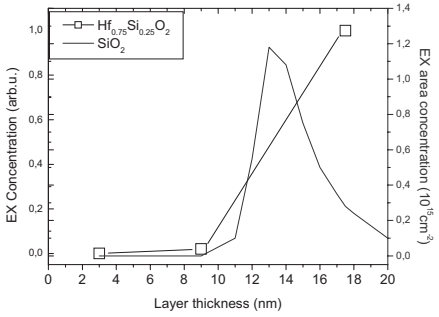


Figure 8. Left scale: EX center concentrations observed in this work(rectangles), right scale (blue line) EX center area concentrations in SiO_2 after ref 16,17.

An analysis of the lineshape at higher resolution shows it to be hyperlorentzian, which is an indication for the importance of exchange narrowing. Exchange interaction is often observed for systems with high local spin densities. We estimate the volume averaged defect concentration to $>10^{18}cm^{-3}$ and thus exchange interaction can be expected to be relevant. The exchange narrowing effect is expected to hide most information on the microscopic structure of this defect such as any hyperfine interaction similar to the case of a-C:H with spin concentrations are in the 10^{19}-$10^{20}cm^{-3}$ range; thus the nonobservation of any hyperfine or SHF line is not surprising inspite of the presence of nuclei with non zero nuclear spin: ^{29}Si,^{77}Hf,^{79}Hf,^{17}O.

A defect with very similar properties, the so-called EX center, has been previously reported in thermally grown a-SiO_2 on Si[16-19]. Its parameters are a g-factor of g_{iso}=2.0024 and a linewidth of $\Delta B_{pp}\approx$1G. In the case of pure SiO_2 a superhyperfine doublet with a splitting of 16.1G and an intensity ratio $I_{SHF}/I_{central}$=0.14 has been observed. It has been attributed to the interaction with 3 equivalent Si atoms. As an oxygen related defect seemed to be a possible model EPR studies on ^{17}O enriched layers have also been attempted[18]. However, the results were not conclusive as no resolved ^{17}O hyperfine interaction was observed. So the microscopic structure of this center is still unsettled. Further characteristic properties of the EX center in SiO_2 are (i) its nonhomogenous distribution in the oxide layer- in fact it is a concentrated in a 3nm deep surface layer- and (ii) its strong nonlinear variation with the oxide thickness (fig.8). Its concentration shows a sharp maximum for a “magic”

oxide thickness of 14nm and decreases rapidly for thinner and thicker oxides[16-17]. This very particular and unexplained concentration dependence on the layer thickness is also observed in our thick hafnium silicate layers. It is equally possible to passivate this center by hydrogen annealings at 450°C and to depassivate the center at 500°C under vacuum. From a correlation between the 4K EPR concentration profile and room temperature C(V) measurements a positive charge state of the EX center has been suggested[19].

Surprisingly, a defect with the same g-factor g=2.0024 and a slightly increased 16.4G SHF doublet structure has recently been reported in ALCVD grown $Si/SiO_2(0.5nm)/ZrO_2(5nm)$, $Si/Al_2O_3(0.5nm)/ZrO_2(5nm)$ and $Si/SiO_x(O.8nm)/HfO_2(5nm)$ stacks after a 800°C post deposition oxidation plus VUV photoexcitation treatments[20]. This center has equally been attributed to the EX center. The observation of the EX center in stacks not containing SiO_2 or only ultrathin SiO_2 layers seem to be at odds with the exceptional layer thickness dependence of this center reported previously. Eventhough the thickness of the ultrathin SiO_2 layers in the as deposited stacks might have been modified by the post deposition oxidation anneals a 14nm thick SiO_2 layer will not be expected to have formed by this treatment. Thus the assignment of the paramagnetic center in these stacks to the EX defect should be taken as tentative. In fact, the identification of a paramagnetic center with a g-factor of ≈2.0023 is never straightforward: its numerical value is not sufficiently selective as many radicals will show this free electron g factor. In such a case the hyperfine structure becomes the main basis for any model. For the case of the Si/SiO_x/high-k stacks the measurement of the 16G SHF structure with a K-band spectrometer is complicated due to the overlapping lines of the E' center (high field SHF line) and P_{b1} center (low field SHF line) respectively. A confirmation by additional experiments at other microwave frequencies seems to be necessary.

In our case of $Hf_{0.75}Si_{0.25}O_2$ the properties of the EX like center observed are in closer agreement with those reported for the EX center in SiO_2 with in particular the strong dependence of the defect concentration on the layer thickness and high concentrations for a "magic" thickness of ≈13nm. The increase in the linewidth as compared to the SiO_2 case is expected in an alloy structure. It will also lead to a larger distribution of the hyperfine interaction constants which will render their observation much more difficult even in the absence of exchange narrowing effects.

A further property of the EX center in SiO_2 is its sensitivity to hydrogen passivation treatments. We have therefore verified the effect of forming gas (5% H_2) annealing on the EX center in the $Si/SiO_2/Hf_{0.75}Si_{0.25}O$ stack (J19P), which showed the strongest EX center signal. And indeed, a forming gas annealing at 400°C/60min at a pressure of p=1at –typical conditions for the

passivation of the EX center in SiO_2- leads to a complete passivation of the EX center. As we will show below, the $HfSiO_2$ layers can be easily nitrided by NH_3 treatments in the 600-800°C range contrary to the case of the HfO_2 layers. It is thus the SiO_2 fraction in the alloys which can be nitrided. To investigate how the nitridation modifies the EX center properties we have annealed the 17.5nm $Hf_{0.75}Si_{0.25}O_2$ stack at a temperature T=800°C, NH_3 pressure of p=100mbar for t=15min. Under these conditions a total amount of [N]= 5at% is incorporated with a surface concentration of [N]=7 at%. After this annealing

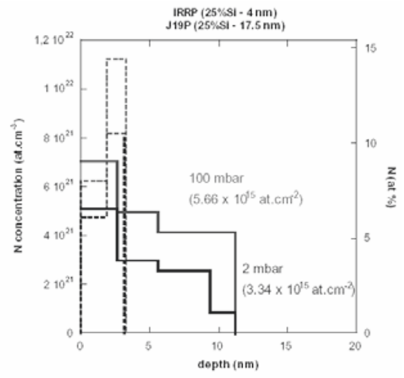


Figure 9. Box profiles of the ^{15}N area concentrations ($10^{15}cm^{-2}$) in the 4nm and 17.5nm $Hf_{0.77}Si_{0.23}O_2$ layers after a 2mbar/100mbar ntridation annealing; 0 is the surface position.

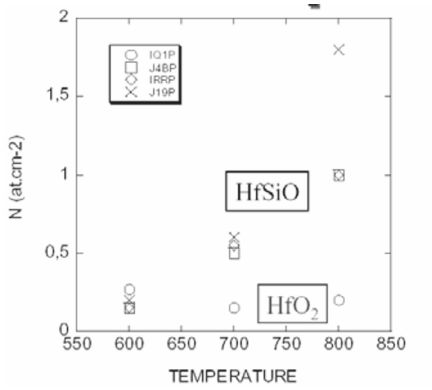


Figure 10. Total ^{15}N area concentration ($10^{15}cm^{-2}$) for 4 different layers (table)as a function of the annealing temperature; p=20mbar, t=15min.

the intensity of the EX center and also of the Pb center spectra were below the detection limit. To verify whether the incorporation of the N has eliminated the center or whether the center has only been passivated by hydrogen formed in the nitridation process we have submitted the nitrided layer to an additional vacuum annealing at 600°C. After this treatment the EX defect density is fully recovered which proves the H passivation character of the NH_3 treatment and that the structure of the EX center is not modified by the nitrogen incorporation.

4. Ion Beam Analysis

The composition of the $HfSiO_2$ layers has been investigated by Rutherford Backscattering, Nuclear Reaction Analysis and ERDA. The ion beam techniques reveal that the overall composition of the 17.5nm thick film with anominal composition of $Hf_{0.75}Si_{0.25}SiO_2$ is close to $Hf_{0.77}Si_{0.23}SiO_2$. The error is estimated to less than 3%. The homogeneity of the Si distribution in the

hafnium silicate layer has been measured by Nuclear Resonance Profiling using the 29Si(p,γ)30P resonance. Our results show that the film is richer in Si near the dielectric/silicon interface than in the surface region.

The nitridation of the hafnium silicate and hafnium oxide layers has been studied by nuclear reaction profiling (NRP). We use the resonance $^{15}N(p,\alpha\gamma)^{13}C$ at Ep=429keV (fig.10) which gives a resolution of 13keV/A. This allowed us

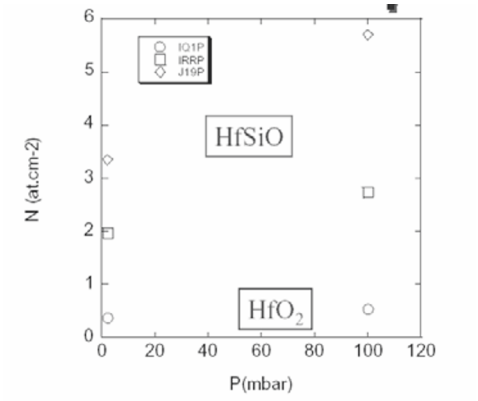


Figure 11. Total ^{15}N area concentration ($10^{15}cm^{-2}$) for 3 different layers as a function of the NH_3 pressure, temperature; T=800°C, t=15min.

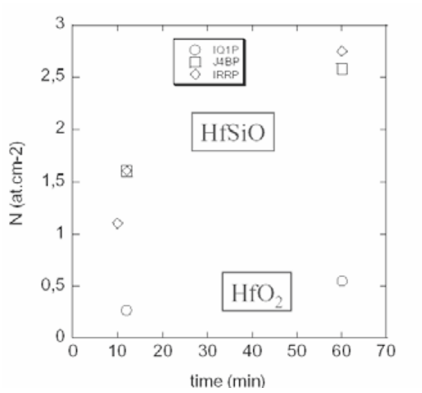


Figure 12. Total ^{15}N area concentration ($10^{15}cm^{-2}$) for 3 different layers as a function of the annealing time; p=20mbar, T=800°C.

to measure the in-depth profile of the ^{15}N incorporation with a resolution of 2nm for the 4nm thick layer and 4nm for the 17.5nm thick layer. The samples used are the same as those used for the EPR studies. Fig.9 shows the ^{15}N profiles for the 4nm and 17.5nm thick layers nitrided at 2mbar and 100mbar $^{15}NH_3$ respectively. The first information we wanted to obtain was whether the nitridation was limited to the surface layer or extended throughout the bulk of the layer. The concentration profiles obtained show in both cases that the nitridation proceeds throughout the bulk of the high-k layers. The absolute scale of the abscisse is slightly incorrect due to the unsufficient knowledge of the density of the alloy layers. Here we have assumed a density of 8 g/cm^3 for $Hf_{0.75}Si_{0.25}O_2$ as compared to a value of 8.75g/cm^3 reported for pure HfO_2.

The thinner layer shows a higher concentration at the interface than at the surface due to the efficient nitridation of the intermediate SiO_2 layer in the stack structure. The temperature dependence of short (15min) low pressure (20mbar) annealings is shown in fig.10 The results show a thermal activation of the N incorporation above 600°C for the HfSiO layers. The pure HfO_2 layer is practically not nitrided even at 800°C. The $HfSiO_2$ layers can apparently be nitrided due to the 25at% SiO_2 fraction which behave similar to pure SiO_2

layers.The pressure and time dependences of the total nitrogen incorporation (in units of 10^{15} at/cm^2) are given in fig.11 and 12. The N profiling of the HfO_2 layers (not shown here) demonstrate that the N is mainly incorporated at the interface and the intermediate 1nm SiO_2 layer.

5. Conclusion

The defects at the interface between the (100) Si and the SiO_2/high-k stacks are identical to the interface defects known frm the interfaces with thermal SiO_2. Their concentration is essentially determined by the growth conditions of the ultrathin intermediate SiO_2 layer and not influenced by the succeeding high-k layer deposition. The $Hf_{1-x}Si_xO_2$ layers present a paramagnetic center which has all the properties of the EX center in SiO_2. Its concentration strongly depends on the layer thickness. It is probably as in SiO_2 a defect located in the surface region of the $HfSiO_2$ layer and shows high concentrations of 10^{18}cm^{-3} for ≈15nm thick layers. The center can be passivated by forming gas treatments and depassivated by vacuum annealing at 600°C. $HfSiO_2$ layers can be nitrided by themal treatments in NH_3 with nitrogen being incorporated in the whole bulk of the layer. The tempertaure, NH_3 pressure and treatment time dependence have been determined and the nitrogen profiles measured by nuclear reaction profiling.

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DEFECTS AT THE HIGH-*K* /SEMICONDUCTOR INTERFACES INVESTIGATED BY SPIN DEPENDENT SPECTROSCOPIES

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Abstract. The interfaces between high-*k* dielectrics, grown by atomic layer deposition, and semiconductors have been characterized using various electrically detected magnetic resonance spectroscopy techniques. The dominant center at the interface was found to be P_{b0}-like. Microwave contactless photoconductive resonance and defect-assisted spin dependent tunneling spectroscopies, performed at low temperatures, reveal also a signal which could be related to E'-like near interfacial oxide traps.

Keywords: Defects, electrically detected electron spin resonance, interfaces, atomic layer deposition

1. Introduction

The scaling down of modern nano-electronic devices, based on a metal-oxide-semiconductor (MOS) structure, has motivated an intense activity on high-*k* dielectrics.[1] Although a large number of materials have been investigated, candidates suitable for the scaling down to the 32 nm node and beyond have not been identified yet. Several parameters must be optimized: dielectric constant (around 30-40), band lineups (CBO > 1 eV) and carrier effective mass in the oxide, thermo-dynamical stability, and interface control. A possible additional

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intrinsic problem could be related to the reduction of the effective electron mobility in the inversion layer of the Si substrate due to remote Coulomb and phonon scattering. This issue motivates the investigation of advanced dielectrics on high-mobility substrates such as Ge, despite the lower junction breakdown voltage and difficulties in the etching steps, and GaAs. Among the most important deposition methods successfully applied we find atomic layer deposition (ALD) and molecular beam epitaxy (MBE).

Defects at the semiconductor/high-*k* interface and in the dielectric layer play a crucial role in determining the device performance. Therefore there is a need to identify the microscopic structure of the electrically active point defects.

Electrical measurements such as capacitance-voltage (C-V), conductance-voltage (G-V), deep level transient spectroscopy (DLTS), noise spectroscopy, and inelastic electron tunneling spectroscopy (IETS) can provide important defect parameters such as activation energies, density, time constants and capture cross-sections, and distance from the interface, but they cannot identify the chemical and structural properties of the defect acting as recombination center. Conventional electron spin resonance spectroscopy (ESR), one of the most powerful spectroscopy techniques for the investigation of point defects in semiconductors and insulators, suffers from sensitivity problems when dealing with state-of-the-art test devices due to their small total area as well as low density of defects, both in the bulk and at the interface. It is therefore necessary to use non conventional magnetic resonance techniques which, exploiting a variety of spin-dependent scattering mechanisms, achieve improved sensitivity. In general these techniques, which have also the intrinsic advantage of the selectivity for electrically active defects, rely on the detection of a certain electrical parameter (photo-current, capacitance, and tunneling current) of the device under investigation in spin resonance conditions. This spin to charge swap improves significantly the sensitivity and can in principle lead to single spin detection.[2,3] We shall refer to these techniques as electrically detected magnetic resonance spectroscopies (EDMR).

Following the first EDMR experiment, performed by Schmidt and Solomon in 1966,[4] by detecting changes at 1.7 K in the intrinsic photoconductivity of P doped Si in ESR conditions, several other reports appeared.[5,6] It was also shown that EDMR techniques are suitable to investigate electrically active defects at the Si/SiO_2 interface.[7-9] Spin dependent transport at the Si/SiO_2 interface in MOSFETs or in short channel in nMOS transistors have been also reported.[10,11] All these applications were based on spin dependent recombination or generation processes affecting the conductivity of the device. One important limitation of this approach is the difficulty in extracting quantitative information (defect density). Attempts to combine EPR and capacitive methods (C-V, DLTS) to obtain a defect spectroscopy which is highly sensitive, quantitative, and provides structural information have been made.[12-14] Several

theoretical schemes have been proposed to explain the observed changes of the conductivity in ESR conditions, and its temperature and microwave frequency dependence. However, due to the lack of systematic experimental data where all possible measurement parameters are considered, several questions remain unanswered.[15]

We report on the investigation of defects at the high-*k*/semiconductor interface as well as attempts to observe defects in the bulk of the high-*k* oxides by applying different EDMR techniques. Three different approaches are considered: in the first case the spin dependent response of the photocurrent is measured between ohmic contacts,[16] in the second the sample is moved out of the center of the resonant cavity, in a position where both electric and magnetic field components of the microwave are present, allowing a contact-less measurement,[17] while in the third the defect-assisted spin dependent tunneling is detected.[18] We will refer to the first technique as dc-photoconductive resonance spectroscopy (DC-PCR), to the second as microwave contact-less photoconductive resonance spectroscopy (MWCL-PCR), and to the third as defect-assisted spin dependent tunneling spectroscopy (DA-SDT). We have investigate several systems, however here we shall discuss, as examples, HfO_2 and Lu_2O_3 films grown by ALD on different semiconductor substrates (Si, SiGe, Ge). The main focus will be on defects at the semiconductor/dielectric interface. However, experimental attempts to identify defects in the thin dielectric layers will be also presented. The influence of the precursor chemistry used for the ALD process has been also addressed. The experimental results are compared with those found at the Si/SiO_2 interface.

2. Experimental methods

2.1 SAMPLE PREPARATION

The high-*k* dielectric films, Lu_2O_3 and HfO_2, have been deposited by ALD on Si, and also for HfO_2, on SiGe and Ge. The Si(100) substrates (Siltronix) were either n-type (P doped, 1-5 Ω cm), or highly resistive (5000 – 15000 Ω cm). RCA cleaning ($HCl:H_2O_2:H_2O$=1:1:5 ratio, 10 min at 85 °C) followed by dipping for 30 s in a diluted HF solution (1:50=$HF:H_2O$) at room temperature was used to prepare the surface which turned out to be H-terminated. The Ge(100) substrates (Umicore) were n-type (Sb doped, 0.073-0.150 Ω cm). They were simply dipped for 30 s in a diluted HF solution at room temperature. This results in a hydrophilic Ge surface. Four types of SiGe layers with different stoichiometry (5%, 20%, 50%, and 80% of Ge) were grown by low-energy plasma enhanced chemical vapour deposition (LEPECVD) (Prof. H. Von Känel, Politecnico di Milano) on highly resistive n-type Si(100) (800-1400 Ω cm). These substrates were cleaned with the same procedure used

for pure Ge. A 30 s long rinse in de-ionized water followed each cleaning step for all substrates.

The HfO_2 films were deposited at 375 °C from the combination of $HfCl_4$ and H_2O,[19] or of $HfCl_4$ and $Hf(O^tBu)_2(mmp)_2$.[20,21] The former precursor combination generated HfO_2 layers at a growth rate of about 0.08 nm/cycle. $Hf(O^tBu)_2(mmp)_2$ acts both as metal and oxygen source promoting a high growth rate (0.16 nm/cycle) when combined to $HfCl_4$. Its organometallic ligand behaves as a basis inducing nucleophilic substitution of the oxygen with the halogen in a halogen-containing complex. Films with nominal thicknesses between 2 and 10 nm were grown on Si and Ge substrates. The HfO_2 films deposited on SiGe from $HfCl_4$ and $Hf(O^tBu)_2(mmp)_2$ had a nominal thickness of 20 nm. The Lu_2O_3 films were deposited from the combination of the newly synthesized complex $[(\eta^5\text{-}C_5H_4SiMe_3)_2LuCl]_2$ [Ref. 22] with H_2O at 360 °C.[23] Lu_2O_3 films having two different nominal thicknesses, 11 nm and 2.5 nm, were deposited on Si and Ge substrates. Lu silicates, 30 nm thick, were deposited from $[(Me_3Si)_2N]_3Lu$ and H_2O.[24]

Two films, respectively 10 and 20 nm thick, were deposited using O_3 as oxygen source: the former is an HfO_2 film grown with $HfCl_4$ as the cation source, the latter is a Si-rich Lu_2O_3, grown using $[(\eta^5\text{-}C_5H_4SiMe_3)_2LuCl]_2$ as Lu source.[25] After the growth, samples 4 x 9 mm^2 in size were cut with the long edge along the $[0\,\bar{1}\,1]$ direction. For DC-PCR aluminum contacts were deposited directly on silicon; details on the experimental procedure can be found elsewhere.[16]

MOS devices for DA-SDT were fabricated by thermal evaporation of aluminum through a shadow mask (150-nm-thick aluminum dots with an area of 1.15 mm^2). Aluminum was also evaporated on the backside as ohmic contact.

All samples have been studied in the as grown conditions, without any post-deposition treatment. Annealing studies are in progress and will be reported elsewhere.

2.2 SPIN DEPENDENT TECHNIQUES

Several spin dependent transport phenomena can be exploited to achieve high sensitivity and selectivity in magnetic resonance detection. We will discuss briefly three different variants pointing out their main features.

In all the different experimental configurations the measurements were carried out in an X band (9.2-9.5 GHz) spectrometer equipped with a rectangular TE_{102} cavity. A frequency counter was used to monitor the microwave frequency. The *g*-factors were determined using the reference signal of α,α'-diphenyl-β-picryl hydrazyl (DPPH) or, when possible, the P signal.

The samples were glued onto a quartz rod or onto a silver rod attached to a cold finger cryostat capable of operating at temperatures in the range 4 K – 300 K.

During the measurements the sample under investigation was illuminated with blue light (470 nm) provided by light emitting diodes. The short wavelength was chosen to generate carriers close to the interface with consequent enhancement of the sensitivity to the surface defects. Spin-dependent changes of the photoconductivity were monitored using phase sensitive detection and magnetic field modulation at low frequency (1-10 kHz) to match the recombination time.[5]

The DC-PCR and MWCL-PCR measurements were performed at room temperature with a microwave power of 180 mW, which corresponds to a microwave H_1 field of ~0.4G,[26] and does not lead to a noticeable line broadening. MWCL-PCR measurements were also performed at T = 10 K with the same microwave power used at room temperature. The DA-SDT measurements were performed only at T = 10 K with a maximum microwave power of about 30 mW.

2.2.1. *Dc-photoconductive resonance (DC-PCR)*

In this experimental set-up changes in the photocurrent between ohmic contacts are detected. An important feature of this technique is the microwave power dependence. It has been reported to exist three regimes depending on the saturation level.[27] In our case, we observed a $P^{0.5}$ dependence, in contrast to the linear dependence in microwave power revealed by MWCL-PCR for similar power levels.

2.2.2. *Microwave contact-less photoconductive resonance (MWCL-PCR)*

An alternative technique, based on the photo-excited free carriers absorption induced losses of the microwave electric field which produce a detectable change in the cavity Q-factor, has been also proposed.[17] In this experiment the sample was displaced from the center of the resonant cavity in order to have both magnetic and electric field components of the microwave field active on the sample. This technique has been shown to be more sensitive than conventional ESR detection and DC-PCR. In addition, in this case, the signal from a linear detector is proportional to the incident microwave power P, and even when the ESR transition is saturated the signal will increase as $P^{0.5}$ due to the electric field component.[17]

2.2.3. *Defect-assisted spin dependent tunneling (DA-SDT)*

In this method, electron spin resonance of the traps was detected by monitoring the modulated gate current in a metal oxide semiconductor (MOS) capacitor placed in the microwave cavity. Spin dependent phenomena in the trap assisted tunneling current through thin dielectrics (thickness less than 3 nm) have been

previously reported in SiN layers on Si.[18] The method is based on the fact that the trap-assisted tunneling current depends on the spin state of the conduction electron and trap. With sufficiently high magnetic fields and at low temperatures the tunneling takes place only when the spin system is in a singlet configuration.[18] This techniques offers two potential advantages, when compared with the DC-PCR and MWCL-PCR. The first is an increased sensitivity to defects in the oxides in addition to those at the interface. The second is the possibility to modify the working condition with the voltage at the gate, V_G, allowing the determination of the defect level distribution, similarly to what has been achieved with gated ESR.[28] In case of half saturation the power dependence of the tunneling current change, in resonance conditions, is given by $\Delta I/I \approx \alpha P/(1+\alpha P)$ where α is a constant proportional to the spin relaxation time.[18]

3. Experimental results and discussion

Several dielectric/semiconductor interfaces have been characterized, as listed in Table I and II. For DC-PCR and MWCL-PCR the spectra were recorded for different orientations of the sample with respect to the *H* field, rotating the sample in the $(0\,\bar{1}\,1)$ plane. All interfaces show a similar behavior. In the following we report the data obtained for Lu_2O_3 on Si and HfO_2 on Si, SiGe, and Ge.

3.1 Lu_2O_3 on Si

Figure 1 shows the MWCL-PCR room temperature spectra observed at the Si/Lu_2O_3 interface. DC-PCR and MWCL-PCR spectra were identical within the experimental error.The overlap between the different signals having a not well-defined line shape, makes the deconvolution rather difficult. The best results were obtained assuming a center with trigonal symmetry, an isotropic center, and using lorentzian lines. The simulations, with the individual components, are reported in Figure 1. Small deviations between experimental data and simulations might be due to a Gaussian contribution to the line shape and to the presence of other less abundant defects possibly characterized by a different symmetry. The number of lines introduced in the simulation was kept as low as possible in order not to over-interpret the experimental data. The principal values of the *g*-matrix determined for the trigonal center are very close to those observed for the P_{b0} center, a silicon dangling bond pointing in the [111] direction towards the oxide at the $Si(001)/SiO_2$ interface.[16,29-33] All different interfaces show the trigonal center with slightly different $g_\perp$ and $g_\parallel$ and line width values, as reported in Tab. I.

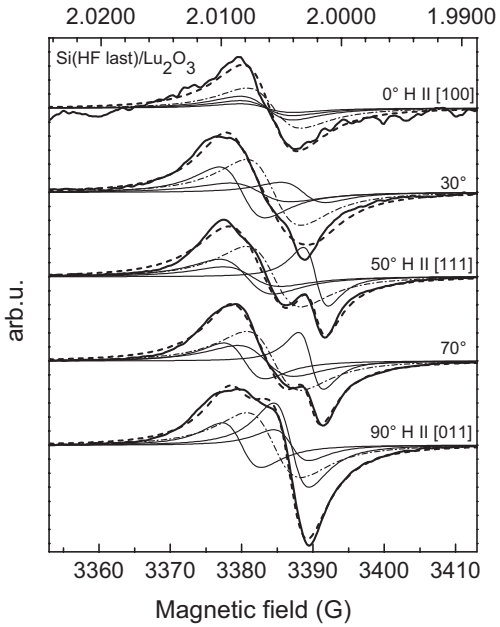


Figure 1. Microwave contact-less photoconductive resonance spectra observed at room temperature for atomic layer deposition (ALD)-grown Si(HF last)/Lu_2O_3 interfaces at different angles between the magnetic field H and the [100] direction of the surface normal. The thick solid lines show the measured data. The thin lines represent the signals of the trigonal center (solid) and the isotropic center (dotted) used to simulate the experimental data. The thick dashed lines are the overall result of the simulation.

To simulate the spectra it was necessary to introduce an isotropic center with $g = 2.0055 \pm 0.0001$ and $\Delta H_{pp} = 9 \pm 2$ G (depending on the interface). This *g*-value is characteristic of Si dangling bonds in disordered or amorphous silicon. The presence of the silicon dangling bong defect at the Si/high-*k* oxide interface has been previously reported,[16,32] and attributed to disorder at the interface and at the sample edges, and to micro-cracks.

The observed dependency of the line width on the angle between the principal axis of the *g*-matrix and the static magnetic field has been previously reported by Pierreux *et al.* and attributed to the strain present at the interface.[34] The dominant trigonal center observed at the Si/high-*k* interface showed line widths larger than those reported for P_{b0} center at the Si(100)/SiO_2 interface.[29] This feature seems to be connected with the relatively low growth temperature of the ALD process.[30] Microwave power effects can be ruled out, as it was experimentally proved that microwave-induced broadening starts above 300 mW.

The Si/SiO_2 character of the Si/high-*k* oxide interface is not a surprise. Sharp high-*k*/silicon interfaces cannot be produced by any deposition methods and an

interfacial oxide or sub-oxide is always present.[35] This observation combined with the fact that P_b-like centers are highly localized unsaturated silicon bonds, almost pure *p*-states,[36,37] explains why the main defect features are P_{b0}-like. The low sensitivity of the silicon dangling bond to probe its surroundings explains the similarity in the observed g-matrix parameters for the different high-k/Si interfaces. Let us consider the case of the lutetium oxide deposition. It has been shown by XPS, X-ray reflectivity, and FT-IR spectroscopy, that $[(Me_3Si)_2N]_3Lu$ combined with H_2O leads to a Lu silicate,[24] while $[(\eta^5\text{-}C_5H_4SiMe_3)_2LuCl]_2$ combined with H_2O generates Lu_2O_3 films.[23] In both cases the DC-PCR and MWCL-PCR room temperature spectra revealed the presence of the trigonal center and of the isotropic resonance. The resonance observed for the silicate/silicon sample is characterized by a larger $g_\perp$ and slightly larger line width (see Table I).

Table 1. Samples investigated by DC-PCR and MWCL-PCR at room temperature and corresponding parameters of the trigonal center used for the simulation. Not listed is the g value of the isotropic signal given in the text.

Interface	Precursors involved in the ALD growth	$g_\perp$	$g_\parallel$	$\Delta H_{pp\perp}$ (G)	$\Delta H_{pp\parallel}$ (G)
Si/SiO_2	Thermal oxidation [Ref. 29]	2.0081(1)	2.0019(1)	2.3(3)	8.1(9)
Si/Al_2O_3 [Ref. 16]	$Al(CH_3)_3 + H_2O$ (a)	2.0074(3)	2.0024(3)	9.3(6)	6.2(5)
Si/ZrO_2 [Ref. 16]	$ZrCl_4 + H_2O$ (a)	2.0084(3)	2.0016(3)	6.0(6)	5.1(3)
Si/Lu_2O_3	$[(\eta^5\text{-}C_5H_4SiMe_3)_2LuCl]_2 + H_2O$	2.0078(2)[(a)]	2.0016(2)	9.0(9)	4.5(8)
		2.0081(2)[(b)]	2.0019(2)	8.5(9)	3.5(9)
	$[(Me_3Si)2N]_3Lu + H_2O$ (a)	2.0090(2)	2.0018(2)	7.5(9)	5.0(8)
Si/HfO_2	$HfCl_4 + H_2O$ (a)	2.0079(2)	2.0028(2)	8.6(8)	5.8(6)
	$HfCl_4 + Hf(O^tBu)_2(mmp)_2$ (a)	2.0085(2)	2.0015(2)	7.6(6)	4.1(4)
	$HfCl_4 + Hf(O^tBu)_2(mmp)_4$ (a)	2.0079(2)	2.0022(2)	7.8(6)	6.2(5)

[(a)] measurement performed with DC-PCR; [(b)] measurement performed with MWCL-PCR.

We now discuss the results obtained by MWCL-PCR and DA-SDT measurements performed at 10 K for Lu_2O_3/Si(001) samples and, as reference, on Si(100)/SiO_2 sample. The spectra, acquired with H ‖ [011], and their simulations are shown in Figure 2. The low temperature MWCL-PCR spectra could be simulated using three lines, while for the DA-SDT two additional lines were necessary. These lines are due to P shallow donors, not present in the MWCL-PCR samples. The resonance parameters are reported in Table II. Both

techniques give similar results, however, DA-SDT allows the surface electrochemical potential manipulation by changing the voltage at the gate, V_G. The MOS was operated in accumulation. Changes in the signal intensities were observed as function of V_G and these results will be reported elsewhere.

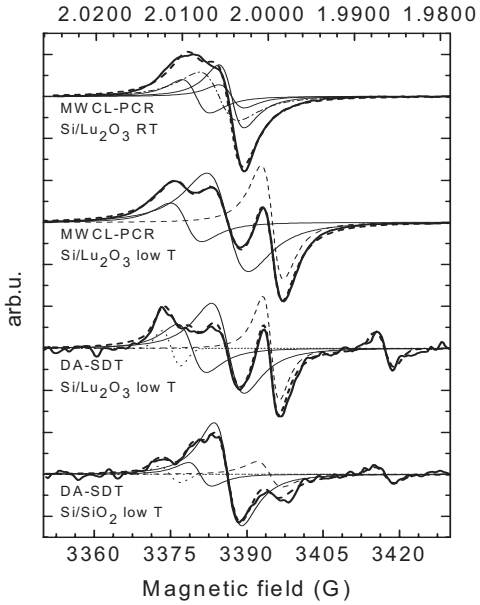


Figure 2. MWCL-PCR and DA-SDT spectra of Si/Lu_2O_3. The thick solid lines are the experimental data, the thick dashed lines is the resulting simulation, the thin solid lines are the P_b center component, the dotted thin line is the P doublet. The dashed thin lines are attributed to oxide traps near the interface. All spectra are recorded for H ‖ [011] at 9.5 GHz.

The lines characterized by g_1 and g_2 are related to the P_{b0}-like center, with $g_1=g_\perp$. A new line, not visible at room temperature, appears at higher fields, corresponding to the smaller g_3. The observed *g*-values are close to the *g*-value of E' signals (g=2.0004(4)) observed for example by Jupina and Lenahan[38] and attributed to near-interfacial or border traps physically part of the oxide, but close enough to the interface to communicate with Si. As a comparison a DA-SDT for a SiO_2/Si(100) (2 nm thermal oxide) is also shown in Figure 2 and the corresponding simulation parameters given in Table II. It can be noticed that the line characterized by g_3 has a higher relative spectral intensity in Lu_2O_3/Si than in SiO_2/Si a result consistent with a more defective SiO_x interfacial layer 3.2 HfO_2 on Si, $Si_{1-x}Ge_x$, and Ge Room temperature DC-PCR measurements on the HfO_2/Si(100) interface does not reveal any surprise. The spectra and their angular dependence could be simulated as

in the previous case (see Table I). It is worth noticing that we observe modest, but reproducible, changes in the P_{b0}-like resonance parameters when O_3 is involved, independently of the high-k dielectric deposited. In that case almost featureless spectra have been observed. From the deconvolution, the intensity of the spectra components due to the dangling bonds pointing towards the oxide seems to increase dramatically. Capacitance-voltage spectroscopy shows an increased density of interface defects when O_3 instead of water is used as oxygen precursor. This observation can be explained by Lucovsky's constraint theory: the higher oxygen coordination of the silicon atom observed in oxides grown with ozone[39] induces a larger semiconductor-oxide mismatch promoting a higher density of defects.[40] Further investigations are in progress to understand the different microstructure of the interfacial layer produced with O_3 based processes.

Room temperature DC-PCR and MWCL-PCR measurements on $HfO_2/Si_{1-x}Ge_x$ ($x \geq 0.5$) did not reveal any signal. However, at low temperature (T = 10 K), signals in the MWCL-PCR spectra could be observed, as shown in Figure 3.

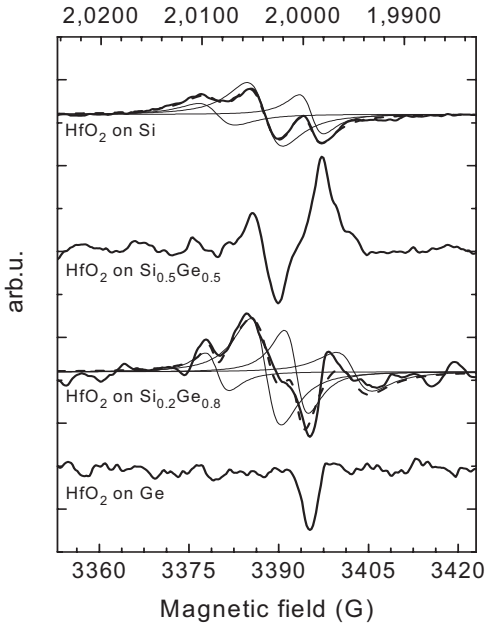


Figure 3. Low temperature (10 K) MWCL-PCR of HfO_2 on Si, SiGe and Ge. The thick solid lines are the experimental data, the thick dashed lines are the resulting simulation, and the thin solid lines are the deconvolution components.

The simulation of these spectra is, in some cases, difficult and more work is necessary to understand the experimental data. Only the spectrum detected for $HfO_2/Si_{0.2}Ge_{0.8}$ could be reasonably simulated with 4 lorentzian lines with parameters given in table II. The observed g values are consistent (g_1 and g_2) with Si - P_{b0} – like centers, the line characterized by g_3 could be related to E'-like centers, while the origin of the line at $g=g_4$ is still unclear. The interpretation is very preliminary and work is in progress to clarify the origin of this line as well as of the signal observed for HfO_2 grown on Ge. In the latter case the resonance, revealing itself as an absorption peak, is definitely related to the interface as etched Ge did not reveal any signal.

Table 2. Samples investigated at low temperature (10 K) using MWCL-PCR or DA-SDT and parameters used to simulate the corresponding spectra.

Interface	Precursors involved in the ALD growth	Experimental Technique	g_1 (a) g_2 (b) g_3 (c) g_4 (d)	ΔH_{pp1} [G] ΔH_{pp2} [G] ΔH_{pp3} [G] ΔH_{pp4} [G]
Si/SiO_2	Thermal Oxide	DA-SDT	2.0076(2) 2.0044(2) 1.9995(2) 1.9986(2) (a)	4.5(5) 5.4(1) 4.7(3) 4.0(2)
Si/Lu_2O_3	$[(\eta^5C_5H_4SiMe_3)_2LuCl]_2$ + H_2O	DA-SDT	2.0086(2) 2.0044(2) 1.9993(2) 1.9985(2) (a)	5.4(3) 6.3(2) 3.15(1) 3.5(1)
Si/Lu_2O_3		MWCL-PCR	2.0092(2) 2.0044(2) 1.9992(2)	5.9(1) 8.0(1) 4.2(1)
Si/HfO_2		MWCL-PCR	2.0089(2) 2.0041(2) 1.9995(2)	5.9(2) 5.7(8) 3.9(1)
$Si_{0.5}Ge_{0.5}/HfO_2$		MWCL-PCR	-	-
$Si_{0.2}Ge_{0.8}/HfO_2$	$HfCl_4$ + $Hf(O^tBu)_2(mmp)_2$	MWCL-PCR	2.0082(2) 2.0035(2) 2.0004(2) 1.9947(2)	4.0(1) 5.1(3) 4.0(3) 5.9(5)
Ge/HfO_2		MWCL-PCR	≈1.9992	-

(a) Phosphorous doublet.

4. Conclusions and outlook

Electrically detected magnetic resonance spectroscopy techniques have been successfully used to investigate the high-k/semiconductor interfaces. Using different EDMR variants it is possible to efficiently detect interface, P_b-like, and near interface, E'-like, defects. Due to the strong localization of the defect wave-function and the presence of an oxide or sub-oxide interfacial layer the observed resonance parameters depend weakly on the high-k material, even in the case of defect-assisted spin dependent tunneling which, in principle, should efficiently detect trapping centers in the oxide, indicating that the dominant defects are located in a region at the interface or within 3 nm from it.

The interfaces between HfO_2 and SiGe have been also investigated revealing, only at low temperatures, MWCL-PCR signals closely related to Si-P_{b0} and E' like centers. A MWCL-PCR signal has been observed also for HfO2 on Ge, however more work is necessary to identify its origin. The interface between high-*k* dielectrics and high-mobility semiconductors such as Ge and GaAs is currently under investigation.

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FIXED OXIDE CHARGE IN Ru-BASED CHEMICAL VAPOUR DEPOSITED HIGH-κ GATE STACKS

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Abstract. We have analysed capacitance – voltage curves of metal-oxide-semiconductor structures containing Al_2O_3, HfO_2, $HfSiO_x$ and Gd_2O_3 dielectric films prepared by metal-organic chemical vapour deposition (MOCVD). The Ru gate electrode was grown by MOCVD. The structures with MOCVD grown Ru electrode exhibited fixed charge density of about 10^{12} cm^{-2}. The structures were submitted to post – deposition annealing in oxygen, forming gas (90% N_2 + 10% H_2) ambient. Post-deposition treatment significantly reduced fixed oxide charges in studied metal-oxide-semiconductor structures.

Keywords: High-κ, MOCVD, oxide charges, Ru gate.

1. Introduction

Defect oxide charges and their minimization are of great importance for correct performance of metal-oxide-semiconductor field effect transistor, MOSFET. Oxide charges are sources of possible MOSFET instabilities. Shift in a flat band voltage due to fixed charge results in unacceptable transistor threshold voltage. Charges in dielectric film scatter carriers in the field effect transistor channel, thereby reducing their mobility. Oxide charges density as

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low as ~ 10^{10} cm^{-2}, commonly achieved in current SiO_2 based CMOS technology, are necessary for proper MOSFET operation.

Fixed oxide charge in metal-oxide-semiconductor (MOS) structures arises from defects in dielectric film, located near the dielectric/semiconductor interface. Magnitude of the charges depends on oxidation process and post-annealing. Origin of fixed charges in SiO_2 based MOS structures is either in excess of silicon (occurrence of trivalent silicon) or due to loss of an electron from excess oxygen centers. Generally, oxide charge in SiO_2 dielectric is supposed to be located within 3 nm from the SiO_2/Si interface and has positive sign.[1]

High-κ dielectric derived MOS structures suffer from significant fixed charges, often exceeding values 10^{12} cm^{-2}. Origin of the fixed charges in high-κ gate stacks is not yet fully understood. Magnitude and sign of fixed charges are closely related to deposition process of the dielectric film and are caused by local non–stoichiometry or structural defects. Internal interfaces within the high-κ dielectric film are additional source of defect charges. In addition to the charges in dielectric film, damage associated with the gate electrode deposition can substantially increase charges in MOS structure. This effect gains more importance with decreasing thickness of dielectric film to few nm. In MOS structures with ultra thin dielectric film, defects related to the interface between the gate dielectric and gate electrode introduces additional charges.

Appropriate post-deposition annealing can significantly alter oxide charges in the MOS structure. It was observed, that annealing in hydrogen environment at temperatures above 400 °C introduces positive charges at the SiO_2/Si interface.[2] The authors assumed, that hydrogen protons cause fixed charge because a proton can form a dative bond with a bridging oxygen site.[3] The situation is far less clear in MOS structures with high-κ dielectric film.[4] Even low deposition temperature processes like atomic layer deposition or metal organic chemical vapour deposition, commonly employed for high-κ dielectric film, introduce defect charges into deposited films. Despite this, only few studies on post-deposition treatment effect on oxide charges in high-κ dielectric based MOS structures are available in the current literature. [5, 6]

In our contribution we focus on fixed oxide charge behaviour in advanced MOS structures with high-κ dielectric films and Ru gate electrodes. We review and summarize experimental data obtained from capacitance – voltage measurements performed on gate stacks containing atomic-layer chemical vapour deposited (ALCVD) Al_2O_3, HfO_2, and metal organic chemical vapour deposition (MOCVD) grown $HfSiO_x$ and Gd_2O_3 dielectric films. It is shown, that the structures contain large amount of fixed oxide charges. Post-deposition annealing of MOCVD grown MOS structures in hydrogen containing ambient is carried out to decrease oxide charges. To assess the effect of post-deposition

treatment in hydrogen, comparison is made with samples annealed in pure nitrogen.

2. Oxide charge determination

The value of fixed oxide charge can be determined from the high-frequency capacitance – voltage characteristics using set of MOS structures with varying dielectric film thickness. Flat band voltage shift V_{FB} in a real MOS structure is a sum of voltages coming from the difference between work function of metal and semiconductor substrate, Φ_{MS}, and from the fixed charge in oxide film:

$$qV_{FB} = \Phi_{MS} \pm \frac{qN_{ox}}{\kappa_{ox}} t_{ox} \tag{1}$$

where N_{ox} is a density of fixed charge in oxide film, q is the absolute charge of an electron, κ_{ox} is dielectric constant and t_{ox} is thickness of the oxide film. It can be assumed that the fixed charge density in the dielectric, N_{ox}, is located near the dielectric-Si interface and does not vary with the dielectric thickness. Then, the fixed charge density is determined from the slope of the V_{FB} versus equivalent oxide thickness (*EOT*) dependence. The *EOT* is defined as the equivalent thickness of SiO_2 required to obtain the same capacitance as with the high-κ dielectric:

$$EOT = \frac{\kappa_{SiO_2} \cdot t_{ox}}{\kappa_{ox}} \tag{2}$$

Unfortunately, in some cases such extrapolation results in non-reasonable values of the gate electrode work function, presumably due to oxide charge distribution throughout the oxide film thickness. To estimate the oxide charge in this case, it is possible to fix the gate electrode work function and calculate density of oxide charge from the Eq. (1), assuming that the flat band shift is given only by the oxide charge. More complex analysis of charge distribution in gate stack, taking into account charges at internal interfaces, was given by R. Jha et al.[7]

3. Experimental

Al_2O_3 and HfO_2 dielectric films were prepared by ASM International using atomic-layer chemical vapour deposition.[8] The $Hf_xSi_{1-x}O_y$ layers were grown by MOCVD derived technique - AVD® (Atomic Vapor Deposition®) in an

AIXTRON Tricent® system.[9] The AVD technique allows growing the $Hf_xSi_{1-x}O_y$ films with various Hf/Si ratios. Typical process conditions included deposition temperatures of 550 °C and pressures of 10 mbar. The $Hf_xSi_{1-x}O_y$ films with the composition Hf/Si = 75/25 have been analysed in this study.

Gd_2O_3 films were prepared by MOCVD in a low-pressure hot-wall quartz MOCVD reactor using Gd $(TMHD)_3$ precursor.[10] The layers were deposited on the HF etched (100) silicon substrate at 500 °C.

Ru films were deposited by AIXTRON TriJet™ liquid precursor delivery technology at 350 °C. Ru $(thd)_2(cod)$ dissolved in n-octane was used as a precursor. Gate electrodes for capacitance-voltage (*C-V*) measurement were patterned by standard optical lithography followed by dry (Ar ion beam) etching. After the electrode deposition and patterning the MOS structures were submitted to forming gas annealing (FGA, 90% N_2 + 10% H_2) during 30 min.

Capacitance – voltage (*C-V*) measurements were performed using an HP 4248A LCR-meter at frequencies between 100 kHz and 1 MHz. Correction to series resistance was employed to extract capacitance and conductance from the measurements. Measurement at frequency 500 kHz was chosen for evaluation of the MOS properties. The interface traps density (D_{it}) was determined from the conductance measurement following Hill and Coleman technique.[11]

4. Results and discussion

In this part we will summarize our results on MOS structures with Ru gate electrode. The Ru gate electrode has work function close to 5.1 eV and is considered as promising candidate for pMOSFET applications.[12] Figure 1 shows determination of the oxide charge density for MOS structures with SiO_2, Al_2O_3, and HfO_2 dielectrics and Ru gate electrode. While the density of oxide charge in the SiO_2 dielectric is well below 10^{11} cm^{-2}, oxide charge density in Al_2O_3 and HfO_2 is above 10^{11} cm^{-2}. In several cases we obtained oxide charge density in Ru/ HfO_2/Si structures above 10^{12} cm^{-2}. Corresponding Ru work function determined from the extrapolation is 5.1 eV for SiO_2, 5.0 eV for Al_2O_3 and 5.3 eV for HfO_2 dielectrics.[12]

The oxide charge density determination in MOS structure with Gd_2O_3 dielectric and Ru gate electrode yields value above 10^{12} cm^{-2}, Figure 2. Similarly, oxide charge density in Ru/$HfSiO_x$/Si structures is close to 10^{12} cm^{-2}. Post-deposition annealing of the Ru/ Gd_2O_3/Si and Ru/$HfSiO_x$/Si structures in forming gas (FGA) at 430 °C decreases interface traps density D_{it}, leading to values below 10^{11} eV^{-1} cm^{-2}. Oxide charge density is not affected by forming gas annealing at 430 °C.

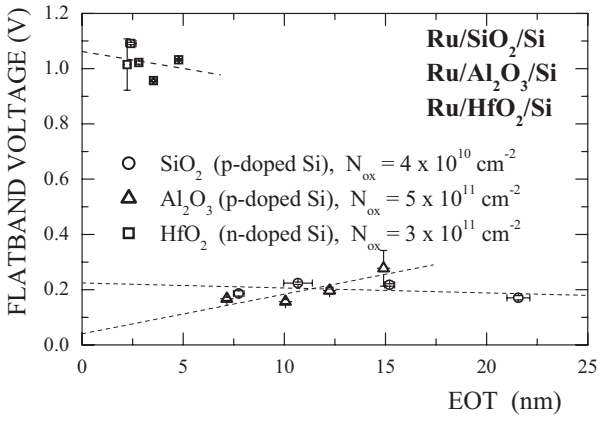


Figure 1. Determination of oxide charge density in MOS structures with SiO_2, Al_2O_3, and HfO_2 dielectrics and Ru gate.

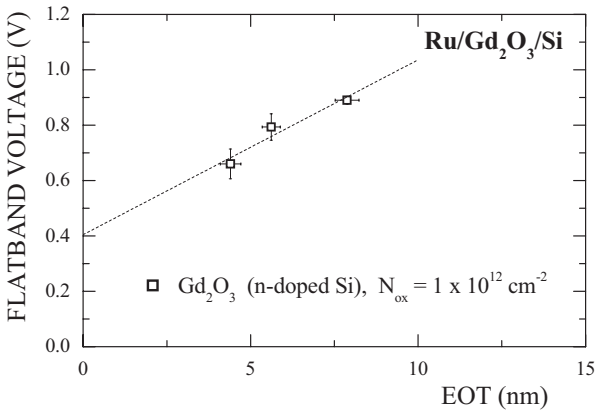


Figure 2. Determination of oxide charge density in MOS structures with Gd_2O_3 dielectric and Ru gate.

Flat band voltage and, consequently, oxide charge in MOS structures can be strongly influenced by post-deposition annealing in oxygen. Figure 3 and 4 show capacitance – voltage characteristics of Ru/$HfSiO_x$/Si and Ru/Gd_2O_3/Si MOS structures, respectively, after deposition and annealing in atmospheric pressure of oxygen at 500 °C during 30 min. The structures received FGA during 30 min at 430 °C after oxygen annealing. Thickness of the $HfSiO_x$ and Gd_2O_3 dielectric films is 7.5 nm and 9.8 nm, respectively.

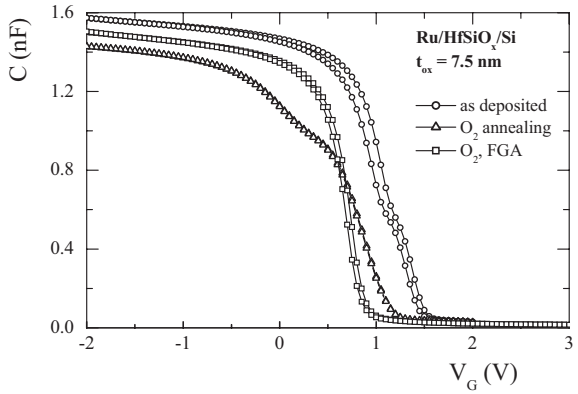


Figure 3. Shift of the capacitance – voltage characteristics of Ru/HfSiO$_x$/Si MOS structure after annealing in oxygen.

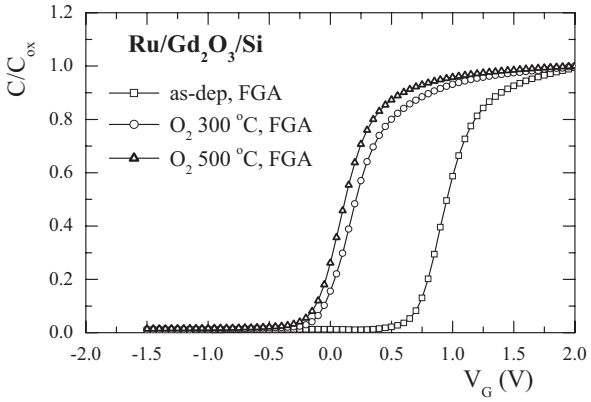


Figure 4. Shift of the capacitance – voltage characteristics of Ru/Gd_2O_3/Si MOS structure after annealing in oxygen.

To estimate the effect of oxygen annealing we fixed the Ru work function to 5.1 eV. Following Eq. (1) shift of the Ru/HfSiO$_x$/Si structure capacitance – voltage characteristic after annealing in oxygen is equivalent to decrease of initial negative oxide charge density from 6 * 10^{12} cm^{-2} down to 4 * 10^{12} cm^{-2}, Figure 3. Final oxide charge density after FGA 3 * 10^{12} cm^{-2} remains negative and is still high, but is lowered to its half value. In addition, hysteresis of the C-V curve, associated with trapped charge is strongly reduced by oxygen annealing. Observed capacitance decrease after oxygen and forming gas annealing can be attributed to SiO_2 interface layer increase. Stretched

capacitance – voltage characteristic of the $Ru/HfSiO_x/Si$ structure after oxygen annealing indicates significant amount of traps at the $HfSiO_x/Si$ interface. The density D_{it} of the traps at the interface of the oxygen annealed $Ru/HfSiO_x/Si$ structure drops below 10^{11} eV^{-1} cm^{-2} after FGA.

Even more pronounced effect of oxygen annealing is observed in the case of the $Ru/Gd_2O_3/Si$ structure, Figure 4. The structures were annealed during 30 min in atmospheric pressure of oxygen at 500 and 300 °C. The shift in flat band voltage of about 0.8 V after oxygen and forming gas annealing is equivalent to the change of originally negative charge with the density of $1.7 * 10^{12}$ cm^{-2} to positive charge of $1.3 * 10^{12}$ cm^{-2}. We suggest, that in the Gd_2O_3 film oxygen annealing fills oxygen vacancies, thereby decreasing defect oxide charges. Density of interface traps diminish from $3 * 10^{11}$ eV^{-1} cm^{-2} for the sample without oxygen annealing to $2.6 * 10^{11}$ and $1.1 * 10^{11}$ for the structure annealed at 300 and 500 °C, respectively.

The above-described results demonstrate, that low temperature oxygen annealing is effective process for reduction of oxide charges in high-κ dielectric based MOS structures. Oxygen annealing presumably improves stoichiometry of the dielectric oxide films. Subsequent forming gas annealing is necessary for passivation of the SiO_2/Si interface. Attention should be paid to appropriate post-deposition oxygen annealing conditions to avoid excessive SiO_2 interface layer growth.

Forming gas anneal is routinely applied in CMOS technology to decrease interface traps by the filling dangling bonds by hydrogen protons at the SiO_2/Si interface. Annealing of SiO_2/Si structures in forming gas at temperatures 450 – 650 °C was found to produce a considerable density of positive charged centers.[2, 3] There are theoretical[14] indications, that hydrogen is a possible source of positive fixed charge also in high-κ dielectrics.

Therefore, in the next step we have investigated the effect of forming gas annealing on fixed charge and density of interface traps in $Ru/Hf_xSi_{1-x}O_y/Si$ structure. The samples were annealed in forming gas from 430 up to 550 °C during 30 min. To verify the effect of FGA on fixed charge, we have submitted another $Ru/Hf_xSi_{1-x}O_y/Si$ structure to annealing in nitrogen at the same conditions. The structures annealed in nitrogen at various temperatures were subsequently annealed in forming gas at 430 °C. Capacitance – voltage characteristics of the $Ru/Hf_xSi_{1-x}O_y/Si$ structures annealed in forming gas and nitrogen, respectively, are displayed in the Figure 5. One can observe gradual shift of the capacitance – voltage characteristics to negative gate voltage with temperature increasing for both annealings.

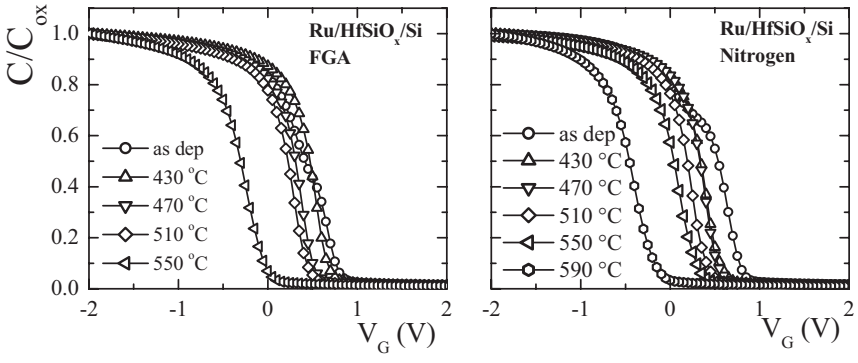


Figure 5. Capacitance – voltage characteristics of $Ru/HfSiO_x/Si$ MOS structures annealed in forming gas and nitrogen at temperatures from 430 up to 590 °C.

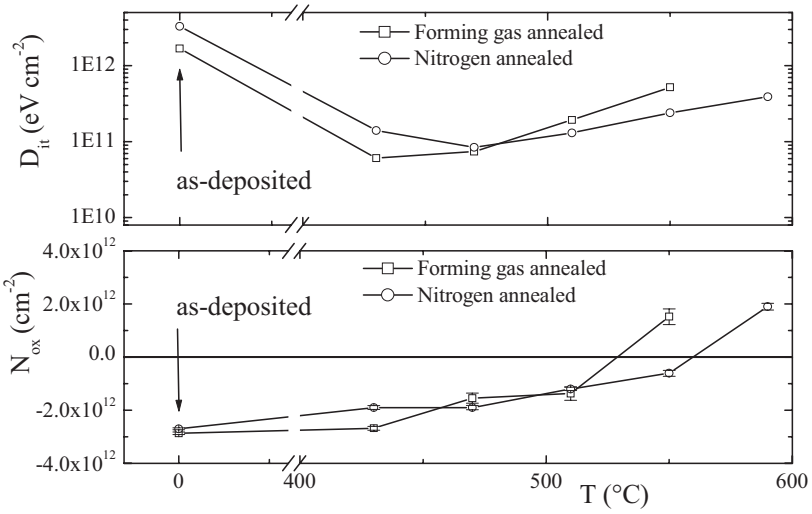


Figure 6. Density of fixed charge N_{ox} and interface traps density D_{it} of $Ru/HfSiO_x/Si$ structure as a function of forming gas and nitrogen annealing.

To evaluate the fixed charge in the films annealed in forming gas and in nitrogen, we fixed the work function of the Ru gate electrode to 5.1eV. Using Eq. (1) we calculated the fixed charge density from the flat band shift of the capacitance – voltage characteristics. Figure 6 shows evolution of the fixed

charge density and interface traps density as a function of annealing temperature for both forming gas and nitrogen ambients. Annealing in forming gas and in nitrogen have similar effect on $Ru/Hf_xSi_{1-x}O_y/Si$ structures: fixed charge density has negative sign in the as deposited structures with the value of $\sim 3 * 10^{12}$ cm^{-2}. With increasing of annealing temperature fixed charge in the structures becomes less negative. At temperatures above 500 °C the fixed charge changes its sign. Further annealing at temperatures above 550 and 590 °C in forming and nitrogen, respectively, degrades gate stack properties. Density of the interface traps has minimal value at temperature between 430 and 470 °C for both kinds of annealing.

We have speculated, that the apparent decrease of the negative charge with increasing annealing temperature in forming gas is due to compensation by positive charges, induced by presence of hydrogen.[9] However, similar behaviour of the $Ru/Hf_xSi_{1-x}O_y/Si$ structures in forming gas and nitrogen ambients rules out this hypothesis. It seems that decrease or compensation of negative charges during annealing is more likely due to annealing out of structural defects in the dielectric film. Additional analysis of hydrogen and nitrogen presence in the gate stack is necessary to explain mechanism of the fixed charge behaviour during annealing.

5. Summary

Fixed oxide charges in high-κ dielectric based MOS structures attain high values, close to $\sim 10^{12}$ cm^{-2}. Oxide charges can be reduced by post-deposition annealing. We observed, that annealing in oxygen effectively decreases charges in the dielectric, presumably due to improved oxygen stoichiometry. Forming gas annealing is necessary after oxygen treatment for passivation of the SiO_2/Si interface. Surprisingly, post-deposition annealing in nitrogen has similar effect as treatment in forming gas. Additional analysis of gases present in gate stack structures should clarify mechanism of the fixed charge behavior during annealing in forming gas and nitrogen.

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ELECTRICAL DEFECTS IN ATOMIC LAYER DEPOSITED HFO_2 FILMS ON SILICON: INFLUENCE OF PRECURSOR CHEMISTRIES AND SUBSTRATE TREATMENT

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Abstract. Capacitance-voltage, deep level transient spectroscopy, and conductance transient measurement results on atomic layer deposited (ALD) Al/HfO_2/Si structures are presented here. These methods assist in establishing the optimal process conditions to obtain high quality capacitors in terms of defect densities. Samples grown using novel precursor chemistries and substrate treatment have been compared. Based on our results, using growth sequences consisting of several ALD cycles exploiting both $HfCl_4$ and $Hf[N(CH_3)_2]_4$ precursors may occur advantageous compared to the process sequences consisting of ALD cycles using either $HfCl_4$ or $Hf[N(CH_3)_2]_4$. Regarding the substrate treatment preceding ALD, it seemed that HF-etching is more adequate than ^{t}BuOH treatment. In the case of chloride precursor, a thermal annealing in forming gas after HF-etching decreased the interfacial defect densities about one order of magnitude. On the contrary, when dimethylamide precursor was used, thermal annealing of HF-etched or butoxylated substrates did not improve the interface quality.

Keywords: High-k dielectrics, hafnium oxide, atomic layer deposition, MOS, electrical characterization, interfacial state density, disorder-induced gap states.

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1. Introduction

Hafnium oxide[1,2] is one of the most promising candidates to replace SiO_2 on the next microelectronic generations, for which there may be several reasons: high k (15-25) value, large Gibbs energy of formation, and as compared to ZrO_2, a better thermodynamic stability in contact with silicon. Atomic layer deposition (ALD) is a very suitable technique for obtaining uniform thickness films of high-k dielectrics because it allows a precise control of film composition and thickness as the growth proceeds one sub monolayer at a time on an atomic scale[3,4]. The growth conditions and precursors must be chosen to enable the self-limited deposition during every reaction step[5]. A great challenge is the control of the interface region between the deposited dielectric and the silicon substrate, because this region can significantly impact the electrical characteristics of the whole device, in terms such as the interface trap density, the near-interface oxide trap distribution, the gate leakage conduction mechanisms, and so on.

In previous works, we studied the effect of growth temperature[6] and post-metallization annealing[6], and the effect of precursor partial pressures[7] on the electrical characteristics of HfO_2 films fabricated by ALD. In this work we also present a comparative study on the electrical properties of metal-oxide-semiconductor (MOS) capacitors fabricated by ALD deposition of HfO_2 films on silicon substrates. But in this case different ALD sequences varying precursor and ALD cycles as well as different treatments of silicon surface previous to the dielectric growth have been tried in order to evaluate the effect of deposition conditions on both densities of interfacial states and of defects located very near to the interface but spatially distributed in the insulator, so called slow traps or disorder induced gap states (DIGS)[8]. Interfacial states have been measured by deep-level transient spectroscopy (DLTS), and DIGS profiles have been obtained by the conductance transient technique[9,10]. Capacitance-voltage (C-V) measurements assisted us to characterize some features of MOS devices such as flat-band voltage shift and hysteresis phenomena.

2. Experimental details

All the samples studied were grown in a hot-wall flow-type commercial F120 ALD reactor[11] onto <100>oriented n-Si (14 Ω cm) single crystal substrates. Two different Hf-precursors, $HfCl_4$ or $Hf[N(CH_3)_2]_4$ and H_2O were applied, in order to follow changes and possible compromise in dielectric behaviour. Film thicknesses and growth recipes are listed in Table 1. As for reference films, the growth temperature in the case of only the dimethylamide precursor used (K1784) is 250 ºC. It was chosen 50 ºC lower than in the case of chloride

precursor (K1771), 300 ºC. Indeed, in the dymethylamide case the most conventional temperature 300 ºC may already cause some thermal precursor decomposition[12]. However, for the films grown from both precursors in the

Table 1. Experimental details and some electrical characterization results corresponding to samples involved in the study of the influence of chemical precursors on the electrical defects of atomic layer deposited HfO2 on silicon.

Sample d_{HfO2} (nm)	Growth recipe	D_{it} (cm^{-2} eV^{-1})	Max. DIGS (cm^{-2} eV^{-1})
K2304 21	180 × [1 × $Hf[N(CH_3)_2]_4/H_2O$ + 1 × $HfCl_4/H_2O$]	6×10^{11}	1.4×10^{11}
K2308 30	45 × [4 × $Hf[N(CH_3)_2]_4/H_2O$ + 8 × $HfCl_4/H_2O$]	4×10^{11}	2×10^{10}
K2306 23	200 × [$Hf[N(CH_3)_2]_4$ / $HfCl_4$ / H_2O]	2×10^{11}	1.5×10^{12}
K1784 20.4	220 × [$Hf[N(CH_3)_2]_4/H_2O$]	$1–3 \times 10^{11}$	2.5×10^{11}
K1771 19.6	300 × [$HfCl_4/H_2O$]	2×10^{12}	4.5×10^{11}

same experiments (K2304, K2308, and K2306), substrate temperature as high as 350 ºC was used in order to improve the film growth rate. So, in Table 1, the reference samples are grown at the temperatures close to optimum ones in terms of low growth temperature and still reasonably low impurity concentration. Further, the samples grown using a novel combination of precursors were grown at maximum temperatures (350 ºC) not yet causing uncontrollable decomposition of $Hf[N(CH_3)_2]_4$ and achieving better purity in the case of $HfCl_4$ process. Since the effect of growth temperature to this double-precursor process is actually unknown, the temperature was elevated to 350 ºC to possibly achieve better purity. Studies on crystal growth and elemental composition are going on. Prior to the ALD deposition, all samples in the Table 1 were etched in 5% aqueous solution of hydrofluoric acid in order to remove the native SiO_2 layer, and then rinsed in distilled water.

In addition, we have compared the quality of films atomic layer deposited on HF-etched, propoxylated, or butoxylated Si, where the density of adsorption sites on silicon surface should be increased by anchoring alkoxy-groups by catalytic activation of $[Si\text{-}H]^+$ species with I_2 and subsequent formation of alkoxy-terminated surface[13]. That might increase the average homogeneity

and/but modify the trap density. The effect of a thermal annealing in forming gas (95% N_2 + 5% H_2) at 400ºC during 30 min. after evaporating the

Table 2. Experimental details and some electrical characterization results corresponding to samples involved in the study of the influence of substrate treatment on the electrical defects of atomic layer deposited HfO2 on silicon.

Sample d_{HfO2} (nm)	Substrate treatment Hafnium precursor	D_{it} (cm^{-2} eV^{-1})	Max. DIGS (cm^{-2} eV^{-1})
K1794Pr 8.4	Si-^{i}PrOH, unannealed $HfCl_4$	6–7 × 10^{11}	1.5 × 10^{11}
K1780H 7.4	HF-etched, unannealed $HfCl_4$	3-4 ×10^{11}	1.4 × 10^{11}
K1782HF400 4.1	HF-etched, annealed $HfCl_4$	1-2 × 10^{11}	6 × 10^{10}
K1782Bu 6.5	Si-^{t}BuOH, unannealed $HfCl_4$	2-6 ×10^{11}	3.2 × 10^{11}
K1782Bu400 6.5	Si-^{t}BuOH, annealed $HfCl_4$	2-3 × 10^{11}	5.5 × 10^{11}
K1776H 8.4	HF-etched, unannealed $Hf[N(CH_3)_2]_4$	1-2 × 10^{11}	2.2 × 10^{10}
K1779HF400 3.8	HF-etched, annealed $Hf[N(CH_3)_2]_4$	1 × 10^{12}	4.5 × 10^{11}
K1776Bu 7.9	Si-^{t}BuOH, unannealed $Hf[N(CH_3)_2]_4$	1-2 × 10^{11}	1.8 × 10^{11}
K1779Bu400 3.8	Si-^{t}BuOH, annealed $Hf[N(CH_3)_2]_4$	2-3 × 10^{11}	3 × 10^{11}

aluminium contacts has also been studied. Experimental details are shown in Table 2. The samples were grown at 300 ºC in the case of $HfCl_4$ and H_2O precursors, and at 250 ºC in the case of $Hf[N(CH_3)_2]_4$ and H_2O precursors. The growth temperatures were chosen to provide the film growth with residual chlorine content less than 0.5 at.% and carbon content less than 2 at.% in the case of $Hf[N(CH_3)_2]_4$ [12]. The amount of ALD cycles applied in order to achieve some, quite arbitrary, thickness was 100, 100 and 50 for samples K1794, K1780, and K1782, respectively, in the case of $HfCl_4$ process. For $Hf[N(CH_3)_2]_4$, the cycle numbers were 90 and 45 for K1776 and K1779, respectively. The annealing was made on samples which do not work in as-deposited state, because they are too thin, as we can see in Table 2.

In all cases, for both Tables 1 and 2, the Hf precursor pulse length was 0.4 s, while water pulse and purge times were always 0.5 s

The electrical measurements were carried out on Al/HfO_2/Si MOS capacitors. They were fabricated by e-beam evaporating aluminium electrodes on top of the dielectric layers. The 120-150 nm thick-Al dot electrodes had an area of 0.204 mm^2. To form nearly ohmic contacts on Si substrates, the backsides of the wafers were etched in hydrofluoric acid and metallized by evaporating a 100 nm thick Al layer.

3. Results and discussion

3.1. PRECURSOR CHEMISTRIES

In Table 1 some electrical characterization results are listed. Also, Fig. 1 shows 1 MHz capacitance-voltage curves measured at room temperature (a) and at liquid nitrogen temperature (b), whereas interfacial state density profiles provided by DLTS measurements are shown in Fig. 2. Lastly, we can see in Fig. 3 the three-dimensional plots of DIGS density (N_{DIGS}) as a function of the energy position related to the semiconductor conduction band edge ($E_{CSC} - E_T$), and of the distance to the interface (X_C) of some selected samples of Table 1.

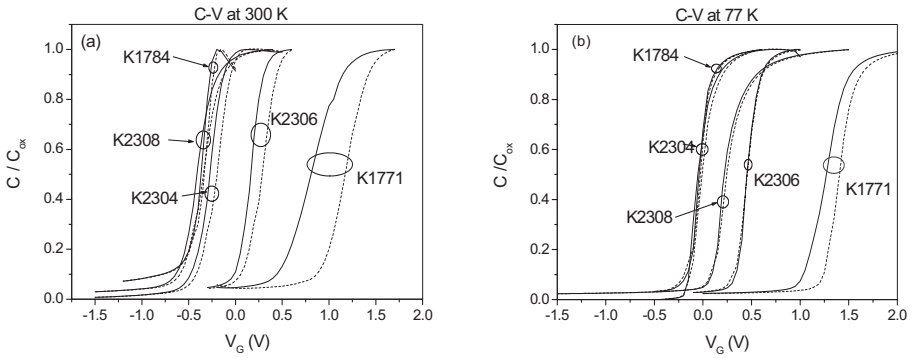


Figure 1. 1 MHz C-V curves for HfO_2 film-based MIS devices listed in Table 1. Measuring temperature: room temperature (a), 77 K (b).

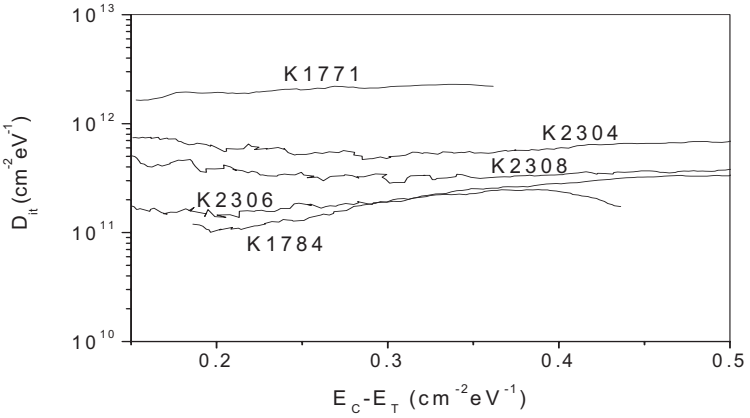


Figure 2. DLTS profiles for HfO_2 film-based MIS devices listed in Table 1.

By inspection of all these results we can conclude that the reference sample growth from $Hf[N(CH_3)_2]_4$ and H_2O (K1784) exhibits better electrical characteristics that the growth from $HfCl_4$ and H_2O one (K1771). The C-V curves corresponding to K1771 sample exhibited a great amount of flat-band voltage displacement and hysteresis value compared to those corresponding to K1784 one. Moreover, the mean interfacial state density value of K1771 is nearby to one order of magnitude greater that the value measured for K1784. Finally, DIGS density of K1771 is also greater than DIGS density of K1784.

It is very interesting to compare these two reference samples with samples grown by using sequences consisting of several ALD cycles separately for chloride and dimethylamide precursors (K2304 and K2308) and with samples grown by using sequences consisting of alternating single ALD cycles with each precursor (K2306). As for C-V and DLTS measurements, we could conclude that these three samples exhibit an intermediate behaviour between the two reference samples. However, if we also consider conductance transient measurements, we observe that DIGS density of K2308 is one order of magnitude lower than the best reference sample. Moreover, DIGS density of K2306 sample is more of three times the corresponding to the poorest reference sample. This might be explained as due to reactions occurring between the two precursors ($HfCl_4$ and $Hf[N(CH_3)_2]_4$) on the substrate. These reactions may produce distribution of contaminant residuals that deteriorate the HfO_2 film quality. The phenomenon can possibly be explained after closer, more detailed, study on the film growth mechanism in the future. As for K2304 sample, although DIGS density value is lower than the corresponding to reference samples, interfacial state density is clearly higher than the value measured in the other samples, except K1771. So, it is clear that using growth sequences

consisting of several ALD cycles separately for chloride and dimethylamide precursors can occur advantageous related to DIGS compared to the process based only in dimethylamide and water precursors. At the same time, process sequences consisting of alternating single ALD cycles with each precursor may not qualify because the high values of DIGS densities.

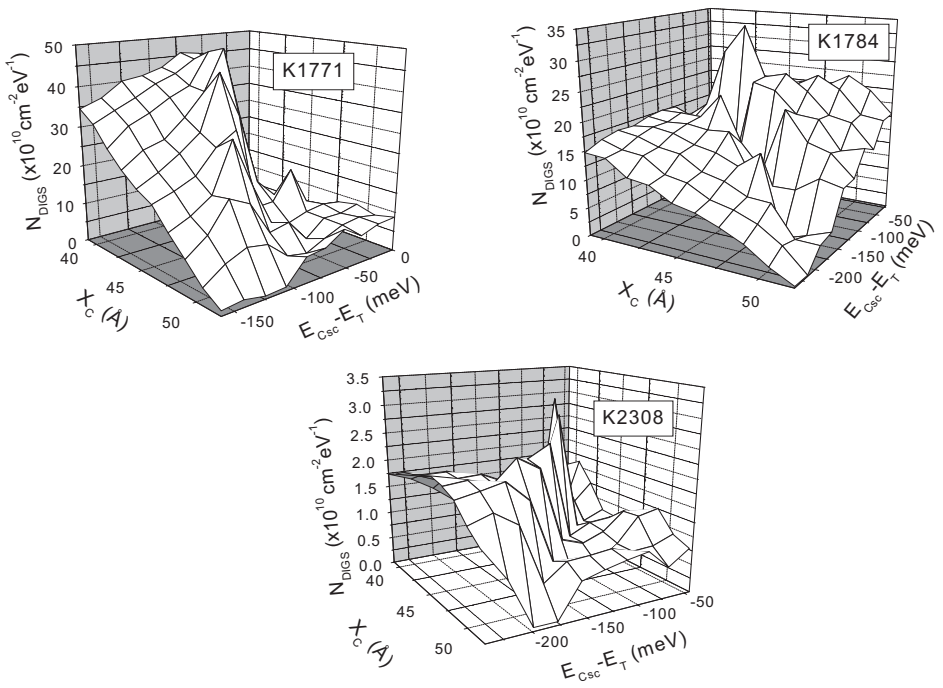


Figure 3. DIGS profiles of some selected HfO_2 film-based MOS capacitors listed in Table 1.

3.2. SUBSTRATE PRE-TREATMENT

As for the influence of substrate treatment on the electrical characteristics, some electrical characterization results are listed in Table 2. Also, Figs. 4 and 5 show C-V curves, and Fig. 6 shows interfacial state density distributions, obtained by DLTS, corresponding to these samples. Regarding the samples grown from chloride, our measurements indicate that MOS capacitors fabricated on unannealed HF-etched substrates exhibit better characteristics than those fabricated on unannealed ^{i}PrOH and ^{t}BuOH treated substrates. Indeed, C-V curves (Fig. 4) indicate that the flat-band voltage shift and the amount of hysteresis is greater in samples grown on silicon butoxylated or propoxylated

than in samples grown on HF-etched substrates. Also, in Fig. 6 (a) is shown that to HF-etched substrates correspond similar values of interfacial state density than to butoxylated ones, whereas in the case of propoxylated silicon, we obtain higher D_{it} values. Finally, from Table 2, DIGS densities are similar to ^{i}PrOH

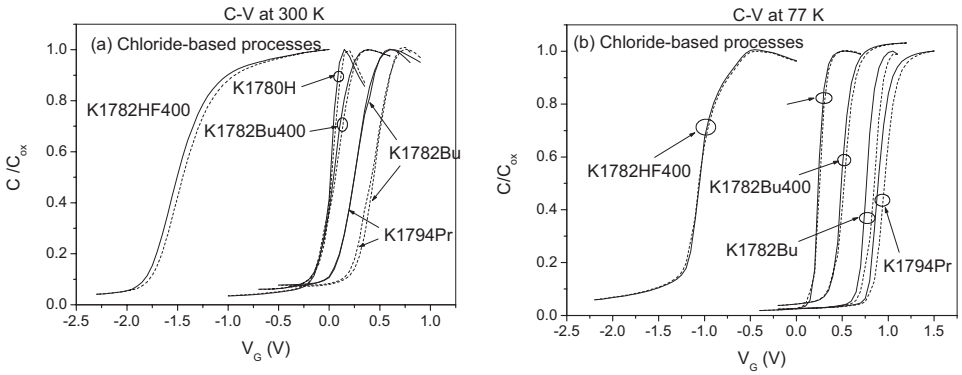


Figure 4. 1 MHz C-V curves corresponding to MIS devices based on atomic layer deposited by chloride-based processes HfO_2, listed in Table 2. Measuring temperature: room temperature (a), 77 K (b).

and HF treated substrates, lower than DIGS density obtained in the ^{t}BuOH case. Thermal annealing in forming gas after metallization provides better values of interfacial state density to respect to unannealed substrates both in the HF-etching and in the ^{t}BuOH cases, but DIGS density only diminishes in the samples based on annealed HF-etched silicon.

MOS capacitors fabricated with HfO_2 grown from dimethylamide on unannealed HF-etched substrates exhibit electrical characteristics similar to those fabricated on unannealed ^{t}BuOH treated substrates. Indeed, from C-V curves (Fig. 5), the flat-band voltage shift and the amount of hysteresis is only slightly lower in samples grown on silicon butoxylated than in samples grown on HF-etched substrates. Also, DLTS measurements indicate that to HF-etched substrates correspond near the same values of interfacial state density than to butoxylated ones (Fig. 6(b)). However, from Table 2, DIGS densities are clearly lower for HF treated substrates than to ^{t}BuOH ones. So, HF-etching is better than ^{t}BuOH substrate treatment in terms of DIGS.Secondly, thermal annealing in forming gas does not improve interface quality in terms of D_{it} nor DIGS in the ^{t}BuOH cases. Furthermore, C-V measurements (Fig. 5) revealed that flat-band voltage of annealed samples is less negative to respect unannealed ones, and hysteresis and stretch-out slightly increases. With regard to samples grown on HF-etched substrates, C-V measurements (Fig. 5) have indicated that thermal annealing clearly degrades the interface quality. Indeed,

flat band voltage shift and hysteresis amount strongly increases with thermal annealing. Moreover, annealing seems increase the interfacial state and DIGS densities one order of magnitude. Once again, reactions between residuals after the annealing, coming from the organic precursor, may degrade the oxide in a similar way as mentioned in the previous paragraph. These reactions seem not take place at room temperature, but upon heat-treatment.

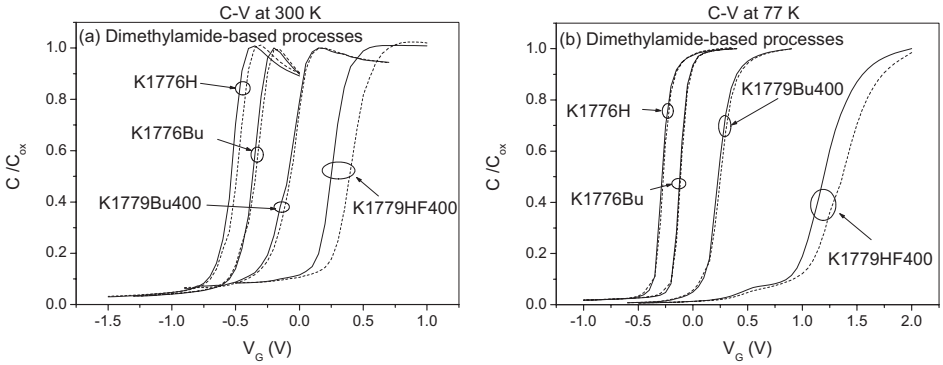


Figure 5. 1 MHz C-V curves corresponding to MIS devices based on atomic layer deposited by dimethylamide-based processes HfO2, listed in Table 2. Measuring temperature: room temperature (a), 77 K (b).

Finally, in comparing samples in Tables 1 and 2, we can expect that electrical characterization results will be very similar for the samples in both Tables grown by using the same precursor. So, K1784 (Table 1) and K1776H (Table 2) would be very similar, as both are grown by using $Hf[N(CH_3)_2]_4$ and water precursors. Also, K1771 (Table 1) and K1780H (Table 2), both grown by using $HfCl_4$ and water precursors, would have similar electrical characteristics. However, differences are observed, probably due to the very different thickness of samples in Tables 1 and 2. In a previous work[7] , we stated that for the $HfCl_4/H_2O$ combination of precursors the interface quality does not depend on the film thickness. However, the conditions of the sample preparation of samples studied in Ref. 7 were not entirely te same than the preparation conditions of those presented here: the films were grown in different reactor, by using longer pulses and higher water dose.

Then, it might become true that in the conditions more close to surface saturation the film/substrate interface is not that sensitive to the film thickness and accompanying fluent changes in ordering. Moreover, The effect of film thickness on the defect densities may not be similar in the cases of $Hf[N(CH_3)_2]_4$ and $HfCl_4$ based ALD processes. $HfCl_4$ process results in relatively pure films, whereas films grown from $Hf[N(CH_3)_2]_4$ are more heavily

contaminated by carbon and hydrogen. Critical crystallization thickness and temperature are higher in the case of $Hf[N(CH_3)_2]_4$, too. Therefore, in the particular case sample K1784 and K1776H might indeed show difference in DIGS density because of thickness.

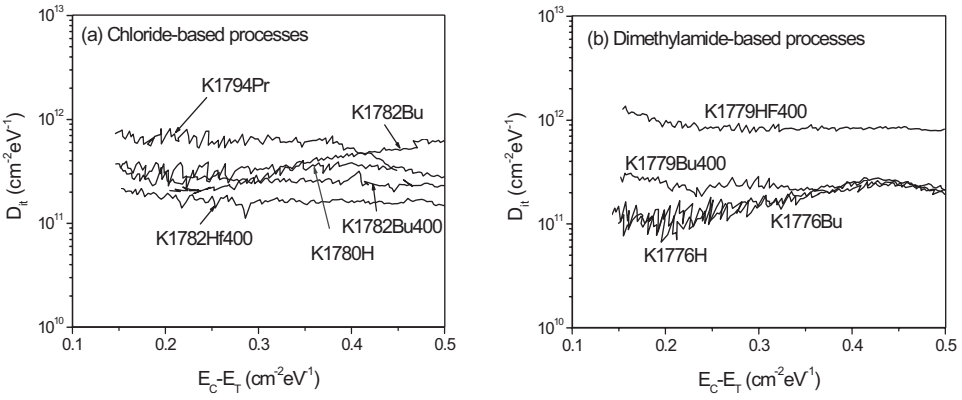


Figure 6. DLTS profiles for HfO_2 film-based MIS devices listed in Table 2.

4. Summary

A comparative study of the interface quality of Al/HfO_2/Si MOS capacitors has been carried out. By using different precursor chemistries, HfO_2 films have been atomic layer deposited on silicon substrates submitted to several previous treatments. The results indicated that growth sequence consisting of several subsequent alkylamide-water and chloride-water ALD cycles is advantageous mainly in terms of disorder-induced gap state densities compared to process sequence consisting of alternating single ALD cycles with each precursor. Indeed, we obtain D_{it} densities of about 4 x 10^{11} cm^{-2} eV^{-1}, and values of DIGS densities as low as 2 x 10^{10} cm^{-2} eV^{-1} by using 45 x [4 x Hf[$N(CH_3)_2$]$_4$ / H_2O + 8 x $HfCl_4$ / H_2O] growth recipe. When alternating single ALD cycles with each precursor are used, reactions between the two precursors, $HfCl_4$ and Hf[$N(CH_3)_2$]$_4$ can produce contaminant distribution and, thus, interface quality degrades. More work will be needed in order to clarify this kind of reactions.

In the case of $Hf[N(CH_3)_2]_4/H_2O$ precursors, the best results were obtained on unannealed HF-etched silicon (D_{it} densities of 1-2 x 10^{11} cm^{-2} eV^{-1}, and DIGS densities of about 2.2 x 10^{10} cm^{-2} eV^{-1}). When $HfCl_4/H_2O$ precursors were used, the best result corresponded to films annealed in forming gas at 400 ºC for 30 min. HF-etched silicon substrates (D_{it} densities of about 1-2 x 10^{11} cm^{-2} eV^{-1}, and DIGS densities of about 6 x 10^{10} cm^{-2} eV^{-1}). Butoxylated substrates did not

lead to better MOS devices as compared to HF-etched substrates. Thermal annealing in forming gas, although effective on HF-etched silicon with $HfCl_4/H_2O$ precursors, increased the amount of interfacial defects with both HF-etched and butoxylated silicon when $Hf[N(CH_3)_2]_4/H_2O$ precursors were used. Thermally activated chemical reactions between residual contaminants – nitrogen, carbon and higher amounts of hydrogen at the interface may be the cause of this degradation.

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THE EFFECTS OF RADIATION AND CHARGE TRAPPING ON THE RELIABILITY OF ALTERNATIVE GATE DIELECTRICS

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Abstract. The radiation response and long-term reliability of alternative gate dielectrics will play a critical role in determining the viability of these materials for use in future space applications. The total dose response of several potential replacement materials for SiO_2 in future IC technologies is discussed. Post deposition anneals and interfacial layer thicknesses are shown to significantly impact radiation-induced charge trapping. A discussion of reliability and negative bias temperature instability is also presented. It is shown that for current high-κ technologies, the dielectric strength is dominated by the low dielectric constant interfacial layer, and exposure to ionizing radiation can significantly increase bias instabilities.

Keywords: Alternative dielectric, high-k, radiation effects, reliability, oxide trapped charge, interface trap, MOS capacitor, MOSFET, NBTI, TDDB, bias dependence, process dependence, annealing.

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1. Introduction

To meet the need for reduced off-state leakage currents in highly scaled devices, several high dielectric constant (high-κ) alternative gate dielectrics to SiO_2 have been investigated for incorporation into future ICs[1-10]. While several high-κ gate dielectrics have shown reduced leakage currents, there are still several problems that need to be solved before high-κ gate dielectrics can be incorporated effectively into commercial ICs.

Finding a material to replace silicon dioxide is a formidable challenge because SiO_2 is a nearly perfect gate dielectric. Some of the most notable properties of silicon dioxide, which will likely be difficult to achieve with alternative gate dielectric materials are: (1) it is amorphous and remains thermodynamically stable on Si to temperatures exceeding 1100 °C, (2) it has a wide band gap (9 eV) with large (> 2.5 eV) conduction and valence band offsets for Si, (3) it is nearly insoluble in water, (4) it has a tremendous breakdown strength, and can maintain electric fields of up to < 15 MV/cm, (5) it can be processed with low (< 10^{10} cm^{-2}) densities of bulk and interfacial defects. Indeed, the only notable drawback to SiO_2 is that it has a relatively low dielectric constant (3.9). Some of the high-κ materials being considered for integration into future IC technologies are Al_2O_3, HfO_2, ZrO_2, Y_2O_3, TiO_2, and Ta_2O_5 and/or the silicates and aluminates of some of these materials[2,11-16]. Each of these materials has advantages and disadvantages, but none of them is currently at the material quality level of SiO_2. Still, all of these alternative gate dielectrics have a larger dielectric constant than SiO_2. Therefore it is possible to manufacture a gate stack that is physically thicker, yet electrostatically shows a capacitance which is similar to an ultra-thin SiO_2 layer. The increased physical thickness significantly reduces the probability of tunneling across the insulator, and therefore reduces the amount of off-state leakage current[2,5,13,15-20]. However, an increased dielectric constant usually comes at the expense of a smaller band gap and smaller conduction and valence band offsets between the substrate and the gate dielectric[3,17,21]. With the exception of Al_2O_3, most high-κ materials have a conduction band offset of only < 1.5-2 eV[22,23]. Since leakage current increases exponentially with decreasing film thickness and barrier height[24,25], this trade-off between dielectric constant and barrier height will limit the relative advantages an alternative dielectric offers in terms of reduced leakage current compared to devices with standard thermal gate oxides. Still, the initial data in the literature are promising, and most high-κ gate dielectrics exhibit < 5 orders of magnitude less leakage current than electrically equivalent SiO_2[3,13,19].

There are still problems that need to be solved before high-κ gate dielectrics can be effectively incorporated into commercial ICs. It is important to understand the stability and long-term reliability of these materials to ensure the problems

associated with ultra thin SiO_2 are not simply traded for an even larger set of problems with alternative dielectrics. Moreover, before these materials can be used for space applications, it is equally important to understand their radiation response. In this chapter we review the results of recent radiation studies of high-κ gate dielectrics and how radiation affects the long-term reliability of these materials.

2. Total Dose Radiation Effects

Ionizing radiation interacts with a CMOS device by producing electron-hole pairs (EHPs) in the gate and isolation dielectrics. Some of the radiation induced charge recombines and does not affect the device, but a significant fraction of the initial EHPs can become trapped at micro-structural defects in the dielectric. The mechanism for radiation induced charge generation and charge trapping in SiO_2 gate dielectrics is shown by the energy band diagram in *Figure 1*. This figure shows the case for a metal gate, p-substrate MOS capacitor, irradiated under positive gate bias. For this bias condition the electrons are swept out toward the gate electrode, while the holes transport toward the Si/SiO_2 interface via defect sites in the oxide[26]. Some of the unrecombined holes will become trapped in the oxide, forming a positive oxide trap charge density. As shown in *Figure 1*, protons are released during hole transport to the interface. These protons have been linked to radiation-induced interface trap formation in devices with SiO_2 gate oxides. Although *Figure 1* only shows hole trapping in the oxide, most gate dielectrics can also trap a significant density of electrons. Indeed, some HfO_2 films have exhibited more electron trapping than hole trapping after exposure to ionizing radiation[27]; however, the radiation induced oxide trapped charge in SiO_2 and alternative dielectrics is generally net positive[28-30].

Positive charge trapping in the gate and isolation oxides can invert the underlying Si, creating leakage paths, and enabling leakage current to flow in the OFF state condition (V_{GS} = 0 V). This will result in an increase in the static power supply current of an IC and may cause IC failure. Ionizing radiation can also change the interface trapping properties of a device. Interface traps are located directly at the interface with energy levels that exist within the silicon band gap[31]. Traps in the lower half of the band gap are donor like, meaning they are neutral when filled and positively charged when empty[31]. Interface traps in

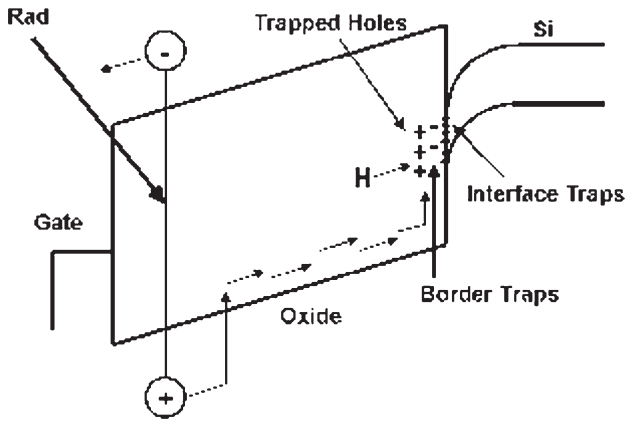


Figure 1. Energy band diagram showing ionizing radiation creating electron-hole pairs in the SiO_2 layer of a MOS capacitor under positive gate bias[26].

the upper portion of the band gap are acceptor like, meaning they are neutral when empty and negatively charged when filled[31]. In general, trap sites below the Fermi level are filled, and trap sites above the Fermi level are empty. Therefore, the number of occupied or unoccupied trap sites at the interface is bias dependent, and when a device is biased at midgap, the interface traps are neutral[32,33]. Interface trapped charge buildup tends to decrease the drive of transistors, degrading timing parameters of an IC[34,35]. For both present-day and future conventional MOS technologies, total ionizing dose radiation hardness is dominated by radiation-induced charge buildup in gate oxides and field or isolation oxides.

Historically, the gate oxide thicknesses of CMOS devices were relatively thick and radiation-induced charge buildup in gate oxides was a major concern. Fortunately, as IC technology is scaled and the gate oxide thickness is decreased, the radiation hardness of thermally grown gate oxides (SiO_2) can improve dramatically. It has been shown that oxide and interface trapped charge buildup is proportional to the square of the physical insulator thickness[31]. The physical reason one expects a t_{ox}^2 dependence is to account for charge generation throughout the entire volume of the oxide, and to account for the

moment arm effect resulting from the spatial distribution of the charges in the oxide projected to the interface[36]. Thus, excellent total-dose hardness is a supplementary benefit of aggressive gate oxide scaling. For very thin oxides (<20 nm), there is evidence that the amount of radiation-induced oxide-trap charge decreases with an even faster dependence on oxide thickness[37]. Because of the improvement in hardness with decreasing thickness, thermally grown gate oxides in advanced commercial technologies can be extremely radiation hard, withstanding accumulated doses in excess of 1 Mrad(SiO_2) with little threshold voltage shift. With high-κ gate materials, much thicker dielectrics and multi-layer stacked dielectrics can be used to obtain the equivalent capacitance of ultra-thin SiO_2 gates. This is a reversal of the oxide scaling trend and therefore raises the concern that gate oxide radiation response could worsen as alternative gate dielectrics are incorporated into future IC technologies.

3. Charge trapping in alternative gate dielectrics

It has been shown that the trapping properties of alternative gate dielectrics can be correlated to the trapping properties of other high-κ materials as well as electrically equivalent SiO_2 by a comparison of their trapping efficiencies[30]. Trapping efficiency is a dimensionless quantity used to approximate the intrinsic "trappiness" of an insulator[38]. For alternative gate dielectrics, it is possible to calculate an effective trapping efficiency. The effective trapping efficiency is defined as what the trapping efficiency would be if the gate dielectric was SiO_2 instead of a high-κ material. This definition is consistent with the concept of EOT, which describes what the thickness of the dielectric would be if the insulator was SiO_2 instead of an alternative dielectric. It has been shown that the effective trapping efficiency can be estimated for an alternative dielectric film using[28]

$$f_{ot} = -\frac{\Delta V_{mg}\varepsilon_{ox}}{q\kappa_g f_y t_{eq} t_{phys} D} \tag{1}$$

where f_{ot} is the effective trapping efficiency, ΔV_{mg} is the midgap voltage shift, ε_{ox} is the permittivity of SiO_2 (< 3.5×10^{-13} F/cm), $-q$ is the electronic charge, κ_g is the number of electron-hole pairs (EHP) generated per unit dose, f_y is the charge yield, t_{eq} is the equivalent oxide thickness, t_{phys} is the physical thickness of the alternative dielectric, and D is the total dose[28,38].

Effective trapping efficiency has been used to compare the radiation response of alternative gate dielectrics to thermal oxides of equivalent electrical thickness[28,30]. *Figure 2* is a plot of the radiation induced voltage shift for hafnium silicate gate dielectrics[28], aluminum oxide gate dielectrics[30], and

several thermal oxides[37,39-42]. These data show that the alternative dielectrics trap significantly more charge for a given total dose than the thermal oxides of similar electrical thickness. Some of the difference is due to the increased physical thickness of the high-κ films relative to the SiO_2, but the high-κ films also have a much larger trapping efficiency than the thermal oxides. For a total dose of 500 krad(SiO_2) the effective trapping efficiencies of the hafnium silicate and Al_2O_3 devices are < 28%, and < 19% respectively[28,30]. However, at this same total dose the trapping efficiency of the thermal oxides in *Figure 2* is only < 1.2%[28]. Still, even given a larger trapping efficiency, the high-κ films of most interest to industry (i.e., <4.0 nm) are still extremely insensitive to ionizing radiation as discussed below.

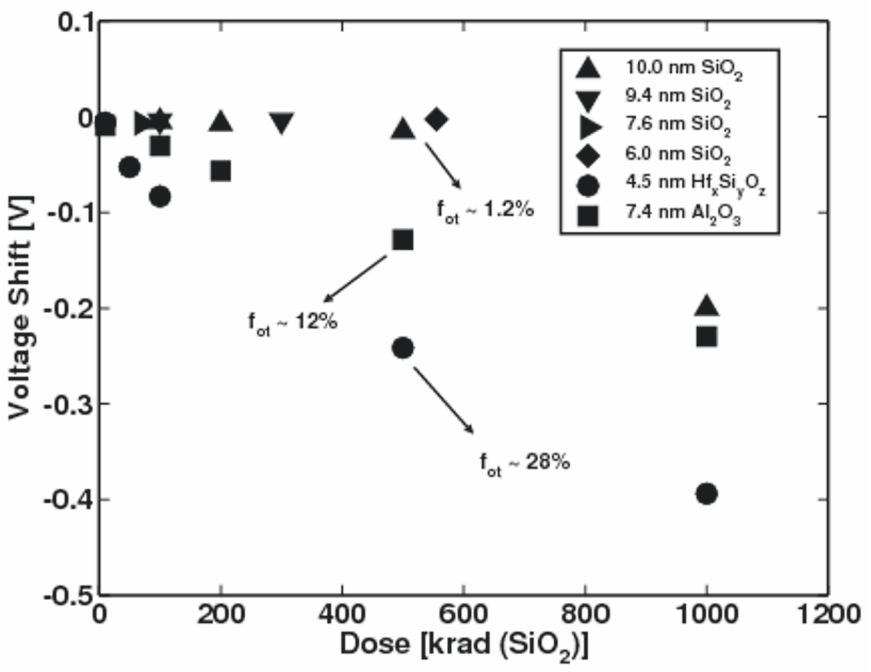


Figure 2. Voltage shift versus dose for several ultra thin thermal oxides and high-κ dielectrics. For similar electrical thicknesses, the intrinsic quality of the thermal oxides is much better than the high-κ films[30].

4. Effects of processing

From a manufacturing perspective, it is not clear which processing methods result in the highest quality, most reliable, alternative gate dielectrics[10,43]. For radiation effects, this has potentially serious implications because it is known that changes in processing can significantly alter the radiation response of a material[30,45]. Thus, it is important to understand how the various processing methods used to fabricate devices with alternative gate dielectrics affect the radiation response and reliability of these materials.

4.1. ALUMINUM OXIDES

Figure 3 is a plot of midgap voltage shift versus total dose for devices with 10 nm, 7.5 nm, and 5.0 nm Al_2O_3 layers deposited by atomic layer deposition on a 1.1 nm interfacial oxynitride for devices which received either a forming gas anneal (FGA) or an O_2 anneal and FGA[30]. It was shown that the devices that received the additional O_2 anneal had a significantly improved radiation response[30]. Similar results have also been observed in thermal oxides[44]. For doses greater than < 1 Mrad(SiO_2) the 10 nm and 7.5 nm O_2 annealed devices showed < 50% less voltage shift than the devices which received a FGA only. The 5.0 nm devices show almost no shift with dose up to 10 Mrad(SiO_2), and there is no measurable difference between the FGA and O_2+FGA processed devices. Therefore, the significant processing dependence shown in *Figure 3* essentially vanishes for film thicknesses of most relevance to commercial use.

The large differences observed in the 10 nm and 7.5 nm devices suggests that the O_2 anneal either decreases the density of hole trap precursors or increases the density of electron trap precursors in the near oxynitride interfacial region of the Al_2O_3 or at the Al_2O_3/oxynitride interface. It has been shown that the electron trap density in SiO_2 can be significant (on the same order as hole traps) and is dependent on device processing[45]. Electron traps are classified as either "deep" or "shallow" depending on their energy distribution. Deep electron traps are very stable, and will compensate some of the trapped holes, thereby

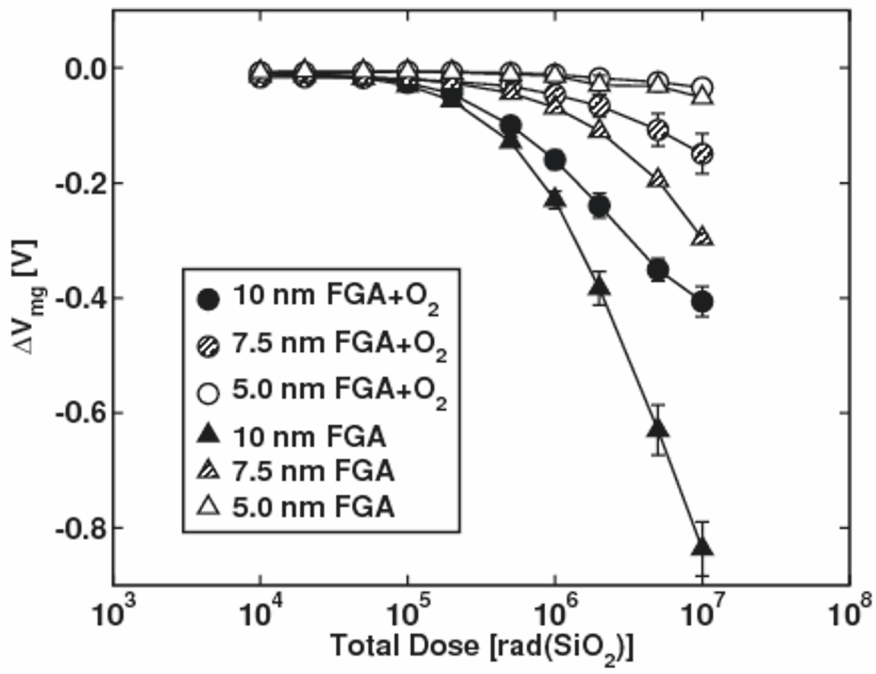


Figure 3. Midgap voltage shift versus dose for 10.0 nm (solid symbols), 7.5 nm (striped symbols), and 5.0 nm (open symbols) devices annealed with either a FGA or an O_2 anneal and a FGA after Al_2O_3 ALD[30].

reducing the net oxide-trapped charge density measured using the midgap CV shift method[45]. Shallow trapped electrons can move easily in and out of the gate dielectric, producing effects such as CV hysteresis. For the capacitors of Fig. 3, only the O_2 annealed devices showed a measurable hysteresis[30]. Thus, these data may be evidence of significant electron trapping in the Al_2O_3/oxynitride dielectric stacks that received the O_2 anneal. This result is consistent with early work on Al_2O_3 gate dielectrics, which showed those aluminum oxides had a significant density of electron traps[46]. Prior work often found that Al_2O_3 exhibited good total-dose radiation hardness because it trapped a significant amount of electrons, which compensated the trapped holes[46-48]. Furthermore, it

was shown that Al_2O_3 contains several trap levels in the band gap, making it easy for electrons to tunnel between the dielectric and the substrate[49,50]. Therefore, although the O_2 annealed devices of *Figure 3* may trap fewer holes, the possibility of increased electron compensation cannot be ruled out.

4.2. HAFNIUM OXIDES

Figure 4 is a plot of ΔV_{mg} for 7.5 nm Al_2O_3 (same data as *Figure 3*) and HfO_2 layers on 1.1 nm interfacial oxynitrides which received a FGA, O_2 anneal and FGA, or no anneal after high-κ atomic layer deposition. The HfO_2 devices that received no anneal show almost no shift at 10 Mrad(SiO_2), whereas the annealed devices shift < -200 mV. The HfO_2 devices in *Figure 4* had a hysteresis that varied with processing just like the Al_2O_3 devices of *Figure 3*. For all of the devices in *Figure 4* the amount of CV hysteresis was inversely proportional to the magnitude of the radiation induced voltage shift. Thus, the non-annealed devices show the best radiation response, and have the most CV hysteresis, whereas the Al_2O_3 devices annealed in forming gas have the worst radiation response and have no measurable CV hysteresis. It is interesting to note that the Al_2O_3 and HfO_2 devices that received an O_2 anneal and FGA showed similar amounts of CV hysteresis and have nearly identical radiation responses.

4.3. ELECTRICAL CHARACTERISTICS

Processing changes not only affect the radiation response of alternative gate dielectrics, but can also impact their electrical response. By comparing the capacitance-voltage (CV) characteristics of non-irradiated devices to a theoretical CV curve, it has been shown that processing changes have a significant impact on the amount of bulk and interface charge in these materials[30,51]. For example, devices that receive a FGA after high-κ deposition tend to show very little bulk charge, but have a large ($>10^{11}$ cm^{-2}) density of interface charge[51]. Conversely, devices which receive a FGA followed by an O_2 anneal show almost no interface charge, but exhibit a relatively large ($\sim 10^{12}$ cm^{-2}) density of fixed negative charge in the bulk of the material[51]. Furthermore, the O_2 annealed devices also exhibited a CV hysteresis of ~ 20-

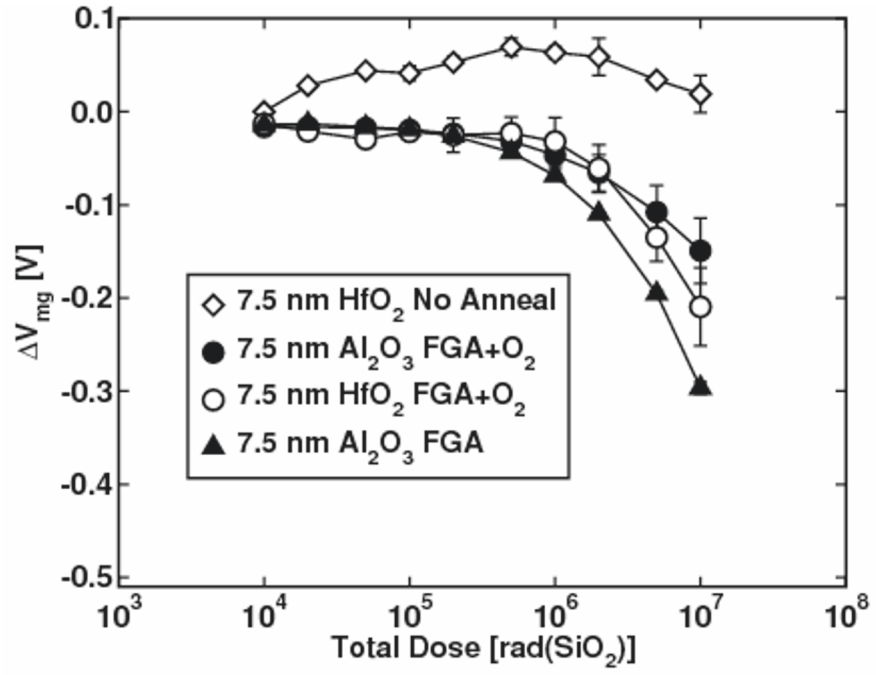


Figure 4. Midgap voltage shift versus dose for 7.5 nm HfO_2 and Al_2O_3 ALD deposited on a 1.1 nm oxynitride for several annealing conditions.

30 mV with a bias dependence that was consistent with electron motion into and out of border traps in the near-interfacial region of the gate dielectric stack[28,51]. Therefore, the current data suggest that an additional O_2 anneal improves the radiation response and interface quality while inducing negative trap charge centers in the bulk and a small CV hysteresis. Relating this to the discussion above in section 4.1, the electrical characterization data suggests that the improvement in radiation response that has been observed in some Al_2O_3 devices with O_2 anneal is the result of additional electron compensation

compared to devices that only receive a FGA. To quantitatively separate the effects of processing on electron and hole trapping in alternative gate dielectrics, it is necessary to use techniques such as thermally stimulated current (TSC)[52]. Recently some irradiated MIS capacitors with 20 nm Al_2O_3 gate dielectrics that were deposited by atomic layer deposition on a 1.0 nm interfacial oxynitride where characterized using TSC.

After exposure to 100 krad(SiO_2) these devices exhibited an oxide-trapped charge density of ~ 1.8×10^{12} cm^{-2}. After baking the device to 350 °C and measuring the TSC, it was found that the residual oxide-trapped charge was ~ 1×10^{12} cm^{-2}. Thus, after the TSC measurement, the net charge density was only reduced by ~ 55%. Similar results have been observed for SIMOX[53], doped oxides[54], and other high-κ gate dielectrics, and have been attributed to deep traps and impurities. In contrast, only a small[55] fraction of the oxide-trapped charge remains at 300 °C in high quality thermal SiO_2[52]. Indeed most of charge removal in SiO_2 generally occurs at temperatures between 150 °C and 250 °C, and has been associated with holes detrapping from E′ centers (oxygen vacancies)[52]. Currently defect microstructures for high-κ dielectrics are not well understood, but these preliminary TSC measurements suggest that the trapped charge distribution in alternative gate dielectrics may be somewhat more complex to what has been observed in thermal SiO_2. Furthermore, these data suggest there is a fairly significant portion of the radiation-induced charge trapped in deep traps that cannot be thermally annealed even at temperature as high as 350 °C.

5. Effects of the interfacial layer

Interfacial layer formation is one of the largest obstacles to high-κ integration. For maximum capacitance, it is best to have the high-κ material in direct contact with the Si substrate. However, it is currently difficult to create high quality direct interfaces between high-κ materials and Si. Indeed, most high-κ devices in the literature exhibit interface trap densites which are ~ 100 times larger than can be achieved for high quality thermal SiO_2 gate oxides[17,56]. Therefore, to improve interface quality it is common practice to use interfacial barrier layers (oxides or oxynitrides). The purpose of an interfacial layer is to take advantage of the natural Si-SiO_2 interface while also incorporating a high-κ material to increase the capacitance and thickness and thereby reduce the direct tunneling probability. Nitrided interfacial layers are also used to limit dopant diffusion into the channel. In a standard polysilicon CMOS process, the gate

electrodes are implanted with dopants such as phosphorous, arsenic, and boron[57]. The devices are then annealed at high temperatures to activate the dopant and distribute it throughout the polysilicon. If the dopants are able to diffuse through the gate insulator into the channel, they can change the threshold voltage of the device, or in large quantities, can increase drain to source leakage current. The problem is that a low permittivity interfacial layer reduces the capacitance of the gate stack and ultimately limits the effectiveness of the high-κ material. Even if it is possible to create a clean interface between silicon and a freshly deposited alternative gate dielectric, it is difficult to maintain that interface throughout a standard process flow because most high-κ materials are not good oxygen diffusion barriers[17,18,58]. Oxygen uptake is slowest for Al_2O_3, but even modest oxygen pressures are enough to cause significant interfacial oxidation[58]. In practice, interfaces that are nearly free of oxidized silicon have been achieved in a few systems, most notably Al_2O_3/Si(001)[59]. Still, avoiding silicon oxidation has been difficult in other materials systems. For Group IV metal oxides (HfO_2 and ZrO_2) there is typically an unintentional interfacial layer of SiO_2 that is ~ 0.5 nm or thicker[59-61].

It has been shown that the thickness of the interfacial layer can impact the radiation-induced trapped charge buildup and breakdown characteristics of otherwise identical high-κ gate dielectric stacks. *Figure 5* is a plot of ΔV_{mg} versus dose for 1.0 MV/cm biased exposures from 10 krad(SiO_2) to 10 Mrad(SiO_2) for devices with (a) a 2.5 nm oxynitride and (b) a 1.1 nm oxynitride which received only a FGA after Al_2O_3 deposition. For total doses up to 50 krad(SiO_2), none of the samples trap a significant amount of charge. After additional exposure, there is a clear difference in the amount of trapped charge for each Al_2O_3 film thickness at a given dose. By comparison of Figs. 5a and 5b, we observe a significant reduction in the amount of radiation damage for a given Al_2O_3 film thickness for the devices with a 1.1~nm oxynitride layer relative to devices with a 2.5 nm SiO_xN_y. These shifts are larger than would be observed in high-quality thermal SiO_2 of equivalent electrical thickness[37,39-52]. However, it is evident that total-dose degradation will not be a major concern for Al_2O_3/SiO_xN_y gate stacks of most interest to modern CMOS manufacturing processes (< 4 nm EOT), as there is only ~50 mV shift after a total dose of 10 Mrad(SiO_2).

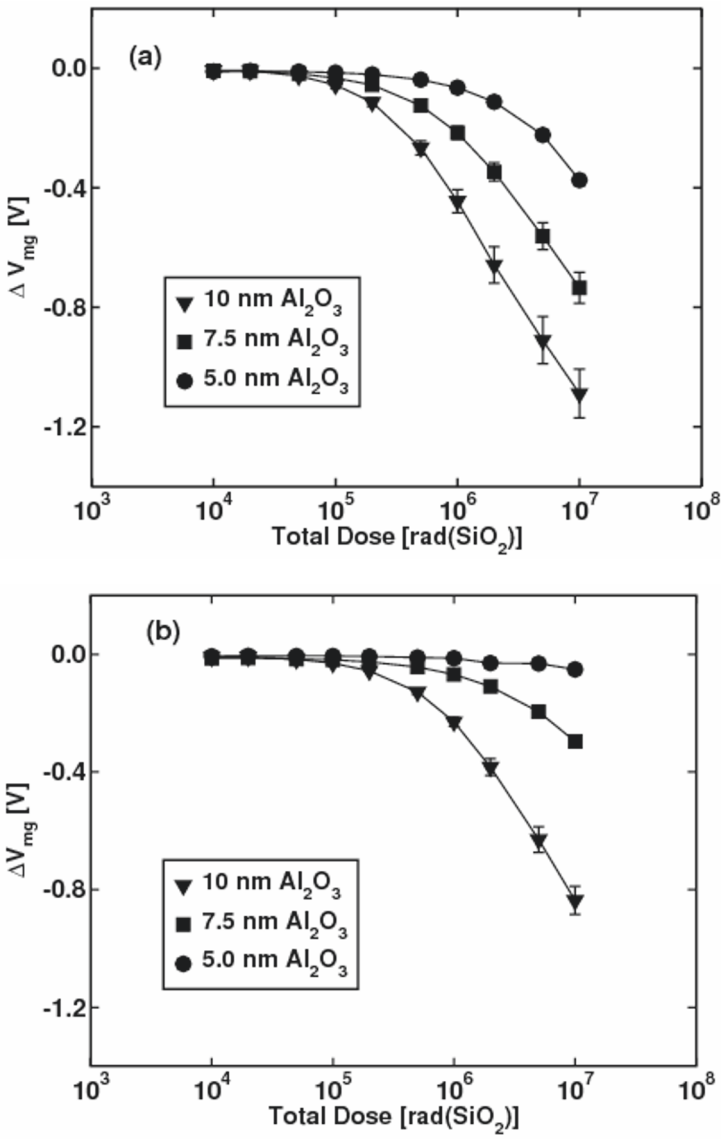


Figure 5. Midgap voltage shift versus dose for stacked Al_2O_3/oxynitride capacitors with (a) 2.5 nm interfacial oxynitride and (b) 1.1 nm interfacial oxynitride, irradiated with 10 keV x-rays at an electric field of 1 MV/cm[30].

It is interesting to consider why there is such a large difference in the amount of radiation induced trapped charge for a given Al_2O_3 thickness for the two separate interfacial layers. One would expect to see less trapping in the

films with the thinner oxynitride since there is less volume in these films within which to generate electron-hole pairs (EHPs). However, for a given Al_2O_3 thickness, the difference in ΔV_{mg} between *Figure 5*a and *Figure 5*b is more than that expected based on a volume argument alone. It has been shown that most of the measurable trapping in these devices occurs in the Al_2O_3 since the charge trapped in the oxynitride is removed due to tunneling[30]. As expected, we see more trapping for thicker Al_2O_3 films due to their larger volumes. However, for a given Al_2O_3 thickness, we see less trapping for the devices with a 1.1 nm oxynitride than a 2.5 nm oxynitride due to a greater tunneling probability for the thinner interfacial layer[30].

In voltage ramp breakdown tests it was shown that that the interfacial layer also plays an important role in the breakdown of the dielectric stacks for these devices. The samples with the 2.5 nm interfacial layer had an average breakdown of ~ 6 MV/cm with a standard deviation of ~ 0.5 whereas the devices with the 1.1 nm interfacial layer broke down at an electric field of ~ 4.7 MV/cm ± 0.6. This result is in good agreement with other data in the literature that suggest high-κ dielectric breakdown is determined by the interfacial layer[62,63]. Since these devices have a two-layer stacked dielectric with different dielectric constants, the electric field is different in each material for a given gate bias. For a two-layer gate stack, the electric field in layer one can be found by

$$E_1 = \left[\frac{\varepsilon_2}{\varepsilon_1 d_2 + \varepsilon_2 d_1}\right]\left(V_g - \phi_{ms}\right) \tag{2}$$

where ε_1 and ε_2 are the dielectric constant of layers one and two, d_1 and d_2 are the thicknesses of layers one and two, V_g is the gate voltage, and ϕ_{ms} is the work function difference between the gate and the substrate. Similarly, the electric field in layer two can be found by

$$E_2 = \left[\frac{\varepsilon_1}{\varepsilon_1 d_2 + \varepsilon_2 d_1}\right]\left(V_g - \phi_{ms}\right). \tag{3}$$

In comparing the electric fields in each of the layers at breakdown, we found that the fields in the oxynitrides were ~ 8-9 MV/cm whereas the fields in the Al_2O_3 were ~ 4-5 MV/cm. Therefore, the breakdown strength in these Al_2O_3/SiO_xN_y dielectric stacks is really limited by the interfacial layer. When the oxynitride breaks down, the entire gate potential is suddenly dropped across the Al_2O_3, and since it cannot maintain as large an electric field, it too breaks down.

Interface engineering is an extremely important aspect for the integration of alternative gate dielectrics into standard commercial IC processing. Minimizing

the thickness of the interfacial layer is beneficial from both an EOT standpoint as well as from an improved radiation response. However, the current data suggest that the interfacial layer dominates the high-κ breakdown strength such that the thinnest layers will ultimately limit the operational voltage for the device. Although the trend in IC design is for smaller operating voltages, the fields present in the lower dielectric constant interfacial layer are larger (as shown by Eqs. (2)-(3)) than in the thicker high-κ layer, and therefore devices with gate dielectric stacks could be susceptible to wear out and early failure. For example, the current time-dependent dielectric breakdown data in the literature suggests that several high-κ devices exhibit a broad failure distribution with a Weibull slope of ~ 1[14,19,51,62] as compared to commercial SiO_2 gate oxides of similar physical thickness which exhibit Weibull slopes of ~ 4 or larger[64]. A broad Weibull slope is indicative of a wide range of failure times, which makes it difficult to perform a lifetime extrapolation for a given use voltage.

6. Negative bias temperature instability

Negative bias-temperature instability (NBTI) is an important reliability problem affecting CMOS devices[65,66]. NBTI is associated with the generation of oxide and interface trap charge at the Si/dielectric interface, causing a threshold voltage shift and reduced drive current, when negative bias is applied to the gate for long times and/or elevated temperatures[67]. Although NBTI has been observed for more than 30 years[68], the origins of NBTI are still under debate. Recently, Zhou et al. compared NBTI in capacitors with thermal SiO_2 gate oxides to capacitors with HfO_2/SiO_xN_y gate dielectric stacks[69]. For the SiO_2 capacitors, the estimated activation energies were 0.27±0.03 eV and 0.31±0.04 eV for oxide-trapped and interface trap charge respectively. Similarly, for the HfO_2 devices, the activation energies for oxide and interface trap formation were estimated to be 0.35±0.04 eV and 0.22±0.03 eV[59].

Density functional theory (DFT) calculations show the critical role of the interactions of hydrogen with dopants in the Si channel in determining both the magnitude and the temperature dependence of NBTI in MOS transistors. A recently proposed mechanism for trap generation during NBTI stress is that excess hydrogen, weakly bound to the antibonding site at dopant atoms in the substrate is released as H^- and migrates to the interface to depassivate a Si—H bond[69-72]. Using first principles DFT calculations, it was determined that the energy required to move H from the antibonding site to a remote position in Si is 0.6 eV[70]. When combined with the 0.7 eV migration barrier for H^- in Si[73], a total activation energy of 1.3 eV is required for this process. This is in good agreement with the experimental value of 1.18 eV[74]. Because of the relatively

large density of dopant atoms in the substrate, only a very small percentage of dopant atoms must bind a hydrogen atom prior to NBTI stress in order to produce the numbers of interface traps typically measured in NBTI experiments[70].

As mentioned above, exposure to ionizing radiation also leads to the buildup of oxide-trapped charge and interface-trapped charge. Therefore, it is important to understand the combined effects of NBTI in a radiation environment. This is of interest since high-κ replacements for SiO_2 gate oxides could eventually be used in future aerospace applications. To date there have been little data published on this topic, but recently we combined effects of irradiation and bias-temperature stress have been compared in two types of capacitors[75]. The *n*MOS capacitors we tested have Al_2O_3 + SiO_xN_y as gate dielectrics, and the *p*MOS capacitors have HfO_2 + SiO_xN_y as gate dielectrics. The high-κ layer in both groups was prepared by atomic layer deposition using conventional surface chemistries; the physical thicknesses of Al_2O_3 and HfO_2 were 5.0 nm and 6.8 nm, respectively. For each type of device, 1.0 nm thick interfacial oxynitride films were thermally grown in a mixture of NO and O_2 at 900 °C, resulting in ~10 % to 15 % N incorporation in both groups. Al was deposited to form the gate electrode on each type of capacitors. Biased 1 Mrad(SiO_2) 10-keV X-ray irradiation at a dose rate of 31 krad(SiO_2)/min was performed on some capacitors before bias-temperature stress at positive, negative, or zero bias. Control groups that received only irradiation or bias-temperature stress were also employed. For negative or positive bias-temperature stressing, the MOS capacitors were heated with a hot chuck and held for 600 seconds at 75 °C, and then cooled to room temperature for measurement. The electric fields for biased irradiation and temperature stressing were ±2.1MV/cm. The trapped charge densities were determined by the midgap charge separation method.

In *Figure 6*, the overall shifts due to irradiation and bias-temperature stress generally are much larger for the HfO_2 + SiO_xN_y capacitors (*p* substrates) than the Al_2O_3 + SiO_xN_y capacitors (*n* substrates). Positive-bias (or zero bias) irradiation followed by negative bias-temperature stressing is the worst case environment of those investigated for the HfO_2 + SiO_xN_y capacitors, leading to a midgap voltage shift greater than 0.3 V in magnitude. On the other hand, negative-bias irradiation followed by negative bias-temperature stressing is the worst case for Al_2O_3+SiO_xN_y *n* capacitors. The results for the HfO_2 + SiO_xN_y capacitors in *Figure 6* suggest that the relatively small shifts observed for the irradiation-only cases are due to the presence of relatively large, nearly offsetting, densities of trapped positive and negative charges in the dielectric layers[76]. The application of negative bias leads to a significant increase in midgap shift after irradiation; this suggests that the negative charge probably is not stably trapped in the HfO_2, but likely is associated with border traps in the

SiO_xN_y. These electrons compensate the holes during the positive or zero bias irradiation, but are forced back into the Si with the application of negative bias at elevated temperature[77-80]. For the Al_2O_3 + SiO_xN_y devices, these results suggest there is either a smaller density of dipoles, or more stable trapped electrons[80], thus leading to the smaller shifts during the irradiation and bias-temperature stress. The presence of a large density of trapped electrons in HfO_2 dielectric stacks is consistent with the results shown in *Figure 4* above[43]. Although additional work is need to fully understand the relationship between radiation damage and NBTI, these results suggest potential reliability challenges for use of high-κ dielectrics in MOS ICs in a space environment.

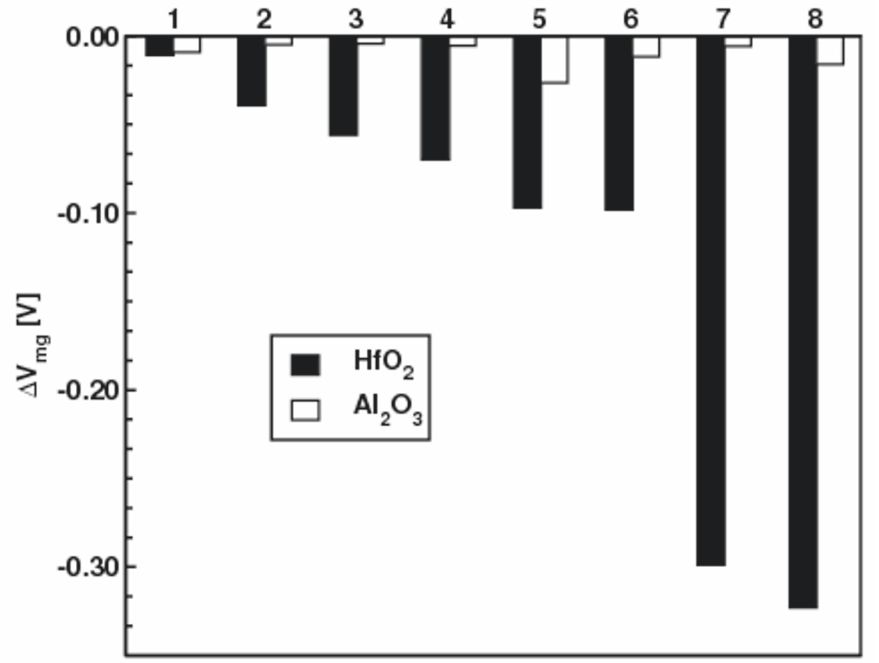


Figure 6. ΔVmg for Al/HfO_2+SiO_xN_y/pSi capacitors and Al/Al_2O_3+ SiO_xN_y/nSi capacitors under different experimental conditions: 1) negative-bias irradiation without bias-temperature stressing, 2) negative bias-temperature stressing (NBTS) without irradiation, 3) zero-bias irradiation without bias-temperature stressing, 4) positive-bias irradiation without bias-temperature stressing, 5) positive-bias irradiation followed by positive bias-temperature stressing (PBTS) 6) negative-bias irradiation followed by NBTS, 7) zero-bias irradiation followed by NBTS, and 8) positive-bias irradiation followed by NBTS. The electric fields for the irradiation and bias temperature stress were ± 2.1 MV/cm.

7. Conclusions

The midgap voltage shift for future high-κ films of most interest to industry (i.e., < 4.0 nm) are projected to be on the order of a few millivolts at doses of 1 Mrad(SiO_2) or more. Therefore, as is the case for ultra thin SiO_2, charge trapping in the gate oxide after exposure to ionizing radiation will not likely be a major concern for future devices, which incorporate alternative gate dielectrics. However, there are still several engineering problems that must be addressed before these materials can be reliably incorporated in future space electronics. Currently most devices with high-κ gate dielectrics have interface trap densities which are ~ 100 times larger than observed in thermal SiO_2 gate oxides. It is unlikely that IC manufacturers will be willing to incorporate high-κ dielectrics and accept the significant reductions in channel carrier mobility that come with degraded interface quality. Therefore, before alternative dielectrics can be a viable replacement to SiO_2, there must be notable advancements in the interface engineering of these materials. Since process variations can alter radiation hardness, it is important to continue to monitor the radiation response of high-κ dielectrics as processing conditions and material compositions evolve.

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CAN LEIS SPECTRA CONTAIN INFORMATION ON SURFACE ELECTRONIC STRUCTURE OF HIGH-K DIELECTRICS?

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Abstract. While investigating the surface composition of thin layers containing Hf with low energy ion spectroscopy (LEIS) utilizing He^+ ions with energy E_0=300÷800 eV, the fine structure of Hf line was observed. Hf spectrum consists of several narrow lines on top of a broad asymmetric peak. The number of lines and their separation does not depend on He^+ incident energy, but rather on the chemical composition of the surface layer: spectrum of metallic Hf is remarkably different from that of HfO_2, and, on the contrary, is very similar to $HfSi_x$. The observed effect is explained in terms of single electronic excitations due to promotion of Hf-He^+ molecular orbitals during impact which leads to the inelastic energy loss of He^+. Since LEIS is sensitive to the utmost surface layer, the observed effect can be potentially utilized to probe the surface electronic structure of compounds containing Hf.

Keywords: LEIS; high-k dielectrics; surface electronic structure.

1. Introduction

There is an enormous interest and significant research activities in developing novel high-*k* dielectric materials to replace traditional ultrathin (sub-2nm) SiO_2 gate oxides for advanced complementary metal-oxide-semiconductor technology[1]. Among many high-*k* insulators reported to date, family of hafnia based materials, such as HfO_2, $HfSi_xO_y$, HfO_xN_y, $HfSi_xO_yN_z$, currently emerges as a leading candidate. Among the challenges hindering the integration of these Hf based dielectrics into CMOS silicon technology, possible reaction(s) between poly-Si gate and high-*k* dielectric at elevated temperatures is a major concern. In addition, there is a problem of Fermi level pinning at the interface resulting from defects in the surface layer of dielectric.

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For an alternative metal gate approach, the effective work function of metal in contact with high-*k* dielectric is again determined by defects formed at the interface. It is therefore vital to monitor the surface electronic structure of HfO_2 and other Hf based dielectric layers during and upon heat treatments prior to the deposition of the gate material. Low energy ion spectroscopy (LEIS) is an analytical technique which is sensitive to the outmost surface layer. It is mostly used to determine elemental composition at the surface. However, LEIS spectra were also reported to exhibit the fine structure determined by the target surface electronic structure[2-4].

In this work, we have attempted to utilize the earlier observed effects in LEIS spectra to differentiate between the electronic structures of Hf based compounds. We present the experimental data for HfO_2 dielectric layers in comparison with metallic Hf as well as $HfSi_x$ and the model explaining the fine structure of the spectra. It is evident from our results that LEIS spectra taken with He^+ ions at the incident energy in the range E_0=300-800 eV are sensitive to the electronic structure of Hf compound and therefore can be potentially used to extract information on the surface electronic structure.

2. Experimental

Si(100) wafers dipped in 5% HF prior to the loading into the vacuum chamber were used as a substrate and mounted on the sample holder of electron spectrometer XSAM-800 (Kratos) equipped with the heater. Thin films of metallic Hf were grown by pulsed laser deposition (PLD) technique in the preparation chamber at the base pressure $P \sim 10^{-9}$ Torr. To grow Hf silicide, the sample was further annealed *in situ* at T=800º C. Thin layers of hafnia were formed by reactive PLD of Hf in O_2 atmosphere ($P(O_2)=10^{-3}$ Torr) at RT with subsequent annealing at T=700º C in the same oxygen environment.

LEIS experiments were performed *in situ* in the analytical chamber of the spectrometer. He^+ ions with the primary kinetic energy E_0=0.2÷1.0 keV were backscattered at θ=125º fixed for all the measurements, and were detected by a hemispherical analyzer of the spectrometer. Prior to LEIS experiments, the surface chemical composition of the sample was monitored by X-ray photoelectron spectroscopy. To minimize surface oxidation and/or contamination during LEIS experiment, the samples were kept heated to T=400º C. For comparison, LEIS spectra of Au surface in the same conditions.

3. Results and discussion

Experimental spectra of He^+ ions with primary energy E_0=0.2÷1.0 keV scattered from HfO_2 and metallic Hf surfaces are shown in Fig. 1.

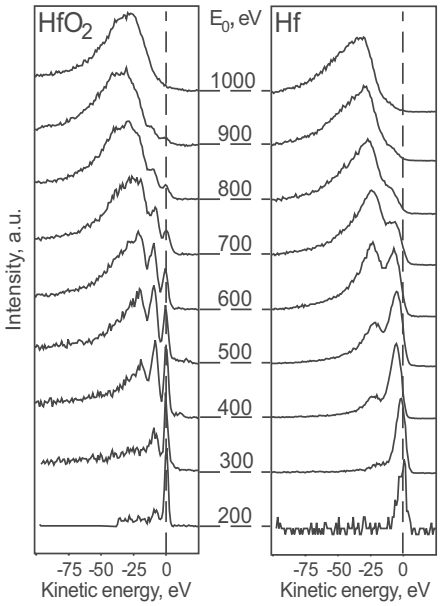


Figure 1. Normalized energy spectra of He^+ ions with primary energies E_0=0.2÷1.0 keV scattered from HfO_2 and Hf surface.

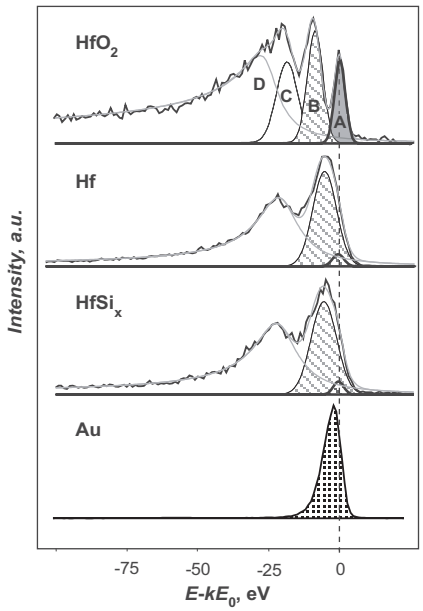


Figure 2. Normalized energy spectra of E_0=500 eV He^+ ions scattered from HfO_2, Hf, $HfSi_x$, and Au surface.

The spectra are normalized in intensity and are plotted on the energy scale so that the elastic binary Hf-He^+ collision energy kE_0 is set to zero. At low energies $E_0 \leq 200$ eV the spectra are dominated by one sharp peak (width at half maximum W=3÷7 eV) corresponding to the elastic scattering. With increase of He^+ energy in the range of E_0=300÷900 eV the intensity of this peak decreases while several additional sharp peaks (W=3÷10 eV) and a broad (W=40÷60 eV) asymmetric one appear. The total number of sharp peaks depends on the chemical state of the target Hf atoms: 3 for oxidized and 2 for metallic state. At higher energies (E_0>900 eV) sharp peaks are almost undistinguishable and only a broad asymmetric one is observed. The spectra obtained from $HfSi_x$ film (not shown) are very similar to those of a metallic hafnium. He^+ spectra taken for O and Si atoms of HfO_2 and $HfSi_x$ (not shown) do not reveal any fine structure.

For detailed analysis of Hf spectra structure the experimental data were fitted by Gaussian and asymmetric Doniach-Šunjić functions[5]. The former was

used to fit the sharp peaks because the broadening of elastic LEIS peaks is described by Gaussian function[6], while the latter, originally proposed to describe asymmetric lineshape of XPS spectra of metals caused by many-particle effects[7], was taken as a model function to fit a broad asymmetric background of LEIS spectrum. The result of the fitting is given in Fig.2 for the spectra of E_0=500 eV He^+ ions scattered from HfO_2, Hf, $HfSi_x$ and Au surfaces.

We denote the observed components of the spectra as: *A* for the peak of elastically scattered ions, and *B*, *C* and *D* for the peaks corresponding to ions undergoing certain additional energy loss. Figure 2 also shows the spectrum of He^+ ions scattered from the clean Au surface. A remarkable difference between Au and Hf spectra is evident. The Au peak is a single asymmetric line, 14 eV wide, and with a maximum shifted down to ~ 2.6 eV with respect to the value of elastic binary Au-He^+ collision, and can therefore be considered as a quasi-elastic peak with no fine structure.

The shifts of the spectral peak positions with respect to the energy of elastically scattered ions kE_0 are plotted as a function of primary He^+ energy E_0 for HfO_2 and metallic Hf in Fig.3, *a* and *b*, respectively.

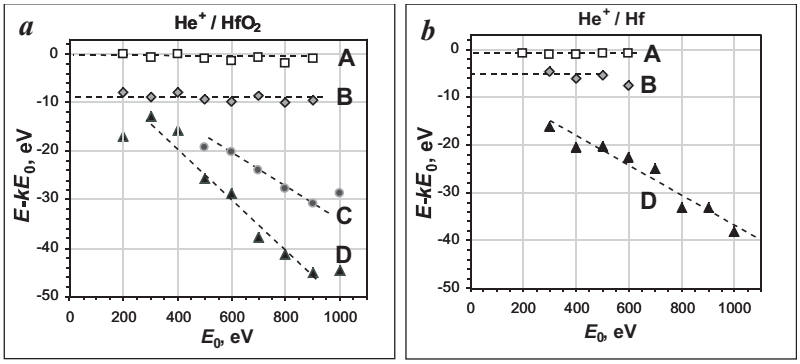


Figure 3. Energy shifts E-kE_0 for spectral peaks *A*, *B*, *C*, *D* for He^+ scattered from HfO_2 (*a*) and Hf (*b*) surface vs. E_0 as obtained by fitting the experimental spectra shown in Fig.2.

The position of peak *A* in the whole range of He^+ primary energies E_0=200÷900 eV corresponds to the energy of elastically scattered ions (E_A=0) within the accuracy ±(1÷2) eV of our experimental data. The width of the peak varies with E_0 in the range W_A=3÷7 eV. The energy of peak *B* with respect to the elastic peak is found to be E_B=9±1 eV and 5.0±1.5 eV for HfO_2 and Hf ($HfSi_x$), respectively, and is therefore sensitive to the chemical state of hafnium. The width of peak *B* is comparable to that of peak *A* for HfO_2 (W_B=3.5÷5.5 eV) and is slightly larger for Hf (W_B=7.3÷8.5 eV). The analysis of HfO_2 spectra reveals the presence of a second inelastic sharp peak *C* at E_C=19÷30 eV, most

pronounced at E_0=600÷800 eV. Its energy is constant (E_C=19±1 eV) for E_0=500÷600 eV and then linearly increases as a function of E_0. The fitting of the experimental spectra for HfO_2 with only three peaks *A*, *B* and *D* does not give satisfactory result. On the contrary, Hf and $HfSi_x$ spectra are well fitted by these three peaks, and so the peak *C* was not introduced in the fit procedure. For the primary energy E_0~300 eV the asymmetric background peak *D* appears at E_D=15÷20 eV and linearly shifts up to 40÷45 eV as a function of E_0. Its width increases with E_0 from ~20 to 65 eV.

The seemingly straightforward way to explain the observed fine structure of LEIS spectra for Hf is to attribute it to multiple elastic scattering of He^+ ions from Hf-Hf, Hf-O or Hf-Si surface atoms. However, in this case, the separation between peaks should linearly depend on E_0. Indeed, this is the case of peaks *D* and C at E_0>500 eV. The fact that the intensity of peak *D* increases with E_0 so that it dominates at E_0>700 eV, as well as its broad shape, indicates that it should be rather attributed to the energy loss due to multiple scattering from the deeper layers of the target than from its surface atoms. Longer interaction with target atoms during multiple scattering should result in higher probability of neutralization for such ions, so the peak *D* apparently comes from He re-ionized somewhere in the path[4]. However, the peak *B* can not be explained in terms of any elastic scattering since its energy does not change with E_0. Hence, it should be attributed to inelastic loss of He^+ energy during the collision.

The most important inelastic process during ion scattering from solid surface is related to the electronic excitations[2,8]. The charge-exchange excitation accompanied by the electron exchange between the scattering particle and the target atom results in either ion neutralization (Auger / (quasi)resonance neutralization QRN) or its subsequent reionization. During the neutralization process the kinetic energy of the scattering particle can not change significantly, while reionization process leads to the energy loss comparable to the ionization energy. The collision process may also induce single electronic excitations (SEE) of the target electrons[2] as well as collective electronic excitations (plasmons[8] and electron-hole pairs[9]) in metals also leading to energy loss.

The manifestation of the abovementioned processes in LEIS spectra for different ion/target combinations (H^+, D^+, He^+, N^+, O^+ and Ne^+ scattering form alkali-halides, oxides and metals) and the role of the surface electronic structure in these processes was investigated by Souda et al.[2-4]. The spectra of He^+ scattered from the insulators surface were generally found to consist of an elastic and two inelastic peaks that is qualitatively similar to our results. Here we apply the model of Souda[2-4] to explain our experimental results.

The schematic diagram of energy levels of He^+ and the band structure for metallic and oxidized Hf, as well as the corresponding MOs, is shown in Fig.4.

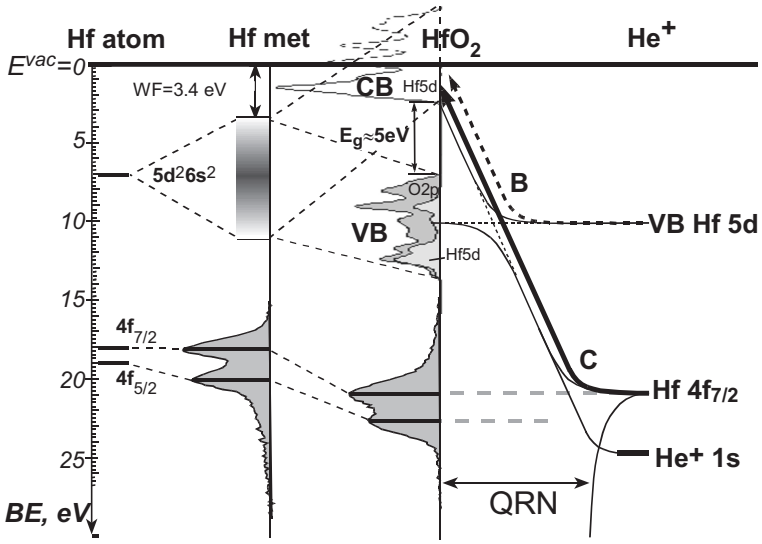


Figure 4. The schematic diagram of atomic energy levels for He^+ and Hf, as well as the band structure of metallic Hf and HfO_2 (courtesy of J. Robertson, Cambridge University, UK), and promoted molecular orbitals forming during the inelastic scattering.

Hf 4*f* levels are represented by experimental XPS spectra, while hafnia valence and conduction bands are the calculated density of filled and empty Hf 5*d* and O 2*p* states[10]. The binding energy (BE) of Hf4$f_{7/2}$ electrons with respect to the vacuum level is BE=21 eV and 18 eV for HfO_2 and Hf, respectively, the wokfunction for Hf is ~4 eV[11], the hafnia electron affinity is $\chi \approx 2.5$ eV and the bandgap $E_g \approx 5$ eV[12]. The formation of hafnia valence (VB) and conduction (CB) bands from metallic Hf 5*d*6*s* band splitting into bonding and antibonding MOs due to the covalent bonding with oxygen is indicated in Fig.4. by dashed lines.

In the violent collision process the atomic shells of an incident He^+ ion and a target Hf atom deeply penetrate in each other, so that the He-Hf system can be treated as a quasimolecule[13]. Spatial overlapping of the He^+ 1*s* orbital (BE=24.6 eV) with Hf 4*f* orbital resulting in their mixing and the formation of bonding and antibonding molecular orbitals (MO) shifted (promoted) in the opposite directions as shown with thin solid lines in the right part of Fig.4 (for clarity, only $4f_{7/2}$ component is shown). The promoted antibonding Hf 4*f* orbital interacts with the above-lying valence-orbitals resulting in the promotion of MO of the same symmetry correlated with valence levels (crossing of MOs with the same symmetry and parity is avoided[2,13]). Finally, a valence electron can be transferred to the open CB states of the target as indicated by thick dotted arrow *B*. The energy loss due to this process can be estimated as $E_{VB} - \chi \approx 9$ eV (E_{VB} is the energy of the valence electron in the middle of VB) which is

close to the energy of the observed inelastic peak *B* in the hafnia LEIS spectra. The peak *C* at $E_C \approx 20$ eV can be attributed to the energy loss due to the excitation of Hf 4*f* electron along the antibonding MO with its diabatic transition to MO correlated with valence level at the crossing point (thin dashed lines) as indicated by thick solid arrow *C* in Fig.4. The energy loss in this case should be $E_{Hf4f} - \chi \approx 22\text{-}2.5 \approx 19.5$ eV that is consistent with E_C value. Peak *C* could also be explained in terms of excitation of two valence electrons to the CB leading to the energy loss of $2E_B$=18 eV, although the probability of simultaneous excitation of two electrons seems to be less than that of one electron, and hence peak *C* intensity should be less than peak *B*, which is inconsistent with the experimental results for E_0>500 eV.

In the case of metallic Hf and $HfSi_x$ with no band gap, MO promotion can lead to the excitation of Hf electrons to the vacant state above the Fermi level E_F. Energy loss for 4*f* electron excitation is $E_{Hf4f} - E_F \approx 19 - 4 \approx 15$ eV that is close to the positions of peak *C* and *D* at E_0=300 eV. The excitation of valence electron at $E_{VB} \approx 7\pm3$ eV results in the energy loss $E_{VB} - E_F \approx 3\pm3$ eV close to the position of the peak *B* in Hf and $HfSi_x$ spectra. Note that none of the peaks can be attributed to surface plasmon excitations in Hf and $HfSi_x$ with energy $\hbar\omega_s$=7.8 eV that does not correspond to any of the observed peaks (see Fig.3,*b*).

The possible He^+ neutralization during the collision should also be taken into account. Indeed, due to the close energies of He 1*s* and Hf 4*f* levels ΔE=1.6÷3.6 eV and 4.6÷6.6 eV in oxide and metal, respectively, the quasi-resonant neutralization should occur. However, the presence of the elastic peak *A* in the experimental spectra evidences either the low probability of QRN process, or the re-ionization of He^0 in the collision. The latter process can be caused by the excitation of He 1*s* electron along the promoted MO to the target CB[2], leading to the energy loss of $E_{He1s} - \chi \approx 22$ eV for hafnia. Comparing this value with the energy of peaks *C* and *D* we conclude that the neutralization-reionization processes can also contribute to these peaks in the spectra.

It is worth noted that the promotion of MO, playing the main role in the SEE processes responsible for the observed spectral fine structure, strongly depends on the electronic structure of the target atoms, in particular, the orbital symmetry of the target atomic level overlapping with He 1*s* level. This promotion is strongly suppressed in the case of almost filled *d* orbital of the target located at $BE < BE_{He1s}$[2]. Hence, a weak promotion and no fine structure should be expected for the He^+ spectra taken from the surface of the noble metals, which is in agreement with the observed LEIS spectra of Au (see Fig.2). On the contrary, the presence of filled *f* levels in the target atom seems to activate the promotion of MOs, which is supported by the fact that the fine structure of He^+ spectra was also observed for some rare-earth metal oxides[14] (e.g., Yb_2O_3) having the similar electronic configuration as Hf: $4f^{14}5d^{0\div2}6s^2$.

Summarizing, the fine structure of Hf line in the LEIS spectra of He^+ back scattering from Hf, HfO_2 and $HfSi_x$ was observed. It is ascribed to the electronic excitations processes during the collision induced by molecular orbital promotion, and thus strongly depends on the core energy levels and the band structure of the target surface. Due to the extreme surface sensitivity of the LEIS technique, the observed effect can be used to probe the surface electronic structure of materials considered to be used in advanced CMOS applications. In particular, it is critically important to elucidate HfO_2 dielectric layer surface electronic structure during heat treatments and prior to the formation of a metal gate on top which seems to be possible utilizing the described effect.

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LOW SUBSTRATE DAMAGE HIGH-K REMOVAL AFTER GATE PATTERNING

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Abstract. As conventional SiO_2 gate dielectric is being replaced by high-k materials, a high-k removal process selective towards the Si substrate should be developed. High-k can be removed dry or wet. Dry removal (by plasma etch) is anisotropic (do not create an undercut in the high-k layer under the gate) but might damage the Si substrate. Wet removal could bring little or no damage to the substrate but creates an undercut due to its isotropic nature. Moreover, a crystallized (upon anneal) high-k can be hardly removed by wet treatment. For the Hf-based high-k materials (HfO_2 and Hf silicate with various Hf content) we propose a combi[1]ned removal approach: first the high-k is etched away partially dry (down to approx. 1 nm) by BCl_3 plasma, then the remaining plasma damaged layer is removed wet by an HF/HCl water solution. Such an approach combines advantages of both dry and wet removal techniques.

Keywords: high-k; dry high-k removal; wet high-k removal

1. Introduction

Continuous scaling down of semiconductor devices brings many challenges. One of them is the increased leakage through the gate oxide as it becomes too thin and allows carrier tunneling. Materials with high dielectric constant (high-k materials) are being introduced to replace SiO_2 as a gate dielectric since the high gate capacitance can be reached with a thicker layer of a high-k material that would reduce the leakage.

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Removal of the high-k dielectric after the gate patterning is a critical issue in the metal gate/high-k processing stacks. While the high-k should be completely removed the substrate should not be "touched" at all. There are two approaches for high-k removal: dry (by plasma) and wet. Every approach has its own advantages and disadvantages.

Dry removal provides anisotropy (no lateral attack of high-k beneath the gate) but brings damage to the substrate due to the plasma exposure. The most promising chemistry for dry high-k removal is BCl_3-based one. BCl_3 is known to etch metal oxides (most of high-k materials are metal oxides) with relatively high selectivity towards Si substrate, provided by formation of Si-B bonds.[1]

HF based solutions can be used for wet removal of the hafnium oxide-based high-k layers.[2] The wet removal can be selective towards the Si substrate un certain conditions, but due to its intrinsic isotropic nature creates an undercut in the high-k layer under the gate. Another drawback of the wet removal is the fact that even though the as-deposited amorphous high-k layers can be easily removed, the wet etch rate of an annealed high-k is very low[3] (high-k layers are known to crystallize during a post-deposition anneal).[4] However, the wet etch rate of a crystallized high-k layer can be enhanced by amorphization using, e.g. ion implantation.[5]

In this paper, we report a combined dry/wet removal process of Hf-based (Hf oxide and Hf-silicate with various Hf/Si ratio). The idea behind the combination of the dry plasma removal with the wet removal is the following: apply a dry etch plasma to remove most of the high-k layer but stop the process before reaching the Si substrate, in this way the desired anisotropy and damage the remaining high-k can be obtained. The remaining high-k layer, which is damaged (amorphized) by ion bombardment during the plasma exposure, is removed by a wet solution that is selective towards the Si substrate.

2. Experimental

The following high-k layers have been used: 2-4 nm HfO_2 obtained by atomic layer deposition (ALD) with or without post-deposition anneal at 700°C and hafnium silicates $Hf_xSi_{1-x}O$ with different Hf/Si ratios (23%, 55% and 65% of Hf), obtained by metallo-organic chemical vapour deposition (MOCVD). Thicker MOCVD high-k layers (30 nm to 40 nm) were used for the etch rate tests. Plasma etch tests were performed in a Lam Versys 2300 plasma etch chamber configured for 200 mm wafers. The following plasma etch parameters were used: plasma power = 450W, substrate bias = 55V, pressure = 5 mTorr, total gas flow = 100 sccm. An HF based solution ($HF/HCl/H_2O$, [HF]=0.03 m/l, pH=1) has been used to remove the remaining high-k layer completely. The etch rates and selectivity of this solution towards Si and SiO_2 were shown

elsewhere.[6] The thickness of the studied high-k layers was measured by spectroscopic ellipsometer (SENTECH SE801), the removal of the high-k layers (in terms of Hf concentration) was checked by Total Reflection X-ray Fluorescence (TXRF) technique that has the Hf detection limit of 10^{11} cm^{-2}.

3. Results and discussion

3.1. PLASMA ETCH RATE TESTS

The etch mechanism of metal oxide high-k (ZrO_2 and HfO_2) in Cl_2/BCl_3 plasma is supposed to be the following:[1] the metal oxide is reduced by BCl_3 through formation of a volatile compound BOCl, while chlorine forms volatile metal tetrachlorides with the reduced metal. It should be noted that pure Cl_2 is known to be inefficient for metal oxide etch since the times of Al metallization etch.[7] We have extended this theory towards the hafnium silicates high-k layers trying to optimise the etch process regarding the etch rate and selectivity towards the Si substrate. To find out the best chemistry for the dry high-k removal, we measured the etch rate of the different high-k dielectrics (HfO_2, Hf silicates and SiO_2 for comparison) in BCl_3/Cl_2 plasma mixture as a function of BCl_3/Cl_2 ratio.

The etch rate (ER) data are presented in Figure 1.

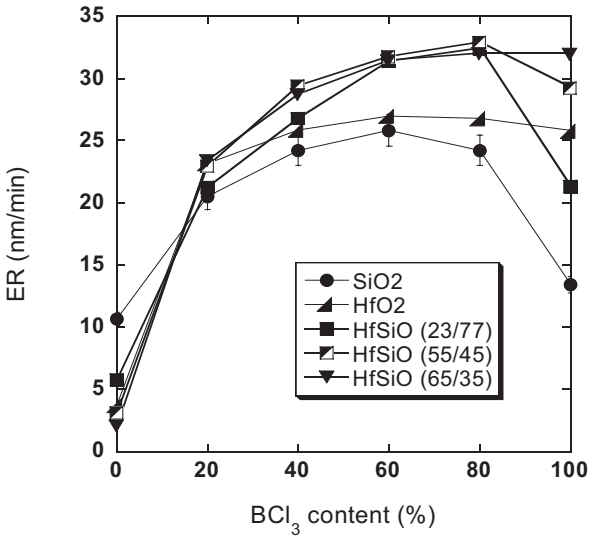


Figure 1. Etch rate of the studied high-k dielectrics in BCl_3/Cl_2 plasma as a function of BCl_3 content.

In general, all the dielectrics show similar etch behaviour: low ER in pure Cl_2 that increases in presence of BCl_3 and stays fairly constant until pure BCl_3 is used. Some differences, however, can be pointed out. In pure Cl_2, SiO_2 is etched with the highest rate (approx. 10 nm/min) while HfO_2 has the lowest etch rate (approx. 3 nm/min), the silicates with high Hf-content have ER close to that of HfO_2 while the ER of the silicate with only 23% Hf is slightly increased. For the intermediate BCl_3 concentrations all the silicates have slightly higher ER as compared to HfO_2 and SiO_2. In pure BCl_3, the ER of SiO_2 drops by almost 50% (from the maximal value at 60% BCl_3), while the ER of HfO_2 does not change significantly. The silicates exhibit an intermediate behaviour as compared to the two limiting cases (HfO_2 and SiO_2): the higher Hf content has the silicate, the less ER is decreased in pure BCl_3. The silicate with 65% Hf shows no decrease, while the silicate with 23% Hf shows a decrease comparable with that of SiO_2. It can be concluded that the dry etch behaviour of hafnium silicates falls between the two limiting cases: SiO_2 and HfO_2.

In order to select the best Cl_2/BCl_3 ratio for the high-k removal that is selective towards Si, the ER of Si was measured as a function of BCl_3 content. The ER data of Si, SiO_2 and HfO_2 are summarized in Figure 2.

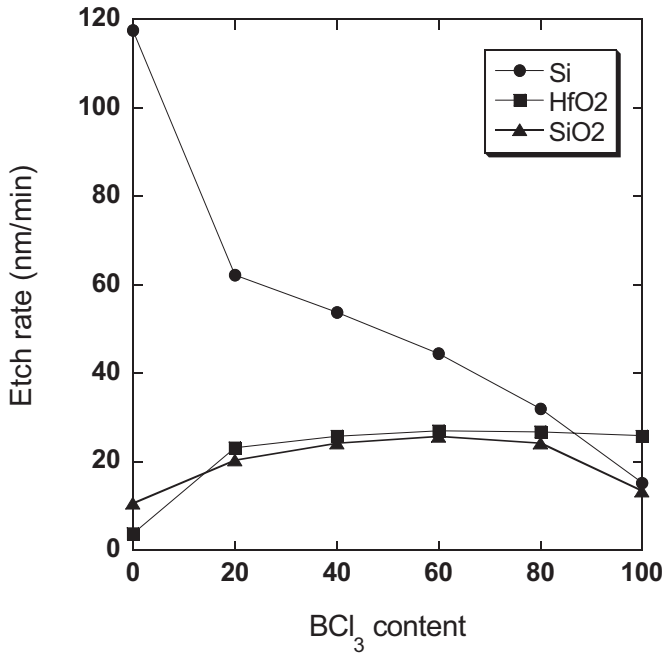


Figure 2. Etch rate of Si, SiO_2 and HfO_2 as a function of BCl_3 content in the Cl_2/BCl_3 plasma mixture.

One can see that the most promising candidate is pure BCl_3 plasma as it has the highest selectivity towards Si. Even though the high-k removal is intended to stop before reaching the Si substrate, a chemistry that is selective towards the substrate is preferred as it increases the process window and relaxes margins of error in the processing.

3.2. COMBINATION OF DRY AND WET REMOVAL

Addition of Si to HfO_2 (making hafnium silicates, in other words) increases crystallization temperature of this high-k.[8] As was mentioned above, non-crystalline high-k are wet etched much faster as compared to the crystalline ones. Therefore, we concentrated our efforts on the development of the dry/wet removal of the high-k layer that is most difficult to remove: HfO_2 with post-deposition anneal that results in the layer crystallization.[6]

To simulate the real metal gate/high-k stack, a layer of TaN (15 nm) was deposited on top of the high-k. The TaN was removed in two steps: main etch (ME) and over etch (OE). The ME consists of BCl_3/O_2 (5% of oxygen is added for gate profile control and found to produce little difference on high-k etch), the OE (which is at the same time a high-k removal step) consists of pure BCl_3. The high-k thickness as measured by spectroscopic ellipsometry (SE) after dry/wet etch is shown in *Figure 3*.

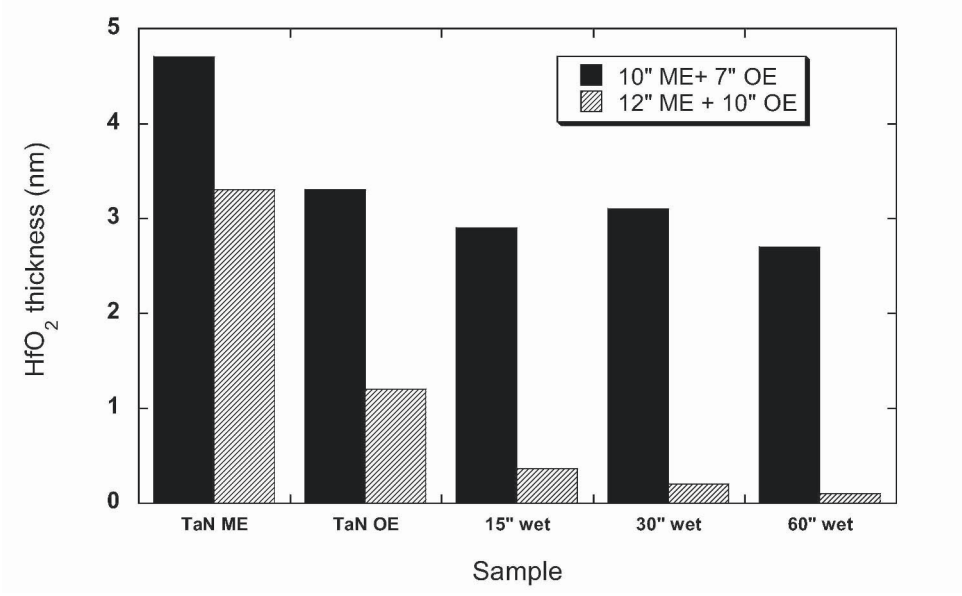


Figure 3. Thickness of the annealed high-k (measured by spectroscopic ellipsometry) after different dry and wet removal steps.

First, 10 s of ME was applied followed by 7 s OE. It was found by SE that the TaN is not completely removed by the ME (not shown in the figure) and approximately 3 nm of the high-k is left after the OE. The subsequent wet removal was not efficient for etching away the remaining high-k: even after 60 s of the treatment by the HF/HCl water solution the thickness didn' t decrease significantly with no clear trend observed. It can be concluded that plasma damage for the remaining 3 nm of the high-k was not high enough to amorphize the whole layer and facilitate the wet removal. As the etch time was increased (ME to 12 s and OE to 10 s), only 1 nm of the high-k layer was left after the dry etch. This remaining layer appears to be sufficiently damaged as it was readily removed by the same mixture. The 12 s ME plus 10 s OE was selected as the dry part of the removal process.

To confirm the high-k removal by the dry/wet process, TXRF measurements of three different high-k (HfO_2 with anneal, HfO_2 without anneal and Hf silicate with 50% Hf, no anneal) were performed after the dry removal combined with wet treatment of varied time (12 s and 30s). The results are presented in Figure 4.

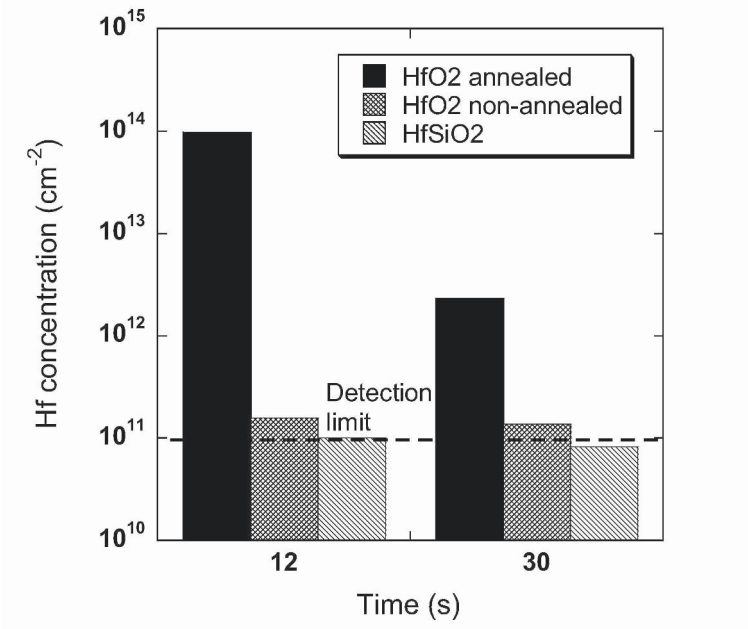


Figure 4. The surface concentration of Hf (as measured by TXRF) after the wet high-k removal as a function of wet removal time. The dry removal (combined with TaN etch) is 10 s ME and 12 s OE.

One can see that the concentrations of the non-annealed HfO_2 as well as the Hf silicate are below the detection limit already after 12 s, while the annealed HfO_2 is still present on the surface after 30 s of the wet treatment. However, the concentration of the latter high-k is rapidly decreasing (increasing the wet etch time from 12 s to 30 s decreases the Hf concentration by more than order of magnitude). The wet removal time of 60 s was selected as a final wet removal process for the annealed HfO_2. As only the plasma damaged high-k can be removed wet, no lateral etch under the gate is expected since the high-k under the gate is not exposed to plasma. Therefore, in the case of the annealed HfO_2 the wet removal time can be safely extended. For the non-annealed high-k, however, the wet etch time should be limited to avoid an undercut due to lateral etch of the high-k under the gate.

4. Conclusions

A combination of dry and wet etch processes can be used for high-k (HfO_2 and Hf silicates) removal without any exposure of the Si substrate to the plasma. The high-k is removed dry partially until only approximately 1 nm of the layer is left; the rest of the layer (damaged by ion bombardment during the plasma exposure) is removed wet. Care should be taken in selecting the dry removal time of a crystallized (annealed HfO_2) – if not enough material is removed by plasma, the wet treatment is inefficient in the removal of the remaining high-k.

It was found that pure BCl_3 plasma is a good candidate for the removal of the Hf-based high-k as it has relatively high selectivity towards the Si substrate. The dry etch behavior of Hf silicates in BCl_3/Cl_2 plasma was found to be intermediate to the SiO_2 and HfO_2 except the fact that at medium BCl_3 concentrations the silicates are etched slightly faster than both HfO_2 and SiO_2. The silicates with Hf content of more than 50% are etched in a way similar to HfO_2 while the silicates with lower Hf content behave more like SiO_2.

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MONITORING OF FERMI LEVEL VARIATIONS AT METAL/HIGH-K INTERFACES WITH *IN SITU* X-RAY PHOTOELECTRON SPECTROSCOPY

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Abstract. A method to monitor Fermi level changes at the metal/high-k interface depending on the materials of choice and peculiarities of interface formation is presented. The method is based on the deposition of ultrathin (1-5 nm) continuous and very uniform layers of Si, metal (Ni) or/and a dopant (Sb and Ge) marker layer on high-*k* (HfO_2) by pulsed laser deposition (PLD) and *in-situ* x-ray photoelectron spectroscopy (XPS) measurements. Core level binding energy shifts following Fermi level (work function) change at metal/dielectric interface were monitored. The method was applied to investigate the work function (WF) change during the silicidation reaction between thin Ni overlayer on thin $Si/HfO_2/Si(100)$ as well as the effect of the dopants on fully-sillicided (FUSI) gate formation and work function modulation. It was found that the effective work function in contact with HfO_2 was 4.4 eV, 4.5-4.7 eV, and 4.2 eV for NiSi, Ni_2Si, and Si+Sb, respectively, These values are in a good agreement with electrical measurements on MOS devices. Germanium interlayer at $NiSi/HfO_2$ interface produces no effect on FUSi workfunction.

Keywords: high-*k* dielectrics, x-ray photoelectron spectroscopy, metal gate, work function engineering, nickel silicide, pulsed laser deposition.

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1. Introduction

The scaling of gate length and gate oxide thickness in CMOS transistors dictates the need to replace SiO_2 as a gate dielectric for a novel high-*k* material[1]. It also aggravates the problems of poly-Si gate depletion, high gate resistance and dopant penetration from the gate into the channel. In addition, high-*k* and poly-Si gate may appear incompatible due to Fermi level pinning at the high-*k* / poly-Si interface which causes high threshold voltages in transistors[2]. As a result, there is an immense interest in metal gate technology. A metal gate material would eliminate the gate depletion and boron penetration problems, and also greatly reduce the gate sheet resistance. Metal gate approach requires a dual-work-function metal gate technology for advanced high-performance devices, analogous to poly-Si gate. Therefore, a major challenge is to find two metals with appropriate work functions (WFs) and to integrate them into a CMOS technology. In the selection of metal gate materials, a common assumption that the work function of a metal on a gate dielectric is the same as that in vacuum has been experimentally observed to be incorrect[3,4]. In practice, the effective metal gate work function is determined by the energy band alignment between the metal gate and the gate dielectric at the interface [4] which, in turn, depends on chemical reactions and/or defects at the interface. Therefore, the value for the effective WF can be determined only in the experiments on a particular metal/high-*k* dielectric system.

Recently, full silicidation (FUSI) of polysilicon gates was proposed [5,6,7] as a relatively simple approach to form metal gate electrodes for highly scaled CMOS transistors. Devices have been reported with several different silicides, prominently with nickel. Nickel monosilicide has a workfunction close to silicon midgap. Dopant pre-doping before silicidation was shown[8,9] to produce work functions closer to valence and conduction bands of silicon (for NFETs and PFETs), depending on the dopant type. In particular, As, P as well as B were capable to set threshold voltages useful to NMOS and PMOS transistors. However, this dopant segregation method which enabled a wide WF tuning for FUSI-NiSi on SiO_2 appeared to be not applicable to HfO_2 based dielectrics[9], due to the Fermi level pinning problem mentioned above. An alternative approach to control effective WF value by changing the composition (i.e. phase) of Ni silicide gate was then proposed [10].

In this paper, we propose a method utilizing x-ray photoelectron spectroscopy (XPS) to measure WF changes following the formation of metal gate on top of high-k dielectric by monitoring shifts in dielectric core level energy. XPS is a well established technique sensitive to changes in the chemical

state of elements in subsurface (~5 nm) layer as well as to the charging of defects and/or electric dipole layer built-up in this subsurface region. The proposed method is based on the sequential deposition of ultrathin (1-5 nm) continuous and very uniform layers of Si[11], metal (Ni) or/and a dopant (Sb and Ge) marker layer on high-*k* (HfO_2) by pulsed laser deposition (PLD) with the well-controlled rate of as slow as 0.01 monolayer/pulse and *in-situ* monitoring by XPS the elements core level binding energy shifts following Fermi level (work function) change at the metal/dielectric interface.

2. Principles of WF change monitoring with XPS

Schematic energy band diagram describing XPS experiment is shown in *Figure 1*. It is known that, generally, there is a contact voltage built between the metallic sample surface and the entry of the analyzer, and sample core electron binding energy (BE) is measured with respect to the Fermi level (E_F).

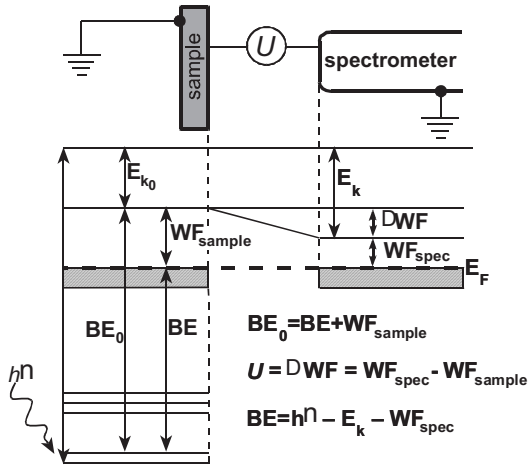


Figure 1. Energy band diagram illustrating XPS experiment.

In case of Si, the position of E_F depends on the type of dopant (*Figure 2*,a), and so is the binding energy of Si2p core level electrons. In fact, Si2p line appears to have different position for highly doped n^{++}- and p^{++}-Si (*Figure 2*,b), separated by silicon bandgap of about 1eV. When a compound is formed, the core level electron energy can change with respect to the pure element due to the change in the electronic structure of the valence band. However, this may or may not result in the change of BE value since E_F can also be modified in the

compound. Particularly, when Ni silicide is formed during solid state reaction in Ni/Si bilayer, both the chemical shift and E_F change may contribute to BE shift, and it is difficult to differentiate between them (*Figure 3*).

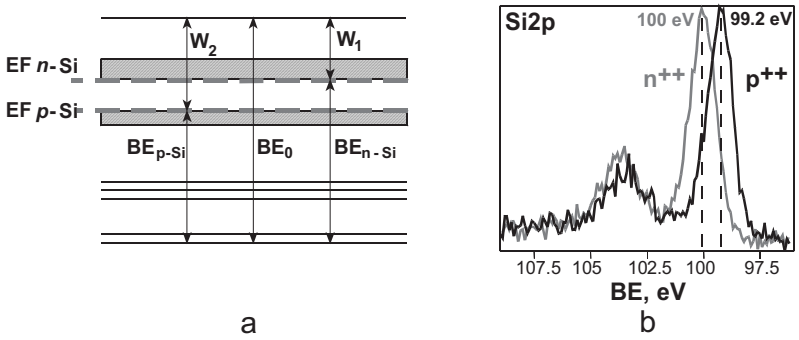


Figure 2. The effect of Si doping on the E_F position: a) schematic energy diagram; b) Si*2p* line recorded for n^{++}- and p^{++}-Si.

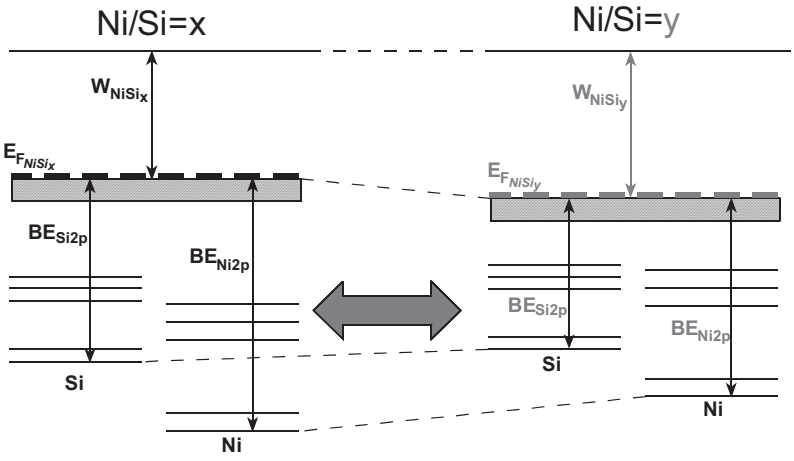


Figure 3. Contributions to Ni, Si core level line BE changes upon silicide formation.

For a dielectric, BEs of elements are not well defined and are "floating" depending on the charge neutralization of the sample surface following photoelectron emission (Figure 4,a). This remains the case upon deposition of an ultrathin continuous metal overlayer on top of dielectric, since it has the same potential as the dielectric surface (same vacuum level, Figure 4,b). However, once this metal overlayer is grounded (Figure 4,c), E_F of the metal

and that of spectrometer are equalized resulting in the shift of the underlying dielectric XPS lines (both metal or oxygen), and all changes in BE_{diel} are attributed to WF changes at the interface. Therefore, the idea of the proposed method is to monitor BE shifts in high-k dielectric (e.g., Hf4f core-level for HfO_2) "coupled" with the metallic overlayer.

Even when the metallic layer adjacent to the interface simultaneously undergoes changes of its chemical state (reactions, dopant diffusion), E_F (work function) and possible electric dipole built up at the interface, the core level line of metal in oxide (dielectric) will only follow the (effective) work function changes.

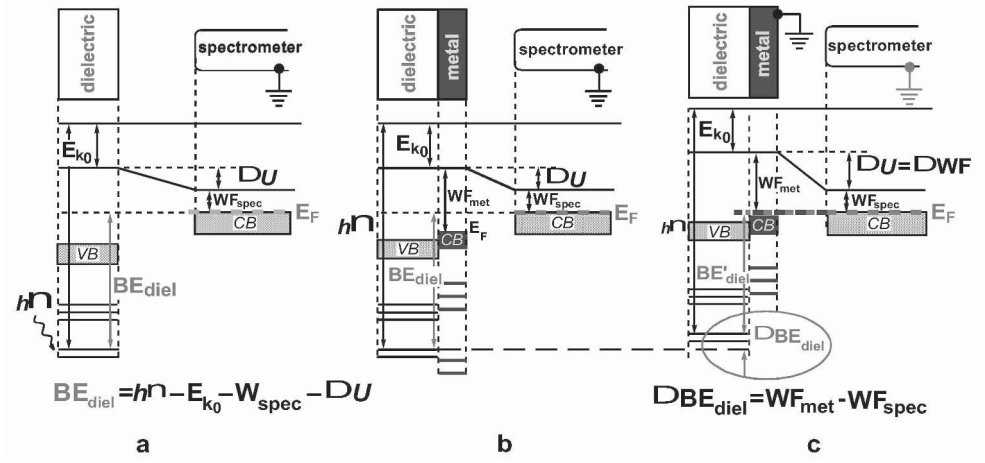


Figure 4. Energy band diagrams illustrating BE changes during XPS experiment on metal/dielectric stack: a) uncapped dielectric; b) metal cap on dielectric (not grounded); c) grounded metal cap.

It is important to note that the method does not allow to measure the absolute values of WF, but rather the changes with respect to a standard metal with known workfunction. The described method was applied to investigate the work function change during the silicidation reaction between thin Ni overlayer on thin $Si/HfO_2/Si(100)$ as well as the effect of the dopants on FUSI formation and work function modulation.

3. Experimental

The experiments were performed in a two chamber UHV system based on XSAM-800 spectrometer (Kratos). Preparation chamber (base pressure 10^{-7} Pa) was used to controllably grow ultrathin layers of Si and Ni, as well as marker layers of Sb, B and Ge in a ~ML thickness, by PLD employing the second harmonic of YAG:Nd laser (λ=532 nm), operating in the Q-switched regime (τ=15 ns) with the variable output energy E=50÷150 mJ and the pulse repetition rate ν=30 Hz. The deposition rates of ~0.01÷0.1 monolayer per pulse were calibrated with Rutherford backscattering spectrometry (RBS). The technique also allowed growth of alloyed Ni-Si layers with precise particular stoichiometry by sequential deposition of submonolayer coatings of Ni and Si. For the FUSI formation in this work, we used both approaches, namely (i) Si/Ni bilayer depositions followed by annealing at ~ 300-500 C, and (ii) co-deposition of Ni and Si. In some experiments a marker layer, for example Sb atoms were deposited or a thin Ge interlayer between the gate dielectric and Si overlayer. All the experiments were performed on samples with a 3 nm HfO_2 layer grown *ex-situ* by ALD on Si(100) with ~ 0.5 nm SiO_2 interlayer. A 100nm thick Au layer was separately deposited on the part of the sample surface to ensure electric contact between the spectrometer and the silicide overlayer to be formed during *in situ* experiment. Prior to PLD depositions, the samples were annealed up to 500^0C in UHV to remove hydrocarbon contaminations, as confirmed by XPS. The sample can be resistively heated up to T=500^0C thus allowing to study in-situ silicidation and related phenomena. The samples can then be transferred without breaking vacuum to the analysis chamber equipped with XPS (base pressure ~$5\cdot10^{-8}$ Pa).

XPS (Mg K_α source, E=1253.6 eV) spectra of Si2p, Ni2p, Hf4f, O1s lines as well as those of the corresponding dopants were acquired after each step of the deposition and the Ni silicide formation. Au*4f* $_{7/2}$ line at E_B=84 eV was used as a reference. The thickness of the Si, Ni and dopant overlayer was deduced from the attenuation of the Hf*4f* XPS signal (using the mean free path of the photoelectrons of λ~1.3 nm). One should note that the thickness of Ni/Si overlayer allowed us to probe the upper (Ni-Si/HfO_2) interface throughout the experiment and thus to obtain information on the relative changes in line positions for all the constituents. At the initial stages of overlayer growth, the bottom HfO_2/Si interface was probed as well.

4. Results and discussion

An example of the Hf*4f*, Ni*2p* and Si*2p* spectra evolution during sequential *in-situ* deposition of Si and Ni on HfO_2/Si and subsequent annealing in vacuum is shown in *Figure 5*.

The silicide phase formed upon the annealing to T=400^{0}C of Ni/Si bilayer structure or in a co-deposited alloyed Ni-Si layer is assumed to have the composition defined by the thickness of individual Ni and Si layers during deposition. BE's for Hf*4f*, Ni*2p* and Si*2p* lines along with the corresponding ΔWFs for different overlayers on HfO_2/Si(100) are collected in the *Table 1*.

Assuming WF for pure Ni overlayer is WF_{Ni}=5.1 eV[12] (BE_{Hf4f} =17.1 eV), the effective WFs for different Ni silicides including those "doped" with markers in contact with HfO_2 can be deduced. Particularly, for NiSi we obtain WF_{NiSi}=4.4 eV, regardless of the method it was formed, while for Ni_2Si phase the values WF_{Ni2Si}=4.5÷4.7 eV are obtained depending on the growth mode (bilayer vs. co-deposition).

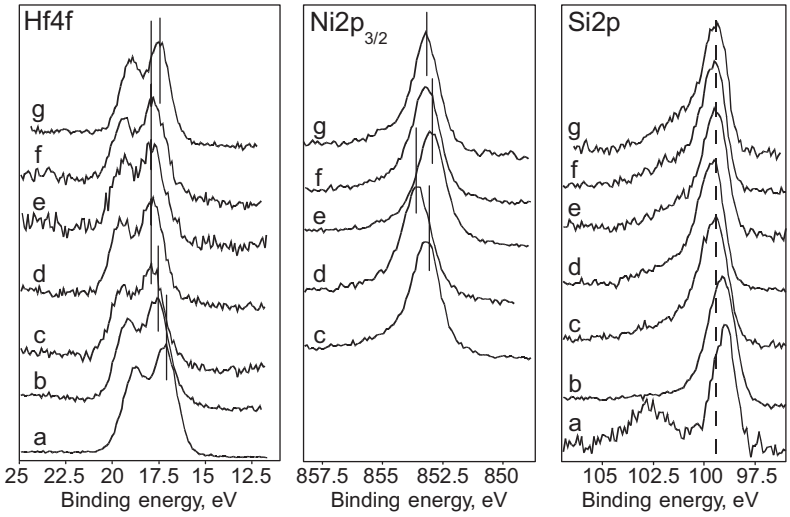


Figure 5. Hf*4f*, Ni*2p* and Si*2p* XPS spectra evolution for different stages of Ni silicide formation on HfO_2/Si surface: a) initial HfO_2 surface; b) deposition of Si (2 nm); c) further Ni (1.1 nm) deposition; d) annealling at T=300^{0}C, 1 min.; e) additional Ni (1.1 nm) deposition; f) annealling at T=300^{0}C, 3 min.; g) Ni-Si co-deposition (Ni:Si=2:1).

These values are in good agreement with the results obtained for devices with the corresponding silicide gates[10]. Nickel monosilicide is known to be a midgap material while the metal-rich phases are more PFET-like. In an attempt to model the dopant segregation method applied in FUSI, Si:Sb (~1:1) co-deposited layer was grown on HfO_2, and the resulting $WF_{Si\text{-}Sb}$=-4.2 eV (with respect to pure Ni). This value agrees well with NFET-like workfunction for Sb-doped Si. Surprisingly, Ge interlayer (~1 ML) deposited at HfO_2 surface prior to NiSi silicide growth does not affect effective WF of the latter.

Table 1. Ni*2p*, Si*2p* and Hf*4f* BEs (eV) for different overlayers grown on HfO_2/Si and calculated effective WFs (eV) with respect to pure Ni overlayer (WF_{Ni}=5.1 eV).

Overlayer/HfO_2	BE_{Ni2p}	BE_{Si2p}	BE_{H4f}	ΔBE_{Ni}	$\Delta WF(\Delta BE_{Hf})$	**WF**
Ni	852.5		17.1	0	0	***5.1***
NiSi	853.2	99.5	17.8	-0.7	- 0.7	**4.4**
NiSi co-deposition	853.2	99.5	17.8	-0.7	-0.7	**4.4**
Ni_2Si	852.8	99.4	17.7	-0.3	-0.6	**4.5**
Ni_2Si co-deposition	852.7	99.3	17.5	-0.2	-0.4	**4.7**
Si + Sb		99.7	18.0	-0.6	-0.9	**4.2**

By comparing BE shifts Ni→NiSi for Ni*2p*(ΔBE=-0.7 eV) and Hf*4f* (ΔBE=-0.7 eV), one can also conclude that all changes are attributed to WF change rather than to chemical shift.

5. Conclusions

We developed a method to monitor effective work function changes for a metal overlayer grown on high-k dielectric. The method is based on the pulsed laser deposition of ultrathin and continuous layers of metal and Si (as well as monolayer dopant markers) in combination with in situ x-ray photoelectron spectroscopy probing the whole stack including underlying dielectric layer. The method was applied to investigate WF changes following the formation of different phases of Ni silicides on HfO_2/Si as well as to elucidate the role of dopants in this process. Our results confirm that NiSi has a midgap WF=4.4 eV in contact with HfO_2, while for a Ni rich phase (Ni_2Si) WF is measured as

4.5-4.7 eV depending on the growth mode; Si-Sb alloy reveals WF=4.2 eV, and Ge interlayer at NiSi/ HfO_2 interface does not affect WF value.

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STRUCTURE, COMPOSITION AND ORDER AT INTERFACES OF CRYSTALLINE OXIDES AND OTHER HIGH-K MATERIALS ON SILICON

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Abstract. High-resolution medium energy ion scattering (MEIS) was used to investigate structure, composition and defects in amorphous and crystalline oxides, and their interface with silicon. Isotopic oxygen reactions were examined in several model high-κ systems, including Hf and Ce oxides, silicates and nitrided silicates as a function of composition, crystallinity and post-deposition annealing conditions. Our results show that for post-growth oxidation of Hf-based films there was extensive O exchange throughout the film which could be suppressed by the addition of SiO_2. Under our growth conditions, there was no measurable interfacial SiO_2 formation. In contrast Ce silicates exhibit rapid interface growth under similar oxygen exposures. Epitaxial $SrTiO_3$ and Sc_2O_3 films grown by MBE on Si were studied in different channeling geometries. We show that diffusion of Ti and O during

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$SrTiO_3$ film growth on Si (001) results in substitution of thin interfacial Sr silicide layer used at the initial stages of growth by Ti- or Sr-silicate like interfacial layers depending on the growth condition.

Keywords: ion scattering; interface; high-κ oxides; epitaxial oxides; Si

1. Introduction

Understanding the thermodynamics and kinetics of film growth during fabrication of high-κ gate stacks is vital to establish atomic level control of interfacial layers and to minimize defects. Annealing such films in different atmospheres may lead to diffusion and reactions with significant consequences on the electrical properties. Characterization of such films and the interfaces they form with the semiconductor substrate is challenging, in particular if quantitative information is needed. Medium energy ion scattering (MEIS) has emerged as one of the most powerful methods for investigating buried layers and interfaces with high depth resolution (sub-nm).[1] As the ion-solid interaction is classical and well understood, the technique is quantitative and element specific. By using isotope tracing, most commonly ^{18}O, one can study not just the structures of such ultrathin films,[2, 3] but also the processes responsible for their formation. In this paper, we briefly summarize some recent results related to structure, composition and defects in amorphous and crystalline oxides, and their interface with silicon.

1.1. AMORPHOUS OXIDES ON Si: Hf AND Ce

We will first consider Hf and Ce oxides with specific emphasis on their behavior during annealing in an oxygen atmosphere. HfO_2 based systems are today the leading candidates to become the next gate dielectric material for near future CMOS technology. Its favorable characteristics are well known: a high dielectric constant, low leakage characteristics and stability under annealing. We contrast the behavior of HfO_2 with that of CeO_2, a less widely studied oxide. It has also a high dielectric constant, ranging from ~ 15 for amorphous CeO_2 to ~ 26 for polycrystalline CeO_2; single-crystal ceria films grown on Si(111) have demonstrated dielectric constants as high as 52[4, 5]. This material is also chemically stable on silicon over a significant temperature range.

The formation of interfacial SiO_2 layers during high-κ film deposition is a critical issue that needs to be understood and controlled for the successful integration of these materials. Our results below demonstrate that the Hf based

system shows extensive oxygen exchange under oxygen annealing. We further demonstrate that this can be suppressed by mixing the oxide with SiO_2. Little SiO_2 interfacial growth was observed for the range of processing parameters under consideration here. The exchange reaction saturates with time and appears to be enhanced after film recrystallization. In contrast, Ce silicates exhibit rapid interface growth under similar conditions.

1.2. CRYSTALLINE OXIDES

An ordered oxide/semiconductor interface could have numerous advantages for many electronic applications. However, it is only relatively recently that, using molecular beam techniques, such films have been created. The properties of these films can be significantly influenced by defects (inhomogeneous phase formations, structural imperfections, etc.) at their interfaces. The nature of these imperfections is often not known because of the challenges in characterizing thin films on an atomic level.

Epitaxial oxides on semiconductors represent an entirely new class of materials with potentially revolutionary properties well beyond the high-κ CMOS field, and their basic physical properties are currently being explored by both experiment and theory. [6] High-quality epitaxial films grown on Si could offer better uniformity, lower defect density, and higher reliability than amorphous and polycrystalline ones. Aside from potential use as high-κ dielectrics, epitaxial films with the perovskite structure, such as $SrTiO_3$ and $BaTiO_3$, can be used as the intermediate or buffer layers for more complex heterostructure growth. Of high interest is their potential use in novel ferroelectric and spintronic devices. [7-10]

We have used MEIS to study composition and structure of thin (40 – 200 Å) epitaxial Sc_2O_3 and $SrTiO_3$ (STO) films grown by molecular beam epitaxy (MBE) on Si. [11] Our results show that the films have very good crystal quality. We find that the Sc_2O_3/Si interface is abrupt and free of mixed phases, as expected from thermodynamic calculations. The large lattice mismatch between Sc_2O_3 and Si, and the unique position of atoms at the interface, favor a 60° (or 180°) rotation of the film with respect to the substrate. For $SrTiO_3$/Si (001), where the interface is kinetically stabilized during the growth, the mobility of Ti and O species during re-crystallization anneal results in formation of compositionally different interfacial regions that are dependant on the re-crystallization temperature.

1.3. EXPERIMENTAL

MEIS can be thought of as a low-energy, high-resolution version of conventional Rutherford backscattering (RBS). Compared to RBS, a lower ion beam energy (100 keV in our case, compared to ~2 MeV in RBS) is used. This has two basic advantages. First, the electronic stopping power, dE/dx, for protons is larger in the MEIS region, which results in better depth resolution. Second, and more important, in the MEIS energy region an electrostatic ion energy analyzer can be used, instead of a surface barrier detector commonly used in RBS. The total energy resolution in our system is approximately 150 eV, which can be compared to ~ 12 keV in RBS. Our resulting depth resolution is approximately 3 Å in the surface region. Due to the broadening of the beam energy as the ions penetrate the target (straggling), the absolute resolution is only some 8 Å at a depth of ~ 40 Å, although average changes in depth, thickness and composition on a smaller scale, for example upon annealing, can be easily observed. De-convolution of the MEIS spectra provides quantitative information on the depth distribution of the elements in the film. By analyzing the angular distribution of the backscattered ions, one can draw conclusions about surface termination and film registry relative to the substrate. Our MEIS data were obtained in a double alignment geometry, with both detector and incident ion beam along (different) substrate crystallographic directions. This means that the detected silicon signal, aside from a small contribution from the substrate, is a measure of the number of Si atoms in the amorphous film.

The films studied in this paper were grown ex-situ. The STO films were made by MBE techniques at Penn State University, PA, [12] while the Sc_2O_3 films were made at National Tsing Hua University in Taiwan. [11] The HfO_2 films were deposited by Atomic Layer Deposition (ALD) at Sematech in Austin, TX and the CeO_2 films were grown in a separate vacuum chamber at Rutgers using Ce evaporation under controlled oxygen pressure. Further growth details will be given in forthcoming publications. Annealing and reoxidation in $^{18}O_2$ was performed in-situ at Rutgers. In some cases a mild anneal was used before analysis to eliminate surface contamination.

2. Results

2.1. AMORPHOUS OXIDES

2.1.1. *Hafnium oxide*

Fig. 1 shows MEIS results for HfO_2 films before and after reoxidation in ^{18}O at 500°C. The figure only shows the region of the Si and O signals. The Si signal occurs at a higher backscattering energy than the O one because of its higher atomic mass. (The Hf signal does not change under reoxidation and is therefore not shown.)

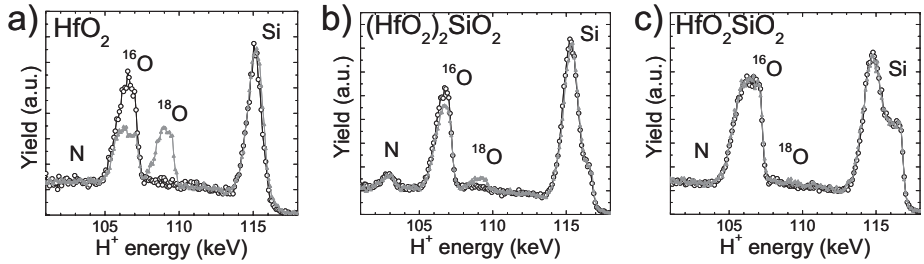


Figure 1. MEIS spectra of HfO_2 films on Si (100) before (open circles) and after reoxidation (closed symbols) at 500 °C. The spectra were obtained with 130.3 keV protons in a channeling and blocking configuration. The SiO_2 content is in a) 0%, in b) 33% and in c) 50%.

Reoxidation results in a broad and strong ^{18}O signal. The area under the ^{18}O peak is equal, within statistical error, after correction for the known backscattering cross sections, to the reduction in the ^{16}O signal. The silicon peak remains unchanged, indicating no increase in off-lattice-site (amorphous) silicon. These results show that there is a strong exchange of ^{16}O for ^{18}O, which, as the two peaks (^{16}O and ^{18}O) have the same width, extends over the entire thickness of the film. As there is no net oxygen increase and as the

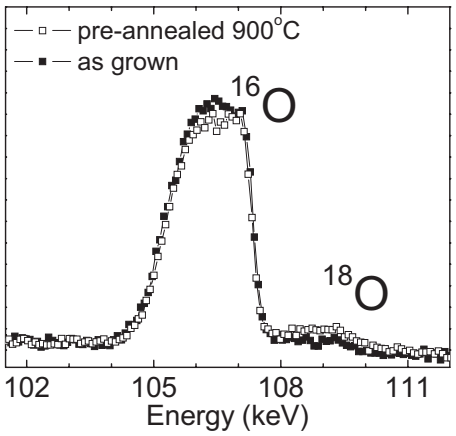


Figure 2. Results for HfO_2SiO_2 films after annealing in ^{18}O at 500 °C. The dark symbol curve is the result shown in Fig.1c, while the open symbol curve corresponds to the film annealed in vacuum to 900 °C prior to oxidation.

(amorphous) silicon content does not change, we conclude that there is no growth of SiO_2 at the interface. When SiO_2 is mixed in to an HfO_2 film during growth, we find that the exchange reaction slows down dramatically (Fig. 1, b), and is almost completely suppressed for a SiO_2 content of 50% (Fig. 1, c).

Under the conditions explored, we did not observe growth of additional interfacial SiO_2. This lack of ^{18}O exchange (Fig. 1, c) has interesting implications. Evidently, the existence of SiO_2 (or an SiO_2-like species) in the near surface region is enough to completely turn off the exchange reaction. The detailed mechanism responsible for this rather dramatic effect has yet to be understood.

If the mixed HfO_2/SiO_2 film is heated ≥ 900 °C in vacuum, it should recrystallize and phase segregate. [13] MEIS spectra for the crystallized film after re-oxidation (Fig. 2) shows slight ^{18}O uptake compared to almost complete suppression of the exchange reaction in as-grown films. One possibility is that some grain boundaries develop at the vacuum – solid interface which facilitate the ^{18}O transport and uptake. On the other hand, nitrogen incorporation in the HfO_2/SiO_2 film (not shown) results in a decreased ^{18}O uptake (less film reactivity). Nitride barrier layers are used to slow O, Si and dopant diffusion, as well as silicate formation and other interface reactions. Another beneficial aspect is that nitridation also raises the crystallization temperature.

2.1.2. *Ce oxide*

The close CeO_2-Si lattice match and relatively high thermal stability makes it a good candidate material for heteroepitaxial growth of single-crystal films or for a buffer layer in a gate stack. In particular, CeO_2(100)-oriented films may be considered for use as a buffer-layer between perovskite structures and silicon, [14, 15] and (111)-oriented films as a buffer layer in metal ferroelectric insulator semiconductor structures (MFIS). [16] The

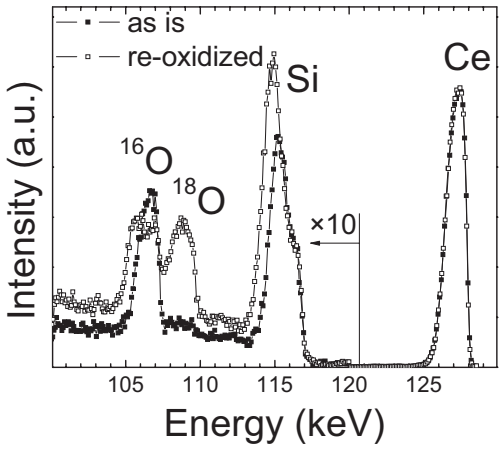


Figure 3. MEIS spectra of a Ce silicate film before and after reoxidation at 10^{-2} Torr $^{18}O_2$, 500°C for 15 min. The proton energy was 130.75 keV and the scattering angle 125.3°.

presence of two cerium valence states, Ce^{3+} and Ce^{4+}, brings an additional complication (or opportunity). Hirschauer et al. report a complex cerium oxide film containing silicon oxide, a mixed Ce:Si:O layer, and at least two cerium oxide phases resulting from depositing CeO_2 over Si(111). [17] In addition, the behavior of $(CeO_x)_n(SiO_2)_m$/Si interfaces during annealing, particularly the mechanisms of oxidation and reduction for silicon in contact with cerium as well as the evolution of the film composition, are not well understood.[17, 18]

Compared to the Hf case, the effects of oxygen annealing are dramatically different for Ce silicate films (Fig. 3). An inspection of the peak widths in the spectrum before reoxidation shows that the depth distributions are consistent with those expected for a predominantly uniform cerium silicate, with a thin (≤ 3 Å) interfacial SiO_2 layer. After ^{18}O reoxidation, we find again significant oxygen exchange, but this is less pronounced than in the Hf case (Fig. 1, a) above. There is also a very significant increase in the total oxygen content. Furthermore, the width of the ^{16}O peak increases, which implies that some ^{16}O species move further away from the surface. Finally, the Si peak area also becomes larger, while the Ce peak does not change. These observations together imply growth of an interfacial SiO_2 layer below the silicate. The SiO_2 thickness can be easily estimated either from the Si and O peak width increase (assuming a proton stopping power in SiO_2 matrix of 11.6 eV/Å), or from the increase of the Si and total (^{16}O + ^{18}O) oxygen peak areas (assuming a SiO_2 density of 2.19 g/cm^3). Both methods show the formation of a 14-16 Å thick SiO_2 interface, confirmed by explicitly fitting the spectra. The measured ratio of the visible Si increase to that of O is of 1:2.13, very close to the stoichiometry ratio.

From these results we conclude that the overall oxygen incorporation in the film is primarily due to the interface reaction with Si, while the reaction in the bulk of the ceria film is limited to the substitution of network ^{16}O by ^{18}O, arriving from the gas phase. The large growth rate of interfacial SiO_2 in the case of cerium-based films can be explained by the well-known fact that Ce presence readily promotes Si oxidation by reduction of Ce^{4+} to the Ce^{3+} state, and concurrent formation of a Ce silicate. Ce^{4+} can be re-formed from Ce^{3+} in the silicate by reaction with oxygen from the gas phase. A detailed analysis shows that the interfacial SiO_2 layer grown during re-oxidation is mostly formed by the ^{16}O isotope initially present in the film. This could not be realized if oxygen from the gas phase was able to migrate directly to the interface via interstitial diffusion; our data imply that the oxygen is instead transported across the film by an exchange mechanism with network oxygen in the silicate.

Preliminary AFM measurements indicate that as deposited our films are flat with an RMS roughness of 1.5-2.2 Å, and remain flat upon annealing up to

850°C. Above this temperature, oxygen leaves the films, which break up to form cerium silicide, with an RMS roughness of 10 nm or larger.

2.2. CRYSTALLINE OXIDES

2.2.1. *$SrTiO_3$*

$SrTiO_3$ has a cubic perovskite–type structure with a lattice parameter of 3.908Å. An epitaxial relationship $(100)_{Si} \parallel (100)_{STO}$ and $[001]_{Si} \parallel [011]_{STO}$ is observed during STO growth on Si with a small lattice mismatch between two materials (a_{Si} = 5.409 Å; $a_{Si}/\sqrt{2}$ = 3.842 Å). Due to reactivity between the $SrTiO_3$ film and the Si substrate, the nature of the $SrTiO_3$/Si (100) interface and structural

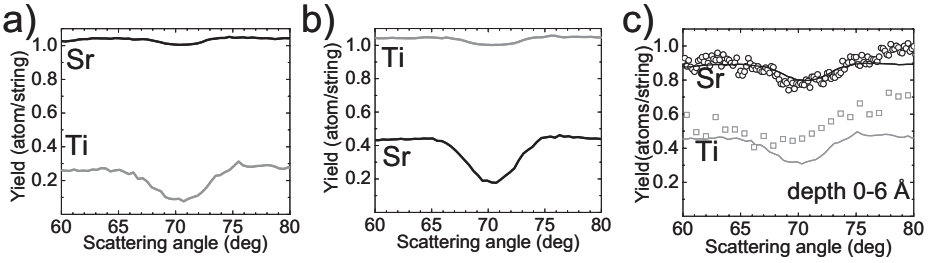


Figure 4. Angular distributions of the backscattered ions corresponding to Sr and Ti peak integrated intensities. Simulations curves are shown for SrO terminated film in a) and TiO_2 terminated in (b), whereas experimental results with the best fit simulated data are presented in c).

defects in $SrTiO_3$ thin film become critical to the structural and chemical integrity of devices and their electrical performance. Our MEIS data give direct information about the composition of the sample, top surface termination and STO/Si interface.

Perovskite $SrTiO_3$ structures can be considered as alternating SrO and TiO_2 layers. MEIS measurements in the (110)$SrTiO_3$ scattering plane allows one to determine top surface termination. If the incident beam is aligned in the [111]$SrTiO_3$ direction (54.74° off the normal) and the detector is positioned along the [1$\underline{11}$] axis, two distinct situations are possible. If the top surface is a SrO layer (SrO termination), every Ti atom in the second layer will be in the shadow cone of Sr atom and the measured Ti yield will be much smaller than that of Sr. Simulated angular distributions for Sr and Ti assuming SrO termination are shown in Fig. 4, a. The other alternative is TiO_2 termination, where every Sr atom is shadowed by a Ti atom. The simulated ion yields for this case are presented in Fig. 4, b. Also shown are modeling calculations for the ion scattering spectra, assuming ~80% SrO and 20% TiO_2 termination (Fig.

4, c) which gives the best fit to the experimental data. Clearly, the surface is predominately SrO terminated.

In Fig. 5 we show a complete spectrum of the film discussed above. As we are using a channeling and blocking configuration, we should not detect subsurface atoms that are in their equilibrium lattice positions. All atoms in amorphous regions should be visible to the ion beam. This results in highly simplified spectra where the scattering from interface species is clearly separated from scattering at the surface. Well-resolved peaks are observed corresponding to surface Sr, Ti, and O (as well as some carbon impurities), showing the excellent crystalline nature of the film. Two additional peaks are also observed, at ~ 87 keV (corresponding to Ti at the interface) and ~ 76.5 keV (interfacial O). Clearly, the dominant metal atom in the interface region is Ti. At first glance this is a surprising result as the initial deposition of a small number of Sr atoms on top of the Si substrate is said to be a crucial step in the creation of the epitaxial film. [7, 12] Quantitatively, the spectrum in Fig. 5 can be modeled by a ~ 78 Å crystalline film on top of a ~ 2 Å SrO layer, a ~ 7 Å $TiSi_xO_y$ layer and a $TiSi_x$ layer or islands extended deeper into bulk Si. Studies of the angular dependence of the ion backscattering yield (not presented here) show that the interfacial layer is crystalline.

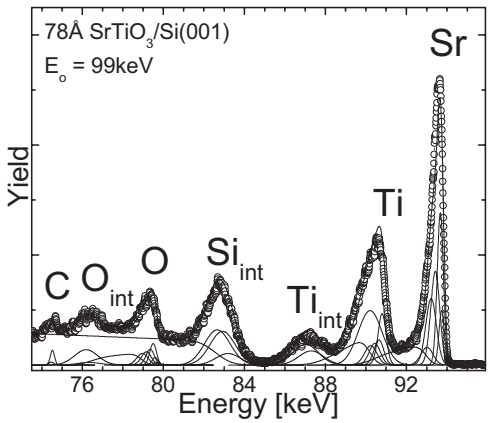


Figure 5. Ion scattering spectrum from a 78 Å epitaxial film of $SrTiO_3$ on Si (001). A fit is shown by the solid line with the peak deconvolutions (thin lines) for each element with a Ti-rich interface composition of $SrTiO_3/SrO/TiSi_xO_y/TiSi_2/Si$ (001).

Control over the interfacial region composition can be achieved by carefully varying re-crystallization temperature during the growth. Ion scattering data for the film re-crystallized at 400°C show a much narrower Ti peak, indicating that Ti is not moving deeper towards the substrate, and the interface composition can be modeled as a $SrSi_xO_y$ crystalline layer.

2.2.2. *Sc_2O_3*

Sc_2O_3 is a potentially very useful dielectric material with a relatively high dielectric constant (~ 14) and a large bandgap. It is thermodynamically stable on silicon and can be used to passivate GaN. Recently, very high quality

epitaxial films of Sc_2O_3 have been grown on Si (111) and on sapphire. These films have the bulk bixbyite cubic phase with a sharp interface with Si.

Figure 6 shows a MEIS backscattering energy spectrum for an uncapped Sc_2O_3 film exposed to air prior to analysis. The measurement was done in a double

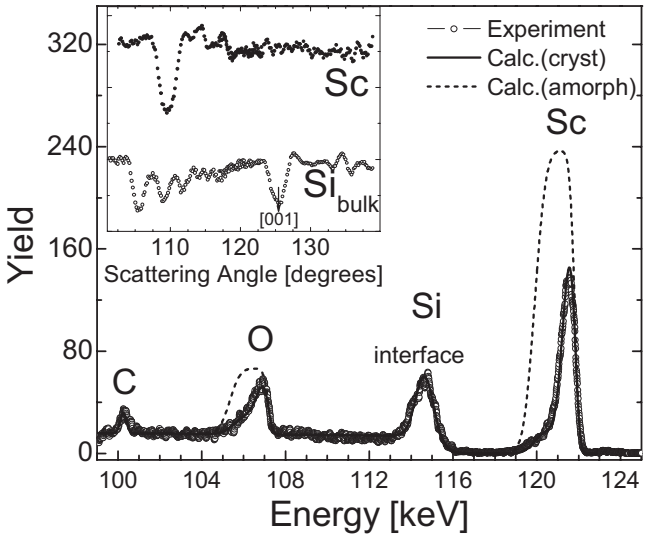


Figure 6. Results from an epitaxial Sc_2O_3 film on Si(111). The dotted line is the calculated result for an amorphous sample. The insert shows the angular distribution of the ion scattering yield for Sc, compared to the bulk Si data.

alignment geometry with the Si substrate. Observation of distinct blocking minima in Sc signal, shown in the insert in Fig. 6, and comparison of the Sc signal just below the surface Sc peak to a calculated yield for the same thickness amorphous film (the dashed line in Fig. 6) indicate very good crystalline quality. No interfacial Sc and O peaks are observed, indicating a highly ordered Sc_2O_3 lattice structure at the interface with Si. The small additional visibility of Si atoms at the interface (compared to an ideal, bulk terminated lattice) suggests good crystallinity of the interface with possibly some minor deformation of or defect formation in the Si lattice.

The angular distribution of the Sc yield shows no evident minima when the detector is aligned with the Si substrate blocking position. Instead a strong Sc blocking minimum is observed at 110°. The position of this minimum can be assigned according to the stereographic projection of the (111) faced cubic crystal and corresponds to the [111] blocking direction in the [211] scattering

plane. This provides evidence for a 60° rotation of the Sc_2O_3 film relatively to a substrate. In terms of atomic structure, neither the (111) bulk terminated surface structures of Sc_2O_3 bixbyite nor the substrate Si(111) non-reconstructed surface is symmetric under a 60° rotation about the center. In the bixbyite case, oxygen atoms octahedrally coordinating scandium cations strongly define a 3-fold rotational symmetry about the origin. In the silicon case, even though the top layer of atoms exhibits a 6-fold symmetry, this gets reduced to 3-fold rotational symmetry when the second layer of atoms is taken into account.

Cubic Sc_2O_3 and Si have significantly different crystal structures, bonding, and lattice constants. The bulk lattice constants of Si (5.43 Å) and Sc_2O_3 (9.86 Å) are mismatched by 9.2 % (relative to the $2a_{Si}$). It is intriguing that a highly ordered epitaxial growth was obtained with this unusually large mismatch. HRTEM will be needed to understand the dislocation network that should be present at the interface.

Acknowledgements

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INTERFACE FORMATION DURING EPITAXIAL GROWTH OF BINARY METAL OXIDES ON SILICON

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Abstract. The Si/dielectric interface properties influence the device performance significantly. Often the interface is not stable and changes during and after the growth. For a better understanding of the interface and layer formation processes, well-defined experimental studies were performed under ultra-clean ultra-high vacuum conditions. Molecular beam epitaxy in combination with real time reflection high-energy electron diffraction is here the most advantageous method because of its ability to monitor the formation of structures under ultra-high vacuum in situ within a wide range of different conditions. When combined with methods analyzing the bonding properties without leaving the vacuum, this approach results in a rather detailed insight into the interface formation and properties. Here, we will present results of the interface and film formation during epitaxial growth of Nd_2O_3 on silicon.

Keywords: high-κ dielectrics, molecular beam epitaxy, lanthanide oxide, interface formation

1. Introduction

The common approach for alternative high-κ gate dielectrics has involved amorphous materials with higher dielectric constants, such as metal oxides and

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their silicates. In general, attempts have been made to keep these materials amorphous, in particular, after post-deposition high temperature processing in order to avoid increased surface roughness and additional leakage due to the formation of grain boundaries.[1]

The Si/dielectric interface properties influence the device performance significantly. Often the interface is not stable and changes during and after the growth. The formation of SiO_2 and/or metal silicate interfacial layers can occur when these materials are deposited upon silicon.[2] Further growth of silicon dioxide or a silicate takes place during subsequent annealing, which is usually found to be necessary to reduce leakage currents. It is important to note, however, that using an interfacial layer of SiO_2 or another low permittivity material, will limit the highest possible gate stack capacitance, or equivalently, the lowest achievable *equivalent oxide thickness (EOT)* value. For a better understanding of the interface and layer formation processes, well-defined experimental studies are needed which are performed under ultra-clean ultra-high vacuum conditions.

A good interface requires either that the oxide is amorphous, or that it is epitaxial and lattice-matched to the underlying silicon. Amorphous dielectrics are expected to be able to adjust the local bonding to minimize the number of Si dangling bonds at the interface. The alternative is to use an epitaxial oxide. This involves more effort, but it has the advantage of enabling defined interfaces engineering. Molecular beam epitaxy (MBE), known for its superior capability in atomic level engineering and interface control, has been used in the epitaxial growth of various high-κ materials. MBE in combination with real time reflection high-energy electron diffraction (RHEED) is here the most advantageous method because of its ability to monitor the formation of structures under ultra-high vacuum *in situ* within a wide range of different conditions. When combined with methods analyzing the bonding properties, like x-ray photoelectron spectroscopy (XPS), this approach results in a rather detailed insight into the interface formation and properties.

Generally, there are two groups of possible candidates for epitaxial growth on Si, namely (a) perovskite-type structures and (b) binary metal oxides. Various perovskite-type metal oxides (ABO_3), in particular, have become a technologically important class of materials due to their unique dielectric, piezoelectric, ferroelectric, ferromagnetic, optical, electro-optic, and catalytic properties. These perovskite oxides cover a wide range of materials from insulators to conductors and superconductors, and everything in between. It is extremely important and desirable to integrate these highly functional metal oxides into mature semiconductor technologies. Successful heteroepitaxy of these metal oxides on semiconductors such as Si opens the door to a wide range of novel device technologies with enhanced functionality and flexibility.

2. Epitaxial Metal Oxides on Silicon

Here, we will focus on the epitaxial growth of binary metal oxides. Epitaxial growth on a clean surface requires matching in symmetry as well as in atomic spacing. Lanthanide oxides (LnO's) form the most interesting group for epitaxial growth on silicon. The LnO's can have different oxygen compositions LnO_x, with x ranging from 1 to 2 due to the multiple oxidation states (+2, +3, and +4) of the rare-earth metals. This leads to oxides with different stoichiometries (LnO, Ln_2O_3, LnO_2,). All known Ln (II) oxides, like EuO, are not insulating[3]. Therefore, they will not be considered here any further.

Different oxygen content can lead to different structural phases including two cubic phases, such as the calcium fluoride (CaF_2) structure for the Ln(IV) only, and the manganese oxide (Mn_2O_3) or *bixbyite* structure for Ln(III). The *bixbyite* structure is based on the calcium fluorite structure, where 1/4 of the oxygen atoms have been removed from specific lattice sites. Some LnO's also crystallize in the hexagonal lanthanum oxide structure, which is suitable for epitaxy only on Si(111). Also, monoclinic phases are known for various lanthanide oxides[3]. Both, the calcium fluoride and the *bixbyite* structure, have lattice symmetry suitable for epitaxial growth on Si(100) and Si(111). Commonly, the oxides are evaluated on the basis of lattice matching, with the misfit defined as the relative difference in the lattice constants (a_{film} and a_{Si}). Figure 1 summarizes the lattice mismatch for all cubic lanthanide (III) oxides relative to silicon and germanium substrates, respectively.

Taken alone, this is misleading, because the lattice is made up of metal atoms occupying the positions of a face-centered cubic (*fcc*) lattice with a lattice constant a_{film}, where the tetrahedral holes are occupied by oxygen atoms. Therefore, the lattice mismatch would be identical for all three epitaxial relationships, i.e. (100)//(100), (110)//(110), and (111)//(111). All other combinations violate symmetry matching. However, the growth of LnO's is based on the deposition of metal oxide molecules. Due to the existence of highly ionic Ln—O bonds in combination with the high bonding strength of the covalent Si—O bonds, we can assume that the interface is predominantly formed by Si—O—Ln bonds. Therefore, the matching of the oxygen atoms is the important parameter.

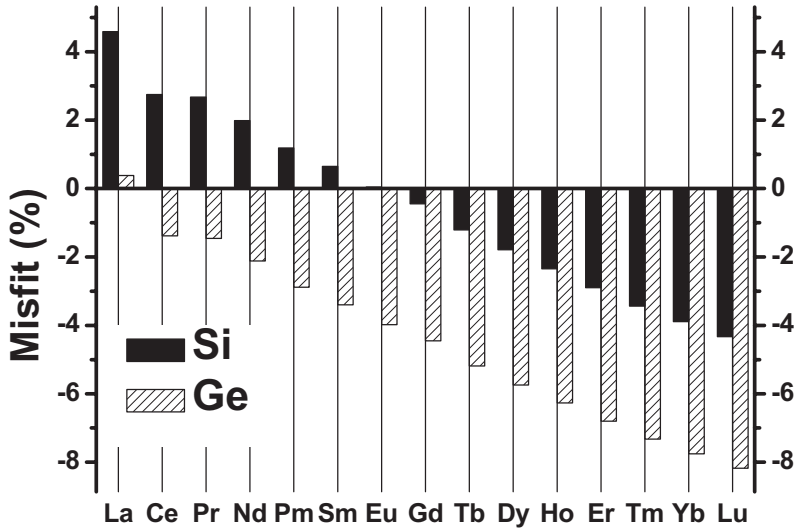


Figure 1. Lattice mismatch of different lanthanide oxides relative to silicon and germanium (lattice constants from Ref. 3).

The complete crystallographic structure can also be described by two non-identical metal and oxygen lattices, respectively. The arrangement of the oxygen atoms forms a simple cubic lattice with a lattice constant of $a_{film}/2$. Thus, the interesting matching condition (Figure 2) for epitaxial growth is the $LnO_2(110)[-110]//Si(001)[010]$ relation. In that case, nearly 1:1 matching should occur along one direction. In the other direction, there would be roughly a 3:2 matching relation. Layers grown in this orientation exhibit mostly two types of (110)-oriented domains, with two orthogonal in-plane orientations (found experimentally for a large variety of binary metal oxides on Si(001)). Due to the 45° rotation of the (110) plane relative to the substrate, the mismatch for the 1:1 matching is identical to that one shown in Figure 2. For the calcium fluorite structure (LnO_2), however, the 3:2 relation leads to unsaturated oxygen bonds that would create additional interface charges. Therefore, $Ln_2O_3(110)//Si(001)$ heterostructures (with the metal oxide having the *bixbyite* structure) are favorable due to the lower oxygen content in that structure.

On germanium however, it seems to be possible to find dedicated conditions for the epitaxial growth of ultrathin CeO_2 layers - even in the (100) orientation.[4]

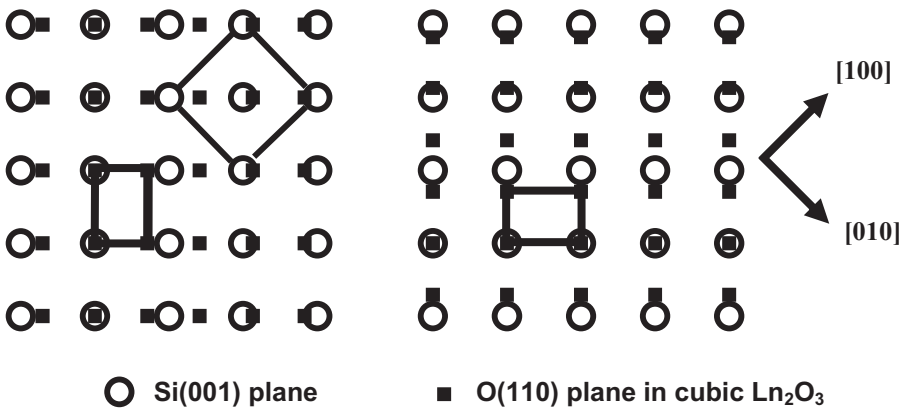


Figure 2. Ln_2O_3(110)//Si(001) alignment (schematically): 1:1 matching occurs along one direction. In the other direction, there is roughly a 3:2 matching relation. Two types of (110)-oriented domains are possible, with two orthogonal in-plane orientations.

For application in a Si-based device fabrication process, all lanthanide oxides exhibiting more than one valence state (+3 and +4) are not the best choice as epitaxial high-κ materials because of the coexistence of phases with different oxygen content. For example, cerium(IV) oxide (CeO_2) can release oxygen under reduction conditions forming a series of reduced oxides with stoichiometric cerium(III) oxide (Ce_2O_3) as an end product, which in its turn easily takes up oxygen under oxidizing conditions, turning the cerium(III) oxide back into CeO_2. This reversible transition has been studied in a number of theoretical works. In Ref. 5, the authors show how the oxygen-vacancy formation process is facilitated in a most essential way by a simultaneous capture of two electrons into the localized *f*-level traps on two cerium atoms, which therefore change their valence from +4 to +3. In addition, stable mixed valence-state structures can occur for some LnO's. For example, Pr_6O_{11} is the most stable phase for praseodymium oxide.[3]

All lanthanide oxides displaying only one valence state are easier to handle due to the absence of transitions between phases with different oxygen content. Based on that argument, we will focus our discussion mainly on lanthanide (III) oxides (occurring as Ln_2O_3).

3. Results for the Growth of Different Rare-Earth Oxides on Silicon

3.1. EXPERIMENTAL

In the following, we will compare results for the MBE growth of three LnO's, namely Pr_2O_3, Nd_2O_3, and Gd_2O_3. All experiments were performed in a multi-chamber ultrahigh-vacuum system (*DCA Instruments*) capable to handle 8" wafer. This system includes a growth, an annealing, and an analysis chamber connected by an ultra-high vacuum (UHV) transfer system. The layers were grown on Si(001) and Si(111) substrates. Substrates were cleaned *ex situ* using as the last step diluted HF etch ($HF:H_2O = 1:10$) followed by a dilution rinse, and then were immediately inserted into the vacuum system. Substrates were annealed *in situ* to transforms the initial hydrogen-terminated (1×1) surface structure into the (2×1) superstructure indicating a clean and well-ordered surface. Commercially available, granular Ln_2O_3 material was evaporated using an electron-beam evaporator. Growth temperatures were in the range 800-1000 K. Typical growth rates were 0.05 – 0.01 nm/s. For some growth experiments, additional oxygen was inserted in the chamber without any activation to yield an oxygen partial pressure of around 10^{-7} mbar. The surface and layer structure was evaluated during the growth by RHEED.

After growth, the wafers were transferred into the XPS analysis chamber without leaving the UHV. Non-monochromatized Al Kα radiation ($h\nu = 1486.6$ eV) was used for the excitation of photoelectrons. All measured wafers were electrically grounded to eliminate charging effects during long-time measurements. To minimize experimental uncertainties associated with energy variations caused by spectrometer instabilities and to improve the signal to noise ratio, the XPS data were collected by repeatedly scanning the silicon, the lanthanide, and the oxygen level. A multipeak Gaussian deconvolution procedure was used to extract the exact line position and intensities.

The layer thickness was measured *ex vacuo* by X-ray reflectivity (XRR) using a standard single crystal diffractometer with graphite monochromator in front of the detector. Layers were also characterized by X-ray diffraction (XRD) (θ/2θ, ω and Φ-scans) and transmission electron microscopy (TEM), i.e., high resolution cross-section and plan-view images combined with selected area diffraction (SAD).

3.2. EPITAXIAL GROWTH ON Si(100)

Recently, we reported results using MBE growth of crystalline praseodymium oxide (as Pr_2O_3 in the *bixbyite* structure) on Si(001) substrates[6,7]. As predicted, the Pr_2O_3 was found to grow as (110)-single-crystalline domains, with two

orthogonal in-plane orientations[6]. Also for the other two LnO's, we found the same crystalline orientation and domain formation. RHEED observations during growth indicate smooth layer-by-layer growth only to a limited thickness (~ 10 nm) for all three materials. For thicker layers, we observe a transition to 3-dimensional growth.

Different investigations indicate that the occurrence of the two orthogonal domains is due to the nucleation on neighboring terraces with Si dimer rows (2x1 reconstruction) perpendicular to each other[8]. Thus, the orientation of the domains correlates with monoatomic surface steps. Domains with different orientations can nearly be prevented with the use of vicinal substrates of 4° miscut. Such a miscut surface exposes surface steps of double atomic layers, thus giving Si terraces of ~8 nm spacing with the same dimer orientation. Single domain Gd_2O_3 films have been realized on vicinal substrates[9].

3.3. EPITAXIAL GROWTH ON Si(111)

On Si(111), we obtained perfect epitaxial growth of hexagonal Pr_2O_3.[10] We also found that a phase transition takes place during the annealing in N_2 of the as-grown layers below growth temperature. Annealed films display a cubic structure isomorphic to manganese oxide, (111)-oriented but 180° rotated (orientation "B") about the Si (111) surface normal ("A"). For Gd_2O_3, no hexagonal structure is known. Nd_2O_3 and Gd_2O_3 already grow in the cubic structure. In addition, Ln_2O_3 layer grown on Si(111) can be epitaxially overgrown with silicon. We found the typical "ABA" orientation of an epitaxial $Si/Nd_2O_3/Si(111)$ stack.

The successfully demonstrated heteroepitaxy of such stacks opens the door to a wide range of novel device technologies with enhanced functionality and flexibility, like novel tunneling devices.

4. Interface Stability

We applied RHEED and XPS to investigate the $Ln_2O_3/Si(001)$ interface and film formation during epitaxial growth. The growth process was interrupted several times to transfer the wafer into an XPS analysis chamber without leaving the UHV environment. Using such an approach, we investigated different Ln_2O_3 layers grown on Si(001). Here, we will show the typical behavior for Nd_2O_3; the main results hold in principle also for the other Ln_2O_3 layers.

First, RHEED investigations were performed under usually MBE conditions, i.e. oxygen partial pressure below $5x10^{-8}$ mbar.[11] They indicate that

the (2x1) reconstructed Si(001) surface changes gradually to an unreconstructed (1x1) surface during the initial deposition stage of Nd_2O_3. Further deposition leads to additional RHEED spots appearing in 1/3 positions between the main (0,1) spots in the zero-order Laue-zone corresponding to an 3-fold periodicity at the surface. Further deposition changes the surface structure again to (1x1) before bulk spots related to oxide island diffraction appear.

Accompanying investigations were performed by XPS without leaving the UHV environment. Figure 3 summarizes the XPS results for the Si-2p core-level spectrum for layers with different thicknesses. For layers with a thickness below 1 nm we found that Si exhibits mainly a peak corresponding to elemental Si (Si^0 state) However, the spectra show significant broadening to the low energy side (in particular visible in the second spectrum), indicating the appearance of a Si^{1-} bonding state due to silicide formation. The relatively small shift points to an $NdSi_2$ phase formation[12]. Spectra for layers with thickness above 1 nm exhibit an additional peak at higher binding energies, but still lower than expected for SiO_2 formation. We attribute this peak to a silicate-like bonding[13].

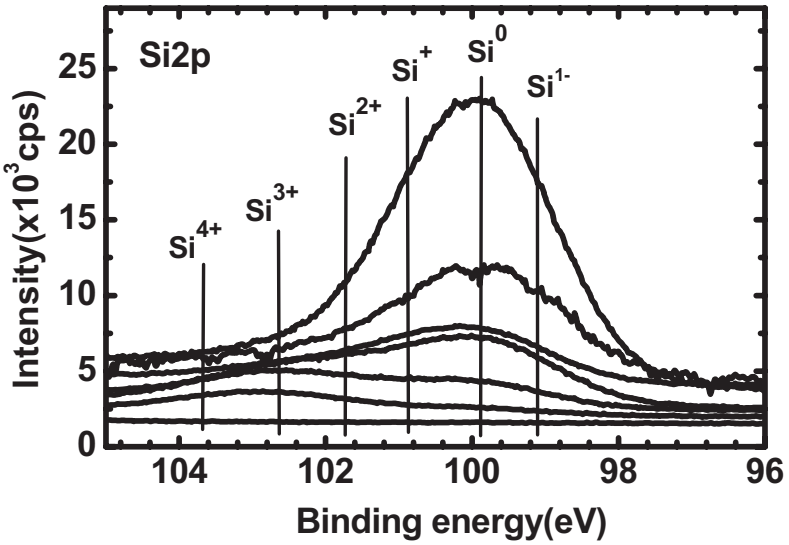


Figure 3. Si 2p core-level XPS spectra for Nd_2O_3 layers of various thicknesses. The layer thickness increases stepwise from ~ 0.5 nm (upper spectra) to 3 nm (layer #6). The lowest spectrum was taken for a 6 nm thick layer. Straight lines indicate the different Si bonding states.

The deconvolution of the individual spectra by a Gaussian fit indicates silicide-like and suboxide-like bonds in the initial stage of growth. Thereby the

number of silicide-like bonds increases compared to the number of suboxide-like bonds with increasing layer thickness. After the next growth step, silicate-like bonds are formed. There is still no indication of SiO_2 formation. Spectra obtained after further deposition can be explained by the appearance of a higher-energy (oxygen-rich environment) and a lower-energy (less oxygen) Si bonding state in a silicate-like bonding configuration. Thereby, the number of states in oxygen-rich environment increases with layer thickness. Such different bonding configurations can appear in different kind of silicates. Ln_2SiO_5, for example, contains one oxygen atom only in a Ln-O-Ln configuration, whereas $Ln_2Si_2O_7$ contains one oxygen atom only in a Si-O-Si configuration giving rise to different ratios in Si bonding states and, therefore, also to a shift in the measured 2p bonding energy[14].

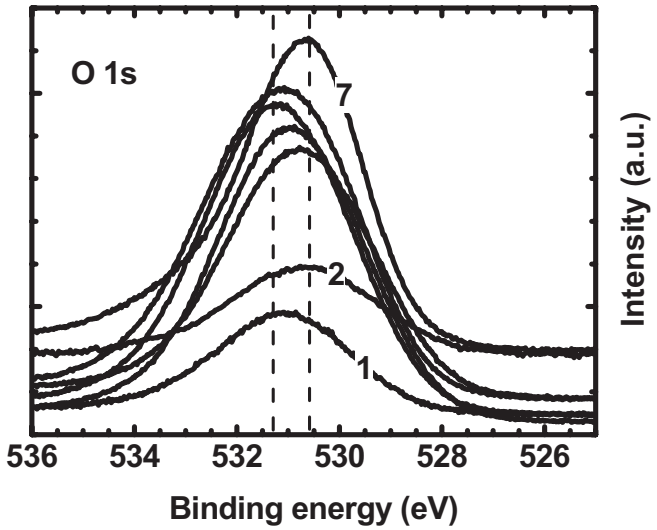


Figure 4. Oxygen 1s core-level XPS spectra of stepwise grown Nd_2O_3 layers on Si(001). The thickness increases stepwise from 0.5 nm (#1) to 3 nm (#6). Layer #7 was 6 nm thick. The lines indicate the appropriate binding energy for oxygen in silicates (531.3 eV) and Nd_2O_3 (530.6 eV).

The oxygen O 1s core-level spectra are summarized in Figure 4. We observe a low energy shift of the O1s peak after the second deposition step to a position almost identical to that of the final thick Nd_2O_3 layer. Thus, mainly Nd-O bonds seem to exist in an about 1 nm thick layer, supporting the assumption that in the initial stage of growth, silicon is mainly bound to neodymium (silicide-like bonding). Detailed deconvolutions of the individual spectra yield that the number of Nd-O bonds increases for the second layer. During further growth,

the number of silicate-like bonds increases initially, visible also by the shift of the O1s signals to higher energies, before the peak originating from Nd-O-Nd bondings in Nd_2O_3 becomes dominating. The corresponding neodymium 3d 5/2 core level spectra support this picture. For the second layer, we observe a shift to lower binding energies, as should be expected if the bonding becomes metal-like. That behavior together with the observed shifts in the Si spectra can only be explained by an exchange of oxygen bound to silicon by neodymium or by a movement of oxygen atoms from a Si-O-Nd interface site into the layer during the initial stage of growth.

In the initial stage of growth, we observe the formation of a silicide-like interface, exhibiting a threefold periodicity. Recently, the appearance of additional 1/3 order reflections in the RHEED pattern during Sr deposition on Si(001) has been explained by a reconstruction of the (2x1) Si surface structure into a silicide-like surface structure[15]. McKee *et al* [16] showed that such a silicide layer on top of Si(001) leads to a crystalline oxide interface commensurate for epitaxial oxide growth. In this way, epitaxial $SrTiO_3$ layers have been grown in (001) orientation on Si(001)[16]. However, Sr exhibits only a 2+ oxidation state, what is different to the Ln-metals, like Nd. Silicide overlayers in case of a 3+ oxidation state can also give rise to a series of submonolayer ordered structures which are commensurate with silicon[17]. However, the structure of such reconstructions on Si(001) is quite different to the case of the 2+ oxidation state, where similar periodicities appear. This could be the reason why epitaxial growth of Ln_2O_3 occurs in (110) orientation, although a similar periodicity was observed in RHEED.

In case of Ln_2O_3 growth, the formation and stability of the silicide-like phase depends on the oxygen chemical potential[18]. Considering the low oxygen partial pressure under UHV conditions (as used in MBE growth), the chemical potential of oxygen can become negative. Thus, silicide formation will be favorable compared to oxide formation.

That is one of the most crucial points for the growth of dielectric layers, because the silicide growth can continue as long as the oxygen content remains low enough or the oxygen chemical potential remains strongly negative. This occurs even faster at a surface or interface region where the energetical equilibrium is out of order, for example, due to stress. TEM micrographs of a Nd_2O_3/Si(001) system layer grown under UHV conditions support this assumption.[11] At the cross-sectional micrograph, we clearly find crystalline inclusions with the interface extending some nanometers into the Si substrates. Moreover, voids were found in such layers. In addition, the plan-view micrograph shows typical Moire fringes originating from these inclusions. Based on a detailed evaluation of the TEM results, we could identify the crystallographic structure of these inclusions to be identical to the known

structure of tetragonal $NdSi_2$. After annealing in an oxygen-rich atmosphere, the silicide inclusions disappear, however, and an amorphous interfacial layer and regions within the layer appear.

These observations are similar to recent results for growth and annealing experiments of HfO_2 and Al_2O_3 layers on Si grown under UHV or oxygen-poor conditions[19].

The appearance of silicide inclusions and the possibility for void formation seem to be a serious drawback for a lot of possible material candidates for future high-κ applications. For the epitaxial growth of Ln_2O_3 oxides, a well controlled interface and subsequent growth engineering is necessary to reach the required electrical properties. This can easily be realized by using modified MBE growth processes. We found, that MBE growth under defined oxygen partial pressures during the interface formation and/or during the subsequent growth can prevent any kind of silicide inclusions and void formation. Layers grown by such a step-controlled MBE process display a sufficiently high-κ value to achieve very thin *EOT* values, combined with ultra-low leakage current densities, good reliability, and high electrical breakdown voltage. This makes epitaxial Ln_2O_3 layers excellent candidates for application as very thin high-κ materials.

5. Outlook

One interesting approach for high-κ materials is based on the development of epitaxial metal oxides grown directly on silicon surfaces. Here we presented results for MBE-grown lanthanide oxides with the Ln_2O_3 composition in the cubic *bixbyte* structure. MBE is known for its superior capability in atomic level engineering and interface control, and is one of the techniques being investigated for the epitaxial growth of various high-κ materials. The development of suitable epitaxial high-κ materials requires a detailed understanding of all processes during interface formation and subsequent growth. Based on this understanding, the whole growth procedure has to be adapted accordingly.

Acknowledgement

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EFFECT OF CHEMICAL ENVIRONMENT AND STRAIN ON OXYGEN VACANCY FORMATION ENERGIES AT SILICON-SILICON OXIDE INTERFACES

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Abstract. Silicon oxide layers formed between silicon substrates and oxides with large dielectric constants (high k) play an important role in determining electrical properties for microelectronic applications such as gates stacks and capacitors. In particular, interfacial layers set limits on the equivalent oxide thickness (EOT) for high k oxides formed on silicon. For sub-nanometer interfacial layers, an amorphous, non-stoichiometric oxide forms; an increase in the dielectric constant relative to SiO_2 in this layer has been inferred from experiment and theoretically predicted. Formation of oxygen vacancies within interfacial layers further reduces the oxygen content and acts to increase the dielectric constant. In this work, the energetics of oxygen vacancy formation at silicon/oxide interfaces is investigated and it is shown that oxygen vacancy formation is energetically more favorable in non-stoichiometric SiO_x than in SiO_2, implying a higher density of oxygen vacancies within interfacial layers.

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Keywords: oxygen vacancies, interfacial layers, dielectrics

1. Introduction

High-k dielectrics are targeted for the 45 nanometer CMOS technology node to meet transistor scaling requirements. Hf-based oxides demonstrate promising characteristics as high-k gate dielectrics, but their integration into silicon fabrication processes continues to face obstacles. Investigation of the local band offsets at the interface, equivalent oxide thickness (EOT), and carrier mobility at the oxide/semiconductor interface have been undertaken to determine the suitability of various high k oxide candidates.

An amorphous interfacial oxide layer in the physical thickness range of 0.6-1.1 nm forms for high k materials on silicon, and this thin mixing layer is an important component for the determination of the oxide/semiconductor interfacial electrical properties. The SiO_x layer formed was feared to limit the gate stack scaling, but there are experimental and theoretical indications that the dielectric constant of the interfacial layer is higher than for stoichiometric SiO_2[1-4], and it has been suggested that the permittivity is associated with oxygen deficiency in the interfacial layer [2,4]. The energetics of oxygen vacancy formation in a thin SiO_x layer on Si(001) are computed by ab initio methods to investigate possible mechanisms for oxygen deficiency at high k/silicon interfaces.

Previously it has been shown by density functional (DFT) calculations and correlated quantum chemistry methods that oxygen vacancy formation (V_O) near the silicon substrate is favored over V_O formation in bulk silica[5], and consequently is favored over V_O formation in hafnia[6]. In this study, strain at the Si/SiO_x interface is considered for a set of interface models[7,8] for which external strains are applied, and as well completely relaxed simulation cells are considered. The chemistry of oxygen vacancy formation is also considered by computing the formation energies for neutral, singlet V_O sites for all possible formal charge states of the silicon atoms situated about an oxygen vacancy. A consistent picture emerges whereby these oxygen vacancies are stabilized at the interface region due primarily to the local chemical environment, with strain playing only a secondary role in formation energies.

2. Computational Details

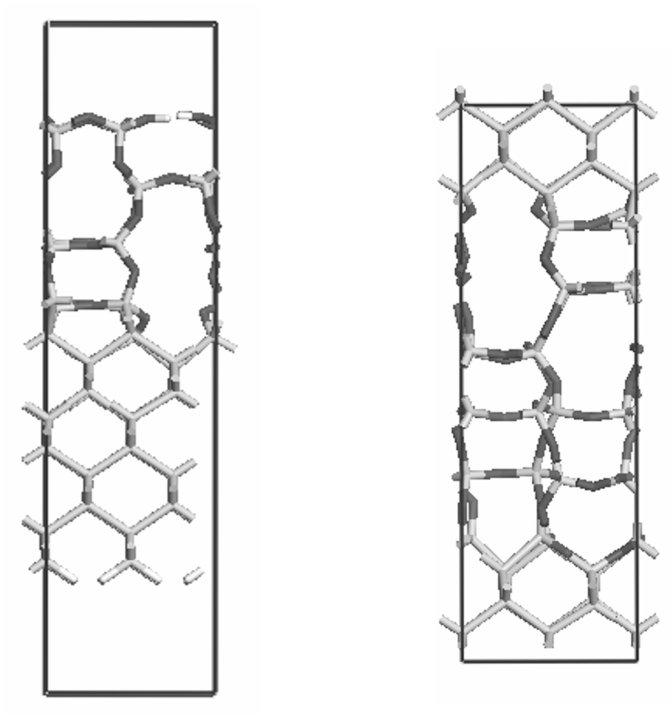
2.1. INTERFACE MODELS

Two models for oxide layers on silicon are considered. Both are derived from the structures due to Pasquarello, Hybertsen and Car[7], with the second being a modified version due to Carrier, Lewis, and Dharma-wardana[8]; these two models will be referred to as PHC and CLD, respectively. The PHC model was generated by bonding a seven layer slab of ß-tridymite to ten layers of Si(001) and terminating all non-saturated atoms at the lowest silicon layer and surface SiO_x layer with hydrogen[7]; in the PHC model, a vacuum layer is introduced resulting in a single interface structure; see fig. 1a). A simulated annealing procedure is used to introduce bond formation between the oxide layer and silicon substrate. Bonding within the structure is then tailored to reproduce know experimental properties at the interface such as the distribution of silicon formal charge states, as derived from photoelectron spectroscopy[9]. In this study, the interface model exhibiting both back bonded and bridging oxygens is considered.

The CLD structure is derived from the model developed by Pasquarello *et al*[7] by introducing two Si/SiO_x interfaces into the simulation cell- this removes the need for hydrogen termination in the structure as the periodic boundary conditions allow for the formation of two oxide/silicon interfaces, and likewise eliminating the need for a vacuum layer within the simulation cell[8]. The resulting superlattice structure is depicted in fig. 1b).

2.2. PLANE-WAVE CALCULATIONS

The Vienna ab initio Simulation Package (VASP)[10] is used for the density functional theory (DFT) calculations for the periodic simulation cells. The gradient corrected PW91 approximation[11] to the exchange-correlation functional is used along with Vanderbilt ultra-soft pseudopotentials[12]. An energy cut-off of 395.7 eV has been applied in the plane-wave calculations and 9.86 Å vacuum layer is included in the direction normal to the interface for the PHC model.



a) b)

Figure 1. Interface models for SiOx on Si(001). a) Interface model due to Pasquarello, Hybertson and Car (PHC). b) Interface model due to Carrier, Lewis and Dharma-wardana (CLD) and derived from the structure depicted in a).

The exchange-correlation potential and other parameters associated with the DFT calculations do not match those from the original model generation. To adjust the lattice parameters, equilibrium lattice values for bulk silicon calculated following the above described procedure and are used to constrain the cell parameters parallel to the interface. As well for the PHC strucuture, the bottom 4 silicon atom layers (and associated H-termination) are held at their bulk positions during geometry optimizations. Total energy convergence with the number of **k**-points was investigated with 2x2x1, 4x4x1 and 8x8x1 grids for the PHC single interface model resulting in energy convergence to less than 20 meV/cell. For the CLD model with two interfaces, geometry relaxation with 2x2x1 **k**-points was performed allowing ionic relaxation and cell volume optimization, with and without the constraint of an orthorhombic simulation cell. No atoms are constrained within these structure relaxations. A final calculation without ion or cell relaxations was performed on the optimized orthorhombic simulation cell with 4x4x2 **k**-points.

2.3. QUANTUM CHEMISTRY CALCULATIONS

Molecular fragment calculations describing the local bonding environments about the oxygen vacancies have been computed using second order many body perturbation theory (or Møller-Plesset (MP2) theory) as implemented in the TURBOMOLE system of programs[13], using correlation consistent polarized valence double zeta (cc-pVDZ) basis sets[14]. MP2 theory provides a size-extensive estimate of the vacancy formation energies and use of molecular fragment allows us to evaluate strain free vacancy formation energies while varying the local chemical environment about the vacancy.

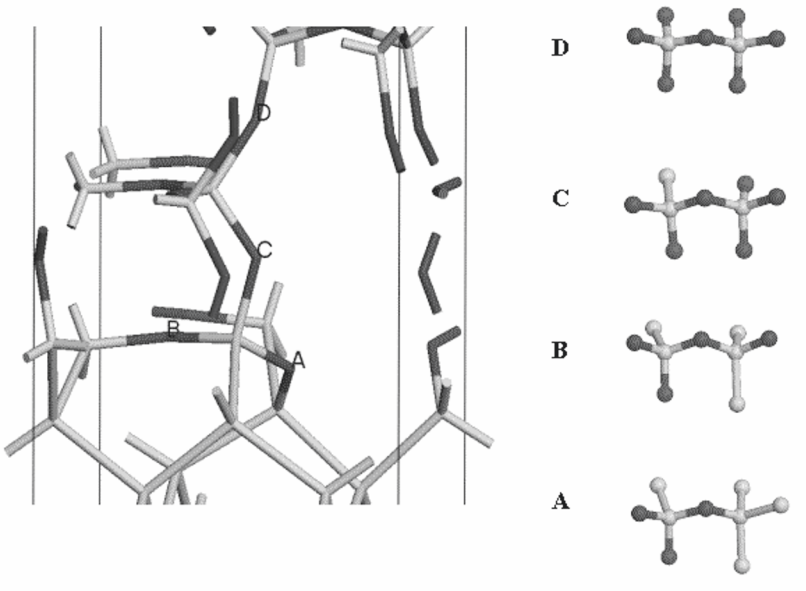
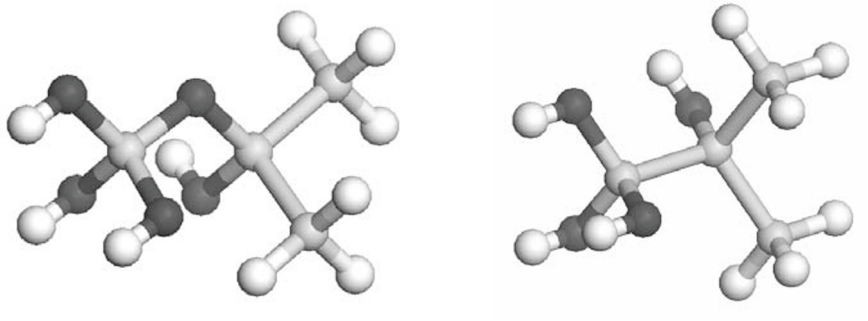


Figure 2. Labeling of oxygen atoms used to created oxygen vacancies in the periodic simulation cells. (A) back bond, (B) surface bridge, (C) interface bridge, (D) bulk sites. Lighter atoms sites represent silicon atoms, darker sites represent oxygen atoms.

Molecular fragments have been built about a Si-O-Si unit by terminating with hydroxyl (-OH) and silane (-SiH_3) groups resulting in a formal Si charge state corresponding to the number of oxygen atoms bonding to a given silicon atom. For the vacancy sites introduced into the periodic simulation cells, the local environments for the oxygen sites may be represented as Si^{+1}-O-Si^{+3}, Si^{+2}-O-Si^{+3}, Si^{+3}-O-Si^{+4}, Si^{+4}-O-Si^{+4} corresponding to the back bond (A), surface bridge (B), interface bridge (C), and bulk (D) sites, respectively. In addition to this set of molecular fragments mimicking the vacancies introduced into the

periodic simulations, molecular fragments with all possible combination of charge states for 4-coordinated silicon atoms have been computed to relate the local chemical environment to oxygen vacancy formation energies.



a) b)

Figure 3. A representative structures used to model the local chemical environment about oxygen vacancies. Formal charge state of the silicon atoms are given by the number of bonding oxygen atoms. Lighter sites represent silicon atoms, darker sites represent oxygen atoms. a) Molecular fragment with central oxygen Si^{+4} – O – Si^{+2} b) The same molecular fragment as in a) after removal of central oxygen atom. Si formal charge states become Si^{+3} and Si^{+1}.

3. Results

Upon removal of the oxygen atoms and after geometry relaxation in the single interface structure, the Si-Si distances at the O singlet vacancy sites relax to 2.31, 2.46, 2.34 and 2.33 Å for defects A, B, C, and D, respectively [5]. This range of values is comparable to findings for Si-Si bond formation at V_O sites in α-quartz[15], and consistent with neutral vacancy sites[16]. Our initial study[5] on the dependence of the formation energies for neutral singlet oxygen vacancies indicate that these defects prefer to form near the silicon substrate and in table 1 the vacancy formation energies for both the PHC and CLD models, and for ease of comparison the relative formation energies, between the sites A, B, C, and D are tabulated.

The formation energy for V_O in α-quartz has been investigated by similar DFT calculations with a vacancy formation energy estimated to range between 5.16 to 8.10 eV, varying based upon the reference chemical potential chosen for free oxygen[6]. The lower energies associated with formation of the vacancies near the interface within the present set of calculations, up to a 1.7 eV difference for interface sites relative to bulk sites, is seen to be significant relative to the formation energies of V_O in bulk silica.

Table 1. Vacancy and relative formation energies for oxygen vacancies near the Si(001)/SiO_x interface for the periodic simulation cells from the PHC and CLD models. Vacancy formation energies given relative to dissociation to molecular ½μ(O_2) and atomic oxygen μ(O).

Defect site	Vacancy formation energy (PHC) ½μ(O_2)/μ(O)	Relative formation energy (PHC)	Vacancy formation energy (CLD) ½μ(O_2)/μ(O)	Relative formation energy (CLD)
Back bond (A)	4.18/7.21	0.00	4.50/7.53	0.00
Surface bridge (B)	5.55/8.58	1.37	5.54/8.57	1.04
Interface bridge (C)	5.68/8.71	1.50	5.71/8.74	1.21
Bulk (D)	5.88/8.91	1.70	5.99/9.02	1.49

Two sources for the difference in the formation energies can be identified: the defect sites exhibit differing local chemical environments, and local strain fields can vary from defect site to defect site. The oxide is capable of relaxing upon introduction of the defect with bond angles and lengths not directly associated to the vacancy site showing some distortion after the introduction of the defect. However, the difference in the average Si-O bond lengths between the PHC cells range by only a few thousandths of an Ångström relative to the vacancy free model, showing relatively little strain associated the introduction of the vacancy. In general, displacement of the substrate atoms relative to their positions in the simulation cell compared to the same simulation cell but without the vacancies is also not large[5]. It is clear from the comparisons to the simulation cell in the absence of a vacancy, that both the oxide and silicon substrate are able to relax to reduce strain about the defect sites, but there is not a large accompanying distortion to either the oxide or silicon layers.

To investigate the effect of strain about the oxygen vacancy sites on the relative formation energies within the PHC simulation cells, tensile and compressive strains of ±1% were introduced in the lattice constants parallel to the Si/SiO_x interface. For compressive strain, there is a slight increase in the relative formation energies, for tensile strain there is a slight decrease- but in both cases the relative formation energies remain within 150 meV of their "unstrained" values. Similarly for the CLD structures, the formation energies when the cell is relaxed without orthorhombic constraints results in shifts of relative formation energies shifted by a maximum of 60 meV. These calculations reveal that the changes due to strain on vacancy formation energies do not alter the preference for the vacancies to form at interface sites.

Table 2. Defect formation energy from molecular fragment models. Vacancy formation energies given relative to dissociation to molecular ½μ(O_2) and atomic oxygen μ(O). HF-SCF- Hartree Fock energies. MP2- 2nd order many body perturbation theory energies.

Molecular fragment	Vacancy formation energies (HF-SCF) ½μ(O_2) / μ(O)	Vacancy formation energies (MP2) ½μ(O_2) / μ(O)
Si^{+1}-O-Si^{+1}	2.86/3.51	2.78/5.20
Si^{+2}-O-Si^{+1}	3.42/4.08	3.48/5.90
Si^{+3}-O-Si^{+1} (A)	3.78/4.41	3.87/6.29
Si^{+4}-O-Si^{+1}	3.75/4.40	3.91/6.33
Si^{+2}-O-Si^{+2}	3.93/4.58	4.09/6.51
Si^{+3}-O-Si^{+2} (B)	4.57/5.20	4.45/687
Si^{+4}-O-Si^{+2}	4.22/4.88	4.46/6.88
Si^{+3}-O-Si^{+3}	4.62/5.27	4.88/7.30
Si^{+4}-O-Si^{+3} (C)	4.65/5.30	4.86/7.28
Si^{+4}-O-Si^{+4} (D)	4.60/5.25	4.93/7.35

MP2 energies for the molecular fragments representing the local environment of the oxygen vacancy are listed in table 2. The formation energies in the table are calculated as the difference in energy of the total molecular fragment in a singlet spin state and the fragment with the central oxygen removed with the two neighboring silicon atoms bonding as a singlet, and either one half the total energy of an isolated oxygen molecule μ(O_2) or the total energy of an oxygen atom μ(O), with both atomic and molecular oxygen in their triplet ground states.

In fig. 4, the role of the local chemical environment on oxygen vacancy formation energies in silica is shown. For example, the lowest values of the formation energy correspond to bonding whereby one of the silicon atoms near the vacancy site is in formal charge state +1. These energies are all approximately 1 eV lower than the corresponding bulk (+4, +4) value as determined by the MP2 calculation on the molecular fragments. All silicon "substrate" atoms bonded to oxide are in a +1 formal charge state. Hence the reduced stoichiometry at the interface favors oxygen vacancy formation over bulk silica sites.

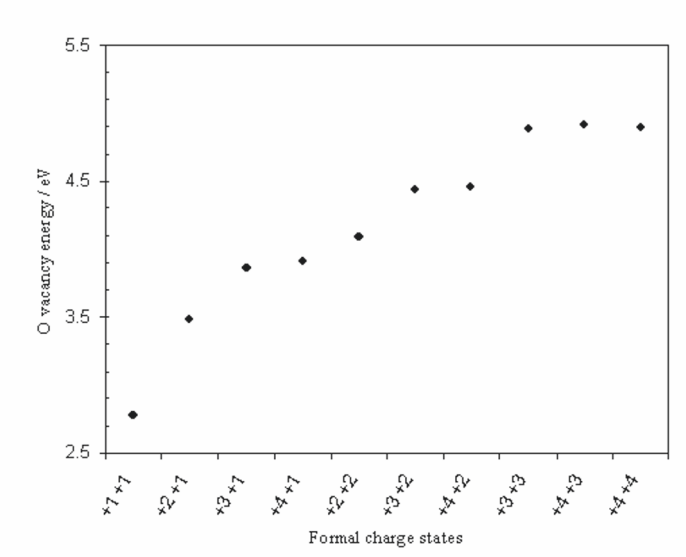


Figure 4. Formation energies relative to dissociation to molecular oxygen for the molecular fragment models. The horizontal axis is labeled by the formal charge states of the two silicon atoms neighboring the oxygen vacancy site, prior to the removal of the oxygen atom from the fragment.

4. Conclusions

Two effects can play a role in oxygen vacancy formation at silicon/silicon oxide interfaces: the local chemical environment, and strain. The calculations reported here indicate that both of these mechanisms determine formation energies, but that the effects of local chemical bonding is the predominate mechanism in determining relative formation energies for neutral singlet oxygen vacancies. When oxygen is bonded to silicon atoms in low oxidation states, the formation energy favors oxygen vacancies relative to oxygen in bulk silica, where most silicon atoms are found in high oxidation states. This finding is consistent with and helps explain the formation of abrupt interfaces at the Si/SiO_x interface[17].

For interfacial oxide layers occurring at high k/silicon interfaces, the reduced stoichiometry implies that oxygen removal is favored at the interface relative to bulk silica. Coupled to the observation that V_O formation in silica is

more favorable than for HfO_2[6], it may be inferred that oxygen may be kinetically driven away from the interface towards the hafnia layer. This effect contributes to reducing the stoichiometry in the SiO_x region, with an accompanying increase in interfacial dielectric constant.

Acknowledgements

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DIELECTRIC AND INFRARED PROPERTIES OF ULTRATHIN SiO_2 LAYERS ON Si(100)

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Abstract. The occurrence of an ultrathin SiO_2 oxide layer at the interface between silicon and high-*k* dielectrics in metal-oxide-semiconductor devices contributes to degrading the capacitance of the gate stack. In this work, we investigate the dielectric and infrared properties of atomically thin SiO_2 layers on Si(100) through a fully quantum-mechanical description. For this purpose, we construct atomistic models of the Si(100)-SiO_2 interface on the basis of available experimental data, by using both classical and first-principles simulation methods. Our model structures account for the experimental density of coordination defects, the distribution of partially oxidized Si atoms, the oxide mass density profile, and the lateral displacements of the Si atoms in the channel region. Our first principles calculations indicate that the permittivity of the SiO_2 layer departs from the bulk value in the limit of atomically thin oxides. This departure is well described through the consideration of an interfacial suboxide layer with a thickness of about 0.5 nm and a dielectric constant of about 6-7. As a consequence, the equivalent oxide thickness of the interfacial layer is smaller than the corresponding physical thickness by 0.2-0.3 nm. Variations of the local dielectric screening occur on length scales corresponding to first-neighbor distances, indicating that the dielectric transition is governed by the chemical grading. We find that the enhanced ionic screening in the substoichiometric oxide results from Si-O bonds formed by Si atoms in the partial oxidation state Si^{+2}. We also extend our investigation to the infrared absorption at the Si(100)-SiO_2 interface. Our study allows us to shed light on the pronounced thickness-dependent red shift of the oxygen stretching modes, which has so far not found a definite interpretation. Indeed, our calculations

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clearly show that the red shift results from a softening of the Si-O stretching vibrations in the interfacial layer.

Keywords: Si-SiO_2 Interface, Density Functional Theory, Dielectric Permittivity, Infrared Absorption

1. Introduction

The Semiconductor Industry Association has indicated the issues related to the gate dielectric in metal-oxide-semiconductor transistors among the most difficult challenges for future device scaling (Semiconductor Industry Association, 2003). Indeed, the equivalent oxide thickness (EOT) required for high-performance applications is as small as 0.8 nm for the 50 nm technology node anticipated for the year 2009 (Semiconductor Industry Association, 2003). In view of the EOT scaling, transition metal oxides such as ZrO_2 and HfO_2, together with their silicate and aluminate alloys, are currently under consideration to replace the natural oxide of silicon (Wilk et al., 2001). However, a very thin SiO_2 interlayer usually forms at the channel interface. Indeed, during the post-deposition anneal for dopant activation, oxygen atoms diffuse out of the transition metal silicate, and oxidize the Si substrate forming an interfacial oxide layer (Van Elshocht et al., 2004). This interlayer may contribute significantly to the overall equivalent oxide thickness, raising questions about the practical scalability limit of gate dielectrics for MOS applications (Muller and Wilk, 2001).

In this context, the accurate determination of the dielectric permittivity at the Si(100)-SiO_2 interface is of primary importance. However, a thorough understanding of the dielectric effect of the interfacial layer is still missing to date. The use of the permittivity of bulk SiO_2 to take into account the interfacial layer contribution to the EOT is questionable, because of the peculiar structural and electronic properties of such a thin interlayer. Indeed, electron-energy-loss spectroscopy measurements of the O-*K* edge profile across the Si(100)-SiO_2 interface indicated a reduced band gap (Muller et al., 1999), suggesting an altered dielectric screening (Muller and Wilk, 2001).

Indirect evidence for an enhanced permittivity within the interfacial oxide has already been reported by Perkins et al. (2001), based on capacitance-voltage measurements on a set of SiO_2-ZrO_2 MOS capacitors. The capacitors considered by Perkins et al. included a gate oxide made of a SiO_2 layer of fixed thickness, and ZrO_2 layers of varying thickness. Extrapolation of the measured EOT of the gate dielectric stack to zero ZrO_2 physical thickness, yielded a static dielectric permittivity of the interfacial layer between 6 and 7, appreciably larger than that of bulk SiO_2 (ε_{SiO2}=3.9). Another indication of an interfacial

layer with an altered dielectric permittivity has been provided by a recent comparison between the thicknesses of ultrathin oxides as measured by medium energy ion scattering and by spectroscopic ellipsometry (Chang et al., 2002). Indeed, Chang et al., (2002) found that the ellipsometric thickness overestimates the physical thickness (as measured by ion scattering) by about 0.2-0.3 nm, when the SiO_2 bulk permittivity is assigned to the MOS gate dielectric.

While an interfacial SiO_2 layer may affect the capacitance of the high-*k* gate stack, it would ensure a smooth transition between silicon and the high-*k* material, therefore preventing the mobility degradation in the channel. From this perspective, it is of primary importance to characterize the structural properties of this interlayer at the atomic scale. Significant information on the local bonding environment can be obtained through infrared spectroscopy, since the high-frequency transverse-optical (TO) and longitudinal-optical (LO) peaks in the infrared spectra of SiO_2 arise from the stretching motion of Si-O bonds (Kirk, 1988). While the interpretation of the infrared spectra of thick SiO_2 samples is well established (Kirk, 1988), the assignment of the absorption bands of ultrathin oxides is still controversial. Indeed, infrared spectroscopic studies of ultrathin SiO_2 films on Si(100) recorded red shifts of the TO and the LO high-frequency peaks for decreasing oxide thicknesses (Queeney et al., 2000; Devine, 1996; Boyd and Wilson, 1987; Miyazaki et al., 1997; Ohwaki et al., 1997). These shifts have variably been ascribed to the compressive strain in the interfacial oxide (Boyd and Wilson, 1987; Miyazaki et al., 1997), to void incorporation (Ohwaki et al., 1997), or to the presence of substoichiometric silica (Queeney et al., 2000). The understanding of the microscopic origin of the TO and LO red shifts at the Si(100)-SiO_2 interface may carry important implications on MOS integrated circuit manufacturing. Indeed, Queeney et al. (2004) recently suggested that the frequency of the Si-O stretching peak could effectively be used to distinguish between ordered and disordered Si(100)-SiO_2 interfaces. The advantage of having an ordered interface with an abrupt transition region is substantial. Indeed, such an interface would be accompanied by an enhanced channel mobility due to the reduced scattering by inhomogeneities in the interfacial layer, leading to larger drive currents and increased transistor performance.

In this work we address the dielectric and infrared properties of the interfacial oxide at the Si(100)-SiO_2 interface within a first-principles approach. After discussing the theoretical framework in sec. 2, we present our results for the dielectric permittivity (sec. 3) and for the infrared absorption (sec. 4). In sec. 5 we summarize our results.

2. Theoretical methods

The Si(100)-SiO_2 model structures were generated by constructing -Si-SiO_2-Si- superlattices based on the transition structures obtained by Bongiorno and Pasquarello (2003) and Bongiorno et al. (2003). The superlattice geometry allowed us to avoid complications arising from silicon-vacuum and oxide-vacuum interfaces. Hence, for each model considered, we mirrored the structure with respect to a Si substrate plane parallel to the interface, so as to obtain opposite Si-SiO_x and SiO_x-Si junctions, separated by a vacuum region. Then, in every considered case, we generated stoichiometric SiO_2 in the central vacuum region by introducing Si and O atoms randomly, and performing a melt-end-quench cycle with classical pair-potentials (Vashista et al., 1990). The [100] cell parameters were chosen so as to obtain melts at the experimental density of vitreous SiO_2. This resulted in Si-SiO_2 superlattices with substoichiometric transition regions and disordered oxides. In order to release the residual strain, we further relaxed the atomic positions through first-principle molecular dynamics. Overall, we obtained three structural models of the Si(100)-SiO_2 interface, which hereafter we will refer to as model I, II, and III, respectively. Models I and II consist of 315 and 313 atoms, respectively, distributed in 13 Si layers and 2.5 nm of oxide, within simulation cells of size $\approx 11\times11\times45$ Å^3. Model III consists of 217 atoms distributed in 9 Si layers and 1.6 nm of oxide, within a simulation cell of size $\approx 11\times11\times30$ Å^3. The transition structure of model I corresponds to model B of Bongiorno et al. (2003), where the terminating Si layer shows a high density of in-plane Si-Si dimers, with a high fraction of oxidized backbonds. The transition structure of model II corresponds to model C' of Bongiorno et al. (2003), where the structure of the terminating Si layer is adapted from a structure generated previously by first-principles molecular dynamics (Pasquarello et al., 1998). The transition structure of model III was obtained from that corresponding to model II by replacing a Si-Si bond in the first Si layer by a Si-O-Si bridge. Model III was generated in order to reduce the computational cost in the calculation of the vibrational eigenmodes.

Our model Si-SiO_2 transition structures are free of coordination defects, consistently with the extremely low density of interface states deduced from electrical (Witczak et al., 1992) and electron-spin-resonance measurements (Stesmans and Afanas'ev, 1998). The amount, distribution and location of Si atoms in intermediate oxidation states is in good agreement with angle-resolved Si-2*p* core-level photoemission spectroscopy (Rochet et al., 1997; Oh et al., 2001). The spatial distribution of the suboxide species in all our interface models shows the Si^{+1} and Si^{+2} species concentrated close to the outermost Si layer, and the Si^{+3} states spread over a broader region, in accord with the experimental results obtained by Oh et al. (2001). The thickness of the

substoichiometric oxides, which we here define as the distance between the farmost partially oxidized Si atoms, is 6.4 Å for model I, 5.1 Å for model II, and 6.1 Å for model III. The simulation of ion scattering experiments in the channeling geometry with ion energies between 0.4 and 1.0 MeV gives an excess Si yield of 2.7 MLs for model I, of 2.9 MLs for model II, and of 2.8 MLs for model III. These values are in good agreement with the experimental result of 3.0 ± 0.3 MLs (Bongiorno et al., 2003). The density of the oxide in proximity of the substrate is ≈ 2.3 g/cm^3 for model I and II, and ≈ 2.4 g/cm^3 for model III, in accord with reflectivity measurements (Awaji et al., 1996; Kosowsky et al., 1997). Inside the oxide regions the density decreases to 2.2 g/cm^3 (model I), 2.1 g/cm^3 (model II) and 2.3 g/cm^3 (model III). The latter values are close to the experimental density of vitreous silica (2.2 g/cm^3).

The electronic structure of our models was described within density functional theory. We used the generalized gradient approximation of Perdew and Wang (1992) for models I and II, and the local density approximation as parametrized by Perdew and Zunger (1981) for model III. The approximation chosen for model III is known to achieve more accurate vibrational properties. We accounted for the valence electrons using normconserving pseudopotentials for Si atoms (Dal Corso et al., 1996; Bachelet et al., 1982) and ultrasoft ones for O atoms (Vanderbilt, 1990). We expanded the wave functions and the charge density on plane-wave basis sets (Pasquarello et al., 1992), with kinetic energy cutoffs of 24 and 150 Ry, respectively (models I and II), and of 24 and 200 Ry, respectively (model III). We sampled the Brillouin zone of the supercell at the Γ point. The relaxation of the atomic positions was performed by means of a damped molecular dynamics scheme (Pasquarello et al., 1992), and carried on until the atomic forces did not exceed 0.03 eV/Å. We calculated the local static and high-frequency dielectric permittivities through the procedure described by Giustino and Pasquarello (2005a). The dynamical matrix which defines the vibrational properties was calculated through finite differences of the atomic forces corresponding to atomic displacements of ±0.05 Å. The dynamical charges required for the infrared intensities were calculated by taking finite differences of the atomic forces with respect to externally applied electric fields of ±0.05 V/Å^{-1}, following Umari and Pasquarello (2002). The calculated spectra were broadened through Gaussian functions with a standard deviation of 40 cm^{-1} in order to overcome the limited statistics. The spatial decomposition of the transverse and longitudinal absorption intensities was performed by determining the dielectric functions of atomically thin layers parallel to the interface. This was achieved through the evaluation of localized infrared dipoles induced by an external electric field (Giustino, 2005). The formalism adopted here constitutes a generalization of the methods developed by Giustino and Pasquarello (2005a) for the static and high-frequency permittivities to the whole infrared spectral range.

3. Dielectric permittivity

Figure 1 shows the calculated profiles of the high-frequency and the static permittivity across our interface models (Giustino and Pasquarello, 2005b). The high-frequency and static permittivities in the middle of the Si slab approximately coincide, due to the vanishing dynamical charges at a sufficiently large distance from the interface. The calculated static permittivity, $\varepsilon^0_{Si} = 12.5$ for both model interfaces, slightly overestimates the experimental value of 11.9. We evaluated an average high-frequency permittivity of 2.3 for the stoichiometric oxides of both model interfaces. The corresponding static permittivities are 4.2 and 4.0 for model I and model II, respectively. Also in this case, the calculated permittivities slightly overestimate the experimental values (2.1 and 3.9 for the high-frequency and the static permittivity, respectively). The difference between the static permittivities of the oxides in our models can be traced back to their different mass densities. The permittivities of the substoichiometric oxide amount to $\varepsilon_{SiO_x} = 6.9$ and $\varepsilon_{SiO_x} = 5.7$ for model I and model II, respectively. The difference mainly arises from the different spatial distributions and orientations of the suboxide Si–Si bonds. Our calculations are consistent with indirect experimental measurements which assign a static permittivity between 6 and 7 to the interfacial layer (Perkins et al., 2001). Furthermore, Figure 1 shows that the permittivity of bulk SiO_2 is recovered as soon as the Si atoms become fully oxidized, i.e. at a distance of 5–6 Å from the substrate. This result is consistent with Auger measurements (Hirose et al., 2003).

The calculated permittivities are reasonably accurate, despite the significant underestimation of the band gaps (we found 0.8 eV and 5.0–5.1 eV for Si and SiO_2, respectively, to be compared with the corresponding experimental values of 1.1 eV and 8.9 eV; Giustino and Pasquarello, 2005b). This is consistent with the observation that the electronic permittivity scales with the inverse of the squared Penn gap (roughly corresponding to the strongest optical absorption peak), which is relatively insensitive to the value of the fundamental band gap (Yu and Cardona, 2003). The overestimation of the electronic permittivity in our calculations arises from the use of a local approximation to the exchange-correlation functional (Gonze et al., 1995), and is consistent with previous calculations for Si (Dal Corso et al., 1994) and SiO_2 (Gonze et al., 1992).

The enhanced *electronic* permittivity of the suboxide region has previously been related to the silicon-induced gap-states which have vanishing tails in the interfacial oxide (Muller et al., 1999; Muller and Wilk, 2001). In order to investigate the role of such states, we evaluated their contribution to the screening of the interfacial oxide through an approach based on maximally localized Wannier functions (Giustino et al., 2003). The contribution of the gap states to the dielectric screening in the interfacial layer was found to be only a

small fraction (13%) of the total electronic polarization in that region, indicating that their role is secondary. At variance, we found that the permittivity enhancement is chemical in origin, being related to the larger polarizability of the structural units associated to partially oxidized Si atoms (Giustino et al., 2003).

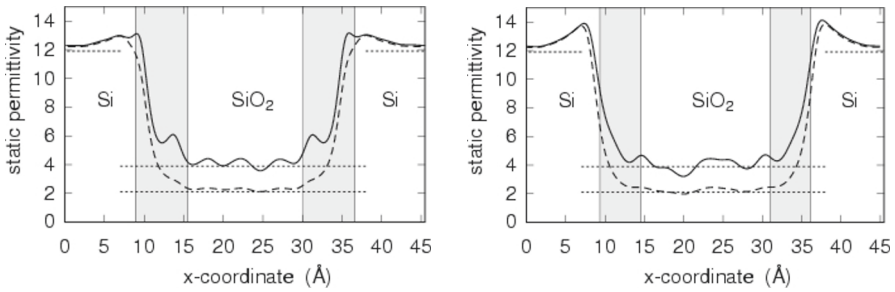


Figure 1. Dielectric permittivity profiles of model I (left) and model II (right) of the Si(100)-SiO_2 interface. Solid lines indicate the static permittivity, dashed lines the high-frequency permittivity. The *x*-coordinate is taken along a direction perpendicular to the interface plane. Horizontal dotted lines correspond to the experimental values. The shaded areas indicate the suboxide regions.

The *ionic* contribution to the dielectric permittivity ε_{ions} scales with the inverse of the vibrational eigenfrequencies squared: $\varepsilon_{ions} \sim \Sigma_n S^2_n/\omega^2_n$, the sum running over the eigenmodes of frequency ω_n and strength S_n. Therefore, the red shift of the infrared absorption peaks of the interfacial oxide could imply an enhanced ionic contribution to the permittivity close to the Si substrate. Indeed, our calculations for model III of the Si(100)-SiO_2 interface indicate that the ionic contribution to the local permittivity of the interfacial layer can be as high as $(\varepsilon_{ions})_{inter} = 2.6$. In Fig. 2 we analyze the contribution of each eigenmode to the static permittivity by showing, as a function of the frequency ω, the ε_{ions} obtained by summing only over the modes with frequency $\omega_n > \omega$. The mode contribution to the static permittivity has been evaluated separately for the bulk oxide and for the interfacial layer in our model Si(100)-SiO_2 interface. For comparison we also report in Fig. 2 the corresponding imaginary dielectric functions. The high-frequency modes are clearly not involved in the enhanced ionic screening of the suboxide, the extra screening arising from a suboxide peak around 230 cm^{-1} (Fig. 2, shaded area). Indeed, when the modes between 220 and 240 cm^{-1} are forced to be silent, the suboxide ionic permittivity drops to the value calculated for the bulk oxide. By inspecting the atomic displacements corresponding to these modes within the suboxide, we found that the main contribution to the extra screening arises from Si^{+2} atoms together with their O nearest neighbors (Giustino and Pasquarello, 2005c). The large polarizability of

the $Si^{+2}O_2$ structural units is a consequence of both the large dynamical charges of Si^{+2} atoms and the small associated vibrational frequency of 230 cm^{-1} (to be compared to the corresponding modes of bulk SiO_2 around 450 cm^{-1}).

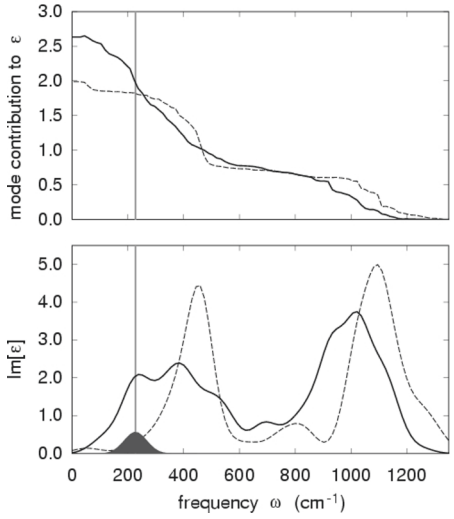


Figure 2. Upper panel: vibrational mode contribution to the static permittivity, evaluated within the interfacial layer (solid) and the bulk oxide (dashed) of our model Si(100)-SiO_2 interface. For each frequency ω, we considered the contribution of all eigenmodes with frequencies higher than ω. Lower panel: imaginary part of the dielectric function vs. frequency, for the interfacial layer (solid) and the bulk oxide (dashed). The shaded region indicates the contribution of $Si^{+2}O_2$ structural units, giving rise to the peak at 230 cm^{-1}. The vertical line indicates that, in proximity of this resonance, the mode contribution to the static permittivity of the suboxide starts exceeding the corresponding one of bulk SiO_2.

The enhanced permittivity of the substoichiometric oxide indicates that the equivalent oxide thickness of an oxide interlayer (including the substoichiometric region) between Si and a high-*k* material is smaller than its physical thickness. In order to quantify this effect, we calculate the EOT of interfacial layers with physical thicknesses between 0.5 and 2 nm (Fig. 3). Overall, the resulting EOT of the interlayer is smaller than the corresponding physical thickness by 0.2–0.3 nm.

As a consequence, the effect of a thin oxide layer between a Si substrate and a high-permittivity material in metal-oxide-semiconductor devices is less severe than expected on the basis of the permittivity of bulk SiO_2. Indeed, the EOT reduction of 0.2–0.3 nm with respect to bulk SiO_2 leaves some limited yet useful margin to the allowed oxide thickness in multilayer gate dielectrics. As an example, we consider the targeted 0.8 nm EOT for the 50 nm technology node. Assuming that the equivalent thickness of the high-permittivity material

were as small as 0.5 nm [the smallest value reported to our knowledge for HfO_2, see Harris et al. (2002)], the maximum allowed *physical* thickness for the interlayer would result in 0.5–0.6 nm instead of 0.3 nm.

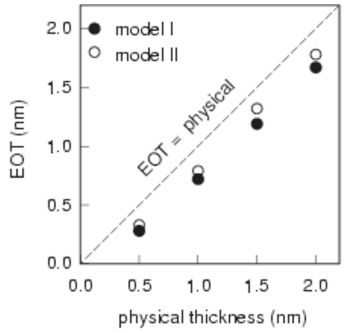


Figure 3. Equivalent oxide thickness vs physical thickness for the oxides in model I (disks) and model II (circles) of the Si-SiO_2 interface. For comparison, we also report the case of an oxide layer with a fixed permittivity corresponding to that of bulk vitreous silica (dashed). The EOT of ultrathin oxides is smaller than the corresponding physical thickness by 0.2–0.3 nm.

4. Infrared absorption

Figure 4 shows the calculated TO and LO infrared absorption spectra across our model interface, at various distances from the Si substrate. At a distance of 8–9 Å from the substrate, the absorption spectra closely match those of bulk vitreous silica (bold curves in Fig. 4). Indeed, the calculated positions of the main TO absorption peaks, 457, 810, and 1097 cm^{-1}, are in excellent agreement with the corresponding experimental peaks at 457, 810, and 1076 cm^{-1} as given by Kirk (1988), and with calculations on bulk disordered SiO_2 from Pasquarello and Car (1997) giving 453, 861, and 1106 cm^{-1}. Similarly, the calculated positions of the main LO peaks, 529, 820, and 1260 cm^{-1}, are in excellent agreement with the corresponding experimental peaks at 507, 820, and 1256 cm^{-1} measured by Kirk (1988).

We focus hereafter on the high-frequency peaks, for which an extensive set of experimental data is available (Queeney et al., 2000; Devine, 1996; Boyd and Wilson, 1987; Miyazaki et al., 1997; Ohwaki et al., 1997). As the distance from the Si substrate decreases, two shoulders develop around 939 and 1077 cm^{-1} in the TO and LO spectra, respectively (Fig. 4). In this region, the oxide is slightly oxygen-deficient and Si^{+2}, Si^{+3} species occur. In the vicinity of the substrate, these shoulders become the principal peaks. The corresponding oxide is highly oxygen-deficient, containing Si^{+1} and Si^{+2} species. Within the silicon substrate, the infrared activity is suppressed as the dynamical charges of Si atoms vanish.

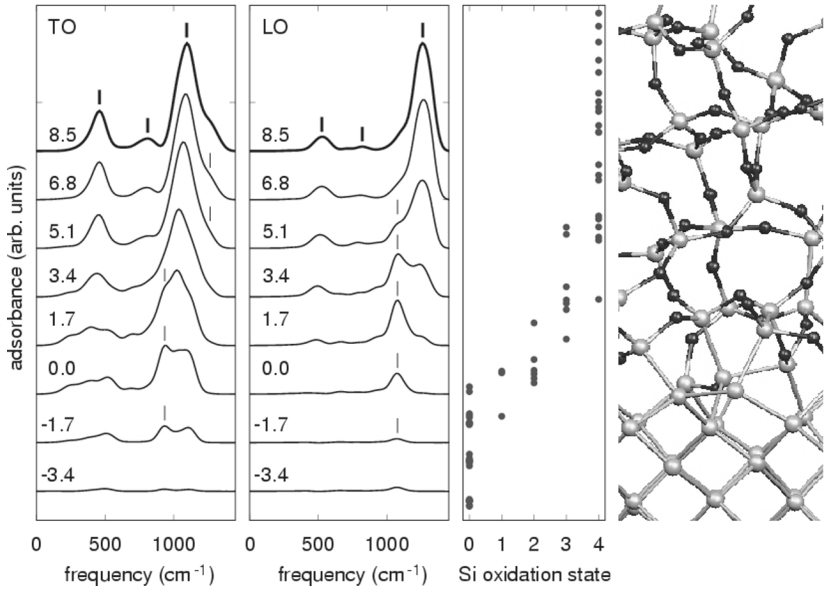


Figure 4. Local TO (first panel from the left) and LO (second panel) infrared absorption spectra calculated at various distances from the Si substrate, for model III of the Si(100)-SiO_2 interface. The distances are indicated in Å and refer to the first O atom of the oxide. The principal spectral features are highlighted. The third panel from the left shows the distribution of the various oxidation states of Si across the interface, and the last panel is a ball-and-stick representation of the model interface.

The largest calculated red shift of the absorption peaks are 158 cm^{-1} for the high-frequency peak of the TO spectrum, and 183 cm^{-1} for the corresponding peak in the LO spectrum. Since these values refer to the *local* absorption, they cannot be compared directly to experiments on the Si-SiO_2 interface, which address the overall behavior of a structure with a strong chemical grading. Nonetheless, these data can be confronted with experiments on bulk substoichiometric silica (SiO_x). Focusing on the high-frequency region of the TO spectrum, several investigations reported peak frequencies within the range 940–987 cm^{-1} for SiO_x with low O content (Pai et al., 1986; Nakamura et al., 1984; Wells et al., 2004; Schumann et al., 1982). In particular, TO peak frequencies for suboxides SiO_x with $x \leq 0.1$ were observed within the range 945–960 cm^{-1}. Furthermore, a recent study of ultrathin SiO_2 layers on Si(100) recorded a shoulder at 980 cm^{-1}, and proposed the assignment of this feature to a substoichiometric interfacial layer (Queeney et al., 2000). Our calculated TO peak at 939 cm^{-1} is therefore in agreement with experimental data on bulk SiO_x with $x \leq 0.1$, and supports the assignment of the shoulder at 980 cm^{-1} to the suboxide layer (Queeney et al., 2000).

5. Conclusions

We investigated the dielectric permittivity of realistic models of the Si-SiO_2 interface from first principles. Our calculations indicate that the permittivity of the interfacial suboxide can be significantly larger than the corresponding value of vitreous silica. A full quantum-mechanical description of the dielectric screening therefore suggests that the ultimate EOT scalability limit of gate dielectric stacks with an oxide interlayer is reduced by 0.2–0.3 nm when the interfacial oxide is accounted for with the proper permittivity.

In addition, we calculated the infrared absorption spectra at the Si(100)-SiO_2 interface within a first-principles approach. The calculated peaks within the interfacial layer agree with experiments on substoichiometric oxides and on Si(100)-SiO_2 interfaces with ultrathin oxides. The present investigation allowed us to assign the origin of the TO and LO high-frequency red shift with decreasing oxide thickness to the softer vibrational modes of the interfacial suboxide layer.

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THE (1 0 0) SURFACE OF SEMICONDUCTOR SILICON (IN PRACTICAL CONDITIONS): PREPARATION, EVOLUTION, PASSIVATION

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Abstract. The chemical structure and morphology of the (1 0 0) Si surface is described in relation to its preparation method. Three techniques have indeed been developed: etching with HF aqueous solution of a thermally grown sacrificial oxide; demolition in an ultra-high vacuum of the native oxide and exposure of the resulting clean 2×1 surface to atomic hydrogen at moderate temperature; or exposure of the native surface to molecular hydrogen at high temperature.

Keywords: (1 0 0) Si surface; hydrogen terminations, oxo termination; surface heterogeneity; surface roughness

1. Introduction

Metal-oxide-semiconductor (MOS) transistors are almost uniquely produced at the surface of (1 0 0) silicon. The progressive scaling down of the channel length (now below 100 nm) has imposed a reduction of the oxide thickness x_{ox} to the length scale of a few nanometers. In turn, the reproducibility of the electrical characteristics of the MOS transistor (in terms of threshold voltage, channel-to-gate leakage current, etc.) has required a control of the Si-SiO_2 interface on the subnanometre length scale—the atomic length scale.

For $x_{ox} < 5$ nm it is likely that the present transistor material structures,

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$$(1\ 0\ 0)\ \mathrm{Si} \mid \mathrm{SiO}_y \mid \mathrm{SiO}_2 \mid \text{poly-Si} \tag{1}$$

or

$$(1\ 0\ 0)\ \mathrm{Si} \mid \mathrm{SiO}_y \mid \mathrm{SiO}_2 \mid \text{poly-Si:Ge} \mid \text{poly-Si} \tag{2}$$

(with $y < 2$) , are no longer acceptable (because of the excessive channel-to-gate direct tunneling), and the MOS transistor is expected to undergo a major change with the substitution of insulators with high dielectric constant K for SiO_2 (for which K_{ox}= 3.9). The expected new material structures are therefore

$$(1\ 0\ 0)\ \mathrm{Si} \mid \mathrm{SiO}_y \mid \text{high-}K\text{ amorphous insulator} \mid \text{poly-Si} \tag{3}$$

or

$$(1\ 0\ 0)\ \mathrm{Si} \mid \text{high-}K\text{ crystalline insulator} \mid \text{poly-Si} \tag{4}$$

In structure (3) SiO_y is actually a buffer layer, which allows the deposited high-K insulator to be chemically compatible with the (1 0 0) Si substrate. In structure (4), instead, the high-K insulator is crystalline and epitaxially grown on the clean (1 0 0) Si surface. In both cases, the (1 0 0) Si surface and its terminations must probably be controlled at an even better level than that necessary for structures (1) and (2). This lecture is devoted to present an overview of the proposed ways for the controlled termination of the (1 0 0) surface of single crystalline silicon.

2. The native surface of commercial silicon

There are several specs for commercially available (1 0 0) silicon. The following considerations apply to most of them and may therefore be seen as characteristic of a hypothetical ‘commercial silicon’.

The (1 0 0) *plane* of silicon is not a cleavage plane. The nominal (1 0 0) *surface* is typically obtained by cutting and lapping the single crystal along a plane as close as possible to the (1 0 0) and chemo-mechanically polishing the resulting rough surface with colloidal SiO_2 dispersed in KOH aqueous solution[1,2]. As a consequence of this process, the actual (local) orientation resulting after cutting and polishing is controlled by the alignment errors of the sawing and lapping machines and by the roughness remaining after polishing. The final result is a misoriented surface (typically to within ±1°), with a local peak-to-valley roughness on the nanometre length scale. For many years the quality of such a surface has been related to the cleaning process after polishing. Due to the rich knowledge of the chemistry of aqueous solutions, most cleaning involved wet

processing. The most widely used of such processes was developed in RCA (Radio Corporation of America) laboratories in the mid sixties. The RCA cleaning employs two steps (where for all X, X_{aq} denotes the aqueous solution of X):

- (*SC1*) standard cleaning 1, where the wafer is exposed to a hot mixture of $H_2O_{2aq} + NH_{3aq}$, aimed to removes organics and particles; and
- (*SC2*) standard cleaning 2, where the wafer is exposed to a hot mixture of $H_2O_{2aq} + HCl_{aq}$, designed to remove metals.

The combination of this procedure with `piranha' etching (a concentrated aqueous solution of $H_2SO_4 + H_2O_2$) before SC1, between SC1 and SC2, or after SC2, followed by a final etching in HF_{aq} and rinsing in de-ionized H_2O has usually been considered an adequate treatment of the surface[3]. In last years, however, the attention has shifted from contaminants (organics, metals, particulates) to the chemical termination of the surface after the cleaning process. This state, indeed, affects appreciably the behaviour of the Si-SiO_2 interface resulting after gate oxidation. The polishing procedure, indeed, produces surfaces with prevailing hydrogen terminations, but containing residual oxo centres (Si–O–Si and Si–O–H) too[4,5]. The oxo-terminated surfaces exposed to humid air at room temperature undergo further oxidation[6,7] and the early stages of oxidation produce a chemically heterogeneous zone where silicon oxidation state is distributed between 0 and 4.[8]

The extent of oxidation and hydroxylation undergone by the surface depends on the following quantities: HF_{aq} concentration, solution *p*H, concentration of dissolved O_2 in rinsing water, H_2O concentration in air, and exposure to air. As far as these quantities are uncontrolled, the state of the surface (the *native surface*) is generally unknown in a broad distribution of allowed states. In the following I shall describe the methods developed for the preparation of surfaces without oxo terminations.

3. Hydrogen-terminated surfaces

The common belief, that defect-free hydrogen-terminated silicon would be indefinitely stable (on the laboratory time scale) in air at room temperature, explains why several methods for the hydrogen termination of (1 0 0) silicon have been developed. They include:

- the chemical attack with HF_{aq} under special *p*H conditions of a sacrificial, thermally grown oxide;

- a two-step process, formed by: (i) the demolition of the native oxide by heating in an ultra-high vacuum (UHV) at a temperature T of, say, 850°C with the formation of a clean 2×1-reconstructed surface; and (ii) the subsequent exposure of the surface to a few langmuirs of atomic hydrogen H; and
- the exposure of the native surface to H_2 at sub-atmospheric pressure (typically in the interval $10^2 – 10^3$ Pa) and high temperature (800–1100°C).

Hydrogen-terminated surfaces can greatly differ according to the preparation procedure.

3.1. THE SURFACE RESULTING AFTER ETCHING IN AQUEOUS SOLUTION OF HF

The dipping of the native or thermally grown oxide in HF_{aq} results typically in a rough and heterogeneous surface. The quality of the surface is controlled by the pH of the etching solution (in turn controlled by HF_{aq} dilution and the presence of buffer species like NH_4F or acids like HCl) and by the amount of dissolved O_2 in the stirring water. Nonetheless, the following features are usually observed: the (1 0 0) surface resulting after HF_{aq} attack has 1×1 symmetry, and is characterized by a heterogeneous distribution of SiH_3, SiH_2 (prevalently) and SiH terminations[5,6,9].

The quality of the surface is controlled by the etching and rinsing process; the best etchant is a very acidic solution (HF:HCl =1:19 at pH < 1)[10]. (Almost ideal hydrogen termination of the (1 1 1) surface is instead obtained[11] after etching in an HF solution buffered with NH_4F or NH at pH > 5.) Inspected by scanning tunneling microscopy, HF_{aq}-etched surfaces usually do not provide any evidence for regularity[12]; images with atomic resolution, giving evidence for 1×1 symmetry[13], can be obtained only for surfaces prepared at low pH.

Understanding why the silicon surface after etching in HF_{aq} has prevailing hydrogen, rather than fluorine terminations, is not trivial. In fact, silicon and fluorine combine to form one of the most stable bonds (if not the most stable at all), with bond energy E_b of 6.9 eV. (The Si–F bond is stronger than the N=N O=O and C=C double bonds, with bond energies of 4.3 eV, 5.2 eV and 6.4 eV, respectively.[14]) Marvel not therefore, the surprise when etching by concentrated HF_{aq} of the native oxide was discovered to leave hydrogen-terminated silicon surfaces[15].

3.1.1. *An explanation—the attack is controlled by oxidative addition of HF to the backbonds to Si–F bonds*

The first explanation of this fact was in terms of polarization of Si–Si backbonds to Si–F bonds. Assuming that the strength of the Si–F bond derives from an electrostatic reinforcement due to electron transfer from silicon to fluorine, the ionicity of the Si–F bond polarizes the Si–Si backbonds, that allows an easy insertion (via oxidative addition) of HF therein. If (as suggested by the natural orientation of the HF dipole in the vicinity of the partial positive charge on silicon bonded to fluorine) the backbond is cleaved with the addition of fluorine to the SiF site and of hydrogen to the other silicon atom, the ionicity is further increased and so is the polarization of the residual backbonds. Reiterating this argument, one obtains that the formation of a SiF_n moiety becomes easier the higher is n, and that this process is concluded with the formation of a volatile SiF_4 molecule and of hydrogen terminations at the neighbouring surface sites[15].

This scheme was investigated quantum mechanically on model molecules (like $H_3Si–SiH_2F$ or H_3SiF) by Trucks *et al.*[16]: Assuming the undissociated HF molecule as etching agent, they supported the conclusion of Ubara *et al.*[15], that the formation of hydrogen-terminated surfaces is kinetically, rather than thermodynamically, controlled (that, in turn, implies that the surface is never fully hydrogenated).

3.1.2. *Is undissociated HF the etching agent?*

The assumption of undissociated HF as the etching agent has since then been widely accepted by the scientific community as a rationale for understanding the hydrogen terminations remaining after HF_{aq} attack to oxidized silicon. This interpretation is however contradicted by the following facts:

- In *diluted aqueous solution* HF is completely dissociated, $HF + H_2O \rightarrow F^- + H_3O^+$; its behaviour as a weak acid is due to the reduction of the H_3O^+ activity resulting from tight ion pairing $F^{-}\cdots H_3O^+$ between the fluoride and oxonium ions.
- In *concentrated aqueous solution* the H_3O^+ activity is increased because of the formation of hydrogen-bonded adduct $F^{-}\cdots HF$ via equilibrium[17] $F^{-}\cdots H_3O^+ + HF \rightarrow F^{-}\cdots HF + H_3O^+$. Thus, although concentrated HF_{aq} contains undissociated HF, its binding energy to F^- is however so high that adduct $F^{-}\cdots HF$ is considered a well defined ion HF_2^-.
- In *gas-phase* hydrogen fluoride occurs mainly as dimer $(HF)_2$.

- The attack by gas-phase hydrogen fluoride produces mainly fluorine-terminated silicon surfaces[18].

The last piece of evidence contradicts the conclusions of Trucks *et al.*[16]; the dimeric nature of hydrogen fluoride and steric effects, not considered by those Authors, may perhaps be responsible for this anomaly.

3.1.3. *The role of ionized species in solution*

The candidate process has a chance of describing the actual process only if the most endothermic step requires an enthalpy not appreciably larger than 1 eV (to allow it to be active at room temperature on the laboratory time scale) and all other steps have a negative enthalpy difference (or very small, if positive) and do not require special low-probability configurations.

An alternative model to account for the hydrogen terminations of silicon after HF_{aq} attack was proposed by Cerofolini and Meda, who advocated a role of ionic species solution[19,20]. The very fact that the solution *p*H controls the quality of the surface demonstrates indeed that the ionic species play a fundamental role in HF_{aq} attack. Since the attack requires the demolition of Si–Si bonds exposed to the etching solution, it is presumably initiated by processes able to weaken the bond. Several reaction pathways can be hypothesized to constitute the early stages of the attack:

- homolytic cleavage,
- heterolytic cleavage,
- heterolytic cleavage via the formation of a Lewis adduct between H_2O and the silicon cation,
- heterolytic cleavage via the formation of a Lewis adduct between HF and the silicon cation, or
- F^- capture by the fluorine coma of silicon.

Of all these pathways the unique reaction scheme giving a formation energy decreasing with the number *n* of fluorine terminations was found to be the capture of a fluoride ion from the fluorine terminated silicon[21]:

$(CH_3)_4Si + F^-_{aq} \rightarrow (CH_3)_4Si\,F^-$ –1.3 eV

$(CH_3)_3SiF + F^- \rightarrow (CH_3)_3Si\,F_2^-$ – 1.7 eV

$CH_3SiF_3 + F^- \rightarrow CH_3SiF_4^-$ –2.2 eV

$SiF_4 + F^- \rightarrow SiF_5^-$ –2.8 eV

Of course, if the fluoride ion is in an aqueous solution, its capture by the silicon surface will result in a reduction of its hydration cloud because of the steric constraint imposed by the surface—that implies that a fraction, expectedly of the order of 50%, of its hydration energy (5.0 eV) is lost in the process.

3.2. THE SEVERAL SURFACE PHASES PRODUCED BY THE EXPOSURE OF CLEAN (1 0 0) SILICON TO ATOMIC HYDROGEN

The preparation of surfaces with homogeneous chemical terminations has hitherto been possible only using dry processing. The one most extensively studied requires the use of atomic hydrogen in an UHV system, where H is produced *in situ* by the dissociation of H_2 after contact with a hot tungsten filament.

3.2.1. *The clean 2×1 (1 0 0) Si surface*

The process starts with the demolition of the native surface by a heat treatment at $T \approx 850$ °C in an UHV system. If this process is sufficiently prolonged, it eventually results in a terraced, clean surface with 2×1 symmetry. If the alignment uncertainty is small, the terraces have height of one atomic step and length controlled by the misalignment. In each terrace the 2×1 units are aligned along a sheaf of parallel straight lines; the orientation of the 2×1 units is rotated by 90° on going from one terrace to the neighboring ones. Each step is limited by two lines, one almost rectilinear ('A line') and the other zigzag shaped ('B line')[22]. If the process is stopped before the formation of the terrace structure, the surface is still clean and dangling bond tend to saturate via atomic pairing, but the surface maintains the original rough character.

The 2×1 unit is interpreted as a silicon dimer $Si{=}Si_d$ in which two silicon atoms are bonded by a double bond. The bonds may be described as: a strained σ bond $Si{-}Si_d$ with bond dissociation energy of ca. 2.0 eV, and a π bond (similar to those in silenes) with negligible bond dissociation energy (about 0.1 eV)[23]. The clean 2×1 (1 0 0) Si surface is extremely reactive and undergoes almost immediately oxidation after exposure to air. It can however be passivated by exposure to atomic hydrogen *in situ*.

3.2.2. *The phases resulting after the exposure of clean 2×1 (1 0 0) Si to H*

Terraced surfaces The clean terraced 2×1 (1 0 0) Si surface reacts readily with atomic hydrogen forming different phases according to the reaction temperature:

- the 1×1 dihydride phase at 300 K,

- 4/3 H monolayers with 3×1 reconstruction at 400 K, or
- the monohydride phase with 2×1 reconstruction at 600 K;

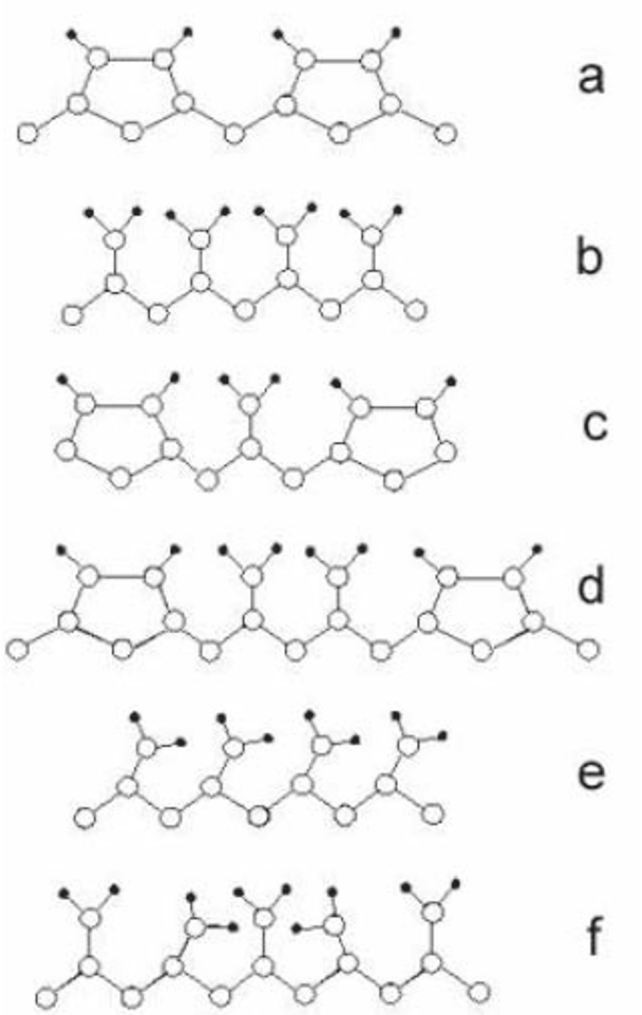


Figure 1. Schematic of various hydrides occurring at the (1 0 0) silicon surface: a, 2×1 monohydrides; b, 'classic' 1×1 dihydrides; c, 3×1 alternating di- and mono-hydrides; d, 'split dimer' dihydrides between monohydride domains; e, canted 1×1 dihydrides; f, 'domain-boundary' situation where dihydrides with elongated Si-Si backbonds alternate with canted dihydrides [see K. Tagami, and M. Tsukada, *Surf. Sci.* **400,** 383 (1998)]

these (and others) are shown schematically in Fig. 1 (unless otherwise specified, all information on hydrogen-terminated silicon surfaces is taken from the review of Oura *et al.*[24]) . Needless to say, the high reactivity of H toward silicon implies that the exposure be accurately tuned. The process is kinetically controlled and overdosing produces surface etching.

Rough surfaces The clean rough 2×1 (1 0 0) Si surface manifests toward H an additional reactivity: indeed, in addition to the superficial 1×1 and 2×1 phases, there is the formation of a buried phase[25]. This phase is formed only in a narrow temperature interval centred on 460 K.

3.2.3. *Thermal stability*

The thermal stability of the various phases, studied by thermal programmed desorption (TPD) may be summarized as follows:

- the 1×1 dihydride phase is desorbed with second order kinetics with an activation energy E^*_{des}(1×1 H) of about 2.0 eV originating the β_2 peak centred on a temperature of 425 °C;
- the 2×1 monohydride phase is desorbed with first order kinetics with an activation energy E^*_{des} (2×1 H) of (2.5±0.1) eV originating the β_1 peak centred on a temperature of 540 °C; and
- buried hydrogen is desorbed at ca. 630 °C originating the α peak.

The β_2 and β_1 peaks are generally explained on the bases of the scheme of Fig. 2. (This scheme is derived from the kinetic behaviour. Evidence based on STM suggests however a different mechanism for the β_2 emission, where the desorption occurs from the combination of two hydrogen atoms on the same silicon. Even assuming the validity of this conclusions, the forthcoming conclusions are not modified if the desorption is immediately followed by hydrogen shift from a neighbouring silicon dihydride to the silicon diradical).

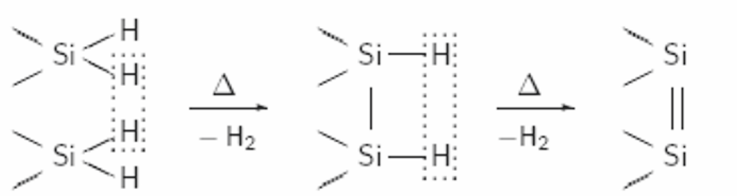


Figure 2. The scheme accounting for the β_2 and β_1 peaks in thermal programmed desorption from hydrogen-terminated silicon

The assumption, that the rate-determining step of both β_2 and β_1 desorption is the concerted cleavage of two silanic bonds and the simultaneous formation of a hydrogen molecule, explains not only why the corresponding activation energies are nearly equal, but also their values:

$$E^*_{des}(1\times1\ \mathrm{H}) \approx E^*_{des}(2\times1\ \mathrm{H}) \approx 2\,E_b(\mathrm{Si–H}) - E_b(\mathrm{H–H}) \approx 2.4\ \mathrm{eV}$$

The value of $E^*_{des}(1\times1\ \mathrm{H})$, somewhat lower than that of $E^*_{des}(2\times1\ \mathrm{H})$, might be explained assuming that even the formation energy of the Si–Si bond brings a contribution to the energy balance.

If the scheme of Fig. 2 is correct, the areas A_2 and A_1 of the β_2 and β_1 peaks determine the initial relative abundance f_2 / f_1 of the dihydride phase to the monohydride one: $f_2 / f_1 = A_2/(A_1–A_2)$. If the surface is completely covered by hydrogen, then $f_1 + f_2 = 1$ and

$$f_2 = A_2/A_1 \tag{5}$$

A generally accepted model for the centre responsible for the α phase is not known yet; on phenomenological bases, however, the α peak is substantially the same as that observed for TPD from hydrogen-implanted silicon[26]. Since implanted hydrogen forms nanoscopic cavities[27], on analogical bases the α peak may thus be attributed to the desorption from hydrogen-decorated cavities in the subsurface region.

The greater thermal stability of the 2×1 monohydride phase than that of the 1×1 dihydride phase does not imply an analogous greater chemical stability in air. In fact, both the 2×1 H and 1×1 H (1 0 0) Si surfaces, provided they are accurately prepared[28,29], show evidence for oxidation only after an exposure to air on a time scale of $10–10^2$ h.

3.3. THE SURFACES RESULTING AFTER EXPOSURE TO MOLECULAR HYDROGEN AT HIGH TEMPERATURE

Needless to say, the process described in parts 3.2.1 and 3.2.2 and involving the heating in an UHV and exposure to atomic hydrogen is unpractical and of difficult industrialization. This explains the efforts addressed to setting up an industrial process for the preparation of hydrogen-terminated (1 0 0) Si from the rough native surface.

Processes satisfying this condition have indeed been developed and involve the exposure of the native surface to molecular hydrogen at moderate-to-high temperature (800–1100°C). Irrespective of mono- or di-hydride terminations, baking in H_2 is associated with a reduction of the surface roughness and the formation of a terraced structure. If the process is carried out below 900 °C, it is limited by surface diffusion[30] and does not involve any appreciable etching of the surface[29,30].

3.3.1. *The 2×1 H phase*

Actually most papers report that the exposure of HF_{aq}-etched (1 0 0) Si to H_2 at sub-atmospheric pressure (in the interval 10–10^2 Pa) and high temperature (in the interval 800–1100 °C) followed by slow cooling to room temperature in the same environment results in the 2×1 monohydride phase[30,31].

The 2×1 H phase is formed during the cooling stage[30], so that the rationale of this process is the following: the high-temperature treatment is addressed to flatten the surface; the H_2 environment in the stage at high T prevents the surface from oxidation; and H_2 environment in the cooling stage controls surface reconstruction and termination.

3.3.2. *The 1×1 H phase*

Recently, however, evidence (based on reflection – high energy electron diffraction, thermal programmed desorption, infrared absorption spectroscopy in total attenuated reflection mode, x-ray photoelectron spectroscopy, scanning tunneling microscopy) has been presented for the 1×1 dihydride phase. This phase is obtained when baking in H_2 is followed by a sudden quenching to room temperature (for instance, by transferring the sample in an N_2 environment) and exposure to air[29,32,33]. That this process leads indeed to the dihydride phase is confirmed by the TPD spectrum of Fig. 4, showing that the β_2 and β_1 peaks have nearly the same area, so that Eq. (5) gives $f_2 \approx 1$.

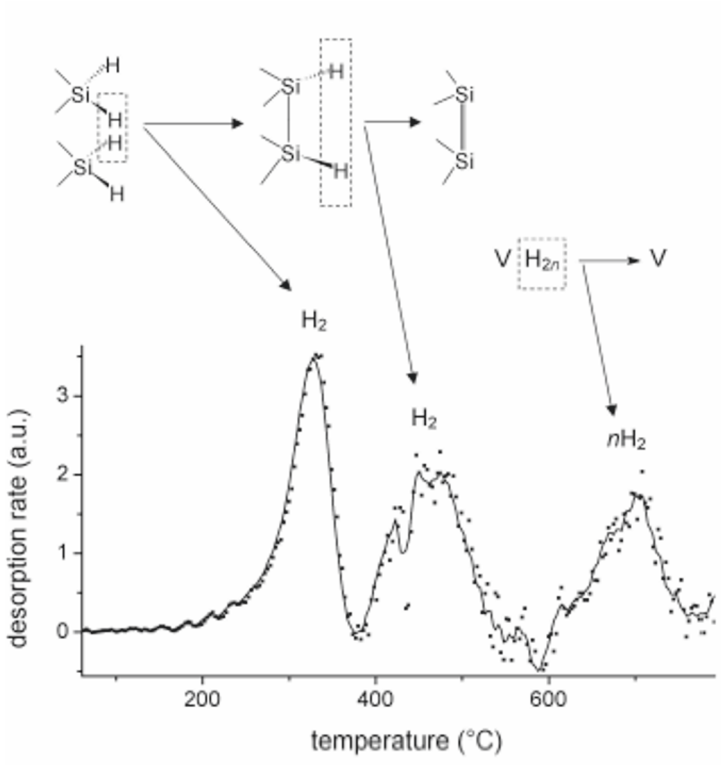


Figure 3. Desorption spectra from a surface prepared by exposure of (1 0 0) Si to H_2 at 1100 °C.

4. Silicon passivation

Although the hydrogen-terminated (1 0 0) Si surface is remarkably stable, it nonetheless undergoes oxidation in air. Its stability is controlled by the nature of terminations (mono- or di-hydride) and their defectiveness (dangling bonds or oxo groups). High-quality di-hydride terminations may resist in air up to 10^4 min without undergoing appreciable degradation. If greater stability is required, the surface must however be passivated with alkanic groups. The effect of these groups (which can be easily removed simply by oxidation) is to impose steric hindrance to the adsorption of water and to inhibit the adsorption of further hydrocarbons (of unspecified nature) from the atmosphere.

For the derivatization of the silicon surface it is convenient to start from a high quality hydrogen-terminated surface. Several routes have been hypothesized. Among them I mention: the silanization via reaction with chlorosilane-terminated[34] molecules and elimination of HCl or with azanes and elimination

of NH_3; the arylation via reaction with diazonium salts and N_2 elimination[35]; and the hydrosilation of alkenes[36,37]. Of them, the one involving the least aggressive pathway (and thus *a priori* the most compatible one with the numerous films, and especially the metal ones, characterizing integrated circuits) is certainly hydrosilation.

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CORRELATION BETWEEN DEFECTS, LEAKAGE CURRENTS AND CONDUCTION MECHANISMS IN THIN HIGH-K DIELECTRIC LAYERS

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Abstract. Results on leakage currents and conduction mechanisms in various high-k dielectric layers (Zr-, Hf-, HfTi-silicates and Ta_2O_5) are presented. It is demonstrated that small alteration of the dielectric composition results in significant difference in the leakage current level, polarity dependence and change in the dominating conduction mechanism. These differences are commented in terms of both band diagrams and defects in the dielectric films. A special attention is given to the influence of the defect nature, their density and spatial and energy location on the dominating conduction mechanism. Examples of defect parameters influencing the charge trapping in the high-k stacks are given. Qualitative models explaining the conduction properties of the structures are presented.

Keywords: high-k dielectrics, conduction mechanisms, defects

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1. Introduction

The scientific community is united about the urgent need for high permittivity (high-k) dielectric materials to replace SiO_2-based dielectrics. A number of materials were studied in search for the most promising alternatives to SiO_2 in the nano-scale regime (top-down microelectronics)[1]. Significant efforts were dedicated to find the most suitable fabrication techniques and technological schemes, including interface engineering and annealing steps. Along with all technological challenges to be solved a deeper knowledge of the structural, dielectric, and electrical properties of high-k materials is required. The need for a more thorough understanding of conduction mechanisms through the high-k gate stacks is required by two reasons: i) the investigation of leakage mechanisms could give valuable (albeit indirect) information on the defects as well as film structure; ii) there is a correlation between the leakage mechanism and reliability of dielectric as the degradation is a direct consequence from the leakage current through the film and the breakdown occurs after some critical level of generated defects in the film is reached. Therefore, it is very important to develop a fundamental understanding of the physical processes, which define the leakage mechanisms. This will allow making the conduction properties of high-k dielectrics more predictable, hence more controllable. In this paper, the leakage currents and conduction mechanisms in several high-k materials that are among the most promising for DRAM (Ta_2O_5) and CMOS (Zr-, Hf- and HfTi-silicates) have been investigated. The results obtained are summarized and conclusions concerning the influence of the defect parameters (density, energy and spatial location) as well as the intrinsic properties of the structures (composition, band structure) are drawn.

2. Sample preparation

Electrical measurements were performed on MIS capacitors manufactured on p-type (100) Si wafers. Surface conditioning in diluted HF was performed before deposition of the dielectric layer. Ta_2O_5 was deposited by rf sputtering of Ta target in a mixture of Ar and O_2 gases. The substrate temperature T_s during deposition was 293 or 493 K. After deposition, the samples were annealed at 873 or 1123 K for 30 min in dry O_2[2]. Al gate electrodes were evaporated to form MOS structures. The Zr-, Hf-, and HfTi-silicate layers were deposited by MOCVD using single source precursors[3]. The deposition was performed at 823 K in Ar/O_2 ambient followed by a rapid thermal annealing (RTA) in O_2 at 1173 K for 10 s. Stacked gate electrodes (Ti(20nm)/Al(500nm) for Zr- and HfTi-silicates and Ni(20nm)/Al(500nm) for Hf-silicate samples) were evaporated through a shadow mask.

3. Results and Discussion

3.1. INFLUENCE OF DEFECT PARAMETERS ON CONDUCTION PROPERTIES

The I-V characteristics of Al-Ta_2O_5-Si structures before and after oxygen annealing (OA) are shown in Fig. 1. Table 1 summarizes several important parameters extracted from the C-V measurements. A lower fixed oxide charge Q_f ($<10^{10}$ cm^{-2}) and higher breakdown field E_{BD} after OA (the effect is more pronounced for the higher annealing temperature) are detected[2,4,5]. The annealing is also highly effective in suppressing leakage current - the lowest current is obtained after OA at 1123 K. HR-TEM and XRD investigations[4,5] reveal that the as-grown as well as the layers annealed at 873 K are generally amorphous and the thickness of both Ta_2O_5 and SiO_2 are reduced. After OA at 1123 K, Ta_2O_5 crystallizes in an orthorhombic phase. As seen from Table 1, these samples exhibit more pronounced hysteresis ΔV_{FB} in the C-V curves as well as a change of its sign. We suggest that this is due to trapping at grain boundaries, i.e. the *crystal phase* electrically manifests as *slow states*[2,4]. Therefore, comparing the results presented in Fig.1 and Table 1 it is seen that there is a direct relation between the *density of oxide charge* and the leakage current – the reduction by one order of magnitude of Q_f after OA results in a dramatic improvement of the leakage current. The reduction of Q_f is related to the specific phenomena of high temperature OA: reduction of oxygen vacancies and bond defects, decrease in film stress, and better quality of the interface transition region at Si. At high temperatures, two concurrent mechanisms probably occur – reduction of both structural nonperfections and defects, and appearance of crystal phase(s). The results imply that the *poor oxidation related defects* are rather the dominant factor in the leakage current than the crystallization effects – the lower leakage currents are observed for the crystallized Ta_2O_5. The dominant conduction mechanism for the as-deposited layers is found to be due to Poole-Frenkel (PF) effect in the field range 0.4-1.3 MV/cm. The mechanisms identified in the annealed Ta_2O_5 are generally attributed to Schottky emission at medium fields, (0.8-1.3 MV/cm) or PF effect for fields higher than 1.3 MV/cm. It may be concluded that there are two dominant conduction mechanisms in the medium field range for layers with different technological history: bulk-limited PF effect for the as-deposited and electrode-limited Schottky emission for the annealed films. In the as-deposited Ta_2O_5 the traps close to the Al-Ta_2O_5 interface act as "stepping" sites for electrons and in this way facilitate their transport through the oxide, i.e. the electron injection from Al into Ta_2O_5 takes place by tunneling of electrons from Al into traps and further the conductivity is governed by PF mechanism (Fig.2).

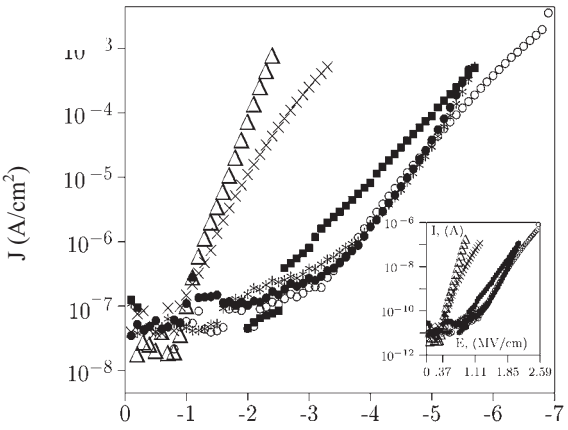


Fig.1

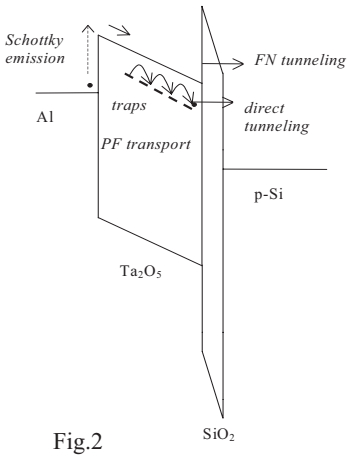


Fig.2

Figure 1. J-V characteristics of Ta_2O_5 films (d=26 nm) (inset, I-E characteristics); Ts=293 K - x- as-deposited, ○ - OA 873 K, ●- OA 1123 K; Ts=493 K - △ -as-deposited, ■ - OA 873 K, * - OA 1123 K.

Figure 2. Schematic illustration of the conduction mechanisms in Al- Ta_2O_5 - SiO_2 - Si structures.

The high temperature O_2 treatment anneals electron traps within Ta_2O_5 and hence the electrons could not tunnel through them in the Ta_2O_5 conduction band. In this case the electrons should acquire enough energy to accomplish Schottky emission above the barrier (Fig. 2). Therefore, it appears that the transition from PF to Schottky emission can be effectively controlled by means of appropriate technological steps.

Table 1. Parameters extracted from the high-frequency (1 MHz) C-V and breakdown voltage measurements of MIS structures with Ta_2O_5.

Sample parameters	As-deposited T_s (K)		OA, 873 K T_s (K)		OA, 1123 K T_s (K)	
	300	493	300	493	300	493
ε_{eff} / EOT (nm)	11.6/9.1	14.2/7.4	13.7/7.7	15.0/7.0	15.2/6.9	16.1/6.5
Q_f(x10^{10},cm^{-2})	20	60	~1	3	~1	~1
ΔV_{FB} (V)	-0.15	-0.15	<0.05	-0.15	+0.2	+0.3
E_{BD} (MV/cm)	2.4	2.0	2.6	2.5	3.8	3.4

To investigate the influence of the energy location of the traps on the conduction properties the I-V curves of Zr-silicate ($Zr_{0.82}Si_{0.18}O_2$) and Hf-silicate ($Hf_{0.86}Si_{0.14}O_2$) layers with similar compositions were characterized at

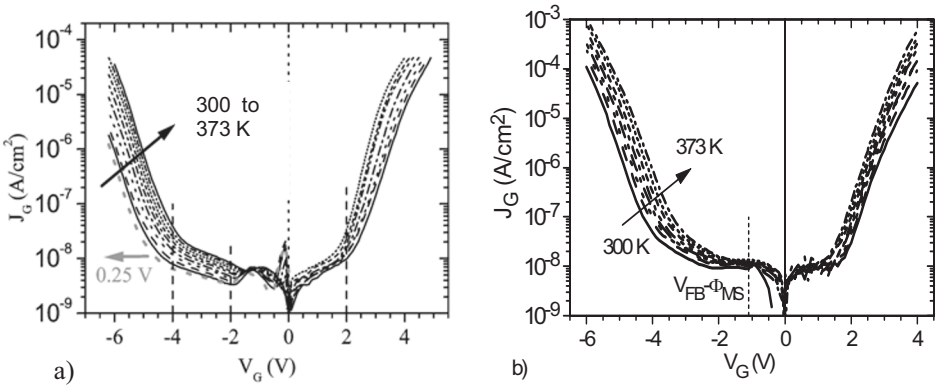


Figure 3. J-V characteristics measured at various temperatures for: a) $Zr_{0.82}Si_{0.18}O_2$ (d=18 nm); b) $Hf_{0.86}Si_{0.14}O_2$ (d=10.5 nm) samples.

different temperatures (Fig. 3). All measurements in inversion were performed under illumination to ensure a sufficient generation of minority carriers. Two different regions of the curves are clearly visible for Zr-silicate (Fig.3a): at higher fields (V<-4 V and V>2 V) the conduction mechanism is of PF type[6]. The determined trap energy Φ_b for both polarities is about 0.90 eV. For -4 < V < -2 V, the curves are well fitted by a trap-assisted tunneling (TAT) model[7] and the estimated trap energy is found to be about 1.5 eV below the conduction band edge of the dielectric[6]. Therefore, it emerges that the traps responsible for PF conduction and TAT are different. Figs. 4a,b show the band diagram of the structure at low and high electric fields and illustrate the correlation between the two different conduction mechanisms and the energy location of traps in the bandgap of dielectric[8]. Measurements at low temperatures show that the conduction mechanism undergoes a transition at about 150 K from PF emission

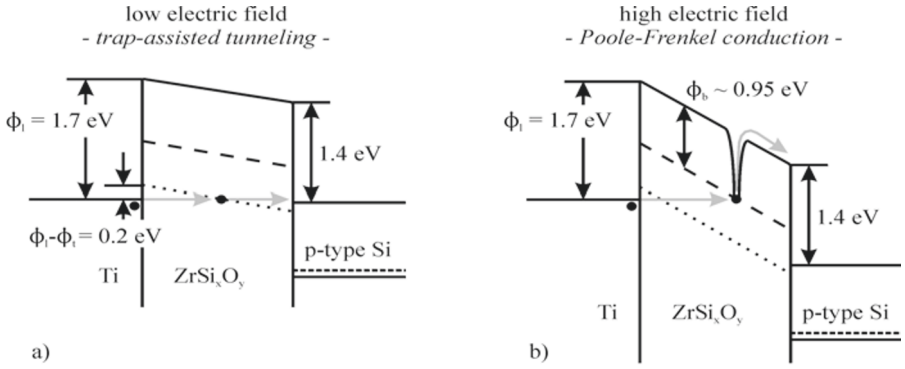


Figure 4. Band diagram of the Ti-$Zr_{0.82}Si_{0.18}O_2$-Si MIS structure and conduction mechanisms through it. a) Trap-assisted tunneling in the case of low electric fields. b) Poole-Frenkel conduction in the case of high electric fields. (ϕ_1 is the barrier height at Ti - $Zr_{0.82}Si_{0.18}O_2$ interface, ϕ_t is the trap energy level with respect to Fermi level of the metal electrode.)

to Fowler-Nordheim (FN) tunneling[8]. The obtained value of 1.4 eV for the barrier height at the Zr-silicate/Si interface is in a good agreement with theoretical calculations[9]. Two regions are also observed in the I-V characteristics of the Hf-silicate sample (Fig.3b). Between -2 and -3.5 V low

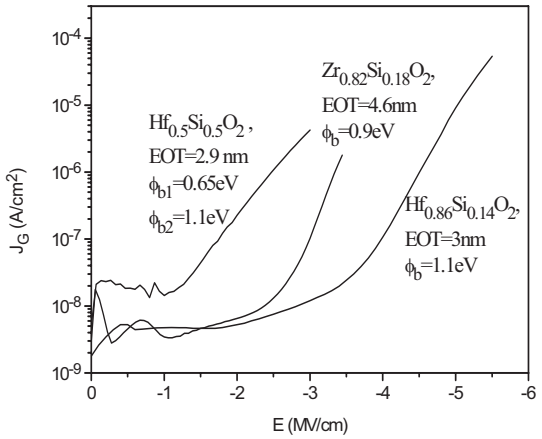


Figure 5. Comparison of J-E curves of MIS structures with different gate dielectrics having different trap energies.

current densities are observed. It is found that for V< -4.5 V (4 MV/cm) the main conduction mechanism at room temperature is FN tunneling[10]. The temperature dependence of the curves, however, implies the existence of another conduction mechanism in addition to FN tunneling. PF emission gives a substantial contribution to the conduction mechanism at elevated temperatures and for both gate polarities we found a trap energy Φ_b of 1.1 eV under the conduction band edge of Hf-silicate[10]. It is interesting to compare the I-V characteristics and conduction mechanisms of the Hf-silicate layers with different compositions with these of Zr-silicate (Fig. 5). It is seen that the deeper the trap level the higher the field at which conduction starts. For $Hf_{0.5}Si_{0.5}O_2$ sample, the dominant conduction mechanism at room temperature is found to be PF emission from traps with energy Φ_{b1}=0.65 eV. At T>373 K, another trap level Φ_{b2}=1.1 eV is also observed. The absence of 0.65 eV level in $Hf_{0.86}Si_{0.14}O_2$ sample most likely is the reason for the better I-V characteristics and the dominance of FN tunneling at room temperature. Comparing the results for $Zr_{0.82}Si_{0.18}O_2$ (Φ_b=0.9 eV, FN tunneling below 150 K) and $Hf_{0.86}Si_{0.14}O_2$ (Φ_b=1.1 eV, FN tunneling at 293 K) samples, it seems that a difference in the *trap energy* of about 0.2 eV causes an increase of more than 100 K of the temperature at which *transition from FN tunneling to PF emission* is performed. This is very important having in mind that FN tunneling is an electrode-limited conduction mechanism whereas PF is a bulk-limited one.

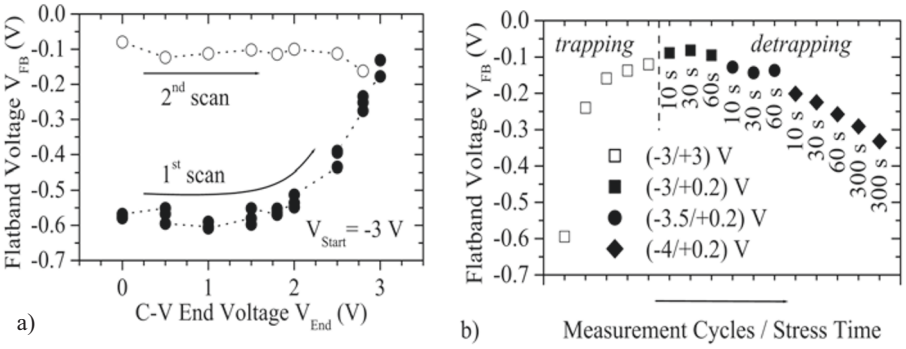


Figure 6. a) V_{FB} vs V_{end} of the last preceding C-V measurement of $Zr_{0.82}Si_{0.18}O_2$ sample; b) Change in V_{FB} after holding the sample in accumulation at different voltages for different times.

The existing traps give rise to flat band voltage V_{FB} instabilities. The V_{FB} of a C-V sweep is strongly influenced by the maximum voltage V_{end} of the last preceding C-V measurement (Fig. 6a, all measurements were performed on one capacitor starting at V_{end}=0 V). V_{FB} is nearly constant up to a V_{end} of 2 V. A further increase of V_{end} leads to a strong increase of V_{FB} (1st scan). This change is irreversible and the subsequent measurements (2nd scan) show a stable V_{FB} of about -0.1 V that means a build-up of a negative charge of about $2x10^{12}$ cm^{-2}. To obtain more information on electron trapping, we tried to detrap the trapped electrons. Successive (-3/+3) V C-V scans were performed to fill the traps (Fig. 6b). The first scan charges nearly all these traps implying that they are near the Zr-silicate/Si interface and their capture cross section is large. After that, the sample was kept in accumulation for different times and at different voltages and V_{FB} was determined again (with fixed V_{end} at 0.2 V, to prevent tunneling of electrons from Si). By stressing at -3 V for 100 s, it is not possible to detrap electrons (no shift of V_{FB} is observed). Keeping the structure at -3.5 V (100 s) and at -4 V (700 s) leads to a partial shift of V_{FB} back to its initial value, i.e. some of the trapped electrons are released. These results reveal that the emission time of the traps is substantially larger than the capture time.

3.2. INFLUENCE OF FILM COMPOSITION ON CONDUCTION PROPERTIES

In this section the strong influence of the layer composition on the conduction properties of the structures is demonstrated. The differences are discussed in terms of interfacial layer formation, band diagram and defects. HfTi-silicates with different Hf:Ti ratios (42:58; 27:73; 12:88; 0:100) in the film are studied and the I-V curves are presented in Figs. 7a-d. The assessment of the curves shows that the main conduction mechanism in Hf:Ti (42:58) sample (Fig. 7a) at both gate polarities is PF conduction[11]. The detailed discussion of the results[12] gives evidence that the trapping/detrapping of electrons near dielectric/Si

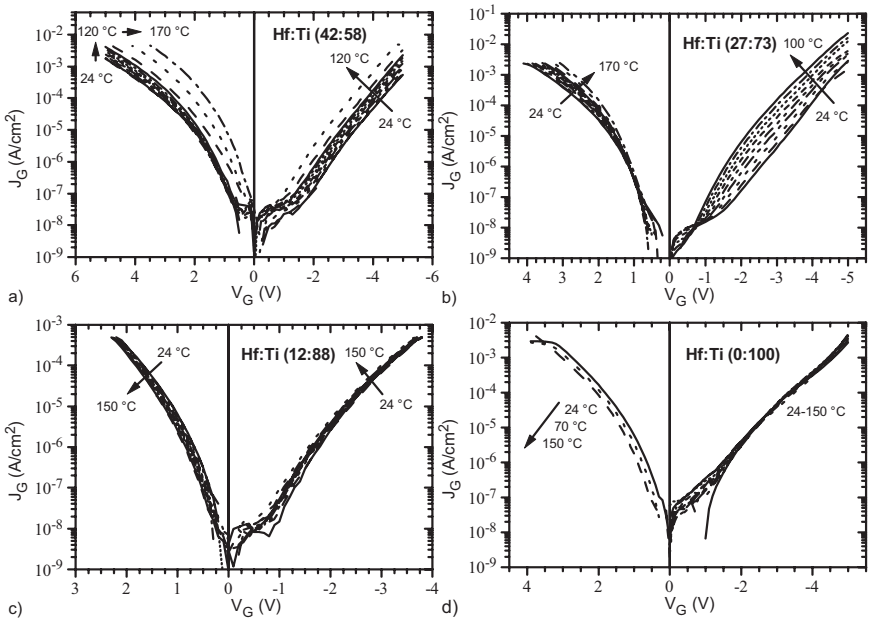


Figure 7. Temperature dependent Jg-Vg curves at two gate polarities for different samples: a) Hf:Ti (42:58) (d=23 nm); b) Hf:Ti (27:73) (d=31nm); c) Hf:Ti (12:88) (d=30 nm); d) Hf:Ti (0:100) (d=24 nm).

interface influences strongly the PF conduction at positive gate biases and is the dominating process giving rise to the *polarity asymmetry* of the curves. From the temperature dependence of the current, two different trap levels at about 0.65 and 0.9 eV are extracted[11]. There is evidence that the traps are non-homogeneously distributed throughout the layer with a density increasing toward the dielectric/Si interface. The effective density of the traps and their centroid from the interface with Si are estimated to be 5.6×10^{12} cm^{-2} and 9 nm[12].

At negative biases, the PF emission from a trap level of 0.9 eV is the dominant conduction mechanism for sample Hf:Ti (27:73) (Fig. 7b)[11]. Therefore, our results show that with the decrease of Hf content in the film a gradual change from PF conduction through traps with energy ~0.65 eV to PF conduction through traps with energy ~0.9 eV occurs. We suggest that the 0.65 eV traps are related to Hf-bonding, whereas the 0.9 eV traps are connected to Ti-bonding. The shape and temperature dependence of I-V curves of Hf:Ti (27:73) sample at negative biases are similar to these of Hf:Ti (42:58) (Fig. 7a) unlike the curves at positive biases that are more similar to the curves of Hf:Ti (12:88) and pure Ti-silicate (Figs. 7c,d). As will be discussed below for the sample Hf:Ti (27:73), the polarity asymmetry of the I-V curves could be explained only with an real asymmetry of the conduction process[12].

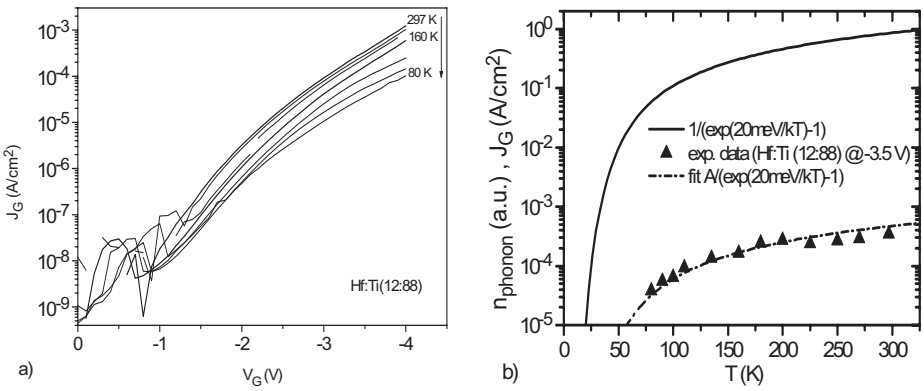


Figure 8. a) J_G-V_G characteristics at low temperatures for sample Hf:Ti (12:88); b) Comparison between temperature dependencies of the current in sample Hf:Ti (12:88) and the density of phonons with an energy of 20 meV.

Further decrease of Hf-content in the film (Figs.7 c,d), results in a qualitative change of the shape of I-V characteristics as well as their temperature dependence. The weak temperature dependence of curves excludes PF and Schottky emissions as possible conduction mechanisms. FN tunneling, which is known to be nearly temperature independent and hence the most reasonable candidate to explain these results, gives no accurate fit of the data. The I-V measurements at lower temperatures show that the current changes slightly down to 180 K and below this temperature it drops steeply and at 80 K it is an order of magnitude lower (Fig. 8a). This behavior is in a strong contradiction with defect-related processes. The activation energy E_a of the process governing the conduction is estimated to be 20 meV[11], which is in the energy range of soft optical phonons in high-k materials[13]. Therefore, the conduction mechanism in these layers is assumed to be governed by a phonon-assisted process. The high permittivity is due to highly polarizable, mainly metal-oxygen bonds[13]. Associated with these bonds are soft optical phonons. We suppose that the phonons with energy E_{ph}=20 meV interact with the electrons passing through the dielectric and influence the conduction mechanism. Proportionality between the phonon density and the current measured at various temperatures is established (Fig. 8b). This gives a straightforward evidence for the participation of soft optical phonons in the process. Conduction governed by a phonon-assisted tunneling between localized states in the bandgap of the insulator should obey the relationship $J \sim \exp(A/E^{1/4})$[11], which gives indeed a good fit to the I-V characteristics in the range from -1.5 to -4 V. This finding can explain the higher leakage current level in the films under consideration. For all commonly considered conduction mechanisms, i.e. PF emission, Schottky emission, and FN tunneling, the

carriers enter at some stage of their transport the conduction band of the dielectric and the conduction is performed in fact in this band. In the case of the phonon-assisted tunneling between localized states, the electrons do not enter the conduction band of the dielectric and the conduction takes place in the bandgap. Combined with the lower band offsets and bandgap this defines the higher leakage currents in the layers with higher Ti content.

The polarity asymmetry in the conduction process (samples Hf:Ti (42:58) and Hf:Ti (27:73)) can be explained with an asymmetry of the band diagram at the two interfaces combined with localized high densities of traps. The asymmetry of band diagram can be due to the formation of a thin interfacial layer with composition and/or structure different from the bulk film, which defines the dominating conduction mechanism. The formation of a double layer structure is rather due to structural changes at the interface than to formation of a separate interfacial SiO_x layer as a result of thermal instability of the film in contact with Si. In the later case, formation of such a layer should be observed also in samples Hf:Ti(12:88) and Hf:Ti(0:100) and should result in an even stronger polarity asymmetry of the I-V curves due to the larger difference between the bandgaps of silicate layer and SiO_x (with the increase of Ti content the bandgap and the band offsets should decrease). The following picture of the structural changes in the films is suggested. Islands of TiO_2, HfO_2, and SiO_2 have been formed near the dielectric/Si interface due to the phase separation, which can take place during the RTA in O_2[14]. An initial stage of phase separation most probably starts for films containing nearly equal amounts of Hf and Ti (Hf:Ti (42:58) sample) and is promoted by local fluctuations in the film composition near the interface. For Hf:Ti (42:58) sample, the islands formed are only inclusions in the amorphous network, which cause an enhanced trapping in the film and modify Poole-Frenkel conduction. The asymmetry of the I-V curves of the Hf:Ti (27:73) sample is assigned to the stronger phase separation near the dielectric/Si interface and formation of a separate interfacial layer. This layer affects significantly the conduction process at positive polarity in this way resembling the conduction process in the Hf:Ti (12:88) and pure Ti-silicate samples. In the last two samples, however, the island formation proceeds throughout the whole layer resulting in the symmetrical I-V curves. A more general conclusion is drawn that the separation process starts at the dielectric/Si interface and with the increase of Ti content it penetrates deeper in the bulk of the film until for Hf:Ti (12:88) sample a full phase separation throughout the whole thickness is obtained. Such a picture is in agreement also with the observed transition from PF emission to phonon-assisted conduction process when increasing Ti content in the film. The phonon modes depend strongly on the crystalline (amorphous) structure and the local bonding. The oscillations of oxygen ion in metal-O bonds give low energy modes, which

couple very effectively with thermal electrons[13] and define the phonon-assisted conduction mechanism. The increase of Hf content results in an amorphous structure and predominating metal-O-Si bonding. As the oscillations of metal-O-Si bonds are characterized with higher energy modes, which couple more poorly with thermal electrons, it is reasonable to expect that the phonon-assisted process will be weaker. Therefore, it appears that the *intrinsic properties* such as *phonon modes* contribute significantly and define the conduction properties of the film. In this sense, formation of silicate layers seems favorable, as the phonon-electron interaction in these materials is weaker.

4. Conclusion

The conduction properties of several high-k materials that are among the most promising for DRAM (Ta_2O_5) and CMOS (Zr-, Hf-, and HfTi-silicates) applications are investigated and commented in terms of both intrinsic parameters (composition, band diagrams and band offsets, phonon modes) and process-related issues (defects, microstructure, etc.). The strong relation and interplay between the parameters of the two groups makes the conduction behavior of each structure very complicated and non-trivial to predict. Nevertheless, several general conclusions could be drawn. Microstructural defects of various kind (structural non-perfections, stoichiometry related defects, phase separation, etc.) in high-k material as well as in the interface region at Si acting as electrically active centers are critical factor in achieving the requirements for high-k gate stacks, including low leakage currents. The defect parameters such as density, energy level and spatial location affect strongly the leakage current and define to a great extent the dominant conduction mechanism. By proper technological steps it is possible to achieve a certain control of the conduction properties of high-k gate stacks. For example, a reduction of oxide charge density by one order of magnitude is obtained by O_2 annealing of Ta_2O_5 layers and this results in a change of conduction mechanism from bulk-limited process to the desirable electrode-limited one accompanied by a reduction of leakage current by several orders of magnitude. The Hf-silicate exhibits much better conduction properties (lower leakage current, domination of FN tunneling at room temperature) compared to Zr-silicate with similar composition. This is assigned to the deeper trap level in the former. It appears that the difference of 0.2 eV in the trap energy location causes an increase of more than 100 K of the temperature at which transition from FN tunneling to PF emission is performed. In fact, FN tunneling is the most favorable case as it is defined only by the inherent properties of the structures. In some materials with higher permittivity (>20) and predominating metal-O bonds the phonon-assisted tunneling can influence substantially the conduction

properties. The intrinsic property of strong electron-phonon interaction in combination with the known decrease of band gap and band offsets with increasing *k* make the higher leakage currents more an intrinsic problem of these materials. The implementation of silicates with predominating metal-O-Si bonds is favorable in order to suppress the strong electron-phonon interaction.

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ELECTRONIC STRUCTURE OF ZRO_2 AND HFO_2

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Abstract. Band structures, density of states and effective masses of electrons and holes of cubic, tetragonal and monoclinic phases of ZrO_2 and HfO_2 have been calculated**.** Oxygen vacancy has been modeled by removing off one oxygen atom from 12-atom monoclinic cell. Incorporation of oxygen vacancy leads to formation of new filled sub-band formed mostly by d-electrons of the metals. Enormously high leakage current, observed in ZrO_2 and HfO_2 is explained by multi-phonon trap ionization model.

Keywords: high-k dielectrics; band structure, effective mass, defects, oxygen vacancy

1. Introduction

Hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) are the two most promising high-k dielectrics for application as gate oxides for future generation of CMOS with low tunnel leakage current and as insulators in memory capacitors of dynamic random excess memory (DRAM)[1,2]. Lately, these dielectrics were proposed as blocking oxides for silicon-oxide-nitride-oxide-silicon (SONOS) electrically erasable read only memory (FLASH EEPROM) for the future generation high-speed and low-power-consumption FLASH, including those based on silicon quantum dots[3,4]. The electronic and atomic structure of silicon oxide SiO_2, nitride Si_3N_4 and oxynitrides SiO_xN_y has been extensively studied during last four decades. However, much less is known about HfO_2 and ZrO_2

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electronic structure and defects in these materials. The purpose of this paper is theoretical study of HfO_2, ZrO_2 bulk and defects electronic and atomic structure.

2. Crystal structures and calculation technique

ZrO_2 and HfO_2 exists in three crystal phases: low temperature monoclinic (space group $P2_1/c$), medium temperature tetragonal (space group $P4_2/nmc$), and high temperature cubic (space group Fm3m). Crystal fragments of these phases are shown in Fig.1. Unit cells contains one metal and two oxygen

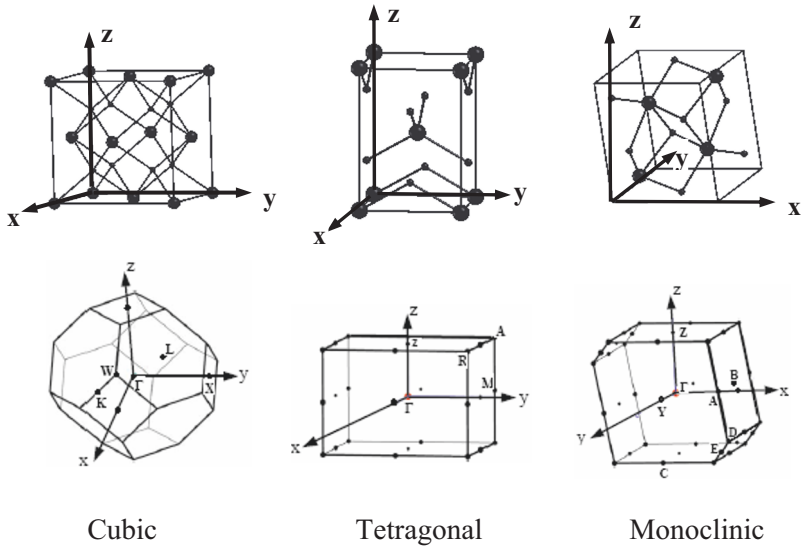


Figure 1. Crystal fragments and Brillouin zones of crystal phases of ZrO_2 and HfO_2. Small dark points in fragments represent oxygen atoms.

atoms for cubic phase, and two times and three times more atoms for tetragonal and monoclinic phases, respectively. The first Brillouin zones of the phases are presented in Fig. 1 also, under corresponding space fragments. We used lattice parameters and atom's position in the unit cells calculated previously for zirconia[5] and hafnia[6].

The most calculations of zirconia and hafnia electronic structure have been performed with Density Functional Theory (DFT) and plain waves (PW) as basis functions[5-12]. Core electrons were treated through pseudopotentials. Hartry-Fock approximation was employed early for ZrO_2[13]. In the present paper calculations were performed with DFT code ADF-BAND[14]. Local Density Approximation (LDA) was used for exchange-correlation potential. However,

Numerical Atomic Orbitals (NAO) calculated with Hermann-Skillman program[15] and Slater Type Orbitals (STO) were used for the basis functions instead PW. The potential of core states was treated explicitly within frozen core approximation. The total number of basis functions for unit cell was 75, 150 and 300 for cubic, tetragonal and monoclinic phases, respectively. Numerical integration was performed with 25000, 31000 and 40000 points in real space and 65, 125 and 17 points in irreducible wedge of Brillouin zone for cubic, tetragonal and monoclinic phases.

3. Electronic structure

3.1. CUBIC PHASE

Calculated band structures of ZrO_2 and HfO_2 are shown in Fig. 2. The both band structures are very similar. There are two valence bands. In both compounds the top of the upper valence bands located at X point of Brillouin zone and the

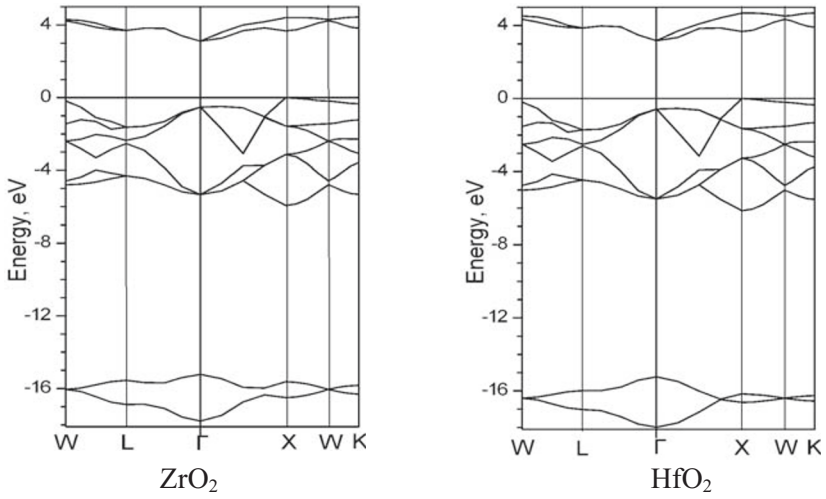


Figure 2. Band structures of cubic phases. Fermi energy is shown by streight line.

botom of the conduction band at Γ point. Corresponding densities of states are shown in Fig. 3. The bandgaps are 3.10 and 3.16 eV for ZrO_2 and HfO_2, respectively. The lower valence bands, located in energy region below

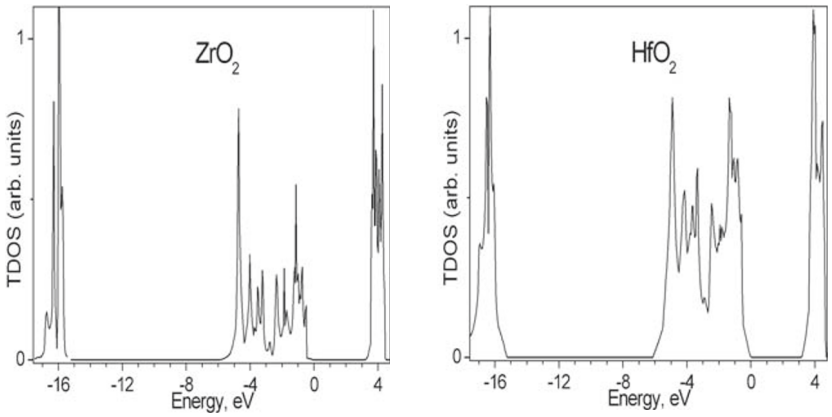
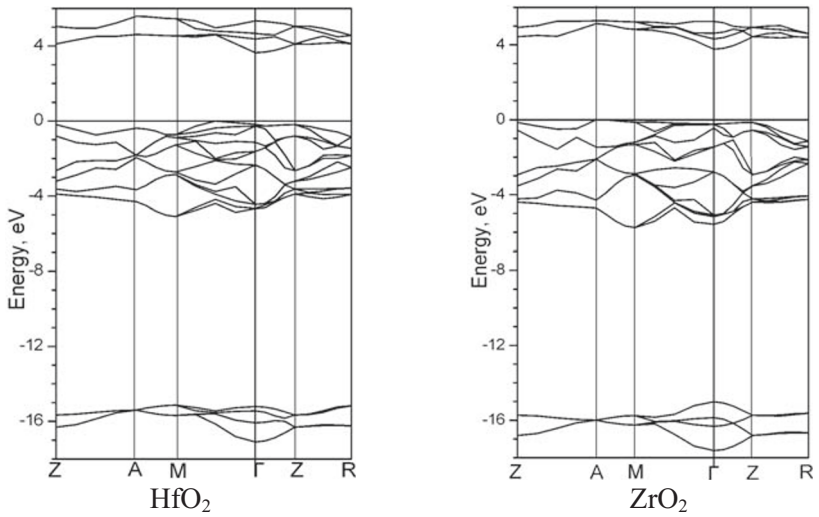


Figure 3. Total DOS for cubic phases.



Figures 4. Band structures of tetragonal phases.

- 15 eV relative to Fermi energy, are formed by O 2s orbitals , while upper valence band is formed by O 2p states with small admixture of metal d states. The conductions bands are formed by d states of metals. That means that valence bands in both ZrO_2 and HfO_2 are formed mostly by oxygen states, while conduction bands are formed by Zr 4d and Hf 5d states respectively.

3.2. TETRAGONAL PHASE

Band structures of tetragonal ZrO_2 and HfO_2 are shown in Fig. 4 and corresponding total density of states in Fig. 5. As for the cubic phase, the botom of conduction band is locates at Γ point, while the top of valence band at point A. Because the unit cell of tetragonal phase is two times larger than cubic, the band structure of the phase looks more complicated. Nevertheless, bands locations and conributions of different atomic states in DOS qualitatively are the same as for the cubic phases: the conduction band is formed be metal d-states, and valence bands by oxygen states. The width of the bandgap is 3.60 and 3.75 eV for ZrO_2 and HfO_2, respectively.

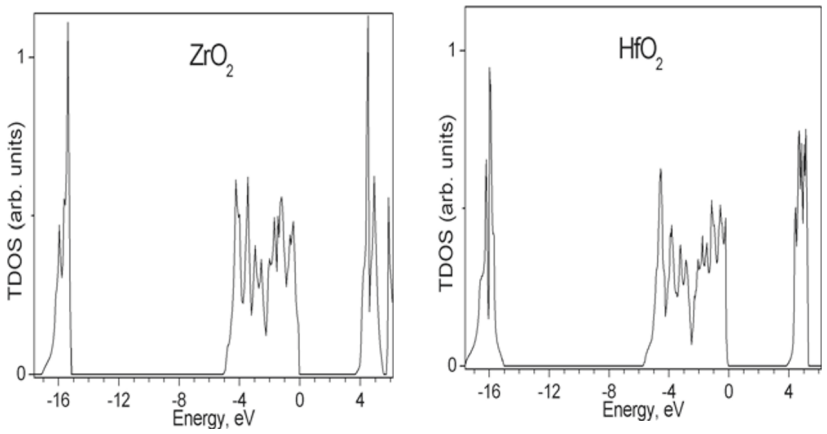


Figure 5. Total DOS for tetragonal phases.

3.3. MONOCLINIC PHASE

Band structures of monoclinic ZrO_2 and HfO_2 are shown in Fig. 6 and corresponding total density of states in Fig. 7. In both compounds the top of valence bands located at Γ point of Brillouin zone and the botom of the conduction band at B point. The bandgaps are 3.40 and 3.47 eV for ZrO_2 and HfO_2, respectively.

A compasion of the DOS of all calculated phases of zirconia and hafnia shows the similarity of the electronic structures in all these crystalls.

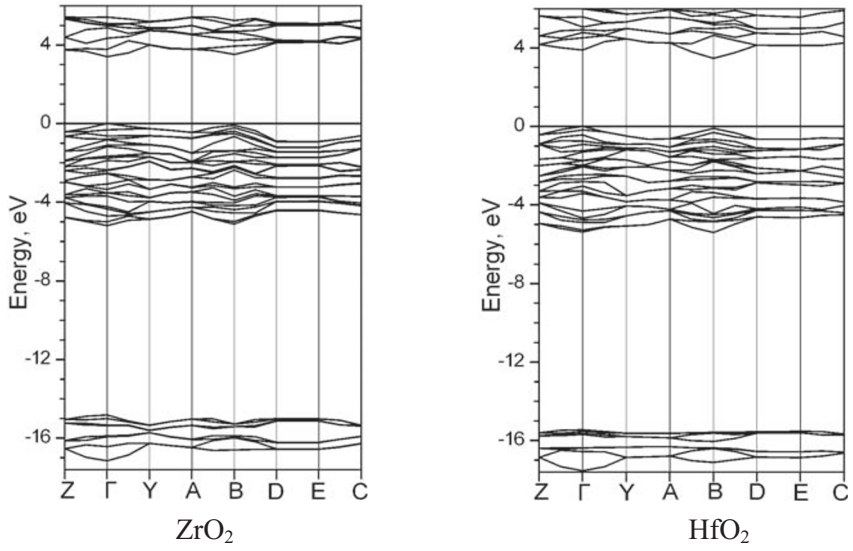


Figure 6. Band structure of monoclinic phases.

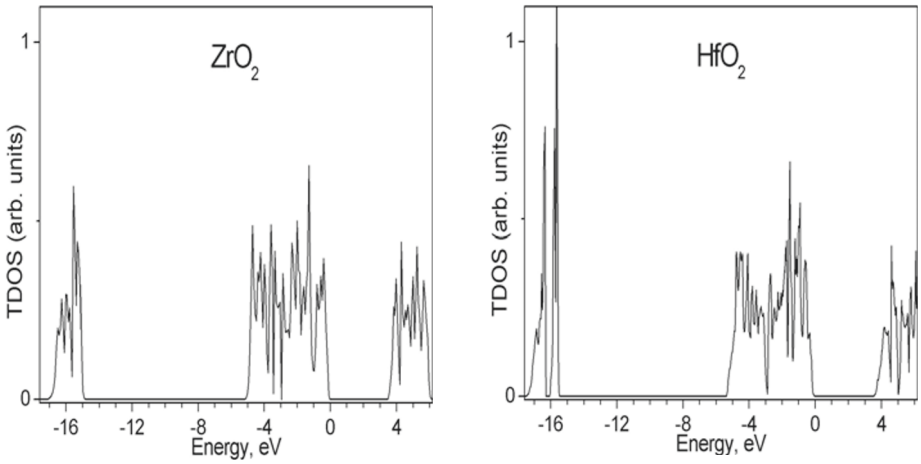


Figure 7. Total DOS for monoclinic phases.

3.4. OXYGEN VACANCY IN MONOCLINIC PHASE

In monoclinic phase there are two types of oxygen atoms: threefold and fourfold coordinated by metal atoms. Vacancy was created by removing off the threefold coordinated oxygen atom out of the unit cell.

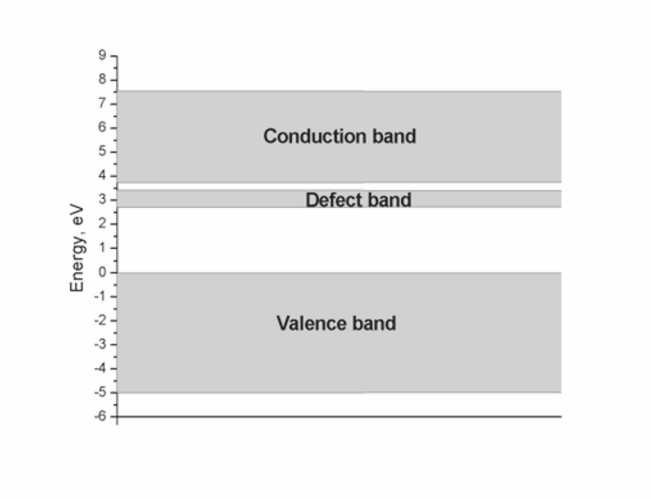


Figure 8. Energy diagram of monoclinic phase with oxygen vacancy.

Schematic energy diagram of crystall with defects is shown in Fig. 8. The principal change in band structure due to oxygen vacanies is appearing under the botom of conduction band a new filled sub-band which is formed predominantly by d-states of Zr or Hf. The sub-band is labeled in Fig. 8 as a defect band. The gaps between the sub-band and conduction band are 0.44 eV and 0.34 eV for ZrO_2 and HfO_2, respectively, with the width of 0.51 and 0.69 eV. Obviously, the defect sub-band width depends on vacancies concentration, and with reduction of the concentration it degenerates into vacancy level. Oxygen vacancies were studied previously for ZrO_2[5,7,8] and for HfO_2[6]. Cralic with coauthors studied oxygen vacancy in the ZrO_2 cubic phase, where one of eight oxygen atoms of 12-atom cell has been removed[8]. They found that vacancy incorporation leads to creation of a filled defect band below conduction band with the gap less than 1 eV (without GWA corrections). The width of the sub-band was more then 1 eV. These results are in satisfactory agreement with those obtained in the present paper. Supercell approach was used previously for oxygen vacancies study, where one oxygen atom has been removed from a 96-atoms supercell[5,7]. The position of energy level relative to the top of valence band was ≈2.2eV and ≈2.8 eV for zirconia and hafnia respectively.

We performed calculations of oxygen vacancies with plane–wave DFT code PWscf [16] for the two supercells with 24 and 81 atoms. The results for the 24-atoms supercell practically coincide with those obtained with BAND and for the 81-atoms supercell with those obtained by Foster and coauthors[5-7]. It means that discrepancy arise from different vacancy concentration. With increasing of concentration of oxygen vacancies, interaction between them leads to broadening of defect band and a small downward shift in energy.

4. Effective masses

To calculate effective masses the energy near a top of valence band and bottom of conduction band was approximated by quadratic form

$$E(k_x, k_y, k_z) = \pm\left(\frac{1}{2m_x}k_x^2 + \frac{1}{2m_y}k_y^2 + \frac{1}{2m_z}k_z^2\right),$$

where the wave vector origin is placed at the extremum point and signs + and – are used for electrons and holes, respectively. Calculated effective masses are presented in Table 1. The bottom of conduction band of the cubic phases at Γ point is formed by two degenerated states, splitting when going from this point.

Table 1. Effective masses

Masses	ZrO_2		HfO_2	
	Electrons	Holes	Electrons	Holes
		Cubic		
m_x	Γ: 0.7; 2.3	X: 0.4	Γ: 0.7; 2.0	X: 0.3
m_y	0.7; 2.3	3.3	0.7; 2.0	3.0
m_z	0.7; 2.3	3.3	0.7; 2.0	3.0
		Tetragonal		
m_x	Γ: 0.9	A: 1.6	Γ: 0.6	A: 0.7
m_y	0.9	1.6	0.6	0.7
m_z	2.5	2.2	1.9	8.26
		Monoclinic		
m_x	B: 3.1	Γ: 2.9	B: 8.2	Γ: 2.3
m_y	3.2	3.0	1.6	2.9
m_z	3.7	3.4	1.0	5.5

In the cubic phases there are two kinds of electrons with different effective masses, one less and another greater than free electron mass (Table 1). In cubic

phases of ZrO_2 and HfO_2 both electrons and holes effective masses are very close. Because of the top of valence band is situated at X point of the Brillouin zone, there is an anisotropy of hole's masses: masses in the plane perpendicular to ΓX direction are one order greater. In tetragonal phases of ZrO_2 and HfO_2 both electrons and holes effective masses are anisotropic. In this phase, electron effective masses are close for ZrO_2 and HfO_2, while difference in holes masses is large. In monoclinic phase, both electrons and holes effective masses for ZrO_2 and HfO_2 differ significantly and there is no electrons or holes lighter than free electron.

5. Charge transport in ZrO_2 and HfO_2

At room temperature, the charge transport in thick dielectrics with the contact barrier value in the range 2.0-3.0 eV is governed by the Fowler-Nordheim tunnel mechanism

$$J = F^2 \frac{e^3}{8\pi h\Phi} \exp\left[-\frac{4(2m*)^{1/2}\Phi^{3/2}}{3heF} \right]$$

Here J-current density, F-electric field, Φ-barrier value, m*- effective mass. The typical effective mass values in the well studied dielectrics such as SiO_2 and Si_3N_4 are $m^*_e \approx m^*_h \approx 0.5\ m_e$[17].

Experimental charge transport investigation in ZrO_2 and HfO_2 films was performed on MOS structures, based on both n- and p-type Si. It was found, that the conductivity of HfO_2 is dominated by electrons at both polarities[18]. Conductivity of ZrO_2 is two-band: at both polarities, from negatively biased contact injected electrons, from positively biased contact injected holes[19].

Enormously high charge injection level at contacts in MOS structures with both ZrO_2 and HfO_2 was observed. Fig. 9 shows the experimental current-voltage characteristics of n-Si/ZrO_2/Al MOS structures in accumulation (black line). Theoretical estimation of electron and hole current from Si in the Fowler-Nordheim approximation with effective electron and hole masses $m^*_e = m^*_h = 0.5\ m_e$ (dots) gives substantially lower current density compared with experimental data (see Fig. 9). To fit experimental data with theoretical Fowler-Nordheim curve enormously low effective mass (m*=0.0005 m_o) must be used. This effective mass value is three orders lower tan mass value predicted with band calculations (see Table.1).

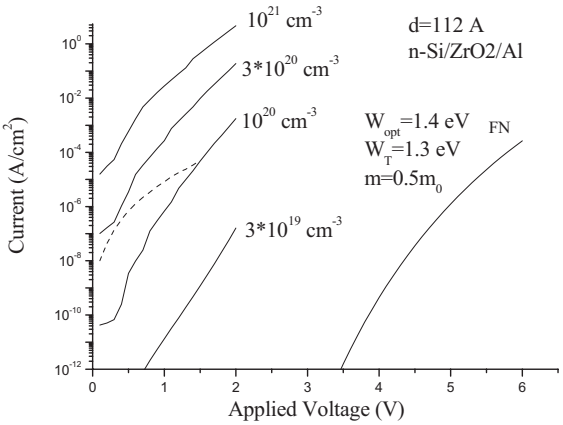


Figure 9. Theoretical current-voltage dependencies (solid lines) for different trap densities and experimental data (dashed line). For comparison the Fowler-Nordheim current is also shown (marked FN).

One of the possible reasons for abnormal high current in high-k dielectrics ZrO_2 and HfO_2 is high density of traps inside dielectrics. In this case carrier injection can be explained by direct carrier tunnel injection from contact to trap sites in dielectric volume and following tunnel transport between traps. We have developed the theory to describe processes of this kind, which based on phonon-coupled trap model[20]. Trap in this model is characterized by two trap ionization energies: optical W_{opt} and thermal W_T. The theory predicts that the role of tunnel transport between traps increases with trap density. The simulation results of current-voltage characteristics in ZrO_2 for W_{opt} =1.4 eV and W_T =1.3 eV are shown in Fig. 9 It is clear that, unlike Fowler-Nordheim mechanism, this approach capable to explain qualitatively the high current value in high-k dielectrics.

6. Conclusions

For band structure of ideal crystals we obtained for ZrO_2 and HfO_2 is close to other DFT calculations[5-11]. The calculated band gaps are less then experimental values and close to those obtained in most other DFT calculations except there RPA corrections to LDA were taken into account[5,8]. Band gaps calculated as difference of the total energies of systems with *N, N*+1 and *N*-1 electrons are also less then experimental values. Nevertheless, relative values of band gaps for different phases in calculations with and without RPA correction are the same: the cubic phase has the smallest band gap and the tetragonal

phases has the largest band gap. The band gaps of hafnia are a little larger then gaps of corresponding phases of zirconia.

The similarity of band structures of zirconia and hafnia is manifested in similar values of effective masses of holes and electrons. Both zirconia and hafnia in cubic phase has two types of electrons, with masses less and more than free electron mass**.** In tetragonal phase, there are both havy and light electrons with masses much less and more than free electron mass. In monoclinic phase there are only havy electrons. Holes are havier than electrons for monoclinic and tetragonal phase ZrO_2, while in the tetragonal HfO_2 there are directions with light and heavy holes.

Incorporation of oxygen vacancy leads in 12-atom monoclinic cell leads to formation of new filled sub-band formed mostly by d-electrons of the metals. However, the location of this band have to be recalculated more accurately, including for example many body effects through GWA corrections.

The observed enormously high leakage current in ZrO_2 and HfO_2 probably can be explaned by multi-phonon trap ionization model. We suggest, that traps in ZrO_2 and HfO_2 are related in oxygen vacancies.

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HIGH-K GATE STACKS ELECTRICAL CHARACTERIZATION AT THE NANOSCALE USING CONDUCTIVE-AFM

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Abstract. A purposely developed Conductive Atomic Force Microscope with enhanced electrical performance (ECAFM) has been used for the electrical characterization of HfO2/SiO2 gate stacks. The conduction of the fresh (without stress), electrically stressed and broken down stacks have been analyzed. The nanometer resolution of the technique and the extended current dynamic range of the ECAFM have revealed details that are masked during standard tests on gated devices.

Keywords: high-k dielectrics; electrical characterization; reliability; CAFM, ECAFM

1. Introduction

The replacement of SiO_2 as gate dielectric in MOS devices by materials with a higher dielectric constant (high-k) will allow to reach the required equivalent oxide thickness (EOT), but with a larger physical oxide thickness, which reduces the leakage current drastically[1]. Several candidates such as HfO_2[2], ZrO_2[3], Hf and Zr Aluminates and Silicates[4,5] have attracted the attention of the scientific community. However, before the effective substitution of SiO_2 in commercial IC's, the electrical properties and reliability of these materials must be well characterized. Much work is devoted to study the BD mechanisms[6,7] and degradation monitors, such as Stress Induced Leakage Current (SILC) and

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bulk trap density[8,9] in these stacks, which are expected to be dependent on the injection polarity[10].

Most of the knowledge about the electrical behavior of high-k materials has been gained from measurements performed on macroscopic MOS capacitors or transistors[2,3,11] using standard electrical characterization methods at wafer level. Although very important information has been obtained using these methods, this kind of tests provides a spatially averaged information on the electrical properties of the material. So that, the averaging effect can mask some degradation and breakdown related phenomena. On the contrary, Conductive Atomic Force Microscopy (CAFM) allows to characterize topographically and electrically the gate dielectric with nanometer resolution. The CAFM works on bare gate dielectric surfaces and the conductive CAFM tip plays the role of the metal gate of a nanometer sized MOS capacitor with an area of few hundreds of nm^2 [12]. With this set-up, IV curves, when the voltage is ramped and the tip is kept fixed on a sample position, and current maps, when the tip is scanned over the surface and a constant voltage is applied between tip and sample, can be measured. The CAFM has been already demonstrated to be very useful in the study of SiO_2 and high-k materials electrical properties. It has been used to measure the dielectric strength of SiO_2 gate oxides[13], local variations of the gate oxide thickness[14], the electrical degradation and breakdown of ultra thin SiO_2 gate oxide layers[15] and the effect of thermal annealing in the local conduction of high-k dielectrics[16], providing new data that could not be obtained before, using standard electrical characterization techniques. However, for reliability testing, the electrical capabilities of standard CAFM are not enough. The limited current measurement range (typically 3 orders of magnitude) is a major inconvenient, because the current evolution until breakdown (as function of time or gate voltage) cannot be fully measured in a single test. To overcome standard CAFM set up limitations, a prototype of CAFM with Enhanced electrical performance (ECAFM) has been developed. With this new set up, described in section 2, the degradation and dielectric breakdown (BD) of a HfO_2 /SiO_2 stack have been analyzed.

2. Experimental

HfO_2/SiO_2 gate stacks (EOT~1.2nm) have been studied. The stack consisted in a 2.5nm thick HfO_2 layer grown by Atomic Layer Chemical Vapor Deposition, on a 0.6nm SiO_2 interface layer (Rapid Thermal Oxidation). P-type silicon wafers (N_A~$10^{15}cm^{-3}$) were used as substrate.

As mentioned in the introduction, the technique used for the electrical characterization of the stacks has been an ECAFM[17]. The ECAFM can be

understood as a CAFM, where the means to bias the tip – sample system and to measure the current through the sample have been substituted by source monitor units (SMU). A SMU (typically included in semiconductor parameter analyzers) is a hardware that allows to apply voltage (current) and measure current (voltage) simultaneously, with a variable and auto selectable measurement range. With the new set-up the standard electrical tests on gated devices can be reproduced at the nanoscale. The current measurement range of the ECAFM is determined by the performance of the SMU, the electrical noise and the electrical characteristics of the ECAFM tip. In this work the ECAFM was equipped with CoCr coated Si tips. With these tips, currents from ~1pA up to ~1mA can be measured. In addition to the enlarged current dynamic range (when compared to a standard CAFM configuration), the ECAFM also provides more flexibility in the definition of tests. To show an example, a current can be forced through the structure while the voltage is measured, enabling constant current stresses at the nanoscale.

I-V characteristics were obtained from Ramped Voltage Stresses[18] (RVS). Each RVS consisted of a forward voltage ramp (increasing voltage from 0 to a voltage value V_G) and a backward voltage ramp (decreasing voltage, from V_G to 0). Constant voltage stresses (CVS) and constant current stresses (CCS) were also applied, to study the degradation of the stack. For all the measurements the tip was kept grounded, whereas negative voltages were applied to the sample, i.e. MOS capacitor is in inversion and injection is from the substrate. (experimental conditions are chosen so that deep depletion is avoided). Some I-V curves were obtained when injecting from the gate. However, very much lower current than expected was measured, probably due to the anodic growth of some Si or Hf related compound[19]. Therefore the CAFM does not allow to correctly characterize these ultra thin stacks at gate injection. However, SILC has been found to be larger during substrate injection[8], so that the set-up allows the worst case polarization for the stack reliability.

3. Electrical conduction of the fresh stacks

Previously to the study of the degradation and BD of the stacks, the fresh (without previous stress) structures have been electrically characterized. I-V characteristics and topography and current maps were measured.

I-V characteristics show different conduction regimes (Figure 1) for voltages larger than ~2V (for lower voltages, measured current corresponds to the noise level). From the first ramp (square line) it can be distinguished: a region where the current increases several orders of magnitude (regime A), a plateau region (in a log scale, regime B) and a region where the current increases again, but now in a noisy way, until a current jump occurs (regime C).

From the stack band diagram, regions A and B can be respectively associated to carrier injection through a triangular HfO_2 barrier (and through a trapezoidal SiO_2 barrier) and to carrier injection at energies above the barrier of the HfO_2 (see schematics inserted in Figure 1). The origin of regime C will be determined in section 5.

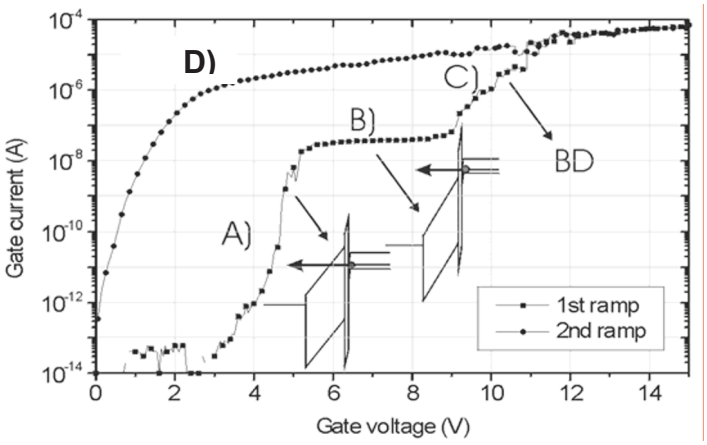


Figure 1. Representative I-V characteristic of a fresh 2.5nm HfO_2 / 0.6nm SiO_2 stack location, when a RVS is applied. Different conduction regimes and BD can been observed.

Fresh characteristic in Figure 1 is typical of a stack site, but small variations are observed from site to site, i.e., the stack conduction is not homogeneous. Although the shape of the curve is always the same, the voltages at which the different regimes are present can slightly vary from site to site. To provide some value, the voltage at which current is first seen above the noise level can vary within a 1V interval. The inhomogeneity of the conduction through the sample can be directly observed in the current maps, where leaky sites (locations that show larger currents) are randomly distributed on the device area (Figure 2.b). Note, however, that no remarkable feature is observed in the topography image (Figure 2.a), which shows a very smooth surface. This conduction inhomogeneity leads to the masking effect in standard electrical tests on gated devices, where thousands (or more) of these sites are stressed in parallel. This has been verified by adding hundreds of I-Vs, similar to the square-lined curve in figure 1[20].

A second I-V performed at the same location (Figure 1, circle line) shows a very different trend, and corresponds to a typical after-BD characteristic. RVS tests with different ending voltages have shown that the post-BD characteristic is only reached after measuring region C. Once the post-BD conduction is reached (regime D), consecutive RVS on the same site provide equal I-V curves, pointing out that a stable conduction mode has been reached. The post-BD behaviour of the stack will be studied in more detail in section 5.

Finally, note that the clear observation of the different conduction modes until BD (A, B, C) in the high-k stack has been possible due to the enlarged dynamic range provided by the purposely developed ECAFM (as compared to CAFM standard configurations) and the nanometer resolution of the technique. We will take advantage of this capability to study the degradation of the stack subjected to electrical stress in section 4.

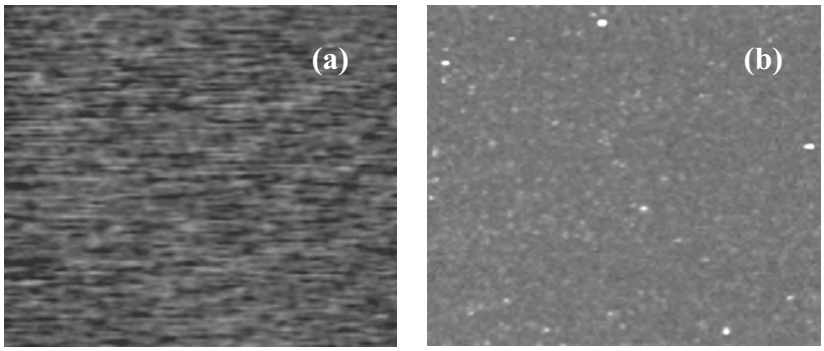


Figure 2. Topography (a) and current (V_{gate}=3V) (b) images measured on the fresh HfO_2/SiO_2 stack. Height range is from 0 (black) up to 0.2nm (white). Current range is from 50fA (noise level) (black) up to 1pA (white).

4. Degradation of the stack layers

As shown before, the ECAFM has allowed to clearly distinguish the voltage ranges where the conduction is controlled by the HfO_2 or SiO_2 layer (regimes A and B, respectively). Therefore, with this technique, the effect of the electrical stress on the conduction through the different stack layers can be separately analyzed, which will be indicative of the degradation induced by the stress. Sequences of RVS on the same stack location, CVS and CCS have been chosen to stress the structure. Low and high stress levels will be applied. This classification has been done by considering the amount of degradation that the stress is able to introduce in the structure, which will depend on the ramp rate and final voltage (for RVS) and on the duration and voltage/current stress values (for CVS/CCS). A RVS will be immediately applied after the CVS to monitor the effect of the stress. Topography images will be also sometimes recorded immediately after the stress. It must be considered that, apart from the intrinsic dispersion of the electrical data shown in section 3, an extrinsic dispersion is also present during CAFM experiments. The last dispersion can be related to the particular experimental conditions during a set of measurements (ambient, electrical properties of the tip, surface contamination…) which can alter the absolute values of the electrical magnitudes from data set to data set.

As for intrinsic dispersion, the shape of the curves is the same and only variations in the electrical magnitudes are measured (see for example figure 3a and 4 where the noise level differs in one order of magnitude and the voltage at which current is first observed above noise differs in ~3.5V). Therefore an absolute comparison of the data is only relevant within one particular set. To draw significant conclusions, the behavior of a fresh location of the stack will be considered as a reference to which the data obtained in stressed locations must be compared.

Figure 3a shows the I-V curves measured during a RVS sequence on the same stack location. The numbers indicate the RVS sequence order (number 1 corresponds to the fresh characteristic). The ending voltage of the RVS is located in region B, so that the effect of stress on regimes A and B can be observed. The voltage was increased fast enough to allow a small degradation of the stack, so that the stress level is low. The figure shows that the current level in region B remains nearly invariant during the whole sequence, i.e., the SiO_2 layer is not affected by the low level stress. Regime A is shifted in voltage, due to a modification of the conduction through the stack[21]. However, there is not a clear tendency for the direction of the shift, since it can take place towards lower or higher voltages. In order to explain the origin of these observations, related to the HfO_2 layer, the topography images measured after the RVS sequence have been analyzed and CCS have been applied in other locations of the structure.

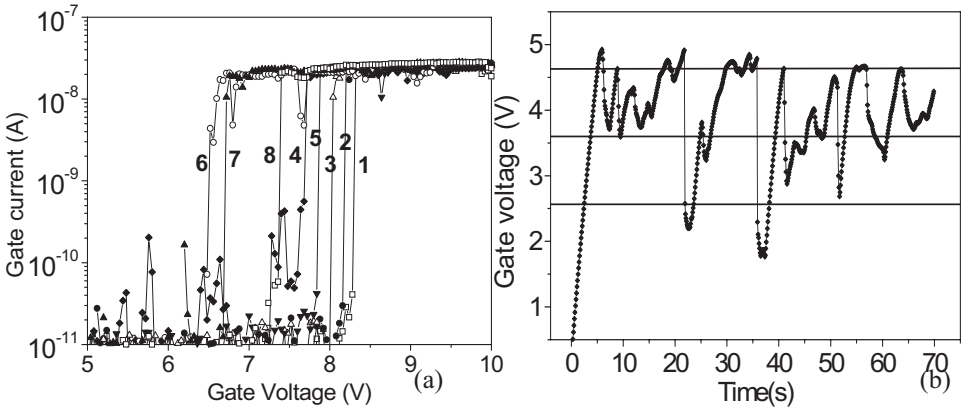


Figure 3. (a) I-V curves registered during a sequence of low stress level RVS (b) Voltage-time evolution during a low level CCS.

Figure 3.b. shows the V-t evolution measured during a 10pA CCS (stress current within regime A, so we are dealing with low stress levels). After an initial transient, switchings between different conduction states have been recorded, separated by approx. 1V, but there is not a net current increment. Similar switchings, which were related to the generation of defects during the

stress and charge trapping/detrapping from these defects, have been previously observed in SiO_2 layers with a C-AFM[15]. To determine whether this explanation could be also valid for the high-k stacks, the presence of trapped charge within the stack has been first corroborated by the topography images, since they show a hillock at the position where the RVS sequence or the CCS have been applied. Similar hillocks have been observed in SiO_2 layers after their BD, which were mainly attributed to an extra deflection of the tip due to negative charge induced during BD at the oxide BD location. From the hillock height, since the force constant of the CAFM cantilever is known, the amount of trapped charge was estimated[22]. Extrapolating these arguments to the high-k gate stack, from the topography images measured after the CCS tests, we have estimated that approx. 120 electrons are trapped within the high-k layer at the stressed position. Once the presence of some trapped charge in the high-k gate stacks has been demonstrated, the shifts in voltage during the sequence of RVS and the switchings during CCS at low stress levels (Figure 3) can be related to trapping/detrapping of elementary charges in the stack. In fact, electrostatic estimations show that the capture/release of an elementary charge in a trap site situated at the SiO_2/HfO_2 interface leads to changes in voltage of ~1V, as observed in Fig. 3b. These traps could probably be native defects, since there is neither a change in the shape of the I-V curve in region A nor a net increment of current during the CCS. Since this phenomena affects region A, these traps must be located in the HfO_2 layer.

Low and high level CVS tests (70 s long) have been also used to stress the structure. For the low stress level, 3-3.5V CVS have been applied (the voltage lies within region A, although current is still bellow the noise level), whereas 6-6.5V CVS have been chosen for the high stress level (voltage within region B). A RVS has been immediately applied after the CVS to monitor the effect of the stress. Figure 4.a. shows the I-V curves recorded after the low-level CVS. In this case, no increase in current seems to take place in region B, pointing out a small effect of the stress in the SiO_2 layer. The I-V curve in region A does not modify its shape, although there is a shift towards lower voltages. However, we cannot distinguish at this moment whether the shift is related to intrinsic dispersion of the data (conduction is not homogeneous, as shown before) or to the effect of stress.

Figure 4.b. shows the I-V curves measured after the high level stress. In this case, the behavior of both layers changes. Regime A (HfO_2 layer) shows a clear increment in current, which can be associated to generation of defects in this layer, leading to SILC. Region B also shows an increase in current and, when compared to the low stress level (figure 4.a), conduction is now much noisy, pointing out the progressive-BD of the SiO_2 layer[23], as discussed in section 5. Note that the transition from regime A to regime B does not change for any of

the curves. Although this observation needs further analysis, it could suggest that the generated defects mask the effect of trapping/detrapping in the as-grown defects in the high-k layer. If the stress level is further increased, the BD of the stack takes place.

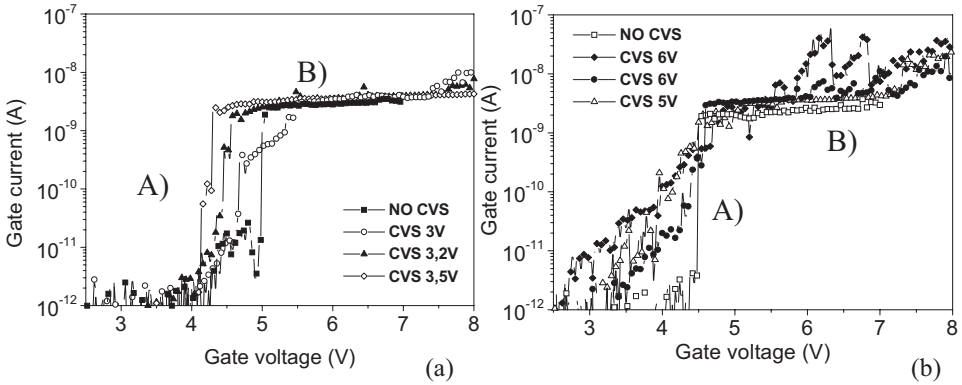


Figure 4. I-V curves after a CVS whose ending voltage lies within (a) region A (before current can be measured above the noise level), low stress level and (b) region B, high stress level. Each curve corresponds to a different stack location.

5. Dielectric breakdown of the stack

In this section, the behavior of the stack after its BD will be analyzed in detail. As described in section 3, once the BD of the stack takes place (regime D in Figure 1), a completely different conduction mode is reached and the three different regions (A, B, C) are not present anymore. When this curve is compared to that measured on a broken down SiO_2 layer of the same thickness (not shown), no differences are observed in the whole voltage range, pointing out that the stack BD is controlled by the SiO_2 layer and, after BD, the high-k layer is transparent to the flow of electrons.

The way a stable regime D is reached depends on the stack location. Actually, series of RVS on the same position have revealed two post-BD behaviors. For about 80% of the series the stack behaves as described in section 3: a stable conduction state is reached after the stack BD during the 1st RVS. We consider that an irreversible BD event has happened in this case. For the rest of the series, the successive forward ramps continuously evolve from the virgin curve (first I-V) to the post-BD characteristic (regime D). In this case, we consider that a reversible BD has happened. Figure 5 shows an example, where 5 consecutive RVS applied on the same site are included. Backward ramps (not shown) are always like curve D in figure 1, so that the stack conduction shows

hysteresis (similar to that observed in SiO_2 layers, when connected to a series resistance[24]). As the number of RVS (electrical stress) increases, region A is shifted to lower voltages. Since we are applying a high level stress (the final RVS voltage is very large and BD took place during the 1st RVS), this shift could be related to an enhanced tunneling current at lower fields due to the generation of defects during the stress (SILC) in the SiO_2 and/or HfO_2 layers, as pointed out in section 4. In region C the final post– BD current value is reached progressively. This behavior has been also observed using standard characterization techniques on gated ultra thin HfO_2/SiO_2 stacks[7]. Since the I-V characteristic of the stack in this region is determined by the interficial SiO_2 layer, region C could correspond to degradation and (progressive) BD[23] of this layer (which finally leads to the final post-BD state).

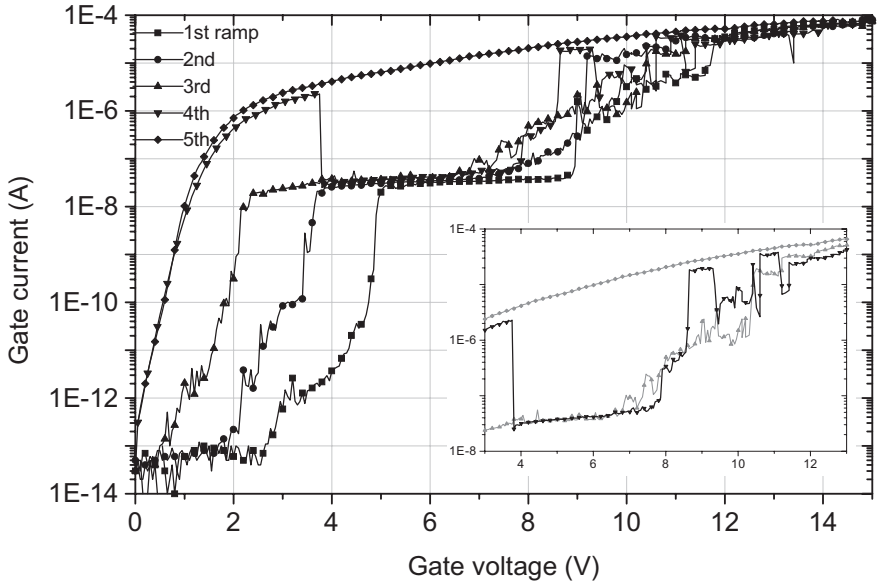


Figure 5. RVS sequence (only forward ramps are shown) for a location of the stack where a reversible BD has happened. The successive forward ramps continuously evolve from the virgin curve (first I-V) to the final post-BD characteristic. A zoom of 3rd to 5th ramp is included, showing switchings between different conduction states in the 4th ramp.

Finally, some times (4th ramp in figure 5) switchings between different conduction states are measured. From the zoom inserted in figure 5, it can be observed that the conduction during the 4th voltage ramp up to ~4V

corresponds to a typical post-BD I-V. At this voltage, the stack recovers the conductivity of a fresh location. As the voltage increases, the I-V curve enters region C. Several conduction switchings are also present in this region until the post-BD characteristic is reached. This kind of switchings has been observed using standard techniques[24,25] and CAFM[15] on thin SiO_2 layers and it is considered to be a consequence of the BD reversibility, i.e., a BD path has been created, but it can be switched on and off. Therefore, if we also take into account the observed hysteresis and the fact that the post-BD of the stack coincides with that of a single SiO_2 layer, we can conclude that the SiO_2 controls the BD of the oxide and the HfO_2 layer has a protective effect during the BD transient. Due to the HfO_2 current limitation, the BD path is not fully developed and a reversible BD event takes place. However, if the stress continues, the BD path is completely formed and the post-BD conduction (regime D) becomes stable and BD irreversible.

After the sequence of RVS, once BD has taken place, the region where the voltage ramps have been applied was topographically and electrically imaged. Low enough scan voltages were used, so that the electrical state of the stack is not modified during imaging. Topography and current maps exhibit modifications: at the stressed locations topography hillocks have appeared and their conductivity has dramatically increased[20]. This kind of behavior is analogous to that observed on SiO_2 layers after their BD[15]. From these hillocks, the amount of trapped charge after the high-k stack BD has been estimated. Considering that the charge appears at the HfO_2/SiO_2 interface, an average of approx. 130 electrons is trapped at the BD location. Note that this amount of charge is very similar to the one measured during the degradation of the stack, which was associated to trapped charge in the HfO_2 layer (section 4). Therefore, for high-k gate stacks the trapped charge in the SiO_2 layer after BD is negligible, when compared to the trapped charge in the HfO_2 layer.

CONCLUSIONS

An electrical characterization of HfO_2/SiO_2 gate stacks has been performed at the nanoscale, for the case of substrate injection. The extended electrical capabilities of a purposely developed Enhanced CAFM have revealed details on the electrical properties of the fresh stacks and their degradation and dielectric breakdown, which cannot be observed during standard electrical characterization techniques on gated devices. Current maps of the surface have shown that the conduction through the fresh device is not homogeneous. The capability of the ECAFM of measuring the I-V characteristics of the stack over a 9 orders of magnitude current range with nanometer scale resolution has shown different conduction regimes in the fresh stack, which are determined by

the conduction of the different stack layers. The observation of these regimes has allowed to separately study the effect of the electrical stress on the different stack layers. Low level stresses have shown that trapping/detrapping of charges in/from native traps in the high-k layer leads to variations in the current through the stack. When the stress level increases, SILC is measured through the SiO_2 and HfO_2 layers, pointing out their degradation. Moreover, progressive-BD of the SiO_2 layer is observed, prior to its final BD. The analysis of the post-BD characteristics has shown that the stack BD is controlled by the SiO_2 layer. Moreover, a hysteresis cycle and switchings between states with different conductivity are observed, which suggest that the BD can be a reversible phenomenon. This reversibility has been associated to the presence of the high-k layer, which acts as a protective series resistance for the BD of the SiO_2. When the BD path is completely developed, BD becomes irreversible.

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MAGNETIC DEFECTS IN PRISTINE AND HYDROGEN-TERMINATED NANODIAMONDS

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Abstract. Magnetic susceptibility study allows to make certain conclusions about the origin and location of itinerant and localized spins in carbon-based nanomaterials as well as their interaction between themselves. Nanodiamonds (ND) with the mean size about 4-5 nm is an interesting object for studying electronic and magnetic properties of diamond surface throughout its high specific area. Chemically modified ND particle is a very promising new unique material for applications in molecular nano-electronics. Results of recent magnetic studies of pristine and hydrogen-terminated ND samples, obtained by detonation technique, are reported and discussed. In addition to characteristic structural defects, originating from dangling C-C bonds of sp^3 sites and located mainly in the interior of the nanocrystals, the hydrogen-terminated ND crystals show a high concentration of excess stable free radicals (up to 10^{21} spin/g), which are due to structural defects (dangling C-C bonds) induced on the surface of diamond nanocrystals by hydrothermal treatment. Strong antiferromagnetic coupling is found between the spins localized on the surface.

Keywords: Diamond nanoparticle, surface modification, dangling bond, localized spins, magnetic susceptibility, antiferromagnetism, low temperatures, SQUID, ESR

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1. Introduction

Nanodiamonds produced in large amounts by the explosion method (detonation nanodiamond – ND) is one of the new kinds of nanocarbon substances which have been intensively studied since the middle of the 90th. [1] An unusual feature of ND is the small crystal size, with most particles varying between 4 and 5 nm. [2-4] Every particle of ND consists of a diamond sp^3- core of about 4.5 nm in size and a graphitic-like sp^2- shell covering the core. The shell thickness depends upon explosion conditions and chemical purification of the non-diamond forms of carbon on the ND particle surfaces.[5,6] High specific area of ND and the possibility to chemically modify the diamond surface give opportunity to use ND as a starting material for many applications in solid state and molecular nano-electronics. ND particles can also be used as a starting material to produce onion-like carbon by heat treatment.[7,8]

Chemical modification of the surface of nanodiamond (ND) particles is expected to give diamond-based functionalized electronic systems. In this paper, the ND particles with its surface hydrogen-terminated are produced, and their structural, electronic and magnetic properties are investigated by means of XRD, SAXS (small angle X-ray scattering), HRTEM, FTIR and Raman spectroscopes, ESR and magnetic susceptibility measurements. [9,10]

2. Preparation and Structural Analysis

ND samples prepared by detonation techniques and purified by different oxidizing agents were used as starting material. The surface of ND particles as prepared is subjected to structural reconstruction, which results in producing graphitic composites on the surface. Therefore, removing the surface graphitic composites is the requisite for chemical modification. It this study, hydrothermal (HyT) treatment in supercritical water was carried out for the purpose of hydrogen termination of the ND surface. ND particles were sealed with distilled water (in the mole ratio of ND:H_20 = 1:3) in a gold capsules and treated at 650^{o}C and 100 MPa during 1, 6, 12, 24, 36, 48 and 94 h. After hydrothermal treatment (HyTT) all the samples were dried and annealed in vacuum at 200 ^{o}C during 12 h.

TEM and XRD data show that in the as-received ND sample the scattering objects are diamond grains of ca.4.4 nm in size. The appearance of wide “G” and “D” bands around 1600 cm^{-1} and 1350 cm^{-1} in the Raman spectrum of non-treated ND demonstrated disordered graphitic carbon distributed on the surface of diamond core. According FTIR spectroscopy data different oxygen-containing surface groups are placed on the surface, and only traces of hydrocarbon fragments are registered.

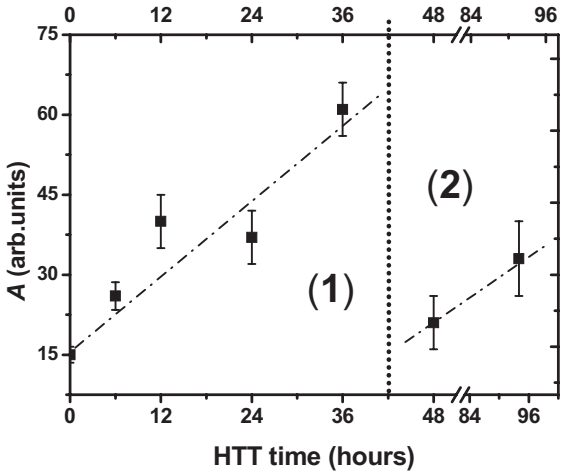


Figure 1. The HyTT time dependence of the intensity of the total absorption band A in the C-H stretching region at 2800-3000 cm^{-1}. A vertical dotted line divides two regions: the region of magnetic reconstruction (1) and surface reconstruction (2).

According to the SAXS data significant dissolution of amorphous shell covering the diamond core is observed after 24 h treatment of ND in water under supercritical condition. Raman spectrum of the ND HyT treated at 24 hrs shows a relatively narrow band near 1326 cm^{-1}, which is typical for ND phase, in addition to the "D" disordered peak around 1350 cm^{-1}, the "G" disordered peak around 1600 cm^{-1} and 1500 cm^{-1} peak, which are owing to the finite size of graphitic areas and bond-angle disorder [12].The reduction of some surface oxygen-containing groups to hydrocarbon species is also revealed by IR measurements. The intensity of the IR absorption near 2900 cm^{-1} can be related to the hydrogen content on the surface. Fig.1. gives the evolution of the intensity of total absorption band *(*A) in the C-H stretching region at 2800 - 3000 cm^{-1} as a function of HyTT time. As the HyTT time increases an increase in *A* is observed. Above 36 h, there is a large drop in the A values. And there is not much change in the number of C-H bonds after the long HyTT time (94 h). The concentration of localized spins N_s shows the same behavior (it will be shown later), suggesting incomplete saturation by hydrogen of bonds during dissolution of amorphous shell in an earlier HyTT stage (Region 1). Region 2 represents structural reconstruction of ND surface which reduces both the N_s and the number of C-H bonds. In the Raman spectra, bands at 1500 cm^{-1} and 1250 cm^{-1} were observed, in addition to the typical "G" peak and characteristic

peak of ND. These bands can be identified with the down-shifted "G" and "D" lines on the same value 100 cm^{-1} due to the surface reconstruction[12].

According to the above result, the reduction of oxygen-containing surface groups to hydrocarbon species under HyT conditions is revealed. Dissolution of graphitic-like shell covering the diamond core is strongly preferred by hydrothermal treatment and ND crystals with their surface being partly hydrogen saturated and graphitic-free are produced.

It should be noted that ND particles with graphitic-free surface have octahedral shape or cubooctahedral one in case if they are bound by eight (111) or additionally by six (100) crystal planes respectively, as mentioned in Ref.11.

3. Magnetic Studies

The results of recent magnetic experiments gave new insight to precise number and origin of localized spins on the nanodiamond particle.

The magnetic susceptibility and magnetization measurements on very pure pristine and hydrogen-terminated ND were carried out with a SQUID magnetometer (Quantum Design Co., MPMS-5) in the temperature range of 1.8 – 380 K in magnetic fields up to 5.5 T in vacuum. To avoid the possible effect of magnetic impurities on the experimental measurements, the nanodiamond powder was subjected to repeated chemical treatments in boiling 38% hydrochloric acid and then washed in boiling water before the hydrothermal treatment. This nearly totally removed the transition metal impurities usually present in commercial detonation nanodiamonds. Both the electron spin resonance (ESR) and the magnetization curves data were used to confirm the absence of traces of magnetic impurities in nanodiamonds.

The samples for the SQUID measurements were vacuum-sealed in tubes after the treatment at 400^{o} C for 4.5 - 5.5 hours at the vacuum level of about $(1.2 - 2.0)\times10^{-6}$ Torr.

Subsequent study of the magnetic properties on these samples shows that magnetic phenomena in pristine and hydrothermal treated ND are associated only with the localized defects with S = ½. The magnetization (M-*H*) curve of pristine ND measured at T = 1.9 K in magnetic fields *H* up to 5.5 T, is interpreted as being a sum of the temperature-independent linear (M-*H*) curve with a negative slope $\chi_o \times H$ (here $\chi_o = -0.38\times10^{-6}$ emu/g is very close to a core diamagnetic susceptibility of the carbon atoms) and the curve with a positive contribution of S = ½ (Figure 2). The latter being fitted to the Brillouin curve yields a concentration of localized spins of 6.3×10^{19} spins/g. No contribution to the magnetization curve due to transition metal ions impurities (spin value S > $^1/_2$) is observed. The concentration of intrinsic localized paramagnetic centers, estimated from the value of 6.3×10^{19} spins/g (assuming the average diameter

and the density of ND particles equal to 5.0 nm and the density of bulk diamond 3.52 g/cm^3, respectively), is found to be about 14 spins per nanoparticle. Such a small number of localized spins, as compared with the total number of the surface atoms in a particle indicates that the surface bonds of a diamond core are almost totally terminated with hydrogen atoms and radical-like paramagnetic centers observed are due to the point-like structural defects in/on the diamond core.[13-15]

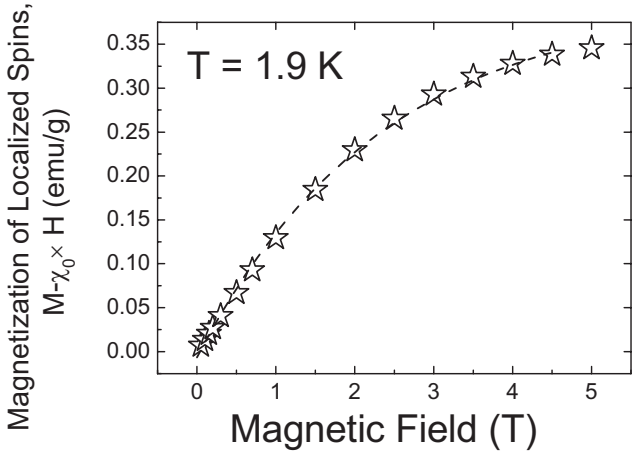


Figure 2. Magnetization curve of pristine ND at T = 1.9 K. Saturating trend in the high magnetic field indicates the localized spin feature. The contribution of $\chi_o \times H$ has been subtracted. The dashed line shows a Brillouin type curve for the least square fit. Fitting parameters – N_s = 6.3×10^{19} spins/g, S = 1/2.

The pristine and hydrothermal-treated NDs are studied by means of magnetic susceptibility χ measurements in the temperature range T = 1.8- 380 K. The temperature dependence of χ for all the samples is shown in Fig.3a in the coordinate scale $1/(\chi - \chi_o)$ vs. T. It is found that in the pristine ND and ND treated during 1-24 hrs of hydrothermal treatment the temperature dependence of magnetic susceptibility follows well or roughly well the Curie law, where the localized spins originate from dangling C-C bonds of sp^3 sites located mainly in the interior of the nanocrystals for the first case and also from the stable free radicals induced on the surface of ND crystals by HyT treatment for the second case. We can assign the excess spins induced by HyT treatment to ones predominantly localized on the diamond nanocrystal facets and least of all on the ribs. This is because in contrast to the interior of ND crystal the surface of

ND or its superficial layer are directly subjected to the active chemical interaction with supercritical water. The slopes of the curves shown in Fig.3a give information about the absolute value of localized spin concentration in the system. The HyTT time dependence of the localized spin concentration is shown in Fig.3b. The total number of spins per particle equals 13-14 in case of pristine ND. HyT treatment smoothly induces additional new spins on the surface of the diamond core and the number of these excess spins is linearly dependent on the treatment time and achieves ca.23 for the 24 hrs treatment. Here we assume that the actual number of surface spins per particle can be evaluated as a difference between the total numbers of spins per particle for the HyTT sample and the non-treated pristine one. This is especially true taking into account the stability and conservation of interior spins located in the ND core against HyT treatment, when the number of interior localized spins (13-14) remains the same during the HyTT.

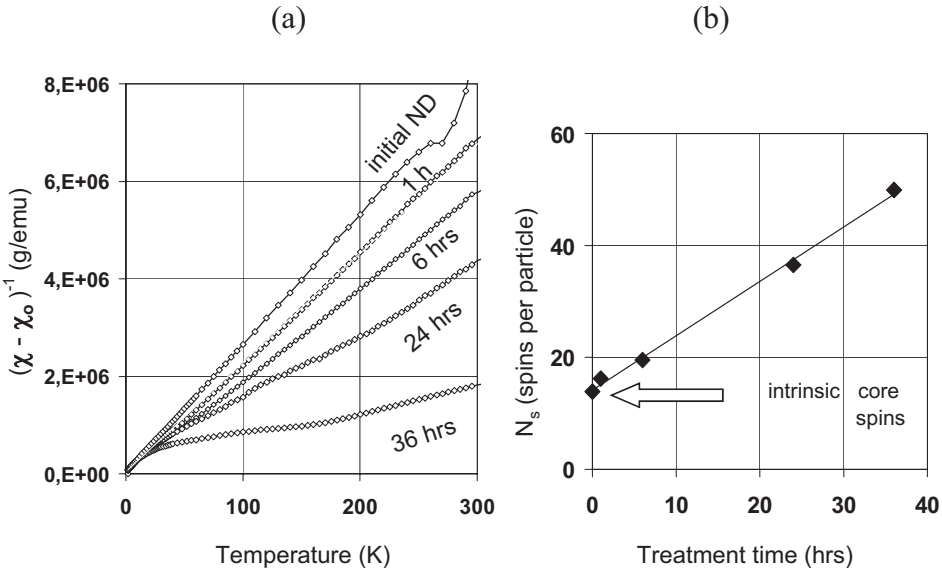


Figure 3. Dependence of 1/(χ - χo) vs. T (a) and the dependence of localized spin concentration Ns vs. HyTT time (b).

In order to produce any conclusion about the interaction between the spins induced by HyT treatment it is necessary to plot a dependence χ vs. T in the

coordinate scale $(\chi-\chi_o)\times T$ vs. T (Fig.4). The downturn on these curves in the low-temperature range means the presence of antiferromagnetic (AFM) interaction between the spins. The downturn for the case of pristine ND takes place in the range T < 40 K, therefore it means that exchange coupling between the spins becomes appreciable in the range of ca. 40 K. For the case of 24 hrs treated ND the downturn on the plot $(\chi-\chi_o)\times T$ vs. T takes place in the range below 200 K, suggesting the presence of a strong AFM coupling between the surface spins.

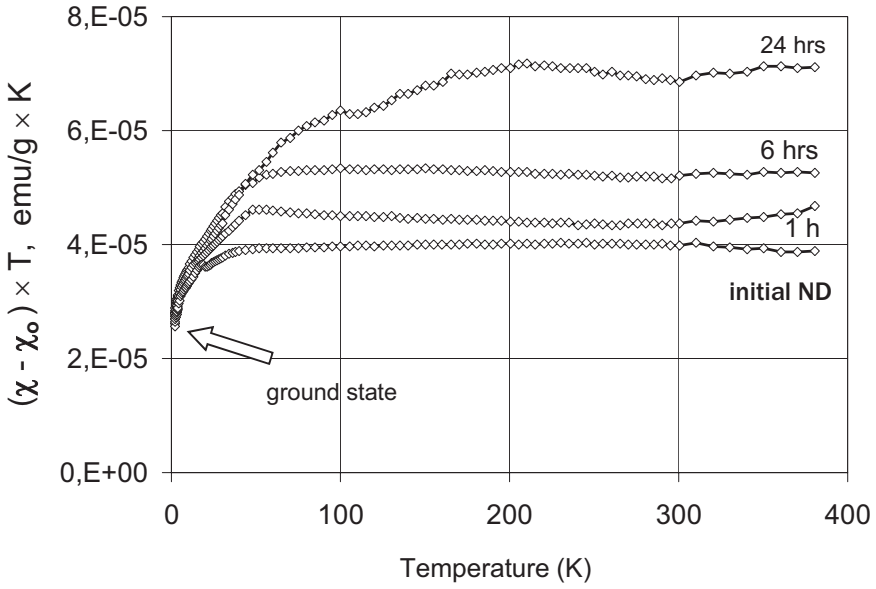


Figure 4. The dependence of product $(\chi - \chi_o)\times T$ versus T.

The specific features observed on the plots $(\chi - \chi_o)$ vs. T in the range below 70 K for the samples treated 1, 6 and 24 hrs can be related with the contributions from pairs and triads of surface spins $S=^1/_2$ antiferromagnetically coupled (dimers and trimers) to the total susceptibility. From the analysis of $(\chi - \chi_o)$ vs. T plot, we found that for the 24 hrs treated sample there are ca. 7 dimers per particle and the exchange constant is approximately $J / k_B \sim -50$ K, if we assume that the susceptibility behaviour can be explained only in terms of AFM dimers although the contributions of isolated spins, dimers, trimers, etc. one present. This conclusion is also well proved by the fact that the ensemble

average number of surface spins (or dangling bonds) laying on one facet equals ca.3 for the case the HyT treatment of 24 hrs if we assume that the nanocrystals have the form of an octahedron [11]. Here, the ensemble average number is easy evaluated by means of dividing the actual number of surface spins per particle (ca.23) by the number of facets of octahedron (8).

Thus, we consider that the increase in the 2D density of surface spins due to long time HyT treatment leads to the decreasing in the average distance between the spins and as a result, the enhanced AFM coupling appears.

The most dramatic change in the magnetic properties of the ND surface takes place at 36 hrs of the HT treatment, where the astounding amount of excess surface spins (ca. 40) is induced in addition to a large increase in the positive temperature-independent paramagnetic contribution (χ_o = 2.0×10^{-6} emu/g). In this special case the ESR line (g= 2.0026) broadens from 0.85 mT to 1.5 mT when the temperature decreases from 300 K to 4 K. The broadening of the ESR line means the appearance of internal exchange field throughout the AFM short-range ordering. The contribution of the surface spins to the total susceptibility ($\Delta\chi$) for the sample treated 36 hrs (plotted in the coordinate scale χ vs. T) demonstrates Pauli-like behaviour in the temperature range T > 100 K, which is very similar to the dependence χ (T) for the normal paramagnetic metals, and indicates that the surface of ND is metallic-like or conductive. We suppose that the development of metallic-like features at T > 100 K takes place before/at the beginning of the process of surface reconstruction where the multiple alternating chains –C=C-C=C- as a forerunner of the surface reconstruction appears on the nanosystal facets. It happens because the each two nearest C-C sp^3 dangling bonds recombine and form the one double C=C bond. Therefore, alternating chains –C = C– C = C– should appear on the crystal facets of ND particle at high level of surface spin concentration. The itinerant partially π- electron spin system is produced on the nanocrystal facets in this case (t > 30 hrs). Moreover, the $\Delta\chi$-T behaviour demonstrates Peierls-like transition at T ~ 70 K to the non-magnetic ground state of surface spins throughout their AFM short-range ordering.

Thus, the slight changes in the surface structure happening before/on the threshold of surface reconstruction lead to the appearance of Pauli-like temperature independent paramagnetic term in the magnetic susceptibility and the surface of diamond nanocrystal demonstrates metallic-like behaviour. That is why conclusion respecting the appearance of alternating chains –C=C-C=C- on the nanocrystal facets before/on the threshold of the surface reconstruction seems very reasonable.

Thus, it is reasonable to consider the giant positive value χ_o = $+2.0\times10^{-6}$ emu/g as a Pauli susceptibility contribution from the spins delocalized on the facets of nanocrystals within the size of linear alternating chains –C=C-C=C-.

Broad peak in DOS (with the width larger than the thermal energy kT) should appear in the bandgap of diamond after the prolonged HyT treatment of diamond surface (Region 1). Exchange interaction between the 20- 40 surface spins (Fig.3b) is probably enhanced throughout their mediation via the multiple alternating chains appearing on the nanocrystal facets before/at the threshold of surface reconstruction. By this way we can significantly change the magnetic properties of diamond surface by HyT treatment.

4. Conclusions

According to the XRD and FTIR data the dissolution of the graphitic-like shell covering the diamond core is strongly preferred by prolonged hydrothermal treatment and ND particles with their surface being partly hydrogen saturated and graphitic-free are produced.

The hydrothermal treatment induces additional spins ($S=^1/_2$) on the diamond nanocrystal facets and least of all on the ribs, where the number of these excess spins depends roughly linearly on the treatment time and achieves ca. 40 spins after 36 hrs. The susceptibility behaviour suggests the presence of a strong antiferromagnetic (AFM) coupling between the surface spins.

The appearance of giant Pauli-like paramagnetic term in the magnetic susceptibility for the samples treated long time proves the metallic-like behaviour of nanodiamond surface and the supposition respecting the appearance of plethora of alternating chains –C=C-C=C- on the nanosystal facets before/on the threshold of the surface reconstruction seems very reasonable.

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ON THE IMPORTANCE OF ATOMIC PACKING IN DETERMINING DIELECTRIC PERMITTIVITIES

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Abstract. The role of the network structure in determining the dielectric constant of binary and ternary oxide insulators is outlined. Seemingly anomalous behavior observed in rare-earth sesquioxides, Ta_2O_5-TiO_2 mixed oxides, lanthanum aluminate and dilute $Zr_xSi_yO_2$ is discussed in terms of the atomic structure. Physical examination of the relevant properties of these materials should lead to an understanding of how to engineer the dielectric constant.

Keywords: High-k, network structure, crystalline structure, dielectric constant, polarizability, molecular volume

1. Introduction

Despite a growing volume of experimental research designed to find dielectrics capable of addressing the requirements set down in the Semiconductor Industries roadmap[1] there is still no medium to long term solution for the gate oxide in metal-oxide-semiconductor field effect transistor (MOSFET) devices. Solutions may exist or the requirements may be relaxed for applications involving embedded capacitors and dynamic random access memory (DRAM) cells. For example, reactivity between the dielectric and the Si substrate will not be of concern as it is for the MOSFET where the insulator is in direct

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contact with the active semiconductor surface. Furthermore, appropriate metal gate electrodes may be chosen so as to minimize charge injection resulting from the insulator conduction band-metal conduction band barrier height and band offset[2].

Solutions for the MOSFET gate insulator have been primarily looked for beginning with simple binary oxides (M_xO_y), examples of these include[3-7] Ta_2O_5, RE_2O_3 (where RE implies a rare-earth ion), Al_2O_3, and ZrO_2 or HfO_2. These materials are beset with a variety of problems, however, such as hygroscopy, low Si conduction band-insulator-conduction band barrier height, low temperature recrystallization and subsequent grain boundary related leakage current or surface roughness issues, inadequate dielectric constant, etc., etc. A natural extension has been to begin to explore ternary compounds[8] such as $LaAlO_3$ whose nominal dielectric constant in the crystalline state is ~ 28. Again, there is evidence that in the amorphous phase which is desired for technological applications in order to avoid grain boundary effects, dielectric constants are generally < 20 and the material is subject to reaction[9] with Si when heated at elevated temperatures (for example, > 800°C).

It turns out that situations such as that for $LaAlO_3$ are not uncommon and that frequently the dielectric constant obtained in the amorphous phase of a material is significantly lower than that in the crystalline phase. Surprisingly, examples also exist, as we shall discuss, where substantially larger dielectric constants than expected may be obtained, both in amorphous and crystalline phases . We are naturally lead to ask the question why this comes about so that we might develop an understanding enabling us to design or engineer the material with the desired dielectric properties. Combining all this information leads us logically to the conclusion that time has perhaps come to endeavor to establish a deeper understanding of the relationship between the insulator dielectric constant and the atomic structure of the network of the insulator.

2. Basics of the dielectric constant

Before treating the specific case of binary or ternary oxides we introduce the underlying physical basis which will be used throughout our discussion of existing experimental results. Following the classical Clausius-Mossotti approach[10] for the dielectric constant, k, in terms of the molecular polarizability, α, and the molecular volume, V_m:

$$(k - 1)/(k + 2) = (4\pi/3)\, \alpha/V_m \qquad (1)$$

The polarizabilities have been tabulated by various authors[11,12]. If one extends the theory to more complicated molecules one can, to first order, develop an

approximate formula based upon a linear sum of the constituent "sub-molecules":

$$(k - 1)/(k + 2) = (4\pi/3)\,(c_1\alpha_1 + c_2\alpha_2)/V_m \qquad (2)$$

where we assume a complex molecule $M_xL_yO_{p+q}$ can be written as a sum of the component parts M_xO_p and L_yO_q with the concentrations, c_1 and c_2, as the weighting factors. Note that this heterogeneous model assumes the insulator is comprised of independent molecules so that the relevant polarizabilities are those related to the M-O and L-O bonds generally embedded in M-O-M and L-O-Lbridges. This model does not make allowance for those bridging bonds which interlink such as M-O-L. The model appears to work, however, for a surprisingly large number of complex materials[12].

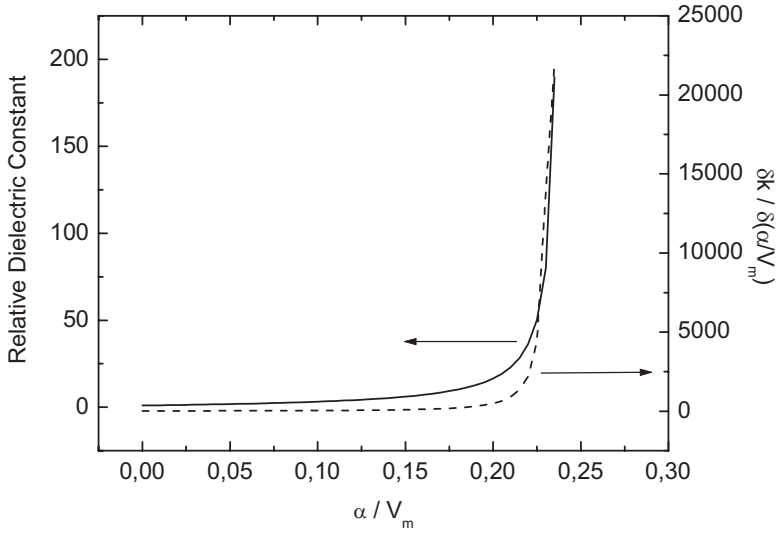


Figure 1. Variation of the relative dielectric constant, k, with α/V_m (solid line) and its derivative (dashed line) as calculated from Eq.(3)

Whether one considers Eq.(1) or Eq.(2), it is clear that the important parameter determining k is α/V_m and this underlines the importance of V_m i.e. the molecular volume or network structure. We can re-write Eq.(1) in a form which demonstrates the importance of α/V_m more rigorously:

$$k = [1 + (8\pi/3)\ \alpha/V_m]/[1 - (4\pi/3)\ )\ \alpha/V_m\ ] \quad (3)$$

In Fig. 1 we represent Eq.(3) graphically (solid line) and we include its derivative (dashed line) to show how rapidly k varies with α/V_m once the value of 0.2 is exceeded. The importance of network volume, V_m, which is inversely proportional to the network density, is clearly demonstrated in Fig. 1. One sees that, if the network volume decreases (the material density increases) then k will increase providing, of course, that any variation is not compensated by a variation in α.

The polarizability term, α, is complicated because, for the low frequency dielectric constant case, it is composed of an electronic term and a term related to vibrational properties of the network[13]. Only the electronic term is relevant for optical properties (for example, the refractive index) because the vibrational part cannot follow the associated high frequency fields. This can be written:

$$\alpha_{el} = 2 \sum [(0|e \sum x_i |j)(j|e \sum x_i |0)]/(W_j - W_0) \quad (4)$$

where the sums run over all electrons (defined by i) and all states defined by j. To a first approximation the vibrational part of the polarizability, α_{ion}, for a diatomic chain can be written:

$$\alpha_{ion} = e^2/(\mu_c V_m \omega_o^2) \quad (5)$$

where μ_c is the reduced mass and ω_o is a characteristic vibrational frequency of the chain. In Eq.(4), the denominator is essentially the insulator bandgap and this should decrease with the molecular volume or increasing density. This would lead to a decrease in polarizability with decreasing density. From Eq.(5) the vibrational part of the polarizability should also decrease when the density decreases so that both polarizability contributions are expected to decrease as the network density decreases. It turns out[13] that for at least two systems studied practically, SiO_2 and TiO_2, the opposite happens and in fact the polarizability increases as the density decreases. This means that other volume dependent factors in Eq.(4) and Eq.(5) have been neglected. At the present time we cannot simply predict the variation of α with density and we are forced to rely upon experimental determination. Fortunately, if the SiO_2 and TiO_2 data can be used as a guide, it would appear that the influence of volume reduction with increasing density outweighs any compensating effect due to α so that k increases (Eq.(3)) as V_m decreases.

The general conclusion of this section is that the dielectric constant increases as the network volume decreases. We are now equipped to research materials where important manifestations of this effect are apparent.

3. EXAMPLES OF REAL SYSTEMS

3.1. DILUTE AMORPHOUS SYSTEMS

The "dilute" alloy system which raised the most amount of interest and remains related to the probable choice for short term industrial development is based upon dilution of Zr in SiO_2. In fact, industrially, Hf in SiO_2 is the likely choice. However, whereas SiO_2 has a low frequency dielectric constant of 3.9, ZrO_2 has a crystalline phase constant ~ 26. The dielectric constant for the stoichiometric compound $ZrSiO_2$ is quoted as[14] 12 but the variation between pure SiO_2 and the stoichiometric compound is found to be supra-linear[14,15] and a dielectric constant of 11 is obtained for the mixed oxide $Zr_{0.15}Si_{0\cdot85}O_2$. The dielectric constant is thus enhanced since a linearly extrapolated value for this concentration should have been ~ 6. The origin of this enhancement has been much discussed but it turns out that the most probable cause is the network structure[16].

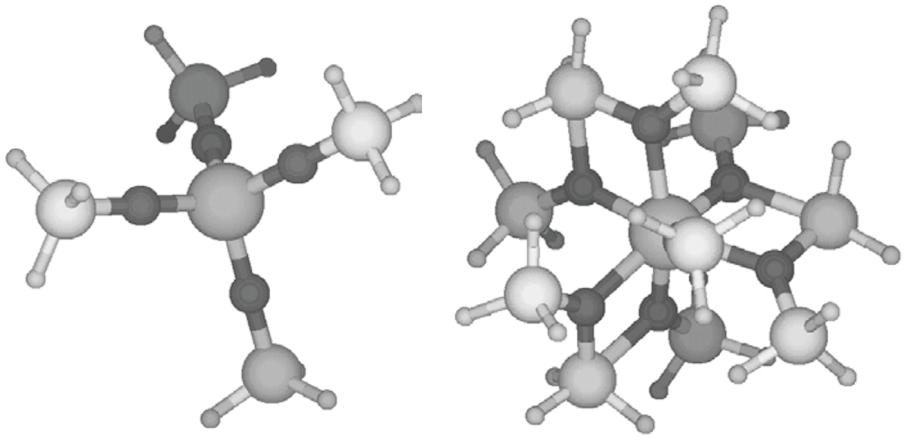


Figure 2. Atomic models used in calculations (reference 16) for Zr in SiO_2. (a) Four fold coordinated Zr (b) Seven fold coordinated Zr. The latter is the most likely in dilute concentrations of Zr.

Initial arguments suggested that Zr simply replaced Si in the SiO_2 network and that the O coordination around the Zr was 4. However, detailed X ray absorption fine structure measurements[17] provide evidence that in dilute mixtures of ZrO_2 and SiO_2, the coordination of the Zr ion is > 7. The consequences of this enhanced coordination were explored theoretically[16] and the nature of the problem resolved. In Fig.(2) we show atomic models of the 4 fold and 7 fold coordinated structures. One striking result is that when one examines the density of the network, one clearly sees that higher coordination numbers lead to much denser networks. The effective molecular volume thus decreases leading to this higher density. The effect on the dielectric constant can be easily anticipated from the arguments relating k to molar volume presented previously. For the moment the densification resulting from higher coordination in the mixed Zr_xSi_yO2 oxide has not been quantified but the atomic structures shown in Fig.(2) leave little doubt that this is indeed the explanation for k enhancement. In support of this it is further interesting to examine density/coordination relationships for known structures. Restricting ourselves to polymorphs of ZrO_2, we show in Fig.(3) a plot of molecular volume as a function of Zr coordination using data taken from reference 18. Though there is clearly a dispersion of results, one cannot avoid the general conclusion that as the coordination increases, the molecular volume decreases leading to higher density structures.

To our knowledge there are no other examples of “dilute” systems where the dielectric constant has been measured as a function of concentration so we proceed to examine the dielectric behavior of stoichiometric, concentrated mixtures or pure materials and how this is influenced by the internal structure.

3.2. CONCENTRATED SYSTEMS

The role of the network structure in determining the dielectric constant in concentrated oxide systems is extremely important to help our understanding of the physics even if these materials, because of crystallinity, may turn out to be unsuitable for technological purposes. In the following we will concentrate on various $M_xL_yO_z$ compounds.

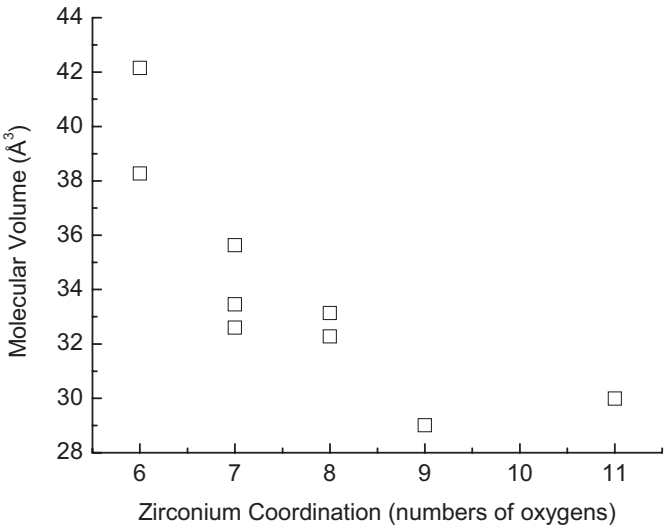


Figure 3. Variation of the molecular volume as a function of Zr coordination in ZrO_2 polymorphs (from reference 18).

3.2.1 *$LaAlO_3$*

The dielectric constant of crystalline $LaAlO_3$ is ~ 28 and this material would therefore appear to be an excellent candidate for applications as a replacement for SiO_2 as a gate oxide. However, efforts to produce amorphous $LaAlO_3$ have failed to yield films[19] with k > 13 despite earlier reports to the contrary[20]. Detailed investigation of the reasons for this "discrepancy" have revealed that the density of typical amorphous films is approximately 64% of the value of the crystalline phase. This alone is sufficient to justify a substantial reduction in the dielectric constant as is indeed observed. There is presently no atomic distribution data such as extended X ray absorption fine structure which can be

used to probe coordination, etc. However, it is worthwhile noting that in the case of SiO_2, amorphous SiO_2 has a density of 2.2 g cm^{-3} whilst the crystalline phase, quartz, has a density of 2.65 g cm^{-3} indicating that the amorphous phase density is 83% of the crystalline value. In the case of SiO_2 there is no coordination change so these numbers clearly indicate that substantial density differences may also occur between the amorphous and crystalline phases without the need to invoke coordination effects – simply the atoms are less densely packed in the network.

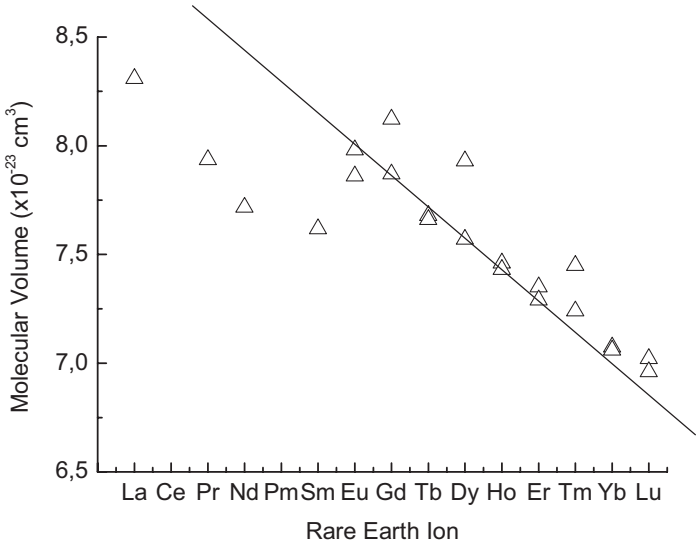


Figure 4. Variation of the molecular volumes as a function of ion in the rare-earth sesquioxide series of compounds. Different values for the same ion correspond to different density values available in the published literature.

3.2.2 *Rare-earth sesquioxides*

A significant effort has been made to study the dielectric properties of the rare-earth (RE) sequioxide insulators (RE_2O_3). Technologically, there materials are problematical because they are hygroscopic and react with Si at relatively low temperatures[21]. In general the dielectric constant measured[12] for the heavy RE sesquioxides (atomic numbers ≥ Gd) is ~ 12-13. The structure of these

materials is cubic. Though there have been relatively few measurements of the dielectric constants of the lighter RE sesquioxides, values do exist for La, Ce and Pr indicating substantially larger constants in the range 20-31. Why would this be the case ?

In Fig.(4) we plot the molecular volume for the RE sesquioxides as a function of RE ion. One observes that for the lighter RE ions there is a decrease in molecular volume and this is associated with the fact that the lighter RE sesquioxides form with a hexagonal structure[22]. It can therefore be anticipated that the dielectric constants of the lighter RE_2O_3 compounds will be larger than those of the heavier RE_2O_3' s because the molecular volumes are smaller. We have ignored potential variations in the molecular polarizabilities and we have no independent means to determine such variations. However, one can reasonably expect that any variation in the polarizability be monotonic across the RE series. Using the dielectric data and the molecular volumes determined in Fig.(4) we plot, in Fig.(5) the anticipated variation of the low frequency polarizability, α. The predicted values of α do, indeed, vary monotonically. We include in Fig.(5) data obtained from a similar analysis on RE garnets ($RE_3Ga_5O_{12}$) where there are no phase changes in the crystalline structure. The variation of α is again monotonic and similar, though different in absolute size, to that anticipated in the RE_2O_3 series but where a phase change does exist. This data gives further credence to the assumption that the significant difference in the dielectric constants of the heavy and light RE_2O_3 compounds is primarily related to the structure of the network.

3.2.3 *Ta_2O_5-TiO_2*

Tantalum pentoxide has been identified as a technologically useful dielectric in DRAM cell applications but not for applications as a gate oxide replacement in MOSFETs. The reason for the latter is the rather small insulator conduction band-Si conduction band offset (< 1 eV) which could lead to substantial charge injection from the Si substrate into the dielectric. In the amorphous phase the dielectric constant is found to be[23] ~ 25 whilst in the crystalline (orthorhombic) state it is[24-26] 30-50 and 55-64 in the hexagonal phase[27]. One again suspects the presence of effects of molecular volume therefore.

An interesting, and important, effect is detected when Ta_2O_5 is diluted with TiO_2. For a concentration of approximately 8 atomic % TiO_2 in Ta_2O_5 extremely large dielectric constants of ~ 126-189 are observed. Intuitively, one

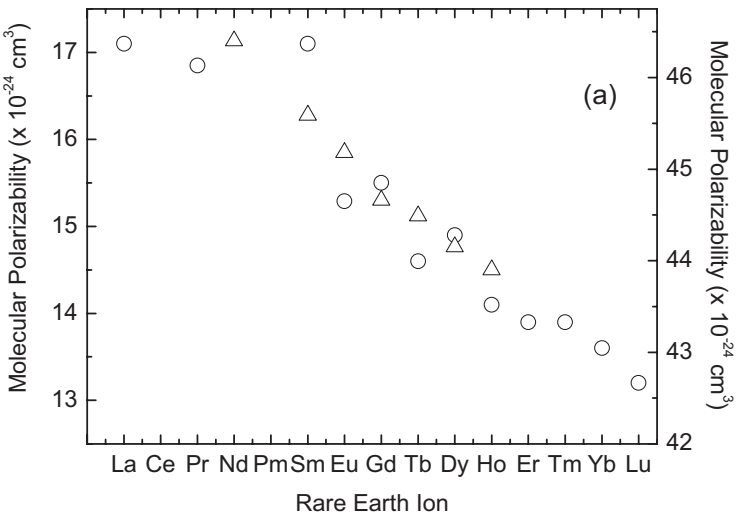


Figure 5. Variation of the molecular polarizability in (○) RE_2O_3 compounds (left hand scale) and (△) $RE_3Ga_5O_{12}$ compounds (right hand scale) as deduced from experimental densities and dielectric constants.

might anticipate that this dramatic increase is in some way related to the large dielectric constant (~ 100) of crystalline TiO_2. However, the mixed oxide contains only 8 atomic % of this material. It turns out that the addition of small quantities of TiO_2 to Ta_2O_5 stabilizes a dense, monoclinic structure of Ta_2O_5 and we can therefore anticipate the presence of network density related dielectric enhancement. In Fig.(6) we plot the measured dielectric constants for the various phases of Ta_2O_5 as a function of the inverse of α/ V_m. For the sake of discussion we have assumes $\alpha \sim 20.2 \times 10^{-24}$ cm^3. Also shown in the plot is the theoretical curve generated using Eq.(3). Inasmuch as we have maintained a constant, the entire variation of the dielectric constant is attributed to the

density differences of the different Ta_2O_5 polymorphs. Some minor variation in α may occur as a function of density but as we have shown in the examples given previously, their overall variation does not mask the primary variable which is the network density.

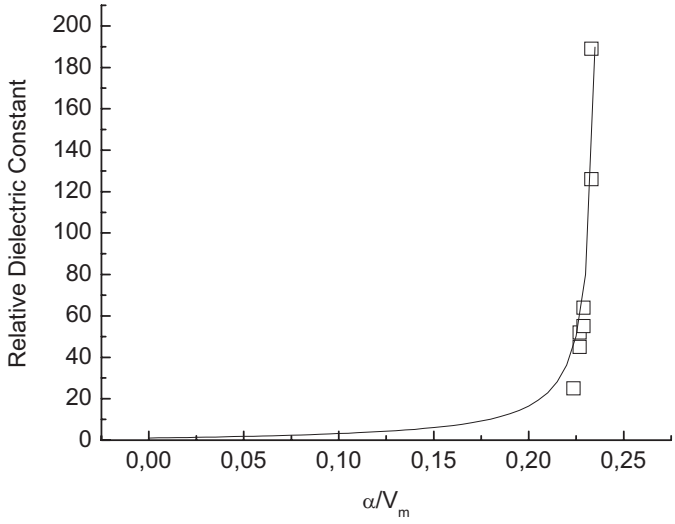


Figure 6. Relative dielectric constant in Ta_2O_5 polymorphs as a function of α/V_m with α taken as 20.2×10^{-24} cm^3. The solid line shows the predicted variation from Eq.(3).

4. CONCLUSIONS

In this paper we have reviewed the role of the network in determining the dielectric constant of binary and mixed oxides. We have discussed what were seemingly difficult and misunderstood systems such as Ta_2O_5-TiO_2 which appeared to have an anomalously large dielectric constant. Furthermore, we have been able to explain seemingly controversial data on RE sesquioxides which appeared to demonstrate very much larger dielectric constants for the

lighter RE's than for the heavy RE's. The conclusion we draw is that network volume and connectivity plays a crucial role in determining k.

- On the basis of the analysis presented here it appears that the dielectric constant of the amorphous phase of any binary or mixed oxide will always be significantly lower than that for the crystalline phase. This appears to result from the fact that the amorphous network is less densely packed than the crystalline phase.
- The role of coordination is extremely important since higher coordination structures result in denser networks. This may be true in both amorphous and crystalline phases. The data on ZrO_2 polymorphs demonstrates the density/coordination perfectly for the crystalline state.
- Some crystalline phases which are not normally stable may become so by addition of stabilizing components (such as TiO_2 in Ta_2O_5). Denser structures and associated higher k values may be obtainable by this route.

These arguments neglect the possible variation of molecular polarizability which, if large enough and of the correct sign, could negate the effects of reduced molecular volume resulting in denser structures. Fortunately, all of the systems we have studied to data appear to indicate that the volume diminution effect dominates.

For technological applications, high k amorphous materials are generally supposed to be the material most desired since possible effects due to grain boundaries are absent. The present work leads us, unfortunately, to the natural conclusion that the amorphous state is the most unsuitable if we want to obtain the maximum k values. At the present time there appears to be no obvious solution to this dilemma.

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INVESTIGATION OF THE ELECTRONIC PROPERTIES OF THIN DIELECTRIC FILMS BY SCANNING PROBE MICROSCOPY

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Abstract: The use of Atomic Force and Scanning Tunneling Microscopy (AFM/STM) and Electric Force Microscopy (EFM) to investigate local electrical properties of thin dielectric films on semiconductor substrates has been demonstrated. The effect of experimental conditions on the relative sensitivities of the methods are discussed.

Keywords: gate insulators, MOSFET, electrical properties, AFM, STM, EFM, Kelvin Microscopy.

1. Introduction

The investigation of alternative dielectric materials that are promising for use as gate insulators in advanced Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) with the thickness of the gate dielectric ~ 1 nm is currently of great interest [see reviews [1,2] and references therein]. Due to the reduction of the lateral size of elements in modern and near-future complimentary MOS (CMOS) integrated circuits (ICs) down to 10 nm and less, the development of new probing techniques with nanometer scale spatial resolution is becoming critically important, in particular, those capable to locally assess the electrical properties of ultrathin dielectric films.

Usually, capacitance – voltage (C-V) measurements of the MOS structures are employed to study the electronic properties of semiconductor/dielectric interfaces. In this technique metal electrodes are deposited onto the dielectric

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films. The information obtained by C-V measurements is averaged over the electrode area, and thus has size limitations.

To investigate the local physical properties of the metal and semiconductor surfaces, variants of Scanning Probe Microscopy (SPM) have been applied [see reviews[3,4] and references therein].

The linear size of the electrodes in standard C-V characterization techniques usually ranges from 50 microns to 1 mm. In SPM the effective size of the metal coated probe is determined by the radius of the probe apex that is about 20-50 nm. SPM techniques potentially allow the investigation of physical properties of a surface or thin film with a spatial resolution of the same order of magnitude as the tip size.

Using EFM one can study the distribution of the electrical potential and the local-probe-to-sample capacitance across the sample surface with the high spatial resolution (up to 30-50 nm)[5].

The purpose of this work was to explore the capabilities of combined AFM/STM and EFM for locally probing of the electrical properties of thin dielectric films on Si substrates.

Recently, we applied the combined AFM/STM to study the electronic properties of ZrO_2(Y) nanostructured films[6].

In the present work, we applied this method to investigate the uniformity of and defects in ultrathin insulating layers with high spatial resolution.

2. Basics of experimental techniques

2.1. COMBINED AFM/STM TECHNIQUE

In our combined AFM/STM measurements we used a standard beam deflection AFM with a conductive cantilever. The feedback was maintained by AFM in a contact mode. I-V curves of the tunneling contact between the cantilever and p+-Si substrate through the dielectric film were recorded simultaneously at every point of the scan. This approach allowed us to decouple maintaining the feedback and measuring the tunneling current, and thus to observe tunneling through the defect states in the dielectric films.

2.2. EFM TECHNIQUE

A standard EFM technique is based on the double pass Non Contact (NC) AFM mode. In the first pass a line profile of the sample surface topography is recorded in the semi-contact mode. Then the probe is lifted above the sample surface and the second pass is done following the line profile recorded during

the first pass thus keeping the probe height z above the sample constant. During the second pass a DC voltage U_{DC} and AC modulation voltage $U_{AC}\sin\omega t$ are applied between the probe and the sample. The variations of the amplitude, the phase, or the frequency of the cantilever oscillations excited by AC modulation reflect the electrostatic interaction between the probe and the sample. The resulting electrostatic force acting on the cantilever has two alternating components with the frequencies ω and 2ω, respectively:

$$F(\omega) = -(U_S + U_{DC})U_{AC}\sin(\omega t)\frac{\partial C}{\partial z} \qquad (1)$$

$$F(2\omega) = \frac{1}{4}U_{AC}^2\cos(2\omega t)\frac{\partial C}{\partial z} \qquad (2)$$

where C is the probe to sample capacitance and U_S is the contact potential difference between the probe and the sample.

It is evident from Eqns. 1 and 2 that both components of the force are sensitive to the local probe-to-sample capacitance, i.e. to the relief of a surface that complicates the analysis of the experimental data on the spatial distribution of the surface potential U_S. However, the opportunity of recording the signals at both frequencies simultaneously allows one to take into account the contribution of the surface relief. As follows from Eqn. 2, the second harmonic of the force $F(2\omega)$ is sensitive to local capacitance only and does not depend on U_S. Therefore, the effect of the probe-to-sample capacitance can be taken into account by theoretical calculations.

Kelvin Force Microscopy (KFM) [7] is a kind of EFM that permits quantitative measurement of the contact potential difference between the surface and the probe U_S. In KFM, an additional feedback loop keeps the first harmonic of the electrostatic force $F(\omega) = 0$ by adjusting U_{DC}.. As follows from Eq. (1), the condition $F(\omega) = 0$ is satisfied when $U_{DC} = -U_S$.

3. Experiment details

3.1. COMBINED AFM\STM

The combined AFM/STM experiments were carried out using an Omicron UHV AFM/STM LF1. Silicon cantilevers covered with platinum were used. The radius of the probe apex was ~ 50 nm. The ZrO_2 films were deposited with Reactive Pulsed Laser Deposition (PLD) (ablation of a metallic Zr target in O_2 ambient) at room temperature followed by post deposition annealing at $T=600^0C$ in the same O_2 ambient ($P_{O2}\approx10^{-2}$ Torr). The film thickness was about

4 nm. Native Si oxide films (≈2 nm in thickness) on p^+-Si were also investigated.

To test the combined AFM/STM, a ZrO_2 film (24 nm thick) deposited on p^+-Si by atomic layer deposition (ALD) in the MDM-INFM Laboratory (Italy) was used. It is well known[8,9,10] that ultrathin HfO_2 and ZrO_2 layers grown on Si are not stable with respect to annealing under reduced conditions, especially in UHV, and degrade with the formation of respective silicide. However, the exact mechanism of oxide degradation at the interface with Si is still debated. To characterize the degradation kinetics with AFM/STM, a ZrO_2/Si sample was annealed in UHV with the temperature gradient across the sample in the range T=800-900^{0}C as measured with a pyrometer. *In situ* x-ray photoelectron spectroscopy (XPS) applied to different areas on the sample revealed complete conversion of ZrO_2 into Zr silicide at T=900^{0}C, while no sign of silicide formation was seen on the opposite end of the sample (T=800^{0}C).

3.2. EFM

EFM measurements in ambient air were carried out using a TopoMetrix TMX-2100 Accurex SPM and in UHV using an Omicron UHV AFM/STM LF1.

For EFM investigations, 10 nm thick HfO_2 films grown by reactive PLD on p^+-Si substrates (following the same recipe as that for ZrO_2) were used. The formation of a continuous HfO_2 layer was revealed with XPS. For comparison, Si substrates covered with a native oxide were also investigated.

The amplitude of cantilever oscillations at the modulation frequency ω (which is proportional to the force component $F(\omega)$ versus the DC voltage applied between the probe and the sample U_{DC}) were measured.

4. Results and discussion

4.1. COMBINED AFM/STM

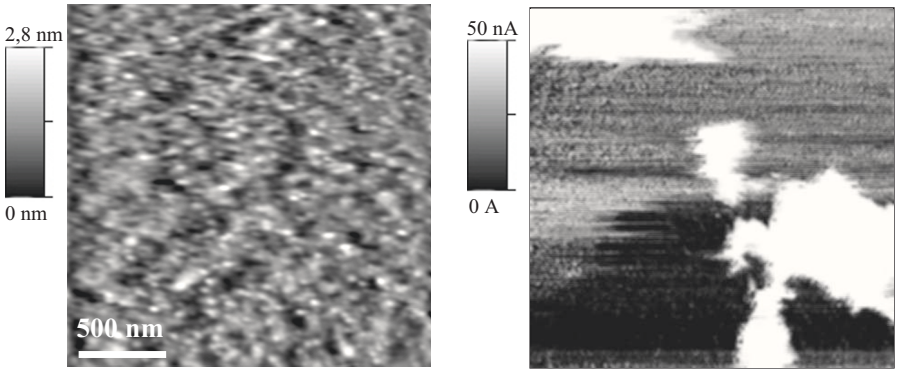


Figure 1. Morphology (left) and current image (right) of ZrO_2 film after vacuum annealing at T ≈900 °C.

In Figure 1 the morphology and the current images of a ZrO_2 film annealed in vacuum to a partial degradation are shown.

It should be noted that no correlation between morphology and the current image was observed. The contrast in the current image implies a layer-by-layer formation of $ZrSi_x$ starting from ZrO_2 /Si interface. In the Z channel we observed the morphology of ZrO_2 film surface, Figure 2 (left), which is rather flat over the scanned area. In the current image, the contrast is attributed to the layer-by-layer island growth of $ZrSi_x$ at ZrO_2/Si interface (Figure 2, right).

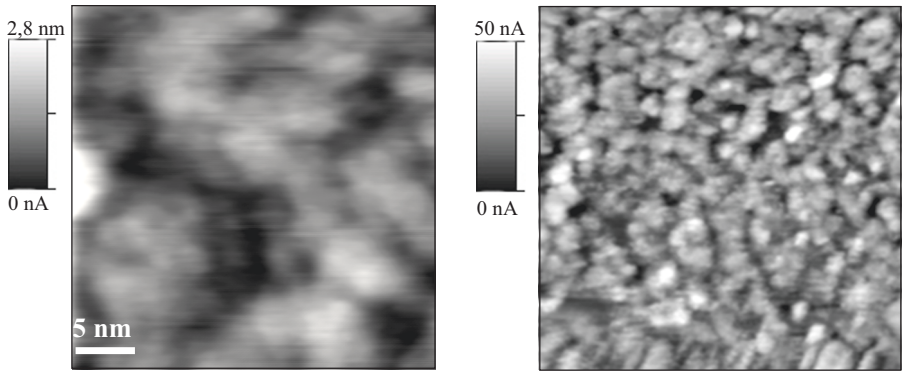


Figure 2. Morphology (left) and current image (right) of ZrO_2 film upon vacuum annealing to T ≈900 °C.

For the sample region annealed to lower T where no degradation occurred no tunneling current through the oxide was observed up to a gap voltage of U=±10 V.

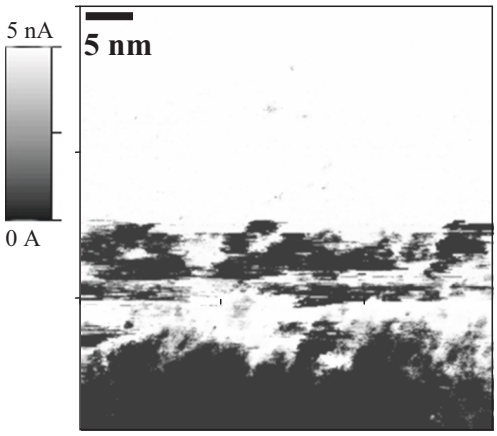


Figure 3. Current image of a natural SiO_2 on Si, Ubias=5V.

In Figure 3 a typical current image recorded on native SiO_2/Si is presented. Native SiO_2 is ~ 2 nm in thickness and is tunnel transparent. The inhomogeneity of the current image in Figure 3 is most likely attributed to the heterogeneity of the dielectric properties of the native oxide film. On the contrary, a ≈4 nm thick ZrO_2 film, also investigated by this method, was homogeneous over the whole image area. The tunneling current through the dielectric does not flow, indicating high quality of the insulated layer. Therefore, the combined AFM/STM method is applicable to investigate with the high spatial resolution the electrical properties in ultra thin dielectric layers. In particular, it was successfully applied to monitor the quality of the MeO_X/Si interfaces and in studying the degradation of MeO_X layers upon annealing.

4.2. EFM

In Fig. 4a typical results showing the dependence of the EFM signal at the modulation frequency ω on the bias voltage U_{DC} measured on SiO_2(native oxide)/Si and on HfO_2(10 nm)/Si are presented. The curves in Fig. 4a have a typical shape with hysteresis quite similar to the low frequency C-V curves of MOS structures.

The values of U_{DC} at F (ω) = 0 differ from that of the contact potential difference of Si and Pt (the probe coating material) U_S(Si-Pt), which can be explained by the effect of a built-in charge in the insulator.

When there is a static charge Q_S in the dielectric film, an additional term appears in the expression for the force of electrostatic interaction between the probe and the sample accounting for an additional Coulomb force[11]. Equation (1) will become:

$$F(\omega) = \left[\frac{\partial C}{\partial z}(U_S + U_{DC}) - \frac{Q_S C}{4\pi\varepsilon_0 z^2} \right] U_{AC} \sin(\omega t) \tag{3}$$

In the Kelvin mode, the built - in charge in the insulator can be determined from the expression:

$$Q_S = \frac{\partial C}{\partial z}(U_S - U_{DC}) \frac{4\pi\varepsilon_0 z^2}{C} \tag{4}$$

where U_S is the theoretical value of the contact potential difference between the probe and the sample materials and U_{DC} is the measured DC bias voltage at $F(\omega) = 0$.

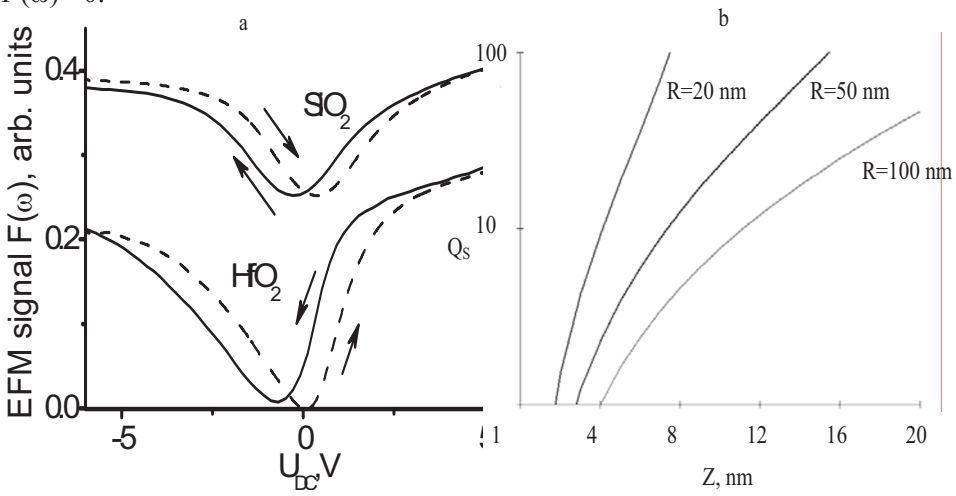


Figure 4.(a)-The dependence of the EFM signal at the modulation frequency ω on the DC bias voltage U_{DC} ; (b) - dependence of the built - in charge Qs (in units of an elementary charge) on the averaged probe - sample distance z for different probes.

To estimate the sensitivity of the method with respect to the built-in charge Q_S, we used the expression for capacity between a flat infinite surface and a probe, the shape of the probe apex was approximated by a hemisphere with the radius R:

$$C = \frac{\varepsilon_0}{4\pi} \frac{R(2z - R)}{2(z - R)} \tag{5}$$

Substitution of expression for the probe-to-sample capacitance (Eq. 5) and its derivative into Eq. (4) gives an expression to estimate the minimum

detectible built-in charge Q_S depending on the parameters of the probe and lifting height *z*.

In Figure 4 (b) the dependences of Q_S (in units of the elementary charge) on the average distance between the probe and the sample are plotted for different realistic values of the probe apex radius *R*. The sensitivity of the method rises with increasing the radius of the probe apex. However, at the same time the spatial resolution decreases. The reduction of the distance between the probe and the sample also increases the sensitivity. Using commercially available probes (with the apex radius $R = 20 - 50$ nm) one can detect a built-in charge for as low as several localized electrons (or holes) at a reasonable lifting height in the second pass (5-10 nm).

5. Conclusion

The advantages of the combined AFM/STM technique for investigating the dielectric properties of ultrathin oxide layers with high spatial resolution are shown. Particularly, MO_2/Si (M=Hf, Zr) interface evolution upon heat treatments is explored. It is observed that vacuum annealing in the range T =800-900 °C of ZrO_2 films grown on Si results in the degradation ZrO_2 with formation of a Zr silicide layer which starts to grow from ZrO_2/Si interface.

The applicability of the EFM technique to investigate of the charge distribution in dielectric layers with high spatial resolution is also shown.

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