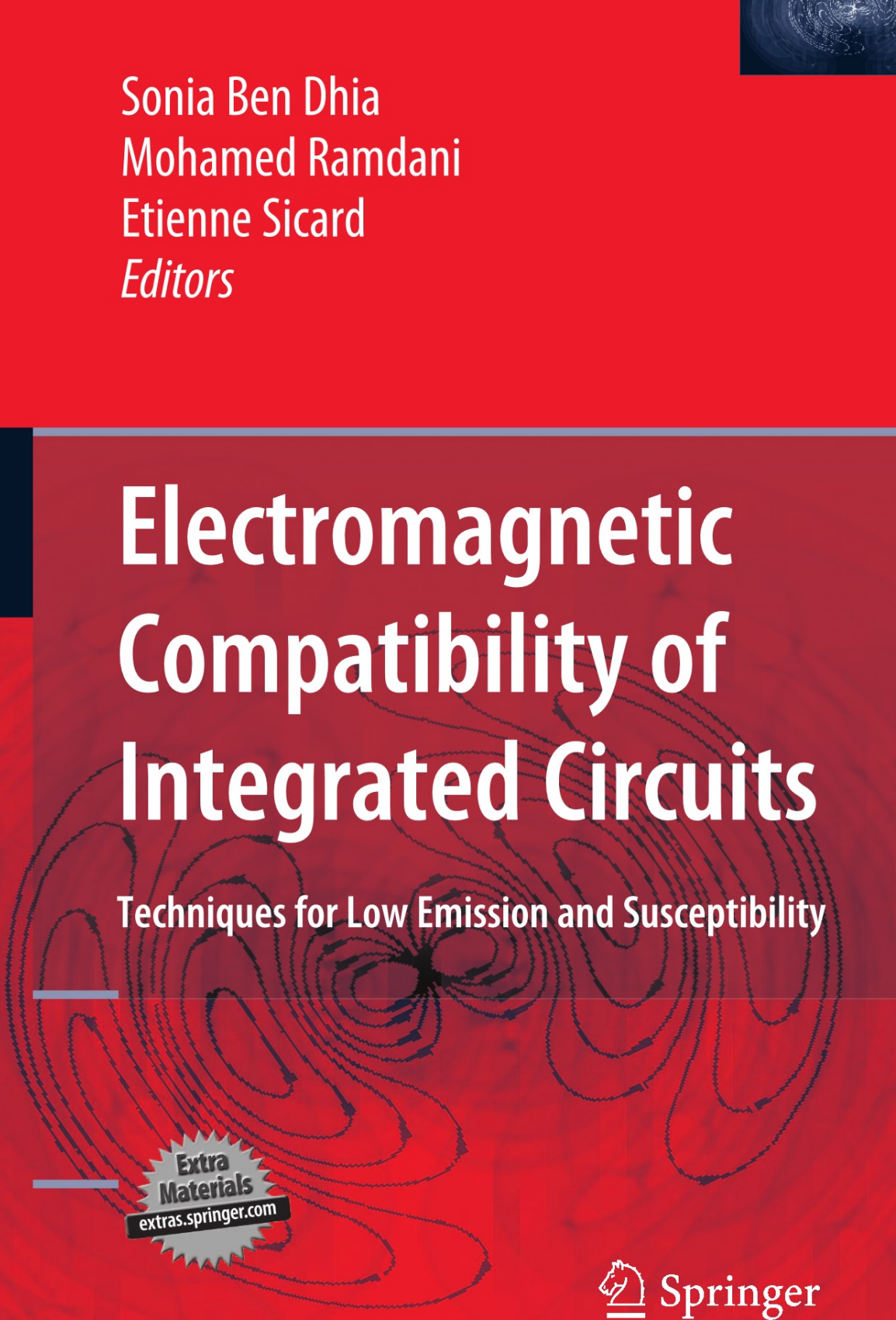
Sonia Ben Dhia
Mohamed Ramdani
Etienne Sicard
Editors

Electromagnetic Compatibility of Integrated Circuits

Techniques for Low Emission and Susceptibility



Springer

ELECTROMAGNETIC COMPATIBILITY OF INTEGRATED CIRCUITS

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Techniques for low emission and susceptibility

Edited by

Sonia Ben Dhia[1], Mohamed Ramdani[2] and Etienne Sicard[1]

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Dedication

To our children

Camille

Cyrine

Daniel

Sadri

Selma

Soumaya

Contents

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Preface

The project of writing a book on electromagnetic compatibility of integrated circuits took form and substance during the international workshop EMC Compo 2004 in Angers, France, and led to this present work. More than thirty contributors to the workshop have been asked to participate the book chapters, according to their expertise. The editors gathered the technical contributions and did their best to build self-consistent chapters related to the major hot topics of this field, namely the measurements methods, the modeling approaches, and the design techniques for low emission. Several test cases have been gathered into a specific chapter. The technical contents of this document are intended to help IC designers and electronics system designers reduce the parasitic emission as well as susceptibility to radio-frequency interference.

This book is a unique collection of information focused on the electromagnetic compatibility of integrated circuits. The basic concepts, theory, and an extensive historical review of integrated circuit emission and susceptibility are provided. Standardized measurement methods are detailed through various case studies. EMC models for the core, I/Os, supply network, and packaging are described with applications to conducted switching noise, signal integrity, near-field and radiated noise. Case studies from different companies and research laboratories are presented with in-depth descriptions of the ICs, test set-ups, and comparisons between measurements and simulations. Specific guidelines for achieving low emission and susceptibility derived from the experience of EMC experts are presented. The companion CD-ROM includes software illustrating key aspects of the book and a collection of demo tools applicable to EMC analysis of ICs.

Acknowledgements

We would like our early colleagues of the IERSET project in Toulouse as well as the partners from the European MEDEA project "EMC Workbench" and "Mesdie" for their support throughout the development of test circuits and design methodologies for improved EMC. We would like to thank Joseph-Georges Ferrante, Werner John for provided their continuous support over the last ten years. Productive technical discussions with the French UTE standardization group, the authors and contributors to EMC Compo 02 in Toulouse, France and EMC Compo 04 in Angers, France, are also gratefully acknowledged.

Special thanks are due to technical contributors to the companion CD-ROM, to our colleagues at INSA and ESEO who always supported our research work, to numerous professors, students and engineers who patiently built the technical contents of the book and gave valuable comments and suggestions. Also, we would like to thank Marie-Agnes Detourbe, John Kerr and Langis Roy for having carefully reviewed the manuscript.

Finally we would like to acknowledge our biggest debt to our parents and to our companion for their constant support.

Chapter 1

BASIC CONCEPTS IN EMC FOR ICS

Abstract: This chapter introduces key concepts related to Electromagnetic Compatibility (EMC) of Integrated Circuits (ICs), describes basic measurement methods and provides an outline of IC modeling for EMC prediction. A brief description of electric and magnetic field coupling, conducted and radiated mode emissions, as well as susceptibility, are also given in this chapter.

Key words: Electromagnetic compatibility; electric field; magnetic field; coupling; simultaneous switching noise; crosstalk; radiated emission; conducted emission; EMC modeling; EMC measurement methods

1. INTEGRATED CIRCUIT EMC

Integrated circuits (ICs) often play an important role in the electromagnetic compatibility of an electronic system. Generally, ICs are the ultimate source of signals and noise that produce interference. They convert the D.C. power supplied to them into the high-frequency currents and voltages that are responsible for unintentional emissions or coupling. The ultimate victims of electromagnetic interference are also, very often, ICs. Of all the components in a typical electronic system, ICs tend to be the most susceptible to damage caused by over-voltage or over-current conditions. Even if they are not damaged, noise coupled to the input or power pins of ICs may cause them to malfunction. Although ICs are generally the ultimate source and/or victim of an EMC problem, the focus of most EMC-related research and problem solving has been external to the IC package. EMC engineers have traditionally focused their efforts on the design of printed circuit boards, enclosures, and cabling. With a few notable exceptions (e.g. over-voltage protection and slew rate control), EMC has not played a major role in the design of the integrated circuit itself.

EMC problems associated with integrated circuits can generally be classified as *intra-chip* or *externally-coupled.*

Intra-chip EMC problems result when a signal or noise created in one or more circuits interferes with the operation of another circuit on the same chip.

Externally-coupled EMC problems result when signals or noise generated on an IC interfere with circuits or devices off the chip; or conversely when noise generated externally interferes with the proper operation of the IC.

1.1 Intra-Chip EMC

The two most common intra-chip EMC problems are crosstalk and simultaneous switching noise. Crosstalk results when voltages or currents in one circuit are unintentionally coupled to another circuit. If the coupling is strong enough, the coupled signal can affect the amplitude and/or timing of the signal received by the victim circuit, causing it to malfunction.

1.1.1 Crosstalk

The crosstalk between two circuits is generally defined as the ratio of the unintentional voltage appearing across the load in the victim circuit to the signal voltage in the source circuit. It is normally expressed in dB as,

$$\textit{crosstalk in dB} = 20\ \log\left|\frac{\textit{coupled voltage appearing at receiver in Circuit 2}}{\textit{signal voltage in Circuit 1}}\right|. \quad (1\text{-}1)$$

Since the coupled voltage is normally smaller than the source voltage, crosstalk expressed in dB is usually a negative value.

In integrated circuits, there are generally three types of coupling that can result in crosstalk: common-impedance coupling, electric field coupling, or magnetic field coupling.

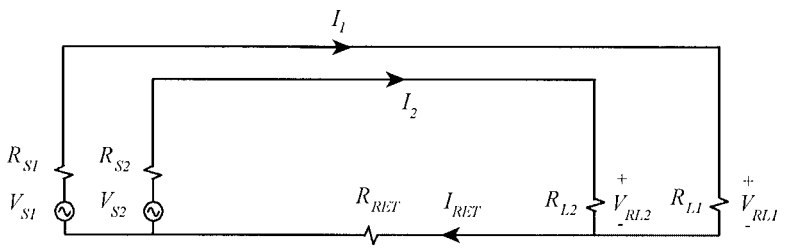

Figure 1-1. Two circuits sharing a common current return path.

Common impedance coupling (also called conducted coupling) occurs when parts of the current paths in two circuits share the same conductor (e.g. the same ground metallization). An example of this is illustrated in Fig.1-1, where two circuits with sources V_{S1} and V_{S2} share a common conductor that has a resistance, R_{RET}.

Note that the finite impedance associated with the shared conductor results in a voltage drop that appears across both circuits. Generally speaking, the coupled voltage is proportional to the product of the shared impedance and the current in the source circuit.

Electric field coupling (also called capacitive coupling) occurs when electric field lines originate on a conductor in one circuit and terminate on a conductor in another circuit. This can be represented schematically by a parasitic capacitance between the two conductors. A typical example of this is the coupling between two closely spaced signal conductors as illustrated in Fig. 1-2. Usually, electric field coupling induces a current in the victim circuit that is proportional to the time derivative of the source signal (i.e. *C.dV/dt*).

Magnetic field coupling (or inductive coupling can also be a significant source of crosstalk in ICs. This type of coupling occurs when magnetic fields produced by the time-varying currents in a source circuit "couple" (i.e. penetrate the loop area) of a second circuit. This is similar to the coupling between the primary and secondary of a transformer.

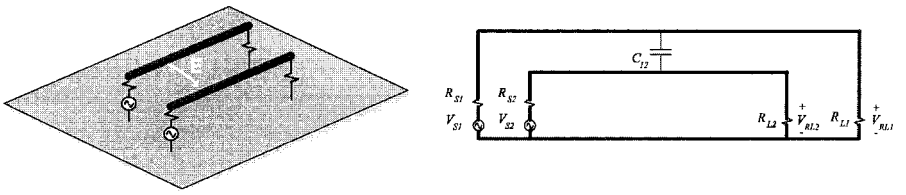

Figure 1-2. Electric field coupling between signal conductors.

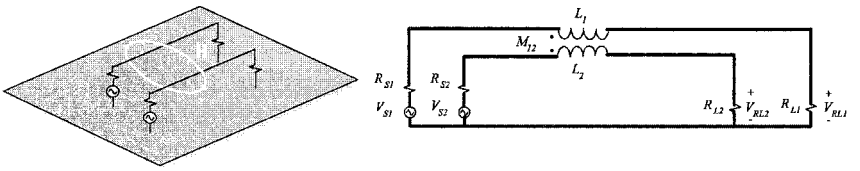

Figure 1-3. Magnetic field coupling between signal conductors.

Table 1-1. Basic coupling mechanisms for IC crosstalk

Type of Coupling	Conditions	Remedies
Common Impedance Coupling	Low-frequency Low impedance	Isolate current paths Reduce impedance of common path
Electric Field Coupling	High frequency High impedance source	Separate circuits Isolate circuits with grounded conductor Reduce signal voltage

Fig. 1-3 illustrates magnetic field coupling between two circuits that have overlapping loop areas. Magnetic field coupling generates a voltage in the victim circuit that is proportional to the derivative of the signal current in the source circuit (i.e. $L.di/dt$).

Table 1-1 lists the 3 basic coupling mechanisms that can result in crosstalk between circuits in an IC as well as the conditions likely to produce each type and possible courses of action. Crosstalk problems in ICs can generally be avoided by following basic guidelines for routing circuits on a chip. It is important to keep track of the current paths associated with each signal as well as the voltages.

1.1.2 Simultaneous switching noise

Simultaneous switching noise is perhaps the most infamous EMC problem associated with integrated circuit design. Also known as ground bounce, power bounce or delta-I noise; simultaneous switching noise has been the source of many chip failures some of which were not detected until after the design was in full production.

Simultaneous switching noise is basically a common impedance coupling problem that arises due to the fact that various circuits in an integrated circuit share the same power distribution bus. When a circuit draws current from the power bus, a small voltage is dropped across the bus. This drop in the power bus voltage affects all circuits connected to the bus.

Fig. 1-4 illustrates the basic concept. Suppose that there are two totem-pole output stages in a CMOS circuit that share the same power distribution path and the resistance of the power path back to the source is $R_{DD} + R_{SS}$. If the first circuit output, V_{SIG1}, is in the high state, then $V_{SIG1} = V_{DD} - V_{SS}$. When the second circuit switches from low to high, a current I_2 is drawn from the V_{DD} side of the power bus and flows to the V_{SS} side of the power bus. The current I_2 only flows long enough to charge the capacitance associated with signal 2. However as I_2 is pulled through the resistance of the power bus, there is a momentary drop in the voltage seen by both circuits. The voltage V_{SIG1} takes on a new value: $V_{SIG1} = V_{DD} - V_{SS} - I_2(R_{DD} + R_{SS})$.

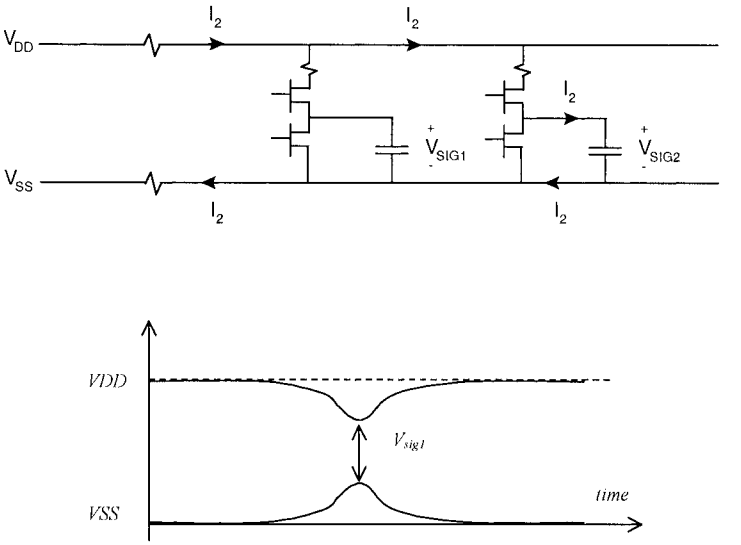

Figure 1-4. Two totem-pole CMOS drivers sharing a power bus.

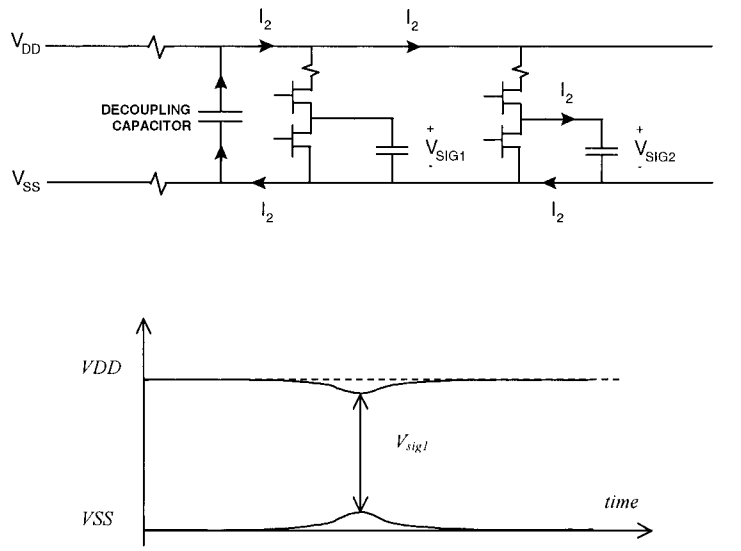

Figure 1-5. Two totem-pole CMOS drivers with nearby decoupling capacitor.

If the resistance is a few milliohms and the peak current is on the order of an ampere, the voltage fluctuation is only a few millivolts. On the other hand if the number of circuits that switch at the same time is large, the peak current drawn through the power bus can be high enough to cause outputs to fluctuate by several volts causing changes in the state of outputs that are supposed to be stable.

Simultaneous switching noise can be reduced by providing low impedance power distribution on the IC. High speed VLSI designs also employ *on-chip decoupling capacitance* to protect against problems due to simultaneous switching. On-chip decoupling capacitors are capacitors connected between V_{DD} and V_{SS} that provide a temporary source of charge for the instantaneous switching currents required by nearby circuits. Fig. 1-5 illustrates how a nearby decoupling capacitor prevents instantaneous switching currents from being drawn from the power bus. When a circuit switches, the peak current required to start charging the signal capacitance is drawn primarily from the larger nearby decoupling capacitor instead of being drawn through the power bus resistance. After the initial peak demand for current has passed, the decoupling capacitor is slowly recharged by the power bus.

1.2 Externally-Coupled EMC

Most integrated circuit designs are thoroughly tested before being mass-produced and intra-chip EMC problems are generally resolved before devices are placed in a real product.

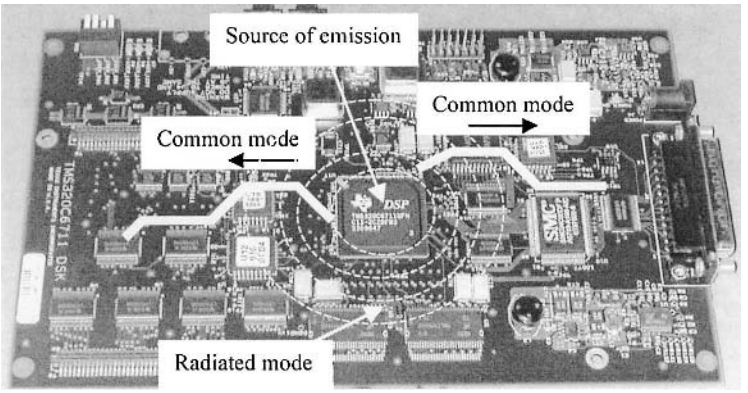

Figure 1-6. Conducted and radiated emission provoked by the internal switching activity of an integrated circuit

However, semiconductor devices that exhibit no intra-chip problems can still be the source (and victim) of EMC problems due to noise that is coupled in or out of the chip package (Fig. 1-6).

There are four possible mechanisms for coupling of electromagnetic noise to or from an integrated circuit. Like crosstalk within a device, externally-coupled noise can be conveyed via a conducted path, an electric field or a magnetic field. Additionally, it is possible to radiate energy directly from the chip or package.

1.2.1 Conducted Coupling

Perhaps the most obvious way to couple noise into or out of an integrated circuit is via the package leads or pins. Crosstalk between a high-frequency input/output and a low-frequency input/output is one way that noise is coupled conductively. Simultaneous switching noise is another common source of high-frequency noise. Since simultaneous switching noise is a fluctuating voltage on the power bus, all of the device pins referenced to a particular power bus may exhibit high-frequency voltage fluctuations if there is inadequate decoupling on the chip or package.

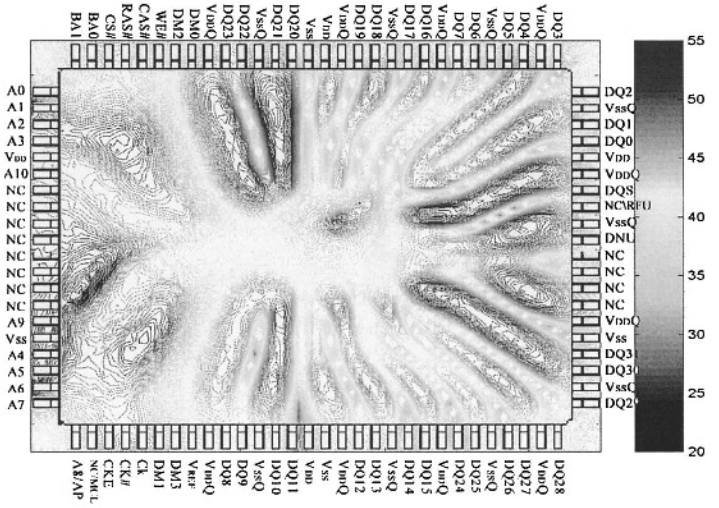

Figure 1-7. H-Field surface scan of a RAM memory module at 200 MHz.

Voltage drops across an IC's substrate can also result in voltage differences between pins connected to different areas of the chip. Fig. 1-7 shows a magnetic near-field scan for an RAM memory device. The device is clocked at 200 MHz and the magnetic field is measured at 200 MHz.

The magnetic fields are strongest just above the lead frame where the currents are the strongest. As the figure illustrates, the strongest currents are flowing in the VCC and GND pins. This is an example of simultaneous switching noise. The high-frequency currents conducted off the chip via these pins can result in significant radiated emissions from any printed circuit board that uses this particular device.

It is not uncommon to observe harmonics of internal clocks on all of the pins connected to an integrated circuit. This can be a difficult problem to address at the board level, since it becomes necessary to route all traces connected to that IC as if they were high-frequency traces. On the other hand, noise problems such as this can be minimized relatively inexpensively through the use of effective on-chip decoupling techniques.

1.2.2 Electric Field Coupling

It is also possible to couple energy to or from an integrated circuit via an electric field. Electric field coupling occurs when a voltage that is developed across a device causes a voltage to appear between two external conductors. Usually, this type of coupling occurs when a metallic object such as a heat sink or a cable is located very near the surface of the chip package.

Large heat sinks can become relatively efficient antennas at frequencies as low as a few hundred megahertz. When boards with heat sinks are located in shielded enclosures, the heat sinks can facilitate the coupling of energy that drives enclosure resonances (Li, 2001).

The average voltage on the surface of the semiconductor device can be different than the voltage on the surface of the PCB due to the signal voltages themselves or the voltage dropped across the connections between the device and the board as illustrated in Fig. 1-8. One possible solution to this problem is to attempt to bond the heat sink to the PCB. Another possible solution is to attempt to shift the resonances of the PCB/heat sink structure so that they don't correspond to enclosure resonant frequencies (Huang, 2001). Both of these solutions can be difficult to implement in a reliable and cost-effective manner.

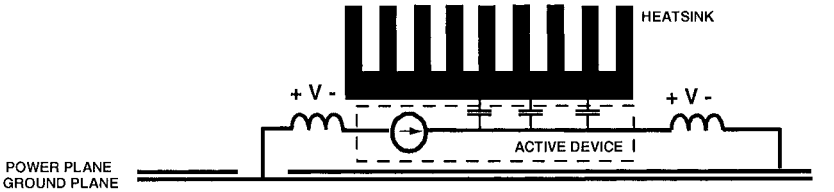

Figure 1-8. Component voltage coupling to heat sink.

A much better solution is to design the chip and package to prevent significant coupling to the heat sink. This can be done by reducing the inductance of the connections between the chip and the PCB or by designing the package to facilitate an effective bond between the heat sink and the PCB.

Although the field is ultimately radiated in this example, we don't refer to this as *radiation* from the integrated circuit itself. The coupling between the IC and the heat sink was through an electric field. The coupling between the IC and the board was conducted. The radiation came from the board and the heat sink. The integrated circuit was the source, but the heat sink/board structure was the antenna.

1.2.3 Magnetic Field Coupling

When a device package contains high-frequency current loops, energy can also be coupled out of the device through a magnetic field. It is possible for the magnetic flux from a current loop in the device to link to circuit loops outside the device. This mutual inductance can produce an unwanted voltage in the external loop. Likewise, an external magnetic flux can induce an unwanted voltage across an interior circuit loop. Magnetic field coupling can be minimized by keeping power and signal loop areas as small as possible.

1.2.4 Radiated Field Coupling

Radiation coupling is the transfer of electromagnetic energy over distances generally greater than a few wavelengths (i.e. to the electromagnetic *far field*). At these distances, fields drop off more slowly with distance than they do very near the source. Both the electric field and the magnetic field are needed to propagate the energy.

Objects that are much smaller than a wavelength do not make very efficient antennas. Most integrated circuit packages are too small to radiate effectively at frequencies below about 10 GHz. At frequencies where the packages are large enough to radiate efficiently, the thin metallic structures in the package tend to be very lossy. As a result, radiation of electromagnetic energy directly from an integrated circuit is not usually a significant problem.

Many papers and texts refer to *radiation* from integrated circuit devices when they actually mean noise coupled out of an integrated circuit and then radiated by something else. If the conductors that make up the antenna are located within the integrated circuit or its package, then we say that the device *radiates*. However, if a device merely couples to an effective antenna located outside the package, we should describe that coupling as conducted,

electric field, or magnetic field coupling. By clearly stating and understanding the coupling mechanism, we are in a much better position to deal with any problems resulting from this coupling.

The best way to deal with radiated electromagnetic noise from integrated circuits is usually to start by identifying the structures that are acting as the effective *antenna.* If the radiation is significant, the conducting surfaces or wires that form the antenna will generally be one-tenth to one-quarter of a wavelength in size or larger. Generally, two large structures are required along with a noise source that drives one of them relative to the other. Once the antenna has been identified, steps can be taken to either:

1. Reduce the amplitude of the noise source
2. Decouple the noise source from the antenna, or
3. Eliminate part of the antenna.

For example, consider the heat sink radiation problem illustrated in Fig. 1-8. The IC is the source. The heat sink is one half of the antenna and the circuit board power/ground plane pair is the other antenna half. The coupling mechanism is partly conducted (power pins connecting to plane pair) and partly electric field coupling (chip surface to heat sink).

We could reduce the amplitude of the source by providing better on-chip or on-package decoupling, which would reduce the high-frequency current drawn through the power pins.

We could decouple the source from the antenna by decreasing the capacitance between the IC and the heat sink or by filtering the connection between the power plane pair and the IC power pins. Alternatively, we could eliminate part of the antenna by shrinking the heat sink or bonding it to the power/ground plane pair.

2. BASIC IC EMC MEASUREMENTS

Well-designed integrated circuits in well-designed systems rarely exhibit significant electromagnetic compatibility problems. On the other hand, getting a system with poorly designed ICs to meet basic EMC requirements can be a difficult and expensive process. Unfortunately, it is hard to tell the difference between a well-designed IC and a poorly designed IC based on data sheets or simple models.

Several measurement techniques have been proposed to try to quantify the relative merits of IC designs from an EMC standpoint. These techniques can be classified as either *emissions measurements* or *susceptibility measurements.*

2.1 Emissions Measurements

Measuring emissions from an integrated circuit can be a difficult task complicated by the fact that the *antenna* responsible for the radiated emissions is probably not part of the IC package. Quantifying the emissions from an IC is a little like trying to quantify the emissions from a collection of radio transmitters without knowing which transmitters will have antennas connected or what those antennas will look like.

Since it is not possible to simulate every possible board or system that an IC will ultimately be used in, the best we can to is to try to measure the ability of the IC to drive various kinds of antennas. This generally involves measuring currents on pins or fields near the device under test. There are three primary methods for evaluating integrated circuits in terms of their potential to be the source of radiated electromagnetic emissions: TEM cell tests, pin current measurements, and near-magnetic field scans.

TEM cells are essentially enlarged transmission lines that support TEM (Transverse Electromagnetic) wave propagation. A radiating object placed in a TEM cell generates a TEM wave within the cell that propagates to a load at the termination of the transmission line.

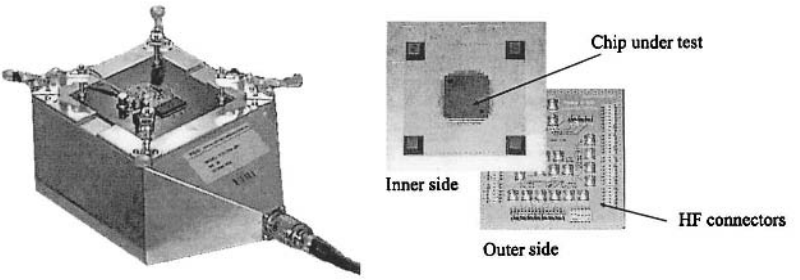

Figure 1-9. TEM cell for measuring integrated circuits.

Under the right conditions, the power coupled to the TEM wave in the cell can be related to the power that radiates from the object when it is outside the cell. Fig. 1-9 shows a TEM cell designed to measure ICs (IEC 61967-2, 2001). The IC is mounted to a printed circuit board that is then mounted to a wall of the TEM cell. Components necessary to support the operation of the IC and connectors are mounted on the opposite side of the board. The IC side of the board faces the inside of the cell so that fields above the surface of the IC are inside the TEM cell.

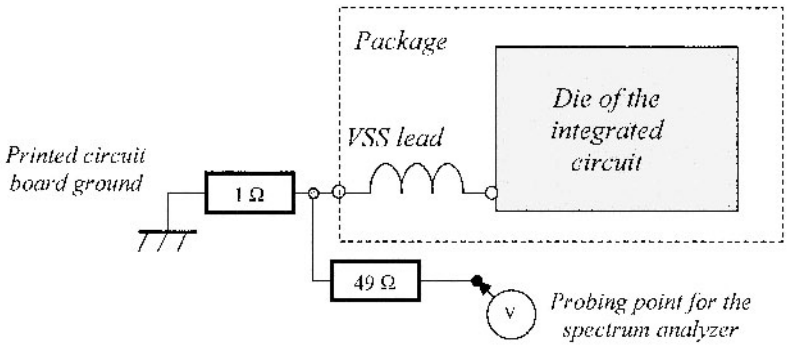

Figure 1-10. 1/150 Ω Conducted mode measurement method.

In theory, the voltage measured at the TEM cell termination gives an indication of the IC's ability to generate radiated emissions. Advantages of the TEM cell measurement are that it is relatively simple to perform, the IC can be mounted in a manner that is similar to the way it would be mounted on a production circuit board, and the measurement apparatus does not significantly change the currents flowing in the IC. However, this type of measurement does not directly measure the noise currents conducted from the IC pins.

Since the TEM cell is neither in the far field or the very near field of the device, results measured with a TEM cell may not correlate very well with near-field or radiated emission measurements. For these reasons, TEM cell measurements are one indicator of how well an IC is designed from an EMC point of view, but they are not the only (or the best) indicator. Another method for evaluating integrated circuits is to measure the conducted noise currents on each pin.

One method of doing this (IEC 61967-4, 2001) is to place a small resistance in series with the pin and measure the voltage dropped across this resistance (Fig. 1-10). Since most emissions problems related to chip designs begin with noise that is conducted out of the chip package via the pins, this measurement can be a particularly good indicator of how well the chip will perform in a real product. However, this approach also has disadvantages.

For example, it is difficult to perform in practice; particularly if the IC has many pins. Also, boards that are designed to route pin currents through a resistor must have extra long traces on each pin and the resistance and inductance of these pin connections may significantly alter the currents being measured.

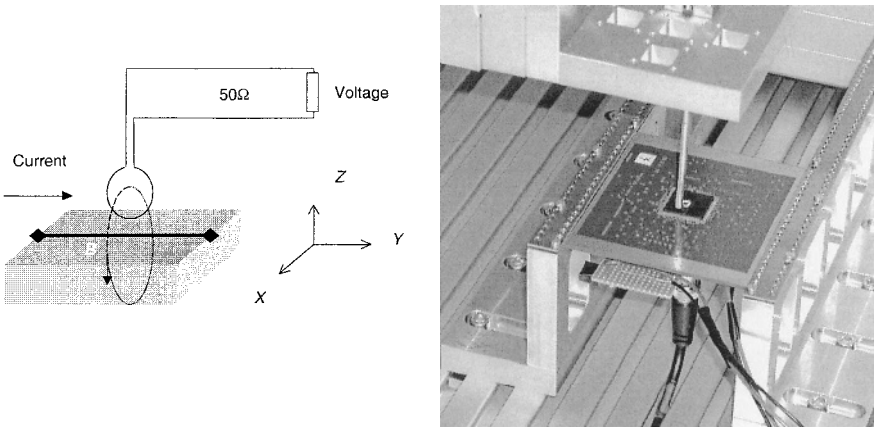

Figure 1-11. Principles for near field scan of the magnetic field.

Another method of measuring currents is to measure the magnetic field near the current path (Fig. 1-11). Near magnetic field measurements can provide a great deal of information about where currents are flowing within an IC package without significantly altering those currents. As we saw in Fig. 1-6, it is possible to create a *map* of the currents flowing within a package by scanning over the surface with a small magnetic field probe.

We can also scan the surface with an electric field probe to get an idea of the voltage distribution within the chip. Near field scans have the advantage that they can be performed without building special circuit boards. Most ICs can be measured in their natural operating environment. A disadvantage of near-field scans is that they require special equipment that is relatively expensive and has limited uses. Also, while near field scans are good for making relative measurements, it is difficult to quantify the currents measured. Converting from a magnetic field measurement to a current requires a fairly detailed knowledge of the geometries involved.

So while no single measurement technique will tell us everything we want to know about an integrated circuit's ability to produce radiated noise emissions, it is often possible to determine the relative merits of various devices using a combination of the techniques described above. As more experience is gained with each of these techniques, it should soon become easier to quickly differentiate between a *good* design and a *bad* design in terms of radiated emissions.

2.2 Susceptibility Measurements

Of course, IC EMC is more than just low radiated emissions. Susceptibility to electromagnetic noise has played a significant role in the design of integrated circuits for many years. Early integrated circuits were easily damaged by transient voltages on gate inputs and small amounts of noise could cause them to latch up or reset. Today most integrated circuits have built-in transient protection and are designed to withstand moderate amounts of electrical noise on power and signal input pins. Nevertheless, the amount of noise required to cause a malfunction can vary widely from one IC design to another. In order to choose the best IC for a particular application, it is important to be able to quantify the relative *electromagnetic immunity* of various devices.

Several measurement procedures have been proposed (IEC 61967-4, 2002) for evaluating the electromagnetic immunity (or susceptibility) of integrated circuits. These measurements generally fall into three categories: bulk current injection, direct power injection, or field coupled. Bulk current injection techniques intentionally couple a noise current onto one or more traces or wires connected to the pins of the IC. The currents are normally coupled via a magnetic field as illustrated in Fig. 1-12.

Bulk current injection limits can be specified for any pin of an IC including output pins. For differential inputs, where the signal is defined as the voltage on one pin relative to the voltage on another pin, bulk current injections testing can be done on both input pins simultaneously to measure the ability of the device to reject common mode noise.

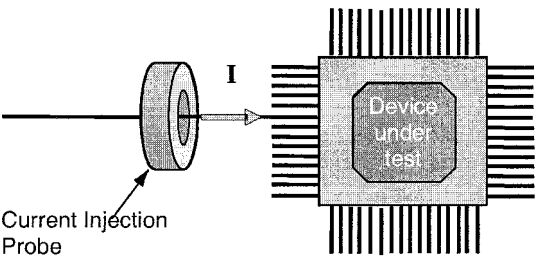

Figure 1-12. Bulk current injection testing.

To evaluate high-impedance input pins, it is generally more appropriate to induce a noise voltage on a pin rather than a noise current. Direct power injection measurements couple voltages to an input though an electric field as illustrated in Fig. 1-13.

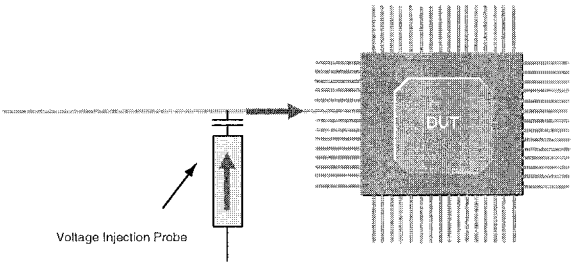

Figure 1-13. Direct power injection testing.

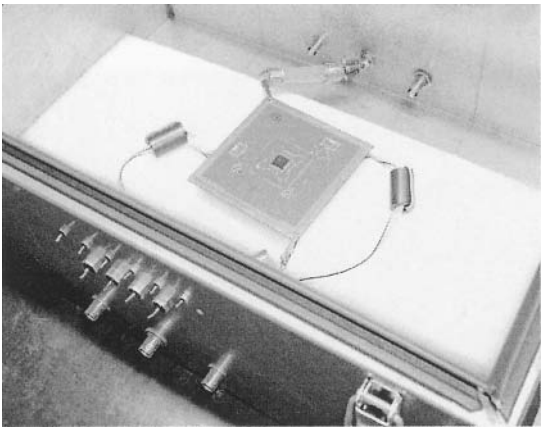

Figure 1-14. Workbench Faraday cage test

These measurements are usually easier to perform because they do not require a probe that must wrap around the injection point. Direct power injection can be accomplished by placing an electric field probe up against a trace on a printed circuit board or even against a package pin while the device is operating in its normal environment.

The third category of susceptibility measurements for ICs exposes the entire device to strong electric or magnetic fields rather than trying to couple to individual pins. One example of this type of measurement is the Workbench Faraday Cage Measurement, in which the IC is mounted to a printed circuit board and placed in a metal enclosure as illustrated in Fig. 1-14. Other field-coupled tests include techniques for measuring ICs with TEM cells or GTEM cells (See Chapter 4 for more information).

3. IC EMC MODELING

As more attention is focused on the EMC design and measurement of integrated circuits, it is important to develop appropriate models for simulating the behavior of the systems that employ these ICs. The IBIS group (IBIS, 2002) has proposed an input/output buffer description standard based on non-confidential data for IC interfaces. IBIS is recognized by IC manufacturers as a worldwide standard for describing IC interfaces to printed circuit boards.

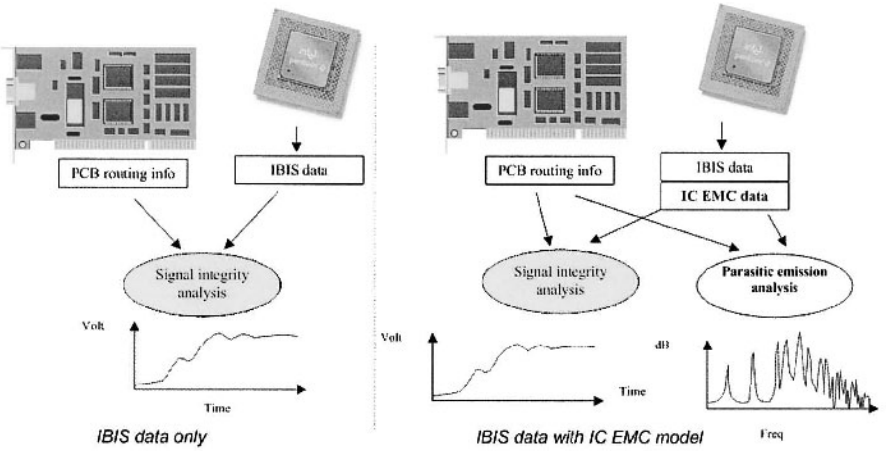

Figure 1-15. Simulation of conducted or radiated emissions using an EMC model.

Although IBIS models provide information that is useful for characterizing electromagnetic emissions, this standard was primarily developed for modeling signal integrity. For this reason, many parameters that are necessary for EMC modeling are not included in the IBIS specification.

An integrated circuit electromagnetic model called ICEM (IEC, 2002) has recently been proposed and released as an IEC draft standard. The goal of ICEM is to provide a relative simple, yet accurate model for parasitic electromagnetic emission prediction from 1 MHz to 1 GHz. More information about this model and similar approaches may be found in Chapter 5.

As illustrated in Fig. 1-15, signal integrity analysis may be performed by combining IBIS data and PCB routing information. Adding an EMC core model could give system designers the ability to simulate parasitic electromagnetic emissions and immunity to radio frequency interference.

4. CONCLUSION

This chapter has presented in a general way the issues involved in the electromagnetic compatibility of integrated circuits. The concepts of intra-chip and externally-coupled EMC have been introduced. The main mechanisms for conducted and radiated mode parasitic emissions from integrated circuits have been described, as well as the standard approaches for measuring these effects. The susceptibility of integrated circuits has also been presented from a general point of view, as well as the most common characterization approaches. Finally, the role of EMC models for simulating the emission and susceptibility of ICs has been outlined.

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Chapter 2

HISTORICAL REVIEW AND STATE-OF-THE ART

Abstract: In this chapter, we provide a non exhaustive review of the research work conducted in the field of integrated circuit electromagnetic compatibility. A wealth of research results has appeared in the last couple of years, and this review aims at describing how new techniques, tools and methods have emerged. Roadmaps for integrated circuits and package, as well as EMC issues are also given in this chapter.

Key words: History; parasitic emission; susceptibility; modeling; standards; technology; packaging; issues

1. THE EARLY WORKS

In 1965, Gordon Moore co-founder of Intel Corporation published a long-term vision of the evolution of integrated circuits.

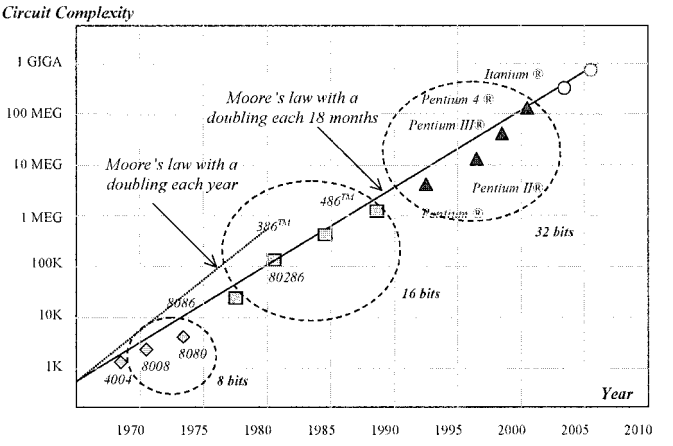


Figure 2-1. Moore's law compared to Intel processor complexity from 1970 to 2005.

SCEPTRE: A Program for Automatic Network Analysis*

Abstract: This paper describes the mathematical formulation of a computer program for automatic transient analysis of electronic networks. The formulation is based on the "state-variable" approach to network analysis and differs from other such programs primarily in the way that the network equations are manipulated to produce a solution. SCEPTRE includes a number of features aimed at providing greater flexibility and convenience for users of the program. Important among these features is that no prescribed equivalent circuit for active elements is required for program operation. Also, linearly dependent voltage and current sources in a network can be handled by the program, and provision has been made to allow a free-form format for input data. The paper includes a discussion of the program's ability to solve networks containing time-varying passive elements, and considers the factors that influence program running time.

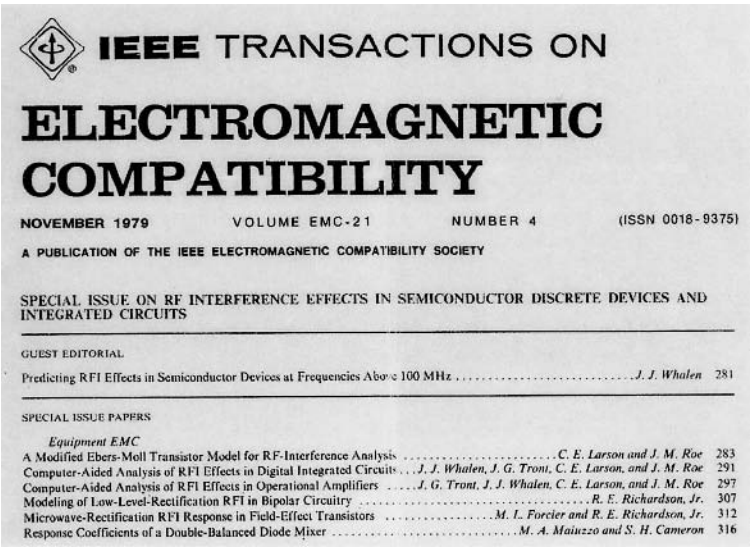
* Work supported by the Air Force Weapons Laboratory under contract AF 29(601) 6852. Dissemination of the SCEPTRE program is controlled by the Air Force Weapons Laboratory, Attn: WLRHT (Capt. Gary Pritchard), Kirtland Air Force Base, New Mexico 87117.

Figure 2-2. The software SPECTRE was originally designed for radiation simulation on electronic devices.

Recognizing a trend in integrated circuit complexity, he extrapolated the tendency and predicted an exponential growth in the available memory and calculation speed of microprocessors which, he said, would double every year (Moore, 1965). With a slight correction (i.e. doubling every 18 months, see Fig. 2-1), *Moore's Law* still holds today.

The American army was a pioneer in the field of integrated circuit EMC. As early as 1965 at the Special Weapons Center, based at Kirtland, New Mexico, they studied the effects of the electromagnetic fields trigged by nuclear explosions on electronic devices used in missile launch sites. As a result of this effort, the simulation software SPECTRE (Sedore, 1967a), was developed at IBM (Fig. 2-2) for simulating the effects of nuclear radiation on electronic components (Sedore, 1967b). With this software, it was possible to correlate simulations and experimental measurements obtained on an electromagnetic impulse test-bench.

At electronic equipment level, protection techniques were developed to face the couplings with radio and television emitters, radars and nuclear electromagnetic pulses. Several military norms were published in the United States on this subject, on one hand the BE Mil-STD (Military standard) 461, which concerned the interference levels that the equipments must hold (Mil-std, 1967), and on the other, the Mil-STD 462 that specified the measurement methods for electromagnetic interference characterization. One of the earliest academic publications on the simulation of integrated circuit concerned the 741 integrated operational amplifier, and was published by Wooley (1971). The author succeeded in simulating the different stages of this integrated circuit with the simulation software *CANCER,* from Berkeley University (An ancestor of the well-known analog circuit simulator SPICE).



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NOVEMBER 1979 VOLUME EMC-21 NUMBER 4 (ISSN 0018-9375)

A PUBLICATION OF THE IEEE ELECTROMAGNETIC COMPATIBILITY SOCIETY

SPECIAL ISSUE ON RF INTERFERENCE EFFECTS IN SEMICONDUCTOR DISCRETE DEVICES AND INTEGRATED CIRCUITS

Figure 2-3. A special issue on radio-frequency interferences in integrated circuits.

As an Associate Professor at the State University of New York in Buffalo, NY USA, James J. Whalen, was another pioneer in the field of integrated circuit EMC. In 1975, he published studies on the radio-frequency pulse susceptibility of discrete transistors (Whalen, 1975). The *IEEE Transactions on Electromagnetic Compatibility* (Fig. 2-3) invited Prof. Whalen to release a special issue that put together a set of papers focused on the effect of radio frequency interferences on integrated circuits (Whalen, 1979). In his editorial, Whalen justified the interest of that special issue by the rising risk of interference between electromagnetic sources in the Very High Frequency band (VHF 30 MHz-300 MHz), Ultra High Frequency band (UHF 300 MHz-3 GHz) and even Extremely High Frequencies with radars (XHF 3 GHz-30 GHz).

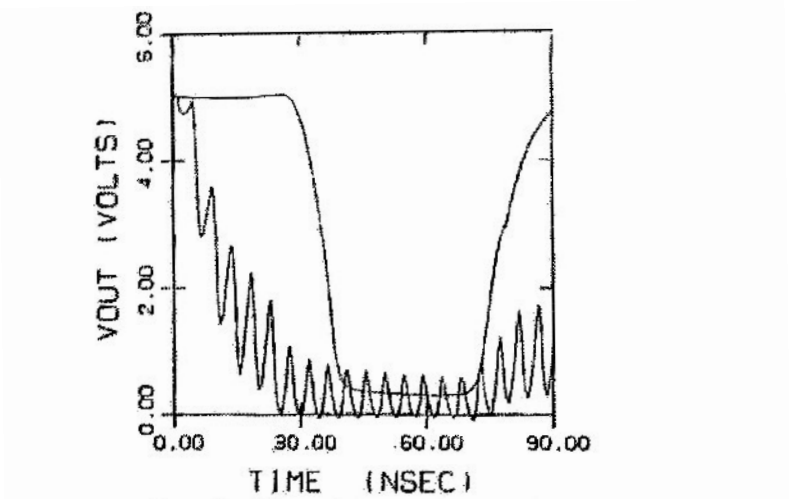
The special issue dealt specifically with the effects of the interference on semiconductor devices and the prediction of these behaviors by means of dedicated simulation tools. The need to modify available device models to account for the unusual conditions of radio-frequency interference was expressed by C. E. Larson (1979), who proposed a modification of the bipolar transistor model.

One year later, Chen and Whalen (1980) proposed a macro-model approach to speed up simulations, an idea that would be utilized by many other engineers and scientists in order to keep the simulation time reasonable while handling ever more complex integrated circuits.

The first ideas on carrying out conducted RF immunity measurements in a compact manner were defined by Bersier (1981) from Swiss Telecom in the beginning of the 80s. Then a method for testing the RF immunity of audio and video products was developed which would not require large semi anechoic rooms and high power RF sources. It was found that the relation between induced common-mode currents and the externally-generated EM-fields on the cables was about 1–5 mA/V/m. Furthermore, it was found that the common-mode impedance as seen by an apparatus in common-mode was around 150 Ω, which is close to the common-mode value as found by other authors.

The first susceptibility analysis of MOS components was published in 1980 and involved memory circuits. J.N. Roach (1981) characterized the sensitivity of 1Kbyte NMOS memories. Some years later, a study was published by (Tront, 1985) concerning the behavior of the 8085 processor in the presence of 100 and 220 MHz radio-frequency interference. Using the simulation software SPICE, he reproduced some of the phenomena observed during measurements (Fig. 2-4).

Watchdog circuits were added to microprocessors (Lu, 1982) for structural integrity checking. Watchdog circuits were found to be of great importance for processor recovery and safe reset after undergoing electromagnetic interference.



V_{OUT} versus time for V_M = 20 V and f = 220 MHz. A plot of the unperturbed V_{OUT} is superimposed on the curve.

Figure 2-4. Unperturbed and perturbed signals simulated by (Tront, 1985).

2. RESEARCH IN EMC FOR ICS BETWEEN 1990 AND 1995

Bakoglu (1990) compiled a remarkable synopsis of the parasitic effects in integrated circuits, packaging and printed circuit boards. He described different problems linked to transient current consumption at active edges of the clock and detailed the basic mechanisms for integrated circuit resonance. Package models were provided for Dual-In-Line (DIL), Quad-flat-pack (QFP) and Pin-Grid-Array (PGA) families.

Also in 1990, Kenneally presented measurement results for simple integrated circuits in CMOS and TTL technologies. He noticed that the sensitivity decreased as the radio-frequency interference increased, from 1 to 200 MHz.

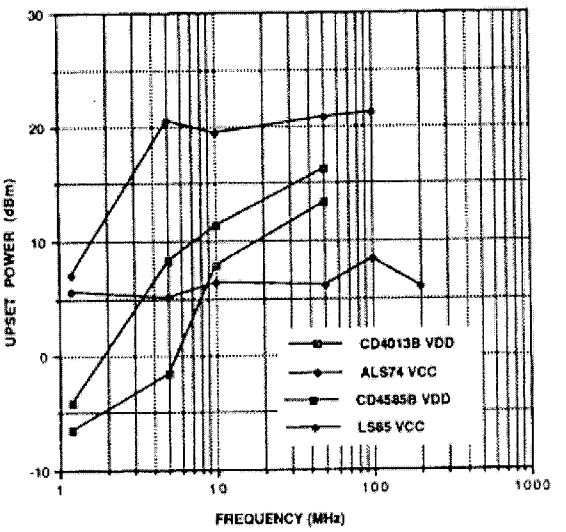


Figure 2-5. Susceptibility thresholds vary depending on the technology.

Significant differences were exhibited depending on the fabrication technology. In all cases, CMOS circuits tended to be less robust than TTL circuits (Fig. 2-5). As a Ph.D. student at the University of Toronto, Laurin (1991) published a study of the effects of radio frequency perturbations on the oscillator circuits used in a Motorola 6809 processor. When placing an electric current loop close to the oscillator, he observed clock jitter, function losses in the microprocessor and data losses on the serial data bus (Fig. 2-6).

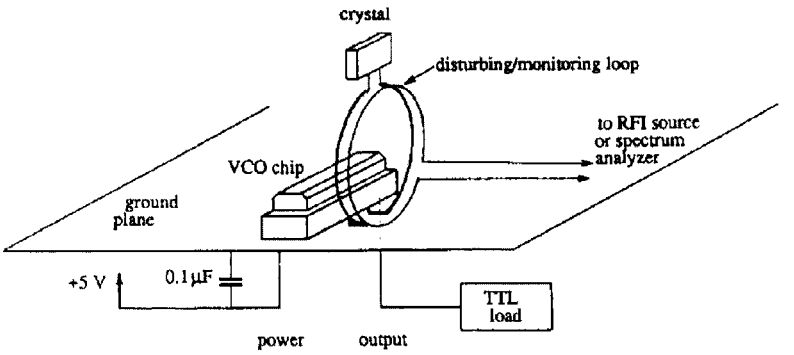


Figure 2-6. Perturbation of an oscillator using a magnetic probe (Laurin, 1991).

Also in relation with microprocessors, Tang (1993) from the University of Singapore showed that electromagnetic interference could cause non-fatal failures that resulted in counting inaccuracy in microprocessors. He performed conducted and radiated susceptibility measurements, and could demonstrate a specific byte-swap problem on the most significant byte of a counter, leading to severe counting errors. Solutions based on software modification and PCB layout improvement was proposed. The author pointed out that low-speed systems were vulnerable to EMI as much as high-speed systems.

Many EMC books published in the early 90s mainly focused on printed-circuit-board EMC. Most of these books only gave a little insight in specific problems of integrated circuits. In chapter 3 of his book "*Principles and applications of EMC*", Weston (1991) compared the switching characteristics of various families of integrated circuits, as well as their impacts on radiated and conducted emission (Weston, 1991).

A study was published by Graffi (1991) about the behavior of 741 operational amplifiers when a 200 KHz - 50 MHz interference signal was superimposed on normal signals. He obtained good correlation between experimental measurements and simulations using simplified macro-model, which accelerated the computation by a factor of up to 50.

Time-Domain Reflectometry (TDR) was used by (Hauwermeiren, 1992) for the characterization of package behavior at very high frequencies. A simple model based on discrete R, L, C components was proposed for Leadless Chip Carriers (LCC) and Pin Grid Arrays (PGA). His approach wais very close to the one later proposed by the IBIS group for the modeling of packaging.

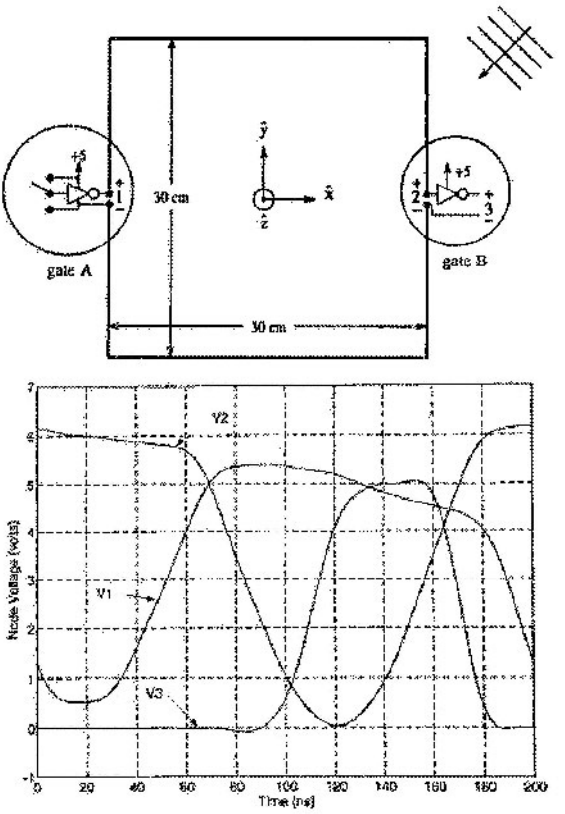


Figure 2-7. Parasitic commutation of an inverter circuit output (V3) connected to a long wire (Near end V1, far end V2) acting as a receiving antenna for a field of 2 V/m.

Synchronous switching noise is one of the most significant chip-level concerns for EMC and signal integrity engineers. One of the earliest publications on this topic was a paper by (Downing, 1993) on the characterization of decoupling capacitance effects including on-chip decoupling and decoupling close to the integrated circuit.

3. SUSCEPTIBILITY OF INTEGRATED CIRCUITS (STARTING 1995)

The effects of an electromagnetic wave coupling to PCB traces and the consequences of this coupling on simple circuits were analyzed by Laurin (1995). With field strengths as high as 200 V/m, no disturbance was observed on the component.

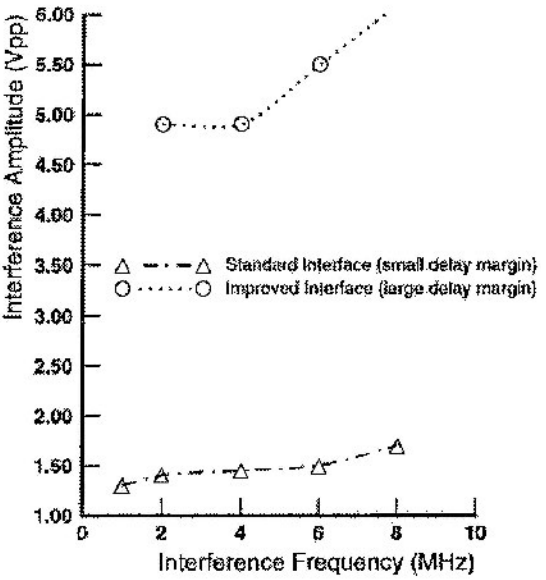


Figure 2-8. Two circuits with same functionality but very different immunity levels.

Adding a long metal wire that was half-a-wavelength long to the interference frequency allowed fields as low as 2 V/m to cause severe malfunctions due to erroneous switching (Fig. 2-7). The authors differentiated between a *static regime* and *transient regime*. In the static regime, only perturbations with high energy affected logic levels. In the transient regime, even weak perturbations could affect switching delays and circuit thresholds.

Chappel (1997) discussed the possibility of *hardening* integrated circuits to electromagnetic interference by specific design techniques that raised the immunity level of ICs from a low 1.5 V to more than 5 V, in the frequency range 1 to 10 MHz (Fig. 2-8). Several other circuits have also been proposed that exhibit a high immunity to RFI including Schmidt triggers, low-voltage differential swing circuits and delay–insensitive structures.

Hattori (1998) demonstrated the advantages of frequency-domain simulations as opposed to time-domain analysis. This approach proved to be very efficient to obtain the behavioral response of analogical circuits quickly, and more particularly the offset variations versus frequency.

While the demand for mobile communications was exploding, the behavior of integrated circuits in the presence of GHz-range interference was not extensively studied.

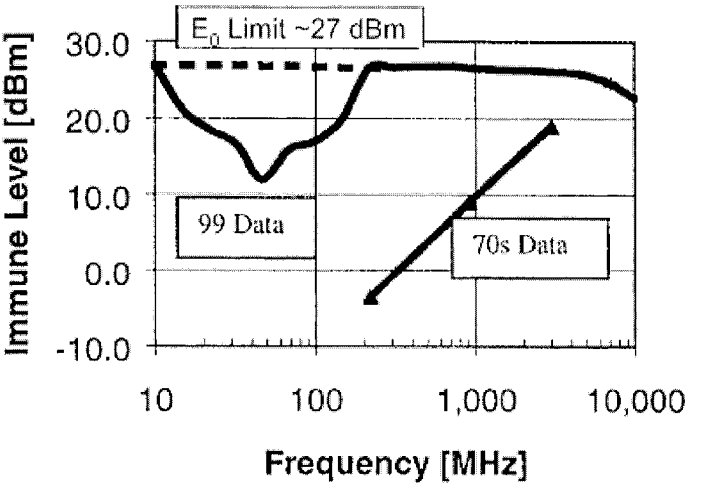


Figure 2-9. : Immunity of the NAND 74LS00.

In 2000, an updated version of the *Integrated Circuit Electromagnetic Immunity Handbook* published by NASA gave valuable information on the immunity levels of simple integrated circuits up to 10 GHZ (Sketoe, 2000). Chapter 4 presented measurement results concerning simple components, with a very interesting comparison with similar measurements performed in the early 80s. The frequency range was 10 MHZ to 10 GHz. From the results shown in Fig. 2-9, the immunity level of recent components has proven to be higher that 70s versions, that could be explained by input/output protection improvements.

Through experience gained on a variety of microprocessors and micro controllers, some engineers started developing strategies for hardening microprocessor-based systems. Coulson (1997) identified the vulnerable points, proposed specific circuits such as supply supervisors or watch-dogs, but also some software-based techniques such as memory integrity checking, token passing, and redundancy coding. Campbell (1998) claimed that by simple *defensive software* programming, a micro controller immunity performance could be increased up to one order of magnitude at a low implementation cost.

Less optimistic, Ong (2001) studied the effect of software-based techniques on the reliability of embedded applications in the presence of EMI. The "defensive software" approach based on function tokens was found to be inefficient and not generally applicable. In contrast, the implementation of NOP fills in unused memory proved to have a positive impact on system reliability.

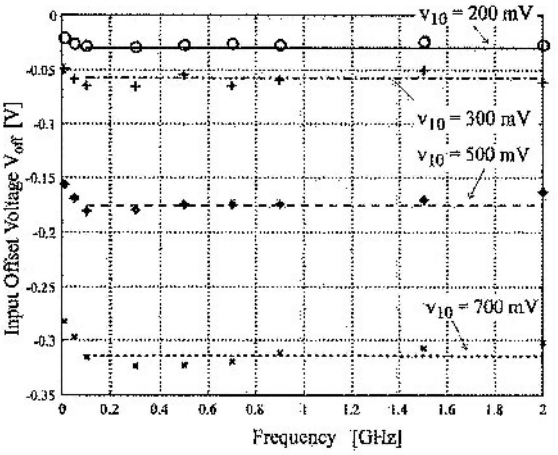


Figure 2-10. Response of an operational amplifier to 100 MHz-2 GHz RFI using microwave probing directly on the chip.

More recently, Fiori (2002) published a study of radio-interference effects on analog amplifiers, up to 2 GHz. The measurement setup employed microwave probes directly positioned on the chip so as to maintain a 50-Ω impedance from the measurement equipment to the integrated circuit (Fig. 2-10). He observed increased DC shifts of the amplifier offset with the RFI amplitude which surprisingly remained almost constant from 100 MHz to 2 GHz.

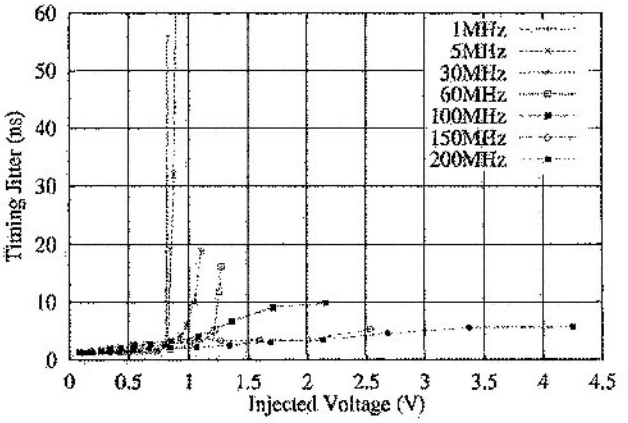


Figure 2-11. Modification of switching delays as a function of amplitude and interference frequency.

Robinson (2003) modeled the variation of signal propagation delays in integrated circuits due to electromagnetic aggressions. Although the experiments were only conducted up to 200 MHz (Fig. 2-11), the component sensitivity to interference tended to decrease with frequency, at frequencies well above the designed operating frequency of the device under test.

4. PARASITIC EMISSION OF INTEGRATED CIRCUITS

Goodman (1995) published results of a comparison between measurements and simulations of signal propagation in Pin-Grid Arrays (PGAs). He showed varying deleterious effects of signal transmission depending on the package pins, explored ground signal delays, and used simple R,L,C elements as proposed in (Hauwermeiren, 1992), but for significantly higher frequencies.

While using discrete R,L,C components to model package leads, bonding and integrated input/output structures, he used transmission lines for the printed circuit board tracks to validate the model up to 4 GHz.

Constant increases in integrated circuit complexity require packages with higher pin density and broader bandwidth. (McCredie, 1996) successfully modeled the switching noise of an ASIC mounted on a compact BGA with around 1000 I/O pins using distributed current sources, on-chip and on-package decoupling capacitance models as well as serial connection inductances (Fig. 2-12).

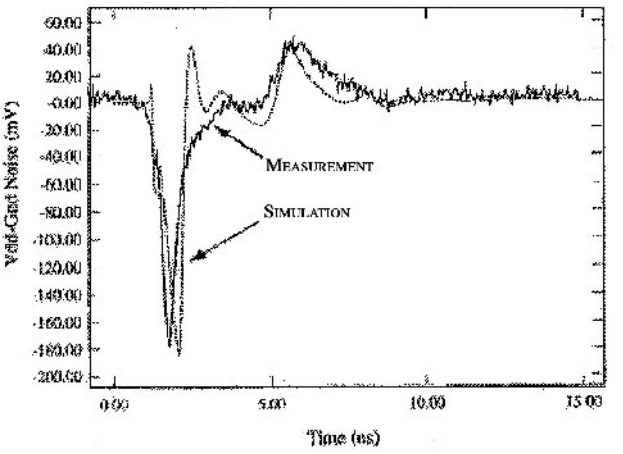


Figure 2-12. Switching noise measurement and modeling on high complexity pin grid array.

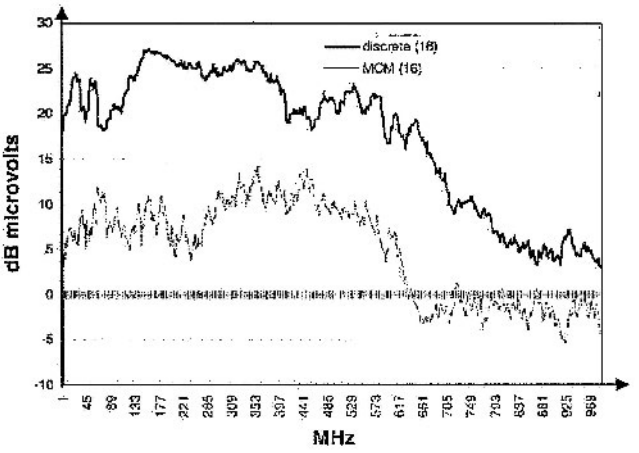


Figure 2-13. Package influence on the radiated emission in TEM cell (dBμV vs. frequency, in MHz).

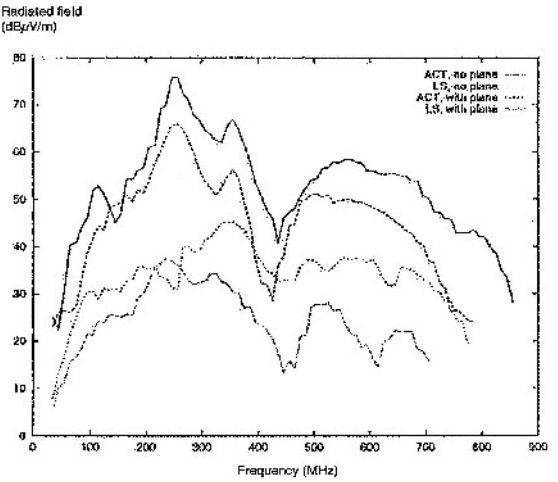


Figure 2-14. Far-field emission (50 MHz-900 MHz) measured at a 3-m distance, produced by simple ICs for varying technologies.

The same year, T. Williams published a practical book on design with EMC constraints with one chapter dedicated to integrated circuits (Williams, 1996). In the United States, the Society for Automotive Engineering (SAE) proposed a measurement method for radiated emissions of integrated circuits using a TEM cell.

Very interesting comparative studies were published by Slattery (1997) regarding 8 and 16 bit microcontrollers, that characterized the impact of technological variations, package and temperature on the spectrum (Fig. 2-13).

Robinson (1998) compared the radiated emissions produced by different families of logic circuits. An antenna was mounted 3 m away from the test board on an open-field test site. Results were provided for simple circuits such as inverters and NAND gates from various logic families: ACT (Advanced CMOS-TTL), FCT (Fast speed CMOS), HC (High speed CMOS), and HCT (High speed CMOS-TTL). Significant behavioral differences were observed, as illustrated in Fig. 2-14.

The author claimed that the peak amplitude E in the measured spectrum could be approximated by the formula

$$E = kAf_{\max}^{0.7} \tag{2-1}$$

where:
k=constant related to the integrated circuit design and technology
A=supply amplitude (V)
fmax=operating frequency (Hz).

Jonghoon (1998) presented the TEM cell measurements of complex processors with and without local decoupling capacitors. This measurement technique is described in details in Chapter 4. The observed benefit of on-chip decoupling capacitors was significant (Fig. 2-15).

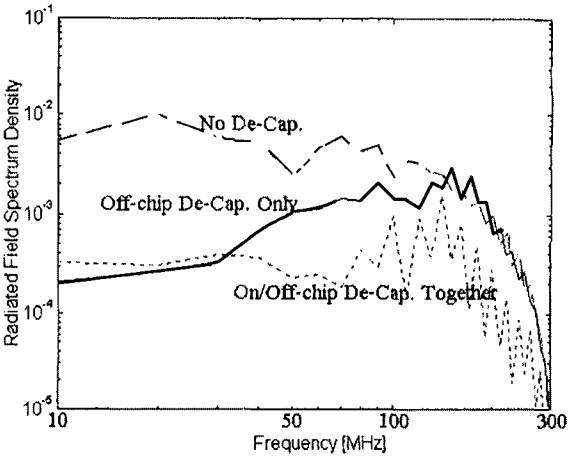


Figure 2-15. Impact of on-chip and off-chip decoupling capacitance on radiated emissions.

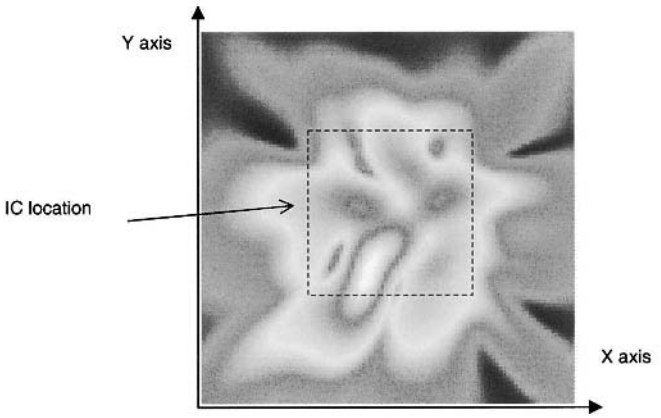


Figure 2-16. Near-field scanning.

Several works were published soon after (Steinecke, 2000; Van Wershoven, 2000) that confirmed that implementing large embedded capacitors, with values from 1 to 50 nF depending on the technologies and the size of the die, was a very efficient way of reducing emissions. Slattery also used the TEM cell (1999) to compare the emission characteristics of several microprocessors.

Van Wershoven (2000) also showed that active slew-rate control could further reduce radiated emissions. Another approach was suggested by Kim Soo-Hyung, who analyzed the impact of absorbent materials (Soo-Hyung 2000) such as ferrites mixed with epoxy, and observed a 3 to 20 dB reduction of the harmonics, especially beyond 300 MHz.

The near field scanner was adapted to the problem of the integrated circuits in 1995 by K. Slattery who was a consultant for Chrysler Corporation at the time. Slattery (1999) also designed and built one of the first near-field measurement scanners with a resolution high enough to map the fields above integrated circuit packages (Fig. 2-16). Many research labs involved in the study of chip-level EMC are now using near-field scanners based on the Slattery design.

Integrated circuit suppliers in Japan are world leaders in the production of low emission processors, in particular for automotive applications. Therefore, it is not surprising to find Japanese authors in scientific publications on the subject. For example, Hayashi (2000) described his approach to low-noise ASIC design, while Takahata (1999) proposed a circuit design model based on power-supply impedance, that provided the foundation for standard model proposals such as (IMIC, 2001).

4.1 Alternatives to Achieve Low Emission

Hardin and colleagues at Lexmark Corporation were probably the first to propose the idea of reducing peak emissions in the harmonics of the clock frequency by fluctuating the clock period in a controlled manner (Hardin, 1994). This idea is illustrated in Fig. 2-17.

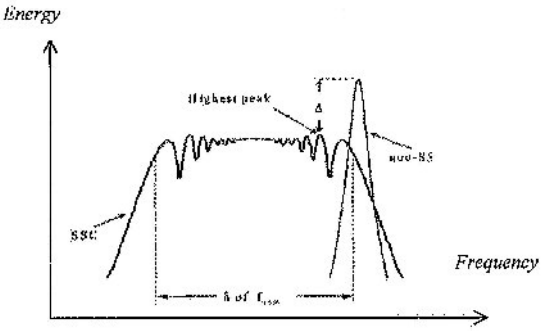


Figure 2-17. The spread-spectrum technique helps to reduce radiated emission.

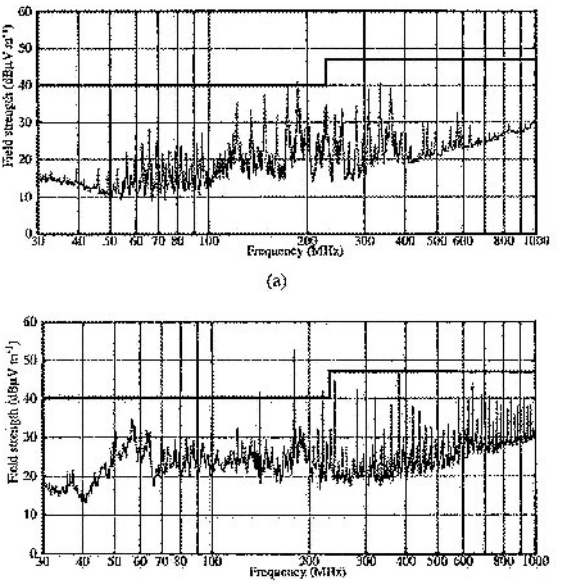


Figure 2-18. Parasitic emission of synchronous processor (a) compared to synchronous ARM60 processor (b).

The energy of a single harmonic concentrated in a very narrow bandwidth is redistributed over a larger frequency band. This noise reduction technique has also been applied to switching power supplies (Feng, 1994). Initially, it was viewed by some experts as a "way to cheat" the radiated emissions test procedures. However, (Slattery, 2001) published experimental results showing that this technique does actually reduce the risks of interference in electronic systems.

An interesting alternative for emission reduction may be found in asynchronous circuit design. Furber published results (1999) showing significant reduction of the peak harmonic (near 180 MHz) as well as high frequency harmonics in the asynchronous version of the ARM60 processor, as seen in Fig. 2-18. An important reference on asynchronous design techniques is the book of Sparso (2001).

5. STANDARDIZATION IN INTEGRATED CIRCUIT EMC

A set of important Electromagnetic Compatibility regulations were implemented in the European community in 1996, which probably revived the interest of the researchers and engineers for this subject, mainly in Europe. The European regulations set maximum limits for parasitic emission levels, as well as minimum immunity levels for most electronic devices.

At the component level, the most important standards were developed under the supervision of the international electro technical commission (IEC) which oversees important standardization activity through more than 100 technical committees. One of these committees, called *Technical Committee 47A*, had focused on integrated circuits as early as 1990. The role of this committee was to prepare international standards focusing specifically on logic circuits, memory, converters and hybrid modules. Another sub-committee called *Technical Committee 93*, was established a little later and focused on integrated circuit design automation.

5.1 Measurement Methods

Various measurement approaches for emission and immunity to electromagnetic waves were developed during the 90s in several countries, mainly in France, Germany, Italy, Holland, the USA and Japan. The establishment of these measurement methods was led by the automotive industry, which was facing frequent electromagnetic interference problems due to the increasing number of on-board electronic devices.

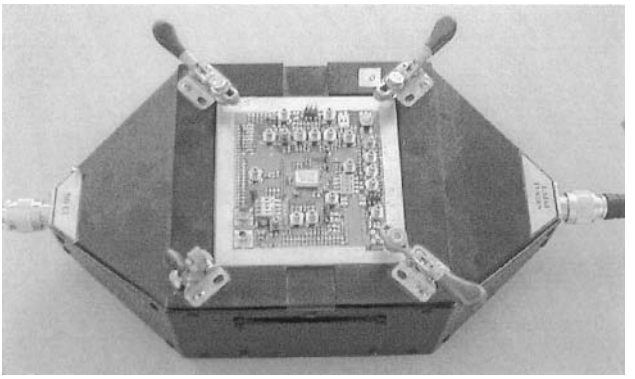


Figure 2-19. The TEM cell standardized in the USA (SAE, 1995).

One of the most common problems was interference in the FM band due to the switching noise of embedded micro-controllers.

The *Society of Automotive Engineers* (SAE) proposed a radiated measurement method using the TEM cell (Fig. 2-19) for the measurement of radiated emissions. A group from Holland proposed a conducted method based on the Workbench Faraday Cage (WBFC), and the German standardization group VDE proposed a conducted measurement method using a 1-ohm resistance in series with the component connection to ground. Researchers in Japan proposed a magnetic loop probing test and the SAE also proposed a near-field scanning technique.

In October 1997, the *Sub-Committee 47A* of the IEC decided to create a working group (WG9) to analyze the suggested measurement methods for integrated circuits. The group held several meetings from 1998 to 2000, notably in Seoul and Paris. After considerable discussion, it was decided to create a "tool box" of five methods for evaluating integrated circuit EMC: a TEM cell measurement, a surface scan technique, a 1Ω/150Ω method, measurement in a WBFC and the magnetic probe method. These measurement procedures are described in the document IEC 61967 "Integrated circuits – Measurement of electromagnetic emissions 150 KHz to 1 GHz" (IEC, 2001):

- Part 1: General conditions and definitions.
- Part 2: Measurement of radiated emissions – TEM-cell method.
- Part 3: Measurement of radiated emissions – Surface scan method.
- Part 4: Measurement of conducted emissions – 1Ω/150Ω direct coupling method.
- Part 5: Measurement of conducted emissions – Workbench Faraday cage method.
- Part 6: Measurement of conducted emissions – Magnetic probe method.

A comparative study of these measurement techniques was published by Lubineau (1999), as well as Fiori (2003) who conducted experimental measurements using these methods on identical devices. Both researchers provided valuable suggestions regarding the measurement setup and limitations. In the *Review of Radio Sciences* edited by Stone (2003), one chapter is dedicated to a synopsis of recent publications in EMC for ICs, with highlights on measurement techniques, modeling and reduction of parasitic emissions, as well as a review of research activities concerning the susceptibility of digital and analog components.

Standard measurement procedures for immunity have also been developed and are described in the five parts of the IEC document 62132 " Integrated circuits - Measurement of electromagnetic immunity » (IEC, 2002). The document is organized as follows:

- Part 1: General conditions and definitions.
- Part 2: Measurement of radiated immunity – TEM cell method.
- Part 3: Measurement of conducted immunity – Bulk current injection method (BCI).
- Part 4: Measurement of conducted immunity – Direct power injection method (DPI).
- Part 5: Measurement of conducted immunity – Workbench Faraday Cage method.

5.2 An EMC Model for Components

The first important contribution to the EMC modeling of components came from the IBIS (*I/O Buffer Information Specification*) group that proposed a standard description of the electric performance of the input/output structures of integrated circuits (Fig. 2-20).

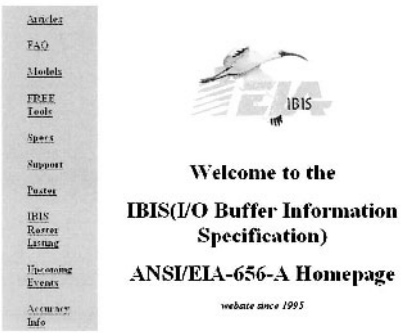


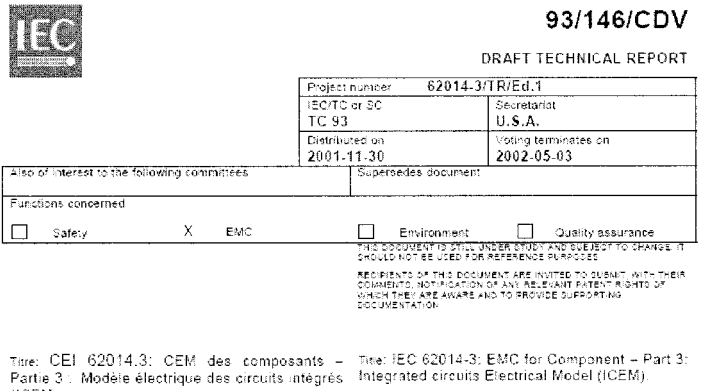
Figure 2-20. The IBIS home page.

The IBIS format was created by Intel Corporation in the early 90s, and was improved in successive versions. In 1993, a group called the IBIS Open Forum was created on the basis of voluntary contribution and association. In 1995, they became affiliated with the *Electronic Industries Alliance* (EIA).

The forum meets on a monthly basis using teleconferences, and works on updates of standards and on technical improvements by means of BIRDs (*Buffer Issue Resolution Documents*). Bob Ross, the coordinator of this forum for several years, has helped to coordinate rapid improvement and word-wide recognition of this format as a standard. The IBIS specification was ratified in 1995 in version 1.1 under the acronym ANSI/EIA-656.

The IBIS standard has been constantly updated since that time (IBIS, 2001), and version 4.1 was ratified in 2004. Details on the IBIS format are provided in chapter 5 of this book. From an electromagnetic compatibility point of view, IBIS provided information about the inputs and outputs of integrated circuits that was not previously available in data sheets. However, it did not provide any information about the core noise or high-frequency currents on the power supply pins.

In 1997, it was decided to create at IEC an EMC task force for which the assigned objective was to promote progress in the study of integrated circuits modeling and simulation. The *Working Group 6* (WG6) had to propose an EMC model for integrated circuit devices and to submit it to national committees for remarks and suggestions.



93/146/CDV

DRAFT TECHNICAL REPORT

Project number: 62014-3/TR/Ed.1	
IEC/TC or SC: TC 93	Secretariat: U.S.A.
Distributed on: 2001-11-30	Voting terminates on: 2002-05-03
Also of interest to the following committees:	Supersedes document:
Functions concerned: ☐ Safety X EMC ☐ Environment ☐ Quality assurance	

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Titre: CEI 62014-3: CEM des composants – Partie 3 : Modèle électrique des circuits intégrés (ICEM)

Title: IEC 62014-3: EMC for Component – Part 3: Integrated circuits Electrical Model (ICEM)

Figure 2-21. The ICEM emission model proposal to IEC.

Table 2-1. The members of the IEC technical committee focused on EMC of integrated circuits in 2005.

Name	Affilation	Representing
Gunter Auderer	Freescale, Munich	Germany
Ross Carlton	Freescale, Austin	USA
Mart Coenen	Philips Semiconductors	Netherlands
M. Joester	Siemens Automotive Regensburg	Germany
F. Klotz	Infineon,	Germany
J. Kolodziejski	University Warschau,	Poland
H. W. Luetjens	Philips Semiconductors	Germany
C. Marot	Siemens Vdo Toulouse	France
S. Mitani	Hitachi	Japan
A. Nakamura	Hitachi	Japan
C. Terrier	EM Microcelectronic Marin SA	Swiss
O. Wada	Okayama university	Japan
T. Watanabe	NEC	Japan

In France, a research project was initiated by a group of academic and industrial partners in Toulouse from 1997 to 2000. The goals of this project were to establish the foundation for a standard model for predicting the emissions from components, and later to reuse this model for the prediction of immunity in the frequency band 1 MHz – 1 GHz. Starting with the characterization of simple components (Lubineau, 1999), a generic model applicable to complex integrated circuits such as ASIC and micro-controllers was proposed under the name ICEM (*Integrated Circuit Emission Model*) (Ben Dhia, 2002). The French UTE group worked on a standard proposal based on ICEM (Fig. 2-21) and applied the approach to commercial components (Lochot, 2003). At the end of 2002, the ICEM proposal appeared on the IEC web site, under the name *IEC 62014-3: Models of Integrated Circuits for EMI Behavioral Simulation.*

Another model proposal called IMIC (IMIC, 2001) was put forward by industrial and academic partners in Japan. At the end of 2003, the proposal *Interface Model for Integrated Circuits* (IMIC) appeared as IEC 62404 (IEC 2003).

5.3 Towards a Merge

At IEC level, the TC47A was designated to analyze the EMC standard model proposals ICEM, IMIC, as well as a new Japanese proposal called LECC with the objective of proposing a unified model that would use the best of each proposal.

The list of participants of this working group in 2005 is given in Table 2-1. The group also continued its work on measurement methods and expanded its activities to include the modeling of immunity. In 2005,, more than 13 documents related to integrated circuit EMC were under consideration, which is a good indicator of the challenges and issues of this new field.

6. SPECIAL EVENTS AND PUBLICATIONS

The first workshop dedicated to integrated circuit EMC was held in January 1999 in Toulouse, and the second workshop in June 2000, also in Toulouse. The official language of both events was French. The 3rd workshop (*EMC Compo 02*) was held in English and attracted approximately 70 experts mainly from France, Germany, Italy and Belgium. In 2004, more than 100 experts from academic institutes and industries attended the 4th workshop (*EMC Compo 04)* held in Angers, France. The 2005 edition was organized in November at Munich, Germany (*EMC Compo 05*), and the 2007 edition should take place in the Netherlands.

A special issue of the Microelectronics Journal (Mejo, 2004) was devoted to the EMC of components, on the basis of a selection of papers from the workshop. The special issue included an overview of the standardization efforts, contributions related to emission prediction, test circuit emission characterization, asynchronous design, and analog circuit susceptibility analysis.

7. IC ROADMAPS

Tremendous advances in lithography over the past few years have made GHz clock rate microprocessors available for general use today. The key improvements have concerned the reduction of the device channel and the multiplication of interconnect layers, as shown in Fig. 2-22 where two portions of layout are reported in 0.8μm CMOS process available in 1990 (left) and 90nm (right) CMOS process, available in 2005.

Inside general-purpose electronic systems such as personal computers or cellular phones, we may find numerous integrated circuits (IC) set together with discrete components on a printed circuit board (PCB) as shown in Fig. 2-23. The integrated circuits have various sizes and complexity. The main core consists of a microprocessor, considered as the heart of the system, that includes several million transistors on a single chip.

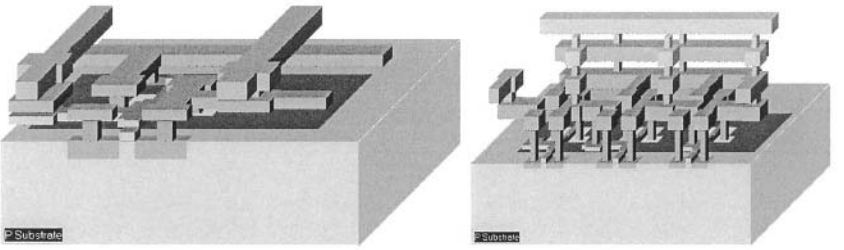


Figure 2-22. Evolution of the integrated circuit technology from 0.8µm 2-metal layer CMOS process down to 90nm 8-metal layer CMOS process.

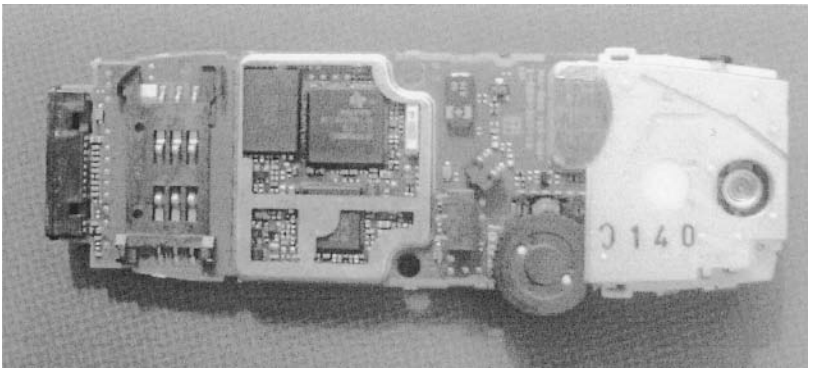


Figure 2-23. Photograph of the internal parts of a cellular phone.

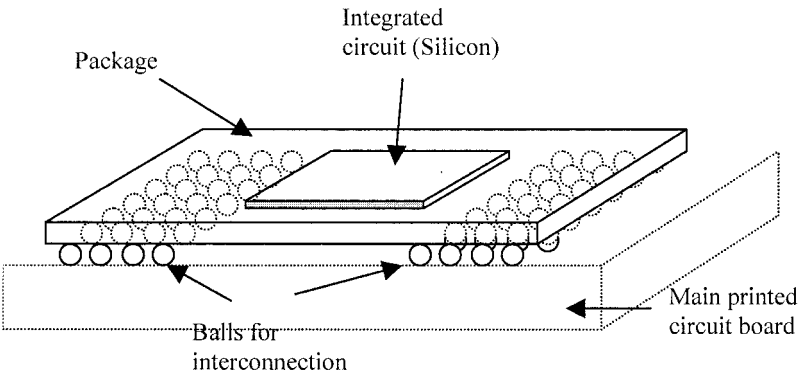


Figure 2-24. Typical structure of an integrated circuit.

The push for smaller size, reduced power supply consumption and enhancement of services has resulted in continuous technological advances, with possibilities for ever-higher integration.

The integrated circuit consists of a silicon die, which is usually around 1 cm x 1 cm in the case of microprocessors and memories. The integrated circuit is mounted on a package (Fig. 2-24) which is placed on a printed circuit board. The active part of the integrated circuit is only a very thin portion of the silicon die.

On the edge of the chip, small solder bumps are used as electrical connections between the integrated circuit and the package. The package itself is a sandwich of metal and insulator materials that convey the electrical signals to large solder bumps which interface with the printed circuit board.

Fig. 2-25 describes the evolution of the complexity of Intel ® microprocessors in terms of devices number on the chip. The Pentium IV ™ processor produced in 2003 included about 50,000,000 MOS devices integrated on a single piece of silicon no larger than 2 x 2 cm.

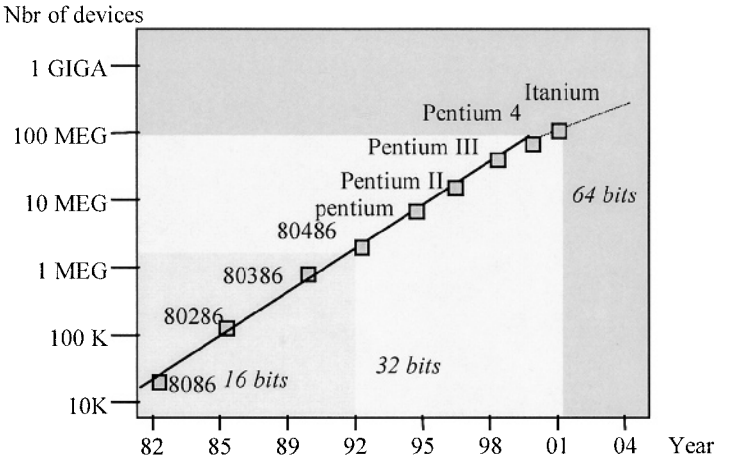


Figure 2-25. Evolution of microprocessors.

Fig. 2-26 illustrates the clock frequency increase for high-performance microprocessors and industrial micro-controllers with the technology scale down. The microprocessor roadmap is based on Intel processors used for personal computers, while the micro-controllers roadmap is based on Freescale micro-controllers used for high performance automotive industrial applications.

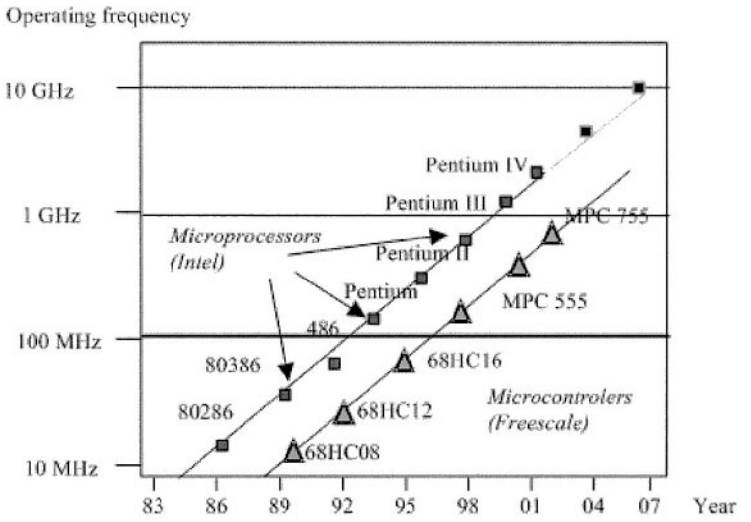


Figure 2-26. Increased operating frequency of microprocessors and micro-controllers.

The PC industry requires microprocessors running at the highest frequencies, which entails very high power consumption (30 Watts for the Pentium IV generation). The automotive industry requires embedded controllers with more and more sophisticated on-chip functionalities, larger embedded memories and interfacing protocols. The operating frequency follows a similar trend to that of PC processors, but with a significant shift.

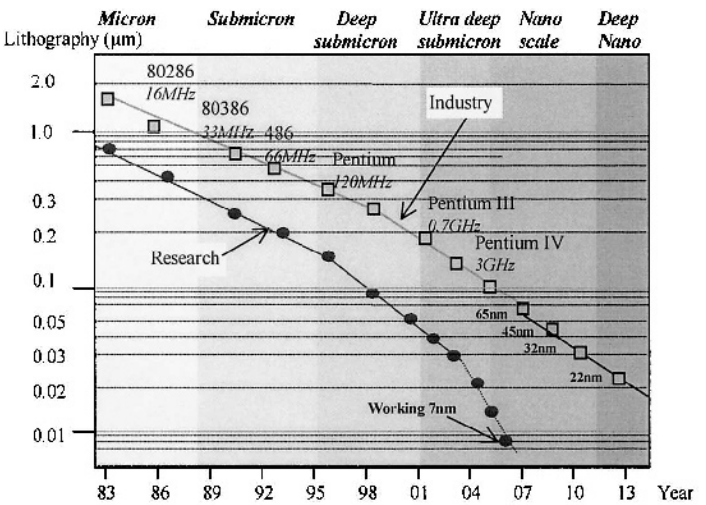


Figure 2-27. Evolution of lithography.

Let us consider four main generations of integrated circuit technologies: micron, submicron, deep submicron and ultra deep submicron technologies as illustrated in Fig. 2-27. The sub-micron era started in 1990 with the 0.8 μm technology. The deep submicron technology started in 1995 with the introduction of lithography better than 0.3 μm. Ultra deep submicron technology concerned lithography below 0.1 μm.

Nanoscale technologies started in 2004 with the 90 nm CMOS technology, followed by the 65 nm. Deep nanoscale technologies should include 32 nm and 22 nm processes, to appear in 2010-2013.

In Fig. 2-27, it is shown that research has always kept around 5 years ahead of mass production. It can also be seen that the trend towards smaller dimensions has accelerated since 1996. The lithography is expected to decrease down to 65 nm by 2007. The lithography expressed in μm corresponds to the smallest patterns that can be implemented on the surface of the integrated circuit. The main consequence of improved lithography is the ability to implement an identical function in an ever-smaller silicon area. Consequently, more functions can be integrated in the same space.

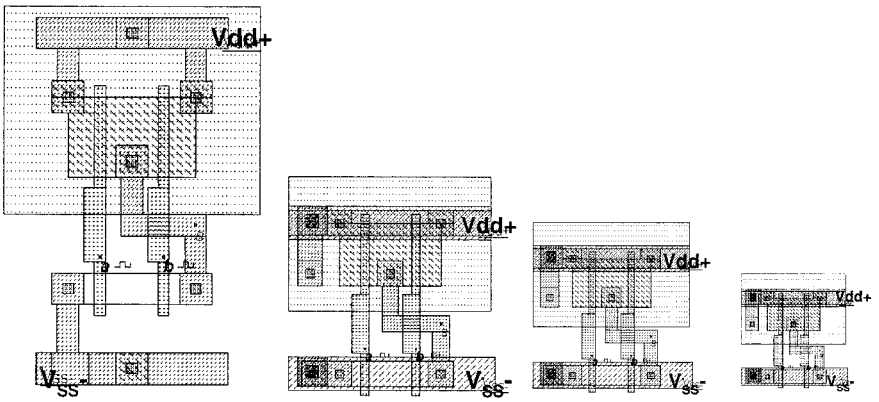
Moreover, the number of metal layers used for interconnects has increased steadily in the course of the past ten years. More layers for routing means a more efficient use of the silicon surface, as is the case for printed circuit boards. Active areas, i.e MOS devices, can be placed closer to each other if many routing layers are provided (Fig. 2-28).

The increased density provides two significant improvements: the reduction of the silicon area goes together with a decrease of the parasitic capacitance of junctions and interconnects, thus increasing the switching speed of cells. Secondly, the shorter dimensions of the device itself speed up the switching, which leads to further operating clock improvements.

When switching, each gate generates a small current pulse which flows mainly on the supply lines. The addition of these elementary current pulses provokes enormous current flows within the chip, close to 100 A in the latest generation of high performance microprocessors.

The increase in operating frequencies, circuit complexity and number of I/Os tends to increase interference, as well as conducted and radiated parasitic emission.

Meanwhile, the silicon wafer, on which the chips are manufactured, has constantly increased in size, thanks to the technological advances. A larger diameter means more chips fabricated at the same time, but it also requires ultra-high cost equipments able to manipulate and process these wafers with an atomic-scale precision. This trend is illustrated in Fig. 2-29. The wafer diameter for 0.12 μm technology is 8 inches or 20 cm (One inch is equal to 2.54 cm). The thickness of the wafer varies from 300 to 600 μm.



(a) 1.2μm, 600 μm^2 (b) 0.5μm, 230μm^2 (c) 0.12μm, 100 μm^2 (d) 90nm, 40 μm^2

Figure 2-28. The evolution of the silicon area used to implement a basic logic gate.

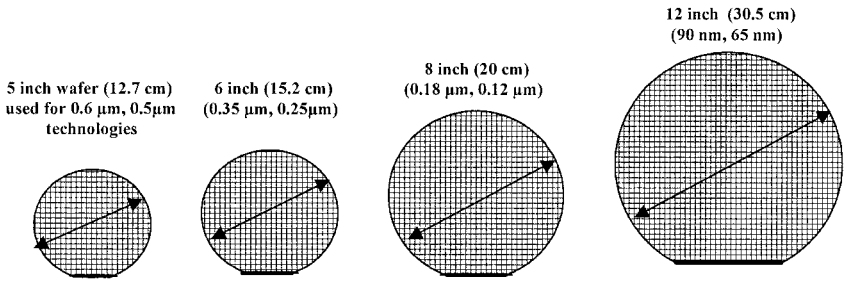


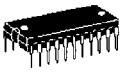
Figure 2-29. The silicon wafer used for patterning the integrated circuits.

8. PACKAGE ROADMAP

So far, the packaging of integrated circuit has been improved so as to increase the number of input/outputs (Table 2-2).

The packaging technology has rapidly improved in terms of I/O density, from the early Dual-in-line structures to the ultimate "Chip-scale" packaging (Fig. 2-30). The most common packaging technology for microprocessors and micro-controllers is the Ball-gate-array (BGA) and Fine pitch Ball Gate Array (FBGA) technology.

Table 2-2. Packaging aspect and I/O number.

Packaging	Definition	Maximum number of I/Os
	Dual In Line (DIL)	40
	Shrink Dual In Line (SDIL)	100
	Small Outline Package (SOP)	100
	Quad Flat Pack (QFP)	250
	Ball Gate Array (BGA)	1000
	Fine Pitch Ball Gate Array (FBGA)	3000
	Chip Scale Package (CSP)	>5000

The integrated circuit is usually connected to the package by bonding wires or solder balls. In the first case, the bonding wires are made of gold. The wires build the link between the pads and the package leads. An example of package connection using bonding wires is shown in Fig. 2-30, for a Quad Flat Pack (QFP).

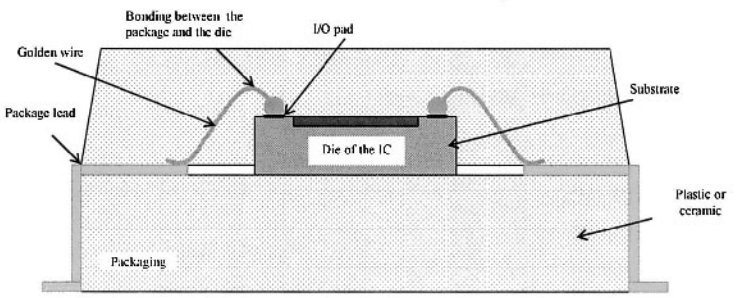


Figure 2-30. The structure of a Quad flat pack (QFP).

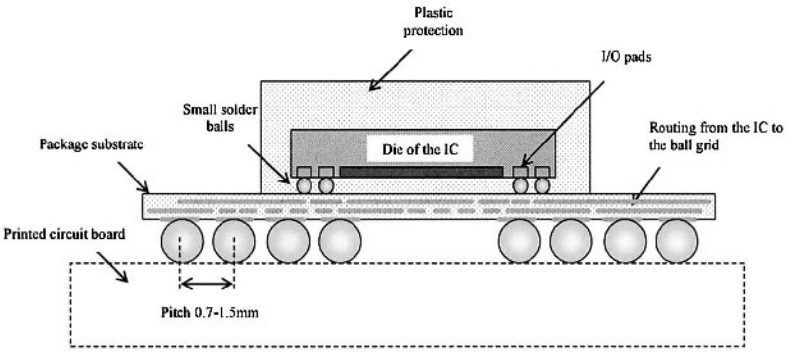


Figure 2-31. The die is attached to the package using micro balls, then the package is linked to the PCB via solder balls to the printed circuit board (BGA).

As the complexity of integrated circuits has kept increasing, a new type of link has been invented, thus creating all the connections between the die and the package in one single step. This technology, called ball grid array, was introduced some years ago and is now commonly used for integrated circuits with more than 200 pins. The cross-section of a ball-grid array and one integrated circuit example are proposed in Fig. 2-31. The die of the integrated circuit is flipped and connected to a specific package thanks to small solder balls.

The package is used as a routing matrix from the IC pads (Pitch close to 100 µm) to the ball gate array (Pitch between 500 µm and 2 mm). The package is a complex network of very thin copper conductors embedded in an insulator. The BGA substrate may include from 2 to 6 metal layers to achieve the routing of general purpose signals and the distribution of power supply. In terms of parasitic emission, the trend towards a decrease of lead length reduces the antenna effects of the package and thus contributes to the decrease of parasitic emission. Furthermore, the reduced size of the leads also decreases the coupling of incident waves to the device, and consequently improves the integrated circuit immunity to radio frequency interference. This global trend has been confirmed by (Sketoe, 2000) with the analysis of IC susceptibility for various packaging technologies.

The chip scale packaging (CSP) shown in Fig. 2-32, consists in connecting directly the chip to the printed circuit board without any intermediate package substrate. The die is flipped and electrically connected to the board via solder balls. The routing constraints in the printed circuit board are very strict as the ball pitch may be as low as 200µm. As there is no more antenna effect, both the emission and susceptibility of such packages should be very low, compared to previous package technologies. However, the die itself may act as a patch antenna for frequencies well above the GHz.

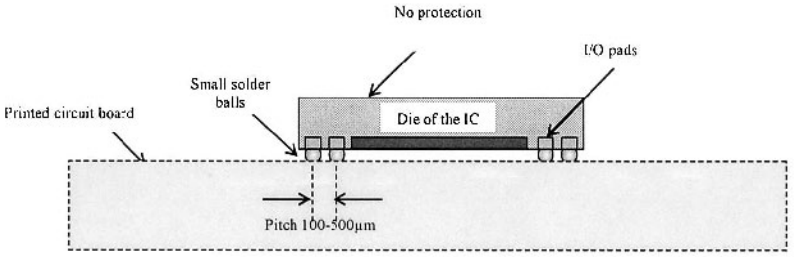


Figure 2-32. The principles of chip scale package

To reduce the surface of the electronic systems, the trend is to stack integrated circuits within a single package, also called System-in-Package. The benefit of this technique is mainly a much more compact system, yet it entails a much more complex assembly as well as reliability and thermal dissipation issues.

One example of stacked integrated circuits is shown in Fig. 2-33. Stacked integrated circuits are particularly attractive when processors, memories, power management, actuators, sensors and radio frequency elements are to be managed simultaneously.

Due to cost and reliability issues, the stacking of heterogeneous integrated circuits may be preferred to a single all-integrated die solution. In terms of EMC, the system-in-package raises the issue of near-field emission and susceptibility between a potential aggressor and its victim situated less than one millimeter away from each other. Coupling may be very strong and lead to a variety of parasitic effects such as capacitive and inductive coupling.

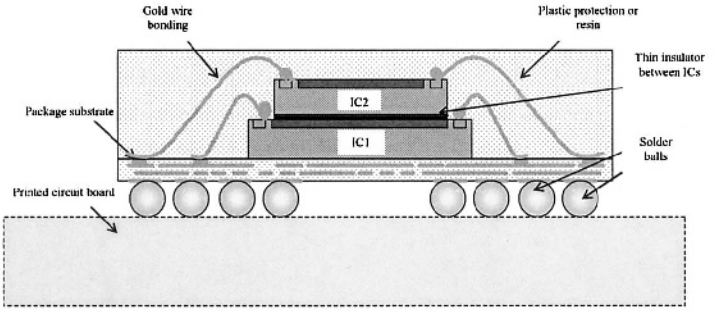


Figure 2-33. The stacking of two different dies in the same package.

9. EMC ISSUES

The need to characterize the electromagnetic compatibility (EMC) performance of integrated circuits (ICs) has been driven by the diverging requirements of semiconductor manufacturers and users on one hand and technology trends on the other.

Modern radio frequency equipments operate at frequency ranges officially called very-high frequencies (VHF), ranging from 30 MHz to 300 MHz, ultra-high frequencies (UHF) ranging from 300 MHz to 3 GHz, and super high frequencies (SHF) ranging from 3 GHz to 30 GHz. Mobiles phones and wireless networking have been the driving applications of radio-frequency integrated circuits, as described in Fig. 2-34.

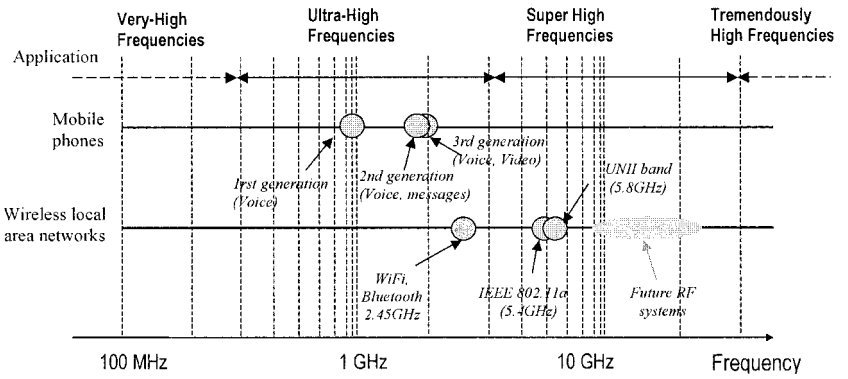


Figure 2-34. The mobile phones and WLAN systems in the frequency spectrum.

The emission spectrum which is strongly correlated with the operating clock frequency, tends to be shifted toward higher frequencies. The IC operating clock frequency, about 10 MHz for early 16-bit processors, is now approaching 1 GHz and is forecast to reach frequencies far beyond the GHz. The parasitic emission spectrum may interfere with several critical frequency bands such as FM radio, mobile phones or local wireless protocols like Bluetooth (Fig. 2-35). Considering the evaluation of parasitic emission level once the integrated circuit has been fabricated, conventional IC design methodologies are obsolete: they often require a redesign with the help of EMC experts (Fig. 2-36).

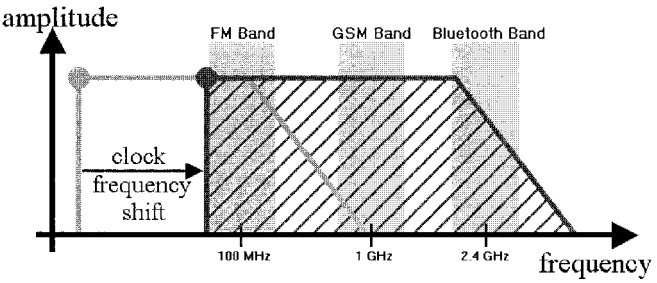


Figure 2-35. Consequences of operating clock increase: parasitic emissions can reach critical frequency bands.

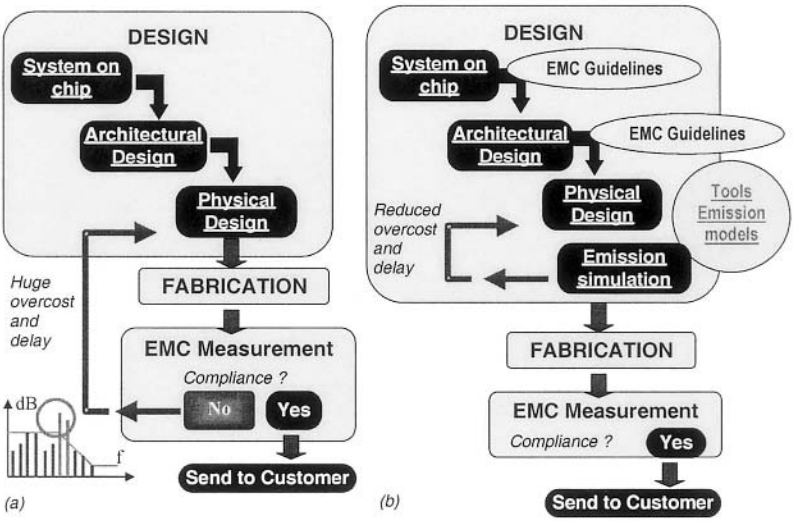


Figure 2-36. Conventional IC design methodologies (a) and low emission design methodologies (b).

But including reduction techniques in the early design phases and simulating the parasitic emission before fabrication, as suggested by low emission design methodologies, require efficient IC models and adequate tools. As a low parasitic emission can represent a significant commercial argument for choosing an integrated circuit, several approaches for reducing parasitic emission at chip level have recently been proposed. Various design strategies have proven efficient to reduce the parasitic emission by several dB for micro-controllers.

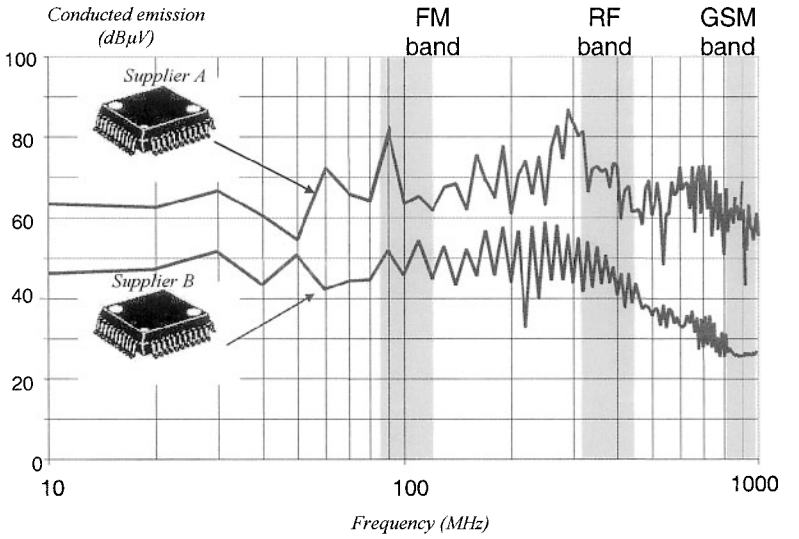


Figure 2-37. Two Ics from different suppliers may exhibit significant differences in terms of parasitic emission.

Fig. 2-37 shows a comparison between two pin-compatible ICs from two different suppliers, mounted on the same test board and measured on the same test bench. Significant differences can be noticed.

Effective techniques involve on-chip decoupling capacitance, current-limiting choke resistance, and supply network optimization. Such design techniques are described in chapter 7. Distributing decoupling capacitors close to main current sources (CPU, clock drivers, PLLs), in combination with current-limiting resistors in series on the supply lines have turned out to reduce the peak harmonics by 10-20 dB.

Other techniques for reducing the parasitic emission concern the use of low-swing clock signals, or asynchronous design approaches.

10. CONCLUSION

Due to increased expectations for low emission and highly immune ICs, EMC measurement methods have been standardized, EMC design guidelines for ICs have been proposed, and later EMC performance prediction tools have been developed since research in that field started in 1970. We expect this field to remain quite active in the future, due to continuous demand towards more complex circuits, higher clock speeds, and lower supply voltages.

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Chapter 3

FUNDAMENTALS AND THEORY

A mathematical background to EMC phenomena

Abstract: This chapter presents five sections explaining some EMC fundamentals and theoretical tools, which aim at providing the reader with basic, understandable and useful theory in the EMC field. The first section deals with the basic theory of electromagnetic emission (electrical dipole, magnetic loop, near field and far field approximations), the second section then brings the concept of the Fourier transform and useful units in frequency domain. The third section deals with transmission lines theory, while the fourth section handles the modeling of RLC passive elements and interconnect in high frequency, the fifth section deals with S-parameter definitions.

Key words: Electromagnetic emission; Fourier; Transmission line; S-parameters; passive elements; skin effect; interconnect

1. BASIC ELECTROMAGNETIC THEORY

This section presents a brief description of basic theory in electromagnetic emission. Any circuit in which some current flows through various shaped wire arrangements radiates electric and magnetic fields. Their emission is similar to the one due to a collection of short electrical dipoles involving two electrical and one magnetic field components, according to analytical formulae given in subsection 1-2.

Assuming these circuits are reduced to a small loop with uniform current flow, electromagnetic field emission may be solved by means of simplified formulae presented in subsection 1-3. Then, depending on the location of the receiver, near field and far field radiation can be respectively differentiated. Furthermore, an electromagnetic wave merging from these circuits carries electromagnetic power, which may be expressed in terms of complex values with reactive power vanishing far away, while active power remains invariant throughout spherical areas centered at the source location. Active power may be related to a radiation resistance.

1.1 Physical context of electromagnetic emission

The circuit depicted in Fig. 3-1 consists of a continuous wave generator connected to a wire and some loads. This produces a current $I(l,t)$, depending on time t and location l, propagating along the wire:

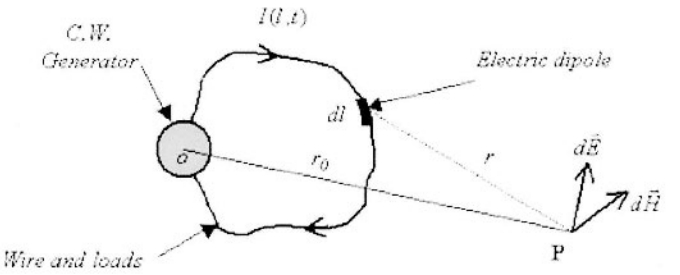

Figure 3-1. [Parameters governing the electromagnetic emission of an arbitrarily shaped electronic circuit.

In terms of time-domain harmonic dependency, this current may be expressed by Eq. (3-1):

$$I(l,t) = I(l)\,e^{j\omega t} \tag{3-1}$$

in which $I(l)$ corresponds to a complex function depending on the location l and the angular frequency ω related with the well-known expression (Eq. 3-2):

$$\omega = 2\pi f \tag{3-2}$$

According to usual electromagnetic theory, electric $\vec{E}$ and magnetic $\vec{H}$ fields radiating from the circuit are expressed in terms of two integrals with elementary fields $d\vec{E}$ and $d\vec{H}$ (Eq. 3-3) attached to an infinitely small length dl of the wire called electrical dipole or Hertzian dipole:

$$\vec{E} = \oint_L d\vec{E} \quad , \quad \vec{H} = \oint_L d\vec{H} \tag{3-3}$$

In these expressions, the L parameter is related to the total length of the wire. Generally, the computation of integrals (Eq. 3-3) can only be achieved numerically. However, assuming that the location of receiver r is small with

respect to the wiring size and the wavelength, these integrals may be solved by an analytical method.

1.2 Formulae of the electrical dipole

In the spherical coordinates depicted in Fig. 3-2, an electrical dipole with a given length dl generates one magnetic field component dH_φ and two electrical field components dE_r and dE_θ. Under the condition that the distance r is large compared with the dipole length dl, the electromagnetic theory leads to the following expressions for dH_φ, dE_r and dE_θ (Eq. 3-4, 3-5 and Eq. 3-6):

$$dH_\phi = \frac{I\,dl\,\sin\theta}{4\pi\ r^2}(1+\gamma r)e^{-\gamma r} \tag{3-4}$$

$$dE_r = \frac{I\,dl}{4\pi\, j\omega\varepsilon_0}\frac{2\cos\theta}{r^3}(1+\gamma r)e^{-\gamma r} \tag{3-5}$$

$$dE_\theta = \frac{I\,dl}{4\pi\, j\omega\varepsilon_0}\frac{\sin\theta}{r^3}\left[1+\gamma r+(\gamma r)^2\right]e^{-\gamma r} \tag{3-6}$$

In these equations, γ corresponds to the propagation constant of electromagnetic waves in free space related to wave number k, velocity of light in vacuum c and wavelength λ (Eq. 3-7):

$$\gamma = jk = j\frac{\omega}{c} = j\frac{2\pi}{\lambda} \tag{3-7}$$

1.3 Emission from a magnetic loop

In the case of a loop-shaped wire with diameter D smaller than the wavelength, the current can be considered as uniform along the wire. Then, integrals (Eq. 3-3) may be solved analytically, and the spherical electromagnetic field components shown in Fig. 3-3 bear simplified equations. Indeed, assuming that the location r of the receiving point **P** is either small or large with respect to the wavelength, the use of the series expansion or the asymptotic limit leads to near field and far field approximations.

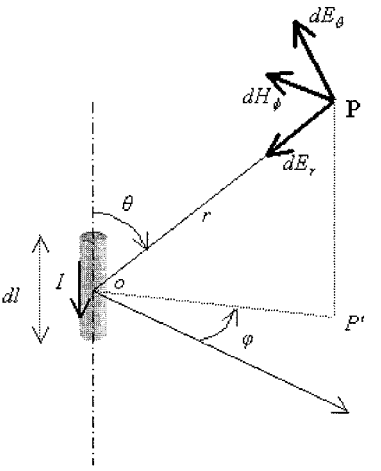

Figure 3-2. Configuration of radiated electric and magnetic field components generated by a uniformly distributed current throughout a thin wire element called "electrical" or "hertzian" dipole.

1.3.1 Near field approximation

Provided that the distance r from the observer is large compared with the loop diameter, the near field formulae are written as (Eq. 3-8 and Eq. 3-9):

$$\lambda >> r \quad \rightarrow \quad H_r \cong \frac{m}{4\pi} \frac{2\cos\theta}{r^3} \tag{3-8}$$

$$\lambda >> r \quad \rightarrow \quad H_\theta \cong \frac{m}{4\pi} \frac{\sin\theta}{r^3} \tag{3-9}$$

In these equations, the m parameter characterizes the magnetic moment expressed in terms of product between the current I and the loop surface ΔS (Eq. 3-10):

$$m = I\,\Delta S \tag{3-10}$$

In Eq. (3-8) and Eq. (3-9), the quasi-static approximation of the magnetic field can be recognized.

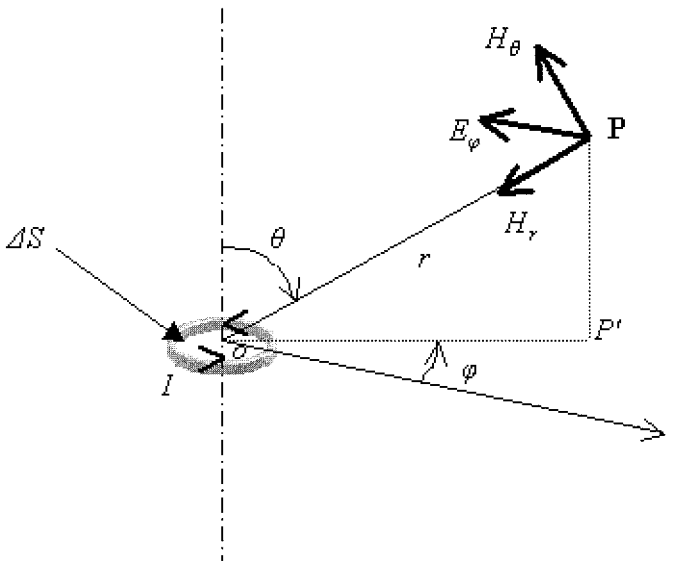

Figure 3-3. Configuration of the radiated electrical and magnetic field components generated by a uniformly distributed current along a small loop called "magnetic dipole".

However, the time dependency of the incoming current I leads to an electric field component orthogonal to the magnetic one, this is proportional to frequency and corresponds to the following expression (Eq. 3-11):

$$E_\phi \cong j\omega \frac{m\mu_0}{4\pi} \frac{\sin\theta}{r^2} \tag{3-11}$$

It can be noticed that the ratio between the electric field and the resulting magnetic field behaves as a reactance lower than the Z_w plane wave impedance in vacuum (Eq. 3-12) (Tesche, 1997):

$$\frac{E_\varphi}{\sqrt{H_r^2 + H_\theta^2}} \cong jZ_w \frac{r}{\lambda} \frac{2\pi \sin\theta}{\sqrt{1+3\cos^2\theta}} \quad \text{with} \quad Z_w = \sqrt{\frac{\mu_0}{\varepsilon_0}} \tag{3-12}$$

1.3.2 Far field approximation

Far away from the loop, the radial magnetic field component H_r vanishes, and only (H_θ , E_φ) remain according to the far field formulae (Eq. 3-13 and Eq. 3-14):

$$\lambda << r \quad \rightarrow \quad H_r \cong 0 \qquad H_\theta \cong \omega^2 \frac{I\,\Delta S}{4\pi c^2} \frac{e^{-\gamma r}}{r} \sin\theta \tag{3-13}$$

$$\lambda << r \quad \rightarrow \quad E_\varphi \cong \omega^2 \frac{Z_w\, I\,\Delta S}{4\pi c^2} \frac{e^{-\gamma r}}{r} \sin\theta \tag{3-14}$$

It can be noticed that the amplitudes of the magnetic field and the electric field decrease with an inversely proportional law to the distance r from the receiver; the propagation in free space thus introduces a phase delay depending on the ratio between r and the wavelength. Furthermore, the previous expressions show that the field amplitude increases with the square of the frequency.

1.4 Radiated power

According to the electromagnetic theory, the power W_r radiating from the circuit can be established with the flux of the Poynting vector $\vec{P}$ throughout a spherical crossing area (Eq. 3-15).

$$\vec{P} = \vec{E} \wedge \vec{H}^* \quad \rightarrow \quad W_r = \oiint_{Sphere} \vec{P} \frac{\vec{r}}{r} dS \tag{3-15}$$

The asterisk corresponds to the conjugated amplitude of the complex vector of the magnetic field. From the previous theory, it can be shown that the power conveyed by near field components is purely imaginary, while it vanishes when the distance to the receiver increases. Conversely, the remaining far field emission power is real and becomes uniform when r increases infinitely in free space. From Eq. (3-13) and Eq. (3-14), the value of the power W_r radiated in far field can be computed as shown by Eq. (3-16):

$$\lambda << r \quad \rightarrow \quad W_r \cong 2\pi Z_w \left(\frac{\omega^2 I\,\Delta S}{4\pi c^2} \right)^2 \int_0^\pi (\sin\theta)^3 \, d\theta \tag{3-16}$$

This integral may be easily solved analytically and is related to the radiating resistance R_r, which is similar to a virtual resistance fed by the current I and dissipating a power strictly equal to W_r ; for the above magnetic loop, R_r is written as (Eq. 3-17):

$$W_r = R_r I^2 \quad \rightarrow \quad R_r = Z_w \frac{\pi}{2}\left(\frac{\Delta S}{\lambda}\right)^2 \tag{3-17}$$

With a *3-cm* diameter loop fed by a current operating at a frequency near *1 GHz*, Eq. (3-17) leads to $R_r \cong 3\,m\Omega$; consequently, at this frequency and with *100 mA*, the emitted power of the loop becomes $W_r \cong 60\,\mu W$.

It can be noticed that this emitted power is very small compared with the inductive power and the wire losses of the circuit. However, in high frequency range, when resonance phenomena occur in the loop, this radiation resistance increases dramatically. Furthermore, for small-sized loops with respect to the distance *r* of the receiver, Eqs. (3-8 and 3-9) and Eqs. (3-13 and 3-14) remain similar whatever the shape of the loop.

1.5 Discussion

The computation of an electromagnetic radiation emitted by a PCB (Printed Circuit Board) may be performed with the above basic theory. However, this approach supposes that the current distribution on PCB tracks is well known. In order to solve this problem, the behavior of a track above a metallic ground plane has to be considered as the one of a transmission line. According to the boundary conditions implied by the voltage source and the load connected to both ends of this line, the current distribution may then be extracted from telegrapher's equations. Another approach consists in solving this problem through lumped elements by means of usual circuit simulators. However, non-linear effects occurring at component level have to be taken into account.

2. FOURIER ANALYSIS

The simulation of integrated circuit parasitic emission is usually conducted in the time domain, using analog tools such as WinSPICE (Winspice). However, the measurements are preferably performed using spectrum analysers rather than oscilloscopes, because of a much higher

sensitivity. The conversion between time domain waveform into frequency-domain spectrum is performed using a Fourier Transform.

Most software calculates the development in Fourier series of the time domain samples, to extract their spectral contents. The mathematical base of the time/frequency transformation is the formula (Eq. 3-18) which describes any function x(t) with a period T, as an infinite sum of cosine and sine of increasing frequency.

$$x(t) = \sum_{n=0}^{\infty} (a_n cos 2\pi n \frac{t}{T} + b_n sin 2\pi n \frac{t}{T}) \tag{3-18}$$

where

$$a_n = \frac{2}{T} \int_0^T x(t) cos(2\pi n \frac{t}{T}) dt \tag{3-19}$$

$$b_n = \frac{2}{T} \int_0^T x(t) sin(2\pi n \frac{t}{T}) dt \tag{3-20}$$

The calculation of a_n and b_n, called coefficients of the Fourier series (Eq. 3-19 and Eq. 3-20), imposes rather heavy calculations, based on integrals and of the multiplications of cosine and sine. The principle interest is in the C_n module expressed by Eq. (3-21).

$$C_n = \sqrt{a_n^2 + b_n^2} \tag{3-21}$$

An algorithm called "Fast Fourier Transform" (FFT) makes it possible to carry out the conversion from time domain to frequency domain much faster than by applying formulations (Eqs. 3-18, 3-19 and 3-20). The FFT algorithm is implemented in the tool IC-EMC given in the companion CD-ROM of the present book. Its major drawback is the constraint on the number of samples for x(t), that should be to the power of 2. By default, the FFT is performed on 1024 points (2^{10}) as shown in Fig. 3-4.

An example of simulated conducted emission on the ground supply pin of a 16-bit microcontroller is given in Fig. 3-5. The spectral decomposition of the waveform is proposed in Fig. 3-6. The horizontal axis represents the frequency, the vertical axis represents the *Cn* value such as given in Eq. (3-21). A high peak of amplitude is thus equivalent to a strong *Cn* value, or a strong cosine or sine amplitude at the corresponding frequency.

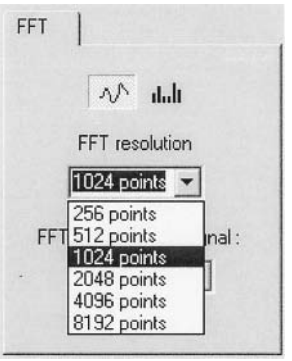

Figure 3-4. The FFT is always applied to 2^n samples.

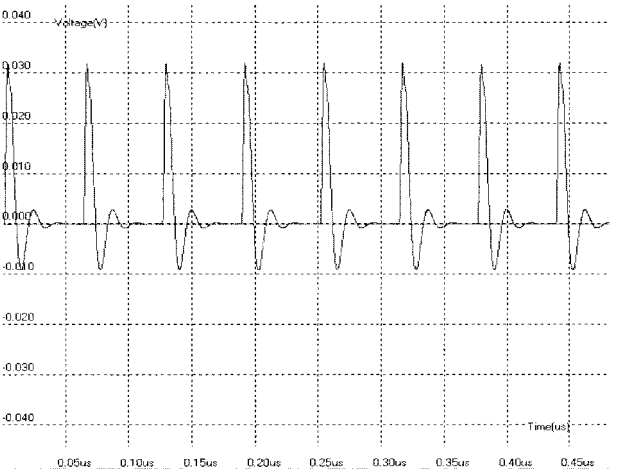

Figure 3-5. Time domain simulation of the conducted noise for a 16-bit microcontroller.

The main problem of using linear axis for frequency and amplitude is its lack of clarity, specifically for harmonics with small amplitude. As most emission level limits are given in log scale, the usual way to display frequency-domain results is in log scale for both X and Y axis, to improve readability and clarity. The voltage represented in Y axis is commonly presented in dBμV expressed by Eq. (3-22).

$$V_{dBuV} = 20.\log\left(V.10^6\right) \tag{3-22}$$

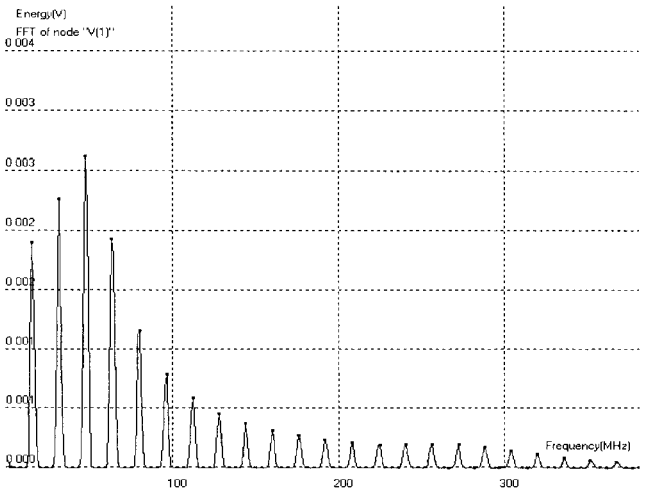

Figure 3-6. Fourier Transform of the conducted noise in linear scale.

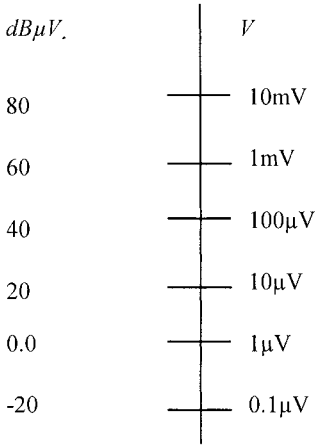

Figure 3-7. Correspondence between Volt and dBμV.

The conversion table given in Fig. 3-7 shows that 1 μV corresponds to 0 dBμV, 1 mV to 60 dBμV and 1 V to 120 dBμV.

The conducted emission example of Fig. 3-6 is redrawn in log/log scale (Fig. 3-8), using the dBμV unit.

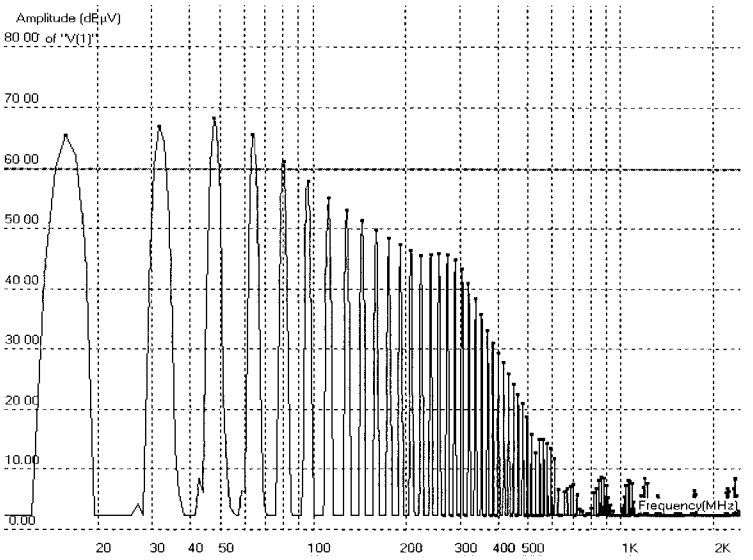

Figure 3-8. Spectrum in log/log, using dBµV.

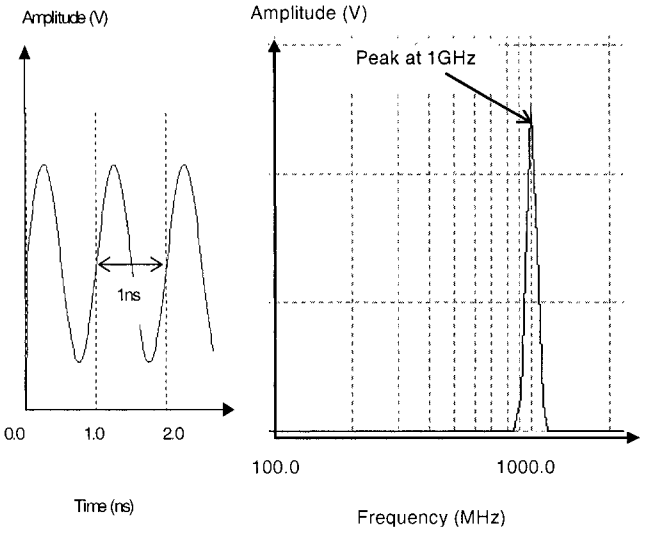

Figure 3-9. A 1 GHz pure sinus in time and frequency domain.

To sum-up, Figs. (3-9 to 3-13) show for each type of signals (pure sinus, square wave, triangular wave and pulsed sinusoidal wave) its time-domain plot and also its spectral contents.

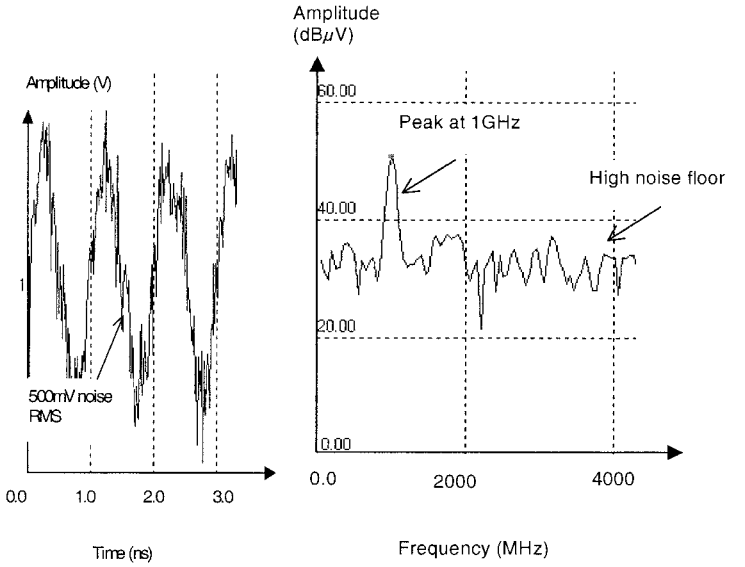

Figure 3-10. A 1 GHz sinus with noise in time and frequency domain.

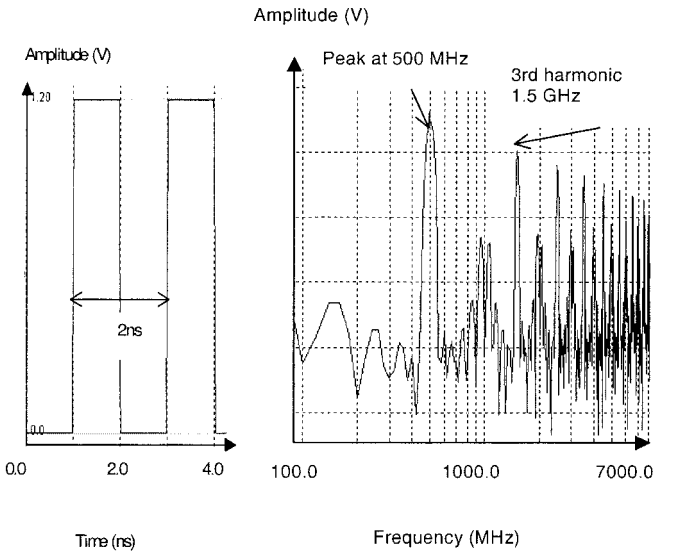

Figure 3-11. A square wave in time and frequency domain.

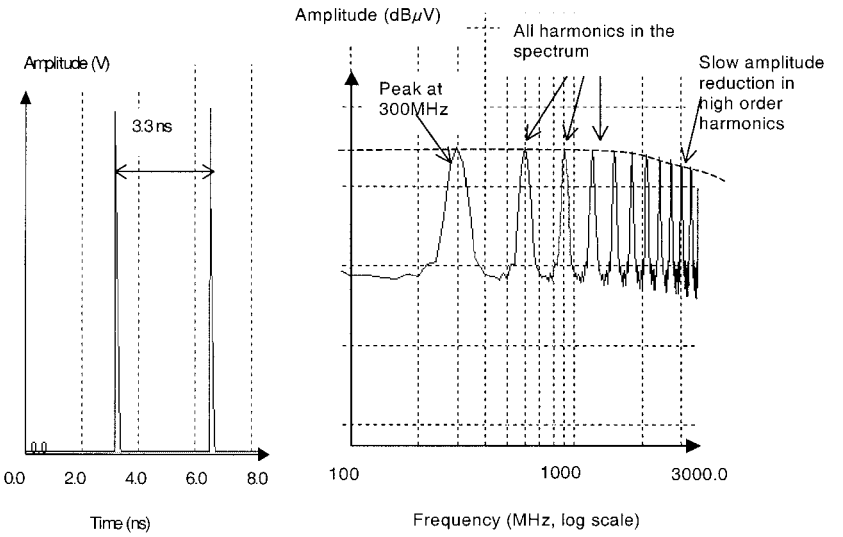

Figure 3-12. A triangular wave in time and frequency domain.

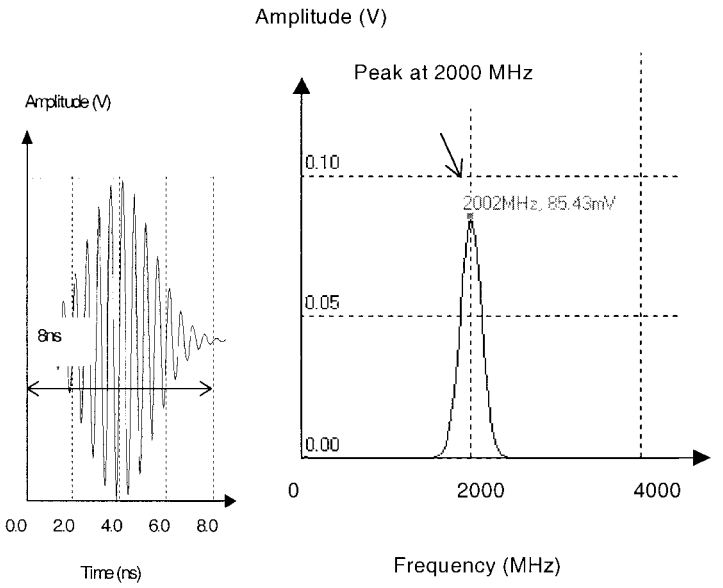

Figure 3-13. A pulsed sinusoidal wave in time and frequency domain.

3. TRANSMISSION LINES

A typical engineering problem involves the transmission of a signal from a generator to a load. The transmission line (TL or t-line) is the part of the circuit that provides the direct link between the generator and the load.

Transmission line theory is a tool, which bridges the gap between circuit theory and a complete field analysis. The sizes of transmission lines lie between a fraction of a wavelength and many wavelengths.

Conversely, in circuit analysis, the physical dimensions of the network are much smaller than the wavelength. A transmission line is considered as a distributed parameter network, unlike a circuit made up of lumped elements. In this case, the voltages and currents associated with a propagating wave in a t-line can vary both in phase and magnitude through the line.

3.1 Transmission line modeling

The signal propagation along a transmission line may be studied in two ways:

- Maxwell method: the transmission line is ranked as a wave-guide. Its structure and its electromagnetic properties are taken into account. Electromagnetic Wave theory is required to describe wave propagation mathematically.
- Kirchhoff method: The transmission line supports the TEM wave (Tranverse ElectroMagnetic). The most important property of TEM waves on transmission lines is that the electromagnetic fields can be uniquely related to a voltage and current.

Therefore, these structures can be analyzed using circuit theory concepts, provided the problem is broken into small parts so that the dimensions of circuit elements are much smaller than a wavelength. To do this, a transmission line can be described by a:

- series resistance per unit length R (due to conductors),
- series inductance per unit length L (due to the mutual inductance between the conductors),
- shunt conductance per unit length G (due to non-ideal isolation),
- shunt capacitance per unit length C (capacitance between the conductors)

A small section of a Δx-long transmission line has thus the following equivalent circuit (Fig. 3-14).

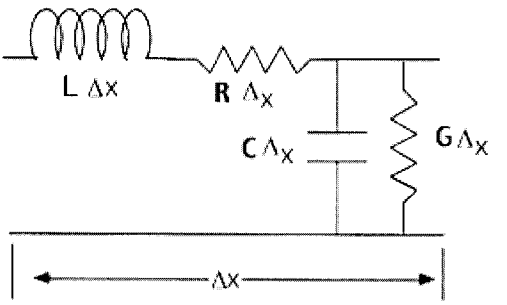

Figure 3-14. Elementary Distributed circuit model of a lossy transmission line.

For example, the parameters of a coaxial cable depend on its geometrical and physical dimensions, as shown in Fig. 3-15. The parameters are given through Eqs. (3-23, 3-24, 3-25, 3-26):

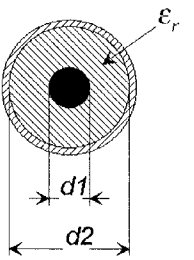

Figure 3-15. Cross-view of a coaxial cable.

$$L = \frac{\mu_0}{2\pi} \ln \frac{d_2}{d_1} = 2 \cdot 10^{-7} \ln \frac{d_2}{d_1} \tag{3-23}$$

$$C = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln \frac{d_2}{d_1}} = \frac{10^{-9}}{18} \frac{\varepsilon_r}{\ln \frac{d_2}{d_1}} \tag{3-24}$$

$$R = \frac{4\rho l}{\pi d_1^2} + R_{ext} \tag{3-25}$$

$$G = 0 \tag{3-26}$$

3.2 Telegrapher's equations

Fixing up the model accordingly, a Δx-long line section can be drawn, as depicted in Fig. 3-14. This ends up with the following version of the telegrapher's equations (Eq. 3-27, Eq. 3-28):

$$\frac{\partial v(x,t)}{\partial x}=-Ri(x,t)-L\frac{\partial i(x,t)}{\partial t} \tag{3-27}$$

$$\frac{\partial i(x,t)}{\partial x}=-Gv(x,t)-C\frac{\partial v(x,t)}{\partial t} \tag{3-28}$$

By differentiating the first equation with respect to x and the second with respect to t, and some algebraic handling, a couple of hyperbolic partial differential equations, each involving only one unknown, can be obtained (Eq. 3-29, Eq. 3-30):

$$\frac{\partial^2 v}{\partial x^2}=RGv+(RC+LG)\frac{\partial v}{\partial t}+LC\frac{\partial^2 v}{\partial t^2} \tag{3-29}$$

$$\frac{\partial^2 i}{\partial x^2}=RGi+(RC+LG)\frac{\partial i}{\partial t}+LC\frac{\partial^2 i}{\partial t^2} \tag{3-30}$$

In the case of a lossless line: $G = R = 0$.

Both equations then degenerate into the exact wave equation (Eq. 3-31, Eq. 3-32):

$$\frac{\partial^2 v}{\partial x^2}=LC\frac{\partial^2 v}{\partial t^2} \tag{3-31}$$

$$\frac{\partial^2 i}{\partial x^2}=LC\frac{\partial^2 i}{\partial t^2} \tag{3-32}$$

3.3 Signal propagation in a lossless line

Equations (3-31) and (3-32) clearly show that the signal is propagating with a velocity v (Eq. 3-33):

$$v=\frac{1}{\sqrt{LC}}=\frac{1}{\sqrt{\varepsilon\mu}} \tag{3-33}$$

$\tau=\sqrt{LC}$ is the propagation delay in a transmission line.

The solutions to these wave equations are superpositions of forward and reverse waves (Eq. 3-34, Eq. 3-35):

$$v(x)=v_1\exp(-\gamma x)+v_2\exp(+\gamma x) \tag{3-34}$$

$$i(x)=i_1\exp(-\gamma x)+i_2\exp(+\gamma x) \tag{3-35}$$

in which:

$\gamma=j\omega\sqrt{LC}$ is the propagation constant $(=\sqrt{(R+jL\omega)(G+jC\omega)})$ in the general case.

Just like with plane waves, the characteristic impedance, namely the voltage-to-current ratio (for positive traveling waves) is defined as Eq. (3-36):

$$Z_c=Z_0=\frac{v_1}{i_1}=\sqrt{\frac{L}{C}} \tag{3-36}$$

$Zc=\sqrt{\frac{R+jL\omega}{G+jC\omega}}$ is the characteristic impedance in the general case.

For a transmission line, the voltage reflection factor or reflection coefficient (at the load Z_L) is defined as the ratio of the reflected voltage over the incident voltage (Eq. 3-37), which can be generally complex:

$$\Gamma_L=\frac{Z_L-Z_c}{Z_L+Z_c} \tag{3-37}$$

The combination of forward and reverse travelling waves produces a standing wave, so-called because the locations of maximum and minimum signals do not vary with time. The actual shape of this standing wave is a function of the load impedance. The standing wave ratio (SWR) is defined as Eq. (3-38):

$$SWR=S=\frac{|v\max|}{|v\min|}=\frac{1+|\Gamma_L|}{1-|\Gamma_L|} \tag{3-38}$$

3.4 Load conditions

If Z_L is the load impedance, d the distance between this load and a given position of the transmission line, it can be easily demonstrated that the impedance Z(d) at this position is given by Eq. (3-39) (for a lossless line):

$$Z(d)=Zc\frac{Z_L+jZ_C.tg(\beta d)}{Z_C+jZ_L.tg(\beta d)} \tag{3-39}$$

βl (l is the transmission line length) is called the electrical length of the transmission line. Some special cases have to be considered:

1. Shorted line: $Z_L=0$ then $Z_{input}=jZ_Ctg(\beta l)$

A short-circuited load will completely reflect an incident microwave beam (the reflection coefficient is $\Gamma_0=-1$). In terms of voltage and current, V = 0 at the load while the current (I) is a maximum there.

2. Open line: $Z_L=\infty$ then $Z_{input}=-jZ_C.cotg(\beta l)$

For an open load, the impedance is infinite ($Zl\rightarrow\infty$); consequently, the corresponding reflection coefficient at the load is $\Gamma_0=1$. In this case, the voltage is a maximum at the load and $I = 0$.

3. Matched line: $Z_L=Zc$ then $Zinput= Zc$

In this situation, the load at the end of the transmission line has an impedance equal to the characteristic impedance of the line ($\Gamma_L=0$). As a result of this impedance matching at the t-line load interface, the whole power of the propagating microwave is transmitted to the load.

4. Quarter-wave Line: $l=\lambda/4$ then $Z_{input}=Zc^2/Z_L$

For a transmission line with a shorted load ($Z_L=0$), a quarter-wavelength away from the short circuit, the input impedance reaches infinity.

Conversely, an open line ($Z_L=\infty$) observed $\lambda/4$ away from the load yields a null input impedance. A short circuit and an open line oscillate over every quarter-wavelength.

3.5 Transmission lines in integrated circuits

Two main kinds of transmission lines are generally used in integrated circuit design: microstrip line and stripline. Fig. 3-16 (EMCLAB) depicts these types of lines.

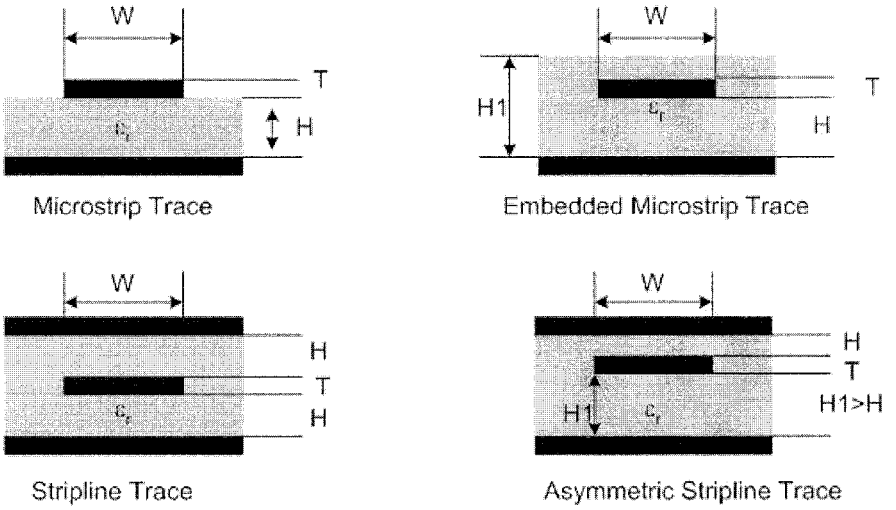

Figure 3-16. Microstrip and stripline lines (EMCLAB).

Microstrip lines are widely used in microwave integrated circuits (hybrid and monolithic). A microstrip line is made up of a W-wide and T-thick conducting metal strip located on a non-magnetic dielectric substrate that is itself located on a conducting metal ground plane. The substrate is H-thick and has a ε_r relative permittivity. A second dielectric material (air) is located above the line.

The main advantage of using a microstrip line is that it is well suited to PCB fabrication processes, and because the strip conductor is exposed on the top side, component mounting is relatively easy.

The expressions of the characteristic impedance of these lines are given in chapter 5.

3.6 The Smith Chart

First of all, Eq. (3-37) which gives the expression of the load reflection coefficient in terms of load impedance Z_L can be transformed by using the normalized impedance (z=Z/Zc) (Eq. 3-40):

$$\Gamma_L=\frac{z_L-1}{z_L+1} \text{ or } z_L=\frac{1+\Gamma_L}{1-\Gamma_L} \tag{3-40}$$

It can be easily demonstrated that the location of constant resistance and reactance points define circles in the complex Γ plane. A plot of these circles is called a **Smith chart**, and is displayed in Fig. 3-17.

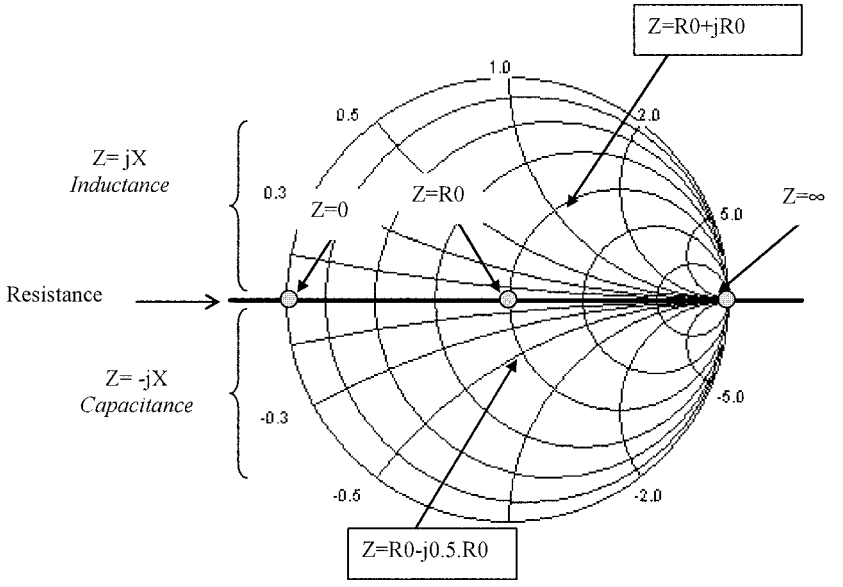

Figure 3-17. Smith Chart.

The Smith chart has some important features:

- It can be used for both impedances and admittances.
- It is defined for normalized impedances or admittances.
- Circles of constant reflection coefficient Γ are centered on the Smith chart.
- Moving clockwise around the Smith chart corresponds to moving away from the load, or towards the generator.

- The resistance at the intersection of a constant circle with the positive real axis is equal to the standing-wave ratio (SWR).

To sum-up, the real axis represent ohmic resistors, above the real axis, inductors are represented, whereas below the axis capacitors are represented.

4. RLC FORMULATIONS

4.1 Introduction

This section deals with the modeling of passive elements such as resistors, capacitors, inductors and interconnects, which are used in every electronic equipment.

Whereas old ASIC technologies allowed these basic elements to be modeled only with a single element, current technologies, involving higher frequencies, thus require more accurate modeling, and consequently, other elements have to be added to cover this broad frequency range. Resistors, capacitors and inductors are the three most commonly used passive elements in electronics, and they can be combined to design complex passive circuits. For example, they are used to model devices such as PCB tracks, package leadframes, bond wires, silicon connections and cables. In low frequency (under 100 MHz for example), the electrical behavior of these passive elements is well known and can be modeled by a single-element circuit:

- R: the resistance is constant with respect to the frequency,
- Z_L: the impedance, $jL\omega$, increases by +20 dB/decade.
- Z_C: the impedance, $1/jC\omega$, decreases by –20 dB/decade.

With more recent technologies, the clock frequencies of electronic devices increase and encompass wider frequency ranges. Therefore, the useful frequency bandwidth needed to propagate a signal is shifted into the VHF band (30-300 MHz), the UHF band (300 MHz-3 GHz) or even the SHF band (3 GHz-30 GHz). In these conditions, the wideband spectral content awakes the natural parasitic elements of these common passive devices and thus modifies their behavior. As a result, a single-element circuit can no longer describe the passive model and fails to predict correctly the behavior over a wide frequency range.

Fig. 3-18.a demonstrates how the signal bandwidth plays an important role in the definition of the model of these passive elements. A resistor is fed by a trapezoidal voltage generator, $e(t)$. Fig. 3-18.b describes the main electrical parameters in the time domain, and Fig. 3-18.c plots the spectrum envelope.

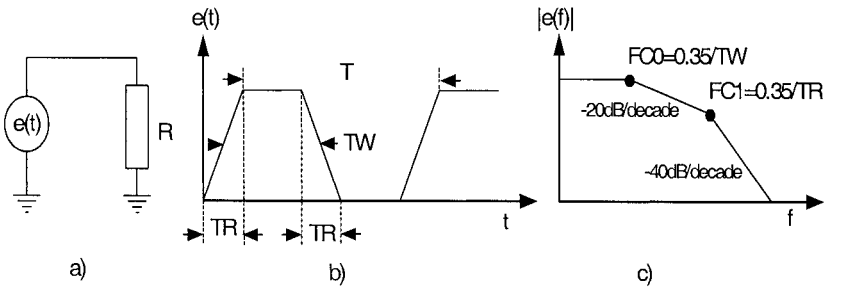

Figure 3-18. The faster the transition time, the larger the bandwidth.

The transition time T_R defines the bandwidth needed to propagate e(t) properly, and is equal to (Eq. 3-41):

$$F_{C1} = \frac{0.35}{TR} \tag{3-41}$$

In order to evaluate the frequency-domain impact on the model, e(t) is then given two different electrical characteristics, A and B, shown in Fig. 3-19. In Fig. 3-19, the spectral content of characteristic A is limited to 600 MHz. In that case, *R(f)* is only a resistance and therefore can be modeled by a single-element circuit. Conversely, when B is used, the structure of the model is frequency-dependent, and its spectral content rises up to 6 GHz. Fig. 3-19 demonstrates that *R(f)* is a pure resistor up to 100 MHz. From 100 MHz up to 1.8 GHz, the inductive part is dominant and *R(f)* has to be modeled as a double-element circuit (R and L). Finally, in the upper frequency range, *R(f)* acts as a transmission line, thus requiring a distributed-element model. Table 3-1 gives the frequency parameters for both *e(t)* configurations.

This introduction clearly shows that the accuracy of passive element models is related to the relevant frequency range. With current technologies, the spectral content of the signal has to be analyzed thoroughly, in order to define accurate models for resistors, inductors, capacitors and interconnections.

Table 3-1. The frequency parameters for each e(t) signal

e(t)	T_{Rn}	Fn=1/Tn	FC0n	FC1n
A	10 ns	10 MHz	7.5 MHz	35 MHz
B	1 ns	100 MHz	75 MHz	350 MHz

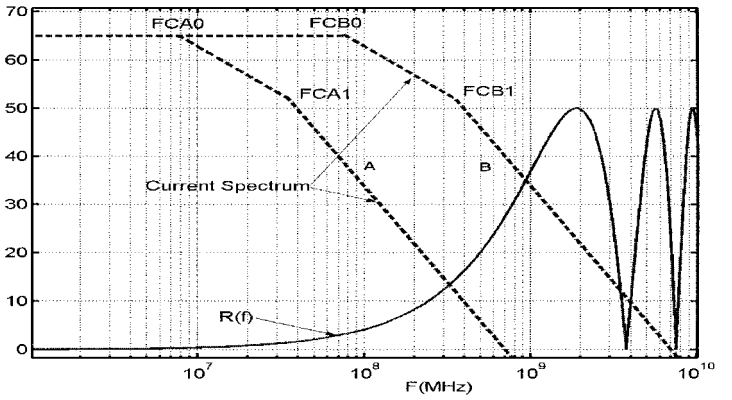

Figure 3-19. Resistor models depend on the frequency bandwidth.

4.2 Distributed and lumped models

Theoretically, every connection in an electrical circuit can be modeled by a transmission line. In past EMC studies, transmission-line models were simplified into lumped models because the relevant frequency range was far below microwave. This is no longer true nowadays because of the increase in the clock frequency and the decrease in transition times, which shift the relevant bands into microwave.

Equation (3-42) gives a general rule of thumb delimiting the minimum track length requiring transmission-line models. It takes into account the velocity in the dielectric and the transition time of the signal propagation into the passive element:

$$Lcrit = \frac{t_r . v_p}{10} \tag{3-42}$$

in which:

Lcrit is the critical length of the passive element, *vp* is the velocity in the dielectric, equal to $\frac{3.10^8}{\sqrt{\varepsilon_r}}$, ε_r is the dielectric constant.

If the transmission line length *L* is greater then *Lcrit*, the distributed model must be used.

4.3 Limitations of the lumped model

The lumped model is the most common model used to describe an interconnection or passive elements such as capacitors, resistors and inductors. This model is built from these three basic elements. The lumped model can be used in case the phase of the signal is constant along the passive element, otherwise the distributed model has to be used. The distributed model is a generic representation for all kinds of interconnections. The transmission line, as explained in section 3, is a possible instantiation of a distributed model.

It can be shown that the lumped model has a lot of limitations in high frequency compared with the distributed one. In order to state this, it is then possible to use an example with a 1-mm wide microstrip track on a 1.6-mm thick PCB. In such conditions, the characteristic impedance Z_0 is 72.5 Ω and the propagation delay T_{P0} is 0.71 ns for a 10-cm length. In order to compare both models, the lumped element model (L_0 and C_0) is determined thanks to the following process: First of all, L_0 and C_0 are expressed according to Eq. (3-43) and Eq. (3-44), which give L_0 = 51.2 nH and C_0 = 9.8 pF.

$$L_0 = Z_0^2 . C_0 \tag{3-43}$$

$$C_0 = \frac{TP_0^{\,2}}{L_0} \tag{3-44}$$

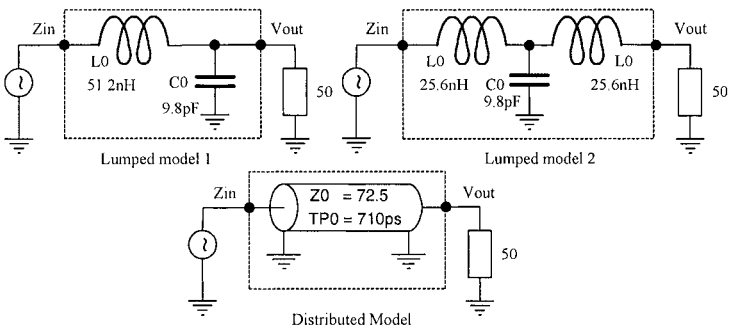

Figure 3-20. Models used for time- and frequency-domain analyses.

The DC resistance is very low (0.86 mΩ) and is not taken into account in this example. Fig. 3-20 shows three PCB track models. All the connections are loaded with a 50-Ω reference.

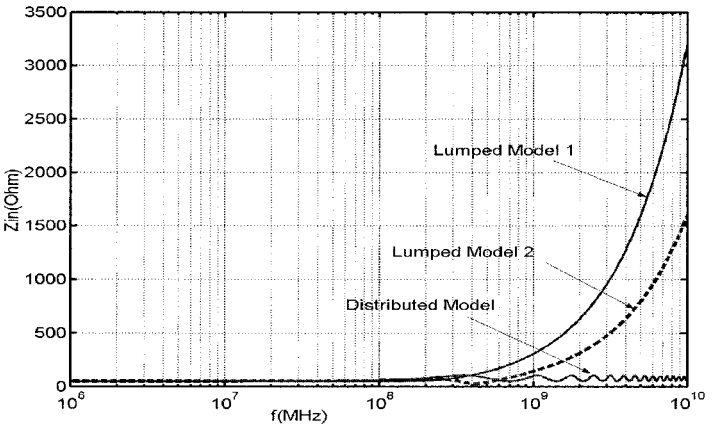

Figure 3-21. Impedance of the three models.

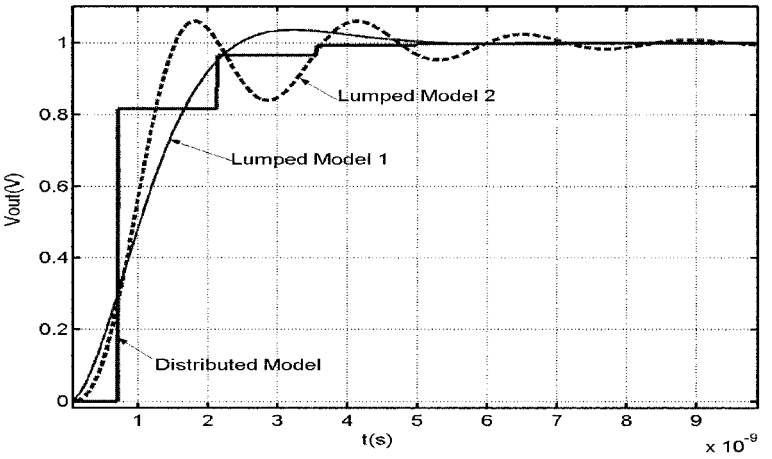

Figure 3-22. Response for the different models.

4.3.1 Frequency-domain analysis

Fig. 3-21 plots the impedance of the three models. Both kinds of models (lumped and distributed) are equivalent up to 300 MHz. Model 1 is thought inaccurate above this frequency.

Lumped model 2 remains usable below 1 GHz but becomes inaccurate in the upper frequency range. The distributed model must then be used if the operating frequency limit is above 1 GHz.

4.3.2 Time-domain analysis

These models can be compared in the time domain as well. A voltage step with a 100-ps rise time T_r is applied to Z_{in}. Fig. 3-22 plots the signal at the output of the PCB trace. Both lumped models are unable to reproduce the propagation delay correctly, even if lumped model 2 is slightly better. Furthermore, the overshoot observed with lumped models does not exist in real-world measurements. In the case of strong timing constraints in a design, the distributed model must then be used.

The choice of the kind of model to be used is closely related to the frequency bandwidth required by the signal flowing into the passive elements. Therefore, a proper definition of the spectral content enables the correct modeling level to be chosen, giving trustworthy results.

4.4 Skin effect

Skin and proximity effects are other frequency-dependent phenomena. With advances in technology, signal rise times decrease and the bandwidth of their spectral content increases. In such conditions, skin and proximity effects are not negligible and affect the accuracy of passive element models.

At high frequencies, the current in a real-world conductor does not flow uniformly throughout the cross-sectional area of the conductor. The magnetic fields induced by the current force the current to flow onto the surface of the conductor. The apparent resistance of the conductor thus increases with the square root of the frequency, due to current redistribution. In this case, all magnetic fields are concentrated in a cross-section with thickness δ and perimeter p, thus having a cross-sectional surface equal to $p\delta$.

The thickness of the apparent conductor is expressed by the following formula (Eq. 3-45):

$$\delta = \sqrt{\frac{1}{\pi \cdot f \cdot \mu \cdot \sigma}} \tag{3-45}$$

in which δ is the skin depth of the conductor, $\omega = 2\pi f$ is the operating frequency (rad/s), μ is the magnetic permeability of the material (H.m, 1.28 x 10^{-6} for a non-magnetic material) and σ is the bulk conductivity of the material. Table 3-2 gives the skin depth for two common materials and for different frequencies.

Table 3-2. Skin depth for different materials versus frequency

Material	1 kHz	1 MHz	10 MHz	100 MHz	1 GHz	10 GHz
Copper (mm)	2.1	0.066	0.21	0.0066	0.021	0.00066
Aluminium (mm)	2.7	0.085	0.27	0.0085	0.027	0.00085

Another physical phenomenon, called the proximity effect, contributes to the increase of the resistance with frequency. If a ground conductor is located close to the conductor carrying the signal, the magnetic field is not uniformly distributed onto the periphery of the conductor. Consequently, the proximity of the ground conductor, along with the skin effect, increases the apparent resistance of the conductor. The cross-sectional area through which the current flows in a conductor is also affected by the presence of other conductors.

Unfortunately, no closed-form equation is available to calculate the influence of the proximity effect. Therefore, 2-D quasi-static or 3-D field solvers have to be used in order to determine such an effect, which may increase the resistance roughly by 20 to 30 %.

In addition to that, because of the frequency dependency of the skin depth, the resistance and the inductance of a conductor vary with frequency as well. The main error in the prediction of the corresponding RLC circuit is then the quality factor and the bandwidth of the RLC circuit.

The general expression of the skin effect for a resistance is given with the following equation (Eq. 3-46):

$$R(f) = R_0(1 + j)\sqrt{\frac{f}{f_{oncet}}} \tag{3-46}$$

in which f_{onset} is the frequency at which the skin depth equals the thickness of the wire. R_0 is the resistance at the f_{onset} frequency.

The inductance of the conductor is frequency-dependent as well. In fact, a conductor has an internal and an external inductance. The internal inductance decreases down to zero as frequency increases, and is thus lower in high frequency. This expression shows that the skin effect affects the real part of the resistance and adds an imaginary part.

Integrated circuits are concerned with two kinds of geometries:

- Circular: bond wires

In an integrated circuit, a bond wire has a circular geometry. The DC resistance R_{DC} is determined using the following expression (Eq. 3-47).

$$R_{DC} = \frac{\rho \cdot L}{S} \tag{3-47}$$

- ρ: resistivity of the material
- L: length of the conductor
- S: cross-section of the conductor

The f_{onset} frequency is determined from the following expression (Eq. 3-48).

$$f_{oncet} = \frac{4.\rho^2}{\pi.\mu_0.R^2} \tag{3-48}$$

R: radius of the conductor. R_0 is determined when the skin depth is equal to the diameter of the bond wire.

- Microstrip or stripline: package.

The skin effect process in a rectangular conductor is linked to the current distribution in the cross-sectional area and to the geometry of the current path. This is why it is hard to find a universal analytical closed-form expression estimating the resistance and the inductance versus frequency, especially for rectangular cross sections.

2D or 3D field solvers have to be used to determine accurately these two parameters with respect to frequency. However, a good estimation can be done for the microstrip topology.

Fig. 3-23 and Fig. 3-24 plot the current density for a micro-strip topology and for three frequency bands. Fig. 3-23 shows the current distribution at 10 MHz while the skin depth (66 μm) is thicker than the thickness of the conductor (36 μm). At 10 MHz, the current is uniformly distributed in the cross-section area.

In Fig. 3-24, the skin depth is smaller than the thickness of the conductor and the skin depth regime begins to dominate.

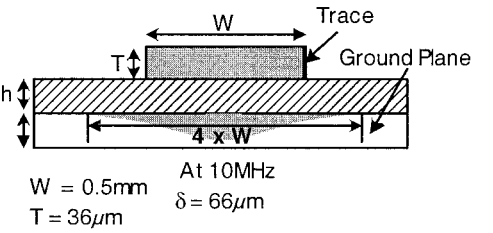

Figure 3-23. Current distribution in the 10-MHz band.

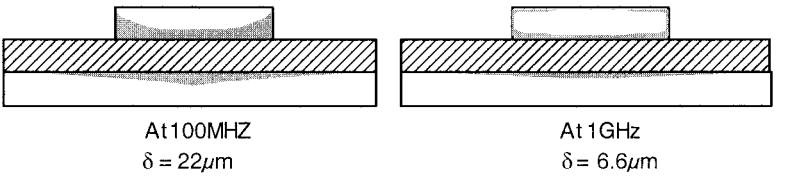

Figure 3-24. Current distribution in the 100 MHz to 1 GHz band.

At 100 MHz, the skin depth is 22 μm, the current density is concentrated on the periphery of the conductor and the proximity effect confines the current density close to the ground plane. At 1 GHz, the current is concentrated on the four sides of the conductor and there is no current distribution in the center. This configuration is applicable for IC packages and PCBs.

4.4.1 Resistances of the track and of the current return path

A closed-form expression of the resistance (Eq. 3-49) of a microstrip conductor is proposed by (Bogatin, 2001):

$$R_{F1}(f) = R_{DC} + R_{AC}(f) \tag{3-49}$$

in which:

R_{DC} is the DC resistance, only proportional to the geometrical cross section, and $R_{AC}(f)$ is the AC term proportional to the square root of the frequency.

The DC resistance of the track is expressed by Eq. (3-50), where ρ is the bulk conductivity of the material and W, T are defined in Fig. 3-23.

$$R_{DC}(f) = \frac{\rho}{W \cdot T} \tag{3-50}$$

The AC resistance of the track itself has the same expression as R_{DC} except for the thickness which is frequency-dependent (Eq. 3-51):

$$R_{AC}(f) = \frac{\rho}{W \cdot \delta(f)} = \sqrt{\rho.\mu 0 \cdot \pi \cdot f} \cdot \frac{L}{W} \tag{3-51}$$

The onset frequency, F_{C1}, namely the frequency at which the skin depth equals the thickness of the conductor or at which $R_{AC}(f)$ equals R_{DC}, can be determined with Eq. (3-52):

$$F_{C1} = \frac{\rho}{\mu 0 \cdot \pi \cdot T^2} \tag{3-52}$$

To obtain the complete expression of the resistance, it is necessary to combine both R_{DC} and $R_{AC}(f)$ expressions. Fig. 3-25 plots the $R_{F1}(f)$, R_{F2} and R_{AC}. A better approximation is proposed by (Johnson, 1993) (Eq. 3-53):

$$R_{F2}(f) = \sqrt{R_{DC}{}^2 + R_{AC}(f)^2} \tag{3-53}$$

Bogatin (2001) proposed to add the resistance of the ground plane to $R_{AC}(f)$, assuming a return path width equal to 4 times the width of the PCB track (Eq. 3-54):

$$R_{F3}(f) = \frac{\rho}{2 \cdot \delta \cdot W} + \frac{\rho}{4 \cdot \delta \cdot W} = 0.75 \cdot \frac{\rho}{\delta \cdot W} \tag{3-54}$$

This formula is actually the best approximation in high frequency, taking into account the currents flowing on both surfaces of the PCB track, and spreading out in the return path to a width equal to 4 times the width of the signal path.

4.4.2 Influence of the skin effect

At low frequencies, the skin depth has a very low influence on accuracy. Conversely, at 10 MHz, this effect becomes significant for parallel and series resonant circuits.

4.4.2.1 Series resonant circuit

The first example shown in Fig. 3-26 plots the input impedance *Z(f)* of a series resonant circuit, such as a capacitor, made up of a resistor connected to a LC circuit.

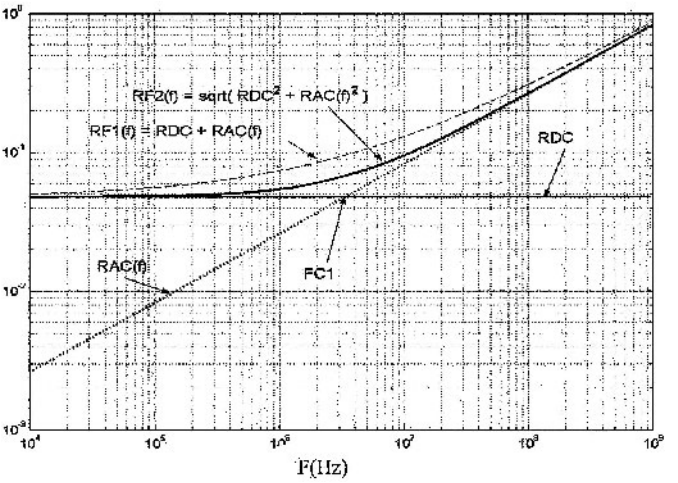

Figure 3-25. Comparison between $R_{I\text{-}1}(f)$ and $R_{I\text{-}2}(f)$.

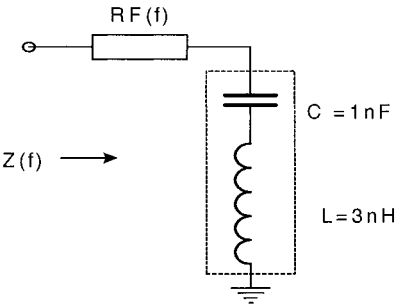

Figure 3-26. Series RLC circuit.

4.4.2.2 Parallel resonant circuit

Fig. 3-27 plots the impedance of the RLC circuit for different capacitor values and by taking into account $R_{AC}(f)$ or not. The effect of the skin depth on $Z(f)$ and at the series resonance can be clearly seen here. If a capacitor is used for decoupling, the ESR (equivalent series resistance) increases the impedance at the filtering frequency and decreases the performance (quality factor and bandwidth) of the decoupling. Fig. 3-28 shows a parallel resonant circuit. Fig. 3-29 plots the $Z(f)$ impedance taking into account or not the skin depth of the resistance.

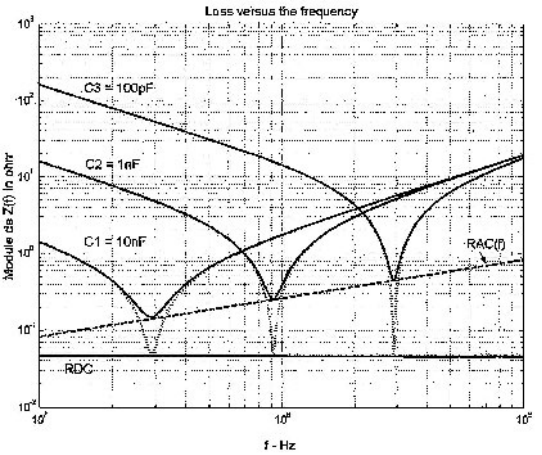

Figure 3-27. Losses versus frequency.

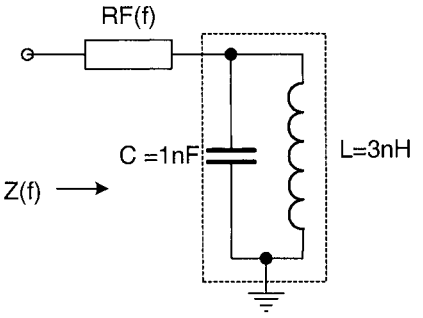

Figure 3-28. Parallel RLC circuit.

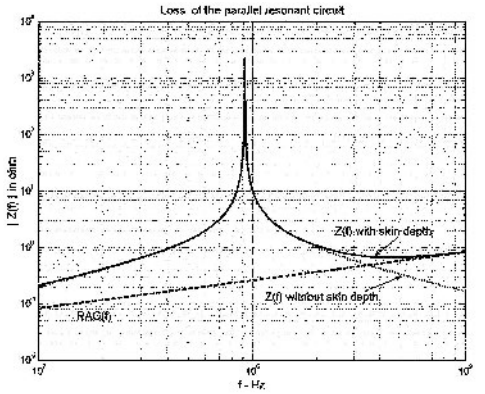

Figure 3-29. Losses in a parallel resonant circuit.

At the resonant frequency, there is no difference because the LC impedance is infinite and there is thus no current in *R(f)*. The difference occurs at 300 MHz, where the resistance increases with the square root of the frequency. The impedance above 300 MHz is higher than with a pure DC resistance and the attenuation above this frequency decreases.

4.4.3 Discussion

The skin and proximity effects affect impedances in high frequency and are thus relevant for the integrated circuit world above 10 MHz. The quality factor and the bandwidth of parallel and series resonant circuits are reduced by these effects. Some analytical expressions have been proposed but only for a round wire and a microstrip line. As far as other geometries are concerned, 2-D or a 3-D field solvers have to be used to estimate the skin and proximity effects.

4.5 Interconnect

The role of interconnects in integrated circuit performance has considerably increased with the technology scale down. RC delays, crosstalk between interconnects and inductance effects have dramatically changed the approach to interconnects problems. The main reason for this is the multiplication of metallization layers (10 layers are now used for the 90 nm CMOS technology), the tremendous shift of the signal spectrum towards ultra high frequencies and the increase in coupling areas which generate parasitic couplings which are both capacitive and inductive (Delorme, 96).

The electrical models of the metallization lines have moved from simple capacitance effects to the more realistic fringing capacitance, crosstalk capacitance, and parasitic resistance effects. The interconnect behavior, either for the transport power supply or active signals, can be simulated using line models built from a combination of capacitances, resistances and inductances. The following paragraph gives an overview of the formulas used to evaluate the on-chip interconnect impedance.

4.5.1 Capacitance associated with interconnects

Interconnect lines behaves like capacitors, as they are able to store charges in the metal/oxide interface. The capacitance effect is not simple to describe and to model. This is due to the fact that interconnects are routed very close to each other, as shown in Fig. 3-30. The capacitance effects are represented by a set of capacitors which link interconnects together electrically.

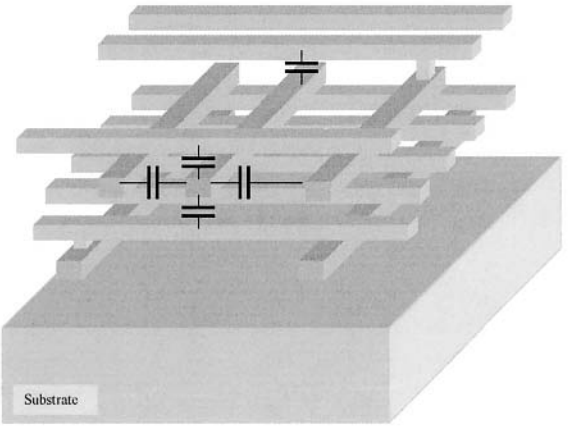

Figure 3-30. One interconnect is coupled to other conductors in several ways, both lateral and vertical.

4.5.1.1 Large plates

In the case of a large metal area (width w, length l) separated from the substrate or other metal areas by an oxide with a thickness e, Eq. (3-55) is quite accurate. The fringing capacitance Cf in that case is neglected. Large plates of metal are used in pads and supply lines (Fig. 3-31).

$$Cs = \varepsilon_0 \varepsilon_r \frac{w.l}{e} \tag{3-55}$$

where $\varepsilon_0 = 8.85 \times 10^{-12}$ Farad/m,
$\varepsilon_r = 3.9$ for SiO_2
w= conductor width (m)
l = conductor length (m) and
e = dielectric thickness (m)

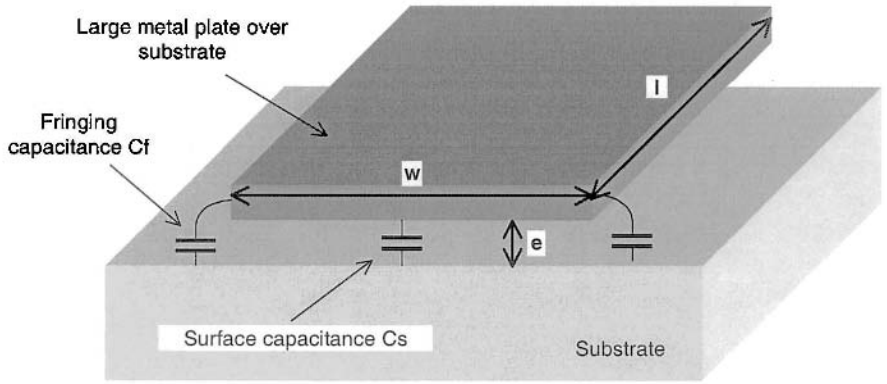

Figure 3-31. Large plate of metal above the substrate.

4.5.1.2 Conductor above a plane

Several formulations have been proposed (Sakurai, 1993; Delorme, 1996) to compute the capacitance of a conductor when the width is comparable to the oxide thickness (Fig. 3-32), which is the case with the large majority of conductors used to propagate signals. Eq. (3-56) gives the total capacitance which consists in the sum of Cs and twice the fringing capacitance *Cf*, from (Delorme, 1996).

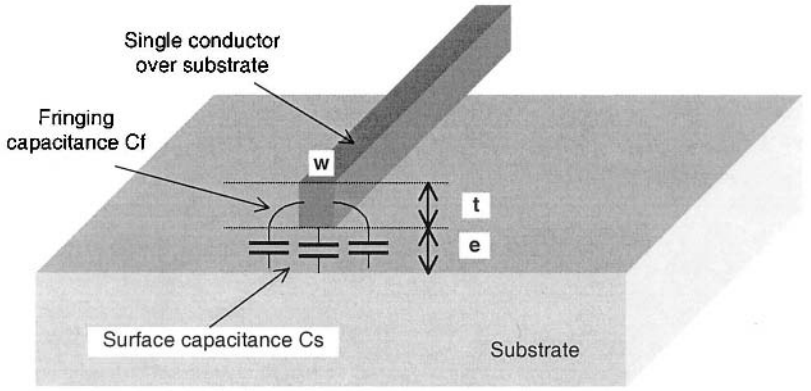

Figure 3-32. One conductor above a ground plane.

$$C=C_s+2.C_f=\varepsilon_0\varepsilon_r(1.13.\frac{w}{e}+1,44.(\frac{w}{e})_{0.11}+1.46.(\frac{t}{e})_{0.42}) \quad (3\text{-}56)$$

where:
C = total capacitance per meter (Farad/m)
Cs= surface capacitance (Farad/meter)
Cf= fringing capacitance (Farad/m)
$\varepsilon_0 = 8.85 \times 10^{-12}$ Farad/m
$\varepsilon_r = 3.9$ for SiO_2
w= conductor width (m)
t= conductor thickness (m)
e = dielectric thickness (m)

4.5.1.3 Two conductors above a ground plane

When a conductor is routed close to another conductor, a crosstalk capacitance, defined as C_{12} is created between the two conductors (Fig.3-33). In 0.12 μm technology, a specific dielectric with a low permittivity (this parameter, called *Low K*, is approximately 3 instead of 4) is used to fill the gaps between interconnects. This is an efficient technique to reduce the crosstalk capacitance while keeping the upper and lower capacitance almost unchanged.

Consequently, the oxide stack alternates between high K and low K materials, as shown in the cross-section. Low K dielectrics were introduced with 0.18 μm technology. Air gaps are the ultimate low K materials, with a lowest possible K=1.

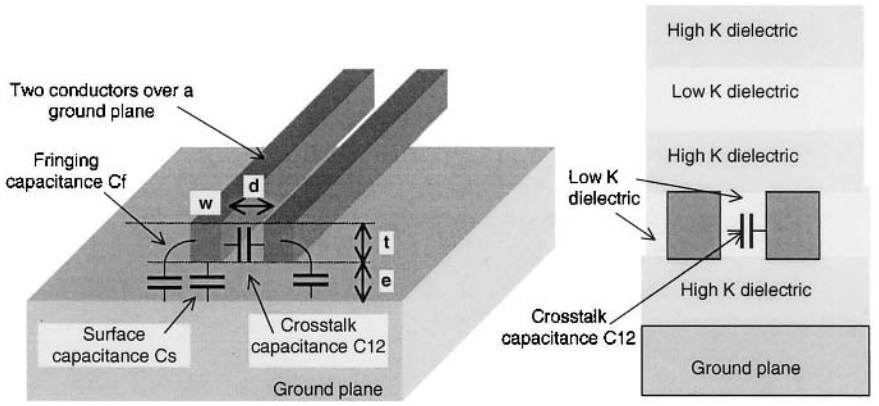

Figure 3-33. Two conductors above a ground plane.

The formulation of capacitances are given by Eq. (3-57) and Eq. (3.58).

$$C = C_s + C_f = \varepsilon_0 \varepsilon_r (1.10\frac{w}{e} + 0.79(\frac{w}{e})^{0.1} + 0.46.(\frac{t}{e})^{0.17}(1 - 0.87e^{(\frac{-d}{e})}))$$

(3-57)

$$C_{12} = \varepsilon_0 \varepsilon_{rlowK} (\frac{t}{d} + 1.2(\frac{d}{e})^{0.1}.(\frac{d}{e} + 1.15)^{-2.22} + 0.253\ln(1 + 7.17\frac{w}{d}).(\frac{d}{e} + 0.54)^{-0.64})$$

(3-58)

where
C = conductor capacitance to ground per meter (Farad/m)
Cs= surface capacitance (Farad/meter)
Cf= fringing capacitance (Farad/m)
C_{12} = crosstalk capacitance (Farad/m)
ε_{rlowK} = permittivity of low dielectric material (around 3.0 in 0.12 μm)
d = conductor distance (m)

4.5.2 Resistance associated with interconnects

The resistivity of interconnect materials used in CMOS integrated circuits is listed in Table 3-3. Conductors have very low resistivity, while semiconductor materials such as highly doped silicon have a moderate resistivity. Conversely, the intrinsic silicon resistivity is very high. If a conductor is l-long w-wide and t-thick, then its series resistance R (Fig. 3-34) can be computed using the formula (Eq. 3-59).

Table 3-3. Resistivity of several materials used in CMOS circuits

Symbol	Description	Used for	Resistivity at 25°C
ρ_{cu}	Copper resistivity	Signal transport	$1.72\ 10^{-6}$ Ω.cm
ρ_{al}	Aluminum resistivity	Signal transport	$2.77\ 10^{-6}$ Ω.cm
ρ_{Ag}	Gold resistivity	Bonding between chip and package	$2.20\ 10^{-6}$ Ω.cm
$\rho_{tungsten}$	Tungsten resistivity	Contacts	$5.30\ 10^{-6}$ Ω.cm
ρ_{Ndiff}	Highly doped silicon resistivity	N+ diffusions	0.25 Ω.cm
ρ_{Nwell}	Lightly doped silicon resistivity	N well	50 Ω.cm
ρ_{si}	Intrinsic silicon resistivity	Substrate	$2.5\ 10^{5}$ Ω.cm

$$R = \rho \frac{l}{w.t} \tag{3-59}$$

where:
- R= series resistance (Ω).
- ρ= resistivity (Ω.m).
- w= conductor width (m).
- t= conductor thickness (m).
- l = conductor length (m).
- d = conductor distance (m).

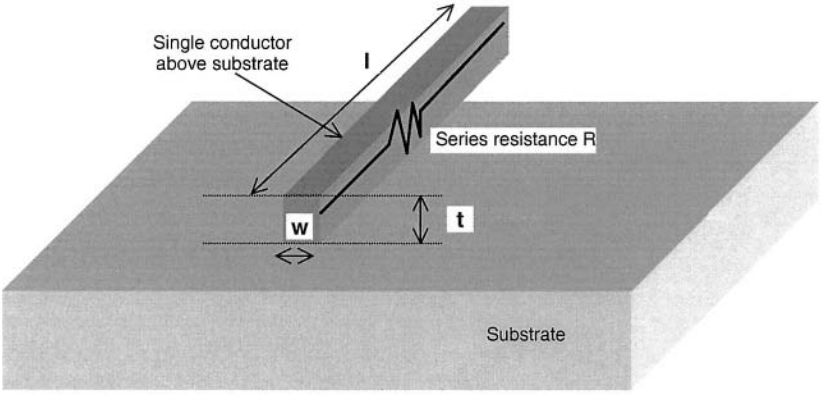

Figure 3-34. Resistance of a conductor.

When designing interconnects, a very useful metric is the "resistance per square". It is assumed that the width is equal to the length, that is (Eq. 3-60):

$$R_{square} = \rho \frac{w}{w.t} = \frac{\rho}{t} \tag{3-61}$$

The square resistance is used to estimate rapidly the equivalent resistance of an interconnect by splitting its layout into elementary squares. The total number of squares is then multiplied by R_{square} in order to evaluate the global interconnect resistance. This concept in illustrated in the layout shown in Fig. 3-35. A resistance per square R_{square} of 50 mΩ is assumed. The resistance from A to B can be approximated by 10 squares, that is a 0.5 Ω resistance.

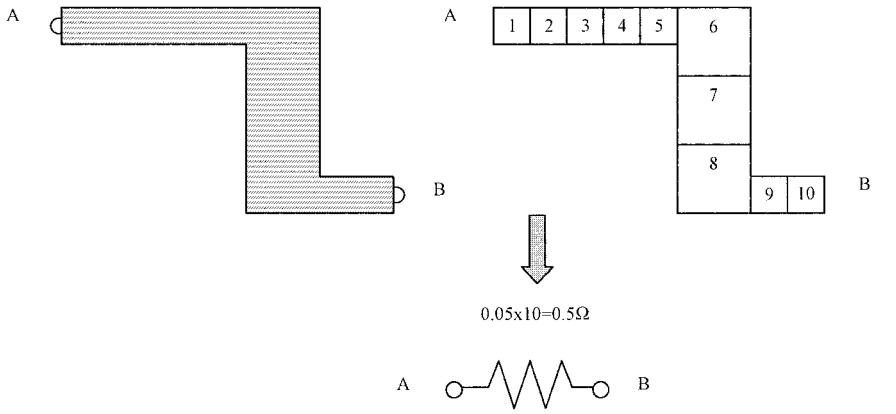

Figure 3-35. applying the concept of resistance per square to a portion of interconnect.

4.5.3 Resistance associated with interconnects

Signal propagation from one logic gate to another uses metal interconnects. Depending on the distance between the source gate and the target gate, interconnect may be considered as simple parasitic capacitances or a combination of capacitances and resistances. In 0.12 µm, interconnects with a length up to 1000 µm can be considered as purely capacitive loads *CL* (Fig. 3-36). For interconnects larger than 1000 µm, the series resistance *RL* should be included into the model. The usual way consists in splitting the capacitance *CL* into two equivalent capacitances and placing the series resistance in between.

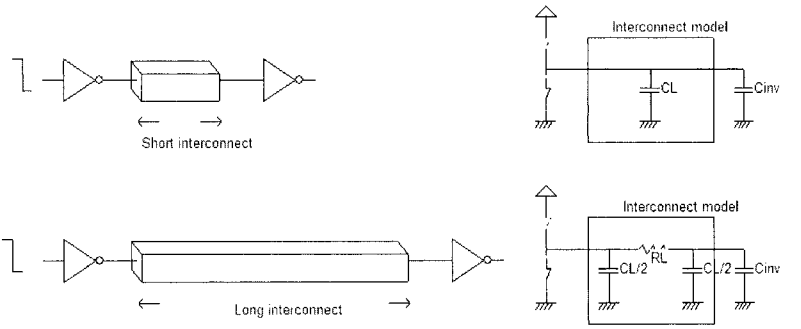

Figure 3-36. C versus RC model for interconnects.

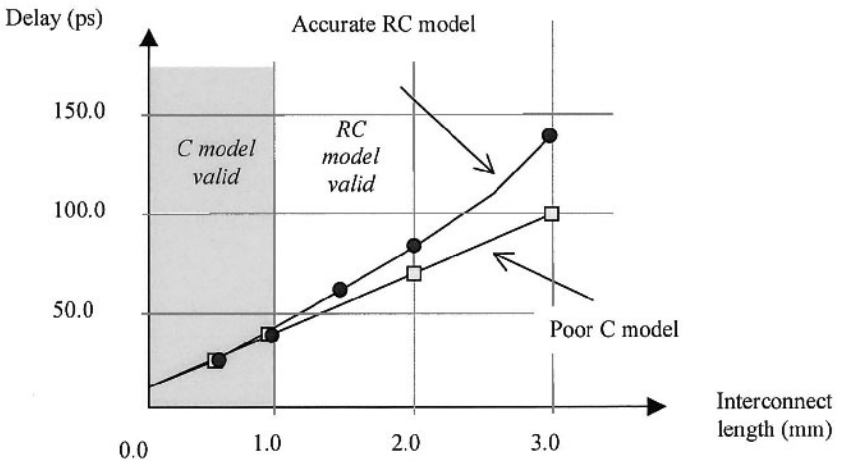

Figure 3-37. Below 1mm, the C model is valid. Above 1mm, the RC model should be considered in 0.12 µm CMOS technology.

The simulated propagation with C and RC models gives no visible difference below 1 mm. Above 1 mm, the C model gives an optimistic prediction of the delay compared to the RC model. The delay versus interconnect length is plotted in Fig. 3-37.

4.5.4 Inductance

Inductance effects are not significant for signal propagation because of the high series resistance of interconnects. Therefore, inductance values and possible consequences on delay estimation or crosstalk amplitude are scarcely taken into account. In the past few years, a lot of research has been dedicated to the extraction and handling of inductances. Brief evaluation and illustration of parasitic inductance effects in deep submicron interconnects is given here.

The formulation (Eq. 3-62) of wire inductance is based on the estimation of a cylinder for which a very simple formulation exists (Lee, 1998). A well known rule of thumb consists in approximating the series inductance to 1 nH/mm, which is accurate enough in the case of bonding wires. The wire has a cylindrical shape and is situated far from the ground plane, as shown in Fig. 3-38.

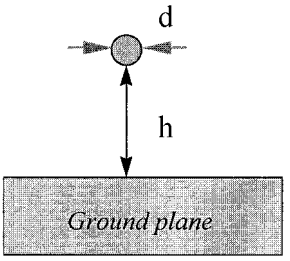

Figure 3-38. Parasitic series inductance of a wire above a ground plane.

$$L = \frac{\mu 0}{2\pi} ln(4\frac{h}{d}) \tag{3-62}$$

with

- μ_0=1.257 x 10^{-6} H/m for most materials (Al, Cu, Si, SiO_2 and Si_3N_4).
- d= wire diameter (m).
- h = distance from wire to ground (m).

In the case of metal interconnects, Eq. (3-62) is adapted with an approximation of the interconnect diameter, based on conductor width and thickness.

The electrical parameters for metal interconnects, such as resistance, capacitance, and inductance effects has been presented. These electrical parameters have to be considered when studying signal propagation and crosstalk effects inside the ICs.

5. S-PARAMETERS

In a microwave circuit, the incoming wave on a transmission line, for example, is "scattered" by the circuit and its energy is partitioned between all the possible outgoing waves on all the other transmission lines connected to the circuit. The scattering parameters are fixed properties of the (linear) circuit which describe how energy is coupled between each pair of ports or transmission lines connected to the circuit.

It is pointed out that the parameters of the scattering matrix or S matrix, which are briefly called S parameters, are used in the case of frequencies above 100 MHz.

In Fig. 3-39, an n-port microwave network is considered. It can have n arms (transmission lines or wave guides) which power can be fed into and taken out of.

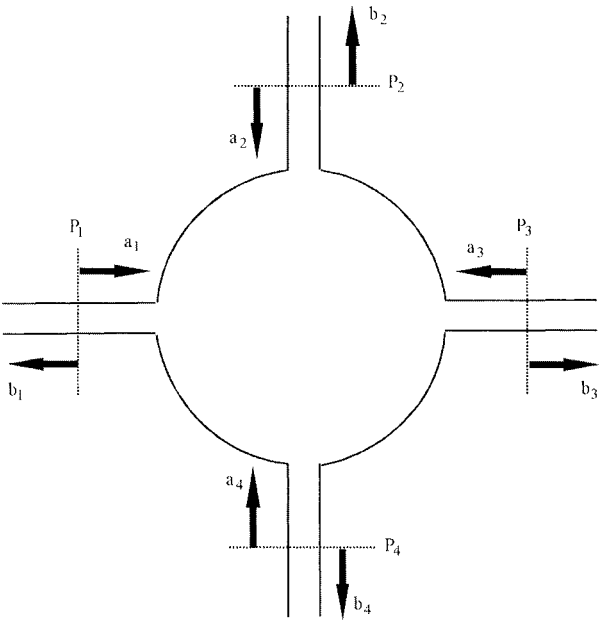

Figure 3-39. A 4-port network.

In general, power can travel from any given arm (as an input) to any other given arm (as an output). There are thus n incoming waves and n outgoing waves. It is also observed that power can be reflected by a port, so the input power to a single port can be partitioned between all the ports of the network to form outgoing waves.

Each port is characterized by its "reference plane" P on which the wave amplitude and phase are defined. Usually, the reference plane associated with a given port is at the same location with respect to incoming and outgoing waves.

The complex amplitudes of the n incoming waves are usually designated by "a", and the complex quantities of the n outgoing waves are designated by "b".

The n order of the network may take the 1, 2, 3, 4 or more values:

- For n=1, 1-port: dipole (open circuit, short circuit and load),
- For n=2, 2-port: quadripole (amplifier, transistor ...),
- For n=3, 3-port: hexapole (circulator, attenuator....),
- For n=4, 4-port: octupole (directive coupler,....),

S-parameters (scattering parameters) are the direct link between these ingoing and outgoing waves. In other words, S-parameters are the direct link between the power transfers between the input and the output of the network.

5.1 Interest of S-parameters

In order to demonstrate the usefulness of S parameters, especially in the microwave field, the case of a quadripole (Q) case (Fig. 3-40) can be examined:

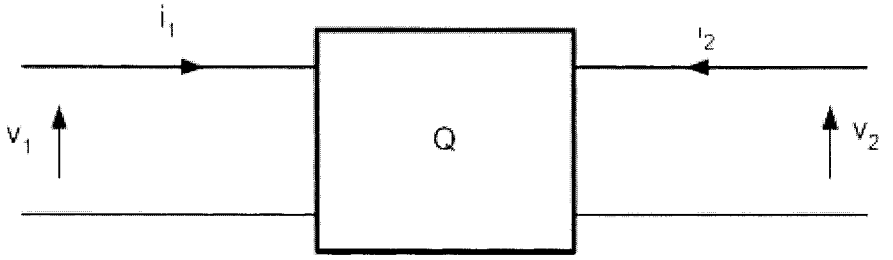

Figure 3-40. Quadripole.

In terms of current and voltages (namely transfer impedances), i_1, i_2, v_1 and v_2 are linked by the following relations (Eq. 3-63):

$(v)=(Z).(i)$ or

$$\begin{pmatrix} v_1 \\ v_2 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} \tag{3-63}$$

For example, Z_{11} can be expressed by Eq. (3-64):

$$Z_1 = \frac{v_1}{i_1}\Big)_{i2=0} \tag{3-64}$$

Obtaining Z_{11} requires that $i_2=0$, to wit an open circuit, but in the microwave domain (above 100 MHz), an open circuit (as well as a short circuit) is difficult to obtain with good accuracy.

Voltages are difficult to define for non-TEM waveguide modes. Even in TEM mode, voltages and currents are difficult to measure directly at microwave frequencies. The best example is the rate at which a digital sampling scope would have to operate to achieve this measurement.

To sum-up, it can be said that it is hard to measure total voltages and currents at device ports in high frequency, and that active devices may oscillate or self-destruct with short and open circuits.

5.2 Definition of S-parameters

As demonstrated in the transmission line section, a current and a voltage can be defined as a sum of an ingoing wave and an outgoing wave (Eq. 3-65).

$$V=Vi+Vr \text{ and } I=Ii+Ir \tag{3-65}$$

For example, Fig. 3-41 displays a generator *Eg* with its internal impedance Z_0, loaded by a Z_L impedance:

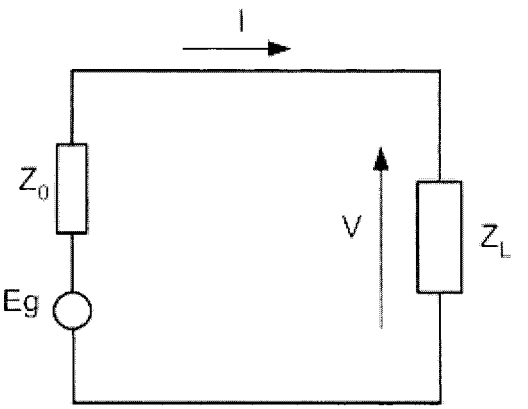

Figure 3-41. A loaded generator with its internal impedance.

If the internal impedance Z_0 is real ($Z_0=R_0$), the reflection coefficient (in terms of voltage and current) at Z_L can be defined as Eq. (3-66):

$$\rho_I=\rho_V=\frac{Z_L-R_0}{Z_L+R_0}=\frac{z_L-1}{z_L+1} \tag{3-66}$$

with $z_L=\frac{Z_L}{R_0}$ (normalized impedance).

If the ingoing wave "a" and the outgoing wave "b" are defined as Eq. (3-67):

$$a=\sqrt{R_0}\,I_i=\frac{Vi}{\sqrt{R_0}} \text{ and } \quad b=\sqrt{R_0}\,I_r=\frac{V_r}{\sqrt{R_0}} \tag{3-67}$$

Then,

$$a+b=\frac{V}{\sqrt{R_0}} \text{ and } a-b=\sqrt{R_0}I \tag{3-68}$$

The normalized voltage "v" and the normalized current "i" are given by:

$$v=\frac{V}{\sqrt{R_0}}=a+b \text{ and } i=\sqrt{R_0}I=a-b \tag{3-69}$$

These incoming and outgoing waves are homogenous to the square root of a power ($W^{1/2}$). These quantities can not be measured directly.

Going back to Fig. 3-40, the incoming waves "a" and the outgoing waves "b" of the network are linked together by Eq. (3-70) and Eq. (3-71):

$$\begin{pmatrix} a_1 \\ a_2 \\ a_3 \\ \\ a_n \end{pmatrix} = \begin{pmatrix} \sqrt{R_{01}} & 0 & 0 & 0 \\ 0 & \sqrt{R_{02}} & & \\ 0 & & & 0 \\ & & & \\ 0 & & 0 & \sqrt{R_{0n}} \end{pmatrix} \begin{pmatrix} I_{i1} \\ I_{i2} \\ \\ \\ I_{in} \end{pmatrix} \tag{3-70}$$

and

$$\begin{pmatrix} b_1 \\ b_2 \\ b_3 \\ \\ b_n \end{pmatrix} = \begin{pmatrix} \sqrt{R_{01}} & 0 & 0 & 0 \\ 0 & \sqrt{R_{02}} & & \\ 0 & & & 0 \\ & & & \\ 0 & & 0 & \sqrt{R_{0n}} \end{pmatrix} \begin{pmatrix} I_{r1} \\ I_{r2} \\ \\ \\ I_{rn} \end{pmatrix} \tag{3-71}$$

The scattering matrix is then defined by the following relation (Eq. 3-72).

$$(b)=(S)(a) \tag{3-72}$$

In the case of a 2-port network, the previous relation can be written as:

$$b_1=S_{11}a_1+S_{12}a_2, \quad b_2=S_{21}a_1+S_{22}a_2$$

In general, all the elements of this matrix, called "s parameters", are frequency-dependent.

5.3 Measurement of S_{11}, S_{12}, S_{21} and S_{22}

First of all, an input is applied to Port 1 and a termination is located at Port 2 with a matched load ($a_2 = 0$):

$S_{11}=\frac{b_1}{a_1})_{a_2=0}$, reflection coefficient at Port 1 (matched load at Port 2).

The same process makes it possible to measure S_{21}.

First of all, an input is applied to Port 2 and a termination is located at Port 1 with a matched load ($a_1 = 0$):

$S_{12}=\frac{b_1}{a_2})_{a_1=0}$, voltage transfer ratio from Port 2 to Port 1 (matched load at Port 1).

The same process makes it possible to measure S_{22}.

It can be noted that each element of the S matrix is generally complex, i.e. (Eq. 3-73):

$$S_{ij}=|S_{ij}|e^{j\varphi_{ij}} \tag{3-73}$$

The derivation of the S-parameters is considered along with their representation in a signal flow diagram. The magnitude and phase of the S-parameters are determined with the help of network analyzers or vector voltmeters.

A one-port scattering parameter S is merely the reflection coefficient gamma and, as seen previously, gamma can be related to the load impedance $z_L = Z_l/Zo$ by the formula gamma = $(z_L-1)/(z_L+1)$.

5.4 Characteristics of the S matrix

5.4.1 Lossless multipole

In the case of a lossless multipole (n order), the power driven by the incoming wave a is given by Eq. (3-74):

$$Pin=\sum_{i=1}^{n}\frac{1}{2}a_i a_i^*=\frac{1}{2}(a)^{t*}(a) \tag{3-74}$$

The outgoing power driven by b wave is then (Eq. 3-75). The active power consumed by the multipole is then the difference between the previous expressions (Eq. 3-76).

$$Pout=\sum_{i=1}^{n}\frac{1}{2}b_i b_i^*=\frac{1}{2}(b)^{t*}(b) \tag{3-75}$$

$$P_a=\frac{1}{2}\left[(a)^{t*}(a)-(b)^{t*}(b)\right] \tag{3-76}$$

Consequently, a loss-less multipole is characterized by Eq. (3-77):

$$(S)^{t*}=(S) \tag{3-77}$$

A matrix that meets this relationship is *unitary*. The superscript "t" denotes the matrix transpose operation and the asterisk corresponds to the conjugated amplitude.

5.4.2 Reciprocity

Reciprocity has to do with the symmetry of the S matrix. A reciprocal S matrix is symmetrical with respect to the leading diagonal. Many networks are reciprocal. In the case of a 2-port network, that means that $S_{21} = S_{12}$ and that exchanging input and output ports does not change transmission properties. A transmission line section is an example of a reciprocal 2-port. A dual directional coupler is an example of a reciprocal 4-port. In general, for a reciprocal n-port (Eq. 3-78). Amplifiers have to be (and are) non-reciprocal, otherwise they would be unstable. Ferrite devices are deliberately non-reciprocal; they are used to build isolators, phase shifters, circulators and power combiners.

$$S_{ij}=S_{ji} \tag{3-78}$$

5.4.3 Transformation of the S-parameters into Z impedance

S parameters are algebraically related to impedance parameters (Z parameters), also to admittance parameters (Y parameters) and to a notional characteristic impedance of transmission lines. Table 3-4 depicts the relationships between S-parameters and the normalized impedance z.

Table 3-4. S-parameters vs Impedance

s-parameters in terms of z-parameters	z-parameters in terms of s-parameters
$S11=\frac{(Z11-1)(Z22+1)-Z12Z21}{(Z11+1)(Z22+1)-Z12Z21}$	$Z11=\frac{(1+S11)(1-S22)+S12S21}{(1-S11)(1-S22)-S12S21}$
$S12=\frac{2Z12}{(Z11+1)(Z22+1)-Z12Z21}$	$Z12=\frac{2S12}{(1-S11)(1-S22)-S12S21}$
$S21=\frac{2Z21}{(Z11+1)(Z22+1)-Z12Z21}$	$Z21=\frac{2S21}{(1-S11)(1-S22)-S12S21}$
$S22=\frac{(Z11+1)(Z22-1)-Z12Z21}{(Z11+1)(Z22+1)-Z12Z21}$	$Z22=\frac{(1+S22)(1-S11)+S12S21}{(1-S11)(1-S22)-S12S21}$

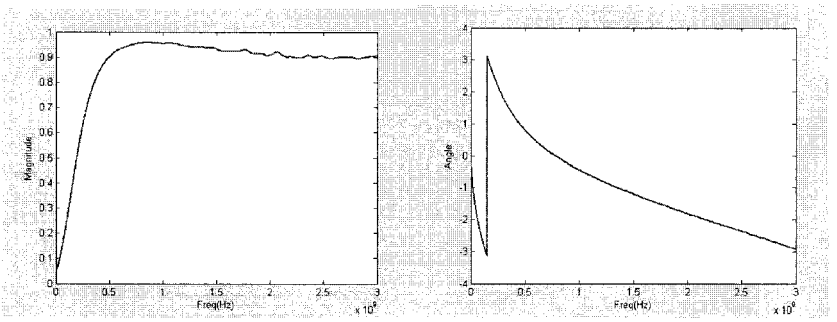

Figure 3-42. Measured S-parameters (magnitude and angle).

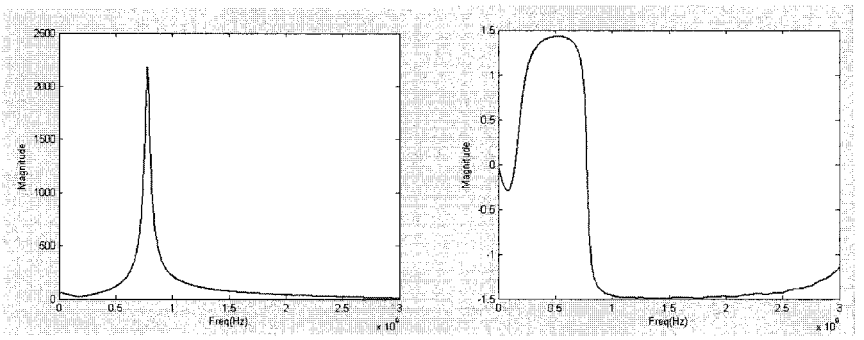

Figure 3-43. Impedance Z (magnitude and angle).

In case of a dipole, the only representing S-parameter *S11* is simply the reflection coefficient g given by Eq. (3-66).

The example illustrated below shows the way of extracting the impedance Z from the measured S-parameter (S=R+jX). According the Eq. (3.66), the real part Zreal and the imaginary part Zimag of the impedance Z are respectively given by Eq. (3-79) and Eq. (3-80).

$$Zreal=Z_0.[\frac{1-R^2-X^2}{(1-R)^2+X^2}] \tag{3-79}$$

$$Zimag=Z_0.[\frac{2X}{(1-R)^2+X^2}] \tag{3-80}$$

Fig. 3-42 depicts the measured S-parameters in terms of its magnitude and its angle. This measurement has been performed on a power supply network for an integrated circuit. Fig. 3-43 shows the corresponding Z.

5.5 Measurement of S-parameters

A vector network analyzer, or VNA, is an instrument which measures the complex transmission and reflection characteristics of two-port devices in the frequency domain.

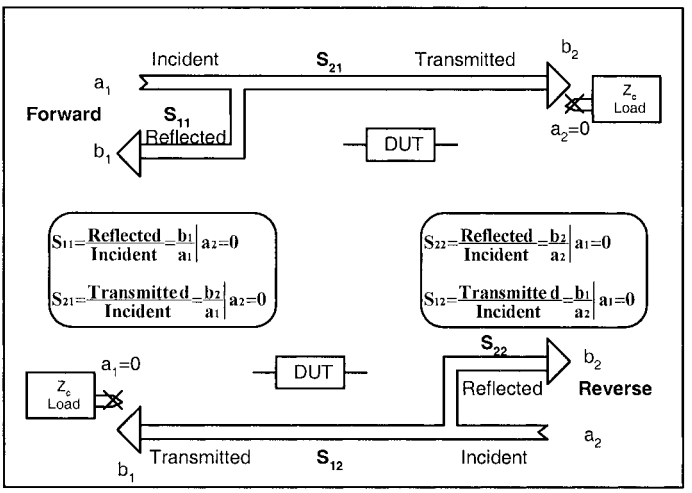

Figure 3-44. Measuring S-parameters.

It does this by sampling the incident signal, separating the transmitted and reflected waves, and then performing ratios that are directly related to the reflection and transmission coefficients of the two-port. Frequency is swept to rapidly obtain amplitude and phase information over a band of frequencies of interest.

The S-parameter representation is the most common format used to represent VNA measurements. The S-parameters S_{11} and S_{21} can be interpreted as the input reflection coefficient and forward transfer coefficient (gain or loss) under the conditions that the source and load impedances represent perfect *Zo* (e.g. 50 Ω) conditions.

Likewise S_{22} and S_{12} can be interpreted as the output reflection coefficient and reverse transfer coefficient (gain or loss) under the conditions that the source and load impedances represent perfect *Zo* (e.g. 50 Ω) conditions (Fig. 3-44).

6. CONCLUSION

The readers should find in this chapter the answers to their needs for EMC fundamentals and theory, particularly mathematical tools and ground concepts such as transmission lines, electromagnetic emission (electric and magnetic dipole), RLC modelling in high frequency, interconnect and S-parameters.

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Chapter 4

MEASUREMENT METHODS

Emission and susceptibility of integrated circuits

Abstract: This chapter deals with measurement methods for characterizing the parasitic emission and immunity of integrated circuits. We detail most of the standard methods promoted by IEC 61967 for emission, namely the TEM/GTEM, the near-field scan, the Workbench Faraday Cage and the 1/150Ω conducted methods. Concerning susceptibility, we detail the Bulk Current Injection and Direct Power Injection methods from the IEC standard 62132. Furthermore, impulse immunity methods are also described, as well as on-chip measurement approaches for noise characterization.

Key words: RF emission; RF immunity; Impulse immunity; DPI; BCI; WBFC; TEM; GTEM; anechoic chamber; mode stirred chamber; near-field scan; probes; international standards; digital circuits; mixed signal; fast pulses; ESD; EFT; IEC 61967; IEC 62132; IEC 62215; Jitter

1. INTRODUCTION

Electromagnetic compatibility test setups at electronic system levels are defined in standards such as CISPR 25 (CISPR, 2002) for parasitic emission and ISO-11452 for susceptibility to electromagnetic interference. In many cases, integrated circuits are the cause of disturbances in electronic equipment. In recent years, there has been a strong demand for simple, reliable and standardized measurement methods focusing only on integrated circuits, that electronic system designers could use to:

- Select components based on their low emission performance and high immunity to electromagnetic interference.
- Define optimum filtering and decoupling components to be added to printed circuit boards.
- Optimize integrated circuit placement and routing, to fulfill EMC specifications at board level.
- Evaluate the impact of integrated circuit redesign, technology shrink or package modification.

The International Electro-technical Commission, sub-committee 47A, working group 9 (Measurement methods for integrated circuits) has released two main standards, one for radio –frequency (RF) radiated and conducted emissions under project number IEC 61967 (IEC, 2001), and more recently a second one for RF immunity under project number IEC 62132 (IEC, 2003). The emission standard IEC 61967 has 6 parts:

- Part 1: General and definitions.
- Part 2: TEM-cell and wideband TEM-cell (radiated emission method).
- Part 3: Magnetic loop (radiated emission surface scan method).
- Part 4: 1 Ω/150 Ω (differential conducted emission).
- Part 5: Workbench Faraday Cage (common mode conducted emission).
- Part 6: Magnetic probe (radiated emission in magnetic probe).

The roadmap for standardization of the measurement methods related to electromagnetic emission is shown in Table 4-1. It can be seen that four parts are completed, while the TEM/GTEM is at the Committee Draft for Voting (CDV) stage. The surface scan method should remain in at the technical report stage. In 2004, a new part has been introduced, related to the mode-stirred chamber.

Table 4-1. IEC 61967 - Measurement of Electromagnetic Emission up to 1GHz

Standard	Description	2000	2001	2002	2003	2004	2005
IEC 61967-1	Definitions		Completed				
IEC 61967-2	TEM/GTEM Cell	Committee draft			CDV		Completed
IEC 61967-3	Surface Scan				Technical report	New prop. >1GHz	
IEC 61967-4	1/150Ω conducted	Final draft for voting		Completed			
IEC 61967-5	WBFC		Final draft for voting		Completed		
IEC 61967-6	Magnetic probe	Final draft for voting		Completed			
IEC 61967-7	Mode stirred ch.					New prop.	

The immunity standard IEC 62132 (IEC, 2003) has 5 parts:

- Part 1: General and definition.
- Part 2: TEM-cell and wideband TEM-cell (radiated immunity method).
- Part 3: BCI, bulk current injection method (conducted immunity).
- Part 4: DPI, direct RF injection method (conducted immunity).
- Part 5: Workbench Faraday Cage (common mode conducted immunity method).

Some similarities with the previous standard may be noticed in the structure of the document. Also, the TEM cell method and the WBFC method have been proposed for both emission and susceptibility characterization. The roadmap for standardization of susceptibility measurement methods (Table 4-2) is clearly shifted in time as compared to the emission roadmap. The most mature measurement method appears to be the WBFC approach, currently at the Committee Draft for Voting stage.

Table 4-2. IEC 62132 - Measurement of Electromagnetic Immunity up to 1GHz

Standard	Description	2000	2001	2002	2003	2004	2005
IEC 62132-1	Definitions	Committee Draft					
IEC 62132-2	TEM/GTEM Cell				New proposal		Committee Draft
IEC 62132-3	Bulk current injection		Committee Draft				
IEC 62132-4	Direct power Injection		Committee Draft				
IEC 62132-5	WBFC		Committee Draft			CDV	
IEC 62132-6	Mode Stirred ch.					New proposal	

Recently, discussions have started on the establishment of a new standard proposal (IEC 62215) for the measurement of transient immunity to impulses, electrostatic discharge (ESD), Electrical Fast Transients (EFT) and electrical overstress (EOS).

This chapter describes the following set of measurement techniques: the TEM/GTEM method, the near-field scan, the Workbench Faraday Cage, the 1/150 Ω method, the bulk current injection, direct power injection and transient immunity methods, the anechoic chamber and on-chip measurement. Finally, recommendations regarding EMC test plans are provided, as well as some prospective and a conclusion.

2. TEM/GTEM METHOD

The Transverse Electromagnetic Mode (TEM) cell and its high-frequency variant – the Gigahertz TEM (GTEM) cell – are commonly used for measuring electromagnetic emissions radiated by an IC as well as for measuring IC immunity to electromagnetic fields. This measurement method is standardized as IEC 61967-2.

2.1 Description

The TEM cell (Fig. 4-1) is an expanded rectangular waveguide with an inner conductor called the septum, whose characteristic impedance is set to 50 Ω and which is terminated by two tapered ends to connect 50 Ω-adapted coaxial cables.

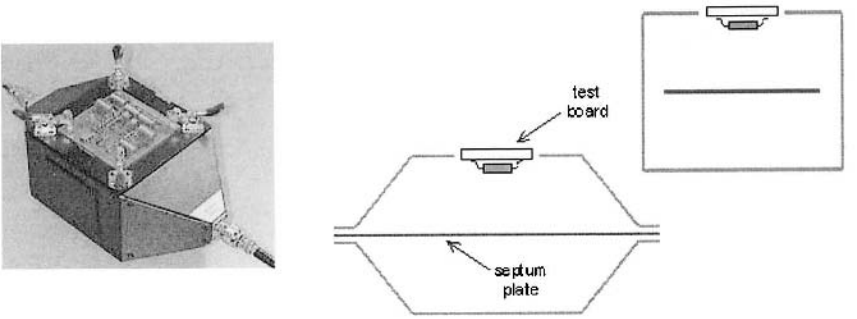

Figure 4-1. Picture and cross-sections of the TEM cell.

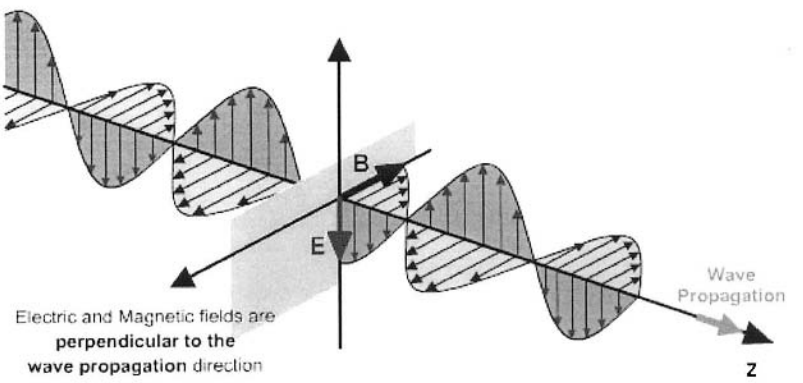

Figure 4-2. Picture of the TEM mode propagating in free space.

Due to the shape of its cross section, a Transverse Electro-Magnetic (TEM) wave can propagate in the cell. The TEM mode (Fig. 4-2) is characterized by electric (E) and magnetic (H) fields that are in a plane perpendicular to the wave propagation direction. In this plane, electric and magnetic fields are also perpendicular to each other (Fig. 4-3).

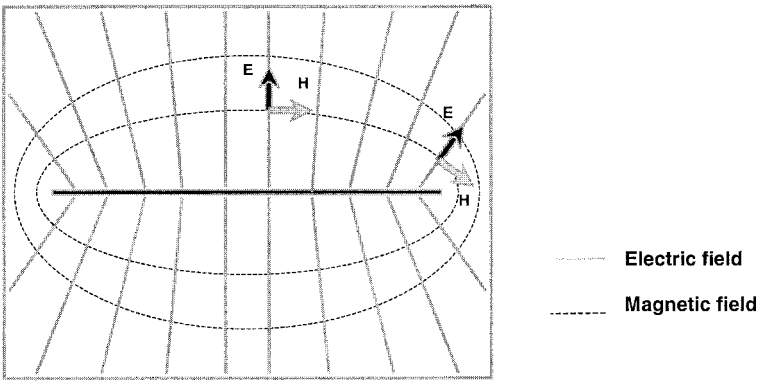

Figure 4-3. E-field and H-field distribution (TEM mode) in a cross-section of the TEM cell.

At low frequency, only the TEM mode can propagate in the cell. But as the frequency of the electromagnetic wave increases, higher order modes (TE for Transverse Electric modes and TM for Transverse Magnetic modes) become propagative in the central section of the cell, and spurious resonance phenomena appear in the cavity. The maximum frequency for the use of the TEM cell is set by the first resonance of the lowest higher order mode, which depends on the size and shape of the cell. Typical cell dimensions are given in Fig. 4-4, which corresponds to a 1-GHz cut-off frequency.

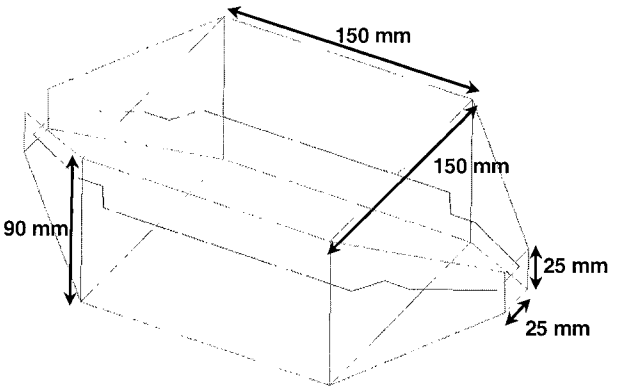

Figure 4-4. Typical dimensions of a 1-GHz TEM cell.

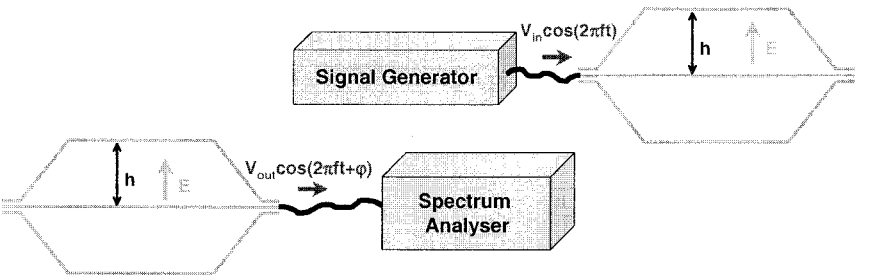

Figure 4-5. Experimental setup for generating or measuring a TEM wave with a known magnitude in the TEM cell.

From DC to the cell maximum frequency, the TEM mode has constant magnitude response as a function of frequency. Hence a known field can be generated in the TEM cell (Fig. 4-5), the strength of the electric field being given by Eq. (4-1) as follows:

$$E = \frac{V_{in}}{h} = \frac{\sqrt{Z_C P_{in}}}{h} \tag{4-1}$$

where h is the height between the septum and the TEM cell outer wall, V_{in} is the magnitude of the voltage applied at the TEM cell input, P_{in} is the input power into the TEM cell, and Z_C is the characteristic impedance of the TEM cell (usually $Z_C = 50\ \Omega$).

Examples of electrical field calculations for varying power and height are provided in Appendix A. On the other hand, the field intensity inside the TEM cell can be deduced from the voltage or the power measured at the cell output, following Eq. (4-2).

$$E = \frac{V_{out}}{h} = \frac{\sqrt{Z_C P_{out}}}{h} \tag{4-2}$$

where V_{out} is the magnitude of the voltage measured at the TEM cell measurement output and P_{out} is the power measured at the TEM cell measurement output.

2.2 IC emission measurement setup in the TEM cell

The aim of the TEM cell measurement standard is to quantify the global radiation from a component, at a short distance. To that purpose, the IC under test is mounted on a 10-cm square Printed Circuit Board (PCB) with four metal layers (Fig. 4-6). The chip under test is fixed alone over a ground layer on one side of the PCB, whereas power supply and other signals necessary to activate the IC are routed on the three other layers.

The test board is inserted in an aperture in the outer wall of the TEM cell with the chip inside the cell, so that the ground layer becomes a part of the wall, closes the ground shielding and isolates the integrated circuit from the outside world. One of the ports of the TEM cell is connected to a spectrum analyzer through an optional low-noise amplifier, while the other port is terminated with a 50 Ω load (Fig. 4-7). A more detailed description of TEM/GTEM compatible board requirements is available in IEC 61967-2 standard.

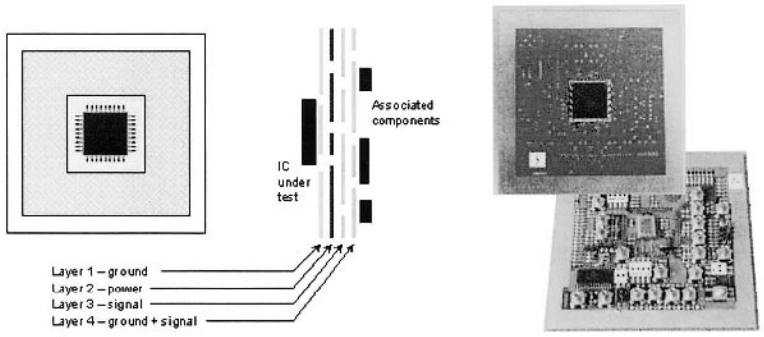

Figure 4-6. Description of the TEM-cell compatible PCB.

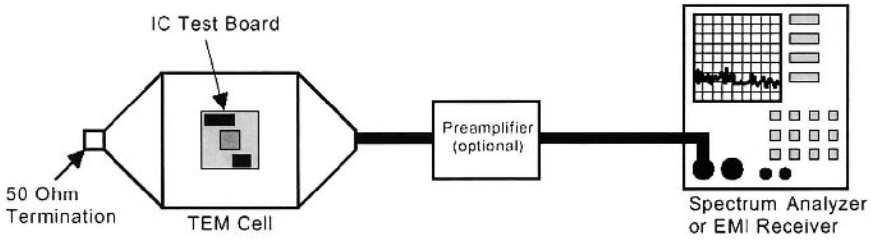

Figure 4-7. TEM cell measurement setup.

As the IC is activated, its radiation excites the TEM mode that propagates toward the cell measurement output. The RF voltage measured – in $dB\mu V$ – at the cell extremity is proportional to the electromagnetic emission spectrum of the component.

The coupling mechanism between IC radiation and the TEM mode has been investigated by Muccioli (1996). In the IC, pulsed currents flow through package pins, lead frames and bonding interconnections that behave like electric and magnetic dipoles. As the IC is inserted in the TEM cell, some of these radiating elements are coupled with the TEM mode while others are not. In the example given in Fig. 4-8, IC current path is equivalent to the combination of a vertical loop and a horizontal loop. In the case of orientation A, the horizontal loop radiates a vertically polarized magnetic field that is orthogonal to the magnetic field distribution of the TEM mode in the cell (see Fig. 4-3). Hence, this radiation does not couple with the TEM mode. The magnetic field radiated by the vertical loop is collinear to the magnetic field distribution in the cell, so the TEM mode is excited by the radiation of this loop. As the IC is positioned in orientation B, neither the horizontal nor the vertical loop is coupled with the TEM mode. Therefore two emission measurements are usually performed to characterize accurately the radiations from an IC: the first measurement is done with the test board mounted in an arbitrary orientation in the cell outer wall, then the second measurement is performed with the test board rotated 90 degrees from the orientation of the first measurement. However, the measurement standard stipulates that the four orientations should be investigated, and that only the spectrum with maximum amplitude should be considered.

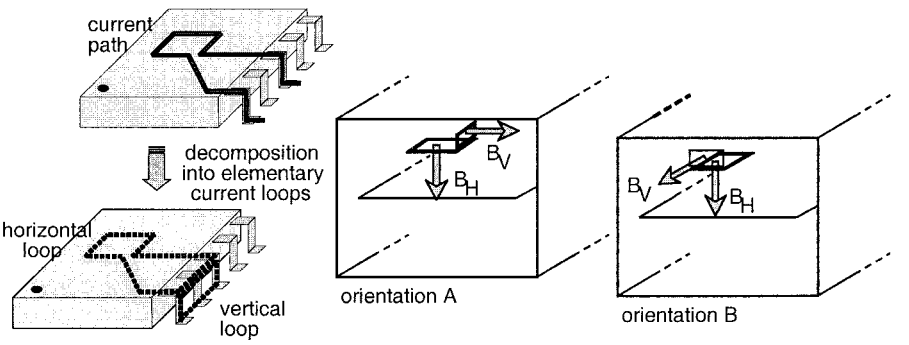

Figure 4-8. Coupling mechanism between IC current paths and the TEM mode propagating in the TEM cell.

2.3 TEM cell measurement of the radiations from a microprocessor

The following section presents typical measurement results of the emissions from an IC. The component under test was a 16-bit microcontroller mounted on a TEM/GTEM compatible test board. The cell used for measurements was a Fischer TEM cell, with a cut-off frequency of 1 GHz, and with a septum-to-aperture spacing of 45 mm. Its output port was connected to an Advantest R3131 spectrum analyzer (9 kHz – 3 GHz) through a 30 dB amplifier (DC to 2 GHz). The resolution bandwidth (RBW) and video bandwidth (VBW) parameters were set to 10 kHz over the whole frequency range. The "max hold" function of the spectrum analyzer was enabled.

Two programs (*OUTCLK* and *OUTCAPA* as detailed in Table 4-3) were loaded in the EEPROM memory of the component.

Table 4-3. Brief description of the programs loaded into the microcontroller

Program	Description
OUTCLK	PPL active
	Clock frequency set to 50 MHz
	Clock signal flowing out of the component through an I/O pin
	Other ports inactive
OUTCAPA	PPL active
	Frequency set to 50 MHz
	Clock signal flowing out of the component through an I/O pin.
	8-pin port terminated by capacitive loads
	Port A set as output
	Port A switching between values of 0x55 (01010101) and 0xAA (10101010)

TEM cell measurements were carried out in the frequency range 1 MHz – 1 GHz, for each program running into the microcontroller, and for two orientations of the test board, with a 90° rotation between the two orientations. The radiation spectra measured for the two programs (*OUTCLK* and *OUTCAPA*) with the same orientation of the microcontroller are compared in Fig. 4-9.

These results point out the importance of the program running into the component. Before performing TEM cell measurements, special attention has to be given to the choice of the operation test mode.

Fig. 4-10 shows the radiation spectra related to the *OUTCLK* program, for two perpendicular orientations of the microcontroller. These results clearly underline the orientation dependence; that is why two measurements with perpendicular orientations of the test board are required.

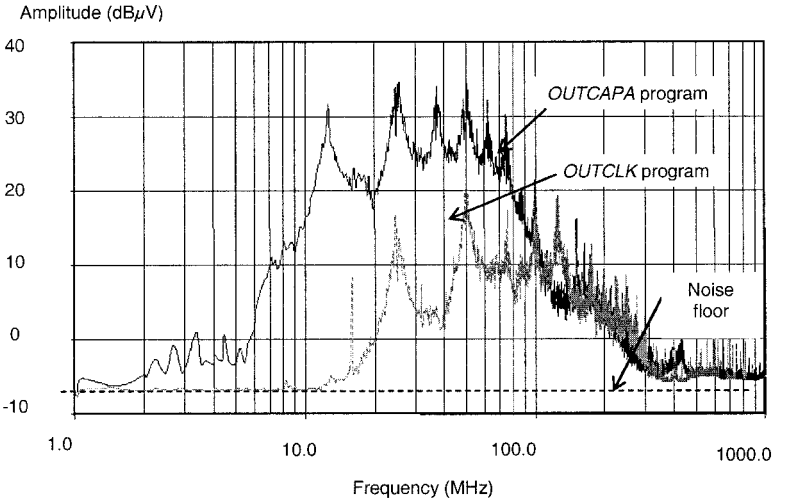

Figure 4-9. TEM cell measurement of the radiation from the microcontroller: same orientation, different programs.

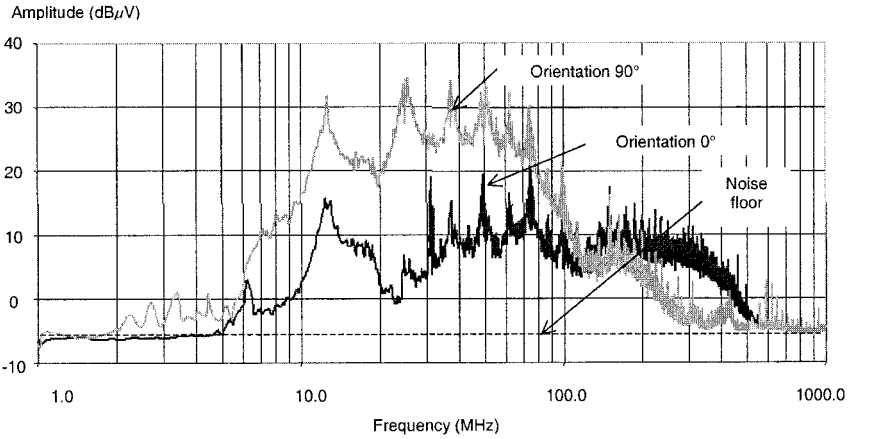

Figure 4-10. TEM cell measurement of the radiation from a component: same program, different orientations.

2.4 The GTEM: a high-frequency variant of the TEM cell

The GTEM cell (Fig. 4-11) was designed to overcome the TEM cell frequency limitation. It consists of a tapered section of rectangular transmission line, with an offset and sloping septum plate. The septum is tapered so that the characteristic impedance is maintained to 50 Ω along the length of the cell. The wide extremity is terminated by a distributed resistive load that operates as a 50 Ω load circuit at low frequency, and by pyramidal foam absorbers that attenuate the electromagnetic wave at high frequency. The narrow extremity is terminated by a 50 Ω -adapted coaxial connector.

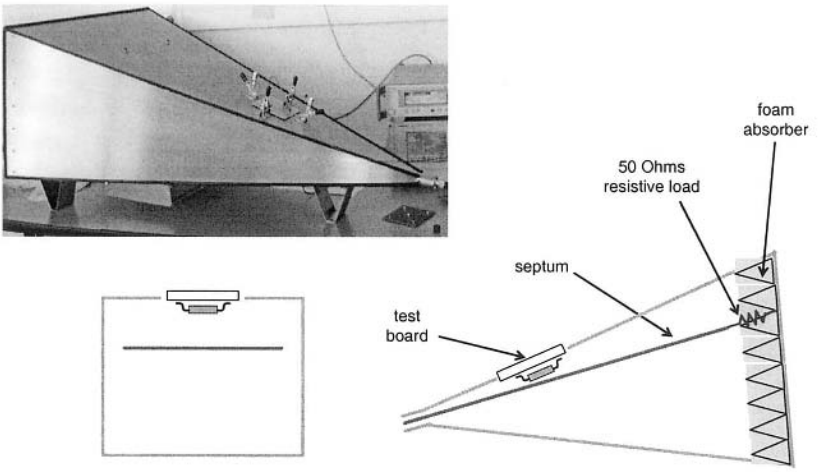

Figure 4-11. Picture and cross-section of the GTEM cell

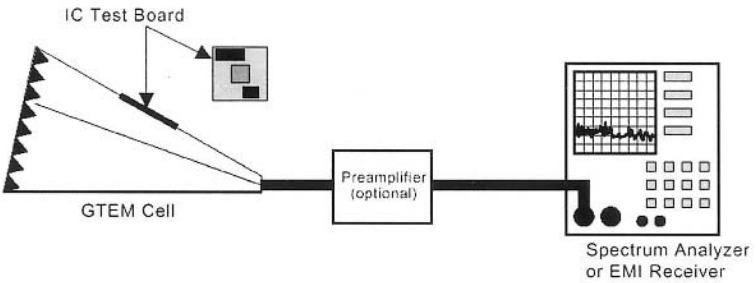

Figure 4-12. GTEM cell measurement setup.

The protocol for IC emission measurement in the GTEM cell (Fig. 4-12) is the same as for the TEM cell. But thanks to its matched termination and its tapered structure, the GTEM cell allows measurements up to frequencies of several GHz – typically 18 GHz.

As the test board is inserted into the cell outer wall, IC emissions locally excite several modes, not only the fundamental TEM, but also TE and TM modes (De Leo, 1991). These modes propagate toward the narrow extremity of the GTEM cell. As the dimension of the cross-section decreases, higher order modes cut off and transfer the power they carried to the fundamental mode. At the cell output, the TEM mode carries almost all the power radiated from the IC.

2.5 Correlating the results of measurements from different cells

Measuring the radiation from the same IC in TEM and GTEM cells should lead to identical results since the IC-to-septum spacing is similar. The correlation factor between two cells can be expressed as:

$$\delta = \frac{V_{out,2}(f)}{V_{out,1}(f)} = \frac{h_1}{h_2} \tag{4-3}$$

where $V_{out,1}(f)$ (respectively $V_{out,2}(f)$) is the voltage spectrum measured at the output of the cell C_1 (respectively C_2) and h_1 (respectively h_2) is the height between the septum and the aperture in the outer wall of the cell C_1 (respectively C_2).

The shift in emission levels between two sets of measurements performed with the same IC inserted successively in cells C_1 and C_2 is given by:

$$V_{out,2}(f)\Big|_{dB\mu V} = V_{out,1}(f)\Big|_{dB\mu V} + 20\log(\frac{h_1}{h_2}) \tag{4-4}$$

The aperture position dedicated to ICs characterization in the GTEM cell has been adjusted to obtain an IC-to-septum spacing close to the one found in most TEM cells (i.e. 45 mm). Figure 4-13 shows the results of emission measurements from a 16-bit microcontroller. The IC was mounted in a TEM/GTEM compatible test board, and successively inserted in a Fischer TEM cell (with a septum-to-aperture spacing of 45 mm) and in the SAE aperture of a Schaffner GTEM 250.

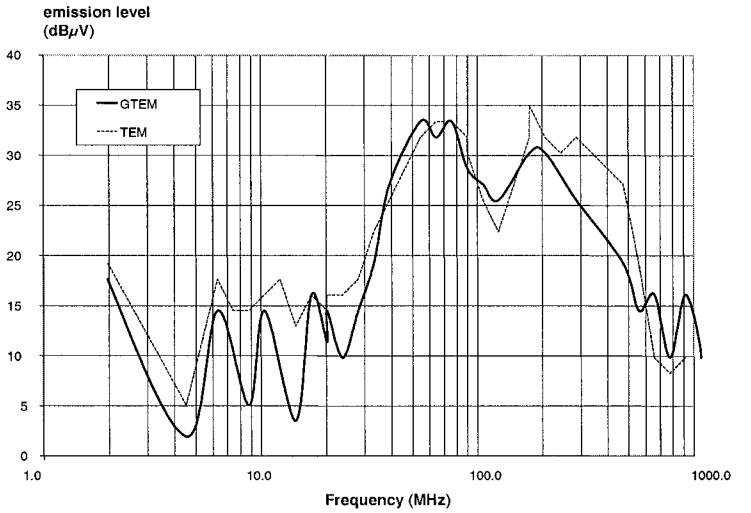

Figure 4-13. Measurement of the radiation from a component in a TEM cell and in a GTEM.

Emission measurements were performed for the same orientation of the component, with the same program running into it, and with the same settings of the spectrum analyzer. As expected, the two plots are almost identical over the whole frequency range.

3. NEAR-FIELD SCAN

The near-field scanner was adapted to the problem of the integrated circuits by K. Slattery (1999), with a resolution high enough to map the fields above integrated circuit packages. Many research labs involved in the study of chip-level EMC are now using near-field scanners. Specific probes connected to a receiver measure the amplitude and phase of a selected component of the electromagnetic field radiated by the integrated circuit.

Measurement methods which determine the EM field by the use of a radio-frequency receiver may be classified in two main techniques. The direct technique involves a coaxial cable to connect the probe to the receiver as shown in Fig. 4-14.

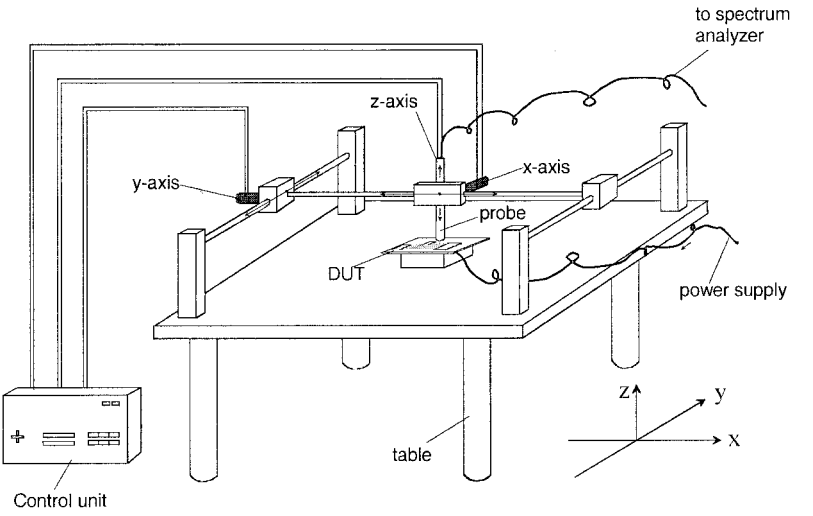

Figure 4-14. Example of a near-field scanner setup.

The second technique creates a perturbation by introducing a scatterer at the desired observation point, to enhance the spatial resolution and to reduce the parasitic coupling between the probe and the device under test. For improved sensitivity and spatial discrimination, the scattered signal is modulated and the receiver discriminates between the modulated and the parasitic signals (Garreau, 1992). Several kinds of modulation - mechanical, electrical and optical – are discussed and compared by Bolomey (2001).

In the case of electrical modulation, the low-frequency signal propagates through a high resistive metallic support to avoid additional perturbations. An optical fiber associated with a modulated light source can be used to reduce further the aforementioned risk of perturbation (Liang, 1997).

3.1 Scanner and positioning system

The mechanical positioning moves either the probe or the device over a planar surface. An example of a near-field scanner developed at ENSEEIHT, Toulouse, France, is shown in Fig. 4-15. The structure should present a minimum amount of reflective area to the test device. Absorbant material can be added and put on the metallic scanner supports and cables.

Displacement of the probe can be carried out according to rectangular or polar axes. The scanning surface needed for integrated circuit near-field measurements usually ranges from 2x2 cm up to 10x10cm.

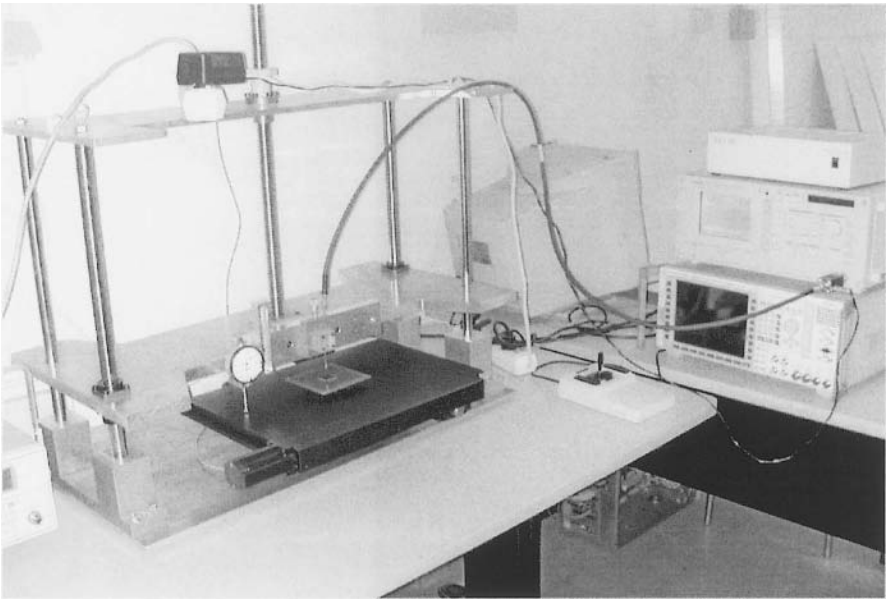

Figure 4-15. Near-field scanner and mechanical setup.

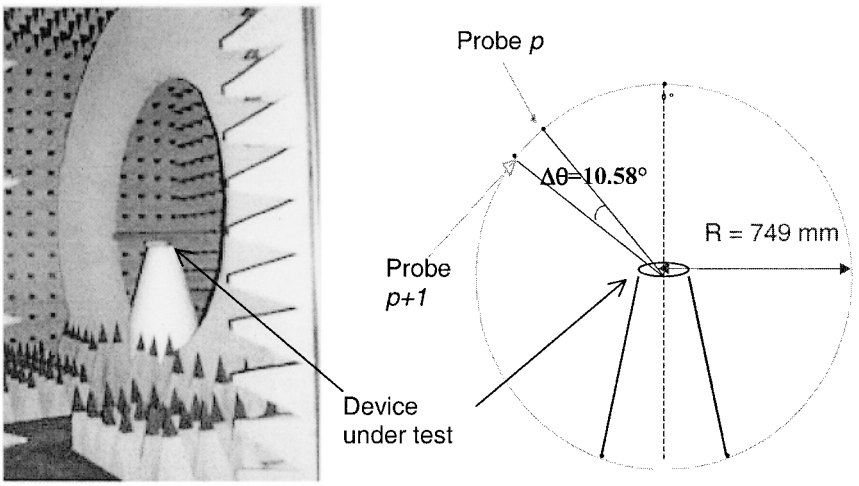

Figure 4-16. Photograph of the spherical test setup at IETR Rennes, France.

The time required to move the single probe can be accelerated using a probe array. The probes are connected to a receiver through a switched combiner or a multiplexer.

To overcome the drawbacks of multiport connections, the signal in the selected channel is modulated which guarantees a good dynamic range. The modulation can be performed using a switched diode. Several available architectures using wired and wireless combiners are described in (Bolomey, 2001). A spherical near-field setup based on the electrical modulation is depicted in Fig. 4-16. Installed in an anechoic room, the system consists of an arch on which about 30 bipolarized probes of measurement are distributed. An electronic sweep of these probes makes it possible to reach, in real time, the radiation patterns. The full radiation sphere is then obtained thanks to a combination with an azimuth positioning.

3.2 Probes for near-field scanning

Near-field probes consist of small antennas mounted on scanning mechanism, and their electromagnetic properties enable to capture one particular component of the field: magnetic field *Hx,Hy, Hz* along the X,Y or Z axis, electrical field *Ex,Ey, Ez* along the X,Y or Z axis. The probes should:

- Be highly sensitive to the desired field component.
- Reject all other undesired components.
- Feature a high spatial resolution.
- Not disturb the measured field.

Simple and practical probes use the inner conductor of a 50 Ω semi-rigid coaxial cable. Fig. 4-17 shows a typical construction for monopole and dipole coaxial probes. The more popular one is the coaxial monopole antenna (*Ez* probe). The coupling between the probe and the device under test is mainly capacitive (Gao, 1998). This type of probe provides the measurement of the vertical component of the *E* field.

The probe size should match the spatial resolution. In practice, the loop size is close to 1 mm, to achieve an acceptable spatial resolution for the scan of integrated circuits. If the probe size is decreased, the amplitude of the received signal will be reduced and the signal-noise ratio will be lowered. For minimum disturbance, the inner conductor is cut in the same plane as for the outer coaxial conductor (Fig. 4-17). This geometry may reduce the intrusion of the probe but leads to a decreased sensitivity. In order to reduce parasitic currents that may flow on the outer part of the coaxial cable, a small shielding or absorbers may be added at the far end of the probe.

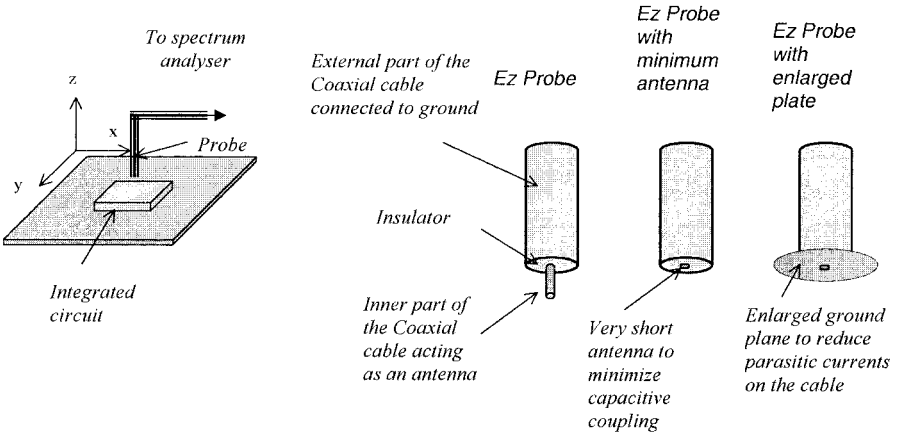

Figure 4-17. Coaxial electric probe for *Ez* measurement.

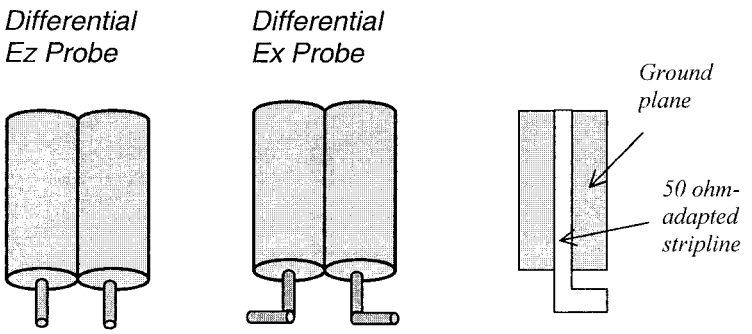

Figure 4-18. Coaxial electric probes for *Ex, Ez* measurement using coaxial cables and planar conductors.

To measure the tangential field components, electrical dipoles can be used in a surface over a device. Fig. 4-18 shows examples of coaxial probes for Ex/Ey measurement, in coaxial and planar technologies. Coaxial probes have been investigated by Budka (1996) for electric field measurement up to 18GHz. Loop probes are widely employed for magnetic field characterization (Kazama, 2002). The IEC 61967 standard (IEC, 2001) includes in its Part 3 a detailed presentation of radiated surface scan measurement methods, with some recommendations regarding the design and connection of magnetic probes. Fig. 4-19 gives an example of a near-field magnetic probe manufactured according to the standard.

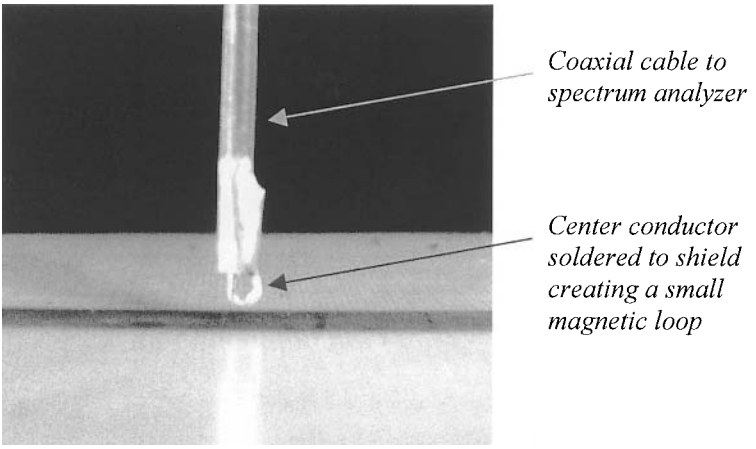

Figure 4-19. Example of magnetic probe.

The current induced across the loop is proportional to the incident magnetic field that is normal to the loop plane, according to the following expression. Considering that the loop terminations are connected via a cable to the 50 Ω input impedance of the spectrum analyzer, the measured power P_{meas} is linearly dependent on the magnetic field present at the probe location.

The probes require a rigorous calibration procedure to obtain absolute field measurements. The link between the power P_{mes}(in dBm) and the magnetic field (dBA/m) may be established by measuring the near-field power above a simple 50 Ω test structure and by comparing it to an absolute field H computed by 3D electromagnetic solvers.

The Probe Performance Factor (PPF) introduced in the following equation has a simple dependence versus frequency up to 1 GHz, as shown in Fig. 4-20 for a 2 mm magnetic loop.

$$H(x,y,h,f) = PPF(f) + P_{mes}(x,y,h,f) \tag{4-2}$$

It should be noticed that the measured field corresponds to an average taken over the surface of the probe. Furthermore, the resulting signal corresponds to a convolution of the electromagnetic field with the probe radiation pattern. The deconvolution is a mathematical operation that modifies the measured scan in order to eliminate the field modifications induced by the probe.

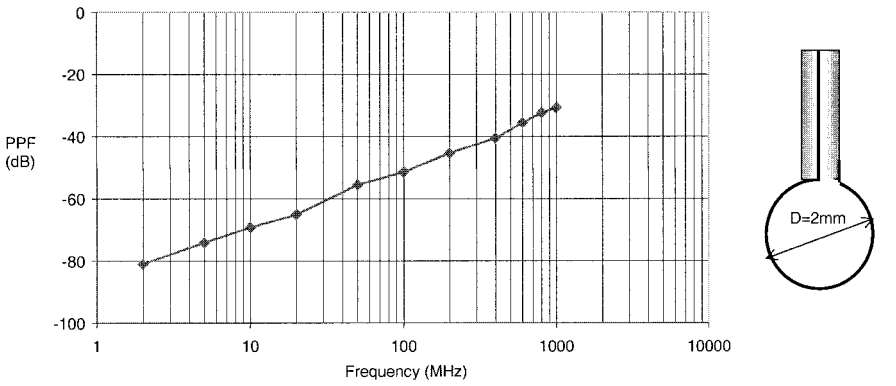

Figure 4-20. Probe performance factor dependence vs. frequency.

It is usually carried out for each (X, Y) coordinate of the scan, by dividing the measured field by the probe response. For a probe having a cross polarization component, the compensation becomes more complex (Bolomey, 2001). Whereas vector field determination requires the absolute measurement of two quantities (modulus and phase), the determination of field level for EMC application firstly requires the measurement of the modulus. Adding the phase information make it possible to extract the current orientation as well as the delay.

3.3 Integrated circuit emission

As a practical application, we present an investigation concerning the radiated emission of an ALTERA programmable device mounted on a leadless carrier fixed on a double-face printed circuit board.

The photographs in Fig. 4-21 show the metal layer on the top and bottom surfaces of the test board. The external components include a 5V regulator, filtering capacitors, and a RAM memory. The BNC connector feeds the board with a 10MHz clock signal with a rise time of 5ns and 50% duty cycle.

The near-field measurements were conducted using the ESIGELEC scanner (Baudry, 2004), with a 2.0 mm magnetic probe built with two adjacent coaxial cables. The probe orientation corresponds to the X axis of Fig. 4-22. The spectrum analyzer measures the difference between the two inner conductors of the coaxial cables thanks to the hybrid 180° coupler.

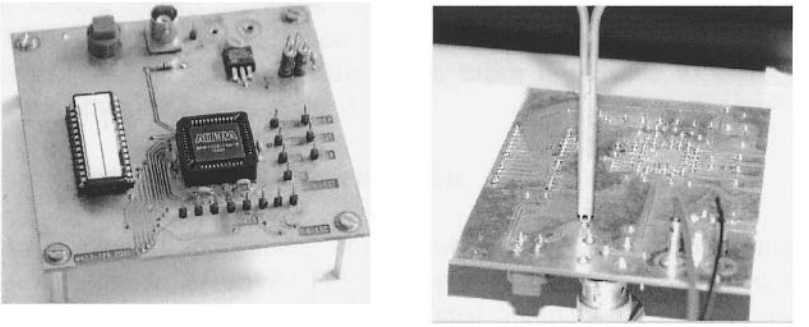

Figure 4-21. The test IC and its printed circuit board.

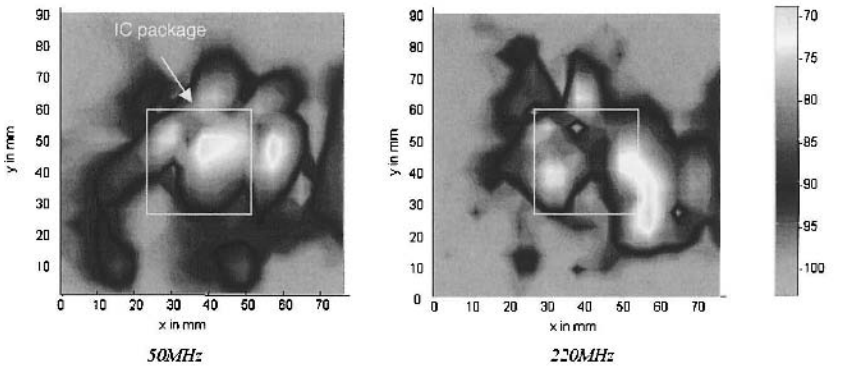

Figure 4-22. Near-field maps (f=50 MHz, right f=220MHz) with probe oriented along the x-axis.

The scan reported in Fig. 4-22 was recorded at 50 MHz and 220 MHz, at an altitude h of 4.0 mm above the board ground plane, which corresponds to the reactive near-field zone ($h<<\lambda/2\pi$). The resolution bandwidth (RBW) of the analyzer spectrum was set to 3 kHz. The gray scale gives the correspondence with the relative magnetic field intensity. One can see that the zone with maximum field is located above the integrated circuit (center of the scan), and correlates to the clock tracks (bottom left). The scan frequency of 50 MHz corresponds to the fifth harmonic of the clock signal, which contains significant energy in higher harmonics due to its square shape. The clock contribution at 220 MHz is significantly reduced, and the field is mainly concentrated around the IC package.

3.4 Discussion

Based on contact-less measurements, the near-field technique represents a valuable tool for investigating the electromagnetic interference produced by integrated circuits, both analog and digital. Regions with a strong magnetic field may be easily localized above the surface of the integrated circuit and the package. Due to the continued demand for miniaturization, improved spatial resolution and higher sensitivity will be required, leading to innovative probe designs that may embed filtering and amplification.

The main drawback of the near-field scan is the time required to complete each scan at each given frequency. A complete scan of all electric and magnetic contributions of the field for the 10 main harmonics of an integrated circuit would require several days of measurement. Isotropic probes combined with parallel measurement setups may reduce the duration to several hours.

4. 1/150 Ω CONDUCTED METHOD

A very useful method for evaluating integrated circuits is to measure the conducted noise currents on each pin. One method of doing this (IEC, 2001) is to place a small resistance in series with the pin and measure the voltage dropped across this resistance (Fig. 4-23). Since most emissions problems related to chip designs begin with noise that is conducted out of the chip package via the pins, this measurement can be a particularly good indicator of how well the chip will perform in a real product. The test set-up for I/Os is given in Fig. 4-24. A combination of resistance and capacitance introduces an equivalent load of 150 Ω.

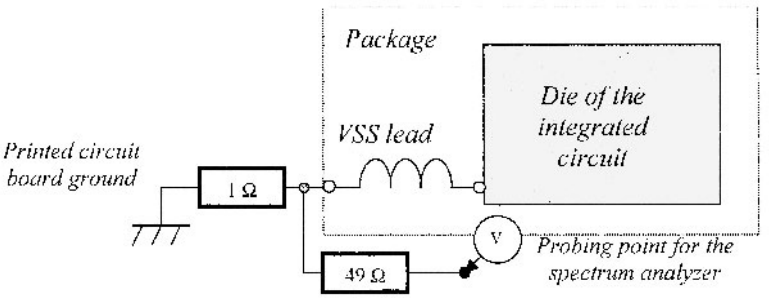

Figure 4-23. 1/150 Ω Conducted mode measurement method.

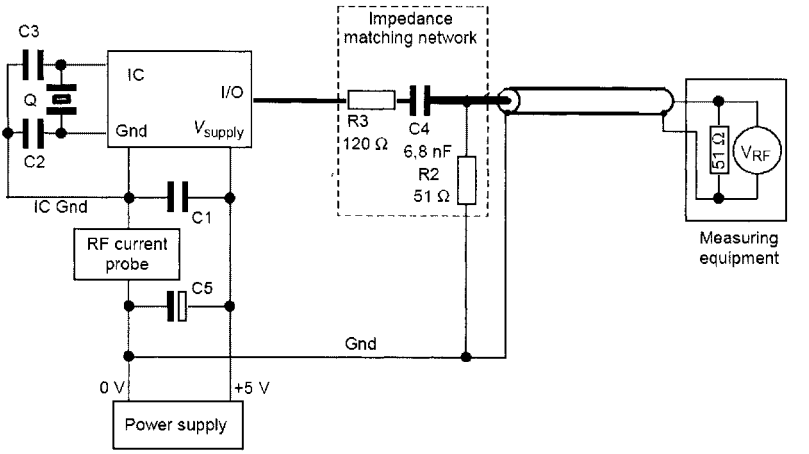

Figure 4-24. Test setup for I/O conducted noise measurement (According to IEC 61967-4).

This test configuration corresponds to a general case but may be adapted depending on the device under test and the application. In the case of an IC with a huge number of pins, a selection should be made to keep the probing points reasonable, as the test boards must include for each test pin supplementary resistance, capacitance as well as high quality connector such as SMA or SMB.

In order to obtain a high degree of repeatability in the conducted measurements and comparison emission performances of ICs mounted on different printed circuit test boards, guidance is given in the standard for the choice of the PCB material and dielectric. The standard also recommends the use of a ground plane on the board, and describes how to implement the DUT with multiple ground and supply. For high power ICs, the 1 Ω probe is replaced by a 0.1Ω resistance, or split among the return current paths.

5. WORKBENCH FARADAY CAGE

The Workbench Faraday Cage is a standard method for carrying out conducted RF immunity measurements (IEC, 2003) in a compact manner, without requiring large anechoic rooms and high power RF sources. The WBFC method may also be used for conducted emission measurements, as described in (IEC, 2001).

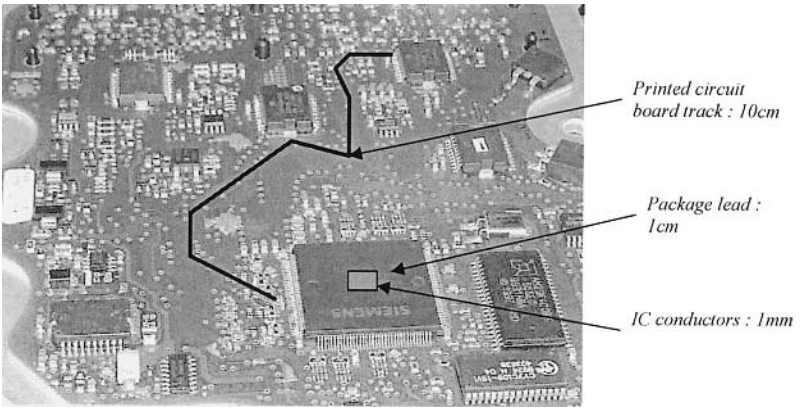

Figure 4-25. Test board example and associated conductor dimensions.

The rationale for conducted EMC measurement stems from the fact that the root cause of RF emission is often the die of the integrated circuit which by means of on-chip and on-PCB coupling paths radiates into the "free-space". Here the rationale of the effectiveness of the antenna applies: the lower the frequency, the larger the antenna needs to be. The IC die dimensions of 5 mm would correspond to an optimum resonant frequency of 16 GHz (Fig. 4-25). The correspondence between resonant frequency and physical dimensions is reported in Table 4-4.

Table 4-4. Optimum antenna effect

Frequency	1 MHz	10 MHz	100 MHz	1 GHz	10 GHz
Wavelength λ	300 m	30 m	3 m	30 cm	3 cm
Optimum antenna (λ/4)	75 m	7.5 m	75 cm	7.5 cm	7.5 mm
Physical antenna	Long cable	Cable	Large PCB	PCB track	Package lead

In case of RF emission testing, a measurement antenna can be used to pick up the electromagnetic field which is then represented on a spectrum analyzer. By means of passive coupling and decoupling networks (CDN), the whole interaction path between the root disturbance source and the input of the measurement receiver can be defined. As passive networks are reciprocal, the same setup can also be used for RF immunity measurements.

Various groups and individuals have been involved with common mode impedance measurements in Switzerland, Germany, Japan, and the Netherlands. All results show a broad distribution of this common-mode impedance which could vary as a function of frequency between less than one Ω to several kilo-Ω.

Table 4-5. Common-mode impedance requirements for coupling and decoupling networks (CDN)

Frequency band	150 KHz – 26 MHz	26 MHz – 1000 MHz
Common-mode impedance	150 Ω +/- 20 Ω	150 Ω +60/-45 Ω

Nevertheless, from all these measurements, the median value found was 150 Ω with rather thigh tolerances. For the sake of reproducibility, the tolerances need to be low.

5.1 Scope of applicability of the WBFC method

Before going any further, the reader should be aware that the scope of this method is restricted to electronic products that will be connected to external wiring. It is not a suitable measuring method for small wireless appliances! Nevertheless, the method will apply for those cases where the wires and cables connected to the sources and victims are much longer than the largest dimension of the integrated circuit. The minimum frequency of the range used will be determined by the maximum length of wire connected to that port.

The size of the cage has been set to 0.5 x 0.35 x 0.15 m and will therefore show specific resonances with respect to these dimensions. The formulation for the resonant frequency of the WBFC depends on its physical dimensions W, L and H as follows (Eq. 4-5):

$$f_{mnp} = \frac{1}{2\sqrt{\mu_0 \mu_r \varepsilon_0 \varepsilon_r}} \sqrt{\left(\frac{m}{L}\right)^2 + \left(\frac{n}{W}\right)^2 + \left(\frac{p}{H}\right)^2} \qquad (4\text{-}5)$$

where
f_{mnp}=frequency (Hz)
ε_0= absolute permittivity (8.85 x 10^{-12} F/m)
ε_r= relative permittivity (Air= 1.0)
μ_0= permeability 4π x 10^{-7} H/m
μ_r= relative permeability (Air= 1.0)
m, n, p=modes (integer 0,1,2...)
L= length of WBFC (m)
W= width of WBFC (m)
H= height of WBFC (m)

However, due to the common-mode loaded PCB placed in the cage during normal use, the quality of these resonances will be poor and restricted to a few frequencies only, above 1 GHz. By applying Eq. (4-5), we find 1.13 GHz, 1.24 GHz, 1.35 GHz, etc.

5.2 Concept of the workbench Faraday Cage method

In Fig. 4-26, a simple test setup is given. In general, an IC on a PCB has 2, 3 or more connections e.g. input, output and supply. In the drawing of Fig. 4-27, only 2 ports are considered. A normalized disturbance source (In case of RF immunity measurements), will determine the RF currents and RF voltages at the product being tested.

When the two ports both represent an impedance of 150 Ω in common-mode, then the voltage at the device U_{com} will be half the source voltage of the disturbance source. The link between the electric field E and the device potential U_{com} is given by Eq. (4-6).

The support height is typically 30 mm for IC measurements. The common-mode current I_{com} will distribute itself over the DUT surface with a current density distribution J_{com} which will result in local H-fields for which formulae from Biot and Savart can be applied (Eq. 4-7). For an infinite number of ports, the current would be no more than double.

$$E = \frac{U_{com}}{height} \tag{4-6}$$

$$H = \frac{J_{com}}{2\pi R} \tag{4-7}$$

$$V_{AB} = I_{com} Z_{DUT} \tag{4-8}$$

On the contrary, the *E*-field between the PCB containing the IC and the ground reference plane (GRP) will diminish as the common-mode voltage would, under this condition, decrease to zero. The schematic diagram of the connection between the DUT and the external equipments is given in Fig. 4-28, showing the DUT, the ferrite rings, the connection cables, the filters in the Faraday Cage wall and the external equipments used to supply and monitor the DUT.

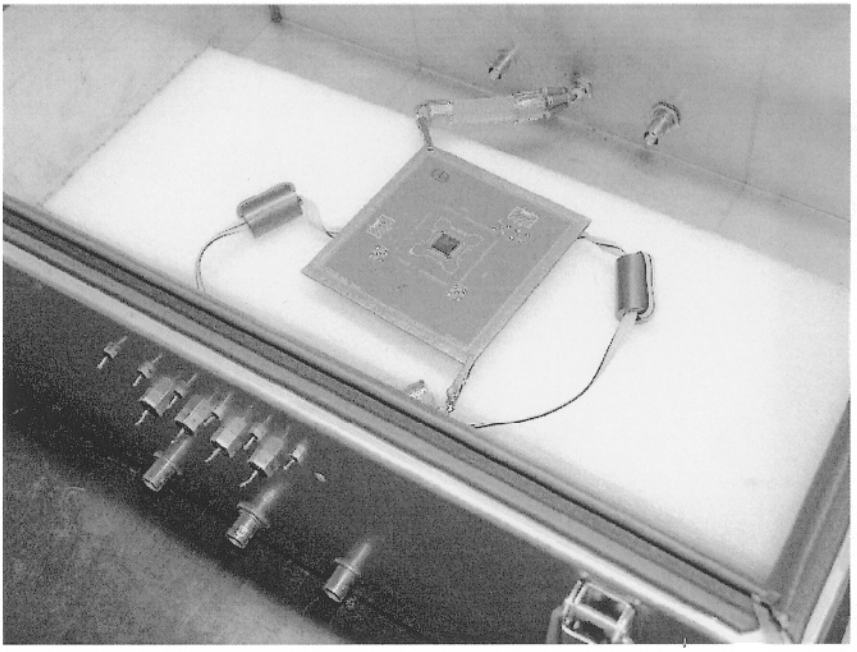

Figure 4-26. The device under test inside the Workbench Faraday Cage (WBFC).

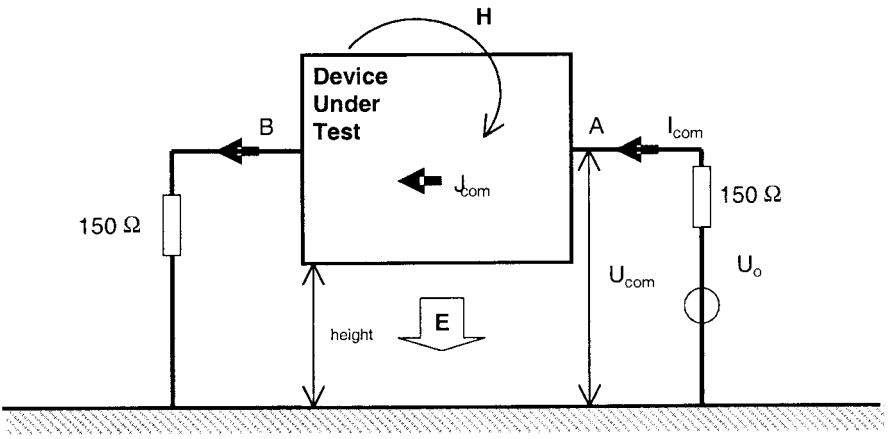

Figure 4-27. Electrical concepts related to the WBFC method.

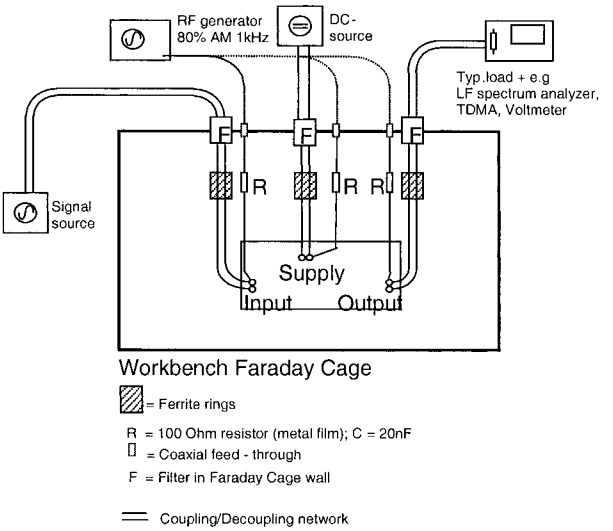

Figure 4-28. Schematic diagram of the connection between the DUT and the external equipments.

5.3 Power matching

Power matching consists in finding the optimum way to transfer the power of the source to the victim. Poor power matching corresponds to the case where the device under test handles a very small fraction of the power generated by the radio frequency source.

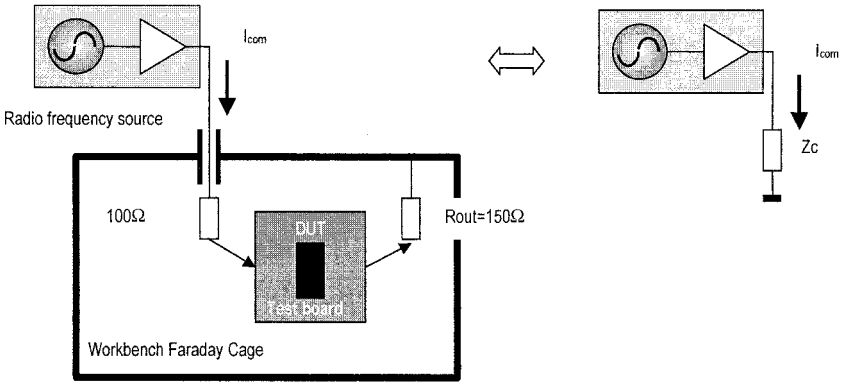

Figure 4-29. The device under test on its test board is equivalent to an impedance *Zc*.

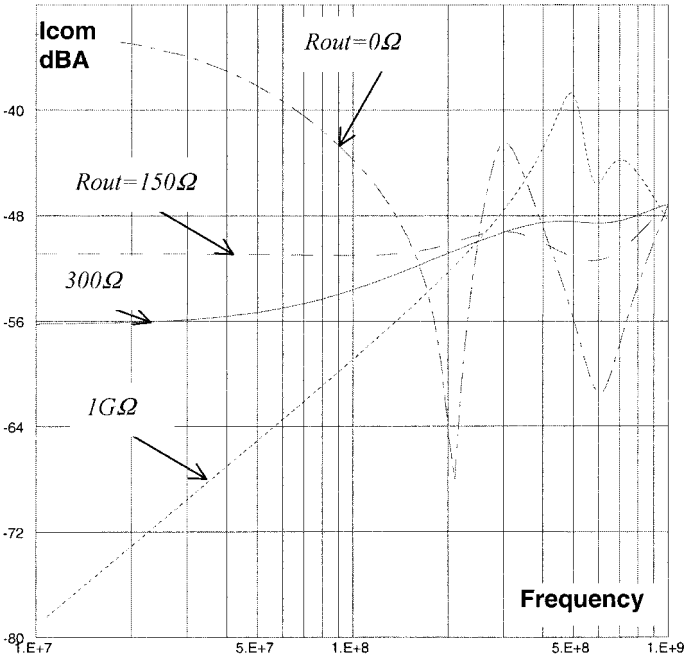

Figure 4-30. Variation of the current delivered by the apparatus for varying frequency and common-mode termination.

Let us have a closer look into the common-mode behavior of the circuit under test. The common-mode impedance Z_c is the equivalent load seen by the radio-frequency generator, as illustrated in Fig. 4-29.

The impedance is strongly dependant on the generator frequency. Z_c may also vary according to the loading conditions of the IC ports. In Fig. 4-30, the current *Icom* delivered by the apparatus to a two-port test-board is simulated for a wide range of frequency, for varying common-mode termination R_{out}.

Power matching occurs when the variations in the current delivered to the test board are almost independent of the injected frequency. As can be seen from simulations, the common-mode can be stabilized best when using a common-mode termination *Rout* of 150 Ω.

5.4 Coupling decoupling networks

The function of the Coupling/Decoupling network (CDN) is to couple the RF signal to the device under test, while being transparent for the functional signal, as illustrated in Fig. 4-31.

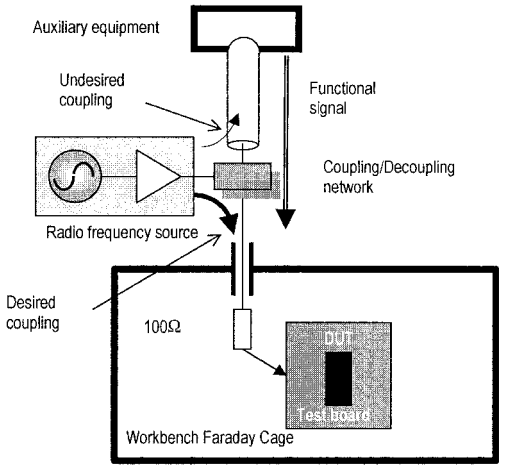

Figure 4-31. Coupling/Decoupling network used to couple the desired signal with the radio-frequency source.

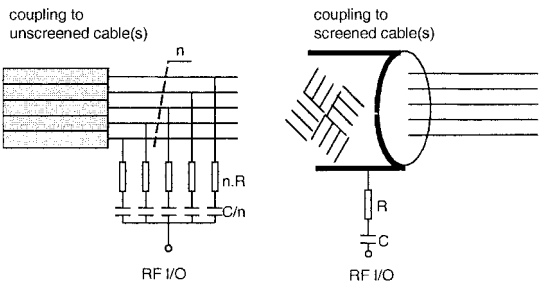

Figure 4-32. Coupling to cables.

Typically a directivity of 40 dB is required from a CDN. The typical insertion loss of a CDN is less than 5 dB. When impedance ratio transformers are used (rather than series resistance transformers), even negative insertion loss values can be obtained.

With non-shielded wires (Fig. 4-32 left), the RF coupling is distributed equally over all the wires, independently of their function. Resistances of N.100 Ω are applied in series with 22 nF capacitors. With shielded cables (Fig. 4-32 right), RF coupling with the shield is done by means of a 100 Ω resistance in series with a 22 nF DC-blocking capacitance. To maintain a common-mode impedance of 150 Ω, the center of the test board ports is located at 30 mm above the ground plane.

5.5 Measurements

With the workbench measurement technique, the RF emission spectrum from an IC applied on a standard test board can be measured from 150 kHz to 1 GHz. These measurements are usually repeated for the various modes of operation of the IC to be tested. Furthermore, similar to the TEM cell method, the EMC test board shall be measured in four orientations, by turning the board over 90 degrees each time. In Fig. 4-33, the max-hold RF emission amplitude as function of frequency is recorded from 0.1MHz to 1GHz.

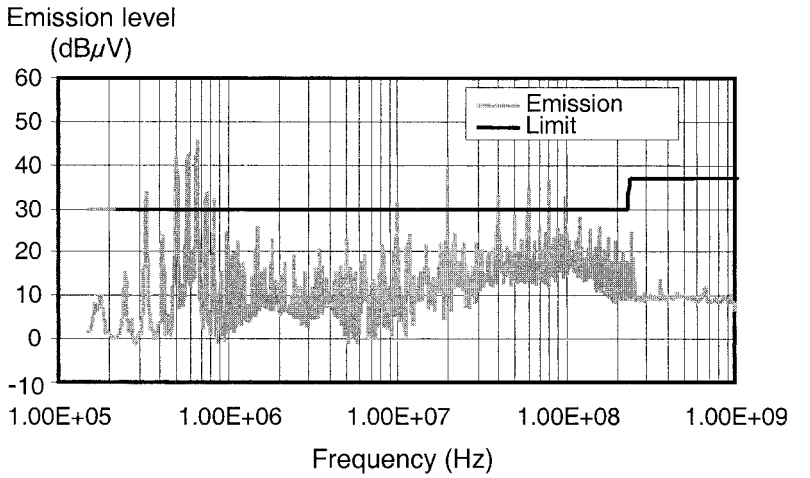

Figure 4-33. Conducted measurement using WBFC.

To determine the RF immunity of a digital device, various parameters can be observed. In the example shown in Fig. 4-34, the jitter on the IC's program cycle is measured as function of the disturbance signal carrier frequency.

Similar to the RF emission test using the WBFC method, the EMC test board shall be measured in four orientations, by turning the board over 90 degrees each time. In this figure, the maximum jitter as function of frequency is recorded for the various orientations. Different jitter responses can be observed depending on the program cycle.

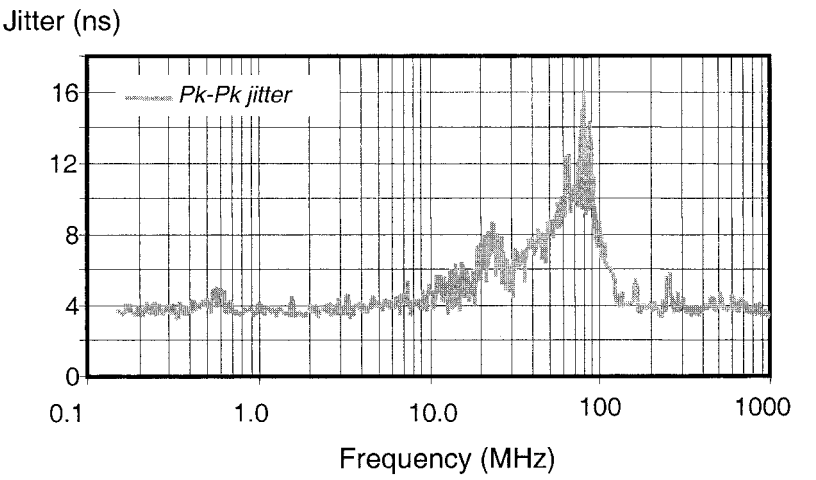

Figure 4-34. Jitter measurement using the WBFC method.

5.6 Discussion

In contrast to techniques such as TEM/GTEM cell, near-field scanning and the DPI, BCI method, the whole application plays a dominant role in the results obtained. Moreover, as RF emission would diminish in a TEM cell measurement, e.g. by placing a copper hood over the IC which is soldered to the reference layer, the RF emission results with the WBFC technique are hardly affected by such a measure as *di/dt* through the IC's pins and the currents through the PCB remain unaffected.

With RF emission measurements, other than the peak RF emission level obtained by a max-hold function, the duration of these peaks becomes relevant as spread spectrum clocks are often used with digital designs or frequency hopping with digital RF modulation formats.

A simple reduction of the measurement bandwidth of the spectrum analyzer or RF measurement receiver to a bandwidth beneath the hopping format or spread spectrum will reveal this information at the cost of measurement time without the used of dedicated measurement equipment.

Setting the requirements is not that simple as they will be determined by what needs to be protected; narrowband RF broadcast, sensitive analog base-band signals or micro-powered broadband logic. Guidance is absent or at best insufficient in the formal standards as this topic is too broad and too open!

With RF immunity measurements, the response of the device has to be observed. Here too, the broad variety of responses means that nearly

everything can be measured, but what is relevant? Responses like audio break-through, similar to the Moire-patterns on a display panel are well known. But simple responses like; supply current fluctuations, DC or base-band gain, a port's output frequency, duty cycle and jitter are easy to detect and measure before a device or product hangs in a real error condition. Lengthy measurement schemes where e.g. Bit-Error-Rate (BER) has to be measured as a function of the disturbance signal's frequency may be necessary but before bit errors occur, jitter will occur on these signals.

Due to the well-defined common-mode impedance conditions, the reproducibility of WBFC measurements is good and the cost for a measurement setup is low. Measurement techniques as defined by the WBFC method can be used to characterize the device emission (IEC 61967-5) and immunity (IEC 62132-5).

6. BULK CURRENT INJECTION (BCI)

This chapter describes the conducted immunity measurement method called Bulk Current Injection (BCI). The measurement philosophy consists in reproducing the induced current that could be generated in the real world by electromagnetic fields coupled on the wires of a system.

The BCI method as defined in the standard proposal IEC 62132-3 (IEC, 2003) is inspired from the system level BCI method and has been adapted to the IC characterization mainly by specifying a specific test board setup.

The pin of the Device Under Test (DUT) that will be disturbed is connected to a typical load as specified by the IC supplier through a wire.

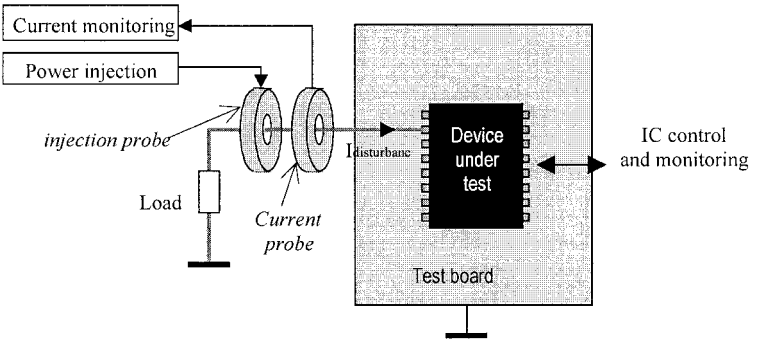

Figure 4-35. Typical configuration for a BCI test.

Load, wire(s) and DUT are located on a ground plane at a specified height and usually inside a Faraday cage. The power supply pins are usually

connected to power supply using filters, for example LSIN equipment (Line Stabilizer Impedance Network) – even if the common LSIN only offers a valid frequency range up to 100 MHz).

In any case, the power supply should not be disturbed by the RF signal. The RF disturbance is then injected into the DUT using an injection probe. The measurement probe monitors the level of injected current. The probe position could differ from one customer specification to another. Several IC pins could be disturbed at the same time, if the injection probe surrounds the wires connected to these pins. Fig. 4-35 illustrates a typical configuration for a BCI test.

6.1 Calibration of the RF injection system

In accordance with IEC 62132-3, the required power from the RF generator is determined during the calibration of the injection probe. The purpose of this calibration is to determine the power level required at the signal generator to reach a defined current level on the 50 Ω-adapted load.

The current level curve, depending on the frequency, is defined in the EMC specification associated with the device under test. This calibration is done in Continuous Wave (CW) mode, which means that the RF disturbance is equal to a pure sinusoidal waveform on the whole frequency range (commonly DC to 400MHz). The setup is shown in the Fig. 4-36. A schematized diagram of the setup is given in Fig. 4-37.

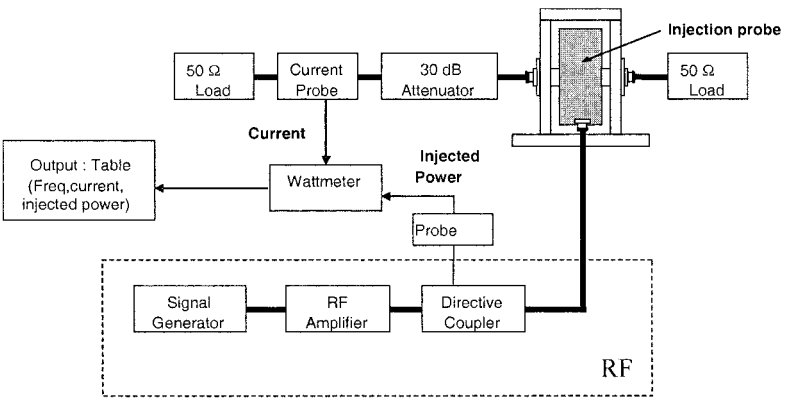

Figure 4-36. Calibration setup for the RF injection probe.

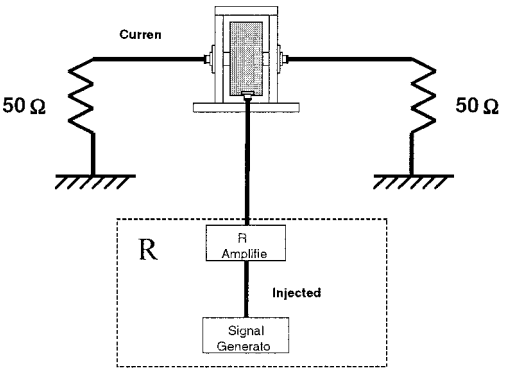

Figure 4-37. Schematized diagram of the calibration setup for the RF injection probe.

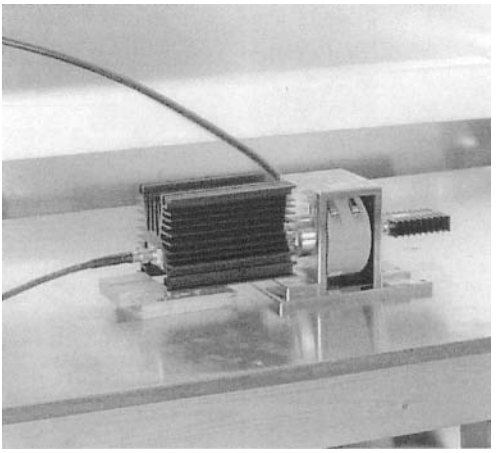

Figure 4-38. Picture of a calibration setup for the RF injection probe.

The two 50 Ω loads, the attenuator, the current probe and the calibration fixture are connected with 50 Ω-adapted cables if necessary. An attenuator (30 dB in this example) is required to protect the 50 Ω-adapted serial current probe from the high current produced by the RF injection probe. The calibration fixture is used as a 50 Ω-adapted load (Fig. 4-38).

The calibration process should be performed for each current limit to take into account the non-linear behavior of the hardware used for the RF disturbance generation (injection probe, amplifier, generator). The calibration procedure produces a plot of the forward current required to inject 200 mA in the reference load of 50 Ω, as a function of frequency (Fig. 4-39).

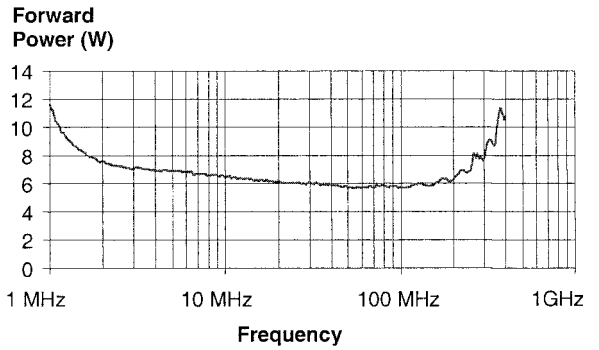

Figure 4-39. Forward current vs. frequency used for probe calibration at 200 mA.

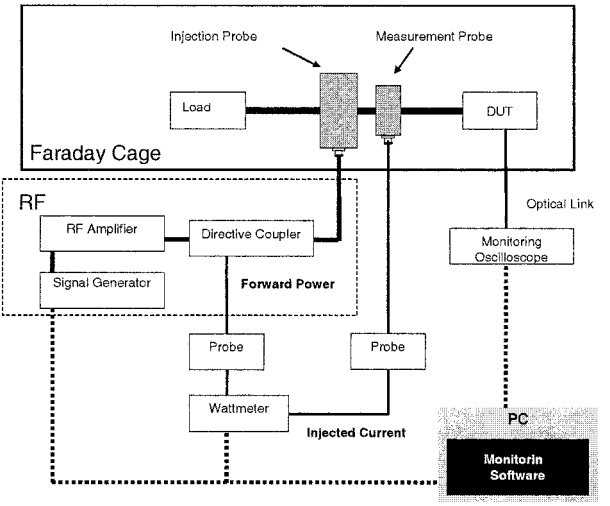

Figure 4-40. BCI measurement test setup.

6.2 Measurement setup

The BCI measurement test setup is described in Fig. 4-40. Although not explicitly required in the standard, the BCI test measurement should be performed inside a Faraday cage. The main justification of this precaution is the measurement repeatability. Inside a Faraday cage, the position of the ground plane is correctly defined, as well as the position of the different elements (probes, cables, DUT). Furthermore, the influence of external EM fields (FM band, cell phones, etc.) is minimized.

Depending on the EMC specification required by the customer, many configurations could be tested: for example, the injection could be performed only on the power supply wire, or on the power supply wire with the ground wire, or on a complete harness (supply wires with additional wires for signals).

6.3 Disturbance

The signal used as the RF disturbance in this test could either be:

- A continuous sinusoidal signal (CW)
- A continuous sinusoidal signal with AM modulation (AM)

Usually, the modulation signal is a sinusoidal waveform with a frequency of 1kHz. The modulation factor m is often fixed at 80%. For ICs, the test method uses a constant peak level for both CW and AM signals as shown in the following figure. The relationship between the peak level for the CW and the AM signals is given by Eq. (4-9):

$$P_{am} = P_{CW} \frac{(2+m^2)}{2(1+m)^2} \tag{4-9}$$

For $m = 0.8$ (i.e. 80%), the relationship becomes:

$$P_{am} = 0.407 P_{CW} \tag{4-10}$$

For the AM disturbance with a modulation factor equal to 80%, the signal level at the generator is decreased by 5.1 dB in comparison with a CW disturbance.

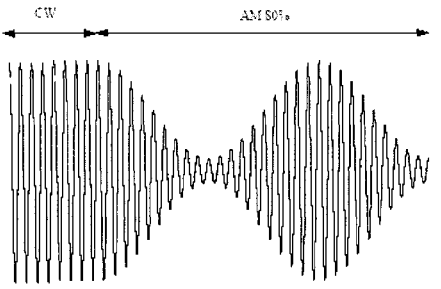

Figure 4-41. Relationship between CW and AM signals.

At each step, the DUT should be exposed to the disturbance during a fixed time called *dwell time*. This dwell time should be at least greater than the minimum response time of the DUT. In any case, the dwell time should not be less than 1s.

6.4 Algorithm for BCI measurement

The calibration procedure gives information about the injected power required for generating a specified current at a given frequency, but on a standard 50 Ω load. Replacing these two 50 Ω-adapted loads by an IC will change the equivalent input impedance and therefore the current generated inside the wire during the BCI test. The RF current induced in the wire could be higher if the input impedance of the IC is lower than 50 Ω, or lower if the input impedance of the IC is higher.

That is why when operating the BCI method, we have to monitor the injected current. With a high input impedance DUT, the injected power limit could be increased by the *k* factor. In automotive applications, *k* varies from 1 to 4 depending on the device under test.

The measurement algorithm is illustrated in the flow graph of Fig. 4-42. For each frequency, the RF disturbance level is increased step by step until one of the conditions is attained: the current limit has been reached, or the DUT has failed. For reducing the test time, the initial power level at the following frequency point may be set for example 6dB lower than the previous one.

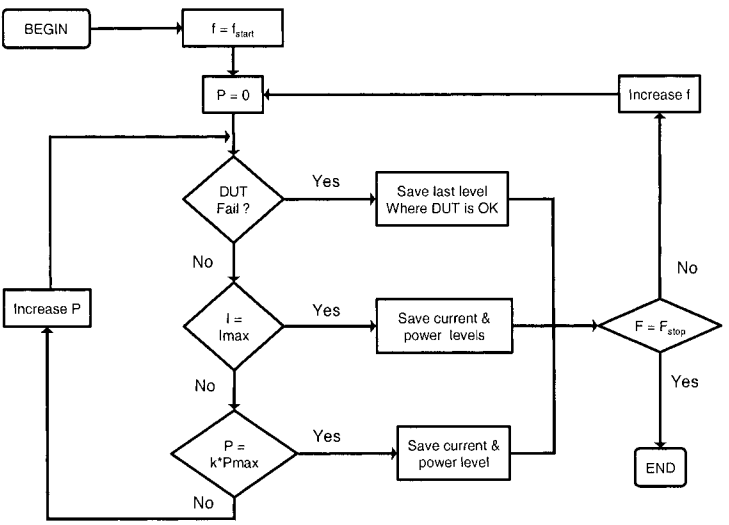

Figure 4-42. Flowchart for BCI measurement.

6.5 Failure criterion detection

For immunity tests, the failure criterion is difficult to define. Today, no universal failure criterion has been highlighted for any type of IC. The failure criterion is relative to an electrical measurement such as current or voltage on a selected pin. Many criteria could be used such as: jitter on a digital signal, undesired activation of an I/O, Reset of a microcontroller, etc.

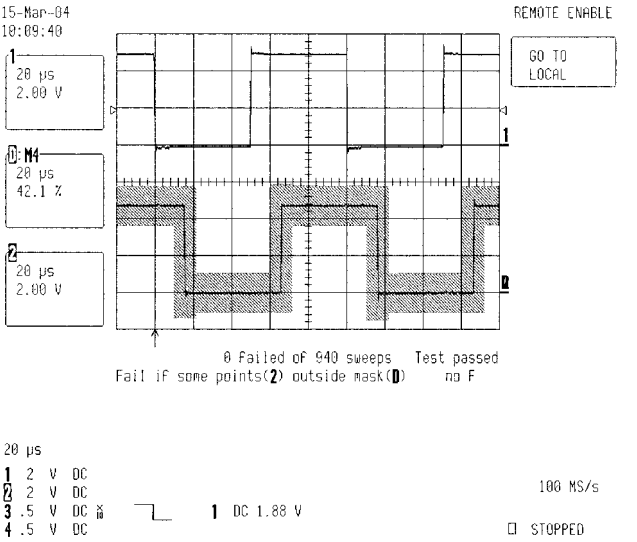

Figure 4-43. Screenshot of an oscilloscope used for envelope detection.

Usually, the failure criterion is detected by using the mask function of an oscilloscope as shown in Fig. 4-43. This method is particularly convenient for automated testing. If the signal is detected outside the mask (defined by a tolerance factor in time and amplitude from the wave without disturbance), the oscilloscope sends a flag signal to the control software, which stops the injection power increase.

6.6 PCB and hardware setup

Up to now, no distinction has been made between the ISO standard and the IEC standard listed in the introduction.

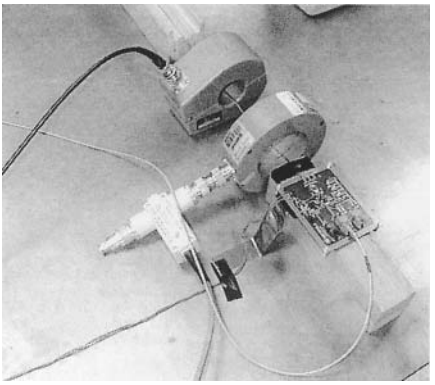

Figure 4-44. ISO BCI setup.

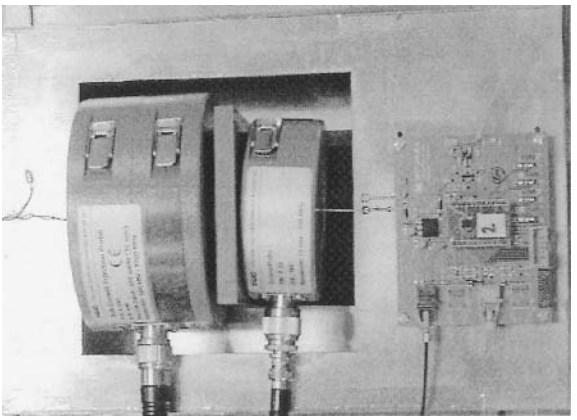

Figure 4-45. IEC BCI setup dedicated to IC.

The ISO standard (Fig. 4-44) is applicable for electronic systems while the IEC standard is dedicated to single components (Fig. 4-45).The example shown here concerns a physical interface for LIN bus communication widely used in automotive applications.

6.7 BCI test results

Fig. 4-46 and Fig. 4-47 give results related to BCI measurements performed on a test chip. On the first graph, the bold line corresponds to the current limit required by the customer; the gray line corresponds to the injected current measured by the current probe.

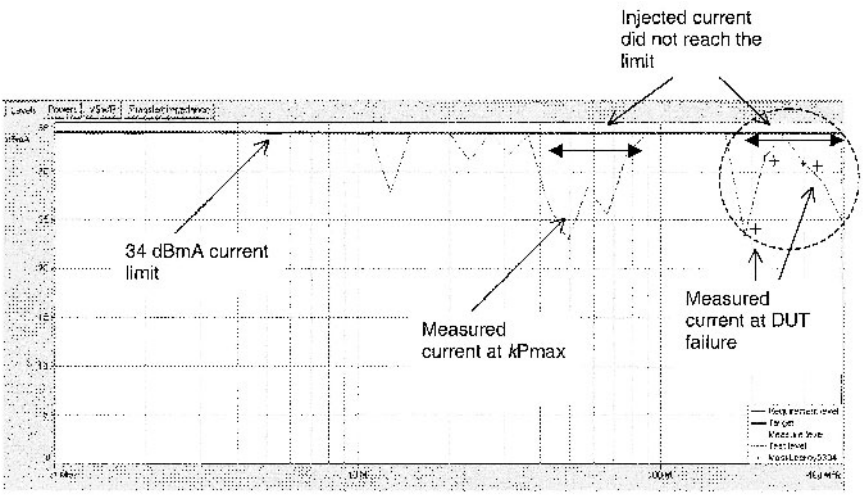

Figure 4-46. BCI current measurement example showing weaknesses around 200 MHz.

This graph should be interpreted with special care, as there is no direct relation between a current level lower than the target limit and the device failure. The injected power is represented in Fig. 4-47. The dotted line corresponds to the calibrated power (power needed to inject 34 dBmA into the calibration setup), the gray curve traces the forward power measured during the BCI test on the bidirectional coupler. In this graph, there is also no direct relation between a power level lower than the target limit and the device failure.

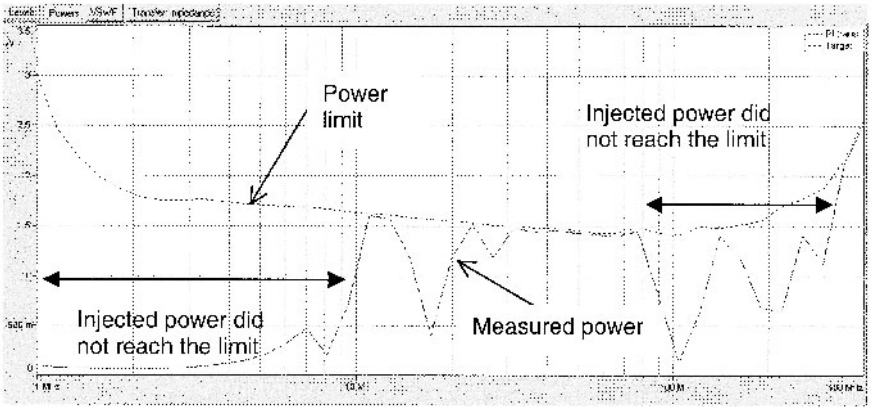

Figure 4-47. Same BCI measurement regarding power.

In the control software setup from *Freescale Semiconductors*, the failure appears in the current curve as black crosses at the corresponding frequency. Below 100 MHz, we can observe than either the current limit (Fig. 4-46) or the power limit (Fig. 4-47) has been reached, without any DUT failure (No cross in this frequency range for Fig. 4-46). The DUT is not susceptible at this frequency range. Near 200 MHz, none of these limits have been reached as the DUT has failed. Consequently, the DUT is not immune from 150 MHz to 350 MHz.

7. DIRECT POWER INJECTION (DPI)

In the case of Direct Power Injection (IEC 62132-4), the RF disturbance is injected on the pin of the component through a decoupling block as shown on Fig. 4-48. Usually the DC block is realized by a capacitor with or without a serial resistor.

The RF disturbance is monitored through the directional coupler by measuring the forward power and the reflected power. To reduce the reflection effects, it is strongly recommended that the setup be built with 50 Ω cable and 50 Ω-adapted printed circuit board tracks, so that the injection path is 50 Ω almost all the way from the RF generator to the DUT. However, the DUT impedance is strongly dependent on frequency, therefore creating reflections and resonant effects. To avoid taking into account the cable effects, an optional attenuator (commonly 3 or 6 dB) may be inserted just before the capacitor, which features a 50 Ω-input impedance.

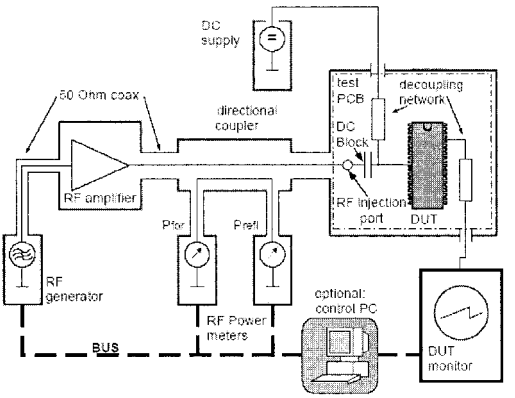

Figure 4-48. Typical Hardware setup for DPI test.

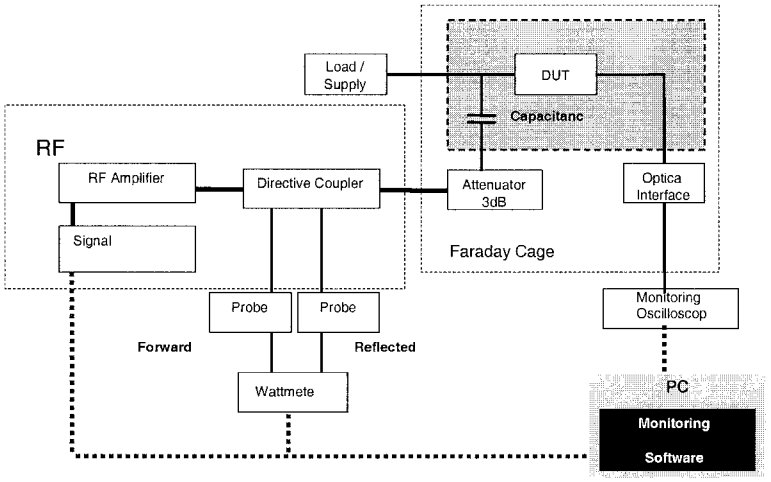

Figure 4-49. DPI measurement setup with attenuator.

Consequently, the injection system including the generator, the amplifier, coupler cable and termination (Fig. 4-49) are 50 Ω-adapted. The mismatching only concerns the small portion of conductor from the attenuator to the capacitor, which can be precisely characterized and modelized.

The path of the RF disturbance is 50 Ω-adapted as far as the coupling capacitor. For measurements to be reproducible, it is highly recommended that the wire between the attenuator and the capacitor be of a fixed length.

Indeed, the coupler and the device input are not 50-Ω adapted and will be the cause of reflections that will depend on the length of the interconnection between the attenuator and the capacitor. It is not necessary to perform the DPI test in a Faraday cage because of the low electromagnetic field radiated by this method.

Commonly the injection capacitor value is between 1 nF and 10 nF. High-voltage capacitor should be used, as the component suffers important electrical overstress. When conducting extensive tests at high injected power levels, the capacitor must be changed frequently be due to rapid degradation of its performances.

In the most recent revision of the standard, the characterization of the injection setup requires measuring the transfer gain (i.e. $[S_{12}]$ parameter) when the DUT is replaced by a 50 Ω port. The ratio between the power delivered by the source and the power delivered to the load maximum should be 0 dB with a maximum tolerance of 3 dB on the whole frequency range.

7.1 Algorithm for the DPI measurement

The measurement algorithm for DPI is simpler than for the BCI (Fig. 4-50) because we only monitor the power injected on the DUT thanks to the directional coupler. The calibration procedure is useful to determine the impedance of the path between the coupler and the DUT and therefore to quantify the exact power received by the DUT.

To reduce the test time, it is often accepted that the first level of power is not fixed to 0, but fixed to P_{limit} – x dBm, where x is the margin in power.

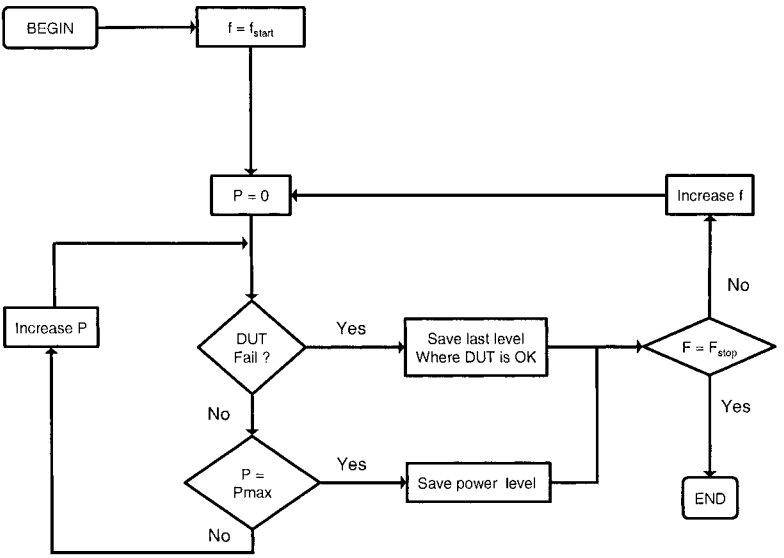

Figure 4-50. Flowchart for DPI measurement.

The DPI flowchart is simpler than the flowchart of the BCI. In this case, for each frequency step, the power is increased up to the power limit given in the customer specification or up to a failure of the device. To reduce the test time, the initial power level at the following frequency could be set for example at 6 dB less than the previous one, therefore reducing the iteration of the power loop.

The RF disturbance signal is a sinusoidal waveform from DC to 1GHz CW or AM (1 KHz with 80% for the modulation factor). The usual power limit is 1 W or 30 dBm. The level could reach 5 W (36 dBm) for specific applications.

7.2 DPI test results

Typical test results for DPI are illustrated in Fig. 4-51. The test was performed on a test vehicle for a LIN interface. The blue curve corresponds to the maximum current injected without creating a failure in the DUT. We can therefore observe that this DUT presents two weaknesses at 10 MHz and 90 MHz.

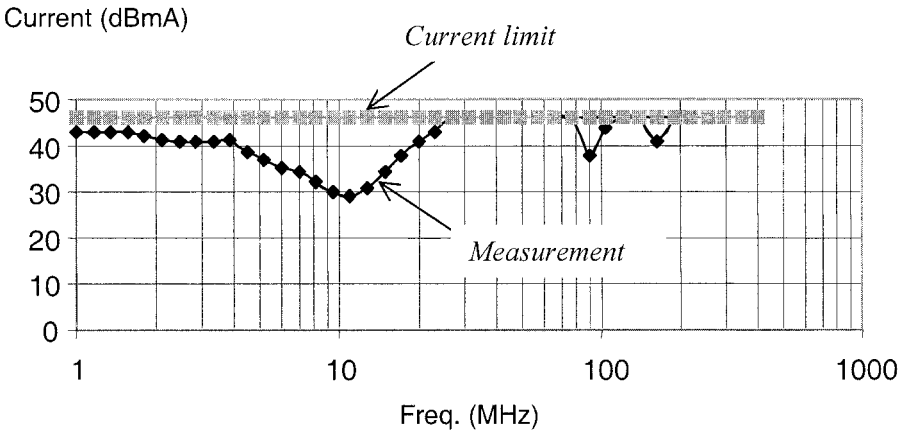

Figure 4-51. Example of DPI result on a LIN interface circuit.

The DPI method is more appropriate for the IC. The difficulty of these methods appears when the number of pin to be tested becomes relatively high. As these tests are costly and time consuming, an alternative may consist to pre-select a reduced set of test pins rather than to test each pin.

8. TRANSIENT IMMUNITY OF INTEGRATED CIRCUITS

This section describes the transient immunity environment and the test methodologies being used or developed to evaluate the transient immunity performance of integrated circuits (ICs). While the transient environments and test methodologies at the product level are well-defined and understood, the equivalent environment and methodology for ICs is undefined.

As a result, work is in progress with the IEC and elsewhere to define a transient immunity environment and test method that is suitable for the evaluation of ICs. Both the application of product level test methods to ICs and the development of emerging IC-specific test methods is discussed.

8.1 Motivation

One reason for investigating IC immunity to impulse waveforms is that the transient immunity tends to decrease (Fig. 4-52) as technology progresses, as observed by Camp (2004). Reasons might be the decreased noise margins, the clock frequency increase or the integrated circuit complexity increase.

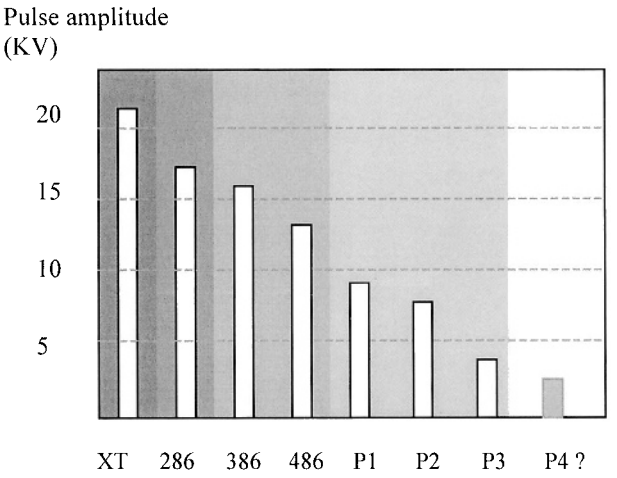

Figure 4-52. Immunity to transients tends to decrease with computer generation (From Camp, 2004).

Several transient noises may be considered at IC level. The most common one is the electrostatic discharge (ESD) that may attain several KV (Kilo-Volt) in a few nanoseconds, with a general shape similar to that of Fig. 4-53.

The ESD may be provoked by human contact to electronic devices, as well as electrical contact with other hardware. An extensive discussion on the ESD modeling is provided in chapter 5. An example of electrical fast transients (EFT), is given in Fig. 4-54, with a rise time of 5 ns and a 5 KHz repetition rate. The input/output interfaces of the integrated circuit contain specific structures which may handle the ESD and EFT pulses, and may dissipate the injected parasitic energy without destroying the component. Some of these structures are discussed by Wang (2002).

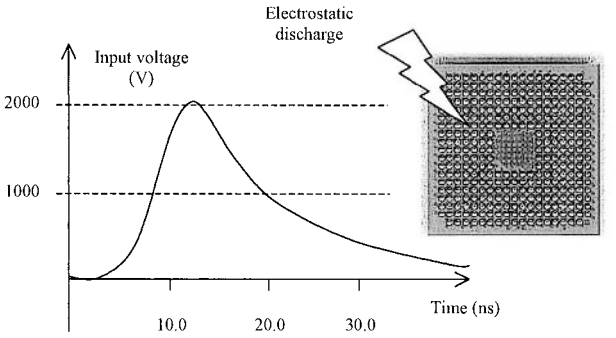

Figure 4-53. Typical aspect of an ESD pulse.

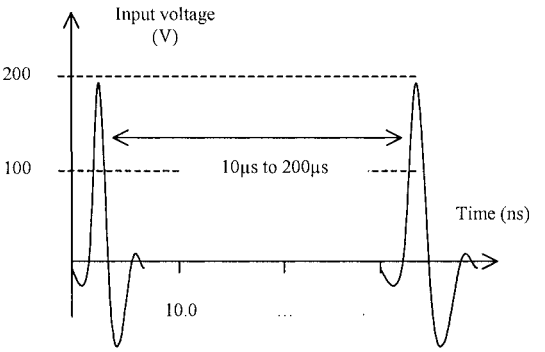

Figure 4-54. Electrical Fast Transient.

8.2 Coupling Path

8.2.1 Effect of Transient Pulse

We consider here the coupling path between the points of application of the transient and the device to be stressed. Either by common impedance, mutual coupling or capacitive coupling, the transient event will propagate toward the possible points of entry: inputs, outputs, peripheral (V_{ssx}) and/or core ground (V_{ssC}), peripheral (V_{ddx}) and/ or core supply (V_{ddC}) or via substrate (V_{ssIS}). The high-pass nature of the coupling path results from the fact that the derivative of the wave-shape is of the utmost importance, as recalled by Eq. (4-11).

$$V_{induced} = L \cdot di/dt \qquad (4\text{-}11)$$

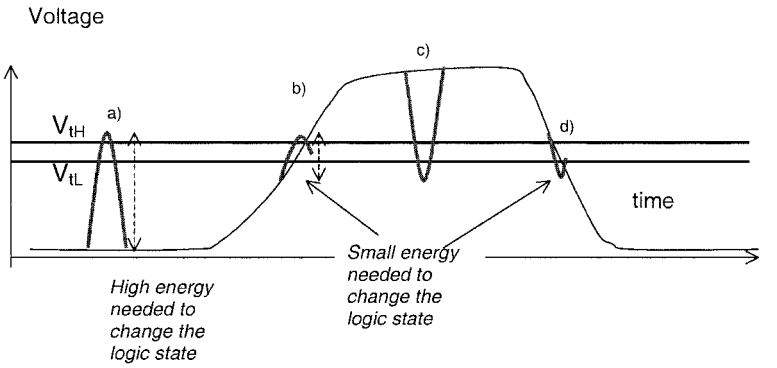

Figure 4-55. The energy needed to alter the logic value is reduced during transitions.

The consequences of the transient on the device operation are illustrated in Fig. 4-55. If the pulse amplitude is high enough, a parasitic glitch appears that alters the signal to an erroneous 1 (Fig. 4-55-a). The symmetrical situation happens in Fig. 4-55-c where an erroneous 0 is provoked by the pulse. An increased sensitivity to transient may also be observed during the normal signal transition (rise edge in Fig. 4-55-b, fall edge in Fig. 4-55-d).

8.3 Transient Immunity environment

The transient immunity environment applicable to electrical and electronic products is currently specified only at the level of the final product. The applicable environment is usually a country-specific legal or regulatory requirement but is often a less formal requirement of the target market. Regardless of the source of the applicable transient immunity environment, it is almost always referenced to an existing international standard.

8.3.1 Product level

The product level transient immunity environment can be divided into three discrete areas: consumer and industrial; automotive; and military and aerospace. This division is driven by the differences in the operational electromagnetic environment for the three discrete application areas.

The characteristics of the electromagnetic environment that influence transient immunity can be found in many national and international standards. For the purpose of this chapter, the focus will be on international standards.

The transient immunity environment for consumer and industrial electrical and electronic products is defined as the electrical fast transient (EFT) as defined in IEC 61000-4-4. The EFT immunity environment for automotive electrical and electronic products is defined ISO 7637-2. These standard test methods are performed by the OEM designer to meet product specifications and regulatory requirements. The military and aerospace environments typically do not define a transient requirement.

8.3.2 Integrated circuit level

For integrated circuits, the transient environment is currently undefined by national or international standards. While environments for products are based on the typical electromagnetic environment for the location of use and, to some extent, the capabilities of the user (home vs. business), the environment for ICs is dictated by the design of the final product. Even for a particular application and environment, the possible implementation choices and their effects on EMC performance make IC level environment standardization impractical. Even so, efforts continue to identify an appropriate IC level transient environment or environments.

In the absence of a reliable IC level transient environment, semiconductor users tend to specify compliance of the IC with the product level environment. While this methodology identifies the worst case environment, these levels are almost never actually seen at the IC pins. Power supply, data filtering and the design of the printed circuit board (PCB) will attenuate the transient levels. As a result, care must be taken when applying product level environments to ICs in order to prevent over-design and unjustified cost.

8.4 Integrated Circuit Test Methods

As in the case of the integrated circuit transient immunity environment, standardized transient immunity test methods for integrated circuits do not yet exist. Work is currently in progress within IEC Technical Committee 47 (TC47) on semiconductors to create a family of transient immunity test methods (IEC 62215) for integrated circuits.

Table 4-6. Proposed standards for integrated circuit impulse immunity measurement

Standard	Description	Stage in 2005
IEC 62215-1	Definitions	New proposal
IEC 62215-2	Impulse immunity method (low voltage)	New proposal
IEC 62215-3	Electrical Fast Transients (EFT), Electrostatic Discharge (ESD) immunity (high voltage)	New proposal

Most of the documents are at the stage of new proposals, as seen in Table 4-6. Until standardized test methodologies are available, semiconductor manufacturers are employing both product level test methods and proprietary, IC-specific test methods.

8.4.1 Application of product test methods to ICs

Product test methods can be used to evaluate IC transient immunity performance provided that the limitations of the applied method are correctly understood. The product test typically applied to an IC is a tailored version of the methods described in IEC 61000-4-4 or in ISO 7637-2. This tailored method is often used by product manufacturers to evaluate the performance of subsystems or modules. As a result, this methodology has the potential benefit of better correlation to the end application than a more application independent test method. Reliable correlation relies on a test setup, hardware configuration, and IC operation that are identical to the end application.

A typical test setup for injecting a fast transient waveform on both the power and signal leads of an IC-specific PCB is shown in Fig. 4-56. The setup employs a standard EFT generator and capacitive coupling clamp (Value from 50 pF to 200 pF) in accordance with the above IEC and ISO standards. The test setup has the following characteristics:

- The ground reference plane (GRP) is a metallic sheet (copper or aluminum) with a minimum thickness of 0.25 mm. The GRP is 1.6 m x 0.8 m in size and is mounted on a non-conductive table 0.8 m in height.
- The test PCB, coupling clamp, and all cables are placed on the GRP and are separated from it by insulating supports having a thickness of 0.1 m. Any PCB loads are bonded directly to the ground plane.
- The EFT generator, coupling/decoupling network (CDN), and PCB loads are mounted directly on the GRP. Each device is bonded to the GRP.
- Signal and/or data cables have a total length of 2 m and are routed through a capacitive coupling clamp. The length of cable between the coupling clamp and either the PCB or load is no more than 0.5 m.
- The AC power cable connected between the CDN and the AC-to-DC power supply of the PCB should have a maximum length of 0.5 m.
- All cables should maintain a 0.1 m separation from the ground plane except when routed though the coupling clamp.
- The minimum distance between the DUT and any other conducting surface, except for the GRP, should be 0.5 m.

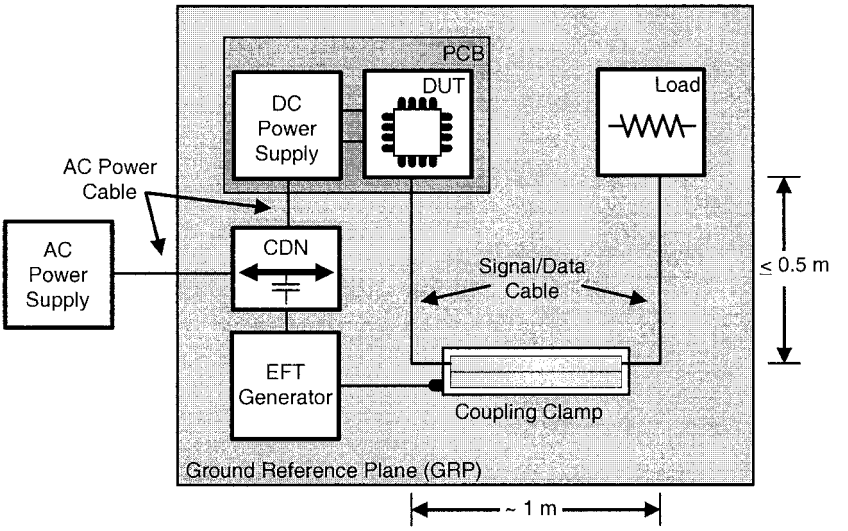

Figure 4-56. PCB EFT test setup, top view (not to scale).

The disturbance signal is typically the same as used for the end product. Reduced transient voltage levels may be used depending on the performance characteristics of the device under test (DUT).

8.4.2 Test Procedure

The generic test procedure for fast transient immunity testing is described by the flowchart shown in Fig. 4-57. The procedure is implemented for each desired transient injection point or location and is valid for ICs, PCBs or end products. After selecting the initial transient polarity and setting the EFT generator to the lowest desired setting, the transient is applied for a period of 60 seconds. The test data, including the immunity performance class as described by the governing standard, is recorded. The appropriate action is then taken based on the last data point: increment the voltage, change the polarity, or end the test.

Note that not all DUT fail conditions require taking the DUT fail path. If the DUT is still operable, the test may continue with higher voltage levels in order to determine the level of the more severe performance classes.

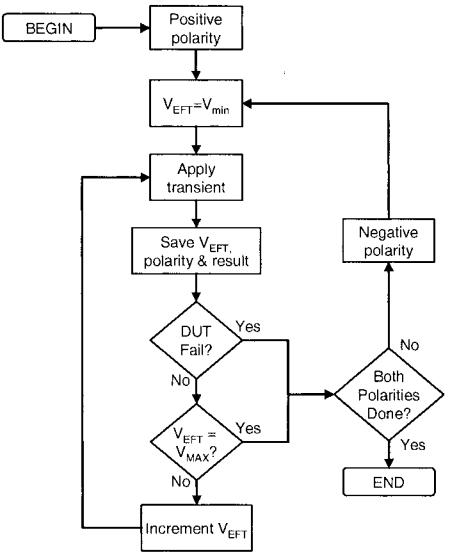

Figure 4-57. Flowchart for fast transient immunity testing.

8.4.3 Failure criteria and monitoring

The failure criteria will vary depending on the IC type, IC functionality, and the impact of the PCB on monitoring and detecting performance degradation. The ability to monitor for the failure criteria will depend on the functionality of the PCB with respect to enabling the detection and reporting of performance degradation.

8.4.4 Test PCB

For this test methodology, the DUT is an IC installed on a PCB with a connected cable harness or harnesses. Options for the PCB include: an actual product PCB, a generic IC demonstration or evaluation PCB, or an application independent PCB for EMC evaluation purposes such as those defined in IEC 61967 (IEC, 2001) or IEC 62132 (IEC, 2003). The choice of PCB type and the resulting test applicability is shown in Table 4-7.

Table 4-7. Test PCB type selection guide

PCB	Application
Product, application specific	Simulate product application performance
Generic, application dependent	Simulate generic application performance
EMC, application independent	Isolate IC performance

Table 4-8. Test PCB type selection guide

Test type	Power supply type
Product, application specific	As in actual application
Generic, application dependent	On PCB recommended. Off PCB allows easy change of power supply impact.
EMC, application independent	Off PCB required.

The IC-specific PCB should either contain its own AC-to-DC power supply or, if not present, a standard AC-to-DC power supply should be provided. The location of the power supply is driven by intent of the test as described in Table 4-8.

8.4.5 Considerations in the application of product level test methods

Using product level transient immunity test methods to evaluate the performance of ICs has real benefits as well as important limitations. Benefits include understanding the impact of PCB and subsystem design choices on IC transient immunity performance, demonstrating IC transient immunity performance in a typical or generic application, illustrating the proper application of EMC techniques, and, if correlation to system EMC performance has been established, optimizing the subsystem design or bill of materials.

The limitations in the application of product level test methods to ICs occur in two mains areas: correlation to system or end product EMC performance; and isolating the EMC performance characteristics of the IC from the PCB and connected power supply and cables. The ease of correlation to product level performance is affected by the similarity of the test setup to the actual application.

With good similarity and sufficient history in designing and testing a particular product type, reasonable correlation can be achieved. The issues associated with such correlation are not discussed herein.

Isolating the IC EMC performance is hindered by many issues. The primary issue is that the actual IC performance is naturally masked by the characteristics of the PCB schematic (including EMI control components and pin loading), PCB layout, and connected cables. Even in the absence of any specific EMI controls, the injected transient immunity test waveform will be modified by parasitic capacitances and inductances by the time it reaches the IC pins.

This leads to the second major issue in isolating IC performance: PCB design differences. PCB layout is critical to IC transient immunity performance. Even for PCBs with the same schematics, seemingly minor differences in layout can result in large variations in measured performance.

As a result, the comparison of data for ICs in different packages is often not practical since different packages require different layouts. This also applies to the comparison of different IC manufacturers unless devices have identical package pinout and functionality. In these cases, PCB differences can be minimized provided that care is taken to produce boards of minimal schematic and layout difference.

In addition, monitoring the injected voltage and current at a single IC pin or all IC pins during a test can be difficult if not impossible. While successful measurements will explicitly describe the susceptibility waveforms, this information has limited usefulness. Reproducing the transients measured at the IC pins of one PCB at the pins of a different IC on a different PCB is not practical.

8.5 Emerging IC test methods

The IEC's TC 47 is in the process of developing a family of transient immunity test methods for integrated circuits. The intent of IC EMC test methods is to extract the EMC performance of the IC without it being unduly affected by the PCB and any connected cables. Isolating the IC EMC performance requires the use of an application independent PCB with sufficient design control to ensure maximum similarity of both the PCB schematic and layout. An example of an application independent EMC PCB is described in both IEC 61967-1 and IEC 62132-1. Other examples can be found in the other parts of these standards.

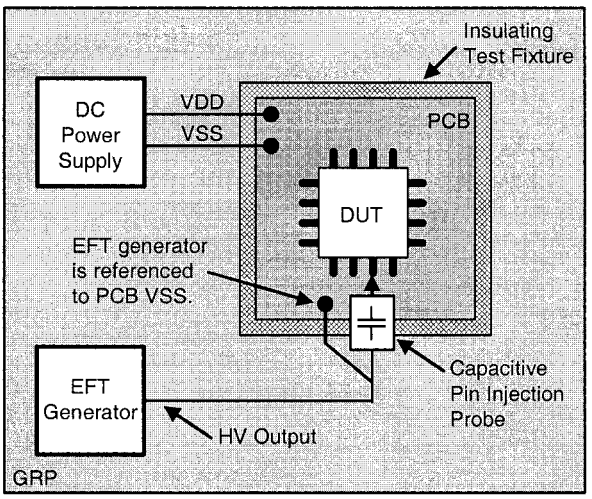

Figure 4-58. Pin injection test setup (top view).

Emerging IC transient immunity test methodologies focus on one of two injection strategies: pin injection, and reference injection. The pin injection strategy couples the output of a transient generator to each individual pin of the IC in turn. The reference injection strategy applies the transient between either a local and remote reference or between different IC ground pins.

8.5.1 Pin injection measurement setup

The pin injection test strategy evaluates the performance of each individual IC pin when subjected to a specified transient waveform. Both positive and negative polarity transients, referenced to IC ground (typically VSS or VEE), are applied. The basic test setup is shown in Figs. 4-58 and 4-59. The test setup shows the DUT installed on a PCB designed in accordance with both IEC 61967-1 and IEC 62132-1. The test setup has the following characteristics:

- The ground reference plane (GRP) is a metallic sheet (copper or aluminum) with a minimum thickness of 0.25 mm. The GRP is 1.6 m x 0.8 m in size and is mounted on a non-conductive table 0.8 m in height.
- The test PCB is separated from the GRP plane by an insulating support having a thickness of 0.1 m.
- The chassis of the EFT generator and power supply are bonded to the ground plane.
- All cables should maintain a 0.1 m separation from the ground plane.
- The minimum distance between the DUT and any other conducting surface, except for the ground plane, should be 0.5 m.
- All connections should be as short as possible.

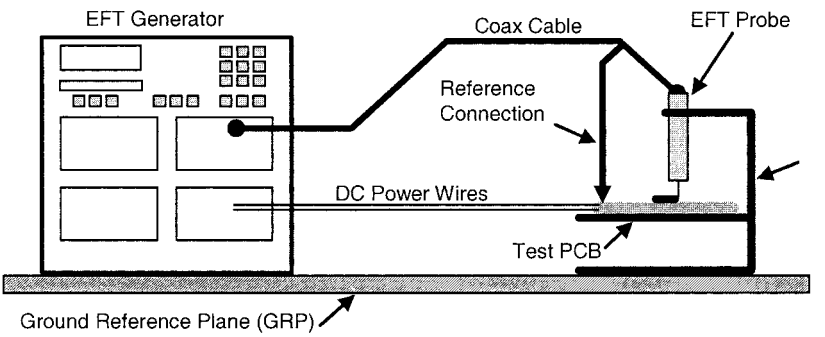

Figure 4-59. Pin injection test setup (side view).

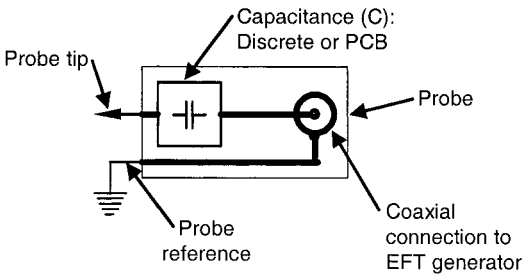

Figure 4-60. Example EFT pin injection probe.

The EFT probe shown in Fig. 4-60 is connected directly to the coaxial high voltage output of the EFT generator. The probe is constructed of a series capacitor and a metallic probe. The value of the series capacitance should be such that it does not significantly load any pin of the DUT. It is recommended that pins be tested in high-impedance or input mode where possible so that the DC blocking capacitance value is not critical to the DUT functionality. For output pins, the DC block capacitance should not exceed 10% of the rated capacitive load to prevent excessive degradation of the output waveform. The DC block capacitor can be realized using discrete components or embedded PCB structures. The test PCB is mounted in a non-conductive fixture that provides stability. The test fixture also provides the ability to position and hold the probe in contact with an individual IC pin or, in the case of a leadless package such as ball grid array (BGA), an individual PCB test point.

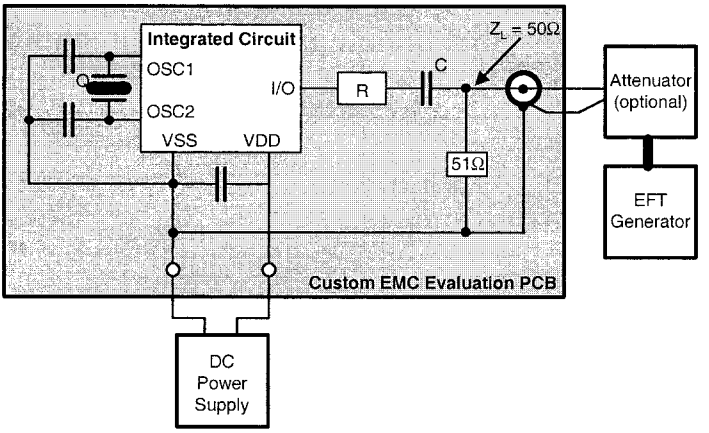

Figure 4-61. Example EFT injection circuit implemented on a PCB.

An alternative implementation of this test method is to integrate the probe capacitance onto the PCB as shown in Fig. 4-61. In this implementation, the coaxial high voltage output of the EFT generator is directly connected to the coaxial adapter on the PCB. The coupling network is identical to that used for RF immunity testing in IEC 62132-4 (IEC, 2003). The resistance (R) is used to limit the injected current, if required. The capacitance (C) is a DC block with a value selected to simulate the desired coupling mechanism as described in Table 4-9.

Table 4-9. DC block capacitor selection

Coupling mechanism	Value of C	Reference
Indirect, Capacitive clamp	50 pF – 200 pF	IEC 61000-4-4
Indirect, Radiated field	6.8 nF	IEC 62132-4
Direct, AC or DC mains	33 nF	IEC 61000-4-4

8.5.2 Reference injection measurement setup

The reference injection test strategy evaluates the performance of the entire IC when subjected to a specified transient waveform. Both positive and negative polarity transients are injected between two locations in the voltage reference. In the conducted emissions measurement methods described in IEC 61967-4, these two locations in the voltage reference are defined as "IC ground" and "peripheral ground." In general, the IC ground is located near the IC and is used as a reference for oscillator components, decoupling capacitors, and other nearby loads.

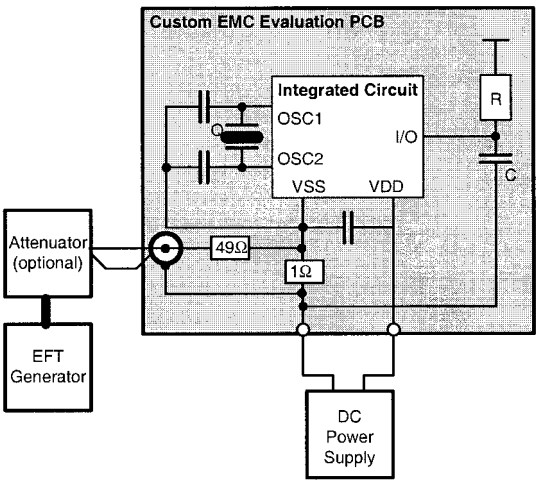

Figure 4-62. Reference injection test setup.

The peripheral ground is remote from the IC and is used as a reference for cables or distant loads. Injecting the transient signal between these two locations will cause current flow in each IC pin connected to the peripheral ground. This test simulates the condition where a transient couples to connected cable bundles.

An alternate use of this method is to inject the transient between VSS pins from different power domains (i.e. – digital VSS and analog VSS). An example of this use has been documented by Fiori (2004).

The basic test setup is shown in Fig. 4-62. The test setup is the same as for the DPI injection method. The test setup shows the DUT installed on a custom EMC evaluation PCB generally designed in accordance with IEC 62132-4 or IEC 61967-4.

8.5.3 Disturbance

The disturbance signal is typically the same as used for the end product. Reduced transient voltage levels may be used depending on the performance characteristics of the device under test (DUT).

8.5.4 Test Procedure

The test procedure will be driven by the functionality of the DUT but is generally similar to the equivalent end product test method.

8.5.5 Failure criteria and monitoring

Once again, the failure criteria will vary depending on the IC type, IC functionality, and the impact of the PCB on monitoring and detecting performance degradation. In the case of application-independent IC EMC evaluation, utilizing a customized IC EMC test board provides the ability to monitor the DUT to produce the most detailed failure description. Using the evaluation of a microcontroller as an example, specialized code and a rigorous microcontroller- or computer-based monitoring system allow the detection and reporting of self-recoverable or "soft" errors in real time. These types of errors can be difficult or impossible to detect in an application or when using only visual indications of susceptibility.

8.5.6 Test PCB

For the pin injection test methodology, the DUT is an IC that can be installed on any type of PCB: an actual product PCB, a generic IC demonstration or evaluation PCB, or an application independent PCB for

EMC evaluation purposes such as those defined in IEC 61967-1 or IEC 62132-1. However, this test method is typically performed using an application independent PCB designed specifically for EMC testing. This type of PCB is used in order to better control the loading of each DUT pin. This results in data that allows more reliability when comparing the performance of different ICs.

For the reference injection test methodology, an application independent PCB designed specifically for EMC testing is required.

8.5.7 Synchronized Impulse Immunity

Testing against impulses is commonly done in a stochastic manner as most EMC-testing related impulse generators (ESD, EFT, etc.) cannot be synchronized or triggered with high accuracy. A series of pulses is applied to a product or device and after that series of pulses it is determined whether the product or device is still working satisfactorily i.e. meeting its expectations.

When a signal level exceeds the specified logic signal condition due to induced impulses, nothing may happen as long as the logic threshold voltage is not exceeded and the duration of the pulse lasts long enough for the logic to react.

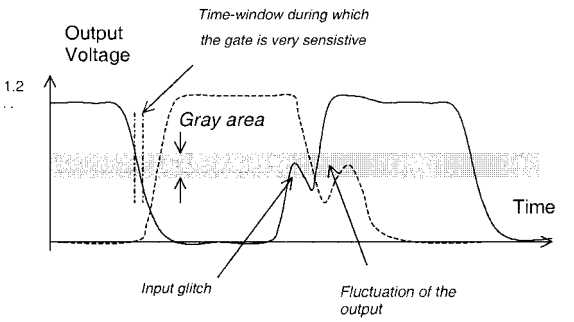

Figure 4-63. A small change in the "gray window" result in a significant change in the output.

With nanometer CMOS technologies featuring a logic gate switching delay in the region of 20 – 50 ps (90nm CMOS), virtually all impulse events may be considered as threats for the integrated circuits. In addition to the above, during a transition of a logic signal, the signal passes the defined logic levels into a grey area where a decision threshold window occurs. In that window, typically less than 100 mV, a change of the input will result in a change of the output of that logic cell, as illustrated in Fig. 4-63.

The equivalent gain of the logic cell in its transition region is very high. Considering a functional signal slope of e.g. 100 ps with a swing of 1.8 V, the time window where the gate is very sensitive to a glitch is around 6 ps. Outside this specific time window, the amplitude needed to induce a logic glitch is very close to $V_{DD}/2$. When the clock is running at 200 MHz (T_{period} = 5 ns), the likelihood of hitting the sensitive up-going transition window will be about 0,1% i.e. 1000 pulses are necessary to hit it statistically only once.

When only 50 impulses are applied to the product (IEC 61000-4-2 requirement) the likelihood of hitting it once at its most sensitive window is unlikely and even when 10000 pulses are applied statistics indicate 10 sensitive occurrences i.e. the lowest disturbance level is found to upset the device. With higher impulse amplitudes, more reactions may have been caused but information about what is caused or when is ultimately lacking.

8.5.7.1 Proposed Approach

To find sensitive time slots in a program cycle, a new impulse immunity test method has been defined by which the impulse is applied to the device in a defined way and at a (pre-) defined moment in time (fully synchronized). The impulse has to be coupled onto the device via various pins; I/O, reset, oscillator, V_{ssx}, V_{ddx} in a defined manner without affecting the functional signal (too much).

A prerequisite is that the program cycle duration with the device to be tested is constant and not determined by any data content. To indicate the completion of a program loop, a dedicated port pin (bit) shall be assigned. The program loop complete toggling bit, together with the device clock and a measurement system available signal will set a trigger condition. With this fixed trigger condition signal, a delay generator is triggered for which a delay can be set from ns to ms with a 10 ps incremental step size. As such, the program cycle can be sliced into 10 ps intervals and at each step, the impulse can be applied (taking into account the systematic delay of the equipment and circuits involved).

From the device under test, the program cycle duration is measured and compared to the duration of a non-disturbed cycle by means of a Time Domain Modulation Analysis (jitter analysis). Due to the induced pulse somewhere during the program cycle, the overall program cycle is affected to become shorter or longer, determined by:

- The polarity of the impulse (+/-).
- The amplitude of the impulse.
- The rise time of the impulse.
- The duration of the impulse.
- The delay i.e. the moment in the program loop i.e. code running.

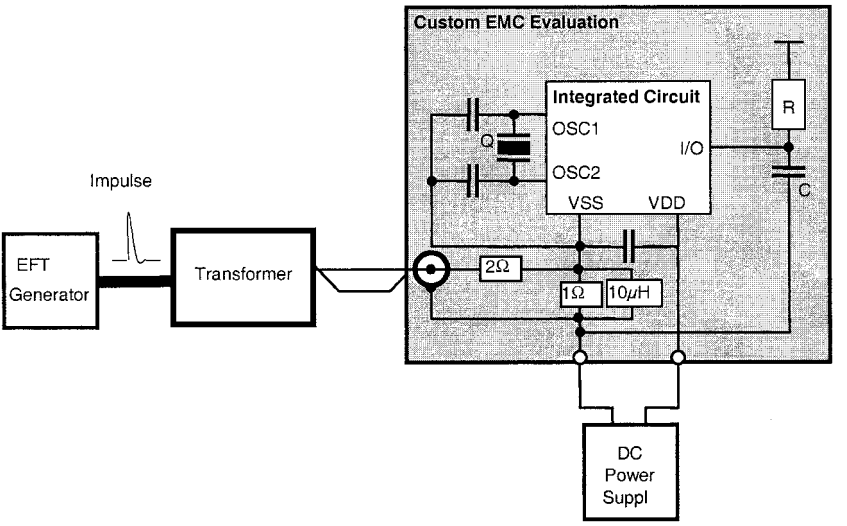

Figure 4-64. Impulse coupling onto the ground pin(s) of an IC.

8.5.7.2 Impulse coupling onto the device

For the coupling onto the supply and ground, a network has been defined which represents a series resistance of 1 Ω in parallel to 10 μH inductor (to by-pass the DC current). As such, hardly any IR-drop (Current-Resistance-drop) results from the coupling network as the impedance of the inductance at DC can be mΩ. Between the 50 Ω generator output and the 1 Ω load an RF transformer is used with a 1:4 ratio to minimize RF losses (Fig. 4-64). In series towards the RF transformer, a 2 Ω resistor is used such that the total load impedance will be 3 Ω.

Together with the RF transformer ratio, a 48 Ω load is presented at the output of the impulse generator. Using this technique has resulted in a broadband coupling network with a bandwidth over 1 GHz (-3dB)[1].

For coupling onto the I/O and other pins, a coupling network shall be used which is functionally transparent, has high directivity towards the pin connected and minimal extra load to that pin. Various attempts have been implemented but ultimately an RF equivalence of the telephone fork circuit has been found most suitable, again with minimal losses. To achieve high directivity, the load condition of the fork has to be made equal to the pin's impedance i.e. the load will be pin-determined.

[1] To benefit from this response, the coupling network has to be placed as close as possible to the relevant pins of the IC

When the fork is used with an input, a signal 40 dB lower is coupled to the input pin rather than to the signal source. Also with an output pin, the same directivity performance can be met. With pins like the oscillator pins, reset input pins, etc. the 1 Ω coupling network can be used in series with the timing capacitor at the reset pin (either to V_{ss} or V_{dd}), the two capacitors to "ground" with a Pierce oscillator application, etc. Again, this coupling measure will not have a significant effect on the functionality.

8.5.7.3 Complexity

With high-density interfaces (HDI) one has to be selective concerning the number of pins chosen to apply the impulses to, as otherwise the total test time would become unacceptably long. With a different core-versus-peripheral supply voltage, all the separate supply and ground pins have to be chosen; minimally 4 or 3.

When the device has one common V_{SS}, the number of pins to inject is reduced from 4 to 3. With I/Os, only a few non-redundant pins shall be selected and only those which are likely to be exposed to external impulses. Other pins, like the oscillator and the reset pin are unlikely to be directly exposed to external impulses but the technique may be applied to investigate the impulse susceptibility of their pins.

Multiplying the number of variables leads to an excessive test time:

- For example 10 pins to be tested.
- Various codes.
- Various impulse conditions.

Most synchronous processors act on the rising edge of the clock. As such, the most susceptible window occurs during the rise time of the clock, with some skew. The rise time window is commonly short compared to the clock cycle e.g. 1:10 or less. Program cycles should be kept short to allow reliable reading with a time domain analyzer as the response "error" that is sought can be only a few ns.

Short series of measurements will already indicate the root cause of the immunity problem: oscillator, PLL, level-shifter, program counter, etc.

8.5.7.4 Results

During the development of the measurement method, various products were tested from simple logic gates to microcontrollers and DSPs. In Fig. 4-65, the jitter is given for a microcontroller. When no impulses are applied or when the pulse is injected before or after the clock edges, the system jitter is of the order of 1 ns.

However in sensitive time windows, the jitter increases to 3 ns, with the amplitude, rise time and impulse duration given here.

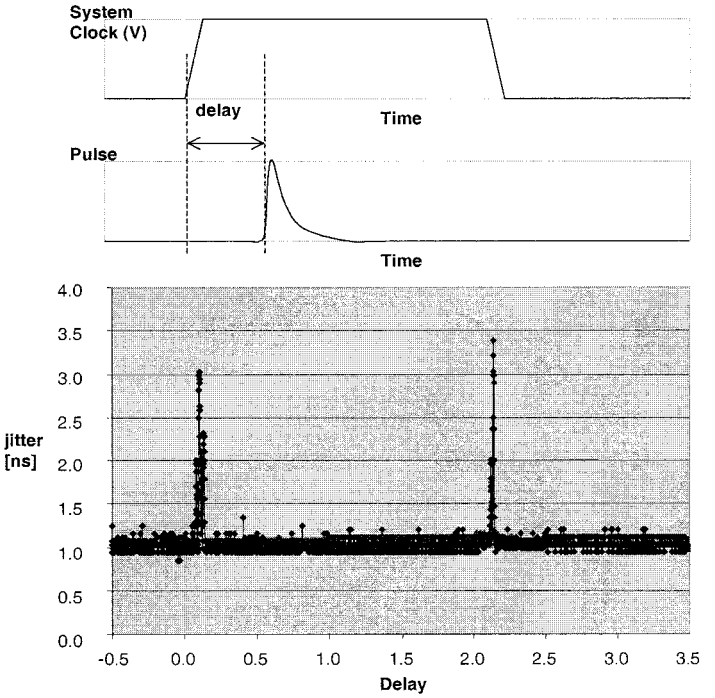

Figure 4-65. Measured jitter vs. impulse delay for a microcontroller.

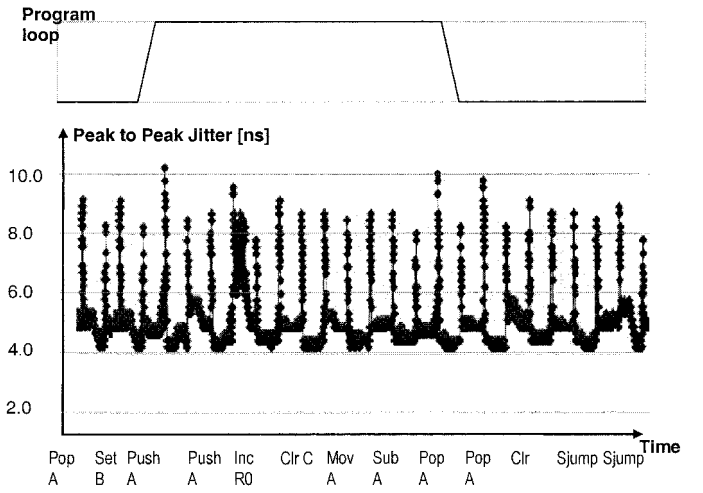

Figure 4-66. TDMA response from a microcontroller as function of the codes running.

In this example, these sensitive windows occur during communication between the core and the peripheral cells while toggling the program loop bit. Using this approach, the most sensitive time windows can be identified and re-used for targeted immunity analysis.

The time slots with high jitter are program-code dependent, as seen in Fig. 4-66. Consequently, the sensitive slots only apply for one specific microcontroller at one specific port, running a fixed set of code instructions. Altering one of these parameters may affect the overall response.

8.6 Discussion

In this section, the fast transient immunity environment and the test methodologies being used or developed to evaluate the transient immunity performance of integrated circuits (ICs) were presented. While every attempt has been made to provide relevant information and guidance, the final form of the standardized IC test method or methods may differ significantly from the information provided herein. In fact, it is expected that work currently in progress by the IEC and others will either refine or diverge from the methods presented in the development of appropriate IC fast transient immunity test methods.

Impulse immunity testing is a time-consuming test methodology. The synchronized approach has the advantage that the exact time window of the program loop where the highest sensitivity occurs can be retrieved.

The coupling method used is applicable to all IC pins as it is supply-current independent. The repeatability of the test method with respect to the detection of the time window and the amount of jitter resulting has proven to be very good.

9. EMISSION AND IMMUNITY TESTS IN ANECHOIC CHAMBER

According to some electronics equipment EMC standards, emission measurement may be carried out taking into account the contribution of far-field radiation coming from electronic circuits. With specific setup arrangements, these measurement approaches may be applied to integrated circuit characterization. This chapter describes the basic ideas beyond far-field emission, possible setup for emission/immunity measurement in anechoic chambers and reverberating chambers.

9.1 Far-field emission from ICs

Generally speaking, far-field emission coming from ICs is due to the combination of radiation of printed board tracks, package lead and bonding, as ICs do not radiate directly except in extremely high frequencies. A typical cross-section of a printed-circuit board is given in Fig. 4-67.

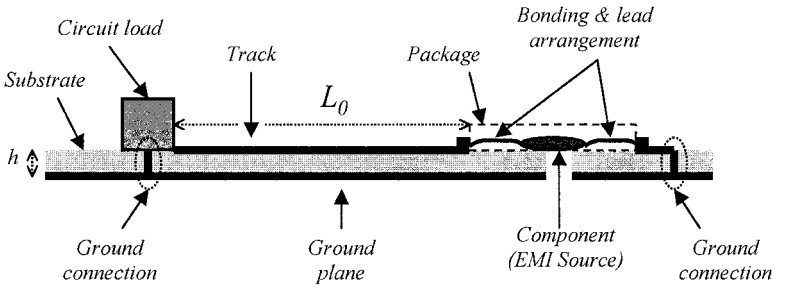

Figure 4-67. Cross-section of a typical printed-circuit board .

Far-field emission depends on the five main parameters: the spectrum figure of the EMI source at component level, the bonding arrangement, the track length, the circuit load and the EMI wavelength. We can distinguish two cases: the low frequency case when the minimum wavelength λ_{min} of interest in the EMI spectrum is much larger than the track length L_0 (Eq. 4-12). In the high frequency case, the minimum wavelength λ_{min} of interest in the EMI spectrum is much smaller than the track length L_0 (Eq. 4-13).

$$\text{Low frequency assumption: } \lambda_{min} >> L_0 \tag{4-12}$$

$$\text{High frequency assumption: } \lambda_{min} << L_0 \tag{4-13}$$

With a wide wavelength compared to the lead and bonding length, emission is mainly due to PCB tracks. According to the low frequency behavior and assigning load values matched with characteristic track impedance, circuit emission is similar either to magnetic or to electric dipoles. Assuming the condition of perfect conductivity and a ground plane of infinite size, we can apply image theory in order to determine the far-field emission of a magnetic dipole with surface equal to $2hL_0$, or an electric dipole with height $2h$ respectively. Radiation is restricted here to a half-infinite free space above the ground plane.

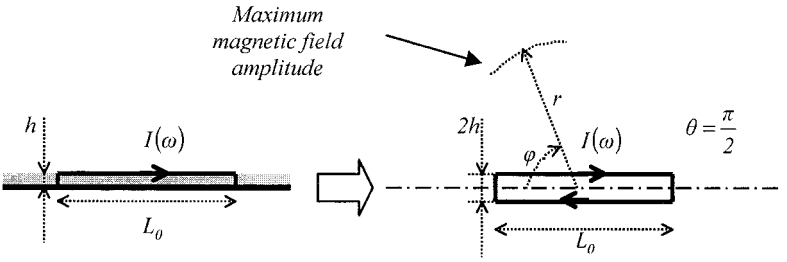

Figure 4-68. Radiation of a current loop.

Considering a current $I(\omega)$ flowing through the loop of length L_0 and height *2h*, the maximum magnetic field is generated on half-circle patterns perpendicular to the ground plane as shown in Fig. 4-68.

Simple formulations exist to compute the E, H contribution in near/far-field conditions, from the elementary current dipole characteristics (See Chapter 3 "Fundamentals and theory").

The IC and PCB under test may be considered as a series of current dipoles with specific space orientation, from which the far EM field may be computed.

9.2 Measurement of electric far-field due to ICs

Far electric field measurement may be carried out by means of the experiment facility shown in Fig. 4-69. The circuit under test is fixed on a rectangular aperture at the outer side of a shielded box.

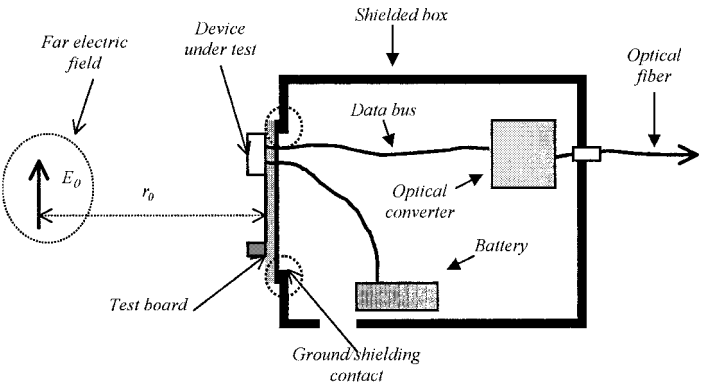

Figure 4-69. Measurement setup applicable at device level

The ground plane of the DUT must be electrically connected to the shielded box all around the test board. A shielded box is used to avoid any parasitic emission coming from the circuit backside. A battery placed inside the box supplies the device under test. The DUT data bus preferably uses optical links with the control test bench to avoid parasitic emission from the cables.

Normally, far-field measurements require that location r_0 of the wide band-receiving antenna must be greater than the wavelength. The typical distance is 1 m to 3 m. The maximum electrical field emission specified by international standards is around 40 dBμV/m (100 μV/m), which corresponds to the sensitivity level of usual broadcasting receivers.

9.3 Emission measurement in anechoic chamber

An anechoic chamber consists of a shielded chamber with electromagnetic absorbing pyramids at the walls and ceiling inner side. Normally, EMC standards do not require absorbing material in the ground plane area. In that case the chamber is called "semi-anechoic". As illustrated in Fig. 4-70, the device under test stands on a moving plate situated at a height *h0* above the ground, and distance *d0* from the antenna. The plate moves the DUT in order to determine the angle for peak emission.

Pyramidal absorbers avoid any reflection on chamber walls, thus reproducing propagation conditions similar to those obtained in free space. However, the absorbers exhibit a low cut-off frequency governed by the size and characteristics of absorbing pyramids, which is typically 100 MHz.

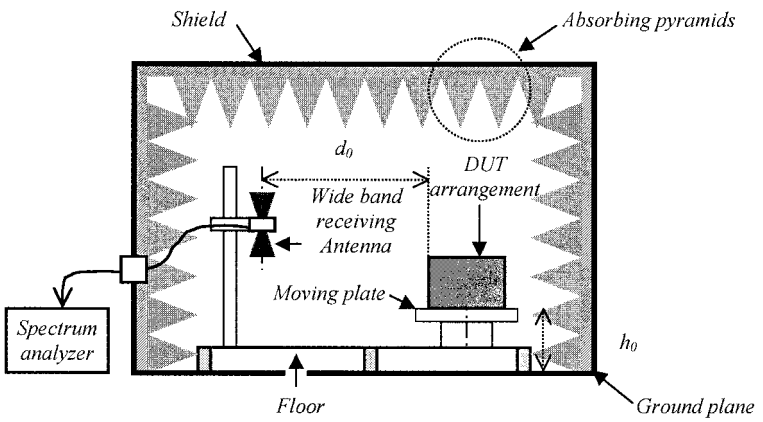

Figure 4-70. Setup for device emission measurement in anechoic chamber.

The distance *d0* between DUT and the antenna depends on the size of the chamber, with a typical value of 1 meter for integrated circuits. The measurement may be performed with a log antenna (dipole array) between 300 MHz and 1 GHz and with a double ridge horn antenna between 1 GHz and 10 GHz, according to (CISPR, 2002)

9.4 Radiation immunity test on ICs

Let us consider a test board submitted to an electromagnetic wave (Fig. 4-70). The coupling effects at board and IC levels are governed by the coupled line theory as summarized in Fig. 4-71. An incoming electromagnetic field at track level is due to the interaction between the plane wave and the shielded box itself.

The resulting normal electric field E_n^r and tangential magnetic field H_t^r components induce a parasitic current represented by a source I_0 and a parasitic voltage represented by the voltage source E_0.

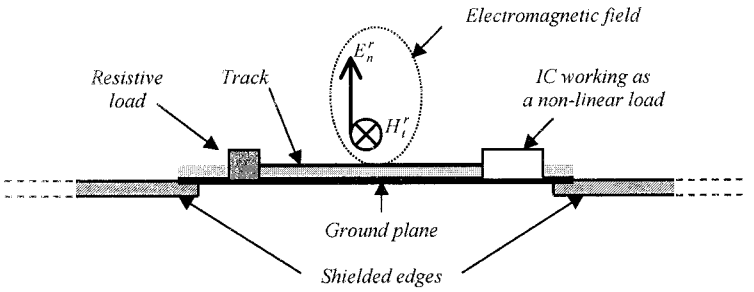

Figure 4-71. Test board illuminated by an electromagnetic wave.

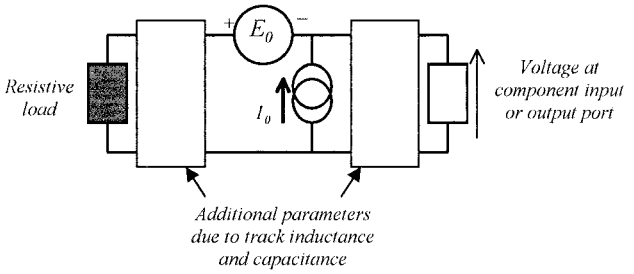

Figure 4-72. The incident EM field induces a parasitic current and voltage on the PCB track.

Assuming sine wave excitation and a wavelength much larger than the physical dimensions of the tracks, the voltage and current sources may related to the incident electromagnetic field with the following equations:

$$E_0 = j\omega\mu_0 H_t^r L_0 h \tag{4-14}$$

$$I_0 = j\omega C_0 E_n^r L_0 h \tag{4-15}$$

In Eq. (4-15), C_0 corresponds to per-unit-length capacitance of the track, *L0* the track length, and *h* the oxide thickness between the conductor and the ground. Equations (4-14) and (4-15) show that coupling strength increases with the frequency.

At high frequencies, coupling is enhanced by resonance phenomena, especially when the load at the left end of the track behaves as a short circuit. Furthermore, the resulting electromagnetic field depends on the plane wave incidence and polarization, and the formulation for *E0* and *I0* cannot be expressed in a simple way.

9.5 Immunity test in anechoic chamber

Faults at IC level usually appear when the incoming electric field rises from 10 V/m to 1000 V/m. Extensive susceptibility measurement published by Hoad (2004) have shown that the field amplitude needed to provoke failure in personal computer motherboards was increased with frequency from 1 to 10 GHz (Fig. 4-73). Worth of interest, the new generations of PCB were significantly less susceptible than older versions.

Very high field levels are very difficult to obtain in open space. Furthermore, such emission levels are prohibited by international regulations, due to significant interference with radio-communications. This context involves performing radiated immunity tests inside a shielded room with absorbing walls in order to obtain propagation like that provided in free space. Fig. 4-74 shows an anechoic chamber facility used to perform this type of experiment.

A high power radio-frequency source placed outside the chamber feeds a wide frequency-band transmitting antenna placed inside the shielded volume. Usually, the distance r_0 between this antenna and the DUT ranges between 1 to 3 meters.

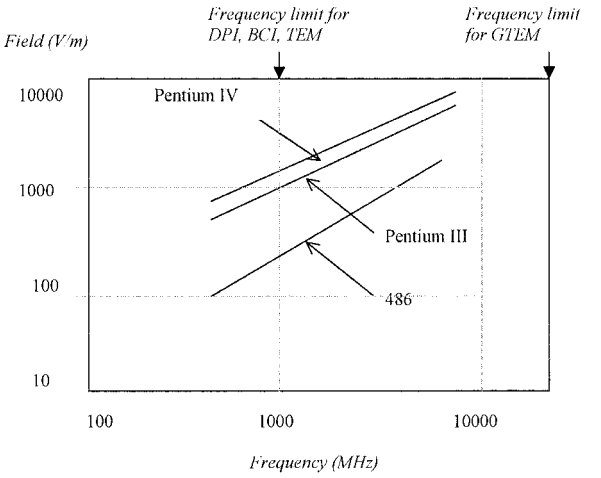

Figure 4-73. Susceptibility trends with interference frequency (Hoad, 2004).

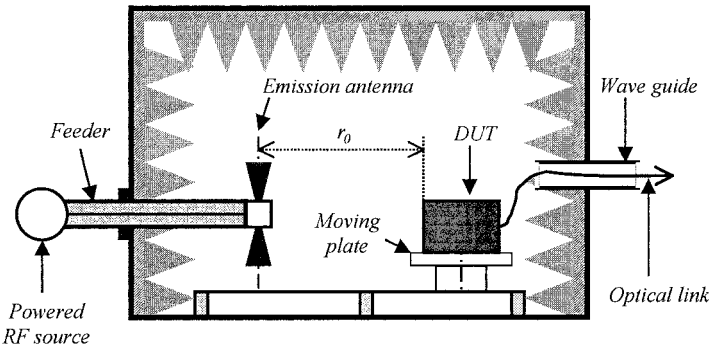

Figure 4-74. Cross-section of an anechoic chamber.

The normal or faulty signal issuing from the DUT is observed by means of an optical link between the output port of the DUT and the measurement equipments located outside the room.

The testing procedure as described in the EMC standard requires two-step, one for field calibration and the other for the test itself. Field calibration without the DUT consists in adjusting the RF power in order to obtain the expected electric field amplitude in the DUT area. The electric field is measured by means of a sensor at a few locations recorded within specified areas close to the DUT. EMC standards recommend that the field deviation should not exceed 6 dB around the average amplitude.

The test is then performed on the device. For each given frequency, the DUT is moved using a rotating plate in order to check for any possible fault. If no fault is detected in all possible orientations, the RF power is increased until a fault is provoked, or the power limit is attained.

To explore the whole radiation pattern, the DUT must be mounted on the top and on one side of the shielded box. Immunity measurements in anechoic chambers are time-consuming and may require very powerful sources. Power amplifiers between 100 W and 1000 W are usually needed to investigate integrated circuit immunity to radio-frequencies.

9.6 Immunity and emission tests in reverberation chamber

The use of mode stirred reverberating chamber may be extended to immunity and emission tests on integrated circuits. A reverberation chamber works like an oversized electromagnetic cavity, and consists of a shielded chamber with highly conductive walls without absorbing material. Assuming a perfectly rectangular cavity with dimension a, b, d, such a cavity produces electromagnetic field resonance at frequencies f_{mnp} predicted by Eq. (4-16):

$$f_{mnp} = \frac{c}{2}\sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2 + \left(\frac{n}{d}\right)^2} \tag{4-16}$$

In this expression, c corresponds to the speed of light in vacuum, while the integer parameters m, n, p, characterize the resonance modes. When excited at their corresponding frequency, standing waves merge within the cavity and the field behaves as a sinusoidal wave distribution. When the wavelength is much smaller than the chamber's dimensions, many wave reflections occur on the walls and the radiation pattern of the field inside some parts of the chamber becomes isotropic.

However, in order to obtain a uniform electromagnetic field with a random distribution, a stirrer with high conductive paddles is moved in the room at an appropriate location. Fig. 4-75 shows a few of the details of the configuration of the reverberating chamber for immunity test on ICs. To avoid direct coupling to the DUT, the exciting antenna is oriented toward a corner of the shielded room.

As previously mentioned, the test board is mounted on a shielded box and placed on a table a few wavelengths away from the walls and the ground floor conductive plane.

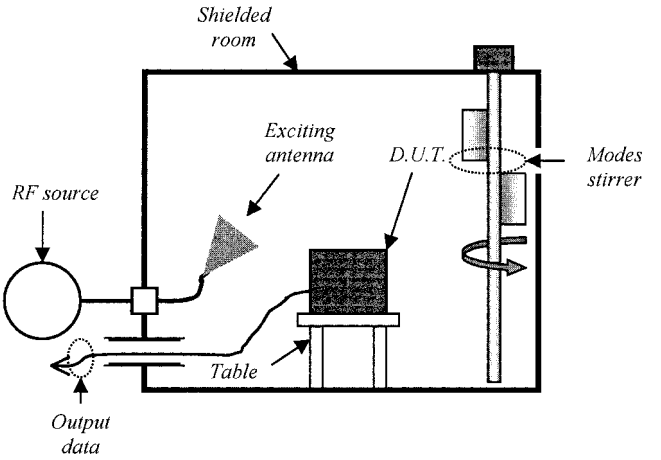

Figure 4-75. Mode-stirred reverberating chamber.

A battery inside the shield box supplies the IC, while the output data is sent outside the chamber through an optical link.

The immunity test is conducted as follows: for each given frequency, the power at the transmitting antenna is adjusted according to the calibration. When moving the stirrer up 360°, amplitude and polarization at DUT location change randomly. The stirrer rotating speed is usually slow (Around 1 turn/second). Higher rotating speeds may shorten the test procedure as the probability of exposing the DUT to the worst case conditions may be increased.

The calibration procedure consists in measuring electrical field amplitude with a small 3D electric probe. Nine points representing the corners and center of a rectangular shaped volume within the room produce data for 27 fields with amplitude uncertainty linked to the position of the stirrer. The standard deviation of the collected data must be within a 3 dB deviation.

It should be noticed that immunity tests carried out in a reverberation chamber produce field strength amplitude reaching 100 V/m or more with reduced incident power at the transmitting antenna (between 1 and 10 W). The reason for this field efficiency is the high quality factor as a consequence of multiple field resonance effects in the cavity.

Emission measurement may also be performed in a reverberation chamber. In this case, radiated field amplitude is deduced from the power collected at the receiving antenna. Experiment facilities are similar to those presented previously, except that a spectrum analyzer replaces the power amplifier, and holds the maximum field amplitude, as the stirrer is moving.

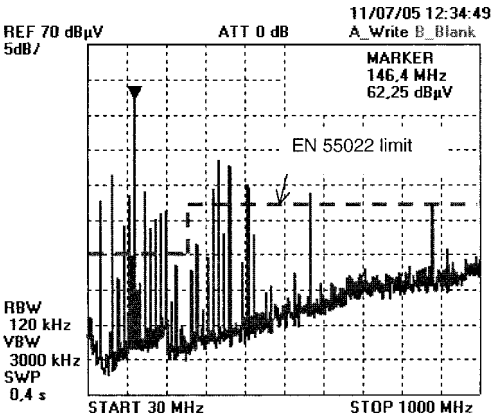

Figure 4-76. Stirred mode chamber used to measure radiated emission of a clock device.

The emission tests presented in Fig. 4-76 concern a digital clock mounted on a small PCB. The DUT was placed inside the anechoic room on a rotating table, one meter above the ground plane. Receiving wide-band antenna was stand at a 3-meter distance from the DUT. A biconical antenna was used for frequency within 30 to 300 MHz, and a log-periodic antenna covered the frequencies 300 MHz to 1 GHz. The measured spectrum do not comply with the EN 55022 standard which fixes the emission limit to 40 dBµV/m from 30 MHz to 230 MHz.

Susceptibility measurements reported in Fig. 4-77 were obtained as follow: for each frequency, power at transmitting antenna was increasing until reaching a fault at the output of the digital circuit under test. The observed error was an erroneous change of the logical state. The electric field amplitude corresponding to the triggering of a fault was put on the vertical axis of the graph. In the figure, the solid line corresponds to susceptibility level recorded in anechoic room within frequency range 450 MHz to 1 GHz, while the doted line is deduced from test performed in modes stirred reverberation chamber with stirrer full rotation. These curves show similar shape: the most critical susceptibility occurs at frequency close to 500 MHz which fits with the resonance of PCB tracks connected at the IC inputs. Above 500 MHz, improved immunity may be explained by the combination of propagation phenomena on PCB tracks with respect to the wavelength, and filtering effects due to parasitic capacitance at package and circuit level.

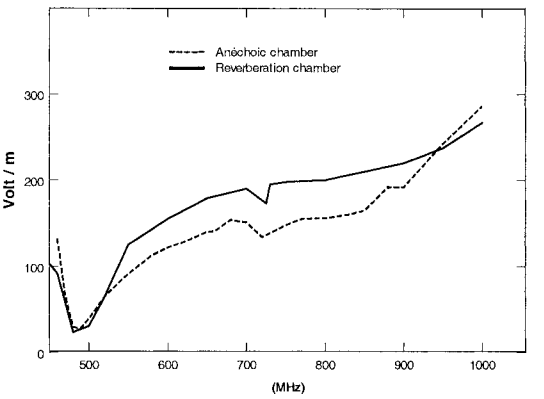

Figure 4-77. Logic circuit susceptibility to RF interference in anechoic and reverberating chambers.

9.7 Discussion

Characterization of ICs in terms of far-field emission and radiated immunity may be carried out using anechoic chambers in order to determine the electromagnetic field as would be found in free space. However, anechoic chambers require costly equipments that must include absorbing materials and wide frequency-range power amplifiers. An alternative way consists in using a reverberation chamber which may significantly reduce the amplifier cost. Similar experimental results have been obtained in anechoic or mode stirred chamber, both from and emission and susceptibility point of view.

10. ON-CHIP MEASUREMENT

Different on-chip techniques may be used to characterize EMC noise sources within ICs, which may give valuable information on the current peak amplitude, flow within the power network and coupling to other parts of the integrated circuit. In the past few years, there has been a strong interest in finding alternatives to complex, expensive and inaccurate off-chip measurements, by measuring internal signals with non-invasive on-chip methods featuring time-domain accuracy the order of a few pico-seconds (ps).

Soumyanath (1999) proposed a non-intrusive time-domain method, based on a rail-to-rail comparator. The calibration required a complex external setup with limited timing resolution. Makie-Fukuda (1996) proposed a method based on voltage-comparator, from which the noise amplitude and rms voltage could be extracted. As MOS transistors have a maximum operating frequency above 30GHz in deep submicron technology, on-chip oscilloscopes for sampling very high bandwidth signals can be designed (Zheng, 2003; Vrignon, 2005), which give valuable information on the internal current flow and from which the parasitic emission of the entire circuit may be derived.

10.1 On-chip Oscilloscope

One of the most efficient approaches is based on an on-chip sample-and-hold circuit that directly probes the voltage fluctuation at a location within the circuit. The schematic diagram of the sampling sensor is reported in the Fig. 4-78. An external signal *Synchro* is used to trigger the parasitic phenomenon, which is sampled, amplified and exported off-chip.

The sampling cycle is repeated for varying delays, externally controlled by *Vanalog*, until the waveform is reconstructed, just as a sampling oscilloscope would do.

The targeted phenomenon is a core switching, which induces a power supply line fluctuation on both the V_{DD} and V_{SS} interconnects. Four probes sample the voltage at both ends of two resistors R_{VDD} and R_{VSS} in series on the supply lines. The resistors have small values to limit the voltage drop that would influence the current measurements. The current is extracted from the voltage drop over the shunt resistors R_{DD} and R_{SS}.

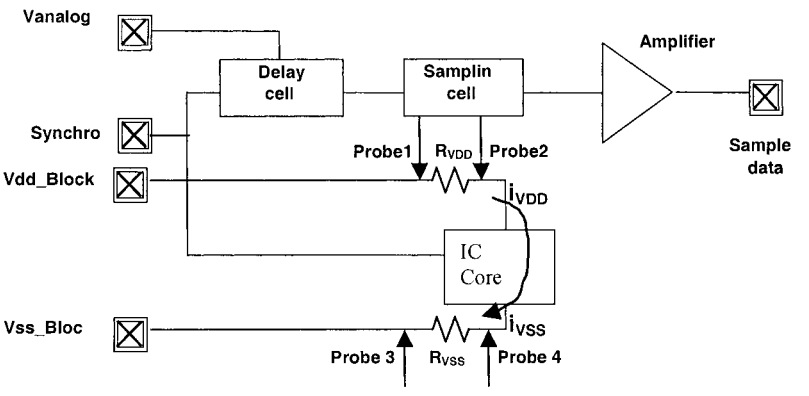

Figure 4-78. Principles of the on-chip sampling of core current.

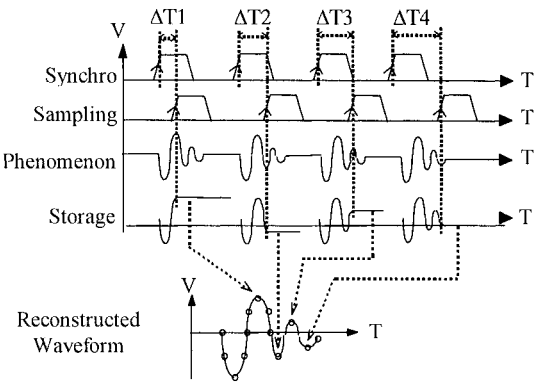

Figure 4-79. Reconstruction of the original current waveform.

The probing sequence is detailed in Fig. 4-79. Each time the *Synchro* signal rises, a current peak appears which creates fluctuations on the supply lines. Concurrently, the sampling signal is delayed by Δt_i. This delay is linearly dependent on the externally controlled voltage *Vanalog*. At the active edge of *sampling*, the voltage value is sampled and stored in a small capacitor that acts as an analog memory for several hundred nanoseconds. The captured analog signal is copied by the follower that regenerates the signal to an external analog-to-digital converter.

The repetition of this procedure for a set of different values of *Vanalog* leads to a reconstruction of the fluctuation, within the limits of frequency and temporal resolution of the sensor.

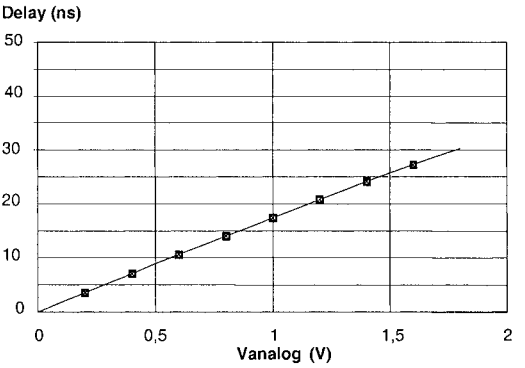

Figure 4-80. Delay cell characterization vs. *Vanalog* voltage control.

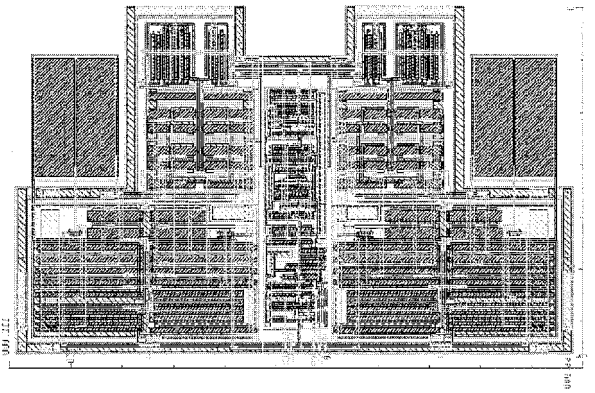

Figure 4-81. Implementation of an on-chip sampling oscilloscope.

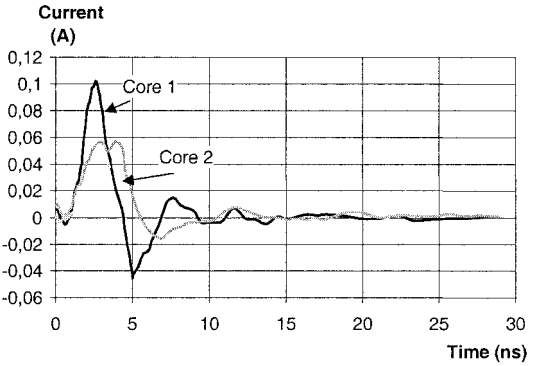

Figure 4-82. On-chip sampling of the core current on VDD supply lines.

Fig. 4-80 shows the delay dependence versus *Vanalog* for the on-chip sampling delay cell, featuring a good linearity. Fig. 4-81 shows the layout of the 4-probe sampling sensor in 0.18µm CMOS technology. The 4 samplers and the source-follower amplifier layouts fit in a silicon surface of 600µm^2. Fig. 4-82 demonstrates the use of the on-chip sensor for the measurement of current flow during active clock edges on a logic core. The current peak corresponds to the synchronous switching of around 10,000 inverters and logic gates.

The V_{DD} line supplies a 2.5 V voltage. The current generates a fluctuation of the long line due to a combination of resistive, capacitive and inductive effects. A damped oscillation can be noticed, which indicates the presence of an inductance effect.

In the first 3 nanoseconds, a current up to 100 mA is observed in the case of a standard logic core (Core 1). The current is reduced to 60 mA for the same core with on-chip decoupling capacitance (Core 2).

Table 4-10. On-chip sampling performances vs. technology

Techno-logy	Band-width	Observability	Voltage resolution	Time resolution	Sensor size
0.7 µm	4 GHz	1 ns to 30 ns	5 mV	5 ps	10^4 µm^2
0.35 µm	8 GHz	1 ns to 100 ns	5 mV	5 ps	2500 µm^2
0.18 µm	10 GHz	1 ns to 300 ns	5 mV	5 ps	600 µm^2
90 nm	14 GHz	1 ns to 500 ns	5 mV	5 ps	400 µm^2

The system performances improve with technology scale-down, in terms of bandwidth and precision (Table 4-10). Silicon area also decreases with progress in integration. Furthermore, the system can be easily adapted to any CMOS technology. In 0.18µm CMOS process, the system featured a 20 GHz bandwidth and a resolution close to 5 mV, well suited to internal core current characterization, as well as substrate noise evaluation.

11. EMC TEST PLAN FOR INTEGRATED CIRCUITS

Still very rare some years ago, EMC specifications have become common elements of global IC specifications submitted by electronic system designers to IC manufacturers. The EMC specification usually covers parasitic emission and immunity levels that the component should comply to. Most EMC specifications are based on international standards such as IEC 61967 and IEC 62132. These specifications recommend methods to be used and give the associated required levels for meeting EMC automotive requirements. These generic specifications may not be fully applicable to any given component. In that case, a detailed conditions test and test setup are described in an additional specific document named Integrated Circuit EMC Test Plan.

11.1 Standard Emission Levels

A detailed classification of emission levels is part of the IEC 61967-4 standard, which applies for conducted noise measurement. The overall envelope of the spectrum must remain lower than a specified limit, such as the one shown in Fig. 4-83. Up to three different slope families of emission amplitudes have been specified: a 0 dB per decade amplitude line [A=84 dBµV, B=78 dBµV, etc.], a slope at –20 dB per decade defined by numbers ("1" crosses 1MHz at 120 dBµV, "10" crosses 1 MHz at 60 dBµV, "20" crosses 1 MHz at 0 dBµV), and a slope at –40 dB per decade.

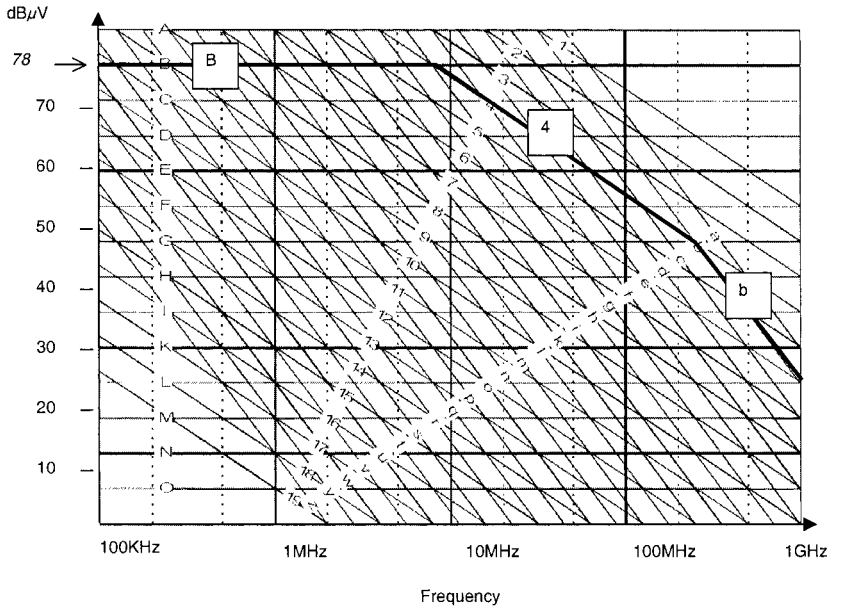

Figure 4-83. Slopes for emission envelope as defined in IEC 61967-4.

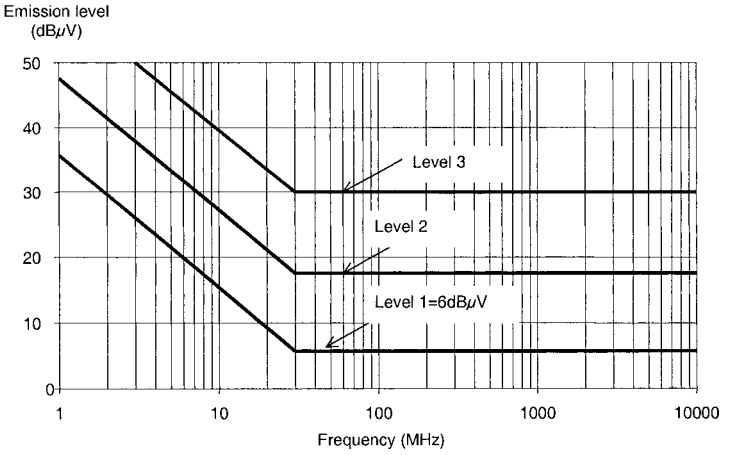

Figure 4-84. IC conducted emission levels specified for automotive applications.

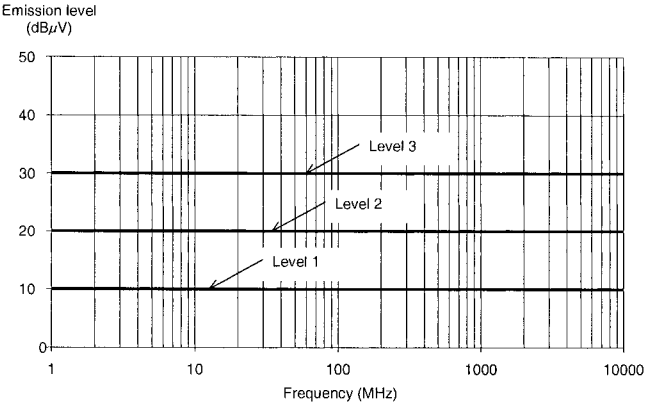

Figure 4-85. Maximum emission levels specified in TEM cell.

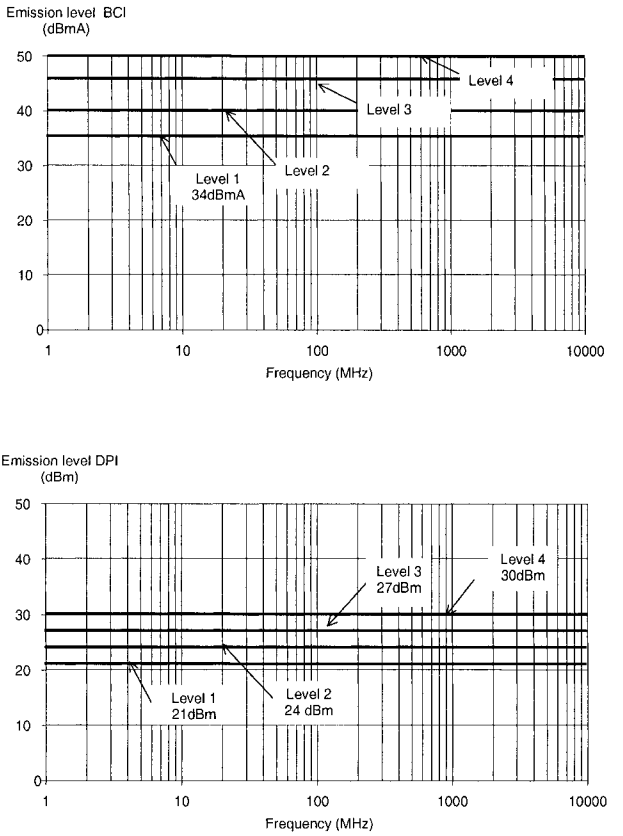

Figure 4-86. IC susceptibility levels using BCI (up) and DPI method (down).

The vertical distance between each slope is 6 dB. The maximum emission level is usually specified by the IC customer, and may be described with one, two or three slopes depending on the application and requirements. Accordingly, the emission level can consist of up to three digits, such as "B4b" in Fig. 4-83. Each digit represents one of the slopes illustrated in the figure. Theses maximum emission levels are a standardized way of communicating maximum emission levels unambiguously. Emission limits given in some specification for automotive applications (Marot, 2004) are presented in the following way (Fig. 4-84). Level 1 corresponding to a very low level of 6 dBμV is required for low cost application with minimum on-board decoupling capacitance, and usually for 2-layer printed circuits.

Automotive equipment manufacturers design low-cost electronic boards using ICs that must comply with radiated noise limitations as low as 10 dBμV (Level 1 in Fig. 4-85). However, most 16-bit ICs exhibit 20-30 dBμV peak noise in TEM cell, which require further on-board filtering and decoupling.

11.2 Immunity Levels

The bulk-current-injection (BCI) standard defines a method for measuring the IC immunity via inductive coupling. Disturbances are induced on wires via a magnetic probe. Limits are given in dBmA, as detailed in Fig. 4-86. A level of 46 dBmA in BCI is usually required for low-cost automotive applications (Marot, 2005). The DPI standard defines a method for measuring the IC immunity via capacitive coupling. Limits proposed in EMC specifications are provided in dBm (dB milli-watt) scale, as illustrated in Fig. 4-86. An immunity level of 30 dBmA is often required for ICs to be mounted in low-cost embedded electronics for automotive applications.

12. DISCUSSION AND CONCLUSION

The main characteristics of the standardized emission measurement methods are listed in Table 4-11. All measurement methods are applicable from 150 KHz to 1 GHz, except the GTEM cell method that can extend the upper frequency to 18 GHz. The TEM/GTEM cell approach relies on a specific board with severe constraints concerning the dimensions, layers and placement of the DUT and its external components. The other methods require much less specific boards, like the 1/150 Ω method that requires discrete components and SMA connectors, or the WBFC method for which the test board can be placed in the measurement chamber just as it is.

Table 4-11. Comparison between emission measurement methods

Item	IEC 61967-2 TEM/GTEM	IEC 61967-3 1/150Ω	IEC 61967-5 WBFC	IEC 61967-6 Magnetic Probe
Frequency range	150 KHz-1/18 GHz	150 KHz-1 GHz	150 KHz-1 GHz	150 KHz-1 GHz
Measurement	E/H from IC	Differential and common-mode emission	Common-mode conducted emission	Differential and common-mode emission
Single pin measurement	No	Yes	No	Yes
Test board	Specific, constraints	Added R,C, SMA connectors	Application board	Long tracks

As for the emission methods, the target frequency range for all these proposals is 150 KHz-1 GHz, except for the GTEM cell that may create incident fields up to 18 GHz. The BCI method generates parasitic current on cables that are directly connected to the DUT.

This method is an adapted version of the BCI standard for characterizing equipment susceptibility. The DPI method injects parasitic over-voltage as close as possible to the IC pin by capacitor coupling. As the IC input impedance is not 50 Ω-adapted, the main drawback of the method is the cable resonance and the needs to make the distinction between the forward, reflected and transmitted RF power.

Table 4-12. Comparison between susceptibility measurement methods

Item	IEC 62132-2 TEM	IEC 62132-3 BCI	IEC 62132-4 DPI	IEC 62132-5 WBFC
Frequency range	150 KHz-1/18 GHz	150 KHz-1 GHz	150 KHz-1 GHz	150 KHz-1 GHz
Injection mechanism	E/H illuminating the IC	Parasitic current on cables connected to the IC	Parasitic over-voltage injected on an IC pin through a capacitor	Power injected on an IC pin through a wire loaded with 100 Ω
Single pin measurement	No	Yes	No	Yes
Test board	Specific constraints	Cables connected to the DUT	R,C, SMA con. for each injection point	Application board

The WBFC approach consists in injecting power on an IC pin through a wire loaded with 100 Ω, an approach which features some similarities to both BCI and DPI methods. Novel measurement methods have recently been proposed which deal with impulse immunity to electrostatic discharge, electrical fast transients and electrical overstress. These methods are strongly supported by consumer electronics manufacturers and automotive equipment designers.

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Chapter 5

EMC MODELING

An overview of emission and immunity phenomena modeling in ICs

Abstract: This chapter deals with the modeling of parasitic effects and EMC phenomena in integrated circuits. Phenomena such as electrostatic discharge and internal current activity are described first. PCB and package models are provided. An overview of models dealing with emissions (such as ICEM, IBIS, IMIC and LECCS) and with immunity is presented.

Key words: Crosstalk; Electrostatic Discharge; HBM; emission; immunity; ICEM; IMIC; LECCS; IBIS; VHDL-AMS; I/Os; PCB; package; TEM Cell; near field

1. ELECTROSTATIC DISCHARGE MODELS

1.1 Introduction

This section provides an overview of the most important ESD test models and standards. The ESD test methods, which are described in several standards, are based on different models like the Human Body Model, the Machine Model, the Charged Device Model, and the Transmission Line Pulse Model. These models were developed to reproduce most of the different failure signatures of integrated circuits, which are caused by ESD stress.

Everybody knows the shocking sparks that leap from one's fingertip when touching a doorknob or the door handle of a car. The lightning you can see (and especially feel) indicates that an electrostatic discharge (ESD) event has occurred. Among all transient disturbances ESD is still one of the most important reliability problems in the semiconductor industry and one should never overlook the damage that has been caused by this re-balancing of charge between objects brought into close contact. Especially in newer technologies with thinner gate oxides and small channel lengths the destructive nature of ESD becomes more apparent (see Fig. 5-1).

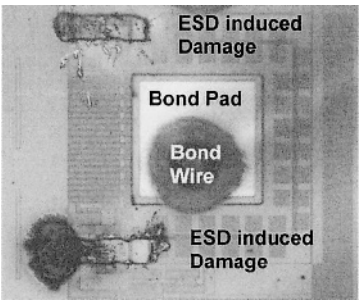


Figure 5-1. Detailed view of melted metal traces due to ESD stress.

In the automotive industry for example very high ESD protection levels are specified in several product specifications, which define the requirements for electrical behavior and EMC of on-board electrical and electronic equipment. Up to now, these requirements mainly concerned direct suppliers of the automotive industry. The suppliers increasingly tend to pass on these specifications to the IC manufacturers. Therefore, ICs for automotive applications are often required to directly handle and survive ESD pulses that originally have been specified for system-level tests (e.g. according to EN 61000-4-2).

In order to keep up with these requirements, improved ESD protection structures will be needed, with the ability to divert even higher currents away from the vulnerable internal circuitry and the capability to clamp high voltages during an ESD event. But device dimensions are shrinking and due to smaller voltage windows, the design of effective ESD protection circuits becomes more challenging. Still, the desired way of handling ESD pulses together with integrated circuits is to use on-chip protection structures.

1.2 ESD Test Models

Evaluating the sensitivity of integrated circuits to ESD is a key element in preventing and controlling ESD damages. Since the early days of ESD control a lot of effort has been spent to develop models for ESD test methods that cover all the different ESD events, which are occurring during the lifetime of an IC. It was found that discharges occurring from handling by persons might damage some ICs, while others may be more prone to be damaged within automated machine handling.

Back in the 1960's, the first ESD model, which was used to stress IC's, was the HBM (Human Body Model). But soon it was noticed that the HBM could not explain all ESD failures and with the increasing use of automated handling machines the MM (Machine Model) was introduced.

Still other types of ESD damage exist, which can not be covered by these two test models. For example when an IC slides down a shipping tube it becomes charged and it will be discharged when it hits a grounded steel table. Therefore the CDM (Charged Device Model) was developed in the early eighties to explain this type of damage. During all these tests the IC is usually not powered up, and "only" the survival of the packaging and handling of the IC is considered. In the future it will be even more taken for granted that the IC has to survive the packaging and handling procedures and the powered up IC will be tested more and more for possible interferences during an ESD event.

To characterize the immunity of ICs against ESD, organizations like AEC (Automotive Electronics Council), ESDA (Electrostatic Discharge Association), EIA/JEDEC (Electronic Industries Alliance/Joint Electron Device Engineering Council), and MIL-STD (US Military Standard) have developed several ESD standards. Depending on the nature of the ESD event, the test methods, which are described in these standards, are based on these three basic models (Ker, 2001)

Although the full spectrum of all different possible ESD events that might stress an IC during its lifetime will never be able to be covered, these models are reproducing most of the ESD field failure signatures. The usual concerns are with multiple failure signatures like junction leakage, short, gate oxide breakdown, thermal destruction, etc. A detailed comparison of ESD models and their failure signatures is given by Kelly et al. for CMOS devices (Kelly, 1995).

1.3 The Human Body Model (HBM)

One of the oldest and widely used models to test the robustness of IC to ESD is the well-known "Human Body Model". It describes the discharge procedure that occurs if a standing charged human person approaches a grounded IC. When the air breaks down between the human's finger and an IC pin, the capacitance of the person is discharged via the IC and the ground pin to ground. The traditional standard for this ESD event was originally defined in the MIL-STD-883x method 3015.7 (US Department, 1991). This standard defines a simplified equivalent circuit to describe the HBM ESD event (see Fig. 5-2). The capacitor C_{HBM}=100 pF in this circuit represents the charged human body and R_{HBM}=1500 Ω specifies the typical human body discharge resistance. The current waveform specification for this HBM ESD pulse, which is generated by an HBM ESD tester to a short wire, is illustrated in Fig. 5-3. For commercial ICs very often HBM ESD levels of 2 kV are specified. The peak current caused by such an ESD event is approx. 1.3 A.

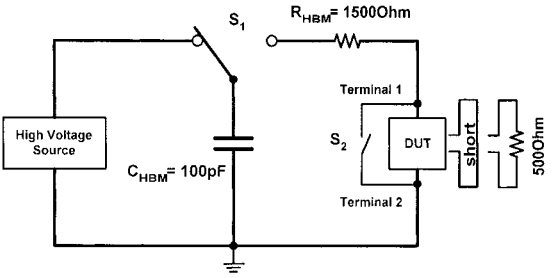


Figure 5-2. Simplified equivalent HBM circuit (MIL-STD-883x).

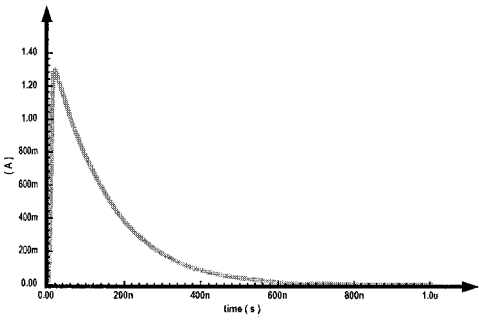


Figure 5-3. Current waveform as defined in MIL-STD-883x for a 2 kV HBM ESD pulse (IC-level).

Usually, well-designed on-chip protection devices can easily divert this current-pulse at voltages low enough to protect vulnerable devices within the core of an IC.

In addition to the MIL-STD-883x method 3015.7 there are several other HBM standards like the JEDEC JESD22-A114-B (EIA, 2000), the ESDA STM5.1-1998 (ESD Association, 1998), or the AEC-Q100-002-REV-C (AEC, 1998).

Another ESD discharge, which is also based on the HBM, is described in the system-level EN 61000-4-2 standard (IEC, 2001). This standard was originally developed to evaluate the performance of a whole electronic system when subjected to electrostatic discharges. It describes an ESD event that occurs if a charged person discharges via a metallic tool (for example a screwdriver, which is held in the hand of a human) into the grounded device under test (DUT).

The electronic system has passed the ESD test if it does not show degradation or loss of the function below a performance level that is specified by the manufacturer.

During the test, degradation is allowed, but not a change in the actual operating state or stored data. The preferred test method is contact discharge; air discharge shall only be used where contact discharge cannot be applied. The voltages for each test method are different and depending on the defined severity level that the DUT has to withstand.

Usually a discharge of ±4 kV using the contact method and/or ±8 kV using the through air method is specified.

Nowadays this standard is increasingly used for characterizations at the IC-level. The automotive industry in particular frequently requires this standard for ICs having a direct connection to the cable harness. Without additional external ESD protection structures the whole discharge current is directly injected into an IC pin.

In (Körber, 2004) a test setup for these system-level ESD tests is proposed for the characterization of ICs used in the automotive industry. This test is based on the assumption that most of the ESD interferences of a semiconductor device are caused by a direct discharge onto the connector pins of an electrical/electronic piece of equipment. It should only be applied to those IC pins, which have a direct connection to the cable harness in the vehicle. To consider the influences of necessary external components, a special test PCB has to be used.

The typical waveform of this system-level ESD event is completely different to that at the IC-level and is shown in Fig. 5-4. It comprises of the discharge waveforms of two sequential discharge events.

First, a very sharp current peak, with an extremely short rise-time (less than 1 ns) describes the discharge procedure of a local capacitance of the metallic tool. This discharge is followed by the discharge procedure of the human body, which is handling the metallic tool.

Compared to the IC-level HBM standard, the specified capacitance of the human body and the discharge resistance is different. For example the EN 61000-4-2 specifies a 150 pF capacitance discharging through a 330 Ω resistor, which results in much higher discharge energies.

Fig. 5-5 shows to what extent a 2 kV system-level HBM pulse differs from a 2 kV IC-level HBM pulse. The peak current produced by such a system-level ESD event can easily reach tens of Amps. Additionally, the pulse has a much faster rise time and contains more energy than an IC-level HBM pulse of the same voltage. From that it can easily be seen that the requirements at the system-level by far exceed the values at the IC-level.

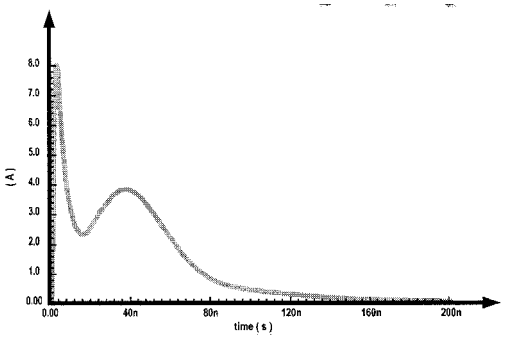


Figure 5-4. Current waveform as defined in EN 61000-4-2 for a 2 kV HBM ESD pulse (system-level).

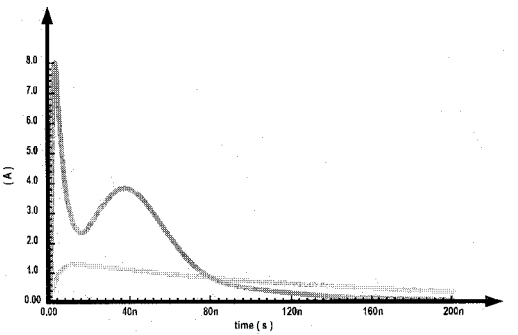


Figure 5-5. Current waveform of a 2 kV system-level (EN 61000-4-2) and IC-level (MIL-STD-883x) HBM ESD pulse.

1.4 The Machine Model (MM)

In addition to a human body discharge, any charged object can cause electrostatic discharges to an IC when touching it. Typically the discharge resistances of such metallic machines are much lower than that of human bodies, which result in much higher peak ESD currents.

The Machine Model (MM) for example represents an ESD stress, which is caused by a machine during the handling of an IC (i.e. metallic machinery in an IC manufacturing or testing process). It originates from Japan and represents a low-impedance high-current discharge into an IC. The primary MM standards are the ESDA STM5.2-1999 (ESD Association, 1999), the JEDEC EIA/JESD22-A115-A (EIA, 1997), and the AEC-Q100-003-REV-F (AEC, 2001).

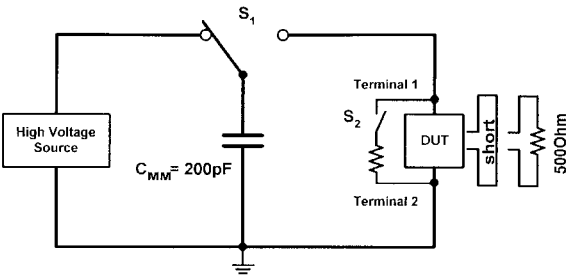


Figure 5-6. Equivalent model circuit for the MM ESD test with CMM = 200 pF and negligible resistance and inductance in the discharge path.

The discharge circuit is similar to that of the HBM, except for the discharge capacitor being defined with 200 pF and almost all of its electric energy being forced into the IC pin, as the discharge resistor is kept to a minimum (preferable 0 Ω). Fig. 5-6 shows an example of a MM model circuit as it is specified in AEC-Q100-003-REV-F.

The very low discharge resistance in the MM ESD test results in very high peak currents, which strongly depend on the parasitic elements of the testing system and the DUT. The voltage levels that the DUT must typically withstand for MM ESD tests (±200 V for regular and ±400 V for increased demands) are much lower than for HBM ESD tests. The typical ESD failures, which are caused by MM ESD tests, are often similar to the failures of HBM tests (thermal failures in the diffusion regions).

The output waveform of a MM ESD tester should match with the typical current waveform that is shown in Fig. 5-7. It oscillates due to the parasitic inductances of the testing system. Due to the parasitic effects in the discharge path, the real ESD current waveform that a MM ESD tester produces may be quite different from what is specified in the standards.

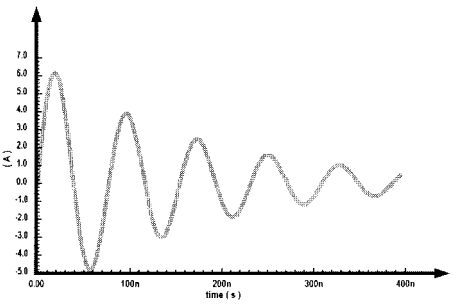


Figure 5-7. Current waveform of a 400V MM ESD discharge as specified in AEC-Q100-003-REV-F.

1.5 The Charged Device Model (CDM)

Unlike the HBM or the MM, where an externally charged human or machine is responsible for electrostatic discharges, the charged device model (CDM) describes an ESD event, where a charged IC itself is the reason for a discharge event (Speakman, 1974). In this case the charge is initially stored in the body of an IC and it self-discharges if one of its pins contacts a grounded object.

This event mainly occurs during the automated manufacturing and assembly processes, where the IC for example charges when it slides down a feeder into an automated tester or a shipping tube.

As human handling is getting more and more redundant in the semiconductor manufacturing process, the characterization of the susceptibility against CDM stress becomes increasingly important. The CDM ESD event represents a very fast discharge (in ns) via a low resistive ground path. Although the charge that is stored in an IC is usually small, the CDM event can produce very large ESD currents due to the low resistances and inductances in the discharge path.

The pre-charging for this ESD event mainly occurs due to two mechanisms: direct or field induced charging. In the case of field-induced charging the entire IC is charged by induction in the presence of an electric field, while in the direct charging case the IC is charged by the direct contact of one of its pins to a high-ohmic voltage source.

There are two general types of CDM test procedures that are used to characterize the susceptibility of an IC. The non-socketed CDM test, where the IC is tested directly, and the socketed CDM test (SDM), where the IC is mounted in an IC socket. For the non-socketed CDM test the DUT is placed upside down in the "dead bug position" on an insulating surface (the charge plate). It can be charged by the field induction or by the direct mode, where the field induction mode is more preferable as it does not damage the IC by charging it. The discharge procedure is carried out by a grounded probe, which directly contacts one of the ICs pins. It is very important that the probe has a very low-impedance and that the discharge path of the CDM tester has very low parasitic influences in order to ensure the reproducibility of the pulse waveform. Fig. 5-8 shows a simple schematic of this test setup.

The primary CDM ESD standards are the JEDEC JESD22-C101-A (JEDEC, 2000), the ESD STM5.3.1 (ESD Association, 1999), and the AEC-Q100-001 (AEC, 2001) to mention the most important.

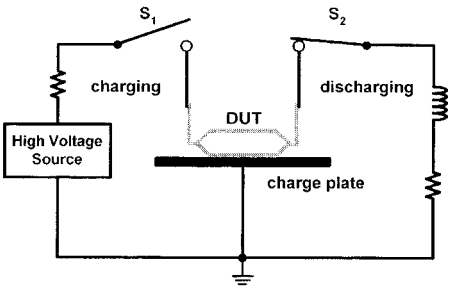


Figure 5-8. CDM ESD test setup (field induced no-socketed CDM).

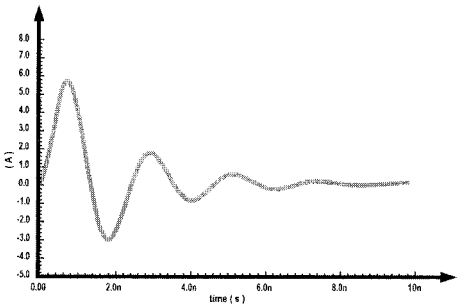


Figure 5-9. Current waveform of a 500V CDM ESD discharge as specified in JEDEC JESD22-C101-A.

A standard CDM ESD pulse waveform, which is specified in the JEDEC JESD22-C101-A standard, is shown in Fig. 5-9. Due to the parasitic effects in the discharge path, which have a strong impact on the pulse waveform, it is very difficult to build a CDM tester, which meets the standardized waveform.

Compared to the previously discussed HBM and MM ESD stress, where thermal failures in the diffusion regions are the main failure modes, a CDM discharge often shows a different failure signature (Maene, 1994; Brodbeck, 1996; Brennam, 2004). One of the typical CDM failure modes is a pinhole in the gate oxide, which is caused by the very short stress duration with high currents (up to several Amperes) and the related high voltages across the thin gate oxide.

According to the shrinking gate oxide thicknesses in modern semiconductor devices, the characterization of the immunity against ESD events has shifted to CDM ESD test.

1.6 The Transmission Line Pulse (TLP) Model

In addition to these test methods, which are commonly used to evaluate the ESD robustness of ICs, another characterization technique has become increasingly important for the non-destructive characterization of ESD protection structures. As the traditional ESD test methods are mainly based on simple pass/fail characterizations, the Transmission Line Pulse (TLP) technique offers numerous advantages and has the potential to replace these test methods.

The TLP technique, which was first reported by Maloney et al. for the characterization of ESD protection structures, is a simple method to produce high current square wave pulses by the discharge of a coaxial transmission line (Maloney, 1985). This pulsed characterization technique addresses the dynamic behavior of an ESD protection element and does not lead to thermal destruction, as is usually the case by DC-characterizations based on the traditional test methods. Its basic principle is shown in Fig. 5-10.

The transmission line T is charged to a certain voltage-level by a high-voltage source via resistor R_V. When switch S is closed the charge, which is stored in the transmission line, is forced via the series resistance R_S and the DUT to ground. This produces a high current pulse, as shown in Fig. 5-11.

The pulse width can be determined by the physical length of the transmission line. A lot of investigations have been made to figure out an ideal TLP pulse, which has the same energy content as an HBM pulse in order to correlate TLP with HBM measurement results (Salome, 1998; Lee, 2000; Barth, 2000; Barth, 2001; Notermans, 1998).

During a discharge, the current-pulse I(t) through the DUT and its corresponding voltage response V(t) is measured and their averaged values give one single point in the IV-characteristic of the device. As the pre-charge voltage is increased step by step, all other current and voltage values for the full IV-characteristic can sequentially be obtained.

The result of a TLP measurement is a quasi-static IV-characteristic of the investigated device, which gives an insight into the behavior of the device under ESD conditions.

Usually the leakage current is measured after each discharge and a significant increase in leakage is considered as a criterion for an ESD-induced damage of the device. This is typically associated with a second snapback of the voltage caused by a second-breakdown of the device.

A TLP measurement example of a silicon controlled rectifier (SCR) ESD protection device is shown in Fig. 5-12.

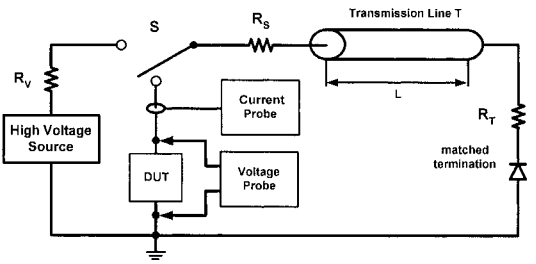


Figure 5-10. Schematic of a TLP test system (RV=1 MΩ, RS=50 Ω – 1000 Ω, RT=50 Ω).

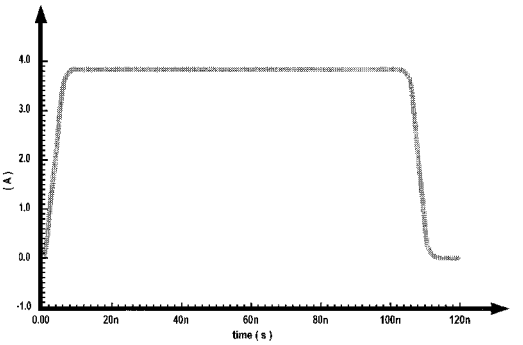


Figure 5-11. Current waveform of TLP as specified in ANSI/ESD SP5.5.1-2004 (pulse width 100 ns, tr=0.2-10 ns, tf=0.2-10 ns).

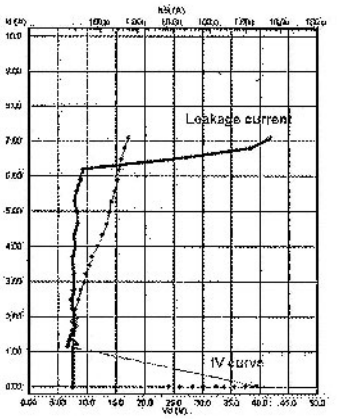


Figure 5-12. Pulsed IV curve and the leakage current measurement of a silicon controlled rectifier (SCR) ESD protection device.

The right curve (thin curve) shows the pulsed IV characteristic of the device, which is sequentially obtained by the voltage and current measurements of several discharges. The left curve indicates the leakage evolution of the device under growing TLP stress (thick curve, right and upper axis). As can be seen the leakage current increases significantly at approximately 6.2 A of pulse current. This conforms to approximately 9 kV stress measured with the IC-level HBM. At this point, which indicates a second breakdown, the device gets severely damaged. Additionally, interesting parameters such as dynamic on-resistance or holding voltage can be extracted from the IV curve to evaluate the ESD protection capabilities of the protection device. The advantages of the TLP characterization, like a well reproducible current pulse waveform, as well as the insights provided by the IV curve have led to the idea of developing a standard TLP test model (Voldman, 2003; Keppens, 2001).

In 2004 the ESD Association has completed a standard practice document, the ANSI/ESD SP5.5.1-2004, which defines the measurement parameters and TLP tester setup regulations to allow comparable and reliable TLP-based ESD tests (ESD Association, 2004).

2. INTERNAL CURRENT SWITCHING

2.1 Origin

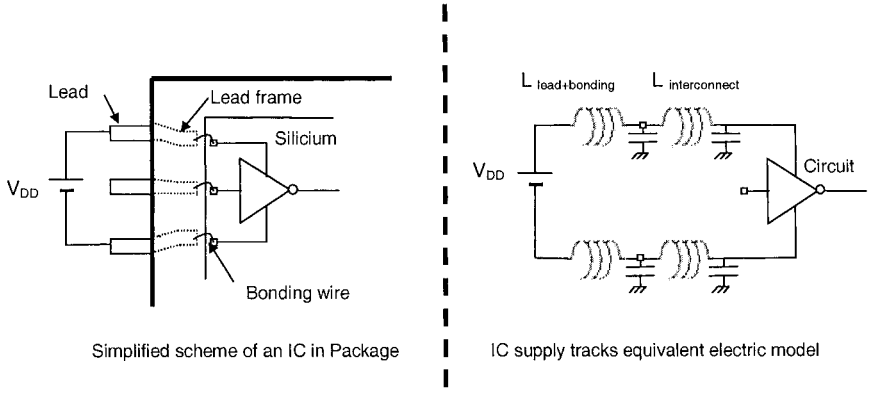


Figure 5-13. Electrical model of an IC in its package.

Simulating the parasitic emission of ICs before manufacture is a key factor for avoiding redesign, which has a very important impact on the overall cost and time to market. To be able to predict accurately the electromagnetic emission of an IC, it is necessary to be aware of the source of perturbation.

The electromagnetic parasitic emission of integrated circuits mainly originates from activity of each elementary gate or inverter externally supplied. Fig. 5-13 gives a simplified view of an elementary gate and a simplified model of its supply tracks.

2.2 Basic mechanism of parasitic emission

When a logic gate is activated (Fig. 5-14), a transition from logic level 0 to 1 and 1 to 0 generates a current peak I_P and I_N on the supply paths (V_{DD} and V_{SS}). The rapid variation of current flowing within the package generates power supply fluctuations. The variations of current through the bonding and package inductances induce a voltage drop that generates a severe ground-bounce close to the FM band.

As the inverter has a non-symmetric structure, the current peak is not the same for the switching On and the switching Off. To simplify the modeling approach the average between these two current waveforms will be considered (Fig. 5-15).

The current peaks depend on two main parameters: the current amplitude and the operating frequency clock of the IC. This technology trend influences the operating frequency of the ICs with significantly large effects on current peaks. They become shorter and sharper, which in turn generates unfortunate consequences on the emission spectrum.

With the progressive miniaturization of CMOS devices, current peak decreases but at a slower rate than cell density increases (Table 5-1).

Table 5-1. Current peak vs. Technologies

Technology	Year	Supply	Density of cells /mm^2	Clock frequency (MHz)	Current per gate	Switching delay
CMOS 1.2 µm	1985	5 V	8 K	4-50	1.1 mA	1 ns
CMOS 0.8 µm	1990	5 V	15 K	4-90	0.9 mA	0.5 ns
CMOS 0.5 µm	1993	5 V	28 K	8-120	0.7 mA	0.3 ns
CMOS 0.35 µm	1995	5-3.3 V	50 K	16-300	0.6 mA	0.2 ns
CMOS 0.25 µm	1997	5-2.5 V	90 K	40-450	0.4 mA	0.12 ns
CMOS 0.18 µm	1999	3.3-2.0 V	160 K	100-900	0.3 mA	0.1 ns
CMOS 0.12 µm	2001	2.5-1.2 V	240 K	150-1200	0.2 mA	70 ps
CMOS 90 nm	2004	2.5-0.8 V	480 K	300-2000	0.15 mA	50 ps
CMOS 65 nm	2007	2.5-0.7 V	900 K	500-3000	0.1 mA	30 ps

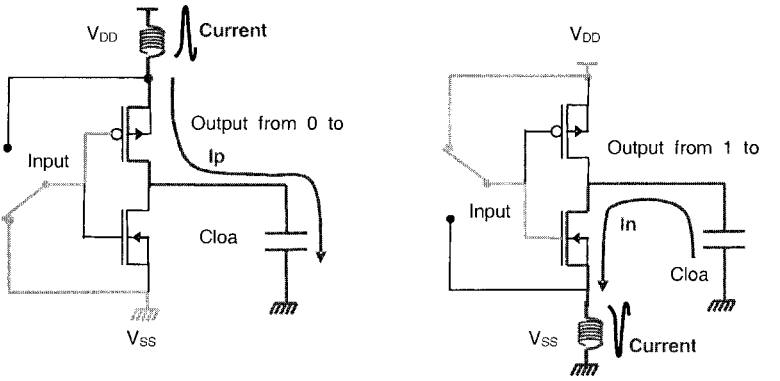


Figure 5-14. Basic mechanism of parasitic emission originates from elementary current flowing during inverter switching.

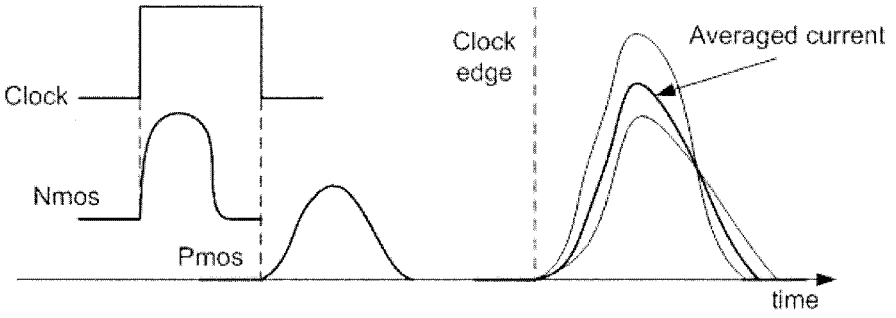


Figure 5-15. Nmos and Pmos consumption current-peak during a switching transition.

As ICs integrate numerous functions located in different blocks, often working in parallel, the global current peak corresponds to the sum of the current consumption of each elementary block. Consequently, the more gates are synchronously switching, the more global current amplitude increases.

Table 5-2. CPU activity

CPU generation	Total number of logic gates	Logic gates active during a clock cycle
8 bits	3000-5000	300-500
16 bits	15,000-100,000	1500-10,000
32 bits	50,000-300,000	5000-30,000

For example, a CPU comprises between 3000 and 300,000 internal logic gates depending on its complexity (Table 5-2). For each clock cycle, only a small portion (10%) of these logic gates is active.

The prediction of the current could be addressed at many simulation levels:

- Circuit simulation or SPICE-like simulation: for more than 10,000 gates, this approach would not be realistic.
- Interpolation simulation with tools like PowerMill (Synopsys©): the main constraint of this approach is that the layout of the component should be available which is not often the case.
- Behavioural simulation: This statistical approach could be applied earlier in the design flow and could take into account a very large number of gates. The statistical estimation can also be used by the customers of the integrated circuit, when the founder does not provide any core model (no need of the layout for example). Based on the technological generation, the die size and the type of processor, a rough estimation of the current peaks generated for each clock cycle can be provided. This method is based on many approximations, but can give an approximate idea of the current consumed by the processor. It seems to be the most suitable for establishing a standard.

In a 16-bit microcontroller with 10,000 logic gates switching simultaneously, the resulting current peak would be approximately 4,5 A! At the present, gates and interconnect delays spread out and reduced the current peak by approximately a factor of 10. In order to preserve energy, the amplitude of the peak is divided by 10. A peak of 450 mA on 4 ns is thus obtained as shown in Fig. 5-16.

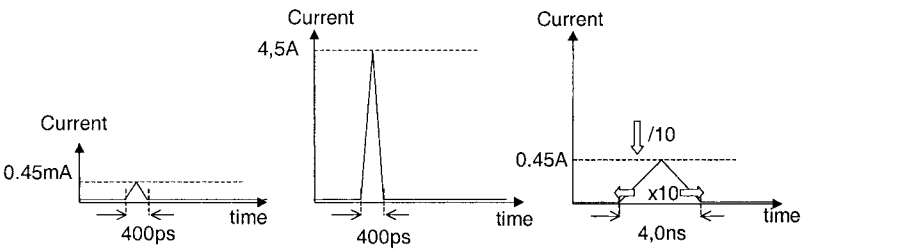


Figure 5-16. Current peak generated by a core of 10,000 switching gates.

3. PRINTED CIRCUIT BOARD MODEL

3.1 PCB overview

EMC modeling and simulation tools have to take into account the accumulation of complex analog, digital or mixed-signal boards within ever smaller structures and, consequently, the advent of tighter electrical/electromagnetic couplings.

In this section, an EMC modeling methodology for electronic Printed Circuit Boards (PCBs) and some applications for electrical-oriented EMC simulations are presented. First of all, the best-known current PCB configurations, along with the technology and the physical characteristics used for PCB design with devices or integrated circuits, are introduced. Measured and simulated EMC signals on test PCBs (format 10 cm x 10 cm), bearing elementary digital circuits, are then displayed.

At low frequencies or switching rates, signals and pulses that propagate along circuit board tracks can, for practical purposes, be regarded as electrical information and digital pulses that are transmitted with no distortion and no delays. However, as clock rates increase in modern electronic circuits, these structures can no longer be studied as passive carriers. Instead, parasitic capacitances and inductances, associated with power losses, introduce time delays and distortion that can adversely affect signals and create parasitic radiated fields.

Some EMC emissions due to PCBs and devices can be identified: DC supply couplings and noise, input/output couplings and direct radiated emissions. In PCBs this is mainly a conducted mode noise due to supply switching currents, flowing through common impedances as well as supply connections. Significant electric or magnetic fields radiate over some elements of the board due to tracks lengths which can be found on a standard PCB.

3.2 PCB standard geometries and characteristics

3.2.1 Single / Double sided PCBs

The connections of high-density integrated circuits are usually achieved on thin solid substrate materials, called boards, on which conductive connections are made by etching or serigraphy: this is the Printed Circuit Board (PCB), with various dimensions adapted to the system under design: from 1 cm^2 to 50x50 cm^2. Devices and packaged chips are attached on one side (component side) of the board.

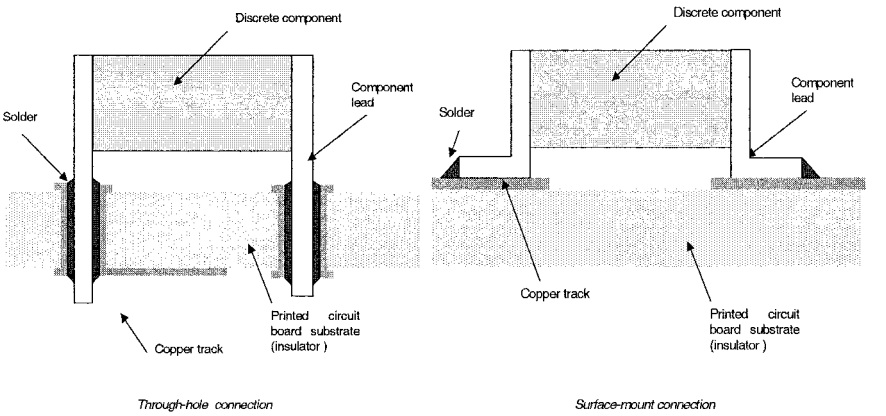


Figure 5-17. PCB technologies.

Two types of interconnecting techniques can be used:

- Single-sided PCBs, on which conductive or copper tracks are located on one side, whereas devices are located on the other. The pins of the packaged circuits are soldered with to the track using a through-hole connecting technique.
- Double-sided PCBs: copper or conductive connections can be installed on both sides of the substrate board. Components can be added on one of these sides, with through-hole SMD (Surface Mount Device) techniques (Fig. 5-17).

The most common conductive material used in PCBs is copper. Aluminum is only used for particular applications (power PCBs). Some physical characteristics of conductive and dielectric materials for PCBs are summarized in Table 5-3.

Table 5-3. Physical characteristics of conductive and dielectric materials for PCB

Conductor	Conductivity σ(S/m)	Dielectric	Relative permittivity εr
Copper	5.76×10^7	PTFE Teflon	2.17~2.33
Aluminium	3.96×10^7	E-Glass epoxy (FR4)	4.3~4.5
Lead	5.0×10^6	Lead-Glass	6.0

An elementary copper track on the PCB substrate can be modeled by the following parameters (Fig. 5-18):

- Substrate height e_S.
- Conductor length L_0.
- Conductor width w.

- Conductor thickness *e*.

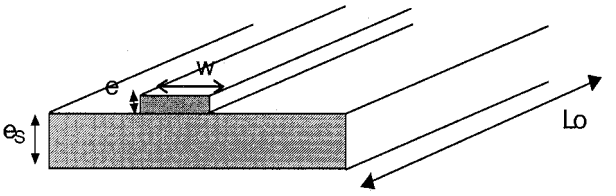


Figure 5-18. PCB elementary interconnection track.

In order to obtain the appropriate impedance of this single track, internal and external conductive parameters have to be considered:

1. Internal parameters are intrinsic to the conductor: R (resistance) and Li (internal inductance):

- Resistance: as demonstrated in Chapter 3, the low frequency resistance (or R_{DC}) is given according to Eq. (5-1) whereas the high frequency resistance (or R_{HF}) takes into account the skin-effect depth (δ) according to Eq. (5-2). This resistance increases with the $f^{1/2}$ law.

$$R_{DC}(\Omega/m)=\frac{\rho}{w.e} \tag{5-1}$$

If the conductor can be identified as a thin strip (e<<w), R_{HF} can be evaluated by (ρ is the material resistivity):

$$R_{HF}\approx\frac{\rho}{2\delta w} \tag{5-2}$$

- Internal inductance: Li_{DC} and Li_{HF} expressions, for a PCB copper track, are complex analytical expressions (Tesche, 1997). In many cases, it can be ignored with respect to the external value of the conductor inductance, Le.

2. External parameters are due to the mutual influence between two neighboring conductors, such as signal and ground or return path conductors (Fig. 5-19).

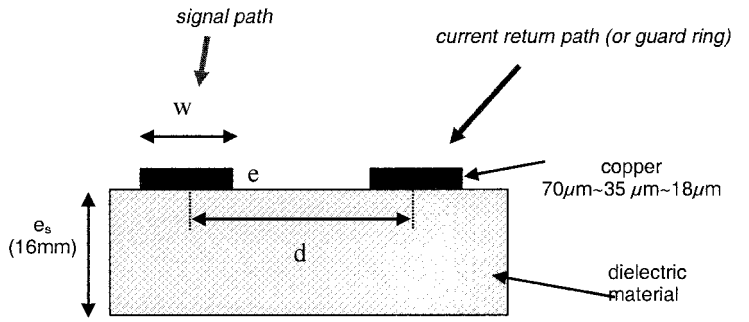


Figure 5-19. Differential track configuration.

Both conductors in this configuration generate: a closed loop defining an external inductance *Le*, and a charge distribution defining a capacitance *C*. Their generic analytical expressions, for any conductor, are given by Eq. (5-3) and Eq. (5-4).

$$Le(H/m)=\mu.f_G \tag{5-3}$$

$$C(F/m)=\frac{\varepsilon}{f_G} \tag{5-4}$$

where μ is the material permeability, f_G is a function which depends on the geometry of the conductor (Tesche, 1997) and ε the material permittivity.

3.2.2 Conductive plane

A conductive plane is considered as quasi-infinite with respect to track dimensions. In this case, there is no return path for magnetic flux, and electric charges can not be stored. Consequently, there are no equivalent inductive or capacitive electrical elements. The impedance of the plane is only a resistance. It varies with frequency due to the skin effect. Its value is expressed in resistance over square (length = width) (Eq. 5-5, Eq. 5-6).

$$R_{DC}(\Omega/square)=\frac{\rho}{e} \tag{5-5}$$

$$R_{HF}(\Omega/square)=370.10^{-9}\sqrt{f} \text{ for a copper plane} \tag{5-6}$$

3.2.3 Microstrip line

With double-sided PCBs, conductive connections can be routed on each side of the dielectric substrate (Fig. 5-20). The classic configuration, which corresponds to state-of-the-art parasitic and noise reduction, is the microstrip configuration.

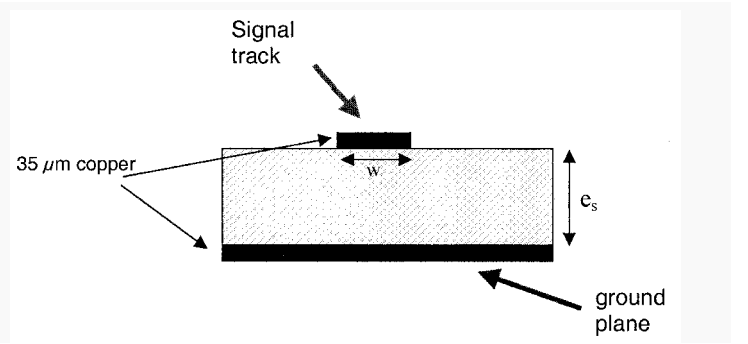


Figure 5-20. Microstrip line configuration.

The current return path for all the nets of the upper side is achieved by a plane layer. This enables designers:

- to reduce the common impedance of the whole surface of the PCB.
- to harden the PCB on its backplane.
- in case of high speed signals or low switching times, to gain control over propagation characteristics, as it is one of the basic configurations of the quasi-static TEM (Transverse ElectroMagnetic) mode.

Propagation characteristics are represented by external electrical parameters Le and C given by Eq. (5-3) and Eq. (5-4) respectively where f_G is given by Eq. (5-7). *Le* and *C* are frequency-independent. They vary with distance (inversely proportional to geometrical dimensions).

$$f_G = \frac{1}{2\pi}\ln\left(\frac{8d}{w}+\frac{w}{4d}\right) \text{ for } \frac{w}{d}\le 1$$

$$f_G = \frac{1}{\left(\frac{w}{d}+1.393+0{,}667\ln\left(\frac{w}{d}+1.444\right)\right)} \text{ for } \frac{w}{d}>1 \qquad (5\text{-}7)$$

3.2.4 Multi-layer PCBs

In modern high-density PCBs, a multi-layer PCB technology, represented by the example of the single stripline topology, is often used: it refers to a track located between two planar conductive structures, with dielectric material completely surrounding the tracks (Fig. 5-21).

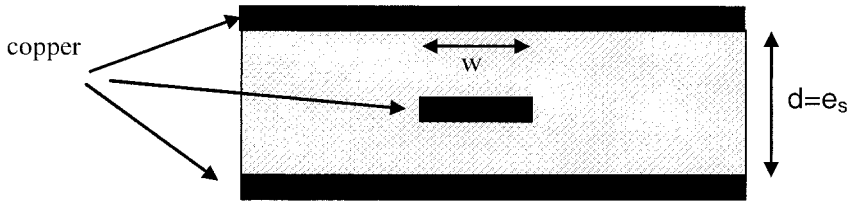


Figure 5-21. Stripline configuration.

The separate planes can act as shielding or wave guides for the correct propagation of signals. They also act as a better return path for the common-mode behavior of the PCB. Two or more separate planes can be related: separate power plane – ground plane, separate analog – digital planes. Devices can be added on the external planes with copper track connections and via hole interconnections with other planes: this achieves a 3D interconnection at PCB level.

Le and *C* are respectively given by Eq. (5-3) and Eq. (5-4) where f_G is given by Eq. (5-8):

$$f_G = \frac{1}{4}\ln\left(\frac{d}{w_{eff} + 0.441d}\right) \text{ for } \frac{w}{d} \le 1 \tag{5-8}$$

$$\text{in which } w_{eff} = w - \begin{cases} 0 & for\ w/d < 0.35 \\ d(0.35 - w/d)^2 & for\ w/d > 0.35 \end{cases} \quad \text{for } \frac{w}{d} > 1$$

Le and *C* are frequency-independent. They vary with distance (inversely proportional to geometrical dimensions).

3.2.5 Power/ Dedicated PCBs

PCBs dedicated to power transients and high-density switching currents are often single or double-sided with large power, ground and interconnection tracks: from 35 µm to 70 µm, because of copper heating due to power current distributions. Power PCBs can also bear a wide ground plane, up to 1 cm, meaning that the PCB lower side can serve as a heat sink, as devices are located on the upper side.

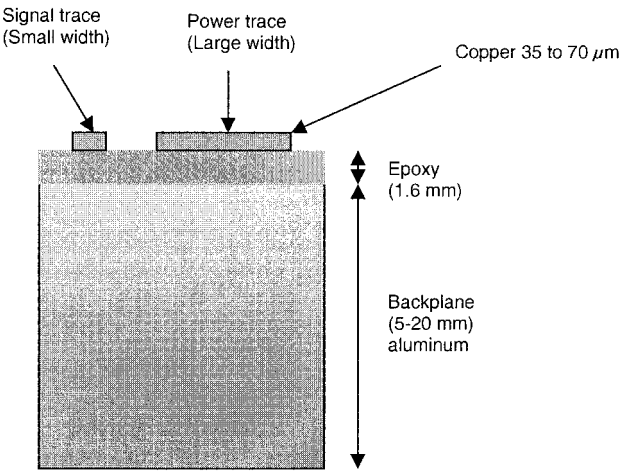


Figure 5-22. 2D view of a Power PCB.

For very high power switching currents, double-sided configurations are designed with copper-epoxy-alumine multilayer configurations (Fig. 5-22) or copper-epoxy-AlN (Aluminium Nitride) configurations. These planes, with a dielectric isolated substrate dedicated to static and dynamic power thermal dissipation, generate non-ideal impedances, as in previous cases (microstrip and stripline configurations). These power PCBs should be modeled with a 3D interconnection approach and the partial equivalent element concept.

3.2.6 3D approach: partial parameters, coupling coefficients

In many real-world cases, PCB tracks, copper zones or planes do not fulfill 2D considerations: finite dimensions of their equivalent lines, edge effects, non-ideal conductors or return paths. Discontinuities associated with bends, junctions and vias are also not taken into account by 2D calculations.

In order to model the effects of such discontinuities, it is thus necessary to draw and analyze a full three-dimensional model of a structure. It is particularly the case when track configurations on a PCB do not match microstrip or stripline schematics. TLT (Transmission Line Theory), with the use of equivalent electrical (RLC) cells can still be used, but the 2D approach is not as well adapted to parameter extraction as it is to the modeling of PCB electrical and EMC effects.

This leads to the introduction of 3D effects. Propagation and electromagnetic effects have to be evaluated, modeled and calculated with numerical techniques. Meshing techniques are used, after which Maxwell equations can be solved in the frequency domain or the time domain, providing solutions for the electromagnetic problem: current distribution densities, potential and field lines, radiated near/far fields with geometry and frequency considerations for the PCB.

The next step consists in transforming these EM solutions into the circuit domain, while including delay and propagation effects: these are the concept and technique associated with partial elements for electrical circuits.

3.2.7 Example

In the following example, the extraction of the equivalent electrical parameters of a test board with 2D and 3D approaches is presented (Fig. 5-23).

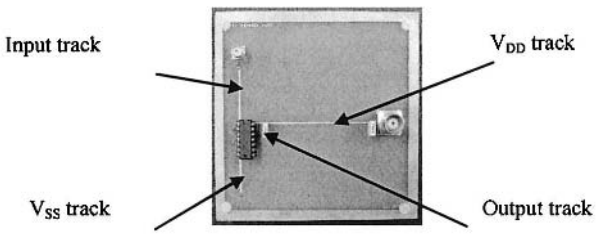


Figure 5-23. PCB test board.

As it is a double-sided 35 µm-thick copper PCB with a ground backplane (10x10 cm²) on the other side, each track can be considered as a microstrip configuration ($w<<L_0$), with the following characteristics:

- V_{DD} track: L_0 = 6.5 cm, w = 0.8 mm.
- V_{SS} track: L_0 = 1.9 cm, w = 0.8 mm.
- Input track: L_0 = 3.2 cm, w = 0.8 mm.
- Output track: L_0 = 1.3 cm, w = 0.8 mm.

3.2.7.1 2D calculation

All the tracks of the test board are assumed to have the same cross section configuration: copper microstrip on epoxy. Considering one cell model (lumped model) for each PCB track, this leads to Fig. 5-24.

For higher-frequency stimuli, cell models can be split into n cells and become a distributed model. The 2D line coupling effects of this board can be taken into account by modeling the vicinity between the output trace (pin 13) and the V_{DD} line. Consequently, along the effective length (1.3 cm), this microstrip differential line configuration can be modeled leading to Fig. 5-24.

3.2.7.2 3D calculation

Under the new assumption that the Vss line, the output line or the input line are influenced by the edges of the PCB, or by mutual couplings with them, this test PCB now has to be modeled with the help of a 3D EM solver (Fig. 5-25). The calculations of the charge distribution and the current density in the four conductors of the board are converted into a 4x4 matrix of equivalent partial electrical elements. In order to represent the electrical schematic, simplifications can be performed depending on coupling factors: a weak coupling factor, below 10 %, allows the elimination of the mutual electrical elements of the structure. These results are summarized in Table 5-4 for this generic test PCB.

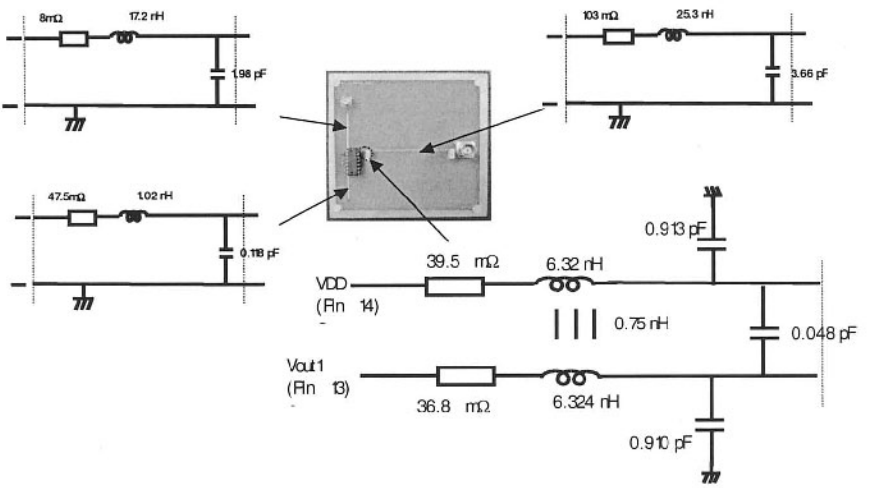


Figure 5-24. Coupling model between VDD and output.

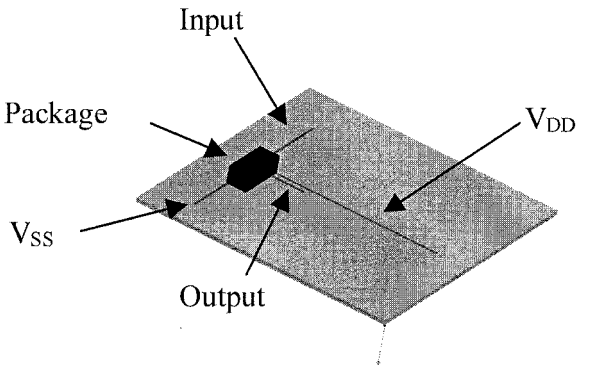


Figure 5-25. 3D schematic of the test PCB.

Table 5-4. Values of the equivalent electrical elements

Conductor	Ci (self capacitance)	Li (self inductance)	Ri (self resistance)
Input	***0.62 pF***	***31 nH***	***0.057 Ω***
Output	***0.53 pF***	***10.3 nH***	***0.024 Ω***
Vdd line	***1.18 pF***	***72.2 nH***	***0.11 Ω***
Vss line	***0.57 pF***	***16.5 nH***	***0.032 Ω***

4. PACKAGING

Historically, the continual improvement in power/speed/cost characteristics that has underpinned the growth of most electronics industries has mainly been the result of scaling down chip geometries in accordance with Moore's Law.

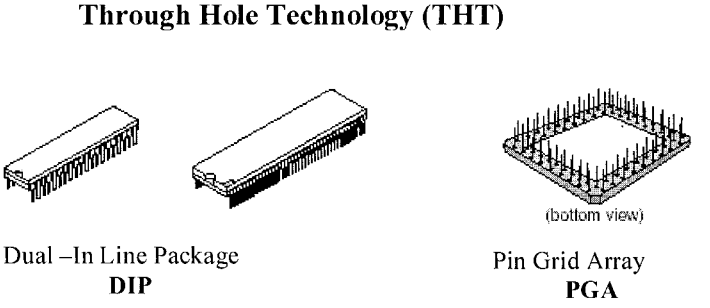


Figure 5-26. Survey of Through-Hole Packages.

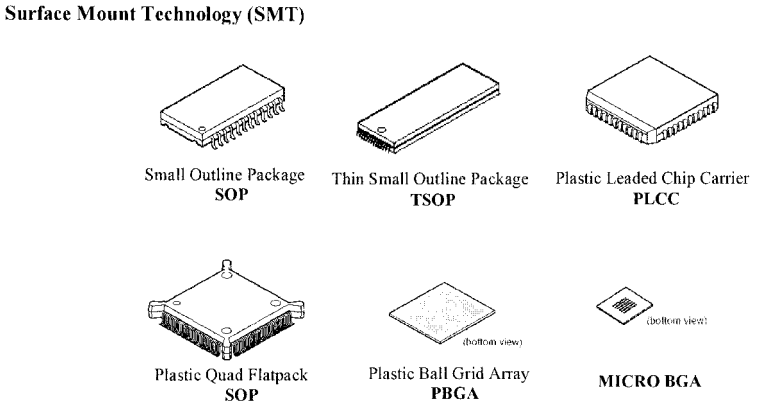


Figure 5-27. Survey of Surface-Mount Packages.

Packaging technology, as part of the back-end process, has therefore largely played a background role. One of the most important trends today is the emergence of new packaging technologies in which silicon-level integration is augmented by package-level integration, which houses two or more die in a common package. In this section, some current standard IC packages and the principles of their technology are presented first. Then analytical and numerical calculations and methods to extract the values of their electrical equivalent models will be presented.

4.1 Standard IC package technology

Package technology is characterized by three parameters:

- The lead pitch, which ranges from 2.54 mm in the case of dual in-line packages to 0.3 mm in the case of Plastic Quad Flat Packages (PQFP)
- The pin count which is about 40-60 in DIPs, and 500 in the Ball Grid Array (BGA) family.
- The efficiency of interconnections, intended as the ratio between active chips and the package footprint, which is 1-5% in DIPs, 50% in Thin Small Outline Packages.

The different technologies are illustrated in Fig. 5-26 and Fig. 5-27.

4.2 Calculation of equivalent packaging circuit

An electrical model of a package translates its physical properties into electrical characteristics that are usually combined into a circuit representation. The typical electrical circuit characteristics that are reported are DC resistance (R), inductance (L), capacitance (C), and characteristic impedance (Zo) of various structures in the package. This model describes the signal path from the die to the board. Fig. 5-28 depicts the physical view of chip-package interconnections.

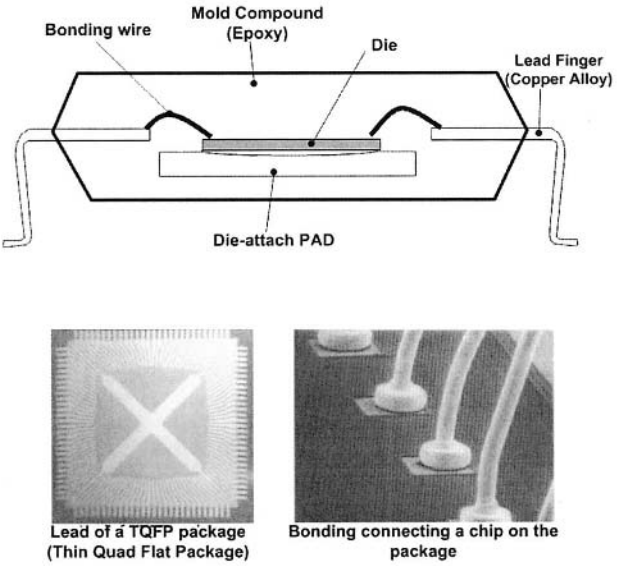


Figure 5-28. Physical view of chip package interconnections.

Depending upon the complexity of the model required for simulation purposes, the model can take the form of a simple lumped circuit model, a distributed lumped circuit model, a single-conductor transmission-line model, or a multiple-conductor transmission-line model.

4.2.1 Package Resistance

Ceramic packages have relatively high resistance because of the high resistivity of the tungsten alloy metallization used with ceramic technology. Plastic/organic packages have much lower resistance because the metallization used is either copper or a copper alloy. (See Chapter 3, Table 3-3).

4.2.2 Package Capacitance

Capacitance (C) is determined by the lead length and cross-sectional dimensions, the spacing between leads, the spacing between the lead and the power or ground plane, the dielectric constant of the surrounding material, and the number of leads involved. The relative dielectric constant of the material used for ceramic packages is in the range of 8–10. The dielectric constant of the material used for plastic packages is in the range of 4–6.

There are formulas for the capacitance of classic geometries; however, the loading capacitance is the total capacitance of a lead with respect to all surrounding conductors. The lead-to-lead capacitance is the mutual capacitance between the two leads. The loading capacitances are the diagonal terms in the so-called "short-circuit" capacitance matrix, and the lead-to-lead capacitances are the off-diagonal terms. The lead-to-lead capacitance and the mutual inductance determine the extent of electromagnetic coupling between the two leads.

4.2.3 Package Inductance

An inductor is any conductor across which there is a voltage drop when there is a time-varying current. This aspect of a package is important in determining the extent of the effects of crosstalk and simultaneous switching noise. The typical definition of inductance implies that the inductance is that of a current loop. However, a loop can be segmented and partial-self and partial-mutual inductances can be attributed to each segment. This is a useful concept of Partial Elements, as described for 3D PCBs.

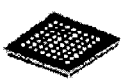
There are few simple formulas for inductance because the inductance is dependent upon both the physical geometry of the structure and the current return path. A few classic problems have been solved in closed form. Software codes that use electromagnetic analysis techniques associated to Partial Element Matrix extraction are better suited to compute the inductance of the complex structures in packages, or high power packages.

Typical values of capacitance and inductance of packages most currently used are presented in Table 5-5.

4.3 First example: medium power IC package

A simplified representation of a Small Outline Package has been achieved with a 3D electromagnetic simulation program. The computed electrical field distribution gives access to the charge and the potential distribution on and around the conductive parts of this drawing.

Table 5-5. Capacitance and inductance of current packages.

Package	Description	Lead capacitance	Lead inductance
	Dual in line (DIL)	1 – 10 pF	2 – 15 nH
	Shrink dual in line (SDIL)	1 – 10 pF	1 – 10 nH
	Small outline package (SOP)	1 – 7 pF	1 – 7 nH
	Quad flat package (QFP)	2 – 5 pF	3 – 7 nH
	Bold gate array (BGA)	1 – 10 pF	0.5 – 10 nH
	Fine pitch ball gate array (FBGA)	1 – 20 pF	0.5 – 10 nH
	Mold chip scale package (MCSP)	1 – 15 pF	0.5 – 5 nH

Then, using the Partial Element concept, the capacitance matrix of (i-j) size is converted from the initial electromagnetic calculations. The *Cii* values are the capacitance value of each finger. The *Cij* values are the "mutual" lead-to-lead capacitance values (Fig. 5-29).

A numerical study can be derived from the quarter portion of the package, which provides an initial 14-14 size matrix. The capacitance matrix is illustrated in Table 5-6.

The inductance and the resistance matrix can also be obtained and represented in the same form.

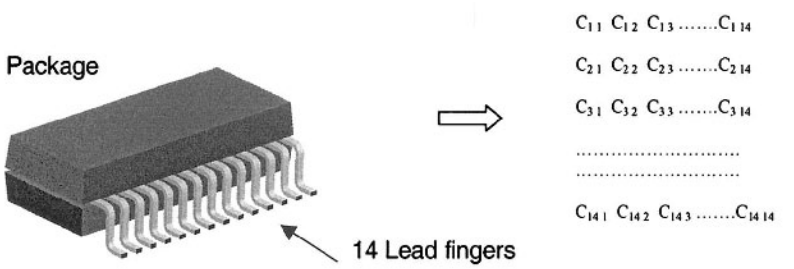


Figure 5-29. 3D Schematic of the ¼ of a Small Outline Package SO56.

Table 5-6. Capacitance matrix of the package

$C_{1\,1}$=1.056 pF	C_{12} = 0.64 pF	C_{13}=0.15 pF	.....		$C_{1\,14}$
$C_{2\,1}$ = 0.64 pF	$C_{2\,2}$=1.34 pF	C_{23}=0.44 pF	.....		.$C_{2\,14}$
C_{31} = 0.15 pF	$C_{3\,2}$=0.44 pF	$C_{3\,3}$=1.2 pF	.....		$C_{3\,14}$
.....					
.....					
.....					
.....			$C_{12\,12}$	$C_{12\,13}$=0.19 pF	C_{1214}=0.054 pF
$C_{13\,1}$	$C_{13\,2}$	C_{13_3}	....	$C_{13\,12}$=0.19 pF $C_{13\,13}$=0.53 pF	C_{1314}=0.21 pF
$C_{14\,1}$	$C_{14\,2}$	$C_{14\,3}$	.....	$C_{14\,12}$=0.054 pF $C_{14\,13}$=0.21 pF	$C_{14\,14}$ = 0.37 pF

4.4 Second example: Cesame Chip package

The Cesame chip (see the companion CD-ROM) is assembled into a TQFP144 package. The electrical model of the package has been performed with the use of a 3D-field solver. Fig. 5-30 shows the electrical circuit of two pins in the package. The inductive coupling between the pins is represented by current-controlled voltage sources.

Table 5-7 gives the approximate values of the passive elements of the package model. As the power supply pin pairs (linked to the cores of the circuit) are located symmetrically all around the chip, the lengths of the bondings and the leads are identical for each core.

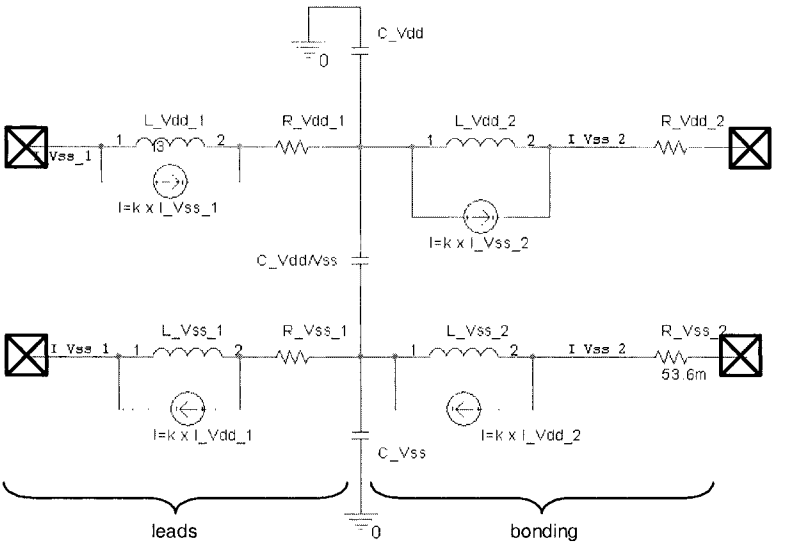


Figure 5-30. Electrical model for a TQFP144 package.

Table 5-7. Parasitic elements of the power supply network

	Inductance (nH)				Resistance (mΩ)		Capacitance (pF)	
	L1	K1	L2	K2	R1	R2	Ground coupling	C_vdd/vss
Pin vdd	6.2	0.65	6.0	0.66	56	53	0.45	0.67
Pin vss	6.2	0.65	6.0	0.66	56	53	0.45	

5. EMISSION MODELS

5.1 Introduction

The development of an emission model for integrated circuits at system level is a typical requirement. In fact, in order to ensure compliance with system-level emission standards, system EMC engineers have to compute the maximum emission level that any equipment should not exceed within the system under development. Moreover, equipment suppliers have to predict whether the noise coming from its printed circuit board is likely to meet the specifications or not. In order to perform such computations, it is necessary to identify the different noise sources in an electronic circuit. This is particularly acute in Very Large Scale Integrated Circuits (VLSI) as well as in Systems-on-Chip (SoC).

5.1.1 Physical aspects of the problem

In the electronic network of a piece of equipment or circuit board, electronic and electromagnetic energies can be represented in three different forms:

- A conducted form in which the current and its associated potential travel through wires and components,
- A near-field magnetic and electrical form, in which energy is stored in capacitances and self-inductances,
- A far-field radiative form, in which energy is radiated through electromagnetic waves.

A noisy source can therefore broadcast its energy through any of these. All kinds of energy are included in Poynting's law (Eq. 5-9):

$$\frac{\partial u}{\partial t}+\nabla.S=-J.S \tag{5-9}$$

in which (**u**) is the total energy density, (**S**) the Poynting vector, (**J**) the current density and (**E**) the electrical field.

5.1.2 Strong and weak couplings

In EMC studies, the printed circuit board, the component, the harness, the packaging and the system are often considered separately. Theoretically, it is quite easy to compute a value for each element separately and then to include this element into a system. However, this assertion supposes that adding the element to the system does not influence its own properties. For example, the output circuit of a buffer can be modeled with special-purpose software without any connected load. Then, the time-domain voltage and current on a line driven by this buffer can be computed using circuit analysis software with the previous results. However, the results may not be the same if the model of the buffer included the line itself.

The impedance of the package of an integrated circuit can be extracted by measurements using a probe. Then, the model of the package itself can be obtained by subtracting the impedance of the probe from the results. However, the true impedance of the package may be influenced by the probe itself.

In practice, it is commonly assumed that each element behaves independently and separately, and it should be possible to confirm or invalidate this by comparisons between simulations and measurements. In other cases, characterizations are performed in so-called "representative configurations", namely with realistic electrical conditions.

In the field of chip design, this approach is called "co-design", and consists in taking into account the electrical characteristics of the package during silicon design. More generally, these assumptions are called "strong" or "weak" coupling, depending on the level of independence between the elements.

5.1.3 From the package to the PCB

With the assumption of weak coupling, the analysis should characterize the noisy source separately, and then, re-use the noisy source model within a PCB schematic in order to compute the noise spreading onto the PCB.

The wide-band electrical schematic of a device is defined in a wave plane located at one of its input pins. The schematics of other devices such as capacitors and tracks will then be added to the initial schematic until the board connector is reached. In order to obtain an accurate estimation of the noise level, the schematic must often include a level-one harness model and the loads at the opposite side of the harness (what could be called a global co-design approach). Moreover, modeling the conducted emission standard often produces significant results. In this case, the harness wires to be modeled are those of the power supplies.

5.2 ICEM model

5.2.1 Introduction

The scale down of the technology increases the density of transistors per square millimeter and more complex electronic functions are embedded on silicon. With the newest technologies, analogue, digital and power technologies share the same piece of silicon. Some parts of the chip generate EMI while the others have very low sensitivities regarding the EMI level. It is an issue to ensure that all the embedded functions are able to operate (auto-compatibility or internal immunity). Table 5-8 gives an idea of the sensitivity range currently used on modern ICs. The digital activities and the number of switching IOs increase and cause huge peak current in the 10 to 50 amperes for modern VLSI circuits. Parasitic components of the package and silicon induce impedances, which increase with the frequency.

Table 5-8. Sensitivity of the on-chip analog functions

Analog functions	PLL	Analog Comparator	12bits ADC	RF
Sensitivity level	~10 mV	~1 mV	~100 µV	~10 µV

Only a few hundreds of milliohms and few nanoHenry are enough to cause critical internal voltage drops on the power distribution networks, in the 10 mV to 300 mV range. Consequently, if a part of the digital noise in transmitted to the analog functions, through the power distribution network, it will cause incompatibility problems inside and by the chip itself.

Because the technology has been scaling down, there are more transistors on-chip and the peak currents of a digital activity increases drastically. This process increases the current flowing through the wires, the packages and the PCB traces. The level of crosstalk between the PCB and the package increases in near field and the PCB traces can propagate more RF emissions outside of the PCB. It can cause malfunctions on the PCB and higher emission level in the far field. It demonstrates the necessity to have an IC EMC model to apply EMC analysis early in the IC or electronic system design stage.

Improving the first pass yield of integrated circuits and electronic equipment is one of the ultimate goals of all EMC designers. Depending on the application family, 3 to 10 runs are needed today to achieve EMC standards. On the other hand, new tools and methodologies are available to better predict the EMC criteria of ICs and electronic equipment. To do this, an IC EMC model, called ICEM, proposed by the French standardization group (UTE) is currently in the standardization process.

5.2.2 IC EMC model requirements

The IC EMC model should cover different types of EMC analysis detailed below.

5.2.2.1 IC Emission Analysis

Internal activities of IC are the main source of the conducted and radiated emissions. Fig. 5-31 shows the different origins of the radiated and conducted emissions. The conducted emissions are transmitted to the power supply network and to the IO lines. Package and die propagate the radiated emissions.

Fig. 5-32 shows one possible structural description of the IC EMC model to do emission analysis. The internal digital activities (culprit) propagate emissions to the coupling path and finally to the emission component (trace, wire and loop). A part of this emission is transmitted to the IO part via the inter-block coupling path, then to the IO terminal and finally to the emission component (PCB trace and wire). IO activities can propagate its own emission as the digital part does.

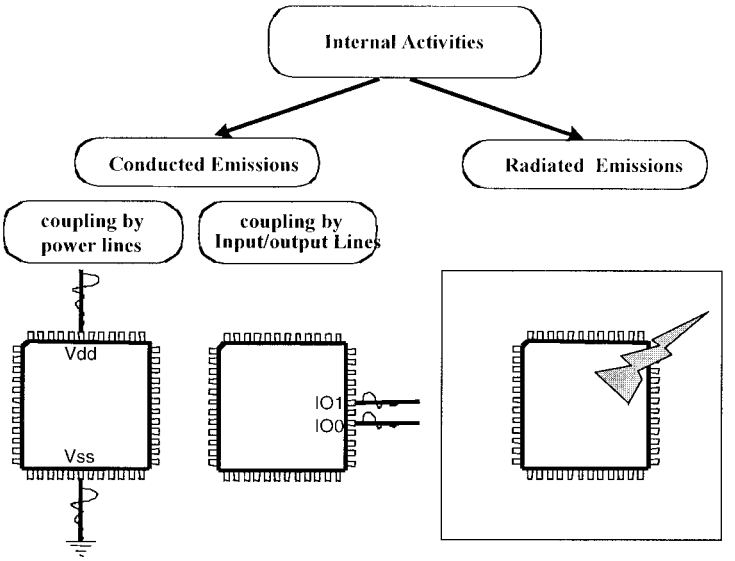


Figure 5-31. Internal activities of IC are the main sources of radiated and conducted emissions of IC.

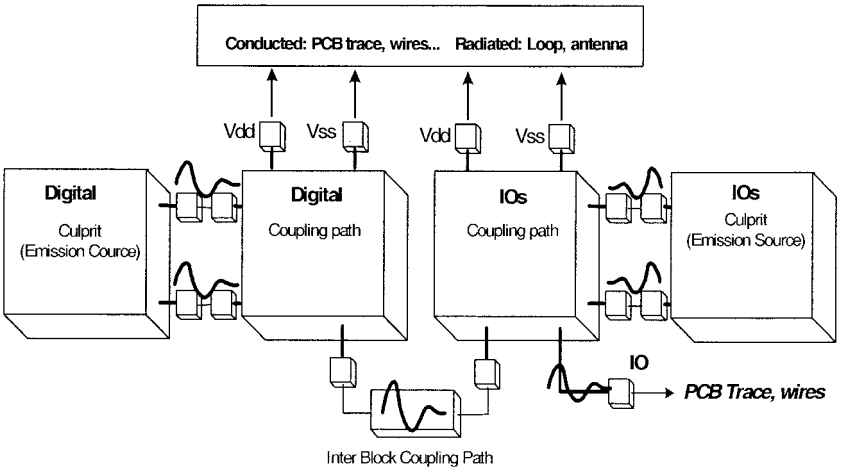


Figure 5-32. Typical IC Emission analysis using ICEM.

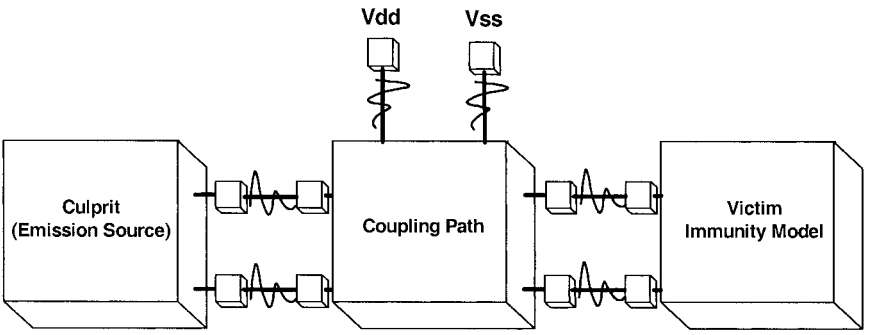


Figure 5-33. Typical approach for an auto-compatibility analysis using ICEM.

5.2.2.2 IC auto-compatibility Analysis

The auto-compatibility analysis (internal immunity) needs a description of an emission model of the emission source (culprit), a description of the coupling path and a description of the immunity model of the victim. Fig. 5-33 shows the classical concept applied to analyze an immunity issue. The internal digital activity generates emissions. These emissions are coupled to the victim (ADC, PLL, and amplifier) through the coupling path. If the level emissions are too strong, they can degrade the performance of the victim and causes auto-compatibility problems.

5.2.2.3 PCB Analysis

Thanks to the IC EMC model, the profile of the external current and the impedance seen on the terminals are well known. This information is strictly mandatory to allow the conducted and radiated emission predictions at the PCB level.

- Conducted emissions:

The power distribution network of the PCB consists of power planes, tracks, decoupling network and voltage regulator. The impedance of this network is frequency-dependent and contains several resonance and anti-resonance frequencies, which can cause out of emission specification at these frequencies. The IC EMC model allows tuning and controlling the power network impedance in the IC operation frequency range. The decoupling capacitors are currently used to stabilize this impedance. The IC EMC model allows finding, without black magic, the right values and the number of decoupling capacitors. This reduces the number of trial-and-errors usually done by the EMC designer.

- Radiated emissions:

The IC EMC model gives all the necessary information to process this analysis. Specific tools are required to do such analysis.

- Immunity analysis:

Knowing the IC EMC model and the model of the power distribution network implemented on the PCB, it is possible to analyze some immunity problems transmitted by the PCB to the chip.

5.2.3 ICEM philosophy

An IC is specified by a description called an IC architecture. This architecture describes all the functional blocks used to achieve the IC functional specification. All the internal and external connections used to connect all the IC blocks and to interface the external devices are described.

Based on this IC architecture, an IC EMC model is defined to describe the electrical and electromagnetic behavior of all the internal blocks. Fig. 5-34, depicts the concept of this model.

An ICEM model describes the EMC behavior of an IC architecture. An ICEM model is built around a set of ICEM blocks. An ICEM block is built around a set of ICEM components (IA, PDN and IBC). The structural description of each component is not the aim of this standard and it is left opened. It is not possible to cover all the cases with only one model.

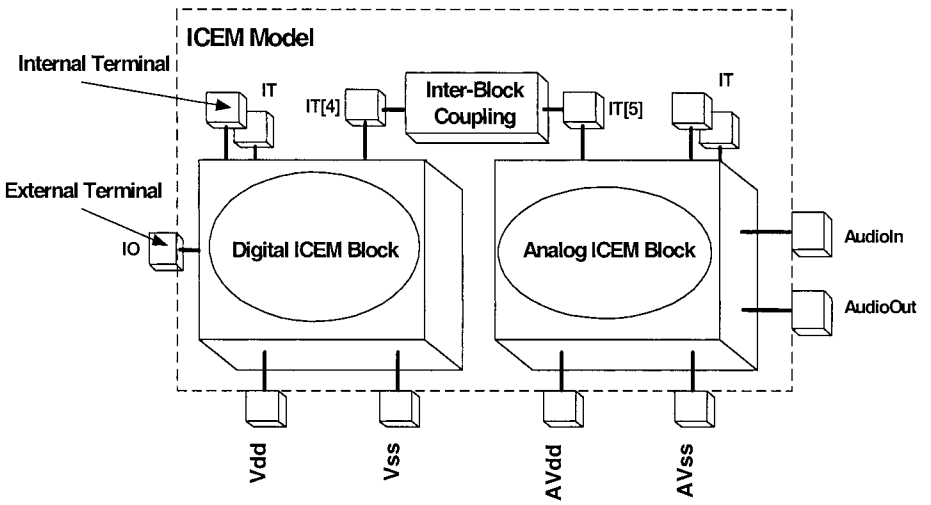


Figure 5-34. An ICEM model is built around a set of ICEM blocks.

Furthermore, the technology scales down and the frequency reaches the GHz band. The ratio between the wavelength and the velocity of the electrical signal are in the same order and the structural description will be more complex in the short-term future. As for examples, connections have to be modeled with transmission line, and the skin effect has to be taken into account.

5.2.4 ICEM description

As shown in Fig. 5-35, three ICEM components are needed to describe an ICEM block.

5.2.4.1 The PDN component (Passive Distribution Network)

The PDN component describes an impedance structure between terminals. PDN can have various forms depending on the type of analysis performed.

- Conducted analysis:

The PDN for this analysis describes impedances seen between terminals such as power-supply and I/O.

- Radiated analysis:

The PDN in that case describes an electromagnetic dipole used to model the electromagnetic field around the dipole. The radiated structure includes the package geometry or equivalent radiation source structure.

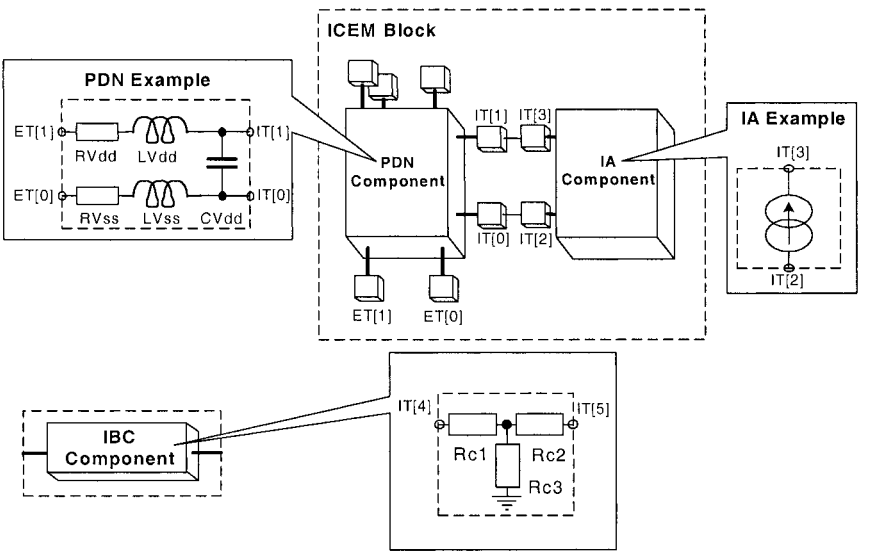


Figure 5-35. A block ICEM model is built around a set of ICEM components.

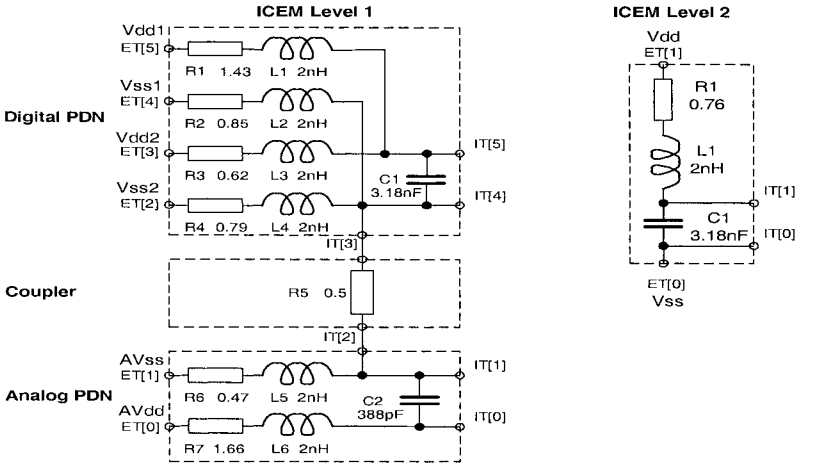


Figure 5-36. PDN component description levels.

An ICEM model has two levels of description as shown in Fig. 5-36. ICEM level 1 gives a PDN description with a lot of details about the impedance structure This view is very useful for the auto-compatibility analysis. Indeed, it is possible to access the internal power rails and measure the internal voltage drops. The level of digital noise rejection on the analog power rails can be estimated and the loss of the performances of the analog functions can be evaluated. An ICEM level 2 has a simplified view giving only a general external view of the PDN. This view is used to evaluate the decoupling network of the PCB.

5.2.4.2 The IA component (Internal Activity)

The IA component describes the internal activity of the ICEM model and has various forms depending on the analysis type.

- Conducted emissions:

The IA describes the current driven by the internal blocks. It can be expressed in time or frequency domains. Spice source components such as IPWL and IPULSE can be used to describe low complexity signals. A specific Spice source component called ISTIM can be used to download an external IA source described in a file.

- Radiated emissions:

The IA describes the electromagnetic emissions using vectors of current. Each current vector is expressed with a current module for a set of frequencies. A specific format in ASCII is contained in the standard and could adapted for the end user electromagnetic simulator. IC-EMC (IC-EMC) could be one of these tools.

5.2.4.3 The IBC component (Inter-Block Coupling)

The IBC component describes the connection between two internal terminals such as two different grounds. One example is given in Fig. 5-35. The IBC component models the linkage of the substrate between two internal ground terminals (digital IT[4] and analog IT[5] ground terminals). It can be a simple resistor or a complex impedance network.

The external and internal terminals are not ICEM components but they are just generic nodes. The external terminals allow the external devices to be connected to the IC. They are either power-supply pins or inputs and outputs pins. The internal terminals are used to connect other ICEM components such as PDN, IA or IBC, and to connect immunity models, magnetic and electric dipoles.

With these three ICEM components and a set of block ICEM models, a structural ICEM model can describe a full IC architecture. For example, IOs can be described using the PDN for the internal and external impedance and the IA for the specific activity of this port.

5.2.5 ICEM modeling process

This model can be generated either by measurements or during the design process.

5.2.5.1 By measurements

The PDN structure is extracted using a network analyzer or a time domain reflectometer. A test board is needed to measure this impedance and must be de-embedded to obtain the PDN parameters.

The measurement is performed with the use of a vector network analyzer (S_{21} parameter). This method is explained in depth in (Novak, 1999).

Fig. 5-37 plots in solid line the impedance of an IC after the de-embedding process (Levant, 2004). The dotted line represents the PDN model extracted from the measurement.

IA models the internal activity of the IC. This current cannot be measured directly. The PDN of the IC is assumed to be well known. Only the external current, *Iext(t),* can be measured (Fig. 5-38). The internal current *Iint* is then extracted in the frequency domain with the following expression (Eq. 5-10).

$$I\text{int}(f)=Iext(f)\cdot\frac{Zc+Zl}{Zc} \qquad (5\text{-}10)$$

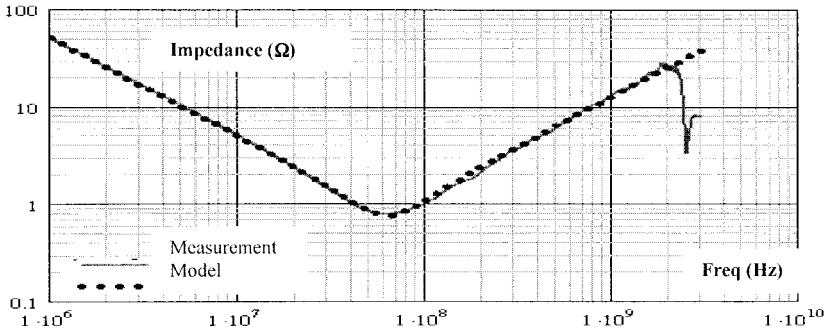


Figure 5-37. The PDN impedance after de-embedding.

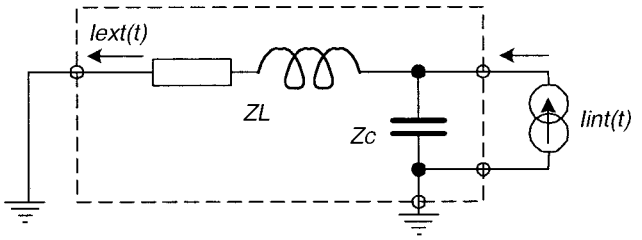


Figure 5-38. Iint(t) extraction principle.

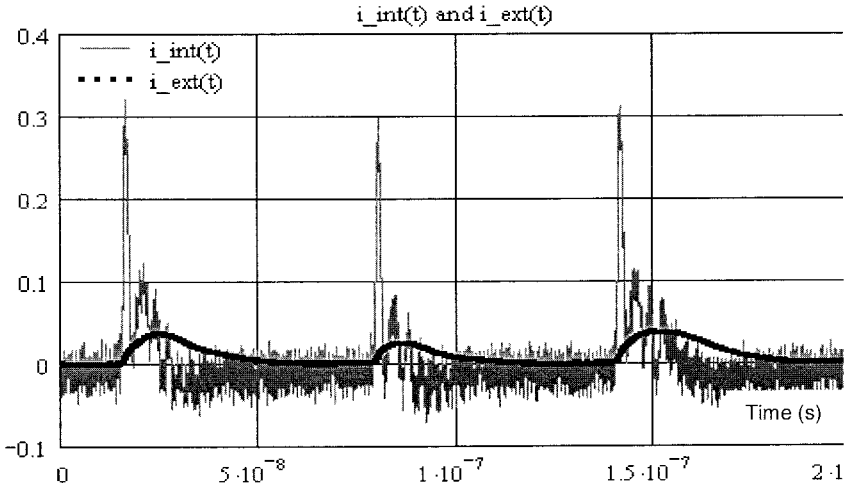


Figure 5-39. Internal and external currents.

Iext(t) is measured in the time domain. Then using a FFT, *Iext(t)* is converted to *Iext(t)*. *Int(f)* is then computed. The last step consists in applying the inverse of FFT to *Int(f)* to obtain *Int(f)*.

Fig. 5-39 plots *Iint(t)* and *Iext(t)* after applying the previous process. *Int(t)* is much larger than *Iext(t)*. Packages behave like a low-pass filter and suppress the high frequency harmonic contents.

5.2.5.2 Design process

The parameters of the PDN are extracted easily either from the package supplier data-base or using a 3D-field solver. The PDN extraction during the design phase is based on the silicon maker's experience.

The modern EDA tools allow the current consumes to be rebuilt by thousands of transistors. These new tools allow to simulate a whole IC and to analyze deeply only a part of this IC at the transistor level.

Some tools mix the VHDL, SPICE and VHDL-AMS languages which makes it possible to simulate any kind of programs and rebuild the IA component of the complete IC (see section 5-2-7).

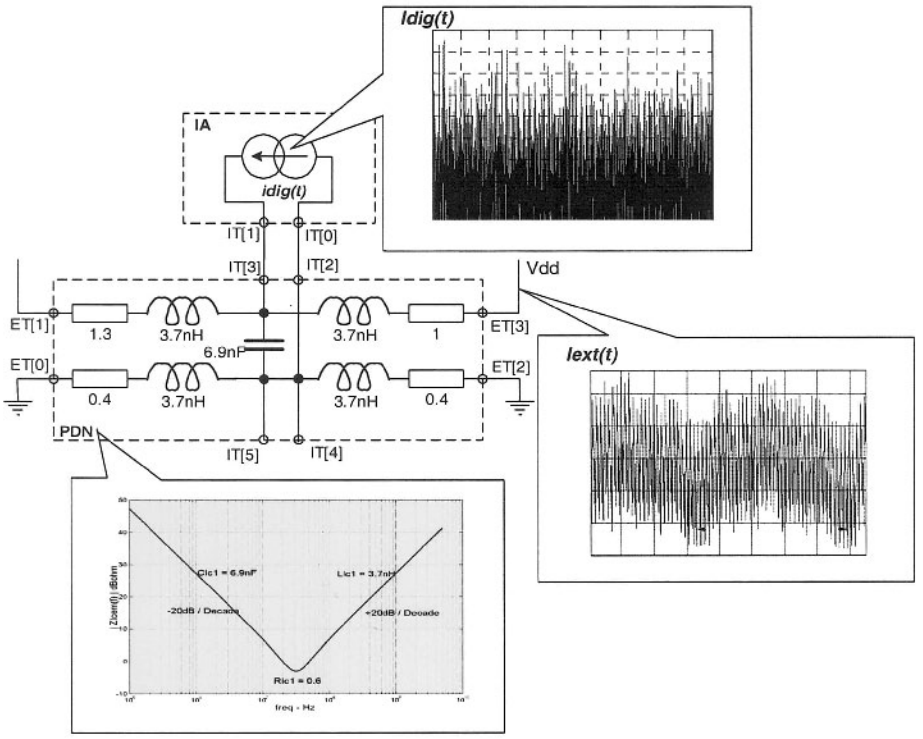


Figure 5-40. ICEM model of an 8-bit microcontroller.

5.2.6 ICEM Applications

5.2.6.1 8-bit microcontroller ICEM model

Fig. 5-40 shows an ICEM model of an 8-bit microcontroller. It has two pairs of power terminals. The IA component description is done in the time domain. The structure of PDN component is a RLC impedance plots between the Vdd and ground terminals in the frequency domain. IT[0] to IT[3] are the internal terminals used to connect the PDN to the IA components. IT[4] to IT[5] are other internal terminals used to connect parts of the IC as needed. ET[0] to ET[3] are the external terminals used to connect the power-supply. Idig(t) is the IA component.

Different analysis can be done with this model. For example, the internal power-supply IT[3] and IT[T2] can evaluate the internal voltage drops. If this voltage drop is out of specification, the number of power pins has to be adjusted or the package changed or the internal decoupling capacitor increased.

5.2.6.2 Decoupling network at the PCB level

The next example explains, thanks to the ICEM model, a methodology to define a decoupling network on a PCB. Fig. 5-41 shows a typical application using a electronic board with a microcontroller. The decoupling network must cover a wide frequency band and several decoupling capacitors have to be used to lower the impedance in the frequency band used by the IC. The value and the position for each capacitor is important. The complete study can be found in (Levant, 2005).

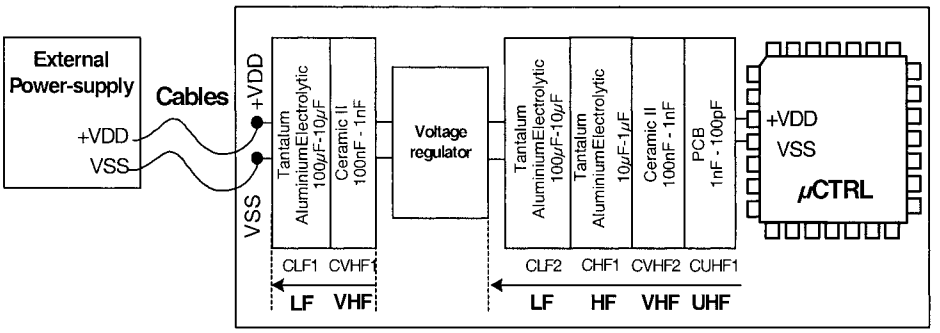


Figure 5-41. Typical decoupling network structure.

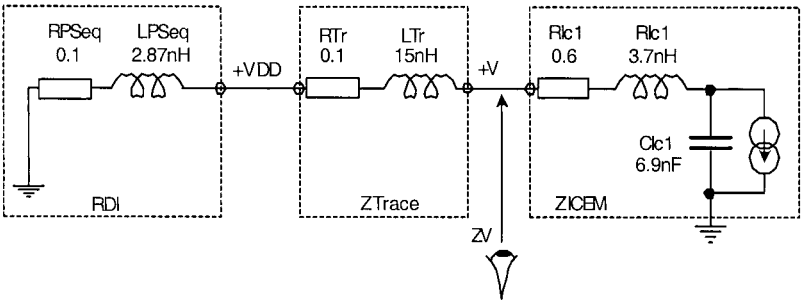


Figure 5-42. ICEM model and the power distribution model of the PCB.

In this example, only the decoupling network inserted between the voltage regulator output (+V pin) and the microcontroller is presented.

The ICEM model, once determined, is connected to the power distribution network model as shown in Fig. 5-42. The node +V is the reference point of decoupling.

The spectrum of the conducted emission (taken at +V pin) shows strong emissions at 16 MHz and at several 16 MHz harmonics (Fig. 5-43). The 16 MHz frequency is the clock frequency on the microcontroller. The first decoupling capacitor must short-circuit the 16 MHz frequency. There is a parasitic inductance L associated to the capacitor and to its connections. It is estimated at 3 nH. At F=16 MHz this capacitor constitutes a LC filter and the C_{HF} value can be determined according to Eq. (5-11):

$$C_{HF}=\frac{1}{(2\pi F)^2.L}=33nF \qquad (5\text{-}11)$$

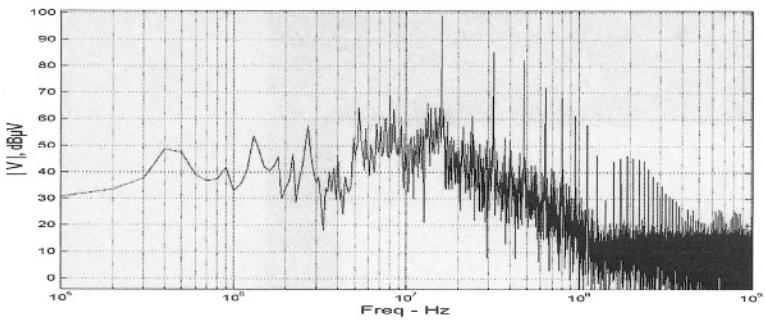


Figure 5-43. Spectrum of the conducted emission at +V.

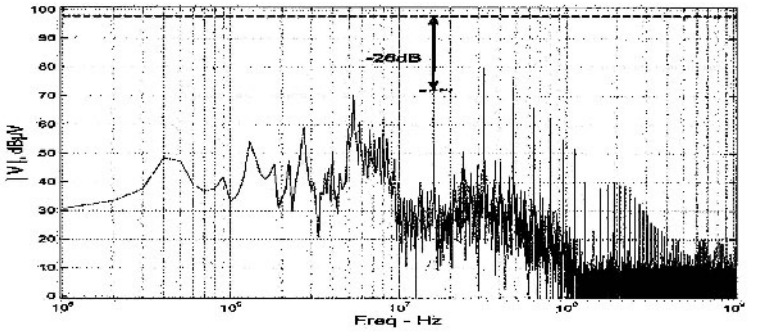


Figure 5-44. Spectrum of the conducted emission at +V with one decoupling capacitor (33 nF).

To reduce the noise level in others frequency bands, others decoupling capacitors have to be added and they can be determined in the same way. Once these frequencies are optimized and the decoupling capacitors are calculated and placed at +V pin, the conducted emission is reduced by 26 dB in frequency domain as shown in Fig. 5-44.

5.2.7 VHDL-AMS-based ICEM-IP models

5.2.7.1 Introduction

The ever increasing complexity of integrated circuits leads to a parallel increase in the complexity of associated ICEM models. Although these models can still be extracted from measurements on a sample IC, the ability to build them before chip manufacturing would shorten time-to-market and cut out NRE costs by releasing EMC-compliant ICs from the first run.

Moreover, the advent of Systems-on-Chip (SoC) is tightly bound to the use of IP[2]-based "design reuse" methodologies. In fact, these ICs are built from reusable digital or mixed-signal blocks (i.e. microcontroller cores, memories, peripherals) which are then placed and routed together, thus reducing design times and increasing reliability. Therefore, these circuits may include several millions of transistors.

It is clear that extracting the ICEM current generator of such an IC from a 2-month SPICE simulation, performed on a flattened 10-million transistor netlist, is not compatible with an industrial design flow. Therefore, a similar "design reuse" methodology can be put into practice for ICEM models.

[2] Intellectual Property

5.2.7.2 The ICEM-IP model

The corresponding methodology is based on block-level ICEM models, called ICEM-IP, which are extracted separately and then connected together in order to build the top-level ICEM model of an IC.

Such ICEM-IP models have to fulfill several requirements:

- Reduced simulation time: the ICEM simulation of a whole IC must be almost as fast as its functional simulation,
- Reusability: an ICEM-IP model has to be easy to maintain and to include into a top-level model,
- Confidentiality: the model must not reveal the technology of the corresponding block.

In addition to that, the dynamic activity of a complex block (i.e. CPU, memory) may widely depend on input signals; the ICEM-IP model of such a block should thus take into account input activity (in the current generator model).

As can be seen on the IBIS or IMIC models in the next sections, the I/Os of an integrated circuit may also generate additional conducted emission on its power supply rails. Therefore, the ICEM-IP model of a block driving I/Os has to include corresponding I/O models.

Fig. 5-45 summarizes these requirements into a proposed ICEM-IP model. Local passive devices (depending on the block-level power supply network and the block capacitance) are included. Digital inputs influencing the activity of the current generator are also clearly visible.

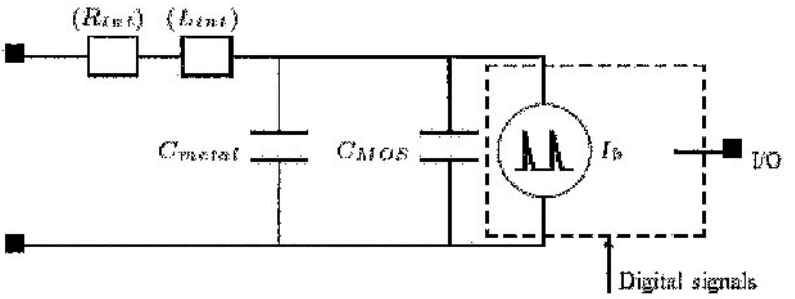


Figure 5-45. The ICEM-IP model.

5.2.7.3 Behavioral modeling: the VHDL-AMS language

The aforementioned simulation speed criterion precludes the use of the transistor netlist itself for the representation of the ICEM current generator. Another kind of modeling, called behavioral modeling, must then be used.

A behavioral model expresses the outputs of a system as a function of its inputs and of several internal "state variables", i.e. by the means of

mathematical formulae. A behavioral model can then take into account only the most important phenomena required by the application; consequently, there is always a tradeoff between simulation speed and accuracy.

Even if traditional computer languages such as C may be used, many specific behavioral modeling languages have been developed throughout the last decade, among which MAST, HDL-A, VHDL-AMS and Verilog-AMS.

VHDL-AMS (Analog and Mixed-Signal) has many advantages over other languages: it is standardized (IEEE 1076.1-1999), upward-compatible with VHDL, and modeling and simulation tools are now mature. The companion CD presents a quick overview of the language, and there are many other books and publications available (Ashenden, 2002; Hervé, 2002; Christen, 1999).

For many reasons, this language is well-suited for this application:

- Models are easy to write and read back for maintenance,
- Its upward compatibility with VHDL allows functional and activity models to be co-simulated with a unique CAD tool,
- It can be used to model digital, analog and mixed-signal blocks, even if this methodology has only been applied to digital blocks up to now,
- It is a multi-technology language, which allows non-electronic parameters to be taken into account: temperature, self-heating, ageing.

Fig. 5-46 represents an example of co-simulation between VHDL/Verilog functional models and VHDL-AMS activity models. Each block of the IC is represented by its functional model (VHDL or Verilog for digital blocks), its ICEM-IP model (VHDL-AMS), and optionally some ICEM-IP I/O models.

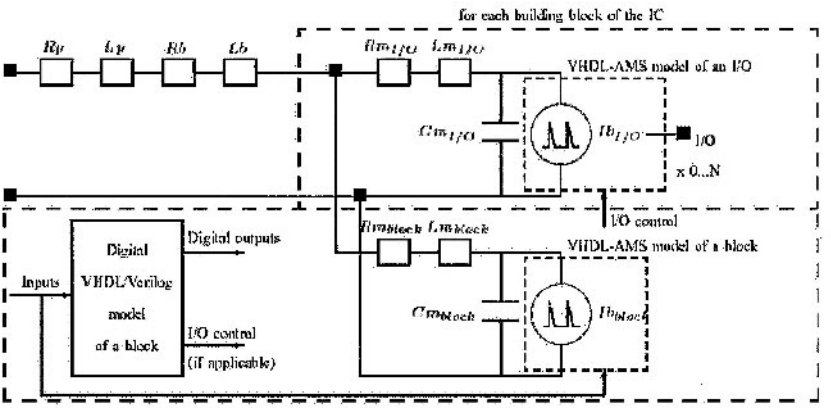


Figure 5-46. ICEM-IP-based co-simulation of an IC block.

These blocks share the same inputs, and the outputs of the functional model drive the I/O models. Provided that the ICEM-IP current generator depends on block inputs, there is thus a direct relationship between the conducted emission generated by the block and the digital activity of the block within its environment.

ICEM-IP blocks can then be combined (depending on the floorplan) to build up the whole ICEM model of the IC.

This can be used to extract best- or worst-case activities in complex ICs. A top-level ICEM model of the whole IC can then be obtained from simulation results and supplied to system integrators, including a simplified worst-case current generator including the equivalent activities of all IC blocks.

5.2.7.4 Proposed methodology for building ICEM-IP models

An ICEM-IP model, like any other ICEM model, includes a passive network and a current generator; both have to be extracted by simulation means. It should be noted that the "global" passive elements related to the package and the bonding are not addressed here; they can be characterized from measurements and then reused for subsequent designs.

Consequently, this paragraph addresses the cases of parameter extraction for the passive network, and the current generator of an internal block.

5.2.7.4.1 Passive network

The passive network of an ICEM-IP model includes the equivalent resistance, inductance and capacitance of the metallic power rails of the block as well as the equivalent capacitance of its MOS transistors. Extraction methods for package- and bonding-related elements will not be addressed here.

Distributed MOS capacitances can be modeled by a lumped capacitance. By performing an AC simulation of the current flowing into the transistor netlist of the block, the global impedance of the netlist can be extracted, including the capacitance and a parallel resistance (often negligible for emission, not for immunity).

5.2.7.4.2 Current generator of an internal block

Thanks to the lumped-capacitance approach, the dynamic current consumed by an internal block can be extracted from a transient simulation of the transistor netlist powered by an ideal voltage generator (the lumped capacitance is thus removed).

For that purpose, some VHDL-AMS-based simulation tools such as ADVance-MS© (Mentor Graphics©) are capable of integrating SPICE netlists along with digital VHDL or Verilog blocks.

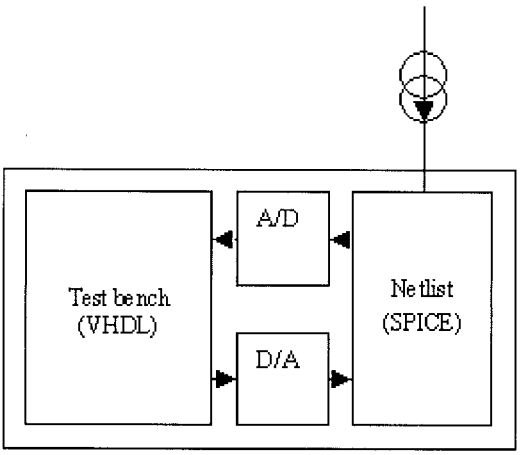


Figure 5-47. Extraction of the current consumed by a block in true operating conditions.

Both kinds of blocks are interconnected thanks to A/D and D/A converters specified either in SPICE or VHDL-AMS format (Fig. 5-47). The rise and fall times of such converters can be adjusted to match those of the physical drivers implemented on the chip.

The test bench to be used has to be chosen in order to perform the most useful characterization of the block activity. This test bench may be a digital VHDL model of another block in the circuit, reused from the digital design flow without any modification.

For example, a digital memory model may contain the code executed by a microcontroller core described at transistor level. Conversely, for example in the case of a memory block, this test bench has to be custom-written, and should allow the designer to de-correlate and characterize the activity of each internal sub-block (i.e. address decoder and memory cells). The simulated transistor netlist is then replaced by a VHDL-AMS model using the same inputs, in which the current generator is described as a piece-wise linear (PWL) waveform. The whole process is then reiterated for each block.

More precisely, it has been shown that the current supplied by the generator depends linearly on the voltage applied to its terminals. Consequently, a time-varying resistance model was chosen in the examples given in this book. In practice, this resistance is implemented in VHDL-AMS thanks to a PWL realtime linear interpolation between time/resistance points stored in two vectors.

The companion CD includes an example of VHDL-AMS code for the "conductance" generator. This code was designed to be compatible with most commercial compilers, which often do not implement the whole VHDL syntax (multi-dimensional arrays in particular); in fact, there are better

VHDL-AMS implementations of PWL generators, but they can not be compiled on the CAD tools used to validate this approach.

Moreover, it can be noted that the current profile widely depends on the rise and fall times of the "digital" inputs of the model. Therefore, these times are implemented as "generics" in the model, and their influence is taken into account in the generator. Other important design parameters, such as load capacitances on output signals, may then be implemented as generics as well.

Simulation results demonstrate the interest of such a modular approach: simulations last 3 hours with the transistor netlist and only 4 seconds with the VHDL-AMS model, and both output almost the same results.

5.2.7.5 A few guidelines for ICEM-IP usage

Once written, the ICEM-IP models representing the different blocks of an integrated circuit now have to be connected together in order to simulate the whole dynamic activity of the circuit.

In complex chips such as SoC or microcontrollers, the influence of the length of the power supply rails between the blocks is not negligible. In this case, a structural VHDL-AMS description of the circuit makes it possible to build a floorplan before the place-and-route step. By adding equivalent resistances and inductances (and decoupling capacitances) related to floorplanning, the designer may compensate for the higher emission of some blocks with respect to the others:

- By reducing interconnection resistances and inductances (namely track length), voltage drops on power supply lines, to which analog and mixed-signal blocks are often very sensitive, are reduced as well, thus improving immunity,
- Conversely, by increasing the magnitude of these parasitic elements, the voltage across digital blocks can be reduced, thus reducing parasitic emission (but at the expense of immunity).

In addition to that, this method allows the influence of the implementation of on-chip decoupling capacitors to be studied within the design flow. It can be noted that this solution is becoming more and more appropriate for EMC-sensitive, pad-limited designs.

As stated before, model accuracy can be improved by estimating capacitive loads on internal buses.

The floorplan is described as a structural VHDL-AMS model. Most of the time, this model has to be written by the designer as a source file. However, some CAD tools such as SystemVision© (Mentor Graphics©) allow VHDL-AMS models to be assembled through a graphical interface, which is more convenient.

5.2.7.6 Discussion

This paragraph introduces an innovative ICEM-based methodology for predicting conducted emission in integrated circuits before tapeout. It is based on the assembly of local "ICEM-IP" models including dynamic activities and passive power supply networks. Thanks to the VHDL-AMS language, realistic, parameter- and input-dependent activity models can be written, thus allowing the designer to study the influence of design parameters, and even design alternatives, on conducted emission for each block. This reuse-based methodology is well suited to complex ICs and facilitates the drawing up of their global ICEM models.

The reader may refer to (Perdriau, 2004) for any additional information about this methodology.

5.3 IBIS model

IBIS (Input/Output Buffer Information Specification) is a standardized format for modeling analog interfaces of digital I/O buffers. IBIS is popular because it provides the right balance between comprehensive detail and sufficient accuracy. The term "IBIS model" usually refers to the complete component description or its text file, whereas the term "model" within an IBIS file refers to one model. In printed circuit board (PCB) analysis, IBIS models enable reasonably accurate and fast signal integrity (SI) simulations. Because IBIS hides proprietary device and internal connectivity detail, it is supported by most semiconductor and EDA tool vendors. So, knowing IBIS is important.

An IBIS model is formatted as human-readable ASCII text. It is mostly based on (black-box) extracted tables versus connected structural elements as in SPICE models. SPICE models tend to be *buffer-centric*; the model often represents only one of several inputs or outputs of a buffer. IBIS models are *component-centric*; the IBIS model describes all pins of the physical component. So, IBIS models are particularly well-suited for interfacing with the component footprints of large PCB databases describing hundreds or thousands of nets.

IBIS models are developed primarily from SPICE simulation test suites or from measurements, and also with some necessary data sheet specification information for pin assignments and test data. Documents and IBIS models (ihs; IEC 62014-1; eigroup) show that the IBIS format supports nearly all of the features of existing parts. The key aspects of IBIS are highlighted to develop the framework for current and future applications.

5.3.1 IBIS Evolution

Prior to IBIS, several vendor-specific table formats and SPICE formats had already proven useful for SI analysis. Such formats helped promote vendor features, but the differences hampered wide-spread model availability. To enable more efficient model support, Intel Corporation devised its own spread-sheet format. Intel then invited several EDA tool vendors in 1993 to use this as the basis for developing a common modeling format, and IBIS evolved into its current text-based form for easier tool processing. With increasing industrial support, the group formally affiliated with the Electrical Industrial Alliance (EIA) as the EIA IBIS Open Forum. This Forum continues to promote IBIS development and standardization.

Table 5-9 summarizes milestones in IBIS evolution. Currently, IBIS Version 3.2 is standardized nationally and internationally, and work is continuing on higher versions. Some important (often free) support utilities have accelerated IBIS support. Specifically, the committee has funded parsers (up to ibischk4) for syntax and data checker checking. North Carolina State University, as part of an overall government contract, has been developing public SPICE to IBIS modeling utilities.

Table 5-9. Major IBIS version number advances with important features

1.1 Basic Model	Component pins and package
June - August 1993	Model I-V tables
	Ramp stimuli
	Typ-min-max corners
	C_comp
	Model_types
	CMOS and TTL technologies
2.1 Practical Extensions	Independent voltage references
June 1994 - December 1996	Pin mapping for rail assignments
ANSI/EIA 656	Differential pins
	Coupled package models
	Waveform tables for improved accuracy
	ECL/PECL technologies
	Terminator models
	Timing test loads
3.2 Technical Advances	Driver schedule (multi-staged, pre-emphasis)
June 1997 - April 2001	Submodels (dynamic clamps, bus hold)
ANSI/EIA 656-A	Cascaded uncoupled packages elements
IEC 62014-1	Electrical board description for boards
	Series and series switch models
4.1 Language Linkage	Submodel (fall back)
July 2002 - present	More specification detail
Standardazation planned	Multi-lingual extensions for VHDL-AMS,
	Verilog-AMS and SPICE linkage
	Possible Interconnect Model linkage

Several companies also offer free and commercial IBIS development, viewing, and checking utilities. EDA tools are emerging with multi-lingual capability for co-simulation in several languages including SPICE, Verilog-AMS, and VHDL-AMS. IBIS has added language linkages to provide a better means for expanding its capability, as opposed to continually evolving the fixed format syntax. With this linkage approach, EMI/EMC analysis (discussed later) and more advanced buffers can be handled with IBIS models.

5.3.2 IBIS Basics

Version 2.1 contains the basic elements of IBIS. Table 5A-1 and Table 5A-2 show content in IBIS files. Keywords are denoted by square brackets, and a vertical bar serves as the default comment character. Keywords can be followed by other keywords or by (what IBIS designates as) subparameters. The IBIS file contains these elements:

- **Information and Specification** content starting with a header block [IBIS Ver] and also presented elsewhere throughout the file.
- **Package** information within each of one or more [Component] blocks and under a default [Package] keyword.
- **Pin out** information within each of one or more [Component] blocks and under the [Pin] keyword giving pin-specific model references and optional pin-specific package values
- **Model** blocks beginning with one or more [Model] keywords.

IBIS has some case sensitivity and line length restrictions and a few other syntactical rules and practices, leading to a common appearance. Columns for numerical data usually follow a typ-min-max format. The typical data is always required, but minimum and/or maximum data is optional. The typ-min-max data entries are usually ordered by magnitude outside of models because they are uncorrelated. However, they are mostly grouped within a model based on voltage, temperature and process limits to describe typ, min (slow, weak), and max (strong, fast) corners. The reserved word, NA, for not available serves as a placeholder. Other reserved words are POWER, GND, and NC for power, ground and no-connect pin references.

Numerical data for a single line subparameters follow equal signs, but a text names or arguments follow white-space (spaces or tab characters). Numerical data is expressed using base units (volts, amperes, seconds, etc.) with fixed, floating and scientific notation and/or with appended, case-sensitive multiplier characters (f, p, n, u, m, (none), k, M, G, T) for femto through tera in three-decade steps. Other appended characters have no technical meaning, but are often attached to show base units.

Keywords within blocks mostly can appear in any order. Subparameters appear first in keywords, such as [Model], which scope both subparameters and other keywords. If several keywords or subparameters exist in an IBIS file and cover the same functionality (the usual case because of required defaults), then the more complex or detailed way of documenting the data overrides the simpler way. These and other rules and conventions help users locate the information and check content.

The [Model] block contains the data for electrically simulating and testing a model at the pin interface. Table 5A-2 shows the [Model] keyword followed by the Model_type subparameter. Its argument classifies the model by types including Input, Output, I/O, 3-state, Open_drain and Open_source (for open buffers), ECL, Terminators, etc. The other subparameters specify input voltage thresholds and test loads for delay adjustment. This additional information (beyond what SPICE models offer) allows EDA tools to use IBIS models to automatically check simulations against design rules.

The remaining content under the [Model] keyword describes electrical detail for EDA tool simulation. Fig. 5-48 shows the model structure with some primary blocks represented by boxes. All blocks are not always needed or applicable. For example, Input and Terminator models do not use the output buffer blocks. Fig. 5-49 shows a CMOS transistor I/O structure and corresponding blocks. Two of the four static I-V table blocks (current as a function of voltage) documented by [Pullup] and [Pulldown] keywords tabulate the transistor drive strengths. The Kpu(t) and Kpd(t) multipliers discussed later are calculated from the switching information. The diodes are documented by [Power Clamp] and [Gnd Clamp] I-V tables. These diodes might not exist in some technologies. In CMOS technology, some or all of the clamp diode currents can come from substrate P-N junctions. Other contributions can come from Electrostatic Discharge (ESD) protection circuits. Clamp currents are usually negligible in the normal buffer operating regions between the power and ground. However, clamp tables can contain currents from internal terminator resistors (usually MOSFETs) if they exist.

While these tables are often referenced to [Voltage Range] values and ground, each table can also be referenced independently, as needed by certain technologies or structures, with keywords: [Pullup Reference], [Pulldown Reference], [Power Clamp Reference] and [Gnd Clamp Reference]. Current flow directions, shown in Fig. 5-49, are based on the SPICE convention of positive flow into the interface node. Voltages follow polarity conventions based on offsets from the reference supplies to provide positive voltages in normal operating regions.

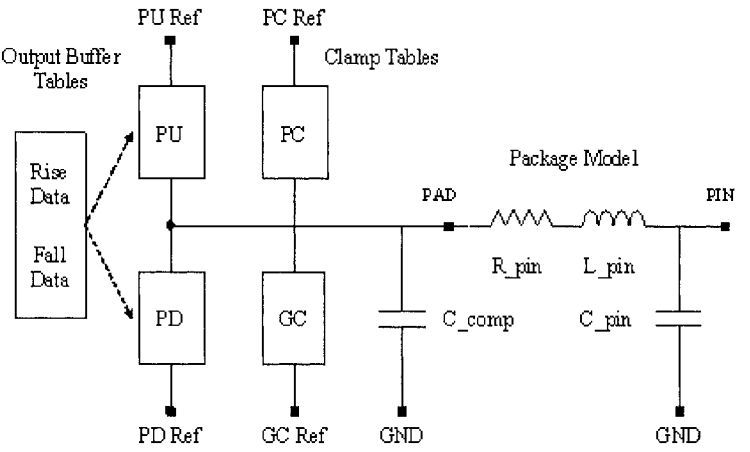


Figure 5-48. IBIS Version 2.1 blocks with pin-specific package (PU = Pullup, PD = Pulldown, PC = Power Clamp, GC= Gnd Clamp, Ref = Reference).

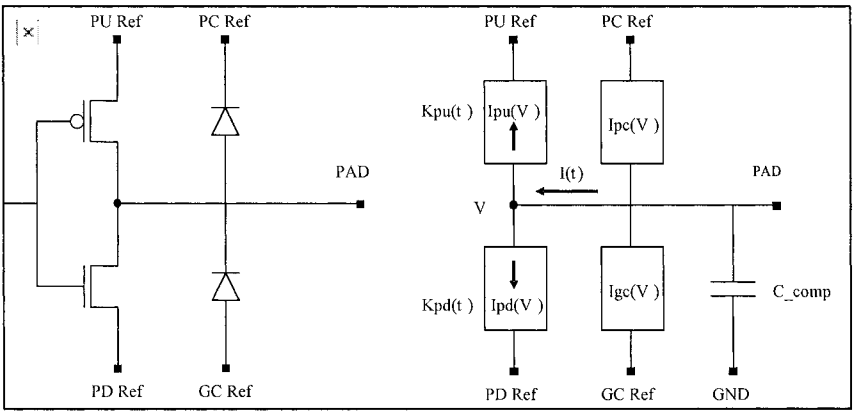


Figure 5-49. CMOS transistor output stage and IBIS block functional representation.

So, voltages in tables with the more positive voltage references are expressed by Vtable = Vpower - Vmeasured. The Rise Data and Fall Data box documents the transitions back and forth between low and high states. The [Ramp] keyword provides a default description. However, V-T tables (voltage as a function of time) under [Rising Waveform] and [Falling Waveform] keywords are recommended for better accuracy. Fig. 5-50 displays a V-T waveform for each specified fixture load condition.

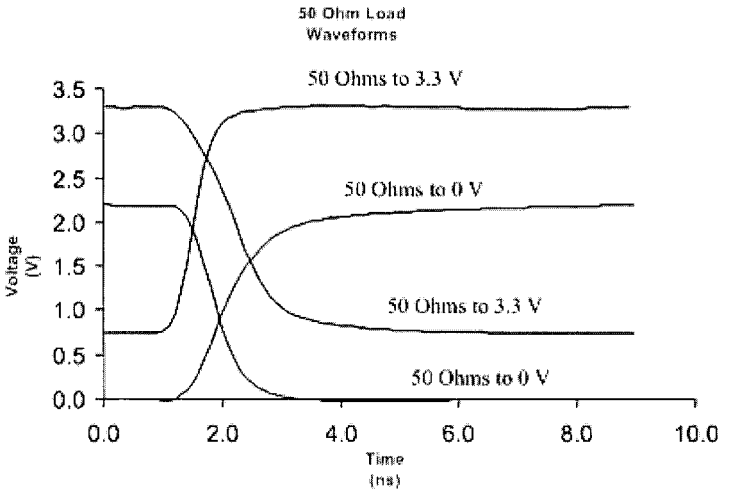


Figure 5-50. Plots of typical corner Rising and Falling Waveform data.

The buffer impedance is modeled by the static I-V slope resistance and a reactance from a single capacitor designated by the C_comp subparameter. C_comp corner values are ordered by magnitude because they can contain some uncorrelated capacitances from die metallization and other sources. This ordering contrasts with the other model corners based on voltage, temperature, and process. This basic IBIS structure along with the advances in Table 5-9 allows IBIS to support most digital I/O buffer technologies.

5.3.3 IBIS Model Processing Algorithms

Historically, EDA algorithms have been private, and IBIS continues to leave processing methods up to the EDA vendors. Fortunately, EDA tools tend to produce nearly overlaying waveform simulations with the documented IBIS waveform data. A suggested 50 ohm resistive load for extracting waveforms is consistent with PCB trace impedances in high-speed applications. Thus, IBIS simulations are well-suited for the associated SI, crosstalk and EMI analysis.

One representative algorithm uses Kpu(t) and Kpd(t) table multipliers in Fig. 5-49 for buffer switching. Fig. 5-51 shows curves of the normal operating region of I-V tables in a model, but with the measured Pullup voltages rather than its table values. The block arrows represent switching between DC low and high states along the load lines. Notice that the 50 ohm DC load line intersection voltages are also the Fig. 5-50 waveform starting and ending voltages.

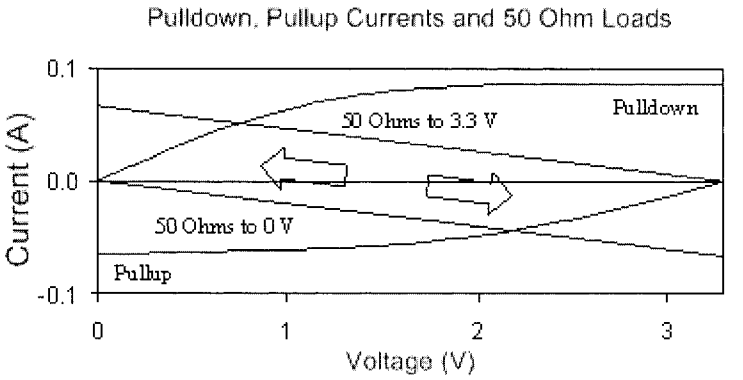


Figure 5-51. Plots of active region Pullup and Pulldown data with waveform load lines.

Buffer switching is simulated by having the multipliers simultaneously turn on one table while turning off the other over time.

The switching multipliers are calculated from currents at the I(t) position. Consider the rising edges only, and let rising edge multipliers be denoted as *Kpur(t)* and *Kpdr*(t). Two current tables, denoted as $Ir(Vr_1)$ and $Ir(Vr_2)$, are numerically calculated by EDA tools from corresponding waveforms $Vr_1 = Vr_1(t)$, and $Vr_2 = Vr_2(t)$, their fixture loads, and using the *Ipc*(V) and *Igc*(V), and $I = C\_comp*dV/dt$ currents.

This sets up two equations for the rising edge multipliers in terms of the table currents *Ipu(V)* and *Ipd(V)*:

$$Kpur(t)*Ipu(Vr_1) + Kpdr(t)*Ipd(Vr_1) = Ir(Vr_1),$$
$$Kpur(t)*Ipu(Vr_2) + Kpdr(t)*Ipd(Vr_2) = Ir(Vr_2).$$

Solving the two equations at each time step generates the multipliers. Falling edge multipliers are found in a similar manner. These time-dependent multipliers (from 0-to-1 and 1-to-0) work for any buffer load. With this approach, the initial and final waveform voltages are still determined by the I-V tables.

The multipliers can be non-monotonic and go outside of the 0-to-1 range to support undershoot and overshoot in waveforms and to supply the extra current needed to charge *C_comp*. Under recommended extraction conditions (50 ohms to ground and power) to cover the normal operation region, the multiplier model simulations match well the SPICE and physical operation for actual loads. One-transistor technologies (such as Open_drain buffers) require only one waveform table per transition. In most other cases,

a one-waveform model is less accurate because the EDA tool must make some non-physical, simplifying assumptions. However, the accuracy may still be acceptable if the buffer operates over a narrow voltage range, such as with ECL and certain differential bus technologies.

EDA tool algorithms usually include limit tests, spline fitting, and so forth to minimize numerical artifacts. Some tools even accept more than two waveforms and dynamically select waveform pairs with fixture voltages on either side of the output voltage during simulation.

5.3.4 Advanced IBIS and Future Directions

As Table 5-9 shows, the IBIS format has buffer details for pre-emphasis, switched terminators, dynamic clamps, and bus hold. These syntactical extensions are based on additional controlled current structures. However, to avoid continually adding new fixed format structures to IBIS, the Open Forum has added multi-lingual links in IBIS Version 4.1 to SPICE or standardized code. So, advanced models can be called directly from external code rather than require new IBIS keywords and subparameters.

The multi-lingual extension also provides an IBIS wrapper for exploring and supporting some emerging methods for handling more variables. Potentially, such methods can encode mathematical simulation models based on more parameters and many conditions (loads, power supply voltages, temperatures, etc.) for better accuracy over a wide range of operation.

5.3.5 IBIS and ICEM

ICEM descriptions presented in external code can also be linked to IBIS. Four new keywords describe the main elements of the IBIS multi-lingual extension. Links to external code are documented by the [External Model] and [External Circuit] keywords for external digital I/O models and general types of on-die circuitry (passive and active). On-die and interface pin connections are documented by the [Node Declarations] and [Circuit Call] keywords. Most of the ICEM details can be handled by [External Circuit] and [Circuit Call] keyword references and calls to external code.

For example, Fig. 5-52, and Fig. 5-53 illustrate attaching an ICEM core noise generator to power and ground pins. Table 5A-3 shows portions of IBIS multi-lingual additions for ICEM. IBIS already documents the package details. The SPICE model consists of equivalent on-die power distribution network with Cd, RVDD, LVDD, RVSS, LVSS, and Cb elements, and a statistically derived periodic current generator Ib for internal clocking. Core currents can drive PCB traces and simulate the resulting emissions.

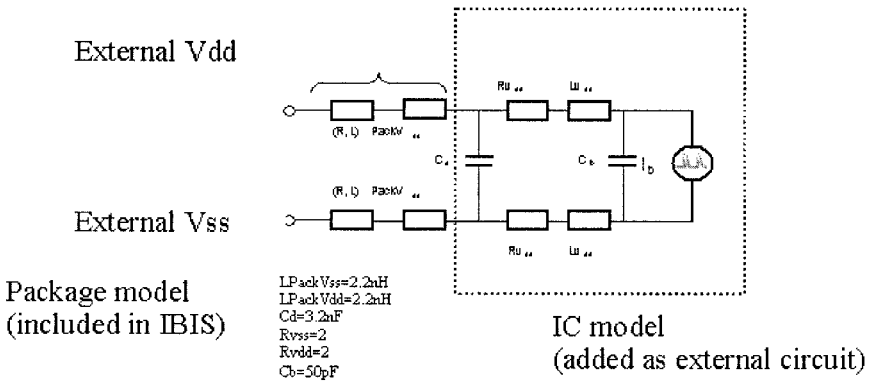


Figure 5-52. 68HC12 D60 ICEM model.

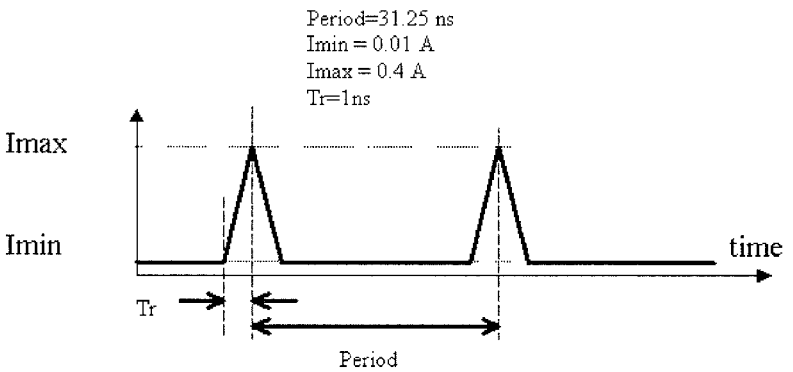


Figure 5-53. ICEM Current generator.

As discussed in ICEM, equivalent networks interacting with buffers can also be modeled by using more buffer and power bus connections.

While the IBIS format is still evolving, IBIS and ICEM potentially can provide a common industrial format for EMC simulations.

5.4 IMIC model, an I/O Interface Model for Integrated Circuits

5.4.1 Introduction

IMIC (I/O Interface Model for Integrated Circuits) (EIAJ ED-5302) was developed and standardized by JEITA. Simulations of signal integrity, power integrity and conducted EM emission are possible using IMIC. It features hierarchical model structure, tabular device model for non-linear devices and net-list circuit description with waveforms. Those features provide analytical interface models that show good accuracy in simulation results and protection of proprietary information.

Simulations have become indispensable in board designs. IBIS V. 3.2 (IEC 62014-1, 2001) was standardized for this purpose as an IEC standard in 2001. IBIS has been making a substantial contribution to electronic industries.

But, frequencies of electronic systems have been drastically increasing, and for this reason, semiconductor makers are sometimes required by their customers to prepare more accurate I/O models.

One candidate that can achieve good accuracy is the SPICE model. But the SPICE model contains proprietary information such as process information, device information and circuit information, so it is difficult for IC venders to provide IC users with SPICE models.

On the other hand, IMIC can achieve almost the same accuracy as the SPICE model and can protect IC venders' proprietary information. Although IMIC was originally intended for signal integrity and power integrity, it is applicable to conducted EM emissions.

5.4.2 Structure of IMIC

Fig. 5-54 shows the hierarchical structure of IMIC. The hierarchy consists of three levels of model such as module model, IC model and package model. Those three models are described in a unified way. In a simulator the module model refers to the IC models, and the IC model refers to the package model just like procedure call of software. The module model also can refer to other modules.

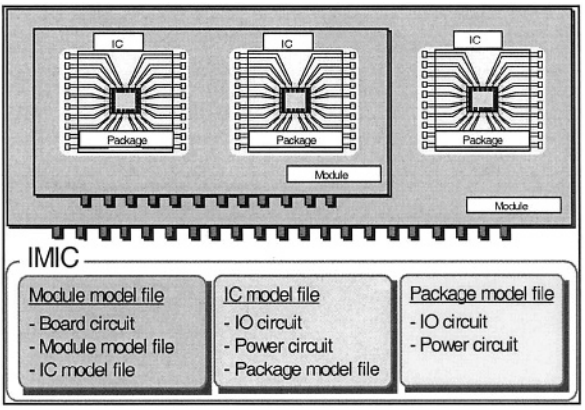


Figure 5-54. Hierarchical Structure of IMIC.

This hierarchical structure provides the following advantages:

- Users can easily recognize pins and signals at which they aim, because outer terminals and signals of each model are clearly defined in each model.
- IC makers and package makers can provide IC models and package models, respectively, because each model is independent from each other except for the part that defines their relationships.

With using all models of three hierarchical levels, users can simulate whole board systems in block.

5.4.3 Netlist Circuit Description with waveforms

The circuits in each hierarchical level are described using the extended SPICE format. Inductors (self and mutual), capacitor, resistor, and non-linear elements such as MOS transistor, bipolar transistor and diode can be used. Wide variety of voltage sources and current sources are also supported.

Fig. 5-55 is an example of circuit description that contains two output buffers. In this example, the output buffer is defined as a sub-circuit. Thus, the amount of description can be reduced. IC venders can easily make models because the models are described in popular SPICE format, and IC venders usually own the net-list because IC venders have to make the net-list in the course of IC development. Complicated circuits can be easily described using net-list.

One of the major aspects of the circuit description is waveform. Waveforms can be defined and be assigned to circuit nodes. Waveform appears similar to Piecewise Linear in SPICE, but PWL is fitted in net-list.

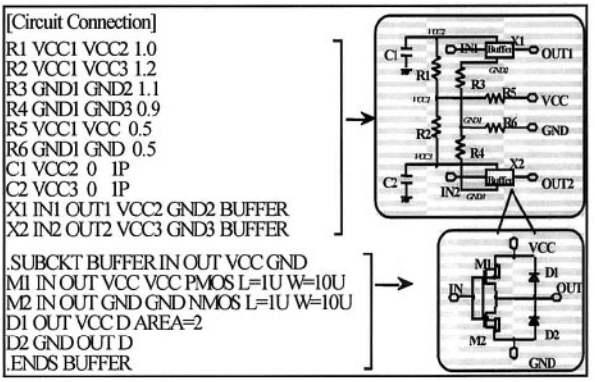


Figure 5-55. Circuit Description using Netlist.

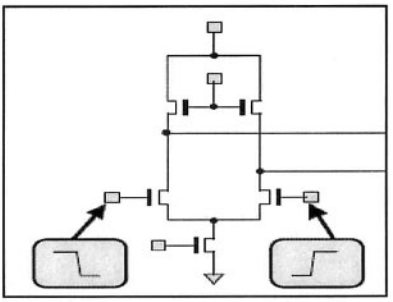


Figure 5-56. Differential Buffer using Waveforms.

This means PWL is normally on. On the other hand, the waveforms in IMIC are controlled by a simulator. Fig. 5-56 shows an example of a differential output buffer using waveforms. The waveforms are defined and assigned to the input nodes of output buffer.

Those features of the circuit description provide following merits.

- Easy to make models
- With using waveforms, it is not necessary to describe pre-buffers and this can reduce the proprietary information disclosure of circuit description.

Users can easily simulate various kind of combination of output buffers' switching by setting the simulation conditions. And there is no need for IC venders to make each net-list for each combination of switching.

5.4.4 Tabular Device Model

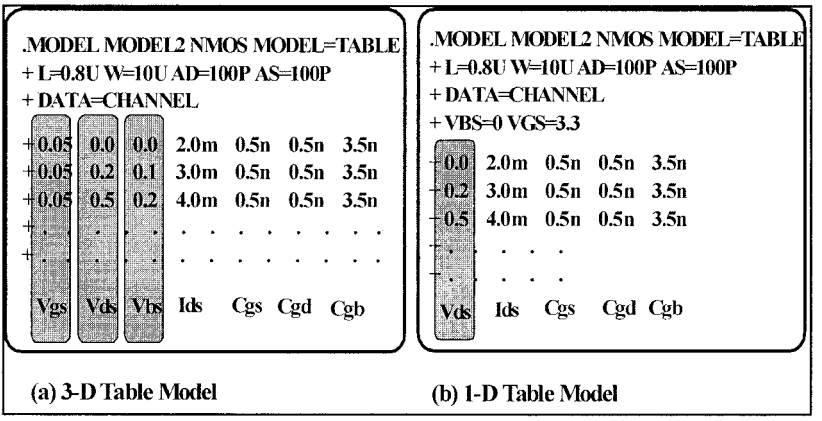


Figure 5-57. Tabular MOS Device Model.

BSIM is widely used in SPICE simulations. But, the parameters of BSIM contain proprietary process information. A non-disclosure agreement is typically required to obtain these from a vendor.

In IMIC, the non-linear devices such as MOS transistors, bipolar transistors and diodes are modeled using tabular format that consists of sets of parameters that are independent variables and dependent variables. In tabular models, the independent variables are terminal voltages and the dependent variables are current and capacitances. According to the number of independent variables, there are three types of model such as 1-dimensional, 2-dimensional and 3-dimensional model. The tabular device model is a main feature of IMIC, and IMIC is called "Table SPICE".

Fig. 5-57 (a) is an example of 3-dimensional tabular device model of a MOS transistor. This table has three independent variables such as Vgs, Vds and Vbs. Fig.5-57 (b) is a device model for a switch MOS transistor. In this case, Vgs and Vbs are constant. If any parameter has the same value in every set of numbers, the parameter can be removed from every set of numbers. As a result, the characteristics of this switch MOS can be described as a 1-dimensional tabular model with an independent variable of Vds.

Thus, disclosure of proprietary information of process parameters can be greatly reduced.

5.4.5 Level of Model

The level of the model is set according to the purpose of the simulation. The relationships between the level and the purpose of simulation are indicated in Table 5-10. The level-1 is to analyze signal integrity, and the level 2 is to analyze power integrity and conducted EM emission.

The models of level-2 should contain descriptions of power and ground line circuits in each model. The load to simulator of this level is usually heavy, since the models of this level contain large size of L, C and R. Some kind of physical models may be helpful to this level.

For the simulation of conducted EM emission, macro models for core circuits are crucial. IMIC does not support any specific physical core models. But, physical core models such as ICEM (IEC TR62014-3) and LECCS (Fukumoto, 2001) can be easily described using net-list.

The Level-3 is to analyze direct EM emission. The current version of IMIC does not support this level, and Level-3 is a future task. Structures and materials need to be defined.

Table 5-10. Level of Model

Level	Object	Simulation
Level-1	Signal Integrity	To analyze signal waveform
Level-2	Power Integrity and Conducted EM	To analyze Power/ Ground bounce and conducted EM
Level-3	EMI	To analyze Direct EM emission (Future work)

5.4.6 Simulation results

Applied Simulation Technology Inc. provides a commercial simulator that can operate IMIC. And "Aichi Institute of Tech." developed software (Nakamura, 2004a) that converts IMIC format into popular HSPICE format. Using this software, IMIC can be operated by HSPICE simulator.

This section shows some simulation results of IMIC model compared with SPICE model. The DUT is 16-bit Buffers / Drivers with 3-state Outputs.

5.4.6.1 Signal and Power Integrity

Fig. 5-58 shows the simulation results of signal integrity. The output signal of package pin is simulated under the condition of correspondent buffer switching. The load of the output pin is a transmission line. The results of SPICE simulation are also shown in the figure. The simulation result of IMIC model is almost equivalent to the results of SPICE simulation.

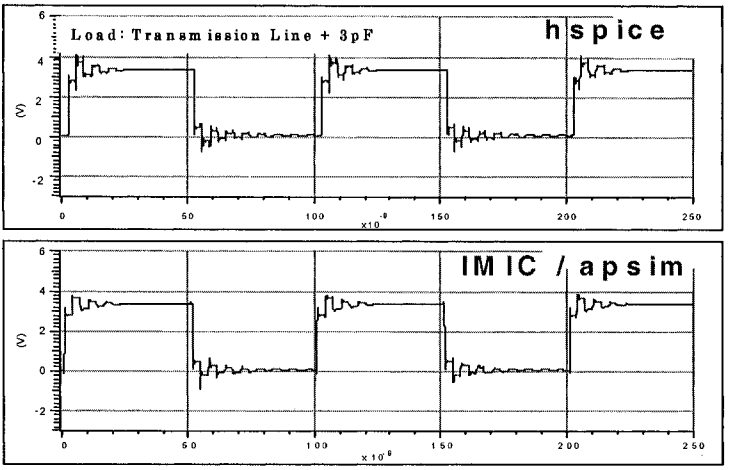


Figure 5-58. Results of Signal Integrity simulation.

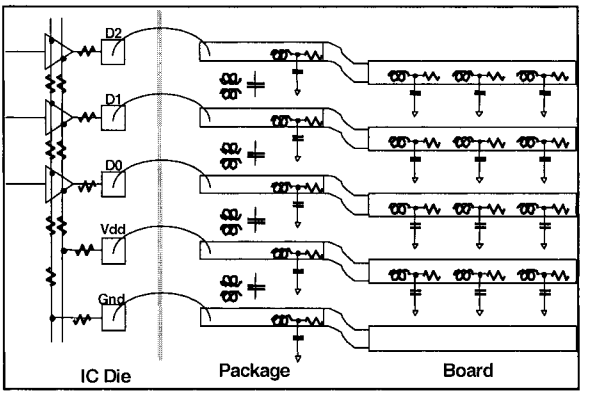


Figure 5-59. Circuit Model for PI Simulation.

The circuit for power integrity simulation is shown in Fig. 5-59. The LCR networks describe the package and board. The simulated result is shown in Fig. 5-60. In this figure, the simulated waveform of un-operated output pin is shown under the condition of simultaneous switching of 15 buffers.

5.4.6.2 Conducted EM

Conducted EM emission of I/O activity can be simulated whether with the use of tabular device model or by using physical model.

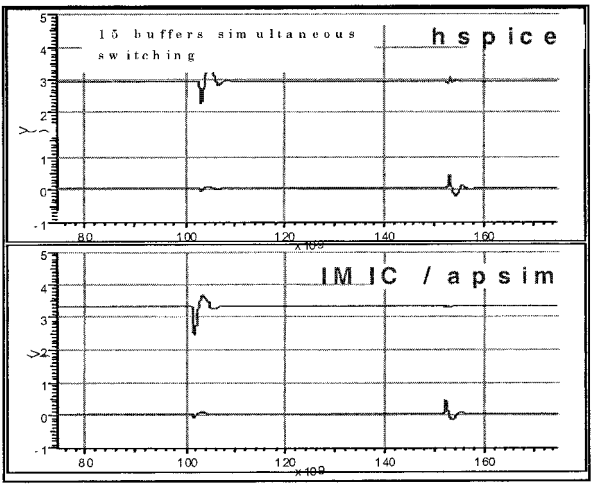


Figure 5-60. Results of Power Integrity Simulation.

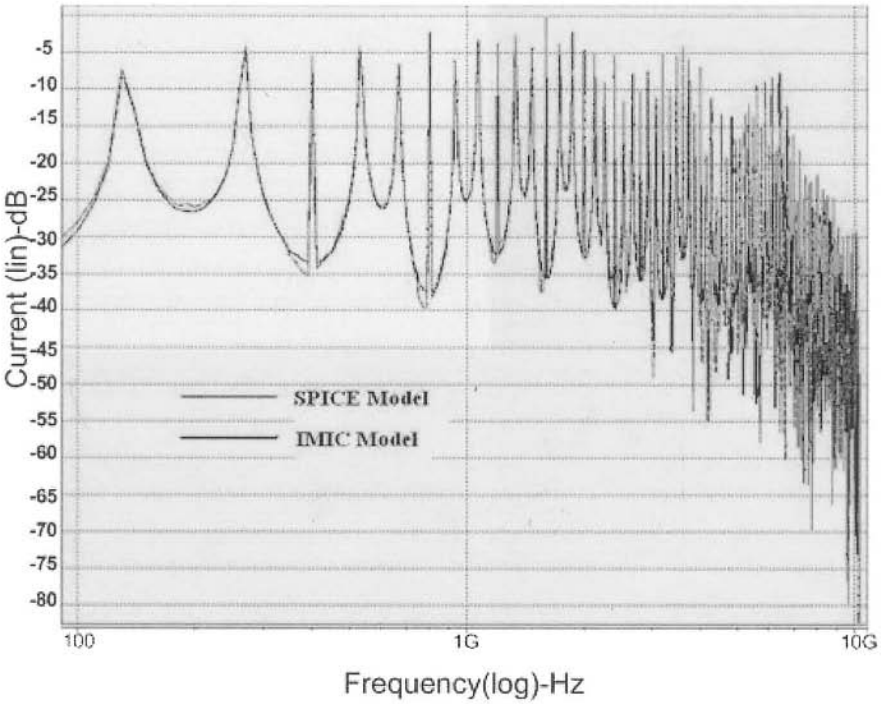


Figure 5-61. Conducted EM Emission of Power Line.

Fig. 5-61 shows the results of conducted EM emission of the power line. In this case, DUT is operated at 133 MHz and the load of output pin is small capacitance to confirm the difference of noise in a high frequency region. The results of simulations indicate that the tabular device model shows almost the same accuracy in simulations as SPICE. IMIC does not specify any physical macro models for EM simulation. But physical models such as ICEM or LECCS can be easily described using IMIC format. Therefore, IMIC can operate simulations using physical models.

Fig. 5-62 shows the structure of IC model file of IMIC that describes physical model. The DUT is a single-chip microcomputer, and the model consists of three noise sources (Ichikawa, 2004): a digital core, an analogue core and IO. These sources are modeled using LECCS models. The die parts of LECCS models such as noise current sources and L, C, R in the die are described in "IC model file" itself, and the package circuits are described in "Package model file."

Fig. 5-63 shows the result of simulation using IMIC model compared with SPICE model. These two results completely agree with each other. The physical model does not contain any non-linear element; therefore, the difference between IMIC and SPICE is only the description format. IMIC can act as a container of physical macro models for conducted EM emission.

As mentioned above, IMIC model shows almost the same accuracy as SPICE model in simulation results of SI and Conducted-EM emission (and also PI). In addition, IMIC can completely protect process and device information and greatly reduce the disclosure of circuit information.

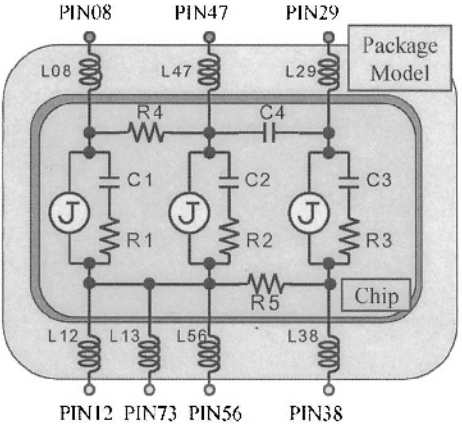


Figure 5-62. Structure of IC Model File.

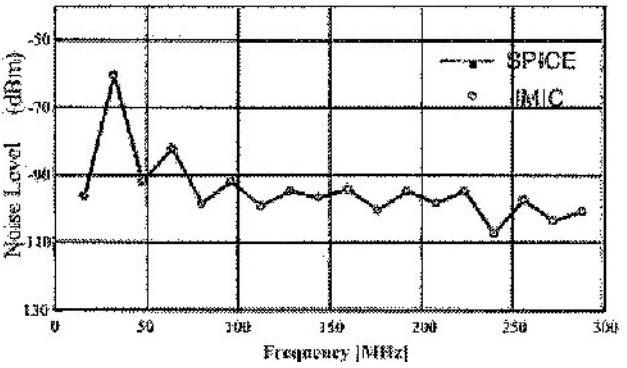


Figure 5-63. Simulation Result Using Physical Model.

5.5 LECCS models: Linear Equivalent Circuit and Current-Source models

To achieve fast EMI/EMS simulations of digital devices and printed circuit boards (PCBs), an EMC macro-model for digital ICs/LSIs has been developed that was named the the LECCS[3] model. The model was originally proposed to evaluate the RF noise current on a power pin of a core logic circuit (*LECCS-core*) (Takahata, 1999; Wada, 2000; Fukumoto, 2001). Some groups in Japan, ones at Okayama University, Hitachi Ltd. and DENSO Corporation, developed similar models (Fukumuto, 2002; Ichikawa, 2004; Nakamura, 2004a; Mabuchi, 2005). Each model consists of linear equivalent circuits (LEC) with *R*, *L*, and *C*, and internal equivalent current sources (CS). They have been applied to practical ICs/LSIs to simulate and control RF power current of devices. At Okayama University, the LECCS-core model was combined with a swift electromagnetic field simulator for the power-bus resonance simulation of a PCB, which was implemented as HISES[4] software, and the decoupling characteristics were evaluated with good accuracy (Wada, 2003; Koga, 2004; Takayama, 2003). The LECCS model was later extended to a model for devices that have output drivers for high-speed I/O (*LECCS-I/O*) (Osaka, 2004a; Osaka, 2004b; Osaka, 2004c).

[3] LECCS: Linear Equivalent Circuit and Current Source.
[4] HISES: High Speed EMI Simulator

5.5.1 Linear device models for EMC simulations

CMOS digital ICs consist of a number of p-MOS and n-MOS transistors. Each of them has, of course, nonlinear switching characteristics, and its impedance varies in accordance with its evolution of switching operation. However, most of the noise characteristics are related to certain resonance phenomena of the PCB and device impedances, and most of the noise appears as a combination of dumped oscillations. The switching duration of each transistor is as short as sub-nano seconds, which is short enough when compared to the time constants of the noise current. Therefore, most of the noise characteristics of the device under test (DUT) can be expressed by linear macro-impedance models such as the one shown in Fig. 5-64, and the macro impedances, including a chip and package, can be evaluated from the outside. So, the equivalent circuit of linear impedance is practically applicable and accurate enough for EMC simulations.

LECCS models consist of linear equivalent circuits (LEC) combined with equivalent current sources (CS) that express the internal noise source caused by the switching operations of the transistors. Two types of LECCS models have been proposed, the LECCS-core for the internal core logic circuit and the LECCS-I/O for the output buffer circuit (Fig. 5-65). Fig. 5-64 shows the most simplified LECCS-I/O model for a CMOS driver.

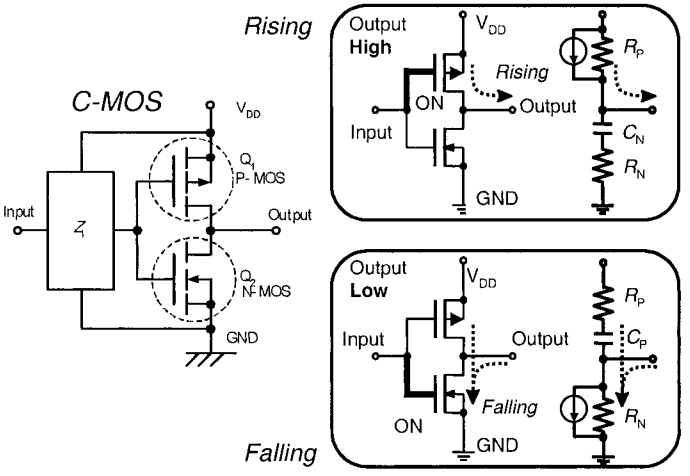


Figure 5-64. Macro-impedance modeling of CMOS digital IC with linear circuits.

5.5.2 LECCS-Core model

Initially the LECCS-core model was a two-terminal model having a power and a ground terminal. The internal LEC parameters were determined by impedance measurement or simulation, and the calculation from the measured power current and the internal and external impedances in the frequency domain derived the CS spectrum. It is composed of a linear equivalent impedance, Z_i, and an internal equivalent current source, I_i, as shown in Fig. 5-66. Both of these values were derived from the direct measurements of the device (Takahata, 1999; Wada, 2000; Fukumoto, 2001). The device model provides the RF current in the power pin of an IC/LSI as the noise excitation source. The LECCS model for core circuits has the following features: (1) All the model parameters can be determined by measurements, so there is no need to consider the internal design parameters. Of course, the parameters can also be derived from a SPICE model of the device. (2) The internal current source is determined from the measured current spectrum. The standard measurement method for an RF current spectrum is described in international standards IEC 61967-6 and IEC 61967-4 (IEC 61967-6, 2002; IEC 61967-4, 2002).

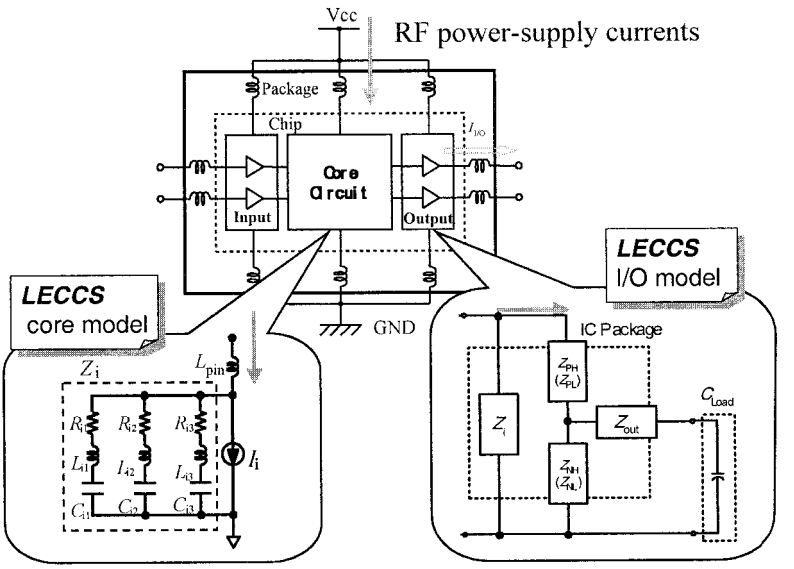


Figure 5-65. LECCS-core and LECCS-I/O models.

(3) The model can express RF noise characteristics of the power current of an IC/LSI. The effects of decoupling capacitors on a PCB or of on-package and on-chip decoupling capacitors can be evaluated (Wada, 2003; Koga, 2004; Takayama, 2003). This was demonstrated during the design process of a microprocessor (Tsujikawa, 2002). (4) Although the model is linear, its accuracy is sufficient enough for EMI/EMS simulations. The LECCS-core model was applied to simulate EMI from practical PCBs and good agreements between the simulation and measurements were achieved (Koga, 2004; Takayama, 2003). The results include decoupling simulation with on-package and on-board capacitors, and EMI simulation with a power-bus resonance model of a multi-layer PCB.

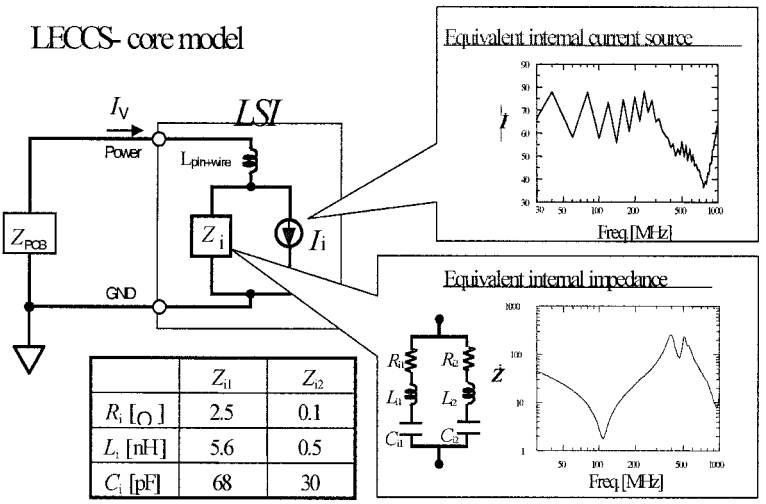


Figure 5-66. Example of two-terminal LECCS-core model.

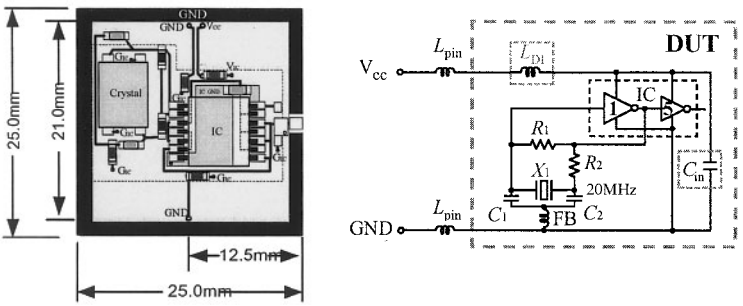


Figure 5-67. IC module to demonstrate power decoupling and its equivalent circuit.

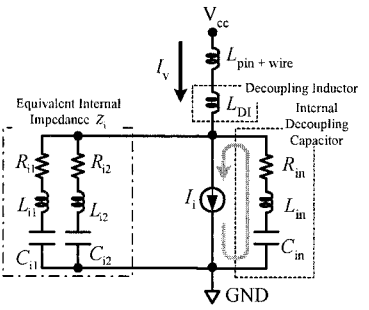
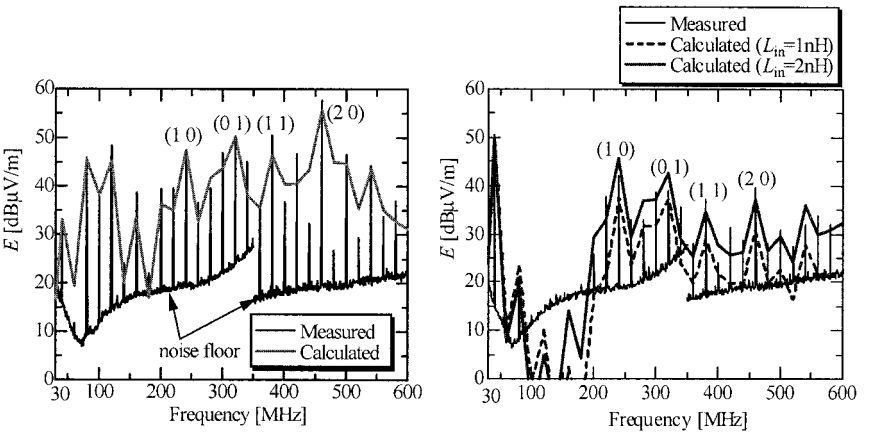


Figure 5-68. LECCS-core model of IC module with decoupling elements.

To validate the LECCS model for core circuits, an evaluation module was designed (Wada, 2003; Takayama, 2003), which is called the "IC module" here (Fig. 5-67). The IC module consists of a CMOS six-inverter IC (74LVC04, SSOP) and a crystal oscillator on a 1-inch-square four-layer PCB with some passive components. It was designed for evaluating the internal power decoupling technique on a package. As shown in Fig. 5-68, the operation current, I_i, of the IC is supplied from either the DC power supply of the PCB or a bypass capacitor mounted close to the IC. The high-frequency (RF) component of the power current, I_V, drives the power and ground planes in the PCB and causes EMI. If the RF current is bypassed by introducing an internal decoupling capacitor, as shown in Fig. 5-67 and 5-68, the EMI can be reduced. Moreover, if inductance is added, L_{DI}, in series with a power-pin connection, as shown in the figures, this also suppresses the RF current. The IC module includes pads for the internal decoupling capacitor, C_{in}, and the internal decoupling inductor, L_{DI}.

An IC module and a battery module have been mounted on an evaluation board (320 mm x 235 mm, FR-4) having rectangular power and ground planes. The radiated emission has been simulated and measured in a semi-anechoic chamber (Wada, 2003; Takayama, 2003). Fig. 5-69 shows the simulation results with and without the internal decoupling, in which some emission peaks related to circuit and power-bus resonances were observed. The simulated EMI spectra corresponded with the experimental results within 6 dB, which illustrates that the linear equivalent circuit model is quite accurate and effective for EMI simulations. A very small parasitic inductance was observed, such as a trace inductance of 1 nH, could affect the results and make a few decibels of difference. In Fig. 5-69 (b), different calculated results with two different values for the internal decoupling inductance, L_{DI}, is plotted.



(a) Without decoupling (b) With decoupling (C_{in} = 1000 pF)

Figure 5-69. Power decoupling; simulated and measured EMI spectra.

Recently the LECCS-core model was extended to a multiple power-supply pin LSI (Ichikawa, 2004; Nakamura, 2004b). When an LSI has multiple and electrically well tied power and ground pins, a two-terminal LECCS-core model is applicable for power current simulations. However, practical PCBs, particularly most of single- or two-layer PCBs, do not always have low enough interconnection impedance. Therefore, the connection impedances between the pins in a package and on the board have to be expressed.

Fig. 5-70 shows one example of the extended LECCS-core model used by research groups at DENSO Corporation, Hitachi Ltd. and Renesas Technology Corporation (Ichikawa, 2004). Fig. 5-71 shows a simulated power-current spectrum with multiple power-supply and multi-current models in comparison to a single source model. Using the extended LECCS-core model, the power current was accurately simulated. The difference of conducted emission levels was also accurately simulated for different locations of the decoupling capacitors on a practical two-layer PCB.

Linear equivalent circuit and current source models of LSIs were developed aiming at swift anticipation of electromagnetic noise emissions. Electromagnetic field emissions from printed circuit boards were evaluated using the LECCS models. Accuracies were experimentally examined and their effectiveness in the application of EMC designing was proven in simulations of conducted and radiated emission and immunity (see immunity section). The value of these models will increase with the increased sharing of these interfaces between other models and CAD tools that is now under way.

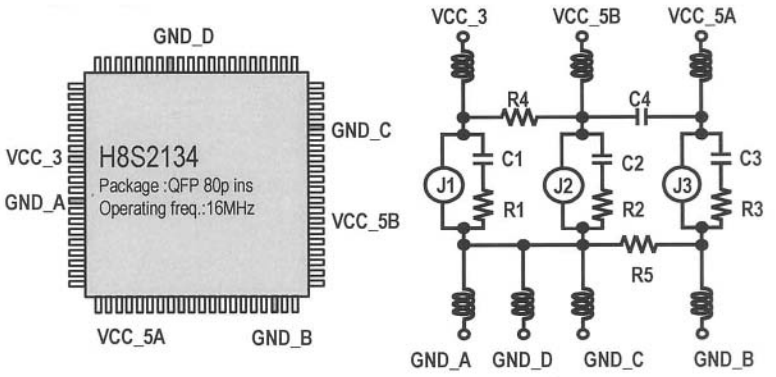


Figure 5-70. LECCS-core model for H8S/2134 (Renesas, 16-bit Microcontroller) (Ichikawa, 2004).

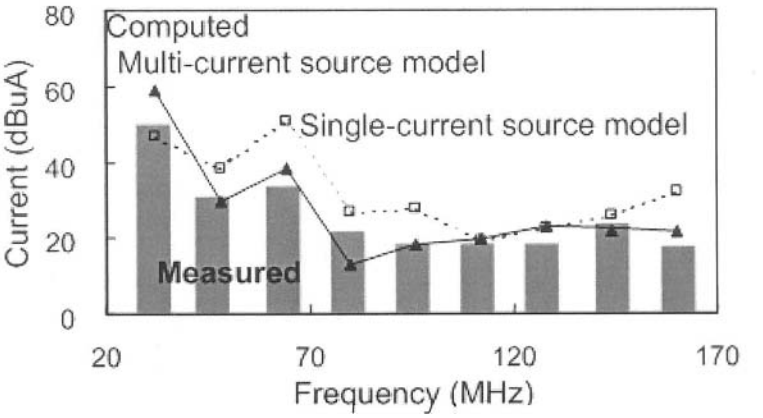


Figure 5-71. Comparison between single and multi-current source models (Ichikawa, 2004).

6. INPUT/OUTPUT MODELS

6.1 Introduction

The increasing complexity of integrated circuits has lead to a corresponding growth in the number of I/Os. In today's advanced technology (90 nm and below), it is common to have chips with more than one thousand switching I/O buffers, which can cause emission problems.

To evaluate the I/O activity and its interactions with the core, there is a need to add an I/O model to the ICEM-core model. As can be seen in section 5.3, IBIS is dedicated to signal integrity and it can not be used for noise studies just as it is. But, an I/O model in SPICE based on IBIS data can easily be developed and adapted for conducting emission simulations. In this part, a methodology is presented for establishing a buffer model from IBIS information.

LECCS-IO corresponds to other well-suited emission models which will also be presented.

6.2 I/O block description

The I/O block can typically be divided into three main parts:

- an inverter or a buffer composed of nMOS and pMOS transistors which are sized to give a sufficient drive to the signal,
- clamp diodes to protect the circuits from electrostatic discharges,
- a pad capacitance to which the package model can be added.

Fig. 5-72 shows the output structure according to the IBIS model. Although IBIS describes each part of the I/O block in detail, it provides only $I_d(V_d)$ tables for active devices and the characteristics of transient state transitions defined with output buffers connected to arbitrary loads. This representation is inadequate for conducted emission studies. Indeed, the load can change and, consequently, the transient state transition characteristics are not valid. Moreover, the perturbations on power and ground supplies are widely dependent on the voltage applied to the gates. So, it is necessary to use a dedicated emission model, derived from IBIS, but taking into account the particularities of noise studies. The model has the same structure as IBIS, but it replaces the $I_d(V_d)$ characteristics by their equivalent analog components.

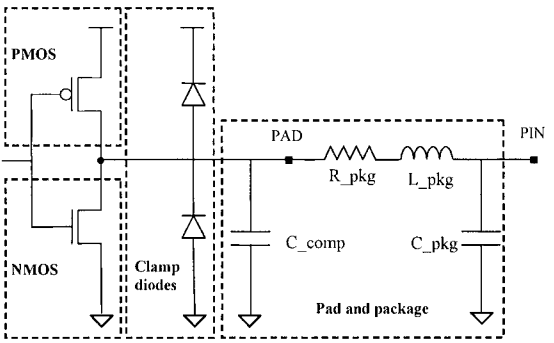


Figure 5-72. Output stage representation according to IBIS.

6.3 Buffer model

Different methods for extraction and simulation of transient behavioral models of state transition of digital I/O buffers were proposed by (Peivand, 1996; Wang, 1999). Their models use Piecewise Linear generators to represent the equivalent current or voltage sources described in the IBIS model. Another solution is to reconstruct an analog SPICE circuit from IBIS. To achieve this, the $I_d(V_d)$ tables are used to evaluate the sizes of nMOS and pMOS transistors.

The DC characteristics of the driver must be fitted to the IBIS data. An inverter circuit with nMOS and pMOS devices is used, and a level 3 model (Fig. 5-73, 5-74, 5-75). The MOS channel length is fixed to the minimum technology size, and fits the width in order to match the IBIS information. The tool IC-EMC (IC-EMC) offers an IBIS translator, which helps to compare the $I_d(V_d)$ tables to the transistor simulation. The analog simulation is performed in the time domain by a SPICE simulator such as WinSpice (Winspice).

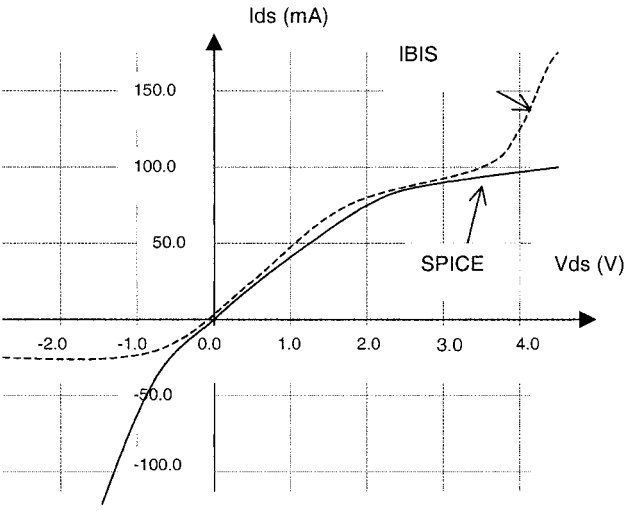


Figure 5-73. Fitting DC Id/Vd characteristics between IBIS and nMOS level 3.

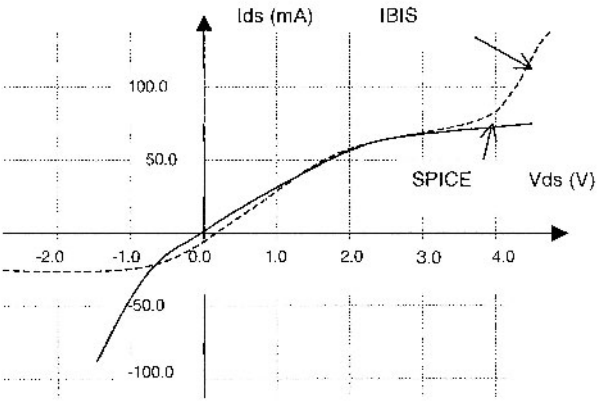


Figure 5-74. Fitting DC Id/Vd characteristics between IBIS and pMOS level 3.

6.4 I/O block model

Once the equivalent buffer has been defined, the passive network, including package, PCB and load capacitance information, is added to the buffer model. Fig. 5-76 gives an example of an I/O block model. The clamp diodes are not taken into account in this representation because it is only necessary to study the I/O block in standard activity without electrostatic discharge.

```
MN1 3 2 7 3 MN W=90u L=0.35u
MP1 5 2 7 5 MP W=60u L=0.35u

.MODEL  MN  NMOS
+ LEVEL=3              TPG=+1
+ GAMMA=0.2            THETA=0.5          KAPPA=0.1          ETA=0.002
+ DELTA=0.0            UO=620             VMAX=100E3         VTO=0.35
+ TOX=2e-9             XJ=0.1U            LD=0.00U           NSUB=1E+18
+ NSS=0.2              NFS=7E11           RD=1               RS=1
+ CJ=4.091E-4          MJ=0.307           PB=1.0
+ CJSW=3.078E-10       MJSW=1.0E-2
+ CGSO=3.93E-10        CGDO=3.93E-10

.MODEL  MP  PMOS
+ LEVEL=3              TPG=-1
+ GAMMA=0.2            THETA=0.5          KAPPA=0.01         ETA=0.001
+ DELTA=0.0            UO=250             VMAX=500E3         VTO=-0.35
+ TOX=2E-9             XJ=0.1U            LD=0.0U            NSUB=1E+18
+ NSS=0.0              NFS=7E11           RD=1               RS=1
+ CJ=6.852E-4          MJ=0.429           PB=1.0
+ CJSW=5.217E-10       MJSW=0.351
```

Figure 5-75. MOS level 3 model parameters.

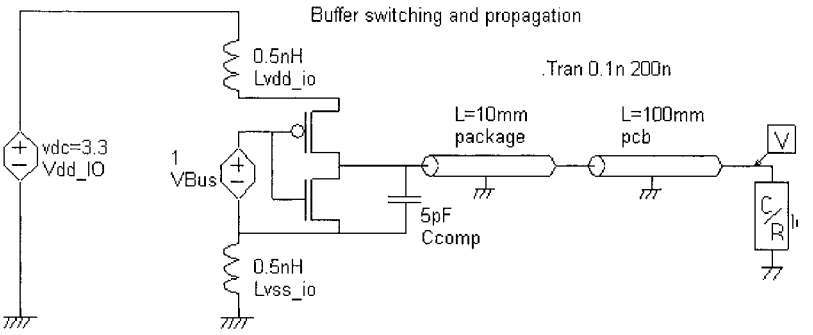


Figure 5-76. I/O block model representation.

To study the dependencies between the core and the I/O block, the analog I/O SPICE model can be simulated with the ICEM-core model. This can be achieved either by connecting the supplies in the case of a common power network, or by including a substrate resistance that links the logic Vss and the I/O Vss.

6.5 LECCS-I/O MODEL

LECCS model is also applicable for I/O modeling. RF noise on a power-supply connection of the output buffers strongly depends on the output loads. Normally a device having an external output has multiple buffers (Fig. 5-77). The LECCS-I/O model was proposed to express the variation of the RF power current dependent on the external output load of the drivers. Two quasi-static (H or L) states were separately modeled with a set of linear equivalent circuits as shown in Fig. 5-65. For practical simulation, the above two models were combined into one (Fig. 5-78), and the total power current was simulated.

When the LECCS-I/O model is compared with the LECCS-core model, they can be defined as follows: the LECCS-core model describes the electrical characteristics of the internal blocks of an LSI or IC with no global I/O interconnection, and the LECCS-I/O model describes the characteristics of blocks having external I/O interconnections.

For example, a six-inverter IC (74LVC04) was modeled and simulated (Osaka (2), 2004; Osaka (3), 2004). Fig. 5-79 shows the comparison of the measured and simulated current waveforms on the power pin; the rising and the falling waveforms were simulated with the 'output-high' and 'output-low' models, respectively.

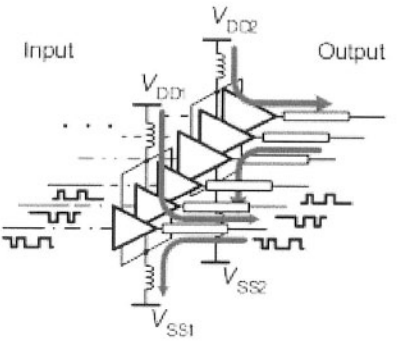


Figure 5-77. Output buffers with multiple-outputs.

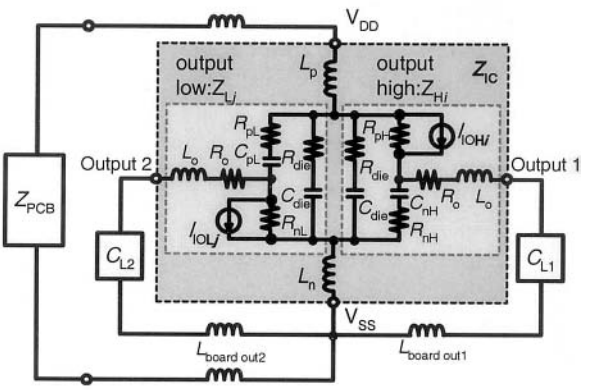


Figure 5-78. Equivalent circuit of multi-bit LECCS-I/O model.

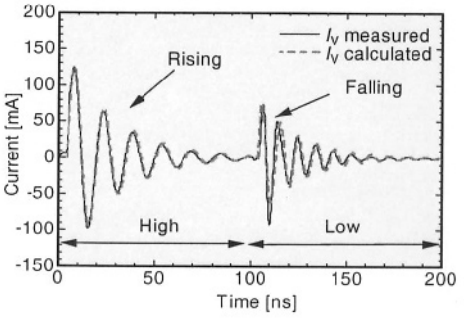


Figure 5-79. Time-domain simulation of LECCS-I/O model.

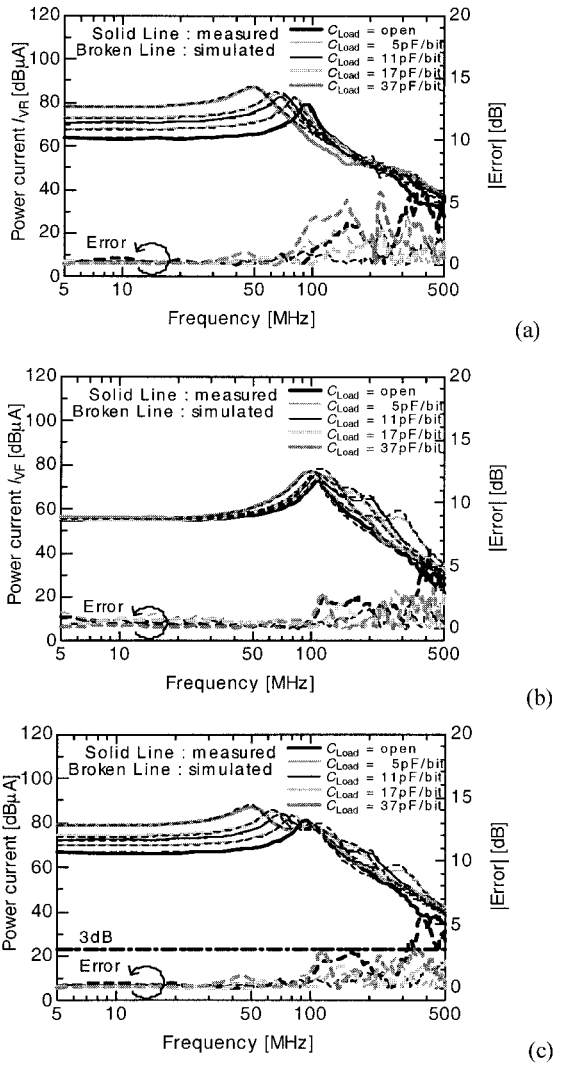


Figure 5-80. Noise current spectra and its simulations with LECCS-I/O model (a) Rising, (b) Falling, and (c) Total current spectra.

The frequency of the dumped oscillation and its Q-factor can be calculated as the resonance characteristics observed from the internal current source that depend not only on the DUT impedance but also on the impedance of the external circuit. Fig. 5-79 shows the results for single-bit switching. For simultaneous switching of multi-bit outputs with different bit patterns and different output loads, simulated results for the combinations of

the 'output-high' and the 'output-low' states will be superimposed. In order to obtain the spectrum of the RF noise on the power current, the waveform was transformed to the frequency domain with FFT. The evaluation of the impedance of die and core logic circuits was also reported, which is shown as R_{die} and C_{die} in Fig. 5-78, is important in order to obtain accurate results of the simulations (Osaka, 2004). Fig. 5-80 shows the comparison between the measured and simulated RF current spectra (DUT: 74LVC04). Fig. 5-80 (a) is the variation of the spectrum of the rising current, and (b) is that of the falling current for output load capacitance open to 37 pF/bit. Combining these current spectra, the total current spectra shown in (c) is obtained, which expresses the variation of noise current peaks accurately dependent on the output condition.

7. IMMUNITY MODELS

7.1 Introduction

The immunity model needs to be predictive, so that the manufacturer can simulate the chip's behavior before sending it to for production, while remaining simple enough to keep simulation time to a minimum and to facilitate integration of the model into the stream of design tools. Furthermore, for immunity measurements made in the laboratory based on the direct power injection (IEC 47A/526/NP, 2001) method, the proposed integrated circuit immunity model will be defined in the frequency range from 1 MHz up to 1 GHz in conducted mode. In this section, the elements of the proposed immunity model for integrated circuits are described. The simulation setup and the criteria of susceptibility within the framework of a simulation are proposed. The case of internal immunity is also discussed.

7.2 Description of the elements of the immunity model

Since the integrated circuit emission model (ICEM) (IEC, 2003) used for the simulation of parasitic emissions gave interesting results, a similar development path to set up the immunity model for components is used. Furthermore, the frequency bandwidth covered by the ICEM model being identical to that covered by the DPI method, the physical description of elements could be made by means of RLC parameters. Consequently, the passive electrical elements described by the ICEM model, namely the package model and the internal power supply network of the integrated circuit were retained.

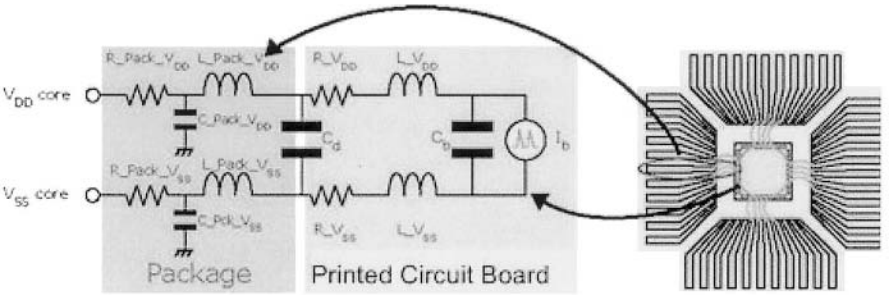


Figure 5-81. ICEM model reused for simulating component immunity.

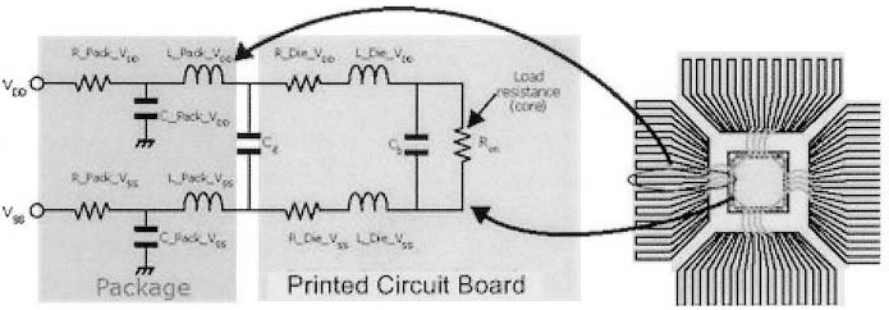


Figure 5-82. Integrated circuit immunity model.

As illustrated in Fig. 5-81, the integrated circuit immunity model reused the passive elements of the ICEM model. The electrical elements of the model are directly linked to the physical dimensions of the component, to the on-chip capacitances and to the power supply network.

Immunity simulation is relatively different to parasitic emission simulation. One consequence is that a current generator is no longer necessary. On the other hand, from the point of view of the radio frequency (RF) generator, the IC's core is perceived as a load. Consequently, the current generator is replaced, in a first approximation, by a resistance load as shown in Fig. 5-82. This resistance is included in the range of 10 Ω to 100 Ω for a 16-bit microcontroller core.

This model can be completed with additional circuits as necessary. During injection of RF disturbances on an input/output, additional care must be taken. To this end, the manufacturers have developed structures to protect integrated circuits against electrostatic discharges (ESD). These surges can cause deterioration or even destruction of the thin layer of gate oxide. For this reason, two protections among those most frequently used will be described: clamp diodes and coupled gate NMOS transistors.

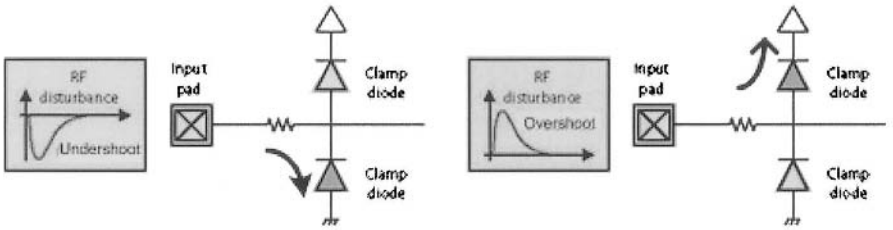


Figure 5-83. Input protection by clamp diodes.

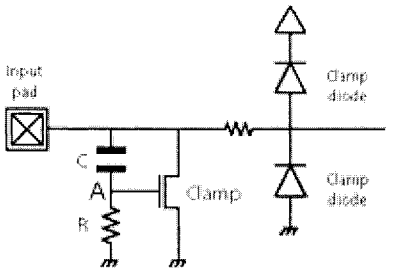


Figure 5-84. I/O protection by coupled- gate NMOS transistor.

The clamp diode device consists of a resistance and two diodes which precede the first element input stage (Fig. 5-83).

The resistance is generally in poly-Si or in N-well, with a value between 10 Ω and 1 kΩ. The main role of the resistance is to limit the voltage injected into the I/O transistor gate. In the case of a poly-Si resistance, the thickness of the poly-Si layer determines the value of the maximum current which can be driven.

In nominal functioning, the clamp diodes play no role because the input voltage will be between V_{SS} and V_{DD}. On the other hand, if a strong under-voltage (left part of Fig. 5-83) appears, the lower clamp diode is going to begin driving and thus injecting the disturbance towards the substrate. In the case of a surge (right part of Fig. 5-83), it is the upper clamp diode which drives the aggression into the V_{DD} power supply network.

The coupled-gate NMOS transistor described by Dabral (Dabral, 1998) and illustrated in Fig. 5-84 is relatively advantageous for protecting integrated circuits against electrostatic discharges. The elements which make it up are distributed in two stages. The first drives the largest part of the current towards the substrate, whereas the second stage will take care to evacuate the rest of the RF aggression. Such a device turns out to be effective even for surges of several kilovolts (5 – 7 kV).

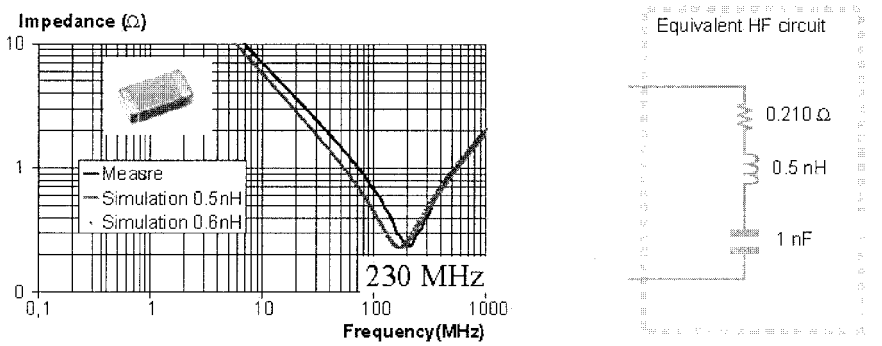


Figure 5-85. Equivalent coupling capacitor.

The I/O RC circuit acts as a high-pass filter: point A is by default at V_{SS} because the resistance R pulls it down. Consequently in nominal functioning, the transistor NMOS is blocked and the device inactive. The appearance of a very rough surge is going to come to couple on this node A and force the NMOS transistor to enter conduction. Therefore, the main part of the current is going to cross this transistor to be forwarded to the substrate of the component. As long as the surge does not reach a weak enough level, the transistor of the clamp continues to drive. The return to normal thus occurs relatively to the decline of the surge.

In the case of the immunity simulation of integrated circuits, the injected disturbance is supposed to be of a large enough amplitude to activate these protection devices. It is therefore necessary to model them which can amount to replacing the active components with a resistance. In the case of the clamp diodes, it is necessary to consider the diode which can drive because both cannot drive simultaneously. Considering the coupled gate NMOS transistor, the R_{ON} resistance is sufficient.

The elements of the printed circuit board must be modeled, and more especially the 1 nF coupling capacitor. This capacitor not being ideal (Giacotto, 2003), a 0.5 nH series inductance is associated with it as Fig. 5-85 illustrates.

7.3 Simulation setup

The prediction of the immunity behavior of an integrated circuit is more difficult than the parasitic emission simulation because it requires the definition of a failure criterion. It also needs considerable post-processing that must be in agreement with the chosen failure criterion.

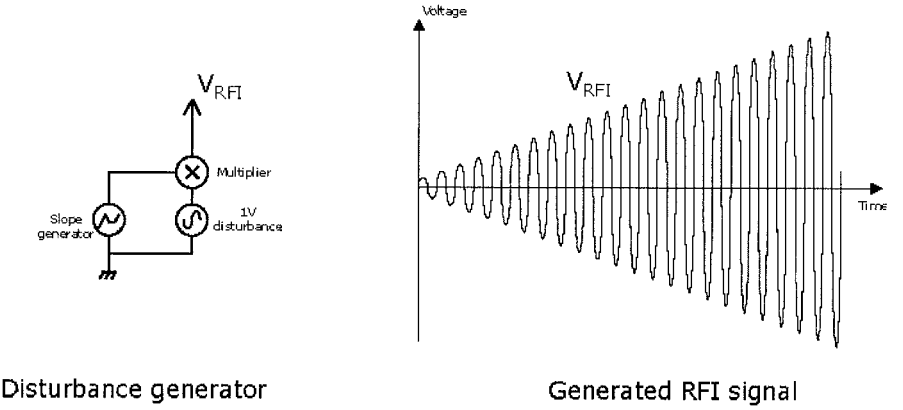


Figure 5-86. Example of RF disturbance generator under SPICE tools (left part) - Obtained output signal (right part).

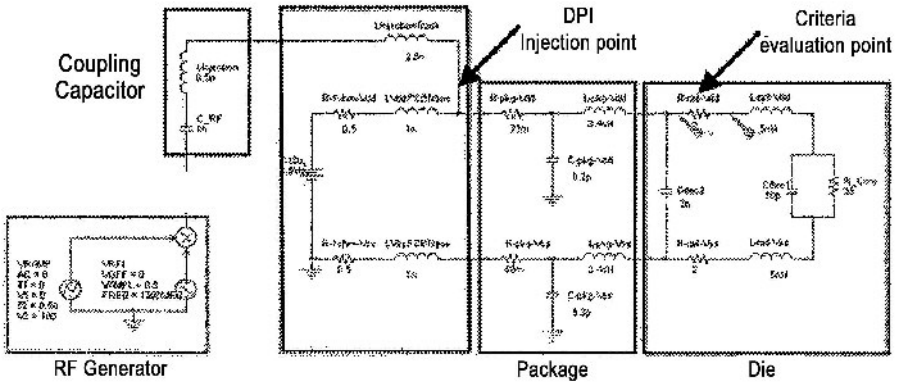


Figure 5-87. Full immunity simulation model.

To simulate the growth of the RF disturbance amplitude, two solutions can be chosen indifferently.

The first consists in making parametric simulations by varying, for a given frequency, the RF signal amplitude. This can be made under SPICE by using the .PARAM option. The results obtained are then a function of the defined amplitude step. The simulation time and the desired precision of these results increase in inverse proportion to the size of this step.

The second solution consists in generating a disruptive signal whose amplitude increases during the simulation. For that purpose, it is sufficient to introduce a modulating factor. This can be done easily by multiplying the unit aggression signal by a slope whose characteristics define the amplitude

variation (Fig. 5-86). An example of a full immunity model is illustrated in Fig. 5-87.

7.4 Definition of a failure criteria

In this paragraph, a non-exhaustive list of failure criteria based on the generation of physical faults at integrated circuit level is presented. Among these, the stress of the power supply, the decrease of the power supply, decline of differential voltage and the over consumption of current will be considered. These criteria have the advantage of being relatively easy to implement in a simulation environment. The purpose is to be able to predict the susceptibility of an integrated circuit during the design phase.

7.4.1 Stress of the power supply

In the presence of a radio frequency disturbance (Fig. 5-88), the voltage of power supply can fluctuate. This fluctuation is called ground bounce when it is observed on the V_{SS} Die, and supply bounce when it results from the V_{DD} Die. Below a certain limit, these effects are tolerated by the active blocks of the circuit and no error is observed. Beyond this limit, the potential difference between the external and internal V_{SS} references is such that a part of the information from the outside can be badly interpreted by the active parts of the circuit and generate logical faults. Only the V_{SS} reference is considered, but in a similar way, this phenomenon can occur on the V_{DD} reference of the circuit.

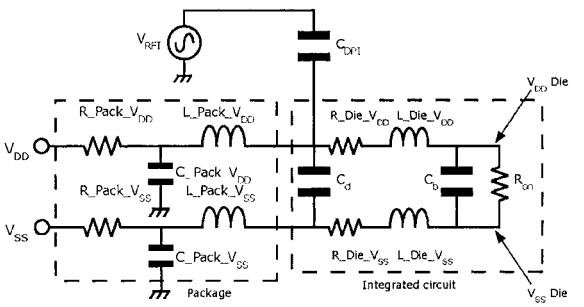


Figure 5-88. Stress owing to bounces of the internal power supply.

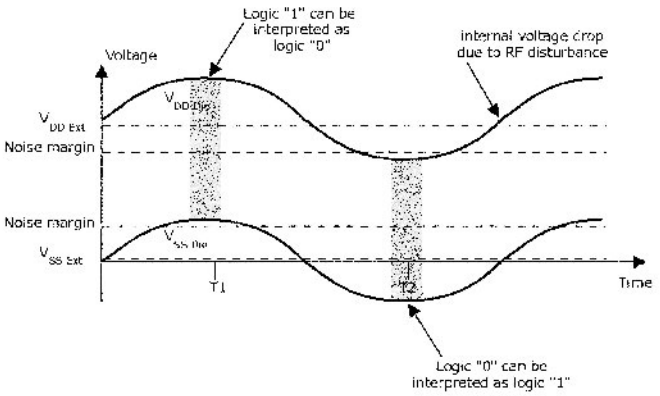


Figure 5-89. Logical fault generation due to an excessive stress of the internal power supply of the integrated circuit.

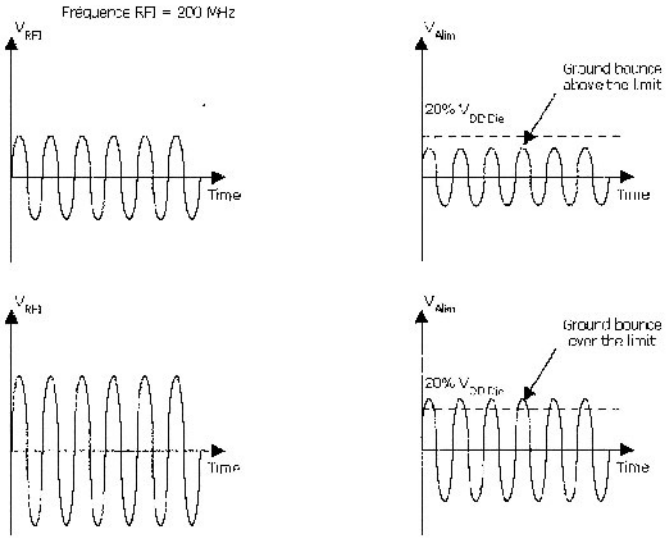


Figure 5-90. The amplitude of the RF disturbance grows until it exceeds the fixed immunity threshold (20 % of the nominal power supply).

That means, when a logical "1" is present on the IC input, the core of the chip will consider this logical "1" as a logical "0". This phenomenon is illustrated in Fig. 5-89 at time T1.

The logical fault appears and is then processed, thus propagating an error in the whole circuit. In the same way, a logical "0" can be considered as a logical "1", as presented at time T2 of Fig. 5-89.

In analog simulations, the idea is to perform iterative simulations by varying the frequency characteristics of the aggression voltage (V_{RFI}). For each frequency, the amplitude of the disturbance is increased until the fluctuation of the internal V_{SS} reference is higher or equal to 20 % of the nominal power supply voltage. At this moment, the criterion of susceptibility is supposed to be reached (Fig. 5-90).

7.4.2 Decrease of the power supply voltage

An important failure criterion lies in the decrease of the internal power supply voltage (Fig. 5-91). This notion corresponds to the difference which exists between the reference voltages V_{DD} Die and V_{SS} Die. Below a certain margin, which can be defined at 30 % of V_{DD}, the switching of the logical circuits is significantly slowed. This phenomenon is at the origin of delays at signal distribution level, and can lead to the loss of features of logical or analog circuits.

Fig. 5-92 presents the delays of switching according to the fall of the power supply voltage. This simulation was made for an CMOS inverter designed in 0.25 µm technology with typical load conditions (Caignet, 1999). It shows that a decrease of 30 % of the power supply voltage (from 2.5 V to 1.75 V) corresponds to an increase of the switching delay of about 60 %. A decrease of 50 % of the voltage V_{DD} generates a switching delay 150 % higher. Such increases cause some functional blocks to be no longer operational or correctly synchronized and thus generate faults at the component level.

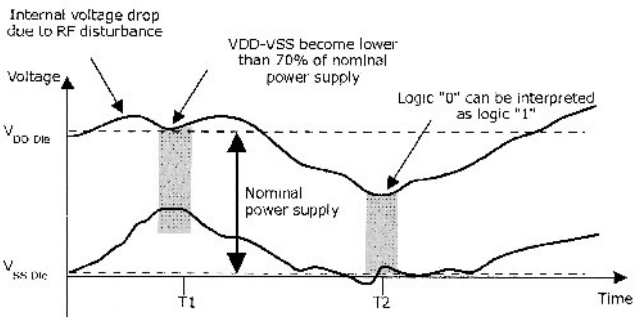


Figure 5-91. Logical origin of faults due to a reduction of power supply.

7.4.3 Over-consumption of current

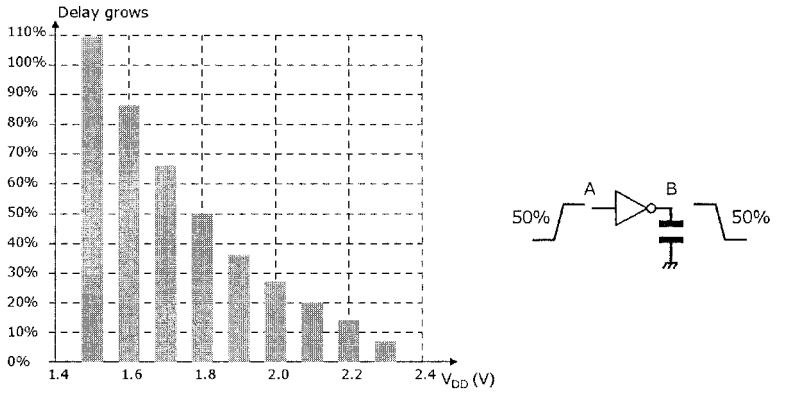


Figure 5-92. The distribution delay is significantly increased with the decrease of the power supply voltage.

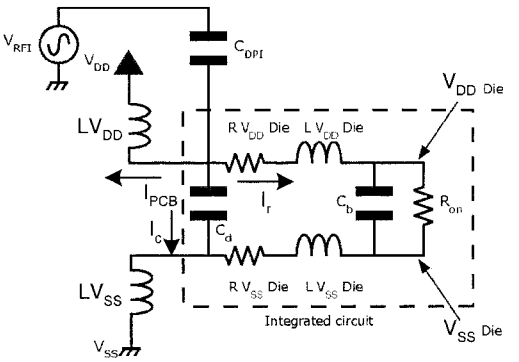


Figure 5-93. The over-consumption of current inside the chip.

A disturbance injection on the power supply network of a printed circuit board can generate parasitic effects on the on-chip power supply network, such as current flow with very strong intensity. Fig. 5-93 describes three kinds of these currents:

- A current, I_C, which flows through the internal decoupling capacitance of the integrated circuit (C_d).
- A current, I_r, flowing on the internal power supply network of the chip.
- A last current, I_{pcb}, which flows on the power supply network of the printed circuit board.

Due to the physical elements which they go through, these currents possess certain limitations. The intensity that it is possible to pass nominally through a gold bonding wire with a radius of 15 µm can be estimated by means of Eq. (5-12). A maximal current of about 2 A is founded. On the other hand, it is important to note that the dependence on temperature is not taken into account. Consequently, in nominal functioning, this maximum current is certainly lower than the proposed value.

$$I_{max} = I_{gold}\pi.r^2 \qquad (5\text{-}12)$$

Where:

- I_{gold}: the maximal current density A / µ m^2.
- r: conductor radius µm (15 µm for a typical bonding).
- I_{max}: the maximal current which can flow before destruction of the conductor.

Consequently, these limits can be exploited to define a new failure criterion within the framework of analog simulations. This failure criterion can also be used during an immunity measurement. In that case, a VDE probe must be added onto the power supply network.

An integrated circuit which consumes a nominal current (I_{nom}) of about 100 mA, is supposed to be able to support 500 mA (5 x I_{nom}) current peaks. Furthermore, currents whose intensity is higher than one ampere have a very strong probability of destroying the most fragile elements of the chip. So, from these various levels, functioning areas are defined as illustrated on Fig. 5-94: a nominal area from 0 to 5 x I_{nom}, an area where functional errors appear (5 x I_{nom} - 10 x I_{nom}) and a destruction area of the integrated circuit beyond 10 x I_{nom}.

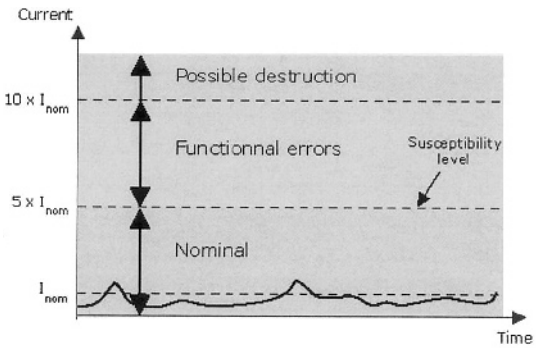


Figure 5-94. Definition of current over consumption thresholds.

7.5 Comparison simulation / measurement results

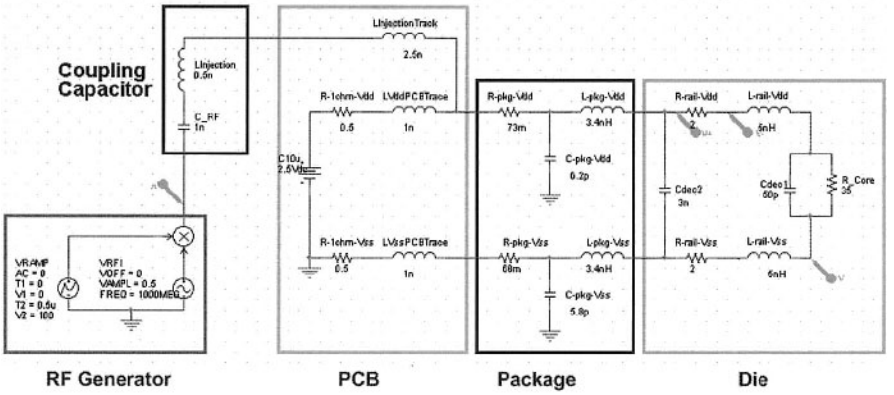


Figure 5-95. Electrical schema of the simulation environment.

To set up the comparison of the simulation with the measurement, it is necessary to model not only the component but also its environment. This associated environment is going to depend strongly on the mode and on the point of aggression defined during the measurement. In this study, a radio frequency disturbance was injected into the power supply network of the component under test.

Fig. 5-95 presents a schematic diagram of the whole electrical layout that was used to simulate the immunity behavior of the 16-bit micro-controller considered. This description can be divided into five representative independent blocks of the various physical elements implemented during the measurement.

The left part corresponds to the generation of the radio frequency disturbance. It is composed of a sinusoidal generator with a peak to peak amplitude of 1 V. A slope generator is associated to it via a multiplier to vary the amplitude of the effectively generated signal.

The last element of the aggression path taken into account, at the pcb level, corresponds to the inductance of the track connecting the injection capacitor with the device under test. This track is relatively short, less than 5 mm, so its inductance is consequently estimated at approximately 2.5 nH.

Finally, the last elements not yet described are a part of the power supply network of the printed circuit board. The present voltage regulator is modeled by a DC voltage source which is associated to a 1W resistance needed for the parasitic emission measurement.

The elements of the device under test are divided into two groups: the package model and the chip model.

Any IC immunity simulations require the definition of a failure criterion. The stress of the power supply is chosen here. So, as soon as the fluctuation, in absolute value, of the power supply voltage is higher than 20 % of V_{DD}, the device under test is considered to have failed.

All the simulations were performed using an analogical PSPICE simulator (Orcad, 1998). The injected disturbance frequency is considered as a parameter of analysis. The number of points by decade is fixed to 10. This choice is a compromise between the precision of the results and the time required for post-processing. Indeed, the definition of each point of the immunity level versus frequency curve is not immediate. Therefore, at each frequency, it is necessary to determine the moment when the internal power supply voltage reached the defined failure criterion.

Then it is necessary to calculate the power injected by the RF aggression source to obtain points comparable with those of the measurements. Consequently, for a relatively short simulation period (half an hour for all the frequencies), the post-processing time is practically multiplied by a factor of ten.

Fig. 5-96 presents a comparison between simulation results and measurements performed on a 16-bit microcontroller.

For the frequencies lower than 100 MHz, except for the 20 MHz simulation point, the results are in fairly good agreement with the measurements.

Indeed, for the frequencies between 1 MHz and 10 MHz the simulation is considerably above the measurement results, but these last were limited to a power level equal to 25 dBm.

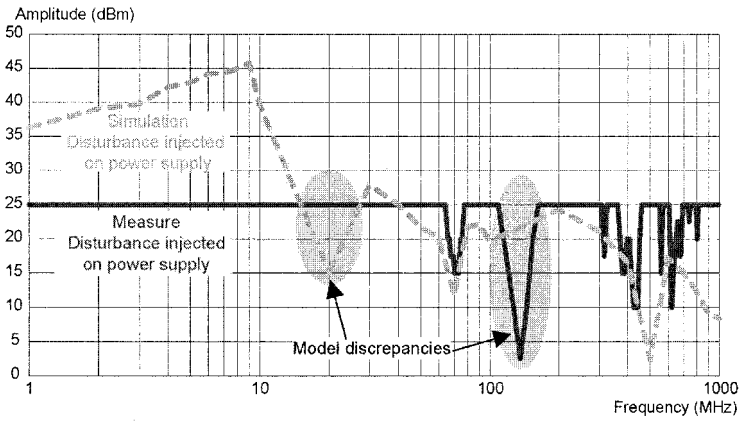


Figure 5-96. Comparison between measurement and simulation results.

For the frequencies higher than 100 MHz, a satisfactory shape is obtained, except for the 130 MHz point. At this level several hypotheses can be made:

- The model defined is insufficient and one or several elements were not taken into account.
- This particular susceptibility does not depend on the microcontroller but on the external voltage regulator. This last is modeled on an ideal DC voltage source, what is doubtless not realistic.

7.6 Immunity LECCS model

The LECCS-core model is also applicable for immunity evaluations of an LSI (Takahashi, 2002). The simulated results clearly explained the immunity test results with the direct RF power injection (DPI) method (IEC 62132-4) (IEC 62132-4, 2001). In the simulation, the internal impedance of the device (an 8-bit microcontroller, 100 pin QFP) Z_L and the impedances of the power/ground connections Z_V and Z_G were separately evaluated and modeled (Fig. 5-97). RF noise was injected from the power interconnection on the test board following the set-up of the DPI method as shown in Fig. 5-98, and the forward RF power at the malfunction of the LSI was recorded. In the simulation the voltage across the chip (V_L) was calculated with the LECCS model. Fig. 5-99 shows the comparison of the measured and calculated results, which demonstrate a good correlation between the induced voltage across the chip and the immunity level.

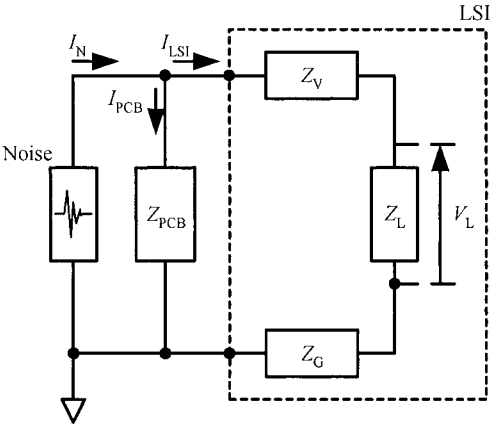


Figure 5-97. Immunity evaluation model with LECCS (Takahashi, 2002).

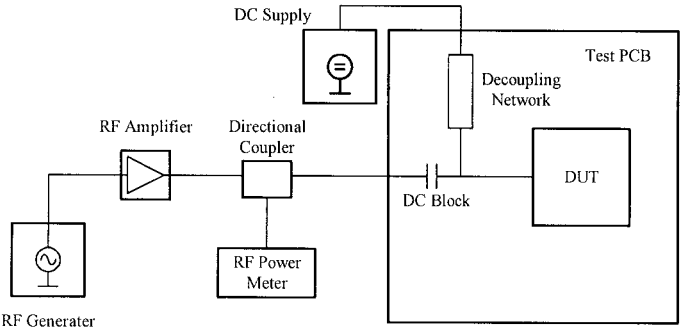


Figure 5-98. Arrangement for DPI test set-up.

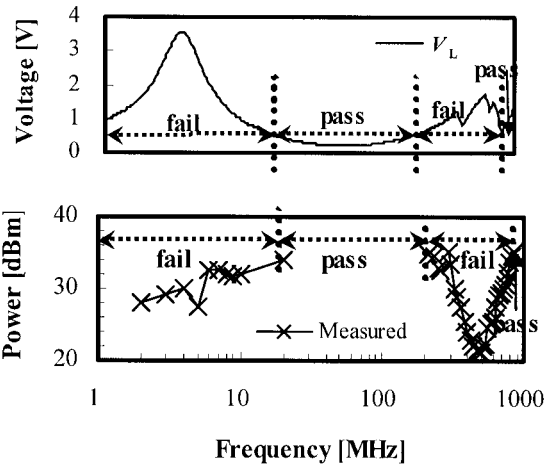


Figure 5-99. Simulation and experimental results of immunity test (Takahashi, 2002).

7.7 Internal immunity analysis

In the case of internal immunity, disturbances are created inside the chip itself and ICEM model enables to check its auto-compatibility.

This example deals with an audio amplifier immunity (see Fig. 5-33) analysis using ICEM model. Fig. 5-100 shows the PDN (Power Distribution Network) of the amplifier part and its immunity model.

The ICEM model of the digital part is simplified to the VnDig noise source. The IBC component is a simple resistor in a low frequency range and connects the VnDig to the internal terminal IT[0].

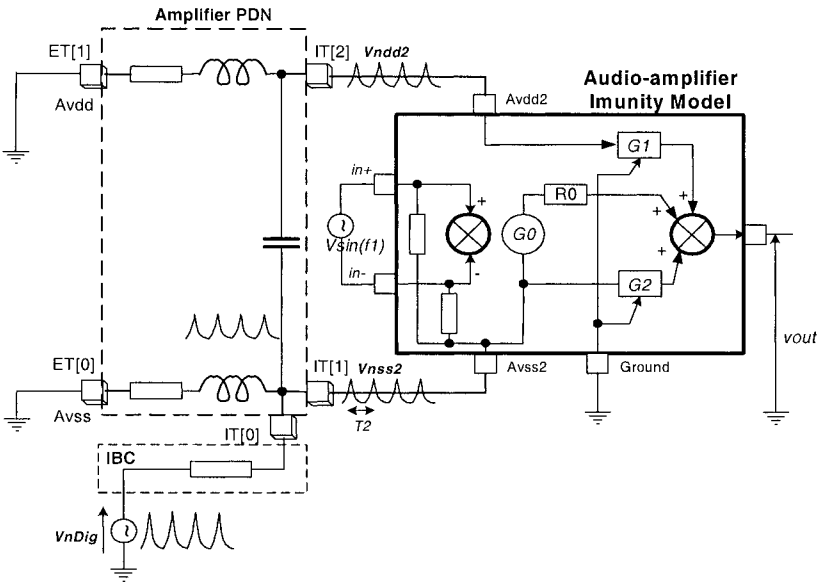


Figure 5-100. Immunity analysis example using the PDN and the IBC of ICEM components and the amplifier immunity model.

The immunity model must take into account the power and ground rejection ratio (PSRR). The G1 and G2 transfer functions characterize the attenuation level of the noise transmitted by the digital activity to the audio output. Under these conditions, the audio output level is expressed with the following expression:

$$vout = vsin \cdot G0 + Avdd2 \cdot G1 + Avss2 \cdot G2$$

The output level is degraded by the presence of noise on the Vdd2 and the Vss2 internal rails. Several tens of millivolts are generated by the digital activity. Only a few millivolts can be heard by the human ear and a good PSRR is mandatory to guarantee a good audio reproduction.

7.7.1 Internal immunity Spice Model

Fig. 5-101 shows the spice immunity model using the standard source components. V4 generates an audio frequency for test purposes.

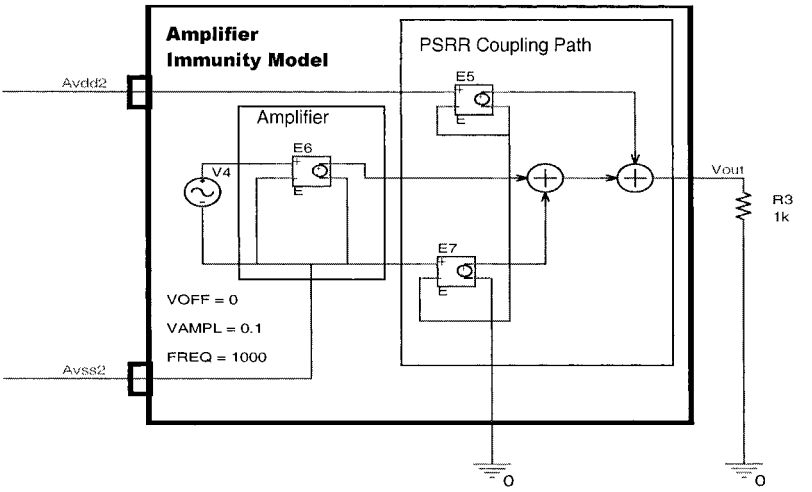


Figure 5-101. Immunity model in Spice language.

7.7.2 Immunity criteria

Fig. 5-102 plots an example of an incompatibility between the digital activity and the audio production. Above F1, the level of the digital activity is out of specification. This digital noise is added to the F2 frequency and is heard by the user.

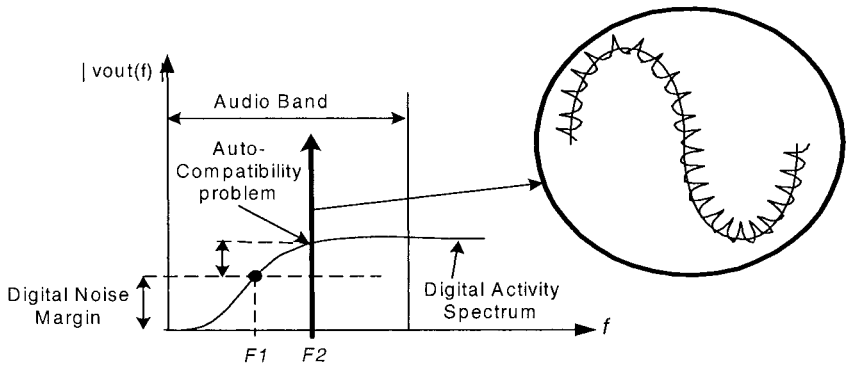


Figure 5-102. Example of immunity criteria for an audio amplifier.

7.7.3 Immunity analysis result

Fig. 5-103 plots the noise propagated by the digital activity to the amplifier output. The immunity criteria is 2.5 mV and at 9 μs the noise level is not within the specification. A power-supply rejection ration default has been detected on the audio amplifier. It has been increased to 20 dB. Thanks to the ICEM model the immunity criteria has been checked and accepted (Fig. 5-104).

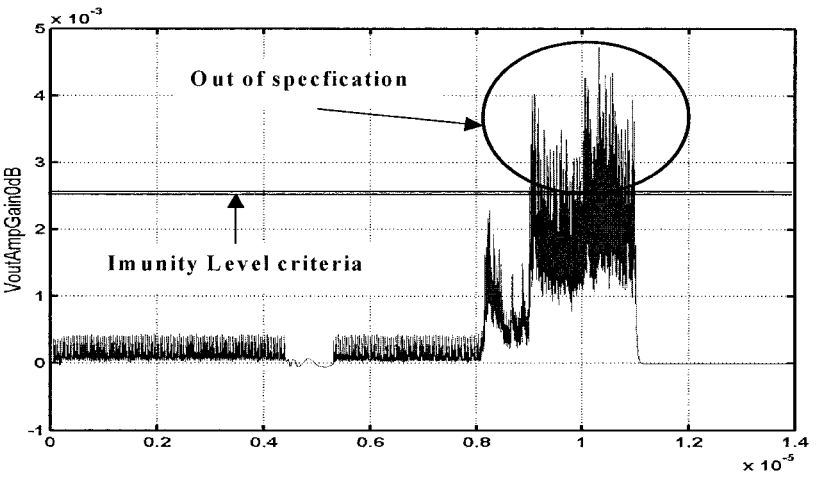


Figure 5-103. Immunity level at the amplifier output.

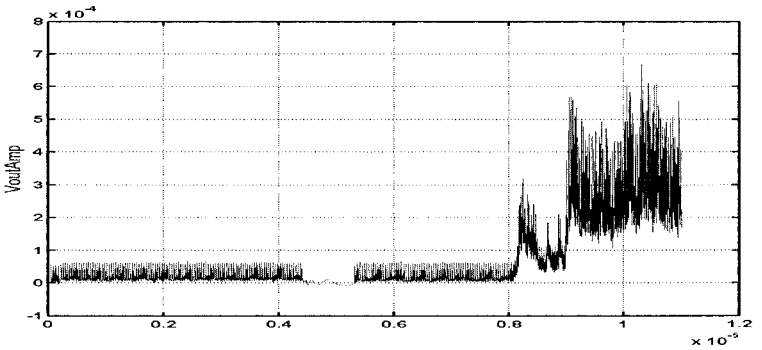


Figure 5-104. Immunity level after PSRR correction.

8. CROSSTALK EFFECTS

The main crosstalk effects, which can be fully described in recent references (Caignet, 2001; Werner, 2001; Moll, 1998), are spurious signals appearing in victim lines when aggressor lines switch, and crosstalk-induced delays when victim lines and aggressor lines switch simultaneously; this causes a change in the propagation delay of the victim line. This effect is very important in modern ULSI microprocessors presenting very long interconnection lines. Of course, the importance of the effects described above depends on the technology used in microelectronic design as well as on interconnection topology.

Another important effect of coupling capacitances is an increase in dynamic power consumption (Moll, 2003; Sotiradis, 2000; Machiarulo, 2002) because of two contributions: the first one consists of the spurious signal produced by the coupling capacitance, which causes an extra amount of dissipation in the driver of the coupled line; the second one is due to the propagation of this spurious signal through logic gates in the subsequent nodes of the coupled signal.

In this section, only the first contribution will be dealt with. First of all, it will be analyzed from a mathematical point of view (Moll, 2003), considering an electrical model and its solution. Once the model is developed, a set of simulation results will be presented in order to validate its predictions and also to analyze the influence of the different parameters involved in the problem. Then, in the last subsection, an experimental setup aiming at validating the results obtained from simulations will be introduced.

8.1 Mathematical model

The circuit depicted in Fig. 5-105 presents two interconnection lines which are driven respectively by two CMOS inverters. Each line is described as a capacitance to ground, modeling ground parasitic capacitances (C_1 and C_2), along with a coupling capacitance in between, modeling capacitive crosstalk (C_{12}). Additionally, I/O coupling capacitors C_{c1} and C_{c2} are included in the driver model.

It has been demonstrated (Moll, 2003) that the total dissipated energy is given by Eq. (5-13):

$$E_T = E_{SC} + E_{ST} + E_{IO} + E_{LINES} \tag{5-13}$$

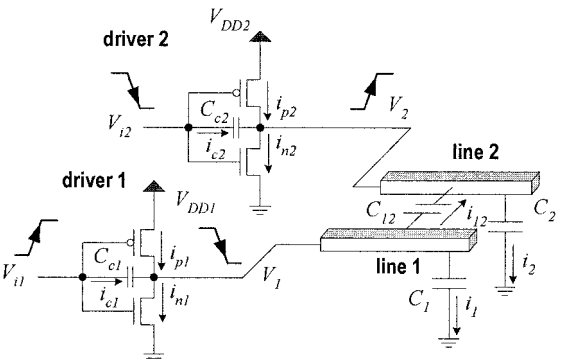


Figure 5-105. Circuit used to model the structure of two coupled lines with inverter drivers.

In this expression, the following contributions can be identified:

- E_{ST} and E_{SC} corresponding to the cut-off transistor in the quiet driver (subthreshold current contribution) and the cut-off transistor of the active driver in its final state (short-circuit current contribution).

  A contribution in the active driver due to the input-output parasitic capacitances of the devices (E_{IO}). This contribution can be calculated from $E_{IO} = \frac{3}{2} C_{C1} V_{DD}^2 + C_{C1} \int V_1 \frac{dV_{i1}}{dt} dt$ for positive transitions and $E_{IO} = \frac{1}{2} C_{C1} V_{DD}^2 + C_{C1} \int V_1 \frac{dV_{i1}}{dt} dt$ for negative ones.

- A contribution due to interconnections, given by $E_{LINES} = 1/2(C_1+C_{12})V_{DD}^2$.

In the more complex case of two non-simultaneous input transitions, the total energy is given by Eq. (5-14):

$$E_T = E_{SC} + E_{ST} + E_{IO} + \tfrac{1}{2}(C_1 + C_{12})V_{DD}^2 + \tfrac{1}{2}(C_2 + C_{12})V_{DD}^2 \pm \Delta \qquad (5\text{-}14)$$

being $\Delta \equiv C_{12}V_{DD}^2 + (C_2 + C_{12} + C_{C2})V_{DD}D_2 - C_{12}V_{DD}D_1$.

D_1 (D_2) are the distances of the voltage V_1 (V_2) from their initial quiescent values when the second transition begins. Regarding the ± symbol, the positive case corresponds to transitions in opposite directions, while the negative case is for transitions in the same direction.

This expression predicts a maximum in the energy for simultaneous transitions in opposite directions and a minimum for simultaneous transitions in the same direction. A more detailed analysis for both single and double transitions can be found in (Moll, 2003).

8.2 Energy consumption increase due to crosstalk: simulation analysis

Energy consumption can be estimated by using an electrical simulator such as HSPICE. Parasitic capacitance values in the example structure were extracted by using data from a 0.18 μm CMOS technology (1.8V supply voltage, 1 poly and 6 metal layers).

In order to estimate the values of line capacitances C_1, C_2, and C_{12}, an electromagnetic field solver integrated in HSPICE was used. It must be noted that C_1 and C_2 include an estimated fanout capacitance C_g = 5 fF (equivalent to approximately 5 minimum size inverters) in addition to the substrate coupling capacitance. Post-processing features are used to calculate the instantaneous power and the energy as the power integral over time.

Two equal lines with minimum width and minimum separation on the first metallization level have been used as the coupled structure in the simulation analysis. Equal and approximately balanced drivers (L= 0.18 μm, W_n = 1 μm, W_p = 2.5W_n) were considered, and input signal rise/fall times have been set to 200 ps.

8.2.1 Single transition

Three energy values were obtained:

- The total energy including crosstalk effects (C_{12} value given by the field solver).
- The total energy excluding crosstalk effects (C_{12} = 0).
- The line contribution to the total energy, labeled E_{LINES}, which is calculated analytically.

The device contribution is the total energy minus the line contribution.

Fig. 5-106 shows the different energy contributions vs. line length. Device contribution represents 50% of the total energy dissipation for a very short line (1 μm), and decreases rapidly when line length increases. For example, for a 250 μm long line, device contribution is only around 10 % of the total energy consumption. It can be seen that, for 100 μm long lines, crosstalk contribution is around 40 % of the total energy dissipation. Therefore, this contribution can be neglected only for short lines.

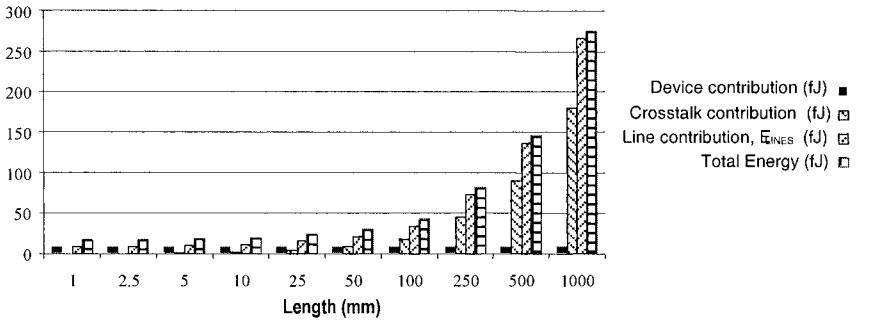


Figure 5-106. Device, crosstalk and line contributions to total energy consumption.

This result shows that, as far as energy dissipation in VLSI circuits is concerned, line effects, including crosstalk, can not be neglected, while device effects could be ignored for lines longer than a given value. This result can be used in estimation tools for energy dissipation to obtain accurate results and improve analysis time.

8.2.2 Non simultaneous transitions in both nodes

This section deals with the more complex case of non simultaneous transitions in both lines, and how the energy dissipation depends on the relative delay, and on line length.

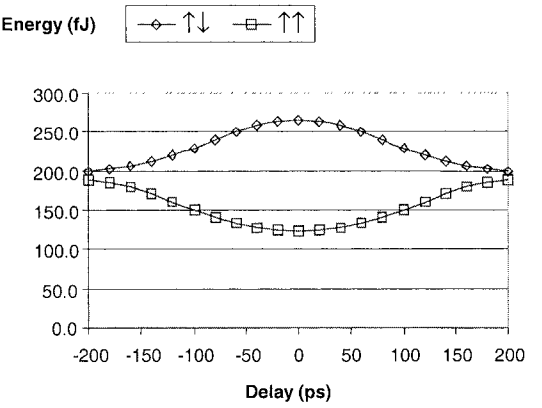


Figure 5-107. Energy dissipated in the driver transistors, vs. delay between both input transitions.

Non simultaneous transitions in both nodes can be classified in two cases: transitions in the same direction (↑↑ notation is used) and transitions in opposite direction (↑↓).

8.2.2.1 Energy consumption dependency on relative delay

The energy dissipation depends on the relative delay between input transitions. One line switches at a fixed time, while the other switches with a variable relative delay, ranging from –200 ps to 200 ps.

Fig. 5-107 shows the simulation results. As predicted by the analytical expressions, the total energy presents a maximum (minimum) for simultaneous opposite direction (same direction) transitions and tends to a constant minimum (maximum) value for maximum delay. Actually, when the transitions are separated by more than the output rise time, which is about 200 ps for these drivers and lines, the energy is the same as the one given by individual separated transitions.

8.2.2.2 Energy consumption dependency on line length

Energy consumption depends on line length, and therefore, on the values of the line capacitors. Fig. 5-108 presents the energy dissipated in the drivers in a log-log scale. For short lines, this energy is almost a constant, indicating that the main contribution to the transistor dissipation is due to shortcircuit and leakage currents, which are basically independent from line capacitance. However, for line lengths around 100 μm, it increases with a 20 dB/dec slope, corresponding to an energy proportional to length, and therefore to the line capacitances.

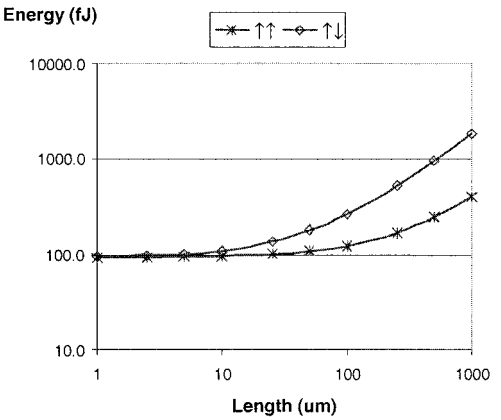


Figure 5-108. Energy dissipated in the driver transistors, vs. line length.

Consequently, within this range of line lengths, the energy dissipated is basically devoted to charging and discharging the line capacitances, including the crosstalk capacitance. That range of line lengths is quite common in medium to large size circuits; therefore, crosstalk contribution has to be seriously considered in power estimation tools if accurate predictions are necessary.

8.3 Experimental measurement procedure

In order to characterize this increase in energy dissipation experimentally, a VLSI CMOS circuit is considered. It is composed of two coupled lines, each one driven by an inverter and terminated with a load inverter. Fig. 5-109 shows a schematic of this circuit. Considering separate biasing pads for the drivers is mandatory for accurate measurements of energy dissipation.

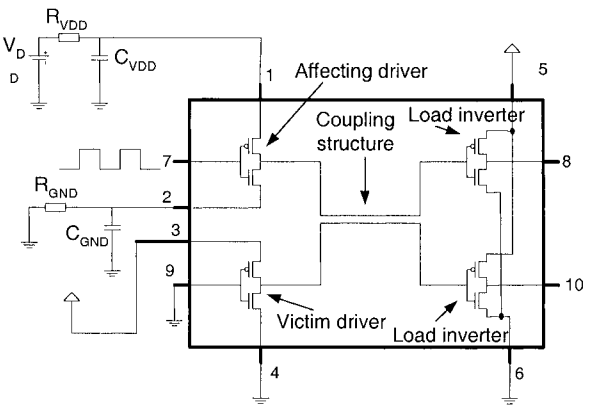


Figure 5-109. Schematic of the circuit.

Different coupling structures were implemented in a 0.35 μm test circuit. The same coupling structure, i.e. two level-1 minimum-width metal lines separated by the minimum distance allowed by the technology, were implemented for different line lengths. To compare vertical vs. horizontal couplings, a level-2 over level-1 line was also included. Fig. 5-110 represents the layout of one case in the designed circuit. Without the use of on-chip sampling sensors (Delmas, 1999), it is practically impossible to measure noise waveforms with good accuracy. The approach considered in this chapter thus deals with direct energy measurements.

The idea is to extend the method which was applied by Rius et al (Rius, 1999) to measure I_{DDQ} contributions, and by Figueras et al. (Figueras, 1999) in terms of energy defect detection in VLSI CMOS circuits, to determine the crosstalk energy consumption contribution.

As can be seen in Fig. 5-109 the biasing terminals of the drivers are connected directly to dedicated supply pads. These nodes are different from the global V_{DD} and GND pins, which bias the substrate (of all NMOS transistors), the n-well (of all PMOS transistors) and the load inverters. This enables the evaluation of the energy dissipated in the drivers by using an external capacitor and measuring its voltage drop. The method is illustrated in Fig. 5-109 with an example in which the measurement of the energy dissipation in the affecting driver is considered. The V_{DD} pin of this driver (pin 1) is connected to a V_{DD} source through a resistor R_{VDD} and including also a capacitor C_{VDD}. The GND pin of this driver (pin 2) is connected to GND including the same RC structure as on the V_{DD} pin. Because this example is dedicated to the measurement of the energy in this driver, the equivalent nodes in the victim driver (pin 3 and 4) are respectively connected to the global V_{DD} and GND.

R_{GND} is very small (short-circuit) and R_{VDD} presents a huge resistance value. Then, the voltage in node V_2 is connected to ground by a low resistance path implying very small variations on the voltage of this node while the inverter is switching. Conversely, a high resistive path can be observed between V_1 and V_{DD}. The following measuring procedure is used:

- The capacitor C_{VDD} is precharged up to V_{DD}.
- The buffers of both lines (pin 7 and 9) are excited with switching signals, depending whether a single transition case or a multiple transition case is considered. The energy dissipated in the buffers is derived from the energy stored in the biasing capacitors. The period of these excitation signals has to be much smaller than the $R_{VDD}C_{VDD}$ time constant, so that the capacitor is unable to recharge its value up to V_{DD}.
- Finally, the voltage drop in the capacitor, ΔV_1, is measured and related to the total energy consumed ($E=1/2\ C_{VDD}\Delta V_1^2$).

It must be taken into account that the total voltage drop has to be kept small in order to maintain the operating point of digital circuits (an inverter gate in this case). This condition implies some limitations in the value of the C_{VDD} capacitance and also in the number of successive transitions used to excite the input buffer in a complete measurement process, without a new pre-charge of the biasing capacitor. The selection of the value of the C_{VDD} capacitor depends on the energy dissipated when the circuit is in switching activity. High values of dissipated energy require high values of biasing capacitors in order to maintain the level of V_1.

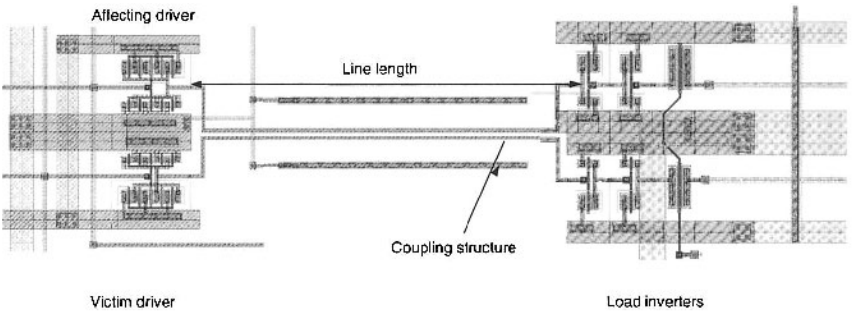


Figure 5-110. Layout of the test chip.

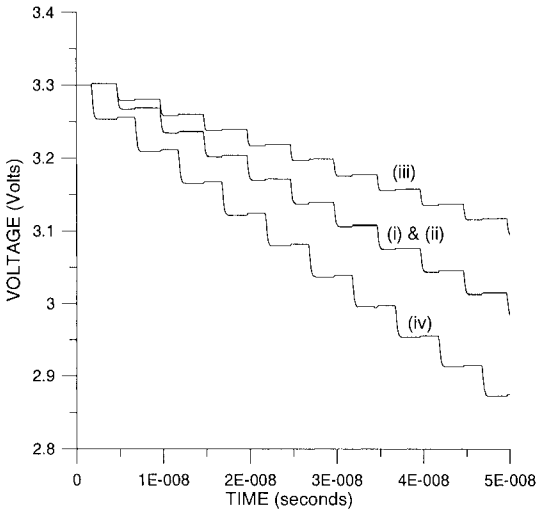


Figure 5-111. Change of the voltage across CVDD.

Only a small decrease in V_1 is allowed, because an important change in this voltage implies an important reduction in the effective value of the power supply of this driver, with subsequent effects on its correct behavior.
In addition to the measurement procedure previously presented, a set of simulations from layout extraction are performed, showing its effectiveness. In the first experiment (Fig. 5-111), a pulsed signal is applied to the affecting buffer. Four different cases are plotted depending on the input of the victim buffer: (i) victim buffer connected to GND, (ii) victim buffer connected to V_{DD}, (iii) connected to the same pulsed signal and, (iv) connected to a complemented pulsed signal.

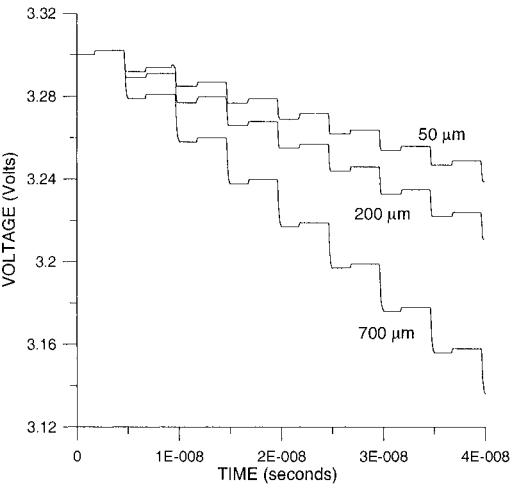


Figure 5-112. Change of the voltage across CVDD: influence of line length.

The voltage value at the biasing capacitor is plotted on the Y-axis. It is noted that the same direction for the transitions in both lines implies a reduction in the dissipated energy, while maximum energy dissipation is obtained with different directions in both lines.

The second experiment (Fig. 5-112) deals with the analysis of line length effect in energy dissipation. The voltage in the biasing capacitor is plotted during 8 periods of the switching signal, and considering different lengths of the coupled lines (50, 200 and 700 µm). As expected, it can be seen that the voltage drop increases (energy increases) with line length.

9. RADIATED EMISSION MODELING

This section deals with modeling measurement equipment used for radiated emission. The TEM cell and the near-field scanner are the most commonly used in this area.

9.1 Modeling the TEM cell measurement method

The TEM cell model proposed in this section is applicable to integrated circuit radiated emission prediction up to 1 GHz. The cross-section of the TEM cell is given in Fig. 5-113. The IC is coupled to the inner metallic plate of the TEM cell (septum) by proximity effects.

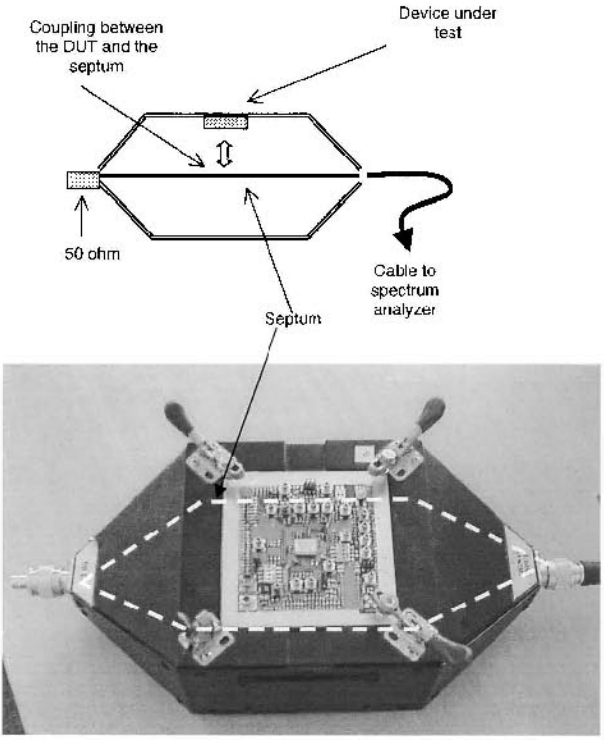


Figure 5-113. Cross-section of the TEM cell showing the coupling between the DUT and the septum.

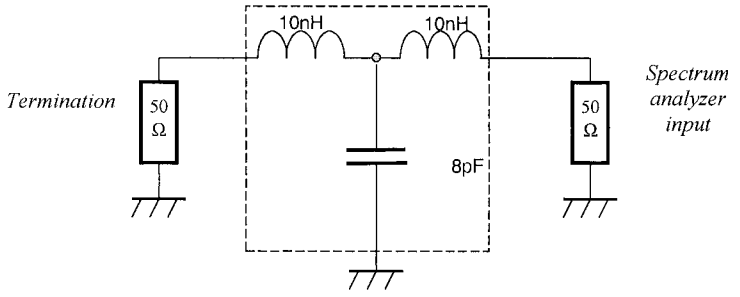


Figure 5-114. Simple TEM cell model.

With no device in the cell, the simplest TEM model consists of a capacitor (8 pF) and an inductor (20 nH). The values have been computed using 2D and 3D field solvers, and confirmed by measurements.

In order to keep the model symmetrical, the inductance is split into two discrete components L1 and L2, as illustrated in Fig. 5-114. Both terminations are 50 Ω.

When a device is placed in the TEM cell, two types of coupling may be observed: a magnetic coupling between IC inductances and the TEM inductances, and electric coupling by proximity effect. The inductance coupling is usually described as a coupling coefficient from 0 to 1. From 2D/3D simulations, it was found that the coupling percentage is near 1% for QPF package leads, and 0.1% for BGA leads. The inductance coupling is dependent on the orientation: when the package lead is perpendicular to the septum, the inductive coupling is decreased by 20 dB. Consequently, the coupling coefficient is reduced by a factor of 10.

The capacitance coupling is represented by *Cdie_septum*, with a value ranging from 20 fF to 200 fF, depending on the die size. To summarize, the interaction between the component and the cell is modeled by means of lumped capacitance and mutual inductance. Measurement and simulation results have shown close agreement in TEM emission levels from 1 MHz to 1 GHz.

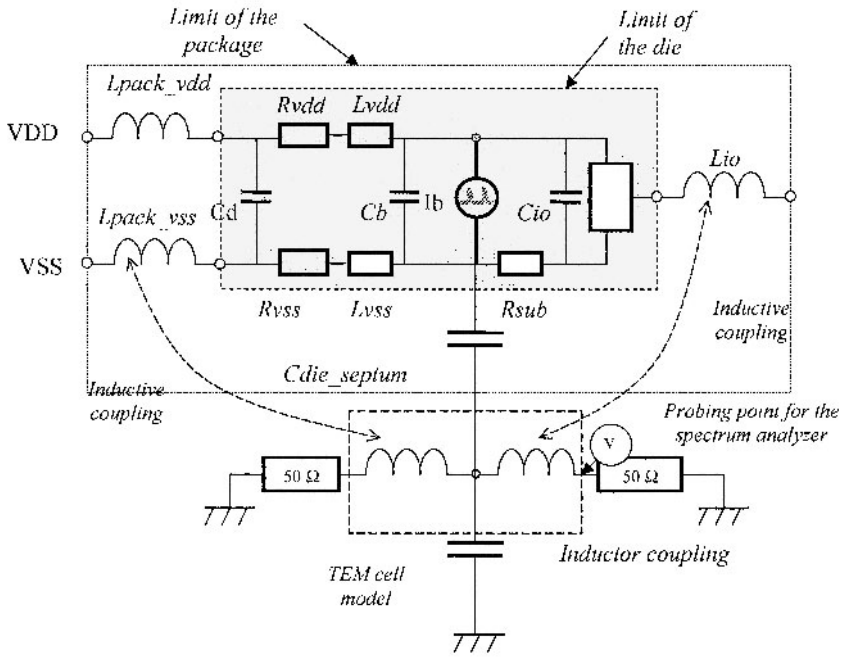


Figure 5-115. Coupling between an IC and the TEM cell.

For greater accuracy, more complex models of the coupling mechanism between the TEM cell and the component can be developed, as with the distributed coupling effect between the septum and the different parts of the component (die, bondings, leads) (Fig. 5-115). S-parameter-based modeling by means of 3D electromagnetic simulations has also been investigated to characterize more accurately the interactions between the cell and the IC current paths at high frequency.

9.2 Near-field scanning

In this section, a use of the near-field scanning method to extract the IC's radiated emission models is shown. It leads to the prediction of the coupling phenomena on the electronic board and to the evaluation of the radiated emission. An estimation of the scalar and vector potentials is found with the scan. With these results it is then possible to calculate the near and far emissions.

9.2.1 Measurement method

The scanner is made of a plastic holder on which the PCB is fixed (Fig. 5-116). The electromagnetic probes move above the device under test in a plane. As the emitted field that will be coupled on tracks at a few millimeters from the IC is the object of interest, it is sufficient to scan the field with a commercial probe, with a diameter of 1 cm.

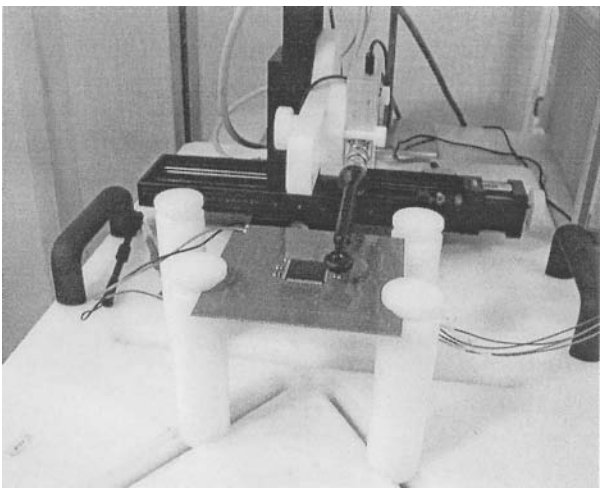


Figure 5-116. Near-field scanning test bench (courtesy of Valeo France).

The detailed activity of the component core will not be measured, but a synthetic view of the radiated emission toward the environment. For the same reason one measurement every millimeter is sufficient to give a complete characterization. The field measured is the vertical magnetic field H_Z, and it is then possible to build an image of the field with only one cartography, instead of two if working with the H_X and H_Y fields.

To validate the measurement and simulation principles, simple passive circuits using a network analyzer were studied. A model of the near and far-field emissions for such simple circuits is first proposed and compared with measurements. Then, a real case study on a microprocessor is shown.

9.2.2 Passive Element Case

The case study used is a simple square loop as shown in Fig. 5-117. The cartography is first performed using a network analyzer, which powers the board. The model is based on the scalar and vector potentials expressed in the Lorentz gauge. Using the scalar potential V, and the vector potential, expressions of the electric and magnetic fields can be obtained. It is clear that if the distribution of currents and electric charges are known in a circuit, then it becomes easier to estimate the emitted fields at every point in the space. As far as field simulation is concerned, wires are considered as short enough with respect to wavelength, so that the associated current is assumed to be constant and the charges linearly variable.

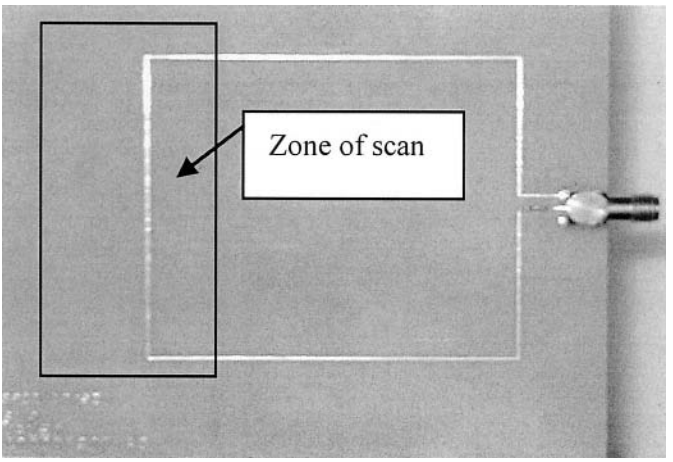


Figure 5-117. PCB test board.

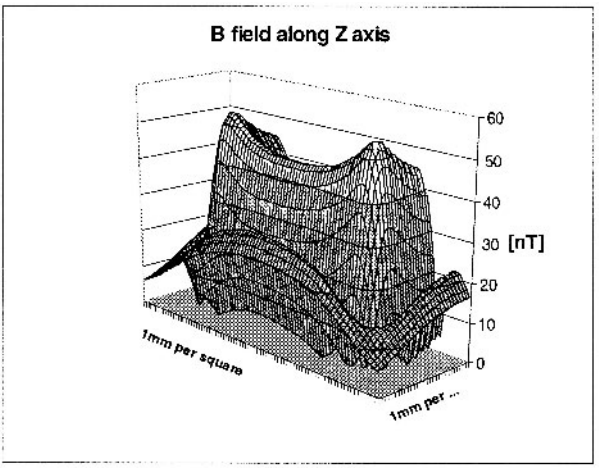


Figure 5-118. Measured magnetic field (Bz) at 100 MHz (probe at 3.5 mm above the PCB).

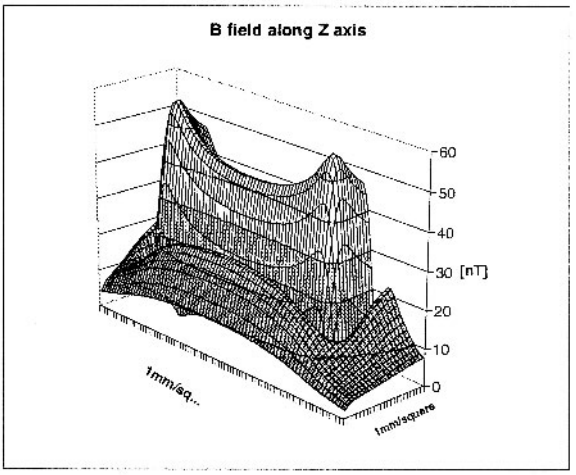


Figure 5-119. Simulated magnetic field (Bz) at 100 MHz, (probe at 3.5 mm above the PCB).

As the circuit described here is very simple, the field is easily computed. It is the sum of the contributions of each branch of the square root. The effect of the probe has still to be taken into account. For this the simulation result given here is the average of the field passing through a surface of the same size as the probe: the average vertical magnetic field through a horizontal 1 cm diameter disc.

The measurements are performed in planes at different heights above the PCBs: 3.5 mm, 8.5 mm and 13 mm. The case for 3.5 mm is illustrated in Fig. 5-118 (measurement) and Fig. 5-119 (simulation). The current value chosen is the one giving the best near-field estimation for all the distances.

9.2.3 Microprocessor Case

In the case of a microprocessor the number of unknowns increases dramatically. Both the geometry of the lines driving the current and the intensity of the current have to be identified. To achieve this at each position of the magnetic probe a measurement is performed in the full frequency bandwidth from 8 MHz to 400 MHz and at three different heights. Then for each harmonic of the microprocessor running at 8 MHz a specific task is performed to determine the positions and intensities of the lines of current.

As for the passive case, it is considered that the right model is the one that best matches the scans at different heights.

Fig. 5-120 and Fig. 5-121 illustrate the vertical magnetic field measured (Fig. 5-120) and simulated (Fig. 5-121) at 5 mm above the microprocessor, at 32 MHz, using a 1 cm diameter magnetic probe. The microprocessor radiated emission model can be presented as a set of vectors representing the current flowing into the component for each harmonic. These vectors are easy to handle and allow further processing, such as far field emission.

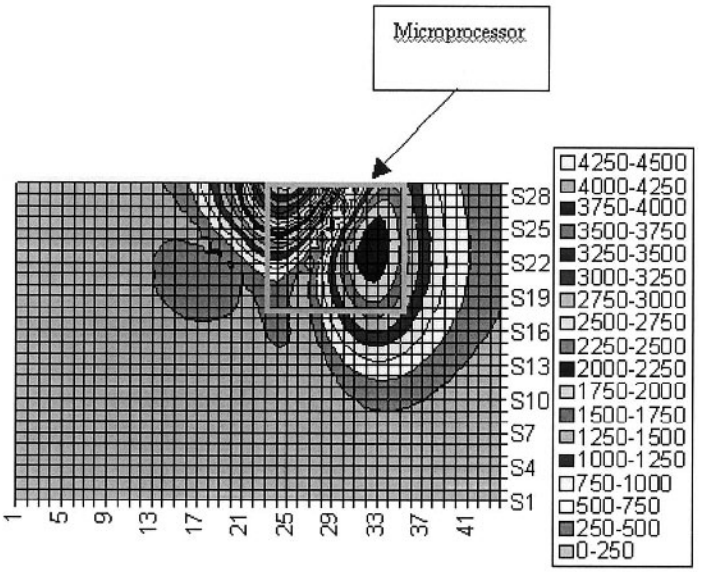


Figure 5-120. Measured magnetic field.

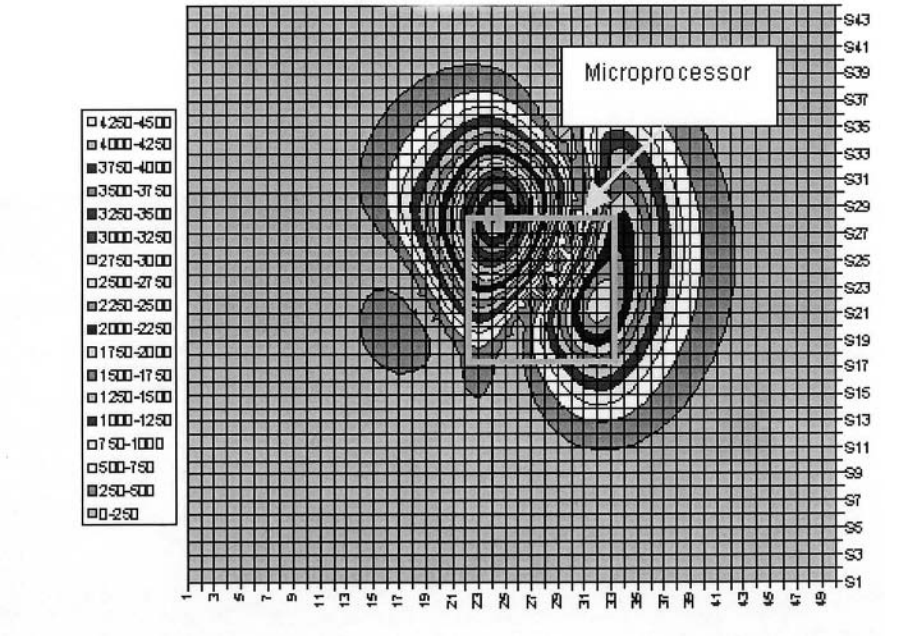


Figure 5-121. Simulated magnetic field.

10. CONCLUSION

In this chapter, most parasitic phenomena in ICs have been described, and several models have been proposed. Among these models, some of them have already been adopted as standards, whereas others are still under standardization process.

APPENDIX

Table 5A-1. Example of IBIS model structure (data deleted for brevity).

```
[IBIS Ver]      3.2                          | HEADER INFORMATION
[Comment Char]  |_char
[File Name]     sample.ibs
[File Rev]      3.0
[Source]        Teraspeed Consulting Group LLC.
[Date]          March 15, 2005
[Notes]         ....
[Disclaimer]    ....
[Copyright]     ....
|*****************************************************************************
[Component]     SAMPLE_NAME                  | COMPONENT SECTION
[Manufacturer]  XYZ
|-----------------------------------------------------------------------------
[Package]                                    | PACKAGE
| variable      typ          min           max
R_pkg           1.5243E-02     1.4866E-02     1.5620E-02
L_pkg           8.3838E-10     8.1763E-10     8.5913E-10
C_pkg           2.7715E-13     2.7029E-13     2.8401E-13
|-----------------------------------------------------------------------------
[Pin] signal_name model_name  R_pin     L_pin     C_pin    | PIN OUT
|                                      | PACKAGE
 1   _CE        INPUT      1.5620E-02  8.5913E-10  2.8401E-13
 2   SO         BI-DIR     1.4866E-02  8.1763E-10  2.7029E-13
 3   _WP        INPUT      1.4866E-02  8.1763E-10  2.7029E-13
 4   VSS        GND        1.5620E-02  8.5913E-10  2.8401E-13
 5   SI         INPUT      1.5620E-02  8.5913E-10  2.8401E-13
 6   SCK        INPUT      1.4866E-02  8.1763E-10  2.7029E-13
 7   _HOLD      INPUT      1.4866E-02  8.1763E-10  2.7029E-13
 8   VDD        POWER      1.5620E-02  8.5913E-10  2.8401E-13
|
|*****************************************************************************
[Model]         INPUT                        | MODEL
Model_type      Input
| ....
|*****************************************************************************
[Model]         BI-DIR                       | MODEL
Model_type      I/O
| ....
|*****************************************************************************
[End]
```

Table 5A-2. Expanded bi-directional model detail.

```
|*********************************************************************
[Model]        BI-DIR                          | MODEL
Model_type     I/O
|
Vinh  = 2.0V
Vinl  = 0.8V
Vref  = 0.0V
Cref  = 30.0pF
Vmeas = 1.65V
|
|-------------------------------------------------------------------
| variable     typ           min           max
C_comp         1.34pF        1.57pF        1.97pF
|
|-------------------------------------------------------------------
[Voltage Range]    3.30V       3.00V         3.60V     -
[Temperature Range] 50         100           0
|
|-------------------------------------------------------------------
[Pulldown]
-3.30000V      -247.125mA    -223.172mA    -280.762mA
-3.00000V      -224.669mA    -202.915mA    -255.253mA
| ....
|
 6.00000V       85.9530mA     69.9950mA     99.5520mA
 6.60000V       85.9530mA     69.9985mA     99.5520mA
|
|-------------------------------------------------------------------
[Pullup]
 6.60000V      -71.7678mA    -57.5256mA    -87.4081mA
 6.30000V      -71.0722mA    -56.8733mA    -86.5068mA
| ....
|
-2.70000V      134.178mA     120.892mA     149.624mA
-3.30000V      164.017mA     147.786mA     182.962mA
|
|-------------------------------------------------------------------
[GND Clamp]
| ....
|
|-------------------------------------------------------------------
[POWER Clamp]
| ....
|
|-------------------------------------------------------------------
```

Table 5A-2 Cont. Expanded bi-directional model detail.

```
[Ramp]
dV/dt_r        1.31336/1.02715n  1.10742/1.37071n  1.49148/852.312p
dV/dt_f        1.53482/1.01786n  1.33819/1.26112n  1.71328/917.270p
R_load = 50.0Ohms
|
|-------------------------------------------------------------------
[Rising Waveform]
R_fixture    = 50.0
V_fixture    = 0.00
|
 0.0000E+00     0.0000E+00     2.2551E-16     3.2960E-16
 1.0000E-10    -1.5841E-04    -4.8761E-04    -1.1753E-05
| ....
|
 8.9000E-09     2.1904E+00     1.8485E+00     2.4912E+00
 8.9600E-09     2.1897E+00     1.8491E+00     2.4921E+00
|-------------------------------------------------------------------
[Falling Waveform]
R_fixture    = 50.0
V_fixture    = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
|
 0.0000E+00     3.3000E+00     3.0000E+00     3.6000E+00
 1.0000E-10     3.2980E+00     3.0005E+00     3.6020E+00
| ....
|
 8.9000E-09     7.4265E-01     7.7012E-01     7.4567E-01
 8.9600E-09     7.4218E-01     7.7002E-01     7.4485E-01
|
|-------------------------------------------------------------------
[Rising Waveform]
R_fixture    = 50.0
V_fixture    = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
| ....
|-------------------------------------------------------------------
[Falling Waveform]
R_fixture    = 50.0
V_fixture    = 0.00
| ....
|
|*******************************************************************
```

Table 5A-3. Portions of IBIS multi-lingual additions for ICEM

```
| Some additions to the IBIS model:
|*****************************************************************   ********
[Circuit Call]  ICEM
| mapping  port      node
Port_map    vdd_ic    12
Port_map    vss_ic    14
[End Circuit Call]  | Code connecting  vdd_ic  to pin 12 and  vss_ic to
                    | pin 14.
|*****************************************************************   ********
[External Circuit] ICEM
Language SPICE
| Corner     corner_name     file_name   circuit_name  (.subckt  name)
Corner      Typ              icem_d60.spi   icem_typ
| Ports are in same order as defined in SPICE
Ports       vdd_ic     vss_ic
|*****************************************************************   ********
*  Separate SPICE file icem_d60.spi
*****************************************************************   ********
.SUBCKT icem_typ  vdd_ic  vss_ic
RVDD Vdd_ic Vdd_n1   2
LVDD Vdd_n1 Vdd_n2   2.2n
Cd Vdd_ic Vss_ic   3.2n
Cb Vdd_n2 Vss_n2   50p
RVSS Vss_ic Vss_n1   2
LVSS Vss_n1 Vss_n2   2.2n
Ib Vdd_n2 Vss_n2 PULSE(0.01 0.4 10ns 1.0ns 1.0ns 0.01ns 31.25ns)
.ENDS icem_typ
*****************************************************************   ********
```

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Chapter 6

CASE STUDIES

EMC Test-chips, low-emission microcontrollers

Abstract: This chapter presents a collection of case studies dealing with electromagnetic compatibility of integrated circuits. Emission and susceptibility of microcontrollers from several IC manufacturers are measured using standard methods and predicted using a macro-modeling approach. Specific test chips dedicated to the characterization of internal switching noise and to the validation of low emission design techniques are also described.

Key words: Test chip; microcontroller emission; microcontroller susceptibility; internal current switching; low emission design rules

1. *ST-MICROELECTRONICS* TEST CHIP FOR THE CHARACTERIZATION OF CONDUCTED AND RADIATED EMISSION

1.1 Overview

The CESAME test chip is dedicated to the characterization of conducted and radiated emission of six identical logic core blocks, each having a specific design technique which aims at reducing parasitic emission (Vrignon, 2004a, 2004b, 2005).

The first goal of the test chip is to validate these design rules and to quantify the benefits in terms of reduced parasitic interference. The second goal is the improvement of core modeling so that the impact of design changes on the level of emission may be forecast. Table 6-1 gives the identity card of the *ST-microelectronics* test chip.

A standard logic block is implemented in several versions, each one using design or process improvements. By integrating 6 similar blocks in the same chip, qualitative and quantitative comparisons are made possible.

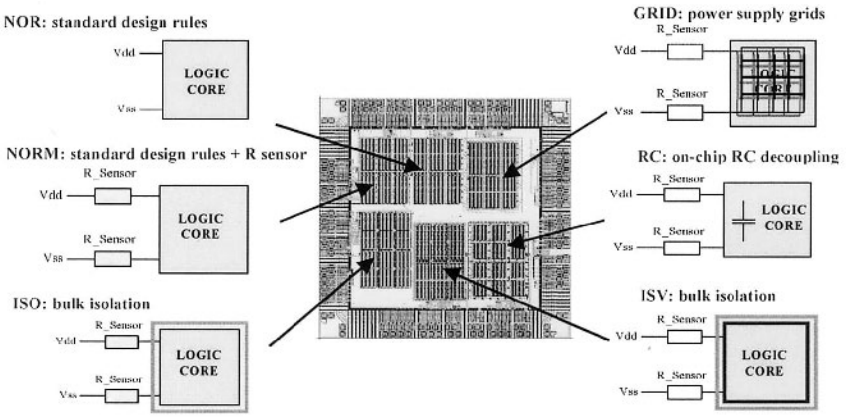


Figure 6-1. Internal blocks of the CESAME test chip.

Table 6-1. Identity card of CESAME test chip

Project name	CESAME
Main partners	*ST-Microelectronics*, France *LESIA*, INSA Toulouse, France MESDIE Project (Medea+ A509)
Design leader	L. Courau, *ST-Microelectronics*, I/O and Analog libraries, Crolles, France
Web sites	www.st.com, www.ic-emc.org
Technology	CMOS 0.18µm, *ST-Microelectronics*
Die size	3.3x3.3 mm^2
Packaging	144-pins TQFP, 20x20 mm^2
Complexity	700,000 transistors shared in six logic blocks
Circuit objective	Demonstrator for low emission
Scheduled	2002-2004

All these blocks have an identical structure reflecting the standard core activity. Each version has its own layout implementation in order to study layout solutions for reducing emission levels. Each block has a dedicated power supply so that its internal current consumption can be studied separately.

On-chip voltage sensors are connected to each logic block for studying voltage bounce and deducing the transient current of each power and ground supplies. The layout representation of CESAME is reported in Fig. 6-1. It includes 700,000 transistors, on a die size 3310x3310 µm, corresponding to a surface of 11 mm^2.

The first logic core, called NOR, is a standard one with no particular rules concerning the noise reduction. In the NORM core, we have added two 1.7 Ω resistors on the power supplies.

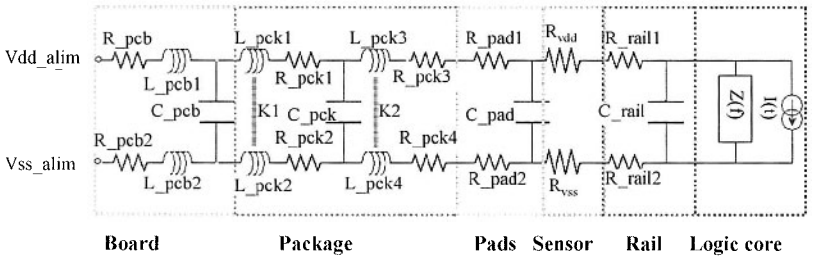


Figure 6-2. Complete model of the CESAME test chip.

The ISO and ISV cores have specific isolation with a buried layer. The GRID core uses a power supply grid and the RC core integrates a distributed decoupling capacitor, equivalent to 1 nF. All blocks, except NOR core, have two 1.7 Ω serial resistors on the power supplies.

1.2 Proposed Model based on ICEM

The modeling goal is to predict the internal current consumption with sufficient accuracy to optimize the floor plan and supply pads and to keep parasitic emission as low as possible. The approach used for the circuit modeling is based on ICEM (IEC 62014-3).

Table 6-2. Values for model parameters of RC core

Parameter	Description	Typical
I(t)	Core current, calculated with a transient SPICE simulation	400 mA
Z(f)	Core impedance, calculated with AC SPICE simulation	100 pF
C_rail	On-chip decoupling capacitance, extracted from post layout simulation	1 nF
R_rail	On-chip sensor resistances (calibration patterns)	1.7 Ω
Rvdd, Rvss	On-chip series resistance (inductance can be added), extracted from post layout simulation	1 Ω
Rpad	Pad access resistance, extracted from post layout simulation	0.1 Ω
Cpad	Pad access capacitance, extracted from post layout simulation	10 pF
Rpck	Series access resistance in package, calculated with electromagnetic CAD tool (HFSS and EMC 2000)	0.3 Ω
Lpck	Series access inductance in package, calculated with electromagnetic CAD tool (HFSS and EMC 2000)	6 nH
K1, K2	Coupling between access inductance, calculated with electromagnetic CAD tool (HFSS and EMC 2000)	60%
Cpck	Package supply coupling, calculated with electromagnetic CAD tool (HFSS and EMC 2000)	0.6 pF

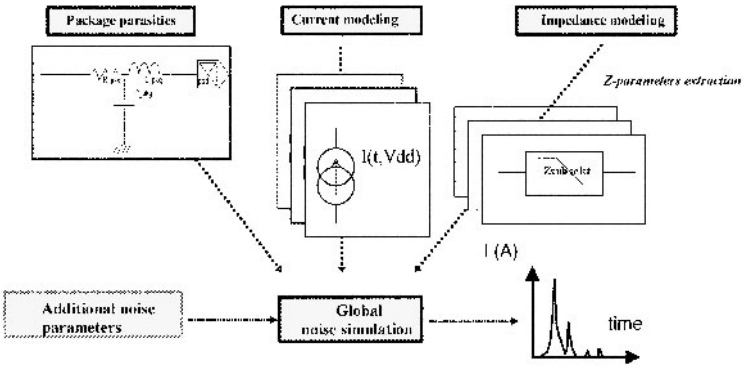


Figure 6-3. Global noise simulation.

The chip modeling task can be divided into several parts: board, package, pad-I/O, on-chip supply rails core impedance and on-chip switching current (Fig. 6-2). All these blocks are modeled using R, L and C elements. The current generator connected with an impedance represents the logic core.

The current source is obtained using a SPICE simulator. The result is stored in a file and is re-used in a global noise simulation as piece-wise-linear generator. We can also approximate the current peak by a triangular pulse. The impedance Z(f) is inferred from the AC analysis of the core.

The size elements of the RC network of supply interconnect are determined from post-layout extraction or calculated using analytical formulas and physical dimensions of the electrical circuit. In the case of long power supply rails within the chip, the series inductors L_{vdd} and L_{vss} should also be considered (Delorme, 1996; Grabinski, 1998). Typical values for package and chip parameters are given in Table 6.2.

After retrieving the waveform current and the equivalent power/ground impedance of the circuit, simulation leads to realistic supply bounces and current consumption of the block inside the package (Fig. 6-3). As the input/outputs have their dedicated power supply, we do not take into account the I/O corresponding to data or clock signals. But these parameters could be easily added to the simulation.

1.3 Measurements

The test chip is mounted on a TQFP144 package, low cost and easy-to-use. A dedicated board called ALI has been designed in parallel to explore conducted, radiated and on-chip measurements in a raw (Fig. 6-4).

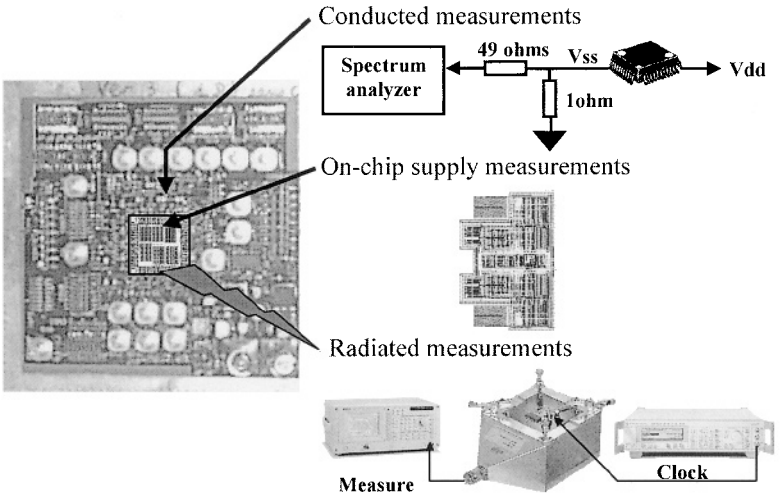


Figure 6-4. The CESAME test board used for on-chip current and EMI measurements.

Using an on-chip sensor, we measured the current peak directly on the supply rails inside the chip. As shown in Fig. 6-5, the GRID, NORM and ISV cores provoke the highest current peaks on V_{DD}, while ISO and RC cores are the least noisy blocks. Using decoupling capacitance (RC core) reduces the current peak by 60% with regard to the standard NORM core. The 1-Ω measurement confirms these results (Fig. 6-6).

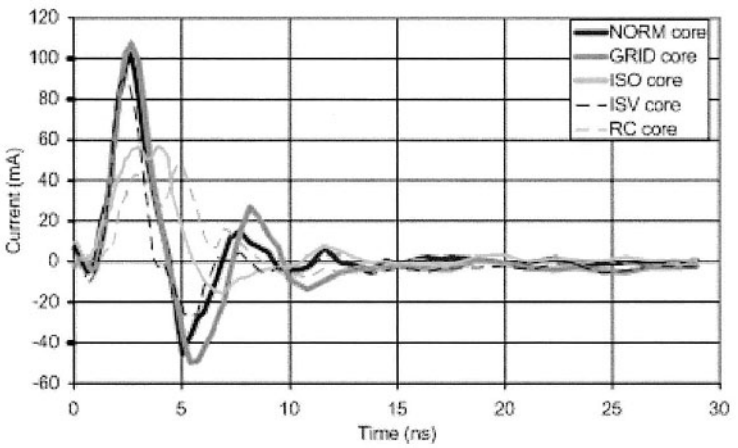


Figure 6-5. Current flowing on the Vdd supply rails, 100% activity, measured with on-chip sensor.

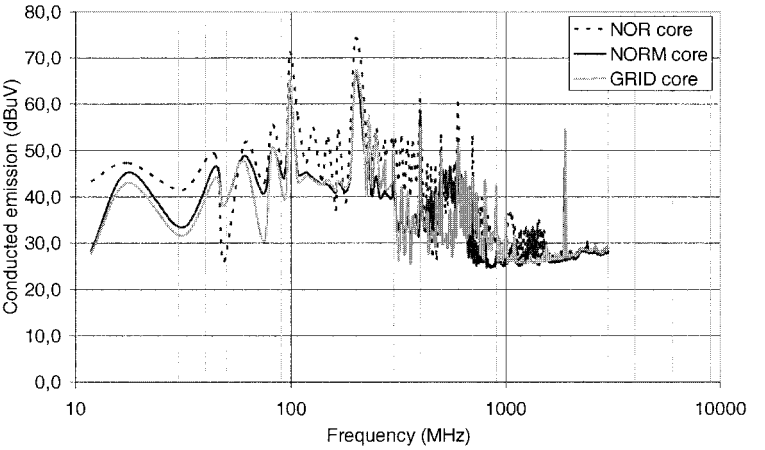


Figure 6-6. Conducted noise spectrum corresponding to 100% activity, 100-MHz clock and 20-MHz data for NOR, NORM, GRID cores.

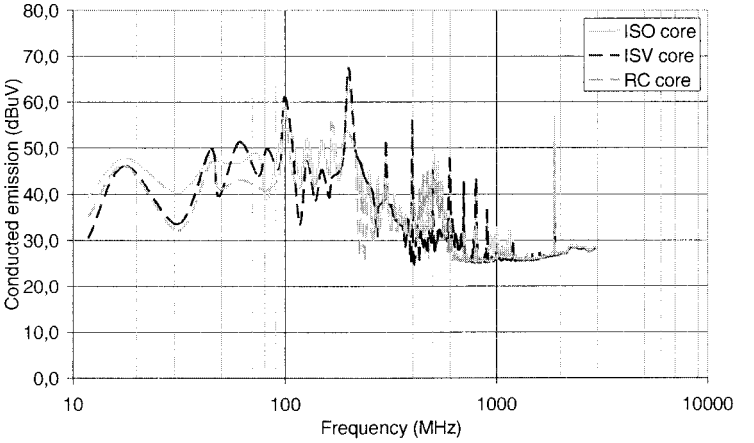
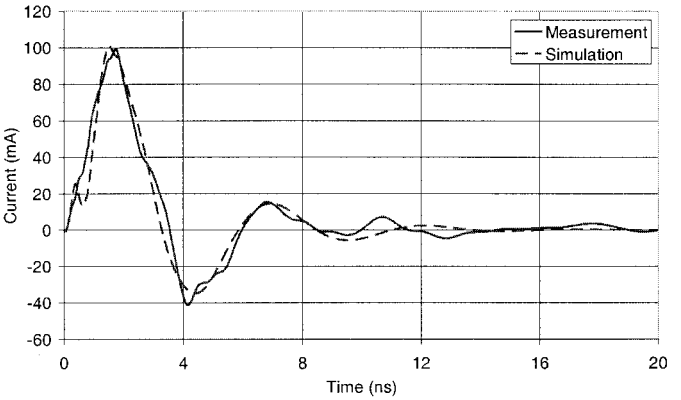
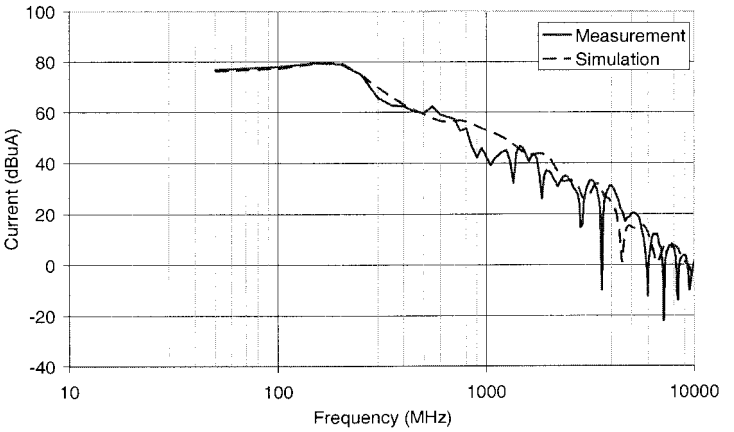


Figure 6-7. Conducted noise spectrum corresponding to 100% activity, 100-MHz clock and 20-MHz data for ISO, ISV and RC cores.

The conducted emission of the RC core is significantly lower than all other cores (Fig. 6-7), particularly at clock harmonics from 200 MHz to 600 MHz corresponding to the frequency at which the capacitive effect becomes predominant.



(a)



(b)

Figure 6-8. Comparison between on-chip measurement and simulation of the current through RVDD for the NORM core: (a) Time-domain results, (b) Frequency-domain results, calculated by FFT.

1.4 Comparison between measurements and simulation

In Fig. 6-8, the transient current waveform and current spectrum obtained through on-chip sampling are compared with the simulation using the ICEM model shown in Fig. 6-2. The current prediction is quite close to the measurement both in the time and frequency domain.

The difference from 700 MHz and 1.5 GHz can be corrected by adding a capacitor between the Vss node of the die and the Vss node of the board (1 pF) which represents the physical coupling between the die and the printed circuit board return reference.

Similar results are also obtained by comparing conducted emissions measurements and simulation. In this case, the model of 1-ohm measurement is added to the CESAME model. The positive impact of the on-chip decoupling and series resistance (RC core) is well modeled by changing the model parameter *C_rail* and *R_rail.*

1.5 Conclusion

Thanks to this test chip in CMOS 0.18µm, the current peaks on VDD supply have been characterized with a high precision. The internal current switching was accurately modeled, as compared with on-chip current measurements.

The effectiveness of emission reduction techniques such as on-chip decoupling capacitance and series resistance have been quantified in both the time and frequency domain. Significant reductions of the measured noise spectrum were observed in conducted emissions. A complete model, based on ICEM, including the core, the package, and the probe was developed for noise spectrum prediction. Good agreement between simulations and measurements of on-chip currents were achieved up to 10 GHz.

2. *PHILIPS* TEST CHIP: MULTI-PARAMETER ANALYSIS FOR THE INTERROGATION OF SI AND EMC MEASURES

2.1 Objectives

Many IC design houses, manufacturers and silicon foundries have SI and EMC rules and guidelines but the possible interaction between the various measures are mostly unknown. An EMC test-chip (Coenen, 2003) has been developed for the purpose of evaluating the presently known EMC design rules and of investigating some new measures such as power grid adjustments and dampening resistances between peripheral supply and substrate.

Instead of carrying out an experiment permuting One Factor At a Time (OFAT) a multi-parameter analysis technique, using Design-of-Experiments (DoE) was created with ultimately positive results (Box, 1978, Padke 1989).

Table 6-3. Identity card of Multi-Parameter test chip

Project name	Multi Parameter
Main partners	Philips
Design leader	Mart Coenen
Web site	www.philips.com
Technology	0.35µm CMOS from Philips
Die size	15 mm^2
Packaging	QFP44
Complexity	380k transistors
Circuit objective	Multi parameter analysis for EMC reduction
Scheduled	2000

The experiment was carried out with 8 core and 5 peripheral parameter settings considering 7 responses, meaning: $7 \cdot (3^8 + 3^5) = 47628$ relationships.

This first EMC test-chip (Table 6-3) has been designed in C075 (0.35µm CMOS) technology, as with the start of this project the proper RF device modeling was available. The evaluation results of the EMC test-chip are included in the on-chip EMC design rules for C075 and newer process technologies.

The EMC test-chip has been defined and has been measured by using the multi-parameter Design-of-Experiment (DoE) statistical method. A DoE method makes it possible to investigate a large number of factors/ parameters with relatively few experiments. There are two reasons for restricting the number of permutations: to minimize the number of IC test samples required and to restrict testing / measurement and simulation time.

2.2 Test-chip description

All parameters (known as factors in the DoE method) will be investigated at three levels, see Fig. 6-8. The three levels are chosen as an option to allow analyses of a higher order than linear (when only two or one levels are taken with the permutations) modes of influences. By proper parameters permutations chosen, the experiments are fully balanced (Box, 1978). A control block within the EMC test-chip can set some parameters. Those parameters that cannot be set by external control voltages have been implemented in separate hardware blocks.

The response measurements that are taken for the EMC test-chip as off-chip effects are; supply current and the supply current derivatives, the ground-bounce of the core and I/O and substrate voltage gradients. For the on-chip effects, the standard cell supply voltage and supply voltage ripple are taken as response parameters.

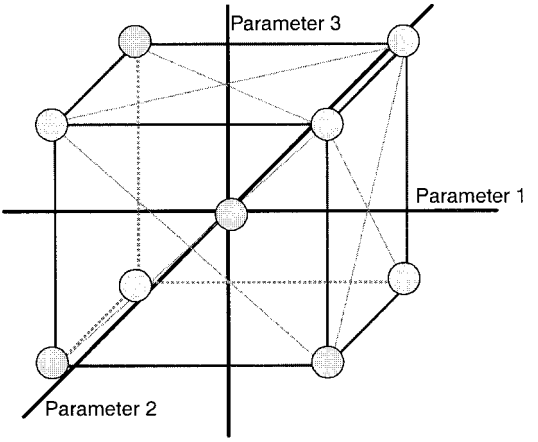


Figure 6-9. Experiment space for 3 levels

These variations of the voltage within the supply nets (cell voltage) on-chip as a function of the above will be simulated and measured to observe the margins for its functional behavior specifications.

The PCB used with the EMC test-chip has been designed according the requirements of (IEC 61967-1; IEC 62132-1) such that it fits into the various IEC standardized EMC test set-ups; TEM-cell and WBFC, which therefore allow further investigation of the implemented measures in the frequency domain, by taking the RF spectral emission characteristics with all the permuted modes of the PCB application.

2.3 Statistical Approach

First of all, all known on-chip related issues were collected. The chosen factors, parameters and their responses are taken orthogonal and/or independent from one another. For all the chosen variables or factors, the domain or range of investigation has to be considered up to practical levels that will allow inter- and extrapolation of the interactions found. The on-chip decoupling for example will be examined on its amount and placement. Also the type of decoupling (= RC time-constant) could be considered, but this has not been implemented with this test-chip. Power nets have been permuted in track width but not in spacing. As on-chip decoupling and power nets cannot be influenced afterwards, the full permutation of these factors (3 x 3 = 9 functionally identical cores) has been implemented.

The on-chip decoupling will have an interaction with the off-chip decoupling. The required amount of decoupling will be determined by the activity, the clock rate and the drive strength with the clock tree. Furthermore, the slopes of the signal(s) out of the clock tree may affect the response of the core(s).

The output drivers will be examined on their slew and non-slew rate behavior. For the latter, it is already known that slew-rate controlled drivers will produce less dI/dt than the non-slew rate controlled drivers. As the last stage of the output drivers are separated from the common substrate (library dependent), resonances might occur due to the parasitic capacitance between the output circuit geometry and substrate when combined with the lead frame and package inductances and the external capacitive loads. To control these resonances, resistors have been included between the V_{ssIS} (substrate) and the V_{ssE}. The external load to the output driver has an effect on the dI/dt of that driver.

The internal clock drive may be varied from a gentle slope to a steep slope. Using the knowledge that not all gates have the same transition threshold level, this will result in a wider spread in time of peak current. Intended clock skew between the several clock domains may be used to smear out the peak current over a longer time even further. The logical depth of the logic chain used between the flip-flops used also determines the smear of peak current.

The activity of the EMC test-chip can be varied from 0 (25 % is chosen as minimum) to 100 % dependent on the data content and the operation performed[5]. Since ICs have to comply with the EMC limits and have to remain running with all activities, the effect of activity is further investigated. Supply voltage variations will influence the behavior of the transition speed and cross current.

2.4 Measurable parameters

To enable comparison between the measurement and simulation results, the definition of the responses has to be unique and unambiguous for both areas. It will be obvious that many more response parameters can be analyzed from the simulation results than from the measurements, as all nodes of the EMC test chip design are accessible.

[5]Since the data and clock signals are fed into the test-chip via an AC coupled path, the average value of both data and clock has to be kept symmetrical in order not to disturb the DC-settings of the internal signals. The clock and data signals have to be locked in both frequency and phase.

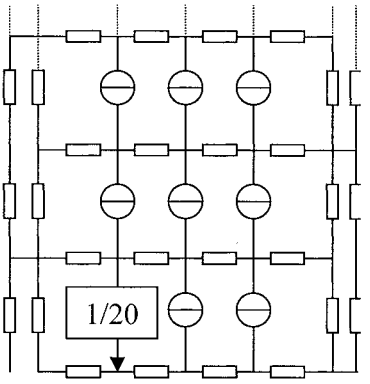


Figure 6-10. Macro model used with the simulations

Whereas signal integrity (SI) measurements are taken on-chip, most EMC measurements are taken off-chip. Special pads have been added to the core area to allow measurement of the cell supply voltages (differentially measured) again as a function of the various permutations given. The measurement of off-chip responses with respect to on-chip effects e.g. substrate noise, requires a decomposition of the results in the time and frequency domain.

To allow simulation of large ICs, macro-modeling has to be used, see Fig. 6-10, to allow analogue simulation of the overall chip by a SPICE simulator, Pstar (Philips propriety analogue simulation tool) or Spectre. For this purpose, a separate experiment has been carried out to derive the need for circuit and topology details in relation to the responses obtained. From the core design used it became clear that a sub-circuit could be used to represent the sub-core but that the overall power net could not be over-simplified to the need to have (negative) feedback of the power net onto the active circuit. With this experiment, the power-net parameters have been derived from the GDS2 files. Excluding this negative feedback to the 'source' resulted, with our experiment, to responses of the circuit that exceeded the supply voltage applied unrealistically.

2.5 Parameter range coding and decoding

The most crucial part, next to the choice of the parameters and their responses, is the coding of all parameters in such a way that a well-balanced statistical approach is possible.

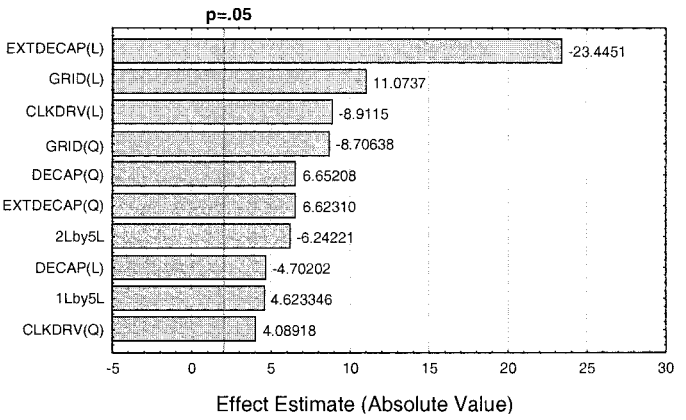


Figure 6-11. Pareto plot of the peak current response

For this reason all upper, lower and center bound conditions of the parameters were coded to: -1, 0, and 1 independently of the range in which the factors or parameters are varied (either on a linear or logarithmic scale). Based upon these normalized parameters relations (regression) between them and each of the responses were derived, each with a mean value and its deviation thereto. This normalization process requires that all parameters have to be quantitative, continuous and progressive.

As 8 core related factors were taken (subdivided in two groups of 5 and 3 leading to 46 and 15 experiments), their linear, squared and linear cross-interactions with each other have become possible contributors to the final response. By means of a Pareto analysis with a lower bound e.g. less than 5% influence on the response, the most critical parameters and their interactions were taken into the final equation for optimization, see Fig. 6-10.

Furthermore, when a parameter occurs in squared or by cross-interaction with another parameter, the linear parameter was taken into account too. From the response example: I_{peak}, in Fig. 6-11, it can be seen that the cross-interaction becomes significant at the seventh and ninth position. What can be observed from Fig. 6-11 is that the external decoupling has the most significant influence in de peak current occurring.

Furthermore, the factors: on-chip decoupling, power net resistivity and external decoupling show a higher than linear order impact on this response. Whether the quadratic approximation is sufficient to represent the interaction is determined by the width of the parameter domain applied.

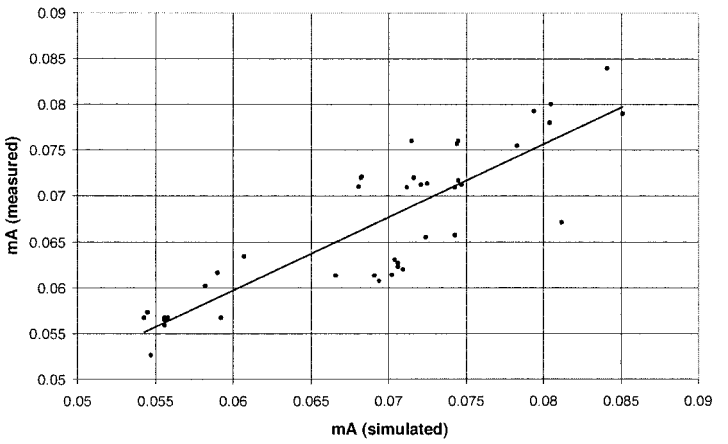


Figure 6-12. Example of the correlation between measured and simulated peak supply core currents for the various permutations.

Hereafter, each of the 7 responses can be weighted (in order of importance of the results to be obtained: EMC, speed, robustness, low-power, etc.) and the best overall setting of the factors or parameters can be derived to obtain an optimal overall response. For this reason, the weighting can also be normalized or a dominant response can be selected.

In Fig. 6-12, a correlation between the simulated and measured results is given for the first experiment with 5 core related factors. Although an 80% correlation is already quite satisfactory, several causes were noted which will enhance the correlation even further. Thereafter, decoding to the normalization functions used can derive the real optimum setting for each of the parameters. Furthermore, based on the fact that both a mean value and its deviation are known, the upper and lower bounds of these relations can be used to find out whether the optimum is critical or not e.g. by a Monte-Carlo simulation. The criticalness of the optimum can also be observed from the surface response plots of the various interactions. These plots (using Statistica from Statsoft ©) can also reveal whether further optima exist outside the boundaries of the domain chosen for experiments.

Fig. 6-13 gives a 3D-surface plot of the peak current as a function of 2 parameters where the other 3 are fixed to a certain value. As can be seen from the saddle curve, there are various options possible considering that the dark green area is considered an optimum at both sides of the saddle curvature. For the function above, the left hand side shows the lowest side. Whether this is also an optimum for the other responses is to be considered.

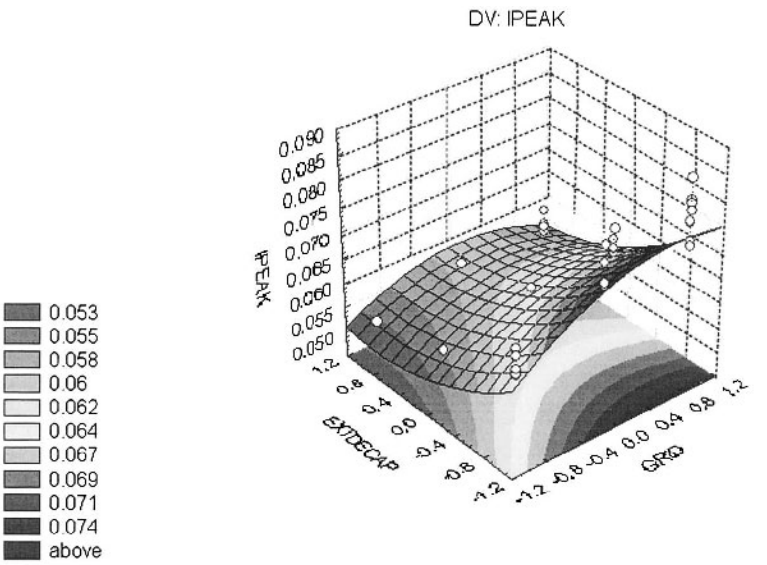


Figure 6-13. 3D-surface of I_{peak} response

2.6 Thorough analysis

As the results of the total EMC test chip experiment are not public, the interaction between the variables and factors used will also rely on:

- the silicon foundry IC process options
- the design philosophy (architecture) and
- the libraries i.e. circuits used.

Due to the good correlation between the simulations and the measured results, evidence was given that the approach used is suitable for other processes like high-ohmic substrate without epitaxial layer or low-ohmic substrate with epitaxial layer.

For the statistical analysis, the tool *Experimental Design* from *Statistica Statsoft* was used. For optimization a CQM tool called *Compact* was used. MS Excel spreadsheets can be used to carry out further analysis. The latter is extremely useful for studying various "what-if" optimizations with the interaction information obtained from the statistical analysis.

2.7 Conclusions

- The overall correlation between the simulation and measurement results is quite good. For the critical responses correlation factors of 0,8 have been found.

- There appears to be NO real conflict between the optimized parameter/ factor settings for EMC and those required to achieve optimal signal integrity performance i.e. robustness. This conclusion is drawn from the fact that the minimum cell voltage is hardly affected by the settings of the other parameters with the experiment.
- The minimum cell voltage occurring across the standard cells is substantially less than calculated from the static IR-drop. For the sake of robustness, either the cell voltage ripple or minimum cell voltage level can be optimized.
- The use of a Box-Behnken experimental set-up is more suited for the analysis of complex multi-parameter designs like Taguchi, mainly due to the balanced experiment that is established and influences are less confounded.
- When the relation between the various parameters, the interactions and their responses is unknown, it is clear that experiments need to be set-up by using (at least) 3 levels for each parameter. The settings should be such that the upper and lower bounds of a realistic design are considered.
- Within the discrete settings of the parameters/factors in their chosen domains, the response can be influenced by a factor of 12 in most cases for *di/dt*, substrate noise gradient and ground-bounce. Considering continuous values within the parameters of each domain, the upper and lower bound for this experiment could result in a ratio of 1:50 between the worst and the best cases.
- Allowing further extrapolation of the parameters/factors and their responses outside their given domains indicates even larger areas for improvement.
- The results have led to the insight that off-chip measures are of dominant importance, to minimize RF emission and improve RF immunity from the core supply system.

3. *INFINEON* TEST CHIP FOR ANALYSIS OF INTERNAL SWITCHING CURRENTS

3.1 Objectives

TASC, the Test chip for Analysis of Switching Currents, was designed to perform dynamic on-chip voltage and current measurements and correlate them with electromagnetic emission measurements in the frequency domain. Table 6-4 gives a list of TASC key parameters.

Table 6-4. Identity card of TASC test chip

Project name	TASC
Main partners	*Infineon*, MESDIE project
Design leader	T. Steinecke
Web site	www.infineon.com
Technology	0.13µm CMOS, *Infineon*
Complexity	150,000 transistors
Die size	11.5 mm²
Packaging	CLCC-68
Circuit objective	Demonstrator for low emission
Scheduled	2002-2004

3.2 Introduction

All TASC activities were carried out as part of the European funding project (MESDIE-A509) in the framework of MEDEA+. The principal motivation for the TASC chip was the difficulty of correlating behavioral emission models with measurements of switching currents. TASC measurement results led to a refinement and quality improvement of the behavioral models. These behavioral models are still on functional module level and called ECS (Equivalent Current Sources). ECS is the previous stage to ICEM models which describe the dynamic switching currents and noise coupling paths of a complete IC including the package. To meet these targets, TASC had to provide several new design features:

- Design of a highly sensitive and noise-robust on-chip sensor for current measurements in the range of 10-microamps in a 10-picoseconds time resolution.
- Design of regular scalable gate arrays to offer a wide variety of settings, covering switching currents from single gates to logic modules.
- Easy-to-use user interface for test chip configuration and measurement control.

3.3 Structure of emission models

Emission models have been described in detail in Chapter 5. However, for an understanding of the TASC chip structure it is essential to know about the special model requirements behind it. In general, emission models describe the switching current of more or less complex gate arrays, which are known to be at the origin of electromagnetic emission noise. For big logic modules, in addition to the noise sources, the noise propagation paths have to be modelled as well. These are the main power supply traces routed on the chip itself. IC-level emission models must also consider the power supply structures in the IC package.

Consequently, two research topics were started in parallel:

- analytical description of a logic gate's switching current (noise source part),
- impact of supply trace inductance on switching noise (noise propagation part).

The noise sources in a functional module are represented by "Equivalent Current Sources" (ECS). Since functional modules consist of many "simultaneously" switching gates, the switching currents of all single gates have to be overlaid in the time domain to get the total switching current. Although in modern digital circuits all flip-flops are triggered with the edge of a high-speed master clock, the subsequent logic gates offer propagation delays for the alternating signals rippling through the combinatorial logic. This effect led us to consider logic depths in digital logic. The resulting switching current pulse of switching logic issued by the master clock edge (which releases the new flip-flop states into the subsequent combinatorial logic) is formed by the delayed overlay of many single gate-switching currents at well-defined capacitive fan-out loads. Fig. 6-14 shows the principle of this logic depth approach.

By parsing the gate netlist of a synchronously clocked digital module, all gates can be assigned to a logical depth (LD), where LD=1 contains all gates which receive at least one of their inputs directly from the flip-flops controlled by the master clock. This approach assigns a certain time slot per logic depth, so all gates within one logic depth start switching at the same time. These simultaneously switching gates are replaced by one single gate with an equivalent switching current.

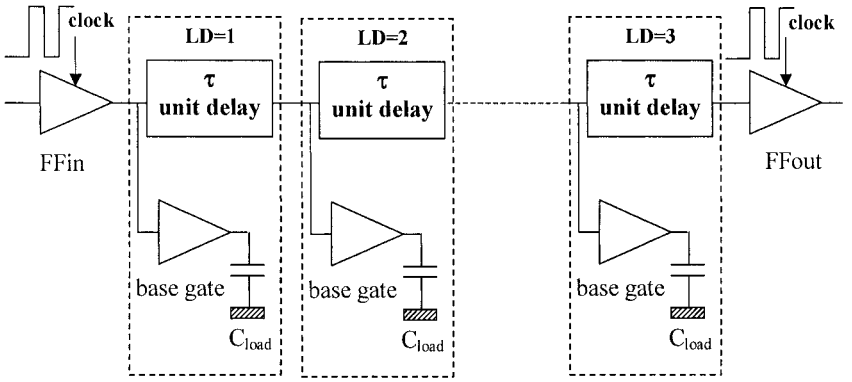


Figure 6-14. Logic depth structure in a synchronous digital design.

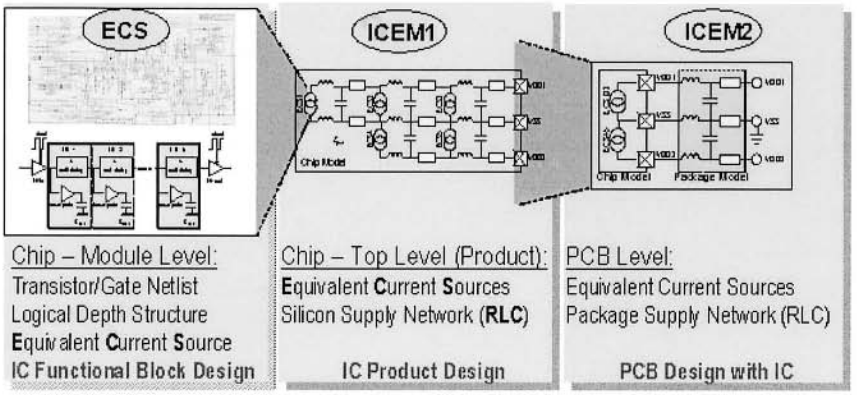


Figure 6-15. Emission model types.

The overlay of all these equivalent gates in the logic depth stages in the time domain leads to the equivalent current source (ECS) mentioned above. This is done by a SPICE simulation of a circuit which contains only the equivalent gates and their extracted load capacitance as shown in Fig. 6-14. At module level, the inductance of the power supply routing can be neglected as will be shown below.

In short, a logic functional module can be described as an ECS. A complete IC consists of many ECSs plus their top-level power supply routing. The power supply system extends through bond wires or bumps to a package lead-frame or substrate and finally to the package pins or balls.

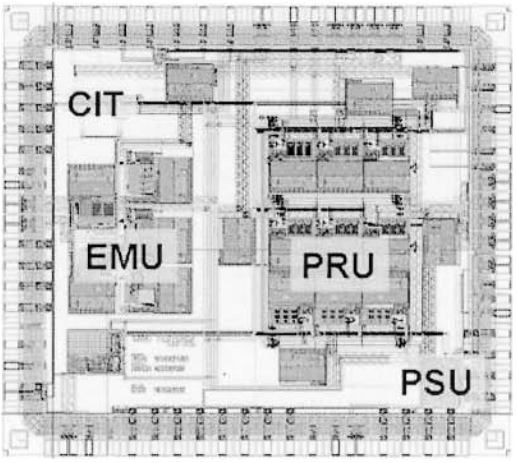


Figure 6-16. TASC modules.

This complexity leads to the need for different complexity classes of emission models. Fig. 6-15 shows the module-level ECS, the chip-level ICEM1 and the IC-level ICEM2. One or more (in case of big modules with a non-negligible area distribution) ECSs models represent the switching current of one functional module. ICEM1 represents a complete chip where many ECS are connected by a global power supply network described by lumped RLC circuits.

ICEM1 is used during the design phase of an IC to get the optimal module placement and power routing as well as power pad distribution during the feasibility and design phases of an IC. ICEM2 is the emission model format which will be given to users of the IC who want to run system-level emission simulations.

3.4 TASC building blocks

The TASC chip aims at the verification of equivalent current sources (ECS) describing switching currents at module level, and to a certain extent at ICEM1, where several modules are connected by global power traces. Consequently, it contains two major modules for model correlation:

- The EMI Modelling Unit (EMU) contains regular and irregular arrays of standard cells for verification of the module-level ECS models.
- The Power Routing Unit (PRU) consists of various local and global supply topologies for the evaluation of different supply concepts and for the correlation with the chip-level ICEM1 models.

In addition, a Port Switching Unit (PSU) contains 16 configurable pad output drivers for estimating the simultaneous switching noise. All other I/Os serve as control interface signals for configuration and on-chip measurement. The Calibration Unit (CIT) is required for sensor adjustment and trace inductance measurement.

TASC was manufactured in a 130 nm single-well CMOS technology which was the state-of-the-art platform for modern microcontrollers. The TASC layout is presented in Fig. 6-16.

For the evaluation of the quality of ECS models, it must be possible to measure systematic switching gate arrays. This is the only way to verify these scaled models which represent equivalent gates of more or less real switching gates. The EMU module therefore consists of a total of 2400 gates, structured in a matrix of 8 logic depths ("columns") and 300 rows. The number of rows and the number of logic depths activated for switching can be enabled from 1 to all. It is thus possible to switch only one single gate and measure its switching current by the on-chip sensor.

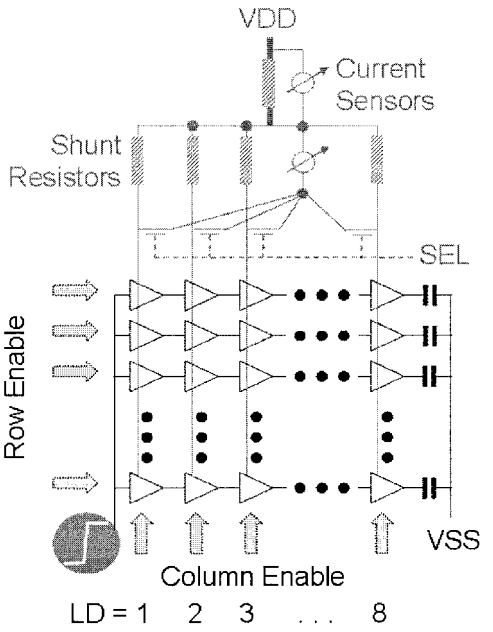


Figure 6-17. EMU gate matrix.

The 2400 gates are divided into 4 groups of different gate types: 3 groups of NAND gates with different driver strength, and 1 group composed of mixed gates. The NAND gates offer high-quality scaling correlation, whereas the mixed gates represent a more realistic functional module. Fig. 6-17 shows a diagram of the EMU gate matrix. Local current sensors are present at each logic depth and a global one per group. Due to the single-well CMOS technology used, only V_{DD} currents can be measured.

The quality of ICEM1 models is supported by the PRU module which consists of 9 logically equal gate arrays similar to the EMU matrix structure which use locally different power supply networks. These 9 submodules are surrounded by a "global" power supply ring which is connected to 4 power supply pin pairs located north, east, south and west. The 9 local power nets differ by type and amount of built-in capacitors. The global power ring can be disconnected from any of the 4 power pin pairs. It offers partly decoupling capacitors. Current sensors are placed in each main power entry. Fig. 6-18 gives an overview of the PRU module.

The impact of path inductance on the resulting switching currents is not negligible. It was shown that the inductance of on-chip supply traces is about 1 nano-Henry per millimeter, thus comparable with bond wire inductances.

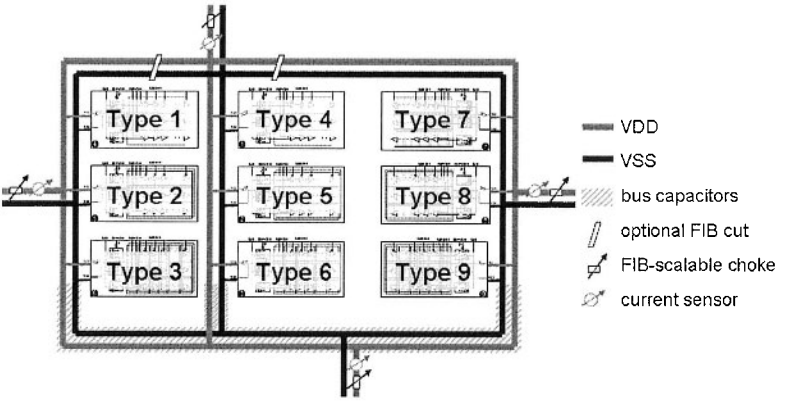


Figure 6-18. Submodule matrix.

An important task beside the supply current measurements with TASC was the development of a powerful inductance extraction methodology from GDS layout data. Partial inductance models were calculated by the Fast Henry tool based on a back-annotated layout netlist.

3.5 TASC current sensor

The on-chip current sensor module aims at measuring dynamic switching currents of single CMOS gates or groups of switching gates, resulting in a current range of 10 µA up to 100 mA. Since the gate switching takes place in the time range of 100 ps, a time resolution of 10ps is mandatory.

We use a sample-and-hold measurement principle where the desired time slot is divided into sampling points, and every measurement adds one current value for a dedicated time value in the result curve. Fig. 6-19 shows the measurement principle which had already been introduced on previous test chips for voltage measurements (Delmas-Ben Dhia, 2000).

One complete measurement takes around 1000 samples, depending on the selected time resolution. The switching phenomenon is therefore periodically triggered, and the switching current response is sampled along the time interval of interest. Special design care has to be taken for the sampling gate design since the current values vary in a picoseconds time range, thus the electric charges in the sampling gate have to be handled very carefully.

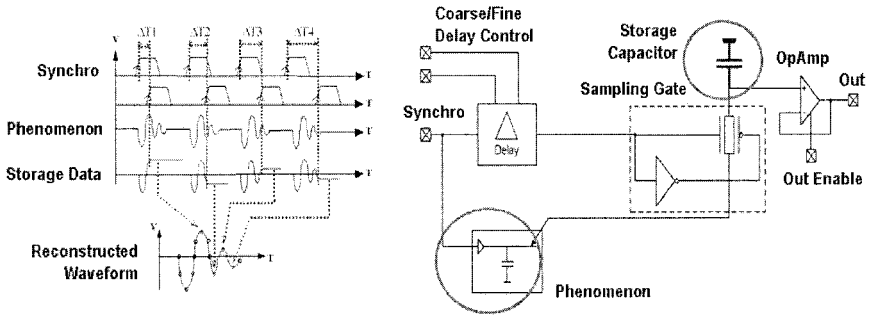


Figure 6-19. Voltage sensor measurement principle.

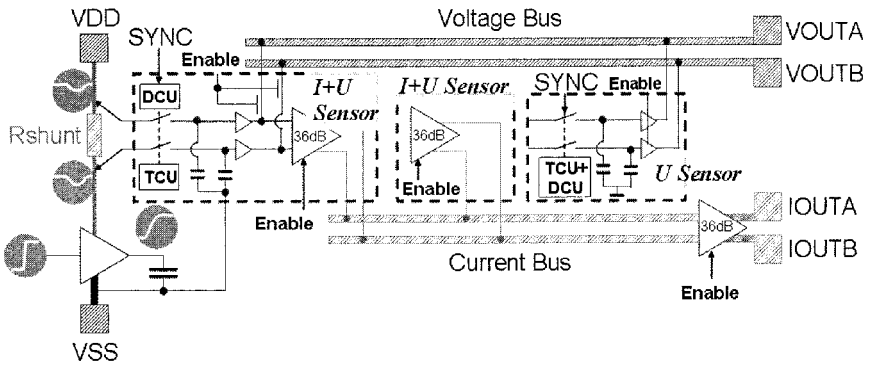


Figure 6-20. Voltage and current sensing and amplifying circuit.

The current is measured by two voltage measurements at a shunt resistor of 500 mΩ. Since the voltage drop over this shunt resistor is typically in the 100 μV range for small groups of gates, it has to be amplified by subsequent circuits to generate an output signal in the 1 V range which can be evaluated by off-chip circuits. Fig. 6-20 gives an overview of the complete current sensor circuitry used on the TASC chip.

The two voltage measurement nodes of the active current sensor are connected by the "voltage bus" VBUS to the TASC pins VOUTA and VOUTB. These are single-ended outputs with VSS reference. The differential signal of the measured current is available for external evaluation at pins IOUTA and IOUTB.

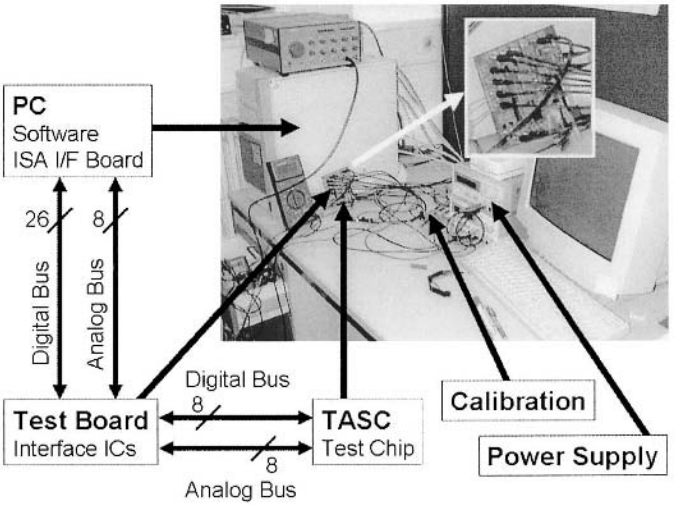


Figure 6-21. TASC test setup.

3.6 TASC test setup

The TASC test setup (Fig. 6-21) consists of the test chip itself, a test board which holds the test chip plus voltage regulators, amplifiers, oscillator and passive parts, an interface board mounted inside a PC with digital communication ICs and A/D and D/A converters, a PC running the control and measurement software.

The user software configures the test chip by sending commands to the JTAG interface built into TASC. These commands enable or disable test modules and select the measurement nodes for voltage and current. The measurement itself is then controlled by digital "start" and "ready" lines plus analog control voltages for the sampling delay. The measured voltages and currents are amplified on the test board if necessary and transferred to the PC interface card through 50-Ω cables.

In addition to voltage and current measurements in the time domain, the TASC test board was prepared for conducted and radiated emission measurements according to the international standard IEC 61967. Thus the test chip itself is the only component facing inside the inside of the TEM cell. Fig. 6-22 illustrates top and bottom views of the test board with 4" x 4" size.

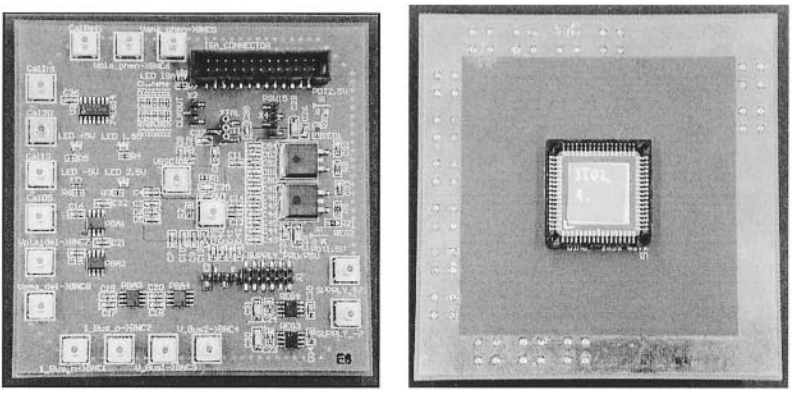


Figure 6-22. TASC test board (top and bottom layer).

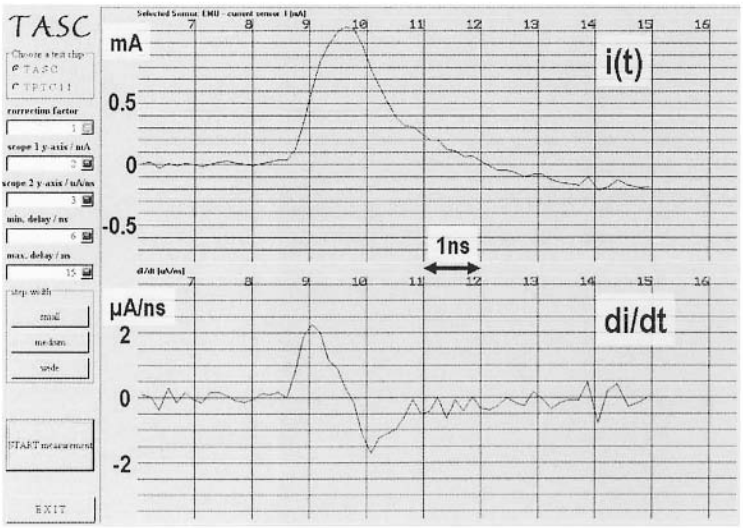


Figure 6-23. Current measurement on TASC

The control software for measurements in the time domain is strictly test module oriented. After program start, in an initialization window basic settings like oscillator/PLL and common current amplifier are done. It is also mandatory to run the calibration routine for the on-chip sensors. This chip-specific data is stored in a file and can be reloaded whenever this test chip is measured again. The module under test then has to be selected and configured by probing point selection and voltage/current sensor settings.

The measurement data are processed by the software and displayed graphically on the screen. Fig. 6-23 displays the switching current (pulse on top) of a chain which consists of 8 gates. The delayed current pulses of sequentially switching gates overlay, resulting in a relatively slow edge, a maximum, and an even slower decrease of current. From this pulse, the current derivative di/dt is calculated (with *di/dt* on the bottom).

3.7 Simulation of TASC modules

The purpose of the TASC test chip is the on-chip measurement of switching currents, depending on the circuit configuration. The influence of number and chaining of switching gates, i.e. noise sources, is evaluated by the 5 on-chip EMU modules. The influence of the power supply network, i.e. noise propagation paths, is evaluated by the 9 on-chip PRU modules.

The basic structure of EMI models was described above. As long as the TASC test chip was not ready for measurements, its building blocks were simulated with SPICE. Supply current simulations of the EMU modules visualize the propagation delay of the clock pulse along the logic depth of switching gates as well as the superposition of current pulses for simultaneously switching gates. Fig. 6-24 shows the total supply current pulse (left) and the delayed gate-unique current pulses of each gate in a chain of 8 mixed gates (right) in the EMU module. The total pulse is generated by overlay of the single pulses. The total switching current of a gate array can be calculated by the sum of all single-gate switching currents, delayed by their propagation delay time.

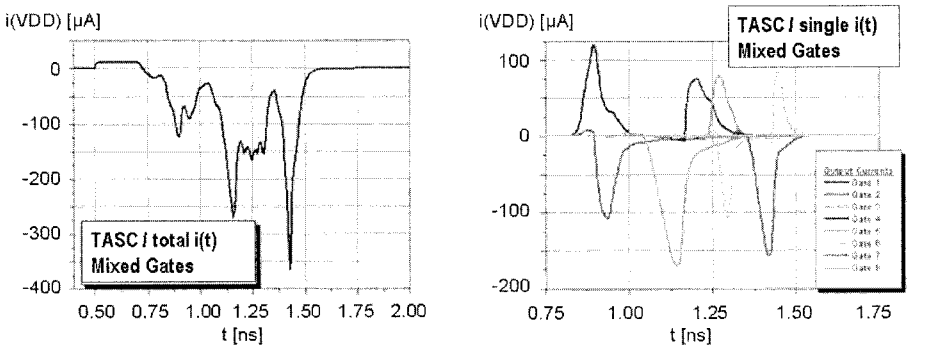


Figure 6-24. Switching current of EMU gate row – total pulse (left) and local pulses (right).

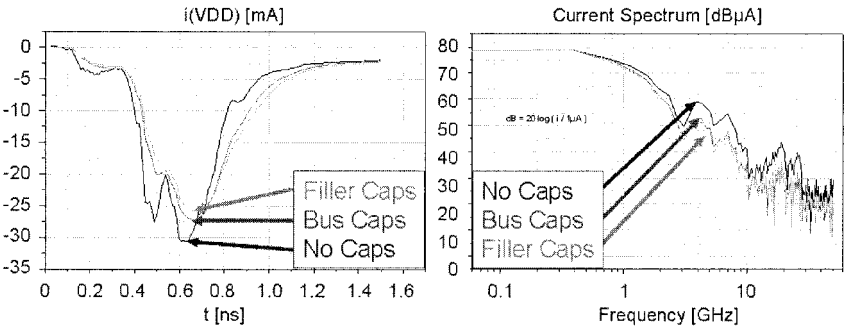


Figure 6-25. Switching current of PRU modules: time (left) and frequency domain (right)

The emission behavior of different power supply decoupling techniques has been evaluated on TASC modules PRU 1-9. Fig. 6-25 shows the difference between tree-shaped supply traces without any capacitors, with bus capacitors and with bus plus filler capacitors. The resulting supply current pulses are displayed in the graph on the left, the resulting frequency spectrum in the graph of the right. As expected, the amplitudes of the dynamic switching current increase by roughly 20% if no capacitors are placed close to the switching gates. Accordingly, the emission peak amplitudes rise roughly 6 dB. Furthermore, the current peak shows high frequency content – i.e. an additional local peak between 0.5 ns and 0.6 ns in the left diagram of Fig. 6-25.

3.8 Measurements in time and frequency domain

Measurements of the TASC test chip have been performed in the time domain using the on-chip sensors, and in the frequency domain, using the EMI test setups described in IEC 61967-4 (conducted emission) and IEC 61967-2 (radiated emission).

On-chip current measurements have been performed mainly in the EMU test modules to get current profiles of different gate array configurations. Variable parameters were the logic depth and the gate switching activity of every logic depth. The 5 implemented EMU modules consist of gates with different driver capability. Fig. 6.25 shows as an example two switching current groups for different driver strengths and varied logic depth.

As was expected, doubling the number of switching gate does not lead to a doubled switching current peak. The peak's amplitude depends heavily on the delays among all contributing switching gates.

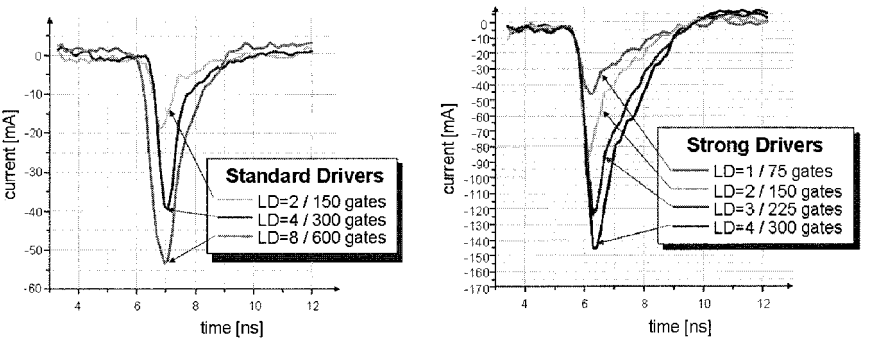


Figure 6-26. Measured switching current in EMU: standard (left) and strong drivers (right).

The more gates that switch simultaneously, the higher the current peak; delayed switching reduces the peak, but increases the duration of the current peak. In addition to the measurements in time domain, it is important to verify the correlation between increased or faster current switching and the resulting electromagnetic emission. Therefore the TASC test board was prepared for conducted and radiated emission measurements according to the international standard (IEC 61967) parts 2 and 4.

Fig. 6-27 provides two emission spectra overlays. The upper graph shows conducted emission on the power supply net in the case of one active PRU module and with all PRU modules active. The lower graph shows radiated emission in the same configuration. It can be seen that deactivating parts of the switching logic decreases the measured emission significantly. Consequently, functionally unused logic blocks should always have their clock signals disabled to reduce electromagnetic emissions.

3.9 Conclusion

The TASC test chip offers many opportunities to measure switching currents from single gates up to a few thousand gates. The biggest design challenge was the high-sensitive on-chip current sensor, which needs to transform milli-Volts of measured dynamic voltage across the shunt resistors into Volts on the analog output pins to be able to feed external A/D converters. For this purpose, this sensor has been optimized through a series of redesigns. In addition, a newer version of TASC offers the possibility of measuring dynamic currents on the V_{SS} net.

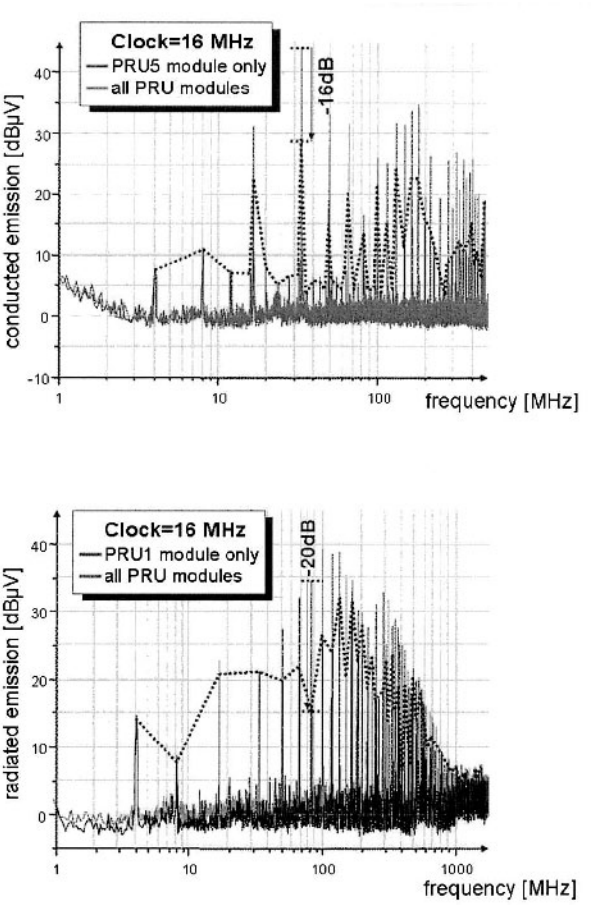


Figure 6-27. Conducted (up) and radiated (down) emission of PRU modules.

Results of these improved test chip versions are not yet available. For the next generation of measurements, where the investigation of EMC-optimized gate libraries is in the focus, the on-chip sample-&-hold sensors have been completely redesigned. They now offer 800 µA accuracy at 2 picoseconds digital time resolution. The analog-to-digital conversion is performed by an on-chip module, thus only digital signals leave the chip.

4. *FREESCALE* MICROCONTROLLER CONDUCTED EMISSION CHARACTERIZATION

4.1 Overview

The aim of this experiment was to measure and simulate the conducted parasitic emission of a 68HC12 microcontroller, with focus on the effects of input/output port activity. Table 6-5 gives the identity card of this microcontroller.

Table 6-5. Identity card of D60 microcontroller.

Project name	D60
Main partners	Motorola Gmbh, Motorola SSA
Design leader	Joachim Kruecken, Motorola Gmbh, Munich
Web site	www.freescale.com
Technology	0.25um, TSMC
Die size	22x22mm^2
Packaging	112-pins TQFP
Complexity	16-bit CPU, 60k bytes flash EEPROM.
Circuit objective	Modeling the conducted emission

The MC68HC912D60 micro-controller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (CPU12), 2-Kbyte RAM, 60-Kbyte flash EEPROM, 1-Kbyte EEPROM. The core (CPU12) of D60 is a high-speed, 16-bit processing unit, with a clock operating at 8 MHz under 5 V.

Table 6-6. Supply pins of the 68HC912D60.

Name	Specifications
V_{SS}	Logic Ground
V_{DD}/V_{SS}	Voltage supply of the component
V_{DDX}/V_{SSX}	Voltage supply of the buffers of I/O
V_{DDPLL}/V_{SSPLL}	Voltage supply of the Phase Lock Loop
V_{DDA}/V_{SSA}	Voltage supply of the ATD
V_{RHX}/V_{RLX}	ATD high and low reference values
V_{FP}	Supply which permits programming of flash memory
V_{PP}	Supply which permits programming of EEPROM memory

The technology used for this circuit (CMOS 0.25µm) supplies the digital core cells with 2.5 V, while the I/O and interface peripherals operate at 5 V. The 68HC912D60 is mounted on a quad flat pack (TQFP) and comprises 112 pins, of which some are dedicated to the supply voltage as listed in Table 6-6.

4.2 Microcontroller Suggested Model

The suggested model (Fig. 6-27), is based on previous works (Lubineau, 2000; Ross, 2002) and is composed of 3 blocs, 2 of which are integrated into the micro-controller represented by the ICEM model:

- Bloc 1: corresponds to the core of the 68HC12 *(Is, Cb)*, rails of power supply of 2.5 V and the coupling with the remainder of the blocks.
- Bloc 2: consists of the I/O with its power supply *Vdd* = 5 V and its commutation voltage control *Vio* between 0 and 5 V.
- Bloc 3: represents the interface with the measuring instrument (cable, probe and input impedance of the oscilloscope).

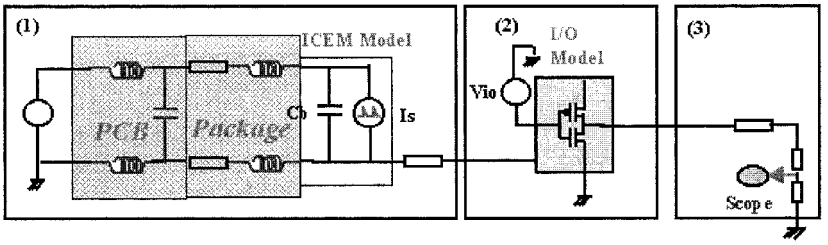


Figure 6-28. Suggested model.

We focused on the I/O activity effect on parasitic emission. The switching inverter of Block 2 generates sharp peaks of current which are one of the main sources of conducted and radiated emission. To build our I/O model, the DC characteristics of the driver had to be fitted with 68HC912D60 IBIS data. We used an inverter with nMOS and pMOS devices, and a SPICE model 3. We fixed the MOS channel length to 0.5µm, and fitted the width to match the IBIS information. We found that W= 90 µm for PMOS and W= 78 µm for the NMOS give an accurate fit with IBIS model (Fig 6-29).

The software tools used for simulation are listed below:

- *IC-Emc* (Sicard, 2005) draws the logic and analog schemas of the circuit, based on simple passive and active elements, and to generates files (.cir) that can be simulated by the analog simulator.
- *WinSpice3* (Smith, 2003) is used to simulate static and time-domain characteristics of the electronic circuit. *WinSpice3* generates simulation result text files which are post-processed to be compared to measurements.

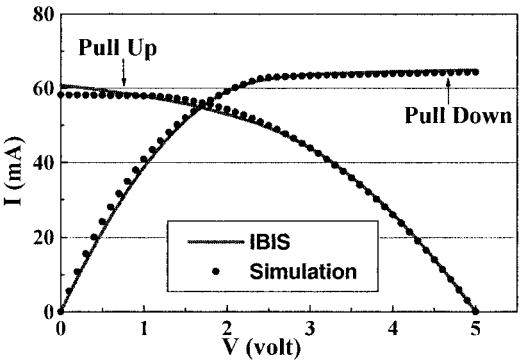


Figure 6-29. Fitting the IBIS I(V) for the NMOS and PMOS with SPICE LEVEL3 model.

4.3 Conducted measurements and simulation

The measurements are conducted using the Freescale evaluation board M68EVB912D60. The board consists of a 4- layer PCB which provides the interface and power connections to the MC68HC912D60 micro-controller (MCU). A test program is loaded in the micro-controller which activates one I/O (*PB*0) at its highest speed (2 MHz). Measurements consist in probing the signal produced on *PB*0, in order to characterize the switching noise and validate the I/O model. The time-domain measurement results are reported in Fig. 6-30.

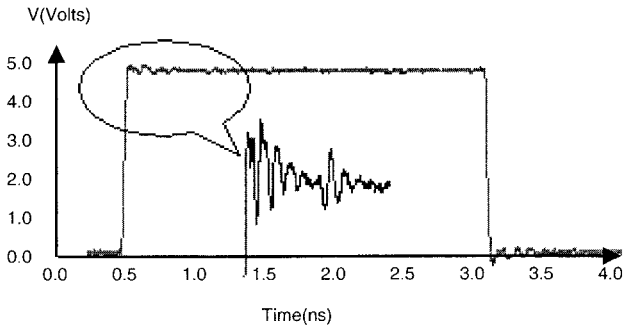


Figure 6-30. Signal measured on PB0.

The slight voltage oscillations observed on *pin PB*0 are mainly due to the internal decoupling capacitance of IC and the parasitic inductance of the package and PCB.

The spectrum (Fig. 6-30) corresponding to the time-domain measurements is obtained by Fast Fourier Transform of the time-domain oscilloscope information. In this figure, the level of harmonics around 80 MHz is slightly higher than the general negative decreasing trend, which confirms the observation in the time-domain measurements.

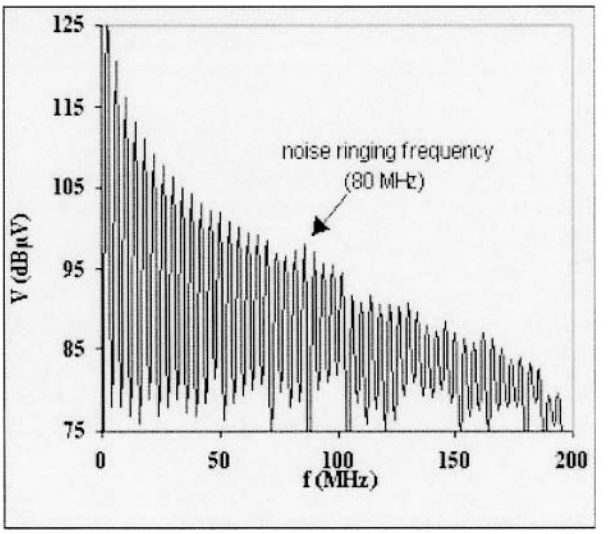


Figure 6-31. Frequency domain spectrum of the signal measured on *PB0*.

Indeed, the strong and rapid variation of the current crossing the rails of power supply causes important fluctuations of the internal supply voltage because of the parasitic inductance of the tracks of the micro-controller. Physically, these inductances correspond to the "bonding" wires connecting the chip to its case, the package "leads" as well as tracks of the printed circuit board (Schuster, 2000).

In the final I/O model shown in Fig. 6-32, the series resistances *Rb1, Rb2, Rb3* and *R4* are used to absorb some part of the current flowing through the MOS devices, thus causing a fall of the output voltage, according to the time-domain waveforms observed with the oscilloscope. Physically, these serial resistances account for the long metal supply lines on-chip.

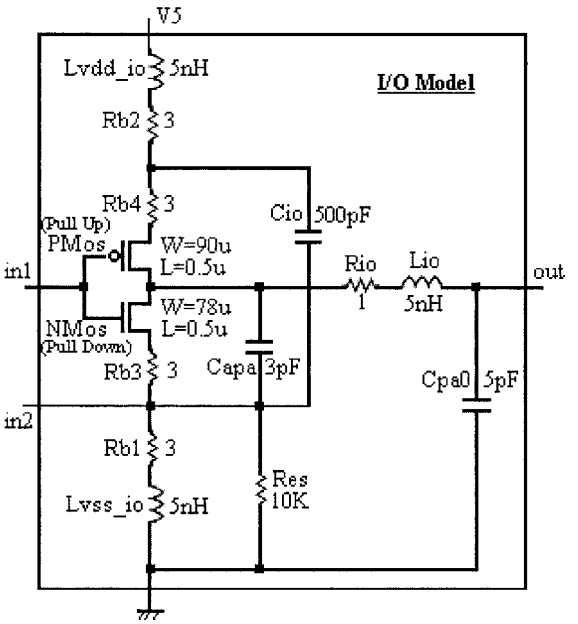


Figure 6-32. Suggested model of I/O

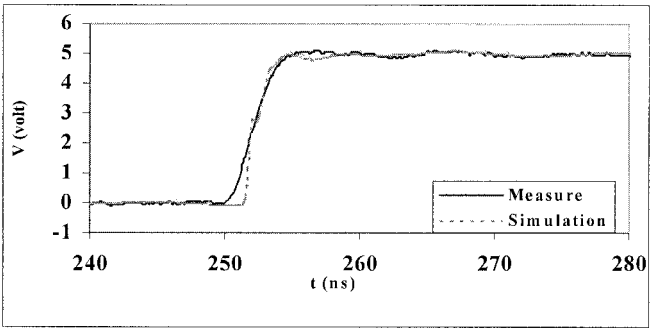


Figure 6-33. Rise front of the simulated and measured signals.

After several changes of parameters of the suggested model (ICEM and I/O), the time-domain simulation of the I/O switching with *WinSpice* leads to results shown in Fig. 6-32. In this figure, we show the comparison of conducted emission measurements with the simulation results. It can be seen that results from the measurements and the simulation are very similar.

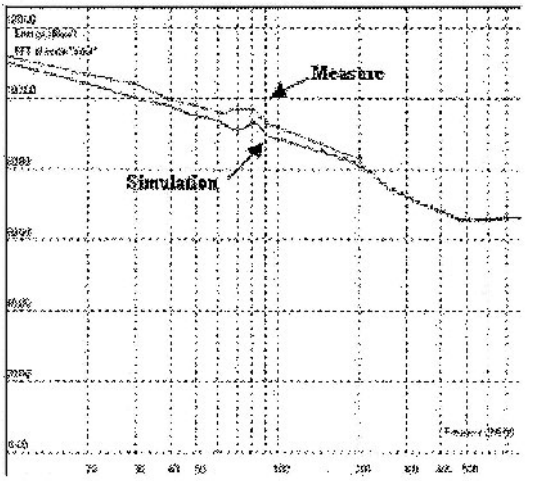


Figure 6-34. Comparison of the simulated and measured spectrum.

From a comparison between measurement and simulation spectra shown in Fig. 6-34, we find that the switching ringing enhances the harmonic levels near 80 MHz in the spectrum. According to the theory, the resonance frequency of an RLC circuit can be calculated by Eq. (6-2).

$$f_c = \frac{1}{2\pi\sqrt{2L_{pkg}C_d}} \tag{6-2}$$

Where
L_{pkg} *is* the package inductance (=1nH)
C_d is the internal decoupling capacitance (=2pF).

4.4 Conclusion

In this section, conducted emission measurements and the model have been applied to a 68HC12 microcontroller and the I/O model has been validated. The model is able to predict the resonance due to internal decoupling capacitance and package and PCB parasitic inductances.

5. *ATMEL* MICROCONTROLLER CONDUCTED EMISSION CHARACTERIZATION

5.1 Overview

This study proposes a methodology aimed at modeling and predicting the conducted emission level of an 8-bit microcontroller. This approach, using the ICEM model, allows reusable, behavioral dynamic activity models to be built that can be combined in order to evaluate the whole activity of a complex IC, including inputs and outputs as well as highly integrated blocks. Comparisons between simulations and measurements have been performed on the VIPER microcontroller (Table 6-7).

Table 6-7. Identity card of VIPER microcontroller

Project name	VIPER (89C51 family)
Main partners	ATMEL
Design leader	Jean Luc levant
Web site	www.atmel.com
Technology	0.35 µm, ATMEL
Die size	9 mm^2
Packaging	44-pin QFP
Complexity	8-bit CPU, 48-MHz external frequency, CPU core (70000 transistors)
Circuit objective	Modeling the conducted emission

5.2 ICEM model

Although the commercial version of the microcontroller is packaged in a 44-pin QFP, EMC measurements were performed on a chip-on-board version mounted on a special-purpose PCB. Fig. 6-35 shows a photograph of the test board.

A SMA connector is mounted on the other side of the board and is used for power supply as well as for impedance measurements. A 1.2-Ω precision resistor is also soldered on the VDD pin of the chip and measures its external current thanks to a differential probe.

The ICEM model of the passive distribution network (PDN) of the VIPER microcontroller on its PCB has been extracted by measuring the Z11 parameter of the power supply using a network analyzer.

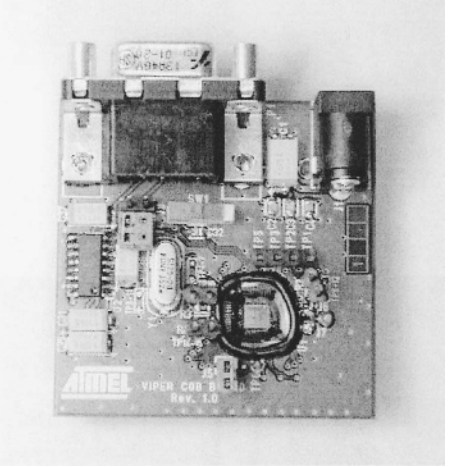


Figure 6-35. VIPER test board (chip-on-board version).

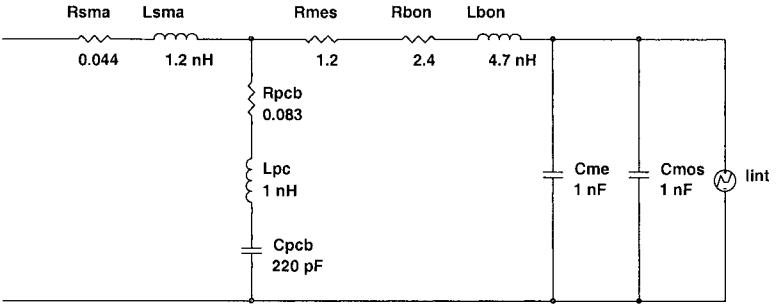


Figure 6-36. ICEM model of the VIPER microcontroller.

The equivalent lumped-element model is given in Fig. 6-36. This model depicts from left to right:

- The RL model of the SMA connector.
- The RLC model of the PCB.
- The measurement resistor.
- The RL model of the bonding and power supply rails.
- The equivalent metal capacitance *Cmet* of the rails.
- The equivalent MOS capacitance *Cmos* of the whole circuit.
- The equivalent current generator representing the CPU core alone.

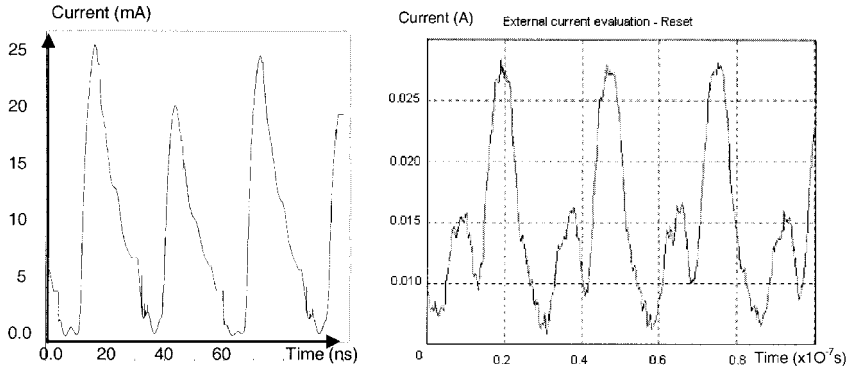


Figure 6-37. simulated (left) and measured (right) external currents of the CPU core

Both equivalent capacitances can be differentiated by measuring the *Z11* parameter without power supply (giving only *Cmet*) and with power supply (giving *Cmet* and *Cmos* in parallel).

5.3 Simulations

5.3.1 CPU core simulation results

5.3.1.1 Internal and external currents

The internal current of the CPU is extracted by means of a transistor-level simulation of the netlist powered by an ideal voltage generator. This netlist is then combined with the ICEM passive network obtained from measurements, in order to estimate the external current on the VCC pin. Fig. 6-37 depicts behavioral simulation results and real measurements of the external current through the 1.2Ω resistor.

It can be seen that, although peak values and transition times are identical in both cases, an additional spike is visible in these measurement results and not in the behavioral simulation. This can be explained by the high-current clock driver which is not simulated in the CPU core alone.

A PWL behavioral conductance model, including the simulated MOS capacitance, is then coded in VHDL-AMS and is used as a replacement for the transistor netlist. The total simulation time is then divided by 2500 while still providing enough accuracy for an EMC-oriented simulation.

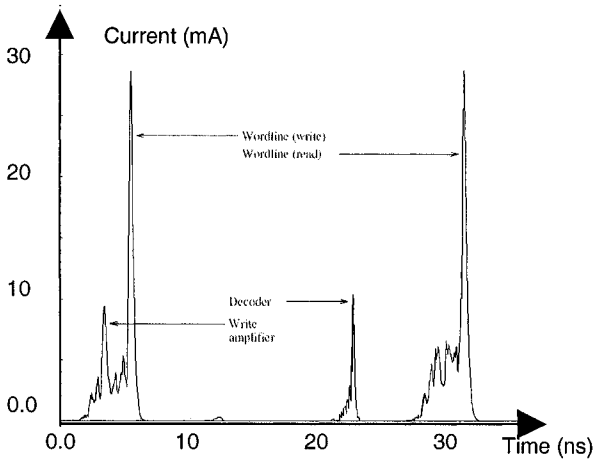


Figure 6-38. Example of dynamic activity for SRAM accesses.

5.3.2 SRAM modeling and simulation results

A SRAM (Static RAM) is made up of several building blocks:

- A memory array organized in sub-blocks.
- An address decoder selecting sub-blocks, rows and columns.
- An interface circuitry with write amplifiers, sense amplifiers and output buffers.

Each block has its own dynamic activity, which can be de-correlated from the others thanks to an accurate analysis of the architecture of the SRAM. Fig. 6-38 shows an example of dynamic current activity for a write access followed by a read access.

5.3.2.1 VHDL-AMS model of the SRAM

The SRAM is described in VHDL-AMS by an event-driven model similar to the one used for the core. However, each sub-block (X, Y and Z decoders, memory cells) is modeled by a separate VHDL-AMS process generating its own PWL waveform. Fig. 6.39 shows the results obtained with the SPICE netlist and the VHDL-AMS model. Simulation times are 1 hour for the netlist and 4 seconds for the model, which clearly demonstrates the usefulness of behavioral modeling.

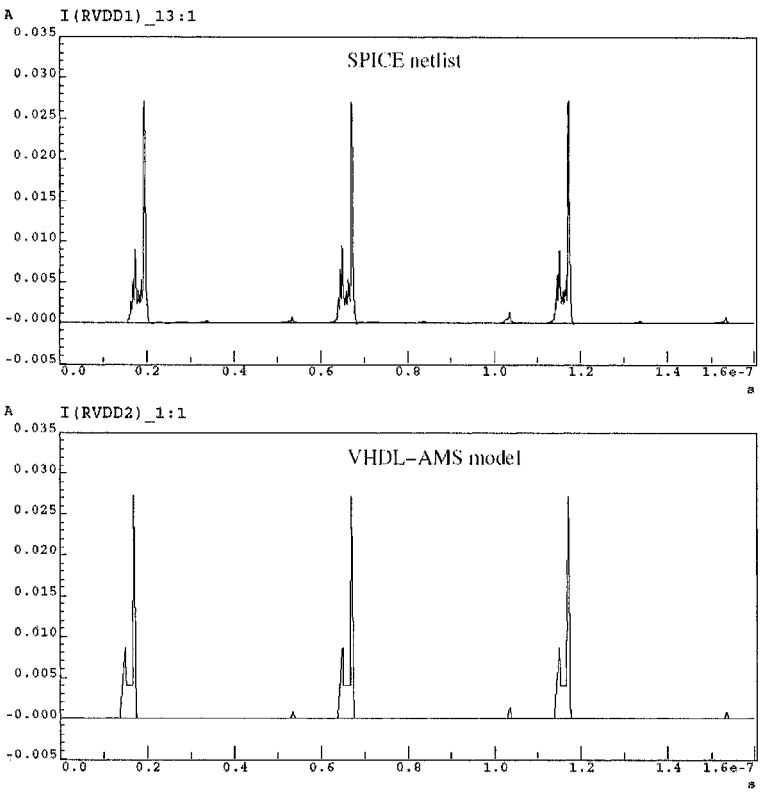


Figure 6-39. SRAM simulation: SPICE netlist (top) and VHDL-AMS model (bottom).

5.3.3 I/O simulation results

The objectives of I/O simulations are to verify the influence of the clock driver of the μC on the total current consumption, and to characterize and quantify the crosstalk between the core and the I/Os of the μC.

5.3.3.1 Influence of the clock driver

In order to characterize the influence of the clock driver on the total current in RESET mode, a couple of I/Os were instantiated and loaded by the same circuitry as on the existing PCB. In particular, rise and fall times were measured and introduced in the simulation.

The only difference between the real μC and the simulated version lies in the strength of the driver (weaker general-purpose I/Os were used in order to extract only one parameter set for the models).

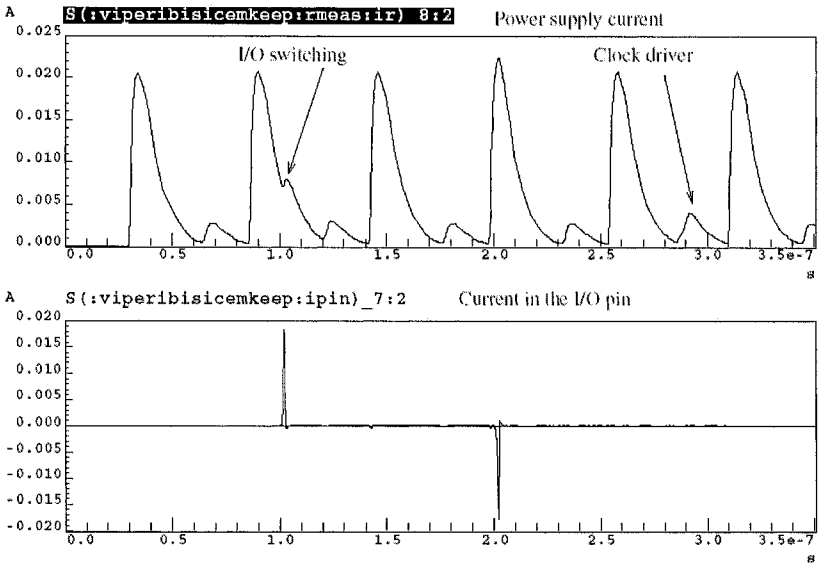


Figure 6-40. Simulation results for the clock driver (VHDL-AMS model).

Simulation results for the behavioral VHDL-AMS model are plotted in Fig. 6-40. By comparing the results with those displayed in Fig. 6-37 (left), the additional pulse in the middle of the period is clearly visible and correlates better with the measurements displayed on the right of the same figure.

5.3.3.2 Core-I/O crosstalk

As can be seen in Fig. 6-40, an additional general-purpose I/O is switched up and down during operation within the simulation performed in the previous paragraph. The corresponding results are zoomed in Fig. 6-41.

These results have to be interpreted from a qualitative point of view. In fact, a better knowledge of the effective coupling circuitry between the core and the I/Os would be required for accurate prediction. Anyway, this simulation demonstrates that voltage drops due to core activity propagate onto the I/Os themselves. Conversely, the switching of an I/O has a clear influence on the external power supply current.

These results may be helpful for the design of a low-emission integrated circuit, for the choice of PCB decoupling capacitors and for signal integrity analysis.

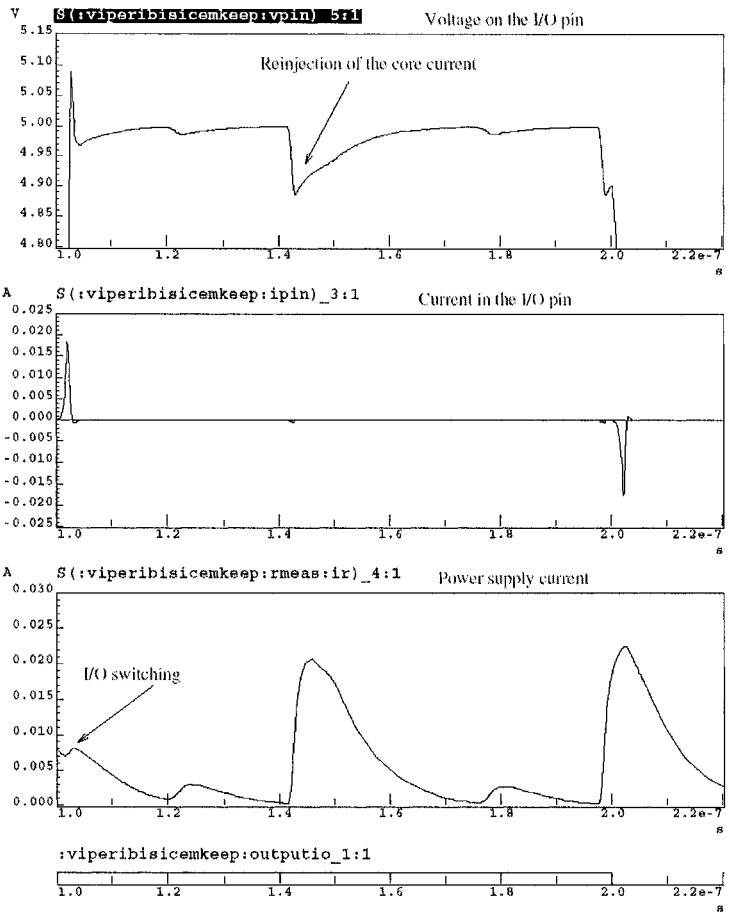


Figure 6-41. Core-I/O coupling.

5.4 Conclusion

In this case study, the use and the validity of the ICEM model were demonstrated from the correlations observed between simulations and measurements. A methodology for activity-dependent modeling was then designed and presented in the case of a SRAM block. Finally, the cross-dependencies between the core and the I/Os of the circuit were studied and linked together with CPU core activity in order to improve simulations.

These results clearly show that the ICEM model can be used to predict conducted emission before the first tape-out of an integrated circuit.

6. SUSCEPTIBILITY OF INTEGRATED INVERTERS TO HIGH FREQUENCY AGGRESSIONS

6.1 Overview

The aim of this experiment was to improve our knowledge about susceptibility of integrated circuits to high frequency aggressions (Pozzolo, 2002), with the sight of an equipment manufacturer. The second goal is to propose a methodology in order to create an electrical model able to simulate circuits under threat, thanks to SPICE-like computations.

Several aggression experiments were done and it was important to use simple integrated circuits to understand the phenomenon and to have the possibility to compare technologies. Moreover, these circuits had to be relatively recent: with low voltage, a compact package and very fast CMOS technology.

6.2 Devices under test

6.2.1 Digital Circuits

In order to fulfill all the technological criteria of the test (low voltage, compact package, simple function), logical inverters from Texas Instruments (6 items per package) seem to be a good solution as they propose IBIS models for each circuit. Fig. 6-42 shows the pin-out of a circuit. Table 6-8 presents the circuits used for the experiments.

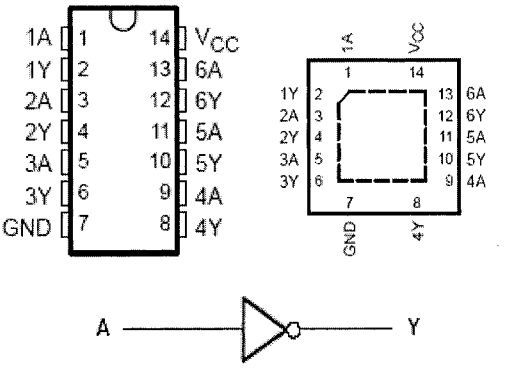


Figure 6-42. Pinout for SOIC, TSSOP (left), and QFN (right). Function of the circuit.

Table 6-8. Circuits used for the experiments

References	Supply Range	Packages available
SN74AHCT04	4.5 V to 5.5 V	SOIC, TSSOP, QFN
SN74AUC04	0.8 V to 2.7 V	QFN
SN74AHC04	2 V to 5.5 V	SOIC, TSSOP, QFN
SN74ALVC04	1.65 V to 3.6 V	SOIC, TSSOP, QFN

With such different types of circuit, it will be possible to deduce after several experiments what the main factors in the circuit susceptibility are, such as packages, speed or supply voltage. All of these circuits are very fast: time delays between IN and OUT are often below 2 ns and rise times are often near 50 ps.

6.2.2 Printed circuit board

To avoid losses during direct injection, circuits were mounted on a special PCB made in ROGER 4003. Permeability of this material is known and constant over 10 GHz. Such a PCB is dedicated to characterizing integrated circuits. The first layer of the PCB is dedicated to the signal and the second layer to the ground plane. V_{dd} and pins (IN) and (OUT) of one inverter are linked through a 50 Ω-matched track to a SMA connector for PCB.

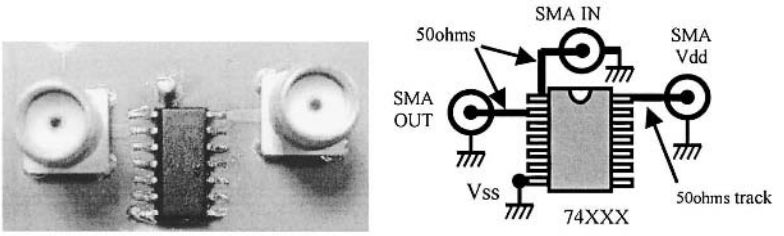


Figure 6-43. Connectivity of a circuit under test.

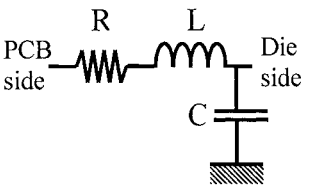


Figure 6-44. Package model from IBIS file.

The shield of this coaxial plug is connected to ground. The V_{ss} pin of the circuit under test is directly connected to the ground plan, through the PCB, with a wire as short as possible to reduce inductive effect. Fig. 6-43 represents the connectivity of the circuits under tests.

6.3 Model description

First, the integrated circuit model is based on the IBIS model supplied by Texas Instruments, manufacturer of the circuit. Each pin used (V_{dd}, V_{ss}, IN and OUT) is modeled in the IBIS file by a simple RLC circuit as shown in Fig. 6-44. For our modeling, we did not take into account parasitic effects between pins used and other pins of the package (inductive or capacitive coupling). L represents the inductive effect of the package and C, the capacitive effect with the PCB ground plane.

I(V) curves supplied by the IBIS file are completed and improved thanks to I(V) characteristics measured with a Tektronix 370A on the four pins that we used. Hence, a SPICE model of ESD protection and output transistors can be deduced. For ESD protection, a Zener diode appeared to be the simplest and the best model for input protection (Wang, 2002), and two clamping diodes are used to model output protection.

Texas Instruments and the IBIS file of the circuit do not give any information about an internal inverter model. The circuit under test works in 5V, so it is possible to consider that the circuit is most probably made in CMOS technology near 0,5µm. Thanks to the IBIS file that indicates electrical performances of the circuit output, it is possible to deduce of the dimensions (W and L) of the output stage. Fig. 6-45 gives atypical inverter behavior simulated with SPICE and deduced from I(V) curves.

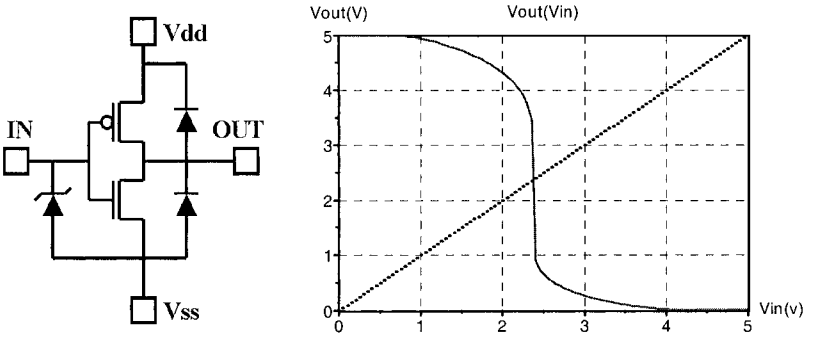


Figure 6-45. Simple stage inverter with ESD protections and its characteristic Vout(Vin).

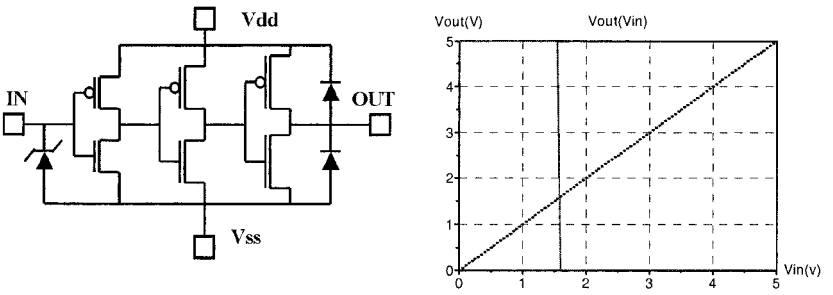


Figure 6-46. Three stages inverter and its Vout(Vin) behavior with SPICE.

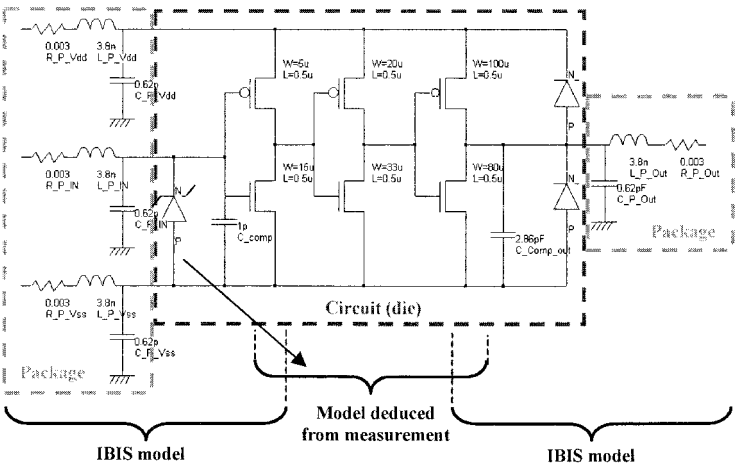


Figure 6-47. Parts and topology of the model.

But simulations of function Vout(Vin) on this simple stage inverter were very different from measurements done by an acquisition card on a PC: such output transistors are designed to supply a possible strong current, incompatible with time delay and voltage transfer performances. This is why they need a fast command on their grid, supplied by another inverter. Finally, to respect the global function of the circuit, a structure based on a three-stage inverter was necessary (Fig. 6-46). Transistor dimensions are obtained after several SPICE simulation in order to fit Vout(Vin) curves on those measured. Notice that the triggering point is not at $V_{dd}/2$.

Fig. 6-47 summarizes the previous elements about circuit modeling and shows the schematic diagram obtained by exploiting the IBIS file information and measurement results.

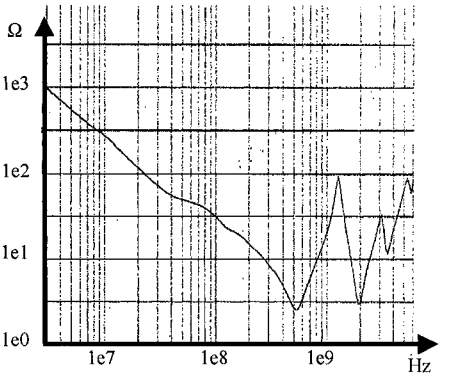


Figure 6-48. Impedance measurement between Vdd and Vss pins

But this model does not take into account any out-band behavior of the circuit and most of the aggressions seen by the circuit, conducted or radiated, have a spectrum outside its functional frequency band. It is therefore necessary to complete the model with passive elements that take into account the behavior of the component under high frequency threat.

These elements are deduced from impedance measurements done with a network analyzer in reflected mode (S11). This technique gives the impedance seen between a "hot" point and the ground, hence, V_{ss} in the case of our circuit. In impedance measurements, the reference plane used for calibration needs to be as close as possible to the circuit pin. Impedances were measured between V_{dd} and V_{ss} pins (Fig. 6-48), In and V_{ss} pins and then Out and V_{ss} pins (Levant, 2002).

In comparison with the previous diagram, several elements have been added which traduce passive effects of the circuit die. Metallic tracks inside the die are modeled by a simple inductance, L. In order to match special resonance, a few parts are modeled with an RLC circuit. Moreover, the influence of the capacitance between the die and the PCB ground is modeled by a RC circuit. Few resistors are needed to reduce resonances of passive circuits. To finalize the whole diagram and to match impedance measurement as well as possible, it was necessary to add few passive elements not linked to a physical construction inside the circuit. We finally obtained a complex model (Fig. 6-49) that suits in-band working and near out-band behavior of the circuit (Fig. 6-50).

After modeling the circuit under test, the second step is to describe the aggression test bench and then to model it. Before simulating circuit susceptibility, it was necessary to model the behavior of the whole bench.

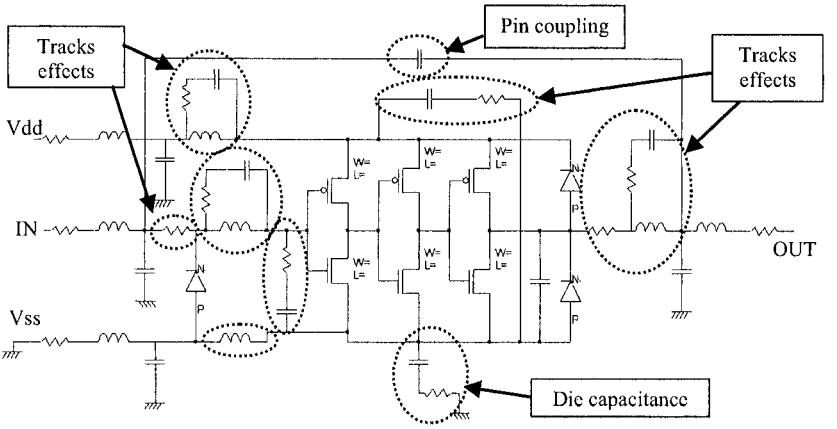


Figure 6-49. Equivalent model of TI inverter with parasitic effects.

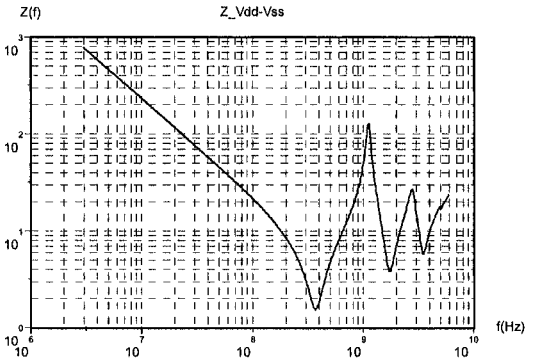


Figure 6-50. Simulation of impedance seen between V_{dd} and V_{ss} pins.

6.4 Aggressions test bench

6.4.1 Principles

The test bench (Fig. 6-51) is based on "classical" direct power injection. An amplified signal is conducted to circuit input pins across a small capacitor (IEC62132, 2001; Maurice, 1995).

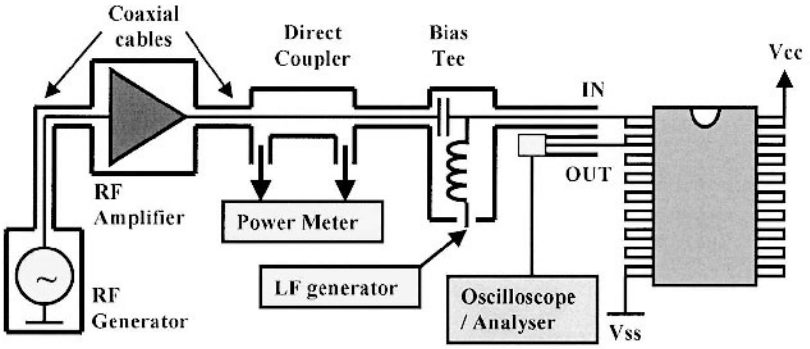


Figure 6-51. Description of the test bench.

The following list describes equipments used in this test bench:

- Rhode & Schwarz SML01 generator 9 kHz to 2.2 GHz.
- M2S amplifier, same frequency range, protected against high VSWR.
- Directional coupler with –20dB coupling factor.
- HP3150A bias tee 100 MHz-18 GHz.
- HP437B power meter with thermal probe.
- LeCroy 500 MHz digital oscilloscope.

Power signals delivered by the amplifier are directly injected into the component under test thanks to a bias tee, which is a capacitive device. This allows a nominal signal to be mixed with a threat signal on the circuit input. An oscilloscope connected to the inverter output is used to detect faults, using a time and voltage gauge, and to apply the desired susceptibility criteria. The dual directional coupler is used to measure the forwarded power delivered by the amplifier and the reflected power from the circuit because it behaves as a mismatched load and then reflects a part of the incident wave.

Differences between these two powers indicate the level of transmitted power that provokes faults on the circuit. It is easier to consider the transmitted power because it's independent of the test bench. All the followings results about susceptibility tests deal with this power.

In order to simulate this aggression test bench, we decided to simulate the whole test bench by completing the integrated circuit model. Hence, the first step was to create a model for each part of the test bench.

6.4.2 Modelling the elements of the test bench

In order to simulate circuit aggression, it is necessary to make a model of each element. Most of these models are directly deduced from a characterization or a measurement. We used SPICE and SABER models.

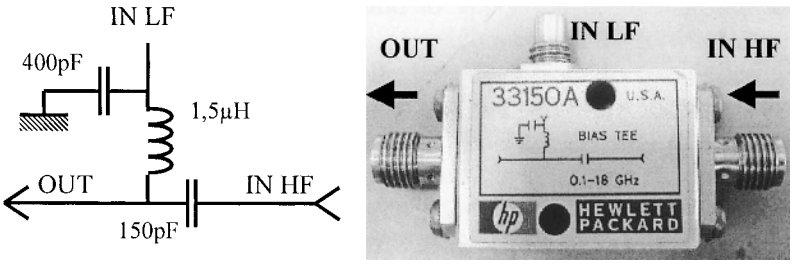


Figure 6-52. Bias tee diagram and photo.

Even if the aggression only reached 2 GHz, most of the models are true beyond 3 GHz, in accordance with the bandwidth of our network analyzer.

6.4.2.1 Cable + directive coupler

Cable and directional coupler are modeled by a lossless transmission line, TLINE (Z0=50 Ω et TD=4.2 ns) for SPICE. A vectorial network analyzer was used to characterize the length and delay of this line. Of course, the easiest way to measure the delay of a line is to use a Time Domain Reflectometer.

6.4.2.2 The bias tee

From S11 measurements taken with a vectorial network analyzer in different configurations (load, short circuit, open circuit), it is possible to deduce the values of the elements mentioned in the bias tee diagram. Hence, the following diagram (Fig. 6-52) is used to complete the bench model.

6.4.2.3 SMA connectors and PCB tracks

Each track and connector of the PCB are modeled by a simple RLC circuit because we use very short tracks in comparison with our bandwidth. This schema is directly deduced from measurements done with a vectorial network analyzer in reflected mode (S11). Measurements are taken in two steps: firstly, the track is connected to the ground, giving the global inductive behavior of the tested track, and secondly, the same track is measured opened, giving the capacitive behavior. In each case, the slope of impedance measurement gives the value of the main passive components, and the resonance frequency gives the values of the secondary components. Finally, we obtain the typical diagram shown in Fig. 6-53. Of course, these operations must be repeated for each track.

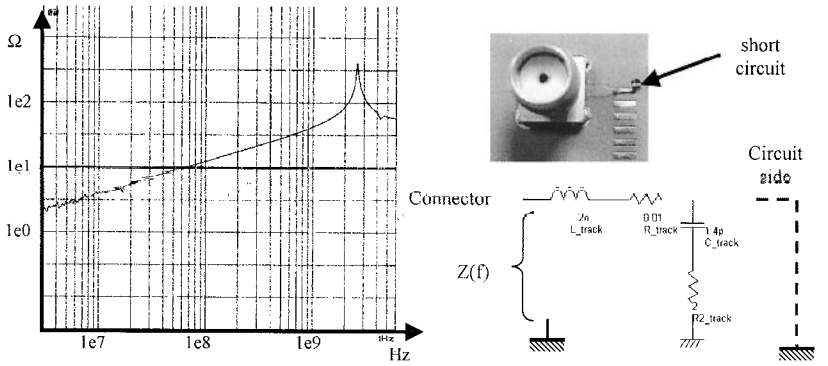


Figure 6-53. SMA and track measurement in short circuit. It can bee seen that the slope is typical of an inductive effect.

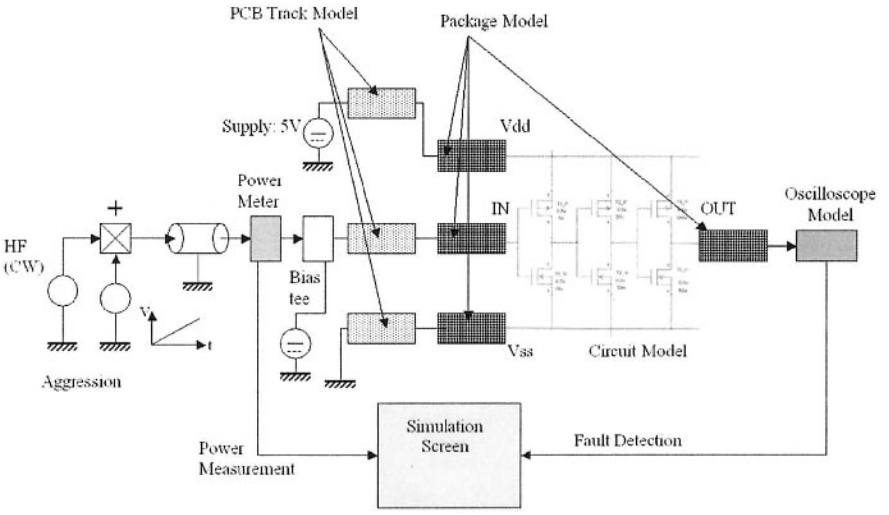


Figure 6-54. Synoptic of aggression bench model.

6.4.3 Model of the whole test bench

The whole model is obtained by combining all the previous models at (test bench and component). Fig. 6-54 gives a global view of the test bench model.

The oscilloscope model is reduced to a simple RC circuit, in accordance with the technical description of the probe. The power measurement is made with a particular function that is described in the following part. The simulation screen is used to determine faults due to the aggression. The following part describes conditions and criteria of the susceptibility test.

6.5 MEASUREMENTS

6.5.1 Susceptibility criteria and aggression

For the test, the aggression signal is a continuous wave from 400 MHz to 2 GHz. The frequency step is by 50 MHz up to 1 GHz and by 100 MHz beyond. The power of the signal is increased until a fault is detected; the power is then recorded. This procedure is repeated for each frequency point. Incident power is limited to 1 W to avoid circuit destruction. The aggression signal is only injected on circuit input.

For our experiment, two criteria were used. The first one was a voltage gauge around a constant voltage level (V_{dd} or V_{ss}) and was used to detect perturbations of the integrated circuit when a constant voltage on input was applied. The voltage variation accepted is more or less 20% of V_{dd} around the constant level. Over this limit, circuit function is considered as lost. The second criterion was based on a time and voltage gauge in order to measure perturbation of circuits when a clock signal is applied on input (Barber, 1994). Such a criterion is able to detect voltage faults and time faults (rise/fall time and extended time delay). The voltage limits are the same as for the first criteria. The delay limit is more or less 5% of the signal period around falling and rising edges.

It would of course have been possible to consider a lot of different criteria like the current consumption of the circuit under test, the spectrum shape of circuit output or the propagation time. It is very complicated to monitor several criteria in the same experiment. For us, the most significant criterion was voltage level, followed by time.

6.5.2 Behavior of the circuits under test

As expected, there are differences between circuits and those working with lower voltage are more sensitive to high frequency aggressions, as the noise margin is lower. Fig. 6-55, 6-56, & 6-57 illustrate this matter for several circuits tested in accordance with the first susceptibility criterion (constant voltage gauge). These circuits are in the same package but built in accordance with different technologies.

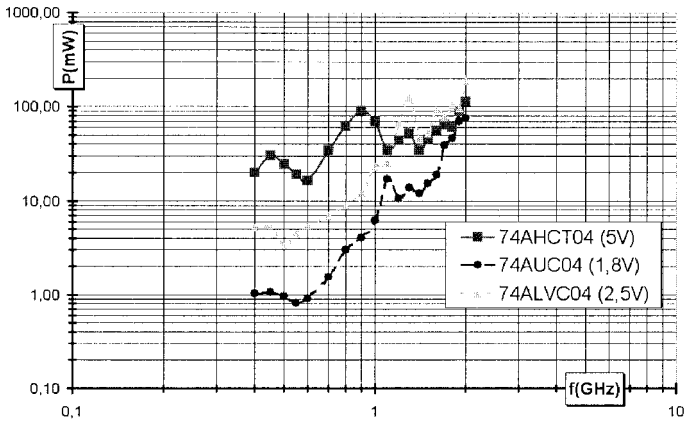


Figure 6-55. Susceptibility comparisons between technologies in SOIC package.

Surprisingly, it is more difficult to deduce influences due to packages on susceptibility for CMOS of integrated circuit. Passive effects of packages, which can be considered as a filter, are not so different, probably because all these packages are very small. Fig. 6-56 shows aggression experiments for different packages, in accordance with the constant voltage criterion.

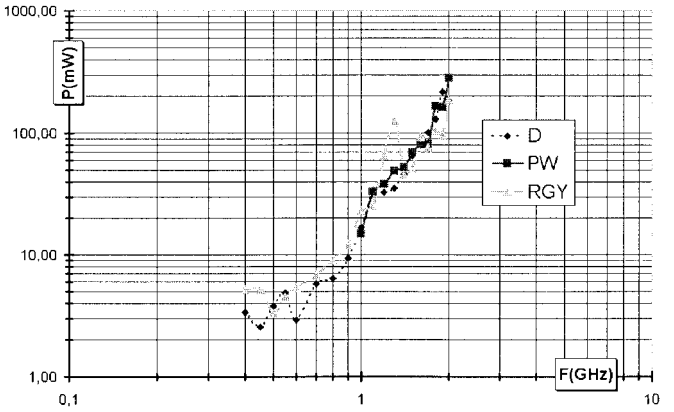


Figure 6-56. Influence of package on circuit susceptibility. SN74ALVC04 - 2.5 V.

A circuit is also more sensitive when the input signal is a clock rather than constant voltage level, as shown in Fig. 6-57. It is well-known that digital circuits are more sensitive on rise/fall edges than at a constant level.

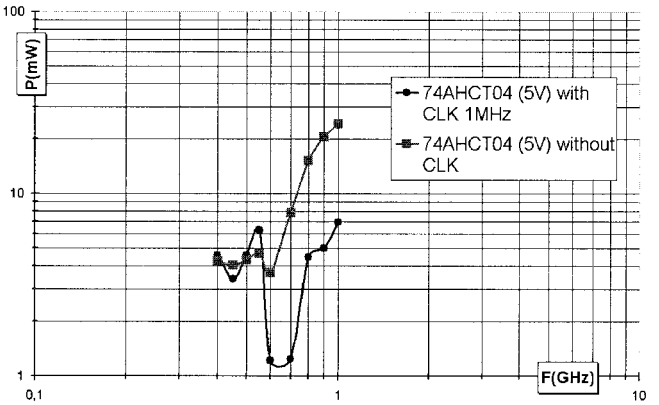


Figure 6-57. Input signal behavior on circuit susceptibility. SN74AUC04 – 1.8 V.

In fact, transistors cease to work normally under aggression, and it is easier to see this changing in dynamic mode. The following figures show susceptibility differences when the circuit works with a constant voltage or a clock in input. Of course, for this test, the second criterion, based on a voltage and time gauge, is applied.

6.5.3 Simulation of aggressions

Simulations of this model are computed with SABER in transient (time domain) to take into account the non-linearity of active components of the model. SABER is a mixed simulation program that allows circuit (SPICE) and behavioral models. Only two parts of our model were described in a behavioral model: power measurement and criterion application.

The aggression was modeled by a continuous sine wave mixed (multiplied) with a voltage ramp that simulated the power increase. During the same period, the voltage of the circuit output was monitored. Whenever this voltage did not respect the failure criteria decided on, the circuit was considered as disrupted. Of course, this criterion is exactly the same as the one used for the experiment. So, in principle, simulations of the fault detection were very close to those really measured.

One of the most difficult parts of the simulation was to establish a link between the voltage generator, as it exists in computation software, and the power supplier as used in measurement. The chosen solution was to create a special element under SABER that computed transmitted power to our circuit. A second behavioral model provided the fault detection.

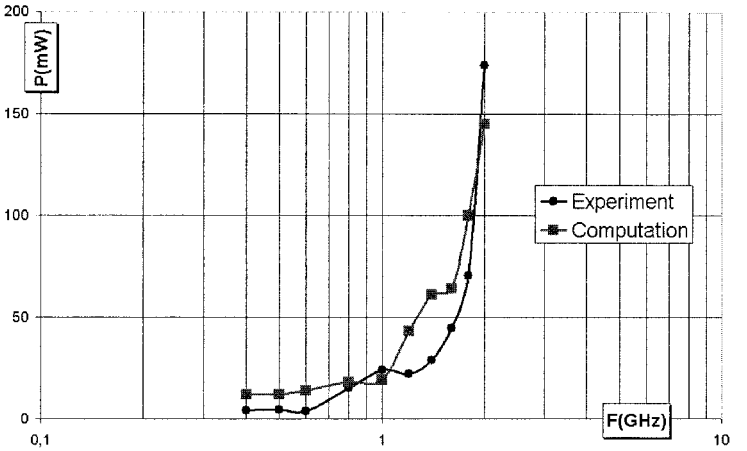


Figure 6-58. Comparison between measurements and computation.

It reproduced voltage gauge and monitored the voltage level based on the oscilloscope model, and then displayed the power needed to provoke a voltage exceeding the chosen gauge. Fig. 6-58 gives a comparison between curves of power obtained by simulations and measurement. These values match the power it is necessary to inject on input in order to provoke a fault in accordance with the first criteria. Even if there is a small difference between these two powers, the model can be considered as acceptable because it gives a good idea of the circuit susceptibility range. The global shape of the curve and amplitudes are respected.

6.6 Conclusions

These tests of injections accompanied by a global modeling are an important and necessary milestone in the understanding of the susceptibility of digital integrated circuits. The chosen approach, which consists in modeling each item at the circuit level, is interesting because it is very close to the physical reality of the component (substrate capacitor, inductive effects of metallic tracks, etc.) and shows that it is partially possible to simulate the aggression level needed in input to provoke a logic fault on circuit output.

But this approach possesses several limits: Each HF item must be characterized beforehand, the network of power supply must be perfectly modeled to take its passive effects into account, and the test methodology must be perfectly defined to make the experiments easily reproducible.

Circuit modeling is complex: a lot of measurements are necessary to obtain a complete model of the circuit. The relationship between voltage level, as in computation software, and power measurement, as in experiments, is not direct and requires conversions. It is difficult to adapt this measurement to all digital circuits and the direct injection technique is limited in frequency.

Beyond 4 GHz, the capacitive injection seems very difficult to operate in view of the reflections and unmatched elements. But it remains an interesting equipment test for specific investigations. It could be, for example, used in the case of particular susceptibilities on a frequency range, or in order to learn the global level of susceptibility of an I/O or a power supply. Such a measurement on all circuit pins is difficult or even impossible with complex digital circuits like microprocessors or FPGA.

To conclude, this series of experiments has allowed us to acquire a better knowledge about susceptibility phenomena and brings us a lot of information about digital circuit behavior under HF aggressions.

7. *FREESCALE* MICROCONTROLLER SUSCEPTIBILITY

7.1 Overview

The aim of this experiment was to improve our knowledge about the susceptibility of microcontrollers and to propose a methodology to predict this electromagnetic susceptibility. The MC9S12DP256 (MCS912DP25, 2002), or "Barracuda", is a 16-bit microcontroller designed in 2002 (Table 6-9) mainly intended for automotive applications.

Table 6-9. Identity card of Barracuda microcontroller.

Project name	BARRACUDA
Main partners	Freescale Toulouse & Munich
Design leader	Joachim Kruecken, Freescale, Munich
Web site	www.freescale.com
Technology	0.25 TSMC
Die size	2.25 mm^2
Packaging	112-pins TQFP
Complexity	16-bit CPU, 256k bytes flash EEPROM.
Circuit objective	Microcontroller susceptibility

7.2 Design constraints

To measure the microcontroller immunity, a specific test board was developed. This test board, realized on a FR4 substrate, initially had to answer as well to emission measurement constraints as well as to immunity measurement constraints.

As regards the emission issue, it offers the possibility of performing measurements on the power supply network and some input/output according to the conducted 1Ω method (IEC 61967, 2002). That is why, some connectors and their associated circuits are implemented. It is also possible to perform radiated emission measurement according to the TEM cell method (IEC 61967, 2002), or to aggress the integrated circuit in radiated mode using a GTEM cell.

We will now consider the immunity measurement constraints. The test bench that we will used is based on the DPI (Direct Power Injection) method (IEC 62132, 2001). Consequently, some precautions are necessary to drive the disruptive signal as close as possible to the device under test (DUT) while keeping the maximum of energy. In other words, it is necessary to limit the reflections of the aggression signal. For that purpose, we adapted to 50 Ω all tracks that must drive a disruptive signal. That impedance is equivalent to those of the amplifier and generator outputs. Furthermore, the SMB connector used is also 50 Ω adapted in order not to generate impedance rupture along the injection line. The coupling capacitors and the connectors are placed close to the DUT input, which minimizes the injection track length of the printed circuit. Finally, to isolate the disruptive line from the other signals as much as possible, the spacing between tracks was widened.

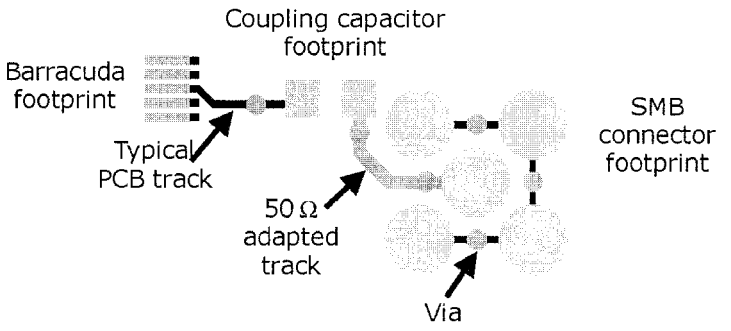


Figure 6-59. Typical routing of injection tracks.

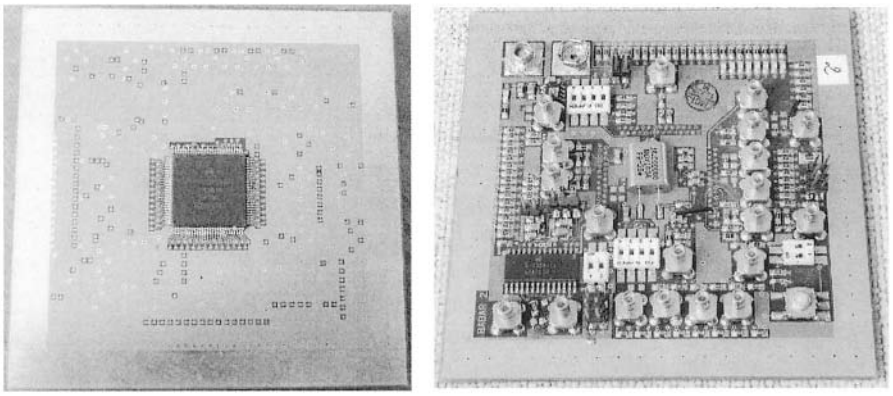


Figure 6-60. Test board for Barracuda ; component side (left), associated component's side (right).

Fig. 6-59 presents the typical routing used for the aggression tracks. Because of the incompatibility between width of the adapted tracks and distance between two microcontroller pins, the 50-Ω adaptation can only be realized between the connector center and the first coupling capacitor pin.

This is not very important because the first impedance break appears at coupling capacitor level. Finally, several via are present. Their utility is multiple: at electric level, they allow several layers to be connected together; at the mechanical level, mainly on metal plans, they provide a warning in the event of a possible unsticking during component assembling on the PCB (during its passage in an oven).

Finally, the last design constraint corresponds to the fact that the test board has to allow to test in a independently way as well the immunity of a CAN interface as the one of Barracuda. For that purpose, the power supply networks of both components were separated.

The test board is illustrated in Fig. 6-60. The microcontroller is mounted on one side (left), whereas all the associated components are implemented on the other side (right).

7.3 Setup to perform microcontroller immunity measurement

In the following paragraphs, we describe the electrical circuits which can measure the microcontroller immunity. We then detail the various electrical parts into which we inject the RF disturbances, that is to say the power supply network, and the external synchronization clock output (ECLK) and the analog-to-digital converter.

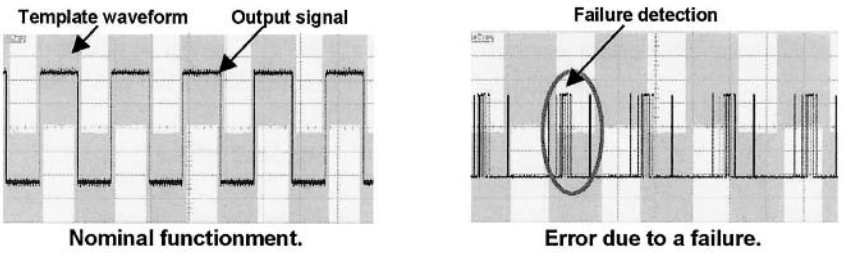


Figure 6-61. Nominal signal (left) and failure signal (right) during immunity measurement.

7.3.1 Test setup elements to monitor the state of the microcontroller

The microcontroller state monitoring circuit is essential in the immunity measurement because it allows detecting in real time the failures of the integrated circuit under test. Indeed, it is considered as our failure criterion during the immunity measurement.

The microcontroller state monitoring circuit is based around the general purpose port B of Barracuda. This digital port is programmed as an output port and is connected to 8 luminescent electrical diodes (LED). Moreover, the output number 5 presents the particularity to be connected with a SMB connector, so in that case, it can be easily monitored through an oscilloscope input for real time failure detection. Fig. 6-61 present two output signal examples: the signal on the left part corresponds to a nominal signal (without failure), whereas the signal on the right part shows the detection of a failure. As a remark, that kind of probe present another advantage, because it can be integrated in an automatic immunity test bench.

The functioning of this microcontroller state monitoring circuit is similar to a conventional external watchdog: periodically the output number 5 switches generate a square wave with a 50% duty cycle. If the square wave signal keeps this waveform, this means that the microcontroller activity is in close good agreement with the execution behavior. In the other case, a software or hardware failure has appeared.

In an embedded application, this signal has no meaning, but for our case study it is highly important because it allows measurements to be to simplified and automated.

Finally, the 7 other LEDs implemented on the test board can give additional information in some particular measurement cases. The content of the information can be various and very specific: it can indicate which part of the microcontroller failed, in the case of a test on an analog signal it can show the effects on this signal (overshoot, undershoot).

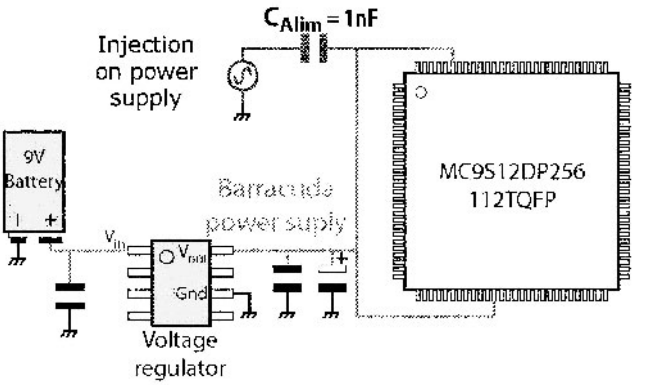


Figure 6-62. Electrical diagram for performing immunity measurements on the power supply network of Barracuda.

7.3.2 RF disturbances injected into the power supply

The BARRACUDA microcontroller uses several power supply networks: one for the CPU (Central Processing Unit), and one for the other electrical blocks. The decoupling capacitances are all 100 nF and implemented as close as possible to the microcontroller power supply pins.

We can now describe how to perform an immunity measurement by injecting an RF disturbance into the power supply network. Fig. 6-61 illustrates the electrical circuit. The principle described below only considers the V_{dd1} and V_{ss1} (core supply), but in a similar way, it is possible to inject the RF disturbance into every power supply path.

To propagate the RF disturbance over the whole network, the RF disturbance is injected after the voltage regulator output and as close as possible to the DUT through the coupling capacitance C_{Alim}. The principal inconvenience in this procedure comes because we cannot distinguish a failure due to the voltage regulator and from due to the microcontroller.

On the other hand, it presents the advantage of not focusing only on any specific power supply pin, and thus to be general aggression enough. Furthermore, the RF disturbance is injected before the coupling capacitances as could be it an aggression which would couple in the tracks of the printed circuit in the natural environment of the system.

In order to characterize this radio frequency injection probe, we measured its transfer function using a network analyzer. The transfer function of the coupling path is representative of the effective injected power. The elements implemented during the measurement are described on the left part of Fig. 6-63.

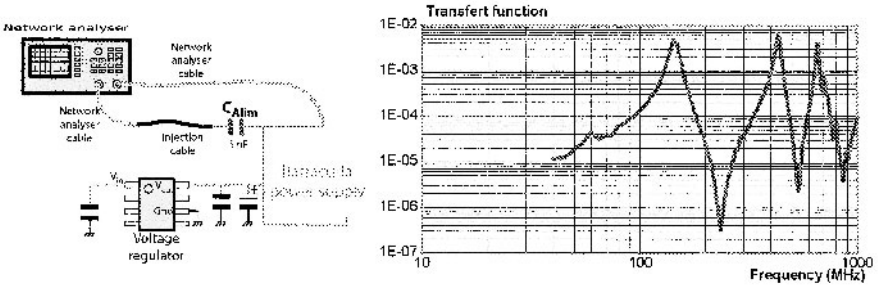


Figure 6-63. Setup (left) and transfer function (right) of the injection probe used to aggress the power supply of Barracuda.

We find that all the components are used during the immunity measurement except the microcontroller under test which is not mounted on the test board. This measurement is made in the 40 MHz - 1 GHz bandwidth.

The results obtained are presented on the right part of the Fig. 6-63. The observed behavior is similar to a transmission line: the injected power rate varies strongly between 6.10^{-3} and 3.10^{-7}, according to the resonance (150, 430 and 660 MHz) and anti-resonance (240, 540 and 860 MHz). Besides, on the whole frequency domain, the coupling of the RF disturbance on the circuit is weak.

The immunity measurements were performed according to the direct power injection method. So each point corresponds to the level needed to detect a microcontroller failure at a determined frequency. The maximum injected power level was initially fixed at 25 dBm (about 300 mW). This fixed upper limit was chosen in order not to have physical consequences on the microcontroller: destruction of some physical elements or blocks of the microcontroller.

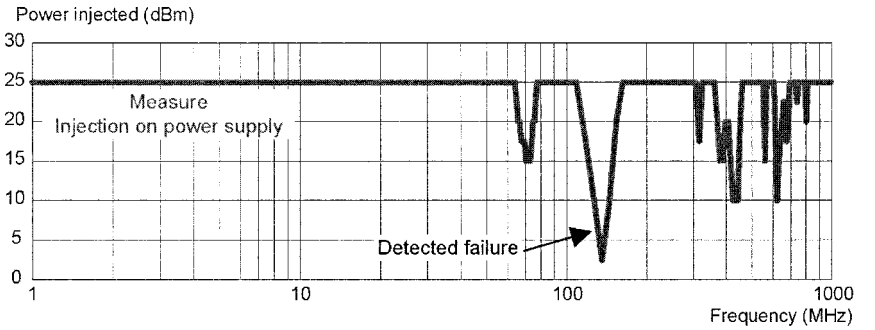


Figure 6-64. Immunity measurement results.

The results of the immunity measurement are presented in Fig. 6-64. At low frequency (below 60 MHz), no failure was detected. The most sensitive frequency was located at about 130 MHz, where only a few milliwatts are sufficient to generate a failure. As a remark, we do not know if this failure is due to the microcontroller under test or due to the voltage regulator.

7.3.3 RF disturbances injected on the external synchronization clock output

The clock network of the microcontroller can be considered as a vital organ. In the case of Barracuda, the only way to reach this network is to inject the disturbance on the ECLK pin. Indeed, in some operational modes, this pin can transmit the signal of internal clock to external components (external memory for example). After a reset, the ECLK pin of Barracuda is inhibited, for consumption and parasitic emission reasons. It is therefore necessary to activate it by programming an internal register dedicated to the clock functions. In this configuration, the output pin is no longer in high impedance mode and as a consequence an electromagnetic aggression can disturb the internal clock.

The disturbance is injected through a coupling capacitor. A major difference appears with the presence of a resistance to ground. Indeed, the ECLK pin is a part of the general purpose input/output port named port E. Consequently, when the function of clock synchronization is not configured, it is necessary to add a 10 kΩ load resistance as for the other pin on this port.

This RF injection probe was also characterized by means of a network analyzer according to the electrical diagram presented in the Fig. 6-65 (left). Here again, we find all the components used during the immunity measurement except the microcontroller under test which is not mounted on the test board.

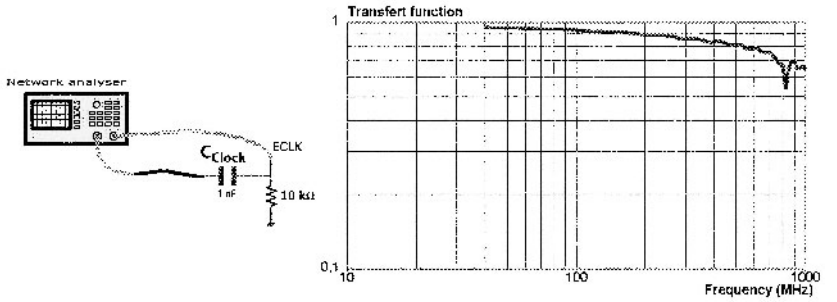


Figure 6-65. Setup (left) and transfer function (right) of the injection probe for an injection on the clock network

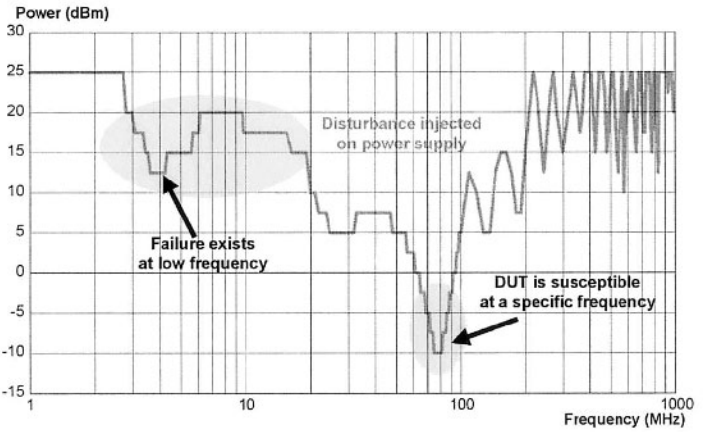


Figure 6-66. Immunity measurement results.

The transfer function obtained in the 40 MHz - 1 GHz bandwidth is presented in Fig. 6-65 (right). For frequencies lower than 600 MHz, we obtained a very interesting characteristic. Indeed more than 80 % of the total power can be injected into the circuit under test. Consequently, the coupling of the injected disturbance through this probe is particularly effective. This is largely due to the simplicity of the implemented elements and to the presence of the 10 kΩ resistance.

Here again, the immunity measurements were performed according to the DPI method. The maximum injected power level was initially fixed at 25 dBm. The failure criteria for this test and for the RF injection into the power supply network were the same.

The results of the immunity measurement are presented in Fig. 6-665. In comparison with the obtained immunity graph for an RF injection into the power supply, the immunity graph is rather different and the levels needed to disturb the component under test are lower. For example, it only requires a few hundred microwatts to generate failure if we consider the 80 MHz frequency.

7.3.4 RF disturbances injected into an analog-to-digital converter

The last microcontroller block that we tested during an immunity measurement is one of the two analog-to-digital converter (ATD). In that case, the test method was slightly different: analog devices are very often more susceptible than digital devices. So the injection power needed to generate failure can be lower, and the power amplifier is not always required.

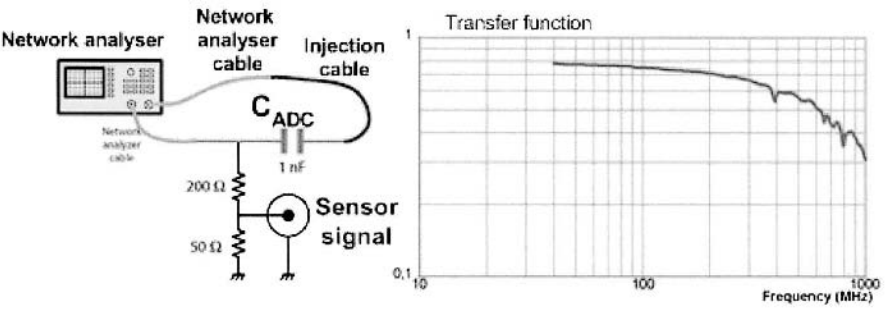


Figure 6-67. Components (left) and transfer function (right) of the injection probe for an injection into the integrated analog to digital converter of Barracuda.

Moreover, the question of the failure criterion is more difficult, because we must define margins within the analog-to-digital converter is in a good working order. And those margins must be in coherent with the allowed fluctuations of the analog signal that will be sampled.

So to test the immunity of the integrated ATD integrated on Barracuda, we defined an RF disturbance that coupled to the ADC through an injection probe. This probe was characterized by means of a network analyzer according to the electrical diagram presented on Fig. 6-67 (left). The transfer function obtained in the 40 MHz - 1 GHz bandwidth is shown in Fig. 6-67 (right). For the frequencies lower than 200 MHz, we obtained an interesting characteristic. Indeed more than 70 % of the total power can be injected to the circuit under test. Consequently, the coupling of the injected disturbance through this probe is particularly effective.

Here again, the immunity measurements were performed according to the DPI method. The maximum injected power level was initially fixed at 10 dBm because of the analog nature of the sensor signal.

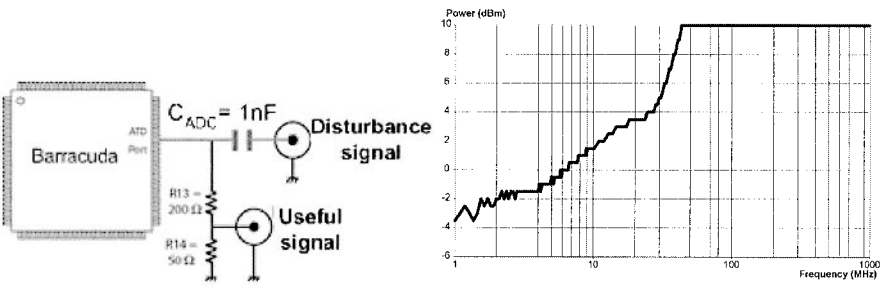


Figure 6-68. Immunity measurement results.

The results of the immunity measurement are presented in Fig. 6-68 (right). These results are in close agreement with our expectations (FIORI, 2000), and demonstrate the low-pass character of that kind of component. Indeed, above 25 MHz, a 30 dBm/decade attenuation is effective. Moreover, those results confirm that analog devices are particularly susceptible because only a few hundred microwatts are needed to generate a failure.

7.4 Conclusion

In this section, we have illustrated how to setup and to perform an immunity test for complex integrated components such as microcontrollers. These measurements have been realized with harmonic signals according to the DPI method.

8. PHILIPS IMMUNITY CASE-STUDY

8.1 Overview

The circuit described in this case study concerns TV signal processing. An intermediate-frequency (IF) input stage was provided with an IF-modulated signal from the tuner and several internal circuits delivered the relevant signals for controlling the horizontal and vertical deflection and several other TV signals. When running radiated RF-immunity tests according to EN55020 the circuit was disturbed such that the picture quality was affected. Cable looms attached via PCB tracks to the IC-pins were responsible for receiving the RF-disturbing field and introduced this disturbance signal to the integrated circuit.

The TV processor is divided in several sub-blocks such as current mirrors, differential amplifiers, multipliers, D/A-converters, voltage to current converters, reference sources, etc. In this case, only the last block in the signal chain is accessible via its output pins. If an LF-interference is generated somewhere in this signal chain, it will be difficult to determine from the output measurement results where the cause is located. Possibilities to measure these effects on-chip are lacking. As a consequence a thorough understanding of the non-linear effects of several kinds of analog circuits and how these effects propagate through the whole chain are required. Besides that, it has been proven that the RF-disturbance penetrates the IC via other pins than those belonging to the geometry-processing block. From this, the interfered sub-circuit cannot be so easily assigned as suspected.

Immunity tests specify that RF-signals modulated by low-frequency amplitude should be applied. Investigations of the frequency spectrum at the output pins show that the interference does not only contain the demodulated LF-frequency but also several other frequencies. Moreover, some frequencies are present as differential-mode (DM) interference, others as common-mode (CM) interference. By considering these interference modes, the occurring frequencies and the influence of several settings (e.g. amplitude, waveform correction) it should be possible to pinpoint a susceptible sub-circuit or the possible transistor that is affected within a huge amount of transistors belonging to the entire analog processing block.

8.2 Low frequency investigations

Suppose the geometry-processing block is exposed to an RF-disturbance that is amplitude-modulated with a 987.5 Hz (frequency choice will be elucidated later) sine wave. The undisturbed 50 Hz (common frame frequency for European TV-systems) saw tooth waveform will contain a DC-part and an AC part with frequency components at each multiple of 50 Hz.

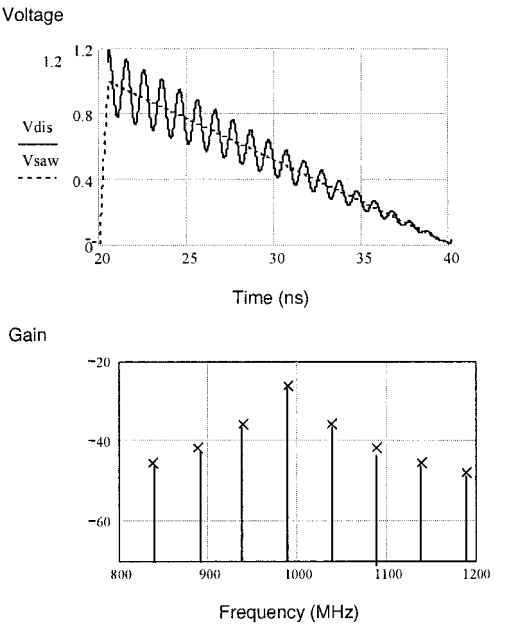


Figure 6-69. LF-disturbance and a part of the resulting LF-spectrum of the output voltage with a saw tooth input voltage and a LF-disturbance at the bias current.

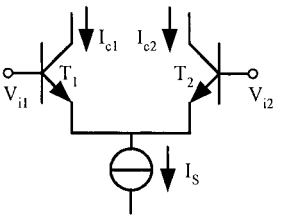


Figure 6-70. Differential pair and associated currents.

Due to non-linear properties of the bipolar and MOS-transistors, a DC-shift and additional LF-components may occur, depending on the kind of circuit and where the disturbance is affecting it.

The demodulation by non-linearity may be explained by the superposition of the sinusoidal LF disturbance $V_{dis}(t)$ at 987.,5 Hz on the saw tooth signal $V_{saw}(t)$ (Eq. (6-3)) resulting in: $V_{saw}(t) + V_{dis}(t)$. As a result, in the frequency domain an additional 987.5 Hz component will appear. In the event of superposition at one input of a differential amplifier only, the differential mode output disturbance voltage will be large and if submitted to both inputs the output level will be low and will depend on the common-mode rejection ratio (CMRR). The common mode output level may depend for instance on the emitter bias source impedance. Multiplication of the LF-disturbance signal with the sawtooth signal according $V_{saw}(t) \cdot (1 + f_{dis}(t))$ while:

$$V_{saw}(t) = a_0 + \sum_{n=1}^{\infty} a_n \cdot \sin(2\pi \cdot n \cdot 50 \cdot t) \tag{6-3}$$

with n = 1, 2, ..
and

$$f_{dis}(t) = A \cdot \sin(2\pi \cdot 987.5 \cdot t) \tag{6-4}$$

Close to 1 kHz additional frequency components will appear at 987.5 Hz and 987.5 Hz +/- n · 50 Hz according to the equations. In Fig. 6-69 a part of the saw tooth spectrum (represented by V_{saw}) and the additional disturbance frequencies (represented by V_{dis}) at one transistor collector output is depicted.

This multiplication effect can appear in the collector current I_{C1} and I_{C2} if the bias current I_S (see Fig. 6-70) is modulated with this LF-disturbance $f_{dis}(t)$ from Eq. (6-4) accordingly when:

$$I_{C1} \approx \tfrac{1}{2} I_S[1 + f_{dis}(t)] \cdot [1 + \frac{(V_{i1} - V_{i2})}{2V_T}] \tag{6-5}$$

In case of an analog multiplier an LF-disturbance term fdis(t) in the denominator may appear according to: Isaw(t) / (1 + fdis(t)), Fig. 6-71. If we assume IA represents a saw-tooth current and IB represents a multiplication factor, then the output currents are:

$$I_{o1} = I_B - (i_a \cdot i_b)/I_A \tag{6-6}$$

$$I_{o2} = I_B + (i_a \cdot i_b)/I_A \tag{6-7}$$

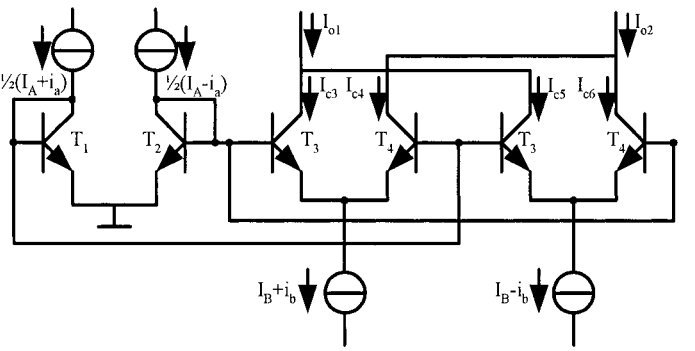


Figure 6-71. Four-quadrant analog multiplier.

If an LF-disturbance signal $f_{dis}(t)$ affects I_B as indicated in Eq. (6-4) and (6-5) then:

$$I_B(t) = I_S \cdot (1 + A \cdot \sin(2\pi \cdot 987.5 \cdot t)) \tag{6-8}$$

This will not affect the DM output current because I_B is cancelled out from the DM output current:

$$I_{o2} - I_{o1} = 2 \cdot (i_a \cdot i_b)/I_A \tag{6-9}$$

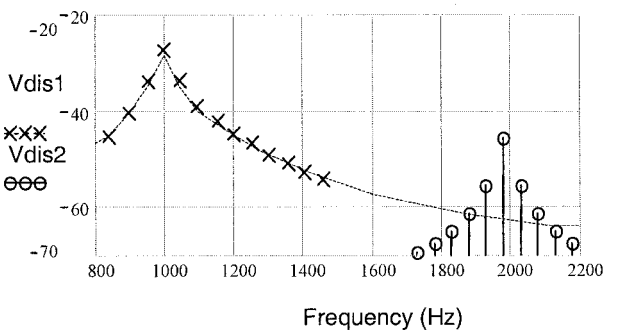


Figure 6-72. Output frequency components due to a LF-disturbance in the diode bias current of a four quadrant analog multiplier with additional frequency component vdis2 around 1975 Hz.

Regarding the single-ended output current the disturbance in I_B will only appear as one frequency component at 987.5 Hz according to Eq. (6-5) and (6-6). This is all in contrast with the differential amplifier. Furthermore if I_B is affected, the disturbance at one output will disappear when I_A is reduced to zero which makes this multiplier different from a differential amplifier.

LF-disturbance in I_A according to Eq. (6-8) will cause the same frequency components in I_{o1} and I_{o2} as in the case of a differential amplifier that is 987.5 Hz (except for DM) and 987.5 Hz +/- n · 50 Hz. But an LF-disturbance term in the denominator frequency components may arise at 2 · 987.5 = 1975 Hz and 1975 +/- n · 50 Hz. To be able to distinguish the LF-disturbance components at 2 kHz from the saw-tooth harmonics the fundamental of the disturbance is chosen at 987.5 Hz. In Fig. 6-71 the dotted line V_{dis1} represents the output voltage containing the 987,5 Hz and 987,5 +/- n · 50 Hz components while V_{dis2} represents the additional 1975 Hz and 1975 +/- n · 50 Hz components. In the event that I_A does not contain a DC-part ($\overline{i_a} = 0$) then 987.5 Hz and 1975 Hz will not appear. The presence of the LF-disturbance around 1975 Hz will show the special properties of this circuit.

These are a few examples of how LF-interference can be investigated and which kind of circuit may be responsible for the generated LF-interference response. As such the frequency spectrum may be helpful in selecting suspected circuits suffering from the RF-disturbance. By changing the amplification or bias setting of certain stages, additional insight can be achieved as to where in the entire chain of circuits the RF-disturbance is causing LF-interference.

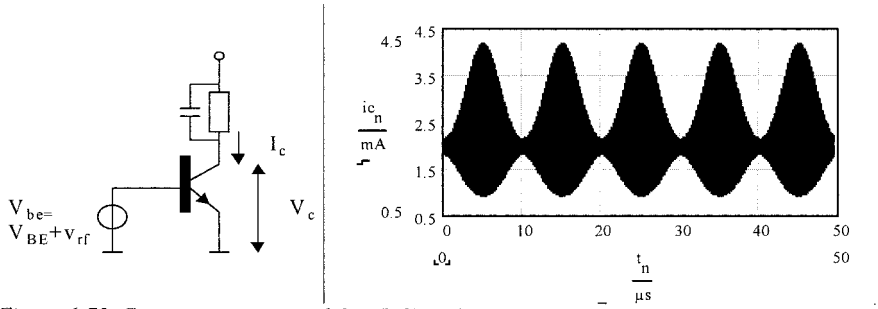


Figure 6-73. Common emitter amplifier (left) and representation of the collector current Ic as a result of an RF-input signal (right)

8.3 Non-linear behavior of analog circuits on RF-signals.

Distortion may be caused by the non-linear properties of transistors. Additional signal components with deviating frequencies will be generated. Consider a bipolar common emitter amplifier containing an RC network as a low-pass filter (see Fig. 6-73). Higher harmonics of the signal applied to the base will occur in the collector current due to the exponential relation between the base-emitter voltage V_{be} and collector current I_c according to:

$$I_c(t) = I_0 \cdot \exp\left(\frac{v_{be}(t) + V_{BE}}{V_T}\right) \qquad (6\text{-}10)$$

For RF-immunity testing amplitude-modulated RF-signals are applied and as such a fraction may be superimposed on the V_{be} voltage.

Let us assume that a 100 MHz (f_c) carrier is amplitude-modulated with f_m = 100 kHz. On top of the bias voltage V_{BE} an RF-voltage is applied.

$$v_{be}(t) = A \cdot [1 - m \cdot \cos(2\pi \cdot f_m \cdot t)] \cdot [\sin(2\pi \cdot f_c \cdot t)] \qquad (6\text{-}11)$$

With A = 11 mV, V_{BE} = 650mV, $I_0 = 10^{-14}$ and m = 80 % and after substituting (9) in (8) the frequency spectrum as partly represented in Fig. 6-74 for the collector voltage is generated. In addition to the 100 kHz AM-modulating frequency higher harmonics of this 100 kHz were also generated. A component is generated at $2f_m$ (= 200 kHz) with a 4/m = 5 times (14 dB) less amplitude than at f_m while m = 80%. The same decrease of 14 dB would be achieved for higher harmonics.

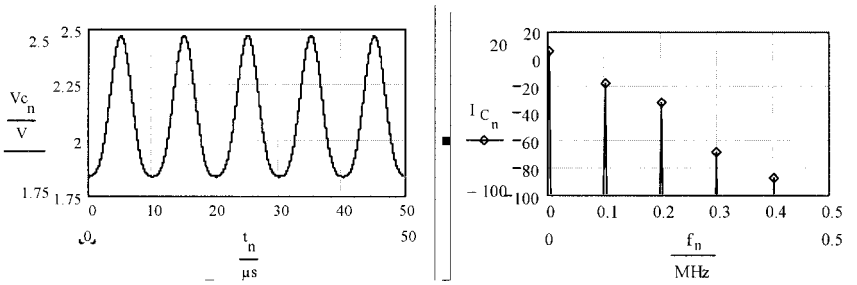


Figure 6-74. Collector voltage Vc (left) and LF-frequency spectrum current Ic in dBmA (right).

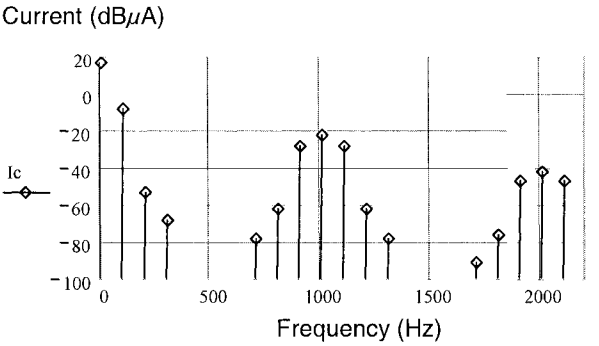


Figure 6-75. Simulation results for the collector current Ic of an analog multiplier with a 100 Hz input signal and affected by a 1 kHz bias current disturbance.

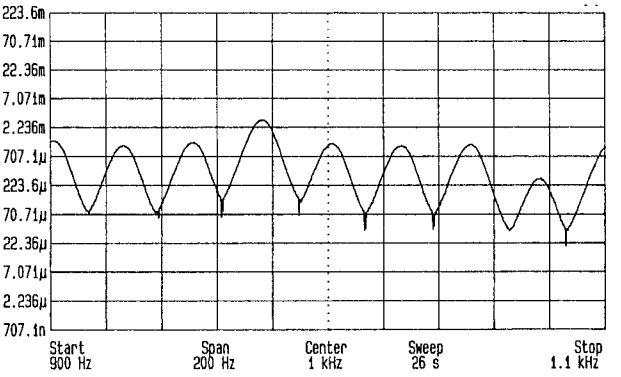


Figure 6-76. Measured LF interference by AM modulated RF-disturbance occurring in the one-chip TV signal processing IC.

Only the main properties of bipolar transistors that will arise as non-linear behavior are mentioned in this chapter in order to be able to distinguish the relevant kind of analog circuits. The behavior of MOS-transistors is quite different from that of bipolar transistors, and the modeling of the non-linear effects is very difficult.

8.4 Simulation and measurement results

An RF-disturbance may cause an LF-interference in a current mirror due to the non-linear effects of the transistors and diodes. If this current I_A disturbed according to Eq. (6-8), is applied to the diodes of the analog multiplier as represented in Fig. 6-70 an interference term may occur in the denominator of Eq. (6-9).

To investigate the consequences of this LF-interference, a discrete analog multiplier is built and disturbed by a 100 Hz sine wave combined with a 1 kHz sine wave. The resulting collector current I_C is represented in Fig. 6-75. The 100 Hz sine wave suffers from distortion so some higher harmonics also appear near 1 kHz +/- 100 Hz and 2 kHz +/- 100 Hz.

Fig. 6-75 shows the LF-interference measurement results concerning the one-chip TV processing IC. The LF amplitude modulation frequency was set to 975 Hz so that it could be distinguished between the 50 Hz saw-tooth harmonics. With the center frequency at 1 kHz and a 200 Hz span the 975 Hz and 975 +/- n·50 Hz components are clearly noticeable.

8.5 Conclusion

By using this method, the consequences of non-linear effects of analog integrated circuits for RF-disturbance can be elucidated. RF-disturbances do not only cause a DC-shift. In the presence of the relevant signal such as the saw tooth signal of a TV-processing integrated circuit certain LF-disturbance signals can be generated. Investigation of this LF-disturbance in the frequency domain may help to detect the RF-susceptible sub-circuit situated in an extensive analog integrated application. Investigation of the CM, single-ended and DM-signals and variation of available settings are useful for determining the location of the disturbance.

By applying a two-tone instead of amplitude-modulated RF-signal for immunity testing the output's signal frequency spectrum can be used for analysis. Depending on the signal components appearing in the frequency domain at the output it is still possible to determine which kind of sub-circuit has been affected. In this case study, only bipolar transistors were considered, but the method is also suited for analog MOS-transistor circuits.

9. APPLICATION OF LECCS MODEL TO AN ELECTRONIC CONTROL UNIT DESIGN FLOW

9.1 Overview

Applications of EMC simulation using the LECCS model are described. Our investigations have been done assuming application of th LECCS model in the design flow used by product designers. This chapter describes case studies of such use. The following were considered to be the cases in which designers would want to do simulations:

1. When a designer wants to investigate how to set new EMC design rules in the pre-design stage.
2. When a designer wants to confirm whether product design results satisfy the EMC test requirements.
3. When the product does not satisfy the EMC requirements and the designer wants to know how to redesign against the cause of this failure.

For application in cases (2) and (3), designers need a quick simulation that can be completed in a short time. Moreover, when the analysis results are problematic, information is necessary that can be used to investigate measures for redesigning. A simple pass/fail result is insufficient in these analyses. Case (1) has more latitude in terms of time than cases (2) and (3), but in analyses conducted by designers rather than researchers there are clearly stricter time limitations. This section describes methods of analysis using LECCS models that can meet these demands.

The background for the examples in this section is as follows. The electronic products evaluated here are ECUs (electronic control units) for automobiles. Compared with other electronic products, those used in automobiles are placed in an environment in which ECUs that emit noise are located near to those that must not malfunction even if subjected to noise, making it likely that EMC problems will occur. The arrangement becomes even denser with increased use of electronics in automobiles, so there is also a trend for increasingly strict regulation values. Because the cost of ECUs is also decreasing, the printed circuit boards used generally have fewer layers than regular consumer products; in most cases, they are single-sided and double-sided boards. The number of noise suppression components that can be used is also limited. Moreover, in recent years there is a trend for shorter product development times.

Ensuring the EMC performance of ECUs has a great impact on product development. Automobile ECUs have become more computerized, and are rapidly adopting communications functions and becoming high-level, complex electronic systems.

The semiconductors (IC/LSI) supporting these systems must also increasingly have high performances, and are being used in increasing numbers. EMC problems on ECUs are affected more and more by the EMC performance of these semiconductors. Key design tasks in the design of ECU are the selection of semiconductors with low noise and high immunity, and investigation of layout design of semiconductors on printed circuit boards to assure EMC performance of ECUs.

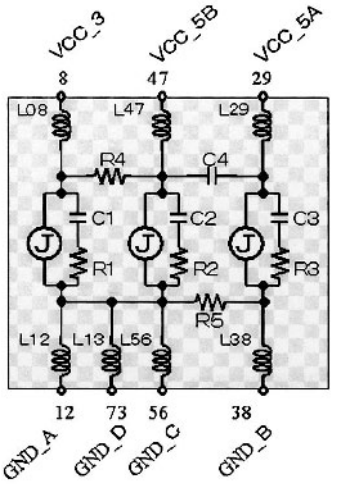
To ensure EMC quality, ECU designers should evaluate the board design at an early stage of product design to check the usage and layout design of semiconductors and additional components on printed circuit boards, which are a source of noise and cause of malfunction in ECUs. In the case that a noise problem does occur, it is necessary to investigate causes and implement countermeasures and also set a design rule for the subsequent product design. Such investigations in the early design stages can reduce EMC trouble on test stages, shorten time to market, and reduce costs. In the following paragraphs, examples of design using simulation to support ECU design are introduced.

9.2 Analysis of LSI peripheral circuitry levels

LSIs have many power-supply and GND terminals, and the power-supply terminals are usually categorized for some internal blocks of the LSI such as logic cores and analog blocks. With different uses, the amount of emission noise from terminals also differs. The power line layout between LSI and power-supply terminals of ECUs needs to be considered in circuit board design (Ichikawa, 2004a). For effective pre-assessment in actual board design, a design plan for the LSI periphery that adequately reflects the LSI characteristics should be prepared at the evaluation board level. For this an LSI model that reflects the noise characteristics of the power-supply and GND terminals is needed.

In the following analysis the LECCS model shown in Fig. 6-77 is used unless noted otherwise. The device under test (DUT) is H8S2134 (Renesas Technology Corporation), a 16-bit microcontroller.

When mounting an LSI on a board, the amount of noise propagation from an LSI to the circuit board is found to differ depending on several factors of the LSI.



Capacitance/ Resistance	C1=6.03[nF] C2=3.93[nF] C3=0.10[nF] C4=0.10[nF]	R1=2.34 [Ω] R2=2.51 [Ω] R3=8.58 [Ω] R4=168[Ω] R5=24.57 [Ω]
Inductance		L12=5.46 [nF]
Self	L08=5.46 [nF] L47=6.05 [nF] L29=6.58 [nF]	L56=6.05 [nF] L38=6.58 [nF] L13=6.03 [nF]
Mutual	K47_56 9.29e-02 K47_29 2.69e-02 K47_38 9.29e-02 K47_12 -1.84e-02 K47_08 -2.03e-02 K47_73 -5.90e-03 K56_29 -5.13e-03 K56_38 2.78e-02 K56_12 -1.92e-02 K56_08 -1.68e-02	K56_73 2.82e-02 K29_38 9.44e-02 K29_12 3.51e-02 K29_08 1.96e-02 K29_73 -1.99e-02 K38_12 -1.62e-03 K38_08 -8.37e-03 K38_73 -1.92e-02 K12_08 1.97e-01 K12_73 2.45e-02 K08_73 4.01e-02

Figure 6-77. LECCS model of a microcontroller

For example, noise propagation is affected by the following:

- Assignment of power-supply and GND terminals of an LSU
- Location of input/output terminals of the oscillation circuit in the LSI and its relevant GND terminal.

There are cases in which even if no large difference is seen in LSI evaluation boards, there exists a large difference in products that must be designed under various constraints. Several examples are shown herein.

First, the analysis results are shown for an LSI evaluation board in terms of decoupling capacitor arrangement. A board used for verification is shown in Fig. 6-78.

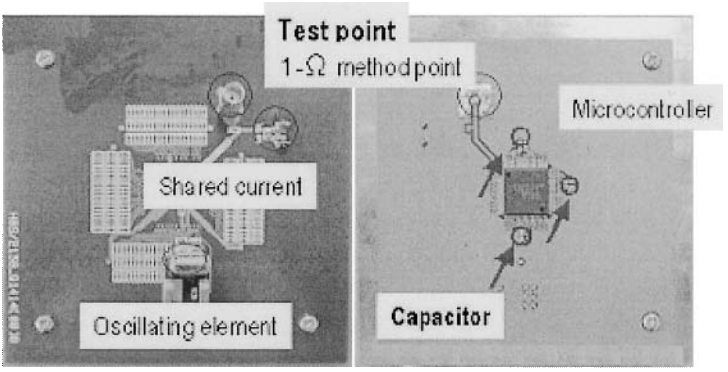


Figure 6-78. LSI evaluation board.

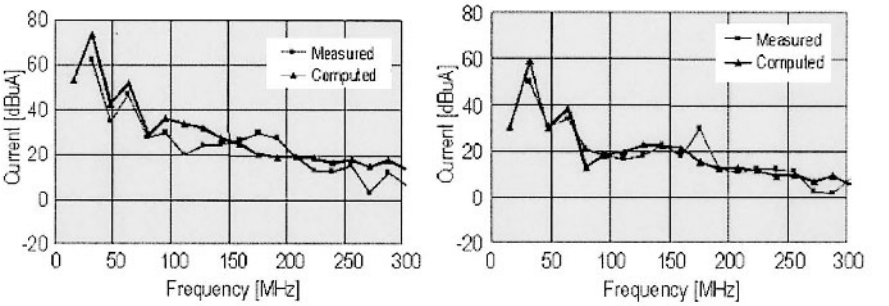


Figure 6-79. Noise current spectrum without capacitor (left), with capacitor (right).

It is a 4-layer board of 100mm x 100mm designed for noise evaluation based on the 1-ohm method, i.e. (IEC 61967, 2002). Analysis was performed combining the LECCS model with the equivalent circuit model of the evaluation board expressed by the PEEC method (Fukumoto H., 1995). The analysis results without capacitors are shown in Fig. 6-79 (left), and those with three decoupling capacitors are shown in Fig. 6-79 (right). These results demonstrate that an adequate evaluation is possible at the level of a single LSI evaluation board.

9.3 Analysis at the product board level

The effectiveness of simulation at the product scale level has been confirmed (Mabuchi, 2005). The product evaluated here is an ECU with a 2-layer board 92 mm x 110 mm in size. The power-supply terminal of this product was connected with an LISN (line impedance stabilization network), and an analysis was conducted with 2 different capacitor arrangements. The evaluation system is shown in Fig. 6-80. The measured and simulated results for capacitor arrangement A are shown in Fig. 6-81 (left), and those for capacitor arrangement B are shown in Fig. 6-81 (right). In both conditions the capacitors are located near the LSI power-supply terminals. It is seen that even a slight difference in capacitor arrangement has a large effect, in this case 20 dB, on the results. Thus, it was found that even at the product level sufficient analysis accuracy can be assured.

A microcontroller with an internal regulator in the LSI has a noise control terminal called "C" or "REGC", which requires an externally connected capacitor. The terminal is a power terminal that does not require an external supply, but generates a large amount of noise because it is connected to a core logic circuit.

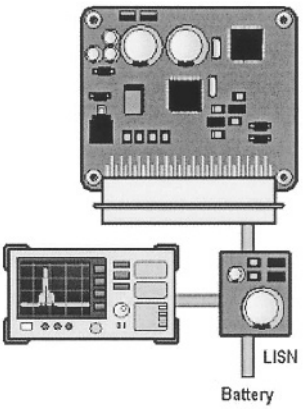


Figure 6-80. Measurement system.

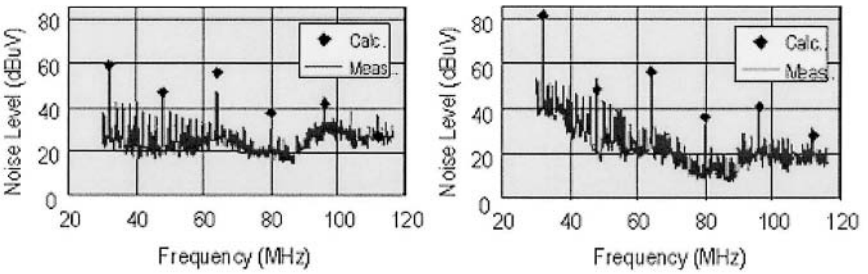


Figure 6-81. Measurement and simulation for two different capacitor arrangement.

A top priority capacitor arrangement must therefore be assured for the terminal, but this is not mentioned in most hardware manuals and few ECU designers seem to be aware of this. Moreover, even if the capacitor is connected to the internal regulator output terminals "C" or "REGC," the RF-current would spread over a large area on the circuit board unless the shortest return circuit path is formed by a GND pattern layout between the capacitor and the LSI, and noise will propagate over the entire ECU. This phenomenon was confirmed in simulation.

The ECU used is the same as that shown in Fig. 6-80. In this analysis we analyzed not the noise level of the connector terminals, but rather the RF-current path propagating on the board. The results are shown in Fig. 6-82 & 6-83. As in Fig. 6-81, a pass/fail analysis can be done with only an evaluation of the noise level at the connector terminals, but in the case of a fail result no information is given for improvement of the design. This is therefore not a useful tool for designers.

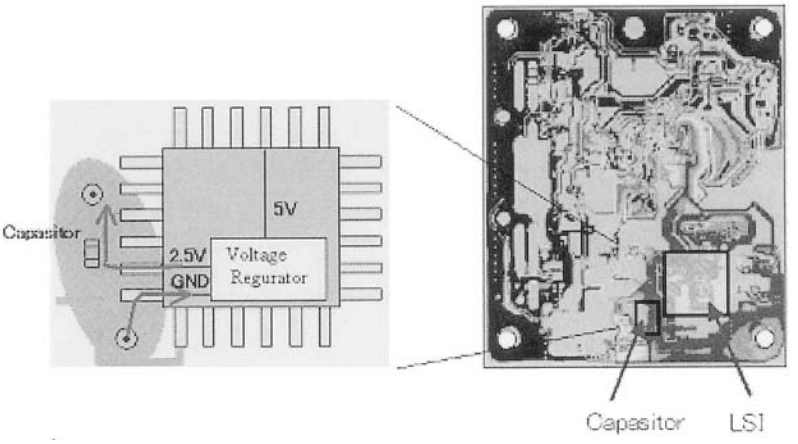


Figure 6-82. Noise current flow when the location of the external capacitor and its connection to an internal regulator is inappropriate.

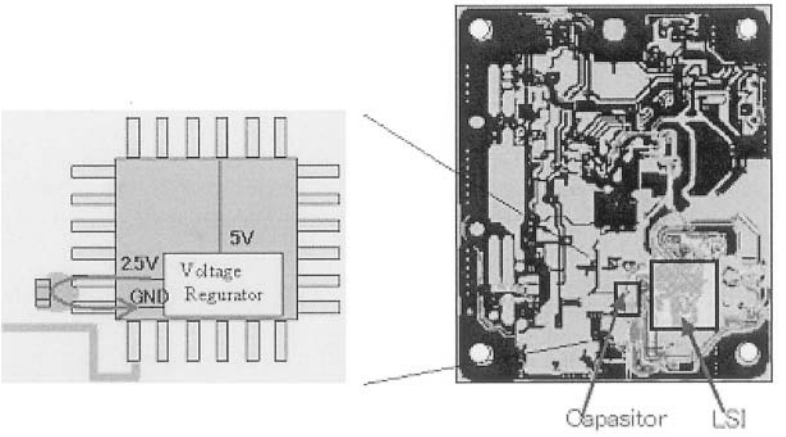


Figure 6-83. Noise current distribution with improved location of the external capacitor and its connection to an internal regulator is inappropriate.

One useful method for designers is a propagation path analysis. In Fig. 6-82 and 6-83 we can see the importance of board layout and capacitor arrangement, and investigations of this are possible with simulation using the LECCS model.

Another example is the GND pattern layout of the oscillator circuit; noise propagates over the entire board if an appropriate return path is not set for the GND terminals of the buffer in LSI for the oscillator circuit.

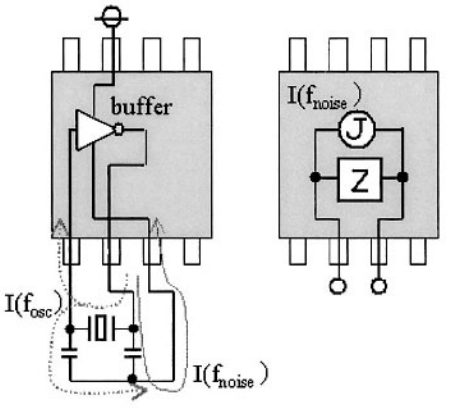


Figure 6-84. LECCS model for oscillation circuit.

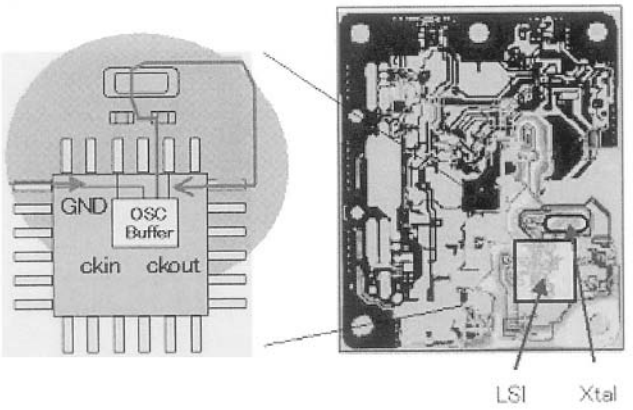


Figure 6-85. Influence of inappropriate positioning of oscillation circuit GND.

If the connection relation between components, such as ceramic or crystal oscillator and capacitors, and GND terminal of the LSI is inappropriate, noise propagation is large. To analyze this phenomenon, it is necessary to model the oscillator buffer in LSI. This modeling was done using the measured data of the RF-current at the oscillator buffer. An example of this model is shown in Fig. 6-84.

Fig. 6-84 shows the results of analysis with an inappropriate ground pin assignment, and the connections of the GND on the board, while the results with appropriate wiring are shown in Fig. 6-85.

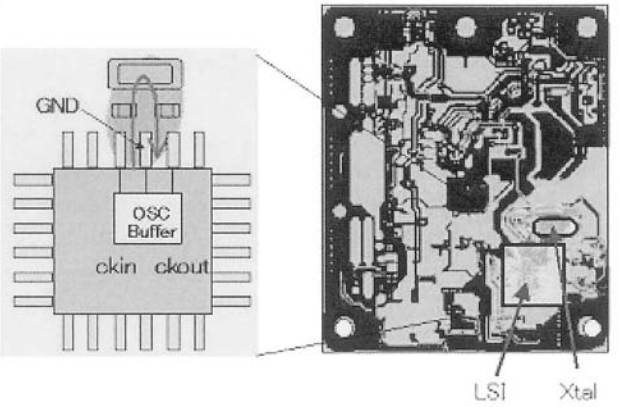


Figure 6-86. Appropriate positioning of oscillation circuit GND.

In the example of an oscillator circuit, noise propagation on the circuit board will become greater when GND wiring to the LSI GND terminal is inappropriate, so the arrangement of LSI terminals is important. In Fig. 6-82 and also 6-83 as well, the positional relationship between GND terminals and "C" or "REGC" terminals is important. For microcontrollers to realize easy EMC design of a circuit board, it is understood that terminal arrangement is important together with a low noise level in the microcontroller itself. In the terminal arrangement in microcontrollers, it is necessary to determine the positional relationship between power and GND terminals, and oscillation circuit terminals with consideration of easy layout design.

Simulations at the ECU level were conducted to analyze the effect of externally mounted capacitors on regulator pathways and the effect of GND wiring of the oscillation circuits, respectively, and demonstrated a high effectiveness of simulations using the LECCS model. In real-life product design the analysis time must also be considered. It cannot be utilized in design flows unless analysis results become available in a short time. To conduct analyses in a short time, it is suitable to make a linear model and use it in the frequency domain rather than in the time domain. With AC analysis conducted in the frequency domain, results can be obtained in a short time. Models built in the time domain require considerable time to obtain frequency domain results from transient analysis, and it is also difficult to calculate propagation paths of specified frequency components on a circuit board.

9.4 Immunity analysis at the product board level

Next, an example of application of the LECCS model to immunity analysis is shown (Takahashi,. 2002; Ichikawa, 2004b). The LECCS model for immunity analysis (Fig. 6-87 right) is a modified version of the LECCS model used in the analysis above (Fig. 6-87 left). An example simulation is shown in Fig. 6-88 (right) for a case in which an LSI is tested using the DPI method (IEC 62132-4) as shown in Fig. 6-88 (left).

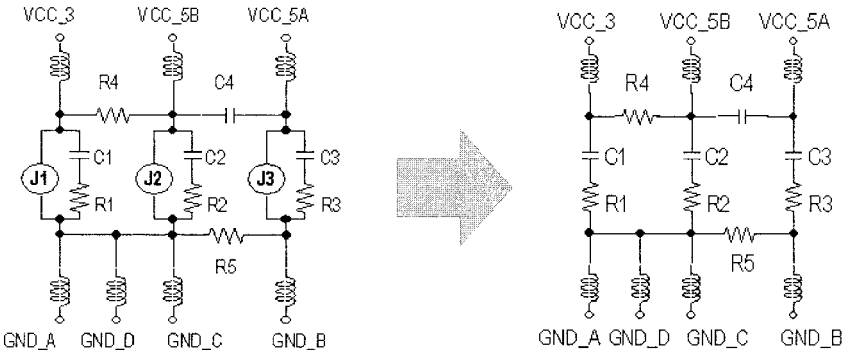


Figure 6-87. LECCS Model for EMI (left) and EMS (right)

With regard to the LSI malfunction level, the voltage level that occurred across the LSI power terminal and GND at the time of malfunction is taken to be the malfunction voltage. The evaluation system shown in Fig. 6-87 was modeled, an LSI model was added, and simulation of the terminal voltage impressed on the LSI due to the injected power in an amount to reach the malfunction level was taken to be the malfunction power, shown on the vertical axis in Fig. 6-87. In the test of immunity, the models derived at low power may have a limitation in accuracy, but even so there is agreement between the simulation and measured results up to the level in Fig. 6-87. In addition, the path of noise entry on the printed circuit board was analyzed. In this analysis LSI and power distribution circuits were allocated on the printed circuit board, and the DPI test was conducted. Current distributions with no additional capacitor to the power distribution path, and also with one additional capacitor arrangement on the path, were characterized with immunity tests.

The measurement results can be predicted by simulation. The validation of LSI modeling under high power conditions and development of criteria for judging malfunction needs to be investigated in the future, and efforts should be made to improve analysis accuracy.

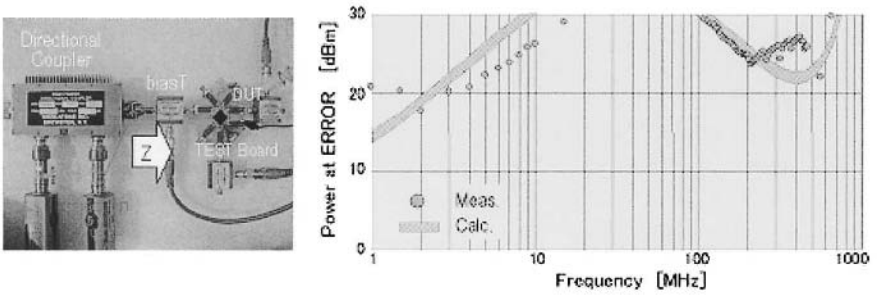


Figure 6-88. DPI test set-up, measured and calculation results.

9.5 Conclusion

Several examples of EMC simulation using LECCS models of LSI were shown. With an appropriate LSI noise model such as LECCS, many EMC phenomena caused by LSI and appearing within the printed circuit board can be analyzed. Using a frequency axis and linear model, the analysis time can be shortened. This is because we can perform the analysis while limiting the part and limiting the frequency. This makes it possible for designers to use simulations in the design flow, and for EMC performance to be built in to the product at the time of design. To improve product design efficiency, the effectiveness and application range for items such as unconfirmed know-how can be verified through simulation, and LSI noise characteristics can be closely analyzed beforehand. Establishing the design in the vicinity of the LSI is useful, and simulation can play a role in this.

Know-how is built up in this way with the use of simulation, and effectively incorporating this know-how in the design task is necessary to achieve EMC performance at low cost and in a short period. The computerization of automobile electronics devices is accelerating, while EMC specifications are becoming stricter and the design period is being reduced. Under these conditions, use of simulations will become increasingly important.

10. CONCLUSION

In this chapter academic and industrial contributors have presented case studies related to EMC characterization and modeling of integrated circuits. ST-Microelectronics described a test chip focused on the validation of low emission design techniques, which monitors internal current switching and correlates the on-chip noise to external conducted and radiated measurement.

Following similar goals, Philips proposed a test chip allowing a multi-parameter analysis, using design-of-experiments instead of carrying out an experiment permuting one factor at a time. Next, the Infineon test chip focused on the analysis of switching currents, thanks to a dynamic on-chip voltage and current sensor, in order to establish the correlation with electromagnetic emission measurements from 1 MHz to 10 GHz. The Freescale approach consisted in measuring and simulating the conducted parasitic emission of a 16-bit microcontroller, with focus on the effects of input/output port activity. Another approach by Atmel consisted in building reusable behavioral models to evaluate the activity of an 8-bit microcontroller, including inputs/outputs as well as processing and memory blocks.

As far as susceptibility phenomena are concerned, experiments from Philips and Eads-CCR were reported on simple integrated circuits for various technologies a well as electrical models that aim at predicting the response of the circuit under radio-frequency interference. Another experiment aimed at measuring the susceptibility of a 16-bit microcontroller from Freescale, and providing a methodology to predict its electromagnetic susceptibility.

Applications of EMC simulations using the various model approaches have also been described, that van be applied just as successfully in the pre-design stage as in the redesign process after an EMC failure.

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Chapter 7

GUIDELINES

Rules to improve EMC

Abstract: This chapter describes a set of efficient design techniques which may significantly reduce the parasitic emission and susceptibility of CMOS integrated circuits. Both layout level and package-related guidelines are presented. Concerning immunity, a set of defensive software techniques applicable to microcontrollers is also described. These guidelines have been applied successfully to several commercial products as well as specific test circuits.

Key words: Guidelines; low emission; improved immunity; on-chip decoupling; floor planning; defensive software; analog immunity; RFI

1. GUIDELINES FOR LOW EMISSION

Parasitic emission from an IC can be represented by three related but independent sources, core supply current, substrate or V_{ss}-net noise and I/O currents, as illustrated in Fig. 7-1. Guidelines presented in this part concern:

- The core supply noise.
- The packaging.
- The on-chip decoupling.
- The I/O noise.

1.1 Guidelines related to the core supply noise

When the core current as function of time is observed, the instantaneous peak current magnitude is much higher than the average supply current (Fig. 7-2). Two important guidelines apply for the core noise: reduction of the peak current $I_{peak.}$, decrease of the operating frequency f.

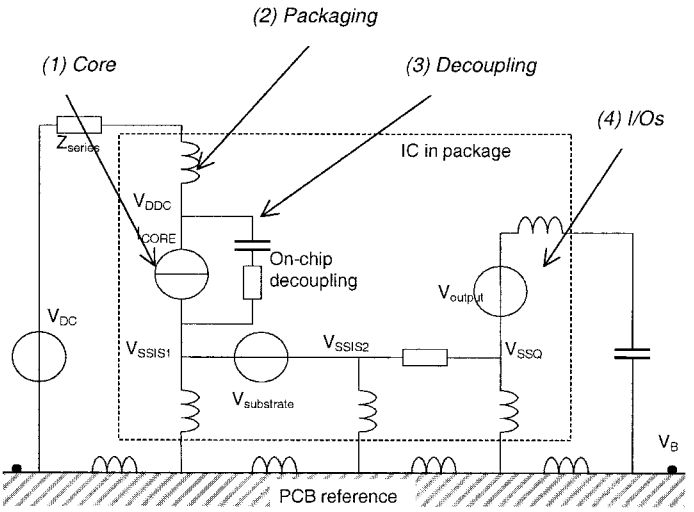


Figure 7-1. Guidelines for low emission may concern the core noise, packaging, on-chip decoupling and I/Os.

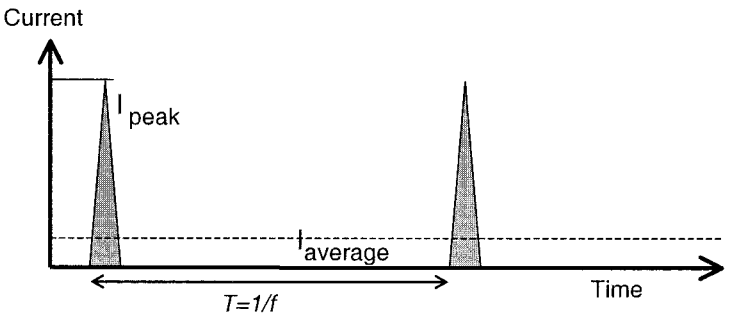


Figure 7-2. Current vs time.

1.1.1 Peak Current

The peak current has a direct impact on both the conducted and the radiated emission spectrum. Any unused clock, oscillator or buffer output should be turned off when not needed. Clock trees with distributed buffers should be preferred to very large clock drivers that produce strong switching current.

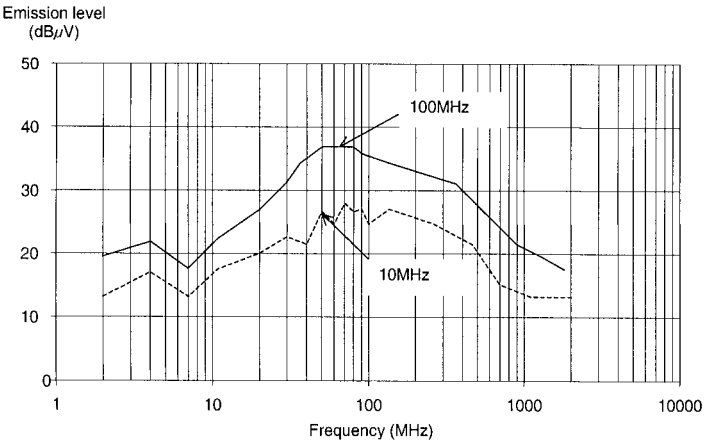


Figure 7-3. Reduced operating frequency leads to significant emission reduction.

Reduced di/dt is achieved by splitting the clock tree into sub-sections driven by a medium-fanout buffer, as well as by carefully adjusting the speed requirements and the buffer strength. When not justified by a very large load, oversized buffers are good targets for lower emission redesign.

The main guideline to reduce on-chip oscillator noise consists in transforming the large voltage-swing circuitry into a sinusoidal low-swing oscillation driven by a low current. This circuit features the same oscillation function without generating harmonics. High current mode may be used to start the oscillator or to lock the PLL quickly, but the oscillator should be turned to a low current mode just to maintain the oscillation. Reduced operating supply voltages are an efficient way to reduce the power consumption, current peaks and parasitic noise.

1.1.2 Operating Frequency

The operating frequency should be set to the lowest frequency needed to run the customer's application. Running a microcontroller at 10MHz instead of 100 MHz leads to a 20 dB reduction of the peak emission in a wide frequency range in the spectrum, as shown in Fig. 7-3.

1.1.3 Asynchronous design

Most of the digital integrated circuits today are synchronous, which means that their activity is controlled by a global clock which triggers thousands of logic gates at each active edge.

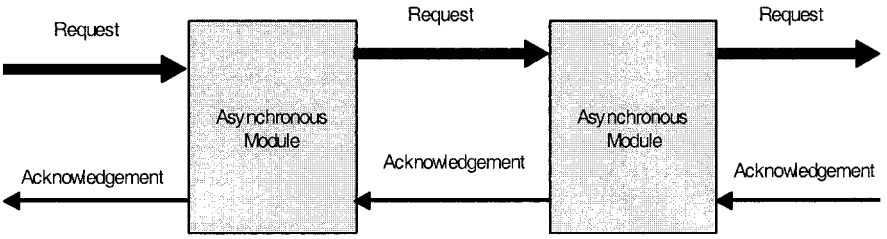


Figure 7-4. Handshake- based communication between modules.

Digital asynchronous circuits are composed of individual modules which are not controlled by a global clock but by data events. Communications through module ports are not controlled by an external clock signal but by a communication protocol (Fig. 7-4) based on request and acknowledgements known as handshaking (Renaudin, 2000).

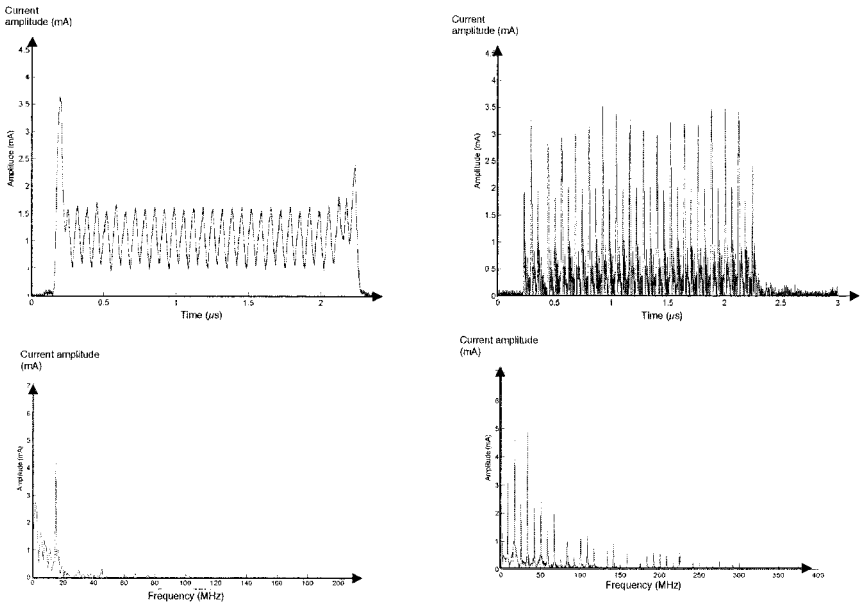


Figure 7-5. Time-domain and frequency-domain current measured on an asynchronous circuit and its synchronous version.

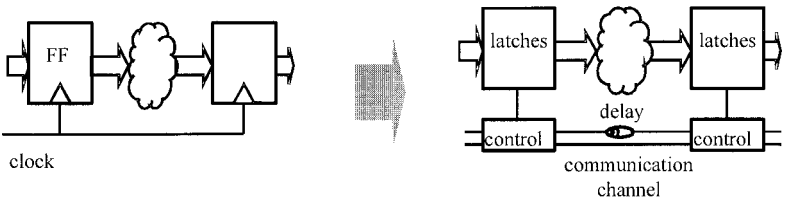


Figure 7-6. De-synchronization example.

Therefore, based on this principle, asynchronous circuits are not delay-sensitive. Asynchronous circuits usually require a larger number of gates and therefore a larger silicon area. In terms of EMI, an advantage of asynchronous circuits is that the electrical activity is spread in time and not concentrated on clock edges as is the case for synchronous circuits. This key intrinsic property suggests that asynchronous circuits generate lower electromagnetic emission than synchronous circuits, even if they use a larger number of active gates circuits. Novel design methodologies which aim at minimizing the parasitic emission of asynchronous circuits have been recently proposed in the literature (Panyasak, 2004).

Fig. 7-5 presents the measurements performed on two data-encryption standard (DES) crypto-processors designed and fabricated using a 130-nanometer CMOS technology. The current and the current spectrum curves are provided for the asynchronous version of a crypto-processor (left-hand side of Fig. 7-5) and for the synchronous version (right-hand side). Assuming that the level of emission is strongly correlated to the internal current spectrum, these results demonstrate that the asynchronous design approach significantly reduces the electromagnetic emission (Bouesse, 2004).

1.1.4 Guidelines for De-synchronization

Most IC design engineers have a digital synchronous background, with little knowledge of asynchronous circuits. A solution explored by the asynchronous community is to provide a means of transforming a synchronous circuit into another one that would be very similar to an asynchronous type one.

Basically, the "de-synchronization" methods (Panyasak, 2004b) basically replace the global clock by a set of local ones, generated by a distributed set of handshaking components. This principle is illustrated in Fig. 7-6.

To ensure valid data latching by the local clocks, the delay value must be matched to the worst-case latency of the combinational blocks.

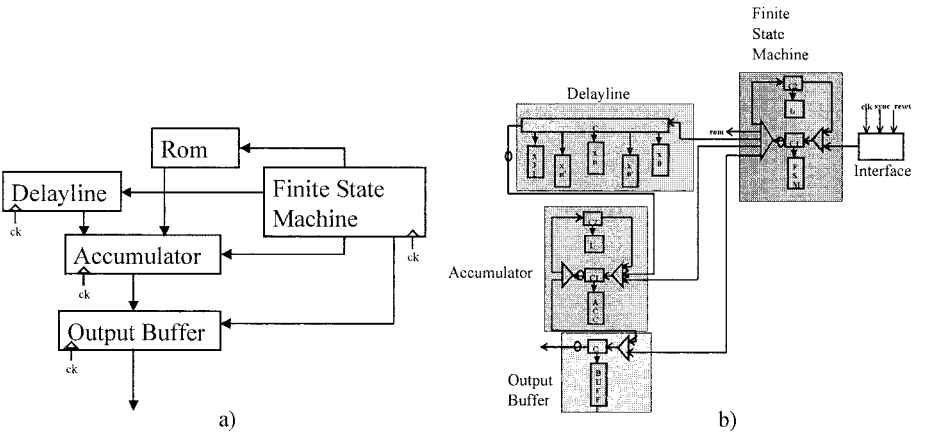


Figure 7-7. a) Synchronous FIR Filter. b) Asynchronized FIR Filter.

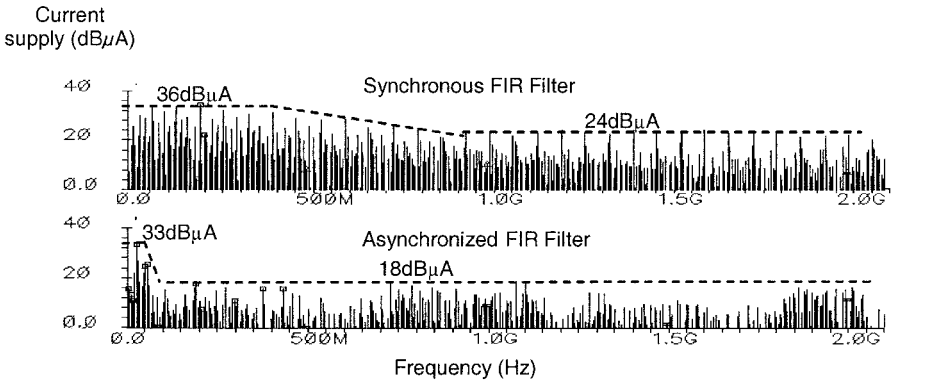


Figure 7-8. Impact of asynchronization on the current spectrum, in the example of a 4-coefficent FIR filter.

The communication protocol has to be chosen carefully because it has to guarantee data flow equivalence between the synchronized and the de-synchronized versions (Bluno, 2004). Moreover, data initialization in the synchronous circuit must be kept unchanged in the de-synchronized version. The method has been applied to a synchronous Finite Impulse Response Filter (Fig. 7-7).

The structure obtained after applying the de-synchronization method is given in Fig. 7-7b, where only the control parts and latches are represented. Fig. 7-8 presents the current spectrum for both versions of the FIR filter obtained by applying the Fast Fourier Transform (FFT) on the simulated time-domain current. It appears that the method leads to a -3 dB peak magnitude reduction, -18 dB average reduction from 50 up to 400 MHz and -6 dB above 800 MHz.

1.1.5 Current Shaping Methodology

Even if the noise reduction is substantial, the previous methods do not minimize the current peaks due to simultaneous switching noise within the circuit. A methodology called "current shaping" has recently been proposed (Panyasack, 2004), which aims at controlling the handshaking communications, especially the request and acknowledgment signal arrival times. The concurrent execution of the blocks is distributed over time to spread their current peaks. To achieve this, a set of delay is introduced in the communication channels, using the four fundamental steps detailed as follows:

- Modeling of the architecture. Concurrent blocks are identified using Control Data Flow Graphs (CDFG). Fig. 7-9a presents a CDFG for three parallel combinational blocks (multiplication, addition and ID).
- Estimating architecture block latencies. Delays inside the circuit are required for estimating the current profile duration. The CDFG is annotated with latencies estimated by logic synthesis and critical paths computation at the gate level.
- Modeling the Current Profiles (Fig. 7-9b). The current activity of each operator is split into sub-sets of current phases related to the communication protocol from which triangular current profiles are derived.
- Shaping the global current by scheduling. The scheduling strategy is applied so as to distribute the current consumption while not exceeding the maximum latency of the parallel blocks. By applying a Force Directed Scheduling (Paulin, 1989), the optimal start execution time of each parallel block is extracted (Fig. 7-9d to Fig. 7-9e). Results after optimization are shown in Fig. 7-9f.

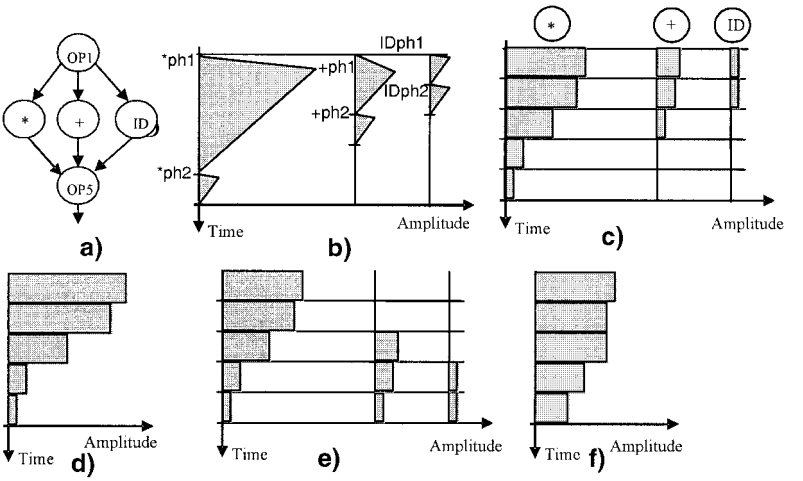


Figure 7-9. Illustration of the Current Shaping methodology.

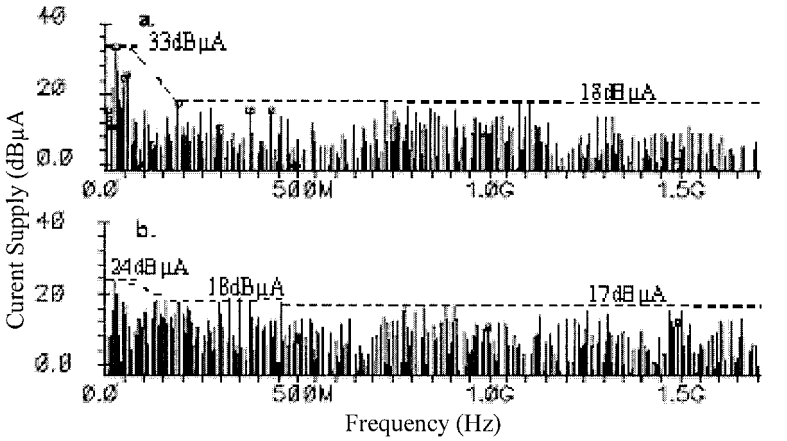


Figure 7-10. Current spectrum of the Asynchronized FIR filter before (a) and after (b) using current shaping methodology.

The method was applied to the 4-coefficients FIR filter presented in Fig. 7-7. Once the combinational blocks were estimated, analog electrical simulations provided the current profiles for each component.

Fig. 7-10 compares the current consumed by the asynchronous FIR circuit before and after applying the Current Shaping method. Despite the fact that the circuit features few concurrencies, the magnitude of the maximum current was reduced by about 9 dB.

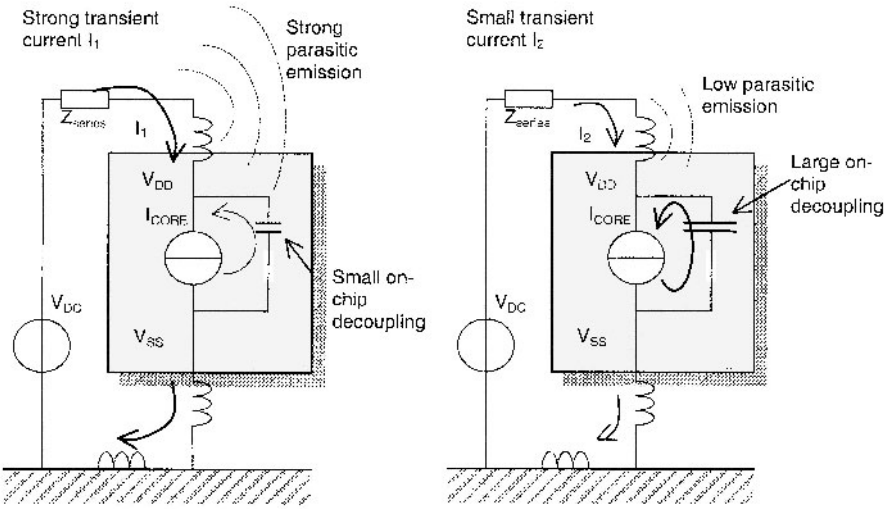


Figure 7-11. The role of on-chip capacitance for reducing parasitic emission

Applying asynchronization and current shaping to this circuit leads to a – 12 dB current peak reduction. The spectrum amplitude was kept almost unchanged above 200 MHz (-1 dB reduction).

1.2 Guidelines for On-chip Capacitance

An on-chip capacitance between supply lines acts as a charge reservoir for transient core switching which reduces the amount of current flowing through the leads. In the case of a small on-chip capacitance, most of the transient current flows outside the IC and generates high conducted and radiated emission (Fig. 7-10 left).

When decoupling capacitance is added on-chip (Fig. 7-10 right), the transient current flows mostly inside the IC, thus significantly reducing *di/dt* noise on package leads (Larsson, 1998). The time domain aspect of the external currents I_1 and I_2 is given in Fig. 7-11. Efficient techniques to implement on-chip capacitance consist in implementing large VDD and VSS power rails on top of each other for maximum coupling effect, connecting junction capacitance in the free area underneath the routing channels (Vrignon, 2005). The thin-oxide gate capacitance or metal-insulator-metal (MIM) capacitance may be used to generate high value capacitance (several nF).

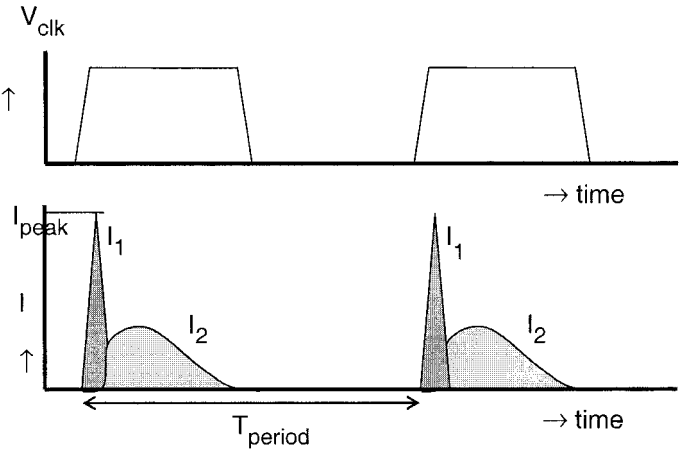


Figure 7-12. External current vs time with and without on-chip added capacitance.

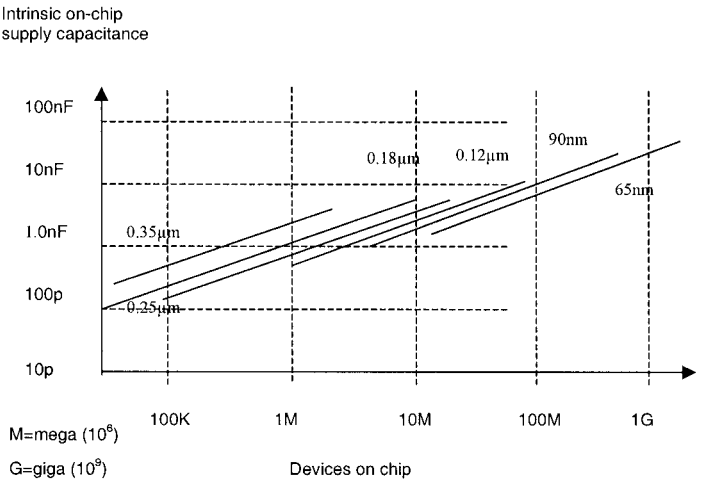


Figure 7-13. Intrinsic on-chip supply capacitance vs. complexity and technology.

The amount of on-chip decoupling capacitance is strongly related to the number of devices implemented on-chip, as well as to the technology, as outlined in Fig. 7-13. As an example, a 100-million transistor IC fabricated in 90 nm technology has an intrinsic capacitance around 10 nF. Adding on-chip capacitance may lead to a distributed 50 nF decoupling capacitance.

For nominal operation, the on-chip supply voltage should not be reduced by less than 90% of the nominal supply voltage to make sure that timing verification models can be interpolated within their operating conditions. To ensure this, the switching on-chip capacitance has to be of a lower order of magnitude than the non-switching capacitance.

The non-switching capacitance is a sum of all parasitic capacitance found in the supply wiring, N-well capacitance to substrate and the added on-chip gate decoupling capacitances, gate oxide, trench capacitances, etc. This 90% condition holds when the on-chip capacitance switches at once e.g. at the rising edge of the clock. In reality, switching capacitance occurs within flip-flops, standard cells and their wiring. The total amount of switching capacitance can be X pF/clock cycle where the charging current can be Y mA. With this assumption, the total (static) on-chip decoupling is set to be $10.X$ pF to satisfy the supply bounce conditions.

An improved on-chip decoupling system consists in adding a choke serial resistance. The principle of this technique is to further reduce the external transient current flow. This technique has proven to reduce the emission of a test IC efficiently (See chapter 6).

1.3 Floor-planning

The bonding wires that link the die of the IC to the package are mainly inductive and significantly contribute to the serial inductance on the supply path. A package cavity adjusted to the die size shortens the bonding and reduces the serial inductance. Furthermore, the assignment of low current wires to the longest leads is preferable, while supply lines should use the shortest tracks (Fig. 7-14).

The systematic use of adjacent VDD and VSS wires minimizes the power-ground current loop, therefore reducing the magnetic field radiated by the IC (Coenen, 1996). Furthermore, assuming that the time-domain current waveforms are similar for the VDD and VSS leads, a phenomenon called field cancellation can be noticed that significantly reduces the magnetic field radiated by the leads, as seen in the simulation of Fig. 7-15.

Multiple supply paths divide the equivalent inductance and thus reduce the supply fluctuations in a linear way. An example of pin assignment for a 16-bit microcontroller is given in Fig. 7-16. Up to 22 ground signals (VSS) and 22 supply signals (VDD) have been dispatched around the package. Some of the supply signals are assigned to the logic core, others at the oscillators, analog parts and I/Os.

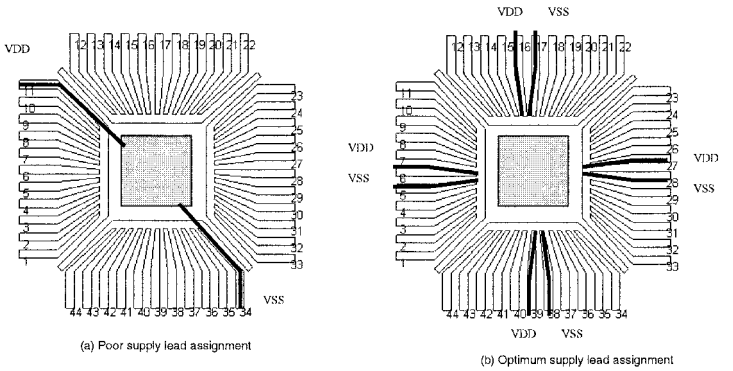


Figure 7-14. Improved VDD/VSS assignment

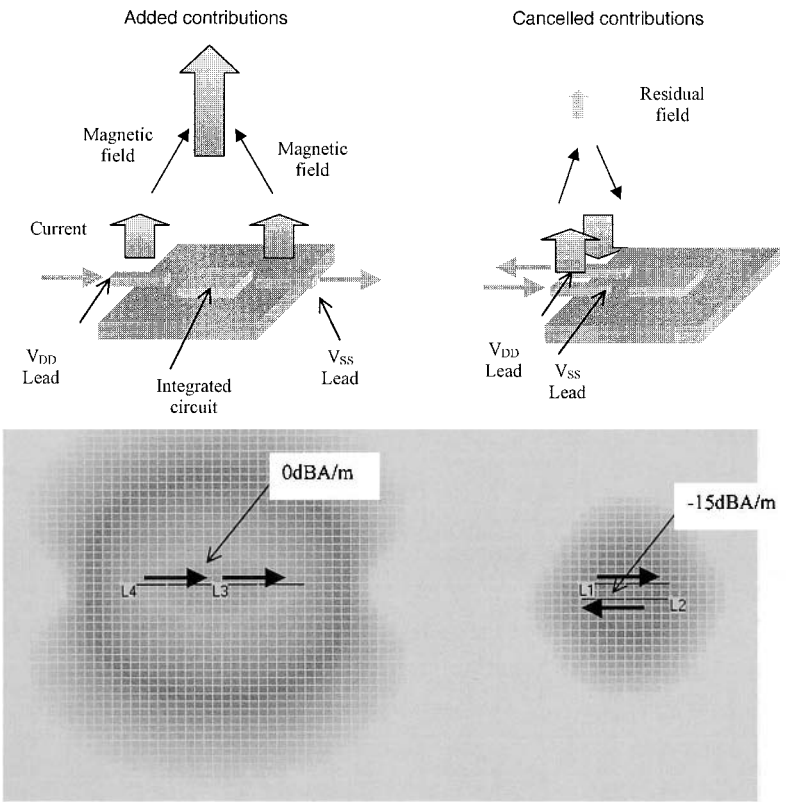


Figure 7-15. Using VDD/VSS pairs instead of placing VDD and VSS at each corner of the IC may lead to 15dB emission reduction

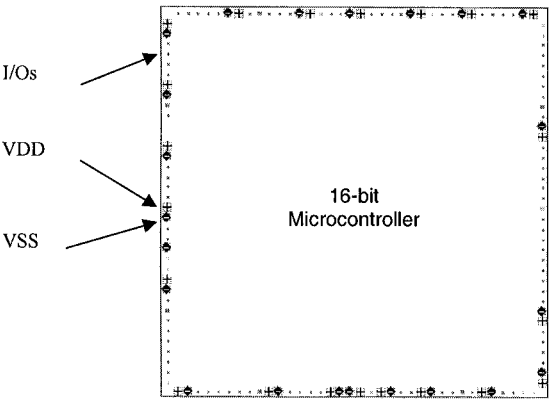


Figure 7-16. Placement of supply lines by pairs (VDD= 5 V, VSS= 0 V).

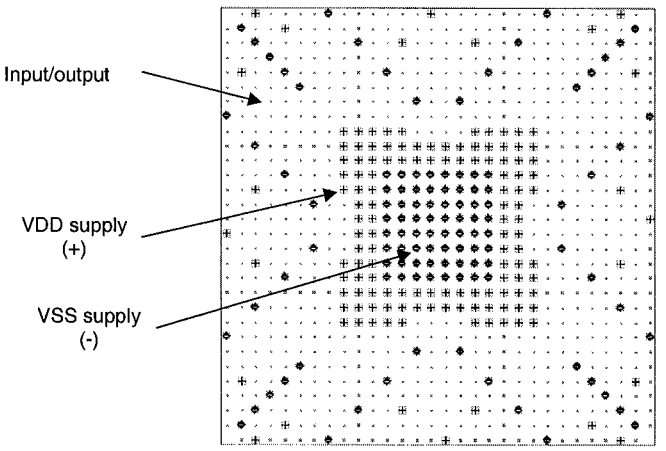


Figure 7-17. VDD/VSS assignment for a VIRTEX programmable device.

Another floor planning example concerning the Virtex programmable device is given in Fig. 7-17. The use of multiple VDD and VSS access pins at the center of the package spilts the current into more than 60 paths, thereby reducing the equivalent parasitic inductance and the resulting ringing effects. Implementing VDD and VSS pads close to each other also eases external decoupling and increases the VSS/VDD capacitance.

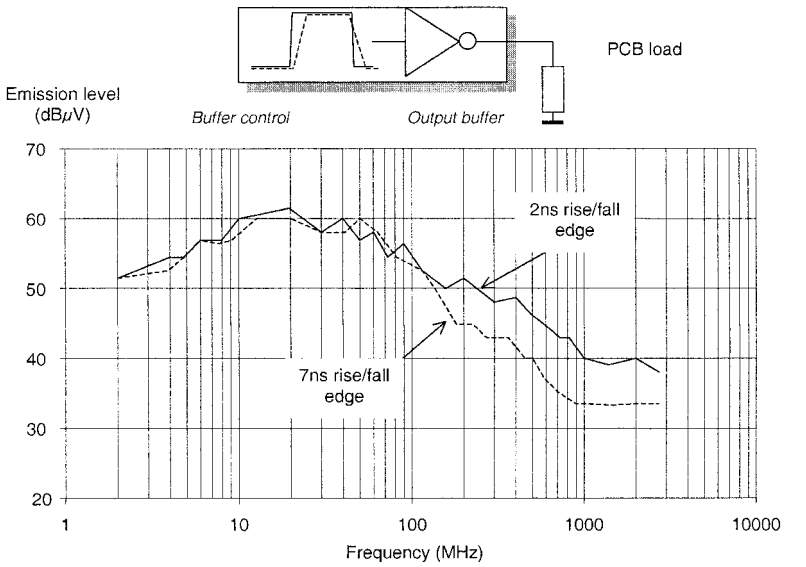


Figure 7-18. The high-frequency conducted noise emission may be reduced by a slew-rate control of the output buffer

1.4 Input/Output Buffers

One major source of *di/dt* noise comes from the output buffers. The buffer is usually designed with a very high drive to match worst-case switching speed constraints, thus large MOS devices with *Ion* maximum current capability are often present. The synchronous switching of the *n-channel MOS* and *p-channel MOS* devices leads to a short circuit current peak that can be reduced by adding a small delay between the device transitions. Most microcontrollers and programmable devices feature programmable-size drivers that may accommodate any loading condition ranging from the large capacitive loads found in large boards or cable interfaces to smaller loads such as external memory interfaces.

An important element to take into consideration in reducing the parasitic emission is the slew-rate control of the buffer. The technique consists in slowing down the buffer control signal so as to avoid ringing while meeting the switching delay requirements of the target application. The gain in terms of parasitic emission is significant in the range 100-1000 MHz, as seen in an experimental conducted noise measurement performed on a 16-bit microcontroller (Fig. 7-18).

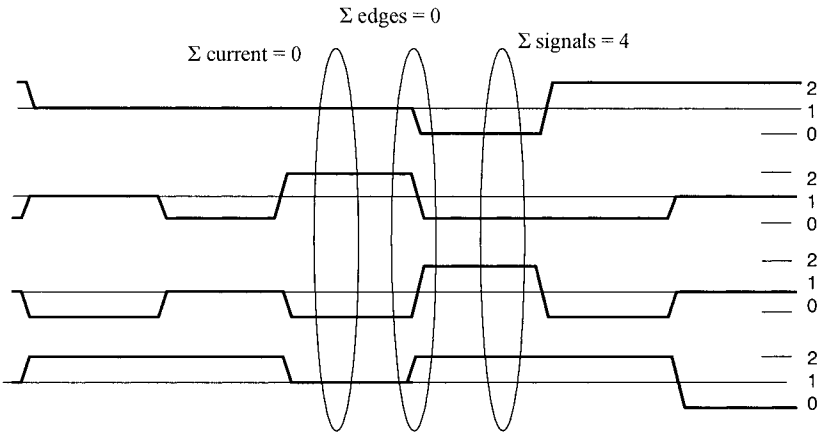


Figure 7-19. An I2Q signal representation.

Input/Output busses can be a burden to the overall system as they are necessary to allow communication between several blocks inside the chip and between ICs. There are several options to ensure that only DC current is drawn by the bus, whatever its data content. A simple option is a differential bus like USB, Firewire, RS-442, 485, LVDS, SLVS, PCI Express, etc. where the sum of currents exchanged is ideally constant. The main disadvantages are that the number of pads required doubles (100% overhead) and that, in comparison to digital interfaces, more complex sense analog circuits have to be designed.

Other options are the use of balanced codes rather than differential signals. By using 6 lines instead of 4 (50% overhead), 128 codes are available out of which at least 16 can be chosen, whose sum of signals is constant (but still binary). When ternary levels are used like illustrated in Fig. 7-19, 3^4 codes (=81) are available out of which another 19 codes can be selected, whose sum is constant.

1.5 Substrate noise

Although the *di/dt* parasitic effect in the off-chip supply rails can be diminished, the peak currents on-chip will remain unchanged and will flow, time-variant, through the V_{DD} and V_{SS} nets of the core between the active circuits and the non-active and passive decoupling, as illustrated in Fig. 7-20. As a result of the fact that the V_{SS} net impedance cannot be reduced below the sheet resistance value of the top metallization layer, 10-50 mΩ-square, the voltage gradient between north-south or west-east V_{SS}-pads will be zero on average but not at any moment in time.

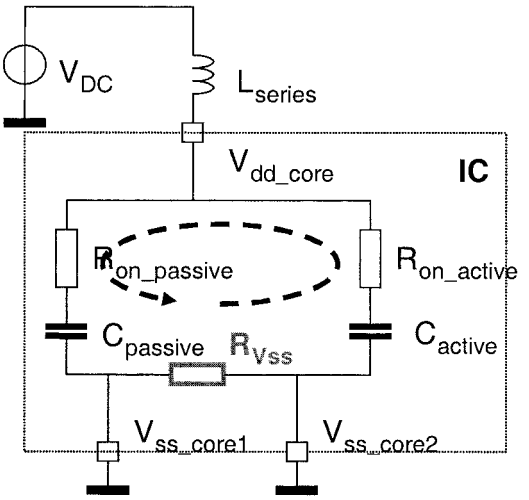


Figure 7-20. On-chip current flow through the substrate

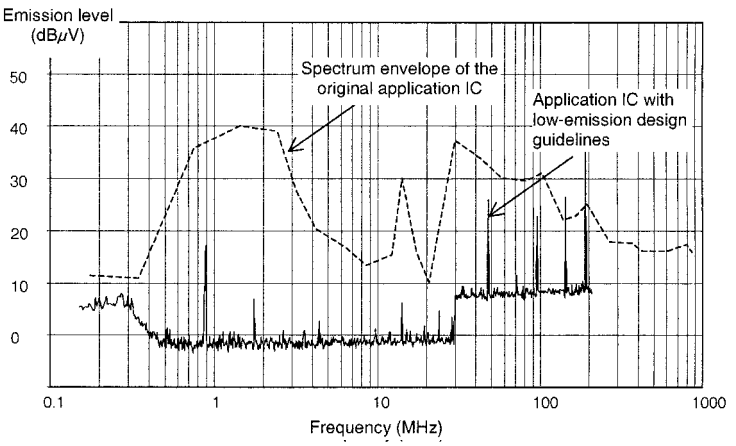


Figure 7-21. Conducted RF emission according to IEC 61967-4, original (dot) and modified version (spectrum).

For example, when a large bus is applied from north to south and the communication is from master to slave or from slave to master, the opposite polarity of noise will be induced in the V_{SS}-net, though the average noise over time, as calculated in IR-drop calculations, is approximately zero. Design guidelines to minimize the peak currents may consist in placing decoupling capacitances next to circuits that require peak currents regularly.

The instant charge can then be supplied from the adjacent decoupling capacitance. Thus only the re-charge current will be drawn from the remainder of the decoupling capacitance available on-chip. This requires the ratio of RC-time constants between the adjacent decoupling and the global on-chip decoupling to be such that the adjacent decoupling delivers the high peak current i.e. that is the fastest response.

Other obvious options are to distribute the clock phases over the clock cycle to ensure that no instantaneous switching will ever takes place, but that all actions are performed sequentially. This solution is very close to asynchronous logic design solutions as described earlier in this chapter, though the synchronism with the system clock may still be used.

A demonstration of low emission design rule effectiveness is provided in Fig. 7-21, with a comparison of measured conducted emission concerning a digital CMOS 0.18µm application product with and without implementing these guidelines. The figure shows the improvements versus the original performance (dot), without any performance degradation for this application circuit. What can be noted is a small emission level increase above 100 MHz.

2. GUIDELINES FOR IMPROVED IMMUNITY

2.1 Introduction

Traditional approaches for improved immunity consist in adding filtering and shielding to protect the electronic systems against radio-frequency interference. At integrated circuit level, similar techniques may be applied to enhance the immunity to radio-frequency interference. Specific design techniques or embedded software approaches may also be used, as detailed in this section.

2.2 On-chip decoupling

On-chip decoupling has proven to be a very efficient way to reduce emission. In terms of immunity, the impact of the on-chip decoupling from the point of view of transfer efficiency from the source to the internal core can be investigated by an AC analysis, as shown in Fig. 7-22. The injection source consists of a perfect voltage source. A transmission line without losses models the injection cable, and the DPI injection is represented by a simple 6nF capacitance.

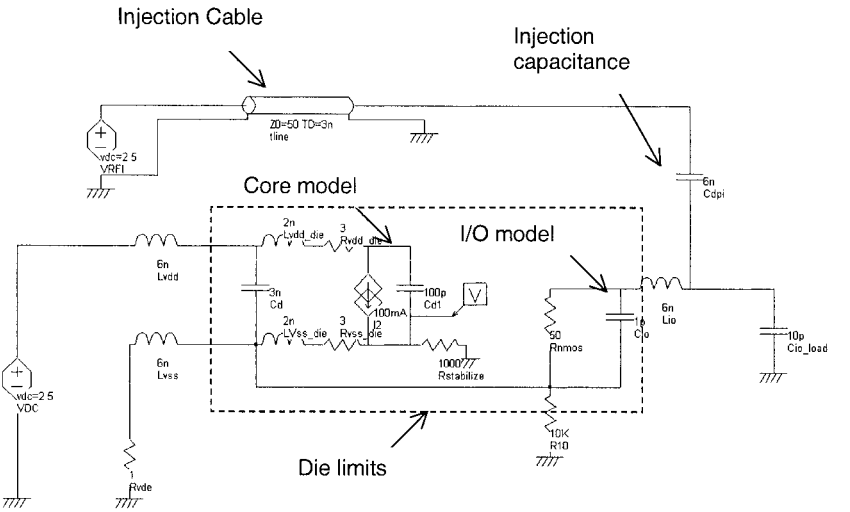


Figure 7-22. Immunity simulation to investigate the role of the decoupling capacitance

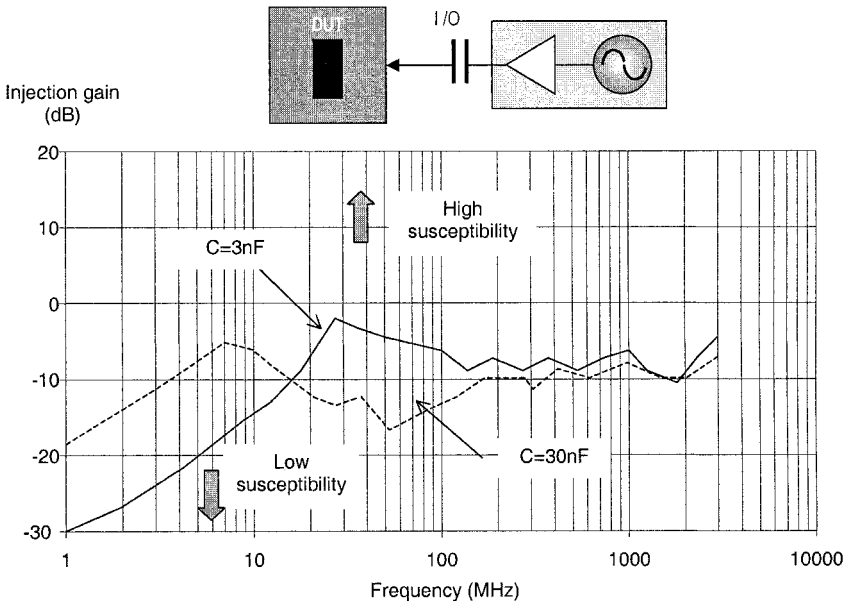


Figure 7-23. Effect of on-chip capacitance on transfer gain from the RFI source and the IC core.

When on, the pull-down MOS device may be considered as a resistance ranging from 10 to 1000 Ω depending on the buffer driver. One possible path for the power injection on the IC output is the resistive and capacitive link of the I/O to the substrate. The RFI noise propagates to the core and may disturb the nominal behavior due to ground and power bounce.

From the simulation of Fig. 7-23, it can be seen that the on-chip decoupling capacitance *Cd* has a significant impact on the low-frequency transfer gain between the noise source and the internal part of the IC. By increasing *Cd* from 3 nF to 30 nF, the resonant frequency is shifted from 30 MHz to 7 MHz.

2.3 Defensive Software

Focusing on the microcontroller world, part of the hardware problems due to EM susceptibility may be handled by using software solutions. This technique is called defensive software, and aims at reinforcing the robustness of the embedded system. The modification of the embedded software can make it possible to meet EMC requirements without having to modify the hardware. Moreover, the software modification is generally less time-consuming than the electronic board modification, or the obviously the IC design itself.

In the next paragraphs, we shall distinguish three categories of defensive software: input/output management techniques, volatile memory handling, and control flow supervision. All the software techniques presented hereafter are focused on embedded applications.

2.3.1 I/O management

In all applications, the management of the inputs/outputs is paramount as it connects the control processor unit to sensors, actuators or communication interfaces. Microcontroller input/outputs are privileged accesses for the disturbances induced by the electromagnetic fields. Communication protocols, data registers, and execution units are potential victims of such interferences.

Communication protocols use redundant additional bits such as parity bits which are able to detect an error in the transmitted information, but which are usually insufficient to allow the error correction (Coulson, 1998). Redundant codes such as the BCH code (Bose, 1960) used in the Control Area Network (CAN) protocol allow both error detection and correction.

Microcontrollers include general-purpose ports that can be configured as input or output ports. The configuration is usually user-programmable through a data direction register.

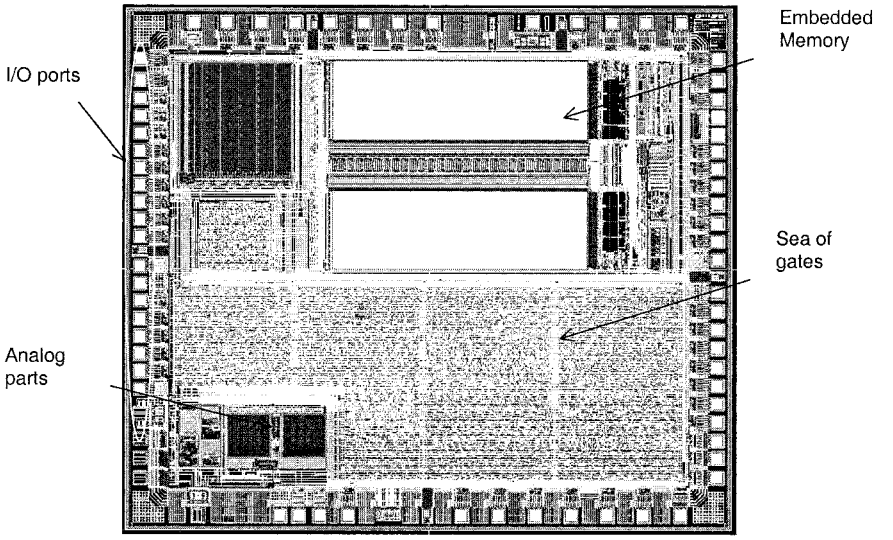


Figure 7-24. Layout of a 16-bit microcontroller (Courtesy Freescale Semiconductors)

To avoid corrupting the port configuration, a software technique consists in regularly refreshing the value of the port data direction register (Campbell, 1998), with negligible time cost and memory space.

2.3.2 Input data management

The input data management depends on the analog or logic nature or on the information. Although defensive software solutions are linked to target applications, generic solutions exist (Baffreau, 2002), as described in this section.

Fig. 7-25 illustrates the fact that the sensor response is usually valid for a given voltage or current range. Consequently, the software can easily detect and ignore sampled values outside the validity domain, such as the ones induced by a transient electromagnetic disturbance. The variation of the sensor response may also be investigated. An excessive variation between two measurements may be considered as an erroneous value. For example, a temperature fluctuation should not exceed 1 degree over a one-millisecond time interval. More traditional signal processing techniques such as numerical filtering may also be used, at the expense of increased code size and execution time.

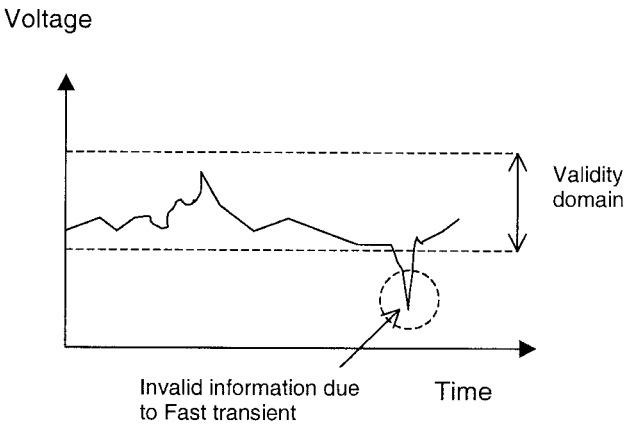


Figure 7-25. Sampling and management of the analog input.

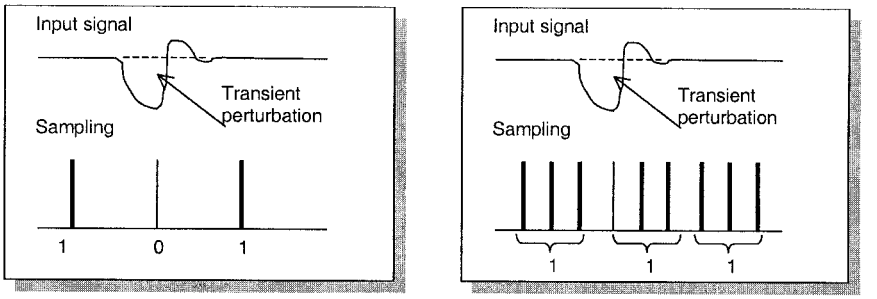


Figure 7-26. Logic filtering to tolerate the effect of fast transients on an input

A data checking similar to the analog data processing can be performed for numerical data (Coulson, 1998). Thus, rather than validating an input data immediately (Fig. 7-26 left), several samples can be stored with a vote to determine the value to consider (Fig. 7-26 right). The approach is not time consuming as long as a reduced number of samples is considered (3 in the example).

Furthermore, the data can be considered as valid if all samples are identical. If not, the system rejects the data, acquire a new set of samples and waits for a stable input information. This technique is particularly efficient at detecting signals mixed with fast transients or even with radio-frequency interferences.

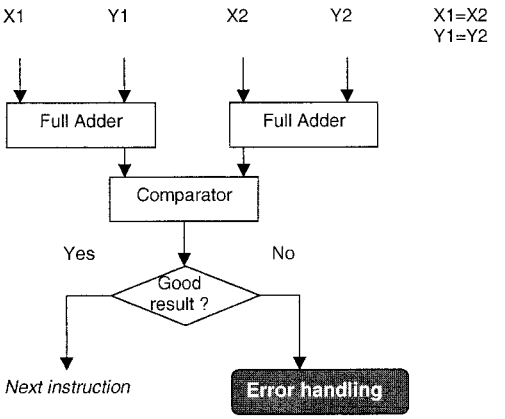


Figure 7-27. Data duplication, parallel processing and result comparison

2.3.3 RAM management

Several memory management methods exist to increase the software protection against erroneous execution as a consequence of RF interference. The data duplication and parallel processing (Geffroy, 2002) illustrated in Fig. 7-27 in the case of an addition, slows down the program execution significantly. Although an error might be detected, the method does not provide any correct data recovery.

A similar technique presented in (O'har a, 2001) named "Code Ghosting" is based on the triplication of data and the code execution on valid data only. Obviously, the main drawback of this approach is the memory space and execution time increases. A lighter solution (Coulson, 1998) consists in affecting several variables to a table and associating a checksum. Before each access to a variable of the table, the checksum is recomputed to make sure that its contents have not been corrupted. At each writing access, the checksum is computed and updated.

This technique has the advantages of not being memory-space consuming, and of allowing error detection and recovering, which complies with embedded system regulation constraints. However, the executing time overhead might not be negligible when dealing with a large number of variables and frequent read/write table access handling. In this last case, it is strongly recommended to split variables into several tables, each one having its own checksum and functioning on the principle established beforehand. Another important recommendation is to select critical variables only.

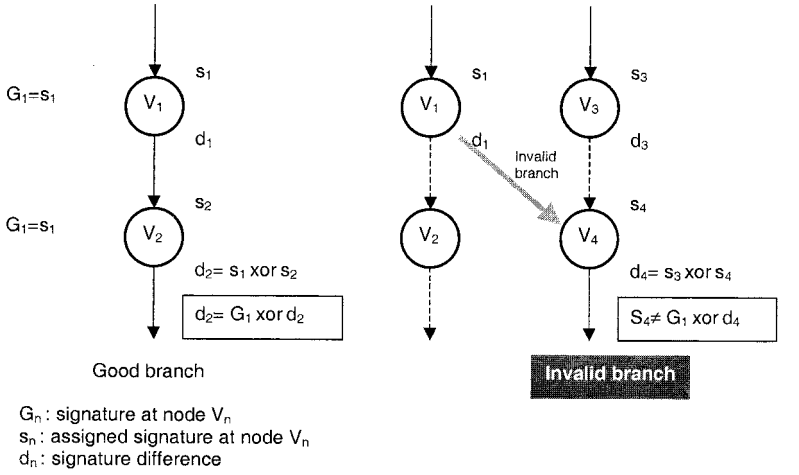


Figure 7-28. Principle of software signatures for checking of the control flow.

Moreover, a precise knowledge of the memory space needed for the application may give boundaries to the memory stack. Suppose the software entered an involuntary infinite loop that uses the stack to store particular variables at each iteration. The consequence would be a continuous growth of the stack memory that would eventually lead to a stack pointer overflow. Establishing a maximum size of stack memory can make it possible to avoid erratic behaviors.

2.3.4 Control flow management

The control flow corresponds to the management of the program sequences. The good execution of its sequences is essential to obtain reliable data processing. Various defensive software techniques may be applied to control flow. Checking the control flow by software signatures is described by (Oh, 2002). The principle is illustrated in Fig. 7-28. Application softwares can be subdivided into several independent blocks: procedures and functions. The main properties of these blocks come from the fact that they cannot have jump or branch instructions apart from the first and the last instructions. Moreover, at compilation time, each block is assigned a signature, noted s_i, and an associated signature difference, noted d_i.

During the software execution, a general-purpose register, noted *Gn*, is specifically reserved to contain the current block signature. When a block change occurs, *Gn* is updated via a simple comparison function, such as an exclusive-OR with the *dn+1* signature difference.

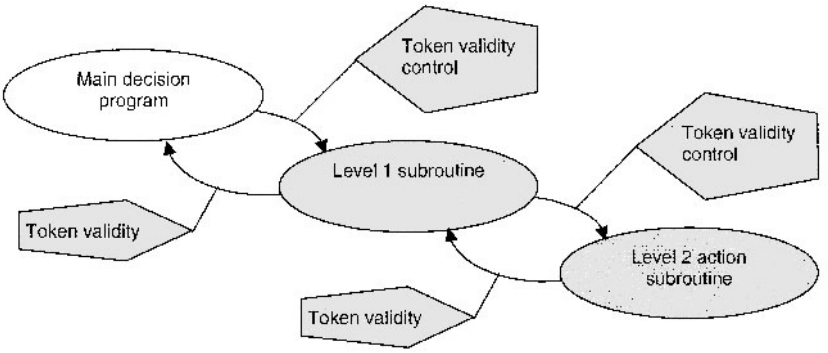


Figure 7-29. Principle of operation of the markers of passages.

If the contents of new *Gn* corresponds to the block signature and its valid branch, the program continues its execution. Otherwise, the program is diverted towards a specific error-handling mode.

This technique can be directly implemented in a compiler, thus being transparent to the programmer. Moreover, if the block size is large, the signature checking represents a small computational time overhead. Specific registers must be reserved for the signature storage and management, which fits well with RISC processors as they feature a large number of general-purpose registers. In contrast, CISC processors may need more complex memory access and the execution time could be strongly penalized.

2.3.5 Token passing

The principle of the token passing (Fig. 7-29) is similar to that of control flow signature, but concerns function or procedure calls (Ong, 2001). During the software execution, the sender block checks that the token passing to a procedure corresponds to its own token passing. Then, it modifies the token passing to take the value of the called block. The approach is applicable to sub-calls such as those illustrated in Fig. 7-29. If the token is invalid, the program is diverted towards an error-handling routine.

2.3.6 Filling the unused program memory space

Software applications rarely use all the available memory space. Unused memory space usually contains "0xFF" hexadecimal value (Equivalent to all bits set to "1") by default. Depending on the microcontroller instruction set, this "0xFF" value will correspond or not to an executable instruction. As a consequence of electromagnetic interference, the counter program may jump to an unused memory space address, and execute a wrong code.

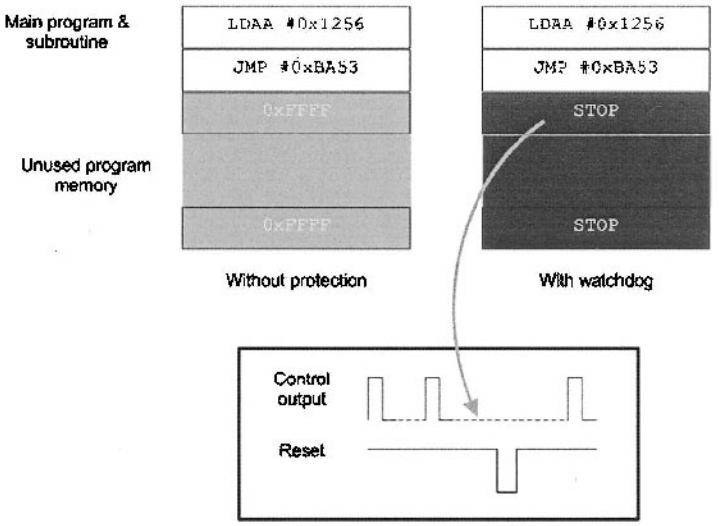
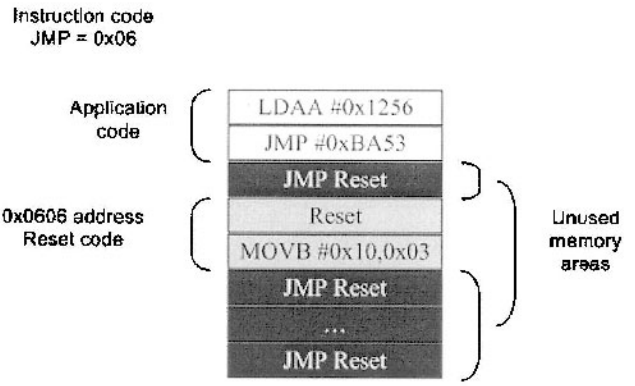


Figure 7-30. Filling the unused program memory with the STOP instruction.



There are several solutions to anticipate this erroneous behavior. The first possibility consists in filling the unused memory with a *Stop* instruction that puts an end to the execution program and sets the microcontroller to a state of latency (Baffreau, 2002). The on-chip or off-chip watchdog will detect an abnormal microcontroller state and generate a reset, as illustrated in Fig. 7-30. An alternative to the *Stop* instruction is the *No Operation* (NOP) instruction, terminated by a jump to the main reset program. If the unused memory space is large, the latency time before a master reset will be significant.

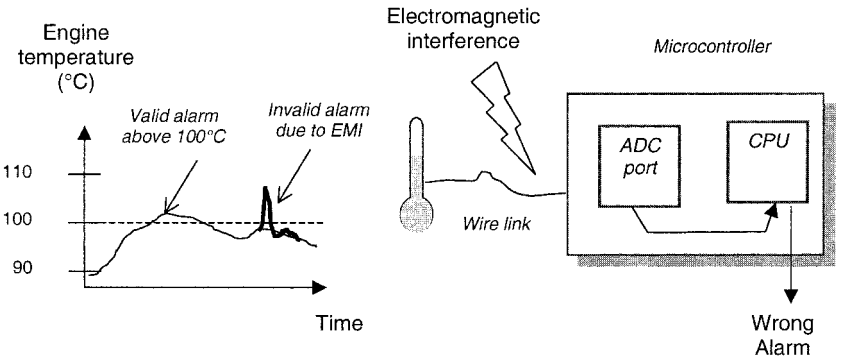


Figure 7-32. Over-temperature monitoring example.

The *Nop* instructions may also be replaced by *Jump* instructions to the reset address. In that case, the reset address should be user-configurable. Furthermore, the reset address should be identical to the *Jump* instruction code and correspond to a valid program memory location, which unfortunately is not always the case. In Fig. 7-31, the *Jump* code is "0x06", and the address "0x0606" is user-accessible, with a branch to the reset procedure. This technique does not require any additionnal execution time or memory space.

2.4 Defensive software example

This paragraph illustrates a defensive software example dealing with temperature sensing by a microcontroller. The general diagram of the application is reported in Fig. 7-32. The engine temperature is captured by a sensor, sampled by an analog-to-digital converter and processed by a microcontroller. An alarm should be asserted if the measured temperature exceeds a predefined limit. An electromagnetic disturbance may couple to the sensor, disturb the analog information and provoke a false alarm.

2.4.1 Signal Specifications

The sensor information is valid between a minimum and maximum sensor voltage limit, appearing in Fig. 7-33 as *SL_min* and *SL_max*. Moreover, the sensor information may be considered as invalid if the variation between two samples is higher than a predefined limit.

In the example, the sensor information is emulated with a triangular signal from 1.15 V to 3.85 V, with a slow period corresponding to the engine temperature variations.

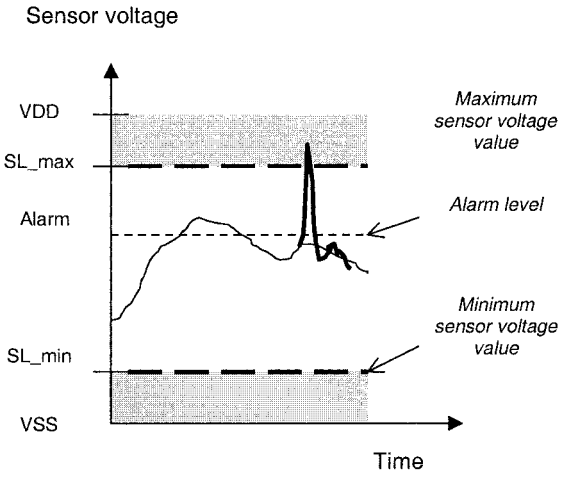


Figure 7-33. Illustration of generic sensor limits.

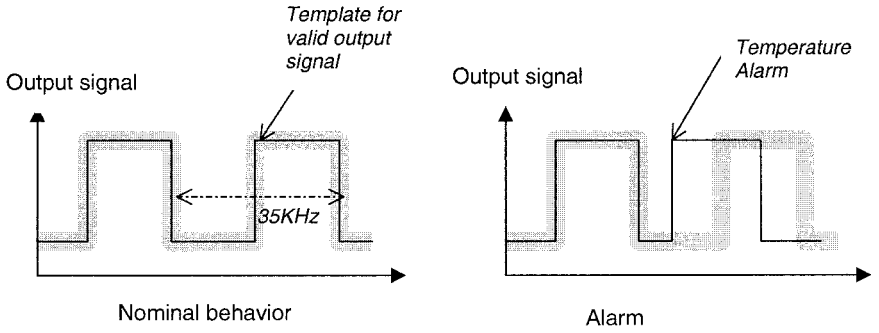


Figure 7-34. Characteristics of the alarm signal.

The microcontroller could generate an output signal to inform of a temperature alarm as follows:

- A low voltage level corresponds to a nominal operation.
- A high voltage level announces a temperature overflow.

Such a signal has the advantage of being simple and easily observable by the immunity control software. However, in case of a sudden microcontroller stop, it is probable that the output will be not refreshed and consequently the monitoring system will not be able to detect the internal processor failure.

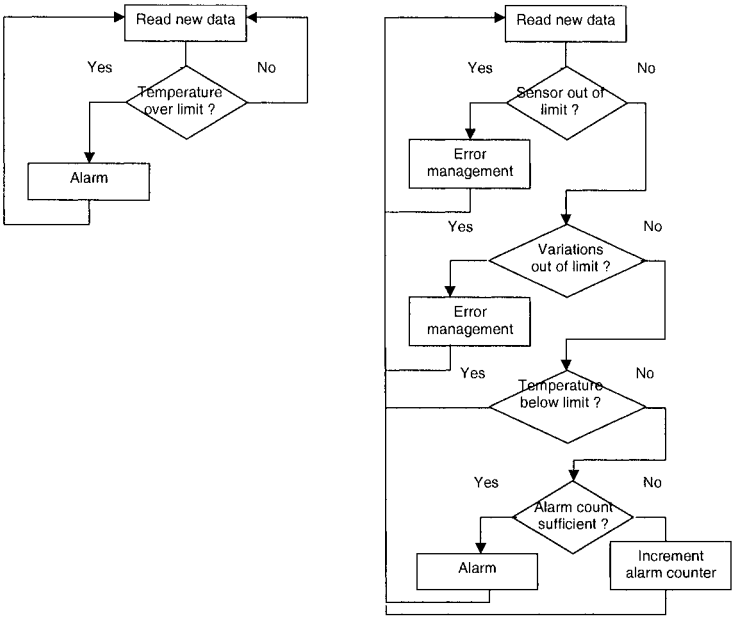


Figure 7-35. Flow chart of the standard and defensive software

The output signal should preferably consist of a periodic signal generated by the microcontroller (Here 35 KHz frequency, see Fig. 7-34). In the event of an alarm, the output signal state is changed to cause a sudden modification in the output frequency. A frequency counter, a memory oscilloscope or a logic analyzer, can easily detect this alarm signal. The output signal should remain in a defined template waveform, usually fixed with a time and voltage tolerance of +/- 10%. The right part of Fig. 7-34 illustrates the consequence of a temperature alarm on the output signal shape.

2.4.2 Defensive Software Implementation

Fig. 7-35 presents the flow chart of the default and defensive software. The number of samples taken before making the decision to switch on the alarm is an important parameter for defensive software.

By default, the alarm counter must be set to 3 for asserting the external alarm. The sensor variation limit is set higher than the ambient noise, but lower than fluctuations due to electromagnetic interference.

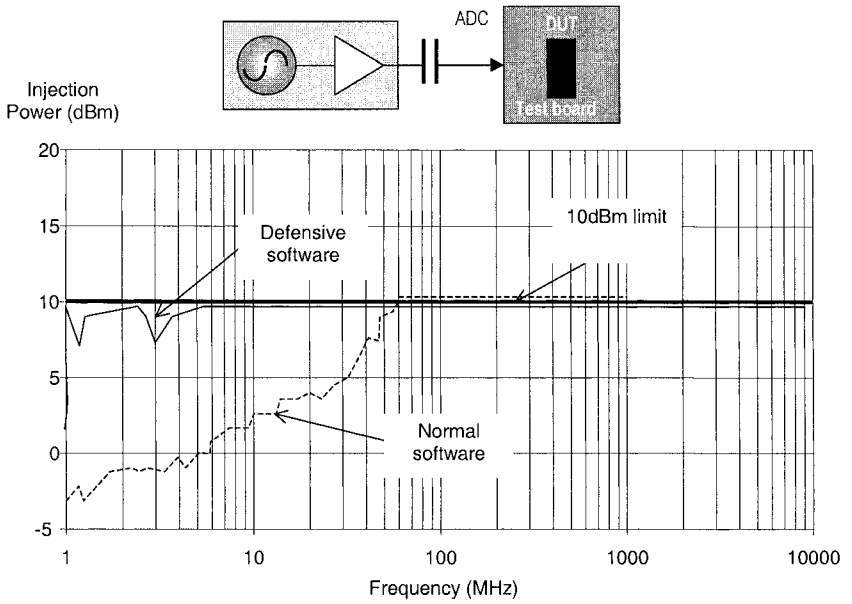


Figure 7-36. Wrong alarm setting with and without defensive software

2.4.3 Measurements

Fig. 7-36 illustrates the comparison between results of the standard and defensive software performances. The X-axis corresponds to the interference frequency, while the Y-axis is related to the incident disturbance power. This measurement (Baffreau, 2002) clearly demonstrates the low-pass behavior of the IC. Near 1 MHz, a fraction of milli-watt is enough to switch a wrong alarm on the device.

The defensive software proves to be effective on the whole frequency range. However, for some frequencies that are multiples or submultiples of the IC clock frequency, the defensive software shows some weaknesses. This can be related to the fact that the analog-to-digital converter clock is directly derived from the microcontroller clock.

However, the latency time to make a decision has been increased. Consequently, the defensive software parameters such as the alarm count should be fitted to the application time constraints to avoid degrading its functionality. In the default software, the latency time is around 90 µs, and rises to nearly 300 µs for the defensive software version, which is easily tolerable for a temperature alarm.

Table 7-1. Compared performances of conventional and defensive software

Software	Memory space (Bytes)	Execution time (Clock cycles)
Conventional software	88	83
Defensive software	202	123

The sensor limit detection combined with the sensor variation detection and the alarm count, although delicate to configure, prove to be very efficient at increasing the embedded system immunity against electromagnetic interferences. The defensive software requires additional memory space and additional execution time, as reported in Table 7-1. The memory space is more than doubled, while the execution time is slowed down by nearly 50%.

This memory overhead could doubtless be unacceptable for some embedded applications with severe memory constraints. However, with further technology progress, the addition of a few hundred bytes of code is could become acceptable.

As most embedded software is compiled from a C language description, optimization may help to free some memory space for defensive routines. Considering the execution time increase, the execution difference between the software versions is quite small, although a significant latency delay deso exist for asserting a valid alarm in the case of defensive software.

2.4.4 Discussion

The effectiveness of defensive software to protect programmable ICs against radio frequency disturbances is strongly dependent on the application, the type of data exchange, and the disturbance level that the device undergoes.

The defensive software has proven very effective for managing low amplitude analog with low to medium interference level. However, in the case of more powerful disturbance, the detection software might stop working properly. Thus, hardware-based recovery mechanisms such as watchdogs, nonvolatile memory, and redundant storage of the most crucial data might help to handle this type of interference.

2.5 Improved Immunity by Design

Operational amplifiers, like most analog integrated circuits, are extremely susceptible to EMI, which are conveyed into integrated circuits through wires, PCB traces and IC package interconnections.

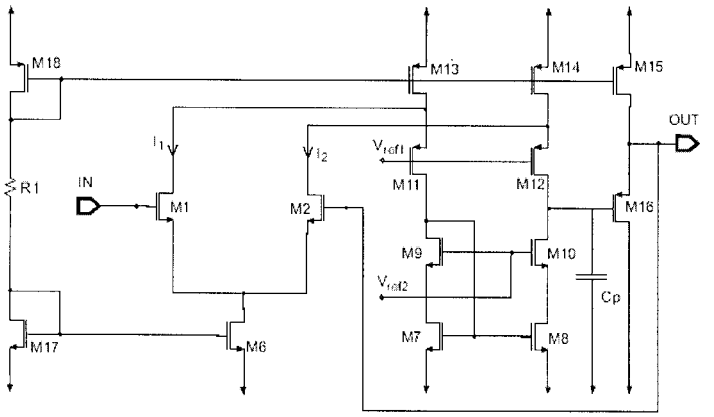


Figure 7-37. Schematic diagram of a conventional feedback operational amplifier

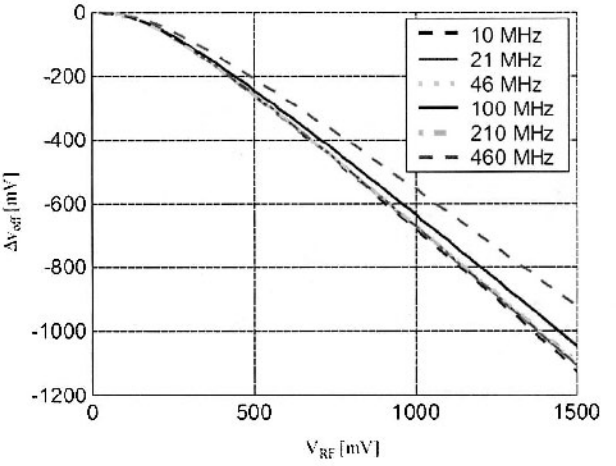


Figure 7-38. Voltage follower susceptibility to EMI: output offset voltage vs. interference amplitude

Once added to nominal signals, radio frequency interference (RFI) propagates all over the integrated circuit (metal interconnections and silicon substrate) reaching active components like bipolar and MOS transistors, where it excites their nonlinear operation (Masetti, 1996). Because of RFI-induced inter-modulation products with frequency within the circuit bandwidth, nominal signals cannot be recovered and failures in the system operation are induced.

For instance, a CW RFI added to the DC input voltage (the nominal input signal) of a feedback CMOS operational amplifier, like that shown in Fig. 7-37, generates an output offset voltage whose magnitude depends on the interfering signal amplitude and frequency, as it is shown in Fig. 7-38.

Although all the transistors of an operational amplifier are excited by RFI, only those of the input differential stage significantly contribute to the output voltage, because in-band inter-modulation products generated within the first stage of the operational amplifier are strongly amplified by the following stages. Consequently, guidelines focus on the reduction of RFI-induced distortion phenomena in differential pairs.

On the basis of models such as those proposed in (Fiori, 2003), the operational amplifier susceptibility to EMI can be significantly reduced by a careful selection of the differential pair design, aspect ratio and the bias current magnitude. From the simulation trend shown in Fig. 7-39, it can be seen that the input offset tends to decrease with the bias current increase, which leads to an improved immunity to RFI.

Finally, it has been shown in (Fiori, 2001) that the immunity of operational amplifiers to RFI can be significantly increased by using proper circuit topologies of the input differential pair, like that shown in Fig. 7-40.

In this case, a double differential pair replaces the differential pair of the folded-cascode operational amplifier. The output current of the pair M3-M4 is modulated only by the input signals with a frequency higher than the high-pass CR cut-off frequency.

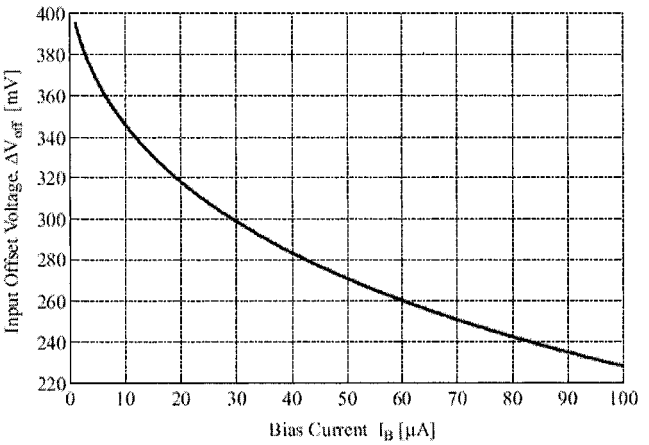


Figure 7-39. Offset variation vs. Bias current *Ib*.

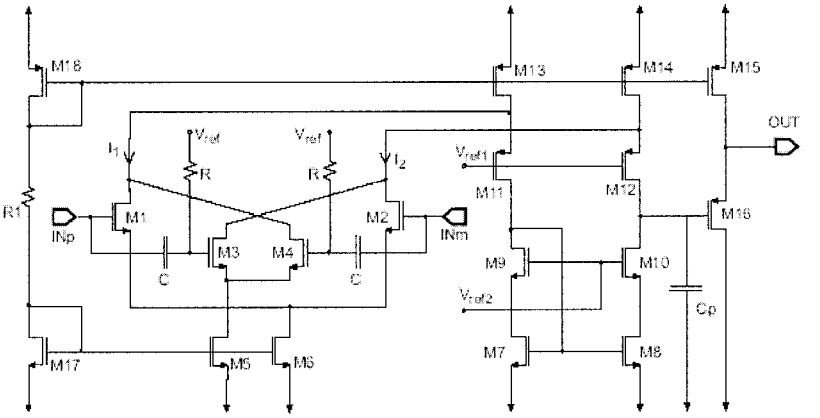


Figure 7-40. Folded-cascode operational amplifier with a double differential pair immune to EMI.

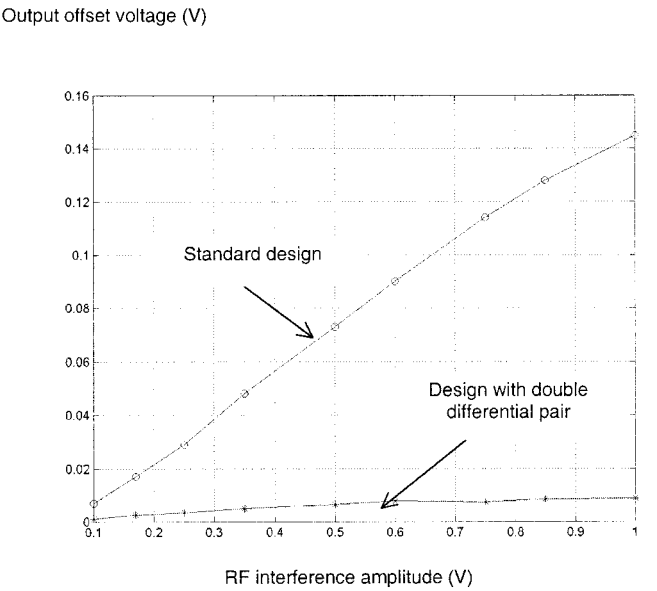


Figure 7-41. Output offset voltage versus RF interference amplitude for interference frequency of 100 MHz.

Thus, the overall output differential current consists of the difference between the in-band intermodulation products of M1-M2 and that of M3-M4. As a result, the demodulation of RFI in the operational amplifier input stage is minimized. To this purpose, Fig. 7-41 shows that the EMI-induced offset voltage with the circuit configuration of Fig. 7-40 is reduced of about a factor of ten. Circles refers to the standard folded-cascode, while crosses refer to the folded-cascode that include a double differential pair.

3. CONCLUSION

In this section, a brief review of design guidelines for achieving low parasitic emission and high immunity to radio-frequency interference at integrated circuit level has been presented. The guidelines may be applied at various levels of the IC structure: on-chip decoupling capacitance, VDD/VSS supply network, and functional architecture. The potentials offered by asynchronous design have also been investigated, with focus on de-synchronizing digital architectures which significantly lower the internal current spectrum peak magnitude. From an immunity point of view, an efficient design technique has been presented that applies to analog operational amplifiers.

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Appendix A

USEFUL TABLES

1. CONVERSION TABLES

$$V_{dB} = 20.\log(V)$$

Table A-1. Conversion between dB and Voltage-Current ratio

dB	Voltage or current ratio
120	10^6
100	10^5
80	10^4
60	1000
40	100
30	31.6
20	10
10	3.16
6	2.0
3	1.412
0	1.0
-3	0.708
-6	0.5
-10	0.316
-20	0.1
-40	0.01
-60	0.001
-80	10^{-4}
-100	10^{-5}

$$V_{dBuV} = 20.\log(V.10^6)$$

Table A-2. Conversion between dBμV and Voltage ratio

dBμV	Voltage ratio
120	1 V
100	100 mV
80	10 mV
60	1 mV
40	100 μV
30	31.6μV
20	10 μV
10	3.16 μV
0	1 μV
-10	0.316 μV
-20	0.1 μV

$$P_{dBm} = 10.\log\left(P.10^{3}\right)$$

P = power (Watt)

P_{dBm}= power in dB milli-watt (dBm)

Table A-3. Conversion between dBm and Watt

dBm	Watt
120	1 GW (Giga-watt, 10^9)
90	1 MW (Mega-watt, 10^6)
60	1 KW (Kilo-watt, 10^3)
40	10 W
30	1 W
20	0.1 W
10	10 mW
0	1 mW
-10	0.1 mW
-20	0.01 mW

2. INDUCTANCE VS. FREQUENCY

$$\left|Z_L\right| = 2\pi.f.L \qquad \text{(A-1)}$$

f= frequency (Hz)

L=inductance (Henry)

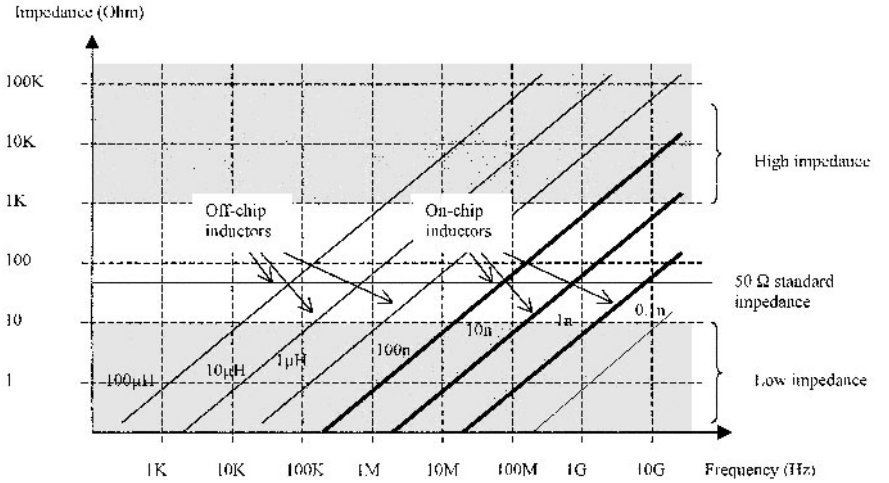

Figure A-1. Inductance impedance vs. frequency.

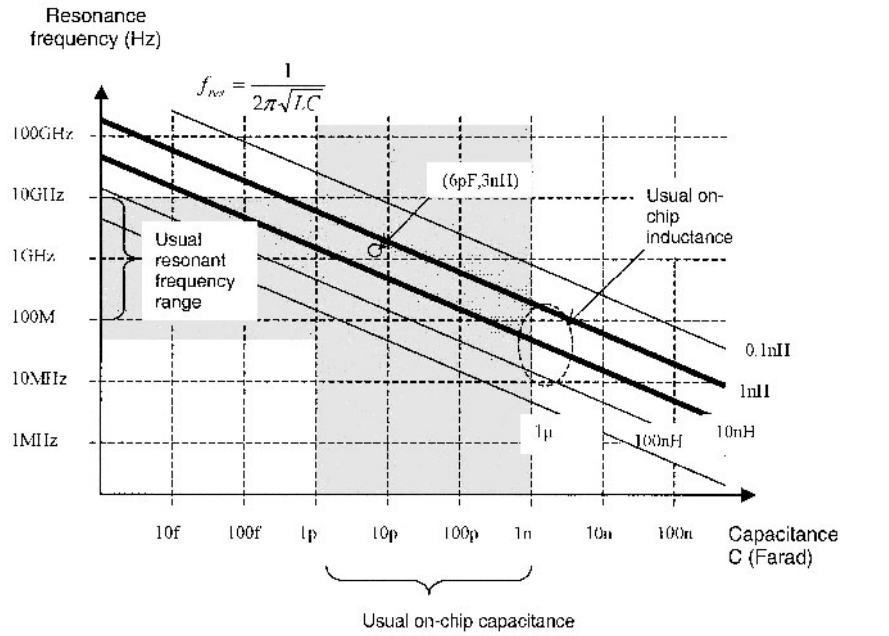

Figure A-2. Relationship between usual capacitance, inductance and resonant frequency.

3. RESONANT FREQUENCY

$$f_r = \frac{1}{2\pi\sqrt{L.C}} \qquad \text{(A-2)}$$

fr= resonant frequency (Hz)
L=inductance (Henry)
C=capacitance (Farad)

4. RELATION BETWEEN FREQUENCY AND ANTENNA EFFECT

$$\lambda = \frac{c}{f\sqrt{\varepsilon_r}} \qquad \text{(A-3)}$$

λ=wavelength (m)
f= wave frequency (Hz)
c=speed of light (m/s)
ε_r=relative permittivity

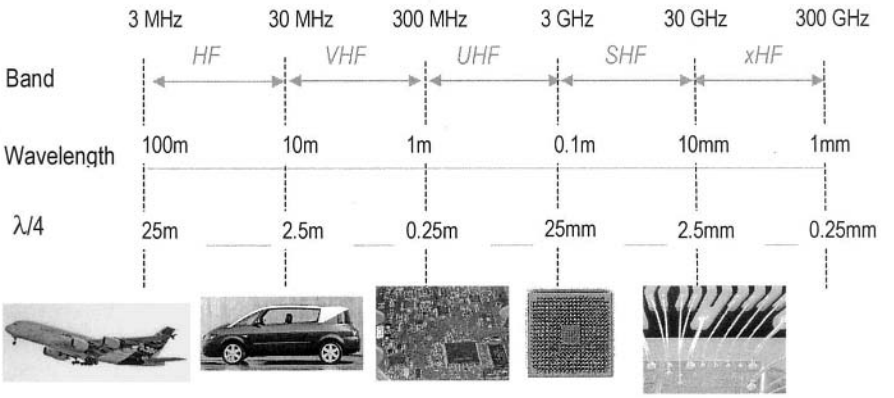

Figure A-3. Link between the frequency and optimum antenna size.

HF = High Frequencies, VHF = Very high frequencies
UHF = Ultra high frequencies, SHF = Super high frequencies
xHF = Extremely high frequencies, THF = Tremendously high frequencies

5. ELECTRIC FIELD VS. POWER

$$E \approx \frac{\sqrt{Z_C.P}}{d} \qquad \text{(A-4)}$$

E= Electric Field in V/m
P = Source power (Watt)
Zc = Characteristic impedance of the line connected to the power source
d = distance from Antenna in meters

Table A-4. Electric field vs. distance and power for Zc=50Ω

Power/Distance	1mm	1cm	10cm	1m	3m
1μW	7.07 V/m	0.707	0.07	0.007	0.0007
1mW	223	22.3	2.23	0.223	0.022
1W	7071	707.1	70.7	7.07	2.35
10W	22360	2236	223.6	22.36	7.45
100W	70710	7071	707.1	70.7	23.57

6. VOLT/METER, AMPERE/METER

In far field conditions:

Table A-5. Conversion between magnetic, electric field and power density

1 A/m	= 377 V/m
1 A/m	= 25.8 dBW/m^2
1 V/m	= 0.00265 A/m
1 V/m	= -25.7 dBW/m^2
1 W/m^2	= 19.4 V/m
1 W/m^2	= 0.0515 A/m

7. METERS AND INCHES

Table A-6. Correspondence between meters and inches

1 meter	= 39.37 inches
1 inch	= 25.4 mm
1 inch	= 1000 mil

8. USEFUL CONSTANTS

$$\varepsilon_0 = \frac{1}{36\pi.10^9} \approx 8.8419 pF/m$$

$$\mu_0 = 4\pi.10^{-7} \approx 1.256 \mu H/m$$

Appendix B

COMPANION CD-ROM

EMC-related tools

The companion CD-ROM includes a training course on EMC applied to integrated circuits and a selection of EMC-related tools. It also includes useful links to interesting tools that have been applied successfully to the simulation of EMC effects at integrated circuit level. The appendix gives a short description of each of these tools.

1. GETTING STARTED

- Insert the CD-ROM
- With your Web browser, double-click "Index.html"

The following screen appears.

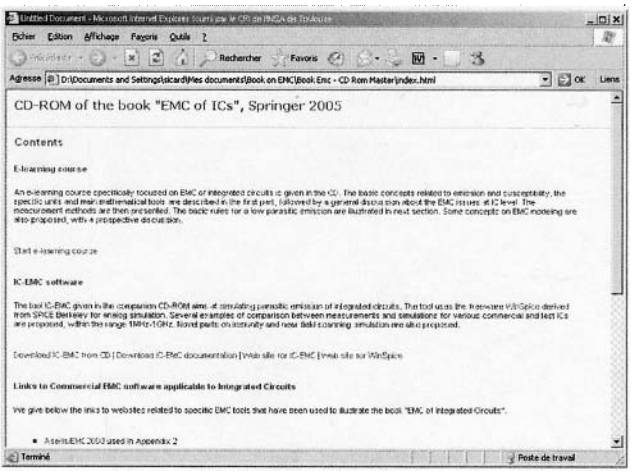

Figure B-1. Welcome menu of the companion CD-ROM.

2. E-LEARNING COURSE

An e-learning course specifically focused on integrated circuits EMC is proposed in the companion CD-ROM. The e-learning course has been written by Ben Dhia (2004).

A screen example is given in Fig. B-2. The course contents are summarized in Table B-1. The basic concepts related to emission and susceptibility, the specific units and main mathematical tools are described in the first part, followed by a general discussion about the EMC issues at IC level.

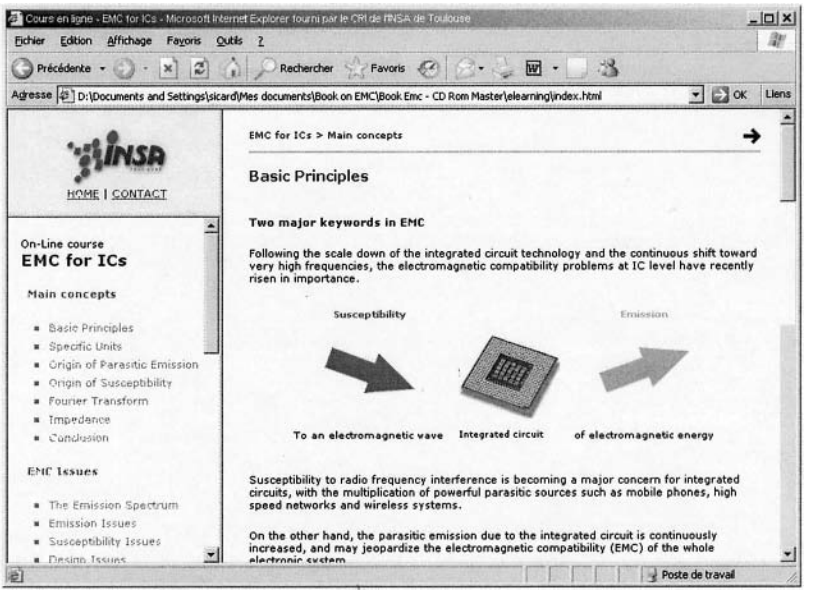

Figure B-2. E-learning course in EMC of ICs

Table B-1. e-learning course outlines

Chapter Title	Contents
Main concepts	Basic principles, specific units, origin of parasitic emission, origin of susceptibility, Fourier transform, impedance
EMC Issues	The Emission spectrum, emission issues, susceptibility issues, design Issues
Measurement Methods	VDE 1/150Ω, TEM, GTEM, BCI, DPI, scan, WBFC
IC Floorplan	Golden rules for low Emission, on-chip decoupling, case study
Models for EMC Simulation	Models: what for? Macro-model of an IC, package models, correlation measurement/simulation, future of EMC models

The measurement methods are then presented. The basic rules for a low parasitic emission are illustrated in the next section. Some concepts on EMC modeling are also proposed, with a prospective discussion.

3. IC-EMC SOFTWARE

The tool IC-EMC (Sicard, 2004) given in the companion CD-ROM aims at simulating parasitic emissions of integrated circuits. The tool uses the freeware WinSpice (Smith, 2004) derived from SPICE Berkeley for analog simulation. Several examples of comparison between measurements and simulations for various commercial and test ICs are proposed, within the range 1 MHz-1 GHz. Novel parts on immunity and near field scanning simulation are also proposed. The global flow for using IC-EMC and WinSpice is outlined in Fig. B-3.

The latest version of the IC-EMC software may be downloaded from www.ic-emc.org. The analog simulation tool WinSPICE may be downloaded from www.winspice.com.

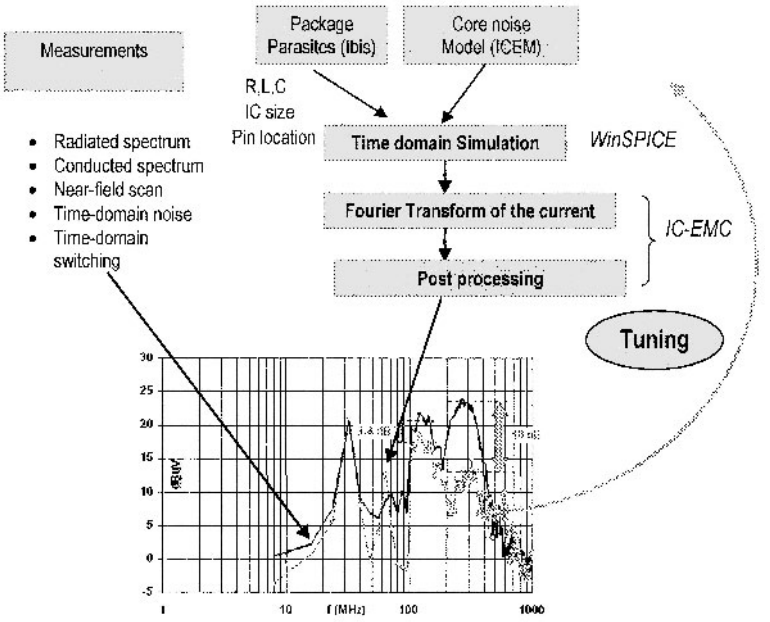

Figure B-3. EMC simulation flow using IC-EMC and Winspice

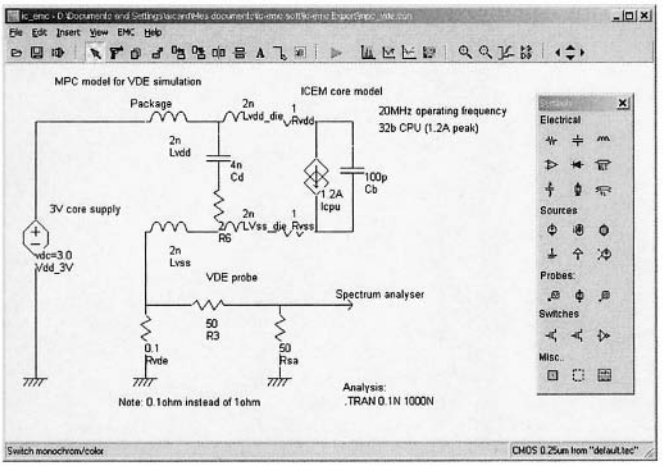

Figure B-4. The IC-EMC initial screen with a 32-bit micro-controller model.

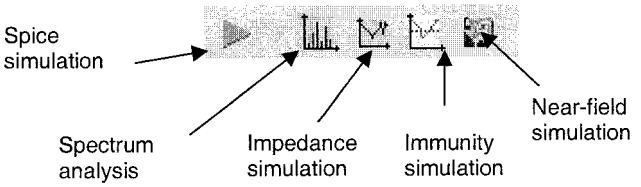

Figure B-5. Access to the main simulation tools in IC-EMC.

3.1 Getting started

The main screen of the schematic editor is shown in Fig. B-4. The editor contains a palette of symbols (Window "Symbol Library" situated on the right of the screen) as well as some basic editing icons to build the schematic diagram of the circuit. The R,L,C components may be found in the "Advanced" index of the symbol library.

The main commands of the tool are shown in Fig. B-5. From left to right, the Spice simulation icon translates the schematic diagram into a SPICE-compatible text file, the other icons give access to the emission spectrum window, the impedance vs. frequency, the immunity simulation screen, and the near-field simulation screen.

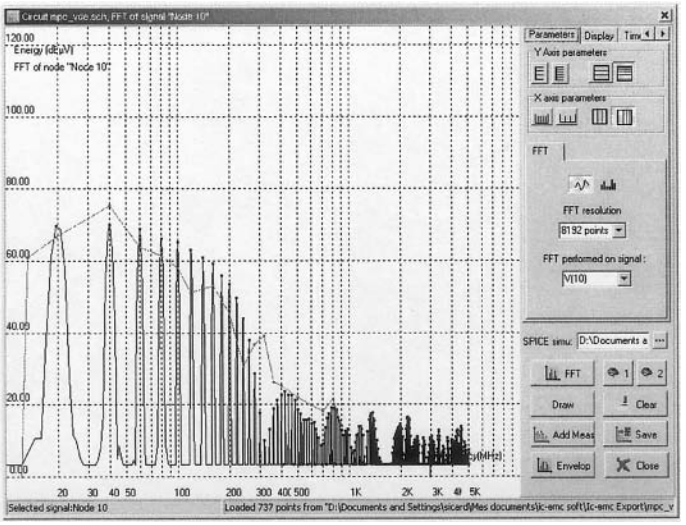

Figure B-6. Comparison between measured and conducted emission of the MPC processor.

3.2 Conducted Mode Simulation and comparison with Measurements

The schematic diagram is converted into a SPICE-compatible text file. The voltage waveform computed by the analog simulator WinSpice is translated into frequency domain by a Fast Fourier Transform (FFT). The X axis covers the range 10-1000 MHz in logarithmic scale. The representation of the energy on the Y axis is in dBµV.

The spectrum appears as shown in the Fig. B-6. Measurements are superimposed to the simulation for comparison purpose. The case-study proposed in Fig. B-6 concerns a 32-bit micro-controller for automotive applications. Comparisons between measurements and simulation are also proposed in the IC-EMC package for several other conducted-mode test cases, as well as for radiated-mode emission.

3.3 Other features

In IC-EMC, specific tools are also provided for various aspects of integrated circuit characterization, as well as simple screens to ease data conversion and resonant frequency evaluation. The EMC menu is detailed in Fig. B-7.

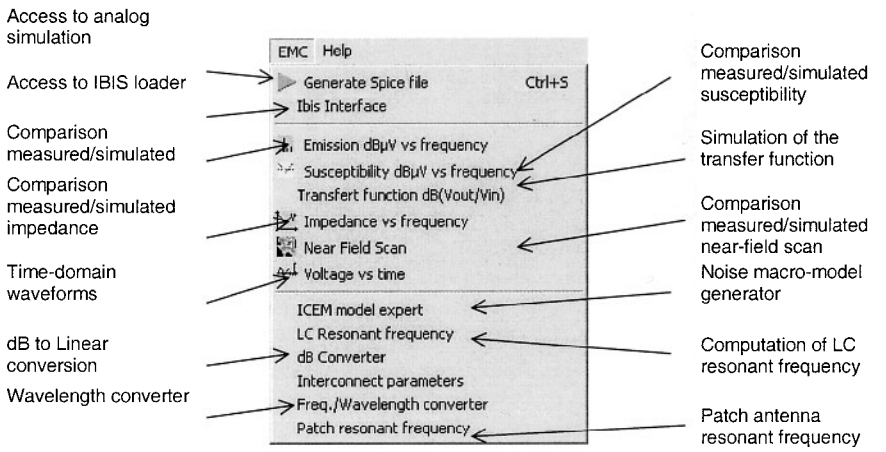

Figure B-7. The EMC menu provides access to a large set of tools to ease simulation/measurement comparison.

4. FEKO

The name FEKO is an abbreviation derived from the German phrase **Fe***ldberechnung bei* ***K****örpern mit beblieger mit beliebiger* **O***berfläche.* (*Field computations involving bodies of arbitrary shape*). As its name suggests, FEKO can be used for various types of electromagnetic field analyses involving objects of arbitrary shapes. This software is developed by EM Software and Systems [1]. It runs under Windows and Linux environment.

FEKO is a computer code dedicated to solve electromagnetic problems as antenna design, antenna placement, shielding, micro strip circuits, scattering problems with metallic or dielectric structures.

4.1 Presentation of the solver FEKO

The program FEKO provides a resolution of Maxwell's equations in the frequency domain for structures with a surfaced mesh and for dielectric objects with a mesh in volume. It is based on the *Method of Moments* (MoM) which computes the electric surface currents on conducting surfaces and equivalent electric and magnetic surface currents on the surface of a dielectric solid to obtain electromagnetic fields.

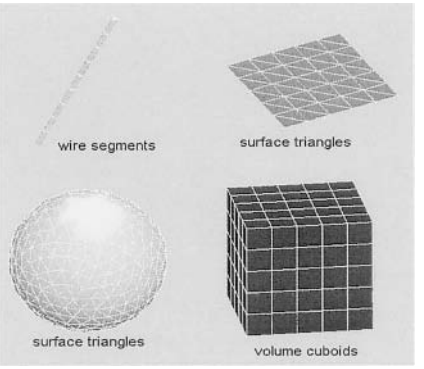

Figure B-8. Meshed geometry in FEKO (wire segments, surface triangles and volume cuboids).

Surface currents are obtained by solving a linear system: $[Z]\times[I]=[V]$, where [I] is the unknown matrix of surface currents, [Z] represents the impedance matrix or interaction matrix which is computed from the meshed geometry and describes interactions between each element of the meshed model (or basis functions).

The model can be composed of geometric elements such as wire segments, surface triangles and volume cuboids (Fig. B-8). The vector [V] is the vector of excitations and depends on incident fields and voltage, current or power sources.

The formulation of the MoM in FEKO permits the resolution of fields in electromagnetic problems with:

- Metallic structures,
- Planar Green functions for planar multilayered media,
- Surface and volume integral formulations for the treatment of dielectric bodies,
- Dielectric coated wires,
- Thin dielectric sheets,
- Real or ideal ground planes,
- Spherical Green's functions for special spherical problems.

The knowledge of the current distribution allows to obtain near fields, far fields, radar cross sections, directivities, input impedances of antennas, S parameters, VSWR calculations, radiated power and Specific Absorption Rate in a loss dielectric.

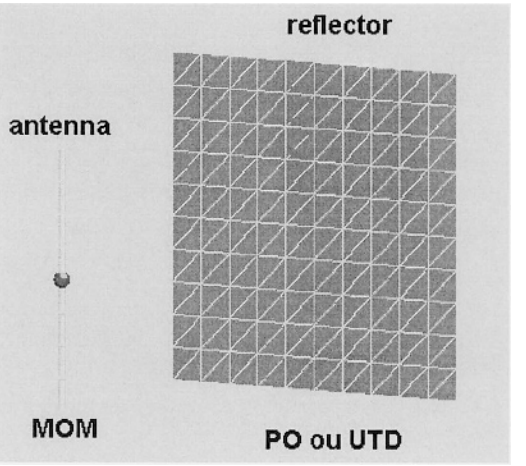

Figure B-9. Resolution of reflector problems with an hybrid method.

4.2 Hybridization of the method of moments

Very large electromagnetic problems require enormous computational resources in term of memory and computational time, because the dimensions of structures are larger than the wavelength. To solve them, some asymptotic techniques exist like the Physical Optics (PO) approximation or the Uniform Theory of Diffraction (UTD) which both perform high frequency approximation. In FEKO, an hybrid approach between MoM and PO or between MoM and UTD has been developed, this hybridization is made at the level of the interaction matrix.

Physical optic approximation and UTD are well adapted for problems like antennas in front of large reflecting structures. In this kind of problems, antenna structures are defined with MoM and the reflecting surface with PO approximation or UTD, as illustrated by Fig. B-9. Surface current is computed on each triangle of PO surfaces thanks to a simple formulation of currents.

With UTD, the size of structures does not influence computational resources since only reflection point, diffraction from edges and corners, and creeping waves are accounted for. All of them are calculated from a ray-tracing algorithm on the model. UTD formulations apply on non-meshed models.

The computation time depends only on the number and the type of ray interactions. However, for the current version of FEKO, hybrid method MOM/UTD can apply only on polygon plates or on cylinders.

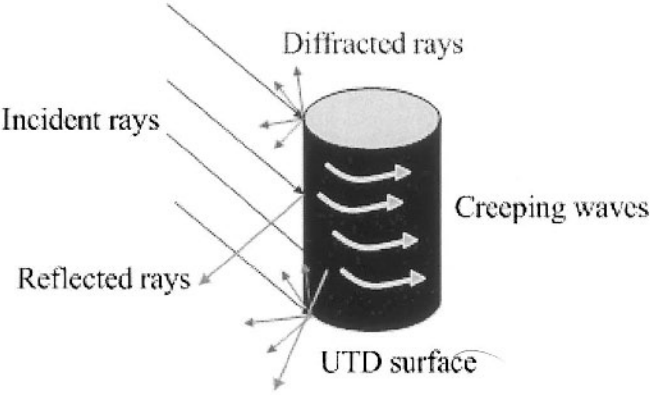

Figure B-10. Resolution with hybrid UTD/MOM.

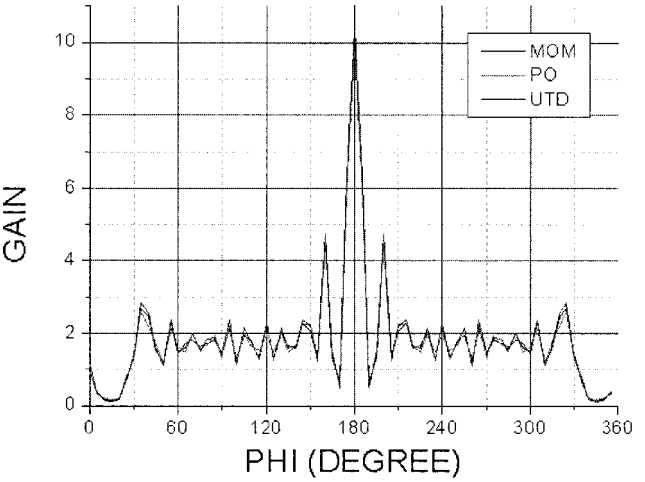

Figure B-11. Comparison of MoM, PO and UTD results on a rectangular reflector case.

FEKO offers a visualization of all the rays, which permits a physical analysis of the problem. Fig. B-10 shows all the rays radiated from a source placed in front of the reflector and diffracted by its corners.

Table B-2. Comparison of CPU time between the 3 methods

Methods	**CPU time (s)**
MoM	4186
PO	2
UTD	0.36

The classical case of a dipole in front of a rectangular reflector is illustrated in Fig. B-11, with a model meshed with 4418 triangles. The far field and the gain are computed in the three following cases: the reflector is defined with MoM, PO or UTD. Fig. B-11 shows the comparison between the three cases and it is obvious that the three methods give the same result. However, an important decrease of computational time is achieved in with both PO and UTD as Table B-2 shown. In a recent update of FEKO, a new hybrid method has been introduced: the FEM/MoM hybrid. It allows the modeling of sub-regions of a model with FEM (Finite Elements Method) and other regions with the MoM.

Since FEKO version 4.2, a multi-level fast multipole method has been included, with significant memory size reduction. Contrary to PO approximation and UTD, it is a rigorous technique not based on specific high frequency approximations and has no restricted domain of validity.

4.3 Organization of FEKO

FEKO consists of several interfaces dedicated to specific functions. The first step to start a project is the definition of the geometry of the model and of its surface mesh. FEKO offers two different ways to define meshed models. Firstly, CadFEKO allows the creation and set up of FEKO models in a CAD environment. CadFEKO is only used for the geometry, meshing phase and specification of dielectric properties of the different regions, but is not used to define solution requirements. This action is carried out under EditFEKO. CadFEKO supports parametric model construction.

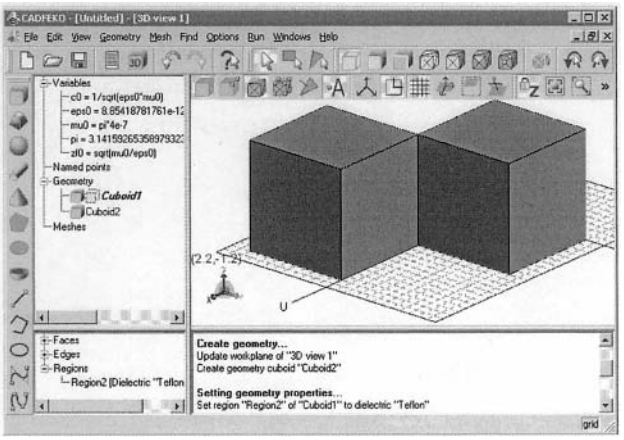

Figure B-12. The CAD interface CADFEKO.

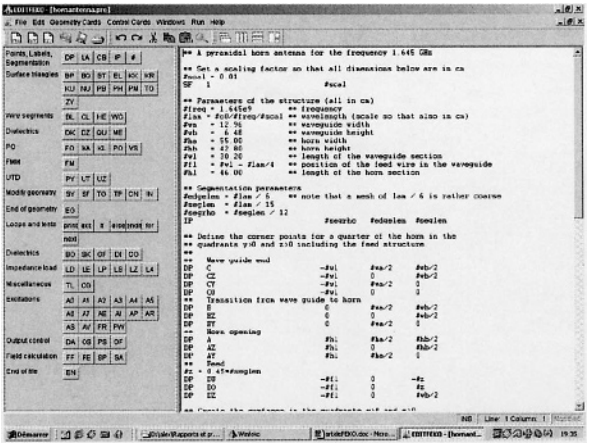

Figure B-13. The text editor EditFEKO.

Indeed it allows the definition of symbolic variables which can be computed with mathematical functions and expressions to construct the model. If the variables are changed, all the model is changed. It is particularly useful if an antenna size must be tuned for a required frequency or input impedance. CadFEKO allows to define complex meshing since it permits to define local mesh refinement and to adapt the size of the mesh. Fig. B-12 shows the main interface of CadFEKO which includes:

- a 3D window area which displays the 3D views,
- a main menu and the toolbars to define projects, to create and modify geometry, meshing or properties, to modify the view,
- a tree view which gives information about geometry, variables and properties,
- a message window which displays messages about user interaction such as geometry creation and error messages.

Secondly, the geometry can also be created thanks to the text editor EditFEKO (Fig. B-13). The interface of EditFEKO helps the user to write an a standard ASCII input file of geometry, mesh, and properties as well as solution requirements (definition of sources, impedances, and desired calculation description) thanks to a lot of cards which control a certain number of parameters and commands.

Just like CadFEKO, EditFEKO supports parametric geometry. In addition, it is possible to create loops that make it possible to write some advanced algorithms. The preprocessor/mesher PreFEKO creates meshed geometry and allows the direct importation of meshed geometry in FEMAP neutral, NASTRAN, PATRAN, AutoCAD *dxf*, STL or ANSYS *cdb* formats.

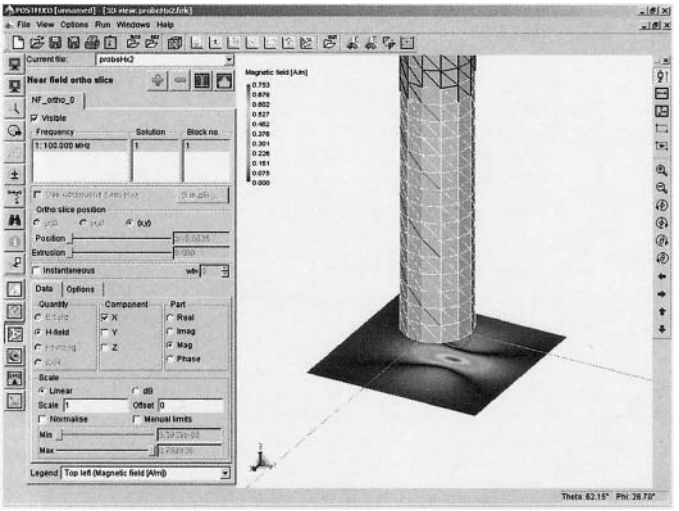

Figure B-14. Visualization of 3D near field results on PostFEKO interface.

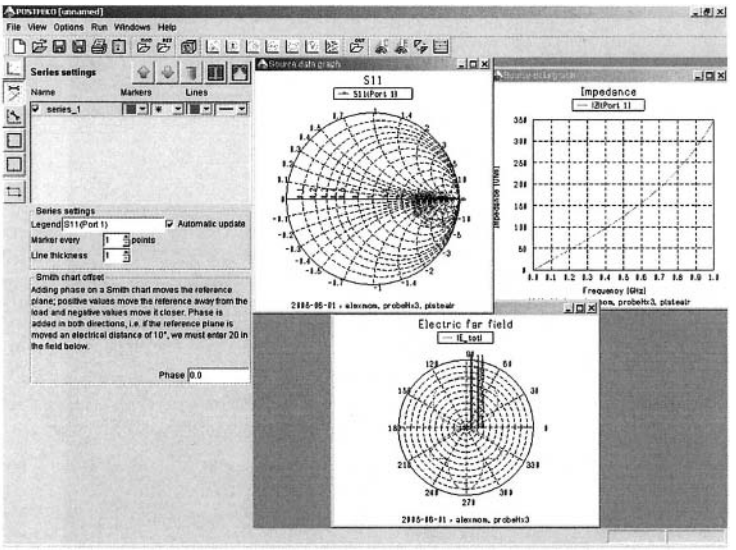

Figure B-15. Visualization of 2D results on PostFEKO interface.

After preprocessing operation, the meshed model can be visualized under PostFEKO. PostFEKO is the validation display of the model and the post processing interface. It allows multiple 3D views with multiple geometry and result files in a single session. The solver FEKO that can be launched either by EditFEO or by PostFEKO performs all computations. All the solutions are contained in an output file created by FEKO.

Results like currents, near or far fields, specific absorption rate and UTD rays can be displayed on 3D over the model, as we can see on Fig. B-14.

PostFEKO (Fig. B-15) is also used to visualize in 2D graphs results such as far or near fields, currents, S parameters, input impedance and admittance, radiated power, gain, directivity, Radar Cross Section, Specific Absorption Rate... in linear or logarithmic scale, polar or Smith charts.

4.4 Special modules of FEKO

FEKO offers several special modules. First, TimeFEKO solves electromagnetic problems in time domain. It uses the solver FEKO that computes solutions in frequency domain and transforms them into time domain with a inverse FFT algorithm, when transient pulses are applied. TimeFEKO uses 2 types of files:

- the input file for PreFEKO where the frequency is defined.
- the definition file for the pulse, the highest frequency and the number of samples.

Several pulse forms are available: Gaussian, triangle, double exponential, ramp pulse and double exponential impulse. Let's take the case of a micro strip on a substrate planar layer. A voltage source is applied on this line with a ramp pulse of 20 ns and 1 V of amplitude. The line is ended with a load resistance (Fig. B-16). We measure current on the line when this line is adapted and non-adapted (Fig. B-17).

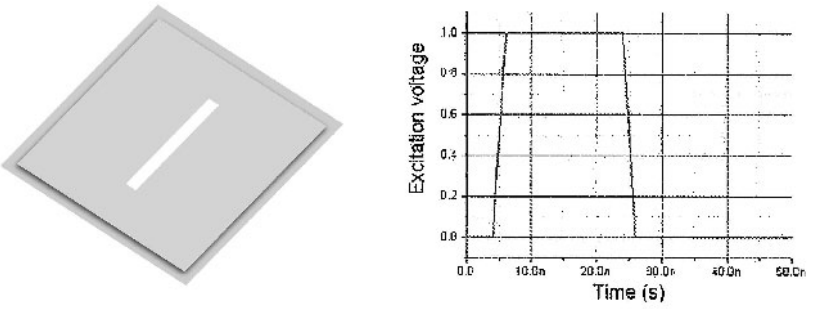

Figure B-16. Micro strip with a ramp pulse voltage source.

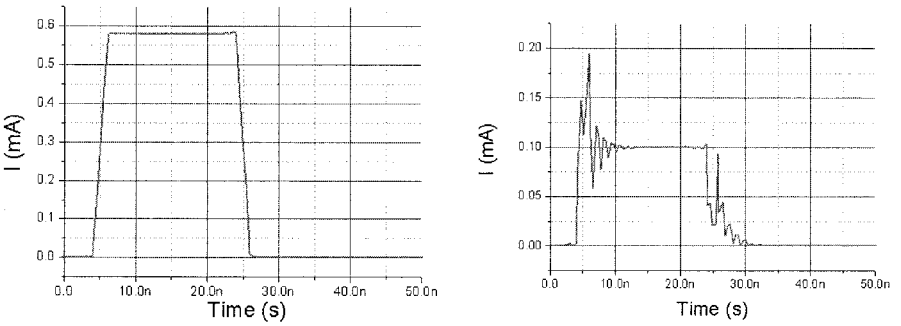

Figure B-17. Current on the line with adapted (left) and non-adapted load (right).

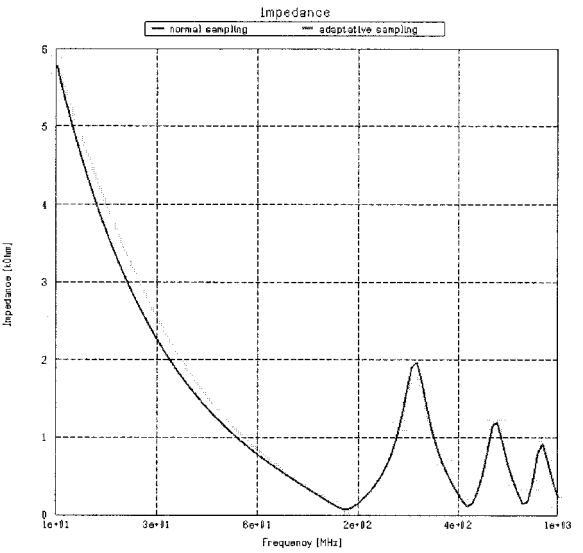

Figure B-18. Computation of *Zin* with discrete frequency sampling and continuous frequency sampling.

Next, a module called AdaptFEKO makes an adaptative frequency sampling interpolation and gives a continuous sampling of frequencies. Indeed, for a very wide band of frequencies with narrow resonances, it is difficult to have a good resolution on resonances without increasing the number of frequency samples dramatically. The adaptive frequency sample technique of AdaptFEKO automatically selects sample points, using smaller steps near resonances and larger steps where the behavior is quite smooth, and then carries out the interpolation.

Fig. B-18 shows the comparison between a discrete frequency sampling (normal sampling, for each specified frequency a computation is made) and a continuous frequency sampling with AdaptFEKO. The input impedance *Zin* of a dipole antenna is computed. In this example, adaptive frequency sampling requires 10 samples whereas normal frequency requires 100 samples.

OptFEKO can optimize gain/directivity of antenna, radiation pattern, RCS, omni directivity, impedance/ reflection factor, resonance and near fields. OptFEKO uses several predefined optimization algorithms : discrete points, simplex methods, the conjugate gradient method and the quasi Newton method.

5. VHDL-AMS SOFTWARE : AN OVERVIEW

Several commercial tools supporting the use of the VHDL-AMS language may be used for EMC simulation at integrated circuit level.

- ADVance-MS© [1] and SystemVision© [2] from Mentor Graphics©
- Simplorer© [3] from Ansoft©
- Smash© [4] from Dolphin Integration©
- Auriga© [5] from FTL Systems©

Feature-limited evaluation versions of these tools are downloadable for free and are often powerful enough for basic EMC modeling. In addition to the evaluation versions quoted above, VHDL-AMS simulation freeware is also available. The most advanced products are :

- hAMSter© [6] from Simec© (the core of which is reused in Simplorer©)
- SIERRA [7] from the University of Cincinnati

5.1 Comparison between SystemVision© and ADVance-MS©

SystemVision© and ADVance-MS© are based on the same simulation core, but with different orientations and features.

ADVance-MS© (ADMS), running on UNIX platforms, is mainly aimed at chip design : it can be interfaced with Mach©, a fast transistor-level simulator. Behavioral models of complex analog and mixed-signal IC blocks can then be validated against transistor-level simulations. ADMS does not include any schematic editor in its standard version; this task is accomplished by the optional Design Architect IC© (DA-IC) product.

SystemVision©'s analog simulator relies exclusively on the Eldo© core. Therefore, only "small" analog blocks can be simulated (less than 1000 devices). Moreover, simulating BSIMx models requires ADMS licenses. However, SystemVision© is easier to use for quick ICEM prototyping and is less expensive, as well.

Both products can be interfaced with ModelSim© which allows the use of the Verilog and SystemC languages in addition to VHDL, VHDL-AMS and C. VHDL-AMS models developed under ADVance-MS© can be reused in SystemVision© without any modification.

5.2 SystemVision© overview

SystemVision© allows the designer to model and simulate a complete industrial system, including almost any physical domain (electronics, mechanics, hydraulics, thermal effects ...). Under SystemVision©, a system is represented graphically by an assembly of functional blocks. Each block of the system may be implemented :

- By a behavioral description written in VHDL, VHDL-AMS or C language,
- By a structural SPICE-based model,
- By a sub-schematic using both kinds of descriptions above.

SystemVision© runs on Windows© 2000 and XP platforms.

Both professional and educational SystemVision© versions have the same features, but the educational version is limited to 30 analog quantities (professional : 1500), 30 analog nodes (1500) and 100 digital signals (3000). However, the latter is suitable for an ICEM model, provided a hierarchical design methodology is used.

5.3 Principle of operation

A SystemVision© model consists of a graphical assembly of several blocks represented by symbols. A symbol may refer either to a language-based model (VHDL, VHDL-AMS, C), a SPICE netlist, or a composite model (another schematic). In order to enable the simulation, all language-based models are first compiled, and the top-level schematic is then "netlisted" into either a VHDL-AMS model or a SPICE netlist depending on the options chosen.

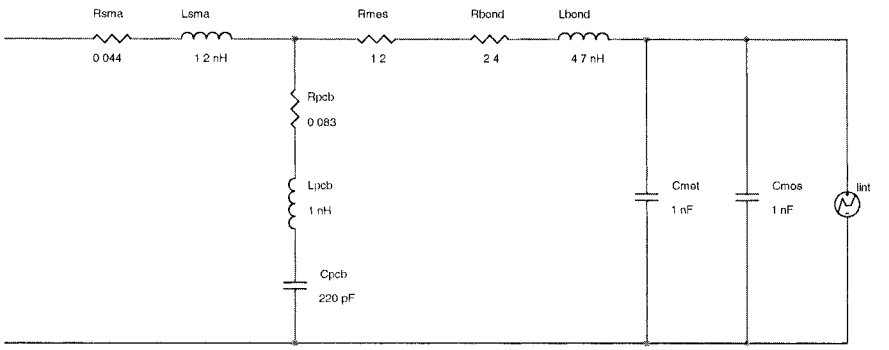

Figure B-19. ICEM model of the VIPER microcontroller.

5.4 Advantages

The main advantage of SystemVision© over "conventional" SPICE-based simulation tools running on Windows© platforms lies in the use of VHDL-AMS for the description of event-driven IC current generators. The whole ICEM-IP methodology can thus be transposed, except for complex transistor-level simulations and comparisons with behavioral models, which still have to be performed with ADVance-MS Mach©.

Once ICEM-IP models have been written, they can be linked together graphically along with passive elements, which makes it easier to build and validate the internal power network of the IC.

5.5 Description of the ICEM model

This illustration is based on the ICEM model of the ATMEL "Viper" 89C51 microcontroller, given in chapter 6. The passive elements of this model, including a measurement resistor, the PCB and the power supply SMA connector, are given in Fig. B-19.

All passive devices will be instantiated as schematic elements, except the MOS capacitance which is included in the current generator model. The current generator is described in VHDL-AMS. The corresponding simulation result is plotted in Fig. B-20. The graph shows the external current in the measurement resistor. The current generator has to be triggered by a 36-MHz digital clock generator.

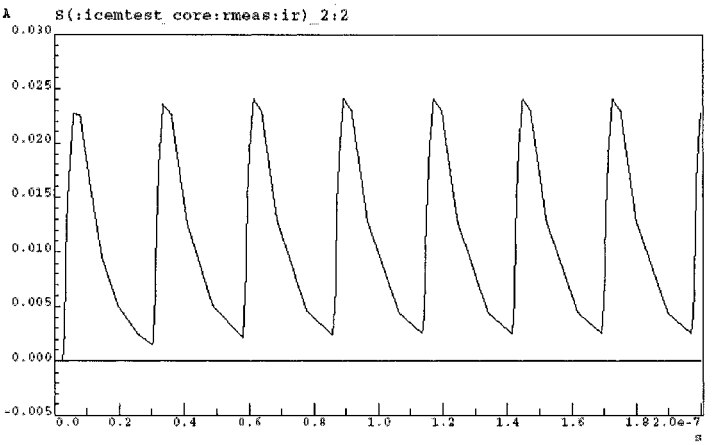

Figure B-20. Simulation of external current flow on the VIPER microcontroller.

A top-level EMC simulation of an integrated circuit is made possible thanks to a VHDL-AMS-based tool. The process can then be reiterated for the other internal blocks and for the I/Os of the IC, leading to the prediction of the global conducted emission.

6. ASERIS-EMC2000

The ASERIS/EMC2000 code (www.aseris-emc2000.com) is a multi-purpose frequency-domain 'exact' code based on a Method of Moment (MoM) for evaluating emission and susceptibility effects between interference sources and 3D objects.

Within the frame of the MEDEA A-408 project, the tool was successfully used for the evaluation of radiated coupling of ICs inside a TEM cell (Fig. B-21). ASERIS-EMC2000 was also successfully used in the European project MEDEA-A509 'MESDIE' for the computation of ICs near-fields, N-port package impedance matrix and high density interconnect couplings.

6.1 Core computation processes

The MoM simulation is based on the so-called electric field integral equation and also includes the magnetic field integral equation to treat arbitrary problems including metallic parts, apertures, dielectric and magnetic materials, ground and symmetry planes etc.

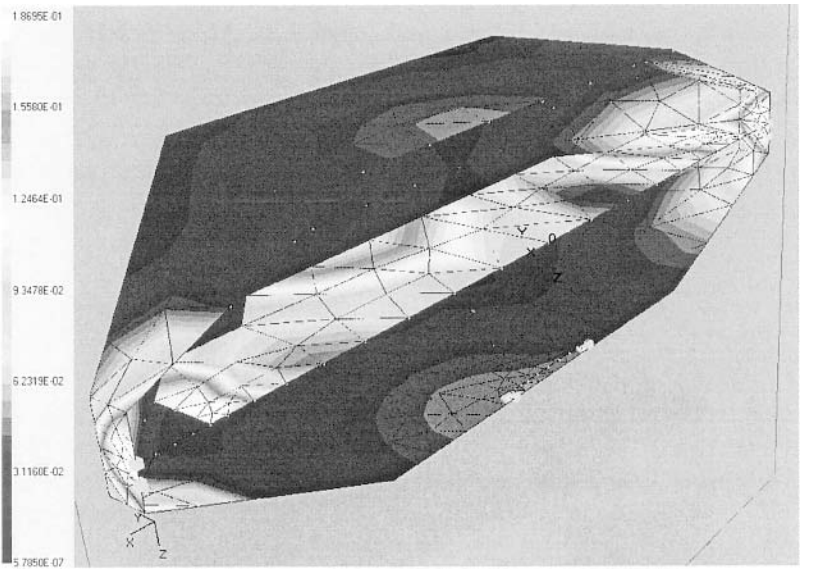

Figure B-21. Example of the surface current and radiated E field (TEM mode) inside a TEM cell due to a wire current representing the noise emitted from an IC, computed with ASERIS/EMC2000.

The simulated geometrical model may consist of :

- Open surfaces such as plates of infinitesimal thickness, which may have various surface impedance properties and may contain apertures,
- Closed surfaces which may contain various dielectric or magnetic, possibly lossy materials,
- Wire structures which may be arbitrarily connected to the surface area and support a wide library of distributed or lumped passive components and sources,
- Ground and symmetry planes.

Surfaces are represented as a set of triangles (patches) and wires as a set of segments. A model can contain an arbitrary combination of wires and surfaces via surface/wire junctions.

Specific functions are used to represent the variation of currents on each element (triangles and segments) which discretize the geometry (surfaces and wires). These functions automatically insure the continuity of current flowing through the involved element.

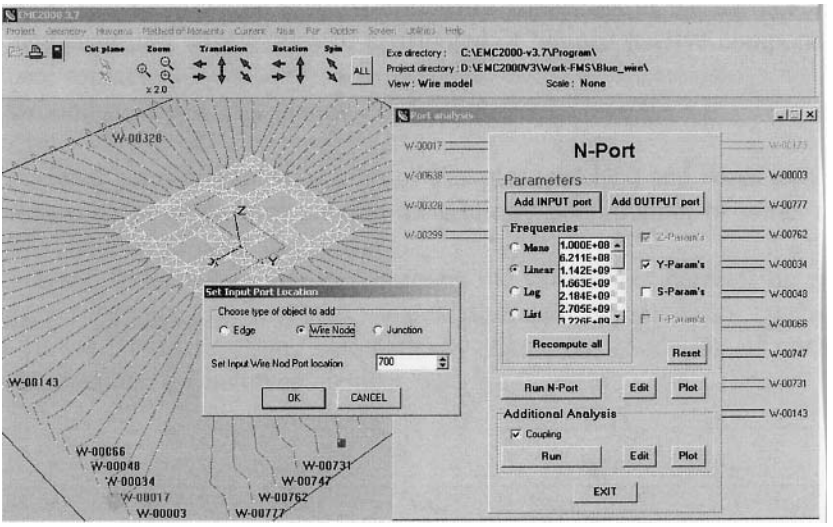

Figure B-22. Interactive port assignation for IC emission simulation.

6.2 User interface

ASERIS/EMC2000 is organized around a menu-driven interface, coupled with a 3D display window (OpenGL). Interactive windows appear when one of the ASERIS/EMC2000 modules is called. ASERIS/EMC2000 is a collection of processes that make it possible to performing an electromagnetic analysis sequentially.

The interactive pre-processing in Method of Moments menu permits definition and placement of a wide variety of material properties and field sources. Sources that are frequency dependent include an impinging plane wave, different types of antennas or conducted sources located on the surfaces or wires of the object. In this last case, sources can incorporate series/parallel internal impedances. In ASERIS/EMC2000, a graphical module has been developed that allows the user to manage the N-port analysis easily. It starts by assigning the port entries in the 3D model interactively. A capture of the screen associated to this procedure is shown on Fig. B-22, applied to a micro-electronic circuit.

Losses may be incorporated as lumped elements or as dielectric coating on metallic conductors. (i.e. resistance, inductance, capacitance or more complex form of the impedance depending on the frequency). Distributed losses are impedances defined on surface and wire elements.

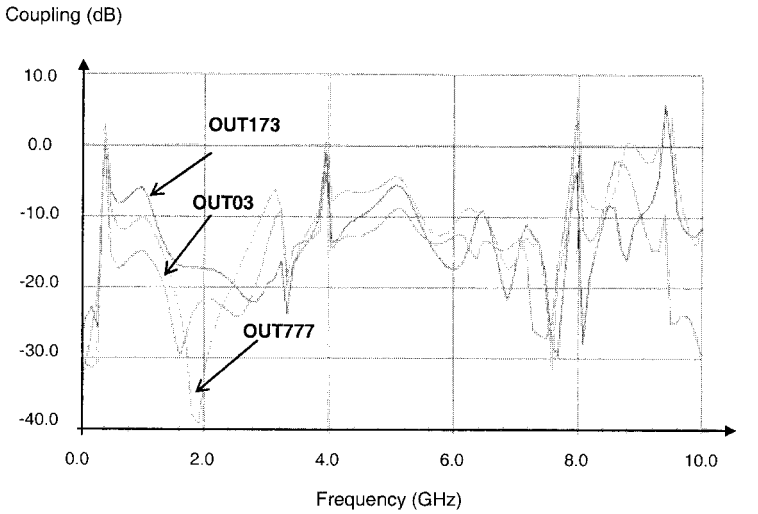

Figure B-23. Simulation of the coupling between ports vs. frequency.

Table B-3. Description of the main commands of ASERIS/EMC2000

EMC2000 menu	**Description**
Project	Manages the creation and loading of projects.
Geometry	Defines/loads the geometrical configuration of the model.
Huygens	Defines electrical parameters and perform the Huygens's analysis.
Method of moments	Defines electrical and computational parameters and perform the MoM analysis.
Current	Performs the current analysis post-processing.
Near	Performs the near field analysis post-processing.
Far	Performs the far field analysis post-processing.
Option	Set miscellaneous parameters, especially for graphical display.
Screen	Sets view angle of 3D models.
Utilities	Plots various 2D format files, define a new color palette, performs the N-port analysis and Ray-tracing operation.
Help	Gets ASERIS/EMC2000 information and on-line HTML Help.

The coupling analysis can then be carried on to obtain the coupling factors between any ports. A click on the port symbol allows to activate an impedance load on the designed port (50 Ω by default). Coupling analysis involves the small Z-port matrix and therefore is performed almost instantaneously, which allows easy parameter analysis by changing active port or loads. A result example is given in Fig. B-23.

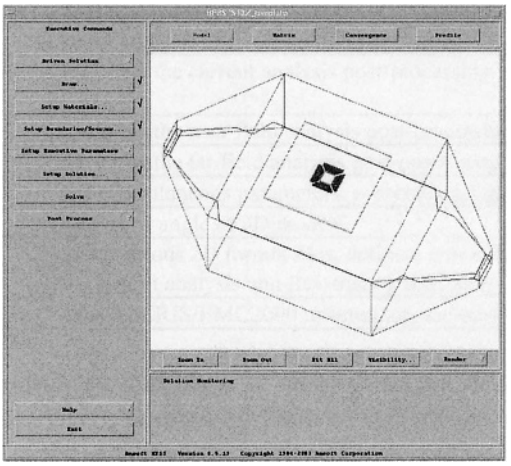

Figure B-24. Main menu window of the HFSS solver version 8.5.

7. HFSS

The High Frequency Structure Simulator (HFSS) from Ansoft is a full-wave electromagnetic field simulator for arbitrary 3D volumetric passive device modeling. Based on the Finite Element Method, the HFSS solver allows to calculate S-parameters, resonant frequency and electromagnetic fields. The tool is used in various research, development and virtual prototyping domains including package modeling, PCB modeling, Silicon/GaAs (inductors and transformers), EMC/EMI, antennas and mobile communications, connectors, waveguides and filters.

7.1 Building an HFSS project

The HFSS software is user-friendly environment that is organized around a main interface window. A picture of the executive window from the version 8.5 is presented in Fig. B-24.

The first sub-menu allows the user to construct the 3D geometry that will be analyzed. The second sub-menu is dedicated to the definition of the materials used in the model: perfect conductors and metals with finite conductivity, dielectric and magnetic materials with possible lossy, anisotropic or non-linear behavior. In the third sub-menu dedicated to surface conditions settings, the user can define excitation and assign boundary conditions, such as perfect electric or magnetic condition, finite

conductivity, impedance, absorbing boundary condition, symmetry plane, etc. In the "setup solution" sub-menu, the user defines the desired frequency range as well as convergence criteria. The computation process is based on the FEM method that consists in meshing the geometrical model into tetrahedral elements, which are each soluble with direct analytical methods. The entire problem is then solved as a matrix of simultaneous equations.

HFSS includes an adaptive meshing algorithm that works as follows. A first simulation is performed with the initial mesh. The areas with strong field fluctuations are meshed more densely, and the field is re-calculated with the refined meshing. The error between the two passes is evaluated. If this error is too important, the meshing is refined and the process continues until convergence criteria are met.

Once the computation is completed, the post-processor interface allows to plot solution data (S-parameters, impedance, propagation constants) in Cartesian or polar format. The S-parameter matrix can be de-embedded, renormalized and exported in several file formats, so that it can be easily imported in a Spice-like software for performing electrical simulations. Thanks to a friendly graphical display window, field quantities (electric and magnetic fields, Poynting vector...) can be plotted and superimposed to the 3D geometry.

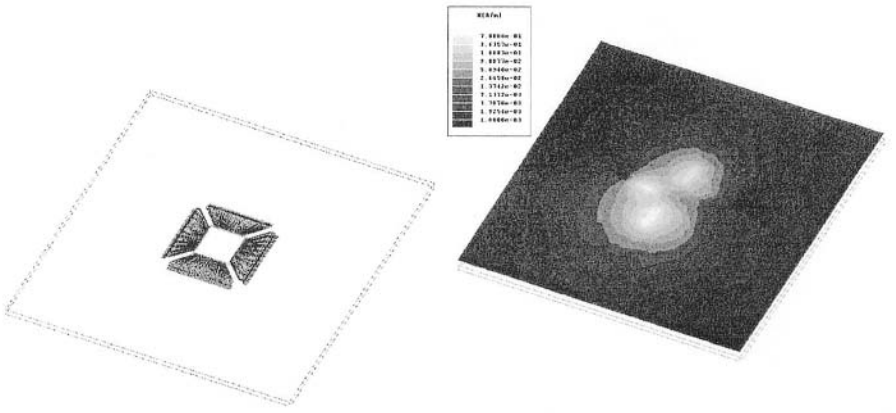

Figure B-25. Prediction of the near-field radiation from an integrated circuit.

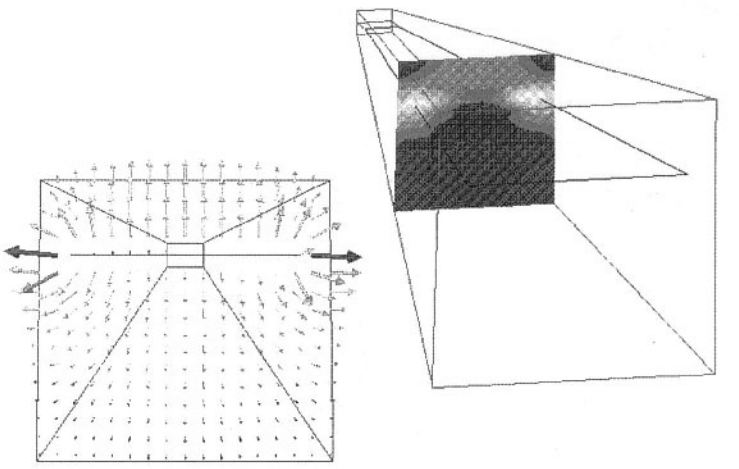

Figure B-26. Calculation of the electric field distribution (magnitude and vector form) in the transverse section of a GTEM cell .

7.2 EMC characterization of ICs with the HFSS solver

Fig. B-25 gives an example of HFSS usefulness for simulating the EMC behavior of ICs. Once the waveforms of the currents flowing inside IC lead frame have been calculated thanks to an electrical software or a tool using VHDL-AMS language, the cartography of the electromagnetic field radiated by the component can be simulated with HFSS and compared with experimental near-field scan measurements.

Particularly efficient for waveguides modeling, the HFSS solver can also be used for the calculation of the electromagnetic field propagating inside TEM and GTEM cells. Fig. B-26 presents the repartition of the electromagnetic field in the transverse section of a GTEM cell 250 from *Schaffner*.

8. FD2D

FD2D is a freeware developed and distributed by Carlsson (2005). This program uses the finite difference method to compute the inductance and capacitance matrices for multi-conductor transmission lines with conductors of arbitrary shape.

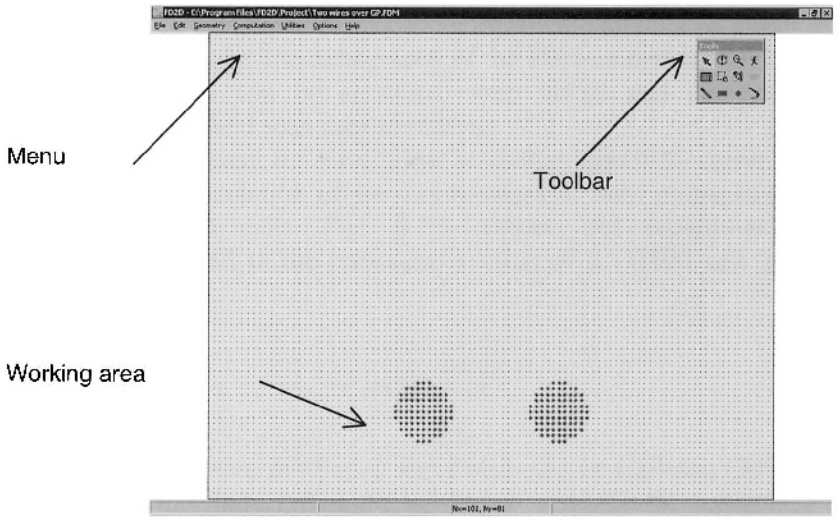

Figure B-27. FD2D General Interface to define the geometry.

The objective of this tool is to generate an equivalent circuit to perform time domain or frequency domain within circuit analysis programs, such as SPICE. As its name expresses, the structure must be defined by its cross section in 2D. This tool is particularly adapted to create equivalent models for transmission lines that have homogeneous structure along the 3rd dimension. In this annex we will focus more on the use of this tool than on the numerical techniques abundantly described in the literature.

8.1 Objectives and presentation of the interface

To perform EMC risk analysis on complex 3D structures, engineer's approach consists in making first approximations with some simplifications of the structure or of the problem to study. This is often based on a reduction of the problem using the topology approach, which consists in dividing a complex problem into several smaller parts depending on the electromagnetic environment. Another reduction is possible by reducing the problem from a 3D geometry to a 2D geometry when it is feasible. This can be done by some approximations of the structure and that it saves up a lot of time in the simulation.

FD2D is especially suited to perform such analysis. The general interface is presented below with the main functions of interest that will be described in the next part which focus on to a simple application.

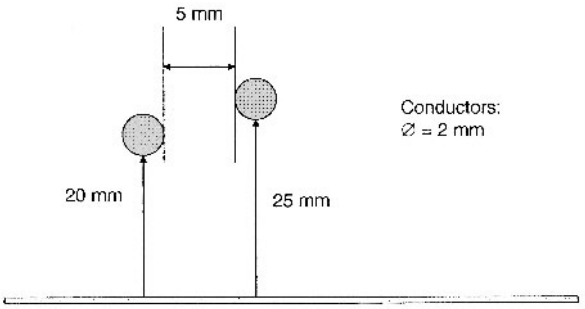

Figure B-28. Example of typical geometry solved with FD2D.

8.2 Modeling of homogeneous structure

To detail the use of this tool, we shall work on a small example which is defined by two cylindrical conductors above a ground plane. The geometry is presented in Fig. B-28.

In this first example we shall create an equivalent spice model for these wires above a ground plane. The first step will be to define the surface to be considered for the computation. Since all boundaries are electric walls in this tool, the surface must be far from the limits if open boundaries conditions are to be simulated. The grid is defined using arbitrary units. In our example 1 mm step is enough to describe our structure (for a more accurate result the step could be also reduced to 0.5 or 0.2 mm). FD2D can take into account a permittivity in the complete calculation domain, and also allows considering different permittivity for different areas.

Two important things must be checked at the end of the simulation to validate the accuracy of the result. The first one is the deviation obtained at the end of the simulation. If this value is higher than the maximum value defined in the simulation parameters, it means that the number of iterations obtained is not high enough and should be increased. The second thing to check is that the field is not disturbed by the boundary conditions (electric wall placed far enough of the object to simulate open boundary). This can be done by looking at the potential and/or E-field.

In our example, the result appears correct, which means that our structure is correctly defined. If the metallic wall were too close to the object the results could look like the right figure, with equipotential lines near the boundary and with fields reinforced due to this proximity (Fig. B-29).

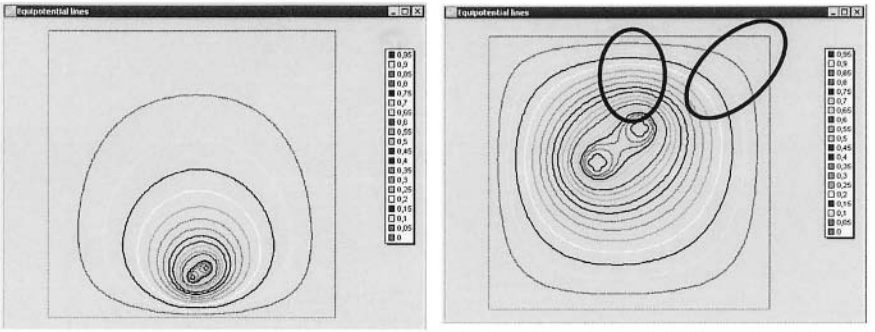

Figure B-29. Potential plot – structure validation

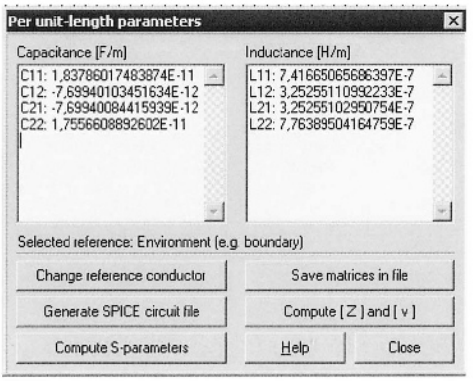

Figure B-30. Per unit length parameter results

Since the structure and parameters are validated, we can compute the per-unit length parameters. A new window opens (Fig. B-30) at the end of the calculation and allows to perform several interesting actions, such as saving the L and C matrices in ASCII files, calculating equivalent Z and velocities in these lines, or computing S-parameters.

From this result a Spice model of the structure can be computed directly, as proposed in the menu above. The length of the structure must be identified (1 meter for example), and the number n of Pi-sections must be specified. This can be calculated by Eq. B-2 which related n to the upper frequency of interest f_{max} with which the model is to be used.

$$n = \frac{(Length\_of\_transmission\_line) \cdot 10 \cdot f_{\max}}{c} \qquad \text{(B-2)}$$

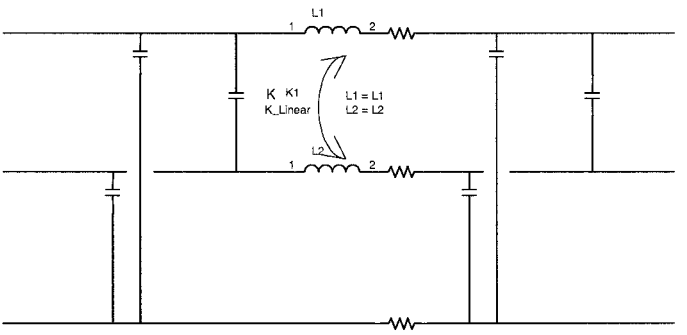

Figure B-31. Elementary Pi section used for the Spice model generation.

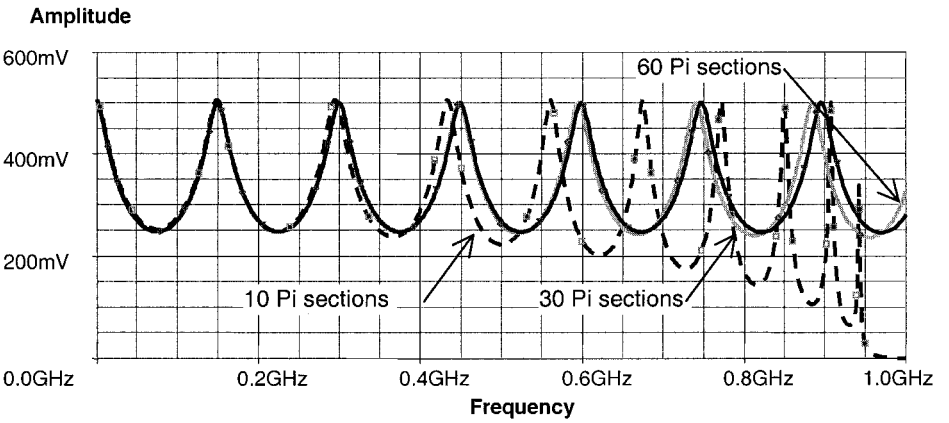

Figure B-32. Influence of Pi sections on accuracy – Transmission on one line.

In the netlist we can identify the values of the different parts of the generic π structure illustrated in Fig. B-31. Some typical results are shown in Fig. B-32 for a transfer analysis and with 10 / 30 and 60 π sections for the models. It makes it possible to show the limitation of the model and the margin regarding the criteria given above. The result with 10 π sections is valid until 400 MHz, which corresponds to our objective.

8.3 Comparison with 3D Techniques

A comparison with the result obtained with a 3D Numerical technique on transmission and crosstalk is given below (Fig. B-33) and makes it possible to validate the model extracted with FD2D.

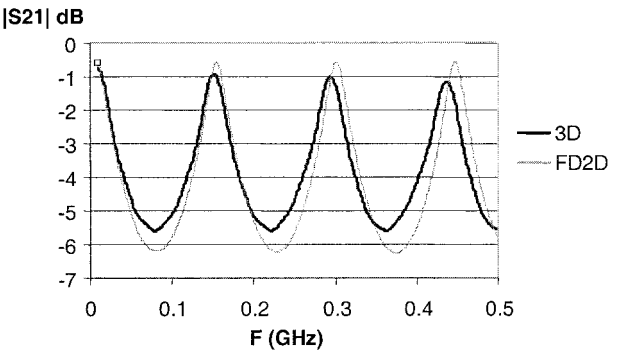

Figure B-33. Comparison between 3D result and FD2D – Transmission line 1

The results obtained exhibit differences less than 1 dB between the 3D numerical technique and FD2D. We can consider that this is enough to perform risk analysis. To have a better accuracy we have to keep in mind that this software computes L and C matrices and builds transmission lines without any losses (radiations and resistive losses). Another key point is that in our example the structure had been defined with big meshes, and with a smaller mesh, results would also be closer to the 3D result.

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Hamster, more information on http://www.hamster-ams.com

Aseris/Emc2000, more information on www.aseris-emc2000.com

Feko, more information on http://www.feko.info/

F2D2, more information on http://www.sp.se/electronics/RnD/software/eng/default.htm

GLOSSARY

Abbreviations used in the field of Electromagnetic Compatibility and Integrated Circuits

Abbreviation	Description
AC	*Alternating Current*
ACT	*Advanced CMOS-TTL*
ADC	*Analog-to-digital Converter*
AEC	*Automotive Electronic Council*
AM	*Amplitude Modulation*
AMS	*Analog and Mixed-Signal extension of VHDL language*
ANSI	*American national standard institute www.ansi.org*
ASIC	*Application Specific Integrated Circuit*
BCH	*Bose Chaudhuri Hhochquenghem mutlilevel error coding*
BCI	*Bulk Current Injection susceptibility method*
BER	*Bit Error Rate in data transmission*
BGA	*Ball gate array package*
BIRD	*Buffer Issue Resolution Documents at the IBIS committee*
BSIM	*Berkeley Small Channel MOS Model*
CAN	*Control Area Network*
CDV	*Committee Draft for Voting (IEC standards)*
CDFG	*Control Data Flow Graphs*
CDN	*Coupling Decoupling Network*
CDM	*Charged Device Model for Electrostatic Discharge*
CE	*European conformity (French)*
CISPR	*International special committee on radio interference*
CM	*Common Mode*
CMRR	*Common-mode rejection ratio*
CMOS	*Complementary Metal-oxide-Semiconductor*
CQM	*Certified quality manager*
CRT	*Cathode ray tube*
CSP	*Chip Scale Packaging*
CW	*Continuous Wave*
dBm	*Decibel above one milliwatt*
dBuV	*Decibel above one microvolt*
DC	*Direct Current i.e. continuous flow of electricity through a conductor*
DIL	*Dual-In-Line package*
DM	*Differential Mode*
DOE	*Design-Of-Experiment*
DSM	*Deep-Submicron technology for IC fabrication*

Abbreviation	Description
DSP	*Digital Signal Processor*
DUT	*Device Under Test*
ECS	*Equivalent Current Source*
ECU	*Electronic Control Unit*
EDA	*Electronic Design Automation*
EEPROM	*Electrically Erasable Programmable Read Only Memory*
EFT	*Electrical Fast Transients*
EIA	*Electronic Industries Alliance*
EMI	*Electro Magnetic Interference*
EMC	*Electro Magnetic Compatibility*
EMU	*EMI modeling Unit*
EOS	*Electrical Over Stress*
ESD	*Electro Static Discharge*
ESDA	*Electrostatic Discharge Association*
ESR	*Equivalent Series Resistance*
FBGA	*Fine-pitch Ball Grid Array*
FCT	*Fast speed CMOS*
FFT	*Fast Fourier Transform*
FM	*Frequency Modulation*
GDS	*Generic Data format for IC layout description*
GND	*Designates the ground voltage*
GTEM	*Gigahertz Transverse Electromagnetic*
GRP	*Ground Reference Plane*
GDSII	*Graphic Design System version II, for IC layout description*
HBM	*Human Body Model for electrostatic discharge*
HC	*High speed CMOS*
HCT	*High speed CMOS-TTL*
HF	*High frequency (3MHz-30MHz)*
IA	*Internal Activity*
IBC	*Internal Block Coupling*
IBIS	*I/O Buffer Information Specification*
IC	*Integrated Circuit*
ICEM	*Integrated circuits emission model*
ICIM	*Integrated Circuit Immunity Model*
IEC	*International Electro technical Commission*
IEEE	*Institute of Electrical and Electronics Engineers*
IF	*Intermediate Frequency*
IMIC	*I/O Interface Model for Integrated Circuits*
IO	*Input/Output*
IP	*Intellectual Property*
ISO	*International organization for standardization www.iso.org*
JEDEC	*Joint Electron Device Engineering Council*
JEITA	*Japan electronic and information technology industrial association*
JTAG	*Joint Test Action Group, acronym for the IEEE 1149.1 standard for logic testing of ICs*
LCC	*Lead-less chip carrier*
LD	*Logical Depth*
LECCS	*Linear Equivalent Circuit and a Current Source Model*

Abbreviation	Description
LIN	*Local Interconnect Network*
LISN	*Line impedance stabilization network*
LSI	*Large Scale Integration*
LVDS	*Low Voltage Differential Swing Input/output interface*
MIL-STD	*Military Standard*
MM	*Machine Model for Electrostatic Discharge*
MOS	*Metal-oxide-Semiconductor*
NOP	*No-operation (Microprocessor instruction)*
OEM	*Original equipment manufacturer*
OFAT	*One factor at a time*
PEEC	*Partial element equivalent circuit (numerical method)*
PC	*Personal computer*
PCB	*Printed circuit board*
PDN	*Passive-Distribution-Network*
PGA	*Pin-Grid-Array package*
PLL	*Phase-Lock-Loop*
PMU	*Power Routing Unit*
PRU	*Power Switching Unit*
PWL	*Piece-Wise-Linear*
PWM	*Pulse-Width Modulation*
QFP	*Quad-flat-package*
RAM	*Random-Access Memory*
RBW	*Resolution Bandwidth of spectrum analyzers*
RF	*Radio Frequency*
RFI	*Radio Frequency Interference*
SAE	*Society for Automotive Engineering, USA*
SC	*Sub-committee of IEC*
SDIL	*Shrink Dual-In-Line package*
SHF	*Super High Frequency (3GHz-30GHz)*
SI	*Signal Integrity*
SIP	*System-In-Package*
SMA	*Subminiature connector version A*
SMB	*Subminiature connector version B (Smaller than A, up to 4GHz)*
SMD	*Surface mount device*
SOC	*System-On-Chip*
SOP	*Small outline package*
SPICE	*Analog Simulation software from Univ. of Berkeley, USA*
SRAM	*Static Random Access Memory*
SWR	*Standing wave ratio*
TC	*Technical Group at IEC*
TDMA	*Time Domain Multiple Access*
TDR	*Time Domain Reflectometry*
TEM	*Transverse Electromagnetic Mode*
THF	*Tremendously High Frequency (300GHz-3THz)*
TL	*Transmission Line*
TLP	*Transmission Line Pulse*
TM	*Transverse Magnetic*
TQFP	*Thin Quad Flat Package*

Abbreviation	Description
TTL	*Transistor to Transistor Logic*
UBGA	*Micro Ball gate array package*
UHF	*Ultra High Frequency (300MHz-3GHz)*
ULSI	*Ultra Large Scale Integration*
USB	*Universal Serial Bus*
UTE	*Union technique de l'électricité et de la Communication (French)*
VBW	*Video Bandwidth. Used for spectrum analyzer filter.*
VCC	*Voltage at the Common Collector. Used to designate the positive supply voltage*
VDE	*Verein Deutscher Elektroniker (German)*
VHDL	*Very High Speed Integrated Circuit Hardware Description Language*
VHDL-AMS	*Analog and Mixed-Signal extension of Very High Speed Integrated Circuit Hardware Description Language*
VHF	*Very high Frequency (30MHz-300MHz)*
VLSI	*Very Large Scale Integration*
VNA	*Vector network analyzer*
VSWR	*Voltage standing wave ratio*
WBFC	*Workbench Faraday Cage*
WG	*Working Group of IEC*
XHF	*Extremely High Frequency (30GHz-300GHz)*

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