Howard Cam Luong · Jun Yin

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Preface

Voltage-controlled oscillators (VCOs) and frequency dividers are two of the key building blocks in phase-locked loops (PLLs) and frequency synthesizers, not only to generate clean LO signals for frequency conversion in wireless transceivers but also to generate accurate high-frequency clock signals for wireline systems. As the system applications continue to demand higher and higher performance in terms of higher frequency, wider bandwidth, lower phase noise, and lower power consumption, the design of these building blocks becomes more and more challenging, in particular in aggressively scaled low-voltage CMOS processes for low cost and high system-on-chip integration.

Many years ago, we published a book entitled "Low-Voltage CMOS RF Frequency Synthesizers" to discuss and summarize various inductor-based design techniques for low-voltage high-performance frequency synthesizers. The main focus was on low-voltage and low-power designs for narrow-band applications, in which integrated inductors play a critical role. However, due to their high-Q and narrow-band characteristics, these design techniques have limited applications in recently emerging multi-band multi-mode and software-defined radios. Fortunately, transformer-based design techniques have recently been developed and emerged as potential replacement of integrated inductors for more features and even better performance. However, to the best of our knowledge, there has still been no book aiming to introduce transformer-based low-voltage and wideband CMOS VCOs and frequency dividers.

As continuation and complementary to our previous book and intended for engineers, mangers, researchers, and students who are working on or interested in CMOS radio frequency or mm-Wave integrated circuits and systems, this book presents in-depth description and discussion of transformer-based design techniques that enable CMOS oscillators and frequency dividers to achieve ultra-wide frequency tuning range and ultra-wide frequency locking range while maintaining state-of-the-art performance in terms of high operation frequency, low supply voltage, good phase noise, and low power consumption. In addition to the design, simulation, and characterization of integrated transformers for different

applications, this book will also discuss their unique characteristics and features that enable performance improvement, such as passive coupling or multiple impedance peaks, which have not been covered in any of the existing books. Finally, to illustrate the usefulness of these transformer-based design techniques, design consideration and optimization of various CMOS oscillators and frequency dividers for different applications together with their measured performance are elaborated, focusing on not only ultra-low supply voltage but also ultra-wide frequency tuning range and locking range at very high frequencies.

More specifically, detailed description and discussion of the following selected designs will be included in the book.

1. A transformer-feedback VCO (TF-VCO) features high swing and low phase noise even at a supply voltage below the device threshold voltage. Fabricated in a 0.18-μm CMOS process, a 1.4-GHz PMOS TF-VCO achieves an FoM of 190 at 0.35-V supply voltage, and a 3.8-GHz NMOS TF-VCO achieves an FoM of 193 at 0.5-V supply voltage.

2. A quadrature VCO using transformer coupling (TC-QVCO) eliminates both noise and power consumption by active coupling devices in existing QVCOs while exhibiting all advantages in the TF-VCO. Fabricated in a 0.18-μm CMOS process, a 17-GHz TC-QVCO achieves an FoM of 187.6 and a phase error of $1.4°$ at 1-V supply voltage.

3. A transformer-based dual-mode VCO achieves a wide frequency tuning range exploiting the two impedance peaks of a transformer tank. Fabricated in a 0.13-μm CMOS process, the 2.7-to-4.3 GHz and 8.4-to-12.4 GHz dual-mode QVCO achieves average FoM_T of 195 and 203 in the two bands, respectively.

4. A magnetically tuned multi-mode VCO (MT-VCO) measures ultra-wide frequency tuning range around 70 GHz by changing the coupling coefficient of the transformer. Fabricated in a 65-nm CMOS process, the 57.1-to-90.1 GHz MT-VCO achieves an average FoM_T of 188.2 at 1-V supply.

5. Transformer-feedback injection-locked frequency dividers (TF-ILFDs) feature quadrature outputs with enhanced output swing even with low supply and low power. Fabricated in a 0.18-μm CMOS process, a 18.1-GHz TF-ILFD with differential outputs achieves 21.6 % locking range when consumes 2.75–4.35 mW at 0.5-V supply, and a 17.5-GHz TF-ILFD with quadrature outputs achieves 27.8 % locking range when consuming 11.4–13.6 mW at a 0.6-V supply.

6. A self-frequency-tracking injection-locked frequency divider (SFT-ILFD) utilizing transformer to generate the injection current with frequency-dependent phase shift to extend the locking range. Fabricated in a 65-nm CMOS process, a 62.9-GHz SFT-ILFD achieves 29 % locking range while consuming 1.9 mW at a 0.8-V supply voltage.

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Contents

Chapter 1
Introduction

1.1 Motivation

Wireless and wireline transceiver systems have greatly been benefited from the aggressive scaling down of CMOS technology to improve their performance in terms of speed, power, and form factor. On the other hand, the CMOS technology scaling down also imposes great challenges to designs of radio frequency (RF) and analog circuits mainly because the supply voltage (V_{DD}) scales much faster than the threshold voltage (V_{th}) of CMOS transistors. From Fig. 1.1, the available overdrive voltage ($V_{DD}-V_{th}$) in 65-nm CMOS technology is reduced to around 0.5 V, which limits the voltage headroom and significantly degrades the performance of RF and analog circuits.

For emerging applications powered by various energy-harvesting methods, the generated supply voltage V_{DD} may be as low as or even lower than the device threshold voltage V_{th}, which limits practical use of many conventional RF and analog integrated circuits design techniques. Although on-chip boost converters can be employed to increase the supply voltage, for applications with such low input voltages and large voltage conversion ratios, their limited efficiency of around 40–75 % would cause significant power penalty [2]. Instead, exploiting RF and analog circuit techniques that can work under supply voltage close to V_{th} has been proven to be a promising solution to greatly reduce the power consumption [3].

On the other hand, emerging wireless applications utilizing much high carrier frequencies can take advantages of the large bandwidth available to provide services with data rate of multi-gigabit per second. For example, the IEEE 802.11ad (WiGig) standard [4] and IEEE 802.15.3c standard [5] located at 60 GHz provide available bandwidth of 9 GHz. However, design of wideband transceivers to cover such a large bandwidth at such a high frequency becomes quite challenging.

RF frequency synthesizers based on phase-locked loops (PLLs) to provide the local oscillation (LO) signals for frequency conversion is one of the key building
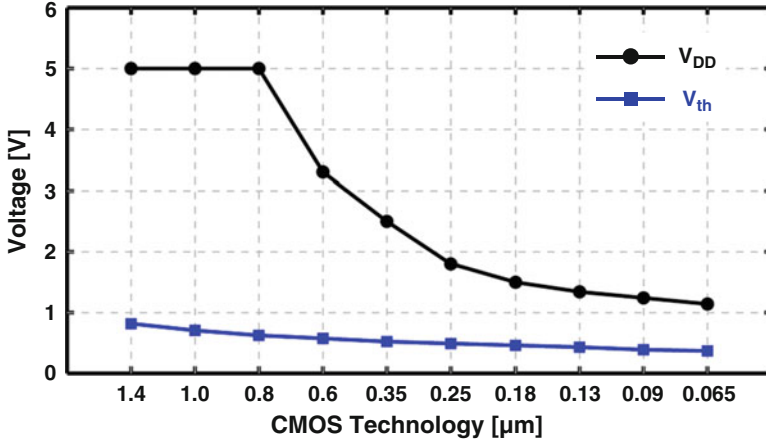
Fig. 1.1 Scaling down of supply voltage (V_DD) and threshold voltage (V_th) with the CMOS technologies [1]

blocks in wireless transceivers. The quality of the LO signals in terms of phase noise and spur would significantly affect the performance of the whole transceivers, such as the receiver sensitivity and the transmitter spurious emission. For PLLs, researches have recently focused more and more on the digital-intensive designs to make use of aggressive scaling down in CMOS technologies [6]. In digital PLLs (DPLLs), although there are digital substitutes for the phase-frequency detector (PFD), loop filter, and even frequency dividers operating at several GHz, the voltage-controlled oscillator (VCO) or the digitally controlled oscillator (DCO) still needs to be designed in the analog domain due to its high operating frequency and stringent noise performance requirement. Similarly, at millimeter-wave (mm-Wave) frequencies, the frequency dividers serving as prescalers also need to be carefully designed in the analog domain for high performance in terms of frequency, locking range, and power consumption [7].

VCOs and frequency dividers, as the two critical building blocks operating at the highest frequencies, directly affect the output frequency range and the out-of-band phase noise of the whole PLLs. LC-VCOs as shown in Fig. 1.2a are usually employed in the frequency synthesizers for wireless applications since LO signals with low out-band phase noise are required to meet the stringent blocker or spurious emission requirement for the receiver or transmitter, respectively. For the design of frequency divider, although current-mode logic (CML) dividers are fast enough for applications at giga-Hz frequency range in submicron CMOS process, injection-locked frequency dividers (ILFDs) [8, 9] with inductive tank as shown in Fig. 1.2b and c are still a necessity at mm-Wave frequencies since they feature higher operation frequencies with lower power consumption compared with CML dividers [10, 11]. For LC-VCOs and LC-ILFDs based on conventional LC tanks, their performance such as noise, operating frequency range, and driving capabilities would degrade rapidly with the scaling down of supply voltage, which limits their
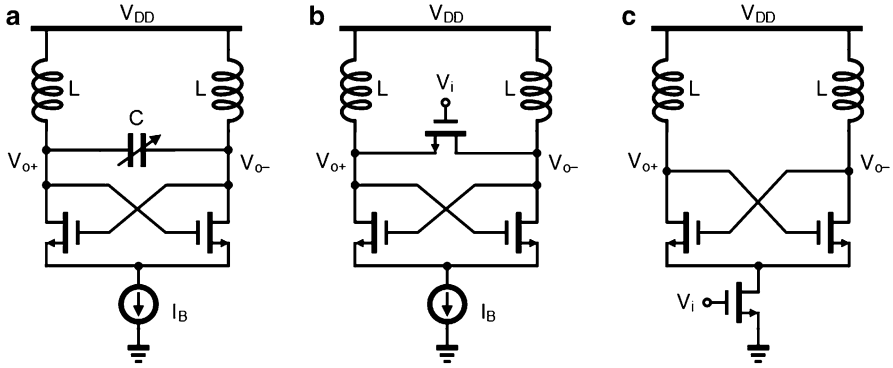
Fig. 1.2 Schematic of conventional (**a**) LC-VCO, (**b**) LC-ILFD with direct injection, and (**c**) LC-ILFD with indirection injection from current bias

usage as the CMOS technology is further scaled down. Even worse, for the applications requires a supply voltage lower than the device threshold voltage V_{th}, the conventional LC-VCOs and LC-ILFDs may fail to work properly since the cross-coupled transistors cannot provide large enough negative transconductance to compensate the loss from the LC tank.

For the design of LC tanks in conventional LC-VCOs and LC-ILFDs, high tank quality factor (Q) is preferred to suppress the noise while still maintaining low power consumption. On the other hand, the narrowband frequency response characteristics of a high-Q tank would in turn limit the operating frequency range of LC-VCOs and the locking range of LC-ILFDs. In particular, it would impose a critical challenge in modern RF transceivers that can support multi-standard and multiband applications or even the software-defined radio (SDR) and cognitive radio applications, in which ultra-wideband LOs are required. The most straightforward way to cover a wide frequency range is to duplicate multiple narrowband LC VCOs and to multiplex their outputs [12, 13]. For example, in a 40-nm digital CMOS process, two LC-VCOs (6–9 and 9–12 GHz) are needed to cover the required 6–12 GHz frequency range with sufficient phase-noise performance for SDR application in [14]. However, this method is not area efficient since the monolithic inductor occupies much larger chip area than other devices and is not scalable with CMOS technology.

To make the matter worse, the problem with insufficient tuning range of conventional LC-VCOs becomes more and more acute as the oscillation frequency keeps increasing. Since the varactor Q becomes dominantly low in the tank, the limited varactor size degrades the frequency tuning range greatly. The typical tuning range of LC-VCOs reported at around 60 GHz is less than 10 % [14–16], which is far from being sufficient to cover the 9-GHz bandwidth required by IEEE 802.11ad standard or IEEE 802.15.3c standard when taking into account process variations and inaccurate device modeling. Similarly, high-frequency LC-ILFDs suffer from a big

problem with insufficient frequency locking range due to their desirable high tank Q for low power consumption and narrowband filtering. At input frequency of around 60 GHz, the typical locking range of LC-ILFDs reported is around 12 % [17, 18].

In this book, in-depth description and discussion of transformer-based design techniques that enable CMOS VCOs and ILFDs to achieve state-of-the-art performance in terms of low supply voltage, low-power consumption, good phase noise, high operation frequencies, and wide frequency tuning range and locking range are presented. To illustrate the usefulness of these transformer-based design techniques, design consideration and optimization of various VCOs and dividers for different applications together with their measured performance are discussed in detail, focusing on not only ultra-low supply voltage but also ultrawide frequency tuning range and locking range at high frequencies.

1.2 Book Organization

This book is organized as follows. Chapter 2 will introduce how to design, simulate, and characterize on-chip inductors and transformers in CMOS process, including step-by-step procedures to simulate and model the passive devices for circuit design and to verify the model based on silicon measurement. In Chap. 3, the phase-noise analysis and design consideration of VCOs and quadrature VCOs (QVCOs) will be reviewed, and the performance degradation with the scaling down of V_{DD} will be discussed in detail. Chapter 4 introduces the principle of ILFDs and Miller dividers and analyzes their locking range based on the phasor diagram. To demonstrate the usefulness of the transformer-based design techniques, detailed design considerations and measured results of a couple selected low-voltage high-performance VCOs and QVCOs using transformer feedback will be presented in Chap. 5. Chapters 6 and 7 will focus on the designs of transformer-based dual-mode or multimode VCOs for wideband applications. In Chap. 8, design examples for ILFDs using transformer technique to achieve either low-voltage or wide locking range will be discussed. Finally, conclusion will be drawn in Chap. 9, from which recommendations for future work will be made.

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Chapter 2
Transformer Design and Characterization in CMOS Process

2.1 Background

On-chip inductors have become essential in RF system-on-chip design and integration. As compared with off-chip inductors on the printed circuit board (PCB) or bondwire inductors, the use of on-chip inductors prevents degradation of circuit performance due to the loss and the parasitics from the chip interface. Moreover, high-level integration with on-chip inductors can not only significantly reduce the cost and the form factor but also improve the reliability of the whole wireless systems.

Unfortunately, on-chip inductors suffer from a low quality factor Q, which would result in performance degradation in terms of noise, gain, and power consumption. As a consequence, modern RF CMOS processes provide one or two thick top metal layers far above the lossy substrate to improve the quality factor Q and the self-resonant frequency of the on-chip inductors [1, 2]. In addition, due to its relatively narrowband characteristics, on-chip inductors may not be suitable for wideband applications, such as multiband, multimode, or software-defined radios.

As potential replacement and improvement of on-chip inductors, integrated transformers have recently been considered and widely used in wideband RF and mm-Wave circuits and systems. Their main applications include (1) impedance transformation in the impedance matching network, (2) amplification for voltage or current signal, (3) balun for on-chip single-ended to differential or differential to single-ended signal transformation, and (4) high-order resonant tank to obtain either multiple narrowband or wideband frequency response of amplitude and phase for many circuits, including LNAs, VCOs, frequency dividers, frequency multipliers, etc.

Figure 2.1a shows the schematic symbol of an ideal N:1 transformer, where $N = V_1/V_2$ is defined as the turn ratio between the primary coil and the secondary coil. Since an ideal transformer is passive and no energy losses occur during the voltage and current transformation, the current ratio I_2/I_1 equals to $-N$. As a result,
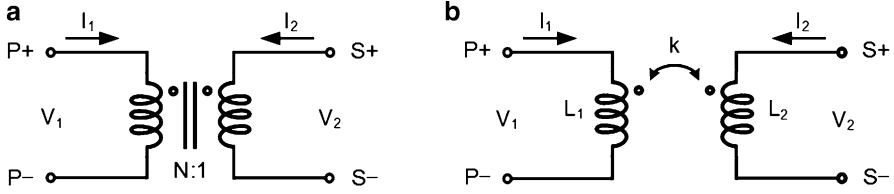
Fig. 2.1 Schematic symbol of (**a**) an ideal N : 1 transformer and (**b**) a transformer made of two coupled inductors

the impedance seen from the primary coil becomes N^2 times of the loading impedance of the secondary coil.

Figure 2.1b shows a transformer made of two coupled inductors. From the Faraday's law of induction, the induced voltage at either coil equals to the rate of change of the total magnetic flux going through it:

$$V_1 = -\frac{d(\Phi_{11} + \Phi_{21})}{dt} = \left(-\frac{d\Phi_{11}}{dI_1}\right) \cdot \frac{dI_1}{dt} + \left(-\frac{d\Phi_{21}}{dI_2}\right) \cdot \frac{dI_2}{dt} \qquad (2.1a)$$

$$V_2 = -\frac{d(\Phi_{22} + \Phi_{12})}{dt} = \left(-\frac{d\Phi_{22}}{dI_2}\right) \cdot \frac{dI_2}{dt} + \left(-\frac{d\Phi_{12}}{dI_1}\right) \cdot \frac{dI_1}{dt} \qquad (2.1b)$$

where Φ_{11} (Φ_{22}) is the magnetic fluxes in the primary (secondary) coil generated by the current I_1 (I_2) in itself and Φ_{21} (Φ_{12}) is the magnetic fluxes in the secondary (primary) coil generated by the current I_2 (I_1) in its neighboring coil. By defining the self-inductance as $L_1 = -(d\Phi_{11}/dI_1)$, $L_2 = -(d\Phi_{22}/dI_2)$, the mutual inductance as $M = -(d\Phi_{12}/dI_1) = -(d\Phi_{21}/dI_2)$, and applying Laplace transformation to (2.1a) and (2.1b), V–I equations of the ideal transformer can then be expressed as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} sL_1 & sM \\ sM & sL_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \qquad (2.2)$$

In the circuit analysis, the T-model as shown in Fig. 2.2 is typically employed to represent the transformer made of coupled inductors as shown in Fig. 2.1b, which can also be easily shown to be equivalent to (2.2). To represent the coupling strength between the two coupled inductors, the magnetic coupling coefficient k defined as the ratio between mutual inductance and self-inductance can be used as below:

$$k \equiv \frac{M}{\sqrt{L_1 L_2}} \qquad (2.3)$$

According to the definition, k is an indicator of the coupling strength between the primary and secondary coils. For ideal transformers, there is no leakage of magnetic flux, and the coupling coefficient is unity. However, due to the poor confinement of

Fig. 2.2 T-model of the
transformer
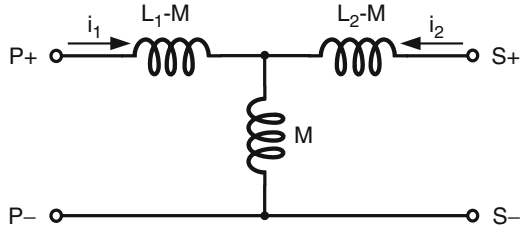
magnetic flux in integrated transformers, the coupling coefficient is always sub-
stantially smaller than one [3].

Figure 2.3 shows another equivalent circuit model of the transformer
that employs an ideal transformer. Here, the ideal transformer with a turn ratio
$N = M/L_2 = k\sqrt{L_1/L_2}$ and the inductance $k^2 L_1$ represents the coupling effect
between primary and secondary coils, while the inductance $(1-k^2)L_1$ models the
leakage flux that does not contribute the magnetic coupling. It is easily proved that
the equivalent model as shown in Fig. 2.3 is mathematically the same as the
T-model. As shown in the following chapters, the proper choice of the equivalent
models can facilitate the circuit calculation.

It is worthwhile to note the meaning of the dots in the transformer symbols in
Fig. 2.1. Assuming k is always positive, the dots should be denoted in such a way
that when the currents are sent into the dotted terminals from both the primary and
secondary coils, the generated magnetic fluxes from both coils should go in the
same direction which reinforce each other [4]. Figure 2.4 shows the example to
determine the dot location based on this convention.

2.2   Transformer Layout

The common ways to realize integrated transformers are illustrated in Figs. 2.5, 2.6,
and 2.7, which offer different tradeoffs on self-inductances, magnetic coupling
coefficient, inter-coil and coil-to-substrate capacitances, self-resonant frequencies,
and chip area [5]. Here, all the layouts are based on the differential configurations
since they are commonly used in VCOs and frequency dividers with balanced
differential outputs.

Figure 2.5 shows an interleaved transformer layout. Both the primary and
secondary coils are implemented with the same metal layer. As for on-chip inductor
design considerations [2], the thick top metal layer is typically used for maximum
quality factor Q and high self-resonant frequency because it has much smaller
square resistance than other metal layers and far away from the low resistance
substrate in CMOS process. When the metal traces need to be crossed over, the
lower metal layer can be used as a bridge. Since the interleaved configuration
allows large common periphery between the primary and secondary coils, it can

Fig. 2.3 Equivalent circuit
model of the transformer
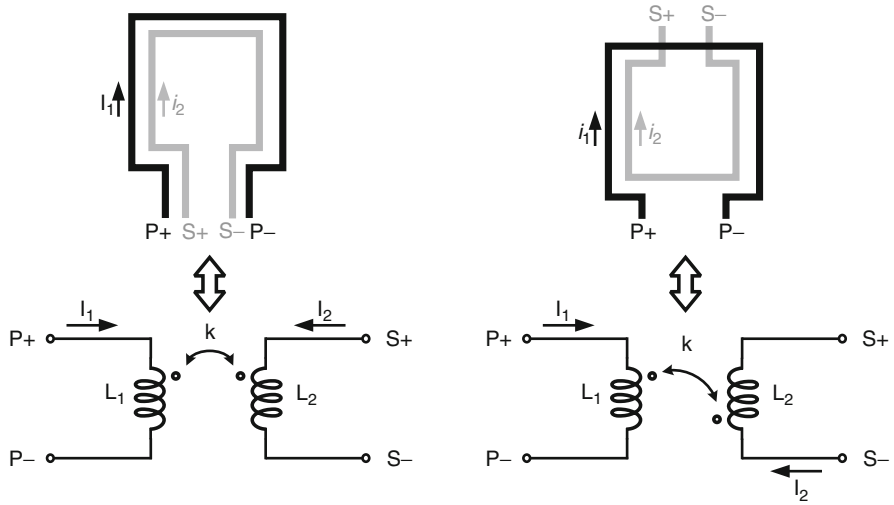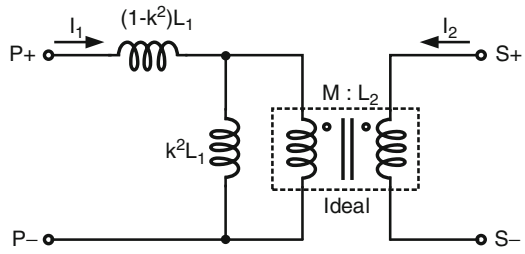
Fig. 2.4 Transformers with different coupling directions and their corresponding schematic
symbol using the dot convention

Fig. 2.5 Layout of an
interleaved transformer
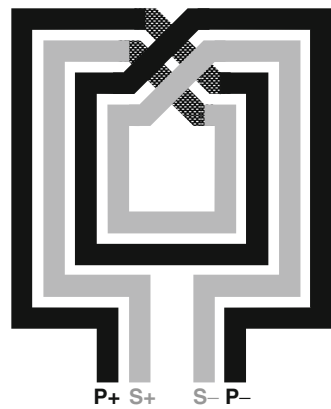
Fig. 2.6 Layout of a tapped transformer

P+ S+   S− P−
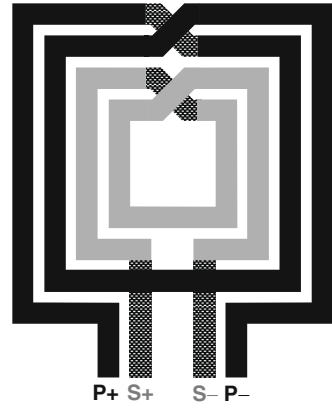
Fig. 2.7 Layout of a stacked transformer: (**a**) top view and (**b**) cross-section view

a

P+ S+   P− S−

b

Metal Trace

Dielectic

Dielectic

Substrate
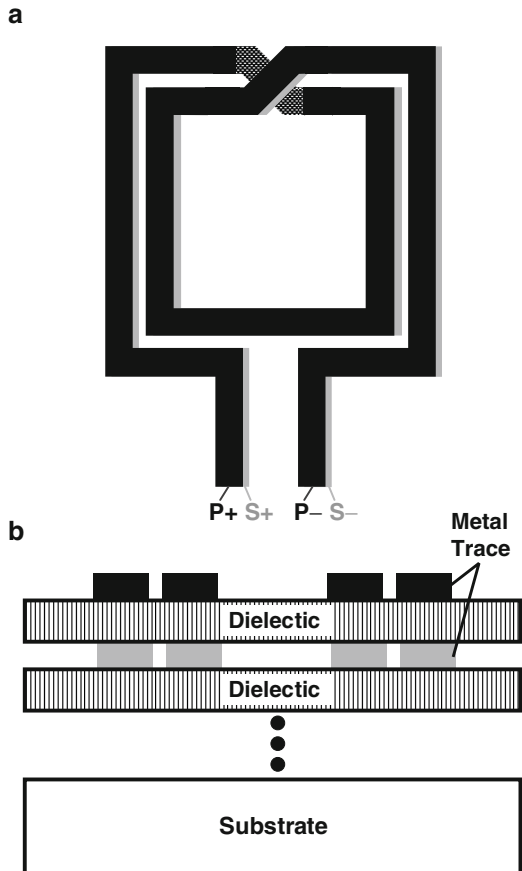
Table 2.1 Comparison of different types of integrated transformer

Transformer structure	k	Self-inductance	Area	Self-resonant frequency
Interleaved	>0.7	Medium	Medium	Medium
Tapped	0.3–0.7	Low	Large	High
Stacked	~0.9	High	Small	Low

provide a relatively high coupling coefficient of above 0.7 at the expense of increased inter-coil capacitance and reduced self-inductance since the neighboring metal traces in the same coil are separated by the metal trace from the other coil.

In a taped transformer, both the coils are also implemented in the top metal layer shown in Fig. 2.6. Since the two coils are completely separated, the self-inductance is maximized and the inter-coil capacitance is minimized. However, because only a single turn in the two coils share the common periphery, the coupling coefficient k becomes lower than that of the interleaved configuration. Depending on the space between the two coils, the typical k of the taped transformer can vary from 0.3 to 0.7. Furthermore, the spatial separation of the two coils also results in larger chip area.

Figure 2.7 shows a stacked transformer layout, in which the primary and secondary coils are implemented in different metal layers. Both vertical and lateral magnetic coupling are utilized to maximize the self-inductance and thus achieve the best area efficiency. Since the dielectric thickness is much smaller than the minimal space between the two neighboring top metal traces, the magnetic coupling is enhanced compared with that of the interleaved configuration. As an example, in a 65-nm CMOS process, the dielectric thickness is smaller than 1 μm, while the minimal space of the top metal is around 2 μm. Consequently, the coupling coefficient can be close to 0.9 if the metal traces in different layers are perfectly aligned. On the other hand, the inter-coil capacitance increases due to the reduced space between the two coils. In addition, the capacitance from the secondary coil to the substrate also increases since it is implemented in the lower metal layer closer to the substrate. It follows that stacked transformers usually have the lowest self-resonant frequency. The performances of different types of integrated transformers are summarized and compared in Table 2.1.

2.3 Transformer Measurement and Characterization

Basic considerations and guidelines for design, simulation, layout, and characterization of integrated transformers are mostly the same as those for on-chip inductors, which have been well described in many references [2, 3] and will not be repeated here. In the following section, only critical differences unique for integrated transformers are summarized and highlighted.

As illustrated in Fig. 2.8, a typical design and characterization flow of integrated transformers is summarized as below:

Fig. 2.8 Design and
characterization flow of
integrated transformers
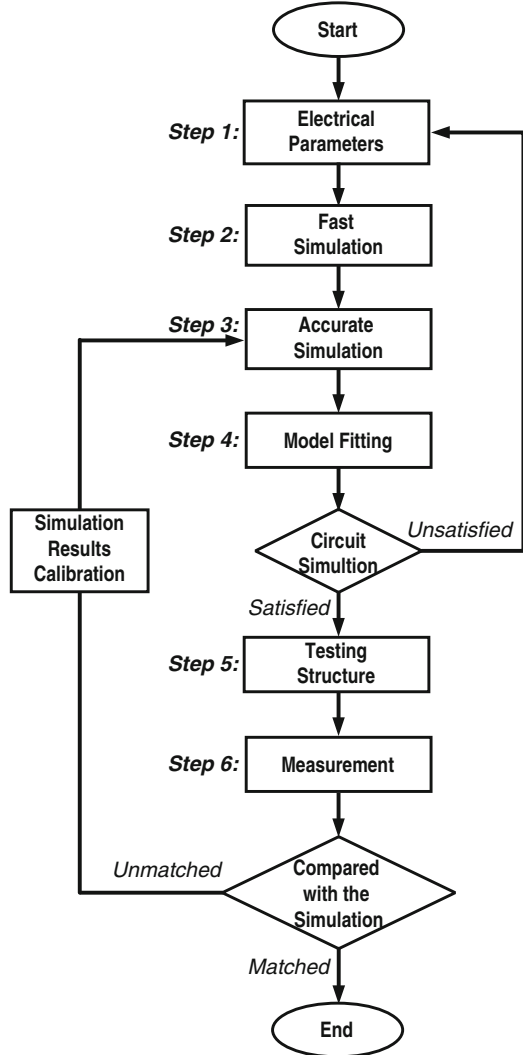
Step 1: Obtain the required electrical parameters of the transformer such as self-inductance, quality factor, and coupling coefficient from either calculation or simulation of the targeted transformer using equivalent circuit models.

Step 2: At the beginning, the physical parameters of the transformer can be quickly estimated and optimized for a given transformer structure by using a fast simulator such as ASITIC [6]. In the optimization, different layout configurations can be considered, from which the physical parameters such as the number of turns, the diameter, metal width, and metal space can be adjusted. Since fast simulators usually overestimate the quality factor Q, the relative trend of the quality factor from different parameter combinations is more useful than its absolute value as a quick reference for optimization.

Step 3: After obtaining the physical parameters from a fast simulation, the transformer can be further simulated by using more accurate electromagnetic (EM) simulator such as the ADS Momentum [7] or HFSS [8]. Usually the simulation results are in the formats of S parameters. To compare with the design goals, the simulated S-parameter data need to be converted into the Z-parameters using the following equations [9]:

$$Z_{11} = Z_0 \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \qquad (2.4a)$$

$$Z_{12} = Z_0 \frac{2S_{12}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \qquad (2.4b)$$

$$Z_{21} = Z_0 \frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \qquad (2.4c)$$

$$Z_{22} = Z_0 \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \qquad (2.4d)$$

where Z_0 is impedance of the ports used in the simulation. With the Z-parameters, the following equations can be employed to obtain the electrical parameters of the transformer:

$$L_1 = \frac{\mathrm{Im}(Z_{11})}{\omega} \quad \text{and} \quad L_2 = \frac{\mathrm{Im}(Z_{22})}{\omega} \qquad (2.5a)$$

$$Q_1 = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})} \quad \text{and} \quad Q_2 = \frac{\mathrm{Im}(Z_{22})}{\mathrm{Re}(Z_{22})} \qquad (2.5b)$$

$$k = \frac{\mathrm{Im}(Z_{21})}{\sqrt{\mathrm{Im}(Z_{11}) \cdot \mathrm{Im}(Z_{22})}} \qquad (2.5c)$$

where $\omega = 2\pi f$. At this stage, the physical parameters can be further fine-tuned to obtain the optimized design that can best satisfy the requirements.

Step 4: After the physical parameters of the transformer are fixed, the lumped model as shown in Fig. 2.9 can be used for circuit simulation. This lumped model is based on the wideband inductor model from [10], which merges the π models from [11] and [12] and the substrate-coupled model from [13]. Here, the self-inductance and the ohmic loss are modeled by components L_1/L_2 and r_1/r_2, while the parasitic capacitance and the resistive loss of the substrate are modeled by C_{ox1}/C_{ox2}, C_{sub1}/C_{sub2}, and R_{sub1}/R_{sub2}. The magnetic coupling and capacitive coupling between the two coils are modeled by k and C_C, respectively, and the capacitive coupling between the metal traces in the same coil is modeled by C_{m1}/C_{m2}. The substrate-coupled network made of L_{ed1}/L_{ed2} and R_{ed1}/R_{ed2} models the substrate losses due to the eddy current which is increased with frequency. The model parameters are extracted from and fitted to the simulated S-parameter data by using optimizer and fitting tools. Simulations can be used to ensure that the frequency response of the
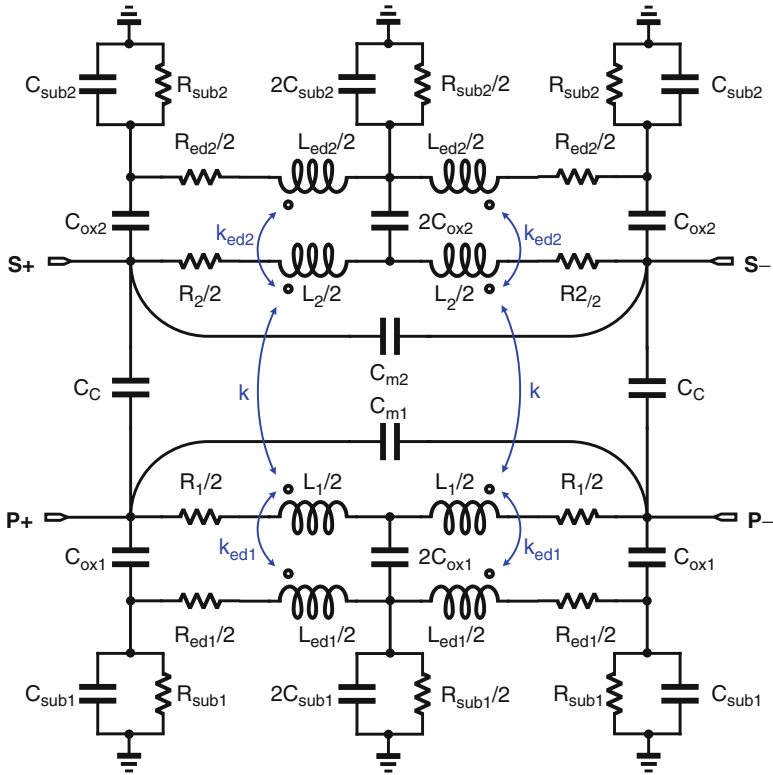
Fig. 2.9 A wideband transformer model for parameter extraction and circuit simulation

model can match well the EM simulation results over a wide frequency range. The transformer model can then be directly used in the time-domain or frequency-domain transistor-level simulation, which enables complete evaluation of the circuit performance. In practice, several iterations with the whole procedure repeated may be necessary to fine-tune the physical and electrical parameters of the transformers until the circuit specifications are satisfactorily met.

Step 5: The transformer testing structure as shown in Fig. 2.10a and its de-embedded structures as shown in Figs. 2.11a and 2.12a can be laid out and fabricated for measurement, characterization, and comparison with the simulation results. The de-embedded open and short structures are employed for de-embedding purpose to eliminate the impacts from the testing PADs and the parasitic metal traces connecting between the transformer core and the testing PADs. For simplicity, the single-ended testing structures with one port of the primary and secondary coils being directly connected to the ground plane are considered here. If a 4-port network analyzer is available, the fully differential testing structures can be constructed in a similar way. The de-embedding principles and procedures in Step 6 can also be applied to the differential testing structures.

a   **b**
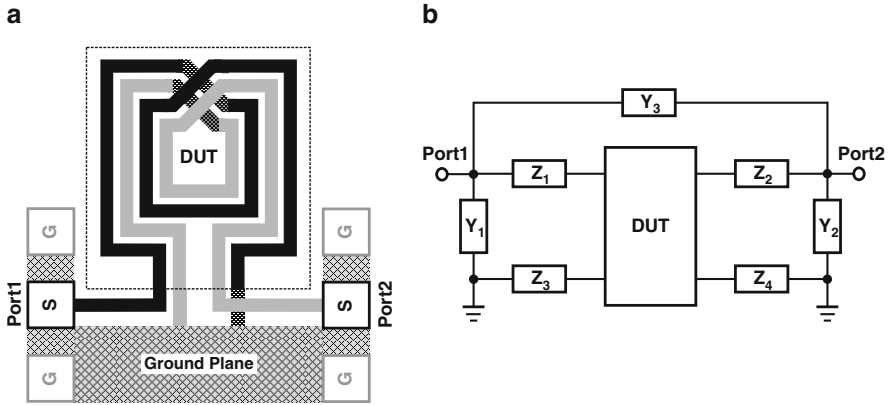
Fig. 2.10 (**a**) Layout and (**b**) equivalent circuit of the transformer testing structure

a   **b**
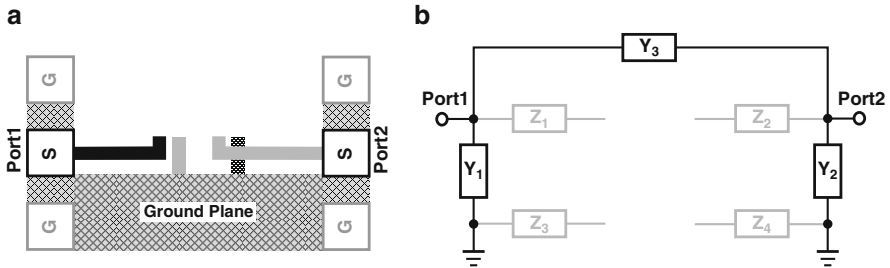
Fig. 2.11 (**a**) Layout and (**b**) equivalent circuit of the open de-embedded structure

a   **b**
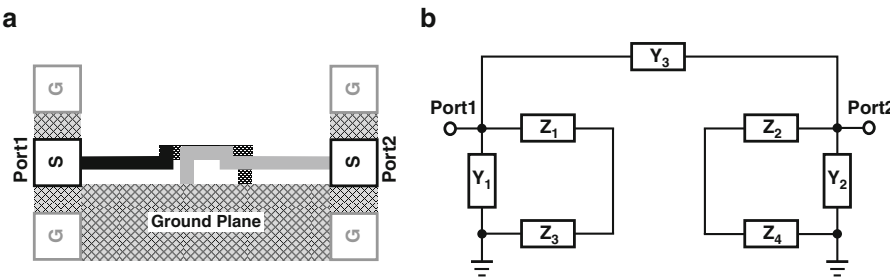
Fig. 2.12 (**a**) Layout and (**b**) equivalent circuit of the short de-embedded structure

Step 6: Using a 2-port network analyzer, the S-parameter of the transformer testing structure (S_{raw}) in Fig. 2.10a and the de-embedded structures (S_{open} and S_{short}) in Figs. 2.11a and 2.12a can be obtained by on-chip probing. The S-parameters (S_{raw}, S_{open}, and S_{short}) can be further converted to the Y-parameters (Y_{raw}, Y_{open}, and Y_{short}) by using the following equations [9]:

$$Y_{11} = \frac{1}{Z_0} \cdot \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \tag{2.6a}$$

$$Y_{12} = \frac{1}{Z_0} \cdot \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \tag{2.6b}$$

$$Y_{21} = \frac{1}{Z_0} \cdot \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \tag{2.6c}$$

$$Y_{22} = \frac{1}{Z_0} \cdot \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \tag{2.6d}$$

Using the Y-parameters, the following de-embedding procedures can be applied to obtain the corresponding electrical parameters of the transformer:

1. Extraction of the parasitic parameters Z_1 to Z_4. According to the equivalent circuits for the open/short de-embedded structures as shown in Figs. 2.11b and 2.12b, the parasitic parameters Z_1 to Z_4 can be extracted by subtracting Y_{open} from Y_{short} to obtain Y_{DE1} first:

$$Y_{DE1} = Y_{short} - Y_{open} \tag{2.7}$$

   and then converting Y_{DE1} to Z_{DE1}. So Z_{DE1} only contains the information of parasitic parameters Z_1 to Z_4.
2. Open de-embedding for measurement data of the transformer testing structure. According to the equivalent circuits for the transformer testing structure and the open de-embedded structures as shown in Figs. 2.10b and 2.11b, the effect of parasitic parameters Y_1 to Y_3 can be removed by subtracting Y_{open} from Y_{raw}:

$$Y_{DE2} = Y_{raw} - Y_{open} \tag{2.8}$$

3. Short de-embedding for measurement data of the transformer testing structure. After converting Y_{DE2} to Z_{DE2}, the effect of parasitic parameters Z_1 to Z_4 can be removed by subtracting Z_{DE1} from Z_{DE2}:

$$Z_{DUT} = Z_{DE2} - Z_{DE1} \tag{2.9}$$

Here, Z_{DUT} represents the impedance of the transformer core after de-embedding. By applying (2.5a–2.5c), the measured self-inductance, quality factor, and coupling coefficient for the transformer core can be obtained.

Step 7: Finally, the measured electrical parameters are compared with the EM simulation results. If the results are not satisfactory, the transformer design would need to be modified by going back to Step 3, starting from the EM simulation of the modified design. The differences between the simulation and measurement results of the transformer can also be utilized to correlate the difference in the measured circuit performance for further optimization.

In the transformer layout in Fig. 2.10a, the primary and secondary ports are located on the same side. If the two ports of the transformer need to be placed on the different sides, the layouts of the testing structures also need to be changed to those as shown in Fig. 2.13.

Fig. 2.13 Layout of testing
structures for the
transformer with two ports
on different sides: (**a**) the
transformer testing
structure, (**b**) the open
de-embedded structure, and
(**c**) the short de-embedded
structure
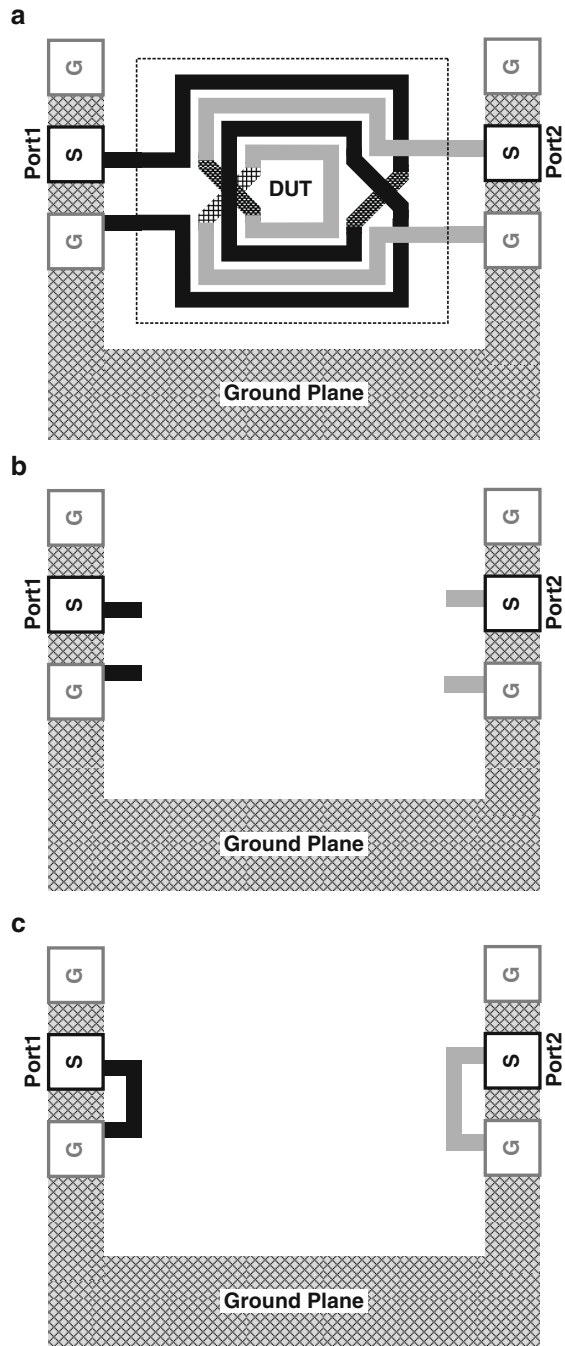
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Chapter 3
Design Considerations for CMOS Voltage-Controlled Oscillators (VCOs)

3.1 Basic Concepts

Voltage-controlled oscillator (VCO) is one of the most critical building blocks in a phase-locked loop (PLL) since it needs to operate at the highest frequency and its phase-noise performance determines the out-of-band phase noise of the PLL at offset frequency larger than the loop bandwidth. Besides, the output frequency range covered by the PLL is also directly limited by the tuning range of the VCO.

3.1.1 Start-Up Oscillation Conditions

Figure 3.1a shows the feedback model of a general oscillator. The closed-loop transfer function is expressed as

$$G(j\omega) = \frac{\text{Out}(j\omega)}{\text{In}(j\omega)} = \frac{H(j\omega)}{1 - H(j\omega)} \tag{3.1}$$

To make the positive feedback system oscillate at a certain frequency ω_0, the amplitude and phase of the open-loop transfer function $H(j\omega)$ must simultaneously meet the conditions (Barkhausen's criterion) expressed as below:

$$|H(j\omega_0)| = 1 \tag{3.2a}$$

$$\angle H(j\omega_0) = 2\pi \cdot n \; ; \quad (n = 0, 1, 2 \ldots) \tag{3.2b}$$

The feedback model for an LC oscillator is shown in Fig. 3.1b. The LC tank serves as a frequency selection network to stabilize the frequency and to provide narrow-band filtering, while the negative G_m cell injects the energy to compensate the loss of the LC tank. Assuming the negative G_m cell provides no phase shift, the phase
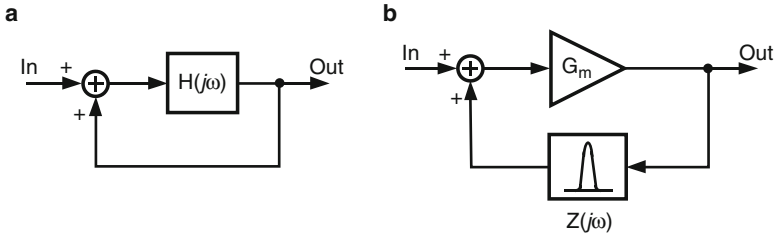
Fig. 3.1 Feedback model of (**a**) a general oscillator and (**b**) an LC oscillator

shift of the LC tank should be zero to enable the oscillation. The start-up condition of the LC oscillator can be expressed as below:

$$G_m \cdot \text{real}\{Z(j\omega_0)\} > 1 \tag{3.3a}$$

$$\text{imag}\{Z(j\omega_0)\} = 0 \tag{3.3b}$$

After the oscillation starts up, the effective G_m drops with the growth of the output amplitude which in turn would be limited due to the nonlinearity of the active devices. As a result, the large signal loop gain $G_m \cdot \text{real}\{Z(j\omega_0)\}$ will always equal to one for stable oscillation.

If the gain and phase conditions in (3.3a) and (3.3b) are met at multiple frequencies, the oscillator may start up with any of these frequencies and have multiple modes of oscillation [1]. For the frequency with larger loop gain, there would be a higher chance for the oscillator to start up because less energy is required. If the loop gains at multiple frequencies are close to each other, concurrent oscillation may even happen if the active devices in the negative-G_m cell meet certain nonlinearity requirement [2–4].

3.1.2   Phase-Noise Definition

In the time domain, an ideal oscillator provides a perfectly periodic output of $V_{out}(t) = V_0 \cos(\omega_0 t)$, with a constant amplitude V_0 and a constant oscillation period $T_0 = 2\pi/\omega_0$. However, in a real oscillator, noise would cause fluctuations on the phase of the output signal, which can be expressed as below:

$$V_{out}(t) = V_0(t) \cos[\omega_0 t + \phi_n(t)] \tag{3.4}$$

where $\phi_n(t)$ represents the small random phase noise that perturbs the zero crossings of $V_{out}(t)$ as shown in Fig. 3.2. This perturbation on the zero crossings will change the oscillation frequency or period, which corresponds to jitter in the time domain.

Since phase perturbation $\phi_n(t)$ is small, it can be assumed that $\cos[\phi_n(t)] \approx 1$ and $\sin[\phi_n(t)] \approx \phi_n(t)$. So (3.4) can be approximated by
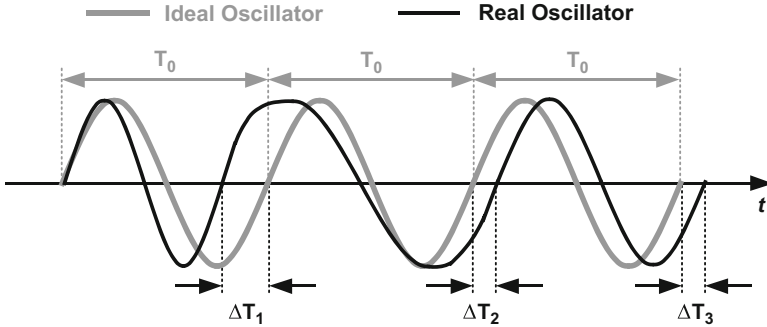
Fig. 3.2 Output waveforms of an ideal and a real oscillator

$$V_{out}(t) \approx V_0(t) \cos(\omega_0 t) - V_0(t) \phi_n(t) \sin(\omega_0 t) \tag{3.5}$$

Since the amplitude is limited by the nonlinearity of the active devices, the fluctuation of $V_0(t)$ is typically small and can be assumed to be constant for simplicity. The instantaneous power of the $V_{out}(t)$ can be obtained by calculating the autocorrelation $E[V_{out}^2(t)]$, and the power spectrum density (PSD) $S_{out}(f)$ of $V_{out}(t)$ can be obtained by applying the Fourier transform to the autocorrelation:

$$S_{out}(t) \approx S_{sig}(\omega) + S_{sig}(\omega) * S_{\phi_n}(\omega) \tag{3.6}$$

where $S_{sig}(\omega) = (V_0^2/2)\delta(\omega - \omega_0) + (V_0^2/2)\delta(\omega + \omega_0)$ is the PSD of the ideal oscillation signal, $S_{\phi_n}(\omega)$ is the PSD of the phase noise $\phi_n(t)$, and the operator $*$ represents convolution in frequency domain.

Figure 3.3 shows the actual spectrum of a typical oscillator. The skirts located on both sides of the desired tone at frequency ω_0 and $-\omega_0$ represent the effect of the frequency fluctuation caused by phase perturbation $\phi_n(t)$. Intuitively, the oscillator is expected to spend more time at frequency ω_0, so the phase noise should be lower as the frequency offset from ω_0 becomes larger. Typically, the phase noise is defined as the ratio of the single-side-band noise power within 1-Hz bandwidth at a frequency offset $\Delta\omega$ away from ω_0 to the carrier signal power as shown in Fig. 3.4:

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left[\frac{P_{noise}(\Delta\omega, 1Hz)}{P_{carrier}}\right] \tag{3.7}$$

which has a unit of "decibels below the carrier per Hertz" or dBc/Hz.
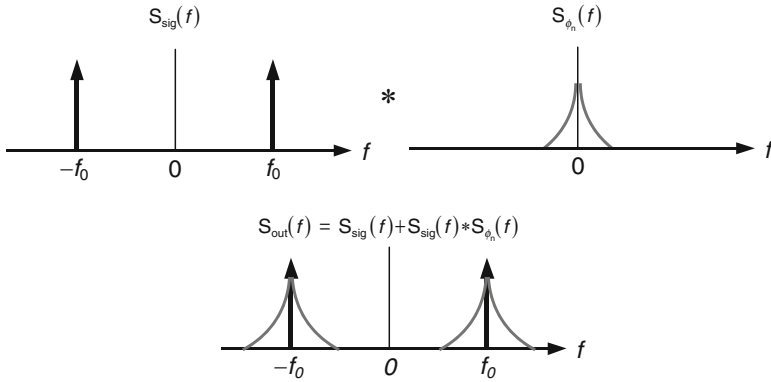
Fig. 3.3 Frequency spectrum of a real oscillator

Fig. 3.4 Definition of phase noise
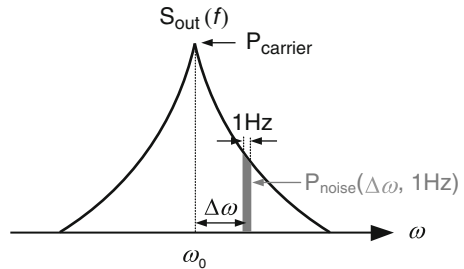
3.1.3   LC-Tank Properties

As shown in Fig. 3.5a, an LC resonant tank is made of an inductor L and a capacitor C with their resistive loss modeled by a parallel tank resistor R_p. The tank impedance Z_t can be expressed as

$$Z_t(\omega) = \frac{1}{\frac{1}{R_P} + j\left(\omega C - \frac{1}{\omega L}\right)} \tag{3.8}$$

According to the phase condition in (3.3b), the resonant frequency ω_0 is

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{LC}} \tag{3.9}$$

From Fig. 3.5b, the amplitude of tank impedance also reaches its maximum (R_p) at ω_0. Since the frequency response of the LC tank exhibits the band-pass characteristic, ω_0 is also called the center frequency.

Denoting the series resistive losses in the actual inductor and capacitor as r_{sL} and r_{sC}, their quality factors are defined as $Q_L = \omega L / r_{sL}$ and $Q_C = 1/(\omega C \cdot r_{sC})$,

Fig. 3.5 (**a**) LC tank with a parallel resistor and (**b**) frequency responses of its amplitude and phase
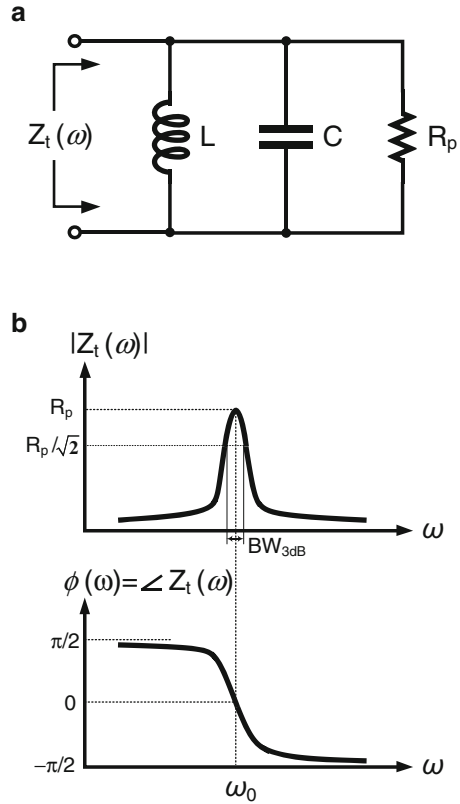
respectively. If the Q_L and Q_C are high $\left(Q_L^2 \gg 1, Q_C^2 \gg 1\right)$, the effective parallel resistances become $R_{pL} \approx Q_L^2 \cdot r_{sL}$ and $R_{pC} \approx Q_C^2 \cdot r_{sC}$. So the total parallel resistance of the LC tank is given by $R_p = R_{pL} || R_{pC}$, and the quality factor of the LC tank (Q_T) can be defined as

$$\frac{1}{Q_T} = \frac{\omega_0 L}{R_P} = \frac{1}{(\omega_0 C) \cdot R_P} = \frac{1}{Q_L(\omega_0)} + \frac{1}{Q_C(\omega_0)} \tag{3.10}$$

In other words, the tank quality factor Q_T equals to $Q_L || Q_C$ and is typically dominated by the inductor Q_L at frequencies below ~20 GHz but by the capacitor Q_C at frequencies above ~40 GHz.

When the operating frequency has a small deviation $\Delta\omega$ from the resonant frequency ω_0, the tank impedance can be approximated as below:

$$Z_t(\Delta\omega) \approx \frac{1}{\frac{1}{R_P} + j\left(\frac{2Q_T}{R_P} \cdot \frac{\Delta\omega}{\omega_0}\right)} \tag{3.11}$$

Equation (3.11) is quite useful when calculating the amplitude and phase of the LC tank at a frequency offset close to ω_0.

It is worth to note that the definition of Q_T in (3.10) only works for the second-order LC tank. For a high-order resonant tank, more general definitions of the tank quality factor can be used [5]:

1. From the perspective of energy, the tank quality factor can be defined as the ratio of the energy stored in the resonant tank to the energy dissipated per cycle:

$$Q_{T\_Energy} = \omega_0 \cdot \frac{E_{stored}}{P_{diss}} \tag{3.12}$$

   From the definition, a high Q_{T_Energy} indicates a small energy loss and thus a small power consumption of the oscillator. In the second-order LC tank, it is easy to prove that Q_{T_Energy} just equals to Q_T defined in (3.10) since $E_{stored} = LI_{max}^2/2$ and $P_{diss} = (R_{sL} + R_{sC})I_{max}^2/2$.

2. From the perspective of band-pass filters, the quality factor can also be defined as the ratio of the center frequency to the 3 dB-bandwidth as shown in Fig. 3.5b:

$$Q_{T\_BW} = \frac{\omega_0}{BW_{3dB}} \tag{3.13}$$

   Here, a high Q_{T_BW} indicates a narrow passband that provides better frequency selection and thus better phase-noise rejection capability. According to (3.11), $BW_{3dB} = \omega_0/Q_T$ if BW_{3dB} is small. So, as long as Q_{T_BW} is high, it can also be well approximated by Q_T defined in (3.10).

3. From the perspective of feedback systems, the quality factor can be defined as a measure of the phase slope of the open-loop transfer function $H(j\omega)$:

$$Q_{T\_PS} = \frac{\omega_0}{2}\left|\frac{d\phi(\omega)}{d\omega}\right|_{\omega=\omega_0} \tag{3.14}$$

   In this definition, a higher Q_{T_PS} indicates a sharper phase response to the frequency change around ω_0, which suggests that if the phase noise causes a deviation from the oscillation frequency, it will tend to return to ω_0 faster, resulting in a "purer" frequency spectrum since the oscillation frequency stays at ω_0 for a longer time [6]. This definition of quality factor is useful in the oscillator design since it can be directly derived from the open-loop transfer function regardless of the types of the resonant tanks employed.

Generally, for an oscillator with a second-order open-loop transfer function as $H(s) = b_1 s/(s^2 + a_1 s + a_0)$, by substituting s with $j\omega$, it can be rearranged as below:

$$H(j\omega) = \frac{j(b_1\omega)}{(a_0 - \omega^2) + j(a_1\omega)} \tag{3.15}$$

The phase of $H(j\omega)$ is $\phi(\omega) = \pi/2 - \tan^{-1}[a_1\omega/(a_0 - \omega^2)]$. According to the Barkhausen criterion, the oscillation frequency $\omega_0 = \sqrt{a_0}$ can be determined by satisfying the phase condition. And the tank quality factor can be obtained by using (3.14)

$$Q_{T\_PS} = \frac{\omega_0}{2}\left|\frac{d\phi(\omega)}{d\omega}\right|_{\omega=\omega_0} = \frac{\sqrt{a_0}}{a_1} \tag{3.16}$$

Again, from (3.11), Q_{T_PS} equals to Q_T when a second-order LC tank is employed.

3.1.4 Frequency Tuning

According to (3.9), the oscillator frequency can be tuned by changing either the tank inductance or capacitance. Generally, varactors (variable capacitors) are most widely used because their capacitance can be tuned by adjusting the control voltage. Figure 3.6a shows the tuning characteristic of a PMOS capacitor by connecting the drain, source, and body nodes of a standard PMOS transistor together. When V_{BG} is lower than the flat-band voltage V_{FB}, the device works in the accumulation mode. Since electrons can move freely at the channel surface, the MOS capacitor just equals to the oxide capacitor $C_{ox} = \mathcal{E}_{ox}(WL)/t_{ox}$, where W and L represent the channel width and length, respectively, while $\mathcal{E}_{ox}$ and t_{ox} represent the oxide permittivity and thickness, respectively. As V_{BG} increases, the PMOS enters the depletion region, and the total capacitor becomes the oxide capacitor in series with the depletion capacitor. When V_{BG} is much larger than the threshold voltage V_{th}, the device is operated in the strong inversion region, where the channel is open to allow the holes from the source and drain to move freely at the channel surface. So the MOS capacitor rises up to C_{ox} again.

In a VCO, since the varactors are connected to the nodes with a larger voltage swing, the effective capacitor is determined by the average capacitance during each cycle. So the monolithic C–V characteristic is necessary to guarantee the monolithic frequency tuning. By preventing the PMOS transistor from entering the inversion or accumulation region, either accumulation-mode MOS (AMOS) varactor or inversion-mode MOS (IMOS) varactor can be realized, respectively. Figure 3.6b shows the cross section of an AMOS varactor. Removing the P+ doping

a

b
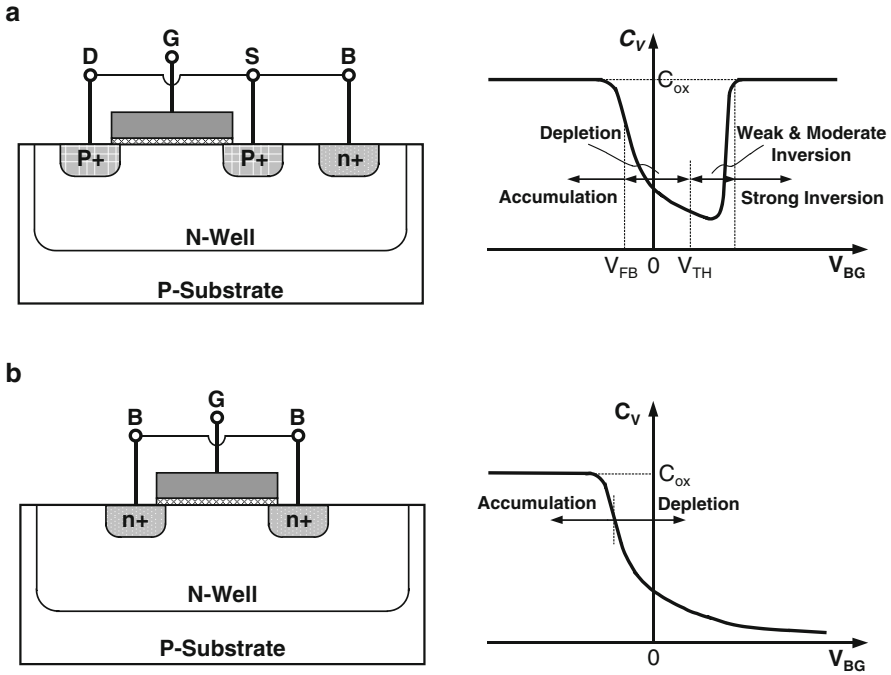
Fig. 3.6 Cross sections and tuning characteristics of (**a**) a pMOS capacitor and (**b**) an AMOS varactor

of source and drain would avoid the inversion mode since there are no suppliers for the holes. In the advanced CMOS technologies, the AMOS varactor is mostly used since it displays better noise performance than both the IMOS and diode varactor [7].

The tuning range of the varactor is determined by the C_{max}/C_{min} ratio. Since most of the C_{min} comes from the overlap capacitors between the gate and the drain/source, the C_{max}/C_{min} ratio can be increased by increasing the channel length at the cost of the Q degradation due to the increased channel resistance.

3.2   Phase-Noise Analysis

VCO phase noise has direct and negative impact on the performance of wireless communication systems. In the receiver path, blockers and interference at some frequency offset from the desired RF frequency would be folded into the frequency band of the desired signal through reciprocal mixing with the phase noise of the VCO at the same frequency offset. On the other hand, in the transmitter path, the LO phase noise would cause spurious emission outside the frequency band of the desired signal, which may become blockers or interference for other receivers

nearby. Besides, the LO phase noise also corrupts phase-modulated signals during frequency up-conversion or down-conversion [6]. So this section will deal with various methods to analyze the phase noise in an LC-VCO, which would serve as guidelines on how to achieve a low phase-noise LC-VCO design.

3.2.1 Linear and Time-Invariant (LTI) Model

In an NMOS LC-VCO shown in Fig. 3.7, the noise comes from the tank loss, the active devices in the cross-coupled pair, and the current bias. From a linear time-invariant model in Fig. 3.8a, the noises from the active devices and the parallel resistor of the tank can be modeled by noise currents $\overline{i_{n,a}}$ and $\overline{i_{n,t}}$, respectively. When the oscillation becomes stable, the effective G_m should be equal to $-1/R_p$ to satisfy the Barkhausen criterion, so the effective impedance seen by both the noise currents is just the impedance of lossless LC tank as shown in Fig. 3.8b. Since $\overline{i_{n,a}}$ and $\overline{i_{n,t}}$ are uncorrelated, the total output noise voltage can be expressed by

$$\begin{aligned}
\overline{v_{n,out}^2} &= \frac{1}{2}\left(\overline{i_{n,a}^2} + \overline{i_{n,t}^2}\right) \cdot |Z_{t\_ideal}(\Delta\omega)|^2 \\
&= \frac{1}{2}F \cdot \overline{i_{n,t}^2} \cdot |Z_{t\_ideal}(\Delta\omega)|^2
\end{aligned} \tag{3.17}$$

where $F = 1 + \overline{i_{n,a}^2}/\overline{i_{n,t}^2}$ is the excess noise factor. Since the amplitude noise is greatly suppressed by the amplitude-limiting mechanism in practical oscillators, the total output noise would be dominated by the phase noise. So according to the equipartition theorem of thermodynamics that noise energy would split equally between phase and amplitude noises [8], a scaling factor 1/2 is added to (3.17). By substituting $\overline{i_{n,t}^2} = 4kT/R_p$ and $|Z_{t\_ideal}(\Delta\omega)| = \left[R_p/(2Q_T)\right] \cdot (\omega_0/\Delta\omega)$ in (3.17) and normalizing the output noise power to the carrier power, the phase-noise equation can be expressed as

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{\overline{v_{n,out}^2}}{P_{sig}}\right) = 10\log_{10}\left[\frac{2kTF}{P_{sig}}\left(\frac{1}{2Q_T}\frac{\omega_0}{\Delta\omega}\right)^2\right] \tag{3.18}$$

From (3.18), the most straightforward way to reduce phase noise is to increase Q_T and the signal power. Furthermore, (3.18) can be rearranged by substituting $P_{sig} = \left(V_0/\sqrt{2}\right)^2/R_p$ and $Q_T = \omega_0 C \cdot R_p$ as below:

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{F}{Q_T V_0^2} \cdot \frac{kT}{C} \cdot \frac{\omega_0}{\Delta\omega^2}\right) \tag{3.19}$$

Fig. 3.7 Current-biased LC-VCO with a NMOS cross-coupled pair and a NMOS tail-biasing transistor

a

b
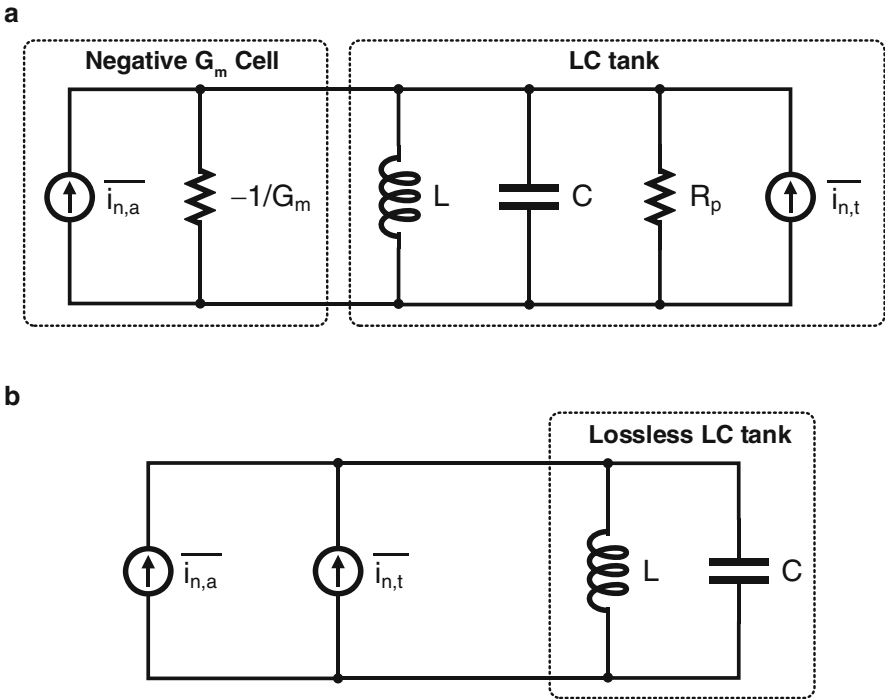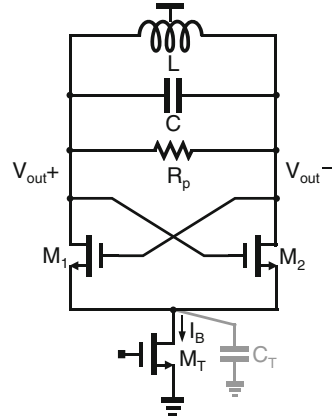
Fig. 3.8 (**a**) Equivalent circuit for the calculation of phase noise from the active devices and the tank loss in a LC-VCO, (**b**) simplified equivalent circuit for stable oscillation

where V_0 is the output amplitude. In other words, the noise contribution from the tank is proportional to kT/C if ω_0 is fixed, which suggests that the combination of a large capacitor and a small inductor would reduce the phase noise if Q_T and V_0 are kept unchanged. However, large power consumption would be required to keep the same V_0 since a small L would decrease the parallel tank impedance R_p.

3.2.2 Linear and Time-Variant (LTV) Model

Despite its simplicity, the time-invariant model has two major limitations when converting the noise from the resonator and from the active devices to the output phase noise:

1. The impulse responses of the phase and amplitude of the output waveform strongly depend on when the noise current pulse $\delta(t - \tau)$ is actually injected into the LC tank. As shown in Fig. 3.9, assuming $V_{out}(t) = V_0 \cdot \cos(\omega_0 t)$ where $T_0 = 2\pi/\omega_0$ is the oscillation period, injection of the noise current $\delta(t - \tau)$ at the time t_1 when $V_{out}(t_1) = 0$ would cause maximum phase shift but with zero amplitude shift. On the other hand, if $\delta(t - \tau)$ is injected at the time t_2 when $V_{out}(t_2) = V_0$, the phase shift would be zero, but the amplitude shift would be maximum. If the injection of $\delta(t - \tau)$ is at times other than t_1 and t_2, both phase and amplitude shift would occur. In other words, the impulse response of the LC tank has the time-variant property. Due to the amplitude-limiting mechanism in practical oscillators, the amplitude shift would decay with time. However, the phase shift would always persist.
2. The amplitude of the current noise from the active device is not constant. As shown in Fig. 3.10 with Φ and φ being the conduction angle of the active devices and the phase of output voltage, respectively, in Region 1 (R1), when $\pi/2 + \Phi/2 < \varphi < 3\pi/2 - \Phi/2$, M_1 is off and produces no noise current. In Region 2 (R2), when $0 < \pi/2 - \Phi/2$ or $3\pi/2 + \Phi/2 < \varphi < 2\pi$, although M_1 is on, its noise current cannot find a path to return to the LC tank since M_2 is off. Assuming that the current source I_B is ideal, which has infinite output impedance, and that the parasitic capacitor at the common source node of M_1 and M_2 is negligibly small, the noise current cannot sink to the ground either. So the noise current would not be converted to the output phase noise. Only in Region 3 (R3), when $\pi/2 - \Phi/2 < \pi/2 + \Phi/2$ or $3\pi/2 - \Phi/2 < 3\pi/2 + \Phi/2$, both M_1 and M_2 are on, and their noise current would be injected into the LC tank and converted to phase noise. The effective noise injected to the tank from $M_{1/2}$ is cyclo-stationary since their amplitude changes with the phase of the output signals within one cycle but stays the same when injected at the same phase for different cycles.

   To handle the time-variant and cyclo-stationary properties of the noise sources in the oscillator, *Harjimiri* and *Lee* proposed a phase-noise theory based on impulse-sensitivity function (ISF) [8]. Assuming that a small current impulse is injected to the oscillator output node at time τ (Fig. 3.9), the resultant output phase shift can be expressed as [9]

$$\Delta\phi = \Gamma(\omega_0\tau)\frac{\Delta V}{V_0} = \Gamma(\omega_0\tau)\frac{\Delta q}{q_{max}} \tag{3.20}$$

where $\Delta q = \Delta V \cdot C$ is the effective charge injected into the tank and C is the tank capacitance, $q_{max} = V_0 \cdot C$ is the maximum charge swing, and $\Gamma(x)$ being periodic
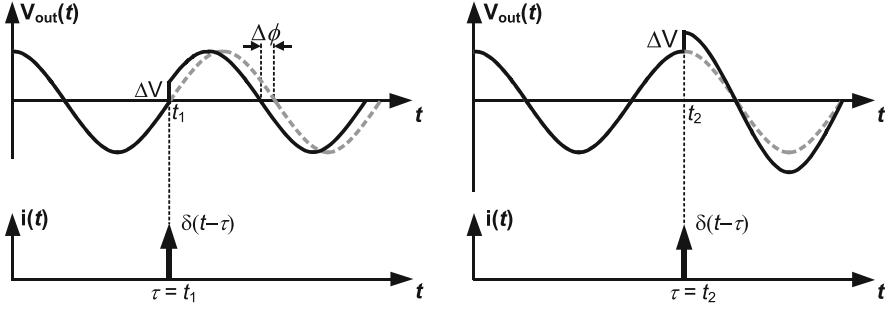
Fig. 3.9 Impulse response of the LC tank
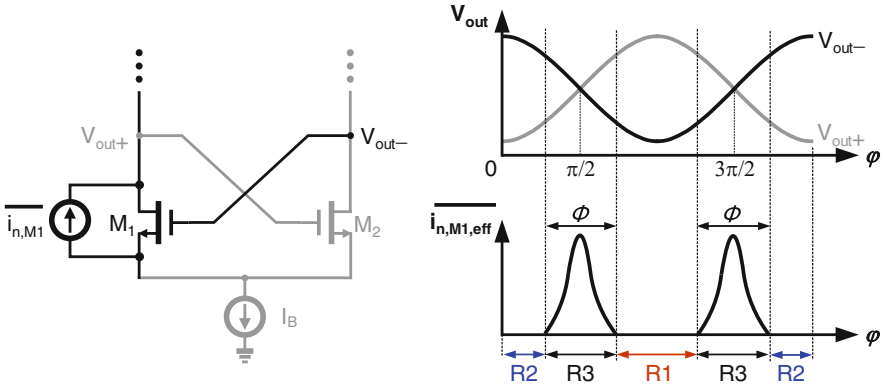
Fig. 3.10 Cyclo-stationary property of the effective noise from the active device M_1

in 2π is a dimension-less time-varying ISF, which is a measure of how sensitive the output phase is to the small charge injected. When normalized to q_{max}, $\Gamma(x)$ is made to be independent of the output amplitude V_0 and can be used to compare the phase noise of oscillators with different output amplitudes.

Since the injection charge Δq due to the noise current impulse is quite small, the system is still linear. As a result, the output excess phase $\phi_n(t)$ can be obtained using the superposition integral [8]

$$\phi_n(t) = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_0 \tau)\alpha(\omega_0 \tau)\, i_n(\tau)d\tau \tag{3.21}$$

where $\alpha(\omega_0 t)i_n(t)$ is the cyclo-stationary noise current injected to the interested node and $\alpha(\omega_0 t)$ represents the noise amplitude modulation in each cycle. Usually, the effective ISF $\Gamma_{eff}(x) = \Gamma(x)\alpha(x)$ is defined to merge the cyclo-stationary effect of the noise current into the ISF.

The noise power spectrum can be directly calculated in the frequency domain [10]. First, the Fourier transform is used to convert the product $\Gamma_{\text{eff}}(\omega_0 t) i_n(t)$ to the convolution $\Gamma_{\text{eff}}(\omega) * I_n(\omega)$ in the frequency domain. Then, the spectrum of $\phi_n(t)$ can be expressed as

$$
\begin{aligned}
\Phi_n(\omega) &= \frac{1}{q_{\max}} \left\{ \frac{1}{j\omega} [\Gamma_{\text{eff}}(\omega) * I_n(\omega)] + \pi\delta(\omega)[\Gamma_{\text{eff}}(0) * I_n(0)] \right\} \\
&= \frac{1}{q_{\max}} \frac{1}{j\omega} [\Gamma_{\text{eff}}(\omega) * I_n(\omega)] \quad (\omega \neq 0)
\end{aligned}
\tag{3.22}
$$

Since $\Gamma_{\text{eff}}(\omega_0 t)$ is also periodic, its spectrum $\Gamma_{\text{eff}}(\omega)$ can be expressed by

$$
\Gamma_{\text{eff}}(\omega) = \sum_{k=-\infty}^{+\infty} a_k \delta(\omega - k\omega_0)
\tag{3.23}
$$

Since the coefficients a_k are real, then $a_k = a_{-k}$. The convolution with the impulse functions of $\Gamma_{\text{eff}}(\omega)$ generates frequency components with frequency shifted by $k\omega_0$ and amplitude amplified of by a_k. Then these frequency components are added together to get the final result of the convolution. As shown in Fig. 3.11, the current noise located at both $k\omega_0 \pm \Delta\omega_0$ ($k = 0, 1, 2$) is converted to equal sidebands at $\pm\Delta\omega_0$ in $S_{\phi_n}(f)$. So the single sideband phase noise can be expressed as

$$
\begin{aligned}
\mathcal{L}(\Delta\omega) &= 10\log_{10}\left(\frac{|\Phi_n(\omega)|^2}{2}\right) \\
&= 10\log_{10}\left[\frac{1}{4q_{\max}^2 \Delta\omega^2} \cdot \frac{\overline{i_n^2}}{\Delta f}\left(\frac{c_0^2}{2} + \sum_{k=1}^{\infty} c_k^2\right)\right]
\end{aligned}
\tag{3.24}
$$

where $c_k = 2a_k = 2a_{-k}$. According to Parseval's relation,

$$
\frac{c_0^2}{2} + \sum_{k=1}^{\infty} c_k^2 = \frac{1}{\pi}\int_0^{2\pi} |\Gamma_{\text{eff}}(\phi)|^2 d\phi = 2\Gamma_{\text{eff,rms}}^2
\tag{3.25}
$$

Equation (3.24) can also be expressed as

$$
\mathcal{L}(\Delta\omega) = 10\log_{10}\left[\frac{\Gamma_{\text{eff,rms}}^2}{2q_{\max}^2 \Delta\omega^2} \cdot \frac{\overline{i_n^2}}{\Delta f}\right]
\tag{3.26}
$$

From the time-variant model, not only the noise in the vicinity of ω_0 contributes to the phase noise, the noise located at low frequencies close to DC as well as at the vicinity of the integral multiples of ω_0 are also folded to the vicinity of ω_0 and also contribute to the phase noise. This noise folding phenomena cannot be captured by the time-invariant model descript in Sect. 3.2.1. Figure 3.12 shows a typical phase-
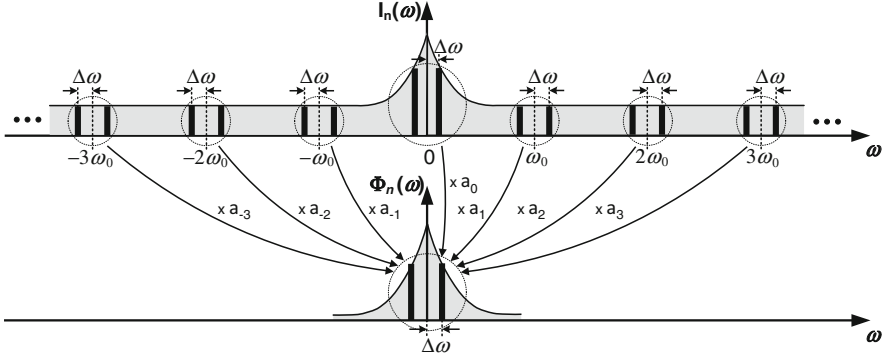
Fig. 3.11 Calculation of the convolution $\Gamma_{\text{eff}}(\omega) * I_n(\omega)$ [8]

noise plot. If the flicker noise of the active devices are considered and used to replace the current noise power at low frequency with $\overline{i_n^2}/\Delta f = K_f/\Delta\omega$, according to (3.24), the phase noise can be expressed as

$$
\begin{aligned}
\mathcal{L}(\Delta\omega) &= 10\log_{10}\left[\frac{1}{4q_{\text{max}}^2\Delta\omega^2}\cdot\frac{c_0^2}{2}\cdot\frac{\overline{i_n^2}}{\Delta f}\right] \\
&= 10\log_{10}\left\{\frac{K_f}{8\pi q_{\text{max}}^2\Delta\omega^3}\cdot\left[\int_0^{2\pi}\Gamma_{\text{eff}}(x)dx\right]^2\right\}
\end{aligned}
\tag{3.27}
$$

where the phase noise becomes proportional to $1/(\Delta\omega)^3$, which also coincides with the measurement results. At moderate offset frequencies $\Delta\omega$, the phase noise is proportional to $1/(\Delta\omega)^2$ as predicted by both the time-invariant and time-variant models since the thermal noise in the active devices becomes dominant. At large $\Delta\omega$, the frequency response of the tank amplitude becomes flat, which indicates that the tank provides weak noise filtering, and the phase noise is limited by the noise floor.

To calculate the total phase noise due to more than one noise sources, $\Gamma_{\text{eff,i}}(\omega)$ from each source to the output excess phase can be calculated separately, and the phase-noise power density $|\Phi_{\text{n,i}}(\omega)|^2$ induced by each noise source can be determined accordingly. If the noise sources are uncorrelated from each other, $|\Phi_{\text{n,i}}(\omega)|^2$ can be directly summed up to obtain the total phase-noise power [8].

3.3   Design Insights Using the Time-Variant Model

Based on the time-variant model, intensive researches have been done to study the LC-VCO phase noise due to different noise sources.
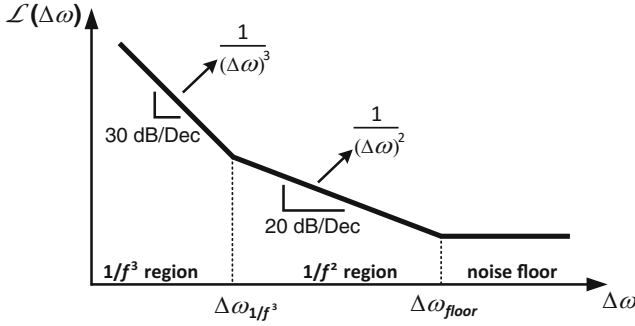
Fig. 3.12 A typical phase-noise plot of LC oscillators as a function of offset frequency (*x*-axis in log scale)

3.3.1   *Phase Noise in 1/f² Region*

Thermal Noise from the Cross-Coupled Transistors

For an LC-VCO with NMOS cross-coupled pair and tail-biasing transistor as shown in Fig. 3.7, if assuming that (1) M_1 and M_2 always stay in the saturation region when turned on, (2) the parasitic capacitor C_T at the common source nodes of M_1 and M_2 is negligibly small, and (3) the output voltage is a sinusoidal waveform, then the phase noise in $1/f^2$ region due to the M_1 and M_2 can be calculated using the ISF method as [11, 12]

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left[\frac{1}{Q_T V_0^2} \cdot \frac{kT}{C} \cdot \frac{\omega_0}{\Delta\omega^2} \cdot \left(1 + \frac{2I_B R_P}{\pi V_0} \cdot \gamma\right)\right] \qquad (3.28)$$

where V_0 is the differential output amplitude and γ is the MOS channel noise factor which is around 2/3 for long-channel devices but may become 2 to 3 or even larger for short-channel devices [13]. Compared with (3.18), the excess noise factor F can be explicitly determined as below:

$$F = 1 + \frac{2I_B R_P}{\pi V_0} \cdot \gamma \qquad (3.29)$$

In the current-limited region where the output amplitude is small, M_T always stays in the saturation region and provides constant I_B during the entire oscillation period as shown in Fig. 3.13a. Since the harmonics of I_B are filtered by the LC tank, the output amplitude V_0 is proportional to the fundamental component I_{B,ω_0} of the bias current and the current efficiency is defined as $\beta = I_{B,\omega_0}/I_B$. So if I_B keeps constant, $V_0 = \beta I_B R_P$ also increases linearly with I_B, and the excess noise factor F is kept constant, which indicates that phase noise can be reduced by increasing I_B at a slope of -20 dB/dec according to (3.28). However, when V_0 is large enough, M_T enters the triode region during the period when either $V_{out}+$ or $V_{out}-$ is close to its
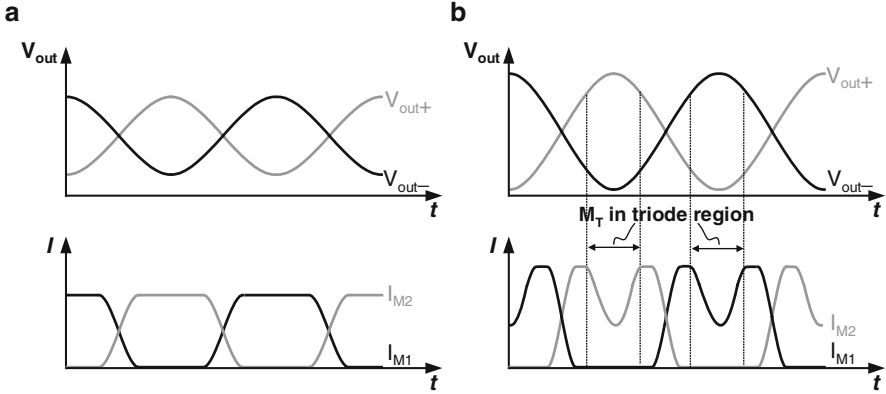
Fig. 3.13 Voltage and current waveforms in (**a**) the current-limited region and (**b**) the voltage-limited region

minimum amplitude as shown in Fig. 3.13b. Eventually V_0 approaches its maximum value, which is around $2V_{DD}$[1] for the NMOS LC-VCO in Fig. 3.7 and cannot be further increased by increasing I_B. So the oscillator enters the voltage-limited region. Since the current efficiency β drops, then F increases, indicating that M_1 and M_2 now contribute more noise and that the phase noise is increased with I_B. As a result, I_B should be properly chosen to bias the oscillator at the boundary between the current-limited and voltage-limited regions to achieve the minimum phase-noise performance, as shown in Fig. 3.14.

In the current-limited region, if the current commutation between M_1 and M_2 is fast, square-wave waveform is reasonable to be assumed with $\beta = 2/\pi$. Together with (3.28), the excess noise factor can be simplified to $F = 1 + \gamma$, which indicates the noise contribution from M_1 and M_2 is independent of the transconductance and thus of the transistor size for the same I_B. Intuitively, as shown in Fig. 3.15, large transistor sizes of M_1 and M_2 will result in a large equilibrium g_m when $I_{M1} = I_{M2}$ and thus large noise power $\overline{i^2_{n,M1}} = 4kT\gamma g_m \Delta f$. On the other hand, large transistor size allows a fast current steering between M_1 and M_2, and the conductance angle Φ is reduced which implies that M_1 and M_2 spend less time injecting noise into the tank. As a result, the total noise energy injected into the tank during each cycle is kept the same [6].

It's worthwhile to note that if the parasitic capacitor C_T is large, even harmonics of the noise current from M_1 will find a path to ground from C_T and thus contribute to the output phase noise even when M_2 is off [14]. Moreover, if M_1 and M_2 enter the deep triode region under large output amplitude V_0, their output impedance will significantly drop. Since M_2 is off, M_1 will be in series with C_T and effectively a low Q capacitor will be added in parallel with the tank, which degrades the tank Q and thus the output phase noise. So it is important to keep C_T small.

---

[1] The exact value of the maximum V_o should be $2(V_{DD} - V_{D,MT})$, where $V_{D,MT}$ is the minimum drain voltage of M_T. The maximum V_o approaches $2V_{DD}$ for a large V_{DD}.

Fig. 3.14 Output amplitude and phase noise as functions of I_B
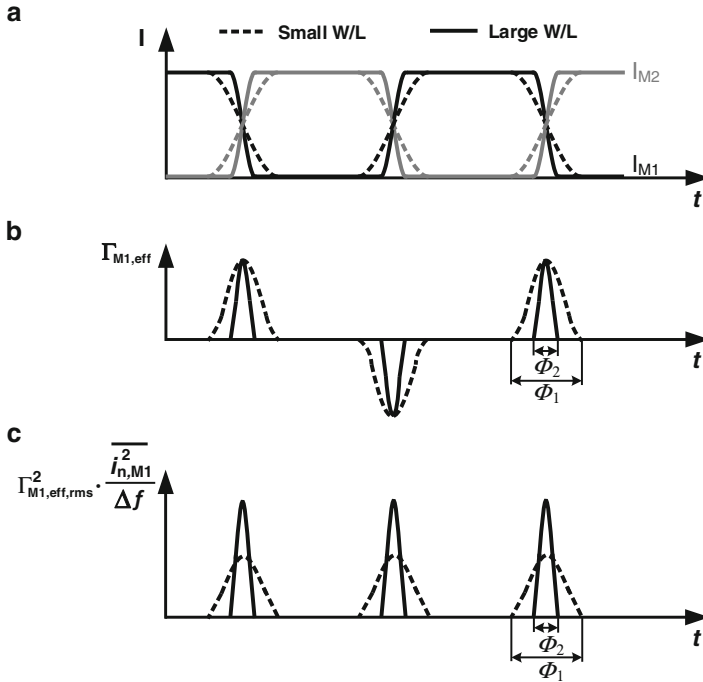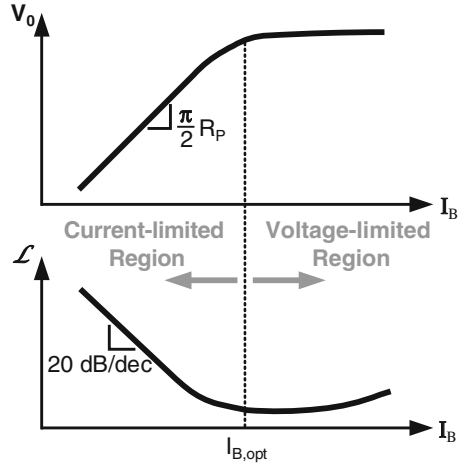
Fig. 3.15 Waveforms of (**a**) the drain currents in M_1 and M_2, (**b**) the effective ISF for the current noise from M_1, and (**c**) the effective PSD for the current noise from M_1

Thermal Noise from the Tail-Biasing Transistor

The noise current from tail-biasing transistor M_T experiences frequency translations when converted to the phase noise [6, 14]. Assuming the V_0 is large and the currents commutated by M_1 and M_2 are close to the square wave, the noise current from M_T is mixed with the harmonic tones of the square wave through the cross-coupled pair. Since the square wave contains only odd harmonics, only the noise current around DC and even harmonics are translated to the frequency in the vicinity of ω_0. At low frequencies, flicker noise only modulates the output amplitude after frequency up-conversion and can be ignored at this stage[2]. The even harmonic components of the noise current are down-converted, which results in both amplitude and phase noise in the vicinity of ω_0. If the noise contribution from M_T is also considered, the excess noise factor F can be revised by adding a third term [11]:

$$F = 1 + \frac{2I_B R_P}{\pi V_0} \cdot \gamma + \eta \gamma g_{mT} R_p \qquad (3.30)$$

where the scaling factor $\eta = 2\Gamma^2_{tail,rms}(\Phi)$ depends on the current conductance angle Φ. From the plot of $\eta(\Phi)$ in Fig. 3.16, $\eta(\Phi)$ and thus the phase noise from M_T can be reduced by making M_1 and M_2 switch more softly. However, large Φ makes the current flowing through M_1 or M_2 deviate from the square-wave assumption and causes the current efficiency β to drop, which in turn reduces V_0 and increases the noise contribution from M_1 or M_2. Consequently, the total output phase noise would increase for large Φ. Another way to reduce the noise contribution from M_T is to reduce its transconductance g_{mT} while still keeping the same bias current, which can be realized by increasing its overdrive voltage or reducing the W/L ratio for the same bias current. However, increasing overdrive voltage would result in a large $V_{D,MT}$, which decreases the maximum V_o that can be achieved.

3.3.2 Phase Noise in 1/f³ Region

According to the time-variant model, the flicker noise of MOS transistors is up-converted to the vicinity of ω_0 and causes the close-in phase noise proportional to $1/(\Delta\omega)^3$. In this section, flicker noise up-conversion mechanisms from the cross-coupled pair and the tail-biasing transistor in the current-biased VCO (Fig. 3.7) are discussed.

---

[2] As will be discussed later, the amplitude noise can also convert to phase noise if a varactor is employed for frequency tuning in a VCO.
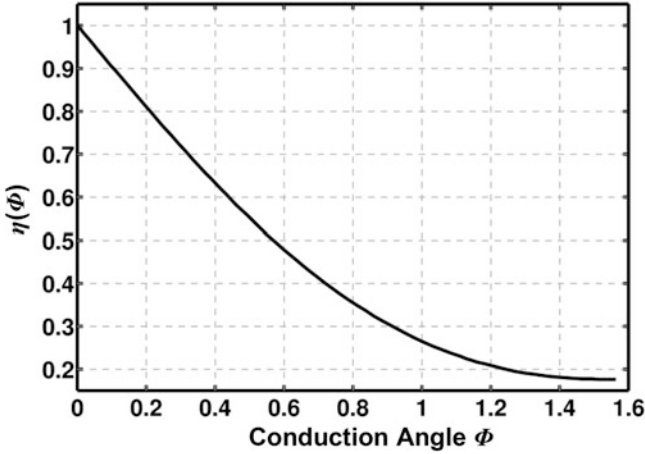
Fig. 3.16 Tail current phase noise scaling factor $\eta(\Phi)$ as a function of Φ [11]

Up-Conversion of Flicker Noise from the Cross-Coupled Transistors

In the previous analysis of the phase noise induced by the thermal noise of the cross-coupled transistors, only the currents generated by the cross-coupled transistors at fundamental frequency are considered, and the waveform of the output voltage is assumed to be pure sinusoidal. However, the MOS transistor is a nonlinear device, and its drain current is rich of harmonics, which cannot be ignored when analyzing the effect of flicker noise.

As shown in Fig. 3.17, the fundamental component of the drain current $I_{D1}(I_{D2})$ only flows through the parallel tank impedance R_p since the tank inductance and capacitance are resonant at the fundamental frequency. But the harmonic currents will flow through the tank capacitors since the capacitor exhibits lower impedance than the inductor at high frequencies. As a result, the electrical energy stored in the capacitors would be larger than the magnetic energy stored in the inductor. So the resonant frequency of the LC tank has to decrease to guarantee the resonance condition that the average electrical energy in the capacitor and magnetic energy in the inductor are kept the same. The shift of resonant frequency due to the current harmonics is commonly referred to as the Groszkowski effect [15]. If the drain current $I_{D1}(I_{D2})$ is constant, then this frequency shift is static. But in the presence of flicker noise, the amplitude and thus the switching time of $I_{D1}(I_{D2})$ will change with time, which causes the fluctuation of the ratios between the harmonic currents and fundamental current. As a consequence, the flicker noise will modulate the oscillation frequency and contribute to the phase noise in $1/f^3$ region [14, 16]. Usually, the second harmonic current is the dominant source for the frequency shift, since the flicker noise in $M_1(M_2)$ modulates the voltage waveform at the common source node, which induces a second harmonic current in the parasitic capacitors C_{gs} of $M_1(M_2)$ that directly injects into the tank [17].
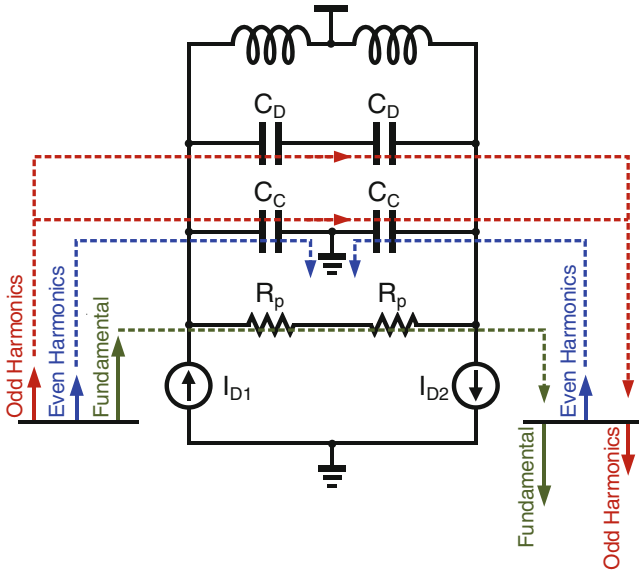
Fig. 3.17 Paths of the tank currents at the fundamental and harmonic frequencies [17]

In the NMOS LC-VCO as shown in Fig. 3.7, if an ideal current source is used, the common source node of M_1 and M_2 is floating so that the second harmonic current is prevented from flowing into the ground. However, when a real transistor M_T is used as current source, second harmonic current always exists due to its finite output impedance and the presence of C_T. So one effective way to reduce flicker noise contribution from $M_1(M_2)$ by eliminating the effect of second harmonic current is to insert an inductor L_F between the common source node and M_T [18], as shown in Fig. 3.18. The L_F is chosen to be resonant with the parasitic capacitors C_S and C_T at twice the oscillation frequency $2f_0$. So a high impedance Z_F of the common source node at $2f_0$ is created to block the second harmonic current. Besides reducing the flicker noise from $M_1(M_2)$, the advantages of the tail filter also include (1) preventing the tank Q degradation when $M_1(M_2)$ enters into the triode region and (2) allowing the use of a large C_T to eliminate the thermal noise from M_T at $2f_0$.

Up-Conversion of Flicker Noise from the Tail-Biasing Transistor

Let's consider the situation when a varactor is included in the LC tank for frequency tuning. If the voltage dependence of C_V only has odd-order terms, e.g., $C_V = C_{V0}(1 + \alpha V_{out} + \alpha V_{out}^3 + \cdots)$, the C–V characteristic of the varactor is symmetrical to the point $(V_{out,DC}, C_{V0})$ as shown in Fig. 3.19a, where $V_{out,DC}$ is

Fig. 3.18 NMOS LC-VCO
with tail filter [18]
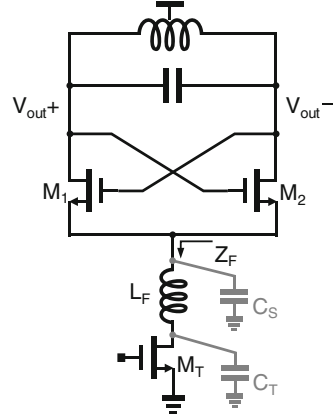
the output DC voltage and C_{V0} is the varactor capacitance when $V_{ctrl} = V_{out,DC}$. If the output voltage is a sinusoid waveform, the average capacitance of varactor defined as $C_{V,avg} = (1/T) \int_0^T C_V(t)dt$ always equals to C_{V0} even if the output amplitude is changed. So there is no noise conversion from amplitude modulation (AM) to phase modulation (PM). However, if the voltage dependence of C_V includes some even-order terms, e.g., $C_V = C_{V0}(1 + \alpha V_{out} + \alpha V_{out}^2 + \cdots)$, the C–V characteristic of the varactor would not be symmetrical to the point ($V_{out,DC}$, C_{V0}) anymore as shown in Fig. 3.19b. As a result, the average capacitance $C_{V,avg}$ would deviate from C_{V0} and change with the output amplitude. Accordingly, the oscillation frequency would be modulated by the fluctuation of the output amplitude which indicates AM-to-PM noise conversion. Since the flicker noise of M_T modulates the output amplitude after frequency up-conversion, it also contributes to the output phase noise at $1/f^3$ region through the asymmetric C–V characteristic of a varactor. Besides the varactor, the nonlinear parasitic junction capacitors from M_1 and M_2 in parallel with the LC tank also cause the AM-to-PM noise conversion due to the same mechanism.

To reduce the phase noise caused by the AM-to-PM modulation, it is better to use the region of the C–V curve that has a C–V relationship similar to that shown in Fig. 3.19a, which can be realized by properly choosing the voltage bias V_B at the gate as shown in Fig. 3.20a. Furthermore, the contribution of capacitance in an LC tank from both the varactor and the parasitic capacitor must be minimized. To reduce the varactor size while still covering enough frequency range, a switch-capacitor array (SCA) in Fig. 3.20a can be employed for coarse frequency tuning [19, 20]. As such, only a small varactor is needed for fine-tuning to cover the frequency gap between the adjacent frequency bands as shown in Fig. 3.20b. Here the capacitors and switches are sized to be binary-weighted to reduce the number of segments and the control complexity. For switch transistor, a minimum channel length is preferred to reduce both on resistance R_{on} and parasitic junction capacitor
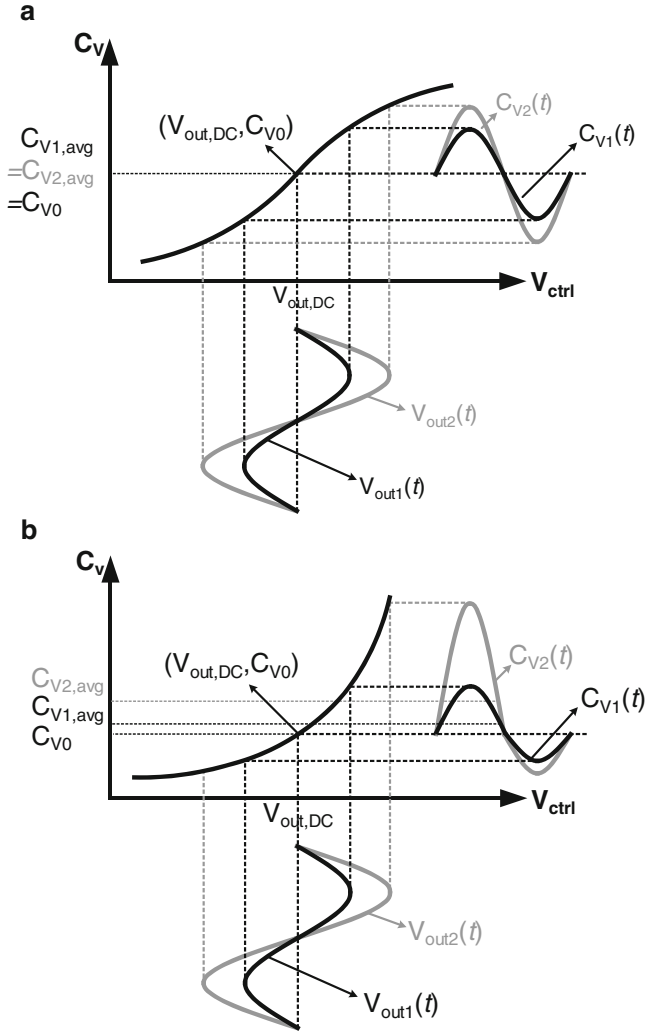
Fig. 3.19 Average capacitance of a varactor with (**a**) a C–V curve containing only odd-order terms and (**b**) a C–V curve containing also even-order terms

C_d at the drain of the turned-off switch. So with the scaling down of CMOS process, a larger capacitor ratio C_{on}/C_{off} between the on and off states of the SCA can be achieved when the Q of SCA is kept the same. It is worthwhile to note that at high frequencies when most switches in the SCA are turned off, the nonlinear parasitic capacitors C_d may dominate the tank capacitance, and the VCO may suffer from larger AM-to PM conversion than at low frequencies when most of the switches are turned on and the tank capacitance is dominated by fixed capacitors C_a. As a result, the phase-noise plot at high-frequency end is expected to have a higher flicker noise corner frequency $\Delta\omega_{1/f^3}$ (Fig. 3.12), which would degrade the close-in phase-noise performance.

a

b
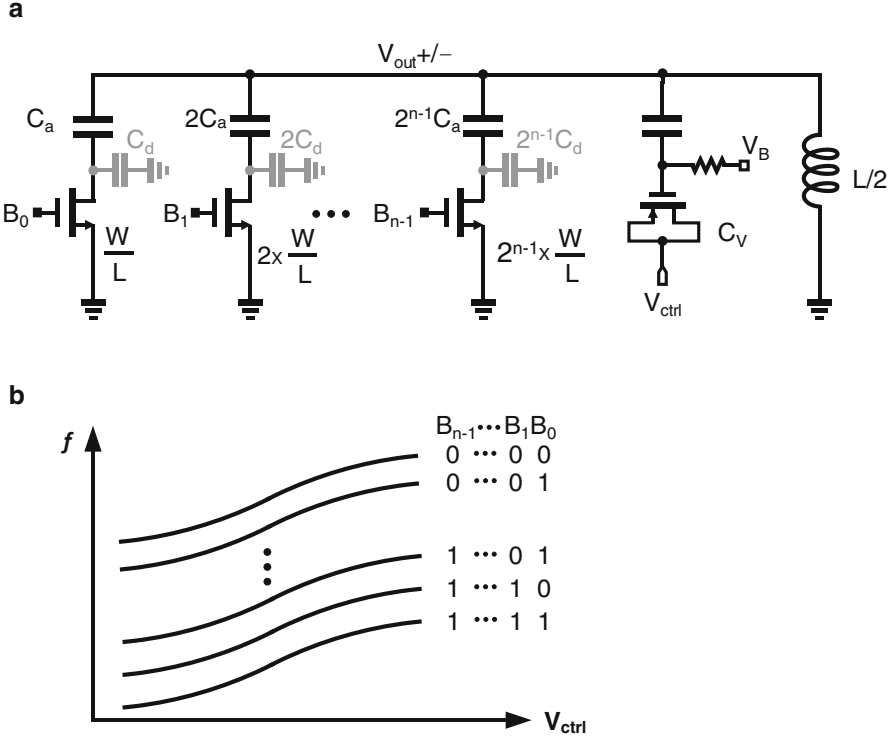
Fig. 3.20 (**a**) Schematic and (**b**) frequency tuning curves of combing a binary-weighted SCA and a varactor

3.3.3   Comparison of Different LC-VCO Topologies

Figure 3.21a shows the schematic of a current-biased LC-VCO with complementary cross-coupled pairs, which employs both NMOS and PMOS cross-coupled pairs to provide the required negative transconductance for oscillation. For the same bias current I_B, the complementary LC-VCO can achieve twice the output amplitude compared with the NMOS LC-VCO in Fig. 3.7, assuming both are in the current-limited region [21]. In the current-limited region, with the similar assumptions for the NMOS LC-VCO in Sect. 3.3.1, the phase noise of the complementary LC-VCO in $1/f^2$ region due to the cross-coupled transistors can be obtained with the help of the LTV model [22]:

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left[\frac{1}{Q_T V_0^2} \cdot \frac{kT}{C} \cdot \frac{\omega_0}{\Delta\omega^2} \cdot \left(1 + \frac{\gamma_n + \gamma_p}{2}\right)\right] \qquad (3.31)$$

where γ_n and γ_p are the channel noise factor for NMOS and PMOS transistor, respectively. If $\gamma_n = \gamma_p$, (3.31) becomes exactly the same with (3.28) in the
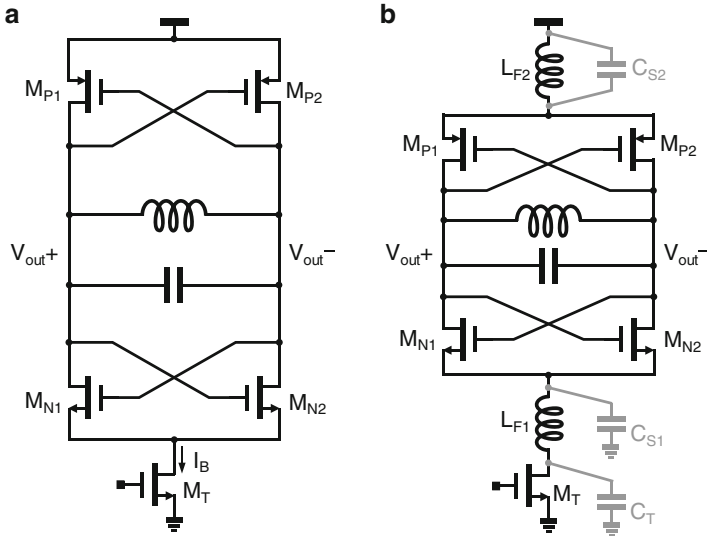
Fig. 3.21 (**a**) Complementary LC-VCO, (**b**) complementary LC-VCO with tail filter [23]

current-limited region when the current commutated by the cross-coupled pairs can be well approximated by a square wave. So the phase noises of both NMOS and complementary LC-VCO only depend on the output amplitude assuming the same LC tank is used. Thus, the complementary LC-VCO can achieve a phase noise 6 dB lower than the NMOS LC-VCO given the same current, assuming both are in the current-limited region. However, with both PMOS and NMOS cross-coupled pairs, the maximum differential output amplitude in the complementary LC-VCO is limited to only V_{DD}, which is only half of that in the NMOS LC-VCO. So the minimum phase noise achieved by the NMOS LC-VCO is 6 dB lower than that by the complementary LC-VCO, when both are biased at the boundary between the current-limited region and the voltage-limited region. Besides, for the same supply voltage, the complementary LC-VCO is easier to start up since it requires only half the current to achieve the same g_m compared with the NMOS LC-VCO. As a consequence, the complementary topology is suitable for the low-power applications with relaxed phase-noise requirements. On the other hand, NMOS LC-VCO is more suitable for the application requiring low supply voltage.

Similar to the NMOS VCO, the tail filter can also be applied in the complementary LC-VCO to reduce the flicker noise from $M_{N1}(M_{N2})$ and $M_{P1}(M_{P2})$ as well as to eliminate the thermal noise of M_T at $2f_0$, as shown in Fig. 3.21b [23].
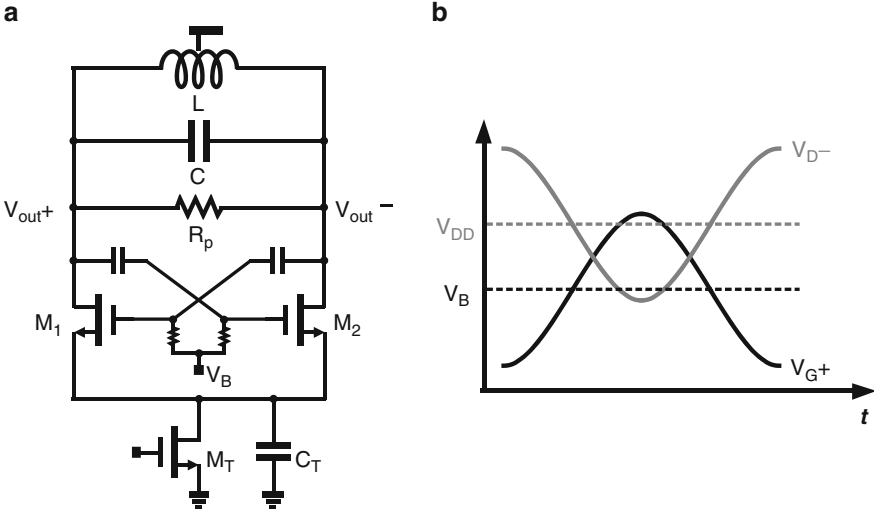
Fig. 3.22 (**a**) Schematic and (**b**) voltage waveforms of the class-C VCO

Figure 3.22a shows the schematic of a class-C VCO [24]. By intentionally adding a large capacitor C_T to the common source node and bias the cross-coupled pair in the class-C mode, the waveforms of the currents commutated by M_1 and M_2 are shaped to narrow pulses as shown in Fig. 3.23b [25]. If the current conduction angle Φ is small and $M_1(M_2)$ stays in saturation region, the amplitude of the fundamental current harmonic I_{ω_0} is close to the bias current I_B, which results in an improved current efficiency close to unity. Since the current efficiency of the class-B VCO in Fig. 3.7 is $2/\pi$, the class-C VCO can theoretically achieve a 3.9 dB lower phase noise given the same bias current I_B when both the class-C and class-B VCO work in the current-limited region [24]. Besides, a large C_T also prevents the noise up-conversion in $1/f^2$ region by bypassing the thermal noise of M_T in the vicinity of even-order harmonics of ω_0 to ground.

However, if $M_{1/2}$ in the class-C VCO enters the deep triode region, the current waveforms are no longer narrow pulses as shown in Fig. 3.23c, so the current efficiency β in turn drops. Even worse, the low Q tail capacitor will load the tank and degrade the phase noise severely. According to Fig. 3.22b, the maximum differential output amplitude V_o that still keeps $M_1(M_2)$ in the saturation region can be calculated as

$$V_o \leq V_{DD} - V_B + V_{th} \tag{3.32}$$

If $V_B = V_{th}$, the maximum V_o equals to V_{DD}, which is only half of that in the class-B NMOS VCO.

Fig. 3.23 Waveforms in a class-C VCO: (**a**) output voltage waveforms, (**b**) current waveforms if transistors are in saturation region, and (**c**) current waveforms if transistors are in triode region [24]
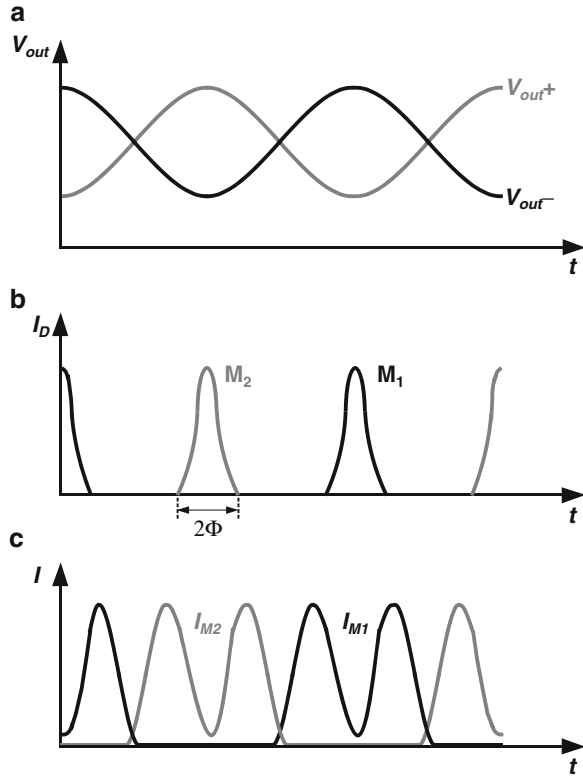
3.3.4 VCO Figure of Merit

To compare the phase-noise performance of VCOs that consumes different power and operates at different frequencies, the figure of merit (FoM) is defined as [26]

$$\text{FoM} = -\mathcal{L}(\Delta\omega) - 10\log_{10}\left[\frac{P_{\text{diss}}}{1\text{ mW}}\left(\frac{\Delta\omega}{\omega_0}\right)^2\right] \tag{3.33}$$

where P_{diss} is the power consumption of the VCO normalized to 1 mW to keep the FoM the same unit with the phase noise. Here, a high FoM represents better VCO performance when the facts of phase noise, power, and oscillation frequency are all taken into account. It is worthwhile to note that only the phase noise in $1/f^2$ region is normalized with offset frequency $\Delta\omega$ according to (3.33). As such, the FoM would drop significantly at small offset frequency $\Delta\omega$ for the same oscillation frequency and power since $1/f^3$ noise becomes dominant. If substituting $\mathcal{L}(\Delta\omega)$ with (3.19), the equation of FoM can be rewritten as

Table 3.1 Comparison of the best phase noise and FoM for different LC-VCO topologies

LC-VCO topology	F	β	Max. V_0	Min. PN	Best FoM
Class-B NMOS (with tail filter)	$1 + \gamma_n$	$2/\pi$	$\sim 2V_{DD}$	$\mathcal{L}_0$	FoM_0
Class-B complementary (with tail filter)	$1 + (\gamma_n + \gamma_p)/2$	$4/\pi$	$\sim V_{DD}$	$\mathcal{L}_0 + 6$ dB	FoM_0
Class-C NMOS	$1 + \gamma_n$	1	$\sim V_{DD}$	$\mathcal{L}_0 + 6$ dB	$FoM_0 - 1$ dB

$$\text{FoM} = -10 \log_{10} \left[\frac{kT}{1\text{mW}} \cdot \frac{F}{\beta Q_T^2} \cdot \frac{V_{DD}}{V_0} \right] \qquad (3.34)$$

where $\beta = I_{\omega_0}/I_B$ is the current efficiency. It can be seen that the FoM in (3.34) is independent of the oscillation frequency, offset frequency, and current consumption, which allows a fair comparison of different VCO designs and provides some design insights. Since the FoM is inversely proportional to Q_T^2, increasing the tank quality factor is the most effective way to improve the FoM. At frequencies below 10 GHz, Q_T is dominant by the inductor quality factor which depends on process parameters, such as the metal thickness, the distance between the metal to the substrate, and the resistivity of the substrate. The noise excess factor F and current efficiency β are related to the VCO topology used. Besides, for a chosen VCO topology, the best FoM is achieved by biasing the VCO for the maximum output amplitude.

Table 3.1 lists the minimum phase noise and best FoM that can be achieved in the $1/f^2$ region for different LC-VCO topologies. Since in both class-B VCO with tail filter and class-C VCO, a large C_T can be used, the noise from the tail transistor M_T can be ignored[3] and only the noise from the tank loss and cross-coupled transistors are considered. It can be seen although the class-C NMOS VCO has better current efficiency, the best FoM is still 1 dB worse than that of the class-B NMOS VCO with tail filter due to the degradation of the maximum output amplitude. However, the tail filter requires extra inductors and thus large chip area. On the other hand, without the tail filter, the phase noise of the class-B VCOs would degrade severely due to the noise from the tail transistor M_T. So it is expected that the best FoM of class-B VCO without tail filter would be worse than that of the class-C VCO.

To include the frequency tuning range in the comparison, the figure of merit with tuning range (FoM_T) is also frequently used:

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[3] Here the effect of AM-PM noise conversion is ignored for simplicity so that the flicker noise from the MT does not contribute to the phase noise, which is a well approximation as long as the varactor is kept small.

$$\text{FoM}_\text{T} = \text{FoM} - 20\log_{10}\left[\frac{\text{FTR}(\%)}{10}\right] \qquad (3.35)$$

where FTR is the frequency tuning range in percentage.

3.4   Quadrature VCOs

Modern wireless transceiver architectures require quadrature LO signals for both up-conversion and down-conversion mixing [6]. To generate the quadrature signals, three techniques are commonly used as follows: (1) a single-phase oscillator followed by a polyphase filter [27], (2) a single-phase oscillator operating at twice the desired LO frequency followed by a quadrature frequency divider [28], and (3) quadrature oscillators [29]. A polyphase filter using passive RC network requires cascading of multiple stages to achieve a wide bandwidth with sufficient quadrature accuracy, which would result in high loss of the LO signals. Oscillators operating at twice the LO frequency suffers from high power, reduced frequency tuning range, and small signal amplitude. Furthermore, the quadrature frequency divider consumes significant extra power. Finally, these drawbacks are further exacerbated at mm-Wave frequencies and beyond. As a result, the quadrature LO generation scheme using quadrature VCOs (QVCOs) becomes more attractive at high frequencies. Figure 3.24 shows the well-known parallel-coupled QVCO (P-QVCO) architecture that couples two LC-VCOs using additional coupling transistors M_{3-4} and M_{7-8} [29].

In the P-QVCO, since the total current injected into the tank equals to the superposition of the currents from the cross-coupled pair and the coupling transistor, the tank voltage and tank current is no longer in phase and there exists a phase shift α between them as shown in Fig. 3.25a. To guarantee the total phase shift of the loop to be zero, the tank must provide an additional phase shift $-\alpha$. As shown in
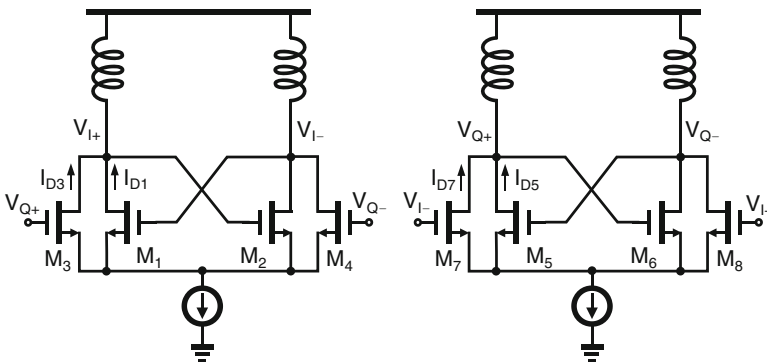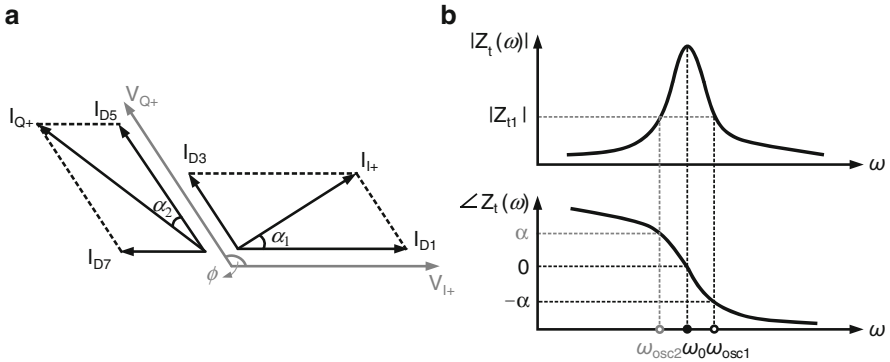

Fig. 3.24 Schematic of the parallel-coupled QVCO (P-QVCO) [29]

Fig. 3.25 (**a**) The relationship between current and voltage phasors in a P-QVCO; (**b**) frequency response of the LC-tank impedance
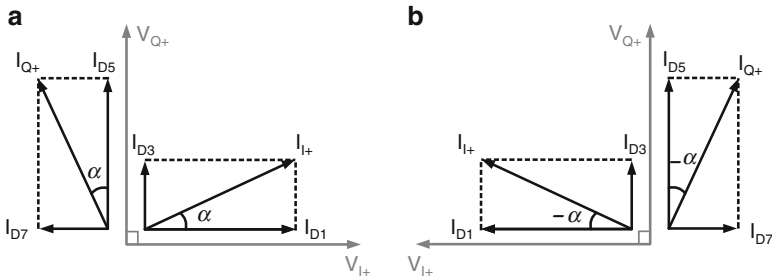
Fig. 3.26 Current phasors of the P-QVCO: (**a**) V_I leads V_Q; (**b**) V_I lags V_Q

Fig. 3.25b, the oscillation frequency ω_{osc1} would need to deviate from the tank resonant frequency $\omega_0 = \sqrt{LC}$ and is eventually determined by both the phase shift $-\alpha$ and the phase response of the tank. The reason that the output voltages V_I and V_Q are quadrature with each other can be explained by the phase relationship of the current phasors as shown in Fig. 3.25a. First, we assume that the phase difference ϕ between V_I and V_Q can be an arbitrary value. Since I_{D1} (I_{D5}) is always in phase with V_{I+} (V_{Q+}), the tank current I_{I+} (I_{Q+}) has a phase shift $\alpha_1(\alpha_2)$ with the tank voltage V_{I+} (V_{Q+}). If the two oscillators are synchronized, they should have the same oscillation frequency. If the two LC tanks are identical, α_1 must equal to α_2 to keep the same oscillation frequency of two oscillators. Since the transistor sizes of M_{1-2} and M_{5-6} (M_{3-4} and M_{7-8}) are the same, $|I_{D1}| = |I_{D5}|$ and $|I_{D3}| = |I_{D7}|$. To guarantee the condition that $\alpha_1 = \alpha_2$, the phase difference ϕ between V_{I+} and V_{Q+} must be $\pi/2$ as shown in Fig. 3.26a, which forces the quadrature relationship between the output voltages V_I and V_Q.

One thing to be noted is that the phase sequence between V_I and V_Q is not well defined if the frequency response of tank impedance is symmetric with ω_0 because the situation that V_I lags V_Q as shown in Fig. 3.26b can also satisfy the phase

Fig. 3.27 Variation of
phase shift α due to the
flicker noise from the
coupling transistors
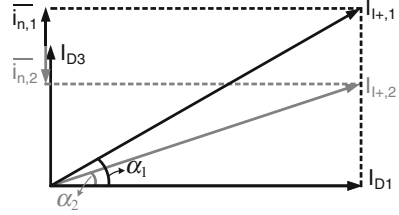
condition and guarantee the oscillation at a lower frequency ω_{osc2} as shown in Fig. 3.25b. The detailed analysis on this bimodal oscillation phenomenon can be found in [30], which suggests that the ambiguity on the oscillation frequency (ω_{osc1}, ω_{osc2}) and IQ phase sequence can be eliminated by adding sufficient phase shift in the coupling paths.

In the P-QVCO, since extra coupling transistors are employed, they would inevitably consume extra power and contribute noise to the VCO output. In the $1/f^2$ region of phase noise, the contribution from thermal noise of the coupling transistors behaves like that from the cross-coupled transistors. By defining the coupling strength $m = I_{D3}/I_{D1}$ as the ratio between the quadrature and in-phase currents injected into each tank, the excess noise factor F in (3.19) increases to (1 + m) times of that in a single-phase cross-coupled VCO [31]. Moreover, since the oscillation frequency ω_{osc} of the P-QVCO in Fig. 3.24 deviates from the resonant frequency ω_0, the effective tank Q_T at ω_{osc} is degraded to around $1/\sqrt{1+m^2}$ times of that at ω_0 [32], which further degrades the phase noise. Although the excess noise factor F and tank Q_T can be improved by reducing the coupling strength m, IQ phase accuracy would suffer in presence of mismatches of the tank components and the active transistors between the two coupled oscillators.

In the $1/f^3$ region of phase noise, as shown in Fig. 3.27, the flicker noise from the coupling transistors changes the amplitude of the coupling current slowly which causes the variation of the phase shift α between the tank voltage and current and thus modulates the oscillation frequency ω_{osc} of the QVCO. This kind of flicker noise up-conversion mechanism does not happen in a single-phase LC oscillator since the tank voltage and current are always in phase. As a result, the corner frequency $\Delta\omega_{1/f^3}$ between the $1/f^3$ and $1/f^2$ region (Fig. 3.12) is increased compared to that of a single-phase LC oscillator [33], which indicates degraded close-in phase-noise performance in the P-QVCO.

Particularly, for the P-QVCO, the coupling transistors consume extra currents, which only induce the frequency shift and have no contribution to the output amplitude since they are in quadrature with the output voltage. As such, the current efficiency drops. To improve the current efficiency and the phase-noise performance, the series-coupled QVCO (S-QVCO) with coupling transistors connected in series with the cross-coupled transistors is proposed in [34] (Fig. 3.28). Since the phase-noise contribution from the coupling transistors is reduced as a result of degeneration in cascode configuration, the trade-off between phase noise and phase accuracy can be relaxed. Unfortunately, the coupling transistors need to be much
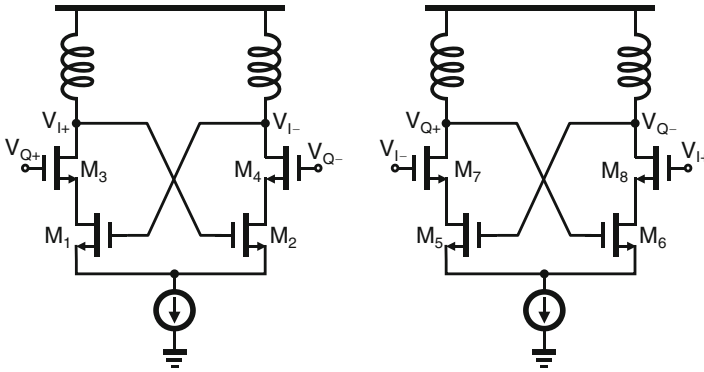
Fig. 3.28 Schematic of the series-coupled QVCO (S-QVCO) [34]

Fig. 3.29 QVCO using superharmonic coupling (SHC-QVCO) [36]
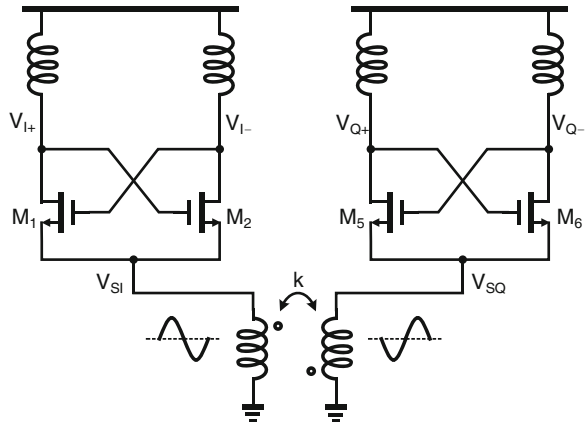
larger than the negative-resistance transistors to minimize their drain-to-source voltage overhead to maximize the output amplitude and thus minimize the phase-noise contribution, which would introduce large loading to the resonate tank and significantly reduce both the operation frequency and the frequency tuning range. Furthermore, connecting the coupling transistors in cascode would increase the voltage headroom and make it unsuitable for low-voltage operation. To remove the noise and power penalty of the coupling transistors, the signals can also be coupled through the substrate terminal of the core transistors [35]. However, the large signals coupled through the substrate may forward bias the substrate junction and hence overload the resonant tank.

Another way to synchronize the LC-VCOs for quadrature generation is to couple the LC-VCOs at the second harmonic frequency. For a single LC-VCO, the tail node exhibits a periodic waveform at $2\omega_0$. If this periodic voltage at the tail nodes of two LC-VCOs is kept $180°$ out of phase, the outputs of the two VCOs will operate in quadrature. Figure 3.29 shows one way to realize the out-of-phase

relationship between the two tail nodes V_{SI} and V_{SQ} by coupling them together with a 1:1 transformer [36]. For this superharmonic-coupled (SHC) QVCO, the coupling relies on the second harmonic and does not require the oscillation frequency to deviate from the self-resonant frequency ω_0, which avoids the degradation of tank quality factor. However, the phase error and the phase noise of the SHC-QVCO are still not independent to each other. On one hand, the on-resistance of the cross-coupled transistors has to be sufficiently low for effective coupling and reduced sensitivity of the phase error to mismatches. On the other hand, large cross-coupled transistors would inevitably limit the maximum oscillation frequency, load the resonator, and thus degrade the phase-noise performance [37].

3.5 Low-Voltage CMOS VCOs

Assuming a VCO is in the current-limited region, according to (3.19) and (3.33), the phase noise and FoM of the LC-VCO are degraded by 6 dB and 3 dB respectively, when the output amplitude is reduced by half. Since the maximum output amplitude is directly limited by the supply voltage, the minimum phase noise is significantly degraded for low-voltage designs. From Table 3.1, it is obvious that both complementary LC-VCO and class-C LC-VCO are not suitable for low-voltage application since its maximum output amplitude is inherently half compared with the NMOS counterparts. Actually, even the NMOS LC-VCO cannot be practically used in the wireless transceivers when supply voltage is reduced to 0.5 V or even lower due to the poor phase-noise performance. In Chap. 5, transformer-feedback techniques will be presented to break the output amplitude limitation set by the supply voltage to achieve a much larger output amplitude than $2V_{DD}$, which would improve the phase noise and FoM under low supply voltage.

3.6 Wideband CMOS VCOs

The SCA as shown in Fig. 3.20 has been widely used for wideband VCO design to reduce the varactor size and thus flicker noise up-conversion of the tail-biasing transistor through AM-to-PM noise conversion. However, as already pointed out, large tuning range requires large C_{on}/C_{off} ratio and thus small switch size to reduce C_{off}, which in turn results in large turn-on resistance and degradation of the quality factor of the switched capacitor and thus the phase noise and FoM. Q_T degradation also reduces the parallel tank resistance R_P, which requires a large power consumption to maintain the same output amplitude. At high frequency, the degradation of tank Q_T is even exacerbated since the capacitor Q becomes dominant. Moreover, the large parasitic junction capacitors from the switches may dominate the tank capacitance at high frequency, which exacerbates the AM-to-PM noise conversion.

Fig. 3.30 Frequency
tuning of an LC tank using
switched inductor
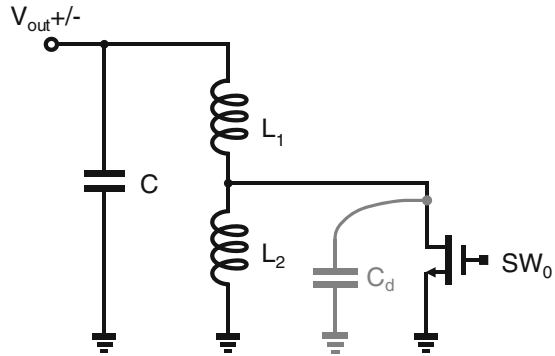
An alternative way to tune the oscillation frequency is to change the tank inductance [38–41]. As shown in Fig. 3.30, a switch is connected in parallel with one segment of the total tank inductor so that the tank inductance can be changed by controlling the switch to be on or off. Since the switched-inductor method provides the coarse frequency tuning, the frequency range that the SCA and varactors need to cover is reduced, which alleviates the capacitor Q degradation. On the other hand, since the turn-on resistor of the switch is directly in series with L_1, it would severely degrade the inductor Q. Increasing the switch transistor size can alleviate the inductor Q degradation at the cost of a large parasitic capacitor C_d when the switch is turned off. A large C_d would in turn decrease the effective inductance of L_2 and limits the frequency tuning range.

In Chap. 6, the fourth-order amplitude and phase characteristic of a transformer tank will be proposed to enable the VCO to operate in dual bands without the use of lossy MOS switches. Chapter 7 will present a magnetically tuning method that changes the effective coupling coefficient k of a transformer to extend the frequency tuning capability from dual bands to multiple bands, which can significantly increase the VCO tuning range at mm-Wave frequencies.

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Chapter 4
Design Considerations for CMOS Frequency Dividers

4.1 Background

In addition to the VCO, a frequency divider is another key building block in PLLs (Fig. 4.1), in particular the one following the VCO. Working at a much higher frequency, frequency dividers typically consume substantially more power than other building blocks operating at much lower frequencies, such as the PFD and the loop filter.

Furthermore, as shown in Fig. 4.2, frequency dividers can also be employed together with a differential VCO to generate in-phase and quadrature-phase (IQ) LO signals that are essential for single-sideband mixers and modern wireless transceivers [1].

4.2 Latch-Based Frequency Dividers

One simple way to realize a divide-by-2 (/2) frequency divider is to use two latches in a feedback loop as shown in Fig. 4.3. The choice of circuit implementation of the latch depends on the input frequency and the CMOS technology. For example, in a 65-nm CMOS process, the latch based on static logics [2] functions well for input frequency below ~100 MHz. As the input frequency increases to a range from several hundreds of MHz to several GHz, the latch based on dynamic logic such as the true single-phase clocking (TSPC) logics [3] and the transmission-gate-based logics [4] can be employed to achieve high-speed operation with low power consumption as shown in Fig. 4.4a, b, respectively.

To expand the input frequency range, the latch based on the current-mode logic (CML) can be employed. Figure 4.5 shows the CML latch with resistive load [5]. Operating in the current mode, CML dividers can achieve much faster speed than both the TSPC and transmission-gate-based dividers. Moreover, CML dividers
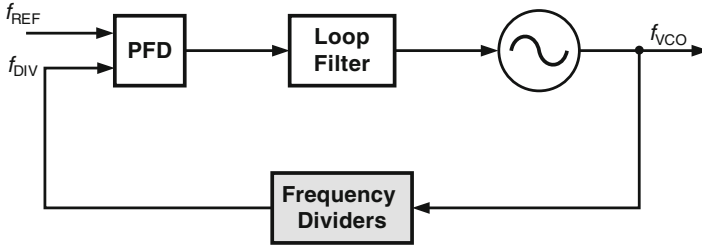
Fig. 4.1 Frequency dividers in the PLL

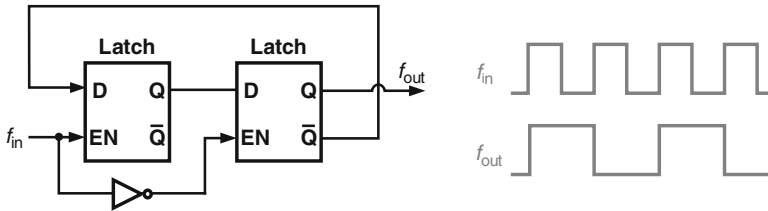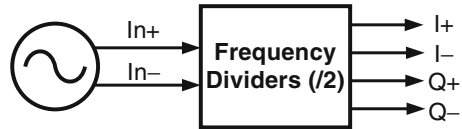**Fig. 4.2** Divider-based IQ LOs generation scheme

Fig. 4.3 Latch-based frequency divider

do not require input signals with full swings, which renders them more suitable for high-frequency applications. The maximum operating frequency that CML dividers can achieve depends on the loading capacitance and the required output swing. Typically in a 65-nm CMOS process, CML dividers can function well at input frequencies up to 10 GHz.

To increase the input frequency, the dynamic load with the PMOS transistors controlled by the clock signal can be employed, as shown in Fig. 4.6. In the sensing mode, the PMOS transistors are operated in the linear region to provide a small RC time constant at the output node. While in the latching mode, the PMOS transistors are turned off to achieve a large RC time constant and small static current [6]. To further boost the input frequency of the dividers, inductive load can also be used to replace the resistive load in the CML latch at the cost of a large chip area.

Fig. 4.4 Frequency divider based on (**a**) TSPC logics and (**b**) transmission-gate-based logics
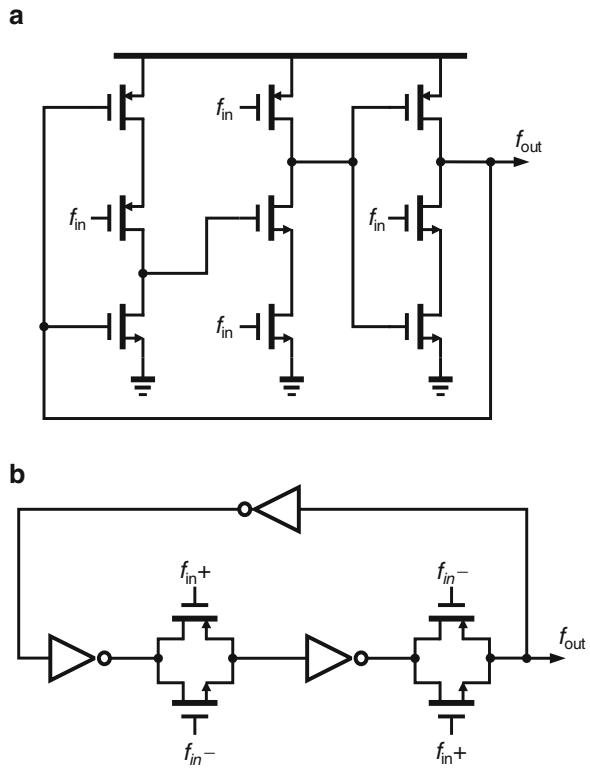


Fig. 4.5 Schematic of the CML latch with resistive load
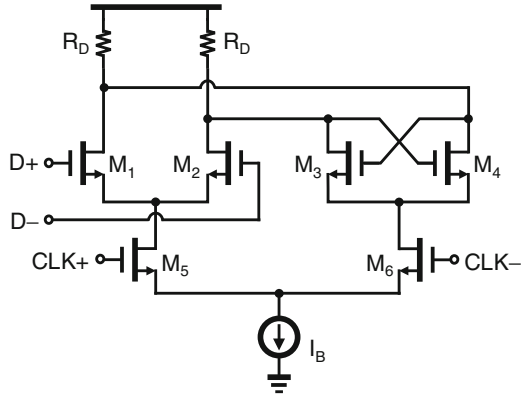
4.3 Injection-Locked Frequency Dividers

Frequency division can also be realized utilizing the injection-locked phenomenon [7]. Figure 4.7a shows the model of an injection-locked oscillator (ILO), where an input signal with frequency f_{in} and power P_{in} is injected into an oscillator with a

Fig. 4.6 Schematic of the
CML latch with dynamic
load [6]
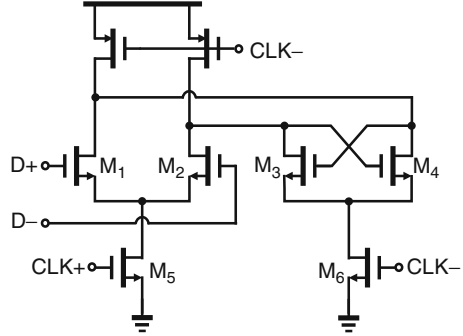
free-running frequency of f_{osc}. Assuming f_{in} is close to f_{osc}, when P_{in} is small ($P_{in} < P_{pull}$), the oscillation frequency will not be disturbed by the input signal and the output frequency f_{out} of the ILO remains as f_{osc}. As P_{in} increases above P_{pull}, the output frequency will be pulled away from f_{osc}. But since P_{in} is not strong enough to make the oscillator perfectly synchronized with the input signal, the output frequency is unstable. Finally, when P_{in} is larger than the minimum required power P_{min} that guarantees the perfect synchronization between the oscillator and input signal, the output frequency will be locked to f_{in}. When the ILO is locked and f_{in} is close to f_{osc}, the output phase noise would follow the input phase noise since the output jitter will be corrected by the input signal every cycle.

By plot P_{min} for different f_{in}, the input sensitivity curve of an ILO can be obtained as shown in Fig. 4.8. Since f_{in} can be either higher or lower than f_{osc}, a certain minimum input power $P_{min,0}$ will correspond to two different input frequencies f_L and f_H in the plot of sensitivity curve. Under the input power of $P_{min,0}$, the ILO can be properly locked only when the input frequency f_{in} is located between f_L and f_H. So the locking range at certain input power is defined as $f_{LR} = f_H - f_L$. When the input power is reduced, the locking range will decrease. Finally, the locking range becomes zero when $P_{in} < P_{pull}$, which indicates that the input signal is too weak to affect the f_{out}. As a result, f_{out} just equals to f_{osc}.

The ILO can be expanded to an injection-locked frequency divider (ILFD) by mixing the output with the input signal first and then inject the two tones ($f_{in} - f_{out}$) and ($f_{in} + f_{out}$) at the mixer output into an ILO, as shown in Fig. 4.9. Since f_{in} is close to $2f_{out}$, the injection-locked phenomena will force $f_{in} - f_{out} = f_{out}$. As a result, the output frequency will be exactly $f_{in}/2$ if ($f_{in} - f_{out}$) is within the locking range of the ILO.
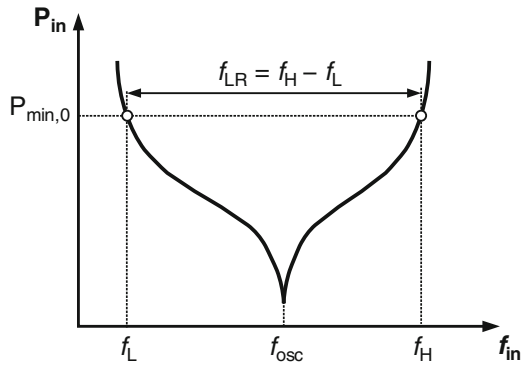
4.3.1 Indirect-Injection ILFDs

Figure 4.10 shows the circuit implementation of the indirect-injection ILFD. The input signal $v_i(2\omega)$ to be divided is applied directly to the gate of the tail-biasing transistor, which converts the input voltage to the current $i_i(2\omega)$ and then mixes it
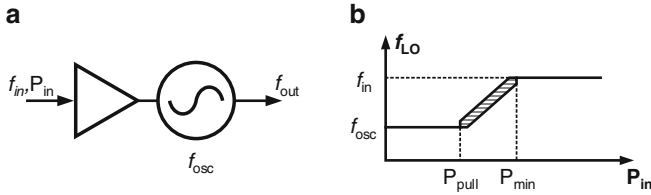
Fig. 4.7 Injection-locked oscillator (ILO): (**a**) behavioral model, (**b**) output frequency as a function of the input power

Fig. 4.8 Input sensitivity curve of an ILO

Fig. 4.9 Simplified behavioral model of the ILFD
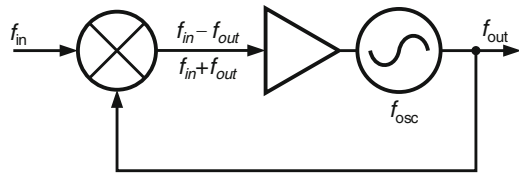
with the output voltage $v_o(\omega)$ through the cross-coupled transistor $M_{1/2}$ to generate the injected current $i_{inj}(\omega)$ to the LC tank. In the indirect-injection topology, the cross-coupled pair providing the negative transconductance for the oscillator also functions as the mixer.

In the indirect-injection ILFD, the total current $i_t(\omega)$ injected into the tank consists of two components: $i_{inj}(\omega)$ and $i_{ccp}(\omega)$. Figure 4.11 shows the behavioral model of the indirect-injection ILFD [8]. The cross-coupled transistor $M_{1/2}$ acts as a single-balanced mixer which mixes the output voltage $v_o(\omega)$ with the currents $i_i(2\omega)$ and I_{DC} from tail transistor, respectively. The expressions for $i_{inj}(\omega)$ and $i_{ccp}(\omega)$ can be summarized as

$$i_{inj}(\omega) = K_1 \cdot i_i(2\omega) \cdot v_o(\omega) \tag{4.1a}$$

Fig. 4.10 Schematic of the indirect-injection ILFD
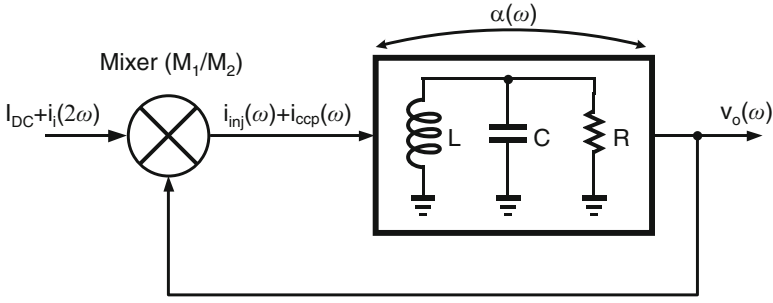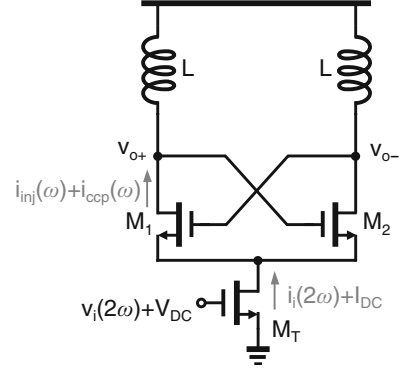
Fig. 4.11 Behavioral model of the indirect-injection ILFD

$$i_{ccp}(\omega) = K_2 \cdot I_{DC} \cdot v_o(\omega) \tag{4.1b}$$

where K_1 and K_2 are the conversion gains of the mixer. According to (4.1a) and (4.1b), $i_{ccp}(\omega)$ is in the same direction with $v_o(\omega)$, while the phase relationship between $i_{inj}(\omega)$ and $v_o(\omega)$ is not fixed and can be an arbitrary value.

Since the injected current components $i_{inj}(\omega)$ and $i_{ccp}(\omega)$ are all at the same frequency ω with different phase, they can be summed up to obtain the total current $i_t(\omega)$ injected into the LC tank using the phasor calculation as

$$i_t(\omega) = i_{inj}(\omega) + i_{ccp}(\omega) \tag{4.2}$$

Similar to an oscillator, for an ILFD to work properly, Barkhausen criterion defined in (3.2a) and (3.2b) needs to be satisfied. Figure 4.12a shows the magnitude and phase plots of the impedance of an LC tank. At the resonant frequency ω_0, the impedance magnitude is maximum, and the phase is zero. To lock the ILFD at a frequency ω different from the resonant frequency ω_0, it is necessary that the LC tank operates away from the resonant frequency with a nonzero phase shift. Assuming the phase of tank impedance is $\alpha(\omega)$ at the frequency ω, the phase shift $\gamma(\omega)$ between the tank current $i_t(\omega)$ and the tank voltage $v_o(\omega)$, as shown in
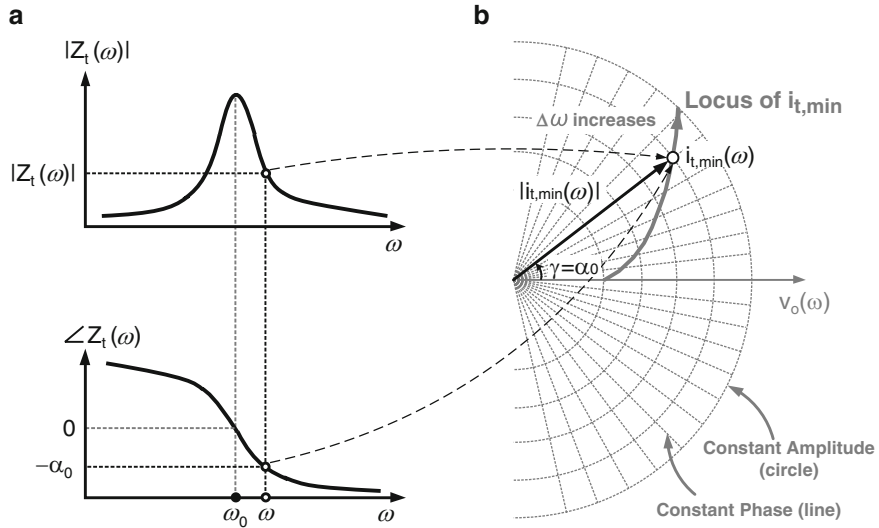
Fig. 4.12 (**a**) Frequency response of the LC tank impedance and (**b**) phasor diagram of the currents injected into the LC tank

Fig. 4.12b, should meet the phase condition, which guarantees that the total phase of the open loop gain is zero:

$$\gamma(\omega) = -\alpha(\omega) \qquad (4.3a)$$

In addition, to satisfy the gain condition, the amplitude of the tank current also needs to be large enough to guarantee that the divider can properly oscillate, and the output voltage is larger than the requirement across the whole locking range. Assuming that the minimal output amplitude required is $|v_{o,min}(\omega)|$, the minimal amplitude of the injection current can be expressed as below:

$$|i_{t,min}(\omega)| = \frac{|V_{o,min}(\omega)|}{|Z_t(\omega)|} \qquad (4.3b)$$

The amplitude and phase requirements of $i_t(\omega)$ can be analyzed with the help of the phasor diagram as shown in Fig. 4.12b [9]. At certain output frequency ω within the locking range, the position of the $i_{t,min}(\omega)$ can be determined by substituting the amplitude and phase of the tank impedance into (4.3a) and (4.3b). To achieve a minimal output amplitude larger than $|v_{o,min}(\omega)|$, $|i_t(\omega)|$ must be larger than $|i_{t,min}(\omega)|$. By connecting the end points of $i_{t,min}(\omega)$ at different frequencies on the phasor plane, the optimal locus of $i_{t,min}(\omega)$ can be determined. When the output frequency ω moves further away from the tank resonant frequency ω_0, the tank impedance $|Z_t(\omega)|$ decreases and the phase shift $|\alpha(\omega)|$ increases, and both $|i_{t,min}(\omega)|$

and $|\gamma(\omega)|$ need to be increased in order to maintain the same output amplitude and to satisfy the phase condition. At the edge of the locking range, if $i_t(\omega)$ locates to the left side of the optimal locus of $i_{t,min}(\omega)$, the divider has excess phase for the phase condition but insufficient amplitude to satisfy the gain condition. On the other hand, if $i_t(\omega)$ locates to the right side of the optimal locus, the divider achieves enough amplitude for the gain condition but insufficient phase to meet the phase condition. Although Fig. 4.12 only shows the situation that $\omega > \omega_0$, the phasor diagram method and the above discussions can also be applied to the situation when $\omega < \omega_0$ by mirroring the phasor $i_t(\omega)$ and the locus of $i_{t,min}(\omega)$ down to the bottom region of the reference phasor $v_o(\omega)$.

By adding the current phasors $i_{inj}(\omega)$ and $i_{ccp}(\omega)$, the complete phasor diagram can be drawn as shown in Fig. 4.13, which provides an intuitive way for locking range analysis and optimization. Based on the definitions from (4.1a) and (4.2b), the directions of $i_{ccp}(\omega)$ is in the same direction with $v_o(\omega)$, while the direction of $i_{inj}(\omega)$ is arbitrary, and the phase difference β between $i_{inj}(\omega)$ and $i_{ccp}(\omega)$ can be any value between 0 and 2π. As a result, the locus of $i_{inj}(\omega)$ or $i_t(\omega)$ becomes a circle.

As shown in Fig. 4.13, if I_{DC} of the indirect-injection ILFD is large, $|i_{ccp}(\omega)|$ is large so that the locus of phasor $i_{inj}(\omega)$ is located to the right side of the optimal locus of $i_{t,min}(\omega)$ but do not intersect with it. In this case, since $|i_t(\omega)|$ is always larger than $|i_{t,min}(\omega)|$, the gain condition is always met, and the locking range is limited only by the phase condition. So the divider is working in the phase-condition-limited (PCL) region. In the PCL region, the maximum and minimum output frequencies ω_H and ω_L are only determined by the maximum phase shift γ_{max} that $i_t(\omega)$ can provide. Based on the phasor diagram in Fig. 4.13, γ_{max} is achieved when $i_t(\omega)$ is tangent to the locus of $i_{inj}(\omega)$ which can be expressed as below:

$$|\gamma_{max}| = \arcsin\left(\frac{|i_{inj}(\omega)|}{|i_{ccp}(\omega)|}\right) \tag{4.4}$$

It follows that the value of ω_H and ω_L can be determined by finding the corresponding frequency for the phase shift $\alpha = -\gamma_{max}$ on the phase plot of the tank impedance as shown in Fig. 4.12a. If the frequency response is symmetrical to the resonant frequency ω_0, the total output locking range can be expressed as $\Delta\omega_{LR} = \omega_H - \omega_L = 2(\omega_H - \omega_0)$.

In the PCL region, according to (4.4), the locking range can be increased by increasing $|i_{inj}(\omega)|$ while still keeps $|i_{ccp}(\omega)|$ the same. In Fig. 4.10, since $i_i(2\omega) = g_m v_i(2\omega)$ and $g_{mT} = 2I_{DC}/(V_{DC} - V_{th})$, where g_{mT} is the transconductance of the tail transistor M_T, $|i_i|$ can be increased by reducing the overdrive voltage $(V_{DC} - V_{th})$, while I_{DC} is kept the same. So M_T with a large W/L ratio is preferred.

To boost the locking range of indirect-injection ILFDs, the current-bleeding technique is proposed in [8] (Fig. 4.14). By adding a current path from V_{DD} to the drain of M_T, the total current flowing through the cross-coupled pair $M_{1/2}$ is reduced, while the total DC current flowing through M_T is still kept the same. Since $|i_i(2\omega)|$ can be still kept the same, the $|i_{inj}(\omega)|/|i_{ccp}(\omega)|$ ratio is increased.

Fig. 4.13 Phasor diagram of the indirect-injection ILFD in the PCL region
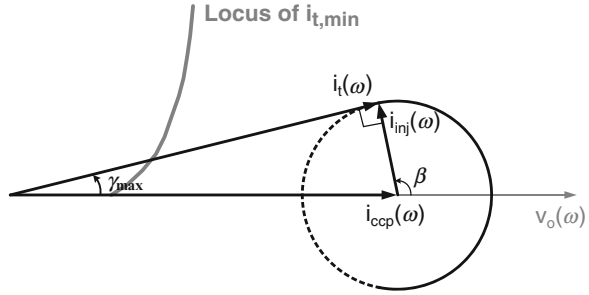
So according to (4.4), the locking range is increased. The current source I_{Bleed} can be implemented with a PMOS transistor as shown in Fig. 4.15. In addition to bleeding the DC current, the input voltage can also be applied to the gate of PMOS transistor to create another injection current $i_{i,p}(2\omega)$. So the total inject current at frequency 2ω is increased to $i_i(2\omega) = i_{i,n}(2\omega) + i_{i,p}(2\omega)$. As a result, $\left|i_{inj}(\omega)\right|/\left|i_{ccp}(\omega)\right|$ and thus the locking range is further increased by reusing the g_m of the PMOS transistor for DC current bleeding.

4.3.2   Direct-Injection ILFDs

An ILFD can also be realized by directly injecting the currents into the LC tank of an oscillator as shown in Fig. 4.16a. Figure 4.16b shows the equivalent half-circuit of the direct-injection ILFD where the total current $i_t(\omega)$ injected into the tank consists of three components: $i_{inj}(\omega)$, $i_0(\omega)$, and $i_{ccp}(\omega)$. In a direct-injection ILFD, the input transistor M_{in} and the cross-coupled transistor $M_{1/2}$ act as single-balanced mixers. As shown in the behavioral model in Fig. 4.17, one input of Mixer 1 (M_{in}) is from the total voltage $V_{DC} + v_{inj}(2\omega)$ applied at the gate of M_{in}, while the other input is fed back from the divider output $v_{o-}(\omega)$. Correspondingly, the output current of Mixer 1 consists of the current components $i_{inj}(\omega)$ and $i_0(\omega)$. Similarly, the injected current $i_{ccp}(\omega)$ is generated by mixing $v_{o-}(\omega)$ and the DC current I_{DC} through Mixer 2 (M_1). The expressions for $i_{inj}(\omega)$, $i_0(\omega)$, and $i_{ccp}(\omega)$ can be summarized as [10]

$$i_0(\omega) = K_1 \cdot V_{DC} \cdot v_o(\omega) \tag{4.5a}$$

$$i_{inj}(\omega) = K_2 \cdot V_i(2\omega) \cdot v_o(\omega) \tag{4.5b}$$

$$i_{ccp}(\omega) = -K_3 \cdot I_{DC} \cdot v_o(\omega) \tag{4.5c}$$

where K_1 and K_2 are the conversion gains of the Mixer 1, while K_3 is the conversion gain of the Mixer 2. According to (4.5a)–(4.5c), $i_{ccp}(\omega)$ is in the same direction with $v_o(\omega)$, while $i_0(\omega)$ is in the opposite direction with $v_o(\omega)$ since the mixing

Fig. 4.14 Concept of the current-bleeding indirect-injection ILFD
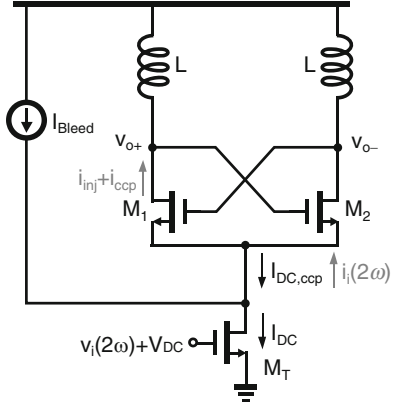
Fig. 4.15 Circuit implementation of the current-bleeding indirect-injection ILFD [8]
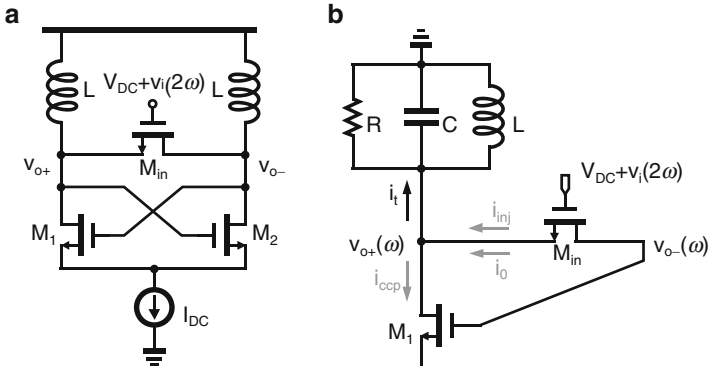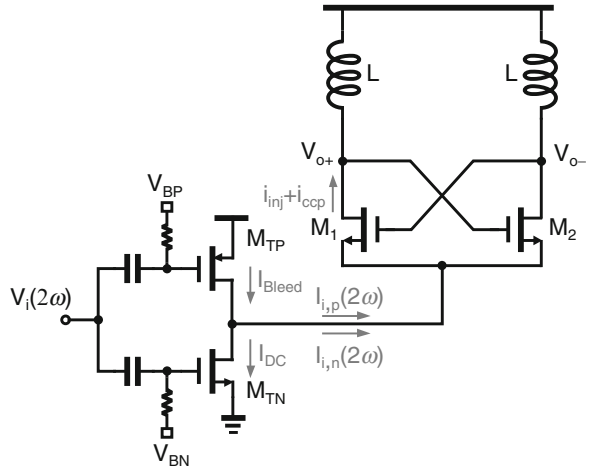
Fig. 4.16 (**a**) Schematic and (**b**) half-circuit of the direct-injection ILFD

Fig. 4.17 Behavioral model of the direct-injection ILFD

inputs $v_{o+}(\omega)$ and $v_{o-}(\omega)$ to generate this two currents are out of phase. The phase relationship between $i_{inj}(\omega)$ and $v_o(\omega)$ is not fixed and can be an arbitrary value.

The phasor diagram can also be employed to analyze the locking range of the direct-injection ILFD. As shown in Fig. 4.18, similar to the direct-injection ILFD, if I_{DC} is large, the direct-injection ILFD is working in the PCL region. The maximum phase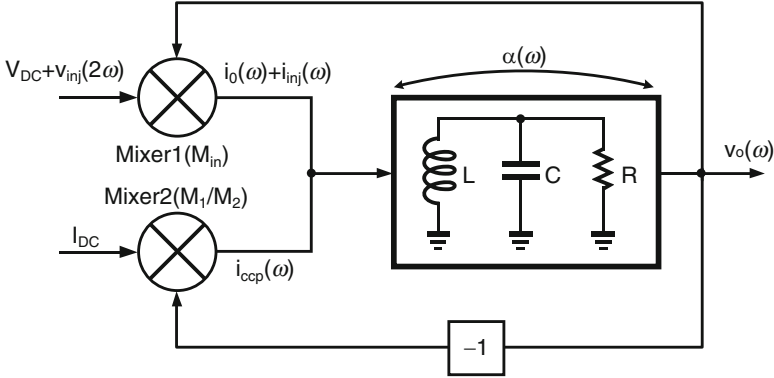 shift γ_{max} that $i_t(\omega)$ can provide is achieved when $i_t(\omega)$ is tangent to the locus of $i_{inj}(\omega)$ which can be expressed as below:

$$|\gamma_{max}| = \arcsin\left(\frac{|i_{inj}(\omega)|}{|i_{ccp}(\omega)| - |i_0(\omega)|}\right) \qquad (4.6)$$

Compared with the indirect-injection ILFD, since $i_{inj}(\omega)$ and $i_{ccp}(\omega)$ in the direct-injection ILFD comes from two different mixers, one more degree of freedom can be utilized for the locking range optimization. In the PCL region, according to (4.6), if $|i_{inj}(\omega)|$ and $|i_0(\omega)|$ from the transistor M_{in} is kept the same, γ_{max} and thus the locking range can be increased by reducing $|i_{ccp}(\omega)|$. On the other hand, reducing $|i_{ccp}(\omega)|$ would reduce the output amplitude. As the output amplitude is still guaranteed to be larger than $|i_{t,min}(\omega)|$ in the PCL region, the bias current I_{DC} should be kept small in order to achieve a large locking range.

In the PCL region, as I_{DC} decreases, the locus of $i_{inj}(\omega)$ moves to the left. After it crosses the locus of $i_{t,min}(\omega)$, the divider starts to work in the gain-condition-limited (GCL) region, as shown in Fig. 4.19. In the GCL region, the maximum locking range is achieved when the direction of $i_{inj}(\omega)$ is vertical to that of $v_0(\omega)$. So the maximum phase shift γ_{max} can be expressed as below:

$$|\gamma_{max}| = \text{arctg}\left(\frac{|i_{inj}(\omega)|}{|i_{ccp}(\omega)| - |i_0(\omega)|}\right) \qquad (4.7)$$
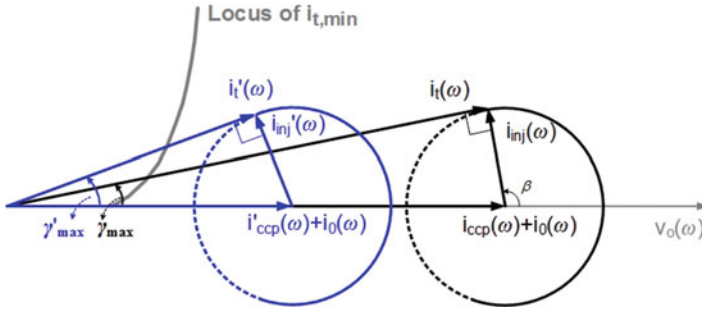
Fig. 4.18 Phasor diagram of the direct-injection ILFD in the PCL region

Fig. 4.19 Phasor diagram of the direct-injection ILFD in the GCL region
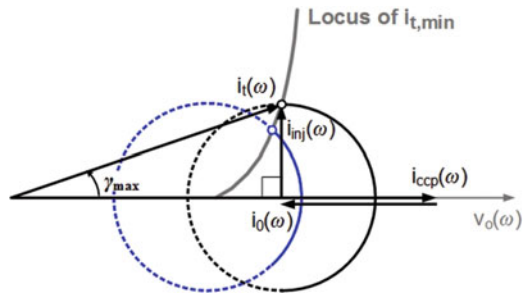
If I_{DC} is further reduced after its optimum value is achieved, the maximum phase shift γ_{max} starts to decrease which in turn degrades the locking range as shown in Fig. 4.19.

To design a direct-ILFD with large locking range, the divider is preferred to operate in the GCL region. When the LC tank and the input transistor M_{in} are fixed, I_{DC} can be properly chosen to make sure that $i_{inj}(\omega)$ is vertical to $v_o(\omega)$. To further extend the locking range, large size of M_{in} can be employed to increase both $|i_{inj}(\omega)|$ and $|i_0(\omega)|$. At the same time, $i_{ccp}(\omega)$ and thus the DC current of the divider also need to be increased accordingly to ensure that $i_{inj}(\omega)$ is still vertical to $v_o(\omega)$. In other words, the locking range is increased at the cost of larger power. Besides, large M_{in} would add more parasitic capacitance, which would limit the maximum operating frequency of the divider.

4.3.3 Design Consideration for the LC-Tank

The locking range depends not only on the maximum phase shift γ_{max} that $i_t(\omega)$ can provide but also on the characteristics of the tank impedance. Consider two ILFDs using two LC-tanks with the same resonant frequency ω_0 and quality factor Q_T but different inductance values as shown in Fig. 4.20a. Since the tank with larger L has a
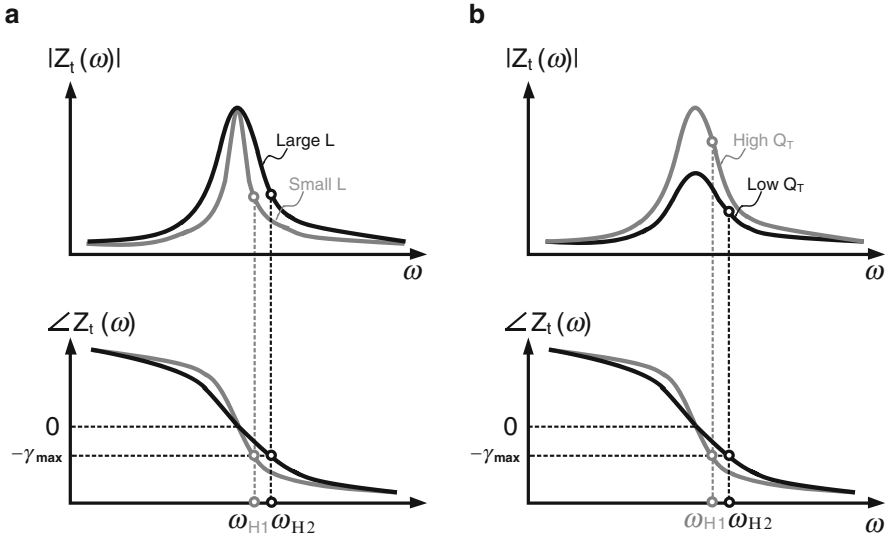
Fig. 4.20 Frequency responses of the LC tank impedance for (**a**) different L/C ratios (with the same Q_T and ω_0) and (**b**) different tank quality factors (with the same L/C ratio and ω_0)

less steep phase response when the frequency is close to ω_0, its ILFD can achieve a wider locking range when operating in the PCL range for the same phase shift γ_{max} that $i_t(\omega)$ can provide. In the GCL region, to achieve the same ω_H, the tank with the larger L can provide a larger $|Z_t(\omega)|$, which results in a smaller I_{DC} to fulfill the gain condition. As a result, a larger inductance or a larger L/C ratio is always preferred in both PCL and GCL regions. In practice, the L/C ratio is limited by the capacitive loading from the next stage as well as the parasitic capacitance at the output node.

Now, let us consider two ILFDs using two LC-tanks with the same ω_0 and the same L/C ratio but different Q_T as shown in Fig. 4.20b. Since the tank with the lower Q has a less steep phase response when the frequency is close to ω_0, its ILFD can achieve a wider locking in the PCL range, again for the same phase shift γ_{max} that $i_t(\omega)$ can provide. However, in the GCL range, to achieve the same ω_H, the ILFD with the lower Q tank needs to consume more power since its $|Z_t(\omega)|$ is smaller at the same frequency. In other words, in the GCL region, a tank with a higher Q is preferred to minimize the power consumption.

4.3.4 Phase-Noise Performance

Figure 4.21 shows the noise model of the ILFD, which is similar to a Type-I first-order PLL [11, 12]. Here N is the division ratio while ϕ_{n_in}, ϕ_{n_out}, and ϕ_{n_osc} represent the phase noises of the injection signal, the divider output, and the divider

Fig. 4.21 Noise model of the ILFD [12]
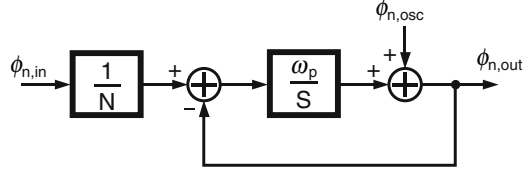
as a free-running oscillator, respectively. The output phase noise can be expressed as below [11]:

$$\mathcal{L}_{\text{out}}(\Delta\omega) = \frac{\omega_p^2}{\Delta\omega^2 + \omega_p^2} \cdot \frac{\mathcal{L}_{\text{in}}(\Delta\omega)}{N^2} + \frac{\Delta\omega^2}{\Delta\omega^2 + \omega_p^2} \mathcal{L}_{\text{osc}}(\Delta\omega) \qquad (4.8)$$

where ω_p can be approximated by the locking range $\Delta\omega_{\text{LR}}$ of the ILFD when the deviation of the output frequency from the tank resonant frequency ω_0 is small [13]. It is worthwhile to note that ω_p decreases as the output frequency moves toward the edge of the locking range [12, 14], which indicates less suppression of the phase noise from the free-running ILFD.

According to (4.8), the output phase noise contains two terms. In the first term, the input phase noise $\mathcal{L}_{\text{in}}(\Delta\omega)$ is firstly scaled by $1/N^2$ and then filtered by a low-pass filter (LPF) with a 3-dB bandwidth of ω_p. Meanwhile, in the second term, the phase noise from the free-running ILFD is filtered by a high-pass filter with a 3-dB bandwidth of ω_p. The output phase noise can be obtained by summing up the noise contributions from both the input and the free-running ILFD as shown in Fig. 4.22. At low offset frequencies, the output phase noise is dominated by the input phase noise plus 20 log(N). On the other hand, at offset frequencies larger than ω_p, the output phase noise just follows the phase noise of the free-running ILFD since the input does not affect the output anymore. For an ILFD operating at mm-Wave frequencies, the locking range is typically of several GHz so that the output phase noise would be dominated by the input phase noise at offset frequencies in the range of several hundreds of MHz.

4.3.5 ILFD Figure of Merit

Based on the locking range analysis in Sects. 4.3.1 and 4.3.2, the maximum locking range achieved is a direct trade-off with the power consumption. So the most used figure of merit (FoM) of the ILFD is defined as below:

$$\text{FoM} = \frac{\Delta f_{\text{LR}}\,[\text{GHz}]}{P_{\text{diss}}\,[\text{mW}]} \qquad (4.9)$$
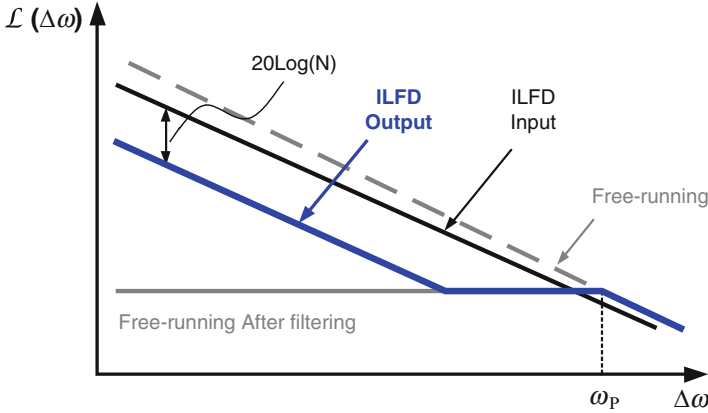
Fig. 4.22 Phase noises of the ILFD as functions of the offset frequency

where Δf_{LR} and P_{diss} are the frequency locking range and power consumption of the ILFD, respectively. When properly locked, the output phase noise within the interested offset frequency is determined by the input phase noise, and the phase noise is excluded from the FoM expression to make sure that ILFDs with different injection sources can be fairly compared.

4.4 Miller Frequency Dividers

Another effective way to realize the frequency division at high frequencies is based on a regenerative topology consisting of a mixer and a LPF in a feedback loop, as shown in Fig. 4.23. The mixer has two inputs: one being the input signal to be divided and the other being the output signal itself. Due to the mixing operation, there are two output tones at frequencies of $(f_{in} - f_{out})$ and $(f_{in} + f_{out})$ at the mixer output. After passing through the LPF, only the tone with the lower frequency of $(f_{in} - f_{out})$ is remained. Since the feedback loop forces that $f_{in} - f_{out} = f_{out}$, the output frequency will be exactly $f_{in}/2$.

Figure 4.24a shows the circuit implementation of the mixer-based frequency divider which is also well known as a Miller divider [15]. Here, a double-balanced mixer is employed with the inputs connected to the gates of the tail transistors M_{7-8} and the outputs fed back to the gates of switching transistors M_{1-4}. The inputs of the Miller divider can also be swapped. In other words, the outputs of the Miller divider can also be fed back to the gates of the tail transistors $M_{7/8}$, while the inputs are connected directly to the gates of the switching transistors M_{1-4} as shown in Fig. 4.24b, which can reduce the output capacitance at the cost of increased input capacitance. To achieve better suppression of the unwanted frequency component $(f_{in} + f_{out})$, which becomes the third harmonic of the desired output signal, the LPF is typically replaced by a narrow-band band-pass filter formed by an LC tank load [16].
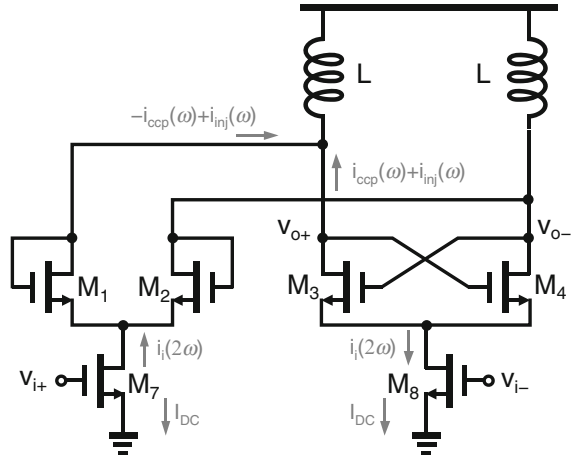
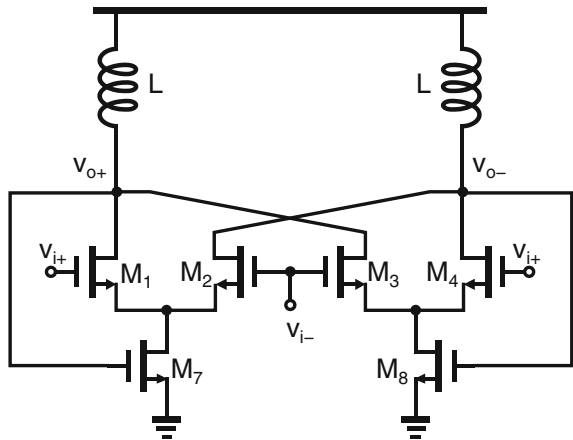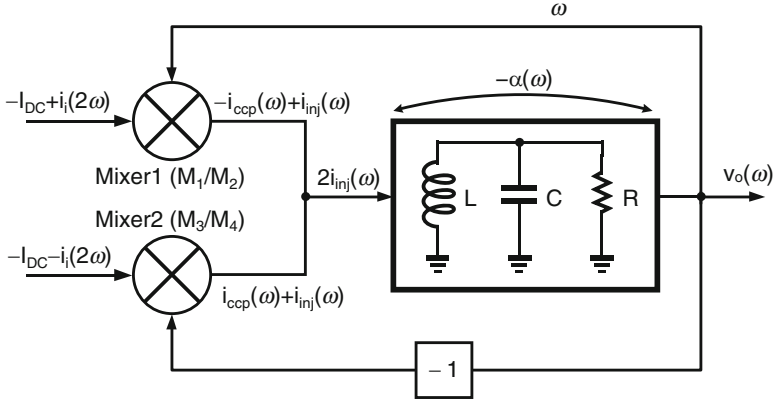**Fig. 4.23** Simplified behavioral model of the Miller divider
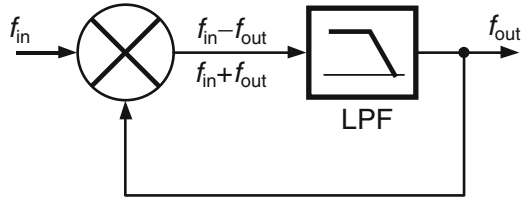
Fig. 4.24 (**a**) Type-I and (**b**) Type-II Miller dividers

Fig. 4.25 Behavioral model of the Type-I Miller divider

Figure 4.25 shows the corresponding behavioral model for the Miller divider in Fig. 4.24a, in which $i_i(2\omega) = -g_{m7/8}v_i(2\omega)$ and $i_{ccp}(\omega)$ and $i_{inj}(\omega)$ are the mixing products of the output voltage $v_o(\omega)$ with the DC current $-I_{DC}$ and with input current $i_i(2\omega)$, respectively. The expressions for i_{inj} and i_{ccp} can be summarized as

$$i_{inj}(\omega) = K_1 \cdot i_i(2\omega) \cdot v_o(\omega) \tag{4.10a}$$

$$i_{ccp}(\omega) = K_2 \cdot I_{DC} \cdot v_o(\omega) \tag{4.10b}$$

where K_1 and K_2 are the conversion gains of the Mixer 1 and 2, respectively.

Due to the double-balanced configuration, the $i_{ccp}(\omega)$ from Mixers 1 and 2 are in the opposite direction and thus completely canceled with each other. Since the total current injected into the tank contains only one component of $2i_{inj}(\omega)$, there will be no current flowing through the tank without the input signal, which indicates that the Miller divider cannot self-oscillate. The lack of $i_{ccp}(\omega)$ also explains the reason for large power consumption required by the Miller divider. As shown in the phasor diagram in Fig. 4.26, the Miller divider can only operate in the DCL region, in which the phase condition can always be satisfied, and the locking range is limited by insufficient loop gain. Since the DC current only serves to provide the transconductance converting the input voltage to current and has no contribution to the loop gain, the FoM of the conventional Miller divider is certainly much lower than ILFDs.

To improve the performance of the Miller divider, the double-balanced mixer architecture can be modified to intentionally introduce imbalance to prevent the current $i_{ccp}(\omega)$ from Mixers 1 and 2 from being perfectly canceled. One way to realize this imbalance is to bleed the DC current flowing through the transistors M_1 and M_2 by adding another current source as shown in Fig. 4.27 [9]. As shown in the behavioral model in Fig. 4.28, since the DC current of M_7 is kept the same as that of M_8, the input currents $i_i(2\omega)$ generated by M_7 and M_8 and thus the $i_{inj}(\omega)$ generated by Mixers 1 and 2 still have the same amplitude. However, since the DC currents of

Fig. 4.26 Phasor diagram of the Miller divider
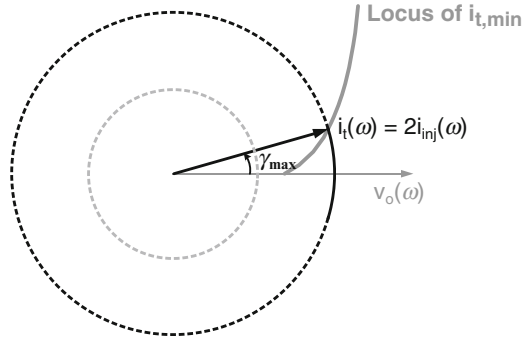
Mixer 1 is smaller than that of Mixer 2, the mixing product $|i_{ccp,bl}(2\omega)|$ becomes smaller than $|i_{ccp}(2\omega)|$. Consequently, the total current injected into the tank is increased to $2i_{inj}(\omega) + \Delta i_{ccp}(2\omega)$, where $\Delta i_{ccp}(2\omega) = i_{ccp}(2\omega) - i_{ccp,bl}(2\omega)$ and can be adjusted by controlling the bleeding current I_{bleed}. As shown in Fig. 4.29, with the help of the current phasor $\Delta i_{ccp}(2\omega)$, the locus of $i_{inj}(2\omega)$ can be moved toward the right, and the divider can achieve a larger locking range compared with the conventional Miller divider without consuming more power.

Unlike the conventional Miller divider, the current-bleeding Miller divider may oscillate even when there is no input signal if I_{bleed} and I_{DC} are large enough. Actually, as shown in Fig. 4.29, to achieve the optimal condition that $i_{inj}(2\omega)$ is vertical to $v_o(2\omega)$ for maximum locking range, $\Delta i_{ccp}(2\omega)$ is already large enough to sustain the oscillation without input signals. As the main difference between the conventional Miller dividers and ILFDs is whether the divider can self-oscillate without input signals, the current-bleeding Miller divider is more suitable to be categorized as an ILFD.

4.5   Summary

As discussed in Sects. 4.3 and 4.4, the indirect-injection ILFD, direct-injection ILFD, and current-bleeding Miller divider can all achieve a large locking range at mm-Wave frequency. Since the size of input transistor in direct-injection ILFD is much smaller than those in indirect-injection ILFD and current-bleeding Miller divider. The direct-injection ILFD presents the smallest loading capacitance to the VCO output and thus is most widely used in the frequency synthesizer [17–19] at mm-Wave frequency.

In Chap. 8, the transformer techniques will also be employed to effectively reduce the supply voltage of the regenerative ILFD which evolves from the Miller divider and significantly boost the locking range of the direct-injection ILFD. Thanks to the compact layout of the integrated transformer, the area of the ILFD with a transformer tank can be kept almost the same as that of the ILFD with a simple LC tank.
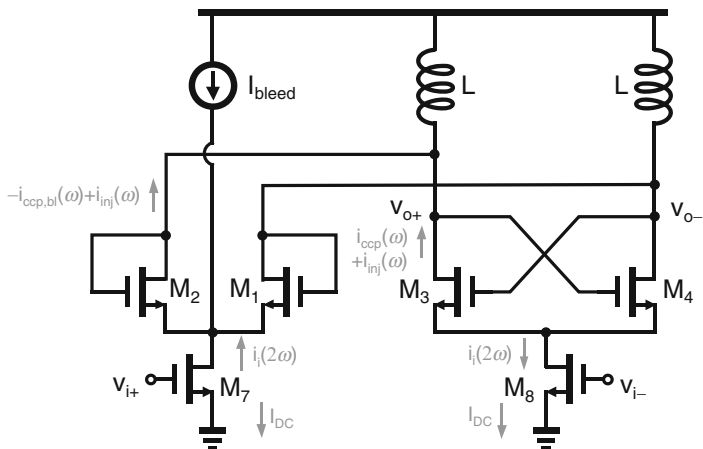
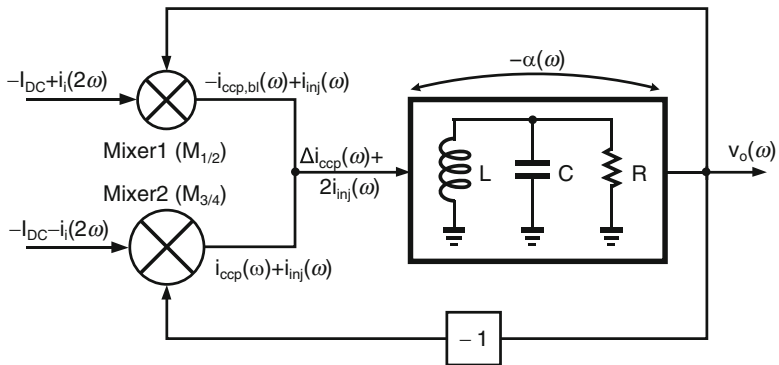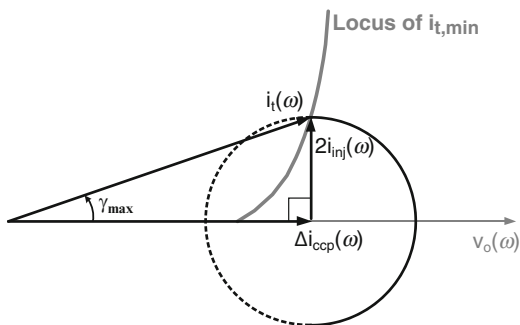**Fig. 4.27** Schematic of the current-bleeding Miller divider [9]

Fig. 4.28 Behavioral model of the current-bleeding Miller divider

Fig. 4.29 Phasor diagram of the current-bleeding Miller divider

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Chapter 5
Ultralow-Voltage VCO and QVCO Using Transformer Technique

5.1 Introduction

For the conventional NMOS LC-VCO as shown in Fig. 3.7, a low supply voltage would result in the decrease of the output signal amplitude V_o and thus the degradation of the phase-noise performance since the phase noise is inversely proportional to $V_o{}^2$ according to (3.19). For example, if the supply voltage is reduced from 1.2 to 0.3 V, the maximum V_o would roughly decrease from 2.4 to 0.6 V (ignoring the voltage headroom required by the current-biasing transistor). As a result, the minimum achievable phase noise will degrade by 12 dB[1] assuming all other parameters, including the tank capacitance, the tank Q_T, the oscillation frequency ω_0, and the offset frequency $\Delta\omega$, are kept the same. Such a phase-noise degradation is unacceptable for many cellular standards with stringent phase-noise requirements such as GSM requiring -162 dBc/Hz at 20-MHz frequency offset from a carrier frequency of 900 MHz [1].

Firstly, in this chapter, a novel design technique is presented to realize a transformer-feedback VCO (TF-VCO) in a standard CMOS process with high performance even at a supply lower than the threshold voltages of the MOS transistors [2]. The advantages of the TF-VCO over the conventional LC-VCOs are twofold: (1) the main limitation of the signal amplitude of a VCO with a low supply voltage is overcome by the concept of dual signal swings, which enables the output signals to swing above the supply voltage and below the ground potential to increase the carrier power and thus to improve the phase noise; (2) the transformer-feedback technique also improves the tank quality factor and shows an excellent cyclo-stationary noise property, which helps reduce the phase noise for a given

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[1] The FoM is still kept the same according to (3.30) since the current to sustain the maximum V_o also reduces by 4 times, and thus the power consumption reduces by 16 times. However, at low supply voltage, even the power budget can be increased, and the phase noise could not be improved anymore since the oscillator would enter the voltage-limited region.

power consumption. The transformer-feedback technique was demonstrated with two VCO prototypes fabricated in a standard 0.18-μm CMOS process. The first version is a 0.35-V 1.46-mW 1.4-GHz TF-VCO using PMOS transistors and two single-ended transformers [3]. The second version is a 0.5-V 570-μW 3.8-GHz TF-VCO using NMOS transistors and a single differential transformer. Measurement results of the two designs show comparable FoMs with the recent state-of-the-art VCOs that operate at much higher supply voltages.

Secondly, the technique to passively couple two LC-VCOs through on-chip transformers for quadrature generation is presented [4, 5]. By replacing the coupling transistors with the coupling transformer, undesirable effects contributed by the coupling transistors (including flicker noise, channel thermal noise, parasitic capacitance, and extra power consumption) are eliminated, which reduces both the phase noise and power consumption and increases the oscillation frequency of the QVCO. Moreover, the transformer-coupling technique also enjoys all the advantages of the TF-VCOs, including reduction of the minimum supply voltage required for the QVCO.

5.2 Transformer-Feedback VCO (TF-VCO)

5.2.1 Topology and Circuit Model

Figure 5.1a shows the schematic of the transformer-feedback VCO, which employs an integrated transformer in place of the inductor in the conventional LC-VCO. The primary coil of the transformer with self-inductance L_d is connected at between V_{DD} and the drain terminal of the cross-coupled transistor $M_{1/2}$, which constitutes the tank together with the capacitor C_d, while the secondary coil with self-inductance L_s is connected between ground and the source terminal of $M_{1/2}$. The primary coil L_d and the secondary coil L_s are magnetically coupled to each other with a coupling coefficient k.

Figure 5.1b plots the single-ended voltage waveforms, where V_d and V_s represent the voltages at the drain and source terminals of the transistor $M_{1/2}$, respectively. Since the source of $M_{1/2}$ is connected to the secondary coil of the transformer instead of directly being connected to the ground, it can swing below the ground potential. Furthermore, when the gate voltage is increased, the drain and source voltages are decreased at the same time. The reduction of the source voltage effectively lowers the ground potential and allows the drain voltage to go to a negative potential when the transistor is turned on. Since the drain and source signals oscillate in phase, the gate and source voltages are forced to be out of phase, which enlarges the effective gate-source overdrive voltage. Compared to the conventional LC-oscillators which can only achieve a maximal output amplitude of $\sim V_{DD}$, this phase synchronization provides extra voltage headroom for the drain oscillation and increases the driving capability of the cross-coupled

a

b
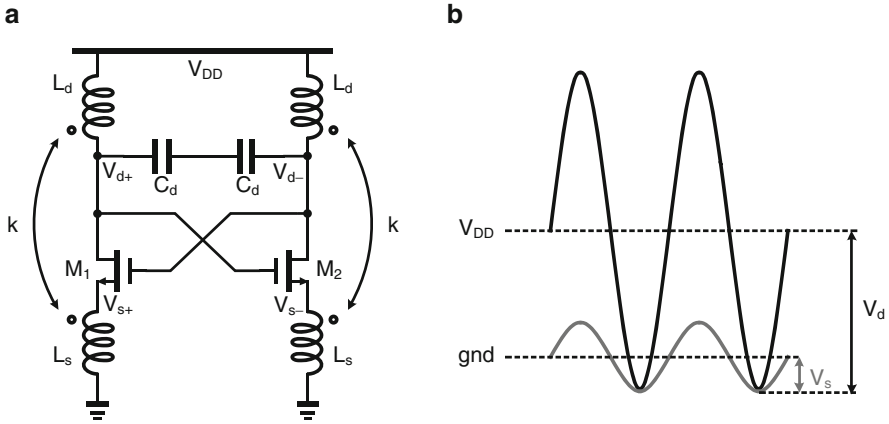
Fig. 5.1 Transformer-feedback VCO: (**a**) schematic and (**b**) waveforms of drain and source terminals

transistors, which effectively boosts the maximum oscillation amplitude. To estimate the maximum output amplitude, assuming an ideal coupling coefficient $k = 1$ for simplicity, the source signal amplitude V_s is related to the drain signal amplitude V_d by $V_s = V_d/N$, where N is the turn ratio between the primary and secondary coils defined as $N = \sqrt{L_d/L_s}$. As shown in Fig. 5.1b, the maximum drain voltage amplitude is given by $V_d = V_{DD} + V_s$ for the TF-VCO. So by substituting V_s with V_d/N, $V_{d,max}$ is expressed as

$$V_{d,max} = \frac{N}{N-1}V_{DD} \tag{5.1}$$

Figure 5.2 compares the output amplitude of the TF-VCO with that of a conventional LC-VCO. At a 0.5-V supply voltage, the TF-VCO with $N = 2$ achieves a maximal V_d of 1 V, which is twice of the maximum V_d that the conventional LC-VCO can achieve at the same supply voltage.

To analyze the performance of a TF-VCO, the feedback loop through the cross-coupled pair is broke and the circuit is rearranged as shown in Fig. 5.3. Now the open-loop transfer function becomes $V_{out}/V_{in} = (V_{out}/V_x)(V_x/V_{in})$. Since $V_{out}/V_x = V_x/V_{in}$ due to the symmetric property, then $|V_{out}/V_{in}| = |V_x/V_{in}|^2$ and $\angle(V_{out}/V_{in}) = 2\angle(V_x/V_{in})$. So the loop can be characterized by calculating the half-circuit transfer function V_x/V_{in}.

5.2.2 Oscillation Frequency and Phase Noise

To calculate the transfer function V_x/V_{in}, the transformer is replaced by the equivalent circuit model in Fig. 2.3 to obtain the small-signal equivalent circuit

Fig. 5.2 Simulated voltage
waveforms at the drain and
source of M1/2 for both the
TF-VCO and the
conventional VCO at a
same V_{DD} of 0.5 V
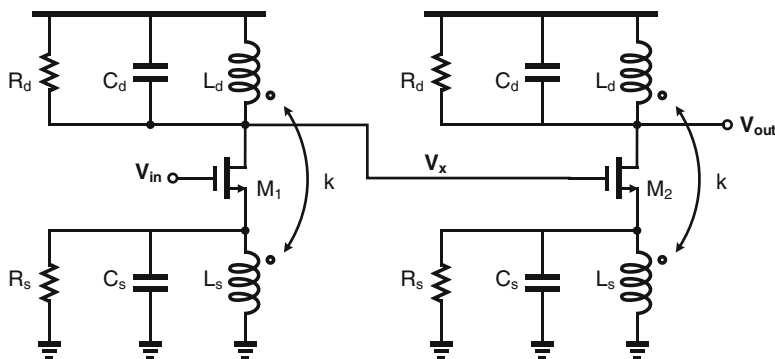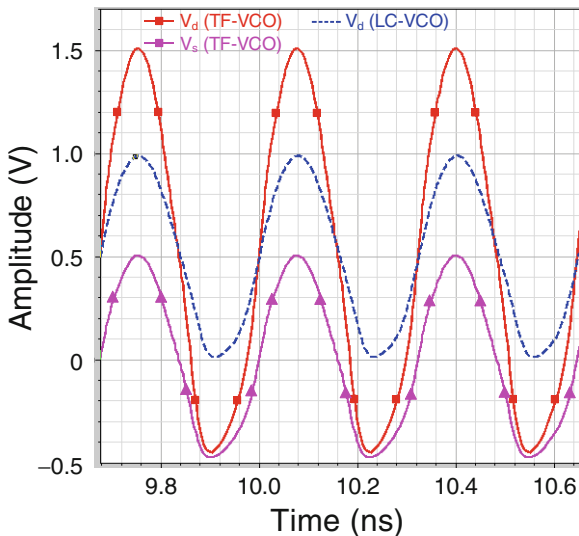
Fig. 5.3 Open-loop rearrangement of the TF-VCO

for the half-circuit as shown in Fig. 5.4, where R_d and R_s represent the parallel tank resistances of the primary and secondary coils, respectively. For simplicity, assume that $k = 1$ and that the output impedance of $M_{1/2}$ are negligibly large. By applying Kirchhoff's current law to both the source and the drain terminals, the following equations can be obtained:

$$g_m(V_{in} - V_s) = \left(\frac{1}{R_s} + sC_s + \frac{1}{sL_s}\right)V_s + Ni_x \qquad (5.2a)$$
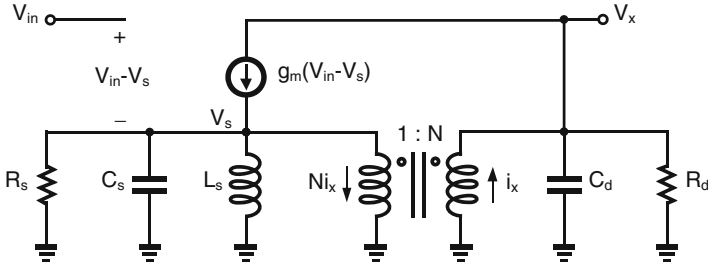
Fig. 5.4 Small-signal equivalent circuit for the half-circuit

$$i_x = -\left(\frac{1}{R_d} + sC_d\right)V_x - g_m(V_{in} - V_s) \tag{5.2b}$$

Substituting i_x with (5.2b) and V_s with V_x/N in (5.2a), the transfer function V_x/V_{in} can be expressed as

$$\frac{V_x}{V_{in}} = \frac{sg_mL_d\left(\frac{1-N}{N}\right)}{s^2(L_dC_d + L_sC_s) + s\left[g_mL_d\frac{1}{N}\left(\frac{1}{N}-1\right) + \frac{L_s}{R_s} + \frac{L_d}{R_d}\right] + 1} \tag{5.3a}$$

Assuming the inductor loss dominates the tank loss and the quality factor Q_d and Q_s of L_d and L_s are high, which is typically true at the frequency range of several GHz, then R_d and R_s can be expressed by $\omega_d L_d Q_d(\omega_d)$ and $\omega_s L_s Q_s(\omega_s)$, respectively, where $\omega_d = 1/\sqrt{L_dC_d}$ and $\omega_s = 1/\sqrt{L_sC_s}$ are the resonant frequencies of the tanks at drain and source terminals, $Q_d(\omega_d)$ is the quality factor of L_d at frequency ω_d, and $Q_s(\omega_s)$ is the quality factor of L_s at frequency ω_s. By further defining $K = \sqrt{C_d/C_s}$, (5.3a) can be rearranged as

$$\frac{V_x}{V_{in}} = \frac{sg_m\left(\frac{1-N}{N}\right)}{s^2L_dC_d\left(1 + \frac{1}{(NK)^2}\right) + s\left[g_mL_d\left(\frac{1-N}{N^2}\right) + \frac{1}{\omega_d}\frac{1}{Q_d} + \frac{1}{\omega_s}\frac{1}{Q_s}\right] + 1} \tag{5.3b}$$

According to Barkhausen criterion, the phase of V_x/V_{in} needs to be 180° to guarantee the oscillation. So the oscillation frequency can be expressed as

$$\omega_0 = \frac{1}{\sqrt{L_dC_d}} \cdot \frac{1}{\sqrt{1 + \frac{1}{(NK)^2}}} = \frac{\omega_d}{\sqrt{1 + \left(\frac{\omega_d}{\omega_s}\right)^2}} \tag{5.4}$$

According to (5.4), if ω_s is much larger than ω_d, ω_0 can be approximated by $\omega_d = 1/\sqrt{L_dC_d}$ so that the oscillation frequency of the TF-VCO is only determined by the tank at drain terminal.

Equation (3.16) can be employed here to directly obtain the tank Q_T from the second-order transfer function given by (5.3b):

$$Q_T = \left[\left(\frac{\omega_0}{\omega_d} - (g_m R_d) \frac{N-1}{N^2} \right) \frac{1}{Q_d} + \frac{\omega_0}{\omega_s} \frac{1}{Q_s} \right]^{-1} \tag{5.5}$$

Since the resonant frequency of the secondary tank ω_s in this design is far above the oscillation frequency ω_0 and the inductor quality factor Q_s at higher frequency ω_s would be larger than Q_d at ω_0, the second term of (5.5) can be reasonably ignored. Using the approximation that $\omega_0 \approx \omega_d$, Q_T can be well approximated as below:

$$Q_T \approx \frac{1}{1 - (g_m R_d) \frac{N-1}{N^2}} \cdot Q_d \tag{5.6}$$

The term $(N-1)/N^2$ could be optimized with a maximum value of 1/4 when N equals to 2. So a maximum Q_T is achieved when $N = 2$. Assuming $g_m R_d = 2$, $L_d = 3$ nH, $\omega_d = 2\pi \cdot (4\,\text{GHz})$, $\omega_s = 4\omega_d$, $Q_d = 5$, and $Q_s = 10$, Fig. 5.5 compares the simulated Q_T and the calculated Q_T by using (5.5), which are quite close to each other.

Figure 5.5 also plots the simulated magnitude of the transfer function V_x/V_{in} at the oscillation frequency. It can be seen that $|V_x/V_{in}|$ is increased with N. Since a large $|V_x/V_{in}|$ indicates a large open-loop gain, a large N is preferred to make the TF-VCO easier to start up. However, according to (5.1), a small N is preferred to achieve a large maximal output amplitude. So the choice of N needs to take considerations of the Q_T, the start-up condition, and the maximum output amplitude comprehensively. In this design, $N \approx \sqrt{5}$ is chosen to guarantee the robust start-up at low supply voltages, for which the Q_T degradation is negligible compared to its maximum value obtained at $N = 2$. Meanwhile, according to (5.1), $N = \sqrt{5}$ still gives a maximum output amplitude of ~1.8 times larger than that of the conventional LC-VCO.

In addition to the enhancement of the tank Q_T, the TF-VCO also inherits the low phase-noise feature of the Colpitts oscillator because of the similar feedback mechanism. Figure 5.6a and b shows a comparison between a common-gate Colpitts VCO and the half-circuit of TF-VCO, where the transformer is represented by the equivalent circuit model in Fig. 2.3. For the Colpitts oscillator, the capacitors C_1 and C_2 form the feedback network. These capacitors constitute an important part of the total tank capacitance and thus limit the maximum achievable L/C ratio. This contradicts the requirement for a high tank impedance to achieve a low phase noise and low-power design. Furthermore, the capacitor dividers also limit the maximum oscillation frequency the Colpitts VCO can achieve. So the Colpitts VCO is not favorable for low-power applications. The TF-VCO, on the other hand, uses a single transformer for the feedback across the drain and source nodes and does not impose extra capacitance to the tank circuit, which is similar to the Hartley design [6, 7]. As a result, the TF-VCO can operate at a higher oscillation frequency.
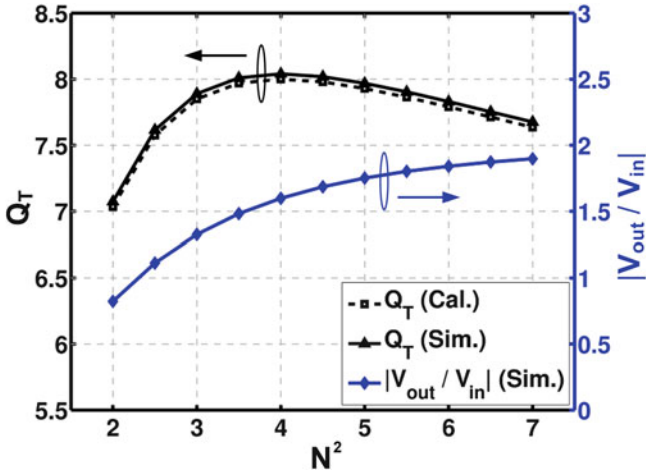
Fig. 5.5 Simulated and calculated tank QT and |Vout/Vin| as functions of N2
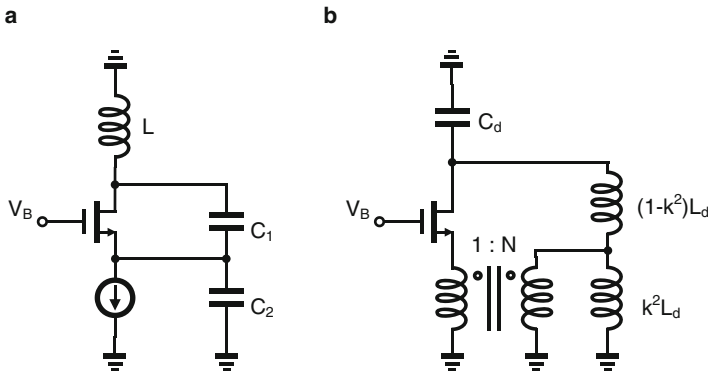

Fig. 5.6 Schematics of (**a**) Colpitts VCO and (**b**) the TF-VCO

The TF-VCO, which consists of cross-coupling of two single-ended VCOs, further enhances the cyclo-stationary noise property of the Colpitts structure. The idea is similar to the designs in [8] in which a single-ended Colpitts VCO uses a transformer to dynamically control the gate voltage bias or a differential Colpitts VCO uses two cross-coupled Colpitts VCO at the gate nodes. The TF-VCO shows advantage over [8] by using a single transformer rather than two capacitors for the feedback action.

In order to verify the cyclo-stationary noise advantage of the TF-VCO over the conventional LC-VCO, the impulse sensitivity function (ISF) $\Gamma(x)$ and $\Gamma_{\mathrm{eff}}(x)$ defined in Sect. 3.2.2 of the two topologies are compared. Two 4-GHz oscillators using the transformer tank and the conventional LC-tank are simulated with the same drain inductance value with quality factor of 5. The TF-VCO consumes
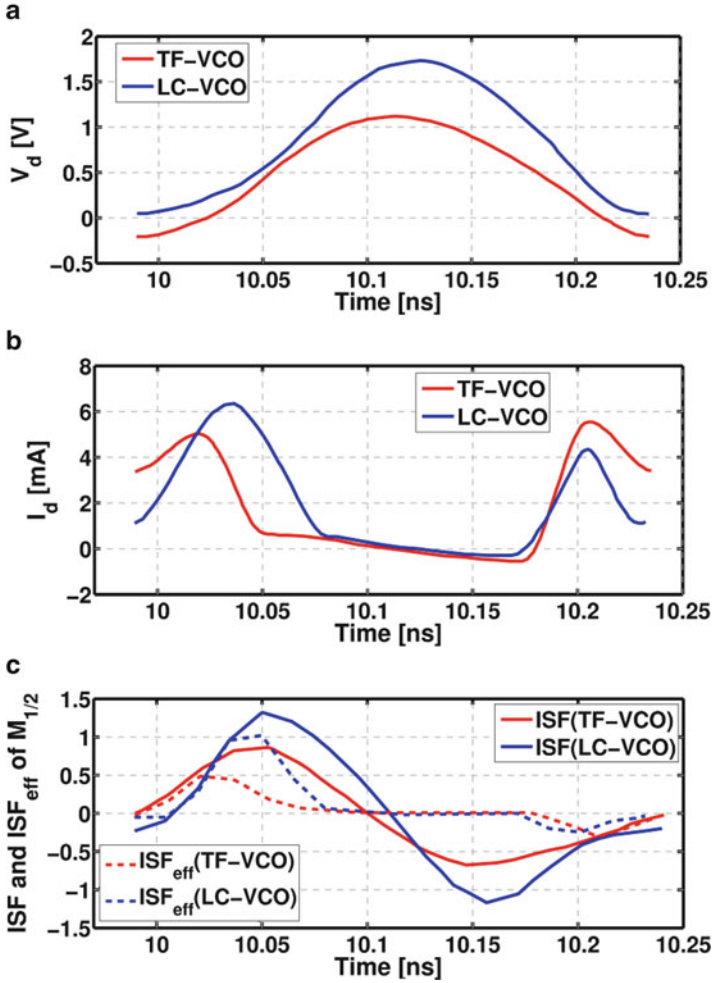
Fig. 5.7 Comparison between the TF-VCO and the conventional LC-VCO: (**a**) voltage waveforms of the drain, (**b**) current waveforms of the drain, and (**c**) ISF and ISFeff of the cross-coupled transistor M1/2

4.2 mA at a 0.5-V supply voltage, while the conventional VCO has the same current consumption but at a higher supply voltage of 0.9 V. A current source between transistor's drain and source nodes is included and acts as a noise impulse with a total charge of 7.8 fC. Figure 5.7 plots the voltage and current waveforms of the drain terminals and the ISFs of the two topologies, which shows that the TF-VCO gives much lower ISF and ISF_{eff} than those of the conventional LC-VCO. The simulated phase noise of the TF-VCO and LC-VCO are -105.6 dBc/Hz and -101.5 dBc/Hz at 1-MHz frequency offset, respectively.

Fig. 5.8 Schematic of the
PMOS TF-VCO
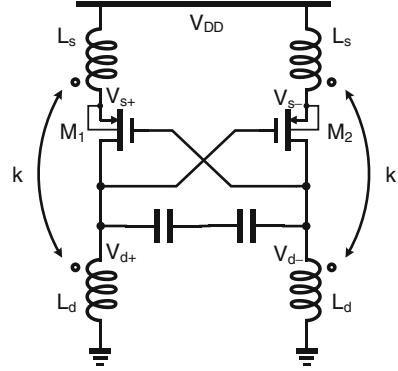
5.2.3   Circuit Implementation

To demonstrate the effectiveness of transformer-feedback techniques on reducing the supply voltage of the VCO, two TF-VCO prototypes are designed.

Figure 5.8 shows the first design, which employs PMOS cross-coupled pair and two single-ended transformers. The schematic is similar with that in Fig. 5.1a with the NMOS being replaced with PMOS transistors. To avoid forward biasing of the source-bulk junction when the instantaneous voltage at source terminal is larger than V_{DD}, the source and bulk of $M_{1/2}$ are connected together.

Figure 5.9 shows the single-ended transformer used in the PMOS TF-VCO. Here both the two inter-winding square spirals with three turns for the primary coils and a single turn for the secondary coil are implemented in the top metal layer. Under-passes are constructed with stacking of metal 4 and metal 5 to reduce their losses. The transformer has an outer diameter of 325 μm, an inner hole with a diameter of 120 μm, a metal width of 25 μm, and a spacing of 1 μm. From the measurement results at 1.4 GHz, the self-inductances of the primary and secondary coils are 2.6 nH and 0.55 nH, respectively, while the quality factors are 6 and 2.8, respectively. The coupling coefficient k is around 0.66.

The second design using NMOS transistors is exactly the same as that shown in Fig. 5.1a. To avoid the forward biasing of the source-bulk junction, the NMOS transistor is placed in a deep n-well which enables the direct connection between the bulk and source terminals. This design takes advantage of the higher mobility of the NMOS transistors compared to PMOS transistors so that the NMOS TF-VCO can oscillate at a higher frequency.

Besides, a single differential transformer as shown in Fig. 5.10 is employed in the NMOS TF-VCO. Compared to the single-ended inductor, the differential inductor can achieve a better quality factor because the magnetic coupling between the adjacent conductors reinforces the magnetic field and thus increase the inductance value while the series loss is unchanged [9]. The differential transformer also enjoys the same advantage over the single-ended transformer. In addition, the chip area occupied by the differential transformer is also reduced for a given inductance

Fig. 5.9 Layout of the
single-ended transformer
for PMOS TF-VCO
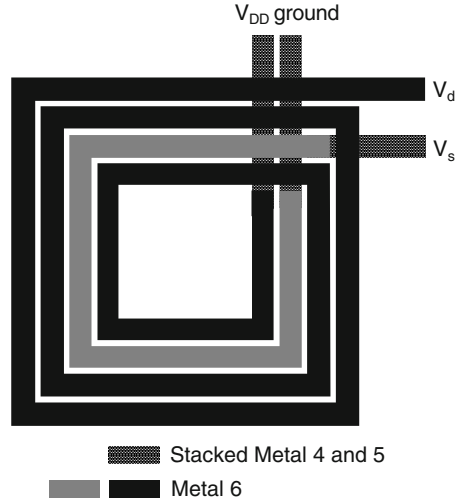
Fig. 5.10 Layout of the
differential transformer for
NMOS TF-VCO
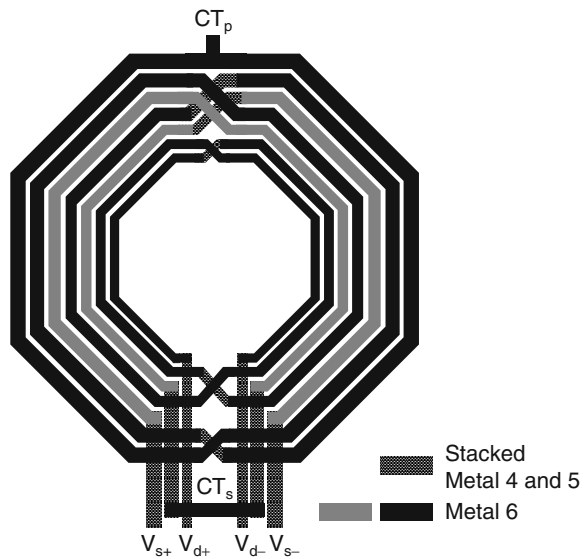
value. In this design, the quality factor of differential transformer is further opti-
mized by increasing the metal width progressively from the inner to the outer turn
[10]. As such, the series loss in the outer turn is reduced, while its substrate loss
associated with the wider metal width does not cause much degradation on the
quality factor since it is more close to the virtual ground at the inductor's center tap.
The transformer has an outer diameter of 343 μm and an inner hole with a diameter
of 156 μm. Both the two inter-winding octagonal spirals with five turns for the
primary coil and two turns for the secondary coil are implemented in the top metal
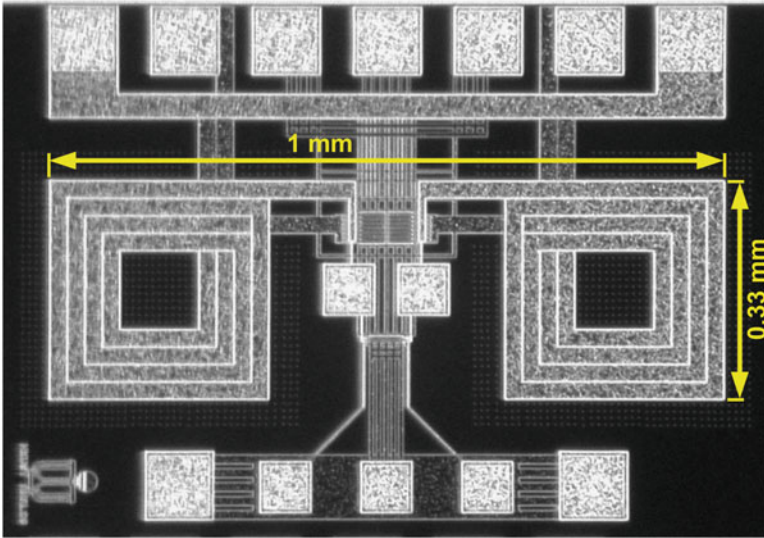
Fig. 5.11 Chip micrograph of the PMOS TF-VCO

layer. Metal width of the innermost turn is chosen to be 9 μm and is increased progressively to 15 μm for the outermost turn. From EM simulation, the self-inductance of the primary and secondary coils are 7.74 nH and 1.65 nH, respectively. The coupling coefficient is around 0.78.

5.2.4   Experimental Results

Both the PMOS and NMOS TF-VCO are fabricated in a standard 0.18-μm CMOS process with a nominal supply voltage of 1.8 V and 6 metal layers. The thickness of the top metal is 2-μm. The threshold voltages of the NMOS and PMOS devices are around 0.45 V and −0.52 V, respectively.

Figure 5.11 shows the chip micrograph of the PMOS TF-VCO with a core area of 0.33 mm^2. The PMOS TF-VCO consumes 1.46 mW at a supply voltage of 0.35 V.

For testing, an open-drain buffer is employed at the output of the VCO to drive the 50-Ω loading from spectrum analyzer. Figure 5.12 shows the output spectrum of the PMOS TF-VCO. Figure 5.13 compares the measured and simulated phase noise and supply sensitivity. The measured phase noise is −128.6 dBc/Hz at 1-MHz frequency offset from a center frequency of 1.38 GHz, while the measured frequency sensitivities to the supply voltage are −230 MHz/V. It can be seen that the improvement of phase-noise performance with the increase of supply voltage from the measurement is less significant compared to the simulated value, especially at the supply higher than 0.5 V. This is because the oscillation amplitude increases

Fig. 5.12 Output spectrum of the PMOS TF-VCO
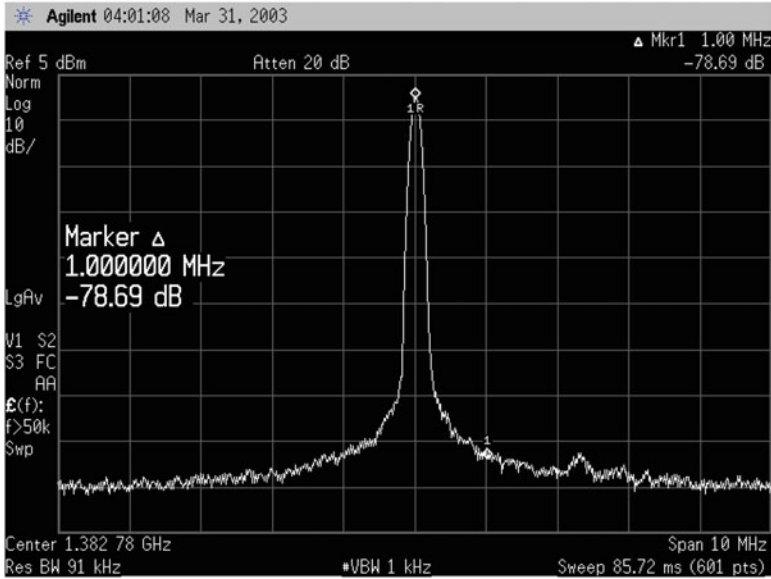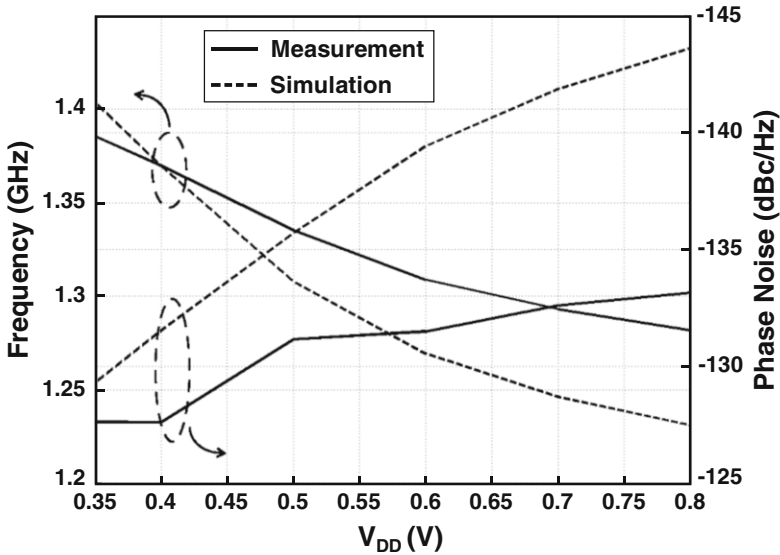

Fig. 5.13 Measured and simulated phase noise and supply sensitivity of the PMOS TF-VCO

with the supply voltage and the transient gate-drain voltage of the cross-coupled transistors approaches the breakdown voltage of 1.8 V. Since the simulated peak gate-drain voltage increases from 1.75 V at 0.6-V supply to 2.52 V at 0.8-V supply, the transistor model is no longer valid.

Figure 5.14 shows the micrograph of the 0.5-V NMOS TF-VCO with a core area of 0.23 mm^2. The NMOS TF-VCO consumes 0.57 mW at a supply voltage of 0.35 V.

The measured phase noise can be obtained from the closed-in spectrum as shown in Fig. 5.15, which is −119 dBc/Hz at 1-MHz frequency offset from a 3.7 GHz carrier at a varactor tuning voltage of 0.2 V. The TF-VCO is tuned by a simple AMOS varactor, and the measured and simulated frequency tuning curves are shown in Fig. 5.16. The frequency is tuned from 3.65 to 3.76 GHz when the tuning voltage varies from 0 to 0.5 V, which corresponds to a tuning range of 3.0 %. With a higher tuning voltage of 1.8 V, the tuning range will increase to 8.4 %. Phase-noise performance across the tuning range is also plotted in Fig. 5.16. It can be seen that the phase noise is degraded as the VCO gain increases since the AM-PM noise conversion becomes significant. The measured and simulated frequency sensitivities to the supply voltage are plotted in Fig. 5.17 at a fixed tuning voltage of 0.9 V. The supply sensitivity is around 273 MHz/V when V_{DD} changes from 0.35 to 0.8 V. Figure 5.17 also shows the measured phase noise as a function of the supply voltage. The phase noise can be reduced by increasing the supply voltage at the cost of a large power consumption.

Table 5.1 summarizes the performance of the two low-voltage low-power TF-VCO prototypes and compare them with the published state-of-the-art low-power VCOs. The average FoM of the NMOS TF-VCO is larger than both the VCO reported in [12] and [14] and around 2–3 dB lower than that of the VCO reported in [11] or [13]. However, the class-C VCO in [11] requires a relatively high supply voltage of 1.0 V for achieving the best FoM of 195. Since the class-C topology suffers from degraded maximum output amplitude as discussed in Sect. 3.3.3, the cross-coupled transistor would enter the deep triode region when turned on if the supply voltage is further reduced, which would cause a sharp degradation of the FoM. For the enhanced-swing differential Colpitts VCO demonstrated in [13], since two separate differential inductors are needed, its core area would be larger than that of the NMOS TF-VCO employing only a single differential transformer when both VCOs operate at the same frequency.

5.3   Transformer-Coupled QVCO (TC-QVCO)

5.3.1   Topology and Circuit Model

Figure 5.18 shows the schematic of the transformer-coupled QVCO (TC-QVCO). Two LC-VCOs are coupled passively by on-chip transformers instead of actively by coupling transistors as in conventional QVCOs to generate quadrature outputs. The architecture of each VCO is similar to the TF-VCO presented in Sect. 5.2. The primary coil of the transformer (L_d) at the drain of each VCO is used to resonate with the total output capacitance and to simultaneously couple to the secondary coil
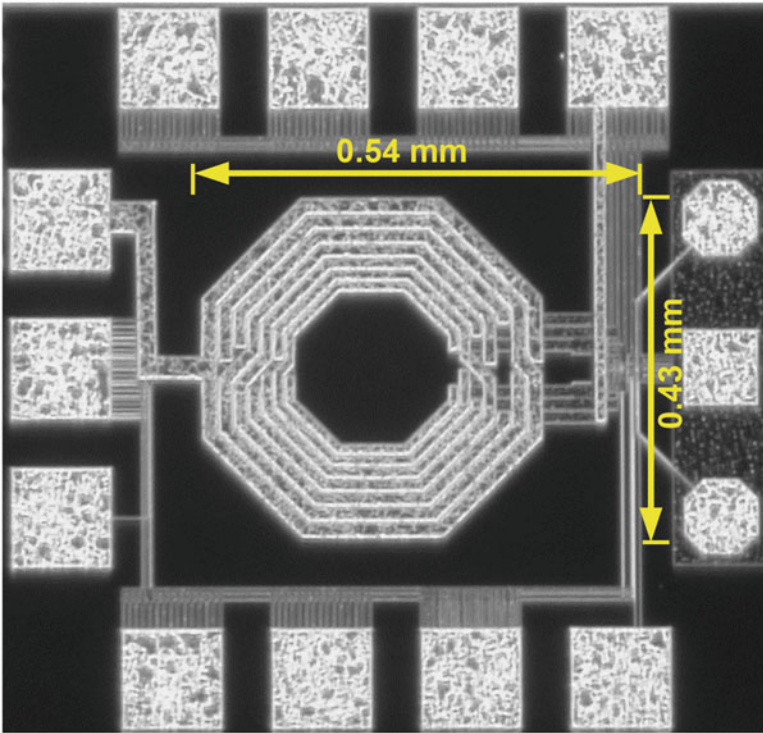
Fig. 5.14 Chip micrograph of the NMOS TF-VCO
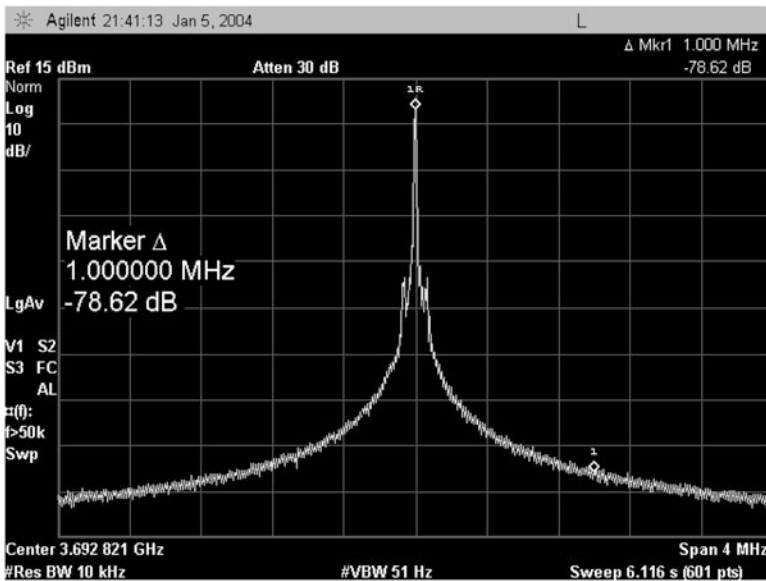
Fig. 5.15 Output spectrum of the NMOS TF-VCO
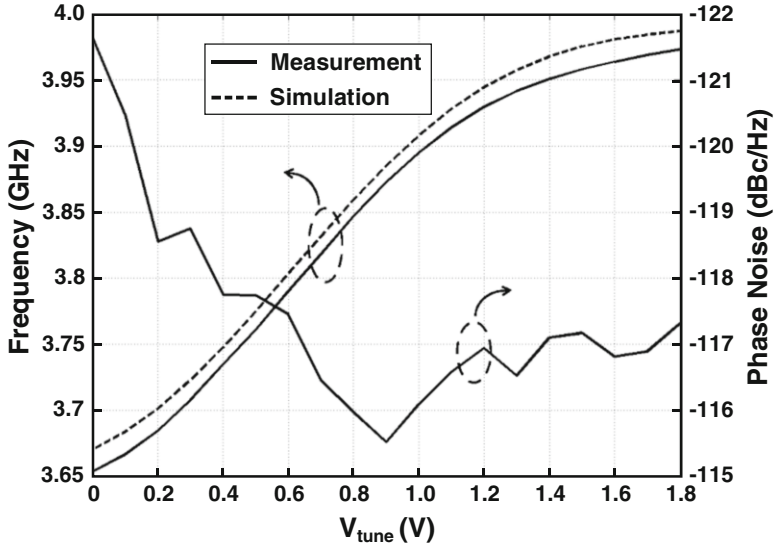
Fig. 5.16 Measured and simulated phase noise and oscillation frequency of the NMOS TF-VCO as functions of the varactor tuning voltage ($V_{DD} = 0.5$ V)
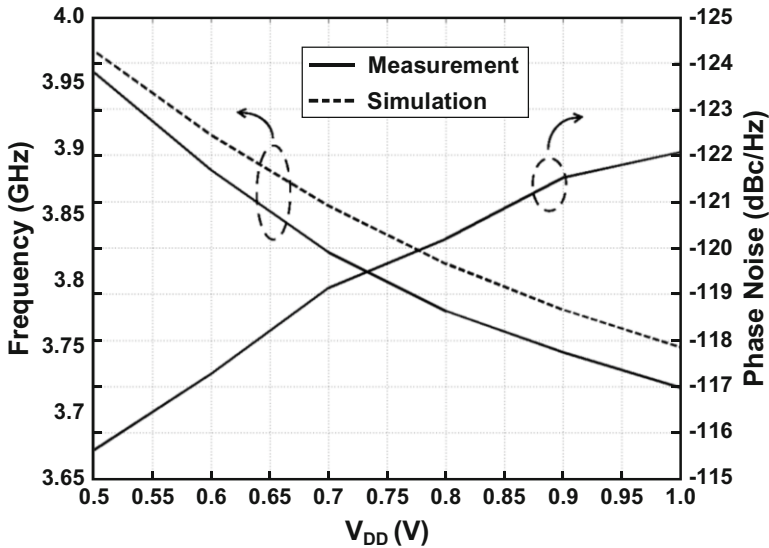
Fig. 5.17 Measured and simulated phase noise and oscillation frequency of the NMOS TF-VCO as functions of supply voltage

(L_s) at the source of the other VCO. As such, the parasitic capacitance and the power contributed by the coupling transistors are removed, which results in higher operating frequency, larger tuning range, and lower power consumption. Moreover,

Table 5.1 Performance summary and comparison

References	Technology	Frequency (GHz)	Power (mw)	Supply (V)	PN@1 MHz (dBc/Hz)	FOM (dBc/Hz)	Core area (mm^2)	Topology
[11]	0.13-μm CMOS	4.9 (10.5 %)	1.3	1.0	−122.5[a]	195[b]	0.33[c]	Class-C
[12]	0.18-μm CMOS	4.5 (0 %)	0.159	0.3	−109	190	0.29	Class-C & Class-B
		4.5 (0 %)	0.114	0.2	−104	187		
[13]	0.13-μm CMOS	4.9 (2.5 %)	3	0.475	−126.2[a]	196.2	0.27[c]	Enhanced swing diff. Colpitts
[14]	65-nm CMOS	2.53 (29 %)	0.28	0.85	−116.6[a]	190.2	0.13	Current reuse
This work	0.18-μm CMOS	1.4 (0 %)	1.46	0.35	−129	190[b]	0.33	PMOS TF-VCO
		3.8 (8.4 %)	0.57	0.5	−119	193[b]	0.23	NMOS TF-VCO

[a]Phase noise normalized from 3-MHz offset in the original measured data from the references
[b]Average value across the frequency tuning range
[c]Core area estimated from the chip micrograph
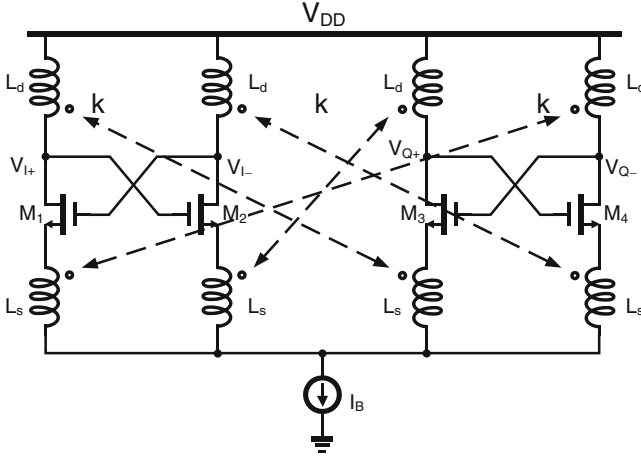
Fig. 5.18 Transformer-coupling QVCO (TC-QVCO)

by utilizing the transformer coupling, the thermal noise and the flicker noise of the active coupling devices are completely removed. In addition, the transformers enable signals at the source terminals to swing below the ground, which helps effectively reduce the voltage headroom and the minimum supply voltage as discussed in Sect. 5.2.

To gain more insight into the operation of the TC-QVCO, the schematic in Fig. 5.18 is redrawn as in Fig. 5.19. Similar to the P-QVCO, the TC-QVCO can be rearranged as a ring structure with active coupling replaced by magnetic coupling. Figure 5.20a shows the linear model of each stage with the transformer replaced by its equivalent model given in Fig. 2.3. All the capacitances at the drain including the frequency tuning capacitance, parasitic capacitance, and the loading capacitance are lumped into the total capacitance C. For simplicity, the magnetic coupling coefficient k of the transformer is assumed to be 1, and the loss of the transformer is being modeled as a parallel resistance R. The equivalent circuit can be simplified as shown in Fig. 5.20b, where N is the turn ratio between the primary and secondary coils defined as $N = \sqrt{L_p/L_s}$. It can be seen that the impedance looking into the source node is boosted up by N^2 times when presented to the tank at the drain.

As shown in Fig. 5.20b, the current components injected into the tank can be expressed as

$$i_1 = -g_m \left(V_{I+} - \frac{V_{Q+}}{N} \right) \tag{5.7a}$$

$$\frac{i_2}{N} = \frac{g_m}{N} \left(V_{Q+} - \frac{V_{I-}}{N} \right) \tag{5.7b}$$

So the total current injected into the tank can be calculated by summing the current phasors i_1 and i_2/N together:
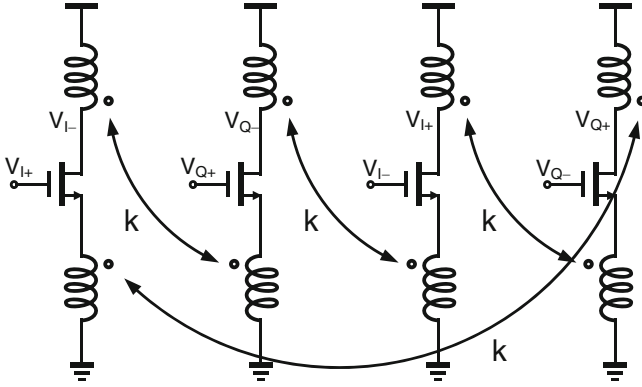
Fig. 5.19 Ring configuration of the TC-QVCO circuit
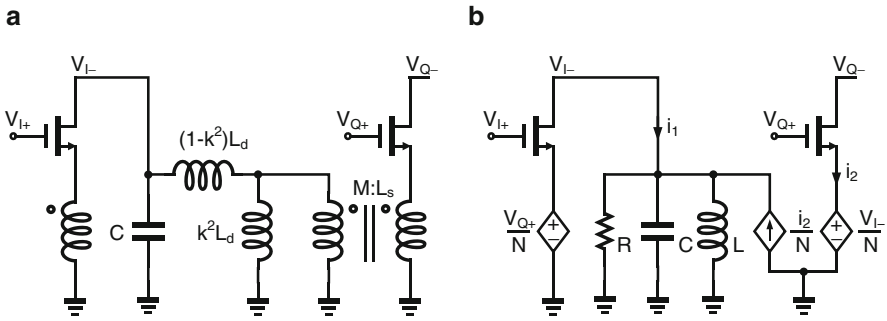
Fig. 5.20 Equivalent circuit for the TC-QVCO: (**a**) $k \neq 1$ and (**b**) $k = 1$

$$i_{tank} = -g_m \left(1 - \frac{1}{N^2} \right) V_I + g_m \left(\frac{2}{N} \right) V_Q \tag{5.7c}$$
$$= i_I + i_Q$$

where i_I and i_Q are the in-phase and quadrature-phase currents, respectively. The in-phase current is mainly generated by the cross-coupled transistor, while the quadrature-phase current comes from both the transformer and the cross-coupled transistor, which is inversely proportional to N. Similar to the P-QVCO, the tank voltage is also in phase with I_I.

According to (5.7c), the coupling strength m of the TC-QVCO is given by

$$m = \frac{i_Q}{i_I} = \frac{2N}{N^2 - 1} \tag{5.8}$$

which would decrease as N increases.

5.3.2 Oscillation Frequency

Since the load of the TC-QVCO can be modeled as an equivalent parallel RLC resonator, the admittance of the tank impedance can be expressed as

$$A(j\omega) = A_I(j\omega) = A_Q(j\omega) = \frac{1}{R} + j\frac{Q_T}{R}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) = G + jY(j\omega) \qquad (5.9)$$

where $\omega_0 = \sqrt{LC}$ is the resonance frequency of the tank and R and Q_T are the tank impedance and quality factor at ω_0, respectively. Applying Kirchhoff's voltage law to the in-phase and the quadrature-phase resonators, the following equations can be derived to describe the behavior of the TC-QVCO:

$$V_I = g_m\left[\left(1 - \frac{1}{N^2}\right)V_I - \frac{2}{N}V_Q\right]\frac{1}{A_I(j\omega)} \qquad (5.10a)$$

$$V_Q = g_m\left[\left(1 - \frac{1}{N^2}\right)V_Q + \frac{2}{N}V_I\right]\frac{1}{A_Q(j\omega)} \qquad (5.10b)$$

By replacing $V_I = V_0$ and $V_Q = V_0 e^{j\phi}$ in (5.10a) and (5.10b), ϕ is solved to be either $\pi/2$ or $-\pi/2$ which represents two possible oscillation modes of the TC-QVCO. So the corresponding oscillation frequencies ω_{osc1} and ω_{osc2} can be derived by substituting $\phi = \pm\pi/2$ in (5.10a) and (5.10b) and equating the imaginary parts:

$$\omega_{osc1/2} = \omega_0\left[\pm\frac{m}{2Q_T} + \sqrt{\left(\frac{m}{2Q_T}\right)^2 + 1}\right] \qquad (5.11)$$

where m is the coupling strength defined in (5.8). Figure 5.21 plots the normalized oscillation frequency as a function of the transformer turn ratio N assuming the tank quality factor is 6. It can be seen that the deviation of the oscillation frequency from the resonant frequency increases when the coupling strength increases. This is similar to the situations for both the P-QVCO and the S-QVCO, in which a larger quadrature-phase current injected into the tank results in a larger phase shift to be compensated by the resonator and thus a larger deviation of the oscillation frequency from the tank resonant frequency. So the similar method by adding phase shift in the coupling path as discussed in Sect. 3.4 can also be employed here to avoid the bimodal oscillation and guarantee a well-controlled IQ phase sequence.

Fig. 5.21 Normalized oscillation frequencies as functions of the transformer turn ratio N (QT = 6)
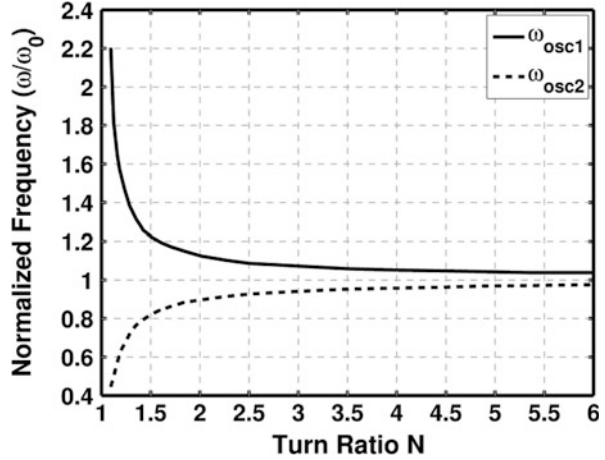
5.3.3 IQ Imbalance and Phase Noise

When the TC-QVCO is implemented in the CMOS process, there exist inevitable component mismatches between the two resonators, which would cause the phase and amplitude imbalance and thus cause the performance degradation of wireless transceivers. As discussed earlier, for the P-QVCO, the phase noise and the phase error are strong functions of the coupling strength m. The phase and amplitude errors decrease, while the phase noise increases with the increase of the coupling strength. This trade-off is more relaxed in the S-QVCO as the coupling strength is relatively constant.

To simulate the phase and amplitude errors of the TC-QVCO in presence of the component mismatches, a 0.1 % mismatch between the tank capacitances of the two resonators is assumed. The phase and amplitude errors of the TC-QVCO are translated into the sideband rejection (SBR), which measures the power ratio of the wanted sideband to the unwanted sideband. Figure 5.22 shows the simulated phase noise and SBR as functions of N for the TC-QVCO with a tank Q_T of 6 and a transformer-coupling coefficient of 0.7. The oscillation frequency is set to be around 17 GHz. When N is small, the source impedance will load the tank and degrade the effective quality factor significantly, which is similar to the case in the TF-VCO discussed in Sect. 5.2. Besides, small N also results in a large coupling strength which further degrades the phase noise. When N becomes large, the coupling strength is reduced, and the phase noise is improved, but the QVCO becomes more sensitive to the component mismatches, which degrades the SBR.

Fig. 5.22 Simulated phase noise and SBR of the TC-QVCO as functions the transformer turn ratio N
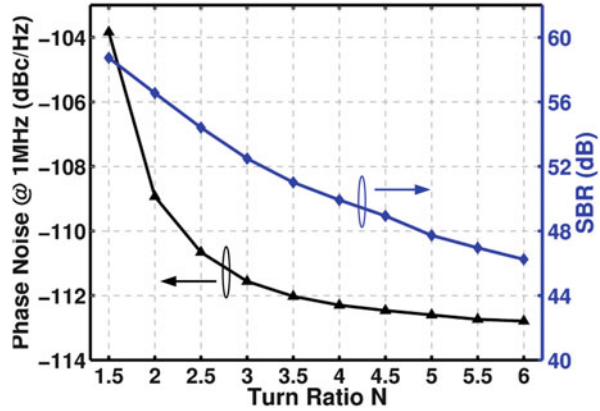
So the transformer turn ratio N should be chosen as a compromise between phase accuracy and phase noise.

Notice that all the above analyses and results are obtained assuming that the magnetic coupling coefficient k of the transformer is equal to 1 for simplicity. In practice, k of a tightly coupled transformer at 17 GHz is around 0.6–0.8. As proved in Appendix A.1, when k is close to 1, the results obtained before is still applicable by replacing N with the effective turn ratio $N_{eff} = N/k$ given by (A.5).

To fairly compare the phase noise of QVCOs with different coupling methods, it is important to keep the same level of phase error since there always exists trade-off between the phase noise and the phase error in any QVCO topology. Figure 5.23 compares the simulated phase-noise performance of the P-QVCO (Fig. 3.24), the S-QVCO (Fig. 3.28), the SHC-QVCO (Fig. 3.29), and the TC-QVCO. All QVCOs are designed to have the same level of phase errors under 1-V supply voltage at 17 GHz. The quality factors of the inductor and transformer are both assumed to be 6. From Fig. 5.23, the TC-QVCO shows significant improvement in phase noise compared to the P-QVCO and is closed to that of S-QVCO due to the structural similarity. The TC-QVCO shows comparable performance with the SHC-QVCO at high frequency offset although the tank Q_T is degraded due to the deviation from the resonant frequency. An alternate super-harmonic QVCO architecture in [15] shows improved phase-noise performance at the expense of two more LC resonators.

5.3.4 Circuit Implementation

Figure 5.24 shows the complete schematic of the TC-QVCO, where 2-bit binary-weighted SCAs are used for coarse frequency tuning, while AMOS varactors are used for fine frequency tuning. To further reduce the parasitic off capacitance, the switches in the SCA are drawn in square-gate structure (donut structure) [16, 17] as

Fig. 5.23 Comparison of
simulated phase noise of the
P-QVCO, the S-QVCO, the
SHC-QVCO, and the
TC-QVCO at 17 GHz
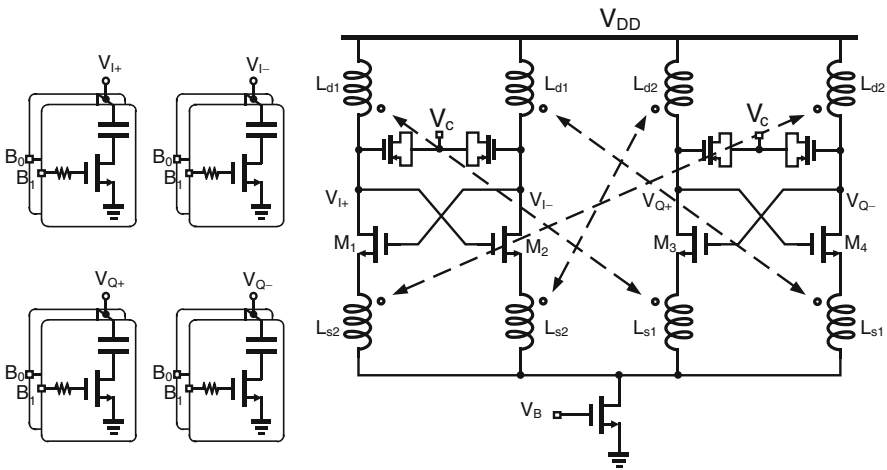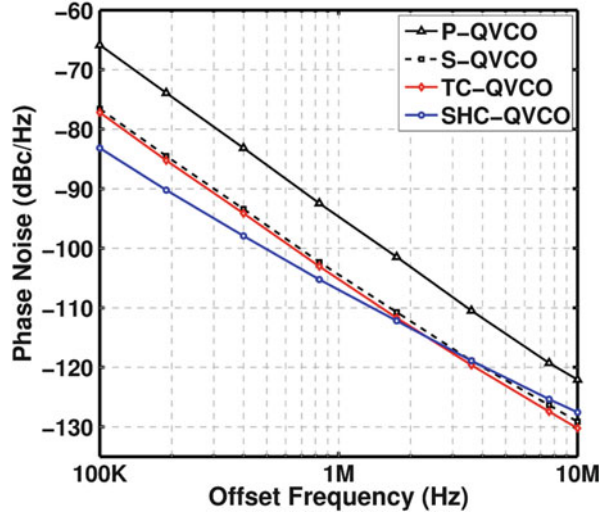
Fig. 5.24 Complete schematic of the TC-QVCO

shown in Fig. 5.25. For this structure, the gate of the transistor encloses the drain
junction, which minimizes the drain junction and maximizes the grounded source
junction. So the parasitic capacitor at the drain is reduced at the cost of larger
parasitic capacitor at the source. However, the increase of the source capacitor is
not important as it is not directly connected to the output tank.

As the TC-QVCO is fully differential, two symmetrical octagonal differential
transformers as shown in Fig. 5.26 are used to implement (L_{d1} and L_{s1}) and (L_{d2} and
L_{s2}) to achieve higher quality and smaller area compared with its single-ended
counterpart. The top thick metal is employed for both the primary and secondary

Fig. 5.25 Layout of the square-gate transistor structure
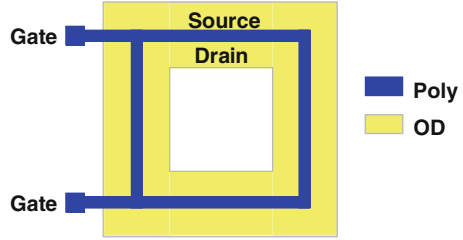
Fig. 5.26 Layout of the transformer
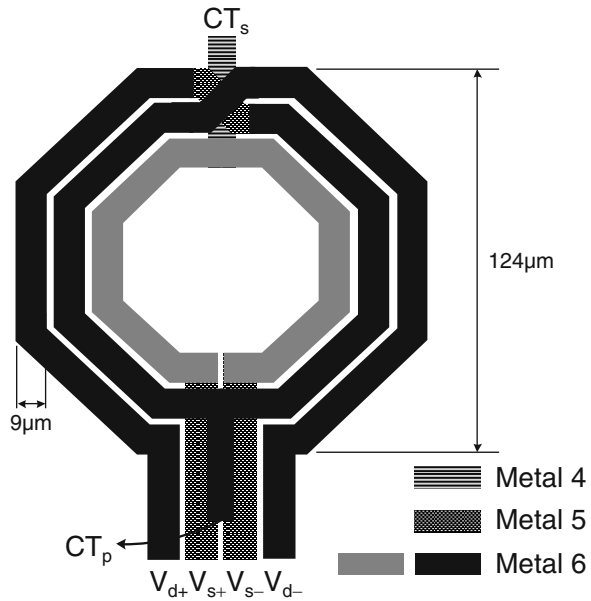
coils to maximize both the quality factor and the self-resonant frequency. To achieve large inductance ratio, the 2-turn primary coil is laid totally outside the single-turn secondary coil. The bias can also be applied through the center tap nodes (CT_p, CT_s) without affecting the RF performance. From the measurement, L_d and L_s are 328 pH and 97 pH, respectively, which corresponds to a turn ratio N of 1.84. The Qs of the L_d and L_s are 5.2 and 2.5, respectively. The coupling coefficient k is around 0.59.

To measure the phase accuracy, a single-sideband (SSB) mixer as shown in Fig. 5.27 is included on chip. The phase and amplitude errors of the QVCO, which are very difficult to measure directly and reliably at high operating frequencies, are translated into the sideband rejection (SBR) by using the SSB mixer, which measures the power ratio of the wanted sideband to the unwanted sideband. The IQ outputs of the TC-QVCO are directly connected to the LO ports of the SSB mixer, while the baseband IQ signals are applied off chip. By monitoring the RF_{out} ports with a spectrum analyzer, the SBR and thus the phase accuracy can be measured [18]. To reduce the mismatches due to the long LO interconnection, the connection is being shielded by a ground cave at expense of slightly larger parasitic capacitance.
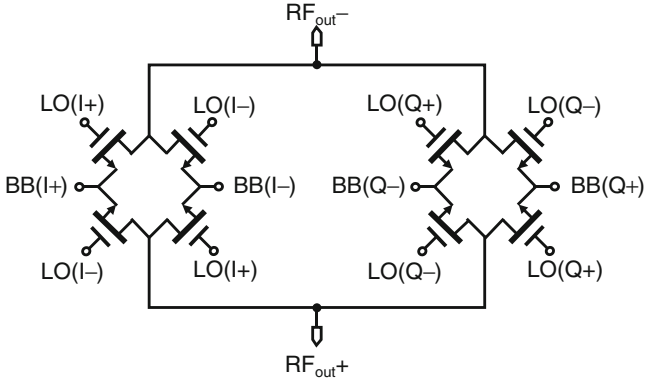
Fig. 5.27 Schematic of the SSB mixer for phase accuracy measurement

5.3.5 *Experimental Results*

The TC-QVCO is fabricated in a 0.18-μm CMOS process. Figure 5.28 shows the chip microphotograph with a core area of 0.126 mm^2.

Besides the transformer testing structure, other passive devices, including the accumulation-mode varactors and SCAs, are also characterized using individual test structures. Two-port S-parameters of the devices are measured using a vector network analyzer with proper calibration. For the AMOS varactor, the capacitance can be tuned from around 26–67 fF when the tuning voltage changes from 0 to 1.8 V, which corresponds to a capacitance tuning range of $C_{max}/C_{min} = 2.58$, with a minimum quality factor of 12. For the SCA, the capacitance can be switched from 22.5 to 47.5 fF, which corresponds to a capacitance tuning range of $C_{max}/C_{min} = 2.11$, and the minimum quality factor across the tuning range is measured to be 24. The size of the switch can be further reduced if large tuning range of SCA is preferred at the cost of degraded quality factor.

To measure the phase noise, the differential signals are combined using an external power combiner and amplified by an external amplifier before going to the spectrum analyzer. Figures 5.29 and 5.30 show the measured frequency spectrum and the tuning characteristic of the TC-QVCO, respectively. The TC-QVCO can be tuned from 14.8 to 17.6 GHz with a tuning voltage from 0 to 1.8 V, corresponding to a tuning range of 16.5 %.

Figure 5.31 shows the measured phase-noise plot. Drawing 5 mA from a supply voltage of 1 V, the TC-QVCO measures a phase noise of −110 dBc/Hz at 1-MHz offset from the 17-GHz carrier frequency. The TC-QVCO is also tested at lower supply voltages and can operate properly for a supply voltage as low as 0.6 V. Figure 5.32 shows the phase-noise plot at a 0.6-V supply, from which the measured phase noises at 1-MHz and 10-MHz offset frequency are −102.6 dBc/Hz and −125.3 dBc/Hz, respectively.

In order to measure the quadrature accuracy, the TC-QVCO together with a single-sideband mixer (Fig. 5.27) is also implemented as a separate testing
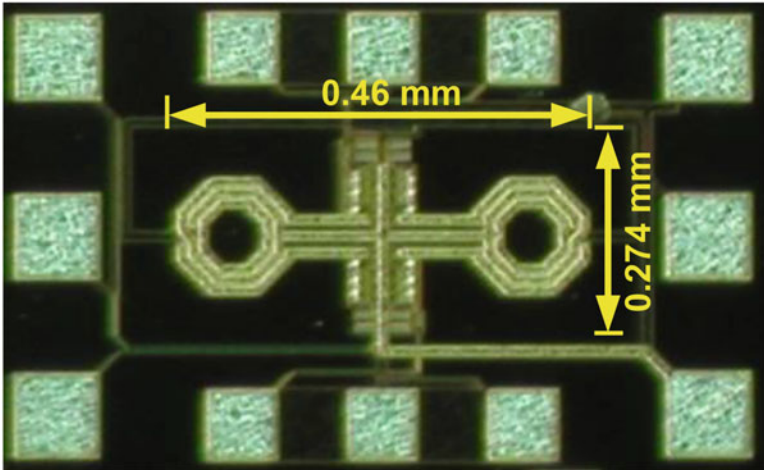
Fig. 5.28 Chip micrograph of the TC-QVCO
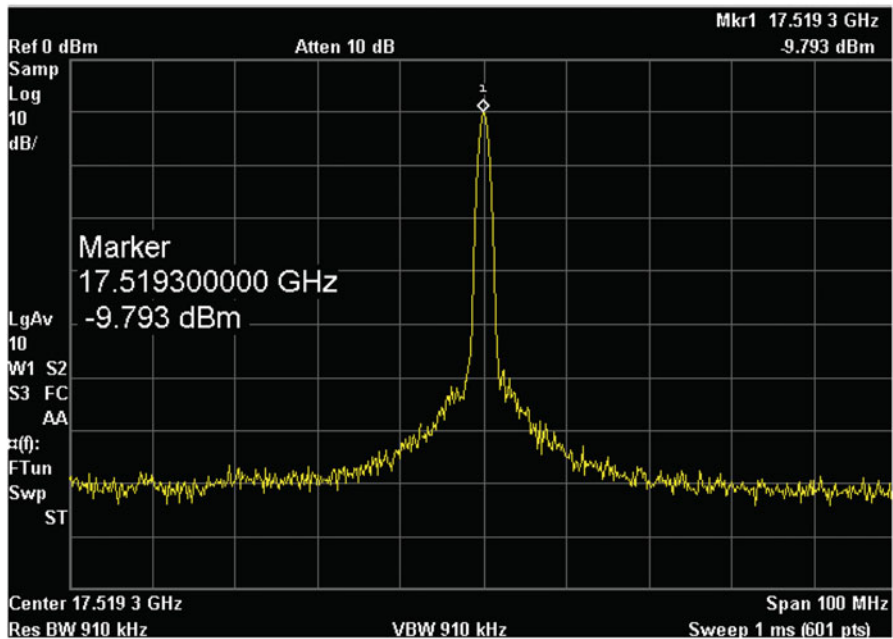
Fig. 5.29 Measured frequency spectrum of the TC-QVCO

structure, where the baseband low-frequency IQ signals are generated off chip by the vector signal generator. Figure 5.33 shows the up-converted frequency spectrum at the RF_{out} ports. The worst-case SBR is 38 dB among the measurement results of four samples. The output frequency of the SSB mixer is lower than that of
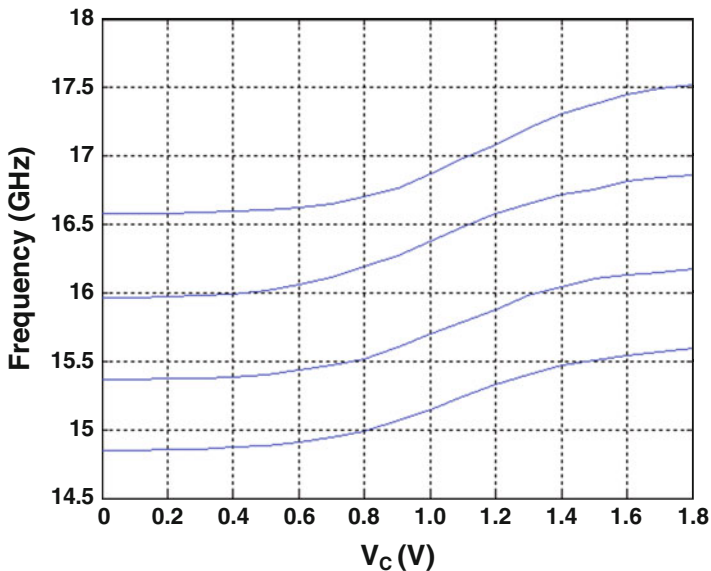
Fig. 5.30   Measured frequency tuning characteristic of the TC-QVCO
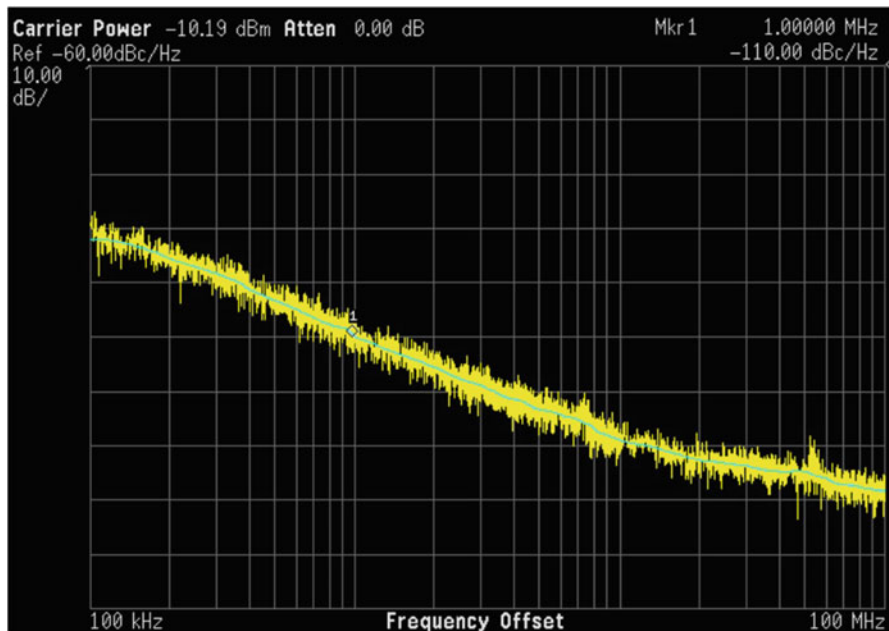
Fig. 5.31   Measured phase-noise plot at 1-V supply voltage
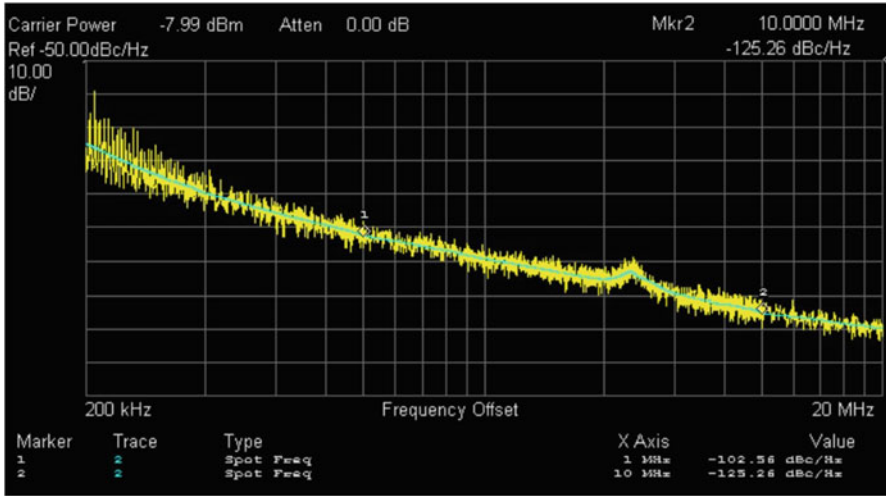
Fig. 5.32 Measured phase-noise plot at 0.6-V supply voltage
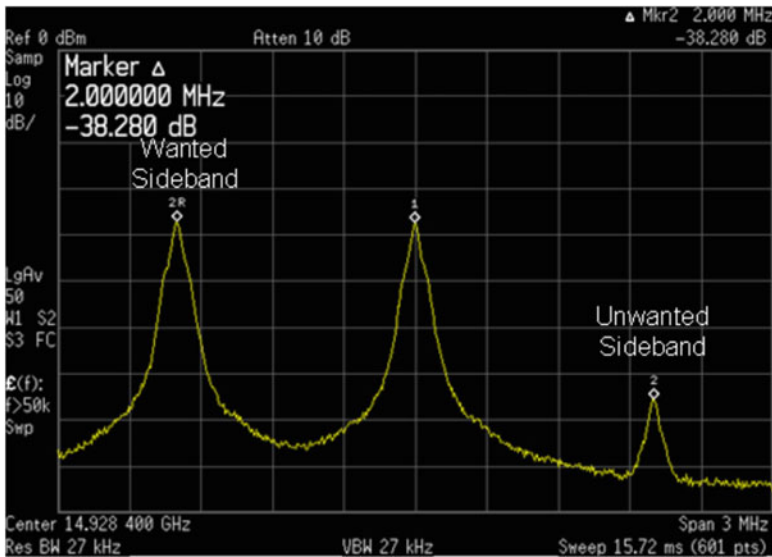
Fig. 5.33 Measured SBR at the output of the SSB mixer

the standalone TC-QVCO due to the extra parasitic capacitance from the SSB mixer. Assuming that the IQ mismatch of the low-frequency external signals is negligibly small, the measured SBR of >38 dB is equivalent to a phase error of <1.4° [5.5].

Table 5.2 summarizes the measured performance of the TC-QVCO and compares it with those of published state-of-the-art CMOS QVCOs.

Table 5.2 Performance summary and comparison

References	Technology	Frequency (GHz)	Supply (V)	Power (mw)	PN @ 1 MHz (dBc/Hz)	FOM (dBc/Hz)	Phase error	Topology
[10]	0.25-μm CMOS	1.8 (17 %)	2.5	20	−133.5[a]	185.5	3°	P-QVCO
[19]	0.35-μm CMOS	1.8 (18 %)	2	50	−130.5[a]	182	0.25°	S-QVCO
[20]	0.18-μm CMOS	1.1 (28 %)	1.8	5.4	−127.5[a]	181	N/A	Substrate-coupled QVCO
[21]	0.25-μm CMOS	4.88 (13 %)	2.5	22	−125	185	2.6°	SHC-QVCO1
[15]	0.18-μm CMOS	5.1 (17 %)	1.8	27.7	−132.6	192	N/A	SHC-QVCO2
[22]	0.25-μm CMOS	1.57 (24 %)	2.0	30	−137.9[b]	187.1	N/A	P-QVCO with 90° phase shift in coupling path
[23]	65-nm CMOS	4.8 (67 %)	1.2	6–20	−114.1[c]	176.5	<1.5°	P-QVCO with transformer coupling
This work	0.18-μm CMOS	17 (16.5 %)	1.0	5	−110	187.6	1.4°	TC-QVCO

[a]Phase noise normalized from 3-MHz offset in the original measured data from the references
[b]Phase noise normalized from 600-kHz offset in the original measured data from the references
[c]Phase noise normalized from 10-MHz offset in the original measured data from the references

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Chapter 6
Transformer-Based Dual-Mode VCO

6.1 Introduction

The ever-increasing demand for global mobility and multimedia services has motivated realizations of multimode, multiband, and multi-standard wireless communication systems. Software-defined radios (SDR) that can cover not only all the existing wireless standards (including cellular, WLAN, WPAN, broadcast, positioning, etc.) but also future standards would be a promising and attractive platform. Such radios require a local oscillator capable of ultrawide frequency tuning range (TR) with sufficiently high spectrum purity to support diverse specifications.

In order to achieve a wide-tuning range using the capacitive-tuning method, a large C_{max}/C_{min} ratio is required, which would inevitably degrade the Q of the SCA or the varactor. Furthermore, even if it does not consider the degradation of capacitor Q, the FoM cannot be kept constant over a wide frequency tuning range. To elaborate this point, firstly the design goal is set to keep the phase noise reduced with frequency in a slope of 20 dB/dec as shown in Fig. 6.1a. The phase-noise expression of (3.18) is rearranged as below:

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{kTF}{\beta^2 I_0^2 R_P}\left(\frac{1}{Q_T}\frac{\omega}{\Delta\omega}\right)^2\right] \tag{6.1}$$

where I_0 is the VCO current consumption, R_p is the tank parallel resistance, and β is the current efficiency. Assuming that tank Q_T is kept constant across the frequency tuning range from f_1 to f_2, then to guarantee that the phase noise is proportional to ω^2, $I_0^2 R_p$ needs to be kept constant when ω changes. Assuming that R_p is still dominant by the inductor loss, then $R_p \approx Q_L \cdot (\omega L) \propto \omega$. So $I_0 \propto 1/\sqrt{\omega}$ which indicates that the power consumption at the low-frequency end needs to be increased as shown in Fig. 6.1b. In case of FoM, according to (3.34), it can be seen that $FoM \propto 1/\sqrt{\omega}$, which indicates that FoM would degrade at the
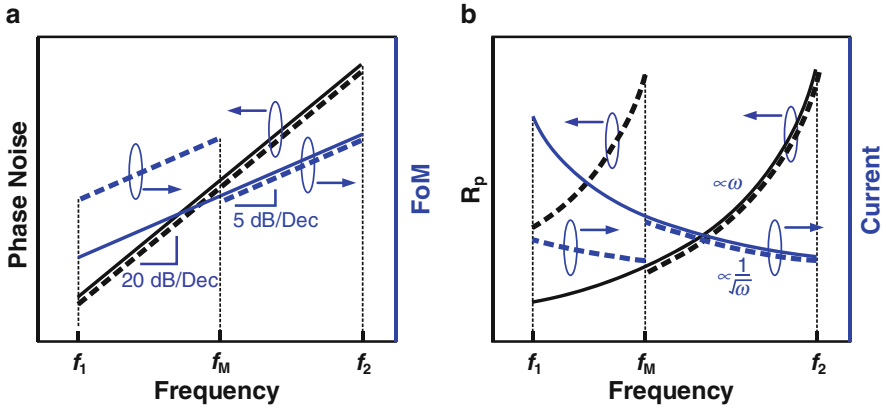
Fig. 6.1 (**a**) Phase noise and FoM as functions of oscillation frequency with x-axis in log scale; (**b**) tank parallel resistance R_P and current consumption as functions of oscillation frequency with x-axis in normal scale. (The *solid line* and *dash line* represent the cases using a single inductor and two inductors, respectively)

low-frequency end as shown in Fig. 6.1a. For example, if $f_2 = 2f_1$, the required current needs to be increased by ~1.4 times, and the FoM will degrade by 1.5 dB at the low-frequency end as compared with the current and FoM at the high-frequency end. If considering the loss from the SCA and the varactors, R_p will further decrease significantly, which would result in an even larger power consumption as well as an even worse FoM at the low-frequency end.

If multiple inductors are used to create multiple frequency bands, the power and FoM degradation can be alleviated. Here consider the case with two inductors for simplicity. If L_2 with the same inductance value as that in the single inductor case is employed only to cover frequency range from f_m to f_2 (assuming $f_2 = \alpha f_m$), then L_1 of a larger inductance $L_1 = \alpha L_2$ can be employed. Since the use of a larger L_1 makes R_p at f_m the same as that at f_2, the current consumption and the FoM at f_m can also be kept the same as those at f_2. As a result, the increase of power consumption and the degradation of FoM can be significantly reduced across the whole tuning range. For example, by assuming $f_2 = 2f_1$ and choosing $f_m = \sqrt{f_1 f_2}$, the FoM degradation can be reduced to 0.75 dB, and the required current only needs to be increased by ~1.2 times across the whole tuning range from f_1 to f_2.

To extend the frequency tuning range while still keeping the constant power and FoM performance, multiple VCOs with optimized inductance values are used in [1, 2]. However, these solutions are quite inefficient in terms of chip area and cost. Multiple frequency bands can also be generated by employing single-sideband mixers [3, 4], but narrowband LC filtering is required to overcome the sideband-rejection problem and the spurious emission caused by the mixing nonlinearity and mismatches, which is not an area-efficient solution either. To keep a compact chip area, switching inductors are used to realize dual-band or wideband VCOs [5–8]. However, as discussed in Sect. 3.6, the use of switches inevitably introduces

extra loss and degrades the inductor Q. Consequently, the switches contribute large parasitic capacitance, which in turn results in the reduced tuning range.

Recently, multiple frequency peaks of high-order LC resonant tanks based on multi-tapped inductors or transformers are exploited to realize multiband or wideband VCOs [9–13]. In [9], multi-tapped inductors are used to realize a fourth-order tank, and based on one-port oscillations, a 0.8-GHz/1.8-GHz dual-mode VCO is demonstrated with phase noise good enough for GSM/DCS/PCS standards. However, the use of multiple inductors still consumes large chip area. In [10], a differential dual-mode VCO is introduced and demonstrated using transformers with small turn ratio and moderate coupling. To cover a wide tuning range from 3.4 to 7.0 GHz, a one-port oscillator configuration is employed for the low-band mode, while a two-port oscillator configuration is used for the high-band mode. Making use of transformers with large turn ratio and high coupling, [11] demonstrates a 4-GHz/10-GHz dual-band QVCO and shows that one-port oscillators can be stabilized with a notch-peak cancelation technique. Finally, exploiting a loosely coupled 3-coil transformer, [13] presents a one-port triple-mode wideband VCO tunable from 1.28 to 6.06 GHz.

As demonstrated in these works, because the inductive components of a high-order LC tank can be integrated as transformers, the chip area penalty is not as much as compared to the conventional VCOs based on second-order LC tanks. In addition, because there is no extra physical resistive loss introduced into the tank as in the switched-inductor-based VCOs, the high-order LC tank-based VCOs show great potential for the wideband or multiband applications. Moreover, with higher-order resonant tanks, both one-port and two-port oscillation configurations become available. However, compared to the conventional LC-VCO design, as the order of the resonator increases, the design complexity is also increased, stability becomes an issue, and more design parameters (including the inductor ratio, the capacitor ratio, and the coupling between the inductors) need to be considered and optimized simultaneously. As a result, it is desirable to have comprehensive evaluations and comparisons of different circuit topologies and of their design parameters to achieve optimal designs at different frequency bands for specific applications.

In [10], close-form expressions of the oscillation frequencies and the start-up conditions for transformer-based one-port and two-port oscillators are derived by assuming all capacitors are lossless, which unfortunately becomes invalid in wide-tuning-range VCOs for multiband multi-standard applications. In this chapter, to provide more complete understanding and to facilitate better performance evaluation and optimization, the transformer-based one-port and two-port oscillator configurations are systematically analyzed and compared not only with capacitive loss but also for other key design parameters, including tank Q_T, phase noise, and power [14]. It will be shown that, comparatively, one-port oscillators consume less power but need to be stabilized if the oscillation at the higher peak frequency is desired, while two-port oscillators have no stability issue and have superior phase-noise performance for a given output swing but is less efficient in converting the bias current to the tank swing. Based on the analysis, a 2.7–4.3- and 8.4–12.4-GHz dual-mode QVCO for SDR applications is designed and illustrated as a case study [14].
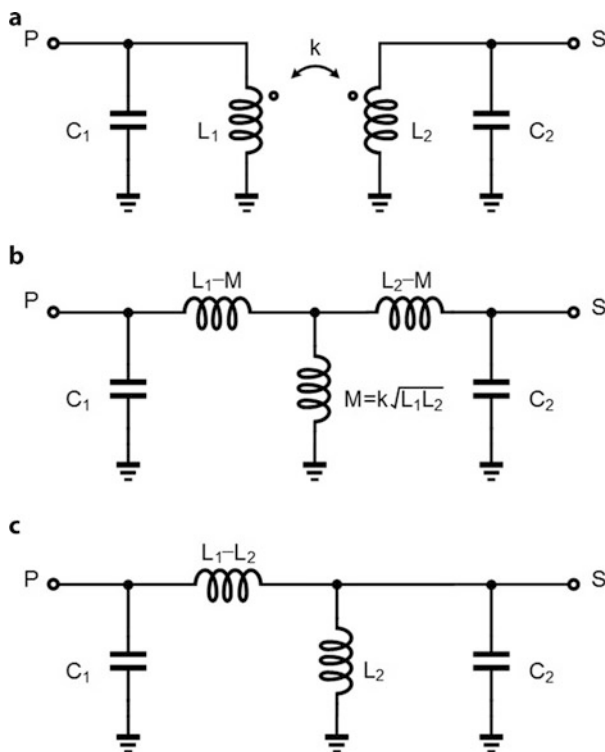
Fig. 6.2 Transformer-based LC tank: (**a**) original network, (**b**) an equivalent network with T-model, and (**c**) a simplified network in a special case when M is equal to L_2

It is worthwhile to notice that a fourth-order LC tank based on multi-tapped inductors is possibly equivalent to a transformer tank. Figure 6.2a shows the transformed-based fourth-order LC tank with lossless inductors and capacitors. By replacing the transformer with its equivalent T-model, the network is redrawn in Fig. 6.2b. Considering a special case when M is equal to L_2 ($L_2/L_1 = k^2$), the network can be further simplified to the one in Fig. 6.2c, which is exactly a fourth-order LC tank based on a multi-tapped inductor without considering the coupling between the inductors. This network is used by many designs [9, 12, 15] and shows very similar properties as the transformer-based LC tank. Consequently, most of the conclusions drawn for the transformer-based VCOs are also applicable for multi-tapped-inductor VCOs.

6.2   Analysis of the Transformer-Based Dual-Mode Oscillators

6.2.1   One-Port Oscillators

Oscillation Frequency

Figure 6.3a shows the general model of the one-port dual-mode oscillator. Resistive components are added in series with the inductors and capacitors to account for the loss of the network, which can be typically compensated for oscillation by employing a negative transconductance cell at either Port 1 or Port 2. The quality factors of inductors and capacitors are defined as $Q_{L1} = \omega L / r_{sL1}$, $Q_{C1} = 1/(\omega C \cdot r_{sC1})$, $Q_{L2} = \omega L / r_{sL2}$, and $Q_{C2} = 1/(\omega C \cdot r_{sC2})$.

To facilitate the calculation of the tank impedance, the transformer is replaced by the equivalent circuit model in Fig. 2.3. The network in Fig. 6.3b can be represented by a simple network in Fig. 6.3c where C_1 is in parallel with the effective inductance $L_1 = L_1 + \Delta L_1$. The expression of ΔL_1 and Δr_{L1} can be derived as below:

$$\Delta L_1 = \frac{k^2 \left(\frac{\omega L_1}{k^2}\right)^2 \left[\left(\frac{\omega_2}{\omega}\right)^2 - 1\right]}{\left[\frac{L_1}{k^2 L_2}(r_{L2} + r_{C2})\right]^2 + \left(\frac{\omega L_1}{k^2}\right)^2 \left[1 - \left(\frac{\omega_2}{\omega}\right)^2\right]^2} L_1 \tag{6.2a}$$

$$\Delta r_{L1} = \frac{\frac{L_1}{k^2 L_2}(r_{L2} + r_{C2})(\omega L_1)^2}{\left[\frac{L_1}{k^2 L_2}(r_{L2} + r_{C2})\right]^2 + \left(\frac{\omega L_1}{k^2}\right)^2 \left[1 - \left(\frac{\omega_2}{\omega}\right)^2\right]^2} \tag{6.2b}$$

where the ω_1 and ω_2 are given by $\omega_1 = 1/\sqrt{L_1 C_1}$ and $\omega_2 = 1/\sqrt{L_2 C_2}$, respectively.

Without loss of generality, let's define $L_1 = mL_2 = mL$ and $C_1 = nC_2 = nC$ and assume that $k > 0$ and $\sqrt{mn} = \omega_2/\omega_1 > 1$ in all the following discussions so that $\omega_1 < \omega_2$. Then Z_{11} can be quickly estimated by assuming a low-loss case (r_{L1}, r_{L2}, r_{C1}, $r_{C2} \to 0$):

$$Z_{11} \approx (1/sC_1) || \left(sL_1'\right) = \frac{j\omega_1^2 L_1 \omega \left[(1 - k^2)\omega^2 - \omega_2^2\right]}{(k^2 - 1)\omega^4 + (\omega_1^2 + \omega_2^2)\omega^2 - \omega_1^2 \omega_2^2} \tag{6.3a}$$

Due to the symmetric property of the network in Fig. 6.3a, Z_{22} can be directly rewritten from Z_{11} as below:

a

b

c
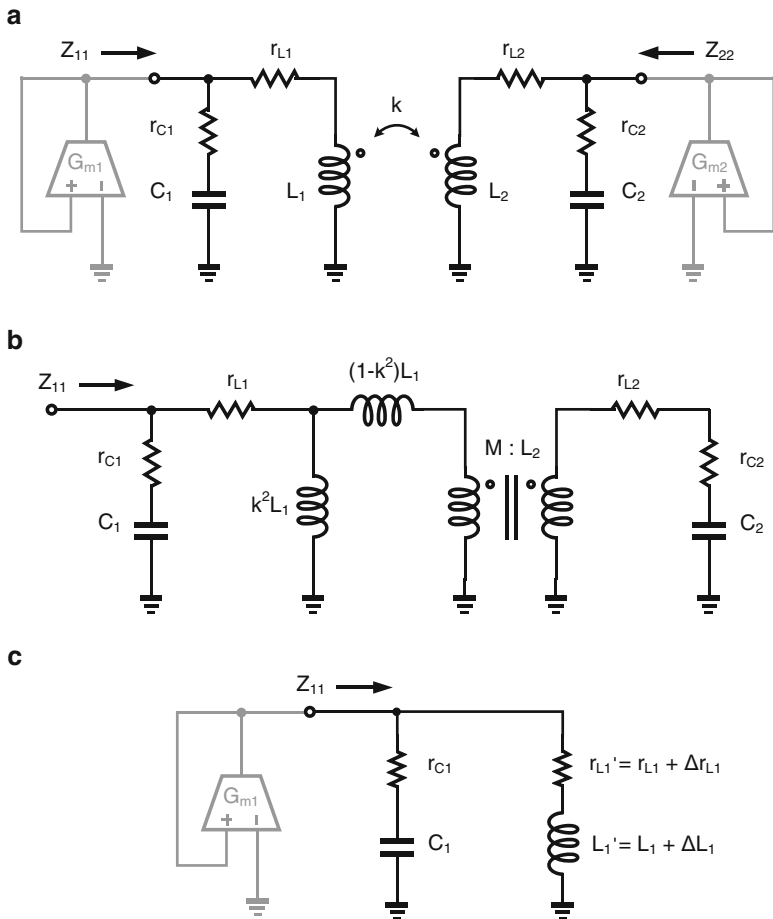
Fig. 6.3 Transformer-based one-port oscillator: (**a**) general model, (**b**) equivalent network for Z_{11} calculation, and (**c**) a simplified network for Z_{11} calculation

$$Z_{22} = \frac{j\omega_2^2 L_2 \omega \left[(1-k^2)\omega^2 - \omega_1^2\right]}{(k^2 - 1)\omega^4 + (\omega_1^2 + \omega_2^2)\omega^2 - \omega_1^2\omega_2^2} \tag{6.3b}$$

From (6.3a) and (6.3b), Z_{11} and Z_{22} have exactly the same two peak frequencies located at

$$\omega_{H/L}^2 = \frac{\omega_1^2 + \omega_2^2 \pm \sqrt{\left(\omega_1^2 - \omega_2^2\right)^2 + 4k^2\omega_1^2\omega_2^2}}{2\left(1 - k^2\right)} \tag{6.4}$$

Besides the peak frequencies, there is one notch frequency $\omega_{1,\text{notch}}$ in Z_{11} and another notch frequency $\omega_{2,\text{notch}}$ in Z_{22}, which are given as below:

$$\omega_{1,\text{notch}} = \frac{\omega_2}{\sqrt{1 - k^2}} \tag{6.5a}$$

$$\omega_{2,\text{notch}} = \frac{\omega_1}{\sqrt{1 - k^2}} \tag{6.5b}$$

Start-Up Condition

Figure 6.4 plots the magnitude and phase responses of Z_{11} and Z_{22} with high-Q inductors and capacitors. The phase shift begins from $90°$ at low frequencies, crosses $0°$ at the first peak frequency ω_L, and returns to $90°$ after either $\omega_{1,\text{notch}}$ in Z_{11} or $\omega_{2,\text{notch}}$ in Z_{22} and crosses $0°$ again at the second peak frequency ω_H.

According to (3.3), the start-up condition of the one-port oscillator shown in Fig. 6.4a is given as below:

$$G_{m11/22} > \frac{1}{\text{real}\{Z_{11/22}(j\omega_{\text{osc}})\}} \tag{6.6a}$$

$$\text{imag}\{Z_{11/22}(j\omega_{\text{osc}})\} = 0 \tag{6.6b}$$

where $\omega_{\text{osc}} = 1/\sqrt{L_1'C_1}$ is equal to either ω_L or ω_H in the lossless case.

Assuming high Q_{L1} and Q_{C1}, the minimum G_m for Port 1 to start-up oscillation can be expressed as

$$G_{m11,\text{min}} = \frac{1}{\left(Q_{L1}'^2 r_{L1}'\right) || \left(Q_{C1}^2 r_{C1}\right)} = \frac{C_1}{L_1 + \Delta L_1}(r_{L1} + \Delta r_{L1} + r_{C1}) \tag{6.7}$$

Substituting ΔL_1 and Δr_{L1} with (6.2a) and (6.2b), $G_{m11,\text{min}}$ can be further expressed as below:

$$G_{m11,\text{min}} = \frac{1}{A_1\omega_{\text{osc}}L_1}\left[\frac{1}{A_1}\frac{1}{Q_{L1}} + \frac{1}{Q_{C1}} + \lambda\left(\frac{1}{A_2}\frac{1}{Q_{L2}} + \frac{1}{Q_{C2}}\right)\right] \tag{6.8a}$$

where $A_1 = \omega_1^2/\omega_{\text{osc}}^2$, $A_2 = \omega_2^2/\omega_{\text{osc}}^2$, $\lambda = (A_2(A_1 - 1))/(A_1(A_2 - 1))$, and the high-order terms such as $1/(Q_{L1}Q_{C1}Q_{C2})$ can be ignored due to high Q_{L1} and Q_{C1}.

Symmetrically, $G_{m22,\text{min}}$ can also be rewritten from (6.8a) as below:
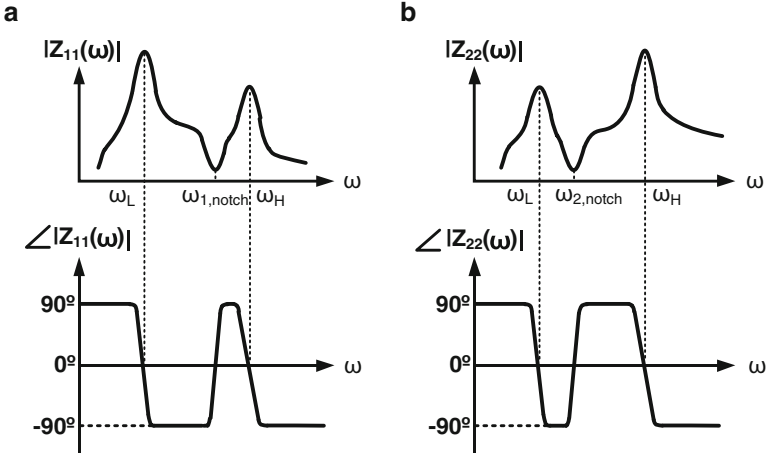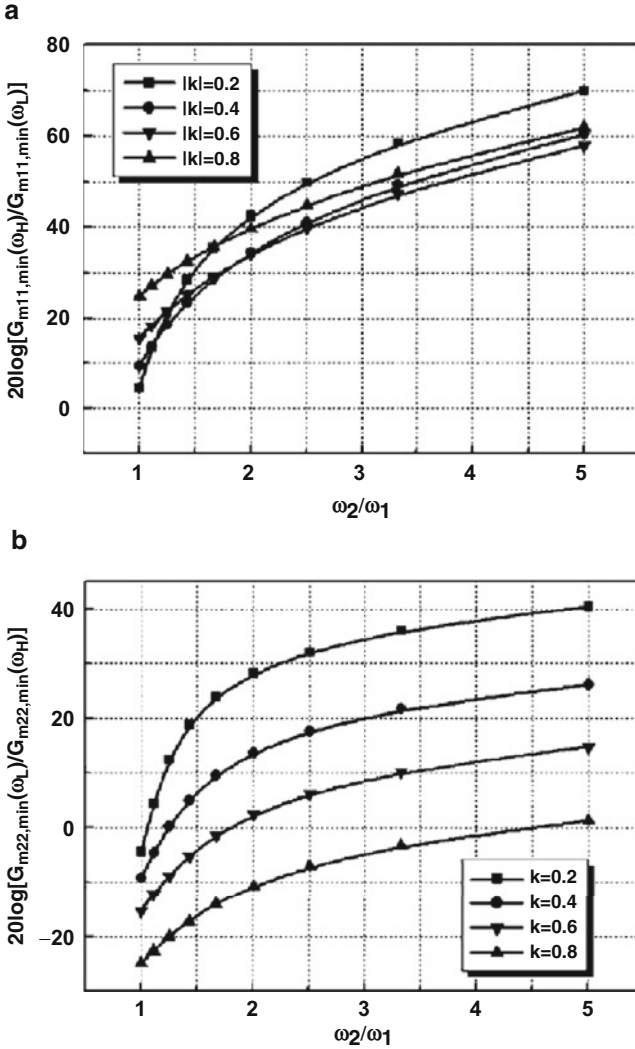
Fig. 6.4 Impedance of a fourth-order LC tank: (**a**) Z_{11} and (**b**) Z_{22}

$$G_{m22,min} = \frac{1}{A_2 \omega_{osc} L_2} \left[\frac{1}{A_2} \frac{1}{Q_{L2}} + \frac{1}{Q_{C2}} + \lambda^{-1} \left(\frac{1}{A_1} \frac{1}{Q_{L1}} + \frac{1}{Q_{C1}} \right) \right] \quad (6.8b)$$

At both the potential oscillation frequencies ω_L and ω_H, the phase shift is $0°$, and thus (6.6b) is satisfied. So the necessary conditions for start-up oscillation at ω_L would become $G_{m11} > G_{m11,min}(\omega_L)$ or $G_{m22} > G_{m22,min}(\omega_L)$, and for start-up oscillation at ω_H would become $G_{m11} > G_{m11,min}(\omega_H)$ or $G_{m22} > G_{m22,min}(\omega_H)$. If G_{m11} or G_{m22} is large enough to satisfy the two conditions, the oscillator can potentially oscillate at either frequency ω_L or ω_H or concurrently oscillate at both frequencies. The final steady-state oscillation depends on detailed configuration of the high-order LC tank and specific form of nonlinearity of the active device.

In either case, to avoid the concurrent oscillation and the potential stability problem that the one-port oscillator could jump from one oscillation frequency to the other in the presence of some disturbances, it is highly desirable to control the oscillator to operate stably at only the wanted frequency. This can be achieved by introducing the notch-peak cancelation concept [11]. From (6.4), (6.5a), and (6.5b), if $|k| \to 0$ or $mn \to \infty$, the notch frequency $\omega_{1,notch}$ and $\omega_{2,notch}$ would approach ω_H and ω_L, respectively, which suggests that the notch in Z_{11} is prone to cancel the high-frequency peak at ω_H, while the notch in Z_{22} is prone to cancel the low-frequency peak at ω_L. As such, in Fig. 6.4a, b, there would be only one dominant peak at $\omega_L(\omega_H)$ in the magnitude response of Z_{11} (Z_{22}) for a practical tank Q_T. The phase shift of Z_{11} (Z_{22}) would stay around but fail to cross $0°$ at $\omega_H(\omega_L)$ as $\omega_{1,notch}(\omega_{2,notch})$ is close by. So in both cases, there is no stability problem since the start-up condition can be satisfied at only one peak frequency.

Figure 6.5a, b plots the transconductance ratio $G_{m11,min}(\omega_H)/G_{m22,min}(\omega_L)$ and $G_{m22,min}(\omega_L)/G_{m22,min}(\omega_H)$ in a log scale, using the component values of $L = 1$ nH, $C = 300$ fF, $Q_{L1} = Q_{L2} = 7$, $Q_{C1} = Q_{C2} = 20$, $m = n = \omega_2/\omega_1$. For $G_{m11,min}(\omega_H)/$

Fig. 6.5 One-port oscillator: (**a**) $G_{m11,min}(\omega_H)/G_{m11,min}(\omega_L)$ and (**b**) $G_{m22,min}(\omega_L)/G_{m22,min}(\omega_H)$ (both in log scale)

$G_{m11,min}(\omega_L)$, with different values of $\sqrt{mn}$ and k, the transconductance ratio is always larger than 1, which implies that if the cross-coupled pair is placed at Port 1 and designed such that $G_{m11,min}(\omega_L) < G_{m11} < G_{m11,min}(\omega_H)$, the VCO will always oscillate at the low peak frequency. Usually, large $G_{m11,min}(\omega_H)/G_{m11,min}(\omega_L)$ is preferred since in some applications that requires low phase noise, and G_{m11} could be quite large to maximize the output amplitude. For $G_{m22,min}(\omega_L)/G_{m22,min}(\omega_H)$, the transconductance ratio is not always larger than 1, so the values of $\sqrt{mn}$ and k need to be properly chosen. For example, when $k = 0.4$, $\sqrt{mn}$ needs to

be larger than 1.5 to provide at least 6-dB margin for designing G_{m22}. On the other hand, when $k = 0.8$, $\sqrt{mn}$ needs to be larger than 4.5 to prevent the VCO from oscillating at ω_L. Consistent with the notch-peak cancelation concept, large $\sqrt{mn}$ and small $|k|$ values are critical for the implementation of dual-band one-port oscillator.

Tank Quality Factor (Q_T)

According to (3.14), the tank quality factor $Q_{T,11}$ for one-port oscillators at the oscillation frequency ω_{osc} can be expressed as

$$Q_{T,11} = \frac{\omega_{osc}}{2}\left|\frac{d\phi_{11}}{d\omega}\right| = \frac{\omega_{osc}L_1'}{r_{L1}' + r_{C1}}\left(1 + \frac{\omega_{osc}}{2L_1'}\frac{dL_1'}{d\omega}|\omega = \omega_{osc}\right) \qquad (6.9)$$

where ϕ_{11} denotes the phase of Z_{11} and again $\omega_{osc} = 1/\sqrt{L_1'C_1}$ is equal to either ω_L or ω_H in the lossless case.

Combining (6.2a) and (6.2b) and ignoring high-order terms such as $1/(Q_{L1}Q_{C1}Q_{C2})$ due to high Q_{L1} and Q_{C1}, $Q_{T,11}$ in (6.9) can be further expressed as

$$Q_{T,11} = \frac{1}{(1+\lambda)A_1}\frac{1}{Q_{L1}} + \frac{1}{1+\lambda}\frac{1}{Q_{C1}} + \frac{1}{(1+\lambda^{-1})A_2}\frac{1}{Q_{L2}} + \frac{1}{1+\lambda^{-1}}\frac{1}{Q_{C2}} \quad (6.10a)$$

Symmetrically, $Q_{T,22}$ can be rewritten from (6.10a) as below:

$$Q_{T,22} = \frac{1}{(1+\lambda^{-1})A_2}\frac{1}{Q_{L2}} + \frac{1}{1+\lambda^{-1}}\frac{1}{Q_{C2}} + \frac{1}{(1+\lambda)A_1}\frac{1}{Q_{L1}} + \frac{1}{1+\lambda}\frac{1}{Q_{C1}} \quad (6.10b)$$

Although the expressions of $Q_{T,11}$ and $Q_{T,22}$ are exactly the same, their values are distinguishable since the desired oscillation frequencies are different (all the parameters, A_1, A_2, and λ, are functions of ω_{osc}).

Phase Noise

Figure 6.6a shows the schematic of the transformer-based one-port dual-mode oscillator, where the negative transconductance cells are implemented with the NMOS cross-coupled pairs. The tail capacitor $C_{T1/T2}$ can be employed for current shaping to increase the current efficiency [16]. The oscillation at either low-band frequency ω_L or high-band frequency ω_H can be selected by controlling the bias current I_{B1} and I_{B2}. At the low-band mode, I_{B1} is enabled while I_{B2} is disabled, and the negative G_m formed by M_1 and M_2 is added at Port 1 to compensate the loss of the tank as shown in Fig. 6.6b. Based on the notch-peak cancelation concept
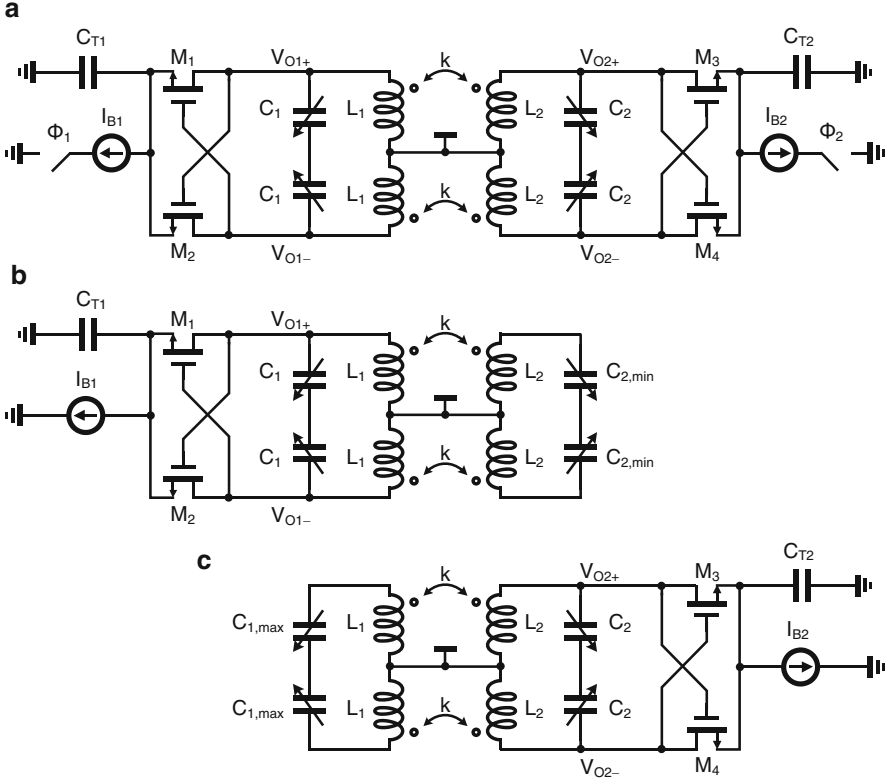
Fig. 6.6 Transformer-based one-port dual-mode oscillator: (**a**) complete schematic, (**b**) simplified schematic for low-band mode, and (**c**) simplified schematic for high-band mode

described earlier, C_2 is minimized to maximize ω_2/ω_1 for stable oscillation at ω_L. At the high-band mode, as shown in Fig. 6.6c, I_{B2} is enabled while I_{B1} is disabled, and the negative G_m formed by M_3 and M_4 is added at Port 2 to compensate the tank loss. Here, C_1 is maximized to maximize ω_2/ω_1 for stable oscillation at ω_H.

Within a narrow bandwidth around ω_{osc}, the characteristic and thus the noise-shaping property of a transformer-based LC tank are the same as a second-order LC tank, since the high-order tank can be equivalently treated as a single capacitor in parallel with an effective inductor L_1 or L_2, like in Fig. 6.3c. Thus, the phase noise of the one-port oscillator can be expressed, directly using (3.28), as

$$\mathcal{L}_{1\text{-port}, 11/22}(\Delta\omega) = 10\log\left[\frac{kT}{C} \cdot \frac{\omega_{osc}}{Q_{T, 11/22}\Delta\omega^2 A_{11/22}^2}(1+\gamma)\right] \qquad (6.11)$$

where C is the differential tank capacitance, which is equal to $C_1/2$ for the low-band mode or $C_2/2$ for the high-band mode. The differential output amplitude $A_{11/22}$ can be derived:

$$A_{11/22} = \beta \frac{2I_{b1/2}}{G_{m11/22,min}(\omega_{L/H})}. \tag{6.12}$$

where the current efficiency β equals to $2/\pi$ or 1 without or with current shaping, respectively.

6.2.2 Two-Port Oscillators

Oscillation Frequency

Figure 6.7a shows the general model of a transformer-based two-port oscillator. Replacing the transformer with the equivalent model as shown in Fig. 6.3b, the transfer impedance $Z_{21} = v_2/i_1$ can be derived as below:

$$Z_{21} = \frac{k\left(R_{C1} + \frac{1}{j\omega C_1}\right)\left(R_{C2} + \frac{1}{j\omega C_2}\right)}{(1 - A_1)R_2\sqrt{\frac{L_1}{L_2}} + (1 - A_2)R_1\sqrt{\frac{L_2}{L_1}} - j\frac{R_1 R_2}{\omega\sqrt{L_1 L_2}} + j\omega\sqrt{L_1 L_2}\left[(1 - A_1)(1 - A_2) - k^2\right]} \tag{6.13}$$

where $R_1 = R_{L1} + R_{C1}$, $R_2 = R_{L2} + R_{C2}$. The result in (6.13) is perfectly symmetrical with respect to the two ports, which indicates $Z_{21} = Z_{12}$, as expected for such a passive network.

Again, with high-Q assumption ($r_{L1}, r_{L2}, r_{C1}, r_{C2} \rightarrow 0$), Z_{21} can be simplified as

$$Z_{21} \approx \frac{jk\sqrt{L_1 L_2}\omega_1^2\omega_2^2\omega}{(1 - k^2)\omega^4 - (\omega_1^2 + \omega_2^2)\omega^2 + \omega_1^2\omega_2^2} \tag{6.14}$$

From (6.14), the two peak frequencies of Z_{21} can also be expressed by (6.4), which implies that the potential oscillation frequencies ω_L and ω_H are exactly the same for both one-port or two-port configurations as long as the inductors and capacitors Qs are sufficiently high.

Start-Up Conditions

For the two-port oscillator as shown in Fig. 6.7a, the current provided by the G_{m21} cell flows into the tank and generates a voltage across the transformer, which is then fed back to the input of the G_{m21} to form a feedback loop. The start-up conditions of the two-port oscillator can be expressed as
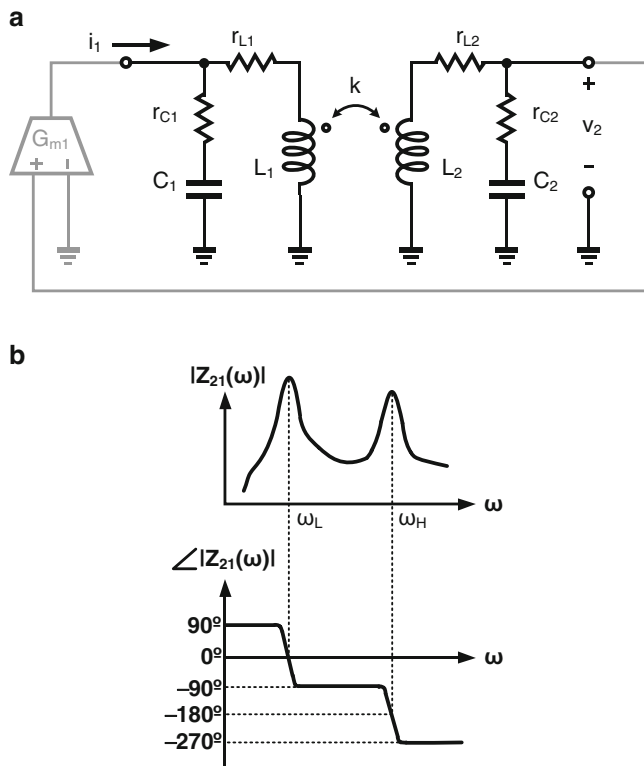
Fig. 6.7 Transformer-based two-port oscillator: (**a**) general model and (**b**) frequency response of Z_{21}

$$G_{m21} \cdot \text{real}\{Z_{21}(j\omega_{osc})\} > 1 \tag{6.15a}$$

$$\text{imag}\{Z_{21}(j\omega_{osc})\} = 0 \tag{6.15b}$$

From the frequency response as shown in Fig. 6.7b, due to the absence of the nonzero frequency notch, the phase shifts of Z_{21} are distinct as $0°$ and $-180°$ at the peak frequencies ω_L and ω_H, respectively. So if G_{m21} is positive, the oscillator will operate at ω_L since real$\{Z_{21}\}$ also needs to be positive. If G_{m21} is negative, the oscillator will operate at ω_H since real$\{Z_{21}\}$ needs to be negative. As a result, the selection of the low-band and high-band modes for the two-port oscillators can be realized simply by controlling the polarity of G_{m21}. As long as the polarity of G_{m21} is fixed, there is only one ω_{osc} that meets the start-up condition. In other words, unlike the one-port counterpart, two-port oscillators are free from the stability problem.

From (6.15a), with high-Q approximation, the minimum G_{m21} to sustain the oscillation can be simplified as below:

$$G_{m21,min} = \frac{(A_2 - 1)\frac{1}{Q_{L1}} + (A_1 - 1)\frac{1}{Q_{L2}} + A_1(A_2 - 1)\frac{1}{Q_{C1}} + A_2(A_1 - 1)\frac{1}{Q_{C2}}}{kA_1A_2\omega_{osc}\sqrt{L_1L_2}} \quad (6.16)$$

Note that when $\omega_{osc} = \omega_L$, $A_2 > A_1 > 1$, and $G_{m21,min}$ is positive. When $\omega_{osc} = \omega_H$, $A_2 < A_1 < 1$, and $G_{m21,min}$ is negative. If all the capacitors are assumed to be lossless, $G_{m21,min}$ can be simplified exactly to the result obtained in [10].

Tank Quality Factor (Q_T)

The tank quality factor $Q_{T,21}$ for the two-port oscillator at the desired oscillation frequency can be derived from $(\omega_{osc}/2)|(d\phi_{21})/(d\omega)|$, where ϕ_{21} denotes the phase of Z_{21}. After simplification with high-Q approximation, it can be derived that expression for $Q_{T,21}$ is exactly the same as (6.10a) or (6.10b), which indicates that both the one-port and the two-port oscillators have approximately the same tank quality factor at the low-band (or the high-band) mode as long as the inductors and capacitors are low losses.

Phase Noise

Figure 6.8a shows the schematic of a transformer-based two-port dual-mode oscillator. When only the current source I_{B1} is enabled as shown in Fig. 6.8b, the associated transistors M_1 and M_2 forms an equivalently positive G_{m12}, and the oscillator operates at the lower-frequency ω_L. When only the current source I_{B2} is enabled as shown in Fig. 6.8c, the associated transistors M_3 and M_4 forms an equivalently negative G_{m12}, and the circuit oscillates at the higher-frequency ω_H.

Making use of the transformer, the gate and drain voltages of M_{1-4} can be independently biased to redistribute the amplitudes and keep the transistors from entering into triode region [17]. If the V_{GS} of $M_{1/2}$ or $M_{3/4}$ voltages are reduced equal to or even lower than the threshold voltage and a large tail capacitor $C_{T1/T2}$ is employed for current shaping, the two-port oscillator would operate in the class-C mode and the phase noise can be expressed as [18]

$$\mathcal{L}_{2\text{-port}}(\Delta\omega) = 10\log\left[\frac{kT}{C}\frac{\omega_{osc}}{Q_{T,21}\Delta\omega^2A_{21}^2}\left(1 + \frac{\gamma}{k_{GD}}\right)\right] \quad (6.17)$$

where C is the differential capacitance at the transistor's gate, which is equal to $C_1/2$ for the low-band mode or $C_2/2$ for the high-band mode, and k_{GD} is the voltage ratio of the gate amplitude to the drain amplitude. According to (6.17), it is desirable to maximize k_{GD} to minimize the phase noise. Therefore, in the low-band mode, the drain of $M_{1/2}$ is connected with L_2 as shown in Fig. 6.8b, and in the high-band mode, the drain of $M_{3/4}$ is connected with L_1 as shown in Fig. 6.8c. With the above analysis, k_{GD} can be well determined as equal to $G_{m22,min}(\omega_L)/G_{m21,min}(\omega_L)$ for the
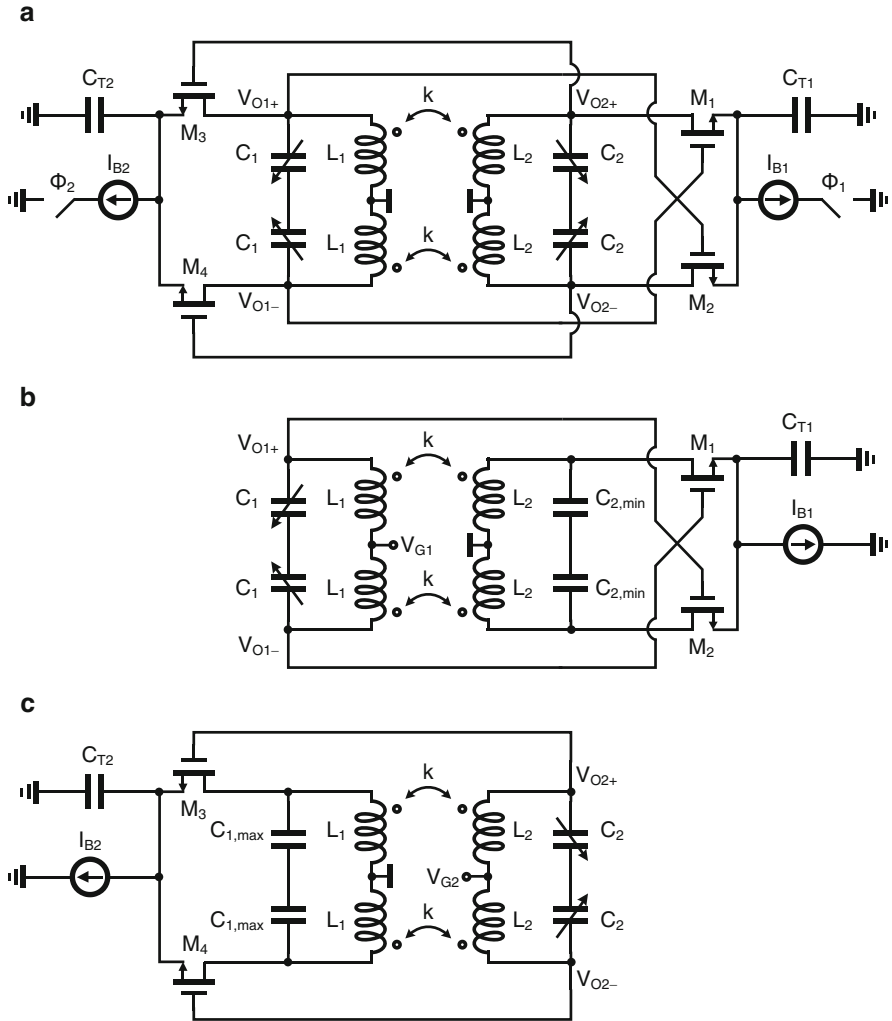
Fig. 6.8 Transformer-based two-port dual-mode oscillator: (**a**) complete schematic, (**b**) simplified schematic for low-band mode, and (**c**) simplified schematic for high-band mode

low-band mode and $G_{m11,min}(\omega_H)/G_{m21,min}(\omega_H)$ for the high-band mode. According to (6.8a), (7.7b), and (6.16), k_{GD} increases with larger ω_2/ω_1 ratio and smaller coupling coefficient k, which implies that the notch-peak cancelation technique not only improves the stability of one-port oscillator but also reduces the phase noise of a two-port oscillator. Finally, the differential output amplitude A_{21} is derived as

$$A_{21} = \beta \frac{2I_{B1/2}}{G_{m21,min}(\omega_{L/H})} \tag{6.18}$$

where the current efficiency β equals to $2/\pi$ or 1 without or with current shaping, respectively.

6.2.3   Comparison of One-Port and Two-Port Oscillators

Oscillation Frequency

Figure 6.9a, b plots and compares the two peak frequencies ω_L and ω_H of nonideal one-port and two-port oscillators for different values of k and different ω_2/ω_1 ratios. The tank inductance and capacitance values are the same as above. From the plots, the calculated result of (6.4) with low-loss assumption is in general a good estimation of the actual peak frequencies of typical one-port and two-port oscillators although special attention needs to be paid to the higher peak frequency when the two coils of the transformer are tightly coupled. Furthermore, the plots also show that ω_L is always smaller than ω_1, while ω_H is always larger than ω_2. It is expected because the effective inductance L_1 is larger than L_1 in the low-frequency band according to (6.2b), while L_2 is smaller than L_2 in the high-frequency band. When $k \rightarrow 0$, the transformer behaves as two independent inductors, and $\omega_{L/H}$ is close to $\omega_{1/2}$. As k increases from 0 to 1, ω_L decreases and eventually reaches a minimum value of $\sqrt{\omega_1^2 \omega_2^2 / (\omega_1^2 + \omega_2^2)}$ when k $=$ 1, which is equal to $0.707\omega_1$ if $\omega_2/\omega_1 = 1$ or equal to ω_1 if $\omega_2/\omega_1 \rightarrow \infty$. At the same time, ω_H also increases and finally approaches to infinity when k is very close to 1.

Start-Up Conditions

For comparison, Fig. 6.10 plots the calculated and simulated required $G_{m,min}$ to oscillate at ω_L and ω_H for both one-port and two-port configurations. It can be clearly seen that in most situations the two-port oscillator requires much larger G_m to sustain oscillation than the one-port oscillator does. For the one-port oscillator, it can be observed from Fig. 6.10a that $G_{m11,min}$ required to oscillate at the lower frequency is relatively constant for different ω_2/ω_1 ratios and k values. On the contrary, Fig. 6.10b shows that $G_{m22,min}$ required to oscillate at the higher-frequency ω_H is reduced with large ω_2/ω_1 ratio and small k. Intuitively, for Z_{11}, as the low-frequency peak is always dominant as compared to the high-frequency peak, there is not too much variation for the peak impedance at ω_L. In contrast, for Z_{22}, because the high-frequency peak is not always dominant as compared to the lower-frequency peak, the requirements for ω_2/ω_1 and k are the same as the stabilizing conditions. $G_{m22,min}$ is not plotted for small ω_2/ω_1 and large k values
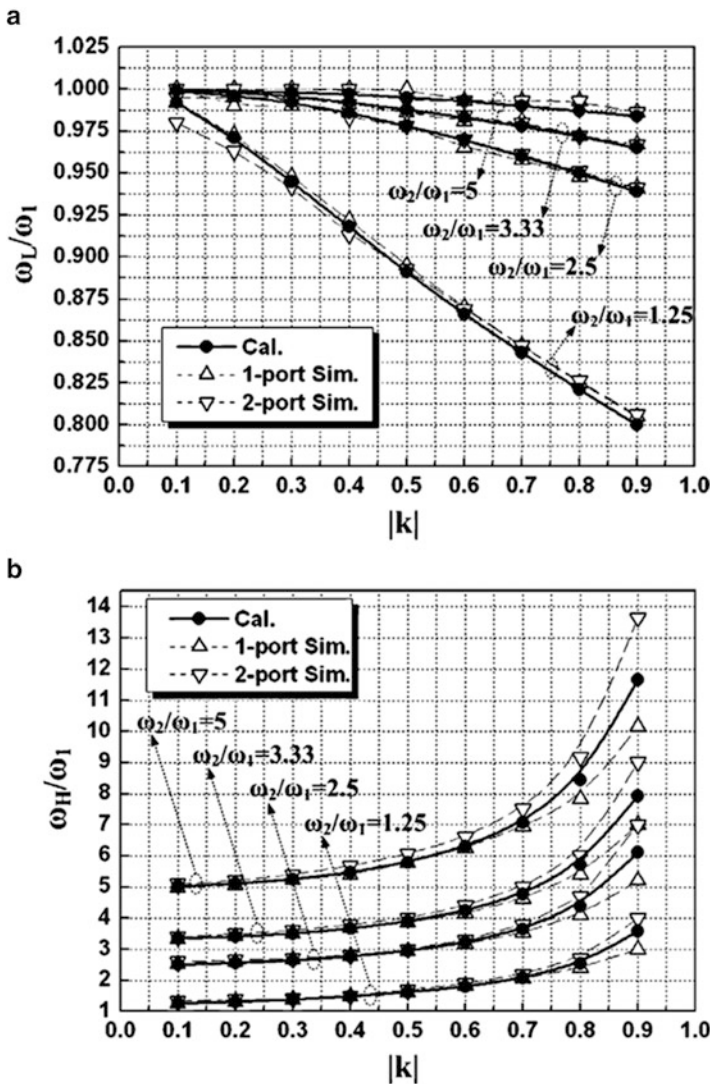
Fig. 6.9 Calculated and simulated oscillation frequencies of transformer-based one-port and two-port oscillators: (**a**) ω_L and (**b**) ω_H

because the one-port oscillator could hardly oscillate at the high-frequency peak under these conditions. For the two-port oscillator, large k and small ω_2/ω_1 ratio result in reduced $G_{m21,min}$ at the low-frequency peak, while, for the high-frequency peak, small k and small ω_2/ω_1 ratio are required to facilitate the oscillation start-up.
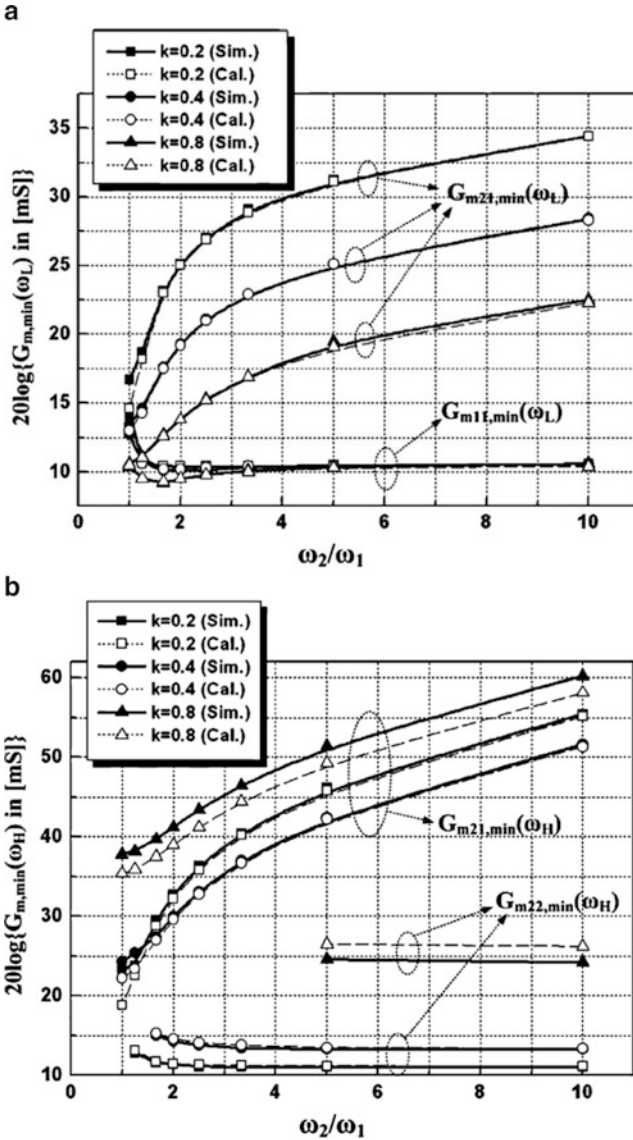
Fig. 6.10 Calculated and simulated start-up conditions of transformer-based one-port and two-port oscillators: (**a**) required $G_{m,min}$ at ω_L and (**b**) required $G_{m,min}$ at ω_H

Tank Quality Factor (Q_T)

Figure 6.11 plots the calculated and simulated one-port and two-port tank quality factors at the two peak frequencies with the same parameters used previously and with the inductors Qs and capacitors Qs being set to 7 and 20, respectively. The
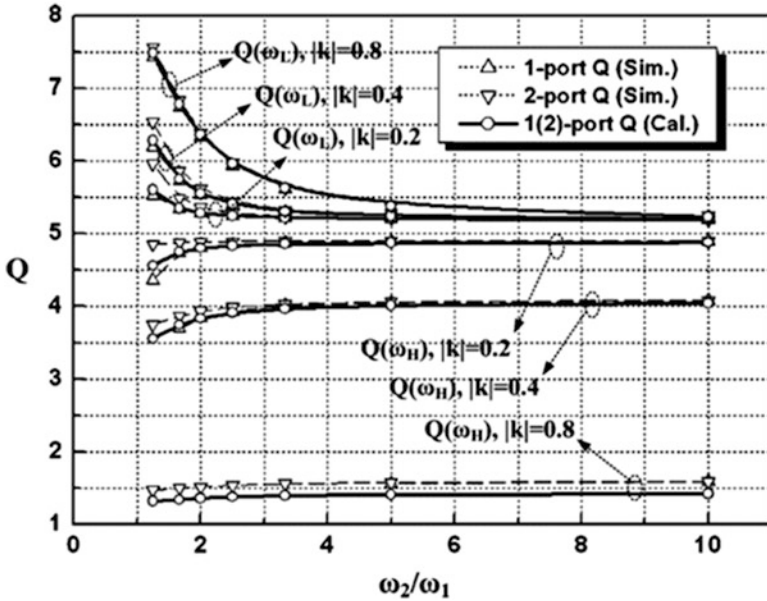
Fig. 6.11 Calculated and simulated tank quality factor of transformer-based one-port and two-port oscillators at ω_L and ω_H

discrepancy between the calculated and simulated tank quality factors for the two oscillators is decreased and finally approaches to zero as the inductor and capacitor Qs are increased, which validates the derivation. Moreover, Fig. 6.11 shows that, in general, compared to a second-order LC tank with the same inductor Q and capacitor Q, the transformer-based fourth-order LC tank has a better Q_T at the lower-frequency peak but a worse Q_T at the higher-frequency peak. This can be understood from Fig. 6.3c and (6.2a) and (6.2b). At the lower-frequency ω_L, the effective inductance L_1 is larger than L_1. Although the effective inductor loss r_{L1} also increases, the effective inductor Q_{L1} still increases, which results in an improved Q_T. At the higher-frequency ω_H, the effective inductance L_2 becomes smaller than L_2, while the effective inductor loss r_{L2} still increases. As a consequence, the effective inductor Q_{L2} inevitably decreases, which corresponds to a degraded Q_T.

From Fig. 6.11, it can be further concluded that the improvement or degradation of the tank Q_T at ω_L or ω_H becomes more effective with a smaller ω_2/ω_1 ratio and/or a larger k. This can also be estimated from (6.10a) and (6.10b). Assuming that $Q_{L1} = Q_{L2} = Q_L$, $Q_{C1} = Q_{C2} = Q_C$, and $m = n = \omega_2/\omega_1$, the equations can be rewritten as below:

$$\frac{1}{Q_T(\omega_L)} = \frac{(n^2 A_1^2 - 1) - k^2}{(n^2 A_1^2 - 1) + k^2} \frac{1}{Q_L} + \frac{1}{Q_C} \tag{6.19a}$$

$$\frac{1}{Q_T(\omega_H)} = \frac{(1 - A_2^2/n^2) + k^2}{(1 - A_2^2/n^2) - k^2} \frac{1}{Q_L} + \frac{1}{Q_C} \tag{6.19b}$$

From (6.19a) and (6.19b), it can be directly seen that when n is decreased or k is increased, the $Q_T(\omega_L)$ is improved, while the $Q_T(\omega_H)$ is degraded because A_1 at ω_L and A_2 at ω_H are weakly dependent on n and k when k is not close to 1. In the limiting case when $\omega_2/\omega_1 = 1$ and k = 1, ω_L is reduced to $0.707\omega_1$, and A_1 is 2. If the capacitor loss is ignored, the maximum $Q_T(\omega_L)$ is 2. On the other hand, under the same condition, as ω_H is close to infinity, A_2 is close to zero, which indicates that the $Q_T(\omega_H)$ would be infinitely small.

Phase Noise

As shown in Figs. 6.9 and 6.11, the oscillation frequencies and the tank quality factors of one-port and two-port oscillators are approximately the same as long as the inductors and capacitors are of low loss. Moreover, according to (6.11) and (6.17), it is obvious that two-port oscillators can achieve lower phase noise than one-port oscillators assuming that they have the same output amplitude ($A_{11/22} = A_{21}$) and that the transistors M_{1-4} are always kept in the saturation region to reduce their phase-noise contributions by properly controlling the ratio of the gate and drain voltages. However, the two-port oscillators require a larger current to sustain the same output amplitude as shown in Fig. 6.10. In other words, the phase-noise improvement for the two-port oscillators is at the cost of large power consumptions.

Assuming that the capacitor at the tail node $C_{T1/2}$ is much smaller than $C_{1/2}$ and using the passive component values in previous discussion together with m = n = 4 and k = 0.6, the output amplitude and phase-noise values are simulated versus different tail currents I_{B1} and capacitances C_{T1} and plotted in Fig. 6.12a when the one-port oscillator operates at ω_L. The transistors size of 50 μm/0.12 μm in a 0.13-μm CMOS process (with V_{th} being around 0.4 V) are used for M_{1-2} to make the operation close to hard switching. The calculated phase noise and output amplitude based on (6.11) and (6.12) are also plotted for comparison with no C_{t1} and with very large C_{t1}.

In Fig. 6.12a, when I_{B1} is small and A_{11} is not larger than V_{th} so that M_{1-2} do not enter into triode region, both the output amplitude and the phase noise are linearly improved with the increase of I_{B1}, and the simulated results can be well predicted by the calculated ones. Since the tail capacitor can help improve the current efficiency, the output amplitude and thus the phase noise are improved with larger tail capacitance even when I_{B1} is kept the same [16]. However, when I_{B1} and A_{11} are further increased, $M_{1/2}$ would enter the triode region, and the output amplitude begins to deviate from the predicted linear curve because the tank is loaded by the
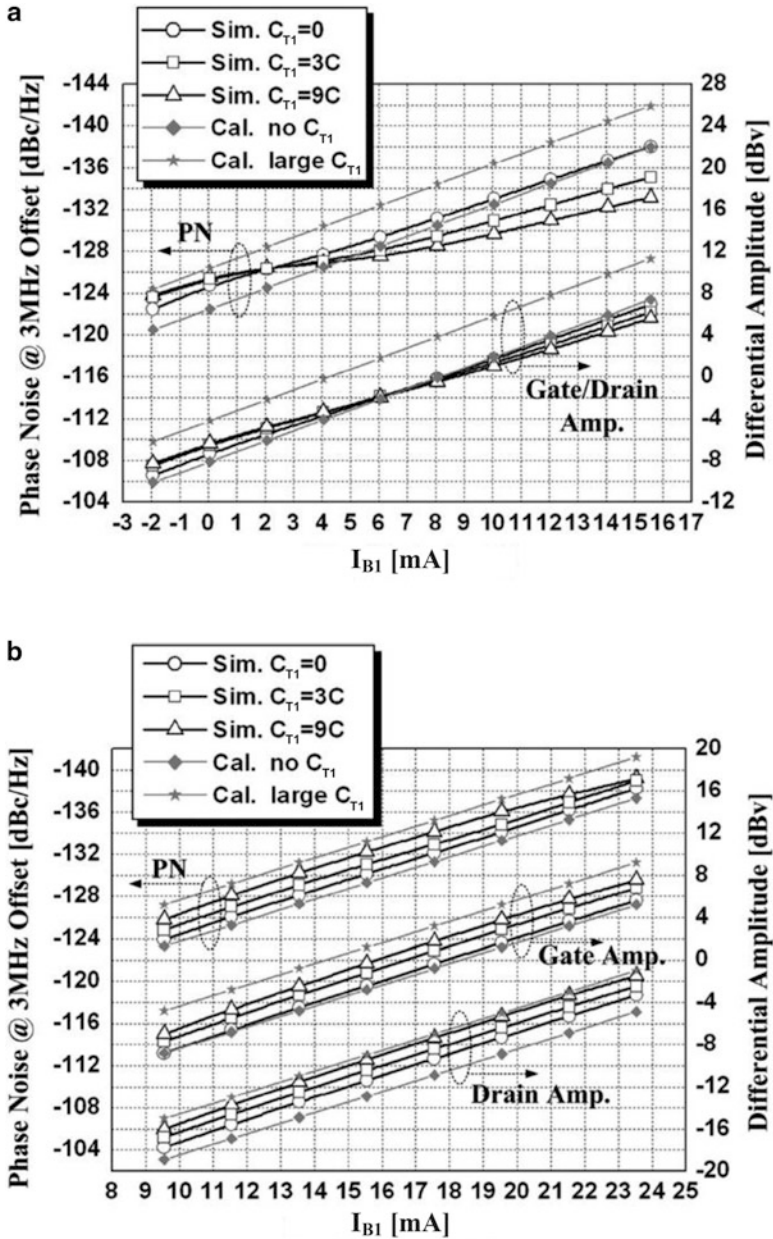
Fig. 6.12 Calculated and simulated phase noise and amplitude of (**a**) the transformer-based one-port oscillator and (**b**) the transformer-based two-port oscillator

tail capacitor with the finite turn-on resistance of the $M_{1/2}$ in triode region as discussed in Chap. 3. Furthermore, the degradation of the tank Q_T also causes the degradation of the phase noise.

Using the same parameters as above, Fig. 6.12b plots the calculated and simulated amplitudes and phase noise with different I_{B1} and C_{T1} when the two-port oscillator operates at ω_L. Compared to the one-port oscillator, the I_{B1} of two-port oscillator needs to be around three times larger in order to achieve the same output amplitude. However, because the drain amplitude is much smaller than the gate amplitude and the gate voltage can be biased to be much lower than the supply, $M_{1/2}$ can be kept away from the triode region even when the differential output amplitude is as large as 2 V (V_{DD} is 1.2 V). Even if the negative transconductance $M_{1/2}$ in one-port oscillators are also biased in the class-C mode using AC-coupled capacitors as shown in Fig. 3.22, the maximum output amplitude that keeps $M_{1/2}$ in the saturation region still cannot be as large as that in the two-port oscillator since the ratio k_{GD} between the gate and drain amplitude cannot exceed unity in one-port oscillators. As such, the two-port oscillator exhibits better amplitude and better phase-noise "linearity" with the increase of I_{B1}, which also agrees well with the ideal calculated results. It follows that, with sufficiently large bias current, the two-port oscillator is able to achieve lower phase noise compared to the one-port oscillator.

6.3 Case Study of a Dual-Mode QVCO for SDR Frequency Synthesizer

6.3.1 Circuit Implementation

Making use of the analytical results in Sect. 6.2, a dual-mode transformer-based QVCO is designed for a wideband SDR frequency synthesizer as described in [19]. The design target is to generate IQ LO signals to support all wireless standards from 47 MHz to 10 GHz (utilizing direct-conversion transceiver architecture) and from 57 to 66 GHz (employing dual-conversion transceiver architecture). With dual-band operations, the transformer-based QVCO covers the fundamental frequency bands from 3 to 4.2 GHz as well as from 8.4 to 12 GHz. After divided by 2, the high band can cover a frequency range from 4.2 to 6 GHz with IQ signals. Consequently, together with the low-band frequency, a continuous tuning range from 3 to 6 GHz can be achieved. With a cascade of /2 dividers, IQ LO signals from 47 MHz to 3 GHz can be further derived. Moreover, to support all the 14 OFDM UWB frequency bands from 3 to 10 GHz, the 8.448-GHz IQ signals covered by the high-band mode is used to generate the required IQ LO signals at frequencies 4224, 2112, 1056, 528, and 264 MHz for single-sideband (SSB) mixings [20] by reusing the divider chain in the PLL.
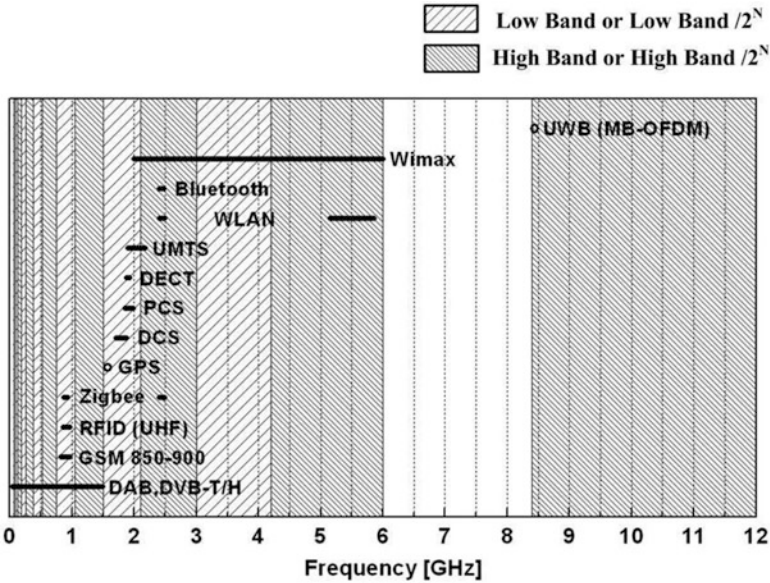
Fig. 6.13 Frequency plan for the transformer-based dual-mode QVCO

As discussed in Sect. 6.2.3, compared to a second-order LC tank, the Q_T of a transformer-based LC tank is improved at the lower-frequency peak but degraded at the higher-frequency peak. It is therefore more desirable to make the VCO operate at the low-frequency band when the phase-noise requirement is stringent. So the corresponding frequency plan is made, in which the frequency of interest can be generated at either of the two frequency bands or at a subharmonic of these frequency bands by dividing them down by 2^N as shown in Fig. 6.13. Here, the frequency bands covering all the standards with the most stringent phase-noise requirement (such as GSM requiring < -162 dBc/Hz at 20-MHz offset and passive UHF RFID requiring -144 dBc/Hz at 3.6-MHz offset) are all assigned into the low-frequency band, while the frequency bands for the other standards with more relaxed phase-noise requirement are assigned in the high-frequency band.

Since the tank Q_T is dominated by the inductor Q at the operating frequency range, Q_{L1} and Q_{L2} should be optimized at the low-band and high-band frequencies, respectively. Assuming $Q_{L1} = 14$, $=Q_{L2} = 7$ at the low-band mode, while $Q_{L1} = 7$, $=Q_{L2} = 14$ at the high-band mode, which are the typical values of the achievable inductor Q using a 2-μm-thick top metal layer, all the design parameters (including the required bias currents to obtain differential output amplitude of 2 V, the tank quality factors, the phase noise of both one-port and two-port oscillators, as well as stability conditions of the one-port oscillator) can be quickly and accurately estimated by using the equations in Sect. 6.2, which are plotted in Fig. 6.14. Since the desired frequency ratio ω_H/ω_L around 2.8 is not achievable when k becomes larger than 0.77, the curves are only plotted up to $k = 0.7$.
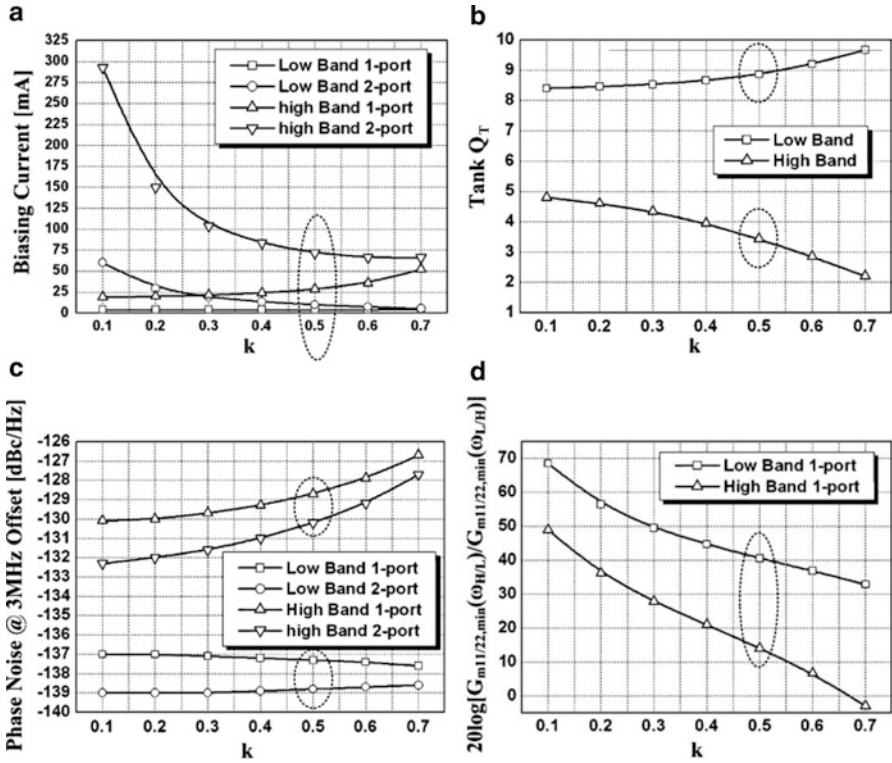
Fig. 6.14 Estimated (**a**) required bias current for maximum output swing, (**b**) tank Q_T, (**c**) phase noise at 3 MHz frequency offset, and (**d**) stability margin of one-port oscillator at different k

When plotting Fig. 6.14, L_1 and L_2 are varied to make the dual-mode VCO oscillate at 3 and 8.4 GHz for the worst scenario when all the switching capacitors are turned on. It is also assumed that the tail capacitance is negligibly small for the one-port oscillator and is large enough for the two-port oscillator to achieve the lowest achievable phase noise and the maximum output swing. As shown in Fig. 6.14a, when k is increased, the required bias current is reduced for the two-port oscillator but increased for the one-port oscillator. As k is increased to around 0.6, the bias current of two-port oscillator can be comparable to that of the one-port oscillator for the low-band oscillation. On the other hand, to sustain a maximum swing for the high-band oscillation, the two-port oscillator requires large current above 60 mA while the one-port oscillator required around 25 mA when k is less than 0.5. In Fig. 6.14b, the low-band tank Q_T is improved from 8.4 to 9.7, while the high-band tank Q_T is degraded from 4.8 to 2.2 when k is increased from 0.1 to 0.7. In the high-band mode, the loss from SCA (Q_{C2}) also becomes significant, and Q_{C2} can be improved by increasing the switch size in SCA at the expense of smaller tuning range. In Fig. 6.14c, for the one-port oscillator, when k is increased, the low-band phase noise is improved because the low-band Q_T is improved, but the

high-band phase noise is degraded because the high-band Q_T gets smaller. On the other hand, for the two-port oscillator, when k is increased, because the gate and source voltage ratio k_{GD} is decreased for both the low band and the high band, the low-band phase noise actually degrades slightly although the Q_T is improved, while the high-band phase noise degrades significantly. Figure 6.14d illustrates that the one-port oscillator can operate stably at the low band for any k value but would fail to operate at the high band when k is close to 0.7.

In this design, to meet the most stringent phase-noise requirement with a bias current of less than 10 mA, the two-port configuration is chosen for the low-band operation, while the one-port configuration is used for the high-band operation to greatly save the power consumption. To balance the phase noise and power consumption as well as guarantee the stability condition in high-band mode, k is optimally selected to be around 0.5.

Figure 6.15 shows the schematic of the transformer-based dual-band QVCO. The operation can be divided into two modes. In the low-band mode, the current sources I_{core1} and I_{tune1} are turned on while I_{core2} and I_{tune2} are turned off, for which the VCO operates as a two-port oscillator. As M_1 and M_2 are connected to make the G_{m21} positive, the VCO oscillates at the low-frequency band. In the high-band mode, the current sources I_{core1} and I_{tune1} are turned off while I_{core2} and I_{tune2} are turned on, and the VCO operates at the high-frequency band as a one-port oscillator. According to the frequency plan, around 45 % tuning range is required for either the low band or the high band to cover the PVT variations with enough margins. So 5-bit binary-weighted SCAs are employed to achieve the coarse tuning for each band in both modes, while the fine frequency tuning is realized by varying the coupling current [21] instead of using varactors to reduce AM-to-PM noise conversion and to prevent the tank Q_T from being further degraded by varactors. To control the tuning current, a voltage-to-current converter with tunable transconductance is implemented to convert the control voltage from the loop filter to the tuning current to make effective K_{VCO} tunable for dynamic control of the loop bandwidth. 5-bit binary-weighted SCAs are placed at both the first and the second coils of the transformer to realize the coarse tuning and to reduce the required tuning range of $I_{tune1/2}$. In the low-band mode, the SCAs at Port 2 are turned off in the first mode, while in the high-band mode, the SCAs at Port 1 are turned on in the second mode to ensure a large frequency ratio ω_2/ω_1 is always achieved, which helps not only minimize the phase noise of the two-port oscillator in the first mode but also stabilize the one-port oscillator in the second high-band mode. To eliminate any potential bimodal oscillations, the cascode transistors M_{5-6} are added to create enough delay in the coupling paths.

To improve the IQ matching, the current sources of "I" and "Q" parts are connected correspondingly as shown in the dotted lines in Fig. 6.3 [22]. In order to measure the IQ sideband-rejection (SBR) ratio directly, the QVCO's IQ outputs are connected to an on-chip SSB mixer. A low-frequency divider is also embedded to generate the second low-frequency IQ input signals for the SSB mixer from an external low-frequency input signal.
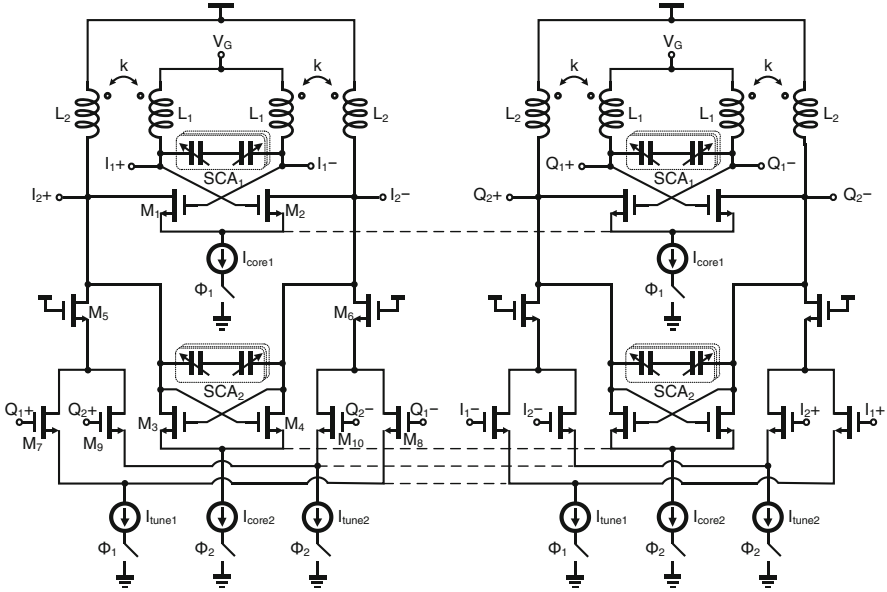
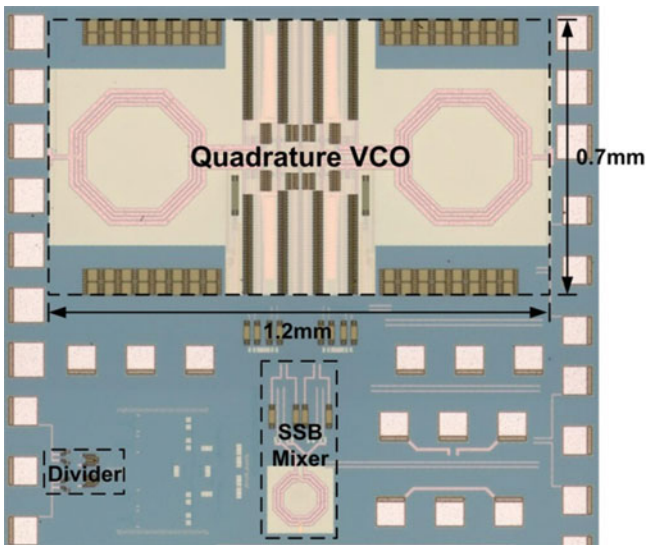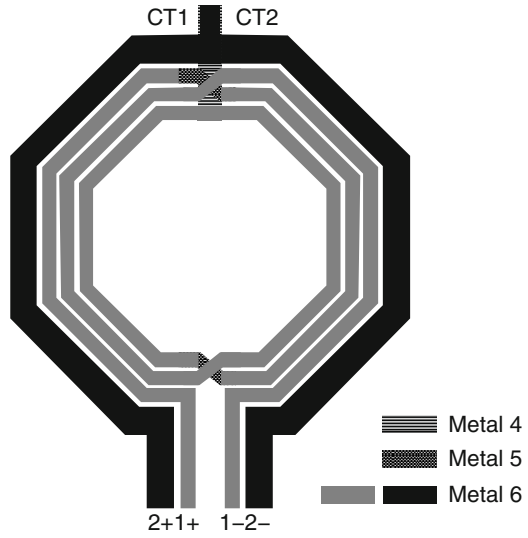**Fig. 6.15** Schematic of the transformer-based dual-mode QVCO

Figure 6.16a shows the layout of the transformer designed for the dual-mode QVCO. To achieve a desired k value of 0.5, the 3-turn primary coil is placed inside the 1-turn secondary coil with a space of 3 μm. The widths of the primary and secondary coils are optimized to be 9 and 12 μm to locate the peak Q_{L1} and peak Q_{L2} at the low band and high band, respectively. From EM simulations, $L_1 = 2.6$ nH, $L_2 = 0.43$ nH, $Q_{L1} \approx 13$ at the low-frequency band, and $Q_{L2} \approx 14$ at the high-frequency band. Simulation also verifies that at the worst case when all the switched capacitors at the secondary coil are turned on, the high-frequency peak impedance $\left|Z_{22}(\omega_H)\right|$ is more than 10 dB larger than the low-frequency peak impedance $\left|Z_{22}(\omega_L)\right|$. In the QVCO layout, all the transistors and SCAs for the high-frequency band are placed closer to the transformer than those for the low-frequency band to maximize the ratio C_1/C_2 and to balance the power consumption of the two modes.

6.3.2 Experimental Results

The dual-band QVCO is fabricated in a 0.13-μm CMOS process. Figure 6.17 shows the chip micrograph together with the on-chip SSB mixer and divider for the SBR measurement, where the QVCO core occupies an area of 0.84 mm².

The dual-mode QVCO draws a current from 12 to 20 mA from a 1.2-V supply voltage in both modes. Figure 6.18 shows the measured frequency curves of the QVCO in the two modes as functions of the tuning current. The QVCO is

Fig. 6.16 Layout of the transformer

Fig. 6.17 Chip micrograph of the transformer-based dual-mode QVCO

continuously tunable from 2.7 to 4.3 GHz in the low-band mode and from 8.4 to 12.4 GHz in the high-band mode, corresponding to tuning ranges of 45.7 % and 38.5 %, respectively. As a result, the experimental dual-mode QVCO can successfully meet the target frequency requirement for the SDR applications. During the measurement, it is found that the QVCO could oscillate at the lower-frequency peak in the second mode when the SCAs at the Port 1 are all intentionally turned off,
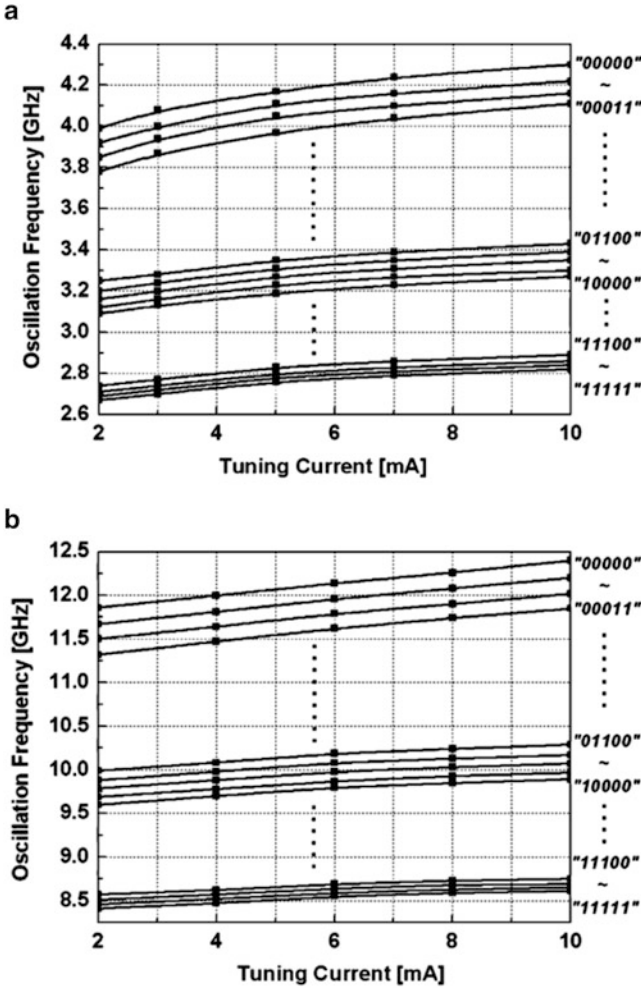
Fig. 6.18 Measured frequency tuning curves for the QVCO in (**a**) the low-band mode and (**b**) the high-band mode

while the SCAs at Port 2 are all on, which further verifies that keeping a large capacitor ratio C_1/C_2 is important for the stability of the one-port oscillation.

Figure 6.19 shows the measured phase-noise profiles at 3.6 and 10.4 GHz with the QVCO drawing 16 mA, from which the phase-noise values of -135.9 and -119 dBc/Hz at 3-MHz offset are achieved, respectively. With proper frequency division as required, in the low-band mode, the measured phase noise exceeds the requirement of GSM standard. In the high-band mode, the measured phase noise meets all the requirements of the target standards including WLAN and UWB standards.
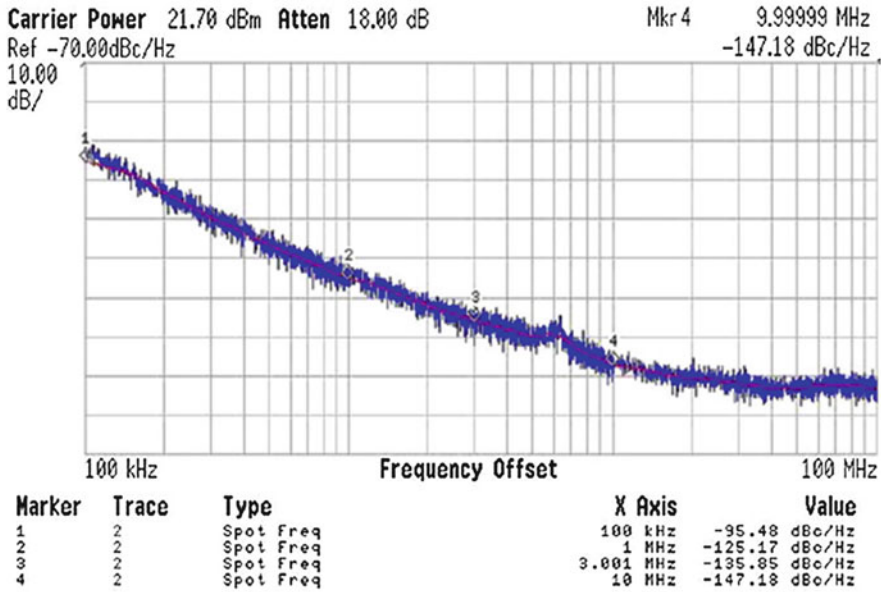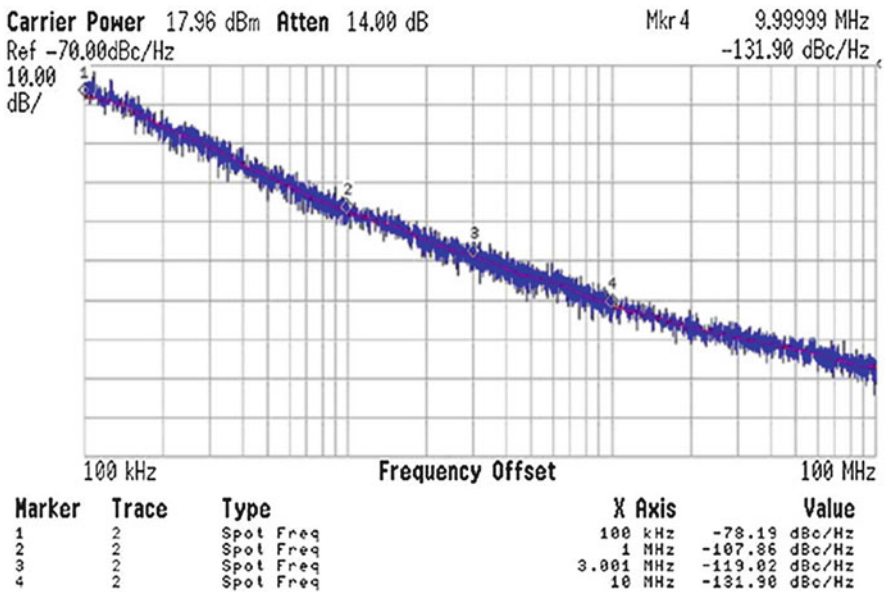
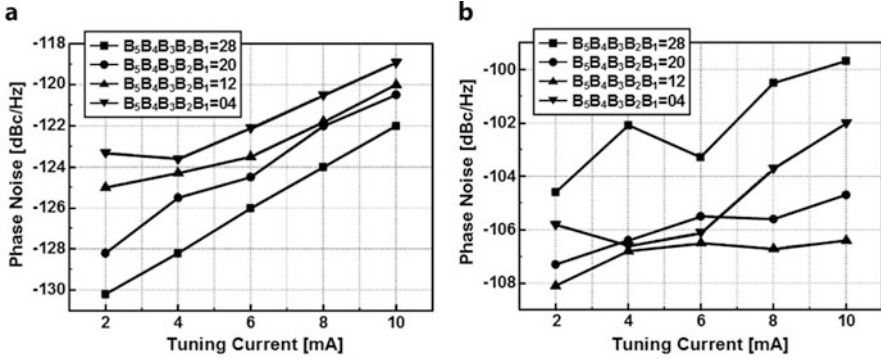**Fig. 6.19** Measured QVCO phase noise as a function of offset frequency at (**a**) 3.6 GHz (the low-frequency band) and (**b**) 10.4 GHz (the high-frequency band)

Fig. 6.20 Measured phase noise at 1-MHz offset as functions of tuning current for different SCA settings: (**a**) in the low-band mode and (**b**) in the high-band mode

Figure 6.20 shows the measured phase noises as functions of the tuning current with different SCA settings. When the tuning current varies from 2 to 10 mA, the measured phase noise at 1-MHz offset is between -118.9 and -130.2 dBc/Hz for the lower-band mode and between -99.7 and -108.1 dBc/Hz for the high-band mode. As expected, the phase noise is degraded with increased tuning current. From the frequency tuning curves plotted in Fig. 6.18, a tuning current between 2 and 6 mA is sufficient for covering the required frequency bands with 5-bit binary-weighted SCAs. As a result, at 1-MHz frequency offset, the low-band phase noise can be reduced to between -122.1 and -130.2 dBc/Hz, and the high-band phase noise can be reduced to between -102.1 and -108.1 dBc/Hz.

Figure 6.21 shows the measured spectrum at the SSB mixer's output. Assuming that the mismatch of the QVCO is dominant, SBRs of 37 and 41 dB are achieved for the low-band and high-band modes, corresponding to IQ phase errors of $1.6°$ and $1°$, respectively.

Table 6.1 summarizes the performance of the designed dual-band QVCO compared with the state-of-the-art dual-mode or wideband VCOs.

a
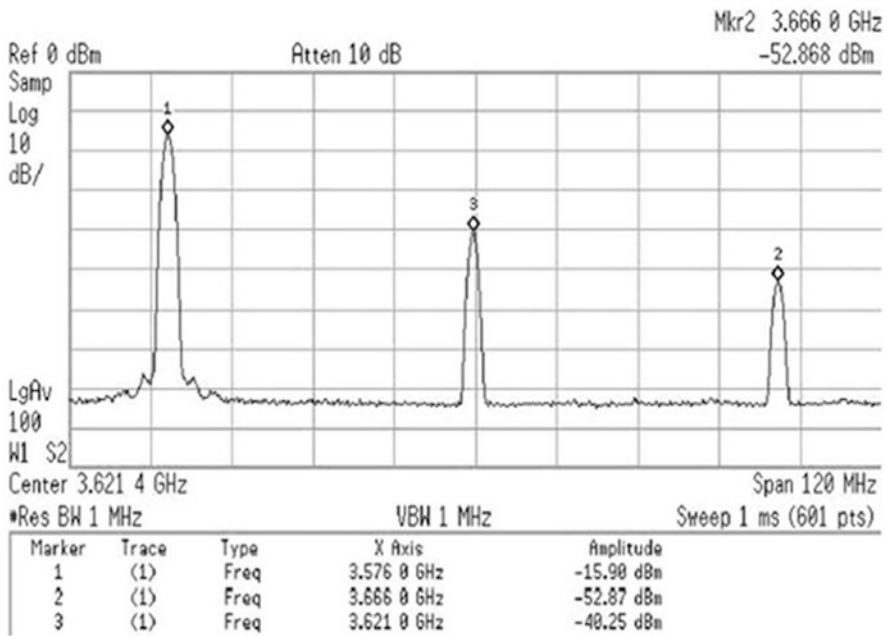
b
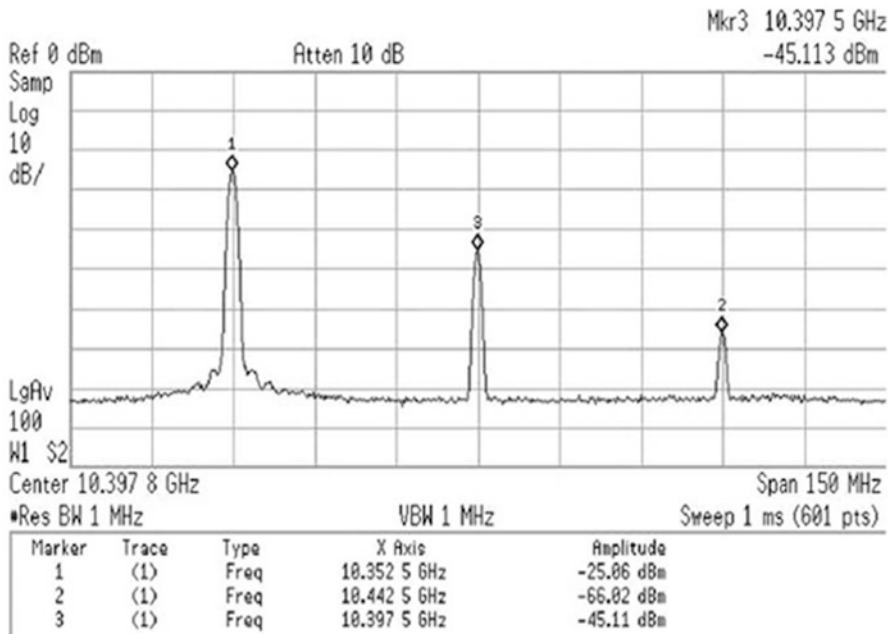
Fig. 6.21 Measured spectrum at the SSB mixer's output at (**a**) 3.6 GHz in the low-frequency band and (**b**) 10.4 GHz in the high-frequency band

Table 6.1 Comparison of dual-mode differential and quadrature VCOs

Reference	Technology	First band (GHz)	Second band (GHz)	Power (mW)	PN @ 3 MHz (dBc/Hz)	FOM (dBc/Hz)	FOM$_T$ (dBc/Hz)	Area (mm²)
[3]	0.18-μm Bi-CMOS	6.3–6.6 (5 %)	9.45–9.9 (5 %)	19.4[a]	−115.5/−113.5[b]	177/178	177/178	1.65[c]
[5]	0.25-μm CMOS	0.98–1.16 (17 %)	1.60–2.01 (23 %)	11/14[d]	−138/−132	178/177	190/189	0.25
[8]	0.13-μm CMOS	3.3–8.4 (87 %)		7–15[d]	−126.5-−131.5[b]	181–185	200–204	0.1
[9]	0.5-μm Bi-CMOS	0.79–0.85 (7 %)	1.75–1.87 (7 %)	15[d]	−145.5/−143.5[b]	181/188	184/191	3.61[c]
[10]	0.13-μm CMOS	3.4–7 (69 %)		1–8[d]	−110.5-−128.5[b]	167–192	184–209	0.65[c]
[11]	0.18-μm CMOS	3.27–5.02 (42 %)	9.5–11.4 (18 %)	6/10[a]	−125.5/−121.5[b]	181/182	197/198	0.88
[12]	90-nm CMOS	3.1–3.9 (23 %)	8.8–11.2 (24 %)	2.2–4.2/6.7–10[d]	−123.6/−118.6[e]	181	194	0.034
[23]	0.18-μm CMOS	2.4 (0 %)	4.7 (0 %)	3.4[d]	−131.5/−132.5[b]	185/192	–	–
[24]	0.18-μm CMOS	0.82–0.87 (5 %)	1.64–1.81 (10 %)	16[d]	−139/−137[f]	176/181	180/184	0.90
[25]	90-nm CMOS	8.1–15.4 (62 %)		7.7[d]	−115.5[b]	179	194	–
This work	0.13-μm CMOS	2.7–4.3 (46 %)	8.4–12.4 (38 %)	14–24[a]	−136/−119	185/177	203/195	0.84

[a]I/Q outputs
[b]Normalized from frequency offset at 1 MHz
[c]Area include pads
[d]Differential outputs
[e]Normalized from frequency offset at 2.5 MHz
[f]Normalized from frequency offset at 0.6 MHz

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Chapter 7
Magnetically-Tuned Multimode CMOS VCO

7.1 Introduction

As the operation frequency of VCOs increases, it becomes more and more difficult to achieve large tuning range while still maintaining low phase noise and low power. At mm-Wave frequencies, since the varactor Q is dominantly low, increasing the frequency tuning range by increasing the varactor size would inevitably degrade the tank impedance. To guarantee the oscillation, the size of the negative-g_m cell in the VCO would need to be increased, which in turn would increase the parasitic capacitance, degrade the frequency tuning range, and limit the maximum oscillation frequency. So it is necessary to explore other frequency tuning methods.

At mm-Wave frequencies, the existing tuning-range enhancement techniques introduced in the previous chapters become less effective. For the switch-inductor technique [1] discussed in Sect. 3.6, since the tank inductance is quite small, increasing the switch size to improve the tank Q is ineffective because the large parasitic capacitance would prevent the switch from being turned off. For the coarse frequency tuning using high-order LC resonant tanks with transformers or multi-tapped inductors [2–4], the tuning range is still limited when applied at mm-Wave frequency since only two or three coarse tuning bands are created.

In [5], switched-coupled inductors are used for coarse frequency tuning. Because both the effective turn-on resistance and turn-off parasitic capacitance of the switches are significantly reduced due to the impedance transformation with small coupling coefficient, the tank Q degradation is much less than that of the switched-inductor technique. However, the total number of the frequency bands and thus the total frequency tuning range created by the switched-coupled inductors are limited because the inductor Q drops significantly as the number of switched-coupled inductors is increased.

In this chapter, a novel frequency tuning technique by changing the coupling coefficient of a transformer tank in a dual-band VCO is presented. By exploiting the three states with different magnetic coupling coefficients created by the

switched-triple-transformer technique, the stability problem is eliminated, and continuous frequency tuning range can be achieved, which significantly increase the tuning rang of VCO at mm-Wave frequency [6]. Furthermore, the design insights and design procedure of the multiband magnetically tuned VCO (MT-VCO) are also presented based on the derived analytical expressions of the switched transformers.

7.2   Transformer-Based Magnetic-Tuning Method

7.2.1   Working Principle

Before introducing the magnetic-tuning method, let's review the conventional one-port dual-band VCO with a transformer tank as shown in Fig. 6.3 first. According to (6.4), the oscillation frequencies ω_L and ω_H can be tuned by changing ω_1 and ω_2 through changing the capacitor C_1 and C_2, which corresponds to the conventional varactor tuning method and is limited at mm-Wave frequency as discussed earlier. On the other hand, ω_H and ω_L can also be tuned by changing the magnetic coupling coefficient k even when ω_1 and ω_2 are kept constant. As shown in Fig. 7.1, which plots the relationships between $\omega_H(\omega_L)$ and k for different ω_2/ω_1 ratios, with $\omega_H(\omega_L)$ being normalized to $\omega_2(\omega_1)$, it is clear that ω_H is quite sensitive to the coupling coefficient k. For example, if $\omega_1 = 60$ GHz and $\omega_2 = 75$ GHz are chosen, ω_H is changed from 77.2 to 85.6 GHz (or 11 %) when k increases from 0.15 to 0.35. In other words, changing the magnetic coupling coefficient k is an effective way to change the oscillation frequency and can be employed for coarse frequency tuning.

The switched-single-shielded transformer as shown in Fig. 7.2a provides a way to change the magnetic coupling coefficient k, where the shielded coil L_A along with a series switch M_A is inserted between the coils L_1 and L_2. Intuitively, when M_A turns on, the current i_1 in L_1 induces a current i_A' in L_A and another current i_2' in L_2, both of which are in the opposite direction with i_1. Since i_A' also in turn induces another current i_2'' in L_2, which tends to cancel i_2' and reduce the total induced current in L_2, as a result, the effective coupling coefficient k_{12} between L_1 and L_2 actually becomes lower as compared with the original transformer without L_A [7]. On the other hand, when M_A turns off, the coil of L_A is open, and there is no induced current flowing through L_A. So k_{12} remains almost the same. Consequently, k_{12} can be effectively changed by switching the transistor M_A "on" and "off." To calculate the effect of the switch on the inductance and energy loss, the switch transistor M_A can be modeled as a resistor $R_{on,A}$ when turned on and a parasitic capacitor $C_{off,A}$ when turned off as shown in Fig. 7.2b. The loss of each coil is modeled by the series resistance $R_{L1} = \omega L_1/Q_{L1}$, $R_{L2} = \omega L_2/Q_{L2}$, and $R_{LA} = \omega L_A/Q_{LA}$, where Q_{L1}, Q_{L2}, and Q_{LA} are the quality factors of coils L_1, L_2, and L_A, respectively. The model in Fig. 7.2b can be further simplified to the equivalent model constituted of two coupled coils with different model
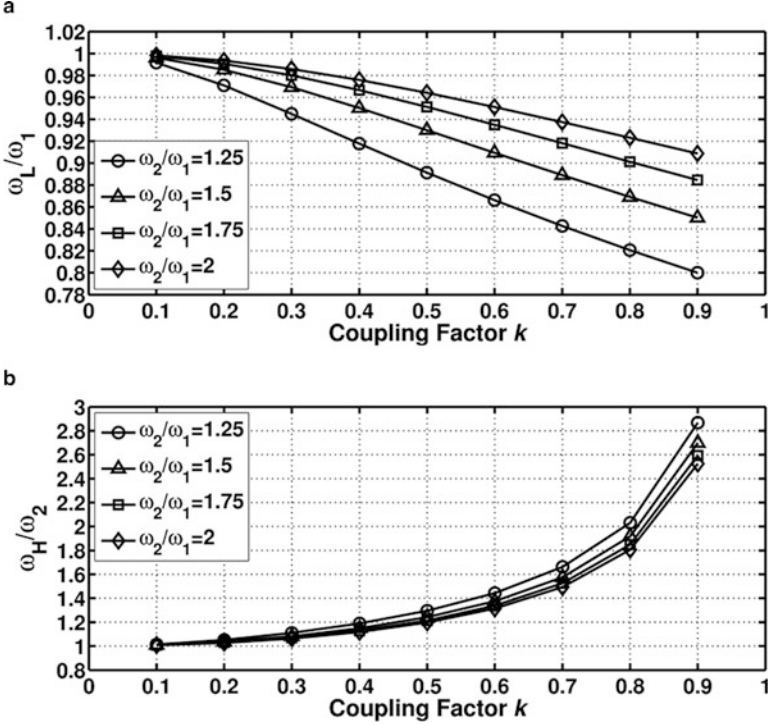
Fig. 7.1 Calculated (**a**) ω_L and (**b**) ω_H as functions of the magnetic coupling coefficient k for different ω_2/ω_1 ratios

parameters for low-k and high-k states as shown in Fig. 7.3. Here, the loss of the two coils are modeled by $R_{L1/2,low-k} = \omega L_{1/2,low-k}/Q_{L1/2,low-k}$ at low-k state and $R_{L1/2,high-k} = \omega L_{1/2,high-k}/Q_{L1/2,high-k}$ at high-k state, where $Q_{L1/2,low-k}$ and $Q_{L1/2,high-k}$ are the quality factors of the two coils at low-k and high-k states, respectively.

By applying the V-I equations to the three coupled coils, the model parameters for the single-shielded transformer in both the low-k and high-k states can be obtained (Appendix A.2).

In the low-k state, the switch M_A is on. With an assumption of a high-quality factor Q_{LA} and a small on-resistance $R_{on,A}$ of the switch so that $(R_{LA} + R_{on,A})^2 \ll (\omega L_A)^2$, the effective inductance $L_{1,low-k}'$ and the effective magnetic coupling coefficient $k_{12,low-k}'$ can be approximated as

$$L_{1,low-k}' \approx (1 - k_{1A}^2)L_1 \tag{7.1a}$$

$$k_{12,low-k}' \approx (k_{12} - k_{1A}k_{2A})\sqrt{\frac{L_1 L_2}{L_{1,low-k}' L_{2,low-k}'}} \tag{7.1b}$$
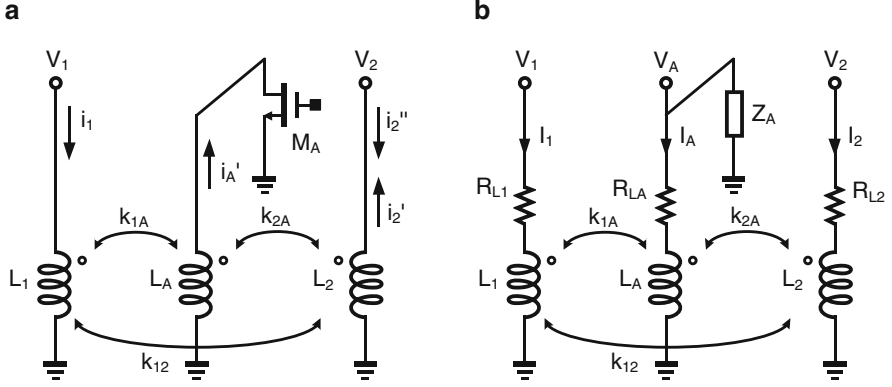
Fig. 7.2 Single-shielded transformer: (**a**) schematic and (**b**) model
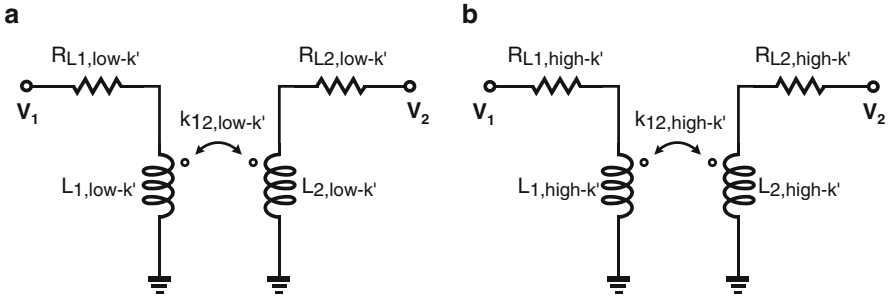
Fig. 7.3 Simplified equivalent models of the shielded transformer at (**a**) low-k state and (**b**) high-k state

In the high-k state, the switch M_A is off. It is reasonable to assume that $R_{LA}^2 \ll [(\omega C_{off,A})^{-1} - \omega L_A]^2$ with a small parasitic capacitance $C_{off,A}$ of the switch. Then $L_{1,high-k}'$ and $k_{12,high-k}'$ can be estimated as:

$$L_{1,high-k}' \approx \left(1 + \frac{1}{\omega_A^2/\omega^2 - 1}k_{1A}^2\right)L_1 \tag{7.2a}$$

$$k_{12,high-k}' \approx \left(k_{12} + \frac{k_{1A}k_{2A}}{\omega_A^2/\omega^2 - 1}\right)\sqrt{\frac{L_1 L_2}{L_{1,high-k}' L_{2,high-k}'}} \tag{7.2b}$$

where $\omega_A = (L_A C_{off,A})^{-1/2}$. Actually, two possible solutions for $L_{1,high-k}$ exist in (7.2a), which indicates the dual-resonance characteristic of the transformer tank with the capacitor load [5]. Here, the switch size is kept small enough to make sure $\omega_A > \omega$ so that only one resonant mode can occur over the entire frequency tuning range. Since coils L_1 and L_2 are in the symmetric positions, the model parameters

for the secondary coil L_2 ($L_{2,low-k}'$ and $L_{2,high-k}'$) can be obtained by just replacing k_{1A} and L_1 with k_{2A} and L_2 in (7.1a) and (7.2a), respectively.

   The problem for the single-shielded transformer is that switching on and off the coil L_A changes not only the coupling coefficient k_{12}' but also the effective inductance of $L_{1/2,low-k}'$ and $L_{1/2,high-k}'$, which can be seen from (7.1a) to (7.2b). So it makes the change of the effective magnetic coupling coefficient $\Delta k_{12}' = k_{12,high-k}' - k_{12,low-k}'$ less significant. For example, a high ω_H requires a high k; on the other hand, switching to the high-k state results in an increased effective inductance of coil L_2 since $L_{2,high-k}' > L_{2,low-k}'$, which in turn will make ω_2 drop. From either (7.1a) and (7.1b) or Fig. 7.1b, the large drop of ω_2 would decrease ω_H even when k_{12} increases. As such, in order to increase the frequency tuning range, it is highly desirable to keep $L_{1,low-k}' = L_{1,high-k}'$ and $L_{2,low-k}' = L_{2,high-k}'$ when the switch M_A is turned on and off.

7.2.2   Analysis of the Switched-Triple-Shielded Transformer

To solve the inductance imbalance problem in the single-shielded transformer, a switched-triple-shielded transformer is proposed to keep $L_{1,low-k}' = L_{1,high-k}'$ and $L_{2,low-k}' = L_{2,high-k}'$. In the switched-triple-shielded transformer as shown in Fig. 7.4a, two extra coils L_B and L_C with the switches M_B and M_C connected to their two ends are added to the left and right sides of L_1 and L_2, respectively. By replacing the switches M_A, M_B, and M_C with the impedance Z_A, Z_B, and Z_C as shown in Fig. 7.4b and using the similar method as that for the single-shielded transformer, the model parameters in both low-k and high-k states of the simplified model (Fig. 7.3) for the switched-triple-shielded transformer can be derived (Appendix A.2). Although the simplified model topology is the same as that of the switched-single-shielded transformer, the expressions for the model parameters are quite different.
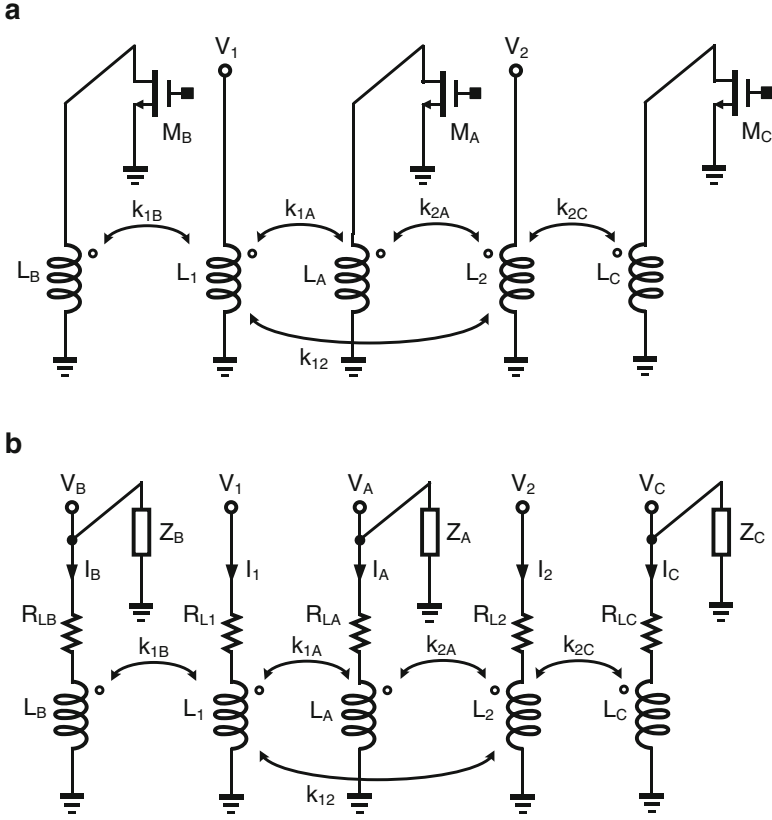
   In the low-k state, M_B and M_C are off while M_A is on. With the assumptions that $(R_{LA} + R_{on,A})^2 \ll (\omega L_A)^2$ and $R_{LB/C}^2 \ll [(\omega C_{off,B/C})^{-1} - \omega L_{B/C}]^2$, $L_{1,low-k}'$, $R_{L1,low-k}'$, and $k_{12,low-k}'$ can be approximated as

$$L_{1,low-k}' \approx \left[1 - k_{1A}^2 + \frac{1}{\omega_B^2/\omega^2 - 1}k_{1B}^2\right]L_1 \tag{7.3a}$$

$$R_{L1,low-k}' \approx R_{L1} + \frac{L_1}{L_A}k_{1A}^2(R_{LA} + R_{on,A}) + \frac{1}{(\omega_B^2/\omega^2 - 1)^2}\frac{L_1}{L_B}k_{1B}^2 R_{LB} \tag{7.3b}$$

$$k_{12,low-k}' \approx (k_{12} - k_{1A}k_{2A})\sqrt{\frac{L_1 L_2}{L_{1,low-k}' L_{2,low-k}'}} \tag{7.3c}$$

where $\omega_B = (L_B C_{off,B})^{-1/2}$ and $\omega_B > \omega$.

Fig. 7.4 The switched-triple-shielded transformer: (**a**) schematic and (**b**) model

In the high-k state, M_B and M_C are on while M_A is off. With the assumption that $(R_{LB/C} + R_{on,B/C})^2 \ll (\omega L_{B/C})^2$ and $R_{LA}{}^2 \ll [(\omega C_{off,A})^{-1} - \omega L_A]^2$, $L_{1,high-k}{}'$, $R_{L1,high-k}{}'$, and $k_{12,high-k}{}'$ can be estimated as:

$$L_{1,\,high\text{-}k}{}' \approx \left[1 + \frac{1}{\omega_A^2/\omega^2 - 1}k_{1A}^2 - k_{1B}^2\right]L_1 \tag{7.4a}$$

$$R_{L1,\,high\text{-}k}{}' \approx R_{L1} + \frac{1}{\left(\omega_A^2/\omega^2 - 1\right)^2}\frac{L_1}{L_A}k_{1A}^2 R_{LA} + \frac{L_1}{L_B}k_{1B}^2(R_{LB} + R_{on,B}) \tag{7.4b}$$

$$k_{12,\,high\text{-}k}{}' \approx \left(k_{12} + \frac{k_{1A}k_{2A}}{\omega_A^2/\omega^2 - 1}\right)\sqrt{\frac{L_1 L_2}{L_{1,\,high\text{-}k}{}' L_{2,\,high\text{-}k}{}'}} \tag{7.4c}$$

where $\omega_A = (L_A C_{off,A})^{-1/2}$ and $\omega_A > \omega$.

Interestingly, an additional state can also be exploited to further increase the frequency tuning range and relieve the stability problem by simultaneously turning on all the three switches. In this low-inductance (low-L) state, with assumptions

that $(R_{LA/B/C} + R_{on,A/B/C})^2 \ll (\omega L_{A/B/C})^2$, $L_{1,low-L}'$, $R_{L1,low-L}'$, and $k_{12,low-L}'$ can be approximated as:

$$L_{1,\,low-L}' \approx \left[1 - k_{1A}^2 - k_{1B}^2\right]L_1 \tag{7.5a}$$

$$R_{L1,\,low-L}' \approx R_{L1} + \frac{L_1}{L_A}k_{1A}^2(R_{LA} + R_{on,A}) + \frac{L_1}{L_B}k_{1B}^2(R_{LB} + R_{on,B}) \tag{7.5b}$$

$$k_{12,\,low-L}' \approx (k_{12} - k_{1A}k_{2A})\sqrt{\frac{L_1 L_2}{L_{1,\,low-L}' L_{2,\,low-L}'}} \tag{7.5c}$$

The expressions of $L_{2,low-k}'$, $R_{L2,low-k}'$, $L_{2,high-k}'$, $R_{L2,high-k}'$, $L_{2,low-L}'$, and $R_{L2,low-L}'$ can be obtained by replacing k_{1A}, k_{1B}, L_1, L_B, ω_B, R_{L1}, R_{LB}, and $R_{on,B}$ with k_{2A}, k_{2C}, L_2, L_C, ω_C, R_{L2}, R_{LC}, and $R_{on,C}$ in (7.3a), (7.3b), (7.4a), (7.4b), (7.5a), and (7.5b), respectively.

In both the low-k and high-k states, one of the two coils adjacent to L_1 or L_2 is always switched on, while the other is switched off. Consequently, it is possible to design the coupling coefficients k_{1A}, k_{1B}, k_{2A}, and k_{2C} and the switch sizes to keep $L_{1,low-k}' = L_{1,high-k}'$ and $L_{2,low-k}' = L_{2,high-k}'$. By using the expressions of $L_{1/2,low-k}'$ and $L_{1/2,high-k}'$ derived before, the following conditions can be obtained:

$$\frac{k_{1A}^2}{k_{1B}^2} = \frac{1 - \omega^2/\omega_A^2}{1 - \omega^2/\omega_B^2} \quad \text{and} \quad \frac{k_{2A}^2}{k_{2C}^2} = \frac{1 - \omega^2/\omega_A^2}{1 - \omega^2/\omega_C^2} \tag{7.6}$$

By making $k_{1A} = k_{1B}$, $k_{2A} = k_{2C}$, and $\omega_A = \omega_B = \omega_C$, (7.6) can be satisfied even when the frequency ω changes, and the effective change of the coupling coefficient $\Delta k_{12}' = k_{12,high-k}' - k_{12,low-k}'$ can be expressed below:

$$\Delta k_{12}' = 1/\sqrt{\left(\frac{\alpha}{k_{1A}} + 1\right)\left(\frac{\alpha}{k_{2A}} + 1\right)} \tag{7.7}$$

where $\alpha = (2 - \omega_A^2/\omega^2)/(\omega_A^2/\omega^2 - 1)$.

Figure 7.5 compares the calculated parameters for both the low-k and high-k states with the simulated results using the model shown in Fig. 7.4b, where $L_1 = 115$ pH, $L_2 = 66$ pH, $L_A = 86$ pH, $L_B = 150$ pH, $L_C = 60$ pH, and $k_{12} = 0.3$. For simplicity, the Q of each coil is assumed to be constant at 30 as the frequency is changed. To guarantee $L_{1/2,low-k}' = L_{1/2,high-k}'$, the condition $k_{1A} = k_{1B} = k_{2A} = k_{2C} = k_0$ is kept, and the switch sizes are designed to keep $\omega_A = \omega_B = \omega_C = \omega_0 = 115$ GHz. The effective parameters are plotted with different k_0 values. From both Fig. 7.5c and (7.7), larger k_0 results in larger $\Delta k_{12}'$ which is defined as the difference between $k_{12,high-k}'$ and $k_{12,low-k}'$. However, as shown in Fig. 7.5a, b, larger k_0 would also increase the loss from the shielded coils, which would increase $R_{L1/L2,\,low-k}'$ and $R_{L1/L2,\,high-k}'$ and degrade $Q_{L1/L2,low-k}'$ and $Q_{L1/L2,\,high-k}'$. So the choice of k_0 is the trade-off between the change of the magnetic

Fig. 7.5 Calculated and simulated values: (**a**) L_1' and Q_1', (**b**) L_2' and Q_2', (**c**) $\Delta k_{12}'$ for different k_0 ($\omega_A = \omega_B = \omega_C = \omega_0 = 115$ GHz)
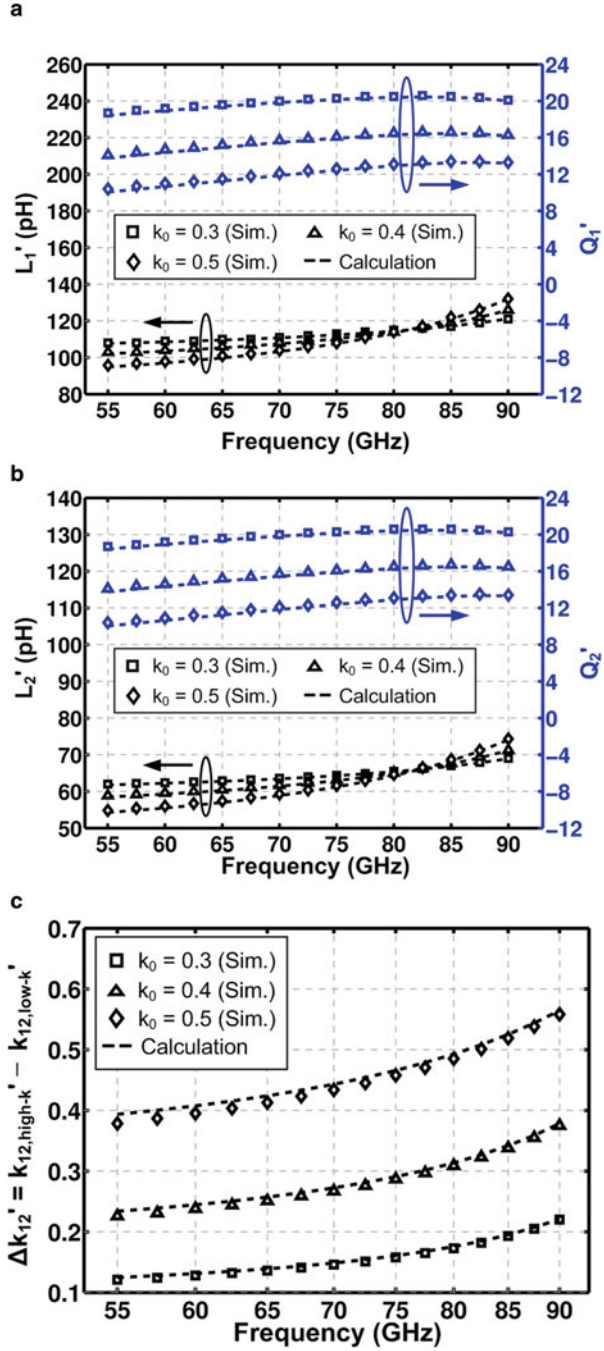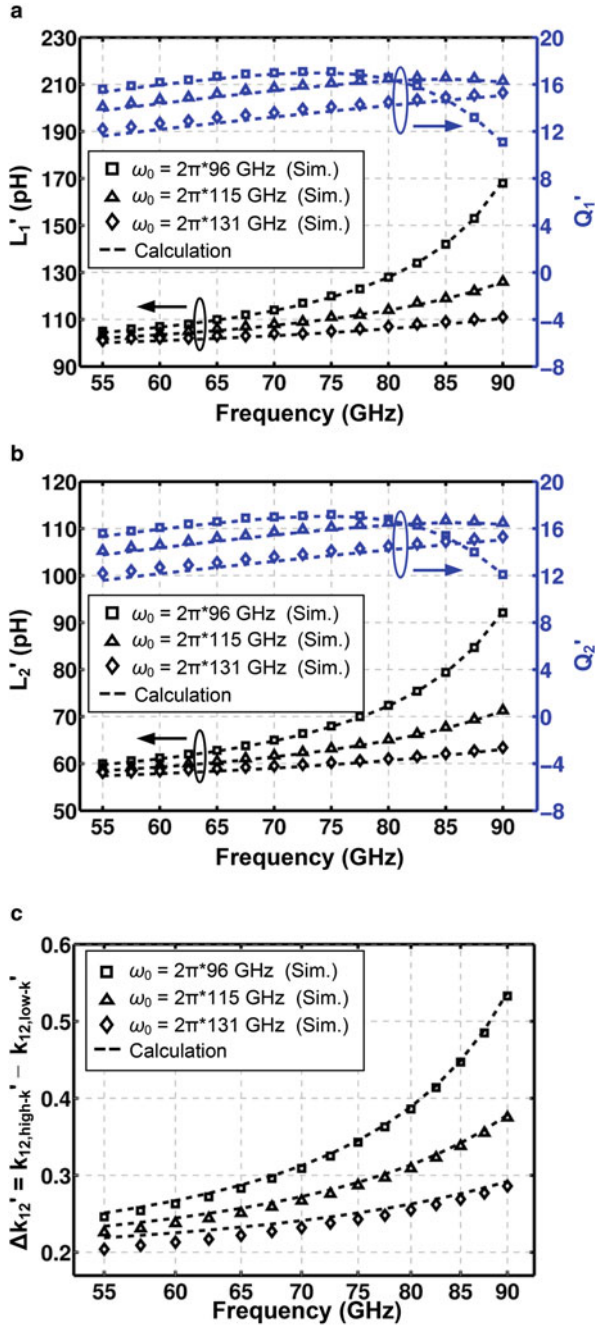
Fig. 7.6 Calculated and simulated values: (**a**) L_1' and Q_1', (**b**) L_2' and Q_2', (**c**) $\Delta k_{12}'$ for different ω_0 ($k_{1A} = k_{1B} = k_{2A} = k_{2C} = k_0 = 0.4$)

coupling coefficient $\Delta k_{12}'$ and the quality factors $Q_{L1/L2,low-k}'$ and $Q_{L1/L2,high-k}'$ of the effective inductances.

Figure 7.6 plots the calculated and simulated effective parameters by using the same $L_{1/2}$, $L_{A/B/C}$, and k_{12} values as used in Fig. 7.5. Here $k_{1A} = k_{1B} = k_{2A} = k_{2C} = 0.4$ is kept, and the switch sizes of M_A, M_B, and M_C are changed to obtain different ω_0 values. The turn-on resistors R_A, R_B, and R_C are also scaled with the switch sizes. It can be seen that small ω_0 results in better $Q_{L1/L2,low-k}'$ and $Q_{L1/L2,high-k}'$ when the operating frequency ω is much lower than ω_0 because the loss of the effective inductances is dominant by the turn-on resistances of the switches, which could be reduced with large switch sizes or small ω_0. However, when ω approaches ω_0, $Q_{L1/L2,low-k}'$ and $Q_{L1/L2,high-k}'$ would start to drop quickly because the series resistance in the shielded coils with the switches being off would dominate the total loss of the effective inductances. As a result, an optimal ω_0 exists for maximizing $Q_{L1/L2,low-k}'$ and $Q_{L1/L2,high-k}'$ in the desired operating frequency range.

7.3   Design and Analysis of the MT-VCO

To verify the magnetic-tuning technique, a MT-VCO prototype as shown in Fig. 7.7 is designed. The switched-triple-shielded transformer described in Sect. 7.2 is used for coarse frequency tuning, while a digitally controlled binary-weighted AMOS varactor array controlled by 2-bit B_1B_0 and a varactor with an analog control voltage V_C are employed for fine frequency tuning. The PMOS current tails are used to bias the gates of varactors at around 0.8 V with 1.2 V supply voltage to increase the capacitance tuning range of the varactors and thus the frequency tuning range of the MT-VCO. The RC filters between the biasing PMOS transistors $M_{5/6}$ and $M_{B5/B6}$ are employed to remove the thermal noise from $M_{B5/B6}$, which would contribute to a large portion of the output phase noise after frequency up-conversion if a large current ratio is used.

Since the topology of the MT-VCO is exactly the same as the conventional one-port dual-band oscillator with different designed parameters in the three states, the model shown in Fig. 6.3a can also be applied to it, and the VCO design parameters can be obtained as follows by simply using the results from Sect. 6.2 with appropriate expressions for the transformer's parameters $L_{1/2,low-k}'$, $L_{1/2,high-k}'$, $R_{L1/L2,low-k}'$, $R_{L1/L2,high-k}'$, $k_{12,low-k}'$, and $k_{12,high-k}'$ as derived in Sect. 7.2.2.

By replacing ω_1, ω_2 and k with $\omega_1' = \left(L_1'C_1'\right)^{-1/2}$, $\omega_2' = \left(L_2'C_2'\right)^{-1/2}$, and k_{12}', the oscillation frequency of ω_L' and ω_H' for the MT-VCO can still be expressed by (7.1a) and (7.1b). Since large $\Delta\omega_H'$ between the low-k and high-k states requires large $\Delta k_{12}'$, large k_0 is desired for larger coarse tuning range. Moreover, from Fig. 7.6b, when ω approaches ω_0, L_2' starts to increase quickly with frequency, which would in turn decrease ω_2' and limit the maximum achievable ω_H'. As a result, the maximum value of ω_H' can be further extended by increasing ω_0.
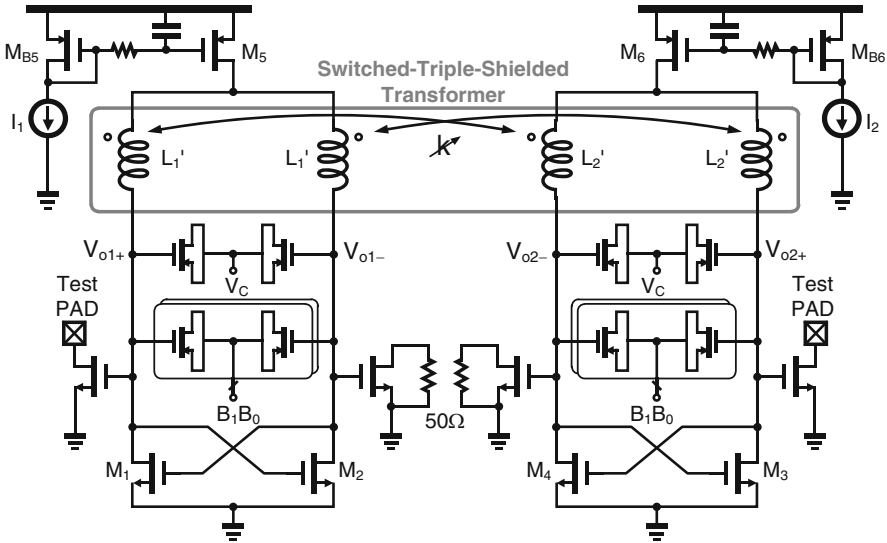
Fig. 7.7 Schematic of the MT-VCO

The one-port dual-band VCO will suffer from the stability problem as discussed in Sect. 6.2. If the amplitude of the two peak impedance at frequency ω_L' and ω_H' shown in Fig. 6.4 are close to each other, then the oscillator could jump from one desired equilibrium oscillation frequency to the other with some disturbance. So the difference between the two peak impedances must be kept large enough to make sure the oscillator is only operating at the wanted frequency, which can be achieved by either separating ω_L' and ω_H' far away or reducing the k_{12}'. Figure 7.8 shows the arrangement of the low-frequency band and high-frequency band in all the three states. The frequency bands of the low-k state are placed between the frequency bands of the high-k state to separate $\omega_{L,high-k}'$ and $\omega_{H,high-k}'$. Moreover, from (7.5a), because the inductance in the low-L state is smaller than that in both the low-k and high-k states, $\omega_{L,low-k}'$ and $\omega_{H,low-k}'$ can be further separated by placing the low-frequency band of the additional low-L state between the two frequency bands of the low-k state. Consequently, the MT-VCO can achieve a continuous ultrawide frequency tuning range without a stability problem. In addition, the high-frequency band of the low-L state can be employed to further increase the maximum oscillation frequency.

In either low-k or high-k state, by assuming that $Q_{L1}' = Q_{L2}' = Q_L'$, $Q_{C1}' = Q_{C2}' = Q_C'$, and $L_1'/L_2' = C_1'/C_2'$, according to (6.10a) and (6.10b), the tank Q of both the primary coil (Q_{tank1}') and the secondary coil (Q_{tank2}') can be estimated as
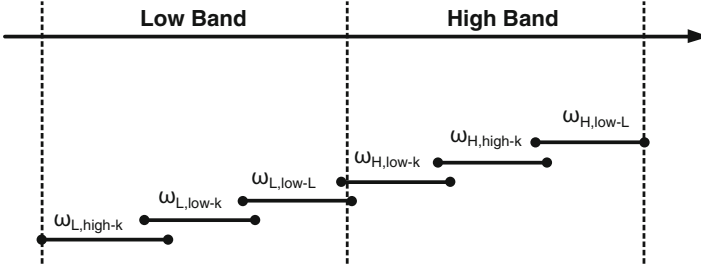
Fig. 7.8 Allocation of the three states for the two frequency bands

$$\frac{1}{Q_{tank1}{}'(\omega_L{}')} = \frac{(n^2 D_1^2 - 1) - k'^2_{12}}{(n^2 D_1^2 - 1) + k'^2_{12}} \frac{1}{Q_L{}'} + \frac{1}{Q_C{}'} \tag{7.8a}$$

$$\frac{1}{Q_{tank2}{}'(\omega_H{}')} = \frac{(1 - D_2^2/n^2) + k'^2_{12}}{(1 - D_2^2/n^2) - k'^2_{12}} \frac{1}{Q_L{}'} + \frac{1}{Q_C{}'} \tag{7.8b}$$

where $D_1 = \omega'^2_1/\omega^2$, $D_2 = \omega'^2_2/\omega^2$, and $n = \omega'_2/\omega'_1$. Compared with the second-order LC tank with the same $Q_L{}'$ and $Q_C{}'$, the contribution of $Q_C{}'$ to the fourth-order LC tank's Q is the same, so whether the tank Q of the fourth-order LC tank is enhanced or degraded would mainly depend on the quality factor $Q_L{}'$ of the effective inductances in the switched-triple-shielded transformer derived in Sect. 7.2.2. By assuming $Q_L = 30$, $Q_C = 6$, the Q of the second-order tank is calculated to be 5. By using $\omega'_1 = 60\,\text{GHz}$, $\omega'_2 = 75\,\text{GHz}$, and $k_{12}' = 0.15/0.35$ and assuming that $Q_L{}'$ drops to around 12 (which is consistent to the simulation results in Figs. 7.5 and 7.6), $Q_{tank1}{}'$ and $Q_{tank2}{}'$ are calculated to be around 4.1 and 3.9 and 4.3 and 3.5 in the low-k and high-k states, respectively. From (7.8a) and (7.8b), it can be seen that $Q_{tank1}{}'$ is always larger than $Q_{tank2}{}'$, and the difference between $Q_{tank1}{}'$ and $Q_{tank2}{}'$ can be reduced by increasing ω'_2/ω'_1 or decreasing $k_{12}{}'$ when k is small. As such, the allocation of the frequency bands in the MT-VCO also helps reduce the difference between $Q_{tank1}{}'$ and $Q_{tank2}{}'$ by enlarging the ω'_2/ω'_1 ratio.

The noise-shaping property of a transformer-based LC tank is basically the same as that of a second-order LC tank within a narrow bandwidth around the oscillation frequency. It follows that the phase noise of the MT-VCO in either the low band or the high band can also be obtained directly by using the time-variant phase-noise analysis result from [8]:

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{k_B T}{C'} \frac{\omega}{Q_{tank1/2}{}' \Delta\omega^2 A_{1/2}^2}(1 + \gamma)\right] \tag{7.9}$$

where k is the Boltzmann constant, T is the absolute temperature, $C' = C_{1/2}'/2$ is the tank capacitance connected to either the primary coil or the secondary coil as shown in Fig. 6.3a, $Q_{tank1/2}'$ is the tank Q from either the primary or the secondary coil, $\Delta\omega$ is the offset frequency from the oscillation frequency ω, γ is the MOS channel noise factor, and $A_{1/2}$ is the output amplitude. From (7.9), it can be seen that the phase noise is directly related to the $Q_{tank1/2}'$. Compared with a conventional oscillator using a second-order LC tank with $Q_{tank} = 5$, the phase-noise degradation of the MT-VCO with $Q_{tank1/2}' = 4$ is only about 1 dB assuming that both oscillators are biased at the boundary of the voltage- and current-limited region to achieve the same maximum output voltage swing.

From the analysis above, the design procedure of the MT oscillator can be summarized as below:

1. Selecting and designing the geometrical dimensions of the primary and the secondary coils for suitable values of L_1, L_2, and k_{12}. Since k_{12}' is dominant by k_{12} from (7.3c) and (7.4c), for the same $\Delta k_{12}'$, larger k_{12} would result in larger frequency difference between the low-k and high-k states as can be seen from the plots in Fig. 7.5c, which implies more effective coarse frequency tuning capability. However, for stability considerations, larger k_{12} requires larger ratio of ω_H'/ω_L'. This would cause a larger frequency gap between the low-frequency band and the high-frequency band of the low-k state, which however cannot be covered effectively even by employing the low band of the low-L state. As a result, the frequency tuning range can be discontinuous.
2. After fixing the design parameters of L_1 and L_2, the spaces between L_1 and L_A and L_B and between L_2 and L_A and L_C can be designed to guarantee that $k_{1A} = k_{1B}$ and $k_{2A} = k_{2C}$. As discussed earlier, the choices of the absolute values of k_{1A} or k_{2A} are the trade-off between the coarse frequency tuning capability and the Q_{L1}' and Q_{L2}'.
3. Designing the ratios between the switch sizes of M_A, M_B, and M_C to make sure that $C_{off,A}$, $C_{off,B}$, $C_{off,C}$ are properly chosen to guarantee that $\omega_A = \omega_B = \omega_C$. The choice of the absolute value of the switch sizes is to obtain high Q_{L1}' and Q_{L2}' while still preventing Q_{L1}' and Q_{L2}' from dropping at the desired maximum oscillation frequency.

Figure 7.9 shows the layout of the switched-triple-shielded transformer with all the five coils being implemented by the top thick metal, which occupies an area of $124 \times 115 \ \mu m^2$. The metal widths of coils $L_{1/2}$, L_A, $L_{B/C}$ are 4.5, 4, 2 μm, respectively. The spacing between L_B and L_1, between L_1 and L_A, between L_A and L_2, and between L_2 and L_C are 5, 3.5, 4.5, and 3.5 μm, respectively. The W/L ratios of M_A, M_B, and M_C are designed to be 27.5 μm/0.06 μm, 17.5 μm/0.06 μm, 42.5 μm/0.06 μm, respectively, all with 2.5-μm finger widths. Odd finger number is used to keep the same parasitic capacitance at the drain and the source in the layout. The source and drain of the switches M_A, M_B, and M_C are biased to the

Fig. 7.9 Layout of the switched-triple-shielded transformer
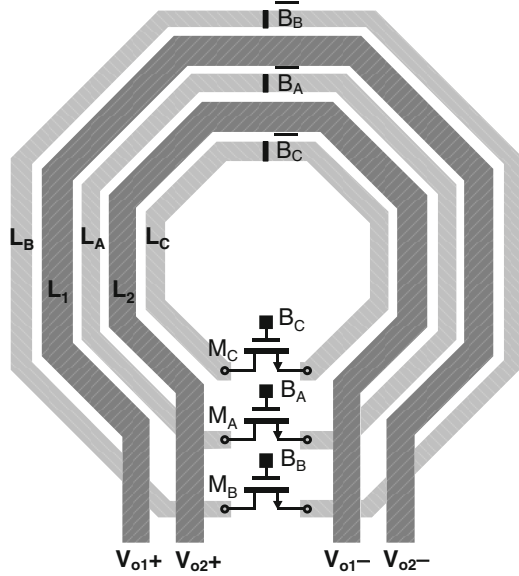

opposite logic levels of the gate voltages through the center taps of the shielding inductors to reduce the parasitic junction capacitance when the switches are off. By doing so, the biasing resistors connected to the drain and source in the conventional designs [5] can be eliminated, which helps prevent further degradation of Q_{L1}' and Q_{L2}'.

Figure 7.10 shows the electromagnetic simulation results of the effective inductances and Qs for the primary and secondary coils of the triple-shielded transformer. L_1' and L_2' are 105 pH and 75 pH in both the low-k and high-k states and 80 pH and 50 pH in the low-L state, respectively. k_{12}' is reduced from 0.35 to 0.15 from the high-k to the low-k state. Q_{L1}' and Q_{L2}' are around 10 and 12 in all the three states, which are still much higher than the varactors Q at the target mm-Wave frequencies.

7.4   Experimental Results

The MT-VCO is fabricated in a 1P6M LP 65 nm CMOS process and draws 7–9 mA from 1.2 V supply. The DC gate bias voltages for M_A, M_B, and M_C are the same as the supply voltage. Figure 7.11 shows the chip micrograph occupying a core area of 0.03 mm^2.
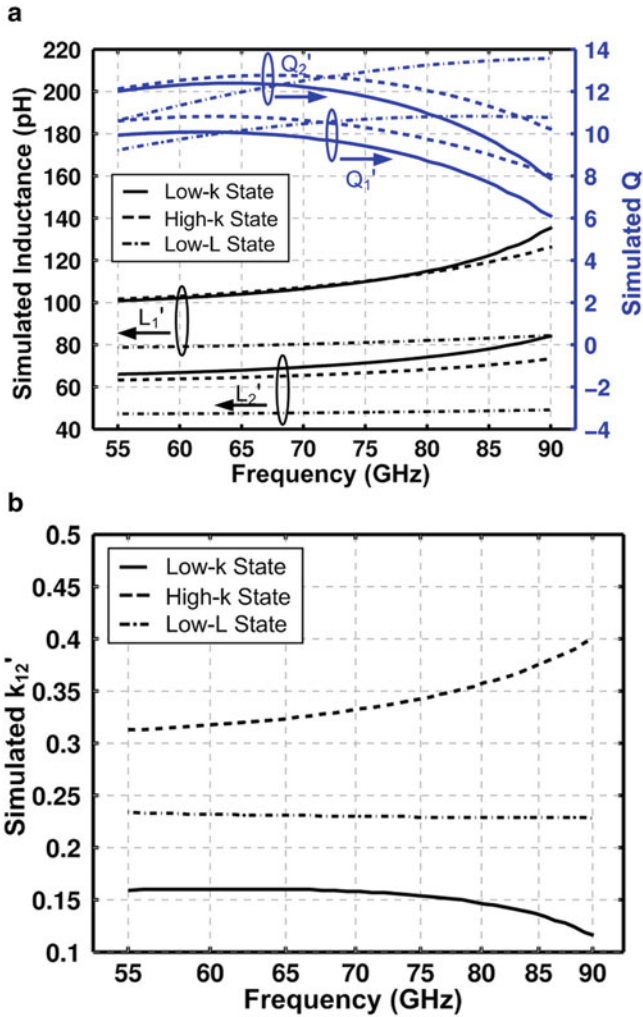
Fig. 7.10 EM simulation results of the triple-shielded transformer: (**a**) inductances and quality factor Qs, (**b**) magnetic coupling coefficients

Table 7.1 summarizes the control logics of the switches in the shielding coils and the biasing currents for the negative-g_m cell connecting to the primary and the secondary coils of the transformer tank for six different modes associated with the three different states. The final implementation uses $B_B B_A B_C = 011$ in Mode 2 and $B_B B_A B_C = 001$ in Mode 5 instead of $B_B B_A B_C = 010$ and $B_B B_A B_C = 101$ to obtain large ω_2'/ω_1' ratios to shift up the frequency tuning range in Mode 2 and minimize the tanks' Qs degradation in Mode 5 as discussed in Sect. 7.3, respectively. Since changing $B_B B_A B_C$ from "010" to "011" in Mode 2 or changing $B_B B_A B_C$ from
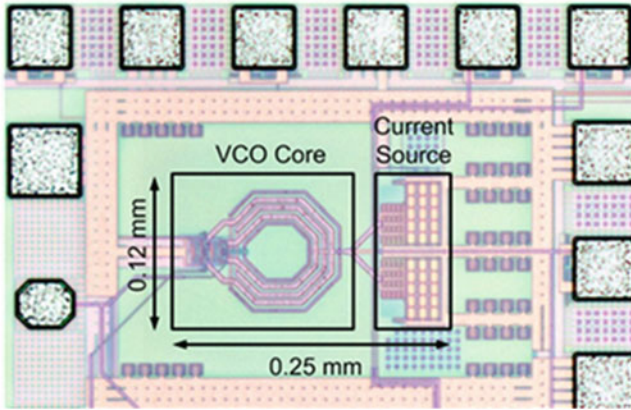
Fig. 7.11 Chip micrograph of the MT-VCO

Table 7.1 Control logics and arrangement for mode selection

	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
$B_B B_A B_C$	101	011	111	010	001	111
I_1	On	On	On	Off	Off	Off
I_2	Off	Off	Off	On	On	On
States	High-k	Low-k	Low-L	Low-k	High-k	Low-L
Bands	Low band			High band		

Table 7.2 Measured frequency tuning range in mode 2 and 5 for different $B_B B_A B_C$ combinations

Mode 2	$B_B B_A B_C = 010$ (theoretical configuration)	$B_B B_A B_C = 011$ (practical configuration)
Tuning range	57.2–64.3 GHz	57.9–64.9 GHz
Mode 5	$B_B B_A B_C = 101$ (theoretical configuration)	$B_B B_A B_C = 001$ (practical configuration)
Tuning range	79.2–85.7 GHz	78.5–85.3 GHz

"101" to "001" in Mode 5 only changes ω_2' in Mode 2 or ω_1' in Mode 5, the oscillation frequency would not change significantly if k_{12}' between L_1' and L_2' is small, which can be seen from either Fig. 7.1a or be verified by the measured frequency tuning range in Table 7.2. So the theoretical analysis in Sect. 7.3 can still be applied.
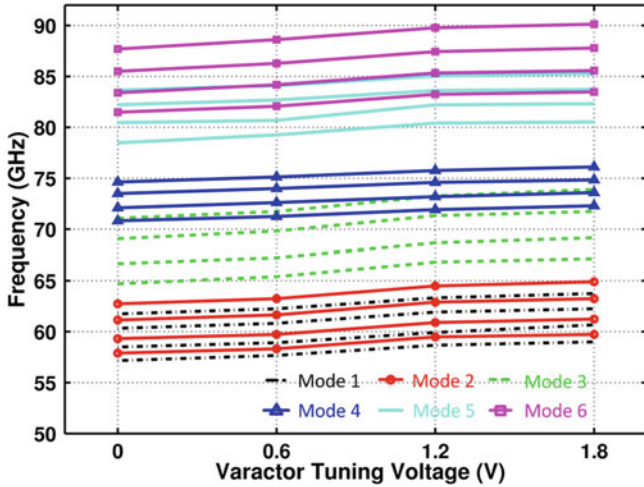
Fig. 7.12   Measured frequency tuning range
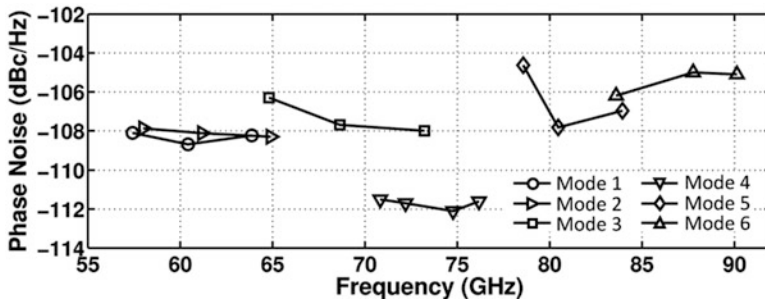
Fig. 7.13   Measured VCO phase noise and at 10-MHz offset frequency

Figure 7.12 shows the measured frequency tuning range as functions of the varactor tuning voltage for the different modes. As shown in (6.4), ω_L is not so sensitive to the change of k_{12} compared with ω_H when k_{12} is small. As such, the operating frequency in Mode 1 and 2 are almost the same as expected. Due to inaccurate modeling, a small frequency gap exists from 76.2 to 78.5 GHz between Mode 4 and Mode 5, which can be eliminated by shifting up the operating frequency of Mode 4 with modification of the transformer tank parameter. Since the total frequency tuning range relies on the tuning range of fine-tuning varactors and the frequency separation between different modes, the frequency separation between each mode needs to be reduced if smaller varactor tuning voltage or larger overlapping between each mode is required in the practical application, which would inevitably decrease the total frequency tuning range.

Figure 7.13 shows the measured phase noise over the entire frequency tuning range. The current consumption is 7 mA for Modes 1, 2, 4, 5, and 6 and 9 mA
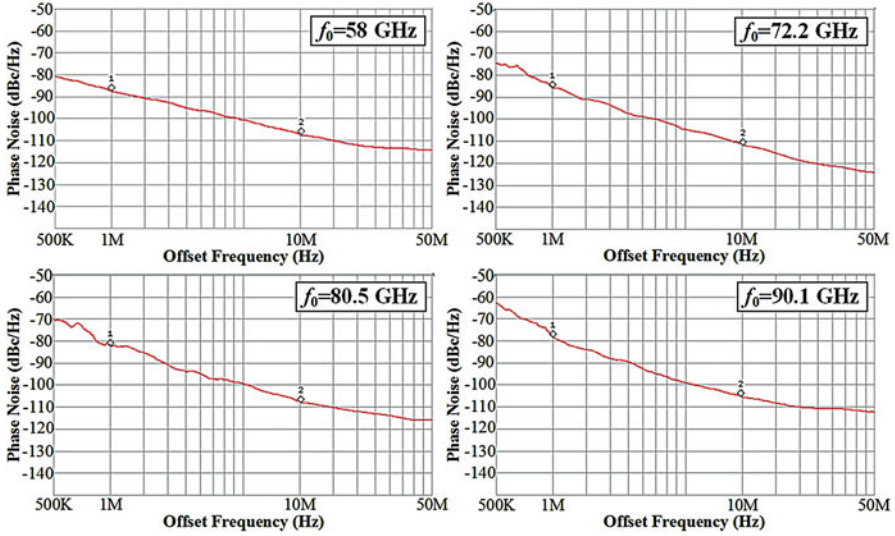
Fig. 7.14 Measured VCO phase noise as functions of offset frequency at different carrier frequencies

for Mode 3, respectively. It can be seen that phase noise in Mode 4 is better than that in other modes. Compared with Mode 5, the tank Q degradation in the high-band mode of dual-band VCO is reduced when k_{12}' is small even when $Q_{L2,low-k}'$ and $Q_{L2,high-k}'$ are kept the same as discussed in Sect. 8.3. It follows that Q_{tank2}' in Mode 4 (low-k state) is larger than that in Mode 5 (high-k state). Compared with Modes 1, 2, and 3, it is because that the effective quality factor Q_{L2}' is larger than Q_{L1}'. In the Modes 6 (low-L state), since the tank impedance drops due to that the tank capacitance does not scale with the inductance when frequency increases, the phase noise is degraded when the same bias current as that in Mode 4 is used. Figure 7.14 shows the phase-noise plots after down-converting the VCO output to around 400 MHz by V-band and W-band balanced mixers. The measured single-ended output power varies from -20 to -25 dBm over the tuning range after de-embedding. Finally, Table 7.3 summarizes and compares the measured performance of the presented MT-VCO with that of the recently reported state-of-art mm-Wave CMOS VCOs. Thanks to the triple-shielded-transformer-based magnetic-tuning technique, the MT-VCO prototype achieves a much larger frequency tuning range of 41.4 % while still keeping a compact area of 0.03 mm^2.

Table 7.3 Performance summary and comparison

Reference	Technology	Freq. (GHz)	TR	Power (mW)	PN@10 MHz (dBc/Hz)	FOM (dBc/Hz)	FOM_T (dBc/Hz)	Area (mm^2)
[9]	65-nm SOI	70.2	9.6 %	5.4	−106.1	−175.8	−175.4	0.0027
[2]	90-nm CMOS	58.4	9.6 %	8.1	−111[a]	−177.2	−176.6	0.0077
		61.7	4.9 %	1.2	−110[a]	−185	−178.6	
[7]	65-nm CMOS	58.2	7.6 %	22[b]	−115 to −117[a]	−177 to −179	−174.5 to −176.5	0.075
[10]	0.13-μm CMOS	60	16.7 %	30	−117.1[a]	−177.9	−182.3	0.172[c]
[11]	65-nm CMOS	67.1	27 %	5.8	−109.5[a]	−178.4	−187	0.031
[12]	90-nm CMOS	61.05	9.27 %	10.6	−110.1[a]	−174.4	−174.9	0.01
[13]	0.13-μm CMOS	50.3	6.8 %	35[d]	−127.8	−186.4	−183.0	0.18[e]
		58.5	9 %	34[b]	−120.6	−180.6	−179.7	0.1[e]
[14]	0.18-μm CMOS	40	20 %	27	−120.2[a]	−177.9	−183.9	0.625[e]
[15]	65-nm CMOS	56	17	15	−119.4[a]	−182.2	−186.8	0.05
[16]	0.13-μm CMOS	62.1	10	3.9	−115[a]	−185	−185	0.00375
		59.1	10.2	3.9	−111[a]	−181	−181.2	0.00425
This work	65-nm CMOS	73.8	41.1 %	8.4–10.8	−104.6 to −112.2[f]	−172 to −180[f]	−184.2 to −192.2[g]	0.03

[a]Phase noise normalized from 1-MHz offset in the original measured data from the references

[b]4-Phase output

[c]Area including the divider

[d]8-Phase output

[e]Area including pads

[f]Best and worst data of phase noise or FOM across the frequency range

[g]FOM_T calculated based on best and worst data of FOM across the frequency range

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Chapter 8
Transformer-Based Injection-Locked Frequency Divider

8.1 Introduction

In Chap. 5, ultralow-voltage VCOs operating near or even lower than the transistor threshold voltage while still achieving low phase-noise performance were demonstrated by employing the transformer-feedback technique. In order to realize ultralow-voltage frequency synthesizers with high performance, the next obstacle to be conquered is the design of frequency dividers capable of operating at ultralow supply voltages, especially the first frequency divider (prescaler) following the VCO, which has the input frequency as high as the output frequency of the VCO.

On the other hand, at mm-Wave frequency, the conventional LC tank-based ILFDs suffer from a critical problem with limited locking range as discussed in Chap. 4. Recently, many design techniques have been reported to increase the locking range of mm-Wave ILFDs. In [1–4], the reported locking ranges are still smaller than 13 %, while wide locking (>17 %) is achieved at the cost of large power consumption (>6 mW) in [5, 6]. In [7], wide locking range of 25.1 % is achieved with small power consumption of 1.65 mW, by separating the loading capacitance with multi-order LC tanks [7]. However, the use of multi-order LC tanks not only significantly increases the silicon area but also decreases the output power and degrades the driving capability of the ILFD.

Firstly, in this chapter, regenerative-ILFD architecture is proposed to reduce the power consumption and boost the operating frequency range of the conventional Miller divider as shown in Fig. 4.6. Moreover, the regenerative-ILFD architecture enables the use of transformer-feedback techniques to achieve ultralow-voltage operation. As illustration, two ultralow-voltage frequency divider architectures are presented and discussed [8, 9]. Working at a supply voltage comparable to the transistor's threshold voltage, the first design, referred to as transformer-feedback regenerative ILFD (TF-ILFD), provides fully balanced differential inputs and differential outputs, while the second design, referred to as transformer-feedback regenerative quadrature ILFD (TF-QILFD), provides fully balanced quadrature

outputs when differential inputs are applied. Both designs successfully demonstrate wide input frequency range and low-power consumption even at ultralow supply voltages.

Secondly, a single-transformer-based self-frequency-tracking (SFT) technique [10] is presented to increase the locking range of the conventional direct-injection ILFD at mm-Wave frequency while still keeps low-power consumption and compact chip area.

8.2 Ultralow-Voltage ILFDs Using Transformer Feedback

8.2.1 Regenerative-ILFD Architecture

As discussed in Sect. 4.4, the locking range of conventional Miller divider as shown in Fig. 4.24b is limited by the insufficient loop gain to maintain the oscillation since the double-balanced mixer architecture cancels the mixing outputs $i_0(\omega)$ and $-i_0(\omega)$ between the DC bias voltage and the output voltage $v_0(\omega)$ so that the total injection current to the tank $i_t(\omega)$ only consists of $i_{inj}(\omega)$ as shown in Fig. 4.26. To achieve certain operating frequency range, $i_{inj}(\omega)$ needs to be large to satisfy the gain condition, which can be realized by increasing the size of the mixing transistors and/or biasing them at a large current. However, the power consumption would be inevitably large, and large parasitic capacitance from the mixing transistors would limit the maximum operating frequency as well.

Besides the current-bleeding Miller dividers presented in Sect. 4.4, the regenerative-ILFD as shown in Fig. 8.1 can also enhance the loop gain and thus significantly boost the operating frequency range by adding the negative transconductance provided by the cross-coupled pair $M_{5/6}$. The gain enhancement effect can also be recognized from the corresponding behavioral model as shown in Fig. 8.2. A new current component $i_{ccp}(\omega) = -k_1 I_B v_o(\omega)$, which comes from the mixing of the bias current I_B and the output voltage $-v_o(\omega)$ through Mixer 2 ($M_{5/6}$) has been added to the total current injected into the LC tank. With the help of $i_{ccp}(\omega)$, $|i_t(\omega)|$ is increased, and the locus of $i_t(\omega)$ is shifted to the right, which relaxes the gain condition as shown in Fig. 8.3. As a result, the maximum phase shift that $i_t(\omega)$ can provide is increased, and the frequency locking range is increased accordingly. Since the conversion gain of Mixer 2 is much larger than that of Mixer 1a (or Mixer 1b) which makes use of the weak second-order distortion effect of the transistor $M_{1/3}$ (or $M_{2/4}$), it is more power efficient to increase $i_{ccp}(\omega)$ than to increase $i_{inj}(\omega)$. As such, the regenerative ILFD is capable of achieving a large locking range at a small power consumption. Unlike the conventional Miller frequency divider, if the negative transconductance provided by $M_{5/6}$ is large enough, the regenerative ILFD will self-oscillate even when there is no input signals, so we still catalog it into the family of ILFDs.
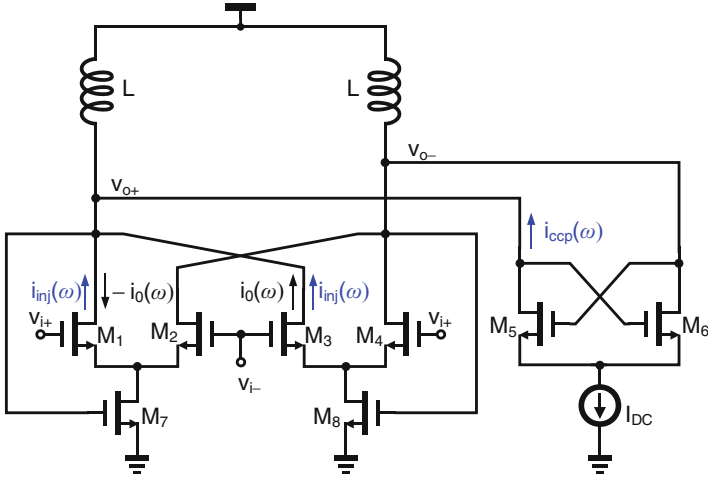
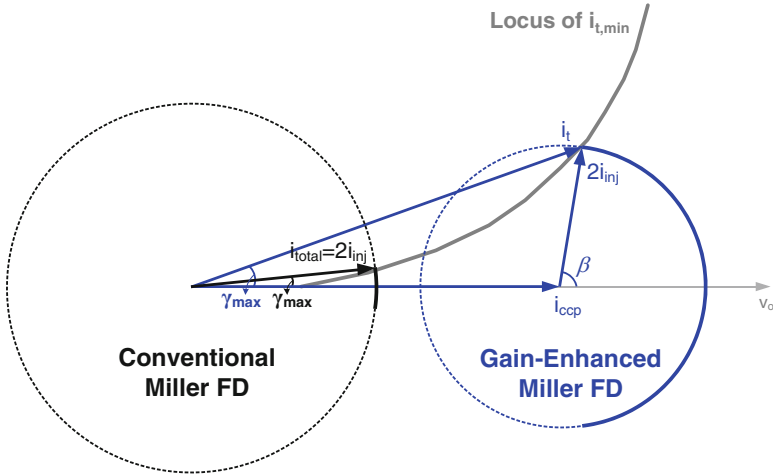**Fig. 8.1** Schematic of the regenerative ILFD
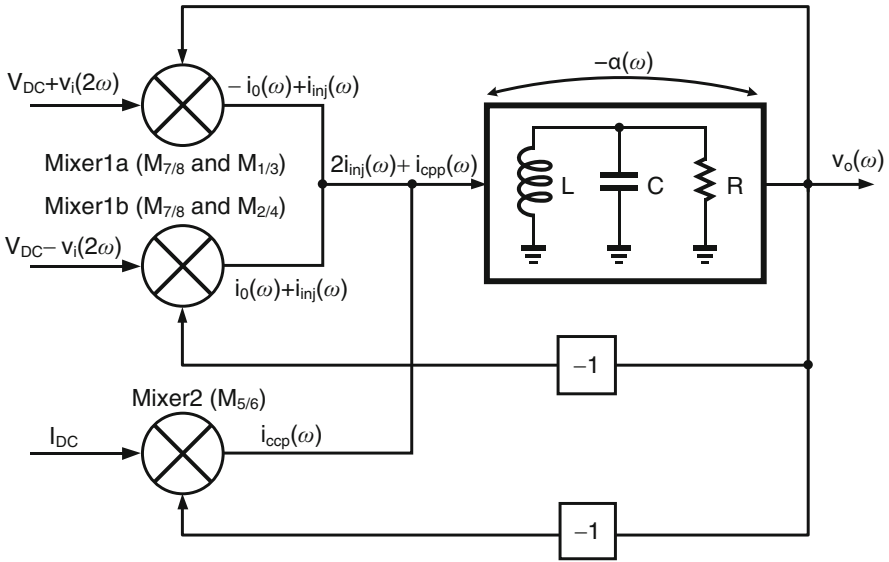
Fig. 8.2 Behavioral model of the regenerative ILFD

8.2.2 *Ultralow-Voltage Regenerative ILFD*

The regenerative ILFD requires at least two cascoded transistors in each path from supply to ground, which limits the minimum supply voltage. To further reduce the supply voltage, the bottom transistor in the regenerative ILFD should be eliminated. Alternatively, transformers become an attractive approach.

Fig. 8.3 Phase diagrams of the conventional Miller divider and the regenerative ILFD

Transformer-Based Regenerative ILFD

Figure 8.4 shows the schematic of the differential-input differential-output transformer-based regenerative ILFD (TF-ILFD) [8, 9], which can be viewed as the combination of an oscillator and a mixer (Fig. 8.5). In the TF-ILFD, the conventional LC-VCO is replaced with a TF-VCO as presented in Sect. 5.2, which is made of by the cross-coupled transistors $M_{5/6}$ and the integrated transformer with primary coil L_d and secondary coil L_s. A double-balanced mixer, constructed by the transistors M_{1-4}, is also implemented with the input signals applied at the gates of the switching pair M_{1-4}. Different from the topology in Fig. 8.1, the feedback from the VCO outputs to the second inputs of the mixer are implemented by employing the same transformers used in the TF-VCOs. By replacing the active devices at the bottom of the switching pairs in the conventional Gilbert mixers with the second coils L_s of the transformers, the supply voltage can be reduced. In addition, with proper transformer coupling, the signals at the drain and the sources can oscillate in phase and swing above the supply voltage and below the ground, respectively. Consequently, the effective minimum supply voltage can be further reduced.

Figure 8.6 illustrates the behavioral model of the TF-ILFD. The two mixers Mixer 1a and Mixer 1b that model the input transistors M_{1-4} in Fig. 8.2 are combined into Mixer 1 since the mixing outputs $-i_0(\omega)$ and $i_0(\omega)$ are canceled with each other, and only the term $2i_{inj}(\omega)$ is preserved after summing up the outputs of Mixers 1a and 1b. For simplicity, assuming $k = 1$ and defining the turn ratio between the primary and secondary coils as $N = \sqrt{L_d/L_s}$, the transformer will have a voltage transfer ratio $v_d/v_s = N$. As such, for Mixer 1, the second input is just $v_s(\omega)$ since the gate of transistors M_{1-4} are connected to the inputs $v_i(2\omega)$. For Mixer 2, the second input is the overdrive voltage $v_{gs}(\omega) = v_{o+}(\omega) - v_{s-}(\omega)$.
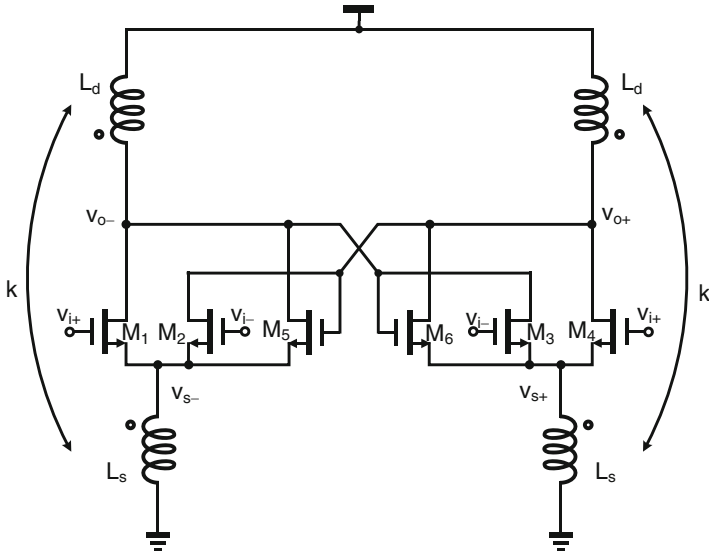
Fig. 8.4 Schematic of the TF-ILFD

Fig. 8.5 Simplified block
diagram of the TF-ILFD
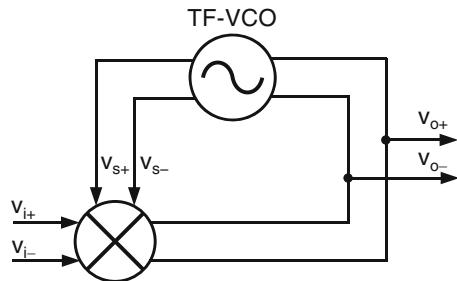
Since the drain and source voltage are in phase, $v_{gs}(\omega) = v_o(\omega) + v_s(\omega) = (1 + 1/N)v_o(\omega)$ and a scaling factor of $1 + 1/N$ is inserted to the feedback path between $v_o(\omega)$ and Mixer 2. The phasor diagram of the TF-ILFD is just the same as the one in Fig. 8.3 with the $i_{inj}(\omega)$ and $i_{ccp}(\omega)$ expressed as below:

$$i_{in\,j}(\omega) = K_1 \cdot \frac{1}{N} v_o(\omega) \cdot v_i(2\omega) \qquad (8.1a)$$

$$i_{cc\,p}(\omega) = K_2 \left(1 + \frac{1}{N}\right) \cdot v_o(\omega) \qquad (8.1b)$$

where K_1 and K_2 are the conversion gains of Mixers 1 and 2, respectively.

To estimate the frequency response of the transformer tank, the T-model as shown in Fig. 8.7a is employed to model the transformer, where R_L represents the
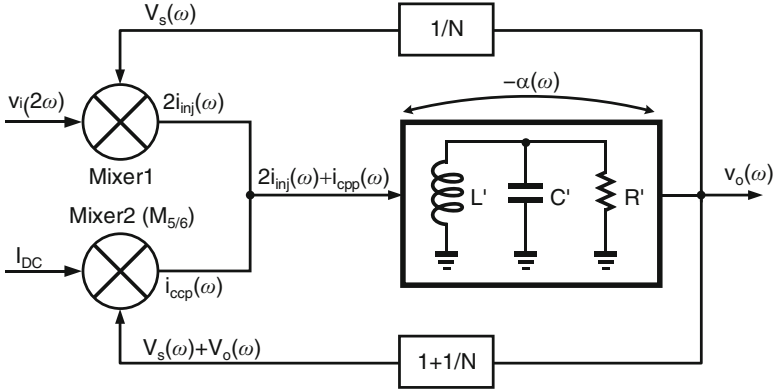
Fig. 8.6 Behavioral model of the TF-ILFD

loading impedance at the secondary coil. Consequently, the impedance of transformer looking into the primary coil can be derived as:

$$Z_{in} = \frac{j\omega L_P\left[L_s C_s R_L\left(1-k^2\right)\omega^2 - j\omega L_s\left(1-k^2\right) - R_L\right]}{-L_d C_d L_s C_s\left(1-k^2\right)\omega^4 + \omega^2 R_L(L_d C_d + L_s C_s) - R_L + j\left[\omega^3 L_d C_d L_s\left(1-k^2\right) - \omega L_s\right]}$$

(8.2)

As plotted in Fig. 8.7b, there is only one dominant peak frequency for the tank impedance when $N = 4$ is chosen. In other words, the transformer tank can be represented by the equivalent LC tank (L', C', and R') within the frequency locking range of the divider as shown in Fig. 8.6.

Similar to the discussion in Sect. 5.2, a small turn ratio of $N = \sqrt{L_d/L_s}$ would increase $v_s(\omega)$ and the conversion gain of Mixers 1 and 2, which helps increase $|i_{inj}(\omega)|$ and $|i_{ccp}(\omega)|$ and thus the frequency locking range at low supply voltages. On the other hand, a small N would degrade the loop-gain condition and push the locus of the optimal i_t to the right, which tends to degrade the frequency locking range for given $|i_{inj}(\omega)|$ and $|i_{ccp}(\omega)|$. As a result, in the TF-ILFD, N is designed to be optimally around 4 to balance the increasing of $|i_{inj}(\omega)|$ and $|i_{ccp}(\omega)|$ and the degradation of the loop-gain condition.

According to the phasor diagrams in Fig. 8.8a, if $|i_{ccp}(\omega)|$ is fixed, a larger $|i_{inj}(\omega)|$ is always preferred to obtain a larger phase $|\gamma_{max}|$ and thus larger locking range no matter whether the divider is limited by the phase condition or the gain condition. However, a large $|i_{inj}(\omega)|$ requires large transistor sizes of M_{1-4}, which increases both the input and output loadings and limits the maximum operating frequency. On the other hand, for a fixed $|i_{inj}(\omega)|$, as shown in Fig. 8.8b, an optimal $|i_{ccp}(\omega)|$ exists for achieving maximum operating frequency range under the condition that the phasor $2i_{inj}(\omega)$ is vertical to the phasor $v_o(\omega)$, while the end point of the phasor $2i_{inj}(\omega)$ is kept on the locus of $i_{t,min}(\omega)$. In practice, this optimal condition can be achieved by properly sizing the W/L ratios of $M_{5/6}$.
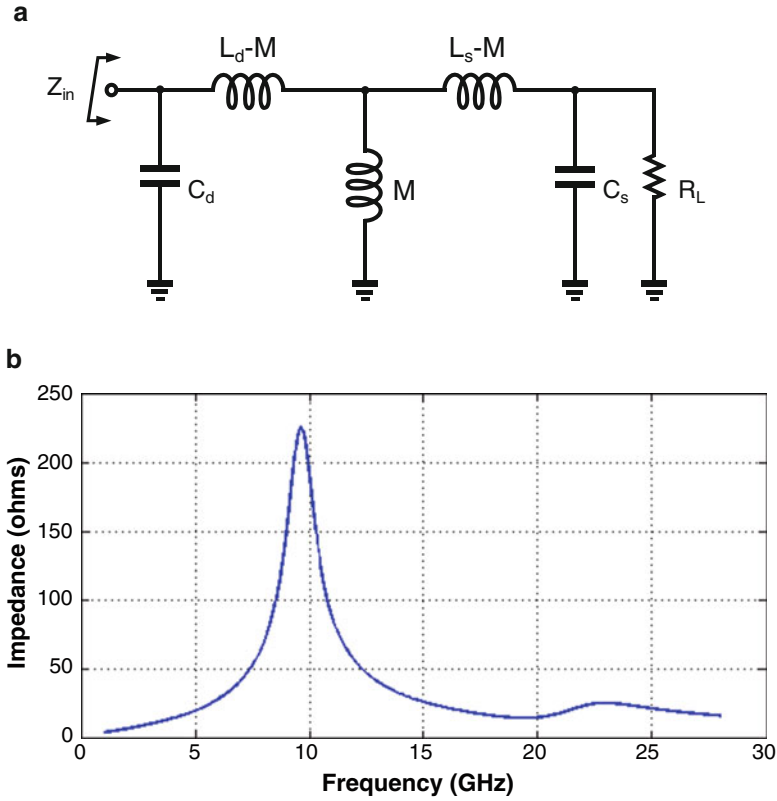
Fig. 8.7 (**a**) T-model for calculating the primary coil impedance Z_{in} of the integrated transformer in the TF-ILFD; (**b**) typical impedance plot of Z_{in} with $R_L = 100\,\Omega$ ($N = 4$)

If quadrature outputs are needed, two TF-ILFDs with different input phases can be employed. To obtain the relationship between the phases of the input and output signals, $v_i(2\omega)$ and $v_o(\omega)$ are expressed as: $v_i(2\omega) = |v_i| \cos(2\omega t + \varphi_{in})$, and $v_o(\omega) = |v_o| \cos(\omega t + \varphi_{out})$. It follows that (8.1a) can be rewritten as:

$$i_{inj}(\omega) = \frac{k_1 \cdot |v_i| \cdot |v_o|}{2N} \cos(\omega t + \varphi_{in} - \varphi_{out}) \tag{8.3}$$

The phase difference β between $i_{inj}(\omega)$ and $v_o(\omega)$ is given by:

$$\beta = \varphi_{in} - 2\varphi_{out} \tag{8.4}$$

If the two TF-ILFDs are identical, then β will always be the same as long as the two dividers operate at the same input frequency. According to (8.4), it is clear that the output phase difference between the two TF-ILFDs will be exactly $\pi/2$ if the input
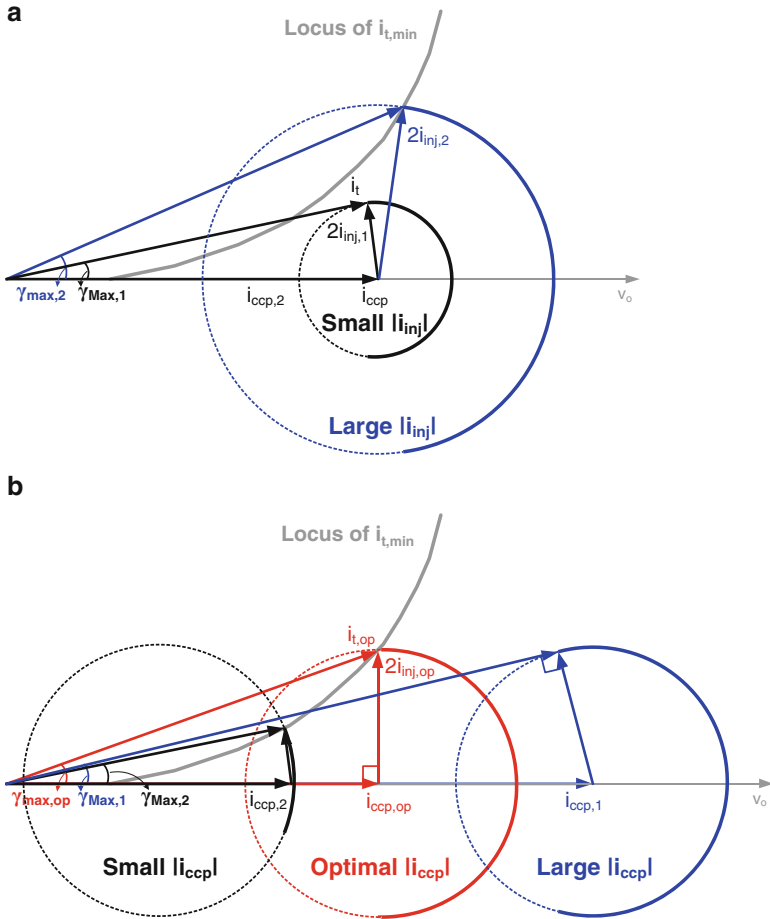
Fig. 8.8 Phase diagrams of the TF-ILFD: (**a**) for the same $|i_{ccp}|$ and (**b**) for the same $|i_{inj}|$

signals have a phase shift of π. The block diagram of the quadrature frequency divider employing two identical TF-ILFDs is shown in Fig. 8.9.

One drawback of the quadrature outputs generation scheme in Fig. 8.9 is that the IQ phase sequence at output of the TF-ILFDs (whether v_{Ao} leads or lags v_{Bo} by $\pi/2$) is not well determined since the phase difference between the two input signals could be either $-\pi$ or π. To realize a low-voltage divider with a deterministic IQ phase sequence, another transformer-based regenerative quadrature ILFD (TF-QILFD) topology as described in the next section can be used. Moreover, as will be explained later, the TF-QILFD can also achieve wider input locking range than the TF-ILFD.
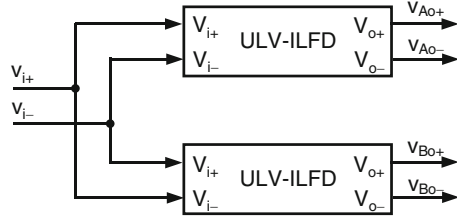
Transformer-Based Regenerative Quadrature ILFD

Figure 8.10 shows a simplified block diagram of the TF-QILFD topology. For intuitive understanding, it is constructed by one QVCO and two mixers with cross-coupled feedback loops. Similar to the operation in the TF-ILFD divider, the divide-by-2 function of the TF-QILFD is accomplished by injecting the output current from the double-balanced mixers into a QVCO, which forces it to oscillate at the frequency of $f_{in}/2$.

Figure 8.11 shows the detailed schematic of the TF-QILFD with quadrature outputs. The divider contains a TF-QVCO as presented in Sect. 5.3 and two double-balanced active mixers. The TF-QVCO is configured by two cross-coupled transistor pairs $M_{5/6}$ and $M_{11/12}$ and two integrated transformers. The two VCOs are cross-coupled by on-chip transformers, rather than active devices, to generate quadrature signals with better performance in terms of operation frequency, power, supply voltage, and phase noise. The primary coil L_d of each transformer resonates with the total capacitance at the drain and is simultaneously cross coupled to the secondary coil L_s for quadrature outputs. As such, the loading capacitance contributed by the coupling transistors in conventional QVCOs is removed, and the supply voltage can be lower because the transformer enables the signals at the sources to swing below the ground.

Two double-balanced active mixers, constructed by transistors M_{1-4} and M_{7-10} and transformers, are also configured in cross-coupled connection through the same transformers used in the QVCO. The second coil L_s of each of the transformer is placed at source terminal of the mixer to realize the second input. The first mixer's output signals are then coupled to the second input of the second mixer through the transformer to form the cross-coupled connections. Thanks to the transformer coupling for both the mixer and the VCO, the minimum necessary supply voltage of the TF-QILFD is significantly reduced.

Similar to the analysis performed for the TF-ILFD in Sect. 8.2.2, the left half-circuits of the TF-QILFD in Fig. 8.11 are modeled with two mixers and an equivalent LC tank as shown in Fig. 8.12, where the ideal transformer is assumed with a voltage transfer ratio of $N = \sqrt{L_p/L_s}$. The input transistors M_{1-4} are modeled with one double-balanced mixer (Mixer 2). The two inputs of the mixer are the input clock signal at the gate and the signal coupling to the source from the right half-circuits via transformer. On the other hand, the gate and source voltage signals of the cross-coupled pair $M_{5/6}$ appear in quadrature phases, which results in

Fig. 8.10 Simplified block diagram of the TF-QILFD
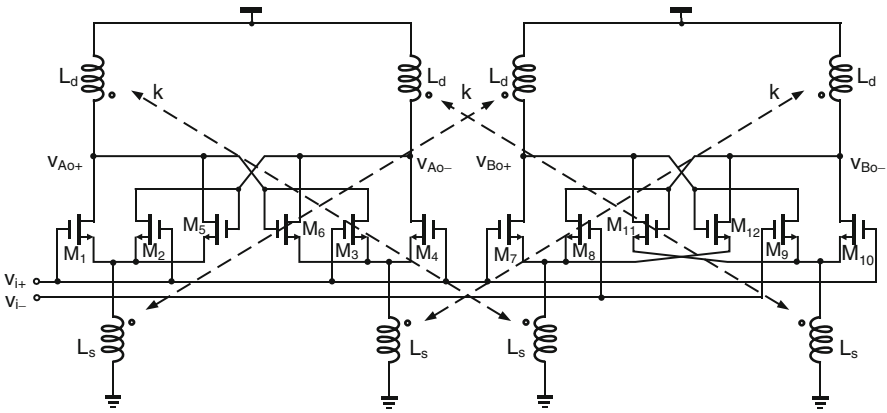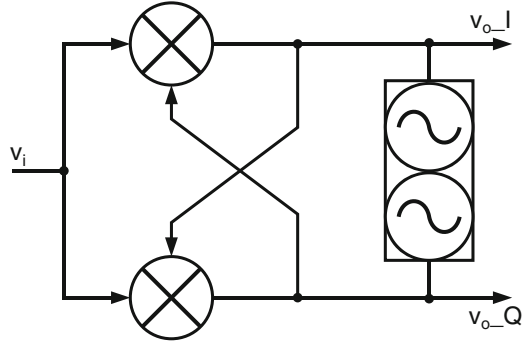
Fig. 8.11 Schematic of the TF-QILFD

two different feedback paths. The multiplier factor $e^{\pm j(\pi/2)}$ in the behavioral model represents a phase shift of either $\pi/2$ or $-\pi/2$ since the output signal $v_{Ao}(\omega)$ can either lead or lag the output signal $v_{Bo}(\omega)$ with $\pi/2$.

Figure 8.13 shows the phasor diagrams of the TF-QILFD when the output frequency ω is higher than the peak frequency ω_p of the tank. $\theta = \pm\arctan(1/N)$ represents the phase difference between $i_{ccp}(\omega)$ and $v_{Ao}(\omega)$, which is positive when $v_{Ao}(\omega)$ lags $v_{Bo}(\omega)$ and becomes negative when $v_{Ao}(\omega)$ leads $v_{Bo}(\omega)$. If ω is close to ω_p, γ becomes small, and either Case 1 ($v_{Ao}(\omega)$ lags $v_{Bo}(\omega)$ with the phasors in red color) or Case 2 ($v_{Ao}(\omega)$ leads $v_{Bo}(\omega)$ with the phasors in blue color) can satisfy both the phase and gain conditions and potentially make the divider function properly as shown in Fig. 8.13a. However, the divider would choose to oscillate in Case 1 since it provides a larger open-loop gain ($|i_{t,1}(\omega)| > |i_{t,2}(\omega)|$). On the other hand, if ω goes much higher than ω_p, γ becomes large, Case 2 would not provide enough phase shift γ to satisfy the loop phase condition as shown in Fig. 8.13b, and the divider can only function properly as Case 1. As a result, the phase sequence with $v_{Ao}(\omega)$ lagging $v_{Bo}(\omega)$ (Case 1) is well determined as long as $\omega > \omega_p$.
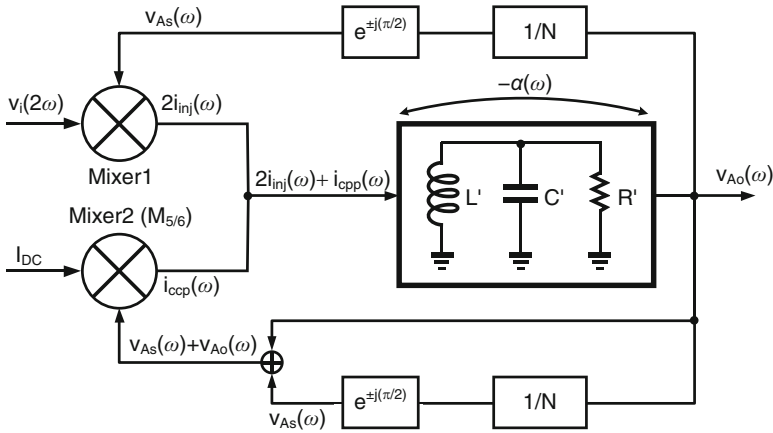
Fig. 8.12 Behavioral model of the TF-QILFD

When ω is lower than ω_p, the phase sequence would be swapped so that $v_{Ao}(\omega)$ will always lead $v_{Bo}(\omega)$ instead as shown in Fig. 8.14.

The TF-QILFD can also achieve wider locking range as compared to the TF-ILFD, since $i_{ccp}(\omega)$ as a combination of the currents from I and Q paths provides an additional phase shift θ, which helps increase the maximum phase shift γ_{max} provided by $i_t(\omega)$. However, if $|\theta|$ is larger than ϕ_0 which is defined as $\phi_0 = \arcsin\left(|2i_{inj}(\omega)|/|i_{ccp}(\omega)|\right)$, the divider would fail to function when $\gamma < \theta - \phi_0\left(\text{for } \omega > \omega_p\right)$ or $\gamma > -\theta + \phi_0\left(\text{for } \omega < \omega_p\right)$, as shown in Fig. 8.15. Consequently, ϕ_0 must be larger than $|\theta|$ to guarantee the continuous locking range, which can be achieved by properly sizing the W/L ratios of M_{1-4} (M_{7-10}) and M_5/M_6 (M_{11}/M_{12}).

8.2.3   Experimental Results

Both the TF-ILFD and TF-QILFD are designed and fabricated in a 0.18-μm CMOS process with six metal layers. Figure 8.16a shows the chip micrograph of quadrature divider employing two identical TF-ILFDs (Fig. 8.4), and Fig. 8.16b shows the chip micrograph of the TF-QILFD (Fig. 8.11). Both dividers occupy the same core area of 0.3 mm^2. And a single-sideband (SSB) mixer as shown in Fig. 5.27 is included to test the IQ imbalance. Two 4-port differential center-tap transformers with the same structure as that used in the TC-QVCO (Fig. 5.26) are designed and implemented in both designs. The single-turn secondary coil L_s of transformer is laid out to be completely inside the two-turn primary coil L_d. The self-inductances
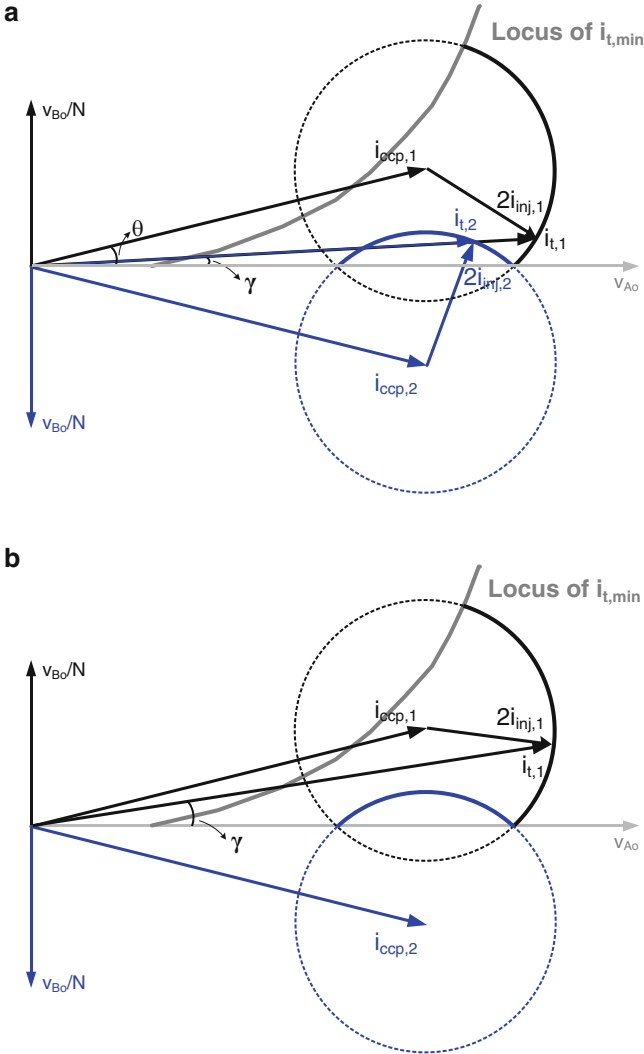
Fig. 8.13 Phasor diagrams of the TF-QILFD when the output frequency $\omega > \omega_p$ with: (**a**) small γ and (**b**) large γ

of the primary and secondary coils are measured to be 465 pH and 147 pH, respectively, with a coupling coefficient k of around 0.7.

At 0.5-V supply voltage, the single TF-ILFD consumes a total power from 2.75 to 4.35 mW across the whole locking range. An input frequency range from 16.1 to 20 GHz is measured with 3-bit switched-capacitors tuning, which corresponds to a tuning range of 21.6 % and is actually limited by the maximum frequency of the external power splitter used. Figure 8.17 shows the output spectrum of the TF-ILFD at the minimum and maximum input frequencies. In Fig. 8.18, the output power of
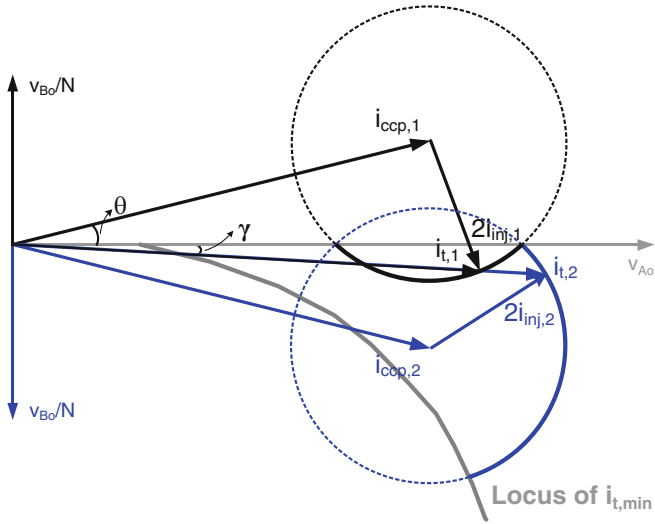
Fig. 8.14 Phasor diagram of the TF-QILFD when output frequency $\omega < \omega_p$
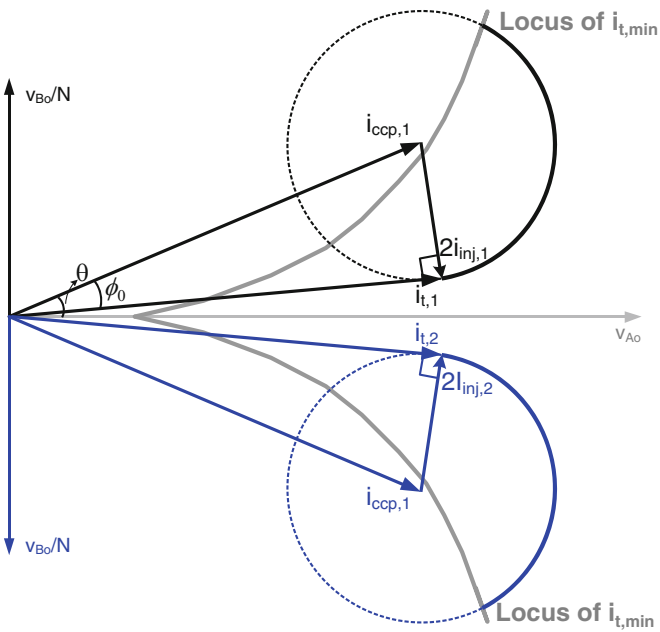
Fig. 8.15 Phasor diagram of the situation that the TF-QILFD fails to function when output frequency ω is close to ω_p
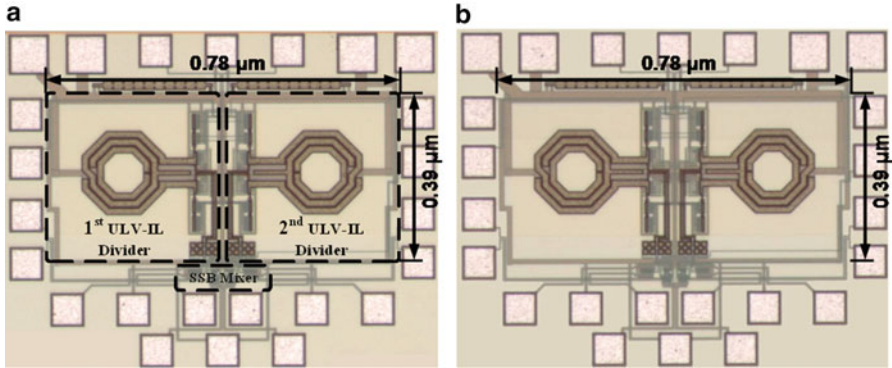
Fig. 8.16 Chip micrographs: (**a**) the quadrature frequency divider employing two identical TF-ILFDs and (**b**) the TF-QILFD

single TF-ILFD versus input frequency under different power consumptions is plotted. The power consumption is changed by changing the supply voltage from 0.5 to 0.7 V. The common DC input voltage of the input clock signal is biased at the corresponding supply voltage. When the power consumption is small, the locking range can be significantly increased with the increase of supply voltage and thus power consumption since the divider works in the GCL region. On the other hand, the locking range extension is no longer obvious when the power consumption is beyond 8 mW since the divider enters into the PCL region.

To verify the phase accuracy of the quadrature signals generated by two identical TF-ILFDs with antiphase inputs (Fig. 8.9), an on-chip SSB mixer is included to measure the SBR. Vector signal generator is used to generate the IQ baseband signals at 5 MHz. As shown in Fig. 8.19, SBR of >35 dB is measured, which corresponds to a phase mismatch of around 2° if amplitude mismatch is neglected.

Under a 0.6-V supply, the TF-QILFD consumes a total power from 11.4 to 13.6 mW across the whole locking range. An input frequency range from 15.1 to 20 GHz is measured with 3-bit switched-capacitors tuning, which corresponds to a locking range of 27.8 % and is actually limited by the maximum frequency of the external balun used for testing. Figure 8.20a, b shows the output spectrums of the TF-QILFD at the minimum and maximum input frequencies, respectively. The measured output power versus the input frequency is plotted in Fig. 8.21. The two discontinuous regions in the locking range plot when the switched-capacitor setting is fixed is because that the divider fails to work properly around the peak frequency ω_p of the tank due to the reason that has been explained in Sect. 8.2.2. To cover all the frequency gaps and achieve a continuous and wide locking range, a 3-bit SCA was included and tuned to vary the peak frequency ω_p of the tank in this design. The TF-QILFD has the same device sizes as those in the TF-ILFD. However, the minimum required supply voltage for the TF-QILFD is around 100 mV higher than the TF-ILFD, which is limited by the reduced open-loop gain. In the TF-ILFD divider, both the feedback paths through the transformer and through the
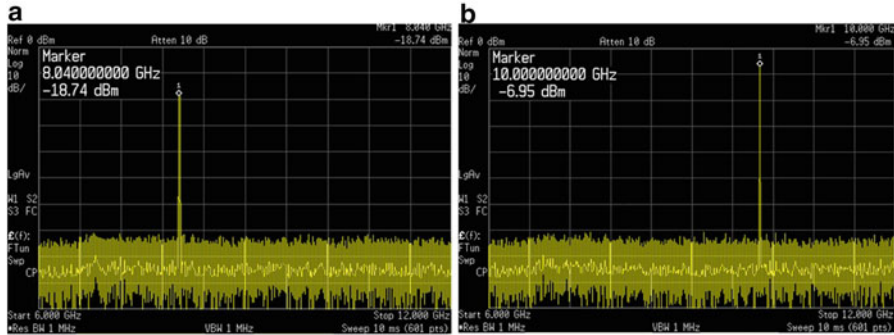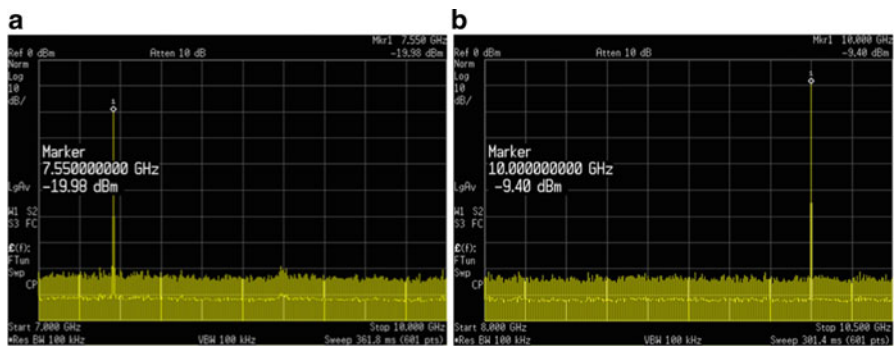
Fig. 8.17 Measured output spectrum of the TF-ILFD at (**a**) the minimum input frequency of 16.2 GHz and (**b**) the maximum input frequency of 20 GHz
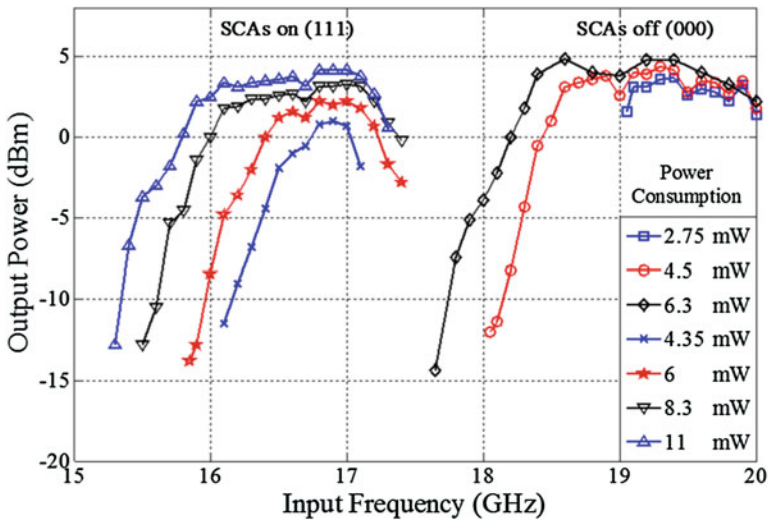

**Fig. 8.18** Measured output power of the single TF-ILFD as a function of input frequency

cross-coupled pair contribute to the open-loop gain of the divider. In contrast, in the TF-QILFD, the transformer-coupled loop is utilized to form the required quadrature loop. As a consequence, the TF-QILFD has a smaller open-loop gain and thus requires a higher minimum supply voltage.

A SBR of 31 dB is measured for the TF-QILFD as shown in Fig. 8.22, which corresponds to a phase mismatch of around 3.2° if amplitude mismatch is neglected. As plotted in Fig. 8.23, the SBR and thus the IQ phase accuracy of the TF-QILFD
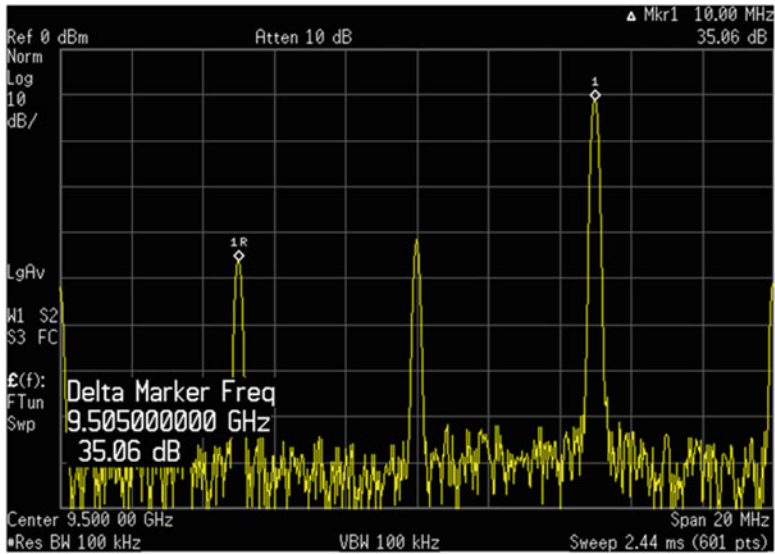
Fig. 8.19 Measured sideband-rejection ratio of two identical TF-ILFDs with quadrature outputs

Fig. 8.20 Measured output spectrums of the TF-QILFD at: (**a**) the minimum input frequency of 15.1 GHz and (**b**) the maximum input frequency of 20 GHz
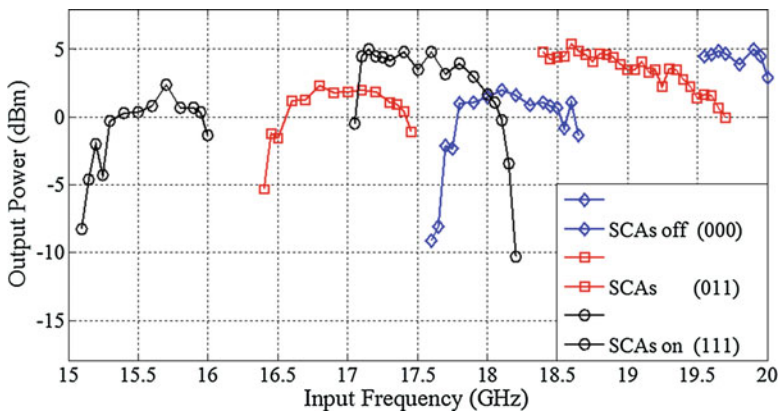
Fig. 8.21 Measured output power of the TF-QILFD as a function of input frequency
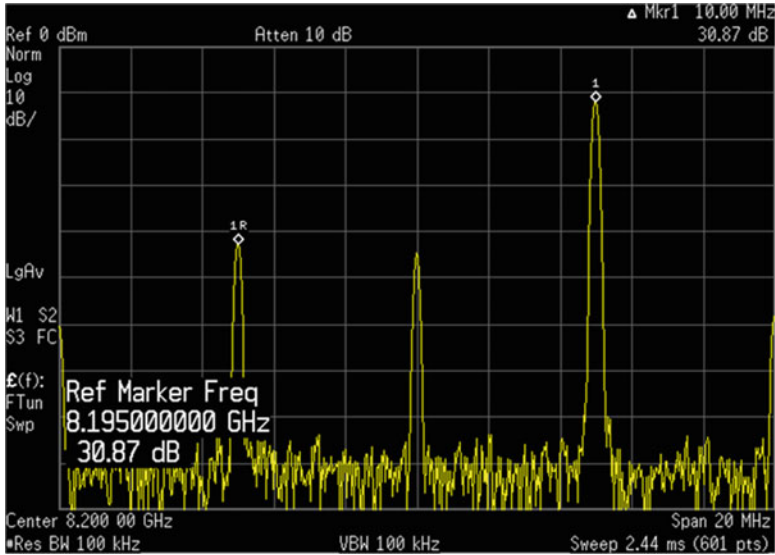
Fig. 8.22   Measured sideband-rejection ratio of the TF-QILFD
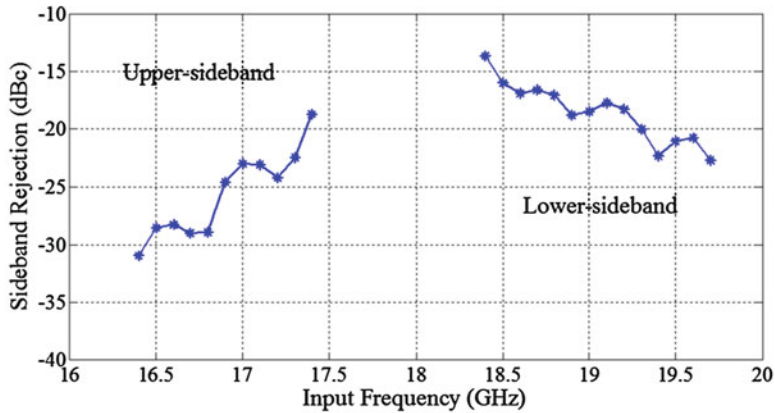
Fig. 8.23   Measured SBR of the TF-QILFD as a function of input frequency

are degraded for output frequencies close to the peak frequency of the tank, at which the coupling from the corresponding quadrature phase becomes weak. As expected, the SSB mixer's output is changed from the upper sideband to the lower sideband when the divider's input frequency is swept from lower to higher as compared to twice of the peak frequency ω_p of the tank.

8.3 Self-Frequency-Tracking ILFD

8.3.1 Locking Range Limitation of the Conventional Direct-Injection ILFDs

As discussed in Sect. 4.3, the locking range of the ILFD can be analyzed based on the phasor diagram. When the conventional direct-injection ILFD works in the PCL region as shown in Fig. 8.24a, the maximum locking range is decided by the maximum phase shift γ between the total current $i_t(\omega)$ injected to the tank and the output voltage $v_o(\omega)$, which can always be increased by increasing $i_{inj}(\omega)$ and $i_0(\omega)$ if the bias current I_{DC} is kept constant. Since $i_{inj}(\omega)$ and $i_0(\omega)$ are the outputs of the same mixer M_{in}, they both increase with the increasing of the transistor size W/L or V_{gs} of M_{in} as long as it stays in the saturation region.

With the increasing of $i_0(\omega)$, the circle of the injection current moves toward the left and finally intersects with the locus of the minimal $i_t(\omega)$ that guarantees the gain condition. Afterwards, the divider enters into the GCL region as shown in Fig. 8.24b. In this region, the locking range no longer depends on the maximum phase γ shift but is restricted by the amplitude of $i_t(\omega)$ that can still maintain oscillation. As shown in Fig. 8.25a, the maximum locking range under a certain I_{DC} is achieved when the phasor $i_{inj}(\omega)$ is vertical to the phasor $i_0(\omega)$ or $v_o(\omega)$, which can be achieved by an optimal combination of V_{gs} and W/L of M_{in}. The only way to further boost the locking range is to increase the $|i_{inj}(\omega)|$. However, $|i_0(\omega)|$ would also be increased since it comes from the same mixer M_{in}, which makes the circle of the injection current move further toward the left and in turn degrades the locking range. Consequently, the bias current I_{DC} needs to be increased at the same time to increase the $|i_{ccp}(\omega)|$ so that the circle of the injection current would move back toward the right to keep $i_{inj}(\omega)$ vertical to $i_0(\omega)$ as shown in Fig. 8.25b. However, a large I_{DC} would result in large power consumption. Moreover, V_{gs} and W/L of M_{in} cannot be increased unlimitedly. Large V_{gs} would eventually push M_{in} into the triode region, which in turn degrades the effective g_m and thus $|i_{inj}(\omega)|$, while large
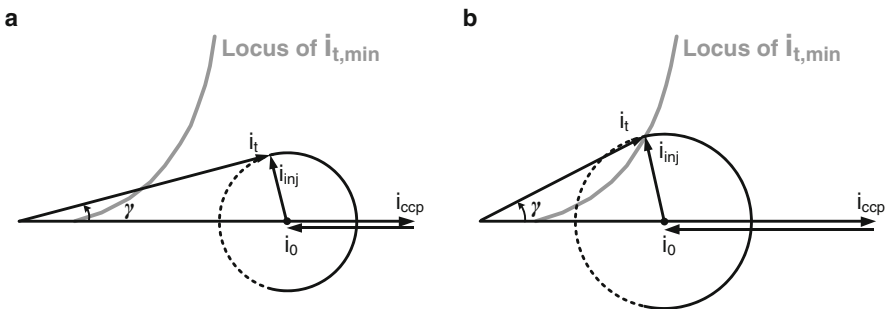
Fig. 8.24 Phasor diagram of the conventional LC tank-based direct-injection ILFD in: (**a**) the PCL region and (**b**) the GCL region
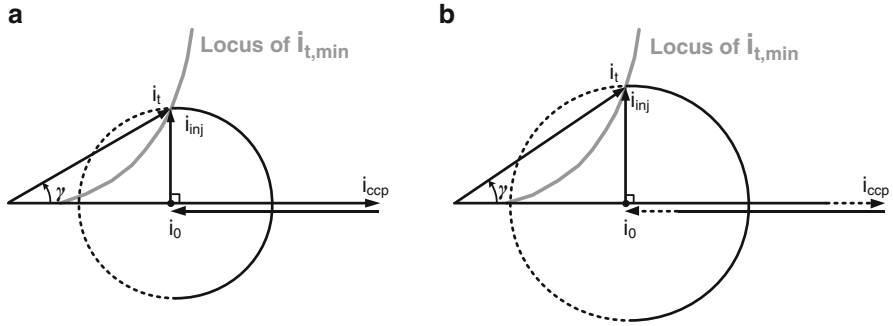
Fig. 8.25 Maximum locking range of the conventional LC tank-based direct-injection ILFD in the GCL region with (**a**) a small I_{DC} and (**b**) a large I_{DC}

W/L would add a large parasitic capacitance to the output nodes, which degrades the maximum operating frequency of the divider.

8.3.2   Self-Frequency-Tracking ILFD

To extend the locking of the ILFD while still maintaining low-power consumption, the self-frequency-tracking ILFD (SFT-ILFD) based on a transformer tank is shown in Fig. 8.26 [10]. Instead of being directly injected to the LC tank from the output nodes (v_{o+} and v_{o-}), the output currents of the mixer M_{in} are injected through the nodes (v_{s+} and v_{s-}) at the secondary coils (L_2 and L_4) of the transformer, while the negative g_m cell is connected to the primary coils (L_1 and L_3). The capacitors C_1 and C_3 represent the total capacitance at the primary coil (including the loading capacitance of the output buffer and the parasitic capacitance from $M_{1/2}$ and interconnecting wires), while the capacitors C_2 and C_4 represent the total capacitance at the secondary coil (including the parasitic capacitance of M_{in} and interconnecting wires).

The two injected currents $i_0(\omega)$ and $i_{inj}(\omega)$ generated by M_{in} can be modeled as two admittances Y_0 and Y_{inj} which is defined as below:

$$Y_0 = \frac{i_0(\omega)}{v_{S+}(\omega)} = K_1 \cdot \left(V_{gs} - V_{th}\right) = |Y_0| \tag{8.5a}$$

$$Y_{inj} = \frac{i_{inj}(\omega)}{v_{S+}(\omega)} = K_2 \cdot \left|v_{inj}(2\omega)\right| \cdot e^{j\varphi} = \left|Y_{inj}\right| \cdot e^{j\varphi} \tag{8.5b}$$

where K_1 and K_2 are the conversion gains and V_{th} is the threshold voltage of the M_{in}. In this way, the mixer M_{in} can be modeled as a two-terminal device for a given input signal $V_{in} = V_{gs} + v_{inj}(2\omega)$ as shown in Fig. 8.27. Since $i_0(\omega)$ is always in phase with $v_{s+}(\omega)$, Y_0 only contains a real part. On the other hand, Y_{inj} is a complex

Fig. 8.26 Schematic of the SFT-ILFD
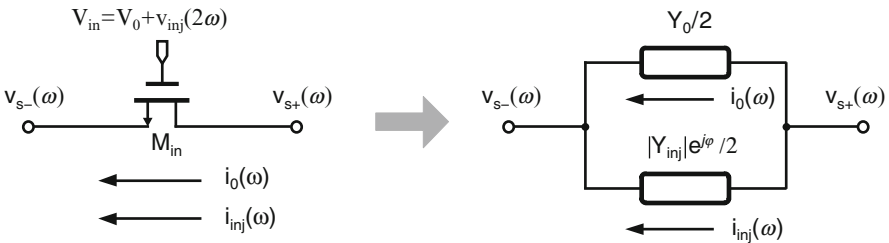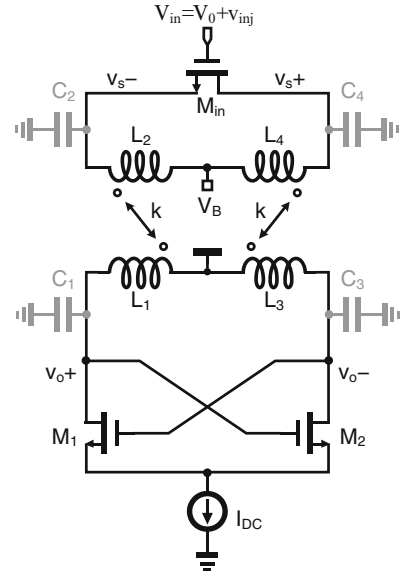
Fig. 8.27 Equivalent admittance model of the mixer M_{in}

admittance because the phase difference φ between $i_{inj}(\omega)$ and $v_{s+}(\omega)$ changes with the input frequency. Moreover, according to (8.5a) and (8.5b), $|Y_0|$ and $|Y_{inj}|$ depend on K_1 and K_2 and thus are well controlled by the input DC bias V_{gs}, the input power, and the amplitude of $v_{s+}(\omega)$.

To calculate the impedance seen from the output node, the equivalent circuits as shown in Fig. 8.28a are used. Due to the symmetrical property of the differential topology, the half-circuit is considered for simplicity, in which M_{in} is replaced with the admittances Y_0 and Y_{inj}. By replacing the transformer with its equivalent T-model, the tank impedance is simplified as shown in Fig. 8.28b. Here, the circuit can be regarded as having the two currents $i_0'(\omega)$ and $i_{inj}'(\omega)$ directly injected into a simple LC tank with the inductance L_1 and the capacitance $C_1 + k^2(L_2/L_1)C_2$. The corresponding equivalent admittances Y_0' and Y_{inj}' can be expressed as:
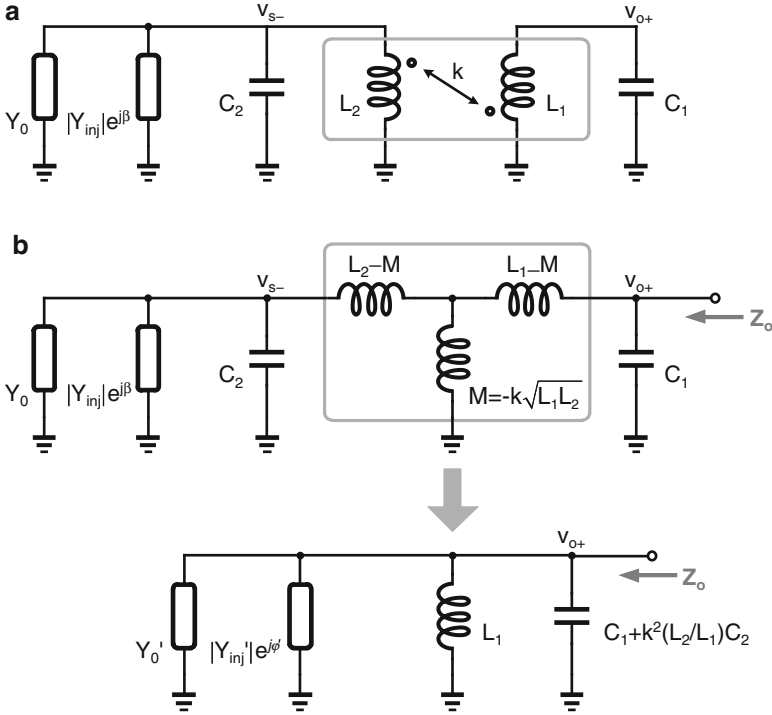
Fig. 8.28 (**a**) Equivalent circuits of the transformer tank with injection, (**b**) equivalent tank impedance Z_o seen from the output node

$$Y_0' = n \cdot \left\{ Y_0 + j\left[a(1-a)\omega C_2 - \frac{a(1+a)\left(Y_1^2 - Y_2^2\right)}{\omega C_2}\right]\right\} \qquad (8.6a)$$

$$Y_{\text{inj}}' = n \cdot \left|Y_{\text{inj}}\right| \cdot e^{j\varphi'} \qquad (8.6b)$$

where ω is the output frequency; parameters a and n are given as below:

$$a = \omega^2 L_2 C_2\left(1 - k^2\right) \qquad (8.7a)$$

$$n = \frac{k^2}{\left(\frac{a}{\omega C_2}\right)^2\left(Y_1^2 - Y_2^2\right) + (1-a)^2} \cdot \left(\frac{L_2}{L_1}\right) \qquad (8.7b)$$

According to (8.6a), now Y_0' contains both the real and imaginary parts, which indicates that $i_0'(\omega)$ is no longer in phase with $v_{o+}(\omega)$. In addition, a phase shift θ has been created by the transformer tank between $i_0'(\omega)$ and $v_{o+}(\omega)$ or $-i_{ccp}'(\omega)$ as shown in Fig. 8.29a, which can be expressed as:

Fig. 8.29 Phasor diagrams of the SFT-ILFD: (**a**) at ω_1 and (**b**) at ω_2 (where $\omega_2 > \omega_1 > \omega_0$)
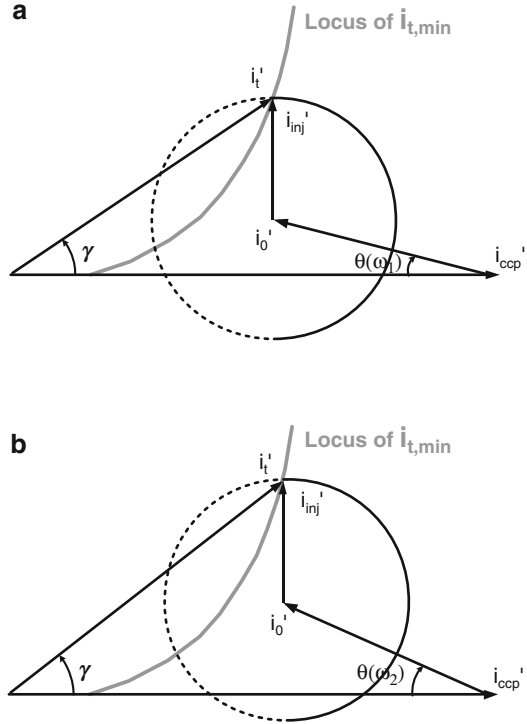
$$\theta = arctg\left[\frac{\frac{a(1+a)\left(Y_0^2 - Y_{inj}^2\right)}{\omega C_2} - a(1-a)\omega C_2}{Y_0}\right] \qquad (8.8)$$

Figure 8.30 plots the phase shift θ as a function of frequency for different C_2 values. It is important to note that θ is increased with frequency. From the phasor diagrams shown in Fig. 8.29b, this self-frequency-tracking property of θ helps increase the locking range even when $|i_{inj}'(\omega)|$ and $|i_{ccp}'(\omega)|$ are kept the same as long as the output frequency ω is larger than the self-oscillation frequency ω_0 of the divider because a larger θ increases the maximum phase shift γ between $i_t'(\omega)$ and $i_{ccp}'(\omega)$ when the input frequency increases.

When the output frequency ω is smaller than ω_0, the locking range is actually degraded as shown in Fig. 8.31. However, θ changes only a little due to its frequency-dependent property, and the degradation of the locking range becomes negligibly small. As a result, the total locking range is still enhanced but shift to higher frequencies.

Usually, it is difficult to increase $|i_{inj}'(\omega)|$ to boost the locking range because both the input voltage swing and the conversion gain of the mixer M_{in} are significantly degraded at high frequencies. Moreover, even if it is possible to increase $|i_{inj}'(\omega)|$,

Fig. 8.30 The phase shift θ as a function of frequency for different C_2 values ($L_2 = 460$ pH, k = 0.65, $|Y_0| = 10$ mS, and $|Y_{inj}| = 5$ mS)
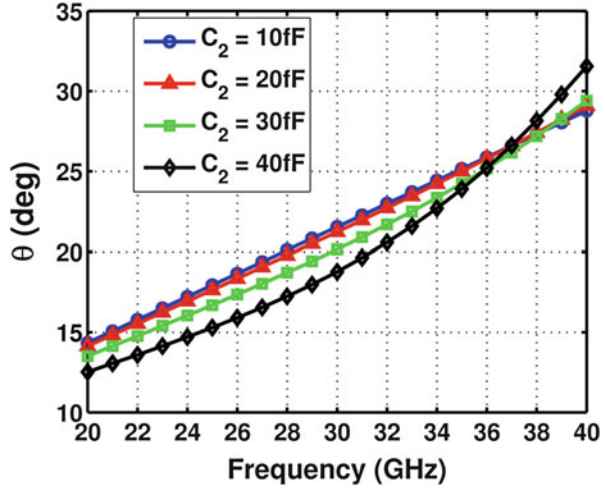
Fig. 8.31 Phasor diagram of the SFT-ILFD at frequency $\omega_3 < \omega_0$
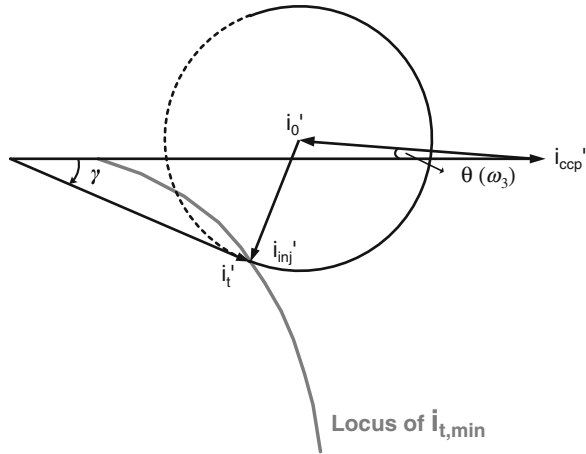

$|i_{ccp}'(\omega)|$ and thus the current consumption are also required to be increased to achieve the optimal condition for the maximum locking range as discussed in Sect. 8.3.1. In contrast, by exploiting the frequency-dependent phase shift θ, the self-frequency tracking technique can boost the locking range without the need of increasing $|i_{inj}'(\omega)|$ and $|i_{ccp}'(\omega)|$. As shown in Fig. 8.30, increasing C_2 also helps increase θ at the high-frequency end. However, since the equivalent tank capacitance $C_1 + k^2(L_2/L_1)C_2$ also increases as shown in Fig. 8.28b, the self-oscillation frequency of the divider would drop. In this design, C_2 is the parasitic capacitance and is estimated to be around 20 fF.

Moreover, in the conventional ILFDs, an AC coupling capacitor is needed between the VCO's output and the ILFD's input to obtain the optimal bias condition ($V_{gs} = V_{DC} - V_{DD}$) of M_{in} since the source and drain voltages of M_{in} are fixed to V_{DD}.
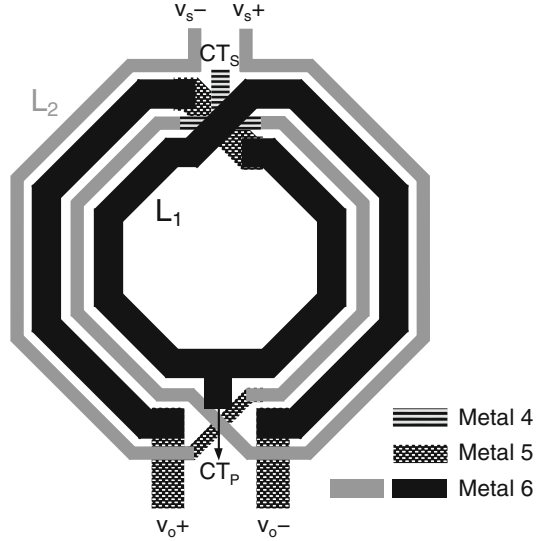
At mm-Wave frequencies, the use of AC coupling capacitor adds parasitic capacitance and degrades the input signal swing, which in turn limits the locking range. In the SFT-ILFD as shown in Fig. 8.26, since the currents are injected through the secondary coil instead of directly into the output nodes as in the conventional ILFD, the source and drain of M_{in} can be biased independently ($V_{gs} = V_{DC} - V_B$), which eliminates the lossy AC coupling capacitor needed in the conventional ILFDs.

Figure 8.32 shows the layout of the four-port differential transformer. Both the primary and secondary coils are implemented by using the top metal (Metal 6) to maximize their quality factors (Qs). The input ports of the two coils are placed in the opposite direction to reduce the coupling capacitance. From the electromagnetic simulation, the inductance of the primary coil ($L_1 + L_3$) and the secondary coil ($L_2 + L_4$) are 680 pH and 920 pH, respectively. From EM simulation, at 30 GHz, the Qs of the primary and secondary coils are 17 and 10, respectively. The coupling coefficient k is around 0.65.

8.3.3 Experimental Results

To verify the effectiveness of the SFT technique, an SFT-ILFD prototype is fabricated in a 65-nm 1P6M LP CMOS process. Figure 8.33 shows the chip micrograph of the SFT-ILFD with a core area of 0.023 mm^2. The size of mixer M_{in} is 13 μm/0.06 μm with 1 μm finger width. The odd finger number is used to keep the parasitic capacitance of the drain and the source symmetrical.

Fig. 8.33 Chip micrograph
of the SFT-ILFD
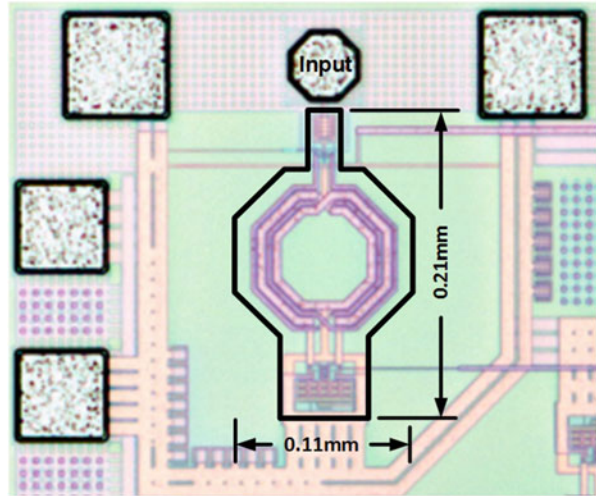
Fig. 8.34 Measurement
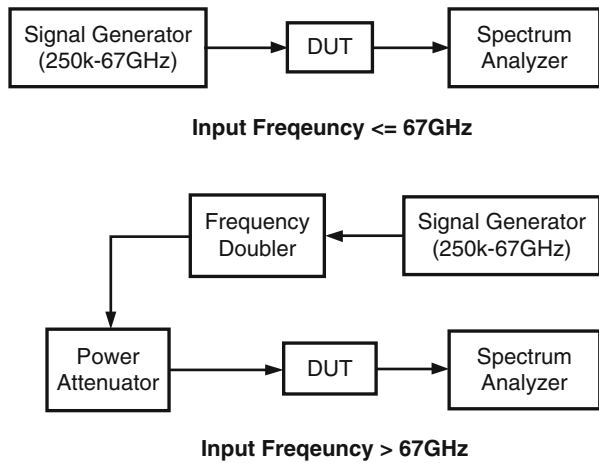set-ups for different input
frequency ranges

Figure 8.34 shows the measurement set-ups. Since the signal generator available
to us can only provide a maximum output frequency of 67 GHz, it is directly
connected to the SFT-ILFD for testing with the input frequency lower than 67 GHz.
For the input frequency higher than 67 GHz, a frequency doubler is employed. A
power attenuator is used after the frequency doubler to adjust the input power
because the output power from the frequency doubler is fixed.

The measured input sensitivity curve is shown in Fig. 8.35. Consuming 1.9 mW
from a 0.8-V supply, the input locking range with 0-dBm input power is measured
to be 18.3 GHz or 29 % from 53.7 to 72.0 GHz at an optimal V_{gs} of 0.75 V, which is
large with sufficient margins to cover the 9-GHz bandwidth required by typical

Fig. 8.35 Measured input sensitivity curve of the SFT-ILFD
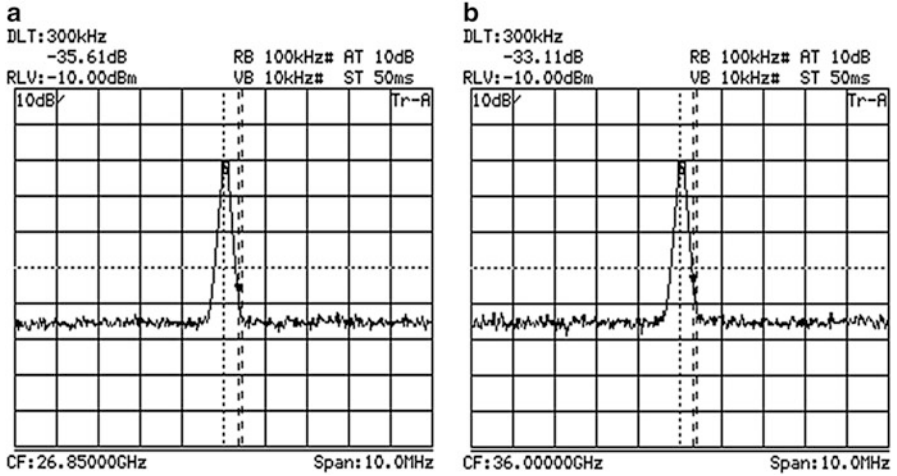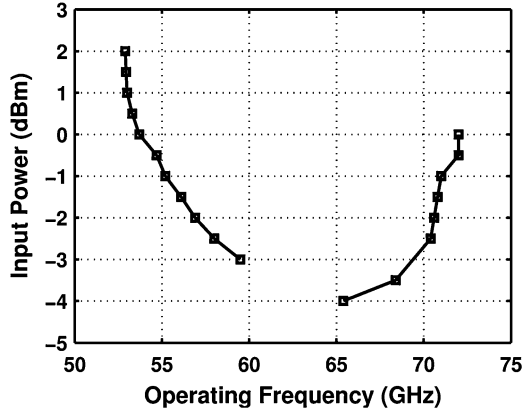
Fig. 8.36 Measured output spectrums at (**a**) the minimum input frequency of 53.7 GHz and (**b**) the maximum input frequency of 72 GHz

mm-Wave applications at 60 GHz. Figure 8.36 shows the measured ILFD's output spectrums at both the lowest and the highest input frequencies.

Figure 8.37 shows the measured locking range as a function of the current consumption I_{DC}. When I_{DC} is increased to 5 mA, the locking range can be further increased from 18.3 to 24 GHz. Finally, Table 8.1 summarizes and compares the measured performance of the SFT-ILFD prototype with that of the recently reported state-of-art low-power wide locking range mm-Wave ILFDs. Thanks to the frequency-tracking technique, the SFT-ILFD achieves an ultrawide locking range while still consuming a low power, which results in an excellent FoM of 9.53, as defined in (4.9). Furthermore, the use of a single four-port differential transformer tank helps maintain a compact chip area.

Fig. 8.37 Measured
locking range as a function
of current consumption
($V_{DD} = 0.8$ V,
$V_{GS} = 0.75$ V)
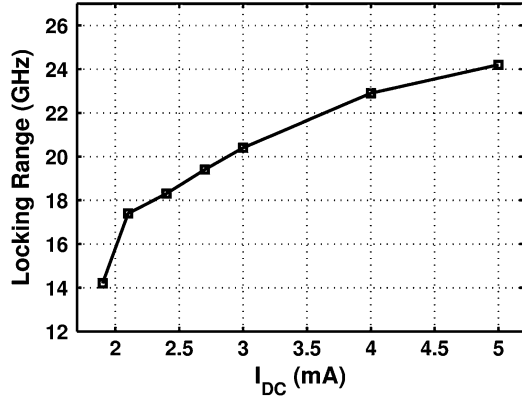
Table 8.1 Performance summary and comparison

Reference	CMOS technology	Input power (dBm)	Input freq. (GHz)	Locking range (GHz)	Power (mW) @ V_{DD} (V)	FOM	Area (mm^2)
[1]	90-nm	0	85.2~96.2	11 (12.2 %)	3.5 @ 1.2	3.14	0.336[a]
[2]	90-nm	0	53.4~60.8	7.4 (13 %)	2.5 @ N/A[b]	3	0.015
[3]	65-nm	−5	128.34~137	8.76 (6.6 %)	5.5 @ 1.1	1.6	0.05
[4]	65-nm	<−5	104~112.8	8.8 (8.14 %)	7.2 @ 1.2	1.22	0.144
[5]	65-nm	<−2	107.9~128.8[a]	20.9 (17.7 %)	6.27 @ 1.1	3.341	0.0544
[6]	0.13-μm	0	49.8~62.0	12.2 (21.8 %)	10.8 @ 0.9	2.02	0.324[a]
[7]	65-nm	0	48.5~62.9	14.4 (25.9 %)	1.65 @ 1.0	8.73	0.0157
[11]	0.13-μm	0	56.7~71.6	14.9 (23.2 %)	5.0 @ 0.8	2.98	0.007
[12]	65-nm	0	53.4~79.4	26 (39.2 %)	2.9 @ 0.8	8.97	0.126
[13]	0.13-μm	0	59.6~67	7.4 (11.7 %)	1.6 @ 0.8	4.63	0.0165
[14]	90-nm	0	52.7~64.8	12.1 (20.5 %)	8.6 @ 1.2[b]	1.4	0.0828
[15]	65-nm	0	57.2~67	9.7 (15.6 %)	1 @ 1.0	9.7	0.013
[16]	65-nm	0	58~77.8	19.8 (29.2 %)	1.44 @ 1.2	13.75	0.013
This work	65-nm	0	53.7~72	18.3 (29 %)	1.9 @ 0.8	9.53	0.023

[a]Area including PADs
[b]Quadrature outputs

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Chapter 9
Conclusion

In conclusion, as elaborated in Chaps. 5–8, integrated transformers are demonstrated to be very useful in VCOs and ILFDs mainly because they help to either reduce the supply voltage by breaking the output amplitude limitation due to supply and ground potentials or increase the frequency tuning/locking range by creating multiple bands as compared to the designs using on-chip inductors.

Several useful design techniques were described in this book in which integrated transformers are exploited to improve the performance of VCOs and ILFDs in terms of supply voltage, power consumption, phase noise, operation frequency, or frequency tuning/locking range, corresponding to state-of-the-art FoM's and FoM$_T$'s. More specifically, detailed transformer-based designs were presented with high performance demonstrated for TF-VCOs and a TC-QVCO in Chap. 5, a dual-mode QVCO in Chap. 6, a MT-VCO in Chap. 7, and low-voltage TF-ILFD and TF-QILFD and a wideband SFT-ILFD in Chap. 8.

For comprehensive comparison, the FoM's as a function of supply voltage and the FoM$_T$'s as a function of the oscillation frequency of the state-of-art CMOS LC-VCOs with oscillation frequencies below 20 GHz are summarized and plotted in Figs. 9.1 and 9.2, respectively, while the FoM$_T$'s of the state-of-art CMOS mm-Wave LC-VCOs are plotted in Fig. 9.3.

Although designed in a relatively old 0.18-μm CMOS technology in which the transistors' threshold voltages are as large as 0.5 V, the TF-VCOs described in Chap. 5 achieve an FoM of 190 dBc/Hz at 0.35-V supply using PMOS cross-coupled pair and a FoM of 193 dBc/Hz at 0.5-V supply using NMOS cross-coupled pair. For the supply voltage equal or lower than 0.5 V, only [9, 14] achieve better FoM's, which are both implemented in more advanced CMOS technologies. The enhanced-swing differential Colpitts (ESDC) topology in [9] requires two separate inductors, which generally would occupy larger chip area than a single transformer. Besides, the ESDC-VCO only demonstrates a narrow tuning range of 2.5 % corresponding to an FoM$_T$ lower than that of the TF-VCO as shown in Fig. 9.2. For the class-D VCO in [14], the advanced CMOS technology is a necessity since the turn-on resistance of the cross-coupled transistors needs to be even smaller than
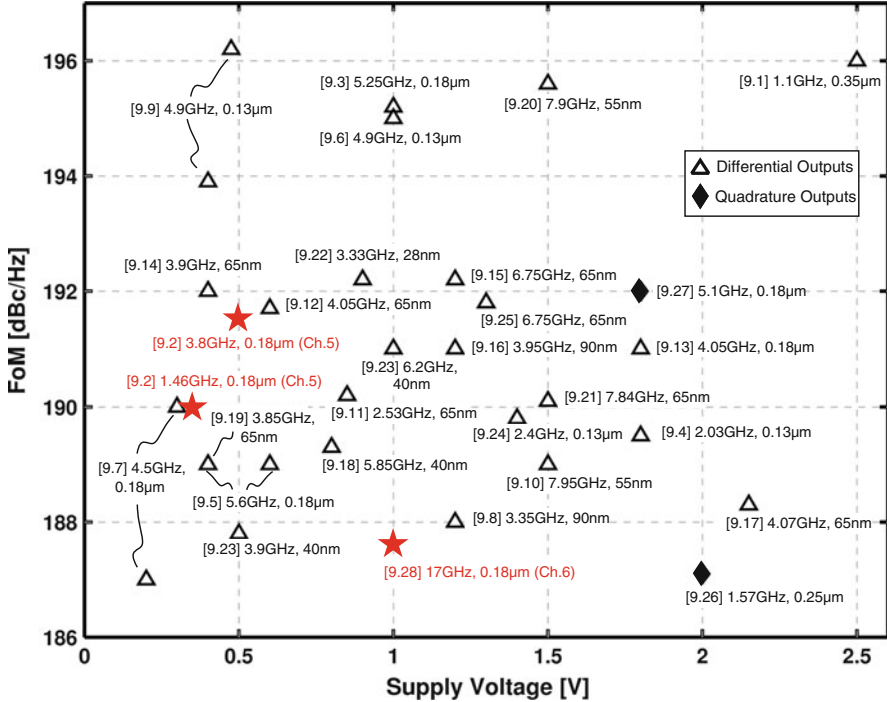
Fig. 9.1 FoM's as a function of supply voltage for state-of-art CMOS VCOs ([reference] center oscillation frequency, CMOS technology)

the series resistance of the inductor to prevent the degradation of phase noise. If implemented in a more advanced technology with lower threshold voltage and less parasitic capacitance of the switches in the SCA, the TF-VCO should be able to achieve a larger tuning range at an even lower supply voltage.

The TC-QVCO proposed in Chap. 5 achieves a high oscillation frequency of 17 GHz and an FoM of 187.6 dBc/Hz at a low supply voltage of 1 V. Although the SHC-QVCO in [20] achieves a much better FoM, it requires a much higher supply voltage of 1.8 V.

Implemented in a 0.13-μm CMOS technology, the transformer-based dual-mode VCO proposed in Chap. 6 achieves an FoM$_T$ of 203 in the low-band mode. As extension of the proposed principle, the triple-mode VCO in [27] based on a loosely coupled 3-coil transformer achieves a similar FoM$_T$ in a similar 0.13-μm CMOS technology. The VCOs in [12, 14, 16, 17] can achieve better FoM$_T$, but are all implemented in more advanced technologies including 65-nm and 40-nm CMOS processes in which the switch-capacitor array enjoys a larger C_{on}/C_{off} ratio when Q is kept same.

At the mm-Wave frequency around 60 GHz, the proposed MT-VCO in Chap. 7 can work in multiple modes with the help of a switched-shielded transformer, which greatly increases the frequency tuning range. As shown in Fig. 9.3, the
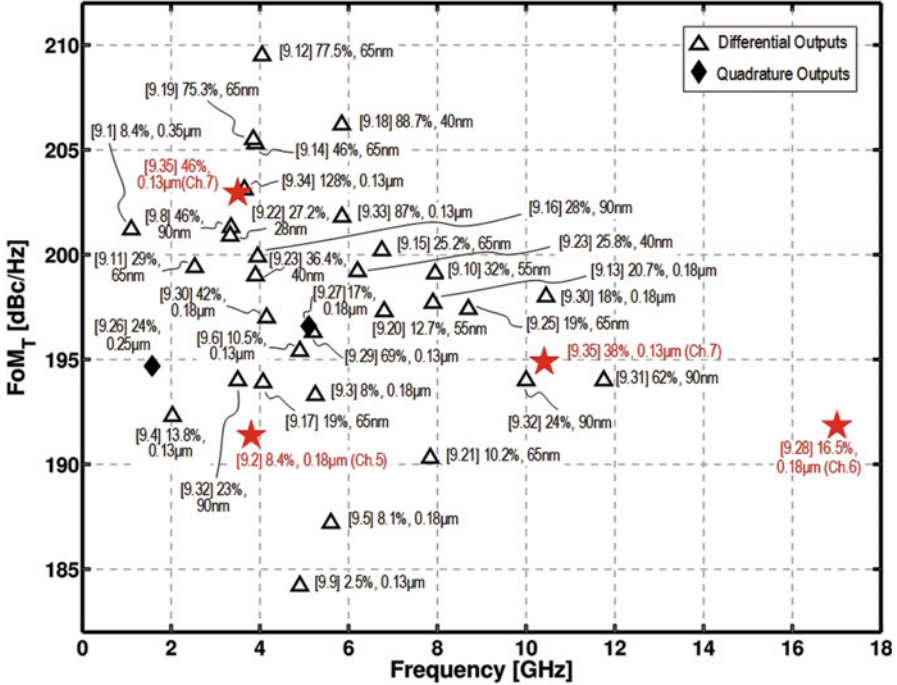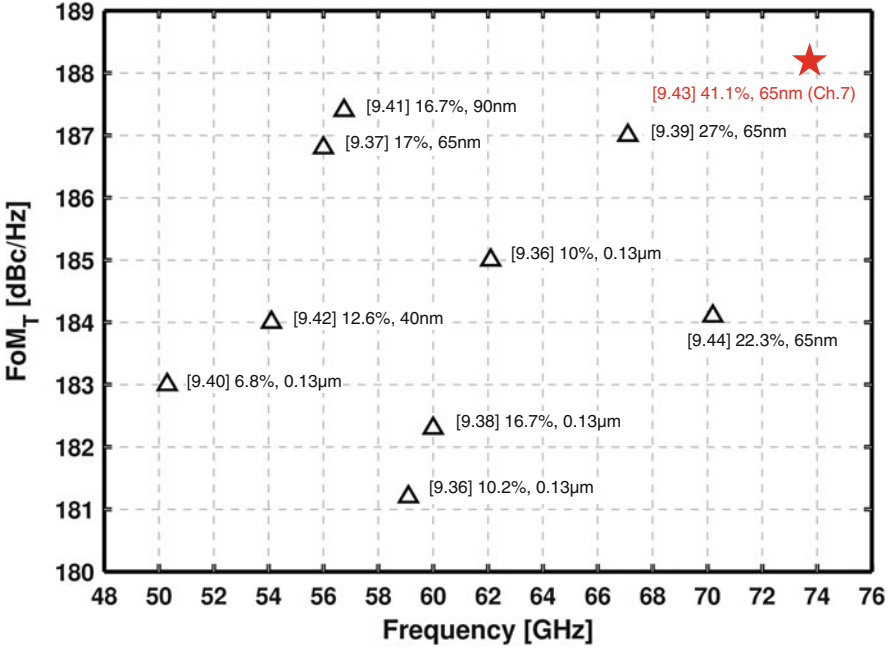
Fig. 9.2 FoM$_T$'s as a function of oscillation frequency for state-of-art wideband CMOS VCOs ([reference] frequency tuning range, CMOS technology)

MT-VCO achieves a highest average FoM$_T$ of 188.2 with a wide frequency tuning range of 41.1 %.

In Fig. 9.4, the state-of-art CMOS mm-Wave ILFDs are summarized, and their FoM's are plotted as a function of supply voltage. For applications that require low supply voltages, the TF-ILFD proposed in Chap. 8 can be a good candidate. Using a 0.18-μm CMOS technique, the TF-ILFD is demonstrated to operate at a supply voltage as low as 0.5 V. The relatively poor FoMs are due to the small absolute locking ranges in the unit of GHz. Actually, as shown in Fig. 9.4, the locking ranges in the unit of percentage of the two TF-ILFDs (21.6 and 27.9 %) are quite high. So if implemented in a more advanced technology, the TF-ILFD is expected to operate in a much higher frequency and thus achieve a much better absolute locking range and FoM at an even lower supply voltages.

The proposed SFT-ILFD in Chap. 8 features a self-frequency-tracking property by injecting the input signal through a transformer tank and achieves an FoM of 9.63, with a wide locking range of 29.1 % at a relative low supply voltage of 0.8 V. Although the ILFDs in [37, 54] achieve comparable and even higher FoMs, respectively, higher supply voltages of 1.0 and 1.2 V are required. Incidentally, both the ILFDs in [37, 54] are also based on transformer techniques.

Fig. 9.3 FoM$_T$'s as a function of oscillation frequency for state-of-art mm-Wave CMOS VCOs ([reference] frequency tuning range, CMOS technology)
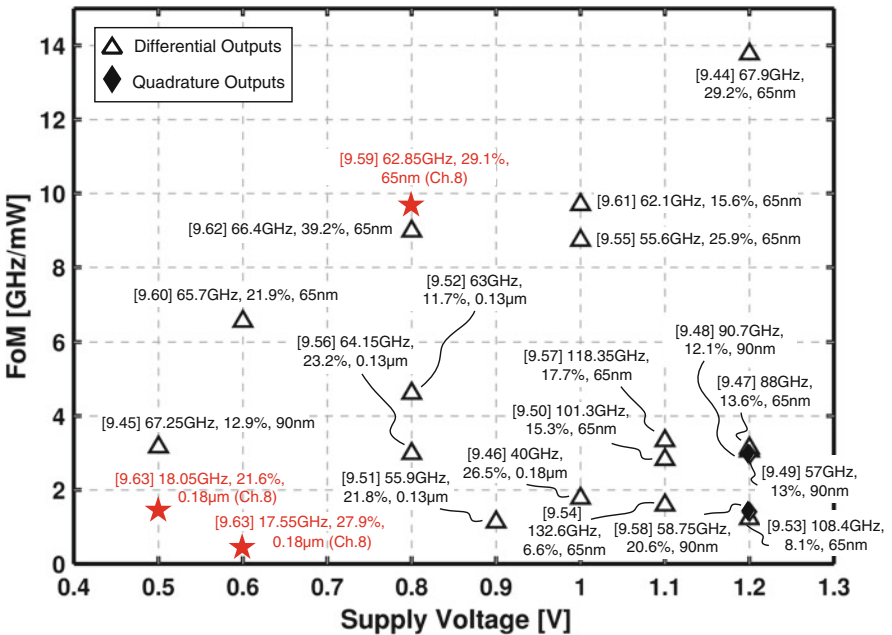
Fig. 9.4 FoM's as a function of supply voltage for state-of-art CMOS mm-Wave ILFDs ([reference] input center frequency, input locking range, CMOS technology)

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Appendix

A.1 Effective Turn Ratio for the TC-QVCO in Chap. 5

To calculate the voltages V_I and V_Q of the TC-QVCO as shown in Fig. 5.9 and obtain the effective turn ratio N_{eff} for an arbitrary coupling coefficient k value for the transformer, the equivalent circuit model in Fig. 5.10a can be used. Applying Kirchhoff voltage law, (5.10a) and (5.10b) can be modified as functions of k as:

$$V_I = g_m \left\{ \left[1 - \frac{X}{(N/k)^2} \right] V_I - \left[\frac{1+Y}{(N/k)} \right] V_Q \right\} \frac{1}{A_I(j\omega)} \tag{A.1a}$$

$$V_Q = g_m \left\{ \left[1 - \frac{X}{(N/k)^2} \right] V_Q - \left[\frac{1+Y}{(N/k)} \right] V_I \right\} \frac{1}{A_Q(j\omega)} \tag{A.1b}$$

where X and Y are expressed as:

$$X = \frac{1 + \frac{g_m}{k^2} j\omega L \left(1 - k^2\right)}{1 + \frac{g_m}{N^2} j\omega L \left(1 - k^2\right)} \tag{A.2a}$$

$$Y = \frac{1 - \frac{g_m}{N^2} j\omega L \left(1 - k^2\right)}{1 + \frac{g_m}{N^2} j\omega L \left(1 - k^2\right)} \tag{A.2b}$$

If the oscillation frequency ω is close to the resonant frequency ω_0 and gm is close to 1/R for stable oscillation with R being the tank resistance, $Q \approx R/\omega L$ and $g_m \omega L \approx (g_m R)/Q \approx 1/Q$. As a result, X and Y can be approximated as:

$$X = \frac{1 + j\frac{1}{Q}\left(\frac{1 - k^2}{k^2}\right)}{1 + j\frac{1}{N^2 Q}(1 - k^2)} \tag{A.3a}$$

$$Y = \frac{1 - j\frac{1}{N^2 Q}(1 - k^2)}{1 + j\frac{1}{N^2 Q}(1 - k^2)} \tag{A.3b}$$

For k being close to 1, $X \approx 1$ and $Y \approx 1$. Consequently, (A.1a) and (A.1b) can be further approximated as:

$$V_I \approx g_m \left\{ \left[1 - \frac{1}{(N/k)^2}\right] V_I - \left[\frac{2}{(N/k)}\right] V_Q \right\} \frac{1}{A_I(j\omega)} \tag{A.4a}$$

$$V_Q \approx g_m \left\{ \left[1 - \frac{1}{(N/k)^2}\right] V_Q - \left[\frac{2}{(N/k)}\right] V_I \right\} \frac{1}{A_Q(j\omega)} \tag{A.4b}$$

Compared to (5.10a) and (5.10b), the effective turn ratio N_{eff} can be defined as:

$$N_{eff} = \frac{N}{k} \tag{A.5}$$

A.2 Design Parameters of Switched-Shield Transformer in Chap. 7

This section shows how to derive the effective inductances and the coupling coefficients for the switched-shield n-coil transformer in Chap. 7. Basically, the V-I equations for a traditional 2-coil transformer can be expanded to represent a more general n-coil transformer with magnetic coupling coefficients k_{ij}'s between any two coils with self-inductances L_i and L_j as shown in Fig. A.1. According to the basic law of electromagnetic induction, the induced voltage in the ith coil can be expressed as:

$$\varepsilon_i = -N\frac{d\sum_{j=1}^{n} \Phi_{ij}}{dt} = \sum_{j=1}^{n} \left(-N\frac{d\Phi_{ij}}{dI_j}\frac{dI_j}{dt}\right) \tag{A.6a}$$

Fig. A.1 Schematic
of a multi-coil transformer
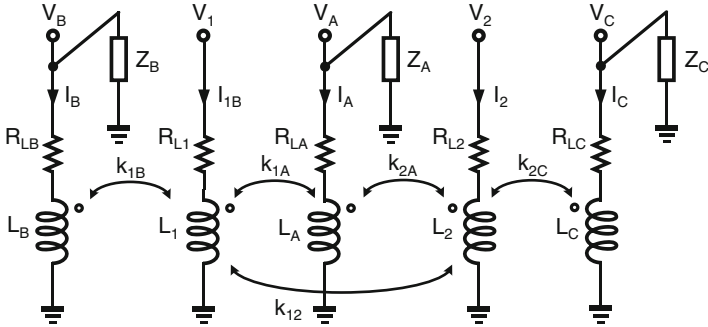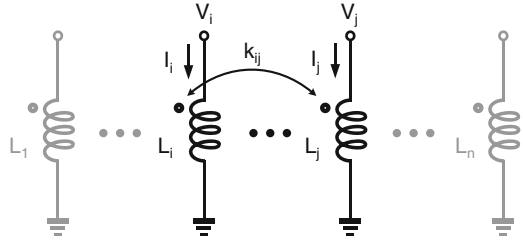
Fig. A.2 Model of the proposed switched-triple-shielded transformer in Chap. 7

$$-N\frac{d\Phi_{ij}}{dI_j} = L_i \quad (i = j) \tag{A.6b}$$

$$-N\frac{d\Phi_{ij}}{dI_j} = M_{ij} \quad (i \neq j) \tag{A.6c}$$

where L_i is the self-inductance of the ith coil, Φ_{ij} is the magnetic flux through the coil L_i induced by the coil L_j, and $M_{ij} = M_{ji} = k_{ij}\sqrt{L_iL_j}$ is the mutual inductance between the ith and jth coils. By putting (A.6b) and (A.6c) into (A.6a) and applying the Laplace transformation, the V-I equation for the ith coil can be expressed as:

$$V_i = sL_iI_i + \sum_{j=1,\ j\neq i}^{n} \left(M_{ij}I_j\right) \tag{A.7}$$

Extending the results in (A.7) to the switched-tripled-shield transformer as shown in Fig. A.2 to get:

$$V_1 = (sL_1 + R_{L1})I_1 + sM_{12}I_2 + sM_{1A}I_A + sM_{1B}I_B \tag{A.8a}$$

$$V_2 = (sL_2 + R_{L2})I_2 + sM_{12}I_1 + sM_{2A}I_A + sM_{2C}I_C \tag{A.8b}$$

$$V_A = (sL_A + R_{LA})I_A + sM_{1A}I_1 + sM_{2A}I_2 = -I_A Z_A \tag{A.8c}$$

$$V_B = (sL_B + R_{LB})I_B + sM_{1B}I_1 = -I_B Z_B \tag{A.8d}$$

$$V_C = (sL_C + R_{LC})I_C + sM_{2C}I_2 = -I_C Z_C \tag{A.8e}$$

Here, the coupling between L_A and L_B and L_A and L_C are ignored because they do not affect L_1 and L_2 directly. By putting (A.8c)–(A.8e) into (A.8a) and (A.8b), the voltages V_1 and V_2 as functions of I_1 and I_2 can be expressed as:

$$
\begin{aligned}
V_1 = &\left(sL_1 + R_{L1} - \frac{s^2 M_{1A}^2}{sL_A + R_{LA} + Z_A} - \frac{s^2 M_{1B}^2}{sL_B + R_{LB} + Z_B} \right) I_1 \\
&+ \left(sM_{12} - \frac{s^2 M_{1A} M_{2A}}{sL_A + R_{LA} + Z_A} \right) I_2
\end{aligned} \tag{A.9a}
$$

$$
\begin{aligned}
V_2 = &\left(sL_2 + R_{L2} - \frac{s^2 M_{2A}^2}{sL_A + R_{LA} + Z_A} - \frac{s^2 M_{2C}^2}{sL_C + R_{LC} + Z_C} \right) I_2 \\
&+ \left(sM_{12} - \frac{s^2 M_{1A} M_{2A}}{sL_A + R_{LA} + Z_A} \right) I_1
\end{aligned} \tag{A.9b}
$$

In the low-k state, M_A is on and M_B and M_C are off, replacing $Z_A = R_{on,A}$, $Z_B = 1/(j\omega C_{off,B})$, and $Z_B = 1/(j\omega C_{off,C})$ in (A.9a) and (A.9b), the following expressions can be obtained:

$$V_1 = \left(L_1' + R_{L1}' \right) I_1 + j\omega M_{12}' I_2 + R_M' I_2 \tag{A.10a}$$

$$V_2 = \left(L_2' + R_{L2}' \right) I_2 + j\omega M_{12}' I_1 + R_M' I_1 \tag{A.10b}$$

where L_1', L_2', R_{L1}', R_{L2}', M_{12}', and R_M' can be expressed as:

$$
\begin{aligned}
L_{1,\text{low-k}}' = &\left\{ 1 - \frac{(\omega L_A)^2}{(R_{LA} + R_{on,A})^2 + (\omega L_A)^2} k_{1A}^2 \right. \\
&\left. + \frac{\omega L_B \left[(\omega C_{off,B})^{-1} - \omega L_B \right]}{R_{LB}^2 + \left[(\omega C_{off,B})^{-1} - \omega L_B \right]^2} \right\} k_{1B}^2 L_1
\end{aligned} \tag{A.11a}
$$

$$L_{2,\text{low-k}}' = \left\{ 1 - \frac{(\omega L_A)^2}{(R_{LA} + R_{\text{on},A})^2 + (\omega L_A)^2} k_{2A}^2 \right.$$

$$\left. + \frac{\omega L_C \left[(\omega C_{\text{off},C})^{-1} - \omega L_C \right]}{R_{LC}^2 + \left[(\omega C_{\text{off},C})^{-1} - \omega L_C \right]^2} k_{2C}^2 L_2 \right\} \tag{A.11b}$$

$$R_{L1,\text{low-k}}' = R_{LA} - \frac{\omega^2 k_{1A}^2 L_A L_1}{(R_{LA} + R_{\text{on},A})^2 + (\omega L_A)^2} (R_{LA} + R_{\text{on},A})$$

$$+ \frac{\omega^2 k_{1B}^2 L_B L_1}{R_{LB}^2 + \left[(\omega C_{\text{off},B})^{-1} - \omega L_B \right]^2} R_{LB} \tag{A.11c}$$

$$R_{L2,\text{low-k}}' = R_{LA} - \frac{\omega^2 k_{2A}^2 L_A L_2}{(R_{LA} + R_{\text{on},A})^2 + (\omega L_A)^2} (R_{LA} + R_{\text{on},A})$$

$$+ \frac{\omega^2 k_{2C}^2 L_C L_2}{R_{LC}^2 + \left[(\omega C_{\text{off},C})^{-1} - \omega L_C \right]^2} R_{LC} \tag{A.11d}$$

$$M_{12,\text{low-k}}' = M_{12} - \frac{\omega^2 M_{1A} M_{2A} L_A}{(R_{LA} + R_{\text{on},A})^2 + (\omega L_A)^2} \tag{A.11e}$$

$$k_{12,\text{low-k}}' = \frac{M_{12,\text{low-k}}'}{\sqrt{L_{1,\text{low-k}}' L_{2,\text{low-k}}'}} \tag{A.11f}$$

$$R_{M,\text{low-k}}' = \frac{\omega^2 M_{1A} M_{2A} (R_{LA} + R_{\text{on},A})}{(R_{LA} + R_{\text{on},A})^2 + (\omega L_A)^2} \tag{A.11g}$$

where $M_{1A} = k_{1A} \sqrt{L_1 L_A}$ and $M_{2A} = k_{2A} \sqrt{L_2 L_A}$.

In (A.11a), the effect of Z_A on the effective series resistance of L_1' through the coupling from L_A to L_1 is already absorbed into the term R_{L1}'. The term $R_M' I_2$ represents the effect of Z_A on the equivalent series resistance of L_1' through the coupling from L_A to L_2 to L_1 because this term becomes zero if the secondary coil is open. As a result, the term $R'_M I_2$ can be ignored when k_{1A}, k_{2A}, and k_{12} are small. Because of the symmetric property for V_2 and V_1, the term $R_M' I_1$ in (A.11b) can also be neglected for the same reason. Consequently, the simplified model for the switched-triple-shield transformer shown in Fig. 8.4 can be obtained, and (A.11a) and (A.11b) can be approximated by the following equations:

$$V_1 \approx \left(L_1' + R_{L1}' \right) I_1 + j\omega M_{12}' I_2 \tag{A.12a}$$

$$V_2 \approx \left(L_2' + R_{L2}' \right) I_2 + j\omega M_{12}' I_1 \tag{A.12b}$$

With assumptions that $(R_{LA} + R_{on,A})^2 \ll (\omega L_A)^2$, $R_{LB/C^2} \ll \left[\left(\omega C_{off,B/C} \right)^{-1} - \omega L_{B/C} \right]^2$, (A.11a)–(A.11f) can be used to obtain (7.3a)–(7.3c) for $L_{1,low-k}'$, $R_{1,low-k}'$, and $k_{12,low-k}'$ and the expressions for $L_{2,low-k}'$ and $R_{2,low-k}'$. Furthermore, by replacing $Z_A = 1/(j\omega C_{off,A})$, $Z_B = R_{on,B}$, and $Z_C = R_{on,C}$ in (A.9a) and (A.9b) and using similar assumptions, the expressions for $L_{1,high-k}'$, $R_{1,high-k}'$, and $k_{12,high-k}'$ as shown in (7.4a)–(7.4c) and $L_{2,high-k}'$ and $R_{2,high-k}'$ can also be derived.

Finally, replacing $Z_A = R_{on,A}$, $Z_B = R_{on,B}$, and $Z_C = R_{on,C}$ in (A.9a) and (A.9b) and using similar assumptions, the expressions for $L_{1,low-L}'$, $R_{1,low-L}'$, and $k_{12,Low-L}'$ as shown in (7.6a)–(7.6c) and $L_{2,low-L}'$, $R_{2,low-L}'$ can be derived. Furthermore, by making $k_{1B} = k_{2C} = 0$, the parameters L_1' and k_{12}' in (7.1a)–(7.2b) and L_2' for the switched-single-shield transformer can also be derived.

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