Practical Guide to Organic Field-Effect Transistor Circuit Design

Antony Sou

SMITHERS RAPRA

Practical Guide to Organic Field-Effect Transistor Circuit Design

Antony Sou

A Smithers Group Company

Shawbury, Shrewsbury, Shropshire, SY4 4NR, United Kingdom
Telephone: +44 (0)1939 250383 Fax: +44 (0)1939 251118
http://www.polymer-books.com

First Published in 2016 by

Smithers Rapra Technology Ltd

Shawbury, Shrewsbury, Shropshire, SY4 4NR, UK

A catalogue record for this book is available from the British Library.

ISBN: 978-1-91024-270-4 (softback)
978-1-91024-271-1 (ebook)

Typeset by Integra Software Services Pvt. Ltd.

Preface

Currently, the field of organic transistor design is fascinating in its breadth and depth. It is at that early stage in its life cycle where the understanding and knowledge of *everything organic* are still accessible. This makes organic electronics a natural melting pot for physicists, chemists, circuit designers, and modelling engineers to come together. However, it also makes it difficult for small research groups to move beyond their usual boundaries. Until now there has been no single concise and coherent work adequately spanning this broad field. This book aims to guide the reader through these different branches with a straightforward text covering the physics and chemistry of the materials, the software construction of the simulation models, and the engineering challenges of the design flow and circuit design.

This book is intended for two main readerships: firstly, physics researchers who have thus far designed circuits using only basic drawing software; secondly, silicon CMOS VLSI Design engineers who are already experienced in the design of full custom transistor level circuits but are not familiar with organic devices or thin film transistor devices. Examples of designs, samples, and measurements are given, allowing the reader to see real-world imperfect devices instead of idealised textbook illustrations. After an introduction in **Chapter 1,** we begin in **Chapter 2** with the physics and chemistry of organic materials and the common fabrication methods. The general principles of field-effect transistors are discussed in **Chapter 3**. Next, the equations of transistor modelling and their translation to a form suitable for simulation are explored in **Chapter 4**. **Chapter 5** describes the design and simulation environments that are necessary to ensure robust reliable design. Finally, all the work dovetails as digital and analogue circuits are described in **Chapters 6** and **7**.

The devices that were designed, fabricated, and analysed in this book were partly fabricated by Guillaume Fichet, Jerome Joimel, Srinivasan Madabhushi, and Liz Speechley at Plastic Logic (now FlexEnable), and by Sungjune Jung and Enrico Gili at the University of Cambridge Cavendish Laboratory. Any references to Plastic Logic's technology has been with their kind permission, although some commercially sensitive details have been withheld. Additional assistance in the cleanroom and labs was provided by Lang Jiang and Vincenzo Pecunia, while further general discussion, conversation, and amusement were amply furnished by Kal Banger, Tom Kehoe, and the entire Optoelectronics department. Furthermore, I am extremely grateful to Professor Henning Sirringhaus for his advice and guidance, and also to Professor

Andrew Flewitt who has been a source of help throughout. This book, and the research from whence it came, would not have been possible without the patience, encouragement, and occasional chiding of my wife Tina, and my daughters Louisa and Alicia.

Antony Sou

Contents

1 Introduction

When the first organic field-effect transistor(s) (OFET) was fabricated in 1987 [1], the established microprocessor of the day was the Intel 80386, which had a minimum channel length of 1.5 μm and 275 000 transistors in an area of 104 mm^2. Nearly 30 years later, the 5.5 billion transistors of the state-of-the-art 18-core Intel Xeon have a minimum channel length of 22 nm in an area of 661 mm^2. Since that first OFET in 1987, there have also been notable advances in the large-scale integration of organic transistors. Recent publications have demonstrated fairly complex circuit functions such as 8 bit, 64 bit, and 128 bit radio frequency identification tags [2–4], programmable logic devices [5], and an 8 bit microprocessor with 3381 transistors at a channel length of 5 μm [6]. These achievements, which are roughly comparable with the Intel 4004 of 1971, are pushing the current envelope of integrated organic transistor circuit design while also benefiting from some of the main advantages of organic transistor technology, such as large area, flexibility, low-temperature fabrication, and solution processing.

Back in 1965, Gordon Moore, the cofounder of Intel Corporation, observed that the number of transistors on an integrated silicon chip had doubled every year since 1958. This observation, though slightly modified to the doubling of transistors every 2 years, was subsequently coined Moore's law [7]. Remarkably, in its much shorter lifetime, the organic transistor count is increasing at almost the same rate, doubling every 25.5 months (**Figure 1.1**). As a consequence, organic transistor circuit design is now experiencing the very same growing pains as its silicon counterpart once did. Continuing exponential increases in circuit complexity and transistor density will not be possible unless accompanied with accurate behavioural modelling and structured design flows.

Thus far, the only Nobel Prize that has been awarded in the field of organic electronics was in 2000 to Alan J. Heeger, Alan G. MacDiarmid, and Hideki Shirakawa [8] 'for the discovery and development of conductive polymers'. Their landmark publication in 1977 for their work on synthesising conducting polymers [9] was the first in a series of notable organic electronics discoveries; namely, the organic photovoltaic(s) (OPV) cell (1986), the OFET (1987), and the organic light-emitting diode(s) (OLED) (1987) [10]. Interest in this new field of research and development has since been rapid, with an increase in scientific publications from 80 in 1999, 393 in 2004 [11], to 602 in 2010. Organic electronics is also beginning to attract real industrial interest

on a global scale, with several active companies such as PolyIC, Polyera, Isorg, and Disasolar. A particular hotbed of organic electronics is in Cambridge, UK. There, the Cavendish Laboratory of the University of Cambridge, UK, has spawned three spin-off companies – Eight19, Cambridge Display Technology, and Plastic Logic (now known as FlexEnable) – which are active in their respective fields of OPV, OLED, and OFET and have attracted significant investment.

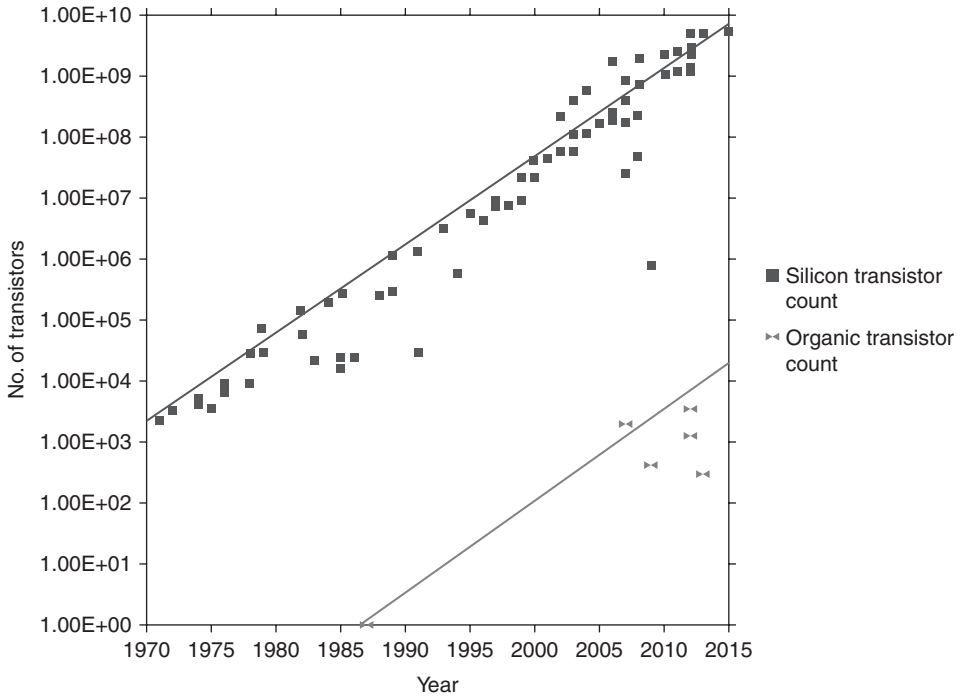


Figure 1.1 Progression of silicon and organic transistor count on a single chip or foil. Both are exhibiting Moore's law, a doubling of transistors approximately every 2 years [2–4, 6]

Despite their poorer performance when compared with their silicon counterparts, organic semiconductors nevertheless have complementary features that make them suitable for alternative applications. Technologically, organic electronics offer the potential for mechanically flexible or conformable devices covering large areas with solution processing. There is also the tantalising promise of system-on-foil, which is the integration of OPV, OFET, and OLED manufactured in a single fabrication process on a single flexible transparent substrate, as a natural goal of organic research to deliver a very elegant final product. In financial terms, the capital outlay necessary for organic electronics is orders of magnitude less than that of silicon foundries. This makes it a

viable proposition for small and medium-sized companies to research and develop, and hopefully industrialise and commercialise. Environmentally too, processing is cleaner and friendlier at lower, even room, temperatures. The first applications of organic semiconductors that have been announced have been based on a large-area matrix of devices with electronic paper displays from companies such as Plastic Logic, but there is also progress in the logic design of more complex circuits.

References

1. H. Koezuka, A. Tsumura and T. Ando, *Synthetic Metals*, 1987, **18**, 699.

2. B.K.C. Kjellander, W.T.T. Smaal, K. Myny, J. Genoe, W. Dehaene, P. Heremans and G.H. Gelinck, *Organic Electronics*, 2013, **18**, 768.

3. E. Cantatore, T.C.T. Geuns, G.H. Gelinck, E. van Veenendaal, A.F.A. Gruijthuijsen, L. Schrijnemakers, S. Drews and D.M. de Leeuw, *IEEE Journal of Solid-State Circuits*, 2007, **42**, 84.

4. K. Myny, S. Steudel, P. Vicca, M.J. Beenhakkers, N.A.J.M. van Aerle, G.H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, *Solid-State Electronics*, 2009, **53**, 1220.

5. A. Sou, Sungjune Jung, E. Gili, V. Pecunia, J. Joimel, G. Fichet and H. Sirringhaus, *Organic Electronics*, 2014, **15**, 3111.

6. K. Myny, E. van Veenendaal, G.H. Gelinck, J. Genoe, W. Dehaene and P. Heremans, *IEEE Journal of Solid-State Circuits*, 2012, **47**, 284.

7. G.E. Moore, *Proceedings of the IEEE*, 1998, **86**, 82.

8. *The Nobel Prize in Chemistry 2000*, Nobelprize.org, 2000. *http://www.nobelprize.org/nobel_prizes/chemistry/laureates/2000/*

9. H. Shirakawa, E. Louis, A. MacDiarmid, S. Chiang and A. Heeger, *Journal of the Chemical Society Chemical Communications*, 1977, **16**, 578.

10. D. Braga and G. Horowitz, *Advanced Materials*, 2009, **21**, 1473.

11. H. Sirringhaus, *Advanced Materials*, 2005, **17**, 2411.

2 Organic Semiconductors

2.1 Introduction

In order properly to appreciate designing with organic transistors, an understanding of the physics and chemistry of organic semiconductors is helpful. Organic electronics is so called because it is based on the carbon atom, on which all known life is based, hence the term *organic*. The modern plastics industry is built upon the same organic polymers made from chains of carbon atoms, so organic electronics is also more popularly known as plastic electronics. This chapter will start by presenting the molecular structure and charge transport properties of organic semiconductors, before discussing and reviewing the current state-of-the-art organic semiconductor materials [1–4].

2.2 Molecular Structure

Organic semiconductors are based on the carbon atom, which has four valence electrons, each able to form a covalent single, double, or triple bond with other atoms. The four valence electrons are found in two atomic orbitals – two electrons in the 2*s* orbital, and two in the 2*p* orbital. Bonding occurs when atoms share electrons to complete their electron shells, and this proceeds via intermediate steps of promotion, where an electron is promoted from the full 2*s* to the empty $2p_z$ energy level to give four unpaired electrons rather than two, and hybridisation to give identical hybrid orbitals [4] (**Figure 2.1**). These hybrid orbitals have their own distinctive shapes, as follows:

- sp^3 hybrid orbitals have four symmetrical fingers in space at 109.5°. In this form, carbon can share four bonds, e.g. CH_4, where each bond is a very strong σ (sigma) bond. The 109.5° bond angle forms the backbone of many conventional polymers. Diamond is an example of carbon formed entirely from σ bonds.

- sp^2 hybrid orbitals have three in-plane fingers at 120° and one perpendicular finger. To form a molecule, another sp^2 hybrid is required. For example, in $H_2C{=}CH_2$, two of the three sp^2 fingers of each carbon bond to hydrogen, and the third sp^2 carbon σ bonds to the other carbon's sp^2. The remaining electron in the p_z orbital forms a delocalised weaker π (pi) bond.

- *sp* hybrid orbitals have two fingers at 180° in one axis and two remaining *p* orbitals. Carbon will bond with two hydrogens and another *sp* hybrid, resulting in one σ bond between the *sp* orbitals and two π bonds with the *p* orbitals.

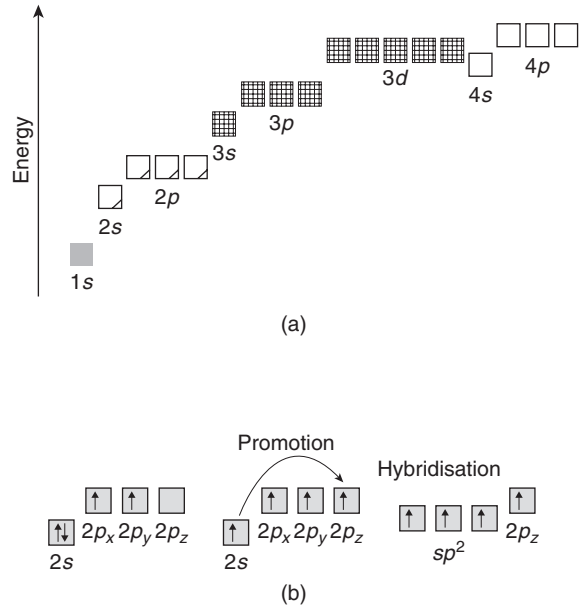


Figure 2.1 (a) Orbital energy levels and (b) promotion and sp^2 hybridisation [5]

To lower the overall energy and increase stability, polymer molecules form a conjugated system of connected *p* orbitals with a backbone based on the hexagonal benzene molecule [e.g., pentacene ($C_{22}H_{14}$), **Figure 2.4**]. These conjugated molecules have alternating single/double or single/triple carbon bonds in which π electrons are delocalised through the entire molecule. The first arriving electrons cluster closely to the nucleus corresponding to the 1*s* orbital which does not participate in bonding. The final electrons go into delocalised π orbitals which do contribute to bonding.

A system of bands for organic semiconductors can also be described. In this case, the last filled pair of electrons occupies a molecular orbit called the highest occupied molecular orbit (HOMO). The next molecular orbit beyond the HOMO, and therefore unfilled, is called the lowest unoccupied molecular orbit (LUMO). In this analogy, the energy difference between the HOMO and the LUMO is also called the bandgap (**Figure 2.2**).

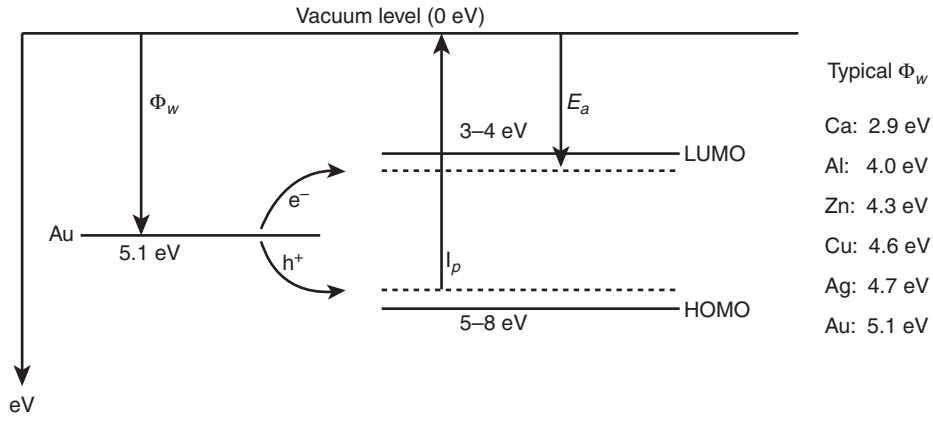


Figure 2.2 Energy bands in an organic semiconductor at the interface with a metal (gold), and some typical work function values. E_a: electron affinity; I_p: ionisation potential; and Φ_w: work function

2.3 Charge Carrier Transport

Organic field-effect transistor(s) (OFET) are usually made from undoped materials. As there are no intrinsic carriers present, in order for a current to flow, charge carriers must be injected from the *source* metal electrode into the semiconductor channel, and collected at the other end of the channel by the *drain* metal electrode. The injected carriers occupy states in the semiconductor's HOMO and LUMO bands but may also occupy localised states in the bandgap that are induced by defects and unwanted impurities [6]. For the organic semiconductor–metal electrode interface, an ohmic connection is generally not possible, and sometimes exhibits a gate voltage and semiconductor thickness dependency [7, 8] requiring charge carriers to overcome energy barriers before entering or leaving the semiconductor. Organic semiconductors can operate in either electron or hole accumulation modes, or both in the case of ambipolar devices, depending on the polarity of the gate voltage. The amount and type of carrier injection is determined by the Φ_w of the metal electrode and the E_a of the semiconductor for electron injection or the I_p of the semiconductor for hole injection. The energy barriers presented at the source and drain electrodes usually limit the devices to unipolar electron or hole accumulation mode operation only. Some typical metal work function values are shown in **Figure 2.2.**

After carriers have been injected into the semiconductor channel, they will move in the direction of the applied source–drain electric field, but their progress is limited by their mobility, μ_0, and by disorder effects. In crystalline inorganic semiconductors

where there is long-range order and delocalised carriers, motion is coherent (band-like) and characterised by a wave vector k. However, in organic semiconductors at room temperature, the precise mechanisms of charge transport are not yet fully understood [9]. Transport is generally described as thermally activated, hopping through localised states and traps, and is thought to be always incoherent even in crystalline materials. Two models of charge transport are discussed later in this chapter.

The local intramolecular structure and intermolecular packing between molecules will greatly affect charge carrier transfer from molecule to molecule [10]. Motion through polycrystalline structures is dominated by grain boundaries impeding charge carriers. The molecular uniformity of the semiconductor–dielectric interface also has a huge influence on charge transport. There are obstacles impeding the progress of the charge, such as static structural and energetic disorder, which slow down carriers, resulting in a percolation motion. There is also current limiting by space charge, whereby the injection of carriers into a semiconductor causes a screening effect of the external electric field, reducing its effect upon other mobile charge carriers. Shallow or deep traps further inhibit the progress of charge carriers, causing a hopping mode of transport.

2.3.1 Hopping Transport

Hopping transport (**Figure 2.3**) is a site-to-site phonon-assisted thermally activated tunnelling mechanism between localised bandgap states that are spatially and energetically close [11], classically described by Vissenberg and Matters [12]. In a charge transport model based on variable range hopping, localised charge carriers in amorphous organic films are not activated to a transport level, but instead are able to hop directly from site to site, either a short distance where there is high activation energy or a long distance where there is low activation energy. The model predicts that μ_0 will increase with increasing gate voltage. This can be explained qualitatively by assuming that accumulated charge carriers will fill lower-lying energy states first. As the lower energy traps are filled, it becomes less likely that other mobile charge carriers will become trapped, so trapping becomes less efficient and μ_0 rises. Subsequent charge carriers will occupy states with higher energies requiring less energy to hop between sites [9]. Mobility μ_0 also increases with temperature and is strongly dependent on the density of localised states [12].

2.3.2 Multiple Trap and Release

Another model for (polycrystalline) organic materials is the MTR model (**Figure 2.3**) [13, 14]. In this transport model, the semiconductor consists of crystallites separated by grain boundaries. This model differs from hopping models in that it predicts that

charges will move in delocalised bands within crystallites until they are trapped at the grain boundaries. These traps may be caused by impurities or physical defects. Charge carriers fall into a trap of localised states in the bandgap and remain trapped until they are released by thermal activation to a transport level, whereupon they once again become active. The time spent in the trap depends on the temperature and on the depth of the trap.

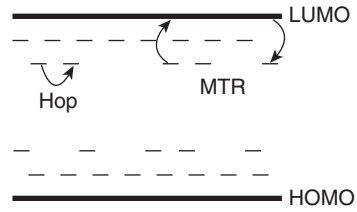


Figure 2.3 Charge transport mechanisms showing hopping and multiple trap and release (MTR) between energy levels

2.4 Materials

2.4.1 Semiconductors

Current small-molecule and conjugated polymer materials have field-effect mobilities exceeding 1 cm^2/Vs, an increase in performance of 3–4 orders of magnitude within the last 25 years [15]. In this section, an overview is given of the state-of-the-art solution-processable p-type organic semiconductors, including small-molecule-based materials, conjugated polymers, and the latest donor–acceptor conjugated polymers. This overview has been taken from an excellent 25th anniversary review article by Sirringhaus published in *Advanced Materials* [15].

2.4.1.1 Small Molecule

Perhaps the first popular organic semiconductor, and still the most used, is $C_{22}H_{14}$. By way of example, $C_{22}H_{14}$ is described here to illustrate several key points about organic semiconductors. $C_{22}H_{14}$ is an organic small molecule that consists of five benzene rings in a linear chain. This forms a planar molecular structure allowing delocalised electrons to move freely (**Figure 2.4a**). Within a monolayer, $C_{22}H_{14}$ molecules are packed in a planar herringbone crystal structure (**Figure 2.4b**), where conductivity in the horizontal *XY* plane is higher than in the vertical *Z* direction [16]. The close molecule stacking of the herringbone crystal structure allows charge carriers easily to hop from one molecule to another by quantum mechanical tunnelling [17]. However, there are grain boundaries and defects that inhibit hopping and reduce μ_0.

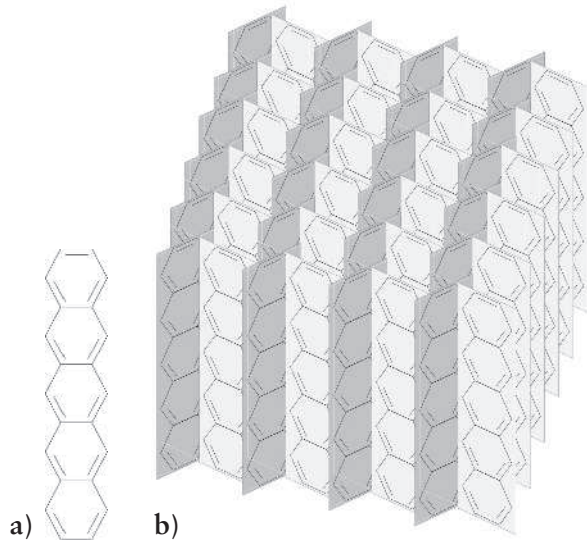


Figure 2.4 $C_{22}H_{14}$ small molecule showing (a) benzene backbone and (b) herringbone stacking structure [1]

As with most organic semiconductors, $C_{22}H_{14}$ is intrinsically ambipolar, able in principle to transport both holes and electrons depending on the gate voltage and the injection barriers at the source and drain. In air, the hole μ_0 in a $C_{22}H_{14}$ transistor is around 0.1–1 cm^2/Vs, but electron μ_0 is much lower. This is due to electrons in the $C_{22}H_{14}$ molecule being very reactive to ambient water molecules, and hydroxyl groups at the semiconductor–dielectric interface acting like traps [1]. As a result, $C_{22}H_{14}$ is considered to be a unipolar p-type semiconductor only, as is the case with most other organic semiconductors.

In general, small-molecule organic semiconductor mobility, μ_0, depends on the molecular structure and the intermolecular packing, which determine the reorganisation energy and transfer integrals. The highest-μ_0 materials have small reorganisation energy and large transfer integrals, with any static structural disorder minimised by material purification and interface control [18].

Many of the highest-μ_0 solution-processed small molecules are based on substituting triisopropyl-silylethynyl (TIPS) onto a $C_{22}H_{14}$ core [19]. Spin-coated 6,13-*bis*(triisopropyl-silylethynyl)pentacene (TIPS-P) films show a highly crystalline structure with a two-dimensional brick-wall cofacial π–π stacking in the plane of the film with side chains normal to the substrate surface. Early spin-coated TIPS-P obtained mobilities exceeding 1 cm^2/Vs [20]. Similar results were achieved with triethylsilylethynyl anthradithiophene (TESADT) [21] and difluorinated-triethylsilylethynyl anthradithiophene (dif-TESADT)

(dif-TESADT) [22]. Using a blade-coating technique, still higher mobilities of up to 11 cm^2/Vs were attainable with TIPS-P [23, 24]. A class of materials based upon end-substituted phenylene-thiophene, selenophene, or thiazine fused ring systems invented by Takimiya [25, 26] led to a bottom-gate OFET with drop-cast di-alkyl end-substituted benzothienobenzothiophene (BTBT) derivative, C_8-BTBT, as the semiconductor and a μ_0 of 5 cm^2/Vs [27]. The highest reported μ_0 so far of 31.3 cm^2/Vs has been seen by Minewari and co-workers using a two-shot printing technique, also with C_8-BTBT [28].

In blended films of TIPS-P and dif-TESADT, where the small molecule tends to segregate to the surface, mobilities of 1 and 2.4 cm^2/Vs have been reported [29]. The binder polymer strongly influences the crystallinity of the small molecule. More recently, dif-TESADT devices with an optimised binder have achieved mobilities of 4–5 cm^2/Vs [30].

2.4.1.2 Conjugated Polymers

Although fully amorphous conjugated polymers have achieved mobilities of 0.01 cm^2/Vs, the most successful conjugated polymers have been based on semicrystalline lamellar structures with an edge-on polymer orientation [15]. In these structures, alternating layers of conjugated backbones are formed, separated from each other by layers of flexible side chains that are parallel to the substrate plane. Charge transport in the plane of the film is thus not impeded by the insulating side chains. The best example of this structure has been using poly[2,5-*bis*(3-alkylthiophen-2-yl) thieno[3,2-*b*]thiophene] (PBTTT) to achieve a μ_0 of 1.1 cm^2/Vs [31, 32].

2.4.1.3 Donor–Acceptor Copolymers

Donor–acceptor copolymers are usually more complex and larger than conjugated polymers. Normally consisting of alternating electron-rich (donor) and electron-deficient (acceptor) units along the backbone, they exhibit a relatively low bandgap that aids in the selection of suitable electron- or hole-injecting contacts.

The first demonstrations of high-μ_0 donor–acceptor polymers were a copolymer of polynaphthalate-bithiophene, an n-type material with a μ_0 of 0.8 cm^2/Vs [33], and cyclopentadithiophene-benzothiadiazole (CDT-BTZ), which had a μ_0 of 3.5 cm^2/Vs in dip-coated thin films [34]. Both polymers were originally thought to be amorphous but were later found to be semicrystalline. Ambipolar donor–acceptor copolymers based on the electron-deficient diketopyrrolopyrrole (DPP) have attracted much interest. The first ambipolar top gate with electron and hole mobilities greater than 1 cm^2/Vs were reported in 2011 [35] and 2012 [36]. Using the same polymer and a

self-assembled monolayer-modified silicon dioxide gate dielectric, mobilities as high as 10 cm^2/Vs have been achieved [37]. Meanwhile, indacenodithiophene (IDT)-based copolymers have reported a μ_0 of 3.6 cm^2/Vs [38, 39], while IDT–BT copolymers have reported mobilities of 1.2–3.6 cm^2/Vs [40, 41].

2.4.2 Dielectrics

The performance of OFET is greatly influenced by the dielectric material and the semiconductor–dielectric interface. In general, a high-*k* dielectric material is preferable to a low-*k* dielectric material. A high-*k* material will allow a higher drive current at a lower voltage. Common dielectrics such as CYTOP™ (relative permittivity E_r = 2.1) and polymethyl methacrylate (PMMA) (E_r = 3.6) are easy to process but are relatively low-*k* materials. Newer materials such as aluminium oxide (E_r = 8–10) and titanium dioxide (E_r = 20–41) offer a higher *k* and lower voltage operation [2]. High-*k* polymer dielectrics have also been researched. These high-*k* relaxer ferroelectric polymers are of the polyvinylidene fluoride (PVDF) family and realise relative permittivities as high as E_r = 50, allowing low-voltage device operation in conjunction with several organic semiconductors [42].

2.5 Summary

In this chapter, the molecular structure and charge transport mechanisms of organic semiconductors have been described. $C_{22}H_{14}$ was introduced as an example of a common organic semiconductor, and the current state-of-the-art organic semiconductor materials were briefly reviewed. In the next chapter, these concepts are abstracted as the theory and operation of transistors is considered.

References

1. H. Marien, M. Steyaert and P. Heremans in *Analog Organic Electronics: Building Blocks for Organic Smart Sensor Systems on Foil*, Springer Science+Business Media, New York, NY, USA, 2013.

2. H. Sirringhaus, *Advanced Materials*, 2005, **17**, 2411.

3. G.G. Malliaras and R. Friend, *Physics Today*, 2005, **58**, 53.

4. M. Grell in *Masters Course in Nanotechnology – Organic Semiconductors*, University of Sheffield, Sheffield, UK, 2009.

5. *Helping You to Understanding Chemistry*, Chemguide. *http://www.chemguide.co.uk*

6. S. Mijalkovic, D. Green, A. Nejim, G. Whiting, A. Rankov, S. Smith, J. Halls and C. Murphy in *Proceedings of the 26th International Conference on Microelectronics, MIEL 2008*, 11–14th May, Niš, Serbia, 2008, p.469.

7. T. Richards and H. Sirringhaus, *Journal of Applied Physics*, 2007, **102**, 094510.

8. J.A. Jiménez Tejada, K.M. Awawdeh, J.A.L. Villanueva, J.E. Carceller, M.J. Deen, N.B. Chaure, T. Basova and A.K. Ray, *Organic Electronics*, 2011, **12**, 832.

9. D. Braga and G. Horowitz, *Advanced Materials*, 2009, **21**, 1473.

10. H. Sirringhaus, M. Bird, T. Richards and N. Zhao, *Advanced Materials*, 2010, **4307**, 3893.

11. S.G.J. Mathijssen, M. Cölle, H. Gomes, E.C.P. Smits, B. de Boer, I. McCulloch, P.A. Bobbert and D.M. de Leeuw, *Advanced Materials*, 2007, **19**, 2785.

12. M. Vissenberg and M. Matters, *Physical Review B*, 1998, **57**, 964.

13. G. Horowitz, R. Hajlaoui and P. Delannoy, *Journal de Physique III*, 1995, **5**, 355.

14. M.E. Gershenson, V. Podzorov and A.F. Morpurgo, *Reviews of Modern Physics*, 2006, **78**, 973.

15. H. Sirringhaus, *Advanced Materials*, 25th Anniversary Article, January 2014.

16. J.C. Sancho-Garcia, G. Horowitz, J.L. Bredas and J. Cornil, *Journal of Chemical Physics*, 2003, **119**, 12563.

17. G.H. Gelinck, E. van Veenendaal and R. Coehoorn, *Applied Physics Letters*, 2005, **87**, 073508.

18. J. Brédas, J. Calbert, D. da Silva Filho and J. Cornil, *Proceedings of the National Academy of Sciences USA*, 2002, **99**, 5804.

19. J.E. Anthony, J.S. Brooks, D.L. Eaton and S.R. Parkin, *Journal of the American Chemical Society*, 2001, **123**, 9482.

20. M. Payne, S. Parkin, J.E. Anthony, C.C. Kuo and T.N. Jackson, *Journal of American Chemical Society*, 2005, **127**, 4986.

21. S.S. Lee, C.S. Kim, E.D. Gomez, B. Purushothaman, M.F. Toney, C. Wang, A. Hexemer, J.E. Anthony and Y-L. Loo, *Advanced Materials*, 2009, **21**, 3605.

22. D.J. Gundlach, J.E. Royer, S.K. Park, S. Subramanian, O.D. Jurchescu, B.H. Hamadani, A.J. Moad, R.J. Kline, L.C. Teague, O. Kirillov, C.A. Richter, J.G. Kushmerick, L.J. Richter, S.R. Parkin, T.N. Jackson and J.E. Anthony, *Nature Materials*, 2008, **7**, 216.

23. Y. Diao, B.C-K. Tee, G. Giri, J. Xu, D.H. Kim, H.A. Becerril, R.M. Stoltenberg, T.H. Lee, G. Xue, S.C.B. Mannsfeld and Z. Bao, *Nature Materials*, 2013, **12**, 665.

24. G. Giri, E. Verploegen, S.C.B. Mannsfeld, S. Atahan-Evrenk, D.H. Kim, S.Y. Lee, H.A. Becerril, A. Aspuru-Guzik, M.F. Toney and Z. Bao, *Nature*, 2011, **480**, 504.

25. K. Takimiya, H. Ebata, K. Sakamoto, T. Izawa, T. Otsubo and Y. Kunugi, *Journal of the American Chemical Society*, 2006, **128**, 12604.

26. T. Yamamoto and K. Takimiya, *Journal of the American Chemical Society*, 2007, **129**, 2224.

27. T. Uemura, Y. Hirose, M. Uno, K. Takimiya and J. Takeya, *Applied Physics Express*, 2009, **2**, 111501.

28. H. Minemawari, T. Yamada, H. Matsui, J. Tsutsumi, S. Haas, R. Chiba, R. Kumai and T. Hasegawa, *Nature*, 2011, **475**, 364.

29. R. Hamilton, J. Smith, S. Ogier, M. Heeney, J.E. Anthony, I. McCulloch, J. Veres, D.D.C. Bradley and T.D. Anthopoulos, *Advanced Materials*, 2009, **21**, 1166.

30. J. Smith, W. Zhang, R. Sougrat, K. Zhao, R. Li, D. Cha, A. Amassian, M. Heeney, I. McCulloch and T.D. Anthopoulos, *Advanced Materials*, 2012, **24**, 2441.

31. I. McCulloch, M. Heeney, C. Bailey, K. Genevicius, I. MacDonald, M. Shkunov, D. Sparrowe, S. Tierney, R. Wagner and W. Zhang, *Nature Materials*, 2006, **5**, 328.

32. B.H. Hamadani, D.J. Gundlach, I. McCulloch and M. Heeney, *Applied Physics Letters*, 2007, **91**, 243512.

33. H. Yan, Z. Chen, Y. Zheng, C. Newman, J. Quinn, F. Dotz, M. Kastler and A. Facchetti, *Nature*, 2009, **457**, 679.

34. H.N. Tsao, D. Cho, J.W. Andreasen, A. Rouhanipour, D.W. Breiby, W. Pisula and K. Müllen, *Advanced Materials*, 2009, **21**, 209.

35. H. Bronstein, Z. Chen, R.S. Ashraf, W. Zhang, J. Du, J.R. Durrant, P.S. Tuladhar, K. Song, S. E. Watkins, Y. Geerts, M.M. Wienk, R.A.J. Janssen, T. Anthopoulos, H. Sirringhaus, M. Heeney and I. McCulloch, *Journal of the American Chemical Society*, 2011, **133**, 3272.

36. Z. Chen, M.J. Lee, R. Shahid Ashraf, Y. Gu, S. Albert-Seifried, M. Meedom Nielsen, B. Schroeder, T. Anthopoulos, M. Heeney, I. McCulloch and H. Sirringhaus, *Advanced Materials*, 2012, **24**, 647.

37. J. Li, Y. Zhao, H. Tan, Y. Guo, C. Di and G. Yu, *Scientific Reports*, 2012, **2**, 754.

38. T. Lei, J-H. Dou and J. Pei, *Advanced Materials*, 2012, **24**, 6457.

39. J. Mei, D.H. Kim, A.L. Ayzner, M.F. Toney and Z. Bao, *Journal of the American Chemical Society*, 2011, **133**, 20130.

40. W. Zhang, J. Smith, S.E. Watkins, R. Gysel, M. McGehee, A. Salleo, J. Kirkpatrick, S. Ashraf, T. Anthopoulos, M. Heeney and I. McCulloch, *Journal of the American Chemical Society*, 2010, **132**, 11437.

41. X. Zhang, H. Bronstein, A. J. Kronemeijer, J. Smith, Y. Kim, R.J. Kline, L.J. Richter, T. Anthopoulos, H. Sirringhaus, K. Song, M. Heeney, W. Zhang, I. McCulloch and D.M. DeLongchamp, *Nature Communications*, 2013, **4**, 2238.

42. J. Li, D. Liu, Q. Miao and F. Yan, *Journal of Materials Chemistry*, 2012, **22**, 15998.

3 Field-Effect Transistors

3.1 Introduction

The first point-contact transistor was invented in 1947 by Bardeen, Brattain, and Shockley, who subsequently received the Nobel Prize for their work in 1956 [1]. Not commercially successful, the point-contact transistor gave way to the subsequent inventions of bipolar junction transistor(s) (BJT) and especially field-effect transistors, which have now become ubiquitous in nearly all electronics products. The premise of the transistor is simple – a voltage-controlled electronic switch, or amplifier – yet transistors have gone on to become the cornerstones of the modern digital world.

In the previous chapter, the concepts, physics, and materials of organic transistors were discussed. In this chapter, their application as transistors is introduced, their operation is explained, and their key parameters are explored.

3.2 Transistor Configurations

An organic field-effect transistor (OFET) is a three-terminal device – gate, source, and drain – where, conventionally, the conductivity of the device is controlled by a vertical electric field from the gate terminal acting upon a horizontal conduction channel that has been formed in the semiconductor between the source and drain electrodes. An organic thin-film transistor (OTFT) is a special case of an OFET in which the semiconductor and dielectric are deposited as thin films on top of an inactive substrate that plays no part in the transistor behaviour. There are four possible configurations of gate, source, and drain in an OTFT (**Figure 3.1**). The most popular configurations are the bottom-gate bottom-contact architecture, for its ease of fabrication in research labs, and the top-gate bottom-contact architecture, which offers the largest area for charge injection and extraction. There is a further classification of staggered or coplanar device, depending on the charge carrier path within the gate-induced accumulation channel. The current path within a coplanar configuration is almost entirely horizontal, whereas in a staggered configuration the current path is vertical near the source and drain, which offers a larger area for charge injection into the semiconductor.

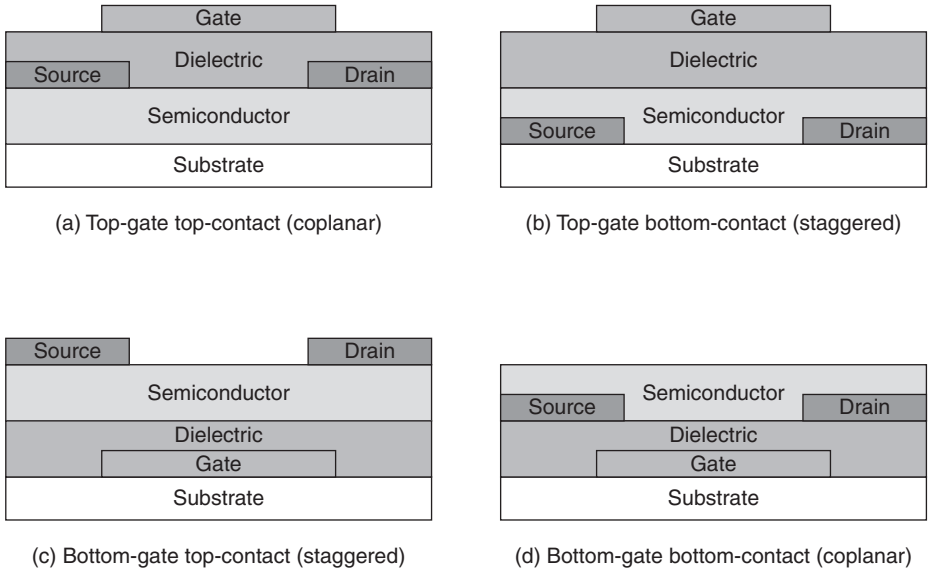


Figure 3.1 Thin-film transistor(s) (TFT) gate and contact configurations

The OTFT is fabricated when the organic semiconductor is deposited across the source and drain electrodes to form the transistor channel. The semiconductor itself is separated from the gate electrode by a thin layer of gate dielectric material. Although the source and drain are physically identical, the source electrode is conventionally considered as the source of charge carriers. Transistors are primarily described by their conduction channels: p-type transistors are those with hole-accumulated channels, while n-type transistors are those that operate with electron-accumulated channels. For p-type transistors, as holes are the charge carriers, the source is the most positive terminal, and is often made of a high-work-function metal such as gold (5.1 eV). Conversely, for n-type transistors, electrons are injected from the negative source terminal, which is ideally a low-work-function metal such as calcium (2.9 eV), though these may not be environmentally stable [2].

It is convenient to reference all transistor voltages to the source electrode. In this respect, a drain-source voltage (V_{DS}) and a gate-source voltage (V_{GS}) are applied. The application of V_{GS} modulates an electric field across the transistor channel, which causes an accumulation of charge carriers at the semiconductor–dielectric interface. The depth of the conducting layer is very thin, no more than a few nanometres at the surface of the semiconductor at the interface.

Transistors may be either enhancement mode or depletion mode. Both p- and n-type enhancement-mode transistors have no conductive channel in the absence of a

gate voltage, while there is always a conduction channel in depletion-mode devices which require an opposite-polarity gate voltage to turn off the transistor. As organic semiconductors are normally undoped with no intrinsic carriers available, organic transistors are usually enhancement mode.

3.3 Transistor Operation

When a gate voltage is applied, a field is induced at the semiconductor–insulator interface that causes the highest occupied molecular orbit and lowest unoccupied molecular orbit to shift relative to the source and drain Fermi levels which are held at a fixed value by external voltages [3]. If the gate voltage is large enough, mobile charge carriers will flow from the source contact into the semiconductor. When a potential difference is then applied to the source–drain, charge carriers will flow to the drain contact, completing the electrical circuit.

Transistors operate in distinct regimes or regions (**Figures 3.2** and **3.3**):

1. In the off state, $V_{GS} << V_T$, there is no accumulated conducting channel. The source–drain current, I_{DS}, is very small and is determined by the intrinsic conductivity of the bulk semiconductor:

$$I_{DS(cut-off)} = I_{leak} \text{ when } V_{GS} << V_T \tag{3.1}$$

   where I_{leak} is a small intrinsic leakage current in the bulk semiconductor and V_T is the threshold voltage.

2. In the subthreshold region, $V_{GS} < V_T$, the source–drain current, I_{DS}, increases exponentially with gate voltage, similarly to the current due to a forward-biased diode. This exponential behaviour is often attributed to deep trap states [4]:

$$I_{DS(subthreshold)} = I_{S0} e^{\frac{V_{GS}}{nV_{th}}} \text{ when } V_{GS} \leq V_T \tag{3.2}$$

   where $V_{th} = kT/q$ is the thermal voltage (~26 mV at room temperature), n is the subthreshold slope factor, and I_{S0} is a process-dependent parameter that also has some dependence on V_T. These two parameters, I_{S0} and V_T, are best extracted from experimental data [5]. In organic devices, owing to the large values of V_T, subthreshold behaviour is important and accounts for a significant amount of current. This current is often considered to be a parasitic leakage current in digital circuits, but in analogue circuits it may be utilised very efficiently in a similar manner to BJT devices or low-power metal-oxide semiconductor field-effect

transistor (MOSFET) devices. Performance of a device in the subthreshold region is measured by the subthreshold slope parameter n, which is defined as the change in V_{GS} needed to effect a decade increase in I_{DS} current.

3. In the linear region, $V_{GS} \geq V_T$ and $V_{DS} < V_{GS} - V_T$. A conducting channel at the semiconductor–dielectric interface is only formed when V_{GS} is greater than the V_T. An equal amount of charge, but opposite in sign, appears on either side of the dielectric. The V_T is the result of either shallow traps in the semiconductor, which need to be filled, or charged dipoles already in the channel, which need additional gate voltage to form the channel [6]:

$$I_{DS(linear)} = \frac{W}{L}\mu C_{diel}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{1}{2}V_{DS}^{2}\right] \text{ when } V_{DS} < V_{GS} - V_T \tag{3.3}$$

where μ is the surface mobility of the channel, C_{diel} is the capacitance per unit area of the gate dielectric, W is the channel width, and L is the channel length.

4. Saturation occurs when $V_{GS} \geq V_T$ and $V_{DS} \geq V_{GS} - V_T$. At these terminal voltages, the potential at some point in the channel drops to zero. At this position in the channel, approximately where $V_{GS} < V_{DS}$, there is now no longer an effective V_{GS} to maintain the charge in the channel. A region depleted of charge carriers forms next to the drain, and the channel is pinched off, with the source–drain current saturated. Further increases in V_{DS} will widen the depletion region next to the drain and move the pinch-off point towards the source, resulting in a shorter accumulated channel length, less resistance, and a small increase in I_{DS}. I_{DS} is now substantially independent of V_{DS} and is mainly controlled by V_{GS}. By substituting $V_{DS} = V_{GS} - V_T$ in **Equation 3.3**, and adding a parameter for the channel length modulation, the source–drain current for the saturation region can be derived:

$$I_{DS(sat)} = \frac{1}{2}\frac{W}{L}\mu C_{diel}\left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right) \text{ when } V_{DS} < V_{GS} - V_T \tag{3.4}$$

where λ is the channel length modulation parameter.

For convenience, in **Equations 3.3** and **3.4**, a transistor gain factor, β, may be defined:

$$\beta = \left(\mu C_{diel}\right)\frac{W}{L} = \left(\mu\frac{\epsilon_r\epsilon_0}{d_{diel}}\right)\frac{W}{L} \tag{3.5}$$

Gain factor β can be further separated into two other factors, a geometry gain factor (W/L) and a process gain factor ($\kappa' = \mu C_{diel}$) or $\left(k' = \mu \frac{\epsilon_r \epsilon_0}{d_{diel}} \right)$, where ε_r is the relative permittivity of the gate dielectric and d_{diel} is the thickness of the gate dielectric. The process gain factor κ' may be occasionally referenced when the semiconductor's mobility μ, the dielectric's relative permittivity ε_r, and the dielectric's thickness d_{diel} are commercially sensitive and not disclosed. For the purposes of calculations in this book, the dielectric's relative permittivity has been assumed to be ε_r = 3.6 throughout, and the thickness of the dielectric has been assumed to be based on a standard value d_{diel} = 850 nm.

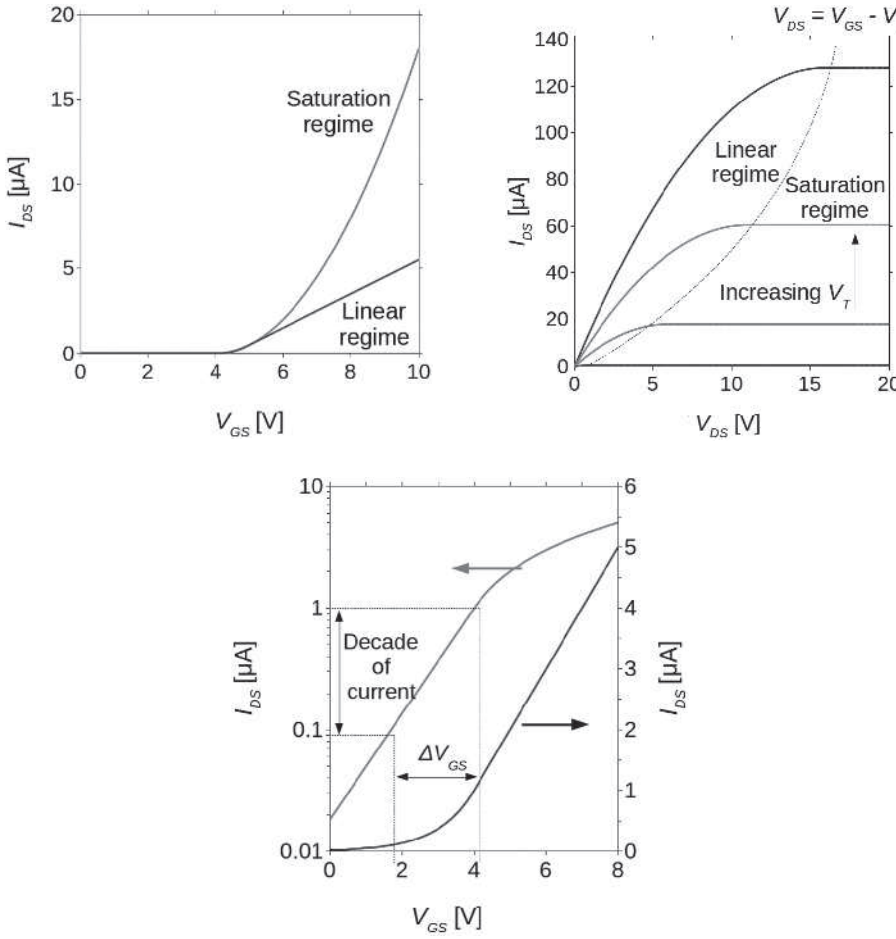


Figure 3.2 Linear and saturation transistor regions of operation shown in (a) a transfer curve and (b) an output curve. The subthreshold transfer characteristic is shown in (c)

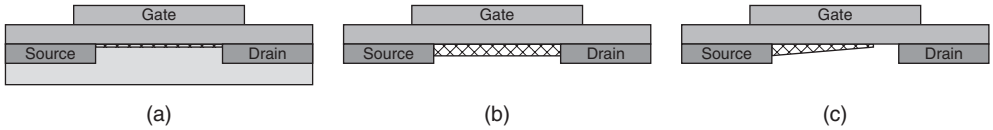


Figure 3.3 Channel region for (a) off state, (b) linear mode, and (c) saturation mode

3.4 Threshold Voltage

OFET operate in accumulation mode with no intrinsic carriers and no depletion layer to isolate the conduction channel from the bulk. Therefore, the V_T is the gate voltage when a depleted channel becomes one in accumulation [7]. At equilibrium, the Fermi level is located in the middle of the bandgap. At low gate bias, most charge carriers go into localised states in the bandgap, and transport occurs with low mobility by hopping between these localised states. As the gate bias increases, more states are filled and the Fermi level moves towards the conduction band. This leads to an increase in carrier concentration in the conduction band and a rise in mobility. In other words, the V_T corresponds to a gate-bias-dependent mobility [8].

The V_T can be extracted from drain current or capacitance measurements [9]. In a paper by Ortiz-Conde [10], 13 methods of V_T extraction for MOSFET were investigated, 11 of which were from the linear region of operation, and two from the saturation region, which proved to be the most accurate. These were compared with an *n*-channel single-crystal bulk MOSFET and an *n*-channel hydrogenated amorphous silicon (a-Si:H) thin-film MOSFET. A similar paper by Boudinet analysed eight V_T extraction techniques for n-type OFET [11]. The two most popular and most often used threshold extraction methods are presented here now.

3.4.1 Extrapolation of Linear Region

By extrapolating the I_{DS} current in the linear region (ELR) of the transfer curve measurement (**Equation 3.3**), V_T is calculated from the intercept with the *x*-axis:

$$\beta\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{1}{2}V_{DS}^2\right] = 0 \tag{3.6}$$

$$V_T = V_{GS} - \frac{1}{2}V_{DS} \tag{3.7}$$

3.4.2 Extrapolation of Saturation Region

By extrapolating the square root of the I_{DS} current in the saturation region (ESR) of a transfer curve measurement (**Equation 3.4**), V_T is given from the intercept with the x-axis:

$$\frac{1}{2}\beta\left(V_{GS} - V_T\right)^2 = 0 \tag{3.8}$$

$$V_T = V_{GS} \tag{3.9}$$

3.5 Mobility

The conducting channel in the semiconductor of an OFET is only a few nanometres thick and located adjacent to the dielectric. It is unsurprising, then, that the charge carrier mobility depends not only on the semiconductor but also on the dielectric and the semiconductor–dielectric interface [12]. Mobility is affected by factors such as the roughness of the semiconductor–dielectric interface and by dipoles in the dielectric. For organic semiconductors, there is a gate-voltage-dependent mobility [13, 14], usually modelled as

$$\mu = \mu_0\left(\frac{V_{GS} - V_T}{V_{aa}}\right)^{\gamma} \tag{3.10}$$

where γ and V_{aa} are empirical fitting parameters, and μ_0 is normally taken to be the band mobility. Parameter γ is related to the conduction mechanism and can describe both an increase or a decrease in mobility with V_{GS}. With an increase in mobility, $\gamma > 0$, which is typical of amorphous and nanocrystalline devices and is related to a trap conduction mechanism. A decrease in mobility with gate voltage, $\gamma < 0$, appears in polycrystalline TFT when surface scattering starts to be important [15].

There are four different types of mobility [16], which can be calculated to a first order as follows:

- Hall mobility – commonly used for bulk or material measurements.
- Effective mobility – calculated from the drain conductance (g_d) in the linear region of the output curve:

$$g_d = \frac{\delta I_{DS}}{\delta V_{DS}} V_{GS} = const \tag{3.11}$$

$$\mu_{eff} = \frac{L}{W} \frac{g_d}{C_{diel}\left(V_{GS} - V_T\right)} \tag{3.12}$$

- Field-effect mobility – calculated from the transistor transconductance (g_m is the slope of the transfer curve) in the linear region:

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} V_{DS} = const \tag{3.13}$$

$$\mu_{fet} = \frac{L}{W} \frac{g_m}{C_{diel} V_{DS}} \tag{3.14}$$

  Any discrepancy between μ_{fet} and μ_{eff} is due to the neglect of any gate-voltage-dependent mobility effects.

- Saturation mobility – derived from plotting $\sqrt{(I_{DS(sat)})}$ against $(V_{GS} - V_T)$ from the output curve:

$$m = \frac{\delta\sqrt{I_{DS}}}{\delta\left(V_{GS} - V_T\right)} V_{DS} = const \tag{3.15}$$

$$\mu_{sat} = \frac{L}{W} \frac{2m^2}{C_{diel}} \tag{3.16}$$

As with μ_{fet}, μ_{sat} also neglects any gate-dependent effects. Also, by definition, in the pinch-off region there are no charge carriers at the pinched-off drain electrode, but there are plenty of charge carriers at the source electrode. As the density of charge carriers varies considerably along the saturated channel, μ_{sat} can therefore only

measure the mean mobility along the channel. For this reason, it is often better to extract mobility when the transistor is in the linear region, where the charge carrier distribution is more uniform [6].

3.6 Contact Resistance

The source and drain electrodes do not usually present a low-resistance ohmic connection to the organic semiconductor. Instead, there is a high-resistance ohmic connection or a non-ohmic (Schottky) contact resistance [17], manifest as a flattened characteristic at low V_{DS} in a transistor's output curve. An example is shown in **Figure 3.4a**. A model for contact resistance to explain the non-linear behaviour is shown in **Figure 3.4b** [13], in which parasitic Schottky diodes in series with the source or drain resistance cause the observed non-linearities [18, 19].

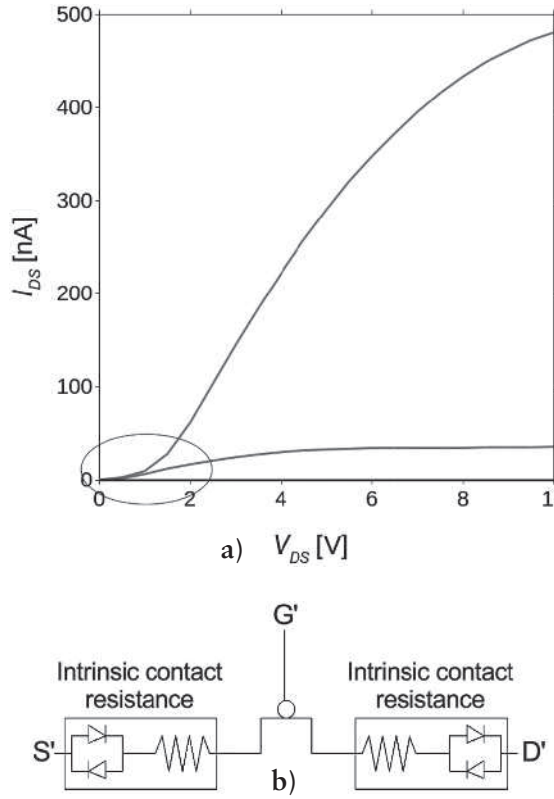


Figure 3.4 Contact resistance: (a) typical transistor output curves showing non-linear behaviour and (b) equivalent circuit with non-linear source and drain contact resistances [13]

3.7 Summary

In this chapter, the operation of organic transistors has been summarised. Transistor operating regions have been described, and the key parameters of mobility and V_T have been analysed. These concepts will be used for circuit design and simulation in the next chapters.

References

1. *The Nobel Prize in Physics*, Nobelprize.org, 1956. *http://www.nobelprize.org/nobel_prizes/physics/laureates/1956/*

2. J. Zaumseil and H. Sirringhaus, *Chemical Reviews*, 2007, **107**, 1296.

3. C.R. Newman, C.D. Frisbie, D. da Silva Filho, J-L. Brédas, P.C. Ewbank and K.R. Mann, *Chemistry of Materials*, 2004, **16**, 4436.

4. S. Abdinia, F. Torricelli, G. Maiellaro, R. Coppard, A. Daami, S. Jacob, L. Mariucci, G. Palmisano, E. Ragonese, F. Tramontana, A.H.M. van Roermund and E. Cantatore, *Organic Electronics*, 2014, **February**, 1.

5. P.E. Allen and D.R. Holberg in *CMOS Analog Circuit Design*, Holt, Rinehart & Winston, Inc., New York, NY, USA, 1987.

6. D. Braga and G. Horowitz, *Advanced Materials*, 2009, **21**, 1473.

7. D. Braga and G. Horowitz, *Applied Physics A Materials Science and Processing*, 2009, **95**, 193.

8. G. Horowitz, R. Hajlaoui, H. Bouchriha, R. Bourguiga and M. Hajlaoui, *Advanced Materials*, 1998, **10**, 923.

9. H. Sirringhaus, *Advanced Materials*, 2009, **21**, 3859.

10. A. Ortiz-Conde, F.J. Garcia Sanchez, J.J. Liou, A. Cerdeira, M. Estrada and Y. Yue, *Microelectronics Reliability*, 2002, **42**, 583.

11. D. Boudinet, G. Le Blevennec, C. Serbutoviez, J-M. Verilhac, H. Yan and G. Horowitz, *Journal of Applied Physics*, 2009, **105**, 084510.

12. V. Coropceanu and J-L. Brédas, *Nature Materials*, 2006, **5**, 929.

13. P.V. Necliudov, M.S. Shur, D.J. Gundlach and T.N. Jackson, *Journal of Applied Physics*, 2000, **88**, 6594.

14. E. Cantatore, T.C.T. Geuns, G.H. Gelinck, E. van Veenendaal, A.F.A. Gruijthuijsen, L. Schrijnemakers, S. Drews and D.M. de Leeuw, *IEEE Journal of Solid-State Circuits*, 2007, **42**, 84.

15. M. Estrada, A. Cerdeira, J. Puigdollers, L. Resendiz, J. Pallares, L. Marsal, C. Voz and B. Iniguez, *Solid State Electronics*, 2005, **49**, 1009.

16. D. Vasileska in *Mobility Modeling*, Arizona State University, Tempe, AZ, USA.

17. G. Horowitz, *Journal of Materials Research*, 2004, **19**, 1946.

18. T. Richards and H. Sirringhaus, *Journal of Applied Physics*, 2007, **102**, 094510.

19. M.S. Shur, D. Veksler, V. Chivukula and A. Koudymov, *Electrochemical Society Transactions*, 2007, **8**, 165.

4 Modelling and Simulation

4.1 Introduction

This chapter introduces the more abstract concepts of models, compact models, and parameter extraction. An example of how a physical model might be developed and used is presented after a study of an existing physical model.

Physical models and simulation algorithms are useful to help understand the behaviour of a material or device on a computer. By abstracting key physical parameters, models aid in the characterisation of materials and devices. Organic transistor behaviour is qualitatively similar to silicon transistor behaviour; however, the fundamentals are different, necessitating new physical models to be developed.

In general use, circuit simulation is performed at the transistor level, although it is acknowledged that this is only suitable when there are few devices in a circuit, as the computation overheads soon become severe with larger designs. And a note on the terminology – the mathematical equations are the *model*, and the computer software implementation is the *compact model*. Although these terms are not strictly adhered to in the literature, the meaning can be usually inferred from the context. Alternatively, there are circuit simulators that delve even deeper into the transistor by modelling devices directly at the level of the materials. These device simulators are used exclusively for research and development of the processing and fabrication and are not suitable even for a small circuit containing no more than a handful of devices.

4.2 Model Types

Models can be broadly split into three different classifications: physical, empirical, and table based. Each type of model has its own distinct advantages and disadvantages, which are listed below and summarised in **Table 4.1**. For example, the history of modelling in the silicon industry has swung from the first physical models (Shichman–Hodges), to the empirical [the very popular Berkeley short-channel IGFET model (BSIM), BSIM2, and HSPICE28], and back to the physical [BSIM3, Enz–Krummenacher–Vittoz (EKV)] [1]. The model used in this book and described later in this chapter is a physical model.

4.2.1 Physical

Physical models are derived from a first-principles study of the physics of the devices and of the characteristics of the measured data in order to arrive at a mathematical representation, or equation, of the terminal behaviour of the transistor. Usually there is considerable simplification of the physics in order to arrive at a working model, which may result in a model that does not fully agree with the experimental data. Although there may be some fine tuning and empirical fitting, most of the parameters are representative of a specific physical attribute, such as V_T or mobility. Having physical parameters will facilitate other simulations that would not be possible in table-based or pure empirical modelling, such as Monte Carlo modelling where a (physical) parameter is systematically altered across simulations. Physical models should, however, have as few parameters as possible [2] (leading to the oxymoron, 'A model shall be simple and accurate' [3]).

4.2.2 Empirical

In the most extreme and purest form, using only mathematical techniques, an equation is generated that fits the observed data. The skill of the programmer and capability of the algorithm determine the final form of the equation, although this may not be available to the user for further analysis, particularly if the algorithm or software is proprietary or confidential. A template equation may possibly be used, which may have been derived from a similar or related physical model and generally fits the expected data. There are companies such as Infiniscale that specialise in this type of data solving and modelling, from which very good (subjectively) data fitting is achievable. In any case, extracted parameters have little or no physical correspondence. Extrapolation outside the observed dataset is likely to be inaccurate.

4.2.3 Table-based Modelling [3]

The measured data are coded into a look-up table. Between data points, linear interpolation is used to estimate values. If the data points are closely spaced, then a reasonable prediction may be made. However, as with empirical models, behaviour beyond the observed boundaries is unreliable, and there are no physical parameters that may be extracted for further analysis. This form of modelling is simple to code for simulation purposes, although examples of the use of this type of model are rare.

Table 4.1 Qualitative comparison of model types against different criteria			
Criteria	**Physical**	**Empirical**	**Table-based modelling**
Time to first model	Very long	Moderate	Very quick
Parameter extraction	Might be difficult	Might be difficult	Easy
Parameters	Mainly physical	Little or no meaning	Have no meaning
Interpolation	Yes	Yes	Yes
Extrapolation	Yes	No	No
Simulation speed	OK	OK	Good

4.3 Organic Models

Having earlier discussed charge transport within organic semiconductors, the challenge now is to produce a model that can best describe the transistor's terminal behaviour. Simple modelling of an organic thin-film transistor (OTFT) is possible with the classic expressions used by silicon metal-oxide semiconductor (MOS) crystalline devices, sometimes with small empirical modifications. But OTFT differ from silicon devices in several ways, such as mobility changes with V_{GS} or V_{DS}. Non-linear behaviour due to non-ohmic source or drain contacts or injection barriers have already been discussed, and leakage currents have been observed to be greater than in silicon devices.

All these organic properties require new models to be developed, and work is ongoing in this area of research. **Table 4.2** is a selected list of publications where the authors have sought to address these challenges of OTFT modelling. For another recent perspective on these models and modelling, see the excellent review article by Kim and co-workers [4].

Table 4.2 Selected list of physical organic modelling papers		
Author – Year	**No. of citations**	**Comments**
Estrada – 2005 [5]	23	Used in a simulation of an organic inverter [12]
Fadlallah – 2006 [6]	11	Used to compare fully printed unipolar and complementary organic logic [13]
Mijalkovic – 2008 [7]	–	–
Yaghmazadeh – 2009 [8]	3	Similar to Estrada – 2005
Marinov – 2009 [9]	33	–
Torricelli – 2009 [10]	14	–
Marinov – 2013 [11]	4	Quasi-static model

4.4 Compact Modelling

After the theoretical aspects of model derivation have been discussed, and the mathematical equations have been formed to describe the transistor's operating regions, the equations must then be transcribed into computer software code for the simulation program with integrated circuit emphasis (SPICE) simulator. The code itself may take the form of a software programming language (such as C, or C++), or a hardware description language (HDL) (such as Verilog-A or very-large-scale integration HDL). (An HDL differs from a software programming language in that the HDL is primarily designed to code electronic circuits and includes the concept of time.) Compact models are more than a mere transcription of the equations into computer code. It is necessary to account for systematic or transient error conditions, such as negative values, negative logarithms, negative square-route functions, or division-by-zero. Any discontinuities between transistor operating regions, either in the source–drain current or in its derivative, will cause numerical problems, so transitioning between operating regions must be accomplished by smoothing functions.

Compact models should fulfil certain criteria in order to make simulation easier [14]:

- The models should consistently represent organic field-effect transistor (OFET) behaviour.
- The source–drain behaviour for a symmetrical OFET source–drain should be symmetrical.
- The models should be analytical, without integrals or differentiation.
- They should be simple and easily derivable.
- It should be easy to determine, or even to guess, the parameters.
- The models should be modular.
- It should be possible to justify the relations physically.

Compact models of transistors for circuit design are split into two parts, an intrinsic core and an extrinsic network (**Figure 4.1**). The intrinsic core of the model relates to the DC or static aspects of transistor behaviour. This is the part that the compact model equations have coded in a programming language. The extrinsic network is built around the intrinsic core using existing library components from the simulator and models the transient (time-dependent) and AC (frequency-dependent) effects. The extrinsic network may be captured as either a drawn schematic or as a netlist, which

is a textual representation of the schematic. Using the extrinsic network in this way, it should be possible to model other frequently observed behaviours of OFET, such as bias stress [15] and hysteresis [7].

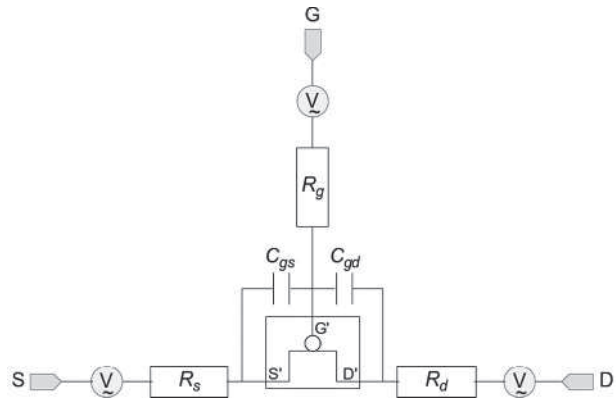


Figure 4.1 Compact model of a transistor structure, showing the intrinsic core and extrinsic network of resistors, capacitors, and noise source components

Intrinsic core features [16]:

- Smooth interpolation of current between regions;
- Gate-voltage-dependent parasitic resistance;
- Gate-voltage-dependent mobility;
- Source–drain leakage current model; and
- Physical temperature scaling.

Extrinsic network features [16]:

- Source–drain contact series resistance;
- Resistor and capacitor (RC) modelling for frequency;
- Overlap capacitance;
- Noise model; and
- Memory (charge storage) effects.

4.5 Parameter Extraction

Parameter extraction is the procedure by which the model parameters are calculated optimally to fit the measured transistor data. There are two primary sets of measurements that are required for transistor characterisation [6]: the transfer characteristic (I_{DS}–V_{GS}), and the output characteristic (I_{DS}–V_{DS}). The Institute of Electrical and Electronics Engineers standard IEEE1620-2008 [17] describes measurement and reporting standards for these types of measurement. Capacitance–voltage characterisation is sometimes used [11], but small values of capacitance make this a difficult measurement task. As well as a good model, it is important to have good parameter extraction. The consequences of a poor model or poor parameter extraction will lead to incorrect values being assigned to the model's physical parameters [2]. For this reason, in the literature, many models are also accompanied with a systematic manual parameter extraction method. However, there are also numerical methods that are used to extract model parameters. Numerical methods fall into two main categories: a least-squares approach, used in this book, and fuzzy logic parameter extraction [18, 19].

4.5.1 Manual Parameter Extraction

Most models have been designed with a view to easing the parameter extraction procedure, allowing the parameter extraction to be performed in a systematic and repeatable manner [6]. The techniques generally involve a gradient approximation or partial integration of the measurements. Usually, independent parameters are extracted first, then those parameters that have the most sensitivity, and finally the empirical and region-smoothing parameters. The sequence of parameter extraction, which may also be applicable to numerical methods, generally proceeds as follows:

1. Extraction of leakage and subthreshold parameters.
2. Extraction of the V_T.
3. Extraction of mobility.
4. Extraction of the source and drain resistance.
5. Extraction of the channel length modulation factor (output conductance).
6. Extraction of empirical and smoothing parameters.

One disadvantage of many manual parameter extraction procedures is that, once a parameter has been extracted, it is not usually altered or refined following subsequent

extraction of other parameters. Another disadvantage is that a parameter is sometimes calculated only from a specific portion of the measured data, ignoring that parameter's effect on the whole dataset. For example, a parameter relating to leakage current may only be extracted from data supposed to be in the subthreshold regions, but the leakage current parameter itself is still present in the model over all operating conditions.

4.5.2 Non-Linear Least-Squares

The non-linear least-squares (NLLS) method is based upon reducing the weighted sum of squared residuals (WSSR) between the measured data and the model function values (**Figure 4.2**). gnuplot was used in this book for NLLS parameter extraction. gnuplot reduces the WSSR until a finishing criterion is reached, e.g., until a small enough residual or an iteration limit is reached. As with manual parameter extraction, the model's parameters still need to be systematically approached. One major difference when compared with a manual parameter extraction method is that gnuplot is able to consider all datasets simultaneously. By combining transfer and output data into a single dataset, or by using multiple sets of data together, gnuplot is able to fit parameters based on more data.

Unlike fuzzy logic matching, NLLS extraction is only able to consider a few parameters during each optimisation run, so many optimisation runs are required with continual and repeated refining and tuning of extracted parameters. Fuzzy logic matching is able to consider the entire dataset and all parameters simultaneously (not used in this book).

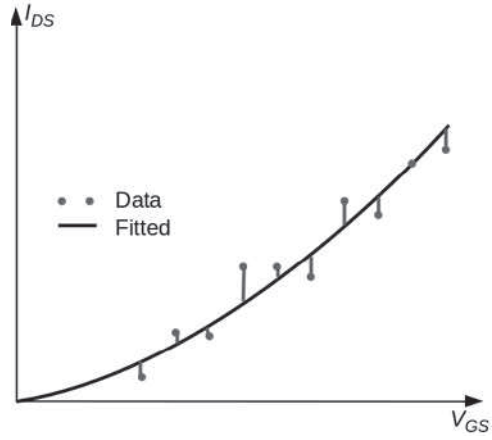


Figure 4.2 An example of fitting by reducing the sum of squared residuals (least-squares fitting)

4.6 Modelling

In this section, an existing model is modified to demonstrate how a model may be used for circuit simulation. Owing to its simplicity, its similarities with the classic MOS equations, and its modular design, the model by Estrada [5] is an excellent starting point. To the Estrada model, empirical adjustments can be made for subthreshold operation and interdomain transitions. This new model is designated here as *est2005c*.

4.6.1 Classic MOS Model

The classic MOS equations introduced in **Chapter 3** are plotted in **Figure 4.3**. It is clear that, owing to the lack of smoothing functions, there are discontinuities in the channel current that will cause abrupt changes between operating regions. The SPICE simulator, which is described in the **Appendix**, depends upon a continuous function and its derivative in order numerically to solve for simulation. While the classic MOS expressions serve well for a first-order manual analysis of transistor behaviour, they are not entirely suitable for computer modelling.

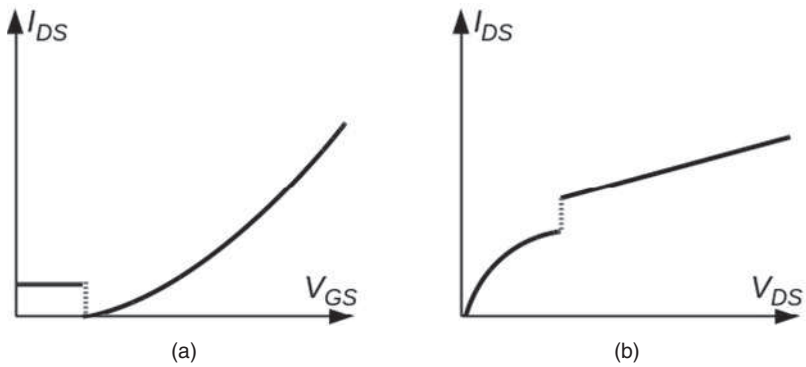


Figure 4.3 The classic MOS equations plotted as (a) a transfer curve in saturation and (b) as an output curve

4.6.2 Intrinsic Core

The derivation and modifications to create the est2005c model are now explained. Firstly, a gate-voltage-dependent model for mobility [20] is introduced as a basic definition, previously described in **Chapter 3** but slightly modified for the compact model:

$$\mu = \mu_0 \left(\frac{V_{GS} - V_T}{V'_{aa}} \right)^{\gamma} \tag{4.1}$$

where $V'_{aa} = e^{V_{aa}}$ in order to prevent a negative value. For parameter extraction by a numerical method (e.g., the least-squares method), negative values may be transiently seen by the algorithm as it seeks the optimal solution. To prevent these unwanted negative values, the exponential substitution is made to restrict the search to positive values only.

To declutter the coming equations, a transistor gain factor is as previously defined:

$$\beta = \left(\mu C_{diel}\right)\frac{W}{L} = \left(\mu\frac{\varepsilon_r\varepsilon_0}{d_{diel}}\right)\frac{W}{L} \tag{4.2}$$

The model for the linear and saturation regions by Estrada [5] is

$$I_{DS}\left(lin, sat\right) = \beta\frac{\left(V_{GS} - V_T\right)}{\left(1 + R\beta\left(V_{GS} - V_T\right)\right)}\frac{V_{DS}\left(1 + \lambda V_{DS}\right)}{\left[1 + \left[\frac{V_{DS}}{V_{DSsat}}\right]^m\right]^{1/m}} + I_0 \tag{4.3}$$

where I_0 is a constant fixed leakage current, λ is the channel length modulation parameter, m is a fitting parameter to smooth the transition between the linear and saturation operating regions, and α is the saturation modulation parameter such that the saturation voltage $V_{DSsat} = \alpha(V_{GS} - V_T)$. Non-ohmic contacts present at the source and drain are modelled by $1 + R\beta(V_{GS} - V_T)$ in the denominator.

However, this model is only valid for the above threshold regions without any subthreshold operation apart from a constant current leakage model. The abrupt change to the constant leakage current will cause numerical problems in the simulator. For subthreshold modelling, **Equation 4.4** from the EKV model [21] is added:

$$V_{transfer} = \ln\left[1 + e^{(V_{GS} - V_T)}\right] \tag{4.4}$$

For large values of $V_{GS} - V_T$ (above threshold), **Equation 4.4** is approximately equal to $V_{GS} - V_T$. For small values of $V_{GS} - V_T$ (subthreshold), $V_{transfer}$ is approximately equal to $e^{(V_{GS} - V_T)}$ (from the Taylor series), while for very small values of $V_{GS} - V_T$, $V_{transfer}$ approximates to 0.

To improve leakage current modelling, the leakage current is observed to vary with V_{DS}. This can be easily modelled:

$$I_{leak} = \frac{V_{DS}}{R'_0} \tag{4.5}$$

where $R'_0 = e^{R_0}$, again to prevent a negative value.

Negative values in $V_{GS} - V_T$ will cause unwanted sign changes in the I_{DS} current. A minimiser function [22] is added to prevent negative values:

$$V_{GT} = \left(\frac{V_{min}}{2}\right)\left[1 + \frac{V_{GS} - V_T}{V_{min}} + \sqrt{\delta^2 + \left(\frac{V_{GS} - V_T}{V_{min}} - 1\right)^2}\right] \tag{4.6}$$

This allows V_{GT} smoothly to approach V_{min} without being less than V_{min}. At large values of V_{GS}, $V_{GT} = V_{GS} - V_T$. So,

$$1 + R\beta\left(V_{GS} - V_T\right) \rightarrow 1 + R'\beta V_{\mathrm{GT}} \tag{4.7}$$

$$V'_{DSsat} = \alpha V_{\mathrm{GT}} \tag{4.8}$$

where $R' = \mathrm{e}^R$.

Putting it all together for est2005c:

$$I_{DS} = \beta \frac{\ln\left(1 + \mathrm{e}^{(V_{GS} - V_T)}\right)}{\left(1 + R'\beta\left(V_{GS} - V_T\right)\right)} \frac{V_{DS}\left(1 + \lambda V_{DS}\right)}{\left[1 + \left[\frac{V_{DS}}{V'_{DSsat}}\right]^m\right]^{1/m}} + I_{leak} \tag{4.9}$$

To analyse est2005c, the model is deconstructed in **Table 4.3** and compared with the classic MOS model. The linear and saturation regions of the deconstructed est2005c can be considered together. The classic MOS saturation model is conventionally related to the linear model by substituting $V_{DS} = (V_{GS} - V_T)$. This is also the case for est2005c, except the saturation model has an extra α saturation term which is usually close to unity (see later parameter extraction), and an extra channel length modulation term $(1 + \lambda V_{DS})$ in the linear model. The source–drain contact resistance term $[1 + R'\beta(V_{GS} - V_T)]$ is present in the est2005c subthreshold, linear, and saturation models. The subthreshold model has an exponential term for gate voltage but little effective empirical parameter control. The leakage model is an improvement on the constant fixed model of the classic expressions.

Table 4.3 Deconstructed model compared against the classic MOS model in the different operating regions		
Operating regime	**Classic MOS model**	**est2005c**
Leakage $V_{GS} << V_T$	I_0	V_{DS}/R_0
Subthreshold $V_{GS} < V_T$	$I_{s0}\mathrm{e}^{\frac{V_{GS}}{nkT/q}}$	$\alpha\beta\frac{(V_{min}(1+\lambda V_{DS})}{1+R'\beta V_{min}}e^{(V_{GS}-V_T)}$
Linear $V_{GS} \geq V_T$ $V_{DS} < V_{GS} - V_T$	$\beta\left[(V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right]$	$\beta\frac{(V_{GS}-V_T)V_{DS}(1+\lambda V_{DS})}{1+R'\beta(V_{GS}-V_T)}$
Saturation $V_{GS} \geq V_T$ $V_{DS} \geq V_{GS} - V_T$	$\frac{1}{2}\beta(V_{GS}-V_T)^2(1+\lambda V_{DS})$	$\alpha\beta\frac{(V_{GS}-V_T)^2(1+\lambda V_{DS})}{1+R'\beta(V_{GS}-V_T)}$

4.6.3 Extrinsic Network

The extrinsic network is as shown in **Figure 4.1**. Instead of a fixed value for every transistor's parasitic gate-source and gate-drain overlap capacitances, C_{gs} and C_{gd} can be calculated from the total gate area coupled to the source or drain or channel area, which can be estimated from the dimensions of the transistor:

$$C_{gs} = C_{gd} = \frac{1}{2}\frac{\varepsilon_0\varepsilon_r A}{d} \tag{4.10}$$

where ε_r is the dielectric constant, d is the thickness of the dielectric, and A is the total gate metal area, which is product of the width of the transistor channel and the sum of metal gate track width. The parasitic series resistances R_s and R_d represent the short metal tracks connecting to the source and drain respectively.

4.7 Transistor Measurements and Parameter Extraction Results

Model validation is an important part of the model flow. In order properly to verify the model equations and simulation, the model should be checked against measured data. The validation of the model is in three parts:

1. Comparison of extracted model parameters μ and V_T against manually calculated values. This will not be an exact comparison, as the model parameters have some gate-voltage dependence whereas the manually calculated values do not. Also, a check should be made of the simulated and measured transistor currents.

2. Comparison of DC transfer characteristics for an inverter.

3. Comparison of transient switching behaviour, for example, for an inverter or a ring oscillator.

The first part of the validation is analysed in this section, parts 2 and 3 are analysed in later chapters. An example of the result of the model parameter extraction for transistors is presented in **Figure 4.4**. A comparison of the extracted parameters and manually calculated values is presented in **Table 4.4**. It should be noted that there are technological, processing, and fabrication differences between all foil samples, so variations in parameters is to be expected.

In general terms, the fit for all samples is subjectively better at higher values of I_{DS} than at lower values. This is to be expected as a consequence of the NLLS parameter extraction which attempts to reduce the WSSR in which the higher values of I_{DS} contribute more than smaller values of I_{DS}.

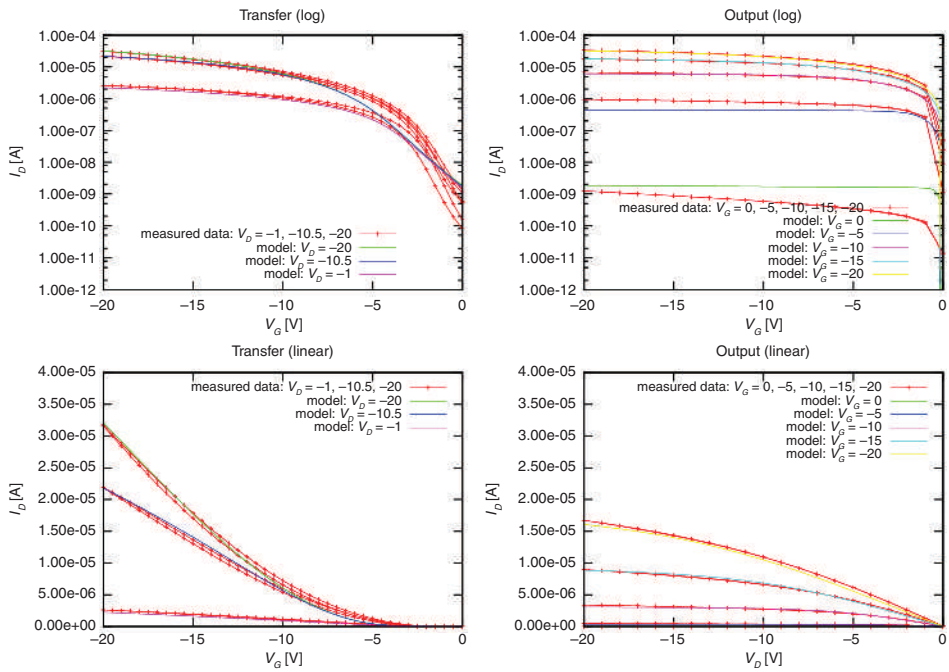


Figure 4.4 Example of fitting results for transfer and output curves, in linear and logarithmic scales

Table 4.4 Comparison of transistor parameters from the model parameter extraction for the different foil samples against manually calculated values. Where applicable, $V_{GS} = V_{DS} = 20$ V

Quantity	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Units
V_T	-6.0	-7.6	-3.8	-4.9	-6.4	V
μ_0	1.71e-2	1.89e-3	1.78e-2	1.02e-1	6.05e-2	cm^2/Vs
$V'_{aa} = e^{V_{aa}}$	7.33e13	21.1	8.79e-16	13.4	12.4	—
γ	-6.65e-4	0.69	-1.46e-3	1.35	0.29	—
$R' = e^R$	6.19e4	2.39e4	6.28e4	3.03e4	2.10e4	Ω
λ	1.61e-3	2.41e-4	4.17e-4	1.00e-5	3.93e-3	V^{-1}
α	1.03	1.01	1.03	1.17	0.99	—
m	9.26	3.05	2.91	3.54	3.69	—
$R'_0 = e^{R_0}$ (fix)	7.20e10	7.20e10	7.20e10	7.20e10	3.58e9	Ω
V_{min} (fix)	-0.2	-0.2	-0.2	-0.2	-5.7	V
δ	10.0 (fix)	3.0 (fix)	10.0 (fix)	9.83	0.21	—
Width/length	12 mm/5 µm	12 mm/5 µm	12 mm/5 µm	3.2 mm/4.5 µm	2.5 mm/4.5 µm	—
Model $\mu = \mu_0 [(V_{GS} - V_T)/V_{aa})^{\gamma}]$	0.017	0.0013	0.017	0.120	0.062	cm^2/Vs
Manual μ_{fet} (**Equation 3.14**)	0.014	0.0011	0.012	0.137	0.070	cm^2/Vs
V_T ELR method (**Equation 3.7**)	-5.3	-10.2	-2.2	-4.0	-3.8	V
V_T ESR method (**Equation 3.9**)	-5.5	-7.2	-3.2	-8.5	-7.9	V
Measured I_{DS}	29.1	7.2	31.7	205	91.1	µA
Model I_{DS}	30.1	7.1	32.1	196	89.0	µA
Final WSSR	5.3231e-10	4.4035e-11	1.0834e-10	2.0570e-9	2.7547e-10	μA^2

Foil samples are from different technologies

ELR: Extrapolation of linear region

ESR: Extrapolation of saturation region

An inspection of the individual extracted parameters is quite revealing. Sample 4 has the greatest gate-voltage dependence (highest γ), but sample 1 has a slightly negative gate-voltage dependence. Sample 3 needed the least smoothing between linear and saturation regions (lowest m), but samples 1, 3, and 4 needed plenty of smoothing between subthreshold and above-threshold operation (highest δ), where as sample 5 hardly required any subthreshold/above-threshold smoothing (lowest δ).

The V_T values are manually calculated from **Equations 3.7** and **3.9**, and also compared with the value extracted for the model. The model's mobility parameter is modified by the V_{GS}, so a comparison extracted model mobility value is derived with V_{GS} = 20 V (**Equation 4.1**) and other values are as extracted for the model. There are discrepancies between the model's extracted values and the manually estimated values of mobility and V_T. Some of this is due to the notorious difficulty of estimating mobility by manually fitting to the ideal classic MOS equations [23]. However, a greater source of difference is a glance at the γ parameter, which is a measure of the variation due to gate voltage (**Equation 4.1**). A value closer to zero in this parameter indicates lesser V_T dependence on gate voltage.

4.8 Summary

In this chapter, the basis of transistor modelling for simulation has been introduced. The three different styles of compact modelling – physical, empirical, and table based – have been explained. A new physical model has been developed to allow the accurate estimation of circuit performance over all operating regions. Measurements from five foil designs were made, model parameters were extracted, and good correlation between extracted model parameters and manually calculated process parameters was confirmed. This model will be used in subsequent chapters to evaluate circuit designs.

References

1. C. Galup-Montoro and M.C. Schneider in *MOSFET Modeling for Circuit Analysis and Design (International Series on Advances in Solid State Electronics and Technology)*, World Scientific Publishing, Singapore, 2007.

2. Y.P. Tsividis and K. Suyama, *IEEE Journal of Solid-State Circuits*, 1994, **29**, 210.

3. W. Liu in *MOSFET Models for SPICE Simulation including BSIM3v3 and BSIM4*, Wiley-Blackwell, Hoboken, NJ, USA, 2001.

4. C. Kim, Y. Bonnassieux and G. Horowitz, *IEEE Transactions on Electron Devices*, 2014, **61**, 278.

5. M. Estrada, A. Cerdeira, J. Puigdollers, L. Resendiz, J. Pallares, L. Marsal, C. Voz and B. Iniguez, *Solid-State Electronics*, 2005, **49**, 1009.

6. M. Fadlallah, W. Benzarti, G. Billiot, W. Eccleston and D. Barclay, *Journal of Applied Physics*, 2006, **99**, 104504.

7. S. Mijalkovic, D. Green, A. Nejim, G. Whiting, A. Rankov, S. Smith, J. Halls and C. Murphy in *Proceedings of the 26th International Conference on Microelectronics, MIEL 2008*, 11–14th May, Niš, Serbia, 2008, p.469.

8. O. Yaghmazadeh, Y. Bonnassieux, A. Saboundji, B. Geffroy, D. Tondelier and G. Horowitz, *Journal of the Korean Physical Society*, 2009, **54**, 523.

9. O. Marinov, M.J. Deen, U. Zschieschang and H. Klauk, *IEEE Transactions on Electron Devices*, 2009, **56**, 2952.

10. F. Torricelli, Z.M. Kovacs-Vajna and L. Colalongo, *IEEE Transactions on Electron Devices*, 2009, **56**, 20.

11. O. Marinov and M. Jamal Deen, *Organic Electronics*, 2013, **14**, 295.

12. N.P. Papadopoulos, A. Marsal, R. Picos, J. Puigdollers and A.A. Hatzopoulos, *Solid-State Electronics*, 2012, **68**, 18.

13. M. Hambsch, K. Reuter, H. Kempa and A.C. Hübler, *Organic Electronics*, 2012, **13**, 1989.

14. O. Marinov and M. Deen, *IEEE Transactions on Electron Devices*, 2009, **56**, 2952.

15. H. Sirringhaus, *Advanced Materials*, 2009, **21**, 3859.

16. S. Mijalkovic, D. Green, A. Nejim, A. Rankov, E. Smith, T. Kugler, C. Newsome and J. Halls in *International Conference on Organic Electronics*, Liverpool, UK, 2009, p.17.

17. IEEE1620, *IEEE Standard for Test Methods for the Characterization of Organic Transistors and Materials*, Institute of Electrical and Electronics Engineers, New York, NY, USA, 2008.

18. R. Picos, B. Iniguez, E. Garcia-Moreno, R. Garcia and M. Estrada in *Proceedings of the Mixed Design of Integrated Circuits and System International Conference*, Gdynia, Poland, 2006, p.159.

19. R. Picos, O. Calvo, B. Iñiguez, E. García-Moreno R. García and M. Estrada, *Solid-State Electronics*, 2007, **51**, 683.

20. P.V. Necliudov, M.S. Shur, D.J. Gundlach and T.N. Jackson, *Journal of Applied Physics*, 2000, **88**, 6594.

21. C.C. Enz, F. Krummenacher and E.A. Vittoz, *Analog Integrated Circuits and Signal Processing*, 1995, **8**, 83.

22. B. Iniguez, R. Picos, M. Estrada, A. Cerdeira, T. Ytterdal, W. Jackson, A. Koudymov, D. Veksler and M.S. Shur in *Proceedings of the Mixed Design of Integrated Circuits and System International Conference*, Ciechocinek, Poland, 2007, p.35.

23. H. Sirringhaus in *Advanced Materials*, January 2014, 25th Anniversary Article.

5 Circuit Design

5.1 Introduction

At the first Caltech Conference on silicon very-large-scale integration (VLSI) in January 1979, Carver Mead (then Professor of Computer Science, Electrical Engineering, and Applied Physics, California Institute of Technology, CA, USA) spoke about the need for the silicon VLSI industry to separate the designing of chips from the manufacturing of chips [1], with clear delineation between design and fabrication, and a clean interface between the two. He recognised that innovation by small insular groups could not be achieved quickly if each group was required to design and fabricate its own devices. His ideas later became the landmark book *Introduction to VLSI Systems* by Carver Mead and Lynn Conway [2].

His comments on the nascent silicon VLSI industry are prescient to today's fledgling organic electronics industry, where the number of integrated transistors on a foil is closely following Moore's law, doubling approximately every 2 years (**Chapter 1**, **Figure 1.1**). Much of the current organic transistor circuit design industry is drawn, not from the silicon VLSI industry, but from the printing and printed circuit board industries. However, integrated circuit design differs from discrete component-level design in two important ways. Firstly, the integrated chip designer is able to alter all the parameters of every component. This gives the designer immense flexibility. Secondly, it is not possible to breadboard or prototype the design. This now lends greater importance to a 'right first time' design approach including accurate simulation and design verification [3].

Mead and Conway advocated several important concepts, some of which are addressed in this chapter:

- Simplified design methods – applicable to large-scale designs where a top-down partitioned approach is necessary.
- Digital data formats – clearly defined with universal standards.
- Scalable design rules – simplification of design rules based on multiples of a single global design constant, λ.

- Clean interfaces between design and manufacturing – the separation of the design process from the fabrication.

- Widely accessible foundries – easily accessible fabrication facilities with a common data interface.

- Multichip projects – quick prototyping service.

It transpired that not all these ideas were practical. For example, λ-based scalable design rules were not ever really widely adopted. And several ground-breaking developments were completely missed altogether, such as [1]:

- High-level hardware description language (HDL) – an HDL allows for the design of (digital) logic by a design or programming language in a similar manner to conventional software development. Prior to the adoption of HDL, logic designs were usually hand crafted at the logic gate level.

- Formal methods – with the introduction of HDL, many of the errors that afflict software programming, as well as conventional design, became more apparent. For example, unintended logic paths in branched statements or insufficient error handling. By making use of mathematical methods and strict programming protocols, more robust designs can be achieved.

- Logic synthesis and place-and-route – increasing computer processing power allowed for design at higher levels with lower-level implementations handled by software algorithms.

Previous chapters have discussed the theory behind organic transistor design. Now, all these concepts must be brought together and used effectively. In this chapter, a coherent modelling ecosystem and a design flow are presented. The difficulties of process and operating variations are discussed, and then the issues of testability and prototyping are briefly touched upon.

5.2 Design Flow

In order to design circuits beyond a handful of devices, it is necessary to be able accurately to predict the behaviour of the intended design, and then reliably to fabricate the design. With mask-based designs still prevalent, non-recurring engineering costs can be high and mask-making is time consuming. On-demand processing, such as inkjet printing, will ease the costs and shorten timescales, but it is still advantageous to fabricate correctly first time.

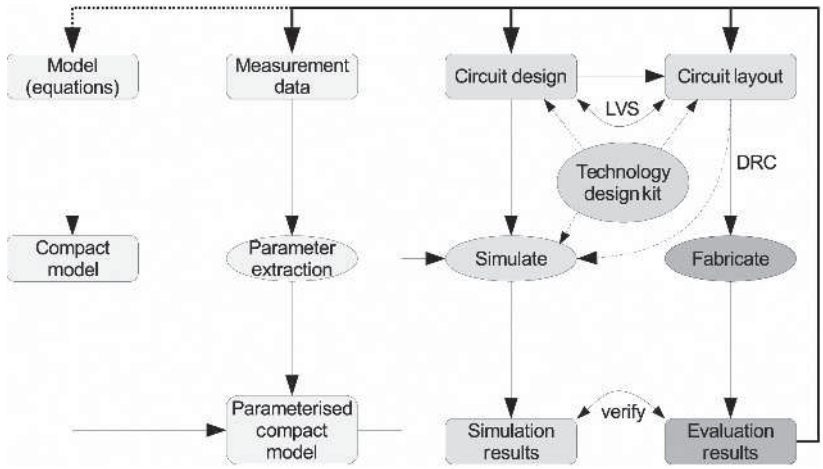


Figure 5.1 Modelling and circuit design flow

To make this possible, a design flow is necessary. The design flow is the combination of design tools (software) and methodologies to design and build a circuit. Some of the primary functions of the design flow are to capture the schematic and layout views, perform functional and performance simulations, and check for errors and consistency. The design flow in **Figure 5.1** is now described. Most circuit design begins with schematic entry, and from this a netlist is produced for simulation in a simulation program with an integrated circuit emphasis (SPICE) circuit simulator. The technology design kit (TDK) is not a single file but a collection of the rules, conventions, and control files that allows a designer to use the technology. A TDK is targeted specifically for a particular electronic design automation (EDA) software suite. When satisfied with the schematic design, the circuit layout is produced. This is a time-consuming task. Design rule checks (DRC) and layout *versus* schematic (LVS) consistency checks ensure the layout is correct. Optionally, the parasitics from the layout can be extracted and used for a more accurate SPICE simulation for further surety of design. From the layout, the foil is fabricated and the sample's evaluation results are checked against the simulation results. Discrepancies between the two sets of results are used further to enhance the model or the model parameters.

Out of necessity, a great deal of software is required. The scale and complexity of designing dictate that a full VLSI design suite capable of schematic and layout capture, with verification capabilities such as DRC and LVS, is required. A SPICE circuit simulator with custom modelling features may also be desirable. A typical set of freely available EDA tools for a Linux-based operating system is listed in **Table 5.1**, and these are used for the later examples.

Table 5.1 EDA software		
Purpose	**Software**	**Version**
Operating system	Ubuntu	12.04 LTS
Circuit simulator	ngspice	26
Custom modelling	Xspice	1.0
Schematic/layout entry	Electric VLSI	9.04
Design verification (DRC/LVS)	Electric VLSI	9.04
Model parameter extraction	gnuplot	4.4

5.2.1 SPICE

The circuit simulator used was ngspice [4]. ngspice is an open-source, mixed-level, mixed-signal circuit simulator ideal for transistor-level simulations. Also, it is one of the few SPICE simulators that can accept custom models, which is achieved with the addition of the Xspice [5] extensions. SPICE internal algorithms are explained more fully in the **Appendix**.

5.2.2 Electric VLSI Design System

The Electric VLSI [6] EDA system was selected as the primary EDA tool suite. Electric was originally created by Steven Rubin in 1982, was then supported by Sun Microsystems from 1999 onwards, and is now maintained by Oracle Corporation following their takeover of Sun in 2010. Electric is an open-source and complete chip design tool suite available for free, though not without its quirks and bugs. Rather uniquely, it is implemented in Java, and as such is largely independent of the operating system.

The schematic capture tools within Electric are conventional, but the layout editor offers a different connectivity-driven approach. This scheme allows Electric to provide an efficient DRC and LVS implementation. Before Electric could be used for design and layout, it was necessary to create a TDK. A TDK captures all the rules and layers associated with a technology. In Electric, a custom TDK was created containing definitions for schematic and layout objects. This includes:

- Layer definitions, including Graphic Database System II layers and visual representations;
- Wire and via (a connection between layers) definitions;

- Transistor definitions; and
- DRC/LVS rules.

5.2.3 gnuplot

gnuplot is a curve plotting and fitting program used extensively here to fit measured transistor data to the transistor model equations. As the model parameters are not independent of each other, gnuplot uses a non-linear least-squares algorithm to fit the data to the function by minimising the weighted sum of squared residuals (WSSR). New parameter values are chosen by gnuplot's built-in Marquardt–Levenberg algorithm until some ending criterion is satisfied; for example, the change in WSSR is below a predefined threshold, or a maximum number of iterations has been reached [7].

5.3 Modelling Ecosystem

The modelling environment is based on ngspice–Xspice and gnuplot, plus some custom glue software (**Figure 5.2**). There are two disparate environments necessary for the entire model flow. The SPICE environment is where the circuit design and simulation occurs, while the gnuplot environment's main contribution is the fitting of experimental data and parameter extraction.

The genesis of the compact model is the SPICE C model and its interface specification. These are standard C code modules but written in such a way that a custom program is able to translate the model into a gnuplot model. The gnuplot model is fitted to measured data to extract the model parameters, which are translated back into SPICE C model parameters. The SPICE C model is now ready for use by the SPICE simulator. A simulation is performed to compare the SPICE simulation result with the gnuplot fitting result, which in turn is compared with the original measured data.

If a custom model is not wanted, then a standard silicon model may be used instead. Typically, this might be an amorphous silicon model (which is not available in ngspice) or even a crystalline silicon model such as the Berkeley short-channel IGFET model, BSIM3. Although these models will differ from organic device behaviour in areas such as temperature dependence and gate-voltage-dependent mobility, their overall characteristics are an approximate match for the organic transistor characteristics.

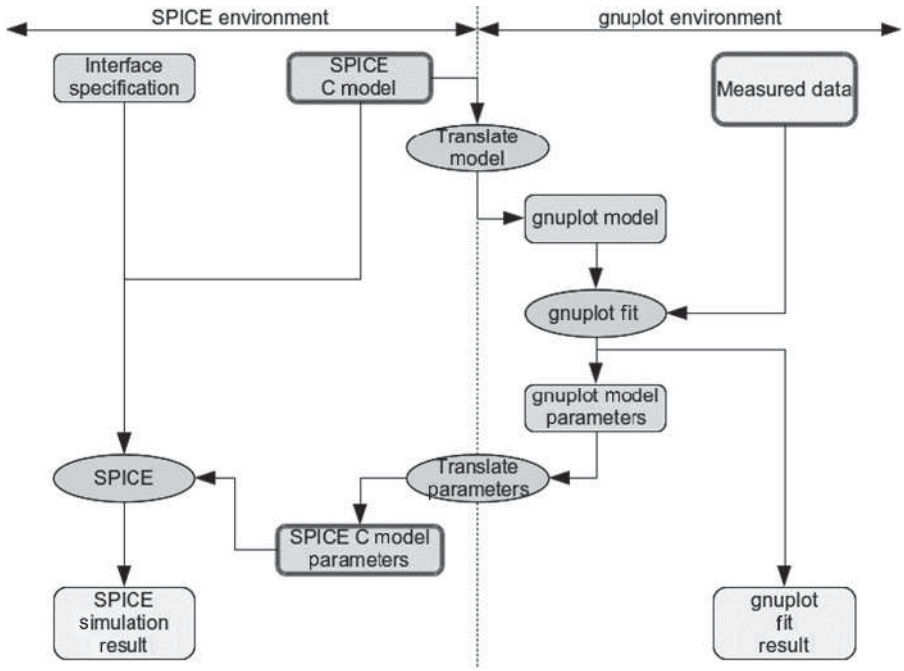


Figure 5.2 Modelling ecosystem

5.4 Design Tolerances

It is not possible to fabricate circuits to a single specification point and then operate at a single particular operating condition [8]. There are device-to-device, foil-to-foil, or batch-to-batch variations due to electrical, lithographic, or timing differences during fabrication, and over time the ageing of materials will affect circuit performance. Additionally, day-to-day environmental operating conditions such as voltage or temperature will vary, although absolute limits can be specified to bound the minimum and maximum design parameters.

As process parameter variations are statistical in nature, this can be used to determine the minimum and maximum parameter values for the purposes of design. Process tolerances follow a Gaussian distribution, so the minima and maxima are normally selected at the $\pm 3\sigma$ [standard deviation(s) (SD)] points of a given process parameter, which will cover 99.73% of fabricated devices.

While the absolute value of a process parameter may vary, mismatch between equally designed devices on the same foil is another important consideration.

This mismatch is the result of several random processes that occur during every fabrication phase [9, 10], but transistor performance is dominated by mismatch in V_T [11]. The mismatch in V_T can be traced back to a physical origin. For silicon devices, V_T mismatch is caused primarily by non-uniform distribution of dopants in the silicon crystal, following a Poisson distribution [12]. There are no dopants in organic devices, but the equivalent mechanism could be hypothesised to be a Poisson distribution of traps, crystallites, or polymer chains. The SD of V_T and transistor gain factor is given by [9]:

$$\sigma(V_T) = \frac{A_{V_T}}{\sqrt{(WL)}}$$
$$\frac{\sigma(\beta)}{\bar{\beta}} = \frac{A_\beta}{\sqrt{(WL)}} \tag{5.1}$$

where $\sigma(V_T)$ and $\sigma(\beta)$ are the SD of the V_T and the transistor gain factor respectively, β is the average transistor gain factor, A_{VT} and A_β are area proportionality constants, and W and L are the width and length of the transistor.

There are two types of analysis that may be performed to account for design tolerances: Monte Carlo and worst case [8]. A comparison of Monte Carlo and worst-case simulations for a ring oscillator is shown later, in **Chapter 6**.

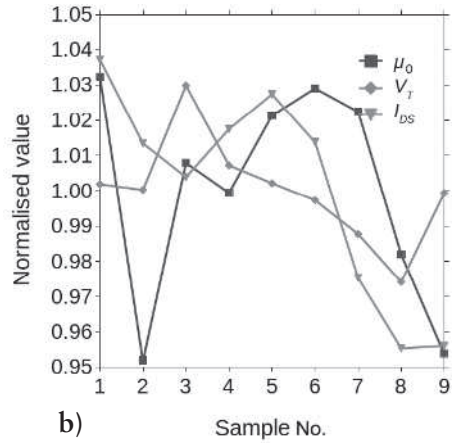
5.4.1 Monte Carlo

A Monte Carlo SPICE simulation statistically alters selected device or model parameters according to the desired distribution. Several different distribution types are available, such as random, Gaussian, or Poisson. Typically, many more simulations are performed in Monte Carlo analysis than for worst-case analysis. However, Monte Carlo simulations are additionally able to provide yield information on the design.

For the Monte Carlo simulations and yield analysis performed later, measurements were made of nine transistors from the same sample (**Figure 5.3**). Extractions of the model parameters from each transistor were used to calculate the mean and SD of the primary performance parameters μ_0 and V_T. As the calculated SD is only applicable to this single transistor size, and lacking any additional data, the SD of other transistor sizes must be estimated using **Equation 5.1**.

No	μ_0 [cm²/Vs]	V_T [V]	I_{DS} [µA]
1	1.78e-02	-3.82	31.65
2	1.64e-02	-3.81	30.93
3	1.74e-02	-3.93	30.63
4	1.73e-02	-3.84	31.05
5	1.76e-02	-3.82	31.35
6	1.78e-02	-3.80	30.94
7	1.77e-02	-3.77	29.76
8	1.70e-02	-3.72	29.16
9	1.65e-02	-3.81	29.18
Mean	1.73e-02	-3.81	30.52
SD	5.04e-04	0.0535	0.8708

a)



b)

Figure 5.3 Measurements from nine transistors: (a) absolute extracted model parameters (mobility, V_T) and measured source–drain current at 20 V and (b) normalised extracted model parameters and measured source–drain current at 20 V

5.4.2 Worst Case

In a worst-case analysis, a simulation is performed for every possible combination of minimum, maximum, and occasionally typical parameter variation. As each simulation parameter has a minimum and maximum value, then for n simulation corners the number of simulations is 2^n. However, the main problem with the worst-case approach is that the probability of all individual corners occurring together is extremely remote, though not impossible. The outcome is that worst-case design results in overengineered products that are difficult to simulate correctly across all worst-case corners. An example of the worst-case corners, calculated at the $\pm 3\sigma$ points and assuming independence of parameters, is shown in **Table 5.2**.

Table 5.2 Example values of worst-case process corners

No.	Design parameter	Symbol	Minimum	Maximum	Unit
1	Mobility	μ_0	1.58e-2	1.88e-2	cm²/Vs
2	Threshold-voltage	V_T	-3.65	-3.97	V
Total corners for simulation			$2^2 = 4$		

5.5 Layout Design

The goal of layout design is to produce a compact and efficient physical representation of the schematic design. For transistor-level design layout, this is a manual full-custom layout, more euphemistically known as polygon pushing. Unfortunately, this is a time-consuming and error-prone task. However, EDA tools such as DRC and LVS can find and eliminate layout errors, ensuring design consistency.

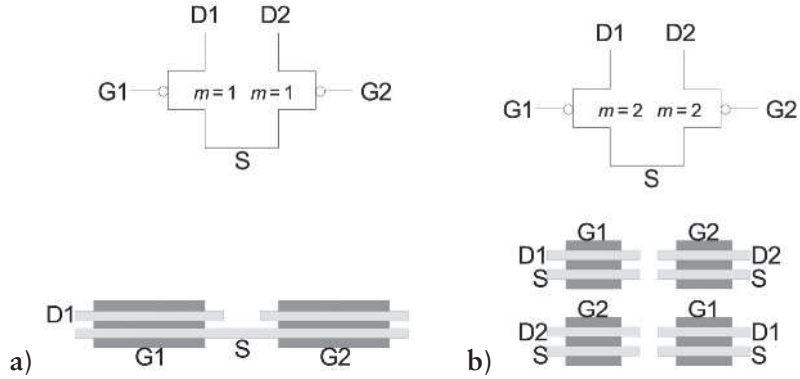


Figure 5.4 Full custom layout examples: (a) typical layout and (b) common centroid layout minimising gradient effects

Design tolerances were discussed in the previous section regarding their effect on the design and simulation of systems. While variation across batches or foils is outside the influence of the layout designer, mismatches within a single foil can be minimised. Mismatches occur as a result of some physical cause, which may be random, systematic, or from gradients in temperature, pressure, or fabrication. Common centroid layout techniques try to ensure that any systematic or gradient effects are distributed identically to all parts of all devices, and thereby its effects are minimised or even cancelled out. For example, the layout in **Figure 5.4a** has not employed any common centroid layout techniques. A gradient from left to right would affect the two transistors differently, while a top-to-bottom gradient would affect both transistors equally. By contrast, the layout in **Figure 5.4b** uses common centroid methods such that a left-to-right gradient would affect both transistors equally, as would a top-to-bottom gradient. Other features of the common centroid layout are as follows:

- It ensures that currents of all transistors are in the same direction.

- It splits transistors into smaller, identical units, and distributes them evenly.
- The coincident layout ensures that the centres of the two distributed devices are at the same coordinate.

In addition, there may be guard or dummy devices around the periphery of the layout for further reduction in any edge effects, ensuring that even the devices at the periphery of the matrix of transistors have the same neighbours as those within the matrix.

5.6 Design for Test

The mantra of testability is accessibility and observability. In a fabricated circuit, it is imperative that all nodes are accessible by the test system, and that all nodes are observable by the test system. For a packaged sample, this might mean the only physical access points are the input or output pins. Clearly, there cannot be direct physical access to all nodes, so access should be made available indirectly through test transparent logic. An inverter is an example of a gate that has test transparency in that any change in its input is reflected by a change in its output. A two-input NAND gate may not be test transparent, as a change in only one of the inputs does not always cause a change in the output. However, if one input is logic-1, then the two-input NAND becomes test transparent.

In a prototype or demonstrator organic foil, there may be full access to all top-level metal features, so the layout should bring all important nodes to appropriate test points. However, there may only be four probes available (including power and ground), so now the issue becomes one of designing a test mode into the logic to minimise the number of required test points. An example of a testable differential amplifier is given in **Figure 5.5**. In **Figure 5.5a**, the differential amplifier has no additional testability measures and will require six probes to test: power, ground, three inputs, and one output. In the testable differential amplifier, **Figure 5.5b**, two of the six inputs are provided on foil by resistor voltage dividers, reducing the number of probes required to four.

For more complex digital and analogue logic, built-in test features are necessary. In a system known as scan test, a connected chain of shift registers allows a pattern to be serially scanned into the circuit, the test is performed, and then the result is scanned out and checked for faults. For built-in self-test, a pseudorandom pattern generator would provide input to a region of combinatorial logic whose output is collected to generate a signature that can be compared with a previously simulated result [13].

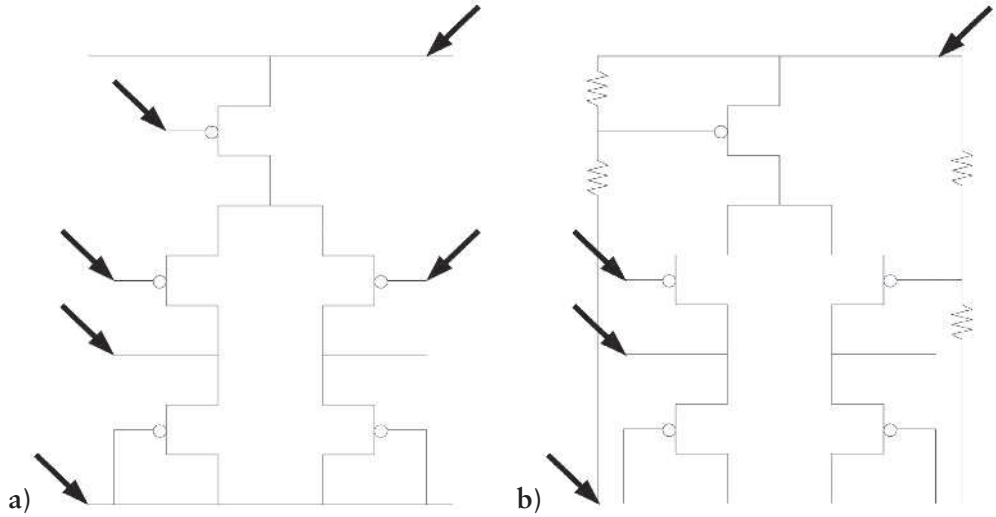


Figure 5.5 Example of testability applied to a differential amplifier: (a) six probes and (b) four probes

5.7 Multichip Wafers

The concept of multichip projects was suggested by Mead and Conway [2] as a means to expedite the development of the silicon industry. In a multichip project, many different small test designs are placed together on a single-mask set. Each design must fit within a fixed area and not require any special processing. In return, the silicon foundry guarantees a delivery time with defined process limits. The advantages to both parties are clear – the designer gets a vehicle to develop new designs at minimal cost, and the foundry expands its potential customer base by being able to offer new circuit designs, or library cells, on its process. Multichip projects typically have the following characteristics:

- Standard size or template;
- Standard processing;
- Guaranteed process parameters (spread);
- Defined EDA interfaces; and
- Minimal back-end data processing.

5.8 Summary

This chapter has introduced key concepts necessary for robust design. A design flow and modelling ecosystem, based on freely available open-source tools, have been described. Other ideas relating to design tolerances, layout techniques, and testability have also been introduced to improve the quality of the manufactured foils. And finally, a rapid prototyping service has been championed as a way to accelerate organic transistor design.

References

1. M. Casale-Rossi, *Proceedings of the IEEE*, 2014, **102**, 114.

2. C. Mead and L. Conway in *Introduction to VLSI Sytems*, Addison-Wesley, Boston, MA, USA, 1980.

3. P.E. Allen and D.R. Holberg in *CMOS Analog Circuit Design*, Holt, Rinehart & Winston, Inc., New York, NY, USA, 1987.

4. *Ngspice Circuit Simulator*, Ngspice. *http://ngspice.sourceforge.net/*

5. Xspice. *http://users.ece.gatech.edu/~mrichard/Xspice/*

6. *Electric VLSI Design System*, Electric VLSI. *http://www.staticfreesoft.com/*

7. T. Williams and C. Kelley in *gnuplot*, 2004. *http://www.gnuplot.info/docs_4.4/gnuplot.pdf*

8. V. Litovski and M. Zwolinski in *VLSI Circuit Simulation and Optimization*, Chapman & Hall, London, UK, 1997.

9. K. Myny, P. van Lieshout, J. Genoe, W. Dehaene and P. Heremans, *Organic Electronics*, 2014, **15**, 937.

10. S. Abdinia, F. Torricelli, G. Maiellaro, R. Coppard, A. Daami, S. Jacob, L. Mariucci, G. Palmisano, E. Ragonese, F. Tramontana, A.H.M. van Roermund and E. Cantatore, *Organic Electronics*, 2014, **15**, 904.

11. M.J.M. Pelgrom, A.C.J. Duinmaijer and A.P.G. Welbers, *Journal of Materials Research*, 1989, **24**, 1433.

12. K.R. Lakshmikumar, R.A. Hadaway and M.A. Copeland, *Journal of Materials Research*, 1986, **21**, 1057.

13. N. Weste and K. Eshraghian in *Principles of CMOS VLSI Design – A Systems Perspective*, Addison-Wesley, Boston, MA, USA, 1985.

6 Digital

6.1 Introduction

Most of the information that flows around the world is binary data, processed by ever faster and increasingly more sophisticated digital circuits. Against this backdrop of silicon domination, organic technologies have been seeking a niche where they can make a substantial difference. Much of the work in the published literature has thus been focused on radio frequency identification (RFID) passive tag systems. In these high-frequency applications, the power for an RFID tag is harvested from a 13.56 MHz radio signal from an RFID reader. The harvested energy drives the local tag circuits, which communicate back to the reader by modulating the incoming radio signal. The expectation is that RFID tags will eventually replace barcodes, and thus there is a basic requirement to be cheap, which is one of the many advantages of organic technologies.

One of the first major works on organic RFID tags was by Cantatore and co-workers in 2007 [1]. They reported a 1938-transistor 64 bit RFID tag operating at 150 Hz and 30 V. Even a standard-compliant 125 kHz data rate was achievable if the reader and tag were in close proximity, allowing the harvesting of 90 V internally. Myny and co-workers combined an inductively coupled antenna with the RFID tag and implemented a 64 bit RFID tag of 414 transistors and a 128 bit RFID tag of 1286 transistors [2, 3]. These operated at data rates of 787 Hz (14 V) and 1,529 Hz (24 V), respectively. While these were impressive achievements, they did not meet the standard specification, so in 2010, Myny and co-workers demonstrated a compliant 8 bit RFID tag running at 50 kHz and 18 V [4]. The higher speed was attained with evaporated pentacene as the semiconductor and high-k aluminium oxide as the gate dielectric. And, as a further demonstration of large-scale integration, in 2012, Myny and co-workers produced an 8 bit 40 instructions per second microprocessor on plastic foil with 3381 transistors, the most transistors yet on a single foil (excluding display applications) [5, 6].

Zschieschang and co-workers showed that transistor speed was just as important as quantity when they measured an 11-stage ring oscillator with a stage delay of only 420 ns at 3 V [7], while Kjellander and co-workers also reminded us in 2013 that solution

processing also has a role to play by demonstrating a 300-transistor 8 bit RFID tag at 86 Hz fabricated by an inkjet-printed active layer blend of 6,13-*bis*(triisopropylsilylethynyl)pentacene and polystyrene [8].

Previous chapters have covered transistors, modelling, and simulation. In this chapter, organic transistors will be formed into logic gates and complex digital subsystems that are comparable to modern silicon chips. Logic gates such as inverters and two-input NAND-gates are shown first, then larger gates such as memory elements, and finally small subsystems such as oscillators until the first example of an organic programmable logic device is demonstrated.

6.2 Logic Types

In order to process digital data, logic circuits must be able to read their input signals and then drive their outputs high or low as required. The outputs may be actively driven both high and low, as in complementary or pseudocomplementary gates, or they may be actively driven to only one of the output states and passively pulled to the other. In most unipolar devices, digital logic is generally designed with passive transistor loads, either diode-connected loads or zero-V_{GS} loads. Other types of passive load, such as resistor loads, require either an additional component, which may not be easily available and may not scale well with shrinking feature sizes, or a biased passive transistor load, which will require a bias voltage, possibly outside the supply rails. The two types of passive transistor load are shown for p-type devices in **Figure 6.1**. Both have a driving transistor and a second transistor acting as the load device [9, 10]. For comparison, complementary and pseudocomplementary inverters [11] are also shown.

6.2.1 Diode-connected Load

In diode-connected load logic (**Figure 6.1a**), the gate of the load device is connected to its drain. This results in an I–V characteristic that resembles a diode, hence the term diode-connected load. As the load device is always on, the driving transistor is unable to pull up to the V_{DD} rail. Instead there is a voltage divider when both transistors are in the fully on state. Careful selection of the channel width and length of both devices is necessary to achieve a satisfactory output level. When the driving transistor is off, the load device is on, as always, but cannot pull below its own V_T, otherwise it would switch itself off, and this sets the lower output level. As the load device pulls down with a relatively large on current, operation of the diode-connected load logic is relatively fast. However, as can be seen from the simulated transfer characteristic (**Figure 6.2**), the gain is low, leading to poor noise margins.

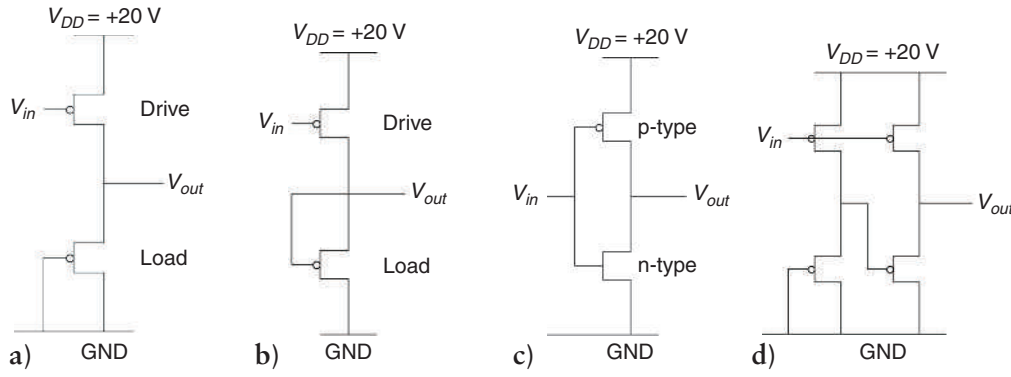


Figure 6.1 Different types of inverter: (a) p-type diode-connected load inverter; (b) p-type zero-V_{GS} load inverter; (c) complementary inverter; and (d) pseudocomplementary p-type inverter

6.2.2 Zero Gate-Source Voltage Load

When the gate of the load device is connected instead to its source (also the output node), this forms the zero gate-source voltage (zero-V_{GS}) load (**Figure 6.2b**). If only enhancement mode devices are available, then this zero-V_{GS} load transistor depends entirely on the leakage current of the load transistor to pull the output node down to ground (depletion mode devices, if available in the technology, would be more suited for the load, but this would require further processing steps). This may also be a disadvantage, as leakage current is not an easily controlled transistor attribute. Given that only leakage current is being utilised, it is possible for the load to pull the output very close to ground, but the driving transistor, which is also off and similarly leaking, must be smaller than the zero-V_{GS} load. Conversely, the pull-up driving device can drive the output much closer to V_{DD}. The small pull-down currents tend to result in slower logic compared with diode-connected load circuits, although gain is much higher, leading to improved noise margins compared with the diode-connected load (**Figure 6.2**).

6.2.3 Complementary Logic

Complementary technologies, on the other hand, offer both p- and n-type devices for the pull-up and pull-down respectively. At the expense of more involved fabrication with more processing steps, for the complementary inverter (**Figure 6.1c**) full rail-to-rail operation is achievable, in addition to symmetrical switching, faster operation, higher gain and noise margin, and almost zero static power consumption [12, 13]. However, the input of a complementary inverter is now connected to two transistors and so will present more gate input capacitance for the previous logic gate to drive.

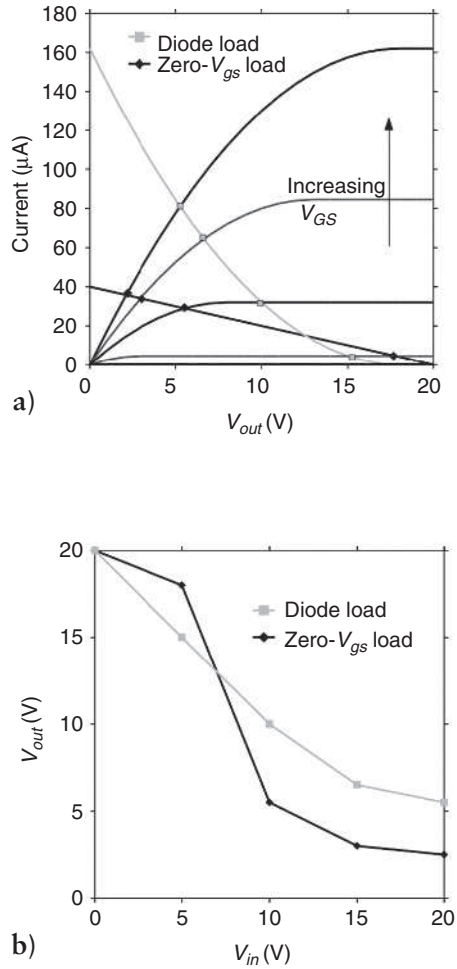


Figure 6.2 Simulated inverter DC transfer characteristics comparing a diode-connected load and a zero-V_{GS} load: (a) load lines and (b) DC transfer response

6.2.4 Pseudocomplementary Logic

An alternative to full complementary logic in unipolar technologies would be to implement a pseudocomplementary inverter [11] (**Figure 6.1d**), which offers some comparable advantages to complementary logic, albeit with larger area and slower operation. The pseudocomplementary inverter is a two-stage logic gate where the first stage is a normal unipolar inverter providing an inverted control signal and the second output driver stage has actively driven pull-up and pull-down unipolar drivers. As with the complementary inverter, the input of the pseudocomplementary inverter

is connected to two transistor gates. When the driver is in pull-up operation, the output can reach V_{DD} as the pull-down transistor is off, or nearly off. In pull-down operation, now the pull-up transistor is off and the pull-down transistor can pull down to its own V_T.

6.3 Logic Gates

Next, the basic logic blocks for building larger, more complex systems are considered. These basic blocks are the inverter, a two-input NAND-gate, and a D-type flip-flop(s) (DFF). There are two main characterisation types to be considered: DC and transient switching. DC characteristics are concerned with static behaviour of the devices, so any time-variant components are allowed to settle down before a measurement is made. This is usually not a problem, as time constants are normally short. Transient switching characteristics capture the behaviour of the circuit with respect to time. This is primarily the charging and discharging of capacitive gate and interconnect loads. Other types of analysis such as AC (frequency response) or noise are not discussed here, although they become important with higher-frequency or sensitive applications.

6.3.1 Inverter

Inverters are the most basic logic elements to be found in any design. DC transfer characteristics for diode-load inverters of various sizes are shown in **Figure 6.3**.

The operation of the p-type diode-connected load inverter can be described simply and qualitatively. As the output of the inverter is driven high, this charges output loading capacitances. The inverter's driving transistor is initially in saturation before moving into its linear region [14]. Meanwhile, the (smaller) diode-connected load transistor is always on and always in saturation (as its V_{DS} is always greater than its $V_{GS} - V_T$), acting against the pull-up driving transistor and reducing the total charging-up current. As both driving and diode-connected load transistors are on, the logic-1 level is set approximately by the ratios of the W/L of the two transistors. When the inverter output switches low, the driving transistor is now off and only the saturated diode-connected load transistor pulls the output low until the diode-connected load transistor reaches its V_T, at which point it can go no lower.

The effect of changing the driver:load transistor channel width ratio for the same channel length is shown in **Figure 6.3a**. An inverter with a driver:load transistor ratio of 8:1 can be seen to be the best compromise between the logic levels, DC transfer gain, switching threshold, and size. For this particular inverter, further measurements were made to gauge the effect of different supply voltages (**Figure 6.3b**).

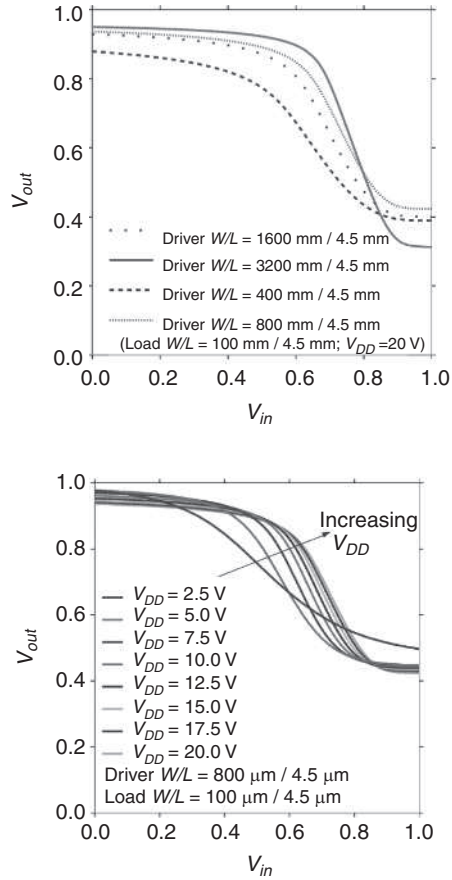


Figure 6.3 Normalised DC transfer responses for diode-connected load inverters: (a) inverters of different size at V_{DD} = 20 V, load = 100/4.5 µm and (b) different V_{DD} for the same inverter, driver = 800/4.5 µm, load = 100/4.5 µm

6.3.1.1 DC Transfer Characteristics

Simulated and measured DC transfer characteristics for inverters are shown in **Figure 6.4a**. The simulations show some deviation from the measured data, which can be due to three factors: (i) the model is not a good representation of the actual device; (ii) the parameter extraction was not accurate; or (iii) the device providing the measured data for the parameter extraction differs significantly from the devices in the inverter. The errors caused by the first two factors will decrease as more data are accrued. Points concerning the final factor will be explored further during the Monte Carlo simulations and analysis.

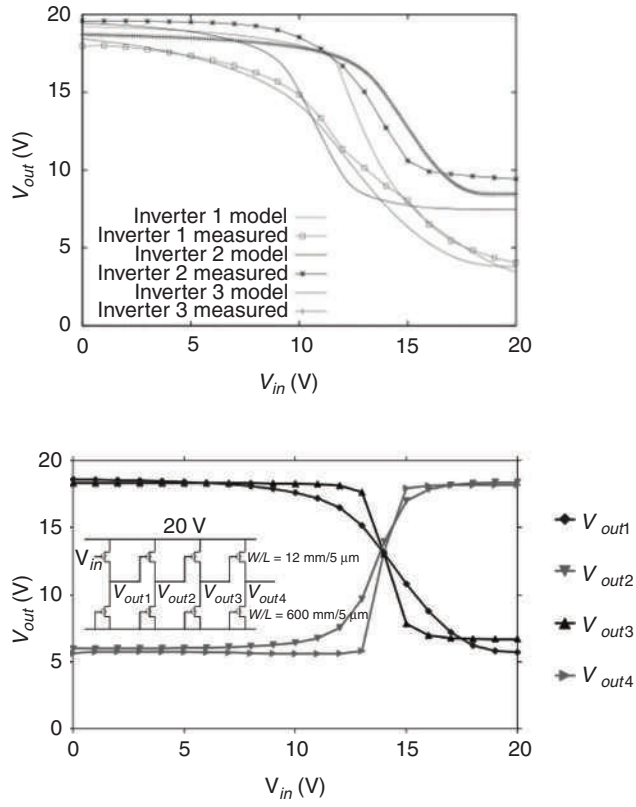


Figure 6.4 Inverter DC transfer characteristics: (a) measured and simulated inverters and (b) measured chain of four inverters on FIPS1

6.3.1.2 Noise Margin

The robustness of an inverter (or any digital logic) can be measured by its noise margin, on the assumption that the same circuit is at the inputs and outputs [15]. This is the amount of noise seen by its inputs that the circuit can tolerate before its operation starts to become degraded or even incorrect. The output levels of an inverter can be denoted by a minimum-output high-value V_{OH} due to a maximum-input low-level V_{IL}, and by a maximum-output low-value V_{OL} due to a minimum-input high-value V_{IH}. From these definitions, the noise margins for the high-state NM_H and low-state NM_L can be defined:

$$NM_H = V_{OH} - V_{IH} \tag{6.1}$$

$$NM_L = V_{IL} - V_{OL} \tag{6.2}$$

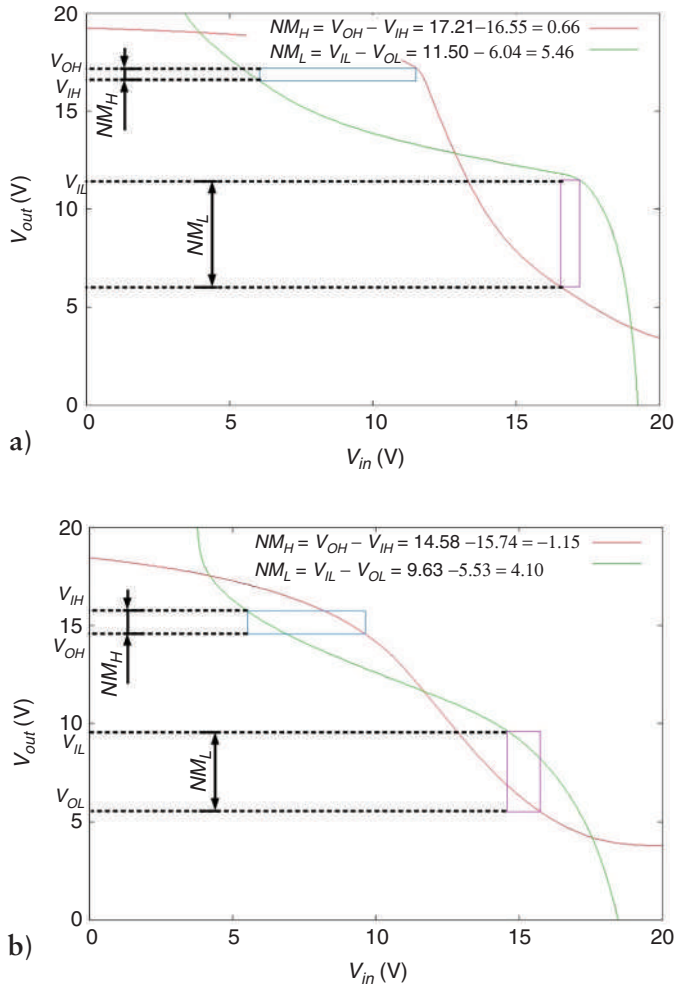


Figure 6.5 Noise margin (butterfly) plots of measured inverters with (a) acceptable noise margin and (b) failing noise margin

A large positive value for the NM_L or NM_H corresponds to a large noise margin and a high tolerance to noise on the inputs. The noise margin plots and values for two inverters are shown in **Figure 6.5**. On each plot, the DC transfer characteristic is plotted twice, firstly as normal, and secondly as though the axes were swapped to produce a trace reflected about $y = x$. The resulting plot is sometimes called a butterfly plot, and rectangles may be drawn within the enclosed areas of the two curves where the corners of the rectangles are at the points on the curves where the gradient is +1 or -1.

An ideal inverter would be symmetrical, switching sharply at the $V_{DD}/2$ point. This would result in maximum noise margins near to $0.5V_{DD}$. It can be seen that the first inverter (**Figure 6.5a**) has a reasonable low-state noise margin (5.46 V = $0.27V_{DD}$) but only a small high-state noise margin (0.66 V = $0.03V_{DD}$). But the second inverter (**Figure 6.5b**), while also having a similar low-state noise margin (4.10 V = $0.21V_{DD}$), unfortunately has a negative high-state noise margin (-1.15 V = $-0.06V_{DD}$). This means that in the worst-case scenario a high output from that inverter may not be high enough to drive the input of a following similar inverter, or a noisy environment may lead to a degraded performance from that inverter.

6.3.1.3 Monte Carlo Analysis

A Monte Carlo simulation is a useful tool to analyse circuit performance and predict yield with statistically variable parameters. In the Monte Carlo analysis shown in **Figure 6.6**, the V_T and μ_0 have a Gaussian distribution. Mean and standard deviation (SD) values of V_T and μ_0 have been calculated for different transistor sizes [16], based on measured data from nine samples (**Chapter 5**, **Figure 5.3**) and this is presented in **Table 6.1**. The predicted yield analysis is discussed in the later section on ring oscillators.

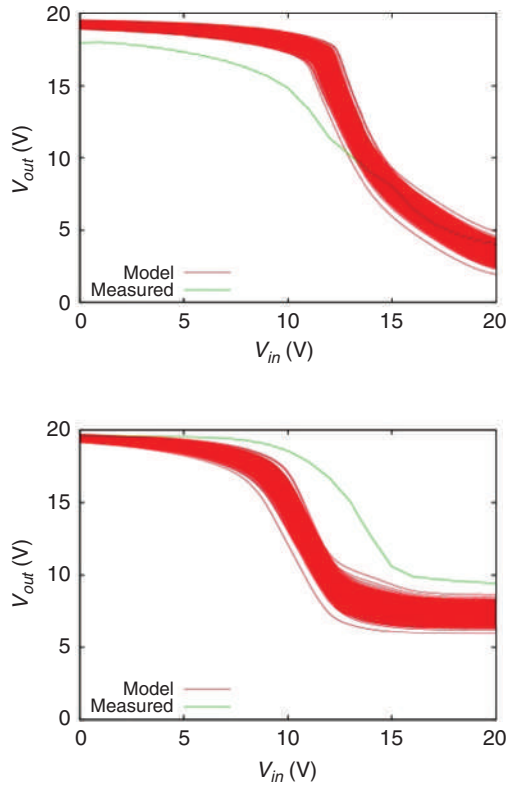


Figure 6.6 Monte Carlo analysis (1,000 simulations) of two inverters

Table 6.1 Monte Carlo SD parameters for mobility and V_T from six different transistors and processes							
	1	**2**	**3**	**4**	**5**	**6**	**Units**
W	12,000	600	3,200	1,600	800	100	μm
L	5	5	4.5	4.5	4.5	4.5	μm
$\sqrt{WL}$	244.95	54.77	120.00	84.85	60.00	21.21	μm
$\sigma\left(\frac{\mu_0}{\overline{\mu_0}}\right)$	0.0292	0.1306	0.0596	0.0843	0.1192	0.3372	—
$\frac{\sigma(V_T)}{\overline{V_T}}$	0.0140	0.0628	0.0287	0.0405	0.0573	0.1621	—

6.3.1.4 Transient Switching Characteristics

A first-order approximation of the switching speed of the inverter can be obtained by assuming the pull-up and pull-down currents to be constant during the transient switching, allowing this simple equivalence to be used:

$$Q = it = CV \tag{6.3}$$

where Q is charge, i is the average pull-up (i_{rise}) or pull-down (i_{fall}) current, t is the time taken for the rising (t_{rise}) or falling transition (t_{fall}), C is the load capacitance being driven by the inverter, and V is the voltage. The load capacitance is the gate capacitance C_g of the driven transistor, which has two components [7]: an intrinsic component, which is the capacitance of the channel area (given by the product of the channel width, W, and the channel length, L), and a parasitic component, which is the capacitance of the overlap of the source or drain and gate electrodes (approximately the product of the channel width, W, and the source or drain to gate overlap, L_g):

$$C_g = \frac{\varepsilon_0 \varepsilon_r}{d_{diel}} W\left(L + L_g\right) \tag{6.4}$$

$$t_{fall} = \frac{C_g V}{i_{fall}} \tag{6.5}$$

$$t_{rise} = \frac{C_g V}{i_{rise}} \tag{6.6}$$

where $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, $\varepsilon_r = 3.6$, and d_{diel} are the dielectric's estimated relative permittivity and thickness respectively. The inverters' estimated switching performance can now be calculated for the measured samples (**Table 6.2**) and will be checked as part of the ring oscillator.

Table 6.2 Estimated inverter switching performance

Quantity	**1**	**2**	**3**
Driver *W/L*	12 mm/5 µm	12 mm/5 µm	800/4.5 µm
Diode-connected load *W/L*	600/5 µm	600/5 µm	100/4.5 µm
Driver:diode-connected load ratio	20:1	20:1	8:1
Measured current at 20 V	29.07 µA	7.21 µA	51.25 µA (est.)
Load *W*	12 mm	12 mm	800 µm
Load *L*	5.0 µm	5.0 µm	4.5 µm
Load L_g	5.0 µm	5.0 µm	5.0 µm
Load d_{diel}	85 0 nm	250 nm	250 nm
Output load	4.50 pF	15.29 pF	0.97 pF
Rise time	6.52 µs	89.31 µs	0.86 µs
Fall time	123.29 µs	1.697 ms	6.05 µs
Stage delay	130.3 µs	1.786 ms	6.91 µs

6.3.2 Two-Input NAND

Two-Input NAND-gates based on diode-connected loads, **Figure 6.7**, were implemented in a test structure. The schematic and logic truth table are shown in **Figure 6.7a**. Normally, the testing of a two-input NAND-gate would require five

probes: two inputs, one output, power, and ground. To limit the number of probes to only four, a test circuit comprising three NAND-gates was designed as shown. The normal logical operation of a NAND-gate is for the output to be at logic-0 only if both inputs are logic-1, else the output is logic-1. The first NAND-gate has a fixed input at logic-1 and the other input is connected to the input from the tester. Its output, Nand1, is an inversion of the input signal. The inputs of the second NAND-gate are connected to logic-0, and its output, Nand2, is always logic-1. The inputs of the final NAND-gate are connected to the outputs of the first two NAND-gates. The input from Nand2 is always logic-1, while the other input from Nand1 switches from logic-0 to logic-1. In this way, with three NAND-gates, the NAND-gate design can be tested with all combinations of logic-0 and logic-1 on its inputs from only four probes, with the final output Nand3 easily observable. In addition, the ability of a NAND-gate to drive another logic gate has also been tested.

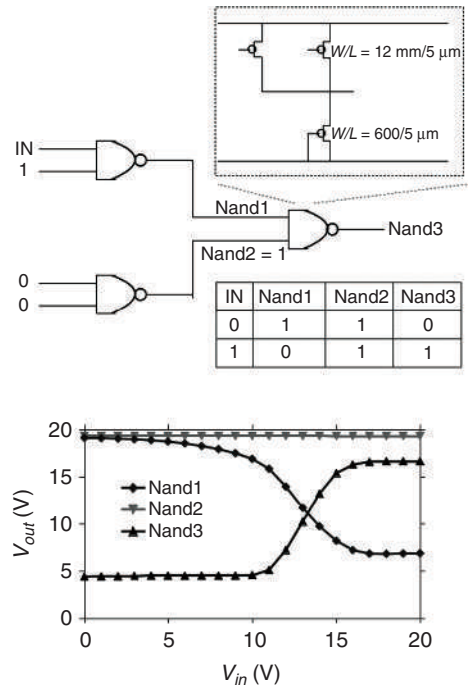


Figure 6.7 Two-input NAND-gates: (a) NAND test schematic and (b) NAND measured results

The result of the NAND test circuit at V_{DD} = 20 V is shown in **Figure 6.7b** and **Table 6.3**. Nand2 is always logic-1 and, being driven by 0 V from a semiconductor parameter analyser (SPA), it maintains a good level of 19.3 V. Nand1 has both inputs

driven at either 0 or 20 V from the SPA. Its logic-0 and logic-1 are 6.7 and 19.1 V respectively. Nand3, meanwhile, is driven entirely by the outputs from other gates; its outputs are 4.4 and 16.6 V.

These measurements show that the two-input NAND-gate worked well at V_{DD} = 20 V. The logic-1 value of Nand3 was, as expected, lower than the logic-1 values of Nand1 and Nand2, as the inputs of Nand3 were driven by the other NAND-gates which could not provide a logic-0 level of 0 V. The logic-0 value of Nand3 was, however, lower than expectations when compared with Nand1 (4.4 *versus* 6.8 V).

Table 6.3 Two-input NAND measured test result

	Minimum	**Maximum**
Nand1	6.8 V	19.1 V
Nand2	19.3 V	19.3 V
Nand3	4.4 V	16.6 V

6.3.3 D-type Flip-flop Memory

Storage of data is an essential part of any digital system. For permanent non-volatile storage of data, floating gate processes may be considered [17]. In these processes, an extra gate is inserted in the gate dielectric between the gate electrode and the source–drain channel. This extra gate is unconnected to anything, hence the term 'floating gate'. Under the right conditions, for example, a high gate-voltage and a high source–drain electric field, charge carriers may gain enough energy to cross or tunnel from the transistor channel through the gate dielectric and become trapped in the floating gate. The trapped charge on the floating gate now acts as a stored data bit, screening the channel from the gate electrode until a reverse procedure removes the trapped charge from the floating gate.

For volatile storage applications, DFF are the usual circuit elements. They allow the temporary storage, at clock speeds, of data while data are being processed at those same clock speeds. There are two styles of flip-flop design. The prevalent design for silicon complementary metal-oxide semiconductor circuits is based on back-to-back inverters and transmission gates [14]. However, for a unipolar process without complementary transistors, a NAND-gate-based design is commonly used instead.

Normalised results and design schematics for the memory circuit are shown in **Figure 6.8**. The design is a NAND-based DFF, but, for testability purposes, the inverting output is connected back to the input to make a T-type or toggle flip-flop,

which also shows that the flip-flop can be used without incurring a race condition. The expected function of a T-type flip-flop is that the output should toggle between high and low with each rising edge of the input clock. The SPA was connected to the T-type flip-flop circuit, providing power and clock and enabling monitoring of the non-inverting output. The clock period was approximately 6 s, and successful operation was measured at supply voltages of 10, 15 and 20 V. At these supply voltages, the output high value is consistently at 95% of the supply voltage: 9.5, 14.25 and 19 V, respectively. This corresponds well to the diode-connected load nature of the logic design, where the output high value is set by the ratios of the drive and load transistors.

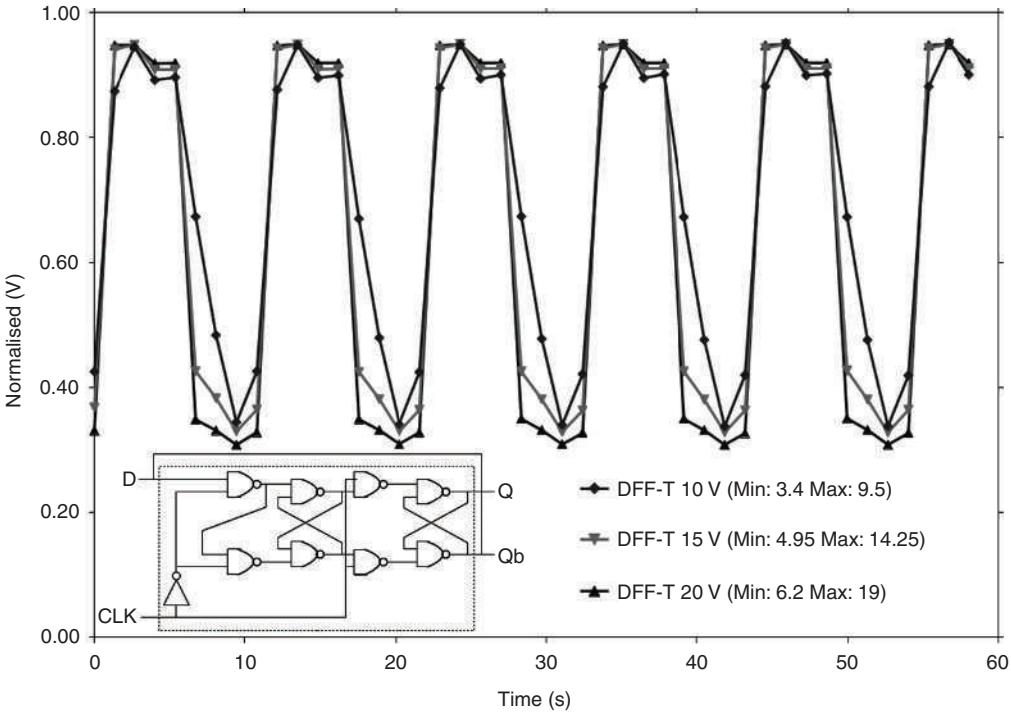


Figure 6.8 Schematic and normalised measurements of a clocked memory element constructed from two-input NAND-gates. The inverse output of the DFF has been connected back to the input to make a toggle T-type flip-flop. Note that the coarse sampling times are due to the SPA being used for the transient measurement. Reproduced with permission from A. Sou, S. Jung, E. Gili, V. Pecunia, J. Joimel, G. Fichet, and H. Sirringhaus, *Organic Electronics*, 2014, **15**, 11, 3111. ©2014, Elsevier [18]

6.4 Digital Subsystems

Having introduced the base logic gates (inverter, two-input NAND, DFF), this section will now assemble them into larger functional blocks.

6.4.1 Ring Oscillator

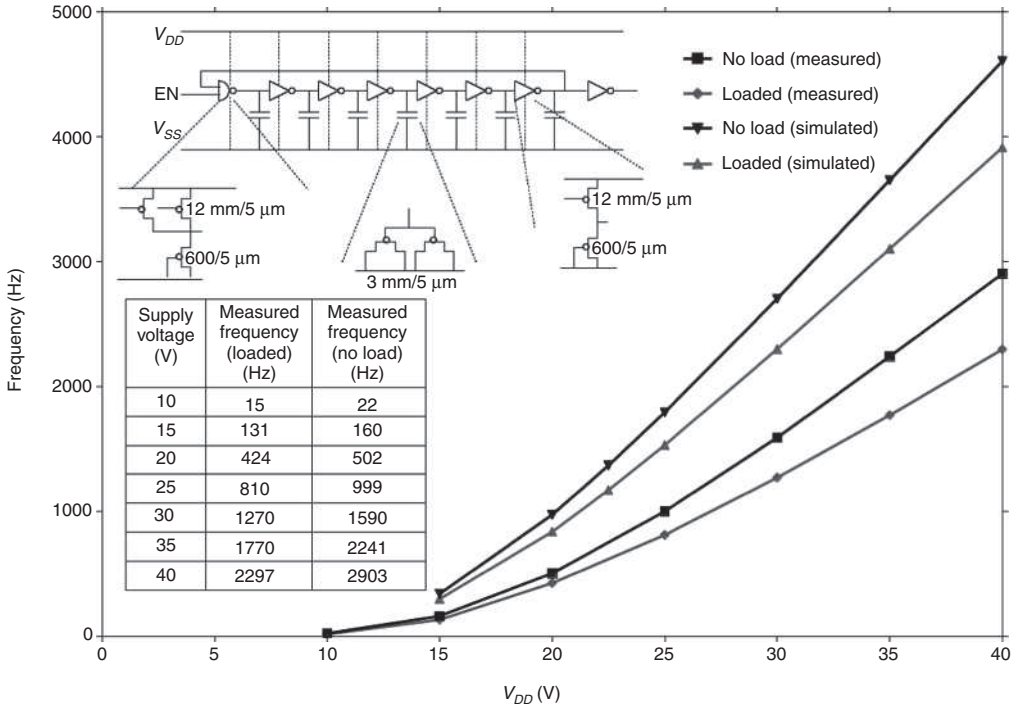
Every synchronous digital system requires a regular clock to regulate the flow of data around the system. These clocks are typically provided by oscillators, which are inherently unstable circuits that alternate state. High-quality on-chip oscillators are usually provided by LC oscillators, which consist of an inductance and a capacitance in parallel. The accuracy of oscillators is measured as deviations from periodicity in the time domain (jitter) or frequency domain (phase noise). LC oscillators usually have less jitter but tend to be large and inflexible as the oscillation frequency is related to the LC product.

Ring oscillators, on the other hand, are small, but jitter is high. Flexibility is afforded by altering the supply voltage to the oscillator, making it a voltage-controlled oscillator (VCO) [19]. Additional circuitry to complete an analogue-phase locked loop will allow the VCO to synchronise with an external clock source or incoming data signal, and this forms the basis of most of today's communications technology.

As ring oscillators are such a seminal part of digital subsystems, they are often fabricated in test devices as part of the process characterisation. Four ring oscillators have been designed and fabricated. The measured results are now presented, followed by an analysis.

6.4.1.1 7-Stage Ring Oscillator

The results of a 7-stage ring oscillator are shown in **Figure 6.9**. The ring oscillator employed a two-input NAND-gate as the first inversion stage, and provided identical capacitive loads for each stage of the ring oscillator. The two-input NAND-gate allowed the use of an enable signal to start or stop the oscillation (**Figure 6.9b**). The capacitive loads, which were simply the gates of unused transistors, allowed a crude frequency control, demonstrating the feasibility of this method to control the speed of oscillation. At 40 V, without the capacitive loads, a maximum oscillation frequency of 2,903 Hz was recorded, corresponding to a single-stage frequency of 40.6 kHz and a VCO gain of 131 Hz/V. With the capacitive loads, the maximum oscillation frequency was reduced by 20% to 2297 Hz, corresponding to a single-stage frequency of 32.2 kHz and a VCO gain of 103 Hz/V.



Supply voltage (V)	Measured frequency (loaded) (Hz)	Measured frequency (no load) (Hz)
10	15	22
15	131	160
20	424	502
25	810	999
30	1270	1590
35	1770	2241
40	2297	2903

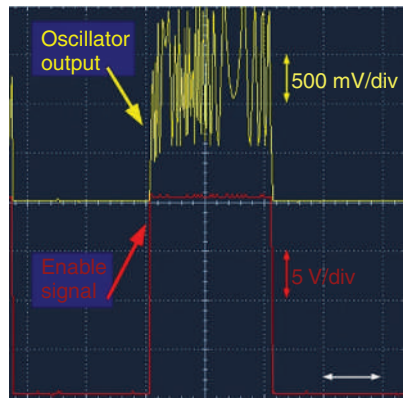


Figure 6.9 7-Stage ring oscillator results: (a) schematic and measurements with frequency adjust on/off and (b) enable operation. Note that oscillator start-up is unpredictable and it took several seconds before stable oscillator operation. Reproduced with permission from A. Sou, S. Jung, E. Gili, V. Pecunia, J. Joimel, G. Fichet and H. Sirringhaus, *Organic Electronics*, 2014, **15**, 11, 3111. ©2014, Elsevier [18]

An alternative way to view the frequency variation would be 2,600 ± 303 Hz (11.6%). Very often it is important in circuit designs to be able to control the speed of a ring oscillator, for example, to meet external standards for data communication. However, wide process and fabrication tolerances and varying operating conditions will cause the performance of sensitive circuits such as the ring oscillator to fluctuate greatly. By allowing the capacitive load at each ring oscillator stage to be variable and controllable, it will be possible to regulate the ring oscillator to meet external specifications.

6.4.1.2 9-Stage Ring Oscillator

The 9-stage ring oscillator was designed using the same size inverters as for the 7-stage ring oscillator. A ring oscillator with an improved organic semiconductor and a reduced dielectric thickness is expected to be faster, and hence a 9-stage ring oscillator was implemented instead of a 7-stage ring oscillator. However, the semiconductor did not perform as well as anticipated, and ring oscillator performance was consequently slower (**Figure 6.10a**).

6.4.1.3 17-Stage Ring Oscillator (1)

This 17-stage ring oscillator had inverters with driver W/L = 800/4.5 μm and diode-connected load W/L = 100/4.5 μm (**Figure 6.10b**).

6.4.1.4 17-Stage Ring Oscillator (2)

A second 17-stage ring oscillator was of the same design but a different process (**Figure 6.10c**).

6.4.1.5 Oscillator Summary

The performance of the oscillators is summarised in **Table 6.4**. While there is a discrepancy between the measured, the calculated, and the simulated values, the difference is within reasonable limits. The worst calculated value discrepancy was for the 17-stage (2) ring oscillator, where the calculated value was 2.5 times slower than measured. The worst simulated value was for 17-stage (1) ring oscillator, for which the simulation was 2.5 times slower. The simulated value for the 7-stage ring oscillator was also significantly different to the measured values, being 1.9 times faster. However, these results for the calculated and simulated values should be considered reasonable and 'in the right ballpark'. With further refinement of the model and better parasitic estimates, improvements in accuracy should be achievable.

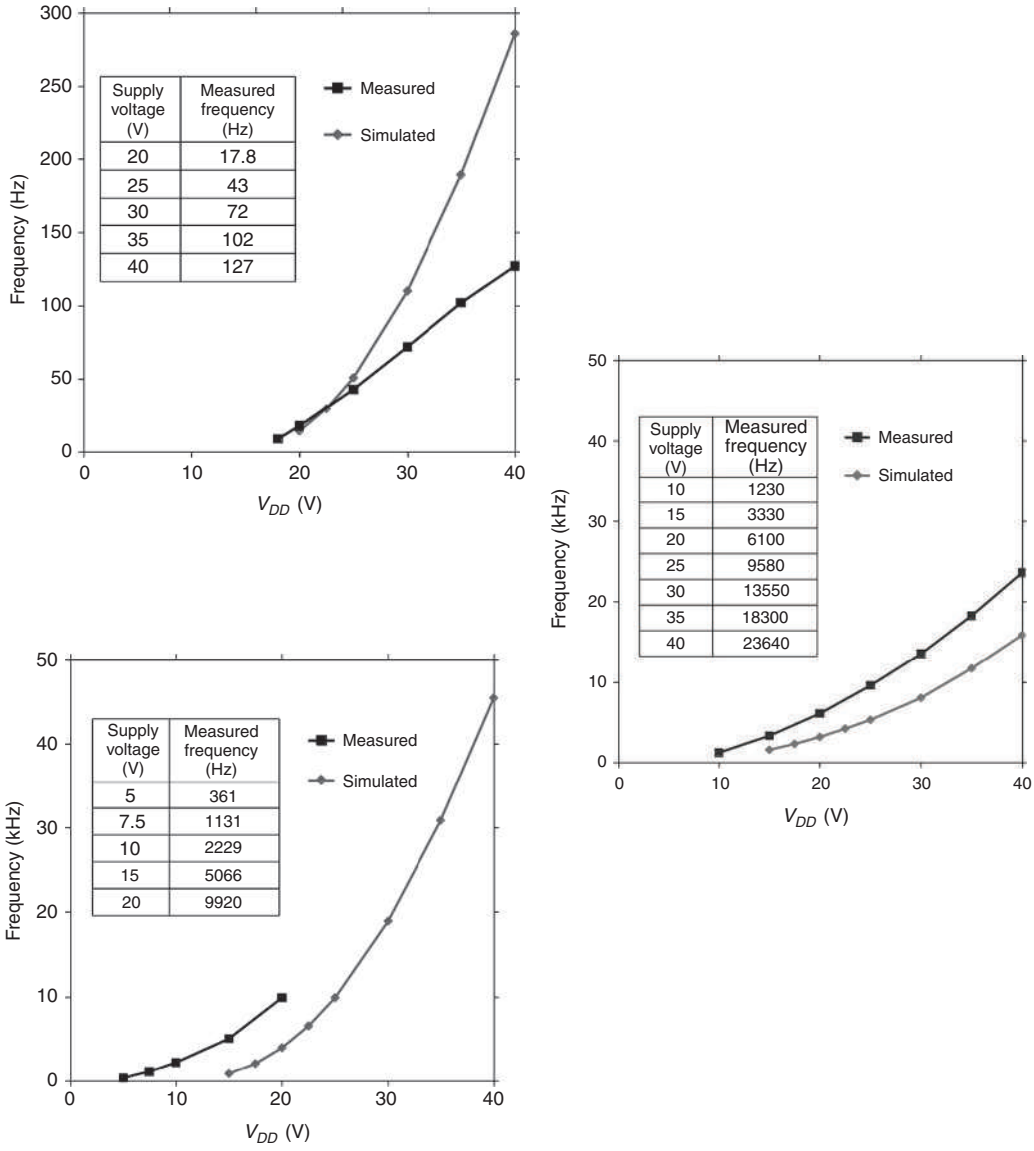


Figure 6.10 (a) 9-Stage ring oscillator, measured and simulated results; (b) 17-stage ring oscillator, measured and simulated results; and (c) 17-stage ring oscillator, measured and simulated results

Table 6.4 Measured ring oscillator speed compared with published work, and against calculated (expected) and simulated speeds							
Parameter	**Zschieschang [7]**	**Kjellander [8]**	**7-Stage**	**9-Stage**	**17-stage (1)**	**17-stage (2)**	**Units**
Number of stages	11	19	7	9	17	17	—
Total area	—	—	128	80	2.75	2.75	mm^2
Area/stage	—	—	18.3	8.9	0.16	0.16	mm^2
Inverter driver *W/L*	—	—	12,000/5	12,000/5	800/4.5	800/4.5	µm/µm
Inverter load *W/L*	—	—	600/5	600/5	100/4.5	100/4.5	µm/µm
Mobility μ_0	—	—	0.0171	0.0019	0.102	0.0605	cm^2/Vs
V_{DD}	3	10	20	20	20	20	V
Measurements							
Frequency	108	0.503	0.502	0.018	9.920	6.100	kHz
Stage delay	0.420	52.3	142.3	3121.1	2.96	4.82	µs
Stage frequency	2381	19.1	7.0	0.320	337	207	kHz
VCO gain	46.0	—	0.109	0.054	0.769	0.696	kHz/V
Calculations							
Stage delay	—	—	130	1786	6.91	12.16	µs
Stage frequency	—	—	7.67	0.56	144.7	82.3	kHz
Simulations							
Frequency	—	—	0.971	0.014	3.987	3.187	kHz
Stage delay	—	—	73.5	3879.6	7.38	9.23	µs
Stage frequency	—	—	13.6	0.258	135.56	108.36	kHz
VCO gain	—	—	0.173	0.0096	1.500	0.424	kHz/V

There is also a significant increase in speed between the 7- and 9-stage ring oscillators and the later 17-stage ring oscillators. For example, the measured stage frequencies of the 17-stage (1) ring oscillator and the 9-stage ring oscillator are 337 and 0.320 kHz respectively, a three orders of magnitude difference. The reasons for the speed difference are both technological and design related:

- There is a difference in semiconductor mobilities by a factor of 53.
- The 17-stage (1) ring oscillator is 55 times smaller per stage than the 9-stage ring oscillator. This consequently leads to much smaller parasitic gate overlap and interconnect capacitances and/or resistances.
- The ratio of driving transistor to load transistor is smaller for the 17-stage (1) ring oscillator. This also leads to a smaller load on each stage of the ring oscillator.

The combination of materials and design choices results in the much improved performance for both the 17-stage ring oscillators.

6.4.1.6 Monte Carlo Simulations (Yield Analysis)

One of the advantages of a physical-based simulation model are physical parameters that may be varied statistically to give yield analysis projections. A yield analysis was performed on the 7-stage ring oscillator. A total of 100 Monte Carlo simulations were run with the V_T and μ_0 parameters from **Table 6.1**. Of the 100 simulations, six failed for unknown reasons, but 94 simulations were successfully completed. The results are presented in **Figure 6.11**. It has already been noted that the simulated results for the 7-stage ring oscillator were faster than the measurements, so these results have to be analysed with that in mind. The VCO gain of the 7-stage ring oscillator was simulated as 173 Hz/V (**Table 6.4**). As an example of a failure criterion, if a VCO could only manage ±0.5 V deviation from the mean as a control signal, this sets the pass criterion as a frequency between 862 and 1,035 Hz. This results in a number of passes of 55/94 and a yield of 58.5%.

6.4.1.7 Worst-case Simulations

Using the worst-case methodology previously described for two corners only, namely V_T and μ_0, four simulations were executed with V_T and μ_0 corners. The results (**Table 6.5**) can be directly compared with the Monte Carlo simulations (**Figure 6.11**). It can be seen that at the fast-fast and slow-slow corners, the oscillator is running well outside the range of the Monte Carlo simulated speeds. This is to be expected, as the worst-case corners are combining two statistically unlikely scenarios to create an even more unlikely scenario. It also highlights the challenges involved when designing

with a worst-case methodology. The slowest and fastest worst-case simulated ring oscillator speeds were 377 and 1,960 Hz, respectively. By contrast, the slowest and fastest ring oscillator speeds from 100 Monte Carlo simulations were 729 and 1,184 Hz respectively. The mean Monte Carlo speed was 949 Hz, with an SD of 100 Hz, and thus the simulated slowest and fastest speeds were at the -2.2 and +2.3σ points respectively. The worst-case simulated values of 377 and 1,960 Hz correspond to points at the -5.7 and +10.1σ positions, a statistically extremely unlikely occurrence.

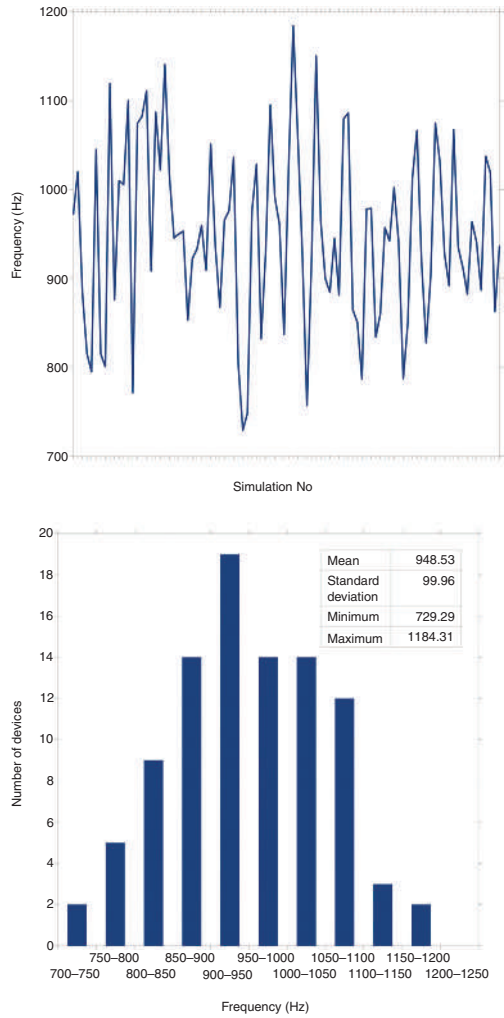


Figure 6.11 7-Stage ring oscillator Monte Carlo simulations for yield analysis: (a) the frequency of the oscillator for each simulation run – the first run (No. 1) uses the mean values of μ_0 and V_T, and subsequent runs have random values but follow a Gaussian distribution and (b) summary of simulation runs

Table 6.5 7-Stage ring oscillator worst-case simulations			
Corner name	**V_T (V)**	**μ_0 (cm²/Vs)**	**Frequency (Hz)**
Fast-fast	-4.90	2.37	1960
Fast-slow	-4.90	1.04	864
Slow-fast	-7.17	2.37	849
Slow-slow	-7.17	1.04	377

6.4.2 Programmable Array Logic

In order to alleviate the often prohibitive time and expense of silicon chip design and fabrication, semi-custom and programmable logic designs are often used instead of full custom multiple mask sets. With semi-custom designs such as Gate Array or Sea-of-Gates implementations [14], a mask set for a generic array of transistors is used partially to fabricate the chip, requiring only a final metal layer mask (or masks) which customises the function. In this way, the costs of the common masks are shared over all applications, and only the cost of the final customising mask is additional. Alternatively, for a programmable logic device, the entire mask set is made and the chip is fabricated, but a customised function is then programmed in the final chip. There are several ways to accomplish the programming, such as Erasable Programmable Read-Only Memory, Electrically Erasable Programmable Read-Only Memory, Static Random Access Memory, or antifuse [20]. Inkjet printing has also been previously used to create a print-programmable read-only memory for use as an instruction generator in a hybrid oxide–organic complementary microprocessor system [21].

A full featured inkjet PAL comparable with commercially available silicon simple programmable logic devices was designed and implemented onto two foils. The PAL (**Figure 6.12**) with extensive routing capabilities by a programmable switch fabric featured eight inputs, eight outputs, 32 product terms, a fully programmable AND-plane, a fixed OR-plane, and a programmable macrocell at every output (a programmable logic array, as opposed to a PAL, has programmable AND-planes and programmable OR-planes). Each macrocell consists of a memory cell, 2:1 multiplexors, and inverters. Every part of the macrocell can be individually programmed to provide true or inverse, registered or non-registered output and feedback options.

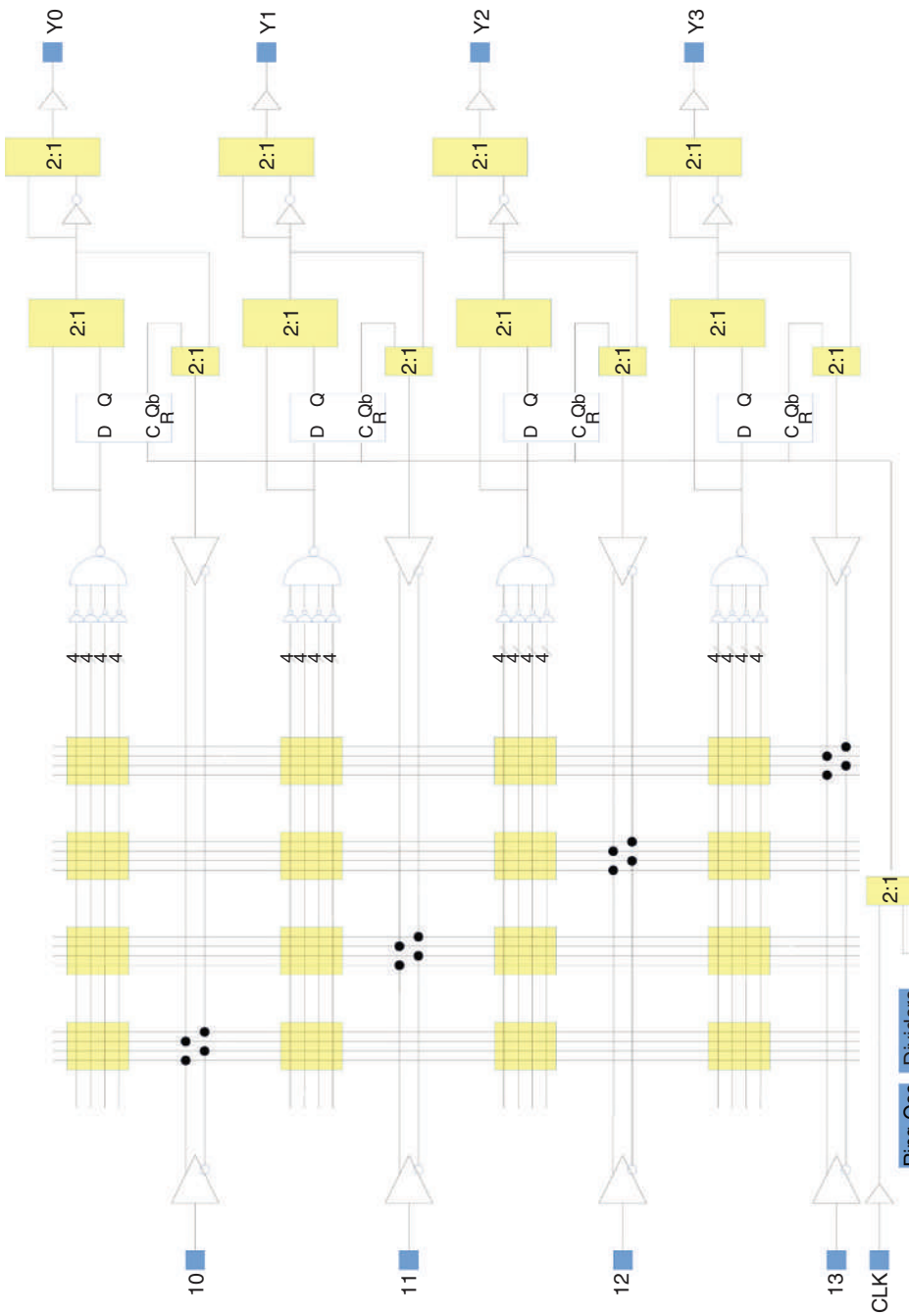


Figure 6.12 Part schematic of the programmable array logic (PAL), showing only four rows instead of eight. Reproduced with permission from A. Sou, S. Jung, E. Gili, V. Pecunia, J. Joimel, G. Fichet and H. Sirringhaus, *Organic Electronics*, 2014, **15**, 11, 3111. ©2014, Elsevier [18]

To demonstrate a design on the PAL, a 2:4 demultiplexor directly driving the E-Ink display was implemented. The demultiplexor is a combinatorial logic circuit that decodes two inputs in order to drive one of the display patterns, or none of them. The remaining inputs and outputs were unused and not connected. With reference to **Figure 6.12** and **Table 6.6**, the 2:4 demonstrator logic was implemented as follows:

- Y0 = I0.I1 (vine pattern);
- Y1 =I0.I1 (swirl pattern); and
- Y2 = I0.I1 (background pattern).

Silver wires were also inkjet printed to the edge of the foil to provide connection points for the inputs, power, and display common node (**Figure 6.13**). These connection points were attached to external wires by silver dag and secured with glue. Measurements of the E-Ink driving voltages for a 20 V supply voltage were in the range 16.7–18.9 V. For a portable demonstrator, the external supply wires were connected to four 9 V PP3 batteries providing a total 36 V. The E-Ink common external wire was attached to the 27 V point of the four batteries, and the inputs alternately touched on the 0 or 36 V terminals as necessary to provide logical input to the demultiplexor. This portable demonstrator was shown to work on the desktop with no external components other than the four batteries. For practical applications, it will be necessary to operate at much lower voltage levels. A voltage of 36 V was chosen because it provided the best display performance for the demonstration. As was seen with the memory circuit previously, operation is viable down to 10 V, but this would have led to a degraded display, both in terms of the speed of black/white switching and in black/white intensity. Retesting of the portable demonstrator after 9 months storage in normal office conditions revealed that the 2:4 demultiplexor circuit and display were still fully functional.

Table 6.6 Demultiplexor function truth table

I0	I1	Vines	Swirls	Background
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

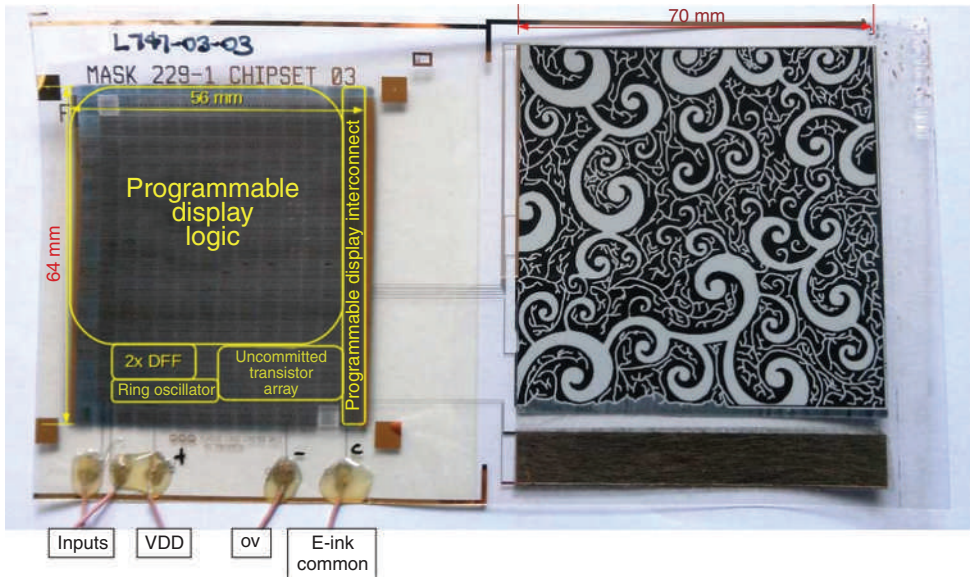


Figure 6.13 Photograph of the PAL driving an electrophoretic ink (E-Ink) display. Reproduced with permission from A. Sou, S. Jung, E. Gili, V. Pecunia, J. Joimel, G. Fichet and H. Sirringhaus, *Organic Electronics*, 2014, **15**, 11, 3111. ©2014, Elsevier [18]

6.5 Summary

In this chapter, the first examples of PAL devices with organic transistors programmed by the inkjet printing of conductive silver wires have been demonstrated. An organic transistor circuit driving a flexible display integrated on a single polyethylene naphthalate substrate, the only external components being batteries, has also been shown. It is expected that, by extending this work to larger digital designs and incorporating analogue circuit elements, flexible organic electronic subsystems will be ideally placed for markets that are currently served by conventional, though bulky, discrete printed circuit boards but are too small for custom-designed integrated silicon chips.

References

1. E. Cantatore, T.C.T. Geuns, G.H. Gelinck, E. van Veenendaal, A.F.A. Gruijthuijsen, L. Schrijnemakers, S. Drews and D.M. de Leeuw, *IEEE Journal of Solid-State Circuits*, 2007, **42**, 84.

2. K. Myny, S. Steudel, P. Vicca, M.J. Beenhakkers, N.A.J.M. van Aerle, G.H. Gelinck, J. Genoe, W. Dehaene and P. Heremans, *Solid-State Electronics*, 2009, **53**, 1220.

3. K. Myny, S. Van Winckel, S. Steudel, P. Vicca, S. De Jonge, M. Beenhakkers, C. Sele, N.A.J.M. van Aerle, G.H. Gelinck, J. Genoe and P. Heremans, *IEEE Journal of Solid-State Circuits*, 2008, **4**, 290.

4. K. Myny, S. Steudel, S. Smout, P. Vicca, F. Furthner, B. van der Putten, A.K. Tripathi, G.H. Gelinck, J. Genoe and W. Dehaene, *Organic Electronics*, 2010, **11**, 1176.

5. K. Myny, E. Van Veenendaal and G.H. Gelinck, *IEEE International Solid-State Circuits Conference*, 2011, p.322.

6. K. Myny, E. van Veenendaal, G.H. Gelinck, J. Genoe, W. Dehaene and P. Heremans, *IEEE Journal of Solid-State Circuits*, 2012, **47**, 1.

7. U. Zschieschang, R. Hofmockel, R. Rödel, U. Kraft, M.J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J. Butschke, H. Richter, J.N. Burghartz and H. Klauk, *Organic Electronics*, 2013, **March**, 3.

8. B.K.C. Kjellander, W.T.T. Smaal, K. Myny, J. Genoe, W. Dehaene, P. Heremans and G.H. Gelinck, *Organic Electronics*, 2013, **14**, 768.

9. K. Myny, M.J. Beenhakkers, N.A.J.M. van Aerle, G.H. Gelinck, J. Genoe, W. Dehaene and P. Heremans, *IEEE Journal of Solid-State Circuits*, 2011, **46**, 1223.

10. I. Nausieda, K. Ryu, D. He, A. Akinwande, V. Bulovic and C. Sodini, *IEEE Transactions on Electron Devices*, 2011, **58**, 865.

11. T-C. Huang, K. Fukuda, C-M. Lo, Y-H. Yeh, T. Sekitani, T. Someya and K-T. Cheng, *IEEE Transactions on Electron Devices*, 2011, **58**, 141.

12. M. Guerin and A. Daami, *IEEE Transactions on Electron Devices*, 2011, **58**, 3587.

13. E. Gili, M. Caironi and H. Sirringhaus, *Applied Physics Letters*, 2012, **100**, 123303.

14. N. Weste and K. Eshraghian in *Principles of CMOS VLSI Design – A Systems Perspective*, Addison-Wesley, Boston, MA, USA, 1985.

15. S. De Vusser, J. Genoe and P. Heremans, *IEEE Transactions on Electron Devices*, 2006, **53**, 601.

16. K. Myny, P. van Lieshout, J. Genoe, W. Dehaene and P. Heremans, *Organic Electronics*, 2014, **15**, 937.

17. B. Peng and P.K.L. Chan, *Organic Electronics*, 2014, **15**, 203.

18. A. Sou, S. Jung, E. Gili, V. Pecunia, J. Joimel, G. Fichet and H. Sirringhaus, *Organic Electronics*, 2014, **15**, 11, 3111.

19. R. Ganesan, J. Krumm, K. Ludwig and M. Glesner, *Solid-State Electronics*, 2014, **93**, 8.

20. S. Brown and J. Rose, *IEEE Design and Test of Computers*, 1996, **13**, 42.

21. K. Myny, S. Smout, M. Rockele, A. Bhoolokam, T-H. Ke, S. Steudel, K. Obata, M. Marinkovic, D-V. Pham, A. Hoppe, A. Gulati, F. Rodriguez, B. Cobb, G.H. Gelinck, J. Genoe, W. Dehaene and P. Heremans, *IEEE International Solid-State Circuits Conference*, 2014, p.486.

7 Analogue

7.1 Introduction

Just as we must live in the real world, electronic circuits must also interface in the analogue world. However, organic devices are inherently bad at processing analogue data. The combination of low charge carrier mobilities and high threshold-voltage reduces operating performance, while the wide variability in fabrication and device mismatch make robust design more difficult [1]. Nevertheless, organic analogue design is a field that has attracted a lot of interest. Although current literature is still focused on analogue building blocks, there has nevertheless been progress with the integrated analogue systems that are required for projects such as radio frequency identification for which the analogue building blocks were intended. Some analogue building blocks have already been demonstrated in the literature, and today's organic field-effect transistor technologies are capable of designs in the kHz frequency range [2].

One of the first papers to report an organic differential amplifier was Kane and co-workers in 2000 who fabricated a pentacene ($C_{22}H_{14}$) differential amplifier on flexible polyethylene naphthalate (PEN) with a maximum gain of 18.6 dB at 20 V [3]. Further work in 2006–2007 by Gay and co-workers produced $C_{22}H_{14}$ differential amplifiers with smaller gains of 10 dB but substantial progress in the modelling and simulation of analogue circuits [4, 5]. Marien and co-workers then fabricated a differential amplifier, also $C_{22}H_{14}$, with a gain of 18 dB at the low supply voltage of 15 V in 2010 [6]. The highest gains reported so far have been in a 2013 publication by Maiellaro and co-workers [7], where a two-stage complementary organic amplifier with gains of between 40 and 50 dB at 50 V was fabricated on a printed complementary organic thin-film transistor.

Another area of intense research activity is the development of analogue–digital converters (ADC). The best work in this field has come from Marien and co-workers in 2011 with a 26.5 dB (4.1 bit) sigma-delta ($\Sigma\Delta$) ADC [8] (where bits = [signal-to-noise ratio – 1.76]/6.02). Meanwhile, the integration of analogue components in a system was reported by Marien and co-workers in 2012 with work on organic smart sensor systems [9]. In this work, Marien and co-workers fabricated components for a proposed analogue smart sensor system operating from a 15 V supply in a $C_{22}H_{14}$ dual-gate process, namely a capacitive touch sensor, a two-stage operational amplifier (op-amp) with a DC gain of 20 dB, a voltage up-converter, and the aforementioned $\Sigma\Delta$ ADC.

In this chapter, some basic analogue circuits will be presented and analysed. The models and simulation techniques introduced in the previous chapters will be used to show how to estimate and predict performance.

7.2 Analogue Selector

7.2.1 Description

The function of a selector, be it analogue or digital, is to select and route one of a number of input signals to the output. If the select controls are encoded, then this function is referred to as a multiplexor. If the select controls are not encoded, then the function is a selector. A multiplexor has the advantage that the encoded select inputs ensure that no more than one input can be routed to the output.

The basic architecture of a 4:1 selector is shown in **Figure 7.1a**. There are four switches connected in parallel, only one of which should be on at any given moment. When selected, a switch is able to pass the input to the output. Assuming sufficient margins, a digital selector can optionally restore the input signal after it has passed through the switch to recover a poor input signal. On the other hand, the analogue selector must faithfully reproduce the input signal at the output without degradation. Analogue selectors can be used for passing either voltage or current. There are fewer losses associated with passing currents than voltages, and where possible it is preferable to distribute currents instead of voltages, but this is dependent upon the circuit or application. The selector here has been tested for voltage operation.

The essential element of an analogue selector is the analogue switch, which may be a transmission gate (**Figure 7.1b**) or a pass gate (**Figure 7.1c**). The transmission gate comprises both an n-type and a p-type device in parallel, whereas a pass gate only has a single transistor, shown here by a lone p-type. The channel in a field-effect transistor will only conduct when $V_{GS} > V_T$. In other words, assuming a supply rail between 0 V and V_{DD}, an n-type transistor with $V_G = V_{SEL}$ can only pass voltage between 0 V and $V_{SEL} - V_T$, and a p-type transistor with $V_G = V_{SEL}$ can only pass voltages between $V_{SEL} + V_T$ and V_{DD}. The transmission gate having both n-type and p-type devices can therefore successfully pass any value between 0 V and V_{DD}, as at least one of the transistors will be fully on. However, a p-type only pass gate will only pass input voltages greater than $V_{SEL} + V_T$. This is the major drawback with the p-type pass gate – in order to pass voltages down to 0 V, a gate-voltage of $V_G = -V_T$ is required. A secondary issue is also apparent here. If V_{SEL} is provided by a logic gate, such as an inverter, then V_{SEL} will almost certainly be greater than 0 V.

A second problem is the on-resistance of the channel. If the load is capacitive, as a gate input would normally be, then the load can be charged to the full final voltage.

If the load is resistive, then a constant current through the analogue switch will cause a voltage drop across the switch, reducing the value at the load.

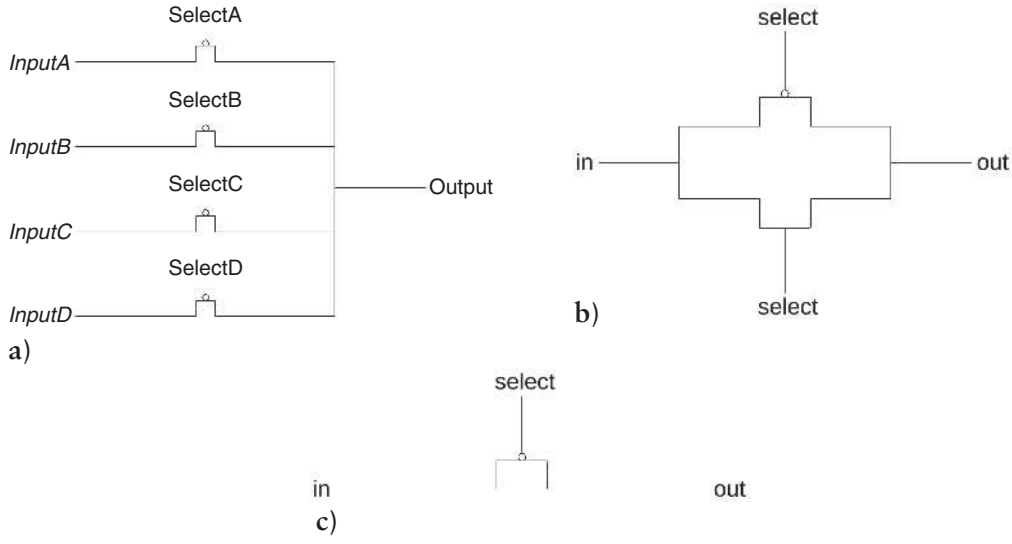


Figure 7.1 Analogue selector and switches: (a) four-to-one selector; (b) transmission gate with complementary transistors; and (c) p-type pass gate

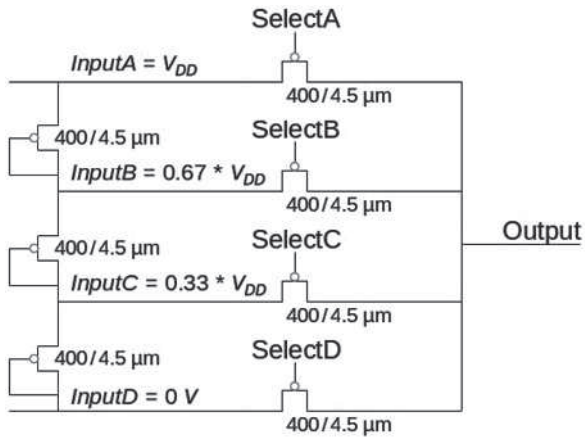
7.2.2 Experimental

A test circuit of the analogue selector (**Figure 7.2**) was designed and fabricated on PEN foil. To ease the probe testing of the sample, the four input voltages were supplied by a voltage divider constructed from diode-connected transistors anchored at either end by 0 V and V_{DD}. This provided input voltage values of $InputA = V_{DD}$, $InputB = 0.67 \times V_{DD}$, $InputC = 0.33 \times V_{DD}$, and $InputD = 0$ V. Instead of being directly driven from the power supply, the select inputs were supplied by a p-type diode-load inverter – driving transistor $W/L = 1{,}600/4.5$ μm load transistor $W/L = 100/4.5$ μm – in order to provide a more realistic operating environment. The selector was then tested across a range of supply voltages from 2.5 to 40 V.

7.2.3 Results

The results of the analogue selector are tabulated in **Figure 7.2** and plotted in **Figure 7.3**. The table shows the measured values, and, as expected, the selector is unable to pass the lower voltage values. The value of the select node was also measured, and this was added to the threshold-voltage obtained from the model

parameter extraction to give the $V_{SEL} + V_T$ value. The $V_{SEL} + V_T$ value represents the lowest voltage that the selector can be expected to pass correctly. The inputs, outputs, and $V_{SEL} + V_T$ values are all plotted together in **Figure 7.3** as both measured values and normalised values. *OutputA* and *OutputB* (corresponding to the higher input voltage values) work well across a wide range of supply voltages. However, *OutputC* and *OutputD* (the lower input voltage values) are not producing any valid function across any measurements. As an aside, the performance of the voltage divider was very good, with close correspondence to the expected values.



	10 V	20 V	30 V	40 V	Units
InputD	0	0	0	0	V
InputC	3.52	6.79	10.18	13.60	
InputB	6.65	13.40	20.13	26.87	
InputA	10.0	20.0	30.0	40.0	
V_{SEL}	3.88	6.87	9.69	12.39	
OutputD	5.24	10.68	15.70	20.59	
OutputC	6.01	10.91	15.34	19.60	
OutputB	6.81	13.42	20.07	26.76	
OutputA	9.64	19.73	29.52	39.23	
$\lvert V_T \rvert$	6.4	6.4	6.4	6.4	
$V_{SEL} + \lvert V_T \rvert$	10.28	13.27	16.09	18.79	

Figure 7.2 Four-to-one selector test circuit and measurements at various V_{DD} supply voltages

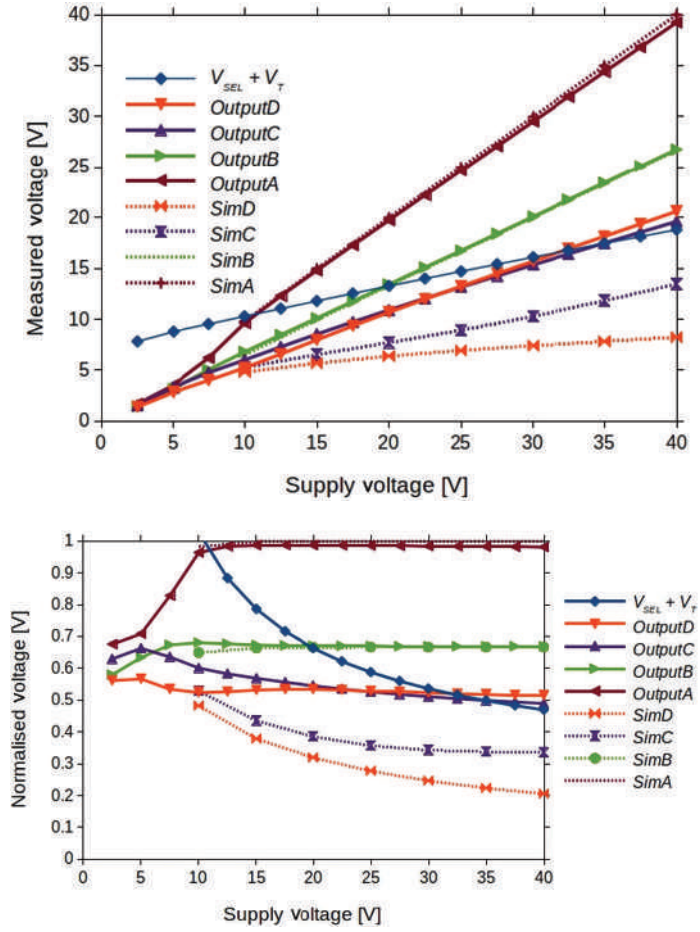


Figure 7.3 Analogue selector measured and simulated results. The $V_{SEL} + V_T$ line indicates the lower boundary of expected correct switch operation: (a) measured values and (b) normalised measured values

The analogue selector was also simulated, and the results are also plotted in **Figure 7.3**. For the higher values of input voltage, the simulation agrees quite closely with the measured data (*SimA* and *SimB*). For the lower values, there is a discrepancy, as the simulation predicts that *OutputC* should work at the higher supply voltages. It was observed in the previous section on the digital inverter that the simulation values were lower than the measured values. For the selector, that leads to a lower $V_{SEL} + V_T$, and hence a lower operating boundary.

7.3 Differential Amplifier

7.3.1 Description

Just as the inverter is the base building block for digital communication, so the differential amplifier is the base building block for analogue signal processing. A versatile circuit, the function of the basic differential amplifier is to amplify the difference between its two inputs to produce a differential output across the two output pins while rejecting any common mode signals on the inputs. With reference to **Figure 7.4**, the large signal function of the differential amplifier is expressed by the following equation:

$$V_{out+} - V_{out-} = A_d\left(V_{in+} - V_{in-}\right) + A_c\frac{\left(V_{in+} + V_{in-}\right)}{2} \tag{7.1}$$

where A_d is the differential mode gain and A_c is the common mode gain. For simplification, or for an ideal amplifier, the common mode gain, A_c, can be approximated to zero, thus:

$$V_{out+} - V_{out-} = A_d\left(V_{in+} - V_{in-}\right) \tag{7.2}$$

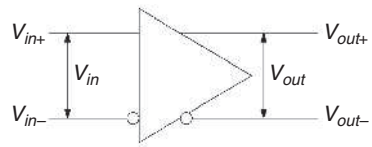


Figure 7.4 Differential amplifier pin view

The basic differential amplifier circuits shown in **Figure 7.5** have three parts: a current source (M5), two identical input transistors (M1, M2), and two identical load devices (M3, M4 or R3, R4). The three different configurations of differential amplifiers shown differ only in their load devices:

1. Resistive loads (**Figure 7.5a**) are often used for their simplicity. Their use is dependent on the availability of on-chip resistors.

2. Diode-connected transistor loads (**Figure 7.5b**) offer a higher small-signal resistance than passive resistors for a smaller area. This leads to a higher overall gain for the amplifier (**Equation 7.4**); however, the load transistors must remain in saturation, which requires greater voltage headroom.

3. If only a single-ended output is required, then a current mirror load (**Figure 7.5c**) may be used. Current from the unused leg is mirrored to the output leg of the

differential amplifier, effectively doubling the gain of the single-ended amplifier. Note that the current mirror is constructed from complementary transistors.

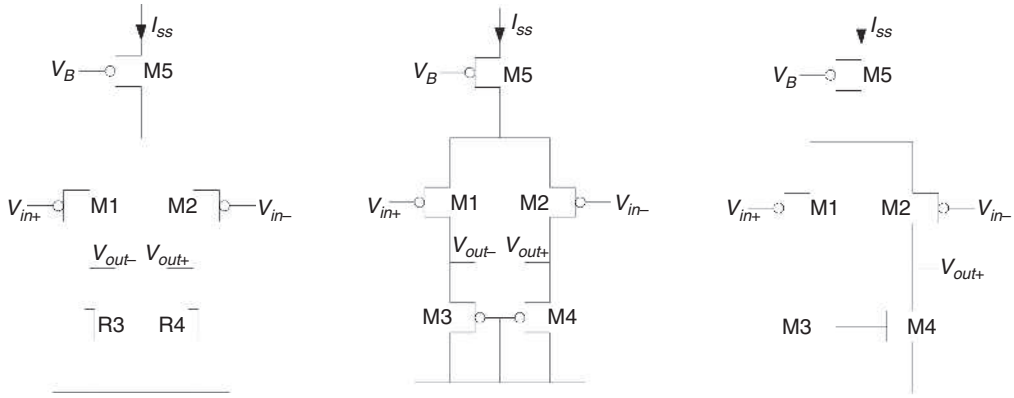


Figure 7.5 Differential amplifiers with different load types: (a) resistive loads; (b) diode-connected transistor loads compatible with p-type only technologies; and (c) single-ended output with current mirror loads requiring complementary devices

The DC operation of the differential amplifier can be explained qualitatively as follows, noting that the description is for a p-type technology. If V_{in+} increases and V_{in-} decreases, then V_{GS1} is reduced relative to V_{GS2} and M2 turns on harder than M1. As the current source M5 provides a constant current, then more current will flow through M2 than M1, i.e. $I_{DS2} > I_{DS1}$. At this point, the type of load will affect the output. For the resistive load, less current through M1 means that less voltage is dropped across R3 than R4, leading to V_{out-} falling and V_{out+} rising. The same is also true for the diode-connected transistor loads, though as the transistor loads are in saturation, they should provide a greater voltage change for the same current change, which leads to a higher gain. For the current mirror load, a reduction in current in M3 is mirrored to M4. But M2 is simultaneously trying to drive more current through, so the current available to a single-ended load at V_{out+} is effectively doubled compared with a single output of the resistive or diode-connected transistor load differential amplifiers.

The transconductance, g_m, and differential voltage gain, A_d, for a differential amplifier with a resistive or diode-connected transistor load are [10]

$$g_m = \frac{\mathrm{d}(i_{out})}{\mathrm{d}(V_{in})} = \sqrt{\left(\mu C_{diel} I_{ss} \frac{W}{L}\right)} \tag{7.3}$$

$$A_d = g_m R_L \tag{7.4}$$

where i_{out} is the differential output current, $V_{in} = V_{in+} - V_{in-}$ is the differential input voltage, μ is the mobility of the semiconductor, C_{diel} is the dielectric capacitance per unit area, I_{SS} is the current source current, and R_L is the load resistance. From these equations it can be seen that g_m is proportional to I_{SS}. For organic devices, both μ and I_{SS} are low when compared with silicon. For example, the typical values for silicon are μ =500 cm^2/Vs and I_{SS} = 1 mA, and for organic devices μ =1 cm^2/Vs and I_{SS} =100 μA, so the gain due to the technology alone is immediately attenuated by a factor of 71 or 37 dB.

The gain of the differential amplifier (**Equation 7.4**) depends intimately on the load resistance. For a diode-connected transistor load, the small-signal resistance is given by [10]

$$r_{ds} = \frac{1}{\mu C_{diel} \frac{W}{L}\left(V_{GS} - V_T\right)} \tag{7.5}$$

For typical values of W/L = 120/4.5 µm, values of r_{ds} = 15 MΩ can be expected.

7.3.2 Experimental

For this test foil, four different diode-connected transistor load differential amplifiers were designed and fabricated and their DC characteristics measured. The transistor dimensions were based on work by Marien and co-workers [6] who had reported a differential gain of A_d = 8 (18 dB) at 15 V. One of the differential amplifiers under test (Diff 1) had almost identical dimensions to the Marien example. A sensitivity analysis was performed whereby the other three test circuits varied the dimensions of the input transistors (Diff 2), load transistors (Diff 3) and current source (Diff 5) one at a time. To ease the testing and probing (maximum of four probe points), an on-foil voltage divider provided the input voltages for the current source M5 and the input transistor M2 (**Figure 7.6**).

7.3.3 Results and Analysis

The results of measurements, simulations, and manual calculations are given in **Table 7.1** and **Figure 7.7a**. There are several observations to be made:

- The presented differential amplifier is not functioning correctly; in particular, there is an asymmetrical DC transfer function. This is due to the transistors of the differential amplifier not being in their correct operating regions.

- Increasing the size of the load transistors led to the best performance (Diff 3).

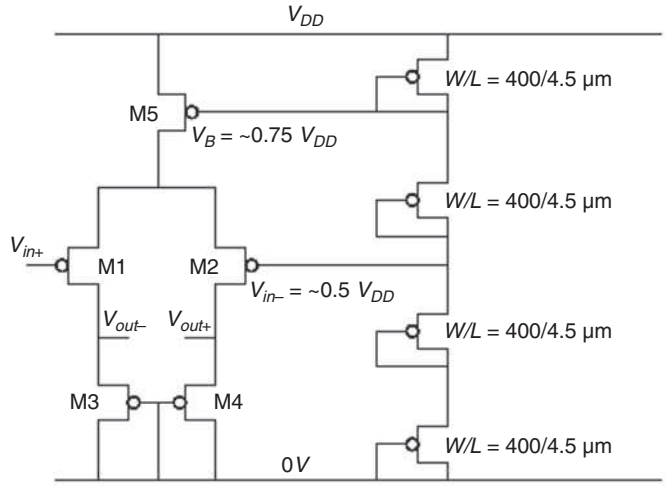


Figure 7.6 Differential amplifier test harness requiring four probes: 0V, V_{DD}, V_{in+}, and output

Table 7.1 Differential amplifier test and simulation results

	Marien [6]	**Diff 1**	**Diff 2**	**Diff 3**	**Diff 5**	**Mod 3**	**Units**
Transistor sizes							
Current source (M5)	10,000/5	10,000/4.5	10,000/4.5	10,000/4.5	20,000/4.5	2,500/4.5	µm
Input (M1, M2)	3,700/5	3,700/4.5	7,400/4.5	3,700/4.5	3,700/4.5	3,700/4.5	
Load (M3, M4)	120/5	120/4.5	120/4.5	240/4.5	120/4.5	240/4.5	
Gain for differential input = 0 V at V_{DD} = 40 V							
Measured gain	8 (at 15 V)	0.28	0.22	1.45	0.20	—	V/V
Simulated gain	—	0.65	0.47	1.43	0.34	2.32	
Calculated gain	—	35.8	50.7	17.9	50.7	9.0	

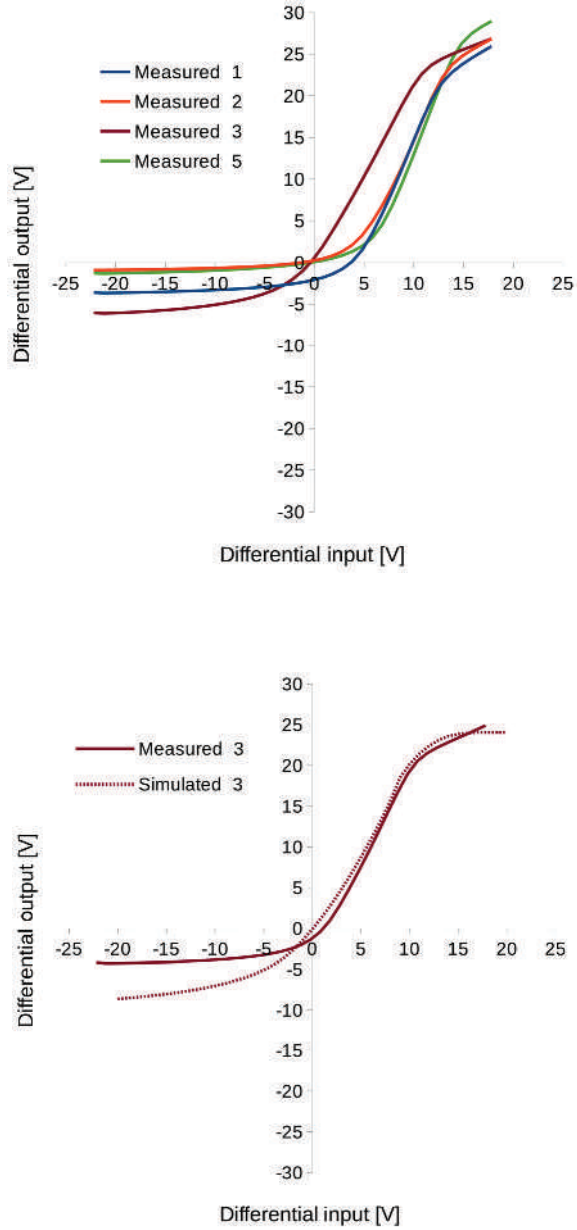


Figure 7.7 Differential amplifier results at V_{DD} = 40 V: (a) measurements from four different designs and (b) comparison of measured and simulated results for a single differential amplifier, Diff 3

- Increasing the size of the input transistors led to a marginal improvement (Diff 2).
- Increasing the size of the current source degraded performance further (Diff 5).
- The measured gain at a differential input of 0 V is not reliable for these measurements on account of the asymmetry.
- The simulated and measured transfer curves show a reasonably strong correlation (**Figure 7.7b**).
- The manually calculated gains, using **Equations 7.3** to **7.5**, are noticeably inaccurate. This is due to the difficulty in estimating the correct voltages at the nodes between transistors for V_{DS} values (simulators are better at this!). The best that can be inferred from the calculated values is the trend when a parameter is altered.

In order to diagnose the functional problems, the differential circuit Diff 3 was simulated for further analysis to expose its internal voltages. From the simulated data (**Figure 7.8a**) it can be seen that the current source M5 V_{DS} is low compared with its V_{GS}, possibly causing M5 to come out of saturation, and also the behaviour of the load transistors M3 and M4 is asymmetrical. By reducing the size of the current source transistor to W/L = 2,500/4.5 μm, M5 is able better to maintain a constant current, and the behaviour of the load transistors M3 and M4 becomes more symmetrical, as shown in the simulation in **Figure 7.8b**.

7.3.4 Monte Carlo Simulation

The modified Diff 3 differential amplifier was further simulated for Monte Carlo analysis (100 runs) using the same methodology as previously described for Monte Carlo simulations. The results, presented in **Figure 7.8c**, show that symmetry is maintained across the expected spread of μ_0 and V_T variations. The simulated gain values varied from a minimum of 1.61 V/V (4.1 dB) to a maximum of 2.79 V/V (8.9 dB), with a mean of 2.20 V/V (6.8 dB) and a standard deviation of 0.59 V/V.

7.3.5 Comparison with Published Work

The results for Diff 1 were based directly on the design published by Marien and co-workers [6]. Yet, while the gain reported by Marien and co-workers was 8 (18 dB) at 15 V, Diff 1 showed a measured gain of only 0.28 (-11 dB) at 40 V. The reasons for this difference from two identical designs should be briefly discussed.

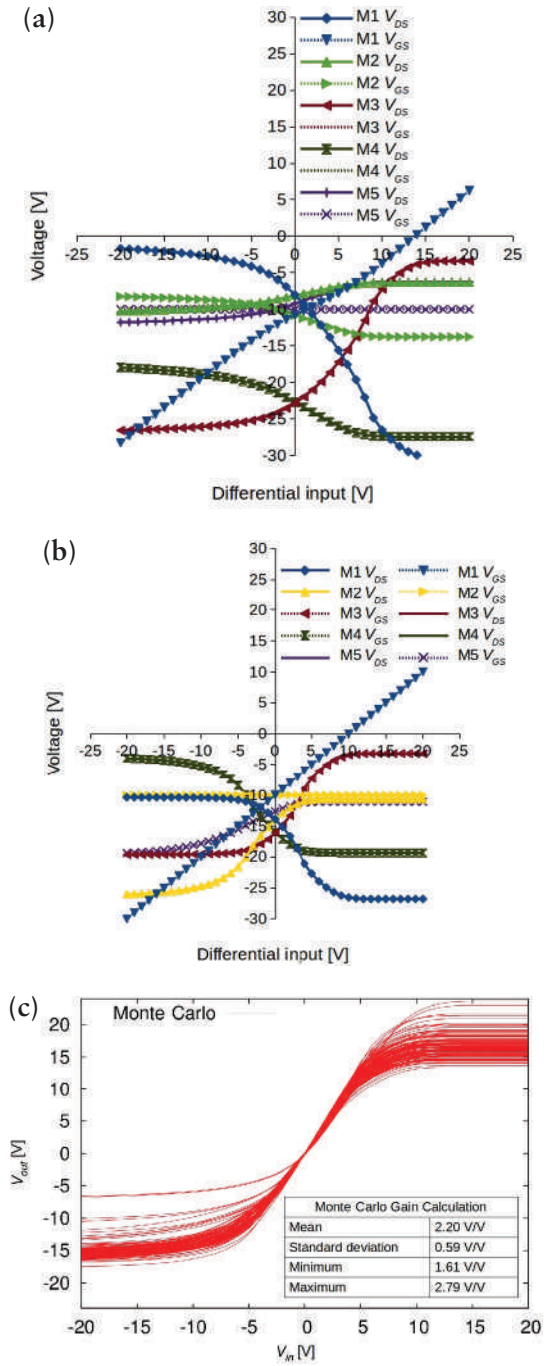


Figure 7.8 Differential amplifier simulations: (a) Diff 3 internal nodes at V_{DD} = 40 V; (b) modified Diff 3 internal nodes at 40 V; and (c) 100 Monte Carlo simulations of the modified Diff 3

The most obvious parameter affecting the gain is the semiconductor mobility, μ. From **Equations 7.3** to **7.5** it can be worked out that the differential amplifier gain is directly proportional to the mobility. The mobility of the semiconductor is not given by Marien and co-workers but is implied to be between 0.1 and 1.0 cm^2/Vs, whereas the mobility of the Diff 1 semiconductor was measured to be 0.06 cm^2/Vs (**Table 4.4**). This calculates to a ×10 difference in the gain due to the semiconductor mobility alone.

The other process parameter to affect the differential amplifier gain is the threshold-voltage, V_T. In the differential amplifier gain equations, V_T is closely linked to the V_{GS} of the transistor in saturation, which is either the current source transistor or the diode-connected load transistor. Marien and co-workers are able to change the V_T of their transistors by the use of a back gate, and values of 2–3 V are shown in the figures. For the Diff 1 differential amplifier, the measured V_T was 6.4 V. A smaller V_T will lead to a larger current source value I_{SS} but also reduce the small-signal load resistance. To ease the analysis, for a transistor in saturation such as the load transistors, qualitatively, the gradients of the I_{DS}–V_{DS} curves probably do not vary by a great amount as $V_{GS} - V_T$ is swept. However, if the V_{GS} of the current source is assumed to be initially approximately double V_T, then a halving of V_T will lead to a differential amplifier gain increase of ×1.5.

Taking these two factors together would lead to an increase in gain of ×15, i.e. a gain increase from 0.28 to 4.2 (12 dB), which is closer to the values published by Marien and co-workers, albeit at 40 V instead of 15 V.

7.4 Summary

In this chapter, two basic analogue circuits have been introduced – the analogue selector and the differential amplifier. Examples of both these circuits have been fabricated, measured, and analysed, and the results compared against simulations. Manual functional evaluation and performance estimation are more difficult for analogue design, and although the accuracy needs improvement, and additional simulation methods such as transient and AC simulations need to be undertaken, simulations have shown their value in analysing and diagnosing analogue circuit design problems. A methodology of model and simulation refinements should lead to a reliable design flow, which will enable the right-first-time future design of analogue circuits.

References

1. H. Casier, M. Steyaert and A.H.M. van Roermund, *Analog Circuit Design*, Springer, New York, NY, USA, 2011.

2. B. Murmann and W. Xiong in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2010, p.504.

3. M.G. Kane, J. Campi, M.S. Hammond, F.P. Cuomo, B. Greening, C.D. Sheraw, J.A. Nichols, D.J. Gundlach, J.R. Huang, C.C. Kuo, L. Jia, H. Klauk and T.N. Jackson, *IEEE Electron Device Letters*, 2000, **21**, 534.

4. N. Gay, W.J. Fischer, M. Halik, H. Klauk, U. Zschieschang and G. Schmid, *International Solid-State Circuits Conference*, 2006, **6**, 1070.

5. N. Gay and W. Fischer in *Proceedings of the 65th IEEE Polytronic Conference 2007*, Tokyo, Japan, 2007, p.143.

6. H. Marien, M. Steyaert, E. van Veenendaal and P. Heremans, *Organic Electronics*, 2010. **11**, 1357.

7. G. Maiellaro, E. Ragonese, A. Castorina, S. Jacob, M. Benwadih, R. Coppard and E. Cantatore, *IEEE Transactions on Circuits and Systems*, 2013, **60**, 3117.

8. H. Maren, M.S.J. Steyaert, E. Van Veenendaal and P. Heremans, *IEEE Journal of Solid-State Circuits*, 2011, **46**, 276.

9. H. Marien, M.S.J. Steyaert, E. van Veenendaal and P. Heremans, *IEEE Journal of Solid-State Circuits*, 2012, **47**, 1712.

10. P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design*, Holt, Rinehart & Winston, Inc., New York, NY, USA, 1987.

Appendix Simulation Program with Integrated Circuit Emphasis

A1.1 Introduction

SPICE is an acronym standing for Simulation Program with Integrated Circuit Emphasis but is so ubiquitous that, like *hoover*, *xerox*, and, more recently, *google* and *text*, it has entered the lexicon of everyday usage and become a verb. Originally conceived in 1973 by Nagel and Pederson [1], SPICE is the most important program for integrated circuit design, and every very-large-scale integration transistor-level circuit designer will be intimately familiar with the use of either SPICE itself or one of its descendants. However, knowledge of its internal workings and algorithms is not so widespread. In particular, an appreciation of SPICE core algorithms, while not entirely essential, will make for efficient modelling, and is extremely useful for debugging simulation problems with circuit design. In this appendix, the SPICE core algorithms are explored, and how the model itself fits into SPICE [2–4].

Table A1.1 lists some of the more notable variants of SPICE [3]. All are based on the original Berkeley written in Fortran. The latest versions, now written in C, are much quicker, can handle larger circuits, and have fewer convergence issues.

Table A1.1 Notable SPICE simulators

Date	SPICE Variant	Note
1972	Berkeley SPICE	The original
	ISPICE	First commercial SPICE
	HSPICE	First widely used SPICE
1984	PSPICE	First PC-based SPICE
1990	Spectre	Cadence
	Eldo	Mentor Graphics
	ngspice	(Free)

Adapted from W. Liu in MOSFET *Models for SPICE Simulation including BSIM3v3 and BSIM4*, Wiley-Blackwell, Hoboken, NJ, USA, 2001 [3]

A1.2 Simulation Program with Integrated Circuit Emphasis Operation

SPICE can be considered to be of a modular design consisting of a number of core functional blocks, each with a specific purpose. These blocks interact and communicate with each other to process the simulation data. As all the simulations in this book are either DC or transient simulations, the three blocks involved in those types of simulation are now described. For simplicity, other types of analysis such as AC or noise are not covered.

A1.2.1 Nodal Analysis

This is the core engine which drives SPICE. Kirchoff's laws state that the sum of currents into and out of a node is zero. In a linear-only circuit, by replacing all of the circuit components with their mathematical equivalents and applying Kirchoff's laws, nodal analysis is able to recast the circuit in terms of a matrix of only conductances, voltages, and currents. This is shown in general form in **Equation A1.1**:

$$\begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{A1.1}$$

SPICE solves the matrix inversion using the Gaussian elimination method, **Equation A1.2**:

$$V = G^{-1} \times i \tag{A1.2}$$

A1.2.1 DC Analysis

If there is a non-linear component in the circuit – diode, capacitor, inductor, transistor – then the circuit must first be converted to a linear equivalent. In the example shown in **Figure A1.1**, the initial operating point, which may be guessed or manually provided, is at value v_0. This is transformed into a linear mathematical equivalent, and then nodal equations are developed and solved by nodal analysis to give a new value at v_1. This Newton–Raphson process repeats until SPICE determines convergence and ends.

A1.2.3 Transient Analysis

Transient analysis is the term used to describe simulation in the time domain [5]. In order to perform a time domain simulation, a step function is applied to move a circuit from one stable state to another, hence the term transient. As in the DC analysis,

transient analysis must first transform any energy storage components into a linear counterpart. Using numerical integration techniques, a prediction is made of the voltage at the next time point by considering the slope of the function (**Figure A1.2**). **Equation A1.3** shows an example with a forward Euler technique:

$$V_{n+1} = V_n + h\frac{\mathrm{d}V_n}{\mathrm{d}t} \tag{A1.3}$$

By substituting $V = Q/C$ and $I = dQ/dt$, this is transformed into its linear equivalent suitable for nodal analysis, shown in general form in **Equation A1.4:**

$$I_{n+1} = \mathrm{G}V_{n+1} + \mathrm{G}V_n \tag{A1.4}$$

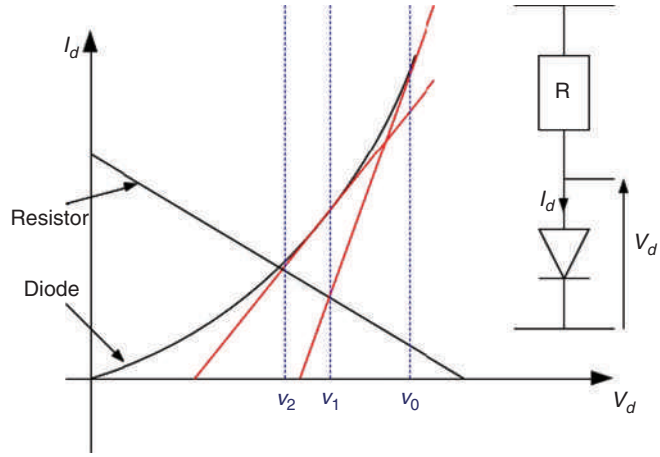


Figure A1.1 Load-line example of a non-linear diode with a linear resistive load being solved by an iterative Newton–Raphson method

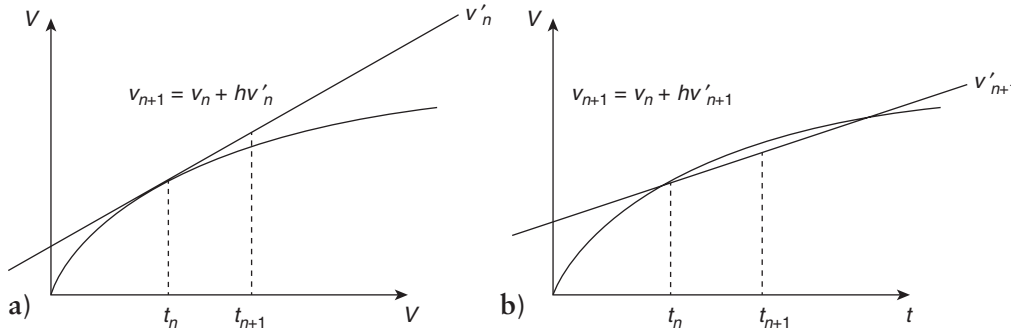


Figure A1.2 Temporal evolution: (a) forward Euler; (b) backward Euler, which offers more accuracy and stability [2, 4, 5]

A1.2.4 SPICE Algorithm Overview

A simplified transient analysis algorithm is shown in **Figure A1.3**. Simple linear DC analysis involves blocks 3 and 4 only. If there are non-linear components, blocks 1 to 6 are looped around until convergence is attained. During linear transient analysis, for each time point, only the outer loop 9 is traversed, excluding 2 and 5. For non-linear transient analysis, the inner loop 2 to 6 is additionally transversed at each time point.

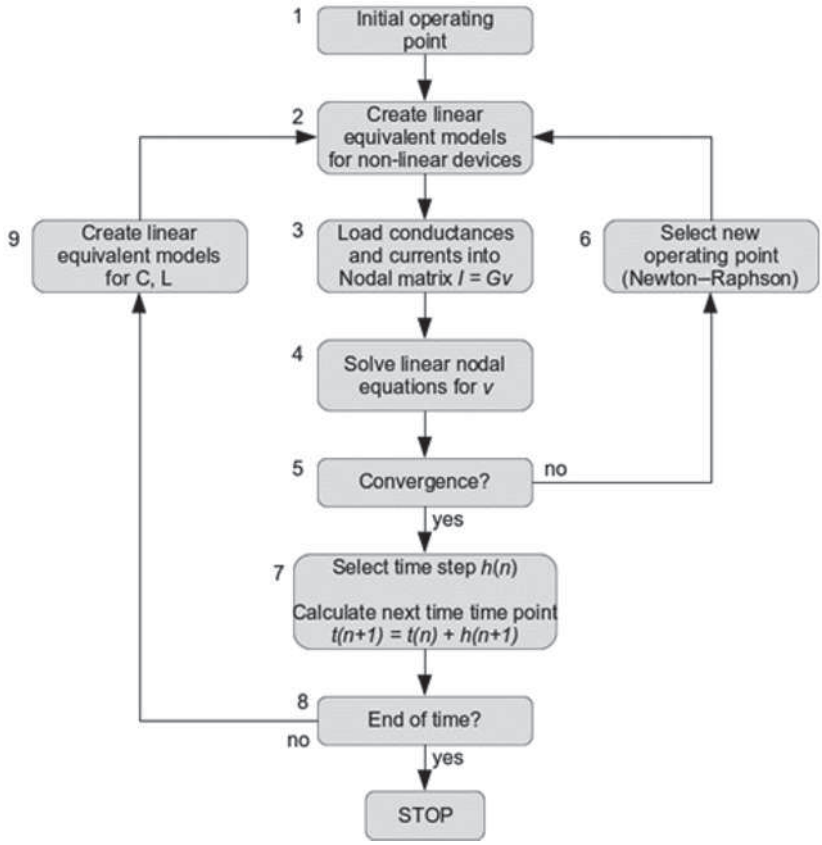


Figure A1.3 Simplified SPICE algorithm [4]

References

1. L. Nagel and D. Pederson in *SPICE*, University of California, Berkeley, CA, USA, 1973.

2. T.A. Fjeldly, T. Ytterdal and M.S. Shur in *Introduction to Device Modeling and Circuit Simulation*, Wiley-Interscience, New York, NY, USA, 1997.

3. W. Liu in *MOSFET Models for SPICE Simulation including BSIM3v3 and BSIM4*, Wiley-Blackwell, Hoboken, NJ, USA, 2001.

4. E Circuit Center, 2011.
http://www.ecircuitcenter.com/index.htm

5. V. Litovski and M. Zwolinski in *VLSI Circuit Simulation and Optimization*, Chapman & Hall, London, UK, 1997.

Abbreviations

AC	Alternating current
ADC	Analogue–digital converters
BJT	Bipolar junction transistor(s)
BSIM	Berkeley short-channel IGFET model
BT	Benzothiadiazole
BTBT	Benzothienobenzothiophene
$C_{22}H_{14}$	Pentacene
CMOS	Complementary metal-oxide semiconductor
DC	Direct current
DFF	D-type flip flop(s)
dif-TESADT	Difluorinated-triisopropylsilylethynyl anthradithiophene
DPP	Diketopyrrolopyrrole
DRC	Design rule check(s)
E_a	Electron affinity
EDA	Electronic design automation
ELR	Extrapolation of linear region
EKV	Enz–Krummenacher–Vittoz
E_r	Relative permittivity
ESR	Extrapolation of saturation region
HDL	Hardware description language
HOMO	Highest occupied molecular orbit
IDT	Indacenodithiophene
I_p	Ionisation potential
LUMO	Lowest unoccupied molecular orbit

LVS	Layout *versus* schematic
MOS	Metal-oxide semiconductor
MOSFET	Metal-oxide semiconductor field-effect transistor
MTR	Multiple trap and release
NLLS	Non-linear least-square(s)
OFET	Organic field-effect transistor(s)
OLED	Organic light-emitting diode(s)
OPV	Organic photovoltaic(s)
OTFT	Organic thin-film transistor
PAL	Programmable array logic
PBTTT	Poly(2,5-*bis*(3-alkylthiophen-2-yl)thieno[3,2-*b*]thiophene)
PEN	Polyethylene naphthalate
PMMA	Polymethyl methacrylate
PVDF	Polyvinylidene fluoride
RC	Resistor and capacitor
RFID	Radio frequency identification
SD	Standard deviation
SPA	Semiconductor parameter analyser
SPICE	Simulation program with integrated circuit emphasis
TDK	Technology design kit
TFT	Thin-film transistor
TESADT	Triethylsilylethynyl anthradithiophene
TIPS	Triisopropyl-silylethynyl
TIPS-P	6,13-*Bis*(triisopropyl-silylethynyl)pentacene
VCO	Voltage-controlled oscillator
VLSI	Very-large-scale integration
WSSR	Weighted sum of squared residual(s)
Φ_w	Work function

Index

Pages followed by 'f' and 't' refer figures and tables respectively.

C

D

E

F

G

H

I

K

L

M

N

O

P

Q

R

S

T

V

W

Y

Z

ISBN 978-1-91024-270-4
90000
9 781910 242704

Published by Smithers Rapra Technology Ltd, 2016

The field of organic electronics spans a very wide range of disciplines from physics and chemistry to hardware and software engineering. This makes the field of organic circuit design a daunting prospect full of intimidating complexities, yet to be exploited to its true potential. Small focused research groups also find it difficult to move beyond their usual boundaries and create systems-on-foil that are comparable with the established silicon world.

This book has been written to address these issues and is intended for two main readerships: firstly, physics or materials researchers who have thus far designed circuits using only basic drawing software; secondly, experienced silicon CMOS VLSI design engineers who are already knowledgeable in the design of full custom transistor-level circuits but are not familiar with organic devices or thin-film transistor devices. In guiding the reader through the disparate and broad subject matters, a concise text has been written covering the physics and chemistry of the materials, the derivation of the transistor models, the software construction of the simulation compact models, and the engineering challenges of a right-first-time design flow, with notes and references to the current state-of-the-art advances and publications. Real-world examples of simulation models, circuit designs, fabricated samples, and measurements have also been given, demonstrating how the theory can be used in applications.

SMITHERS RAPRA

Shawbury, Shrewsbury, Shropshire, SY4 4NR, UK
Telephone: +44 (0)1939 250383
Fax: +44 (0)1939 251118
Web: www.polymer-books.com