Lecture Notes in Electrical Engineering 434

Suresh Chandra Satapathy
Vikrant Bhateja
P. Satish Rama Chowdary
V.V.S.S. Sameer Chakravarthy
Jaume Anguera
Editors

Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications

ICMEET 2016

Springer

Lecture Notes in Electrical Engineering

Volume 434

About this Series

"Lecture Notes in Electrical Engineering (LNEE)" is a book series which reports the latest research and developments in Electrical Engineering, namely:

- Communication, Networks, and Information Theory
- Computer Engineering
- Signal, Image, Speech and Information Processing
- Circuits and Systems
- Bioengineering

LNEE publishes authored monographs and contributed volumes which present cutting edge research information as well as new perspectives on classical fields, while maintaining Springer's high standards of academic excellence. Also considered for publication are lecture materials, proceedings, and other related materials of exceptionally high quality and interest. The subject matter should be original and timely, reporting the latest research and developments in all areas of electrical engineering.

The audience for the books in LNEE consists of advanced level students, researchers, and industry professionals working at the forefront of their fields. Much like Springer's other Lecture Notes series, LNEE will be distributed through Springer's print and electronic publishing channels.

More information about this series at http://www.springer.com/series/7818

Suresh Chandra Satapathy
Vikrant Bhateja · P. Satish Rama Chowdary
V.V.S.S. Sameer Chakravarthy
Jaume Anguera
Editors

Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications

ICMEET 2016

Springer

Editors
Suresh Chandra Satapathy
Deparment of Computer Science and Engineering
PVP Siddhartha Institute of Technology
Vijayawada, Andhra Pradesh
India

Vikrant Bhateja
Department of Electronics and Communication Engineering
Shri Ramswaroop Memorial Group
Lucknow, Uttar Pradesh
India

P. Satish Rama Chowdary
Department of ECE
Raghu Institute of Technology
Visakhapatnam, Andhra Pradesh
India

V.V.S.S. Sameer Chakravarthy
Department of ECE
Raghu Institute of Technology
Visakhapatnam, Andhra Pradesh
India

Jaume Anguera
Department of Electronics and Telecommunications
Universitat Ramon Llull
Barcelona, Barcelona
Spain

ISSN 1876-1100 ISSN 1876-1119 (electronic)
Lecture Notes in Electrical Engineering
ISBN 978-981-10-4279-9 ISBN 978-981-10-4280-5 (eBook)
DOI 10.1007/978-981-10-4280-5

Library of Congress Control Number: 2017935402

Printed on acid-free paper

This Springer imprint is published by Springer Nature
The registered company is Springer Nature Singapore Pte Ltd.
The registered company address is: 152 Beach Road, #21-01/04 Gateway East, Singapore 189721, Singapore

Preface

This volume contains high-quality research papers those were presented at the 2nd International Conference on Microelectronics, Electromagnetics and Telecommunications (ICMEET) held at Departments of Electronics and Communication Engineering of Raghu Engineering Institutions, Visakhapatnam, during 6–7 January 2017. ICMEET aims to bring together academic scientists, researchers and research scholars to discuss the recent developments and future trends in the fields of microelectronics, electromagnetics and telecommunication. Previous editions of the conference were held at GITAM University, Visakhapatnam. The ICMEET received totally 285 submissions for LNEE series of the conference. Each was peer reviewed by at least two members of the Program Committee. Finally, 72 papers were accepted for publication in these proceedings. The ICMEET was technically supported by IETE student forum and IE student chapter. Several special sessions were offered by eminent professors on many cutting-edge technologies. Several eminent researchers and academicians delivered talks addressing the participants in their respective field of proficiency. Topic on evolutionary computational tools and their application for engineering problems has been discussed by Prof. Ganapati Panda, Former Deputy Director, IIT BBSR. A thorough discussion on the opportunities for engineering aspirants in foreign countries in the field of electrical and electronics is presented by Prof. Naeem Hannoon from Malaysia. Professor Lakhmi C. Jain delivered a talk on artificial intelligence paradigms and their applications in complex systems, security, e-education, e-healthcare, unmanned air vehicles and intelligent agents. A brief talk on optical devices and modelling is delivered by Dr. T. Srinivas, IISc Bengaluru followed by a discussion on topic of image processing for research by Prof. S. Srinivas Kumar, JNTU Kakinada.

We would like to express our appreciation to the members of the Program Committee for their support and cooperation in this publication. We are also thankful to Springer team for providing a meticulous service for the timely production of this volume. Our heartfelt thanks to our Chairman Sri Kalidindi Raghu and other management members of Raghu Educational Society for extending wholehearted support to host this in their campus. Special thanks to all guests who

have honoured us in their presence in the inaugural day of the conference. Our thanks are due to all special session Chairs, track managers and reviewers for their excellent support. Last, but certainly not least, our special thanks go to all the authors who submitted papers and all the attendees for their contributions and fruitful discussions that made this conference a great success.

Vijayawada, India — Suresh Chandra Satapathy
Lucknow, India — Vikrant Bhateja
Visakhapatnam, India — P. Satish Rama Chowdary
Visakhapatnam, India — V.V.S.S. Sameer Chakravarthy
Barcelona, Spain — Jaume Anguera
January 2017

Organizing Committee

Chief Patrons
Shri. Kalidindi Raghu, Chairman, Raghu Educational Society
Smt. K. Rama Devi, Secretary, Raghu Educational Society

Patrons
Shri. K. Rahul Varma, Director, Raghu Educational Society
Shri. S. Veerabhadriah, Correspondent, Raghu Educational Society
Prof. I.S.N. Raju, Advisor, Raghu Educational Society

Chairmen
Prof. R. Kameswara Rao, Principal, Raghu Engineering College
Prof. Ch. Prabhakara Rao, Principal, Raghu Institute of Technology

Program Co-Ordinator
Dr. P. Satish Rama Chowdary, Vice Principal, Raghu Institute of Technology

Special Session Chairs
Dr. Sudheer Kumar Terlapu
Prof. Tumati Venkateswara Rao
Dr. Kakarla Hari Kishore

Conveners
Dr. V.V.S.S. Sameer Chakravarthy, Associate Professor, Department of ECE, Raghu Institute of Technology
Sri. K. Phanindra Vinay, HOD, Department of ECE, Raghu Engineering College

Co-Conveners
Sri. B.S.S.V. Ramesh Babu, Associate Professor, Raghu Institute of Technology
Sri. K. Sathi Raju, Associate Professor, Raghu Engineering College

Proceedings Committee
Dr. Ashish Singh, Associate Professor, Raghu Engineering College
Ms. M. Kalpana, Associate Professor, Raghu Institute of Technology

Mr. Lalbabu Prasad, Assistant Professor, Raghu Engineering College
Mr. Anil Kumar Patnaik, Assistant Professor, Raghu Institute of Technology
Mr. P. Rajesh, Assistant Professor, Raghu Engineering College

Technical Program Committee

Ms. A. Sai Ramya, Assistant Professor, Raghu Institute of Technology
Mr. S. Suresh, Assistant Professor, Raghu Institute of Technology
Mr. B. Ramesh, Assistant Professor, Raghu Engineering College
Mr. N. Markendeya Guptha, Associate Professor, Raghu Engineering College
Mrs. P. Unita, Assistant Professor, Raghu Institute of Technology
Mr. Mrs. K. Madhavi, Assistant Professor, Raghu Engineering College

Organising Committee

Mr. M. Pavan, Assistant Professor, Raghu Institute of Technology
Mr. K. Phaneendra, Assistant Professor, Raghu Institute of Technology
Mr. S. KUMAR, Assistant Professor, Raghu Engineering College
Mr. Gupteswar Sahu, Assistant Professor, Raghu Engineering College
Mr. D. Bhaskara Rao, Assistant Professor, Raghu Engineering College
Mr. E.V. Raju, Assistant Professor, Raghu Engineering College

Publicity Committee
Sri. P.V.K. Durga Prasad, Associate Professor, Raghu Institute of Technology
Sri. A. Murali, Associate Professor, Raghu Engineering College
Mr. K. Chandra Sekhar, Assistant Professor, Raghu Institute of Technology
Mr. Y.L.V. Santosh Kumar, Assistant Professor, Raghu Engineering College
Mr. P. Sankara Rao, Assistant Professor, Raghu Engineering College

Finance Committee

Ms. M. Meena Kumari, Associate Professor, Raghu Engineering College
Ms. A.V.S. Swathi, Assistant Professor, Raghu Institute of Technology
Ms. A. Sirisha, Assistant Professor, Raghu Institute of Technology
Mrs. M. Vandana, Assistant Professor, Raghu Engineering College
Mrs. Ch. Sravani, Assistant Professor, Raghu Engineering College

Hospitality Committee

Mr. K.S. Ravi Kumar, Assistant Professor, Raghu Engineering College
Mr. G. Ganeswara Rao, Assistant Professor, Raghu Institute of Technology
Mr. Y.V.S. Charan, Assistant Professor, Raghu Engineering College
Mr. P. Anil Kumar, Assistant Professor, Raghu Engineering College
Ms. A. Swetha, Assistant Professor, Raghu Engineering College

Transportation Committee

Mr. P. Pydi Reddy, Assistant Professor, Raghu Institute of Technology
Mr. G. Santhosh, Assistant Professor, Raghu Institute of Technology
Mr. M. Jagan Mohanarao, Assistant Professor, Raghu Institute of Technology
Mr. Y.E. Vasanth Kumar, Assistant Professor, Raghu Engineering College
Mr. MD. Rameez, Assistant Professor, Raghu Engineering College

International and National Advisory Committee

Prof. Jaume Anguera, Universitat Ramon Llull, Spain
Dr. Tan Shing Chiang, Multimedia University, Malaysia
Dr. Matthew Teow Yok Wooi, Head, KDU University, Malaysia
Dr. Lipo-Wang, NTU Singapore
Prof. Fabrizio Bonani, Italy
Dr. A. Olatunbosun, University of Ibadan, Nigeria
Dr. Rajan A. Beera, Global Director of Engineering, Cortland, NY
Dr. K. Busawon, Professor, Northumbria University
Dr. V. Bhujanga Rao, DS & CC R&D (NS&IC)
Prof. Ganapati Panda, IIT Bhubaneswar
Prof R.V. Raja Kumar, IIT Bhubaneswar
Prof. R.K. Mishra, BU
Prof. G.S.N. Raju, AU
Prof. A. Mallikarjuna Prasad, JNTUK
Prof. S.K. Koul, Deputy Director (S&P), IIT Delhi
Prof. Shanthi Pavan, IIT Madras
Prof. Nandita Das Gupta, IIT Madras
Prof. Pallapa Venkata Ram, IISC Bangalore
Dr. Murthy Ramella Scientist-G, ISRO
Dr. P.V. Anada Mohan, ECIL, Hyderabad
Dr. C.D. Malleswar, Director, NSTL, Visakhapatnam
Dr. D. Sriram Kumar, NIT Trichy
Mr. Y.S. Mayya Associate Director, BARC

Mr. V. Balaji, Head-Wireless Deployment, Reliance Corporate Park, Navi Mumbai
Prof. Ch. Ramakrishna, Director-UGC, GU
Mr. Ramesh Chowdary, Semar Group, Hyderabad
Mr. B. Surendra Kumar, Ramvee Tech Sol, Hyderabad

About the Book

The book is a collection of best papers presented in the 2nd International Conference on Microelectronics Electromagnetics and Telecommunication (ICMEET 2016), an international colloquium, which aims to bring together academic scientists, researchers and research scholars to discuss the recent developments and future trends in the fields of microelectronics, electromagnetics and telecommunication. Microelectronics research investigates semiconductor materials and device physics for developing electronic devices and integrated circuits with data/energy efficient performance in terms of speed, power consumption, and functionality. The book discusses various topics like analogue, digital and mixed signal circuits, bio-medical circuits and systems, RF circuit design, microwave and millimeter wave circuits, green circuits and systems, analogue and digital signal processing, nanoelectronics and giga-scale systems, VLSI circuits and systems, SoC and NoC, MEMS and NEMS, VLSI digital signal processing, wireless communications, cognitive radio, and data communication.

Contents

About the Editors

Dr. Suresh Chandra Satapathy is currently working as Professor and Head, Department of Computer Science and Engineering at PVP Siddhartha Institute of Technology (PVPSIT), Vijayawada, Andhra Pradesh, India. He obtained his Ph.D. in Computer Science and Engineering from JNTU Hyderabad and M.Tech. in CSE from NIT, Rourkela, Odisha, India. He has 26 years of teaching experience. His research interests include data mining, machine intelligence and swarm intelligence. He has acted as program chair of many international conferences and edited 6 volumes of proceedings from Springer LNCS and AISC series. He is currently guiding 8 Ph.D. scholars. Dr. Satapathy is also a Senior Member of IEEE.

Prof. Vikrant Bhateja is Associate Professor, Department of Electronics & Communication Engineering, Shri Ramswaroop Memorial Group of Professional Colleges (SRMGPC), Lucknow and also the Head (Academics & Quality Control) in the same college. His area of research include digital image and video processing, computer vision, medical imaging, machine learning, pattern analysis and recognition, neural networks, soft computing and bio-inspired computing techniques. He has more than 90 quality publications in various international journals and conference proceedings. Professor Bhateja has been on TPC and chaired various sessions from the above domain in international conferences of IEEE and Springer. He has been the track chair and served in the core-technical/editorial teams for international conferences: FICTA 2014, CSI 2014 and INDIA 2015 under Springer-AISC Series and INDIACom-2015, ICACCI-2015 under IEEE. He is associate editor in International Journal of Convergence Computing (IJConvC) and also an editorial board member of International Journal of Image Mining (IJIM) under Inderscience Publishers. At present he is the guest editors for two special issues floated in International Journal of Rough Sets and Data Analysis (IJRSDA) and International Journal of System Dynamics Applications (IJSDA) under IGI Global publications.

Dr. P. Satish Rama Chowdary is Professor and Vice Principal of Department of Electronics & Communication Engineering at Raghu Institute of Technology, Visakhapatnam. His research interests are computational electromagnetics and antennas and MEMS.

Dr. V.V.S.S. Sameer Chakravarthy is Associate Professor in the Department of Electronics & Communication Engineering at Raghu Institute of Technology, Visakhapatnam. His research interests include computational intelligence, computational electromagnetics and antennas.

Dr. Jaume Anguera is Professor in the Department of Electronics and Telecommunication at Universitat Ramon Llull. He is also an R&D Manager at Fractus, Barcelona, Spain. Dr. Anguera is directing projects in the area of multi-frequency and miniature monopoles; dual-frequency dual-polarized microcell antennas; monoband dual-polarized microstrip patch array; dual-band dual-polarized microstrip patch arrays; network feeding architectures for GSM-UMTS arrays; broadband matching networks; high cross-polarization techniques, array pattern synthesis with genetic algorithms, handset antennas, automotion antennas and antennas for military applications among others. He got the degrees Technical Engineer (Electronic Systems) and Electronic Engineer from Ramon Llull University, Barcelona and degree of Telecommunication Engineer and Ph.D. (Doctor Ing.) from Polytechnic University of Catalunya (UPC), Barcelona. His research interests include miniature, wideband, multiband, and high directivity printed antennas and arrays; fractal-shaped antennas; genetic algorithms; handset antennas: internal and external multiband antennas; base station antennas: multi-band cross-polarized antennas; low cross-polarization and high-isolation techniques for BTS antennas; automotive antennas: integration of antennas; short-range wireless and UWB antennas; and educational methods for electromagnetics. He has got over 50 publications in journals and 100 papers in conference proceedings.

Performance of All-Back-Contact Nanowire Solar Cell with a Nano-Crystalline Silicon Layer

Rakesh K. Patnaik, Devi Prasad Pattnaik and Chayanika Bose

Abstract In this communication, few approaches based on structural modifications of silicon solar cell (SC) are made to improve its performance. With respect to a conventional planar p-n junction type SC, a cylindrical nano wire solar cell (NWSC) is much more efficient in separating and collecting photo-generated carriers. Shifting of front contacts to the rear surface of such structures eliminates optical shadowing effects and can further improve the performance of such NWSCs. By adding a nano-crystalline silicon layer between *p* and *n*-layers of the *p-n* junction, light trapping and hence, the carrier generation rate are enhanced leading to improved efficiency. Thus, an all-back-contact NWSC with embedded nano-crystalline silicon layer performs best and shows up to 30% improvement in efficiency over that in a conventional NWSC. For comparison, all the above structures are simulated using CST Microwave studio, MATLAB, and TCAD tools with tight meshing strategy for generating the optical profile and electrical test run.

Keywords Nano wire solar cell · EWT · MWT · Nano-crystalline

1 Introduction

In order to fulfill the increasing demand of electrical energy in our day-to-day life, we have to depend on renewable energy sources. From the consideration of the crisis of fuels and adverse effects of their uses on our environment, the movement

R.K. Patnaik (✉)
Department of EIE, NIST, Berhampur, Odisha, India
e-mail: rkshpatnaik@gmail.com

D.P. Pattnaik
Department of ECE, GITAM University, Visakhapatnam, India
e-mail: deviprasad.pattnaik@gmail.com

C. Bose
Department of ETCE, Jadavpur University, Kolkata, India
e-mail: chayanikab@yahoo.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_1

towards the green energy is a boon from the sky [1]. Use of solar energy, i.e., solar cell (SC) in different areas from handheld calculators to the satellites has greatly solved the issue of power generation. More efficient conversion of solar energy into electrical energy needs improvements in all stages involved in the process, i.e., it needs better light absorption, quick carrier separation, and efficient collection. In order to enhance light absorption, loss of solar radiation should be minimized first. For this, use of anti-reflective coating (ARC) to reduce reflection loss and textured surface for better absorption are suggested. Minimization of losses related to optical shadowing effect, arising from the front metal contacts, is also required. Efficient separation and collection of photo-generated carriers are possible by suppressing the chances of their recombination [2].

In economical design of a planar solar cell, a thin film of silicon is employed as the substrate material. But such a thin film possesses defects, which may trap the carriers and give rise to recombination losses. Better carrier generation and separation are expected if the structure supports a vertical junction rather than a planar one, and in addition, if carriers be separated within one diffusion length from the junction [3]. In the present communication, we simulate array of silicon SCs of three different configurations: nanowire solar cell (NWSC) with both front and back contacts as a regular one, nanowire solar cell with all-back-contacts (ABC NWSC) and all-back-contacts nanowire solar cell with a nano-crystalline Si layer (NC ABC NWSC), all of which support the above-mentioned features. We also compare their performances to achieve the best result.

2 Design and Simulation

All SC structures are designed using process emulation command. For individual layer, required parameter files are chosen. Meshing strategy is adapted and minimum mesh dimension is considered across interface. The dimension, doping, and other parameters related to simulation of various SC structures are described below.

2.1 Conventional NWSC

The structure of solar cell considered first possesses one dimension much larger than the others, and in addition cylindrical shape. Thus it is called nanowire solar cell (NWSC). Silicon NWs are grown on a 22 μm × 22 μm Si substrate. The inner cylinder, called core or base is of *p*-Si with 1 μm diameter [4, 5]. Its diameter is chosen to be larger than few hundreds of nm in order to absorb higher wavelengths of solar radiation. Next, 1 μm thick *n*-Si layer, called shell or emitter is deposited over the core. Thus a vertical p-n junction is formed along the length of the NW. As up to 100 μm long NWs can be grown by vapor–liquid–solid (VLS) technique maintaining the distinct vertical standing wire structure, length of the NW is chosen

here as 100 μm [6, 7]. Doping level is varied from 10^{16} to 10^{19} per cm^3. An anti-reflective coating is deposited over the top surface. Aluminum and Silver are used as contact materials for *p*- and *n*-layers respectively. The same doping level is used for both the core and emitter to ensure symmetry of the *p*-*n* junction. The cross-sectional view of the NWSC is shown schematically in Fig. 1. Sixteen (16) such single NWs are simulated to form a 4 × 4 array of NWSCs on the Si substrate.

A cylindrical NWSC is expected to perform better compared to a planar solar cell due to many reasons. Long length of NW helps in absorption of all low to high wavelengths of solar radiation. A throughout standing cylindrical *p*-*n* junction facilitates quick separation of the generated carriers within the device (Fig. 1). Within the *p*-*n* junction the collection probability is 1. Diameter of the NW, depending on the doping levels of the *p*-*n* junction, is chosen to be optimally sufficient for the efficient separation and collection of carriers. Finally, dense array of such NWs creates stronger optical confinement, and thereby, gives rise to enhanced carrier generation. Thus with improved performance of such NW structures, the quality of SC material can be compromised resulting in overall cost reduction.

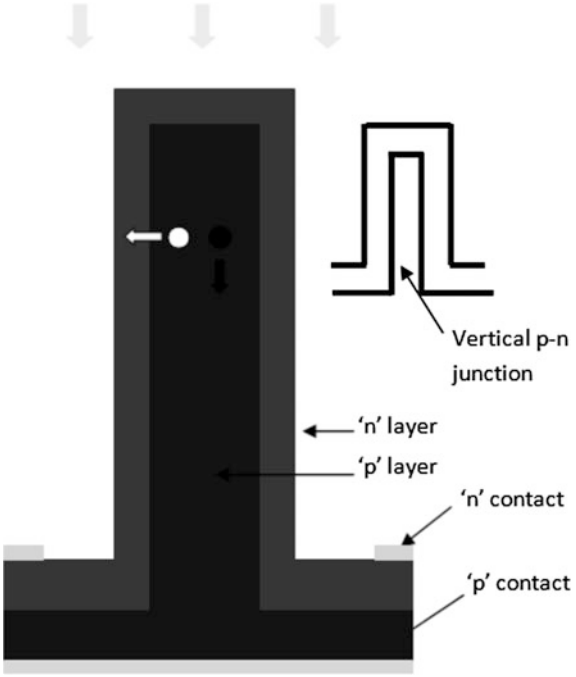


Fig. 1 Cross-sectional view of the NWSC

2.2 All-Back-Contact NWSC

Both front and back metal contacts are used in conventional solar cells. An all-back-contact (ABC) SC is obtained where the front emitter contact is shifted to the back surface of the cell. It offers zero shading loss due to full exposure of the entire front surface, without metal contact fingers, to solar radiation. Front surface can be further improved using textured surface to reduce reflection losses and improve photo-absorption [8, 9]. The front surface carrier recombination occurring at the interface of metal and emitter is also reduced. Three popular configurations of such design are back contact back junction (BC-BJ) [10, 11], metal wrap through (MWT) [10] and emitter wrap through (EWT) [10–13]. Out of these three, EWT offers the best performance. Compared to BC-BJ, wrap-through structures provide quick carrier collection [14, 15], while EWT presents a little more full front active surface than MWT [16–19]. Also, the vertical emitter wrap or fingers offer additional vertical junction. Even the unused substrate areas, where wires are not grown, contribute to areas exposed to radiation.

The 4 × 4 array of regular NWSC structure is altered by removing the front contacts. To shift the front contact to the back surface, 25 holes, each of 0.5 μm diameter, are created from the front to rear surface. Then they are filled with the emitter material (*n*-Si). It is called EWT technique. The structure of a single EWT NWSC is shown in Fig. 2.

Next, 25 contact pads each of dimension 1 μm × 1 μm, are formed at the rear surface, as shown in Fig. 3. One group of contact pads is for the core and another group for the emitter. The latter group effectively replaces the front contacts. The structure now has all contacts on rear surface and the entire front surface gets fully illuminated. Thus a 4 × 4 array of ABC NWSC is designed.

2.3 All-Back-Contact NWSC with Nano-Crystalline Silicon Layer

The term nano-crystalline silicon (NC-Si) refers to a range of materials around the transition region from amorphous to microcrystalline phase in a silicon thin film. It has small grains of crystalline silicon within the amorphous phase and possesses many important properties. NC-Si shows increased absorption in the red and infrared wavelengths, which makes it a useful material in the field of optoelectronics, specifically in amorphous Si solar cells [20, 21]. In addition, a properly grown NC-Si can have higher electron mobility, due to the presence of the Si crystallites. It also offers increased stability over amorphous Si and can be deposited using conventional low temperature amorphous Si deposition techniques, viz. PECVD, as opposed to laser annealing or high temperature CVD processes, in case of polycrystalline Si.

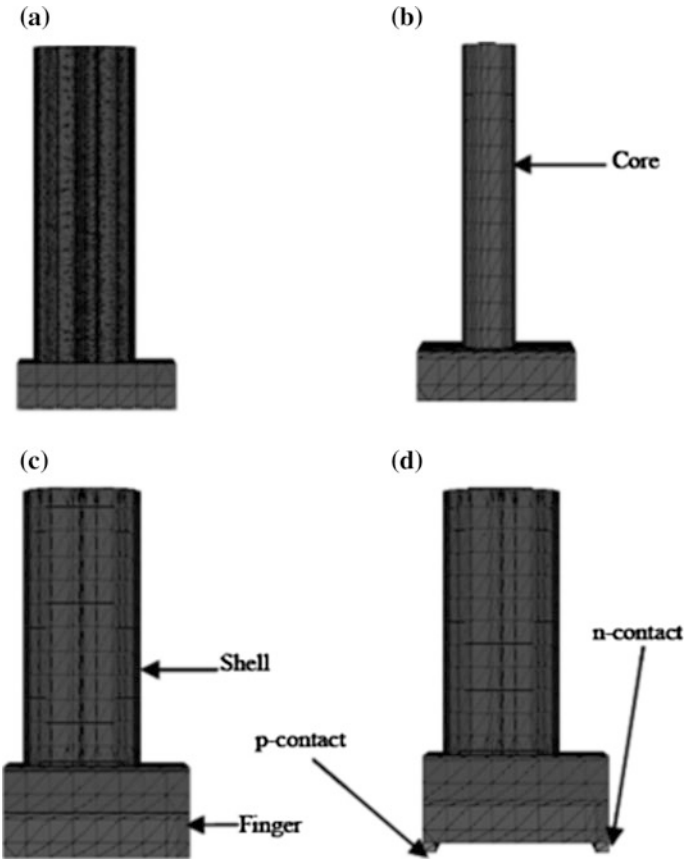


Fig. 2 Structure of a single EWT NWSC **a** with tight meshing, **b** p-type Si core, **c** core is covered by a n-type Si shell, it is connected to rear contact by a n-type extension, **d** both 'p' and 'n' contacts

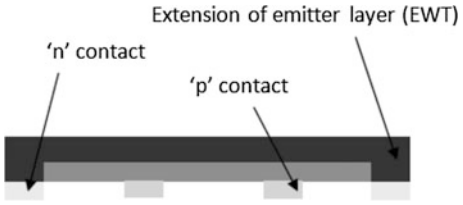


Fig. 3 Structure of EWT NWSC (only lower base part is shown)

Researchers, therefore, propose use of such NC-Si layer as an intrinsic layer within a conventional structure of a photovoltaic cell or a *p-i-n* photo detector [22]. An appropriate layer of NC-Si introduced in a solar cell, acts as a low Q, loss less omni-directional reflector, and thereby, offers better optical confinement or light trapping. It creates multiple orders of resonance at higher wavelengths like red and

infrared. In addition, the presence of small grains (in the range of nano-meter) in NC-Si layer increases the difference between energy levels, and the lifetime and drift mobility of majority carriers [23]. On the other hand, the mobility of minority carrier decreases due to the presence of recombination center within the layer. Thus, an optimally thin NC-Si layer is to be used, so that it can accommodate one minority carrier diffusion length and collect carriers efficiently.

In the array of ABC NWSC structure described earlier, a 1 μm thick NC-Si layer is introduced between the core and shell layers of each NWSC. All the three SC structures are simulated using CST studio, TCAD tool and MATLAB. For solar spectrum, AM 1.5g file is used. Optical profiles are created using CST tool and Ray tracer function of TCAD tool. The Si parameter file is modified to realize NC structure, by updating complex refractive index data, dependence of resonance on size of the grain and layer thickness, and dependence of mobility, band gap, and density of states on temperature. From the available literature, trap densities are also added in NC-Si parameter file. To have the optical profile of only the NC layer, spectrometric commands are used by scanning every individual wavelength of AM1.5g file. After retrieving the optical profile as a log file, it is next applied on the whole structure along with AM1.5g file. Thus, we obtain the final optical profile, which categorizes the higher wavelengths in terms of reflection and absorption. Electrical simulation is next carried out by solving the Poisson's equation and the Continuity equation with bias voltage increased in steps. A tight meshing strategy is adapted throughout the structure and recombination models are considered at surface, bulk, and at interfaces.

3 Performance Evaluations

In order to compare the performance of three NWSC structures discussed above, diameter and length of the core, and thickness of the shell are chosen same in all cases. The corresponding doping levels are also taken same, and varied over a range of 10^{16} and 10^{19} cm^{-3}. As described in earlier section, after design of all the three structures, optical simulation is done. Electrical simulation is then applied on the output result of optical profile. A bias voltage is ramped up to 1 V. Then the output file is called in graph study tool and codes written in '.tcl' commands.

Thus, we finally evaluate performances of the SC structures described above, where the first structure is an array 16 nanowires with front and rear contacts; in the second structure both contacts are placed on the rear side, and in the third one a NC-Si layer is embedded between *p*- and *n*-layers of each cell in the array. The optical profile and resonance peaks are considered simultaneously with solar radiation AM1.5 g spectrums. As evident from Fig. 4, the structure with NC-Si layer provides greater absorption for higher wavelengths. Such better photon harvesting is supported by strong optical confinement due to the formation of

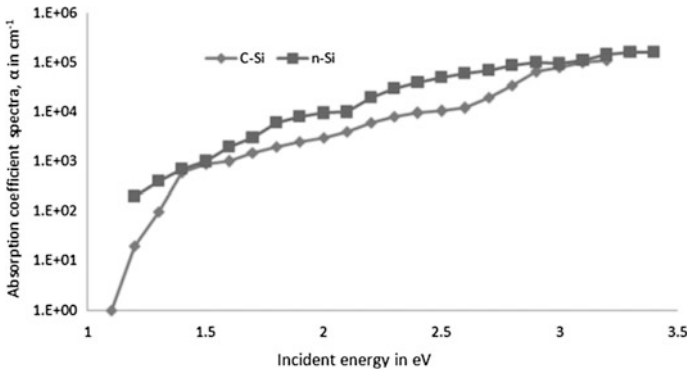


Fig. 4 Variation of absorption coefficient with incident solar radiation

whispering gallery mode (WGM) in the SC with NC-Si layer. Again, as described earlier, thickness of the NC layer is kept quite thin to suppress degradation of minority carrier mobility due to recombination centers present in the layer. A NC-Si layer thus makes efficient carrier collection feasible.

To determine the role of the NC-Si layer in a NWSC, three parameters—Open circuit voltage (V_{OC}), Short circuit current density (J_{SC}) and Conversion efficiency (η) are investigated. Variations of these three key factors are studied with varying doping concentration.

3.1 Open Circuit Voltage (V_{OC})

Figure 5 presents the variations in V_{OC} with change in doping level of the SCs. As a vertical cylindrical *p-n* junction structure offers a larger surface area than a planar junction structure, greater surface recombination loss occurs, which limits the minimum value of V_{OC} around 0.4 V in case of a regular NWSC. In an ABC NWSC, exposure of front surface to incident radiation causes improvement in V_{OC} because of zero shading loss. The V_{OC} is a function of photocurrent and attains higher value for higher doping concentration (Fig. 5). In the NC ABC NWSC, the thin NC layer behaves somehow like an amorphous structure. We know that amorphous structure offers less dark current, and inside the nano-crystal region the mobility of minority carrier decreases. These features help to enhance V_{OC} with growing thickness of NC layer. In the proposed NC ABC NWSC structure, thickness of the NC layer is taken as 1 μm, and the highest value of V_{OC} obtained is 0.54 V for a doping level of 10^{19} cm^{-3}.

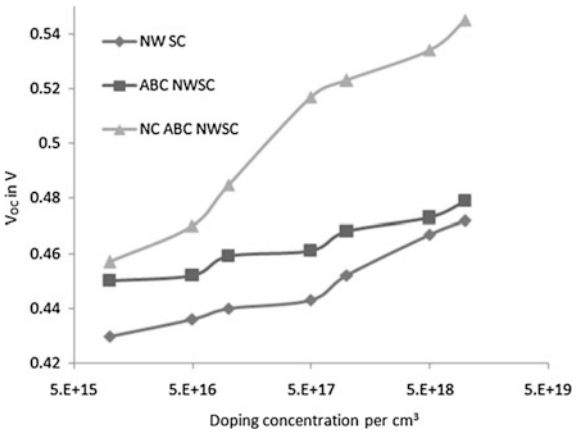


Fig. 5 Variation of open circuit voltage (V_{oc}) with doping level of emitter

3.2 Short Circuit Current Density (J_{SC})

All the three cylindrical NW structures, by virtue of the vertical *p-n* junction, are more efficient in separating photo-generated carriers as compared to a planar solar cell. Figure 6 indicates that for all types of NWSC structures considered here, the J_{SC} increases with increase in doping level. An increase in doping concentration generates more carriers, and in those SC structures the recombination losses are compensated by quick separation of carriers, thus showing rise in J_{SC} with increase in doping. In addition, the EWT technique employed and the vertical nature of the junction make the carrier collection much more efficient. With respect to the conventional NWSC, an ABC NWSC performs better because of entire front surface illumination. In the proposed NC ABC NWSC structure, absorption coefficient is high enough due to photon trapping in the NC layer, and J_{SC} undergoes a huge improvement.

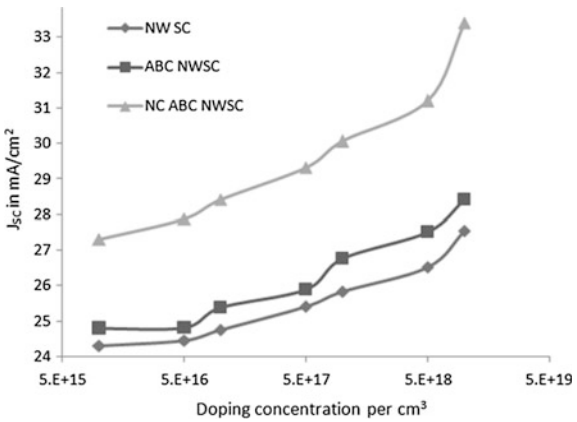


Fig. 6 Variation of short circuit current density (J_{SC}) with doping level of emitter

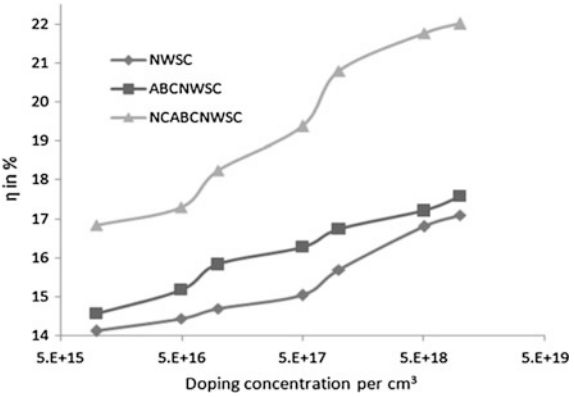


Fig. 7 Variation of conversion efficiency (η) with doping level of emitter

Table 1 Solar cell parameters for different SC configurations with *Si* doping of 10^{19} cm^{-3}

Parameter	Regular NWSC	ABC NWSC	NC ABC NWSC
V_{OC} in V	0.472	0.479	0.545
J_{SC} in mA/cm^2	27.56	28.42	33.40
η in %	17.1	17.57	22.01

3.3 Conversion Efficiency (η)

Conversion efficiency, η is the prime key factor to judge the overall performance of any type of photovoltaic device. It is seen that from the point of view of V_{OC} and J_{SC}, NC ABC NWSC performs best. The fact is also evident from Fig. 7 that exhibits variations of conversion efficiency of different SC structures as a function of core and emitter doping.

The key parameters for a NC ABC NWSC are tabulated (Table 1) to compare quantitatively its performance with respect to other similar SC structures without the NC-*Si* layer.

It is clear from above investigations that NC ABC NWSC is the best structure compared to an ABC NWSC and regular NWSC. It carries several merits because of modified device geometry and morphological changes. First of all, the vertical *p-n* junction supports quick separation of photo-generated carriers, all-back contacts avoid shading loss and NC layer helps in improving light trapping.

4 Conclusion

In this paper, a NC silicon layer is incorporated in an ABC NWSC. Shift of front contacts of regular NWSC to the rear surface, leading to ABC NWSC structure, improves its performance to some extent. Introduction of an appropriately thin

NC-Si layer in the ABC NWSC structure leads to enormous improvement in the key solar parameters. For a specific core and emitter doping, incorporation of a 1 μm thick NC layer causes 13.8%, 18% and 25% (approximately) improvements in V_{OC}, J_{SC} and η respectively, with respect to the ABC NWSC structure. Similar improvements with respect to the regular NWSC with front contacts are obviously greater, and obtained as 15.5%, 22% and 30% respectively. The proposed structure of ABC NWSC with a NC-*Si* layer thus offers a feasible approach to realize high-performance NW *Si* solar cells for practical applications.

References

1. Hocine, D., Belkaid, M. S., Pasquinelli, M., Escoubas, L., Torchio, P. Moreau, A.: Characterization of TiO_2 antireflection coatings elaborated by APCVD for monocrystalline silicon solar cells. Phys. Status Solidi C, 12 323–326. doi:10.1002/pssc.201400085, (2015).
2. Lehr, D.; Helgert, M., Sundermann, M, Morhard, C., Pacholski, C., Patz, J. P.; Brunneret R. Opt. Express 18 pp 23878–23890, (2010)
3. Du, Q. G., Kam, C. H, Demir, H. V, Yu, H. Y., Sun, X. W.: Opt. Lett. 36 pp 1884–1886 (2011)
4. Dai, W. T., Yap, D., Chen, G.: Opt. Express 20 A519–A529, (2012)
5. Basore, P. A. In Conference record of the 22nd IEEE Photovoltaic Specialist Conference, Las Vegas, USA, pp 299–302, (1991)
6. Ali, K., Khan, S. A., Mat Jafri, M. Z.: Sol. Energy, 101 (0) (2014).
7. Wright, D. N., Marstein, E.S., Holt, A.: Double Layer Anti-Reflective Coatings For Silicon Solar Cells, 0-7803-8707-4/05/2005 IEEE, (2015)
8. Kesmez, Ö., Çamurlu, H.E., Burunkaya, E., Arpaç, E.: Ceram. Int. 36 (1) (2010) 391, (2010)
9. Hocine, D., Belkaid, M. S., Pasquinelli, M., Escoubas, L., Simon, J. J., Rivière, G. A., Moussi, A.: Mater. Sci. Semicond. Process., 16 (1) (2013) 113. (2013)
10. Lee, B. G., Skarp, J., Malinen, V., Shuo, L., Sukgeun, C., Branz, H. M.: presented at the Photovoltaic Specialists Conference (PVSC) 2012 38th IEEE, (2012)
11. Ahmed, N., Singh, C. B., Bhattacharya, S., Dhara, S., Bhargav, P. B.: Conference Papers in Energy 2013 4 (2013)
12. Yang, C.H., Lien, S.Y., Chu, C.H., Kung, C.Y., Cheng, T.F., Chen, P.T: Int. J. Photoenergy 2013 1, (2013)
13. Perez-Sanchez, G. F., de la Luz Perez, M., Morales-Acevedo, A.: presented at the Electrical and Electronics Engineering, 2005 2nd International Conference on, (2005)
14. Schiller, S., Beister, G., Sieber, W., Schirmer, G., Hacker, E.: Thin Solid Films 83 (2) (1981) 239
15. Morales-Acevedo, A., Luna-Arredondo, E., Santana, G.: presented at the Photovoltaic Specialists Conference, 2002. Conference Record of the Twenty-Ninth IEEE, 2002
16. Lee, B. G., Skarp, J., Malinen, V., Shuo, L., Sukgeun, C., Branz, H. M.: presented at the Photovoltaic Specialists Conference (PVSC) 2012 38th IEEE, (2012)
17. Kayes, B. M., Atwater, H. A., Lewis, N. S.: Comparison of Device Physics Principles of Planar and Radial p-n Junction Nanorods Solar Cells, Journal of Applied Physics, vol. 97, pp. 114302-1–114302-11, (May 2005)
18. Gunawan, O., Guha, S.: Characteristics of Vapor-Liquid-Solid Grown Silicon Nanowire Solar cells, Elsevier Solar Energy Materials & Solar cells, vol. 93, pp. 1388–1393, (2009)
19. Patnaik, R.K., Pattnaik, D., Choudhury, R.: Efficiency Comparison of MWT and EWT all Backcontact Nanowire Silicon Solar Cells, LNEE 372, Springer India 2016 DOI 10.1007/978-81-322-2728-1_37, 411–420, (2016)

20. Kuo, C.Y., Gau, C., Dai, B.T.: Photovoltaic Characteristics of Silicon Nanowire Arrays Synthesized By Vapor-Liquid-Solid Process, Elsevier Solar Energy Materials & Solar cell, vol. 95, pp. 154–157, January 2011)
21. Synopsys (2012), Sentauraus TCAD user manual, (2012)
22. Mohamed, M., El-Sayed, EL-ZAIAT, Samy, F., Youseff, G., Reda, A.: Enhancing silicon solar cell efficiency with double layer antireflection coating, Turk J Phys 40: 30, (2016)
23. Wang, E.Y., Yu, F.T.S., Sims, V.L., Brandhorst, E.W., Broder, J.D.; Optimum Design of Anti-reflection coating for silicon solar cells. 10th IEEE Photovoltaic Specialists Conference. pp: 168–171, (1973)

Miniaturized Textile Antenna Using Electromagnetic Band Gap (EBG) Structure

M. Ramesh, V. Rajya Lakshmi and P. Mallikarjuna Rao

Abstract A textile antenna is a crucial component for any wireless body-centric communication. It is used to establish body-to-body or on-body communications. The proposed textile antenna is created using circular patch and staircase slots. The textile antenna without Electromagnetic band gap (EBG) structure operates at 8.9 GHz frequency and a combination of EBG structure with vias operate at 2.03 GHz frequency. The textile antenna is miniaturized using EBG structure with four vias.

Keywords Textile antenna · EBG · Patch antenna

1 Introduction

Over the last decade, the response for wearable electronic devices has been increased tremendously. Wireless communication inside wearable devices brings new level of mobility and flexibility. As a result, textile antennas are extensively used in wireless body area networks in order to communicate with each wearable devices. Wearable antennas are used for diverse applications, such as real-time monitoring of health conditions of aged people residing in remote locations, tracking of children; observe the glucose levels of athletes during practice, WLAN and for Fitness applications [1]. Conventional textile antenna is a combination of three layers: ground, substrate, and patch. The ground and patch are conducting

M. Ramesh (✉)
Department of ECE, GITAM University, Visakhapatnam, India
e-mail: manikonda433@gmail.com

V. Rajya Lakshmi
Department of ECE, ANITS, Visakhapatnam, India
e-mail: rajyalakshmivalluri@gmail.com

P. Mallikarjuna Rao
Department of ECE, Andhra University, Visakhapatnam, India
e-mail: pmraoauece@yahoo.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_2

materials and for the substrate dielectric materials are used [2]. In textile antennas, ground and patch are the conductive fabrics like zelt and substrate is a nonconductive fabric like felt, jeans, dacron. Commercial textile materials are cheaper, possess low dielectric constant, and also comfortable to wear [3].

In conventional textile antennas, the resonant frequency decreases with the increasing size of the antenna. This size is relatively larger in modern portable wearable devices. Miniaturization of microstrip antennas are complicated in antenna design and it affects radiating performance too [4]. So, few tactics have been available to miniaturize the patch antenna size such as using, patch antenna is λ/10 miniaturized using reactive impedance substrate, its substrate is made using Trans-Tech MCT-25 magnesium calcium titanate composition [5]. In [6], the antenna is positioned on teflon substrate, inter-digital capacitor provides negative permittivity, CSRR provides negative permeability, its combinations provides Metamaterial behavior and finally achieved significant miniaturization. In [7], using split-ring resonators and two FR-4 substrates, resonant frequency shifts from 6.6 GHz to 4.67 GHz and the antenna is miniaturized by 29.3%. In [8], using PBG Structure 75% size reduction is obtained. By loading of antenna with shorting vias [9, 10]. Using of high dielectric constant substrates and superstrates [11, 12]. In this paper, uniplanar EBG structure has been proposed as it is less sensitive to incident angle and polarization and it makes fabrication easier. The proposed antenna is useful for third-generation wireless Universal Mobile Telecommunications System (UMTS). In Sect. 2, antenna design parameters, analysis of antenna, and EBG structure are presented. Section 3 deals with Results and Discussion. Finally, conclusions are given in Sect. 4.

2 Antenna Design and Analysis

2.1 Antenna Without EBG

The dimensions of the proposed textile antenna with staircase slots and the side view of the textile antenna are shown in Fig. 1. Here, Fig. 1a represents the front view of circular patch with feed line and Fig. 1b exhibits side view of textile antenna without EBG. The order of the layers is ground, substrate, and patch respectively.

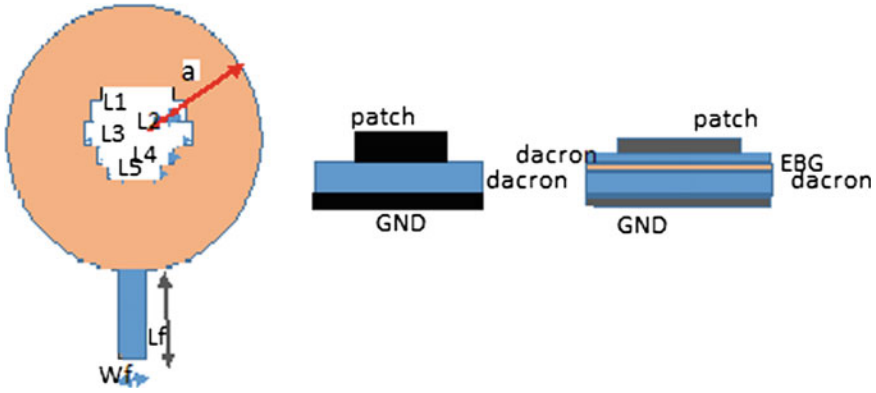
The resonant frequency of circular patch textile antenna is calculated using dominant mode as [2]

$$f_r = \frac{1.84 * C}{2\pi a_e \sqrt{\in_r}} \tag{1}$$

Here fringing is considered, f_r is the resonant frequency, a_e is the effective radius of patch, ε_r is the relative permittivity, h is height of substrate, a is the actual radius, and c is the speed of light in free space.

$$a_e = a\left\{1 + \frac{2h}{\pi a \varepsilon_r}\left[\ln\left(\frac{\pi a}{2h}\right) + 1.7726\right]\right\}^{1/2} \quad (2)$$

The circular patch with staircase slot textile antenna without EBG is shown in Fig. 2.



(a) Top view (b) Side view without EBG (c) Side view with EBG

Fig. 1 Geometry of textile antenna

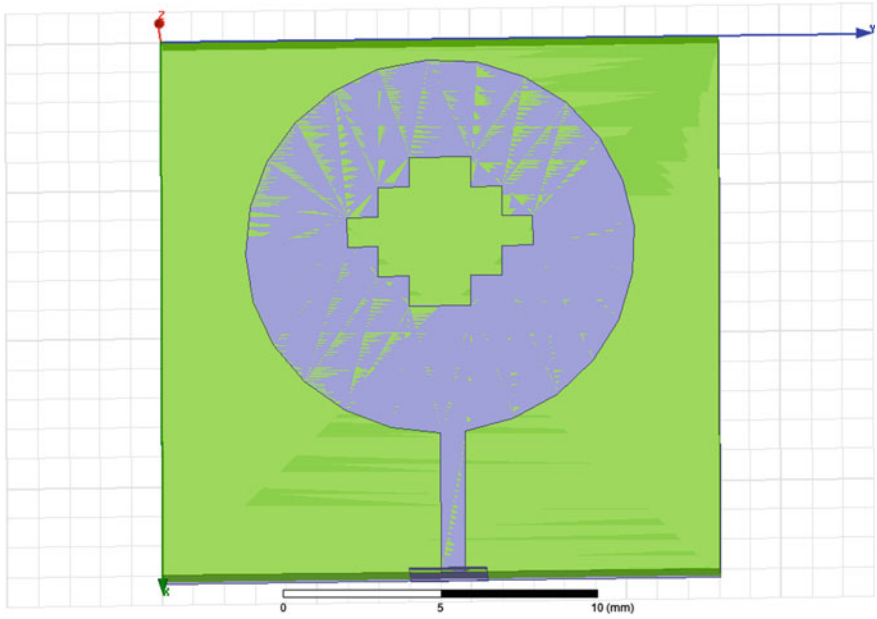


Fig. 2 Proposed textile antenna without EBG

The size of the full ground is 18 mm × 18 mm. In this case, dacron fabric is used as a substrate with dielectric constant ε_r is 3 and loss tangent is 0.025 [13, 14]. It absorbs less water when compared with other textile materials and possess high resistance to wrinkle. The size of the substrate is 18 mm × 18 mm with a thickness of 1.5 mm. The shape of the patch is circular with five slots. The radius of the circular patch, a = 6.1 mm. The length of the slots are L1 = 2 mm, L2 = 4 mm, L3 = 6 mm, L4 = 4 mm and L5 = 2 mm, respectively and the width is 1 mm.

2.2 *Antenna with EBG Structure*

The band gap structure methodology is proposed here to miniaturize the textile antenna size. Here uniplanar EBG structure is used. It is a periodic EBG structure. EBG materials are naturally unavailable. The size of a unit cell is 5 mm × 5 mm square shape with two slots. The overall antenna consists of five layers such as ground, substrate1, EBG structure, substrate2, and circular patch respectively, shown in Fig. 1c. Dacron fabric is used for Substrate1 and substrate2. Here, the same dimensions are used for circular patch except for the ground and substrate.

The circular patch having staircase slots textile antenna with EBG and vias are shown in Fig. 3. The antenna has full ground and its size is 32 mm by 32 mm. The first substrate is dacron fabric, its dimensions are 32 mm × 32 mm and thickness

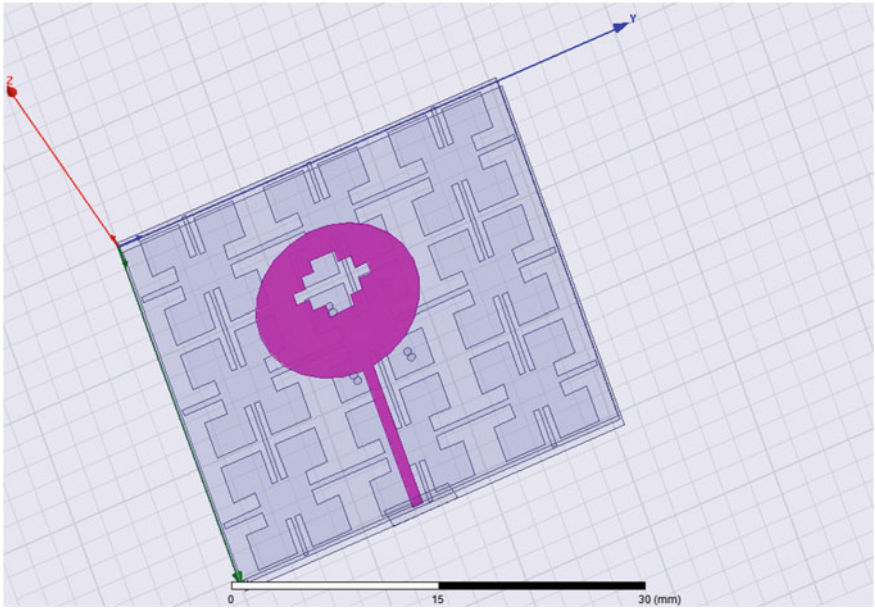


Fig. 3 Proposed textile antenna with EBG

is 1 mm. The next layer consists of uniplanar EBG structure in which 6 × 6 unit cells are used. On top of this EBG structure another substrate, dacron fabric is used having dielectric constant $\varepsilon_r = 3$, loss tangent is 0.025 and its thickness is 0.5 mm from EBG structure to patch. Its size is 32 mm × 32 mm. The next layer consists of a circular patch with staircase slot. Here four vias are used with equal radius of 0.4 mm and height of 1 mm. The vias are arranged between ground and EBG structure. Here, simple feeding technique known as microstrip line feed is used having the length L_f as 5.17 mm and width W_f as 2.5 mm. Finally the distance between ground and patch is 1.5 mm. The antenna is integrated with EBG unit cells.

3 Results

The proposed textile antenna and EBG unit cell are simulated using Ansoft HFSS software.

Figure 4 represents the simulated graph of frequency verses return loss (s11) of circular patch with staircase slot textile antenna without EBG. The simulated return loss −22.8 dB at a resonant frequency of 8.9 GHz and impedance bandwidth of 700 MHz, varying within a range (Return Loss is less than −10 dB is Reference Line) of 8.5–9.2 GHz.

The simulated return loss of the proposed textile antenna with vias and EBG structure is shown in Fig. 5. The circular patch with staircase slot textile antenna achieves resonance at 2.03 GHz frequency with return loss of −15.02 dB. Thus the antenna size is reduced by [8]

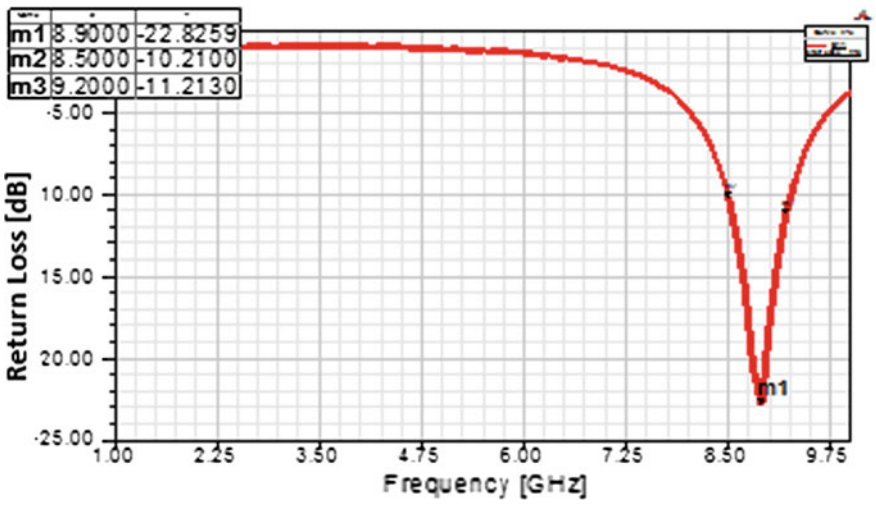


Fig. 4 Return loss of proposed textile antenna without EBG

$$\frac{8.9-2.03}{8.9}\times 100 = 77.19\%. \tag{3}$$

The simulated 3D polar plot of proposed textile antenna with EBG is shown in Fig. 6. It has a directivity of 2.16 dB at a resonant frequency of 2.03 GHz.

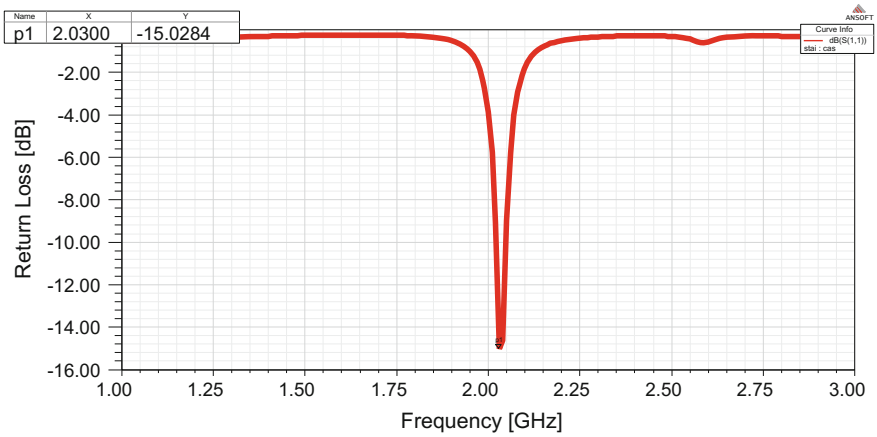


Fig. 5 Return loss of proposed textile antenna with EBG

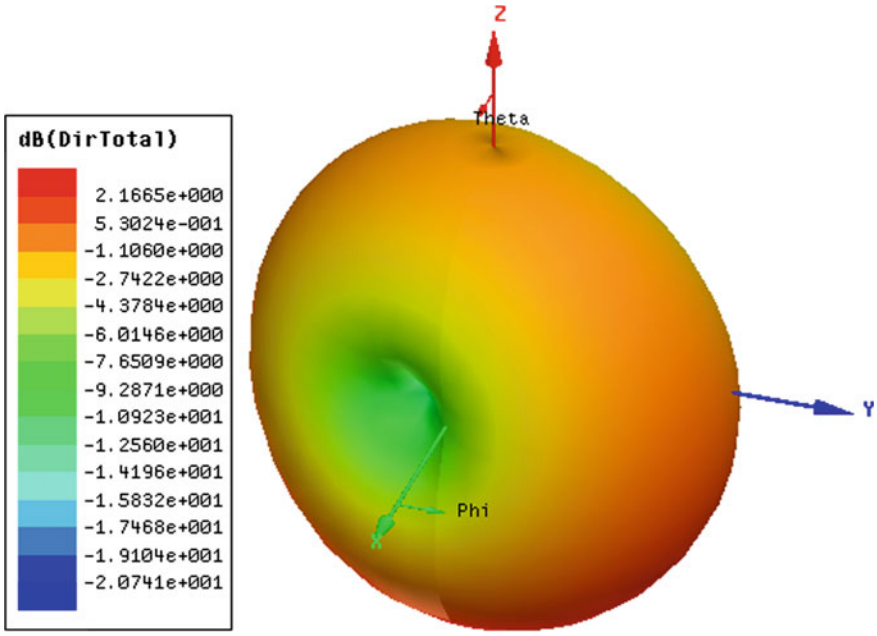


Fig. 6 3D Radiation pattern of proposed antenna

The simulated VSWR of textile antenna without EBG structure is shown in Fig. 7. The VSWR value (less than 2) is 1.15 at a resonant frequency 8.9 GHz. Figure 8 represents simulated VSWR of proposed textile antenna with EBG. The VSWR value is 1.57 at a resonant frequency of 2.04 GHz.

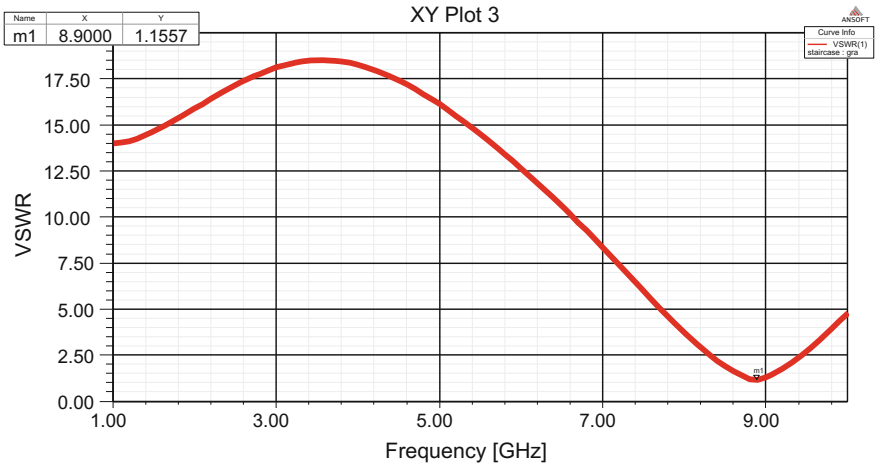


Fig. 7 The VSWR of proposed textile antenna

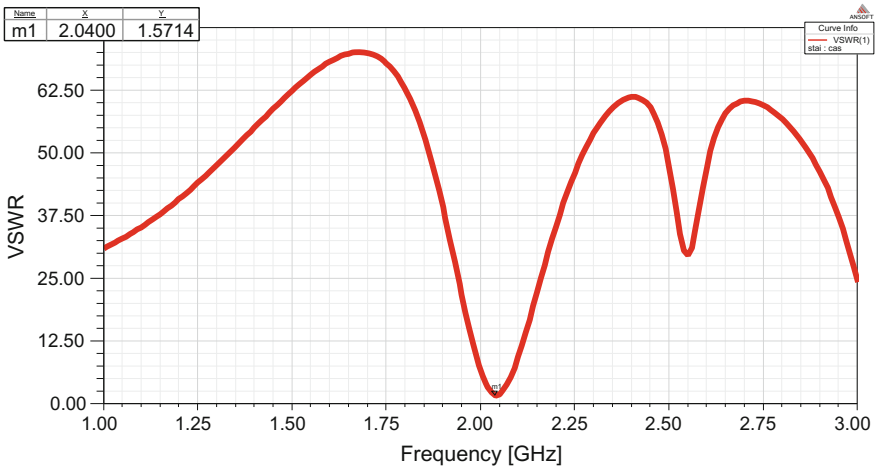


Fig. 8 The VSWR of proposed textile antenna with EBG

4 Conclusion

The resonant frequency of the proposed circular shape patch with staircase slot textile antenna using uniplanar EBG is shifted from 8.9 to 2.03 GHz without change in the size of circular patch and slots. The proposed antenna has a return loss of −15.6 dB at a resonant frequency of 2.03 GHz. The size of the antenna is reduced by 77.19% dacron fabric is used as a substrate for the proposed textile antenna.

References

1. Peter, S. Hall., Yang, Hao.: Antennas and Propagation for Body-centric Wireless Communications. Artech House Publishers (2012).
2. Garg, R., Bhartia, P., Bahl, I., Ittipiboon, A.: Microstrip antenna design handbook. Artech House: London, (2001).
3. Salvado, R., Loss, C., Gonçalves, R., Pinho, P.: Textile Materials for the Design of Wearable Antennas: A Survey. Sensors (Basel, Switzerland), pp. 15841–15857 (2012).
4. John, Volakis., Chi.-Chih, Chen., Kyohei, Fujimoto.: Small Antennas: Miniaturization Techniques and Applications. Text Book, McGraw Hill Professional, Dec (2009).
5. Mosallaei, H., Sarabandi, K.: Antenna Miniaturization and Bandwidth Enhancement Using a Reactive Impedance Substrate. IEEE Trans. Antennas Propag. Vol. 2, pp. 2403–2414 (2004).
6. Indrasen, Singh. Sanjeev, Jain. Vijay, Shanker, Tripathi. Sudarshan, Tiwari.: Micro strip Patch Antenna Miniaturization Using Planar Metamaterial Unit Cell. Quality, Reliability, Security and Robustness in Heterogeneous Networks, pp. 358–364 (2013).
7. Xing, Zhao., Youngki Lee., Jaehoon, Choi.: Design of a compact patch antenna using split-ring resonator embedded substrate. Microwave and Optical Technology Letters 53 (12) December (2011).
8. Abdelnasser, A., Eldek.: A miniaturized patch antenna at 2.4 GHZ using Uni-planar compact photonic band gap structure. Microwave and Optical Technology Letters 50(5), pp. 1360–1363, May (2008).
9. Porath, R.: Theory of miniaturized shorting-post Microstrip antennas. IEEE Transactions, Antennas and Propagation, Vol. 48, No. 1, pp. 41–47 (2000).
10. Kan, H.K., Waterhouse, H.B.: Size reduction technique for shorted patches. IEEE, Electronics Letters, Vol. 35, pp. 948–949 (1999).
11. Lo, T.K., Ho, C.O., Hwang, Y., Lam, E.K.W., B. Lee, B.: Miniature aperture-coupled Microstrip antenna of very high permittivity: Electronics Letters, Vol. 33, pp. 9–10 (1997).
12. Kumar, P., Dwevidi, V. K., Singh, G., Bhooshan, S.: Miniaturization of gap-coupled Microstrip antennas. In. Proceedings, International Conference on Recent Advances in Microwave and Applications (Microwave-08), India, pp. 489–491 (2008).
13. Shuvashis, Dey. Nandita, Saha. Akram Alomainy.: Design and Performance Analysis of Narrow Band Textile Antenna for Three Different Substrate Permittivity Materials and Bending Consequence. In. Loughborough Antennas and Propagation Conference, pp. 1–5, Loughborough, U.K, November (2011).
14. Kawshik, Shikder. Farhadur.: Design and Evaluation of a UWB Wearable Textile Antenna for Body Area Network. In. IEEE, Proceeding of International Conference on Electrical Information and Communication Technology (EICT2015), pp. 326–330 (2015).

A Hybrid Methodology for Multi-owner Information Sharing in Untrusted Cloud Using Secure Mona Convention

Banda S.N.V. Ramanamurthy and D. Sirisha

Abstract Sharing social event asset among cloud clients is a significant impact, so appropriated figuring gives a preservationist and convincing course of action. In perspective of proceeds with change of sharing information, interest in a multi-proprietor way to an untrusted cloud is still a testing issue. Here in this paper, we propose a safe multi-proprietor information sharing arrangement, for dynamic group in the cloud. By giving social affair mark and component show encryption methods, any cloud clients can protectively confer information to others. By then a meanwhile, the limit overhead and encryption count cost of the arrangement are free with the amount of denied clients. In other hand, we explore the security of this arrangement with intensive confirmations. OTP (One-Time Password) is one of the least complex and most prevalent types of confirmation that can be utilized for securing access to accounts. OTP is regularly alluded to as a safe and more grounded types of confirmation, and tolerating them to introduce over different machines. We give a numerous levels of security to share information among multi-proprietor process. Initially the client chooses the pre-chosen picture to login. At that point chooses a picture from the matrix of pictures. By utilizing this, the OTP is produced consequently and sent to comparing email account.

Keywords Security · Broadcast message · Encryption · Cloud computing

1 Introduction

Distributed computing imagines exceedingly accessible, on-interest system access to a common pool of configurable figuring assets [1–3]. Clients can appreciate adaptable capacity limit and calculation ability without paying consideration on the development and support of these bases. While distributed computing acquires promising open doors, it likewise brings along new security and protection issues,

B.S.N.V. Ramanamurthy (✉) · D. Sirisha
Department of CSE, Pragati Engineering College, Surampalem, India
e-mail: ramanamurthy.b@pragati.ac.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_3

which thwart the general population to embrace the cloud advancements. The information in travel or put away in distributed storage could be tempered by unapproved people or even the distributed storage supplier [4–6]. Various encryption methods are accessible to ensure the security of Cloud information and administrations [7–9]. Be that as it may, as these encryption methods bring along new procedures, additional complexities must be conceived to oversee encoded information safely and productively.

For an individual distributed storage client, he/she stores his/her information and recovers part of the put away information later. Be that as it may, for big business clients, the put away information ought to be shared among gathering individuals. One sort of encryption plan called quality-based encryption (ABE) could be utilized to apply fine-grained access control over the mutual information [10–15]. Furthermore, the elements of gathering individuals and relating put away information ought to be considered to build a plausible fine-grained access control for the undertaking [16–18].

Moreover, given the aggregate sum of information created and put away in the cloud, getting to information through route is tedious and annoying. Getting to cloud information through (watchword) hunt is thought to be commonsense and in unnecessary. Nonetheless, as the cloud information are secured through cryptographic methods, which acquire high expenses when recovering through seeking. Searchable encryption was acquainted with empower clients to shroud the searchable watchwords (of a record) by encryption [19–24]. Later, clients could produce proper tokens/trapdoors for particular watchwords to recover the encoded information containing these catchphrases. The clients looking capacity is additionally shared under fine-grain arrangements [25–28] One client can produce searchable records for a document and indicate a subset of clients who can use these searchable files. Clients outside the predefined bunch cannot look out this record. In any case, progression of gathering individuals and searchable records ought to be considered to yield a down to earth and vigorous searchable encryption [29, 30].

In this paper, we propose one novel distributed storage development empowering the administration of element searchable information for gathering coordinated effort. We make utilization of quality-based encryption plan (ABE) and open key encryption with conjunctive catchphrase look (PECK) to outline our convention. We show that our plan remarkably incorporates crucial usefulness for big business clients, to be specific, the fine-grained access control for the searchable file and the substance of the information. Besides, we give security investigation and behavior broad execution assessment to demonstrate the achievability of our configuration for big business clients. The paper is structured as follows. Related background is described in Sect. 2. While targeted system models and two cryptographic building blocks are presented in Sect. 3. Our novel construction is detailed in Sect. 4. Then the security and performance analysis are shown in Sect. 5. Finally, our contributions are reiterated and future direction is mentioned to conclude this paper.

2 Encryption

2.1 Attribute-Based Encryption

Property-based Encryption (ABE) gives a fine-grained access control of shared information. ABE was begun from the work by Sahai and Waters [10]. Later, two tracks of ABE have been produced: figure content strategy ABE (CP-ABE) [13, 15] and key-approach ABE (KP-ABE) [12, 14]. In the CP-ABE plan, the client is conceded characteristic keys (connected with qualities), and the entrance arrangement could be authorized on the figure content. At that point the client possesses the property keys fulfilling the predetermined access arrangement, the client could unscramble the message. An opposite setting is called KP-ABE, which indicates decoding approach on the property keys and the figure content is labeled with an arrangement of traits.

Be that as it may, to send in handy applications, overseeing dynamic access approach is required to bolster steadily changing access bunch. At that point, the property keys ought to be reissued and figure content be re-scrambled to consent to the present access control arrangement. In other hand, client repudiation ought to be done in a productive approach to control the harms. Some ABE proposed that the close time is added with the property when producing related trait keys [13, 17]. In any case, the exchange between the granularity of "window of powerlessness" and the weight to upgrade the property keys ought to be considered. Boldyreva et al. [16] proposed an effective renouncement plan for IBE and KP-ABE, while Yu et al. [18] proposed an ABE plan with quality denial. They coordinated the intermediary re-encryption (PRE) with ABE, and empowered the power to appoint the greater part of the work for key redesign of the client to intermediary servers. Since part based access control (PBAC) is regularly used to confining framework access to approved clients. CP-ABE, which is firmly identified with RBAC, is picked as a building piece of our plan for big business application situation.

2.2 Searchable Encryption

Searchable encryption empowers clients to conceal the searchable catchphrases (of a record) by encryption. Later, clients could create suitable tokens/trapdoors for particular catchphrases to recover the encoded information containing these watchwords. Senegal [19] initially presented the idea of looking on encoded information and gave down to earth arrangements. Goh [20] then formalized the idea of security for this issue and built a more proficient plan utilizing Bloom channel. Taking after that, some examination [22, 23] was led to either enhance the proficiency or give more grounded security of searchable encryption. One shared characteristic of these works is that they all bolstered just single watchword inquiry in the symmetric key setting.

The idea of conjunctive catchphrase looks in symmetric key setting was initially presented by Galle et al. [25]. They gave a security idea to conjunctive catchphrase look over scrambled information and developed a more productive plan contrasted and the one inconsequentially reached out from single watchword hunt plan. Later, Ballard et al. [26] enhanced by shortening the trapdoor size and diminishing calculation/stockpiling overhead. Be that as it may, because of the symmetric key setting, these plans just empower one client to store and recover his/her own private information. Sharing of file building and looking capacity cannot be accomplished effortlessly.

Boneh et al. [21] initially tended to one sort of down to earth applications called email directing framework. The searchable file of a mail can be produced by utilizing the beneficiary's open key. The beneficiary can recover specific messages from the steering server by appointing related trapdoors. The relating messages can be gathered. What's more, Boneh et al. proposed another application brought seeking over review log, where the organization can designate particular trapdoor to the examiner to assess just review related records. Be that as it may, these plans upheld just single catchphrase inquiry. There are different applications requiring more expressive hunt over conceivable watchwords.

To improve look expressions, Park et al. [27] proposed open key encryption with conjunctive catchphrase look (PECK). Boneh et al. further gave a plan supporting the conjunction of subset and reach inquiries on figure content information. At that point their development utilized the bilinear gathering of composite way, which yields less effective development. Furthermore, they considered just single-client setting, where sharing of searchable list is difficult to accomplish. Hwan et al. [28] gave one productive PECK and considered a conceivable expansion to multiclient settings [29, 30]. In this paper, we will advance consider the sharing of searchable list ought to be given to empower bunch coordinated effort (Fig. 1).

Fig. 1 Enterprise cloud storage access model

3 Security and Performance

In this area, we show the security and execution of our convention. In this showing, just approved gathering individuals can (1) look/recover the gathering information and (2) unscramble the recovered gathering information put away in cloud stockpiles. The representative who leaves the gathering or is disavowed cannot recover or decode the put away information in cloud stockpiles. Besides, we assess the calculation and correspondence costs for the CSC in our outline and finish up our configuration is successful and productive for the venture clients to share information and team up as a gathering.

3.1 Security Analysis

The security of our convention depends on the fundamental ABEar [18] and muPECK [28]. From one viewpoint, the ABEar is turned out to be semantically secure under particular id picked plaintext assault (IND-s ID-CPA) accepting decisional bilinear Diffie–Hellman (DBDH) is hard. Taking into account these formal contentions, we can presume that the unapproved element (either CSC or CSP) cannot fashion searchable records and searchable trapdoors since these activities are included in taking care of the difficult issue.

Then again, the muPECK is turned out to be semantically securing under multiclient figure content from arbitrary against picked watchword assaults (IND-mCR-CKA) expecting choice direct Daffier–Hellman (DLDH) is hard. In this manner, the unapproved substance cannot compute characteristic keys for unscrambling, either in light of the fact that these activities are included in taking care of the DLDH difficult issue.

Concerning information flow, the information is re-scrambled to the same figure content space. The recreated key is likewise circulated consistently in the key space. Any foe cannot increase any more preferences since he/she needs to manage the same difficult issues as the ones before information/key upgrade. What's more, the client flow is taken care of by including/evacuating one a player in searchable file of that client and issuing/redesigning the quality keys of that gathering. The mystery of the information encoded under indicated access approach can be ensured when bunch individuals join or leave, while the entrance control of inquiry ability of gathering individuals can be guaranteed.

One approved client, while Update SI relies on upon 2 Hashand 1 increases in G1 for the incorporation/rejection of one single searchable list. If you do not mind allude to Table 1 with respect to correspondence cost, the CSC needs to start a solicitation for Grp Store, Retrieve, Update AK, Update CT, Update AU, and Update SI. At that point the CSC gets the reaction from the CSP. One and only round of correspondence is required.

Table 1 Computation cost of the CSC

Operation	Required basic operation
GrpStore	$(n + m' + 2l + 2)$ $SclrMul_{G1}$, $(l - 1)$ Add_{G1}, $2l$ *HashToPoint*
Retrieve	3 $SclrMul_{G1}$, $(2m' - 1)$ Add_{G1}
GrpDecrypt	$(m + 1)$ *Pairing*, m Mul_{G2}
UpdateAU	1 Exp_{G2}
UpdateSI	1 Add_{G1}, 2 *HashToPoint*

Table 2 Experimental benchmark

Basic operation	Operation description	Time
Mul_{G2}	*multiplication in* G_2	1 μs
Add_{G1}	*addition in* G_1	9 μs
Exp_{G2}	*exponentiation in* G_2	0.22 ms
Pairing	*bilinear pairing*	1.79 ms
$SclrMul_{G1}$	*scaler multiplication in* G_1	2.24 ms
HashToPoint	*hash to element in* G_1	5 ms

The trial benchmark is directed utilizing neighborhood server with Intel Xeon processor E5620 at 2. 40 GHz running Ubuntu 11.10. We utilize GNU numerous accuracy number juggling library (GMP) and blending-based cryptography library (PBC) libraries. We select one super solitary bend over one base field of size 512 bits and the implanting degree is 2. In this way the security level is set to be ECC-160 bits. The measure of one gathering component in G1 is 1024 bits. The expense of one expansion in G1 costs 9 μs, while one increase in G1 requires 2. 24 ms. One increase in G2 requires 1 μs, while one exponentiation in G2 costs 0. 22 ms. At last, the bilinear matching needs 1. 79 ms, and hash to G1 component expends 5. 00 ms (shown in Table 2).

4 Proposed System

Secure situations ensure their assets against unapproved access by upholding access control components. So the quickly expanding security is an issue content-based passwords are insufficient to counter such issues. At that point the requirement for something more secure alongside being easy to use is required. At that point this is the place Image-Based Authentication (IBA) becomes an integral factor. This takes out storm assault, shoulder assault. Utilizing the texting administration accessible in web, client will acquire the OTP after picture checking. At that point this OTP then can be utilized by client to get to their own records. The picture construct verification strategy depends in light of the client's capacity to perceive pre-picked classifications from a matrix of pictures. In this paper I incorporates image-based validation and one-time watchword to accomplish abnormal state of security in verifying the client over the web (Fig. 2).

Fig. 2 System architecture

The fundamental Objective of 3 Level Security framework is a one of a kind and an exclusive investigation of utilizing pictures as secret key and execution of a to a great degree secured framework, distinguishing 3 levels of security.

Level 1: Security at level 1 has been forced by basic content-based secret word.
Level 2: Security at this level has been forced by utilizing picture-based validation (IBA) which wipes out shoulder assault, whirlwind assault. Client needs to choose three pictures from that point sportive lattice.
Level 3: After the viable elbowroom of the above two levels, the Level 3 Security System will then deliver a one-time numeric mystery word that would be true blue just for that login session. The check customer will be instructed of this one-time mystery word on his email id.

5 Conclusion

In this paper, we propose a novel distributed storage development empowering the administration of searchable element information for gathering cooperation. Our commitments are abridged in the accompanying three noteworthy components of our convention: (1) expressly tending to big business application situation of cloud stockpiles as far as framework design and usefulness. (2) A novel access-control plan for the endeavor clients to share the dynamic information and work together as a gathering, and (3) A practical configuration as far as the venture client's stock-piling, calculation and correspondence while (2) is accomplished. For the future work, we might want to facilitate incorporate other vital functionalities for the undertaking, for example, open examining and secure cloud information calcula-tion, to empower completely fledged distributed storage for future venture applications.

References

1. P. Mell and T. Grance, "The nist definition of cloud computing (draft) recommendations of the national institute of standards and technology," Nist Special Publication, vol. 145, no. 6, p. 7, (2011).
2. M. Armbrust, A. Fox, R. Griffith, A. D. Joseph, R. H. Katz, A. Konwinski, G. Lee, D. A. Patterson, A. Rabkin, and M. Zaharia, "Above the clouds: A berkeley view of cloud computing," EECS Department, University of California, Berkeley, Tech. Rep., (Feb 2009).
3. R. Buyya, C. S. Yeo, S. Venugopal, J. Broberg, and I. Brandic, "Cloud computing and emerging it platforms: Vision, hype, and reality for delivering computing as the 5th utility," Future Generation Computer Systems, vol. 25, no. 6, pp. 599–616, (2009).
4. Nist, "Fips pub 197: Announcing the advanced encryption standard (aes)," NIST, (2001).
5. J. Jonsson and B. Kaliski, "Public-Key Cryptography Standards (PKCS) #1: RSA Cryptography Specifications Version 2.1," no. 3, (February 2003) [On line]. Available: http://www.ietf.org/rfc/rfc3447.
6. D. Boneh and M. Franklin, "Identity-based encryption from the Weil pairing," SIAM J. of Computing, vol. 32, no. 3, pp. 586–615, 2003, extended abstract in Crypto'01.
7. N. Virvilis, S. Dritsas, and D. Gritzalis, "Secure cloud storage: Available infrastructures and architectures review and evaluation," in Trust, Privacy and Security in Digital Business, ser. Lecture Notes in Computer Science, S. Furnell, C. Lambrinoudakis, and G. Pernul, Eds. Springer, 2011, vol. 6863, pp. 74–85. (2011).
8. K. Yang and X. Jia, "Data storage auditing service in cloud computing: challenges, methods and opportunities," World Wide Web, vol. 15, no. 4, pp. 409–428, (2012).
9. M. Armbrust, A. Fox, R. Griffith, A. D. Joseph, R. Katz, A. Konwinski, G. Lee, D. Patterson, A. Rabkin, I. Stoica, and M. Zaharia, "A view of cloud computing," Commun. ACM, vol. 53, pp. 50–58, (Apr. 2010).
10. A. Sahai and B. Waters, "Fuzzy identity-based encryption," in Advances in Cryptology - EUROCRYPT 2005, ser. Lecture Notes in Computer Science, R. Cramer, Ed. Springer, 2005, vol. 3494, pp. 557–557. (2005).
11. M. Pirretti, P. Traynor, P. McDaniel, and B. Waters, "Secure attribute-based systems," in Proceedings of the 13th ACM conference on Computer and communications security, ser. CCS '06. New York, NY, USA: ACM, 2006, pp. 99–112. (2006).
12. V. Goyal, O. Pandey, A. Sahai, and B. Waters, "Attribute-based encryption for fine-grained access control of encrypted data," in Proceedings of the 13th ACM conference on Computer and communications security, ser. CCS '06. New York, NY, USA: ACM, pp. 89–98. (2006).
13. J. Bethencourt, A. Sahai, and B. Waters, "Ciphertext-policy attribute-based encryption," in Proceedings of the 2007 IEEE Symposium on Security and Privacy, ser. SP '07. Washington, DC, USA: IEEE Computer Society, pp. 321–334. (2007).
14. R. Ostrovsky, A. Sahai, and B. Waters, "Attribute-based encryption with non-monotonic access structures," in Proceedings of the 14th ACM conference on Computer and communications security, ser. CCS '07. New York, NY, USA: ACM, 2007, pp. 195–203.
15. B. Waters, "Ciphertext-policy attribute-based encryption: An expressive, efficient, and provably secure realization," in Public Key Cryptography - PKC 2011, ser. Lecture Notes in Computer Science, D. Catalano, N. Fazio, R. Gennaro, and A. Nicolosi, Eds. Springer, 2011, vol. 6571, pp. 53–70.
16. A. Boldyreva, V. Goyal, and V. Kumar, "Identity-based encryption with efficient revocation," in Proceedings of the 15th ACM conference on Computer and communications security, ser. CCS '08. New York, NY, USA: ACM, 2008, pp. 417–426. [Online]. Available: http://doi.acm.org/10.1145/1455770.1455823.
17. R. Bobba, H. Khurana, and M. Prabhakaran, "Attribute-sets: A practically motivated enhancement to attribute-based encryption," in Computer Security – ESORICS 2009, ser. Lecture Notes in Computer Science, M. Backes and P. Ning, Eds. Springer, 2009, vol. 5789, pp. 587–604.

18. S. Yu, C. Wang, K. Ren, and W. Lou, "Attribute based data sharing with attribute revocation," in Proceedings of the 5th ACM Symposium on Information, Computer and Communications Security, ser. ASIACCS '10. New York, NY, USA: ACM, 2010, pp. 261–270. [Online]. Available: http://doi.acm.org/10.1145/1755688.1755720.
19. D. X. Song, D. Wagner, and A. Perrig, "Practical techniques for searches on encrypted data," in Security and Privacy, 2000. S P 2000. Proceedings. 2000 IEEE Symposium on, 2000, pp. 44 –55.
20. E.-J. Goh, "Secure indexes," IACR Cryptology ePrint Archive, vol. 2003, p. 216, 2003.
21. D. Boneh, G. Di Crescenzo, R. Ostrovsky, and G. Persiano, "Public key encryption with keyword search," in Advances in Cryptology - EUROCRYPT 2004, ser. Lecture Notes in Computer Science, C. Cachin and J. Camenisch, Eds. Springer, 2004, vol. 3027, pp. 506–522.
22. M. Abdalla, M. Bellare, D. Catalano, E. Kiltz, T. Kohno, T. Lange, J. Malone-Lee, G. Neven, P. Paillier, and H. Shi, "Searchable encryption revisited: Consistency properties, relation to anonymous ibe, and extensions," in Advances in Cryptology - CRYPTO 2005, ser. Lecture Notes in Computer Science, V. Shoup, Ed. Springer, 2005, vol. 3621, pp. 205–222.
23. R. Curtmola, J. Garay, S. Kamara, and R. Ostrovsky, "Searchable symmetric encryption: improved definitions and efficient constructions," in Proceedings of the 13th ACM conference on Computer and communications security, ser. CCS '06. New York, NY, USA: ACM,2006, pp. 79–88.
24. M. Bellare, A. Boldyreva, and A. O'neill, "Deterministic and efficiently searchable encryption," in Advances in Cryptology - CRYPTO2007, ser. Lecture Notes in Computer Science, A. Menezes, Ed. Springer, 2007, vol. 4622, pp. 535–552.
25. P. Golle, J. Staddon, and B. Waters, "Secure conjunctive keyword search over encrypted data," in Applied Cryptography and Network Security, ser. Lecture Notes in Computer Science, M. Jakobsson, M. Yung, and J. Zhou, Eds. Springer, 2004, vol. 3089, pp. 31–45.
26. L. Ballard, S. Kamara, and F. Monrose, "Achieving efficient conjunctive keyword searches over encrypted data," in Information and Communications Security, ser. Lecture Notes in Computer Science, S. Qing, W. Mao, J. López, and G. Wang, Eds. Springer, 2005, vol. 3783, pp. 414–426.
27. D. Park, K. Kim, and P. Lee, "Public key encryption with conjunctive field keyword search," in Information Security Applications, ser. Lecture Notes in Computer Science, C. Lim and M. Yung, Eds. Springer, 2005, vol. 3325, pp. 73–86.
28. Y. Hwang and P. Lee, "Public key encryption with conjunctive keyword search and its extension to a multi-user system," in Pairing-Based Cryptography – Pairing 2007, ser. Lecture Notes in Computer Science, T. Takagi, T. Okamoto, E. Okamoto, and T. Okamoto, Eds. Springer, 2007, vol. 4575, pp. 2–22.
29. Y. Yang, H. Lu, and J. Weng, "Multi-user private keyword search for cloud computing," in Cloud Computing Technology and Science (CloudCom), 2011 IEEE Third International Conference on, 29 2011-Dec. 1 2011, pp. 264–271.
30. M. Li, S. Yu, N. Cao, and W. Lou, "Authorized private keyword search over encrypted data in cloud computing," in Distributed Computing Systems (ICDCS), 2011 31st International Conference on, June 2011, pp. 383–392.

Selfie Continuous Sign Language Recognition with Neural Network Classifier

G. Anantha Rao, P.V.V. Kishore, A.S.C.S. Sastry, D. Anil Kumar and E. Kiran Kumar

Abstract This works objective is to bring sign language closer to real-time implementation on mobile platforms with a video database of Indian sign language created with a mobile front camera in selfie mode. Pre-filtering, segmentation, and feature extraction on video frames creates a sign language feature space. Artificial Neural Network classifier on the sign feature space are trained with feed forward nets and tested. ASUS smart phone with 5M pixel front camera captures continuous sign videos containing an average of 220 frames for 18 single-handed signs at a frame rate of 30 fps. Sobel edge operator's power is enhanced with morphology and adaptive thresholding giving a near perfect segmentation of hand and head portions. Word matching score (WMS) gives the performance of the proposed method with an average WMS of around 90% for ANN with an execution time of 0.5221 s during classification. Fully novel method of implementing sign language to introduce sign language recognition systems on smart phones for making it a real-time usage application.

Keywords Indian sign language · Sobel adaptive threshold · Morphological differencing · Artificial neural networks · Word matching score

G. Anantha Rao (✉) · P.V.V. Kishore · A.S.C.S. Sastry · D. Anil Kumar · E. Kiran Kumar
Department of Electronics and Communication Engineering, K L University, Guntur, India
e-mail: ananth.gondu@gmail.com

P.V.V. Kishore
e-mail: pvvkishore@kluniversity.in

A.S.C.S. Sastry
e-mail: ascssastry@kluniversity.in

D. Anil Kumar
e-mail: danilmurali@kluniversity.in

E. Kiran Kumar
e-mail: kiraneepuri@kluniversity.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_4

1 Introduction

Sign language is a computer vision-based intact intricate language that engages signs shaped by hand moments in amalgamation with facial expressions and hand shapes. Sign language is a natural language for communication among people with low or no hearing sense. Human speech capture in digital format generates a 1D signal for processing whereas human sign language generates 2D signals from image or video data. Classification of gestures can be identified as both static and dynamic. Static gestures involve time-invariant finger orientations, whereas dynamic gestures support a time-varying hand orientations and head positions. The proposed Selfie video model for sign language recognition is a computer vision-based approach and does not employ motion or colored gloves for gesture recognition.

We introduce a novel sign language recognition system, called selfie sign language recognition system capturing signs using a smartphone front camera. The signer holds the selfie stick in one hand and signs with his other hand.

In the past, researchers attempted this type of work on sign images and videos but the novelty of our method lies in capturing selfie sign videos.

In [1], Mohamed proposed a vision-based recognizer to automatically classify Arabic sign language. A set of statistical moments for feature extraction and support vector machines for classification provided an average recognition rate of 87%. Omar [2] proposed a neuro-fuzzy system that deals with images of simple hand signs and succeeded a recognition rate of 90.55%.

Kishore, proposed [3] 4-Camera model. The segmented hand gestures with extracted shapes created a feature matrix described by elliptical Fourier descriptors which are classified with back propagation algorithm trained artificial neural network. The normal recognition rate in the proposed 4-Camera model for sign language recognition is about 92.23%.

2 Pre-processing, Segmentation, Feature Extraction, and Classification

The flowchart of the proposed SLR is shown in Fig. 1. The picture under the first block shows the capture mechanism followed in this work for video capture. Acquired video is in mp4 format having full HD (1920 × 1080) video recording on a 5M pixel CMOS front camera. Let this 2D video be represented as a 2D frame. For video the frame changes with time, which is fixed universally at 30 frames per second. These videos form the database of this work. A threefold 2D Gaussian filter with zero mean ($m = 0$) and three variances in the range 0.1–0.5 smoothens each frame by removing sharp variations during capture.

The smoothed frames in real space $\mathbb{R}$ are treated with a new type of multidimensional Sobel mask. From literature the Sobel edge operator is a 2D gradient

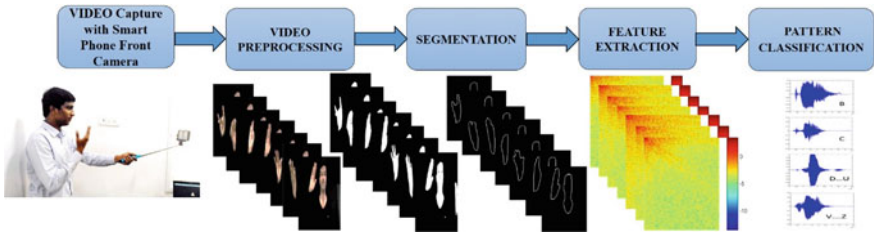


Fig. 1 Flow chart of SLR system with smart phone front camera video capture

operator. Gradients provide information related to changes in the data along with the direction of maximum change. For 2D gradient calculation, two 1D gradients in x and y directions of the frame matrix are computed as follows:

$$g^x = \sum_{k=1}^{N} \mathfrak{F}(x-k, y)g(k) \tag{1}$$

$$g^y = \sum_{k=1}^{N} \mathfrak{F}(x, y-k)g^T(k) \tag{2}$$

where $g \rightarrow [+1, -1]$ is the discrete gradient operator. The gradient magnitude G^{xy} gives magnitude of edge strength in Sobel edge detector computed as $G^{xy} = \sqrt{(g^x)^2 + (g^y)^2}$. The Sobel masks S^{Mx} and S^{My} are sensitive to lighting variations, motion blur, and camera vibrations which are commonly a cause of concern for sign video acquisition under selfie mode. A suitable threshold at the end will extract the final binary hand and head portions. Edge adaptive thresholding is considered with block variational mean on each 3 × 3 Sobel mask is used as threshold. The final binary image is

$$B^x = \sum_{x=1}^{N} \sqrt{(S^{Mx} \otimes \mathfrak{F}^x)^2 + (S^{My} \otimes \mathfrak{F}^y)^2} \geq \sum_{i=1}^{b} \sum_{x=1}^{N} \sqrt{(S^{Mx} \otimes \mathfrak{F}^x)^2 + (S^{My} \otimes \mathfrak{F}^y)^2} \tag{3}$$

where b is the block size and B^x is binary video frame or segmented video frame. S^{Mx} and S^{My} are Sobel masks in x- and y-direction. Figure 2 shows the difference in block thresholding and global thresholding (used 0.2) which failed to handle motion blur.

Sign language is defined by hand shapes. Hand shapes are defined by precise contours that form around the edges of the hand in the video frame. A hand contour $H^C(x) \rightarrow C(B^x)$ in spatial domain is a simple differential morphological gradient on the binary image B^x. The connected component analysis separates head and hand contours. Morphological gradient is defined by line masks in horizontal M_{3H} and vertical M_{3V} directions having length 3. Contour extraction is represented as

$$H^C(x) = \left\{ z | \left(\hat{M}_{3H} \right)_z \cap B^x \neq \varnothing \right\} - \left\{ z | \left(\hat{M}_{3H} \right)_z \subseteq B^x \right\} \tag{4}$$

$$H^C(y) = \left\{ z | \left(\hat{M}_{3V} \right)_z \cap B^x \neq \varnothing \right\} - \left\{ z | \left(\hat{M}_{3V} \right)_z \subseteq B^x \right\} \tag{5}$$

$$H^C(x, y) = H^C(x) \oplus H^C(y) \tag{6}$$

where $H^C(x)$ is hand contour in x-direction and $H^C(y)$ in y-direction. Hand and head contours are separated by finding the connected components with maximum number of pixels with a 4 neighborhood operation to from a contour image $H^C(x, y)$.

Features are unique representation of objects in this world. Feature is a set of measured quantities in a 1D space represented as $F^V(x) = \{ f(x) | x \subseteq \mathbb{R} \}$, where $f(x)$ can be any transformation or optimization model on vector x. Here $f(x)$ is considered as Discrete Cosine Transform (DCT) along with Principle Component Analysis (PCA). Figure 3 shows a color-coded representation of hand DCT features F^V_{uv} for the frame in a video sequence. The head does not change much in any of the

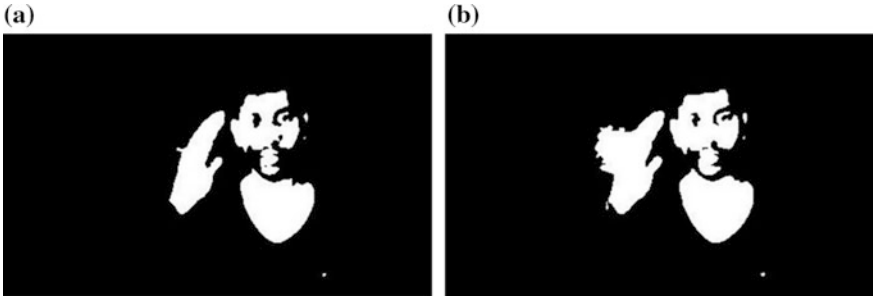


Fig. 2 **a** Block variational mean thresholded frame. **b** Global threshold of 0.2 for Sobel

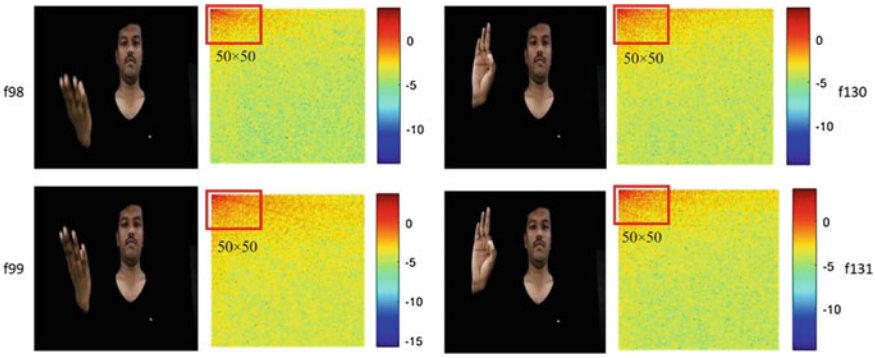


Fig. 3 2D DCT representation of hand classification

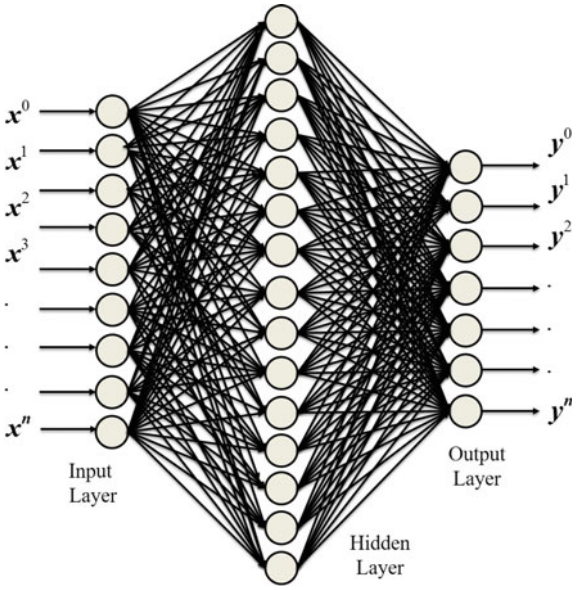


Fig. 4 Neural network model used for sign contour energy representations

frames captured and hence head contour DCT remains fairly constant throughout the video sequence.

The first 50 × 50 matrix of values possess maximum amount of energy in a frame. The boxed region in Fig. 4 is the 50 × 50 feature matrix. This matrix of 50 × 50 is reshaped to from a 1 × 2500 feature vector. But for every frame, a 2500 value feature vector for frame will cost program execution time. PCA treatment of the matrix F_{uv}^{V}, retains only the unique components of the matrix F_{uv}^{V}. The final feature vector F_{uv}^{V} is represented as F_{fn}^{V}, where *fn* gives frame number. PCA reduces the feature vector per frame to from 50 × 50 sample values per frame. Each 50 sample Eigen vector from PCA uniquely represents DCT energy of the hand shape in each frame.

The details of ANN with backpropagation algorithm are listed in our previous work at [4] and the models used for coding are considered form [5].

The model of artificial neural network is presented in Fig. 4. A 3-layered feedforward network of neurons is simulated with F_{fn}^{V} features as input to first layer. Then number of neurons in input layer is estimated from the samples obtained from PCA treated DCT energy matrix. The numbers of output neurons are equal to number of signs to be recognized by the network. Hidden layer neurons are estimated through trial and error method, and an optimum no. of neurons are selected to achieve accuracy at higher execution speech. For this sign classification, the estimated neurons are twice the neurons in the input layer for correct classification at reasonably less simulation times.

3 Results and Analysis

The front camera video recording of sign language gestures with smart phones Asus Zen phone II and Samsung Galaxy S4 at the end of selfie stick are used in experiment. Both the mobiles are equipped with 5M pixel front camera. Sign video capturing is constrained in a controlled environment with room lighting and simple background. The first photo in Fig. 1 demonstrates the procedure followed by signers for video capture. The discussion on results is presented in two sections: quantitative and qualitative. Quantitative analysis provides visual outcomes of the work and qualitative analysis relates to various constraints on the algorithm and how are these constraints are handled.

3.1 Visual Analysis

Each video sequence is having a meaningful sentence. The following sentence "Hai Good Morning, I am P R I D H U, Have A Nice Day, Bye Thank You" is used for training and testing. There are 18 words in the sentence. The words in the training video are sequenced in the above order but the testing video contains same words in different order.

Classification of the words is tested with Euclidian, Normalized Euclidian, and Mahalanobis distance functions from our previous work on this video sequence. Filtering and adaptive thresholding with Sobel gradient produces regions of signer's hands and head segments. Morphological differential gradient with respect to line structuring element as in Eqs. 4–6 refines the edges of hands and head portions. Figure 5 shows the results of the segmentation process on a few frames. Row (a) has original RGB captured video frames. Row (b) has Gaussian-filtered, Sobel-gradiented and region-filled outputs of the frames in row (a). The last row contains morphological subtracted outputs of the frames in row (b).

The energy of the hand and head contours gives features for sign classification. 2D DCT calculates energy of the hand and head contours. DCT uses orthogonal basis functions that represent the signal energy with minimum number of frequency domain samples that can effectively use to represent the entire hand and head curvatures. As shown in Fig. 3, first 50 × 50 samples of the DCT matrix were extracted. These 2500 samples out of 65,536 samples are enough to reproduce the original contour using inverse DCT. This hypothesis is tested for each frame and a decision was made to consider only 2500 samples for sign representation.

With 50 × 50 feature matrix per frame and an average number of frames per video at 220 frames, the feature matrix for the considered 18 signs is a stack of 50 × 50 × 220 matrix. Initiating the classifier with a multidimensional feature matrix of this size takes longer execution periods. Hence, PCA treats each frame of size 50 × 50 energy features by computing Eigen vectors and retaining the principle components to from a 50 × 1 vector per frame. The training vector contains

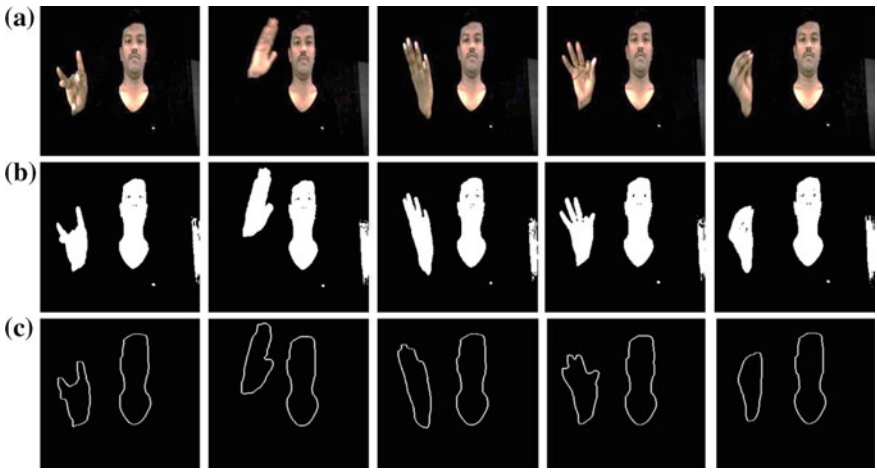


Fig. 5 **a** Few frames in RGB format. **b** Their region segments with Gaussian filtering and Sobel operation. **c** Contours of hands and head produced with morphological subtraction with line structuring elements

only a few head sample values for such 'No Sign' detection. Euclidian distance, Normalized Euclidian distance, and Mahalanobis distance classifies the feature matrix as individual signs. The next section analyses the classifiers performance based on word matching score (WMS). And proposes to use ANN to trade accuracy over speed.

3.2 Classifiers Performance: Word Matching Score (WMS)

Word matching score gives the ratio of correct classification to total number of samples used for classification. The expression for WMS is $M^{S\%} = \frac{Correct\ Classifications}{Total\ Signs\ in\ a\ Video} \times 100$. Feature matrix has a size of 50 × 220, each row representing a frame in the video sequence. To test the uniqueness of the feature matrix for a particular sign or no sign, energy density variations of the 50 samples for first 150 frames is computed.

Exclusive testing with three distance measure on a sign video having 18 signs consisting of 220 frames provides an insight into the best distance measure for sign features. Table 1 gives details of the metric $M^{S\%}$ for three distance measures. The average classification rate with same training feature for testing individual frames is around 90.58% with Mahalanobis distance. The low scores recorded by Euclidian distance (74.11%) and normalized Euclidian Distance (71.76%) compared to Mahalanobis is due to the inter class variance considerations in Mahalanobis. Test repetition frequency is 10 per sign. To further improve performance of the classifier the distance classifier is replaced by artificial neural network. The input layer has 50

Table 1 The performance of three minimum distance classifiers with different testing videos

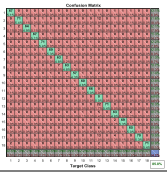
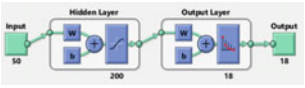
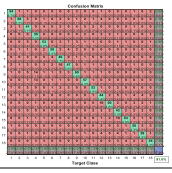
Signs	Euclidian distance classifer	Normalized Euclidian distance	Mahalanobis distance classifier
HAI	70	60	80
GOOD	60	60	80
MORNING	70	70	80
I AM	50	40	80
P	80	80	90
R	80	80	100
I	80	80	100
D	80	80	100
H	80	80	90
U	80	80	90
HAVE	40	40	80
A	60	80	90
NICE	50	40	80
DAY	60	60	80
BYE	40	40	80
THANK	40	40	80
YOU	50	40	80
Average WMS	62.94	61.76	85.88

neurons that feed the hidden layer with 100 neurons are assigned in the output layer represent each sign.

For training 2 sets of videos at the same time with a total of 524 frames from continuous sign sequence of two different signers were chosen for testing with same set with 78 hidden neurons has resulted in a WMS of 80.5%. Putting more number of hidden neurons will further increase the WMS, but reduces speed of execution and they are optimized for this set at 78. In the next phase of experimentation 789 frames trained the ANN and from that 3 sets, 2 sets are tested, i.e. 524 frames. The number of hidden neurons was 125 and we found an increase in WMS at 85.5%. Similarly results for experimentation 3 are shown at the last row of Table 2. The WMS significantly improved for higher sample training with a compromise in speed. Hidden neurons were 200 in the last testing phase.

The average recognition rate was 90% for the total classification method which is on par with other researchers for American Sign Language [6] and Chinese Sign Language [7]. To standardize the entire algorithm, the number of hidden neurons are taken as 100 and testing is carried out with all other values being constant from previous testing's. Minimum Distance Classifier (MDC) with Mahalanobis distance produces a 85.5% WMS at 0.4823 s for a data set with 1313 frames. The ANN-based classifier with same parameters produced a 90% WMS at 0.5452 s.

Table 2 Details of training and testing sign videos under simple backgrounds with different samples and their recognition rates

Training samples	Testing samples	Network architecture	Output confusion matrix	WMS (%)
18 Signs 789 (2 Sets) frames	18 Signs (3 Sets) 524 frames			85.5
18 signs (5 Sets) 1313 frames	18 signs (3 Sets) 789 frames			91.0

ANN's in the recent years have become faster and can be considered for smart phone based sign language recognition system design.

4 Conclusion

A novel idea of putting sign language into smart phones is simulated and tested in this work. Sign video capture using selfie stick is being introduced for the first time in the history of computerized sign language recognition systems. A formal database of 18 signs in continuous sign language were recorded with 10 different signers. Hand and head contour energies are features for classification computed from discrete cosine transform. Execution speeds are improved by extracting principle components with principle component analysis. Euclidian, normalized Euclidian, and Mahalanobis distance metrics classify sign features. Mahalanobis distance reached an average word matching score of around 90.58% consistently when compared to the other two distance measures for the same train and test sets. Mahalanobis distance uses inter class variance to compute distance which is required in sign language recognition due to the fact that no two signers in this world will not perform same sign similarly. For different train and test samples ANN outperformed MDC by an upward 5% of WMS for ANN. Further studies are required for improving the performance of ANN's to be put to use in smart phone based SLR with front camera video capture.

References

1. Mohandes, Mohamed.: Arabic sign language recognition. International conference of imaging science, systems, and technology, Las Vegas, Nevada, USA. Vol. 1. (2001).
2. Al-Jarrah, Omar, Alaa Halawani.: Recognition of gestures in Arabic sign language using neuro-fuzzy systems. Artificial Intelligence, pp 117–138, (2001).
3. Kishore, P. V. V., et al.: 4-Camera model for sign language recognition using elliptical fourier descriptors and ANN. Signal Processing And Communication Engineering Systems (SPACES), 2015 International Conference on. IEEE, (2015).
4. Rao, Ananth. G., Kishore, P. V. V.: Sign Language Recognition System Simulated for Video Captured with Smart Phone Front Camera." International Journal of Electrical and Computer Engineering (IJECE) vol. 6, 2176–2187, (2016).
5. Kumar, V. N., Narayana, K. V. L.: Development of an ANN-Based Pressure Transducer. in *IEEE Sensors Journal*, vol. 16, pp 53–60, (Jan. 1, 2016).
6. Zamani, Mahdi., Hamidreza Rashidy Kanan.: Saliency based alphabet and numbers of American sign language recognition using linear feature extraction" Computer and Knowledge Engineering (ICCKE), 2014 4th International eConference on. IEEE, (2014).
7. Zhang, Jihai., Wengang Zhou, Houqiang Li.: A new system for chinese sign language recognition" Signal and Information Processing (ChinaSIP), 2015 IEEE China Summit and International Conference on. IEEE, (2015).

Hyperspectral Unmixing Using Split Augmented Lagrangian Approach

N. Durga Indira and M. Venu Gopala Rao

Abstract This paper presents a trendy approach for unmixing of linear hyperspectral images. This method deals with the minimal volume class of the process. The method is SISAL method. This is called as Simplex Identification via Split Augmented Lagrangian method. The linear hyperspectral unmixing is related in finding the hyperspectral vectors which were present in the least possible volume simplex. It is a non-convex optimization problem and it has some convex constrains. The spectral vectors are being forced by the positive constrains which belongs end member signatures of the convex hull which were in turn replaced by the soft constrains. Augmented Lagrangian optimizations in the order of sequences are used to solve this problem. The resultants algorithmic approach is very fast in approach so that the problems will be able to be solved far beyond the present state-of-art algorithms. The concept Simplex Identification via Split Augmented Lagrangian is explained with simulated data.

Keywords Hyperspectral unmixing · Endmember · Split Augmented Lagrangian

1 Introduction

Hyperspectral images are spectrally overpersistent. They give us some data for the analysis and categorization of spectrally lone materials with some definiteness which leads to accurate information abstraction. Each photon of light has a wavelength. The wavelength of visible light is in between 400 and 700 nm. This number for radio waves will be 30 cms. Hyperspectral images measure the cast back radiation at a series of circumscribed and adjoining wavelength bands. This

N. Durga Indira (✉) · M. Venu Gopala Rao
K L University, Guntur, Andhra Pradesh, India
e-mail: durga.indira@gmail.com

M. Venu Gopala Rao
e-mail: mvgr03@kluniversity.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_5

type of accurate pixel spectrum can give much more clue about the image. The hyperspectral images are used to dig up and to map a wide collection of minerals having differentiating spectra. It is used in mineral calibration and to define the soil properties which include its moisture, organic material and salinity of the soil [1, 2]. Here, we bring into play the compressive sensing (CS) to the hyperspectral image with a goal to make over the original image again. Generally, hyperspectral imaging gets information from electromagnetic spectrum. There are four ways for sampling purpose. They are Spatial scanning, Spectral scanning, Snapshot imaging and Spatio-spectral scanning.

1.1 Spectral Unmixing

This concept is that when we take a hyperspectral image we will get to know that the hyperspectral images are generally of a low resolution. That means a single pixel will be composed of considerable dissimilar materials. Here, each material possesses a unique hyperspectral signature [3]. So, this spectral Unmixing elucidates a single pixel spectral signal into a mixture of materials. These typical material signatures are called endmembers. The materials existing in the image are analytically helpless and are integrated in a fashion of either linearity or nonlinearity. This type of appropriates are combined with maximum proportions of hyperspectral.

When we are given a set of hyperspectral vectors, Unmixing of linear quantities, aspires at assessing the number of associating quantities. These materials are known as endmembers, which are the spectral images mentioned above, and their ampleness fractions. The accession to Unmixing of hyperspectral images is allocated as analytical or trigonometrical approach.

1.2 Pixel Purity Index (PPI)

This method is used to find pixels that are spectrally pure in hyperspectral images. It corresponds to mixing of endmembers. Pixel Purity Index is used for plotting n-D scatter plots on a unit vector. The number of pixel reoccurrences represents purity of that pixel. A purity of that pixel in an image is created where each pixel value is noted as extreme when the number of occurrences is extreme. The Pixel Purity Index creates a new output by counting number of iterations and also adds results to an output. It requires manual intervention for the selection of final set of endmembers. This works by projecting every pixel onto a vector from a set of vectors that spans the reflectance space. A pixel gets points it represents an extremes of all projections. Pixels with highest score are termed as pure [4] (Fig. 1).

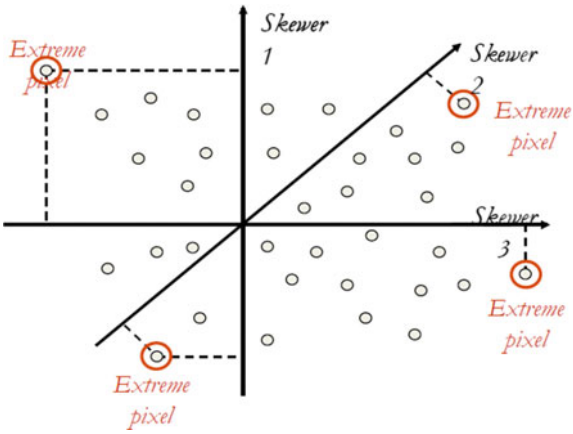


Fig. 1 Graph showing purity index to find endmembers

1.3 Split Augmented Lagrangian Method

Augmented Lagrangian method was known to be method of multipliers and it is considered as best alternative penalty methods. This method was first studied by R. Tyrrel Rockafellar which is in relation to proximal point methods. This method belongs to definite type of algorithms which solves problem of constrained optimization [5, 6]. This method is similar to penalty methods where unconstrained problems are added in series to solve optimization problems and also penalty term is added to that final expression. Generally, another term is added in this method to show difference between augmented Lagrangian and other methods. The added term to this expression is called Lagrange multiplier. This method of adding additional penalty term is called augmentation. From 1970s, Interior point methods and SQP (Sequential Quadratic Programming) are upcoming new methods where the users have increased their usage. They are used mainly because this method considers sparse matrix subroutines. This method has got its reappearance in the areas of compressive sensing and total variation denoizing. Let us consider a constraint

$$\min f(x) \text{ which is subjected to}$$
$$c_i(x) = 0 \quad \forall_i \in I.$$

This constrained problem can be solved by adding series of unconstrained minimization problems by utilization of penalty method

$$\min \varphi_k(X) = f(X) + \sum_{i \in I} c_i\,(x)^2 \mu_k.$$

By using a larger value of μ_k the problem that has occurred here can be solved by a series of iterations. This method uses an objective to solve the constrained problem.

$$\min \varphi_k(X) = f(X) + \frac{\mu_k}{2} \sum_{i \in I} c_i(x)^2 - \sum_{i \in I} \lambda_i c_i(X).$$

After computing each step we must update weights like μ_k and λ following the below step:

$$\lambda_i \leftarrow \lambda_i - \mu_k c_i(X_k)$$

Here X_k is solution to unconstrained problem after k steps, i.e.,

$$X_k = argmin\, \varphi_k\,(X).$$

The λ variable in the equation is Lagrange multiplier, and after every iteration the accuracy increases. The major advantage of this method is we need not do $\mu \to \infty$ for solving original problem. The presence of Lagrange multiplier makes the value of μ smaller.

2 Formulation for the Problem

Assuming p materials in a given scene termed endmembers with spectral signatures $m_i \in R^l$, when value of i tends from 1 to p here i ≥ p. Indicates spectral line numbering. The vectors that are seen in Hyperspectral data are linear endmember mixture of spectrum signs in a linear mixing model wherein weights illustrates the fractions occupied in the pixel by each material. Therefore, the vectors which are present in spectrum represent hull of convex endmember spectrum signs. Let $\mathrm{X} \equiv [x_1, \ldots, x_n] \in R^{l \times m}$ represent set of data (matrix) containing the data that is seen in spectra $x_i \in R^l$, $\mathrm{Q} \equiv [q_1, \ldots, q_n] \in R^{p \times m}$ a matrix having the respective fractions, i.e., $x_i = Nq_i$ for $\mathrm{I} = 1, \ldots, \mathrm{m}$, where $\mathrm{N} \equiv [n_1, \ldots, n_p] \in R^{p \times p}$ is the mixing matrix possessing the endmembers and q_i is a vector indicating the fractions. Because q_i components are non-negative and sum one, the fractional abundance vectors will be in the standard p-simplex set $Q_P = \left\{ q \in R^p : q \geq 0, 1_p^T q = 1 \right\}$. Thus,

$$\mathrm{X} = \mathrm{Nq}, \quad \mathrm{Q} \in Q_P^m \tag{1}$$

Suppose the endmember spectral signatures n_i, where the value of I varies from 1 to p, which are independently linear, now this subset $\{\mathrm{x} \in R^l : x = Nq, q \in T_p\}$ is (p − 1) dimensional simplex, and estimation of N amounts infer its vertices. The

Demonstration about the two simple dataset that produce the column of N. Presuming the signal space and the number of endmembers are known beforehand and the observed vectors $x_i, i = 1, \ldots, n$, indicate coordinates which corresponds q-dimension of the subspace of signal, i.e., i that is equal to q. Here X, and from research paper, concluding N, Q set of data (matrix) by accommodating least part of the input are put through limitations $Q \geq 0$ and $1_P^T Q = 1_m$. As the part which describes total volume that is described by queue of N is proportional to determinant $|(N)|$.

Then,

$$\begin{aligned} N^* &= arg_N min |\det(N)| \\ &\mathrm{RX} \geq 0,\ 1_P^T RX = 1_m^T, \end{aligned} \tag{2}$$

where $\mathrm{R} \equiv N^{-1}$. As det(R) = 1/det (N), (2) Can be replaced with

$$\begin{aligned} R^* &= arg_R min - log|\det(R)| \\ &\mathrm{RX} \geq 0,\ 1_P^T \mathrm{RX} = 1_m^T. \end{aligned} \tag{3}$$

The restraints in above Eq. (3) denote complex arrangement. The set of data (matrix) R is symmetric and definite which is positive, convex problem (3) occurs. But here neither most practical cases R is not true values and hence (3) is not a convex set. Hence here exists no chance to find the optimum values of (3) systematically. Simplex Identification via Split Augmented Lagrangian algorithm introduced mentioned under targets at good suboptimal solutions. Initially to unravel the constraint $1_p^T RX = 1_m^T$. We identify that the vector 1_m^T does not accord empty spacing in X matrix. If not vector would accord the affaire frame N, implies that the columns of N is dependent. Thus, equality values are multiplied on the R.H.S. by $X^T (XX^T)^{-1}$, we get $(1_p^T RX = 1_n^T) = (1_p^T R = b^T)$, where $b^T = 1_m X^T (XX^T)^{-1}$, the problem (3) simplifies to

$$\begin{aligned} R^* &= arg_R min - log|\det(R)| \\ &\mathrm{RX} \geq 0,\ 1_P^T R = b^T \end{aligned} \tag{4}$$

In place of solving (4), solve altered version:

$$\begin{aligned} R^* &= arg_R min - \log|\det(R)| + \tau \|RX\|_{\mathrm{h}} \\ &1_P^T R = b^T, \end{aligned} \tag{5}$$

where $\|X\|_{\mathrm{h}} = \sum_{ij} \mathrm{h}\left([Y]_{ij}\right)$ and h(y) = max{−y, 0} which is called as hinge function. The $\|RX\|_{\mathrm{h}}$ plays the role of regularizer by penalizing the non-positive

parts in RX are proportional with its absolute value. Regularization component is monitored by its constraints $\tau > 0$. Here soft constrained formulation gives answers which have low initialization and are booming to noise. Further altering equality constraints n × p with regularizer gives scope to manage ample problems.

2.1 Convex Subproblem Sequence

Assume r ≡ $vec(R)$ indicate operator which groups elements of R in matrix r. Here Vec (BA) = (A^T I) and defining f(r) = $-\log|\det(R)|$, then (5) can be written as

$$\begin{aligned} r^* &= arg_r min\, f(r) + \tau \|Br\|_h \\ Ar &= b. \end{aligned} \tag{6}$$

We approximate (6) with computation of small group r_k, where value of k ranges between 0, 1, …, for below procedure utilizing the quadratic approximation for f(r).

2.2 Concept of Sisal Method

Some optimization problems are

$$\begin{aligned} &min_{r,z}\, E(r,\ z) \\ &Ar = b,\ Br = z, \end{aligned} \tag{7}$$

where $E(r,z) \equiv g^T r + \mu \|r - r_k\|^2 + \tau \|z\|_h$.

In Eq. (7), there is a variable r which is divided into given set (r, z), the restraint Br = z was linked through it. The constraint Br = z was subjected and the Augmented Lagrangian (AL) is as follows:

$$\mathcal{L}(r,z,d,\tau) \equiv E(r,z) + \alpha^T (Br - z) + \tau \|Br - z\|^2 \tag{8}$$

$$= E(r,z) + \tau \|Br - z - d\|^2 + c. \tag{9}$$

Here, the term α holds the Lagrange multipliers, $d = -\alpha/(2\tau)$, the irrelevant constant is named with c. The AL algorithm comprises in minimization of $\mathcal{L}$th respect to (r, z) now changing value of α with respect to d is as follows [7, 8]. The Lagrange dual of the problem (7) has got applied by PPA with adequate initializations. For k = 0, 1, 2, … the sequence d_k merges. To find the solution for this problem which is of dual kind the points in cluster of that set z_k where the value of k ranges from 0, 1, …. These will be outcomes for problem (7), [9, 10].

3 Experimental Results

This section expresses outputs we got with the Simplex identification via split augmented Lagrangian method, Minimum volume simplex analysis and vector component analysis exercised to the sets which were simulated. We set the parameters of the SISAL regularization to $\lambda = 10$, $\tau = 1$ and $\mu = 10^{-4}$ are remaining parameters which were set to it. Basically, we could also remove these values so as we can obtain better results. With the linear observation model (1) the information was generated. The fractions of ampleness A_r Dirichlet is distributed with criterion $\mu_i = 1$, for $i = 1, \ldots, p$. Here M is a collaborating matrix which is generated arbitrarily with i.i.d. We use components which are uniformly distributed just to confirm that no pure component will become a gift. We possess a tendency where we discard all pixels with ampleness fraction greater than 0.8. Here S/N (SNR) was set to 50 dB.

3.1 Sisal Analysis

The Fig. 2a–c shows the outputs related to the unmixing when we take pixel value = 3 as the endmembers range for Simplex identification via split augmented Lagrangian method, Minimum vector simplex analysis algorithms. Here the representation is as follows where dots are the spectral vectors. Here different representations of symbols are noted as endmembers by the means of unmixing algorithms. Here, when we perform the unmixing downside with number of pixels (n) = 10,000 and number of endmembers are noted to be 3, then the SISAL outputs are obtained as follows. The SNR value is taken to be 50 dB.

The outputs related to the unmixing when we take p = 6, 8, 10, 15 as the endmembers range for Simplex identification via split augmented Lagrangian method, Minimum vector simplex analysis algorithms are shown in Table 1. The representation is as follows where dots are the spectral vectors. Here different

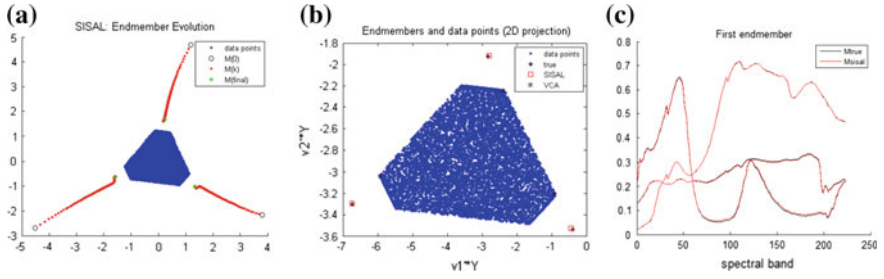


Fig. 2 **a** SISAL endmember evolution for p = 3. **b** SISAL 2D projection for p = 3. **c** Spectral band for p = 3

Table 1 SISAL output values comparison

P	Conditioning value of M	SNR		Time		Error	
		Eigen value	Estimated value	SISAL	VCA	SISAL	VCA
3	14.063388	0.851195	139.043	4.07	0.41	0.163950	0.299697
6	113.786420	0.000021	139.634	3.57	0.37	1.008482	0.482419
8	131.897790	0.000075	139.372	3.89	0.41	1.151109	0.590494
10	186.144444	0.000002	143.623	4.78	0.52	1.390094	0.553926
15	474.319508	0.000001	144.034	5.38	0.61	1.576306	0.688807

representation of symbols are noted as endmembers by the means of unmixing algorithms. Here, when we perform the unmixing downside with number of pixels (n) = 10,000 and number of endmembers are noted to be 6 then the SISAL outputs are obtained as follows. The SNR value is taken to be 50 dB. The below shown table represents various values of SNR, Time and error values for the required SISAL outputs. Time and Error columns estimate the difference between SISAL and VCA. SNR value is estimated in term of Eigen values and estimated values. The table is drawn for various values of endmembers according to their existence.

3.2 *Noise Comparison of SISAL Values*

The Fig. 3a–c shows SISAL values for noise comparison related to the unmixing when we take p = 15 as the endmembers range for Simplex identification via split augmented Lagrangian method, Minimum vector simplex analysis algorithms. Here the representation is as follows where dots are the spectral vectors. Here different representations of symbols are noted at endmembers by the means of unmixing algorithms. Here, when we perform the unmixing downside with number of pixels (n) = 10,000 and number of endmembers are noted to be 15 then the SISAL outputs are obtained as follows. The SNR value is taken to be 50 dB.

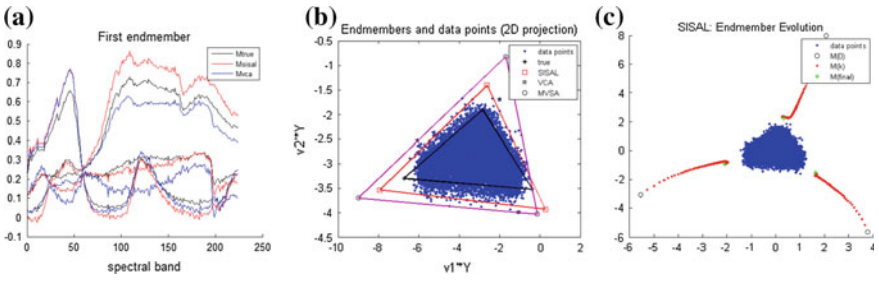


Fig. 3 **a** Endmember evolution for p = 3. **b** 2D projection for p = 3. **c** Spectral band for p = 3

Table 2 SISAL noise comparison of output values

P	Conditioning value of M	SNR		Time		Error	
		Eigen value	Estimated value	SISAL	VCA	SISAL	VCA
3	14.063388	0.851195	139.043	4.07	0.41	0.163950	0.299697
6	113.786420	0.000021	139.634	3.57	0.37	1.008482	0.482419
8	131.897790	0.000075	139.372	3.89	0.41	1.151109	0.590494
10	186.144444	0.000002	143.623	4.78	0.52	1.390094	0.553926
15	474.319508	0.000001	144.034	5.38	0.61	1.576306	0.688807

The various values of SNR, Time and error values for the required SISAL outputs are represented in Table 2. Time and Error columns estimate the difference between SISAL and VCA. SNR value is estimated in term of Eigen values and estimated values. The table is drawn for various values of endmembers according to their existence.

4 Conclusion

Simplex Identification via Split Augmented Lagrangian, a replacement algorithmic rule for unmixing of hyperspectral images is a technique of minimum volume category. Hyperspectral information is obtained by measuring the minimum volume simplex having hyperspectral information. By increasing the series of variable rending increased Lagrangian optimizations, the problems due to optimization is resolved.

References

1. José Bioucas-Dias, M.: A Variable Splitting Augmented Lagrangian Approach To Linear Spectral Unmixing. Technical report, Instituto Superior Te´cnico, TULisbon, Lisbon, (2009).
2. Figueiredo, M., Bioucas-Dias, J., Afonso, M.: Fast image restoration using variable splitting and constrained optimization. Technical report, TULisbon, Lisbon, (2009).
3. Goldstein, T., Osher, S.: The split Bregman method for l1 regularized problems. Technical Report 08-29, Computational and Applied Math., Univ. of California, Los Angeles, (2008).
4. Iusem, A.: Augmented Lagrangian methods and proximal point methods for convex optimization. Investigación Operativa, vol. 8, pp. 11– 49, (1999).
5. Setzer, S.: Split Bregman algorithm, Douglas-Rachford splitting, and frame shrinkage. in Proceedings of the Second International Conference on Scale Space Methods and Variational Methods in Computer Vision, LNCS Springer, (2009).
6. C.-Y. Chi, T.-H. Chan, W.-K. Ma.: A convex analysis based optimization minimum-volume enclosing simplex algorithm for hyperspectral unmixing. in IEEE International Conference in Acoustics, Speech and Signal Processing-ICASSP'2009, Taiwan, (2009).

7. Li, L., Bioucas-Dias, J.: Minimum volume simplex analysis: a fast algorithm to unmix hyperspectral data. in IEEE International Geoscience and Remote sensing Symposium - IGARSS2008, Boston, (2008).
8. Nascimento, B., Bioucas-Dias, J.: Does independent component analysis play a role in unmixing hyperspectral data?. IEEE Transactions on Geoscience and Remote Sensing, vol. 43, pp. 175–187, (2005).
9. Miao, L., Qi, H.: Endmember extraction from highly mixed data using minimum volume constrained nonnegative matrix factorization. IEEE on GRS, vol. 45, pp. 765–777, (2007).
10. Manolakis N. Keshava, D. G., Kerekes, J. P., Shaw, G. A.: Algorithm taxonomy for hyperspectral unmixing. Proc. SPIE Vol. 4049, Algorithms for Multispectral, Hyperspectral, and Ultraspectral Imagery, vol. VI, pp. 42, (2000).

A Robust and Oblivious Grayscale Image Watermarking Scheme Based on Edge Detection, SVD, and GA

Tamirat Tagesse Takore, P. Rajesh Kumar and G. Lavanya Devi

Abstract For multimedia data copyright protection application, robustness to various attacks is one of the most important requirements that a digital watermarking system should possess. Hence, using matrix factorization technique (i.e., singular value decomposition) and genetic algorithm, a new grayscale image watermarking system is presented in this paper which can satisfy the desired watermarking requirements. Canny edge detector is used to form two subimages and watermark is inserted into the first subimage by amending singular value coefficient based on the pixel value of a watermark. The genetic algorithm is employed in the proposed scheme to search the best multiple scaling factors which can give the highest robust watermarked image without losing transparency. The robustness and transparency of the scheme are measured using a quality metric, normalized-correlation-coefficient (NCC), and peak-signal-to-noise-ratio (PSNR), respectively. In this paper, to test the degree of robustness, watermarked image is attacked using a maximum number of image processing attacks compared to other existing methods and experimental results obtained show improved performance in terms of robustness.

Keywords Image watermarking · Singular value decomposition · Genetic algorithm · Edge detection · Robustness · Transparency

T. Tagesse Takore (✉) · P. Rajesh Kumar
Department of ECE, College of Engineering (A), Andhra University, Visakhapatnam, India
e-mail: tameauce2014@gmail.com

P. Rajesh Kumar
e-mail: rajeshauce@gmail.com

G. Lavanya Devi
Department of CS & SE, College of Engineering (A), Andhra University, Visakhapatnam, India
e-mail: lavanyadevig@yahoo.co.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*, Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_6

1 Introduction

Nowadays, due to the proliferation of computers and Internet, exchanging digital multimedia data becomes a very easy task. However, this extraordinary technological revolution makes way for digital multimedia data such as image, audio, and video to be easily duplicated, modified and redistributed without the consent of copyright owner which results in significant revenue loss. Thus, getting efficient copyright protection technique becomes a critical issue among authors and it also gets the attention of numerous scholars. As a result, many research works have been undertaken to find the best potential solution for copyright protection problem and their research findings are available in the literature. Among these suggested methods, a digital watermarking technique is one of the most efficient solutions to the problem [1]. The concept of digital watermarking for copyright protection was introduced at the beginning of the 1990s, and it is a method which inserts a digital signature called watermark into the original data to protect.

There are two major stages in digital watermarking: watermark embedding and extraction [2]. In watermark embedding stage an original data I_M is watermarked using a watermark W_B and watermark key K_E. The embedding process slightly modifies original data I_M using an embedding algorithm, and it gives the watermarked data I_W as an output. The watermarked signal I_W can then be sent via an unsecured transmission channel where it could be corrupted by attackers leading to an altered watermarked image $\hat{I}w$.

The watermark extraction process begins with the reception of the watermarked image which can be attacked one by the third party, while being transmitted through a communication channel. The survival of embedded information can be checked by extracting the watermark using an extraction algorithm. A watermarking scheme which does not require the original data for watermark extraction is known to as a blind (or oblivious) watermarking scheme. However, a non-blind watermarking scheme requires original data I_M to extract inserted watermark.

A watermarking system can be categorized into three groups based on robustness: fragile, semi-fragile, and robust. A watermark, which uses for copyright protection application should always remain in the host data, even if different attacks are performed on watermarked data aiming to remove or destroy the watermark. So, the robust watermarking algorithm provides watermarked data which can withstand different signal processing attacks, and the watermark is still extractable after attacks. On the contrary, a fragile watermarking scheme is used to diagnose unauthorized modification such that slight change of the watermarked data will alter or destroy the watermark easily.

In general, watermark embedding operation can be performed either in the spatial domain, transform domain or hybrid domain. Spatial domain watermarking algorithm embeds a watermark into host image by modifying the intensity value of a cover image directly [3, 4]. However, Transformed domain watermark embedding

technique inserts a watermark by altering the transformed coefficients of the original image. Usually, discrete wavelet transform (DWT) [5, 6], discrete Fourier transform (DFT) [7], discrete cosine transform (DCT) [8, 9], and discrete Hadamard transform (DHT) [10] are the most frequently used transformation methods which are available in the various literature. In addition, singular value decomposition (SVD) technique [11, 12] is also used to represent an image in a different form.

The major challenge in digital image watermarking system is to design a robust watermarking system that can protect copyright by making the embedded watermark resist different image processing attacks. Even though several robust and blind image watermarking algorithms are proposed, still there are some limitations which require further study in the area. In fact, there is no algorithm in the literature with a watermark which can resist all image processing attacks. Hence, in this paper, an attempt is made to make the proposed watermarking system be more robust which can resist a maximum number of attacks compared to existing algorithms. To fill the existing gap we have proposed a blind and robust watermarking algorithm based on SVD, edge detection, and Genetic algorithm (GA). We have employed canny edge detection technique to select suitable regions of the image where a watermark is to be embedded which can give the best robustness and transparency. Two non-overlapping subimages are formed using blocks with a high and low edge number. A watermark is embedded into a first subimage by modifying singular value coefficient based on a pixel value of the watermark, and the second subimage is used as a reference for watermark extraction. Figure 1 depicts the two subimage formed from the original Lena image. We have used a genetic algorithm (GA) to search best scaling factors that modify singular values coefficients of subimages at the time of watermark embedding. In their proposed algorithm, K. Ramanjaneyulu et al. [13] obtained the best performance in terms of robustness and transparency by using multiple scaling factors (MSF). The robustness and transparency of the scheme are measured using a quality metric, normalized-correlation-coefficient (NCC), and peak-signal-to-noise-ratio (PSNR), respectively.

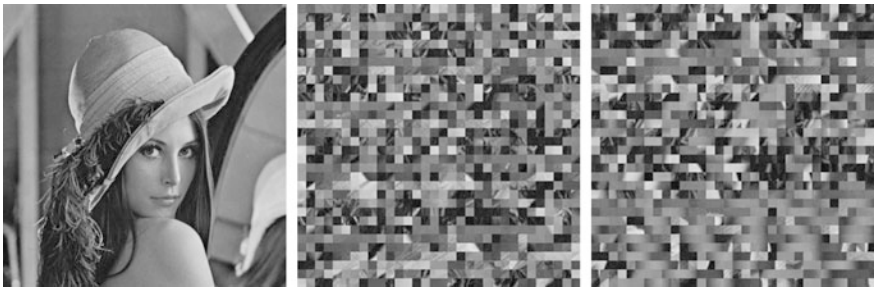


Fig. 1 Images of Lena and subimages formed using Canny edge detection techniques

2 Genetic Algorithm, SVD, and Scaling Factors

2.1 Genetic Algorithm

In digital image watermarking, scaling factors which we use to modify singular value coefficients during watermark embedding determine the level of robustness and imperceptibility of watermarked image. Therefore, the problem of finding suitable scaling factors that can give optimum performance in terms of PSNR and NCC can be viewed as an optimization problem. For that, we have employed GA to optimize the performance of the scheme by searching best suiting scaling factors for watermark embedding. Randomly initializing candidate solutions (known as population) is the first step in the genetic algorithm optimization process, and then each individual is passed to fitness function to evaluate their quality. The fitness function is formulated from quality measuring metric PSNR and NCC. Those individuals with the best fitness values are picked to be parents to produce new generation by using crossover and mutation operation. The processes keep on running until preset stopping condition is satisfied. In this work, we have executed the algorithm number of time varying GA parameters (i.e., population size, selection rate, mutation rate and iteration rate) keeping the record of fitness value for every run. The outline of generic GA algorithm is presented in Fig. 2.

$$\mathrm{ff} = \mathrm{PSNR} + \beta \mathrm{xNCC} \tag{1}$$

where β is constant which uses to keep a balance between robustness and imperceptibility. Formulae for PSNR and NCC are given in Eqs. 2 and 3, respectively.

$$\mathrm{PSNR} = 10\log_{10}\left[\frac{255^2}{\frac{1}{\mathrm{MN}}\sum_{\mathrm{p}=1}^{\mathrm{M}}\sum_{\mathrm{q}=1}^{\mathrm{N}}\left(\mathrm{I_W(p,q)} - \mathrm{I_M(p,q)}\right)^2}\right] \mathrm{dB} \tag{2}$$

$$\mathrm{NCC} = \left[\frac{\sum_p^k \sum_q^L W_B(p,q) W_E(p,q)}{\sqrt{\sum_{p=1}^k \sum_{q=1}^L W_B(p,q)^2 \sum_{p=1}^k \sum_{q=1}^L W_E(p,q)^2}}\right] \tag{3}$$

2.2 Singular Value Decomposition

Singular value decomposition is linear algebra technique, which uses to factorize a real or complex rectangular matrix $\mathrm{I_M}$ into three unique matrices $\mathrm{U_m}$, $\mathrm{S_m}$, and $\mathrm{V_m}$ such that,

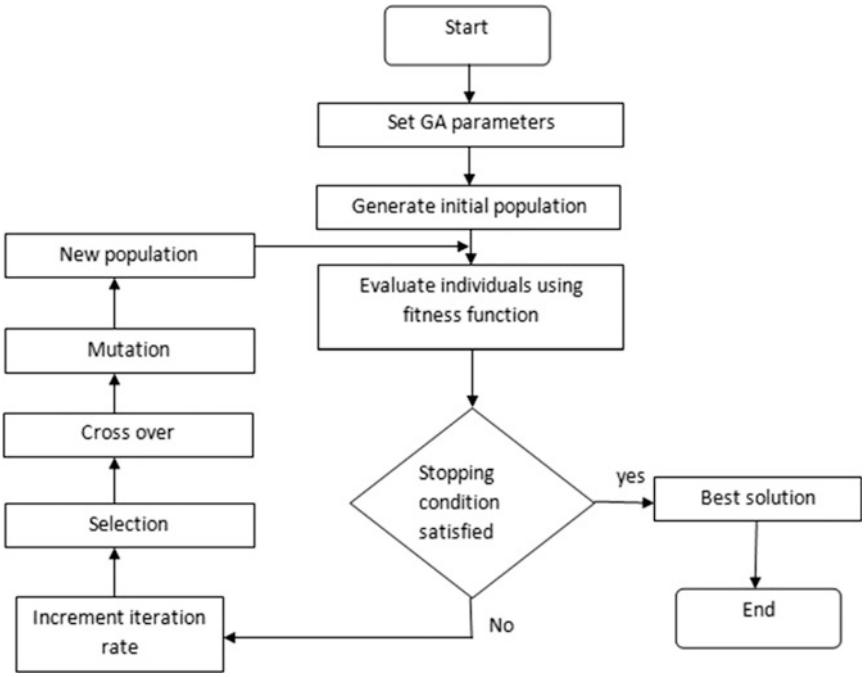


Fig. 2 Generic GA optimization algorithm scheme

$$I_M = U_m x S_m x V_m^T \tag{4}$$

where U_m and V_m are orthogonal matrices (i.e., $U_m U_m^T = I$, $V_m V_m^T = I$); S_m is a non-negative diagonal matrix containing the square roots of the eigenvalues of either U_m or V_m arranged in descending order diagonally. SVD-based watermarking algorithms have a great advantage since original image quality is not affected significantly due to a slight change in singular value and this property makes it be preferred most for a digital image watermarking application. In this paper, we have used SVD to factorize the two subimages to embed a binary watermark.

2.3 Scaling Factors

Scaling factors which we use to modify the coefficients during watermark embedding determine the level of robustness and imperceptibility of the scheme. Using multiple scaling factors (MSF) to modify different range of singular values improve the performance of the watermarking scheme other than using single scaling factor. Hence, we have divided the entire singular value coefficients into two non-overlapping sub-ranges in our work. Let S_{blk1} and S_{blk2} denote block

singular value of subimage 1 and subimage 2, respectively. Two different scaling factors k_1 and k_2, where $k_1 < k_2$ are used to modify singular value coefficients based on pixel value of watermark W_B (i, j). Binary watermark W_B is embedded using the following equation.

$$\begin{aligned}
&\text{If } W_B(i,j) = 1 \\
&\quad S_{blk1}(p,q) = S_{blk1}(p,q) + k \times S_{blk2}(p,q), \text{if } S_{blk1}(p,q) \geq S_{blk2}(p,q) \\
&\qquad\qquad = S_{blk2}(p,q) + k \times S_{blk1}(p,q), \text{if } S_{blk2}(p,q) > S_{blk1}(p,q) \\
&\text{If } W_B(i,j) = 0 \\
&\quad S_{blk1}(p,q) = S_{blk2}(p,q) - k \times S_{blk1}(p,q), \text{if } S_{blk1}(p,q) S_{blk2}(p,q) \\
&\qquad\qquad = S_{blk1}(p,q) - k \times S_{blk2}(p,q), \text{if } S_{blk2}(p,q) > S_{blk1}(p,q)
\end{aligned} \tag{5}$$

where $p = q = 1$ and k denotes the embedding scaling factor, i.e., $k = k_1$ if S_{blki} $(p, q) \geq T$; $k = k_2$ if S_{blki} $(p, q) < T$ for some threshold value T and $i \in \{1, 2\}$.

3 Proposed Watermarking Algorithm

The proposed algorithm has two major processes: watermark embedding and extraction.

3.1 Proposed Watermark Embedding Algorithm

The proposed algorithm takes grayscale cover image I_M of size $N \times N$ and binary watermark W_B of size $R \times R$ as input to give watermarked image I_W as an output. The embedding process is presented as follows:

Step1: Cover image I_M is decomposed into two subimages (i.e., subimage 1 and subimage 2) using the concept discussed in Sect. 1. The size of the two subimages is $N/2 \times N/2$.

Step2: perform block-based SVD operation on both subimages using 8×8 block size. Let block 1 and block 2 be a block of subimage 1 and subimage 2, respectively.

$$\begin{aligned}
[U_{blk1}, S_{blk1}, V_{blk1}] &= \text{SVD (block 1)} \\
[U_{blk2}, S_{blk2}, V_{blk2}] &= \text{SVD (block 2)}
\end{aligned} \tag{6}$$

Step3: Use GA-based procedure to find best scaling factors.

Step4: Modify singular value coefficients $S_{blk1}(1, 1)$ according to watermark pixel value $W_B(i, j)$ using Eq. 5 to obtain modified singular value $S^M{}_{blk1}$.

Step5: Apply block-based inverse SVD operation using modified singular values to obtain watermarked block.

$$\text{Watermarked block} = U_{blk1} \text{x } S^{M}_{blk1} \text{x} V^{T}_{blk1} \quad (7)$$

Step6: place watermarked blocks backs to their original position to obtain a watermarked image I_W.

3.2 Proposed Watermark Extraction Algorithm

Since the proposed watermarking scheme is blind, original cover image I_M is not required for watermark detection and extraction. The extraction process is summarized as follows.

Fig. 3 Test images (i.e., Lena, mandrill and watermark) used for algorithm simulation

Fig. 4 Watermarked Lena and mandrill images

Step1: Possibly attacked watermarked image $\hat{I}w(i, j)$ of size $N \times N$ is decomposed into two subimages (i.e., subimage 1_E and subimage 2_E) using the same technique which we have used during watermark embedding.

Step2: Apply block-based SVD on both reference images.

$$\begin{aligned}[U_{1E},\ S_{1E},\ V_{1E}] &= \mathrm{SVD}\ (\mathrm{block}1_E)\\ [U_{2E},\ S_{2E},\ V_{2E}] &= \mathrm{SVD}\ (\mathrm{block}2_E)\end{aligned} \tag{8}$$

Table 1 Extracted watermark images from attacked watermarked image

Extracted watermark image		Diffrent attacks					
		GS	SPN	MF	HE	CA	CRP
	lena						
	mandrill						
		JPEG	AVF	GF	CM	BP	SRP
	lena						
	mandrill						
		RS	WF				
	lena						
	mandrill						

Step3: Extracted binary watermark image can be obtained using the following equation.

$$\begin{aligned} W_E(i,j) &= 1 \text{ if } S_{1E}(1,1) \geq S_{2E}(1,1) \\ W_E(i,j) &= 0 \text{ if } S_{1E}(1,1) < S_{2E}(1,1) \end{aligned} \tag{9}$$

4 Experimental Results and Discussion

We have conducted a series of test to assess the performance of proposed algorithm varying GA parameters to search the best multiple scaling factors which can give better PSNR and NCC value. We have used two different host images of size 512 × 512 and binary watermark of size 32 × 32 as input test the algorithm. In Fig. 3, these test images are shown. The watermark is embedded into the host image using the proposed algorithm and Fig. 4 depicts a watermarked Lena and mandrill images having a PSNR value of 45.2223 and 43.8038 dB, respectively. Fourteen different image processing attacks were selected to test the robustness. These attacks are: Gaussian white noise (M = 0 and V = 0.01), salt and pepper noise (D = 0.02), median filter (3 × 3), histogram equalization, contrast adjusting ($\gamma = 0.925$), cropping (25% of image portion), JPEG compression (QF = 50), average filter (3 × 3), Gaussian filter (3 × 3), camera motion (len = 9, $\theta = 0$),

Table 2 PSNR, NCC and scaling factors (k) obtained from simulation for various attacks

Attacks	Lena image		Mandrill image	
	[PSNR, NCC]	Optimized scaling factors (k_1, k_2)	[PSNR, NCC]	Optmized scaling factors (k_1, k_2)
GN	[42.0196, 0.9723]	(0.0291, 0.0413)	[41.0535, 0.9915]	(0.0320, 0.0381)
SPN	[40.9829, 0.8824]	(0.0346, 0.0352)	[41.7557, 0.8822]	(0.0381, 0.0422)
MF	[43.8486, 0.9466]	(0.0179, 0.0407)	[40.6241, 0.9707]	(0.0380, 0.0512)
HE	[45.2223, 0.8449]	(0.0105, 0.0374)	[43.0674, 0.8571]	(0.0255, 0.0412)
CA	[43.7274, 0.9702]	(0.0187, 0.0327)	[42.9972, 0.9991]	(0.0293, 0.0380)
CRP	[42.5192, 0.8987]	(0.0250, 0.0372)	[43.0722, 0.8099]	(0.0369, 0.0381)
JPEG	[42.2179, 0.9787]	(0.0275, 0.0417)	[41.8005, 1]	(0.0317, 0.0320)
AVF	[43.4504, 0.9268]	(0.0211, 0.0321)	[42.2168, 0.9465]	(0.0356, 0.0422)
GF	[45.1229, 0.9576]	(0.0110, 0.0411)	[43.1052, 0.9957]	(0.0293, 0.0393)
CM	[44.8819, 0.6775]	(0.0132, 0.0227)	[43.0261, 0.6431]	(0.0297, 0.0421)
BP	[44.5185, 0.9745]	(0.0159, 0.0426)	[43.0971, 1]	(0.0356, 0.0387)
SRP	[44.8228, 0.9915]	(0.0137, 0.0434)	[43.4693, 0.9957]	(0.0227, 0.0399)
RS	[44.2088, 0.9554]	(0.0169, 0.0427)	[41.9521, 0.9915]	(0.0343, 0.0380)
WF	[41.6721, 0.9451]	(0.0305, 0.0423)	[43.0736, 0.9872]	(0.0382, 0.0399)

bitplane removing (LSB image discarded), image sharpening, resizing (512 → 256 → 512), and Weiner filter (3 × 3). For the sake of convenience, the attacks are identified, respectively, as GN, SPN, MF, HE, CA, CRP, JPEG, AVF, GF, CM, BP, SRP, RS, and WF.

We have set Population size of 16, selection rate of 0.5, a mutation rate of 0.01 and iteration rate of 10, 50 and 100 for GA. After performing the attacks on watermarked image, we have checked the survival of watermark using the proposed extraction procedure, and we have computed NCC between original watermark W_B and extracted watermark W_E to evaluate the level of resemblance. In Table 1 extracted watermark images from the attacked watermarked images are shown. The NCC result obtained shows the robustness of proposed watermarking algorithm to the attacks performed. In Table 2, the corresponding PSNR and NCC values obtained for different attacks are given.

5 Conclusion

In this paper, a novel blind grayscale image watermarking algorithm based on canny edge detection and SVD is presented. To achieve the best possible robustness and transparency, a GA optimization technique is employed to find best multiple scaling factors which are used to modify singular values coefficients during watermark embedding. Experimental results demonstrate that the proposed algorithm provides improved imperceptibility and excellent robustness against a wide range of image processing attacks.

References

1. Podilchuk, C., Delp, E.: Digital watermarking algorithms and applications. IEEE Signal Processing Magazine. 18 (2001) 33–46
2. Sharma, A., Jaiswal, A.: A Review on Digital Image Watermarking Techniques. International Journal of Computer Applications. 117 (2015) 36–45
3. Singh, A.K., Sharma, N., Dave, M., Mohan, A.: A novel technique for digital image watermarking in spatial domain. In proc. of IEEE International Conference on Parallel, Distributed and Grid Computing. (2012) 497–501
4. Dorairangaswamy, M.A.: Robust Blind Image Watermarking Scheme in Spatial Domain for Copyright Protection. International Journal of Engineering and Technology. 1 (2009) 249–255
5. Tianming, G., Yanjie, W.: DWT-based digital image watermarking algorithm. İn proc. IEEE International Conference on Electronic Measurement & Instruments. 3 (2011) 163–166
6. Zheng, J.-B., Feng, S.: A Color Image Watermarking Scheme in the Associated Domain of DWT and DCT Domains Based on Multi-channel Watermarking Framework. Digital Watermarking Lecture Notes in Computer Science. (2009) 419–432
7. T., M.: An Efficient Image Watermarking Approach based on Fourier Transform. International Journal of Computer Applications. 136 (2016) 8–11

8. Zeng, Y.-C., Pei, S.-C., Ding, J.-J.: DCT-Based Image Protection using Dual-Domain Bi-Watermarking Algorithm. İn proc. IEEE International Conference on Image Processing. (2006) 2581–2584
9. Wang, C.: Research of digital image watermarking algorithm based on DCT. Eighth International Conference on Digital Image Processing. (2016)
10. Moeinaddini, E., Ghasemkhani, R.: A novel image watermarking scheme using blocks coefficient in DHT domain. The International Symposium on Artificial Intelligence and Signal Processing. (2015) 159–164
11. Takore, T.T., Kumar, P.R., Devi, G.L.: Efficient gray image watermarking algorithm based on DWT-SVD using genetic algorithm. İn proc. IEEE International Conference on Information Communication and Embedded Systems. (2016) 1–6
12. Aslantas, V.: An SVD based digital image watermarking using genetic algorithm. In proc. IEEE International Symposium on Signal Processing and Its Applications. (2007) 1–4
13. Ramanjaneyulu, K., K, R.: An Oblivious and Robust Multiple Image Watermarking Scheme Using Genetic Algorithm. The International journal of Multimedia & Its Applications. 2 (2010) 19–38

Design and Analysis of Various Slots on Hexagonal Boundary Patch Antennas for Enhanced Gain

Kalpana Muvvala, R. Ramana Reddy and Naresh Kumar Darimireddy

Abstract Many antenna experts reported slotted microstrip patch antennas due to their compactness and integration in communication systems. Limitations of patch antennas are bandwidth and gain. Extensive research is carried out on patch antennas to improve gain and bandwidth. Many researchers had reported on regular shapes like square, rectangle, and circular patches. In this paper, a hexagonal boundary patch antenna is considered. In an attempt to increase the gain different shapes of slots on hexagonal patch antenna (HPA) are considered. From the results, it is evident that gain is increased with slots on patch antenna. The hexagonal slot on hexagonal patch antenna results in a gain of 6.8 dB. Simulation is carried out using HFSS software. Fabricated antenna is tested for practical results using vector network analyzer.

Keywords HPA · Return loss · Gain · Bandwidth

1 Introduction

With the increasing density of applications, the design of an antenna for the concerned wide range of frequencies is a challenging task for the antenna engineers [1]. The design aspects are twofold. In one way, the design should ensure sweeping the

K. Muvvala (✉)
Department of ECE, JNTUK, Kakinada, India
e-mail: muvvala.kalpana@gmail.com

R. Ramana Reddy
Department of ECE, MVGR College of Engineering (A),
Vizianagaram, AP, India
e-mail: profrrreddy@yahoo.co.in

N.K. Darimireddy
Department of ECE, Lendi Institute of Engineering and Technology,
Vizianagaram, AP, India
e-mail: yojitnaresh@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_7

entire band and on the other way it should exhibit consistency in terms of several radiation characteristics and physical constraints. The physical constraints include adaptability to compact electronic system environment, while the radiation characteristics involve in producing similar radiation characteristics for the entire band of frequencies [2]. The patch antenna is recommended in order to fit with the demand of compactness and conformableness of the communication system's hardware [3]. In the past, a lot of antennas were developed to operate in the UWB spectrum with reasonable performance [4, 5]. Slots of various shapes have been used to enhance the bandwidth of the patch antennas. Munir et al. [6] have shown that multiple slots etched in the rectangular patch can increase the bandwidth. It has been shown that reduced ground plane along with slots provides high gain and low return loss [7, 8]. Multilayers with slots are incorporated to improve the gain of the patch antennas used for wireless applications [9, 10].

In this paper, a hexagonal shaped patch antenna with slots of different shapes is considered. The antenna is fed with microstrip feed with matched impedance conditions. For each of these slotted hexagonal patch antennas, VSWR, return loss and gain are measured over the frequency range. The gains of slotted hexagonal patch are compared with that of the hexagonal patch without a slot.

2 Antenna Design and Configuration

The advantage of the hexagonal patch antenna is the current distribution is as similar as circular but the area occupation is less in hexagonal patch antenna. The proposed hexagonal antenna is shown in Fig. 1. One side of proposed hexagonal

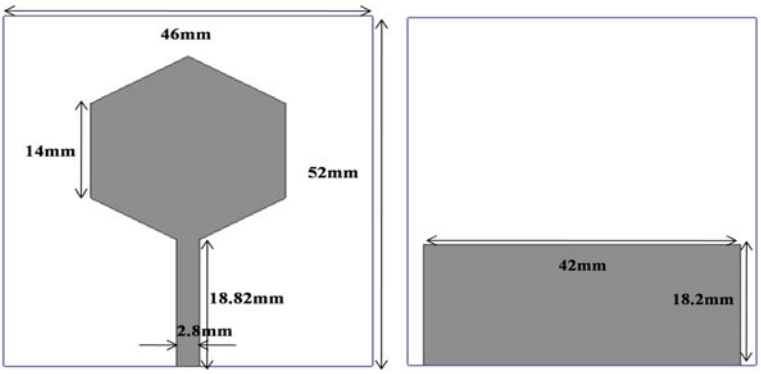


Fig. 1 *Hexagonal boundary* patch antenna design with dimensions

patch antenna dimension is 14 mm, length of the substrate is 46 mm, the width of the substrate is 52 mm, the length of the ground is 42, the width of the ground is 18.2, feed length is 18.82 mm, and width of the feed are 2.8 mm.

From the simulations results, the gain is 5.76 dB, return loss below −10 dB from 2 to 13.5 GHz; the VSWR is 1–2 from 2 to 13.5 GHz. To study the impact of slots on the gain, various slots like circle, square, triangle and hexagon are considered.

2.1 Hexagonal Boundary Patch Antenna with Circular Slot

Return loss is a measure of the effectiveness of power delivered from a transmission line to a load such as an antenna. It is the degree of mismatch between the incident and reflected power in the traveling waves. The return loss for hexagon patch antenna with hexagon slot is shown in Fig. 2. The return loss is below −10 dB from 2 to 13.3 GHz. The VSWR is basically a measure of the impedance mismatch between the transmitters and antenna. The higher the VSWR, the greater is the mismatch. The minimum VSWR which corresponds to a perfect match is unity. For practical applications, it should be between 1 and 2. Gain is the power transmitted per unit solid angle. The gain of the hexagonal patch antenna with the circular slot is shown in Fig. 7. The peak gain observed for this antenna is 5.75 dB.

2.2 Hexagonal Boundary Patch Antenna with Square Slot

The return loss plot for square slot is shown in Fig. 3. The return loss is below −10 dB from 2 to 6.4 GHz and from 6.7 to 13.3 GHz. The peak gain is 5.864 dB.

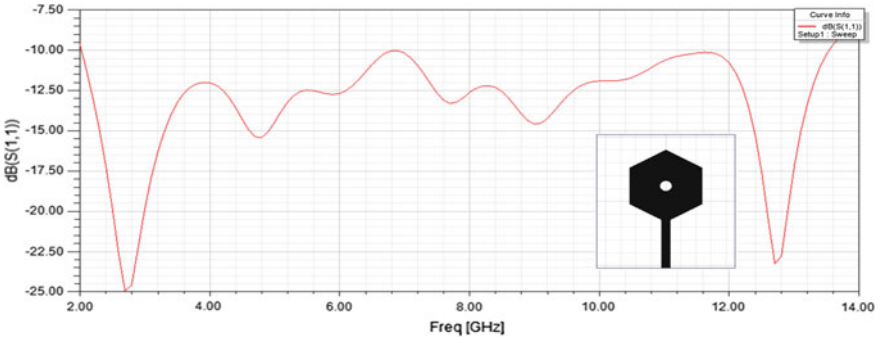


Fig. 2 Return loss for *hexagonal boundary* patch with *circular slot*

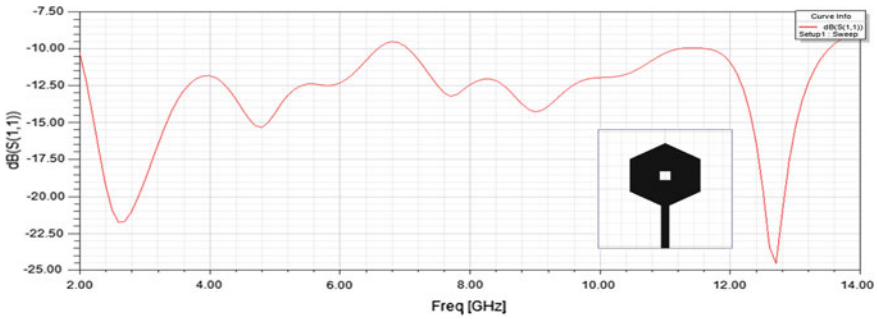


Fig. 3 Return loss for *hexagonal boundary* patch with *square slot*

2.3 *Hexagonal Boundary Patch Antenna with Triangular Slot*

The return loss plot is shown in Fig. 4 for triangular slot on hexagonal boundary patch antenna. The return loss is below −10 dB from 2 to 13.5 GHz. The peak gain obtained is 6.45 dB.

2.4 *Hexagonal Boundary Patch Antenna with Hexagonal Slot*

The observed return loss plot for hexagonal slot on HPA is shown in Fig. 5. The return loss is below −10 dB from 2 to 13.5 GHz. The peak gain obtained is 6.8 dB.

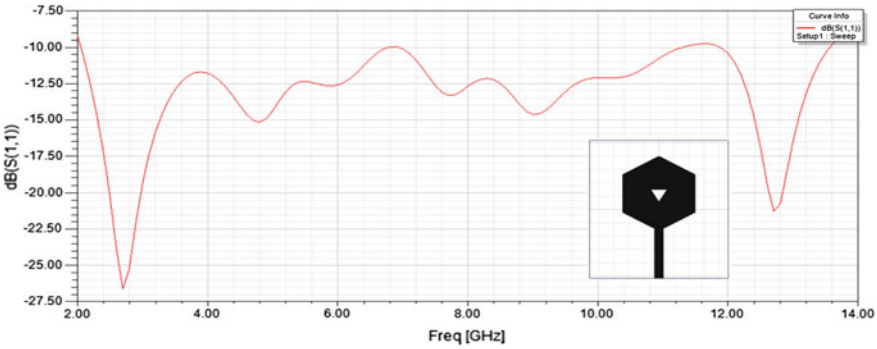


Fig. 4 Return loss for *hexagonal boundary* patch with *triangular slot*

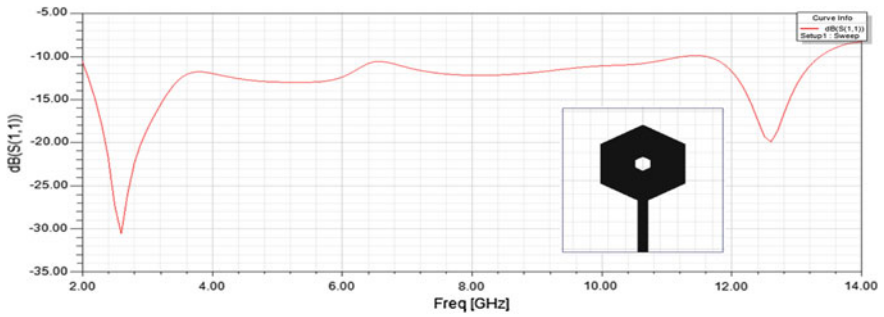


Fig. 5 Return loss for *hexagonal boundary* patch with *hexagonal slot*

2.5 *Comparison and Discussion of Simulation Results*

The comparative analysis is presented in Figs. 6, 7 and Tables 1, 2. Circular, square, triangle and hexagonal slots on the hexagonal patch are considered for analysis. The VSWR obtained from Fig. 6 is below 2 over the entire operating band of 2–13.5 GHz. It is evident from the results of a hexagonal patch antenna with and without slots; the gain obtained without slot is 5.70 dB, whereas with different slots the gain is increased significantly. It is observed that hexagonal slot in the hexagonal patch antenna has the highest peak gain of 6.8 dB. Hence the hexagonal patch antenna with hexagon slot is opted for fabrication.

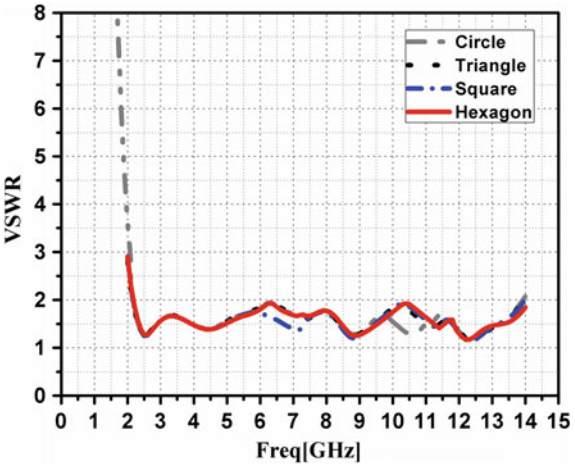


Fig. 6 Comparison of VSWR versus frequency for proposed antenna with different slots

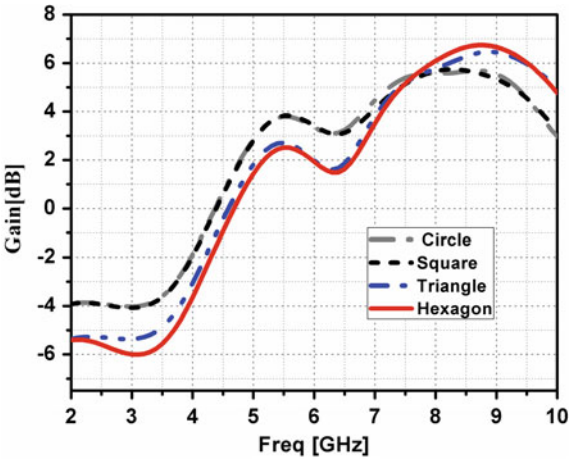


Fig. 7 Comparison of gain versus frequency for proposed antenna with different slots

Table 1 Effect of different shapes of slots on hexagonal patch antenna

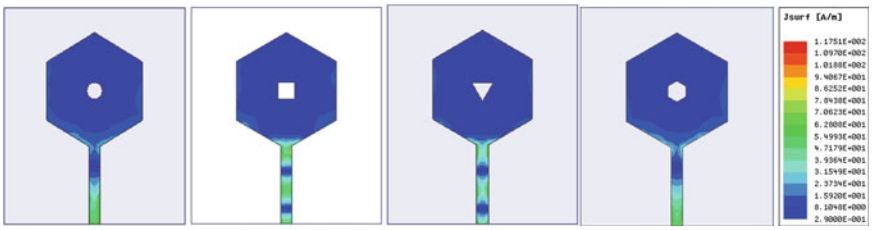
Type of slot	Operating frequency	Gain (dB)
Circle	2–13.3 GHz	5.758
Square	2–6.4 GHz and 6.7–13.3 GHz	5.864
Triangle	2–13.5 GHz	6.452
Hexagon	2–13.5 GHz	6.8

Table 2 Comparison of hexagonal patch antenna without slot and with slot

Parameters	HPA without slot	Proposed HPA with slot
Gain in dB	5.70	6.8
Operating frequency	2–13.5 GHz	2–13.5 GHz
VSWR	2–13.5 GHz	2–13.5 GHz

2.6 Surface Current Distribution for Different Slots

The surface current distribution of hexagonal boundary patch antenna for different slots at the first resonant frequency of 2.58 GHz is shown in Fig. 8.



(a) Circle Slot (b) Square Slot (c) Triangle Slot (d) Hexagon Slot

Fig. 8 Surface current distribution for different slots

3 Fabricated Antenna and Experimental Results

The fabricated structure of hexagon patch antenna with hexagon slot and measurement setup is shown in Fig. 9. The measured return loss and VSWR are presented in Figs. 10 and 11. Vector network analyzer (E5071C) is used for practical measurements.

From the following Table 3, it is observed that simulated and measured results of return loss, VSWR and respective resonant frequencies are in close agreement so that the gain could also be close to the simulated result. The deviations in simulated and practical results are due to open air measurement of the antenna using VNA.

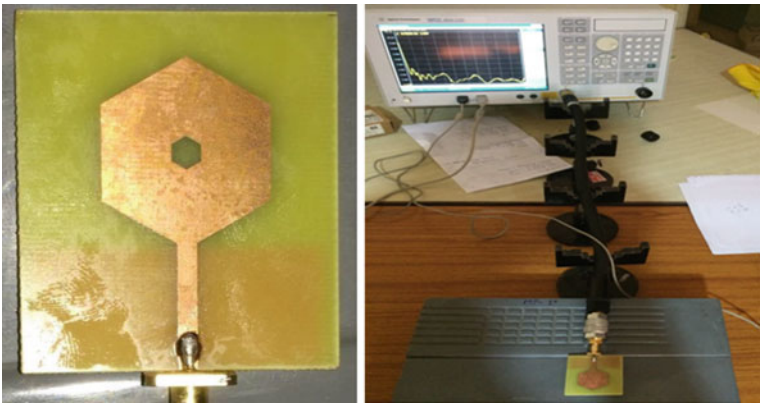


Fig. 9 Fabricated structure and experimental setup of the Antenna

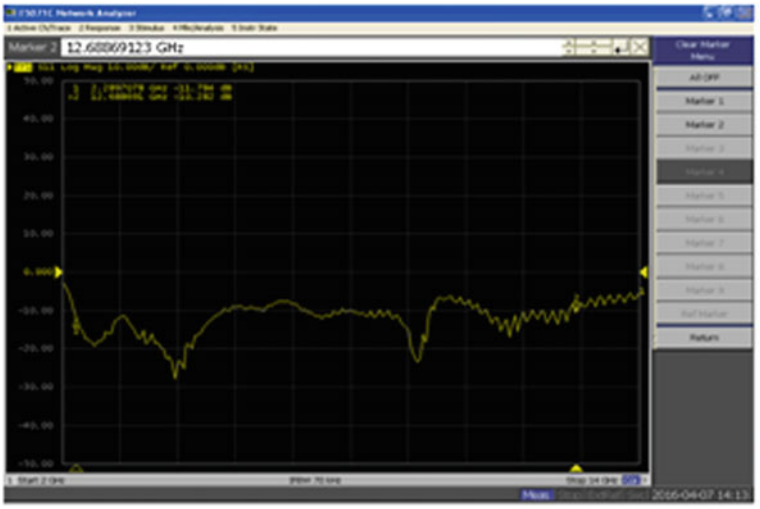


Fig. 10 Measured return loss for *hexagonal boundary* patch with *hexagonal slot*

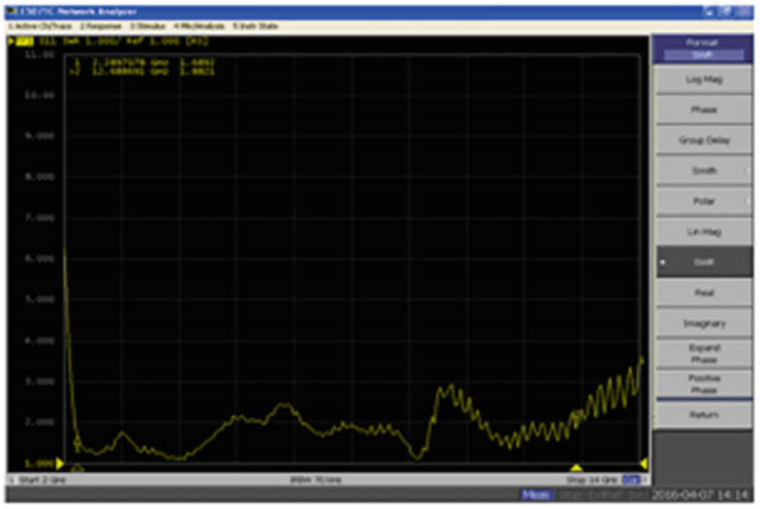


Fig. 11 Measured VSWR for *hexagonal boundary* patch with *hexagonal slot*

Table 3 Comparison of simulated and practical results

Parameters	Simulation results	Practical results
Operating Frequency	2–13.5 GHz	2–13.5 GHz
Return Loss	−30 dB at 2.5 GHz	−20 dB at 2.5 GHz
VSWR	1.05 at 2.5 GHz	1.25 at 2.5 GHz

4 Conclusions

Hexagonal patch antenna with different slots has been successfully designed in HFSS. It is evident from the results that hexagonal patch with hexagonal slot has a higher gain of 6.8 dB compared to other types of slots presented. The hexagonal slot-based hexagonal boundary patch is fabricated and the practical results obtained are in close agreement with simulation results. With suitable slots on patch antennas, gain can be enhanced.

References

1. Shinde PN, Shinde JP. The design of compact pentagonal slot antenna with bandwidth enhancement for multiband wireless applications. Int J Electron Commun (AEÜ) (2015), http://dx.doi.org/10.1016/j.aeue.2015.07.001.
2. Constantine A. Balanis, "Antenna Theory Analysis and Design," Third Edition, Wiley Publication, 2005.
3. Li P, Liang J, Chen X. "Study of printed elliptical/circular slot antenna for ultrawideband applications", IEEE Transactions Antennas and Propagation 2006;54(6):1670–2.
4. Ramesh Garg, PrakashBhartia, InderBahl, ApisakIttipiboon,"Microstrip Antenna Design Handbook," Artech HousePublications, Boston, London.
5. Eskandari H, Booket MR, Kamyab M, Veysi M. "Investigations on a class of wideband printed slot antenna", IEEE Antennas and Wireless Propagation Letters 2010;9:1221–4.
6. AchmadMunir, Guntur Petrus, Hardinusantara, "Multiple slots technique for bandwidth enhancement of microstrip rectangular patch antenna", in *proceedings of IEEE conference*, pp. 150–154, Oct 2013.
7. Mandal K, Sarkar PP.,"High gain wide-band U-shaped patch antennas with modified ground planes", IEEE Transactions Antennas and Propagation 2013;61:2279–82.
8. Guo YX, Luk KM, Lee KF, Chow YL,"Double U-slot rectangular patch antenna", Electronic Letters 1998;34:1805–6.
9. N.K.Darimireddy, R. Ramana Reddy, A. Mallikarjuna Prasad, "Design of Triple Layer Double U-Slot Patch Antenna for Wireless Applications," *Elsevier B.V-Journal of Applied Research and Technology*, (*JART-UNAM*), vol.13, pp. 526–534, Oct 2015. Available: http://www.sciencedirect.com/science/article/pii/S1665642315000577.
10. Naresh Kumar Darimireddy, R. Ramana Reddy, A. Mallikarjuna Prasad, "Performance Analysis of Frequency Dependent and Frequency Independent Microstrip Patch Antennas", in *Proceedings of ICMEET*, *Springer-Lecture Notes in Electrical Engineering* (*LNEE*) *Book Series*, vol. 372, GITAM University, Visakhapatnam, Dec 18–19, 2015.

Biconcave Lens Structured Patch Antenna with Circular Slot for Ku-Band Applications

Ribhu Abhusan Panda, Debasis Mishra and Harihar Panda

Abstract In this paper, the Rotman Lens structure has been modified and implemented as a patch resulting in a structure similar to biconcave lens. Earlier proposed antenna has been designed to operate at the frequency 15 GHz which lies in the Ku-band. By introducing a circular slot, the bandwidth has been increased which enables the antenna to operate over the entire frequency range of Ku-band of frequency range from 12 to 18 GHz used for satellite communication. FR4 Epoxy material has been chosen as the dielectric material for the substrate having dielectric constant 4.4 and the design and simulation has been done using HFSS software. To get the desired result, the optimization tool of HFSS software has been used by choosing a value for the radius of the circular slot that plays the vital role for bandwidth enhancement. Finally, the S-parameter, VSWR, directivity and gain of the proposed antenna were analyzed from the simulation result.

Keywords Rotman lens · Ku-band · Circular slot · HFSS · Directivity · Gain

R.A. Panda (✉) · D. Mishra
Department of Electronics and Telecommunication Engineering,
V.S.S. University of Technology, Burla, Odisha, India
e-mail: ribhupanda@gmail.com

D. Mishra
e-mail: debasisuce@gmail.com

H. Panda
Department of Physics, S.K.C.G. Autonomous College,
Paralakhemundi, Odisha, India
e-mail: harihar4458@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_8

1 Introduction

Many perturbations have been done in the Rotman lens structure that variedfrom designer to designer to achieve the desired goals. In the year 2015, the Rotman lens structure has been modified to create a perturbed elliptical patch for 50 GHz application [1]. Modification of Rotman lens structure as a beam forming lens antenna on high-resistivity silicon (HRS) wafer for IEEE 802.153c 60 GHz WPAN motivates to design of different variant of lens structure suitable for same type of applications [2]. This modification has been done by taking the equations which were developed by Rotman and Turner in the year 1963 [3]. But as the design parameters are very small due to the high operating frequency for the proposed patch structures so far. This results impediment in fabrication and testing. So in this paper, the frequency of operation is reduced and the Ku-band frequency range (12–18 GHz) has been taken into consideration which is used for satellite communication. Many techniques have been developed for enhancement of bandwidth such as using a thicker substrate, implementing the E-shaped patch [4] or implementing structures having more layers with parasitic patches [5, 6]. Rently, a circular patchantenna with reduced dimensions concentrically embedded in an annular ring with cross slotted ground plane [7]. To reduce the complexity, a rectangular slot antenna on a thin substrate has been proposed [8]. In this paper, a simple circular slot has been implemented in the patch which not only increases the bandwidth but also leads to a simple fabrication process reducing all the complexity.

2 Patch Geometry of the Proposed Antenna

2.1 Rotman Lens Equations and Proposed Modification

A prototype design of a lens is guided by the equations suggested by Rotman–Turner based on the geometry of the lens, shown in Fig. 1 [3]. As required to construct a lens structure, the contours of the lens on either side may be altered according to our requirements. Here, the left contour is in circular shape. Taking the help of Gent's equations [3] for calculation of optical path, coordinates of the antenna port on the right contour are derived. The ports are the points on the inner curve whose values can be calculated with reference to three focal points G, F_1 and F_2 [3]. Along with these, other parameters of the Rotman lens structure α, the internal scale angle, F, focal length and G, the distance of axial focal point from the origin are considered.

From Fig. 1, the two symmetrical off-axis focal points F_1 and $F_2$are symmetrical with reference to axis and have coordinates (−Fcos α, Fsin α) and (−Fcos α, −Fsin α). The axial focal point G has (−G,0), considering O as the origin. Defining $\eta = \frac{N}{F}$, $w = \frac{W - W0}{f}, x = \frac{X}{F}, y = \frac{Y}{F}, g = \frac{G}{F}, a0 = cos\,\alpha, b0 = sin\,\alpha$ which are normalized relative to focal length F, the final equations of the array curves derived are:

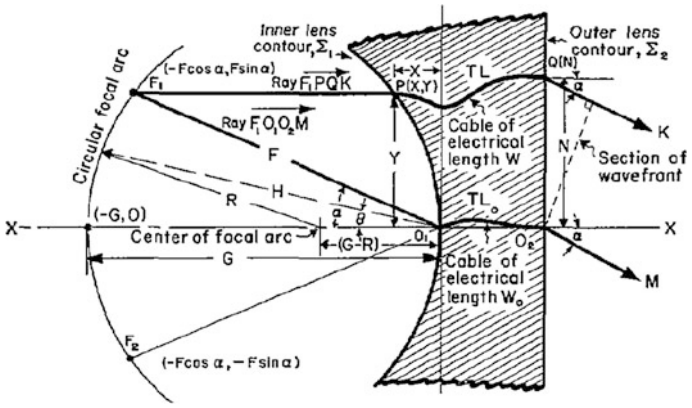


Fig. 1 Rotman lens geometry with coordinates [3]

$$y = \eta(1 - w) \tag{1}$$

$$x^2 + y^2 + 2a_0x = w^2 + b_0^2\eta^2 - 2w \tag{2}$$

$$x^2 + y^2 + 2gx = w^2 - 2gw \tag{3}$$

These equations lead to a quadratic equation

$$Aw^2 + Bw + C = 0 \tag{4}$$

From Eq. (3) it is obvious that the curve is the equation of a circle. For fixed values of design parameters α and g, w can be calculated as a function of η. Avoiding overall phase aberrations, the optimum value of g, ratio of on-axis to off-axis focal length G/F, is found from a simple relation given as a function of α [3] as

$$g = 1 + \left(\frac{\alpha 2}{2}\right) \tag{5}$$

2.2 Feasibility of Biconcave Patch

The modifications of the Rotman lens have been done in the year 2016 for log periodic implementation of the proposed patch having a similar structure of biconvex patch and waning crescent moon [9, 10]. In this paper, the patch structure is modified in order to have a structure like biconcave lens. The minimum distance between two arcs is taken as the same that of the wave length (λ = 20 mm)

corresponding to the operating frequency which is initially taken 15 GHz representing the central of the Ku-band. Then a circular slot has been implemented in the center of the patch. To get the optimum value of the radius of the slot for the desired result the optimization tool of HFSS has been used which is based on finite element method.

3 Design and Simulation of Biconcave Patch Antenna with Circular Slot

3.1 Material for Substrate with Appropriate Height

There is a relation between the frequency of operation and the dielectric constant [11–13]. The cutoff frequency (f_t) in GHz of a dielectric substrate as function of thickness is given by [14]

$$f_t = \frac{150}{h\pi}\left[\sqrt{\frac{2}{\varepsilon_r - 1}}tan^{-1}\varepsilon_r\right] \tag{6}$$

where "h" is thickness of substrate in millimeters. According to (6), the thickness of the substrate is selected to be h = 1.6 mm, which can support up to 20 GHz. FR4 epoxy material is used as the substrate material having a dielectric constant (ε_r) 4.4 which is widely available for the fabrication process.

3.2 Design of the Proposed Antenna

The proposed biconcave antenna has been designed using HFSS (high frequency structure simulator) which is one of the prominent software for all electromagnetic simulations uses finite element method. Microstrip line of (width = 3 mm) has been taken as the feed and a wave port has been assigned for excitation signal. The optimum values of the proposed antenna are as follows: Radius of the slot = 4.75 mm, Radius of the two arcs = 20 mm, substrate and ground plane dimension 80 mm × 80 mm, minimum width between the two arcs of biconcave patch = λ (20 mm) (Figs 2 and 3).

3.3 Results from Simulation of the Proposed Antenna

From the simulation results, it is found out that the resonant frequency of the biconcave patch antenna without slot is 16.28 GHz having a return loss of

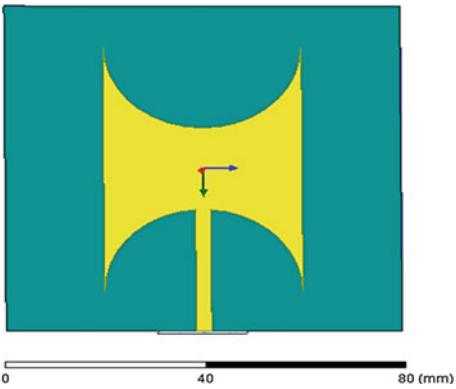


Fig. 2 Biconcave patch antenna without slot

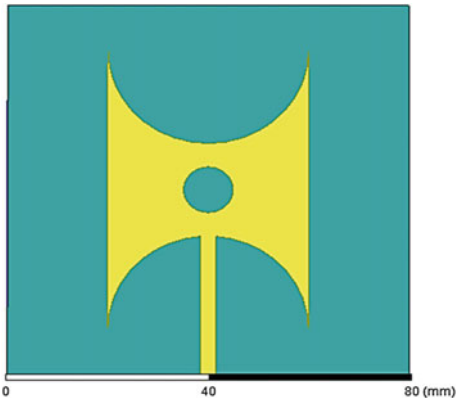


Fig. 3 Biconcave patch antenna with slot

−33.12 dB and the resonant frequency of the biconcave antenna with the slot having the optimum value radius (4.75 mm) is 15.29 GHz with the return loss −32.14 dB. Except this optimum value of the slot radius, no other value yields the return loss curve that includes the whole Ku-band. So the desired bandwidth can be achieved by taking the optimum value of the radius of the slot which is 4.75 mm. In similar way the VSWR, Gain and Directivity were also measured from the simulation result (Figs 4, 5, 6, 7, 8 and 9).

Voltage Wave Standing Ratio (VSWR) is also an important parameter to measure. For the designed biconcave patch antenna without slot at resonant frequency, the VSWR comes1.58 and with slot having the optimum radius value it comes 1.04 which is in good agreement with the desired value which is 1. It is shown in Fig. 10 (Figs. 11, 12, 13).

Figures 14 and 15 indicate the magnitude and vector field of the surface current distribution. From these results, it has been found that the current is flowing through the patch and having peak values at the edges of the patch (Table 1).

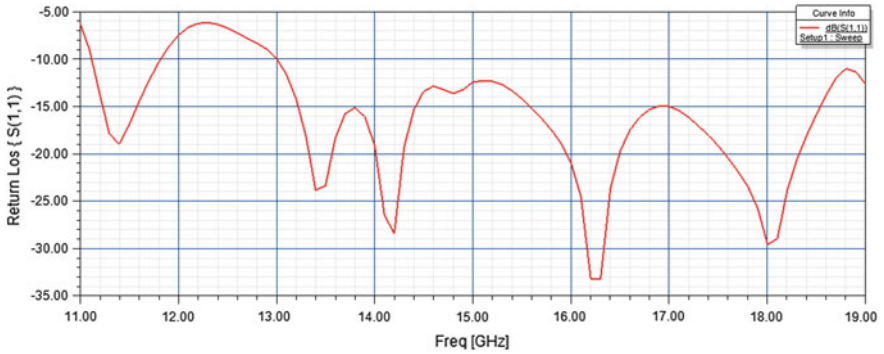


Fig. 4 S_{11} (return loss) of the biconcave patch without slot

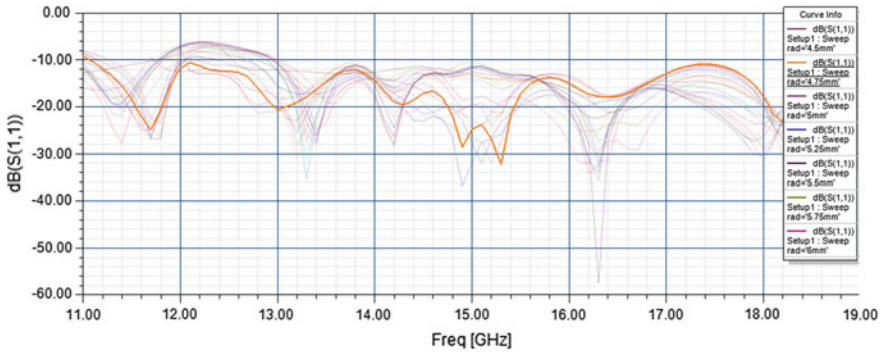


Fig. 5 S_{11} (return loss) of the biconcave patch without slot of radius of different values highlighting the curve resulted from the optimum value

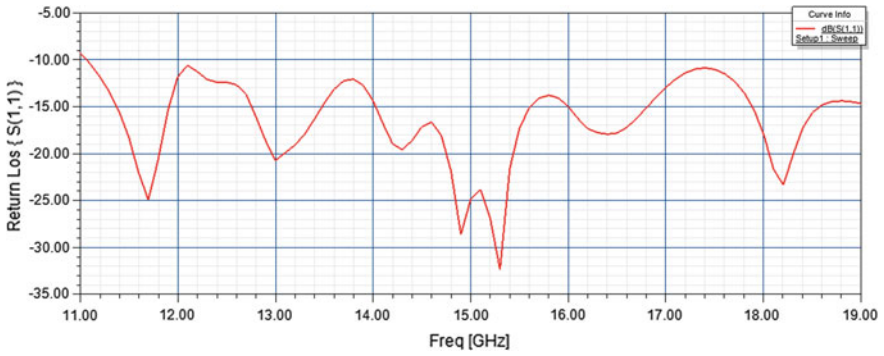


Fig. 6 S_{11} (return loss) of the biconcave patch with slot having the optimum value 4.75 mm

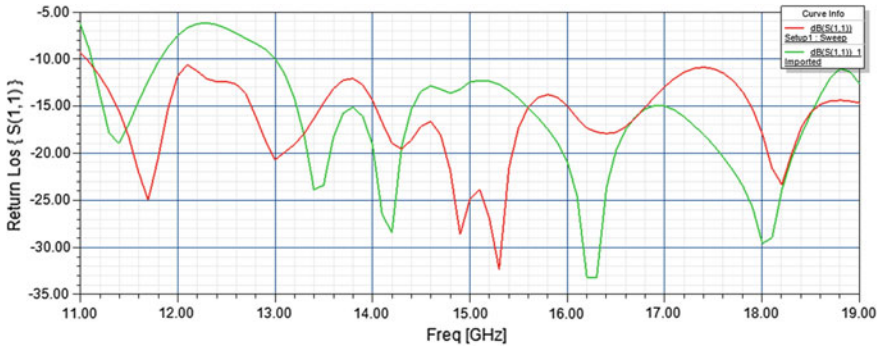


Fig. 7 Comparison of S_{11} (return loss) of the biconcave patch without slot (*green*) and with slot having the optimum value 4.75 mm (*red*)

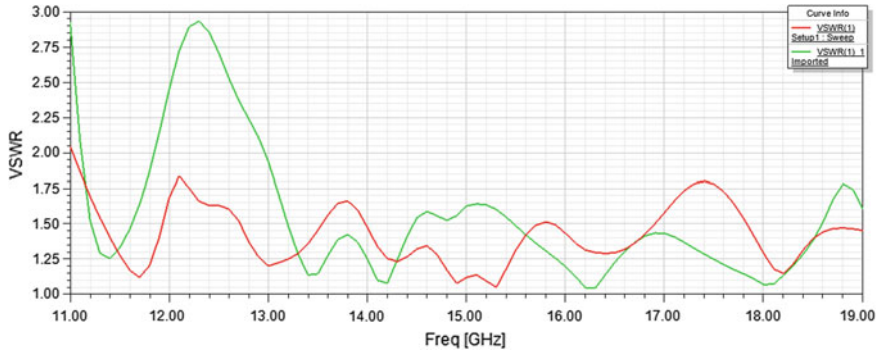
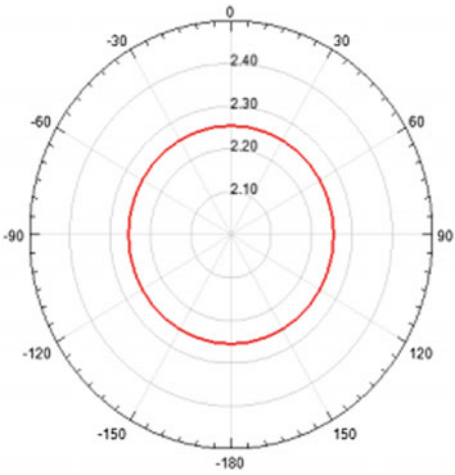


Fig. 8 Comparison of VSWR (voltage standing wave ratio) of the biconcave patch without slot (*green*) and with slot having the optimum value 4.75 mm (*red*)

Fig. 9 Peak gain of the proposed antenna



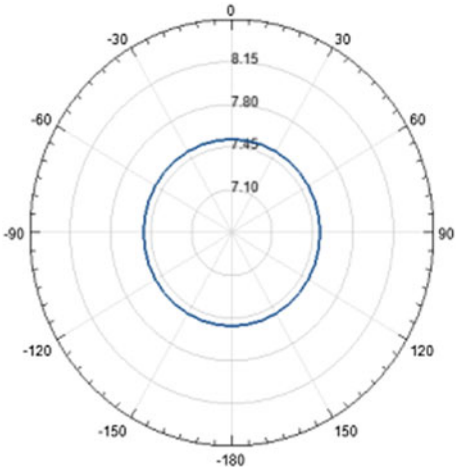


Fig. 10 Peak directivity of the proposed antenna

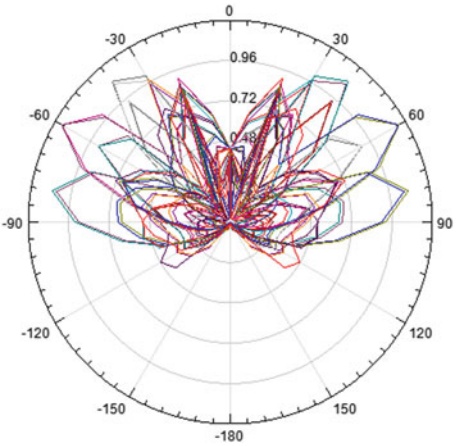


Fig. 11 2D radiation pattern of the proposed antenna at resonant frequency

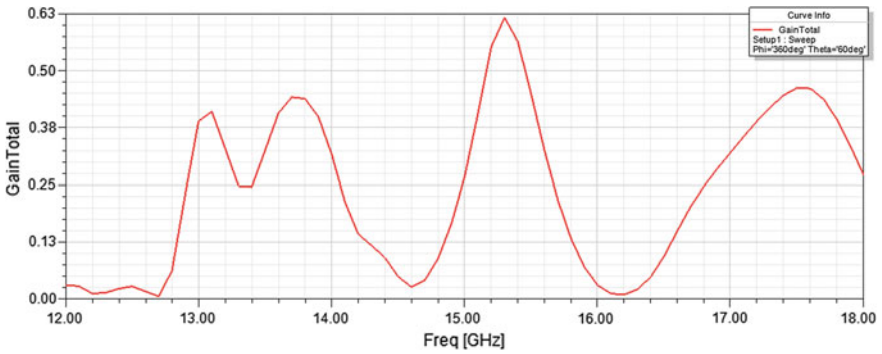


Fig. 12 Gain versus frequency plot of the proposed antenna

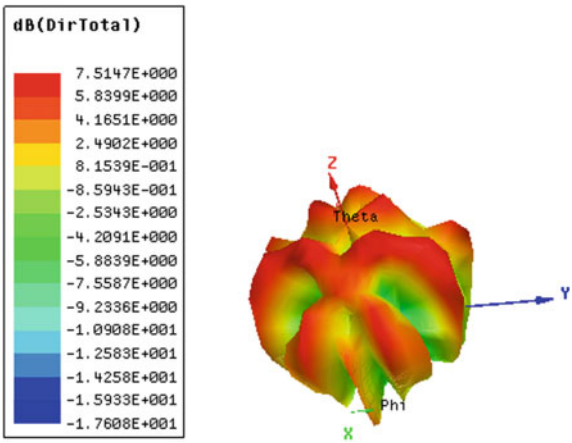


Fig. 13 3D radiation pattern

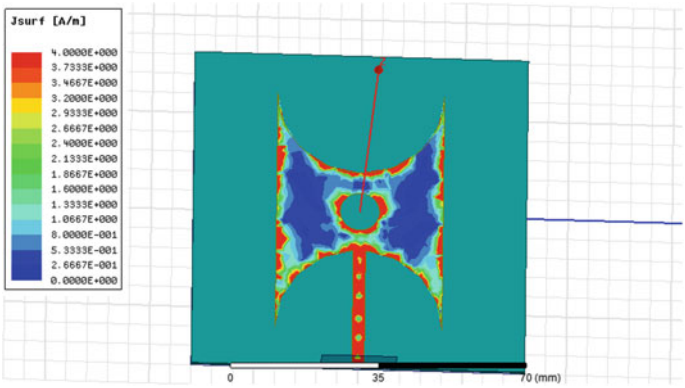


Fig. 14 Magnitude of surface current distribution

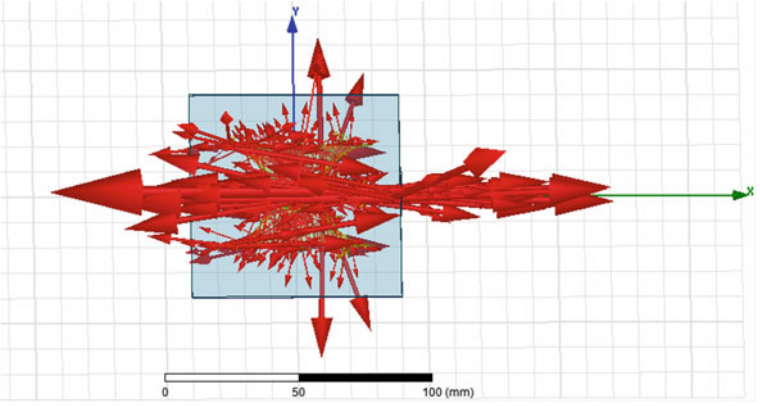


Fig. 15 Vector field of surface current distribution

Table 1 Comparison of parameters measured for biconcave patch without slot and with slot

Parameters measured	Without slot	With slot having radius 4.75 mm
Resonant frequency	16.28 GHz	15.29 GHz
VSWR	1.58	1.04
Directivity	6.8569 dB	7.5147 dB
Gain	0.778 dB	2.2546 dB
S_{11} (return loss)	−33.12	−32.14
Bandwidth	5000 MHz	6000 MHz

4 Conclusion

A biconcave patch antenna with circular slot has been designed for Ku-band application and simulated using HFSS. It has been found out that the biconcave patch antenna with the slot of optimum radius is having 1 GHz more bandwidth with high directivity and gain compared to the biconcave patch antenna without slot. It can be used for the Ku-band applications like satellite communications. Different gain enhancement techniques can be used with the proposed antenna to have a larger gain.

References

1. Ribhu Abhusan Panda, Suvendu Narayan Mishra, Debasis Mishra.: Perturbed Elliptical Patch Antenna Design for 50 GHz application. Lecture Notes in Electrical Engineering, Vol. 372. Springer India, pp 507–518, (2016)
2. Lee, W., Kim, J., Cho, C.S., Yoon, Y.J.: Beam forming Lens Antenna on a High Resistivity Silicon Wafer for 60 GHz WPAN. IEEE Transactions on Antennas and Propagation, Vol. 58. pp 706–713, (March 2010)
3. Rotman, W., Turner. R.: Wide-angle: Microwave Lens for Line Source Applications. IEEE Transactions on Antennas and Propagation, Vol. 11 pp 623–632, (1963)
4. Yikai Chen, Shiwen Yang, Zaiping Nie.: Bandwidth Enhancement Technique for low profile E shaped microstrip patch antenna. IEEE Transaction on Antennas Propagation, Vol 58, no 7, pp 2242–2247, (July 2010)
5. Gh Rafi, Shafai. L.: Broadband microstrip patch antenna with V-slot. IEE Proc. Microwave Antennas Propagation, Vol. 151, no. 5. pp 435–440, (2004)
6. J-H. Lu: Bandwidth enhancement design of single-layer slotted circular microstrip antennas. IEEE Transaction on Antennas Propagation, Vol. 51 no 5, pp 1126–1129, (2003)
7. XLBao, MJAmmann.: Compact annular-ring embedded circular patch antenna with cross-slot ground plane for circular polarisation. Electron Lett, Vol 42, no 4. pp 192–193, (February 2006)
8. Xu-bao Sun, Mao-yong Cao, Jian-jun Hao, Yin-jing Guo.: A rectangular slot antenna with improved bandwidth. Elsevier, International Journal of Electronics and Communication (AEU), Vol 66, 465–466, (2012)
9. Ribhu Abhusan Panda, Harihar Panda and Debasis Mishra: Log-Periodic Implementation of Biconvex Patch Antenna. International Journal of Emerging research in Management and Technology, Vol. 5, Issue 3. pp 10–16, (March 2016)

10. Ribhu Abhusan Panda and Debasis Mishra: Log Periodic Waning Crescent Patch Antenna for X-band Applications. International Journal of Recent Scientific Research, Vol 7, Issue 3, pp 9483–9487, (March 2016)
11. Balanis. C. A.: Antenna Theory: Analysis and Design. 3rd ed. New York: Wiley ch.14, (2005)
12. Kraus, J. D, Marhefka. R. J., Khan. A. S.: Antennas for All Applications. 3rd ed. TMH, ch.14, (2006)
13. Pozar, D. M.: Microwave Engineering. 2nd ed. New York: Wiley ch. 1, (1998).
14. Gupta, K. C., Garg. R., Bahl. I., Bhartia. P.: Microstrip Lines and Slotlines. Norwood, MA: Artech House, ch. 2, (1996)

Developing a Novel Unattended Infant Detection System for Vehicles

Muhammad Faisal, Hong Lin, Mussarat Yasmin and Steven Lawrence Fernandes

Abstract Baby detection and monitoring system using real-time frames from camera is proposed in this paper. Broadly, the process of system is divided into two major phases: training and testing. In training phase, an SVM model is trained to classify a facial image as baby or adult. Five geometric features are extracted using the location of eyes, nose and mouth in the face detected. In testing phase, if a captured facial image is classified as baby the face is stored and after a pause of 2 min another facial image is captured and compared with the first one. Absolute Difference Measure and a threshold value of ten are used to check if both facial images are same or not. The proposed system was trained and tested on 80 images of both adults and babies to classify a face as adult or baby. For training, 56 images were used and system achieved 96.4% of correct classification rate. For testing, 24 images were used and system was able to achieve 95.8% of correct classification rate. The proposed system was also tested at real time to monitor the baby and it achieved an accuracy of 80%.

Keywords Face detection · SVM · Geometric features · Threshold · Classification

M. Faisal (✉) · M. Yasmin
Department of Computer Science, COMSATS Institute of Information Technology, Wah Cantt, Pakistan
e-mail: muhammadfaisalcs@gmail.com

M. Yasmin
e-mail: mussaratyasmin@comsats.edu.pk

H. Lin
Department of Computer Science and Engineering Technology, University of Houston Downtown, Houston, USA
e-mail: linh@uhd.edu

S.L. Fernandes
Department of Electronics & Communication Engineering, Sahyadri College of Engineering & Management, Mangalore, Karnataka, India
e-mail: steven.ac@sahyadri.edu.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*, Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_9

1 Introduction

Detection and monitoring of humans in dynamic scenes is one of the most popular and researched topics that lie under the umbrella of machine learning, computer vision and visual surveillance. In the last 10 years, this area of visual surveillance has received much attention. The intention is to design efficient and smart visual surveillance systems because traditional passive video surveillance systems have proved ineffective as it becomes difficult for human operators to monitor them when number of cameras exceeds human capabilities.

In today's world, the closed circuit television (CCTV) devices to capture and monitor human are becoming very common due to their affordability. But the man power to monitor the video footages captured by CCTV is very short and in some cases proves very expensive. One of the main reasons for poor monitoring in video surveillance systems is the human factors like fatigue. Another reason for the same problem of poor monitoring is that there is no interesting scene for a long time that catches their attention and as a result of this human operators feel boredom [1].

There exists a variety of applications of visual surveillance, some popular among these are traffic surveillance, security guards outside commercial and residential buildings, etc. [2]. Mainly, this paper focuses on the visual surveillance of babies, the proposed system will classify the captured images as an adult or baby and it will alarm if a single baby is captured twice within 2 min. The proposed system can be implemented at places where a baby should not be alone.

Age group classification is a sub-part of proposed work. The selection and extraction of facial features for age classification and estimation system is one of the key and important phases. The feature which has higher discrimination over other features can be categorized as a reliable feature. Generally, the facial features are categorized into: Wrinkle and Geometric-based features, also known as Surface-based and Shape-based features respectively. In this work, only geometric features were extracted because system only needs to classify two age groups, baby and adult. Wrinkle-based features are used to classify the adult age groups to further sub age groups like young, old, etc. [3].

Age group classification is carried out by a trained SVM (Support Vector Machine) classifier and if a captured facial image is classified as a baby, the facial image is saved. After a pause of 2 min another facial image is captured. If second image is also classified as baby, then both images are compared using Absolute Difference Measure and a threshold value 10 is used to compare whether both images are of same baby or not. If a baby remains in front of camera for 2 min, system generates a message "Baby is in Danger".

Following an Introduction section, Related work is summarized in Sect. 2 especially in the area of human age group classification. In Sect. 3, Proposed Methodology is described with the help of flow charts followed by results in Sect. 4. Lastly, the concluding part is covered in Sect. 5.

2 Related Work

A lot of work has been done in the area of age group classification. Kwon and Lobo [4] were the first ones to conduct age group classification. They extracted the geometric features, ratios of distances between mouth, eyes and nose, etc., and some wrinkle-based features. The wrinkle indices were used to classify adult facial images further into senior adults and young adults. Only 47 images were used in experiments and for the baby group correct classification rate was below 68%.

A long-term aging process of each person was modeled by Geng et al. [5] using a sequence of images of same person, the proposed method is known as AGES (Aging pattern Subspace). Geng et al. [5] method was challenged by Yan et al. [6], they proposed a regression method that considers patches and claimed that at different periods of life, a person's facial features could be similar.

A multi-task regression model is formulated by Zhang et al. [7], age estimation function was handled by one learning task. Active appearance models (AAMs) [8] is used by Lanitis et al. [9] to represent facial features as a combination of both appearance and shape features. To classify the different age groups neural network along with shortest distance classifier was employed. Guo et al. [10] tried to reduce the biologically inspired features (BIF) using principal component analysis (PCA) using both classification and regression.

Mostly, only two types of facial features have been used: geometric-based and wrinkle-based, also called shape-based and surface-based features. For example, a baby face is round and the distance between both eyes is larger than the distance between eyes and mouth. With the increase in age, the size of head bone also increases and the head becomes oval. The distance between both eyes becomes equal or smaller than the distance between the eyes and mouse [3]. In the presented work, only geometric features have been used because these features are good enough to classify baby and adult facial images [1].

3 Proposed Method

The proposed baby monitoring system is briefly discussed in this section. Mainly, the proposed system is comprised of two phases: Training and Testing as illustrated in Fig. 1. In first phase a model is trained to classify the captured images by camera as baby or adult, a kind of age group classification. To train the model, first images are loaded from the database (of both adults and babies). The preliminary step of training includes detection of face in the image using Viola Jones algorithm [11]. All the images are resized to same size of (256×256); the rationale of resizing is to avoid miscalculation in the values of bounding box of face because some images may have been taken from closer view and other from some distance.

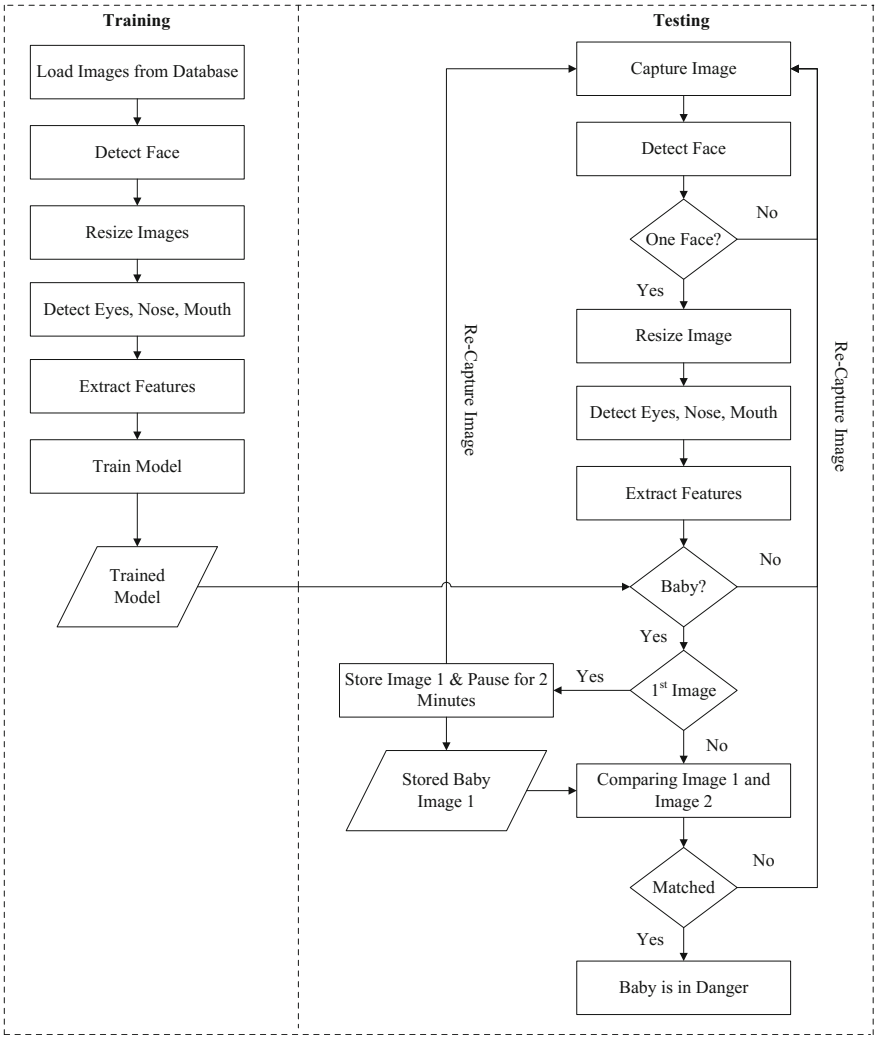


Fig. 1 Overview of proposed system

After the successful face detection, the search regions for mouth, nose and eyes are calculated as illustrated in Fig. 2. Then detection of eyes, nose and mouth is performed using the same Viola Jones algorithm [11]. To improve the accuracy of detection, eyes search area is restricted to upper half rectangular bounding box of face. Similarly, mouth is searched in the lower half rectangular bounding box of face and nose is searched in the area of half squared bounding of face. Figure 3 illustrates the search regions of nose, mouth and eyes respectively.

To classify the two age groups, i.e., adult and baby, geometric features were employed in the system. In the features extraction phase, five geometric features are

Fig. 2 Detection of face, eyes, mouth, nose, right eye, left eye of both adult and baby facial image

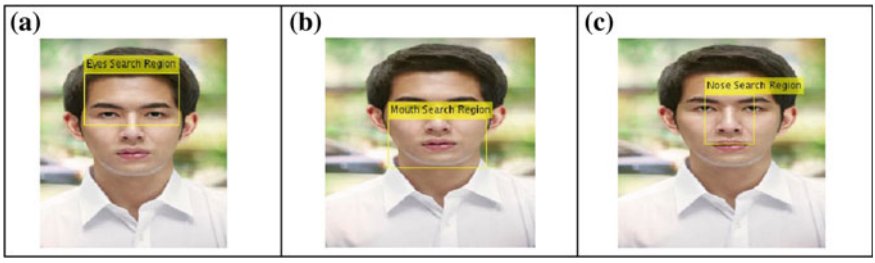


Fig. 3 Search regions for detection of eyes, mouth and nose

calculated: width of bounding box of face, distance of centers of left eye and right eye, distance of both eyes and mouth, distance of center of both eyes and nose, distance of center of mouth and nose. In the age group (adult and baby) classification phase, a two class Support Vector Machine (SVM) is used. The geometric features are fed to SVM model to classify the facial images as baby or adult.

In testing phase, the system keeps capturing the frames until it captures a single face. The captured image is resized to the same size of (256 $\times$ 256) to detect nose,

both eyes and mouth using Viola Jones Algorithm [11]. The same geometric features are calculated and sent to the trained model to classify the image as an adult or baby. If the image belongs to a baby the first image is stored and second image is captured after 2 min. If the same face is captured second time the system displays a message that baby is in danger otherwise it keeps capturing the images.

3.1 Features Extraction

For every classification problem, the key issue is to find the optimal and reliable feature set to achieve better results. Many facial properties change with the passage of time and increasing age [4].

3.1.1 Geometric Features

Distance between the primary features varies in different ages because head bones grow with an increase in age. In infanthood head bones are fully grown. Therefore, choosing geometric relations between primary features are more discriminating and reliable choice for classifying two age groups; baby and adult [3].

Head of a baby is similar to a circle. The distance between both eyes is larger than the distance between eyes and mouth. With an increase in age, the structure of head bones grows and head changes its shape from a circle to an oval. As a result, the distance between mouth and both eyes becomes larger [3].

As shown in Fig. 4, the distance from eyes to nose and distance from nose to mouth is almost equal and smaller than the same distances of an adult face. Therefore, five features have been extracted as discussed above in training section for recognizing babies.

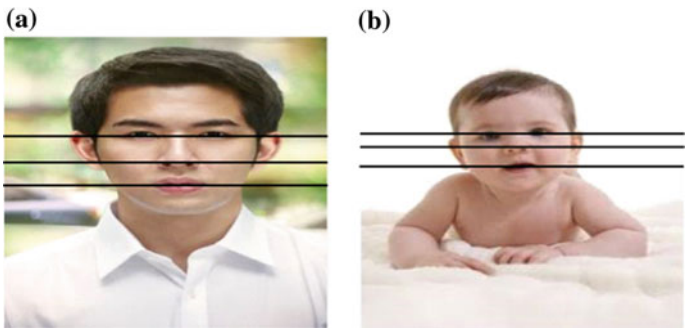


Fig. 4 **a** An adult face, **b** a baby face

The first feature is simply the width of bounding box of face detected in the image. The bounding box of a baby face is smaller than that of an adult as shown in Fig. 2. Second geometric feature is defined as:

$$\text{Dist\_Eyes} = \sqrt{(\text{CReye}_x - \text{CLeye}_x)^2 + (\text{CReye}_y - \text{CLeye}_y)^2}, \quad (1)$$

where $CReye_x$ is x coordinate and $CReye_y$ is y coordinate of center of right eye, $CLeye_x$ is x coordinate and $CLeye_y$ is y coordinate of center of left eye. *Dist_Eyes* represents distance from center of right eye to center of left eye center. Third geometric feature is defined as:

$$\text{Dist\_EyesMouth} = \sqrt{(\text{CEyes}_x - \text{CMouth}_x)^2 + (\text{CEyes}_y - \text{CMouth}_y)^2}, \quad (2)$$

where $CEyes_x$is x coordinate and $CEyes_y$ is y coordinate of center of bounding box of both eyes, $CMouth_x$ is x coordinate and $CMouth_y$ is y coordinate of center of mouth. *Dist_EyesMouth* represents distance from center of both eyes to mouth. Fourth geometric feature is defined as:

$$\text{Dist\_EyesNose} = \sqrt{(\text{CEyes}_x - \text{CNose}_x)^2 + (\text{CEyes}_y - \text{CNose}_y)^2}, \quad (3)$$

where $CEyes_x$ is x coordinate and $CEyes_y$ is y coordinate of center of bounding box of both eyes, $CNose_x$ is x coordinate and $CNose_y$ is y coordinate of center of nose. *Dist_EyesNose* is the distance from center of both eyes to nose. Fifth geometric feature is defined as:

$$\text{Dist\_MouthNose} = \sqrt{(\text{CMouth}_x - \text{CNose}_x)^2 + (\text{CMouth}_y - \text{CNose}_y)^2}, \quad (4)$$

where $CMouth_x$ is x coordinate and $CMouth_y$ is y coordinate of center of mouth, $CNose_x$ is x coordinate and $CNose_y$ is y coordinate of center of nose. *Dist_MouthNose* is the distance from center of mouth to nose.

Since the distance from eyes to nose and distance from nose to mouth of a baby face is almost equal and the distance from nose to eyes of an adult is greater than the distance from nose to mouth because of the growth of nose bone with increasing age, therefore, the geometric features discussed above are power discriminators.

4 Experimental Results

A dataset of facial images is collected from Internet including images of both adults and babies and split into two parts: training and testing. There are 80 RGB color facial images in the database, equally divided among two classes, i.e. adult and baby. The images were partitioned into testing and training sets using holdout of

Table 1 Average correct classification rate for training phase

Age group	Training images	Correctly classified	Accuracy	Overall accuracy
Baby	23	21	91.3%	96.4% (54/56)
Adult	33	33	100%	

Table 2 Average correct classification rate for testing phase

Age group	Testing images	Correctly classified	Accuracy	Overall accuracy
Baby	10	9	90%	95.8% (23/24)
Adult	14	14	100%	

Table 3 Real-time testing results

Total testing iterations	Correctly classified	Accuracy
20	16	80%

0.3, that means 30% for testing. An SVM with polynomial kernel function was employed for training and testing. The results were obtained using an average of ten times simulated results. Table 1 and Table 2, respectively, summarize the average classification results achieved.

Once the age group is classified as a baby, the facial features of that baby are stored for later recognition. When after 2 min' interval another baby is classified by SVM, the facial features set of both babies is compared using Absolute Distance Measure and a threshold is applied for the final decision of whether both images belong to same face or not. The absolute distance is calculated using Eq. 5 and the final decision of whether the facial images are same or not is taken using Eq. 6. The value of threshold (T) was set to 10, since a baby may move forward or backward in 2 min and detected bounding boxes of face, mouth, eyes and nose may get smaller or larger.

$$Difference = ABS(features_{face1} - features_{face2}) \tag{5}$$

$$Final\ \ Decision = \begin{cases} Baby & if\ \ Difference > T \\ Adult & if\ \ Difference \leq T \end{cases} \tag{6}$$

To obtain the results, the system is tested at real time using webcam 20 times. Sixteen times the system predicted the correct results that a same baby is captured twice. Table 3 summarizes the results.

5 Conclusion

In this paper, a baby detection and monitoring system using real-time frames from camera is proposed. The system efficiently classifies two age groups (baby and adult) using geometric features. In the training phase, geometric features using

locations of face, mouth, nose and eyes are extracted from images in the datasets. In testing phase, if a captured image is classified as baby it is stored and after a pause of 2 min another facial image is captured and compared with the stored baby facial image. The final decision was based on the absolute difference between features of both facial images and a threshold value of 10 is used to check if both images are same or not. Experimental results demonstrated that proposed method performs well at real time and achieved an accuracy of 80%.

References

1. Popoola, OP., Wang, K. Video-based abnormal human behavior recognition—a review. IEEE Transactions on Systems, Man, and Cybernetics, Part C (Applications and Reviews). 42, 865–78 (2012).
2. Hu, W., Tan, T., Wang, L., Maybank, S. A survey on visual surveillance of object motion and behaviors. IEEE Transactions on Systems, Man, and Cybernetics, Part C (Applications and Reviews). 34, 334–52 (2004).
3. Horng, W-B., Lee, C-P., Chen, C-W. Classification of age groups based on facial features. 淡江理工學刊. 4, 183–92 (2001).
4. Kwon, YH., da Vitoria Lobo, N. Age classification from facial images. Computer Vision and Image Understanding. 74, 1–21 (1999).
5. Geng, X., Zhou, Z-H., Smith-Miles, K. Automatic age estimation based on facial aging patterns. IEEE Transactions on pattern analysis and machine intelligence. 29, 2234–40 (2007).
6. Yan, S., Zhou, X., Liu, M., Hasegawa-Johnson, M., Huang, TS. Regression from patch-kernel. In: Computer Vision and Pattern Recognition, 2008 CVPR 2008 IEEE Conference on. 1–8. IEEE, (2008)
7. Zhang, Y., Yeung, D-Y. Multi-task warped gaussian process for personalized age estimation. In: Computer Vision and Pattern Recognition (CVPR), 2010 IEEE Conference on. 2622–9. IEEE, (2010)
8. Cootes, TF., Edwards, GJ., Taylor, CJ. Active appearance models. IEEE Transactions on pattern analysis and machine intelligence. 23, 681–5 (2001).
9. Lanitis, A., Draganova, C., Christodoulou, C. Comparing different classifiers for automatic age estimation. IEEE Transactions on Systems, Man, and Cybernetics, Part B (Cybernetics). 34, 621–8 (2004).
10. Mu, G., Guo, G., Fu, Y., Huang, TS. Human age estimation using bio-inspired features. In: Computer Vision and Pattern Recognition, 2009 CVPR 2009 IEEE Conference on. 112–9. IEEE, (2009)
11. Viola, P., Jones, M. Rapid object detection using a boosted cascade of simple features. In: Computer Vision and Pattern Recognition, 2001 CVPR 2001 Proceedings of the 2001 IEEE Computer Society Conference on. 1, I-511-I-8 vol. 1. IEEE, (2001)

A Strategic Node Placement and Communication Method for Energy Efficient Wireless Sensor Network

R.K. Krishna and B. Seetha Ramanjaneyulu

Abstract In the field of wireless sensor networks (WSNs) most of the research is in the direction of saving energy and increasing the lifetime of wireless Sensor Networks. One of the ways by which we can save energy is by placing the nodes in an intelligent manner. In this paper, we propose a novel node deployment scheme where the nodes are first placed in a circular form and then in the next round we deploy the nodes in the form of a pentagon called penta circular node placement or hexagon called hexa circular node placement so that the whole area from where information has to be collected will be covered with minimum number of nodes. The performance of this novel node placement strategy is tested for energy consumption and network lifetime. Simulation results indicate that the proposed method gives better performance in terms of Delay Packet Delivery ratio and Energy consumption in comparison with existing methods.

Keywords Penta circular node placement · Hexa circular node placement · Novel node deployment in WSN · Energy saving in WSN

1 Introduction

Clustering and routing are very important and vital issues in wireless sensor networks. It is known that appropriate clustering and routing techniques can be used to reduce energy consumption so that lifetime of networks will be enhanced. It is also known that in WSNs, most of the energy is consumed in sensing data, data processing and data communication. We can achieve the aim of reducing energy consumption by proper design of the network by taking these energy consumption related issues into consideration.

R.K. Krishna (✉) · B. Seetha Ramanjaneyulu
Department of ECE, Vignan University, Vadlamudi, Guntur, India
e-mail: rkrishna40@rediffmail.com

B. Seetha Ramanjaneyulu
e-mail: ramanbs@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_10

The work presented here mainly focus on finding of ways and means of reducing energy consumption by reducing the number of nodes and placing them intelligently so as to gather the maximum data. In the proposed method, it is tried to reduce the amount of energy consumed by the nodes by decreasing the number of nodes and placing them intelligently so that they are able to gather maximum amount of data. In this technique a novel approach is proposed for the deployment of nodes in the region.

2 Related Work

In [1] Aslam et al. proposed a cluster structured path planning algorithm which they have named as Hybrid Advance Distributed Centralized Clustering (HADCC) path planning energy efficient algorithm. In this method they have divided the whole network region into two physical levels. In the first physical level in the inner circle they have placed normal nodes with the base station at the centre. In the outer circle they have placed advanced heterogeneous nodes. The base station selects the cluster heads by considering factors such as initial energy, residual energy, energy consumption ratio and distance of nodes from the base station to select the cluster head. Cluster head performs the task of data transmission using CSMA MAC protocol.

In [2] Chen et al. proposed a Clustering technique in which they place the sink at the centre of the whole network. Then they have divided the network into many partitions. All the nodes have the same energy except the sink. According to them, the maximum number of cluster heads should be 5% of the total number of nodes. They have selected these heads on the basis of temporal head probability and communication cost. Once heads in the partitions are determined, the partitions are removed and nodes can join any head as a cluster depending on the nearest distance and communication takes place through the cluster heads and nodes.

In [3] Cheng et al. have proposed a High Energy first Clustering Technique in which they have placed nodes with high energy nearer to the base station and nodes with lower energy away from the base station. This is because they claim that the nodes nearer to the base station are more utilized and hence require more energy and consume more energy. Data transmission is done in the usual way that is Cluster head selection, Cluster formation and data communication. The Cluster head of each group sends the message inviting neighborhood sensor nodes to be a part of the group. The nodes then join to become part of the clusters. Each TDMA Schedule is then sent by the Cluster Head to all its members. All sensors then perform its sensing and processing and communication tasks. As usual, cluster heads collect this information and send it to the destination.

In [4], Dash et al. proposed a distributed algorithm to generate the hierarchical structure where each node has two parent nodes except the root node. The algorithm has four phases:

(1) Level discovery Phase.
(2) Energy discovery Phase.
(3) Parent Node Discovery Phase.
(4) Data transmission Phase.

In the level discovery phase, level of each node is decided depending on its distance from the sink. Sink is said to be at 0 level. Nodes that are one hop away will be Level 1 nodes that are two hops away from the sink will be level 2 and so on. After the level discovery phase, each node finds the remaining energy of its neighbor by sending a energy discovery packet that consists of node ID level number and remaining energy. On the basis of this information, every node stores the information of its two neighbors of the same level and information of two neighboring nodes from its immediate lower level. After this process is over then in the third Phase the nodes describe themselves as active or inactive for future. If the node's remaining energy is higher than its neighbor, it declares itself as active. Once it is declared as active, it selects two parent nodes from its neighbor. All the inactive nodes go to sleep mode and active nodes take part in data transmission. In the data transmission phase each node may transmit the sensed data to the sink through some active nodes or the parent nodes. The advantage of keeping two parents is that we get a multipath from the source to sink.

The focus of [5] by Delaney et al. was to develop a good route stability framework where metrics that are presently used are modified to discover routes so that more stability is achieved. The main concept here is the use of the technique of neighborhood heuristics where they combine sensors routing metric with those of the neighbors to find the quality of route being currently used and the quality of routing options that are available. By using this information, good quality routes can be found out and utilized so that stability may be maintained. The neighborhood Heuristics Mechanism is thus used for selecting the best route amongst the multiple routing options that are available for data forwarding thereby improving the efficiency of data communications.

Clustering is generally considered as one of the best methods for energy conservation techniques. In a clustered WSN generally Cluster heads (CHs) near the sink bear the maximum responsibility of data forwarding compared with the CHs that are far away from the sink. This results in an energy hole problem. Ghosal and Halder in [6] propose a routing-aware optimal clustering strategy for improving efficiency of WSNs. They have used Archimedes Spiral for deployment of nodes. A spiral is a curve which starts from the central point and moves progressively away as it revolves around the point. An Archimedes spiral is a continuous spiral and distance between two successive circular turns can be computed. One more feature of Archimedes spiral is that the distance between successive circular turns is constant. Therefore the nodes can be uniformly placed at uniform distance. The Archimedes Spiral is a continuous curve. This curve has to be transformed into a discrete form if we have to locate the nodes at discrete locations.

Guzman-Medina et al. in [7] proposed to use more of high energy nodes and less number of low energy nodes to keep the total number of high energy nodes higher

as compared to the low energy nodes in a wireless sensor network. They also proposed the use of on/off periods where since many nodes have different off duty modes and are capable of turning on and off the sensor nodes. This will result in saving of lot of energy. They propose that nodes with less residual energy will be turned off for longer times as compared to nodes with high energy so that the lifetime of the whole network will increase.

In [8] Jin-Shyan Lee have proposed a Clustering Method wherein nodes are semi-distributed. In this technique they have used hybrid centralized gridding technique for upper level selection of Cluster head whereas for selection of lower level head selection they have used distributed Clustering. In this method they have classified the nodes into four layers from top to bottom as:

(1) Base Station.
(2) Layer 2 Grid Head.
(3) Layer 2 Cluster Head.
(4) Layer 0 Sensor Nodes.

The information that is sensed is first transmitted from Layer 0 to Layer 1 Cluster head and then to Layer 2 Grid Head and finally to Layer 3 Base station.

Prerna and Sanjay Kumar in [9] proposed a new routing algorithm for WSNs. This new routing Algorithm uses both static Clustering Technique concepts and dynamic Cluster head selection method. This method divides the entire network into many fixed regions. They divide the network into static Clusters based on the communication range of the node as the basis behind dividing the network. Sink as usual is placed at the centre of the network. Thus after Cluster formation is done the Cluster head is selected based on the selection parameters such as number of surrounding nodes, the energy left in the nodes and the distance of the node from the base station. A node with maximum weight is selected as Cluster head for one round and node with second maximum weight is selected for the second round and so on. Finally communication takes place as usual through the Cluster heads.

Noor Zaman et al. in [10] also proposed a novel routing protocol which saves lot of energy and can significantly improve the energy efficiency of wireless sensor networks. They have named it as Position Responsive Routing Protocol (PRRP). PRRP protocol shows significant improvement in the efficiency of Wireless Sensor Networks. This is achieved by increasing the life of the battery of individual nodes. In this protocol the area is divided into equal squares. Grid format technique is used. Nodes are distributed randomly and base station is located at the centre. As we know the energy of the sensor nodes cannot be recharged. But the advantage of this technique is that the sensor nodes are aware of their locations. In this protocol they propose to vary the transmission power. Because nodes will be aware of their location and sink, a lot of energy will be saved. This is because energy is not required to search for the initial location of the nodes. They also propose to use energy of all nodes to the last limit and allow all nodes to participate in communication. Also they propose to decrease the distance between gateway nodes and sink so as to decrease the energy consumption.

In this work, it is tried to overcome the shortcomings of the existing methods. In [1], it proposes to divide the whole network to two levels. This method has its own advantages such as energy balancing and improvement in lifetime and also covers a large area of network but at the cost of increasing the number of nodes. We propose a method that not only cover the whole region but also can access information at points deeper and also covers the large area with less number of nodes which not only gives better results but is also energy efficient.

In [2], it proposes a clustering technique in which the network is divided into several clusters and therefore numerous clusters are formed and numerous Cluster heads are required and the transmission has to take place through small hops. In our method we form only two clusters one outer cluster consisting of nodes in hexagon or pentagon and another cluster consisting of nodes in the circle and the select two cluster heads for the two clusters based on the nodes with highest energy thus providing a more energy efficient network.

Cheng et al. [3], proposes to keep the nodes with high energy nearer to the base station as they mention that these nodes will require more energy than the nodes which are far away. Hence the nodes with less amount of energy are placed away from the network. Here if outer nodes have to be more frequently used there is a possibility of some nodes dying earlier as compared to others and networks will have to use some other nodes for transmission. In our method, we propose to distribute the nodes with highest energy in both the clusters with other nodes also placed in equal measure in both the clusters and the node which has the maximum energy in the cluster will be the cluster head. Transmission takes place from CH of one cluster to CH of another cluster to the base station and so on. The advantage of this placement is energy balancing of the network and nodes with higher energy are used more frequently and nodes with less energy are used less frequently and if at all the network dies all the nodes will die simultaneously. Thus the longevity of whole network increases.

Ghosal and Halder [6], proposes deployment of nodes at discrete places using Archimedes principle and this is done as per the mathematical principles. We propose to place the tip of the hexagon or pentagon in the area where we require to access the information and this position may be changed by us depending upon the area that needs to be accessed more. This work also makes use of the good features of some existing methods such as placing the base station at the centre, energy distribution of nodes equally and an ideal clustering technique where Cluster heads are selected depending on the highest energy.

3 Proposed Work

Strategic node placement is the mechanism proposed in this work. We propose the deployment of nodes in a circular fashion so that the whole region is uniformly covered by placing nodes in uniform distances. In the outer region we propose discrete placement of nodes in form of a pentagon shown in Fig. 2 (penta-circular

node placement) or hexagon as shown in Fig. 3 (Hexa-circular Node Placement), so that number of nodes used may be reduced and regions that cannot be covered in a circular fashion and deeply situated regions will also be covered using less of nodes and uniformity will also be maintained. Normal node placement without these methods is shown in Fig. 1.

The base station will be at the centre and the nodes will be divided into two regions. The Cluster heads are selected based on various criteria. Here we select the cluster head based on maximum energy of a Cluster and the node with highest energy is selected as Cluster head and communication is done through them only. This method not only improves the lifetime of the whole network but also covers the whole area where monitoring is to be done and the number of nodes is also reduced and uniformity of network is also achieved. Also we can turn off the nodes which are not participating in the communication so as to save energy.

The proposed method consists of the following steps. At first the Nodes are placed in a circular fashion. Then Nodes are placed in form of a pentagon or hexagon. A node with highest energy is selected as Cluster head of the nodes placed in a circular fashion. A node with highest energy from amongst nodes placed on a

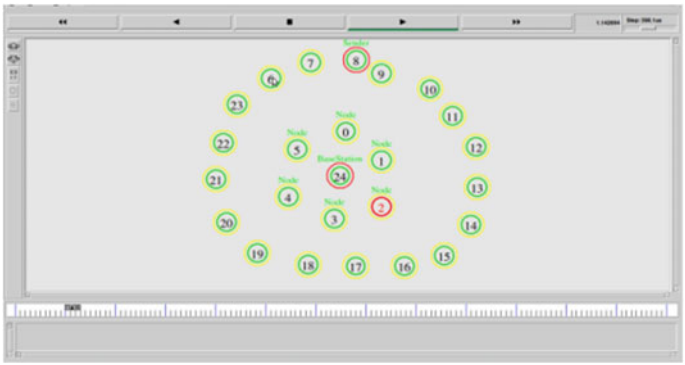


Fig. 1 Two circle node placement

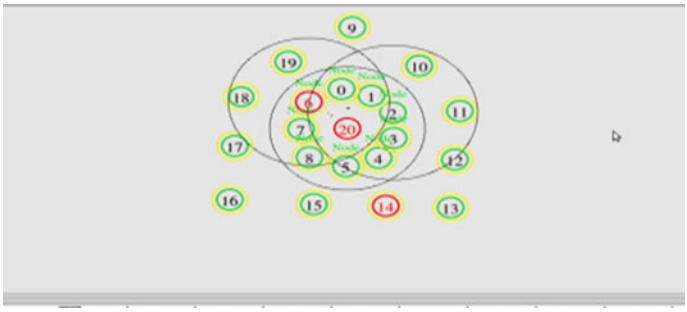


Fig. 2 Penta circular node placement

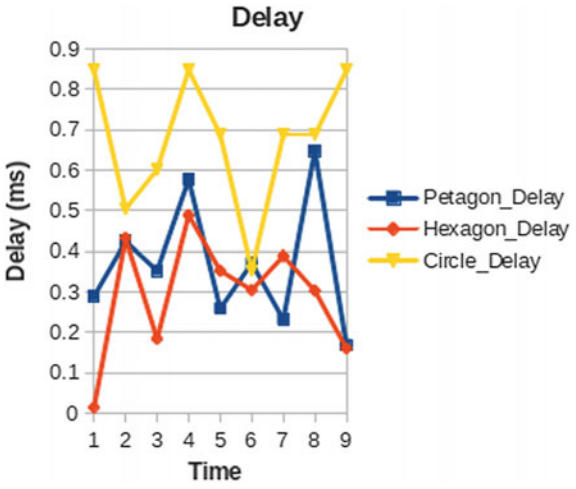
pentagon or hexagon will be selected as its cluster head of the outer cluster. If the sender is far from the base station, then it will send the data to the Cluster head on the Pentagon or hexagon. The data is then transmitted to the Cluster head of the Circle. The data is then transmitted from the Cluster head to the base station. If the distance from the node to the Cluster head is large, then transfer of information takes place through an intermediate node. This scenario and methodology are simulated using NS2 simulator and the quantities of energy consumed, delay occurred and ratio of Packet delivery are recorded.

4 Results

The simulation results for energy, delay and Packet delivery ratio are obtained for the proposed node placement method. These results are compared with the existing technique. Performance comparisons are shown in Figs. 4, 5 and 6.

Fig. 3 Hexa circular node placement

Fig. 4 Delay comparisons



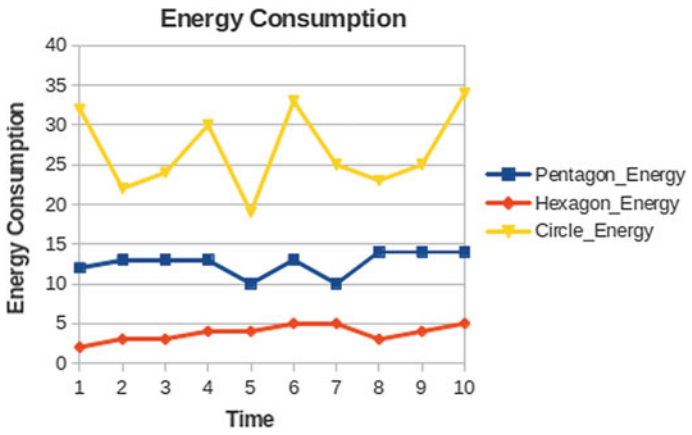


Fig. 5 Energy consumption comparisons

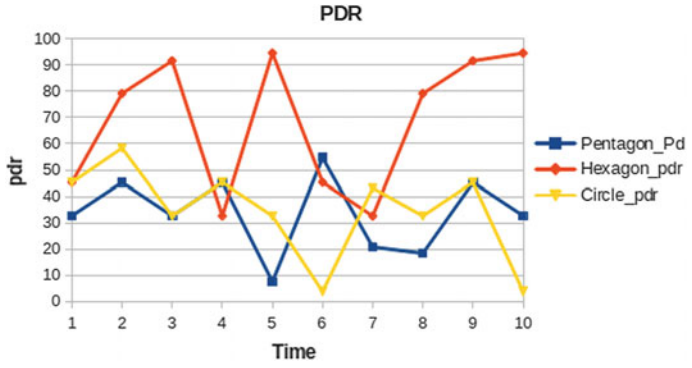


Fig. 6 Packet delivery ratio comparisons

Figure 4 is the delay comparison graph of the proposed technique with the existing technique. It can be observed that delay is minimum using the hexa circular technique. It is reduced by 50%. In Fig. 5, the Energy consumption graph is plotted which shows that energy consumed is minimum in the hexa circular technique. It is reduced to one fourth of its previous value. In Fig. 6, we have plotted the graph for packet delivery ratio which shows that the improvement with the proposed method is almost the double compared to the previous.

5 Conclusions

It is observed that the proposed pentagon and hexagon deployments offer lesser packet delays, better energy savings and higher packet delivery ratios. Hexagon method reduces the delay substantially by up to 50%. Energy consumption is reduced considerably to about 25% when compared to circular method. Packet delivery ratios are increased substantially. Hence the proposed deployment methods may help to improve the network in these aspects.

References

1. Muhammad Aslam, Ehsan Ullahmunir, Muhammad Bilal, Muhamad Asad, Asad li, Tauseef Shah, Syed Bilal: HADCC.: Hybrid Advanced Distributed And Centralized Clustering Path Planning Algorithm For WSNs, IEEE 28th International Conference On Networking And Applications pp 657–664, (2014)
2. Chen Chen, Xiaomin Liu, Hualin Qi, Liqiang Zhao, Zhiyuan Ren.: A Security Enhancement And Energy Saving Clustering Scheme. Smart Grid Sensor Network. Proceedings Of ICCT 848–855, (2015)
3. Bo-Chao Cheng, Hsi-Hsun Yeh, And Ping-Hai Hsu.: Advanced Information Schedulability Analysis For Hard Network Lifetime Wireless Sensor Networks With High Energy First Clustering. IEEE Transactions on Reliability, Vol. 60, No. 3, September 675–687, (2011)
4. Subhasis Dash, Satyasundar Mallick, Hansdah, R.C., Amulyaratna Swain.: A Distributed Approach To Construct Hierarchical Structure For Routing With Balanced Energy Consumption In WSNs. 29th International Conference On Advanced Information Networking And Applications 382–388, (2015)
5. Declan T. Delaney, Russell Higgs, Gregory M. P. O'Hare.: A Stable Routing Framework For Tree-Based Routing Structures In WSNs. IEEE Sensors Journal, Vol. 14, No. 10, October pp 3533–3547, (2014)
6. Amrita Ghosal, Subir Halder.: Lifetime Optimizing Clustering Structure Using Archimedes Spiral-Based Deployment In WSNs. IEEE Systems Journal, pp 1–10, (2015)
7. Carlos A. Guzman-Medina, Mario E. Rivero-Angeles, Izlian Y. Orea-Flores.: ON/OFF Protocol for the Life Extension Of Low Energy Level Nodes In Wireless Sensor Networks. 978-1-4799-7639-3/15/ IEEE (2015)
8. Jin-Shyan Lee, Tsung-Yi Kao.: An Improved Three-Layer Low-Energy Adaptive Clustering Hierarchy for Wireless Sensor Networks. DOI 10.1109/JIOT2530682. IEEE Internet of Things Journal, pp 1–8, (2016)
9. Prerna, Sanjay Kumar, Energy Efficient Clustering Algorithm For WSN.: 2nd International Conference On Signal Processing And Integrated Networks (SPIN) pp 990–993, (2015)
10. Noor Zaman,, Tung Jang Low, Turk Alghamdi: Enhancing Routing Energy Efficiency of Wireless Sensor Networks. ICACT Transactions On Advanced Communications Technology (TACT), Vol. 4, Issue 2, pp 587–594, (March 2015)

Gait-Based Person Recognition Including the Effect of Covariates

M. Hema, K. Babulu and N. Balaji

Abstract The gait is the emerging biometric technology, which is used for person authentication based on walking style of a person. Covariates play a very important role in gait recognition, which degrades the recognition accuracy. Covariates include View point, Clothes, Footwear, Surface type, Carried weight, Walk velocity, Time, Emotional state. Among these, we consider the variation of view-point and large intraclass variations like carrying and wearing conditions. Gait Energy Image (GEI) features are extracted from the binary silhouette images and perform the View Transformation Model (VTM), in order to recognize the person. In this paper, the experiments conducted on CASIA gait database, shows that the proposed algorithm is robust to view point and intraclass variations like carrying and wearing conditions.

Keywords Covariates · Feature extraction · Gait recognition · GEI · VTM

1 Introduction

Human gait is the most important biometric trait for person authentication. The biometric system mainly used to prevent the unauthorized access. Biometric resources such as face recognition, voice recognition, iris, fingerprints, palm prints, shoe prints and handwriting, are a subject of extensive research work, studied and employed in many applications. The advantage of gait as the biometric is that the gait of a human can be captured even from a great distance [1]. Compared to all the

M. Hema (✉) · N. Balaji
Department of ECE, JNTUK-UCEV, Vizianagaram, Andhra Pradesh, India
e-mail: hema.asrith@gmail.com

N. Balaji
e-mail: narayanamb@rediffmail.com

K. Babulu
Department of ECE, JNTUK-UCEK, Kakinada, Andhra Pradesh, India
e-mail: kapbbl@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_11

biometric technologies gait is non-contact one. Like other biometric technologies gait does not require the user cooperation and it is also fast, cheap and accurate.

There is a need for automation in applications such as security systems, crime investigation department and surveillance. Today, biometric is an effective tool for reliable person authentication. The motion vision's main purpose is to use surveillance when unexpected occurrences befall us.

The classification of gait recognition is done in various ways. Human motion and vision is one of a kind, recognition based on a wearable sensor, through sensor information from the floor of the motion are the other types. Wearable sensor systems require carrying the sensors and floor sensor system around that necessitates setting the sensors on the floor [2, 3]. The first kind is further divided, based on appearance and model parameters and appearance method is divided into two categories: they are spatiotemporal and state-space methods. Most researchers used appearance-based method compared to model-based method [4, 5].

In this paper, we consider the covariates carrying and wearing conditions as viewpoint [6–8]. GEI features are extracted from the silhouette image sequences and construct VTM for transforming the gait feature from probe viewing angle to the gallery viewing angle.

The organization of the remaining paper is given as follows. Section 2 describes the various steps involved in the proposed algorithm. The method of implementation is detailed in Sect. 3. Section 4 presents experiments regarding the CASIA database on which the proposed algorithm tested. Section 5 comprises the results and discussions. Finally, Sect. 6 concludes the paper.

2 Proposed Algorithm

We propose a View Transformation Model (VTM) by using Gait Energy Image. The proposed algorithm consists mainly of two parts, one is feature extraction and the other is Gait recognition by constructing View Transformation Model.

The various steps involved in the proposed algorithm are as described below.

(A) *Extraction of gait training and testing image sequences*

The gait training and testing image sequences are extracted from the video files.

(B) *Silhouette Extraction*

Silhouette image sequences [9] are extracted from the gait image sequences by using graph cut background subtraction method. Simply subtracting the original image from its background is nothing but silhouette image. Silhouette image sequences are represented by $B(p, q)$.

(C) *Gait period estimation*

While walking the person starts with one pose and coming back to the same pose is nothing but one gait cycle. Based on gait cycle, we estimate the gait period [10].

(D) *Feature Extraction*

In order to perform the gait recognition we have to extract the features. Here we select the GEI as the feature.

(E) *VTM Construction*

After extracting the gait feature, transforming those gait features from probe viewing angle to the set of gallery viewing angles. Here we look at the test subject viewing angle as the probe viewing angle and training subjects viewing angle is considered as gallery viewing angles.

(F) *Gait Similarity Measurement*

After transforming the probe viewing angle into the gallery viewing angle, then perform the gait similarity measurement by using L1 norm distance.

(G) *Recognition Rate*

The percentage of gait recognition rate indicates how much accurately the test subject matches with the train subjects in the database.

3 Implementation

In this section, it is discussed in detail, how the proposed algorithm implemented with appropriate mathematics. In general, human gait occurs in a periodic manner. A detection period helps in preserving the temporal information which reduces computational complexity and cost. Applying the methods illustrated in [9, 11] estimate the bounding box changes and the aspect ratio, which depends on the periodic alterations in human walk. These methods use GEI as the important gait parameter.

(A) *Feature Extraction*

By the periodic estimation of the GEI features gives the gait information in temporal and spatial domain. Silhouettes are obtained through background subtraction and the GEI is obtained. $B_{l,t}(p,q)$ is a binary silhouette in which the pixels are located at position (p, q). Each binary silhouette has $l(l=1,2,\ldots\ldots L)$ gait cycles. Each gait cycle has $t(t=1,2,\ldots T)$ frames. Silhouette normalization is performed along both vertical and horizontal directions for a fixed range. GEI of height M and width N represents is given by

$$f(p,q)=1/T\sum_{l=1}^{L}\sum_{t=1}^{T}B_{l,t}(p,q). \tag{1}$$

Here T represents total frames in one gait cycle. B represents the silhouette at t, p and q are the coordinates of the image. The 1-D feature vector is obtained by concatenating the value of each position in $B_{l,t}(p,q)$ along all consecutive rows and

columns which is represented by f_k^m, where k represents the kth observing angle and m represents the mth subject.

(B) *View Transformation Model*

The left-hand side matrix of Eq. (2) is called optimized gait representation matrix represented as F_K^M. Every row indicates the gait data under same observing angle from different subjects, whereas column represents same subject with different observing angles. Take a total of M subjects and K observing angles and constructs a View Transformation Model. Singular Value Decomposition is used for factorization [11] as specified below:

$$F_K^M = \begin{bmatrix} f_1^1 & \cdot & \cdot & \cdot & f_1^M \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ f_k^1 & \cdot & \cdot & \cdot & f_K^M \end{bmatrix} = R[z^1 \ldots\ldots\ldots\ldots z^M] = XYZ^T. \tag{2}$$

Here X and Z are orthogonal matrices with dimensions of $KN_f \times M, M \times M$ respectively. f_k^m with dimension $N_f \times 1$. S is a diagonal matrix with dimension M × M.has the singular values. $R = [R_1, \ldots, R_K]^T = XY$, here R_K is sub-matrix of XY and z^m is column vector.

The vector z^m represents the gait feature vector of mth subject for any observing angle. Under a specific observing angle R_K represents transforming matrix which is independent of subject. It helps in projecting a shared gait feature vector z to gait feature vector under specific angle k. From Eq. (2), for an optimized gait vector f_j^m from the mth subject with jth observing angle, the learned gait transformation of feature vectors from jth to ith observing angle is obtained as

$$t_{f_i^m} = R_i R_j^+ f_j^m. \tag{3}$$

Here, R_j^+ represents a pseudoinverse matrix.

(C) *Gait Similarity in Gait* Recognition

The VTM along with factorization process is presented. The gait similarity measurement is simplified using L1—norm distance and is given by Eq. (4).

$$d(f_k^i, f_k^j) = \left\| f_k^i - f_k^j \right\| \tag{4}$$

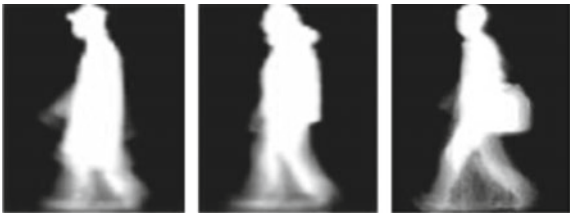
Here d represents the distance of separation between gait signatures of the two different persons under the same observing angle. The gait feature dimension is represented by N. If the distance of separation is more than the similarity between the gait signatures f_k^i and f_k^j.

4 Experiments

Simulations are performed on CASIA gait database [12]. The dataset contains the data is obtained for all 11 degree observation angles from 124 subjects. From each observation angle six sequences are considered with normal walk [9]. Furthermore, this dataset comprises of two sequences indicating respective overcoat attire and the bag carrying situation for all 11 observing angles. In CASIA database [12] the video sequences were captured with an indoor environment.

The CASIA Gait Database is provided free of charge at website http://www.cbsr.ia.ac.cn/. We have taken the 3 sets of experiments (Experiment set A, B and C) for evaluating the gait recognition. With set A, we investigate the how viewpoint affect the gait recognition and an algorithm's robustness to viewpoint variations. From all USB cameras, 10 video sequences are taken. In those 6 are with normal walking, 2 are walking with a coat and 2 are walking with a bag. In set A, the experiments are conducted on normal walking sequences. Consider first 4 normal sequences are gallery set for all 3 datasets and remaining 2 are probe set.

Figure 1 shows the Gait Energy Images of CASIA dataset. Figure 2a shows the subjects are walking normally. Figure 2b shows the subjects are walking with a coat. Figure 2c shows the subjects are walking with a bag. The experiments conducted on these three datasets. The subject's information, such as height, gender, was also recorded.



(a) Normal (b) Coat (c) Bag

Fig. 1 Gait energy images

(a) Walking normally (b) with a coat (c) with a bag

Fig. 2 Walking under different conditions

5 Results and Discussions

In this section, we are presenting the results and graphs obtained by us with the application of proposed algorithm GEI+VTM technique. The algorithm is implemented on the CASIA database, which was detailed as in the previous Sect. 4.

In order to verify the performance of the proposed algorithm we carried three types of tasks. One is to evaluate the gait recognition performance in the condition that person captured in normal walking and tested with the person under normal walking. The second is to evaluate the scenario that where person recognized under a bag carrying condition with the same carrying condition under different view angles, and as a third task we tested the registered person with wearing coat condition with the same wearing condition under different gallery angles. The below Tables and Figures gives the experimental results performed on the Set A (normal walk), Set B (walking with coat) and Set C (walking with bag) with various Gallery angle (θ_g) and Probe angle (θ_p).

As shown in Tables 1, 2 and 3 by taking the gallery data angles 0°–180° and probe data viewing angles one at a time ranges from 0°–180° with an angle difference 18°. The probe data viewing angle is transformed to the set of gallery data viewing angles.

Similar to set A, with set B and set C, we investigated that how clothing and carrying affect the gait recognition and an algorithm's robustness to clothing conditions. When $\theta_g = \theta_p$ our algorithm gives higher recognition rate when compared with the remaining combinations and is observed from Tables 1, 2, and 3. In each set A, B and C, a total of $11 \times 11 = 121$ experiments are conducted.

In order to compare the robustness of the proposed algorithm we have been taken another two parameters, % Average Recognition Rate (ARR) and % standard deviation (σ) when considered data elements diagonally (i.e. when $\theta_g = \theta_p$ from Tables 1, 2 and 3) and the corresponding values are as shown Table 4.

Table 1 The experimental results of Set A (%)

		Probe angle θ_p (normal walking)										
		0°	18°	36°	54°	72°	90°	108°	126°	144°	162°	180°
Gallery angle θ_g (normal # 1-4)	0°	98.4	32.2	10.2	4.8	4.0	4.1	2.8	3.1	5.2	13.1	38.4
	18°	24.1	99.6	40.1	8.9	5.1	4.2	4.2	6.1	14.1	34.5	9.5
	36°	5.2	38.1	98.1	29.9	12.4	10.1	9.2	14.2	24.2	14.1	2.0
	54°	3.2	4.2	30.1	97.7	23.6	17.4	22.2	30.0	22.2	6.1	2.2
	72°	1.4	4.8	8.4	22.8	97.4	82.1	69.1	22.0	6.4	4.1	2.4
	90°	0.6	3.4	5.2	18.7	83.4	97.8	83.2	16.1	6.3	4.4	2.0
	108°	2.1	2.7	3.0	17.7	72.2	88.0	95.4	38.1	7.0	3.2	2.9
	126°	1.8	3.4	7.4	38.5	34.6	23.1	49.1	96.9	27.5	5.2	3.0
	144°	4.2	6.2	29.1	19.4	5.1	2.1	4.1	44.8	97.0	6.4	3.6
	162°	13.1	40.2	16.7	3.1	2.1	1.1	1.4	13.4	6.1	98.8	29.4
	180°	41.1	20.9	9.2	3.8	3.0	1.0	2.1	4.1	13.1	52.1	99.6

Table 2 The experimental results of Set B (%)

		Probe angle θ_p (walking with a coat)										
		0°	18°	36°	54°	72°	90°	108°	126°	144°	162°	180°
Gallery angle θ_g (normal # 1-4)	0°	25.7	7.3	3.2	2.1	1.2	1.1	1.3	1.5	2.2	6.4	9.2
	18°	4.9	28.1	19.2	7.8	1.4	1.3	1.2	2.9	6.1	12.8	3.2
	36°	2.1	9.4	31.3	17.4	2.1	1.6	1.8	6.5	9.8	4.2	1.0
	54°	1.1	3.2	11.2	31.5	6.1	5.1	8.4	15.1	6.1	2.8	1.1
	72°	0.4	3.4	6.3	7.9	32.1	22.4	15.3	9.2	3.0	2.9	0.6
	90°	1.8	3.1	4.8	7.0	21.7	33.4	17.4	7.2	4.2	3.6	1.0
	108°	2.2	3.5	3.4	4.9	18.7	28.2	31.1	9.4	5.4	2.8	1.8
	126°	2.4	2.1	2.5	4.8	11.2	11.2	19.4	27.8	9.5	1.8	2.0
	144°	3.2	3.9	5.1	13.6	5.3	2.8	5.3	19.1	31.4	1.4	2.5
	162°	3.6	8.4	10.2	3.1	1.3	1.1	1.5	2.4	5.4	28.2	7.5
	180°	10.2	7.2	4.1	2.1	1.8	0.4	0.2	2.5	6.2	13.5	28.4

Table 3 The experimental results of Set C (%)

		Probe angle θ_p (walking with a bag # 1-2)										
		0°	18°	36°	54°	72°	90°	108°	126°	144°	162°	180°
Gallery angle θ_g (normal # 1-4)	0°	81.2	20.6	5.8	3.6	3.1	3.0	2.4	2.2	5.2	15.5	26.2
	18°	17.4	77.4	37.2	7.9	9.2	3.4	3.1	5.2	11.2	19.1	9.2
	36°	3.9	24.1	75.4	25.2	10.1	8.1	8.1	11.2	16.4	5.6	2.4
	54°	1.2	3.4	20.2	67.5	20.0	15.1	15.4	19.4	8.2	5.1	1.8
	72°	1.1	4.2	7.4	9.1	61.4	33.2	23.4	12.6	5.2	4.2	2.2
	90°	0.9	3.2	6.1	9.2	43.3	58.7	32.8	10.6	6.8	3.6	2.0
	108°	2.2	1.6	4.2	7.9	38.9	5.1	58.4	24.2	7.5	4.4	2.4
	126°	2.4	3.1	5.0	18.3	26.4	15.1	28.6	66.8	15.4	3.0	2.0
	144°	2.5	5.2	16.3	12.4	7.1	3.0	5.4	32.4	65.2	3.1	2.2
	162°	8.0	24.2	14.1	3.9	3.4	3.1	3.6	4.8	17.1	69.2	19.8
	180°	31.2	13.4	7.4	3.0	2.4	3.2	1.8	3.2	8.4	32.1	81.2

Table 4 Comparision of the performance metrics

Parameter	Technique	Set A	Set B	Set C
% ARR	GEI[12]	0.97	0.28	0.67
	GEI+VTM(proposed)	0.98	0.30	0.69
% ψ	GEI[12]	0.302	0.086	0.195
	GEI+VTM(proposed)	0.012	0.022	0.08

From the recognition rate and standard deviation values in Table 4, it is clear that there is an improvement in the recognition rate (ARR) and reduction in the deviation (ψ) with the corresponding values, which is always a preferable combination in order to prove the robustness of the our algorithm GEI+VTM technique for varying conditions when compared with GEI technique [12] for all experiments with Set A, Set B and Set C.

6 Conclusion and Future Scope

The proposed algorithm performs the gait-based person recognition evaluating the effects of covariates. Here, we consider the covariates as viewpoint, carrying and wearing conditions, and the algorithm robust to viewing angle variation and large intraclass variations like clothing styles, carrying goods, etc. GEI is taken as the feature in order to recognize the persons. In future we will consider the different gait features in order to improve the recognition accuracy. Experiments are conducted on CASIA database, all the gait sequences are taken from an indoor environment. But in future, we will consider the gait sequences from an outdoor environment.

References

1. Gafurov, D., Snekkene, E., Bours, P.: Gait Authentication and Identification Using Wearable Accelerometer sensors. IEEE Workshop on automatic Identification Advanced technologies, pp: 220–225, (2007)
2. Boulgouris, N.V., Hatzinakos, D., Plataniotis, K. N.: Gait Recognition: A Challenging Signal Processing Technology for Biometric Identification. Signal Processing Magazine, IEEE, pp: 78–90, (2005)
3. Moeslunda, T. B., Adrian, H., Volker, K.: A survey of advances in vision based humanmotion capture and analysis, Computer Vision and Image Understanding, Volume 104, Issues 2–3, November-December 2006, pp: 90–126, (2006)
4. Bo, Y., Yumei, W.: A New Gait Recognition Method Based on Body Contour. Control, Automation Robotics and Vision, ICARCV International conference on, pp: 1–6, (2006)
5. Hema, M., Jagadeesh, G.: Gait Based Person Recognition using Partial Least Squares Selection Scheme. (IJCI) Vol. 5, No. 4, pp: 247–254, (August 2016)
6. Nikolaos V. Boulgouris, Dimitrios Hatzinakos, Konstantinos N. Plataniotis.: Gait recognition: A challenging signal processing technology for biometric identification. IEEE Signal Processing Magazine, pages 78–90, (November 2005)
7. Sudeep Sarkar, P., Jonathon Phillips, Zongyi Liu, Rebledo Vega, I., Patrick Grother, Kevin W. Bowyer.: The HumanID gait challenge problem: Data sets, performance, and analysis. IEEE Transactions on Pattern Analysis and Machine Intelligence, 27(2):162–177, (2005)
8. Sloman, L., Berridge, M., Homatidis, S., Hunter, D., Duck. T.: Gait patterns of depressed patients and normal subjects. American Journal of Psychiatry, 139(1):94–97, (1982)
9. Wang, L., Tan, T., Ning, H., Hu, W.: Silhouette analysis based gait recognition for human identification. IEEE Trans. On PAMI, (2003)
10. Makihara, J., Sagawa, R., Mukaigawa, Y.: Gait recognition using a view transformation model in the frequency domain. in ECCV, (2006)
11. Kusakunniran, W., Wu, Q., Li, H., Zhang, J.: Multiple view gait recognition using view transformation model based on optimized gait energy images. in ICCV workshops, 2009.
12. S. Yu, D. Tan, and T. Tan, "A framework for evaluating the effect of view angle, clothing and carrying condition on gait recognition," in ICPR, (2006)

Assistance Vision for Blind People Using *k*-NN Algorithm and Raspberry Pi

P. Satyanarayana, K. Sujitha, V. Sai Anitha Kiron, P. Ajitha Reddy and M. Ganesh

Abstract Eyes are the natural camera that human beings possess. But not all the people are lucky enough to have them. About 15 million people in India suffer with visual impairments. So, through this chapter, an attempt is made to help them by providing assistance for text reading from the documents and papers. The characters present in the text are isolated from cluttered background or the surrounding objects in the camera view. The characters are separated from one another by drawing contours. Once the text characters in the localized text regions are detected, they are binarized and trained using *k*-Nearest Neighbor (*k*-NN). The trained data is stored in a file and these will be the classifiers. These classifiers are loaded while testing. The text in the image is recognized based on the loaded classifiers file. This recognized text is stored and converted to speech.

Keywords Contours · Text detection · Optical character recognition · k-Nearest Neighbor · Classifiers · Speech conversion

P. Satyanarayana (✉) · K. Sujitha · V. Sai Anitha Kiron · P. Ajitha Reddy · M. Ganesh
Department of Electronics & Communications, K L University, Guntur, Andhra Pradesh, India
e-mail: satece@kluniversity.in

K. Sujitha
e-mail: ksujitha643@gmail.com

V. Sai Anitha Kiron
e-mail: anita.kiron@gmail.com

P. Ajitha Reddy
e-mail: ajithareddyponnapati@gmail.com

M. Ganesh
e-mail: mganesh0426@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*, Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_12

1 Introduction

According to census 2014 World Health Organization (WHO) report, it was estimated that 285 million people are visually impaired. Of these, 39 million are blind, 246 million people have low vision, and 82% of people living with blindness are aged 50 and above [1]. They need continuous assistance for every work. The advancement in technology has greatly helped blind people in making their work easy.

Recent developments in Computer Vision, Portable Computers, and Digital Cameras made the problem to be solved easily. By developing camera-based products that combine Computer Vision technology with different products, we can perform Optical Character Recognition (OCR). Some reading assistive frameworks, for example, pen scanners may be utilized in these and comparable circumstances. Such frameworks incorporate OCR programming to offer the capacity of checking also, acknowledgment of content and some have coordinated voice yield. Be that as it may, these frameworks are by and large intended for and perform best with archive pictures with straightforward foundations, standard text styles, a little scope of text dimensions, and very much sorted out characters as opposed to business item boxes with numerous improving designs. To help blind persons to read content from the hand-held articles, the camera-based assistive content reading system to track the object of enthusiasm inside of the camera view and extract print text data from the object. In this chapter, the proposed algorithm successfully detects and recognizes the text that is on a white paper and converts it into speech.

1.1 Optical Character Recognition

Optical character recognition (OCR) is an electronic conversion of images of handwritten text and printed data into machine-encoded text. Some methods for optical character recognition include *K*-Nearest Neighbor (KNN), Support Vector Machine (SVM). One of the prime motivations of early development of OCR system was a reading aid for the visually handicapped. One of the best possible ways of achieving this goal is to convert the *k*-NN output into speech format.

2 Literature Review

For text extraction and recognition, Vamvakas et al. [2] presented a paper using OCR software. Using this software, labels on the products are detected and converted to speech. The products are held in hand and a slight movement of the product will make the camera detect the characters.

Image Segmentation Method was proposed by Zhou et al. [3] and Gatos in their work. Their attempts for extracting the text were purely on Historical Documents. A data base was created for that script and using Image Segmentation they tried to detect the characters in the image. However, the accuracy by this algorithm is very less and hence, contour based technique was used in this chapter.

Zhang and Zhou [4] presented a paper on improved *k*-NN algorithm. The problem is that KNN classifier may decrease the precision of classification because of the uneven density of training data. To solve the problem, a new clustering-based KNN method is presented in this chapter.

Jubair and Banik [5] have proposed a paper for text categorization based on Gini index algorithm. This algorithm was used to reduce high dimensionality. *k*-NN and *fk*-NN classifiers are studied, and an attempt was made to implement the *k*-NN classifier in this chapter.

3 *K*-Nearest Neighbor Algorithm

K-Nearest Neighbor algorithm is a simple and nonparametric lazy learning algorithm used for classification. In KNN classification, the output obtained is a class membership. The object is classified based on the majority of the votes from its neighbors. The classification is based on the value k which means the number of nearest possible neighbors. k is generally a small positive integer, if $k = 1$ the object is simply assigned the value of its closest neighbor.

Given a training set D consisting of n vectors in multidimensional space $\{d_1, d_2, d_3, \ldots, d_n\}$ and $m(m < n)$ classes $\{C_1, C_2, C_3, \ldots, C_m\}$. All the data points of each training set are in a multidimensional space. In order to predict the new class present in the vector of new training set D_{test}, the *k*-NN classifier seeks the k-nearest neighbors of the new set and then assigns them to the class. If $m = n$, that is, when the number of vectors of two classes are equal, then classification is done based on the distance. A commonly used method for finding distance for continuous variables is Euclidean distance. In *k*-NN, Euclidian distance estimation is used to find the distances from the object to the neighbors. When a new object enters the multi-dimension space, the distance from that object to all its neighbors is calculated. Let $\{a_1, a_2, \ldots, a_n\}$ be the vectors for the new object. The vectors of one of its nearest neighbor are $\{d_1, d_2, d_3, \ldots, d_n\}$. Now the Euclidean distance from the new object to its neighbor is

$$\text{Euclidean distance} = \sqrt{(a_1 - d_1)^2 + (a_2 - d_2)^2 + \cdots + (a_n - d_n)^2}. \quad (1)$$

Once the distances from the object to all its neighbors are obtained, the class of this new object is obtained based on these values. The new object is assigned based on the majority class of its nearest neighbors.

For a given vector from the new class, x_t, k-NN algorithm works as

$$y_t = argmax_{c \in \{c_1, c_2, \ldots, c_m\}} \sum_{x_i \in N(x_t, k)} E(y_i, C), \tag{2}$$

where y_t is the predicted class for the given instance x_t, and m is the number of classes present in the data. Here, $N(x, k)$ is the set of k-nearest neighbors of x

$$\text{Also, } E(a, b) = \begin{cases} 1 & if\ a = b \\ 0 & else \end{cases}. \tag{3}$$

Now, the equation of y_t can be written as

$$y_t = argmax\left\{ \sum_{x_i \in N(x_t, k)} E(y_i, c_1), \sum_{x_i \in N(x_t, k)} E(y_i, c_2), \ldots \sum_{x_i \in N(x_t, k)} E(y_i, c_m), \right. \tag{4}$$

$$y_t = argmax\left\{ \sum_{x_i \in N(x_t, k)} \frac{E(y_i, c_1)}{k}, \sum_{x_i \in N(x_t, k)} \frac{E(y_i, c_2)}{k}, \ldots \sum_{x_i \in N(x_t, k)} \frac{E(y_i, c_m)}{k}, \right. \tag{5}$$

$$\text{But,} \qquad P(c_j)_{(x_t, k)} = \sum_{x_i \in N(x_t, k)} \frac{E(y_i, c_j)}{k}. \tag{6}$$

Here, $P(c_j)_{(x_t, k)}$ is the probability of occurrence of jth class in the neighborhood of x_t.

$$\text{Hence, } y_t \text{ becomes: } y_t = argmax\left\{ p(c_1)_{(x_t, k)}, p(c_2)_{(x_t, k)}, \ldots, p(c_m)_{(x_t, k)} \right\}. \tag{7}$$

From the above equation, k-NN uses only priori probabilities to calculate the class of a given instance. Also, k-NN ignores the class distribution around the neighborhood of the given instance (here, x_t).

Consider an example of k-NN algorithm having two different classes. Both the classes are clustered and when a new object enters this cluster, it becomes difficult to classify the new object. A detailed explanation for a simple k-NN classification is stated below.

Figure 1 is an example illustrating the k-NN classification. The dotted circle has a value of $k = 1$ and the solid circle's k value is 3 (say). The test sample (red diamond) should be classified either to first class (green triangles) or second class (blue squares). When $k = 1$, the test sample is classified under first class as there are more triangles (5 triangles) than squares (3 squares). Similarly, when $k = 3$, the test sample is assigned to second class as there are more squares (12) than triangles (11).

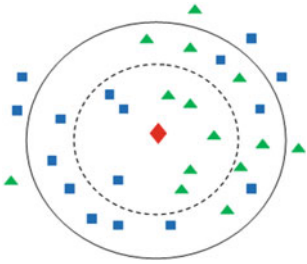


Fig. 1 Example for *k*-NN classification

3.1 k-*NN Classifier*

The purpose of *k*-NN classifier is to define the class of new object by finding similarity between the neighbor objects. The decision function can be defined as

$$\mu_j(X) = \sum_{i=1}^{k} \mu_j(X_i) sim\,(X, X_i), \tag{8}$$

where $\mu_j(X_i) \in \{0, 1\}$ shows whether X_i belongs to $\omega_j\left(\mu_j(X_i) = 1\, is\, true\right)$ or not $\left(\mu_j(X_i) = 1\, is\, false\right)$; $sim\,(X, X_i)$ gives the similarity between the neighbor objects and new object.

4 Proposed Work

The first two stages are based on training and testing the data. The work is extended in the third stage by converting the obtained text data to speech. Furthermore, the entire work is implemented on Raspberry Pi.

4.1 Stage 1—Training Data

Let X be a sample image having all the characters (alphabets, numbers, etc.,) to be trained. Generally, all the documents are written or typed on a white paper. So, we have taken a white paper with black characters on it.

4.1.1 Text Extraction

The input image X is converted into a binary image. This makes the background of the image white with pixel intensity 1 and foreground of the image black with pixel intensity 0. Characters present in the foreground are extracted from background by

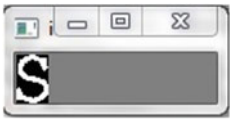


Fig. 2 Resized image after finding contours of a letter in an image

considering the coordinates (x, y) of the black pixel. Maximum and minimum values among the black pixels are counted and from those values, object region (of the character) are extracted. (x_{min}, y_{min}) values become the top-left corner's coordinate and (x_{max}, y_{max}) will be the bottom right corner's object region. The maximum and minimum values of x and y of the extracted region are stored in image matrix X_E (say). The image is resized to a global size and let X_{ER} be the resized image. In this way, the image is partitioned into number of cells. Now contours for the resized image are found and let X_{ERT} be the image after finding contours. Now, contour for each character is detected and accordingly the corresponding character is pressed from the keyboard for training purpose.

Figure 2 is the resized image after finding contours for each letter in each test image. Once all the characters in the image are detected and trained, the training will be completed. In this way, training is done for different fonts of data and the classifiers are generated and stored in notepad for each font.

Figure 3 is a test image used for training the data. The input image is blurred by Gaussian blur, later, thresholding operation (adaptive threshold) is applied for better results and finally the image is converted into a binary image.

Figure 4 is the result obtained after training the data set. The test image is trained by pressing appropriate character from the keyboard. Red squares are the contours detected for each character.

Fig. 3 Input image is converted into binary image and applied adaptive thresholding

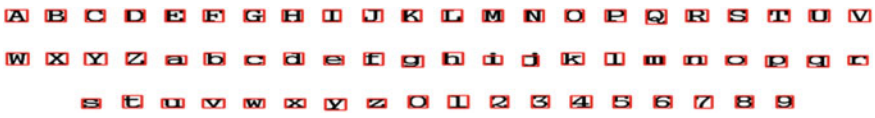


Fig. 4 Training the data set

4.2 Stage 2—Testing Data

The trained data set is stored as classification files while training the data. All the classifiers are loaded while testing the data. Now, the text to be read is passed in the form of continuous frames. The contours are detected for the letters and the extracted letters are classified according to the predefined trained data loaded initially in the program. The recognized text is displayed on the screen and the same is saved into a text file.

4.3 Stage 3—Text-to-Speech Conversion

A speech engine is used for converting the detected text into speech. Generally, a text-to-speech converter is an artificial production of human speech.

4.4 Stage 4—Hardware Interfacing

The device used by the blind persons for this purpose should be easy to handle with hands and the size also should not be large as it may become difficult for handling if the size of the device increases. Hence, a pocket-sized computer, Raspberry Pi was chosen as the hardware interface. Raspberry Pi works with an upgraded ARM v7 multi-core processor and a full Gigabyte cycle of RAM. When compared to other boards, Raspberry pi is very economical. It uses an SD card for booting and persistent storage, with the Model B+ using a MicroSD. The entire program is written and executed using python and OpenCV on Raspberry Pi board.

5 Results and Discussions

Figures 5 and 6 are the results obtained while testing the image which contains the word in Calibri (Body) font. Once the letters are detected the system stores the letters in the word in a text file and then converts the text in the text file to speech and reads it.

Figure 7 is the result obtained while testing the image which contains the word in Simplified Arabic Fixed font. Once the letters are detected the system shows the word it has detected and after detecting it reads the word using Text-to-Speech module (tts).

Figure 8 is the final output results when the code is implemented on Raspberry Pi board.

Fig. 5 Result obtained for Calibri (Body) font

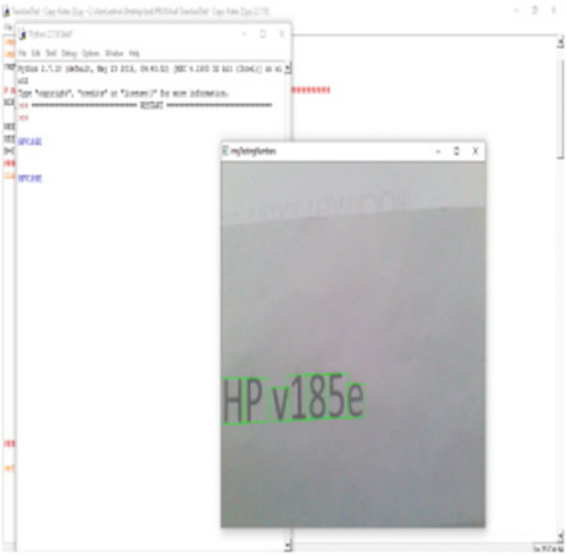


Fig. 6 Result obtained for Calibri (Body) font

Fig. 7 Result obtained for simplified Arabic Fixed font

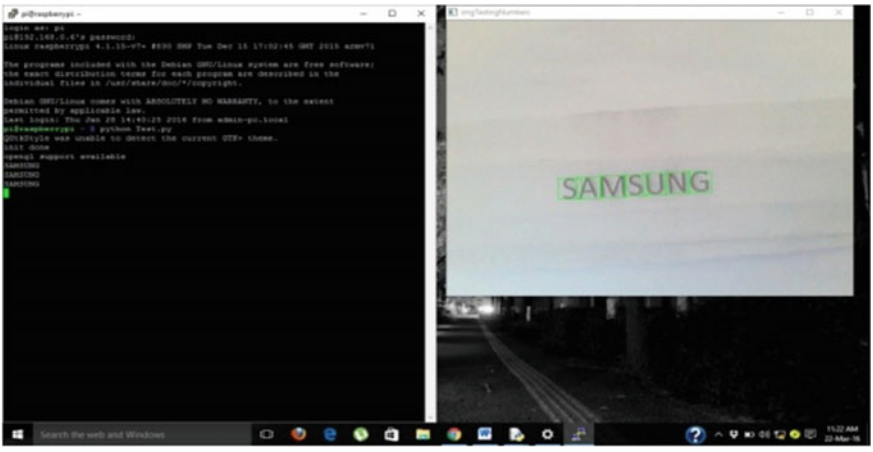


Fig. 8 Result shown on Raspberry Pi terminal

6 Conclusion

In this chapter, a prototype system that reads and converts text into machine readable form was designed. For detecting and recognizing the text, *K*-Nearest Neighbor algorithm was used. Black characters with white background were extracted and recognized correctly and it was observed that using *K*-Nearest Neighbor algorithm, the results obtained were 90% accurate. Using KNN algorithm

hand written text and printed text in cursive letters cannot be recognized accurately. Furthermore, *fk*-NN Classifier, SVM, other OCR methods, are used for detecting and recognizing different fonts with high accuracy.

Acknowledgments We are very grateful to our esteemed Professor Dr. A.S.C.S. Sastry, Head of Department, ECE, KL University, Vaddeswaram, Guntur, A.P., INDIA, for his valuable guidance and creative suggestions that helped us to complete this chapter.

References

1. Chucai Yi, Yingli Tian and A. Arditi, "Portable Camera-Based Assistive Text and Product Label Reading From Hand-Held Objects for Blind Persons," in *IEEE/ASME Transactions on Mechatronics*, vol. 19, no. 3, pp. 808–817, (June 2014).
2. G. Vamvakas, B. Gatos, N. Stamatopoulos and S. J. Perantonis, "A Complete Optical Character Recognition Methodology for Historical Documents," *Document Analysis Systems, 2008. DAS '08. The Eighth IAPR International Workshop on*, Nara, pp. 525–532, (2008).
3. Lijuan Zhou, Linshuang Wang, Xuebin Ge and Qian Shi, "A clustering-Based KNN improved algorithm CLKNN for text classification," *Informatics in Control, Automation and Robotics (CAR), 2010 2nd International Asia Conference on*, Wuhan, pp. 212–215, (2010).
4. Min-Ling Zhang and Zhi-Hua Zhou, "A k-nearest neighbor based algorithm for multi label classification," *Granular Computing, 2005 IEEE International Conference on*, pp. 718–721 Vol. 2, (2005).
5. Mohammad Imrul Jubair and Prianka Banik. Article: A Simplified Method for Handwritten Character Recognition from Document Image. *International Journal of Computer Applications* 51(14):50–54, (August 2012).

Patch Rotation-Based Frequency Reconfigurable Antenna for Wireless Applications

Perla Devi and Valluri Rajya Lakshmi

Abstract Frequency reconfigurable antenna is proposed in this chapter. The antenna structure consists of three patches namely rectangular patch, circular patch, and square patch. These patches are placed on Rogers RT duroid substrate. Frequency reconfigurability is achieved by using patch rotation technique. Rotating the patches by 120° in each rotational stage, the resonant frequency of the antenna is changed. This design is useful for Personal Communication System (PCS), Wi-Fi, and Wi-MAX applications.

Keywords Reconfigurable antenna · Structural alteration technique · Return loss · VSWR

1 Introduction

The design of reconfigurable antennas has received a lot of attention in recent years. The term "reconfigurability" means the ability to change the antenna characteristics with respect to the application [1]. Many techniques can be used to achieve reconfigurability. Most of these techniques employ switches; the switch can be PIN diode, varactor diode, photoconductive diode, or RF MEMS. Other techniques use mechanical alterations like rotation or bending certain antenna part.

P. Devi (✉) · V. Rajya Lakshmi
Electronics and Communication Engineering, ANITS, Sangivalasa, Visakhapatnam, India
e-mail: deviperla5893@gmail.com

V. Rajya Lakshmi
e-mail: rajyalakshmi.ece@anits.edu.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_13

Reconfigurable antennas are used in multiple input multiple output (MIMO) situations, satellite systems, cognitive radios, in wireless devices, and many other systems. The reconfigurable antennas are of three types namely Frequency reconfigurable antenna, radiation-pattern reconfigurable antenna, and polarization reconfigurable antenna. The frequency reconfigurable antenna can change its resonant frequency with respect to application. Similarly, the pattern and polarization reconfigurable antennas can change their radiation pattern and polarization, respectively, with respect to user requirement [2, 3].

Frequency Reconfigurable antennas have been implemented so far using PIN diodes, varactor diode, lumped elements, or photoconductive switches. A hexagonal slot-shaped frequency reconfigurable antenna that uses varactor diode to change the operating frequency of an antenna, when the voltage applied across the diode is changed, the characteristics of an antenna is changed that will change the operating frequency [4]. A rolled monopole antenna is considered, the radius of the monopole can be changed electrically. By changing the radius of the monopole, the structure of the patch that is connected to the feed is changed that will cause changes in the resonant frequency [5]. A stretchable patch is considered, by applying uniform stretching forces on a substrate, the length of the patch will vary and it changes the resonant frequency [6]. The Sierpinski gasket monopole antenna can change its operating frequency from one frequency to another frequency by changing its position of the probe feed on a strip line [7]. A BST film is used as substrate, by applying the voltage across the patch and the ground plane, the characteristics of the substrate will change, that in turn changes the resonant frequency [8]. A rectangular patch antenna with U-shaped slot consists of variable capacitor and inductor between the ground plane and patch. By changing the capacitance value, this antenna exhibits frequency agility [9]. A seven-shaped planar monopole antenna has varactor diode exhibits frequency reconfigurability by changing the diode state [10].

In view of above observations, patch rotation technique based frequency reconfigurable antenna is proposed. The advantage of this technique is that bias lines are not required. When compared with precious designs on frequency reconfigurable antenna, maximum of the designs used switches, in that designs the bias lines might affect the EM performance of the antenna and add further complexity to the antenna structure. In Proposed deign, the frequency reconfigurability is achieved by rotating the patches by 120°. This antenna is useful for PCS, Wi-Fi, and Wi-MAX applications.

2 Antenna Design

The frequency reconfigurable antenna is designed by using patch rotation technique in Ansoft HFSS simulation tool. In patch rotation technique, different numbers of patches are placed on the substrate. At any instant, only one patch is connected to

the feed, by rotating all the patches by a certain angle, the shape that was connected to the feed is changed. This in turn will change the resonant frequency of the antenna.

The frequency reconfigurable antenna design consists of three different patch shapes, these patches are placed on the Rogers RT duroid substrate. The patches are rectangular patch, circular patch, and square patch. At every 120° rotation of the patches, the patch that was connected to the feed will vary. The three essential parameters for the design of an antenna are as follows:

1. Frequency of Operation,

   f_r = 3.45 GHz for Position-1
   f_r = 2.45 GHz for Position-2
   f_r = 1.9 GHz for Position-3

2. Dielectric constant of the substrate, $\varepsilon_r = 4.4$
3. Height of substrate, h = 1.6 mm.

By using above three parameters the dimensions of the design is calculated.

2.1 Rectangular Patch (f_r = 3.45 GHz)

The length and width of the rectangular patch is calculated by using the below formula.

Width of the patch (W) is given by

$$W = \frac{C_0}{2f_r}\left(\frac{\varepsilon_r + 1}{2}\right)^{\frac{-1}{2}}. \tag{1}$$

The length of the patch (L) is given by

$$L = L_{eff} - 0.824\frac{\left(\varepsilon_{reff} + 0.3\right)\left(\frac{W}{h} + 0.264\right)}{\left(\varepsilon_{reff} - 0.258\right)\left(\frac{W}{h} + 0.8\right)}. \tag{2}$$

where

L_{eff} is the effective length of the patch and
ε_{eff} is the effective dielectric constant.

The effective length of the patch (L_{eff}) is given by

$$L_{eff} = \frac{C_0}{2f_r\sqrt{\varepsilon_{eff}}}, \tag{3}$$

where C_0 is the velocity of light in free space.

The effective dielectric constant (ε_{eff}) is given by

$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}(1 + 12\,h/W)^{\frac{-1}{2}}. \tag{4}$$

2.2 Circular Patch (f_r = 2.45 GHz)

The effective radius of circular patch (a_{eff}) is given by

$$a_{eff} = a \cdot \left[1 + \frac{2h}{\pi a \varepsilon_r}\left(\ln\left\{\frac{\pi a}{2h}\right\} + 1.7726\right)\right]^{\frac{1}{2}}, \tag{5}$$

where "a" is the actual radius of patch

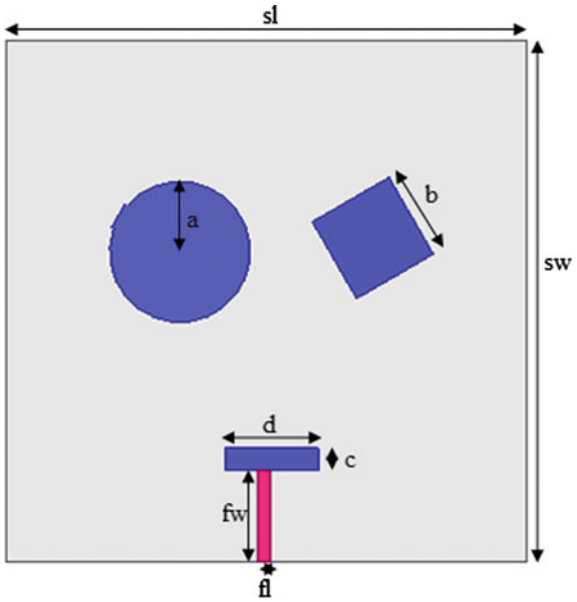


Fig. 1 Frequency reconfigurable antenna

Table 1 Dimensions of Fig. 1

Parameters	Description	Value (mm)
a	Radius of the circle	5.4
b	Length of the square	6.8
c	Width of the rectangle	1.7
d	Length of the rectangle	7.4
fl	Feed length	1
fw	Feed width	7
sl	Substrate length	40
sw	Substrate width	40

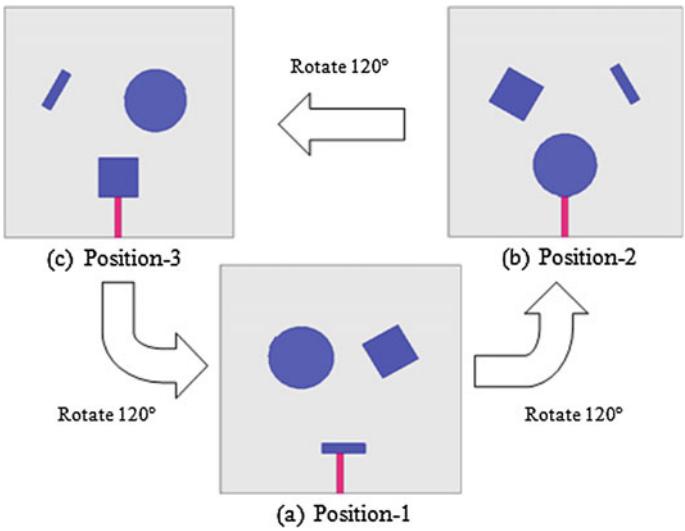


Fig. 2 Antenna reconfigurability process

$$a = \frac{1.84 * c}{2\pi f_r \sqrt{\varepsilon_r}}. \tag{6}$$

2.3 Square Patch (f_r = 1.9 GHz)

$$L = W = \frac{C_0}{2f_r}\left(\frac{\varepsilon_r + 1}{2}\right)^{\frac{-1}{2}} \tag{7}$$

After parameterization, the design of rotatable frequency reconfigurable antenna is shown in Fig. 1 and the dimensions of the Fig. 1 are listed in Table 1.

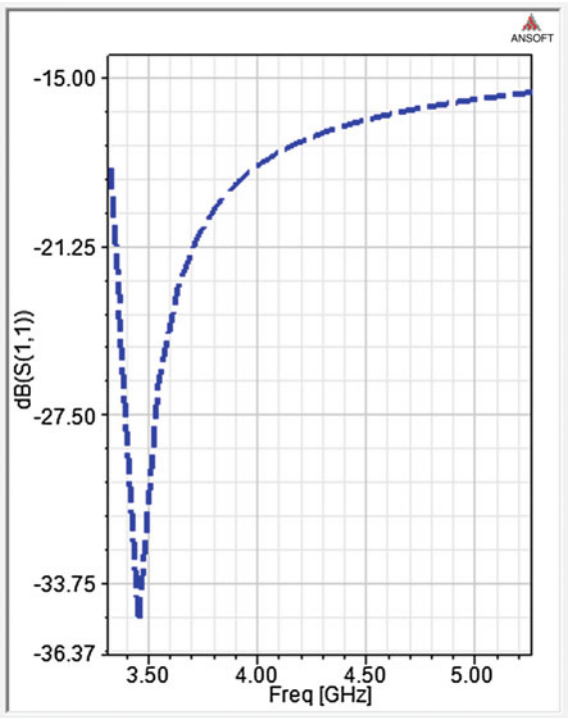


Fig. 3 Return loss plot in position-1

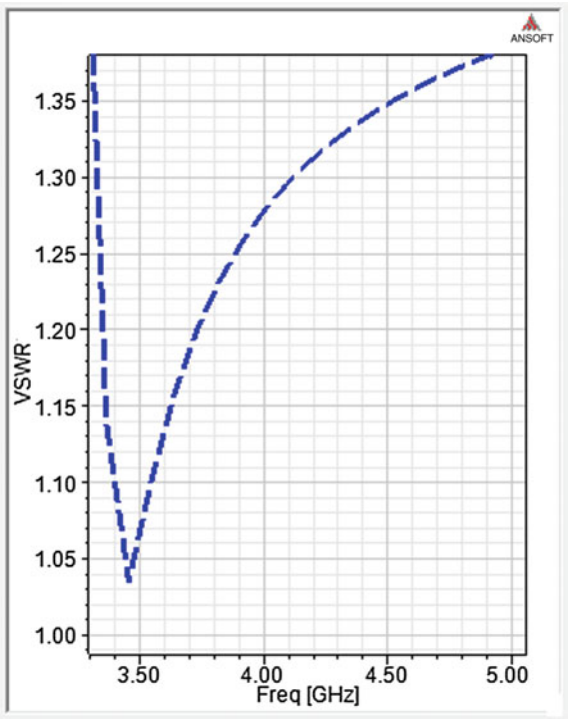


Fig. 4 VSWR plot in position-1

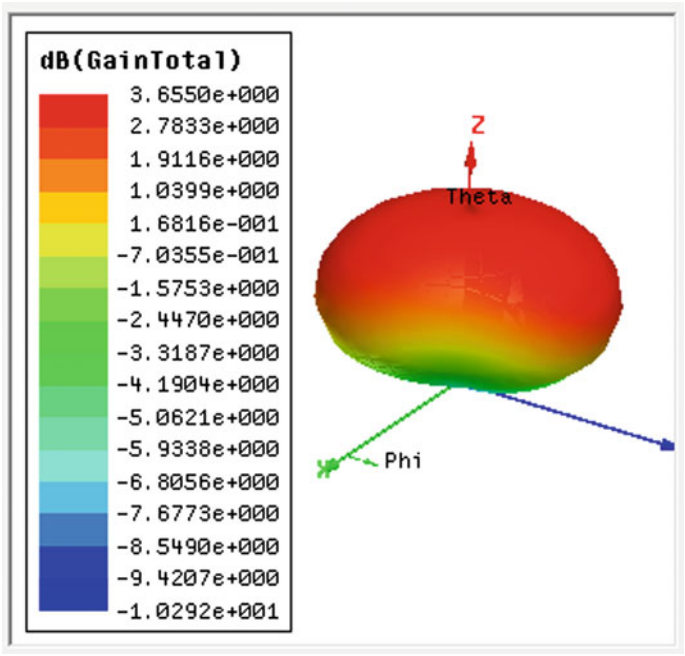
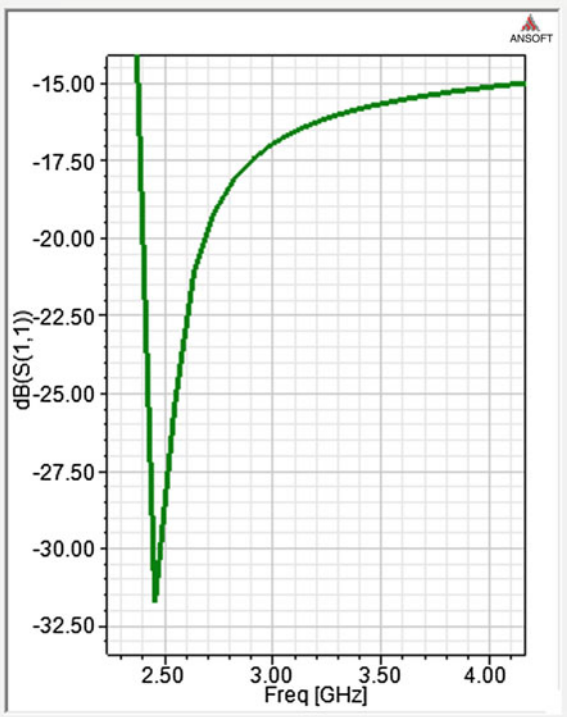


Fig. 5 3-D gain plot in position-1

Fig. 6 Return loss plot in position-2



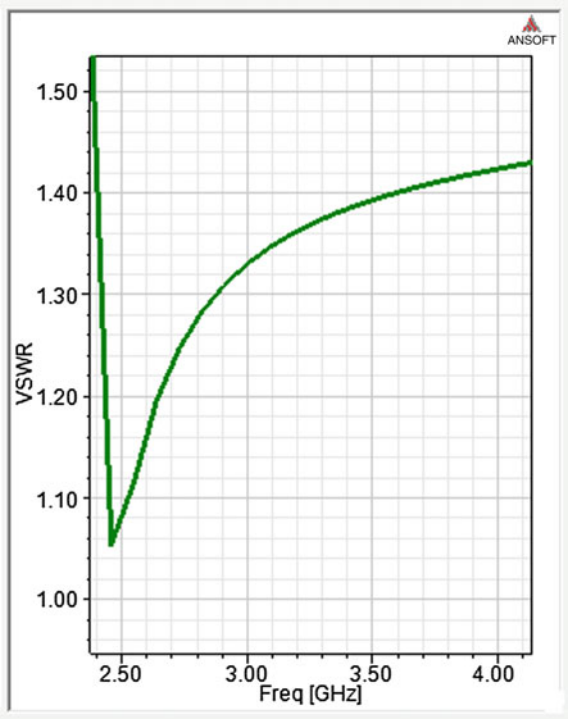


Fig. 7 VSWR plot in position-2

The rotational mechanism is briefly described in Fig. 2. At each rotational stage, the strip line excites a different patch and a different frequency is achieved. In position-1, the rectangular shape was connected to the feed and the antenna structure resonates at 3.45 GHz. In position-2, the circular patch is connected to the feed and it has a resonant frequency of 2.45 GHz. In position-3, the square patch is connected to the feed and the antenna structure resonates at 1.9 GHz.

3 Results

The design is simulated in three different positions.

3.1 Position-1

In Position-1, the design resonates at 3.45 GHz with a return loss of −35.09 dB and VSWR of 1.03. Figure 3 shows the simulated Return loss plot. Return loss ($\mathbf{S_{11}}$) is a measure of how much power is reflected back at the antenna port due to mismatch

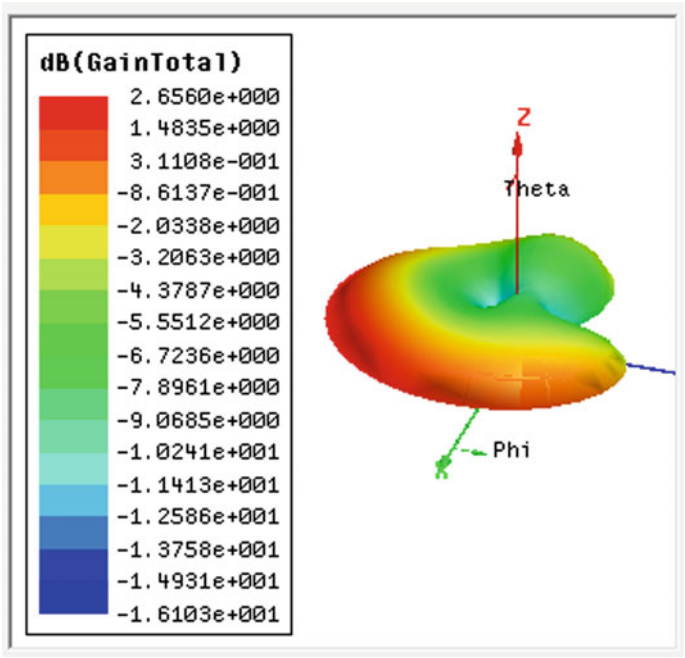


Fig. 8 3-D gain plot in position-2

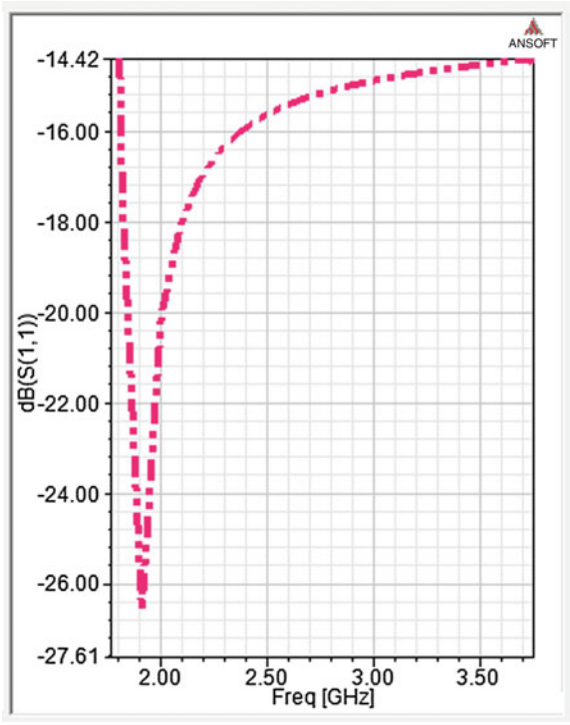


Fig. 9 Return loss plot in position-3

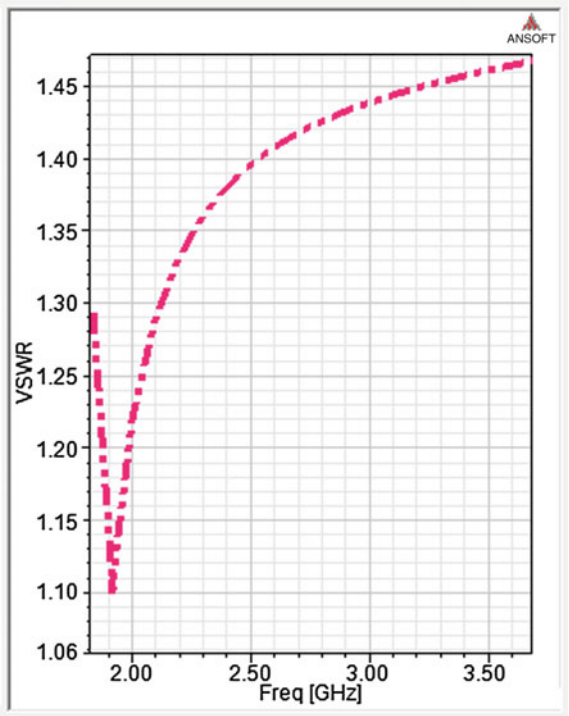


Fig. 10 VSWR plot in position-3

from the transmission line. The VSWR versus Frequency plot is shown in Fig. 4. In this case, the design has a gain of 3.65 dB and the 3D gain plot is shown in Fig. 5.

3.2 Position-2

In Position-2, the design resonates at 2.45 GHz with a return loss of −31.69 dB and VSWR of 1.05. Figures 6 and 7 show the return loss plot and VSWR plot, respectively. 3-D gain plot is shown in Fig. 8 and it has a value of 2.65 dB.

3.3 Position-3

In Position-3, the design resonates at 1.9 GHz with a return loss of −26.55 dB and VSWR of 1.09. Figures 9 and 10 show the return loss plot and VSWR plot respectively. 3-D gain plot is shown in Fig. 11 and it has a value of 4.57 dB.

Finally, the frequency reconfigurable antenna can tune its frequency to three different frequencies by rotating the patches by 120°.

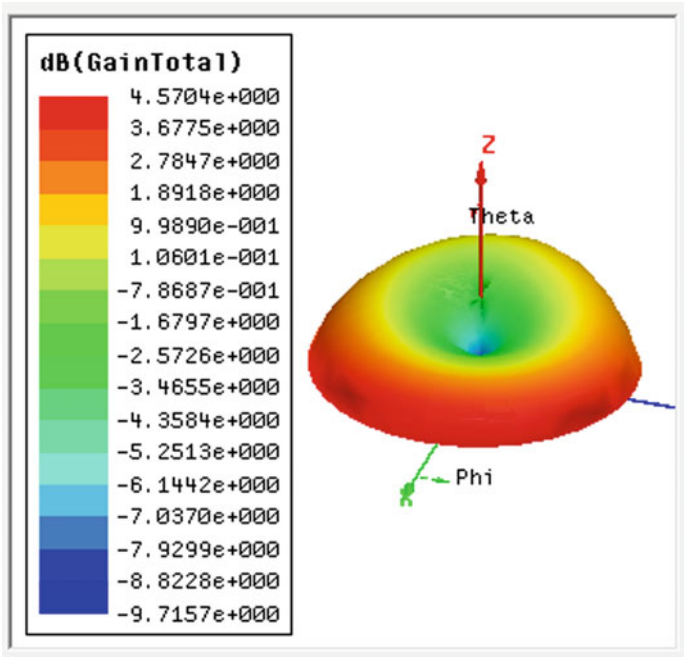


Fig. 11 3-D gain plot in position-3

4 Conclusion

The proposed frequency reconfigurable antenna can tune its frequency to three different frequencies. In position-1, rectangular patch is connected to the feed and it has a resonant frequency of 3.45 GHz with a return loss of −35.09 dB, and it is useful for Wi-MAX application. By rotating the patches by 120° in step, in position-2 circular patch is connected to the feed with a resonant frequency of 2.45 GHz and return loss of −31.69 dB. In position-3, square patch is connected to the feed with a resonant frequency of 1.9 GHz and return loss of −26.55 dB. In position-2 and in position-3, the designs are useful for Wi-Fi and PCS applications, respectively.

References

1. Bernhard, J. T. Reconfigurable Antenna. Sam rafeal. CA, USA, Morgan & claypool, (2007)
2. CG. Christodoulou. Y. Tawk, Lane, S. A., Erwin, S. R.: Reconfigurable antenna for wireless & space applications. Proc. IEEE, vol.100, no.7, pp 2250–2261, (Jul.2012)
3. Haupt, R. L., Lanagan, M.: Reconfigurable antennas. IEEE Antennas & Prop. Mag., vol.55, no.1, pp 49–61, (Feb 2013)

4. Shynu, S. V., Augustin, G., Aanandan, C. K., Mohanan, P., Vasudevan, K.: Design of compact reconfigurable dual frequency microstrip antennas using varactor diodes. Progress in Electromagnetic Research, PIER 60, 197–205, (2006)
5. Giuseppe Ruvio, Max J. Ammann and Zhi Ning Chen. Wideband reconfigurable rolled planar monopole antenna. IEEE Transactions on Antenna and Propagation, vol.55, no.6, (June 2007)
6. Shahrzad Jalali Mazlouman, Xing Jie Jiang, Alireza Mahanfar, Carlo Menon Rodney G. Vaughan.: A reconfigurable patch antenna using liquid metal embedded in a silicone substrate. IEEE Transactions on Antennas and Propagation, vol.59, no.12, (Dec 2011)
7. Ajith Kumar M.M., Amalendu Patnaik, Christos G. Christodoulou.: Design and Testing of a multifrequency antenna with a reconfigurable feed. IEEE Antennas and Wireless Propagation Letters, vol.13, (2014)
8. Yelong Wang, Chunheng Liu, Bin Sun, Yang Liu, Xiadong Sun, Fei Li, Yueguang Lu.: Design of an instantaneous-wideband frequency reconfigurable antenna based on (Ba,Sr) Ti03/MgO composite thin films. IEEE Transactions on Antennas and Propagation, vol.62, no.12, (Dec.2014)
9. Shing - Lung Steven Yang, Ahmed A. Kishik, Kai – Fong Lee.: Frequency Reconfigurable U – Slot Microstrip Patch Antenna. IEEE Antennas and Wireless Propagation Letters, vol7, (2008)
10. Shah, S.A.A., Khan, M.F., Ullah, S., Flint, J. A.: Design of a Multi-Band Frequency Reconfigurable Planar Monopole Antenna using Truncated Ground Plane for Wi-Fi, WLAN and Wi-MAX Applications.: International Conference on Open Source Systems and Technologies, (2014)

OnLight Information Broadcasting in Exhibitions Using Li-Fi

Suchit Purohit, Uma Tolani and Siddhi Goswami

Abstract Visible light communication has come a long way from its use in traffic signals, marine signals and photo phone since Herald Haas demonstrated concept of technology which can communicate as well as illuminate, referred to as Li-Fi or Light Fidelity. Li-Fi emerged as a solution to the growing congestion problem on existing radio spectrum used by Wi-Fi. It offers inherent advantages like security, nonhazardous, availability, bandwidth, efficiency, and SPEED. Li-Fi has come a long way offering numerous applications in varied areas like intelligent transport system, underwater communication, traffic management, disaster management, smart lights, and data transmission in petrochemical industries, hospitals, and aircrafts. This paper presents an application of Li-Fi technology with augmented reality providing OnLight data communication to facilitate the information broadcasting of the exhibits in an exhibition to the mobile phone of the visitor. The proposed model consists of LED lights installed besides the exhibit and a photoreceptor installed at the mobile phone. As soon as the visitor aligns its mobile phone to the exhibit, all the supplementary information about it in the form of text, images, or videos gets downloaded into it. The proposed model offers faster transmission of data with no interference between devices and with other devices using radio waves. The transmission can be accessed anywhere with no dead zones which exists in its counterpart Wi-Fi. Above all it also provides energy friendly illumination because the LEDs would also provide illumination. The model can be used to identify the most and least accessed exhibition areas and items which would help in administrative decision.

Keywords Radio communication · Visible communication · Li-Fi · Augmented reality

S. Purohit (✉) · U. Tolani · S. Goswami
Department of Computer Science, Gujarat University, Navrangpura, Ahmedabad, Gujarat, India
e-mail: suchitpurohit@yahoo.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_14

1 Introduction

The advent in technology and rapidly growing world has shown a drastic increase in the number of mobile Internet users and desktop Internet users from 5.27 billion in year 2010 to 7.27 in year 2016 and is further expected to increase to 9.03 billion in 2020 [1]. In such a scenario problem of spectrum congestion is arising in existing wireless transmission based on radio waves and microwaves. Moreover, the radio communication is limited in capacity, efficiency, availability, and security [2]. The obvious solution is to shift to higher frequency bands like infrared and visible band of the electromagnetic spectrum for transmission of data giving rise to a branch of communication referred to as VLC or Visible Light Communication. Due to safety regulations at high power, infrared cannot be used for transmission over longer distances and UV rays also causes health impairments therefore visible spectrum is the best and only available choice as an alternative to radio communication [3].

VLC refers to communication using an illumination source which provides illumination as well as communication [4]. It can send information using light-signals. The signals are sent by modulating them in ON OFF patterns to transmit 0 and 1. The sources of light used in VLC can be florescent bulbs, incandescent bulbs, lasers, or LEDs [5]. Incandescent lights cannot sustain quick switching in ON and OFF pattern to modulate 0 and 1. In contrast, LED can be fluctuated with high frequency as it is made up of semi-conductor material. LED is also known as green lightning resource because it is energy efficient and does not contain hazardous material like mercury emitted by florescent lamps. Hence, LED has an edge over other sources for VLC [5].

In 2011, Harald Haas from University of Edinburgh, UK, demonstrated VLC through LED evolving a technology called Li-Fi which abbreviates to "LIGHT FEDILITY." He demonstrated a Li-Fi prototype at the TED Global conference in Edinburgh. In this demonstration, he used a LED bulb to transmit a video of a blooming flower which was then projected onto a screen. During the talk, he frequently blocked the light from the LED with his hand to show that the LED was undeniably the source of the video data. He showcased that if the LED is on, 1 is transmitted and if it is off a 0 is transmitted [4]. Since its inception, numerous applications of Li-Fi have been proposed like smart street light communication [6], data transmission in petrochemical industries [6], underwater communication [7], traffic management [8], disaster management [9], hospitals [10], and aircrafts [11].

In this paper a novel application of Li-Fi providing Augmented Reality is proposed. The proposed model is to be used in exhibitions where the information about the exhibits is in static form provided to the user either verbally or on paper. Our proposed model presents a novel solution to this by providing the broadcasting of information regarding the exhibit in form of document files, images, or multimedia content to be downloaded on the user's mobile phone. The proposed model consists of exhibit incorporated by a LED light source connected to an augmented reality server. As soon as the user reaches the exhibit, the data of the exhibit is transmitted via LED offering a Li-Fi communication.

The following sections include introduction and working principle of Li-Fi and the architecture of proposed model.

1.1 Li-Fi

"The light from light emitting diodes (LED's) is used as medium to deliver networked, mobile, high speed communication" [12]. This technology is referred to as Li-Fi or Light Fidelity. In this technology, the data is transmitted through a LED bulb which is flickered at high frequency, imperceptible to the human eye.

The issues with the current radio communication systems utilizing radio and microwaves have motivated the need and evolution of this technology. Some of them are given below.

1.2 Capacity

Radio spectrum has limited bandwidth and is very expensive and due to increasing growth rate in the number of mobile and Internet users; the problem of lack of capacity for catering to demands of exponentially growing number of users is being faced [2]. On the other hand, Li-Fi needs no licensing and offers a low-cost solution to the existing radio communication problem. Though the installation cost is very high but maintenance cost is very low and use of LED also has low-electricity cost and long lasting life hence saving the money [13].

1.3 Availability

Availability of radio waves is a major concern. The usage of devices using radio waves is prohibited in places like airplanes and petrochemical industries and hospitals where radiation could possibly result into negative consequences [2] wherein Li-Fi which uses visible spectrum can also be installed into these restricted areas as the visible light has no harmful effects on the surroundings as well as they do not pose any threat of interference with the surrounding radio communication waves [13].

1.4 Security

In radio communications, routers are the main source of security breach and radio waves can travel large distances, transmit and penetrate through walls. Therefore, they can be intercepted and interpreted and are vulnerable to many security threats [2].

The light waves used in Li-Fi do not penetrate through the walls hence offering a lock-tight security [13].

1.5 Speed

Wi-Fi can transmit data at 150 mbps of speed while Li-Fi can transmit data far more than 10 gbps [10].

There are many choices available for visible light communication like florescent bulb. Incandescent bulbs, Lasers and LEDs of the available choices, Fluorescent Bulb contains gases such as mercury, neon, argon, xenon which is harmful, [5] Incandescent Bulb contains a metal called Tungsten which radiates heat when heated by electrical energy [14]; hence, it cannot sustain quick flickering required for data transmission. Laser requires line-of-sight [14]. LED stands for Light Emitting diode. LEDs are also known as green lightening resource because they are energy efficient and do not contain hazardous materials such as mercury emitted by florescent lamps. The significant feature which makes it best choice for Li-Fi is its ability to be fluctuated with high frequency. Significant development in aluminum, gallium has also facilitated production of colored LEDs [5]. Colored LEDs can be used to increase the data rate by sending the data on different channels using different colors [5]. A microchip can be added to any LED bulb which can be used to blink it ON and OFF. Researchers are designing micron-sized LEDs which could flicker on and off 1000 times faster than LEDs which would facilitate faster data transfer. Moreover, 1000 micron-sized LEDs can fit into area required by 1 mm^2 large single LED. A 1 mm^2 sized set of micron-sized LEDs could hence communicate million times as much information as a single 1 mm LED [8].

Working Principle of Li-Fi

The main components of Li-Fi system are as follows:

(a) A LED lamp which acts as transmission source.
(b) A photodiode as the receiving element.

LEDs can be switched on and off to produce digital strings of various sequences of 1 and 0 s. To produce a new data stream, data has to be encoded in the light by changing the flickering rate of the LED. This flickering of LED is so fast that the human eye fails to perceive it. Photodiodes at the receiving end, detect this flickering which is then converted into 0 and 1 s. This data is processed by the receiver's application and decoded into data stream which then appears on the receiver's device [15].

1.6 Augmented Reality

Augmented reality is a live direct or indirect view of physical real-world environment whose elements are augmented (or supplemented) by a computer generated sensory input such as sound, video, and graphics. Augmented reality is finding its way in many applications like medical, manufacturing and repair, annotation and visualization, robot path planning, military aircrafts, entertainment [16]. In exhibitions, it is necessary to provide information about the exhibits to the visitors. Through, Augmented Reality, it is possible to provide the information about the exhibit which is not directly obtained by looking at it [17].

1.7 Proposed Work

Motivated from the promising behavior of Li-Fi, this paper presents an application model facilitating an OnLight data communication to broadcast the information and augmented data about the exhibits to the mobile phone of the visitor. The proposed model consists of LED lights installed besides the exhibit and a photoreceptor installed at the mobile phone. As soon as the visitor aligns its mobile phone to the exhibit, all the supplementary information about it in the form of text, images or videos gets downloaded to the phone via an application installed on it.

1.7.1 Advantages of Proposed Prototype

This prototype enables energy friendly illumination since LEDs would provide illumination along with faster transmission of data with no interference between devices. Since LEDs can be used anywhere there will not be any problem of dead zones. Moreover, using this prototype most and least accessed exhibits can be identified by analyzing the number of downloads of information pertaining to different exhibits.

References

1. Statistica. www.statistica.com.
2. Vamshi Krishna Sai Nagabandi, Santosh Kumar. K A. Anvith Raj.: Li-Fi (Light-Fidelity) Technology Transmission of data through light.
3. Nikolaos Kourkoumelis., Margaret Tzaphlidou.: Eye Safety Related to Near Infrared Radiation Exposure to Biometric Devices. The Scientific World Journal, vol. 11, pp. 520–528, (2011).
4. PureLifi. http://www.purelifi.com.

5. Sivaranjani. R., Nagasundari. G., Stella. K.: Eco-Friendly Data Transmission Through Li-Fi Technology, in International Conference on Current Research in Engineering Science and Technology, (2016).
6. Abhinav Malik., Shreyaa Nagpal., Dr. Naveen Rathee.: Transmission of Numeric Data and Voice Using Light Fidelity (LIFI) Technology. International Journal for Research in Applied Science & Engineering Technology, (2014).
7. Jeslin Johnson Aman Sodhi.: Light Fidelity (LI-FI) - The Future of Visible Light Communication. International Journal of Engineering Research and General Science, vol. 3, no. 2, (2015).
8. Prof. Shalabh Agarwal, Dr. Asoke Nath Anurag Sarkar.: Li-Fi Technology: Data Transmission Through Visible Light. International Journal of Advance Research in Computer Science and Management Studies, vol. 3, no. 6, (2015).
9. Balakrishnan. S., Karthika. R.: Wireless Communication using Li-Fi Technology, SSRG International Journal of Electronics and Communication Engineering (SSRG-IJECE), vol. 2, no. 3, (2015).
10. Sakshi Jain., Dinesh Khandal.: Li-Fi (Light Fidelity): The Future Technology in Wireless. International Journal of Information & Computation Technology, pp. 0974–2239, (2014).
11. Prerna Chauhan., Ritika Tripathi., Jyoti Rani.: Li-Fi (Light Fidelity)-The future technology In Wireless communication. International Journal of Applied Engineering Research, vol. 7, no. 11, (2012).
12. Varsha Kapil., Prabhakar Rai., Harish Kumar Saini., Vaibhav Rai.: Li-Fi (Light Fidelity) Future of Wireless communications," Journal of Mechanical and Civil Engineering, vol. 13, no. 4, pp. 06–09, (2016).
13. Ravi Ramchandra., Nimbalkar Dhakane., Vikas Nivrutti.: Light-Fidelity: A Reconnaissance of Future Technology. International Journal of Advanced Research in Computer Science and Software Engineering (IJARCSSE), vol. 3, no. 11, (2013).
14. Molecular Expressions. http://micro.magnet.fsu.edu.
15. Vitthal S Saptasagar.: Next of Wi-Fi an Future Technology in Wireless Networking Li-Fi Using Led Over Internet of Things. International Journal of Emerging Research in Management and Technology, vol. 9359, (2014).
16. Ronald T. Azuma.: A Survey of Augmented Reality. Presence: Teleoperators and virtual environments, vol. 6, no. 4, pp. 355–385, (1997).
17. Winson Tan, Dinosaur in Penang Augmented Reality Dinosaur in Penang Museum Playme AR, (2014).

EEG Signal Analysis for Mental States and Conditions of Human Brain

Sk. Ebraheem Khaleelulla and P. Rajesh Kumar

Abstract In the field of medical science, the EEG signal is a tool for measuring the brain activity which reflects the condition of the brain. The electrical activity in brain using small, flat metal discs (electrodes) attached to the scalp is detected by a test called EEG (Electro Encephalogram). The main aim of this thesis is to help the doctors by reducing the time complexity in analyzing EEG signal which produces better results. Brain cells communicate through electrical impulses are active all the time, even when asleep or awake. The brain signals can be analyzed by using five bands of frequency which are namely alpha, beta, gamma, delta, and theta. Each band has a respective frequency range, which determines mental states and condition of human activities. Different activities of the brain will generate different EEG signal. Transform domain techniques like Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT), and Wavelet transforms are used to determine the frequency value of each frequency band. The exact mental state and conditions of the brain such as sleep, drowsiness, stress, and mental ability can be determined. A total of 12 EEG signals are taken from MIT-BIH EEG scalp database and the approach is implemented in MATLAB (R2014a) software.

Keywords Electro encephalogram · Bi-orthogonal wavelet · Fast Fourier transform

Sk. Ebraheem Khaleelulla (✉) · P. Rajesh Kumar
Department of ECE, Andhra University, Visakhapatnam, India
e-mail: ebraheemphd@gmail.com

P. Rajesh Kumar
e-mail: rajeshauce@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_15

1 Introduction

EEG or brain signals are the electrical activity of brain. Commonly, the EEG waves range from 0.5 to 500 Hz. Six frequency bands exists in brain signals, which are mentioned as beta band, alpha band, theta band, gamma band, delta band, and mu band. Delta waves frequency is from 0.5 to 3 Hz. It is the dominant rhythm during deep or dreamless sleep. Theta waves frequency ranges from 4 to 7 Hz. It is slowest wave and is the dominant rhythm in adults. It normally occurs during closure of eyes and disappears when eyes are opened. Alpha waves normally observed in adults which have a frequency between 7 and 12 Hz [1].

In the occipital region alpha activity occurs. It is regarded as a normal waveform. Beta wave has frequency ranges from 13 to 30 Hz. It is the dominant rhythm during alert or anxious states. It is usually observed from the frontal and central portions on the brain. It is generally a normal rhythm and is observed in all age groups. Gamma wave is fastest wave of brain and having a frequency ranges from 30 to 45 Hz and is normally called as fast beta wave but its presence is rarely felt. These waves occur in front central part of brain. EEG signals can be captured using various techniques.

After assigning electrodes on the scalp, EEG recording is obtained. By preparing the scalp part by light absorption, a conductive gel or paste is applied to decrease impedance due to gone skin cells. A separate wire is used to attach the electrodes used by many organisms. When high density arrays of electrodes are needed, some organisms use nets into electrodes which are embedded.

The EEG which is recorded from many electrodes is arranged in a particular montage or pattern. An international 10/20 system also known as common standard is used. These cheap methods give a continuous record of brain activity. They have better than millisecond resolution. High temporal resolution is achieved by this tool, hence detailed properties of dynamic cognitive techniques are explained using ERP (Event Related Potentials) and EEG methods [2–4].

2 Methodology

2.1 EEG and Variables

The state of brain is monitored using a dynamic and noninvasive technique called EEG (Electro Encephalogram). Its main advantage is it indicates the brain's function instantaneously and continuously.

The EEG signal can be recorded by placing electrodes on the scalp, which consists of various waves with different characteristics. The entire scalp is distributed with an array of electrodes for longer than 24 h. EEG signals can be recorded continuously from many channels. Electrode counts have clinical uses like monitoring casual wakefulness and situations involving coma or seizure. Electrical

activity from the scalp is recorded by EEG. For nearly a century, this activity has been used as a clinical diagnostic tool.

An important position is possessed by the scalp EEG as a research and diagnostic tool due to four main characteristics. They are:

- It is inexpensive and simple to record
- It has more time resolution
- It is noninvasive.

By using this technique, the dynamics of brain activity can be monitored with the help of freely moving subject. It is a popular clinical technique that provided important information about a variety of brain disorders which included epilepsy or seizure disorders, coma, encephalopathy, brain death, and sleep disorders. It is a primary method for diagnosing focal brain disorders, strokes, and tumors. It is inexpensive, noninvasive, and has a superior temporal resolution compared with imaging techniques such as PET (Positron Emission Tomography) and MRI. To describe these EEG wave patterns, a standard terminology is used.

The terms conclude the electrocerebral activity and abnormal activity or transient activity in each region of the brain. The terms are the following:

- Voltage
- Transient
- Periodicity
- Frequency
- Attenuation
- Morphology.

2.2 *Frequency Domain Analysis*

In analyzing time domain functions, various mathematical transforms are used which are referred as frequency domain methods. The most commonly used transforms are as follows:

i. Discrete Fourier Transform (DFT)
ii. Fast Fourier Transform
iii. Wavelet Transform.

The DFT changes a sequence of equally spaced samples into a list of finite combination of complex sinusoids. It transforms a sampled function from its domain to frequency domain.

The FFT algorithm executes the DFT of sequence or its inverse. A signal from its original domain is changed to its frequency domain and vice versa using Fourier analysis.

The wavelet transform [5] is arising technique for signal processing. This is used to illustrate nonstatic real-life signals which are highly efficient. A signal is decomposed into a set of basic functions using this transform, such functions are called wavelets. Grossman and Morlet were the first people to describe wavelets in the literature works. A wavelet is a limited duration waveform having zero average value. Wavelets have ideal property to compact signal representation and orthogonality by dilations and shifting. Wavelets are extracted from a single prototype wavelet called mother wavelet. By using wavelets, an image can be converted into series of wavelets which can be stored more efficiently than pixel blocks. The wavelet transform can offer some information on frequency and time domain simultaneously. The time-domain signal is processed through low and high pass filters, respectively, to extract low and high frequency information in this transform. This process is repeated several times, each time a part of signal is extracted.

In general, Every analog signal x(t) with finite energy can be decomposed into a sum of shifted and dilated wavelet function Ψ(t) and shifted scale function Φ(t) as shown in Eq. 1.

$$x(t) = \sum_{m=-\infty}^{\infty} c(m)\varnothing(t-m) + \sum_{j=0}^{\infty}\sum_{m=-\infty}^{\infty} d(j, m)2^{j/2}\varnothing(2^j t - m), \tag{1}$$

where c(m) is scale coefficients and d(j, m) wavelet coefficients. Scale and wavelet coefficients are calculated using scalar products.

$$c(m) = \int_{-\infty}^{\infty} x(t)\varnothing(t-m)dt \tag{2}$$

$$d(j, m) = 2^{j/2}\int_{-\infty}^{\infty} x(t)(2^j t - m)dt. \tag{3}$$

Because of a numerous advantages obtained by this approach, many practical tests are reported to use wavelet transform for steganography. The capacity and robustness of the information hiding system features, the use of such transform is mainly addressed.

2.3 Bi-orthogonal Wavelet

A wavelet whose wavelet transform is invertible but not necessarily orthogonal is known as bi-orthogonal wavelet [6]. Symmetric wavelet functions can be constructed with an additional degree of freedom by using bi-orthogonal wavelet.

Two scaling functions, present in bi-orthogonal case which generates different multi-resolution analysis, as per these two different wavelet functions are generated.

So the coefficients of the scaling sequences M and N may differ. They must satisfy the following biorthogonality condition shown in Eq. 4

$$\sum_{n \in Z} a_n \tilde{a}_{n+2m} = 2.\delta_{m,0}. \tag{4}$$

It is commonly known there is no need Bases that span a space to be orthogonal. In order to have further flexibility in wavelet bases construction, the orthogonal condition is relaxed allowing semi-orthogonal, bi-orthogonal, or nonorthogonal wavelet bases. The families of compactly supported symmetric wavelets include bio-orthogonal wavelets. As it results in the linear phase of transfer function, the symmetry of the filter coefficients is offer desirable. In bi-orthogonal case, it is

Table 1 Frequency bands and corresponding states

Brain wave type	Frequency range (Hz)	Mental states and conditions
Delta	0.5–3	Deep, dreamless sleep
Theta	4–7	Fantasy, imaginary dream
Alpha	8–12	Relaxed but not drowsy
Low beta	13–15	Formerly MR
Midrange beta	16–20	Thinking, aware of self & surroundings
High beta	21–30	Alertness, agitation
Gamma	30–100	Motor functions, higher mental activity

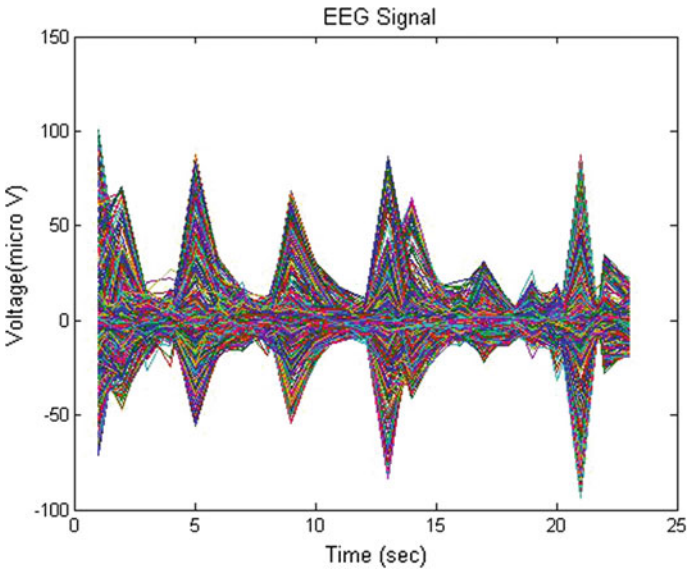


Fig. 1 Input EEG signal

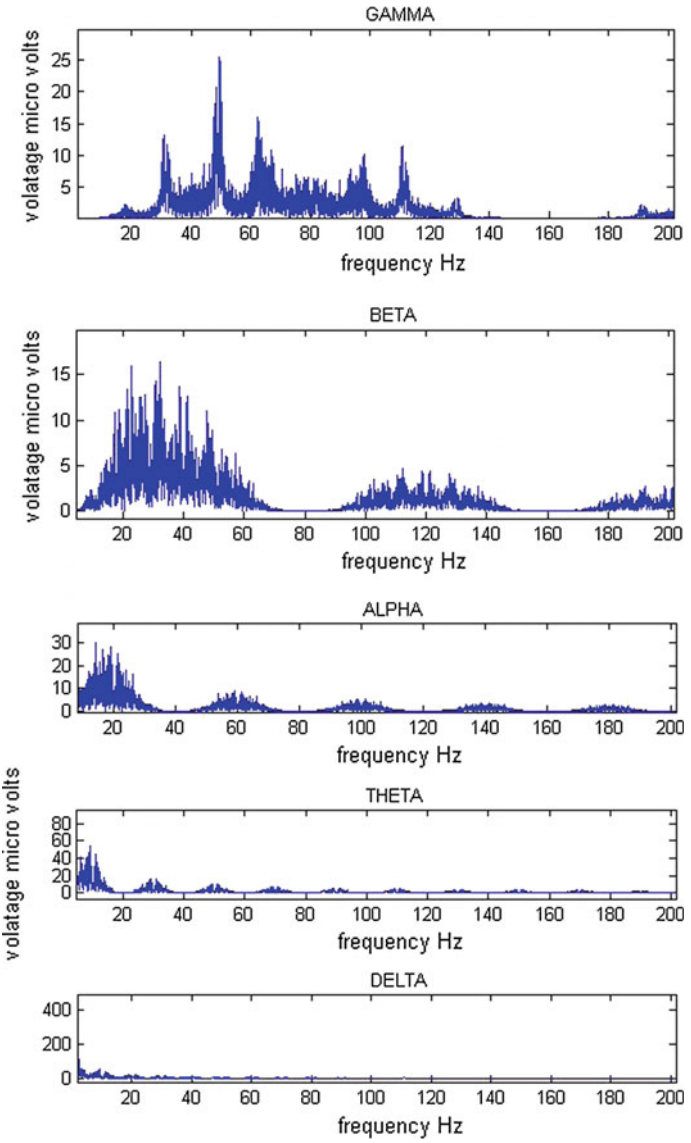


Fig. 2 Biopotentials of α, β, γ, Δ, θ

Table 2 Frequency values

Frequency band	Frequency value (Hz)
Γ	29.30
B	32.30
A	13.869595
Θ	9.0000
Δ	1.00000

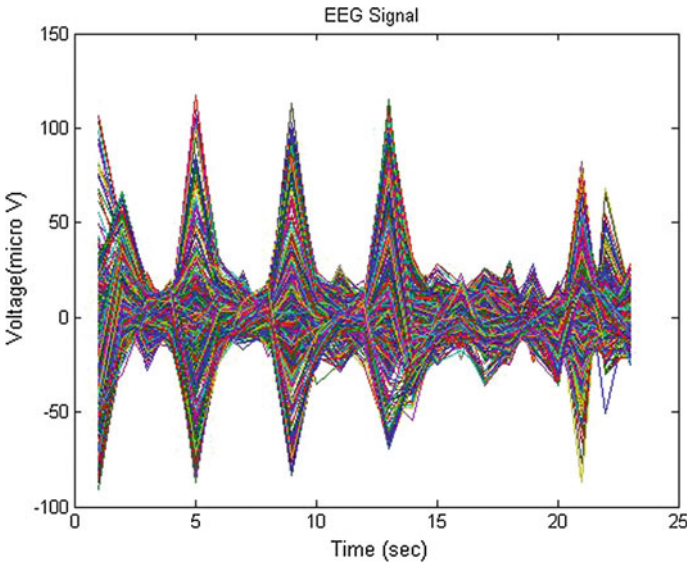


Fig. 3 Input EEG signal

having two scaling functions, which help to generate various multi-resolution analysis. The wavelet functions and dual scaling have the following properties:

1. The associated filters are symmetrical.
2. They are zero outside of a segment.
3. The functions used in Daubechies wavelets are more complex than the functions used in bi-orthogonal wavelet.
4. The calculation algorithms are very simple (Table 1).

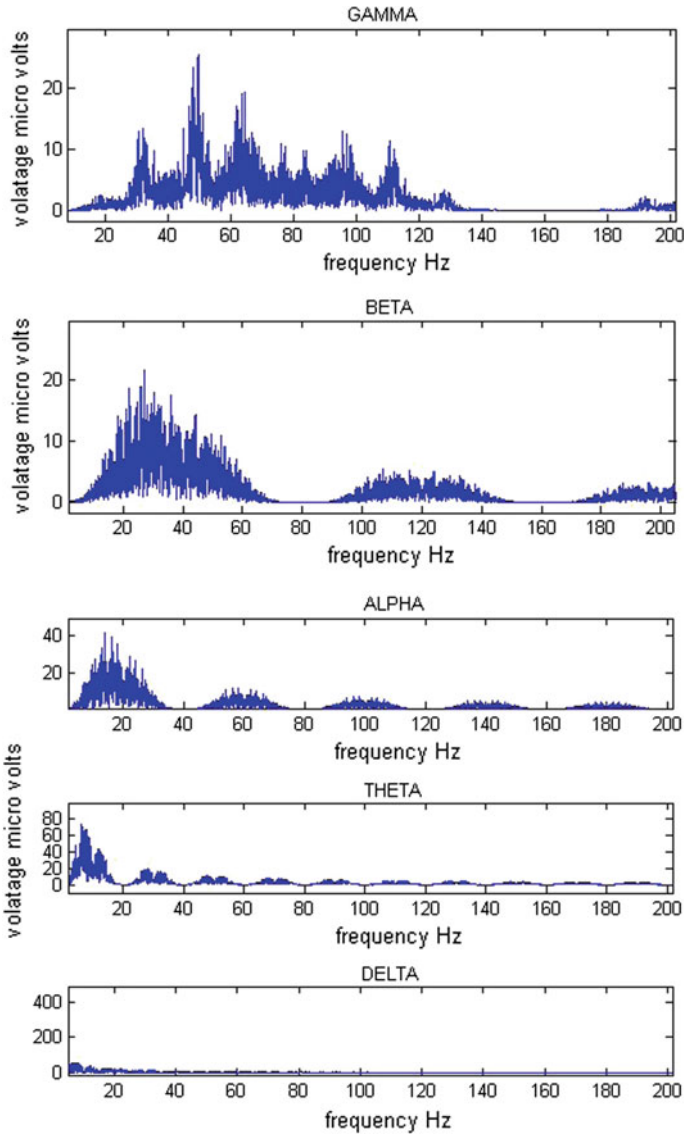


Fig. 4 Biopotentials of α, β, γ, Δ, θ

Table 3 Frequency values

Frequency band	Frequency value (Hz)
Γ	49.48
B	31.13
A	13.739130
Θ	3.782609
Δ	0.4608696

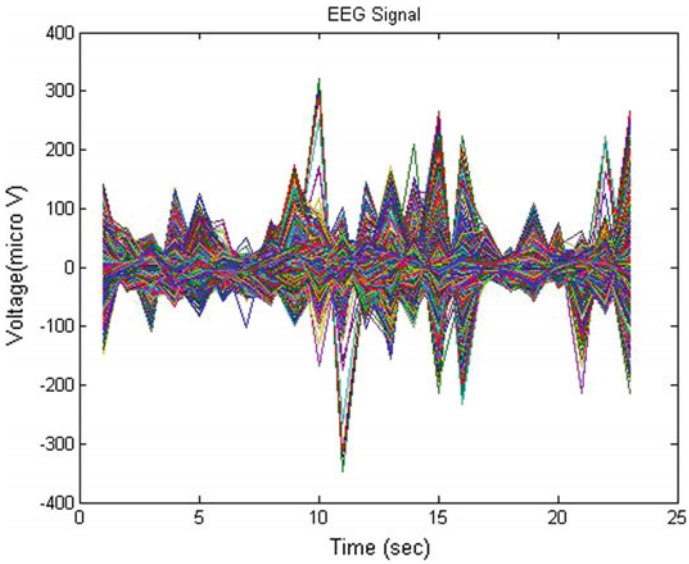


Fig. 5 Input EEG signal

3 Results and Discussions

The EEG input signal data base has been taken for different 12 cases, i.e., from 22 subjects (5 males, ages 3–22; and 17 females, ages 1.5–19). Each case (chb01, chb02, etc.) contains five frequency bands with different values. Based on the values of the frequency bands, we can state the condition of the human brain activity of each case. The results are as follows:

Result 1: Based on the Input signal chb04_01_edfm.mat. The values for frequency bands are as follows (Figs. 1, 2 and Table 2).
Result: From the above values and figures the state of BRAIN is with DEEP DREAMLESS SLEEP WITH HIGH MENTAL ACTIVITY.
Result 2: Based on the Input signal chb07_01_edfm.mat. The values for frequency bands are as follows (Figs. 3, 4 and Table 3).
Result: From the above values and figures, we obtain the state of BRAIN is with HIGH MENTAL ACTIVITY WITH ALTERNESS.

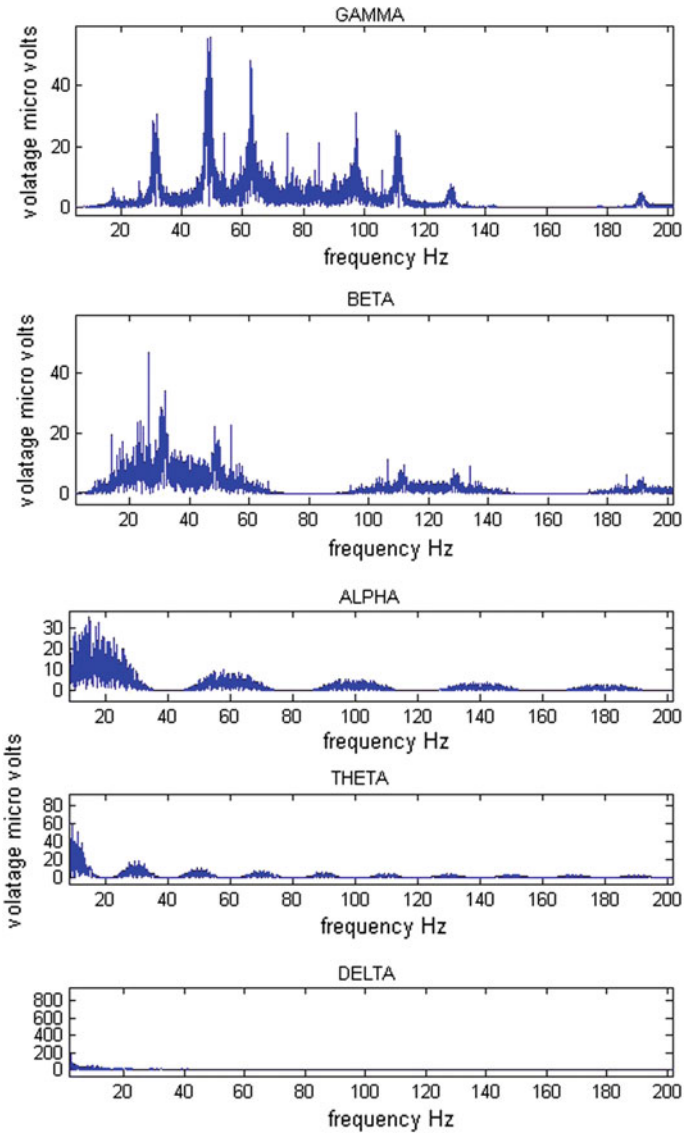


Fig. 6 Biopotentials of α, β, γ, Δ, θ

Result 3: Based on the Input signalchb08_01_edfm.mat, the values for frequency bands are as follows (Figs. 5 and 6 and Table 4).
RESULT: From the above values and figures, the state of BRAIN is with ALTERNESS ALIGATION.

Table 4 Frequency values

Frequency band	Frequency value (Hz)
Γ	29.43
B	26.09
A	14.434783
Θ	7.608696
Δ	0.478261

4 Conclusion

The proposed paper enables us to analyze the normal human brain activity by using various frequency bands namely alpha, beta, gamma, delta, and theta. By identifying the values of each band which has different frequency range for each frequency bands which reflects the particular condition and state of brain. In this paper various samples of data are considered from human brains, this data samples are analyzed using various transform techniques using MATLAB R2014a platform to determine the frequency value of each frequency band.

The stimulated results obtained determines the exact state and condition of brain such as sleep, drowsiness, fantasy, thinking, by comparing values with the predefined values. This thesis helps in real-life applications by helping the doctors in reducing the time complexity by analyzing the state and condition of human brain using EEG signal.

References

1. Duffy, F.H., Hughes, J.R., Miranda, F., Bernad, P., Cook, P.: Status of Quantitative EEG (QEEG) in Clinical Practice, 1994. Clinical EEG and Neuroscience. 25 (1994) 6–22.
2. Bono, V., Biswas, D., Das, S., Maharatna, K.: Classifying human emotional states using wireless EEG based ERP and functional connectivity measures. 2016 IEEE-EMBS International Conference on Biomedical and Health Informatics (BHI). (2016).
3. Mir, H., Prasad, I., Yu, K., Thakor, N., Al-Nashash, H.: ERP signal estimation from single trial EEG. 2014 36th Annual International Conference of the IEEE Engineering in Medicine and Biology Society. (2014).
4. Zakeri, Z., Samadi, M.R.H., Cooke, N., Jancovic, P.: Automatic ERP classification in EEG recordings from task-related independent components. 2016 IEEE-EMBS International Conference on Biomedical and Health Informatics (BHI). (2016).
5. Qin, X.-B., Zhang, Y.-Z., Huang, M.-T., Wang, M.: EEG Signal Recognition Based on Wavelet Transform and Neural Network. 2016 International Symposium on Computer, Consumer and Control (IS3C). (2016).
6. Jichang, G., Jianfu, T., Qiang, L., Yaqi, Z.: The de-noising of gyro signals by bi-orthogonal wavelet transform. CCECE 2003 - Canadian Conference on Electrical and Computer Engineering. Toward a Caring and Humane Technology (Cat. No.03CH37436).

Framework for Classifying Cardiac Arrhythmia

G.V. Sridhar and P. Mallikarjuna Rao

Abstract Cardiac Arrhythmia is caused by irregular heart rhythms, it is either increased or decreased leading to irregular rhythms. The heart arrhythmia is assessed using electrocardiogram (ECG). ECG can clearly detect various types of arrhythmia and correspond to diagnosis of heart disease. There is extensive research involved in removing manual intervention in assessing the type of arrhythmia from the ECG. Arrhythmia can be classified by extracting attributes in the form of RR interval from ECG. This work proposes an approach to classify cardiac arrhythmia. A range of classifiers are proposed such as Chi-square Automatic Interaction Detector (CHAID), Random Forest (RF), and fuzzy classifier. Initially, the attributes are retrieved from the time series present in ECG data employing Discrete Cosine Transform (DCT) and then the distance among RR waves are processed. The dataset used for experimental purpose were obtained from Massachusetts Institute of Technology-Boston's Beth Israel Hospital (MIT-BIH) arrhythmia to evaluate the performance of the method.

Keywords Cardiac arrhythmia · Electrocardiogram (ECG) · RR interval · Discrete cosine transform (DCT) · Chi-square automatic interaction detector (CHAID) · Random forest (RF) · fuzzy classifier

1 Introduction

In the recent times, there are relatively more deaths globally caused due to cardiovascular diseases. The ECG signal is a significant tool in clinical practice as it accurately assesses the cardiac status of patients. The potential difference between

G.V. Sridhar (✉)
Department of ECE, Avanthi Institute Of Engineering & Technology,
Vizianagaram, AP, India
e-mail: sridhar1209@gmail.com

P. Mallikarjuna Rao
Department of ECE, AU College of Engineering (A), Visakhapatnam, AP, India

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_16

two points on the body surface with respect to time emits as ECG signal and is very useful in identifying and clarifying various cardiac arrhythmias. The process is considered to be tedious as ECG contains huge data along with different type of noise. In addition, manual analysis is time consuming and is prone to errors. These aspects necessitate automatic analysis of the extracted features from ECG signals [1, 2]. If the electrical activity of the heart is abnormal, i.e., if it is faster or slower or any other abnormal condition is referred as Cardiac Arrhythmia (dysrhythmia). They cause the heart to pump blood less effectively. The working of heart slows down during an arrhythmia and pumps less amount of blood. There is decreased blood flow throughout the body, damaging the brain, heart or other organs. Though some of the arrhythmias are not fatal, ventricular arrhythmias can cause cardiac arrest.

Consequently, detecting abnormal life-threatening cardiac rhythms (Arrhythmias) are clinically significant as it has to be investigated. Ventricular Fibrillation (VF) and Ventricular Tachycardia (VT) are acute ventricular arrhythmias. On the last decade, there was significant importance for early detection and treatment of arrhythmias but now the emphasis has changed from resuscitation to aggressive Defibrillation therapy [3].

The basic requirements for assessing arrhythmia are identifying the spot at which there is disturbance in conduction, checking whether atrial and ventricular rhythms are present and also the connection between the atrial and ventricular impulses [4].

The human heart beats are varying bio-potential signals and these are recorded as ECG. This is conducted by placing electrodes on the skin of the user to detect the bioelectric signals produced by the heart. These signals reach the skin surface and are captured as ECG signals. Information regarding heart and vascular condition can be obtained from these signals and are used in enhancing the user's quality of life with suitable treatment. ECG proves to be a matchless tool in diagnosing heart conditions. The patterns recorded in the ECG waveform are made to distinct electrical depolarization–repolarization pattern that correspond to individual heart beat with respect to time [5].

ECG is one among the ways to detect heart diseases. P wave, Q wave, R wave, S wave (QRS) complex and T wave forms the ECG signals. The wave forms are represented with capital letters P, Q, R, S, and T. If the heart beat is normal then, the important metrics in the waveform such as the shape, the duration, and the relationship with each other of P wave, QRS complex, and T wave components and RR interval are examined. Arrhythmia corresponds to all abnormal heart beats and some of them are fatal. Recently, the ECG signals are interpreted automatically. Furthermore, arrhythmia is detected using computer-based interpreter systems that can with time and also several approaches be applied to these systems. Most importantly artificial neural network is applied (ANN) [6].

The life of the patient with arrhythmia can be prolonged if the disease is detected at an early stage itself. Hence many techniques are needed to examine ECG signals to detect the heart diseases. The ECG waveform depicts cardiac health with vital features that correspond to the nature of heart disease. The electronic activities of the heart are recorded as ECG signals to detect cardiac arrhythmia. ECG is a widely accepted tool in detecting heart diseases. Several methods are now available to

classify cardiac arrhythmia but yet they are less accurate as they depend on feature extraction of ECG [7].

The below sections illustrates as follows: Sect. 2 analyses the related work in the literature. Section 2 describes the technique used in the suggested work. Section 3 discusses the experiment results and Sect. 4 concludes the proposed work.

2 Methodology

This section, proposes investigation on classification accuracy of CHAID, RF, and fuzzy classifier for a given ECG data. The DCT feature extraction is used to convert the time series data obtained from MIT-BIH into frequency domain. For classification, two types of arrhythmia namely Left Bunch Bundle Block (LBBB) and RBBB are taken into consideration. Many distinct features are incorporated in the datasets that are used in evaluating automated classification of ECG signals. The MIT-BIH database is one among the popular and effective databases used in detecting and classifying arrhythmia. In this work, the suggested approach is assessed using the MIT-BIH database.

2.1 Massachusetts Institute of Technology-Boston's Beth Israel Hospital (MIT-BIH) Arrhythmia Database

Initially only the MIT-BIH Arrhythmia Database was available as a standard test material to assess arrhythmia detectors. This database was also used for researching basic cardiac dynamics in about 500 sites globally from the year 1980. The MIT-BIH Arrhythmia Database was completed in 5 years. Elemental tools were used to create the database according to the current standards. Del Mar Avionics model 445 two-channel reel-to-reel Holter recorders are used in recording ECG signals and Del Mar Avionics model 660 playback unit is used in recreating analog for digitization. A major portion of MIT-BIH Arrhythmia Database is accessible via PhysioNet thus benefitting students and others to use the database for cost-free studies.

ECG datasets signals for training/testing are collected from MIT-BIH arrhythmia database. Selected arrhythmias include LBBB, RBBB, and Normal. Each ECG beat used is a matrix (275×1) for ECG lead. For interpretation purpose every ECG signal has five clear points (P, Q, R, S, and T).

2.2 RR Interval

Arrhythmia beat-by-beat classification is carried out using a set of rules based on RR interval signal. Depending on clinical procedures, the medical experts frame

rules to detect arrhythmic events from RR intervals [8]. These rules are applied in classifying middle RR interval of a three RR interval sliding window. Classification involve second beat of middle RR interval. There are three categories for beat namely (1) Normal sinus beats (N) and two arrhythmic ones, (2) LBBB and (3) RBBB.

This work uses RR interval to identify arrhythmia. The RR peaks are detected as follows:

- Six records are used in computing the moving signal average.
- New signals are obtained by deducting moving average from original signal
- 'R' signal peak is identified
- With relative position, P, Q, R, S, and T peaks are found.

Peak amplitude is calculated from 'k' line and is given by (1)

$$k = Max(\theta_i,\ i = 1,\ 2,\ \ldots,\ 11) + c, \tag{1}$$

where, θ_i is the greatest amplitude, type of heartbeat and 'c' is a constant.

The intervals between successive QRS detection points are represented by RR intervals.

2.3 Discrete Cosine Transform (DCT)

DCT [9] changes time series signal into basic frequency components. Forward Discrete Cosine Transform (FDCT) disintegrates an image into a set of cosine basis functions and process of reconstructing is called IDCT.

The FDCT of a list of n real numbers s(x), x = 0…n−1, is the list of length n given by (2)

$$S(u) = \sqrt{2/n} C(u) \sum_{x=0}^{n-1} s(x)\ \cos \frac{(2x+1)u\pi}{2n}, \tag{2}$$

where $C(u) = 2^{-1/2}$ for u = 0 or otherwise $C(u) = 1$

The constant factors are chosen so that the basis vectors are orthogonal and normalized.

The Inverse Discrete Cosine Transform (IDCT) in Eq. (3)

$$S(x) = \sqrt{2/n} \sum_{x=0}^{n-1} C(u) s(u)\ \cos \frac{(2x+1)u\pi}{2n}, \tag{3}$$

where $C(u) = 2^{-1/2}$ for u = 0 or otherwise $C(u) = 1$

2.4 Chi-Square Automatic Interaction Detector (CHAID)

The relationship among the variants can be established through CHAID, decision tree technique. CHAID examination identifies how the variables combine to detail the result in given dependent variables. CHAID examination uses categorical or ordinal data. In the course of examination, the CHAID technique modifies the continuous data into ordinal data. In CHAID technique, it is possible to visualise the association among the variants and its related factor with a tree. The solution in majority of the surveys is categorical solution as an alternative to a continuous value. To identify the relationship among the categorical values is considered be a tedious task. Using CHAID technique the survey-related queries can be answered effectively. A decision tree or a classification tree is generated during CHAID analysis. On identifying the target variable or dependant variable the process of analysis is initiated. The CHAID algorithm accepts barely the nominal or ordinal categorical predictors. The predictors are analyzed before using it and if they are found nonstop, it is transformed into ordinal predictors. There are three phases in CHAID algorithm namely merging, splitting, and stopping. A tree is grown by frequently using the three stages on each node initiated from the root node [10].

Binning Continuous Predictors: For a given set of break points $a_1, a_2, a_3, \ldots, a_{K-1}$ arranged in ascending order, the given X is represented as category C (X) as (4)

$$C(x) = \begin{cases} 1 & x \le a_1 \\ k+1; & a_k < x \le a_{k+1},\ k = 1, \ldots, K-2 \\ K & a_{K-1} < x \end{cases} \tag{4}$$

Merging: The nonsignificant categories are merged for every predictor variable X. If X splits the node, each resultant category of X will result in one childnode. The merging step also evaluates the modified p-value that is to be used in splitting.

The p-value is calculated depending on the type of dependent variable. In the step where merging takes place, CHAID needs the p-value for a pair of X categories and occasionally needs the p-value for each category of X. Whenever a p-value for a pair of X categories is necessary then only part of data in the current node is associated. Let relevant data be represented by D and suppose in D there are I categories of X and J categories of Y (if Y is categorical). The p-value computation using data in D is as follows [11].

Let us consider a predictor variable with I categories initially and be reduced to r categories after merging. The Bonferroni multiplier B gives the possible number of ways in which I categories be combined into r categories for B = 1, r = I. For 2 r < I, the below formula is used (5)

$$B = \begin{cases} \binom{I-1}{r-1} & \text{Ordinal predictor} \\ \sum_{v=0}^{r-1} (-1)^v \frac{(r-v)^I}{v!(r-v)!} & \text{Nominal predictor} \\ \binom{I-2}{r-2} + r\binom{I-2}{r-2} & \text{Ordinal with a missing g category} \end{cases} . \quad (5)$$

In the process of analysis, a missing dependant variable is not used. If all the predictor variables of a case are missing then the case is ignored. Similarly if the case weight or frequency weight is missing, zero, or negative then the case is ignored. If not, the missing values are considered as a predictor category. The algorithm can create suitable set of categories for original predictors if it uses all the existing information from the data. Later the algorithm identifies the most alike category to the missing category. Finally, the algorithm takes a decision on combing the missing category with the most similar category or to retain the missing category as a separate category.

Splitting: For every predictor, the best split can be identified in the combining step. The splitting step is exploited to adopt the predictor to split the node. The adapted p-value connected is compared with every predictor to perform selection. The adapted p-value is obtained in the merging step.

Adopt the predictor that has the least adjusted p-value.

Then check the adjusted p-value and the user specified alpha level α_{merge}. Split the node using the predictor, if the adjusted p-value is less than or equal to the alpha level α_{merge} or else do not split the node and the node is considered as a terminal node.

Stopping: Based on the stopping rules given below, the stopping step analyses whether the tree growing process must be terminated or not:

If the node becomes pure then the node will not be split.

The node will not be split, if all the cases in a node have same values for every predictor.

The tree growing process will be terminated; if the depth of the current tree reaches the limit value of the user specified maximum tree depth.

If the size of the node is less than the minimum node size set by the user, the node will not get split.

2.5 Random Forest (RF)

RF of trees is termed as growing a collection of arbitrary trees for classification using a probabilistic scheme. As the trees vote for the most popular class, the classification accuracy is high. Random tree is one which is drawn at random from a set of possible trees. Random tree is a decision tree in which K is an arbitrary attribute chosen at each node [12].

The class probabilities on each node depend upon back fitting without pruning.

RF is the most popular method in several classification problems. It is particularly used in domains where there are large numbers of attributes and instances. It is popular for its high speed and accuracy [13]. Interpreting Ensemble's result is difficult as extracting useful rules from forest is not possible. RF is a parametric algorithm depending on the number of trees in the forest. Consequently it is a stochastic algorithm as it has two sources of randomness. To acquire reliable estimates of mean value and variance of the evaluation measures, it is necessary to run the algorithm a number of times.

2.6 Fuzzy Classifier

With fuzzy technique, it is easy to check, modify, and add delete every variable for enhanced automated analysis. This method is more advantageous when compared to deterministic algorithms as it allows multi-conclusions, a common aspect in clinical practice. For a complicated problem with high input dimension, the rule frame has a very high number of fuzzy rules on a very high-dimensional support [14].

The suggested fuzzy Cardiac arrhythmia classifier has two important function blocks namely the ECG Parameterizer and Fuzzy classifier. The ECG Parameterizer detects the ECG features of the database using Daubechies wavelets. The nonlinear parameters of ECG signals can be calculated using these features using the methods discussed above. The derived parameters will be exported to the latter for the classification. The Mamdani fuzzy method is used.

The membership functions of a given input are subjected to fuzzy operations to form fuzzy logic if-then rules. The Gaussian membership function is employed for input parameters. The input parameters range between 0 and 1. The resultant output membership functions are summed up using desired weights, to yield a kind of probability function. The Trapezoidal membership function is employed for output of the fuzzy classifier.

3 Results and Discussion

In this section, the CHAID, RF, and fuzzy classifier are evaluated. Table 1 and Figs. 1, 2, 3 and 4 show the accuracy, sensitivity, specificity, and f-measure.

From Fig. 1, it can be observed that the fuzzy classifier has higher accuracy by 4.46% for CHAID and by 7.27% for RF classifier.

From Fig. 2, it can be observed that the fuzzy classifier has higher sensitivity by 6.26% for CHAID and by 10.63% for RF classifier.

Table 1 Summary of results

Classifiers	Accuracy	Sensitivity	Specificity	F-measure
CHAID	0.8953	0.8839	0.941033	0.872733
Random forest	0.8705	0.846033	0.9227	0.841167
Fuzzy classifier	0.9362	0.9411	0.967033	0.928333

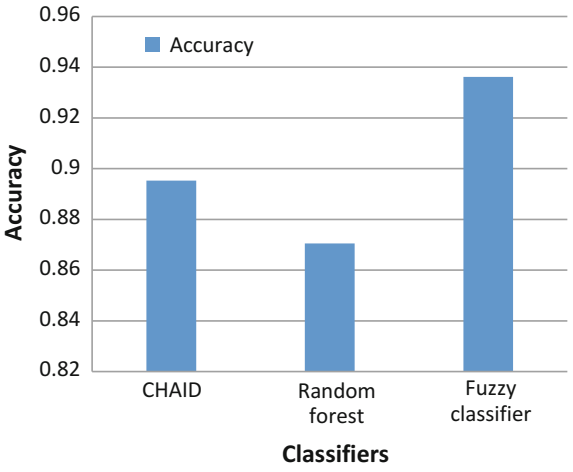


Fig. 1 Accuracy

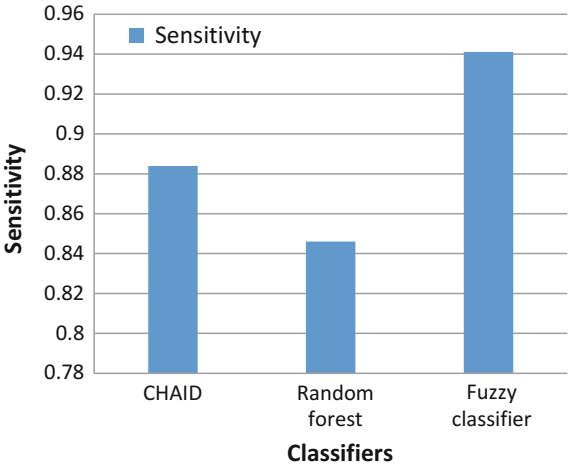


Fig. 2 Sensitivity

From Fig. 3, it can be observed that the fuzzy classifier has higher specificity by 2.72% for CHAID and by 4.69% for RF classifier.

From Fig. 4, it can be observed that the fuzzy classifier has higher f-measure by 6.17% for CHAID and by 9.85% for RF classifier.

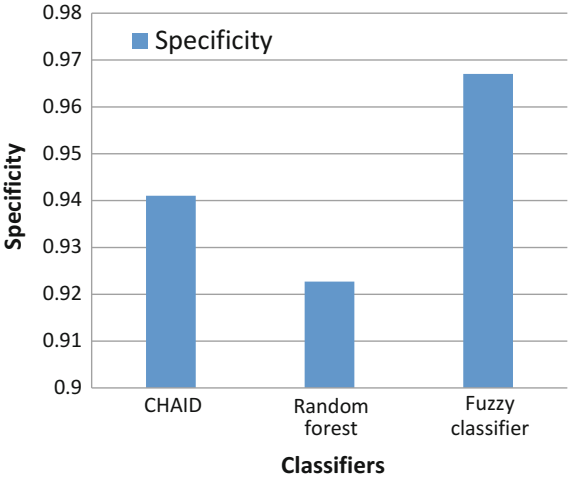


Fig. 3 Specificity

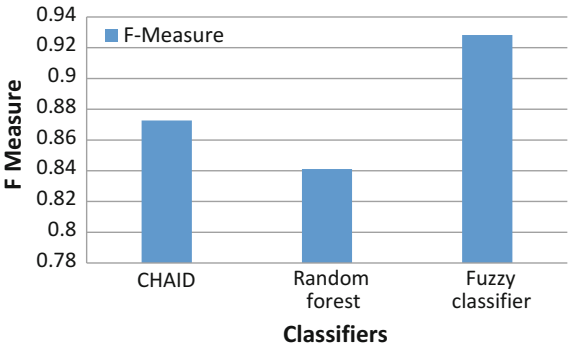


Fig. 4 F measure

4 Conclusion

Cardiac Arrhythmia is a condition where there is an irregular heartbeat caused by irregular rhythm, i.e., increase or decrease in heartbeat. Heart arrhythmia can be assessed by ECG. Several types of arrhythmia types that are related to heart disease are accurately diagnosed using ECG. Extensive research is happening for ECG's automatic arrhythmia assessment. This work proposes to classify the ECG data by retrieving energy using DCT. RR interval is extracted and used as feature. The time series data acquired from MIT-BIH is converted to frequency domain using DCT for feature extraction. Two types of arrhythmia namely LBBB and RBBB with normal beats were classified. Experimental results show that the fuzzy classifier has higher accuracy by 4.46% for CHAID and by 7.27% for RF classifier.

References

1. Sharma, P., & Kaur, L. (2012). Identification of Cardiac Arrhythmias using ECG. International Journal of Computer Technology and Applications, 3(1).
2. Gothwal, H., Kedawat, S., & Kumar, R. (2011). Cardiac arrhythmias detection in an ECG beat signal using fast fourier transform and artificial neural network. Journal of Biomedical Science and Engineering, 4(04), 289.
3. Rawther, N. N., & Cheriyan, J. (2015). Detection and Classification of Cardiac Arrhythmias based on ECG and PCG using Temporal and Wavelet features. International Journal of Advanced Research in Computer and Communication Engineering, Vol. 4, Issue 4.
4. Durham, D., & Worthley, L. I. (2002). Cardiac arrhythmias: diagnosis and management. The tachycardias. Critical Care and Resuscitation, 4(1), 35.
5. Khandait, P. D., Bawane, N. G., & Limaye, S. S. (2012). Features Extraction of ECG Signal for detection of cardiac arrhythmias. International Journal of Computer Applications, 2(1), 520–525.
6. Abhinav-Vishwa, M. K., Lal, S. D., & Vardwaj, P. (2011). Classification of arrhythmic ECG data using machine learning techniques. International Journal of Interactive Multimedia and Artificial Intelligence, 1(4).
7. M Jadhav, S., L Nalbalwar, S., & A Ghatol, A. (2012). Artificial neural network models based cardiac arrhythmia disease diagnosis from ECG signal data. International Journal of Computer Applications, 44(15), 8–13.
8. Kumar, G. R., & Kumaraswamy, Y. S. (2014). Spline activated neural network for classifying cardiac arrhythmia. Journal of Computer Science, 10(8), 1582.
9. Kumar, R. G., & Kumaraswamy, Y. S. (2012). Investigation of Support Vector Machine To Assess Cardiac Arrhythmia. In Int. Conf. on Advances in Computer and Electrical Engineering (ICACEE'2012) Nov (pp. 17–18).
10. Kadhar Nawaz, G. M. (2014). Analysis of Optimization Techniques in Chi-Squared Automatic Interaction Detection. Journal of Theoretical & Applied Information Technology, 65(3).
11. Tang, T. I., Zheng, G., Huang, Y., Shu, G., & Wang, P. (2005). A comparative study of medical data classification methods based on decision tree and system reconstruction analysis. Industrial Engineering and Management Systems, 4(1), 102–108.
12. Ganeshkumar, R., & Yskumaraswamy, D. (2012). Investigating cardiac arrhythmia in ECG using random forest classification. International Journal of Computer Applications, 37(4), 31–34.
13. Jovic, A., & Bogunovic, N. (2012). Evaluating and comparing performance of feature combinations of heart rate variability measures for cardiac rhythm classification. Biomedical Signal Processing and Control, 7(3), 245–255.
14. Anuradha, B., Reddy, V., & Veera, C. (2008). Cardiac arrhythmia classification using fuzzy classifiers. Journal of Theoretical and Applied Information Technology, 4(4), 353–359.

128-Bit Multiplier with Low-Area High-Speed Adder Based on Vedic Mathematics

K. Sunil Kumar and M. Swathi

Abstract High-speed multiplier which uses the high-speed adder is designed based on the Vedic mathematics in this paper. Vedic multiplier is designed easily by using the algorithm, Urdhva-Tiryakbhyam which is a way of multiplication described in Vedic mathematics. This algorithm is an easy way to complete the multiplication when compared to shift and add algorithm. The proposed multiplier uses an adder which has less delay and area compared with the carry select adder. Verilog HDL is used for the programming and XILINX 14.7 for the synthesis and simulation. The proposed design is compared to the Vedic multiplier which uses the carry select adder in terms of delay and area.

Keywords Vedic mathematics · Vedic multiplier · Urdhva-Tiryakbhyam · High-speed adder · Carry select adder (CSLA)

1 Introduction

Fundamental operation in digital signal processing applications is multiplication. Design of an efficient system is one of the most important steps in VLSI. Multiplication takes more time in the whole system; hence the speed of a system depends on the multiplier's speed. So, we can design a multiplier which has less delay [1]. Also, it is important to decrease the area of the multiplier and power consumed by the multiplier [2]. Hence optimization of a system can be done by these constraints. Demand for the DSP applications has increased nowadays, such that demands for

K. Sunil Kumar (✉)
Department of ECE, Raghu Institute of Technology, Visakhapatnam, AP, India
e-mail: sunilkumarkuppili@gmail.com

M. Swathi
Department of ECE, Grandhi Mallikarjuna Rao Institute of Technology, Rajam, AP, India
e-mail: swathimanthini429@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_17

the high-speed multiplier have increased. The main component in the multiplier is an adder. So, speed and area of the multiplier is reduced by decreasing the speed and area of the adder.

1.1 Vedic Mathematic Algorithms

Vedic algorithms decrease the complexity of the mathematics. Vedic algorithms require less calculation time and low area. These algorithms have sixteen sutras for all the mathematics. Urdhva-Tiryakbhyam and Nikhillam are applicable to the multiplication. In this paper, Urdhva-Tiryakbhyam is adopted to describe the multiplication. In conventional multiplication, final result is given by shift and add algorithm [3]. In Vedic mathematics, the final result is given by Urdhva-Tiryakbhyam algorithm. In the shift and add algorithm, first all the intermediate products are generated. After that, we can get the final result by adding these intermediate products as per the algorithm. Hence, it is a time-consuming procedure. Where as in the Urdhva-Tiryakbhyam algorithm, the intermediate products are generated simultaneously and added parallel. Hence, time to get the final result is low. Hence, Vedic multiplier is a high-speed multiplier.

2 Vedic Multiplier Architecture

To implement the N × N Vedic multiplier, we have to implement N\2 × N/2 Vedic multiplier architecture and N-bit adder architectures. N × N multiplier needs four N/2 × N/2 multipliers and three N-bit adders. At first 2 × 2 multiplier is designed. By using this block, 4 × 4 Vedic multiplier is designed. By using 4 × 4, 8 × 8 Vedic multiplier is designed. In this way, 16 × 16, 32 × 32…N × N multipliers are designed. 32 × 32 Vedic multiplier is designed in this paper.

2.1 2 × 2 Vedic Multiplier

Take two binary numbers $P = P_1P_0$ and $Q = Q_0Q_1$. The multiplication of these two numbers can be explained by using the Vedic algorithm called Urdhva-Tiryakbhyam which means vertical and crosswise. According to this algorithm, first, least significant bits P_0 and Q_0 are multiplied that show vertical direction. This result is taken as the least significant bit of the final result. Next, multiplication of P_0 and Q_1; P_1 and Q_0 shows crosswise direction. Hence, it is called as vertical and crosswise algorithm. Adding these two results by an adder gives the sum and one carry bit. This sum is taken as the second bit of the final result and the carry bit is sent to the next stage addition. Finally, multiply most significant bits P_1 and Q_1 and the result is added

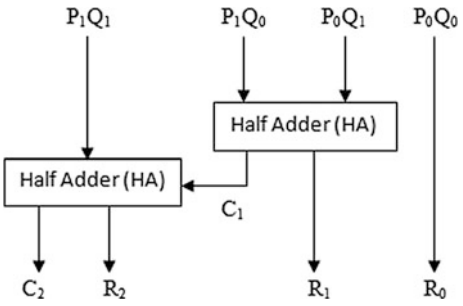


Fig. 1 2 × 2 Vedic multiplier

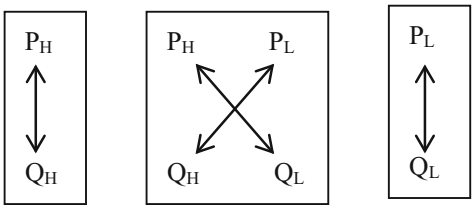
with the carry bit of the previous addition are added through an adder gives the remaining bits of the final result. Architecture of 2 × 2 multiplier is shown in Fig. 1.

2.2 *Procedure for Multiplication by Urdhva-Tiryakbhyam Algorithm*

Step1: Divide the numbers P and Q into two parts of equal bit width.
Step2: Represent the complete number as P_HP_L and Q_HQ_L.

$$P = P_HP_L \quad Q = Q_HQ_L$$

Step3: Now apply Urdhva-Tiryakbhyam sutra to get the result which is shown below.



2.3 *4 × 4 Vedic Multiplier*

4 × 4 Vedic multiplier can be intended by four 2 × 2 Vedic multipliers and three 4-bit adders. Consider two 4 bit numbers P which is written as $P_3P_2P_1P_0$ and Q which is written as $Q_3Q_2Q_1Q_0$. Now apply Urdhva-Tiryakbhyam formula to get the final result. The multiplication can be done by divide them into two groups P_3P_2 and P_1P_0 and Q_3Q_2 and Q_1Q_0. Now by using the fundamental Vedic multipliers i.e., 2 × 2 multipliers, we can plan the 4 × 4 Vedic multiplier which is shown below Fig. 2. Result is of 8 bits wide.

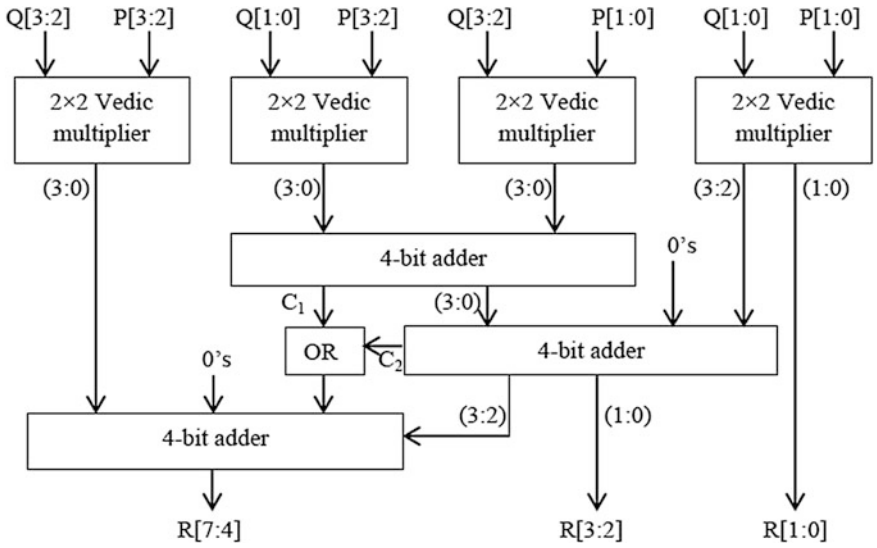


Fig. 2 4 × 4 Vedic multiplier

3 Adder Architectures

Generally there are so many adders like half adder (HA) for two bit addition, full adder (FA) for three bit addition and for more than three bit addition application, ripple carry adder (RCA), carry look ahead adder (CLA), carry save adder (CSA), carry skip adder (CKA) and carry select adder (CSLA) are used [4, 5]. Ripple carry adder is a simple adder but delay is high. Carry look ahead adder has less delay but complexity of the circuit is high than the RCA. Carry skip adder has less delay but area is high. Carry save adder has an extra circuitry to save the carry hence needs high space [6]. Among these adders, carry select adder is a fast adder having simple circuitry to implement [7]. Carry select adder possess two carry select adders (RCAs) along with a multiplexer as shown in Fig. 3.

First RCA does the addition of two numbers along with a carry as 0 and second RCA does the addition of two numbers along with a carry of 1. Final sum is decided by the multiplexer by taking the previous carry as select line. Since the two adders do the addition at the same time, delay of this adder is low. But the space required for this adder is high because of two ripple carry adders. Hence, an adder is proposed in this paper which requires less space and less delay than the ripple carry adder.

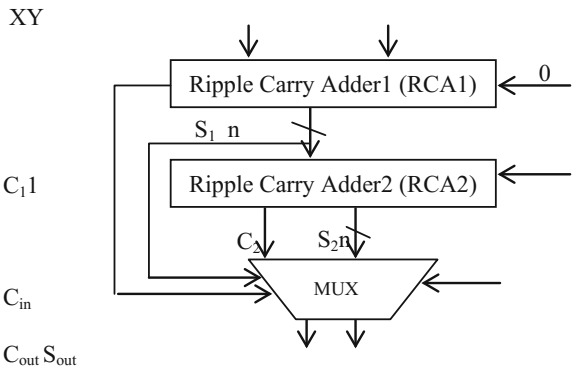


Fig. 3 Carry select adder

4 Proposed Architecture

In the proposed design, 128-bit Vedic multiplier with a high-speed and low-area adder is described. The multiplier architecture requires four 64 × 64 Vedic multipliers and three adders. Vedic multiplier has less delay than the conventional multiplier. Proposed adder is also has less delay and occupies low space. Hence, the proposed design achieves better speed and low area. Proposed adder is shown in Fig. 5. The proposed adder is nothing but the carry select adder in which RCA2 is replaced with the Binary to Excess-1 circuit. In carry select adder, RCA2 does the addition of given two numbers by taking the carry bit as 1 which is nothing but add 1 to the sum generated by RCA1. Binary to Excess-1 circuit that is shown in Fig. 4 does the same operation and requires less number of gate counts. Hence, the adder occupies less area. As the number of gate counts decreased then the path required to

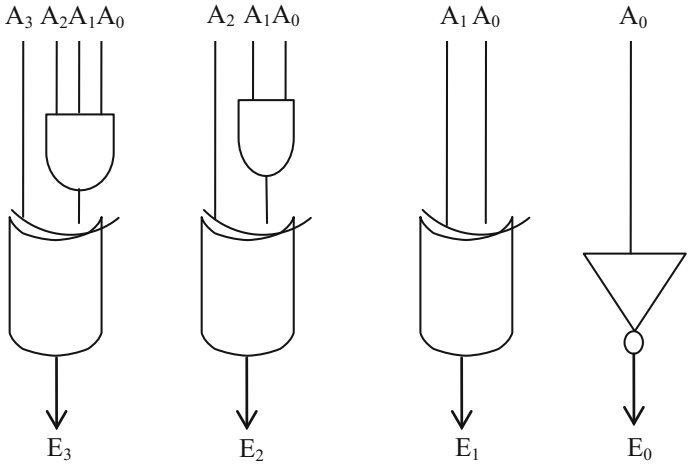


Fig. 4 4-bit binary to excess-1 circuit

the input to give output is reduced. Hence, the delay is also reduced. So, the proposed adder is low-area high-speed adder. Gate comparison of 4-bit ripple carry adder and Binary to Excess-1 circuit is given below Table 1.

Proposed adder is given below in the Fig. 5.

Table 1 Gate comparison of 4-bit RCA and BEC-1 circuit

Module	XOR	AND	OR	NOT
RCA (ripple carry adder)	8	12	4	0
BEC-1 (binary to excess-1)	3	2	0	1

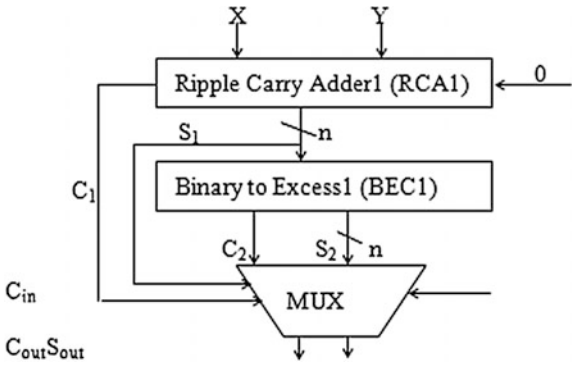


Fig. 5 Low-area high-speed adder

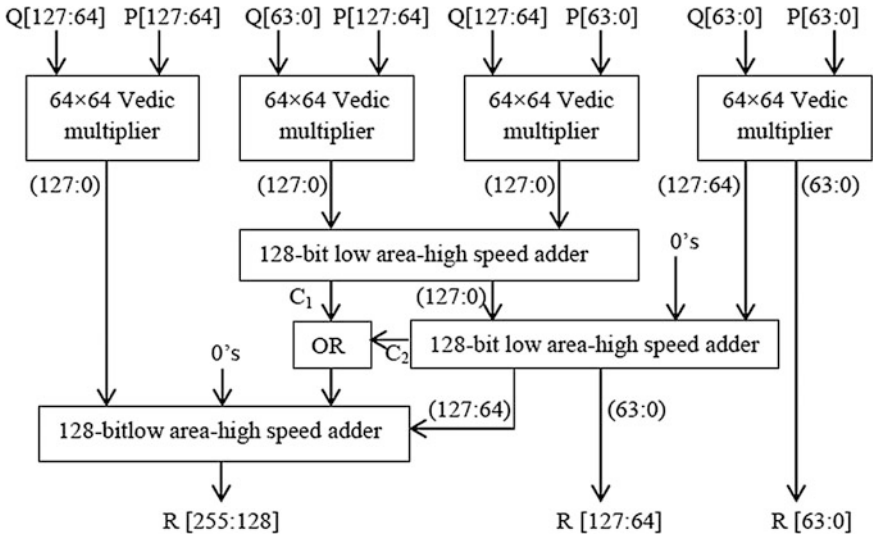


Fig. 6 128-bit Vedic multiplier with 128-bit low-area high-speed adder

The architecture of the proposed multiplier is given in Fig. 6 which uses the low-area high-speed adder. It can be implemented by using the four 64 × 64 Vedic multipliers and three 128-bit low-area high-speed adders. Result of this multiplier is of 256-bit wide. With respect to speed and area occupancy, this multiplier is good. It reduces the delay which in turn gives high speed and requires less number of gates that shows the low area by using the low-area high-speed adder.

5 Results and Comparisons

128-bit multiplier is described in this paper along with the high-speed and low-area adder. The coding part is done by using the Verilog HDL. By using the software XILIN14.7, synthesis and simulation parts are completed. Results are given below and these results are compared with the Vedic multiplier that uses regular carry select adder. In this part, speed and areas are compared by taking delay and number of LUTs required by the both multipliers and the adders. Also, the results of the

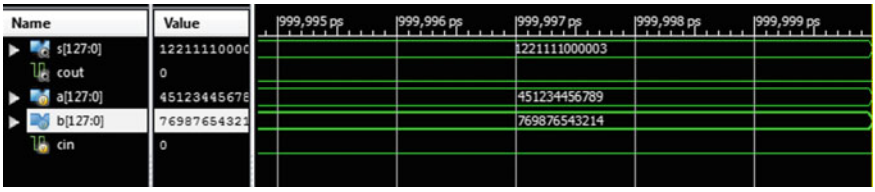


Fig. 7 Simulation result of 128-bit low-area high-speed adder

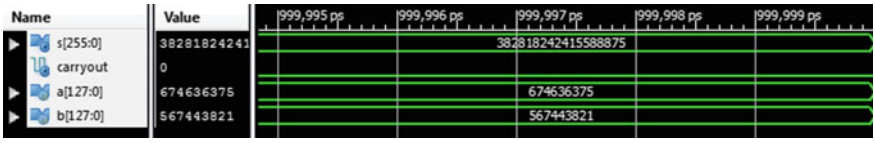
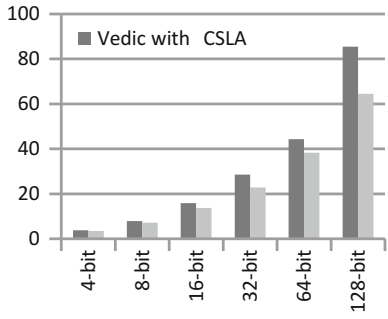


Fig. 8 Simulation result of 128-bit Vedic multiplier

Fig. 9 Delay comparison of multipliers



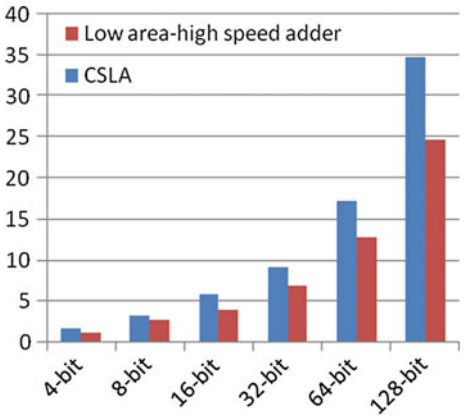


Fig. 10 Delay comparison of adders

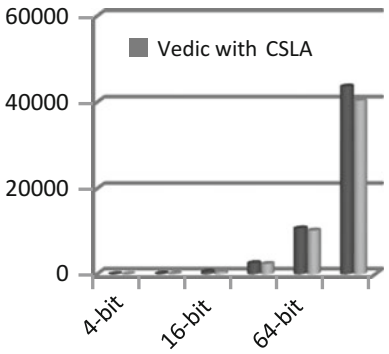


Fig. 11 Area comparison of multipliers

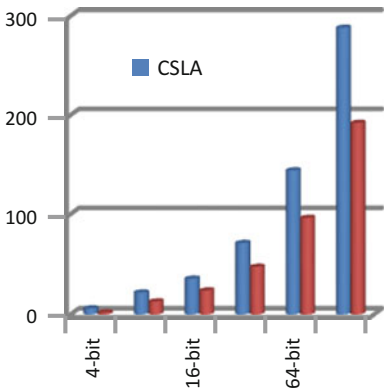


Fig. 12 Area comparison of multipliers

Table 2 Comparison of adders

Bit size	Carry select adder		Low-area high-speed adder	
	Delay (ns)	No. of LUTs	Delay (ns)	No. of LUTs
4-bit	1.604	6	0.972	2
8-bit	3.088	22	2.618	13
16-bit	5.754	36	3.829	24
32-bit	9.107	72	6.777	48
64-bit	17.608	144	12.674	96
128-bit	34.610	288	24.468	192

Table 3 Comparison of multipliers

Bit size	Vedic with carry select adder		Vedic with low-area high-speed adder	
	Delay (ns)	No. of LUTs	Delay (ns)	No. of LUTs
4-bit	3.780	25	3.460	23
8-bit	7.893	132	7.163	128
16-bit	15.877	602	13.704	580
32-bit	28.548	2590	22.862	2411
64-bit	44.369	10721	38.287	10211
128-bit	85.467	43663	64.519	40432

proposed work are compared with the conventional multiplier (Figs. 7, 8, 9, 10, 11 and 12, Tables 2 and 3).

6 Conclusion

In this paper, 128-bit Vedic multiplier is intended with a low-area high-speed adder. Low-area high-speed adder occupies less space and has less delay when compared to the regular carry select adder. Vedic multiplier has more speed than the conventional multiplier. Hence, Vedic multiplier is planned with the low-area high-speed adder to get better efficiency with respect to speed as well as area.

References

1. Jinesh, S., Ramesh, S., JosminThomas.: Implementation of 64 Bit High speed Multiplier For DSP Application-Based on Vedic Mathematics, In: TENCON 2015, IEEE region 10th conference (2015).
2. Sumit Vaidya, Deepak Dandekar.: Delay-Power Performance Comparison of Multipliers in VLSI Circuit. International Journal (IJCNC) vol 2, July 2010.

3. Arushi Somani, Dheeraj Jain, Sanjay Jaiswal, Kumkum Verma and Swati Kasht.: Compare Vedic Multipliers with Conventional Hierarchical array of array multiplier, International Journal of Computer Technology and Electronics Engineering (IJCTEE) Volume 2, Issue 6.
4. John F. Wakerly "Digital Design Principles and Practices" 4th Edition.
5. Douglas A. Pucknell and Kamran Eshraghian "Basic VLSI Design" 3rd Edition.
6. Ravikumar A Javali, Ramanath J Nayak, Ashish M Mhetar, Manjunath C Lakkannavar "Design of High Speed Carry Save Adder using Carry Look ahead Adder" Proceedings of International Conference on Circuits, Communication, Control and Computing (I4C 2014).
7. M. Chithra, G. Omkareswari "128-Bit Carry Select Adder Having less Area And Delay" International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 2, Issue 7, July 2013.

High-Throughput Low-Power Variable Rate Network Intrusion Detection System Using Unique SRAM Controller

S. Nagaraju and P. Sudhakara Reddy

Abstract Network intrusion detection system (NIDS) is a major research area for security mechanism. In recent years, the demand for digital systems in network field increase due to the development of 4G technology and high network traffic rate. In this paper, we propose a bit-based pattern matching algorithm with unique SRAM architecture for parallel processing. To reduce the bit transitions during matching process state encoded finite-state machines (FSMs) were used which the main core in the pattern is matching process, where a number of states remain constant over pattern length. To avoid synchronization problem over variable rate pattern match unique controllers are used which is driven by adaptive digital phase locked loop (ADPLL). The functionality is proved through the test bench simulation using Modelsim and power efficiency is verified using FPGA synthesis. In this work, memory size requirements are reduced by 8 times with an early detection scheme and the overall throughput rate is attained in the range of 13 Gbps. Finally, the dynamic power consumption is greatly reduced by 7% through gated logic.

Keywords Network intrusion detection system (NIDS) · Parallel processing · ADPLL · SRAM · FSM · FPGA · Low power

S. Nagaraju (✉)
Department of ECE, Jawaharlal Nehru Technological University Anantapur, Anantapur, Andhra Pradesh, India
e-mail: snagaraju02@gmail.com

P. Sudhakara Reddy
Department of ECE, Srikalahasteeswara Institute of Technology, Srikalahasti, Andhra Pradesh, India
e-mail: psr_vlsi_dsp@rediffmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*, Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_18

1 Introduction

In recent years, several string matching algorithms have been proposed for field-programmable gate array (FPGA)-based NIDS system. It is clear that only with the more efficient string matching algorithm FPGA-based NIDS system overall performance can be improved [1–3]. In many cases, static random access memory (SRAM) cells are most widely used for data storage [4]. However, there are several design issues are associated with incorporating SRAM cells in NIDS system. First, NIDS needs significant buffering and routing resources to moderate the speed control of all the cells in the system [5]. On the other hand, FPGA-based digital system always provide higher flexibility and high throughput which can exploit the fact that the NIDS rules change relatively infrequently, and use reconfiguration to reduce implementation cost. In addition, one can carry out parallelism in order to achieve satisfactory processing throughput. Additionally, matching a large number of patterns takes a large number of states in FSM-based pattern matching unit, so allocating dedicated logic cells for each character is critical. In order to reduce the number of states required to match large patterns and keep that count as constant here, we proposed bit-based pattern matching since it could save a significant amount of resources, and make designs smaller and faster.

In any cases, data fetching and pattern matching are highly complex and intensively power consuming unit in NIDS system, our proposed architectures exploit the benefits of SRAM design for an efficient bit-based pattern matching and early detection-based gated clock systems. The proposed architectures can able to the match pattern in any length and one can able to store entire NIDS patterns in a single memory device. In this work, we also find solutions for variable rate pattern matching reconfigurable clock divider with ADPLL is used since NIDS systems are used at server side where incoming payload data rate is unpredictable.

2 Pattern Matching for Next-Generation NIDS System

In recent years, the pattern length of intrusions are getting increased while existing software-based approaches can be able to compare each pattern independently against the incoming data, where parallel processing impossible leads more computation time. Another major requirement for next-generation NIDS system is speed constrain. So the need of hardware-based NIDS systems is something that is currently unavoidable [6].

2.1 Software-Based Approach

In the past, fully software-based pattern matching unit is used as open-source NIDS. In many Snort rule sets are widely used. Initially, brute-force algorithm is used [7]

for pattern matching, which was very slow, since the software-based system needs a high-performance processor. Then later Boyer–Moore algorithm is known as most well-known algorithms [8], where numbers of comparisons are greatly reduced with hierarchical-based heuristic approach. In this method, incoming payloads are properly aligned and the comparison begins from the top to bottom valid payloads are shifted out; in the case of mismatch unique signals are asserted.

2.2 Digital System for Pattern Matching

Through processor independent hardware model for pattern matching system, we can support modest throughput. The basic NIDS of systems can be fulfilled, with digital-centric hardware system. Many hardware NIDS systems usually store their patterns using large memory blocks [9, 10], and carry out matching process as a fully integrated processing element in a synchronized manner. Generally, FSMs are used for pattern match where rules are stored as states and American Standard Code for Information Interchange (ASCII)-based matching process is carried out which cannot achieve impressive performance for following reasons.

- The patterns are stored in memory blocks as an ASCII character.
- With any NIDS rules, the mismatch will be triggered only at the end of matching process.

The most common SRAM cells have row and column selection for data storage. For an efficient bit-based pattern matching here, we proposed irregular expressions of SRAM cell with synchronized controller. On the other hand, FPGAs are more suitable because they are reconfigurable they provide hardware speed [11], and exploit parallelism. The main bottlenecks in any FPGA-based NIDS implementations are to balance traffic rate over multiple parallel incoming patterns and to assert functionally equivalent hardware blocks concurrently for each rule set (several hundred rules), the obvious disadvantage is the linear increase in the memory usages. In this work, we propose a different, traffic-aware approach in the design of FPGA-based NIDS. Instead of purely carry out concurrent matching across equivalent modules, we divided into a group of differently capable digitalized blocks, each supporting a different rule set matched with the specific traffic category.

In any case clock signal will be used as a driving forces and time reference for both data propagation and computation in digital. Due to application specific nature of NIDS system, each functional module should synchronize one to another one. This will lead clock mismatch problem. Sometimes it will lead metastability problem. In our proposed FPGA-based NIDS system, this problem can be solved with input data-driven SRAM controller and reconfigurable clock divider and clock skew problem is solved with ADPLL.

3 NIDS System Architecture

Here for digitalized pattern matching SRAM-based controllers are used to drive the intrusion which will be grouped and generated parallel bit stream as per the length of the pattern to enable bit-based matching process. Bit-based pattern search algorithm is a good choice for a string matching engine as the overall computation latency does not depend on the length of the pattern since only eight FSM machines are required each with only three logical states.

In the case of the bit grouping method, the probability of early detection is proportional to a ratio between payload traffic rates over a number of patterns in NIDS SRAM database as shown in Fig. 1. However, parallel-pushing can be used to eliminate significant latency and to increase the throughput rate.

The incoming payloads are divided into subgroups and each value in the subgroup is considered as a unique ASCII values as shown in Fig. 2. To improve the dynamic reconfigurability and user-friendly design nature page enabled intrusion schemes were proposed, where the matching process can be done in the parallel process as shown in Fig. 3. Finally, bitwise FSM-based state transitions are carried out between input bit stream and subpattern from each page and a global match will be done based on the partial matching vector (PMV) scheme.

3.1 Gated Clock Design

Here through data transition reduction controller as a dynamic power management (DPM), one can reduce power consumption in FPGA-based NIDS system. The DPMs strategy consists in disabling some of the FSM circuits by performing early detection operations as shown in Fig. 4, during bitwise matching from least significant bit (LSB) to most significant bit (MSB), thus reducing power consumption.

3.2 All Digital Reconfigurable Multi-rate System

In all other existing system analog circuitry-based voltage controlled oscillators (VCOs) are widely used as a frequency divider. The dynamic range required for

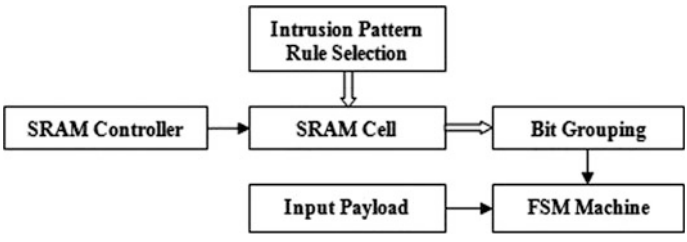


Fig. 1 Bit grouping NIDS system architecture

```
Bytestream generation from input serial digital bits
To detect the length of the pattern L & incoming payload data rate DATA_clk.
Assert ADPLL_enable signal
     Partitioning into L1-L2-L3
While (FSM_clock == DATA_clk)
   Continue delay buffer insertion
End
Enable FSM state machine
Match FSM_clk with SRAM read clock signal
For (i = 1; i < 8; i =++)// from LSB to MSB
If (L1 [i] == PAGE_1_FSM1 [i] && L2 [i] == PAGE_1_FSM2 [i]
&&L3 [i] ==PAGE_1_FSM3 [i])
   Assert PMV1 [i] = 1          // FSM holds database
     Else
   Skip to decision making process
      End
   Assert PMV1 [i] = 0        // partial matching vector
End
If (& (PMV1) = 1)
  MV = 1                              // matching vector
Else
  MV = 0
End
Repeat the same process concurrently overmultiple PAGEs
                                      // each PAGE carries different signatures
Generate score value for each matching foreach MV vector
                                      // ID will be given to each signature
```

Fig. 2 Bit-based pattern matching algorithm

NIDS system and for speed constrain here we proposed adoptive line selection-based fully reconfigurable all digital frequency divider. The input payload droverate-controller as shown in Fig. 5 will assert delay line consists of a combination of inverters and gate chain. Based on the unit delay for each logic cell chains are interconnected in order to meet the clock skew design specification. Therefore, a fine delay control scheme is employed. The variable delay line consists of both coarse and fine delay lines.

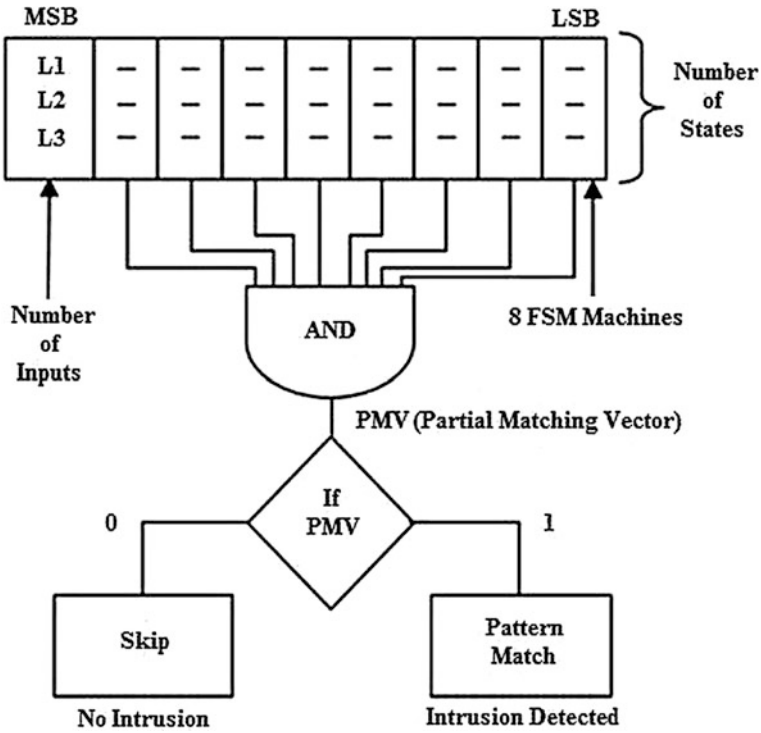


Fig. 3 Bit-based parallel matching process

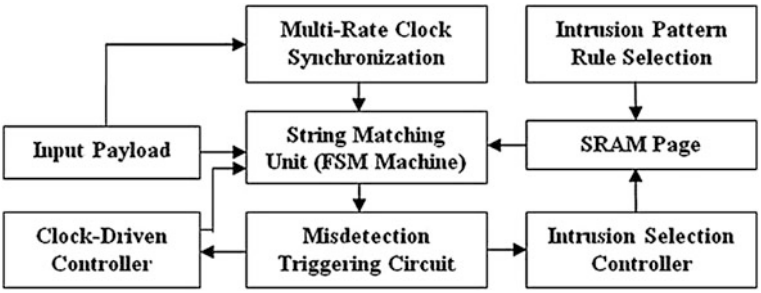


Fig. 4 Low-power NIDS architecture

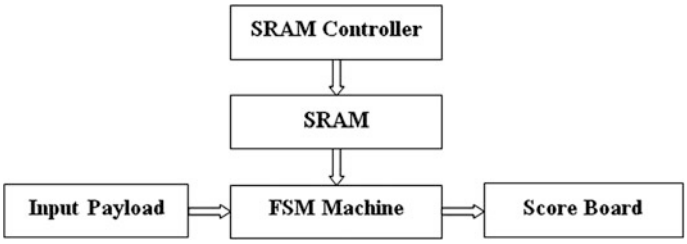


Fig. 5 NIDS intrusion classification module

4 Results

The SRAM controller-based synchronous FPGA-based NIDS system is designed with fully digitalized reconfigurable frequency divider and bit grouping-based pattern matching is carried out for better optimization, over all other digital NIDS system. The unique controller-driven variable rate system is highly suitable for all pattern matching process and its efficiency over parallel process is proved through functional simulation with exhaustive test vectors.

4.1 Simulation Results Using Modelsim

In order to verify the functionality pattern matching process described in the previous section, a variable rate pattern matching is simulated as shown in Fig. 6. Here first, clock division is performed using ADPLL based on the input payload which is matched with intrusion hold in FSM states. Both clock division for all five incoming payloads and pattern matching are simulated. As seen from Fig. 6, the ADPLL clock is disabled if any misdetection will accumulate as the FSM-based matching progress in a bitwise manner. Based on the observation of Fig. 7, the gated clock logic proved the general rules described in the previous section.

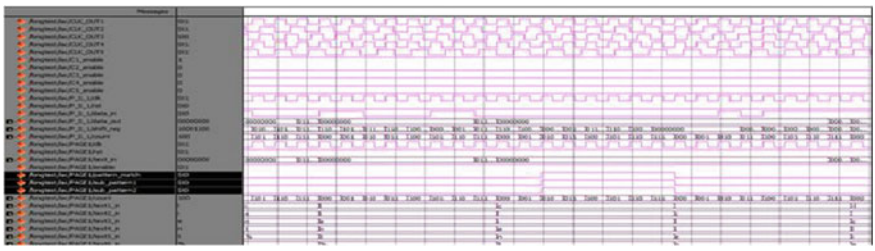


Fig. 6 Intrusion detection system with multi-rate clock

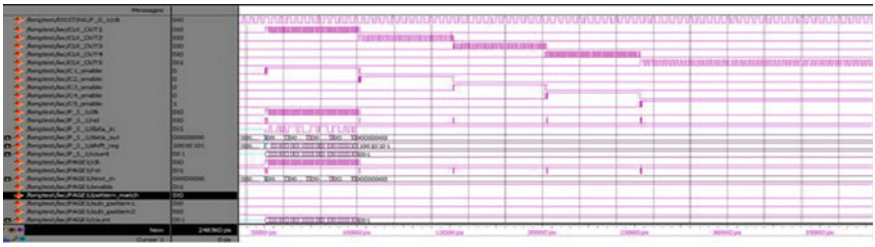
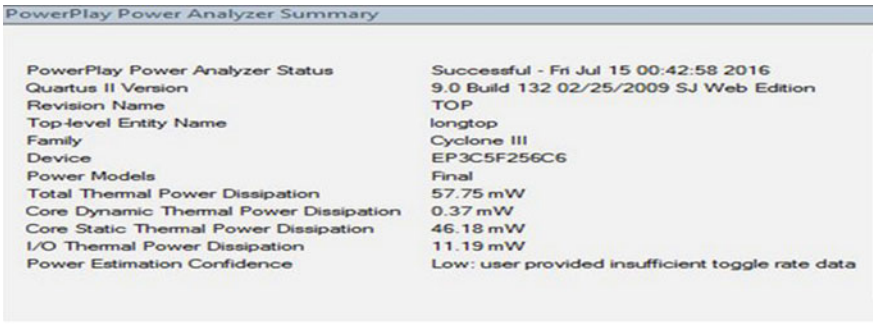


Fig. 7 Intrusion detection system with gated clock

4.2 *Synthesis Results Using QUARTUS II EDA Tool in CYCLONE III Family 65 nm FPGA Device*

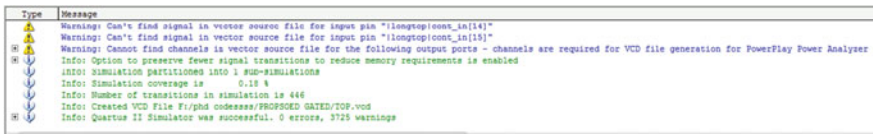
Here, we were used Verilog HDL to describe the NIDS system and synthesized using ALTERA Cyclone III device. First, the power efficiency of proposed gated logic over multi-rate pattern matching and its transition reduction is proved as shown in Figs. 8 and 9. In addition, tradeoff between power efficiency over area, overhead is also analyzed and proved to be negligible one as shown in Fig. 10. However, the computational accuracy and overall power reduction largely depend on a number of patterns used and user rate. And finally, Payload drove digital frequency synthesizer is also verified and its dynamic range is proved to be in



PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Fri Jul 15 00:42:58 2016
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	TOP
Top-level Entity Name	longtop
Family	Cyclone III
Device	EP3C5F256C6
Power Models	Final
Total Thermal Power Dissipation	57.75 mW
Core Dynamic Thermal Power Dissipation	0.37 mW
Core Static Thermal Power Dissipation	46.18 mW
I/O Thermal Power Dissipation	11.19 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig. 8 Power dissipation report with gated clock



Type | Message

Warning: Can't find signal in vector source file for input pin "|longtop|cont_in[14]"
Warning: Can't find signal in vector source file for input pin "|longtop|cont_in[15]"
Warning: Cannot find channels in vector source file for the following output ports - channels are required for VCD file generation for PowerPlay Power Analyzer
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 0.18 %
Info: Number of transitions in simulation is 446
Info: Created VCD File F:/phd codesss/PROPSOED GATED/TOP.vcd
Info: Quartus II Simulator was successful. 0 errors, 3725 warnings

Fig. 9 Number of transitions with gated clock

Flow Status	Successful - Wed Jul 13 05:20:36 2016
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	TOP
Top-level Entity Name	longtop
Family	Cyclone III
Met timing requirements	N/A
Total logic elements	983 / 5,136 (19 %)
Total combinational functions	958 / 5,136 (19 %)
Dedicated logic registers	536 / 5,136 (10 %)
Total registers	536
Total pins	14 / 183 (8 %)
Total virtual pins	0
Total memory bits	0 / 423,936 (0 %)
Embedded Multiplier 9-bit elements	0 / 46 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP3C5F256C6
Timing Models	Final

Fig. 10 Area utilization report with gated clock

1689.19 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)
593.47 MHz	250.0 MHz	p1_enable	limit due to minimum period restriction (max I/O toggle rate)
731.53 MHz	250.0 MHz	p4_enable	limit due to minimum period restriction (max I/O toggle rate)
739.1 MHz	250.0 MHz	p2_enable	limit due to minimum period restriction (max I/O toggle rate)
766.28 MHz	250.0 MHz	p3_enable	limit due to minimum period restriction (max I/O toggle rate)
783.09 MHz	250.0 MHz	p5_enable	limit due to minimum period restriction (max I/O toggle rate)

Fig. 11 Operating frequency report

Table 1 Transition control and power reduction comparison table through FPGA QUARTUS II EDA tool synthesis using CYCLONE III family 65 nm device

Type used	Area used (logic elements)	Number of transitions	Total power consumption (mW)
With multi-rate clock logic	960	4262	62.00
With gated logic	983	446	57.75

several GHz since payload incoming speed can be started from Kbps to Gbps as shown Fig. 11. Detailed results are shown in Table 1.

$$\begin{aligned}\text{Throughput} &= \text{Number of bits processed per clock cycle} \times \text{Maximum frequency} \\ &= 8 \times 1689.19\,\text{MHz} \\ &= 13.513\,\text{Gbps}.\end{aligned}$$

5 Conclusions

In this paper, we proved the merits of input payload driven multi-rate parallel matching in NIDS system in terms of high throughput and power efficiency. The problem over multi-rate is also being mitigated through reconfigurable clock divider

with fully digitalized PLL whose dynamic range can be changed dynamically. To extend the merits of early detection during bitwise pattern matching clock gated controller is used for controlling both FSM and rule selection. The power efficiency is proved to be tolerable one over area overhead.

References

1. Baker, Z. K. and Prasanna, V.K. 2005. A computationally efficient engine for flexible intrusion detection. IEEE Trans. VLSI Syst. 13, 10, 1179–1189.
2. Dharmapurikar, S, and Lockwood, J. 2006. Fast and scalable pattern matching for network intrusion detection systems. IEEE J. Sel. Areas Comm. 24, 10, 1781–1792.
3. A. V. Aho, M. J. Corasick, Efficient string matching: an aid to bibliographic search, Comm. of the ACM, Vol. 18, No. 6, pp. 333–340, (1975).
4. Tuck, N., Sherwood, T., Calder, B., and Varghese, G. 2004. Deterministic memory-efficient string matching algorithms for intrusion detection. In the 23rd Conference of the IEEE Communications Society (Infocomm).
5. Xu, J., Kalbarczyk, Z., Patel, S., and Iyer, R. K. 2002. Architecture support for defending against buffer overflow attacks. In Workshop on Evaluating and Architecting Systems for Dependability.
6. I. Sourdis and D. Pnevmatikatos. Fast, large-scale string match for a 10gbps FPGA-based network intrusion. FPL, 2003:880–889, (2003).
7. http://www.stoimen.com/blog/2012/03/27/computer-algorithms-brute-force-stringmatching.
8. Boyer, R. S. And Moore, J. S. 1977. A fast string searching algorithm. Communications of the ACM 20, 10, 761–772.
9. Vasiliadis, G., Polychronakis, M., Antonatos, S., Markatos, E.P. and Ioannidis, S. (2009) Regular expression matching on graphics hardware for intrusion detection. In Kirda, E., Jha, S. and Balzarotti, D. (eds.), RAID 2009, Lecture Notes in Computer Science (vol. 5785), pp. 265–283. Springer, Berlin, Heidelberg.
10. Ho., J.T.L, and Lemieux, G.G.F. (2008) PERG: a scalable FPGA-based pattern-matching engine with consolidated Bloomier filters. Int. Conf. Field-Programmable Technology, Taipei, Taiwan, December 7–11, pp. 73–80.
11. L. Tan and T. Sherwood. A high throughput string matching architecture for intrusion detection and prevention. In ISCA '05: Proceedings of the 32nd annual international symposium on Computer Architecture, pages 112–122, Washington, DC, USA, 2005. IEEE Computer Society.

Design and Implementation of Low-Power MIL-STD-1553B Bus Controller

C.D. Naidu, P. Kishore, Y. Padma Sai and A. Ashok Kumar Reddy

Abstract The demand in avionics field is increasing day to day and looking for high reliability and efficiency. To accomplish this MIL-STD-1553 has evolved. It has accepted as an international standard for military applications. Due its high reliability and flexibility, it can be widely used in military and space applications. In order to meet the real-world specifications, it is required to optimize the area, power, and to improve the performance of the data bus. This paper aims at designing low-power MIL-STD-1553B BC compatible to Data Device Corporation (DDC). The design has been done using Verilog HDL and simulated using Mentor Graphics tools. The power calculations have done in Design Compiler tool. The functionality of the proposed design is verified in Xilinx ISE 13.4 and the target device used is Spartan 3E FPGA.

Keywords Bus controller (BC) · Command word (CW) · Remote terminal (RT) · Data word (DW) · Status word (SW) · FPGA

1 Introduction

In the present scenario, MIL-STD-1553B bus protocol finds its use in information sharing between devices. It is a serial bus developed by U.S. Air force [1]. Modern military avionics systems consists of various number of devices that needs to

C.D. Naidu (✉) · P. Kishore · Y. Padma Sai · A. Ashok Kumar Reddy
Department of ECE, VNR VJIET, Hyderabad, India
e-mail: cdnaidu@gmail.com

P. Kishore
e-mail: kishore_p@gmail.com

Y. Padma Sai
e-mail: pasmasai_y@vnrvjiet.in

A. Ashok Kumar Reddy
e-mail: aakumar12@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_19

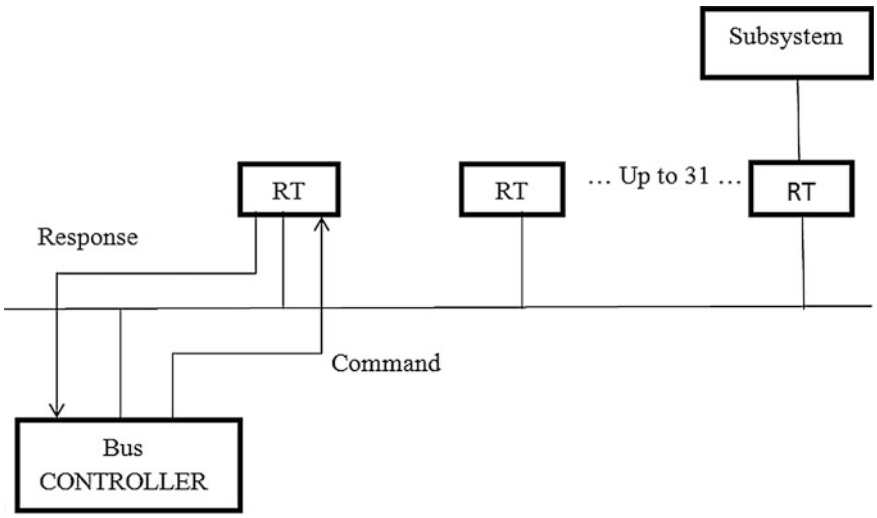


Fig. 1 MIL-STD-1553B data bus structure

communicate with each other for meeting their requirement for a particular application. In the earlier days, point-to-point wiring systems were used but it became very complex, time consuming, bulky, power consuming and hence it affected the performance of the system. So data bus architecture scheme came into existence and is used for communicating between the devices in the avionics systems. To eliminate point-to-point wiring, the bus is dual redundant, bidirectional bus [2]. The bidirectional MIL-STD-1553B bus which connects the devices through a twisted shielded pair cable. It can connect a maximum of 32 devices. Among these 32 devices, one should work as BC and remaining should act as remote terminal(RT) devices. BC is the only one device which can initiate all the communication through the 1553 bus system. This paper aims to design low-power bus protocol controller for MIL-STD-1553B data bus. The 1553B BC is known as the 'heart of the system' since it controls all the activities in the bus. The structure of the 1553B data bus is presented in Fig. 1.

2 System Overview

MIL-STD-1553B system has three main blocks—bus controller, remote terminal, and monitor terminal. This paper focuses on designing of low-power BC for MIL-STD-1553B protocol.

2.1 Bus Controller

The sole responsibility of BC is to control flow of data for all transmission on the bus. All message transfer takes place after the command word sent by BC. Apart from initiating the data transfers, BC must also transmit the data, receive the data and coordinate information transfer on the bus. The message is communicated in command/response mode, i.e., commands are sent to RTs by BC and after receiving the command, RT sends the acknowledgment. The command word (CW) send by BC may instruct RT to send data or requests for data (along with status) from remote terminals.

2.2 Message Format

The data gets transferred in the form of message. The 1553B protocol has different ways on which information transmission takes place. In this paper we focus on BC to remote terminal (BC–RT) and remote terminal to bus controller (RT–BC) message transfers.

The BC–RT message transfer command is also called as receive command. As mentioned earlier all the transfer takes place after BC sends a CW to all the remote terminal. This CW includes the address of a particular RT and @@@contains the information about the number of data words it is sending. After validating the command and all data words, RT sends acknowledgment in the form of status word to the controller. Figure 2 shows the format for BC–RT transfer.

In RT–BC message transfer, as the remote terminals send the data to bus, this mode is also known as transmitting command. As data transmission begins with the command send by BC to all remote terminals. After receiving the command word, the targeted remote terminal, acknowledges to bus by sending status word and then sends the data words as per the requested command word. Figure 3 shows the format for RT–BC transfer.

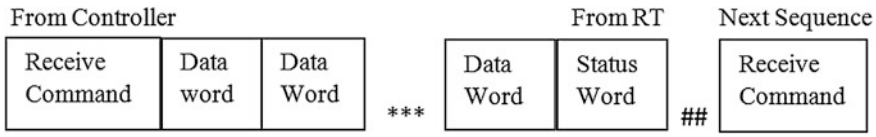


Fig. 2 Controller to RT transfer

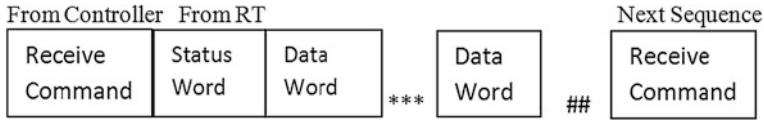


Fig. 3 RT to controller transfer

2.3 Word Format

Three different words that form the messages transmitted on the bus are command word, data word and status word [3–9]. The command contains the information for the remote terminals to perform various operations. Each word of the message consists of three-bit time sync, 16 bits for the information field, and a parity bit at the end, which makes a total of twenty bits. The actual information that needs to be transferred through 1553B bus is contained by data word (DW). The status of the remote terminal is indicated by the status word. RTs must send an acknowledgment in the form of status word as the first word after receiving valid message from BC.

3 Design and Implementation

MIL-STD-1553B BC block diagram is presented in Fig. 4. First, the BC will send a command word which specifies particular RT address to which the data has to be sent/received. The CW contains the information about the transmission/reception, sub-address/modes, the number of data words/mode codes and a parity bit. Flow chart for BC for MIL-STD-1553B is given in Fig. 5.

In BC to RT transfer, the BC will send a command indicating with which RT it wants to communicate. The RT in this mode is receiving the data, which can be identified by looking at the ninth bit of command word, for the receiving mode it

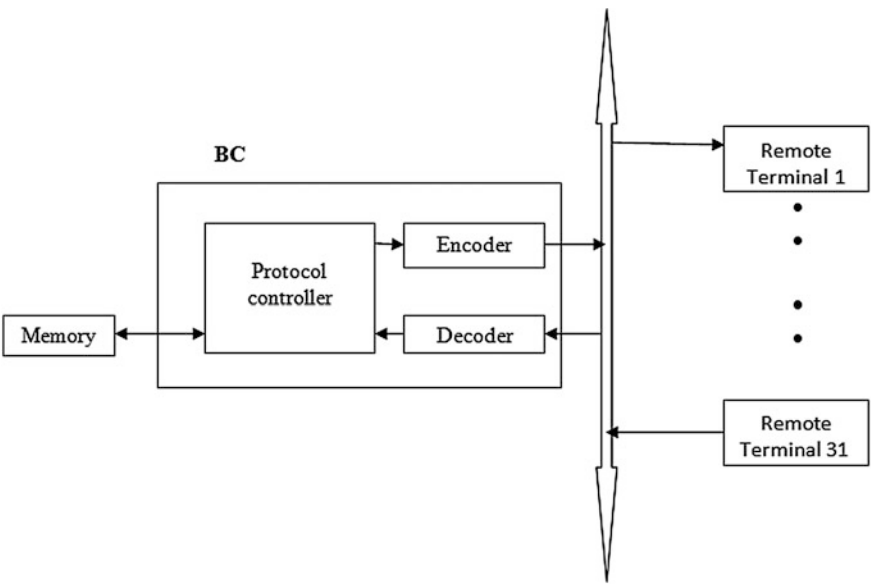


Fig. 4 1553B bus controller's block diagram

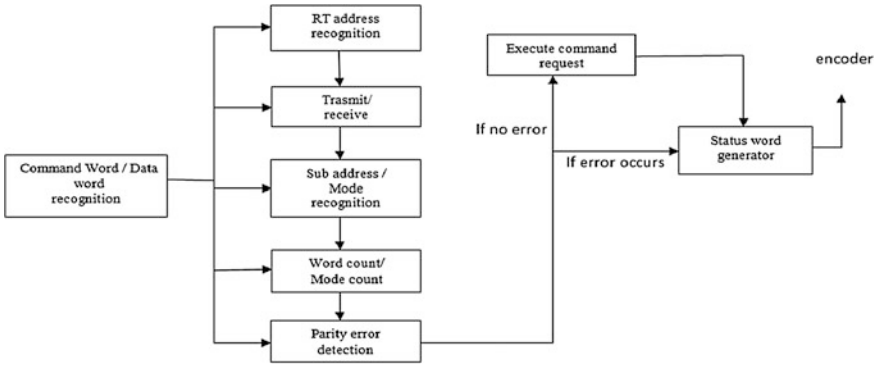


Fig. 5 Flow chart for bus controller for MIL-STD-1553B

should be '0' and for transmission it should be '1.' As it is receive command, it asks the RT to receive the number of data words specified by command. After decoding the RT address, it will generate a status word which is an acknowledgement that the RT has received the data words properly.

In RT to BC transfer, BC will send a transmit CW through bus_out signal. This transmit command specifies the number of data words to be sent by RT. After validating the RT address, that particular RT will send an acknowledgement in the form of status word. If the received RT address is wrong it will generate an error in status word through bus_in signal.

4 Results

The program for the design is written by making use of Verilog language and the same has been simulated using the ModelSim tool. The message transfers between BC to RT are shown in Figs. 6 and 7 and the RT to BC transfers shown in Figs. 8 and 9. The total dynamic power obtained in Design Compiler is 63.2670 μW. The synthesis is being done in Xilinx ISE 13.4 and the selected target device is Spartan 3E FPGA. The result obtained using Xilinx ISE suite is stated below and the device utilization of the designed system.

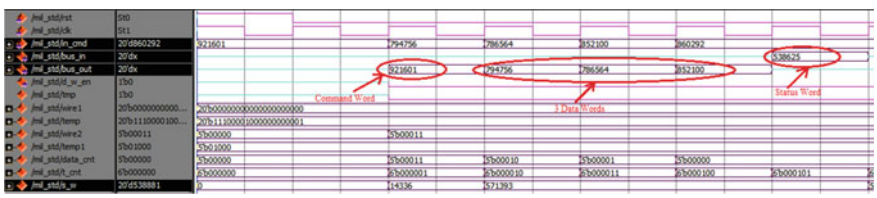


Fig. 6 BC-RT transfer with three data word transfer

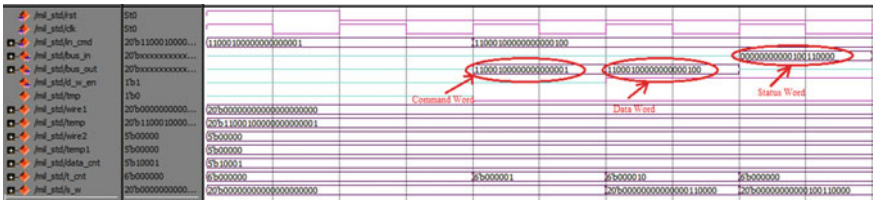


Fig. 7 BC-RT transfer with 1 data word being transferred

Fig. 8 RT-BC mode with 1 data word being transferred

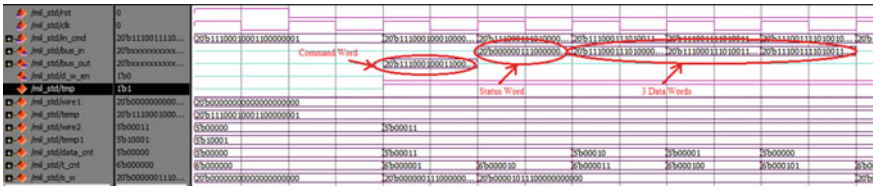


Fig. 9 RT-BC mode with three data word being transferred

Table 1 Device utilization of designed system

Device utilization summary			
Logic utilization	Used	Available	Utilization (%)
Flip flop	84	9,312	1
LUTs	351	9,312	3
Occupied slices	196	4,656	4
IOBs	63	232	27
BUFGMUXs	1	24	4
Average fanout of non-clock nets	3.81	–	–

- Minimum period for the design presented is 10.599 ns.
- Maximum operating frequency is 94.350 MHz.
- Minimum input arrival time before clock is 12.484 ns.
- Maximum output required time after clock is 4.394 ns (Table 1).

5 Conclusion and Future Scope

In this paper, MIL-STD-1553B BC has been designed and implemented successfully on Spartan 3E FPGA using Xilinx 13.4. The two modes of message transfer, i.e., BC to RT and RT to BC have observed and the results are presented. The utilization of the device for the design, which is generated using Xilinx 13.4 shows that only 1% of flip flops, 3% of the available LUTs, 4% of Occupied slices, 27% of IOBs, and 4% of BUFGMUXs are occupied. Using Design Compiler, it is observed that the total power required by the design is 63.2670 μW which is very less considering the complexity of the standard. Thus, the developed system occupies less area and requires less power dissipation. In military and space applications, accuracy and reliability are the key factors. Hence, the future work for this paper may be focusing on improving the performance of the data bus and work can be done on integrating various emerging technologies into it.

References

1. Department of Defence.: MIL-STD-1553B, Aircraft internal time-division multiplexing data bus. Washington, D.C., (1978).
2. Yunfeng Bai, Zucheng Zhou, Junbi Chen.: The implementation of MIL-STD-1553B processor. Emerging Technologies (ICET), 2012 International Conference on, pp. 1–6, Oct. (2012).
3. MIL-STD-1553 Designer's Guide, Data Device Corporation, 6th Edition.
4. Jemti Jose.: An FPGA Implementation of 1553 Protocol Controller, International Journal of Computer Information Systems and Industrial Management Applications. ISSN 2150-7988, Volume 6, pp. 66–76, (2014).
5. MIL-STD-1553 Tutorial, Condor Engineering, Bohemia, New York, (2000).
6. Enumala Srikrishna, Madan Mohan. L., Mallikarjuna Prasad. A.: Development of MIL-STD-1553B Synthesizable IP Core for Avionics Applications. International Journal of Computer Science Issues (IJCSI), Vol. 8, Issue 5, No. 3, (September 2011).
7. Siji K, Saritha N R.: FPGA Implementation of MIL-STD-1553B Bus Protocol Controller for Aircrafts. International Journal of Science and Research (IJSR), ISSN (Online): 2319-7064, (2013).
8. Amrutha V, Anu James, Sreejith S.: FPGA Implementation of MIL-STD-1553B Protocol: A Review. IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 2 Issue 4, (April 2015).
9. Sharon Theresa George, Mangaiyarkarasi. J.: Design and Implementation of Mil-Std-1553B Bus Protocol Controller with FPGA and ASIC. International Journal of Research in Engineering & Advanced Technology (IJREAT), Volume 3, Issue 3, June–July, 2015.

Modified Low-Power Hybrid 1-Bit Full Adder

Chaithanya Mannepalli and Chaitanya Kommu

Abstract The usage of digital devices is increasing rapidly and they became essential part of everyone's life. Digital devices can be designed according to their application and most of them are realized using arithmetic processor which consists of several operations like addition, subtraction, multiplication, etc., all of them can be implemented using full adder as the basic building block. As full adder plays a major role in digital devices we need to design a low-power full adder such that the devices can operate at lower power consumption and has longer battery life. In this research work, a hybrid low-power 1-bit full adder was designed using CMOS logic, pass transistor, and transmission gate logic with 14 transistor. The design was simulated using HSPICE tools in 90 nm technology with supply voltage of 1.2 V. Performance parameters, such as power, delay, and power delay product were compared with the existing designs, such as C-CMOS Full Adder, Mirror adder, hybrid pass-logic with static CMOS output drive full adder and found that the proposed adder has the low-power consumption and power delay product than the aforementioned adders.

Keywords Adder · CMOS · Pass transistor · XNOR · Low power

1 Introduction

Full adder is the fundamental building block of all battery operated devices like mobile phones, personal digital assistants, laptops, and many useful electronic gadgets. This becomes a key factor for researches to propose or modify the existing

C. Mannepalli (✉) · C. Kommu
Electronics and Communication Engineering Department, GITAM University, Rushikonda, Visakhapatnam, India
e-mail: chaithanya15992@gmail.com

C. Kommu
e-mail: chaitanya.kommu@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_20

adders such that the power and delay are reduced. Several designs of full adders were proposed [1, 2] regarding to power and efficiency.

Full adder can be designed with different logic styles, each having its own advantages and disadvantages, these were studied to implement 1-bit full adder. The designs studied were classified into two categories static and dynamic. Static consumes less power and high area with reliability. But dynamic adder has lesser area compared to static adder [3, 4].

As mentioned above full adder is basic block for complex circuits. As full adder reduces circuit complexity and hence used to construct higher bit adders and multipliers. Everyone is relying in battery and performance. Addition is the basic function used in arithmetic operations and used in biomedical applications. Processor chip which consists of ALU (Arithmetic Block unit) consists of full adder. This Block is used to make operations like addition, subtraction, multiplication, and many other operations. Basic operation of 1-bit full adder is to add three 1-bit numbers A, B, and Cin. A and B are the inputs, and Cin is a bit carried in from the previous stage.

Different logic styles will have their own performance parameters at the cost of other parameter. Design which use combination of different traditional logic styles comes under hybrid design. Hybrid designs explore the merits of different logic styles to improve the performance parameters of the full adder.

2 Previous Work

Low-power full adders are optimized using different logic styles.

M. Hosseinghadiry et al. have discussed about the recent trends and traditional adder circuits and studied about the static and dynamic adder circuits and combined them and proposed hybrid full adders [5] with static and dynamic properties.

Complementary pass-transistor logic (CPL) full adder produces the output using the internal nodes and their inverted result. It consumes low power as the stack height is low and the internal voltage swing is small. But due to small voltage swing at the inverters there will be static power consumption which was discussed in N. Zhuang and H. Wu (1992) "A new design of the CMOS full adder" [6].

For implementing a circuit the transmission gate logic requires double the number of transistors than pass transistor logic. Twenty transistors were used in transmission gate adder and 16 for the transmission function full adder which uses pass transistor.

Pass-transistor logic and its design for reduced power consumption were discussed in A. Parameswar, H. Hara and T. Sakurai (1996) "A swing restored pass-transistor logic-based multiply and accumulate circuit for multimedia applications" [7].

Several conventional adder circuits and significance of XNOR circuit in full adder and the reduction of power and delay by using different transistors and logic styles which leads to hybrid adder design was discussed in Partha Bhattacharyya,

Bijoy Kundu, Sovan Ghosh, Vinay Kumar, and Anup Dandapat (2014) "Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit" [8].

This work lead to the motivation for the design of modified low-power hybrid 1-bit full adder.

3 Conventional Full Adders

3.1 Complementary CMOS Adder

The C-CMOS adder [3] shown in Fig. 1 is a regular pull-up and pull-down network. It consists of 28 transistors but it consumes more power and area due to more number of transistors.

3.2 Mirror Adder

Mirror adder [9] is based on the symmetrical arrangement of the NMOS and PMOS transistors. Carry in signal is connected to the transistors which are nearer to the

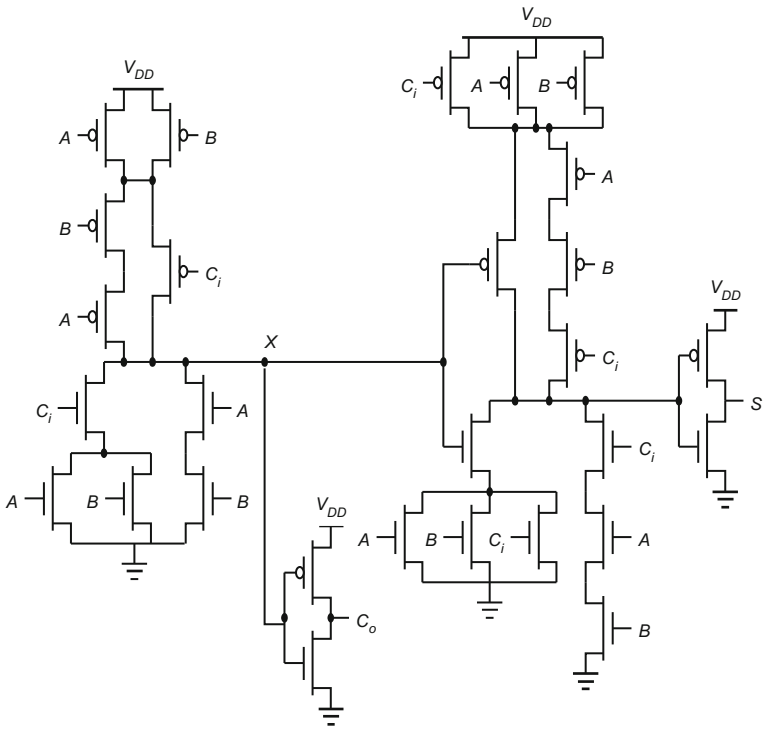


Fig. 1 Complementary CMOS adder circuit

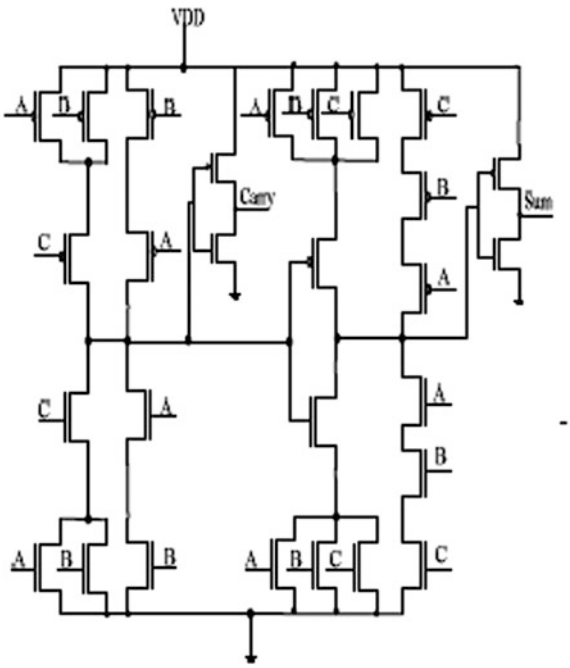


Fig. 2 Mirror adder

output node such that the transistor can be optimized for the lesser delay of the adder. Transistors generating sum can be designed of small size. The arrangement of transistors is different and it also has 28 transistors as shown in Fig. 2.

3.3 HPSC Adder

The hybrid pass-logic (HPSC) full adder [9] shown in Fig. 3 uses 22 transistors and the equations used to design this adder are given in Eqs. 1 and 2.

$$\text{Sum} = \text{H xor Cin} \tag{1}$$

where

$$\text{H} = \text{A xor B}$$

$$\text{Cout} = \text{A.H}' + \text{Cin.H} \tag{2}$$

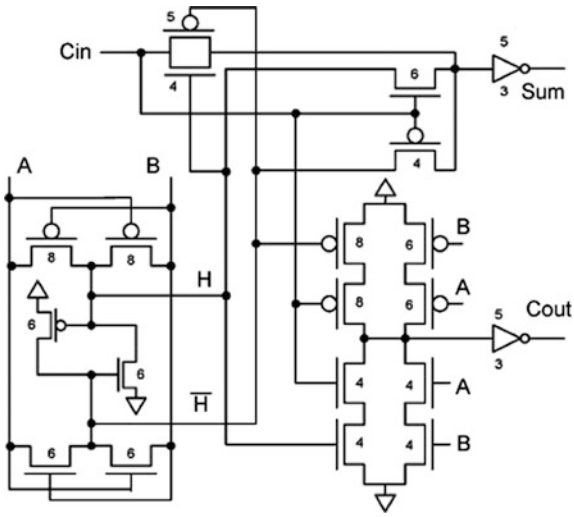


Fig. 3 HPSC adder

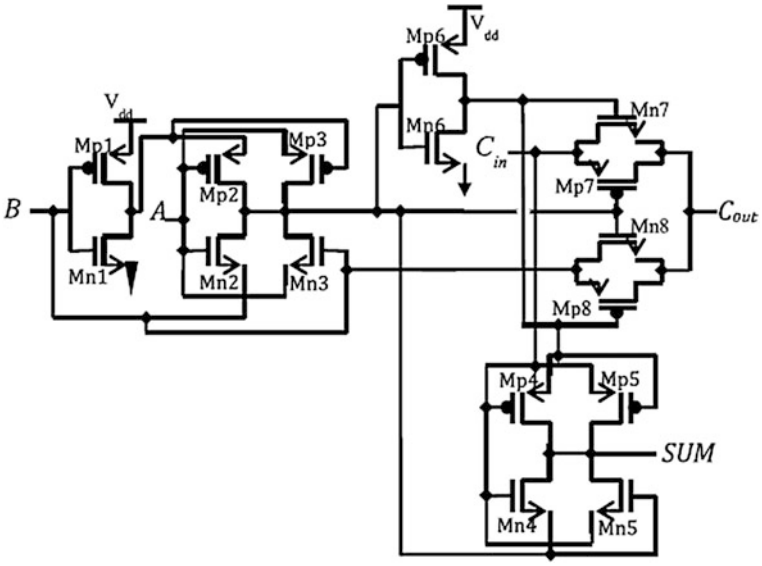


Fig. 4 Hybrid 1-bit full adder

3.4 Hybrid 1-Bit Full Adder

The hybrid 1-bit full adder [8] consists of 16 transistors is shown in Fig. 4 and is designed by XNOR and carry generation modules.

4 Proposed Work

4.1 Proposed XNOR Circuit

The proposed XNOR circuit shown in Fig. 5 is designed with two NMOS and two PMOS circuits, where the nmos transistors are arranged as the pass transistor logic and it gives output as AND gate for inputs 00-0, 01-0, 10-0, 11-1, and when the input is 00 for XNOR we should obtain 1 as output so we use two PMOS transistors arranged in circuit such that it gives output as 1. Hence, we obtain 00-1, 01-0, 10-0, 11-1.

4.2 Proposed Adder

The 1-bit full adder designed by considering the above circuits and proposed XNOR circuit such that the optimal value of power and delay were obtained without degrading the output and the swing of output is obtained successfully.

Implementation. The proposed full adder circuit block diagram is shown in Fig. 6. Sum signal is generated by the first two modules, i.e., 1 and 2 which are XNOR modules and the output carry signal is generated by carry generation module, i.e., 3. Now the basic element is XNOR in full adder so we use proposed XNOR module to reduce power.

The proposed 1-bit full adder is shown in Fig. 7 and it consists of proposed XNOR circuit as module1 and the other XNOR module is taken from the design of hybrid 1-bit full adder such that the output swing is restored and the carry generation module is designed with transmission gate. The proposed 1-bit full adder consists of 14 transistors which are less than hybrid 1-bit full adder.

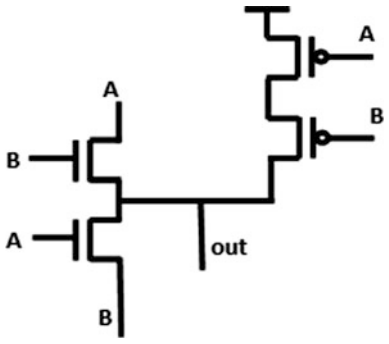


Fig. 5 Proposed XNOR gate

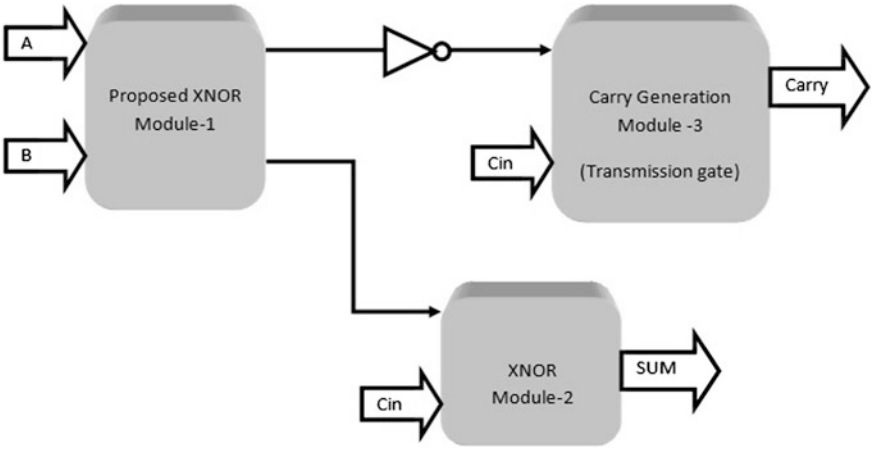


Fig. 6 Block representation of proposed full adder

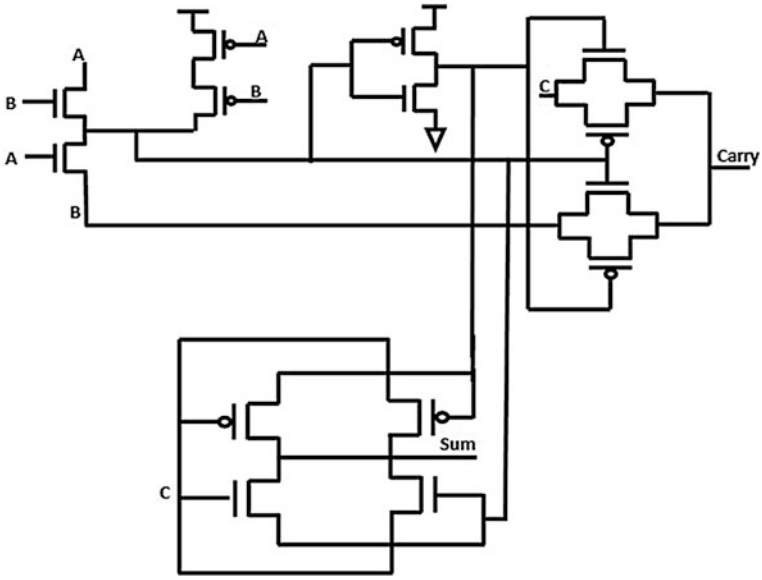


Fig. 7 Proposed full adder

5 Simulation Results

The Table 1 shows the results of the simulation of different full adder circuits.

From the Table 1 it can be seen that the power consumption of the proposed adder is 36.4% less than hybrid 1-bit Full adder and the power delay product is also reduced.

The Fig. 8 represents the graphical comparison of Power consumed by different full adder circuits and the proposed adder has least power consumption.

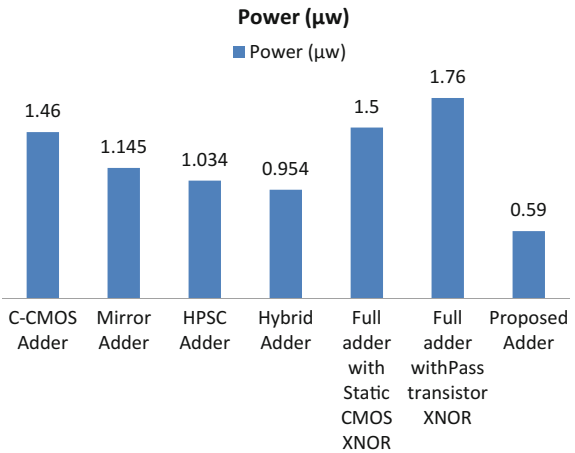
The Fig. 9 represents the graphical comparison of delay of different full adder circuits.

The Fig. 10 represents the graphical comparison of power delay product of different full adder circuits and the proposed adder has lowest power delay product.

Table 1 Comparison of power, delay, and PDP of benchmark circuits and proposed work

S. no.	Design	Power (µw)	Delay (ps)	PDP (fJ)
1	C-CMOS adder	1.46	58	0.085
2	Mirror adder	1.145	55	0.063
3	HPSC adder	1.034	163	0.169
4	Hybrid adder	0.954	8	0.008
5	Full adder with static CMOS XNOR	1.5	133	0.199
6	Full adder with pass transistor XNOR	1.76	19	0.033
7	Proposed adder	0.59	12	0.007

Fig. 8 Comparison of delay



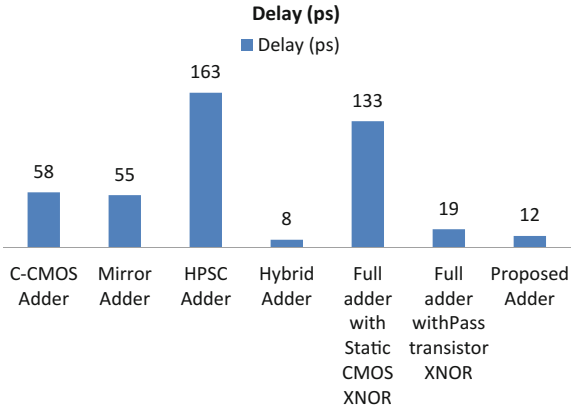


Fig. 9 Comparison of delay

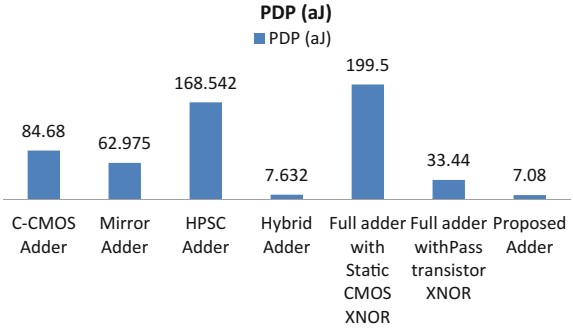


Fig. 10 Comparison of power delay product

6 Conclusions

In this research work, the simulation and analysis of C-CMOS adder, Mirror adder, HPSC adder, and hybrid 1-bit full adder are carried out using HSPICE with 90 nm technology. As the Hybrid adder is divided into modules and XNOR being the basic module for power consumption different XNOR circuits were considered and simulated in HSPICE 90 nm technology with supply voltage of 1.2 V and found proposed XNOR has the lowest power consumption of 0.34 μw. A full adder was designed by using proposed XNOR with 14 transistors and simulated using HSPICE 90 nm technology and found that power consumption of proposed adder, i.e., 0.59 μw is low compared to the benchmark circuits, i.e., C-CMOS adder, Mirror adder, HPSC adder and hybrid 1-bit full adder which has power consumption 1.46, 1.1451, 1.034, and 0.954 μw, respectively. When delay is compared there is a slight increase compared to the hybrid 1-bit Full adder but has the low-power delay product than benchmark circuits.

References

1. C.-K. Tung, Y.-C. Hung, S.-H. Shieh, G.-S. Huang.: A low-power high-speed hybrid CMOS full adder for embedded system, in Proc. IEEE Conf. Design Diagnostics Electron. Circuits Syst., vol. 13, pp. 1–4 (Apr. 2007).
2. S. Goel, A. Kumar, and M. A. Bayoumi.: Design of robust, energy efficient full adders for deep-submicrometer design using hybrid-CMOS logic style, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1321, (Dec. 2006).
3. J. M. Rabaey, A. Chandrakasan, and B. Nikolic.: *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Delhi, India: Pearson Education, (2003).
4. N. H. E. Weste, D. Harris, and A. Banerjee.: *CMOS VLSI Design: A Circuits and Systems Perspective*, 3rd ed. Delhi, India: Pearson Education, (2006).
5. M. Hosseinghadiry, H. Mohammadi, M. Nadisenejani.: Two New Low Power High Performance Full Adders with Minimum Gates, *International Journal of Electronics, Circuits and Systems*, Vol. 3, No. 2, pp. 124–131 (2009).
6. N. Zhuang and H. Wu.: A new design of the CMOS full adder, *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 5, pp. 840–844 (1992).
7. M. Aguirre-Hernandez and M. Linares-Aranda.: CMOS full-adders for energy-efficient arithmetic applications, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 4, pp. 718–721, (Apr. 2011).
8. Partha Bhattacharyya, Bijoy Kundu, Sovan Ghosh, Vinay Kumar and Anup Dandapat.: Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit, IEEE Transactions on very large scale integration (vlsi) systems, (September 2014).
9. Subodh Wairya, Rajendra Kumar Nagaria and Sudarshan Tiwari.: Comparative Performance Analysis of XORXNOR Function Based High-Speed CMOS Full Adder Circuits For Low Voltage VLSI Design, International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.2, (April 2012).

FinFET Modelling Using TCAD

Sreenivasa Rao Ijjada, Chaithanya Mannepalli and Md. Hameed Pasha

Abstract Digital device are playing a crucial role in everyone's life, hence, they are seeking for compact and high-performance devices which can be handled easily. For this researchers made drastic changes to the technology by scaling down the device for lesser area and high performance, but beyond some limit the CMOS device turned in opposite by showing short-channel effects. To subdue them, we design FinFET using TCAD tools, which has superior control over the channel and displays higher performance even after scaling to lower dimensions.

Keywords Short-channel effects · MOSFET · TCAD · FinFET

1 Introduction

MOSFET is the fundamental building block of CMOS integrated circuits [1]. It produces many disadvantages while it is being scaled, the most of which are the short-channel effects and leakage currents [2]. While dealing with short-channel effects in bulk MOSFET, body doping concentration increases and consequently there is a trade-off between the carrier mobility and tunnelling effect, eventually increasing the off-state currents. This leads to increase of parasitic capacitances.

In order to have a control on the DIBL effect, high halo doping can be used but it degrades *on* current and increases the BTB Tunnelling. High-K dielectrics can support to reduce serious gate leakages in short-channel devices. To utilize the

S.R. Ijjada · C. Mannepalli (✉)
Electronics and Communication Engineering,
GITAM University, Visakhapatnam, India
e-mail: chaithanya15992@gmail.com

S.R. Ijjada
e-mail: isnaidu2003@gmail.com

Md. Hameed Pasha
Jayamukhi Institute of Technological Sciences, Narsampet, India
e-mail: hameedjits@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_21

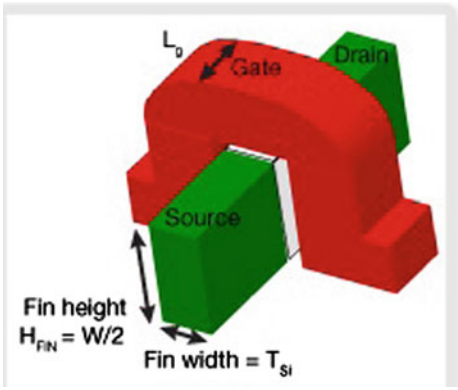


Fig. 1 Geometric description of FinFET

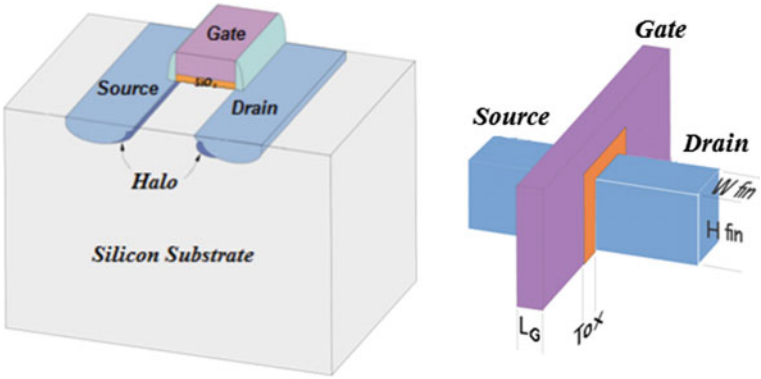


Fig. 2 Planar view of MOSFET and FinFET

advantages of device scaling with minimized SCEs beyond 20 nm technology node the device structures are continuously trying to modify, results FINFET.

FinFET results due to the relentless increase in levels of integration. Based on the earlier depleted lean-channel transistor design [3], FinFET is built on an SOI substrate making it a non-planar and double gate device [4]. FinFET gate is bent up and narrowed down and the FET structure so obtained looks like set of fins when viewed as shown in the Fig. 1 [5]. FinFET have three modes; single gate, double gate and trigate. Double gate reduces DIBL and improves threshold swing.

The dimensional parameters of a FinFET are the height and thickness of the fin and the "critical design dimension" is defined by the drawn gate length that separates the nodes of source and drain. A vertical fin protrudes above the substrate as it traverses from one side of the fin to the other enabling to interface with three sides of the fin or channel as shown in the Fig. 2. It provides a better electrical control over the channel and helps in reducing leakage current and SCEs, thereby achieving high on-current. Thickness of the fin determines the effective channel length of the device.

Effective gate length,

$$L_{eff} = L_{gate} + 2L_{ext} \tag{1}$$

Effective gate Width,

$$W_{eff} = T_{fin} + 2H_{fin} \tag{2}$$

Channel Width,

$$n_{fin} * h_{fin} \tag{3}$$

where, 'n' is the number of fins used. More number of fins is preferred to achieve the constraint of the device performance. FinFET has near ideal sub-threshold behaviour, which is nearly impossible with planar technology.

2 Modelling

Substrate with Undoped/doped Boron–Silicon Nitride hard mask with photo-resist material is patterned over a lightly doped p-substrate with the process of film deposition and photolithography. Fin channel patterning–Fins are formed with highly anisotropic etch process in a specific time limit as there is no stop layer on a bulk wafer as in the SOI. Oxide deposition and planarization—Here, the aspect ratio is kept high and then the oxide is planarized by chemical–mechanical polishing by making hard mask layer as the stop layer. Gate oxidation, patterning and deposition—On top of the fins the gate oxide is deposited through thermal oxidation to separate the channel from the gate electrode. Dopant activation—Since underneath the oxide the fins are still connected, a dopant junction is created due to a high-dose implant at the base of the fin which completes the isolation.

TCAD has certain design flow to design and test the designed device. The flow of TCAD is shown in Fig. 3.

Before, we go for device characterization we need to model the device in TCAD. Device modelling can be done with the following steps at first we need to define the regions and select the materials to be used for designing. Next, we need to place the nitride spacers to avoid lateral diffusion and define the contacts of the modelled device. After, the first two steps we need to define the doping concentration of the source and drain regions, when the doping and the device modelling is done we need to mesh the device there are two meshing global and local meshing. Where global is used to cover entire device and local is used to cover the junctions.

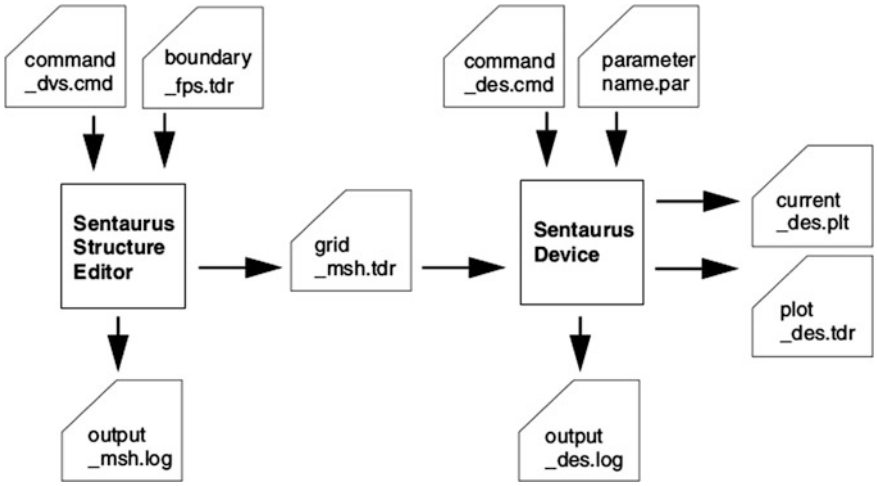


Fig. 3 Tool flow in synopsys TCAD

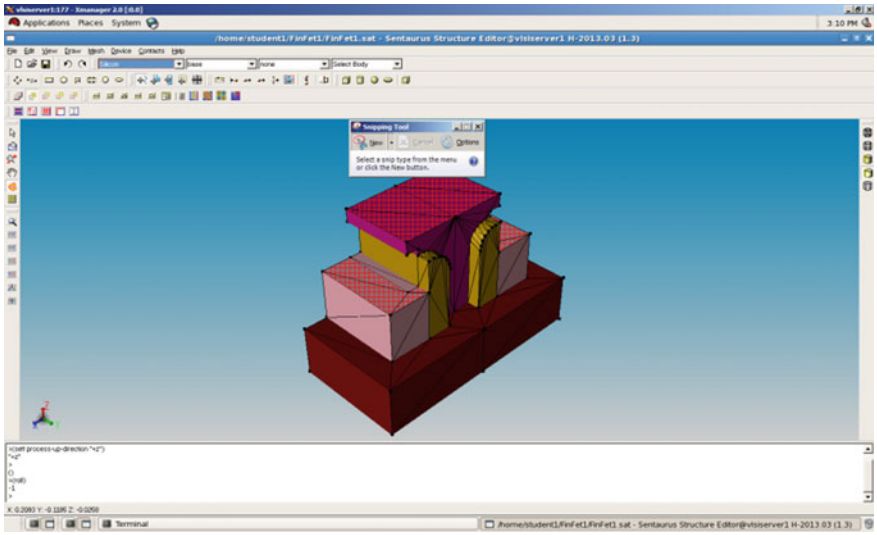


Fig. 4 Three-dimensional FinFET device

For meshing we use command (sde:build-mesh "snmesh" "" "device_name"). Meshing is the final step before device characterization after meshing is successful we go for inspect command for analyzing the modelled device.

The modelled device can be viewed in mesh viewer or tecplot as shown in Fig. 4.

Mathematical Modelling for FinFET

The mobilities of medium- or short-channel devices, however, are not readily extractable from raw capacitance and drain current data due to non-negligible parasitic effects as in the long channel devices.

The different regions of operation of FinFET according to the Ids and V_{ds} Equations is given as follows

The current equation in saturation region goes as follows

$$I_{ds} = \mu C_{ox} \frac{W}{L} \left(\frac{V_g - V_t}{2m} \right)^2, \tag{4}$$

where

$$m = 1 + 3\frac{t_{ox}}{x_d}, \tag{5}$$

x_d is the depletion layer thickness.

In cut- off region, $V_g < V_t$, and the current equation changes to

$$I_{ds} = \mu \frac{W}{L} kTn_i t_{si} s^{\frac{q(V_g - \Delta\phi)}{kT}} \left(1e^{\frac{-qV_{ds}}{kT}} \right). \tag{6}$$

And in the linear region where $V_g > V_t$, I_{ds} increases linearly with V_{ds}.

$$I_{ds} = 2\mu C_{ox} \frac{W}{L} \left(V_g - V_T - \frac{V_{ds}}{2} \right) V_{ds} \tag{7}$$

The threshold voltage of FinFET is given by the Eq. 8

$$V_{th} = \phi + n\frac{kT}{q} \ln \left(\frac{2C_{ox}kT}{q^2 n_i t_{si}} \right) + \frac{h^2 \pi^2}{2m_{ds} W_{si}^2} \tag{8}$$

3 Simulation

By using Tecplot environment FinFET structures are obtained are shown in the Figs. 5 and 6. Tecplot 360 is an integrated post-processing environment that allows analyzing the detailed flow-field data while producing exceptional visual output. It is a computational fluid dynamics (CFD) and numerical simulation software package.

Contour lines/contour—It joins points of equal elevation (height) above a particular given level. Basically, it is used to calculate pressure or temperature.

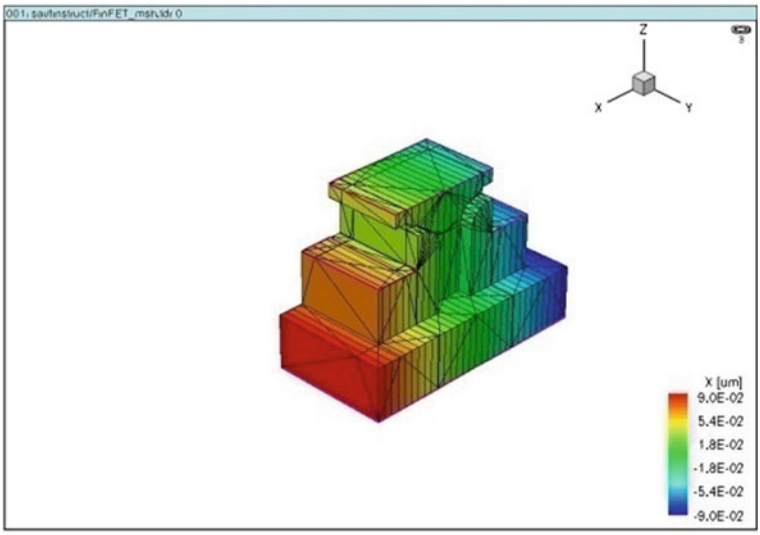


Fig. 5 Three-dimensional FinFET with mesh and contours

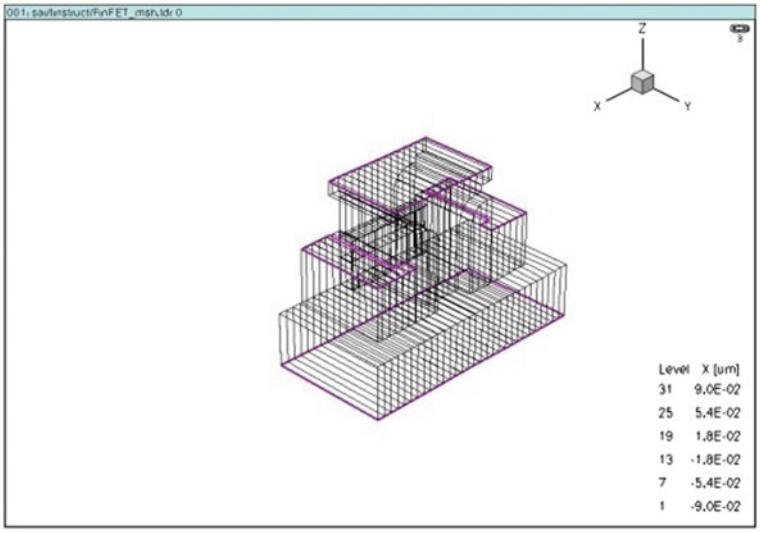


Fig. 6 Three-dimensional FinFET with different contour levels

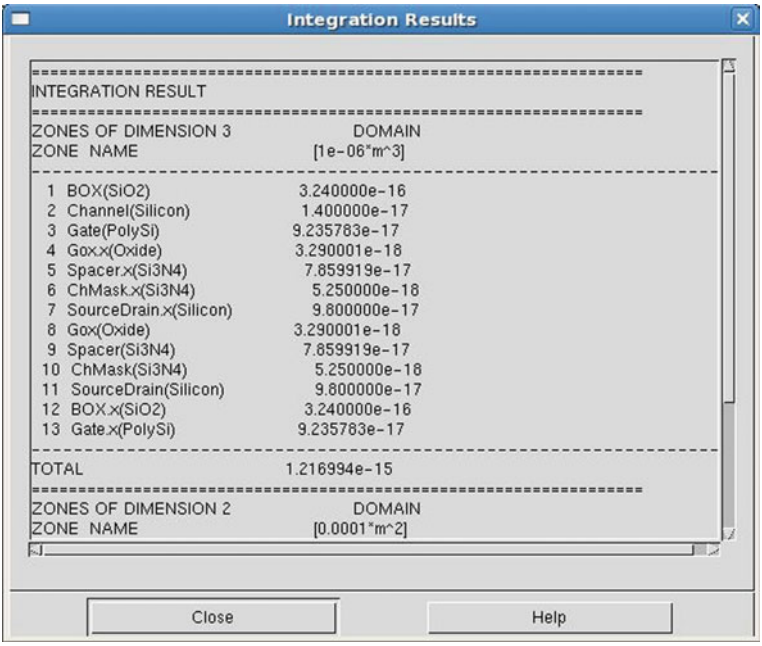


Fig. 7 Integration results for FinFET designed structure

Integration method—It is a trapezoidal method, i.e., second-order accurate. For each cell, the cell-centred value of the quantity being integrated is multiplied by the volume of the cell, and is summed over all cells.

- When the integrand is node-centred, the nodal value of the face nodes is averaged.
- When the integrand is cell-centred, the values of the cells to either side of the face are averaged.

After the integration method the Fig. 7 shows the integration results of FinFET.

4 Results and Analysis

After structure of FinFET is designed, the study of characteristics of FinFET structure is important via transfer characteristics, output characteristics and trans-conductance. The drain currents versus gate voltage at the low drain bias of selected medium channel n-channel FinFETs are obtained with the extracted mobility. The calibrated I_{ds} versus V_{gs} data is shown in Fig. 8 for $V_d = 0.1$ V and $V_d = 1.5$ V.

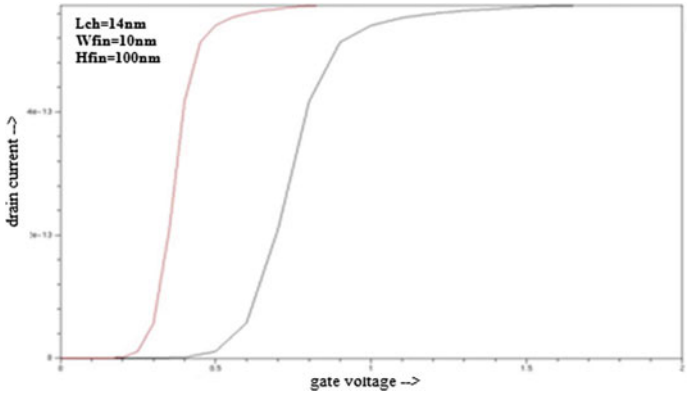


Fig. 8 FinFET transfer characteristics

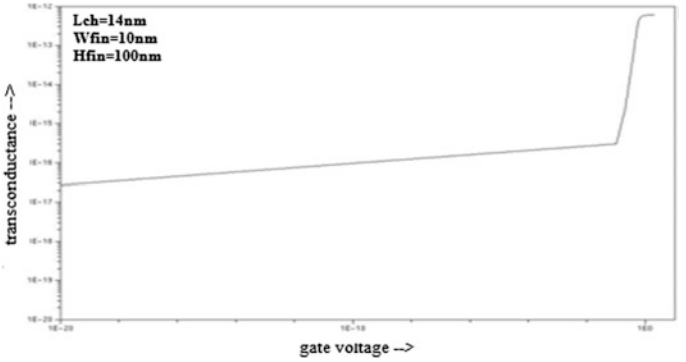


Fig. 9 Transconductance versus drain current of FinFET

In order to model I_{ds} versus V_{ds} graph at high drain bias, the inclusion of high field effects is necessary. The experimental FinFETs does not suffer from excessive channel length modulation, due to the superior gate-controllability over the channel region.

With high gate overdrives, degradation of transconductance *gm* is observed with the Fig. 9. The drain current does not increase linearly proportional to $1 = L$ because the parasitic resistance effects in addition to the mobility degradation due to the relaxed tensile strain. In other words, the normalized drain current degrades towards shorter gate lengths.

The Fig. 10 shows the output characteristics of FinFET from which we can infer that at a positive V_d, a horizontal electric field is formed which is smaller than the thin oxide field which gives rise to the channel formation. Keeping V_g same, if V_d increases, pinched-off portion forms depletion region with high electric field and then it enters into saturation region (I_d remains same).

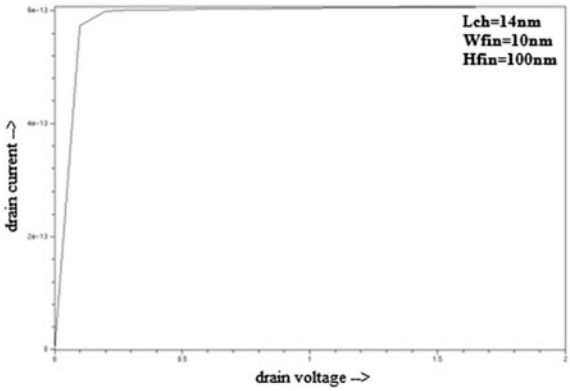


Fig. 10 Output characteristics of FinFET

The drain current plots are in an excellent agreement with the experimental data in all bias regimes. Channel length modulation effects are not excessive in the experimental data due to the excellent control of gate over the channel region.

In the transfer characteristics, since the gate terminal is electrically isolated from the remaining terminals, the V_g is almost equal to 0, this is why, Ig is not the part of the transfer characteristics. From the transfer characteristics graph, we infer that as V_{gs} increases for nFET (for V_{gs} between 0 and 0.5 V, Id is almost equal to 0). This means that equivalent resistance between drain and source terminals are extremely high. Once V_g reaches 0.4 V, the current increases rapidly with V_g indicating that the equivalent resistance at the drain decreases with the increase in V_g. Therefore, nFET has the threshold voltage of 0.4 V. By analyzing the output characteristics of FinFET, we find that at a positive V_d, a horizontal electric field is formed which is smaller than the thin oxide field which gives rise to the channel formation. If V_d increases (when V_g is same), pinched-off portion forms depletion region with high electric field while entering into the saturation region.

5 Conclusions and Future Scope

The usage of FinFET's in the nanodevices has improved results than the MOSFETs. FinFET's overcome the short-channel effects faced by scaled down MOSFET's to operate successfully at lesser channel length. The FinFET developed can be used for suppressing the leakage current and performance enhancement in other circuits like Adder, Schmitt Trigger circuits, and so on. The FinFET-based applications can be extended to various fields, such as nano robots, bio sensing, analog, and RF circuits. The device performance may be also improved by using alternate materials like carbon nano tubes or graphene. This could increase the speed of operation and provides better control over the channel and reduces power consumption. The FinFETs finds suitable in the integration of Si-ULSIs.

References

1. SUNG MO (STEVE) ANG and Yusuf Leblebigi.: CMOS Digital Integrated Circuits Analysis and Design.
2. Vaidy Subramanian, Bertrand Parvais, Jonathan Borremans, Abdelkarim Mercha, Dimitri Linten, Piet Wambacq.: Planar Bulk MOSFETs Versus FinFETs: An Analog/RF Perspective, IEEE Transactions on Electron Devices.
3. Xiaoxia Wu Feng Wang Yuan.: Analysis Of Subthreshold Finfet Circuits For Ultra-Low Power Design, The Pennylvania State University, USA.
4. http://www.inst.eecs.berkeley.edu/~ee130/sp06/chp7full.pdf: MOSFET Technology Scaling, Leakage Current, and Other Topics.
5. http://www.radio-electronics.com/info/data/semicond/fet-field-effecttransistor/finfet-technology-basics.php.

Pipeline Decimal Multiplier Using Binary Multipliers

Hari Pattimi and Rajanbabu Mallavarapu

Abstract Decimal multiplication became the common practice for human computations. The results of the digital computers which were used for the decimal arithmetic operations for various financial and commercial applications should be same when compared with the human made calculations. The slightest error in these calculations may arise greater complications and may cause severe damage. Thus, the importance of decimal computer arithmetic has recognized by the standard floating-point arithmetic IEEE-754 2008. Several design approaches have been proposed already for the decimal arithmetic circuits to perform various operations like decimal addition, multiplication, subtraction, and division. In recent times, significant amount of efforts has been put on the development of Decimal IP cores to reduce the bottleneck in reconfigurable computing architectures. In this article, the pipeline decimal multipliers using binary multiplier architecture has been proposed. The proposed pipelined decimal multiplier has increased the throughput significantly, by reducing overall propagation delay. The architecture is implemented in 8-and 16-bit decimal operands on SPARTAN-3E FPGA architecture. This also helps to understand that which FPGA Architecture is optimal for the proposed multiplier. The performance comparison between proposed pipeline and non-pipeline decimal multiplier using binary multiplier on various FPGA Architectures were also discussed.

Keywords Decimal multiplication · FPGA

H. Pattimi (✉) · R. Mallavarapu
Department of ECE, Lendi Institute of Engineering & Technology,
Jonnada, Vizianagaram, Andhra Pradesh, India
e-mail: hari.lendi@gmail.com

R. Mallavarapu
e-mail: mrajanbabu@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_22

1 Introduction

Decimal multipliers are widely used major arithmetic element used for various applications not only limited to processor applications. In fact, the multipliers were the key component in digital signal processing, digital transformations, digital communications, and various other applications. The digital circuits perform arithmetic operations in binary format. Thus, the input data provided to these circuits should be in binary format. But, when the digital circuits are operated for the human-centric applications most of the data will be available in the decimal format. The human-based information processing methodologies use the decimal arithmetic rather than binary arithmetic. It is practically not possible to process the human-centric applications using binary arithmetic or translating the information and providing it to a digital circuit in binary format. And the human-based information processing is generally more error prone than a computer based processing. To avoid this risk, the traditional approach is using a binary to BCD converters input and processing the data and again converting back to decimal. This was the favorable approach until recent times. It involves less complexity, but the cost comes in the aspect of overhead. The pre-and post-conversion became the bottleneck for the speed of information processing.

In recent times, the decimal arithmetic-based computations were increased numerously as the decimal arithmetic used in various computing application similar to scientific, numerical, finite element, scientific, signal processing, analog/digital communication, digital signal processing, transformations, and Internet-based applications. But, the performance of the decimal arithmetic circuit with binary to decimal converters and vice versa are costing the design performing severely. If such kind of decimal multiplier is used for large data processing arrays in Iterative approach, more than 50% of the system resource are wasted toward the pre-and post-conversion for the data. This may lead to poor performance of the system.

The another problem associated with the traditional approach is the decimal numbers may not be able to properly represented by a finite number of bits in binary information. Apart from this, the rounding off and normalization of the data may insert additional delay and may produce the results with some deviation. As alternate to this approach, software algorithms to perform the binary arithmetic for the decimal data was developed. But, this method is significantly slower when compared to the hardware approach. Thus, this software algorithm approach was not the preferred choice for major applications [1]. As an alternate to this approach, the evolution of dedicated decimal arithmetic circuits was incorporated inside the digital processors to improve the execution speed such as IBM Power6 has a dedicated hardware code for decimal floating-point operations [2].

The decimal multiplication and binary multiplication both are different from each other. The decimal multiplication is a much more complex process than binary multiplication. This is due to the problem associated with representing decimal numbers using a binary number system. The carry information about the bit and

digit were different and invalid results were also must be considered in order to obtain the correct results.

Iterative and parallel are the two major approaches in the design of a decimal multiplication. When the multiplier is used for the iterative kind of approach, the partial products will be generated by multiplying one digit of the multiplier multiplied iteratively with the multiplicand. After this, the generated partial products will undergo the shift and add to produce the final decimal product. The sequential decimal multipliers were also proposed in [3, 4]. These approaches were implemented in such a way that the partial products were generated during the preprocessing step. Then, the partial products selectively added according to the value of the multiplier digits. There have been several attempts were made to improve the performance [4–6]. The design proposed in [4], the partial products are generated in concurrent and the addition of partial products was carried out by decimal carry-save addition tree. This parallel multiplier approach can be much faster than the iterative ones, but the area of the multiplier will be significantly large, which is not quite suitable for major applications.

The decimal multiplier in binary can be implemented in sequential, in parallel, or by semi-parallel approach [7]. There have been several efficient architectures have been proposed in recent times [4, 8]. This article focuses on fully parallel BCD multiplier architecture. The focused fully parallel BCD multiplier architecture generally a three-step process briefly shown below (Fig. 1):

a. PPG: This stage calculates the partial products for every bit of multiplier (Y) with the multiplicand (X) on iterative mode, where the W_i and Y^i is equal to the power of the radix [7].
b. PPR: This is partial product reduction tree, which is a major step in parallel multiplication [9, 10]. This reduces the tree leads to a redundant intermediate representation of product.
c. Final product Computation: The redundant product generated after PPR, the result will be converted to the final BCD product (e.g., via a BCD adder [11]).

The decimal multipliers produce the decimal partial products directly from the decimal number as input. Once producing the decimal partial products, the decimal adder will be used to perform the addition. Instead of using this approach, there has been a new scheme was developed in order to make use of the binary multipliers on

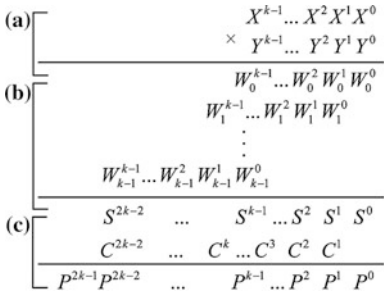


Fig. 1 The parallel decimal multiplication

the chip to save the area and to achieve maximum resource utilization. In this new scheme, the BCD input will be converted to binary and performing the multiplication using binary arithmetic multiplier. Once it produces the binary product, the result will again have converted from binary to BCD. This approach is having the trouble at the binary to BCD conversion and vice versa is too slow. The fast parallel implementation was another new approach proposed in [12]. This fast parallel architecture has showed a significant improvement in the efficiency of the design. But, the area occupied by fully implementation technique is more. But, the throughput of the existed design can be further this paper proposes a pipeline architecture for the existed parallel decimal multiplier model [12].

2 Decimal to BCD Conversion

The data from decimal to binary format conversion can be achieved by performing least common divisor by the number 2. Or the division can be achieved by right shifting the data toward the least significant bit. However, when the bit shifted to the next nibble boundary, the lower decimal value must be subtracted by 3 or must be added with 5 with the most significant removed.

Apart from the above-mentioned, the decimal to binary conversion can also be carried which is described by the below Eq. (1)

$$\mathrm{D_{n-1}} \ldots \mathrm{D_0} = \mathrm{D_{n-1}} 10^{\mathrm{n}-1} + \cdots + \mathrm{D_0} 10^0 \tag{1}$$

By closely observing the above equation closely, the multiplications by the powers of ten and to perform such operations the design would require significantly large multipliers. This can be overcome by rearranging the above equation as shown below

$$D = (((D_{n-1}10 + D_{n-2})10 + : :)10 + D_0) \tag{2}$$

The rearranged equation requires multiplications by 10, this can be implemented by shifting and addition instead of using multiplier to reduce the size and the complexity. In brief, the multiplication by 10 is similar with the multiplication with 8 + 2. To multiplied value by 2 and 8 can be obtained by shifting the data toward most significant bit. The Eq. (2) can be further described as shown in Eqs. (3)–(5)

$$D = (((D_{n-1}10 + D_{n-2})100 + \ldots)100 + (D_1 10 + D_0)) \tag{3}$$

$$D = \left(((D_{n-1}100 + D_{n-2}10 + D_{n-3})10_3 + \ldots)10^3 + (D_2 100 + D_1 10 + D_0)\right) \tag{4}$$

$$D = ((D_{n-1}10 + D_{n-2})100 + (D_{n-3}10 + D_{n-3}))10^4 + \cdots + ((D_3 10 + D_2)100 + (D_1 10 + D_0)) \tag{5}$$

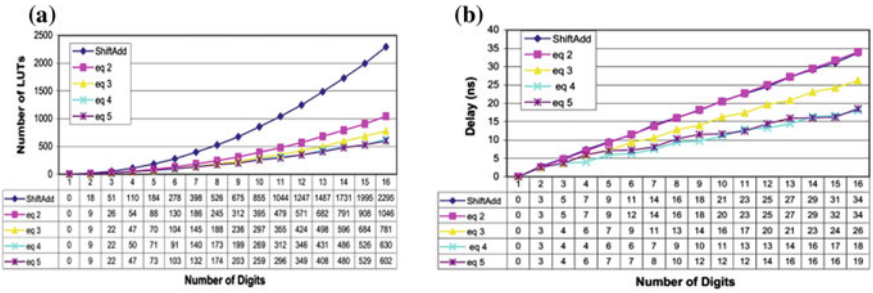


Fig. 2 **a** Case study on the size of the decimal to binary converter for different implementation, **b** delay of the decimal to binary converter for different implementations [11]

The above equations offer more parallelism and suitable to implement the low cost architectures. The Fig. 2b indicates the delays associated with the implementations follow a similar relation. The shift and add method of decimal multiplication is having poor area constraint. The most suitable alternative for this approach is can be derived from the Eqs. 4 and 5 by saving the area to 50–75% than shift and add method.

3 Binary to Decimal Conversion

The conversion of Binary to decimal data is expressed in the below Eq. (6) in decimal.

$$b_{n-1} \cdot 2^{n-1} + b_{n-2} \cdot 2^{n-2} + \cdots + b_0 \cdot 2^0 \tag{6}$$

The above equation indicates the multiplying bit position value by 2, this could be achieved by shift toward the MSB. However, as the operation is in BCD whenever a bit shifts over the boundary the normalization should take place by adding three. The basic module known as (b2TOb1000) which converts binary to decimal information up to 999 × 999 to base 1000. The converter consisting of three blocks: (1) b2TOb1000, (2) A module to compute 24x + y, (3) adder. The density of these blocks required at the output are purely depends on the size of the number and increased in proportional with the size of the binary number to be converted [13].

For the converter for 8-digit numbers,

$$\begin{aligned} b &= b_1 \cdot 2^{17} + b_0 \qquad b_1 \le 762 = \left(10^8 - 1\right)/2^{17} \\ &= 131 \cdot b_1 \cdot 10^3 + b_1 \cdot 72 + b_0 \qquad b_0 \le 2^{17} \end{aligned} \tag{7}$$

$$\text{and} \quad C = b_1 \cdot 72 + b_0$$

$$C \leq \left(2^6 + 2^3\right) \times b_1 + b_0 < 2^{18} \quad \leftarrow 17 \text{ bits} \tag{8}$$

The b2TOb1000 can be already applied to determine the least significant digit, d_0, and part of the following digits, d_1 [13],

$$d = d_1 \times 10^3 + d_0, \text{where } d_1 \leq 185 \leq 2^8 \quad \leftarrow 8 \text{ bits} \tag{9}$$

$$b = (b_1 + d_1) \times 10^3 + d_0, \qquad e \leq 10^5 + 7 \quad \leftarrow 17 \text{ bits} \tag{10}$$

$$e = (b_1 + d_1)$$

Since e can be represented with 17 bits, the b2TOb1000 block can be used to obtain the last two most significant base 1000, that is

$$e = d_2 \times 10^3 + d_1 \tag{11}$$

A hardware implementation of this converter can be designed using a set of adders and the b2TOb1000 unit. Instead of two modules 24x + y and two adders, this new approach use only one module that calculates 72x + y and one adder.

4 Parallel Decimal Multiplier

To perform the decimal multiplication using binary multipliers, the decimal data will be converted into binary, perform the multiplication then converting the result back to decimal format. For this, the design approaches can be implemented in two ways. Such as

a. Perform the multiplication in binary format and converting the input and output operands using the converters.
b. Differentiate the input operands and perform the addition to the partial products.

The first approach implemented with the converters, besides the multiplier, while the second approach needs extra adders, to add the partial products, and several converters. However, in the first approach the converters are large and, given the analysis of the previous section, will utilize much more area than the converters used in the second approach.

The decimal multiplier using decimal partial products of size 8-bit size is shown in the Fig. 3. The input operands were divided into two group with the size of 4-bit each. With every set of 4-digit, the multiplications will be carried out and its results will be arranged. Then the partial products will be performed addition in binary, then converted to decimal. The 16 × 16 decimal multiplier was implemented by converting the subgroups of digits of the operands to binary performing the cross multiplications. Then the inner partial products were arranged and added in binary. And the three sets of partial products were added in decimal as shown in Fig. 4.

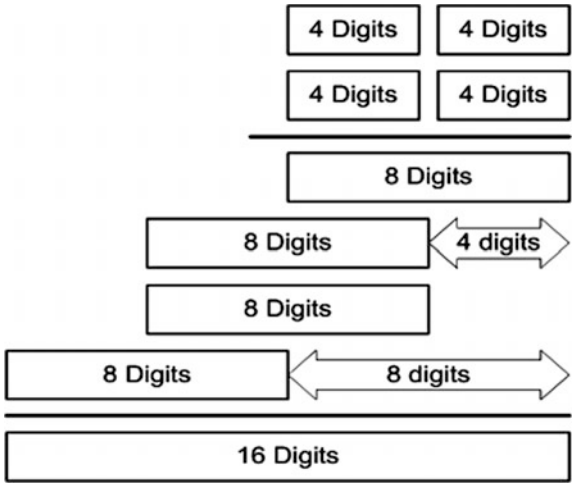


Fig. 3 8-bit decimal multiplier using decimal partial products [13]

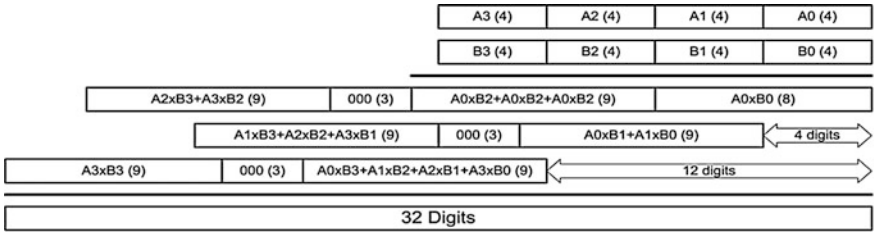


Fig. 4 16-bit decimal multiplier using decimal partial products [13]

5 Pipeline Decimal Multiplier with Decimal Partial Products

The most efficient parallel decimal multiplier using decimal partial products has been discussed in [12, 14]. The parallel decimal multipliers consume large design resources to generate the partial products and adders to perform addition. The proposed pipeline decimal multiplier using decimal partial products will increase the throughput, thus capable of performing more multiplications. The pipeline decimal multiplier architecture is shown in Fig. 5.

The performance comparison between conventional and pipeline decimal multiplier is shown in the Fig. 6.

The proposed pipeline architecture has improved the throughput and the area-delay product (ADP) of the proposed pipeline architecture is 40% lesser than the conventional decimal multiplier. Apart from this, the pipeline architecture has

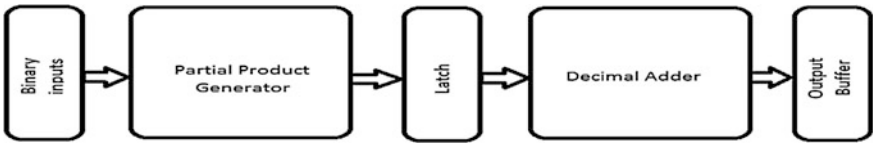


Fig. 5 Proposed pipeline decimal multiplier

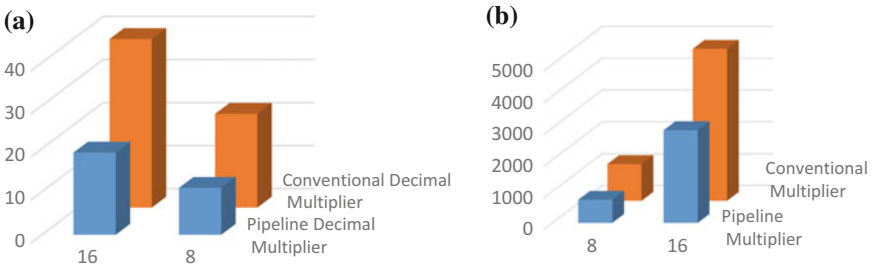


Fig. 6 **a** Delay comparison, **b** area—delay product (ADP) comparison between conventional and pipeline decimal multiplier

obtained the throughput by twice with the area cost of 10% from the conventional architecture.

6 Conclusion

We have implemented an 8 × 8 and 16 × 16 pipeline decimal multipliers using binary multipliers. The results indicate that this approach is efficient than the conventional approach of designing the decimal multiplier with binary multiplier. This architecture could be effectively use in other FPGA architecture and other coarse-grained reconfigurable architecture as well. Further, focus on subdivisions of the initial operands over the performance and the consumed area can be taken as future scope of this design.

References

1. E. A. A. Vazquez, "Conditional Speculative Decimal Addition," in Proceedings of seventh conference Real Numbers Computers (RNC 7), July, 2006.
2. V. Marios P. and N. Horacio C., "Parallel Decimal Multipliers using Binary Multipliers," IEEE, pp. 73–78, 2010.
3. E. M. A. and S. M. J., "Decimal Multiplication via carry-save addition," in IEEE 14th IEEE International Conference on Application Specific Systems, June, 2003.

4. T. Lang and A. Nannarelli, “A radix-10 combinational multiplier,” in IEEE 40th International Ascilomar Conference on signals, systems and computers, Oct, 2006.
5. A. Vazquez, E. Antelo and P. Montushi, “A New family of high-performance parallel decimal multipliers,” in IEEE 18th Symposium on Computer Arithmetic, June, 2007.
6. L. Dadda and A. Nannarelli, “A Variant of radix-10 combinational multiplier,” in IEEE International symposium on Circuits and Systems (ISCAS), May, 2008.
7. G. Jaberipur and A. Kaivani, “Binary-coded Decimal Digit Multipliers,” IET Computers & Digital Techniques, Vols. 1, no. 4, pp. 377–381, July, 2007.
8. R. Richards, Arithmetic Operations in Digital Computers, Van Nostrand, 1955.
9. R. D. Kenney, M. J. Schulte and M. A. Erle, “High-frequency decimal multiplier,” in IEEE International Conference on Computer Design: VLSI in Computers and Processors, Oct, 2004.
10. L. Dadda, “Multi Operand Parallel Decimal Adder: A Mixed Binary and BCD Approach,” IEEE Transactions Computers, vol. 56, no. 10, pp. 1320–1328, Oct, 2007.
11. P. Alfke and B. New, “Serial code conversion between BCD and binary,” Oct, 1997. [Online].
12. M. F. Cowlishaw, “Decimal floating-point: Algorism for computers,” in IEEE 6th IEEE International Symposium on Computer Arithmetic, June 2003.
13. H. Neto and M. Vestias, “Decimal multiplier on FPGA using embedded binary multipliers,” in proceedings IEEE Field programmable Logic and Applications, 2008.
14. T.O. et al., “Apparatus for Decimal Multiplication using Binary Multipliers”. U.S Patent 4677583, June 1987.

Effect of Line Parasitic Variations on Delay and Energy of Global On-Chip VLSI Interconnects in DSM Technology

C. Venkataiah, K. Satyaprasad and T. Jaya Chandra Prasad

Abstract Interconnects are integral part in the chip design which are responsible for the flow of signal from input to output. Due to the presence of parasitic such as resistance, capacitance components, and intermediate devices, the signal integrity problems may occur. Nowadays, because of technological advances, the effects of parasitic are increasing, which are causing adverse effect on the circuit performance in terms of delay and power. So interconnects have become a major problem. In this paper an endeavor has been made to simulate and examine the effect of interconnects due to variation of line parasitic on the circuit performance parameters in various DSM technologies. Here the values of R and C have been estimated for copper interconnects in different technologies with variable lengths and developed a simple RC interconnect simulation model with a driver and load concepts. For the simulated interconnect model with different interconnect structures and variable lengths, delay and PDP values are estimated. Within the same technology, the simulation results of performance metrics indicate 10% variations for variable lengths of interconnects, 5% variation with different interconnect structures, and more than 50% variation in different technologies.

Keywords VLSI · Interconnect · Parasitic · Cu · Power · Delay · PDP

1 Introduction

VLSI is a method of making integrated circuits by combining countless transistors in an exceedingly single chip. In today's era as the technology gets more advances, the number of devices organized on chips increased, leading to more number of interconnects [1]. These interconnect now not behave as simple resistors but can

C. Venkataiah (✉) · K. Satyaprasad
JNTUK, Kakinada, AP, India
e-mail: venki.challa@gmail.com

C. Venkataiah · T. Jaya Chandra Prasad
RGMCET, Nandyal, AP, India

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_23

also have related parasitic consisting of capacitance and inductance, which leads to signal degradations. With growing need of transportable systems, low propagation delay and power dissipation are the major challenges for researchers. As the interconnect length increases linearly, the parasitic interconnect capacitance (C) and interconnect resistance (R) also increase linearly which in turn increase the RC product thereby increasing the propagation delay [2]. This is due to the linear increase in both the interconnect resistance and capacitance with increase of interconnect length. In the same way in deep submicron technologies also the propagation delay increases with increase in the parasitic and interconnects length.

Frequency of operation in the global interconnects is characterized by capacitive, resistive, and inductive properties which have more effect on the circuit performance [2]. In this paper, an attempt is to study the effects of these parasitic on circuit design parameters such as power, delay, and energy by considering different interconnect structures such as single interconnect and coupled interconnects for copper wire with simple CMOS driver and load. Different technologies along with different lengths of interconnects have been considered and calculated the propagation delay, power, and energy. It has been reported that interconnects in any VLSI system account for more than 60% of signal delay [3, 4]. The paper has been prepared in the following way.

Section 2 explains the types of interconnects. Section 3 describes the interconnect models and parameters. Simulation results have been presented and discussed in Sect. 4. The conclusions have been presented in Sect. 5. This brief is organized as follows. Section 2 describes the VCO types. Section 3 describes the proposed ring VCO design. The simulation results are given in Sect. 4 and the conclusion is given in Sect. 5.

2 Interconnect Types

Interconnect or wiring is used in any system or circuit to propagate the clock and other signals which give data, power, or ground to all the circuits in a system. This interconnect is classified based on its length, namely (i) local, (ii) semi global, and (iii) global [5, 6]. Local interconnect offers less parasitic due to the smaller size, does not travel very long distances, and cover smaller distance only in a chip. Semi global interconnect gives parasitic because of wider and taller than local interconnects. This interconnect provides the interconnection between substantial modules and I/O circuitry. Global interconnects have more parasitic because of larger size than others [7, 8]. These are used to provide clock, power, and long distance communication between functional blocks. These occupy the top layers in a chip. These interconnect parasitic introduce noise sources, increase the propagation delay and power dissipation, and thereby increase the power delay product, which have more effect on circuit performance and reliability. There are different simulation interconnect models which have been considered over the past several decades to calculate these parasitic accurately. Single interconnect is used for

circuit-level estimation and parallel interconnect structures are used for bus structures [9–11]. In this paper both structures are have been considered for simulation and analysis using spice tool.

3 Interconnect Model

To study the behavior of on-chip interconnect as function of its parameters, electrical models are required. An interconnect can be modeled as R, RC, LC, RLC, or RLGC networks. Generally, signal and clock interconnects are used to model as RC or RLC. These can be represented either in lumped or distributed model [12].

The interconnect parasitic are generally disbursed along its length. They are not lumped into a solitary position. But for fast observation of the effects of RLC parameters, it is frequently helpful to lump the distinctive parts into a solitary circuit element. In view of low switching frequency, only resistance and capacitance will be considered and neglecting inductance. For low frequencies, it is possible to lump parasitic parameters into a single RC model by neglecting the L. There are different configurations of RC Interconnect models namely L, T, and pi [2, 6]. Any model may be considered to calculate propagation delay. But in lower technologies, lumped models are not considered because of inaccuracy. For a RC interconnect a distributed RC model is more accurate. Because the simulation results of a distributed model match more accurate than the lumped model, for computer-aided analysis distributed RC interconnect can be approximated by a lumped multistage RC ladder network. An Elmore delay model has been considered in this paper for analysis purpose which is shown in Fig. 1. This model has linear relation between length and delay [12].

Delay of a RC network is given by

$$D = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3 + \cdots + (R_1 + R_2 + \cdots + R_n)C_n. \quad (1)$$

3.1 Interconnect Characteristics

All the wires' resistance, capacitance, and inductance values are extracted from interconnect geometry structures. Resistance relates to current I to voltage V

Fig. 1 Multistage RC ladder network

(carrier flow) [13]. For any current-carrying conductor having some resistance, the resistance is given by Eq. 2:

$$R = \frac{\rho l}{wt}, \tag{2}$$

where ρ represents the resistivity, l is the length, W is the width, and H is the thickness of the interconnect [14]. Generally, capacitance relates charge Q to voltage V (electric energy). Interconnect capacitance consists of two components namely (i) ground capacitance Cg (capacitance between metallic layers and substrate) and (ii) coupling capacitance Cc (capacitance between neighboring interconnects). The coupling capacitance is dominating Cg in the lower technologies because of increasing aspect ratio and decreasing wire spacing. The analytical expressions given in Eqs. 3 and 4 are used to calculate the ground capacitance Cg and coupling capacitance Cc for copper interconnects, which are given below [15]:

$$C_g = \varepsilon \left[\frac{w}{h} + 2.22 \left(\frac{s}{s+0.7h} \right)^{3.19} + 1.17 \left(\frac{s}{s+1.51h} \right)^{0.76} \left(\frac{t}{t+4.53h} \right)^{0.12} \right] \tag{3}$$

$$C_c = \varepsilon \left[1.14 \frac{t}{s} \left(\frac{h}{h+2.06s} \right)^{0.09} + 0.74 \left(\frac{w}{w+1.59s} \right) - 1.16 \left(\frac{w}{w+1.87s} \right)^{0.16} \left(\frac{h}{h+0.98s} \right)^{1.18} \right]. \tag{4}$$

Similarly, inductance relates current I to flux H (magnetic energy), and when compared to other parameters, inductance is difficult to extract from the interconnect structures. In case of high-frequency transmission, global interconnects will higher inductance than local interconnects. In this paper, only RC interconnect model has been considered and analyzed for the delay variations in DSM technology.

4 Simulation Results and Discussion

In this paper an attempt has been made to simulate CMOS inverter as driver, consisting interconnect with equivalent R and C derived from analytical expressions and load C_L and the circuit is shown in Fig. 2.

The simulation has been carried out in three different ways, namely (i) single interconnect with CMOS driver and load as shown in Fig. 2; (ii) two parallel interconnects with coupling capacitance operating in same switching; and (iii) two parallel interconnects with opposite switching. The technologies considered in this simulation as case 1 are 180, 130, and 65 nm. The lengths of copper wires considered for these technologies are 2, 5, and 10 mm.

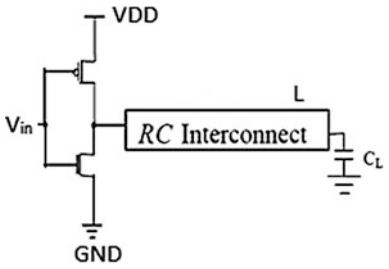


Fig. 2 RC interconnects with CMOS driver and load

In case 2, the technologies considered are as 45, 32, and 22 nm with copper wire lengths of 1, 50, and 100 µm. At lower technologies the lengths of interconnects will be smaller. The simulation results are presented in Tables 1 and 2 and in Figs. 3, 4, 5, and 6. Around 10% variations in delay and PDP values have been observed irrespective of technologies employed with different interconnect lengths, whereas around 5% variation has been observed in delay and PDP values for different interconnect patterns (single, parallel with different switchings) in the same technology with different interconnect lengths. With technology scale down (45, 32, and 22 nm), it is observed that variations in the delay and PDP values are more than 50%. All the simulations were carried out using BSIM4 model files in LT spice simulation tool for above-mentioned technologies.

Table 1 Delay and energy for different technology nodes (180, 130, 65 nm) with variation of interconnect length

Technology (nm)	Interconnect length (mm)	Single interconnect		Coupled interconnect with same switching		Coupled interconnect with opposite switching	
		Delay (ns)	PDP (fJ)	Delay (ns)	PDP (fJ)	Delay (ns)	PDP (fJ)
180	2	8.8	142.7096	7.9	128.114	8.5	137.802
	5	9.26	150.1602	8.83	143.187	9.4	152.458
	10	9.69	157.1137	9.69	157.113	9.2	149.150
130	2	9.69	69.8649	9.69	69.8736	10	72.1
	5	10.69	77.00007	10.9	78.5225	12	86.496
	10	13.8	99.3738	13.7	98.6632	19.5	140.4
65	2	10.73	43.47796	10.7	43.335	11.6	46.9684
	5	20	80.8	20	80.8	22	88.66
	10	27.4	107.9944	30	118.2	31	120.28

Table 2 Delay and energy for different technology nodes (45, 32, 22 nm) with variation of interconnect length

Technology (nm)	Interconnect length (μm)	Single interconnect		Coupled interconnect with same switching		Coupled interconnect with opposite switching	
		Delay (ns)	PDP (fJ)	Delay (ns)	PDP (fJ)	Delay (ns)	PDP (fJ)
45	1	4	39.9716	4	39.971	4	39.968
	50	5.12	50.9462	5.16	51.571	5.1	50.9439
	100	6.48	65.152	6.58	65.760	6.4	63.9552
32	1	3.9	31.5549	3.9	31.554	3.85	31.1465
	50	6.71	54.2398	6.7	54.229	6.7	54.20769
	100	10.4	84.0195	10.4	84.019	10.4	84.0216
22	1	4.475	28.554	4.475	28.550	4.475	28.55498
	50	11.58	73.12	11.6	73.114	11.4	72.1734
	100	18.2	112.507	18.6	110.57	17.6	104.544

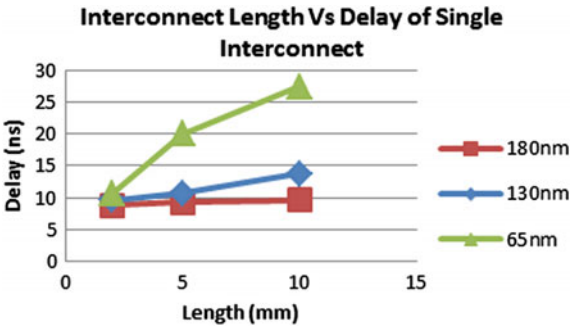


Fig. 3 Variation in delay by change in interconnect length for single interconnect

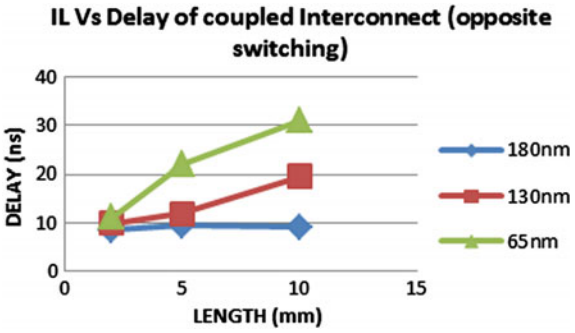


Fig. 4 Variation in delay by change in interconnect length for coupled interconnect when opposite switching

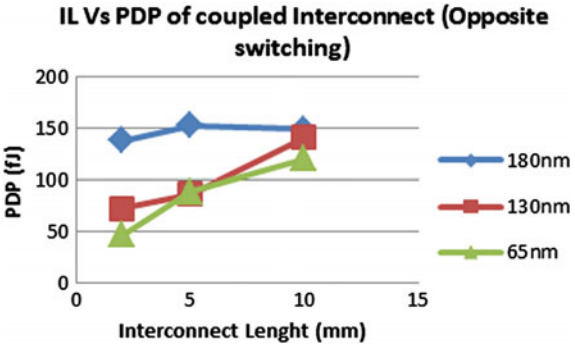


Fig. 5 Variation in PDP by change in interconnect length for coupled interconnect when opposite switching

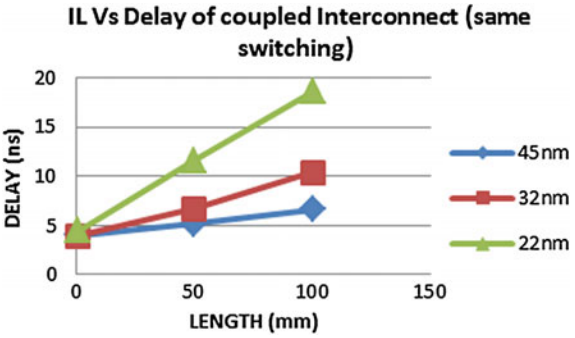


Fig. 6 Variation in delay by change in interconnect length for coupled interconnect when same switching

5 Conclusions

In this paper, an attempt has been made to simulate different copper interconnect structures (single and parallel with different switching events), with a CMOS inverter as driver and load C_L and analyzed the effect of interconnect parasitic on circuit performance metrics such as delay and power delay product. It is observed around 10% variation with different interconnect lengths, 5% variation with different interconnect structures when technology is remains constant in the values of delay and PDP. On the other hand, with variations in technology, around 50% variation has been observed in the values of delay and PDP.

References

1. B. K. Kaushik and S. Sarkar, "Crosstalk Analysis for a CMOS- Gate- Driven Coupled Interconnects" IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 27, no. 6, pp. 1150–1154, Jun. 2008.
2. K. G. Verma, Raghuvir Singh, B. K. Kaushik and Manoj Kumar Majumder "Propagation Delay Deviations due to Process Induced Line Parasitic Variations in Global VLSI

Interconnects" IEEE Conference on Recent Advances in Intelligent Computational Systems (RAICS), 2011.
3. C. Venkataiah, M. Tejaswi "A Comparative Study of Interconnect Circuit Techniques for Energy Efficient on-Chip Interconnects" International Journal of Computer Applications (0975 – 8887) Volume 109 – No. 4, January 2015.
4. International Technology Roadmap for Semiconductors, 2013. [Online] Available: http://public.itrs.net/.
5. S. Borkar, T. Kamik, S. Narendra, J. Tschanz, A. Keshavarzi and V. De, "Parameter variations and impact on circuits and micro architecture," in Proc. Design Automation Conference (DAC), pp. 338–342, 2003.
6. Sandeep Saini "A Novel Approach to Reduce Delay and Power in VLSI Interconnects" M.S. Thesis, Department of Electronics and communication Engineering, Centre for VLSI and Embedded System Technologies, International Institute of Information Technology, Hyderabad, INDIA, May, 2010.
7. Naeemi and J. D. Meindl, "Design and performance modeling for single-walled carbon nanotubes as local, semiglobal, and global interconnects in gigascale integrated systems," IEEE Trans. Electron Devices, vol. 54, no. 1, pp. 26–37, Jan. 2007.
8. Gargi Khanna, Rajeevan Chandel, Ashwani Kumar Chandel and Sankar Sarkar "Analysis of non-ideal effects in coupled VLSI interconnects with active and passive load variations" Microelectronics International, Vol. 26 Iss 1 pp. 3–9(2009).
9. Sandeep Saini, A. Mahesh Kumar, Sreehari Veeramachaneni, M.B. Srinivas, "Alternative approach to Buffer Insertion for Delay and Power eduction in VLSI Interconnects", VLSI design 2010, 3rd to 7th January 2010, Banglore, pages 411–416.
10. Kaushik, B.K., Sarkar, S., Agarwal, R.P. and Joshi, R.C. (2006b), "Cross-talk analysis and repeater insertion in interconnects", Microelectronics International, Vol. 23 No. 3, pp. 55–63.
11. J. M. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits" Prentice Hall, New Delhi, 2nd Edition, 2006.
12. S. M. Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits (Analysis and Design)", 3rd ed. McGraw-Hill 2013.
13. Joshi, A., Soni, G "A comparative analysis of copper and carbon nanotubes based global interconnects." Int. J. Eng. Manag. Sci. (Alied Journals-IJEMS) ISSN-2348–3733, 2(5), (2015).
14. Das, D., Rahaman, H "Analysis of crosstalk in single- and multiwall carbon nanotube interconnects and its impact on gate oxide reliability." IEEE Trans. Nanotechnol. 10(6), 1362, 1370 (2011).
15. V. Ramesh Kumar, A. Alam, B. K. Kaushik, A. Patnaik (2015) "An unconditionally stable FDTD model for crosstalk analysis of VLSI interconnects," IEEE Transaction components, packaging and Manufacturing Technology, 5(12), 1810–1817.

Electroencephalogram-Based OpenBCI Devices for Disabled People

V.R.R. Samson, B. Praveen Kitti, S. Pradeep Kumar, D. Suresh Babu and Ch. Monica

Abstract Each physical development we make is swift in the cerebrum by neural system handling. With the assistance of new hardware and advancements in both cerebrum imaging and cerebral neuroscience, it is conceivable to pursue and record these procedures. In this paper, we have utilized an economical gadget, i.e. OpenBCI Ganglion to control the home appliances or any type of electronic device for physically incapacitated individuals. The EEG signals are caught from client's cerebrum action utilizing OpenBCI Ganglion through "gold cup electrodes (GCE)." The EEG signals that are produced at various level of recurrence, likewise the eye movement, concentration are handled utilizing Arduino Uno which is used to control electronic devices. The BCI helps handicapped to make utilization of the gadgets and applications through their mental exercises. By this, individuals believe that BCI innovation is gift for, who might experience the ill effects of neuromuscular issue.

Keywords Brain–computer interface (BCI) · Electroencephalogram (EEG) · OpenBCI Ganglion · Gold cup electrodes (GCE)

V.R.R. Samson (✉) · B. Praveen Kitti · S. Pradeep Kumar · D. Suresh Babu
Department of ECE, Potti Sriramulu Chalavadi Mallikarjunarao College of Engineering and Technology, Vijayawada, Andhra Pradesh, India
e-mail: richardssamsonvemuri@gmail.com

B. Praveen Kitti
e-mail: praveenkitty17@gmail.com

S. Pradeep Kumar
e-mail: satpradeep@gmail.com

Ch. Monica
Department of ECE, KL University, Vijayawada, Andhra Pradesh, India

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_24

1 Introduction

The hundred billion neurons connected by a hundred thousand billion Synopsys. The human brain is the most complex machine and most mysterious one we know. Incapacitated individuals can operate home appliances or electronic devices using instruments like remote, mouse, voice and console and these information techniques can be efficiently utilized by favoured individuals. Be that as it may, these info techniques are difficult to work by unblessed individuals who are not having control on their muscle action [5]. This issue is totally decreased by utilizing BCI [9].

In non-invasive technique, the cathodes (GCE) are placed on scalp [7]. GCE can read the electrical action and can be measured over a brief timeframe with the help of OpenBCI Ganglion, where the neurons are let go. This EEG voltage approximately starts from 1 μV [1]. This may change as indicated by cerebrum exercises of individual. The EEG signals which are produced are characterized into various sorts as indicated by their recurrence run. Delta, theta, alpha, mu and beta wave (low, midrun, high) are the sorts of EEG waves.

1. This paper explains how to control home appliances and electronic devices through the following modules.
2. Brain waves are extracted through the GCE.
3. The extracted signals (from the GCE) are processed by OpenBCI Ganglion.
4. The processed signals are transmitted to the PC using SIMBLEE and are visualized by OpenBCI master software.
5. The EEG signals are given to Arduino, which controls the home appliance devices and electronic devices.

2 Related Work

EEG method has been utilized by a considerable lot of analysts for controlling of various devices like wheelchair, robotic arm, game controllers, animation movies, etc. Kazno Tanaka prepared an algorithm to identify the patterns from EEG signal to control left and right position of wheelchairs [2]. Junichi Miyata proposed an algorithm in light of coordinates for straight and corner movement of wheelchair [3]. Brice Rebasamen built up a wheelchair using P300 BCI for predefined locations [4]. Naisan Yazdani developed a wheelchair which can move left, right, backward and forward using eight electrodes which are kept in the predefined location on the cerebrum, thereby he implemented 3D virtual environment for capturing EEG signals [6] (Fig. 1).

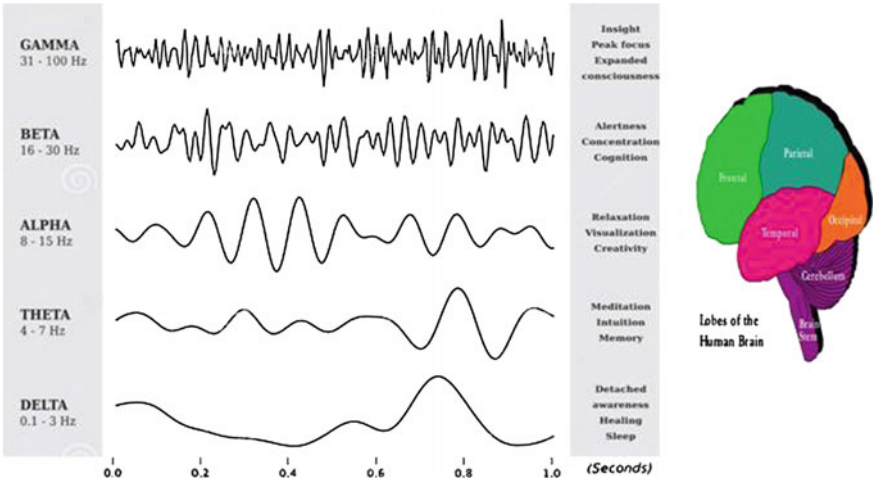


Fig. 1 Human brain waves

3 Proposed Methodology

3.1 System Overview

The proposed EEG-based brain controlled consists of gold cup electrodes, OpenBCI Ganglion, RF module, RS232 serial com, Arduino Uno, etc.

The four electrodes are placed on scalp frontal and parietal positions. As per Fig. 6 they are FP1, FP2, F8 and CP6. The reference electrode and GND electrodes are clipped to ears and by this we can read the brain signals (EEG and EMG) which can help to analyse the electrical behaviour of brain, nerve and muscles. Event of these waves relies on various exercises performed by cerebrum. For this proposed framework Mu musicality is utilize. These Mu waves find in frontal position of mind (Fig. 2).

Generally, EEG signals are characterized by rhythmic activity. Each band has a different level of rhythmic activities. Table 1 gives the information about the different frequency bands and their rhythmic activities. The level analyser values have been determined using the OpenBCI master software of attention and eye blink strength (Fig. 3).

3.1.1 Gold cup electrodes

Electrodes are generally in the shape of metal disc or cup, but here we used gold-coated cup why because to transmit distortion-less EEG and EMG signals. EEG recording can be only achieved when using Ag|AgCl electrodes and a Cl-containing gel (Fig. 4).

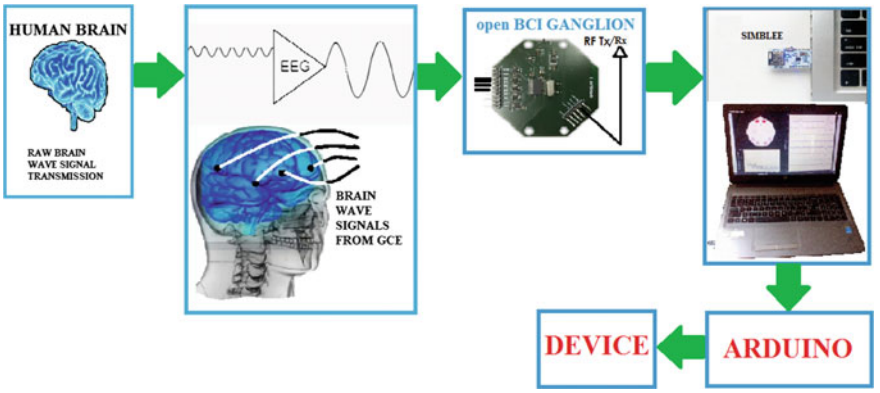


Fig. 2 Proposed design

Table 1 Frequencies generated by different types of activities in the brain

Wave	Frequency (Hz)	Location	Mental state and condition
Delta	0.1–3.9	Everywhere	During sleep, coma
Theta	4–7.9	Temporal and parietal	During emotional stress
Alpha	8–12.9	Occipital and parietal	Reduce amplitude during mental imagery
Mu	9–11	Frontal	Reduce amplitude with intension of movement
Low beta	13–15	Parietal and frontal	Formerly SMR, relaxed yet focused, integrated
Mid-range beta	16–20	Parietal and frontal	Thinking, aware of self and surroundings
High beta	21–30	Parietal and frontal	Alertness, agitation

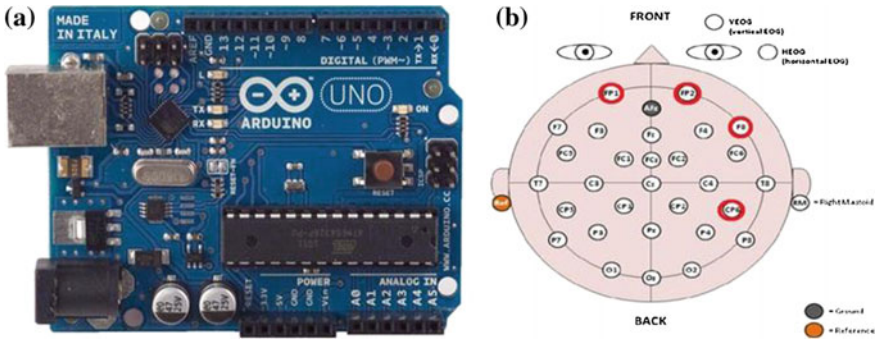


Fig. 3 **a** Arduino board, **b** biosensor placed in the positions of FP1, FP2, F8 on frontal lobe and CP6 on occipital position for EEG recordings

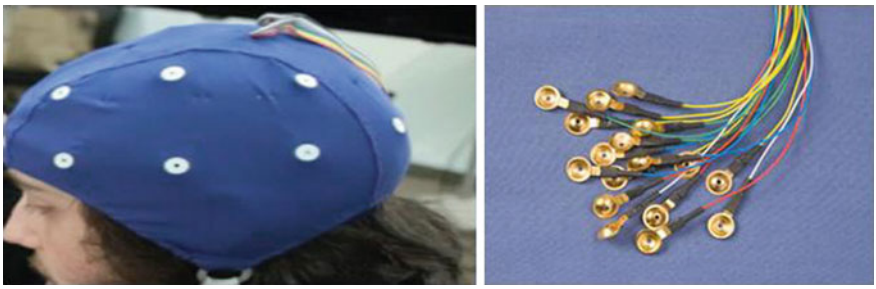


Fig. 4 Gold Cup Electrodes

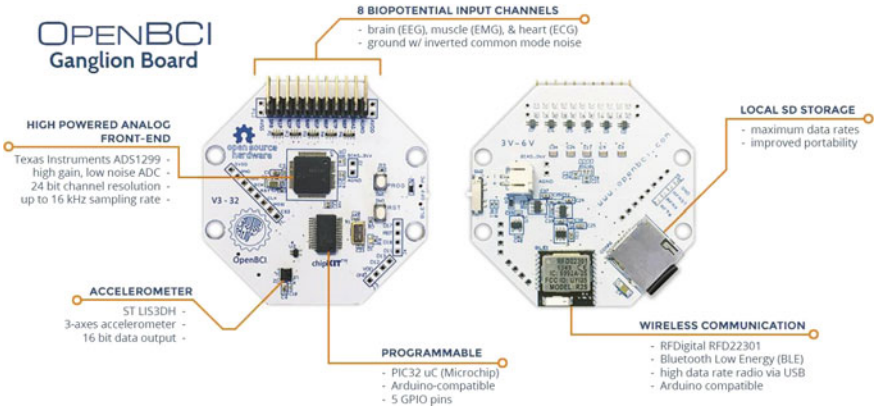


Fig. 5 OpenBCI Ganglion

3.1.2 OpenBCI Ganglion

The OpenBCI Ganglion [8] is a high calibre, moderate bio-detecting gadget. The data sources can be utilized as individual differential contributions for measuring EMG or EEG. The EEG raw signal which is collected by the gold cup electrodes is connected to the OpenBCI Ganglions 4-input channel. Ganglion consists of pre-programmed Texas instrument ADC1299 and the PIC32MX250F128B, which can process the EEG and EMG signals. Ganglion consists of RF module which can transit and receive data to or from any computer or mobile. Here we used Simblee to receive data packets from Ganglion (Fig. 5).

3.1.3 Simblee

The term "Simblee" refers to a revolutionary new technology that allows anyone to create "things" (devices) that can be connected to the Internet of Things (IOT). These devices can be used to monitor and control the world around them. We are utilizing a

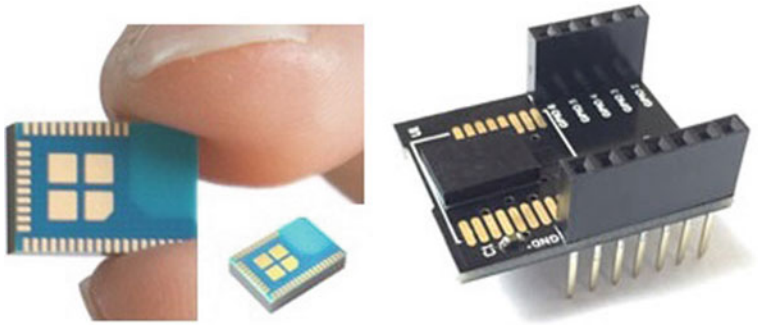


Fig. 6 Simblee RF module for wireless communication

Simblee for our on-board microcontroller and remote association. It is small in size, less expensive and more powerful than the RFDuino. Like RFDuino, Simblee can be programmed using Arduino IDE or sub-line editor.

Features:

1. Interacts with everything without having to download native apps
2. Easily create IOS and Android apps without using hex code or the Android SDK
3. Hardware code and mobile are both on the same page of code
4. Creative phone and table apps are as easy as blinking an LED
5. Create true end-to-end IOT products and accelerate design time (Fig. 6).

Applications:

1. Smart homes, smart buildings and smart cities
2. Medical and patient monitoring
3. Apparel and wearables of all types
4. Smart factories, smart agriculture and smart mining
5. Hero technology for soldiers, fire fighters and police
6. Measure, monitor and log anything
7. Consumer goods such as toys, appliances and gadgets

4 EEG Analysis

Delta waves: The delta waves are produced when the subject is casual or rest or in comma or doing nothing else with the brain. The delta wave frequency that is measured by FFT plot in OpenBCI wave visualizer is 2 Hz. The waves are detected from the four biosensor electrodes (GCE), i.e. at FP1, FP2, F8 and CP6.

Theta waves: The theta waves are produced when the subject is subjected to fear, stress or emotional strain. The theta wave frequency that is measured by FFT plot

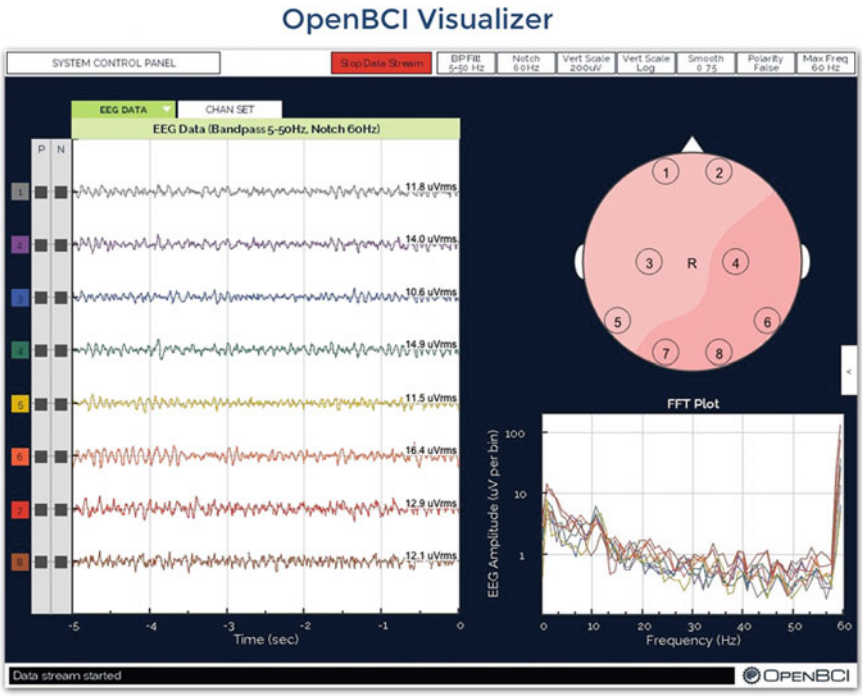


Fig. 7 OpenBCI Master Software

in OpenBCI wave visualizer is 6 Hz. These waves are detected at the parietal and temporal positions, i.e. P2, P3, P4, P7, P8, T7 and T8 positions (Note: In this project these positions are not used. But for the knowledge we analyse the theta waves by placing GCE at the P3 position.)

Mu waves: From Table 1, it is clear that the mu waves are the part of alpha wave frequency range. But mu waves are utilized to read the muscular activity at the frontal position of the brain. The alpha waves are also utilized to read the muscle activity at the occipital and parietal positions of the brain.
When eyes are blink then the mu waves are read from the positions, i.e. FP1, FP2 and F8, as shown in Fig. 8a. When teeth are pressed against each other, alpha waves are read from the CP6 position AS shown in Fig. 9a (Fig. 7).

Beta waves: The beta waves are very quick waves and are produced when the eyes are open or restless mental activities. During the time when eyes are open amplitudes of the waves are going down as shown in Fig. 8b. When subject feels mentally restless, the amplitude of the signals is going to rise. The beta wave frequency that is measured by FFT plot in OpenBCI wave visualizer is 25 Hz.

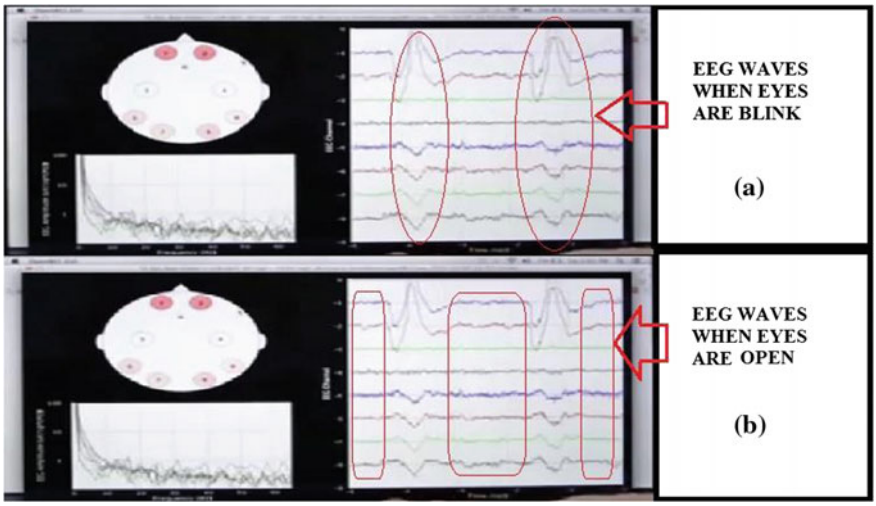


Fig. 8 **a** EEG signals when eyes are blinked. **b** EEG signals when eyes are open

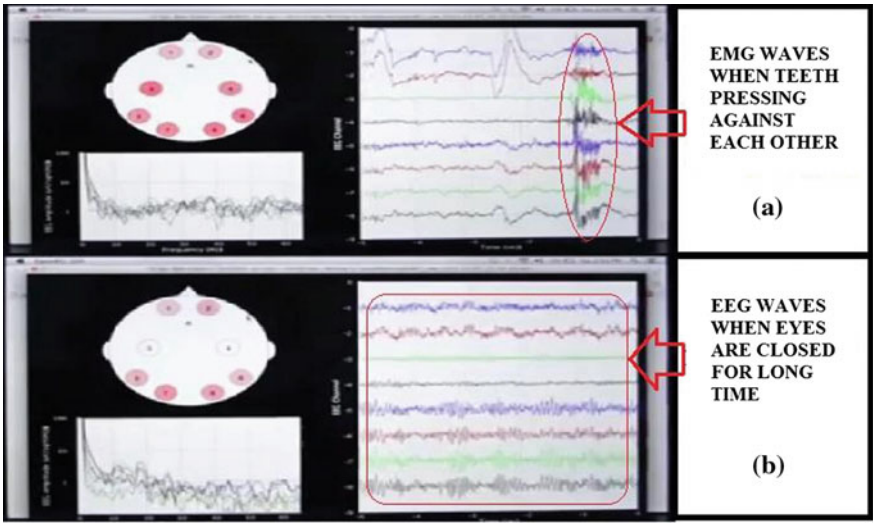


Fig. 9 **a** EEG signals with teeth pressing each other. **b** EEG signals with eyes closed for long time

Alpha waves: The alpha waves are produced when the eyes are closed for a long period (but not sleeping). During this time the amplitudes of the waves are going to rise due to high concentration of brain. The alpha wave frequency that is measured by FFT plot in OpenBCI wave visualizer is 10 Hz. The amplitudes of these waves are higher, when GCE is at CP6 compared to place at FP1,FP2 and F8 as shown in Fig. 9b.

The below are the steps to analyse the EEG data packets through the OpenBCI master software:

1. Download the OpenBCI code examples in libraries from OpenBCI GitHub.
2. Upload the Arduino code from the Arduino brain library.
3. Launch the OpenBCI brain wave visualizer. It has been coded for number of open-source software platform.
4. Open the OpenBCI software and connect the Simblee to the computer.
5. Open the system control panel and select the COM port where the Simblee is placed.
6. Select the start data stream; then EEG waves are appeared in time domain (right side plot), FFT plot (left side plot) as shown in Fig. 7.

5 Conclusion

Previously, brain waves are analysed using only single electrode. In this paper multiple electrodes are used but four electrodes are considered. Depending upon the hardware, EEG signals can be traced at multiple positions of cerebrum. The research and development of BCI with the help of EEG and EMG signals have received a great deal of attention because they can help the people who are having neuromuscular disorder, so they can lead a normal life. Stability of the system depends upon training of the user. It is expected that this paper clarifies a man about the brain waves and how to get them for controlling of electronic gadgets and home appliances.

References

1. I.I. Goncharova, D.J. McFarland, T.M. Vaughan, J.R. Wolpaw EMG contamination of EEG: spectral and topographical characteristics Clinical Neurophysiology 114 (2003) 15801593.
2. Kazuo Tanaka, Kazuyuki Matsunaga, and Hua O. Wang Electroencephalogram-Based Control of an Electric Wheelchair IEEE transactions on robotics, vol. 21, no. 4, August 2005.
3. Junichi Miyata, Yukiko Kaida, and Toshiyuki Murakami, Coordinate-Based Power-Assist Control of Electric Wheelchair for a Caregiver IEEE transactions on industrial electronics, vol. 55, no. 6, June 2008.
4. B. Rebsamen, C. Guan, H. Zhang, C. Wang, C. Teo, M. H. Ang, Jr., and E. Burdet, A brain controlled wheelchair to navigate in familiar Environments IEEE Trans. Neural Syst. Rehabil. Eng., vol. 18, no. 6, pp. 590598, Dec. 2010.
5. J. d. R. Millan, R. Rupp, G. R. Muller-Putz, R. Murray-Smith, C. Giugliemma, M. Tangermann, C. Vidaurre, F. Cincotti, A. Kubler, R. Leeb, C. Neuper, K.-R. Muller, and D. Mattia, "Combining braincomputer interfaces and assistive technologies state-of-the-art and challenges", Frontiers Neurosci., vol. 4, pp. 115, 2010.
6. Naisan Yazdani, Fatemah Khazab, Sean Fitzgibbon, Martin Luerssen Towards a brain-controlled Wheelchair Prototype 2010.
7. Luzheng Bi, Xin-An Fan, Yili Liu, "EEG-Based Brain-Controlled Mobile Robots: A Survey" IEEE transactions on human-machine systems, vol. 43, no. 2, March 2013.

8. Joel murphy, Conor russomanno (2016) Open BCI GANGLION, available at: http://docs.openbci.com/tutorials/01-GettingStarted.
9. Sneha Pushpa S 1, Chandrashekar N S 2, "EEG based Brain-Computer Interface for Controlling Home Appliances" International Journal of Innovative Research in Science, Engineering and Technology Vol. 5, Issue 6, June 2016.

Novel Design of Pulse Trigger Flip-Flop with High Speed and Power Efficiency

Satish Kotta and Rajanbabu Mallavarapu

Abstract In flip-flops (FF) it is considered that about 50% of the total power is consumed by clock distribution or the associated memory. Hence, there is a demand for design of FF with low power rating. Several designs are proposed to achieve this. In this paper, a pulse triggered scheme is adopted in order to reduce the power consumption. This typically helps to reduce the long discharging path. The proposed pulse trigger FF in this chapter is realized using transmission gate-based signal feed through scheme. This will increase the signal feed through capabilities and capable of driving large loads. The post-layout simulation carried out for the layout drawn at CMOS 90 nm and the results were compared with the conventional P-FF design.

Keywords Flip-flops · Pulse-triggered · Feed through

1 Introduction

FFs are widely used in sequential logic design such as finite state machine design, binary counters, shift registers, latches, storage elements, as a delay element in the digital filters and also in the pipelining techniques and many other modules which are meant for various applications. The more efficient flip-flops are needed to design, gated clock buffers which play a major role in the on-chip clock distribution network. These clock distribution networks consume 50% power among the total system power consumption. The performance of FF depends on the performance of chip. Thus, designing of low power and the more efficient flip-flop is a big challenge to meet the performance requirements of the chip [1, 2].

S. Kotta (✉) · R. Mallavarapu
Department of ECE, Lendi Institute of Engineering & Technology,
Jonnada, Vizianagaram, Andhra Pradesh, India
e-mail: satishk.lend@gmail.com

R. Mallavarapu
e-mail: mrajanbabu@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_25

Pulse-Triggered FF (P-FF) is widely used and they are more efficient design than the conventional systems. This is because the pulse-triggered flip-flops were designed using single latch structure so that the design will have low power consumption, fast switching and offer the low complexity of the clock distribution network. A pulse-triggered flip-flop consists of two blocks known as a pulse generator and a latch. The pulse generator produces a sequence of short pulses and the latch is used to store the data. The pulse-triggered Flip-Flop (P-FF) also performs like edge triggered FF if the duration of the pulse is significantly narrow. With this feature, the traditional master–slave flip-flop can be replaced by pulse-triggered flip-flop for low area applications and also possible to achieve high toggle rates. This makes the pulse-triggered flip-flop is more suitable for high-speed applications [3, 4]. P-FFs designs will allow clock borrowing across boundaries and sometimes results in negative set up times [5].

This chapter describes the low-power pulse-triggered flip-flop design the proposed technique employs a feed through scheme. Briefly, the technique involves in direct feeding of input in order to reduce the longer delays. This can be achieved by inserting a pass transistor which will provide additional signal driving. After connecting the PG with the signal feed through scheme the speed and power-delay-product (PDP) of the P-FF will enhance. Designing the balanced performance flip-flop with low power, fast switching for clock distribution network and other switching elements were always a great challenge [6, 7].

2 Existing Design

The pulse-triggered flip-flops can be classified into two types which are known as Implicit and Explicit type. The implicit type of pulse-triggered flip-flops and the pulse generator are designed as an internal part of the element to the latch design such that no explicit pulses were generated to drive the external stages. And in the explicit P-FF, which may need of driving larger loads or may be used clock distribution networks, the pulse generator and the latch are individual. However, the P-FF always struggle from a longer discharging path in the clock distribution network. Due to this long discharging path, it will induce inferior timing characteristics. In contrast, the explicit pulse generation blocks suffer from more power consumption, but it has better performance with the switching speed. In this case, the dynamic power consumption can be reduced by sharing the pulse generator to other groups of the flip-flop in the clock distribution. This also helps to reduce the circuit complexity is effectively reduced as the circuit logic is separated with the pulse generator. So, this paper focuses on the explicit type of pulse-triggered flip-flop.

The existing conventional design is shown in Fig. 1a [8]. Figure 1b shows the layout designed in 90 nm CMOS. It uses NAND-based logic to generate the pulses and semidynamic TSPC latch design. In this design, the data is latched by the logic inverters I_3 and I_4 and the logic inverters I_1 and I_2 will hold the internal node X. The

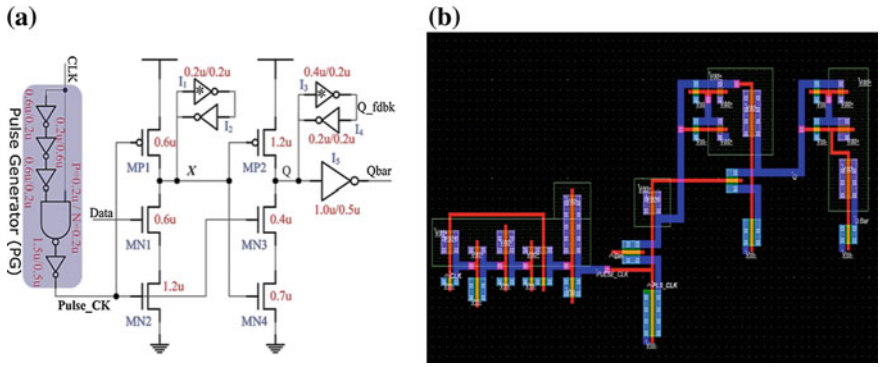


Fig. 1 **a** CMOS circuit diagram of ep-DCO, **b** CMOS layout for ep-DCO drawn at 90 nm

duration of the pulse is derived by the overall delay of three inverters in the pulse generator.

The basic problem with the design is the associated huge power dissipation involved with the switching process. Due to this, various designs have been proposed like Conditional pre-charge, conditional-capture, conditional discharge, and conditional pulse enhancement to reduce the dynamic switching power [9, 10].

Figure 2a shows the conditional discharge (CD)-based pulse-triggered FF [11]. The CMOS layout was drawn for the CD based CMOS 90 nm technology is shown in Fig. 2b. This design has an extra nMOS transistor MN3 is controlled by the output signal Q_fdbk. Due to this, no discharge occurs if the input data remains "1." And the pull-up transistor and a logic inverter were employed at the internal node X for the charging keeper logic design. The static conditional discharge based pulse-triggered flip-flop (SCDFF) is another approach for the design of pulse-triggered flip-flop design. This approach is different from the conventional CD based P-FF design. In this SCDFF, the discharging node X is excluded from the periodical discharge. But, it suffers from the long data-to-Q (D-to-Q) delay when compared with the CDFF. The CDFF and SCDFF both designs are having the problem of worst case delay due to the discharging path consisting of three stacked nMOS transistors indicated from MN1 to MN3. This delay path can be overcome using a powerful pull-down circuit. But the pull-down circuitry occupies additional layout area and power consumption.

Figure 3a represents the hybrid latch flip-flop (HLFF) which does not have any charge keeper circuit at internal node X but uses a static latch only in its design. The MP1, which is a weakly coupled transistor, helps to sustain the signal level at the internal discharge node X when Q value is logic 0. This helps to reduce the complexity in the circuit. But, the design has two limitations. One is associated with node X, due it is not predischarge, so the delay to reach from 0 to 1 is huge. Another limitation is that the node X will remain floating in few cases and the logic value may deviate to create additional DC power [10].

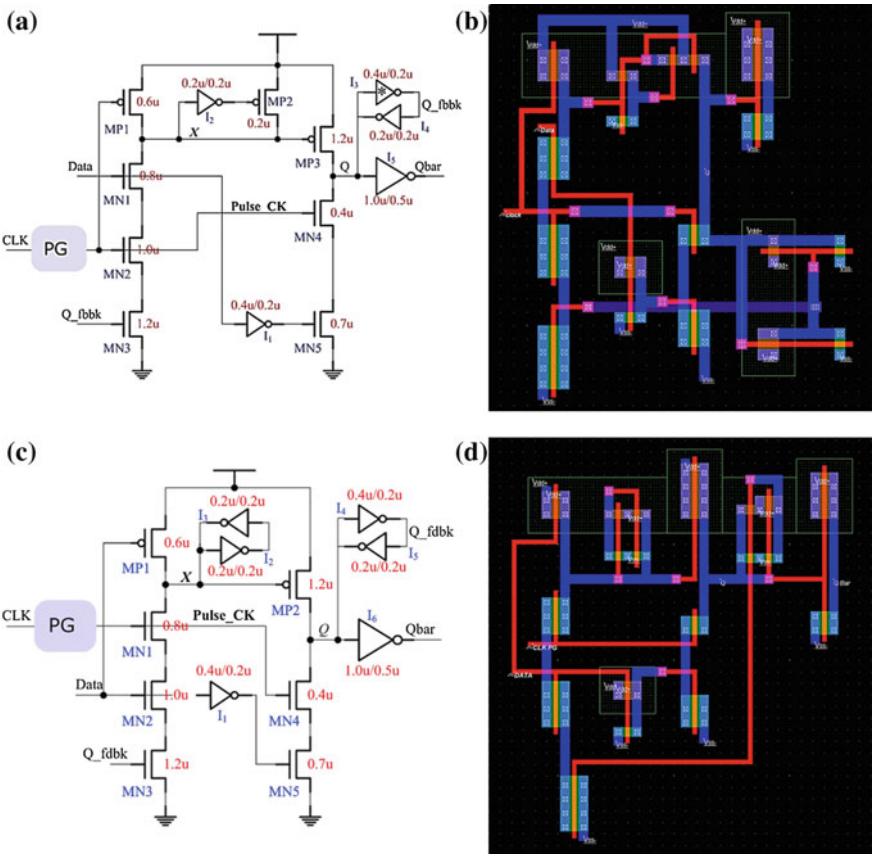


Fig. 2 **a** CMOS circuit diagram of CDFF, **b** CMOS layout for CDFF at 90 nm **c** CMOS circuit diagram of static-CDFF **d** CMOS layout for static-CDFF at 90 nm

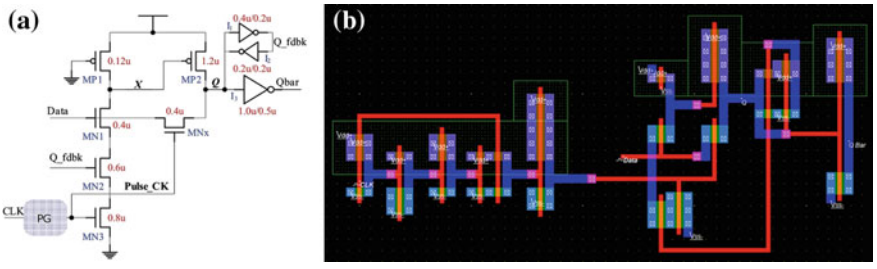


Fig. 3 **a** Schematic of P-FF with signal feed through scheme, **b** CMOS Layout at 90 nm for P-FF with signal feed through scheme

Different designs of p-FF are mentioned above. Since all of them are suffering from the worst case timing for data transitions from logic 0 to 1. It has been a major challenge to overcome this delay [12]. To avoid this superfluous switching, a static latch, and a conditional discharge unit was employed in the signal feed through scheme at the node X. It has been clearly observed that the pulse-triggered signal feed through scheme is having major three differences with the other conventional TSPC latches. The first one is, the first stage of the TSPC latch consisting of a weak pull-up pMOS transistor (MP1). This reduces the load capacitance of internal node X [13–15]. The second one is the pass transistor MN_x which is controlled by the pulse clock. With this, the logic level at this node can be easily pulled up and able to reduce the transition delay. And the last one is, the second stage pull-down network is excluded from the design. This will improve the efficiency of the discharging path at the internal node X. The pulse-triggered flip-flop with signal feed through scheme is shown in Fig. 3a and its CMOS layout is drawn at 90 nm technology shown in Fig. 3b.

The role of MN_x is a twofolded scheme. It provides additional driving to node Q for the data transitions logic 0–1 and vice versa. This design scheme employs the signal feed through scheme consists of a charge keeper which consisting of two logic inverters, pull-down network, and control inverter.

3 Proposed Pulse Triggering Scheme

The conventional pulse-triggered flip-flop with signal feed through scheme [12] shows the most balanced delay behavior when compared with other pulse-triggering schemes. The proposed design consists of a transmission gate at node X. The transmission gate is controlled by the pulse-triggered clock. This will improve the signal feed through of the data Fig. 4.

The working principle of the proposed design is as follows. If there is no transition occurs at the input and if the clock pulse arrives, then no change will occur at node Q. During this, the static ON current passes through the transmission gate to the in-out stage of the FF which will drive the output of the FF. Meantime,

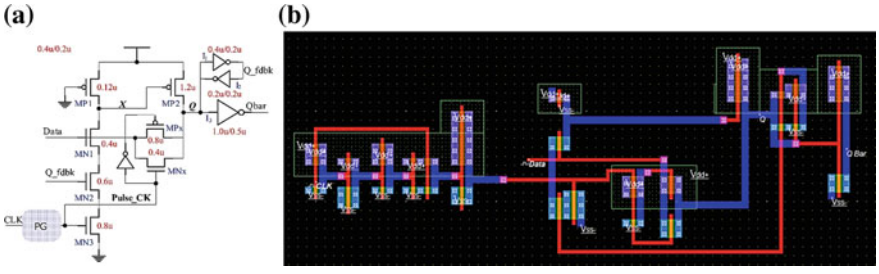


Fig. 4 **a** Proposed pulse triggered FF with signal feed through scheme, **b** CMOS Layout at 90 nm for proposed P-FF with signal feed through scheme

the in-out data and the Q_fdbk will remain complemented to each other and the node X along with the pull-down path will remain in off mode. This cause no internal signal transitions occurs in any node inside the FF. If the data switched from "0" to "1", the MP2 transistor will be turned ON following the node X discharge. This will pull-up node Q to the logic "1". By employing the Transmission gate in the signal feed through scheme the additional signal drive will be obtained from the input source. The input source loading will not be affected as the transmission gate will be turned ON only for the short duration.

4 Simulation Results

The proposed pulse-triggered FF using Transmission gate design is analyzed and compared with the existing designs. The compared designs include the four various types such as Pulse-triggered FF such as ep-DCO, CDFF, SCDFF, MHLFF, P-FF

Table 1 Parameter comparisons of various P-FF schemes

FF designs	ep-DCO	CDFF	SCDFF	MHLFF	P-FF SF	Proposed
No. of transistors	28	30	31	19	24	27
Layout area (μm^2)	77.86	89.70	89.16	78.94	69.13	71.8
Setup time (ps)	−83.8	−88.2	−44.8	1.5	−85.7	−45.3
Hold time (ps)	110	123.5	122.6	173.8	109.1	38.1
Minimum D-Q delay	118.9	129.5	140	173.8	109.1	80.1

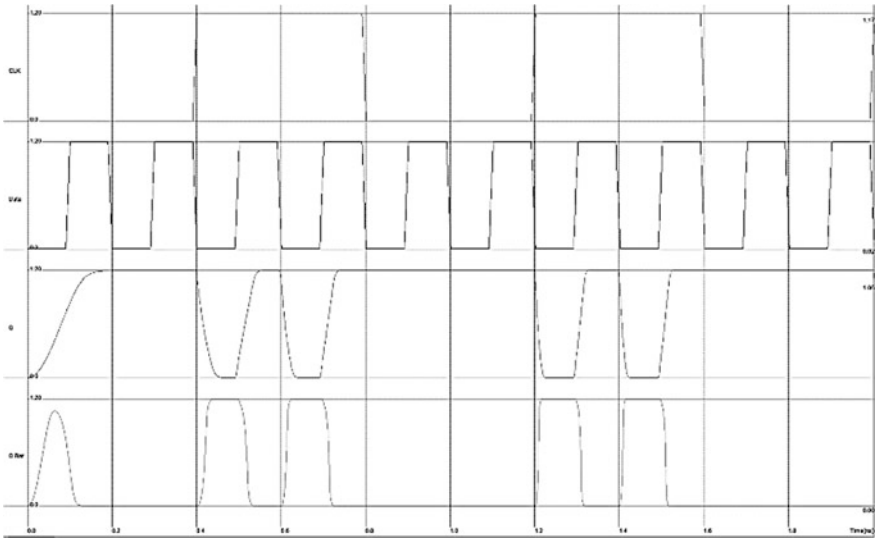


Fig. 5 Simulation result of the proposed transmission gate-based P-FF design

with signal feed through scheme and the proposed Transmission gate-based P-FF signal feed through scheme. The comparisons were shown in Table 1. The 90 nm CMOS technology is used. It is evident that the pulse width determines the exactness of data. It also determines the power consumption [6, 7]. For this reason, the associated transistors are chosen to be sized for 120 ps in pulse duration Fig. 5.

5 Conclusion

The design of the P-FF is successfully performed using efficient modified TSPC latch with the transmission gate design with a mixed design style and a pseudo-nMOS logic. The objective of ensuring better signal feed through between the typical input and interval node is achieved. As a result, it is possible to witness diminished transmission time. This also in term enhanced the performance by enhancing speed and limiting power. The design was successfully achieved and the simulation results were shown that the proposed transmission gate-based signal feed through the scheme is more efficient than the existed TSPC designs.

References

1. Kawaguchi. H., Sakurai. T.: A reduced clock-swing flip-flop (RCSFF) for 63% power reduction. *IEEE Journal of Solid-State Circuit,* vol. 33, no. 5, pp. 807–811, (May, 1998)
2. Chen. K.: A 77% energy saving 22-transistor single phase clocking D-Flip flop with adoptive-coupling configuration in 40-nm CMOS. in *IEEE International Solid State Circuits Conference*, (Nov, 2011)
3. Consoli. E., Alioto. M., Palumbo. G., Rabaey. J.: Conditional Push-pull pulsed latch with 726 flops energy delay product in 65 nm CMOS. in *IEEE International Solid State Circuits Conference*, (Feb, 2012)
4. Sadrossadat. S., Mostafa., H., Anis. M.: Statistical design framework of sub-micron flip-flop circuits considering die-to-die and within -die variations. *IEEE Transactions on Semiconductor Manufacturing,* vol. 24, no. 2, pp. 69–79, (Feb, 2011)
5. Alioto. M., Consoli. E., Palumbo. G.: General strategies to design nanometer flip-flops in the energy-delay space. *IEEE Transactions on Circuits and Systems,* vol. 57, no. 7, pp. 1583–1597, (Jul, 2010)
6. Alioto. M., Consoli. E., Palumbo. G.: Analysis and comparison in the energy-delay-area domain of nanometer CMOS flip-flops: PART-II—results and Fig..s of merit. *IEEE Transactions on Very Large Scale Integration Systems,* vol. 19, no. 5, pp. 737–750, (May, 2011)
7. Sadrossadat. S., Mostafa. H., Anis. M.: Statistical design framework of sub-micron lip-flop circuits considering die-to-die and within-die variations. *IEEE Transactions on Semi-conductor manufacturing,* vol. 24, no. 2, pp. 69–79, (Feb, 2011)
8. B. Kong, S. KIm and Y. Jun, "Conditional-capture flip-flop for statistical power reduction. *IEEE journal for Solid State Circuits,* vol. 36, no. 8, pp. 1263–1271, (Aug, 2001)
9. H. Y-T., L. j-f., S. M.H.: Low power pulse triggered flip-flop design with conditional pulse enhancement scheme. *IEEE Transactions on Very Large Scale Integration (VLSI) systems,* vol. 20, no. 2, pp. 361–366, (Feb, 2012)

10. Zhao. P., Darwish. T., Bayoumi, M.: High-performance and low. *IEEE Transactions on Very Large Scale Integration (VLSI) systems,* vol. 12, no. 5, pp. 477–484, (May, 2004)
11. P. M.W., G. W-L., Y. K-S.: A low-power static dual edge triggered flip-flop using an output-controlled discharge configuration. in *IEEE International symposium on Circuits and Systems*, (May, 2005)
12. Jin-Fa. L.: Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 22, no. 1, pp. 181–185, (Jan, 2014)
13. Zhao. P., McNeely. J., Venigalla. S., Kumar. GP. P., Bayoum. M., Wang. N., Downey. L.: Clocked-pseudo-NMOS flip-flops for level conversion in dual supply systems. *IEEE Transactions on Very Large Scale Integration (VLSI) systems,* vol. 17, no. 9, pp. 1196–1202, (Sep, 2009)
14. Rasouli. S. H., Khademzadeh. A., Afzali-kusha. A., Nourani. M.: Low power single- and double-edge-triggered flip-flops for high speed application," in *IEEE Circuits Devices & Systems*, (Apr, 2005)
15. Mahmoodi. H., Tirumalashetty. V., Cooke. M., Roy. K.: Ultra low power clocking scheme using energy recovery and clock gating. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 17, no. 1, pp. 33–44, (Jan, 2009)

Gate Diffusion Input-Based Design for Carry Select Adder

Siva Rongali and Rajanbabu Mallavarapu

Abstract The regular carry select adder (CSLA) is designed using RCA-RCA configuration. It uses two individual RCA with different anticipated carry input values ($C_{in} = 0$ and $C_{in} = 1$). After the calculation, the appropriate sum and carry-out will be selected using a multiplexer depending on the logic state of the carry input. In recent times, several architectures in CSLA adder were proposed. Boolean to Excess-1 converter (BEC) was one among them. This BEC-1 converter will be used instead of RCA with $C_{in} = 1$, such that the CPD can be reduced. The alternate approach was using common Boolean logic (CBL). This method also succeeded in reducing the CPD. Apart from these two architectures of CSLA, the proposed architecture in this chapter has shown a significant amount of results on reducing the CPD of the binary adder. In this chapter, the proposed CSLA adder employs single stage scheme such that the logic burden can be reduced. In this single stage architecture, the partial sum will be generated for the given input data, later the carry selection will perform according to the input carry then followed by the full sum generation. Thus, it has a single stage carry selection process. In this chapter, the sum generator uses A GDI-based XOR gate. Full Adder (FA) which was used to perform the sum generation was replaced by GDI Full Adder which is an efficient low power adder. Thus, the proposed adder will adopt high speed, low area, and power efficient adder. The comparison results were also discussed in the results section.

Keywords CSLA · RCA · CPD · GDI

S. Rongali (✉) · R. Mallavarapu
Department of ECE, Lendi Institute of Engineering & Technology,
Jonnada, Vizianagaram 535005, Andhra Pradesh, India
e-mail: sivar.lendi@gmail.com

R. Mallavarapu
e-mail: mrajanbabu@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_26

1 Introduction

Fast binary adders with high speed, low power, and area-efficient designs are in great demand for the IC design industries. Because these efficient binary adders involve not only in performing binary addition but also play a vital role in other important elements inside the digital circuits. To achieve the high-performance goal at the system level, it is a must to design these binary adders at optimal cost. Consider the basic ripple carry adder (RCA) which has less circuit complexity and easy to design and implement. But, it has the major drawback of large carry propagation delay (CPD). There are several designs proposed to reduce the CPD such that fast addition can be achieved. The architectures which were proposed to reduce the CPD were known as the fast binary adders. Carry select adder, carry look-ahead adder, carry save adder, parallel prefix adders, etc., are classified as the fast adders. The addition is the most widely used arithmetic operation that widely used in digital computation performed in all digital signal processing applications, digital multiplications, signal transformations, and various other applications as well. The performance of the adders has a great impact on the performance, efficiency of the digital system. There is a great demand for the less delay time, low area adders for the digital signal processing applications (DSP), digital communication, and filtering, transformation, mobile computing, and other applications where digital arithmetic performance is limited by design constraints.

The disadvantage of the ripple carry adder is the addition will start for every bit after the arrival of its carry input. The key idea behind the carry select adder is using two RCA in which, one connected to a constant 0 carry-in, while the other is connected to a constant-1 carry-in. The CSLA adder will choose the actual output from the precomputed values using the multiplexer. The precomputed values obtained by performing the addition for the two alternative values of $C_{in} = 0$ and $C_{in} = 1$. The multiplexer will choose the appropriate precomputed values once the External C_{in} arrive at the select line. With this technique, the time required to take the carry information and then performing addition time both were reduced. This increases the speed of the CSLA adder. But on the other hand, it fails to conserve the area, due to which it is often considered as not area efficient. Hence, designing area efficient CSLA is a challenging task for the VLSI engineers. In this paper, such an attempt to modify the conventional CSLA is performed to achieve the above challenges.

This paper is organized as follows; Sects. 2 and 3 explains the Conventional and modified CSLA and detail structure of BEC, respectively. Section 4 describes the proposed CBL and comparisons of area, power and delay results are analyzed and it is followed by conclusion in Sect. 5.

2 Conventional SQRT-CSLA Architecture

The ripple carry adder is very easy to implement but if offer large CPD which reduces the speed of the adder. As an alternate to this approach, as an alternative to this approach several techniques to limit the CPD are proposed. On the line, the carry save adder, parallel prefix architectures also grabbed the major attention by reducing the CPD.

New architecture which is referred as square root CSLA (SQRT-CSLA) is proposed keeping in view of the above limitation. The SQRT-CSLA typically has an inherent feature to handle large bandwidth address with minimum delay [1–5]. The circuit diagram of this conventional SQRT-CSLA is as shown in Fig. 1.

3 Logical Analysis

The CSLA adder consisting of two elements: (1) The *Sum* and *Carry* generator element (SCG) and (2) the *sum* and *carry* selection unit [6–8]. The critical path of the SCG unit is large as it occupies more number of design elements in the CSLA design.

The CSLA proposed in [6] is based on logic formulation. The logic formulation structure is shown in Fig. 2a–e, the formulation for the shown structure is shown below. Equations (1)–(5),

$$S_0(i) = A(i) \wedge B(i), \quad C_0(i) = A(i) \cdot B(i) \tag{1}$$

$$c_1^0(i) = c_1^0(i-1) \cdot S_0(i) + C_0(i) \; for \; (c_1^0(0) = 0) \tag{2}$$

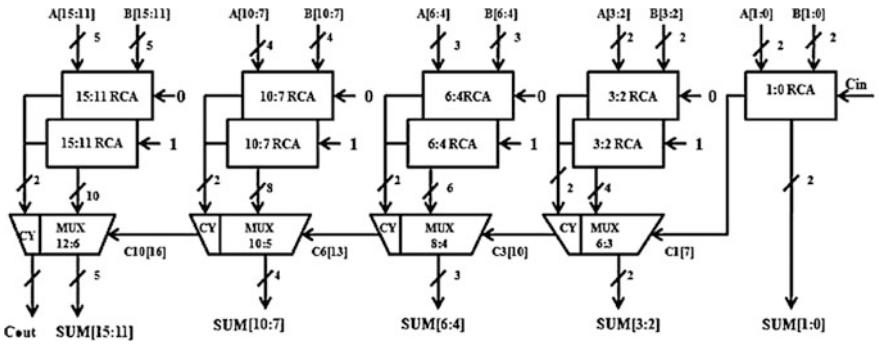


Fig. 1 Conventional SQRT-CSLA adder

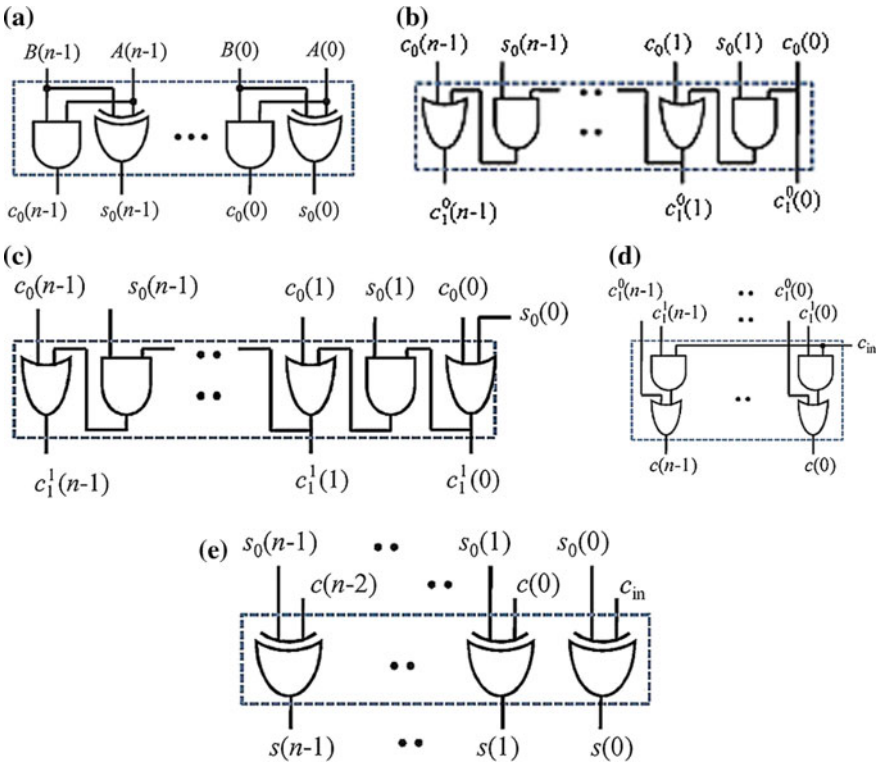


Fig. 2 Logic formulation structure

$$c_1^1(i) = c_1^1(i-1) \cdot S_0(i) + C_0(i) \; for \; (c_1^1(0) = 1) \tag{3}$$

$$C(i) = c_1^0(i) \quad \text{if } (C_{in} = 0) \tag{4}$$

$$C(i) = c_1^1(i) \quad \text{if } (C_{in} = 1) \tag{5}$$

The logical circuit of the ripple carry adder consists of the following blocks: Half sum generator (HSG) unit, full sum generator (FSG) unit, carry generator (CG) unit, and carry selector (CS) unit. Further, the CG unit has carry generators for two possibilities of the carry input. Such as, CG_0 for input carry '0' and CG_1 for input carry '1'. The inputs of the HSG are the input operands of the adder (A and B) and produce the half sum and half carry information without considering the external carry input. The CG_0 and CG_1 will obtain S_0 and C_0 form the HSG unit and generate two n-bit full-carry words c_1^0 and c_1^1 for the input carry '0' and '1', respectively.

The carry selector block is controlled by the C_{in}, using this C_{in} the final carry will be selected from the two carry words produced by the CG unit. If $C_{in} = 0$ then CS block selects c_1^0 otherwise it will select c_1^1. The CS unit is consisting of an n-bit

2-to-1 MUX. This helps to optimize the CS block. The CS block is described in Fig. 2e which consists of *n* AND-OR gates. The CS block produces the final carry output.

4 Sum Generator Using XOR Gate Using Gate Diffusion Input (GDI) Technique

The 2-input XOR gate used for sum calculations utilize 18 Transistors, where as it requires only eight transistors using GDI Technique. This reduces the area of the one XOR gate by 60%. The CSLA architecture has one stage of HSG and FSG. The key component of HSG and FSG are XOR gates. In this chapter, the HSG and FSG were implemented using XOR gates developed using Gate Diffusion Input (GDI)

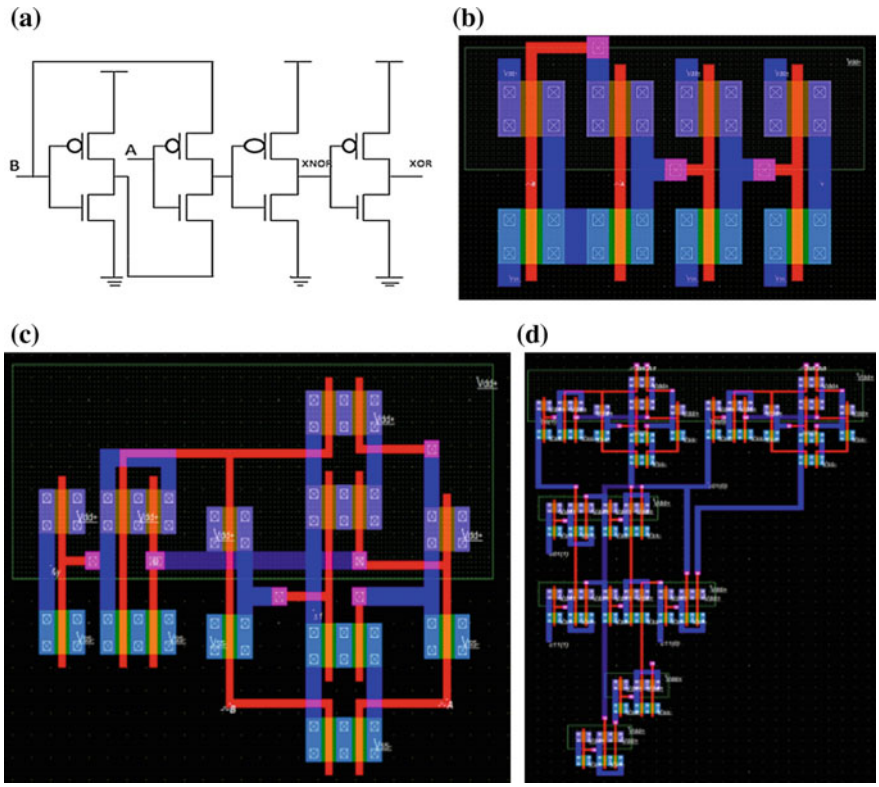


Fig. 3 **a** 2-input XOR gate using GDI, **b** CMOS layout diagram of 2-input XOR-GDI at 90 nm technology **c** CMOS layout for Carry Generator (CG) at 90 nm **d** CMOS Layout for 2-bit CSLA adder with proposed XOR-GDI

Table 1 Comparison between proposed and existing CSLA Architectures

Design	Area	Delay		ADP (μm^2 μs)
		S	Cout	
Conv	1438.12	3.45	3.35	4.96
CSLA [3]	1282.45	4.08	4.08	5.23
CSLA [4]	906.56	3.78	3.78	3.42
CSLA [5]	1654.65	7.3	7.3	12.08
CSLA [6]	951.09	3.87	3.42	3.68
Proposed	683.5	3.41	3.25	3.21

The gate diffusion input (GDI) circuits are much smaller than the CMOS circuit elements, 30% faster and consume 85% less power. The combination of CMOS-GDI circuit provides the optimal solution. The GDI circuit for Half Adder is shown in Fig. 3a. The CMOS layout for the XOR gate-GDI designed at 90 nm technology shown in Fig. 3b.

The performance comparison between various CSLA architectures and proposed CSLA architecture with the GDI-XOR gate is shown in Table 1.

5 Conclusion

In this chapter, the logic operations in the conventional CSLA, CSLA-BEC, CSLA-CBL, and logic formulation of CSLA architecture. Then the XOR gate was replaced with GDI in HSG and FSG and its performance was compared. The GDI technique utilizes very less number of transistors, consumes very less power than the CMOS logic gates. Using this GDI-based XOR gate, the CSLA adder will now adopt its features and its performance will be upscaled. Thus, makes it optimal for high speed, low power, and low area requirement.

References

1. Kore. S. D., K.B.V.S.: Modified Carry Select Adder Using Binary Adder as a BEC-1," *European Journal of Scientific Research,* vol. 103, no. 1, pp. 156–164, (2013).
2. B. O.J., "Carry-Select Adder," *IRE Transactions on Electronics * Computers,* pp. 340–344, (1962).
3. He. Y., Chang. C. H., Gu. J.: n area-efficient 64-bit square root carry select adder for low power application," in *IEEE international symposium on Circuits and Systems*, (2005).
4. M. S., S. V.: An Efficient SQRT Architecture of Carry Select Adder Design by Common Boolean Logic. (2013).
5. Parhami. B.: Computer Arithmetic: Algorithms and Hardware Designs, 2 ed., New York, NY, USA: OXFORD UNIVERSITY PRESS, (2010).
6. Basant Kumar Mohanty, Sujit Kumar Patel.: Area-Delay-Power Efficient Carry-Select Adder. *IEEE Transactions on Circuits and Systems -II Express Briefs,* vol. 61, no. 6, pp. 418–422, (June, 2014).

7. Rohit Tripati, Paresh Rawat.: A Efficient Low-Power High Speed Digital Circuit by using 1-bit GDI Full Adder Circuit. *International Journal of Engineering Trends and Technology (IJETT),* vol. 36, no. 3, pp. 155–160, (June, 2016).
8. I-chyn. W., Cheng-chen. H., Yi-Sheng. L., Chien Chang. P.: An Area-Efficient Carry Select Adder Design by Sharing Common Boolean Logic Term. in *IEEE International symposium Circuits Systems*, (2005).

Wavelet-Based Protection Scheme for SVC Compensated Multi-terminal Transmission System with Hybrid Generation

Y. Manju Sree, G. Ravi Kumar and R. Kameswara Rao

Abstract The majority of transmission system development is easily affected to several temporary and permanent faults due to transients and short circuits. These faults can destroy the transmission network internally and can lead to power system instability. It is necessary to clear these faults within the permissible operating time and have high degree of reliability and security for protective systems. This paper deals about wavelet-based protection scheme for SVC compensated multi-terminal transmission system in presence of hybrid generation. Fault indices are determined by detailed coefficients of current signals at all three terminals using Bior 1.5 mother wavelet. To discriminate the fault on the transmission system, fault indices are compared with a threshold value. The proposed algorithm is found to be reliable, accurate and fast as compared to conventional methods for different types of faults on SVC compensated multi-terminal transmission system with hybrid generation at various terminal locations and fault inception angles.

Keywords Multi-terminal transmission lines · Hybrid generation · Wavelet analysis · SVC

1 Introduction

There is a significant need to prevent damage of highly sophisticated and widely used equipment from electrical failures, fault, and discontinuities. The protective scheme to fulfill the above need should ensure high degree of continuity with

Y. Manju Sree (✉) · G. Ravi Kumar
Kakatiya Institute of Technology and Science, Warangal, India
e-mail: manju547sree@gmail.com

G. Ravi Kumar
e-mail: goli.ravikumar@yahoo.com

R. Kameswara Rao
Raghu Engineering College, Visakhapatnam, India
e-mail: rkameswara@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_27

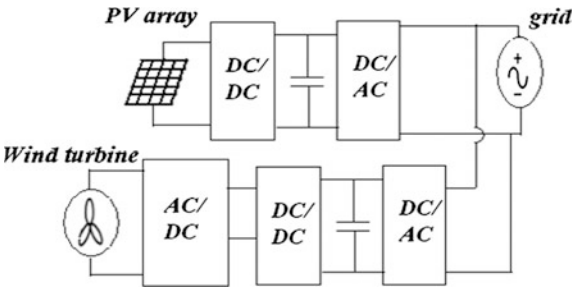


Fig. 1 Block diagram of hybrid PV and wind energy system

electrical supply. The technique lies in designing a system that monitors the power systems for its failures at times. The design should intuitively respond to the fault characteristics, which help in identifying the same. Protection is needed not only against short circuits but also against any other abnormal conditions which may arise on a power system. Most of the faults on transmission and distribution lines are caused by overvoltage resulting in short circuits [1]. Three terminal and multi-terminal line projects generally have protection complexities and lead to compromises in reliability. In the recent past, there is a huge advancements with used in utilizing renewable energy sources. The hybrid energy system [2] is capable of providing electricity to remotely located areas. Wind turbines and solar panels are some to exemplify such systems. The wind turbines operate only during the winter season where there is a possibility of huge wind. Similarly, the solar panel is functional during summer when there is abundant sunlight. If any fault occur on the transmission line due to bad weather or any other condition, hybrid system are present to continue the supply [3]. The proposed system configuration and control scheme provides integration of PV source and wind energy source as illustrated in Fig. 1. The proposed research work is carried out to protection of multi-terminal transmission system with SVC in presence of hybrid system which is the combination of wind, PV generation using wavelet-based multi-resolution analysis. The system with hybrid generation [4] and three terminal transmission systems are tested with various combinations of faults on the phases with respect to the distance.

2 Multi-terminal Transmission Line Protection Scheme

Transmission system typically connects the generation plants to the remotely located region. These are further classified based on their individual voltage levels. This paper describes the most common types of three terminal protection scheme [5] for various types of faults. At a point where permanent fault occurs in the lines it takes huge amount of time to detect the fault, meanwhile the reliability of the system diminishes. There is a financial advantage in the development of three terminal transmission systems since it stays away from the cost of all or a segment of a substation and normally decreases the transmission line losses.

The technique of using a differential current relay (DCR) circuits is often considered as the simplest way of detecting faults and protecting the electrical system. The sensed imbalance forces a signal to trip, at the terminals with respect to its preset value and give the trip signal received at the terminals will immediately activate the local breaker. In such protection scheme is proposed which is capable of covering the entire length of multi-terminal transmission line protection (MTL) [6].

3 Wavelet Analysis

Wavelet analysis is a versatile tool which is extensively signal processing applications [7]. In this work such wavelet analysis is employed to detect as well as to discriminate the faults in transmission lines. The wavelet transform is one of the method which involves in sensing the electromagnetic transients which are possibly generated during the power system failures at the time of switching instants. The technique is similar to application of Fourier transform for fault analysis. However, wavelet-based application is more reliable and is capable of analyzing nonperiodic signals.

Wavelet transform allows the decomposition of a signal into different levels of resolution. The signal characterization is better and more reliable, thus discrimination can be obtained by using wavelet transform. It is a unique method for

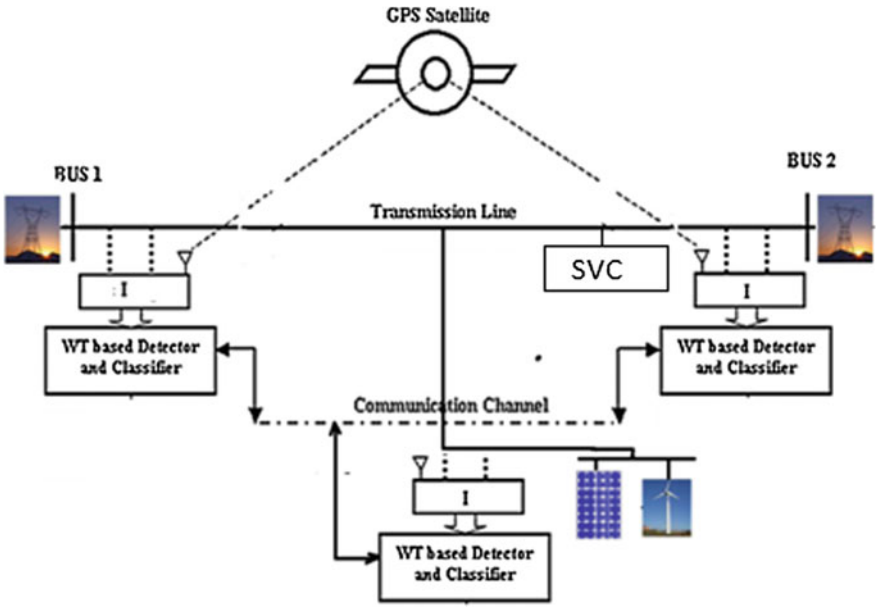


Fig. 2 Single line diagram of SVC compensated multi-terminal transmission system with hybrid energy source

Table 1 Power system specification and corresponding wavelet characteristics

Generator 1		500 kV, 9000 MVA Y-g, X/R = 10, phase angle = 0°
Generator 2		500 kV, 9000 MVA Y-g, X/R = 10, phase angle at A = 20°
Hybrid system	Wind	10.5 MVA
	PhotoVoltaic	1.25 MVA
Distributed transmission line		R = 0.01273 Ω/km, R_0 = 0.3864 Ω/km L = 0.9337e−3 H/km, 4.1264e−3 H/km C = 12.74e−9 F/km, C_0 = 7.751e−9 F/km
Static var compensator (SVC)		Rating: 300-Mvar Coupling transformer: 500 kV/16-kV 333-MVA One 109-Mvar thyristor-controlled reactor bank (TCR) Three 94-Mvar thyristor-switched capacitor banks
Mother wavelet		Bior 1.5
Sampling frequency		216 kHz
Information analyzed		Detail at 1, D1
Frequency band		108–54 kHz
Number of samples per cycle		21,600
Occurrence of fault		Second cycle
Data window length		One cycle/17.7 ms

evaluating transient signal [8] at different frequencies with resolutions can be effectively studied by wavelet multi resolution analysis of power system transients.

4 Description of the Proposed System

Figure 2 describes single line diagram of static var compensator compensated multi-terminal transmission system with hybrid energy source with all terminals of the proposed scheme (Table 1).

5 Proposed Scheme for MTL Protection

Synchronized sampling at all the three terminals of three-phase currents is carried out with the help of a global positioning system. The absolute values of the detailed coefficients for three-phase currents of all the three terminals are determined using Bior 1.5 mother wavelet. The detail coefficients are used for discriminations of fault in the MTL system [9]. The detail coefficients generated from phase currents of each terminal and then sum of the detailed coefficients are calculated. The number of faulty phases is discriminated by using the sum of the detailed coefficients [10] with a fault threshold value of three-phase currents. The proposed scheme is tested

for various types of faults at different locations and fault inception angles in the range 0–180°. It is possible to state that the technique is effectively working in detecting and discriminating all possible types of faults.

6 Simulation Results

The fault indices of three-phase current signals are obtained by using wavelet first level detail coefficients of Bior 1.5 mother wavelet. The number of faulty phases can be identified by comparing fault index I_{f1} of each phase current with the predetermined threshold value Th_1. It is observed that the fault index of phase A is very large compared to that of other phases as illustrated in Fig. 3. Thus, Phase A to ground fault at 40 km distance from terminal-1 of transmission system. Figure 4 shows that three-phase currents and Local D1-coefficients at terminal-1 multi-terminal transmission system with SVC (Fig. 5).

The Fault Index I_{f1} is calculated with various locations from 10 to 100 km with step size is 10 km up to middle point of the transmission line from terminal-1 is illustrated for SLG, DL of all combinations of phase A, phase B and phase C. It is observed that fault index If1 of all faulty phases is greater than Threshold T_{h1} value. The fault Index of healthy phases remains less than the threshold value. So that the faulty phases determined effectively which are illustrated in Figs. 6, 7 and 8 and it describes that the Fault index and variation of distance of 3ph Currents for SVC

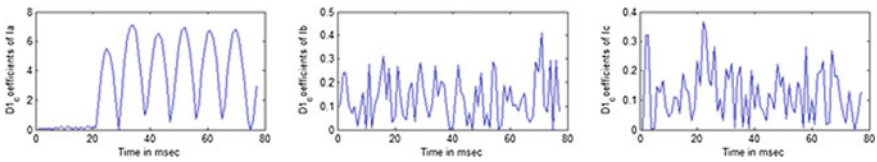


Fig. 3 Phase A to ground fault at 40 km distance from terminal-1 of transmission system with deviation of effective coefficients

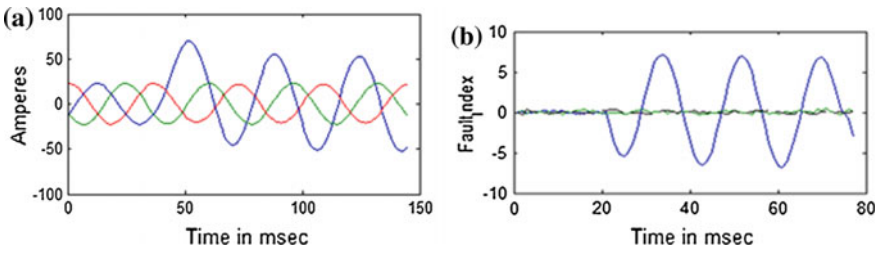


Fig. 4 **a** Three-phase currents at terminal-1 of Phase A to ground fault at 40 km distance of the line with SVC. **b** Local D1-coefficients of terminal-1 for Phase A to ground fault with SVC

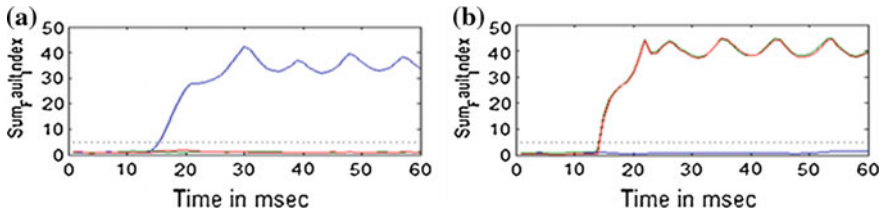


Fig. 5 Sum of detailed coefficient index varying at terminal-1 from 40 km distance with **a** single line to ground **b** double line

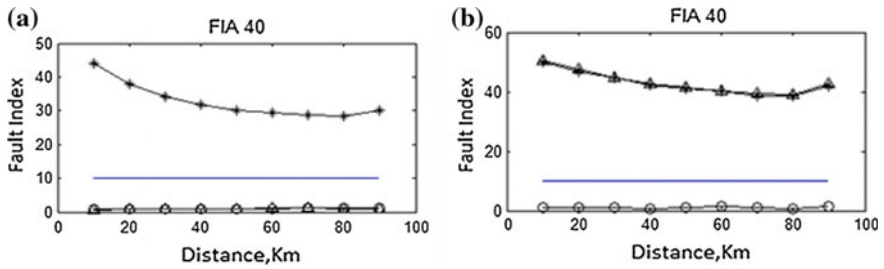


Fig. 6 Fault index and variation of distance of 3ph currents for fault inception angle of 40° for SVC compensated multi-terminal transmission system with hybrid generation at terminal-1 **a** SLG fault **b** DL fault

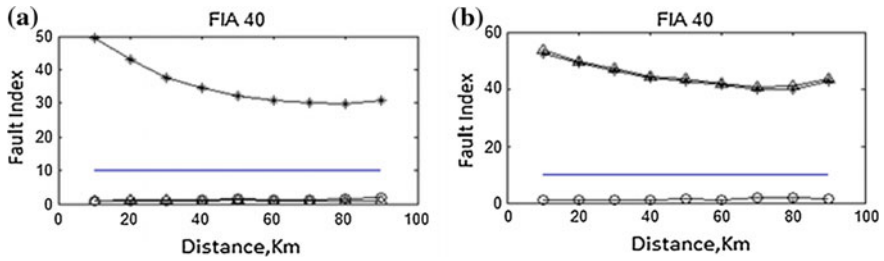


Fig. 7 Fault index and variation of distance of 3ph currents for fault inception angle of 40° for SVC compensated multi-terminal transmission system with hybrid generation at terminal-2 **a** SLG fault **b** DL fault

compensated multi-terminal transmission system with hybrid generation of 40° at terminal-1 for SLG, DL. The effect of variation fault index is studied by varying the fault inception angle ranging from 0° to 180° in steps of 20° at various locations. In all the cases I_{f1} is always less than T_{h1}. Figures 9, 10 and 11 illustrates variation in fault index and incidence angle of three-phase currents at terminal-1 for 40% of the transmission line with SVC at line to ground fault and double line fault. It is observed that the proposed algorithm detects the fault less than half cycle using wavelet analysis.

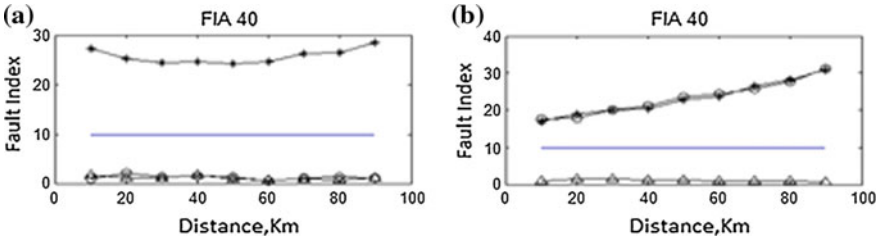


Fig. 8 Fault index and variation of distance of 3ph currents for fault inception angle of 40° at terminal-3 **a** SLG fault **b** DL fault

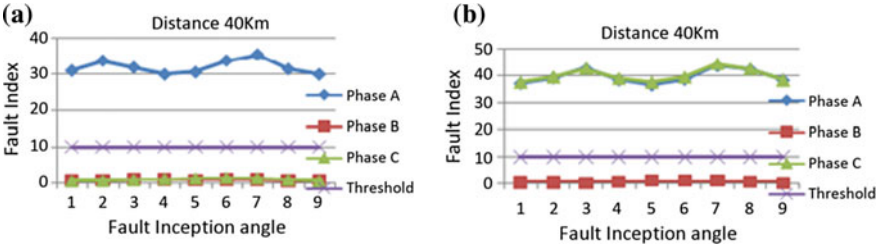


Fig. 9 Variation in fault index and incidence angle of three-phase currents at terminal-1 for 40% of the transmission line with SVC. **a** SLG fault **b** DL fault

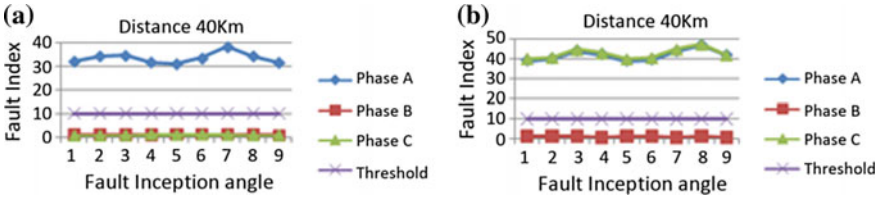


Fig. 10 Variation in fault index and varying incidence angle of three-phase currents at terminal-2 for 40% of the transmission line with SVC **a** SLG fault **b** DL fault

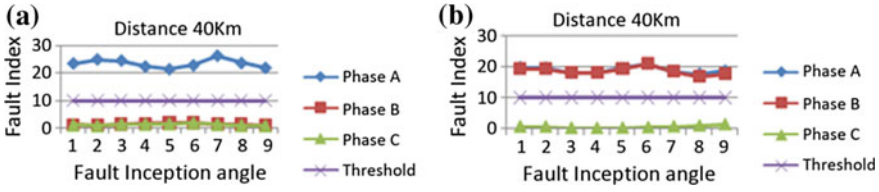


Fig. 11 Variation in fault index and varying incidence angle of three-phase currents at terminal-3 for 40% of the transmission line with SVC. **a** SLG fault **b** DL fault

7 Conclusions

The proposed system is developed for multi-terminal transmission system with hybrid PV and wind energy source with static var compensator using simulation software. The paper describes the protection algorithm for detection and classification of short circuit faults using wavelet-based multi-resolution analysis approach. The fault Indices are calculated with various locations at all the three terminals by analyzing the detailed coefficients of the current signals. Detection and discrimination of the fault in the system is analyzed by the wavelet coefficients of current signals which are greater than the threshold value which indicates the type of fault is observed. It is found that the scheme is working reliable and accurate for several types of faults at different locations and at different fault inception angles with and without SVC.

References

1. Giovanni Manassero, Jr., Eduardo Cesar Senger, Renato Mikio Nakagomi, Eduardo Lorenzetti: Fault-Location System for Multiterminal Transmission Lines, IEEE Transactions on Power Delivery, Vol. 25, July (2010).
2. Bikash Narayan Panda: Microgrid- A Smart Grid for Community Users. Proceedings of National Seminar on Dispersed Generation and Smart Grid.
3. Aditi, Dr. A.K. Pandey: Performance Analysis of grid connected PV Wind Hybrid Power System. International Journal of Applied Engineering Research ISSN 0973-4562 Volume 11, pp 706–712 © Research India Publications (2016).
4. Kola Venkataramana Babu, Manoj Tripathy and Asheesh K Singh: Recent techniques used in transmission line protection: a review. International Journal of Engineering Science and Technology, Vol. 3, pp 1–8 (2011).
5. M. A. Redfern, J. Lopez, and R. O'Gorman: A Flexible Protection Scheme for Multi-Terminal Transmission Lines. pp. 7803–9156. IEEE (2005).
6. Peyman Jafarian and Majid Sanaye-Pasand: High-Frequency Transients-Based Protection of Multiterminal Transmission Lines Using the SVM Technique, IEEE Transactions On Power Delivery, pp. 885–8977, IEEE(2012).
7. Liang Feng, Jeyasura B: Transmission line distance protection using wavelet transform algorithm, IEEE Trans Power Delivery, pp. 545–53, IEEE (2004).
8. Ravi Kumar Goli, Abdul Gafoor Shaik, S.S Tulasi Ram: A transient current based double line transmission system protection using fuzzy-wavelet approach in the presence of UPFC Electrical Power and Energy Systems, pp. 91–98 (2015).
9. Y. Manju Sree G. Ravi Kumar Abdul Gafoor Shaik: Multi-Terminal Transmission Line Protection using Wavelet Based Digital Relay in the Presence of Wind Energy Source ICEEOT (2016).
10. Osman AH, Malik OP: Transmission line distance protection based on wavelet Transform, IEEE Trans Power Delivery, pp. 515–523(2004).

ARM-Based Industrial Circuitous like Robotic Implementation Using CAN Bus for Surveillance

T. Sairam Vamsi and G.R.L.V.N. Srinivasa Raju

Abstract The major objective of this paper is to design a circuitous- or serpentine-like robot using Controlled Area Network and controlling through ARM. Generally snakes can capable of crawl and wriggle on any kind of surface to make an effective locomotion even in rough paths. The design of this robot consists of legs instead of wheels, because design with wheels can limit the usage of robot in some particular areas like hills, terrines, and rough surfaces Dowlink (Proceedings 1999 IEEE International Conference on Robotics and Automation, 2015, [1]). This robot is implemented with the advanced communication modules like CAN bus, ARM Controller, and ZigBee Technology. Controlled Area Network (CAN) Bus will be for transferring real-time data transfer between the robotic section and monitoring section. This robot is equipped with some sensors for surveillance and the data from sensors are transmitted through monitoring section using ZigBee Technology. The heart of the design is ARM controller, which is the advanced controller rather than 8051, PIC and AVR microcontrollers for performing all the actions of robot. Such kinds of robotic implementations are best used in the conditions like earth quakes, environmental hazards, etc., for inspection and surveillance.

Keywords Snake robot · CAN bus · Locomotion model · Sensors · ZigBee · ARM

T. Sairam Vamsi (✉) · G.R.L.V.N. Srinivasa Raju
Department of ECE, Shri Vishnu Engineering College for Women (AUTONOMOUS), Bhimavaram, India
e-mail: vamsi.0438@gmail.com

G.R.L.V.N. Srinivasa Raju
e-mail: hodece@svecw.edu.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_28

1 Introduction

Generally there are several kinds of robotic models are existing which are inspired from nature physically and geographically. There are many creatures that have special features similarly snake is also having the ability to crawl and wriggle to make a movement. There are many metrics for choosing the design of the robot as snake because most of the robots are developed with wheels which gives smooth movement on plain surface but on rough surfaces they faces the problem [1]. General feature of snake is without legs, these can penetrate through normal or rough surface smoothly and easily, this concept is used for the design of this circuitous or serpentine robot.

There are several methods for snake locomotion which is defined from the observation of naturally existing different kinds of snakes; such as lateral undulation, which has the limitation while snake runs in smooth surface because of the lack of holding grip; concertina method, which is very useful in curbed places like tunnels and very narrow places; side-winding technique, which is mostly used by desert snakes where surface gets slippery and loose. Last method is rectilinear method, related to elastic skin of snake which internally connected to skeleton acts [2].

2 Design Methodology

The robot locomotion model used in the design is wriggle model as shown in Fig. 1. In this model, each servomotor and section of robot is alternately up and down according to angle calculations to make a robot movement forward [3].

Here, each section is equipped with one servo motor and relay on the wave with different angles which is used to vary time derivation of position. All the angles of each servo motor is predefined in the program written in Keil software and CAN bus will send these values to servo motors. The type of servo motor used for the design is VTS-05A also known as economically friendly motors.

The Fig. 2 shows the motor dimensions and it will be operated with 6v and speed 0.10 s per 60° at no load [3, 4]. To make the movement of snake robot, the servo motors are programmed with the following angles which are shown in table (Table 1).

The above table shows different angles for servomotor by assuming five modules for the circuitous model. Not only five modules, it is possible to add many number of modules for smooth movement of robot, so some load is added at tail to make a move as normally snakes have weight in their head.

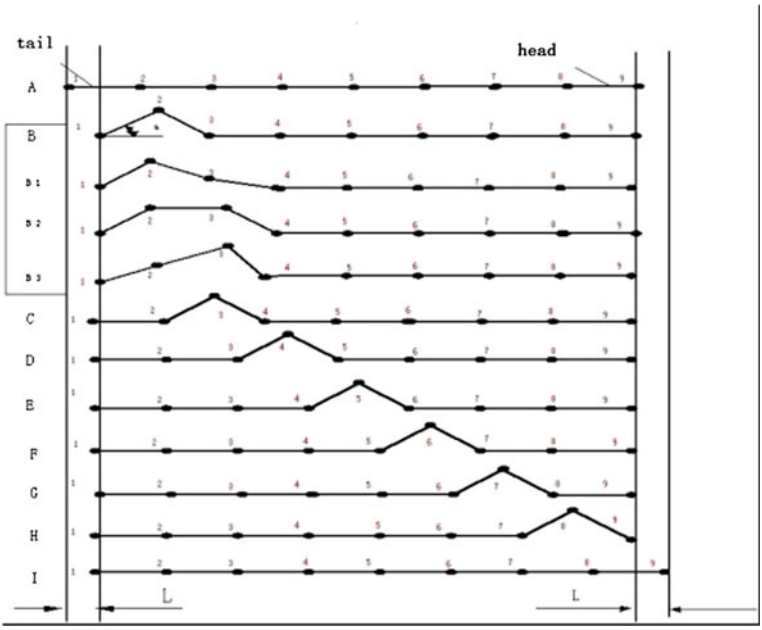


Fig. 1 Wriggle locomotion model

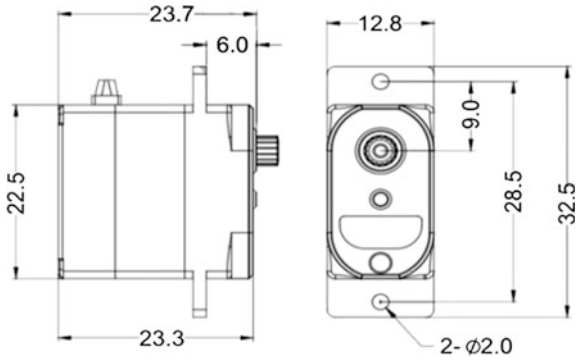


Fig. 2 Dimensions of servo motor

Table 1 Angle representation for servo motors

Servo 1	Servo 2	Servo 3	Servo 4	Servo 5
0	0	75	75	75
150	150	150	75	75
75	0	0	0	75
75	75	150	150	150

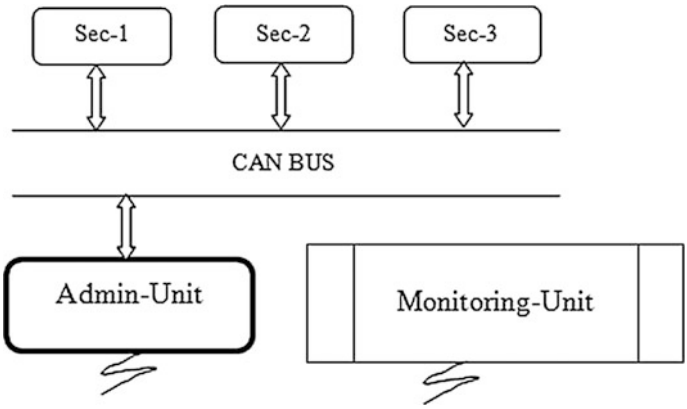


Fig. 3 Overall architecture of the system

3 System Architecture and Comparative Study

The total design of the robot is divided into three sections, such as (Fig. 3)

- Robot section
- Control section or admin section)
- Monitoring section, nothing but personal computer.

Control section will be used to control all the actions performed by the robot using ARM controller and ZigBee Module. For performing controlling action, the robotic hardware is implemented with two ARM controllers named as LPC2148 and associated hardware which is accountable for robot movement and communicating sensor values to the monitoring section using ZigBee [5]. Monitoring section is used for inspection. Robotic section consists of all other hardware modules such as L293D IC, MAX-232, etc.

A. **Comparission between controllers**: (Table 2)

Table 2 Comparsion table between different controllers

Parameter	Atmel family	PIC	ARM	AVR
Operating frequency	12–15 MHz	20 MHz	40–60 MHz	<20 MHz
RAM	<4 kB	20 kB	32–512 kB	<64 kB
Communication protocols	UART, I2C	UART, SPI, I2C, ADC, CAN, LIN, ETHERNET	UART, SPI, I2C, ADC, CAN, LIN, ETHERNET, IrDA	UART, SPI, I2C, ADC
Cost	Very low	Average	Low	Average
Memory architecture	Von-newmann	Modified harward	Modified harward	Harward

The table shows the comparison between different families of controllers for different parameters. But observing the above parameters with all controllers ARM gives best results for the large designs especially for the development of robots. The designers prefer ARM controllers because of its operating frequency and communication protocols that it supports [6].

4 Arrangement of Administrative Unit

The administrative unit consists of ARM7TDMI controllers (LPC2148), CAN Bus controller (MCP 2515), ZigBee transceiver, and some other interfacing connections.

B. ***Controller***

Generally the main role of controller is to process all the information coming from different types of sensors and CAN bus and activating corresponding servo motors for snake movement and sensor values are transmitted to monitoring section in real time. For performing two functions, the robotic equipment requires two controllers of same machine or different machine. One controller continuously communicates the sensed values to monitoring section. And another controller will be used for controlling the robotic section. Hence two Advanced RISC Machines (ARM7TDMI) are used in the design [7].

Figure 5 shows the indication of all the components present in the ARM Board. The major features of LPC2148 are on chip memory, operating frequency, and on board devices. It is a 32 bit controller with program memory 512 kb and data memory of 32 kb. It has up to 60 MHz operating frequency; hence speed of microcontroller is very high compared to other types of controllers. It has many onboard peripheral devices like I2C, SPI, two UARTs, 10Bit ADC Channels, etc.

C. ***Outlining CAN BUS***

The existing communication busses like Inter Integrated Circuit (I2C), Serial peripheral Interface (SPI) are having some limitations such as low data rates and low speed transmission. To overcome this limitation, in 1983, Robert Bosch one of the pioneer of automation industry developed the "controller area network" with high data rates and high speed. Since the release of CAN bus into the market, it made big impact on the automation industry. It is mostly useful for quick process and to avoid catastrophes [8].

This CAN bus provides different types of services

- **Fault confinement**: This feature is used for detecting permanent failures from short disturbances.
- **Message validation**: After data frame is transformed to CAN, protocol format it is validated by message validation.
- **Error detection**: It will be used for performing different types of functions like frame check, Bit stuffing, Bit monitoring, Acknowledge check, and cyclic redundancy check (Fig. 4).

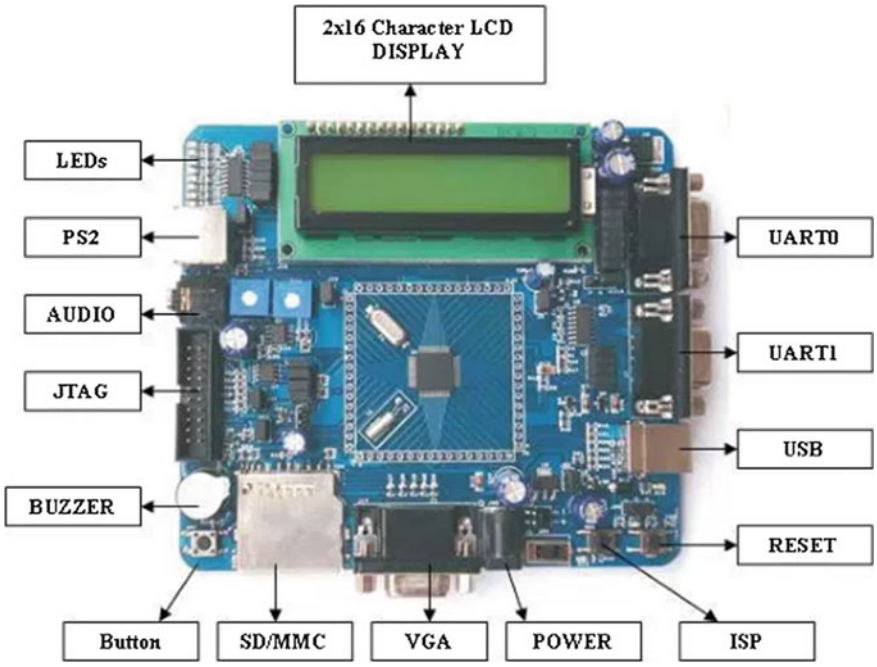


Fig. 4 ARM7TDMI (LPC2148) development board

D. CAN Controller

CAN Controller plays a vital role for effective communication between different machine controllers. There are different types of CAN controllers available such as MCP 2515, MCP 25625, etc. This MCP 2515 IC consists of 18 pins which has serial pins for SPI and CAN Transmission, reception, etc. LPC2148 does not have in-built CAN controller; so to convert SPI to CAN format, MCP 2515 integrated circuit is used. The data communication is established through this controller only [9].

E. Communicati on Network

There are so many communications techniques for wireless communication like Dual Tone Multi-Frequency (DTMF), Radio frequency communication, Infrared communication, etc [10]. Out of all, for industrial surveillance of monitoring all the sensor information and transmitting to monitoring section in real time, ZigBee devices are very useful which has precise features like reliability and power consumption. ZigBee is standardized with IEEE 802.15.4 physical band with frequency range 2.400–2.484 GHz.

Generally ZigBee module consists of transmitter device and receiver device. The communication is like

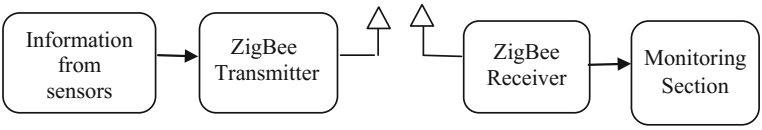


Fig. 5 ZigBee communication

From the above Fig. 5, information from sensors will be transmitted to ZigBee transmitter through RS232 and MAX-232 which acts as interfacing device and level shifter between ZigBee and processor. The ZigBee receiver is connected to Monitoring section through processor.

F. Sensors and Other Hardware

The major application of the robot is surveillance; hence it requires inspection of different critical parameters like temperature, humidity, gas, pressure, etc. The prototype of this robot is equipped with humidity and temperature sensors which are monitored in real time. It is possible to add many sensors to the LPC2148 controller. For activating sensors and communicating sensor information to PC, it follows the algorithm as shown in Fig. 6. Once the information from ZigBee transmitter is received by ZigBee receiver, then a special interfacing cable like RS232 will be used for transferring data to PC through HyperTerminal in Windows PC.

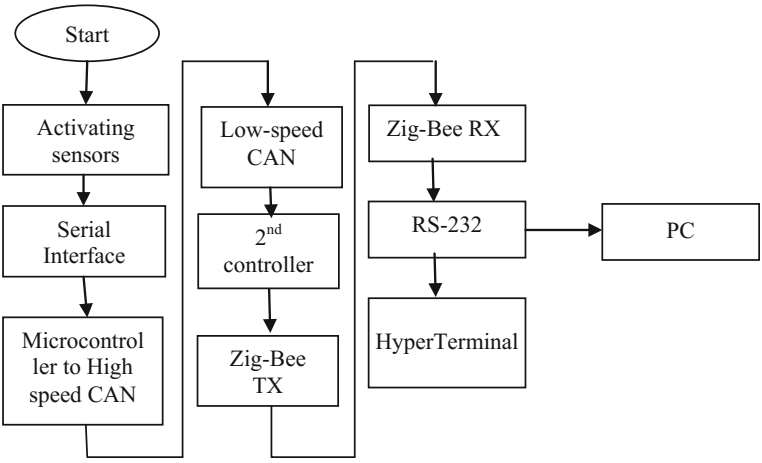


Fig. 6 Flow of sensor values

5 Algorithms for Controlling Climbing Robot

A. CAN Transmission

The above Fig. 7 shows how real-time data from sensor are transmitted through CAN bus to the monitoring section. The flowchart is explained with the half of transmitter instruction formats supported by CAN bus and Keil software for performing programming. When CAN bus is available, then information will be transmitted through bus to the monitoring section and if information is not transmitted successfully and even CAN bus is active, then the CAN bus sends error message to source.

B. CAN Reception

The figure shows how a real-time data from CAN Transmitter. The flowchart is explained with the half of receiver instruction formats supported by CAN bus and Keil software for performing programming. When CAN receiver detects a valid message then it will send to original receiver, if not, it will send an error message indicating that valid message is not received.

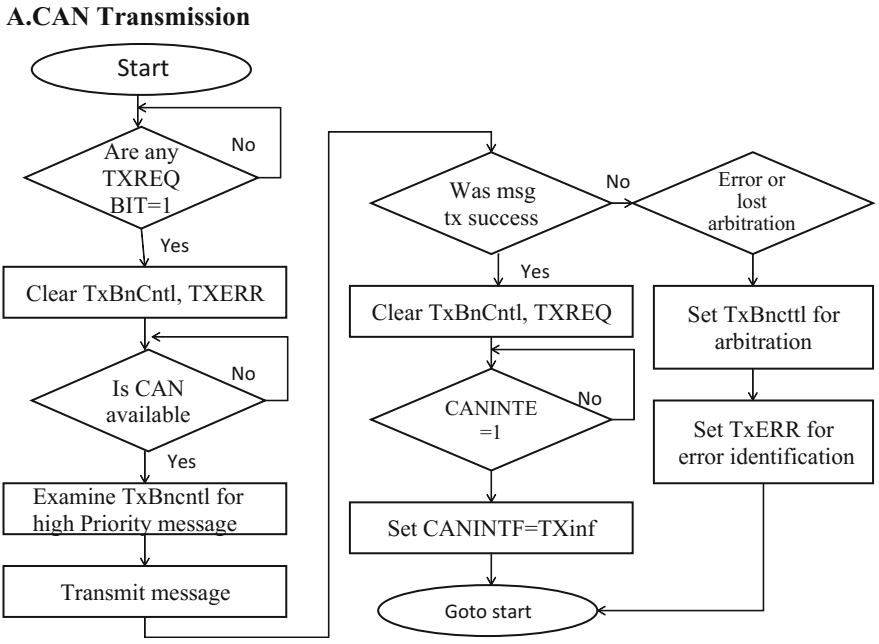


Fig. 7 Flowchart for CAN transmission

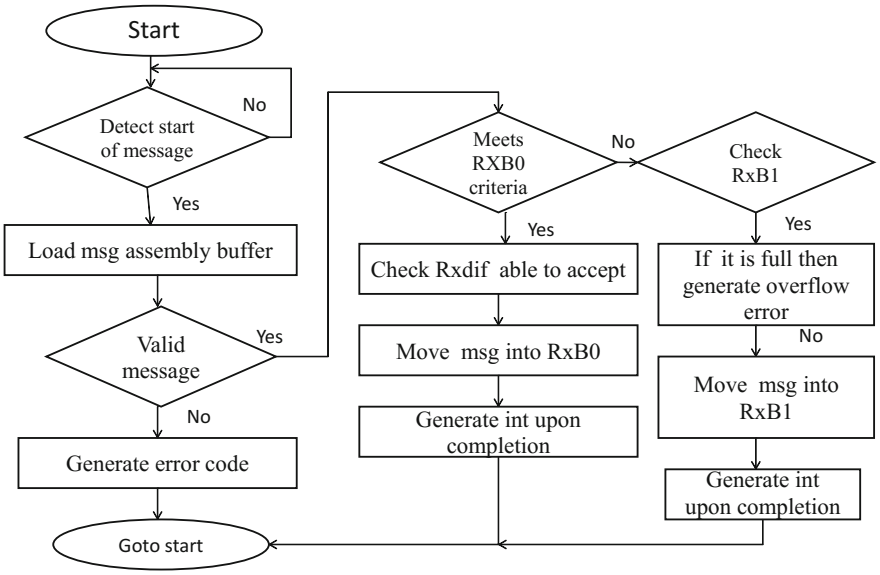


Fig. 8 CAN reception

C. Software Architecture

Centralized software architecture is used in this robotic hardware and controller responsible for servo motor angle calculation and proper transmission. Servo motors are provided with proper Pulse Width Modulated (PWM) signals by driving circuitry [11]. Modules are differentiated with identifiers given to them for the purpose of avoiding collisions on CAN bus. Keil µvision3 software IDE is used for compiling and debugging the code because the Keil software having inbuilt compiler named as C51 and inbuilt assembler named as A51 along with debugger, linker, and locator. This Keil software is compatible for code written under ARM and ATMEL family of controllers only (Fig. 8).

6 Monitoring Unit and Experimental Results

Measured values such as temperature and humidity of different environments can be communicated by two ways.

- Using Liquid Crystal Display (LCD) directly available on LPC2148 development board.
- Dsiplaying values in PC by Interfacing the ZigBee receiver with proper baud rate to PC by MAX-232 and RS-232 connector will be displayed in HyperTerminal. If PC has advanced operating system them XTU-T software will be used for displaying information [9] (Fig. 9).

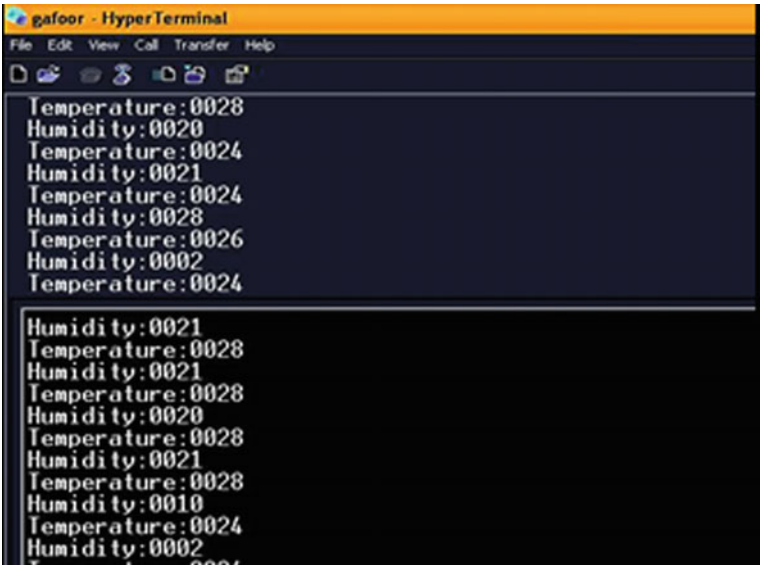


Fig. 9 Monitored values on PC

The Fig. 10 shows the complex setup of robot. The designed robot consists of group of several modules approximately six modules, out of five modules are controllable and sixth module is added as load (weight) [12]. Generally snakes have weight in their heads that helps them in wriggling, so the same feature is added to this model also to push the robot in the required direction.

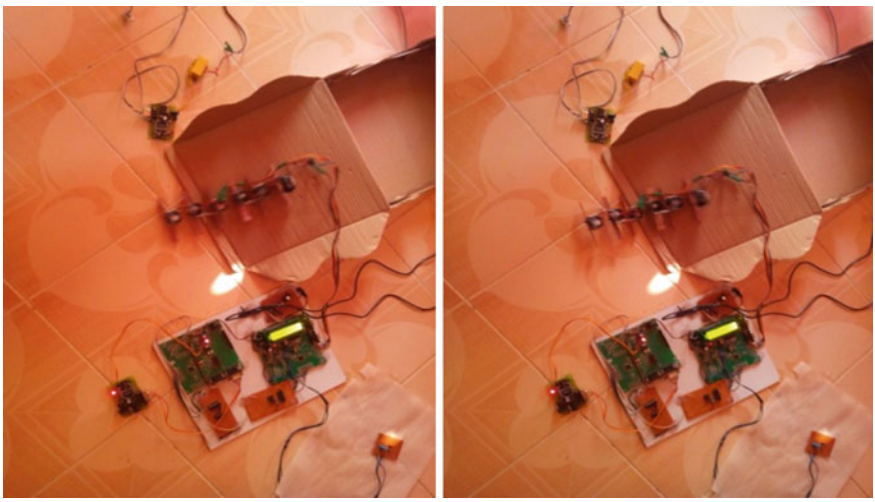


Fig. 10 Serpentine model robot

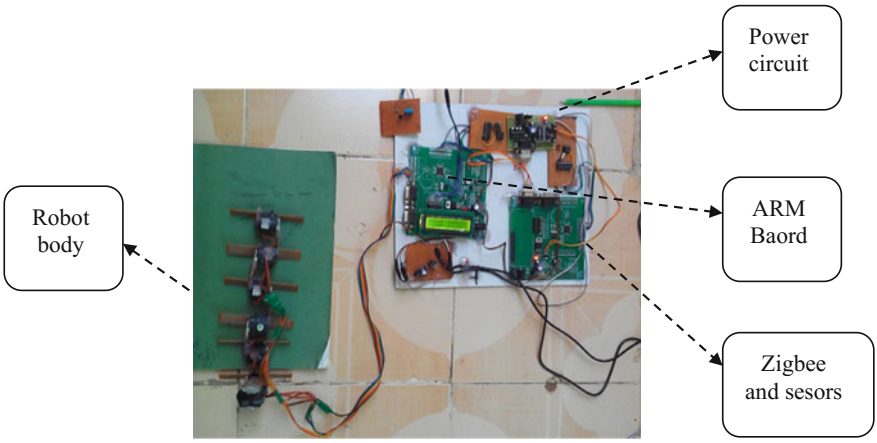


Fig. 11 Complete board set up

The above Fig. 11 shows complete board setup along with robot and on the development board LCD is displaying the parameters measured by sensors.

7 Conclusion

ARM-based industrial circuitous like robot using CAN bus for surveillance is designed and implemented. Here this serpentine or circuitous robot can run in any kind of surfaces like flat, rough, and terrains too. It uses the ARM7TDMI (LPC2148) as processing unit, different types of sensors like temperature and humidity for industrial surveillance, ZigBee module for communicating sensor information to the monitoring section and finally CAN bus for transferring the data from sensors to ZigBee transmitter through controller and some hardware units like RS232 and MAX-232. This robot is not only useful in industries and also in different types of places where surveillance and monitoring is required. This can be extended by adding camera and more sensors to the robot.

References

1. Dowling, K.: Limbless locomotion: learning to crawl. Robotics and Automation, 1999. Proceedings. 1999 IEEE International Conference on, vol. 4, no., pp. 3001,3006 vol. 4, (2015)
2. Hirose, S.; Yamada, H.: Snake-like robots [Tutorial]. Robotics & Automation Magazine, IEEE, vol. 16, no. 1, pp. 88, 98, (March 2014)

3. Murai, R.; Ito, K.; Nakamichi, K.: Proposal of a snake-like rescue robot designed for ease of use -Improvement of operability for non-professional operator- Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE, vol., no., pp. 1662,1667, 10–13 (Nov. 2008)
4. Bayou Song; Guohui Tian; Guodong Li; Fengyu Zhou; Dongxu Liu.: ZigBee based wireless sensor networks for service robot intelligent space. *Information Science and Technology (ICIST), 2011 International Conference on*, vol., no., pp. 834,838, 26–28 (March 2011)
5. He Li; Bo Yin; Shanshan Wang; Qingshu Yang.: Design of underwater robot controller based on CAN bus. *Electronic and Mechanical Engineering and Information Technology (EMEIT), 2011 International Conference on*, vol. 9, no., pp. 4906,4909, 12–14 (Aug. 2016)
6. Rashid, M.T.; Ali, A.A.; Ali, R.S.; Fortuna, L.; Frasca, M.; Xibilia, M.G.: Wireless underwater mobile robot system based on ZigBee. *Future Communication Networks (ICFCN), 2012 International Conference on,* vol., no., pp. 117,122, 2–5(April 2012*)*
7. MCP 2515 CAN controller driver manual. http://www1.microchip.com/downloads/en/devicedoc/21801e.pdf
8. Zhang Yue; Li Xin; Zhou Xianli. A Reconfigurable Snake Robot Based on CAN-Bus. *Computer Science and Electronics Engineering (ICCSEE), 2012 International Conference on,* vol.1, no., pp. 493,497, 23–25 (March 2012)
9. Varga, M.; Pogar, I.; Varga, P.; Mate, A.; Vegh, J.: Developing sensors and real-time controlling software for a robot," *Carpathian Control Conference (ICCC), 2012 13th International,* vol., no., pp. 752,756, 28–31 (May 2012)
10. Chen Li, Wang Yuechao, Ma Shugen, Li Ben.: the Research of a Reconfigurable Snake Robot, China Mechanical Engineering Phase 1, (2003)
11. VTS- 05A servo motor data sheet http://www.vigorprecision.com.hk/uploadfile/20120530/20120530173622817.pdf
12. ARM7 controller (LPC2148) data sheet http://www.keil.com/dd/docs/datashts/philips/lpc2141_42_44_46_48.pdf

SIW-Based Uniform Slotted Leaky-Wave Antenna at Ku Band with FR4 Dielectric Material

Manish Trivedi and D.K. Raghuvanshi

Abstract In this paper, SIW leaky antenna has been investigated with FR4 substrate. This SIW leaky antenna consists of a series of circular holes with pitch of 0.75 mm along with six cut slots. The width of SIW has been taken as 10.5 mm. Simulations are carried out using tetrahedral mesh using physics controlled mesh with coarser element size. The SIW antenna achieves uniform radiation properties between 15°–75° at 12.25 GHz.

Keywords SIW · Leaky-wave antenna · Slot

1 Introduction

Traditionally, waveguide has characteristics of good gain and other contenders like Microwave Integrated Circuit (MIC) are smaller in size files but with lesser gain. In terms of Quality factor Q, Normal waveguide has better value as compared to MIC. For designing high-performance millimeter-wave system, classical waveguide technology has to be used and this technique is unsuitable for cost effective bulk production [1] as post-fabrication tuning and assembling become a tough task for manufacturers at later stages for finer changes. Further, the waveguide technique suffers from bulkiness. Between these extremities their lies SIW (Substrate integrated waveguide) which offers best of both world with Higher Q than MIC and many other parameters comparable as normal waveguide networks [2].

SIWs can be studied by exploiting the theory of classic rectangular waveguides. They are built by using two rows of conducting cylinders [3] at the outer edge of the dielectric substrate within a waveguide-like structure. The top and bottom plane are electrically conductive metal plates (Fig. 1). Most of the normal waveguide can be

M. Trivedi (✉) · D.K. Raghuvanshi
Department of Electronics & Communication Engineering, NIT-Bhopal, Bhopal, India
e-mail: trivedi.work@gmail.com

D.K. Raghuvanshi
e-mail: dkraghuvanshi3@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_29

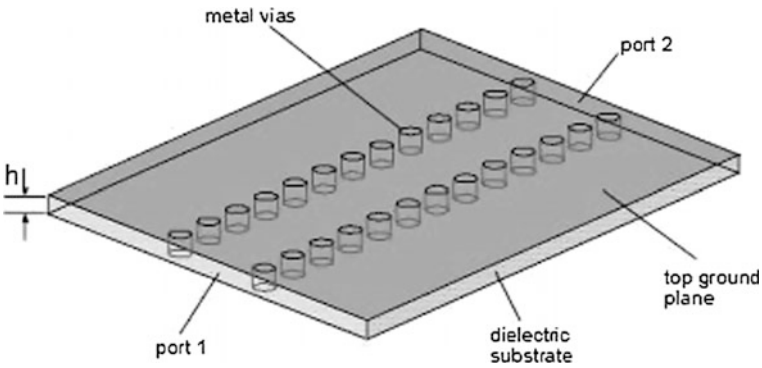


Fig. 1 SIW basic structure

bulky and heavy while SIW structure are in planar form. The planar form provides major benefit as it is compatible with existing planar processing techniques like standard printed circuit board (PCB) or low-temperature co-fired ceramic (LTCC) technology.

SIW structure shows wave properties similar to ones of conventional waveguide. It shows drastically similar field pattern and dispersion characteristics. Classical waveguide exhibit high quality factor and power handling capacity which in turn is matched by SIW in broader perspective. It is also called post-wall waveguide or laminated waveguide.

Moreover, another major advantage is that there is possibility to integrate one or more chip-sets on the same substrate. There is no need for transitions between elements fabricated by different methods utilizing nonplanar form to planar form thus reducing microwave losses [4].

2 Design Equation of SIW

With geometrical similarity between SIW and rectangular waveguide, mathematical relations have been obtained. The SIW dimensions choice must be chosen carefully in order to get desired specifications [5]. In this case, the two plain perfect conductors walls are replaced by metallic posts, cylinders must be the closest possible to end towards a rectangular waveguide filled with air or dielectric material.

The cutoff frequency of a rectangular waveguide is given as

$$f_c = \frac{c}{2\pi\sqrt{\mu_r \varepsilon_r}} \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \tag{1}$$

The cut off frequency at fundamental TE_{10} mode is determined [6] by the following equation:

$$f_c = \frac{c}{2a} \tag{2}$$

$$a_d = \frac{a}{\sqrt{\varepsilon r}} \tag{3}$$

The width of SIW waveguide width is given by

$$a_s = a_d + \left(\frac{d^2}{0.95p}\right) \tag{4}$$

d diameter of the via
p distance between the via
f_c cutoff frequency for the waveguide
a_d effective width of waveguide with dielectric waveguide
a_s equivalent width of waveguide

Substrate Integrated Waveguides (SIW) have been used as Leaky-wave antenna [7]. Waves are emitted from a slot array on the top surface of this model. The emitted beam in a certain direction can be steered by properly choosing an operating frequency. Substrate integrated waveguides (SIWs) are mostly preferred as they are easy to fabricate and any shape of slotted patterns can be drawn on the top surface.

3 SIW Design

SIW leaky antenna has been investigated with FR4 substrate. This SIW leaky antenna consists of a series of circular holes with pitch of 0.75 mm along with six cut slots. The width of SIW has been taken as 10.5 mm. The thickness of substrate is 1.524 mm. In this SIW, a 50 Ω microstrip line in and output is linearly tapered to a wider line at the middle of a 1.524 mm thick substrate with εr = 4.70. The tapering length section is of 1.5 mm while the port length section is taken as 3.25 mm (Fig. 2).

The microstrip line and the ground plane play the role as the top and bottom walls of the waveguide and side walls are constructed by adding metallic vias between the wider part of a microstrip line and the ground plane. All metallic parts are modeled using perfect electric conductor (PEC). For impedance matching of 50 Ω, a circular slot is provided on both tapered sides with 3 mm diameter.

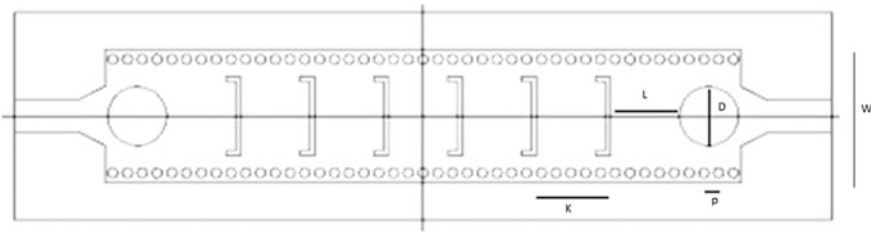


Fig. 2 SIW leaky wave antenna with L 4 mm, K 3.5 mm, D 3 mm, p 0.75 mm, w 6.5 mm, outer width 10.5 mm, outer length 41.5 mm

Six slots along the line of vias are placed on the top surface of the microstrip line for a leaky wave radiation. The antenna is modeled in a spherical air domain. The air domain is perfectly terminated with the Perfectly Matched Layers (PMLs) which absorb all outgoing radiation.

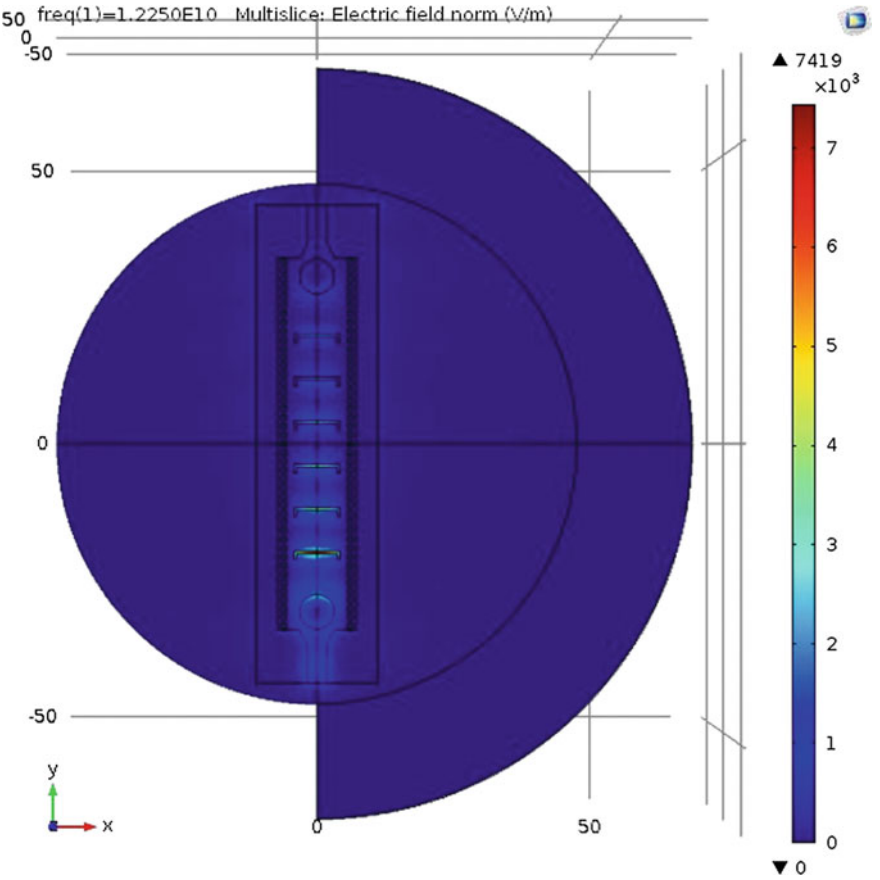


Fig. 3 Electric field distribution in SIW leaky wave antenna

The calculated cutoff frequency of the SIW is 7.765 GHz having the width 10.5 mm at TE_{10} mode. In this design via distance pitch p is taken as p = 2d [8]. The cutoff frequency as discussed in (Eq. 1) is lower than the operating frequency.

4 Results

Figure 3 shows the default electric field norm plot on xy-plane. The electric field intensity of the coupled to each slot continuously diminishes as we move from input port to output port. As the wave travels inside the SIW, the phase of the each slot continuously changes.

The combination of change in electric field strength and phase determine the weight function for slot array antenna SIW leaky-wave antenna's maximum radiation pattern can be steered by controlling the operating frequency.

The 3D far-field radiation pattern is visualized in Fig. 4. Though the slots are open to the upward direction, the radiation pattern is tilted toward the outport at 12.25 GHz scattering parameter for this SIW leaky antenna has been found to be 16.84 db at 12.25 GHz. Figure 5 shows the polar plot for the same and its quiet evident that 3db beamwidth covers large angle.

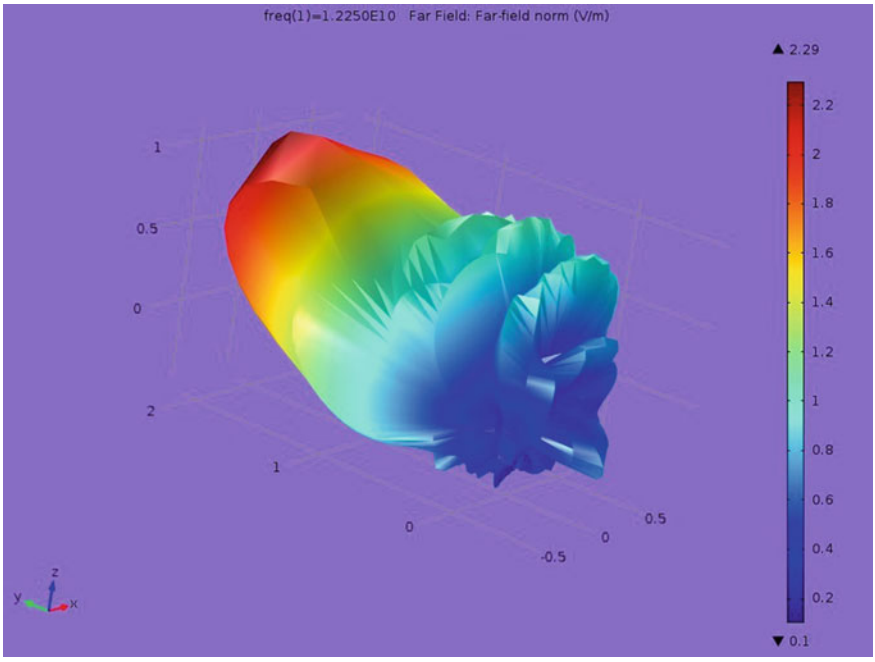


Fig. 4 Far field radiation pattern

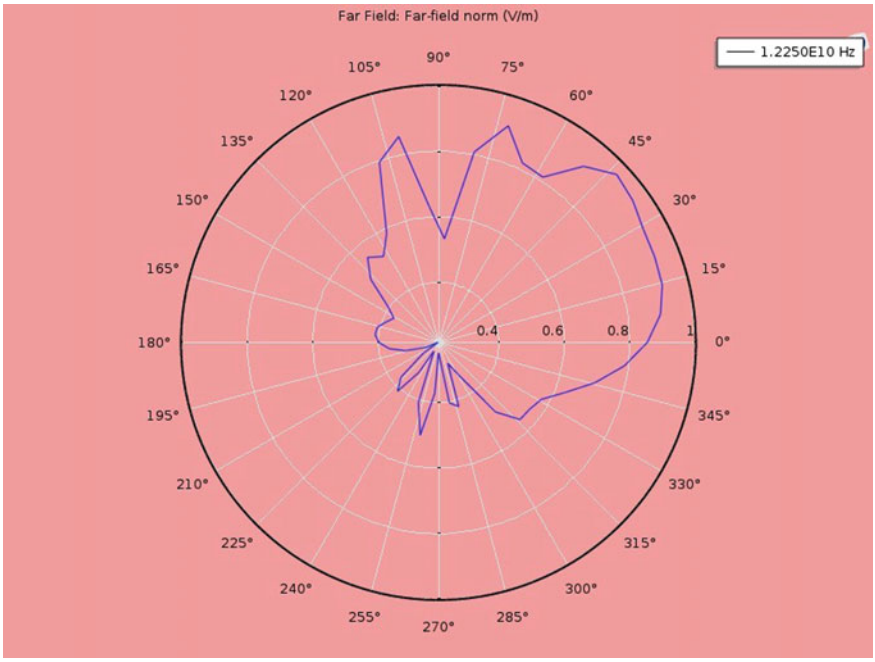


Fig. 5 2D polar plot for the field

5 Conclusion

This paper has presented SIW leaky wave antenna with antenna array of six elements to operate in Ku band. Reflection coefficient (s11) at 12.25 GHz is found to be 16.84 db. This antenna achieves a near about uniform radiation properties between 15°–75° in azimuthal plane.

Such antenna can be good candidate for 45° sectorized antenna useful for Satellite and Military applications.

References

1. Ke Wu, Dominic Deslandes, and Yves Cassivi.: The Substrate Integrated Circuits - A New Concept for High-Frequency Electronics and Optoelectronics IEEE Microwave Review (2003) 1–8
2. D. Zelenchuk, V. Fusco.: "Low insertion loss substrate integrated waveguide quasi-elliptic filters for V-band wireless personal area network applications," IET Microwaves, Antennas Propag. vol. 5, no. 8, (2011) 921
3. S. Moitra, A. K. Mukhopadhyay, A. K. Bhattacharjee.: Ku-Band Substrate Integrated Waveguide (SIW) Slot Array Antenna for Next Generation Networks,vol. 13, no. 5, (2013)

4. M. Bozzi, L. Perregrini, K. Wu, P. Arcioni.: Current and Future Research Trends in Substrate Integrated Waveguide Technology vol. 18, no. 2, (2009) 201–209
5. N. Keltouma, D. Mehdi, and C. Tc.: Design of substrate integrated Waveguide single longitudinal slot antenna, vol. 2, no. 11, (2013) 794–797
6. M. A. Rabah, M. Abri, J. W. Tao, and T. Vuong.: Substrate Integrated Waveguide Design Using the Two Dimensional Finite Element Method vol. 35, (2014) 21–30
7. J. Liu, D. R. Jackson, Y. Long, and S. Member.: Substrate Integrated Waveguide (SIW) Leaky-Wave Antenna With Transverse Slotsn vol. 60, no. 1, (2012) 20–29
8. Feng Xu and Ke Wu.: Guided-Wave and Leakage Characteristics of Substrate Integrated Waveguide IEEE Transactions On Microwave Theory And Techniques, Vol. 53, No. 1, January (2005) 66–70

Detecting the Sonar Target by Using Optimization Technique

T. Pavani, M. Rajeswari and Ch. Padma Vani

Abstract The general important problems in a lot of application areas are to pull out the signal of interest from background noise. Background noise is an indiscriminate form; the occurrence of the signal and the performance of signal are also indiscriminate. Thus, it is sensible to deal with the signal removal problem using methods based on optimization technique and statistical estimation. Within this paper, signal and noise environment has been encountered in active sonar system. The optimum receiver is obtainable for range-Doppler-shift dispensation in a background-noise-limited environment using firefly optimization method for dropping the noise. There are various techniques for target detection, but this paper shows a new approach for target detection using a firefly algorithm to optimize the received signal by reducing the noise. FFT-based implementation for detection of CW active sonar target using firefly optimized algorithm has been shown.

Keywords Optimum detector · Background-noise-limited · FFT-based implementation · Ambiguity function · Firefly algorithm

1 Introduction

In SONAR, SO stands for Sound, NA stands for NAvigation and R stands for Ranging. A sonar system contains many similarities to that of radar and also some with electro-optical systems. The process of sonar is based on the propagation of sound waves between a target and a receiver. The main purpose of sonar is the detection or classification (estimation of position, velocity and identity) of

T. Pavani (✉) · M. Rajeswari
Department of ECE, Vignan's Institute of Information Technology, Visakhapatnam, AP, India
e-mail: pav.tum@gmail.com

Ch. Padma Vani
Department of ECE, Vignan's Institute of Engineering for Women, Visakhapatnam, AP, India

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_30

submerged, floating or buried objects [1, 2]. The nature of the required object, known as the sonar target, depends on the application. Examples include man-made objects of military significance (a mine or submarine), shipwrecks (as a navigation hazard or archaeological artifact), and fish (the target of interest to a whale or fisherman). In military applications, sonar systems are used for detection, classification, localization and tracking of submarines, mines or surface contacts, as well as for communication, navigation and identification of obstructions or hazards. In commercial applications, sonar is used in fish finders, medical imaging, material inspection and seismic exploration [3].

There are two most familiar types of sonar system. One is passive sonar and other is active sonar. Passive sonar is the system in that contains only the receiver but does not have a transmitter in order to transmit the input signal. The signal which is to be detected is the sound which is emitted by the target. In an active sonar system, the waves propagate from a transmitter to a target and back to a receiver, analogous to pulse-echo radar [4].

Active sonar knows more about the signal to be detected, and therefore the receiver is designed to match the signal, i.e. it uses matched filter processing [5]. But the background, against which the signal has to be detected, contains reverberation in addition to the ambient noise and self-noise of passive sonar [6–8]. This additional background is all important in active systems and the designer has to be aware of its magnitude as well as how to discriminate beside it. Active sonar mainly uses two types of pulses. Continuous wave (CW) is a pulse which has constant frequency and the duration of the pulse is T seconds. The bandwidth of the pulse, and of the matched filter is used for optimum detection of the pulse, is 1/T Hz. Frequency modulation (FM) is which the frequency of the pulse changes throughout the T second's duration of the whole pulse which to be transmitted. The bandwidth is denoted by B, which is not inversely proportional to of the pulse length of the given pulse [9].

The detection of a scatterer and the estimation of its parameters are some of the main goals of active sonar. Sonar waveforms are transmitted into the ocean, and their echo signals are processed for information pertaining to range and velocity characteristics of any scatterers, that the signals encounter [10]. The ability to successfully estimate these scatterer parameters in different situations depends on the sonar waveforms that are used to gather this information. Some waveforms have good delay (or range) resolution but poor Doppler (or velocity) resolution, while others exhibit excellent Doppler resolution but inferior delay resolution. Here, in this paper, a new method for target detection of active sonar is used. FFT-based implementation for background-noise-limited environment [11, 10] using CW pulse is shown which gives both Doppler and range resolution.

Here, in this paper, Sect. 2 gives a quick review about the continuous wave pulse [11]. Section 3 says about Range-Doppler-shift processing. Section 4 deals with fast Fourier transformation (FFT) based implementation [11] of CW active sonar and final results are shown.

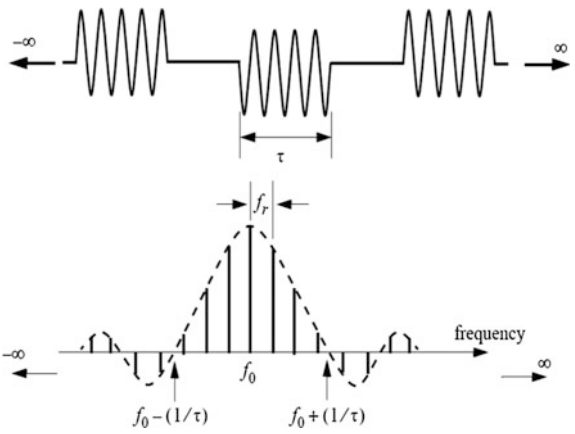


Fig. 1 Amplitude spectrum for a coherent pulse train of infinite length

A. **Modelling of Continuous Wave Pulse**:

The continuous wave (CW) pulse can be modelled as s(n) is given by [12] (Fig. 1).

$$s(n) = \begin{cases} \exp\left(\frac{2j\pi f_0 n}{f_s}\right); & -\frac{N}{2} \le n \le \frac{N}{2} - 1 \\ 0; & \text{otherwise} \end{cases} \quad (1)$$

2 Range-Doppler-Shift Processing in Background-Noise-Limited Environment

In this section, the optimum detector for the CW pulse in a background-noise-limited environment is considered. Consider the CW pulse which is being operated in zero-mean white Gaussian. The quadrature receiver is said to be optimum detector for the following reason. The problem of detecting a CW pulse is equivalent to that of detecting a sinusoidal signal of finite duration in noise.

3 FFT-Based Implementation

This FFT-based implementation involves two variables unlike the narrowband, broadband and modulation processors. The hypotheses are

$$\begin{aligned} H_1 &: x(n) = s\left(n - n_i, \beta_j\right) + g(n) \\ H_0 &: x(n) = g(n) \end{aligned} \tag{2}$$

The composite receiver consists of a set of optimum detectors which are adjusted to the discrete frequencies, βj, j = 1, … J. A set of discrete time, n_i is calculated where i = 1, 2, … I. The maximum output of the J detectors at each value of n_i is compared with the threshold. If the maximum output exceeds the threshold then the corresponding frequency value to which the detector is matched serves as the estimate of β, or Doppler shift. The time at which the detection is occurred is the estimate of range.

A. **Processing of CW**

A bank of parallel detectors is implemented. Each detector is adjusted to separate f, $\beta_j = \delta_i f_o$. The output of the detector is calculated at the time intervals of $n_1, n_2, \ldots n_l$. At the ith time, the output of the jth optimum detector is given by

$$q_j^2(n_i + N) = \left[\sum_{n=n_i}^{N-1+n_l} x(n) \sin\frac{j2\pi\beta_j n}{f_s}\right]^2 + \left[\sum_{n=n_i}^{N-1+n_l} x(n) \cos\frac{j2\pi\beta_j n}{f_s}\right]^2 \tag{3}$$

The global maximum over the indices i and j in the previous equation provides the estimates of the range and Doppler shift. A DFT, followed by an SLD for each frequency bin, is approximate realization of quadrature receiver. The length of the DFT is matched to the duration of the pulse.

Consider a set of CW with the centre frequency of 3 Hz. The lengths of the pulses ranging from 5 ms to 1 s are considered. By using these set of pulse lengths, the effect of reverberation noise pulse for contacts with various values of Doppler shift is minimized. The maximum velocity is said to be as 30 knots in magnitude and c is assumed as 3000 knots. The compression parameter at maximum v, δ = 2 v/c will fall in the range of $-0.02 \leq \delta \leq 0.02$. Therefore, the maximum Doppler shift magnitude is equal to 60 Hz.

To obtain an FFT-based implementation for 62.5–1000 ms pulses. The frequency width varies inversely with T, it achieves a maximum value of 32 Hz for the 62.5 ms pulse. As a result of Doppler shift, the received centre frequency occurs in the range of $f_o - 60 \leq f \leq f_o + 60$. After shifting the centre of spectrum to zero frequency, the highest frequency in the baseband data is given by 76 Hz. Selecting a sampling frequency of 256 Hz at the input to the FFT results in a transition region for the low pass filter, $f_a - f_p$ is equal to 104 Hz. The highest frequency in the analog data is equal to the sum of the normal centre frequency, the maximum Doppler shift and half of the maximum power spectral width. Therefore, the highest frequency in the analog signal is 3260 Hz. If aliasing is allowed in the transition region of analog filter then a sampling frequency of 8192 Hz results in transition region of $f_p/(f_s - f_p)$ is equal to 0.66. This corresponds to use of a 6-pole 6-zero elliptic anti-aliasing filter. It is desirable to use a short analog filter by over sampling

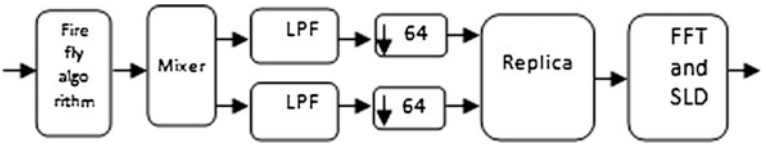


Fig. 2 Signal processing for the CW pulses

the analog filter to 16384 Hz. This is given to the square law detector. The output is compared with threshold to detect whether the target is present or not. The length of the FFT is given by Tfs which is equal to 265. The FFT length to the pulse length is matched [11] (Fig. 2).

First, firefly algorithm is implemented to the received signal in order to remove the noise. By considering all the above, the fitness function is formulated as follows

$$\text{Cost} = \min(\text{MSE}) \tag{4}$$

$$\text{MSE} = (F_2 - F_1)^2 \tag{5}$$

where MSE is the mean square error, F_2 received signal from the target and F_1 is the transmitted signal.

4 Firefly Algorithm

Firefly algorithm (FA) is the lone of the most recent swarm intelligence meta-heuristics. In this algorithm, the search is stimulated by the flashing behaviour of fireflies and the happening of bioluminescent communication [13]. The flashing light helps fireflies for finding mates to attract their potential prey and defending themselves from their predators. The most important principle of the algorithm is that each firefly move towards brighter and more eye-catching (attractive) locations by the flashing light intensity that is related with the intention function of the problem which is considered [14].

The progress of firefly algorithm is based on three idealized set of laws:

- Each one of the fireflies attracts all other fireflies which are weaker flashes without considering of their sex.
- Attractiveness is directly proportional to their brightness and decreases with the distance between them increases.
- The brightness of a firefly which is affected and determined by the allocation of the objective function.

For the purpose of maximization difficulty, brightness can be just proportional to the value of the cost function. Other form of brightness is able to be defined in a like method to the fitness function in genetic algorithm. The fundamental steps of the FA can be summarizing as the pseudo-code.

Begin

1. Initialize parameters of the algorithm for finding the maximum generation, α, β_o, γ
2. generate initial population of N fireflies $x= (x_1, x_2, x_3 \ldots x_D)^T$ inside D dimensional searching space
3. Objective function f(x), $x= (x_1, x_2, x_3, \ldots\ldots\ldots, x_D)^T$
4. find out I_i at x_i resolute by $f(x_i)$
5. While (t < maximum generation)
   For i=1 to N (all N fireflies)
   For j=1 to N (all N fireflies)
   if ($I_j > I_i$)
   Move a firefly i in the direction of j in dimension D
   End if
   Estimate new solutions and then update light Intensity
   End for j
   End for i
   Then rank the fireflies to find out the current best
   End while
   Post the process results and then visualize
   End procedure

In this algorithm, every firefly has a location $x = (x_1, x_2, x_3 \ldots x_D)^T$ in a D-dimensional searching space. Light intensity is considered as I(x) (or) attractiveness as β(x), which are directly proportional to an objective function f(x). The brightness of a firefly and the attractiveness of each firefly are calculated at every iterative step. The positions of the fireflies are updated according to these values. All fireflies meet to the best probable position on the searching space after an adequate quantity of iterations.

5 Simulation and Results

The transmitted CW pulse of frequency 3 kHz is shown in Fig. 3a. The delayed and Doppler shifted signals are shown in Figs. 3b and c respectively. The sampling frequency is 16384 kHz. Pulse width is 62.5 ms. Number of samples is 1025 samples. The transmitted CW pulse Power spectral density is shown in Fig. 4a. The PSD of delayed and Doppler shifted signals are shown in Figs. 4b and c respectively. Received signal with White Gaussian Noise is shown in Fig. 5. Received Signal after applying fire fly algorithm where noise is suppressed is shown in Fig. 6. PSD of receiver output inphase and out phase components after filter are shown in Fig. 7. The in-phase and quadrature-phase components after decimation are shown in Fig. 8.

Command window results:

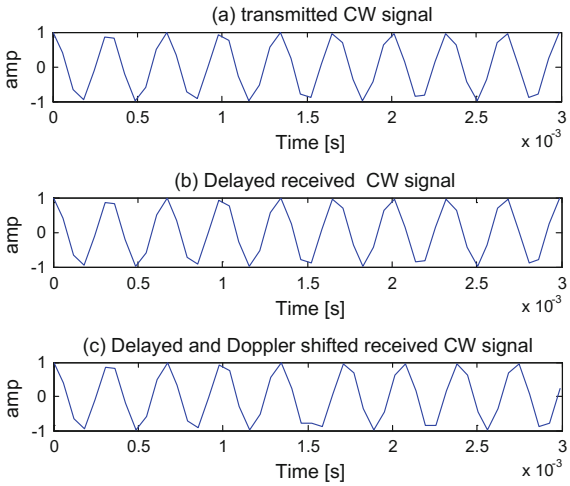


Fig. 3 **a** Transmitted CW signal. **b** Delayed received CW signal. **c** Delayed and Doppler shifted received CW signal

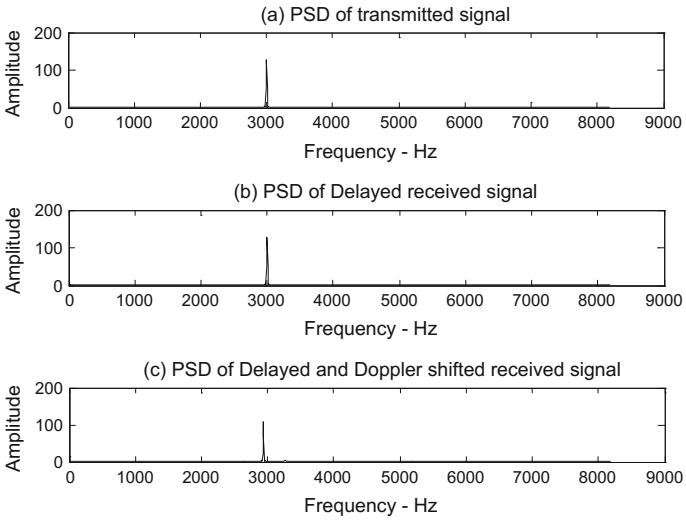


Fig. 4 **a** PSD of transmitted CW signal. **b** PSD of delayed received CW signal. **c** PSD of delayed and doppler shifted received CW signal

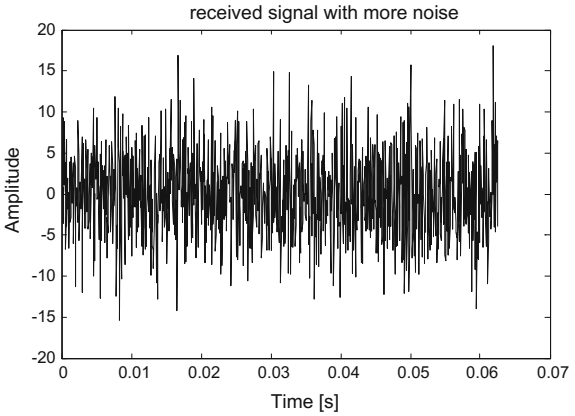


Fig. 5 Received signal with *White* gaussian noise

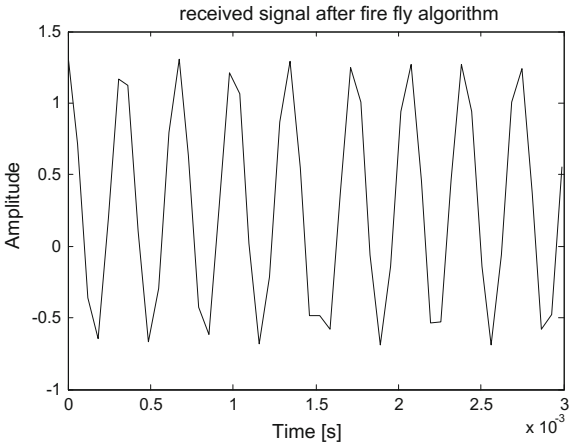


Fig. 6 Received output signal after applying firefly algorithm where noise is suppressed

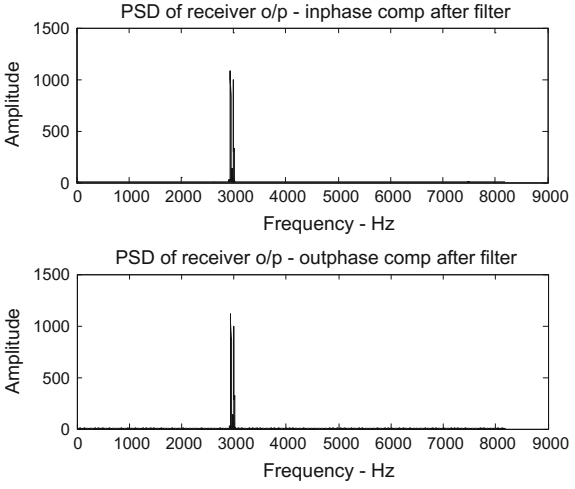


Fig. 7 PSD of receiver output inphase and outphase components after filter

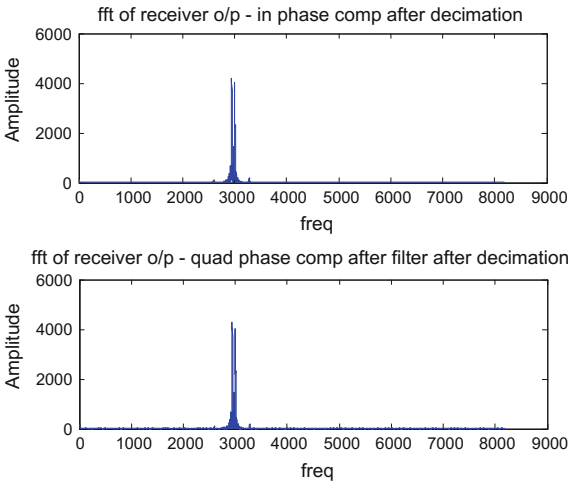


Fig. 8 FFT of receiver output inphase and outphase components after filter after decimation

6 Conclusion

The FFT-based implementation of CW active sonar under noise background environment using firefly optimized algorithm is implemented using MATLAB successfully and the results are shown. By using this method the optimum receiver has been designed for range-Doppler-shift processing in a background-noise-limited environment using firefly optimization technique and the noise has been suppressed as shown in Fig. 6. The threshold using Neyman–Pearson (NP) criterion is found out. The maximum output of the detector is compared to that threshold in order to detect the target presence. The target presence is shown in command window. FFT of received Doppler shift signal is shown. By using firefly optimized algorithm, the resolution of the FFT which obtained is as fine as 3-dB Doppler shift intercept of the ambiguity diagram. At output of the filter, the length of the FFT is given by T fs = 265.

References

1. Prior. M. K.: "A scatterer map for the Malta Plateau," IEEE Journal of Oceanic Engineering, vol. 30, no. 4, pp. 676–690, (October 2005)
2. Yang. X. S.: Firefly algorithms for multimodal optimization. In Stochastic algorithms:foundations and applications (pp. 169–178). Springer Berlin Heidelberg. (2009)
3. Michael A. Ainslie.: Principles of Sonar Performance Modeling. Springer New York, (2010)
4. Urick, Robert J.: Principle of Underwater Sound (McGraw-Hill), (1975)
5. Whalen, Anthony D.: Detection of signals in Noise. (Academic Press, N. York), (1971)

6. Dorfman. Y. Y., Dyer. I.: Monostatic and bistatic reverberation statistics west of the mid-atlantic ridge. The Journal of the Acoustical Society of America, vol. 106, no. 4, pp. 1755–1764, (1999)
7. Abraham. D. A., Lyons. A. P.: Novel physical interpretations K-distributed reverberation, IEEE Journal of Oceanic Engineering, vol. 27, no. 4, pp. 800–813, (October 2002)
8. La Cour. B. R.: "Statistical characterization of active sonar reverberation using extreme value theory," IEEE Journal of Oceanic Engineering, vol. 29, no. 2, pp. 310–316, (2004)
9. Waite. A. D.: SONAR for Practising Engineers', Third Edition, Wiley (2002)
10. William S Burdic.: Underwater Acoustic System Analysis, Englewood Cliffs, NJ: PrenticeHall. (1984)
11. Richard O Neilson. Sonar Signal Processing, Artech House, (1991)
12. Preston. J. R., Abraham. D. A.: Non-Rayleigh reverberation characteristics near 400 Hz observed on the New Jersey Shelf. IEEE Journal of Oceanic Engineering, vol. 29, no. 2, pp. 215–235, (April 2004)
13. Pavani, T., Raju, G. S. N., Sridevi, P. V.: Synthesis of Thinned Concentric Ring Array with Dipole Radiators Using Firefly Algorithm, vol. 9, no. 5, pp. 40–48 (September 2014)
14. Pavani. T., Rudra Pratap Das, Naga Jyothi. A., Sampath Dakshina Murthy. A.: Investigations on Array Pattern Synthesis using Nature Inspired Metaheuristic Algorithms, vol. 9, no. 2, pp. 1–11 (January 2016)

Study of Slotted E-Shaped Rectangular Micro-Strip Antenna

M.V. Chaitanya Eswar, V.P.Ch. Vinay Kumar, P.V. Akhilesh and P. Chandra Sekhar

Abstract This paper overviews the study of E-shaped rectangular Micro-Strip Antenna with multi-band frequencies which includes the study of VSWR, Gain parameter and far-field patterns within the operating frequencies 2–10 GHz and these interpretations are graphically represented. The substrate used is FR-4 (lossy), copper (annealed) used as a ground plane and also as a patch which gives the best results for the proposed antenna whose dimensions are $40 \times 37 \times 3.7$ mm in CST STUDIO 2014, where a gain of -74.74 dB and VSWR $= 1.0003$ are obtained at a frequency of 3.28 GHz.

Keywords Rectangular micro-strip antenna · VSWR · Gain parameter · Far-field pattern · Multi-band frequencies

1 Introduction

Carved micro-strip antenna, which is also known as *rectangular Micro-Strip Antenna,* is a low profile radio antenna, which is installed on a leveled surface. It is composed of a rectangular-shaped sheet (patch) of a metal, installed on top of a large metal sheet called as ground plane. Micro-Strip transmission line consists of a resonant piece which can be formed by bringing two metal slabs together and it works effectively, when the length of the transmission line is approximately equal

M.V. Chaitanya Eswar (✉) · V.P.Ch. Vinay Kumar · P.V. Akhilesh · P. Chandra Sekhar
Department of ECE, GITAM University, Visakhapatnam, India
e-mail: eswarchaitanya66@gmail.com

V.P.Ch. Vinay Kumar
e-mail: vpcvinay@gmail.com

P.V. Akhilesh
e-mail: pvakhilesh5696@gmail.com

P. Chandra Sekhar
e-mail: chandrasekhar.au@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_31

to half of the wavelength of radio waves because electrically, the antenna behaves larger when compared to its original physical dimensions. This effect is caused due to the radiation procedure that occurs at docked edges of Micro-Strip transmission line [1]. Some characteristics of the antenna such as Gain, far-field patterns, etc. vary in accordance with the material type and thickness of substrate and patch [2].

This paper contains design of a micro-strip antenna with exploiting elements which has high Gain when compared to regular micro-strip antenna. Different dimensions of several materials are considered along with their di-electric constants to determine the resonant frequency of the antenna with proposed dimensions and are theoretically calculated. The simulation results are shown in CST Microwave Studio-2014 for the proposed theoretical calculations. The most interesting aspect of the proposed antenna is its size, low cost, easily fabricated and their provision of wider bandwidth.

2 Antenna Geometry

The proposed compact-carved Micro-Strip Antenna consists of a slot and a feeding line on dielectric substrate of thickness 3.5 mm and ground plane of about 0.1 mm thick. These are some of the optimal dimensions of antenna for obtaining a maximum gain with the combination of materials, copper (annealed) used as a ground plane and patch, FR4 (lossy) used as a substrate whose dimensions are shown in Table 1.

3 Analysis

The Gain parameter expounds the efficiency of a transmitting antenna. The ratio of power created by an antenna from a far-field source on the antenna beam axis and power created by speculative lossless isotropic antenna is generally defined as antenna gain [3]. For this antenna, we get a gain of −74.74 dB, by using FR-4 (lossy) as dielectric.

In Microwave engineering and tele-communications, standing wave ratio abbreviated as SWR is defined as amplitude of a limited standing wave at an anti-node to that of the amplitude at node along a transmission line. SWR quantizes

Table 1 Antenna construction and dimensions

S.no.	Used as	Material	Measurements (l * b * h) mm
1	Ground	Copper (annealed)	40 * 37 * 0.1
2	Substrate	FR4 (lossy)	40 * 37 * 3.5
3	Patch	Copper (annealed)	18 * 18 * 0.1
4	Feeder line	Copper (annealed)	12.25 * 0.25 * 0.1

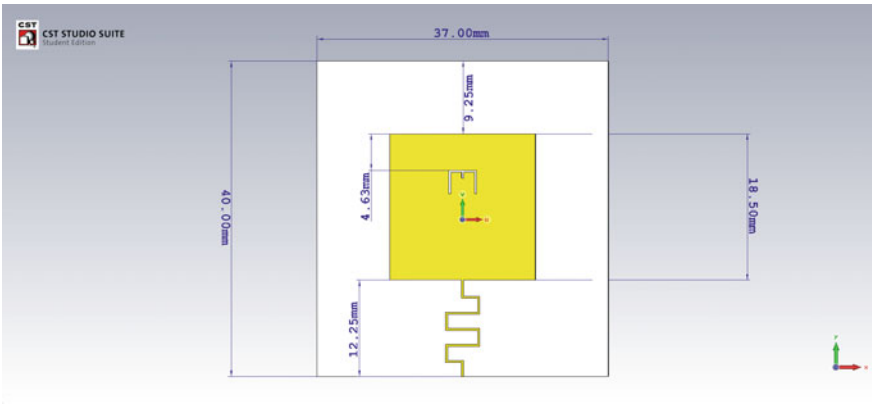


Fig. 1 Micro-strip antenna [5]

the impedance harmonizing of a load with the characteristics of a transmission line. In general, impedance mismatch effects in the power transfer. Since SWR is precisely measured as ratio of maximum to minimum AC voltages, it is called as VSWR (Voltage standing wave ratio). These characteristics of antenna are successfully analyzed either in close field or far-field range with suitable implementations. The plot of many associated variables like the field strength at a constantly large radius; the power per unit solid angle and the directive gain are the graphical representations of the radiation pattern (far field). Generally, only the relative amplitude which is normalized either to the amplitude on the antenna boresight or to the total radiated power, is only plotted. The charted quantity is shown in either in dB or on continuous scale. In general, a three dimensional plot is used or graphs for horizontal and vertical planes are used, respectively. This plot is called polar diagram [4]. The antenna dimensions and structure are clearly mentioned in Figs. 1, 2, and 3.

3.1 Design Interpretations and Calculations

In general, the most regularly utilized Micro-Strip Antenna is a Rectangular strip which looks like a docked Micro-Strip transmission line which is approximately of half wavelength long of a radio wave. According to Howell Micro-Strip antenna, if air is considered as a di-electric substrate, then the length of the rectangular Micro-Strip Antenna should be approximately equal to half of a free-space wavelength. This relates the length of the antenna inversely proportional to the length of the antenna. Hence, whenever a dielectric is used as a substrate, the length of the antenna increases with the decrease in relative dielectric constant. The resonant length of the antenna is slightly shorter because of increase in electrical length of the antenna slightly due to extended electric "Fringing fields." The above replica of

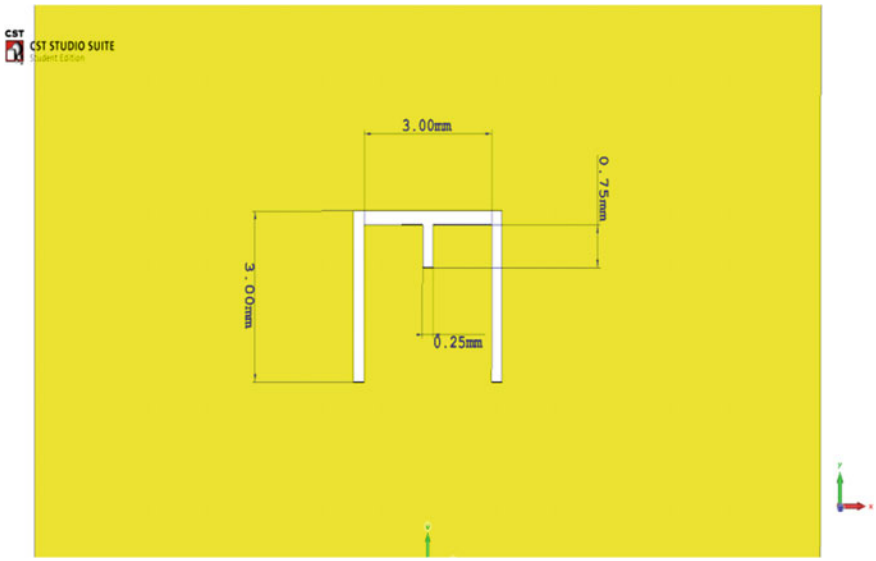


Fig. 2 Patch

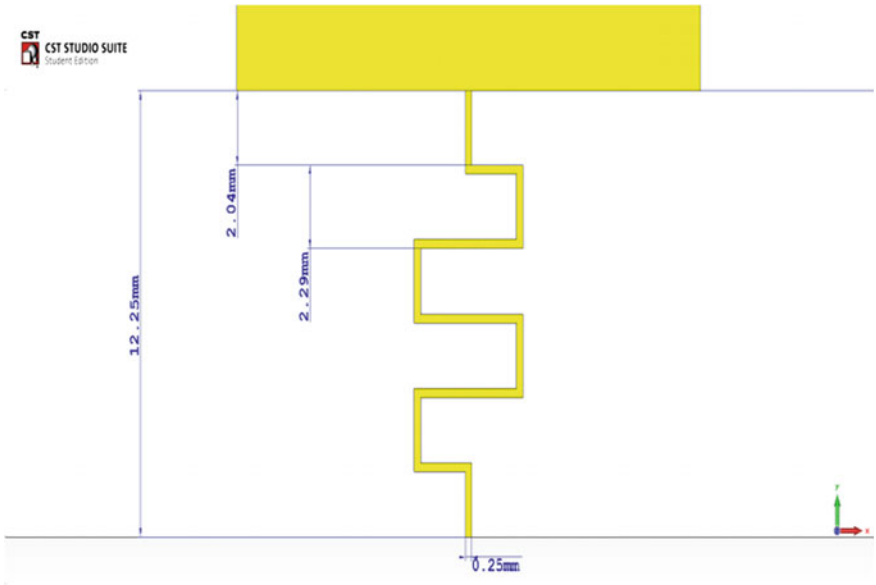


Fig. 3 Feed-line

the Micro-Strip Antenna is a segment of Micro-Strip transmission line with equivalent loads on either end to represent the radiation loss [6].

Impedance bandwidth, Radiation pattern of a Micro-Strip antenna is affected by loading of dielectric. The increase in dielectric constant of a substrate results in decrease of antenna bandwidth which in turn increases the Q-factor of the antenna and therefore decreases the impedance bandwidth. The radiation from a rectangular Micro-Strip Antenna may be comprehended as two equivalent slots. These slots behave in an array in which the highest directivity of an antenna is achieved when air is used as dielectric. When the antenna is brimmed with materials having high dielectric constant, the directivity of an antenna decreases [7]. Here we have taken FR-4 (lossy) as dielectric.

The resonant frequency of the designed antenna is calculated below:

Height (h) = 3.7 mm, width (w) = 37 mm, length (L) = 40 mm, relative permeability (ε_r) = 4.5

$$\varepsilon_{reff} = \frac{(\varepsilon_r + 1)}{2} + \frac{(\varepsilon_r - 1)}{2}\left[1 + 12\left(\frac{h}{w}\right)\right]^{\frac{-1}{2}} \tag{1}$$

$$\varepsilon_{reff} = 3.762$$

$$\Delta L = 0.412 * h\frac{(\varepsilon_{reff} + 0.3)}{(\varepsilon_{reff} - 0.258)}\left[\frac{\frac{w}{h} + 0.264}{\frac{w}{h} + 0.8}\right] \tag{2}$$

$$\Delta L = 1.679$$

$$\begin{aligned} L_{eff} &= L + 2\Delta L = 40 + 2 * 1.669 \\ L_{eff} &= 43.359 \end{aligned} \tag{3}$$

Substituting the values of (1), (2), (3) in below equation, we get

$$f_r = \frac{1}{2L_{eff}\sqrt{\varepsilon_{eff}\mu\varepsilon}}$$

$$f_r = 3.28\,\text{GHz}$$

4 Performance Characteristics

In this section, the characteristics of VSWR, gain parameter, and far-field patterns are discussed and are graphically represented. A feed is given to the patch antenna of about 2–10 GHz and an output gain of −74.74 dB is obtained at frequency of 3.28 GHz. Also VSWR = 1.0003 is obtained at the same frequency (Figs. 4 and 5).

The characteristics of an antenna can be accurately delineated on either a near-field range or far-field range with appurtenant accomplishment. Cost, size, and

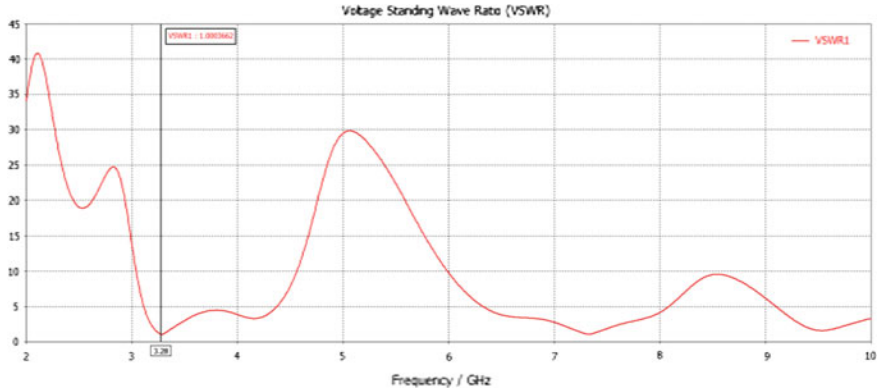


Fig. 4 VSWR characteristics

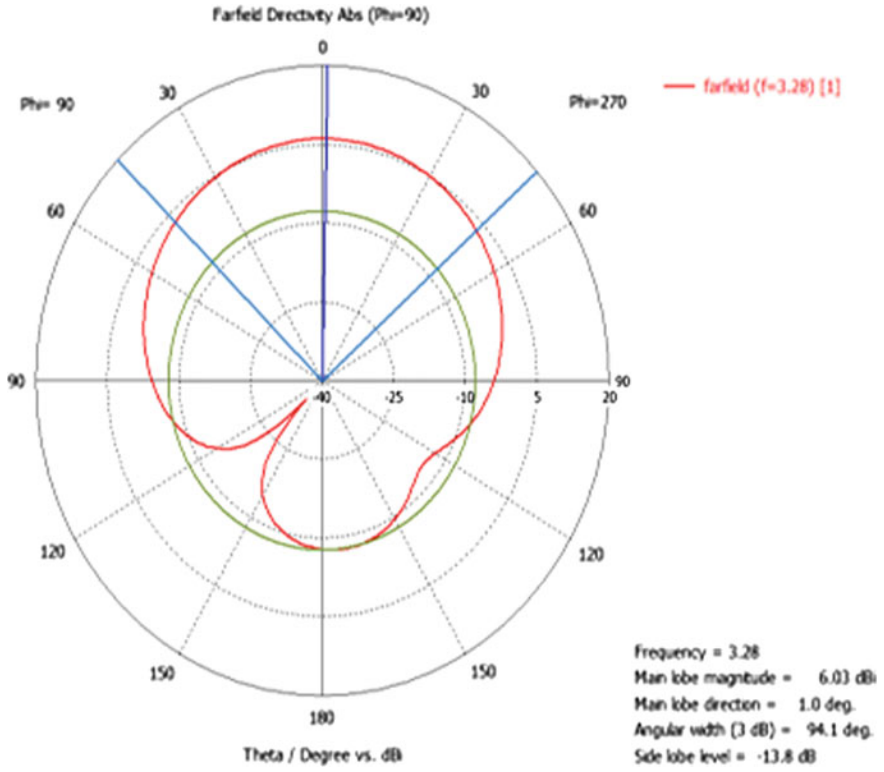


Fig. 5 Far-field pattern

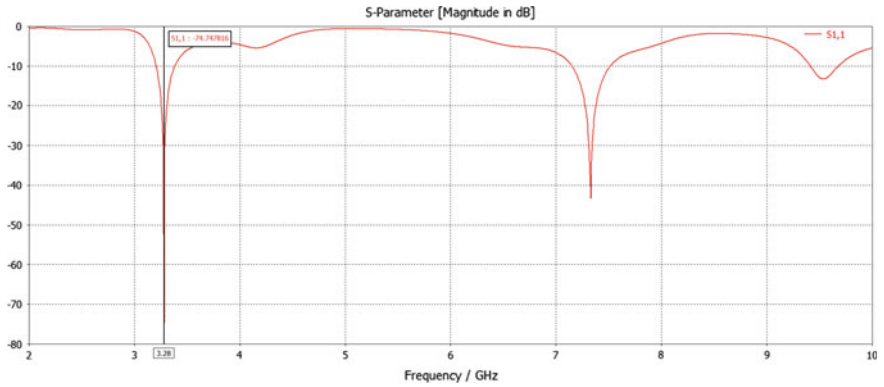


Fig. 6 S11 parameter (Gain)

efficiency are the most important which recommends one model over the other in any electrical application [8]. Moreover, there may be lack of symmetry at outrageous frequency levels due to radiating elements in the anatomy of antenna. Far-field radiation patterns of Micro-Strip Antenna for FR-4 (lossy) as a substrate is inspected because they have an acceptable return loss curves when compared to use of other substrates in combination with this antenna structure [9].

Radiation pattern is a ratio of gain to that of the direction. Usually, this ratio is expressed in decibels and hence gain is expressed in dB in above graph [10].

In Fig. 6, we can observe that the gain of the Micro-Strip Antenna is −74.74 dB at a frequency of 3.28 GHz in CST Microwave STUDIO 2014 environment.

5 Conclusion

It is shown that multi-band characteristics are attained for carved compact rectangular Micro-Strip Antenna by the use of a feed line with E-shaped strip. FR4-lossy is used as a substrate, copper as a ground plane, for the confined dimensions. The E-shaped micro-strip and slot dimensions with substrate thickness of 3.5 mm and a resonant frequency of 3.28 GHz are the most predominantly depicted parameters that determine the characteristics of the antenna such as VSWR = 1.0003 and gain = −74.74 dB. Simulated results have affirmed multi-band characteristics of the proposed antenna as well as nearly Omni-directional radiation properties over major parts of the operating bandwidth. These properties and their compact proportions make Micro-Strip antenna more attractive for inexhaustible wide band exercises.

References

1. Garg, Ramesh. Microstrip antenna design handbook. Artech house (2001)
2. Chandrasekhar, P., P. Gowtham Kumar, and K. Santhosh. "Study on Fractal Microstrip Fork Antenna with Enhanced Directivity." International Journal of Application or Innovation in Engineering & Management (IJAIEM) 4.3: pp 80–84, (2015)
3. Pozar, David M., and Daniel H. Schaubert. "Microstrip antennas: the analysis and design of microstrip antennas and arrays." John Wiley & Sons, (1995)
4. Eugene F. Knott, John F. Shaeffer, Michael T. Tuley, "Radar Cross Section", 2 Edition, SciTech Publishing, (2004)
5. Chandrasekhar, P., and T. Sree Hari. "Study of compact ultra wide band printed elliptical slot antenna." 2014 Annual IEEE India Conference (INDICON). IEEE, (2014)
6. Lo, Y. T., D. Solomon, and W. Richards. "Theory and experiment on microstrip antennas." IEEE Transactions on Antennas and Propagation 27.2: 137–145, (1979)
7. Schaub, Keith B., and Joe Kelly. Production Testing of RF and System-on-a-chip Devices for Wireless Communications. Artech House, (2004)
8. Kumar, P. Gowtham, P. Chandrasekhar, and K. V. R. S. Santhosh. "Study on Dual Band Double Layered Substrate Microstrip Fork Antenna."
9. Pozar, David M. "Microstrip antenna aperture-coupled to a microstripline." Electronics letters 21: 49, (1985)
10. Bancroft, Randy. Microstrip and printed antenna design. The Institution of Engineering and Technology, (2009)

Analog Fault Model for Biquad Filter by Using Distance Method

Gurunadha Ravva and K. Babulu

Abstract In this paper, a simple shortcoming model for a CMOS exchanged capacitor low-pass channel is tried. The Switching capacitor (SC) model is characterized as macros. These play some potential role as they incorporate some circuits and circuit elements like OPAMP, switches, and capacitors. The circuit is distinguished as flawed if the recurrence reaction of the exchange capacity does not meet the configuration detail. Several models are proposed to estimate the capacity of the circuit under test (CUT). A CMOS exchanged capacitor low-pass channel for sign recipient applications is picked as a case to exhibit the testing of the simple shortcoming model. To find out error is to calculate EIGEN values and EIGEN vectors are to detect the error of each component and parameters.

Keywords CMOS · SC · CUT · EIGEN · OPAMP · SFG

1 Introduction

It is always a difficult task to design of an analog circuit fault models. The possible reason being the simulation time or the assumptions derived. The analog faults are further categorized into hard and soft faults. The soft or parametric faults are due to variance of designated valued passive Components like resistance and capacitance. Similarly, the hard fault (HF) refers to short or open circuits. The SCs have become

G. Ravva (✉)
Department of ECE, JNTUK-UCEV, Vizianagaram, Andhra Pradesh, India
e-mail: gururavva@gmail.com

K. Babulu
Department of ECE, JNTUK, Kakinada, Andhra Pradesh, India
e-mail: kapbbl@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_32

the constituent part of several CMOS circuits. The SC inherently possesses several merits like excellent linearity with a wide range. In addition, it also preserves specific frequency tuning. In the recent past, a variety of AFM is proposed which is based on static linear behavior. The efficiency of the model is that, it is capable of handling both the parametric as well as catastrophic faults. Hence, it is capable of dealing with the faults persisting with the OP-AMPS, switches and the capacitors of the cut. However, the multi-fault models are more complexed than conventional fault model. The multi-fault models typical involves in using enhanced number of switches.

To minimizing the number of switches in a circuit the switch sharing technique is used and to improve the filter characteristics two methods are used dynamic range scaling and minimum capacitor scaling.

In this paper is organized as follows. Section 2 discusses the SFG's that are helpful in SLB fault model. Section 3 depicts the analysis that was made on the CUT, fault injections and their results are shown Sect. 4. Depicts the switched capacitor common mode feedback circuit description and finally conclusion from obtained results in Sect. 5.

2 Static Linear Behavior Fault Model

There are several parameters that contribute to faultiness of CUT. For a given OPAMP, the open loop gain should have minimum specifications and the offsets have the largest specification.

Capacitors: Ratio of the capacitors to the corresponding feedback circuit capacitance in the CUT.

Switches: Delayed switched capacitor branch and the delay free switched capacitor branch contain the switches have an additional fault.

The schematic circuit is drawn as shown in Fig. 1.

The specifications of the circuit are clock frequency of 6.144 MHz and band pass from 0 to 20 kHz, and band attenuation is higher than 40 dB and pass band ripple is <1 dB the remaining specifications are summarized in Table 1.

The signal flow graph corresponding to Fig. 1 is shown in Fig. 2.

3 Fault Injection

The schematic of the fault injection aided SC biquad is as shown in Fig. 3. The corresponding CUT is similar to the design which depicts a differential circuit. The circuit inherently possesses immunity to noise. The simulation was done on

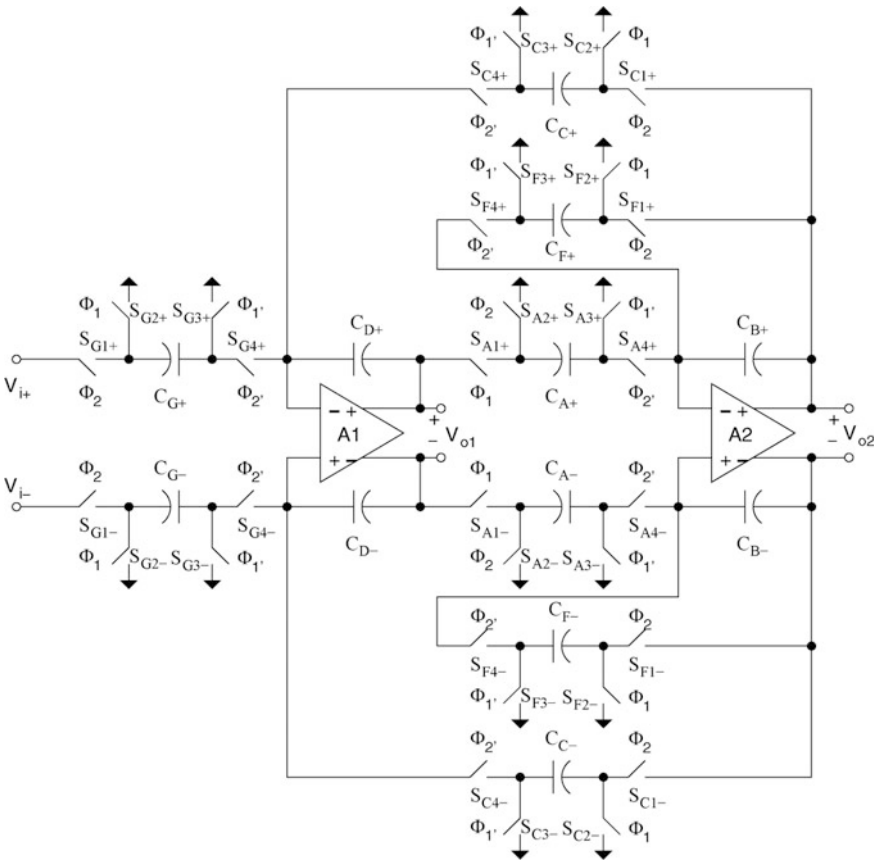


Fig. 1 SC Biquad filter

Table 1 Parameters of the switched capacitor circuit

Parameter	Specification values
C_A	1.706 pF
C_B	3.293 pF
C_C	1.706 pF
C_D	1 pF
C_F	3.259 pF
C_G	1.011 pF
A1	80 dB
A2	80 dB

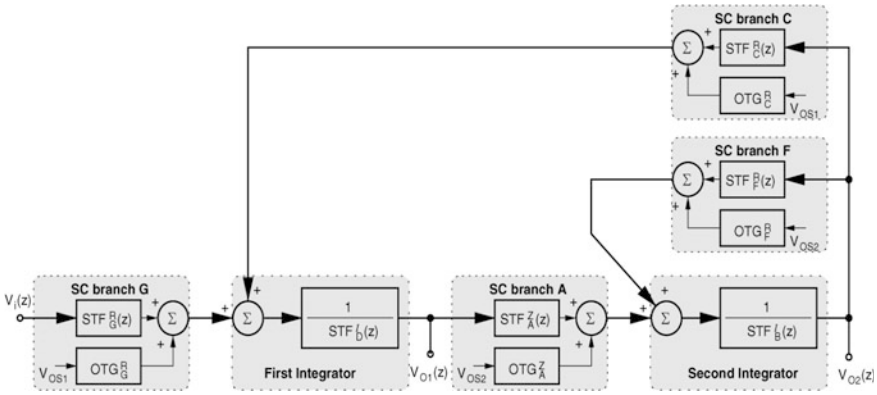


Fig. 2 Signal flow graph of the CUT

0.35 μm CMOS technology available in Mentor Graphics. Conventional folded cascode topology is used for implementing the Op-Amps. The design values of the capacitors in the fault injected CUT are given in Table 2.

In its general form, the SC biquad structure can be understood as a low-pass butterworth filter. The corresponding filter typically possesses pass band of 20 kHz. While, the stop band is 400 kHz with typical attenuation features of 30 dB.

Several switches namely SGs, SHs, and SGo are used to learn the effects of the SLB fault model incorporated in the block. It is clear from the basic schematic that the corresponding aspect ratios of the switches incorporated should be large enough comparatively with those of other switches like SGn and SHn. From the circuit, it can be learned that these switches are exists in parallel.

By keeping SGs or SHs turn-on, a short fault is injected to the corresponding switch. The design allows injecting a stuck-open fault to the biquad, too. The switch SGo can be turn off for injecting the stuck-open fault.

4 Simulated Results

It is in general to employ a three tone test for the analog circuits. For this purpose, it is suggested to use a typical three different tone generator for testing purpose. The three tone frequencies cover low frequency, high frequency as well as a corner frequency. Considering this, the determined frequencies for consideration are 22, 51 and 398 kHz. The simulation carried out using tanner 0.25 μm technology. The results pertaining to second and fifth order biquad filters are given in this section. The schematic of second order low pass is as shown in Fig. 4. The corresponding

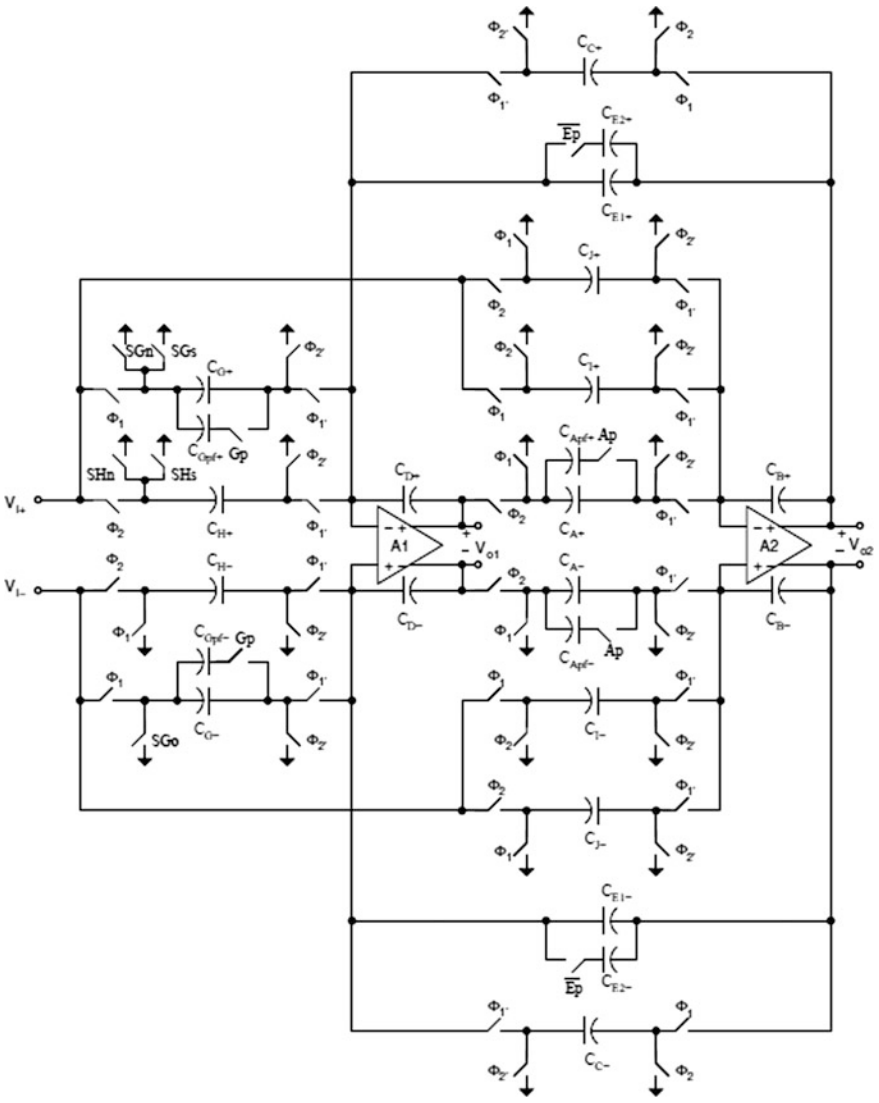


Fig. 3 Fault injected schematic [1]

Table 2 Results of distance method in biquad filter

Faults	$D_{F(VOUT)}$		$MD_{(VOUT)}$	
	VO_1	VO_2	VO_1	VO_2
Fault free	0.9162	2.2617	4.213	1.4718
NMOS 2	1.84889		14.1119	
NOMS 6	2.7028		47.8269	
Capacitor short	1.9294		**1.3048**	
Capacitor ground	1.1302		**0.8528**	

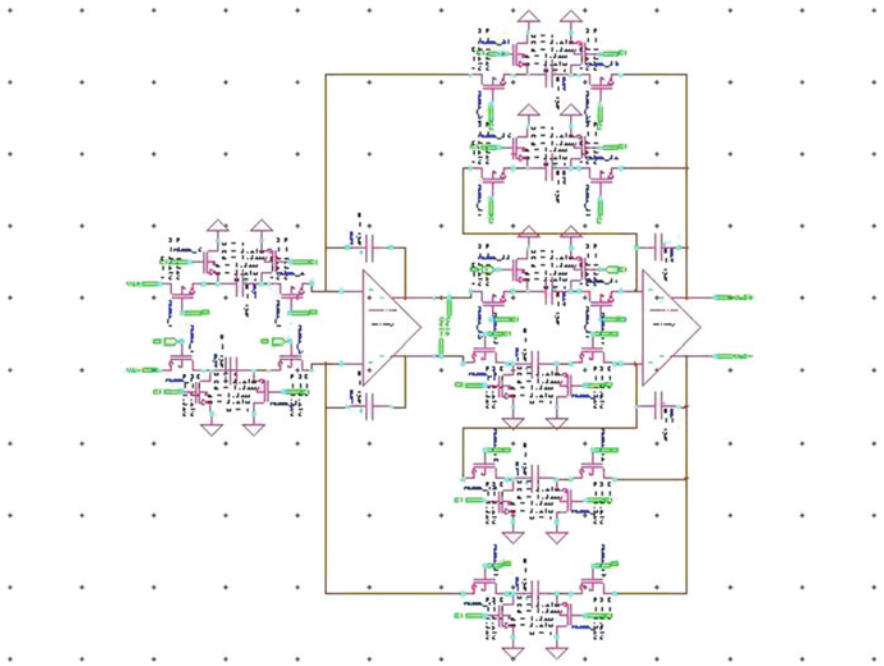


Fig. 4 Biquad filter using second order low-pass filter

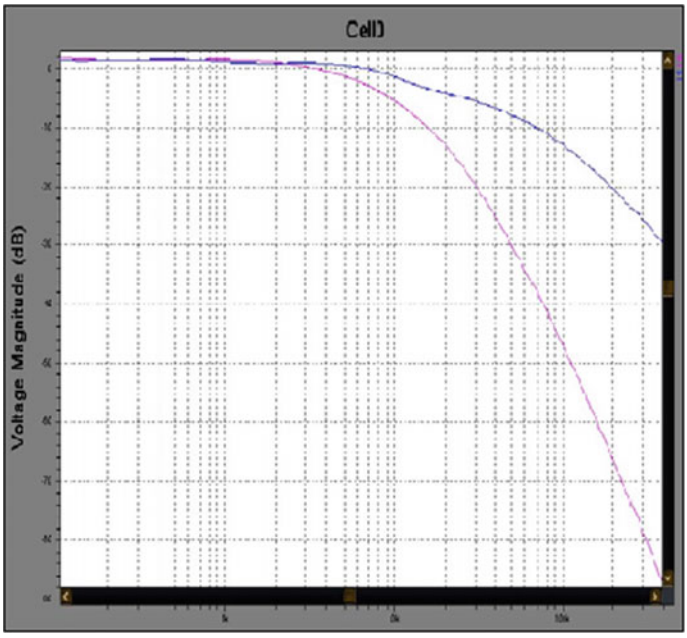


Fig. 5 Frequency response of biquad filter in second order filter

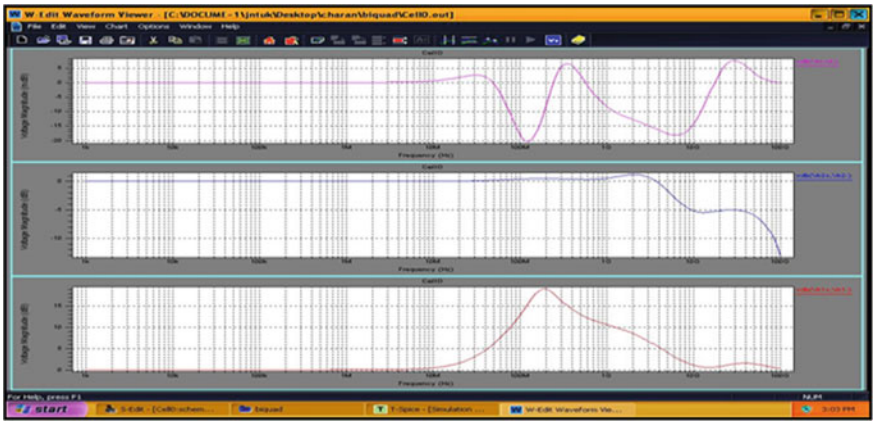


Fig. 6 Biquad filter output of without injecting any fault

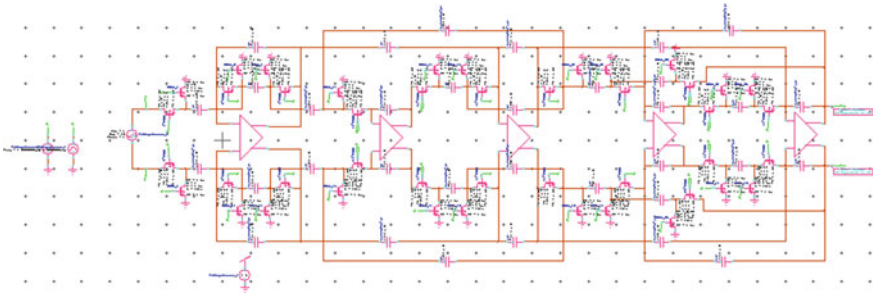


Fig. 7 Schematic view of fifth order SC low-pass filter

frequency response is as shown in Fig. 5. The response without injecting any fault is as shown in Fig. 6. Figure 7 represents the schematic view of fifth order low-pass filter. Figure 8 shows the simulation results of the CUT during the injection of the fault. As a result of this injection model, the respective gain in the band gets attenuated with the CUT. The accuracy of the TF remains unaltered even with the failure of the CUT. Yet, the estimated TFs successfully depict the faulty frequency responses of the CUT. The corresponding frequency response of the LPF can be learned from the Fig. 13. Also, it is clear that the pass band frequency of 8 MHz. Similarly, the pass band ripple is <1 dB, 80 MHz clock frequency at the supply voltage of 1.8 V. The corresponding band attenuation is typically greater than 40 dB.

Similarly, the schematic of fifth order biquad filter is given in Fig. 7. Experimental results pertaining to injecting parametric fault C_{GPF}, A_p, E_p, are given in Figs. 8, 9, and 10, respectively. Similarly, the results corresponding to switch SH_s and SG_o are given in Figs. 11 and 12, respectively.

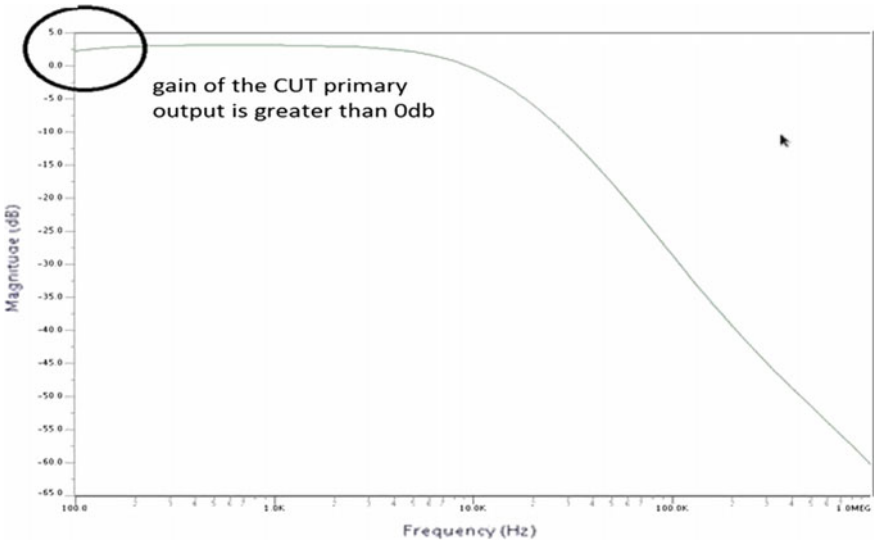


Fig. 8 Performance with the fault injection (C_{Gpf})

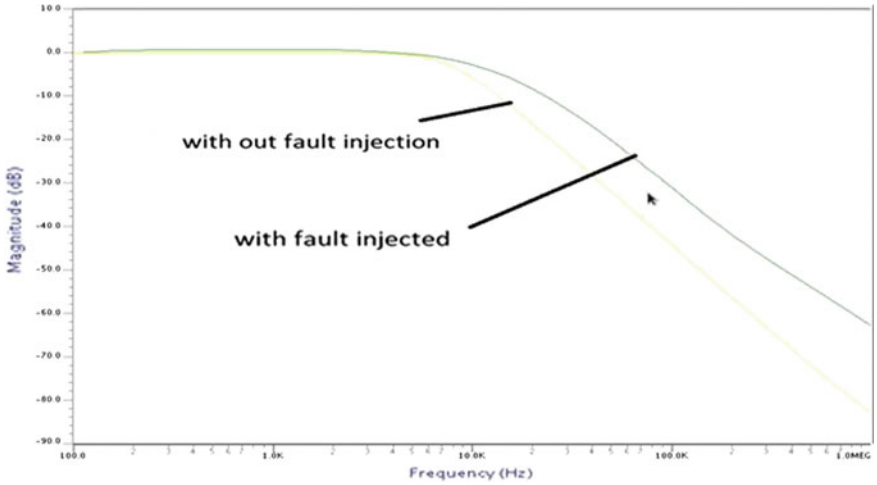


Fig. 9 Performance with the fault injection (Ap)

The frequency response is as shown in Fig. 13.

The corresponding Wavelet-Based Distance Method Results are given in Table 2. This result shows the coefficients of distance method in biquad filter circuit.

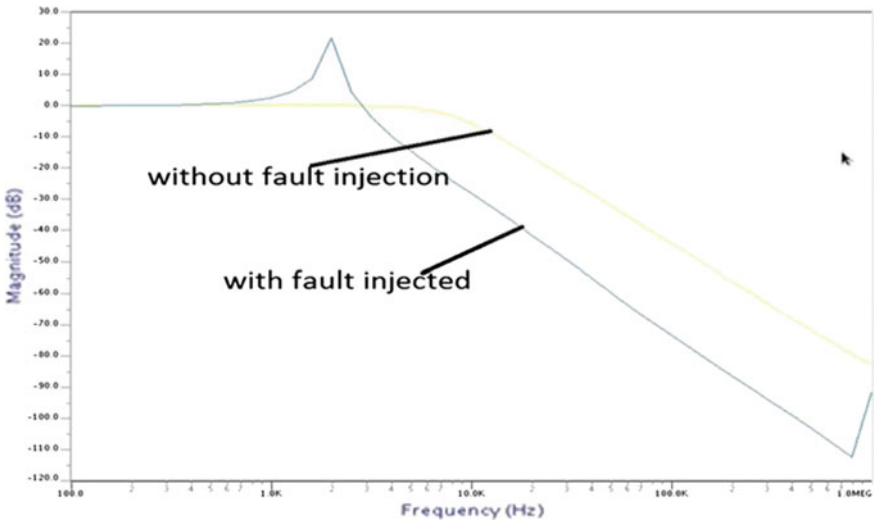


Fig. 10 Performance with the fault injection (Ep)

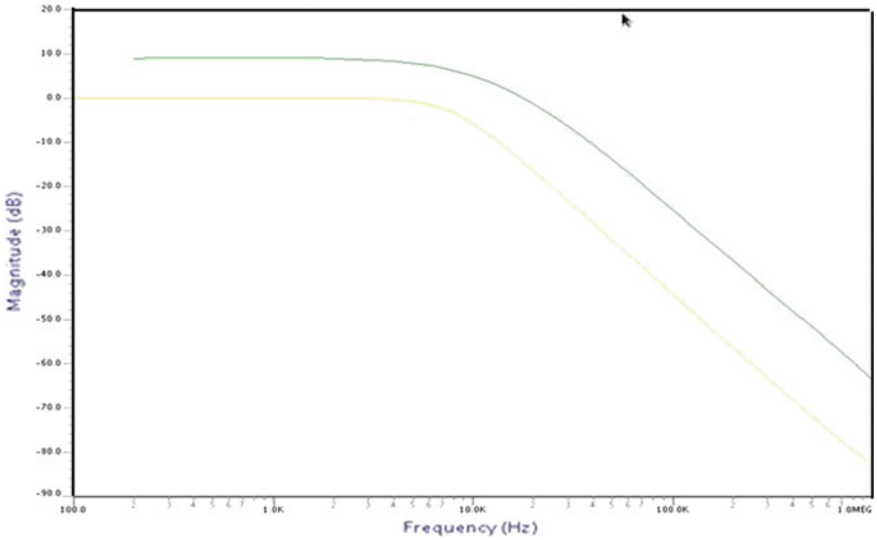


Fig. 11 Performance evaluation with switch SHs is short

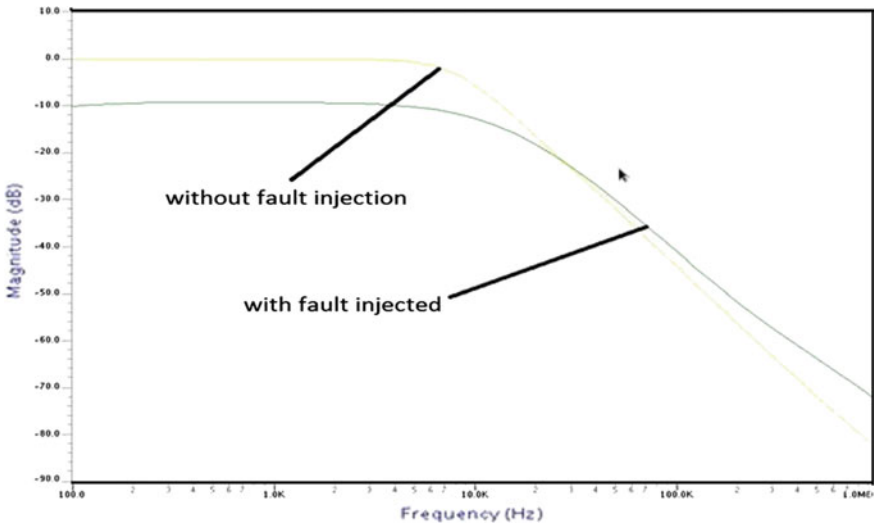


Fig. 12 Performance evaluation switch SGo is open

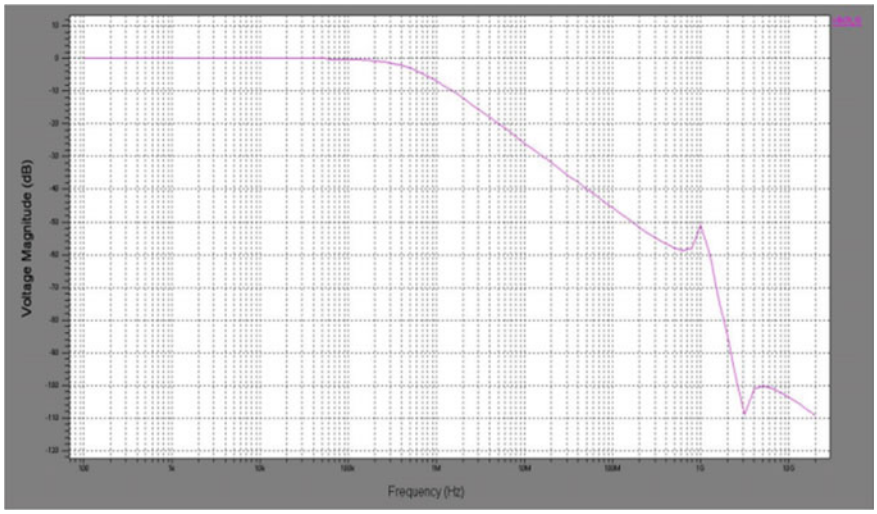


Fig. 13 Frequency response of the SC low-pass filter

5 Conclusion

In this paper, the SLB simple shortcoming model for straight SC circuits is been checked and a SC low-pass biquad channel is taken as a case to show the adequacy of the SLB issue model. We lead with different stimulus tones and check if the test reactions fit in those anticipated by the recovered TF. Trial results check that the settled TF layout supposition holds for every one of the issues that we infused. Extending the shortcoming model to incorporate the planning related deficiencies would be a fascinating subject for the future exploration work.

References

1. Long-Yi Lin., Hao-Chiao Hong.: Design of a Fault-Injectable Fleischer-Laker Switched-Capacitor Biquad for verifying the Static Linear Behavior Fault Model. 22nd Asian Test Symposium, (2013)

Segmentation and Analysis of Brain Tumor Using Tsallis Entropy and Regularised Level Set

V. Rajinikanth, Steven Lawrence Fernandes, Bharath Bhushan, Harisha and Nayak Ramesh Sunder

Abstract Image processing is extensively considered in medical field for computer-supported disease assessment. Brain tumor is one of the deadliest cancers for the human community and requires image/signal processing approaches to record and analyze the disease-affected regions. In this work, Cuckoo Search Algorithm (CA) assisted approach is proposed to segment tumor from a two-dimensional Magnetic Resonance Image (MRI). Primarily, Tsallis entropy-monitored multilevel thresholding is implemented for the brain MRI dataset based on CA. Afterward, the skull section is detached by means of an image filtering approach. The skull stripped image is then treated using the image morphological function in order to obtain a smooth image exterior. Lastly, the tumor section is mined using the regularized level set technique. The efficiency and the clinical importance of presented method are confirmed based on the image similarity measures and the statistical measures. Experimental results of the proposed approach offer better values of Jaccard, Dice, precision, sensitivity, and accuracy values. Hence the proposed approach is clinically significant and in future, it can be used to diagnose the brain tumor images.

Keywords Brain MRI · Cuckoo search · Tsallis entropy · Level set segmentation

V. Rajinikanth (✉)
Department of Electronics & Instrumentation Engineering, St. Joseph's College of Engineering, Chennai, Tamil Nadu, India
e-mail: rajinikanthv@stjosephs.ac.in

S.L. Fernandes
Department of Electronics & Communication Engineering, Sahyadri College of Engineering & Management, Mangalore, Karnataka, India

B. Bhushan · Harisha
Department of Computer Science & Engineering, Sahyadri College of Engineering & Management, Mangalore, Karnataka, India

N.R. Sunder
Department of Information Science & Engineering, Canara Engineering College, Mangalore, Karnataka, India

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_33

1 Introduction

Computer-aided disease examination is widely used in medical discipline to investigate anatomical and pathological sections from clinical images. Medical imaging procedures will support the early detection and diagnosis of various diseases and also help to reduce the morbidity and mortality rates.

In the literature, a number of procedures are proposed and implemented by the researchers to extract significant information from the traditional and medical images [1–3]. The heuristic algorithm-assisted image segmentation is widely considered in recent years because of its simplicity and easiness in implementation. Otsu's function and heuristic algorithm-assisted multi-thresholding procedure for breast thermal images [4], brain region segmentation based on heuristic algorithm-guided Otsu's multi-level thresholding, and Markov random field [5] are some recent works in the medical image segmentation. Recently, Despotovic et al. discussed about the segmentation challenges and method existing for the 2D and 3D brain images and concluded that combination of several techniques is essential to achieve better segmentation [6].

This paper proposes a computer-aided segmentation methodology to extract the tumor from the 2D brain MRI database. Initially, global thresholding scheme based on the Tsallis entropy is considered to enhance the tumor region in the brain MRI. Tsallis entropy criterion was initially proposed in 1988 and is a non-extensive statistical approach, being typically adopted in image processing applications [5]. The combination of Tsallis function and various heuristic algorithms have been presented over the past years for image thresholding applications [1]. In this paper, the cuckoo algorithm (CA)-assisted Tsallis entropy-based global thresholding is employed. Later, visual appearance of the multi-level threshold image is improved using traditional morphology operation. Finally, level set approach-based segmentation procedure is adopted to divide the input image into various clusters. Level set is a well-known segmentation approach, and works well on images with various uncertainties, such as noise, degradation, imprecise information, and partial data [7, 8].

The efficiency of proposed segmentation methodology is confirmed with a relative examination between the segmented tumor region and the ground truth image. The result authenticates that proposed approach is efficient in obtaining the better image similarity index values [9] and statistical measure values [10].

2 Methodology

This work focuses on developing the heuristic algorithm-assisted tool to segment the tumor section from 2D MRI images recorded using various modalities. The proposed work is segregated as the preprocessing and post-processing section. The preprocessing stage is considered to enhance the tumor region of the brain MRI image. In this stage,

the following operations are performed: heuristic algorithm-guided multi-level thresholding and skull stripping to remove the high intensity region of the MRI image, such as the skull region and morphological operation to smooth the intensity levels of the thresholded brain MRI image. In post-processing stage, level set segmentation is adopted to extract the tumor section.

2.1 Tsallis Entropy

In general, the entropy is related with the measure of chaos within a system. Shannon primarily considered the entropy to compute the uncertainty regarding the information content of the system [1]. Shannon also assured that, when a physical system is separated as two statistically free subsystems A and B, the entropy value can be expressed as

$$S(A+B) = S(A) + S(B). \tag{1}$$

Based on Shannon's theory, a non-extensive entropy concept was proposed by Tsallis and defined as

$$S_q = \frac{1 - \sum_{i=1}^{T} (p_i)^q}{q-1}, \tag{2}$$

where T is the system potentials and q is the entropic index.

Equation (2) will meet the Shannon's entropy when $q \to 1$.

The entropy value can be expressed with a pseudo-additivity rule as

$$S_q(A+B) = S_q(A) + S_q(B) + (1-q).S_q(A).S_q(B). \tag{3}$$

Tsallis entropy can be considered to find the optimal thresholds of an image. Consider a given image with L gray levels in the range $\{0, 1, \ldots, L-1\}$, with probability distributions $p_i = p_0, p_1, \ldots, p_{L-1}$.

Tsallis multi-thresholding can then be expressed as

$$f(T) = [T_1, T_2, \ldots, T_k] = argmax$$

$$\left[S_q^A(T) + S_q^B(T) + \cdots + S_q^K(T) + (1-q).S_q^A(T).S_q^B(T) \ldots S_q^K(T)\right], \tag{4}$$

where

$$S_q^A(T) = \frac{1 - \sum_{i=0}^{t_1-1} \left(\frac{Pi}{P^A}\right)^q}{q-1},\ P^A = \sum_{i=0}^{t_1-1} Pi$$

$$S_q^B(T) = \frac{1 - \sum_{i=t_1}^{t_2-1} \left(\frac{Pi}{P^B}\right)^q}{q-1},\ P^B = \sum_{i=t_1}^{t_2-1} Pi$$

$$S_q^K(T) = \frac{1 - \sum_{i=t_k}^{L-1} \left(\frac{Pi}{P^K}\right)^q}{q-1},\ P^K = \sum_{i=t_k}^{L_2-1} Pi.$$

The aim of multi-level thresholding process is to find the optimal threshold (T) which maximizes $f(T)$. In the proposed work, the threshold value is chosen as $T = 3$, and thus the required probability values are P^A, P^B, and P^C.

2.2 Cuckoo Algorithm

Cuckoo algorithm (CA) was initially proposed in 2009, based on the mimic of breeding tricks followed by the parasitic cuckoos [11]. Because of its capability, CA was adopted to solve a variety of image multi-thresholding problems [12].

The mathematical equation of the CA adopted in this work is presented below:

$$X_i^{(t+1)} = X_i^{(t)} + \alpha \oplus Levy(\lambda), \tag{5}$$

where $X_i^{(t)}$ is the early location, $X_i^{(t+1)}$ is the updated location, α is selected as 1.2, and ⊕ is the sign for entry-wise multiplication.

The Levy flight directed search is considered to update the position of the CA using the following Levy distribution:

$$Levy \sim u = t^{-\lambda} \quad \text{for} \quad (1 < \lambda \leq 3). \tag{6}$$

In this paper, optimization exploration based on CA is adopted to find the best possible thresholds with the aid of Tsallis entropy.

2.3 Skull Stripping

Skull stripping is necessary to eliminate the skull and the background area from MRI for quantitative analysis. Skull stripping is normally performed using an image filter which separated the skull and the rest of the image sections by masking the pixels having similar intensity levels. In brain MRI, the skull/bone section will have the maximum threshold value (threshold > 200) compared to other brain regions.

Hence, the image filter is considered to divide the brain region based on a chosen threshold value. Then by employing the solidity property, the skull is stripped from the test image [9].

2.4 Morphological Operation

Morphological operation is usually used in image processing application to improve the visual appearance. In this paper, line-based structuring element (*strel*) and image fill (*imfill*) are considered to enhance the edges and appearance of multi-threshold and skull-stripped brain image. This morphological operation enhances the suspicious regions and supports faster segmentation during the post-processing operation.

2.5 Level Set

Level set approaches have been extensively used in image segmentation applications. The level set (LS) procedure was initially developed in 1990s [13–15].

The proposed work implements the recent version of LS methodology to segment the tumor region from 2D brain MRI database [16, 17].

The chosen LS approach can be mathematically expressed as follows:

$$\text{Let the curve evolution is} = \frac{\partial C(s,t)}{\partial t} = FN, \tag{7}$$

where C is the curve vector with the spatial parameter (s) and temporal variable (t), F is the speed function, and N is the inmost normal vector to the curve C.

More details regarding the chosen LS function in this work can be found in [15].

2.6 Tumor Analysis

In this paper, MRI datasets, such as with and without skull sections, are considered. For both the cases, the segmented tumor mass is analyzed using a comparative study with the expert's ground truth image. First, the image similarity measures, such as Jaccard index (JI), Dice coefficient (DC), false positive rate (FPR), and false negative rate (FNR), are computed [9]. Further, the image statistical measures, such as precision, F-measure, sensitivity, specificity, balanced classification rate (BCR), balanced error rate (BER), and accuracy are also computed [10].

3 Result and Discussions

This section presents the experimental results of the proposed work. The initial CA parameters are assigned as follows: Number of agents (N) = 15; dimension of search = $T = 3$; iteration number (t) = 1000; and stopping criteria = $f(T)_{max}$ [13]. The proposed approach is initially implemented on a 256 × 256 sized, horizontally registered brain MTI dataset. During the study, 2D slices of the dataset (slice number 40, 45, 50, 55, and 60) are considered for investigation. Figure 1 depicts the MRI brain tumor test image considered for the study. Figure 1b, c shows the brain region and tumor region, respectively. Figure 1 d–g depicts the outcome of the preprocessing work and Fig. 1h and i presents the outcome of the post-processing operation. Similar procedures are considered for the other slices of test image (slice45 to slice60) and the results are presented in Table 1.

The extracted tumor region is then compared with the ground truth in order to confirm the clinical significance. Table 2 depicts results obtained for other slices. Similar procedure is repeated on 216 × 160 sized brain tumor image segmentation (BraTS) dataset recorded using the Flair and T2 modalities [16–18].

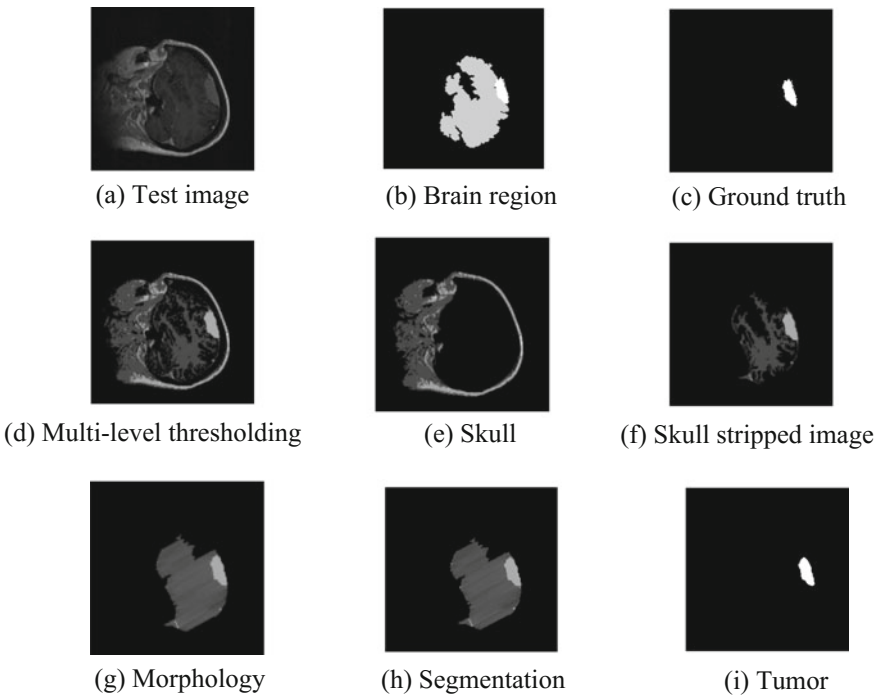


Fig. 1 Segmentation result for slice40

Table 1 Segmentation results for MRI database

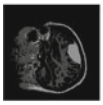
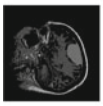
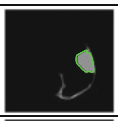
	Threshold image	Skull stripped image	Segmentation	Tumor
Slice45				
Slice50				
Slice55				
Slice60				

Table 2 Test image and ground truth of BraTS dataset

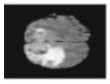
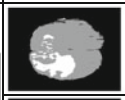
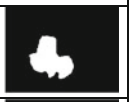
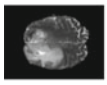
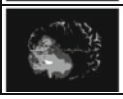
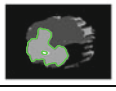
Test Image		Ground truth	Threshold image	Morphology	Segmentation	Tumor
$\mathbf{Flair}_{120}$						
$\mathbf{T2}_{120}$						

Table 2 shows the chosen test images (slice number 120) and preprocessing and post-processing section results. From this table, it can be noted that proposed approach offers better result on Flair and T2 modality-based MRI dataset.

The efficiency of segmentation procedure is analyzed using the well-known image quantitative measures, such as image similarity index and statistical measures. Table 3 demonstrates that, in all the image cases, the segmented tumor image is closely correlated with the ground truth image and the average JI and DC are found to be greater than 0.8.

Table 4 confirms that proposed approach helps to attain better values of precision, F-measure, sensitivity, specificity, BCR, BER, and accuracy. These results prove that the proposed segmentation work offers better results for 2D brain MRI

Table 3 Relative result between ground truth and segmented tumor

Image	JI	DC	FPR	FNR
Slice40	0.8435	0.9151	0.1731	0.0105
Slice45	0.8728	0.9321	0.1457	0.0000
Slice50	0.8017	0.8899	0.2440	0.0027
Slice55	0.8124	0.8965	0.2309	0.0000
Slice60	0.6667	0.8000	0.4715	0.0190
$Flair_{120}$	0.8515	0.9198	0.0905	0.0715
$T2_{120}$	0.8876	0.9405	0.0490	0.0689

Table 4 Statistical measure values

Image	Precision	F-measure	Sensitivity	Specificity	BCR	BER	Accuracy
Slice40	0.9999	0.9992	0.9985	0.9895	0.9940	0.6007	0.9940
Slice45	1.0000	0.9986	0.9973	1.0000	0.9987	0.1344	0.9987
Slice50	0.9999	0.9971	0.9943	0.9973	0.9958	0.4191	0.9958
Slice55	1.0000	0.9976	0.9952	1.0000	0.9976	0.2375	0.9976
Slice60	0.9997	0.9964	0.9931	0.9810	0.9870	1.2954	0.9870
$Flair_{120}$	0.9911	0.9899	0.9887	0.9285	0.9586	4.1379	0.9581
$T2_{120}$	0.9914	0.9926	0.9939	0.9311	0.9625	3.7488	0.9620

recorded with various modalities. This confirms that the proposed approach is very efficient in extracting the tumor mass from the brain MRI dataset and this approach is clinically significant.

4 Conclusion

In this paper, segmentation and analysis of brain tumor is demonstrated by considering 2D brain tumor MRI dataset. It is an automated procedure and effectively extracts the tumor mass from the MRI dataset obtained using various modalities, such as T2 and Flair. In order to authenticate the superiority of the proposed approach, extracted tumor region is compared with the ground truth. Experimental result confirms that proposed approach offers better results for the image similarity index values and the statistical measure values. Hence, the proposed work is extremely significant for the segmentation of brain MRI image and can be used as the automated screening tool for the brain MRI-related diseases.

References

1. Bhandari, A.K., Kumar, A. and Singh, G.K: Modified artificial bee colony based computationally efficient multilevel thresholding for satellite image segmentation using Kapur's, Otsu and Tsallis functions, Expert Systems with Applications, vol.42, no.3, pp. 1573–1601, (2015).
2. Rajinikanth, V., Raja, N.S.M. and Satapathy, S.C: Robust color image multi-thresholding using between-class variance and cuckoo search algorithm, Advances in Intelligent Systems and Computing, vol. 433, pp. 379–386, (2016).
3. Satapathy, S.C., Raja, N.S.M., Rajinikanth, V., Amira S. Ashour. and Nilanjan Dey: Multi-level image thresholding using Otsu and chaotic bat algorithm, Neural Computing and Applications, doi:10.1007/s00521-016-2645-5, (2016).
4. Raja, N.S.M., Sukanya, A. and Nikita, Y: Improved PSO based multi-level thresholding for cancer infected breast thermal images using Otsu, Procedia Computer Science, vol.48, pp. 524–529, (2015).
5. Tsallis, C: Possible generalization of Boltzmann-Gibbs statistics, Journal of Statistical Physics, vol.52, pp. 479–487, (1988).
6. Despotovic, I., Goossens, B. and Philips, W: MRI Segmentation of the human brain: Challenges, Methods, and Applications, Computational and Mathematical Methods in Medicine, vol. 2015, Article ID 450341, pp. 23, (2015).
7. Lu, H., Kot, A.C. and Shi, Y.Q: Distance-reciprocal distortion measure for binary document images, IEEE Signal Processing Letters, vol.11, no.2, pp. 228–231, (2004).
8. Malladi, R., Sethian, J.A. and Vemuri, B.C: Shape modeling with front propagation: A level set approach, IEEE Transactions on Pattern Analysis and Machine Intelligence, vol. 17, no.2, pp. 158–175, (1995).
9. Chaddad, A. and Tanougast, C: Quantitative evaluation of robust skull stripping and tumor detection applied to axial MR images, Brain Informatics, vol.3, no.1, pp. 53–61, (2016).
10. Moghaddam, R.F., & Cheriet, M. A multi-scale framework for adaptive binarization of degraded document images, Pattern Recognition, 43(6), pp. 2186–2198, 2010.
11. Yang, X. S., & Deb, S. Cuckoo search via Lévy flights. In: Proceedings of World Congress on Nature and Biologically Inspired Computing (NaBIC 2009), IEEE Publications, USA, pp. 210–214, (2009).
12. Raja, N.S.M. and Vishnupriya, R: Kapur's entropy and cuckoo search algorithm assisted segmentation and analysis of RGB Images, Indian Journal of Science and Technology, vol.9, no.17, pp. 89936, (2016).
13. Caselles, V., Catte, F., Coll, T. and Dibos, F: A geometric model for active contours in image processing, Numerische Mathematik, vol.66, no.1, pp. 1–31, (1993).
14. Glaister, J., Wong, A. and Clausi, D.A: Segmentation of skin lesions from digital images using joint statistical texture distinctiveness, IEEE Transactions on Biomedical Engineering, vol. 61, no.4, pp. 1220–1230, (2014).
15. Li, C., Xu, C., Gui, C. and Fox, M.D: Distance regularized level set evolution and its application to image segmentation, IEEE Transactions on Image Processing, vol.19, no.12, pp. 3243–3254, (2010).
16. Menze et al., The Multimodal Brain Tumor Image Segmentation Benchmark (BRATS), IEEE Transactions on Medical Imaging, vol. 34, no.10, pp. 1993–2024, (2015).
17. Brain Tumor Database (BraTS-MICCAI), http://hal.inria.fr/hal-00935640.
18. Palani, T.K., Parvathavarthini, B. and Chitra, K: Segmentation of brain regions by integrating meta heuristic multilevel threshold with Markov random field, Current Medical Imaging Reviews, vol.12, no.1, pp. 4–12, (2016).

A New Approach to Investigation of Discrete Wavelet-Based Multiuser MIMO-OFDM for BPSK Modulation Scheme

A. Vamsidhar, P. Rajesh Kumar and K. Raja Rajeswari

Abstract This paper investigates the approach of discrete wavelet to multiuser (MU) MIMO-OFDM systems and further makes a comparison with the conventional Fast Fourier Transform (FFT) founded MU-MIMO-OFDM. Discrete wavelet-based system is found superior in performance over the FFT based one, where the requirement of cyclic prefix has been eliminated making flexible with greatest selection. The concept of discrete wavelets is a best fit in all the areas of Wi-Fi verbal schemes with OFDM, which is an enduring application for subsequent users. Simulations were created for the double multicarrier schemes. Haar wavelet has been utilized in this paper since it shaded out the performance of its counterparts like Daubechies and Symlet. The proposed wavelet-based scheme superseded the conventional-based system in terms of Bit Error Rate (BER) taking a couple of antennas by means of BPSK and QPSK as dual modulation schemes over the Additive White Gaussian Noise (AWGN) Channel.

Keywords MU-MIMO-OFDM · DWT · Haar · BER · BPSK · AWGN

1 Introduction

An orthogonal frequency division multiplexing (OFDM) scheme is a multicarrier transmission approach, which is based on separating the available spectrum into orthogonal frequencies carrying information undistorted. The multipath propagation in the wireless networks always faces a greatest enemy of multipath fading,

A. Vamsidhar (✉)
Department of ECE, Dadi Institute of Engineering & Technology, Visakhapatnam, India
e-mail: vamsianagani@gmail.com

P. Rajesh Kumar · K. Raja Rajeswari
Department of ECE, College of Engineering, Andhra University, Visakhapatnam, India
e-mail: rajeshauce@gmail.com

K. Raja Rajeswari
e-mail: krrauce@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_34

occurring in both the frequency and spatial domains. This multicourse fading greatly diminishes the performance of an OFDM procedure. OFDM has very exact velocity skills premiums, and these knowledge premiums are splitted into wide variety of subcarriers. The FFT-headquartered common OFDM procedure is used to multiplex the alerts collectively and furthermore decode the received symbols via the receiver. The cyclic prefix is introduced earlier than the transmission of the data, to stay away from the Intersymbol Interference (ISI). The introduction of DWT into this arena greatly enhances the transmission efficiency over FFT method. The sub-band coding in discrete wavelet makes a redundancy in cyclic prefix, hence boosting up the channel efficiencies at a lower error rate.

A. *Binary segment shift keying*

In BPSK, the section of the sinusoidal service is modified in line with the info being transmitted. Symbol 0 or 1 modulates the provider.

Let the service sign accept by means of

$$s(t) = A\,Cos(2\pi f_c t) \tag{1}$$

Then

$$P = \frac{1}{2}A^2 \Rightarrow A = \sqrt{2P} \tag{2}$$

When a symbol is changed, the segment of the provider is modified.

Defining

$$s(t) = b(t)\sqrt{2P}Cos(2\pi f_c t) \tag{3}$$

with $b(t) = 1$ for binary '1' sent and $b(t) = 0$ for binary '0' sent.

Figure 1 suggests the symbols constellation, which clearly is the representation of the intricate envelope of the sign. The distance between the signals on the constellation determines how well the receiver can differentiate between all feasible symbols when the sign has been corrupted by way of noise or when noise is present [1]. The greater the distance, the simpler is the risk of proper symbol detection. The smaller the gap between the symbols, the bigger is the chance of the receiver failing

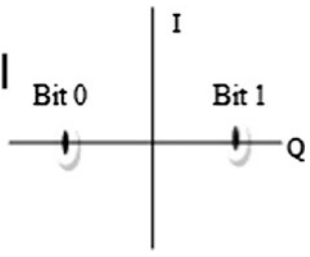


Fig. 1 BPSK constellation diagram

to differentiate between the received symbols which might be whether or not the bit is a 0 or a 1. Within the generation of BPSK alerts, the binary data stream is converted into an NRZ bipolar signal through an NRZ encoder. Then it is utilized to a product modulator whose output is the BPSK signal.

2 FFT Centered MU-MIMO-OFDM

MIMO (Multi-input Multi-output) strategies use many antennas at either the transmitter or receiver (array of antennas) in Wi-Fi communication systems [2]. First, MIMO approach broadly raises the channel potential, which is in proportion to the whole number of transmitter and receiver arrays. 2D MIMO procedure presents the capabilities of spatial style, each and everyone's transmitting sign is detected via the entire detector array, which was most powerful increased system robustness and reliability, however, in addition reduces the influence of ISI (intersymbol interference) and the channel fading, since the truth that every sign option is based on N detected outcome. In unique phrases, spatial sort over's N impartial replicas of transmitted sign. 1/3, the Array collect can also be multiplied, this means that SNR receive completed with the help of focusing vigour in desired course is multiplied. In contradiction, MIMO utilizes extra power at transmission process and increases the circuit power consumption.

The block diagram representation of Transmitter and Receiver of FFT-situated MIMO-OFDM is proven in Fig. 2 and Fig. 3 respectively. In the Transmitter block diagram, the input data is encoded and sent by means of the sign mapped. Then, it is handed via a space Time Block Coder (STBC) where the sign is splitted and inverse FFT is participated on the output of STBC. Look after Interval is introduced for the inversed modified sign as a way to hinder the channel interference and transmitted via multiple antennas. The receiver operation is relatively the reverse of transmitter operation.

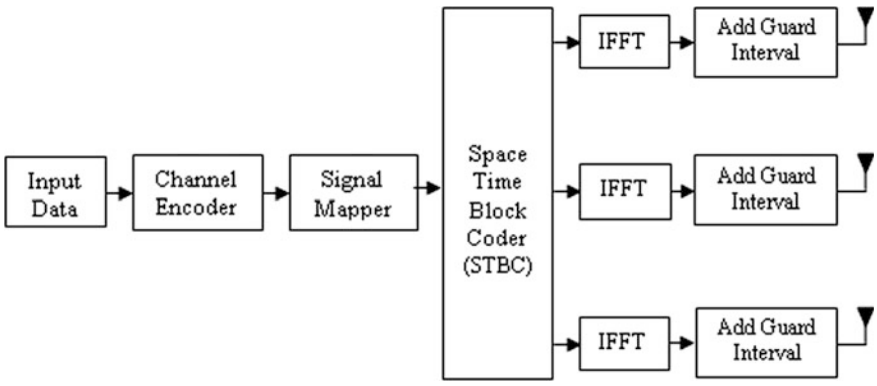


Fig. 2 Block diagram illustration of FFT situated MU-MIMO-OFDM Transmitter

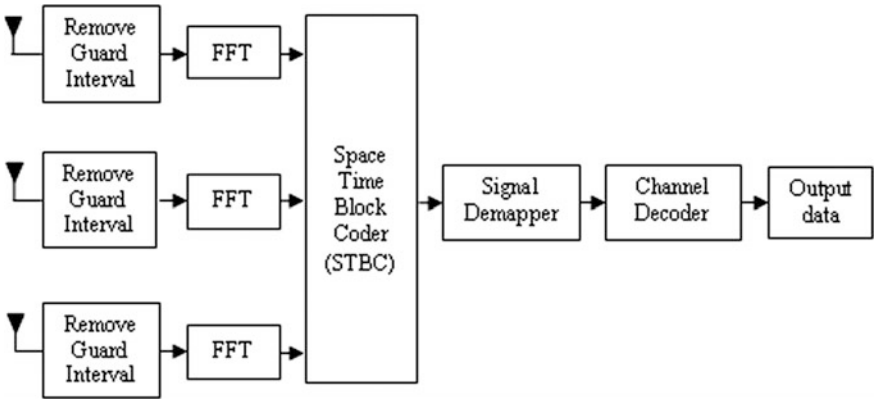


Fig. 3 Block diagram illustration of FFT situated MU-MIMO-OFDM Receiver

3 Wavelet Based MU-MIMO-OFDM

Wavelets developed as a predominant mathematical tool for multidecision continuous time sign differentiations with the help of quality frequencies additionally exotic times in OFDM systems [3]. Now, it has been enhanced into larger frequencies which might be superior that is determined in time, as well as lesser frequencies are better made up our minds in frequency Its Continuous and Discrete time versions are much integrated in many signal-processing applications. Taking this into consideration, the sign stays reproduced via orthogonal wavelet intent; additionally calculate independently converted materials of the time discipline sign [4]. The wavelet even be categorized as two lessons, Continuous ripple develop into discrete ripple change into. A sub-band coding is implemented in discrete wavelet where the sign is analyzed and processes over a series of filter banks. The complete source sign will be split into multiple frequency bands and encrypts each frequency separately on the spectrum. Hence this gives rise to the two steps which might be utilized in signal transmission scheme, namely the decomposition and the reconstruction.

Also,

$$2\sqrt{P} = \sqrt{\frac{2E_b}{T_b}} \tag{4}$$

with

$$E = \frac{1}{2}A^2 T_b \tag{5}$$

where T_b is the bit duration.

Therefore,

$$s_1(t) = \sqrt{\frac{2E_b}{T_b}} Cos(2\pi f_c t) \tag{6}$$

for binary 1 and

$$s_2(t) = -\sqrt{\frac{2E_b}{T_b}} Cos(2\pi f_c t) \tag{7}$$

for binary 0 sent. Hence, defining

$$\phi_{12}(t) = \pm\sqrt{\frac{2}{T_b}} Cos(2\pi f_c t) \text{ for } \quad 0 \le t \le T_b \tag{8}$$

Then the signal set of the BPSK signal is

$$s(t) = \left\{\sqrt{E_b}\phi_1(t), -\sqrt{E_b}\phi_2(t)\right\} \tag{9}$$

The evaluation interval entails of sub-band filter surveyed with the aid of down sampler and the period of synthesis subsequently makes the use of up sampler. Ultimate restoration process can be exhibited by the use of this filter through the channel, giving rise to Quadrature Mirror Filter (QMF) [5]. Each and every stage is engaged with LPFs and HPFs for analyzing frequency intervals and converting them into corresponding DWT coefficients. The approach of restoring the coefficients based on the received symbols is termed as DWT demodulation in other words Inverse DWT. Geared towards every state of filter fiscal institution measurement, the DWT coefficients are up sampled furthermore for the synthesis filter banks.

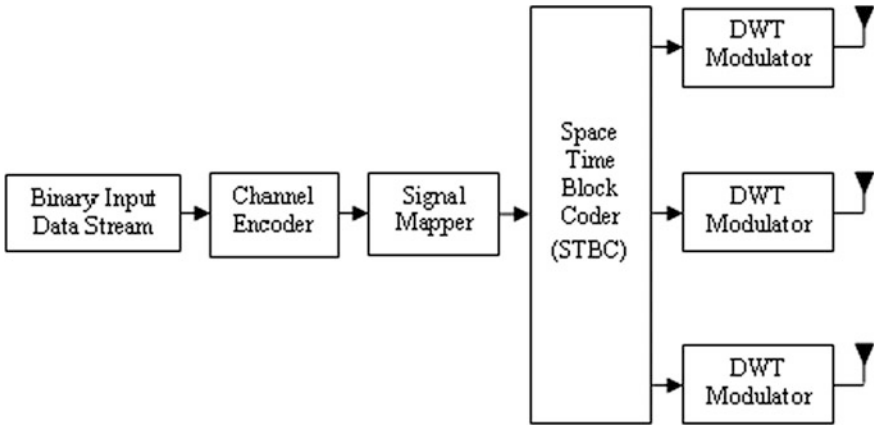


Fig. 4 Block diagram representation of DWT based MU-MIMO-OFDM Transmitter

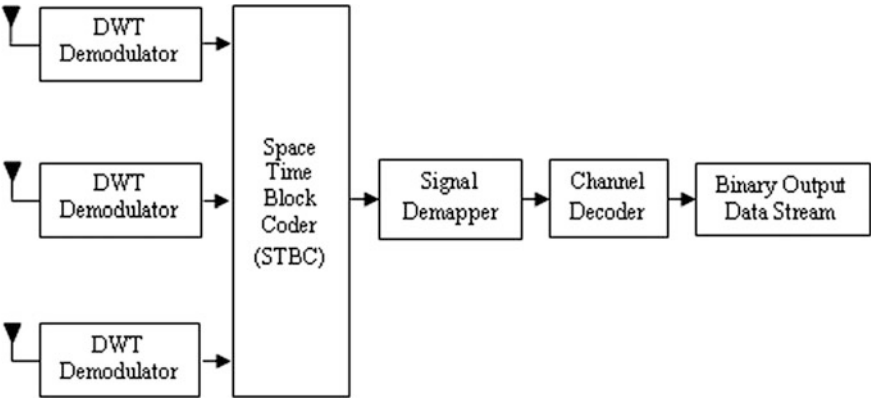


Fig. 5 Block diagram representation of DWT based MU-MIMO-OFDM Receiver

The block diagram representation of transmitter and receiver of DWT situated MU-MIMO-OFDM is shown in Fig. 4 and Fig. 5 respectively. Except the guard interval blocks, all the blocks remain same compared to the FFT centered ones.

4 Simulation Outcomes

Figure 6, Fig. 7, and Fig. 8 show the graphical illustration of thought and sensible procedure of Daubechies, Symlet, and Haar wavelets respectively. It has been proven from the simulated results that the Haar mother wavelet supersedes the opposite two within the performance. The simulations outcomes are centered on BER versus SNR (signal-to-noise Ratio) for QPSK modulation scheme under the MIMO-OFDM methods.

The above Figure shows that the theoretical and practical approaches of the first two wavelets are not smooth enough and has a high BER at some points of SNR, but whereas the Haar version gives a smooth curve with diminishing BER over an increased SNR.

Figure 9 illustrates the performance analysis of the DWT based MU-MIMO-OFDM for BPSK modulation scheme under AWGN channel. The theoretical and the simulated versions depicted clears that the simulated version gives a low BER.

Figure 10 and Fig. 11 determines the illustration of FFT headquartered MU-MIMO-OFDM and DWT headquartered MU-MIMO-OFDM for 10^4 and 10^6 transmitted symbols respectively. Right here a 64-user case is regarded with a couple of antennas at the transmitter and at the receiver. The simulation outcomes are obtained by utilizing BPSK and QPSK modulation schemes under AWGN Channel. It can be clearly observed that the BER of DWT based MU-MIMO-OFDM outperforms the FFT based one. Comparison analysis states

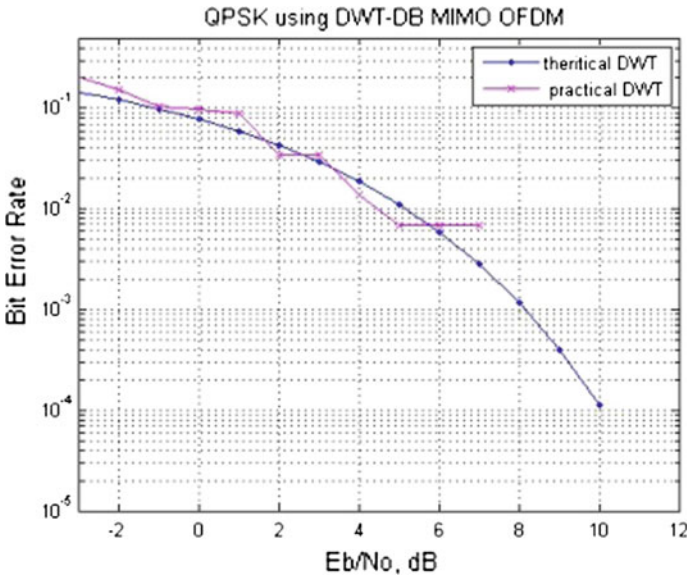


Fig. 6 QPSK based MIMO-OFDM using Daubechies Wavelet

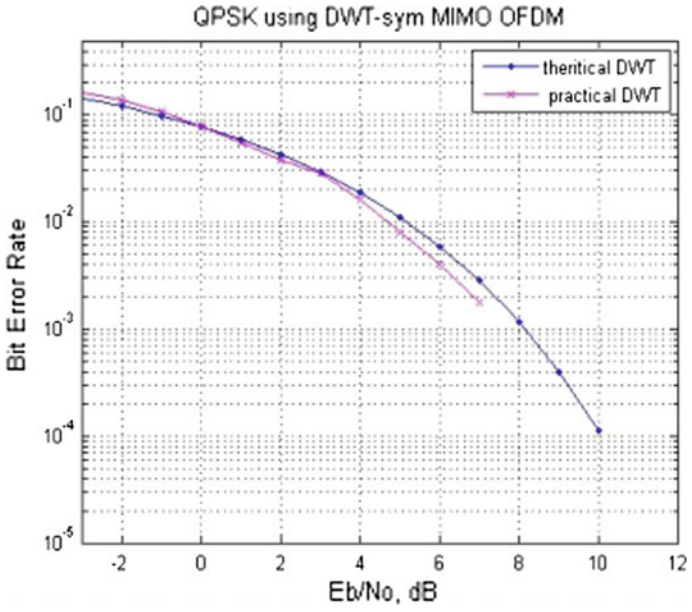


Fig. 7 QPSK based MIMO-OFDM using Symlet Wavelet

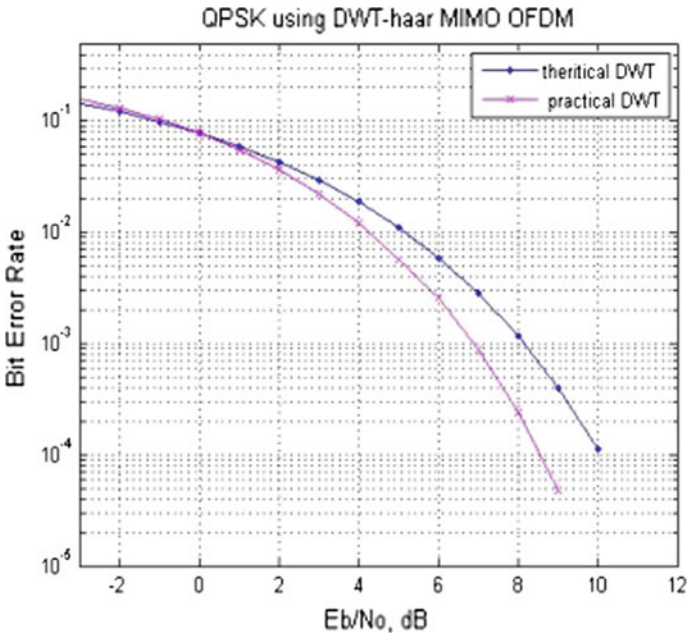


Fig. 8 QPSK based MIMO-OFDM using Haar Wavelet

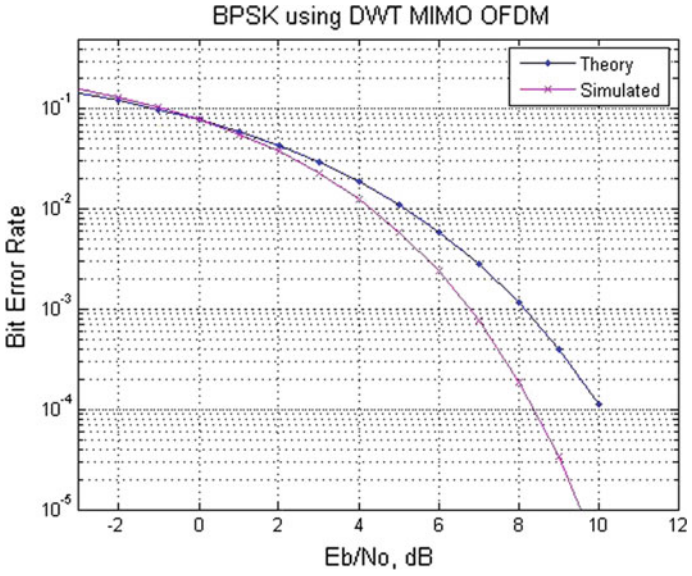


Fig. 9 BER versus E_b/N_o for DWT based MU-MIMO-OFDM for BPSK Modulation Scheme

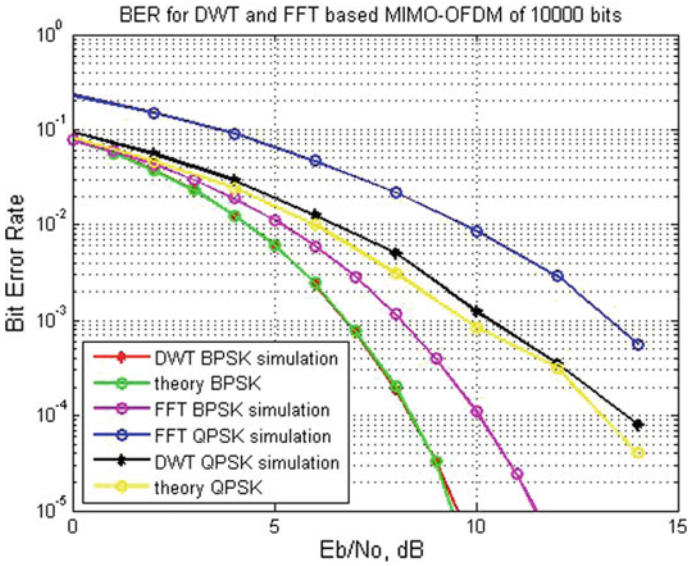


Fig. 10 BER versus E_b/N_o for FFT and DWT based MU-MIMO-OFDM for 10^4 transmitted symbols

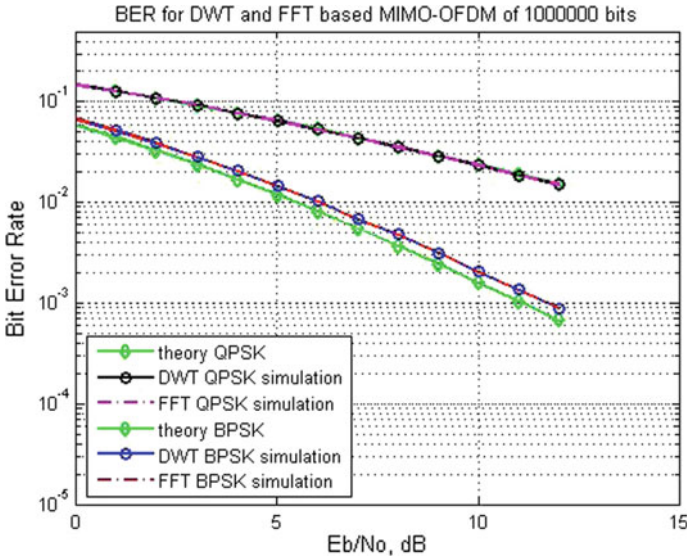


Fig. 11 BER versus E_b/N_o for FFT and DWT based MU-MIMO-OFDM for 10^6 transmitted symbols

that the bandwidth usage is potentially higher in the former case whether the safeguard intervals present or not.

5 Conclusion

To enhance the efficiency of an OFDM system, MIMO is a greatest approach. By evaluating the simulation outcomes, DWT founded MU-MIMO-OFDM outperformed the FFT-headquartered MU-MIMO-OFDM, which is based on the representation of BER. The need for cyclic prefix has been removed thus achieving a higher transmission capability. An impressive low Bit error rate with the discrete wavelet process gathered higher competencies in the new WiFi verbal exchange method for achieving excessive capabilities. Although, the information price by means of BPSK is lesser to QPSK, the BER performance of BPSK is sophisticated than QPSK. An increase in the antenna array at both the ends acquires assets by gathering additional energy which makes the BER to decrease furthermore.

References

1. Abdullah., Hussain.: Studies on DWT-OFDM and FFT-OFDM systems, ICCCP, 2009.
2. Meenakshi, D., Prabha. S., Raajan. N. R.: Compare the performance analysis for FFT based MIMO-OFDM with DDWT based MIMO-OFDM. 2013 IEEE International Conference on Emerging Trends in Computing Communication and Nanotechnology (ICECCN), (2013).
3. Nagesh. B.G., Nikookar. H.: Wavelet Based OFDM for Wireless Channels, IEEE Vehicular Technology Conference, Vol. 1, pp. 688–691, (2001).
4. Monisha. B., Ramkumar. M., Priya. M.V., Jenifer Philomina. A., Parthiban. D., Suganya. S., Raajan. N.R.: Design and Implementation of Orthogonal Based Haar Wavelet Division Multiplexing For 3GPP Networks (ICCCI -2012), Jan. 10–12, (2012).
5. Communication systems, 4th edition, Simon Haykin, John Wiley and Sons, Inc.
6. Wornell. G. W.: Emerging applications of multirate signal processing and wavelets in digital communications. Proc. IEEE, vol. 84, pp. 586–603, (Apr. 1996).

Digital Image Watermarking in RGB Host Using DWT, SVD, and PSO Techniques

Deepika Sanku, Sampath Kiran, Tamirat Tagesse Takore and P. Rajesh Kumar

Abstract The significance of watermarking is hiding the digital information by inserting bits into the host image. Hybrid domain image watermarking (I_{wg}) scheme using discrete wavelet transform (DWT) and singular value decomposition (SVD) is proposed in this paper. Singular values of WI are obtained using SVD and modified by scaling factor. In this paper, we propose evolutionary computing tool known as particle swarm optimization (PSO) for efficient and secured I_{wg}. Different image processing attacks were performed on the watermarked image to evaluate the performance of the algorithm. By evaluating PSO for watermarking in the presence of several attacks, the proposed method becomes robust than the other conventional methods discussed earlier. The visual quality of watermarked image (I_{wd}) is measured using PSNR. The existence of watermark is checked by extracting it and the robustness is measured using NCC. The proposed algorithm is implemented using matlab software.

Keywords DWT · SVD · PSO · PSNR · NCC

D. Sanku (✉) · S. Kiran · T.T. Takore · P.R. Kumar
Department of Electrical and Communication Engineering (ECE),
Andhra University College of Engineering (Autonomous), Andhra University,
Visakhapatnam, Andhra Pradesh, India
e-mail: sankudeepika@gmail.com

S. Kiran
e-mail: sampathauce115@gmail.com

T.T. Takore
e-mail: tameauce2014@gmail.com

P.R. Kumar
e-mail: rajeshauce@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_35

1 Introduction

Discretely submerging a mark in a noise tolerant signal is known as digital watermarking. Digital watermarks are basically used to endorse the authentication of a signal, copyright shielding, software crippling, etc. The information which is submerged in other image is known as watermark. Similarly, the host image refers to the image which contains this watermark. Then the watermarked digital signal is transmitted through communication channel where the data is exposed for attacks. The two main requirements of watermarking is robustness and imperceptibility. The technique of watermarking can be considered as robust if it could survive through several desired and undesired transformation. Over the time both the host as well as the watermarking image should remain unaltered and indistinguishable.

In recent past, several DWT techniques are proposed. These techniques are mostly based on spatial as well as frequency domain. They are capable of embedding watermark image (I_w) in the host image. Also they are involved in extracting I_w from the host image. Several algorithms like DWT, DCT, and DFT often applied for efficient watermarking and extraction. Attacks used in this paper are Gaussian noise insertion attack, Salt and Pepper noise attack, Rotation attack, Bit plane removal, and Resizing attack.

In this paper, the novel technique of employing PSO is performed for better watermarking for its obvious advantages due to its inherent realistic approach. The approach is capable of overcoming several issues cited above. The following sections are as organized: Sect. 2 discusses the I_{wg} techniques-SVD, DWT, PSO and Arnold scrambling. Section 3 discusses the proposed work and Sect. 4 consists of results followed by acknowledgement.

2 Watermarking Techniques

Original host image is decomposed using DWT to obtain LL_3 sub band which is approximation coefficients of third level DWT decomposition. Singular values of watermark image are obtained using SVD and after modified by scaling factor, it is embed on LL_3 sub band. PSO is used to optimize imperceptibility and robustness by searching best scaling factor.

2.1 SVD and DWT

SVD involves in complexed matrix manipulation. The SVD of an $A \times B$ dimensioned matrix referred by 'm' is realized by $U\Sigma V^*$. Here 'U' has $A \times A$ dimension which can be real or complexed, which Σ is $A \times B$, real valued on its diagonal. The matrix V is again a complex valued with dimensions $B \times B$.

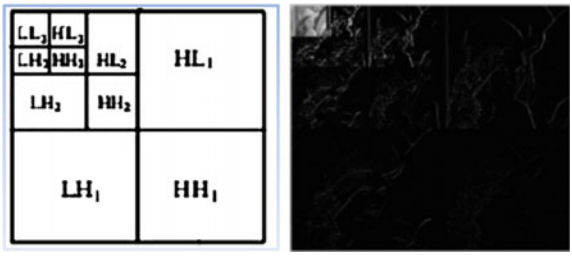


Fig. 1 Three level DWT decomposition

Similarly the DWT perform watermarking by taking quantization of adjacent wavelet coefficients. These coefficients are from the wavelet tree. Moreover, these coefficients can be extracted blindly. Considering the inherent energy consumption properties, these DWT have become popular in the recent past. The three-level DWT which is employed in the proposed work is demonstrated in Fig. 1.

2.2 Particle Swarm Optimisation

PSO emerged as a potential algorithm for optimization [1, 2]. The first step in PSO is initializing of swarm particles. Every particle say P_i holds two variables. These two variables are referred as position and velocity. For the first iterations, these positions are considered to be the local best. PSO Algorithm is as follows:

(i) Initialize position $p_i(t)$ and velocity $v_i(t)$
(ii) For each position fitness function is to be evaluated.
(iii) The local best position and global best position are computed.
(iv) The above computed values of $p_i(t)$ and $v_i(t)$ are substituted in the Eqs. (1) and (2):

$$v_i(t+1) = w \times v_i(t) + L1 \times \text{rand}(l_{\text{best}} - p_i(t)) + L2 \times \text{rand}(g_{\text{best}} - p_i(t)) \quad (1)$$

and

$$p_i(t+1) = p_i(t) + v_i(t) \quad (2)$$

W—inertia weight, every iterations step size is determined.
L1, L2—are local and global learning coefficients.
Rand—generate a number between (0, 1).

(v) Steps (ii–iv) are repeated until stopping criteria is achieved.

Fitness function: Fitness function can be calculated using the equation

Fitness function is denoted as 'f' and it is defined as

$$f = Q + PSNR + \frac{1}{N}\sum_{i=1}^{N} \lambda_i \rho_i \tag{3}$$

where weighting factor N is used to balance the imperceptibility and robustness of embedded watermark [3] and Q is the image quality index factor.

The root mean square error (RMSE) and peak signal to noise ratio (PSNR) is measured as

$$RMSE = \frac{\left[\sqrt{\left[f_{(i,j)}\right] - \left[F_{(i,j)}\right]}^{2}\right]}{N^2} \tag{4}$$

$$PSNR = 20 \log \frac{255}{RMSE} dB \tag{5}$$

The RMSE significantly distinguished the host and water marking images and the amount of degradation is given by PSNR. In the above equation f(i, j) and F(i, j) represent the host and the watermarked images, respectively.

2.3 Arnold Scrambling

The watermark should be provided with a high level security so that it holds itself robust in the case of unauthorized access. For this purpose the pixels in the image needs to be shuffled in a way that it can be reversed only by the unique key or a code. AT provides iterative movement to the elements present in an array [4]. For this reason AT is termed as a powerful tool in this process. Arnold transform in 2-D dimensions is as follows:

$$\begin{bmatrix} x_i \\ y_i \end{bmatrix} = \begin{bmatrix} 1 & m \\ n & mn+1 \end{bmatrix} \begin{bmatrix} x_i - 1 \\ y_i - 1 \end{bmatrix} \bmod (h) \tag{6}$$

m, n—Positive integers
h—Height of the image
x_i, y_i—Updated value of x and y pixels after ith iterations.

The above process is cyclic, i.e. the transforming values return to their original value after a fixed number of iterations. As the time period (T) depends on m, n and i the value can be used as a key for randomization. Watermark logo and its Arnold transformed image are shown in Fig. 2.

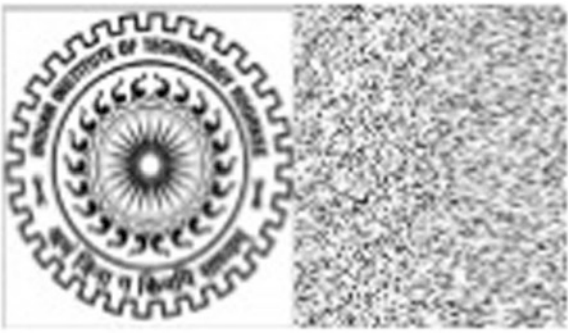


Fig. 2 Watermark logo and its Arnold transformed image

3 Proposed Work

The proposed algorithm comprises of two main processes: Like watermark embedding.

The details of the two processes are given below.

3.1 Watermark Embedding

The following are the steps which are used to insert watermark to the host image

Input: Original Image (I) of size P × Q and watermark image(M) of size r × c.

Output: Watermarked image $I_{M.}$

Step 1: The host image is decomposed into Red Green Blue (RGB) components and one component at a time is selected.

Step 2: Perform three level DWT on R component using haar wavelet and select the approximation coefficient LL_{I3}.

$$LL_{I3} = \text{Three level DWT } (R, \text{Haar});$$

Step 3: Scramble (disorder) watermark image W using Arnold method.

$$W_{arn} = \text{Arnold transform } (W, \text{key});$$

Step 4: Use SVD method to factorize both LL_{I3} and W_{arn} to insert watermark using singular value.

$$[U_1, S_{LLI3}, V_1] = SVD(LL_{I3})$$
$$[U_2, S_{Warn}, V_2] = SVD(W_{arn})$$

Step 5: Using the scaling factor obtained from the PSO the watermark is embedded.

$$S_{IW} = S_{II3} + K \times S_{Warn}$$

Step 6: Perform inverse SVD.

$$LL_{I3W} = U_1 \times S_{IW} \times V_1^T$$

Step 7: Obtain watermarked image R $_{channel}$ by performing three level inverse DWT.

$$R_m = \text{Three level, Inverse DWT}(LL_{I3W})$$

Step 8: Combine the three components $R_{M,}$ G, B to obtain watermarked colour image.

$$I_M = \text{RGB component}(R_M, G, B)$$

3.2 Watermark Extraction

The process of Watermark extraction is the reverse of watermark insertion. The following are the steps:

Input: Watermarked image I_M and watermark M.
Output: Extracted watermark M_E.

Step 1: Split I_M into RGB components and select the component on which the watermark is to be extracted.
Step 2: Perform three level DWT on selected component to obtain LL_{3E}.
Step 3: Perform SVD on LL_{3E} to get S_E.
Step 4: Using the scaling factor which was used during embedding watermark to the following equation is extracted:

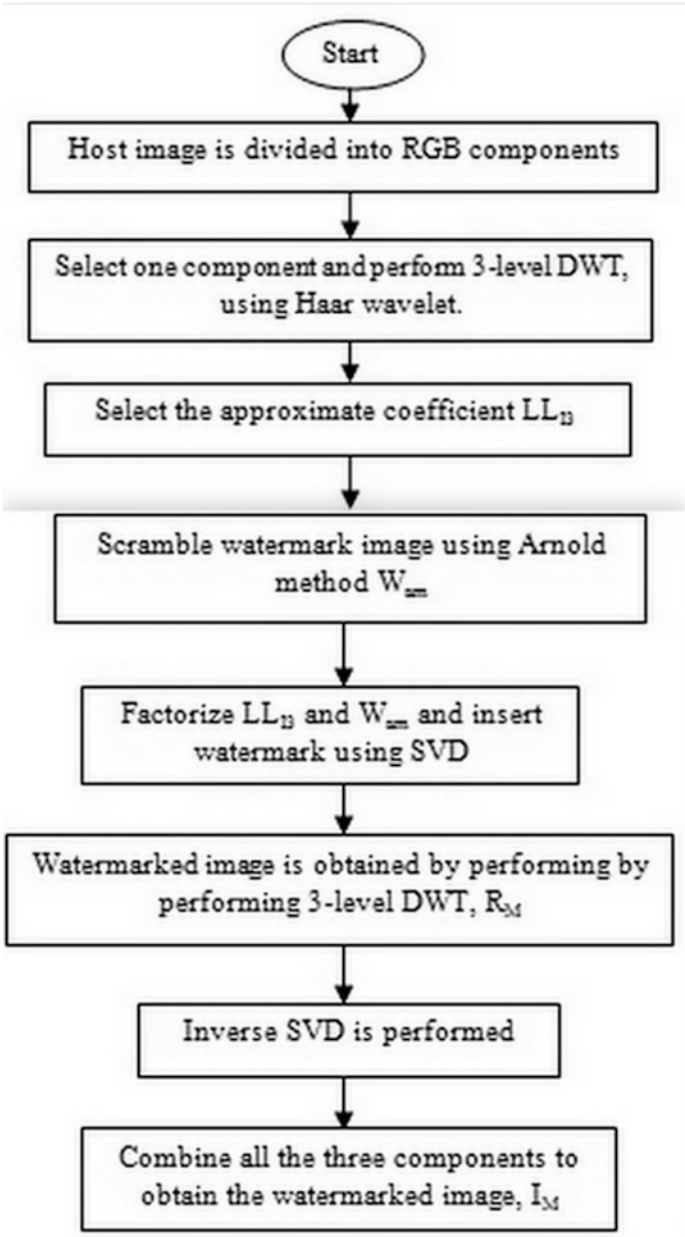


Fig. 3 Flow chart of the embedding process

$$S_E = (S_{ME} - S_I)/K$$

Step 5: Perform inverse SVD to obtain the scrambled extracted watermark.

$$M_{arn} = U_m \times S_E \times V_M^T$$

Step 6: Use inverse arnold scrambling to get extracted watermark M_E.

Below is the flowchart describing the embedding process in Fig. 3 and watermark extraction process in Fig. 4.

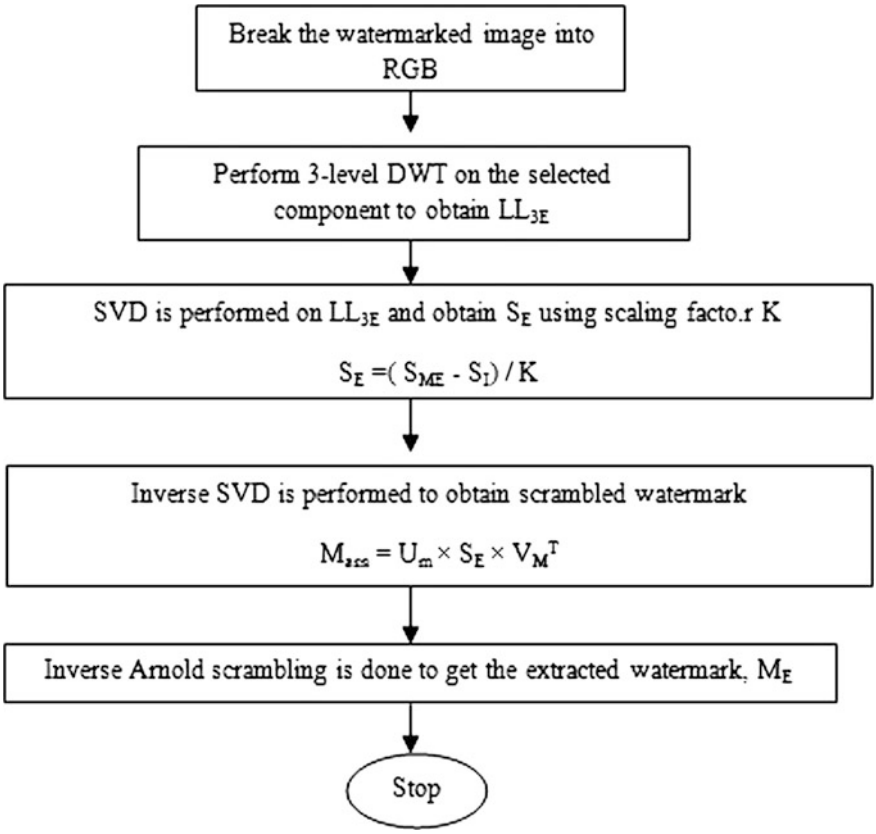


Fig. 4 Flow chart of watermark extraction

4 Results

In this section, results pertaining to proposed work are presented.

Figure 5 is the original watermark, encrypted watermark and the original host image on which we used on the proposed algorithm. In Table 1 attacked watermarked image, extracted watermark and the corresponding PSNR and NCC values are given.

Fig. 5 Original watermark, encrypted watermark and host image

Table 1 NCC and PSNR values obtained for various attacks

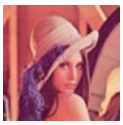
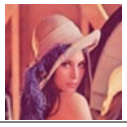
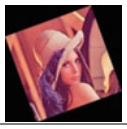
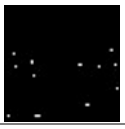
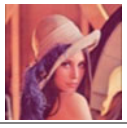
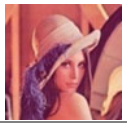
Attack name	Image of the attack	Scaling factor	Watermark extracted	NCC	PSNR
Gaussian noise insertion attack		0.0257		0.9435	55.9299
Salt and pepper noise attack		0.1670		0.9872	39.6742
Rotation attack		0.0189		0.3818	58.5993
Bit plane removal		0.0360		0.9977	48.5655
Resizing attack		0.0249		0.9098	56.2045

Table 2 Comparing PSNR values between reference paper [5] and proposed thesis

Attacks	PSNR value		NCC value	
	Proposed method	Reference paper	Proposed method	Reference paper
Gaussian noise insertion	55.9299	15.3425	0.9435	0.9306
Salt and pepper noise insertion attack	39.6742	11.3131	0.9872	0.9948
Rotation attack	58.5993	21.6937	0.3818	0.9855
Bit plane removal	48.5655	N.A.	0.9977	N.A.
Resizing attack	56.2045	25.8556	0.9098	0.9788

On comparison with an international journal on communications paper which worked on robust colour image watermarking based on SVD and DWT (2014), the proposed algorithm in this thesis yield better PSNR values as demonstrated in the Table 2.

5 Conclusion

Efficient watermarking technique is stimulated using SVD, PSO, DWT and Arnold Scrambling. The technique is simple with less computational steps and less complexity. The performance in terms of PSNR and NCC is outstanding with PSO compared with conventional.

References

1. Analysis of Gray Scale Watermark in RGB Host using SVD and PSO Ferrante Neri Centre for Computational Intelligence.
2. The Gateway, De Montfort University Leicester, United Kingdom fneri@dmu.ac.uk.
3. http://www.cptwg.org/.
4. Sridhar. B., Arun. C.: A Wavelet based Image Watermarking Technique using Image Sharing Method", IEEE (2013).
5. A Robust Color Image Watermarking Based on SVD and DWT, Li ZHANG*, Jia Wei XIAO, Jing Yun LUO, Institute of Information Engineering, Shenzhen University, Shenzhen Guangdong 518060, China *wzhangli@szu.edu.cn; jiaweixiao@szu.edu.cn; jingyunluo@szu.edu.cn.

Improved SQRT Architecture for Carry Select Adder Using Modified Common Boolean Logic

Jaya Lakshmi Jujjuru and Rajanbabu Mallavarapu

Abstract The binary adders are the most essential and fundamental circuit element to perform the arithmetic operations in digital computers. These binary adder circuits are widely used in integrated circuits (IC) such as processors, and their usage does not limit inside arithmetic logic unit (ALU) of a processor. In fact these binary adders are also playing key role in various applications like digital filters, digital transformation cores, signal processing elements, digital modulators and demodulators, digital image/video processing, and cryptographic applications. The small performance metric of the binary adder circuit will yield significant advantage in larger computations. Designing of faster, smaller, and more powerful efficient binary adder has been the ultimate challenge for many researchers. To succeed in this challenge, numerous architectures were proposed in past, which results in various architectures for the binary adder. In recent times, the carry select adder (CSLA) architecture was considered as one of the best suitable architectures which showed better performance among the others. Several new architectures were introduced in CSLA to improve its performance further. The area occupied by the CSLA adder is one of the performance metrics to evaluate the efficiency of the CSLA adder. This is because the CSLA adder uses two ripple carry adders for the both states of single carry input. Thus, the adders use two times more circuit elements than necessary. Several approaches like binary-to-excess-1 converter (BEC-1), common boolean logic (CBL), and SQRT architectures were proposed to reduce the area of the CSLA architecture. This article introduced a new approach in SQRT–CSLA adder using modified CBL. The common Boolean logic performs the evaluation of carry-based selection with less area than other design techniques. The design proposed in this article introduced a new CBL architecture which succeeded in reduction of area compared to the previous architectures. The CSLA adders with

J.L. Jujjuru (✉) · R. Mallavarapu
Department of Electronics and Communication Engineering,
Lendi Institute of Engineering & Technology, Jonnada, Vizianagaram
535005, Andhra Pradesh, India
e-mail: lakshmij.lendi@gmail.com

R. Mallavarapu
e-mail: mrajanbabu@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_36

the proposed CBL architecture were implemented for the various word sizes like 8-bit, 16-bit, and 32-bit. The reduction of area has been clearly observed in the results. These results prove that the proposed CSLA scheme exhibits better performance than the regular SQRT–CSLA.

Keywords CSLA · SQRT · CBL

1 Introduction

An adder is the arithmetic component which performs addition constructed by digital circuit. The digital circuits perform the addition in binary format. This addition can be performed by binary adders. These adders can be easily found inside arithmetic logic unit (ALU) of any processor. Apart from the processor, the binary adders were the most essential element in other applications such as digital filter applications, digital transformation applications (FFT, IFFT, DCT, DWT, etc.), signal processing applications, digital modulator/demodulator, digital image/video processing, and cryptographic applications. The performance of the binary adder does not show great impact when it is used inside a processor. This is because the processor performs the addition operation as a machine cycle under an instruction cycle. Beyond this, in most of the cases, the adder may not be necessary to operate. Thus, the impact of the binary adder circuit efficiency on the general purpose processor may be significantly less. Unlike the processor, the performance of the adder circuit shows significant impact on the overall performance of the application-driven logic circuits. This is because the binary adder should perform the addition in iteration cycles or the streaming data flown from the input or previous stage. Here, the performance of the binary adder is a great concern and in most of the applications this binary adder behaves like speed limiting and more power-consuming element as well.

The demand for the high-speed, low-area, and power-efficient adders has increased predominantly. Several researchers proposed various architectures to meet the performance requirements. But achieving the optimal design is a big challenge as speed, area, and power consumption were contrast to each other. The demand for the handheld and mobile computing devices is exponentially increasing in daily life. These mobile devices occupy less space and its performance also great concern. So, for these, the area constrained must be strictly satisfied without compromising in the speed of the circuit. So the area of the circuit must be minimized without affecting the speed of the circuit. The CSLA adder was considering one of the options to choose as the best adder for the high-speed requirements.

The CSLA adder works on the principle of selecting the result based on the carry input. In detail, the external carry input is 1-bit size that means it will have either carry information as logic-0 or logic-1 in any arbitrary case. With this principle, the CSLA adder works. The regular CSLA has two ripple carry adders in which one adder performs the addition between the input operands by considering carry

information as logic-0 ($C_{in} = 0$) and another ripple carry adder was used to perform the addition to the same inputs by considering carry as logic-1 ($C_{in} = 1$). The both results were given to a group of 2:1 multiplexer and the select line of all multiplexers attached to actual carry input. With this, based on the logic state of the carry input, the corresponding pre-computed sum and carry out will be then passed to output. This will help to reduce the carry propagation delay from carry input to carry output. This enables faster addition with small switching delay offered by the select line of the multiplexers.

The two significant properties of adder circuit are termed as power consumption and propagation delay. These two properties of an adder circuit are contrasted to each other. The longer propagation delay effects the speed and power consumption and vice versa. Any proposed model considers these two on design parameters for their vital contribution to the performance. However, these two are often comprised to enhance the performance with low area. Most of the architectures provide different insights and therefore require different implementations. The both area and speed of the adder circuit must optimize carefully.

The problem associated with the CSLA adder is its area. The regular CSLA use two ripple carry adders. Apart from this, the modern VLSI technologies keep on continuing with the feature reduction of the MOSFET along with the constant field scaling to compensate various short-channel effects of the device. As the applied electric field to the MOSFET scaled down, the control on the channel will be reduced. This will increase the leakage current exponentially and as the chip density increases all these combined together will increase the static power consumption of the chip. The dynamic switching power of the chip depends on the rate of processing done by the chip. Thus, the adder will consume huge dynamic switching power as the increase in the speed of its operation. This summarizes that the high-speed, low-area, and energy-efficient architecture must be developed so that the design can meet the requirements and overcome the design challenges.

By considering these above challenges, several CSLA adder architectures have been proposed in recent times. Each architecture provides different insights and thus suggests different implementations. This article proposes the low-area carry select adder using modified common Boolean logic. The half adder (HA) based on common Boolean logic [3–7] simplifies the Boolean logic for the generation of duplicate sum and carry output, designed using simple NOT and OR logic gates and select the value using the multiplexer. The proposed design in this article helps further reducing the area of the adder.

This paper is organized as follows: Sects. 2 and 3 describe about the conventional and modified CSLA using BEC, respectively. Section 4 describes about the CSLA adder with common Boolean logic (CBL) and proposed CBL and the results are analyzed in Sect. 5 followed by conclusion in Sect. 6.

2 Conventional SQRT–CSLA Architecture

Once the carry-in bit is received by the full adder (FA), the instruction for carry out is initiated. This is taken place due to the changeover of this incoming carry. This is a chain process that migrates from previous stage to next stage. By this way the C_{in} effects the C_{out}. As a result the RCA speed appears completely governed by the C_{out} from the previous stage. Hence, it can be understood that there exists a linear relationship between C_{in} and $C_{out.}$ In CSLA in order to enhance the speed, the C_{in} is assumed either '0' or '1'. Using these values it is possible to generate both C_{out} and partial sum at a time. For this purpose multiplexer (MUX) is employed. The role of MUX in this case is to determine the final sum as well as carry. The technique uses the received C_{in}. Using this, it is possible to reduce the computation and area consumed. For this purpose, in 7 A 16-bit SQRT–CSLA is designed and demonstrated. The conventional model of CSLA is shown in Fig. 1. It is visible from Fig. 1 that circuit has five groups. Sum and carry are mentioned as follows:

$$S = a \oplus b \oplus c_{in} \tag{1}$$

$$C_{out} = a.b + b.c_{in} + a.c_{in}. \tag{2}$$

In this a, b, c_{in} are inputs and S, C_{out} are sum and carry out.
For the group 2, calculations are given as follows:

2-bit RCA gates requires = 2 * FA.
With the conclusion 2:1 MUX the output Y is given as

$$Y = a.s + b.s. \tag{3}$$

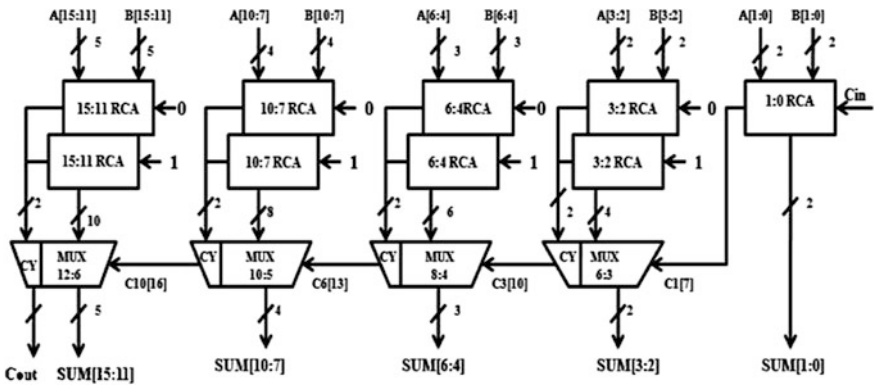


Fig. 1 Conventional SQRT–CSLA adder

2:1 MUX in this case comprises 2 AND gates, 1 NOT gate, and 1 OR gate; similarly, 6:3 MUX should be implemented by 3, 2:1 MUX.

$$\text{Total gate count in group 2} = 2-\text{bit RCA with } C_{in} = 0 + 2-\text{bit RCA with } C_{in} = 1 + 6{:}3\ \text{MUX}$$
$$= \{2*(\text{FA})\} + \{2*(\text{FA})\} + \{6*(\text{AND}) + 3*(\text{or})\} + 1*(\text{INVERTER})\}.$$

3 SQRT–CSLA Using Binary to Excess-1 Converter (BEC-1)

To minimize the area and power consumption a new technique is proposed. The technique involves in using a single carry adder with binary to excess-1 converter instead of RCA with $C_{in} = 1$. For implementing this CSLA, n-bit RCA and an n + 1 bit BEC are used. The function table of 4-bit BEC is in given Table 1. The expressions of 4-bit BEC are shown Fig. 2; the 16-bit CSLA using BEC implementation is mentioned. It has five groups with separated bit size of RCA and BEC.

$$X_0 = \sim B_0 \tag{4}$$

$$X_1 = B_0 \wedge B_1 \tag{5}$$

$$X_2 = B_2 \wedge (B_0\ \&\ B_1) \tag{6}$$

$$X_3 = B_3 \wedge (B_0\ \&\ B_1\ \&\ B_2). \tag{7}$$

The modified 16-bit CSLA using BEC is shown in Fig. 2. The structure is again divided into five groups with different bit sizes RCA and BEC.

The logic diagram of a 4-bit BEC-1 is shown in Fig. 3a and the CMOS layout diagram is shown in Fig. 3b. The input to n + 1 bit BEC is the sum output of n-bit RCA. This generates an output which is similar to RCA output when $C_{in} = 1$. This is possible by adding binary-1 to the correct input. This is followed by a MUX. One input to this MUX is output of the above case, whereas the other input being the case when $C_{in} = 0$. Now, using the stage C_{out} signal, the final 'S' and 'c' are generated. For the above cases, it is possible to perform using 1HA in place of the

Table 1 Function table of the 4-bit binary to excess-1 converter (BEC-1)

Binary [3:0]	Excess-1 [3:0]
0000	0001
0001	0010
0010	0011
|	|
|	|
1110	1111
1111	0000

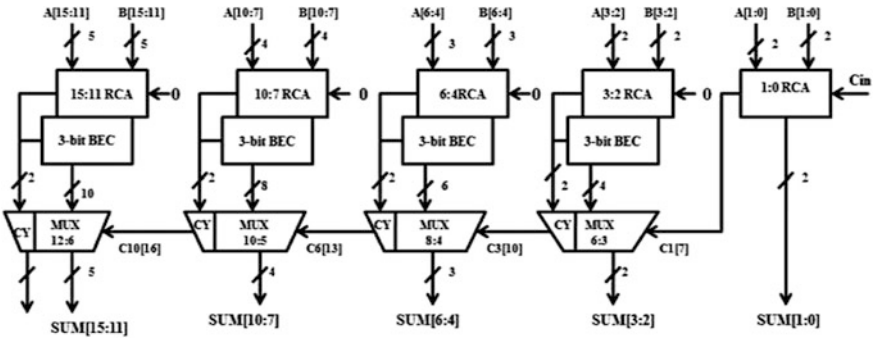


Fig. 2 SQRT–CSLA architecture using binary to excess-1 converter (BEC-1)

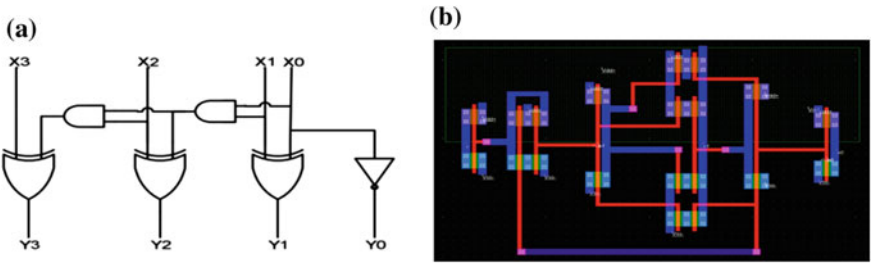


Fig. 3 **a** Binary to excess-1 converter, **b** CMOS layout

first FA or RCA. This is due to the reason that only two bits are involved in calculation.

Calculation based on CSLA with BEC-1 is shown in Table 2.

The BEC structure in the modified CSLA adder has reduced the area and power when compared with the regular CSLA adder, but the delay in the BEC-based CSLA is increased than the regular CSLA [1].

Table 2 Gate calculation of SQRT–CSLA using BEC-1

Parameter	HA	FA	XOR	OR	AND	NOT
Group-1	1	1	0	0	0	0
Group-2	1	1	2	3	7	2
Group-3	1	2	3	4	10	2
Group-4	1	3	4	5	13	2
Group-5	1	4	5	6	16	2
Total	5	11	14	18	46	8

4 SQRT–CSLA Using Common Boolean Logic (CBL)

The binary to excess-1 converter (BEC) is replaced by common Boolean logic (CBL). The advantage of the common Boolean logic block is which eliminates the need of duplicated adder cells by sharing the sum and carry data. This will make the design as an area-efficient as shown in Fig. 4. The overall transistor count with this approach will drop down and achieve low dynamic power consumption of the circuit.

4.1 Common Boolean Logic Using FA

In Fig. 5, the CSLA and CBL of sum and carry are designed by forming of sum and carry pair. It needs only 1 OR gate with 1 NOT gate. Based on the logic state at the C_{in} signal, the selection of proper C_{out} is carried out.

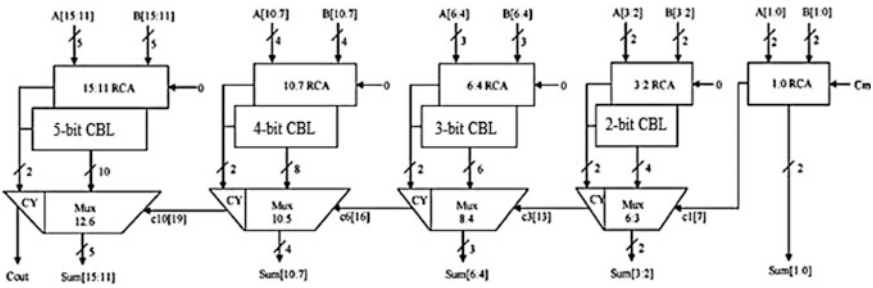


Fig. 4 SQRT–CSLA adder using common Boolean logic (CBL)

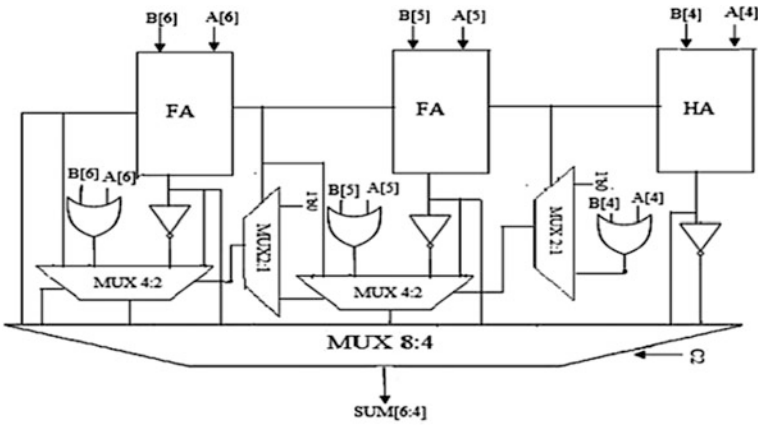


Fig. 5 Group-3 common Boolean logic

Table 3 Truth table of single-bit FA and single-bit FA with CBL

C_{in}	A	B	S_0	C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The inverter and OR gate derive the sum and carry output signals for the input $C_{in} = 1$. Then with the help of the multiplexer, the corresponding outputs can be selected based on the external carry-in value. By understanding the truth table of 1-bit full adder shown in Table 3, it has been observed that the output summation complemented for the values $C_{in} = 0$ and $C_{in} = 1$ [2].

As the inverter and OR gate derive the sum and carry output signals for the input $C_{in} = 1$, then with the help of the multiplexer, the corresponding outputs can be selected based on the external carry-in value. Figure 5 refers to group-3 logic design. These are totally 36 number of gates used for this design. The RCA block at $C_{in} = 0$ forms one input to MUX, while the other in CBL.

A 3-bit addition is performed in group-3 using 1HA and 2, FA. The CBL comprising 4:2 MUX to select the carry out and sum for the $C_{in} = 1$. Through 2:1 multiplexer the carry signal is propagate to the next adder cell. The 6:3 multiplexers and 4:2 multiplexers are the combination of 2:1 multiplexer.

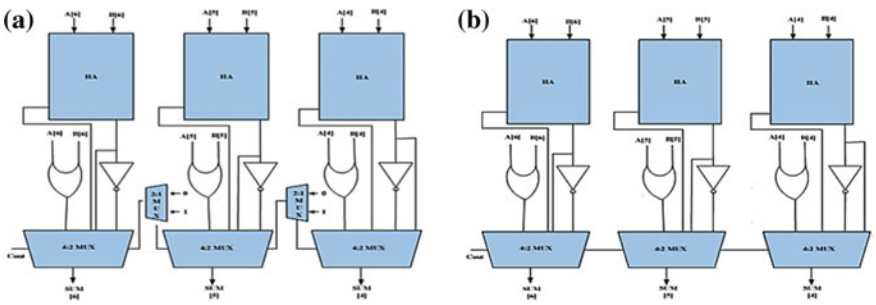


Fig. 6 **a** SQRT–CSLA adder using CBL-HA, **b** Proposed SQRT–CSLA adder using modified CBL

Table 4 Logic gate comparison for SQRT–CSLA using CBL-FA, CBL-HA, proposed CBL

	SQRT–CSLA adder with CBL using FA					SQRT–CSLA adder with CBL using HA					Proposed SQRT–CSLA adder with modified CBL using HA				
Parameter	HA	FA	OR	AND	NOT	HA	FA	OR	AND	NOT	HA	FA	OR	AND	NOT
Group-1	0	2	0	0	0	0	2	0	0	0	0	2	0	0	0
Group-2	1	3	8	12	2	2	2	7	10	2	2	2	6	8	2
Group-3	1	4	13	20	3	3	3	11	16	3	3	3	9	12	3
Group-4	1	5	18	28	4	4	4	15	22	4	4	4	12	16	4
Group-5	1	6	23	36	5	5	5	19	28	5	5	5	15	20	5
Total	4	20	62	96	14	14	16	52	76	14	14	16	42	56	14

4.2 Common Boolean Logic (CBL) Using HA

This design requires only one HA and CBL which optimizes the CSLA in the both area and power constraints. The half adder can be realized with one XOR and one AND gate only to generate the sum and carry output, respectively. And the CBL requires only one NOT and one OR gate to generate the pair of output signal for the input $C_{in} = 1$. The existing and proposed models are as shown in Fig. 6.

4.3 Modified Common Boolean Logic (CBL) Using HA

This article proposes the modified common Boolean logic (CBL) using HA which is shown in figure. In the proposed design, the carry selection MUX was removed. This is because it has been observed that the switching delay of the multiplexer inside every group of the SQRT–CSLA is having the same value with CPD of every group without the multiplexer. Thus, the multiplexer has been placed at every group instead of every bit. This will reduce the area of the circuit and the carry propagation path will slightly effected. As the SQRT–CSLA does not have longer carry path, the architecture was segmented as groups. This will nullify the overhead delay caused by removing the carry selection mux at every bit operation. The comparison results are shown in Table 4.

5 Performance Analysis of Proposed Model

The proposed common Boolean logic requires less number of gates for the logic realization and offer moderate delay between carry propagations. The proposed adder was implemented at 45 nm fabrication node. The area, power, and delay comparison is shown in Fig. 7.

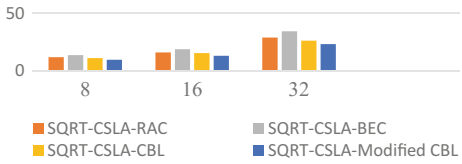


Fig. 7 Delay comparison between proposed and various SQRT–CSLA architectures

6 Conclusion

In this article, a simple approach on reducing the area of the SQRT–CSLA adder was proposed. The SQRT–CSLA adder has group segmented architecture, and thus the carry selection at every group may be sufficient. With this approach, the mux for carry selection at every bit can be compensated. The tradeoff has to be considered between the area and delay. The proposed SQRT–CSLA with modified CBL uses multiplexer at every stage instead of every bit for the selection which minimize the area as well as power consumed, when compared with conventional CSLA. This is due to enhanced delay with binary to excess-1 converter. The proposed model is suitable for the low-area and energy-efficient applications.

References

1. Ramkumar, B., Harish, K.: ASIC Implementation of modified faster carry save adder. Eupro. J. Sci. & Res. 42 53–58 (2010).
2. Kanchana Bhaaskram, V.S.,: Modified Carry Select Adder using Binary Adder as a BEC-1. Eupro. J. Sci. & Res. 103 156–164 (2013).
3. I-chyn, W., Cheng-chen, Yi-Sheng, L., Chien Chang, P.: An Area-Efficient Carry Select Adder Design by Sharing Common Boolean Logic Term. In IEEE Int. symposium circuit systems, (2005).
4. Manju, S., Sornagopal, V.: An Efficient SQRT architecture of carry select adder design by Common Boolean Logic. In Int. Con. VLSI Emb. Sys. Nano Ele. & Telcom. Sys (ICEVENT) (2013).
5. Sakthi Kumaran., Samiappa., Salivahanan, S., Kanchana Bhaaskaran. V.S., Vinoth, C.: A Very Fast and Low Power Carry Select Adder Circuit 3rd Int. Con. on Ele. & Com. Tech - ICECT (2011).
6. Rabaey., Jan M.: Digt. Intg. Cirt - A Design Perspective, Upper Saddle River, NJ: Prentice - Hall, (2001).
7. Bedrij, O.J.: Carry-Select Adder. IRE Trans. on Elec. and Comm., 340–344, (1962).

Synthesis and Design of Microwave Bandpass Filter Using Impedance Independent Coupling Matrix

Saurabh Kumar Pandey, Arvind Kumar Pandey and R.K. Chauhan

Abstract In this paper, a coupling matrix based method is used to synthesize a bandpass filter. The designing method is independent of change in source and load impedances. The proposed filter is synthesized by frequency transformation from lowpass prototype to bandpass filter. The MATLAB code is developed for frequency transformation and coupling matrix is generated. The filter is designed on RT/Duroid substrate with relative dielectric constant of 10.8 and thickness of 1.27 mm. The filter is designed and simulated on HFSS and response is found in good agreement with the response found from mathematical model.

Keywords Coupling matrix synthesis · Chebyshev filtering function · MATLAB · Frequency transformation

1 Introduction

A bandpass filter is a two-port network, which allows transfer of desired frequency component from input port to output port and restricts undesired frequencies. The group of desired frequencies is referred as band of filter. Microwave bandpass filter is a key component for wireless communication; many methods are developed for synthesis of microwave filter.

The coupling matrix approach for synthesis of filter is given by Atia et al. [1]. In 1980s, Cameron introduces a synthesis approach to generate transversal coupling

S.K. Pandey (✉) · A.K. Pandey · R.K. Chauhan
Department of Electronics & Communication Engineering, Madan Mohan Malaviya University of Technology, Gorakhpur, India
e-mail: saurabh0411@gmail.com

A.K. Pandey
e-mail: arvindmknk@gmail.com

R.K. Chauhan
e-mail: rkchauhan27@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_37

matrix for Chebyshev filtering function [2, 3], from coupling matrix, an eigenvalue optimization approach is developed to generate user-defined coupling matrix.

All the synthesis approach developed so for is based on the premises that any two-port network is terminated by real-valued impedances at both ends. However, in recent years, synthesis approach is developed with complex-valued impedance at either end of network [4]. Recently a synthesis technique of coupling matrix with arbitrary reference impedances at both ends is developed [5].

This paper proposes a design of bandpass filter with arbitrary reference impedance using the concept given for lowpass prototype. This paper also demonstrates the MATLAB-based coding of synthesis of microwave filter based on coupling matrix approach.

2 Synthesis Procedure

2.1 Chebyshev Filtering Function

The filtering function is expressed in form of transfer and reflection polynomial as

$$S_{11}(s) = \frac{F(s)}{\varepsilon_r E(s)} \quad S_{21}(s) = \frac{P(s)}{\varepsilon E(s)} \tag{1}$$

The reflection parameter $S_{11}(s)$ at port 1 of the network is expressed as the ratio of two finite-degree polynomials *E(s)* and *F(s)*, where *E(s)* is an Nth-degree polynomial with complex coefficients e_0, e_1, e_2, …, e_N. *N* is the degree of filter network under consideration. Also *F(s)* is an *N*th-degree polynomial with complex coefficient f_0, f_1, f_2, …, f_N. ε_r allows the normalization of the highest degree coefficient of *E(s)* and *F(s)* to unity. *E(s)* is strictly Hurwitz, because this is lossless and passive network. The numerator of transfer parameter $S_{21}(s)$ is *P(s)*/ε, whose zeros are the transmission zeros of the filtering function. The degree nfz of the polynomial *P(s)* corresponds to number of finite position zero that the transfer function incorporates. This implies that nfz $\leqslant N$; otherwise $S_{21}(s)$ exceeds unity as $s \rightarrow j\infty$, which is impossible for a passive network.

2.2 Synthesis Process

The synthesis of microwave filter starts from the specification of desired filter, that is, position of prescribed transmission zeros is expressed as polynomial *P(s)*, from *P(s)*, *F(s)* is obtained using a recursive loop in MATLAB. *P(s)* and *F(s)* give the value of *E(s)* using mathematical relation

$$\varepsilon^2\varepsilon_r^2 E(s)E(s)^* = [(jP(s)) + \varepsilon F(s)][\varepsilon_r(jP(s)) - \varepsilon F(s)]^* \quad (2)$$

E(s) is an Nth-degree polynomial with complex coefficients. *E(s)* must be Hurwitz polynomial, any singularity in the right half-plane can be reflected about the imaginary axis to lie in the image position in the left half-plane. Now knowing the position of the N singularities in the left half-plane, we can form the polynomial *E(s)*. After knowing the values of *P(s)*, *F(s),* and *E(s)*, the values of rest of the mathematical function is obtained using MATLAB coding. Algorithm demonstrated in following flow chart Fig. 1.

Using the expression of ABCD parameter given in [6], the short circuit admittance parameter obtained above is expressed as [7]

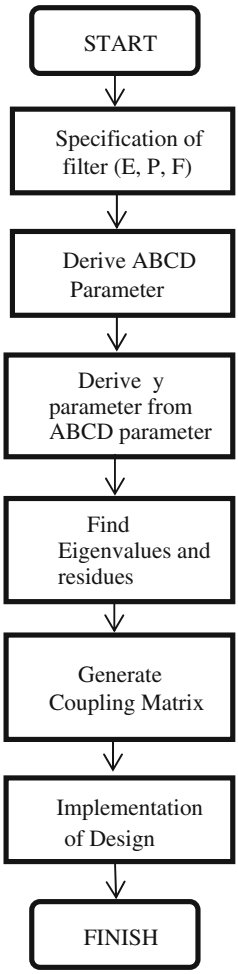


Fig. 1 Flowchart for MATLAB algorithm

$$y_d = Z_S^* Z_L^* E + Z_S Z_L^* \frac{F_{11}}{\varepsilon_R} + Z_S^* Z_L \frac{F_{22}}{\varepsilon_R} + Z_S Z_L \left(\frac{F_{11} F_{22}}{\varepsilon_R^2 E} - \frac{P^2}{\varepsilon_R^2} \right) \tag{3}$$

$$y_{11n} = Z_L^* \left(E - \frac{F_{11}}{\varepsilon_R} \right) + Z_L \left(\frac{F_{22}}{\varepsilon_R} - \frac{F_{11} F_{22}}{\varepsilon_R^2 E} + \frac{P^2}{\varepsilon_R^2 E} \right) \tag{4}$$

$$y_{22n} = Z_S^* \left(E - \frac{F_{22}}{\varepsilon_R} \right) + Z_S \left(\frac{F_{11}}{\varepsilon_R} - \frac{F_{11} F_{22}}{\varepsilon_R^2 E} + \frac{P^2}{\varepsilon_R^2 E} \right. \tag{5}$$

$$y_{21n} = -2\sqrt{Re(Z_S) Re(Z_L)} \frac{P}{\varepsilon}, \tag{6}$$

where y_d is denominator and y_{11n}, y_{21n}, y_{22n} are numerators of admittance matrix Y. The two port network is lossless and reciprocal, hence due to the orthogonally unitary condition

$$F_{11}^* = (-1)^N F_{22} \tag{7}$$

$$\frac{F_{11} F_{11}^*}{\varepsilon_R^2} + \frac{P P^*}{\varepsilon^2} = E \tag{8}$$

$$P(s)^* = (-1)^{N+1} P(s) \tag{9}$$

With the help of (7) and (8), a new relationship can be expressed as

$$\frac{F_{11}(s) F_{22}(s)}{\varepsilon_R^2} - \frac{P(s)^2}{\varepsilon^2} = (-1)^N E(s) E(s)^* \tag{10}$$

With the help of (9), the expressions (2–5) can be
Simplified to a new general synthesis formulas

$$y_d = Z_S^* Z_L^* E + (-1)^N Z_S Z_L E^* + Z_S Z_L^* \frac{F_{11}}{\varepsilon_R} + Z_S^* Z_L \frac{F_{22}}{\varepsilon_R} \tag{11}$$

$$y_{11n} = Z_L^* E - (-1)^N Z_L E^* + Z_L \frac{F_{22}}{\varepsilon_R} - Z_L^* \frac{F_{11}}{\varepsilon_R} \tag{12}$$

$$y_{22n} = Z_S^* E - (-1)^N Z_S E^* + Z_S \frac{F_{11}}{\varepsilon_R} - Z_S^* \frac{F_{22}}{\varepsilon_R} \tag{13}$$

Now, let us consider a matched network having complex source and load impedances Z_S and Z_L respectively. From the concept of power wave [8], the incident and reflected power vector is expressed as

$$a = D(v + Gi), \quad b = D(v - G^{+} i), \tag{14}$$

where 'a' is incident power vector and 'b' is reflected power vector. D and G are diagonal matrix with Kth component D_K and G_K as $1/2\sqrt{ReZ_K}$ and Z_K respectively, and + indicate complex conjugate transpose matrix, v is voltage and i is current. The admittance matrix is expressed as $i = Yv$. The power scattering matrix S is expressed as $b = Sa$. Thus from Eq. (5), we expressed admittance Y as

$$Y = (SDG + DG^{+})^{-1}(D - SD) \tag{15}$$

This expression is utilized to obtain admittance matrix Y from power wave scattering matrix S with random reference impedance G.

The coupling matrix obtained above is for lowpass prototype filter. To find the value of coupling matrix for bandpass filter, transformation of center frequency is required. The center frequency is transformed using relation

$$s = j\frac{\omega_0}{\omega_2 - \omega_1}\left[\frac{\omega_B}{\omega_0} - \frac{\omega_0}{\omega_B}\right] \tag{16}$$

Here $\omega_0 = \sqrt{(\omega_1 \omega_2)}$ is the center frequency of bandpass prototype (=1 rad/s), ω_2 and ω_1 are lower and upper band edge frequencies respectively, and ω_B is the bandpass frequency variable. Coupling matrix for proposed bandpass filter is developed from transformed frequency components.

2.3 Matrix Generation and Design of Filter

By taking an example of a fully canonical fourth-degree asymmetric filtering function with 22 dB return loss and four TZs, at $-j3.7431$, $-j1.8051$, $+j1.5699$ and $+j6.1910$. The coefficient of admittance parameter and coupling matrix for bandpass filter is derived as follows (Table 1, Fig. 2).

The coupling matrix for the proposed filter is generated using MATLAB. The simulated response of the proposed filter is plotted in the Fig. 3.

Table 1 Measured value of coefficient of admittance parameter

$Z_S = 0.5 + j0.5,\ Z_L = 0.5 - j0.5$				
s^i i	coefficient of y	coefficient of y_{11n}	coefficient of y_{22n}	coefficient of y_{21n}
0	1.9877	$+j1.8273$	$-j1.8323$	$+j0.9995$
1	$-j0.0489$	+3.3378	+3.2418	$+j0.0226$
2	+3.6063	$+j2.5422$	$+j2.5484$	$+j0.4046$
3	$-j0.0047$	+2.2488	+2.2446	$+j0.0337$
4	+1.0000	$+j0.0005$	$-j0.0005$	$+j0.0152$

5.8333	1.0603	0	0	0	0.0151
1.0600	5.8310	0.8739	0	−0.3259	0.0315
0	0.8739	5.8816	0.8359	0.0342	0
0	0	0.8259	5.7665	0.8723	0
0	−0.3259	0.0342	0.8723	5.8504	1.0595
0.0151	0.0315	0	0	1.0595	5.8333

Fig. 2 Coupling matrix

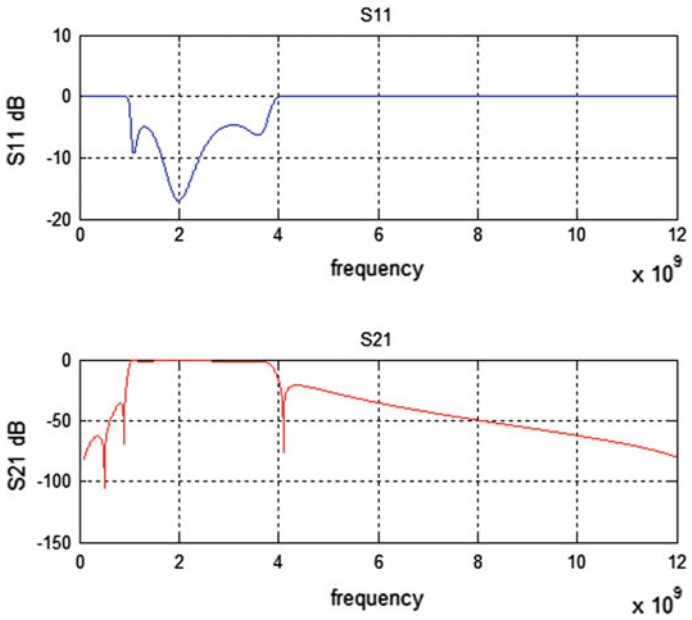


Fig. 3 Response of the proposed filter

This response shows bandpass behavior and satisfied the specifications used in the synthesis of the filter (Fig. 3).

3 Filter Design and Simulation

Once the transverse coupling matrix is generated, the next step is to find the coupling coefficient and spacing between resonators. In general, coupling coefficient between resonators is determined by EM simulation software's. An approach is introduced in [9] to determine coupling coefficient, by establishing a relationship between coupling coefficient and resonant peaks of resonators. Resonant peak is observed when resonators are over-coupled. Two open-loop resonators are over-coupled to find resonant peaks, as shown in Fig. 4.

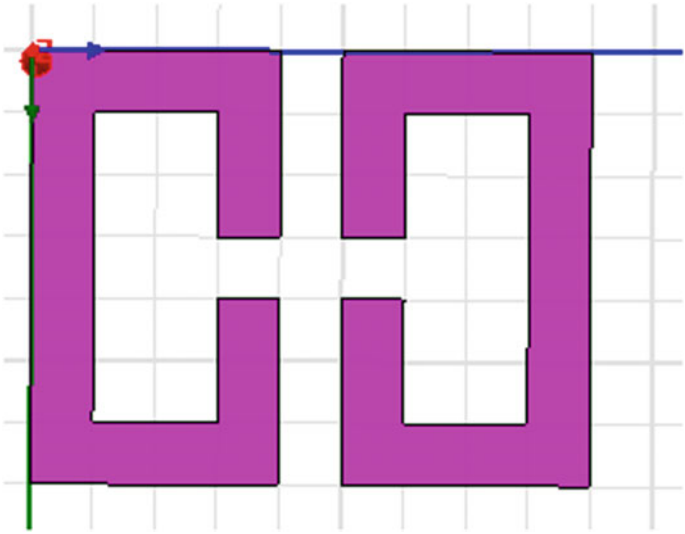


Fig. 4 Electric coupling between resonators

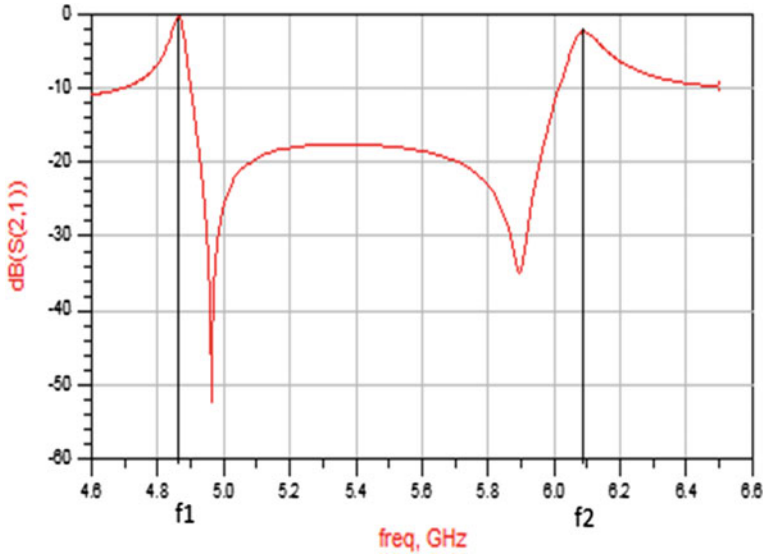


Fig. 5 Resonance curve for determination of coupling coefficient

The frequency response of coupled resonators is shown in Fig. 5.

Relationship between resonating peaks and coupling coefficient is expressed as [9]

$$K = \frac{f_2^2 - f_1^2}{f_1^2 + f_2^2}, \tag{17}$$

where K is coupling coefficient between two resonators and f_1 and f_2 are natural resonant frequencies. The coupling coefficient K is used to determine the spacing between resonators. The relation between and coupling coefficient and spacing between resonators is defined in [9]. The calculated values of f_1, f_2, K and separation(s) are tabulated in Table 2.

The element of coupling matrix determines the nature of coupling between resonators. If the value of element is positive then there is electrical coupling, similarly if the value of element is negative then there is magnetic coupling. However, there is no hard and fast rule for the type of coupling but electrical and magnetic coupling are opposite in nature, that is, if one shows positive value of coupling matrix element then other one shows negative value.

To design proposed filter based on coupling matrix, four resonators are coupled. The coupling configuration between the resonators follows the coupling matrix elements. The configuration of resonators is designed on HFSS, as shown in Fig. 6.

Table 2 Measured value of coupling parameter

Frequency/Separation	Values
f_1	4.95 GHz
f_2	6.10 GHz
K	0.2059
s (separation)	2.01 mm

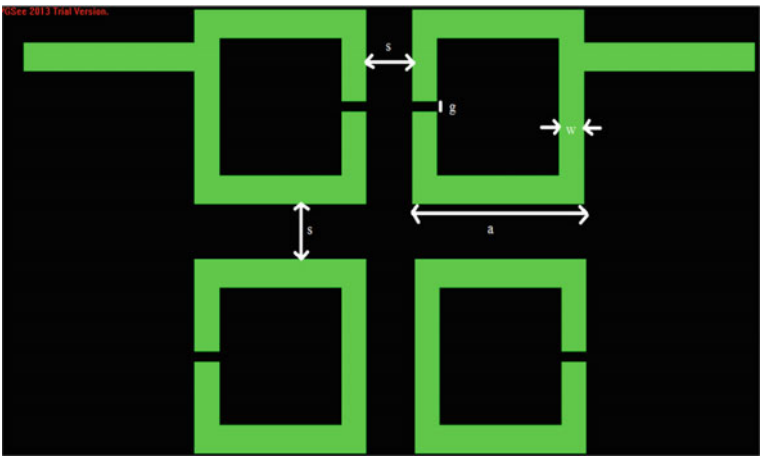


Fig. 6 Layout of bandpass filter

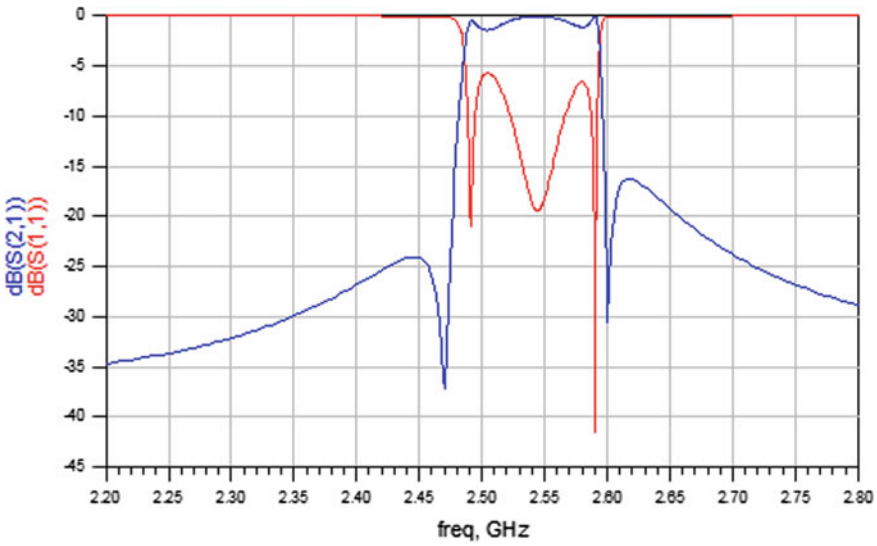


Fig. 7 Response of designed filter

The simulated response of the filter designed on HFSS is shown in Fig. 7. The simulated result found from mathematical modeling in MATLAB shown in Fig. 2 shows good agreement with the response from the HFSS.

4 Conclusions

In this paper, a bandpass filter is synthesized by a coupling matrix method. The method used is independent of the reference impedances at source and load terminals. Designing method is coded on MATLAB to generate coupling matrix and to derive the coupling coefficient and scattering parameter of proposed filter. The proposed bandpass filter is designed and simulated on HFSS for center frequency of 2.56 GHz using generated coupling matrix. A good agreement is seen between MATLAB response and HFSS response of the filter.

References

1. Atia A.E., Williams A. E, and Newcomb R.W.: Narrow-band multiple-coupled cavity synthesis, IEEE Trans. Circuits Syst., Sep. (1974). 649–655.
2. Cameron R.J.: General coupling matrix synthesis methods for Chebyshev filtering functions, IEEE Trans. Microw. Theory Tech., Apr. (1999). 433–442.

3. Cameron R.J.: Advanced coupling matrix synthesis techniques for microwave filters, IEEE Trans. Microw. Theory Tech., Jan. (2003). 1–10.
4. Kozakowski P., Lamecki A., Sypek P., and Mrozowski M.: Eigenvalue approach to synthesis of prototype filters with source/load coupling, IEEE Microw. Wireless Compon. Lett, Feb. (2005). 98–100.
5. Chuan G., Zhu X.W., Jiang X., Xu X.J.: A General Synthesis Approach of Coupling Matrix with Arbitrary Reference Impedances, IEEE Microw Wireless Compon Lett, June (2015).
6. Cameron R.J., Kudsia C.M., and Mansour R.R., Microwave Filters for Communication Systems: Fundamentals, Design and Applications, John Willy & Sons Inc, (2000). 243–27.
7. Amari S.: Synthesis of cross-coupled resonator filters using an analytical gradient-based optimization technique, IEEE Trans. Microwave Theory Tech. (2000). 1559–1564.
8 Kurokawa K.,: Power waves and the scattering matrix, IEEE Trans.Microw. Theory Tech., Mar. (1965).194–202.
9. Hong J. and Lancaster M.J.: Coupling of microstrip square open-loop resonators for cross-coupled planar microwave filters, IEEE Trans Microwave Theory Techniques 44 (1996). 2099–2109.

Combination of EEMD and Morphological Filtering for Baseline Wander Correction in EMG Signals

Deepak Kumar Tiwari, Vikrant Bhateja, Deeksha Anand, Ashita Srivastava and Zaid Omar

Abstract This paper aims at proposing an effective method for Baseline Wander removal from the EMG signals. Ensemble Empirical Mode Decomposition (EEMD) Algorithm is first applied to the baseline corrupted EMG signals to decompose them into Intrinsic Mode Functions (IMFs). After this step, morphological filtering employing octagon-shaped structuring element has been applied to filter out each IMF. Finally, the results of the proposed filtering methodology are compared with those of EMD- and EEMD-based filtering methods. Simulation results report that the methodology used in this study has eliminated the baseline wander from EMG signals with minimal distortions.

Keywords EMG · Baseline wander · EEMD · Morphological filtering

D.K. Tiwari (✉) · V. Bhateja · D. Anand · A. Srivastava
Department of Electronics and Communication Engineering,
Shri Ramswaroop Memorial Group, Lucknow 226028, Uttar Pradesh, India
e-mail: srmdeepaktiwari57@gmail.com

V. Bhateja
e-mail: bhatejavikrant@ieee.org

D. Anand
e-mail: deeksharoma2012@gmail.com

A. Srivastava
e-mail: srivastavaashita95@gmail.com

Z. Omar
Faculty of Electrical Engineering, Universiti Teknologi Malaysia,
81310 Johor Bahru, Malaysia
e-mail: zaidomar@utm.my

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_38

1 Introduction

Electromyogram (EMG) signal is an electrical (biomedical) signal which is emanated whenever the muscles contract and is controlled by the nervous system. Its acquisition is done by the placement of electrodes on the surface of skin or by inserting needle deep inside the muscles [1]. EMG signal proves to be useful for diagnosis and treatment of numerous neuromuscular diseases and fatigue in muscles. For clinical applications, the EMG signal is recorded at low contraction levels so that individual (MUAPs) can be distinguished. However due to reasons such as relative shaking of electrodes, wires with respect to muscles, bad cable fixation, variations found in skin potential which is induced by needle electrodes, the electrical drifts found in equipments used for acquisition; the baseline shifts from its electrical zero which is termed as 'Baseline Wander'. These baseline fluctuations can degrade the signal quality which affects the analysis both qualitatively and quantitatively; therefore its cancelation is required for effective diagnosis [2]. Various techniques have been implemented so far for the effective removal of baseline wander from EMG signal. Carreno et al. [3] proposed a method of filter design by estimating the spectral information of the baseline fluctuation and then a high pass filter was applied to deal with baseline fluctuation. Rampp et al. [4] used Discrete Wavelet Transform (DWT) for removing baseline artifact. It has been reliable in terms of pattern preservation and effectiveness but was found to be computationally intensive. Law et al. [5] applied an approach of nonlinear error modeling for baseline wander removal. It proved to be useful especially in the case when SNR is low. However, it worked only for burst or discrete periods of signal and was not applicable across a time signal universally. Pal et al. [6] proposed baseline removal approach by estimating the spectral information of baseline fluctuation and then utilizing this for designing a high pass butterworth filter. Vergallo et al. [7–9] discussed in their work the application of EMD approach on EEG signals. Verma et al. [10, 11] used morphological filtering with non-flat structuring elements for baseline correction in ECG signals. In the proposed work, an algorithm based on Ensemble Empirical Mode Decomposition (EEMD) along with morphological filtering is used for the effective removal of baseline wander with minimum signal distortion. EEMD overcomes the scale separation problem without introducing a subjective intermittence test and decomposes the EMG signal into IMFs plus a residual signal. Morphological filters are employed on the IMFs to eliminate the baseline noise and maintain the shape of original EMG signal. Signal-to-Noise Ratio (SNR) and Percentage Root-Mean-Square Error Difference (PRD %) have been selected as the two performance metrics for the evaluation and validation of the proposed methodology. These performance metrics also helps in comparing the proposed methodology with other techniques of baseline wander removal. The organization of the rest of the paper is as follows. Section 2 gives a detailed description of the proposed methodology. Section 3 discusses the experimental results and the conclusions are provided under Sect. 4.

2 Proposed Baseline Correction Approach

The proposed methodology aims to combine the EEMD algorithm followed by morphological filtering to eliminate the baseline wander from the corrupted EMG signal. First, the EMG signal undergoes decomposition via Ensemble Empirical Mode Decomposition (EEMD) which converts the multicomponent frequency signal into mono-component frequency signal components. These mono-component frequency signal components known as Intrinsic Mode Functions (IMFs) are then filtered by morphological filters. After that, the filtered IMFs are added together to get the reconstructed baseline removed EMG signal. At the end, the signal fidelity assessment is done by performance metrics SNR and PRD % respectively.

2.1 EEMD

The Empirical Mode Decomposition (EMD), designed especially for nonlinear and nonstationary signals, is a local, data-driven technique which decomposes the signal without any precedent premise about the signal. EMD breaks down a multifrequency component signal into nonoverlapping frequency spectrums called Intrinsic Mode Functions (IMFs) and a residual signal. The IMFs are mono-frequency components that follow two conditions:

- The difference between the number of extrema (including both the local maxima and minima) and zero crossings in the time-series must be not more than one.
- The mean value of the upper envelop (defined by maxima) and lower envelop (defined by minima) is zero through the entire time-series.

EMD being such a capable decomposition technique crops some annoying problems. The fundamental problem with the original EMD is the frequent occurrence of mode mixing, i.e., the detail related to one scale can appear in two different intrinsic modes. To discard the mode mixing problem, a new noise-assisted data analysis (NADA) method introduced by Huang et al. [12], the Ensemble EMD (EEMD), defines the true IMFs as the mean of an ensemble of trials, each consisting of the signal plus a white noise of finite amplitude. The procedural steps of EEMD Algorithm are shown in Fig. 1. The resultant IMFs, namely $c_{ij}(t)$ are averaged across trials to obtain the final IMFs, $c_i(t)$ as

$$c_i(t) = \frac{1}{N}\sum_{j=1}^{N} c_{ij}(t), \tag{1}$$

where, i is the IMF order, j denotes the trial index and N is the total number of trials.

	BEGIN
Step 1:	*Input:* Baseline Corrupted EMG signal.
Step 2:	*Process:* Add a white noise series to the corrupted EMG signal.
Step 3:	*Compute:* All Local Maxima and Minima.
Step 4:	*Compute:* Upper and Lower Envelopes through Cubic Spline function.
Step 5:	*Compute:* Mean of Upper and Lower Envelopes.
Step 6:	*Compute:* Difference by subtracting mean from the noisy signal.
Step 7:	*Process:* Check if the difference is an IMF.
Step 8:	*Compute:* Residue signal by subtracting difference from the noisy signal if it is an IMF otherwise repeat steps 1-7.
Step 9:	*Process:* Check if residue signal is a monotonic function.
Step 10:	*Process:* Repeat steps 1-9 again and again with different versions of noise each time.
Step 11:	*Compute:* Mean (Ensemble) of corresponding decomposed IMFs as the final true IMFs.
	END

Fig. 1 Procedural steps for EEMD algorithm

2.2 Morphological Filter

Morphological filtering signifies nonlinear transformation technique mainly used for locally altering the structural features of a signal using the basic applications of set theory. In this technique, each examined signal can be viewed as a set in Euclidean space and morphological filters are set operations that modify the graph of the signal and can provide a quantitative description of its geometrical shape. An important type of morphological transforms, i.e., hat transforms can be used for detailed extraction of signal. Proper selection of structuring element is a very important step for extracting the features from the original EMG signal. Also, the size of the structuring element should be selected with proper care as its inaccurate selection may deform the adjoining wave of the EMG signal [13]. In the proposed methodology, octagon-shaped structuring element of radius 3 as shown in Fig. 2 is chosen. Baseline wander which is an artifact of low frequency is being eliminated by the help of morphological operators that constitute both high pass and low pass filter characteristics. Therefore, the proposed methodology uses top-hat filtering and bottom-hat filtering for the effective removal of baseline drift. The respective expressions of top-hat transform and bottom-hat transform is given by

$$T_h = c_i - (c_i \circ b) \tag{2}$$

$$B_h = (c_i \bullet b) - c_i, \tag{3}$$

where, T_h and B_h represent top-hat and bottom-hat transforms, c_i represents the decomposed IMFs and b is the structuring element.

Top-hat filtering and bottom-hat filtering of the IMFs decomposed from the baseline distorted EMG signal is done which generates peaks and valleys

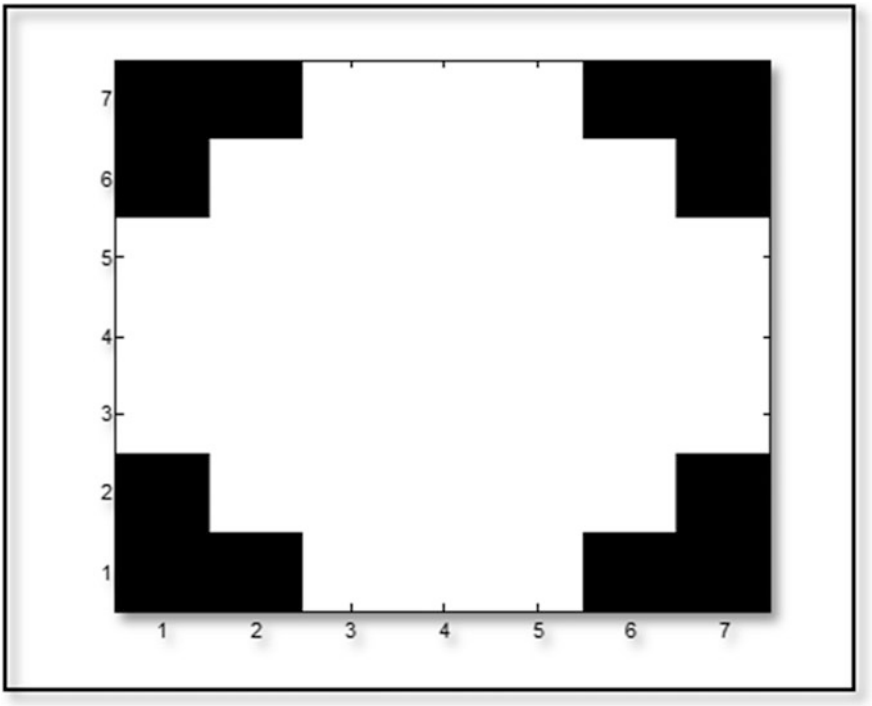


Fig. 2 Octagon structuring element of radius 3

respectively followed by subtraction of valleys from the peaks. This whole process is repeated for each IMF and after that the filtered IMFs are added to get the baseline removed EMG signal.

3 Results and Discussions

In the proposed methodology, the EMG signals are taken from The UCI Machine Learning Repository [14] including 10 normal and 10 aggressive physical actions that measure the human activity. During simulations, these EMG signals were first converted into column vector followed by the decomposition process using the EEMD Algorithm as discussed in the preceding section. After this, the decomposed IMFs were filtered using morphological filters and the filtered IMFs were reconstructed for the baseline wander removal. The decomposed IMFs using the EEMD Algorithm have been shown in Fig. 3.

The number of iterations and the noise parameter needs to be considered for applying EEMD Algorithm. Herein, ensemble number (NE) is selected 10. The noise parameter (Nstd), defined as the ratio of the standard deviation of noise to the

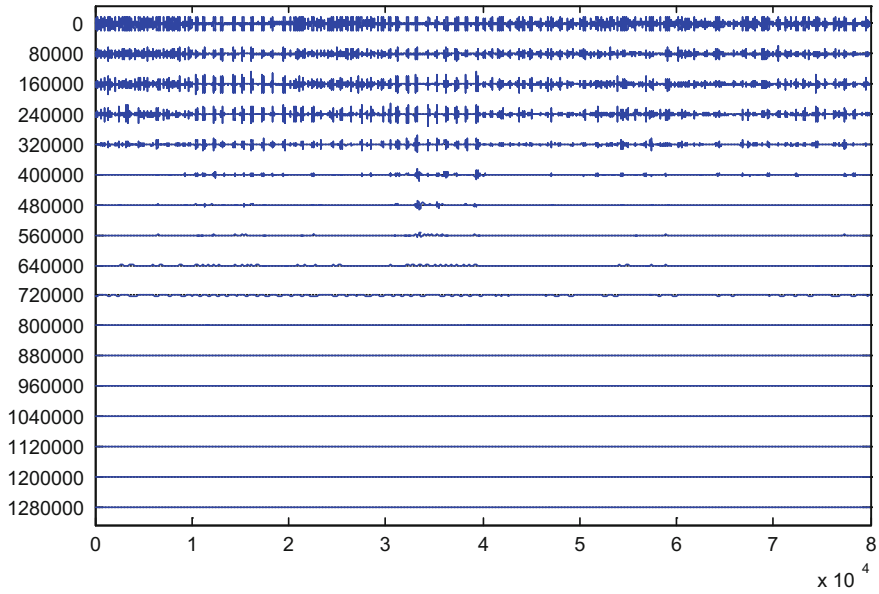


Fig. 3 IMFs obtained from EEMD algorithm

standard deviation of the signal power, is selected to be 0.2. An 'octagon' shaped structuring element with radius of 3 is chosen which gives the best result. The results of the baseline corrected EMG signals using the proposed methodology along with the outputs of the other techniques (EMD and EEMD) are shown in Fig. 4. Figure 4a shows an original EMG signal (Pushing4) which is already baseline drifted. It can be seen from Fig. 4b and c that the baseline corrected signals using the EMD and EEMD techniques are almost the same that is the exact replica of the original signal as the signal properties remains the same. But there is an improvement in the output of the proposed methodology over the other two methods. In this, since morphological filtering employing top-hat filtering and bottom-hat filtering is used along with the EEMD algorithm thus the baseline throughout the whole signal is brought to a zero reference which is clearly seen in Fig. 4d.

Furthermore, SNR and PRD % has been used as the two performance metrics for the evaluation and validation of the proposed methodology. The comparison of SNR and PRD % values of the baseline corrected signal using the proposed methodology with the EMD- and EEMD-based techniques has been shown in Tables 1 and 2 respectively.

Signal-to-noise ratio is a parameter which evaluates the improvement in the signal quality with respect to noise. The SNR of the proposed methodology for signal (S1) is reported to be 63.2500 dB which is much better as compared to EMD

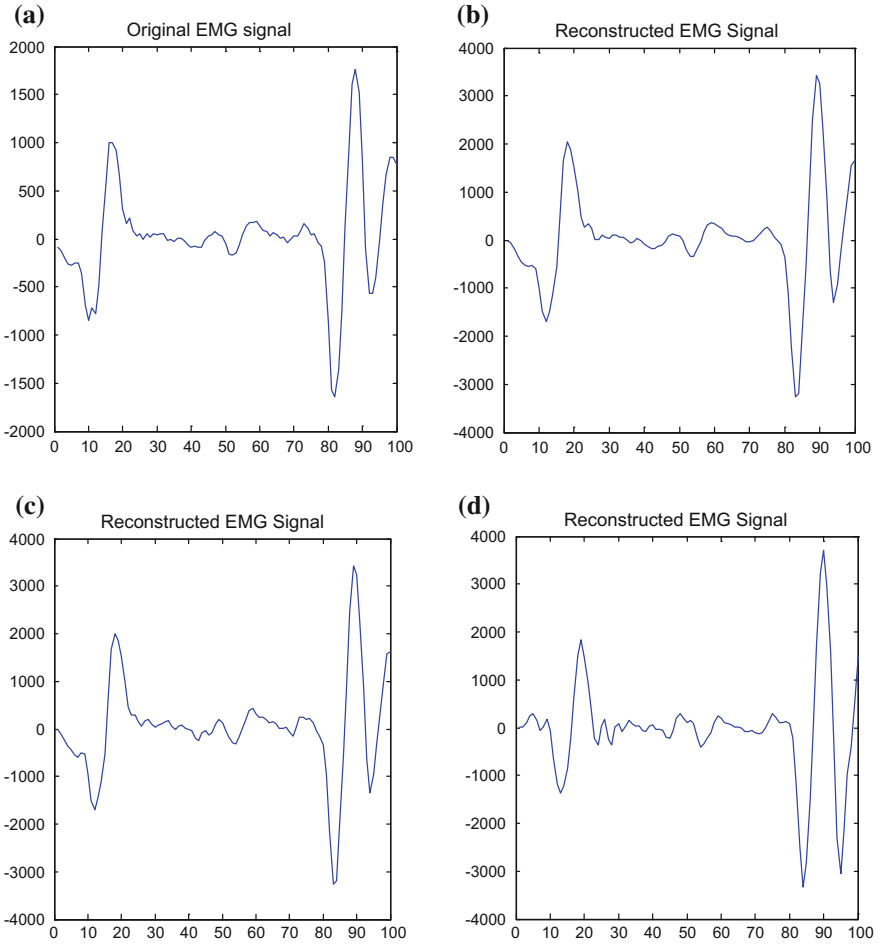


Fig. 4 **a** Original EMG signal (pushing 4), **b** EMD output signal, **c** EEMD output signal, **d** Proposed methodology output

Table 1 Comparison of SNR (in dB) of different existing methods used for baseline correction with the proposed methodology

EMG signal ref. no.	Original	EMD [15]	EEMD [15]	Proposed methodology
S1	−41.2400	−40.9150	−40.9091	62.3500
S2	−54.4346	−54.3271	−54.1080	55.0471
S3	−101.9355	−100.2435	−91.5264	−62.6738
S4	−50.3090	−50.2436	−50.1838	55.9229
S5	−65.1993	−64.9756	−64.4496	63.2815

Table 2 Comparison of PRD % values of different existing methods for baseline correction with the proposed methodology

EMG signal ref. no.	EMD [15]	EEMD [15]	Proposed methodology
S1	0.4944	0.4942	0.4752
S2	0.7506	0.7504	0.4518
S3	0.5557	0.5551	0.5298
S4	0.4074	0.4071	0.3924
S5	0.4765	0.4761	0.4731

and EEMD techniques in which the SNR is increased by only unity. Similar results are obtained for other signals also, i.e., S2–S5; wherein the proposed methodology certainly performs better with respect to the other two techniques.

4 Conclusion

This paper presented an approach for the elimination of baseline wander from EMG signals based on EEMD followed by morphological filtering. The EEMD algorithm effectively decomposes the EMG signal in time domain allowing varying frequency in time to be preserved. On the other hand, morphological filtering successfully removes the baseline wander with minimum distortion of the original EMG signal. The performance of this approach was compared with the existing EMD and EEMD algorithms [15]. This methodology achieved better results than the other two methods. The baseline drift was easily detected and removed from the decomposed IMFs. The proposed methodology outperforms the existing EMD- and EEMD-based methods in terms of both SNR and PRD % values.

References

1. Luca, C. J. D., Gilmore, L. D., Kuznetsov, M., Roy, S. H.: Fitering the Surface EMG Signal: Movement Artifact and Baseline Noise Contamination, Journal of Biomechanics, vol. 43, pp. 1573–1579, (2010).
2. Luca, C. J. D., Adam, A., Wotiz, R., Gilmore, L. D., Nawab, S. H.: Decomposition of Surface EMG Signals, Journal of Neurophysiology, vol. 96, pp. 1646–1657, (2006).
3. Carreno, I. R., Trigueros, A. M., Useros, L. G., Irujo, J. N., Falces, J. R.: Filter Design for Cancellation of Baseline Fluctuation in Needle EMG Recordings, Journal of Computer Methods and Programs in Biomedicine, vol. 8, pp. 79–93, (2005).
4. Rampp, S., Prell, J., Thielemann, H., Posch, S., Strauss, C., Romstock, J.: Baseline Correction of Intraoperative Electromyography using Discrete Wavelet Transform, Journal on Clinical Monitoring and Computing, vol. 21, no. 4, pp. 219–226, (2007).
5. Law, L.F., Krishnan, C., Avin, K.: Modelling Nonlinear Errors in Surface Electromyography Due to Baseline Noise: A New Methodology, Journal of National Institute of Health, vol. 44, no. 1, pp. 202–205, (2011).

6. Pal, S., Pal, G. P.: Removal of Baseline Fluctuation from EMG Recordings, International Journal of Engineering Research and Applications, vol. 1, no. 3, pp. 449–455, (2012).
7. P. Vergallo, A. Lay-Ekuakille, N. I. Giannoccaro, A. Trabacca, F. C. Morabito, S. Urooj and V. Bhateja, "Identification of Visual Evoked Potentials in EEG detection by Emprical Mode Decomposition," Proc. (IEEE) 11th International Multi-Conference on Systems, Signals and Devices- Conference on Sensors, Circuits & Instrumentation Systems, Castelldefels-Barcelona, Spain, pp. 1–5, February 2014.
8. P. Vergallo, A. Lay-Ekuakille, S. Urooj and V. Bhateja, "Spatial Filtering to Detect Brain Sources from EEG Measurements," Proc. (IEEE) International Symposium on Medical Measurements and Applications, Liboa, Portugal, pp. 1–5, June 2014.
9. A. Lay-Ekuakille, P. Vergallo, G. Griffo, F. Conversano, S. Casciaro, S. Urooj, V. Bhateja and A.Trabacca, "Mutidimensional Analysis of EEG Features using Advanced Spectral Estimates for Diagnosis Accuracy," Proc. of IEEE International Symposium on Medical Measurements and Applications (MeMeA-2013), Gatineau (Quebec), Canada, pp. 237–240, May 2013.
10. R. Verma, R. Mehrotra and V. Bhateja, "A New Morphological Filtering Algorithm for Pre-Processing of Electrocardiographic Signals," Proc. of (Springer) 4th International Conference on Signal and Image Processing (ICSIP 2012), Coimbatore, India, vol. 1, pp. 193–201, December 2012.
11. R. Verma, R. Mehrotra and V. Bhateja, "An Improved Algorithm for Noise Suppression and Baseline Correction of ECG Signals," Proc. of (Springer) International Conference on Frontiers in Intelligent Computing Theory and Applications (FICTA 2012), Bhubaneswar, India, AISC vol. 199, pp. 733–739, December 2012.
12. Wu, Z., Huang, N. E.: Ensemble Empirical Mode Decomposition: A Noise Assisted Data Analysis Method, Advances in Adaptive Data Analysis, vol. 1, no. 1, pp. 1–51, (2005).
13. V. Bhateja, R. Verma, R. Mehrotra and S. Urooj, "A Non-linear Approach to ECG Signal Processing using Morphological Filters," International Journal of Measurement Technologies and Instrumentation Engineering (IJMTIE), IGI Global, vol. 3, no. 3, pp. 46–59, Jan 2014.
14. UCI Machine Learning Repository.
15. Zhang, X., Zhou, P.: Filtering of Surface EMG using Ensemble Empirical Mode Decomposition, Journal of Medical Engineering and Physics, vol. 35, no. 4, pp. 537–542, (2014).

ANN-Based Classification of Mammograms Using Nonlinear Preprocessing

Ananya Tiwari, Vikrant Bhateja, Aman Gautam and Suresh Chandra Satapathy

Abstract Preprocessing and enhancement of mammograms is necessary to improve the visual quality and detectability of the anomalies present in the breasts. In this work, a nonlinear logistic function has been applied for enhancement (preprocessing) of mammograms. To define the texture of the detected anomaly gray level cooccurrence matrix (GLCM) features are formulated. Lastly, a feed-forward artificial neural network (FF-ANN) is used as a classification tool for segregating the mammogram into normal or abnormal. A set of four confusion matrices regarding the learning, testing and validation of the classifier has been computed to analyze the performance of classifier at each stage. The proposed classifier approach has reported of considerably better accuracy in comparison to other existing approaches.

Keywords Contrast enhancement · Feedforward artificial neural networks (FF-ANN) · GLCM · Region of interest (ROI)

A. Tiwari (✉) · V. Bhateja · A. Gautam
Department of Electronics and Communication Engineering,
Shri Ramswaroop Memorial Group, Lucknow 226028, Uttar Pradesh, India
e-mail: absoluteananya@gmail.com

V. Bhateja
e-mail: bhatejavikrant@ieee.org

A. Gautam
e-mail: gautamaman543@gmail.com

S.C. Satapathy
Deparment of Computer Science & Engineering, PVP Siddhartha Institute
of Technology, Vijayawada, Andhra Pradesh, India
e-mail: sureshsatapathy@ieee.org

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_39

1 Introduction

Breast cancer possesses an uncoordinated growth of the developed tumor region; with an unknown root cause of this illness leading to a high mortality rate. The analysis of mammograms (X-ray image of the breast) is mostly done by experienced radiologists, who play a keen role in determining the features and shape(s) of the lesions present. However, the human factor results in a low precision outcome [1]. To improve the analysis of the radiologists, a correlation with computer-based techniques is needed, which can be used for analysis, detection or the overall diagnosis of breast cancer. Computer-based diagnosis systems, however, are not self-generating in nature but they can be actively used by the radiologists so that the final decision is made faster and with a greater degree of accuracy. Another problem faced by the radiologist is that during the screening of mammograms, the image obtained from the X-ray machine having low contrast is extremely marginal. In poor quality images, the slight dissimilarity between the normal and malignant tissue is not distinguishable, and thus it becomes difficult on the radiologists' part to give accurate results. Thus, enhancement of the mammogram becomes essential after the screening of mammograms has been done [2]. Some related works and studies have been done in the past for the contrast improvement and classification of the mammograms. Tzikopoulosa et al. [3] performed breast density estimation over the mammograms for its segmentation and used SVM classifier for classification. The processing time of the approach was its limitation yielding an accuracy of 85.7%. Wu et al. [4] used a Laplacian Gaussian pyramid algorithm followed by a contrast limited adaptive histogram equalization (CLAHE) for contrast improvement. The denoising of the mammogram was not performed due to which the SNR value was low as compared to other approaches mentioned in their work. Sriramkumar et al. [5] worked on identifying microcalcifications present in digital mammograms. They divided the overall image into several small patches and analyzed its textural behavior using GLCM features. As the number of patches was increased for the mammogram the accuracy was improved but the complexity and computation time was increased. Wang et al. [6] performed CAD based visual enhancement of mammograms by removing major background tissues by applying image matting. Al-Najdwai et al. [7] performed a four class classification of mammograms. They used a combination of CLAHE and median filter for the contrast improvement. The proposed approach increased the pixel intensity of the background along with the tumorous region which reduced the detectability of the anomalous entity. Recently nonlinear polynomial filters [8, 9] and nonlinear unsharp Masking [10] approaches are also deployed for preprocessing of mammograms. In this paper, a nonlinear preprocessing algorithm has been used to improve the overall contrast of the image without affecting the information present in the original mammographic image. To define the textural features of the anomaly four GLCM features are computed. For final classification module, a neural network based on feedforward classification technique has been used. The detailed

explanation of the methodology, analysis and discussions of results along with conclusions are mentioned in the sub sections to follow.

2 Proposed Methodology

The proposed CAD system comprises of three modules such as preprocessing, features extraction, and classification. First, the input mammogram is fed for preprocessing where RGB to gray conversion and enhancement process takes place. This module uses a nonlinear enhancement based preprocessing technique which suppresses background and refines the contrast of the foreground containing the tumor present in the breast. Block diagram shown in Fig. 1 depicts the proposed methodology.

Second, the detected ROI is sent to a features extraction module where a structure of quantitative data is obtained by calculating various attributes such as energy, entropy, and correlation, etc., for final classification. Lastly, the selected features are provided to FF-ANN classifier which categorizes the detected ROI into normal and abnormal.

2.1 Preprocessing Using Nonlinear Enhancement

For noise free enhancement of mammograms, a logistic function is used for nonlinear processing. It is given by Eq. (1).

$$\log istic\,(x) = \frac{1}{1+e^{-x}} \tag{1}$$

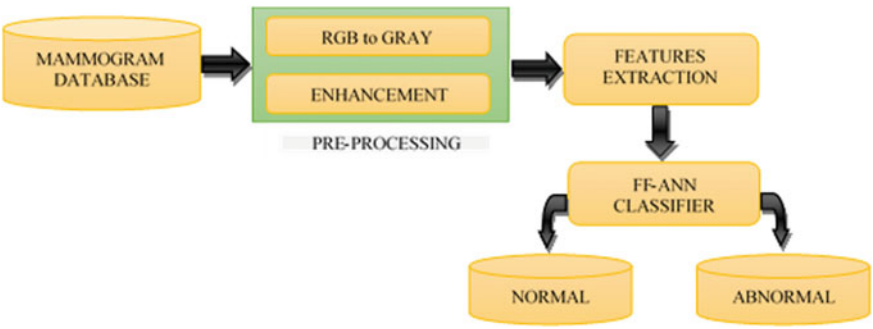


Fig. 1 Block diagram of proposed methodology to classify normal and abnormal and mammograms

The function modifies the mammogram by defining a certain threshold, pixels having magnitude above this threshold are enhanced while the rest are suppressed. The enhancement using the aforesaid function has been carried out by combining the function of Eq. (1) in a linear fashion along with a gain parameter as given in Eq. (2).

$$y(x) = a[\log istic\{k(x-b)\} - \log istic\{-k(x+b)\}] \tag{2}$$

where x indicate the intensity of gray level for original ROI at coordinate (i, j) and parameter a is given by Eq. (3).

$$a = \frac{1}{\log istic\{k(1-b)\} - \log istic\{-k(1+b)\}} \tag{3}$$

where $b \in R$ while $k \in N$ and parameter b (where $0 < b < 1$, $b \in R$) manages the threshold value while, parameter k [1] governs the effective contrast enhancement of the mammogram.

2.2 Features Extraction and Classification

The abnormal breast tissues reveal distinct characteristics as compared normal tissues. Therefore, before the classification procedure, features of detected ROI(s) should be extracted. GLCM is an analytical method of examining the texture of detected anomalies by considering the structural correspondence of pixels. It calculates how frequently does a pair of pixel occur in an image within a specified structural network to categorize the texture [11]. For each GLCM, four Haralick features are calculated which provide textural information of the ROI are enlisted in Table 1 on next page. These four features are fed to a FF-ANN for final diagnosis. FF-ANN is an artificial neural network where the movement of information is in only one direction. The features extracted are sent to the input node, hidden nodes performs different algorithm for classification, and the final result is shown at output node. It is based on training and testing mechanism where first the neural network is trained with a separate database and then its learning is tested with single input of images.

Table 1 Description of haralick features used in proposed methodology

Features	Description
Contrast	Refers to the local variations in the GLCM
Correlation	Measures gray tone linear dependencies in the image
Energy	Measures the order of the image
Homogeneity	Measures the similarity of pixels

3 Results and Discussions

In proposed methodology, the digital mammograms are taken from the cancer imaging archive (TCIA) [12] which provides a classified set of images (for cancer anomalies) available publically as a weblink. The same has been widely used for researches pertaining to cancer imaging. During simulations, these mammograms are normalized by performing RGB to gray conversion followed by enhancement process using nonlinear transformation as discussed in the previous section.

The results of enhanced mammograms using the proposed nonlinear enhancement function are shown in Fig. 2. Figure 2a shows an original mammogram (Mam#1) which is containing a malignant mass. After enhancement, it is observed

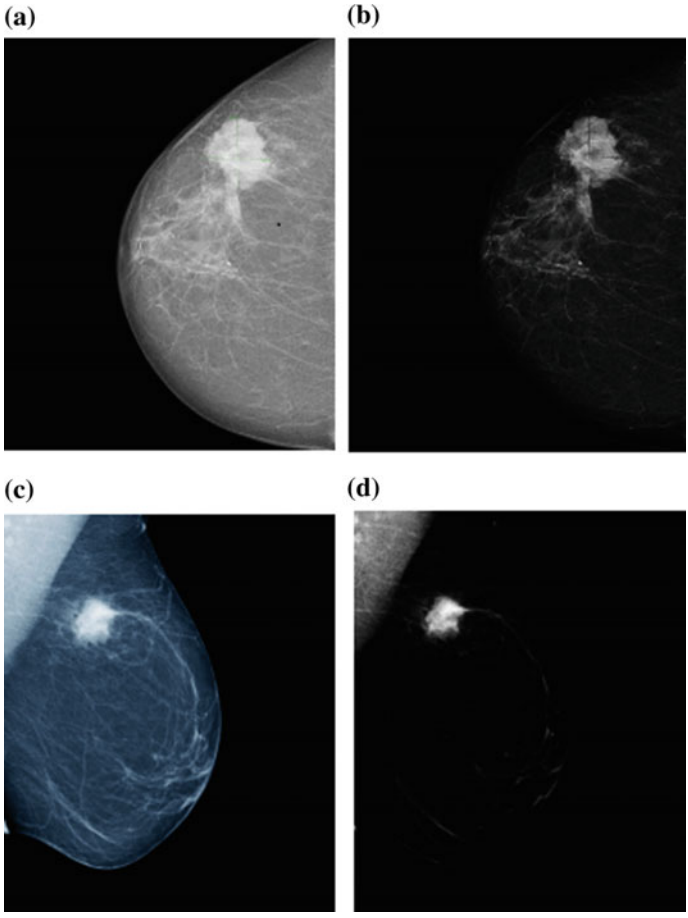


Fig. 2 **a** Original mammogram Mam#1, **b** enhanced Mam#1, **c** mammogram with tumor Mam#2, **d** enhanced Mam#2

that the background is suppressed while the contrast is improved and the targeted ROI is very clearly visible as shown in Fig. 2b here, the distorted boundaries indicates the presence of malignancy in the mass. Similarly, Fig. 2c shows another mammogram (Mam#2) containing tumor whose enhanced image is shown in Fig. 2d. These enhanced ROI is now suitable for features extraction at the next stage. Now the enhanced and segmented ROI is used for features extraction where

Table 2 Simulation parameter(s) of FF-ANN

Features	Selected values
Number of neurons	10
Number of hidden layers	50
Type of thresholding	Log-sigmoidal
Epoch	22 iterations

Fig. 3 Confusion matrices of enhanced mammograms

Table 3 Comparison of accuracy of proposed methodology with other existing approaches

Approaches used	Classification accuracy (%)
S. Saini et al. (2015)	87.5
K. Vadehi et al. (2015)	91.51
Proposed methodology	97

four GLCM features are extracted namely contrast, homogeneity, energy, and entropy. These features are given as inputs to FF-ANN comprising the following set of input simulation parameters as shown in Table 2.

The FF-ANN has been simulated to be used for training validation and finally testing. The performance of the classifier obtained at each of these stages can be communicated using the confusion matrices shown in Fig. 3. Based on Fig. 3, the performance of the classifier during training, validation, and testing can be analyzed from the first three matrices. The last matrix named "All Confusion Matrix" portrays the overall decision making capability of the classifier.

Accuracy is the ability to detect cancerous and non-cancerous masses which are identified as such. The accuracy of the proposed approach is reported to be 97% with a false positive score of 1.9% and true negative of 33.3%. A false positive score determines the incorrect identification of a non-cancerous mass as cancerous whereas, a true negative score informs the correct identification of non-cancerous mass as such. In the proposed work, not only the accuracy of detecting a cancerous mass is high but also the incorrect classification of non-cancerous mass is low. These obtained results are considerably better in comparison to the works reported in [13, 14] as depicted in Table 3. The results of the proposed work affirm an improvement in the classification performance of the overall system and are quite promising.

4 Conclusion

In the proposed work, a nonlinear enhancement approach for contrast improvement of mammogram has been deployed. The prime advantage of this method with respect to the other approaches mentioned in the literature is its ability to improve the pixel intensity in only the anomalous region. Also, it reduces the necessity for further segmentation of mammogram as the ROI is well defined after the enhancement procedure only. The simulation results of the classifier show that with enhancement of mammograms, the classification accuracy is optimized and is proved to be better in comparison to other state of art approaches. Future development of the presented research concerns with the improvement of the adaptability of the proposed algorithm. The mentioned technique can be incorporated in the conventional CAD system under the preprocessing module to achieve precise diagnosis of breast cancer.

References

1. Jain, A., Singh, S., Bhateja, V.: A Robust Approach for Denoising and Enhancement of Mammographic Breast Masses, In: International Journal on Convergence Computing, vol. 1, no. 1, pp. 38–49, Inderscience Publishers (2013).
2. Bhateja, V., Urooj, S., Misra, M.: Technical Advancements to Mobile Mammography using Non-Linear Polynomial Filters and IEEE 21451-1 Information Model, In: IEEE Sensors Journal, vol. 15, no. 5, pp. 2559–2566, Advancing Standards for Smart Transducer Interfaces (2015).
3. Tzikopoulosa, S. D., Mavroforakisb, M. E., Georgioua, H. V., Dimitropoulosc, N., Theodoridisa, S.: A Fully Automated Scheme for Mammographic Segmentation and Classification based on Breast Density and Asymmetry, In: Computer Methods and Programs in Biomedicine, vol. 102, no. 1, pp. 47–63, 2011.
4. Shibin Wu, Yu, S., Yang, Y., Xie, Y.: Feature and Contrast Enhancement of Mammographic Image Based on Multiscale Analysis and Morphology, In: Computational and Mathematical Methods in Medicine, vol. 2013, pp. 1–8, Hindawi Publishing Corporation (2013).
5. Sriramkumar, D., Malmathanraj, R.: Mammogram Tumour Classification using Modified Segmentation Techniques, In: Biomedical Engineering and Technology, vol. 13, no. 3, pp. 218–239, 2013.
6. Wang, H., Li, J. B., Wu, L., Gao, H.: Mammography Visual Enhancement in CAD-based Breast Cancer Diagnosis, In: Clinical Imaging, vol. 37, no. 2, pp. 273–282, 2013.
7. Al-Najdawia, N., Biltawib, M., Tedmori, S.: Mammogram Image Visual Enhancement, Mass Segmentation and Classification, In: Applied Soft Computing, vol. 35, pp. 175–185, 2015.
8. Bhateja, V., Misra, M., Urooj, S., Lay-Ekuakille, A.: A Robust Polynomial Filtering Framework for Mammographic Image Enhancement from Biomedical Sensors, In: IEEE Sensors Journal, vol. 13, no. 11, pp. 4147–4156, IEEE (2013).
9. Bhateja, V., Misra M., Urooj, S.: Non-Linear Polynomial Filters for Edge Enhancement of Mammogram Lesions, In: Elsevier-Computer Methods and Programs in Bio-medicine, vol. 129C, pp. 125–134, Elsevier (2016).
10. Bhateja, V., Misra, M., Urooj, S.: Human Visual System based Unsharp Masking for Enhancement of Mammographic Images. In: Journal of Computational Science (2016).
11. Mohamed, H., Mabroukb, M. S., Sharawy, A.: Computer Aided Detection System for Micro Calcifications in Digital Mammograms, In: Computer Methods and Programs in Biomedicine, vol. 116, no. 3, pp. 226–235, April 2014.
12. The Cancer Imaging Archive (TCIA). Available Online at: http://www.cancerimagingarchive.net/ updated on 31st August, 2016.
13. Saini, S., Vijay, R.: Mammogram Analysis Using Feed-Forward Back Propagation and Cascade-Forward Back propagation Artificial Neural Network. In: 5th IEEE International Conference on Communication Systems and Network Technologies, pp. 1177–1180, IEEE, Gwalior (2015).
14. Vadehi, K., Subashini, T. S.: Automatic Classification and Retrieval of Mammographic Tissue Density using Texture Features, In: IEEE Sponsored 9th International Conference on Intelligent Systems and Control (ISCO 2015).

Performance of Firefly Algorithm for Null Positioning in Linear Arrays

Md. Javeed Ahammed, A. Swathi, Deepika Sanku, V.V.S.S.S. Chakravarthy and H. Ramesh

Abstract In this paper, linear array (LA) synthesis for desired nulls is performed using firefly algorithm (FFA). The undesired signals are often termed as interference approaching the radiating system in certain directions. It is possible to reject these signals thereby avoiding potential interference by simply placing nulls in the direction of arrival of interference in the respective radiation pattern of the antenna array. In order to demonstrate this, single and multiple nulls are obtained using FFA in linear arrays. The radiation patterns are obtained for both single and multiple nulls when the beam is positioned from 0° to 30° which typically refers to scanned and unscanned beams.

Keywords FFA · Linear array · Null positioning · Optimization

Md. Javeed Ahammed (✉) · H. Ramesh
Department of ECE, Paladugu Parvathi Devi College of Engineering & Technology, Nunna, Vijayawada, India
e-mail: ahammed.javeed@gmail.com

H. Ramesh
e-mail: ramesh.harimanikyam@gmail.com

A. Swathi · V.V.S.S.S. Chakravarthy
Department of ECE, Raghu Institute of Technology, Visakhapatnam, AP, India
e-mail: swathiarinana@gmail.com

V.V.S.S.S. Chakravarthy
e-mail: sameersree@gmail.com

D. Sanku
Department of ECE, AUCE (A), Andhra University, Visakhapatnam, India
e-mail: sankudeepika@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_40

1 Introduction

Antenna arrays are always been a better choice for enhanced directivity which is an essential property in wireless communication. In addition to this, the array of antennas is capable of producing desired radiation patterns in accordance with the requirement and application. Several features like beam steering, scanning, side lobe level suppression, beam width control and shaped patterns are possible with arrays. Several conventional numerical techniques [1–6] are employed to achieve the above features. However, they failed to give the optimum result as they often end up with local minima. This is certainly a drawback, as the complete efficiency of the array antenna is not achieved. As a result, in order to obtain better response, several nature inspired metaheuristic algorithms are proposed for antenna array synthesis problems [7–14]. In array synthesis, the problem statement can be defined as to determine optimal set of amplitudes of current excitation at each element in the array which produces desired pattern. The desired pattern in the present work is to achieve nulls in the desired directions under scanned and unscanned conditions. In this paper, according to the problem statement the amplitude distribution is obtained using firefly algorithm (FFA). Further in the paper, the description of the problem formulation is given in Sect. 1. The FFA is briefly described in Sect. 2. The implementation part is described in Sect. 3. The results and discussions are presented in Sect. 4. Overall conclusion on the work presented are mentioned in conclusion, i.e. Sect. 5.

2 Problem Formulation

Formulation of array factor and the cost function play a key role in the problem statement modelling. In this section, the description of both the formulations is given as follows.

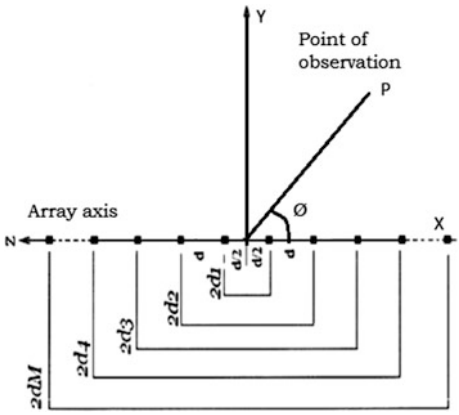
2.1 Array Factor of Linear Array

The geometry of a simple linear array in which the elements are distributed symmetrically on either sides of the reference position is as shown in Fig. 1. Symmetrical distribution functionally means that the current distribution is also symmetric.

The array factor formulation of the linear array is as follows.

$$AF(\theta) = 2\sum_{n=1}^{N} A_n \cos\left[\mathrm{kd}_n \cos\theta + \beta_n\right] \tag{1}$$

Fig. 1 Linear array geometry



Where n is the element number, N refers to total number of elements in the array, d refers to inter-element spacing, and β is the progressive phase constant.

3 Firefly Algorithm

FFA is a novel metaheuristic algorithm inspired by the behaviour of fireflies [15]. It is proposed by Xin-She Yang. It is another swarm intelligence based algorithm which is inspired by the phenomenon of bioluminescent communication.

The following are a set of rules proposed and framed as an algorithm [15].

- Fireflies (FF) are unisex and can attract any fellow FF.
- Attractiveness depends on ones brightness.
- The brightness or light intensity of a firefly is influenced by the landscape of fitness/cost function.

The basic steps of the FA can be summarised as the pseudo code in Fig. 2.

4 Array Design Using Firefly Algorithm

The implementation of the algorithm for the array design problem is explained in several steps as discussed below.

```
Begin
    1. Initialisation max iteration, α, β_o, γ
    2. Generate initial population
    3. Define the Objective function f(x),
    4. Determine Intensity (I) at cost (x) of each individual determined by f(x_i)
    5. While (t < Iter max)
                For i=1 to n
                    For j=1 to n
                        if (I_j > I_i)
                            Move firefly i towards j in K dimension
                        end if
                    Evaluate new solutions and update light intensity
                end for j
            end for i
        Rank the fireflies and find the current best
    end while
    6. Post process results and visualization
End procedure
```

Fig. 2 Pseudo code for firefly algorithm

4.1 Population Initialization

A finite number (P) of fireflies are initialized randomly in the K variable (dimensional) search space. These constitute initial solutions. They are further improved by an iterative process which terminates ether when the best solution is found or when maximum number of iterations is achieved. The selection of population size depends on the specific optimization problem. For the current linear array synthesis, the K dimensional search space includes K variables representing the amplitudes of current excitation of each element.

This is represented as a vector

$$x_i = [x_1, x_2, x_3 \ldots x_K] \tag{2}$$

The population matrix is given as

$$X = \begin{bmatrix} x_1 \\ x_2 \\ \cdot \\ \cdot \\ x_P \end{bmatrix} = \begin{bmatrix} x_{11}\ x_{12} \ldots x_{1K} \\ x_{21}\ x_{22} \ldots x_{2K} \\ \ldots\ldots\ldots\ldots\ldots \\ \ldots\ldots\ldots\ldots\ldots \\ x_{P1}\ x_{P2} \ldots x_{PK} \end{bmatrix} \tag{3}$$

Range of the search space variables is mentioned as

$$x_{min} < x_i < x_{max} \tag{4}$$

4.2 Firefly Evaluation

FF evaluation means to evaluate the fitness of the FF and the corresponding amplitude distribution.

$$I_i = \text{ObjFunc}\,(x_i)$$

4.3 Attractiveness

The calculation of the attractiveness of a FF can is given by

$$\beta\,(r) = \beta_o * \exp\left(-\gamma r_{ij}^2\right) \tag{5}$$

where

r refers to the distance
β_0 refers to initial attractiveness
γ refers to absorption coefficient.

4.4 Movement

FF tend to move towards more attractive FF. This movement is modelled as

$$x_i = x_i + \beta_o * \exp\left(-\gamma r_{ij}^2\right) * \left(x_j - x_i\right) + \alpha * (\text{rand} - 1/2) \tag{6}$$

5 Results and Discussion

The entire simulation based experimentation is divided in to four cases. Description of the problem statement and the corresponding radiation pattern plots are given case-wise in the following discussion.

5.1 Case-1

In this, a simple linear array is synthesised with desired nulls at one positions, i.e. at 20°. Due to the inherent symmetry a similar null appears on the other side of the pattern at −20° also. The radiation pattern obtained for the amplitude distribution determined by the FFA is presented in the Fig. 3. A null at 20° with null depth of less than −80 dB can be observed. The corresponding amplitude distribution is as given int he first column of Table 1.

5.2 Case-2

In this case multiple nulls are considered. The objective of this case involves in positioning the second null at 40° in addition to the earlier existing null. The validation and the effectiveness of the algorithm is evident with this kind of effort to generate the null which doesn't appears in the previous case protecting the existing null. The corresponding radiation pattern is as shown in the Fig. 4. The amplitude distribution is as mentioned in the Table 2.

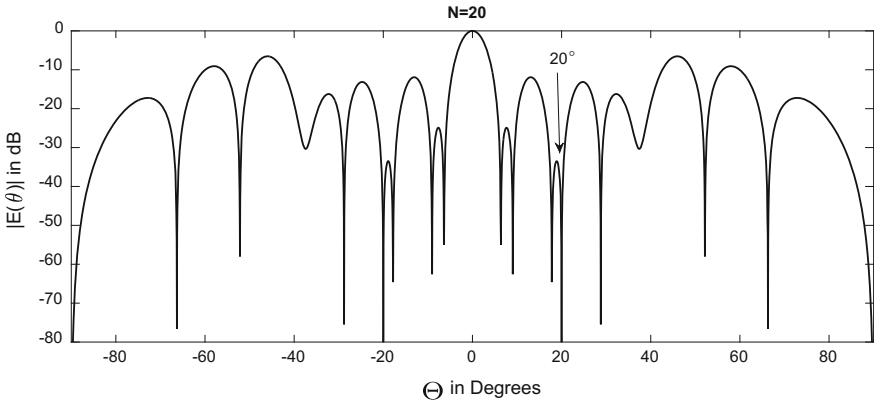


Fig. 3 Radiation pattern with null 20°

Table 1 Parameter benchmarking for FFA

Description	Parameter	Typical value
Maximum attractiveness	β_0	1
Time varying algorithm parameter initial value	α	0.25
Absorption coefficient	γ	1
Swarm size	P	30
Number of iterations	iter	250

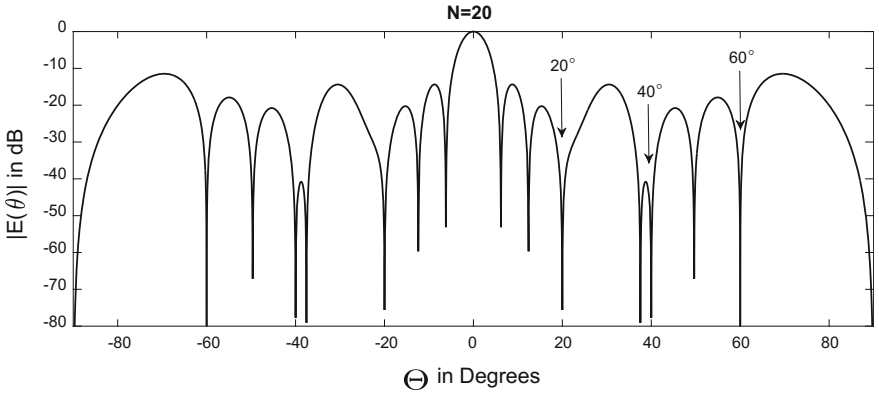


Fig. 4 Radiation pattern with nulls at 20°, 40° and 60°

Table 2 Amplitude distribution obtained using FFA for different cases

Element number	Amplitude distribution			
	Case-1	Case-2	Case-3	Case-4
1&1′	0.698	0.778	0.443	0.934
2&2′	1	0.868	0.949	0.602
3&3′	0.267	0.567	0.746	0.608
4&4′	0	0	0.519	0.379
5&5′	0.939	0.228	0.388	0.203
6&6′	0.078	1	0.985	0.860
7&7′	0.404	0.156	0.571	0.135
8&8′	0.524	0.211	0.848	0.004
9&9′	0	0.814	0.038	0.911
10&10′	1	0.534	0.622	0.082

5.3 Case-3

This case is similar to case-2, but with enhanced number of nulls. Keeping the earlier two nulls in their position in the radiation patterns, an extra null is located at 60°. This further helps in validating the efficiency of the algorithm in positioning the nulls in the desired directions as well as handling multiple nulls. This is demonstrated in Fig. 4 where the arrow marks show the position of the desired three nulls. The amplitude distribution obtained using the FFA is given in Table 2.

5.4 Case-4

Beam steering is one of the desired characteristics in beamforming. It is often desired to steer the main beam to the desired direction which is the DOA of the

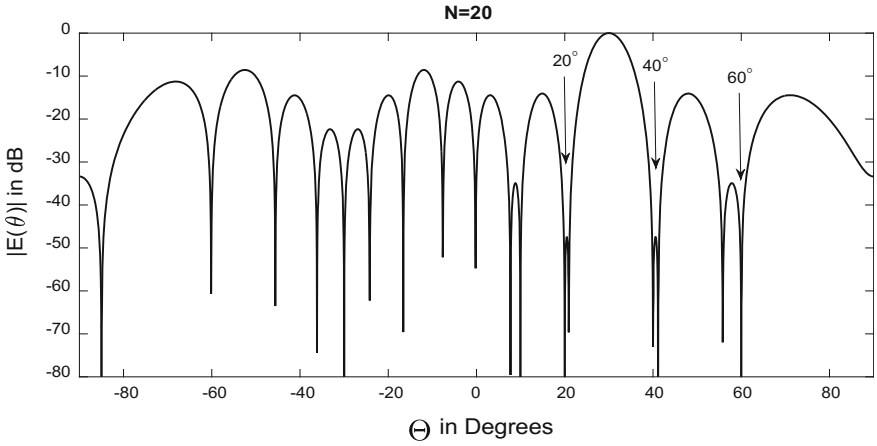


Fig. 5 Beam steering with an angle of 60°

actual signal. In addition to this, three nulls are also positioned as mentioned in the case-3 which are considered as the DOA of the interference signals. This is shown in the Fig. 5 where the main beam is steered to an angle of 30° which is considered as the DOA of the desired signal. The corresponding amplitude distribution is as given in Table 2.

6 Conclusion

The technique of generating nulls in the desired directions in order to suppress the interference signals is well demonstrated under unscanned and scanned conditions for beamforming characteristics. The novel algorithm has shown its efficiency and simplicity in terms of computation and complexity. The technique demonstrated in this paper can easily be extended to any multimodal problems with several constraints.

References

1. C.A. Balanis, Antenna Theory: Analysis and Design, 2nd ed. Singapore: John Wiley and Sons, Asia (2003).
2. Skolnik, I. M., Radar Handbook, McGraw-Hill (1990).
3. Elliott, R. S., Antenna Theory and Design, Prentice Hall, Englewood Cliffs, NJ (1981).
4. S.A. Schelkunoff, H.T. Friis,: Antennas Theory and Practice, JW&Sons Inc., London (1952).
5. K.-K. Yan and Y. Lu, "Sidelobe reduction in array-pattern synthesis using genetic algorithm," IEEE Transactions on Antennas and Propagation, vol. 45, no. 7, pp. 1117–1122 (1997).

6. R. L. Haupt Phase-only adaptive nulling with a genetic algorithm, IEEE Transactions on Antennas and Propagation, vol. 45, pp. 1009–1015 (1997).
7. D. Karaboga, K. Guney and A. Akdagli "Antenna array pattern nulling by controlling both the amplitude and the phase using modified touring ant colony optimisation algorithm", Int. Journal of Electronics, vol. 91, pp. 241–251 (2004).
8. Chakravarthy, V.V.S.S.S.; Rao, P.M., "On the convergence characteristics of flower pollination algorithm for circular array synthesis," in Electronics and Communication Systems (ICECS), 2015 2nd International Conference on, vol., no., pp. 485–489, 26–27 Feb. (2015).
9. Sameer Chakravarthy, V.V.S.S.; Mallikarjuna Rao, P., "Amplitude-only null positioning in circular arrays using genetic algorithm," in Electrical, Computer and Communication Technologies (ICECCT), 2015 IEEE International Conference on, vol., no., pp. 1–5, 5–7 Mar. (2015).
10. K. D. Cheng, "Optimization techniques for antenna arrays," Proceedings of the IEEE, vol. 59, no. 12, pp. 1664–1674 (1971).
11. V. S. S. S. Chakravarthy Vedula, S. R. Chowdary Paladuga, and M. Rao Prithvi, "Synthesis of Circular Array Antenna for Sidelobe Level and Aperture Size Control Using Flower Pollination Algorithm," International Journal of Antennas and Propagation, vol. 2015, Article ID 819712, 9 pages (2015).
12. L. Manica, P. Rocca, A. Martini, and A. Massa, "An innovative approach based on a tree-searching algorithm for the optimal matching of independently optimum sum and difference excitations," IEEE Trans. Antennas Propag., vol. 56, no. 1, pp. 58–66, Jan. 2008.
13. M. Alvarez-Folgueiras, J. A. Rodriguez-Gonzalez, and F. Ares-Pena, "Synthesising Taylor and Bayliss linear distributions with common aperture tail," Electron. Lett., vol. 45, no. 11, pp. 18–19, Jan. (2009).
14. V. V. S. S. S. Chakravarthy, K. Naveen Babu, S. Suresh, P. Chaya Devi, and P. Mallikarjuna Rao, "Linear array optimization using teaching learning based optimization," Advances in Intelligent Systems and Computing, vol. 338, pp. 183–187 (2015).
15. X.-S. Yang, "Firefly algorithms for multimodal optimization," in Stochastic Algorithms: Foundations and Applications: 5th International Symposium, SAGA 2009, Sapporo, Japan, October 26–28, 2009. Proceedings, vol. 5792 of Lecture Notes in Computer Science, pp. 169–178, Springer, Berlin, Germany (2009).

Circularly Polarized Notch Band Antenna with Defected Ground Structure

Abdul Rahiman Sheik and Kalva Sri Rama Krishna

Abstract A compact printed wideband antenna with circular polarization is designed and the antenna parameters are analyzed in this work. Finite element method-based HFSS tool is used to design and simulate the antenna model. A basic structure of rectangular monopole is converted into a trapezoidal shape with tapered step ground. Different iterations of radiating element as well as defected ground structures are examined in this work to analyze the circular polarization characteristics of the antenna. A peak realized gain of 4.3 dB and peak directivity of 3.8 dB is attained from the current designed models. A wide bandwidth is attained using the CPW fed by defected ground trapezoidal patch antenna. The analysis is carried out using the simulated reports like return loss and surface current density. The concept of circular polarization is evident from other reports like axial ratio and radiation pattern.

Keywords Circular polarization (CP) · Defected ground structure (DGS) · Notch band · Split ring resonator (SRR) · Wideband antenna

A.R. Sheik (✉)
Department of ECE, Acharya Nagarjuna University,
Guntur, AP, India
e-mail: ska.rehman@rediffmail.com

A.R. Sheik
Department of ECE, NRI Institute of Technology,
Pothavarappadu, AP, India

K.S.R. Krishna
Department of ECE, V R Siddhartha Engineering College,
Vijayawada, AP, India
e-mail: srk_kalva@yahoo.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_41

1 Introduction

The CP is considered as an extremely required feature of UWB antenna [1, 2]. The CP realization is often considered to be cumbersome task with complexed circuit. However, in the recent past the circularly polarized antennas have gained demand due to their inherent properties which are the basic characteristics of the radiating system for satellite applications. Several types of CPA models like crossed dipoles, spiral and yagi uda antennas are proposed as radiating system for CP application. However, several sophisticated wireless applications demand for antennas with CP which are conformal and miniaturized. Considering this, microstrip antenna geometry is suggested with all these features mentioned above as its inherent properties. But, the feed system takes a complex construction which produces orthogonal components of electric field with phase quadrature [3–8].

In this paper, a basic structure of rectangular monopole is converted into trapezoidal shape with tapered step ground. Different iterations of radiating element as well as defected ground structures are examined in this work to analyze the circular polarization characteristics of the antenna. A defected structure etched in the metallic ground plane of a microstrip line is one of the smart solutions. It provides deep and extensive stop band, sharp cutoff with its compact size to encounter evolving applications. Further the paper is organized as follows.

Design of antenna models is given in Sect. 2. Simulated results and discussions are mentioned in Sect. 3. The overall conclusions are mentioned in Sect. 4.

2 Proposed Design of Antenna

Figure 1 refers to model 1 with trapezoidal shape slot antenna on defected ground structure. The antenna is designed on FR4 substrate of dimensions 60 × 50 × 1.53 mm. A ground is also printed in the same side of substrate along with radiating patch element. A rectangular slot of dimensions 40 × 23 mm is ground plane with CPW feed. At the end of the feed line, a trapezoidal shaped radiating stub protruding into the slot is arranged. The rectangular slot is cut into two circular arcs at lower left corner and upper right corner and having different radii to serve as perturbations required for recognizing circular polarization. In this model, ‘S’ refers to the spacing between the longest trapezoid side and the side of the slot toward the feed line. The trapezoidal shape stub has widths of Ws1 and Ws2 and has length as Ls. The parameter values are shown in Table 1.

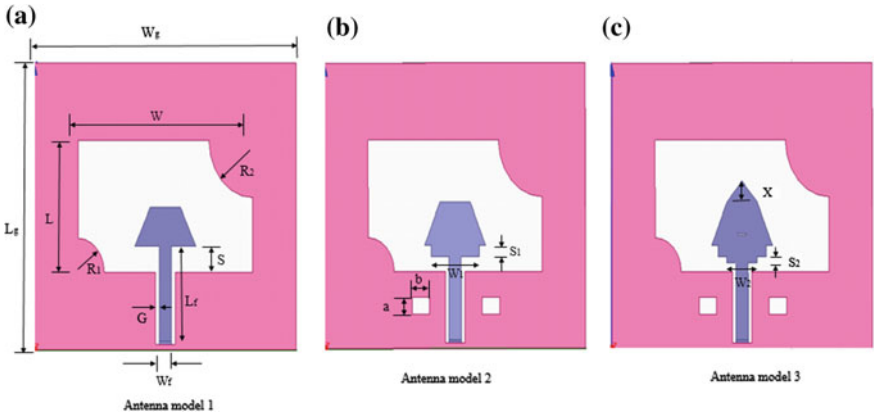


Fig. 1 Tapered ground monopole, **a** trapezoidal monopole, **b** trapezoidal stub monopole with DGS, **c** trapezoidal stepped stub monopole with DGS

Table 1 Antenna model 1 dimensions

Parameter	Dimensions (in mm)
Wg	60
Lg	50
W	40
L	23
R1	6
R2	10
Lf	16.62
Wf	2.8
S	3.68
G	0.85
Ws1	7
Ws2	14
Ls	7.5
H	1.53

In order to enhance the CP and bandwidth characteristics, the model is modified. Accordingly, the two modified version of antenna model 1 are designed they are named as antenna model 2 and antenna model 3. The antenna model 2 has step size 11 × 2 mm is added to trapezoidal shaped tuning stub, two rectangular slots of dimensions 3 × 4 mm are cut in the ground plane. In the antenna model 3, one more step is added to the tuning stub and a slit of dimensions 2 × 0.2 mm is cut at the center of trapezoidal tuning stub. The modified dimensions of antenna model 2 and antenna model 3 are shown in Table 2.

Table 2 Modified dimensions (in mm) of antenna model 2 and antenna model 3

Parameter	W1	S1	W2	S2	X	A	b
Antenna model 2 dimensions	11	2	–	–	–	3	4
Antenna model 3 dimensions	11	2	7	1	3.685	3	4

3 Results and Analysis

Figure 2 show the reflection coefficient of the antenna iterations shown in Fig. 1. Antenna model 1 is giving a bandwidth of 4.8 GHz and antenna model 2 is giving the bandwidth of 5.4 GHz. By changing the radiating element shape and by incorporating defected ground structure we attain additional resonant band for antenna model 2. To improve the bandwidth characteristics of the designed antenna model, we incorporated additional changes in the patch element by taking tapered step structure. Antenna model 3 is providing bandwidth enhancement of 7.2 GHz which is almost double to the basic antenna model 1.

The circular polarization characteristics of the designed models can be observed through axial ratio curve of Fig. 3. In the operating band of this antenna models only at certain frequency bands, the designed antennas are showing circular polarization characteristics. 3 dB cutoff circular polarization characteristics at certain frequency bands can be observed from Fig. 3. Figures 4, 5, and 6 show the radiation characteristics of the designed antenna models at center resonant frequency in the operating band. All these models are providing almost omnidirectional radiation pattern in H-plane and monopole like radiation in the E-plane. Figure 7 shows the surface current distribution of designed antenna models and by analyzing current distribution characteristics at different phases we examined the circular polarization from these models.

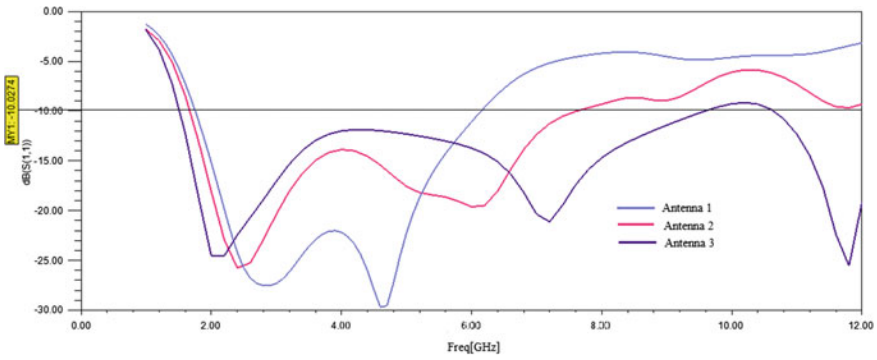


Fig. 2 Reflection coefficient of antenna models 1, 2 and 3

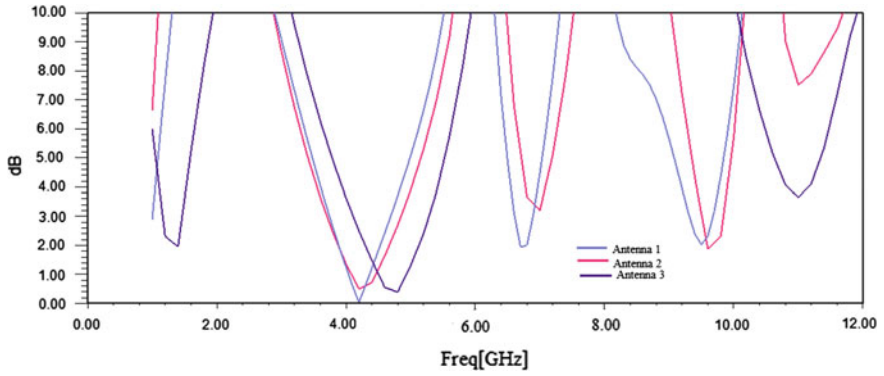


Fig. 3 Axial ratio of antenna models 1, 2 and 3 with respect to resonant frequency

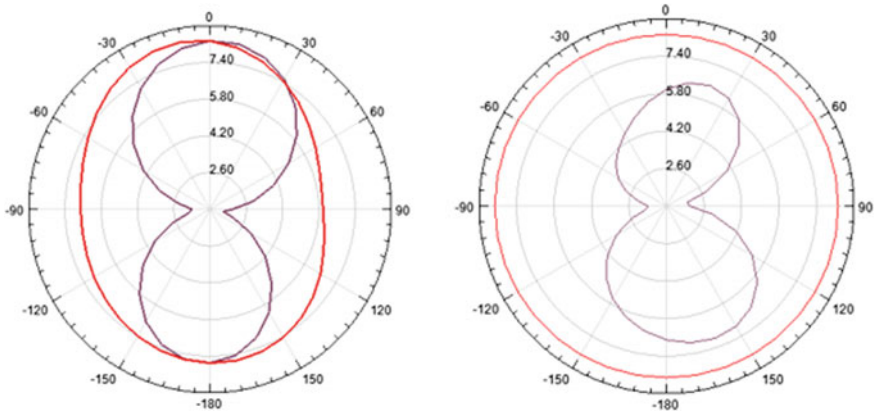


Fig. 4 Radiation pattern of antenna model 1 at 4 GHz

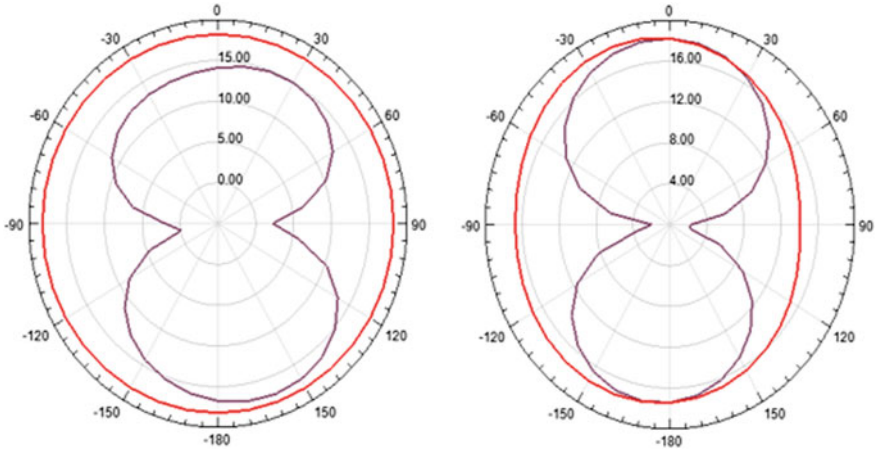


Fig. 5 Radiation pattern of antenna model 2 at 4 GHz

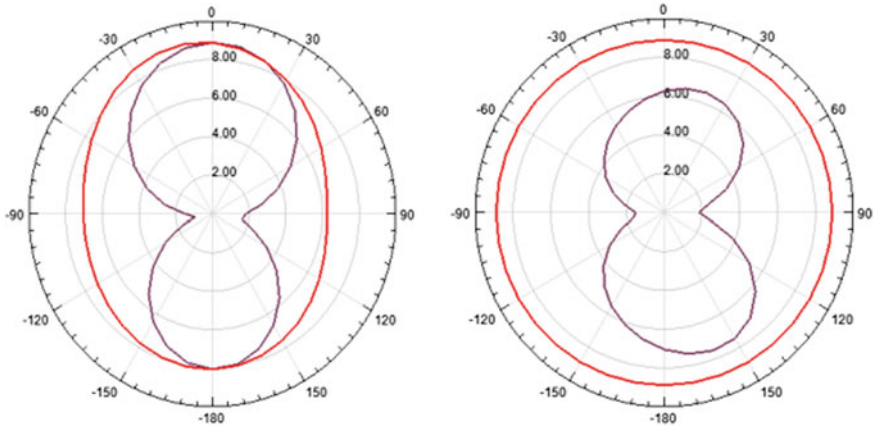


Fig. 6 Radiation pattern of antenna model 3 at 4 GHz

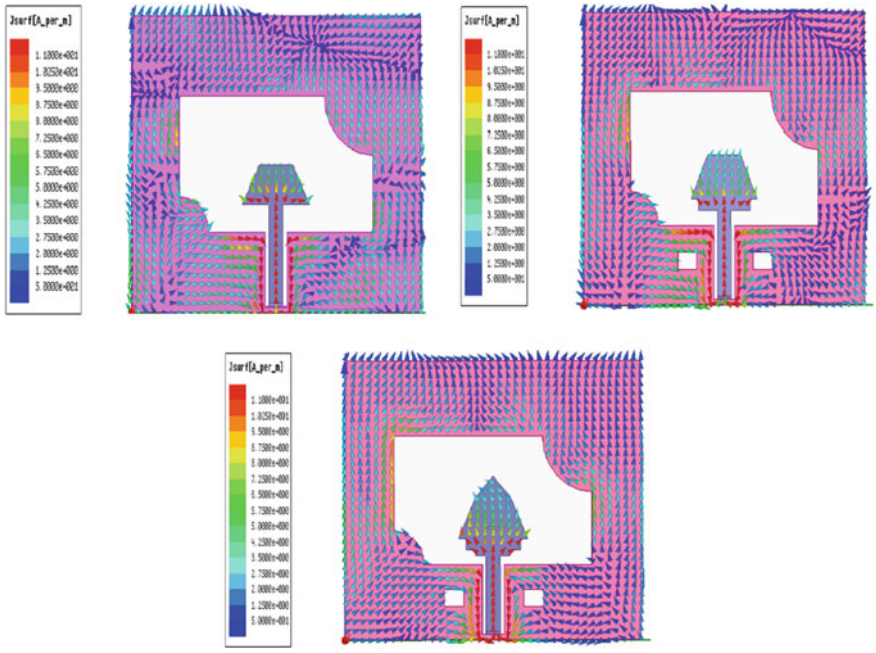


Fig. 7 Current distribution of antenna models 1, 2 and 3 at 4 GHz

4 Conclusion

Design of CPW fed patch antenna with defected ground structure (DGS) is performed and modified to achieve wide band and circular polarization. A novel structure of trapezoidal monopole antenna with defected ground structure is designed in this work.

References

1. Ram Krishna, R.V.S., Raj Kumar.: Design of ultra-wideband trapezoidal shape slot antenna with circular polarization. AEU- international journal of electronics and communications, 67 (12), 1038–1047 (2013).
2. Madhav, B. T. P., Sai ram, K., Deepika, M., Naresh, V.: Circularly Polarized Koch Fractal Trib and Antenna for Communication Applications. ARPN Journal of Engineering and Applied Sciences, 10(14), 5795–5801 (2015).
3. Wang, C-J., Lin, C-M.: A CPW-fed open-slot antenna for multiple wireless communication systems. IEEE Antennas Wireless Propag Lett, 11, 620, (2012).
4. Phani Srinivas, K., Madhav, B. T. P.: Novel Koch fractal circularly polarized micro strip antenna for global positioning system application. Leonardo Electronic Journal of Practices and Technologies, 27(2), 31–40, (2015).
5. Chen, C-H., Yung, EKN.: Dual-band circularly-polarized CPW-fed slot antenna with a small frequency ratio and wide bandwidths. IEEE Trans Antennas Propag, 59(4) 1379–84, (2011).
6. Lakshmi, M. L. S. N. S., Habibulla Khan, Madhav, B. T. P.: Novel Sequential Rotated 2x2 Array Notched Circular Patch Antenna. Journal of Engineering Science and Technology Review, 8(4), 73–77, (2015).
7. Madhav, B. T. P., Habibulla Khan, Sarat Kotamraju, K.: Circularly Polarized Slotted Aperture Antenna With Coplanar Waveguide Fed for Broadband Applications. Journal of Engineering Science and Technology, 11(2), 267– 277, (2016).
8. Madhav, B. T. P.: Analysis of Defected Ground Structure Notched Monopole Antenna. ARPN Journal of Engineering and Applied Sciences, 10(2), 747–752, (2015).

Multiband Characteristics of the Slot-Loaded Aperture Fed Antenna

B. Deepa, B. Roopa and Anil Kumar Patnaik

Abstract Etching multi-resonant shapes on the radiating patch of a microstrip antenna is often used to interpret multiband characteristics. In this paper, such a multiband antenna is designed using aperture-coupled feed. The proposed multi-resonant geometry captivates the advantages of both planar microstrip patch antenna (MPA) and the aperture feed system. The antenna is simulated in high-frequency structure simulation (HFSS) tool and analyzed using radiation characteristics plots like reflection coefficient voltage standing wave ratio (VSWR) and polar radiation plots.

Keywords Aperture feed · MPA · Multiband

1 Introduction

Since the origin of basic MPA geometry, several feed systems are proposed. Most popular are microstrip line and co-axial based. The MPA inherently suffers from several drawbacks like unintentional surface waves and diminishing radiation efficiency due to the dielectric substrate [1, 2]. Moreover, the above discussed feed systems are more prone to such drawbacks as they get in contact with the dielectric material in the antenna system. As a solution, the alternate step is to wave the feed mechanism indirectly. Such feed mechanism was proposed during 1985 [3, 4] and

B. Deepa (✉)
Anil Neerukonda Institute of Technology and Sciences, Sangivalasa, Visakhapatnam, India
e-mail: deepakundala@gmail.com

B. Roopa
Chaitanya Bharathi Institute of Technology, Hyderabad, India
e-mail: roopabammidi@gmail.com

A.K. Patnaik
Raghu Institute of Technology, Dakamarri, Visakhapatnam, India
e-mail: akp266@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*, Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_42

named as aperture feed system. In addition to its immune mechanism to surface waves, the feed system also has advantage of electrical isolation. Hence, soon the technique emerged as the best feed system for array configuration which requires high degree of electrical isolation in order to overcome the mutual interference [5–7].

In this paper, the multiband characteristics of MPA with aperture feed are simulated and analyzed. Two different types of antenna are simulated. The first design consists of a slot typically in the shape of 'S' the second design uses two such shapes interconnected perpendicularly to form an as symmetric 'SWASTIK'.

Further, the paper is organized to describe the proposed geometry in Sect. 2 and simulation results and discussions are given in Sect. 3 followed by conclusion as Sect. 4.

2 Design of the Antenna

The design and description of the aperture feed system and the two geometries along with its dimensions are discussed in the subsequent sub-section.

2.1 Aperture-Coupled Feed (ACF)

The structure of the ACF is as shown in Fig. 1. It typically consists of two substrates with permittivity εr_1 and εr_2 between which a conducting ground plane runs with a horizontal slot. The radiating patch is on top on the surface of the top substrate. Through the feed mechanism is complexed and associated with fabricated difficulties, yet has the advantages that suppress spurious radiation.

2.2 Antenna Geometry

As discussed above, two designs are proposed. The geometry of design-1 is as shown in Fig. 2. Similarly, the geometry of design-2 is presented in Fig. 3. The dimensions are listed in Table 1.

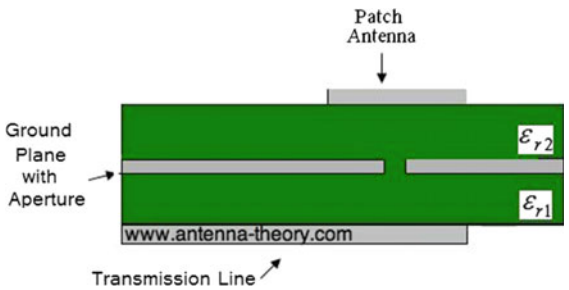


Fig. 1 Geometry of aperture feed system

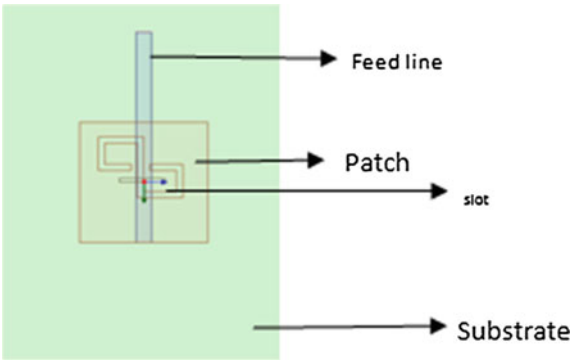


Fig. 2 Geometry of design-1

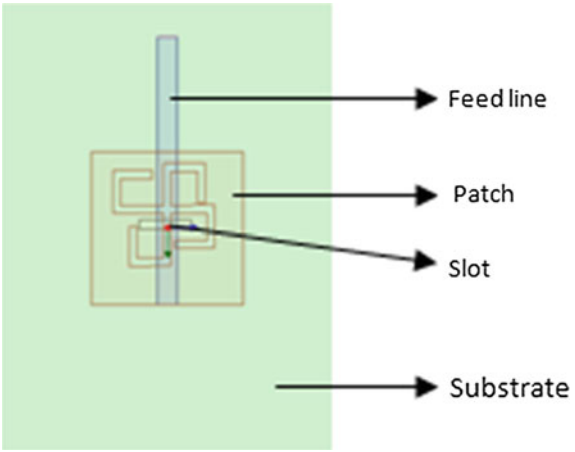


Fig. 3 Geometry of design 2

Table 1 Antenna design 1 and 2 parameters

Dimension	Design-1	Design-2
Sub length (cm)	12	12
Sub width (cm)	9	9
Sub height (cm)	0.32	0.32
Patch length (cm)	4	4
Patch width (cm)	4	4
Strip width (cm)	0.495	0.495
Slot length (cm)	1.4	1.4
Slot width (cm)	0.155	0.155
Sw (mm)	2	2

3 Results and Discussions

The antenna is designed with Rogers RT/Duroid substrate and $\varepsilon_r = 2.2$ and 0.32 cm thickness. The dimensions of the design 1 and 2 are as given in the Table 1. Results pertaining to the designed antenna models are given in this Section. Further, the analysis of the antennae is carried out using the simulated reports. All the simulated results of Design 1 antenna are as shown in Figs. 4, 5 and 6 and results of design 2 antenna are as shown in Figs. 7, 8 and 9. The resonant characteristics of the first design are evident from the Figs. 4 and 5. With a band gap of 1.5 GHz there are two resonant frequencies located at 2.38 and 2.53 GHz. The first resonant frequency is considered for plotting the radiation pattern. The simulated polar field plot for the selected frequency is as shown in Fig. 6. It can be read from the plot that the radiation is maximum in the upper hemisphere than the lower hemisphere following the template pattern of a typical patch antenna.

Similarly, the radiation and the resonant characteristics of the second model can be analyzed using the S11 and VSWR plots given in Figs. 7 and 8. The radiation

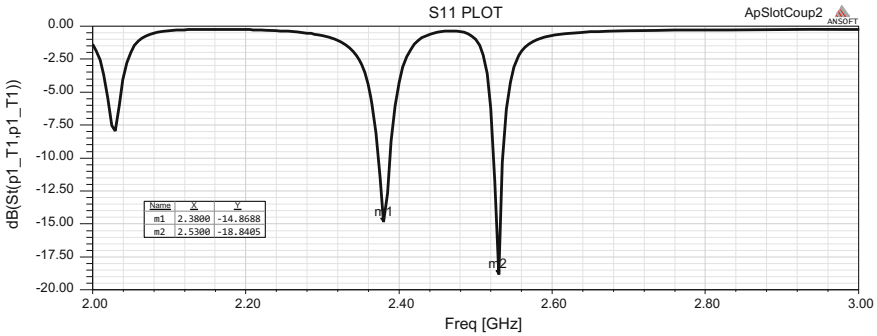


Fig. 4 Simulated S_{11} of design 1

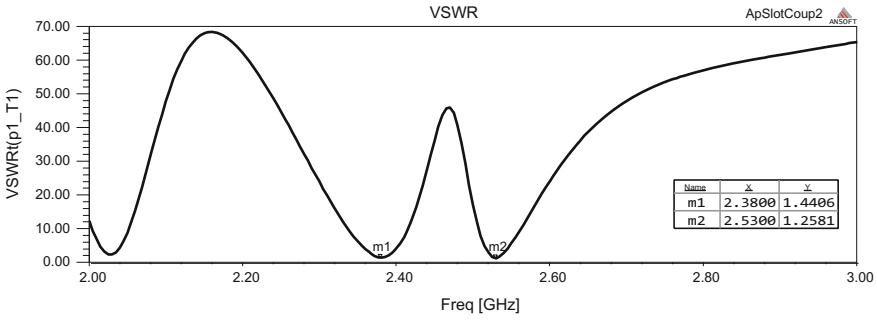


Fig. 5 Simulated VSWR of design 1

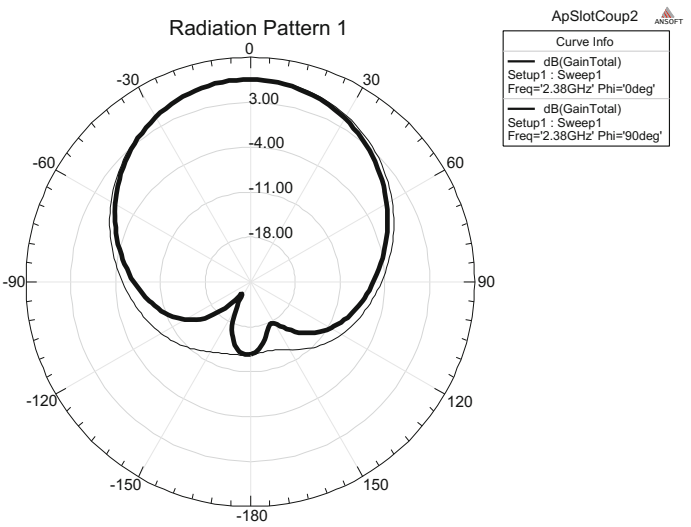


Fig. 6 Simulated polar plot of design 1

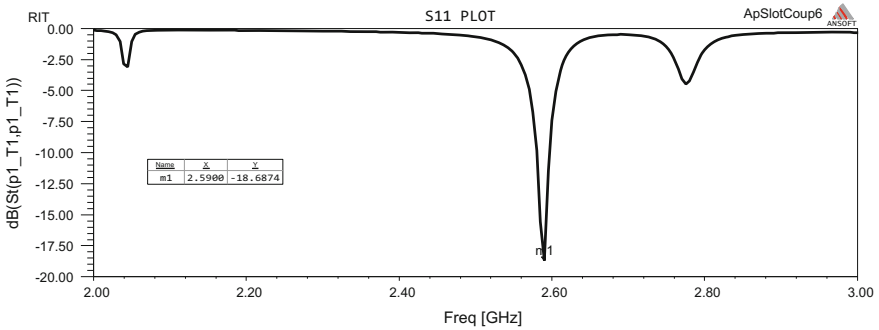


Fig. 7 Simulated S_{11} of design 2

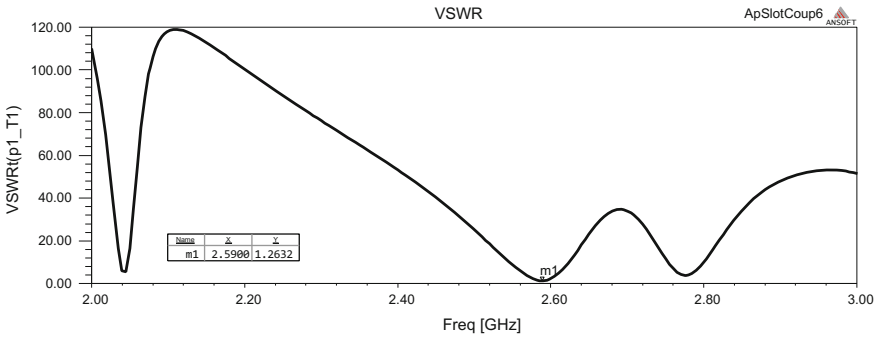


Fig. 8 Simulated VSWR of design 2

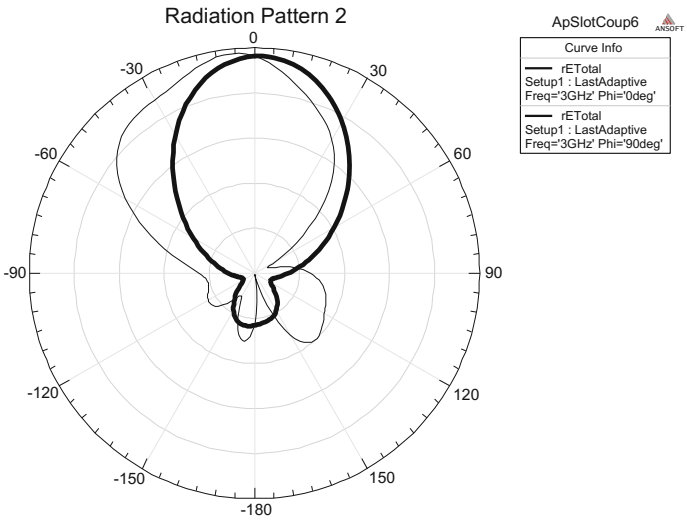


Fig. 9 Simulated polar plot of design 2

pattern plot in Fig. 9 is useful to validate the basic antenna features of the modelled antenna. The resonant frequencies of the antenna have slightly shifted to right side of the plot to the higher band.

4 Conclusion

The multi-resonant characteristics of the patch antenna with aperture feed technique are verified using two different designs. The base design of the antenna exhibits narrow band characteristics at 2.35 GHz like any other patch antenna. However, the multi-resonant slot geometry transforms the antenna into a slot-loaded patch antenna with the complexed aperture feed technique. The multiband characteristics are evident with both the designs which clearly states that the slots have impact on the radiation characteristics no matter with the feed system.

References

1. Pozar. D. M.: A Microstrip Antenna Aperture Coupled to a Microstrip Line. Electronics Letters, Vol. 21, pp 49–50, (Jan 1985).
2. M. Pozar, “A reciprocity method of analysis for printed slot and slot coupled microstrip antennas”, IEEE Trans. Antennas and Propagation, vol. AP-34, pp. 1439–1446, (December 1986).

3. Y. Yashimura, "A microstrip slot antenna," IEEE Trans. Antennas Propag., vol. AP-29, pp. 2–24, Jan. 1981.
4. Michael Civerolo., Dean Arakaki.: Aperture Coupled Patch Antenna Design Methods (2010).
5. Shrivastava. S. C., Zarreen Aijaz.: An Introduction of Aperture Coupled Microstrip Slot Antenna. International Journal of Engineering Science and Technology Vol. 2(1), 36–39 (2010).
6. P.S.R Chowdary: "Design and Performance Study of Sierpinski Fractal Based Patch Antennas for Multiband and Miniaturization Characteristics". Wireless Personal Communications, Aug., Volume 83, Issue 3, pp 1713–1730 (2015).
7. P.S.R Chowdary: "Simulation of Radiation Characteristics of Sierpinski Fractal Geometry for Multiband Applications". International Journal of Information and Electronics Engineering 3.6 Nov: 618 (2013).

Design and Analysis of Circular Notch Band DGS Monopole Antenna

S.S. Mohan Reddy, P. Mallikarjuna Rao, B.T.P. Madhav and B. Prudhvi

Abstract A configuration of circular notch band monopole antenna with DGS structure is demonstrated in the present article. The proposed MSP antenna is feed by microstrip line feeding with circular radiating element on top side of FR4 substrate and defected ground structure on the lower side. The basic circular monopole antenna is initially designed to operate in the wideband (2.5–12 GHz) and the modified proposed antenna is oriented to operate as notch band antenna (7.5–8 GHz). In order to attain single notch band characteristics, square shape slots in the ground plane are used. Better gain characteristics of 4.9 dB are realized by placing defected ground structure in the antenna model.

Keywords Defective ground structures (DGS) · Patch antenna · Monopole

1 Introduction

Microstrip antennas became the most attractive candidates of the modern communication systems with their low profile and ease of integration on MMIC and RFIC printed circuits. The disadvantages of the microstrip antennas include narrow bandwidth and surface wave related problems. The design of microstrip antenna

S.S. Mohan Reddy (✉) · B. Prudhvi
Department of ECE, S R K R College of Engineering, Bhimavaram, AP, India
e-mail: rahulmohan720@gmail.com

B. Prudhvi
e-mail: prudhvi273835@gmail.com

P. Mallikarjuna Rao
Department of Electronics and Communication Engineering, Andhra University, Visakhapatnam, AP, India
e-mail: pmraoauece@yahoo.com

B.T.P. Madhav
Department of ECE, K L University, Vaddeswaram, AP, India
e-mail: btpmadhav@kluniversity.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_43

with high efficiency became very crucial by considering all these points. The basic step in the design of an antenna is to select proper substrate. The substrate material in microstrip antennas is basically required for the strong mechanical and electrical support to the antenna metallization. To give such support to the antenna by the substrate needs to have a solid dielectric material, which will affect the overall electrical performance of the antenna, circuits and the transmission line. A substrate must, therefore equally satisfy the mechanical and electrical requirements, which may be most of the times difficult to meet the requirements [1–3].

Substrate material choice and evaluation are the essential parts of the antenna design procedure. Generally many substrate material properties are to be considered: The material dielectric constant, dielectric loss tangent and their variation with respect to temperature and frequency, thermal coefficient, homogeneity, isotropicity and temperature range, dimensional stability with respect to processing of temperature, thickness and uniformity of the substrate, humidity and aging are all of importance [4–7]. Similarly, the other physical properties like resistance to chemicals, machinability, tensile and structural strengths, flexibility, impact resistance, strain relief, bondability, formability and substrate characteristics are important in fabrication.

Antenna with dual band, multiband and wideband characteristics became essential parameters for modern communication systems. The design of such antennas involves modifications in the structure of the antennas with advanced material technology. Defected ground structure and partial substrate removal are the promising techniques in the design of high gain and high bandwidth antennas with multiband and wideband characteristics [8–12]. This chapter is mainly focussing on the design of such defected ground structured antenna with notch band characteristics in the wide operating band, [13–15].

2 Antenna Geometry

The proposed model of antenna structure with DGS is occupying small dimensions of 47 × 40 × 1.6 mm on a commercial FR4 substrate with dielectric constant 4.4. A circular monopole antenna with radius 10 mm is designed on defected ground structure model as shown in the Fig. 1. Rectangular slots are placed on the defected ground to enhance the bandwidth of the antenna and to get additional resonant frequencies in the subsequent models. The antenna iterations with slots on the ground plane can be observed from Fig. 2. The proposed notch band antenna geometry is shown in Fig. 3. The dimensional properties of the proposed notch band antenna are presented in Table 1.

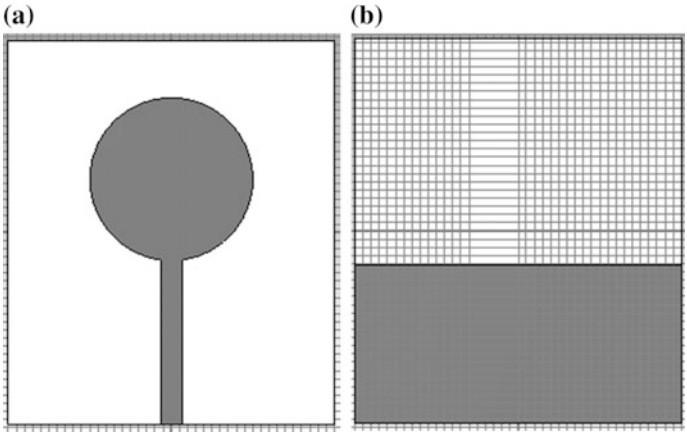


Fig. 1 Circular monopole antenna. **a** Top view. **b** Back view

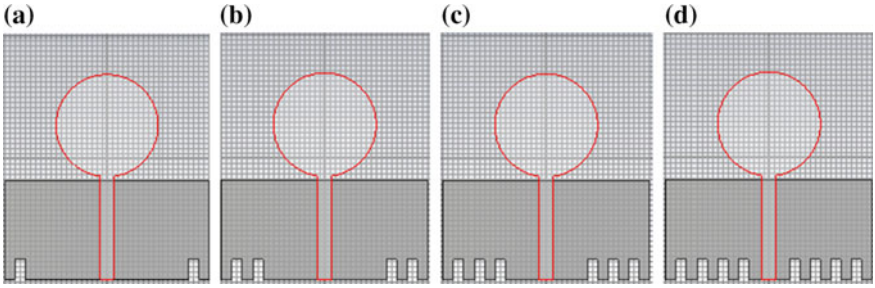


Fig. 2 Antenna DGS iterations. **a** Iteration 1. **b** Iteration 2. **c** Iteration 3. **d** Iteration 4. **e** Iteration 5

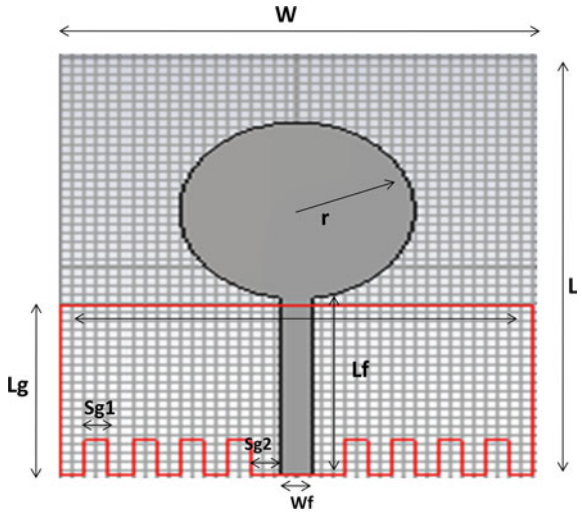


Fig. 3 Proposed notch band antenna geometry

3 Results and Discussion

CST microwave studio tool is used to simulate the antenna models. Initially circular monopole antenna with DGS is designed in CST and using time domain solver the simulation results are presented in this work. Figure 3 shows the proposed model of notch band antenna with DGS slots. The geometrical description is presented in the antenna geometry section with dimensional characteristics in tabular form. Figure 4 shows the reflection coefficient characteristics of antenna iterations. It has been observed that the circular monopole antenna is giving the bandwidth of 8.5 GHz and the subsequent antenna iterations with DGS are giving 8.55, 8.6 and 8.65 GHz bandwidth. The proposed notch band antenna is showing band rejection from 7.5 to 8 GHz and providing impedance bandwidth of 60% in the lower operating band and 33% in the higher operating band.

Table 1 Antenna dimensions

Parameter	L	W	L_f	L_g	r	S_{g1}	S_{g2}	W_f	h
Dimension in mm	47	40	20.3	19.3	10	2	2	2.6	1.6

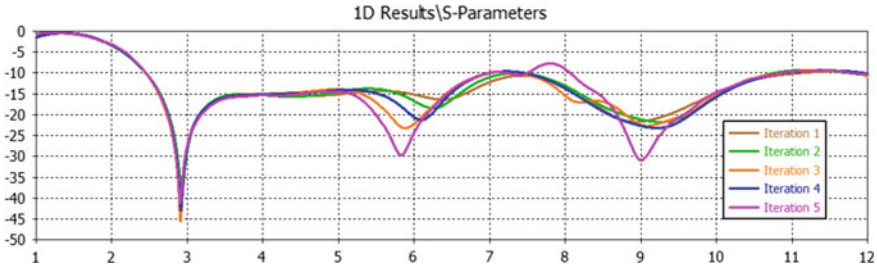


Fig. 4 Return loss versus frequency of antenna iterations

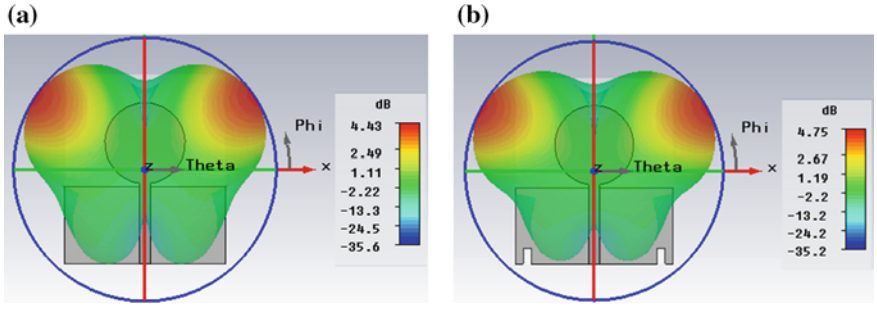


Fig. 5 3-dimensional radiation pattern characteristics of circular monopole antenna. **a** Iteration 1 at 6.5 GHz. **b** Iteration 2 at 6.5 GHz

The radiation pattern characteristics of designed antenna models are shown in Figs. 5, 6, 7, 8 and 9. The three dimensional view of the circular monopole antenna radiation pattern at 6.5 GHz is shown in Fig. 5a. A peak gain of 4.43 dB is attained from the basic circular shaped monopole antenna with DGS. A modified DGS structured monopole antenna radiation pattern is shown in Fig. 5b. A gain improvement of 0.32 dB is attained with this model. The radiation pattern of third iteration and fourth iteration are presented in Fig. 6. Third iteration is giving the gain of 4.9 dB and fourth iteration is providing gain of 4.75 dB. The notch band antenna radiation pattern in 3D is presented in Fig. 8. The radiation pattern at notch band frequencies are showing disturbed pattern and gain is also very poor at notch band. The radiation patterns of the all four iterations are presented in polar coordinates also in the Fig. 8. The monopole like radiation pattern can be observed from the obtained results. The notch band antenna radiation patterns also can be observed in polar coordinates from Fig. 9.

The current elements distribution characteristics of the designed DGS antenna iterations can be observed from Fig. 10. The current elements distribution at

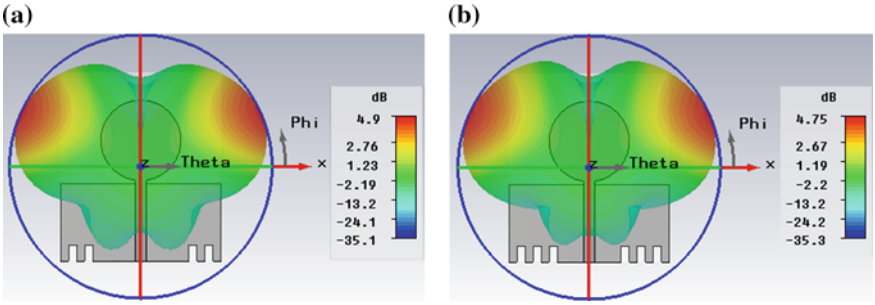


Fig. 6 3-dimensional radiation pattern characteristics of circular monopole antenna. **a** Iteration 3 at 6.5 GHz. **b** Iteration 4 at 6.5 GHz

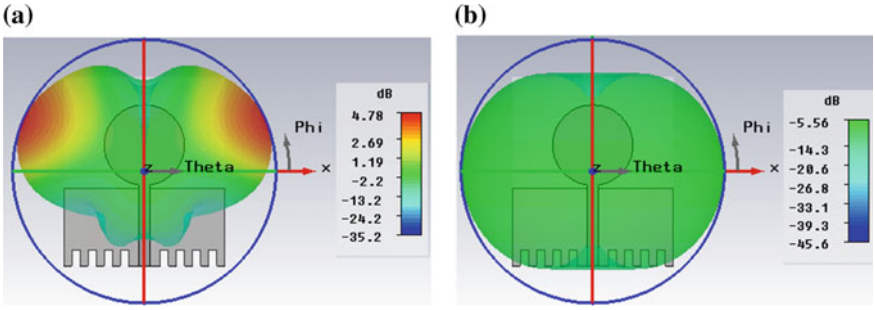


Fig. 7 3-dimensional radiation pattern characteristics of circular notch band antenna (Iteration 5). **a** At 6.5 GHz (Operating Band). **b** At 7.8 GHz (Notch Band)

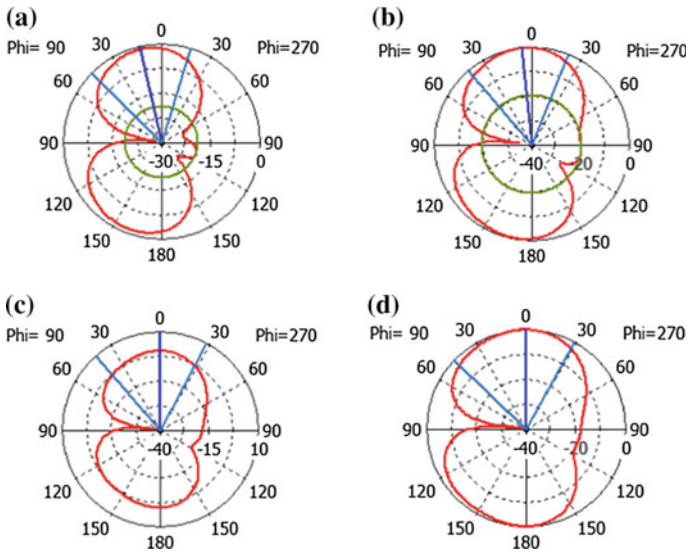


Fig. 8 Radiation pattern characteristics of circular monopole antenna at 6.5 GHz. **a** Iteration 1. **b** Iteration 2. **c** Iteration 3. **d** Iteration 4

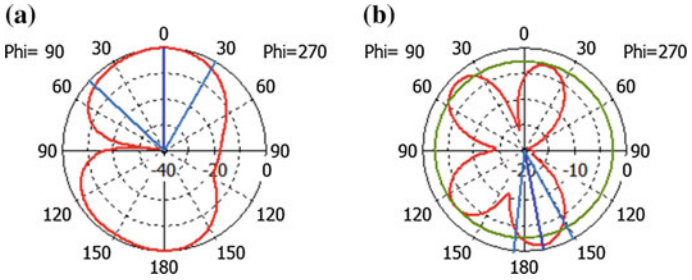


Fig. 9 Radiation pattern characteristics of circular notch band antenna (Iteration 5). **a** At 6.5 GHz (Operating Band). **b** At 7.8 GHz (Notch Band)

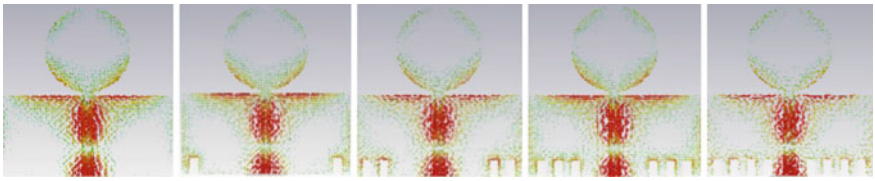


Fig. 10 Surface current distribution characteristics of circular monopole antenna iterations at 6.5 GHz

corresponding operating frequencies of current antenna models are providing the radiation characteristics and propagating modes. The feed line and the lower portion of the antenna elements are providing maximum intensity rather than the upper part of the radiating element. The current elements distribution over proposed notch band antenna at 7.8 GHz is shown in Fig. 11. At notch band the current intensity is very poor on the patch element and the radiation getting from the notch band antenna is because of feed line.

The proposed notch band antenna with DGS is fabricated on FR4 substrate and presented its photograph in Fig. 12. The front view and back view of the prototyped antenna can be cleared observed from this figure. The measured reflection coefficient characteristics over the proposed antenna is taken from ZNB 20 vector network analyzer and presented in Fig. 13. The simulation and measured results are showing good agreement with respect to operational characteristics. The notch band characteristics of the antenna can be observed from this measured result on VNA. The shift in the notch band for measured results is because of improper soldering of SMA connector on the ground plane.

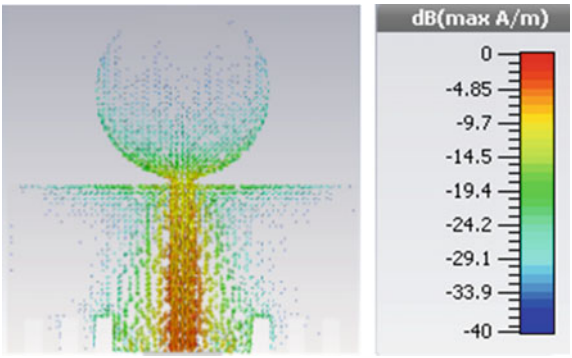


Fig. 11 Surface current distribution characteristics of notch band antenna at 7.8 GHz

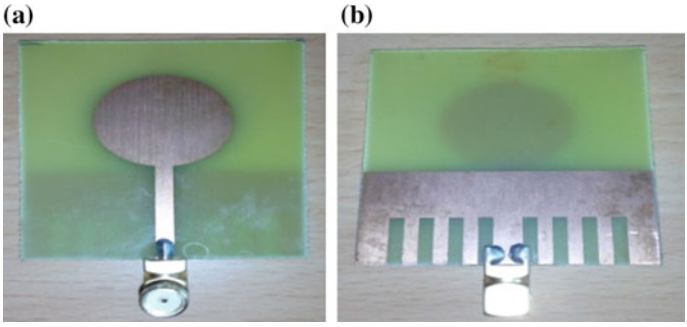


Fig. 12 Prototyped antenna. **a** Front view. **b** Back view

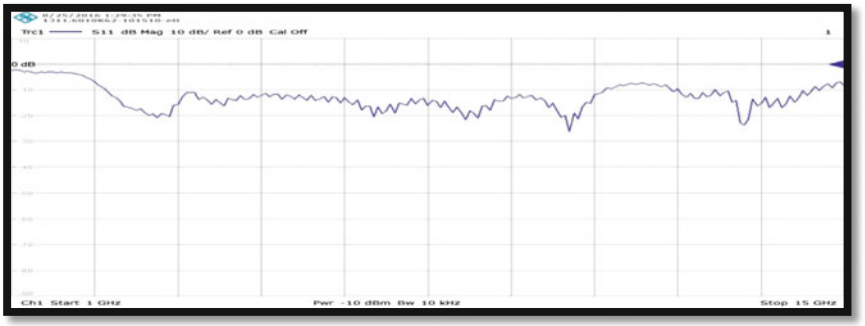


Fig. 13 Measured S11 on ZNB 20 VNA

4 Conclusion

Circular notch band monopole antenna with DGS is proposed in this work. The CST simulated results of the notch band monopole is in good agreement with the measured results on the ZNB 20 vector network analyzer. The proposed notch band is providing a peak realized gain of 4.7 dB in the operating band and very poor gain in the notch band. It is clear evidence from the present work that the defected ground structure in the antenna model enabled the improvement of gain by 0.5 dB. The achieved results show that the proposed antenna has good performance characteristics with respect to radiation pattern, gain and reflection coefficient for working frequency range except the notch band.

Acknowledgements Authors like to convey their gratitude to Dept. of ECE, S R K R Engineering College, Bhimavaram, Andhra University and K.L. University for their encouragement during this work. Madhav likes to express his thanks to DST through grant ECR/2016/000569 and SR/FST/ETI-316/2012.

References

1. B T P Madhav, A Manikanta Prasanth, Sreeramineni Prasanth, Batchu Mohan Sai Krishna, Devani Manikantha, Usirika Sharmila NagaSai, "Analysis of Defected Ground Structure Notched Monopole Antenna", ARPN Journal of Engineering and Applied Sciences, ISSN 1819-6608, Vol. 10, No. 2, Feb, pp 747–752(2015).
2. M. Ojaroudi, Ch. Ghobadi, and J. Nourinia, "Small square monopole antenna with inverted T-shaped notch the ground plane for UWB application," IEEE Antennas Wireless Propag. Lett., vol. 8, pp. 728–731(2009).
3. B T P Madhav, Harish Kaza, Thanneru Kartheek, Vidyullatha Lakshmi Kaza, Sreeramineni Prasanth, K S Sanjay Chandra Sikakollu, Maneesh Thammishetti, Aluvala Srinivas, K V L Bhavani, Novel Printed Monopole Trapezoidal Notch Antenna with S-Band Rejection, Journal of Theoretical and Applied Information Technology, ISSN: 1992-8645, Vol 76, No 1, pp 42–49(2015).

4. R. Rouhi, Ch. Ghobadi, J. Nourinia, and M. Ojaroudi, "Ultra-wideband small square monopole antenna with band notched function," Microw. Opt. Technol. Lett., vol. 52, no. 9, Sep, pp. 2065–2069(2010).
5. P. Lakshmikanth, Kh Takeshore, B T P Madhav, Printed Log Periodic dipole antenna with Notched filter at 2.45 GHz Frequency for wireless communication applications, Journal of Engineering and Applied Sciences, ISSN: 1816-949X, Vol 10, Issue 3, Aug, pp 40–44. DOI:10.3923/jeasci.2015.40.44 (2015).
6. D S Ram Kiran, B T P Madhav, Novel compact asymmetrical fractal aperture Notch band antenna, Leonardo Electronic Journal of Practices and Technologies, ISSN 1583-1078, Vol 27, Issue 2, Dec., pp 1–12(2015).
7. S. Yzadanifard, R. A. Sadeghzadeh, and M. Ojaroudi, "Ultra-wideband small square monopole antenna with variable frequency band-notch function," Prog. Electromagn. Res. C, vol. 15, pp. 133–144(2010).
8. M L S N S Lakshmi, Habibulla Khan and B T P Madhav, Novel Sequential Rotated 2×2 Array Notched Circular Patch Antenna, Journal of Engineering Science and Technology Review, ISSN: 1791-2377, Vol 8, issue 4, Dec., pp 73–77(2015).
9. M. V. Reddiah Babu, Sarat K. Kotamraju, B. T. P. Madhav, compact serrated notch band mimo antenna for uwb applications, ARPN Journal of Engineering and Applied Sciences, ISSN 1819-6608, Vol. 11, NO. 7, Apr., pp 4358–4369(2016).
10. M. L. S. N. S. Lakshmi, B. T. P. Madhav, Habibulla Khan, Tapered Slot CPW-Fed Notch Band MIMO Antenna, ARPN Journal of Engineering and Applied Sciences, ISSN: 1818-6608, VOL. 11, NO. 13, Jul., pp 1–7(2016).
11. S.S. Mohan Reddy, P. Mallikarjuna Rao, B.T.P. Madhav, Partial Substrate Removal Techniques for the Enhancement of Gain and Radiation Characteristics in Fractal Antenna, Research Journal of Applied Sciences, Engineering and Technology, ISSN: 2040-7459, Vol 10, Issue 1, May, pp 79–85(2015).
12. Swarup Das, Debasis Mitra, and Sekhar Ranjan Bhadra Chaudhuri, Design of UWB Planar Monopole Antennas with Etched Spiral Slot on the Patch for Multiple Band-Notched Characteristics, International Journal of Microwave Science and Technology, Volume 2015, Article ID 303215(2015).
13. Seyed Saeed Mirmosaei, Seyed Ebrahim Afjei, Esfandiar Mehrshahi and Mohammad M. Fakharian, A dual band notched ultra wideband monopole antenna with spiral slots and folded SIR, DGS as notch band structures, International Journal of Microwave and Wireless Technologies, Published online: 27, Apr.(2015).
14. N.C. Karmakar; S.M. Roy; I. Balbin: Quasi-static modeling of defected ground structure. IEEE Trans. Microwave Theory Tech, 54, 2160–2168(2006).
15. Tahsin Ferdous Ara Nayna, Emranul Haque, Feroz, Design of a X Band Defected Ground Circular Patch Antenna with Diamond Shaped Slot and Ring in Patch for UWB Applications, International conference on Signal Processing, Communication, Power and Embedded System (SCOPES)-(2016).

Circularly Polarized Defected Ground Broadband Antennas for Wireless Communication Applications

Abdul Rahiman Sheik, Kalva Sri Rama Krishna and B.T.P. Madhav

Abstract In this chapter a broadband antenna with defected ground is proposed for mobile (1.9–2.1 GHz), Wireless LAN (2.4 GHz) and Bluetooth (2.4–2.45 GHz) applications. The proposed antenna exhibits circular polarization in the range of 2.2–2.45 GHz with axial ratio less than 3 dB. A modified ground structure antenna is also proposed in this work for notching the band between (2.2–2.45 GHz). Antenna model 1 with circular polarization is providing impedance bandwidth of 32% and Antenna model 2 with linear polarization is providing impedance bandwidth of 25% (1.7–2.2 GHz) at fundamental resonant frequency and 16% (2.5–2.9 GHz) at second resonant frequency. The axial ratio bandwidth for circularly polarized antenna is around 38%. The designed antennas are providing peak realized gain of more than 5 dB in the operating bands and showing excellent monopole like radiation patterns with good impedance matching.

Keywords Axial ratio · Broadband antenna (BA) · Circular polarization (CP) · Defected ground structure (DGS) · Impedance bandwidth · Wireless communications

A.R. Sheik (✉)
Department of ECE, Acharya Nagarjuna University, Guntur, AP, India
e-mail: ska.rehman@rediffmail.com

A.R. Sheik
Department of ECE, NRI Institute of Technology, Pothavarappadu, AP, India

K.S.R. Krishna
Department of ECE, V R Siddhartha Engineering College, Vijayawada, AP, India
e-mail: srk_kalva@yahoo.com

B.T.P. Madhav
Department of ECE, K L University, Guntur, AP, India
e-mail: btpmadhav@kluniversity.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_44

1 Introduction

Compact circularly polarized antennas are accelerating their demand in the field of wireless communication systems. In most of the wireless communication applications circularly polarized antennas have been employed to reduce the matching between transmitter and receiver. Generally, the circular polarization will be achieved by feeding two orthogonal signals of 90° out of phase with equal amplitude to the non-radiating and radiating edges of the patch antenna [1–4]. To have a high circular polarization and better axial ratio, generally dual feeding technique is preferable but it requires a lot of board space and an external polarizer [5, 6]. To avoid these problems with current printed board technology, single feed simple technique is preferred.

To design circular polarization antennas, slot antennas have been receiving much attention from last one decade [7–10]. These slot antennas have larger bandwidth compared with conventional microstrip antennas due to their bidirectional radiation characteristics. As per the babinet's principle the slot antennas are nothing but microstrip antenna complementary structures. The perturbation technique can be applied on slot antennas to get circular polarization and these slot antennas can mitigate manufacturing tolerances of perturbation segments [11, 12].

In this chapter, a monopole antenna with defected ground structure is proposed to attain circular polarization. The slots on the ground plane are nothing but combination perturbation of notches and stubs to attain proper acceleration bandwidths. A microstrip line feeding technique is being used in the current structure.

2 Antenna Geometry

Two antenna models are proposed in this work. The antenna model 1 consisting of broadband characteristics and antenna model-2 exhibiting dual band characteristics. A diagonal-fed patch with a pair of notches or stubs along with two opposite edges can provide circularly polarized waves. When the slot edges are modified along with the feeding position by considering orthogonal modes of same magnitude and phase difference of 90°. Two stubs are placed in the design to attain circular polarization and impedance bandwidth. A commercial FR4 substrate with dielectric constant $\varepsilon_r = 4.4$ and dielectric loss tangent, i.e., $\tan\delta = 0.02$ is used in the current design of antennas. The square slot is rotated by 45° and 135° away from the feed line. The total perturbation area ΔA is obtained by

$$\left(\frac{\Delta A}{A}\right) Q_0 \cong \frac{1}{2}, \tag{1}$$

where, A is area of square patch without perturbations and Q_0 is quality factor of patch.

Table 1 Antenna dimensions in mm

L_s	W_s	L_f	W_f	L_g	S_1	S_w	S_2	W_2
80	80	40	3.2	40	15.5	4	7.4	7.2

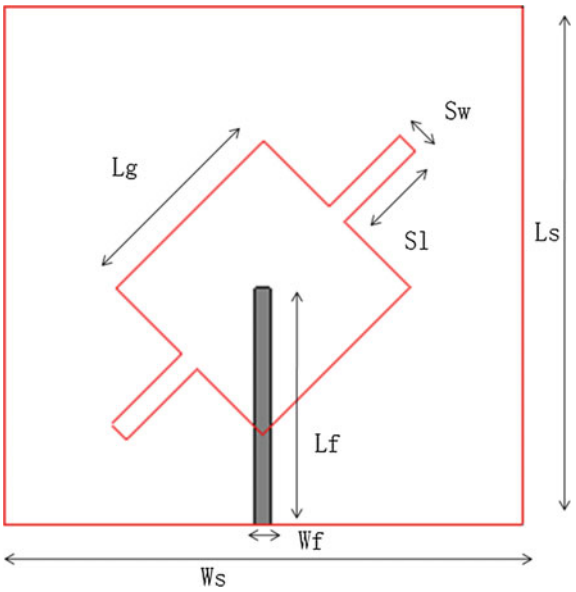


Fig. 1 Broadband antenna model 1

While designing slot antenna with stubs we fixed the stub length to obtain better circular polarization performance and after that the length of the stub is tuned to get impedance matching. The dimensional characteristics and the designed antenna structures are shown in Table 1, Figs. 1 and 2.

The antenna models are initially designed with CST studio software and the basic simulation work is performed for the identification of performance characteristics. The FDTD simulation approach is considered and the antenna parameters are analyzed in this work.

3 Results and Discussion

The design and simulation of the proposed antenna models are carried through CST and the findings are presented in this section. Figure 3 gives the return loss characteristics of the broadband antenna model 1 and dual band antenna model 2. The broadband antenna model 1 is resonating in the band of 1.9–2.7 GHz and the dual band antenna model 2 is resonating in two bands (1.7–2.3 and 2.5–2.9 GHz). The dual band antenna notching the frequency band of 2.3–2.5 GHz, where Wireless LAN and Bluetooth applications are blocked.

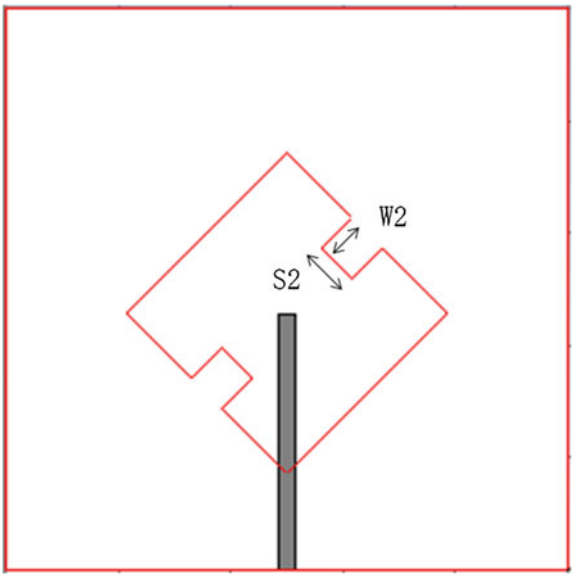


Fig. 2 Dual band antenna model 2

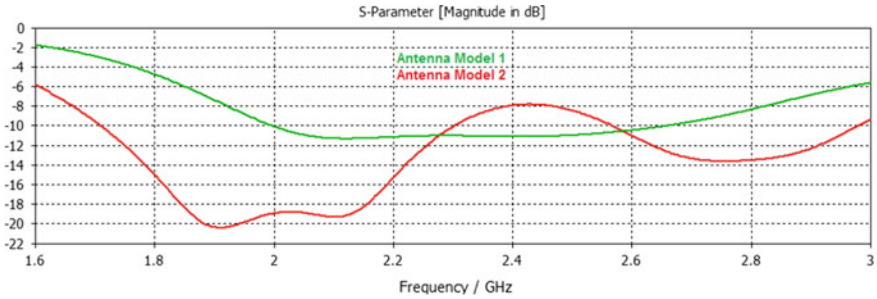


Fig. 3 Simulated reflection coefficient of antenna models (Broadband and Dual band)

The simulated voltage standing wave ratios of both the antenna models are presented in Fig. 4. Antenna model 1 is impedance bandwidth of 32% and whereas antenna model 2 is showing 25 and 16% at fundamental and second resonant band. Figure 5 shows the impedance characteristics of the antenna models with respect to resonating frequencies. It is been observed that between 1.7 and 2.1 GHz the impedance is close to the ideal impedance of 50 Ω. The time-domain analysis of the current models with respect to port signals are presented in Figs. 6 and 7.

The radiation characteristics of the designed antenna models are presented from Figs. 8, 9, 10, 11 and 12. The radiation pattern from Fig. 8 shows that the antenna is providing monopole like radiation at 1.9 GHz and showing gain more than

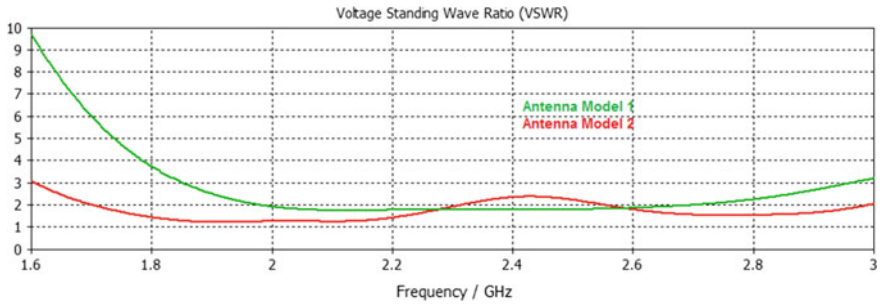


Fig. 4 Simulated VSWR of antenna models (Broadband and Dual band)

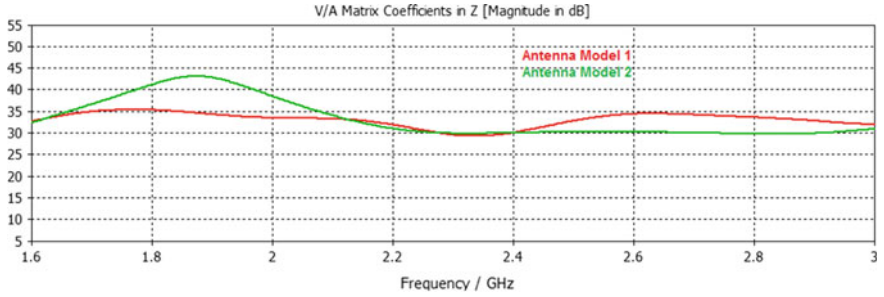


Fig. 5 Simulated impedance characteristics of antenna models (Broadband and Dual band)

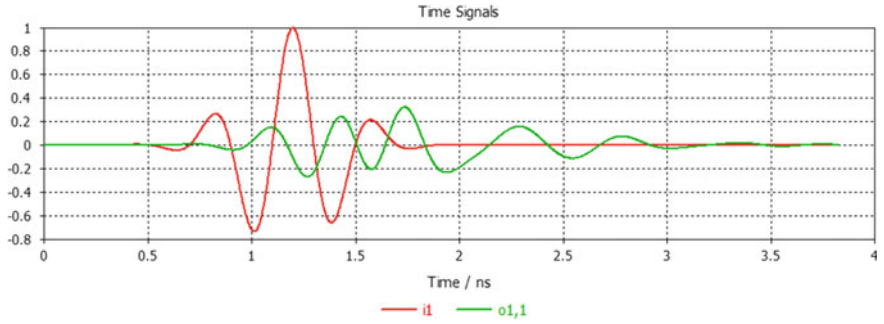


Fig. 6 Time-domain analysis of antenna model 1

4.7 dB in the desired direction. Figure 9 provides the similar kind of radiation pattern with gain of 5 dB at 2.1 GHz. At 2.4 GHz the gain is more than 5 dB.

The dual band antenna model 2 radiation characteristics are collected and presented in Fig. 11 for 1.9 GHz. The maximum gain is 4.83 dB at 1.9 GHz and 4.9 dB at 2.1 GHz. The radiation is like monopole like radiation and the antenna

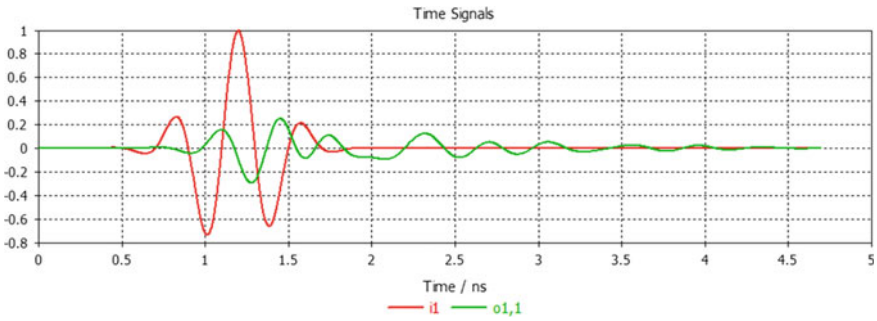


Fig. 7 Time-domain analysis of antenna model 2

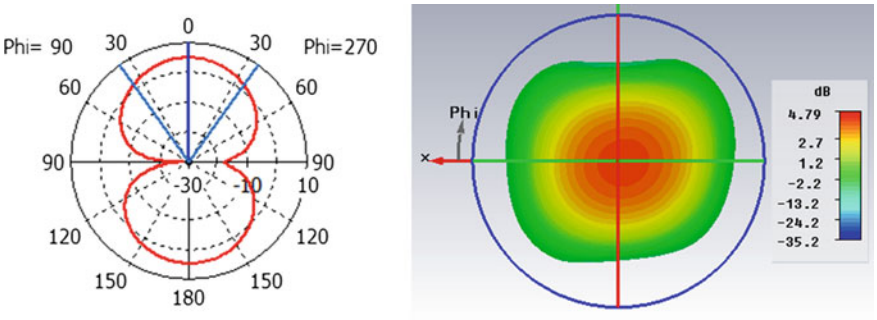


Fig. 8 Radiation pattern of broadband antenna at 1.9 GHz

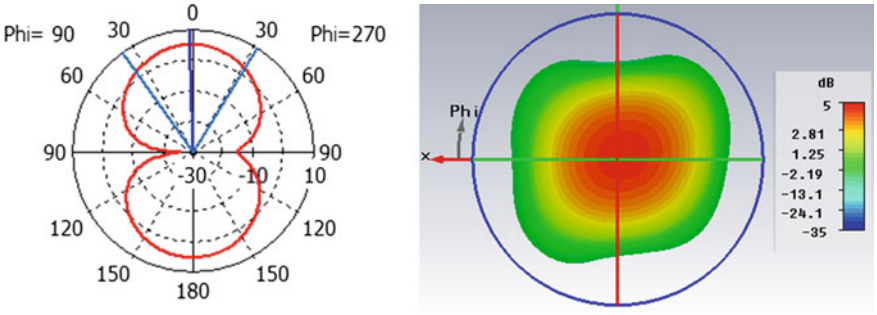


Fig. 9 Radiation pattern of broadband antenna at 2.1 GHz

models are maintaining desired gain of more than 4.5 dB at all the resonating frequencies and showing very low gain at notch band.

The broadband antenna model 1 is showing circular polarization in the frequency range of 2.2–2.45 GHz. The axial ratio bandwidth for circularly polarized antenna is around 38% (Fig. 13).

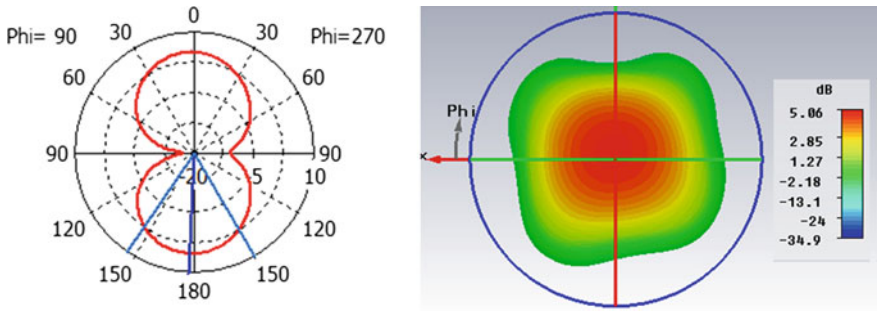


Fig. 10 Radiation pattern of broadband antenna at 2.4 GHz

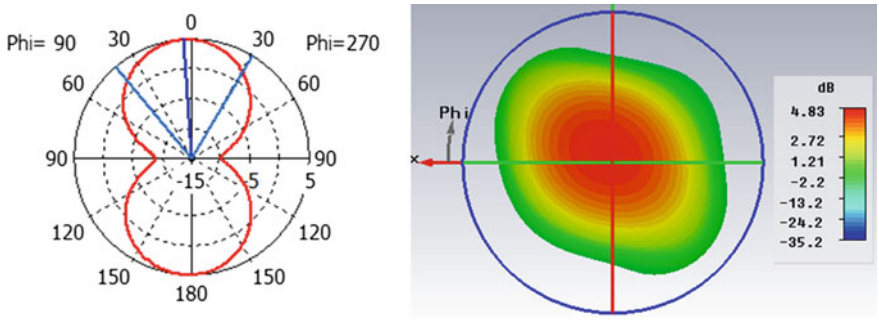


Fig. 11 Radiation pattern of dual band antenna at 1.9 GHz

The surface current distribution of the antenna models are presented in Fig. 14. For antenna model 1 the most of the current density is focussed around the defected ground whereas for antenna model 2 the current density is concentrated more at lower half only. The radiating element is contributing towards radiation rather than slotted ground.

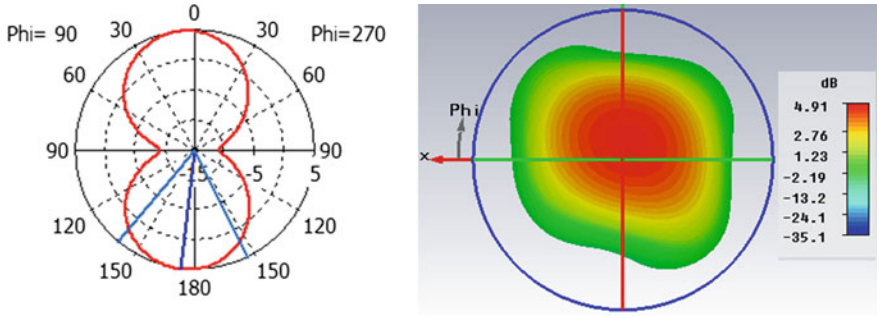


Fig. 12 Radiation pattern of dual band antenna at 2.1 GHz

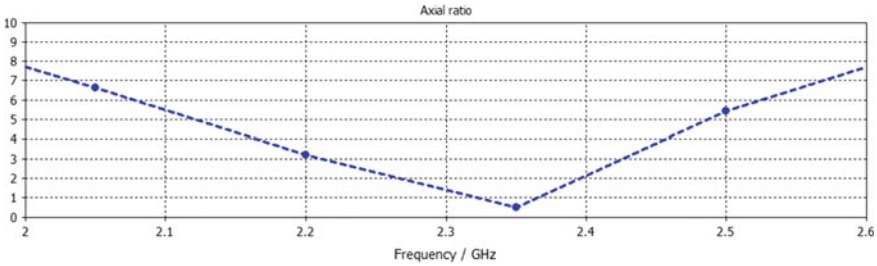


Fig. 13 Axial ratio versus frequency of broadband antenna model 1

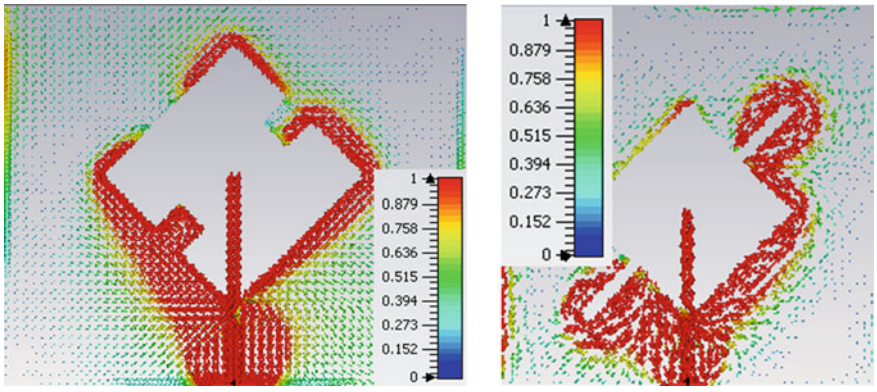


Fig. 14 Surface current density on antenna model 1 and model 2 at 2.1 GHz

4 Conclusion

Two monopole antenna models are designed in this work. The antenna model 1 is designed to operate in the broadband with circular polarization and the antenna model 2 is designed to operate in the dual band. Antenna model 1 of broadband is showing impedance bandwidth of 32% and gain more than 5 dB in the operating band. Antenna model 2 of dual band is showing impedance bandwidth of 25% at fundamental resonant frequency and 16% at second resonant frequency with gain more than 4.5 dB. The designed antenna models are showing excellent radiation characteristics in the wireless communication applications bands of mobile, wireless LAN and Bluetooth with good impedance matching.

Acknowledgements We acknowledge our sincere thanks to the management of NRI Institute, V R Siddhartha Engineering College and K L University for their support and DST through grant SR/FST/ETI-316/2012 and ECR/2016/000569.

References

1. T.-C. Yo, C.-M. Lee, C.-M. Hsu, and C.-H. Luo: Compact circularly polarized rectenna with unbalanced circular slots. IEEE Trans. Antennas Propag, vol. 56, pp. 882–886 (2008).
2. Nasimuddin, X. Qing, and Z. N. Chen: A compact circular polarized cross-shaped slotted microstrip antenna. IEEE Trans. Antennas Propag, vol. 60, pp. 1584–1588 (2012).
3. B T P Madhav, K Sai ram, M Deepika, V Naresh: Circularly Polarized Koch Fractal Triband Antenna for Communication Applications. ARPN Journal of Engineering and Applied Sciences, Vol. 10, pp. 5795–5801 (2015).
4. Ghobadi and M. Dehmollaian: A printed circularly polarized Y-shaped monopole antenna. IEEE Antennas Wireless Propag. Lett, vol. 11, pp. 22–25 (2012).
5. K Phani Srinivas et al: Novel Koch fractal circularly polarized micro strip antenna for global positioning system application. Leonardo Electronic Journal of Practices and Technologies. Vol. 27, pp. 31–40 (2015).
6. Krishna RVS Ram, Raj Kumar: Design of ultra wideband trapezoidal shape slot antenna with circular polarization. AEU-Int. J Electron Commun, Vol 67, pp. 1038–47 (2013).
7. B. T. P. Madhav, Habibulla Khan, Sarat K. Kotamraju: Circularly Polarized Slotted Aperture Antenna With Coplanar Waveguide Fed for Broadband Applications. Journal of Engineering Science and Technology, Vol. 11, pp. 267–277 (2016).
8. Kumar A, Gautam AK, Kanaujia BK: An annular-ring slot antenna for CP operation. Microwave Optic Technol Lett, Vol 55, pp. 1418–22 (2013).
9. V. Sai Krishna et al: High Bandwidth Circularly Polarized X-Slot Antenna. Far East Journal of Electronics and Communications. Vol. 16, pp. 561–572 (2016).
10. Chiang M-J, Hung T-F, Bor S-S: Dual-band circular slot antenna design for circularly and linearly polarized operations. Microwave Optic Technol Lett, Vol 52, pp. 2717–21 (2010).
11. Y. S. V. Raman et al: Analysis of Circularly Polarized Notch Band Antenna with DGS. ARPN Journal of Engineering and Applied Sciences, Vol. 11, (2016).
12. Ojaroudi Y, Ojaroudi N, Ghadimi N: Circularly polarized microstrip slot antenna with a pair of spur-shaped slits for WLAN applications. Microwave Optic Technol Lett, Vol 57, pp. 756–759 (2015).

Design of Simple PCMPA for X Band Applications

Rayapalli Sankara Rao, Pavani Tummala and R.P. Das

Abstract Proximity coupling feed is a novel electromagnetic coupling system to improve the radiation characteristics of planar antenna. In this paper, such feed technique is implemented to excite circular patch antenna with modified ground. The modeling and simulation results shows that the radiation characteristics like return loss, voltage standing wave ratio (VSWR) and gain have improved with the slot. When compared to without slot for Proximity fed Circular disk patch antenna. The simulation is carried out in HFSS and the analysis is carried using S_{11}, VSWR and radiation pattern.

Keywords X band · Patch · HFSS · Proximity coupled patch antenna

1 Introductıon

Microstrip patch antenna (MPA) is widely used now a days as a result of its quite a lot of applications such as satellite, wireless communications systems, etc. The advantages such as light weight, low volume, compatibility with built in circuits, and low price. İn the current scenario, modern wireless systems require small antenna size and has wider bandwidth. However, MPAs have disadvantages that low power handling capacity, narrow bandwidth, low gain [1].

Basically, a Microstrip patch antenna consists of a planar radiating design of desired geometrical shape on one side and a ground plane on the other side of the substrate material. Generally preferred Microstrip radiating geometries are rectangular and circular. Still, other shapes are also considered depending upon the applications.

R. Sankara Rao (✉) · P. Tummala · R.P. Das
Vignan's Institute of Information Technology, Visakhapatnam, India
e-mail: sankar0489@gmail.com

P. Tummala
e-mail: pav.tum@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_45

There are four different types of feeding techniques are available and they are Microstrip feed, Co-axial feed, Aperture coupled feed and Proximity coupling feed [2]. The commonly used and the simplest feed is the co-axial feed. The advantage being that the location of feed point can be identified with ease and freedom on the surface of the patch. However, the unwanted spurious radiation is always degrading the performance of co-axial feed [2–4].

In aperture coupled technique, it is difficult to fabricate the antenna by shielding the feed circuitry using a perfectly electric conducting plane embedded with an aperture that acts as a vent for energy transmission.

Proximity coupling feed technique is used for the proposed Microstrip antenna. In this technique, two dielectric substrates are used. In between the two substrates, feed is placed. The various techniques such as capacitive loading, inductive loading and employing parasitic stubs, etc., have been used in with the main antenna pattern to widen the bandwidth in addition to miniaturization [5]. However, this technique reduces radiation efficiency. Also, MPAs at higher microwave band offer high metallic losses there by decrease in the bandwidth, radiation efficiency and gain. The circular disk patch occupies less space compared to rectangular patch [6, 7].

In this paper, the proximity fed circular disk Microstrip patch antenna has been designed at 10 GHz frequency. The return loss is increased by putting the slot in the ground plane. For X band applications such as radar, satellite communications, wireless communication systems, and medical these proximity fed circular disk microstrip patch antennas are suitable [8].

2 Antenna Design

The Microstrip patch circular antenna consists of a ground plane placed at one side of the FR4 substrate and other side of FR4 substrate metallic circular patch is placed. The feed system in the proposed antenna uses a conducting patch running between two substrates which couples the feed indirectly to the circular patch as shown in Fig. 1. The design of proposed antenna is shown in Fig. 1. The feed line is centered with respect to the center of the radiating patch of an antenna. The two

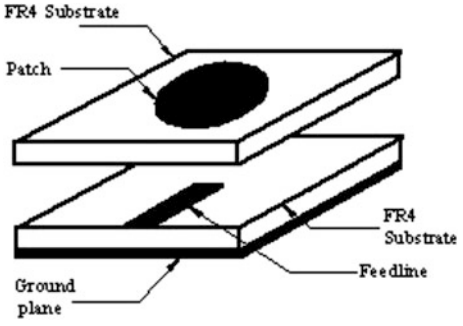


Fig. 1 The geometry of the proximity coupled patch antenna

substrates have different thickness and permittivity, but in this report, we provide for same thickness.

There are many analysis methods for the design of antenna. In this paper we are using transmission line analysis method for the design of antenna.

Step 1 **Width calculation (W)**

The Microstrip patch antenna width is given as

$$w = \frac{v_o}{2f_r}\sqrt{\frac{2}{\varepsilon_r + 1}} \tag{1}$$

c Light Velocity
f_r Resonant frequency
ε_r Antenna dielectric constant

where c = 3.0 × 10^{11} mm/s, ε_r = 4.4 and f_0 = 10 GHz, W = 9.1 mm.

Step 2 **Length calculation (L)**

Effective dielectric constant (ε_{eff})

If width is known, then calculate the effective dielectric constant for finding the length of radiating patch, therefore by knowing width and thickness of a substrate (h), then effective dielectric constant can be directly calculated and it is given by [9]

$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\frac{h}{W_f}\right)^{-1/2} \tag{2}$$

For the above specified resonant frequency the effective dielectric constant ε_{eff} = 5.69.

Length extension (ΔL)

The physical dimensions of the Microstrip antenna looks larger than its actual antenna because of Fringing field effects and width-to-height (W/h) ratio. Then the extended length is

$$\frac{\Delta L}{h} = 0.412\frac{\left(\varepsilon_{reff} + 0.300\right)\left(\frac{W}{h} + 0.264\right)}{\left(\varepsilon_{reff} - 0.258\right)\left(\frac{W}{h} + 0.800\right)} \tag{3}$$

Substituting ε_{eff} = 4.4, W = 9.1 mm and h = 1.6 mm obtain ΔL = 0.66 mm.

Actual length of patch calculation (L)

The equations mentioned above are used to calculate various parameters. The length of the patch is given by [10]

$$L = \frac{1}{2f_r\sqrt{\varepsilon_{reff}}\sqrt{\mu_o\varepsilon_o}} - 2\Delta L \tag{4}$$

Substituting L_{eff} = 6.2 mm and ΔL = 0.66 mm: L = 4.88 mm.

3 Simulation Results

The modeled antenna is simulated for the frequency range from 1 to 15 GHz. For this comparison analysis similar conditions are used for analysis of proximity coupled circular patch antennas with slot are designed. In terms of return loss and VSWR the best output for circular patch antenna is designed based on the cavity model.

The simulation-based experimentation is divided into two cases namely without and with slot. The return loss characteristics are plotted for both the cases as shown in Figs. 2 and 3. In Fig. 2, the reported return loss is 26.5 dB from Fig. 2.

In case-2 the return loss measurement is −45 dB which is better than −20 dB.

Radiation Pattern

The radiation pattern represents the relative field strength radiated by an antenna during the transmission and reception process. The patterns described in rectangular form or polar form with a strength scale of dB.

The E-Plane and H-Plane polar plots are merged and presented as shown in Fig. 4. The operating frequency is the resonant frequency of the antenna with slot. It can be inferred from the plot that the resultant antenna pattern matches with the

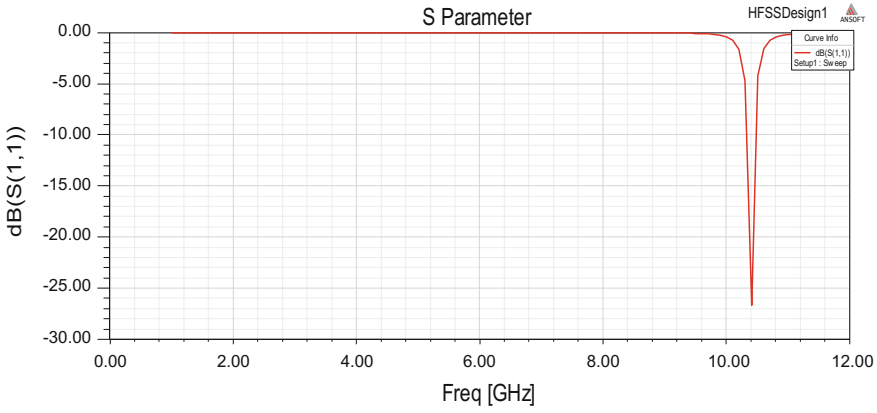


Fig. 2 Case-1 return loss plot

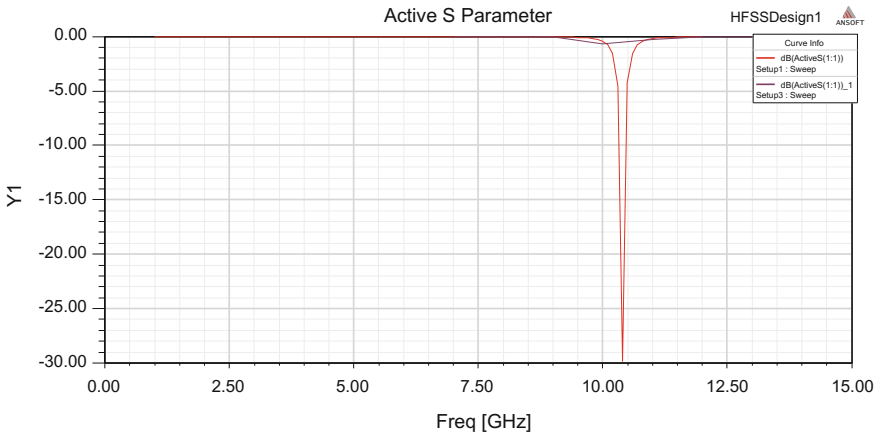


Fig. 3 Case-2 return loss plot

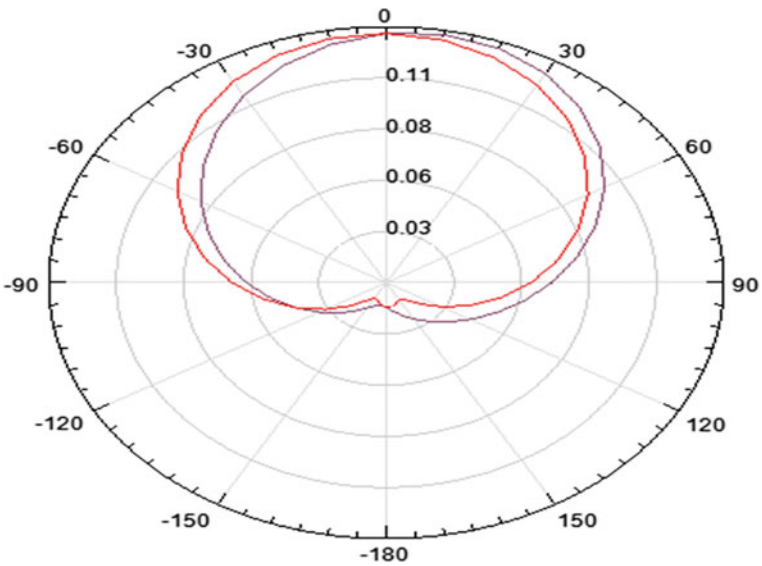


Fig. 4 Radiation pattern

template pattern of the patch antenna with maximum radiation toward the upper hemisphere and minimum radiation toward lower hemisphere.

The Fig. 5 shows frequency versus gain dB.

The antenna impedance match which is connected to the transmission line is measured with the numerical value of VSWR. Reflection coefficient is a measure used to describe the amount of power reflected from the antenna which is a function

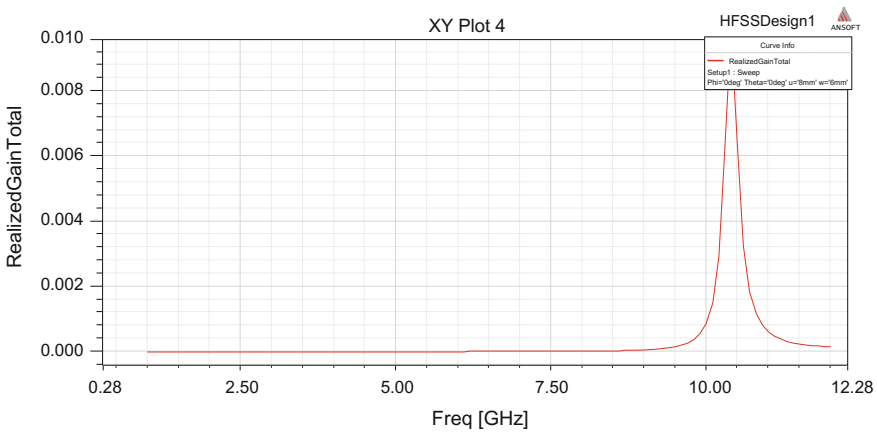


Fig. 5 Gain versus frequency

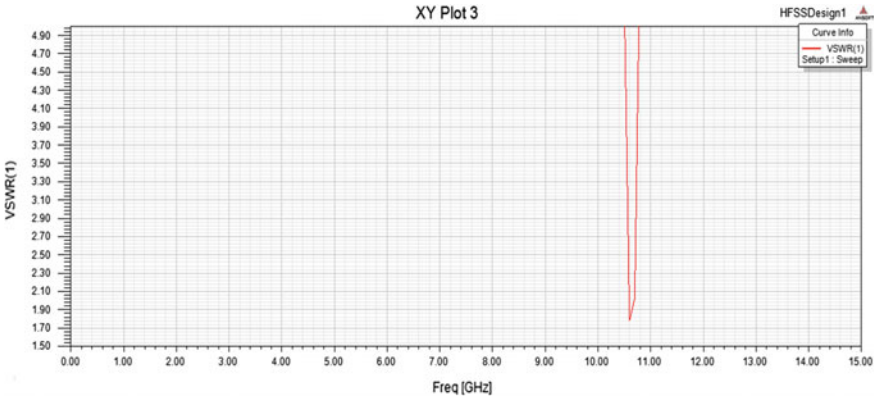


Fig. 6 Voltage standing wave ratio curve

of VSWR. The antennas VSWR can always be a real and positive number. The antenna is matched better to the transmission line and can deliver high amount of power with the lowest VSWR (Fig. 6).

4 Parametric Analysis

Figure 7 shows different resonant frequencies with different return losses. This is known as parametric analysis which performs a thorough analysis of the effect of the physical parameters on the radiation characteristics.

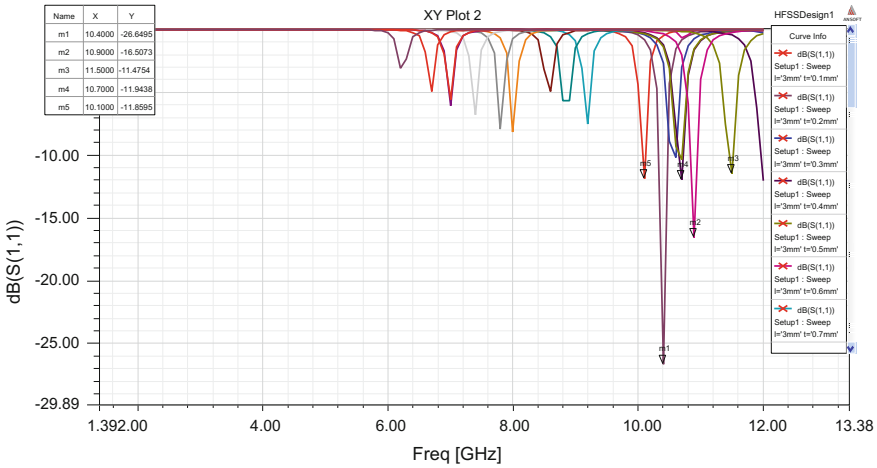


Fig. 7 Parametric study of antenna

5 Conclusion

The design, simulation,and modeling of proximity circular fed microstrip patch antenna describes the structure of an antenna is relatively simple design and quite superior in enhancing the return loss. The return loss is increased by placing the slot in the ground plane in the proximity coupled patch antenna which is compared to without slot in the ground plane. The return loss is increases to 3.5 dB. This antenna is used for X band applications.

References

1. Garg, Ramesh. Microstrip antenna design handbook. Artech house, (2001).
2. Balanis, Constantine A. Antenna theory: analysis and design. John Wiley & Sons, (2016).
3. Sastry., Rama. IVS., Jaya Sankar. K.: Proximity coupled Rectangular Microstrip Antenna with X-slot for WLAN Application. Global Journal of Research and Engineering-GJRE-F 14.1 (2014).
4. Leea, Kai Fong., Kin-Fai Tongb.: Microstrip patch antennas. (2015).
5. Borah, Kunal, and Nidhi S. Bhattacharyya. "Miniaturized patch antennas on magnetodielectric substrate for X band communications." Devices and Communications (ICDeCom), 2011 International Conference on. IEEE, 2011. (2011).
6. P.S.R Chowdary et al: Design and Performance Study of Sierpinski Fractal Based Patch Antennas for Multiband and Miniaturization Characteristics. Wireless Personal Communications, Aug., Volume 83, Issue 3, pp 1713–1730 (2015).
7. P.S.R Chowdary: "Simulation of Radiation Characteristics of Sierpinski Fractal Geometry for Multiband Applications". International Journal of Information and Electronics Engineering 3.6 Nov: 618 (2013).

8. Wood, C.: Improved bandwidth of microstrip antennas using parasitic elements. Microwaves, Optics and Antennas, IEE Proceedings H 127.4 pp: 231–234. (1980).
9. Kumar, Girish, and K. P. Ray. Broadband microstrip antennas. Artech House, 2003.
10. Guha, Debatosh, Yahia MM Antar, eds. Microstrip and printed antennas: new trends, techniques and applications. John Wiley & Sons, (2011).

Analysis and Design of Balanced Vivaldi Antenna for Triple Band Applications

Anil Kumar Patnaik, S. Suresh, A. Swathi, Lal Babu Prasad, G. Kishore Babu and Anusha Koppisetti

Abstract In this paper, a balanced Vivaldi antenna has presented. The exponential and tapered design for edge transitions and feeding is considered for enhancing the bandwidth of proposed antenna. The proposed design shows tri-band operation over 3–14 GHz frequency range with VSWR values 1.12, 1.12, 1.25 and bandwidths 7.6%, 11.4%, 2.8% at three operating frequencies 3.9 GHz, 8.7 GHz, 13.9 GHz, respectively. The proposed antenna uses at satellite broadcasting applications. All simulations are performed by HFSSv13.0 software.

Keywords Vivaldi antenna · Tapered slot · SLL

A.K. Patnaik (✉) · S. Suresh · A. Swathi
Department of ECE, Raghu Institute of Technology, Visakhapatnam, AP, India
e-mail: akp266@gmail.com

S. Suresh
e-mail: suresh.sangam@gmail.com

A. Swathi
e-mail: swathiarinana@gmail.com

L.B. Prasad
Department of ECE, Raghu Engineering College, Visakhapatnam, AP, India
e-mail: gulablal@gmail.com

G. Kishore Babu
Sri Sarathi Institute of Engineering and Technology, Nuzvid, AP, India
e-mail: gubbalakishore@gmail.com

A. Koppisetti
VNR Vignana Jyothi Institute of Engineering & Technology, Secunderabad, India
e-mail: anusha.koppisetti88@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_46

1 Introduction

The VIVALDI antenna (VA) emerged as a significant radiating system in many novel applications like biomedical, RADAR, satellite, and vehicular [1]. Considering this, the antenna has drawn the attention of many electromagnetic engineers and researchers. In the due course of time the basic design went underway many modifications tapered slot [2], flared slot, and tapered notch.

With its excellent impedance matching characteristics which is an inherent property of the flared out design made it a very good radiating element in array [3] In the due course of time, many empirical models are proposed to feature the radiation characteristics of Vivaldi antenna [4, 5]. Similarly, several numerical techniques [6] are also applied which are based on transmission line to carry out the analysis of the antenna, however, designing Vivaldi antenna for applications listed above requires large bandwidth, which is a major design issue.

The main drawback of the VA is the current distribution along the side edges which is known as edge current. These edge currents often lean to severe side lobes (SLL) in the radiation pattern using directors [7] in a way to overcome the SLL problem. These directors can be in the form of dielectrics or metamaterial [8]. Slot edges are also suggested to improve directivity by suppressing SLL [9].

In this paper, we designed a balanced Vivaldi antenna. In view of the above facts, for enhancing the bandwidth, gain and return loss is proposed to Vivaldi antenna. Hence, the proposed antenna works at tri-band applications.

Further the paper is organized as follows. The design and design steps are discussed in Sect. 2. Simulated results and discussion is given in Sect. 3. Overall conclusions are given in Sect. 4.

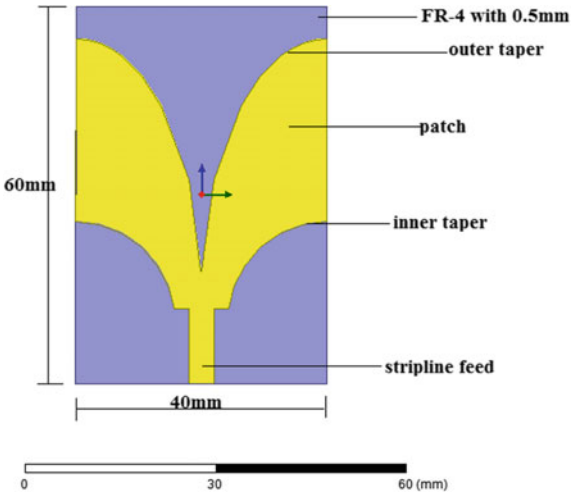


Fig. 1 Geometry and parametric values of balanced Vivaldi antenna

2 Design of Proposed Vivaldi Antenna

Balanced Vivaldi antenna has presented in Fig. 1. The proposed antenna dimensions are 40 × 60 mm^2 with FR-4 substrate having dielectric constant $\varepsilon_r = 4.4$. The antenna is fed using a microstrip line feed. The slot flare is tapered exponentially to decrease the antenna size. With the opening rate R of 0.004, of which the shape is determined by Eqs. (1) and (2) where, t_1 and t_2 are determined by the coordinates of the first and last point of the exponential equation.

$$p = t_1 e^{Rx} + t_2 \tag{1}$$

$$w = \frac{c}{2f_{min}\sqrt{\varepsilon_{eff}}} \tag{2}$$

The inner and outer edge tapers are designed as [5] using Eqs. (3) and (4)

$$x_i = \pm t_s \cdot \exp(k_s p) \mp (t_s + 0.5 \cdot t_w) \tag{3}$$

$$x_o = \pm t_w \cdot \exp\left(k_w p^{sf}\right) \mp (t_s + 0.5 \cdot t_w) \tag{4}$$

2.1 *Simulated Geometry*

See Fig. 2.

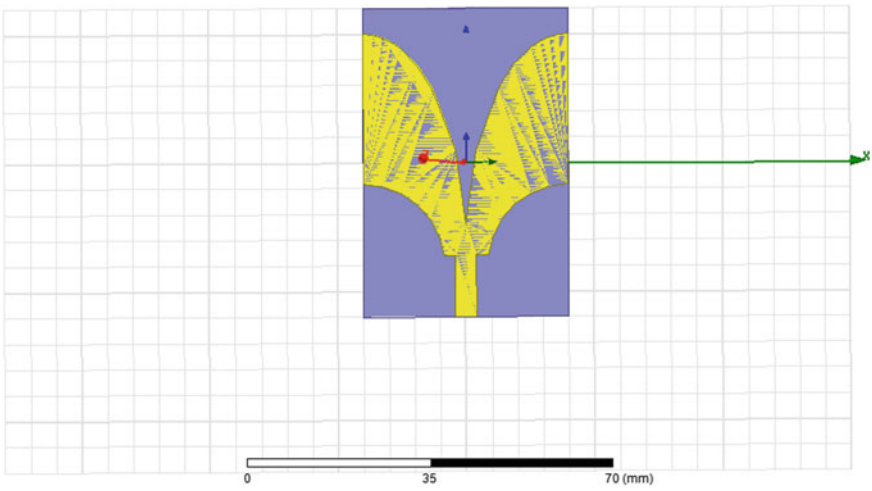


Fig. 2 Geometry of ring slot with circular patch Vivaldi antenna

3 Results and Discussions

The prototype antenna has fabricated with FR-4 substrate with $\varepsilon_r = 4.4$ and 1 mm thickness. The thickness of the patch will be 0.6 mm. The dimensions of the proposed antenna are shown in Table 1. All the simulated results of this antenna are shown in Figs. 3, 4, 5, 6, and 7.

Table 1 Parametric values of Vivaldi antenna

Substrate width	60 mm
Substrate length	40 mm
Feed line width	4 mm
Substrate height	0.6 mm
Dielectric constant	FR-4 (4.4)

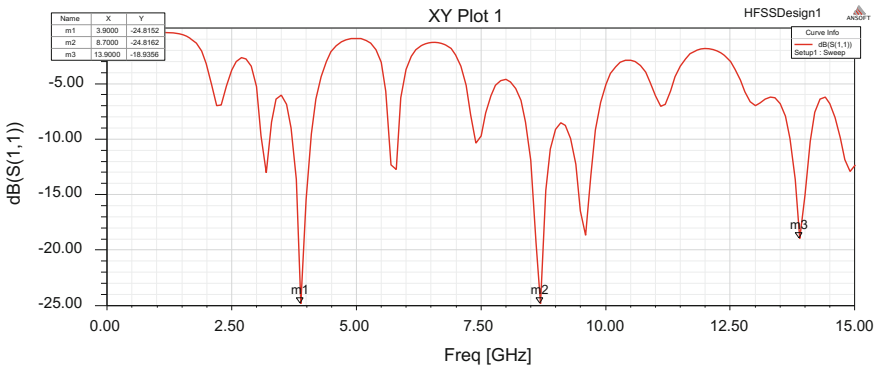


Fig. 3 Simulated return loss of balanced Vivaldi antenna

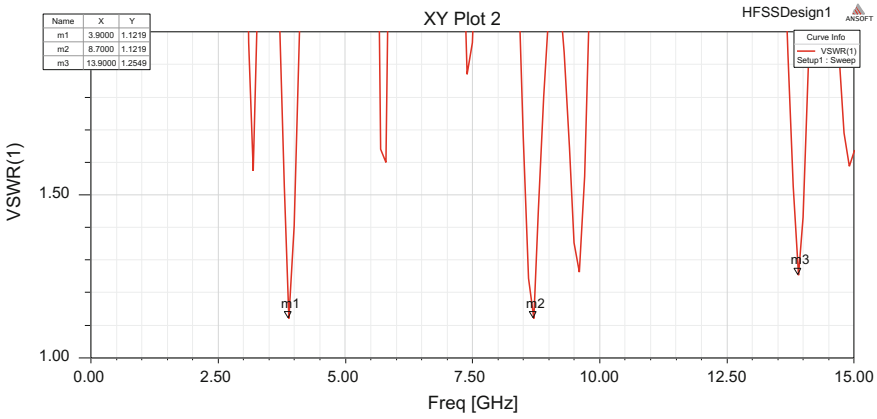


Fig. 4 VSWR response of ring slot circular patch Vivaldi antenna

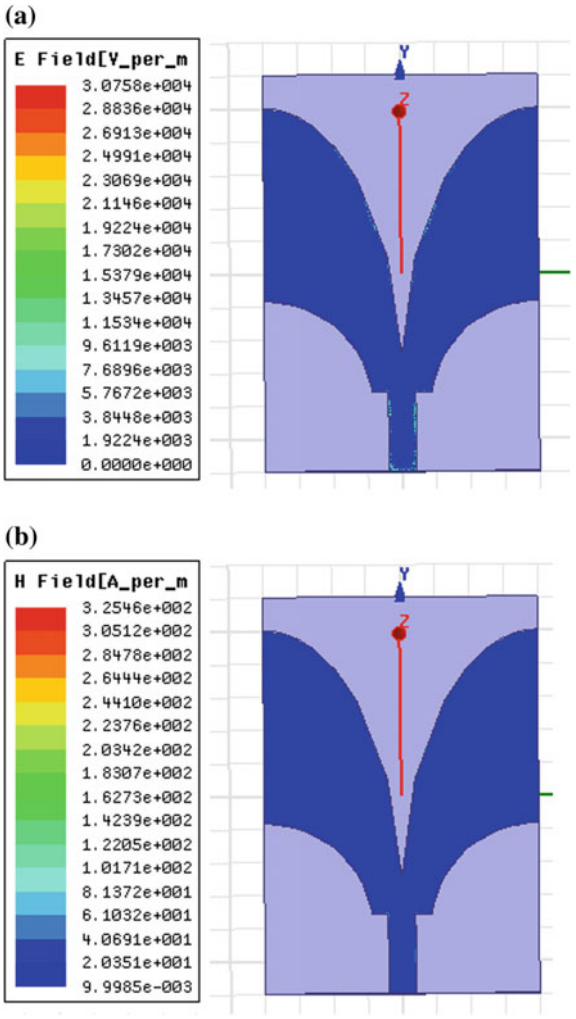


Fig. 5 The surface current flow of balanced Vivaldi antenna at **a** E-field, **b** H-field

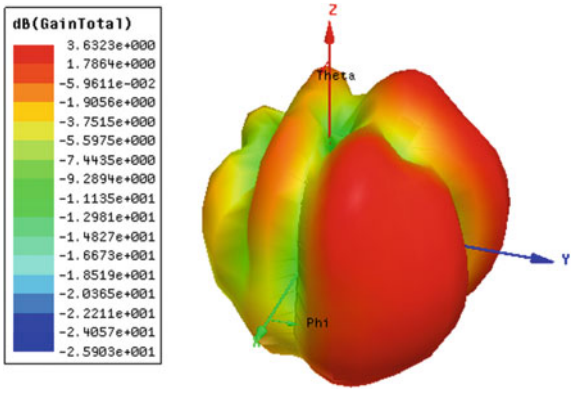


Fig. 6 Gain plot of balanced Vivaldi antenna

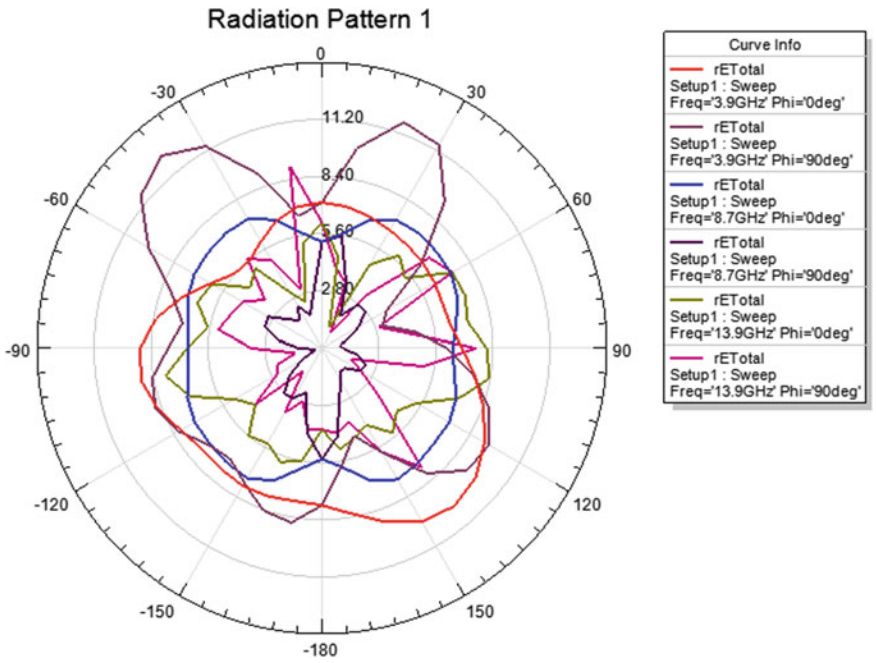


Fig. 7 Radiation patterns of balanced Vivaldi antenna at triple band frequencies

Triple operating frequency bands are obtained at 3.9 GHz, 8.7 GHz, 13.9 GHz frequencies and return loss is found −24.8 dB, −24.8 dB, −18.9 dB, respectively.

The voltage standing wave ratios for all the three resonating frequencies are less than 2 that is 1.12, 1.12, 1.25. This indicates the proposed antenna work efficiently at all the three frequencies.

4 Conclusion

The balanced Vivaldi antenna has fed with strip line. Due to exponential tapering at side of feeding line, the bandwidth of the operating frequency is increased and gain is moderately enhanced. The proposed design shows tri-band operation over 3–14 GHz frequency range with VSWR values 1.12, 1.12, 1.25 at three operating frequencies 3.9 GHz, 8.7 GHz, 13.9 GHz, respectively. So, these results are very useful at broad banding satellite applications.

References

1. Gibson, P. L.: The vivaldi aerial. in Pmc. 91th EurMicmwove Con/, Brighton, U.K. 101–105, (1979).
2. Janaswamy, R., Schaubert, D., H.: Analysis of a Tapered Slot Antenna. IEEE Transactions on Antennas and Propagation, AP-35, No. 9, 1058–1065 (1987).
3. Sang-Gyu Kim*, Kai Chang.: A Low Cross-Polarized Antipodal Vivaldi Antenna Array for Wideband Operation. IEEE (2004).
4. Bo-huaGan., Liang Zhou., Yao-Ping Zhang., Hua-hua Zhou., Jun-Fa Mao.: Design of a Dual-Band Microstrip Antenna Using Slotted Annular-Ring and Concentric Disk. IEEE (2015).
5. Aaron Zachary Hood, TutkuKaracolak, "A Small Antipodal Vivaldi Antenna for Ultrawide-Band Applications" IEEE Antennas and wireless propagation letters, vol. 7, 2008.
6. Bourqui, J., Okoniewski, M., Fear, E. C.: Balanced antipodal Vivaldi antenna with dielectric director for near-field microwave Imaging. IEEE Trans. Antennas Propag., 58, 2318–2326, (2010).
7. Juan, L., Guang, F., Lin, Y., Demin, F.: A modified balanced antipodal Vivaldi antenna with improved radiation characteristics, Microw. Opt. Technol. Lett., 55, 1321–1325, (2013).
8. P. Fei, Y. C. Jiao, W. Hu, and F. S. Zhang, "A miniaturized antipodal Vivaldi antenna with improved radiation characteristics," *IEEE* Antennas Wireless Propag. Lett., 10, 127–130, (2011).
9. Zhou, B., Li, H., Zou, X. Y., Cui, T. J.: Broadband and high-gain planar Vivaldi antennas based on inhomogeneous anisotropic zero-index metamaterials. Prog. Electromagn. Res., 120.

Sierpinski Carpet Fractal Antenna Array Using Quarter-Wave Feed Network for Wireless Applications

D. Prabhakar, P. Mallikarjuna Rao and M. Satyanarayana

Abstract This paper focuses on the Sierpinski carpet fractal antenna (SCFA) Array using quarter-wave feed network to increase the gain and impedance matching. The antenna array is designed and simulated by using HFSS software. FR4 glass epoxy having thickness of 1.6 mm and dielectric constant of 4.4 is used as a substrate material for the designing of proposed antenna. The different parameters of the array, such as radiation pattern, gain, reflection coefficients, VSWR, etc. are calculated and analyzed.

Keywords Microstrip antenna · The quarter-wave transformer feed · The corporate feed · Reflection coefficient · WLAN · HFSS

1 Introduction

Numerous self-similar geometries exist in nature, usually referred to as Fractal geometries. In 1975, the fractal geometries were first introduced by Mandelbrot [1]. The most prominent feature of Fractal geometries is self-similarity. The fractals have been exploited in antennas, radiators. The advantage of fractal geometries is that they generate increment in length in limited area, since they are repetitive. As a result of this, fractal antennas become very compact and thus are expected to have

D. Prabhakar (✉)
Department of ECE, DVR & Dr. HS MIC College of Technology, Kanchikacherla, India
e-mail: prabhakar.dudla@gmail.com

P. Mallikarjuna Rao
Department of ECE, AUCE (A), Andhra University, Visakhapatnam, India
e-mail: pmraoauece@yahoo.com

M. Satyanarayana
Department of ECE, M V G R College of Engineering (A), Vizianagaram, India
e-mail: profmsn26@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_47

Fig. 1 Sierpinski carpet square antenna with second iteration

useful applications in various communication systems. The response of fractal antenna makes a remarkable difference when compared with traditional antennas. It implies that simultaneously it has capacity of functioning at various resonant frequency bands [2–5]. Figure 1 depicts the iteration process for Sierpinski carpet fractal antenna [6, 7].

2 Patch Antennas and Feed Mechanisms

An array configuration helps bypass the lower gain and lower power handling limitations. In the construction of an array, feed network design is essential. Therefore, the magnitude and phase of each element can be controlled flexibly by the feed structure. Different types of feed networks are parallel feed, T-Split power divider, quarter-wave transformer and Mitered bend feed.

2.1 Quarter-Wave Transformer

A quarter-wave transformer plays an important role to avert a general mismatch in impedance between two points on a transmission line. Impedance matching is essential to make sure efficient power transfer through feed network. Reflection coefficient between two impedances Z1 and Z3 is reduced by a matching circuit. The quarter-wave transformer is represented in Fig. 2. At the center frequency, a

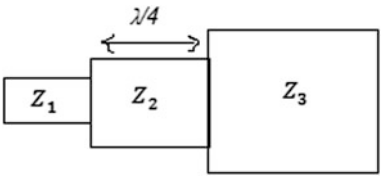


Fig. 2 Quarter-wave transformer

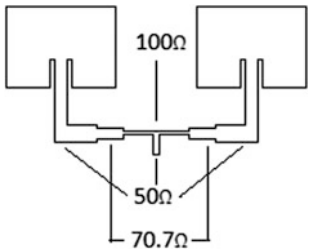


Fig. 3 Two-element corporate-fed microstrip array with quarter-wave element transformer

section of transmission line of length λ/4 (the quarter-wave transformer) is placed between the two transmission lines eliminating the reflection coefficient if its impedance is $Z_2 = \sqrt{Z_1 Z_3}$. A 2-corporate-fed micro strip uniform array is illustrated in the Fig. 3.

3 Design Consideration

The patch dimensions are evaluated using the formulae given below [8–13]:

A. *Width of the patch (W):*

$$W = \frac{c}{2f_0\sqrt{(\varepsilon_r + \frac{1}{2})}}, \tag{1}$$

where $c = 3 \times 10^8$ m/s

B. *Actual Length of the patch (L):*

$$L_{eff} = \frac{c}{2f_0\sqrt{\varepsilon_{reff}}}, \tag{2a}$$

where

$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[1 + 12\frac{h}{W}\right]^{-\frac{1}{2}} \tag{2b}$$

$$L = L_{eff} - 2\Delta L \tag{3}$$

$$\frac{\Delta L}{h} = 0.412\frac{(\varepsilon_{reff} + 0.3)\left(\frac{W}{h} + 0.264\right)}{(\varepsilon_{reff} - 0.258)\left(\frac{W}{h} + 0.8\right)} \tag{4}$$

C. *Feed width of the patch (W_f):*
To achieve 50 Ω characteristic impedance, the required feed width to height ratio $\left(\frac{W_f}{h}\right)$ is computed as

$$\frac{W_f}{h} = \begin{cases} \frac{8e^A}{e^{2A}-2} \frac{W_0}{h} \le 2 \\ \frac{2}{\pi}\left\{B - 1 - \ln(2B-1) + \frac{\varepsilon_r - 1}{2\varepsilon_r}\left[\ln(B-1) + 0.39 - \frac{0.61}{\varepsilon_r}\right]\right\} \frac{W_0}{h} \ge 2 \end{cases}, \quad (5a)$$

where

$$A = \frac{Z_0}{60}\sqrt{\frac{\varepsilon_r + 1}{2}} + \frac{\varepsilon_r + 1}{\varepsilon_r - 1}\left(0.23 + \frac{0.11}{\varepsilon_r}\right) \quad (5b)$$

$$B = \frac{377\pi}{2Z_0\sqrt{\varepsilon_r}} \quad (5c)$$

D. *The no. of iteration is*

$$N_n = 8^n \quad (6)$$

E. *The ratio of fractal length is,*

$$L_n = \left(\frac{1}{3}\right)^n \quad (7)$$

F. *The ratio for the fractal area after the n*th *iteration is,*

$$A_n = \left(\frac{8}{9}\right)^n \quad (8)$$

where n is iteration *n*th stage number.

4 Results and Discussion

4.1 Dimensions of Sierpinski Carpet Fractal Antenna

The dimensions of the patch are 27 mm × 9 mm. By taking scale factor 1/3, the basic square patch is divided by removing the middle square from it for constructing the iteration. Thus, keeping the first iteration constant, a rectangular slot of

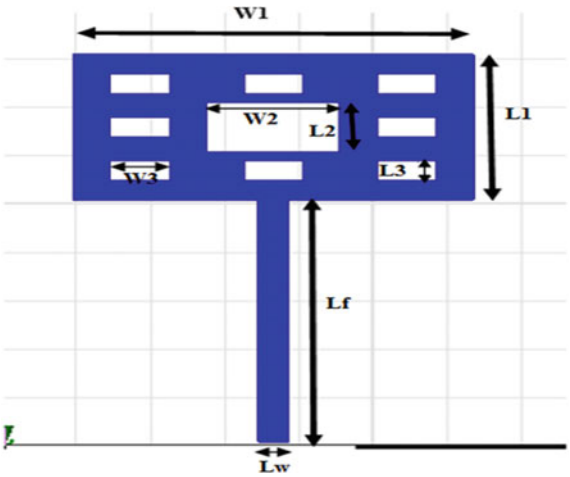


Fig. 4 Structure of single-element Sierpinski carpet fractal antenna

Table 1 Dimensions of single-element carpet fractal antenna

Design Parameter	Value (mm)
W1	27
W2	9
W3	4
L1	15
L2	5
L3	2
Lf	25
Lw	2

dimensions 9 mm × 5 mm is formed. For the second iteration, the segments are formed on the remaining eight squares following maintaining the scale factor of 1/3rd. It is formed with the dimensions of 4 mm × 2 mm as shown in Fig. 4 and corresponding dimensions in Table 1.

Two-element Sierpinski carpet antenna array with quarter-wave feed network is designed and fabricated with the Design equations and is shown in Figs. 5 and 6, respectively. Simulated and practical results such as reflection coefficient, VSWR and gain are observed in Figs. 7, 8, 9, 10 and 11 respectively as shown in Table 2.

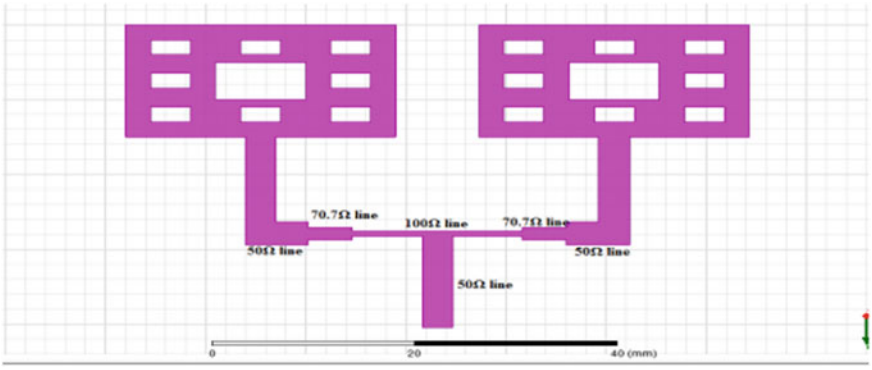


Fig. 5 Geometry for two-element antenna array of quarter-wave feed network

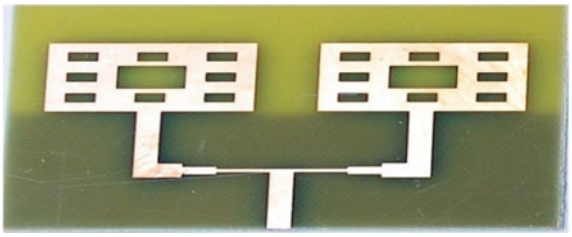


Fig. 6 Fabricated patch of two-element antenna array of quarter-wave feed network

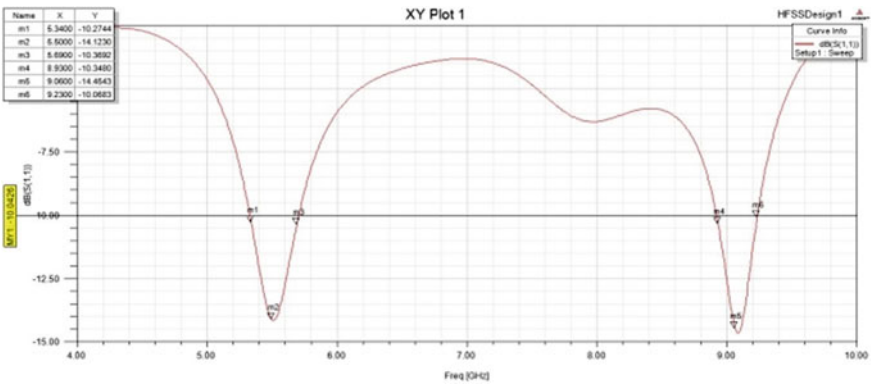


Fig. 7 Reflection coefficient curve of the two-element antenna array of quarter-wave feed network

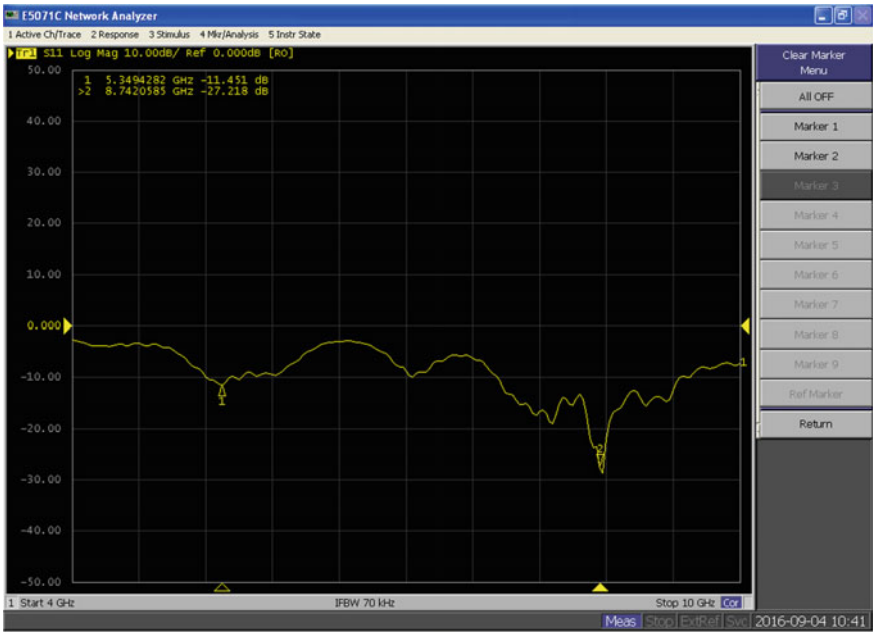


Fig. 8 Reflection coefficient curve of fabricated two-element antenna array of quarter-wave feed network

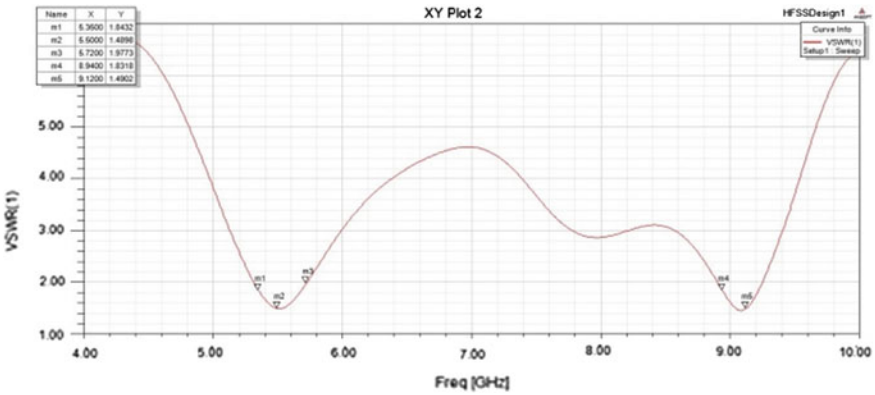


Fig. 9 VSWR curve of the two-element antenna array of quarter-wave feed network

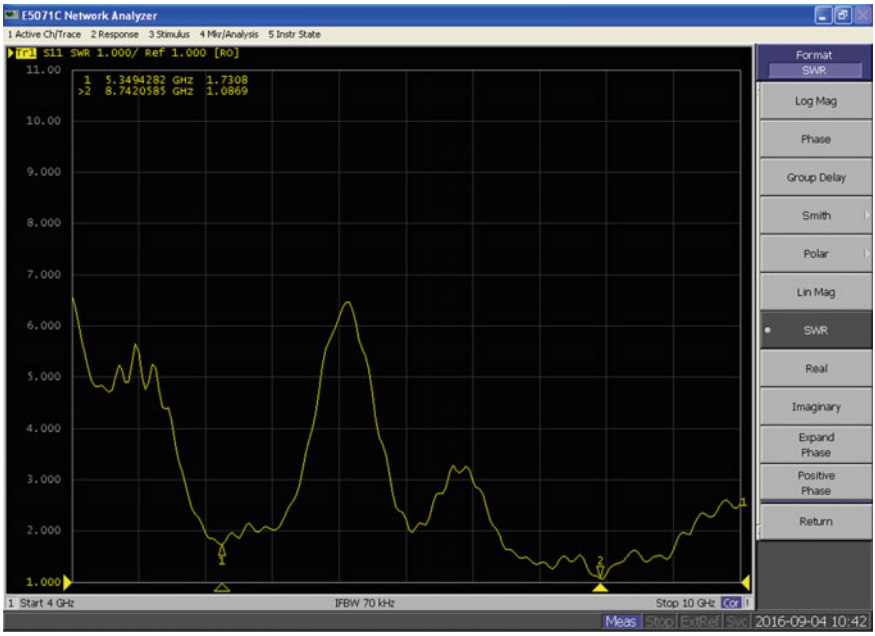


Fig. 10 VSWR of fabricated two-element antenna array of quarter-wave feed network

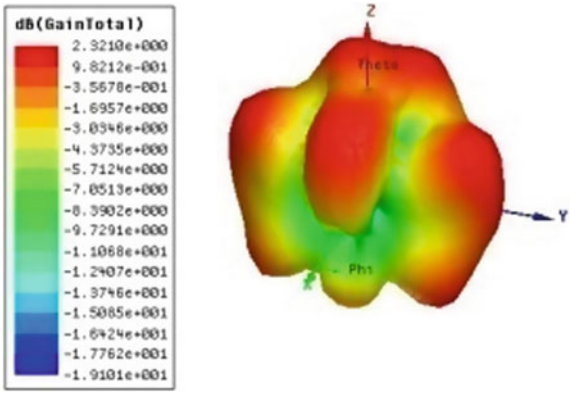


Fig. 11 Gain plot of the two-element antenna array of quarter-wave feed network

Table 2 Results of two-element Sierpinski carpet antenna array with quarter-wave feed network

Type of patch with feed network	Resonant frequency (GHz)		Reflection coefficient (S11) (dB)		VSWR		Gain (dB)
	Simulated	Measured	Simulated	Measured	Simulated	Measured	Simulated
Two-element carpet antenna array with Quarter-wave feed network	5.5 9.06	5.34 8.74	−14.123 at 5.5 GHz −14.45 at 9.06 GHz	−11.45 at 5.34 GHz −27.21 at 8.74 GHz	1.48 at 5.5 GHz 1.49 at 9.12 GHz	1.7 at 5.3 GHz 1.8 at 8.74 GHz	2.82

5 Conclusion

In this paper, Sierpinski carpet fractal antenna (SCFA) array is designed and implemented by using quarter-wave feed network. Then there is an observed improvement in gain from 1.77 dB (single element) to 2.82 dB (2 elements). The obtained results are used in ISM multiband band applications. The number of resonant frequencies increases with an increase in the fractal iterations. The obtained results show a good performance in terms of reflection coefficient S11 and size.

References

1. Douglas H., and Raj Mittra, eds. Frontiers in electromagnetics. Vol. 2. Wiley-IEEE Press, pp. 48–81, (2000).
2. D.C. Pande.: Design and Implementation of circular square fractal antenna based on UWB communication for EMI applications: INCEMIC, Proceedings, pp. 201–206, (2012).
3. C. A. Balanis.: Antenna theory analysis and design: (3rd ed.), (2005).
4. V. H. Rumsey.: Frequency Independent Antenna: Academic Press, New York and London, (1966).
5. Cohen. N.L.: Fractal Antennas Part 1: Communications Quarterly, Summer, pp. 5–23 (1995).
6. Hohlfeld, R.G. and Cohen, N. L.: Self Similarity and the Geometric Requirements for Frequency Independence in Antennas: Fractals, 7, pp. 79–84 (1999).
7. S. N. Khan, J. Hu, J. Xiong, and S. He.: Circular fractal monopole antenna for low VSWR UWB applications: Progress in Electromagnetic Research Letters, Vol. 1, pp. 19–25, (2008).
8. Werner, D. H. and S. Ganguly.: An overview of fractal antenna engineering research: IEEE Antennas and Propagation Magazine, Vol. 45, No. 1, 38–57, (2003).
9. C. Puente, J. Romeu, R. Pous, and A. Cardama.: On the behavior of the Sierpinski multiband fractal antenna: IEEE Trans. Antennas Propagat., vol. 46, pp. 517–524, Apr. (1998).
10. D.C. Pande.: Design and Analysis of a UWB Antenna pulse generating System: INCEMIC, Proceedings, pp. 393–398, (2012).
11. R. Garg, Micro strip antenna design handbook. Boston, Mass. [u.a.]: Artech House, (2001).
12. D. Prabhakar, Dr. P. Mallikarjuna Rao, Dr. M. Satyanarayana.: Design and Performance analysis of Micro strip Antenna using different ground plane techniques for WLAN application: International Journal of Wireless and Microwave Technologies, Vol. 06, Issue. 04, pp: 48–58, July (2016).
13. D. Prabhakar, Dr. P. MallikarjunaRao, Dr. M. Satyanarayana.: Characteristics of Patch Antenna with Notch gap variation for Wi-Fi Application: International journal Applied Engineering Research, Vol. 11, Issue. 0 8, pp: 5741– 5746, April (2016).

Design and Performance Analysis of Slotted Ground Patch Antenna with Shaped Radiating Stub

J. Prasanth Kumar and G. Karunakar

Abstract The bandwidth (BW) of the antenna can be enhanced by generating multi-resonant structures on the patch as well as modifying the ground plane. In this paper, one such attempt by designing a patch antenna with ground plane consisting of a wide slot and modified radiating patch. The radiating patch which is known as the radiating stub is confined to the projection of the slot of the ground on the patch surface. Various geometries of the stub are considered, where each geometry corresponds to specific radiation characteristics according to the current distribution on its surface. The characteristics of the designed antenna are studied using simulated reports like return loss (S11), Voltage standing wave ratio (VSWR), radiation pattern and field distribution plots. The antenna is simulated using CST microwave studio.

Keywords Patch antenna · Bandwidth · Radiating stub · Multi-resonant

1 Introduction

The trend of UWB-based communication system took an accelerating form with the announcement of the entire UWB spectrum [1] as unlicensed. With this, the research focus is directed to the design and development of impulse system. Moreover, designing radiating system for such UWB system is considered as a major problem [2]. Functionally, the design problem is twofold. On one side the radiating system should be capable of covering UWB spectrum and on the other side [3] it should also create an interference free environment with the existing system. In addition to the radiation characteristics, the antenna also should be

J. Prasanth Kumar · G. Karunakar (✉)
Department of ECE, Gitam Institute of Technology, Gitam University, Visakhapatnam, AP, India
e-mail: profkarunakar@gmail.com

J. Prasanth Kumar
Department of ECE, Ramachandra College of Engineering, Eluru, India

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*, Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_48

conformal, simple as well as miniatured. Patch antenna is a best candidate for such applications. However, these patch antennas suffer major setback with their narrow bandwidth. Hence several broad band techniques are proposed for patch antennas. Several multi-resonant structures are proposed for multiband applications like wireless LAN (WLAN), wimax and wifi [4–7]. In this paper, such an attempt to enhance the bandwidth has been made by suggestion modified ground with slot and shaped radiating stub.

Further the paper is organized as follows. The antenna design is given in Sect. 2. Simulation model and case wise results are mentioned in Sect. 3. Overall conclusion is given in Sect. 4.

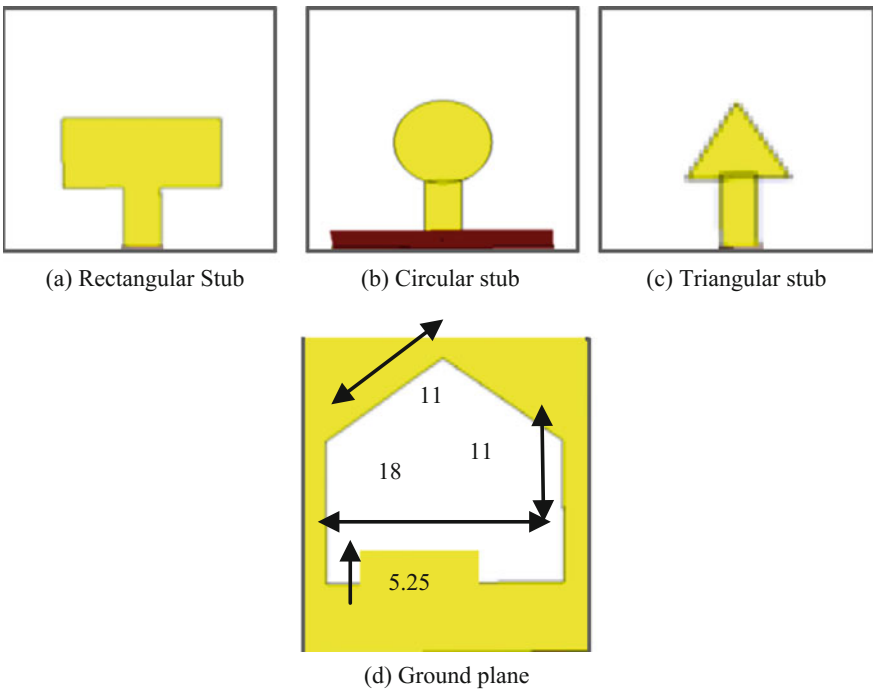
2 Antenna Design

The design of proposed patch antenna constitutes of a microstrip feed. The corresponding ground plane consists of simple slot of regular triangle merged with rectangle. Radiating stubs of different shapes are structured on the patch in the area projected of the area projected of the slot on the top surface. The etched slots are able to achieve a broadband operation at high frequency. The additional resonant modes are excited with the use of a strips embedded in the rectangular slot.

The shape of the stub protruding into the space projected by the slotted ground plane on the other side of the substrate is modified for wide study on the impact of the geometry on the resonant frequencies and its bandwidth. In this regard, the stub has been modified to different shapes like rectangle, circular disc and triangle. Accordingly, the geometry of the proposed antennas using different shaped stubs are as shown in Fig. 1. The rectangular stub is given Fig. 1a, the circular disc-shaped stub is given in Fig. 1b and the corresponding simulated antenna with triangular stub is as shown in Fig. 1c. The common ground plane shape for all the three models is as shown in Fig. 1d. The rectangular size of the rectangular stub is 13×7 mm^2, the radius of the circle is 9 mm and side length of the triangle is 7 mm. The microstrip line feed length is 6 mm and width is 3 mm. The antenna is designed on FR4 substrate of thickness of 1.6 mm, dielectric constant 4.4 and the size of the proposed design is 22×24 mm^2

3 Results and Discussions

Results pertaining to three models for analysis of their radiation characteristics are presented in this Section as follows. For preliminary conclusion on the resonant characteristics, the corresponding return loss and VSWR plots are simulated. Later, the radiation pattern plots are taken in order to verify with the basic radiation characteristics of the patch antenna. Further, for the analysis of the radiation patterns, the corresponding E-field and power flow distribution are simulated on the



(a) Rectangular Stub (b) Circular stub (c) Triangular stub

(d) Ground plane

Fig. 1 Design of proposed antenna

respective geometries. The parametric analysis of the geometry allows to study the impact of the physical dimensions of the antenna on its resonant characteristics. With reference to this, the results description for each geometry are divided and presented in three cases as follows.

3.1 Case-1: Rectangular Stub

The return loss simulated for the rectangular stub radiator -based slot antenna is as shown in the Fig. 2a. The corresponding VSWR plot is as shown in Fig. 2b. Basic resonant band of frequencies is identified to be existing from 3.5 to 12 GHz which is even evident from the VSWR plot. Considering this, two resonant frequencies are taken from this bandwidth for whom the corresponding radiation pattern polar plots are obtained for theta = 0–360 and phi = 0. The two resonant frequencies identified are 5 and 8 GHz and the corresponding radiation patterns are as shown in Fig. 2c, d.

The E-field, H-field distribution plots and the power flow pattern on the surface of the radiating stub are as shown in Fig. 3a–c. From the plots it can be inferred that the main lobe occurs in the region on the patch, where there is high density of

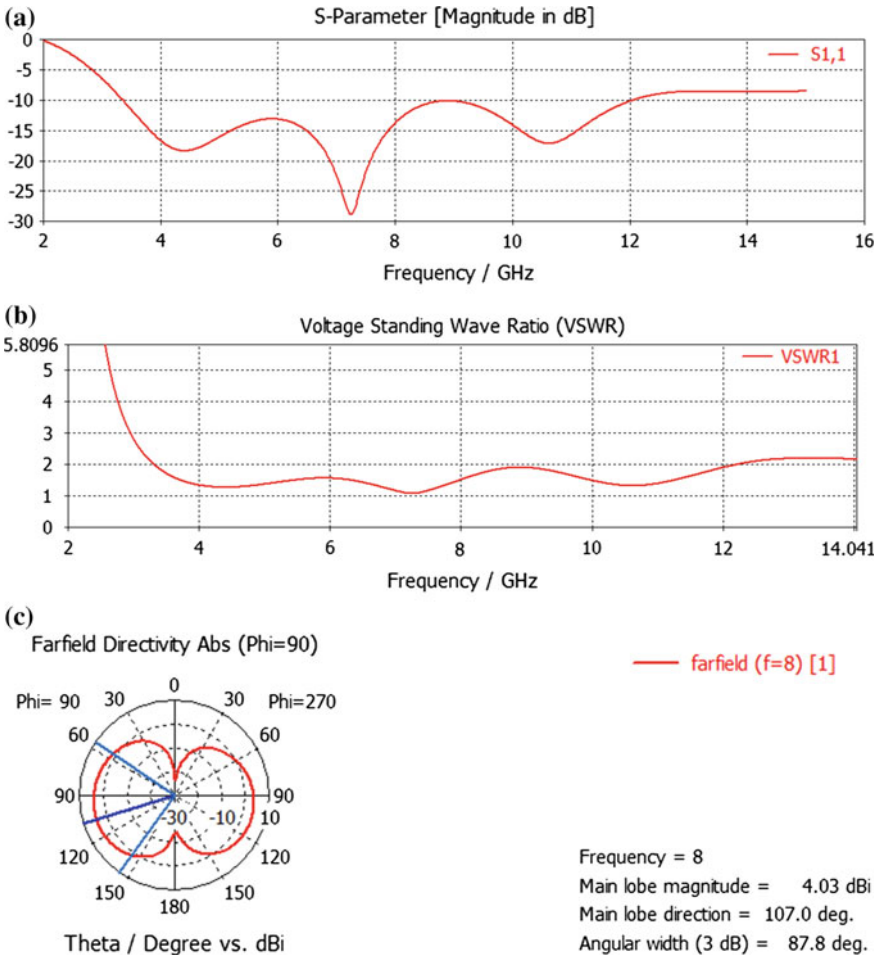
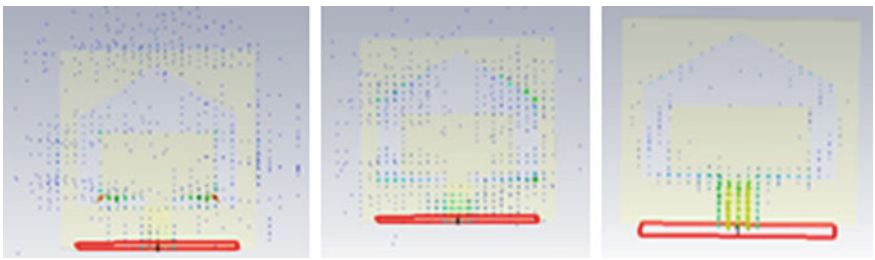


Fig. 2 Results of rectangular stub



(a) E-field (b) H-field (c) Power flow

Fig. 3 Field distribution of rectangular stub

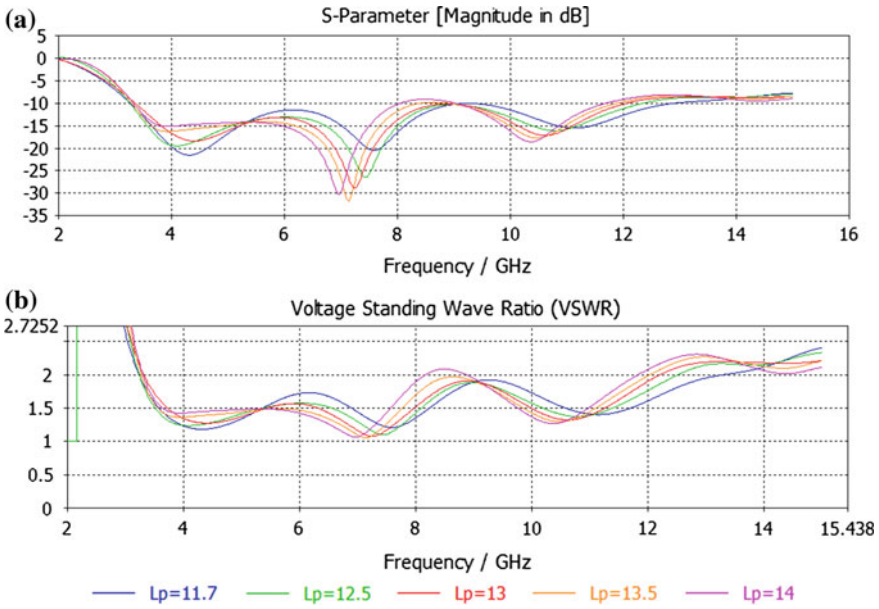


Fig. 4 Parametric sweep

current and field distribution while the null appears at region where the current is minimum.

The parametric analysis with varying Lp over a range of (11.7, 12.5, 13, 13.5, 14 mm) is performed and the corresponding return loss and VSWR are obtained. From both the plots shown in Fig. 4a, b, it is clear that the impact of the length of the stub has not much impact on the radiation characteristics. However, a narrow notch band is visible with increasing Lp after 8 GHz.

3.2 Case-2: Circular Disc Stub

The simulated return loss and VSWR plots for the circular disc stub radiator-based slot antenna are as shown in the Fig. 5a, b. The bandwidth raging from 3 to 5 GHz is evident from the both the return loss and VSWR plots. Considering this, radiation pattern polar plot is obtained for 3.5 GHz resonant frequencies as shown in Fig. 5c.

The field distribution plots and power flow plots are presented in Fig. 6a–c. The radiation pattern plots are completely governed by these field distribution plots.

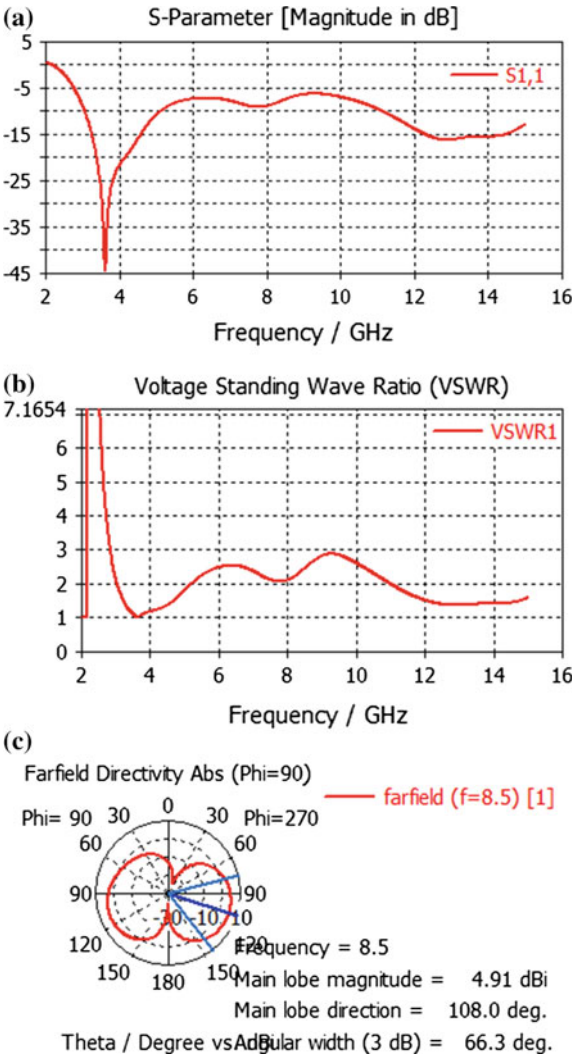
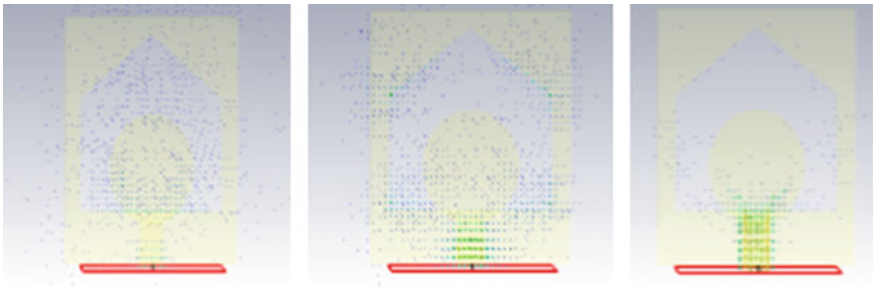


Fig. 5 Return loss, VSWR plots and radiation patterns of circular stub

3.3 Case-3: Triangular Stub

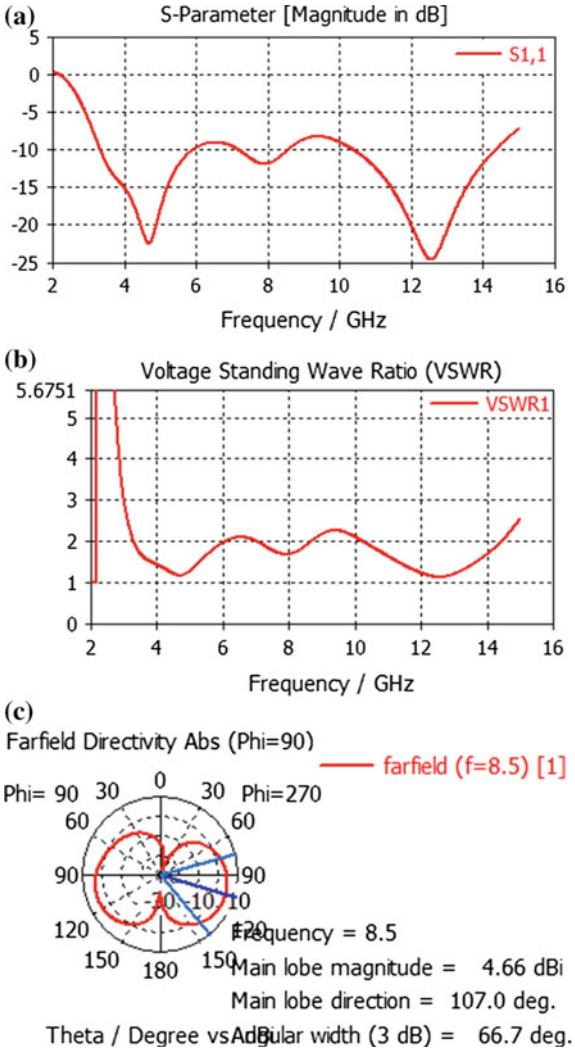
The return loss and VSWR plots are simulated for the triangular stub radiator as shown in Fig. 7a, b. The resonant frequencies are 4.7 and 12.5 GHz. The BW of first band is ranging from 3.5 to 6 GHz and the for the second band the BW is measured to be existing from 10 to 14 GHz. Considering this, two resonant frequencies are considered for plotting polar 2D radiation pattern polar plots which are presented as shown in Fig. 7c.

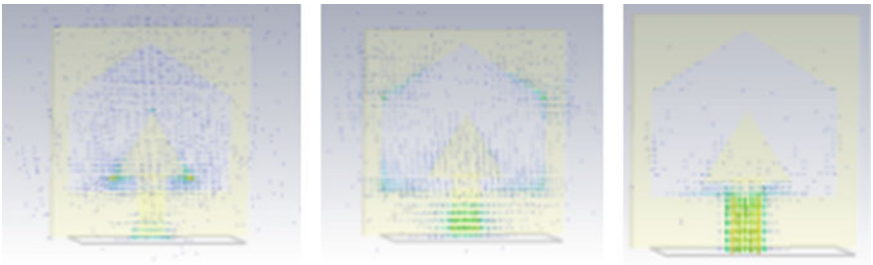


(a) E-field (b) H field (c)Power flow

Fig. 6 Field distribution of circular stub

Fig. 7 Results of triangular slot antenna





(a) E field (b) H field (c) Power flow

Fig. 8 Field distribution of triangular stub

The corresponding E and H field distribution along with the power flow animation plots are presented in Fig. 8a, b. The study of the radiation patterns can be performed using these plots. The broad-side distribution of the maximum radiation is evident from these plots.

4 Conclusion

Slot loaded patch antenna fed with microstrip line feed network is designed and simulated with different shaped radiating stubs. It can be concluded from the radiation characteristics like return loss, VSWR, radiation patterns and field distribution plots that the resonant behaviour of the antennas is different from each other. The rectangular stub reported a wide BW while the triangular observed a split in the wide band into two bands. Similarly, the circular stub resulted in a single band of resonant frequencies. It is observed that the slot loading certainly increased the BW and further the shape of the radiating stub dictates the BW. In future work, introducing notch characteristics in the antenna is better utilization of UWB band.

References

1. Federal communications commission: revision of part 15 of the commission's rules regarding ultra-wideband transmission system from 3.1 to 10.6 GHz. in Federal Communications Commission, 98–153, ET-Docket, Washington, DC, USA, (2002).
2. Sörgel, W., Wiesbeck, W.: Influence of the Antennas on the Ultra Wideband Transmission. EURASIP Journal on Advances in Signal Processing, (2005).
3. Wiesbeck, W., Adamiuk, G., Sturm, C.: Basic Properties and Design Principles of UWB Antennas. Proceedings of the IEEE, 97(2), 372–385, (2009).
4. Ihsan, Z., Solbach, K.: Frequency Invariant Far-Field Beam Pattern of UWB Printed Circular Monopole Antenna Array. in German Microwave Conference (GeMiC), (2012).
5. Balanis, C.: Antenna Theory: Analysis and Design. John Wiley & Sons, (2005).

6. Chowdary P. S. R. et. al.: On the Multiband and Miniaturization Characteristics of Sierpinski Fractal based Patch Antenna for Wireless Applications. Springer-Telecommunications Systems Journal, Accepted. ISSN: 1018-4864.
7. Rezaul Azim, Mohammad Tariqul Islam, Norbahiah Misran, Baharudin Yatim, Haslina Arshad,: Design and Realization of a Planar Ultrawideband Antenna with Notch Band at 3.5 GHz. The Scientific World Journal, Article ID 563830, 7 pages, (2014).

Design and Study of Serially Fed Array Antenna for Ultra-Wideband Applications

Venkateswara Rao Tumati and Anilkumar Tirunagari

Abstract Microstrip array antennas are gaining the attention in research due to the benefits of improvement in gain and directive characteristics. Feed system pertaining to the microstrip array antennas is interesting domain. In this paper, the design of an array antenna is discussed with the objectives of improving the gain along with the achievement of ultra-wideband operating bandwidth. Series feed, partial ground, and stepped truncated patch are used in the array for obtaining desired characteristics. Design of antenna carried out with microstrip line and CPW feed. The spectral characteristics namely reflection loss, VSWR and radiation characteristics in terms of the peak gain as well as radiation patterns are studied which are obtained by 3D modeling of the array structures and the simulation carried out in ANSYS HFSS 15.0.

Keywords Microstrip antenna array · Series feed · VSWR · Microstrip line feed · CPW feed · Gain · HFSS

1 Introduction

The concept of antenna array deals with the spatial infrastructure of multiple radiating elements with the objective of achieving the improved gain and directive radiation performance of the antenna. The sandwiched structure of metallization layers and insulating dielectric material in between them is called the microstrip patch antenna, which is usually having a narrow operating band and radiates with low gain [1]. Antenna element with greater in dimensions will provide improved gain at the cost of huge space accommodation which is not preferable in most of the

V.R. Tumati (✉) · A. Tirunagari
Department of Electronics & Communication Engineering,
Sir C. R. Reddy College of Engineering, Eluru, Andhra Pradesh, India
e-mail: tumati01@gmail.com

A. Tirunagari
e-mail: aniltech8@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_49

communication devices nowadays. The gain improvement of a patch antenna can be done by implementing the array structures instead of increasing the size of the radiating element [2]. Researchers have been extended the array topologies for MPAs and achievement of gain along with operating bandwidth is a challenging task. Some of the works are presented in [3–7]. In [8], a five-element linear array design has been proposed for UWB applications with CPW feed.

In this paper, we have discussed the implementation of linear array for a UWB monopole antenna by increasing the number of radiating elements in series with series feed configuration also the CPW feed configuration of same array has been presented.

2 Construction of Proposed Series Fed Array Antenna

2.1 Design of Three-Element Series Fed Array Antenna (SFAA)

The geometrical modeling of array antenna is started by considering a UWB planar monopole antenna. The patch shape is considered as rectangular one. The microstrip line feed with width 'W_f' is used to give excitation of the patch. The width of the feed line is calculated using the expression given in [1] as,

$$\frac{W}{d} = \frac{2}{\pi}\left[B - 1 - \ln(2B-1) + \frac{\epsilon_r - 1}{2\epsilon_r}\left\{\ln(B-1) + 0.39 - \frac{0.61}{\epsilon_r}\right\}\right] \quad for \quad W/d < 2 \tag{1}$$

$$where \quad A = \frac{Z_0}{60}\sqrt{\frac{\epsilon_r + 1}{2}} + \frac{\epsilon_r - 1}{\epsilon_r + 1}\left(0.23 + \frac{0.11}{\epsilon_r}\right), B = \frac{377\pi}{2Z_0\sqrt{\epsilon_r}}$$

In order to design the compact antenna, the dimensions of the patch are considered which corresponds to the higher resonant frequency that exists in UWB spectrum. The ground plane beneath the substrate bottom is defected by partial metallization. Usually, the rectangular patch antenna is having two radiating slots among one of which is at the patch-feed interface and another is exactly opposite to it. The radiating slot at the patch-feed interface is truncated in two steps. To design the UWB antenna some of the antenna geometrical features are extracted from [9]. The above-mentioned geometrical modification enhances the bandwidth of the resonant rectangular patch antenna to the ultra-wideband.

Such single element UWB antenna is cascaded serially to form multielement antenna array. The geometrical configuration of three-element antenna is shown in Fig. 1a, b. The inter-element distance between the patch elements will impact the radiation characteristics of the array antenna. The cascade topology introduces reflection loss and thus creates undesired notches in its frequency response. In order

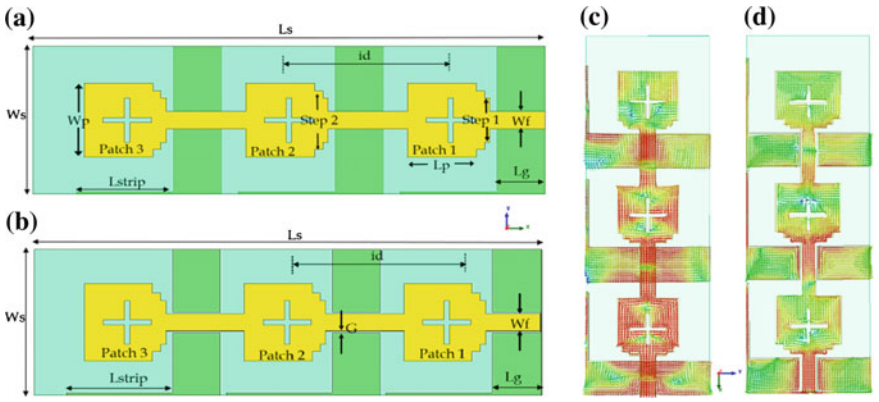


Fig. 1 Geometry of three-element **a** microstrip line SFAA, **b** CPW feed SFAA and Surface current distribution on three-element, **c** microstrip line SFAA, **d** CPW feed SFAA

Table 1 Series-fed array antenna design parameters

Geometrical attribute	Parameters and values	
Substrate	L_s = 95.3 mm	W_s = 30 mm
Patch	L_{patch} = 12.75 mm	W_{patch} = 16 mm
Step1	L_{step1} = 1 mm	W_{step1} = 9 mm
Step2	L_{step2} = 1.5 mm	W_{step2} = 12 mm
Ground plane	L_g = 8.97 mm	W_g = 30 mm
Strip	L_{strip} = 18 mm	W_{strip} = 0.5 mm
Feedline	L_f = 10.25 mm	W_f = 3.5 mm
CPW Gap	G = 0.35	

to compensate this, the partial ground metallization is extended with a thin rectangular strip placed at the one edge of the substrate and aligned along its length-wise. In the similar fashion, the three-element and four-element array configurations are designed for all structures the dielectric substrate with relative permittivity of 4.4 is used. In [10], it was suggested that the ultra-wide impedance bandwidth can be enhanced by etching slots on the planar patch. Hence, two cross-shaped slots (9 mm × 1 mm) were adopted on patch in order to improve return loss response of the array antenna. The array configuration with serially fed coplanar waveguide feed is also designed and shown in Fig. 1 which consists of two ground planes at either side of the signal conductor (microstrip line) and separated by some gap G which is designed using the expressions given in [1]. The surface current distribution plots shown in Fig. 1c, d shows the existence of phase difference of $\pi/2$ between successive elements which can be seen from the reversal of current directions. The geometrical parameters of the proposed array configurations are presented in Table 1.

3 Simulation Results of Proposed SFAA

The EM simulations of the different antenna array iterations were performed under high frequency structure simulator (HFSS) tool and several antenna performance parameters are obtained from the simulation results namely the reflection loss at the antenna port, VSWR and the radiation far-field gain and corresponding field patterns. The antenna simulations were carried out with two substrates: one with FR4 and Rogers TMM4 which are having relative permittivity values 4.4 and 4.5 and loss tangent of 0.02 and 0.002, respectively.

3.1 Return Loss (S_{11})

The return loss of the different antennas is plotted w.r.t frequency and a combined plot is generated and shown in Fig. 2. The UWB antenna with single element results exhibits −10 dB bandwidth from 3.197 to 12.543 GHz with resonances at 3.8, 7.1, 9.25 GHz with the level of return loss below −20 dB. In the SFAA designs the current fed through the port is driven to the first patch and later to the subsequent elements. The reflection loss arises in this case contributes some notch band at 3.8–4.3 GHz and changed the S_{11} performance when compared to the single element patch. Also, some deeper resonances around 3.6, 4.54, and 8.3 GHz can be seen here. While extending the number of patch elements to one more, the UWB response is maintained with starting frequency 3.47 GHz and ends at 11.08 GHz and good return loss can be seen near 7.8 GHz. The CPW configuration of three-element SFAA gets good resonances in its operating band between 3 and 5 GHz. Though there are changes in the operating bands and occurrence of resonances, the S_{11} of antennas with both substrates are in good agreement.

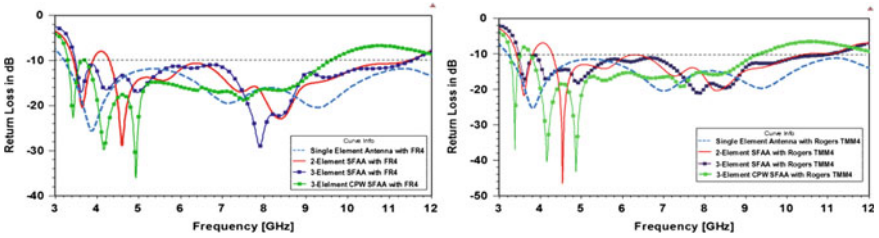


Fig. 2 Simulated return loss characteristics of array antenna iterations with FR4 substrate (figure on the *left*) and with Rogers TMM4 substrate (figure on the *right*)

3.2 Voltage Standing Wave Ratio (VSWR)

The VSWR equals to unity represents good impedance matching criteria at that frequency where the standing waves are minimized so far. The single element, two-and three-element array variations are designed with an objective of obtaining VSWR < 2.0 within the operating band. This can be clearly seen in Fig. 3 with both substrates. For the single element antenna, the minimum VSWR is seen at 3.8 GHz as 1.11. For the two-element SFAA a minimum value of 1.07 is obtained at 4.6 GHz. The operating band which is computed based on VSWR < 2.0 criteria is covering most of the UWB spectrum and a small notch band with center frequency 4.09 GHz is seen for two-element SFAA. Further the upper limit of UWB is diminished when implementing the three-element SFAA with CPW feed.

3.3 Peak Gain Versus Frequency Characteristics

The radiation parameters with respect to frequency are computed and plotted in terms of peak gain for the all antenna variants experimented with FR4 and Rogers TMM4 substrates which can be shown in Fig. 4. For the single element antenna, the peak gain is less in the lower half-UWB and it is increasing after 6.7 GHz then maintains a consistent gain around 5.5 dB. The single element UWB antenna is

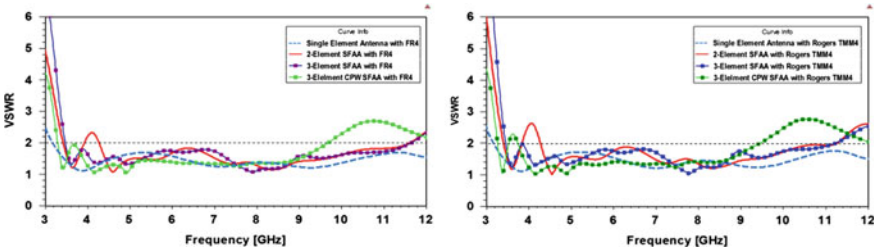


Fig. 3 Simulated VSWR characteristics of array antenna iterations with FR4 substrate (figure on the *left*) and with Rogers TMM4 substrate (figure on the *right*)

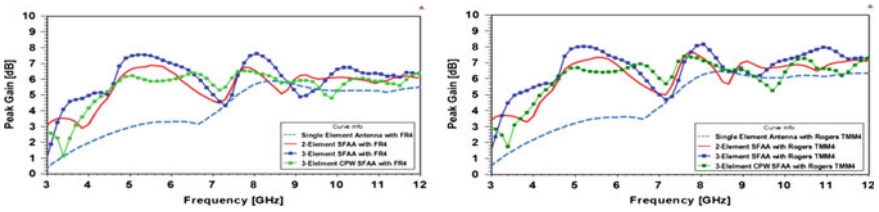


Fig. 4 Simulated peak gain of array antenna variants with FR4 substrate (figure on the *left*) and with Rogers TMM4 substrate (figure on the *right*) plotted w.r.t frequency

having the maximum gain of 6.44 dB (TMM4) and 5.88 dB (FR4) obtained at 8.45 GHz. By the array implementation, the rapid improvement in gain in the lower UWB portion can be achieved. The decrement in peak gain of the antenna observed in the Fig. 4 is in good resemblance with the reflection loss at respective bands. The two-element SFAA is obtaining the maximum of 7.71 dB (TMM4) 6.88 dB (FR4) at 7.75 GHz and 5.5 GHz, respectively. Whereas the three element SFAA is obtaining the maximum peak gain of 8.15 dB (TMM4) 7.62 dB at 8.05 GHz, respectively. From Fig. 4 it can be seen that the three-element SFAA with CPW feed line is having the peak gain of the far-field characteristics are somewhat lesser than that of SFAA with microstrip line feed and noted as maintaining an average value of 6.13 dB (TMM4) and 4.72 dB (FR4) and a maximum gain is noted as 7.41 dB (TMM4 (at 7.6 GHz) and 6.52 dB (FR4 (at 7.75 GHz). The analysis of the peak gain plots for two substrates infers that the loss tangent impacts the UWB SFAA gain due to the inherent dissipation of EM energy and surface wave effects within the dielectric substrate.

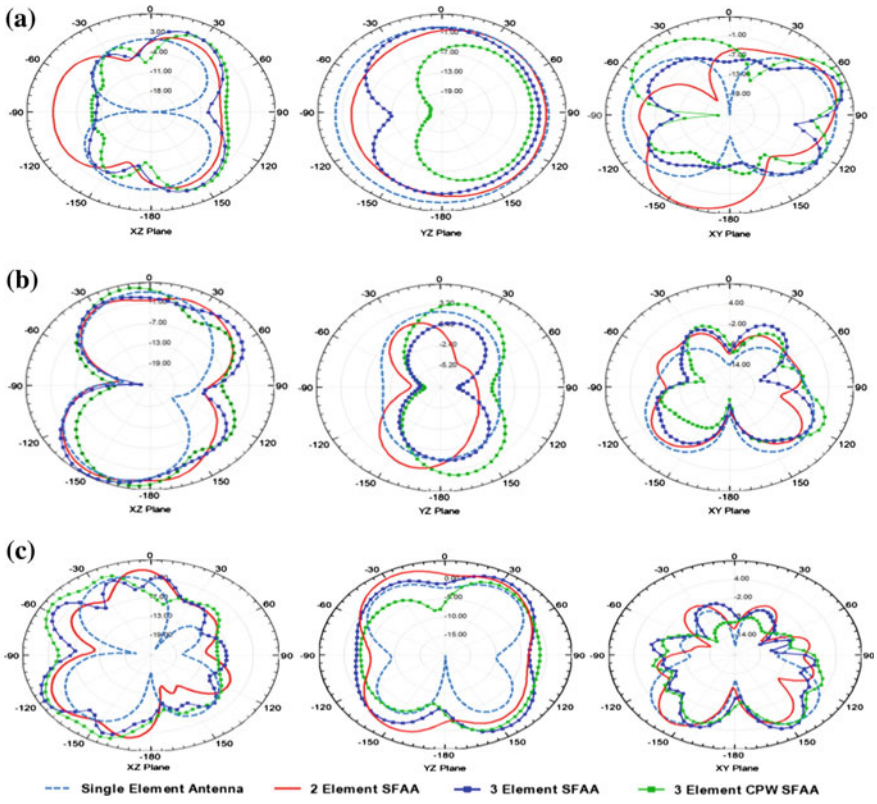


Fig. 5 Simulated radiation patterns of array antenna iterations plotted at **a** 4.45 GHz, **b** 6.7 GHz and **c** 8.5 GHz in XZ-plane (*left*), YZ-plane (*center*), XY-plane (*right*)

3.4 Radiation Patterns of the Proposed Antenna

The far-radiation patterns are computed for all antenna variants. The polar plots are shown in Fig. 5 correspond to the patterns computed at three frequencies 4.45, 6.7, and 8.5 GHz and plotted in three principle planes. The radiation pattern is directional with lesser beam width can be seen at lower UWB frequency, i.e., at 4.45 GHz which is seen from YZ-plane of the antennas in Fig. 5a. The single antenna is showing omnidirectional radiation whereas the increasing the number of elements increases the antenna gain and the radiation pattern is seen in bean-shaped. The small strip extended from the ground plane along the length of the substrate is limiting the field beyond the strip and projects more toward the other edge of the antenna and the radiating beam is having 32° beam width. This can be clearly seen from Fig. 6 in which the single element antenna is having no extended ground strip whereas remaining all models containing the extended strip.

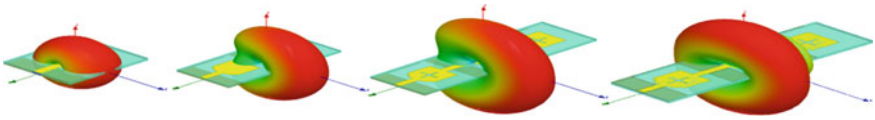


Fig. 6 Simulated three-dimensional far-field radiation of antenna iterations (single, two-, three-element SFAA and CPW SFAA (from *left* to *right*)) obtained at 4.9 GHz

Table 2 Consolidated antenna parameters of SFAA iterations

Antenna model / Parameter	Single element antenna	Two-element SFAA	Three-element SFAA	Three-element CPW SFAA
(a) With relative permittivity ϵ_r = 4.4 and loss tangent *tan* δ = 0.02				
Dimensions (mm^3)	35 × 30 × 1.6	65 × 30 × 1.6	95 × 30 × 1.6	95 × 30 × 1.6
−10 dB return loss bandwidth (GHz)	3.207–12.3	3.434–11.487	3.479–11.535	3.270–9.338
VSWR < 2 bandwidth (GHz)	3.175–12.847	3.421–11.612	3.469–11.641	3.292–9.673
Maximum gain (dB)	5.88	6.88	7.62	6.52
Average gain (dB)	2.75	4.67	4.84	4.72
(b) With relative permittivity ϵ_r = 4.5 and loss tangent *tan* δ = 0.002				
Dimensions (mm^3)	35 × 30 × 1.6	65 × 30 × 1.6	95 × 30 × 1.6	95 × 30 × 1.6
−10 dB return loss bandwidth (GHz)	3.197–12.543	3.415–10.525	3.475–11.081	3.270–9.338
VSWR < 2 bandwidth (GHz)	3.167–12.587	3.403–11.248	3.454–11.214	3.263–9.449
Maximum gain (dB)	6.44	7.71	8.15	7.41
Average gain (dB)	4.60	6.21	6.69	6.13

As the operating frequency increases the radiation far-field emanating into space in multidirections with narrow beam widths. From the polar plot obtained in XY-plane it can be known that the beam toward the patch radiating edges are divided in two with an angle of separation 30° each and some back lobes are seen at the feed line portion of the antenna. The proposed antenna exhibits the different radiation patterns. In YZ-plane, the bean-shaped pattern are slowly converted into dumbbell-shaped at mid UWB. The patterns in XZ-plane clearly depicts the dumbbell-shaped radiations are slowly steered by some angle which and the radiation is toward the radiating edges of the patch of the SFAA.

The performance parameters of all the antenna variants are summarized and tabulated in the Table 2 for comparison.

4 Conclusions

The proposed SFAA configurations are operating in ultra-wideband spectrum. The SFAA designs are successfully achieved the gain improvement and directive radiation characteristics when compared to the UWB single element antenna. The experimentations are carried with two substrates with nearly closer dielectric permittivity but differ in dielectric loss tangents to study the operating and radiation characteristics of the SFAA configurations. The Rogers TMM4 exhibits the good radiation performance when compared to FR4 but for the cost effectiveness FR4 can be used. Further, the directional radiation patterns obtained across 4–5 GHz region can be applicable for target tracking as the half-power beam width is narrow about 30°. The beam width can be further minimized in future research in order to detect the targets and can be used as UWB sensing device. Several adaptive techniques can be implemented further for using this antenna as a beam scanning array.

Acknowledgements Authors would like to express their sincere gratitude to the Research Centre of Dept. of ECE and management of Sir C. R. Reddy College of Engineering, Eluru for providing the licensed 3D EM simulation software ANSYS HFSS 15.0 and their esteemed guidance and support to the work.

References

1. Garg, R *et al.*: Microstrip Antenna Design Handbook. pp. 773, Artech House (2001).
2. Balanis C.A.: Antenna Theory Analysis and Design. pp. 283, John Wiley & Sons, Inc., (2008).
3. Pancera, E., Wiesbeck, W.: Eight – Elements UWB Coplanar Monopole Array for Radar Applications. In: 2nd European Conference on Antennas & Propagation, pp. 1–4. Edinburgh (2007).
4. Yang, Y., Wang, Y., Fathy, A. E.: Design of Compact Vivaldi Antenna Arrays for UWB See Through Wall Applications. In: Prog. In Electromagn. Res. (PIER). 82. 401–418. (2008).

5. Ito, Y., Ameya, M., Yamamoto, M., Nojima, T.: Unidirectional UWB array antenna using leaf-shaped bowtie elements and flat reflector. In: Electron. Lett. 44(1). 9–11. (2008).
6. Wu, Q., Jin, R., Geng, J.: A Single-Layer Ultrawideband Microstrip Antenna. In: IEEE Trans. Ant. and Propag. 58(1). 211–214. (2010).
7. Gibbins, D., Klemm, M., Craddock, I. J., Leendertz, J. A., Preece, A., Benjamin, R.: A Comparison of a Wide Slot and a Stacked Patch Antenna for the Purpose of Breast Cancer Detection. In: IEEE Trans. Ant. and Propag. 58(3). 665–674. (2010).
8. Venkateswara Rao, T., Sudhakar, A., Padma Raju, K.: Design of CPW Feed Triangular Slot Antenna Array for WiMAX and WLAN Applications. In: Int. Conf. on Recent Trends in Engg. and Material Sciences (ICEMS). Jaipur, India (2016).
9. Mullick, T. U., Md. Ershad, E., Matin, M. A., Rahman, A.: Design of UWB Antenna with a Band-Notch at 5 GHz. In: Loughborough Antennas & Propagation Conference, pp. 1–4. Loughborough, UK (2012).
10. Venkateswara Rao, T., Sudhakar, A., Padma Raju, K.: Band Stop Filter Loaded Triangular Slot UWB Notch Antenna. In: Int. Journal. of Applied Engineering Research. 11(6). 4318–4324 (2016).

On the Convergence of Synthesis of Desired Nulls from Circular Arrays Using Flower Pollination Algorithm

V.V.S.S. Sameer Chakravarthy, Sudheer Kumar Terlapu, P.S.R. Chowdary, T. Venkateswara Rao and Suresh Chandra Satapathy

Abstract In this paper, Synthesis of sum patterns from circular arrays to generate desired nulls with reduced sidelobes using flower pollination algorithm is presented. The array design is first formulated as an optimization problem with the goal of reducing peak sidelobe level with a deep null. The objective of the FPA algorithm is to determine the optimized set of amplitude excitation coefficients to obtain the desired pattern. The patterns are numerically computed for different constraints and the results obtained are compared with those of genetic algorithm in the present paper.

Keywords Circular array · Flower Pollination Algorithm · Side lobe level · Fitness function and radiation pattern

V.V.S.S.S. Chakravarthy (✉) · P.S.R. Chowdary
Department of ECE, Raghu Institute of Technology, Visakhapatnam, Andhra Pradesh, India
e-mail: sameersree@gmail.com

P.S.R. Chowdary
e-mail: satishchowdhary@ieee.org

S.K. Terlapu
Department of ECE, Shri Vishnu Engineering College for Women (Autonomous), Bhimavaram, India
e-mail: skterlapu@gmail.com

T. Venkateswara Rao
Department of ECE, Sir C. R. Reddy College of Engineering, Eluru, India
e-mail: tumati01@gmail.com

S.C. Satapathy
Deparment of Computer Science & Engineering, PVP Siddhartha Institute of Technology, Vijayawada, Andhra Pradesh, India
e-mail: sureshsatapathy@ieee.org

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_50

1 Introduction

The applications of the circular aerial arrays and their limitations in communications and direction finding radar is given by [1, 2]. Bayliss [3] proposed a two parameter difference pattern for circular aperture antennas which have equal sidelobes similar to those of Taylor's sum pattern. D. K. Cheng et al. [4] considered the adjustment of relative phase of each element in a uniform linear and circular array synthesis to achieve specified directivity, with the objective being its maximization. R. C. Rudduck et al. [5] has carried out a thorough investigation of the directive gain characteristics with circular Taylor pattern synthesis of planar arrays [6]. The optimum directive gain of the circular Taylor pattern with a given sidelobe level was obtained by appropriate design. Curves of directivity versus inter-element spacing and scan angle for uniformly excited planar arrays composed of discrete identical elements at regular spacing are presented in [7]. N. Goto et al. [8] considered uniformly excited circular array with symmetric pattern for the objective of sidelobe suppression. In [9], R. S. Elliot considered planar circular array for pattern synthesis. Symmetric continuous distribution was assumed which required producing a flat-topped beam with controlled ripple, surrounded by ring sidelobes of controlled height. With M filled in nulls in the shaped region, there are 2M solutions for the aperture distribution. Keen-Keong Yan et al. [10] suggested employing real-coded GA in order to optimize the linear arrays with reduced sidelobe levels. A compilation of variants of GA with its application to linear and circular array synthesis with the objectives of array thinning, null steering in symmetric and asymmetric pattern is given in [11]. The application of GA to wire and planar antenna design and analysis is cited. Panduro et al. [12] considered reducing the SLL with the minimized optimum aperture size as constraint.

However, synthesis of radiation patterns with desired nulls using flower pollination algorithm (FPA) has not been reported so far. Therefore, in this paper an attempt is made to use FPA for the synthesis of the amplitude excitation coefficients to yield a desired nulls from circular array with reduced sidelobes.

The paper is organized as follows. In Sect. 2, formulation of the circular array is discussed. Section 3 deals with concept of FPA. In Sect. 4, formulation of fitness function is explained. The synthesized radiation patterns with desired nulls and reduced sidelobes are presented in Sect. 5. Finally, conclusions are drawn in Sect. 6.

2 Formulation

The geometry of the circular array oriented along the XY plane is as shown in the Fig. 1. The corresponding array factor is given as

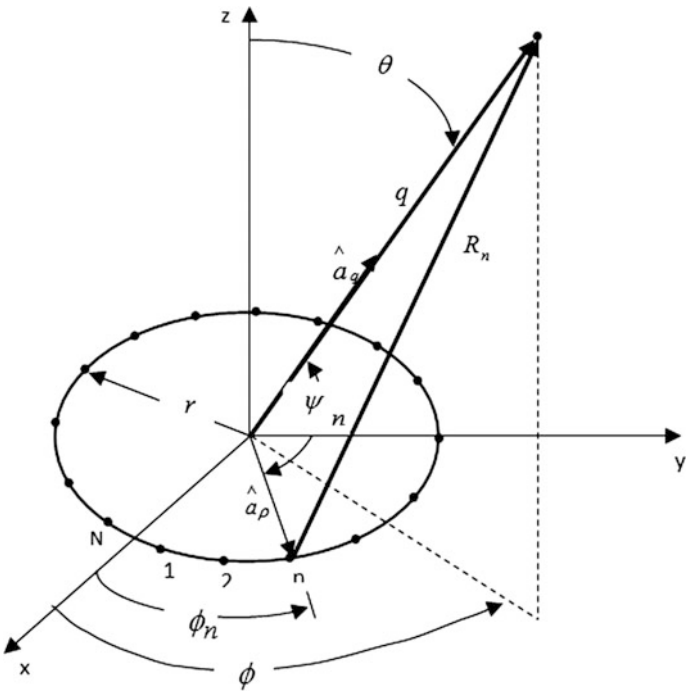


Fig. 1 Geometry of circular array

$$\mathrm{AF}(\phi) = \sum_{n=1}^{N} \mathrm{I_n exp(j(kr\ cos(\phi - \phi_n) + \beta_n))} \tag{1}$$

where,

n is element number
I_n is *n*th element excitation current amplitude
N is number of elements in the array
β_n is the phase of excitation of the *n*th element

$$kr = \frac{2\pi r}{\lambda} = \sum_{i=1}^{N} d_i \tag{2}$$

$$\phi_n = \frac{2\pi}{kr} \sum_{i=1}^{n} d_i \tag{3}$$

The radiation pattern of the array is described as the product of element factor and the corresponding array factor. As the elements in the array are isotropic in nature the element factor is considered as '1.' Hence, the array factor completely describes the radiation pattern of the array.

3 Flower Pollination Algorithm

FPA was proposed by Xin She Yang et al. [13]. The FPA is inspired by the natural phenomenon of pollination which leads to off-spring in flowering plants. The pollination process takes in two different forms as self pollination and cross pollination. The self pollination which corresponds to successful pollination due to pollen grain from the flowers of the same plant is similar to local search. Similarly, cross pollination refers to global search in which the source of pollen is from flowers of plants which are far away and are driven often by wind or breeze.

The solution vector is given by x_i. For updating x_i the following mathematical representation of flower constancy is used [14–18]

$$x_i^{k+1} = x_i^k + L(x_i^k - g*) \tag{4}$$

where 'L' is typically referred as step size that determines the pollination strength and is always positive and nonzero. Step size 'L' is characterized as '*Levy Flights,*' [13, 14, 18] rather than a simple random number in order to mimic the movement of the biotic pollinators that are capable of sweeping long distances.

4 Objectives and Fitness Function

Briefly the objectives of study dealt in this work are classified as follows

a. Positioning nulls in the desired direction without any constraint consideration
b. Positioning nulls in the desired direction with the constraint of desired SLL
c. Positioning nulls with no constraint and with constraint conditions for non scanned beam and beam scanned patterns

The formulation of the fitness function for objectives like single or multiple narrow nulls and desired SLL is given as

$$\begin{aligned} f1 &= \max(\text{null\_depth} + \text{AF}(\theta = \theta_{null(\text{n})})) && \text{if AF}(\theta = \theta_{null(\text{n})}) > -50 \\ &= 0 && \text{otherwise} \end{aligned} \tag{4}$$

$$f2 = SLL_{desired} + \max(SLL_{\theta = -\pi/2 \, to \, \pi/2}) \tag{5}$$

where,

$\text{SLL}_{\text{desired}}$ and null_depth are positive values of the corresponding array factor.

$SLL_{\theta = -\pi/2 \, to \, \pi/2}$ is the side lobe level values between −90° and 90°.

The fitness $f1$ is responsible for observing desired null depth at desired null positions. Whereas, the function $f2$ is responsible for suppressing the SLL.

Table 1 Description of the problem into case-wise objectives

Position of the main beam	Case no.	Null position	Constraint
0°	1	−45, 30	No constraint
	2	−45, 15, 30	
	3	−45, 30	−15 dB SLL
	4	−45, 15, 30	
25°	5	−5, 55	No constraint
	6	−5, −30, 55	
	7	−5, 55	−15 dB SLL
	8	−5, −30, 55	

Basing on the above objectives of study the description problem is as given in Table 1.

For objectives mentioned in unconstrained cases the final fitness is calculated as $F = f1$.

For objectives given in constrained cases the final fitness is calculated as $F = f1 + f2$.

5 Results

The optimized radiation pattern plots with the position of nulls in the desired directions as mentioned in cases 1–8 are presented in Figs. 2, 3, 4, 5, 6, 7, 8 and 9. The convergence graphs are presented for case dealt. In both the radiation pattern and convergence plots the dotted line refers to GA and the solid line refers to FPA. The case-wise objectives are as given in Table 1. Accordingly, the results pertaining to each case are presented in this section. For each case, radiation pattern with the null positions and constraints if any is given along with respective convergence plot. The convergence plots are later used to study the effect of the constraints on the convergence characteristics of the array synthesis problem in terms of computational time and number of iterations consumed to converge.

The nulls as mentioned in Case 1 are obtained which is clearly evident from the corresponding radiation pattern plot as shown in Fig. 2a. It can be inferred from the corresponding convergence plot that the GA consumed around 2500 iterations while the FPA took less than 200 iterations to converge. Similarly the Case 2 radiation pattern is as shown in Fig. 3a in which three null positions are considered at −45, 15, and 30, respectively. The corresponding convergence plot is as shown in Fig. 3b. The convergence plot once again states that there is a possibility of fast convergence with FPA when compared with GA.

A constraint of SLL with −15 dB is included in Case 3 and Case 4 along with the null positions mentioned in Case 1 and Case 2 respectively. The corresponding radiation patterns are given as Figs. 4a and 5a and the convergence plots are mentioned in Figs. 4b and 5b. It is possible to claim that the FPA and GA could

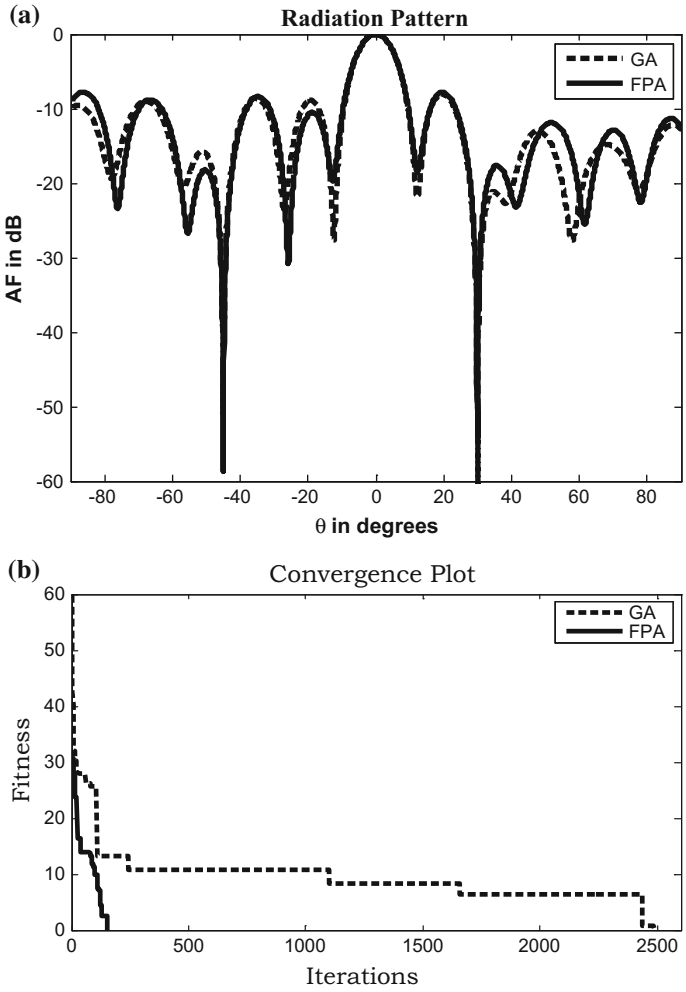


Fig. 2 **a** Radiation pattern with nulls as given in case 1. **b** Convergence plot for case 1 using GA and FPA

efficiently produce the desired radiation patterns while the FPA is quick when compared with GA in terms of convergence plots.

The description of the objectives in Case 5 through Case 8 is similar to Case 1 through Case 4 except that the main beam is scanned to 25°. This is a possible demonstration of efficiency of the circular array synthesis technique under scanned beam conditions. Radiation patterns and the respective convergence plots for Case 5 and Case 6 with no constraint on SLL are given in Fig. 6 and Fig. 7, respectively. Similarly plots corresponding to Case 7 and Case 8 are given in Fig. 8 and Fig. 9, respectively.

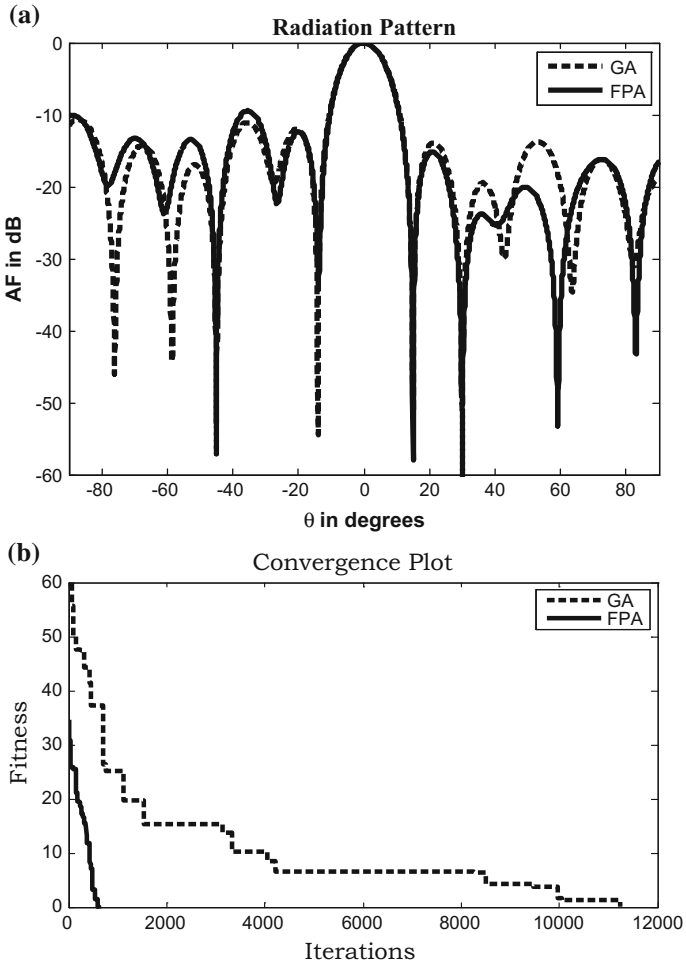


Fig. 3 **a** Radiation pattern with nulls as given in case 2. **b** Convergence plot for case 2 using GA and FPA

Case-wise null positions, number of generations consumed as read from convergence plots under constraint and no constraint scenarios are tabulated in Table 2. It can be inferred from the tabulated data as given in Table 2 that the number of iterations consumed either by GA or FPA has increased when constraint is introduced. Also the number of iteration observed for convergence by GA is larger than the FPA in both the cases of with and without constraints.

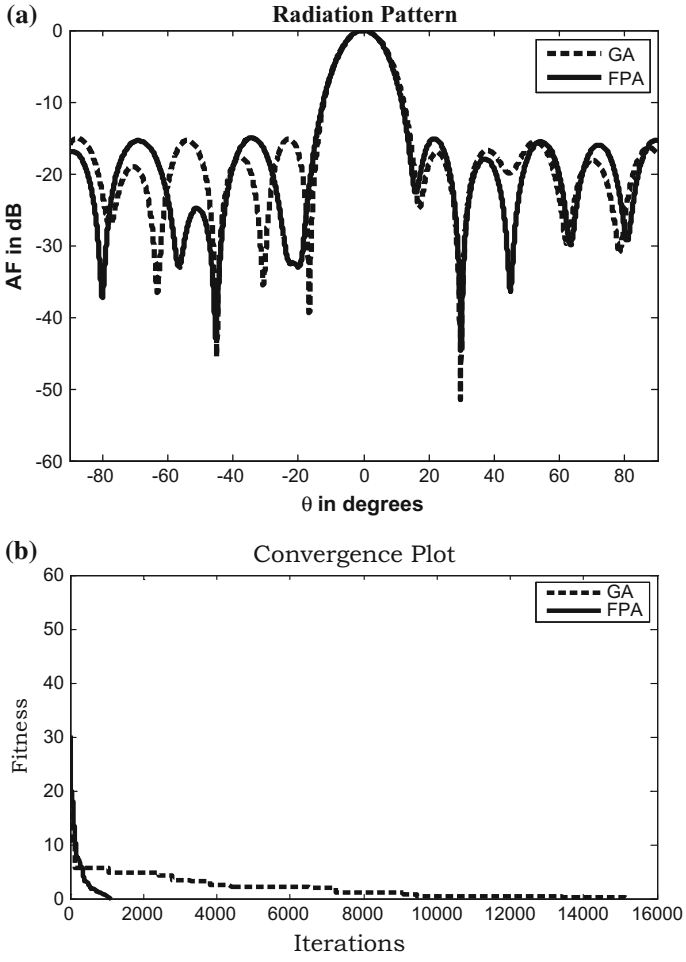


Fig. 4 **a** Radiation pattern with nulls as given in case 3. **b** Convergence plot for case 3 using GA and FPA

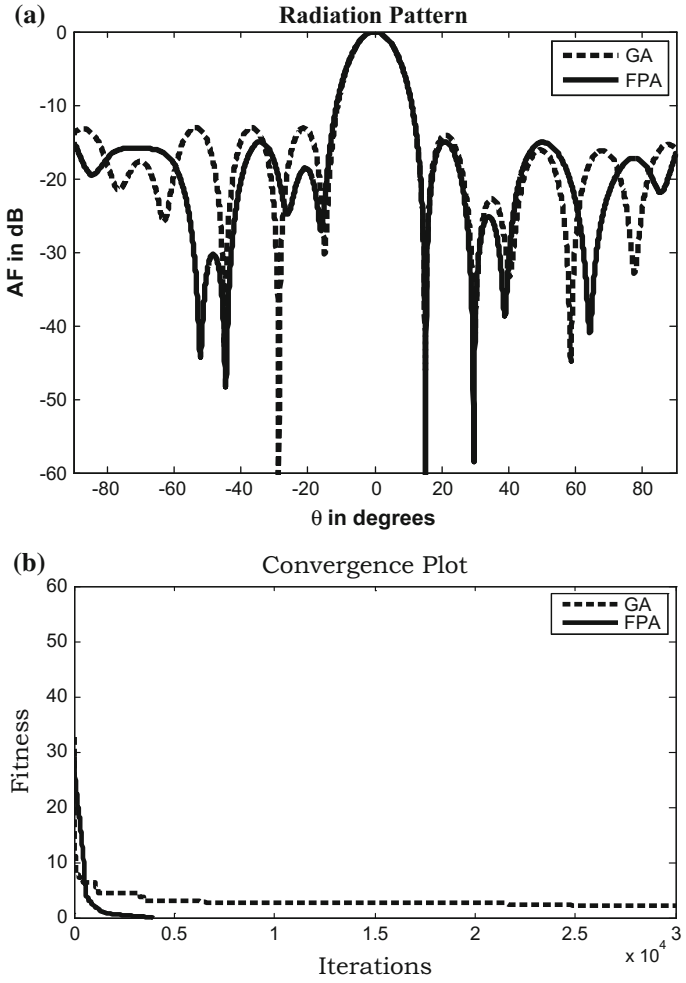


Fig. 5 **a** Radiation pattern with nulls as given in case 4. **b** Convergence plot for case 4 using GA and FPA

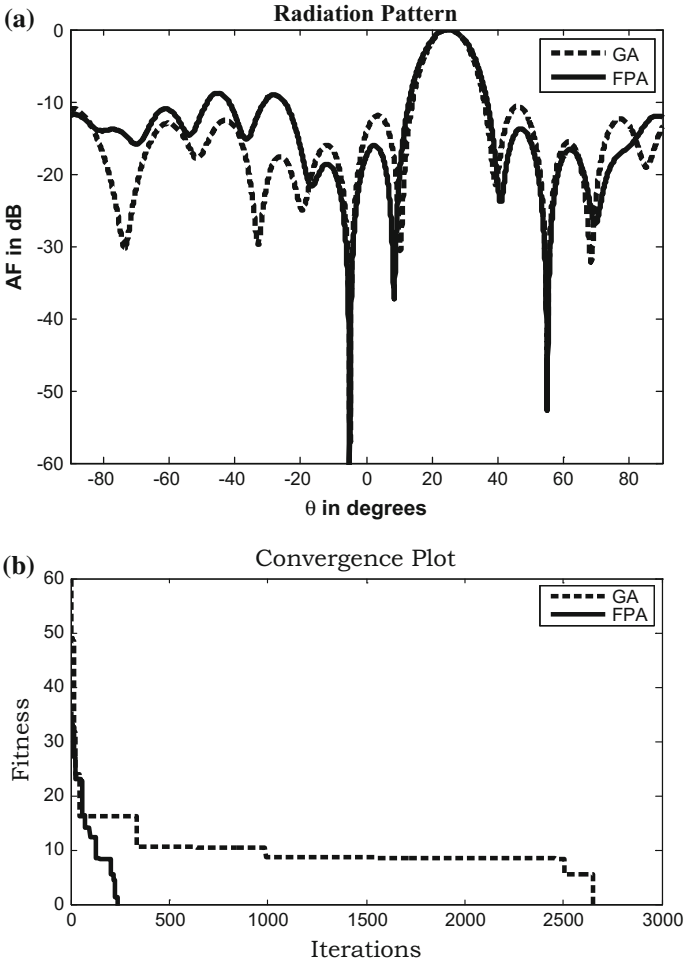


Fig. 6 **a** Radiation pattern with nulls as given in case 5. **b** Convergence plot for case 5 using GA and FPA

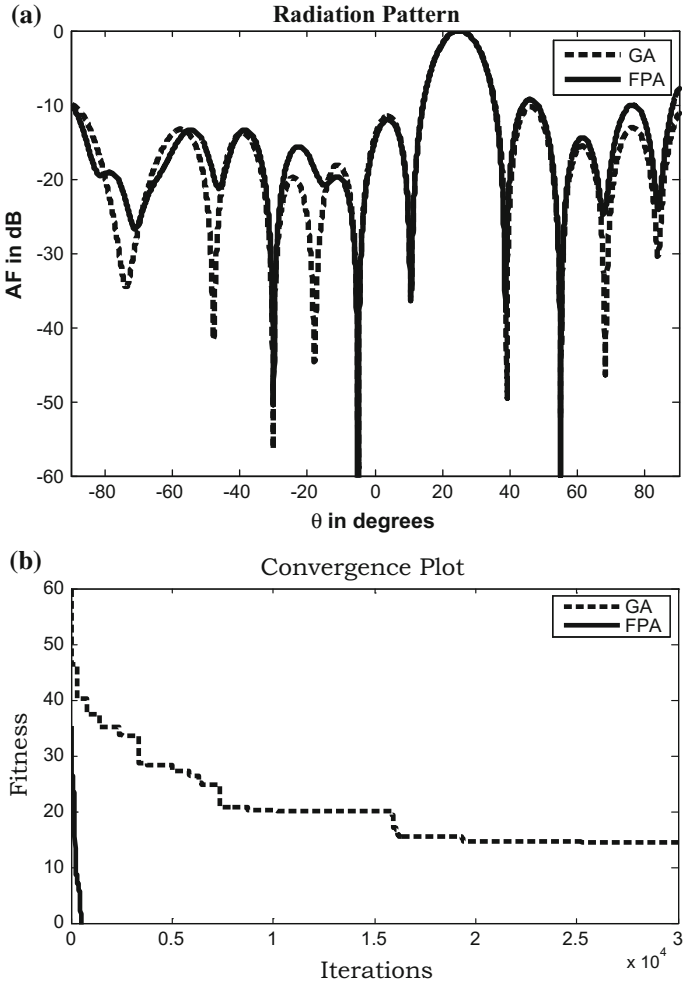


Fig. 7 **a** Radiation pattern with nulls as given in case 6. **b** Convergence plot for case 6 using GA and FPA

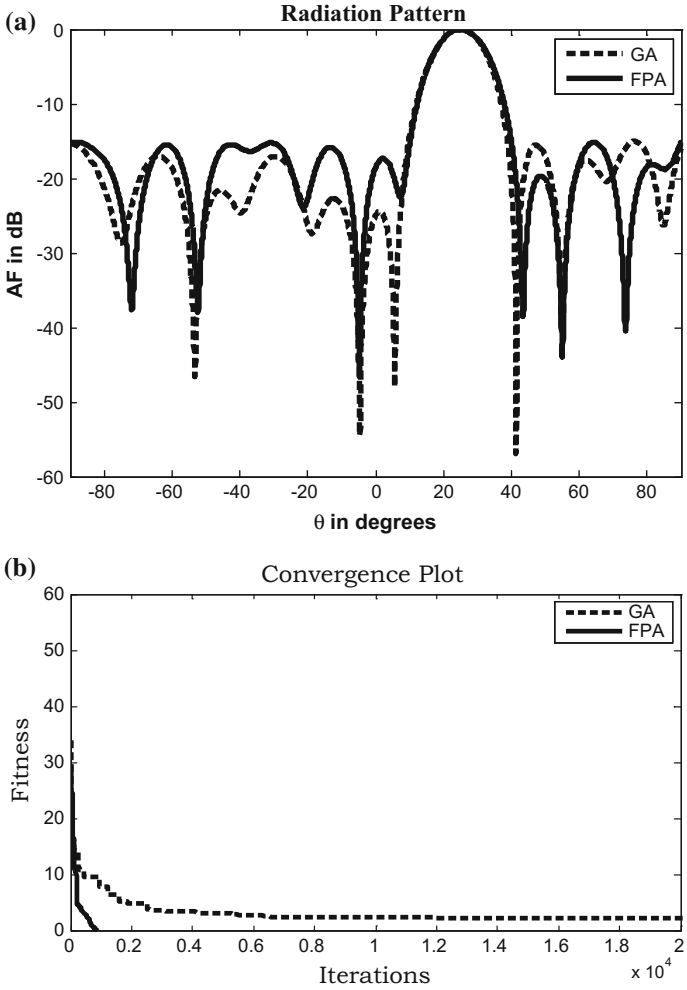


Fig. 8 **a** Radiation pattern with nulls as given in case 7. **b** Convergence plot for case 7 using GA and FPA

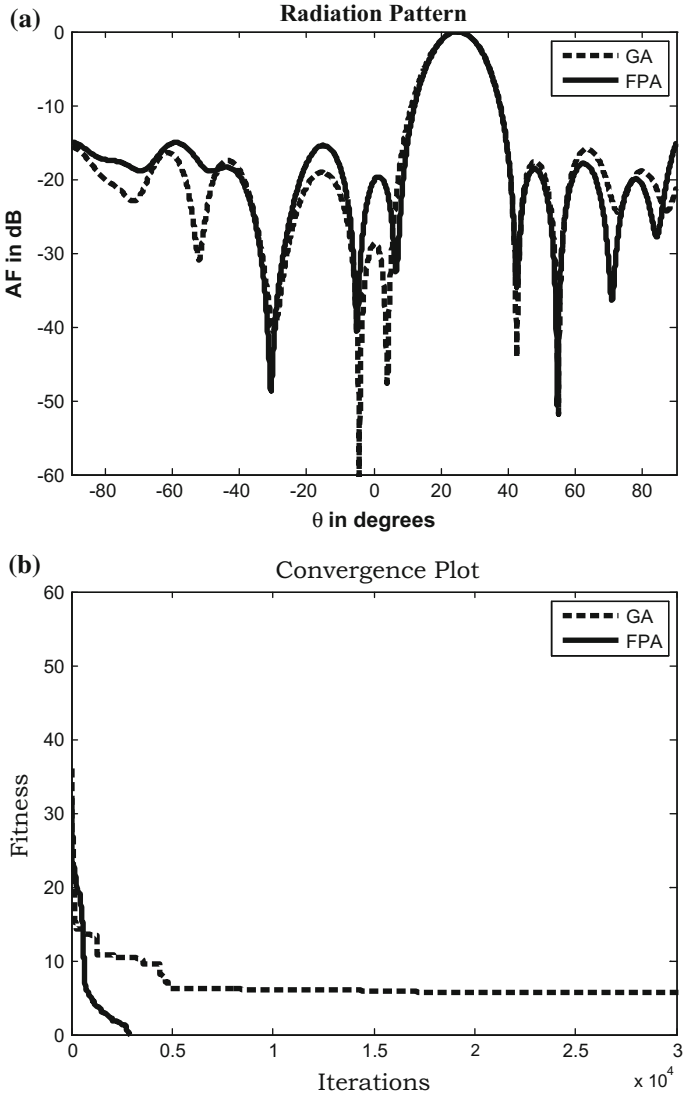


Fig. 9 **a** Radiation pattern with nulls as given in case 8. **b** Convergence plot for case 8 using GA and FPA

Table 2 Comparison of convergence characteristics based on the constraint applied

Null position	Number of generations	Constraint
−45, 30	2500	No constraint
	15,000	With constraint
−45, 15, 30	11,000	No constraint
	100k	With constraint
−5, 55	2600	No constraint
	7000	With constraint
−5, −30, 55	46,000	No constraint
	>100k	With constraint

6 Conclusion

Both GA and FPA are implemented on circular array synthesis problem of positioning nulls. FPA has shown considerable domination over GA in terms of evaluation time and number of generations to converge. The impact of the number of constraints to the problem on the convergence characteristics of the algorithm is studied with respect to the number of iterations. It is possible to conclude that the inclusion of constraint like beam steering and suppressed SLL to −15 dB have increased the computational time but not the quality of solution.

References

1. Davies, D. E N.: A transformation between the phasing techniques required for linear and circular aerial arrays. Electrical Engineers, Proceedings of the Institution of, vol. 112, no. 11, pp. 2041–2045, DOI:10.1049/piee.1965.0340. (November 1965)
2. Mott, H., Dudgeon, J.E.: On circular array pattern synthesis using a digital computer, Proceedings of the IEEE, vol. 56, no. 3, pp. 369–370, DOI:10.1109/PROC.1968.6318. (March 1968)
3. Bayliss. E. T.: Design of monopulse antenna difference patterns with low sidelobes. The Bell System Technical Journal, Vol. 47, pp. 623–650, (May–June 1968)
4. Cheng. D.K., Raymond. P.D.: Optimisation of array directivity by phase adjustments. Electronic Letters, vol. 7, No. 18, pp. 552–554, (September 1971)
5. Rudduck. R. C., et. Al.: Directive gain of circular Taylor Patterns. Radio Sci., Vol. 6, pp. 1117–1121, (December 1971)
6. Taylor, T.T.: Design of circular apertures for narrow beamwidth and low sidelobes. Antennas and Propagation, IRE Transactions on, vol. 8, no. 1, pp. 17–22, DOI:10.1109/TAP.1960.1144807. (January 1960)
7. Forman, B.: Directivity characteristics of scannable planar arrays. Antennas and Propagation, IEEE Transactions on, vol. 20, no. 3, pp. 245–252, DOI:10.1109/TAP.1972.1140209. (May 1972)
8. Goto, N., Tsunoda, Y.: Sidelobe reduction of circular arrays with a constant excitation amplitude. Antennas and Propagation, IEEE Transactions on, vol. 25, no. 6, pp. 896–898, DOI:10.1109/TAP.1977.1141700. (Nov 1977)

9. Elliott, R.S., Stern, G.J.: Shaped patterns from a continuous planar aperture distribution. Microwaves, Antennas and Propagation, IEE Proceedings H, vol. l35, no. 6, pp. 366–370, (Dec 1988)
10. Keen-Keong Yan; Lu, Y.: Sidelobe reduction in array-pattern synthesis using genetic algorithm. Antennas and Propagation, IEEE Transactions on, vol. 45, no. 7, pp. 1117–1122, DOI:10.1109/8.596902. (Jul 1997)
11. Y. Rahmat-Samii and E. Michielssen, Electromagnetic Optimization by Genetic Algorithms, chapter 5. Wiley, (1999)
12. Marco A Panduro.: Design of non – uniform circular antenna arrays for side lobe reduction using the method of genetic algorithms. International Journal of Electronics and communications, Vol. 60, No. 10, pp. 713 – 717, (November 2006)
13. Yang. X.-S., Karamanoglu. M., He. X.: Flower pollination algorithm: a novel approach for multiobjective optimization. Engineering Optimization, vol. 46, no. 9, pp. 1222–1237, (2014)
14. Yang. X.-S. Deb. S.: Cuckoo search via Lévy flights. in Proceedings of the World Congress on Nature & Biologically Inspired Computing (NaBIC '09), pp. 210–214, Coimbatore, India, (December 2009)
15. Łukasik. S., Kowalski. P. A.: Study of flower pollination algorithm for continuous optimization. Advances in Intelligent Systems and Computing, vol. 322, pp. 451–459, (2015)
16. Chakravarthy. V. V. S. S. S., Rao. P. M.: On the convergence characteristics of flower pollination algorithm for circular array synthesis. in Proceedings of the 2nd International Conference on Electronics and Communication Systems (ICECS '15), pp. 485–489, IEEE, (February 2015)
17. Chakravarthy. V. V. S. S. S., Naveen Babu. K., Suresh. S., Chaya Devi. P., Mallikarjuna Rao. P.: Linear array optimization using teaching learning based optimization. Advances in Intelligent Systems and Computing, vol. 338, pp. 183–187 (2015).
18. Chakravarthy Vedula. V. S. S. S., Chowdary Paladuga. S. R., Rao Prithvi. M.: Synthesis of Circular Array Antenna for Sidelobe Level and Aperture Size Control Using Flower Pollination Algorithm. International Journal of Antennas and Propagation, vol. 2015, Article ID 819712, 9 pages (2015).

Design and Study of Frequency Reconfigurable Antenna for Wireless Applications

Venkateswara Rao Tumati and Jaya Cheruku

Abstract In this paper, the design of a frequency reconfigurable antenna for Wi-Fi, Wi-MAX, and C-band applications is presented. Dual and triple frequency reconfigurable antennas are designed and their parameters were plotted. A rectangular patch (18 mm × 14.5 mm) with microstrip line feed is taken as radiating element. FR4 dielectric substrate with $\epsilon_r = 4.4$ and thickness 1.6 mm is taken. Two RF-pin diodes are used to achieve frequency reconfiguration. Antenna is designed and simulated using HFSS v.15 software.

Keywords Microstrip patch antenna · Microstrip line feed · VSWR · Return loss · Reconfiguration · HFSS

1 Introduction

Microstrip antennas have gained much popularity in recent years, and continuously finding applications in microwave field. Patch antennas are one type of microstrip antennas which are small, low profile antennas consisting radiating patch on one side of dielectric substrate and ground plane on other side of dielectric substrate [1]. They can be designed in various shapes in which rectangle and circle are most common [2, 3]. In order to excite the antenna several types of feeding techniques exist. Most common are microstrip line feeding, co-axial feeding, proximity coupled feeding, and aperture coupled feeding [4, 5]. Microstrip line feeding is widely used because of its ease of fabrication.

With rapid growth in communication, the demand for antennas which can be used at different frequencies has increased. And in recent years, reconfigurable

V.R. Tumati (✉) · J. Cheruku
Department of Electronics and Communications Engineering,
Sir C. R. Reddy College of Engineering, Eluru, India
e-mail: tumati01@gmail.com

J. Cheruku
e-mail: jaya.chinni25@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_51

antennas have gained more attention. Reconfiguration means capable of modifying the characteristics and these antennas replaces the use of multiple antennas for multiple frequencies. Reconfiguration can be done in either frequency [6–10], or radiation pattern [11, 12] or polarization [13, 14].

In this paper, a triple frequency reconfigurable antenna is designed for Wi-Fi, Wi-MAX, and C-band applications. Patch and ground plane are separated by FR4 epoxy dielectric substrate (40 mm × 30 mm) with dielectric constant 4.4 and thickness 1.6 mm. Two RF-pin diodes BAR6402 are used for switching. The antenna modeling is discussed in Sect. 2. In Sect. 3, the proposed antenna performance is explained with the simulation results in terms of several antenna parameters and concluded in Sect. 4.

2 Geometrical Modeling of Patch Antenna

Patch antenna consists of a radiating patch of specified length L and width W, a dielectric substrate of length Ls and width Ws, Ground plane of dimensions (L_g W_g) and a feed line (L_f × W_f) which is used to excite the antenna. In this paper, a rectangular patch antenna with microstrip line feed is used. By using transmission-line model dimensions of patch, ground, and feed can be calculated. The transmission-line model equations for patch antenna analysis are given in [2]. The optimized values for single frequency antenna are shown in Table 1.

Frequency reconfiguration can be achieved by using switches, variable reactive loading, structural or mechanical changes, material changes. In this paper, RF-PIN diode switches are used to achieve switching mechanism. In order to achieve dual frequency reconfiguration (Fig. 1b), a stair case slot is made at the center of patch and its position is optimized to get the required frequency of operation. BAR6402 PIN diode (D) is used in the slot at the optimized position. PIN diode modeling is shown in Fig. 2, when it is forward biased, will acts as (closed switch) a small resistance (R_s) in series with a small inductance (L) and when reverse biased it acts as (open switch) a large resistance (R_p) in parallel with a small capacitance (C_p) and in series with a small inductance (L) and the values are shown in Table 2.

In order to obtain triple frequency reconfiguration (Fig. 1c), two stair case slots were made which are mirror images of each other and the slot positions are varied to get the required frequencies. Two PIN diodes D1, D2 were placed in two slots at the optimized positions.

Table 1 Dimensions of patch antenna

Component	Length (mm)	Width (mm)
Substrate	L_s = 40	W_s = 30
Patch	L = 18	W = 14.5
Ground plane	Lg = 10	W_g = 30
Feed line	L_f = 13.699	W_f = 3.3

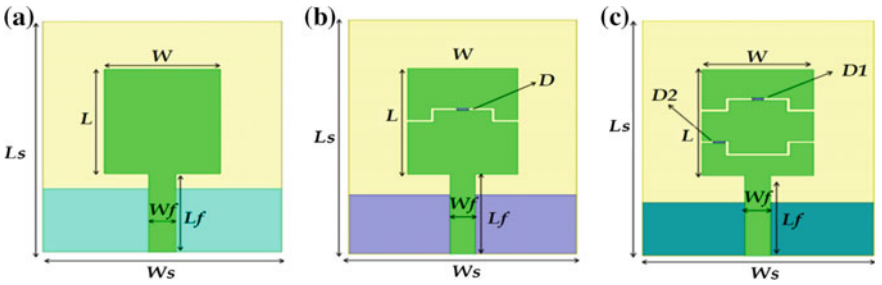


Fig. 1 Geometry of **a** dual band antenna, **b** dual and **c** triple frequency reconfigurable antenna

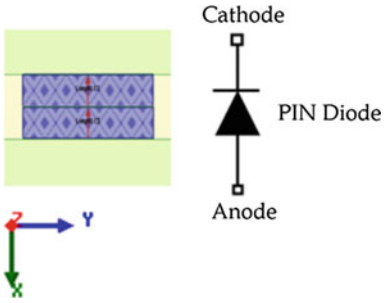


Fig. 2 PIN diode representation with lumped RLC boundary in HFSS

Table 2 BAR6402 PIN diode equivalent circuit parameters

Component	Values
L	0.6 nH
R_s	2.1 Ω
R_p	3000 Ω
C_p	0.17 pF

3 Simulation Results

Antenna is designed and simulated in HFSS (High-Frequency Structural Simulator) V.15 software which is a 3D electromagnetic simulator. The performance of antenna is observed by plotting the return loss, VSWR plots, and by generating radiation patterns in both azimuthal and elevation planes. The surface current distributions were observed to check the functioning of pin diodes.

3.1 Return Loss (S_{11})

Return loss gives the loss of power in signal reflected by any discontinuity in a transmission line. The patch antenna without slots and diodes is first designed

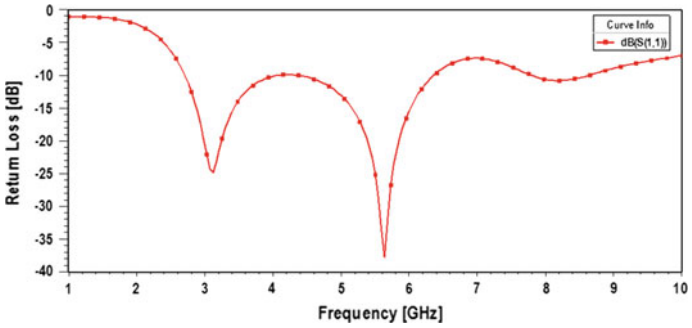


Fig. 3 Simulated return loss characteristics of patch antenna without slots and diodes

(Fig. 1a) and simulated. The return loss is plotted with respect to frequency and shown in Fig. 3. For an efficient antenna, the return loss should be −10 dB. This threshold is set by considering that 90% of signal gets transmitted and only 10% gets reflected. We can adjust the threshold value by assuming maximum amount of signal is transmitted and only a small fraction gets reflected. The antenna resonates at 3.1 and 5.6 GHz with a return loss of −24.8335 dB and −37.8751 dB covering both Wi-MAX and WLAN bands.

A slot is made on patch and pin diode is placed as shown in Fig. 1b. Dual frequency reconfigurable antenna is simulated and return loss versus frequency is plotted for both diodes ON and OFF cases. These two cases were shown in Fig. 4.

Case 1: When diode D is forward biased (ON), then the antenna resonates at 2.5 GHz frequency covering the Wi-Fi band with a return loss, $S_{11} = -29.3547$ dB is obtained.
Case 2: When diode D is reverse biased (OFF), then the antenna resonates at 3.34 GHz and 5.6 GHz frequency covering both Wi-MAX and WLAN bands with S_{11} value of −17.5141 dB and −12.3121 dB, respectively.

Two slots were made on the patch and two diodes were placed as shown in Fig. 1c. This triple frequency reconfigurable antenna is simulated and return loss versus frequency is plotted for three cases and shown in Fig. 4.

Case 1: When diodes D1 and D2 are forward biased (ON), then the antenna resonates at 2.35 GHz frequency covering the Wi-Fi band with a return loss, $S_{11} = -37.4465$ dB.

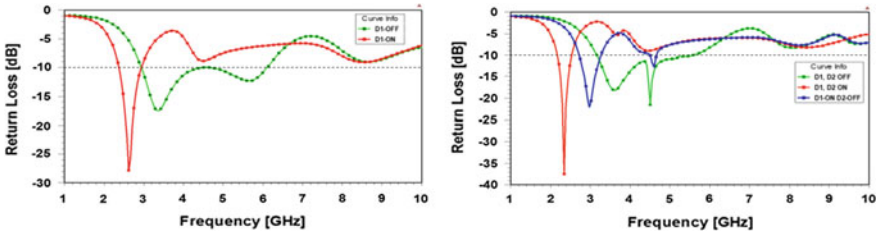


Fig. 4 Simulated return loss characteristics of dual frequency (figure on the *left*) reconfigurable and triple frequency (figure on the *right*) reconfigurable antenna

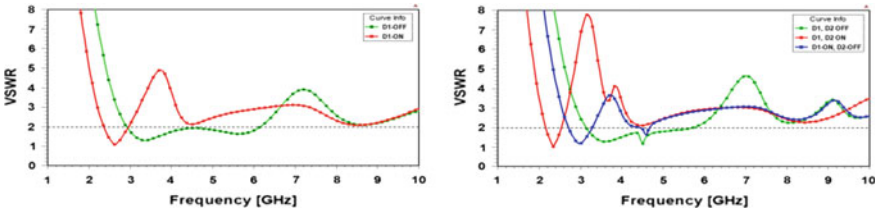


Fig. 5 Simulated VSWR characteristics of dual frequency (figure on the *left*) reconfigurable and triple frequency (figure on the *right*) reconfigurable antenna

Case 2: When diode D1 is forward biased (ON) and D2 is reverse biased (OFF), then the antenna resonates at 3 and 4.6 GHz covering a part of C-band with a return loss, $S_{11} = -23.2694$ dB and -12.3084 dB, respectively.
Case 3: When diode D1 and D2 are reverse biased (OFF), then the antenna covers total 3.16–5.58 GHz band resonating at 3.61–4.51 GHz with a return loss, $S_{11} = -18.228$ dB and -21.5238 dB.

3.2 Voltage Standing Wave Ratio (VSWR)

Voltage standing wave ratio (VSWR) gives the numerical measure of matching. If antenna is perfectly matched to transmission line the there will be no reflections and VSWR equals to 1. But in practical it is impossible to attain unit value. So VSWR < 2 is set as threshold by considering that matching between antenna and transmission line is good enough to avoid any kind of reflections. VSWR versus frequency plots for both dual frequency and triple frequency reconfigurable antenna are shown in Fig. 5.

3.3 Surface Current Distributions on Radiating Patch of the Proposed Antenna

Surface current distributions for triple frequency reconfigurable antenna in three cases are shown in Fig. 6. It can be observed that the conducting mode of the switching diodes which is embedded in the slots establish a current path through it whereas in its non-conducting case these will not establish any current path. The length of the effective current path results the antenna to be resonant at different frequencies.

3.4 Radiation Patterns

Radiation Patterns for dual frequency and triple frequency reconfigurable antenna are shown in Fig. 7a, Fig. 7b, respectively.

3D polar plots for triple frequency reconfigurable antenna in three cases are shown in Fig. 8. It shows that the antenna exhibits nearly omnidirectional pattern and while both diodes are ON the far-field radiation gets oriented in a specific direction (phi = 65°, theta = 105°) with a peak gain of 7.45. The gain values obtained in three cases are given in Table 3.

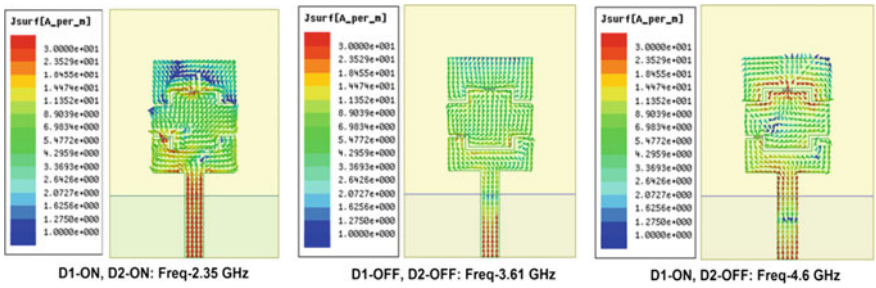


Fig. 6 Simulated current distributions in D1, D2-ON (figure on the *left*), D1-ON, D2-OFF (figure on the *center*) and D1, D2-OFF (figure on the *right*) conditions for triple frequency reconfigurable antenna

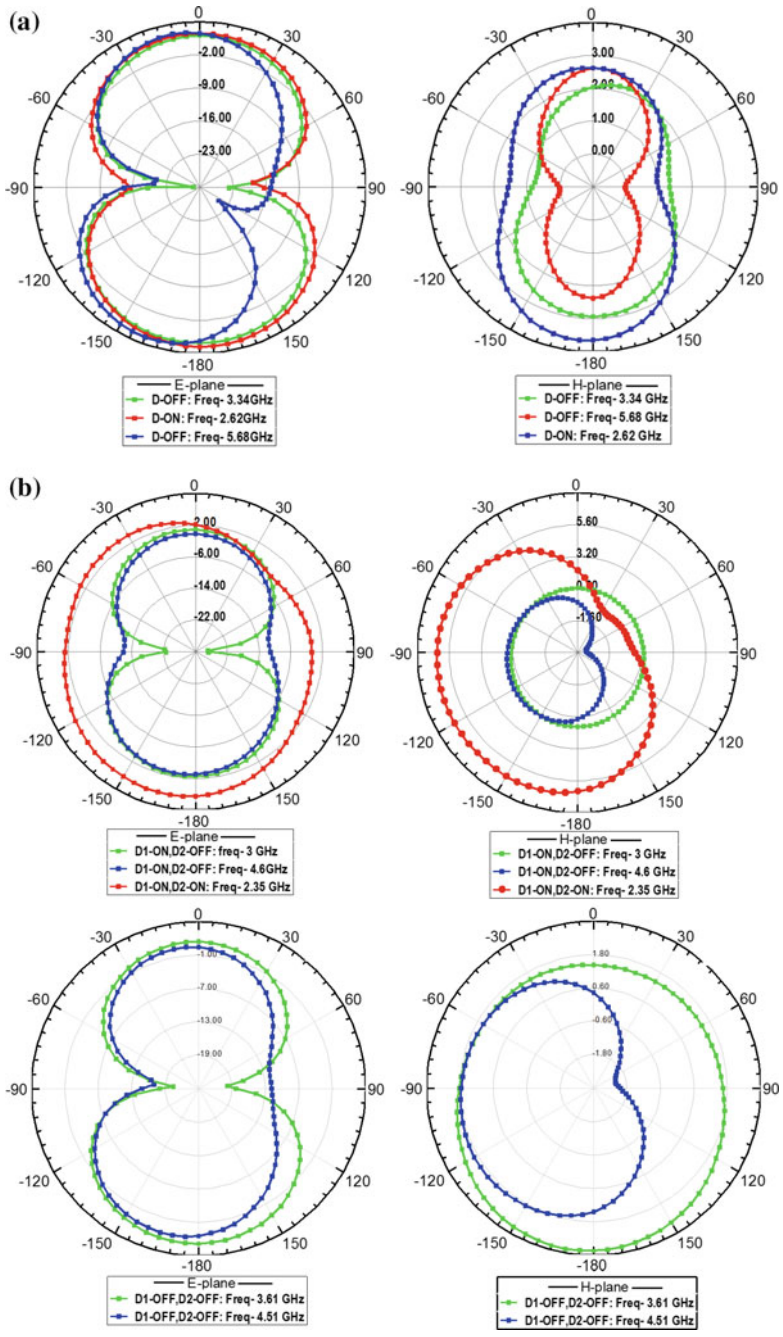


Fig. 7 Simulated radiation patterns of **a** dual frequency reconfigurable antenna and **b** triple frequency reconfigurable antenna plotted at corresponding resonant frequencies in XZ-plane (*left*), YZ-plane (*right*)

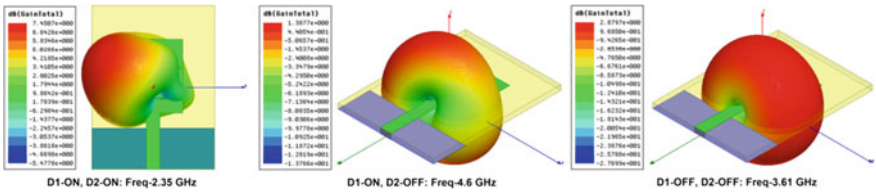


Fig. 8 Simulated Three-dimensional far-field radiation of frequency reconfigurable antenna in D1-ON, D2-ON (*left*) D1-ON, D2-OFF (*center*) D1-OFF, D2-OFF (*right*) cases

Table 3 Gain obtained for triple frequency reconfigurable antenna

D1	D2	Resonating frequency (GHz)	Gain (dB)
ON	ON	2.35	7.45
ON	OFF	4.6	1.38
OFF	OFF	3.61 and 4.51	2.87 and 2.12

4 Conclusions

The proposed Triple Frequency reconfigurable antenna (40 mm × 30 mm × 1.6 mm) resonates at 2.35 GHz, 3.61 GHz and 4.51 GHz in [D1, D2-ON], [D1-ON, D2-OFF], and [D1, D2-OFF] conditions, respectively. The return loss and VSWR values obtained are more than the threshold, making the antenna works for Wi-Fi, Wi-MAX, and C-band applications. Antenna is designed using FR4 substrate which is readily available and cost-effective.

Acknowledgements Authors would like to express their sincere gratitude to the Research Centre of Dept. of ECE and management of Sir C. R. Reddy College of Engineering, Eluru for providing the licensed 3D EM simulation software ANSYS HFSS 15.0 and their esteemed guidance and support to the work.

References

1. Venkateswara Rao, T., Sudhakar, A., Padma Raju, K.: Analysis of Notch in microstrip antenna. International Journal of Advanced Electrical and Electronics Engineering, 4(4), 15–19, ISSN: 2278–8948, Dec (2015).
2. Balanis, C. A.: Modern Antenna Handbook. John Wiley & Sons, Inc., pp. 811–820. (2008).
3. Pozar, D. M.: Microwave Engineering. Fourth Edition, John Wiley & Sons Inc., USA (2012).
4. Mahesh Gadag, M., Danush Kamshetty, S., Suresh Yogi, L.: Design of Different Feeding Techniques of Rectangular Microstrip Antenna for 2.4 GHz RFID Applications Using IE3D. In: Proc. of the Intl. Conf. on Advances in Computer, Electronics and Electrical Engineering, 522–525. (2012).

5. Praveen Kumar, K.., Sanjeeva Rao, K., Sumanth, T., Mohana Rao, N., Anil Kumar, R., Harish, Y.: Effect of Feeding Techniques on The Radiation Characteristics of Patch Antenna. In: International Journal of Advanced Research in Computer and Communication Engineering, 2(2), February (2013).
6. Messaouda, B., Mohammed, B., Zhu, S. Liu, J.: Reconfigurable dual-band circularly polarized microstrip patch antenna for wireless applications. In: J. of Electron. (China) 21(5), 421–425 (2004).
7. Tawk. Y., Christodoulou, C.G.: A New Reconfigurable Antenna Design for Cognitive Radio. In: IEEE Antennas and Wireless Propagation Letters, 8, 1378–1381. (2009).
8. Majid, H.A., Abdul Rahim, M.K., Hamid, M.R., Murad, N.A., Ismail, M.F.: Frequency Reconfigurable Microstrip Patch-Slot Antenna. In: Antennas and Wireless Propagation Letters, IEEE, 12, 218–220 (2013).
9. Alkanhal, M. A. S., Sheta, A. F.: A novel dual-band reconfigurable square-ring microstrip antenna. In: Prog. In Electromagn. Res. (PIER). 70. 337–349. (2007).
10. Venkateswara Rao, T., Jaya, Cheruku.: Frequency Reconfigurable Patch Antenna for Bluetooth, WLAN and Radar Applications. In: International Journal of Innovative Research in Science, Engineering and Technology, 5(4), ISSN: 2319-8753, April (2016).
11. Sabapathy, T., Ahmad, R.B., Jusoh, M., Kamarudin, M.R., Alomainy, A.: A Pattern-Reconfigurable Parasitic Patch Antenna using BAR and HPND PIN Diode. In: 8th European Conference on Antennas and Propagation (EuCAP), 3444–3445 (2014).
12. Fayad, H., Record, P.: Multi-feed dielectric resonator antenna with reconfigurable radiation pattern. In: Prog. In Electromagn. Res. (PIER). 76. 341–356. (2007).
13. Osman. M.N., Rahim, K.A., Yusoff, M.F., Hamid, M.R., Jusoh, M.: Dual-port polarization reconfigurable antenna using compact CPW slot line feeding structure for free-space application. In: IEEE Conference on Antenna Measurements & Applications (CAMA), Dec (2015).
14. Wei, W. -B., Liu, Q.-Z., Yin, Y.-Z., Zhou, H.-J.: Reconfigurable microstrip patch antenna with switchable polarization. In: Prog. In Electromagn. Res. (PIER). 75. 63–68. (2007).

Design of Linear and Circular Arrays Using Natural Search Algorithms for Generation of Low Side Lobe Patterns

M. Vamshi Krishna, G.S.N. Raju and S. Mishra

Abstract Arrays are designed conventionally using standard distribution functions and also using age old techniques like Woodward, Taylor, etc. It is well known that beam width and side lobe are conflicting and is involved in generating a compromise between these two for deserved radiation characteristics. In this paper, design of linear and circular arrays with such optimization is considered. The optimization is carried using the state-of-the-art natural search algorithms like Cuckoo Search Algorithm. Simulation is carried out with the objective of side lobe level (SLL) suppression considering beam width (BW) constraint. These results are compared with that of Accelerated particle swarm optimization.

Keywords Linear array · Circular arrays · Optimization · APSO · CSA

1 Introduction

Antenna arrays hold a lot of advantages in modern day communications [1]. To achieve desired patterns it is necessary that the field elements need to be summed up constructively in wanted direction and add destructively in unwanted directions so the minimal side lobe detection can be done to achieve high power transmission and enhanced spectral efficiency with reduced power consumption.

M. Vamshi Krishna (✉) · S. Mishra
Department of ECE, Centurion University of Technology and Management, Paralakhemundi, Odisha, India
e-mail: vamshi51@yahoo.co.in

S. Mishra
e-mail: s.mishra@cutm.ac.in

G.S.N. Raju
Department of ECE, Andhra University College of Engineering (A), Visakhapatnam, AP, India
e-mail: drrajugsn@yahoomail.co.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*, Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_52

Mobile and Wireless Communication uses various types of antennas out of which most popular are Linear and Circular Arrays [2, 3]. In this paper, we propose natural search algorithms like CSA and APSO to achieve a set of optimum amplitude coefficients positions which provide a maximum side lobe level reduction.

2 Geometry of LA and CA

The geometrical representation of linear array (LA) is as shown in Fig. 1. Similarly, the geometry of the circular array is as shown in Fig. 2. The array factor formulation for both the arrays is very important to obtain corresponding radiation pattern.

The far field distribution for LA is given as [4]

$$E(U) = 2\sum_{n=0}^{N} A_n \cos[k(n-0.5)d(u-u_o)] \tag{1}$$

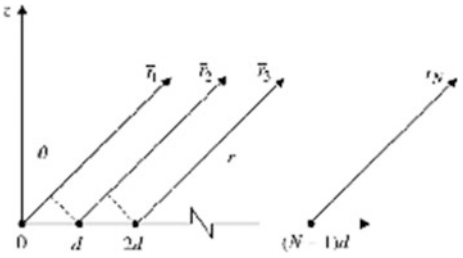


Fig. 1 Geometry of linear array

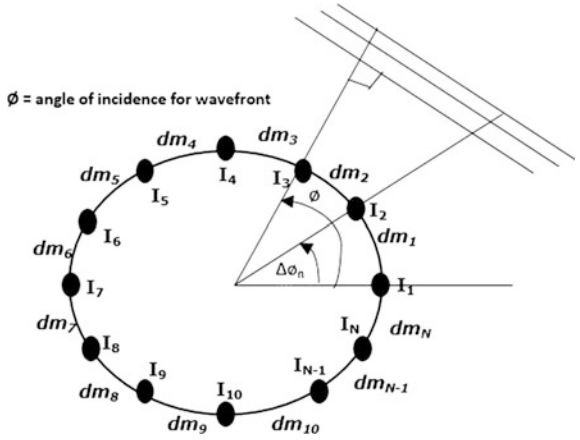


Fig. 2 Non uniform circular array

where

A_n Amplitude of nth element
k wave number = $2\pi/\lambda$
u sin θ
u_0 sin θ_0
θ_0 Scan angle
θ angle between the line of observer and broadside
λ wavelength
d spacing between the radiating elements

Similarly, the array factor formulation of CA is given as

$$AF(\phi) = \sum_{n=1}^{N} I_n \cdot \exp(\mathrm{j} \cdot (\mathrm{kr} \cdot \cos(\phi - \phi_n) + \beta_n)) \tag{2}$$

N refers to total number of elements.
I_n refers to excitation coefficient of nth element.
β_n refers to phase excitation.

Similarly,

$$kr = \frac{2\pi r}{\lambda} = \sum_{i=1}^{N} d_i \tag{3}$$

$$\phi_n = \frac{2\pi}{kr} \sum_{i=1}^{n} d_i \tag{4}$$

3 Nature-Inspired Algorithms

Both the CSA and APSO are discussed in brief in this section as follows.

3.1 CSA

Yang and Deb stated a new metaheuristic search algorithm called Cuckoo Search Algorithm. At initial stages, the host bird discovers the eggs and when it finds that these are not their own, they simply desert the nest and move for a new nest [5]. The main aim is to find best solution (cuckoos) by replacing with old solutions. In the most general form, each nest has one egg called a solution. Instead of a simple random walk, Lévy flight-based random walk style search is used for better performance [6]. As it has only one parameter, it is easy to implement when compared with its counter algorithms [7].

The best nest is chosen as the optimum variable and in this case it refers to the new current amplitude of linear antenna array elements $x_i^{(t+1)}$ for, say cuckoo i, a Lévy flight is simulated [8]

$$X_i^{(t+1)} = X_i^{(t)} + \alpha \oplus \text{Lévy}(\lambda) \tag{5}$$

The Levy flight distribution is typically different from that of random distribution and is given as

$$\text{Lévy} \sim u = t^{-\lambda} (1 < \lambda \leq 3) \tag{6}$$

where, in the above equation, $t^{-\lambda}$, is a parameter dealing with fractal dimension and t being the step size. The value of probability Pa used in this paper is 0.25 as used by Yang and Deb [9].

3.2 APSO

The conventional PSO uses both the global best as well as the local best. Hence, it is capable of handling the solution search modes [10, 11]. However, it is later concluded that the impact of global search is more than the local search. In APSO, the same strategy is incorporated. In conventional PSO the velocity updating is carried as follows.

The working of PSO depends on velocity vector component and position vector component. These are updated using the following expressions:

$$V_n(t+1) = w \cdot V_n(t) + c_1 \cdot r_1(pbest_n - X_n(t)) + c_2 \cdot r_2(gbest - X_n(t)) \tag{7}$$

The corresponding distance is

$$X_n(t+1) = X_n(t) + V_n(t+1) \tag{8}$$

Here 'V' refers to velocity and 'X' refers to displacement of the particle 'n' refers to the *n*th particle. C_1 and C_2 are random constants such that $C_1 + C_2 = 1$. 't' corresponds to the trial or iteration number [12]. As discussed above the APSO uses only the global best and hence the position update is carried out using the following equation.

Here, C_n is random number between (0, 1). α and β values are randomly chosen over the range (0.1–0.4) and (0.1–0.7) respectively [13, 14].

$$X_n(t+1) = (1-\beta)X_n(t) + \alpha \cdot c_n + \beta(gbest) \tag{9}$$

4 Fitness Function

The formulation of the objective function with the aim to suppress the SLL preserving the Taylor BW is given as

$$f1 = \max(\text{null\_depth} + \text{AF}(\theta = \theta_{null(n)})) \quad \text{if AF}(\theta = \theta_{null(n)}) > -35$$
$$= 0 \quad \text{otherwise} \tag{10}$$

$$f2 = SLL_{desired} + \max(\text{SLL}_{\theta = -\pi/2 \text{ to } \pi/2}) \tag{11}$$

5 Results

Results pertaining to the objectives specified are presented in this section.

Linear array for (N = 60) number of antenna elements is considered. The experiments are conducted for a fixed beam width, which is confined to a uniform λ/2 element spacing. The array factor results obtained by the CSA are compared to the array factor obtained using APSO. It has been compared with conventional Taylor series. Specifically, all side lobes have levels less than –35 dB. The results for linear array are placed from Figs. 3 to 4. (Except the first one which is adjacent to the major lobe). Figure 5 shows the circular array factor obtained for N = 60 with same number of elements and λ/2 spacing between element to element it has a maximum side lobe level reduction to –20 dB. CSA provides better performance than its counterpart APSO.

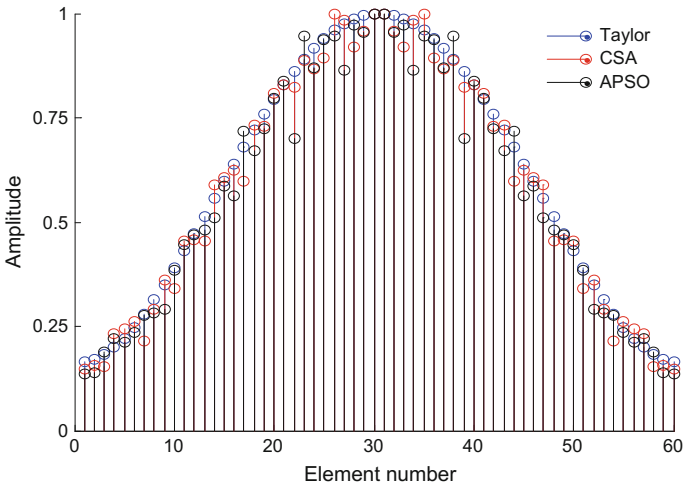


Fig. 3 Amplitude distribution for N = 60 element array using Taylor, CSA & APSO

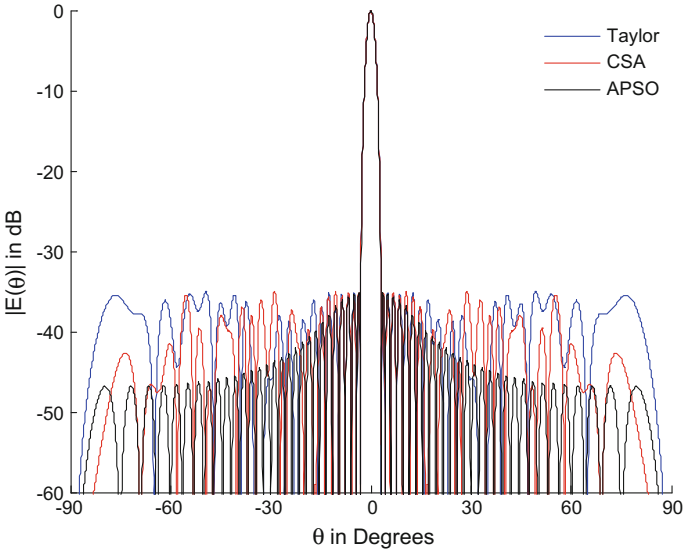


Fig. 4 Sum pattern optimized for N = 60 element array with d = 0.5 and nbar = 6 using Taylor, CSA & APSO

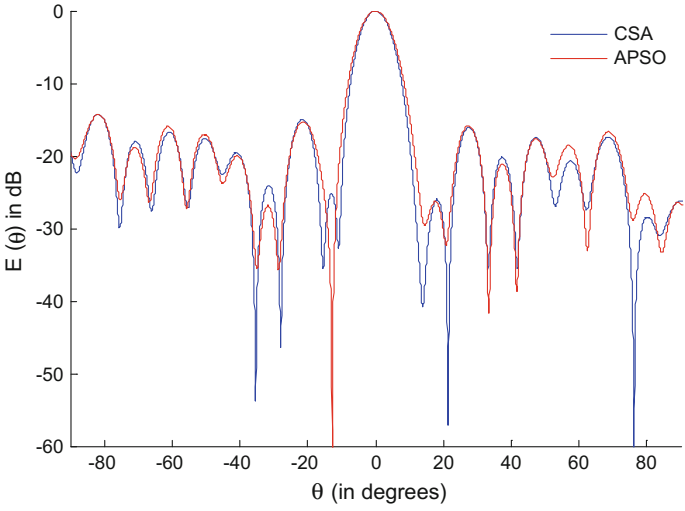


Fig. 5 Nonuniform circular array optimization for N = 60 elements using CSA & APSO

6 Conclusions

The element position and element excitation of each radiating element in Linear and Circular Array are designed using Nature-Inspired Metaheuristics like CSA and APSO. From the above results, it is clear that CSA is found better with its counterpart APSO in designing an array. Derived results had side lobe level reduction and fixed beam width which are found useful in sonar, radar and wireless applications. Reduction in the side lobe level to avoid interference from other sources is mostly been used in radar applications which is very useful. The beam width remains unaltered even after reducing the first side lobe level.

References

1. Collin. R. E., Zucker. F.J.: Antenna theory, New York: McGraw-Hill, (1969)
2. Pathak. N., Mahanti. G. K., Singh. S. K., Mishra. J. K., Chakraborty. A.: Synthesis Of Thinned Planar Circular Array Antennas Using Modified Particle Swarm Optimization, Progress In Electromagnetics Research Letters, Vol. 12, 87–97, (2009)
3. Harrington. R.: Sidelobe reduction by non-uniform element spacing, IRE Transactions on Antennas and propagation. Vol. 9, no. 2, pp. 187–192, 1961
4. Pesik, l. Paul, D. Railton, C. Hilton, G. Beach, M.: FDTD technique for modelling eight element circular antenna array, electronics letters 42 no. 14, 787–788. (July 2006)
5. Panduro, M. Mendez, A. Dominguez, R, Romero, G: design of non-uniform circular antenna arrays for side lobe reduction using the method of genetic algorithms, Int. J. Electron. Commun. (aeu) 60, 713–717. (2006)
6. V. S. S. S. Chakravarthy Vedula, S. R. Chowdary Paladuga, and M. Rao Prithvi: Synthesis of Circular Array Antenna for Sidelobe Level and Aperture Size Control Using Flower Pollination Algorithm, International Journal of Antennas and Propagation, vol. 2015, Article ID 819712, (2015)
7. Yang, X.-S., and Deb, S, Engineering Optimization by Cuckoo Search, Int. J. Mathematical Modelling and Numerical Optimization, Vol. 1, No. 4, 330–343, (2010)
8. Yang, X. S., Deb, S., and Fong, S.: Accelerated Particle Swarm Optimization and Support Vector Machine For Business Optimization And Applications, In: Networked Digital Technologies (NDT2011), Communications In Computer and Information Science
9. Urvinder Singh., Munish Rattan.: Design of Linear and Circular Antenna Arrays Using Cuckoo Optimization Algorithm. Progress in Electromagnetics Research C, Vol. 46, 1–11, (2014)
10. Chakravarthy VVSSS et al, Amplitude-only null positioning in circular arrays using genetic algorithm, Int Conf on Electrical, Computer and Communication (ICECCT), (2015)
11. Nanbo. J., Rahmat-Samii. Y.: Advances in particle swarm optimization for antenna designs: Real-number, binary, single- objective and multi-objective implementations, IEEE Transactions on Antennas and Propagation, Vol. 55, pp. 556–567, (March 2007)
12. Isernia. T., Ares. F.J., Bucci. O.M.: A hybrid approach for the optimal synthesis of pencil beams through array antennas, IEEE Transactions on Antennas and Propagation, Vol. 52, pp. 2912–2918, (November 2004)
13. Song-Han Yang., Jean-Fu Kian.: Optimization of Asymmetrical Difference Pattern with Memetic Algorithm, IEEE Transactions on Antennas and Propagation, Vol. 62, No. 4, (April 2014)

14. Gomez. N.G., Rodriguez. J., Melde. K.L., McNeil. K.: Design of low sidelobe linear arrays with high aperture efficiency and interference nulls, IEEE Transactions on Antennas and Propagation, Vol. 8, pp. 607–610, (2009)
15. Rajo-Iglesias. E., Quevedo-Ternel. T.: Linear array synthesis using ant colony optimization based algorithm, IEEE Transactions on Antennas and Propagation Magazine, Vol. 49, pp. 70–79, (April 2007)

Planar Switchable Notch Band Antenna with DGS for UWB Applications

Allam Vamsee Krishna and B.T.P. Madhav

Abstract A planar notch band antenna with a defected ground structure is proposed in this work. The switchable characteristics for the designed notch band antenna are achieved through open end slots on/off positions. The proposed notch band antenna is capable of notching the frequency bands 3–4 GHz, 5.5–6.5 GHz respectively. A high notch band rejection with VSWR greater than 2 and the return loss greater than −10 dB is achieved at the notching frequencies. The defected ground structure provides balance in the impedance bandwidth to the designed models. By sorting the slots on the radiating structure, the tunability in the notching frequencies are attained in this paper. The antenna radiation characteristics and the surface current distributions at operating bands as well as at notch bands are presented in this work. The proposed notch band antenna is providing high rejection of gain in the notch band and average gain of 2.8 dB in the operating band.

Keywords Defected ground structure · Monopole antenna · Notch band · Switchability · Ultra-wideband

1 Introduction

The accelerated generation of wireless communication systems has constituted a demand for reconfigurable or tunable filters and antennas [1–3]. These type of devices reduce the compulsion to yield extravagant charges correlated with the refitting of wireless infrastructures, considering an adjustment in the frequency,

A. Vamsee Krishna (✉) · B.T.P. Madhav
Department of ECE, K L University, Guntur, AP, India
e-mail: vamseekrishnaa3@kluniversity.in

B.T.P. Madhav
e-mail: btpmadhav@kluniversity.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_53

bandwidth, or other conditions of the hardware can be attained over electronic/mechanical reconfiguration. Reconfigurable equipment further produce the appropriate hardware for a high capable management and adoption of a spectrum through the theory of dynamic spectrum approach and cognitive radio [4–8]. Utilization of reconfigurable devices again allows the time allocation of hardware, which in turn is an advantage to the mass and size contraction of the communication system. This is a great condition in compact devices and of significant influence in satellite communication systems [9–12].

UWB is a radio technology that can use a very low energy level for short range, high bandwidth communications over a large portion of the radio spectrum. Ultra-wideband is a technology for transmitting information spread over a large bandwidth ranging from 3.1 to 10.6 GHz. Ultra-wideband characteristics are well suited to short distance applications, such as peripherals of PC, Personal Area Network (PAN), medical and radar imaging Due to short duration of UWB pulses, it is easier to provide high data rates [13]. Ultra-wideband characteristics are well suited to short-distance applications, due to its low emission levels permitted by regular agencies. The main challenge while designing UWB antennas is to achieve good band notch characteristics with reduced size and cost [14]. Band notch filtering functionally can be achieved using various methods such as using radiating patch with different shapes like rectangular, circular, hexagonal, and with different slots, such as V slot, U slot, W slot, inverted U slot, and elliptical slot.

In this paper notch band antenna model is designed and switches are incorporated in the slots to fine tune the notch band frequencies. Monopole structure with defected ground model is proposed in this work. Frequency tunability with the on and off conditions of the switches at slots are examined.

2 Antenna Geometry and Design

A notch band monopole antenna with inverted u-shaped radiating element is presented in this work. A U slot is also placed on the feed line to achieve notch band characteristics. The back side of the antenna consists of partial ground and an open ended stub for impedance matching. The radiating element consists of another slot on the lower edge nearer to feed line. Depending on the slot on and off conditions the notch band characteristics are analyzed. The geometric aspects of the designed antenna models are presented in Table 1. The proposed dual notch band antenna is prototyped on FR4 substrate with dielectric constant 4.4 and loss tangent 0.02 (Figs. 1, 2, 3 and 4).

Table 1 Antenna dimensional characteristics in mm

Design parameter	Ls	Ws	Lf	Wf	H	W1	W2	W3	W4	W5
Dimensions (mm)	34	34	11.7	2.84	1	13.8	2.2	0.4	0.5	0.6
Design parameter	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10
Dimensions (mm)	4	6	4	0.6	12.4	9.4	7.3	3.2	3.25	11.9
Design parameter	Es	AR	k	g	Gx	R1	R2	rx	Rx1	Rx2
Dimensions (mm)	0.05	2	5	0.8	0.2	5	6	2	R1/AR	R2/AR

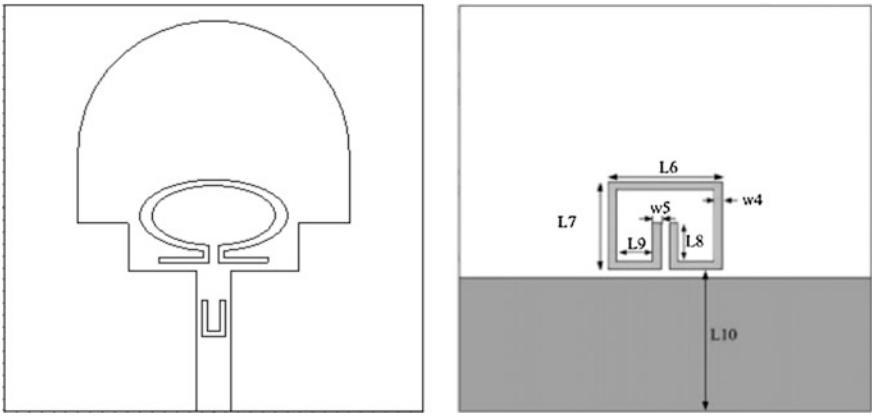


Fig. 1 Notch band antenna model 1

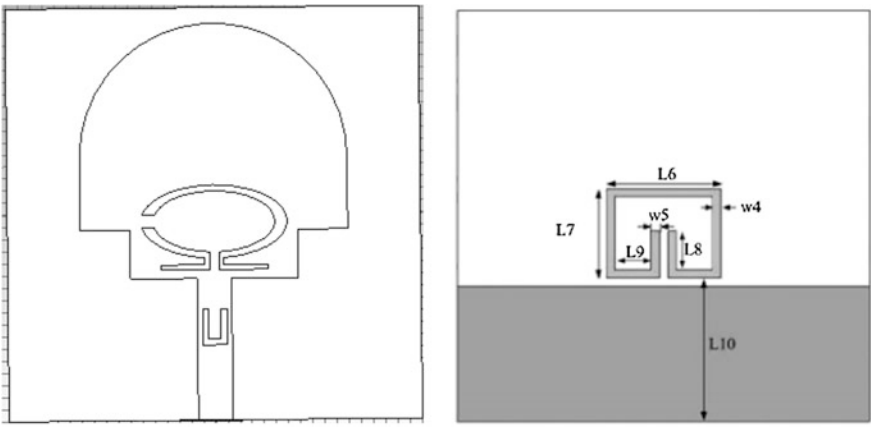


Fig. 2 Notch band antenna model 2

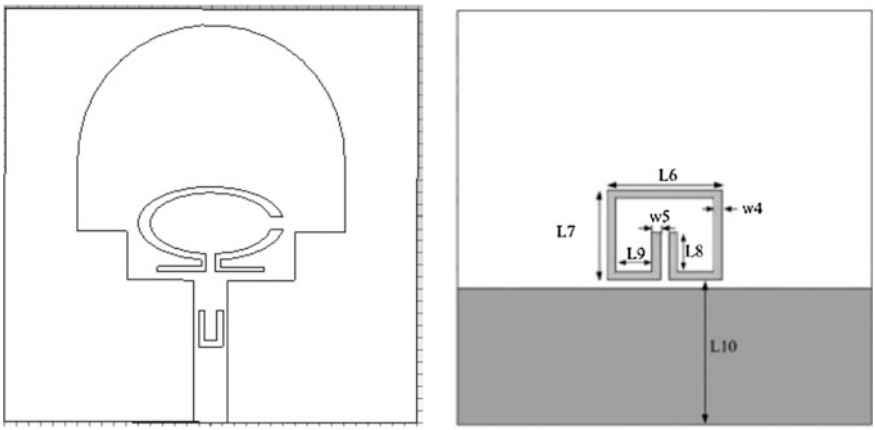


Fig. 3 Notch band antenna model 3

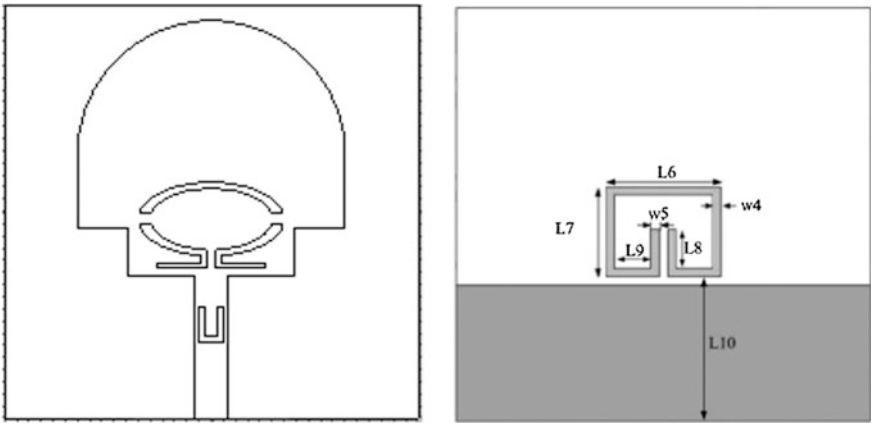


Fig. 4 Notch band antenna model 4

3 Results and Discussion

The designed models are analyzed using commercial electromagnetic tool CST and the results are presented in this section. The reflection coefficients of the designed models are presented in this work to know the operating bands and notch bands for the antenna models. Four models are designed in this work, and by placing switches on the slots we examined the change in resonant frequency and the notch bands. When switch s1 and switch s2 are in off condition then a single notch band can be observed at 5.8–6.2 GHz from Fig. 5. When s1 is off and s2 is on then the notch band is widened and the antenna is notching the band from 4.5 to 6.5 GHz. The

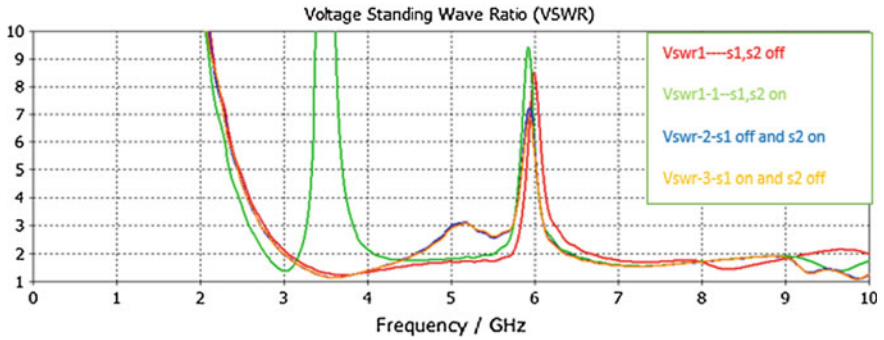


Fig. 5 VSWR versus frequency

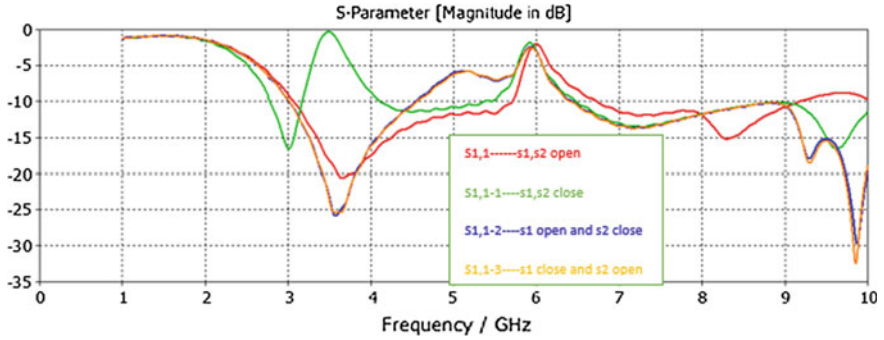


Fig. 6 Return loss versus frequency

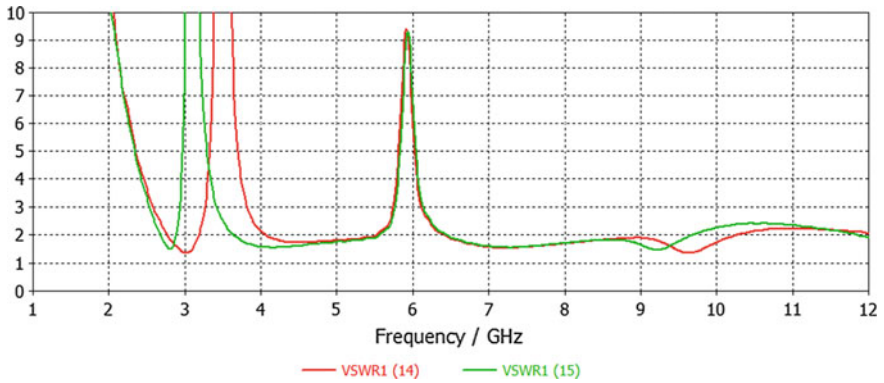


Fig. 7 Parametric analysis with change in r1

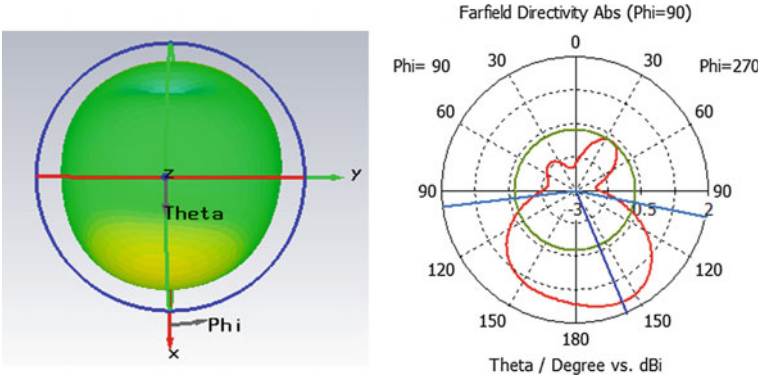


Fig. 8 Radiation pattern of antenna model 1 at 3.486 GHz

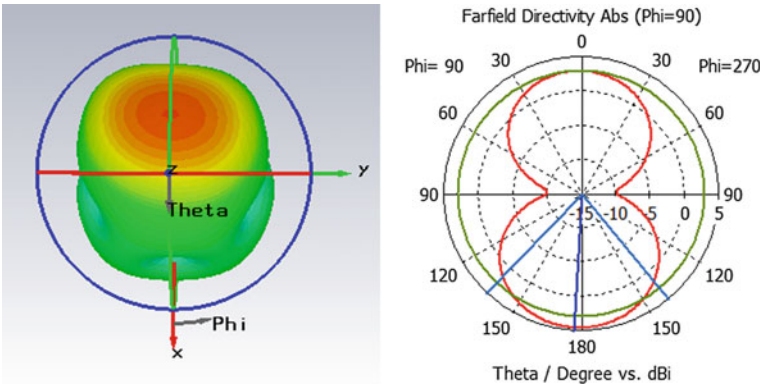


Fig. 9 Radiation pattern of antenna model 1 at 4.5 GHz

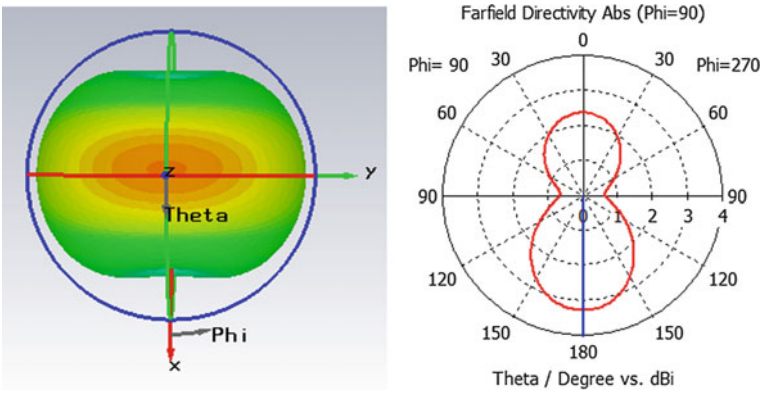


Fig. 10 Radiation pattern of antenna model 1 at 5.9 GHz

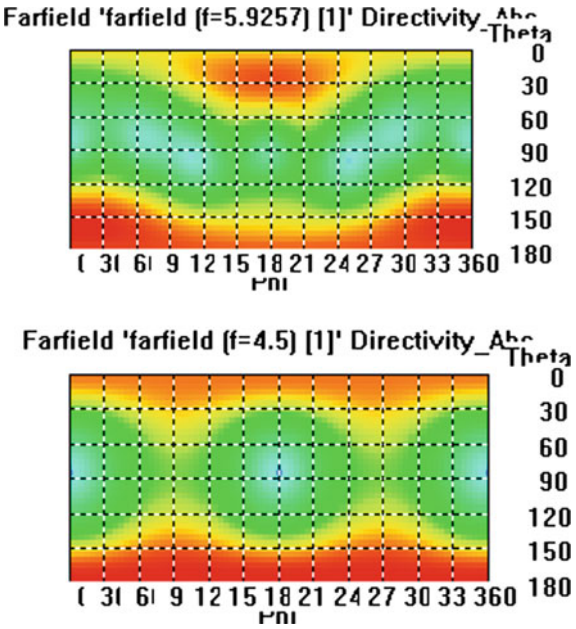


Fig. 11 Far field pattern of proposed dual notch band antenna at 4.5 and 5.9 GHz

same is the case with s1 on and s2 off. When both the switches are in on condition, the proposed model is notching dual band (3.2–4 GHz) and (5.5–6.5 GHz).

The band rejection is also very high at these two notch bands. Figure 6 is providing similar information like VSWR with respect to notch bands and operating bands. The on and off conditions of the switches lead to shift in resonant frequency and notch bands.

Parametric results of VSWR by changing radius r1 from 5 to 5.5 mm are presented in Fig. 7. It is been observed that the there is no change in the notch band from 5.5 to 6.5 GHz, but at fundamental notch band a shift of 0.5 GHz is obtained with change in r1.

The radiation patterns of the single notch band antenna model 1 at different frequencies are presented from Figs. 8, 9, 10. In the operating bands the antenna model 1 is showing a gain more than 5.2 dB and in the notch band the gain is very poor. Antenna is showing directive radiation and monopole like radiation in the operating band, whereas it is showing disturbed pattern in notch band.

The far field radiation of the dual notch band antenna with two switches in on condition is presented in Fig. 11. The three dimensional and polar coordinates based radiation pattern of the antenna is also shown in Fig. 12. Antenna is producing gain more than 5 dB in the operating band and negative values in the notch band. Here, the total radiated power has been normalized to the input power, which is thus equal to the efficiency of the antenna. Also, the proposed structure possesses high notch band-edge selectivity.

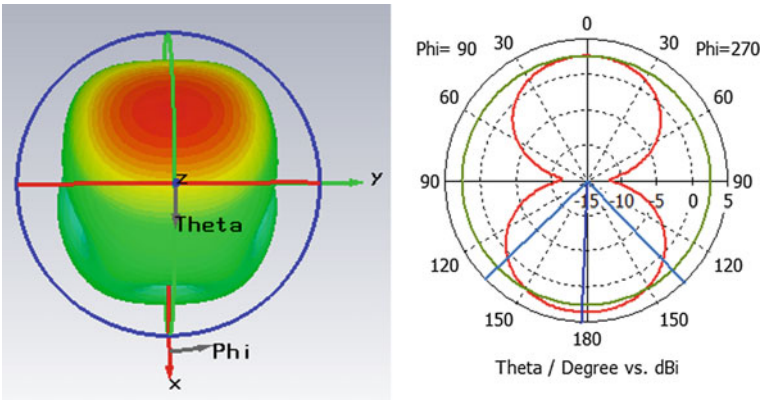


Fig. 12 Radiation pattern of the dual notch band antenna at operating frequency 4.5 GHz

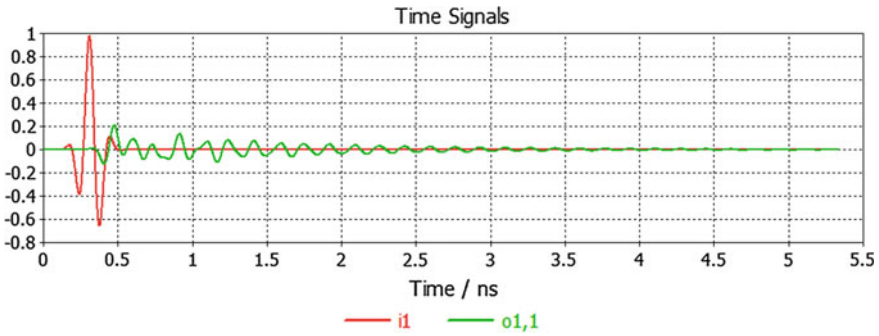


Fig. 13 Normalized source and received pulse when aligned face to face

Figure 13 shows the normalized source and received pulses for dual notch antenna model 2. The pulse fidelity values are larger than 0.5, which gives acceptable range for the case of UWB antennas.

4 Conclusion

A switchable antenna has been designed and analyzed with monopole configuration in this paper. Antennas with slots are demonstrated with on and off conditions to fine-tune the notch band in this work. All the antenna parameters with respect to switching are analyzed and presented. The radiation characteristics and their corresponding directivity and gain parameters are simulated and presented. Antenna with closed switches is providing gain more than 5 dB in the operating band and antenna with open switches providing gain more than 5.2 dB. Time domain

analysis shows the pulse fidelity value more than 0.5 and VSWR < 2 in the operating band. The designed model is simple in structure and easy to fabricate and satisfying the UWB communication requirements.

Acknowledgements The authors feel happy to acknowledge department of ECE, ECM and management of KLU for the support during this work. Dr. B.T.P. Madhav likes to thank DST for their support through grant ECR/2016/000569 and SR/FST/ETI-316/2012.

References

1. W. J. Lui, C. H. Cheng, Y. Cheng, and H. Zhu, "Frequency notched ultra wide band microstrip slot antenna with a fractal tuning stub," Electron. Lett., vol. 41, pp. 294–296 (2005).
2. S.-W. Su, K.-L. Wong, and F.-S. Chang, "Compact printed ultra wideband slot antenna with a band notched operation," Microw. Opt. Technol. Lett., vol. 45, pp. 128–130 (2005).
3. J. William and R. Nakkeeran, "CPW-fed UWB slot antenna with reconfigurable rejection bands," in Proc. Int. Conf. Control, Commun. Power Eng., pp. 154–156 (2010).
4. J. R. Kelly, P. S. Hall, and P. Gardner, "Integrated wide-narrow band antenna for switched operation," in Proc. IEEE EuCAP, Berlin, Germany, pp. 3757–3760 (2009).
5. B T P Madhav, A Manikanta Prasanth, Sreeramineni Prasanth, Batchu Mohan Sai Krishna, Devani Manikantha, Usirika Sharmila NagaSai, "Analysis of Defected Ground Structure Notched Monopole Antenna", ARPN Journal of Engineering and Applied Sciences, ISSN 1819-6608, Vol. 10, No. 2, pp 747–752 (2015).
6. B T P Madhav, Harish Kaza, Thanneru Kartheek, Vidyullatha Lakshmi Kaza, Sreeramineni Prasanth, K S Sanjay Chandra Sikakollu, Maneesh Thammishetti, Aluvala Srinivas, K V L Bhavani, Novel Printed Monopole Trapezoidal Notch Antenna with S-Band Rejection, Journal of Theoretical and Applied Information Technology, ISSN: 1992-8645, Vol 76, No 1, pp 42–49 (2015).
7. P.Lakshmikanth, Kh Takeshore, B T P Madhav, Printed Log Periodic dipole antenna with Notched filter at 2.45 GHz Frequency for wireless communication applications, Journal of Engineering and Applied Sciences, ISSN: 1816-949X, Vol 10, Issue 3, pp 40–44. DOI:10.3923/jeasci.2015.40.44 (2015).
8. D S Ram Kiran, B T P Madhav, Novel compact asymmetrical fractal aperture Notch band antenna, Leonardo Electronic Journal of Practices and Technologies, ISSN 1583-1078, Vol 27, Issue 2, pp 1–12 (2015).
9. M. V. Reddiah Babu, Sarat K. Kotamraju, B. T. P. Madhav, Compact Serrated Notch Band Mimo Antenna for UWB Applications, ARPN Journal of Engineering and Applied Sciences, ISSN 1819-6608, VOL. 11, NO. 7, pp 4358–4369 (2016).
10. K V L Bhavani, Habibulla Khan, D Sreenivasa Rao, B T P Madhav, Dual Band Notched Planar Printed Antenna with Serrated Defected Ground Structure, Journal of Theoretical and Applied Information Technology, ISSN: 1992-8645, Vol 88, Issue 1, pp 28–34 (2016).
11. M. L. S. N. S. Lakshmi, B. T. P. Madhav, Habibulla Khan, Tapered Slot CPW-Fed Notch Band MIMO Antenna, ARPN Journal of Engineering and Applied Sciences, ISSN: 1818-6608, VOL. 11, NO. 13, pp 1–7 (2016).
12. P Syam Sundar, Sarat K Kotamraju, B T P Madhav, Parasitic Strip Loaded Dual Band Notch Circular Monopole Antenna with Defected Ground Structure, International Journal of Electrical and Computer Engineering (IJECE), ISSN: 2088-8708, Vol. 6, No. 4, pp. 1742–1750, DOI:10.11591/ijece.v6i4.10529 (2016).

13. Y. S. V. Raman, B. T. P. Madhav, Analysis of Circularly Polarized Notch Band Antenna with DGS, ARPN Journal of Engineering and Applied Sciences, ISSN: 1819-6608, Vol. 11, No. 17 (2016).
14. Thomas K G, Sreenivasan M. Compact triple band antenna for WLAN/WiMAX applications. Electronics Letters, 45(16): 811–813 (2009).

Design and Simulations of Implanted Antenna Inside the Human Body

Medikonda Ashok Kumar, Susanth K. Mandal and G.S.N. Raju

Abstract Antennas are used in biomedical applications particularly for EM Radiation energy therapy of different tumors. Most often they are used in the frequency range of MHz. In this paper a spiral Planar inverted F antenna is to operate a MICS (Medical Implanted Communication Service) frequency range of 402–405 MHz. It is designed to implant inside the human body for the treatment of different tumors. The design is carried out using HFSS software. The antenna performance characteristics are analyzed using parameters like i/p impedance, reflection coefficient, Return loss, 3D Gain and E-Field distribution are obtained.

Keywords Planer inverted—F antenna (PIFA) · Implanted antenna · Microstrip patch antenna · High-frequency structural simulator (HFSS) · Medical implant communication service (MICS)

1 Introduction

Most of the research in radiation system for biomedical applications is related to producing hyperthermia for medical treatments and monitoring various parameters [1, 2]. These antennas demanded features like small size, low power requirement, and impedance matching. Similarly, it involves in monitoring other parameters.

M. Ashok Kumar (✉)
Department of ECE, Centurion University of Technical & Management, Paralakhemundi, Odisha, India
e-mail: ashok.medikonda@yahoo.com

S.K. Mandal
Department of ECE, Centurion University of Technical & Management, Bhubaneswar Campus, Paralakhemundi, Odisha, India
e-mail: susantakumar@yahoo.com

G.S.N. Raju
Department of ECE, Andhra University, Visakhapatnam, Andhra Pradesh, India
e-mail: profraju@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*, Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_54

Implanted antennas are often used for such applications. Designing antennas which can be implanted inside the human body has to consider several biological aspects [2, 3]. Hence, it is a challenging task. Although several antennas have been proposed for implantable medical devices [4, 5], the accurate full human body model has been rarely included in the simulations. In this paper, an implantable PIFA is proposed based on the design [6] for communication between implanted medical devices in body and outside medical equipment. Since, the MICS band ranging from 402 to 405 MHz, the research on antenna is accelerated. In this paper, PIFA is designed for MICS band. The main aim of this work is to optimize the proposed implanted antenna inside the skin tissue of human body model and characterize the electromagnetic radiation effects on human body tissues. Simulations have been performed using HFSS.

In this paper, a low profile implantable patch antenna design has been performed. The design is carried out in HFSS EM tool with the design consideration like boundary conditions of human biological system. Reports in terms of S11, 3D Gain and radiation pattern are used for analysis. Further, the paper is organized as follows. Simulation description of the proposed design is discussed in Sect. 1. Description of the geometry is presented in Sect. 2. Brief reports about the antenna design along with analysis is presented in Sect. 3. Overall conclusion is mentioned in Sect. 4.

2 Low Profile Implanted Antenna: Design

The general shape of the proposed micro strip patch antenna design for implantation is based on the work presented in [3, 4]. The design of proposed antenna and side view with in single layer, three layers are illustrated in Figs. 3 and 4. The antenna is simulated in HFSS (High-Frequency Structural Simulator), which is based on Finite Element Method (FEM) electromagnetic solver. In this simulation, Rogers R03210 ($\varepsilon r = 10.2$ and $\tan\delta = 0.003$) is used as a substrate and substrate material. The origin of the coordinate system is located in the center of the Antenna's ground plane. The thickness of dielectric layer of both substrate and superstrate is 4 mm. The length and width of the substrate and main patch is in the Table 3. The other parameters of antenna are considered to be changed within the solution space in order to improve PIFA performance at 402–405 MHz MICS frequency [3]. HFSS Optometric, an integrated tool in HFSS for parametric sweeps and optimizations, is used for tuning and improving the antenna characteristics at the MICS bands inside the ANSYS human body model. The location of the feed can be optimized along x-and y-axis to match the antenna to 50Ω over MISC band. The strip lengths are also included in optimizations to provide more degrees of freedom for improving the PIFA performance at the desired frequency band (402–405 MHz). The 3D view of the implantable PIFA is demonstrated in Fig. 2 (Fig. 1).

In order to study the design in realistic environment, implantable antennas can be evaluated within accurate human body models. In fact, as for particular biomedical applications, implant positions and depth could be different. In this condition,

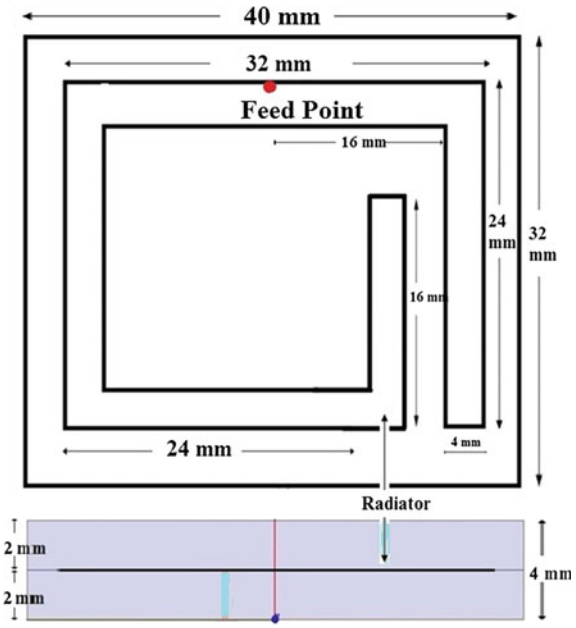


Fig. 1 Proposed spiral microstrip patch antenna

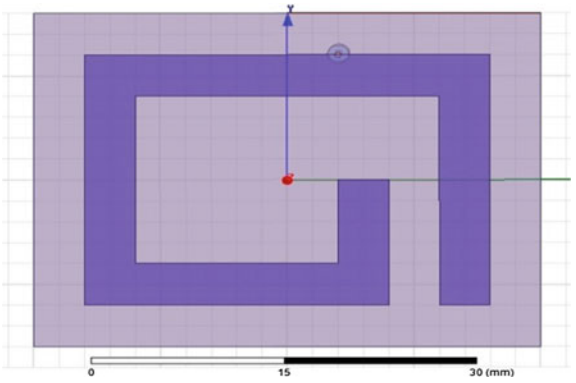


Fig. 2 Design of spiral microstrip patch antenna using HFSS

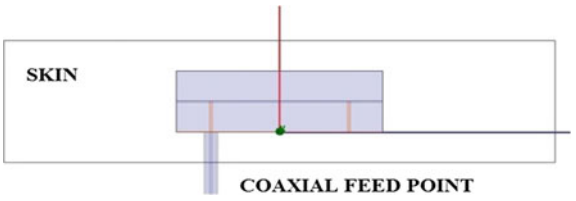


Fig. 3 Design of antenna geometry for one layers (skin)

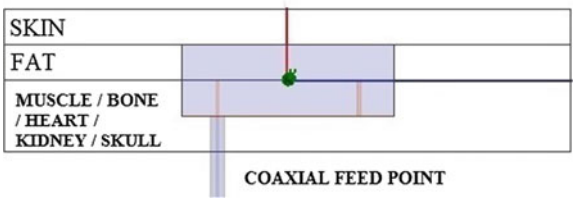


Fig. 4 Design of antenna geometry for three layers (skin, fat, and muscle/bone/heart/kidney/skull)

Table 1 Electrical data of biological tissues [2]

Organ	Permittivity-ε_r	Conductivity	Density
Bone	13.1	0.09	1.81
Heart	66	0.97	1.05
Kidney	66.4	1.1	1.05
Skull	17.8	0.16	1.18

simplified one-layer skin or three-layer tissue model may have low accuracy for antenna design. Accurate human body model is needed for specific applications, such as wireless endoscope systems and neural recording systems. Table 1 shows the electrical data of biological tissues (Fig. 5).

The specific absorption rate (SAR) is a measure of the amount of electromagnetic energy absorbed in a lossy dielectric material. The SAR is a basic scalar field quantity that can be plotted on surfaces or within objects in HFSS. Figure 6 shows the proposed antenna SAR from 1.7959e-004 to 2.0696-001 W/kg.

The proposed antenna is subjected to several modifications in terms of layer distribution like single and three layers form. The analysis of these two is carried out in two cases. Case-1 deals with single-layer form while the analysis of three

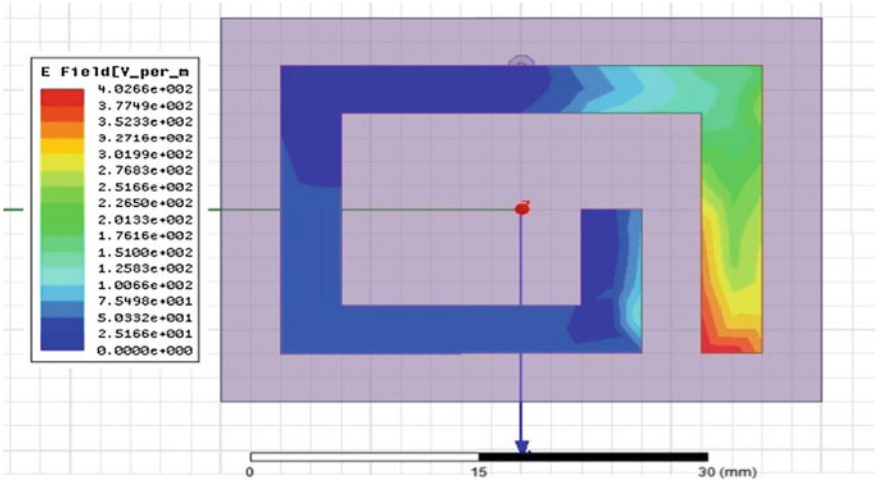


Fig. 5 E-field distribution in designed antenna

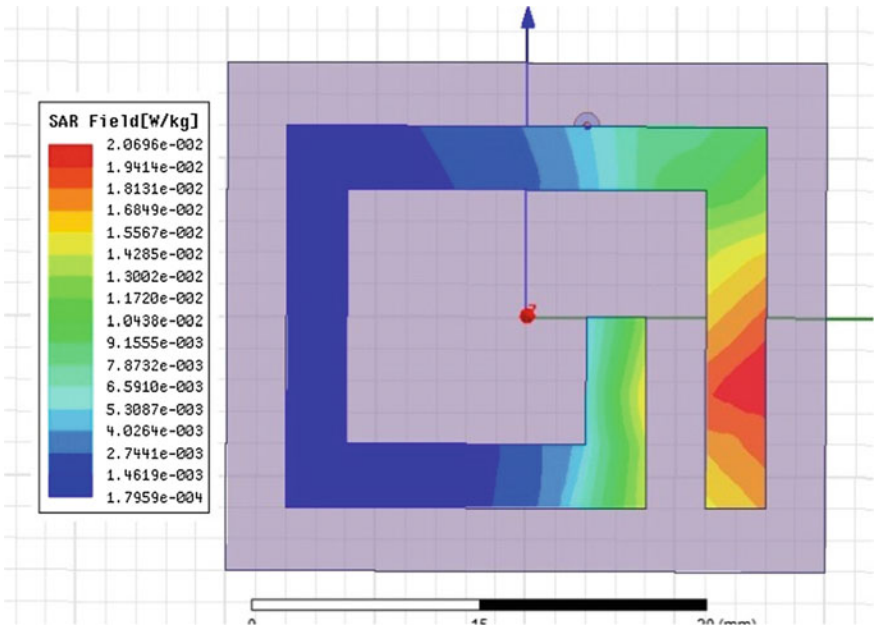


Fig. 6 SAR distribution of proposed antenna

Table 2 Types and layers

S.No	Type	Layers
1	Case-1	Free space
2	Case-2 a	Skin, fat, and bone
3	Case-2 b	Skin, fat, and heart
4	Case-2 c	Skin, fat, and kidney
5	Case- 2 d	Skin, fat, and skull

layers is discussed in case-2. However, case-2 has another 4 variations with respect to the material forming the three layers. A thorough discussion of the corresponding case wise results are discussed as follows (Table 2).

3 Simulation Results and Analysis

Simulation results pertaining to the proposed models are presented in this section. The simulation-based experiment is divided into four cases as mentioned in the previous section. The physical dimension of the proposed antenna is given in Table 3. The case wise results and discussion are provided as follows

Table 3 Length, width, and radius of different parameters

Parameter		Dimensions (mm)
Main patch	Length	16
	Width	24
Substrate (air)	Length	24
	Width	32

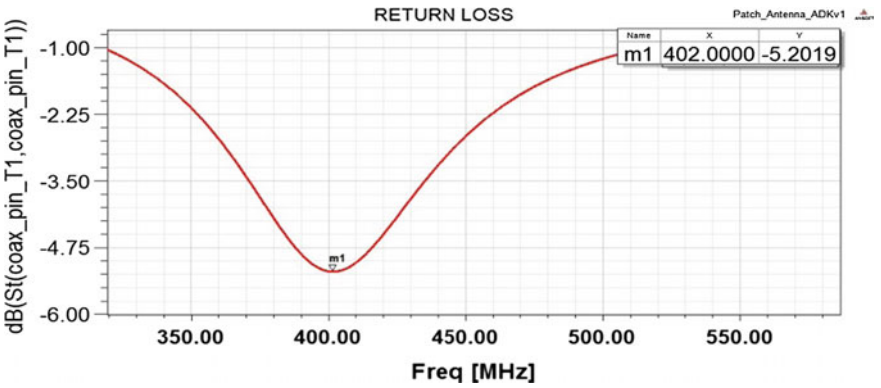


Fig. 7 Return loss (Frequency = 402 MHz and Total Gain = −5.20 dB)

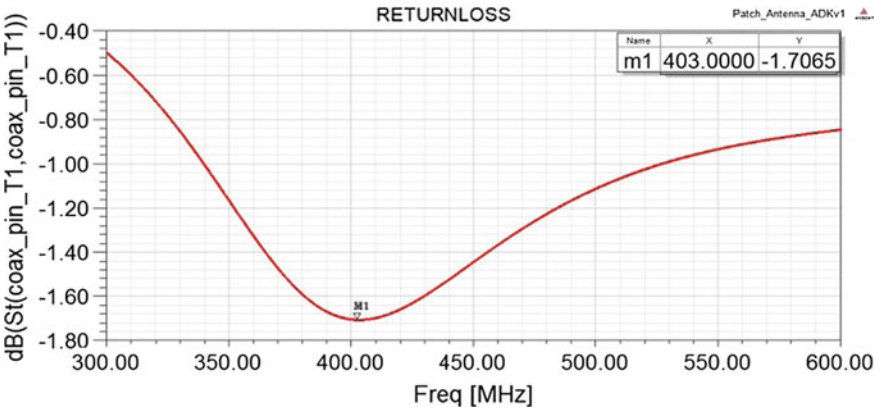


Fig. 8 Return loss (Frequency = 403 MHz and Total Gain = −1.70 dB)

CASE-1 Proposed antenna Return loss within the single layer (Skin)

The S_{11} of the implanted PIFA is presented in Fig. 7. The S_{11} is at 402 MHz with −5.20 db. The proposed PIFA is matched at MICS frequency limit at 402–405 MHz.

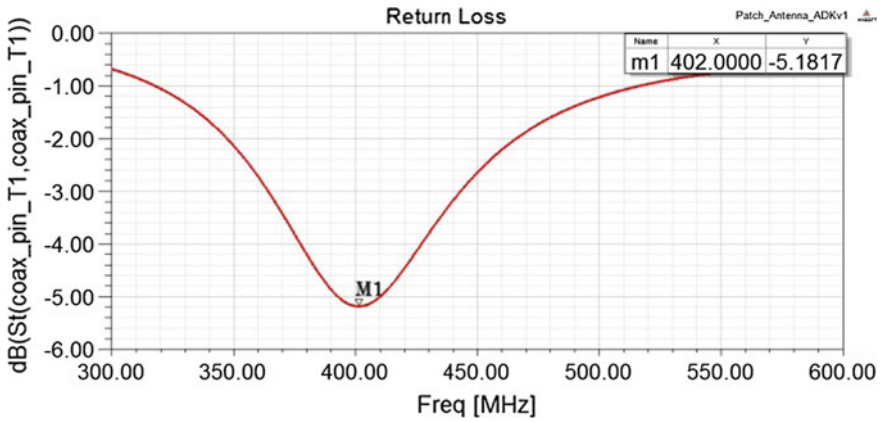


Fig. 9 Return loss (Frequency = 402 MHz and Total Gain = −5.18 dB)

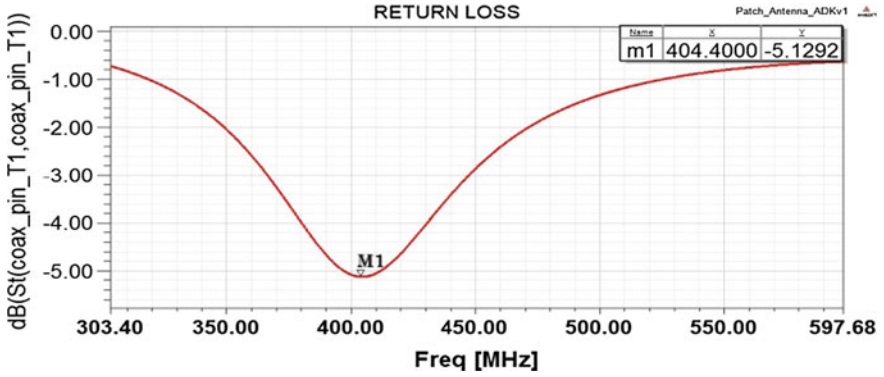


Fig. 10 Return loss (Frequency = 404 MHz and Total Gain = −5.12 dB)

CASE-2 (a) proposed antenna Return loss for three layers (Skin, Fat, and Bone)

The S_{11} of the implanted PIFA is presented in Fig. 8. The S_{11} is at 403 MHz with −1.70 dB. The proposed PIFA is matched at MICS frequency limit at 402–405 MHz

(b) Proposed antenna Return loss for three layers (Skin, Fat, and Heart)

The S_{11} of the implanted PIFA is resented in Fig. 9. The S_{11} is at 402 MHz with −5.18 dB. The proposed PIFA is matched at MICS frequency limit at 402–405 MHz.

(c) Proposed antenna Return loss for three layers (Skin, Fat, and Kidney)

The S_{11} of the implanted PIFA is presented in Fig. 10. The S_{11} at 404 MHz with −5.12 dB. The proposed PIFA is matched at MICS frequency limit at 402–405 MHz.

Table 4 Analysis of different parameters for Case-2 a, b, c, and d

Parameter	Skin Fat Bone	Skin Fat Heart	Skin Fat Kidney	Skin Fat Skull
Peak directivity	1.21138	1.89407	1.97858	1.2942
Peak gain	0.0153524	0.0187999	0.0179972	0.0122168
Peak realized gain	0.00233111	0.00240635	0.00243545	0.00196063
Radiated power (W)	3.20132e-005	1.25933e-005	1.23167e-005	2.43755e-005
Accepted power (W)	0.002526	0.00126876	0.00135407	0.00258226
Incident power (W)	0.0166359	0.00991236	0.0100062	0.0160902
Radiation efficiency	0.0126734	0.00992565	0.00909602	0.0094396
Front to back ratio	1.07261	4.69749	5.49182	1.25426
Gain (dB)	−1.65	−5.18	−5.12	−2.20
***Frequency* (MHz)**	***403***	***402***	***404***	***402.5***

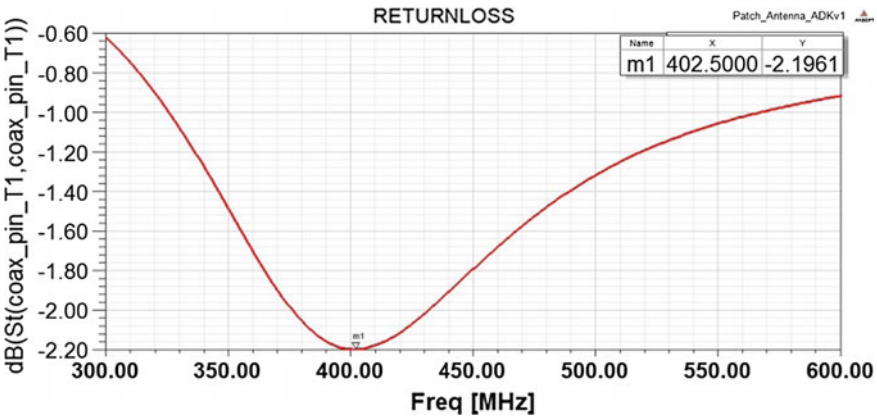


Fig. 11 Return loss (Frequency = 402.5 MHz and Total Gain = −2.19 dB

(d) Proposed antenna Return loss for three layers (Skin, Fat, and Skull) (Table 4).

The S_{11} of the implanted PIFA is presented in Fig. 11. The S_{11} is at 402 MHz with −2.19 dB. The proposed PIFA is matched at MICS frequency limit at 402–405 MHz.

4 Conclusion

In this study, we presented an implanted PIFA inside skin tissue of human body for treatment of different tumors at MICS band. The design and simulation of the antenna was performed using HFSS electromagnetic solver. The optometric feature of HFSS

was employed to optimize the antenna performance at 402–405 MHz. The optimization results demonstrate that the length variation of the radiating strip affects the resonance frequency significantly. The resonance frequency, reflection coefficient, radiation characteristic of the implanted antenna were evaluated. For the sake of more investigations, an extensive antenna optimization could be performed to obtain miniaturized antenna size and improved antenna performance for implantable medical devices.

References

1. W. C. Liu, S. H. Chen, and C. M. Wu, "Implantable broadband circular stacked PIFA antenna for biotelemetry communication," J. of Electromagnetic Waves and Appl., vol. 22, pp. 1791–1800(2008).
2. Medical implant communications service (MICS) federal register, Rules Reg., vol. 64, no. 240, pp. 69926–69934(1999).
3. W. C. Liu, S. H. Chen, and C. M. Wu, "Implantable broadband circular stacked PIFA antenna for biotelemetry communication," J. of Electromagnetic Waves and Appl., vol. 22, pp. 1791–1800(2008).
4. Changrong Liu, Yong-Xin Guo, and Shaoqiu Xiao A review of Implanted antennas for wireless Biomedical devices, in FERMAT, Dec. 2012.
5. J. Kim and Y. Rahmat-Samii, "An implantable antenna in the spherical human head: SAR and communication link performance," presented at the IEEE Topical Wireless Communication Technology Conf., (2003).
6. Medical implant communications service (MICS) federal register, Rules Reg., vol. 64, no. 240, pp. 69926–69934, (1999).

Design of Microstrip Patch Antenna for RFID Reader Applications

K.P. Vinay, B. Ramesh, Lal Babu Prasad and D.V. Rama Koti Reddy

Abstract Slot antennas are effective in handling bandwidth issues. Recently, these slot antennas are employed in RFID applications where bandwidth is a limiting factor when compared with its directivity as both the parameters are mutually conflicting. In this paper, triangular slot geometry is proposed for its obvious advantages of improved directivity and bandwidth applications in several mobile applications. The designed slot is excited with an inset feed system. The antenna design is validated using measured S_{11} and VSWR parameters on the fabricated prototype. The bandwidth of the proposed geometry reported to 40 MHz, which is quiet sufficient to cover the RFID requirements.

Keywords RFID · Slot antennas · Inset feed

1 Introduction

Due to the advancements in wireless communications, the Radio Frequency Identification (RFID) technology gained attraction in various sectors due its own advantages. RFID technology is used for faster data rates, for high range communication, for no line-of-sight communication and for large storage capacity compared to conventional bar code technology [1]. It consists of two blocks namely, RFID transceivers (readers) and RFID transponders (tags). The tag consists

B. Ramesh · L.B. Prasad
Department of ECE, Ragu Engineering College, Visakhapatnam, India
e-mail: rameshboddu11@gmail.com

L.B. Prasad
e-mail: gulablal@gmail.com

K.P. Vinay (✉) · D.V. Rama Koti Reddy
Department of Instrument Technology, Andhra University, Visakhapatnam, India
e-mail: phanikvinay@gmail.com

D.V. Rama Koti Reddy
e-mail: rkreddy_67@yahoo.co.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_55

of a small integrated circuit for storing information and an antenna for communication [2]. Several frequency bands have been assigned to RFID applications: 125 kHz, 13.56 MHz, 869 MHz, 902–928 MHz, 2.45 (2.4–2.483) GHz, and 5.8 (5.725–5.875) GHz [3].

In telecommunications, Microstrip Patch Antenna (MPA) is widely used because of their several advantages like light weight, low volume, low fabrication cost, and broadband applications. The major disadvantages are narrow bandwidth, low gain, and low efficiency [4]. Many researchers are working in this area to increase the bandwidth. Several microstrip antennas for RFID tag have been proposed [5–8]. However, they are complex to design and exhibit narrow bandwidth. Hence, we propose a simple square-shaped patch with triangular slot for RFID applications which is operating at 2.4 GHz. Inset feeding technique is used to feed the patch.

The remainder of this paper is organized as follows: Sect. 2 briefly presents the proposed design. Section 3 summarizes the antenna performance by simulating the proposed design. The performance of the antenna is analyzed by comparing the simulation results with fabricated antenna results and finally Sect. 4 concludes the proposed work.

2 Antenna Design

In this paper, a square-shaped microstrip patch antenna with resonating frequency $f_r = 2.44$ GHz is proposed. The dielectric substrate used for fabrication is FR4 glass epoxy of 1.6 mm thickness which has dielectric constant $\varepsilon_r = 4.3$. The length and width of the patch are calculated as follows:

Width of the patch, $W = \frac{c}{2f_r}\sqrt{\frac{2}{\varepsilon_r + 1}}$

where C is velocity of light.

$$W = \frac{3 * 10^8}{2 * 2.44 * 10^9}\sqrt{\frac{2}{4.3 + 1}} = 37.74\,\text{mm}$$

In order to calculate the actual length of the patch first, we have to calculate the effective length and length extension. To calculate effective length we have to know the effective dielectric constant which is given by

Effective dielectric constant

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + 12\frac{h}{W}}}\right] = \frac{4.3 + 1}{2} + \frac{4.3 - 1}{2}\left[\frac{1}{\sqrt{1 + 12\frac{1.6}{37.74}}}\right] = 3.74\,\text{mm}$$

Effective length

$$L_{eff} = \frac{c}{2f_r\sqrt{\varepsilon_{eff}}}$$

where h is the thickness of dielectric substrate.

$$L_{eff} = \frac{3 * 10 \wedge 8}{2 * 2.44 * 10 \wedge 9\sqrt{3.74}}$$
$$= 0.031\,\text{m} = 31\,\text{mm}.$$

Length extension $\Delta L = 0.412h\frac{(\varepsilon_{eff}+0.3)\left[\frac{W}{h}+0.264\right]}{(\varepsilon_{eff}-0.258)\left[\frac{W}{h}+0.8\right]}$

$$= 0.412 * 1.6\frac{(3.74+0.3)\left[\frac{37.74}{1.6}+0.264\right]}{(3.74-0.258)\left[\frac{37.74}{1.6}+0.8\right]} = 0.65\,\text{mm}.$$

Then the actual length is calculated from the formula

$$L = L_{eff} - 2\Delta L$$
$$= 31 - 2*0.65 = 29.26\,\text{mm}.$$

From the above-obtained patch dimensions, we have calculated the ground plane and substrate dimensions as follows:

$$\text{Length} = 6\text{h} + \text{L} = 6 * 1.6 + 29.26 = 38.86\,\text{mm}$$
$$\text{Width} = 6\text{h} + \text{W} = 6 * 1.6 + 37.74 = 47.34\,\text{mm}.$$

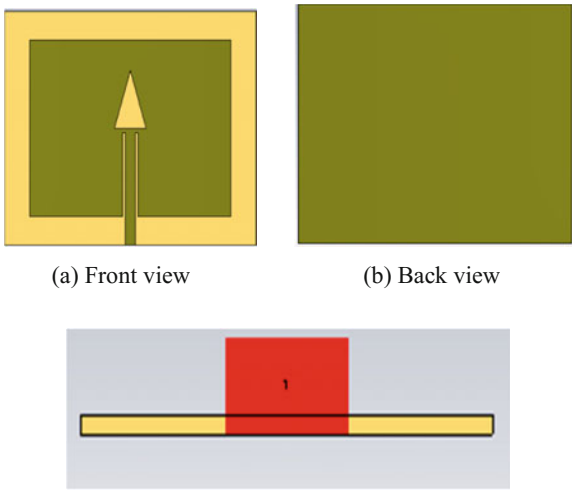
From the above design procedure, the obtained values and the optimized values are shown in Table 1.

Table 1 Calculated and optimized values

Parameter	Calculated value (mm)	Optimized value (mm)
Patch width, pw	37.74	37.74
Patch length, pl	29.26	28
Patch thickness, t	0.01	0.01
Substrate width, W	47.34	47.34
Substrate length, L	38.86	38.86
Substrate thickness, h	1.6	1.6
Inset feed length, iw	0.5	0.5
Inset feed length, il	14	12

3 Proposed Antenna Design

From the above-proposed dimensions, we have started our antenna design in CST design environment. In order to improve the performance of the antenna we have gone for optimization. First, we have optimized the patch length and then we have gone for inset feeding technique. Finally we have designed a triangular slot on the patch. The proposed antenna design is shown in Fig. 1 which consists of front view, rear view which is showing the ground plane and port view.



(a) Front view (b) Back view

(c) Port view

Fig. 1 Proposed simulated antenna design

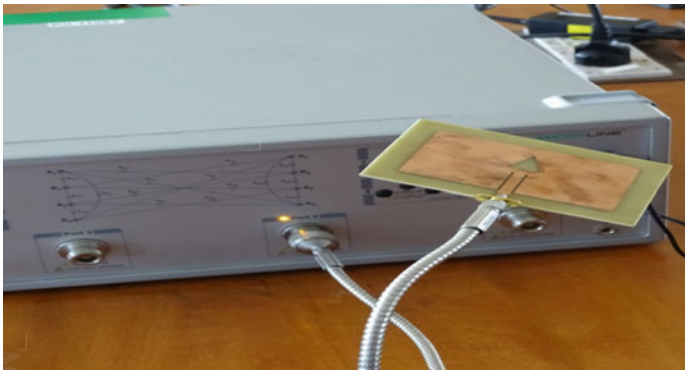


Fig. 2 Fabricated antenna

Figure 2 shows the fabricated antenna to verify the performance of the proposed simulated antenna.

The fabricated antenna is tested by using vector Network Analyzer.

4 Results and Discussion

The return loss plot of basic design is shown in Fig. 3. From the return loss plot, it is observed that the return loss is −4.73 dB which is greater than the reference value, i.e., −10 dB.

By optimization of patch and by modifying the feed to inset type, the performance is improved. The return loss of −55.974 dB at resonating frequency of 2.471GHz is observed and it is shown in Fig. 4. And the return loss obtained for fabricated antenna is shown in Fig. 5 which is −15.4851 dB at a resonating frequency of 2.43 GHz.

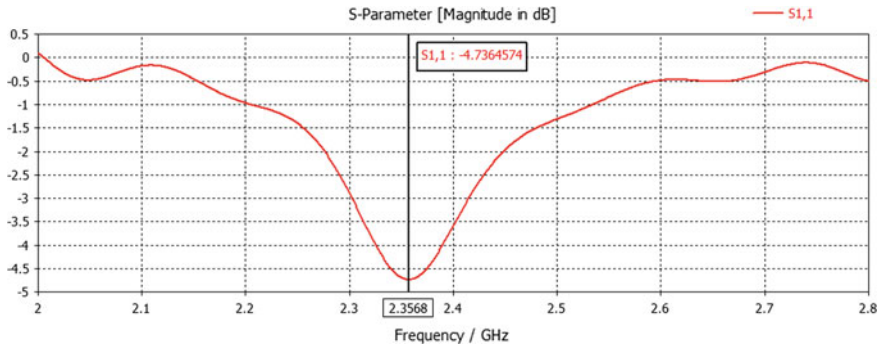


Fig. 3 Return loss plot of basic antenna

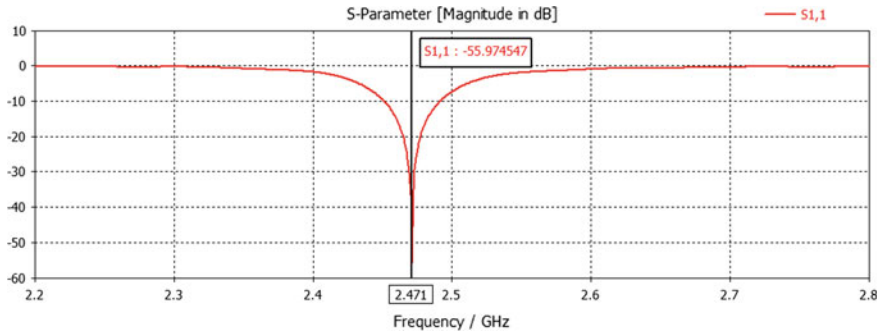


Fig. 4 Simulated return loss plot

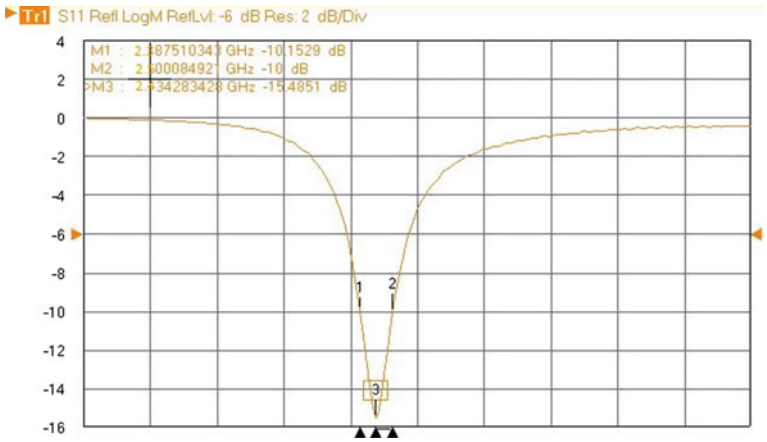


Fig. 5 Return loss plot of fabricated antenna

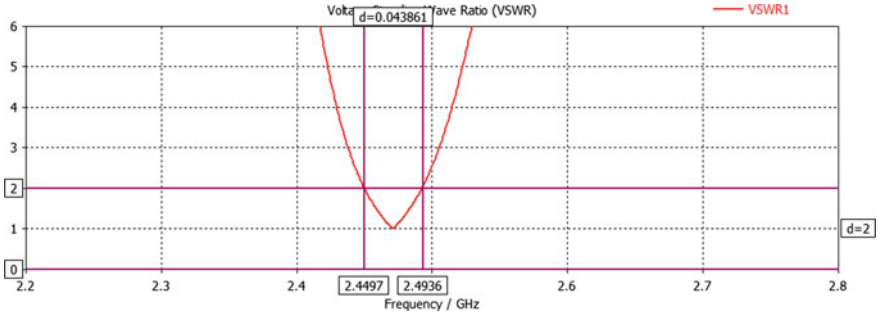


Fig. 6 Simulated VSWR plot

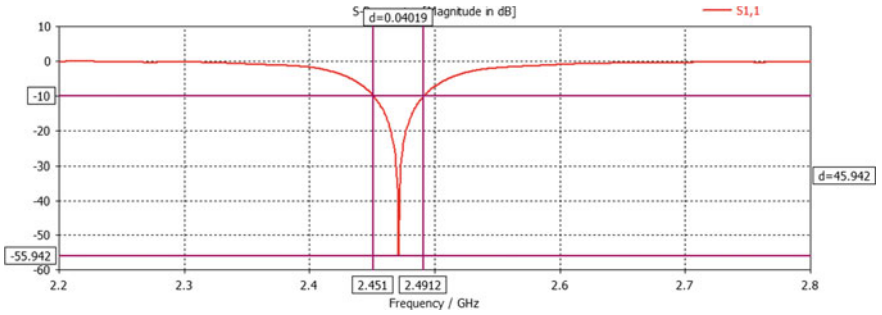


Fig. 7 Band width plot of simulated antenna

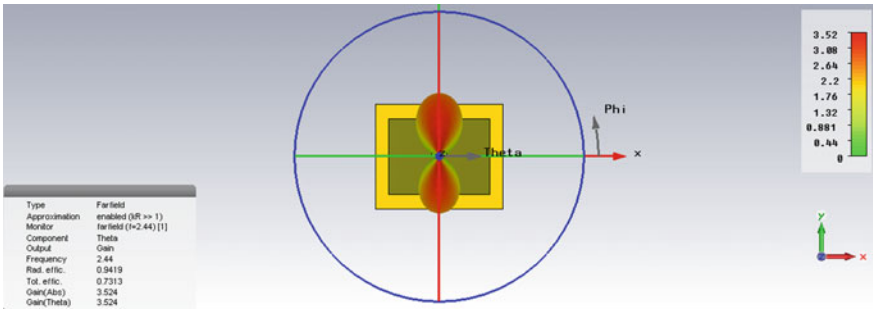


Fig. 8 Simulated antenna gain plot

VSWR of proposed antenna is very much closer to 1 which is shown in Fig. 3. VSWR is nothing but the ratio of maximum amplitude to the minimum amplitude of the standing wave. VSWR should be in between 1 and 2 for efficient operation of an antenna (Fig. 6). The bandwidth of 40 MHz which is covering the SHF range of RFID, i.e., 2.400–2.483 GHz. The bandwidth of the simulated antenna is shown in Fig. 7.

Figure 8 shows the gain plot of proposed antenna and the gain obtained is 3.524 dB. Gain is the ratio of radiation intensity in a given direction to the intensity that would be obtained if the power accepted by the antenna that were radiated isotropically.

5 Conclusion

This paper presents a Radio Frequency Identification (RFID) reader antenna which operates in Super High Frequency (SHF) range from 2.4 to 2.483 GHz with a bandwidth of 830 MHz. The proposed antenna consists of a small triangular slot embedded on the square patch which is designed on FR4 substrate material with dielectric constant value $\varepsilon_r = 4.3$. The 3D-EM Simulation Software called microwave CST is used for design and simulation. For the antenna performance analysis, parameters like return loss (s11), VSWR, and Gain are considered. The proposed antenna is operating at 2.471 GHz with a gain of 3.524 dB, good impedance matching with the microstrip line used for feeding (55.97 dB return loss) and VSWR is <2 and nearer to 1. The bandwidth of proposed antenna is 40 MHz which covers the SHF frequency band. The overall size of the antenna is 38.86 × 47.34 × 1.6 mm which is obtained from the Transmission Line Model. The proposed antenna is fabricated and tested using Vector Network Analyser. The obtained return loss for fabricated antenna is −15.4851 dB which is closer to the simulated results.

References

1. Bafshri, M.S.R., Ibrahmy, M.I., Motakabber, S.M.A.: Design of wide band inductively coupled loop fed patch antenna for UHF RFID Tag. Radio Engineering, vol(24). no.1. (April 2015).
2. Nazish Irfan, Musthapha, Yagoub, C. E., Khlifa Hettak.: Design of a microstrip line fed inset patch antenna for RFID applications, International Journal of engineering & technology (IACSIT) vol(4). No.5. (Oct 2012).
3. Dhrgham. K. Nagi, Jaber. Aziz, S., Road S Fyath.: Design & simulation of RFID aperture coupled fractal antennas, International Journal of engineering business management (INTECH) VOL(4). (2012).
4. Rajesh Kumar gangwar, Swathi singh & swetha agarwal, Design of an UHF RFID reader antenna, International journal of electronic and electrical engineering. vol(7). ISSN 0974-2174, PP 263-268, (2014).
5. PROTHRO, J. T., et al.: The effects of a metal ground plane on RFID tag antennas, In Proceedings of the IEEE Antennas and Propagation Society International Symposium, DOI:10.1109/APS.2006.1711302, (2006).
6. Satish Rama Chowdary, P., Mallikarjuna Prasad, A., Mallikarjuna Rao, P., Jaume Anguera.: Design and Performance Study of Sierpinski Fractal Based Patch Antennas for Multiband and Miniaturization Characteristics, Wireless Communications, Springer Science & Business Media New York (March 2015).
7. GHANNAY, N., et al. Effects of metal plate to RFID tag antenna parameters, In Proceedings of the Mediterranean Microwave Symposium 2009. Tangiers (Morrocco), p. 1–3. DOI:10.1109/MMS.2009.5409801, (2009).
8. TASHI, T., et al.: A complete planner design of microstrip patch antenna for a passive UHF RFID tag, In Proceedings of the 17th International Conference on Automation and ComputingICAC 2011. Huddersfield (UK), p. 12–17, (2011).

Design and Analysis of Modified Circular Patch Antenna with DGS for UWB Applications

Anjaneyulu Katuru and Sudhakar Alapati

Abstract In this paper, a planar monopole antenna with modified circular patch is presented. The proposed antenna is designed to operate from 2.75 to 13.53 GHz frequency range, which covers the whole ultra-wideband (3.1–10.6 GHz). The circular patch is metallized on a FR4 dielectric substrate with a relative dielectric constant of 4.3 and is truncated at its top which is opposite to the feedline. The substrate dimensions of the modified truncated circular patch antenna (MTCPA) are taken as 36 × 36 × 1.6 mm. This antenna is excited by a 50 Ω microstrip line. A defected ground structure (DGS) with a partial ground plane is printed on the back side of the substrate to obtain UWB characteristics. The proposed antenna yields return loss of less than −10 dB ($S_{11} < -10$ dB), VSWR < 2, and nearly omnidirectional radiation patterns. This antenna is designed and simulated in CST Microwave Studio. This antenna is a best suitable candidate for various UWB communication systems.

Keywords Monopole antenna · DGS · UWB · MTCPA · VSWR · Omnidirectional radiation patterns

1 Introduction

The low profile antennas such as microstrip antennas are having applications in the high-performance aircraft/spacecraft environment as well as the missile and satellite applications in which the antennas' size, weight, manufacturing cost as well as their ease of installation and their compatibility to aerodynamic profile are needed [1]. The antenna engineer encounters the challenge in designing a compact antenna with

A. Katuru (✉)
Department of ECE, Tirumala Engineering College, Narasaraopet, AP, India
e-mail: anjikaturu@gmail.com

S. Alapati
Department of ECE, RVR & JC College of Engineering, Guntur, AP, India
e-mail: alapati_sudhakar@yahoo.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_56

wide impedance bandwidth over its entire operating band of a UWB communication system. Several planar monopole radiating element variants such as square, rectangular, and circular with independent geometries have been characterized in [2, 3], moreover, in [4, 5] the techniques to enhance the impedance bandwidth were investigated. The UWB typically possesses a fractional bandwidth of more than 20% or greater than 500 MHz [6] according to FCC, typically facilitates the high data rate transmissions, and makes its field attentive by researchers for new antenna designs [7, 8]. The applications in radar, location tracking, and data transmissions are being carried out in the 3.1–10.6 GHz band, after the approval of FCC in 2002 [9]. The planar monopole radiators satisfy such requirements in addition to the advantages as mentioned above, they are providing omnidirectional radiation and wide impedance bandwidth with ease of fabrication on PCBs.

In this paper, a modified circular patch monopole antenna (MTCPA) with DGS for UWB applications is presented. Section 2 describes the design methodology with intermediate simulation results of different antenna design variants. The simulation results of the proposed antenna are discussed in Sect. 3 and concluded in Sect. 4.

2 Antenna Design

2.1 Conventional Circular Patch Antenna and Partial Ground Plane

The microstrip patch antennas with microstrip line feeding usually possess a sandwiching structure of substrate, radiating patch with feedline, and ground plane as major elements. Since their evolution, the radiating patch has been configured with various shapes such as square, rectangular, circular, and derived shapes such as elliptical, triangular, etc. Due to the ease of analysis, the circular patch is considered in this paper which allows good far-field performance with admirable low cross polarization. The patch is characterized with its radius represented with parameter 'r' = 14 mm and is printed on the substrate and a 50 Ω microstrip line is used to excite the patch antenna. The location of the feed has a wide freedom of choice along the circumference of the circular patch. Considering the above discussions, the circular patch is shown in Fig. 1a and the ground plane configuration is shown in Fig. 1b. The geometric parameters of the conventional circular patch antenna with partial ground plane are shown in Table 1.

The antenna is 3D modeled and simulated in CST Microwave Studio design environment. The simulation performance of the antenna is analyzed in the frequency sweep from 2 to 14 GHz and the results are plotted in terms of return loss and VSWR which are shown in Fig. 2a, b.

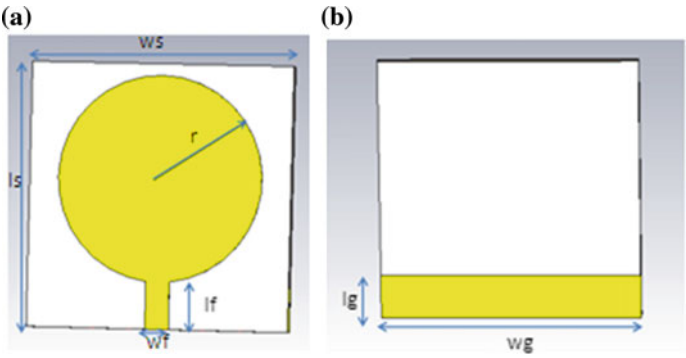


Fig. 1 Geometry of conventional circular patch antenna with partial ground plane **a** *front view* **b** *back view*

Table 1 Geometrical parameters of proposed antenna

Parameters	l_s	w_s	h	r	t_p	l_g	w_g	l_f	w_f	s_l	s_w	T_1
Value (mm)	*36*	36	1.6	14	0.1	6	36	6.6	3.2	4	3	20

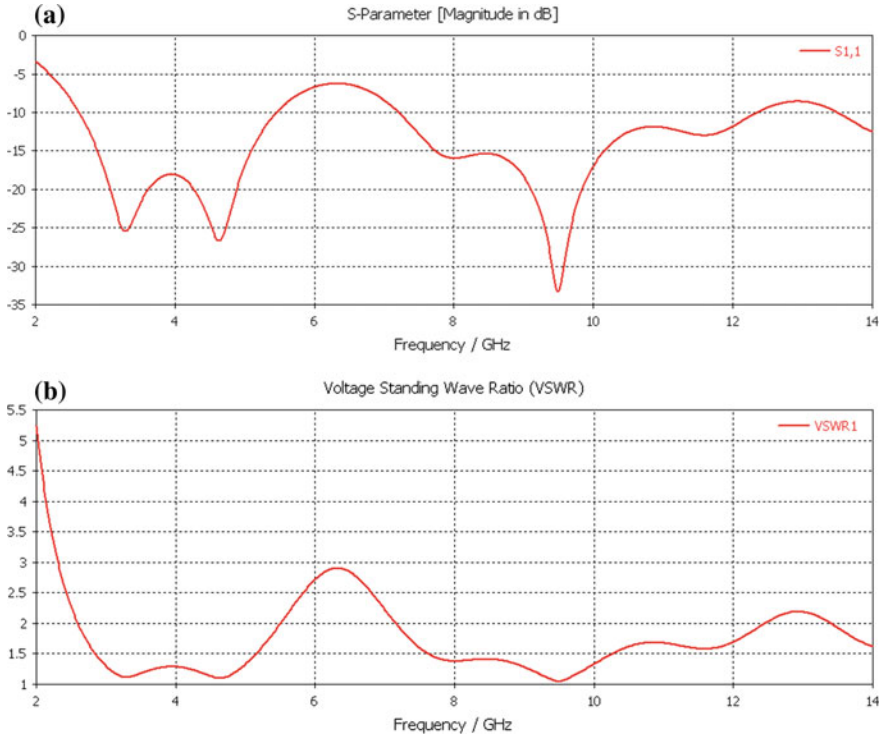


Fig. 2 Simulated results of conventional circular patch antenna with partial ground plane **a** return loss **b** VSWR characteristics

2.2 Truncated Patch Antenna with Partial Ground Plane

The geometry of conventional circular patch antenna discussed above is modified with truncated patch. The geometry of proposed monopole MTCPA is shown in Fig. 3 which is etched on FR4 substrate having relative permittivity 4.3 and with dimensions 36 × 36 × 1.6 mm. The circular patch is truncated from top side with $T_1 = 20$ mm length. A modified partial ground plane is printed on the backside of the substrate with 6 mm × 36 mm dimensions and a notch with 4 mm × 3 mm dimensions is etched in the ground plane to provide ultra-wideband (UWB) characteristics. A 50 Ω microstrip transmission line of width $w_f = 3.2$ mm and length $l_f = 6.6$ mm is used to excite the modified circular patch antenna. With the selection of appropriate antenna dimensions, the proposed antenna could obtain the return loss characteristics with ultrawide impedance bandwidth which shows a good impedance matching with the antenna port. The design parameters of the proposed MTCPA antenna are tabulated in Table 1.

The simulated results of truncated patch antenna in Fig. 3 computed in terms of return loss and VSWR with respect to frequency are shown in Fig. 4a and Fig. 4b, respectively.

In this case, the truncation of patch from the top side is very useful to support ultra-wideband characteristics. In Fig. 4a, the return loss is above −10 dB at 6.27 GHz, but comparing with the Fig. 2a the return loss is decreased due to truncation of the patch. By inserting truncation in the circular patch the antenna provides the band rejection characteristics. To eliminate the band rejection characteristics etching the slot in ground shown in Fig. 5.

2.3 Proposed Antenna Design

The antenna configuration shown in Fig. 3 is modified with some geometrical modification in the ground plane leads to a new design with enhanced

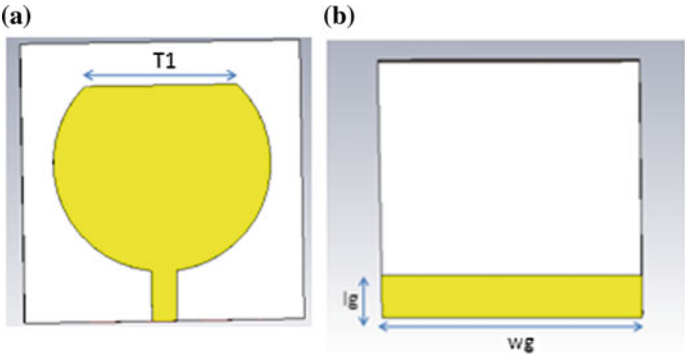


Fig. 3 Geometry of truncated circular patch with partial ground plane **a** *front view* **b** *back view*

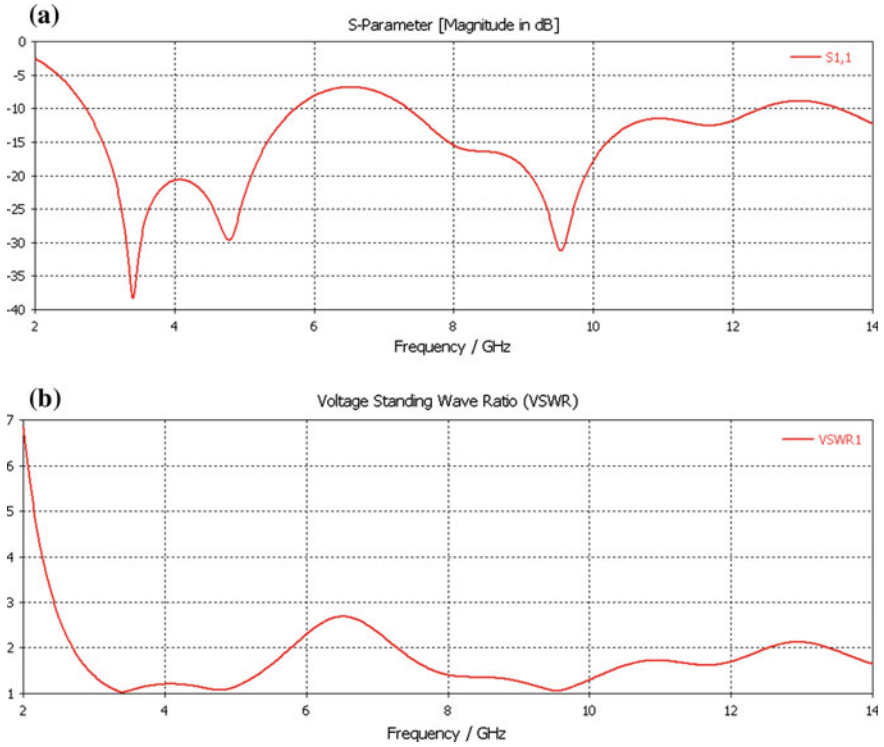


Fig. 4 **a** Simulated return loss **b** VSWR characteristics of truncated patch with partial ground plane

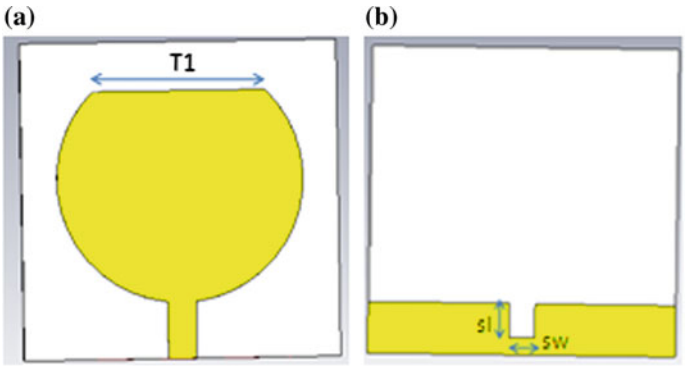


Fig. 5 Geometry of proposed antenna **a** *front view* with truncated circular patch **b** *back view* with ground plane etched with a notch

characteristics which is shown in Fig. 5. In this version, the antenna is obtained by truncating the circular patch from the top side of the patch and a notch of suitable

dimensions of 3 × 4 mm are etched in the partial ground plane. Therefore, the modified circular patch and notched partial ground plane yield the ultra-wideband (UWB) characteristics.

3 Results and Discussion

3.1 Simulated Return Loss and VSWR Characteristics of Proposed Antenna

The provision of a rectangular notch in the partial ground plane impacts the impedance matching and the better matching is provided at the 6 GHz frequency at which the decrease in return loss value below −10 dB is observed in the Fig. 6a, b the VSWR < 2 can be seen at the 6 GHz band where in initial designs the band rejection has occurred. Moreover, the S11 < −10 dB and VSWR < 2 have been maintained over a large bandwidth.

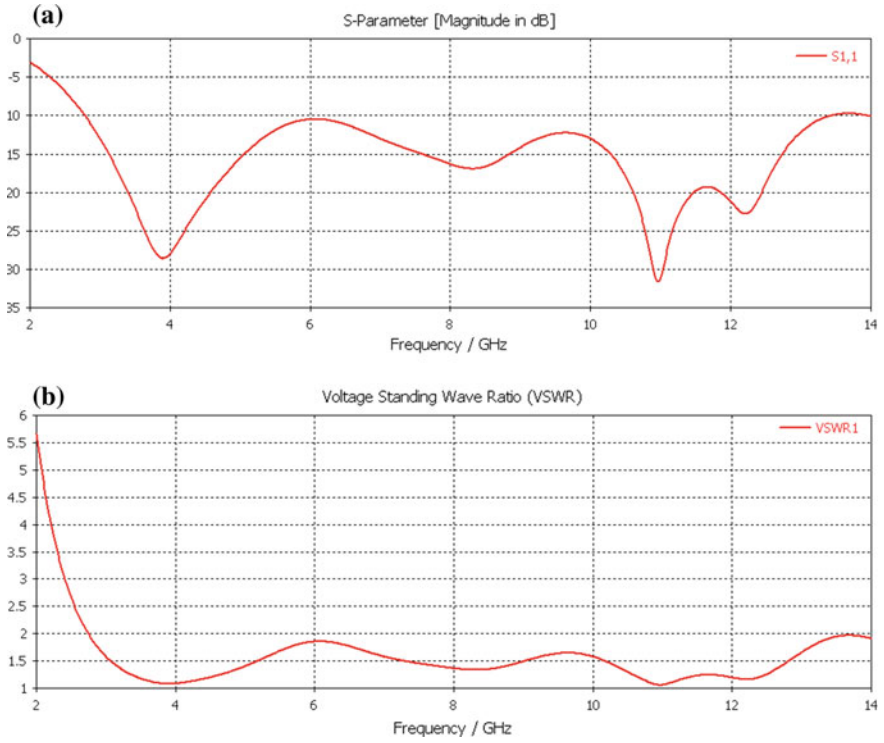
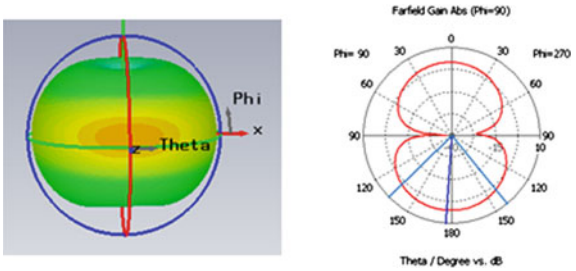


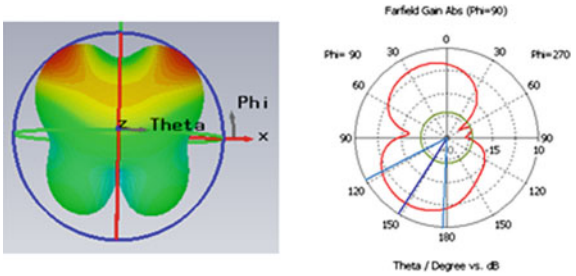
Fig. 6 Simulated results of **a** return loss **b** VSWR versus frequency characteristics of proposed antenna

Table 2 Frequency versus gain characteristics of the proposed antenna

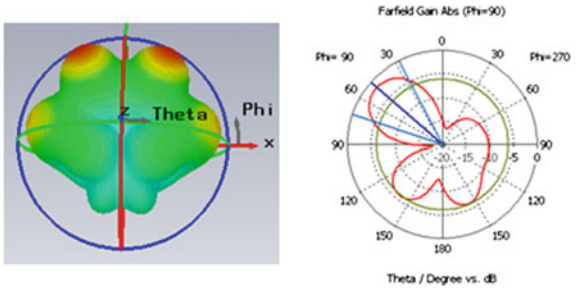
Frequency (GHz)	3.2	6.2	9.2	11.2
Gain (dB)	2.4	4.4	5.9	5.5



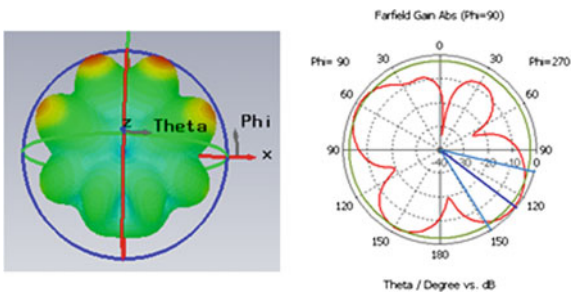
(a) at $f = 3.2$ GHz



(b) at $f = 6.2$ GHz



(c) at $f = 9.2$ GHz



(d) at $f = 11.2$ GHz

Fig. 7 Simulated three-dimensional (figures on the *left*) and two-dimensional (figures on the *right*) radiation patterns

3.2 3D and 2D Radiation Patterns of the Proposed Antenna

The radiation patterns of proposed antenna are simulated for selected frequencies with in the UWB range. Both 3D and 2D radiation patterns are obtained for the frequencies 3.2, 6.2, 9.2, and 11.2 GHz. The antenna gains for the corresponding frequencies are listed in Table 2. The patterns obtained are nearly omnidirectional and are almost similar over the UWB range which means that there is a consistent response over the entire UWB range. The 3D and 2D radiation patterns are shown in Fig. 7.

4 Conclusion

In this paper, the design and simulation of a planar modified circular patch monopole antenna is proposed and supported with the 3D modeling and analysis using CST Microwave Studio. The proposed antenna observed is operated in the UWB spectrum that covers 3.1–10.6 GHz. The truncated circular patch geometry along with the partial ground DGS structure etched with a rectangular notch ensures good impedance matching throughout the band. The proposed antenna exhibits the return loss well below −10 dB and VSWR < 2 for the frequency range of interest. The far-field patterns of the proposed antenna in 2D planar and three-dimensional configurations are also investigated. Further, the study of current distribution and its effect on validation characteristics would be good scope of future work. The fabrication of the proposed antenna and measurements carried on it would be a better mode to validate the antenna geometry furthermore. This antenna may be proved a suitable candidate for various futuristic ultra-wideband communication systems.

References

1. Balanis, C.A.: Antenna Theory: Analysis and Design. 2nd Edition. John Wiley & Sons, New York, 1997.
2. Ojaroudi, M., Yazdanifard, S., Ojaroudi, N., Moghaddasi, M.N.: Small Square Monopole Antenna With Enhanced Bandwidth by Using Inverted T-Shaped Slot and Conductor-Backed Plane. In: IEEETrans. Ant. and Propag. 59(2), 670–674. Feb (2011).
3. Mobashsher, A.T., Islam, M.T., Misran, N.: Wideband compact antenna with partially radiating coplanar ground plane. In: Appl. Comput. Electromagn. Soc. 26(1), 73–81. Jan (2011).
4. Jung, J., Choi, W., Choi, J.: A compact broadband antenna with an L-shaped notch. In: IEICE Tran. Commun. E89-B(6), 1968–1971. Jun (2006).
5. Jung, J., Choi, W., Choi, J.: A small wideband microstrip-fed monopole antennas. In: IEEE Microw. Lett. 15(10), 703–705. Oct. (2005).
6. Chen, C.H., Liu, C.L., Chiu, C.C., Hu, T.M.: Ultra-wideband channel calculation by SBR/image techniques for indoor communication. In: J. Electromagn. Waves and Appl. 20(1), 41–51. (2006).

7. El-Fishawy, N., Shokair, M., Saad, W.: Proposed Mac protocol verses IEEE 802.15.3a for multimedia transmission over UWB networks. In: Prog. In Electromagn. Res. B (PIER B) 2, 189–206. (2008).
8. Stroh, S.: Ultrawideband: Multimedia unplugged. In: IEEE Spectrum. 24, Sep. (2003)
9. Anon: FCC first report and order on Ultrawideband technology. Feb. (2002).

Design of Microstrip Transition to Substrate Integrated Waveguide Fed Slot Antenna for 60 GHz Applications

M. Nanda Kumar and T. Shanmuganantham

Abstract Substrate integrated waveguide is a good candidate for implementing millimeter wave applications. This paper presents microstrip transition to substrate integrated waveguide fed slot antenna for 60 GHz applications, which is developed by Rogers RT/Duroid 5880 with a dielectric constant of 2.2, substrate height of 0.381 mm and metallization thickness is 0.025 mm. The simulation results show that reflection coefficient, VSWR, gain, radiation efficiency, and radiation pattern. Obtained 3.1 GHz impedance bandwidth with respect to −10 dB reflection coefficient and also preserve 44.28% bandwidth over 57–64 GHz band.

Keywords Waveguides · Substrate integrated waveguide (SIW) · Wireless LAN (WLAN) · Printed circuit board (PCB) · Giga bit wireless (GIFI)

1 Introduction

The evolution of millimeter wave range 30 GHz to higher than 100 GHz [1] is critical evaluation of communications and has attracted increasing attention from industry and academia applications, i.e., wireless communication networks (60 GHz) [2, 3] automotive radar systems (79 GHz) [4], passive millimeter wave imaging (94 GHz), and biomedical applications. For this, investigation on high-gain and broadband antenna has attracted growing attention in last decades.

Federal communication commission (FCC) was assigned in 57–64 GHz band (7 GHz) to access unlicensed devices and noted that the spectrum would be suitable for short range, high data rates (multi-gigabits per second), and broadband applications such as wireless computer to computer applications. Due to high bandwidth, this band is attracted toward GIFI, WLAN, and also automotive applications.

M. Nanda Kumar (✉) · T. Shanmuganantham
Department of Electronics Engineering, Pondicherry University, Puducherry, India
e-mail: nanda.mkumar12@gmail.com

T. Shanmuganantham
e-mail: Shanmuga.dee@pondiuni.edu.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_57

For high-frequency applications, microstrip lines are not suitable due to smaller wavelength and require very high tolerance. Next preferred device for high-frequency application is waveguide [5] but its manufacturing process is difficult due to small wavelength.

Substrate integrated waveguide (SIW) [6, 7] is another technology which is suitable to overcome problems that occurred in rectangular waveguide and implemented in millimeter applications, driven by a family of substrate integrated circuits (SICs) [8]. SIW are integrated waveguide-like structure fabricated by using two periodic rows of metallic holes or vias joining the top and bottom ground planes of a dielectric substrate and shown in Fig. 1. This is very standard due to their simple design, printed circuit board process (PCB) [9], or other planar processing techniques used for fabrication due to low cost, possibility to mount one, or more chipsets in single substrate. For RF design, the concept system in package (SiP) is used and extended to the system-on-substrate (SoS) [10]. It is an ideal platform for development due to high performance, low cost, and ease of fabrication.

Compare to microstriplines and planer lines, SIW fabrication process is very easy, compact in size, cost effective, and low weight [11]. Also compared to metallic waveguide, it has high power handling, high quality factor, and low interference due to its complete shielding [12]. SIW's main advantage is integrated in planar form which contains active components, passive components, and antennas.

Slot antenna is attracted for wireless applications due to low profile, easy amalgamation with planar circuits, and improved isolation from feed network [13]. A simple short end waveguide is generally called as cavity backed slot antenna and used to improve broad bandwidth and low profile [14, 15].

SIW slot antenna is entirely realized by multilayered PCB structure, generated by two rows of vias connecting top and bottom ground planes. SIW cavity backed bowtie antenna is used for broadband applications [16].

This paper is structured as follows. First, Sect. 2 defines antenna architecture and design. Second, Sect. 3 summarizes the results. Finally, conclusion is given in Sect. 4.

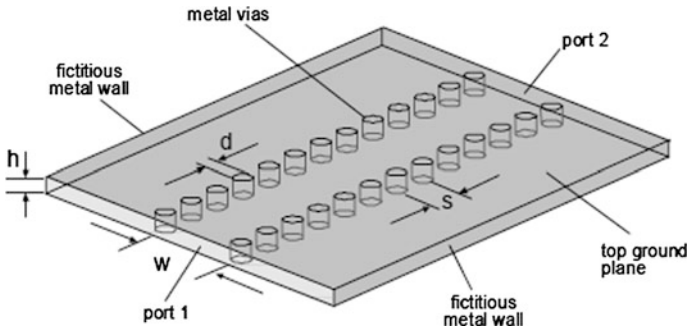


Fig. 1 Substrate integrated waveguide

2 Antenna Architecture and Design

For high-frequency applications, a new concept of substrate integrated circuits (SICs) is introduced, which yields high performance [17] and used to assimilate nonplanar threedimensional structures within a multilayer structure. SIW is a type of transmission line, designed mainly for millimeter and centimeter wavelength applications. SIW is driven from rectangular waveguide, dominant mode of rectangular waveguide TE_{10} and the dielectric filled rectangular waveguide width is

$$a_R = \frac{1}{2*f_c*\sqrt{\in_R}} \tag{1}$$

where a_R is the width of dielectric filled rectangular waveguide and **c** is the light speed. The width of SIW also depends on d as well as s, as given in Eq. (2) [18].

$$a_R = a_S - \frac{d^2}{0.95s} \tag{2}$$

To maintain loss free radiation between metallic vias, It is must satisfy the following equation [19].

$$d \leq \frac{\lambda_g}{5} \tag{3}$$

and

$$s \leq 2d, \tag{4}$$

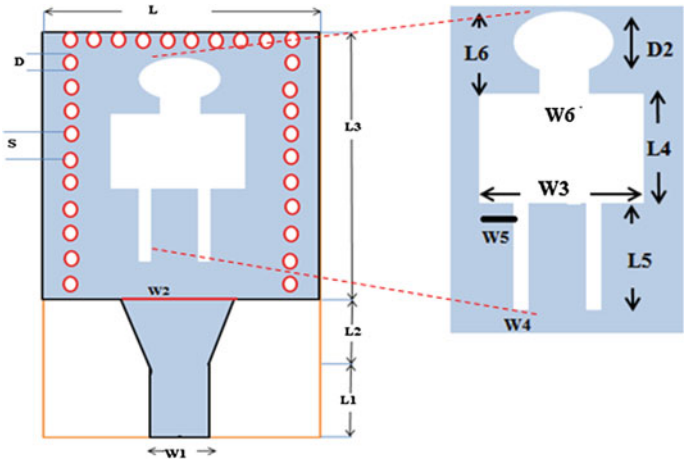


Fig. 2 Proposed antenna design

Table 1 Optimized parameters

Parameters	Dimensions (mm)	Parameters	Dimensions (mm)
h	0.381	L6	W6 + D/2
Asiw	5	W1	0.653
D	0.1	W2	2.2
S	0.15	W3	2.8
L1	2.75	W4	0.3
L2	5.85	W5	0.5
L3	10.5	W6	0.9
L4	2.5	t	0.025
L5	3	D2	0.5

where s is space between two holes, d is diameter of metal holes, and λ_g is guided wavelength.

The design of proposed antenna is shown in Fig. 2 were designed for 60 GHz frequency applications and designed using Rogers RT/Duriod with $\in_r = 2.2$ height of 0.381 mm and Table 1 shows the optimized parameters for designing of an antenna.

3 Simulation Results

The structure was designed with the help of Rogers RT/Duriod, where $\in_r = 2.2$ and substrate thickness is 0.381 mm. Electromagnetic tool Computer Simulation Technology Studio Suite is used for simulation of the proposed antenna. Figure 3 demonstrates the frequency versus reflection coefficient in between the frequency range 57–64 GHz and achieves 3.1 GHz (between 59.268 and 62.368 GHz) impedance bandwidth with respect to −10 dB reference line, and occupies the 44.28% bandwidth of entire band. Two resonant frequencies are obtained from Fig. 3 and their return loss values are −19.302 dB at 59.86 GHz and −24.149 dB at 61.6 GHz.

Compared to Refs. [1, 18], the proposed antenna size is small, and it achieves more bandwidth with respect to −10 dB reference line and gain is average.

Figure 4 shows the voltage standing wave ratio for above simulated antenna, also achieves around 3.1 GHz bandwidth with respect to VSWR (2:1), and also it is observed that VSWR is 1.243 at 59.86 GHz and 1.1322 at 61.6 GHz.

Figure 5 demonstrates the radiation efficiency of proposed antenna and observed that 92.25% at 60 GHz and 93.1% at 62 GHz. Figure 6 expresses the 3D gain pattern for different frequencies (60 and 62 GHz) and can be observed that the main lobe direction is along broadside (z-axis) and gains are 8.01 dBi, 7.54 dBi at 60, and 62 GHz frequencies and that frequency is inversely proportional to gain. Figure 7 demonstrates the E-plane and H-plane patterns for different frequencies, i.e., 60 and 62 GHz.

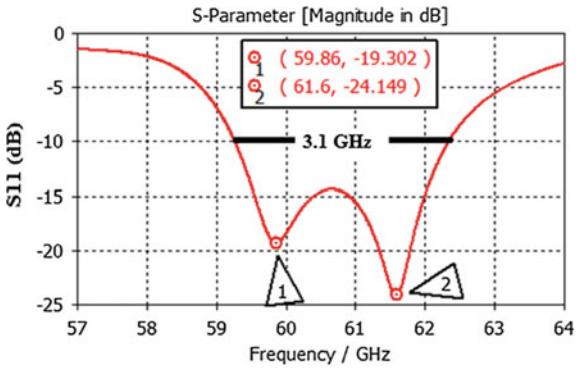


Fig. 3 Reflection coefficient versus frequency

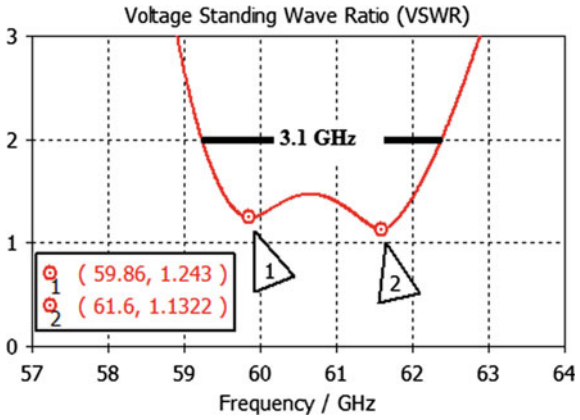


Fig. 4 Voltage standing wave ratio (VSWR)

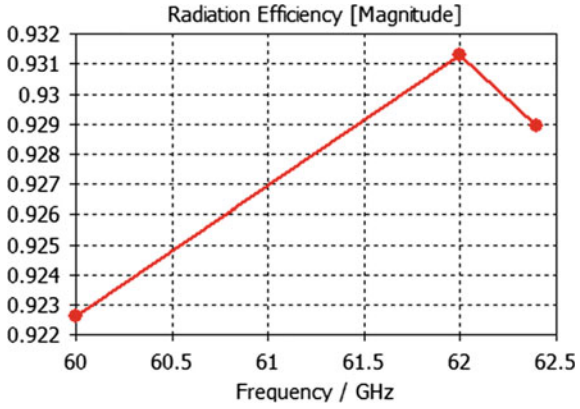


Fig. 5 Radiation efficiency

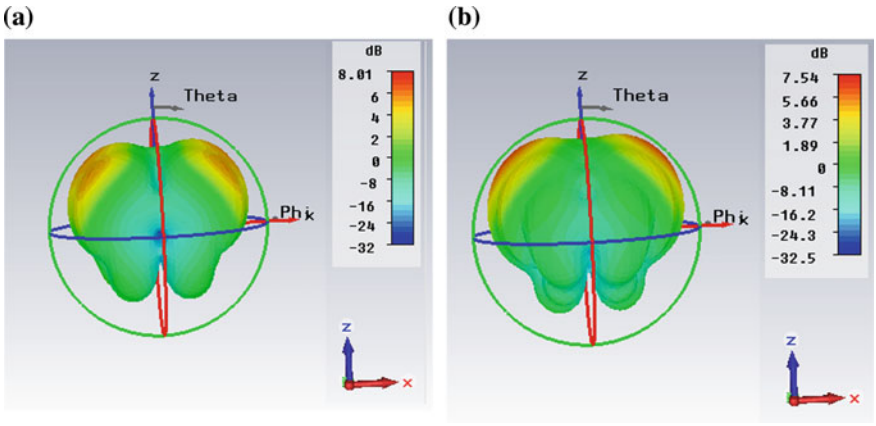


Fig. 6 3D Gain patterns **a** 60 GHz **b** 62 GHz

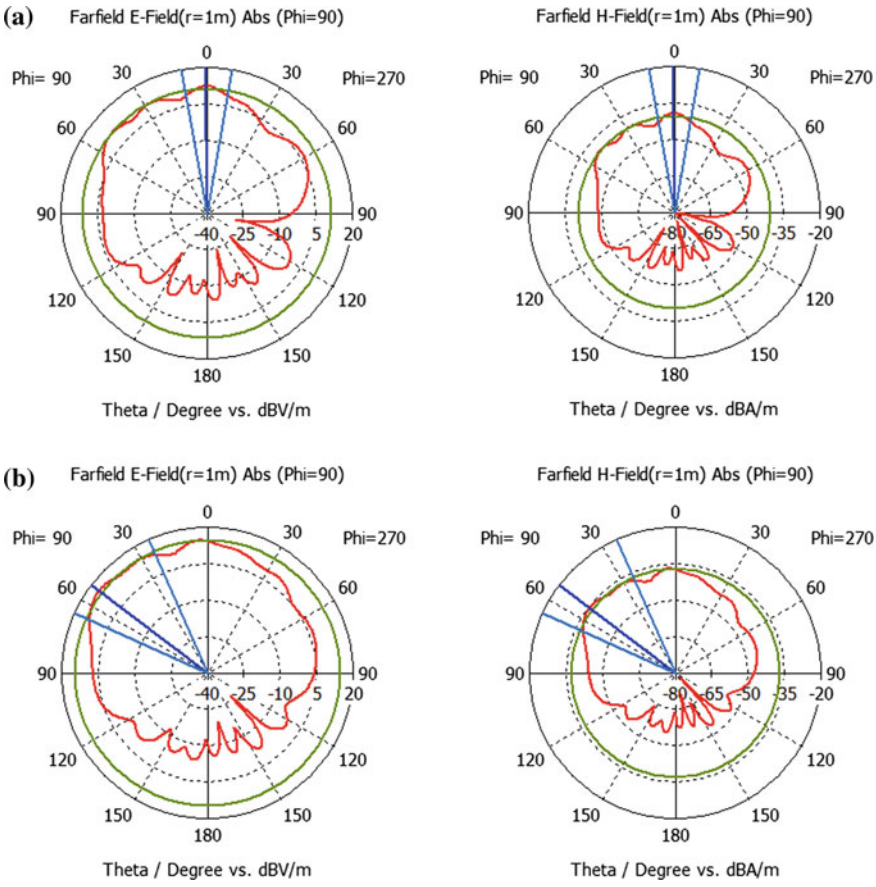


Fig. 7 2D E-plane (*left*) and H-plane (*right*) radiation patterns **a** 60 GHz **b** 62 GHz

4 Conclusion

This paper presented the design of microstrip transition to substrate integrated waveguide fed slot antenna for 60 GHz applications and achieved 3.1 GHz bandwidth respect to reflection coefficient ($S_{11} \leq -10$ dB), VSWR (2:1) and return losses are -19 dB at 60 GHz, -24.171 dB at 61.59 GHz. It preserves 44.28% bandwidth of entire band and also observes gain, radiation efficiency, and radiation patterns. The proposed antenna is used for high data rate applications like GIFI, WLAN, and automotive applications due to large bandwidth. This antenna covers the distance of 10 m.

Acknowledgements Authors are very grateful to DEITY Scheme (Visvesvaraya Ph.D Fellowship) for assisting financial support to do the research work.

References

1. Lockie, D., Peck, D.: High Data Rate Millimeter Wave Radios. IEEE Microwave Magazine. 10(5), 75–83 (2009).
2. Shrivastava, P., Rao, T. R.: Performance Investigations with Antipodal Linear Tapered Slot Antenna on 60 GHz Radio Link in a Narrow Hallway Environment. Progress in Electromagnetics Research. 58, 69–77 (2015).
3. Yujian, L., Kwai, M.L.: Low Cost High Gain and Broadband Substrate Integrated Waveguide Fed Patch Antenna Array for 60 GHz Band. IEEE Transactions on Antennas and Propagation. 62(11), 5531–5538 (2014).
4. Junfeng, X., Zhi N.C., Xianming, Q.: CPW Center-Fed Single-Layer SIW Slot Antenna Array for Automotive Radars. IEEE Transactions on Antennas and Propagation. 62(9), 4528–4536 (2014).
5. John, W.D., Caroline, E.M., Geoff, M.P., Brian, M.T., Silas, H., John, W.B., Martyn, J. C., Roger, D.P., Robert, E.M., Paul, S.D., Steve, R.D.: Fabrication and Characterization of Micro-machined Rectangular Waveguide Components for use at Millimeter-Wave and Terahertz Frequencies. IEEE Transactions on Microwave Theory and Techniques. 48(8), 1293–1302(2000).
6. Maurizio, B., Luca, P., Ke, W., Paolo, A.: Current and Future Research Trends in Substrate Integrated Waveguide Technology. Radio Engineering. 18(2), 201–207 (2009).
7. Xu, F., Wu, K.: Guided-wave and Leakage Characteristics of Substrate Integrated Waveguide. IEEE Transactions on Microwave Theory and Techniques. 53(1), 66–73, (2005).
8. Bozzi, M., Georgiadis, A., Wu, K.: Review of Substrate Integrated Waveguide Circuits and Antennas. IET Microwave Antennas Propagation. 5, 909–920 (2011).
9. Shi, C., Hanna, Y., Henrik, K.: 79 GHz Slot Antennas Based on Substrate Integrated Waveguides in a Flexible Printed Circuit Board. IEEE Transactions on Antennas and Propagation. 57(1) (2009).
10. LI, Z., Wu, K.: 24-GHz Frequency Modulation Continuous-Wave Radar Front-end System on Substrate. IEEE Transactions on Microwave Theory and Techniques. 56(2), 278–285(2008).
11. Cheng, Y.J., Hong, W., Wu, K.: Multimode Substrate Integrated Waveguide H-plane Monopulse Feed. Electronics Letters. 44(2) (2008).
12. Zhang, X.C., Yu, Z.Y., J. Xu.: Novel Band Pass Substrate Integrated Waveguide (SIW) Filter Based on Complementary Split Ring Resonators (CSRRS). Progress in Electromagnetic Research. 72, 39–46 (2007).

13. Guo, Q.L., Zhi, F.H., Lin, X.D., Ling, L.S.: Planar Slot Antenna Backed by Substrate Integrated Waveguide Cavity. IEEE Antennas and Wireless Propagation Letters. 7, 236–239 (2008).
14. Guo, Q.L., Zhi F.H., Wen J.L., Xiao H.Z., Ling, L.S., Jian F.Z.: Bandwidth Enhanced Low Profile Cavity Backed Slot Antenna by using Hybrid SIW Cavity Modes. IEEE Transactions on Antennas and Propagation. 60(4) (2012).
15. Guo, Q.L., Zhi, F.H., Yaping, L., Li, Y.Y., Ling, L.S.:Development of Low Profile Cavity Backed Crossed Slot Antennas for Planar Integration. IEEE Transactions on Antennas and Propagation.57(10) (2009).
16. Soumava, M., Animesh, B., Kumar V.S.: Broadband Substrate Integrated Waveguide Cavity-Backed Bow-Tie Slot Antenna. IEEE Antennas and Wireless Propagation Letters. 13, 1152–1155 (2014).
17. Deslandes, D., Wu, K.: Single-substrate Integration Technique of Planar Circuits and Waveguide Filters. IEEE Transactions on Microwave Theory and Techniques. 51(2), 593–596 (2003).
18. Ramesh, S., Rao, T.R.: Planar High Gain Dielectric Loaded Exponentially Tapered Slot Antenna for Millimeter Wave Wireless Communications. Wireless Press Communication, Springer. 3179–3192 (2015).
19. Deslandes, D., Wu, K.: Accurate Modeling, Wave Mechanisms, and Design Considerations of a Substrate Integrated Waveguide. IEEE Transactions on Microwave Theory and Techniques. 54(6), 2516–2526 (2006).

Band-Notched Circular Serrated Wideband Antenna

D.S. Ramkiran, P. Siddaiah and B.T.P. Madhav

Abstract This letter investigates the performance improvement of coplanar waveguide fed (CPW) circular antenna with the addition of serrated structure in the radiating element. Antenna is providing a huge bandwidth of 13 GHz with an impedance bandwidth of 61% in the operating band. By placing U-shaped slots on the feed line, dual-band notch characteristics in the X-band are achieved. The proposed antenna is occupying a compact dimension of 30 × 30 × 1.6 mm on FR4 substrate with dielectric constant 4.3 and loss tangent 0.025. Prototyped antenna measured results on ZNB 20 VNA are in good agreement with simulated results of CST.

Keywords Circular patch · Computer simulation technology (CST) · Serrations · Notch · Wideband · X-Band

1 Introduction

Wideband and UWB antennas are gaining their importance in the modern communication systems with numerous applications. The selection of a particular antenna for given application is determined by mechanical, electrical constraints, and operating costs [1, 2]. The mechanical parameters are important for size, reliability, weight and manufacturing process, etc. The electrical parameters are frequency of operation, radiation pattern, impedance, gain, polarization, etc. [3–5]. Today antennas find extensive use in military and commercial application like

D.S. Ramkiran (✉)
Department of ECE, JNTUH, Hyderabad, Telangana, India
e-mail: ramkiranduvvuri@kluniversity.in

P. Siddaiah
Department of ECE, Acharya Nagarjuna University, Guntur, AP, India

D.S. Ramkiran · B.T.P. Madhav
Department of ECE, K L University, Guntur, AP, India
e-mail: btpmadhav@kluniversity.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_58

radar, biomedicine, remote sensing, astronomy, air traffic control, GPS, WLAN, collision avoidance, etc.

Depending on the frequency of operation, different applications are raised in the communication domain. In the microwave region, L-band is generally used for long rang surveillance and remote sensing applications, S, C-bands for weather detection and long-range tracking and X-band for satellite communication and missile guidance [6–8]. Depending on the application, one should design an antenna either frequency independent or dependent. While retaining the antenna parameters, the designers should focus on the reduction of the antenna size and weight to fit the modal according to present-day communication technology. In some cases, the unwanted frequency in the operating band should be blocked for designed operation [9].

The demand for broadband antennas that are capable of supporting high data speeds and multiband operation of modern wireless communication systems has significantly increased. Planar antennas are playing important roles in various wireless communication applications owing to unique merits such as same volume or low profile, low manufacturing cost, and easy integration in to planar circuits [10–12].

The present work initially deals with the design and analysis of broadband antennas with good impedance, bandwidth, and gain. To block a particular band of frequencies, a modified structure of modern antenna with serrated radiating element and notching characterizes a slotted section in the feed line is proposed in this work. The design of proposed antenna with different iteration is clearly prescribed in the antenna geometry section. The modeling is done with CST and simulation is carried with FDTD method.

2 Antenna Geometry

Three antenna models are designed in this work for broadband communication applications. The basic model is constructed with circular patch element on FR4 substrate and a coplanar wave guide feeding is used in the design and it can be observed from Fig. 1a. The circular radiating patch element is modified by placing triangular serrated elements as shown in Fig. 1b. The triangular serrated in the radiating element provided different directions for the current elements and affected the impedance bandwidth of the antenna as well as gain. Figure 1c shows the notch band circular serrated antenna with U-shaped slotted elements on the feed like to block certain range of frequencies in the X-band (Fig. 2).

The complete dimensions of the antenna iterations are presented in Table 1. The overall dimension of the antenna is around $30 \times 30 \times 1.6$ mm which is very compact in these kinds of antennas. The proposed structures are constructed on FR4 substrate material with dielectric constant 4.4 and loss tangent 0.025.

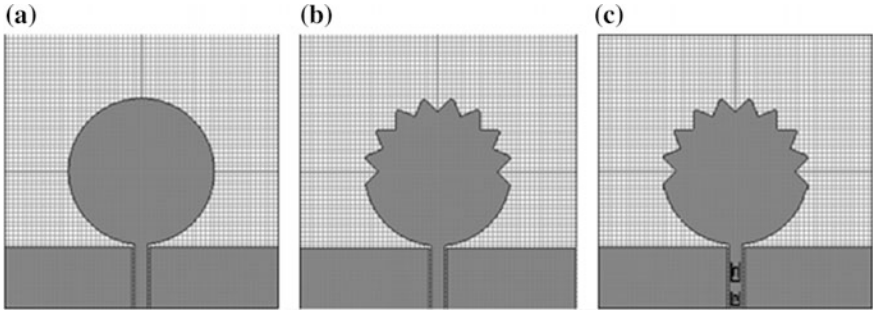


Fig. 1 Antenna geometry. **a** Circular antenna. **b** Circular serrated antenna. **c** Circular serrated antenna with U-slots

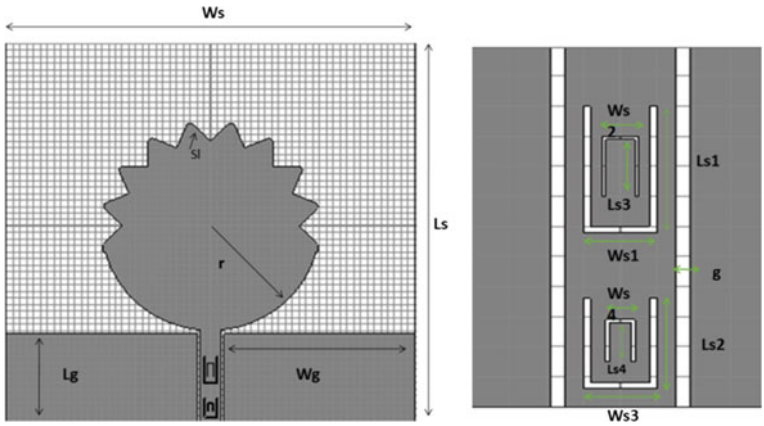


Fig. 2 Proposed circular serrated notch band antenna with U-slots

Table 1 Series-fed array antenna design parameters

Parameter	Dimensions in mm	Parameter	Dimensions in mm
Ls	30	Ls_3	1.9
Ws	30	Ls_4	1.3
Lg	13.5	Ws_1	1
Wg	28.1	Ws_2	0.5
R	16	Ws_3	0.8
S1	3.6	Ws_4	0.4
Ls_1	4.2	g	0.2
Ls_2	2.8		

3 Results and Discussion

The designed antenna models are simulated using CST-Microwave studio and presented in this section. Figure 3 shows the reflection coefficient of the coplanar waveguide fed circular antenna. The designed basic antenna is providing bandwidth of 13 GHz and impedance bandwidth of 46% in the operating band. A modified structure with triangular serrated boundary on the circular patch is providing similar bandwidth but an improvement in the impedance bandwidth of 61% can be observed from Fig. 4.

Modified structures with U-shaped slots are created in the circular serrated model to get the notch band characteristics in the antenna. The proposed antenna is notching two bands in the X-band (Band 1: 9–10.2 and Band 2: 10.8–12.4 GHz). By placing slots in the feed line in the inverted fashion, the notch bands occurred in the wideband antenna. Figure 5 shows the evidence for the notch band characteristics in the proposed antenna.

The complete behavior of the antenna can be analyzed with its radiation characteristics. Figures 6, 7, 8, 9, 10, 11, and 12 show the radiation patterns of the antenna in the passband and stopband. Figure 6 shows the radiation pattern of the

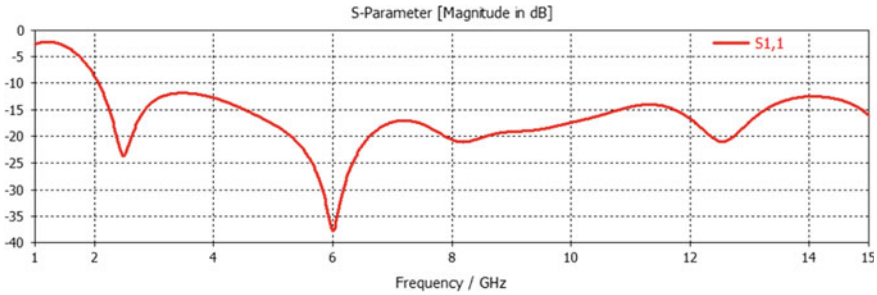


Fig. 3 Reflection coefficient of CPW-fed circular antenna

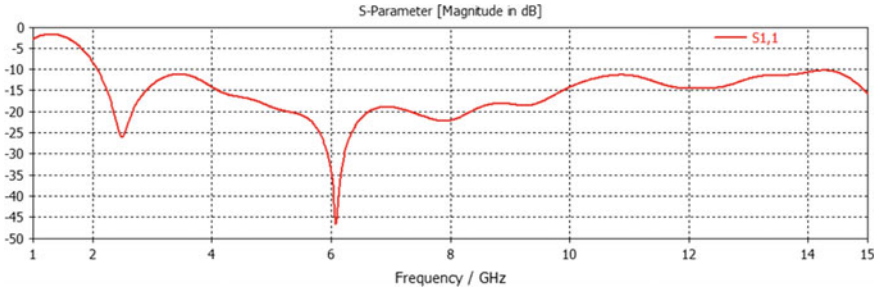


Fig. 4 Reflection coefficient of circular serrated antenna

basic circular antenna in the operating band at 2.5, 6, and 10 GHz. At lower operating band, antenna is showing monopole-like radiation and at higher frequency it is like quasi-omnidirectional. At center frequency, antenna is showing directional radiation pattern from Fig. 6. Antenna gain is also high at higher operating frequencies compared to lower operating frequencies from Fig. 7.

Similar kind of radiation patterns are observed for the case of serrated antenna and notch band antenna at operating band. Three-dimensional radiation pattern curves of serrated antenna from Fig. 9 show gain of 5.17 dB at higher operating

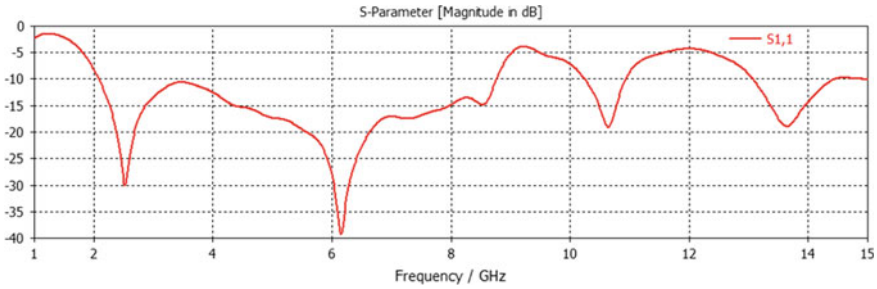


Fig. 5 Reflection coefficient of circular serrated notch band antenna

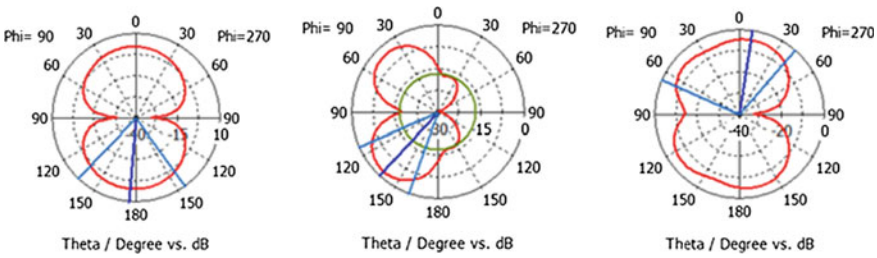


Fig. 6 Radiation pattern of circular antenna at 2.5, 6 and 10 GHz

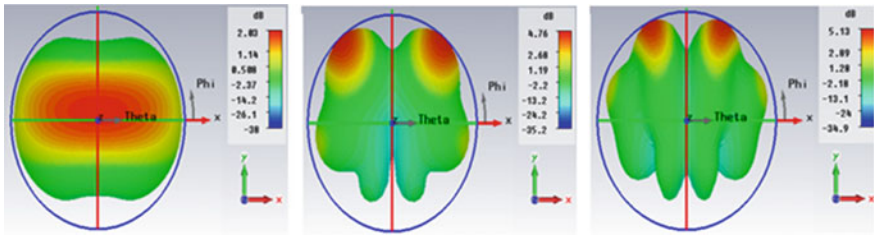


Fig. 7 Three-dimensional radiation pattern of circular antenna at 2.5, 6 and 10 GHz

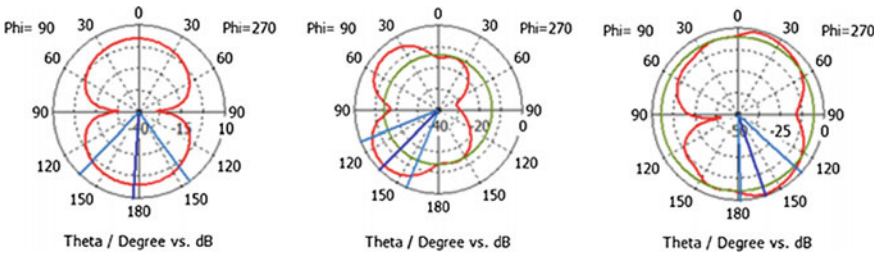


Fig. 8 Radiation pattern of circular serrated antenna at 2.5, 6 and 10 GHz

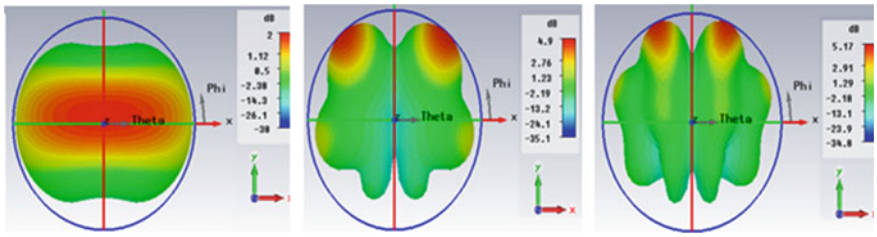


Fig. 9 Three-dimensional radiation pattern of circular serrated antenna at 2.5, 6 and 10 GHz

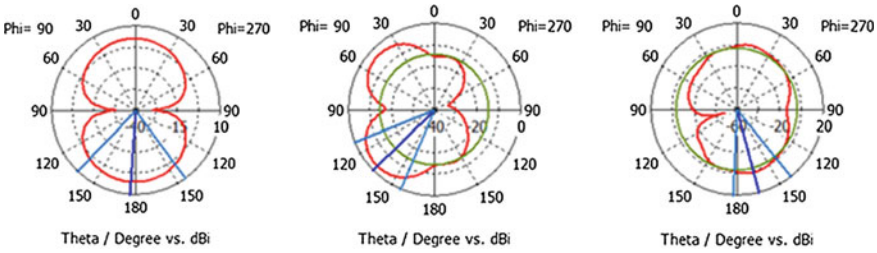


Fig. 10 Radiation pattern of proposed circular serrated notch band antenna at 2.5, 6 and 10 GHz

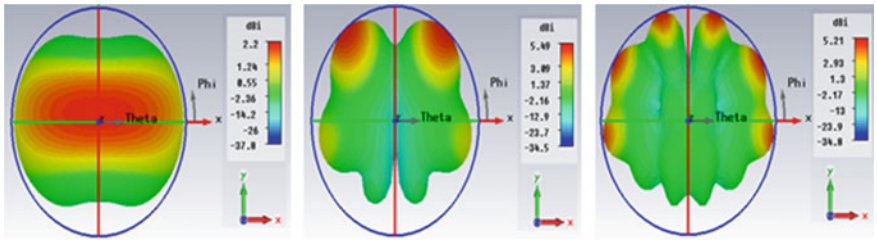


Fig. 11 Three-dimensional radiation pattern of proposed circular serrated notch band antenna at 2.5, 6 and 10 GHz

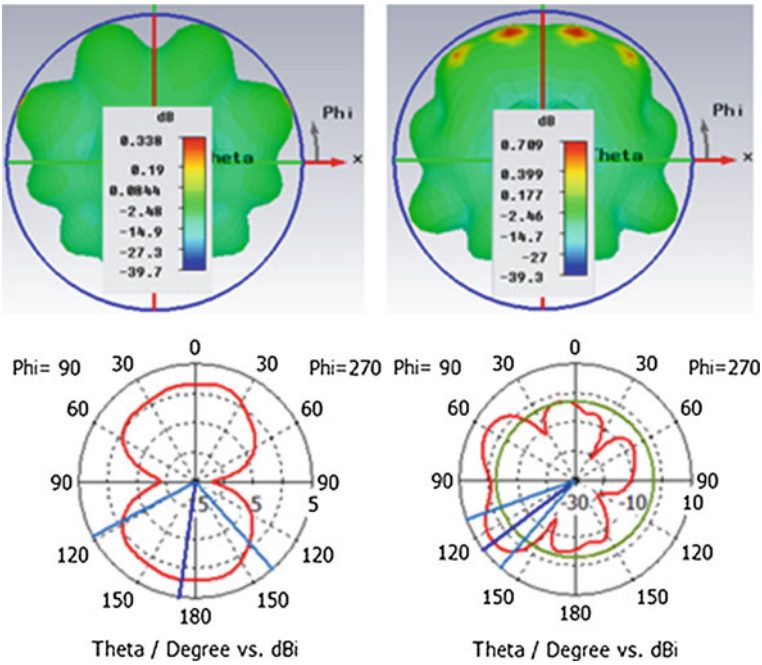


Fig. 12 Radiation pattern of proposed antenna at notch band frequencies 9 and 12 GHz

frequency and minimum of 2 dB at lower operating frequency. Figure 11 gives the gain of 5.21 at 10 GHz and 2.2 dB at lower operating frequency 2 GHz.

Radiation pattern at notch band can be observed from Fig. 12. The antenna radiation pattern is disturbed at notch band and showing poor gain at those frequencies. The surface current distribution of the model 1 and model 2 at different operating bands and at notch band for the proposed model is shown in Fig. 13. At notch band, the current density around both notches is equal in magnitude but opposite in polarity, so the net radiation will be canceled. The proposed antenna

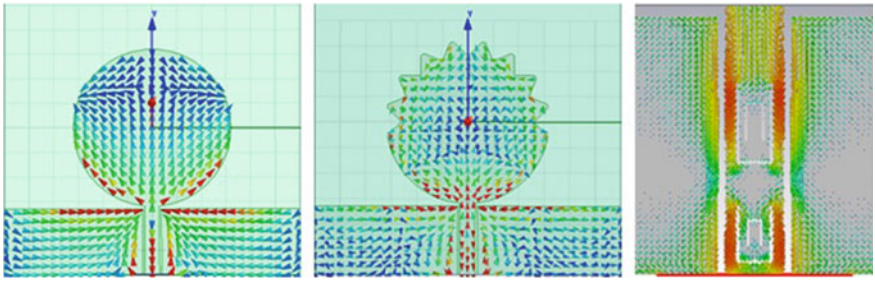


Fig. 13 Surface current distribution of model 1 and 2 at 6 GHz and model 3 at 12 GHz

Fig. 14 Fabricated antenna on FR4 Substrate and its measured result on ZNB 20 VNA

model is fabricated on FR4 substrate and photograph is provided in Fig. 14. The measured result of the proposed notch band antenna is also provided in Fig. 14 and it is showing similar kind of characteristics that are obtained from CST tool.

4 Conclusions

A novel compact serrated notch band antenna is designed and its parameters are analyzed in this work. The serrated radiating element is providing better impedance bandwidth of 50%, when compared with normal circular radiating patch element of impedance bandwidth 46%. A peak realized gain of 5.17 dB and directivity of 5.67 dB is obtained from circular serrated antenna. The proposed notch band circular serrated antenna is providing dual notch band characteristics in the X-band with peak gain of 0.3 and 0.7 dB at notch band frequencies. A peak realized gain of 5.4 dB and directivity of 5.86 is obtained from notch band antenna at its operating band. The proposed notch band antenna measured results on ZNB 20 vector network analyzer is providing good correlation with simulated results and showing evidence for the applicability of the antenna in the desired communication applications.

Acknowledgements Authors like to express their gratitude toward the department of ECE of K L University, Department of ECE of ANU College of Engineering and Department of ECE of JNTUH for their encouragement and support during this work. We would like to acknowledge the DST through grant ECR / 2016/000569.

References

1. Behdad, N., and Sarabandi, K.: A multiresonant single-element wideband slot antenna. In: IEEE Antennas Wireless Propag. Lett., 3(11). 5–8. (2004).
2. Jianxin, L., Chiau, C. C., Chen, X., and Parini, C. G.: Study of a printed circular disc monopole antenna for UWB systems. In: IEEE Trans. Antennas Propag., 53(11). 3500–3504. (2005).

3. Huang, C. Y., and Hsia, W. C.: Planar ultra-wideband antenna with a frequency notch characteristic. In: Microw. Opt. Technol. Lett., 49(2). 316–320. (2007).
4. Madhav, B. T. P., Manikanta Prasanth, A.: Analysis of Defected Ground Structure Notched Monopole Antenna. In: ARPN Journal of Engineering and Applied Sciences, ISSN 1819-6608, 10(2). 747–752 (2015).
5. Gao, Y., Ooi, B. L., and Popov, A. P.: Band-notched ultra-wideband ring-monopole antenna. In: Microw. Opt. Technol. Lett., 48(1). 125–126 (2006).
6. Madhav, B. T. P., Harish Kaza, A.: Novel Printed Monopole Trapezoidal Notch Antenna with S-Band Rejection. In: Journal of Theoretical and Applied Information Technology, ISSN: 1992-8645, 76(1). 42–49 (2015).
7. Ramakrishna, T. V et al.: Triple Band linearly polarized Square Slotted Micro strip Antenna for X – Band Applications. In: Far East Journal of Electronics and Communications, ISSN: 0973-7006, 15(2). 99–110 (2015).
8. Ram Kiran, D. S., Madhav, B. T. P.: Novel compact asymmetrical fractal aperture Notch band antenna. In: Leonardo Electronic Journal of Practices and Technologies, ISSN 1583-1078, 27 (2). 1–12 (2015).
9. Lakshmi, M. L. S. N. S et al.: Novel Sequential Rotated 2x2 Array Notched Circular Patch Antenna. In: Journal of Engineering Science and Technology Review, ISSN: 1791-2377, 8(4). 73–77 (2015).
10. Lee, W. S., Kim, D. Z., Kim, K. J., and Yu, J. W.: Wideband planar monopole antennas with dual band-notched Characteristics. In: IEEE Transactions on Microwave Theory and Techniques, 54(6). (2015).
11. Li, C. M., and Ye, L. H.: Improved dual band-notched UWB slot antenna with controllable notched bandwidths. In: Progress In Electromagnetics Research, 115. 477–493 (2011).
12. Wang, M. F., Xiao, J.-X., and Wang, S. W.: Study of a dual-band notched wideband circular slot antenna. In: Journal of Electromagnetic Waves and Applications, 24. (2010).

Design and Analysis of Slot-Coupled Cylindrical Dielectric Resonator Antenna Array

Kiran Jagadam, Sudheer Kumar Terlapu and R.L.V.N. Srinivasa Raju Gorantla

Abstract Dielectric resonators have emerged as potential candidates for multiband application. These resonators' performance has been explored with a variety of geometrical shapes to make use of the inherent resonant features to form a dielectric resonator antenna (DRA) high gain and directional cylindrical DRA (CDRA) array structure is illustrated using commercial software, HFSS. The typical antenna is simulated and analysed using powerful electromagnetic modelling tools. The reports generated are essential for analysing the performance.

Keywords CDRA · Return loss · Slot feed · Radiation pattern · Array · HFSS

1 Introduction

The dielectric layer of a planar patch antenna typically possesses unique radiation characteristics. These characteristic emphasizes the resonant features inherently existing with it. The radiating system that captivates these resonant features is called dielectric resonant antenna (DRA). The typical function of the DRA constitutes of formation of standing waves by the radiation which is impinged into the resonant cavity using conventional circuit. After the formation of sustained standing waves, the resonant fields escape into the free space through the walls which are partially transparent electromagnetic radiation. One of the advantages with DRA is that, the

K. Jagadam (✉) · S.K. Terlapu · R.L.V.N.S.R. Gorantla
Department of Electronics and Communication Engineering, Shri Vishnu Engineering College for Women (A), Bhimavaram, West Godavari District, AP, India
e-mail: jagadamkiran@gmail.com

S.K. Terlapu
e-mail: skterlapu@gmail.com

R.L.V.N.S.R. Gorantla
e-mail: hodece@svecw.edu.in

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_59

losses due to conducting walls in conventional antenna are avoided. This also enhances the efficiency [1, 2].

Since its first proposal during 1939 [3], the antenna drew the attention of antenna engineers in designing radiating system for sever defence and RADAR applications. In the due course of time, the geometry with different shapes like triangle, rectangular, circular, and spherical is proposed and successfully verified for several applications [3–13].

The shape of a DR can be cylindrical [8], rectangular [4], or hemispherical [6]. Hemispherical DR is chosen because of the simple spherical interface between itself and free space. The simple structure requires no magnetic wall. Impedance [13] was reported and the analysis was limited to the frequencies around the resonance of the TE_{111} mode. In this paper, a rigorous treatment of a probe fed hemispherical DR antenna, cylindrical DR are presented.

The paper is organized as follows. In Sect. 2, antenna design geometry and design procedure are discussed. Analysis and simulation results of antenna are discussed in Sect. 3. Finally conclusions and future scopes are given in Sect. 4.

2 Antenna Design Geometry

Description of the proposed antenna geometry, dimension, and other specification is discussed in this section as follows.

2.1 Cylindrical DRA 2 × 2 Array Antenna Design

Figure 1 shows the schematic of CDRA fed by a parallel microstrip feed network.

The top view and side view of the CDRA are shown in Fig. 2 and Fig. 3, respectively. Instead of full ground plane, partial ground plane has been used which provides better impedance matching of the antenna by reducing back reflection.

Typical dimension of the proposed CDRA and its array configuration are listed in the Table 1.

2.2 Antenna Design Using HFSS

These designs were simulated by using HFSS electromagnetic simulator. HFSS software is used to determine the characteristic of the designed antenna.

The general steps in an HFSS simulation:

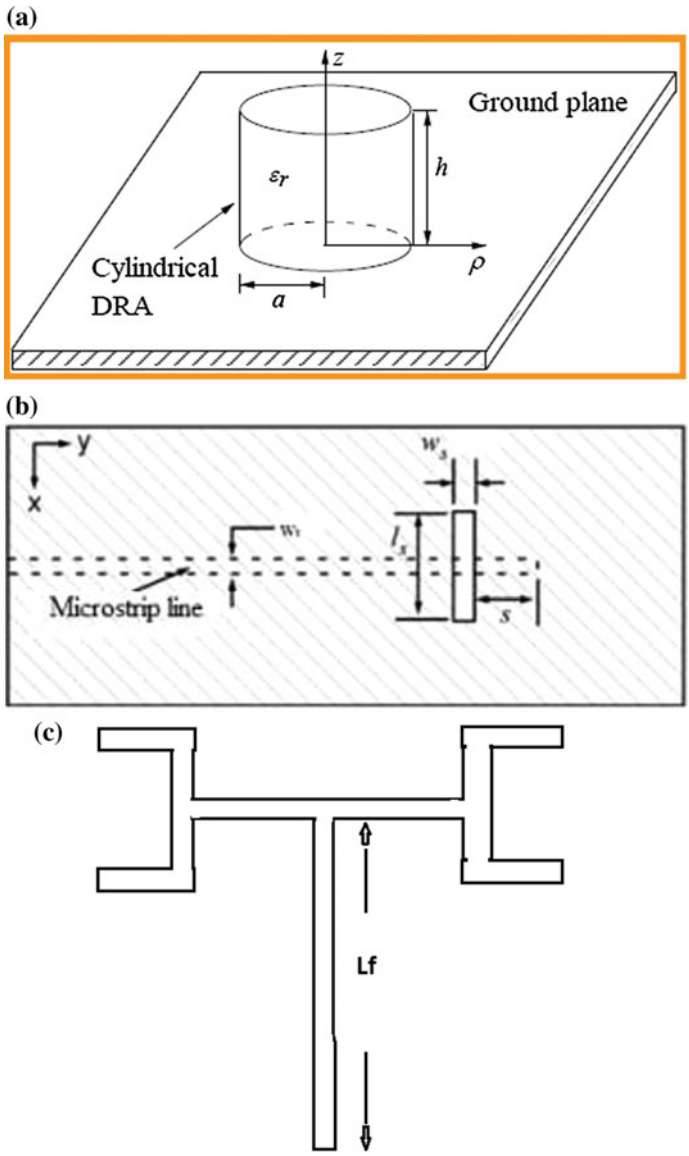


Fig. 1 Geometry of the proposed antenna. **a** Single cylindrical DRA. **b** Microstrip slot feed. **c** Parallel microstrip feed network

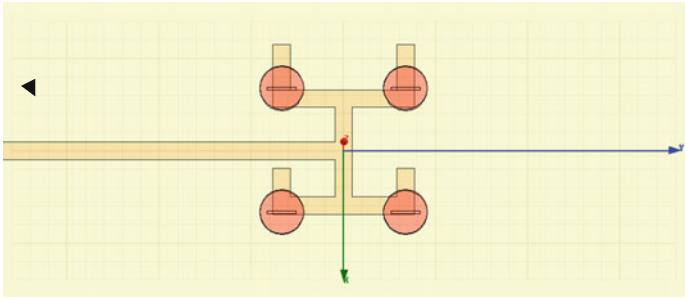


Fig. 2 Top view of cylindrical DRA 2 × 2 array

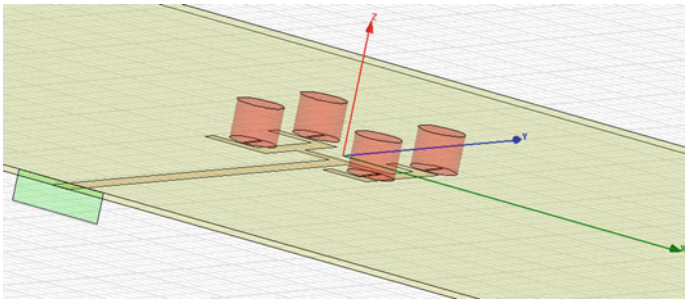


Fig. 3 Active view of cylindrical DRA 2 × 2 array

Table 1 Dimensions of CDRA

Dimensions (mm) (f0 = 6 GHz, εr = 20, loss tangent = 0.0025)		CDRA dimensions (mm)
DR	Radius (a)	5.96
	Height (h)	9.82
Ground plane	Length	300
	Width	300
	Thickness	1.57
Substrate (Rogers RT/durioid 5870 εs = 2.33, loss tangent = 0.0012)	Length	300
	Width	300
	Thickness	1.57
Slot	Length	8
	Width	0.8
Microstrip line	Length	38.3
	Width	4.7

3 Antenna Simulation Results

The simulation of the antenna is carried out in the HFSS tool using the methodology mentioned in Fig. 4. The typical dimension from Table 1 is considered while modelling the design in the embedded CAD tool in HFSS. The analysis of the antenna is carried out using the radiation parameters and reports like reflection coefficient (S_{11}), voltage standing wave ratio (VSWR) and radiation patterns.

3.1 Return Loss (S11 dB) Simulation Characteristics

Figure 5 shows the simulated return loss (S-parameter) for CDRA array. For the case of height of DR h = 9.82 mm, the desired resonant frequency at 6 GHz and 7.4 GHz is achieved.

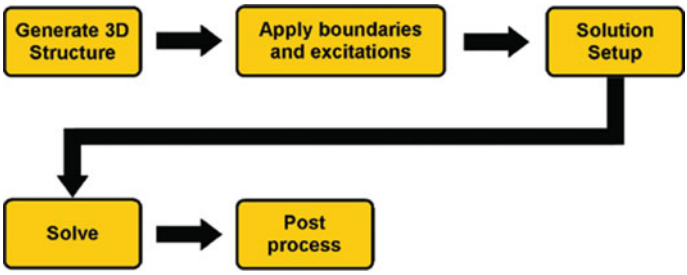


Fig. 4 HFSS simulation process

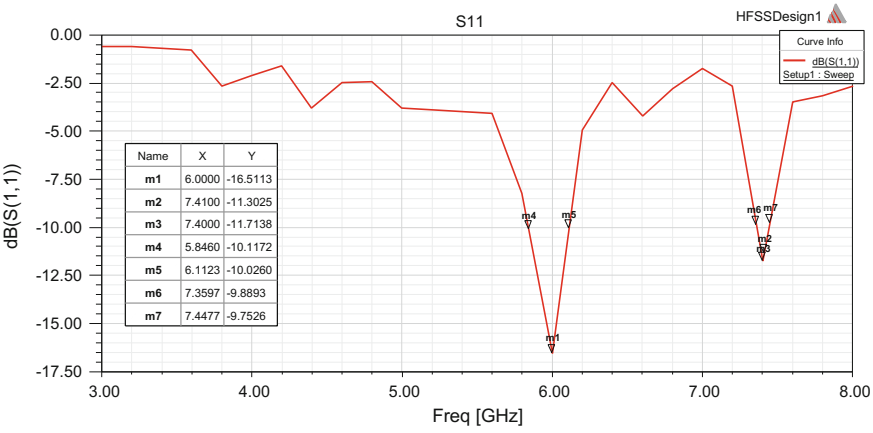


Fig. 5 Return loss (dB(S11)) versus frequency (GHz) of CDRA array

3.2 VSWR Characteristics

Figure 6 shows the simulated VSWR for CDRA array. For the case of height of DR h = 9.82 mm, the desired resonant frequency at 6 GHz and 7.4 GHz is achieved.

Furthermore, the value of VSWR for CDRA is approximately 1 at resonant frequencies Fig. 6. Figure 7 shows the gain versus frequency plot of CDRA.

The simulated plots are analysed and obtained values of return loss and VSWR are listed in Table 2 as follows.

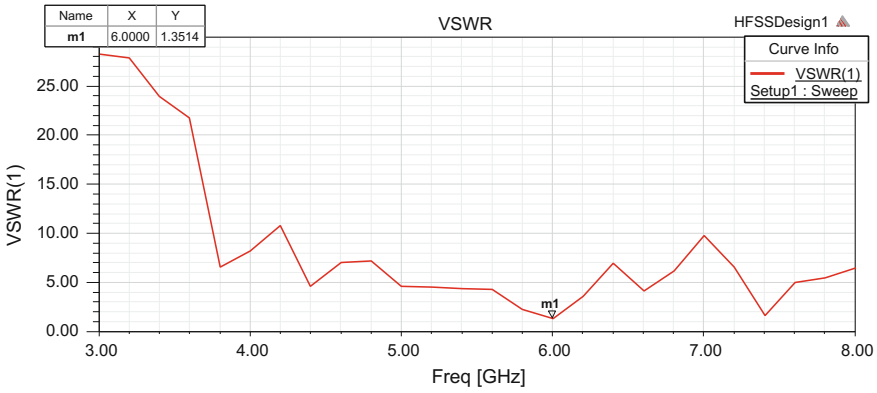


Fig. 6 VSWR versus frequency (GHz) of CDRA array

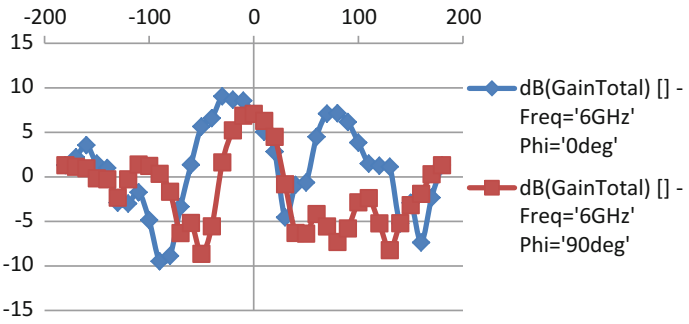


Fig. 7 Gain dB of CDRA array

Table 2 Simulation results of CDRA

Resonance frequency (GHz)	Return loss (dB)	Gain (dB)	VSWR	Bandwidth (%)
6	−16.51	9.05	1.31	27
7.4	−11.72	8.58	1.45	9

3.3 Radiation Pattern Characteristics

Both the 2D polar plots and 3D patterns are generated and presented as shown in Fig. 8 through Fig. 10. The plots are drawn at one of the resonant frequency identified as 6 GHz from the S_{11} and VSWR plots.

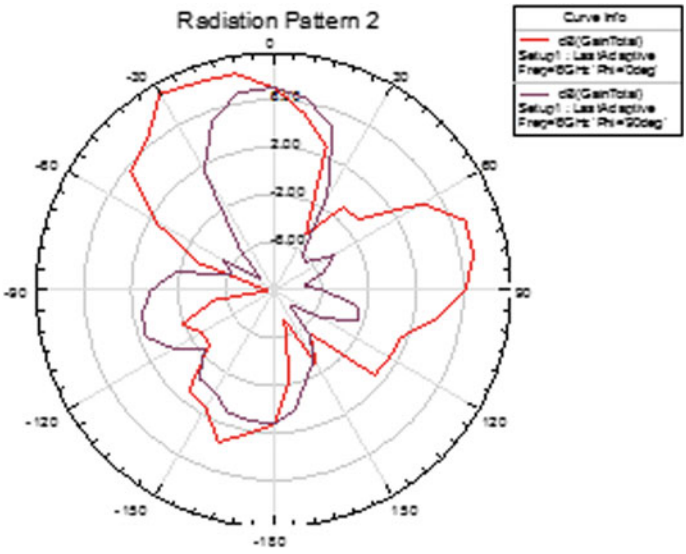


Fig. 8 Radiation pattern of CDRA array at E-plane, H-plane

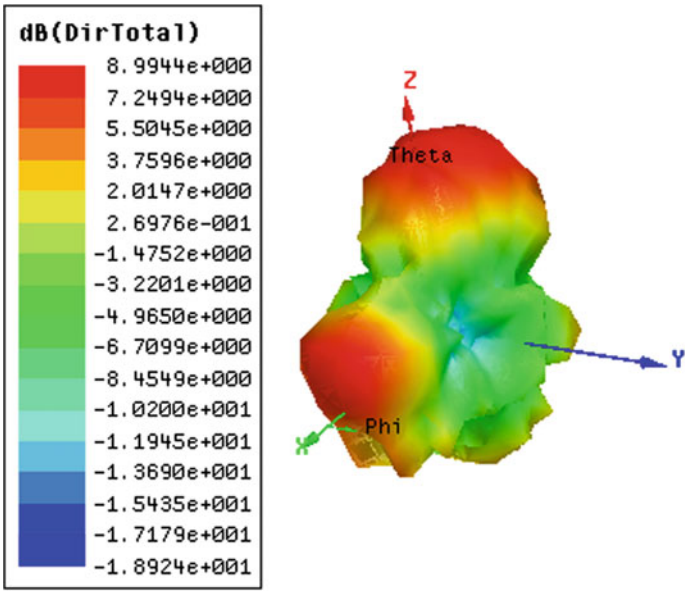


Fig. 9 3D far field radiation pattern (directivity) of CDRA array

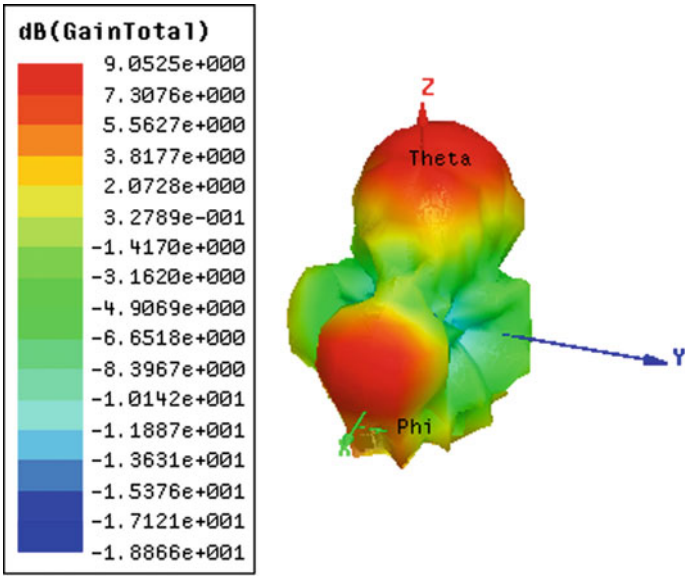


Fig. 10 3D far field radiation pattern (gain) of CDRA array

4 Conclusion

A four-element CDRA array is designed. The simulated results show the designed antenna that covers the frequency range from 5.84 to 6.11 GHz and 7.36 to 7.11 GHz. This elevates the multiband characteristics of the antenna.

It also shows the gain values of 9.05 dB at 6 GHz, and 8.58 dB at 7.4 GHz. The antenna significantly meets the standards of Wimax 5.8 GHz band.

References

1. Mongia, R. K., Bhartia, P.: "Dielectric Resonator Antennas – A Review and General Design Relations for Resonant Frequency and Bandwidth", International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering, 4, (3), pp 230–247, (1994).
2. Luk, K. M., Leung, K.W.: "Dielectric resonator antennas", Baldock, Hertfordshire, England: Research Studies Press Ltd, (2003).
3. Petosa, A.: "*Dielectric resonator antennas Handbook*", Artech House Inc., (2007).
4. Baghaee, R.M., Neshati, M.H., Mohassel, J.R.: "Rigorous analysis of rectangular dielectric resonator antenna with a finite ground plane", *IEEE Transaction on Antenna and Propagation*, Vol. 56, No. 9, 2801–2809, Sept. (2008).
5. Aras, M.S.M., Rahim, M.K.A., Rasin, Z., Abdul Aziz, M.Z.A.: "An Array of Dielectric Resonator Antenna for wireless application," IEEE International RF and Microwave Conference Proceedings, pp. 459–463, (Dec 2008).

6. McAllister, M. W., Long, S.A.: "Resonant hemispherical dielectric antenna," *IEEE Transactions on Antenna and Propagations*, vol. 31, pp. 406–412. (1983).
7. Reena Kumari and Ravi Kumar Gangwar "Circularly Polarized Dielectric Resonator Antennas: Design and Developments," Journal: Wireless Personal Communications, 2016, Volume 86, Number 2, Page 851.
8. HFSS: "*High Frequency Structure Simulator Based on Finite Element Method*", V.11, Ansoft Corporation.
9. Kranenburg, R. A., Long, S.A.: "Microstrip Transmission Line Excitation of dielectric resonator antennas," *IEEE Electronics Letters*, Vol. 24, No. 18, pp. 1,156–1,157, (Sept 1988).
10. Mongia, R. K., et al.: "A Half-split Cylindrical Dielectric Resonator Antenna Using Slot Coupling," Microwave and Guided Wave Letters, Vol. 3, No. 2, pp. 38–39, (Feb. 1993).
11. Al Salameh, M. S., Antar, Y. M. M., Seguin, G.: "Coplanar-Waveguide-Fed Slot-Coupled Rectangular Dielectric Resonator Antenna," *IEEE Transactions on Antennas & Propagation*, Vol. 50, No. 10, pp. 1,415–1,419, (Oct. 2002).
12. Nikkhah, M. R., Kishk, A. A.: "Compact and wideband dielectric resonator antenna," in Antennas and Propagation & USNC/URSI National Radio Science Meeting, 2015 IEEE International Symposium on, vol., no., pp. 450–451, (July 2015).
13. Nikkhah, M. R., Kishk, A. A., Rashed-Mohassel, J.: "Wideband DRA Array Placed on Array of Slot Windows," in Antennas and Propagation, IEEE Transactions on, vol. 63, no. 12, pp. 5382–5390, (Dec. 2015).

Designing a Low-Power Generator Circuit with Switching Theory for Power Reduction

G. Rohith, P. Dhanunjaya Rao, P. Prasanth, A. Lakshmi Deepika and R. Hari Gopalkrishna

Abstract Testing the VLSI circuits is the major aspect to know the parameter variations at different stages. For the self-testing of the circuits, we introduce a suitable structure which can be used for testing the VLSI designs. The structure is built in such a way that the objective of the generator is highly utilized for the power dissipation reduction which does not affect the functionality and the fault coverage. The SOC system approach is established to implement the Altera FPGAs with soft-core processor. This proposed implementation verifies the power test which shows the significant percentage variation.

Keywords VLSI testing · FPGA · Fault coverage

1 Introduction

The demand for the portable computing devices and the communication system are rapidly increasing. The main challenging areas in the VLSI family is bond with some features like performance, cost, area power and reliability. The applications run on different power consuming issues in VLSI circuits can be noted in [1].

P. Dhanunjaya Rao · R. Hari Gopalkrishna
Department of ECE, Raghu Engineering College, Visakhapatnam, AP, India
e-mail: dhanupaila.dp@gmail.com

R. Hari Gopalkrishna
e-mail: harigopalakrishnarudra@gmail.com

G. Rohith (✉) · P. Prasanth · A. Lakshmi Deepika
Department of ECE, Pydah College of Engineering & Technology,
Visakhapatnam, AP, India
e-mail: rohithguntu@gmail.com

P. Prasanth
e-mail: prasanth.paladugula454@gmail.com

A. Lakshmi Deepika
e-mail: deepikahymavathi944@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_60

The complex designs of embedded SOC are well fabricated with more than one processor, memory, interface, and component with accelerating different tasks. The main proceeding of designing the SOC is the platform-based. Xilinx Virtex II Pro and Altera are the examples of platform FPGAs which include the custom designs with processor cores and of reconfigurable logic systems. SOPC is one of the development tools that enable IP cores to be integrated and custom components or blocks with the Nios II which is one of the soft-core processors. The flexibility is high in soft-core processors when compared with the hard-core processors in a application optimizations. But, power dissipation is one of the big problems in SOCs designing and testing. As mentioned in [2, 3], there are some reasons for this problem in the test mode and it also requires high power dissipation than the normal mode. The reasons are

- Nature of testing reflects to the high switching activity.
- At a time the internal cores lead to the parallel activation.
- High integration involvement in the DFT circuitry which consumes much of the power utilization.
- The test vectors resulting in Low correlation.

The high-power utilization creates instantaneous power surge which creates the damage of the circuit and hot spots formations. It is very difficult to verify the performance and reduce the products field and the life time [4]. Hence, the high power ratings are noticed while testing the applications. There are many methods that are introduced previously to overcome this issue. The methods include the algorithms for scheduling minimum power, power reduction techniques, and power reductions while scan testing and the BIST methods. On-chip communications are more faster than the off-chips. The design for the testability is the proposed technique to minimize the required time for the parameter adjustments.

2 Workout Reviews and Analysis

To reduce the switching activity which lowers the power in the test mode in test patterns, the modified clock scheme has been proposed as in [5], for these linear feedback shift registers. In this scheme, half of D flip-flops works and can be in the switching mode. For switching frequency reduction, BIST TPG technique is used as proposed in [6], where the difference of the clock frequencies can be noticed as D-times between the slow LFSR and the normal LFSR. The original rearranged LFSR generates the test pattern with low frequency. LT-TPG is introduced in [7] to reduce the power levels in the circuit while in the test mode.

In [8], the author describes both the LFSP, and these shift registers are required to give a single set of input sequences randomly. As mentioned in [9], it shows that a minimum of $(2m - 1)$ test vectors are embedded between the two adjacent vectors that are generated by the LFSR, where m denotes the length of LFSR. But in

2^m single input change, data can be inserted in between the sequences. Even if the average and the peak powers are reduced with these mentioned methodologies, the clock frequency increases when there is increase in the number of switching activity.

We come up with a brief analysis of the circuitry system. The classification of power dissipation in the CMOS technology is divided into two types. One is the static power dissipation, which is due to the current leakages in the circuits. The other is the dynamic power dissipation, due to transient current and also with charging and discharging of the load capacities. This energy used can be evaluated with parameters as follows:

$$E_i = \frac{1}{2} V_{dd}^2 C_0 F_i S_i, \tag{1}$$

where V_{dd} is the voltage, C_0 is the load capacitance, F_i and S_i are the internal node switching activities of node i. Similarly, the power consumption of this node i can be calculated as,

$$P_i = \frac{1}{2} V_{dd}^2 C_0 F_i S_i f, \tag{2}$$

where f is the clock frequency. From the both Eqs. (1) and (2), the energy E_i and the power P_i depend on the voltage, frequency, and the switching activities.

3 Existing Multiplier Design

The main goal of this paper is to present the low power dissipation with less number of switching activities in the design. Fig. 1 shows the BIST architecture. But this needs the additional blocks to the circuitry system. To these pattern generator blocks, we can use ROM which contains stored patterns or a counter or LFSR. And LFSR used as the signature analyzer. The controller then generates the control signals to activate all the blocks. But this includes the disadvantages where the architecture is based on LFSR. The system introduces a new concept called circuit under test (CUT) for the switching activity, under normal test operations [10].

The multipliers are also useful for DSP operations like the convolution for filtering, correlation, and the filter banks for multi-rate signal processing. Computation cannot be done without these multipliers, in the DSP applications. Hence, using the multiplier in the testing process is essential in the proposed technique. The Braun array multiplier is one among such multipliers. This type of multiplier has been chosen as it has the high speeds when compared with the non-pipelined multiplier. For avoiding propagating delays, the carry bits are made to propagate in further stage. In final step, ripple carry adder is made to produce P4 to P7 product terms as in the Fig. 2.

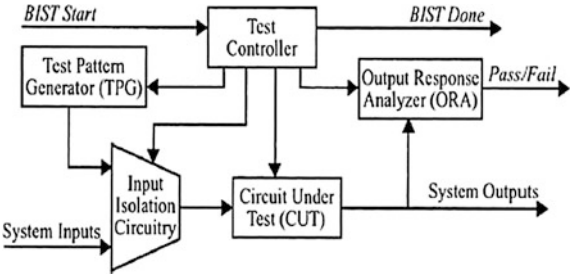


Fig. 1 Basic block diagram of BIST

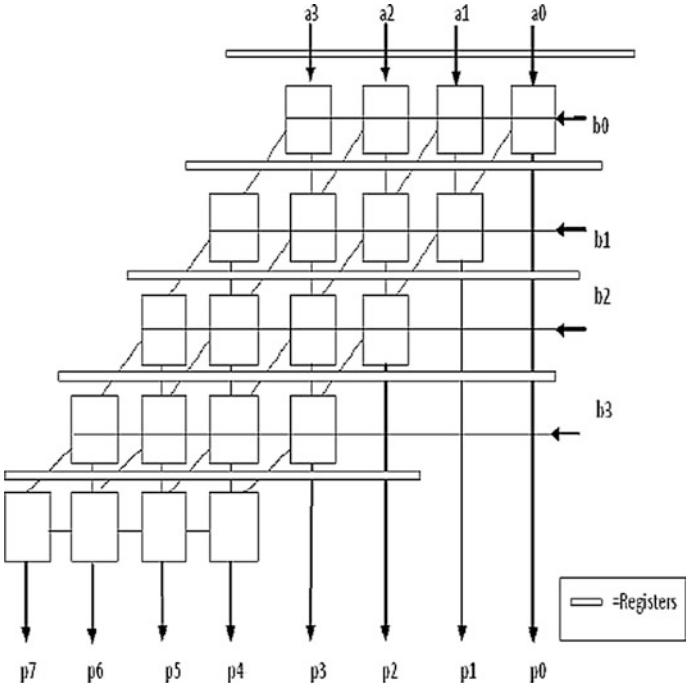


Fig. 2 Braun array multiplier

4 Proposed Methodology

LFSRs are more in use to generate test patterns, since the design occupies less area and is simple as other circuits. In this article, we introduce a novel architectural system that produces the test patterns including switching activity reductions. In LP-TPG, there are a modified low power LFSR, the gray counter, a NOR Gate structure, XOR-array, and also m-bit.

By initializing the m-bit counter with Zeros, 2^m test patterns are generated in the sequence. The purpose of CLK in the circuit is to control both the m-bit and the gray code generator. The generated output from the m-bit counter is used as the input to gray code generator. When all the bits of the counter output are zero, then the NOR-gate output is one. Only then the clock signal is applied to activate the LP-LFSR. It then generates the next signal. This is generated from LP-LFSR where it sets to XOR with generated information from gray code generator. These are final output patterns.

For this approach, an effective algorithm is implemented for LP-LFSR as follows.

Algorithm

1. Considering n > 2 // N-bit internal/external linear feedback shift register.
2. Suppose, if N-bit external LFSR is considered, then a common control signal is assigned to all n-flip-flops in the circuit.
3. Using multiplexers, for exchanging the adjacent flip-flop outputs. The select lines are then chosen from the output of the last stage (ls) flip-flop.
4. If ls = 1, then exchanging of outputs takes place with any one of the adjacent flip-flop.
5. If ls = 0, then exchanging of output are not carried.
6. The output from the other flip flops will be taken.
7. If the process reaches to 2^n states, then the number of expected transitions can be counted as 2^{n-1}. If swapping is done, then the expected transitions are 2^{n-2}.
8. This transition change can be noticed on any output of the multiplexer.
9. Modifications are done by the converter from the counter such that any two successive outputs can differ in only one bit as.

$$\begin{gathered} g[n-1] = k[n-1] \\ g[n-2] = k[n-1] \text{ XOR } k[n-2] \\ \vdots \\ g[1] = k[1] \text{ XOR } k[2] \\ g[0] = k[0] \text{ XOR } k[1] \end{gathered}$$

Thus it is clearly known that any two signal inputs must not share the same vectors. The test patterns produced from the methodology are given in the equations as follows.

$$
\begin{aligned}
&x[0] = f[0] \text{ XOR } g[0] \\
&x[1] = f[1] \text{ XOR } g[1] \\
&\cdot \\
&\cdot \\
&\cdot \\
&X\ [n-1] = f[n-1] \text{ XOR } g[n-1]
\end{aligned}
$$

This single input sequences from the XOR can reduce the maximum switching activity with less power dissipation comparatively resulting in the good targets when compared with the conventional LFSR. According to the designed circuit from Fig. 3, the test patterns are

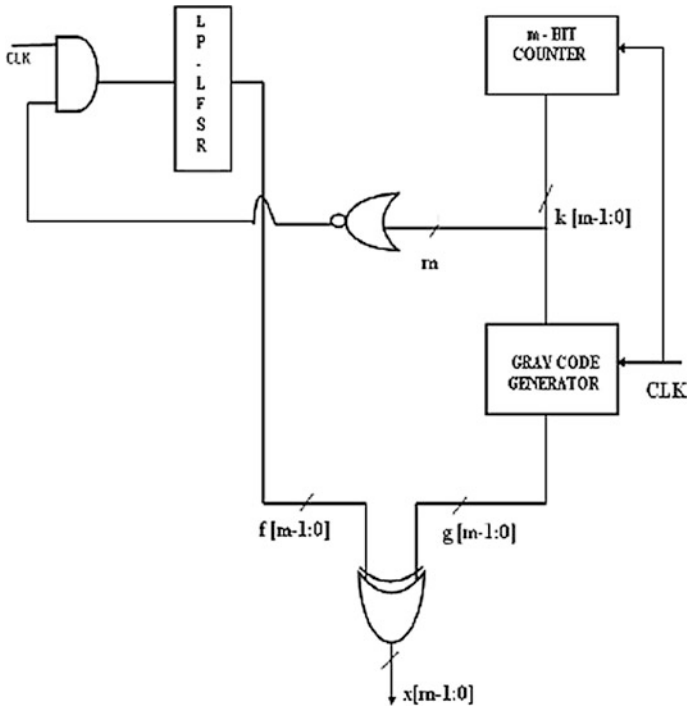


Fig. 3 Example of counter and gray values of the low power test pattern generator

k[2: 0]	g[2: 0]
k0 = 000	g0 = 000
k1 = 001	g1 = 001
k2 = **010**	g2 = **011**
k3 = **011**	g3 = **010**
k4 = **100**	g4 = **110**
k5 = **101**	g5 = **111**
k6 = **110**	g6 = **101**
k7 = **111**	g7 = **100**

To evaluate the effectiveness in proposed methodology, we have chosen the low-power TPG with conventional LFSR for the comparison with the proposed circuit. Table 1 explores the comparison of the power consumption between the TPG using conventional LFSR and the proposed LPLFSR after applying the generated patterns to the Braun array multiplier of 4 × 4 and the multiplier of 8 × 8. The generated test patterns from the mentioned two techniques are used to test the synchronous pipelined 4 × 4 and 8 × 8 Braun array multipliers.

The single-input changing sequence requires less switching activities when compared to the multiple-input changing sequence. Hence, this method of utilization leads to the best performance in the power reduction process. The transitions in the switching process are given in Table 2.

From the results observed in the implemented work, it is known that our proposed technique generates the better power reduction. The implemented circuitry is then tested using Wizard plug-in manager that is provided by the QUARTUS II. This is verified by the NIOS II processor.

Table 1 Comparing the various power reduction systems

System size	LFSR (4 × 4)	LFSR (8 × 8)	LP-LFSR (4 × 4)	LP-LFSR (8 × 8)
Logic elements	86	176	90	178
Frequency (MHz)	132.33	393.55	132.87	401.28
Total power dissipation (mw)	147.72	328.81	140.42	320.32
Dynamic power dissipation (mw)	18.4	50.68	11.34	38.32
Static power dissipation (mw)	80.03	80.65	80.01	80.63
Registers	81	1733	81	173

Table 2 Displaying the no. of switching transitions

Multiplier types	Total transitions
LFSR with Braun array multiplier (4 × 4)	41,956
Proposed technique (4 × 4)	***41,798***
LP-LFSR with Braun array multiplier(8 × 8)	1,26,496
Proposed technique (8 × 8)	***1,21,077***

5 Conclusion

The presented technology in this paper directs to the working method with TPG that has a LP-LFSR. This generator is turned to XOR with a sequence which is gray code generated input sequence. It reduces the switching activities very effectively and the test pattern starts working as a low-power agent in the circuitry system. Thus, the problem of power consumption is controlled significantly with only less number of switching activities. This can work better than the conventional LFSR in the system. The implementation technique shows the better power reduction from the other methodologies.

References

1. Balwinder Singh., Arun khosla., Sukhleen Bindra.: Power Optimization of linear feedback shift register (LFSR) for low power BIST. 2009 IEEE international Advance computing conference (IACC 2009) Patiala, India (March 2009)
2. P. Girard.: Survey of low-power testing of VLSI circuits. IEEE design and test of computers, Vol. 19, no. 3, PP 80–90, (May–June 2002)
3. Zorian. Y.: "A Distributed BIST control scheme for complex VLSI devices," Proc. VLSI Test Symp., P. 4–9, (1993)
4. Mechrdad Nourani.: Low-transition test pattern generation for BIST-Based Applications. IEEE TRANSACTIONS ON COMPUTERS, Vol 57, No. 3, (March 2008)
5. Girard. P., Guiller. L., Landrault. C., Pravossoudovitch. S., Wunderlich. H. J.: A modified clock scheme for a low power BIST test pattern generator. 19th IEEE proc. VLSI test Symp., CA, pp-306–311, (Apr–May 2001)
6. Wang. S., Gupta. S. K.: DS-LFSR: "A BIST TPG for low switching activity," IEEE Trans. computer-aided design of Integrated circuits and systems, Vol. 21, No. 7, pp. 842–851, (July 2002)
7. Mechrdad Nourani.: Low-transition test pattern generation for BIST-Based Applications. IEEE TRANSACTIONS ON COMPUTERS, Vol 57, No. 3, (March 2008)
8. Voyiatzis. I., Paschalis. A., Nikolos. D., Halatsis. C.: An efficient built-in self test method for robust path delay fault testing. Journal of electronic testing: Theory and applications Vol. 8, No. 2, pp-219–222, (Apr-1996)
9. He. R. H., Li. X.W., Gong. Y. Z.: "A scheme for low power BIST test pattern generator," micro electronics & computer, no. 2, pp. 36–39, (Feb. 2003)
10. BOYE., Tian-Wang Li.: A novel BIST scheme for low power testing. IEEE. (2010)

Generation and Decoding of Non-Binary LDPC Codes Using MSA Decoding Algorithm

J. Chinna Babu, C. Chinnapu Reddy and M.N. Giri Prasad

Abstract The latest advancements in low density parity check (LDPC) codes have resulted in reducing the decoding complexity. Hence these codes have excelled over BCH and turbo codes in terms of performance in the higher code rate, hence these codes are the trending topic in coding theory. Construction of LDPC codes is being elaborated in this proposed paper which further helps to study encoding and decoding of these NB-low density parity check codes. In the proposed design architecture, we have considered the Min-Sum Decoding Algorithm (MSA) employed here utilizes reliability estimation to improve error performance and it has advantages over bit flipping (BF) algorithms This algorithm can be improved with still more security level by having a trade-off between performance and data transmission. It can also enhanced by implementing it in real-time applications for data decoding and correction, for smaller size datum and these codes are used for medical and signal processing applications. These proposed LDPC codes are also used in the generation of bar codes, which are used in real time applications.

Keywords LDPC codes · Decoding algorithm · Shannon limit · BCH codes · Turbo codes

J. Chinna Babu (✉) · M.N. Giri Prasad
Department of ECE, JNTUA, Anantapur, Ananthapuramu, AP, India
e-mail: jchinnababu@gmail.com

M.N. Giri Prasad
e-mail: mahendragiri1960@gmail.com

C. Chinnapu Reddy
Department of CTE, SPFU-AP, TEQIP-II, Vijayawada, AP, India
e-mail: ccreddyece@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_61

1 Introduction

For error-free transmission of data from source to its destination over a noisy channel, error coding is needed. Error coding uses mathematical formulae to encode the data for error-free transmission and the resultant code word is decoded at the receiver to obtain the relevant information [1–3]. Different error decoding schemes can be selected depending on the expected error types, the expected error rate of communication channel and on whether data retransmission is possible or not.

1.1 Error-Correcting Code

The parity data or redundant data is added to the original message, so that the original message could be decoded [4] at the optimum receiver side without the need of the data retransmission and also the errors can be detected and corrected [5, 6] if any errors are present. Such codes are called error correct LDPC code (ECC) or forward error correct LDPC code (FEC).

Error-correcting codes are usually of two types:

- Convolution codes: These codes are polished, based on bit-after-bit process.
- Block codes: These codes are also polished, based on block-after-block process.

1.2 Representation of LDPC Codes

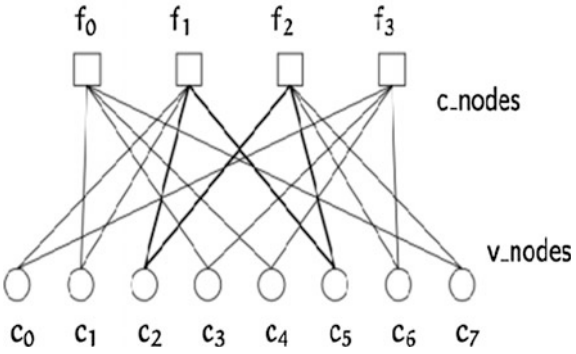
LDPC codes were developed by Robert G. Gallager, hence these were also known as Gallager codes. Since practical realization seems impossible, these codes were neglected although the code was invented in the early 1960s [7–9]. These LDPC codes are linear type of error-correcting codes and approaches near Shannon capacity limit. The term "Low Density" replies one of the unique characteristic features of the parity check matrix which contains only less number of ones in comparison to zeros [10, 11]. The proposed codes are arguably the best error-correcting codes in existence at present scenario.

Proposed LDPC codes are functionally represented by the sparse parity matrix. This defined matrix was often randomly generated and it was subjected to the sparse constraints [12, 13]. An LDPC code is defined by the parity check matrix H which is null space and it is defined with the following properties:

- Each and every row contains p number of ones.
- Each and every column contains r number of zeros.
- The number of ones in between any adjacent two columns which are commonly represented by λ should not be greater than one.
- p and r should be less, compared to the finite variable code length and number of the remaining rows in parity matrix H.

Fig. 1 The Tanner graph for the below mentioned parity check H-matrix

$$H = \begin{bmatrix} 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \end{bmatrix}$$



Since these p and r are very small, the H parity matrix has less number of ones and therefore it is a sparse matrix. Hence, these codes are specified by a parity matrix H and it is called low density parity check code matrix.

Figure 1 shows the parity check matrix with dimensions n × m for a (8, 4) code. The tanner graph is a bi-partite representation of H-matrix, where c-nodes (f_0, f1, f2, f3) are called check nodes or constraint nodes and v-nodes (c_0–c_7) are called variable nodes. This check node f_i is mapped to the variable node c_j, if the element h_{ij} of parity check matrix H is 1 [14].

These LDPC codes are generally classified into two types. They are

1. Regular LDPC codes: These LDPC codes have equal amount of row weights (W_r) and equal column weights (W_c) (No. of 1's in rows and no. of 1's in columns)

   Ex:

$$\begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}$$

   Here, $W_r = 3$ for all rows and $W_c = 2$ for all columns.

2. Irregular LDPC codes: All the rows may have different weights
3. ($W_r \neq$ constant) and all columns may have different weights ($W_c \neq$ constant)

Ex:

$$\begin{bmatrix} 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix}$$

- If all the rows and columns in a parity check matrix contains even number of one's then these are said to be "Non-Binary LDPC codes" otherwise these LDPC codes are known as "Binary LDPC codes".

2 Construction of LDPC Check Matrix

The $H_{M \times N}$ parity check matrix is defined as (N, K), here N is the total variable code length, and K is the number of actual information bits and N–K number of parity bits.

- The code word is said to be legal, if it satisfies when $c \star H^T = 0$
- We can generate the codeword, by multiplying the message 'M' with generator matrix 'G'. Where $C = M \star G$
- The generator matrix G can be obtained from H-matrix by
- By rearranging the H-matrix by using row and column operations
- $H_{sys} = [I_m | P_{m \times k}]$
- Systematic parity check matrix (H_{sys}) can be Rearranged as
- Generator Matrix $(G) = [P^T_{k \times m} | I_k]$
- We can verify our results as $R \star H^T = 0$

2.1 Basic Procedure for Calculation of Parity Check Matrix of LDPC Codes (Non-Binary)

Consider the Non-Binary LDPC code, which is of length (12, 6). It is difficult to calculate (12, 6) parity check matrix, so based upon 2:1 ratio, (12, 6) parity check matrix is calculated by (6, 3) parity check matrix.

Step 1: Primitive polynomial calculation

- Consider the odd numbers from 1 to 6
- 1-001, 3-011, 5-101
- Concatenate MSB bit with '1'
- 1-1001, 3-1011, 5-1101
- Reverse the concatenated bits
- 1-1001, 3-1101, 5-1011
- Compare the concatenated bits with the reversed bits and ignore if they are equal.

$$1 - 1001 - 1001$$
$$3 - 1011 - 1101$$
$$5 - 1101 - 1011$$

- For the primitive polynomial, select the minimum value of remaining.

$$1101 - 13$$
$$1011 - 11$$

Hence 1011 is considered as primitive polynomial P(x) = $x^3 + x + 1$ (1011)

Step 2: Degree term calculation:

The degree terms are calculated by left shifting of the bits and if the value of bits exceeds the value '6' then XOR with the primitive polynomial.

$\alpha^0 = 001 = 1$; $\alpha^1 = 010 = 2$; $\alpha^2 = 100 = 4$; $\alpha^3 = 1000\text{^}1011 = 011$

$\alpha^4 = 110$ ==> Exceeded 6 ==> 0; $\alpha^5 = 1100\text{^}1011$ ==>0111^1011 => 100 => 4

H-Matrix for (12, 6):

From degree terms, we can generate the below matrix by writing the bits in columns from LSB to MSB. The following matrix is considered as (w_r, k), where $w_r = 2$ is row weight and k = 3, number of rows in matrix. The parity matrix is obtained by rearranging the columns accordingly.

Now the parity matrix for (6, 3) code is written as

$$H = \begin{bmatrix} 0 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 \end{bmatrix}$$

By using this (6, 3), H-Matrix we generate the H-Matrix for (12, 6)

$$H = \begin{bmatrix} M1(x) & M1sC(x) \\ M1RsC(x) & M1RC(x) \end{bmatrix}$$

where

M1(x)	It is the parity check matrix for (6, 3) code
M1sC(x)	Shift the row from down and column from the bottom to middle and vice versa
M1RsC(x)	Shift the column
M1RC(x)	Change last column to middle and middle row to column

The final H-Matrix after shifting the rows and columns is

$$H = \begin{bmatrix} 0 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \end{bmatrix}$$

For (12, 6) code, there are 12 variable nodes represented by the columns and 6 check nodes represented by rows.

3 Procedure for Decoding of Non-Binary LDPC Codes

This proposed MS algorithm is employed for decoding of Non-Binary low density parity check codes. This proposed method is based on soft-decision decoding scheme, hence it is efficient for decoding of Non-Binary LDPC codes.

3.1 Algorithmic Steps for Min-Sum Algorithm:

Step 1: Generate the low density parity check matrix H(x).
Step 2: Draw the pictorial representation of the Tanner graph for the resultant parity check matrix H(x).
Step 3: Initialize the logarithmic likelihood ratio (Lr) values to the variable nodes.
Step 4: Update check nodes with permutation values (Pr) obtained from variable nodes.
Step 5: Verify the variable nodes whether they are satisfied or not based on Lr values obtained from check nodes.
Step 6: If the Variable Node Unit (VNU) or variable node updater satisfied with Lr values then output is zero otherwise it can be displayed as one (as shown in Fig. 3).

4 Simulation and Synthesis Results

If reset = 1 then the inputs which are given are assigned and if reset = '0' then whatever the inputs are, it may be assigned to 0. The output can be displayed as Dblk which is a 16-bit information. If all the nodes are satisfied then the output

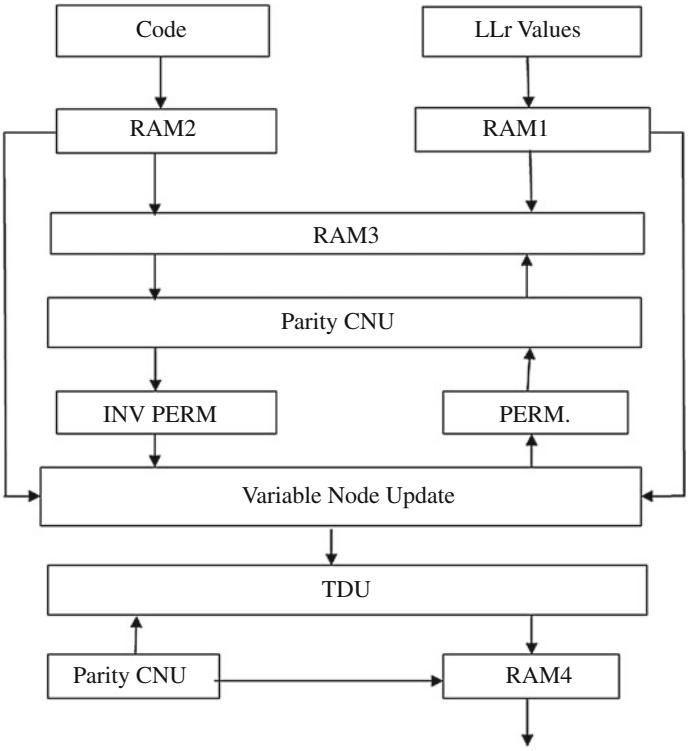


Fig. 2 Block diagram of the Min-Sum Decoding Algorithm

Dblk is displayed as "0000000000000000" else change the iterations value ITER then maximum number of nodes are satisfied. The Lr1 (15:0), Lr2 (15:0) and L Ratio (15:0) are assigned when reset = 1 and displays output Dblk and Pr1 (15:0), Pr2 (15:0). The outputs Pr1 (15:0) and Pr2 (15:0) act as inputs to the CNU block as shown in Fig. 2 [14].

When reset = 1 then the inputs Pr1 (15:0), Pr2 (15:0), Pr3 (15:0), and Pr4 (15:0) are assigned and these inputs are taken from VNU block and the outputs Or1 (15:0), Or2 (15:0), Or3 (15:0), and Or4 (15:0) are displayed. The above-mentioned synthesis results yield better decoding complexity and offer less hardware from the availability resources of the target device used for decoding and generation of the LDPC codes (Figs. 3 and 4) [13, 14].

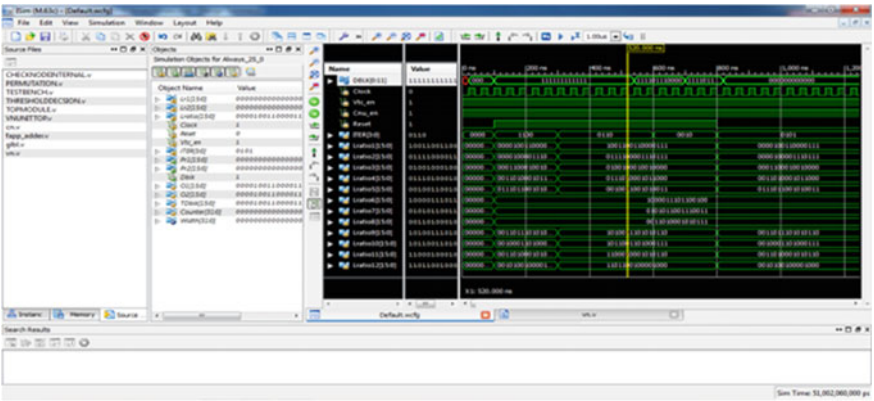


Fig. 3 Simulation results of the Non-Binary LDPC decoder LLR Values

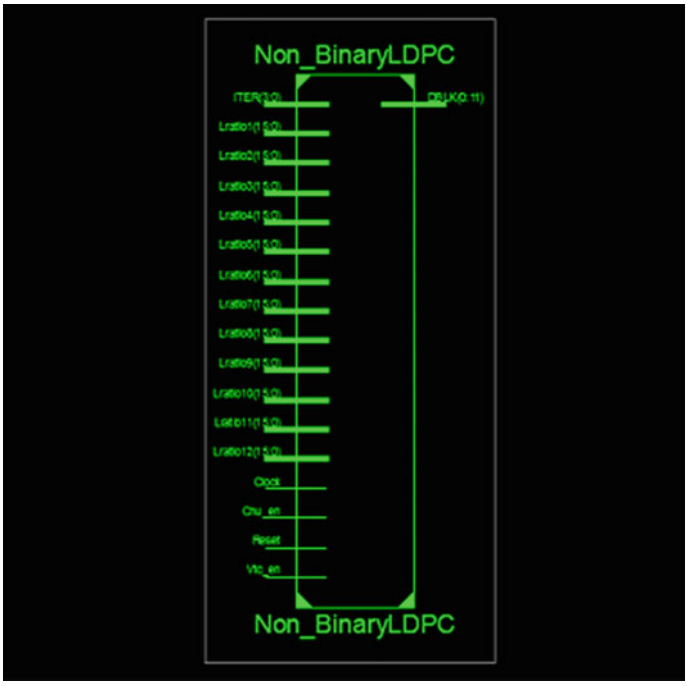


Fig. 4 RTL schematic of the Top Module

5 Conclusion

The good error-correcting capabilities of Geometric LDPC codes are gaining more prominence in many fields. As the technology is advancing many decoding algorithms for the LDPC codes have been developed. The construction of the parity check matrices are explained in this paper for the Non-Binary low density parity check codes. The proposed Min-Sum Decoding Algorithm reduces hardware operations and power consumption along with improved performance. By using this MSA algorithm, we can have several features like low decoding complexity, high throughput, and better error detection and correction capabilities for the proposed Non-Binary LDPC codes.

References

1. Gallager. R. G.: Low density parity check codes", *IRE Trans. Info. Theory*, vol. IT- 8, pp. 21–28, (1962)
2. MacKay. D. J. C., Neal. R. M.: Near shannon limit performance of low density parity check codes. *Electronics Lett*, vol. 32, no. 18, pp. 1645–1646, (1996)
3. D. J. C. MacKay, "Good error correcting codes based on very sparse matrices", *IEEE transactions on Information Theory*, 1997
4. MacKay. D. J. C.: Gallager codes that are better than turbo codes. *Proc. 36th Allerton Conf. Communication, Control, and Computing*, (1998)
5. Kou. Y., Lin. S., Fossorier. M.: Low density parity check code based on finite geometries: a rediscovery and more. *IEEE Transactions on Information Theory*, (1999)
6. Fossorier. M. P. C., Mihaljevic. M., Imai. H.: Reduced complexity iterative decoding of low-density parity check codes based on belief propagation. *IEEE Trans. Commun.*, vol. 47, no. 5, pp. 673–680, (May 1999)
7. Kschischang. F. R., Frey. B. J., Loeliger. H.-A.: Factor graphs and the sum–product algorithm. *IEEE Trans. Inf. Theory*, vol. 47, no. 2, pp. 498–519, (Feb. 2001)
8. Zhang. J., Fossorier. M. P. C.: A modified weighted bit-flipping decoding of low-density parity-check codes. *IEEE Commun. Lett.* vol. 8, no. 3, pp. 165–167, (Mar. 2004)
9. Chen. J., Dholakia. A., Eleftheriou. E., Fossorier. M. P. C., Hu. X.-Y.: Reduced- complexity decoding of LDPC codes. *IEEE Trans. Commun.*, vol. 53, no. 8, pp. 1288–1299, (Aug. 2005)
10. Palanki. R., Fossorier. M. P. C., Yedidia. J. S.: Iterative decoding of multiple-step majority logic decodable codes. *IEEE Trans. Commun.*, vol. 55, no. 6, pp. 1099–1102, (Jun. 2007)
11. Savin. V.: Min-Max decoding for Non-Binary LDPC codes. in *Proc. IEEE ISIT*, 2008, pp. 960–964
12. Cho. J., Sung. W.: High-performance and low-complexity decoding of high-weight LDPC codes. (in Korean) *J. Korea Inf. Commun. Soc.*, vol. 34, no. 5, pp. 498–504, (May 2009)
13. C. Zhang, Z. Wang, J. Sha, L. Li, and J. Lin, "Flexible LDPC decoder design for multi-Gb/s applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 1, pp. 116–124, (Jan. 2010)
14. Zhang. X., Siegel. P. H.: Quantized min-sum decoders with low error floor for LDPC codes," in *IEEE Intl. Sym. Infor. Theory*, pp. 871–875, (Jul. 2012)

Controlling the Traffic Interactions with High Mobility and Constant Network Connectivity by Vanets

G. Vijaya Padma, K. Hari Kishore and S. Jaya Sindura

Abstract Vehicular ad hoc network (VANET) are introduced with high mobility to avoid maximum critical zone on the roads. Wireless collision avoidance (CA) systems play an important role to warn the drivers before they meet the high damages on the roads. Global positioning systems are used for trapping the vehicle positions and communicating process goes in the vehicles of the network. Even the other vehicles does not affect, broadcasting has to be in the multicasting stage at severe stages. To grab the vehicle positions, there are some parameters which depend for calculating the relative positions of the vehicles. The distance between vehicles, the direction of the travelling vehicle and the bearing angle are main parameters that are to be considered. Our paper introduces a system which finds the position using great circle algorithm (GCA). The gradual incremental connectivity of the network in VANETs is used in detecting the failure vehicles and finds the connectivity between the other vehicles on the road sides. It also multicasts the alert messages to the vehicles which are already identified. Hence, broadcasting problem can be avoided.

Keywords VANET · CA · GCA

1 Introduction

Managing the traffic control is most important to avoid the collisions between the vehicles on the roads while travelling. For controlling the traffic interactions, a constant network connectivity between the processing vehicles must be absolutely

G. Vijaya Padma (✉) · K. Hari Kishore
Department of ECE, KLEF, K L University, Green Fields, Guntur, AP, India
e-mail: gujjuvijayapadma@gmail.com

K. Hari Kishore
e-mail: kakarla.harikishore@klunivrsity.in

S. Jaya Sindura
Department of ECE, Raghu Engineering College, Visakhapatnam, AP, India
e-mail: sigireddy111@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_62

maintained. For this, VANETs are the useful systems which are helpful to avoid the vehicle collisions on the highways. VANETs are widely used in the research development standardizations since it can handle the critical situations in the accidental environments of vehicles with road safety issues. Hence, these type of networks are used mainly in the safety applications.

VANETs are provided in various applications, considering the safety and efficient transportation in the highways of the networks became a challenging scenario. Previous research works mainly focused on specific areas and increase the perfectness in the network connectivity at real-time scenarios. The components called Drivers, helps in noticing the accident levels and receive the emergency signals, which can react in a mean time to these emergency situations and also avoids the accident severity. This improves in reducing the collisions of vehicles as well as the road safety and life safety in these aiming networks.

In applications such as collision avoidance and the LBS, the main requirement of such development needs Relative positioning. But in case of raising the performance levels, another technique which can be used is cooperative positioning (CP). The car drivers can receive the Emergency alert messages, only with the perfect connectivity of the network. Thus, drivers can have a chance to break through the accidental environments. The vehicles which are in Region of Interest (RoI) must be connected to the VANETs. There is problem arises with the sparse vehicles in the late nights. To overcome this HOLE problem is the major challenging part of the safety applications in the VANETs.

By RSU, we can able to detect the accidental environments and finds the failure vehicles with Geo positioning. RSU sends the multicasting alert packets only to the networks which are under enhanced VANETs. It manages the location information, relative positioning, with the help of Great Circle Algorithm (GCA). Thus, we can improve the routing of early alert messages and avoid the disconnection problem in the network.

2 Vehicular Applications

The distributed transmission power control in [1], is based on the controlling periodic message loads in the network and to avoid saturated channel conditions. A positive orthogonal code is mentioned in [2], that distributes a transmissions in the form of patterns for broadcasting performance in terms of the probability and reporting the average delay in message delivery. In a simple VANET system, emergency messages are given to the drivers on the road by the wireless Collision Avoidance (CA) system as needed in the dangerous zones.

For measuring the performance, the analytical model is proposed for wireless systems which is termed as the emergency messaging as in [3]. The delay is calculated by minimizing the number of chain collisions as mentioned by [4].

The authors in [5, 6] proposed a special protocol DV-CAST which depends on the vehicular network connectivity for making routing decisions. Vehicle-to-Vehicle communication network is one of the best VANETs for Cooperative Vehicle Safety (CVS) [7].

DTNs are another type of specialized networks that are mention in [8], the end-to-end routing of mobile nodes may not exists, where there is no scope of utilizing the traditional networks like AODV and DSR. But the asynchronous message forwarding paradigm is used to achieve the interoperability in the network connectivity. Naumov et al. has great studies in [9] on VANET routing protocols with mobility information by vehicular traffic simulator which is based on the road-map scenarios' ratio. Most of the authors aimed at fragmentation levels in the networks with mobility applications and a smart solution store–carry–forward is given basing on the routing in disconnected mode of networks [10].

The previous workouts declare that, when the VANET is well connected, the accidental environments can be reduced to some extent and the traffic-related data can be successfully collected. In the sparse network types, the disconnection between the two vehicles probably occurs and the message delivery is taken by the store carry forward scheme.

3 Enhancing the Network Connectivity

Network fragmentation is the raising problem in the network connectivity. This can be solved by multicasting the messages to the vehicles with the Routing protocol. With the efficient routing protocol for emergency messaging, it is essential of introduce a model which is highly reliable and with low delay. The VANETs are used to overcome these unreliable situations. By using the relative positioning, the vehicles can receive the early alerts messaging. This is done by sending the emergency alert messages to those vehicles which are in danger zone. In the accidental environments, the vehicles in these regions are thus multicast with the early alert messages. For this, a few hop counts are highly necessary with high reliability and low delays.

Passing the safety messages to the vehicles through RSU connectivity turns into a challenging aspect in the enhanced deployed connectivity of the network. Fragmentation is a special issue in the VANET networks as in mobility patterns. This special property stands for a while in such cases. To increase the efficiency in the transportation of the data, VANET helps in providing the location and travel information as well as the safety signals to the vehicles. Thus, the flow of the vehicles on the highways is improved and develops a comfort applications. The routing protocol in the VANET networks, many-to-many and one-to-many communication is provided for the perfect communication of the signals. This increase

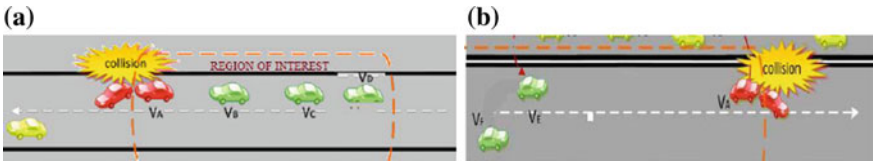


Fig. 1 Different events that effects the vehicle in the connectivity

the multicasting routing protocol. This type of protocol is designed to meet the desired needs in safety and also nonsafety applications.

The Fig. 1 shows clearly that VA come across with an accident. And the four vehicles VB, VC and VD comes into RoI in the network. As the other vehicles are behind, when VA met to an accident, remaining vehicles can receive the emergency signals to be aware of the accident in that region. If accident occurs, then all vehicles will not get affected. And broadcasting is not needed. Hence, multicasting is only solution without broadcasting. But the challenging issue raises to which vehicles is that emergency signal has to pass in the network. Only identified vehicles will get the alert message signals. The breakups in the networks may be created with these sparse vehicles as they have less density at night time.

This is defined as a HOLE problem. Network fragmentation is then created. The solution to this problem is deploying the RSU in desired network which increases the network connectivity. In the above Fig. 1b, it is shown how the network gets fragmented due to the sparse in the connectivity. With the normal traffic conditions on the highway, vehicle may not receive the alerts on long distances and this problem is said to be HOLE problem. So the RSU must be deployed to overcome this. It holds the location information of all the vehicles, notifies the affected vehicle and tries to calculate the Region of Interest (RoI) for it.

4 Research Analysis

The great-circle distance is the distance between the points on the sphere which is also known as orthotropic distance. But the spherical measure is not identical with a Euclidean geometry and it has variable distance values. The Euclidean distance is measured as the length of that straight line from those two considered points. But in the spherical geometry point of view, it replaces all these straight lines in the sphere as it is not formed with straight lines. Hence the great-circles are considered as the Geodesics of the sphere. For any of the considered points, only unique great-circle exists where these points are not in the opposite placements. This forms two equal arcs which have the equal to the half the circumference of the circle (πr). r represents the radius of the circle.

To calculate the vehicle direction it is enough to know the coordinates of two consistently received landmarks. If the Cartesian coordinate system used and adopt the longitude on the axis "X," latitude on the axis "Y"—then we can find the vector of the movement. The Fig. 2a, b elaborates vector calculation and the angle of the vector. With the direction of the vehicle, correction of bearing angle has to be calculated. The following code gives the calculation of the angle of movement (relative to north), with two considered landmarks. Bearing angle can also calculated by GCA, which another alternative method. GPS helps in finding the vehicle current position periodically with accurate measures. The great circle indicates current bearing position and used to find the distance which is used to find the relative positions of vehicles.

In Fig. 3, the VANET scenario is shown where inter vehicular information sharing takes place. All the others vehicles have the location information between them, which is in terms called the vehicular network. Blockage in the traffic occurs, when it passes the alert message to other vehicle in the network.

And hence, the traffic problem is raised. The vehicle's travelling direction plays an important role to find the relative positioning. Even when there exist an emergency event, there is no need of passing any shared information to other vehicles.

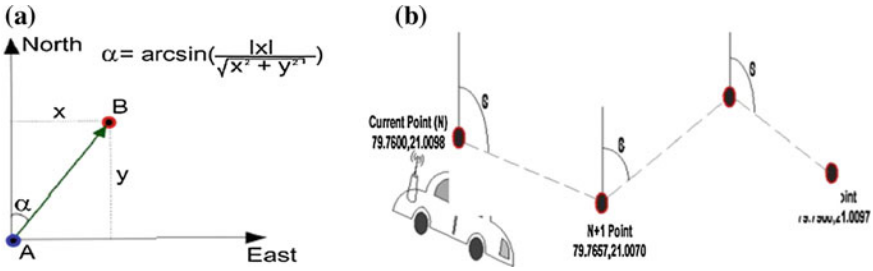


Fig. 2 **a** Finding angle of movement. **b** Finding bearing angle

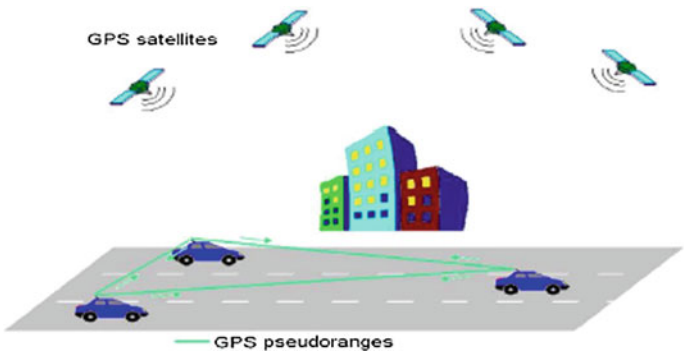


Fig. 3 Locations relation identification

If the vehicle is found behind the accident vehicle, then it avoids to broadcast alert message. Thus, the alert packets can be multicast. RSU detects failure vehicles and holds to manage the vehicular information within the network. It stores the information of vehicles and finds out the affected vehicle (which are mostly affected by failure vehicle). The relative positioning of the vehicle can be determined with bearing angle, distance, and vehicular travelling direction. RSU finds out the affected vehicles and packet is multicast to the calculated vehicles. The relative vehicle positioning depends on the Travelling direction of the vehicles as shown in Fig. 4. Using GPS device protocol data system can get the direction for which system need to parse and process this data.

This algorithm is also helpful in finding the angle Geo points on the earth. Travelling direction of the vehicle can be found with GPS device. But the relative positioning cannot be detected while the vehicle is in travelling condition as the travelling direction will change the relative position.

Assuming the three vehicles in the network say A, B, C are moving to EAST as in Fig. 5. A is the last vehicle which is called the Leading vehicle. The direction and the bearing angle of the vehicle is known, the relative positioning can be measured between the vehicles. If A travels to West, then B and C are said to be behind A. The accident takes place since the direction of B is to East. Hence, bearing angle of C and A must be measured first. The resultant of C is then said to be minor angle

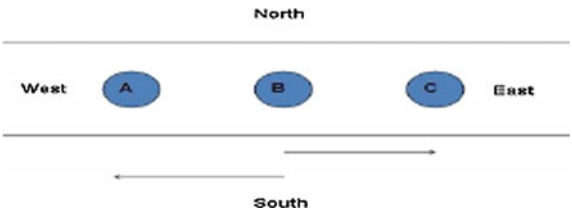


Fig. 4 Travelling direction of the vehicles

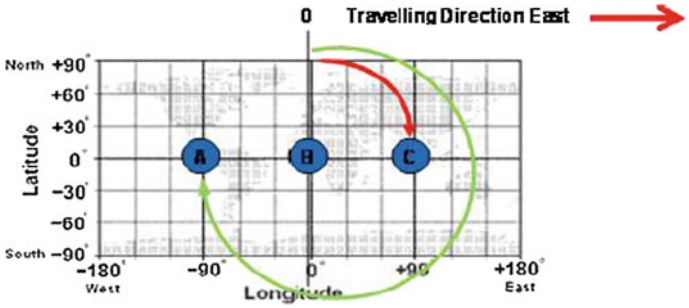


Fig. 5 Direction of the travelling effects

and A is said to be at major angle. Therefore, it is concluded that C is a leading vehicle. A receives the emergency message.

The modules with high quality with low cost, are generally suited for the navigation applications and also the embedded locations. The device output is provided as raw where the connections are arranged in the serial form. The special character 'comma' is used as a delimiter. GPS is provided with various protocols which are used for generating different types of information. And the device can be connected to the PC physically by using a USB or Bluetooth. A logical port is necessary for the backend programming of the device. Generally COM port is used for the programming purposes. O.S Map physical devices to the logical applications are used more frequently. After a perfect connectivity to the system, by the COM port, the data can be read from the device. This data is then parsed for obtaining a complete set of the information, which is fetched by GPS with multiple lines separated with a special symbol ','. The data parsing is done with a function called split() function.

5 The Connectivity of the Vehicles with the RSUs

The Fig. 6a shows the real communication between the RSUs and vehicles with its location information by their routing network. This data is shared among RSU connectivity, for notifying the present position of the RSU. It calculates the relative positions on the basis of Great circle algorithm which describes the vehicles distance and location in between them. The Fig. 6b shows, the RSU connectivity decides the travelling directions with each location of the vehicles, and then calculates the relative positions among all the vehicles that are in the network. RSU can also used in finding the relative positioning of the multiple vehicles and multicasts the alert packets for identifying these vehicles that are in the network connectivity.

With help of GPS receiver, we can probably identify the directions and available placements by the data which is already parsed above explanation. Thus, the data

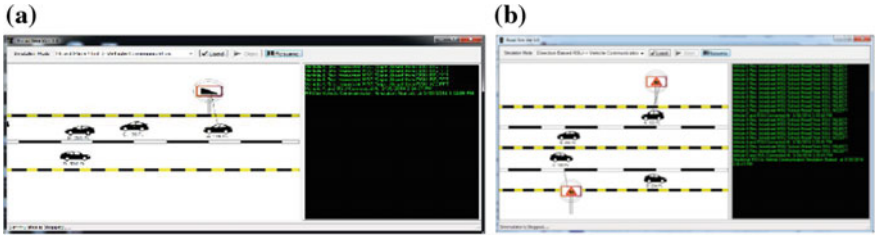


Fig. 6 **a** RSU communication. **b** RSU connectivity

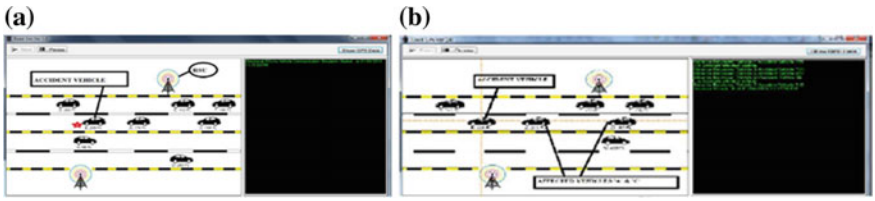


Fig. 7 **a** Calculating the bearing angle with distance. **b** Finding damaged vehicles with relative positioning

can be shared through the vehicles by the help of RSU network connectivity. This connectivity can also calculates bearing angle and distance with this information, with the help of great circle algorithm. The Fig. 7a describes the network connectivity with RSU. If any accident occurred between the vehicles is noticed, the RSU then finds the vehicle that may get affected by these and identifies those vehicles by relative positioning as in Fig. 7b. Once if these vehicles are identified, RSU then multicasts the early alert packets to vehicles that are identified.

6 Conclusion

Travelling safely on the roads became the important issues in the present traffics with the required comforts is one of the goals of the VANETs application systems. On the damaging events like the road accidents occurs, the vehicles on the network will get effected and broadcasting of the early alert messages are not necessarily connected. Hence, multicasting is one of the preferable methods in these issues. Thus, the panic situations can be avoided for the unwanted vehicles. Broadcasting problem can be solved and there are no more of traffic jams on the highways. The roadway accidents thus can be reduced to some extent and the collisions between the vehicles can be controlled by sending the early alert packets. To get the exact information, GPS data is fetched and parsed. Then, the vehicle is instructed to the right direction on the heavy traffics.

References

1. M. Torrent-Moreno, J. Mittag, P. Santi, and H. Hartenstein, "Vehicle-to-Vehicle communication: Fair transmit power control for safety-critical information," *IEEE Trans. Veh. Technol.*, vol. 58, no. 7, pp. 3684–3703, Sept. 2009.
2. F. Farnoud and S. Valaee, "Reliable broadcast of safety messages in vehicular ad hoc networks," in *Proc. IEEE INFOCOM*, Apr. 2009, pp. 226–234.
3. Sok-Ian Sou, "Modeling Emergency Messaging for Car Accident over Dichotomized Headway Model in Vehicular Ad-hoc Networks," 2013 IEEE.

4. Q. Xu, R. Sengupta, and D. Jiang, "Design and analysis of highway safety communication protocol in 5.9 GHz dedicated short range communication spectrum," *IEEE Trans. Veh. Technol*, vol. 57, no. 4, pp. 2451–2455, 2003.
5. O. K. Tonguz, N. Wisitpongphan, F. Bai, P. Mudalige, and V. Sadekar, "Broadcasting in VANET," in *Proc. IEEE INFOCOM MOVE Workshop*, May 2007, pp. 7–12.
6. O. K. Tonguz, N. Wisitpongphan, and F. Bai, "DV-CAST: A distributed vehicular broadcast protocol for vehicular ad hoc networks," *IEEE Wireless Commun.*, vol. 17, no. 2, pp. 47–57, Apr. 2010
7. R. Sengupta, S. Rezaei, S. E. Shladover, J. A. Misener, S. Dickey, H. Krishnan, "Cooperative Collision Warning Systems: Concept Definition and Experimental Implementation," Journal of I TS, vol. 11, No. 3.
8. K. Fall, "A delay-tolerant network architecture for challenged Internets," in *Proc. SIGCOMM*, 2003, pp. 27–34.
9. V. Naumov, R. Baumann, and T. Gross, "An evaluation of inter vehicle ad hoc networks based on realistic vehicular traces," in *Proc. 7th ACMMobiHoc*, 2006, pp. 108–119.
10. Y. Zhang, E. K. Antonsson, and K. Grote, "A new threat assessment measure for collision avoidance systems," in *Proc. 2006 IEEE Intelligent Transportation Syst. Conf.*, pp. 968–975, Sept. 2006

Improved Process Scheduling in Real-Time Operating Systems Using Support Vector Machines

S. Satyanarayana, P. Sravan Kumar and G. Sridevi

Abstract In the field operating systems, most advanced scheduling method is Multilevel Feedback Scheduling. There are multiple queues with different level priorities (high to low). Selection of each process from a queue is based on the priority of the queue. Support Vector Machine (SVM) method is learning linear predictions in high-dimensional feature spaces. SVM approach can handle the sample complexity challenges by searching large margin separators. In this paper, we are proposing an innovative machine learning Support Vector Machines to predict priorities of multiple queues based on the knowledge of past processes in real-time Operating Systems. This approach can train each queue with linear predictions. So that real-time operating systems like Embedded Systems/Firmware can handle nonhomogenous tasks also. The problem of predicting large volume of processes can be solved with high performance. This algorithm is tested with onelakh processes and these processes are scheduled in 1 min 5.377 s.

Keywords Real-time operating systems · Tasks · Vector · Queue · Process type · Priority · Process scheduling · Dynamic allocations · Self-learning algorithms

1 Introduction

Machine-Learning systems automatically learn programs from data. This is an intelligent process which is an alternative for manual learning to programs. Machine learning is used in Search Engines, Spam Filtering, Stock Trading,

S. Satyanarayana (✉) · P. Sravan Kumar · G. Sridevi
Department of CSE, Raghu Engineering College, Visakhapatnam, AP, India
e-mail: satyacomp@gmail.com

P. Sravan Kumar
e-mail: shraonep@gmail.com

G. Sridevi
e-mail: gaddesridevi.85@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_63

Designing Drugs, and many other applications [1]. Now-a-days, machine-learning techniques are used to improve process scheduling in operating System. The core functionality of operating system is process scheduling. Operating system has many scheduling algorithms like first arrived process is executed first, Time Quantum Scheduling (Round Robin), Shortest Process First and others. One of the objectives of these algorithm is to optimize waiting time (avg waiting time). In Multilevel Feedback Queue Scheduling (MFQS) technique, each queue is defined as a vector of processes. Each queue is assigned with a priority number from low to high. These priority numbers are system defined [2]. Using Support Vector Machines (SVM) this priority number of MFQS is automatically learned by the program from the data [2]. The data is a persistent object stored in text/binary file. Each time when operating system selects process from vector, it uses the persistent data available in the file. And the queue containing more number of processes will be with high priority and queue with less number of processes will be with low priority.

Inference

Based on the evidences and reasoning of past research on Multilevel Feedback Queue Scheduling, all the past process scheduling algorithms based on major algorithm steps are [3]:

(i) Divide memory into three multiple queues
(ii) Initially, wait until all the process have been come into first queue
(iii) After entering, sort all processes in according their burst time
(iv) After sorting, apply RR (round robin) scheduling with time quantum
(v) As now, in MLFQ, processes are switched from one queue to another.

In this paper, proposed and designed with high performance Support Vector Machines, which does not waste the system processing in switching between one queue to another. And it does not require any sorting process. This is most innovative method of using Support Vector Machines with self-learning algorithms.

Paper is designed and implemented in the different sections. A literature survey on related work is presented in Sect. 2. Framework for algorithms is given in Sect. 3. Proposed learning algorithms are discussed in Sect. 4 and tested in Sect. 5. Overall conclusion is given in Sect. 6.

2 Background

Create three dynamic vectors for three levels of queues: (i) High priority (ii) Medium priority, and (iii) Low priority. Each queue contains process details like Process id (PID), Burst time (BT) and Frequency (FQ).

When operating system calls the process from the disk, it searches the index file and learns to where each process has to be kept in which queue (High/Medium/Low) [4] (Table 1).

Table 1 The learning index file structure

Pid	Burst time
B1001	5
S1002	2
I147	6

In the above learning index file of processes *PID(S1002) > PID(I147) > PID (B1001)* because of their type of the process. Process id (Pid) is prefixed with either B-Batch process or I-Interactive Process or S-System process. So that in the above processes *S1002* is stored in *High priority queue*, *I147* is directed to Medium Priority Queue and *B1001* is available in *Low priority queue*.

Grouping of processes and storing them in respective queue (High/Medium/Low) is learned through vector learning algorithms associated with the process id(B/I/S) [5–7].

3 Proposed Framework

Declare and define machine-learning algorithms by implementing user defined classes Vector Machine and MFQS.

3.1 Vector Machine Class

This Vector Machine contains three attributes (i) *Process Id (pid)* (ii) *Burst Time, and* (iii) *Next reference* to neighbor process in the same vector (Fig. 1). To manipulate each process, it has been identified the following self-learning operations.

All these functions are learned by using existing file structure data (Table 2). These are self learning operations.

3.2 MFQS Class

The machine scheduling is done in this framework of MFQS. This contains an array of three priority queues (Table 3).

- *0th for high priority*
- *1st for medium priority*
- *2nd for low priority*

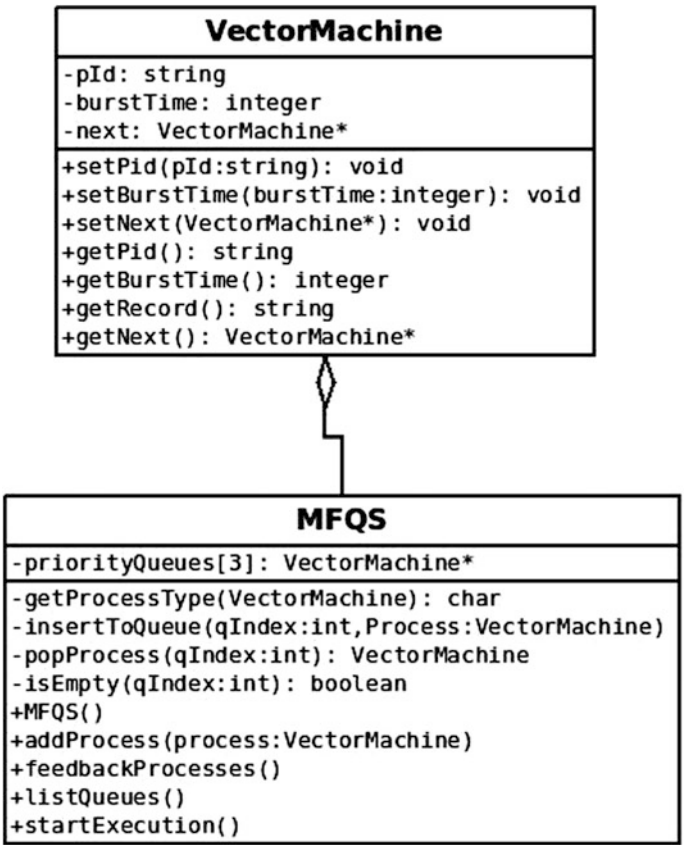


Fig. 1 Shows the frame work of Support Vectors for MFQS scheduler

Table 2 Virtual machine operations

Operation	Description
setPid()	This function sets process id
setBurstTime()	This function sets process burst time
setNext():	This function links current process to neighbor process in the Vector
getPid()	It returns process id
getBurstTime()	It returns burst time
getRecord()	This returns complete details of process in string format
getNext()	It returns neighbor process reference

Table 3 Scheduler machine MFQS operations

Operation	Description
getProcessType()	This operation recognizes the type of the process 'S'—system process, 'I'—interactive process and 'B'—batch process and returns the character
insertToQueue()	This operation is called by *addProcess()* by taking the queue index number and process to be added
*addProcess()**	This operation takes the process details to be added to vector machines
*feedbackProcesses()**	It feedback of processes will be done among medium priority to high priority and low priority to medium
listQueues()	This traverse all the vector machines (queues) and print the details of each process
IsEmpty()	It checks whether specified queue is empty or not
popProcess()	It returns the process by removing from specific vector/queue
*startExecution()**	This operation starts execution of processes in high priority vector/queue and it will use the service of feedback of process also

4 Proposed Learning Algorithms

The following operations are performed by core algorithms for this vector machine MFQS:

1. Adding process to specific Vector Machine Queue (high/medium/low)
2. Removing process from queue and assigning it to Vector Machine for execution in their order and on priority basis
3. Redirecting each process from file index entry to scheduling machine

4.1 Algorithm for addProcess(Process)

Step

1: Start
2: If getProcessType(Process) = 'S' then
3: call insertToProcess(0, process)
4: Else If getProcessType(Process) = 'I' then
5: call insertToProcess(1, process)
6: Else If getProcessType(Process) = 'B' then
7: call insertToProcess(2, process)
[End If]
8: Stop

4.2 Algorithm for **feedbackProcesses()**

Step

1: Start
2: If isEmpty(0) = true Then
3: Repeat steps 4, 5 while not isEmpty(1)
4: process = call popProcess(1) //get process for Medium priority queue
5: call insertToQueue(0, process) //add process to high priority queue
[End While]
[End If]
6: If isEmpty(1) = true Then
7: Repeat steps 8, 9 while not isEmpty(2)
8: process = call popProcess(2) //get process for low priority queue
9: call insertToQueue(1, process) //add process to medium priority queue
[End While]
[End If]
10: Stop

4.3 Algorithm for **startExeccution()**

Step

1: Start
2: set Count = 1 //this is for counting process that are executed
3: Repeat steps 4–8 while !isEmpty(0) or !isEmpty(1) or !isEmpty(2)
4: Repeat steps 5–7 while(!isEmpty(0)) //repeating for poping each process for execution
5: VectorMachine process = popProcess(0) //get process from vector queue
6: print process //processing of poped process
7: Set count: = count + 1
[End While]
8: call feedbackProcesses() //calling feedback service or operation
[End While]
9: Stop

4.4 *Algorithm for* Main Scheduler

Step

1: Start
2: Declare Scheduler
3: Open file "FileIndex.txt"
4: Repeat step 5, 6 While end of file
5: Read each process record from file
6: Call Scheduler->addProcess(process) operation
[End While]
7: Close the file
8: Call Scheduler->startExecution() operation
9: Stop

5 Test Results

These algorithms are tested with C++ simulator by taking 1000 and one lakh process records as inputs. It has been found with good performance during execution (Fig. 2).

Case #1: Input index file with 1000 process records

Case #2: Input index file with 100000 (one lakh) process records has been tested with time performance. It has been taken 1.5 min to complete one lakh records feed backing and processing (Fig. 3).

```
Process 996: B207       95
Process 997: B821       63
Process 998: B388       78
Process 999: B771       66
Process 1000: B111      6
real    0m0.045s
user    0m0.008s
sys     0m0.016s
Process returned 0
satyacomp@satyacomp-dell-3346:~/CPP/Support Vector Machines for MFQS$
```

Fig. 2 Screenshot of simulation with 1000 processes

```
Process 99996: B73027   86669
Process 99997: B55247   52999
Process 99998: B31029   38072
Process 99999: B28916   19734
Process 100000: B93187  88110
real    1m5.377s
user    0m55.376s
sys     0m1.788s
Process returned 0
satyacomp@satyacomp-dell-3346:~/CPP/Support Vector Machines for MFQS$
```

Fig. 3 Screenshot of simulation with 1 lakh processes

6 Applications

Most of real-time operating systems applications are *Event Response* applications. These applications require a response to a stimulus in a certain amount of time. It needs to be careful, when designing event response applications. There should be guaranteed response should be happened deterministically within a certain maximum amount of time. Considering the demerit of Embedded Systems/Firmwares are low multitasking, which runs few tasks (processes) and stay focused on them. But using the above Support Vector Machines in Embedded Systems/Firmwares, they can focus on many tasks (processes) instead same or few tasks (processes). Each task is classified as separate simple Vector.

7 Conclusion

In this study, most advanced scheduling algorithm of Multilevel Feedback Queue Scheduling (MFQS) performance and intelligence is improved by Machine Learning algorithm and Support Vector Machines. The tested simulation is under the conditions of open source Operating System Linux (Ubuntu14.04LTS), it might varies based on implementation conditions of other operating systems. But defined Machine-Learning algorithms are constant for implementations of any operating system. Operating systems process schedulers can adopt Machine-Learning Algorithms for processing large volumes of server and client processes. These algorithms can use any Intelligent Algorithms in Machine learning. Another important preemptive scheduling algorithm Round Robin can be designed with Support Vector Machines.

Acknowledgements We are grateful for the sincere advice and care by Andhra University, Dept of Computer Science and Systems Engineering and other superiors in achieving this research paper. The authors would like to thank Raghu Engineering College, Visakhapatnam for their infrastructural support. Our gratitude goes to the people, who previously succeeded in

implementation of General Scheduler Mechanisms, Vector Machines, Process Communication, Learning Algorithms, Event Analysis, Interrupt Handling etc., and making it available for further development.

References

1. Steinwart. I., Christmann Andreas.: Support Vector Machines. Springer Publications, ISBN: 978-0-387-77241-7, e-ISBN: 978-0-387-77242-4, DOI:10.1007/978-0-387-77242-4
2. Guang-Bin Huang Ã., Qin-Yu Zhu., Chee-Kheong Siew.: Extreme learning machine: Theory and applications. Neurocomputing 70 489–501, http://www.elsevier.com/locate/neucom (2006)
3. Akusok A., Björk. K., Miche. Y., Lendasse. A.: "High-Performance Extreme Learning Machines: A Complete Toolbox for Big Data Applications", 2169–3536, IEEE. (2015)
4. Negi A, Senior Member, IEEE, Kishore Kumar P, Department of Computer and Information Sciences University of Hyderabad.: Applying Machine Learning Techniques to improve Linux Process Scheduling. atulcs@uohyd.ernet.in, kishoregupta os@yahoo.com
5. Vaishali Chahar CSE Deptt, ITM University, Gurgaon India Supriya Raheja CSE Deptt, ITM University, Gurgaon India: "A Review of Multilevel Queue and Multilevel Feedback Queue Scheduling Techniques", Volume 3, Issue 1, January 2013 ISSN: 2277 128X International Journal of Advanced Research in Computer Science and Software Engineering
6. Itamar Arel, Derek C. Rose, and Thomas P. Karnowski The University of Tennessee, USA Deep Machine Learning—"A New Frontier in Artificial Intelligence Research", IEEE COMPUTATIONAL INTELLIGENCE MAGAZINE (NOVEMBER 2010)
7. Rakesh Kumar Yadav, IFTM University, INDIA and Anurag Upadhayay, IFTM University, INDIA - "A fresh loom for Multilevel Feedback Queue Scheduling Algorithm", International Journal of Advances in Engineering Sciences Vol. 2, Issue (3, July, 2015)

New Training Pattern for DFT-Based Channel Estimation in OFDM System

Potnuru Narayanarao, Jampana Siddartha Varma and Kasi Murali Krishna

Abstract Here, a training sequence pattern is proposed to estimate the 2-tap Rician channel for different Rician factor (K) values, in orthogonal frequency division multiplexing (OFDM) systems, using comb-type pilot arrangement. Here the estimation is done by pilot signal estimation and channel interpolation. The pilot signal estimation is done by the least squares (LS) estimator and channel interpolation by linear interpolation and spline interpolation.

Keywords Comb-type pilot arrangement · Least squares estimator · Linear interpolation · Mean square error · Rician factor · Spline interpolation · 2-tap Rician channel

1 Introduction

Orthogonal frequency division multiplexing (OFDM) is most significant wideband transmission technique for high-speed wireless data communication systems. It uses multi-carrier modulation technique [1]. Compared to other wideband transmission techniques like CDMA, OFDM combat inter-symbol interference (ISI) by dividing the entire wideband channel into multiple narrowband sub-channels, which have *overlapping* but *non-interfering* frequency spectra, thereby maintaining high data rates [2, 3].

P. Narayanarao (✉) · J.S. Varma
Department of ECE, Pydah College of Engineering and Technology, Visakhapatnam, AP, India
e-mail: narayana1student@gmail.com

J.S. Varma
e-mail: siddartha_varma@yahoo.co.in

K.M. Krishna
Department of ECE, ANITS, Visakhapatnam, AP, India
e-mail: mkasi71@yahoo.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*, Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_64

The use of multi-amplitude modulation schemes, such as QAM, in wireless digital communication systems requires channel estimation [4]. Since OFDM is operated with a number of parallel narrowband sub-carriers, it is inherent to estimate the channel in frequency domain using pilot symbols which are known to the transmitter and the receiver.

In this paper, a training pattern is proposed to estimate the channel using comb-type pilot arrangement in the DFT-based approach. Section 2 explains the basic OFDM block diagram with sufficient blocks required for channel estimation. In Sect. 3, the proposed training sequence is explained and the channel estimation process in the comb-type pilot arrangement is explained with least squares (LS) channel estimation with required interpolation methods. In general, the channel has a finite-length impulse response in the wireless OFDM systems. The cyclic prefix is used to prevent inter-symbol interference (ISI) to provide the orthogonality between the symbols, whose length is always greater than the channel length. Using this feature, the DFT-based channel estimation method is proposed.

2 System Model

Figure 1 shows the OFDM system based on training pattern (pilot)-based channel estimation. The input data which is binary data is modulated using specified modulation scheme following that the pilots are inserted between the input sequence uniformly. Then the input sequence of length, which is extended up to the length of IDFT, is converted into time-domain signal using IDFT block.

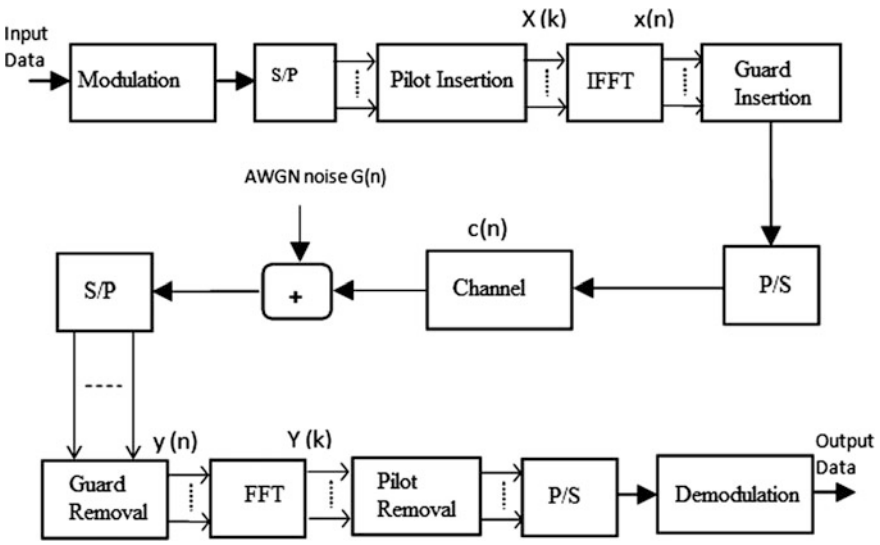


Fig. 1 OFDM system

After that, at guard insertion block, guard bits are inserted before the input information, whose length is larger than the channel delay spread and it is cyclically extended part of OFDM symbol. This guard interval is used to prevent or eliminate the ISI and ICI. The guard inserted data, $x_g(n)$, is transmitted through the Rician fading channel and after that additive white Gaussian noise, G(n), is added.

At receiver side, the output of guard removal block is sent to the DFT block. After transforming the guard removed signal from time and frequency domain, the pilot signals are extracted and H_{est}, which is an estimate of true channel, for the data bits is obtained at the channel estimation block. After the estimation, transmitted data is

$$X_{est} = \frac{Y(k)}{C_{est}(k)}, \quad k = 0, 1, \ldots (N_{fft} - 1). \tag{1}$$

Then, the resultant estimated input information is obtained as an output of "Demodulation" block.

3 Proposed Training Sequence and Channel Estimation

3.1 Proposed Training Sequence

The following training sequence [5, 6] is proposed to obtain the constant envelope of the pilot signal

$$P(n) = Ae^{j\pi n^2/N_{fft}}, \quad n = 0, 1, \ldots (N_{fft} - 1), \tag{2}$$

where A is the magnitude of the training symbols. The special property of this training sequence is that its inverse discrete fast Fourier transform (IFFT) is a chirp sequence amplitude where amplitude is constant [5]. This pilot signal has a required peak-to-average power ratio (PAPR) in time-domain processing.

3.2 Channel Estimation at Pilot Positions

In this channel estimation process, estimation is divided into estimation at pilot positions based on least squares (LS) method. In this arrangement, the N_p pilot signals are inserted into the input data uniformly according to Eq. (3). Then X(k) becomes

$$X(k) = X(mL + l) = \begin{cases} P(m), & l = 0 \\ input\_data, & l = 1 \ldots L - 1 \end{cases}, \tag{3}$$

where L is the number of sub-carriers/N_p and *m* is the number of OFDM symbols. Then the estimate of the channel at pilot positions or at pilot sub-carriers based on LS method is, as shown in (4),

$$C_{est}(k) = \frac{Y_p(k)}{X_p(k)}, \quad k = 0, 1, 2 \ldots (N_p - 1), \tag{4}$$

where N_{ps} is the spacing between pilots and N_p is the number of pilots; and $Y_p(k)$, $H_p(k)$, and $X_p(k)$ are the output value, frequency response of the channel, and input value at position of *k*th pilot sub-carrier, respectively.

3.3 Channel Estimation at Data Positions

Interpolation is used to estimate the channel at the data positions using the estimated channel information at the pilot sub-carriers. The channel estimation at the positions of data sub-carriers using linear interpolation (LI) is done using Eq. (5):

$$\begin{aligned} C_{est}(k) &= C_{est}(mL + l), \quad 0 \leq l < L \\ &= (C_p(m+1) - C_p(m))\frac{1}{L} + C_p(m). \end{aligned} \tag{5}$$

Linear interpolation generates a line between the adjacent break points and returns the point on that line corresponding to the input.

The spline cubic interpolation (SCI) gives a continuous and smooth polynomial to given data points compared to linear interpolation. Cubic spline means a third degree polynomial. So SCI fits a cubic spline to the adjacent break points and returns the point on that polynomial corresponding to that point.

3.4 DFT-Based Channel Estimation

The application of DFT on least squares with interpolation in comb-type pilot-based channel estimation improves the performance of estimators by eliminating the noise [7].

In general OFDM systems, the length of the cyclic prefix, L_c, is greater than the length of the channel impulse response. The DFT-based channel estimation uses this concept to improve the performance of the estimators. It considers the part which is larger than L_c as noise, and treats that part as zero to eliminate the effect of noise. The DFT-based channel estimation transforms from frequency to time-domain channel estimation.

The frequency-domain value of estimated channel at k^{th} sub-carrier is $C_{est}(k)$, and then its corresponding time-domain component is

$$\mathrm{IFFT}(C_{est}(k)) = c_{est}(n),\ \ n = 0, 1, 2 \ldots (N-1), \tag{6}$$

where N is the total number of sub-carriers.

To eliminate the effect of noise in the time-domain component in order to achieve better accuracy

$$c_{est}^{DFT}(n) = c_{est}(n), \quad n = 0,\ 1,\ 2 \ \ldots\ (L_c - 1). \tag{7}$$

Taking the fast fourier transform (FFT) of the $c_{est}^{DFT}(n)$ is given by

$$\mathrm{FFT}(c_{est}^{DFT}(n)) = C_{est}^{DFT}(n). \tag{8}$$

After the estimation, the transmitted data (9) is

$$X_{est}^{DFT} = \frac{Y(k)}{C_{est}^{DFT}(k)}, \quad k = 0,\ 1,\ \ldots\ (Nfft - 1), \tag{9}$$

where X_{est}^{DFT} is an estimated transmitted data with DFT-based channel estimation.

4 Simulation

4.1 Simulation Parameters

In the simulation process, we consider that the length of the guard interval or cyclic prefix is greater than the Max. delay spread in order to avoid inter-symbol interference. The lists of parameters used in channel estimation are shown in Table 1.

Table 1 Simulation parameters

Parameters	Specifications
FFT size	32
Signal-to-noise ratio	1–30 dB
Guard interval length	16 (cyclically extended type)
OFDM symbol length	80 (48 + 16 + 16)
Data bits per OFDM symbol	48
Pilot spacing	4
Number of pilots	16
Signal constellation	16-QAM
Channel model	2-tap Rician channel (Rician factor K) for K = −40 dB (Rayleigh), K = 15 dB (Gaussian)

4.2 Simulation Results

In all the plots, where the proposed training sequence is used, signal-to-noise ratio (SNR), from 1 to 30 dB, is considered on X-axis and mean square error (MSE), in dB, is considered on Y-axis.

Figures 2 and 4 give the mean square error (MSE) performance between the general LS with linear interpolation and DFT-based LS with linear interpolation for K = −40, 15 dB, respectively (Fig. 3).

Figures 3 and 5 give the MSE performance between the general LS with spline interpolation and DFT-based LS with spline interpolation for K = −40, 15 dB, respectively.

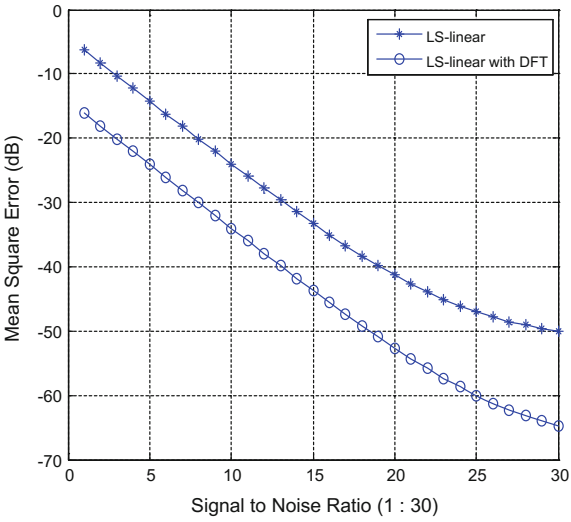


Fig. 2 MSE performance between LS—linear and DFT-based LS—linear for K = −40 dB

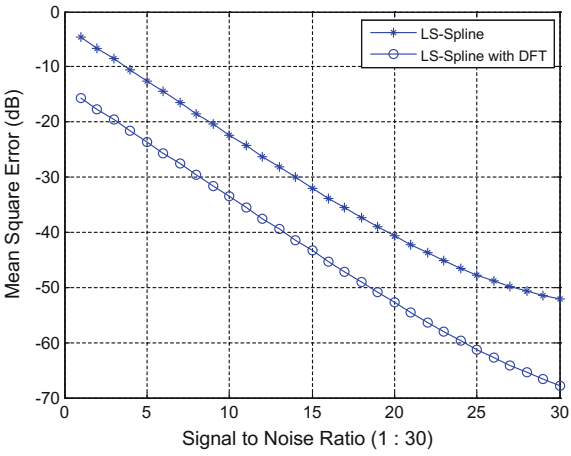


Fig. 3 MSE performance between LS—spline and DFT-based LS—spline for K = −40 dB

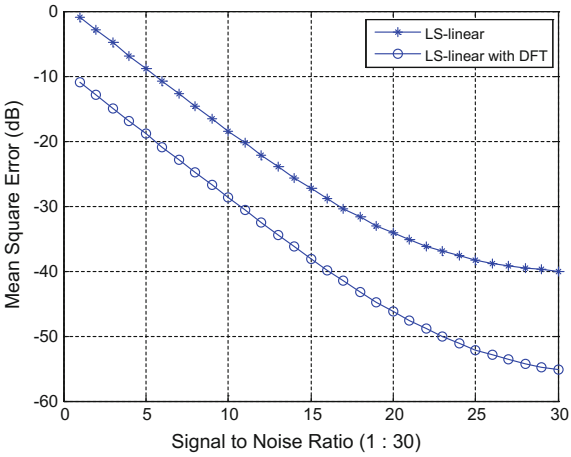


Fig. 4 MSE performance between LS—linear and DFT-based LS—linear for K = 15 dB

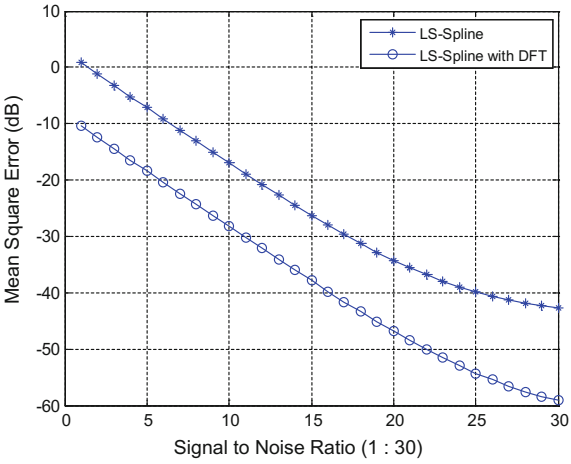


Fig. 5 MSE performance between LS—spline and DFT-based LS—spline for K = 15 dB

It is clearly observed that the simulation results are better if the estimated output is subject to DFT.

From the above, we observed that as the SNR increases, the MSE decreases in DFT-based LS-spline approach compared to DFT-based LS-linear approach.

5 Conclusion

In this, a review of DFT-based LS channel estimation with interpolation using comb-type pilot arrangement is given. In this pilot arrangement, the channel estimation at pilot positions using least squares (LS) estimator and channel estimation at data sub-carriers is done using linear and spline interpolation. Simulation results

indicate that the DFT-based approaches give 11–15 dB better compared to general estimation approaches, and the approaches based on proposed training sequence gives approximately 10 dB better results compared to conventional approaches. As signal-to-noise ratio increases LS with spline interpolation gives better mean square error than LS with linear interpolation with the proposed training sequence.

References

1. Volker Kühn, 'Wireless communications over MIMO channels, applications to CDMA and multiple antenna systems', Universität Rostock, Germany, Wiley Publications
2. Taewon Hwang, Chenyang, Gang Wu, Shaoqian Li, Geoffrey Ye Li.: OFDM and its wireless applications: A survey. IEEE Transactions on Vehicular Technology, vol. 58, No. 4, (May 2009)
3. Zhao-yang Zhang, Li-feng Lai, 'A noval OFDM transmission scheme with length adaptive cyclic prefix', Journal of Zhejiang University Science, Springer. (2004)
4. van de Beek. J. J., Edfors. O., Sandell. M., Wilson. S. K., Borjesson. P O.: On channel estimation in OFDM systems. in Proc. IEEE 45th Vehicular Technology Conference, Chicago, IL, pp. 815–819. (Jul. 1995)
5. Cioffi, J. M., Bingham, J. A. C.: A Data-Driven Multitone Echo Canceller. *IEEE Trans. Commun.*, vol. 42, no. 10, pp. 2853–2869, (Oct. 1994)
6. Murali Krishna. K., Manmada Rao. G., Nageswara Rao. M. V., Ramanjaneyulu. K., Krishna Prasad. P. M., Raja Rajeswari. K.: MIMO-OFDM channel estimation using Special Training Sequences. International Conference on Systemics, Cybernetics and Informatics, Hyderabad, India, (January, 2007)
7. Yong Soo Cho., Jaekwon Kim., Won Young Yang., Chung G. Kang.: MIMO OFDM wireless communications with MATLAB. IEEE press, John Wiley and Sons (Asia) Pte Ltd

Design and Analysis of End-to-End QAM System for Wireless Communication

Naveen Sai, K. Swetha, Ashish Singh, A. Murali, N. Markandeya Gupta and M.K. Kishore

Abstract This paper presents the performance analysis of end-to-end 256 bit quadrature amplitude-modulated signal approach using the AWR simulating software. The QAM system is designed on simulating software and their characteristics are studied such as constellation diagram, BER, EVM, and power spectrum. Further, same system has been designed on the Matlab Simulink and their parameters are compared with simulated results obtained via a AWR software.

Keywords Quadrature amplitude modulation (QAM) · Bit error rate (BER) · Constellations diagram · Additive white gaussian noise (AWGN) channel · Error vector magnitude (EVM)

1 Introduction

Communication is the process by which one can transfer its information to others through some medium. In past or primitive days, the information signal was transferred using the sound (drums) and light (fire or smoke) signals. After that, human and animal (pigeons and horses) used to take written materials for passing the information from one place to the other. These communications were not as effective as well as it was time consuming to transfer the information. Thereafter, a number of techniques were tried for the fast and successful transmission of the information. In 1792, Claude Chappe proposed the first long distance semaphore telegraph line. Later on Samuel Mores developed the long distance electric telegraph line. After that, in 1876 Graham Bell and Watson developed electric telephone [1, 2]. Further, lots of development have gone in field of communication,

N. Sai · K. Swetha · A. Singh (✉) · A. Murali · N. Markandeya Gupta · M.K. Kishore
Department of ECE, Raghu Engineering College, Visakhapatnam, AP, India
e-mail: ashsin9@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_65

now wireless communication has came into existence which comprise wireless sensor networks, mobile communication, and radio communication. In the wireless communication to transfer the information to long distance communication, there is the need of modulation signal.

For long haul communication, modulation of the signal is required. It is the process of superimposing carrier signal with a modulating signal that has data to be transmitted. In the modulation of the digital signal, discrete pulse or digital bit streams are transferred over an analog link. Basically, digital modulation techniques can be classified on the basis of keying, phase-shift keying (PSK), frequency-shift keying (FSK), amplitude-shift keying (ASK), and quadrature amplitude modulation (QAM), and are used for finite number of amplitudes, frequencies, phases, and of at least two phases and at least two amplitudes, respectively [3]. In QAM, an in-phase and a quadrature-phase signal of finite number amplitudes are modulated, and later they are summed. It is the combination of two-channel system in which both channel has ASK but second channel provides 90° phase shift in comparison of first channel. Thus the obtained signal is similar to the combination of PSK and ASK. An analog and a digital modulation scheme are applicable in QAM. It can transmit the information from two digital bit streams or analog message signals using digital modulation scheme or amplitude modulation scheme. In QAM scheme two carrier waves are of same amplitude while differed by 90° with each other. Final wave obtained at the receiver is the combination of ASK and PSK schemes. Thus, QAM scheme is one of the key modulation schemes in digital communication system. Further, QAM scheme has certain advantages such as high spectral efficiencies, limited noise level, and has linear relationship with communication channels. Due to these reasons it encourages the researchers, scientists, and telecom industries to increase the use QAM scheme in communication fields.

In past decades, lots of research work on QAM have been published such as S. W. Ho discussed on the Adaptive modulation (QAM, QPSK) scheme, further Suraweera et al. reported dual hop- asymmetric channel and investigated the probability and bit error probability of M-QAM modulations. Later on, Alam et al. analyzed the performance of non-fixed relays cooperative network by applying M-PSK and QAM signals. Further, Takpor and Idachaba analyzed LTE downlink and uplink transceiver using QAM techniques, thereafter Alhassan and Fattah studied the performance of IEEE 802.16-2004 by 64QAM techniques, after that Ghosh worked on OFDM technology and analyzed it on different modulations are 8QAM, 16QAM, 64QAM [4–11]. All this reported paper of QAM has limitation such as they have not compared the 64QAM techniques with other higher and lower QAMs and they have not compared their simulation results with other simulation tools.

In this view, 64-bit QAM scheme has been designed on AWR simulation tool and Matlab. Performance analyses of 8, 16, 64, 128, and 256 QAM are done and results are compared with higher order bits. The transmission errors in the received signal for different QAM systems are also presented.

2 QAM System Design

2.1 Matlab QAM Design

QAM systems are designed on the Matlab tool. The general QAM system is designed using QAM modulator and demodulator. The generated random integer is passed to QAM baseband modulator, and then signal is passed through channel, i.e., an additive white gaussian noise (AWGN) channel which is demodulated at QAM baseband demodulator. The analysis of signal loss is done by BER calculation after the demodulation block. Signal is compared in BER block in which it has two signals, i.e., transmitted and received signals. At the end of modulation, AWGN blocks the discrete time scatter plots which are placed, i.e., constellations diagram. Figure 1 shows the general QAM system design. Further to design 8, 16, 64, 128, 256 QAM system, modulator and demodulator blocks are replaced by rectangular 8, 16, 64, 128, 256 QAM baseband modulator that is excited by Bernoulli binary generator. Figure 2 shows the proposed 8, 16, 64 128, 256 QAM system design. In the modulator and demodulator there is an option to change 8, 16, 64, 128, 256 bit QAM and the Bernoulli binary generator sample per frame 768 for 64QAM.

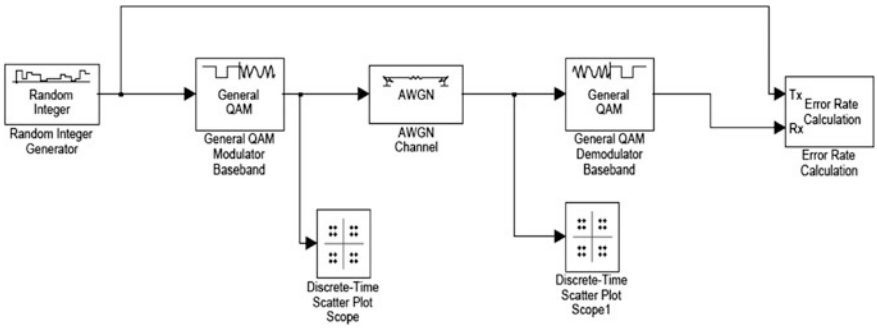


Fig. 1 QAM simulation model

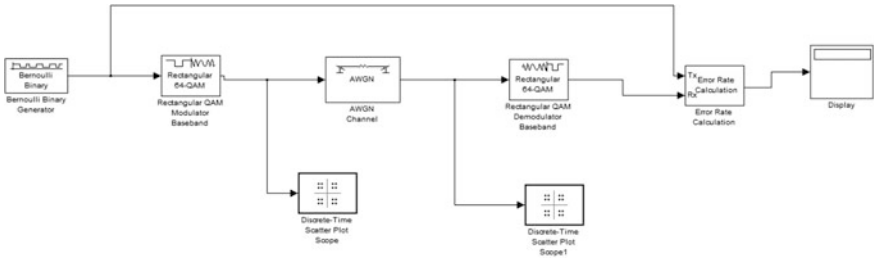


Fig. 2 64 QAM simulation model on MATLAB

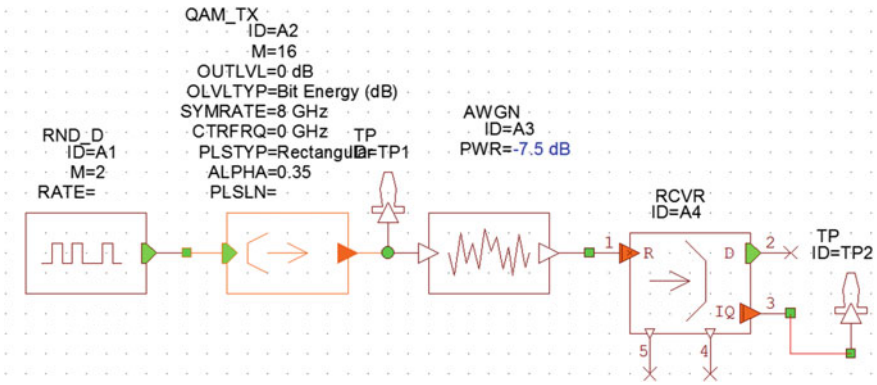


Fig. 3 General QAM system on AWR simulation tool

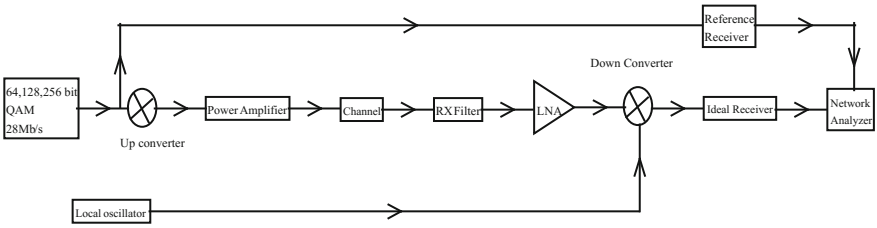


Fig. 4 64 bit, 128 bit, and 256 bits QAM system design on AWR simulation tool

2.2 AWR QAM Design

The general QAM system design on AWR simulation [12] tool is shown in Fig. 3. Design of 64, 128, 256 bits QAM system is shown in Fig. 4. The design of 64, 128, 256 bits QAM system on AWR simulation tool is complicated since designed QAM system on simulation tool are close to real world. So lots of other blocks have been used such as up converter, power amplifier, AWGN channel, receiver filter, linear amplifier, down converter, reference receiver, network analyzer, and ideal receiver.

3 Discussion of Results

3.1 Matlab Results

The analyses of QAM system performance are done with the constellation diagrams and BER. Figure 5 shows the output plot for the constellation diagrams before and after the channel. The constellation output diagrams for the 64QAM systems before the channel are as follows.

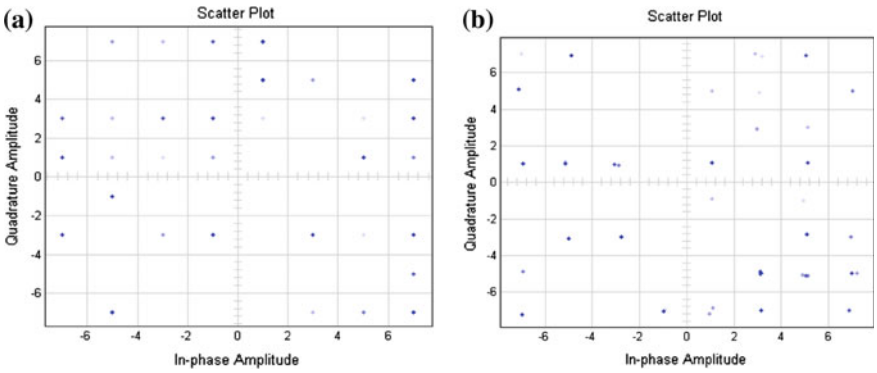


Fig. 5 **a** Constellations before channel. **b** Constellations after channel

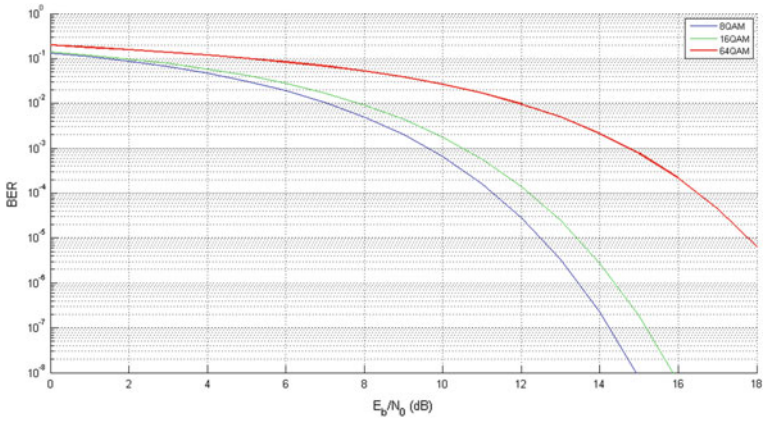


Fig. 6 BER versus SNR

Here each quadrant has 16 constellations as it is 64QAM system.

Bit error rate (BER) of communication system can define as total number of errors in receiving the bits to the total number of bits transmitted. BER curve is shown in Fig. 6 which shows the comparison of 8, 16, and 64QAM. BER = Errors/Total Number of Bits. Figure 7 shows the comparison for Simulink and theoretical plot of 64QAM system. From the figure it is observed that the both plots are in close agreement with each other.

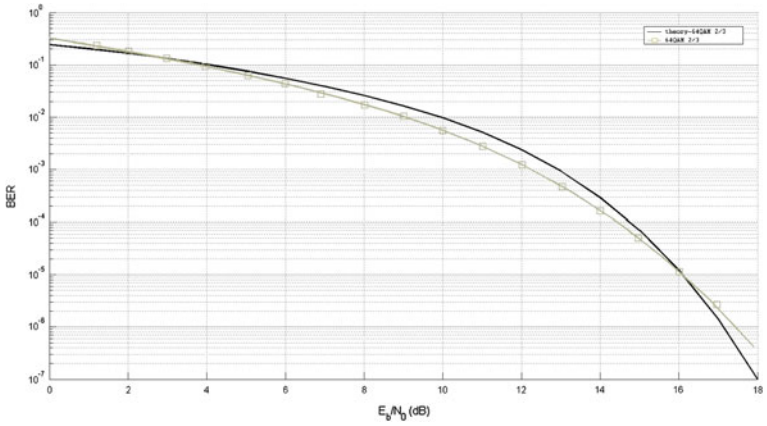
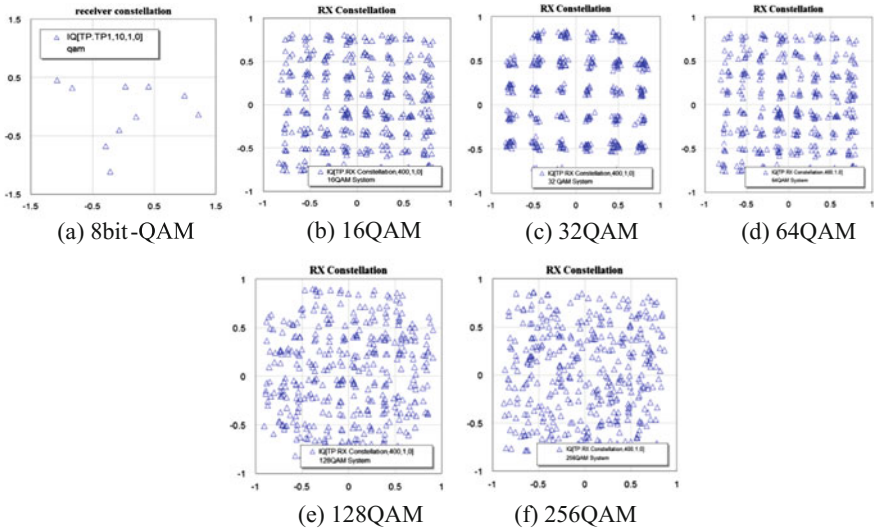


Fig. 7 Simulation result of 64QAM



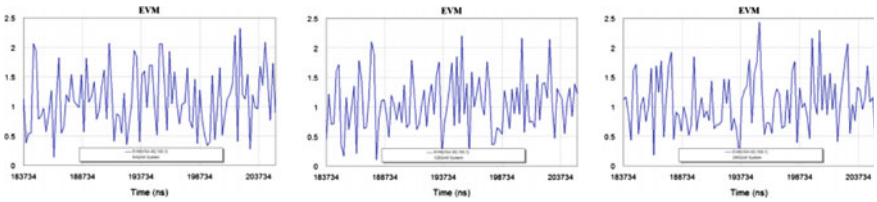
(a) 8bit-QAM (b) 16QAM (c) 32QAM (d) 64QAM

(e) 128QAM (f) 256QAM

Fig. 8 Constellation diagrams for QAM system

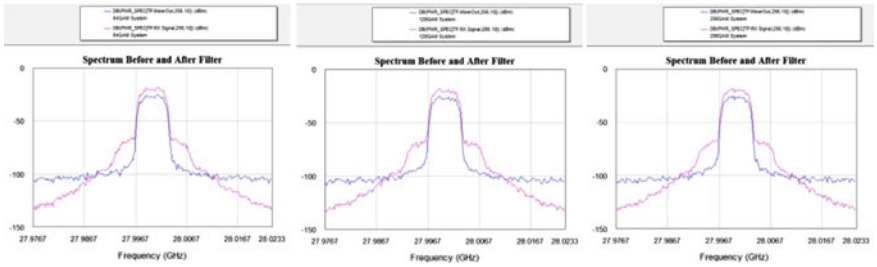
3.2 AWR Results

Figure 8a–f shows the constellation diagram 8, 16, 32, 64, 32, 64, 128, 256 bits QAM. Constellation diagram is drawn between amplitude (Y plane) and in-phase (X plane) quadrature. It represents the digital modulated signal after the channel, i.e., receiver constellation. This diagram displays the signal in two-dimensional



(a) 64QAM (b) 128QAM (c) 256QAM

Fig. 9 EVM is plotted between magnitude and time (ns)



(a) 64QAM (b) 128QAM (c) 256QAM

Fig. 10 Power spectrum before and after filter for QAM system

X–Y plane, i.e., amplitude (Y plane) and in-phase (X plane) quadrature are scattered. For 8 bits QAM constellation diagram 10 points have plotted while for 16, 32, 64, 32, 64, 128, 256 bits QAM 400 points are plotted.

Figure 9a–c shows the error vector magnitude (EVM) for 64, 128, and 256 bits QAM. Vector analyzer is used to verify the error in the QAM system.

Figure 10a–c shows the power spectrum for 64, 128, and 256 bits QAM. It shows the power spectrum of the signal in dBm with frequency (GHz) before and after the filter.

4 Conclusion

The performances of end-to-end QAM system have been analyzed. Performance analyses of QAM system have been done via a constellation diagrams, bit error rate, and power spectrum and error vector magnitude. QAM system is designed on Matlab and AWR simulation tool, and their results are studied. AWR design system is complicated, and then the Matlab design system since AWR design system is close to real-world QAM modulation system. Proposed QAM system can be used for present-day wireless communication system.

References

1. Keiser, G.: Optical fiber communications. 4th Ed. Tata Mc Graw-Hill (2008)
2. Senior, J. M.: Optical fiber communications-Principles and practice. 2nd Ed. PHI (1992)
3. Ho, W. S.: Adaptive modulation (QPSK, QAM). Intel in Communication (2004)
4. Suraweera, H. A., Karagiannidis, G. K., Smith, P. J.: Performance analysis of the dual-hop asymmetric fading channel. IEEE Transactions on Wireless Communications. vol. 8, pp. 2783–2788 (2009)
5. Alam, S., Olabiyi, O., Odejide, O., Annamalai, A.: Performance analysis of amplify-and forward relay based cooperative spectrum sensing in fading channels. International Journal of Wireless & Mobile Networks. vol. 4, (2012)
6. Takpor, Temitope and Idachaba, F. E.: Analysis and simulation of LTE downlink and uplink transceiver. Proceedings of the World Congress on Engineering, London, U.K. July 2–4 (2014)
7. Alhassan, H. A., Fattah, E. A.: A Study on the performance of IEEE 802.16-2004 includes STBC. ASEE 2014 Zone I Conference, University of Bridgeport, Bridgpeort, CT, USA, April 3–5 (2014)
8. Ghosh, S.: Performance evaluation on the basis of bit error rate for different order of modulation and different length of subchannels in OFDM system. International Journal of Mobile Network Communications & Telematics. vol. 4, No. 3, June (2014)
9. Hou, N., Niu, K. He, Z., Sun, S.: Test and performance analysis of PUSCH channel of LTE system. IEEE 5th International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications (MAPE), Chengdu, pp. 110–114, Oct. 29–31 (2013)
10. Indumathi, G., Joe, D. A.: Design of Optimum Physical Layer Architecture for a High Data Rate LTE Uplink Transceiver. Proc. IEEE Int. Conf. on Green High Performance Computing (ICGHPC). India (2013)
11. Rezaei, F., Hempel, M., Sharif, H.: A Comprehensive Performance Analysis of LTE and Mobile WiMAX. IEEE International Wireless Communications and Mobile Computing Conference (IWCMC) Limassol, Cyprus. pp. 939–944 (2012)
12. AWR Simulation software 3.2 1960 E. Grand Avenue, Suite 430 El Segundo, CA 90245 (2003)

Implementing the Reconfigurable Intelligent Sensor Interface in Wireless Networks

G. Sridevi, S. Satyanarayana and P. Sravan Kumar

Abstract To abstract and collect the sensor data, an essential media is needed which is primarily used in the Industrial wireless sensor networks in the most possible programming environments. Even these devices are available for such activities, and some factors are restricted by these devices such as the signal types of the sensors, current, etc. The programming environment needs large data collection program code. For this reason, we designed a reconfigurable sensor interface in which CPLD is embedded in the design as a core controller. It reads the data with high speed on multiple sensor data. This design is based on the IEEE1451.2 standards. It stipulates the hardware and software design framework. The system is a combination of CPLD technology and intelligent sensor specification in IEEE standards. The performance of the design is verified in the water environment in the practical application with good and effective results.

Keywords IoT · ZigBee · CPLD

1 Introduction

An emerging technology of the modern wireless communication systems has a rapid advancement and the Internet of Things (IoT) is one of the attractive application areas including the healthcare systems manufactured as in [1, 2]. Wireless sensor networks (WSN) are employed in data collection about the physical

G. Sridevi (✉) · S. Satyanarayana · P. Sravan Kumar
Department of CSE, Raghu Engineering College, Visakhapatnam, AP, India
e-mail: gaddesridevi.85@gmail.com

S. Satyanarayana
e-mail: satyacomp@gmail.com

P. Sravan Kumar
e-mail: shraonep@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_66

phenomena in many other monitoring applications [3]. These WSN systems are well suited for the long-term industrial environmental data acquisitions for IoT representations [4]. As mentioned in [5], the interface device is used for detecting the various kinds of the sensor data of the industrial WSN in IoT environments. As it enables us to acquire the sensor data, the information in the other environments can be understood easily as well.

Even though there are multiple interface equipments available in the market with matured technologies, these sensor interface devices are specialized systems, and hence they are not adaptable individually in IoT environments [6]. The CPLD is a unique hardware logical control, real-time performance, and synchronicity as in [7] which allows the parallel acquisition of multi-sensor data and improves the system performance [8]. In previous workouts, the authors came to know that MCU (Micro Control Unit) performs the task by way of interruptions, which may not really parallel in collecting the multi-sensor data. At present CPLD is more popular than MCU in multi-sensor data acquisition in IoT environment.

The data acquisition device is the key point in the industrial WSN applications [9]. To avoid the compatibility problem, the STIM interface [10] enables the sensor to search network and promotes the improvement of the WSN [11]. This interface makes our proposed device with more compatible in the field of industrial WSN in IoT environment.

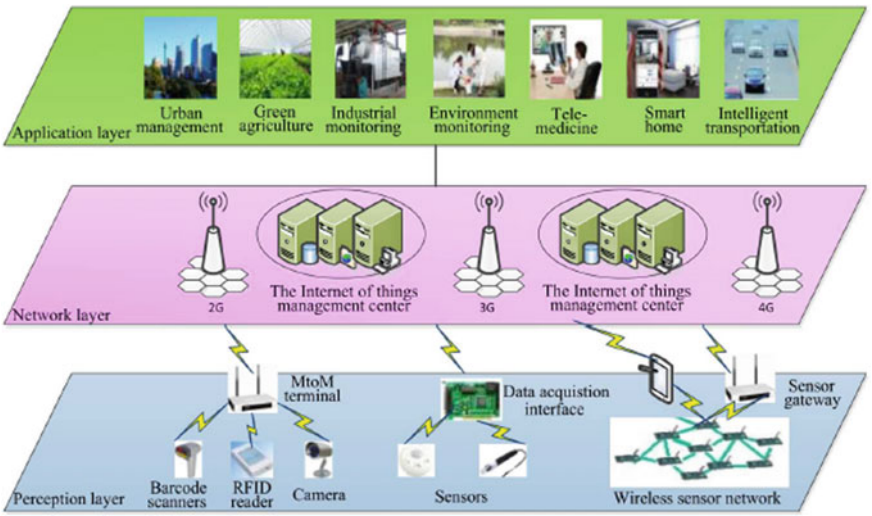


Fig. 1 Architecture of Internet of Things (IoT)

2 IoT Environment in Detail

A new trend of ubiquity is established with the various advanced internet technologies and WSNs [12]. Since IoT is associated with huge number of wireless sensor devices, it generates a large number of data [13]. The architecture of IoT is illustrated in Fig. 1.

It has three layers: Perception, Network, and the Application layers [14]. The design of the data acquisition (DA) interface is mainly employed in the first layer, i.e., perception layer of the IoT. This layer has sensors, RFID readers, cameras, M2M terminals, and various other data collection terminals as mentioned in [15].

Monitoring in the water is one of the IoT applications, where the information on the water quality in high complex measures is used to find the quality. Many other data collecting devices support the monitoring of water quality in the present market. These systems can run at high speed of DA for multiple sensors. Our design and implementation of such interface can also use for this type of environmental monitoring.

3 Architecture of CPLD

We designed the reconfigurable interface device with the combinational properties of integrating the data collections, data processing, and the wireless or wired transmission. In real-time sessions, this device can be used in IoT and WSN applications, to collect the various kinds of sensor data. CPLD is designed such that it is programmed with IP core model with the corresponding available protocol. Hence, the device can automatically discover the sensor connections and can collect the multiple sets of the sensor data intelligently with high speed. The proposed approach can be achieved with the wired connections through Universal Serial Bus (USB) interface and the wireless communication through the ZigBee module. For this, we have chosen special mode of transmission in the various industrial application environmental developments.

Figure 2 describes the reconfigurable smart sensor interface device process of working. Practically, this device then collects the analog signal transmitted from color sensors, light intensity, and other similar sensors through the analog signal interface. It collects the digital signal transmitted from the digital sensors too through the digital signal interface.

CPLD can control both the analog-to-digital converter (ADC) and signal interface as it is a core controller, as it is possible to collect the 8-channel analog signals and 24-channel digital signals circularly, and sets these collected data into the integrated SRAM. The transmission of this collected data is done at host computer through USB as we achieved through the serial-wired or ZigBee network, and thus the user can analyze and process the data.

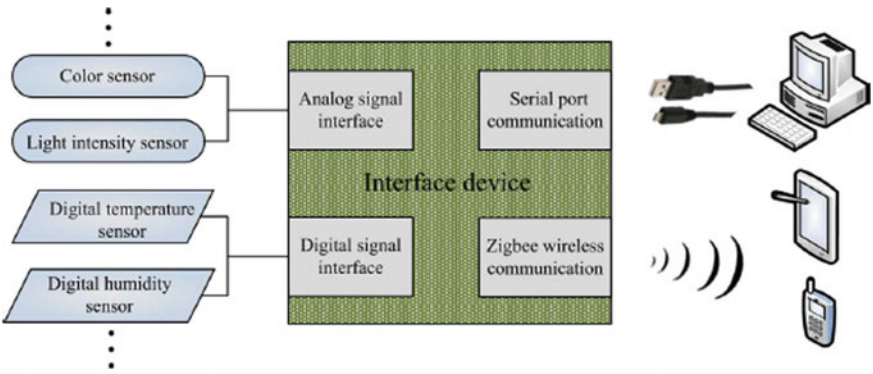


Fig. 2 Intelligent interface device

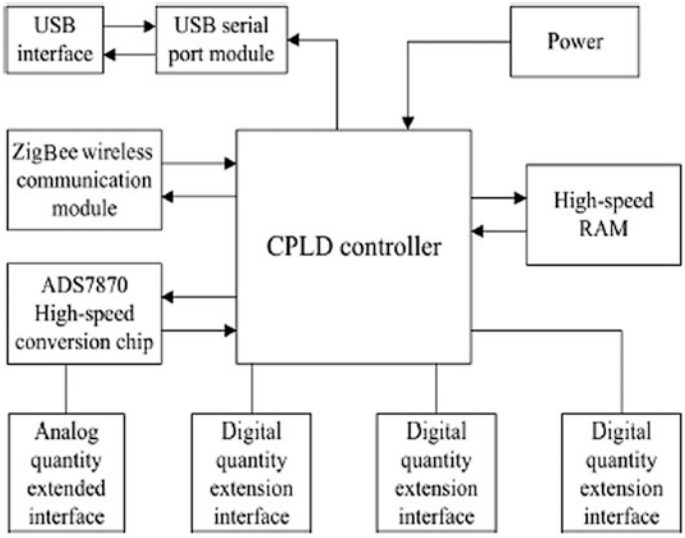


Fig. 3 Block diagram of CPLD controller

4 Implementing the Device Structure

The structure consists of CPLD chip, crystals, communication circuit (PL2303HXC), 1.8 and 3.3 V of power supply, SRAM memory (TC55V400 chip), LED indicator light, and analog and three digital extended interfaces. These interfaces can be connected to the independent sensors (8). The reconfigurable smart sensor interface device can access these 8 analog and 24 digital signals. Figure 3 shows the block diagram of CPLD.

The hardware system sends data to control center via USB serial port or wireless module and receives the information by the sensor data acquisition. ZigBee is the wireless communication module that connects with mini USB interface or extensible GPIO interface. ZigBee is also used as transceiver node, when the main controller receives the trial or executive instructions [16]. The running status of the device is controlled by the data communication function. It feedbacks the actions after it ends the processing of the received data, to the sensor interface device.

5 Application in Detail

As the environmental monitoring has the higher requirements for the equipment and used for the more complex environmental information, it has become popular and an important aspect using the WSN applications in the IoT environments [17]. As in this example application, we need to grab the information from the water environmental information of all kinds with accuracy. At present, this has got many disadvantages like design complexity, expensive, and bulkiness. Hence, it is not suitable for monitor the individual or small organizations. It mainly includes the following aspects.

- Purity, internal, and external temperature of the water can be monitored. The concentration, light intensity, is also to be maintained on the water surface.
- Multiple nodes can be distributed in various areas in the pool of water.
- Battery with low power supply can also be adjusted for accessing the power to the system.

To maintain the quality of the water in the pool, the hardware and the software designs are detailed as follows.

1. Hardware design: This is the CPLD-based reconfigurable interface device. All the above-mentioned requirements can be possible with this design. At first, hardware sensors are arranged such that it should be able to collect the required data. In the second step, wireless module which is known as ZigBee is connected to the circuitry device to send and receive the data. And finally, the battery of 1.8 V is arranged that can work for more than 10 h.

Figure 4 shows the functional block diagram of the design.

After combining all the above hardware, it satisfies all the characteristics such as low power consumption, low cost, and less volume. This design works more flexible and in convenient manner.

This suits for the water quality projects more often. For achieving low-cost levels, the system collects multiple data sets from various nodes and monitors the entire water quality environment. Figure 5 shows the exploration of the hardware of the water quality monitoring.

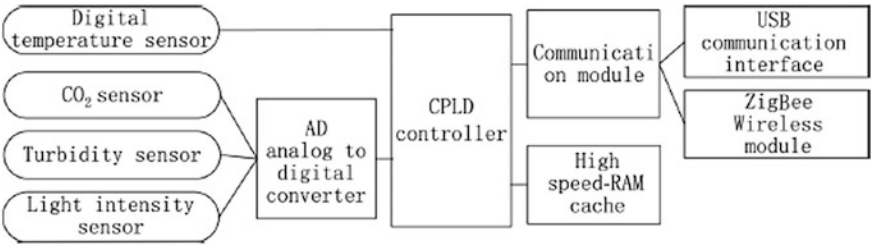


Fig. 4 System's block functional design

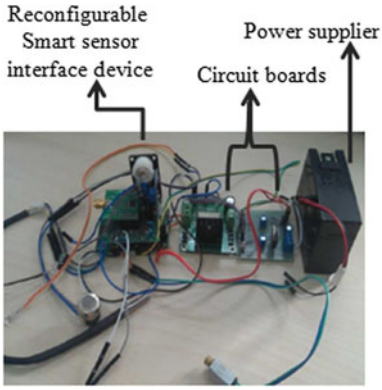


Fig. 5 Water quality monitoring hardware equipment

2. Software design: It includes mainly two parts: First, HDL programming is used based on the CPLD, for controlling the sensor data acquisition and communicational process. The modular grouping mode is established in various modules for further development. Primarily, implementing the functions in the process and summarizing these functions fulfill the original instantiation, and next by modifying the data format in spreadsheets according to the systems. Thus the difficulty in modifying such programs can be solved. A software client is then programmed to send the control signals and receives collected data and is displayed in the window. In this way, data displayed in the serial debug terminal is achieved. The collected data from the text is 16 hexadecimal form. This is in the form of

$$0xFD + data\ length + target\ address + data.$$

The data bits with unconnected to the sensors are displayed as 00. After the sensor connects, the system searches for data format automatically through the predefined interface and corresponding relation to the spreadsheet. Finally, the transformed data is then displayed on the port terminal.

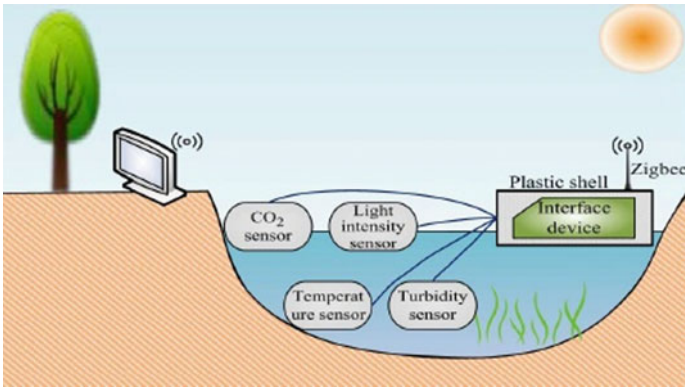


Fig. 6 Schematic picture of monitoring equipment installation

Table 1 Sensor specifications

Sensor name	Sensor type
Temperature sensor	DS18B20
Temperature and humidity sensor	SHTxx series
CO_2 sensor	MG 811
Light intensity sensor	GY-30
Turbidity sensor	KIE-TS-300B
Pressure sensor	MPX5999D
PH sensor	YBK10-WQ201

The actual effective evaluation of the water monitoring service includes monitoring of the water turbidity, temperature, and carbon dioxide on the water level. The circuitry design is arranged in the pool for a clear measurement that results in the temperature and turbidity on the water surface. The light intensity sensor and the carbon dioxide sensor should be open above the water. Now, it seems like the entire equipment is covered with a water proof shell for the processing. For a clear idea, we display the schematic picture of monitoring equipment installations in Fig. 6.

The system immediately collects the sensor data when the power supply is passed. The designed system is more compatible for different types of sensors. Hence, the practical testing methodology for different sensors has got successful achievements.

The sensor specification types are given in Table 1.

6 Conclusion

In this paper, we introduced the reconfigurable interface with smart sensor for the industrial WSN in IoT environment. The system is designed in such a way that it can collect the sensor data intelligently since the IEEE1451 protocol is embedded

with CPLD and wireless communication applications. This can be used mostly in the real-time cases in the high-speed data acquisition system in IoT environments. The CPLD application is a simplified design of the peripheral circuit which is having more flexibility and extensibility. Other types of sensors are also be used when the system is connected. With the water environmental application in the IoT environment, the system is thus verified and achieved the good effective results in the practical application.

References

1. He. W., Yan. G., Xu. L.: Developing vehicular data cloud services in the IoT environment, IEEE Trans. Ind. Informat., vol. 10, no. 2, pp. 1587–1595, (2014)
2. Fan. Y., Yin. Y., Xu. L., Zeng. Y., Wu. F.: IoT based smart rehabilitation system. IEEE Trans. Ind. Informat., vol. 10, no. 2, pp. 1568–1577, (2014)
3. Wang. L., Xu. L. D., Bi. Z., Xu. Y.: Data cleaning for RFID and WSN integration. IEEE Trans. Ind. Informat., vol. 10, no. 1, pp. 408–418, (Feb. 2014)
4. Lazarescu. M. T.: Design of a WSN platform for long-term environmental monitoring for IoT applications. IEEE J. Emerg. Sel. Topics Circuits Syst., vol. 3, no. 1, pp. 45–54, (Mar. 2013)
5. Xu. L.: Introduction: Systems science in industrial sectors. Syst. Res. Behav. Sci., vol. 30, no. 3, pp. 211–213, (2013)
6. Benini. L.: Designing next-generation smart sensor hubs for the Internet of Things. in Proc. 5th IEEE Int. Workshop Adv. Sensors Interfaces (IWASI), p. 113. (2013)
7. Chen. Y., Dinavahi. V.: Multi-FPGA digital hardware design for detailed large-scale real-time electromagnetic transient simulation of power systems. IET Gener. Transmiss. Distrib., vol. 7, no. 5, pp. 451–463, (2013)
8. Dafali. R., Diguet. J., Creput. J.: Self-adaptive network-on-chip interface, IEEE Embedded Syst. Lett., vol. 5, no. 4, pp. 73–76, (Dec. 2013)
9. Li. S., Da Xu. L., Wang. X.: Compressed sensing signal and data acquisition in wireless sensor networks and internet of things. IEEE Trans. Ind. Informat., vol. 9, no. 4, pp. 2177–2186, (Nov. 2013)
10. Hanzalek. Z., Jurcik. P.: Energy efficient scheduling for cluster-tree wireless sensor networks with time-bounded data flows: Application to IEEE 802.15. 4/ZigBee. IEEE Trans. Ind. Informat., vol. 6, no. 3, pp. 438–450, (Aug. 2010)
11. Lee. K. C., et al. IEEE-1451-based smart module for in-vehicle networking systems of intelligent vehicles. IEEE Trans. Ind. Electron., vol. 51, no. 6, pp. 1150–1158, (Dec. 2004)
12. Kelly. S. D. T., Suryadevara. N., Mukhopadhyay. S. C.: Towards the Implementation of IoT for environmental condition monitoring in homes. IEEE Sensors J., vol. 13, no. 10, pp. 3846–3853, (Oct. 2013)
13. Zhou. J., et al.: An efficient multidimensional fusion algorithm for IoT data based on partitioning. Tsinghua Sci. Technol., vol. 18, no. 4, (Aug. 2013)
14. Li. L. et al.: The applications of WIFI-based wireless sensor network I n internet of things and smart grid in Proc. 6th IEEE Conf. Ind. Electron. Appl. (ICIEA), pp. 789–793. (2011)
15. Bi. Z., Xu. L., Wang. C.: Internet of Things for enterprise systems of modern manufacturing. IEEE Trans. Ind. Informat., vol. 10, no. 2, pp. 1537–1546, (2014)
16. Cheong. P. et al., "A ZigBee-based wireless sensor network node for ultraviolet detection of flame," IEEE Trans. Ind. Electron., vol. 58, no. 11, pp. 5271–5277, (Nov. 2011)
17. Salvadori. F. et al.: Monitoring in industrial systems using wireless sensor network with dynamic power management, IEEE Trans. Instrum. Meas., vol. 58, no. 9, pp. 3104–3111, (Sep. 2009)

Design of a Low-Power Low-Kickback-Noise Latched Dynamic Comparator for Cardiac Implantable Medical Device Applications

Nadhindla Bala Dastagiri, Kakarla Hari Kishore, Vinit Kumar Gunjan and Shaik Fahimuddin

Abstract This brief presents a new architecture of dynamic latched regenerative comparator that suited for the cardiac implantable medical device applications. In this proposed architecture, the comparator is designed with low transistor count to reduce power dissipation. Also the proposed comparator has a positive feedback mechanism for achieving low kickback noise and high resolution. It is shown that the generated kickback noise is reduced a lot when compared with the other existing architectures. The proposed comparator is designed with an additional circuitry that provides extra shielding between the nodes of input and output to reduce the generation of kickback noise. The presented work is simulated using Mentor Graphics tools in 130 nm technology. The proposed work is designed well to suit the functionality with supply voltages ranging from 450 mV to 1 V.

Keywords Cardiac implantable medical device applications · Low transistor count · Kickback noise · Comparator

1 Introduction

Cardiac implantable medical devices like wearable ECGs and pacemakers equip great favourable features to the patient's life with regard to various clinical opportunities and also give crucial information for the study and diagnosis of

N. Bala Dastagiri (✉) · K. Hari Kishore
KL University, Vaddeeswaram, Guntur, India
e-mail: baluece414@gmail.com

K. Hari Kishore
e-mail: kakarla.harikishore@kluniverity.in

V.K. Gunjan · S. Fahimuddin
Investigators, DST-SERB & AITS, Rajampet, India
e-mail: vinitkumargunjan@gmail.com

S. Fahimuddin
e-mail: fahim6285@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_67

cardiac conditions. As the cardiac IMDs are inserted in the heart, they influence the daily life of the patient and it is reduced dramatically. In fact, the cardiac IMDs have to be implanted in the heart through a risky surgery and it is very expensive [1]. The life time of battery operated implantable device is very crucial and it has to work for more than 5 years in order to avoid repeated surgeries. Therefore, for extending the life time of the devices, the focus is on designing of low-power systems [2].

The low-power electronic systems have to be effective in both power consumption and silicon area. When compared with all the electronic components present in cardiac IMDs, analog-to-digital converter is the effective component and consumes majority of the power as it is required to convert the analog cardiac signals to digital data continuously. The band width for cardiac signals will be in the range of few kilohertz. Therefore, for the conversion of the low-frequency cardiac signals, it does not require a high-speed data converter, but requires a low-power operation [3–5].

In an ADC, comparator plays a crucial role in providing a tradeoff among accuracy, conversion speed, resolution, design complexity and power efficiency. Nowadays, there is huge demand for designing complex systems with low battery size, that is, pushing the design engineers to work at advanced technology with low-power dissipation. But the leakage currents and tunnelling effects became a huge concern for the designers as they degrade the efficiency of the system. Also comparators suffer from lower supply voltages as their threshold voltages are not scaled to the same extent of supply voltages in CMOS process. Therefore, it is challenging to design a low-power dynamic latched comparator at low supply voltages [6–8].

In this brief, a new dynamic latched comparator for cardiac IMDs is designed using 130 nm technology in Mentor Graphics EDA tools. In the design of the comparator, leakage power consumption, kickback noise and offset voltage will become crucial parameters. This work starts to deal with a new design methodology to answer design issues. The main objective of this is to design a comparator with low transistor count in order to achieve high degree of simplicity without comprising performance.

The remaining part of the brief is organized as follows. Section 2 describes the existing architectures of conventional latched comparators. In Sect. 3 the new architecture of latched dynamic comparator is proposed. Implemented simulation results are discussed in Sect. 4. Section 5 draws the conclusion.

2 Existing Architectures of Latched Dynamic Comparators

Latched dynamic comparators have found a number of applications in biomedical field since they can make accurate and efficient decisions due to the positive feedback present in the regenerative latch.

2.1 Conventional Single-tail Latched Comparator

The schematic diagram of existing latched dynamic comparator architecture is depicted in Fig. 1. The functionality of the comparator is as follows. In the reset phase of the latched comparator when the clock input is equal to zero (clk = 0), Mtail transistor is in off state and reset transistors M7 and M8 pull the output nodes outp and outn to a voltageVDD. During the comparison phase of the comparator, when the clock input is equal to VDD, transistors M7–8 will be in off state and transistor Mtail will be in on state. Therefore, the outputs that are pre-charged to VDD tend to discharge at different rates depending on their applied input voltages. If CINP > CINN, the node outb discharges quickly when compared with outb, and therefore outb reaches to VDD-Vthp well before outa, in turn the corresponding PMOS M5 will be in on state and thus initiating the regeneration of the latch caused due to the connection of back-to-back inverters (M3–M5 and M4–M6). Hence, the node outa is pulled to VDD voltage and outn is discharged to 0 V.

In general, this architecture of latched comparator has a benefit of rail-to-rail output swing, high input impedance, low static power consumption and also noise efficient. Although there are numerous advantages, conventional single-tail latched comparator suffers from certain disadvantages. First, it is difficult to assure that all MOS transistors are working properly, as there is too many stacking of transistors. Second, due to the fast switching action of the latch, comparator suffers from high kickback noise [9–11].

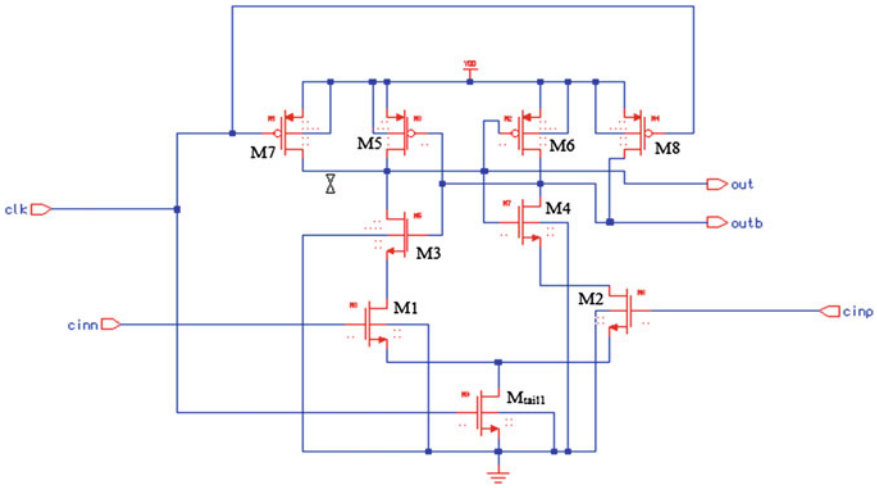


Fig. 1 Conventional single-tail latched comparator

2.2 *Double-tail Latched Comparator*

Double-tail latched comparator is described in Fig. 2. It functions mainly in two phases. In reset phase, when the clock input is low, current source transistors M5 and M12 are in OFF state and hence no static power is dissipated. The transistors M3 and M4 are in ON state resulting in the output nodes to be charged to VDD. In the regeneration phase of the comparator, the current source transistors Mtail1 and Mtail2 are in OFF state. Therefore, the outputs outn and outp will be discharged at different rates in corresponding to their inputs. The regenerative latch provides the positive feedback mechanism, propelling one of the outputs to 0 V and the other output node to VDD.

Double-tail latched regenerative comparator has less stacking of transistors resulting with the operation of lower supply voltages. The transistors MR1 and MR2 offer extra shielding between the input nodes and output nodes of the comparator, resulting in the reduction of kickback noise [9, 11].

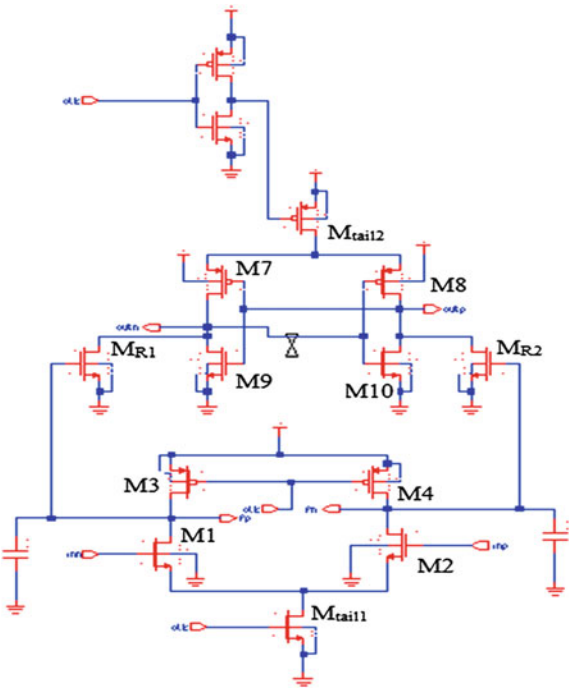


Fig. 2 Conventional double-tail latched comparator

3 Proposed Latched Regenerative Comparator

The architecture of proposed latched regenerative comparator is described in Fig. 3. The transistors M6–M8–M9–M12 form a cross-coupled regenerative latch, which is responsible for providing positive feedback mechanism in the comparator. This comparator functions in a mode, that is, in reset mode when clock input is VDD, and the transistors M2–M5–M11–M7–M10 will be in ON state determining both the output nodes VOP and VON to 0 V and also there exists no supply current in the comparator. During the evaluation mode of the comparator, that is, clock input is 0 V, the drains of the transistors M3–4 tend to regenerate the latch depending on their input voltages. With respect to the given input the cross-coupled inverters M6–M12 and M8–M9 are responsible for generating more current, thus providing the final output of the comparator where one of the nodes is pulled to VDD and the

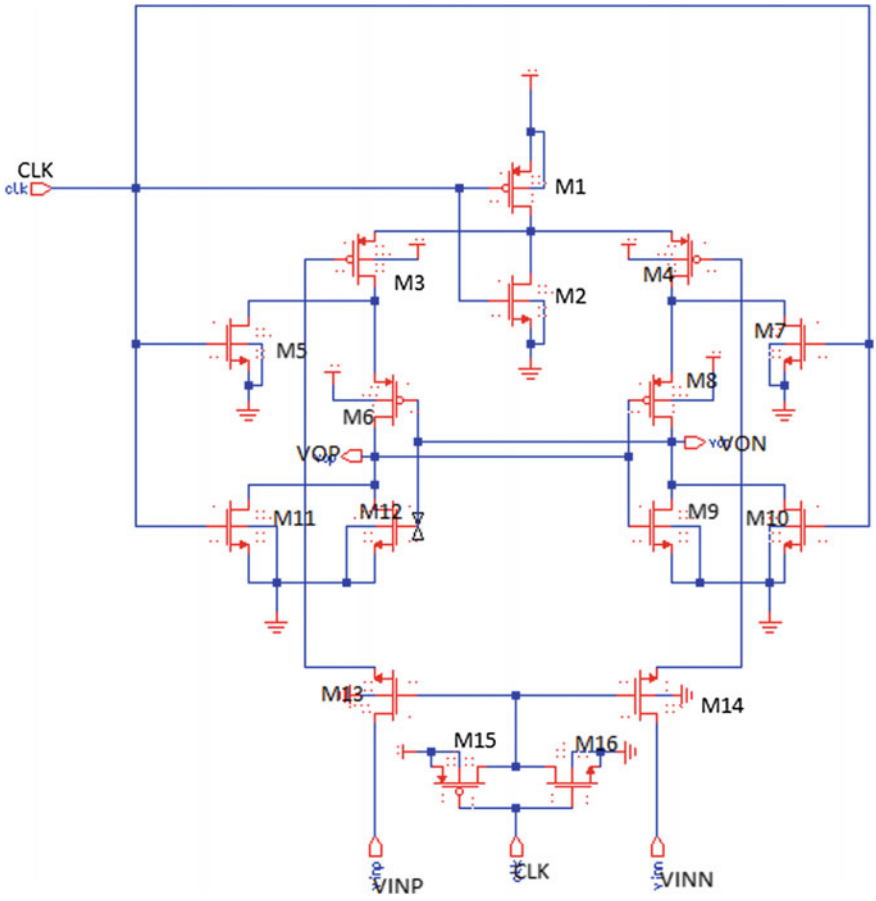


Fig. 3 Architecture of proposed latched regenerative comparator

other to 0 V. The drains of the input nodes M3 and M7 have a rail-to-rail movement resulting in the kickback noise generation. In this proposed architecture, to cancel out the generated kickback noise, an additional circuitry M13–16 is designed to provide isolation at the inputs of the transistors, that is, offering shielding between the output and input nodes of the comparator by reducing the kickback noise [12]. During the reset phase, the kickback noise reduction circuit will be in OFF state and in regeneration phase, the proposed circuitry provides the required isolation to reduce the kickback noise.

For any dynamic latched regenerative comparator, input offset voltage is the important performance metric that directly affects the system performance. As the technology scales, the input offset voltage tends to get worsened due to the process variations in the devices. Generally, the offset voltage is generated due to the variations in current factor, parasitic capacitances and threshold voltages. For the proposed comparator, the common mode input voltage is at the mid rail voltages, and thus the offset voltage of the proposed compared will be the static offset voltage. The non-ideal primary limitation on the proposed comparator is the thermal noise in the form of KT/C. For the proposed comparator, the input offset voltage is based on the Gaussian distribution and its corresponding standard deviation $\sigma os = \Delta VIN_{min}/\sqrt{2}\ \mathrm{erf}^{-1}(2Y-1)$. For reducing the power dissipation the proposed comparator is designed with less number of transistors.

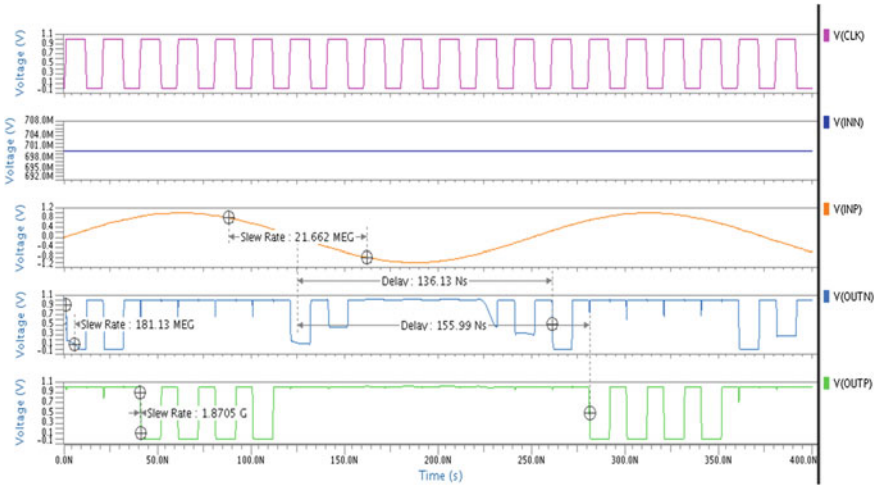


Fig. 4 Transient response of proposed dynamic regenerative latched comparator

4 Simulation Results and Discussions

In this segment of the brief, the simulation results of proposed dynamic comparator are presented graphically and the comparison summary of proposed dynamic comparator is tabulated. For simulation purpose, AMS (Eldo) simulator tool is used. It is the one of the products of Mentor Graphics EDA tools and for viewing the waveforms, EZ wave analyzer is used.

Figure 4 shows transient response of the proposed dynamic comparator for the input specification of Vinp = 1 V amplitude sinusoidal wave with frequency of 4 MHz, Vinn = 0.5 V constant reference voltage and Clk = 1 V with pulse waveform with time period of 20 nsec.

DC response of proposed dynamic comparator is shown in Fig. 5. For this, the input specifications given are both the inputs given with constant 0 V supply and one input which is set to sweep from −1 to +1 V with step division of 0.01 V. DC response helps to check the comparator characteristics and gives the offset voltage of comparator.

From Table 1, it is evident that the proposed comparator uses less number of transistors for power saving and it dissipates low power and generates less kick-back. Even though single-clock-phase dual-rail comparator is designed with less number of transistors, it generates more kickback noise and suffers from more input offset voltage when compared with the proposed work.

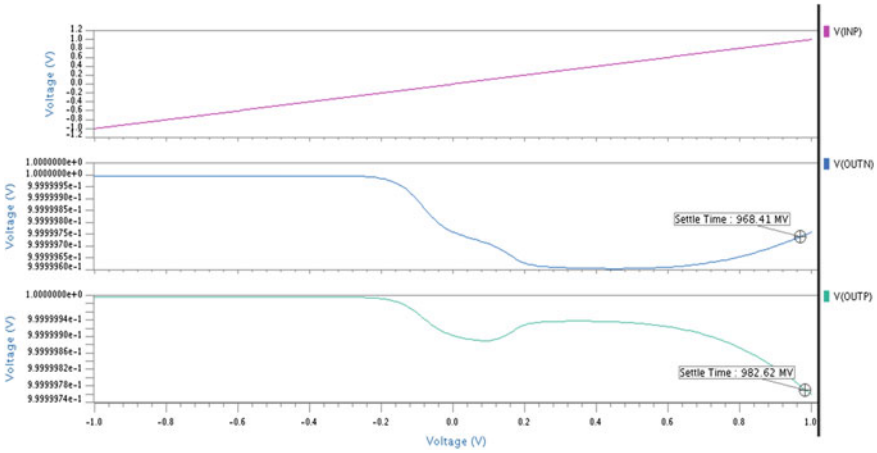


Fig. 5 DC response of proposed latched dynamic comparator

Table 1 Comparison

Comparator architectures	Transistor count	Power dissipation (nW)	Kickback noise (mV)	Offset voltage (mV)
Balanced latched comparator [13]	**24**	2.6319	1767.6964	**31**
Single–clock-phase dual-rail latched comparator [14]	**13**	1.1370	1145.2952	**32**
Dynamic regenerative latched comparator with SR latch [15]	**17**	6.0143	993.4096	**35.1**
Proposed comparator	**16**	**2.59**	**608.002**	**34**

5 Conclusion

Herein, a new architecture of the dynamic latched regenerative comparator designed with low transistor count is presented. The presented architecture of the comparator works well in the range of supply voltages 450 mV to 1 V. In order to check the efficiency of the proposed work, the results are compared with the existing architectures of comparators in cardiac IMDs. The simulation results show that the proposed architecture of dynamic comparator generates less kickback and also dissipates moderate power when compared with other works used in cardiac IMDs. Due to the additional circuitry, the kickback noise is reduced to 30% when the input supply voltage is 1 V. The proposed work is carried out using Mentor Graphics EDA tools in 130 nm technology.

Acknowledgements This work is sponsored by the Annamacharya Institute of Technology and Sciences, Rajampet, Andhra Pradesh, India and KL University, India. The authors would like to thank Dr. S. Fahimuddin and S. Seshadri for their mind stimulating discussions.

References

1. Anantha P. Chandrakasan, Naveen Verma and Denis C. Daly, "Ultralow- Power Electronics for Biomedical Applications" Annu. Rev. Biomed. Engg. 2008., April 2008.
2. W. H. Maisel, M. O. Sweeney, W. G. Stevenson, K. Ellison, and L. M. Epstein, BRecalls and safety alerts involving pacemakers and implantable cardioverter-defibrillator generators, J. Amer. Med. Assoc., vol. 286, pp. 793–799, 2001.
3. J. G. Webster, *Medical Instrumentation Application and Design*. New York, NY, USA: Wiley, 1998.
4. M. Malik, T. Cochrane, D. W. Davies, and A. J. Camm, Clinically relevant computer model of cardiac rhythm and pacemaker/heart interaction, Med. Biol. Eng. Comput., vol. 25, no. 5, pp. 504–512, 1987.
5. P. Gerrish, E. Herrmann, L. Tyler, and K. Walsh, "Challenges and constraints in designing implantable medical ICs," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 435–444, Sep. 2005.
6. B. Razavi, Design of Analog CMOS Integrated Circuits (McGraw-Hill, New York, 2001).

7. J. Yoo, D. Lee, K. Choi, A. Tangel, Future-Ready Ultrafast 8 Bit CMOS ADC for System-on-Chip Applications. IEEE 14th Annual IEEE International ASIC/SOC Conference, September 2001, pp. 455–459.
8. P. Nuzzo, F. De Bernardinis, P. Terreni, G. Van der Plas, Noise analysis of regenerative comparators for reconfigurable ADC architectures. IEEE Trans. Circuits Syst. I 55(6), 1441–1454 (2008).
9. S. Babayan-Mashhadi and R. Lotfi, "Analysis and design of a low-voltage low-power double-tail comparator," IEEE Transactions on Very Large Scale Integr. (VLSI) Syst., [Online]. Available: http://dx.doi.org/10.1109/TVLSI.2013.2241799.
10. Pedro M. Figueiredo and Joao. C. Vital, "Kickback Noise Reduction Techniques for CMOS Latched Comparators," IEEE Transactions on Circuits and Systems-II, Vol. 53, No. 7, July 2006.
11. Ka-Meng Lei, Pui-In Mak, Rui P. Martins, "Systematic Analysis and Cancellation of Kickback Noise in a dynamic Comparator", Analog Integrated Circuits and Signal Processing, Vol. 77. pp. 277–284.
12. S. Kim and M. Song, "An 8-bit 200MSPS CMOS A/D converter for analog interface module of TFT-LCD Driver," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2001, vol. 1, pp. 528–531.
13. Zhangming Zhu, and Yuhua Liang, "A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC inv0.18um- CMOS for Medical Implant Devices", IEEE Journal of solid state circuits, Vol. 62, No-9, and September 2015.
14. Howard Tang, Zhuo Chao Sun, Kin Wai Roy Chew and Liter Siek, "A 5.8 nW 9.1-ENOB 1-kS/s Local Asynchronous Successive Approximation Register ADC for Implantable Medical Devices", IEEE Transactions on Very Large Scale Integration (VLSIz) Systems.
15. Dai Zhang, Ameya Bhide, Atila Alvandpour, "A 53-nW 9.1-ENOB 1-KS/s SAR ADC in 0.13um CMOS for Medical Implant Devices", IEEE Journal of solid state circuits, Vol. 47, N0-7, and July 2012.

A Lecture Notes on Cognitive-Based Radio Ad Hoc Networks

C.V. Subhaskara Reddy

Abstract CRAHN routing metric will play a vital role in selecting the best path for forwarding the data packets across the secondary users (SUs) in a network under various network situations like multicasting, real-time QOS, dynamic topology/scalability, etc. To improve CRAHN routing performance, one has to acquire the complete knowledge about Cognitive Radio Ad Hoc Network architecture, requirements, and its challenges. An attempt has been made in this paper by comparing with classical multi channel/hop Ad Hoc network because of its similarities with CRAHN. The routing issues, challenges, and routing metric considerations that enhance the performance are discussed.

Keywords CRAHN · Cognitive radio · Ad hoc network · QOS

1 Introduction

With the ever growing interest for new wireless high speed/data-rate interest uses and services the spectrum requirement is growing exponentially in wireless networking. This augmentation needful for bandwidth and spectrum scarcity in some frequency bands along with their under use has lined the way toward dynamic spectrum allocation (DSA) policies for efficient utilization of radio spectrum in wireless networks. The exponentially growing demand for wireless connectivity results into the spectrum scarcity since much of the usable spectrum has already been allocated to certain services.

Recently, the FCC and other organizations such as the Defense Advance Research Projects Agency (DARPA) have shown that the large portions of the licensed spectrum bands are abundantly underutilized. More specifically, the measurements showed that the licensed spectrum is underutilized for 15–85% of

C.V. Subhaskara Reddy (✉)
Department of ECE, Santhiram Engineering College, Nandyal, AP, India
e-mail: Subaskar.reddy@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_68

the time duration, based on the spatial location. Other measurement studies conducted by academic and/or industrial organizations have shown similar trends.

2 Cognitive Radio Networks—An Overview

Dynamic spectrum allocation (DSA) refers to the communication standards in which the communicating devices with dynamism use the spectrum bands that are not utilized by the primary wireless services approved to work over in their bands. DSA must not disturb the performance of a licensed service by immediately vacating its spectrum band once a licensed user is prepared to use its legitimate spectrum. In which case, DSA implies that the communicating devices will search for another unused spectrum band to utilize during the absence of actions of its licensed users. Figure 1 conceptually illustrates dynamic spectrum access.

The Cognitive-based Radio Network (CRN) is a key recognized technology for implementing Dynamic Spectrum Access to improve the solution associated with spectrum scarcity resulting with underutilization of channels. CRNs are envisaging as the next-generation wireless communication technologies that offer wireless connectivity for promising services. The important component of CRN as well as Dynamic Spectrum Access is the cognitive-based radio transceiver. A cognitive-based radio is a wireless device that is capable of sensing the nearby radio environment and hence dynamically captures the unused frequency band(s) depending on its assessment of the actions of the licensed primary networks.

In order to make effective use of the unused bands, cognitive capable devices are connected together to form cognitive radio network in which there are two different kinds of users with dissimilar rules: where in for the licensed spectrum band primary users (PUs) have the priority to operate and the same must be accessed by secondary users (SUs) opportunistically without interfering with PUs.

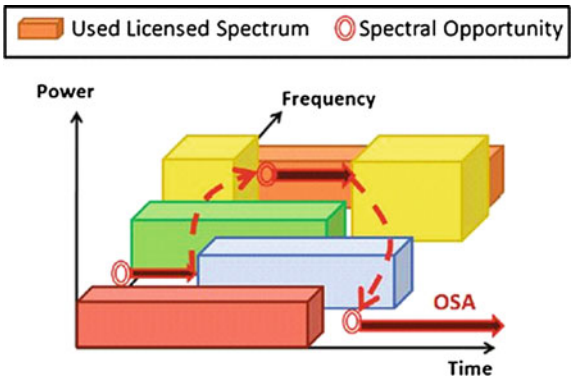


Fig. 1 Spectrum hole concept

2.1 Requirements for a CRN

The main requirements [1] for cognitive-based radio are briefly explained in the following manners.

Spectrum Sensing: Spectrum sensing is the ability of a radio technology to be aware about the parameters that regard to electromagnetic wave propagation that happens in one particular band of frequency among many bands. It is one of the main significant functions of a cognitive radio because it provides the knowledge of the spectrum handling at different timings in the nearby atmosphere. This information required is gathered in conventional manner by sensing spectrum dimensions such as operating frequency, time of transmissions, spatial and code by using geo-location and database. The advanced techniques such as Angle of Arrival, Frequency Hopping Code, and Beam forming are the other measures for spectral estimation. Based on this spectral estimation, the cognitive radio can arrive at an exact position regarding to radio environment.

Spectrum Analysis: Identifying the spectrum opportunity can be viewed as another important function of cognitive cycle and typically defined as *a range of frequencies* or *bandwidth* for which the primary users were absent in their transmissions at one particular time and geographical area. This kind of description is not so good as it covers only three dimensions regarding spectrum sensing: time, frequency, and space. However there are extra scope that must be explored; for example, Spread Spectrum Coding and Frequency Hopping Codes, angle measurement and multiplexing multiple users into an identical channel at the same time of same location creates spectral opportunities to the cognitive radio users.

Spectrum Access Decisions: Spectrum Access Decisions is the final step involved in the cognition cycle of CRN to select more appropriate band required to fulfill their QOS among the available bands. Spectrum Access Decision can be carried by considering various spectrum holes along with their characterization parameters such as: 1. Maximum allowable power for CR user to estimate channel capacity 2. Transmission range and its path losses 3. Modulation method and level of interference 4. Link errors due to interference. Desirable spectrum band is identified based on combining all the above characterizations of parameters gathered during spectrum sensing and analysis to find available spectrum for accurate spectrum decision.

2.2 Reconfigurability of a Cognitive Radio

Reconfigurability refers to the capability of a cognitive-based radio to retune its transceiver parameters to the newly selected values as shown in Fig. 2 so that unused spectrum is accessed and active communication is continued over the new channel. A cognitive-based radio transceiver should be more flexible and must be capable to reconfigure broadcast parameters such as transmission frequency,

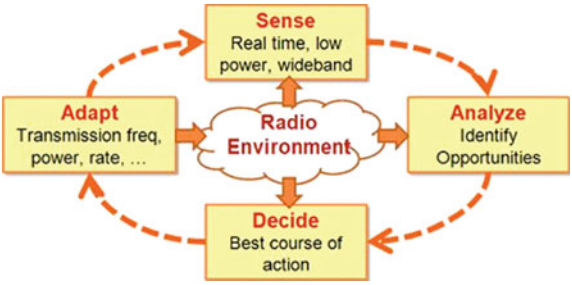


Fig. 2 Cognitive radio cycle

data rate, and power according to a certain communication protocol. The protocol stack for different layers must adapt to new channel parameters and select proper communication models at PHYSICAL and UPPER layers. A cognitive radio cannot be restricted to one kind of communication protocol; instead it must be able to use different spectral opportunities based on the radio environment. The software-defined radio is the ideal implementation environment of radios with seamless configuration capabilities. Thus, cognitive-based radios were originally referred to as software radios with extended self-awareness capability.

Spectrum Mobility: The reconfigurability of a cognitive-based radio transceiver reflects the spectrum mobility function of the cognitive radio. Spectrum mobility or Spectrum Handoff is a result of either change in transmission frequency or to move from one channel to another. At the time of spectrum mobility the cognitive radio must observe (1) the appearance of PU's of current band (2) degradation of current channel quality (3) interruption of ongoing transmission due to other CR users. That means spectrum mobility is the function of cognitive radio that allows dynamically discovering the new available spectrum opportunity by which handoff method guarantees the change over to the novel frequency band without interrupting the communication between communicating nodes. CRN spectrum mobility can be implemented on two strategies namely REACTIVE and PRO-ACTIVE. In REACTIVE handoff CR, users switch the spectrum after link collapse due to spectrum mobility without any grounding time, resulting in considerable loss in current transmission. Conversely, in PRO-ACTIVE handoff CR, users can estimate future action in the present link and find a novel spectrum, while maintaining the current transmission.

2.3 Cognitive Radio Network Architectures

The basic Architecture of CRAHN [1] consists of two major sections namely (i) primary network users (PUs) and (ii) CR networks or secondary users (SUs). A primary network as well referred as a licensed network that is approved to operate in an assured spectrum band. Prime networks can either be a centralized infrastructure or a distributed ad hoc in nature. The nodes/users of a prime network

can only have precedence with respect to spectrum access license to operate. The primary users cannot extend any kind of collaboration to the secondary network or secondary users (SUs) as they are only the licensed users to the spectrum.

Alternatively, CR network consists of users who are not licensed to operate in a specified or predefined band. The CR users (SUs) have to wait for opportunity to access both their licensed and unlicensed spectrum band opportunistically. The network state is controlled by primary networks (PRNs) and has its upper boundary on CRN (SUs) activities. On the arrival of licensed user, CRNs are required to stop their transmissions over present communication channel and switches to another one.

Centralized Cognitive Radio Networks: A centralized cognitive radio network is an infrastructure-based networks in which the communication activities of secondary users are controlled and coordinated through the cognitive radio base station as shown in Fig. 3a. The central base station collects spectrum-related information about each link and processes this information to take overall spectrum access decisions for every node. IEEE 802.229 (WRAN) is the first worldwide standard for CRNs in point-to-multipoint communication scheme over the unused vacant T.V channels or T.V white spaces in the VHF and UHF bands of frequency between 54 and 862 MHz for a distance of 33 km. Other examples include the European Dynamic Radio meant for IP services in Vehicular Environment and Spectrum capable Uni- and Multi-cast Services over active radio network in Vehicular Environments.

Distributed Cognitive Radio Networks: On the other hand, the secondary users can also have the communication with each other based on ad hoc nature defined as the category of networks operating without the support of any fixed infrastructure. The absence of central base station make CRNs users to coordinate among themselves in distributed manner in which all nodes share their spectrum access decisions for spectrum opportunity as shown Fig. 3b. This model needs a device-to-device synchronization for spectrum access coordination. Additionally, disseminated cooperative detection and communication techniques are used to

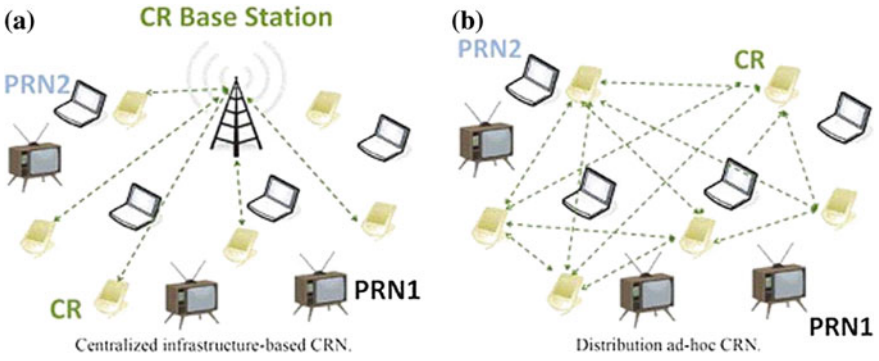


Fig. 3 Centralized/distributed CRAHN

advance the overall network performance. Example for disseminated CRNs includes the device-to-device mode of DARPA's next-generation (XG) dynamic access network.

3 CRAHNs Versus Multichannel Ad Hoc Network

The differences between the classical multi channel/hop ad hoc network and CRAHN with respect to various described features are summarized in the table.

Sl. no.	Parameter	Multi channel/hop ad hoc network	CRAHN
1	Transmission spectrum	Predefined channel that remains unchanged with time. All the channels are available continuously for transmission and every user can be able to select few from this on self-interference factors	Largely distributed channels over wide frequencies which, can vary with time and space. Each secondary user has dissimilar spectrum accessibility based on primary user activity
2	Dynamic topology information	Periodic beacon messages exchanged between nodes together with dynamic topology information based on local coordination	Transmitting beacons over all possible licensed spectrums is not possible resulting into incomplete topology information
3	Range of frequency	Less number of fixed channels, at most 10 or even less	Wide range of frequencies available in both licensed and unlicensed bands for e.g., T.V and F.M radio spectrum bands. (54–862 MHz) as well as 4.9 and 5 GHz
4	Multi-hop/multi spectrum environment	Multi-hop point-to point network will result in increase of hop count, ubiquitous connectivity and coverage. Traffic flow happens through nodes by relay or forwarding. The allowed channels are from single spectrum band with similar physical channel characteristics like coverage, modulation, and power management as an example of IEEE 802.11 ad hoc network based on 2.4 GHz spectrum band with 13 channels	It requires cooperative routing among nodes which vary in link frequency or channels based on PU arrival. The MAC and NETWORK layer protocols deal with no predefined channels, interference from other nodes/primary and heterogeneity in radio frequency. Keeping end-to-end QOS involves not only in the traffic load but also spectrum bands along path. This CRN information must be shared among all flows in the network [4]

(continued)

(continued)

Sl. no.	Parameter	Multi channel/hop ad hoc network	CRAHN
5	Routing strategy	Routing is a major challenge that affects the performance of the total network. The distance between the nodes, nodes mobility, limited power or energy level and network lifetime are the parameters that affects the network connectivity [3]	The routing strategy has additional challenge to deal with active behavior of PUs, which change network topology and effects on changing spectrum opportunities. Direct deployment of ad hoc routing protocol in CRN will affect in poor performance in terms of throughput, end-to-end delay and probability of packet loss
6	Mobility support	Every node in a MANET is free to move separately in any direction resulting into change in its links to other nodes regularly while maintaining the required information properly in the routing tables. The device or node has to incorporate routing functionality with bandwidth constraint. Node mobility increases the detachment rate of route in wireless networks	To study the node mobility in CRAHN, the MAC protocol has to deal with spectrum sharing function among the nodes to get better throughput and to reduce the effect of spectrum mobility caused by mobile CR nodes. CSMA/CA and multichannel MAC and C-MAC protocols have the advantage of handling with hidden terminal problem
7	Quality of service	QOS is the overall performance or measures of ad hoc network considered from user point of view related to aspects such as throughput, delay, error rate, jitter, congestion prevention, etc. It is a priority-based service that provides different priorities to different applications, users, or data flow	QOS provides priority among CR nodes/data flows and guarantees certain level of performance. Largely spectrum mobility constraint, dynamic network topology, route stability are new and good metrics for QOS in CRAHNs. Combining them along with delay and bandwidth provide a good frame work for real-time applications

Multicasting or cluster communication is a fundamental network primitive used in various wireless applications that includes video conferencing, file distribution, and broadcast transmission. Multicasting over wireless networks is a tough goal because it has to address issues like topology, security, and QOS. Furthermore, multicasting in CRAHNs is challenging due to the dynamic topology of CRNs which adopts techniques and protocols based on optimization theory, network coding theory, and game theory [6]. There is very little research on recovery of packets that were lost. In fact, recovery problems in cognitive radio networks has

similarity with recovery in multichannel, multi-hop ad hoc networks but with an added goal to deal with the active behavior of PUs and their effects on varying spectrum opportunities availability of SUs.

4 Framework to Network Layer

A classical ad hoc routing table maintains the information which is only about next hop. But in CR networks these routing tables additionally must be included with the channel, transmission rate, modulation adopted, and other parameters that are unique to each link. The final end-to-end performance is affected by a finite channel switching delay. The route table with additional information has to cover the full channel usage along the complete path from present node to the destination and the channel will be selected such that to reduce the number of channel switches in the path. This additional spectrum information along the path needs larger storage space and also increases database access time.

Switching to other channel or changing from existing route is the responsibility of decision block based on the sensing and path information and required QOS performance. Decision block is influenced by the QOS evaluation block which considers traffic facts such as number, length and inter arrival time for packets. Based on necessities precise by the application layer the decision block signals for a new route founding, through route establishment block or go on with the on hand path without changes.

The routing framework must also include learning block for self-learning and environment-aware paradigm. It helps the decision block to select superior channel and path switching decisions based on feedback from destinations for a given routing cycle.

4.1 CRAHNs Routing Algorithm

Routing in multi-hop CRAHNS is a significant issue that affects the performance of whole network. CRAHNs routing algorithms has to deal with challenges like; dynamic changes in spectrum channels due to the dynamic behavior of the primary and secondary users, heterogeneity of radio frequencies, i.e., sensed channels to one pair of nodes is not the same to other pair, support for maintaining multiple routes for a given source to destination, ability to provide definite QOS requirements, geographical location awareness, scalability with respect to network size and nodes synchronization on different channels.

One of the main mechanisms of a routing protocol is its routing measure or metric that determines the performance of different routes. A good metric for CRAHNs has to consider the different challenges like dynamic topology of network, network lifetime, nodes mobility, and their limited power apart from added

constraints from PUs. The routing metric assigns different weights to different spectrum bands (channels) based on their accessibility and interruption due to PUs' activity and channel switching time when channel switching decision is taken. This channel switching time is the time necessary to communicate the channel change over assessment to the next hop and time to tune for new channel. Mustafa Youssef and Mohammed Ibrahim et al. [5] have offered a study and classification of dissimilar routing metrics for CRAHNs, based on two main categories: single-path routing and multipath routing. Dissimilar metrics were discussed as well as the routing protocols that use them.

A survey on routing protocols in CRAHNs has been carried by Samar and Mustafa et al. [2] and classified them as: delay based, link based, throughput based, and location based. They concluded with open research issues which are addressed routing-related areas that need more contribution in research as Cross layering, Mobility support, Path robustness (multiple routes) and Quality of service(QOS). Cross layer design allows to exchange sensing information among physical, MAC and Network layers with co operation.

The common characteristics that are to be observed are the Protection of PUs from interference during route construction and data forwarding, make joint path and channel selection at each forwarder and enhance network throughput through usage of multiple concurrent packet transmission on different channels.

References

1. Akyildiz. I.F., Lee. W.Y., Chowdhury. K.R.: CRAHNs: cognitive radio ad hoc networks. Ad Hoc networks, vol 7, No. 5, pp. 810–836, (Jul. 2009).
2. Samar Abdelaziz, Mustafa EL Nainay.: Survey of Routing Protocols in Cognitive Radio Networks. Preprint Submitted to Elsevier, (October 1, 2012).
3. Li Gui., Xiaofeng Zhong., Shihong Zou.: Traffic Assignment Algorithm for Multi-path Routing in Cognitive Radio Ad Hoc Networks. IEEE Wireless Communications and Networking Conference (WCNC): (Networks, 2013).
4. Shamik Sengupta., Subbalakshmi. K.P.: Open Research issues in Multi-Hop Cognitive Radio Networks, IEEE Communications Magazine, (April 2013).
5. Moustafa Youssef., Mohamed Ibrahim., Mohamed Abdelatif., Lin Chen., Athanasios V. Vasilakos.: Routing Metrics of Cognitive Radio Networks: A Survey. IEEE Communications Surveys & Tutorials, vol.16, No.1, First quarter (2014).
6. Junaid Qadir., Adeel Baig, Asad Ali., Quratulain Shafi.: Multicasting in cognitive radio networks: Algorithms, techniques and protocols. Journal of Network and Computer Applications, Elsevier, (2014).

Implementation of Reconfigurable Circuit with Watch-Points in the Hardware

A. Murali, K. Hari Kishore, L. Srikanth, A. Trinadha Rao and V. Suresh

Abstract This paper introduces the use of watch-points in the FPGA designs that creates the debugging environment. We described some designed techniques that can be automated and modified the watch-point logics using the debugging tools like Jbits and Jroute. This reduces the hardware debugging time. In the proposed technique, the watch-point logic modification makes the speedup from 5 to 12 times with the other benchmark circuitry systems.

Keywords FPGA · Debugging tools · VLSI

1 Introduction

A typical reconfigurable application requires the hardware compiled on more than one FPGA circuits. This application debug includes both hardware and software components. Hardware simulation is one of the techniques that is most popular for

A. Murali (✉)
Department of ECE, Raghu Engineering College, Visakhapatnam, AP, India
e-mail: amurali3@gmail.com

A. Murali · K. Hari Kishore
KLEF, K L University, Green Fields, Guntur, AP, India
e-mail: kakarla.harikishore@klunivrsity.in

L. Srikanth
Department of ECE, GMR Institute of Technology, Rajam, AP, India
e-mail: srikanth451@gmail.com

A. Trinadha Rao
Department of ECE, Chintalapudi Engineering College, Guntur, AP, India
e-mail: akula.trinadha@gmail.com

V. Suresh
Department of ECM, Vignan's Institute of Information Technology,
Visakhapatnam, AP, India
e-mail: vayasisuresh@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_69

hardware debugging. This technique is relatively slower when examining the circuitry details. This process is time-consuming at very starting stage of the design, when the multiple runs take over to ensure the correctness of the circuit. This isolated process of debugging in the hardware and the software components is a time-consuming process with the simulators. As a result, the resultant application after the integration may not give good results since there might cause the errors while integrating the both components. This time can be minimized by running the hardware directly on the target platform. This target platform is available for the reconfigurable computing applications before the complete design [1, 2].

In most cases, the FPGA designs enable the key feature for debugging functionality which commonly known as readback capability [3]. This operation can be performed on the internal elements of the FPGAs like LUTs, flip-flops, IOBs. It matches the state with some symbolic name in the original circuitry. It can be used to analyze the signal values while execution. It also used to get the state of the circuit at design execution. Before the initialization of this readback operation, the clock supplied to the design must be halted. Once if the clock is set to suspended, the signal values can be sampled by single-stepping or after stepping the multiple clock cycles (multi-stepping) at a time. The readback operation allows to debug the circuitry design on the target platform.

But this includes a few disadvantages when it is performed on the resultant platform. The readback operates slowly. Without stopping the design execution or halting, the debugging process cannot be done in the design. And for every clock cycle, the configuration of readback takes at least 1 s which is very slow to check for a signal value. To overcome these drawbacks, the secondary debugging circuit is embedded into the design for the fast operations. This is nothing but a watch-point, which controls and the observed at the execution time which is close to the normal speed of the system. Now the readback operation can make its process securely without any issues raising in the design.

This embedded design (watch-point) can also be removed from the circuitry system, when the system is at its final validating process. Thus, it concludes that the same area and the speed of the design can be varied with the watch-points and enable the controlled execution process for the hardware design and the speedup the debugging process with less user intervention.

2 Fpga Circuitry Design

As the authors in [4] and [5] presented the debugging logic operation in the designed circuits with validating and debugging purposes which are also has been proposed previously. For a complete debugging style, a scan chain is proposed in [4], whereas in [5] a technique is implemented with the JavaScript which is less familiar than the schematic environments. It allows debugging logic at a bit-level, while in the other cases, the modifications varies in frequent. Thus, it slows down the time for accessing and loading the bitstreams on the target FPGA circuit.

To embed this debugging logic in the circuitry, many commercial tools provide more powerful features to the FPGA designs. Chipscope is one of such tool provided by Xilinx [6] which allows to embed with ELA (Embedded Logic Analyzer) into the cores of the designs. At predefined condition, it drops a trigger at the execution level of the design. These factors can be re-modified with no recompilation of the circuit. Logic Analyzer is used to notify the status of the signals and it even helps in the port connections on the reconfigurable computing states of the board. Coming to the area, it is a fixed type and it can remain in the same size even if some signals have to be monitored. SignalTap is another product which is mentioned by Altera [7] and is operated similar to the Chipscope. A complete recompilation is needed for any modification in the design.

Debugging and validation of the systems with only embedding debugging logic is not the end. But some authors specifies with the breakpoint logic units [8] and hardware breakpoint capability as in [9].

3 Tool Analysis

The software debugging tools and the hardware simulators introduces the watch-points for the hardware designs on the co-processor board. The signals can be monitored from these watch-points for any specific condition. The following Table 1 gives a clear analysis of the trigger conditions for any signal that can be monitored to any condition. These signals are compared with the user-defined patterns with each clock cycle. If the signal value matches and satisfies the user-specified trigger condition, the execution process is then stops and an interrupt raises to the processor.

Table 1 Watch-points trigger conditions

Trigger condition	Description
>	Triggers when the signal monitored is greater than the watch-point value
>=	Triggers when the signal monitored is greater than or equal to the watch-point value
<	Triggers when the signal monitored is less than the watch-point value
<=	Triggers when the signal monitored is less than or equal to the watch-point value
=	Triggers when the signal monitored is equal to the watch-point value
Rising edge only	Triggers only when a signal monitored makes rising edge transition
Falling edge only	Triggers only when a signal monitored makes falling edge transition
Both edges	Triggers when a signal monitored either makes rising or falling edge transition

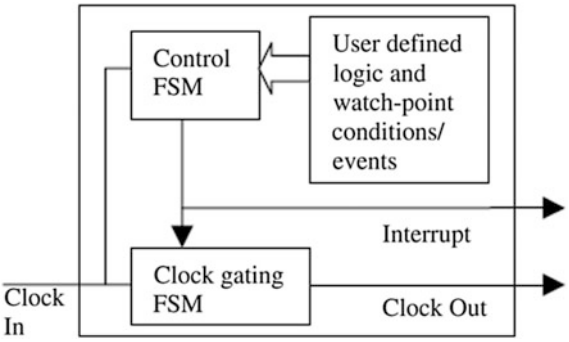


Fig. 1 The clock control operation

With the raise of this interrupt, the software initiates a readback operation. After the readback operation, the system must be able to be connected to the same state from where it stops the execution. This can be implemented with the Finite State Machine (FSMs) and also with the gated clock. FSM enable the clock once the interrupt is acknowledged by software which is running on the system.

Figure 1 illustrates this operation. Depending on the requirement, the AND or OR can be logically set for any multiple trigger conditions for a single signal. And for the different trigger conditions with multiple signals, the logically set AND or OR can be made to one interrupt output.

4 Implementation of the Watch-Point Logic

For implementation of the watch-point logic, we described two methodologies.

4.1 Hardwired Condition

Adding the debugging logic with constant value is nothing but adding the watch-point condition. In HDL designs, these constant type signals can be monitored as of here. In this technique, the trigger conditions are designed and added to the HDL. It is then synthesized to optimize and implement with the debugging logic. This is mostly considered in terms of area as of adding the watch-point logic condition. This design can be utilized in the CLB utilization where high area is needed with less space for additional logic. This can also change or modify the patterns of the watch-point logic within its HDL file. As the names are changed in the process after synthesis, it is difficult to relate the constant signals with the generated names after the synthesis. Hence it is a time-consuming method for larger designs to make changes of the watch-point logics, since, for each iteration requires the complete synthesis time.

4.2 Register Chain

This technique implements the watch-point logic with signal value storages in the flip-flops. Adding the design level register chain which is analogous to the flip-flop scan chain in the VLSI testing [10].

A register chain is formed when all the flip-flops are connected as a chain together to implement the watch-point logic. The output of one flip-flop is connected to the input of the other flip-flop and so on forming a chain. At initialization stage, the corresponding data values of the watch-points are shifted into the respective registers with many clock cycles. Here with the help of the comparator, the data in the registers can be compared with the user-specified signals. So, the RESET signal is assigned in the circuit whenever the user changes the signal pattern and the data thus is sent to the memory input port. For synchronizing the operations, shifting the data and enabling the RESET logic, FSM control takes care in the design. The main advantage is with the register chain, where the modifications can be easily made by the user online only by asserting the RESET signal with API calls. Time-consuming synthesis is completely bypassed.

As part of this research, this method can be integrated with GUI-based co-debugging utility. Because it is a user-specific stored values that are presented in the register chain by using the GUI concept. Recompilation of the design is not necessary for this technique. The Fig. 2 gives a brief idea of this methodology. To modify or change the values in the comparator, LUT values of LUTs can be changed, which correspond to the comparator in the NCD file and then finally generates a new bitstream.

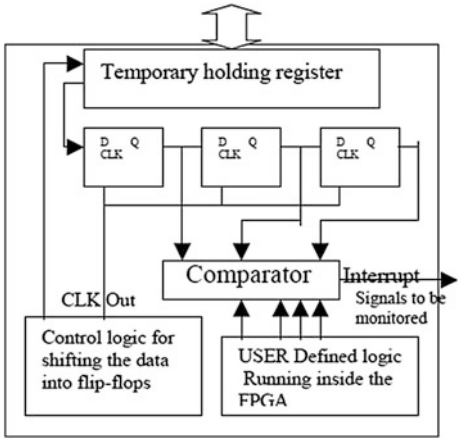


Fig. 2 Register chain technique for watch-point logic

5 Comparisons of the Experimental Results

Table 2 describes the comparison of the watch-points that are implemented in the various design modes. The design of the circuit depends on the features like area, ease to modify, time required for modification single patterns which can be modified by a co-debugging interface that is developed between the hardware and the software. As the original design is already a constrained one, the design does not become slow with the watch-point logic. But it is not constrained in the placement and the routing process. Since, then the placer is flexible to place it at any point, to reach the original design constraints.

The hardwire condition technique is the most efficient methodology. Here the synthesis, route and place can freely implemented by optimizing the watch-point logic. For the larger designs, this technique can still introduce the watch-point logic. But this may not be possible with other techniques as they consume more area and need more routing space.

Table 2 Comparing the various watch-point logics

Watch-point technique	Area overhead	Time to change watch-point value	Changes in watch-point value possible through co-debug interface
Register chain	Large	Small	Yes
Component instantiation	Medium	Medium	No
Hardwired condition	Small	Large	No

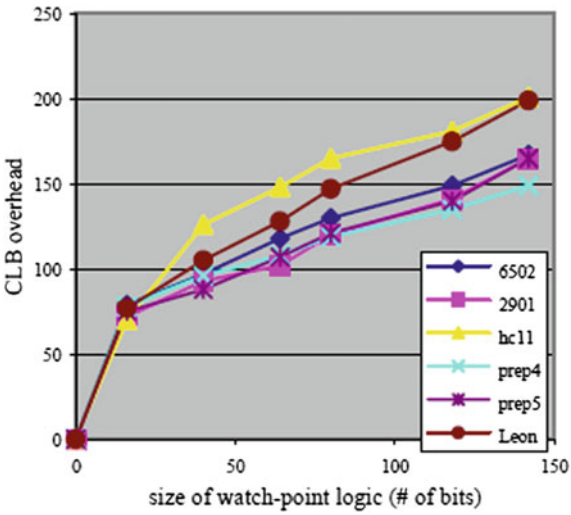


Fig. 3 Area overhead for register chain technique

The areaoverhead of sizes in other variations is shown in the form of graph (Fig. 3) for the register chain methodology. This graph is generated with CLB overhead calculations which are reported in the Map Report File (.mrp) that is formed with Xilinx design implementation tools. This file contains the CLB counts after calculating the factors like mapping, placement and the routing. Finally, the obtained CLB count is then considered from original and modified designs, and then are overhead is calculated. Hence, the steep increase at the starting point as the control FSM is added at the initial watch-point addition.

6 Conclusion

Our proposed technique evaluates the two approaches to implement the watch-point logic in the FPGA design circuitry for the hardware and the software co-debugging environment. Readback capability provides the co-debugging environment which is highly featured as of a traditional hardware and the software systems. The process of debugging the hardware designs by using the watch-point logic is faster than the traditional hardware simulation systems.

References

1. B.L. Hutchings and Brent E. Nelson. Unifying Simulation and Execution in a Design environment for FPGA Systems IEEE trans. on VLSI Vol. 9 No 1, Feb. (2000).
2. K. A. Tomko and A. Tiwari. Hardware/Software Co-debugging for Reconfigurable Computing IEEE International High Level Design Validation and Test workshop, Oakland CA, Nov. (2000).
3. Lucent Technologies, Allentown, PA, ORCA Series 4 FPGAs, Dec. (2000).
4. T. Wheeler et. al. Using design-level scan to improve FPGA design observability and controllability for functional verification FPL'01.
5. Paul Graham et. al. Instrumenting Bitstreams for Debugging FPGA Circuits proceedings of IEEE Symposium on Field-Programmable Custom Computing Machines, Apr. (2001).
6. Xilinx, San Jose CA. ChipScope software and ILA Cores User Manual, v. 1.1. Jun. (2000).
7. Altera, San Jose CA. SignalTap Embedded Logic Analyzer Mega-function, ver.2.0, Apr. (2001).
8. Triscend Inc. E5 Configurable System-on-Chip Platform data sheet, Jul. (ver. 1.06). http://www.triscend.com/produs/dse5csoc.pdf (2001).
9. FIPSOC user manual chapter 7, SIDSA Inc. http://www.sidsa.com/FIPSOC/Users_manual/Chapter_07.pdf.
10. M. Abramovici, M.A. Breuer, A.D. Friedman. Digital Systems testing and testable design pp. 358 IEEE press 1990 ISBN 0-7803-1062-4.

Ad Hoc Networks: Route Discovery Channel for Mobile Network with Low Power Consumption

SK. Nagula Meera, D. Srinivasa Kumar and Srinivasa Rao

Abstract The mobile networks are the independent node networks with limited power sources and mobility. The source node acts as an intermediate node for communication with the target nodes with direct transmission range of source node. For the clear network establishment between the source and the target nodes, the selected node must have the sufficient power and minimal power consumption. Hence, establishing the stable path between the source and destination nodes is crucial for multicast routing network paths. For multicasting networks, a special route discovery channel is proposed for mobile ad hoc networks. This approach is based on the evolutionary strategy. The topology discriminates other tree-based multicast routing topologies by adopting evolutionary computation strategy called genetic algorithm to select the multicast tree with optimal intermediate nodes that have the maximal residual energy and minimal energy usage.

Keywords Mobile networks · Multicasting · Ad hoc

1 Introduction

MANETs are the mobile node networks that can maintain the communication for themselves without the other infrastructure supports. These types of networks are configured independently and are operated jointly by all the nodes without any fixed units of infrastructure like base stations, access points, or routers. The routing

SK. Nagula Meera (✉)
Department of ECE, CMRIT, Medchal, Telangana, India
e-mail: nag.meera@gmail.com

D. Srinivasa Kumar
Institute of Technology & Science, Beerpalli, Krishnagiri, Tamil Nadu, India
e-mail: Srinivaskumar_d@yahoo.com

S. Rao
Department of ECE, College of Engineering, JNTU, Hyderabad, Telangana, India
e-mail: dsraoece@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_70

decisions are made independently by the nodes which act as both host and router. Power is the critical resource as the routing of the data is made using batteries and exhaustion of the batteries leads to network disconnections. For the maximum connectivity of the nodes, minimum power in the routing has to be efficiently managed, as the power consumption is supplied by the batteries.

MANETs use the multi-hop communication for data transmission, so that nodes use less power and avoid draining of the battery power. The routing schemes are based on consuming very less battery energy maintaining the good residual battery capacity after every routing session. The techniques devised for offering QoS services with multicast routing consider different metrics of multi-constraints such as multi-constrained minimum cost multicasting [1] and degree-constrained least cost multicasting [2] without giving importance to the energy efficiency factor and due to this they are inapplicable for the routing process in MANETs.

The genetic algorithms technique usually has large number of iterations making it inapplicable for MANETs in the routing of multimedia content that are delay sensitive based. The current research shows high computational capabilities achieved with new hardware-based applications of genetic algorithms [3]. We applied the genetic algorithm in MANETs to the source-based multicast routing and developed an energy-efficient genetic algorithm which determines in the multicast source routing, multicast trees with delay constraints to achieve energy efficiency which is proved by the results of the experiments performed in this paper.

Power-aware multicast routing schemes help in managing the energy resources, preventing the draining of battery power, and avoiding the partitioning of the total networks. A solution for the multiple QoS constraints-based QoS multicast routing challenge [4] is applying the artificial intelligence based genetic algorithm approach.

2 Related Work

The models devised in [5–8] are benchmarking multicast routing protocols redefined the transmission range of the node by the power consumption ratio. These models consider the node mobility, transmission strength, and residual energy of the nodes in order to select optimal node within the transmission ring. Redefining the transmission range is a continuous process and hence the ring-based protocols are affected by the process overhead. The routing protocols that are GA-based energy efficient QoS multicast routing protocols as in [9, 10] aimed to achieve stability and energy-efficient MANET routing. This model estimates the signal strength to predict the hop level stable links and aggregation of signal strength observed for selected links is used further to conclude the fitness as route stability and energy usage of the multicast tree. The major constraint of this model is: it is aimed at stable route in the cost of battery life and process complexity observed due to the traditional genetic algorithm used.

The explore existing models are effected by process overhead, moreover these models are aiming link stability at the cost energy consumption that caused turn-around network life span is considerably low. We introduced a minimal energy usage competent multicast route discovery strategy that establishes Steiner tree based multicast route that guarantees maximal life time of the network. The proposed model devised a set of critical metrics called energy consumption fraction, residual energy fraction, and multicast restraint fraction. In order to select the best optimal tree among the available, our proposed model is using the evolutionary computation technique called genetic algorithm. The cost or fitness function of the genetic algorithm is using the proposed metrics to estimate the resultant tree fitness.

3 Energy Consumption with Multicast Steiner Tree Based Route Discovery

Initially, the possible multicast trees must be discovered, where the data can be transmitted between the selected source and the destination nodes. As the selective nodes forms the tree structure, these paths are referred as the Steiner trees. Assuming as in [11], the multicast trees *MT* is the set of trees that are selected from the route request process. These set of trees are then used as the initial chromosomes for genetic evaluationt_1.

$$MT = \{t_1, t_2, \ \ldots, \ t_{|MT|}\}$$

The energy consumption fraction is defined as the unexceptional energy required to transmit a frame by a node n_p to its successive node in the route. The energy consumption fraction (*ecf*) at each node n_p is measured as follows:

$$ecf_{n_p} = \frac{aec_{np}}{|h|},$$

$$\text{where } aec_{n_p} = \sum_{q=1}^{|\mathrm{h}|} \left(\left(\rho^{\frac{n_p \leftrightarrow n_q}{|h|}} \right) \mathrm{X}\, ec + \overline{ec}\, \mathrm{X}\, \tau \right), \tag{1}$$

where ρ is the minimum frequency required for unit of distance (ud), $n_p \leftrightarrow n_q$ denotes the actual distance between the nodes n_p, and n_q. τ denotes the probable retransmission factor.

The aggregation of the unexceptional energy consumption observed between node n_p to all successive nodes in hierarchy h is found further the same used to find energy consumption fraction for node n_p.

The optimal energy efficient multicast route among the possible multicast routes discovered by using evolutionary computation strategy is called genetic algorithm (GA) [5]. The progressive evolution strategy was adopted to minimize the

computational overhead of the GA that applied on set initial multicast trees $MT = \{t_1, t_2, \ldots, t_{|MT|}\}$.

The Optimal multicast Steiner tree Discovery Function
$es \leftarrow true$ //evolutions state
While (es) Begin
$nMT \leftarrow \phi$
$\forall_{i=1}^{|MT|}\{t_i \exists t_i \in MT\}$ Begin //for each entry in MT
$\forall_{j=1}^{|MT|}\{t_j \exists (t_j \in MT \wedge j \neq i)\}$ Begin //for each entry in MT, which is not t_i
$nMT \leftarrow$ GAE (t_i, t_j) // Invoking GA Evolutions, leads to find new evolutions of the multicast trees from t_i and t_j.
End
End
$\overline{MT} \leftarrow MT$ //initialize $\overline{MT}$ by MT
$\overline{MT} \leftarrow nMT$ //Move all discovered multicast trees to $\overline{MT}$

$mtf\ \overline{MT}$ //see section 3.1
$if\ MT \cong \overline{MT}$ Begin // identical by approximation
$es \leftarrow false$
End
End

4 Analysis of the Explored Result

The experimental setup was a simulation formed by NS2 which uses core standards like MAC 802.11 DCF, data to be transmitted in the form of CBR, 2.0 Mbps as bandwidth capacity of physical layer and node transmission range is set to 50 m^2. The node level residual energy, position, mobility direction, transmission frequency for unit of distance, and other desired factors were initialized using Gaussian distribution strategy. All the possible multicast tree routes between given source and destination nodes will be found by traditional benchmarking strategy called MAODV [12]. These initial routes are further used as the inputs to the ECMST. The testbed of the network is formed with the range of 60–240 nodes and the metric

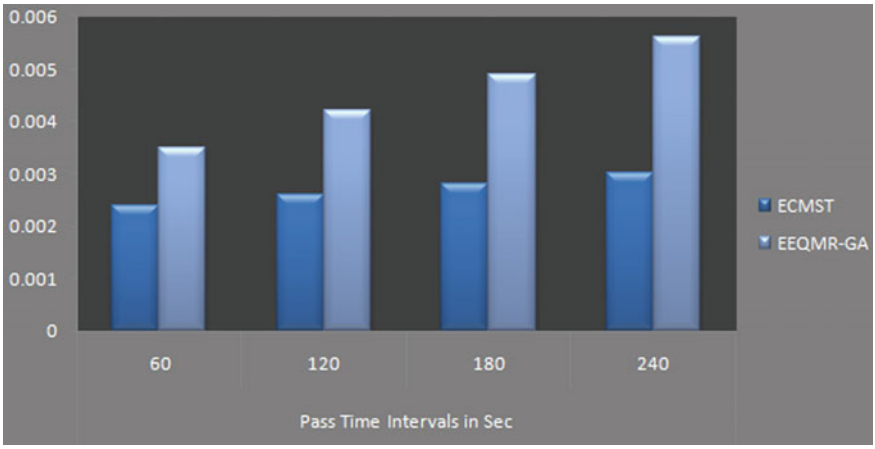


Fig. 1 End-to-end delays at divergent pass times

values are obtained at different simulation intervals and compared to the benchmarking model called EEQMR-GA [10].

The performance of the ECMST is assessed by the results observed for end-to-end delay, packet delivery ratio, and residual energy ratio. The metrics obtained from the networks build with divergent count of nodes are optimal, firm, and also indicating that the proposed ECMST is scalable and robust. These metrics obtained at different simulation intervals were compared with the values obtained to same metrics for benchmarking model EEQMR-GA.

According to these results, the end-to-end delay observed for ECMST is substantially low that compared to EEQMR-GA. Figure 1 gives the clear illustration of the difference.

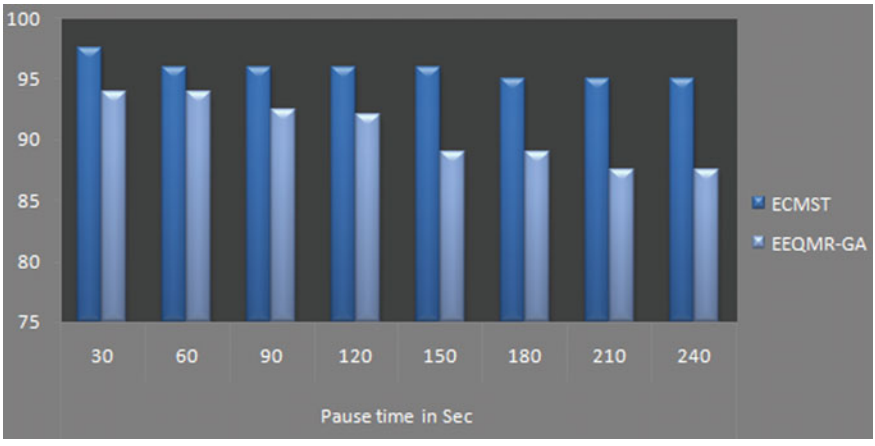


Fig. 2 Packet delivery ratio between ECMST and EEQMR-GA

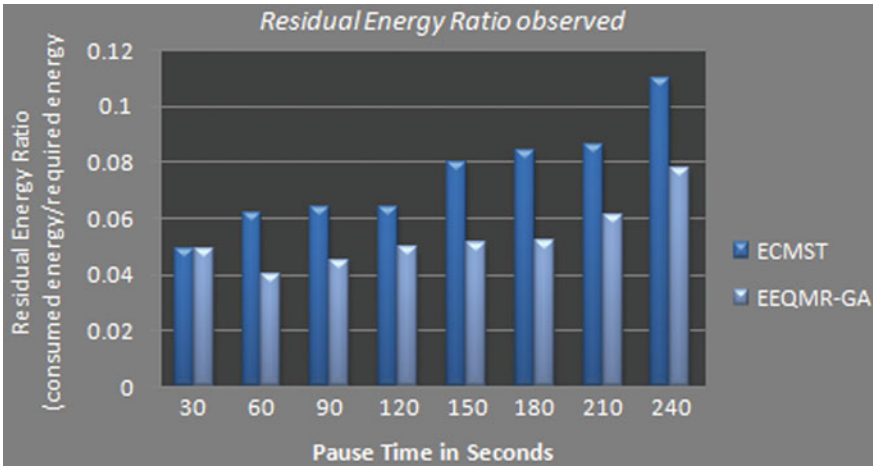


Fig. 3 Residual energy ratio of ECMST and EEQMR-GA

The packet delivery ratio observed for ECMST is potentially high when compared with the EEQMR-GA and found optimal with around 97% successful delivery as seen in following Fig. 2.

Similarly, the energy usage of the ECMST is observed as lower when compared to the EEQMR-GA. Figure 3 displays the clear output of the energy levels that are consumed on ECMST.

5 Conclusion

The proposed approach is an evolutionary computation strategy that adopts progressive genetic algorithm [5]. This topology assesses the optimality of the multicast tree by the three crucial metrics called energy consumption fraction, residual energy fraction, and opportunistic multicasting scope. The impact of this topology was explored by applying on the routes discovered by MAODV. The progressive genetic algorithm used to identify energy efficient multicast tree is balancing the process overhead by refining input chromosomes by comparing the fitness with child chromosomes formed. It has been proved that the experimental study for the proposed ECMST is scalable and robust. The future research can extend the ECMST by considering the node mobility speed and direction as another heuristics to identify energy efficient routes for high-speed mobile networks and can also define the multiobjective QqoS aware multicast route discovery.

References

1. D.P. Agrawal, Q. Z., Introduction to wireless and mobile systems. CA: Brooks/ Cole Publishing (2003).
2. Luo Junhai, Y. D., Research on topology discovery for IPv6 networks. IEEE, SNPD, 804–809 (2007).
3. Yang, S. C., Genetic algorithms with immigrants and memory schemes for dynamic shortest path routing problems in mobile ad hoc networks. Applications and Reviews, IEEE Transactions, 52–63(2010).
4. Toumpis, S., Wireless ad-hoc networks. Vienna Sarnoff Symposium,. Vienna: Telecommunications Research Center (2004).
5. Layzer, David. "Genetic variation and progressive evolution." American Naturalist: 809–826 (1980).
6. Zhou, Y., Li, G.S., Zhan, Y.Z., Mao, Q.R., &Hou, Y.B., DRMR: Dynamic-ring-based multicast routing protocol for Ad hoc networks. Journal of Computer Science and Technology, 19, 909–919(2004).
7. B. Wang, S. G., On maximizing lifetime of multicast trees in wireless ad hoc networks. IEEE International Conference on Parallel Processing, pp. 333–340(2003).
8. Biradar RC, M. S., Ring mesh based multicast routing scheme in MANET using bandwidth delay product. Wireless Personal Communication, 117–146(2012).
9. A.T. Haghighat, K. F., GA-based heuristic algorithms for QoS based multicast routing. Journal of Knowledge-Based Systems, 305–312(2003).
10. Lu, T., & Zhu, J., Genetic algorithm for energy-efficient QoS multicast routing. Communications Letters, IEEE, 17(1), 31–34(2013).
11. Srinivas, K., and A. A. Chari. "SLR: Sustainable Longevity Routing Protocol for ad hoc networks." Signal Processing, Communication and Computing (ICSPCC), 2013 IEEE International Conference on. IEEE (2013).
12. Royer, E. M., & Perkins, C. E., Multicast ad-hoc on demand distance vector (MAODV) routing. IETF Draft, draftietf-manet-maodv-00.txt (2000).

Methodology for Detecting the Node Efficiency in the Wireless Ad Hoc Systems

P. Sravan Kumar, G. Sridevi and S. Satyanarayana

Abstract As the manufacturing technologies are increased in the digital electronics, the wireless communication devices have become a leading development in the present networks. As the computing and the communication capability increases, there are other characteristics like low power, low cost and the small sizes, that has to be minimized in the communication wireless sensor networks. Clustering a wireless Ad Hoc network improves the performance and analyzing of the quality of clustering in Ad Hocs. In the proposed approach, the main idea is to prioritize the favorable nodes in the election and re-election process of the cluster heads. Our contribution to this work extends the previous tests with special properties and analyses QOC in the Ad Hoc network. The distribution of the workload among all the network nodes has been set uniformly and ensuring the constant connectivity in the network.

Keywords Ad Hoc networks · QOC · Clustering

1 Introduction

In the electronic family, the wireless connectivity if the communication networks are more popular these days. Clustering is one of the important techniques for partitioning the large networks into the small networking blocks. The cluster-based architectures reduces the energy consumptions very effectively and also enables the MAC with integrated quality. Cluster is defined as the group of interconnected nodes with a special node called cluster head (CH). These cluster heads are

P. Sravan Kumar (✉) · G. Sridevi · S. Satyanarayana
Department of CSE, Raghu Engineering College, Visakhapatnam, AP, India
e-mail: shraonep@gmail.com

G. Sridevi
e-mail: gaddesridevi.85@gmail.com

S. Satyanarayana
e-mail: satyacomp@gmail.com

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_71

responsible for managing the clusters like scheduling the medium access, dissemination of control messages [1]. Therefore, it is difficult to operate the network with the cluster heads alone. The weight-based clustering algorithm (WCA) adapts itself in distributed environment in dynamic manner, with developing applications in the Ad Hoc networks as described in [2]. Here, the nodes has to be served by the cluster heads are restricted, and hence, it does not suppress the MAC functioning. In addition, it acquires the ability to assign the different weights and has the combined effectiveness in the power transmission and mobility battery power of the nodes. To minimize the unnecessary signaling, power and bandwidth, a modified algorithm in introduced by [3]. The main aim of that approach is reducing the overhead communication with linear auto regression and cluster formations.

Bettstetter [4], used a heuristic approach by describing with the equations for the cluster density and the homogeneous distribution of the nodes in the DMAC algorithm. As mentioned in [5], a new algorithm, enhancing the Weighted Clustering Algorithm (EWAC) is proposed to increase balanced workload and also stability in MANETs. The CH is chosen based on some properties like distance mobility, battery lifetime, energy, transmission power and transmission range. As it is not possible to change CHs dynamically, there is a noticeable change in the reduction of the formed clusters. In all the mentioned theories [6], all nodes require the same selection process that affects the cluster quality.

2 Workout Analysis

As in [2], the network of the linked nodes is represented as a graph $G = (V, E)$. Where V denotes the set of nodes v_i and E denotes the set of links e_i. The cardinality of $V(|V|)$ remains unchanged but $|E|$ always varies with adding or removing the links. Clustering is the partitioned graph with additional constraints. Hence, this graph is said to be as a NP-hard problem as defined in [7]. The direct linked nodes to their neighborhood nodes $\Gamma(v_i)$, are within the transmission range (R_{v_i}). This denotes the degree of the node v_i.

$$\Gamma(v_i) = (v_j, \text{ such that } \text{dist}(v_i, v_j) < R_{v_i}) \tag{1}$$

where dist(v_i, v_j) is average distance between v_i and v_j. The ratio of the power received and transmitted, is estimated by the mutual distance between the nodes. The degree of the node v_i is derived from the cardinality of the set $\Gamma(v_i)$:

$$\deg(v_i) = |\Gamma(v_i)| \tag{2}$$

In graph, each and every normal node has at least one CH neighbor and officially connects with the neighboring CH which has the least weight. But the two CH nodes cannot be neighbors [8]. In clustering algorithms, the two models are

proposed in Fast Weighted Clustered Algorithm (FWCA). One is the Node Stability, and the other is Load Balancing.

As in [2], any node can become a CH. This is explained with an example for WCA algorithm. The Fig. 1 shows the initial configuration of the nodes in the network with individual node Ids, and the fixed transmission range for each node is represented as the circles in the dotted lines. The Fig. 1a and b, represents the WCA election stage and cluster formation stage respectively. The nodes 2, 3, 4, 6, 11 from Fig. 1b are selected as CHs.

Actually, the nodes at borders and isolated, are considered as undesirable CHs. To overcome the inefficiencies observed in WCA, our contribution on the node aggregation model, defines a mathematical explanations to the set of nodes in Ad Hoc wireless networks as follows.

$$\text{Set name}(v_i) = \{v_i, \text{ such that condition}\}$$

where the *Set name* and *condition* are given in the following Table 1.

The Table 1 shows the priority of Strong Node is higher than the other nodes. Hence, the node type indicator of any node (*ntype*) is calculated as:

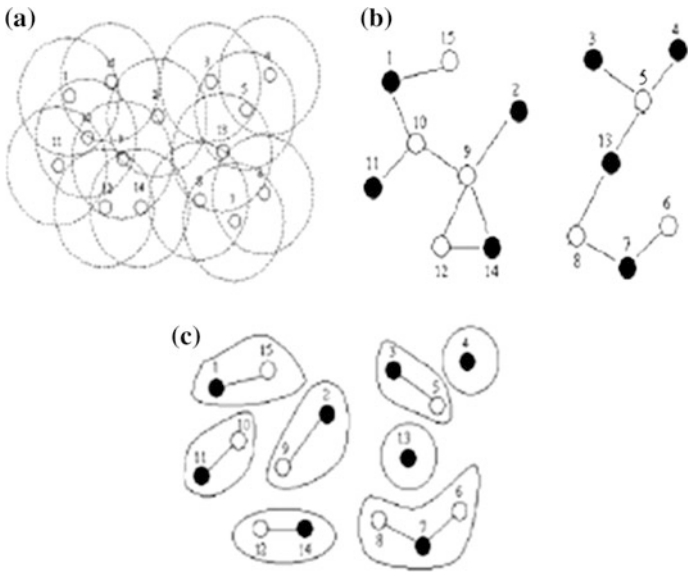


Fig. 1 **a** System's topology; **b** WCA election stage; **c** WCA formation stage

Table 1 Set nodes and their conditional representation

Set name	Strong nodes S (v_i)	Weak nodes W (v_i)	Border nodes B (v_i)	Isolated nodes I (v_i)
Condition	$\deg(v_i) \geq 3$	$\deg(v_i) = 2$	$\deg(v_i) = 1$	$\deg(v_i) = 0$

$$\text{ntype}(v_i) = \begin{cases} 1, \deg(v_i) \geq 3 \\ 2, \deg(v_i) = 2 \\ 3, \deg(v_i) = 1 \\ 4, \deg(v_i) = 0 \end{cases} \tag{3}$$

and the quality of the node is denoted by (ndq), is calculated as:

$$\text{ndq}(v_i) = \text{ntype}(v_i) \times \deg(v_i) \tag{4}$$

The density of the node (k-density) $(v_i) \in v$ is defined as the ratio between—the number of edges between (v_i) and its k-neighbors, and the number of edges between the v_i 'S k-neighbors and the number of nodes inside v_i 'S k-neighbors as in [9].

$$\rho_k(v_i) = |e = (v_j, v_k) \in Ev_j \in (v_i, \Gamma_k(v_i)\} v_k \in \Gamma_k(v_i)| / \deg(v_i) = |e(v_i)| / \deg(v_i) \tag{5}$$

As of the node mobility can be defined in the MANETs, there is a necessity of maintaining the stable cluster structure [10].

Despite the mobility of the node, it has to be kept as stable as possible if not, it effects the entire network with the performance and scheduling protocols as mentioned in [10]. Hence, we introduced a scheme which is based on the transmission variations as shown in the Fig. 2. The transmission zone of a node v_i is within the circle with radius r_2. The trusted nodes are said to be more favorable with their neighborhood of well-defined periods. The range indicator (*rind*) between the two neighbor nodes v_i and v_j is given as: $dist(v_i, v_j)$

$$\text{rind}(v_i, v_j) = \begin{cases} 1, dist(v_i, v_j) \leq r_1 \\ \alpha(r_1 - r_2), dist(v_i, v_j) < r_2 \\ 0, dist(v_i, v_j) = r_2 \end{cases} \tag{6}$$

where $0 < \alpha < 1$ is the input user coefficient adjusted by selecting the values based on the mobility range of the network. The zonal distance is the beneficial measure that can be calculated from a node v_i to the node v_j. This measure is considered along with the zone types, where the node v_i is present and calculated as:

$$\text{zonedist}(v_i, v_j) = \text{rind}(v_i, v_j) \times \text{dist}(v_i, v_j) \tag{7}$$

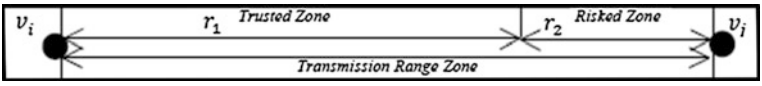


Fig. 2 Partitioning of trusted and risked zones in the transmission range zone

Based on the results obtained, there are some new parameters introduced for the Quality of Clustering. The characteristics of the clusters can be measured, and guaranteed for the predictable results. "Stability factor" of the each node depends on the zonal distance $(ZD(v_i))$ of the node v_i to all the set of its neighbor nodes $(n = |\Gamma(v_i)|)$ which are directly linked to it.

$$\mathrm{ZD}(\mathrm{v_i}) = \sum_{j=1}^{n} \mathrm{zonedist}\left(\mathrm{v_{i,}}\, \mathrm{v_j}\right) \tag{8}$$

then the stability factor,

$$\mathrm{STF}(\mathrm{v_i}) = \mathrm{ZD}(\mathrm{v_i})/\deg(\mathrm{v_i}) \tag{9}$$

In the proposed FWCA algorithm, nodes with higher $STF(v_i)$ have high possibility to be selected as CHs. The stability of this system is achieved by reducing cluster formation count and also the number of re-affiliations of other scenarios. The author in [11] specifies that the system can contain high and low-density clusters. In high-density clustering, CH will be overwhelmed with the processing load and communication, and consumes its energy quickly. But with the low-density clustering, CH will get into idle state.

Assuming that all nodes in the network are identical, that they produce the data at the same rate, and balancing with load in the circuitry, we have to balance the number of nodes in a cluster with the communication energy required per CH. For this purpose, we have to calculate the relative dissemination degree, which reflects its neighbors in a current setting as in [12].

$$\beta(\mathrm{v_i}) = |\delta \leq \deg(\mathrm{v_i})|/\deg(\mathrm{v_i}) \tag{10}$$

where $\delta \leq 2\ln(\mathrm{N})$, is a constraint on the number of nodes that a CH can handle ideally $(\mathrm{N} = |V|)$.

High power consumption is required for communication to a large distance. Hence, the authors evaluated the energy consumption by calculating it for every node v_i, the sum of distances $D(v_i)$ with its neighbors $(n = |\Gamma(v_i)|)$, as

$$\mathrm{D}(\mathrm{v_i}) = \sum_{j=1}^{n} \mathrm{dis}\left(\mathrm{v_i}, \mathrm{v_j}\right) \tag{11}$$

But the above Eq. (11) does not differentiate between favorable and unfavorable nodes. However, a CH consumes less energy if it is surrounded by favorable nodes. Our contribution is to replace Eq. (11) by (8).

The node equilibrium is the parameter that compares the stability and the load balancing of a node. It is calculated as

$$\text{equi}(v_i) = \beta(v_i) \backslash \text{STF}(v_i). \tag{12}$$

If $equi(v_i) > 1$, then the node is more load balanced than stable, otherwise it is more stable.

If $equi(v_i) = 1$, then the node is said to be simultaneously stable and load balanced.

3 Proposed Methodology in Brief

The FWCA algorithm effectively combines the system parameters with certain weighting factors selected accordingly to the system needs. This algorithm can be applied in the networks to make flexible changes in the weight factors as in [2]. The result of the CH election process is a set of some nodes called the dominant set. This process is invoked at the time of the system activation and when current dominant set is unable to cover all the nodes. It is not necessary to elect all the CHs in the previous dominant set with new replacements. If a node detaches itself from its current CH and attaches to other CH, then these are updated with the member list instead of invoking the election algorithm with reference to [13–15]. The structure of the FWCA contains two sections as CH selection and Cluster members' set formation. The CH selection process defines with FWCA algorithm.

Algorithm 1

Input: G(V,E), neighborhood, distances
Output: Set of clusterheads

1. For each node $\mathbf{v_i} \in \mathbf{G}$
2. Begin
3. Find the neighbors of $\mathbf{v_i}$ using (2)
4. Calculate Energy consumption using (9)
5. Calculate Stability Factor using (10)
6. Evaluate Relative Dissemination Degree using (11)
7. Calculate Remaining Battery energy.
8. Calculate the combined weight $\mathbf{W(v_i) = w_1 ZD(v_i) + w_{2R} RBE(v_i) + w_3 STF(v_i) + w_4 \beta(v_i)}$
9. $\mathbf{CW \leftarrow W(v_i)}$
10. End
11. Sort **CW** in increasing order
12. While **CW** is not empty
13. Begin
14. $\mathbf{v_i \leftarrow CW}$ /* Extract the first node v_i
15. $\mathbf{CH \leftarrow v_i}$
16. Delete node $\mathbf{v_i}$ from **CW**
17. Delete all $\mathbf{\Gamma(v_i)}$ from **CW**
18. End
19. End

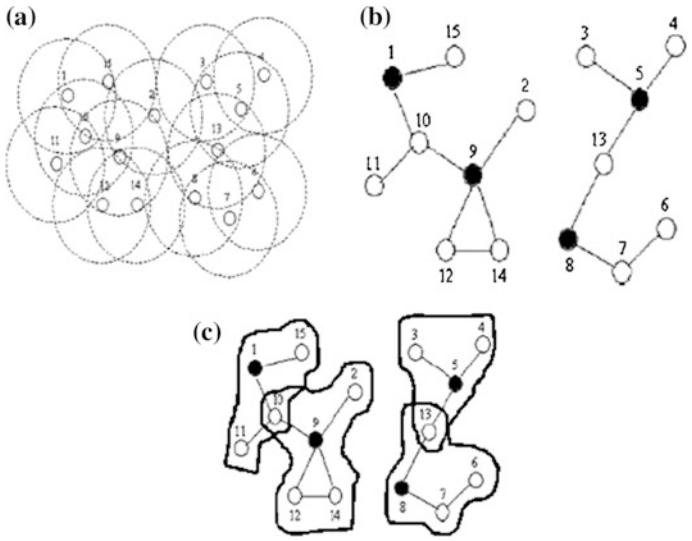


Fig. 3 **a** Network topology. **b** Election stage. **c** Cluster formation stage

The cluster member formation constitutes the last stage of the algorithm, and represents the cluster member' set which can be seen in the Fig. 3c. Each of the CH defines it neighbors at maximum of two hops, which forms the members of the cluster. Each cluster head stores the information about its members. All the nodes in the network record the cluster head identifier. This exchanging of the information allows the routing protocol to function in and between the clusters. The nodes move in different directions with various speeds provoking the configuration of that cluster. Consequently, the placements of that particular nodes and the speeds must be updated periodically. The speed of the node generates the choice of the updated time slots, since the speed is responsible for the change in its positions.

These periodical updates with the higher frequencies should be avoided as they provoke the power consumption through batteries and hence increases in the configuration changes.

4 Conclusion

The main aim of this project is to organize the nodes with wireless Ad Hoc networks in clusters and fill-up the robustness where the topological changes may cause by the factors like node insertion, node deletion, node motion and node failures. We implemented the new strategy of stable clustering based on the previous workouts. And a brief explanation of simple clustering load balancing scheme

in the same strategy. The proposed scheme overcomes the inefficiencies found in WCA and is resulted in the high performance comparing to the other similar cluster algorithms.

References

1. Maher Khemakhem and Abdelfettah Belghith, "A multipurpose multi-agent system based on a loosely coupled architecture to speed-up the DTW algorithm for arabic printed cursive OCR", (AICCSA-05), Cairo, Egypt, January 3–6 (2005).
2. M. Chatterjee, S. K. Das, and D. Turgut. WCA: a weighted clustering algorithm for mobile Ad Hoc networks. Cluster Computing 5, 193–204 (2002).
3. S. Muthuramalingam, R. RajaRam, Kothai Pethaperumal and V. Karthiga Devi. A Dynamic Clustering Algorithm for MANETs by modifying Weighted Clustering Algorithm with Mobility Prediction. International Journal of computer and Electrical Engineering Aug., Vol. 2, No. 4, 1793–8163 (2010).
4. Christian Bettstetter. The Cluster Density of a Distributed Clustering Algorithm in Ad Hoc Networks. IEEE International Conference Communications; Page(s): 4336–4340 Vol. 7 (2004).
5. S. K.B. Rathika and J. Bhavithra. An Efficient Fault Tolerance Quality of Service in Wireless Networks Using Weighted Clustering Algorithm; Bonfring International Journal of Research in Communication Engineering Feb.; Vol. 2, Special Issue 1, Part 4 (2012).
6. F. Tolba, D. Magoni, P. Lorenz. A stable clustering algorithm for highly mobile Ad Hoc networks. P. Second International Conference on Systems and Networks Communication 2007. ICSNC (2007).
7. B. Bollbas. Random Graphs. Academic Press. (1985).
8. S. Basagni. Distributed clustering for ad hoc networks. In: Proc. Intern. Symp. Parallel Architectures, Algorithms, and Networks (ISPAN); (Perth/Fremantle, Australia) Jun. (1999).
9. G. Gupta, Mohamed Younis. Load-balanced clustering of wireless sensor networks, IEEE International Conference on Communications, ICC '03 (2003).
10. Mitton, N., Busson, A., & Fleury. Self-organization in large scale ad hoc networks. In Mediterranean ad hoc Networking Workshop, E. Jun. (2004).
11. Mohamed Aissa, Abdelfettah Belghith. An Efficient Scalable weighted clustering algorithms for mobile Ad Hoc networks. ICITES' 2013, the 3th International Conference on Information Technologies and E-Services; March 24–26, Sousse, Tunisia (2013).
12. Suchismita Chinara, Santanu Kumar Rath. A Survey on One-Hop Clustering Algorithms in Mobile Ad Hoc Networks. Journal Network. System Management; 17:183–207 (2009).
13. Imen Jemili, Abdelfettah Belghith and Mohamed Mosbah, "Algorithme distribué de clusterisation sans connaissance du voisinage: principe et évaluation", NOTERE 2007, Marrakech, Marocco, Jun. 4–8 (2007).
14. Imed Lassoued, Jean Marie Bonnin and Abdelfettah Belghith, "Towards an Architecture for Mobility Management and Resource Control", The IEEE Wireless Communications and Networking Conference WCNC 2008, Las Vega, USA, Mar. 31-April 3 (2008).
15. Imen Jemili, Abdelfettah Belghith and Mohamed Mosbah, "A Synchronous Tiered Based Clustering Algorithm for large-scale Ad hoc Networks", The 10th IFIP MWCN'08, Toulouse, Farnce, Sept. 29–30 (2008).

Modified LEACH Protocols in Wireless Sensor Networks—A Review

D. Rajendra Prasad, P.V. Naganjaneyulu and K. Satya Prasad

Abstract A Wireless Sensor Network (WSN) is a node of sensors of large number with insufficient energy, storage space, and processing power. Collecting data and forwarding them to Base Station (BS) is the important tasks of the sensor nodes. Therefore, to design the gathering schemes effectively, the lifetime of the network is the main criteria in WSN.LEACH is a protocol based on cluster to rotate the cluster head randomly for distributing the load energy randomly between sensors in the network. To minimize the data quantity, the data aggregation method has been incorporated into the routing protocol to transmit from CH to BS. In this paper, we have surveyed and analyzed different hierarchical routing protocols that are being modified from LEACH.

Keywords WSN · Base station (BS) · LEACH · Energy-efficient LEACH (EE-LEACH)

1 Introduction

WSN typically comprises several autonomous sensors. These sensors are often employed to monitor atmosphere, climate features and other systems. Recent bidirectional networks enable sensor control activity. In general, a small device of three basic workings: a subsystem for sensing physical nearby condition for data acquisition, a subsystem for processing data and storage, and for transmission of data, a wireless communication subsystem [1].

D. Rajendra Prasad (✉)
Department of ECE, St. Ann's College of Engineering & Technology, Chirala, India
e-mail: rp.devathoti@gmail.com

P.V. Naganjaneyulu
MVR College of Engineering & Technology, Vijayawada, India

K. Satya Prasad
Department of ECE, Jawaharlal Nehru Technological University, Kakinada, India

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5_72

Node deployment is one of key characters of WSN, which started dominating the Mobile Ad hoc Networks (MANET). Data redundancy is another feature by which sensors are deployed thickly in region of interest in the application of sensor network to achieve an ordinary sensor's task. Sensor network with a precise application is intended and deployed. Also the sensed data by the nodes in the sensor flows from different sources to the exact sink [2].

LEACH is a protocol based on cluster to rotate the cluster head randomly for distributing the load energy randomly between sensors in the network. To minimize the data quantity, the data aggregation method has been incorporated into the routing protocol to transmit from CH to BS. In setup phase, cluster formation has been done and it has three steps. In the first step, for becoming the CHs, the self-elected candidates promote their intentions and in the second step, it received the promotion messages from the CH to join based upon the signal strength. In the final step, CHs launch the schedule messages of Time Division Multiple Access (TDMA) [3].

LEACH protocol has some features: in setup phase, the clusters are localized by coordination and control. The CH is manipulated for distributing the energy necessities between the network nodes. Compression techniques are used for reducing the amount of data transmission in CH and for identical networks it is best suited [4].

LEACH Protocols has some advantages: LEACH has achieved reduction factor of 7 in the dissipation of energy over direct communication and 4–8 factor over the minimum transmission in the energy routing protocol. Randomly the nodes die and increase the lifetime of the dynamic clustering system. LEACH is distributed completely and no global knowledge is required in the network. The limitation in LEACH Protocol is that the nodes are sending the data including CH by the similar initial energy. The CH numbers are predefined with 5 or 10% total nodes. To cover all area it may not be sufficient for the evenly distributed sensor nodes. The CHs are selected randomly in the node and are concentrated in one area; for cluster formation, the residual energy is not measured. Therefore, a few nodes in the area have no CH in their network and also it does not provide appropriate CH location. In single hop way, the aggregated data are sent from CHs to BS and in large regions. LEACH is not suitable for the deployed networks [5].

By M-LEACH, the distributed setup phase is modified to select appropriate cluster-head-based on the attenuation model. To minimize the attenuation power, optimal CHs are selected [6].

Energy-Efficient Extended LEACH (EEE LEACH) is a method of multilevel clustering for reducing energy efficiency by minimizing the distance of radio communication distance. Transmission typically takes place from first CH to corresponding CH by means of fuse mechanism; the CHs aggregate the received data; Master CHs (MCH) are formed in the second layer; and the nearest MCHs are searched by the CHs to calculate the distance among them. In EEE LEACH, the MCHs numbers are kept less than the CHs numbers for minimizing communication distance among the nodes and BS. EEE LEACH protocol has performed enhanced network lifetime and is more energy-efficient over LEACH protocol [7].

2 Related Work

Sharma and Sharma [8] proposed a modified LEACH protocol called EEE LEACH protocol. The new version LEACH protocol recognizes an approach of multilevel clustering to minimize the communication distance among nodes and proposed MCH with CHs. Simulations had been done in MATLAB and the results had showed that EEE LEACH was more energy-efficient than LEACH protocol.

Christian and Soni [9] introduced LEACH with well-liked cluster-based structures in WSN. This work used the Improved LEACH (ILEACH) protocol and compared it to LEACH protocol. In terms of FND (First Node Dies) and HND (Half of the Nodes Die) lifetime sensors was evaluated to take care for the consistency and efficiency of the power in WSN.

Mehta et al. [10] developed an Equalized Cluster LEACH (C-LEACH) to initialize and maintain even-sized clusters for locating transversely in the network. From viewpoint of the energy constraints, this algorithm has involved minimum routing processing overhead to extend the setup phase of conventional LEACH. It also incorporated "adoption" concept for orphaned the cluster nodes efficiently to incorporate into adjacent clusters.

El and Shaaban [11] projected a Modified Security-LEACH (MS-LEACH) which provides security to the data and authentication to the CH node by using pairwise keys that are shared among CHs. Investigation had showed that it had effective security features and achieved WSN security goals. With reference to several existing protocol, which are specific for security purpose, the version of MS-LEACH appears to be dominating with its obvious efficient secured characteristics.

Xu et al. [12] proposed Enhanced-LEACH (E-LEACH) to enhance the hierarchical routing protocol LEACH. In this, selecting the CH was in a random way and fixed in the round time. For balancing the network load, it considered remnant power in the sensor node and the round time changes was dependent on the cluster size. The simulation results had showed that this protocol had increased network lifetime by 40% over the LEACH algorithm.

Jan et al. [13] enhanced the sensor network lifetime by LEACH protocols and proficiently utilized the limited energy accessible in the sensor nodes. The base station in sensor network was not important for the delivered data but the quality of the data was most important. It enhanced the lifetime and value of the delivered data in sensor network. This work had evaluated the approach by using multiple node sets of energy levels. This approach had showed significant development when compared to the existing cluster-based hierarchical routing protocols. This work had evaluated the system in energy consumption, lifetime and value of delivered data at the base station.

Salim et al. [14] projected the LEACH routing protocol was measured and enhanced. This author had performed a cluster-based routing protocol named as Intra-Balanced LEACH (IBLEACH), to extend LEACH protocol by means of harmonizing the energy consumption. The simulation results had showed that

IBLEACH outperformed LEACH and the obtainable developments of LEACH in terms of lifetime network and minimizing energy.

Masdari et al. [15] proposed the safe LEACH and its security textures of all solution and emphasize their objectives, advantages and limitations. Also, these works classified safe LEACH system into cryptographic-based and trust-based solutions and assessed the main improvement in these two categories. It presented a valued comparison based upon different security metrics on safe LEACH systems. Finally, this work concluded by open research problems.

Mahmood et al. [16] studied accurately about cluster-based routing in WSN. Additionally, "LEACH" can be modified as MODified LEACH (MODLEACH) by efficient CH replacement systems and dual transmission power levels. The modified LEACH was compared with LEACH and had outperformed metrics of CH data, throughput and network life. After that, hard thresholds and soft thresholds were implemented based on MODLEACH to boost the performance further. Lastly, a concise performance investigation of LEACH, MODLEACH with Hard Threshold (MODLEACHHT) and MODLEACH with Soft Threshold (MODLEACHST) had been undertaken by considering the metrics of throughput, network life and cluster head replacements.

Aslam et al. [17] offered energy-efficient hierarchical routing protocols from conservative LEACH routing protocol. The major focus was to extend the protocols to increase the lifetime and to improve the quality of the routing protocol for WSNs. In addition, this work had highlighted few problems faced by LEACH and explained how to handle these problems by extensive versions of LEACH. This work had compared with the selected hierarchical routing protocols of features and performance problems.

Zhao et al. [18] enhanced the convention equation used to select CHs for considering the dynamic node energy change. In the meantime, this work was to establish a vice CH in communication process for each cluster aiming to diminish the energy consumption on clustering and extended the time in steady-state phase. Simulations had showed that the enhanced protocol had performed better over the LEACH and the LEACH-C.

Iqbal et al. [19] projected and evaluated Advanced Low-Energy Adaptive Clustering Hierarchy (Ad-LEACH) of static clustering-based heterogeneous routing protocol. The entire network field was split into static clusters and in all the clusters separate Ad-LEACH protocol had been applied. This protocol with CH selection criterion had been inherited from LEACH Distributed Energy-Efficient Clustering (DEEC). This had enabled Ad-LEACH to cope with different nodes. Because of small static clusters, all nodes had reduced their transmit message power, since it covered onlya small region. This work was modeled in MATLAB for checking the effectiveness of Ad-LEACH. The simulation results showed that the Ad-LEACH outperformed LEACH and DEEC in energy efficiency with throughput.

Lu et al. [20] proposed a version of LEACH, which later emerged as an excellent protocol termed for clustering and widely expanded its application in WSN. However, in this version, the nodes had fast energy consumption and diminished corresponding energy efficiency. This is due to the reason that the near as well as

the distant energy nodes from BS are turned into cluster head nodes. By investigating the respective model, several significant factors were considered: The corresponding energy in all the nodes, the frequency of existence of nodes was chosen for the CH. Similarly the distance implied with the nodes and BS to change the threshold node function can eventually lead to extend the life of the respective network. This clearly realized the balancing of energy in network. The simulation results had indicated that new protocol extended network's lifetime and also balanced the energy consumption.

Bara's and Khalil [21] projected the performance of Evolutionary Algorithms (EAs) with cluster routing problem by means of formulating a novel fitness function to incorporate two clustering aspects, namely cohesion and partition error in WSN. Simulation of 20 random WSNs had showed the Evolutionary-based clustered Routing Protocol (ERP) extended the network's lifetime, preserved more energy when compared to the results obtained from the existing heuristics like LEACH, Stable Election Protocol (SEP), and Hierarchical Cluster-based Routing (HCR) protocols. In addition, ERP had outperformed LEACH and HCR in extending the constancy period when compared to SEP for various networks with extra 10% heterogeneity, but it needed further heterogeneous-conscious alteration with 20% of node heterogeneity.

Mitra and Biswas [22] proposed a hierarchical clustering algorithm called LEACH for sensor networks. This method had described two ways for selecting CH. Analysis had showed that Enhanced-LEACH protocol had balanced the energy expenditure, saved the node energy and extended the network's lifetime.

Shi et al. [23] offered an energy-effective Optimized LEACH-Centralized. Using LEACH-C, a group of CHs were selected. Next, to create a model for CH energy conservation, it considered retransmission and recognition. From all CH to the node member, it then calculated the quadratic sum distances for optimal solution. Lastly, for single CH in second round the main energy consumption was estimated and the residual node energy was bigger than the intended consumption which was taken to a new round for simulated annealing to find an improved solution. Hence, CH loss in all the rounds can be reduced and the lifetime could be extended ultimately in WSN.

Shankar et al. [24] projected adaptative clustering protocol to produce optimum energy intake for WSNs, and consequent in an extended network lifetime. The preparation phase had been performed at a time in first round ahead of setup phase. In all the rounds of setup phase and steady-state phase, the processes were similar as in LEACH. Simulations outcomes had showed that LEACH outperformed a reduction factor of 8 in energy dispersion, when compared to customary routing protocols. Additionally, LEACH had uniformly distributed energy dispersion in the sensors for doubling network lifetime.

Tripathi et al. [25] proposed clustered routing protocol and described LEACH compromisation by Black hole and Gray Hole attacker of WSN. To imitate this attacks on NS-2 "high energy threshold" approach had been used. The WSN execution for the attack had been investigated thoroughly by means of applying multiple network parameters with multiple node densities. It had been determined

that the black hole attack effect's performance was much more when compared to the gray hole attack.

Manzoor et al. [26] focused to extend the lifetime of a network for efficient resource utilization in WSNs. Multiple approaches based on clustering were projected for optimal functionality. Sensor node energy was related to the network lifetime at distant region for invariant fault patient monitoring. Here, Quadrature-LEACH (Q-LEACH) enhanced the stableness, network's lifetime and throughput for similar networks.

Ahlawat and Malik [27] investigated clustering routing protocol LEACH and its demand and proposed better V-LEACH. An improved V-LEACH protocol had been done on Vice CH selection. The Vice CH was an alternative head to work if CH would die. The Vice CH selection process has three basic factors: minimum distance, maximum residual energy and minimum energy. This approach had improved the network's lifetime when the CH will die. It replaced its Vice CH when CH would die. After the simulations, it was found that the improved V-LEACH had outperformed the true version of LEACH to increase the network's lifetime 49.37%.

Zhang et al. [28] introduced an energy-balanced routing scheme based upon Forward-Aware Factor (FAF-EBRM), the adjacent-hop node had been selected in accordance with the link weight and forward energy compactness. Moreover, a natural reconstruction execution for localized topology had been designed. In the research, FAF-EBRM had been compared to LEACH and EEUC, simulations results had been showed that the FAF-EBRM had been outperformed LEACH and EEUC to balance the energy consumption, to extend the lifetime and guaranteed the advanced Quality of Service (QoS) in WSN.

Geetha et al. [29] proposed to optimize numerous routing protocols to optimize efficiency on resource constraints in WSN. The clustering algorithms gained significance as it increases the WSN lifetime due to the CH selection and data aggregation approach. LEACH as an initial clustering routing protocol proved better when compared with other algorithms. This work had compared with two significant clustering protocols, LEACH and LEACH-C (centralized), by means of NS2 tool for various conditions chosen and the simulated results for the performance metrics was against in latency and lifetime of the network. This work was concluded by commenting the observance made on the simulated results on these protocols.

Gambhir and Fatima [30] provided a model LEACH protocol version called as Optimized LEACH (OP-LEACH) to reduce the energy intake in the WSN. Both current LEACH and projected OP-LEACH were evaluated by means of simulations using simulator OMNET++ had showed that the Op-LEACH had performed better over LEACH protocol.

Subhashree et al. [31] proposed IBLEACH, a clustering routing protocol to extend LEACH protocol by means of balancing the energy conservation of the network. The simulation results had showed that IBLEACH outperformed LEACH and the current advancements of LEACH in network lifetime and energy intake minimization.

3 Conclusion

In this survey paper, the authors have discussed the three versions of LEACH protocols from the perspective of implementation in WSN applications. The emphasis of the literature survey corresponds to focus the research carried for examining the energy efficiency. Similarly the study also performed to explore the maximization of the throughput.

References

1. Bokare. M., Ralegaonkar. M. A.: Wireless sensor network: A promising approach for distributed sensing tasks. Excel Journal of Engineering Technology and Management Science, 1(1), 1–9. (2012).
2. Goyal. D., Tripathy. M. R.: Routing protocols in wireless sensor networks: a survey. In 2012 Second International Conference on Advanced Computing & Communication Technologies (pp. 474–480). IEEE, (2012, January).
3. Rahayu. T. M., Lee. S. G., Lee. H. J.: Survey on LEACH-based security protocols. In 16th International Conference on Advanced Communication Technology (pp. 304–309). IEEE, (2014, February).
4. Madheswaran, M., Shanmugasundaram, R. N.: Enhancements of leach algorithm for wireless networks. The proceedings of Journal On Communication Technology, 4, 821–827. (2013).
5. Bakaraniya. P., Mehta. S.: K-LEACH: An improved LEACH protocol for lifetime improvement in WSN. International journal of engineering trends and technology, 4(5), 1521–1526. (2013).
6. Choudhary, S., Sharma, S.: A Survey of LEACH Protocol and its Modified Versions in Wireless Sensor Network. International Journal of Advanced Research in Computer Science and Software Engineering, 4(1), 850853. (2014).
7. Sharma, M., Shaw, A. K.: Transmission time and throughput analysis of EEE LEACH, LEACH and direct transmission protocol: a simulation based approach. Advanced Computing, 3(6), 75. (2012).
8. Sharma. M., Sharma. K.: An energy efficient extended LEACH (EEE LEACH). In Communication Systems and Network Technologies (CSNT), 2012 International Conference on (pp. 377–382). IEEE. (2012, May).
9. Christian. A., Soni. H.: Lifetime prolonging in LEACH protocol for wireless sensor networks. In Intelligent Systems and Signal Processing (ISSP), 2013 International Conference on (pp. 350–355). IEEE. (2013, March).
10. Mehta. R., Pandey. A., Kapadia. P.: Reforming clusters using C-LEACH in wireless sensor networks. In Computer Communication and Informatics (ICCCI), 2012 International Conference on (pp. 1–4). IEEE. (2012, January).
11. El. M., Shaaban. E.: Enhancing S-LEACH security for wireless sensor networks. In Electro/Information Technology (EIT), 2012 IEEE International Conference on (pp. 1–6). IEEE. (2012, May).
12. Xu. J., Jin. N., Lou. X., Peng. T., Zhou, Q., Chen. Y.: Improvement of LEACH protocol for WSN. In Fuzzy Systems and Knowledge Discovery (FSKD), 2012 9th International Conference on (pp. 2174–2177). IEEE, (2012, May).
13. Jan. M. A., Nanda. P., He. X., Liu. R. P.: Enhancing lifetime and quality of data in cluster-based hierarchical routing protocol for wireless sensor network. In High Performance Computing and Communications & 2013 IEEE International Conference on Embedded and

Ubiquitous Computing (HPCC_EUC), 2013 IEEE 10th International Conference on (pp. 1400–1407). IEEE. (2013, November).
14. Salim. A., Osamy. W., Khedr. A. M.: IBLEACH: intra-balanced LEACH protocol for wireless sensor networks. Wireless networks, 20(6), 1515–1525. (2014).
15. Masdari. M., Bazarchi. S. M., Bidaki. M.: Analysis of secure LEACH-based clustering protocols in wireless sensor networks. Journal of Network and Computer Applications, 36(4), 1243–1260. (2013).
16. Mahmood, D., Javaid, N., Mahmood, S., Qureshi, S., Memon, A. M., Zaman, T.: MODLEACH: a variant of LEACH for WSNs. In Broadband and Wireless Computing, Communication and Applications (BWCCA), 2013 Eighth International Conference on (pp. 158–163). IEEE. (2013, October).
17. Aslam, M., Javaid, N., Rahim, A., Nazir, U., Bibi, A., Khan, Z. A.: Survey of extended LEACH-Based clustering routing protocols for wireless sensor networks. In High Performance Computing and Communication & 2012 IEEE 9th International Conference on Embedded Software and Systems (HPCC-ICESS), 2012 IEEE 14th International Conference on (pp. 1232–1238). IEEE. (2012, June).
18. Zhao, F., Xu, Y., Li, R.: Improved LEACH routing communication protocol for a wireless sensor network. International Journal of Distributed Sensor Networks, 2012. (2012).
19. Iqbal, A., Akbar, M., Javaid, N., Bouk, S. H., Ilahi, M., Khan, R. D.: Advanced LEACH: A static clustering-based heteroneous routing protocol for WSNs. arXiv preprint arXiv:1306.1146. (2013).
20. Lu, Y., Zhang, D., Chen, Y., Liu, X., Zong, P.: Improvement of leach in wireless sensor networks based on balanced energy strategy. In Information and Automation (ICIA), 2012 International Conference on (pp. 111–115). IEEE. (2012, June).
21. Bara'a, A. A., Khalil, E. A. A new evolutionary based routing protocol for clustered heterogeneous wireless sensor networks. Applied Soft Computing, 12(7), 1950–1957.
22. Mitra, R., & Biswas, A. (2012). Enhanced clusterhead selection algorithm using leach protocol for wireless sensor networks. International Journal Of Computational Engineering Research, 2(3), 766–770. (2012).
23. Shi, S., Liu, X., Gu, X.: An energy-efficiency Optimized LEACH-C for wireless sensor networks. In Communications and Networking in China (CHINACOM), 2012 7th International ICST Conference on (pp. 487–492). IEEE. (2012, August).
24. Shankar, M., Sridar, M., Rajani, M.: Performance evaluation of LEACH protocol in wireless network. International Journal of Scientific & Engineering Research, 3(1), 1. (2012).
25. Tripathi, M., Gaur, M. S., Laxmi, V.: Comparing the impact of black hole and gray hole attack on LEACH in WSN. Procedia Computer Science, 19, 1101–1. (2013).
26. Manzoor, B., Javaid, N., Rehman, O., Akbar, M., Nadeem, Q., Iqbal, A., Ishfaq, M. Q-LEACH: A new routing protocol for WSNs. Procedia Computer Science, 19, 926–931. (2013).
27. Ahlawat. A., Malik. V.: An extended vice-cluster selection approach to improve v leach protocol in WSN. In Advanced Computing and Communication Technologies (ACCT), 2013 Third International Conference on (pp. 236–240). IEEE. (2013, April).
28. Zhang, D., Li, G., Zheng, K., Ming, X., Pan, Z. H.: An energy-balanced routing method based on forward-aware factor for wireless sensor networks. IEEE transactions on industrial informatics, 10(1), 766–773. (2014).
29. Geetha, V. A., Kallapur, P. V., Tellajeera, S.: Clustering in wireless sensor networks: performance comparison of LEACH & LEACH-C protocols using NS2. Procedia Technology, 4, 163–170. (2012).
30. Gambhir, S., Fatima, N.: Op-LEACH: an optimized LEACH method for busty traffic in WSNs. In 2014 Fourth International Conference on Advanced Computing & Communication Technologies (pp. 222–229). IEEE. (2014, February).
31. Subhashree, V. K., Tharini, C., Lakshmi, M. S.: Modified LEACH: A QoS-aware clustering algorithm for Wireless Sensor Networks. In Communication and Network Technologies (ICCNT), 2014 International Conference on (pp. 119–123). IEEE. (2014, December).

Index

S.C. Satapathy et al. (eds.), *Proceedings of 2nd International Conference on Micro-Electronics, Electromagnetics and Telecommunications*,
Lecture Notes in Electrical Engineering 434, DOI 10.1007/978-981-10-4280-5