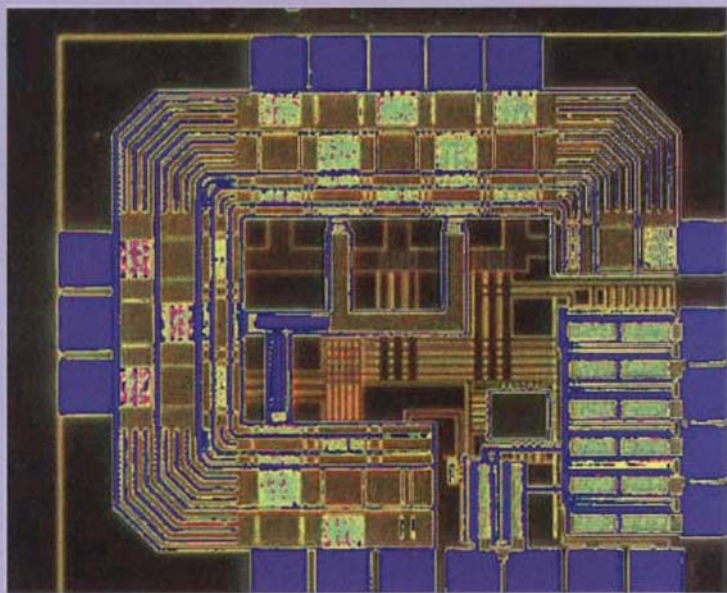# RF CMOS Power Amplifiers

Theory, Design and Implementation

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RF CMOS Power Amplifiers:
Theory, Design and Implementation

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Theory,Design and Implementation

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Preface

The convergence of home electronics, computer, and communication technologies is one of the most exciting technological and business trends of the next decades. The key to a wireless solution is the building of intelligent units, that can communicate clearly in a wire-free environment, occupy as little space as possible, and consume low power to maximize battery life. All these criteria are best met by highly integrated, low power, battery operated micro-systems.

Wireless applications are witnessing tremendous growth with proliferation of different standards covering wide, local and personal area networks (WAN, LAN and PAN). The trends call for designs that allow 1) smooth migration to future generations of wireless standards with higher data rates for multimedia applications, 2) convergence of wireless services allowing access to different standards from the same wireless device.

The key to integration, and reduction in costs is the correct choice of the implementation technology. CMOS technology has played an important role in providing higher functionality and complexity at low costs.The performance of power amplifiers is a crucial issue for the overall performance of the transceiver's chain. Until now, power amplifiers for wireless applications have been produced almost exclusively in GaAS technologies, with few exceptions in LD-MOS, Si BJT, and SiGe HBT. Sub-micron CMOS processes are now considered for power amplifier design due to the higher yield, and the lower costs it can provide. A typical power amplifier module for wireless communications consists of 3 dies, and 15-20 passive components plus decoupling. A CMOS power amplifier design solution could lead to component count that can be reduced to one die and 3-5 passives plus decoupling. This reduction in component count leads to a significant reduction in power amplifier cost.

The is the first monograph addressing RF CMOS power amplifier design for emerging wireless standards.The focus will be on power amplifiers for short distance wireless personal and local area networks (PAN and LAN), however the design techniques are also applicable to emerging wide area networks

(WAN) infrastructures using micro or pico cell networks. The book discusses CMOS power amplifier theory and design principles, describes the architectures and tradeoffs in designing linear and nonlinear power amplifiers. It then details design examples of RF CMOS power amplifiers for short distance wireless applications (e.g,Bluetooth, WLAN) including designs for multi-standard platforms. Design aspects of RF circuits in deep submicron CMOS are also discussed.

This book will serve as a reference for RF IC design engineers , RF and R&D managers at industry, and for graduate students conducting research in wireless semiconductor IC design in general and with CMOS technology in particular. The book focuses mainly on the design procedure and the testing issues of CMOS RF power amplifiers and is divided into five main chapters.

Chapter 2 discusses the basic concepts of power amplifiers; optimum load, load line theory, and gain match versus power match. Performance parameters such as efficiency and linearity are presented. Different power amplifier classes are discussed and compared in terms of linearity and efficiency. Finally some common power amplifier linearization techniques are briefly investigated.

Chapter 3 presents the design and optimization techniques used to implement a 900MHz class E power amplifier. The theory behind class E operation is illustrated, the effects of some circuit components on the performance of the amplifier are demonstrated. The potential for applying the same concepts to multi-standard operation is also discussed. Finally testing procedure and measurement results are given.

Chapter 4 deals with extending the limits of the used technology to achieve 2.4GHz operation, and satisfy the Bluetooth standard. This is the first reported work on class 1 Bluetooth power amplifiers. Section 4.2 describes the details of the 2.4GHz power amplifier design, together with the implementation of the power control mechanism. Section 4.3 presents the simulation results, while experimental data is given in section 4.4. Chapter 5 presents an improved version of the power amplifier , using 0.18 micron technology in which class 1, class2, and class 3 power amplifiers are implemented. Finally conclusions are drawn in chapter 6.

This book has its roots in the doctoral dissertation work of the first author at the Analog VLSI Lab,The Ohio State University. We would like to thank all those who supported us at the Analog VLSI Lab and at other locations including the Radio Electronics Lab at the Swedish Royal Institute of Technology, and Spirea AB, Stockholm.

MONA MOSTAFA HELLA, MOHAMMED ISMAIL

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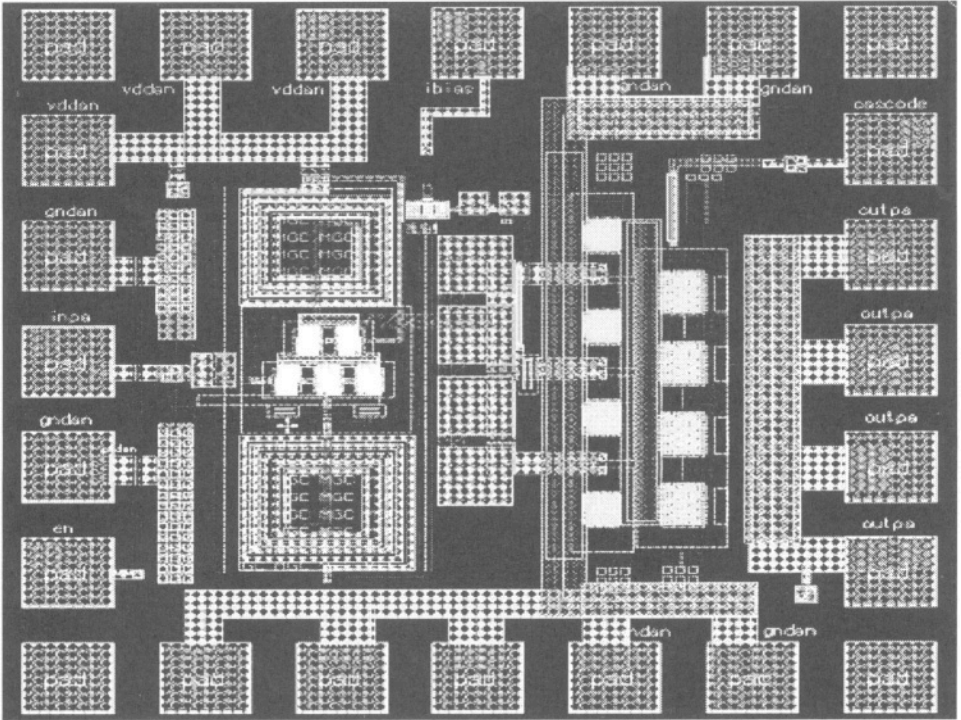
Figure 5.17. The layout of $0.18\mu m$ CMOS PA for class 1 Bluetooth standard.

the operation of the power amplifiers have been verified with simulation results at different operating conditions.

Chapter 1

INTRODUCTION

1. RF CMOS Transceivers

The expansion of the market for portable wireless communication devices has given tremendous push to the development of a new generation of low power radio frequency integrated circuit (RFIC) products. Cellular and cordless phones, pagers, wireless modems, and RF ID tags, require more compact and power saving solutions to accommodate the ever-growing demand for lighter and cheaper products [1]. These listed devices use different standards employing a wide range of frequency from 900MHz to 5.6GHz.

Radio frequency integrated circuits, RFIC's, have to deal with performance issues such as noise, both broadband and near carrier, linearity, gain, and efficiency, in addition to the traditional requirements of power dissipation, speed, and yield. As a result, the optimum integrated circuit technology choices for RF transceivers in terms of optimum devices and levels of integration, are still evolving. Engineers planning to implement wireless transceivers are confronted with various possibilities: silicon CMOS, BiCMOS, and bipolar technologies, GaAs MESFET, hetero-junction bipolar transistor (HBT), and PHEMT, as well as discrete filters. Traditional commercial implementation of high performance wireless transceivers typically utilizes a mixture of these technologies in order to implement a complete system [2]. Even though RF designs contain fewer devices compared to digital chips, they are inherently more challenging, as very little automation is available for the design process. More-over, RF devices are typically pushed to their performance limits; thus, all the nonlinearities and second order effects need to be taken into account.

The optimum goal is to achieve low cost, low power, and high volume implementation of radio functions that are traditionally implemented using bulky, expensive, and power hungry hybrid components. Additionally, developers of

Reference	Architecture	Application	Technology	Power
[4]	Homodyne	ISM band	1.0μm CMOS	177mW
[5]	Wideband-IF	DECT	0.6μm CMOS	198mW
[6]	Low-IF	DCS1800	0.25μm CMOS	192mW
[7]	Weaver	GSM/DCS1800	0.6μm CMOS	72mW/75mW
[8]	Heterodyne	GSM	0.25μm CMOS	50mW

Table 1.1.   Performance summary of CMOS RF transceivers

new wireless applications are also looking to provide consumers with both the convenience of added connectivity and the benefit of additional services provided by a transceiver able to operate with multiple RF standards. The VLSI capabilities of CMOS make this technology particularly suitable for very high levels of mixed signal radio integration while increasing the functionality of a single chip radio to cover multiple RF standards [3]. At the research level, CMOS RF technology is already expanding its applications to radio systems with stringent requirements such as cellular telephony, as shown in table 1.1, based on the work in [4], [5], [6], [7], [8]. For compact low cost, and low power portable devices, the prospect of a single chip CMOS radio has received considerable interest, even though it remains to be researched whether it is feasible to put the RF front end on the same die with the rest of the mobile terminal. Even the less ambitious objective of implementing the mobile phone as a set of separate chips in the same CMOS technology may bring considerable economic benefits [9].

2.   CMOS Short Range Wireless Transceivers

The implementation of a single chip CMOS transceiver has recently been commercially available thanks to the fast growth of wireless computing technologies. Short-range wireless communication systems such as IEEE 802.11, Wireless Local Area Network (WLAN) and the Bluetooth standards have made wireless computing and other broadband services possible. Each radio device covers 10-100m range, and is required to have high bit rate. A short-range wireless system can be used in an environment where users are highly mobile such that wired network installations would require higher costs. Thus, there is much interest today in single-chip wireless transceivers which consume a small amount of power, need no off-chip components, support voice and data traffic over short ranges by transmitting modest power, implement power control, and are resilient to interferes [4].

The development that took place in the area of wireless communications is evident by comparing two figures. The first figure (Figure 1.1) is the traditional super-heterodyne transceiver, implemented using a combination of several in-

tegrated circuits built using different technologies: GaAs, bipolar, and ceramic SAW filters are used for the RF section, bipolar for the IF section, and CMOS for base band. This design partitioning has changed recently, thanks to the advance in CMOS technology [1].
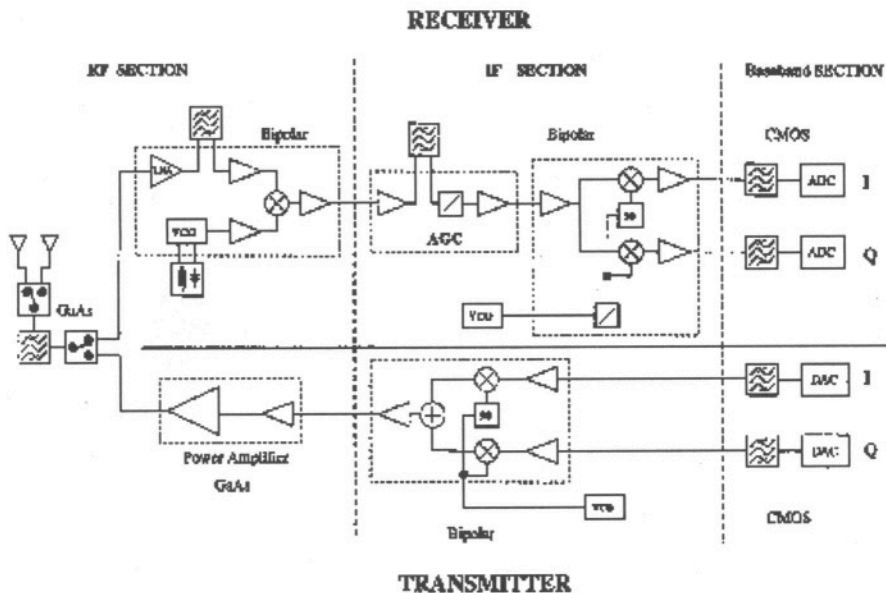
Figure 1.1. Example of a super-heterodyne transceiver implemented using multiple technologies.

On the other hand Figure 1.2 shows a very recent design of a complete transceiver for the new Bluetooth technology [10]. In contrast to traditional designs, CMOS has been used to implement all system blocks operating at 2.4GHz band. This fully integrated System-on-Chip (SoC) [10] includes the RF front-end, the digital baseband processor, the microprocessor, and the flash memory with the software stack. This achievement has been possible thanks to the relaxed performance requirements, and the low output power (OdBm-4dBm) of the Bluetooth standard, together with the use of deep sub-micron technologies.

The next challenge is to achieve higher levels of output power at such high frequencies as 2.4GHz, and ultimately at 5GHz. This work will focus on the transmit power amplifier as one of the most challenging building blocks for wireless transmitters as will be illustrated in the next sections.
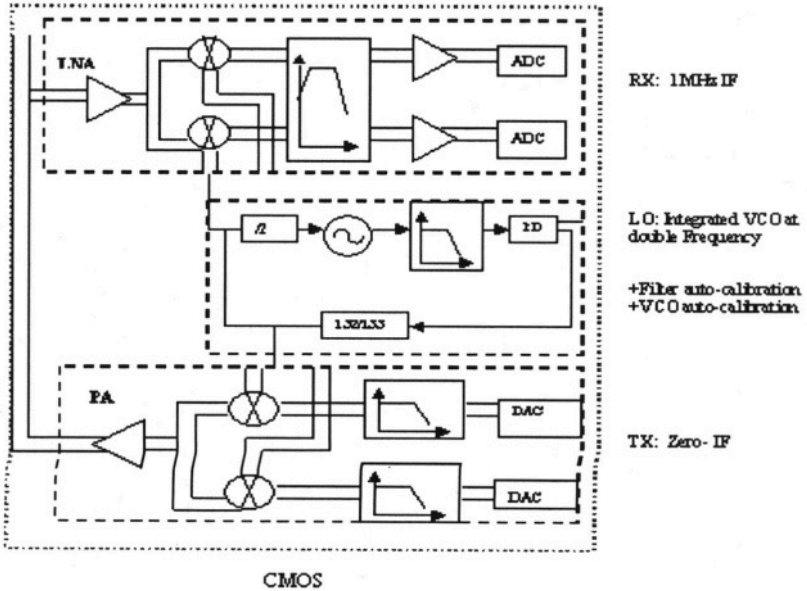
Figure 1.2. A fully integrated single chip for Bluetooth

Parameter	NADC	IS-95 CDMA	GSM	DECT
RF Tx. Freq. (MHz)	824-849	1860-1910	890-915	1880-1900
Multiple access	TDMA/FDM	CDMA/FDM	TDMA/FDM	TDMA/FDM
Duplexing	FDD	FDD	FDD	TDD
number of channels	832	20	124	10
Channel spacing	30kHz	1.25MHz	200kHz	1.728MHz
Modulation	π/4-DQPSK	QPSK/OQPSK	GMSK	GFSK
Peak to average ratio	3.5dB	10dB	1.5dB	0dB
Spectral regrowth	medium	high	low	low

Table 1.2. Example of some digital wireless standards.

3.   Wireless Transmission Protocols

Second generation (2G) mobile radio systems have shown great success in providing wireless service worldwide with the use of digital technology, in contrast to the analog first generation systems. Digital modulation techniques provide improved spectral efficiency, enhanced voice recognition, and quality as well as security. The most important 2G systems are global system for mobile communication (GSM), North American Digital cellular NADC (IS-54, IS-136) and personal digital cellular in Japan. However, 2G systems are limited to voice and low data rate services.

Within the next few years, third generation wireless standards will be implemented and used to provide broadband multimedia and high data rate applications with the aim of providing universal access and global roaming [11]. UMTS, CDMA 2000, W-CDMA, and EDGE are examples of 3G systems. Once they are launched, there will be an increasing demand for multi-standard terminals. Such terminals should allow access to different systems providing various services, including backward compatibility to existing standards. The coexistence of the second generation with third generation cellular systems would then require multi- mode, multi-band mobile terminals [12]. The main characteristics of some 2G and 3G systems are summarized in Table 1.2.

Short-range wireless communication standards are defined in Table 1.3. These standards are defined at 2.4GHz, and 5GHz unlicensed Industrial Scientific, and Medical (ISM) band. The IEEE 802.11 committee established the five different standards, which are Infrared, 2.4GHz Frequency hopping Spread Spectrum (FHSS), 2.4GHz Direct Sequence Spread Spectrum (DSSS), 2.4GHz High Rate DSSS(HR/DSSS), and 5GHz Orthogonal Frequency Division Multiplexing (OFDM). Only the OFDM standard uses the 5GHz frequency band in the 802.11 standards, while the others use the 2.4GHz ISM band.

European Telecommunication Standards Institute (ETSI) high-performance radio LAN (HIPERLAN) also uses the 5GHz band. The first draft of HIPERLAN standard adopted GMSK modulation scheme for high bit rate, and FSK for low bit rate. In order to harmonize the WLAN standards at 5GHz range and provide high speed access to a variety of networks, a new standard called HIPERLAN2 is developed. The multiple access method and modulation method of the HIPERLAN2 are the same as those of the 5GHz IEEE802.11 standard.

While the 802.11 and HIPERLAN standards are developed for the enterprise network, the Bluetooth and the HomeRF have their own special interests. The Bluetooth is for a short range Radio link between mobile PCs, mobile phones, and other portable devices. The HomeRF is for wireless voice, and data networking within the home at consumer price points. IEEE 802.11 FHSS, Bluetooth, and HomeRF standards use the same frequency hopping multiple access method, and same modulation scheme. However, they have different data rate, hopping rate, and Bluetooth has lower sensitivity than the others. Therefore, there is more room for higher noise figures in Bluetooth standard. The most important factor is that the Bluetooth standard focuses more on small size and low cost. HomeRF standard mainly focuses on home networking, which makes connections between the PC and internet throughout the home and yard.

Looking at these standards from the power amplifier design perspective, the modulation method along with the base band filtering utilized in digital systems may cause the modulated carrier to exhibit a non-unity peak to average power ratio, therefore requiring some degree of Linearity in the power amplifier. Table 1.2, and Table 1.3 shows the basic requirements of some standards.

Standard	Frequency Range	Multiple access	Modulation	Data Rate
IEEE802.11 DSSS	2.4GHz	DSSS	DBPSK DQPSK	1Mbps 2Mbps
IEEE802.11 FHSS	2.4GHz	FHSS	2GFSK 4GFSK	1Mbps 2Mbps
IEEE802.11 HR/DSSS	2.4GHz	DSSS	CCK	5.5Mbps 11Mbps
IEEE802.11a OFDM	5.250GHz 5.775GHz	OFDM	BPSK/QPSK 16 or 64 QAM	6,9,12,18 Mbps 24,36,48,54Mbps
HIPERLAN Type 1	5.250GHz	FDMA TDMA	FSK GMSK	1.47 Mbps 23.6 Mbps
HIPERLAN Type 2	5.250GHz 5.6GHz	OFDM	BPSK/QPSK 16 or 64 QAM	6,9,12,18 Mbps 27, 36, 54 Mbps
Bluetooth	2.4GHz	FHSS	GFSK	1 Mbps
HomeRF1.0 (1 MHz)	2.4GHz	FHSS	2GFSK 4GFSK	1 Mbps 2 Mbps
HomeRF2.0 (5 MHz)	2.4GHz	FHSS	2GFSK 4GFSK	5 Mbps 10 Mbps

Table 1.3.   Short-Range wireless standards.

Those techniques employing $\pi/4$-DQPSK and QPSK/OQPSK require highly linear power amplifier to limit spectral growth caused by their abrupt phase changes. Although those employing GMSK, FM, and GFSK do not require high linearity, some standards like GSM have power control mechanisms that necessitate efficiency enhancement techniques at lower power levels.

Another feature required of power amplifiers in digital wireless standards is the control of the output power. For example, in TDMA systems such as IS-54 and GSM, the PA is turned on and off periodically to save power. Also in IS-95, the output power must be variable in steps of 1 dB. In class 1 Bluetooth radio, the output power must be controlled from 4 dBm to 20dBm in steps of 2, 4, 6, or 8dB.

4.   CMOS PAs: Related Design Issues

The design of power amplifiers in CMOS technology is mainly affected by the following factors:

1 Low breakdown voltage of deep sub-micron technologies. This limits the maximum gate-drain voltage since the output voltage at the transistor's drain normally reaches 2 times the supply for classes B, and F, and around 3 times the supply for class E operation. Thus, transistors have to operate at a lower supply voltage, delivering lower power. Additionally CMOS tech-

nology has lower current drive; i.e. the gain provided by the single stage is very low. Either multiple stages would be used or new design techniques that would reduce the number of stages by decreasing the input drive requirements of the large transistors in the PA, are employed [13].

2 In contrast to semi-insulating substrates, a highly doped substrate is common in CMOS technology. This results in substrate interaction in a highly integrated CMOS IC. The leakage from an integrated power amplifier might affect the stability of, for example the VCO in a transceiver chain.

3 Conventional transistor models for CMOS devices have been found to be moderately accurate for RFICs, and need to be improved for analog operation at radio frequencies. Large signal CMOS RF models and substrate modeling are critical to the successful design and operation of integrated CMOS radio frequency power amplifiers, owing to the large currents and voltage changes that the output transistors experience [14]. As a result, traditional PA design relies heavily on data measured from single transistors.

4 Since the inherent output device impedance in the power amplifier case is very low, impedance matching becomes very difficult, requiring higher impedance transformation ratios. Additionally, the output matching elements require lower loss, and good thermal properties since there are usually significant RF currents flowing in these elements. If CMOS technology is used, the losses in the substrate will decrease the quality factor of the passive elements in the matching network. Usually the output- matching network is implemented off chip as the antenna itself is off chip.

5 The power amplifier delivers large output current in order to achieve the required power at the load. This current can be high enough that electromigration and parasitic in the circuit may cause performance degradation [14].

5.   CMOS PAs: Recent Progress

The research in the area of power amplifiers is divided into two main categories; the design and monolithic implementation of power amplifiers, and the integration of Linearization techniques. While the implementation of a complete transceiver was the focus of many publications ([4]- [6], [15]), the power amplifier was included in only two of the reported CMOS wireless transceivers [4], [15].

The first reported CMOS power amplifier targeted the 900MHz ISM band [16] delivering output power from 20μW to 20 mW using a 3V supply, and was implemented in 1μm technology. In an effort to provide higher integration level by having the de-feed inductors in the output stage on-chip, an extra fabrication step to remove the substrate beneath the inductor in order to improve the quality factor was employed. However, the measured drain efficiency of the power amplifier with the de-feed inductors of the output stage implemented on chip is 25%, compared to 40% with the inductors off-chip. No input matching to 50 Ohm was included since the power amplifier was integrated in the complete transceiver [4]. The output-matching network is implemented off-chip.

In [17] a 1W BiCMOS PA is reported. The design involves a negative resistance stage to boost the gain. The reported power added efficiency (PAE) is 30% using a 5V supply. External inductors are used as part of the inter-stage matching network, with the output-matching network completely off chip. Measurement results are reported for a chip-on-board die. While BiCMOS is capable of supporting other RF transceiver functions and is a strong candidate as a low cost technology for realizing a single chip radio, the reduction in performance of a BiCMOS PA compared to GaAs is evident in this paper.

Many publications advocated that CMOS would be limited only to low power-low performance applications. In [18] a 1W-2.5V supply monolithic power amplifier was reported. The PA targeted NADC standards (824MHz-849MHz). A gain of 25dB is achieved through 3 gain stages (operating in class A, AB, and C), with the output stage operating in class D (the transistor is used as a switch). This power amplifier has a measured drain efficiency of 62% and a PAE of 42%. It does not achieve a high degree of integration sine the output-matching network is implemented off chip. Bond wires are also used as a part of the inter-stage matching network.

The use of nonlinear power classes has been limited to low frequency operation until a recent publication explored the possibility of using class E power amplifiers at the 900MHz band. In [19] a fully integrated, yet GaAs MESFET implementation of a class E PA is reported. This nonlinear power amplifier outputs 250mW at 835MHz with power added efficiency (PAE) of 50% in a 2.5V system. A class F amplifier is used as a driver stage to generate the required square wave input driving signal. Bias voltages are applied externally but all matching networks are included on chip. This paper illustrated the advantages of operating in class E rather than in classes C, B, or F considering the fact that it has higher optimum load and higher PAE under low voltage operation.

Class E power amplifiers have gained wide interest after the previously mentioned publication due to their inherent high efficiency. In [13] a 1.9GHz 1W class E PA is implemented in 0.35μm CMOS technology using a 2V power

supply. The input driving requirement of the output stage is greatly reduced by employing the concept of mode-locking in which the amplifier acts as an oscillator whose output is forced to run at the input frequency. The output-matching network is off chip, and all inductors included are bond wire inductors. The measured PAE using chip on board packaging is 48%. The draw back of the mode-locking (positive feedback) technique is that the PA is prone to locking onto interfering signals picked up by the antenna from adjacent mobile users.

While the trend in most publications is to adopt nonlinear power classes (class D [18], Class E [9], [13], [20], and [21], and class F ([22] - [23]) to implement high efficiency and high power amplifiers, the continuous decrease in the voltage breakdown of transistors for deep sub-micron technologies makes the use of Class E amplifiers more difficult. Class F emerged as a possible solution in this case [13-14]. However, modern communication standards employ non-constant envelope modulation techniques that require linear power amplifiers, which means that either added linearization circuitry would be required or traditional linear power amplifier classes are used [14], [24].

A sample of the publications listed in Table 1.4 shows that even though the inductors and capacitors that may be realized in CMOS technology are not suitable for high performance RF circuits, CMOS transistors have still adequate gain till 2GHz to allow the design of low cost hybrid 1W amplifiers. The real merits of CMOS PAs lie in the potential for integration. While the feasibility of a stand-alone CMOS PA does not imply its compatibility in a larger system, the integration issues will rely on system, circuit and layout solutions rather than the design of the individual block.

In the Linearization area, few papers were published that dealt with the monolithic implementation [25]- [26], while most of the published work focused on system simulations and discrete implementation [27], [28].

In [26] a phase correcting feedback system to reduce the AM to PM distortion of class E PA used in NADC standard was presented. The system employed a limiting amplifier, a phase detector, and a phase shifter all-operating at 835 MHz. In order to reduce the phase error in the output caused by class E amplifier, the output and input phases of the amplifier are compared and an error phase signal is generated. The error signal is applied to a phase shifter at the input of the PA. The phase correcting feedback system reduces the phase distortion from 30 degrees to 4 degrees, and consumed 21.5mW while the PA delivers 500mW.

In [25] a fully monolithic CMOS implementation of the Envelope Elimination and restoration linearization system that improves the Linearity of an efficient PA is fabricated in $0.8\mu m$ CMOS process. A delta modulated switching power supply is employed to extend the modulation bandwidth to fit that of the NADC. The Linearization system improves the overall efficiency from 36% to 40% while increasing the maximum linear output power from 26.5dBm

Reference	Technology	Frequency(MHz)	Pout(dBm)	PAE(%)
[16]	1μm	900	13	30-40
[18]	0.8μm	824-849	30	42
[9]	0.25μm	900	29.5	41
[13]	0.35μm	1900	30	48
[14]	0.25μm	1950	29.2	27
[24]	0.35μm	1730	30.4	45
[22]	0.25μm	1400	24.7	43
[23]	0.2μm	900	31.7	43

Table 1.4.   Example of reported CMOS power amplifiers.

to 29.5dBm. Compared to the usual discrete implementation of EER systems used in high power base station, this design is amenable to integration in a low cost CMOS technology and makes linearization affordable to handsets.

In [20] a 20dBm power amplifier for Linear Amplification with Non-linear Components (LINC) transmitters is reported. An open loop linearized PA has been realized by combining two nonlinear class E amplifiers. The paper deals with a portion of the transmitter, not the whole system, and achieves 35% of power added efficiency under linear operation.

6.   Motivation

For applications requiring moderate to high power, the power amplifier contributes significantly to the total transceiver power consumption, making the PA efficiency critical to the overall system performance. Realizing high efficiency in CMOS is impeded by the technology's low breakdown voltage, low current drive and lossy substrate. In addition, maximum efficiency is normally achieved when the amplifier is operating at maximum power, which typically accounts for only a small portion of time in transceiver's normal operation.

In addition to efficiency and output power requirements, linearity in some modulation techniques is a major issue. Bandwidth-efficient modulation schemes require linear PAs to minimize spectral re-growth, and AM-PM conversion. This means that the modulated signal will leak into the neighboring channels. The leakage is characterized by the adjacent channel power ratio (ACPR), relating the power in the channel to the power leaked into the neighboring channel. All these effects will be discussed in chapter 2. Furthermore, amplifiers that simultaneously process many channels require linearity to avoid cross modulation [29].

There are two approaches to satisfy Linearity requirements for power amplifiers; either employ a linear operating class as an output stage, or start with

a nonlinear-high efficiency amplifier and apply linearization techniques, Linearization techniques are usually utilized in complex, expensive RF and microwave systems but they have not yet found their way in low cost portable terminals on a large scale. This is mainly due to the fact that such systems require various adjustments and become less effective as device characteristics change with temperature and output power [29].

In order to realize a complete transceiver on chip, issues related to system specifications, individual block performance, and the layout of the whole chip have to be dealt with. Although many publications have proved the capabilities of CMOS in delivering power levels around 1W, integrating such high power amplifier with the rest of the transceiver would introduce temperature and substrate noise effects that will affect the performance of the rest of the transceiver. Integration can be a cost effective solution without compromising performance in the case of short-range wireless applications. Even without regarding the integration issue, a stand-alone power amplifier, implemented in CMOS, and capable of covering multi-frequency bands can provide low-cost solution to less demanding wireless standards, e.g. Bluetooth.

The objective of this work is to target the design issues encountered in the design and implementation of power amplifiers in standard CMOS technology, for short-range wireless applications. The investigation of class E power amplifiers for the 900MHz band and its capabilities to operate as a multi-band amplifier will be explored. In order to push the limits of the used technology to achieve high frequency operation above 2GHz, which is the highest reported frequency; the use of linear power classes to implement a class 1 Bluetooth power amplifier is discussed. A novel circuit implementation to realize power control, and satisfy the Bluetooth standard is presented. A 0.18μm amplifier is also presented together with simulation results. Measurement results from two fabricated chips operating at the above mentioned frequencies are given.

7. Outline

This book focuses mainly on the design procedure and the testing issues of CMOS RF power amplifiers. It is divided into four main chapters. Chapter 2 discusses the basic concepts of power amplifiers; optimum load, load line theory, gain match versus power match. Performance parameters such as efficiency and linearity are presented. Different power amplifier classes are discussed and compared in terms of linearity and efficiency. Finally some common power amplifier linearization techniques are briefly investigated.

Chapter 3 presents the design and optimization techniques used to implement a 900MHz class E power amplifier. The theory behind class E operation is illustrated, the effects of some circuit components on the performance of the amplifier is demonstrated. The potential for applying the same concept

to multi-standard operation is also discussed. Finally testing procedure and measurement results are given.

Chapter 4 deals with extending the limits of the used technology to achieve 2.4GHz operation, and satisfy the Bluetooth standard. This is the first reported work on class 1 Bluetooth power amplifiers. Section 4.2 describes the details of the 2.4GHz power amplifier design, together with the implementation of the power control mechanism. Section 4.3 presents the simulation results, while experimental data is given in section 4.4. Chapter 5 presents an improved version of the power amplifier , using $0.18\mu m$ technology in which class 1, class2, and class 3 power amplifiers are implemented. Finally conclusions are drawn in chapter 6.

Chapter 2

POWER AMPLIFIER;
CONCEPTS AND CHALLENGES

1.   Introduction

Power Amplifiers are part of the transmitter front-end, and are used to amplify
the signal being transmitted so that it can be received and decoded within a
fixed geographical area The design of PAs, especially for linear, low-voltage
operation, is still a difficult task. In practice, PA design has involved a sub-
stantial amount of trial and error, that is why discrete and hybrid implemen-
tations have traditionally been utilized. The main performance parameters for
the power amplifier are the level of output power it can achieve, depending on
the targeted application, linearity, and efficiency. There are two basic defini-
tions for the efficiency of the PA. The drain efficiency is the ratio between the
RF output power to the dc consumed power, and the power added efficiency
(PAE) which is the ratio between the difference of the RF output power and
the RF input power to the dc consumed power. The PAE is a more practi-
cal measure as it accounts for the power gain of the amplifier. As the power
gain decreases, more stages will be required. Since each stage will consume
a certain amount of power, the overall power consumption will increase, thus
decreasing the overall efficiency.

While power efficiency is a performance issue, Linearity is imposed by the
utilized modulation technique, or the level of output power back-off during op-
eration.

Most power amplifiers employ a two-stage configurations, with matching
network placed at the input, between the two stages, and at the output. Since
the output stage typically exhibits a power gain of less than 10dB, a high-gain
driver is added so as to lower the minimum required input level. The choice
of the minimum input level depends on the driving capability of the preced-

ing stage, the modulator or the up-converter. The output stage is commonly designed as a common-source stage with a large inductor connected between the output node, and the supply. The large inductor [called a "radio-frequency choke"] acts as a current source that can sustain positive and negative voltages.

Designing an integrated CMOS power amplifier is different from the traditional microwave PA design using discrete components. In traditional microwave PA design, a data sheet is usually provided by the manufacturer, giving the large signal input and output impedances at certain dc operating point. Thus, the optimum load of the amplifier can be determined. A load-pull technique is usually employed to obtain a functional relationship between the output power and output matching [30].

In designing a power amplifier, the designer has to choose the number of stages, the operating class of each stage, determine the optimum load of the output stage, and decide whether to use differential or single-ended structure. These issues depend on the used technology, the kind of modulation (constant-envelope, or nonconstant-envelope technique), and whether the amplifier will be integrated with the whole transceiver or will be on a separate chip.

This chapter presents the main concepts and challenges of RF power amplifiers. The difference between the matching of the power amplifier and any other front-end device is illustrated in the next section through the introduction of power match. The effect of the transistor knee (pinch-off) voltage especially for low-voltage operation is given. An overview of different power amplifier classes of operation, together with linearization/efficiency enhancement techniques is described. Finally, the effect of the nonlinearity of the PA on the output signal, the main stability issues, and means for controlling the output power are presented.

2.   Conjugate Match and Load line Match

The concept of conjugate match is widely known as setting the value of the load impedance equals to the real part of the generator's impedance such that maximum output power is delivered to the load. However, this delivered power is limited by the maximum rating of the transistor acting as a current generator, together with the available supply voltage. By referring to Figure 2.1, it is evident that the device in this case would show limiting action at a current considerably lower than its physical maximum of I_{max}. This means that the transistor is not being used to its full capacity. To utilize the maximum current and voltage swing of the transistor, a load resistance of lower value than the real part of the generator's impedance value needs to be selected; this value is commonly referred to as the load-line match, R_{opt}, and in its simplest form is the ratio $R_{opt} = V_{max}/I_{max}$, assuming the generator's resistance is much higher
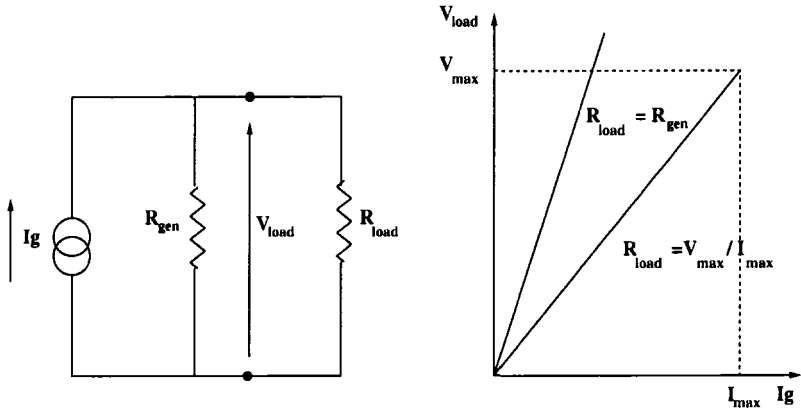
Figure 2.1. Conjugate match and load-line match.

than the optimum load resistance.

Thus the load-line match represents a real compromise that is necessary to extract the maximum power from RF transistor, and at the same time keep the RF voltage swing within the specified limits of the transistor and the available dc supply.
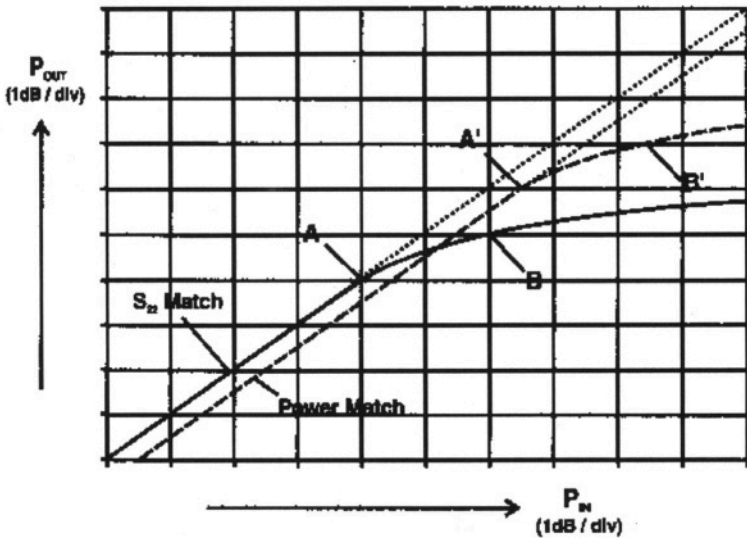
Figure 2.2. Compression characteristics for conjugate match (S22) (solid curve) and power match (dotted curve). 1 dB gain compression points (B, B') and maximum power points (A, A') show similar improvements under power-matched conditions.

Figure 2.2 illustrates the effect of the difference of gain match versus power (load-line) match on the output of a linear amplifier. The solid line shows the response of an amplifier that has been conjugately matched at much lower drive levels. The two pints A, and B, refer to the maximum linear power and the 1 dB compression power. In a typical situation, the conjugate match yields a 1 dB compression power about 2 dB lower than that which can be obtained by the correct power tuning, shown by the dotted line in Figure 2.2. This means the device would deliver 2 dB lower power than the device manufacturers specify. Since in power amplifier design, it is always required to extract the maximum possible power from the transistor, power-matched condition has to be taken more seriously, despite the fact that the gain at lower signal levels may be 1 dB or less than the conjugate-matched condition. Across a wide range of devices and technologies, the actual difference in output power, gained by power-matched condition, may vary over a range of 0.5dB to 3dB [30].

However, a load-line (power) matched rather than a conjugate (gain) match, might cause reflections and voltage standing wave ratio (VSWR) in a system to which it is connected. The reflected power is entirely a function of the degree of match between the antenna and the 50-Ohm system. The PA does present a mismatched reverse termination, which could be a problem is some situations. An Isolator or a balanced amplifier [31] is a simple and effective way of dealing with the problem.

3.   Effect of the Transistor Knee Voltage

As mentioned earlier, traditional power amplifier design starts by determining the optimum load using the load line approach as shown in Figure 2.3. The knee voltage (pinch-off voltage) divides the saturation and the linear region of the transistor and can be defined as, for example, V_{ds} at the 95% of I_{max} point. The optimum load resistance is

$R_{opt} = (v_{max} - V_{knee})/I_{max}$

While this is an effective approach for most power transistors, it is not suitable for sub-micron CMOS transistors. This is mainly due to the fact that V_{knee} is only about 10% to 15% of the supply voltage for typical power transistors, while it can be as high as 50% of the supply for deep sub-micron technologies as shown in Figure 2.3. Therefore, precluding the CMOS transistor from operating in the linear region does not result in optimum output power. In fact, a large portion of the RF cycle can be in the linear region. Therefore, both saturation and linear regions must be considered when determining the optimum load.This can be done using a general MOSFET equation valid in all regions of operation [23] or relying on harmonic balance simulations of circuits, with accurate transistor models, as will be discussed later in chapter 4.
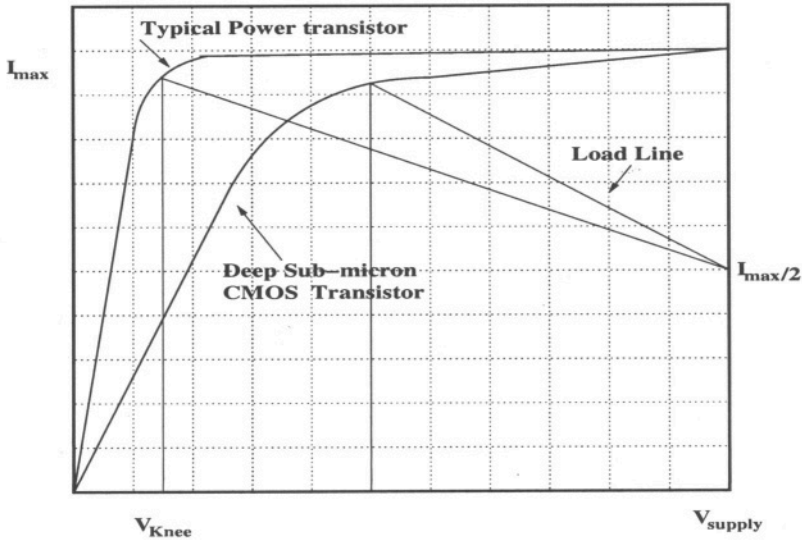
Figure 2.3. Effect of the knee voltage on the determination of the optimum load.

4. Classification of Power Amplifiers

Power amplifiers have been traditionally categorized under many classes: A, B, C, AB, D, E, F, etc [32]. Power amplifier classes can be categorized either as bias point dependent, such as classes A, B, AB, and C, or depending on the passive elements in the output matching network that shape the drain voltage and current, provided that the transistor in this case operates as a switch. In the next subsections, the details of each operating class are discussed.

4.1 Class A, B, AB, and C PAs

The primary distinction between these power amplifier classes is the fraction of the RF cycle for which the transistor conducts. For class A PAs, the transistor is conducting for the entire RF cycle, whereas for class B PAs it is ON for half the RF cycle, and for less than half the RF cycle for class C. Class A, AB, and B amplifiers may be used as linear PAs, whereas class C are more nonlinear in nature [33]. Figure 2.4 illustrates the schematic and current waveforms for the above-mentioned classes of operation. While the third-order intercept point (IP3), adjacent channel power ratio (ACPR), 1 dB compression point, and harmonics are various measures of Linearity of PAs, drain efficiency and power added efficiency (PAE) of the PA are used to indicate the current drawn from the supply. The PAE is defined as

$$PAE = \frac{(P_{rf,out} - P_{rf,in})}{P_{dc}} \qquad (2.1)$$
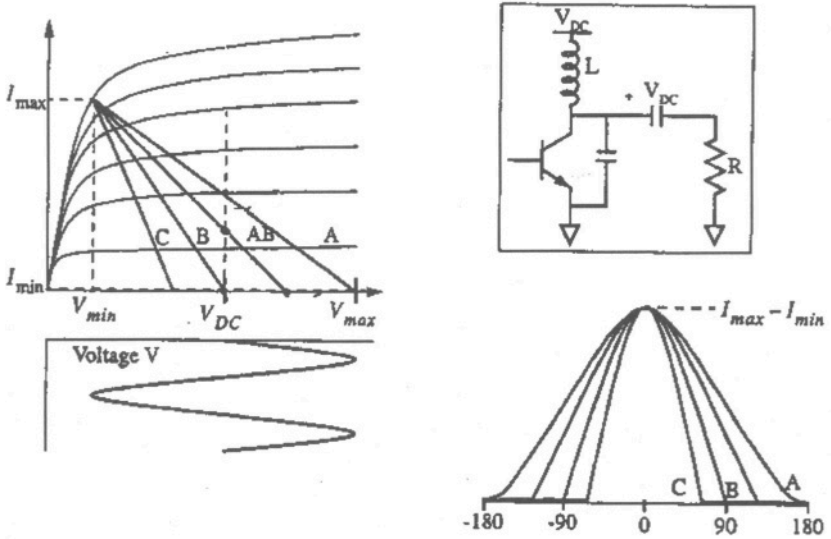
Figure 2.4.   Traditional illustration of the schematic and current waveforms of classes A, B, AB, and C.

where $P_{rf,out}$ is the RF output power, $P_{rf,in}$ is the RF input power, and P_{dc} is the total dc power drawn from the supply.

The efficiency and output power for a power amplifier operating in class A, AB, B, or C, are given by [30];

$$\eta = \frac{v_{dd} - v_{dsat}}{v_{dd}} \frac{\theta - \sin\theta}{4(\sin\frac{\theta}{2} - \frac{\theta}{2}\cos\frac{\theta}{2})} \qquad (2.2)$$

$$P_{out} = \frac{1}{2}(v_{dd} - v_{dsat})\frac{I_m}{2\pi}(\theta - \sin\theta) \qquad (2.3)$$

where V_{dd} is the supply voltage, θ is the conduction angle of the drain current, V_{dsat} is the pinch-off voltage (knee voltage), and I_m is the maximum drain current in the input transistor. Equations (2.2) and (2.3) are plotted in Figure 2.5(a). From this figure, it is evident that the increase in efficiency, obtained by reducing the conduction angle is achieved at the expense of the reduced output power from the power amplifier. In deep sub-micron technologies, the low output power of a reduced conduction angle is a major drawback. In order to achieve the required output power, the load resistance has to be lowered to impractical values considering the values of the parasitic resistances.

As the conduction angle of the drain current decreases, the harmonic content of the current signal increases. The magnitude of the nth harmonic of the output drain current is given by [30];
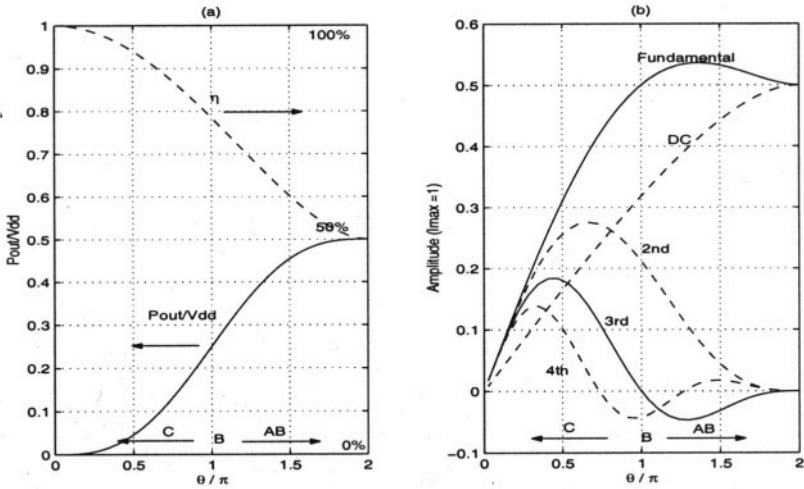
Figure 2.5. (a) RF power and efficiency as a function of the conduction angle, (b) Fourier analysis of the drain current.

$$I_n = \frac{1}{\pi} \int_{-\frac{\theta}{2}}^{\frac{\theta}{2}} \frac{I_m}{1 - \cos(\frac{\theta}{2})} \left(\cos \alpha - \cos(\frac{\theta}{2}) \right) \cos n\alpha d\alpha \qquad (2.4)$$

By examining Figure 2.5(b), it is clear that the dc component decreases monotonically as the conduction angle is reduced. In class B, the fundamental component is the same as in class A while the dc component is reduced by $\pi/2$. For conduction angles below π, corresponding to class C operation, the dc component continues to drop, but the fundamental component of the current signal also starts to drop below its class A level. This results in high efficiency, and lower power utilization factor (PUF). The odd harmonics can be seen to pass through zero at the class B point, For class AB mode, the third harmonic is not negligible. Still, class AB represents a compromise between linearity, PUF, and efficiency.

4.2 Class E

Figure 2.6 shows a conceptual picture of a class E power amplifier [34], [35]. In operation, the input signal v_{in} toggles the switch periodically with approximately 50% duty cycle. When the switch is ON, a linearly increasing current is built up through the inductor. At the moment the switch is turned off, this current is steered into the capacitor, causing the voltage across the switch V_s to rise. The tuned network is designed such that in steady state, V_s returns to zero with a zero slope, immediately before the switch is turned on. The band pass filter then selectively passes the fundamental component of V_s to the load, creating a sinusoidal output that is synchronized in phase and frequency with

the input. In practical applications, V_{in} may be phase or frequency modulated, in which case the information embedded in the modulation is also passed to the output with power amplification [13].

By comparing V_s, and I_s in Figure 2.6, it can be observed that the switch voltage and current are never simultaneously nonzero. Since the instantaneous power dissipation of the switch is the product of these two quantities, the switch is ideally lossless, and all the power from the dc supply is delivered to the radio frequency output. In addition, the capacitor is designed to be fully discharged before the switch is turned ON.

In high-speed operation, the switch transition time can become a significant fraction of a signal period. During these transitions, the switch voltage and current may be simultaneously nonzero, causing potential power loss in typical switching-mode amplifiers. For proper class E operation, this loss is alleviated at the turn on transistors by a zero switch current resulting from the simultaneously zero V_s, and dv_s/dt. On the other hand, turnoff transition loss is reduced by delaying the switch voltage rise until the switch is turned off. These properties have made class E-PAs attractive for high efficiency operations.

One of the features of class E amplifiers is the large peak voltage that the switch sustains in the off state, approximately $3.56V_{dd}\text{-}2.56V_{min}$; Where V_{min} is the minimum voltage across the transistor. Operating at class E requires either high transistor breakdown voltage, or operating at V_{DD} less than the specified value for a given technology. The equations describing the operation of class E will be discussed in Chapter 3.
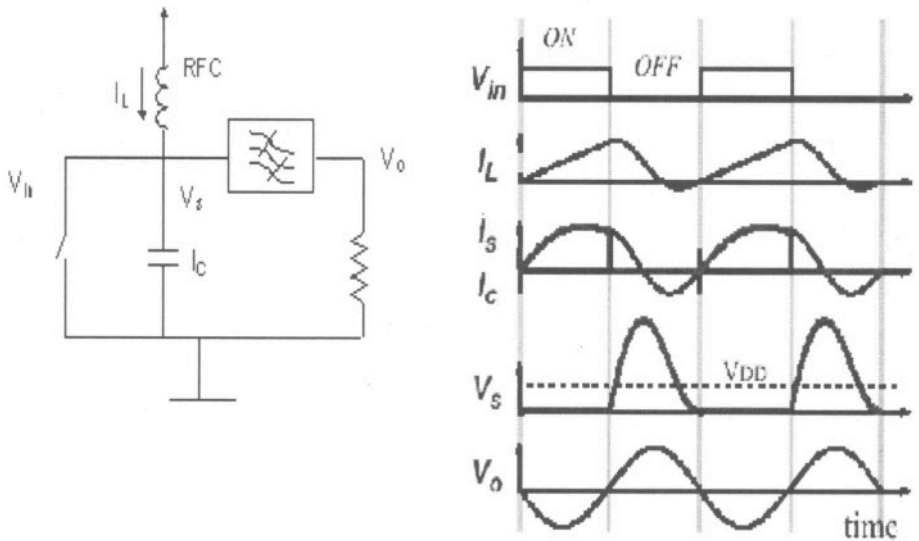
Figure 2.6.   A simplified class E power amplifier, and its steady state operation.

4.3 Class F

The basic idea behind class F and class D is to shape the output signal at the drain of the transistor such that it has more of a square shape than a sinusoidal shape. The load network provides a high termination impedance at the second or third harmonics, thus the voltage waveform across the switch exhibits sharper edges than a sinusoid, thereby lowering the power loss in the transistor.
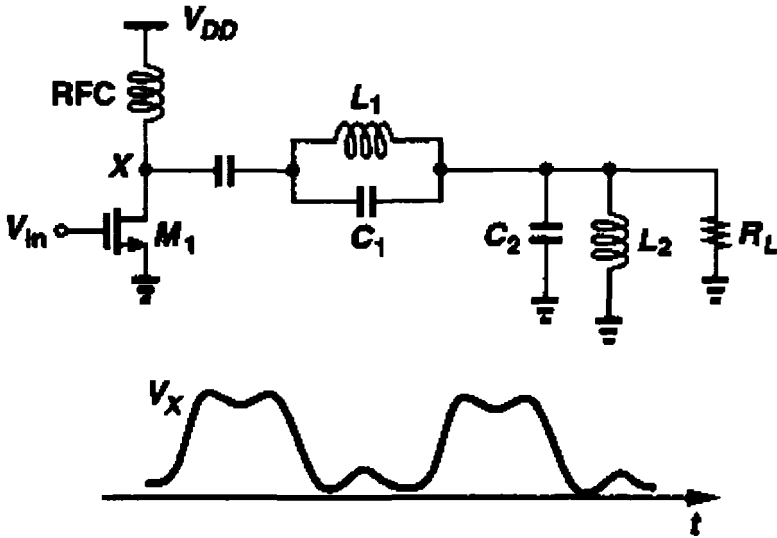
Figure 2.7. Schematic, and output waveform of a typical class F stage.

Figure 2.7 shows an example of the class F topology. The tank consisting of L_1 and C_1 resonates at either $2f_{in}$ or $3f_{in}$, where f_{in} is the input signal frequency, thus boosting the second or third harmonics at point X. Thus, the voltage across the switch approaches a rectangular waveform as the third harmonic becomes stronger. If the drain current of M_1 is assumed to be a half sinusoid (i.e., half-wave rectified sinusoid), then it contains no third harmonic. The product of the rectangular drain voltage and half wave rectified current represent the power losses in the transistor. Since this power losses are minimum due to the shaping of the two signals, the efficiency can be relatively high. The theoretical efficiency of a class F power amplifier can reach 88%.

To summarize the discussion on previous classes, what determines the class of operation of the power amplifier is its conduction angle, input signal over-drive, and the output load network. Figure 2.8 shows how the PA relate to the conduction angle and the input signal over-drive. It illustrates that a given PA can be in any of the classical operating modes depending on the above two
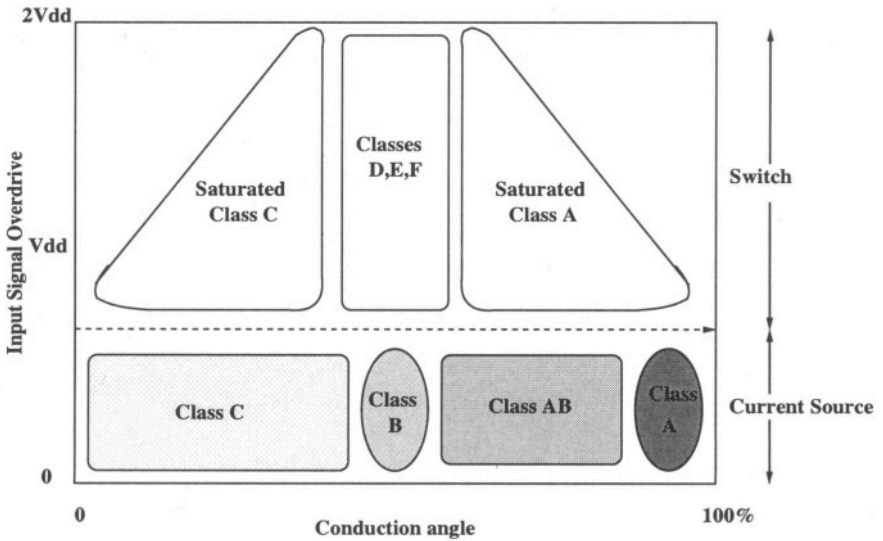
Figure 2.8.   Classical definition of power amplifier classes.

factors. For a small RF input signal V_{in}, the amplifier can operate in class A, AB, B, or C depending on the conduction angle (bias voltage relative to the transistor's threshold voltage). The PA efficiency can be improved by reducing its conduction angle by moving the design into class C operation, but at the expense of lower output power. An alternative approach to increasing efficiency without sacrificing output power is to increase the input over-drive such that the transistor acts as a switch. These are called saturated class A and C, class D, class E, or class F, depending on the conduction angle, and the shape of the load network.

5.   Power Amplifier Linearization

Linearization techniques are mostly utilized in base stations due to their complexity. For mobile phones, increasing the talk time and lowering the weight of the terminal rely on having an efficient amplifier that does not consume a lot of dc power. On the other hand, an efficient amplifier is normally nonlinear, while a spectrally efficient modulation technique produces non-constant envelope signals. If this non-constant envelope signal is applied to a nonlinear amplifier, the signal will suffer spectral growth, which will lead to adjacent channel interference. One of the solutions would be to use an efficient nonlin-

ear PA and apply a suitable linearization technique to restore Linearity.

The conventional techniques are feed forward, feedback, predistortion [30], [36], Envelope Elimination and restoration (EER) [37], Linearization using nonlinear components (LINC) [38], Bias adaptation, and Doherty amplifier [30]. The first three techniques are complex and need adjustments, or pre-measured data to achieve the required Linearization. They are usually utilized in base stations. The simplicity of the last three techniques makes them amenable to integration depending on the degree of linearity required and the channel bandwidth. Even for modulation techniques that do not require linearization, some techniques like EER, LINC, Doherty's amplifier, and Bias adaptation can be used for efficiency enhancement at lower output power levels.

5.1 Feed Forward
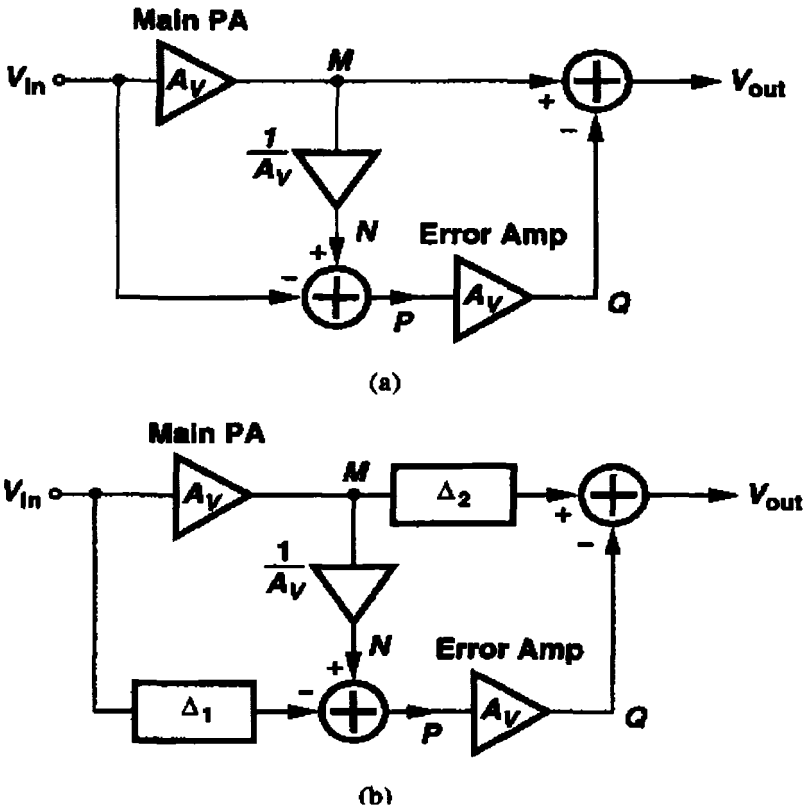
Figure 2.9. (a) Simple Feedforward topology, (b) Addition of delay elements.

A nonlinear power amplifier generates an output voltage waveform that can be viewed as the sum of a linear replica of the input signal and an error signal. A feed forward topology computes this error and, with proper scaling, substrates it from the output waveform. Shown in Figure 2.9 is a simple example where the output of the main PA V_M is scaled down by $1/A_v$, generating V_N. The input is subtracted from V_N, and the result is scaled by A_v and subtracted from V_M. If $V_M = A_V V_{in} + V_D$, where V_D represents the distortion content, then $V_N = V_{in} + V_D/A_V$, yielding $V_P = V_D/A_V$, and $V_Q = V_D$, and hence $V_{out} = A_V V_{in}$. In practice, the two amplifiers in the circuit exhibit substantial phase shift at high frequencies, mandating the use of delay lines such that Δ_1 compensates for the phase shift of the PA, and Δ_2 for the phase shift of the error amplifier.

The advantage of the feed forward topologies over feedback methods is inherent stability even with finite bandwidth and substantial phase shift in each building block. This is particularly important in RF and microwave circuits because inevitable poles and resonances at frequencies near the band of interest make it difficult to achieve stable feedback. Feed forward Linearization suffers from several disadvantages. First, the implementation of analog delay elements require passive devices such as micro-strip lines, with the power loss of Δ_2 being critical. Second, the output subtractor must be realized using a low loss component, e.g., a high frequency transformer [29].

5.2   Doherty Amplifier

The Doherty amplifier is primarily an efficiency enhancer rather than a linearization technique. It employs relatively linear amplifiers, which are known to have lower efficiency at lower power levels. It is used to preserve the peak efficiency at back-off points in modulation schemes that have high peak to power ratio. This means that a given level of Linearity, or spectral re-growth, at a given level of mean RF power can be achieved using the same device periphery but at substantially higher efficiency than in simple open-loop configuration.

The principal of the Doherty amplifier is to use one main power amplifier (PA) and one auxiliary PA. At maximum output power, both PAs contribute equally to the output. By decreasing the input drive level until typically half the maximum combined output power (-6dB from P_{max}), the auxiliary PA approximately shuts down. The way the Doherty amplifier achieves high efficiency is by keeping the main amplifier at maximum device output voltage when the auxiliary amplifier is operating. High device output voltage results in high power efficiency. The schematic of Doherty amplifier, and the corresponding output power waveforms are shown in Figure 2.10

The Doherty amplifier uses what is called the active load pull technique,
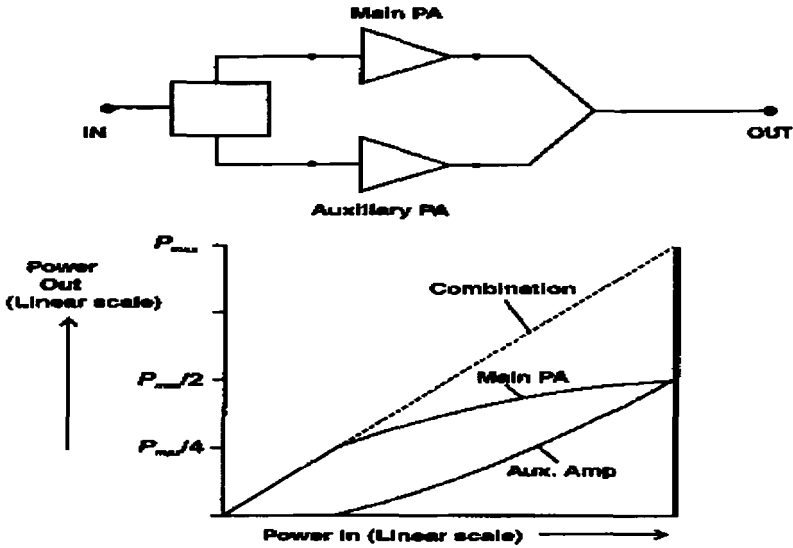
Figure 2.10. Basic Doherty amplifier configuration

which means that the whole operation is equivalent to the resistance or reactance of the RF load being modified by applying current from a second phase coherent source, which is the auxiliary amplifier. By doing so, the impedance seen by the different amplifiers is a function of the other elements and the common load. The load-pulling effect together with a quarter-wave transformer, causes the effective load resistance to decrease with increasing drive level. This impedance transformation is necessary to keep the main amplifier device voltage at its maximum in the high power region. The power efficiency of the main amplifier alone is ideally constant in the high power region. The auxiliary amplifier has its highest power efficiency at maximum output power. Therefore the complete Doherty amplifier has a high efficiency in the whole power range and especially at the medium output power level compared to classical power amplifier design.

5.3 Envelope Elimination and restoration

Figure 2.11 shows the block diagram of the EER Linearization scheme as proposed by Khan [37]. As the name "envelope elimination and restoration" implies, the envelope of the RF input is first eliminated by a limiter to generate a constant amplitude signal. At the same time, the magnitude of the input information is extracted by an envelope detector. The magnitude and phase information are amplified separately, and then recombined to restore the desired RF output. A way to combine the magnitude and phase components is to use
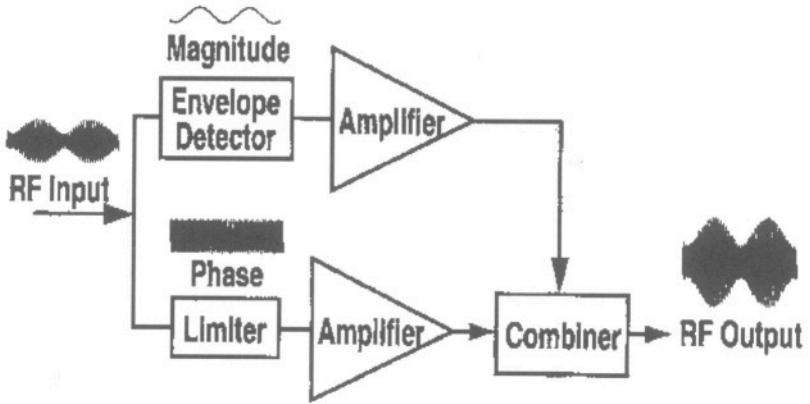
Figure 2.11. Conceptual diagram of Envelope Elimination and Restoration technique

an efficient switched-mode RF power amplifier. In a switched mode PA, the output power is directly proportional to the square of the supply voltage. Thus, the envelope of the RF output of the switched mode RF PA is directly proportional to its supply voltage. Assuming that the output stage of the switching PA is formed of a single transistor, with its drain connected to the supply via an RF choke coil, the envelope and phase components can therefore be recombined if the phase signal (RF) is applied to the gate of the transistor while the magnitude signal (Low frequency) directly modulates the supply. The key advantage of this EER approach is that the PA always operates as an efficient switched-mode amplifier. Thus, high efficiency can be obtained without compromising the Linearity.

Practically, the process of amplifying the detected envelope signal up to the necessary voltage and current capacity to modulate the PA device will consume a significant amount of power. However, modem techniques focusing on high efficiency pulse width modulation developed for high fidelity audio amplification can be used for this application, and maintain relatively high efficiency [25]. One problem would be the bandwidth of the modulator, which would appear to be limited to few megahertz. This will limit using this technique to certain modulation standards.

5.4   Linear Amplification Using Nonlinear Components

This technique is also called the out-phasing amplifier. It adopts the same concept as EER, the use of nonlinear power amplifiers, but avoiding non-constant envelope input signals. The idea is that a band pass signal, $v_{in}(t) = a(t)\cos[\omega_c t + \phi(t)]$ can be expressed as the sum of two constant amplitude phase modulated signals, $v_1(t) = 0.5V_o\sin[\omega_t t + \phi(t) + \theta(t)]$ and $v_2(t) = -0.5V_o\sin[\omega_t t + $

$\phi(t) - \theta(t)]$ where $\theta = \sin^{-1} a(t)/V_o$.
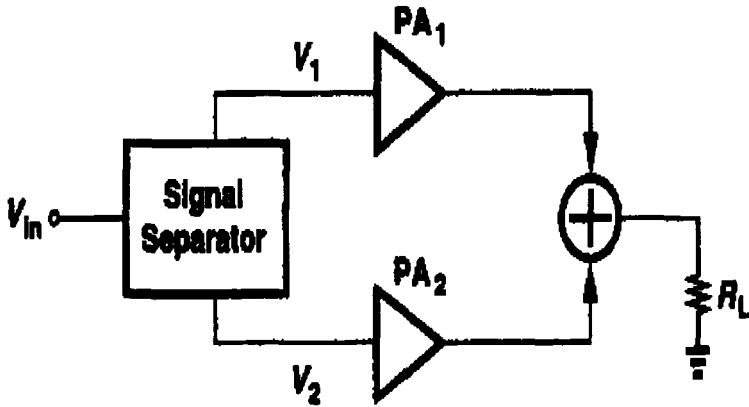
Figure 2.12. Linear Amplification using Nonlinear Stages

Thus, if $v_1(t)$ and $v_2(t)$ are generated from $v_{in}(t)$, amplified by means of nonlinear stages, and subsequently added, the output contains the same envelope and phase information as $v_{in}(t)$. Realization of $v_1(t)$ and $v_2(t)$ from $v_{in}(t)$ requires substantial complexity, primarily because their phase must be modulated by $\theta(t)$, which itself is a nonlinear function of a(t). A block achieving the separation of varying envelope signal into two constant envelope signals is referred to as Signal Component Separator (SCS). Recently reported work on integrated 200MHz SCS has demonstrated a sideband suppression of 45dBc using two open loop amplitude compensated saturated wideband BJT amplifiers [39]. In practice, LINC transmitters must deal with two crucial issues. First, gain and phase mismatch between the two signal paths as shown in Figure 2.12 results in residual distortion. Second, the interaction between the nonlinear amplifiers through the combiner network can limit the overall linearity achieved in this open loop configuration as the two nonlinear amplifiers when connected together might cause the two phase modulated signals to corrupt each other's phase. Nevertheless, This kind of transmitters has achieved wide interest lately, and reported results have shown improved linearity at 1GHz [20].
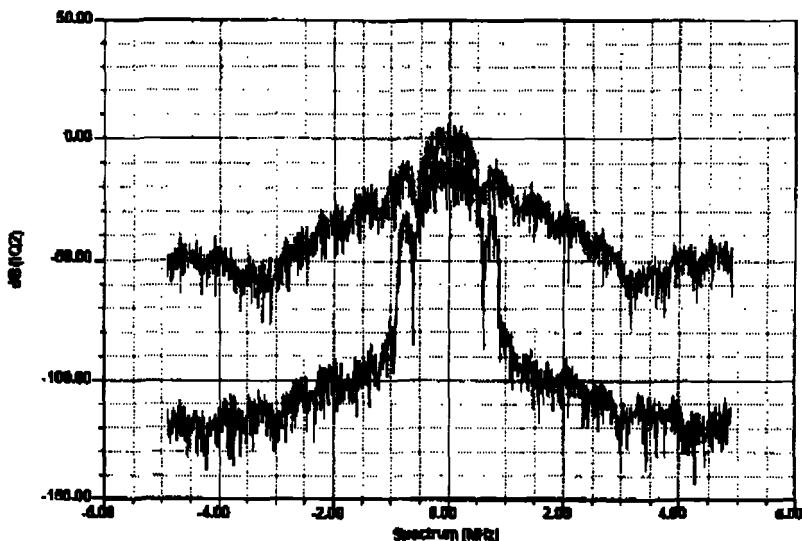
Figure 2.13.   Spectral regrowth due to amplifier nonlinearity

6.   Spectral Regrowth

Abrupt changes in a digitally modulated waveform, for example, QPSK, result in envelope variations if a filter limits the bandwidth of the signal before being applied to the PA. If the power amplifier exhibits significant nonlinearity, then the shape of the input signal to be transmitted is not preserved, and the spectrum is not limited to the desired bandwidth. This effect is called "spectral regrowth", and can be quantified by the relative adjacent channel power. Figure 2.13 illustrates this effect in the case of a QPSK signal applied to a weakly nonlinear power amplifier.

In order to limit spectral regrowth, linear power amplifiers are usually utilized. However, linear PAs are usually less efficient than nonlinear ones, as they consume a considerable amount of power with respect to the rest of the portable phone. Nonlinear PAs, on the other hand, exhibit efficiencies as high as 60%. Thus, it is desirable to employ modulation schemes that do not experience spectral regrowth when processed by nonlinear amplifiers.

7.   Power Amplifier Stability Issues

RF PA oscillation problems can be broadly categorized into two kinds; Bias oscillations, and RF oscillations. Bias oscillations occur at low frequencies, in the megahertz to VHF range, and are caused by inappropriate and uninten-

tional terminations at those frequencies by the bias insertion circuitry, such as the addition of a large-value decoupling capacitors. The oscillations have little to do with the details of the RF matching circuitry, where the RF blocking and decoupling capacitors become open circuit terminations at lower frequencies. RF oscillations, on the other hand, typically occur either in band or commonly out of band but still quite close to the desired bandwidth from the low frequency side. These latter kinds of oscillations are too common in single ended multi-stage designs, and their elimination will require modifications to the RF matching network topology and element values. Both kinds of instability can be analyzed effectively using the k-factor analysis [31]. Although k-factor analysis assumes a linear two-port device, it is usually a satisfactory assumption to assume that RF oscillations in power amplifiers will more likely occur when the amplifier is backed off into its linear region, where the k-analysis is valid. In the case of deep class AB or B operation, it is necessary to increase the quiescent current to perform the stability analysis with a representative amount of gain. A simple way to test stability of the PA, is to run the entire circuit on a linear simulator, sweeping the frequency all the way down to dc.

Higher frequency instability will show up in a k-factor analysis of individual stages. Any single-ended design must show a k-factor greater than unity over the widest frequency sweep, extending from the low-frequency bias circuit range all the way up to the frequency at which the gain rolls off to lower than unity. Designing or modifying a circuit to obtain such a response for the k factor typically will involve some sacrifices in the in-band RF performance through the use of resistive elements, which will affect the efficiency of the PA.

8. Power Amplifier Controllability

Implementing power amplifiers in CMOS technology is considered a major step towards the realization of a complete transceiver on-chip. Modern transceivers require means for adjusting the transmitted power over a finite range to further reduce power consumption and improve channel capacity. A low performance, short-range wireless standard such as the Bluetooth radio requires a high level of integration, and low cost that can only be achieved using CMOS technology, together with means of controlling the output power up to 20dBm. In addition, power amplifiers are typically backed-off relative to their peak power and power added efficiency points in order to meet the Linearity requirement of the system. The degree of back-off varies depending on the modulation scheme employed-0dB for Gaussian-filtered minimum shift keying (GMSK) (GSM and DECT), 7dB for π/4DQPSK (IS-54 and PHS), l0dB for QPSK (IS-95) and 12 dB for 16QAM are typical. Thus, adding efficient techniques for adjusting the output power level is considered a challenging issue to integrated power amplifiers.

Linear power amplifiers can have their power adjusted by the variation of biasing or dynamic variation of the load seen by the output stage (Doherty amplifier [30]). The output power can also be controlled through the variation in the input signal amplitude; this can be realized by having a variable gain amplifier as a preceding stage. However a large dynamic range of output power requires a linear wide dynamic range variable gain amplifier which is usually power consuming and hard to achieve. Also this configuration suffers from a large reduction in efficiency at lower power transmission because the standing bias current at the output stage does not scale with the output power. This technique requires a very linear power amplifier for any kind of signal shaping at the input.

In non-linear power amplifiers, the input to the amplifier provides only timing information. Thus, the output power cannot be controlled through the variation in input signal amplitude as is done in linear or weakly nonlinear amplifiers. Instead, output power control can be realized effectively through a variable supply, implemented for example by a dc-dc converter. The losses in the DC- DC converter might cause the efficiency to drop to reach that of a linear power amplifier's case. A new methodology based on switching a combination of power amplifiers in parallel is presented in [22] and represents an extension to the idea of Doherty amplifier to non-linear power amplifiers.

9.   Summary

This chapter has presented the main concepts of power amplifier design. Power matching, and the effect of the transistors' knee voltage at low-voltage operation has been discussed. The chapter has also covered different power amplifier classes of operation, together with means for linearization and efficiency enhancement. Finally, the issues of spectral-growth, stability, and power control have been addressed.

Chapter 3

A 900MHZ CLASS E CMOS PA

1.   Introduction

In general, the main performance parameters for power amplifiers used in mobile transceivers are power efficiency, power gain, output power, linearity, and ability to work at lower power supply voltages. However, many wireless standards that are located in the 900MHz band or close to it, such as GSM, NADC (835MHz), and other standards that use the ISM band, do not require high degree of linearity. A class E power amplifier suits the first and third applications, while some form of added linearization would be required in the second application (NADC).

   The choice of the operating class of the power amplifier is not only dependent on the wireless standard utilized, but also on the characteristics of the used technology. A 0.35μm, three metal layers, double poly CMOS process is used in this design example. This process is also characterized by having a relatively high breakdown voltage (8V) [40].

   The choice of Class E depends on several factors. First, switching-mode power amplifiers such as class D, E, and F have generally higher efficiency than linear power amplifiers because an ideal switch does not have an overlapping period of nonzero switch voltage and current. Practically, however, the transition between the ON and OFF state of a switch takes finite time, during which substantial amount of power can be dissipated as shown in Figure 3.1. This kind of switching is called hard switching, and is one of the main reasons for efficiency reduction in switching-mode power amplifiers such as class D, and F. On the other hand, the load network in class E power amplifiers is designed such that the switch voltage returns to zero with zero slope right before the switch turns on, ensuring no overlap of nonzero switch voltage and current as mentioned earlier in chapter 2 (Refer to Figure 3.2). This soft switching
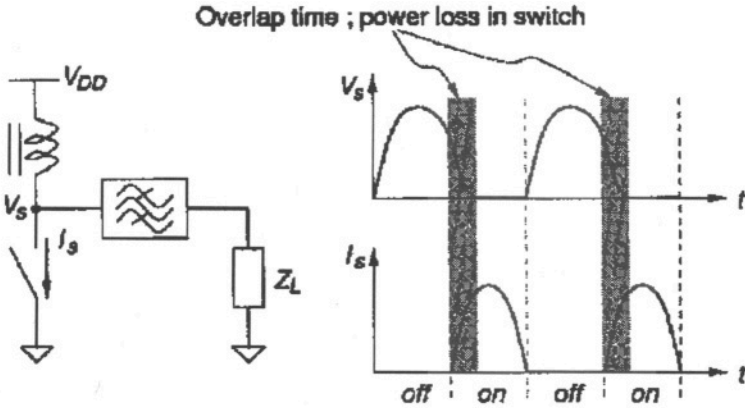
Figure 3.1. Waveforms of a switching-mode power amplifier with hard switching.

of class E Power Amplifier minimizes the power loss in the switch and thus highly efficient amplification is possible for constant envelope modulated signals [9]. Second, as the supply voltage decreases, the value of the optimum load required to achieve a specific value for output power also decreases. This decrease in the load resistance will increase the matching network transformation ratio from 50 Ohm, causing more losses in the matching network. This effect is less pronounced in class E than classes B [41], C, and F [9], [19], making it more suitable for low voltage operation.

2.   Class E PA Circuit Design

Figure 3.3 shows the basic schematic of a class E stage, with the associated values of circuit components. The formulas describing the dependence of various elements on output power (P_{out}), supply voltage (V_{dd}), loaded quality factor (Q_L), and operating frequency ($\omega = 2\pi f$) is derived in [42], based on the following assumptions:
1. The inductance of the DC choke is very high.
2. The Quality factor of the series inductor (L) is high.
3. The losses in the switch are negligible.

By utilizing the class E conditions, $v_D(\pi)=0$ and $i_D(\pi)=0$, and the 100% power efficiency assumption, the drain voltage waveform of the amplifier becomes;

$$v_D = \frac{V_{DD}}{\pi}(\theta + \frac{\pi}{2}\cos(\theta) + \sin(\theta) - \frac{\pi}{2}) \tag{3.1}$$

Where $\theta=\omega t$. The drain voltage waveform is Fourier transformed in order to solve the fundamental frequency phase angle ϕ_1 and amplitude α_1 of the signal at node A.
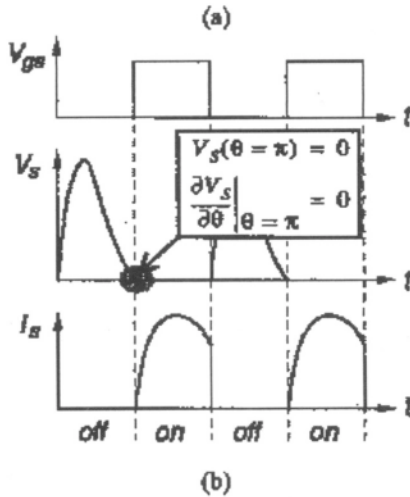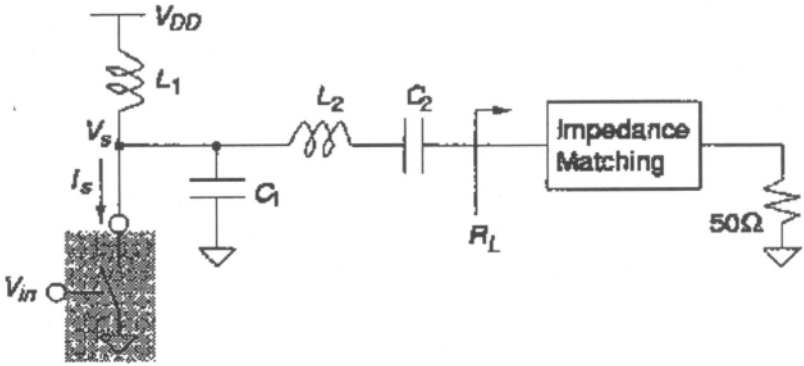
Figure 3.2. (a) Typical schematic of a class E power amplifier, (b) Its voltage and current waveforms showing the soft switching characteristics.

$$\tan \phi_1 = -\frac{\int_0^1 v_D \cos \theta d\theta}{\int_0^1 v_D \sin \theta d\theta} \tag{3.2}$$

$$\alpha_1 = \frac{1}{\pi}\sqrt{(\int_0^\pi v_D \sin \theta d\theta)^2 + (\int_0^\pi v_D \cos \theta d\theta)^2} \tag{3.3}$$

To achieve the correct phase at the load, an excess reactance X is added in series with the load resistance. The values for R and X are calculated using the solved α_1 and ϕ_1

$$R = \frac{v_{out}^2}{2P_{out}} = \frac{\alpha_1^2}{2P_{out}}\left(1 + (\frac{\pi \tan \phi_1 + 2}{\pi - 2\tan \phi_1})^2\right)^{-1} \tag{3.4}$$

P_{out}	$\dfrac{\pi^2+4}{8} I_{DC}^2\, R$
R	$\dfrac{8\,V_{DD}^2}{P_{out}\,(\pi^2+4)}$
X/ω	$\dfrac{\pi\,V_{DD}^2\,(\pi^2-4)}{2\omega P_{out}\,(\pi^2+4)}$
L	$\dfrac{8\,V_{DD}^2 Q_L}{\omega\,P_{out}\,(\pi^2+4)}$
C	$\dfrac{P_{out}\,(\pi^2+4)}{\omega\,8\,V_{DD}^2 Q_L}$
Cd	$\dfrac{P_{out}}{\pi\omega\,V_{DD}^2}$

Figure 3.3.   Single-ended class E resonant power amplifier.

$$X = R\tan\left(\phi_1 - \tan^{-1}\left(\frac{-2}{\pi}\right)\right) \tag{3.5}$$

The maximum drain voltage occurs when $\theta = 2\tan^{-1}(2/\pi)$

$$v_{D,max} = 2\pi V_{DD}\tan^{-1}\left(\frac{2}{\pi}\right) = 3.562 V_{DD} \tag{3.6}$$

This is one of the crucial issues of class E PAs, especially in deep sub-micron technologies where the breakdown voltage of MOS devices is low. However, with the used technology of 8V maximum stress, the supply voltage can be reduced to a maximum voltage of 2.24V to reduce the stress on the transistors without compromising efficiency.
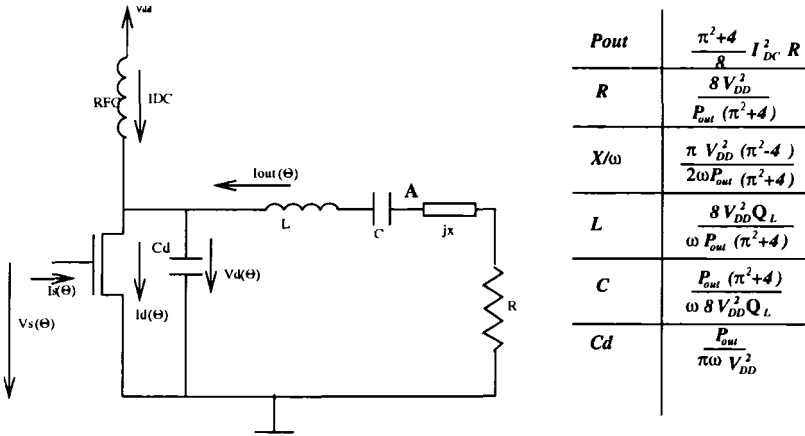
Figure 3.4 shows the schematic of the common source switched PA. The de-feed inductor (L_{RFC}) can either be an RF choke or a finite inductance. One method to provide the relief on the supply voltage and the load resistance is to use a finite inductance instead of an RF choke [43]. The values of passive elements in this case will be modified from that shown in Figure 3.3, and can be determined by solving a set of nonlinear equations reported in [43], [44].

2.1   Driver Stage Design

A main issue in class E power amplifier design is the generation of the input signal by a driver stage to turn the transistor on and off. Ideally a square wave-form should be applied to the output stage to avoid long transition times from one switching state to another. This square wave generation can be either done using an inverter, a class F amplifier, or a pseudo class E pre-driver stage.
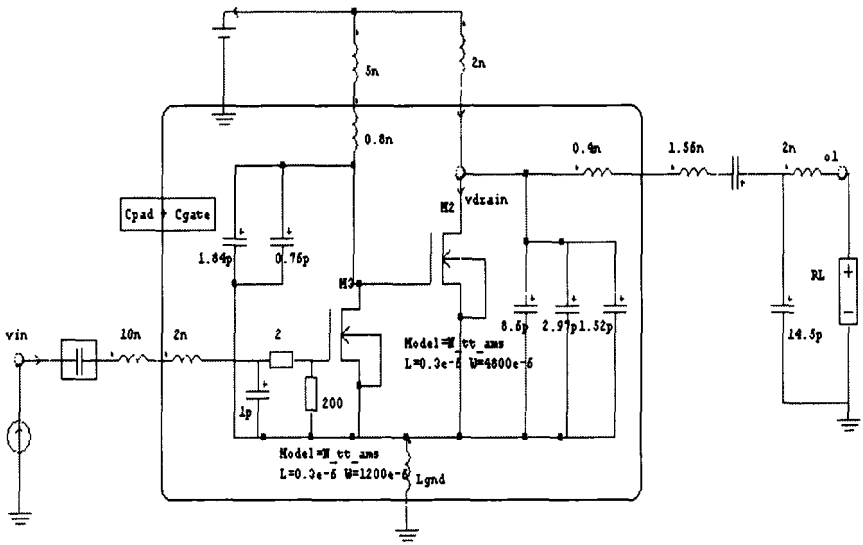
Figure 3.4. Schematic of the 900MHz Class E Power Amplifier.

Class F:

Class F is the ideal theoretical solution. However, the performance of class F amplifiers relies heavily on the realization of the harmonic traps as described in chapter 2. The load network of class F circuit has two tuned LC circuits in series. If an integrated solution is required, the inductors connected to the drain of the driver stage have to be implemented on chip, which is not possible in this case, since usually large current flows in these inductors that the width of the spiral inductor has to be wide enough or a parallel inductor scheme would be used. Implementing the load network of a class F driver off chip will increase the footprint of the circuit and increase the number of external components.

Inverter Stage:

Using an inverter stage will increase the current consumption, especially at high frequencies. The inverter's performance depends on the characteristics, and models available for the PMOS devices in the used technology. However, using inverters prevent the possibility of negative swing at the gate of the output stage.

Pseudo-Class E:

The driver stage in this work is a pseudo class E, or simply a band pass stage with a transistor of width = 1.2mm and 120 fingers. The inductor connected to the drain of the transistor tunes out the capacitance of the gate of the output stage. The size of the transistor in the output stage is based on several factors. Since the drain efficiency is given by;

$$DE = \frac{1}{1 + 1.4\frac{r_{on}}{R_L}} \qquad (3.7)$$

Where DE is the drain efficiency of the PA, r_{on} is the resistive loss in the switch while conducting, and R_L is the optimum load resistance required to achieve class E operation.

Device Sizing

A small transistor would increase the resistive loss of the switch, thus, decreasing power added efficiency. While a large transistor would negligibly improve efficiency, and at the same time limit the operating frequency of the amplifier due to the increase in the associated parasitic capacitance. Determining the total width and the number of fingers is also dependent on the transistor layout and the current handling capability of different metal layers. An initial estimate for the transistor width is derived from a physically based analytic model of a single FET class E power amplifier reported in [45]. This model is implemented in MATLAB with parameters from the used technology and the required operating conditions. It provides the effect of changing the width of the transistor on the output power and power added efficiency. As mentioned earlier, increasing the width beyond certain limits will not increase the output power, in fact it will need more driving power, and therefore less power added efficiency. Figure 3.5 illustrates this effect. It can be seen that approximately the maximum power added efficiency reaches a maximum at a number of fingers equal 400 using a unit transistor width of $12\mu m$, thus the total width of the transistor in the output stage is 4.8mm.

2.2   Simulated Performance

The circuit is simulated using SPECTRE RF and APLAC simulators and 0.35 μm technology parameters. The simulated voltage and current waveforms are shown in Figure 3.6. In Figure 3.6(a), the voltage at the drain of the transistor, together with the drain current are shown. It is evident that when the switch is ON, the voltage on the drain is very low, accounting only for the drop on the transistor's on-resistance. The drain current also reaches zero when the drain voltage is at its peak. Figure 3.6(b) shows the current in the inductor connected between the supply and the drain of the transistor.
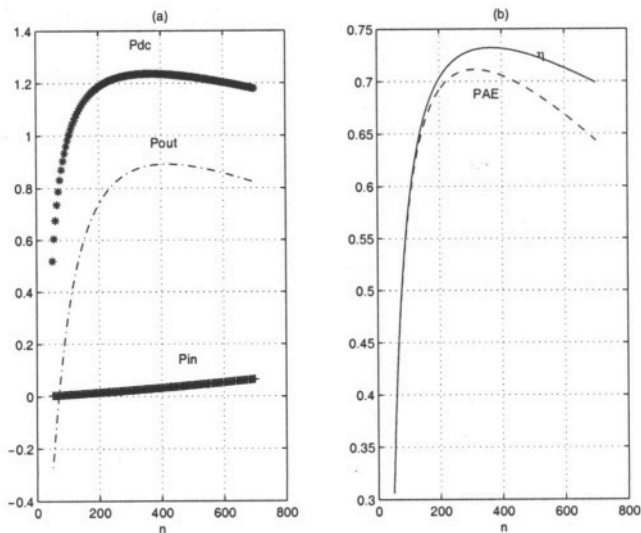
Figure 3.5. (a) DC Power (PDC), input power (Pin), and output power (Pout), (b) Efficiency and power added efficiency (PAE) versus the number of fingers of the transistor in the output stage.

As mentioned earlier, a finite value for L_{RFC} (dc feed inductor connected to the drain of the output transistor) will give an extra degree of freedom when determining the values for the optimum load, and drain capacitance required to achieve optimum operation. In fact, even with the same component values as the theoretical results given in Figure 3.3 , lowering the dc feed inductance increases efficiency as shown in Figure 3.7. It is worth mentioning that there is a limit on how low the inductor can go depending on the minimum realizable bond wire and board trace inductances.

Stability

Stability is one of the most important issues in amplifier design. A stable amplifier is free of unwanted oscillations. Instability occurs when some of the output energy is fed back to the input port in the proper phase so as to make negative resistance appear at the output or input of the amplifier. Coupling from output to input occurs through capacitances within the active device and through external elements. Because the reactance of the feedback capacitance decreases with increasing frequency, the likelihood of unwanted oscillations is higher in RF amplifiers.

(a)

(b)
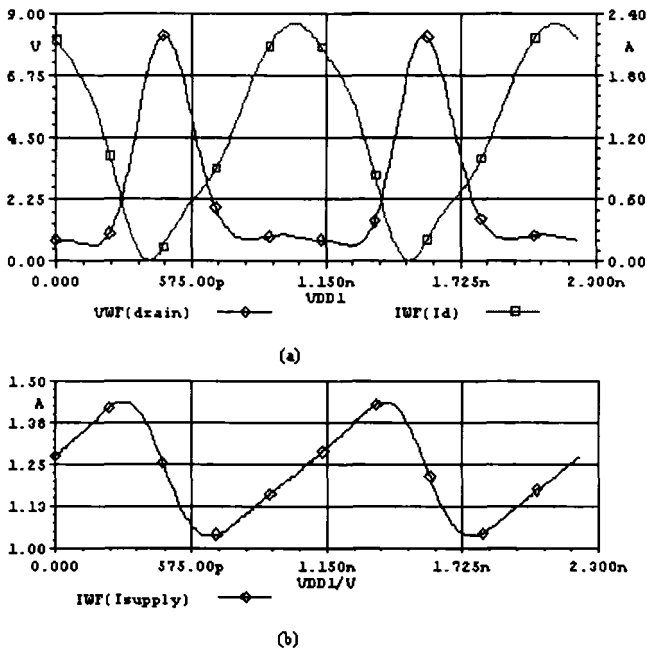
Figure 3.6. Simulated waveforms of the class-E power amplifier, (a) The drain voltage, and the drain current of the output stage transistor, (b) the supply current.
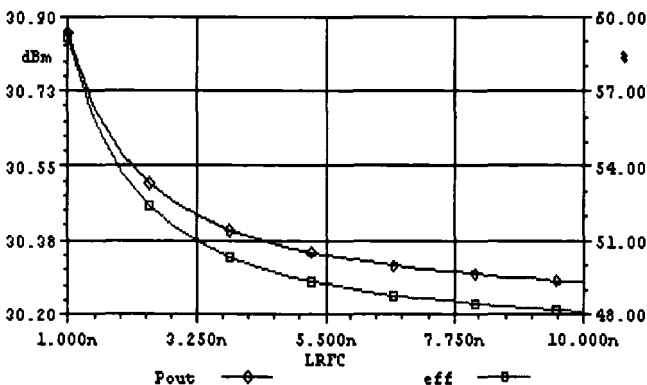
Figure 3.7. The effect of having a finite dc-feed inductance on the output power and efficiency of a class E Amplifier.

The usual k-factor stability definition does not actually have a meaning in the case of Class E amplifiers since the transistors in this case are acting as switches, while the definition of the k-factor is based on small signal analysis. The practical way to test stability in this case is to perform transient analysis using a step input located at various nodes and check that the output settles

down to a fixed level within a short period of time.
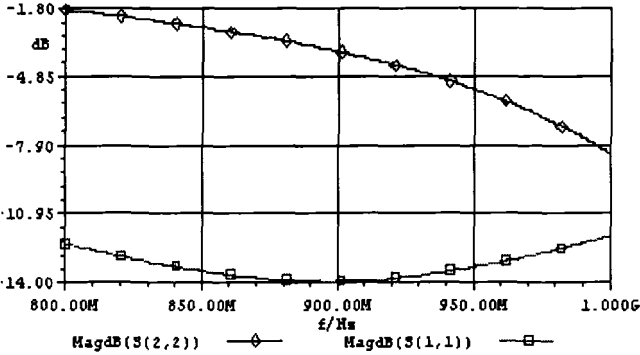
Figure 3.8. S_{11}, and S_{22} of the power amplifier.

Input Matching

In order to perform input matching, large signal S-parameter simulations are required. Since the available simulators do not support this kind of simulation, Harmonic Balance simulations are performed, and used to calculate the input impedance using the ratio of the input voltage and input current. The magnitude of the input reflection ratio is calculated using the input impedance of the amplifier, and used to derive the value of S_{11}. The same concept is utilized to find S_{22}. The results of S-parameter simulations are shown in Figure 3.8.

Efficiency Dependence on the Supply Voltage

The supply voltage of a class E PA is the only reference in the switching circuit, every node voltage is proportional to V_{DD}, and every power term is proportional to the square of V_{DD}. This means that the output power is controllable through the supply voltage, which leads to the potential of maintaining a constant efficiency over a wide range of output power variations as illustrated in Figure 3.9. This is one of the main benefits of class E PAs. In general, this can be explained by the assumption that the only loss is the finite switch on resistance (r_{on}). Since both the loss and the output power scale with V_{DD}^{2}, their ratio, the overall efficiency, is ideally unaffected as the output power is adjusted through the variation in V_{DD}. Nevertheless, dc-dc converters, which are typically used to change supply voltages are very complex building blocks that have stability issues, and consume certain amount of power that affects the overall efficiency.

The simulated output power and efficiency as a function of the supply volt-

age are shown in Figure 3.10. It is evident that the efficiency is approximately constant within a certain range of supply voltages. At very low supply voltage, the output power drops, and becomes comparable to the losses from various sources, such that the efficiency drops below its constant value.
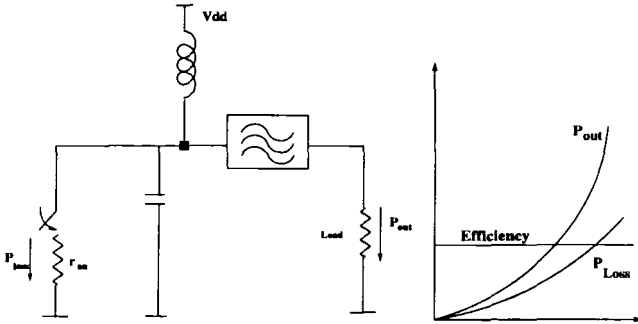
Figure 3.9.   Constant efficiency over supply voltage.
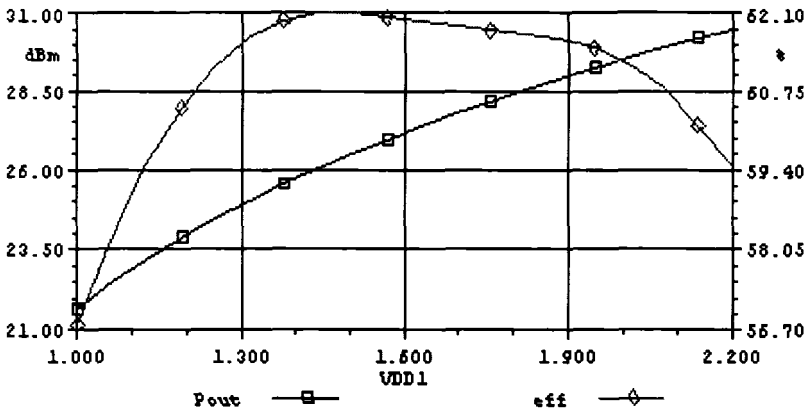
Figure 3.10.   Simulated output power and efficiency versus the supply voltage.

3.   Effect of Finite Ground inductance

Ground bounce is a critical performance limiting factor for high power PAs. It results from the ground plane having a finite inductance associated with it. This inductance affects both the efficiency and the gain of the PA, in addition to generating unwanted tones. Having a number of bond wires in parallel, connected to the ground pad, is a way to minimize their values. However, this will increase the number of pads dedicated to ground, and thus increases the overall area of the chip. The previous discussion on Class E power amplifier, together with the exact analysis given in [43], [44] assumes negligible source

inductance. Figure 3.11 shows the effect of a finite source inductance of 1nH on the current, and voltage waveforms. When the switch is ON, the voltage on the drain does not settle at a minimum level, instead it has a much higher value than the ideal case. Comparing Figure 3.12 with Figure 3.10, the efficiency is not constant as the ideal case. In fact it decreases as the output power increases, and the level of output power is much smaller than the ideal case.
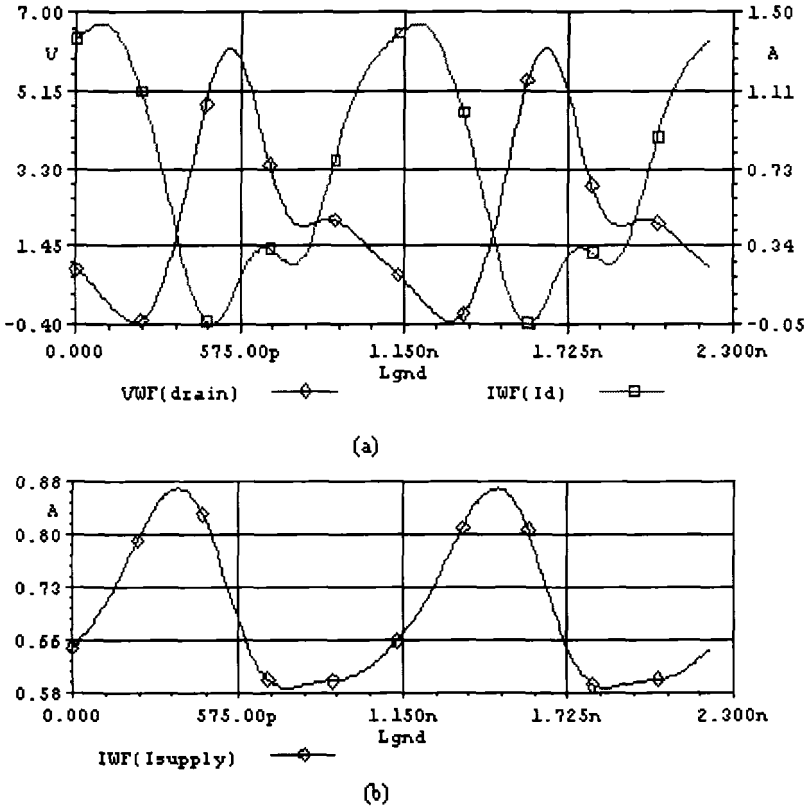
Figure 3.11. Simulated current and voltage waveforms of class E PA with 1nH source inductance.

4. Layout Considerations

The power amplifier was layed out using CADENCE layout tool. The layout of RF devices, especially for power amplifiers, require special attention. The output transistor M_2 (Figure 3.4) carries 300mA of dc current, plus the RF current, and has a total width of 4.8mm. The transistor is arranged in 6 groups of transistors, with the first 5 having 66 fingers, and the sixth having 70 fingers. The drain contact area of each transistor is enlarged, and parallel layers

Figure 3.12. Simulated output power and efficiency versus the supply voltage of a class E PA with 1 nH source inductance.

of metal 1, metal 2, and metal 3 are used as drain and source connections such that the device is able to handle large currents. The output devices are placed as close as possible to the output pads.

Five output pads are connected to the transistor's drain, such that the bond-wire inductance is minimized, and the values of the output-matching network can be controlled. Also, many bond-wires can handle the large output currents. 9 ground pads were used in order t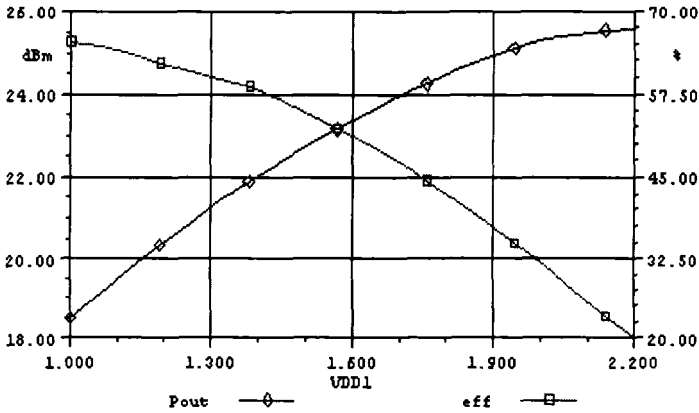o minimize the ground bond-wire inductance. A larger number was not possible since it would have caused an empty area inside the chip.

The layout of the chip is shown in Figure 3.13 using only metal pads as the RF pad. Another version of the layout was done using the pads provided by the manufacturer in order to provide ESD protection. The main problem with ESD pads is that they set limits on the current to be supported, plus they load the device with finite capacitance value that has to be subtracted from the designed value of the drain capacitance. The chip micro-graph of the former is shown in Figure 3.14, while that of the second is shown in Figure 3.15. The parasitics are extracted from the layout, and an estimation of the gate resistance based on the resistivity of the poly layer in the used technology (9 Ohm/sq.), and the number of gates used is included in the simulated schematic whose results are shown earlier. It is worth noting that no pad resistance or substrate resistance effect was available to account for.

5. Testing Procedures and Results

The class E power amplifier was fabricated using triple metal, double poly 0.35 μm nwell Standard process. The area of the chip is 1.4 mmx1.6 mm. The chip

has to undergo a cutting process since there was many circuits on the same die that left the cutting edge around 0.3mm away from the real edge of the circuit. This will add to the value of bond-wire inductances.

During test, a bare die has been attached directly to the ground plane of the printed circuit board to minimize the length of the bonding wires, instead of packaging the chip. Since the quality factor of the inductors connected to the output node and the supply of the output stage is critical to the performance of high efficiency power amplifiers, on-chip spiral inductors cannot be used in standard CMOS processes (with limited number of metal layers), due to the loss in silicon substrate and metal layers. Also, usually the available inductor models, if provided by the foundry are limited to certain inductors with finite width that has limited current capabilities. The bonded chip is shown in Figure 3.16.

The inductors required in this circuit are; the input matching inductor (10 nH), the inductor connected to the drain of the first stage (5.8nH), L_{RFC} (2 nH), and the inductor connected to the output node (2nH). The input matching inductor is implemented using both bond-wire, and an external inductor. The rest of the inductors are implemented using board traces while taking into account also the value of associated bond wires. The micro-strip line inductance, and capacitance were calculated using micro-strip calculator [46]. Figure 3.17 shows the details of the board. The whole circuit uses only two external elements, the output matching capacitance (14.5pF), and the input matching inductor.

The first prototype was tested by applying an RF signal at 900MHz, and 10dBm input power to the input matched port. A supply voltage of 2V was used to avoid the excessive increase in temperature at higher supply levels. Figure 3.18 shows the obtained results which is similar to the simulation results shown in Figure 3.12, indicating a relatively high value of ground inductance. Instead of constant or increasing efficiency with the increase in the supply voltage, the finite source impedance consumes higher power, and decreases the overall efficiency of the amplifier.

A second prototype was implemented with more careful chip bonding. Figure 3.19 shows the expected variation of output power and PAE with the supply voltage. The class E power amplifier delivers a maximum output power of 24dBm at 2V supply with a maximum of 48% power added efficiency. Figure 3.20 shows the variation of output power and efficiency within the band of interest. It is worth noting that higher output power levels can be obtained provided that more accurate models are used, and lower values of ground inductances.This design can be used for applications in the ISM band, and with higher level of output power, it can be utilized for the GSM standard.

6. **Towards a Multi-Standard Class E Power Amplifiers**

It is the authors' point of view that class E amplifiers are the most suitable power amplifiers for multi-standard operation, especially when preceded with a pseudo-class E driver stage.

First, linear power amplifiers require inter-stage matching, and bias adjustment that is dependent on the operating frequency. Since the amplifier in this case is used as a current source, its transconductance, g_m, is a function of frequency, as well as the power gain of the amplifier. Nonlinear power amplifiers on the other hand utilize the transistor as a switch, so basically only wide enough transistors, driven by the proper signal is required. The only problem in this case is the driver stage, being able to generate the required switching signal at different frequencies, representing different applications or standards or bands. Class F can be a solution provided that its harmonic traps are off-chip. As mentioned earlier, this means having larger circuit foot-print. An inverter-based driver can't be used unless it is covering a wide range of frequencies. A class E stage on the other hand, requires only the variation of the inductance connected to the input stage to be tuned for a different frequency.

A *CDMA/Bluetooth Multi-Mode Design*

Multi-standard operation is divided into two categories, either multi-band or multi-mode operation. While the former means having the same modulation scheme but different frequency of operation, the latter is more general as it incorporates different applications at different frequencies. A multi-mode PA for example can support both the Bluetooth (2.4GHz band) and CDMA (1.9GHz) standards. The general schematic of the class E amplifier in Figure 3.3 indicates that 5 elements are governing the operation of a class E PA; R, L, C, X, and C_D. L and C form the resonant circuit, and they are usually replaced by the matching network that will transform the 50 ohm resistance to the required optimum load at a given frequency. Thus, if the same configuration should be used for two standards, a double section matching network(refer to Figure 3.21) should be designed such that it will transform the 50 Ohm to resistance R_1 at a frequency f_1 and transform the 50 Ohm to resistance R_2 at a frequency f_2. The remaining parameters are the excess inductance X/ω and shunt capacitance C_d. Practically, it is more realizable to change the capacitance C_d than changing an inductance. Thus, the value of the excess inductance should be kept constant.Therefore,

$$[\frac{v_{dd}^2}{\omega P_{out}}]_{CDMA} = [\frac{v_{dd}^2}{\omega P_{out}}]_{BT} \tag{3.8}$$

substituting by the values of output power(20dBm for Bluetooth, and 30dBm for CDMA) and operating frequency,

$$\frac{[v_{dd}]_{CDMA}}{[v_{dd}]_{BT}} = 2.78 \tag{3.9}$$

since $v_{D,max}$=3.562 v_{dd}= 8V (from technology parameters), $[v_{dd}]_{CDMA}$ = 2.24V, $[v_{dd}]_{BT}$ = 0.8V.

Substituting in the parameters equations, the optimum load resistance needs to be changed from 2.9 Ohm(CDMA) to 3.5 Ohm (BT), and the capacitance from 5.1pF (CDMA) to 3.4pF (BT).The remaining problem is to determine the dimension of the transistor and decide whether to use a single ended or a differential structure.

The theoretical model(Section 3.2), implemented in MATLAB, for determining the optimum dimensions of the transistors in class E stage is used in the case for the CDMA and Bluetooth parameters. It provides the effect of changing the width of the transistor's gate on the output power and power added efficiency (PAE). Figure 3.22 and Figure 3.23 illustrate this effect for both cases.

It is clear from figure 3.23 that a single ended class E amplifier won't be able to achieve 1W of output power under a low supply voltage of 2.2V using the available technology parameters, thus a differential structure has to be used. In order to utilize the same transistor for both standards, the input has been adjusted to achieve the required output power in each case for the same number of fingers. This has led to a compromise in the power added efficiency for the Bluetooth case since the point of maximum power added efficiency doesn't coincide with the point of the required output power.

A 900MHz/1.9GHz Dual-band Design

The previous example suffers from the fact that implementing two standards having different output power levels, together with different frequency bands will result in performance degradation in the case of the lower output power standard.

On the other hand, having multi-band operation is possible using the same supply voltage, input power, but varying the input, and output matching, together with the inter-stage inductors. Figure 3.24 shows a 1.9GHz power amplifier that uses the same core of the fabricated amplifier (shown in Figure 3.4), with the slight variation in the drain capacitance to account for the different frequency bands. The variable drain capacitance can be implemented either by a wide-range varactor, or by a number of drain capacitors to be connected together using CMOS switches. Figure 3.25 shows simulation results describing the variation of output power and efficiency around 1.9GHz band. From this

discussion, it is evident that the same amplifier core can be utilized at different band, without sacrificing performance provided that the level of output power is preserved.

7.   Summary

This chapter has presented the design and implementation of a 900MHz class-E PA. The single-ended input, single-ended output amplifier has been implemented in $0.35\mu m$ CMOS technology. Measurement results have shown a maximum output power of 24dBm delivered to a 50Ohm load with 48% efficiency, operating from a 2V supply. Different layout considerations, and the effect of ground inductance has been discussed. A physically-based model of the class-E PA has been used to question the advantages and disadvantage of using the same amplifier core for multi-mode operation. A 1.9GHz power amplifier that uses the same core of the fabricated 900 MHz amplifier has been presented. Thus proving that the same amplifier core can be utilized at a different frequency band, without sacrificing performance, provided that the level of output power is preserved.
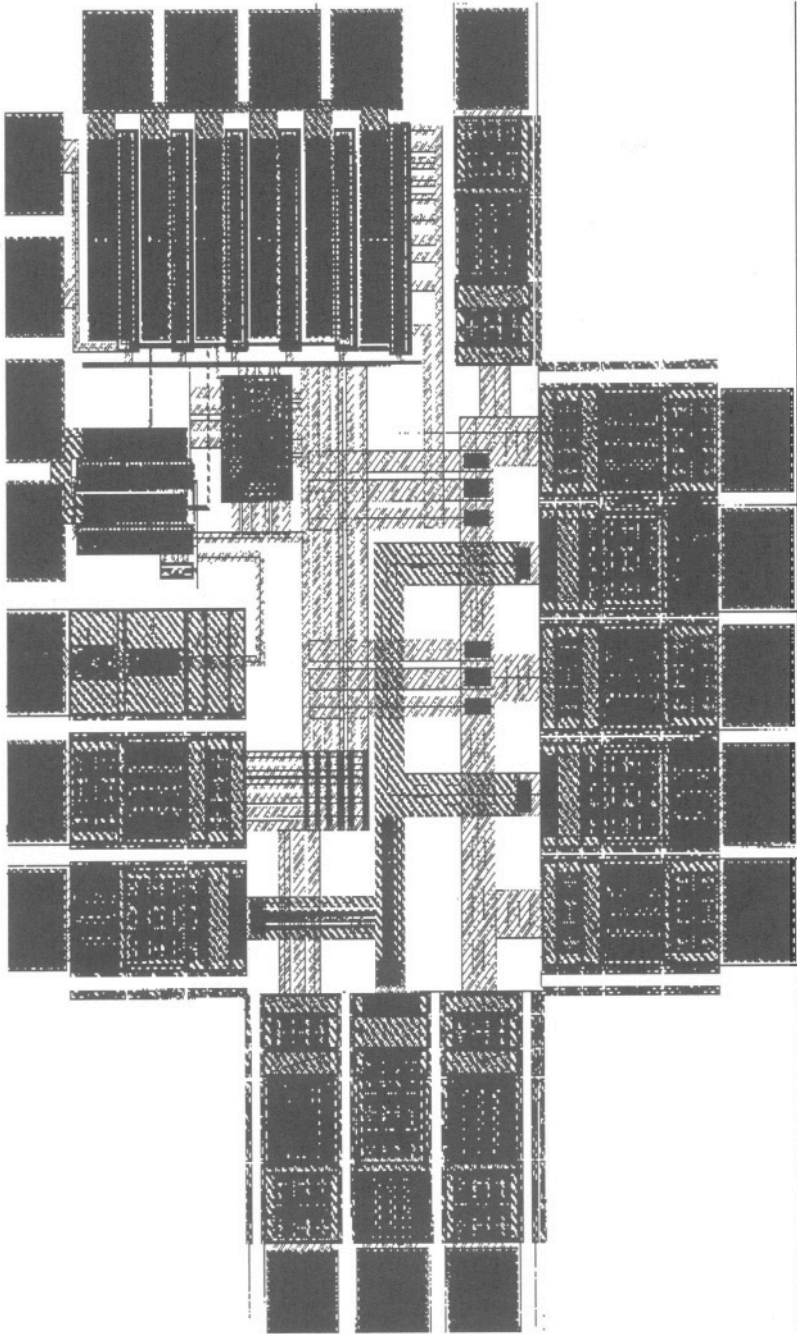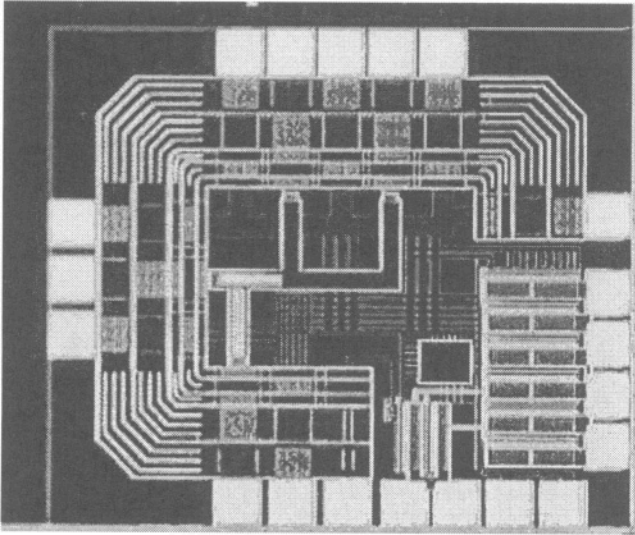
Figure 3.13. Layout of Class E PA.

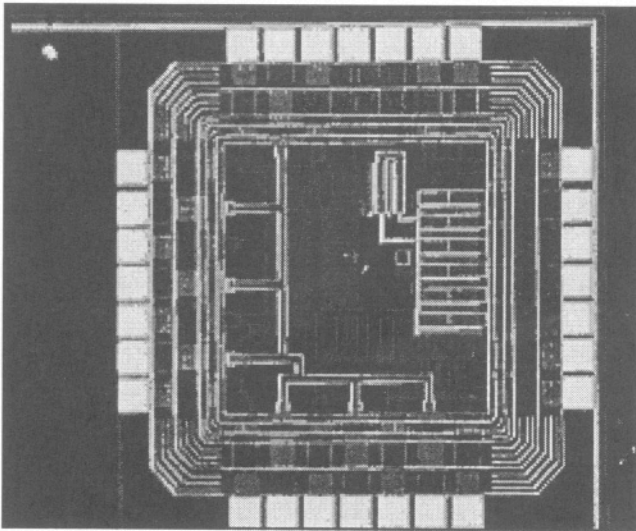*Figure 3.14.*   Chip micro-graph of the class E PA (output pads don't have ESD protection).

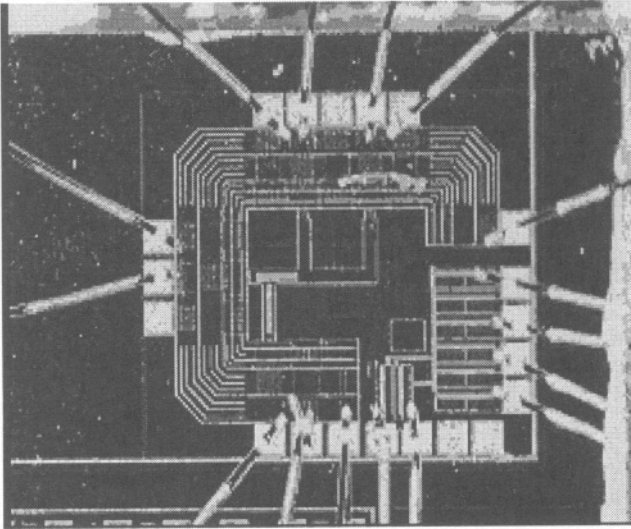*Figure 3.15.*   Chip micro-graph of the class E PA (output pads with ESD protection).

Figure 3.16. Bonded chip micro-graph.
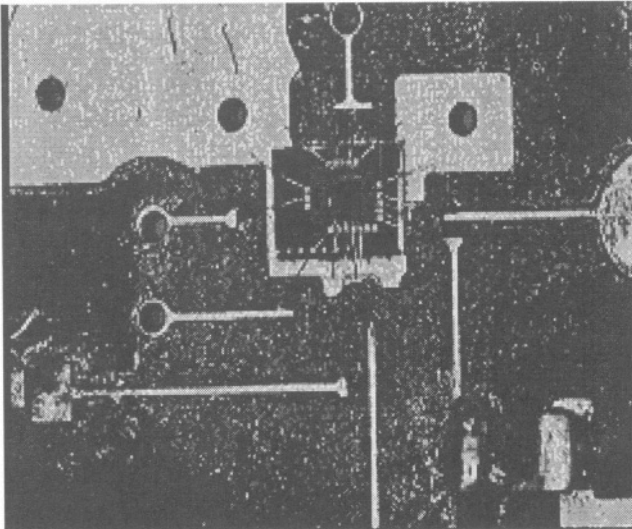

Figure 3.17. Implementation of inductances using board traces.
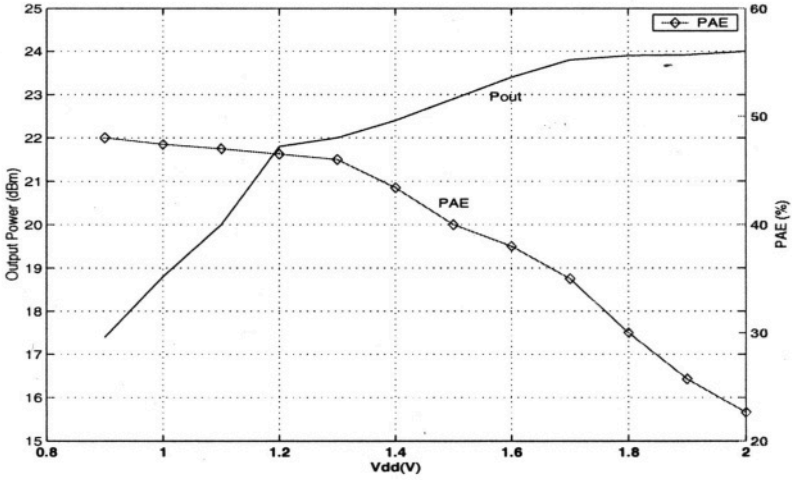
Figure 3.18.   The measured output power, power added efficiency of the power amplifier at 900MHz, indicating relatively high ground inductance values that is affecting the operation of the amplifier as a class E stage.
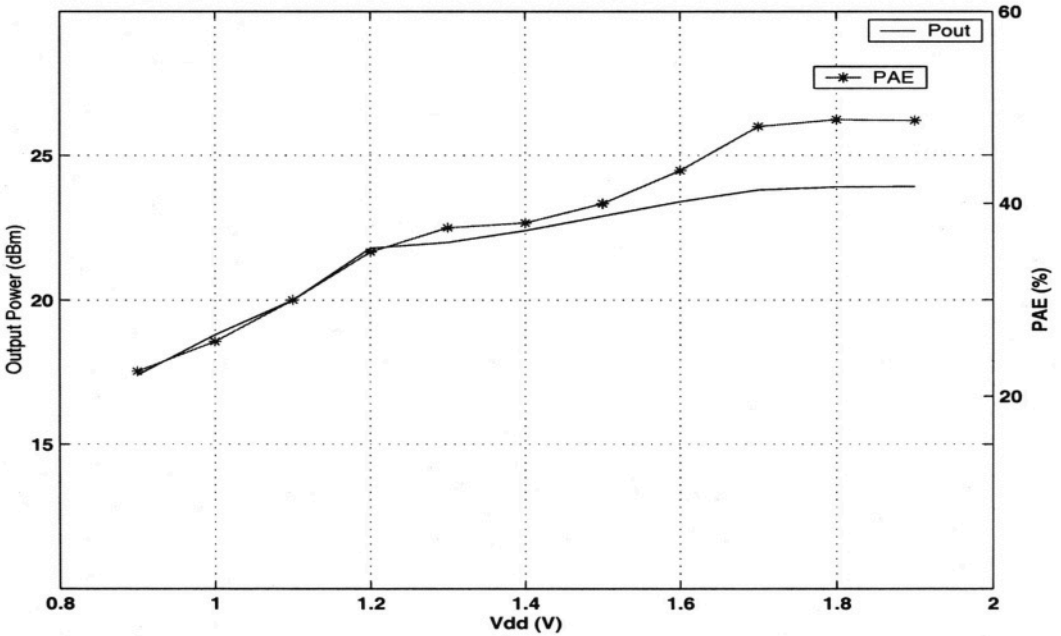
Figure 3.19.   The measured output power and efficiency of the power amplifier at 900MHz.
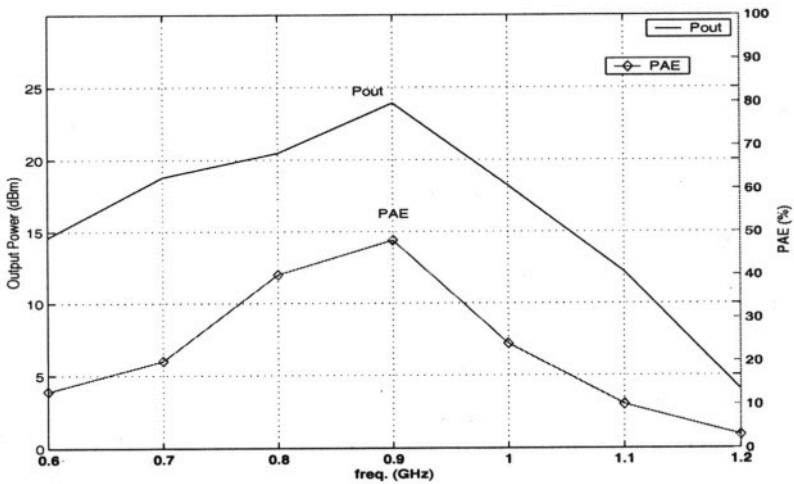
Figure 3.20. The variation of output power and efficiency within the band of interest.
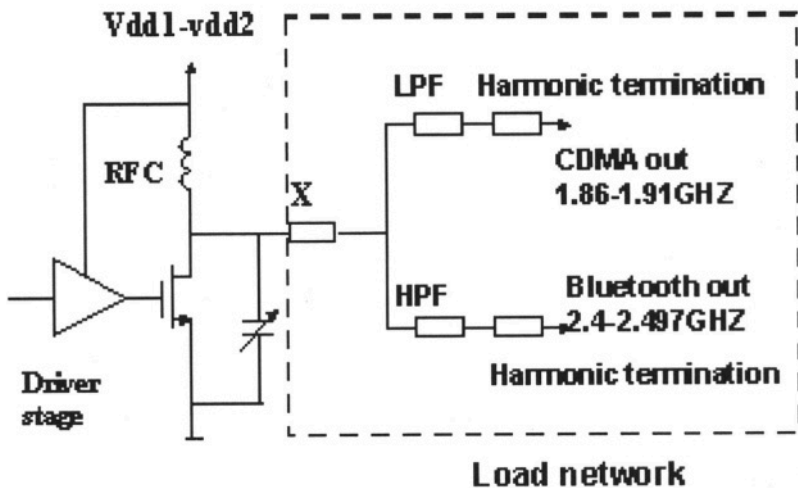
Figure 3.21. A double section matching network to transform 50 Ohm load to two different optimum loads corresponding to two different frequency bands
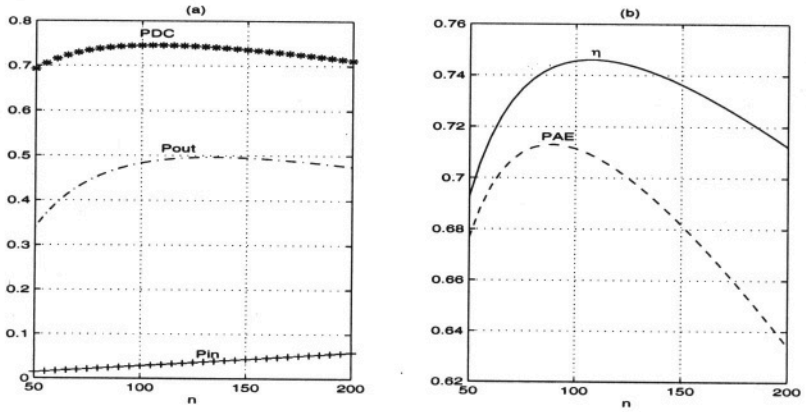
Figure 3.22.   DC power (PDC), input power (Pin), and output power (Pout) (b) Efficiency and Power added efficiency (PAE) versus number of gate fingers (CDMA 1.9GHz)
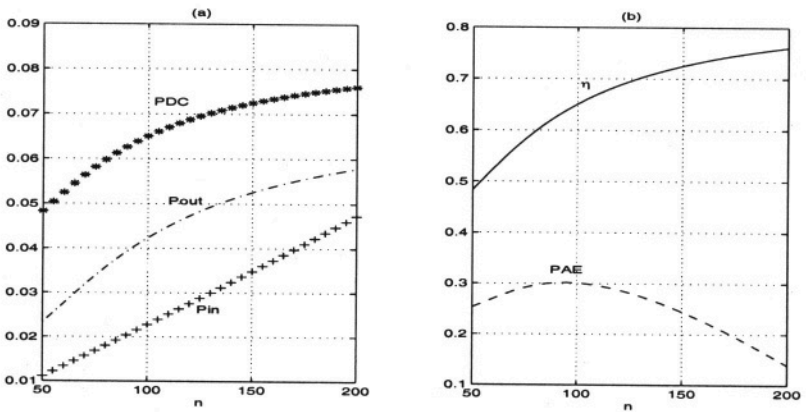
Figure 3.23.   (a) DC power (PDC), input power (Pin), and output power (Pout) (b) efficiency and power added efficiency (PAE) versus number of gate fingers (2.442GHz)

Figure 3.24. Schematic of class E PA operating at 1.9GHz.

Figure 3.25.   (a)Variation of output power and efficiency at 1.9GHz, (b) Input matching.

Chapter 4

A CMOS PA FOR BLUETOOTH

1.   Introduction

Bluetooth is a wireless connectivity standard that provides low cost wireless voice and data communications to link mobile phones, PDA, PCs, digital cameras, and other portable information appliances. Bluetooth is considered to be a high speed, short distance wireless technology, working in the 2.4 GHz radio spectrum

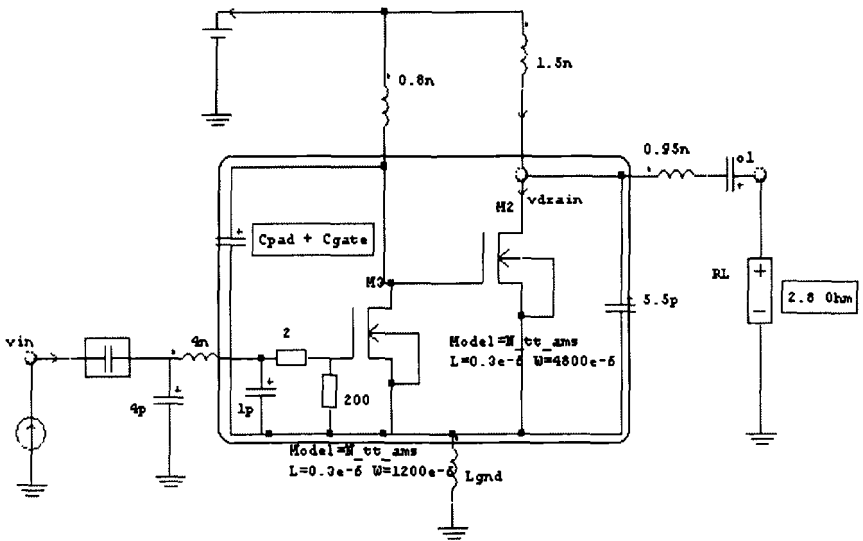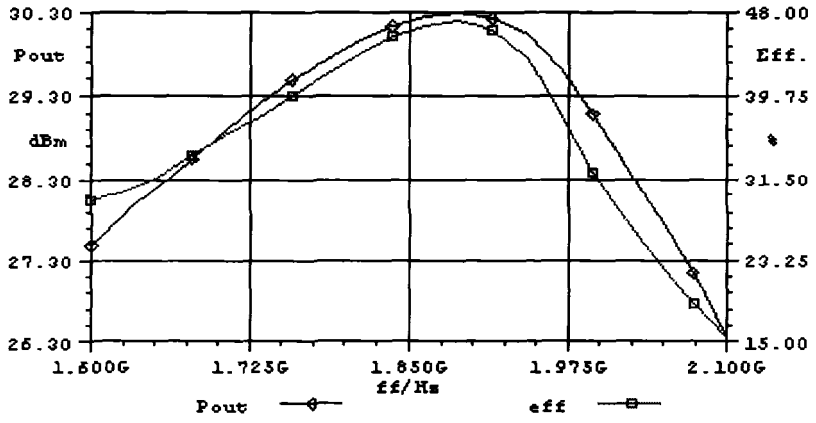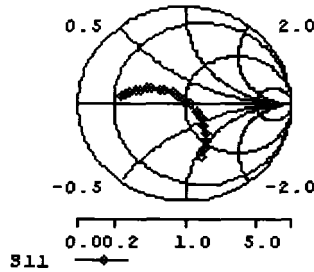Bluetooth devices essentially come in three classes, all using point-to-point communication. Class 3 devices operate at the 0 dBm range and are capable of transmitting 30 feet, through walls or other objects. Class 3 products are expected to include USB and PC-card devices. Class 2 devices operate at the 4 dBm range. The third class of devices is class 1. These devices operate at 20 dBm, which allows for the signal to travel about 300 feet. It is likely that common class 1 Bluetooth-enabled devices will be cordless phones and wireless modems. All Bluetooth classes are rated at about 1 Mb/s, with next generation products allowing anywhere from 2 to 12 Mb/s.

According to Table 4.1, A class 1 equipment with a maximum transmit power of 20dBm must be able to control its transmit power down to 4dBm or less [47]. The power control is used for limiting the transmitted power over 0 dBm. Power control capability under 0 dBm is optional and could be used for optimizing the power consumption and overall interference level. The power steps would form a monotonic sequence, with a maximum step of 8dB, and a minimum step of 2dB. Bluetooth-enables devices with power control capability optimizes the output power in a link with link manager protocol (LMP) commands. It is done by measuring the received signal strength using a Receive Signal Strength Indicator (RSSI) and reporting back, if the power should be increased or decreased.

Table 4.1. Power classes for Bluetooth

power class	Max. output power	Min. output power	Power Control
1	100mW(20dBm)	1mW(4dBm)	4dBm to P_{max}
2	2.5mW(4dBm)	0.25mW(-6dBm)	Optional down to -30dBm
3	1mW(0dBm)	N/A	Optional down to -30dBm

Bluetooth is considered a low performance standard, that is targeting a huge market. Thus a low cost, high yield technology such as CMOS is the most adequate solution. This year, 5 complete CMOS transceivers have been announced that target the Bluetooth class 3 standard [10], [48], [49], [50], [51]. The complete transceiver reported in [10] includes the RF front end, digital base-band processor, microprocessor, and flash memory. In the near future, the transceiver should be able to support all transmission classes, extending its output power range to 20dBm.

This is the focus of this work; trying to realize a 2.4GHz CMOS power amplifier to be integrated, or even connected in the same package to the rest of the transceiver in order to achieve a complete solution. This chapter discusses the design issues, the implementation, and measurement results of a class AB power amplifier targeting the Bluetooth standards, or the 2.4GHz-2.5GHz ISM band in general.

2. CMOS Power Amplifier Design

The power amplifier presented in this work operates in a class AB mode, which represents a compromise between efficiency and Linearity. Class AB has a maximum drain voltage equals twice the supply voltage, which is lower than the stress(maximum drain voltage) in class E and class C as mentioned in chapter 2. Also the Power utilization factor (The ratio of the RF power delivered by a device in a particular mode under consideration to the power it would deliver as a simple class A amplifier) is better than that of classes C and E. A single-ended input, single-ended output configuration has been employed to minimize losses, cost and space encountered when utilizing either an external balun or a micro-strip balun.

Normally in any design, 2-3 stages are required, depending on the output of the mixer in the transceiver chain and the gain of the single amplifier stage. In this application, an input of 4dBm is used, considering that the input of the PA will be a typical class 1, or 2 Bluetooth-transmitter. Thus a total of 16dB of large signal gain is required.

The main idea in employing a class AB is that it can be easily modified to match the requirements of constant-envelope modulation or non-constant

envelope modulation techniques by adding Linearization in either software or hardware. For example, the same power amplifier used for Bluetooth can be utilized for the IEEE802.11 DSSS that utilizes DQPSK modulation with very relaxed Linearization requirements.
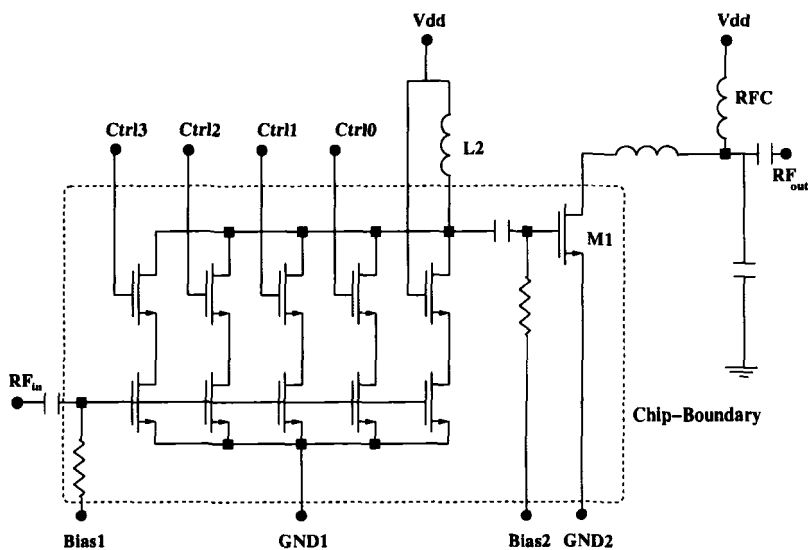
2.1 Design of the Output Stage

Figure 4.1. Simplified schematic of the power amplifier.

The simplified power amplifier schematic is shown in Figure 4.1. It consists of two stages with integrated inter-stage matching. The output stage design starts by determining the transistor's width, adjusting the biasing voltage and the input signal amplitude to achieve class AB operation. The transistor in the output stage is initially sized by determining the required drain current assuming an efficiency of approximately 50%, output power of 100mW, and a 3.3V supply. By performing DC analysis, the drain current can be plotted as a function of the gate voltage for different transistor dimensions. This is considered as an initial guess to start with.

The next step is the determination of the optimum load, the transistor should have its input matched to the source, and a tuned circuit at the center frequency of the operating band is connected to a variable load resistance at the output node. Harmonic balance simulations are performed to find the load resistance that would deliver the required output power at an acceptable efficiency. This process can be repeated by varying both the transistor's width and the load till optimum performance is obtained. Figure 4.2 shows a simple test circuit and the simulation results used to determine the optimum load. A more theo-

retical analysis would employ using a transistor model valid for all modes of operation (cut-off, triode, and saturation), and vary both the load, and the dimensions. A 3-D plot with the output power or efficiency as the Z-plane would point to the required design variables. The optimum load in this case is 20-Ohm, which is reasonable compared to the 50-Ohm port impedance. Thus the losses in the matching network will be minimized. If higher output power levels are required, the optimum load is normally much smaller, requiring higher impedance transformation ratios.

In order to investigate the stability of the output stage, large signal simulation (Harmonic Balance) is performed to determine the input impedance of the output device under the given biasing and loading conditions. The simulation results have shown a possible instability due to negative input impedance at the operating frequency (2.442GHz). To stabilize any amplifier, it is a common practice, either to connect a shunt or series resistor to its input or output. For low-noise applications, the resistance is placed at the output while in high power applications, the resistance is normally placed at the input side. Thus, a 10-Ohm resistor in series with the gate of the output transistor was found adequate to stabilize the output stage of the power amplifier.

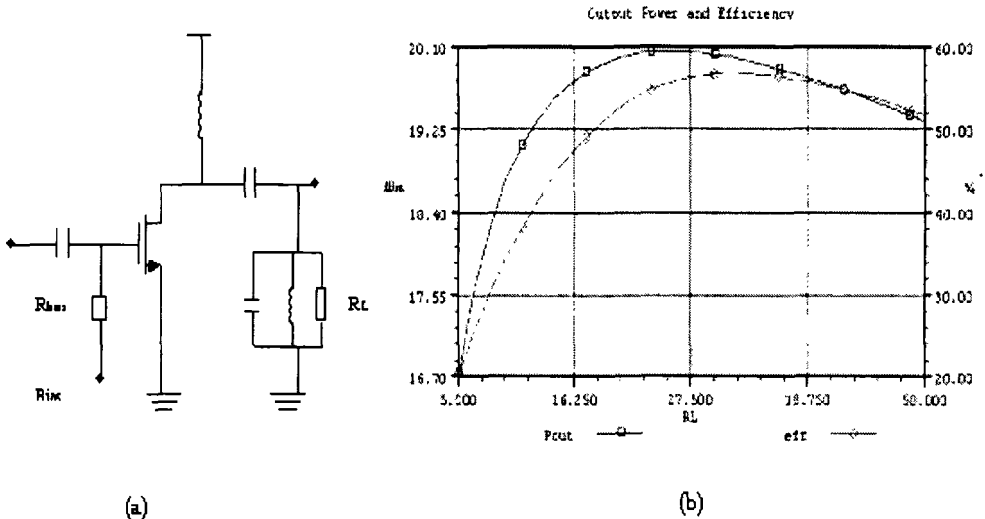(a)   (b)

Figure 4.2.   Determination of the optimum load.

2.2   Driver Stage

A band pass gain stage based on inductive load is employed as the input stage (Figure 4.3(a)). Inductive loads suit low voltage operation design since they
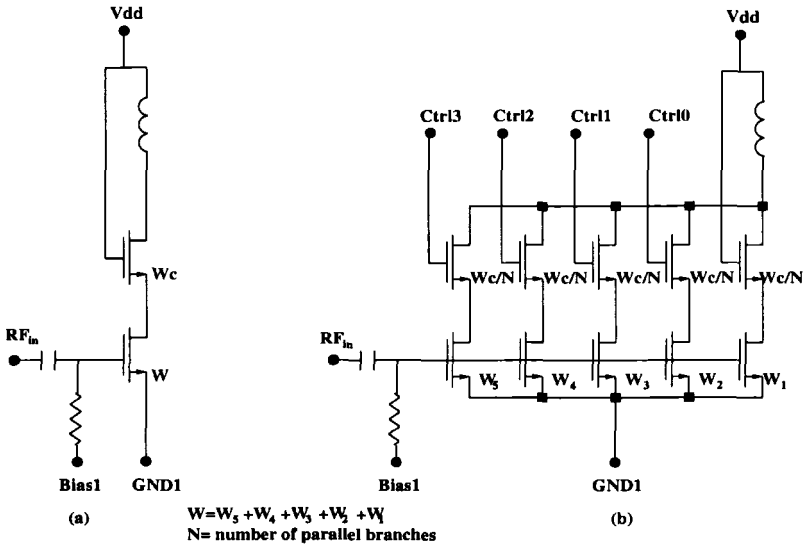
Figure 4.3. (a) A Fixed gain band-pass stage, (b) Parallel band-pass stages to implement power control.

don't consume dc headroom. Thus the inductor L2 (figure 4.1) tunes out the capacitance of the gate of the output stage transistor M1(figure 4.1) to create a circuit that resonates at the desired frequency. This resonating structure decreases the amount of current that is needed to drive larger capacitances inherent in the output stage.

The cascode transistor is used to reduce the miller capacitance and to ensure stability. The main design issues are to size the transistors and adjust the bias point such that the required gain is achieved and the input impedance has a reasonable value for input matching and stability. Figure 4.4 shows the variation of the gain (S21) and the real part of the input impedance as a function of the number of fingers of the cascode transistor while changing the width of the input transistor. As evident from the figure, as the number of fingers of the main transistor increases, the gain of the driver stage increases while the real part of the input impedance decreases.

2.3 Power Control Implementation

In order to control the output power level for the amplifier presented in this work, there are two ways; 1) Changing the output matching network such that the load impedance seen by the output device would vary. Theoretically, this would provide better efficiency at lower power levels. Practically, this cannot be realized since the output-matching network is off-chip, unless a dynamic
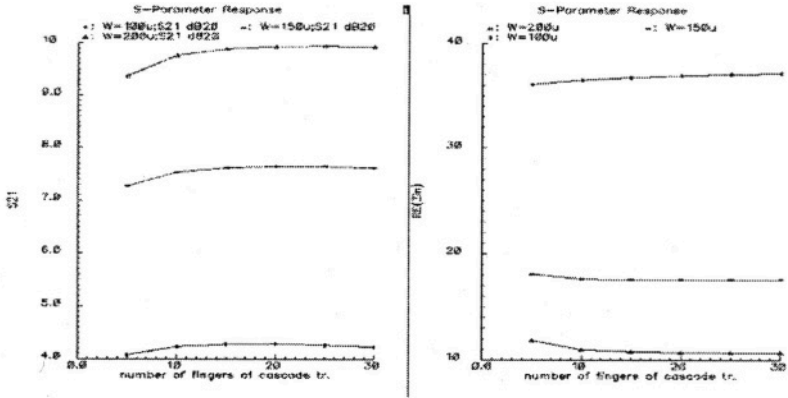
Figure 4.4. The gain (S21) and the real part of the input impedance vs the number of fingers of the input transistor.

variation technique similar to Doherty amplifier is employed. 2). Changing the gain of the input stage by varying the width of the input transistor. This might present different loading on the preceding stage, necessitating the use of a buffer stage. The first method would require two or more amplifiers in parallel, and the accurate implementation of $\lambda/4$ micro-strip lines. Thus increasing both the area, and the footprint of the amplifier. The second method is the one utilized in this work. Varying the width of the transistor in the input stage is equivalent to having a number of transistors connected in parallel and switching them on and off using external control signals, depending on the required output power as shown in Figure 4.3(b).

By referring to Figure 4.1, instead of using a MOS switch to connect each parallel branch, the cascode transistor is acting as a non-ideal switch. The output power level is controlled via the voltages Ctrl3, Ctrl2, Ctrl1, and Ctrl0. Figure 4.5 shows the variation of the output power and efficiency as a function of the number of fingers of the input transistor in the driver stage with $12\mu m$ unit transistor width.

In Figure 4.1, the inter-stage capacitance is adjusted to achieve matching. Biasing for the input stage is done on-chip, while that of the output stage is controlled externally.

3.   Implementation and Simulation Results

The detailed schematic of the core of the transistor is shown in Figure 4.6. The output transistor M1 is 1.44mm wide with $0.35\mu m$ length. In the layout, the transistor is partitioned into 4 separate transistors groups with substrate
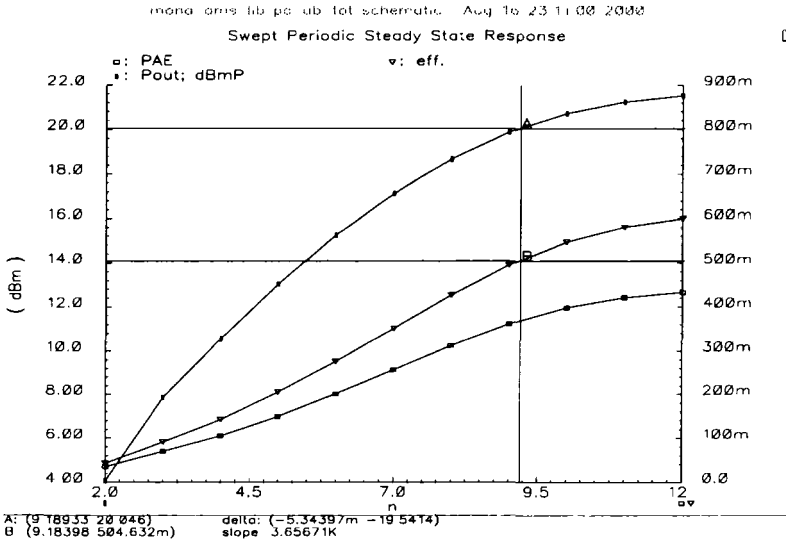
Figure 4.5. Effect of variation of the number of fingers on the output power and efficiency
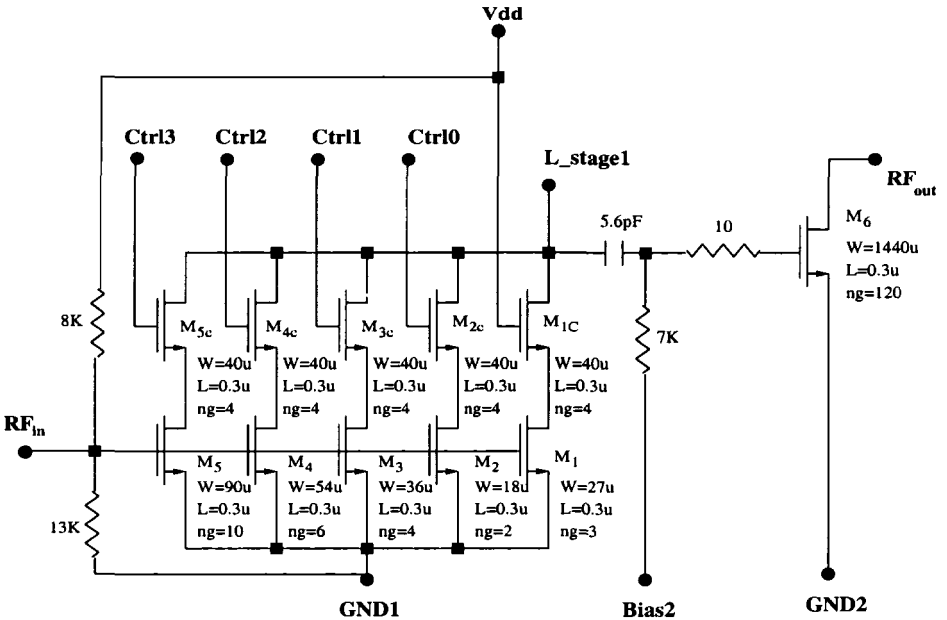

Figure 4.6. The core of the controllable gain power amplifier.

contacts surrounding each group of transistors as shown symbolically in Figure 4.7. In order to avoid any stability concerns, the ground nodes of the first and second stages are not connected together on chip. They have separate
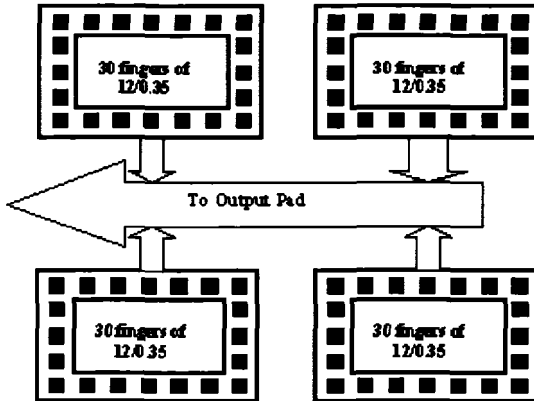
Figure 4.7. Layout of the transistor in the output stage.

nodes, and each is connected to a bond wire, then finally they are connected to the same PCB ground. This is a common practice in power amplifier design in order not to create inner loops and possible oscillations. The output transistor is located as close as possible to the output pad. The metal lines connecting the output node to the output pads are as wide as possible. The output pad is a simple metal pad with no ESD protection to minimize the pad capacitance, together with the fact that the normal pads supplied by the foundry has limited current handling capability that is much smaller than the current delivered by the PA. Additionally, since the output node is the drain of the transistor rather than the gate, the fear of electrostatic discharge is minimal. A total of 10 ground pads are used to minimize the ground inductance. In general, a larger number should be used, but this comes at the expense of the total area. The complete layout is shown in Figure 4.8.

The output-matching network converts the 50-Ohm to the optimum load. Output matching is implemented off chip using a bond wire inductance and an external capacitance. Implementing the inductor on-chip dictates the use of a relatively wide inductor to handle the large output currents. This will increase the chip area, and will introduce a series parasitic resistance in series with the output load, consequently decreasing the amplifierŠs efficiency. The choke coil (RFC) is implemented using micro-strip lines.

The core of the amplifier, together with bond-wire inductances, and the external matching elements are shown in Figure 4.9. The pads are represented by their parasitic capacitance only since no information was available on the substrate resistance. The interconnect resistances are also included.
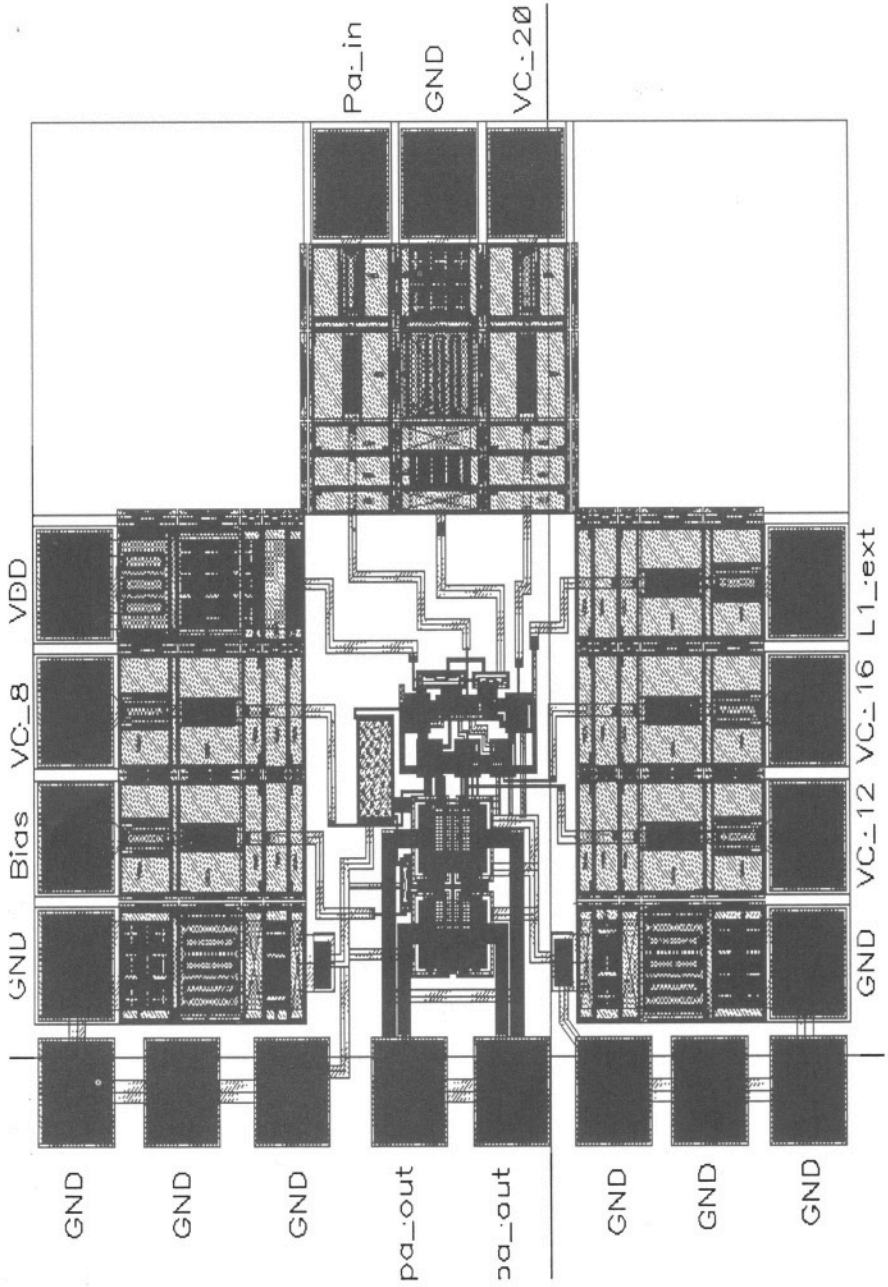
Figure 4.8. The complete chip layout.
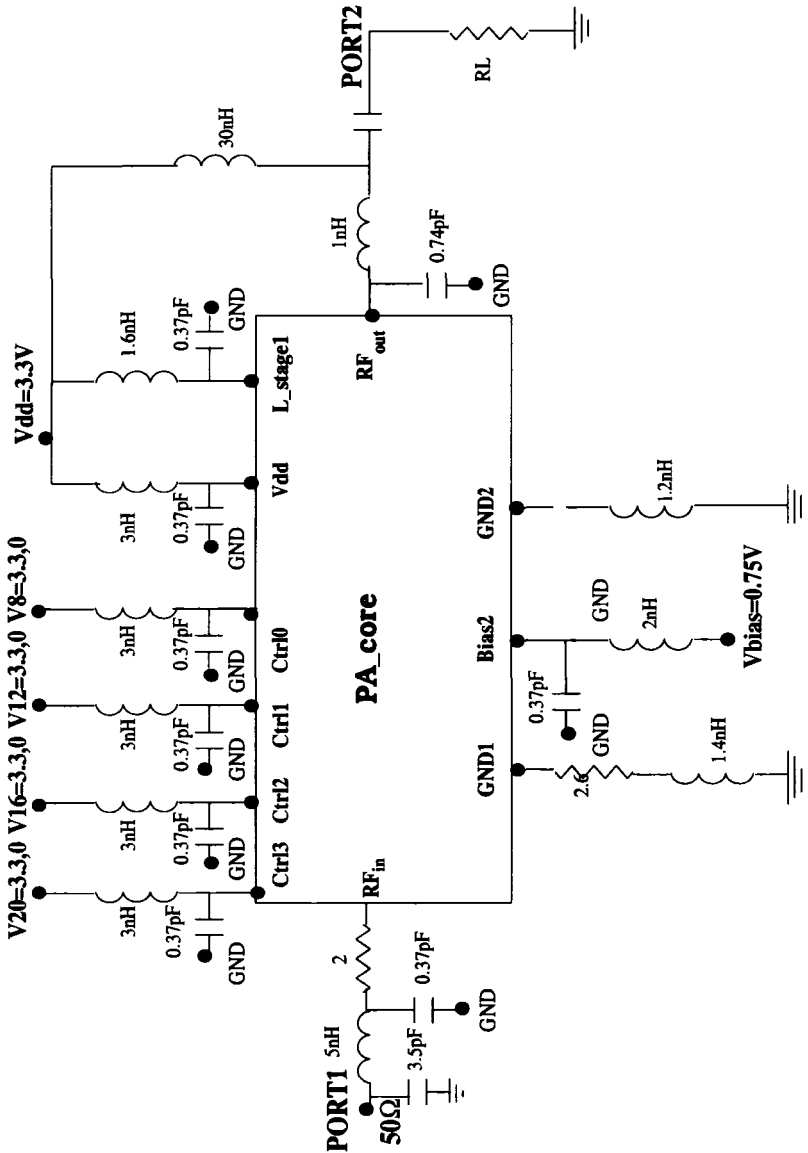
Figure 4.9.   The schematic of the amplifier together with pads, bond-wire inductances, and the external matching elements.

The extracted netlist of the PA is simulated using CADENCE (SPECTRE RF). Figure 4.10 shows the simulation results of the output power, and efficiency, together with the S-parameter of the amplifier. The simulation shows a maximum drain efficiency of 50% and PAE of 35%. The output power reaches 19dBm due to the effect of finite ground inductance, and large gate poly resis-
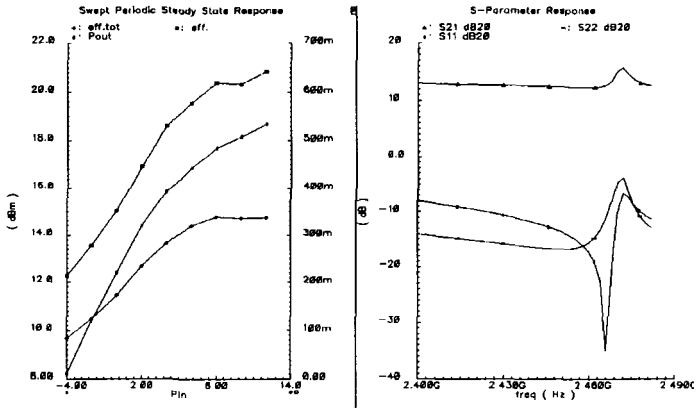
Figure 4.10. Simulation results (a) The output power and efficiency, (b) Input and output S-parameters.

tivity. The maximum output power of the designed power amplifier is limited by the device characteristics such as the saturated drift velocity, transconductance, critical field, and other parasitic resistances. To transmit more power, the environment of the PA rather than the PA itself has to be modified. In fact, trying to have a larger device would increase the parasitic capacitances, and thus lowers f_t, and the gain of the device at such high frequency.

4. Experimental Results

A prototype circuit was fabricated in 0.35μm, double poly, three-layer metal CMOS process. The chip area is 1 x 0.88 mm^2 including bonding pads. The prototype has been connected directly to the printed circuit board, using chip on board packaging. Short gold bond wires connect the ground pads to the die attach area. The supply pins are bypassed by 220pF capacitors. Inter-stage inductor was implemented using micro-strip lines. The micrograph of the fabricated amplifier is shown in Figure 4.11.

The test setup of the amplifier consists of dc blocking capacitors, high frequency network analyzer, and a spectrum analyzer. The amplifier is single-ended input, single-ended output. After connecting the source, and performing s-parameter simulations, the amplifier needed further tuning in order to achieve input matching. This was done by sliding a capacitor (0.5pF), between the input node, and the ground along the 50-ohm transmission line connected to the input source, till a point was achieved where the input was completely matched. Figure 4.12 shows the measurement of S_{11} versus frequency.

Following S-parameter measurements using the network analyzer, the maximum output power was observed to be centered around 2GHz, but failing to
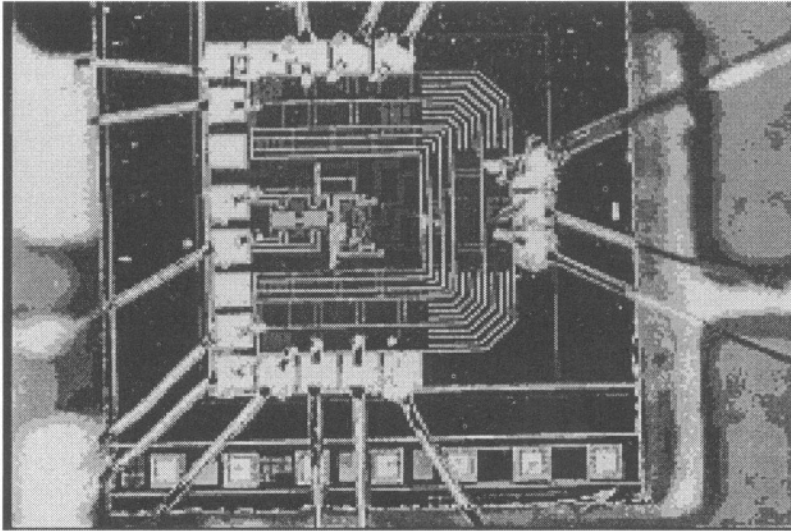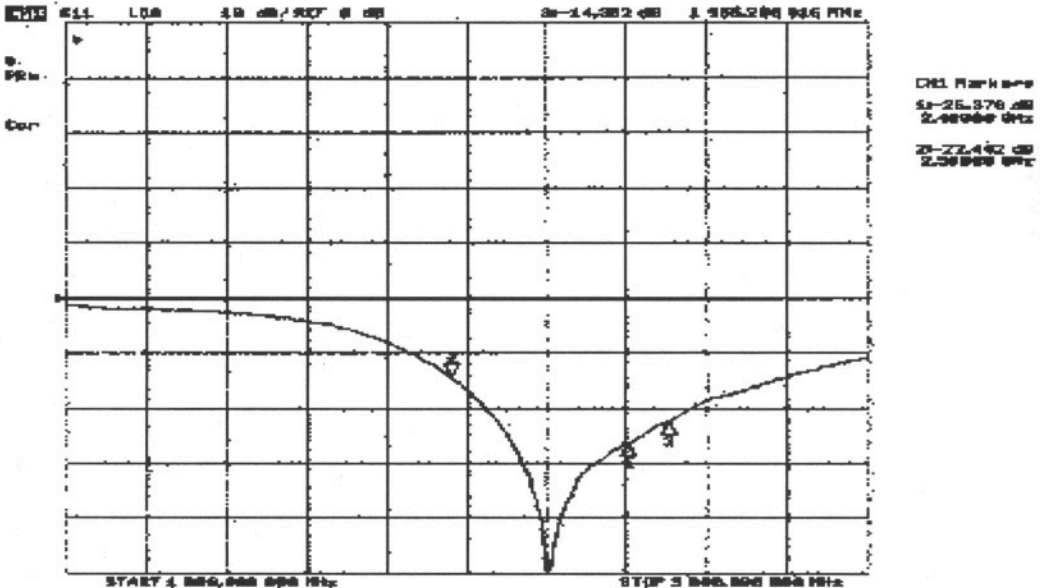
Figure 4.11.   Chip micrograph.

Figure 4.12.   Measurement results of the input matching.

reach the targeted frequency of 2.4GHz. This was also observed by another design (Low Noise Amplifier). In fact the technology was very poorly modelled at such high frequency. The transistors also failed to give the required

high gain above the 2GHz-2.1GHz limits. Figure 4.13 shows the output of the power amplifier versus frequency.

The RF power amplifier was tested, by measuring the RF power at the 50-Ohm output port. Figure 4.14 shows the measured output power and power added efficiency of the amplifier versus the input power, measured at 1.91 GHz and 3.3V supply. The maximum output power is 16.6dBm with PAE of 33%. It is worth noting that higher output power levels can be achieved using more accurate transistor models and lower ground inductance values.

Figure 4.15 demonstrates the variation in the gain of the power amplifier in 2 dB steps by connecting or disconnecting the parallel branches in the input stage.

The power amplifier operates from a supply voltage range of 1.75V to
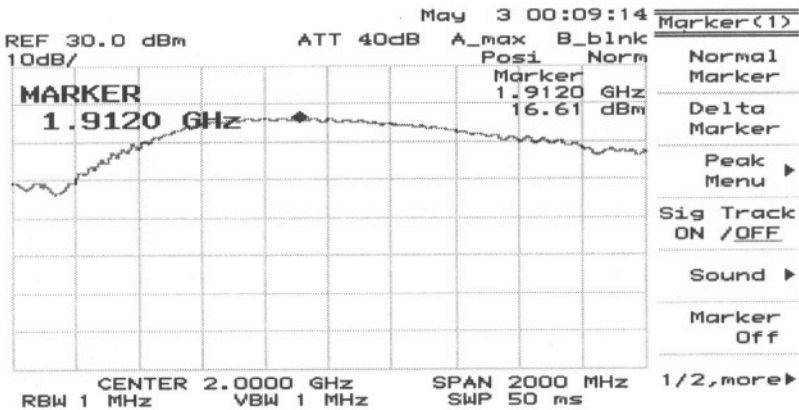
Figure 4.13. Measured output power versus frequency.

3.3V. The output power and efficiency versus the supply voltage are shown in Figure 4.16. It is worth noting that the amplifier is relatively wide band with a maximum power at 1.91GHz. It is suitable for operations up to 2.1GHz with 1dBm drop in output power [52]- [53]. A comparison of most published CMOS power amplifiers is listed in Table 4.2. The amplifiers presented in [4] and [22] have the output power controllability feature. However, both use nonlinear power classes that require complex linearization circuitry if used for non-constant envelope modulation techniques. The linear power amplifier presented in [24] used a CMOS process with high resistivity substrate and thin oxide MIM capacitor, thus decreasing parasitics, and achieving high efficiency and output power. It is worth noting that while [13], [14], and [24] target GSM, EDGE, and UMTS standards, which require 30dBm output power, this work focuses on lower power-class transmitters.
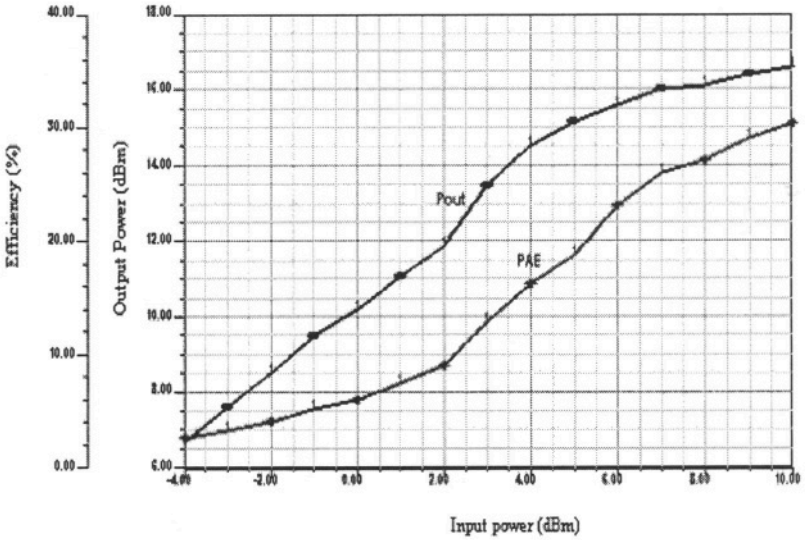
Figure 4.14.   Measured output power and PAE versus input power.
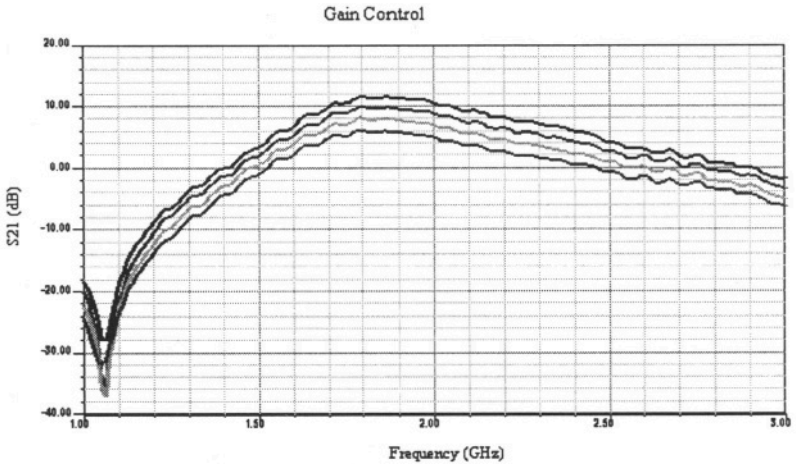
Figure 4.15.   Measured data showing the variation of the gain with control voltage settings.

5.   Summary

A 1.9GHz-2.1GHz class AB power amplifier has been presented with PAE of 33%. The fabricated power amplifier delivers a maximum output power of 16.6dBm to a 50-Ohm load. The output power can be controlled easily by employing a number of parallel semi-cascode branches. By utilizing more accurate transistor models, the same concept can be extended to higher frequency
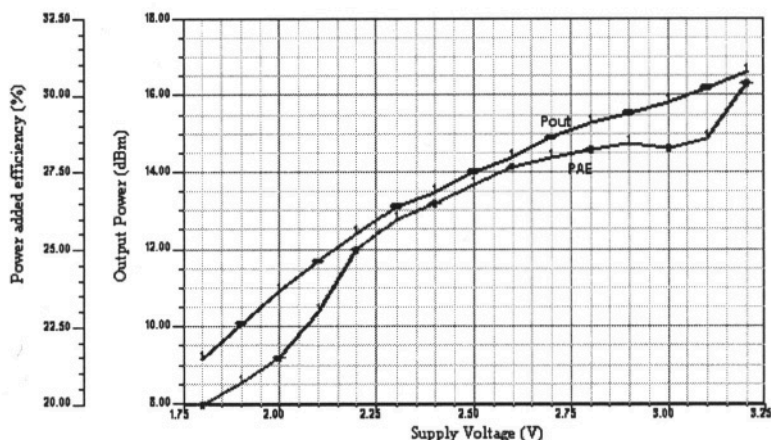
Figure 4.16. Measured output power and efficiency vs. supply voltage at 1.91GHz.

Reference	Process	Frequency (MHz)	Pout (dBm)	PAE (%)	V_{dd} (V)	Area (mm^2)	Class
[4]	1μm	900	13	30-40	3	6.82	C
[18]	0.8μm	824-849	30	42	2.5	1.5	D
[9]	0.25μm	900	29.5	41	1.8	4	E
[13]	0.35μm	1900	30	48	2	0.6	E
[14]	0.25μm	1950	29.2	27	3	N/A	B
[24]	0.35μm	1730	30.4	45	3.5	1.9	AB
[22]	0.25μm	1400	24.7	43	1.5	2.37	F
[23]	0.2μm	900	31.7	43	1.8, 3	2	F

Table 4.2. Performance comparison of CMOS PAs.

applications such as Bluetooth radios, which use a controllable 20dBm trans-
mitter. Operating at class AB, the power amplifier is relatively linear, and sim-
ple Linearization means can be employed to make it suitable for non-constant
envelope modulation standards.

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Chapter 5

A COMPLETE BLUETOOTH PA SOLUTION

A complete Bluetooth solution requires a power amplifier arrangement that is capable of supporting the three classes of transmission. Two solutions are possible. In Figure 5.1(b), an amplifier capable of implementing classes 2, and 3 is connected directly to a class 1 PA. During class 1 transmission, the output of the class 2 PA feeds the final PA stage, which directly feeds the antenna. For class 2, and 3 transmission, the class 1 PA is operating at the lowest gain mode (approximately a gain of 1-2 dB), and acts only as a buffer stage to the preceding class 2, or 3 PA. Although this method offers an integrated solution, its overall efficiency is dependent on the efficiency of the amplifier in the low-gain mode, which will be typically very small. Thus this method suffers high current consumption at class 2, and 3 transmission unless a power amplifier with very wide range of constant efficiency is implemented, which is hard to achieve at low output power levels.

Figure 5.1(a) shows a more efficient solution, since the class 1 PA (which has high current consumption as it is required to deliver high power) is bypassed by a switch. In this case the switch arrangement connects either class 1, or the preceding class 2/3 PA to the antenna. Another switch disconnects the output of the 20dBm PA from the Antenna in order not to load the 4dBm PA with the matching network of the final stage. Integrating this solution is subject to the availability of low loss switches, which might be true with new emerging technologies such as MEMS technology [54]. Even with an integrated solution, at least the switch connecting the output of the 20dBm PA to the Antenna has to be off chip since the output-matching network of the power amplifier is itself off-chip.

In the following sections, the implementation of two power amplifiers in 0.18μm technology is discussed. The first PA targets class 3 transmission, and can be extended to cover both class 2, and 3 by adding a variable gain ampli-

fier as a preceding stage. The second PA targets class 1 operation, and can be controlled down to 4dBm. These amplifiers are to be employed in the power amplifier arrangement of figure 5. l(a) since the overall current consumption of this arrangement is much lower than that of figure 5.1(b).
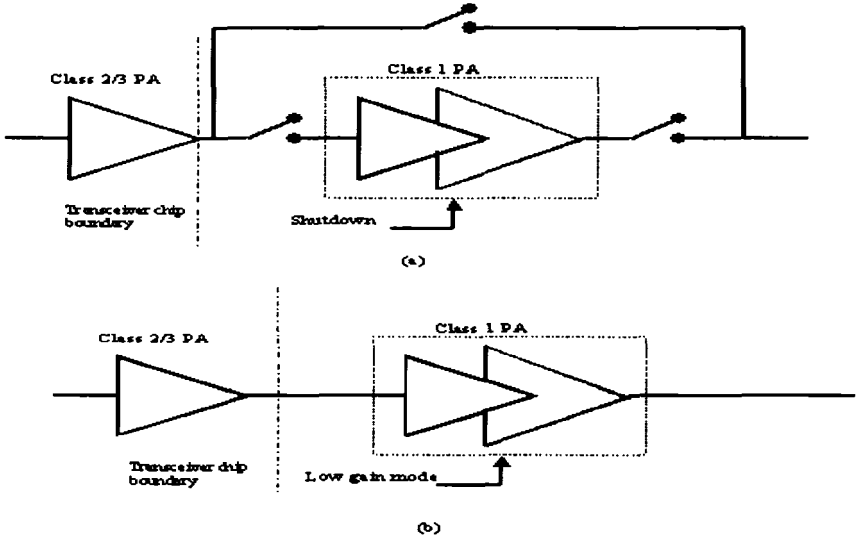

Figure 5.1.   Possible power amplifier arrangements to support all Bluetooth classes of transmission

1.   A CMOS PA for Class 2/3 Bluetooth

According to Bluetooth standards, class 3 transmission is required to deliver OdBm of output power. Its operation can be extended to class 2 transmission provided that it can reach 4dBm. This block is normally integrated with the complete Bluetooth transmitter, thus input matching to 50-Ohm is not required. Also, since its power level is low, it is in fact acting as a pre-amplifier in case a 20dBm PA is added. Since the efficiency for the preamp is not as critical as the PA a nonlinear operating class, requiring an expensive and lossy external filter is neither necessary, nor saves power. Due to the lack of good PMOS transistors, a class B push-pull approach is also unavailable. If the pre-amplifier (0dBm/4dBm) output harmonics that could degrade the PA efficiency are kept low, a class A amplifier can drive the class 1 PA without any external filters. The only requirements for the low-power amplifier classes in this case, are sufficient Linearity, the required output power, and current consumption that will not degrade the total current consumption of the whole transceiver (this is related to the overall transceiver's power budget).

The design of this PA was bounded by some constraints. First, a limited

number of components were available that were completely modelled up to 10GHz. Since modeling is a crucial factor for RF frequency operation, only this limited set of transistors, inductors, and capacitors were used. The input to the power amplifier is the output of the voltage-controlled oscillator (VCO). In order to avoid the effect of loading the VCO and causing frequency pulling, a buffer stage acts as the first stage in the PA implementation. The schematic of the buffer stage is shown in Figure 5.2. The buffer requires a biasing current of 0.4mA, and a bias voltage of 1.5V. Both are applied externally.
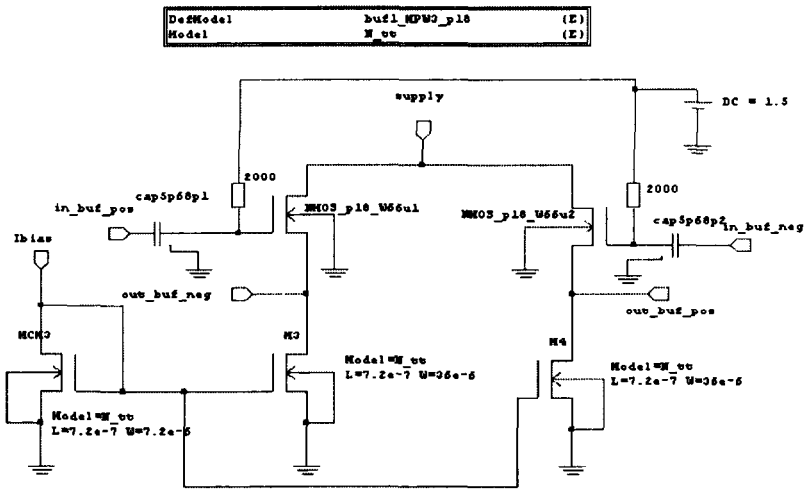

Figure 5.2. The schematic of the buffer stage.

The output stage of the PA (shown in Figure 5.3) is biased at 12mA in order to deliver 4dBm to the Antenna. A differential configuration is employed since the PA is integrated with the complete transceiver.   In order to achieve class A operation, the output transistor is biased at mid supply, A resistor (20-Ohm) is inserted between the inductor (9.3nH), and ac-bypassed by C (5.56pF) as shown in Figure 5.3, the resistor helps stabilize the bias condition.

The complete PA schematic is shown in Figure 5.4. Simulations were done using the APLAC simulator. All components used are represented by their complete models according to the documentation for the 0.18μ technology. An example of the simulated results is shown in Figure 5.5-Figure 5.6. Figure 5.5 shows the harmonic content of the output signal at typical operation. The output power at the third harmonic is around 58dB below the fundamental, and in case of ideal differential operation, the second harmonic is neglected.

Figure 5.6 shows the variation of the output signal versus the input signal for both the fundamental component, and the third harmonic. The distortion level is also plotted. The amplifier is highly linear at the expense of efficiency.
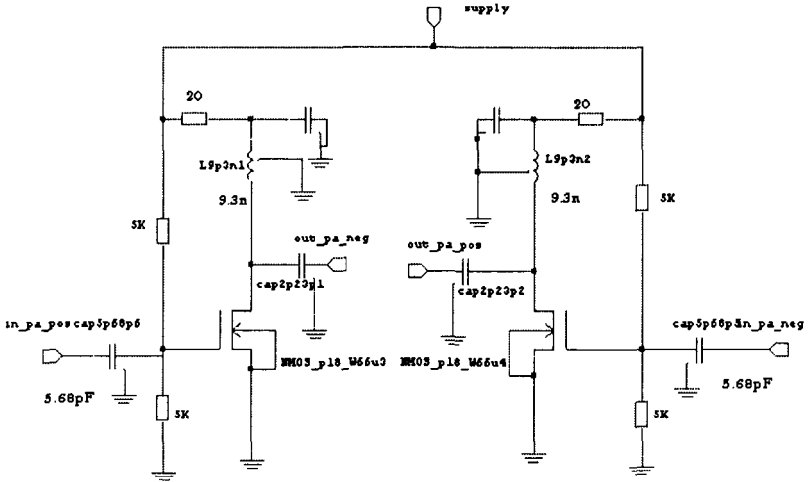
Figure 5.3.   The Schematic of the class A output stage.
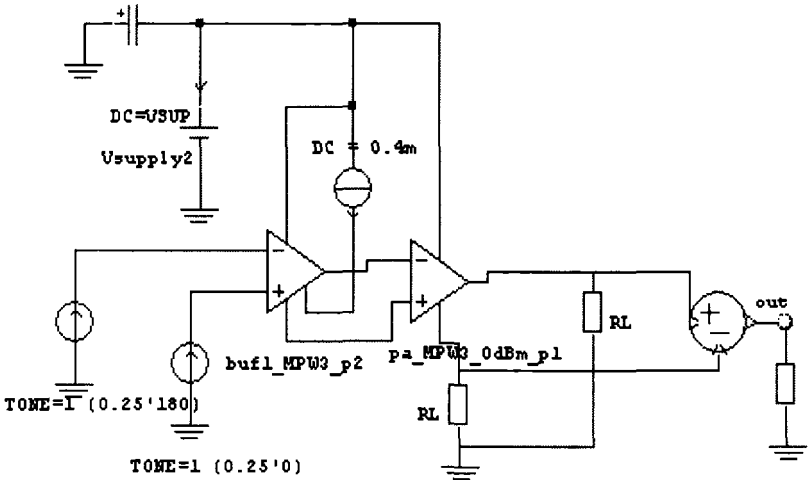
Figure 5.4.   The Block diagram of 0 dBm power amplifier.

An estimation of the distortion level indicates that it does not exceed 0.15%.

This is a complete integrated solution with all components included on-chip. It has been possible through the use of triple well, 6 metal layer, 0.18μm CMOS technology. The inductors available through this technology are implemented using the highest metal layer (metal 6), and can achieve a relatively high quality factor from 8 to 10. A complete model of all passive components enables close prediction of the circuit performance. The layout of the chip is shown in Figure 5.7.

In order to implement the optional control from 0dBm to 4dBm, a variable gain amplifier (VGA) is implemented as shown in Figure 5.8 [55]. The VGA is to be inserted between the buffer stage and the output stage shown in Figure 5.4. The gain can be varied through changing the ratio of the load resistance to R_{gain}, which can be implemented as a MOS transistor in the triode region with its gate voltage acting as the control voltage (Vcontrol). Simulations results showing the variation of the output power and the third harmonic power versus the control voltage (Vcontrol) are given in figure 5.9.
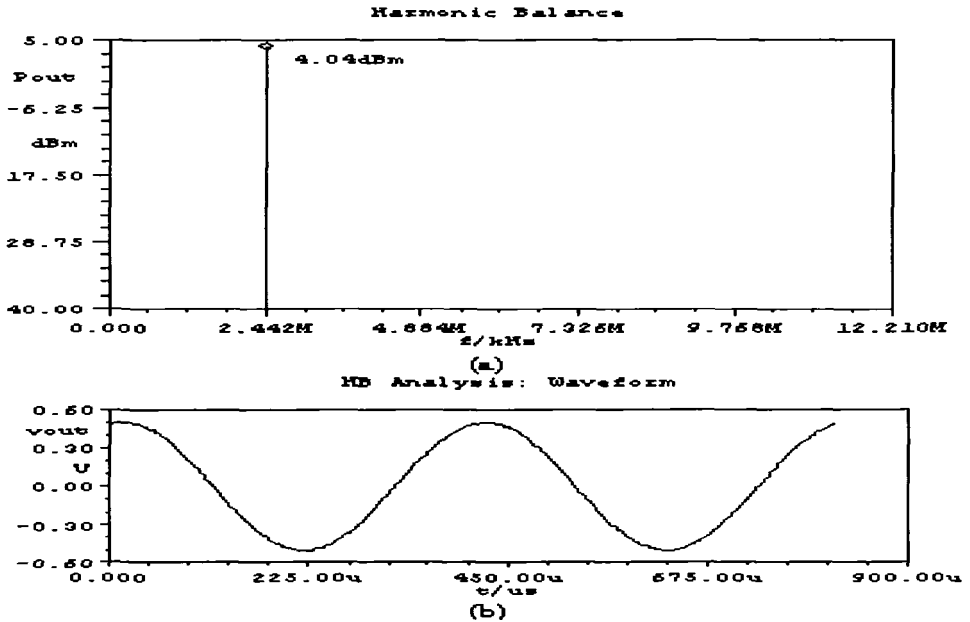
Figure 5.5. Simulation results of the harmonic content of the PA.

2. A Class 1 Bluetooth PA in $0.18\mu m$ CMOS

Implementing a 20dBm PA in $0.18\mu m$ CMOS technology is a major challenge. In fact, there has been no reported power amplifier below $0.2\mu m$ CMOS technology. Although such a deep sub-micron technology is not an attractive choice to the PA, performance-wise, a CMOS PA implemented in the same technology as the rest of the transceiver, would provide huge cost benefits, even if it is not to be integrated with it on the same die.

Designing a PA in $0.18\mu m$ CMOS technology faces 2 major issues: high knee voltage (pinch Ũoff) voltage of the I-V curve, and low oxide breakdown voltage (For this specific technology it is $1.1*1.8 = 1.9V$).

A Class AB amplifier is used for the implementation of the class 1 Blue-
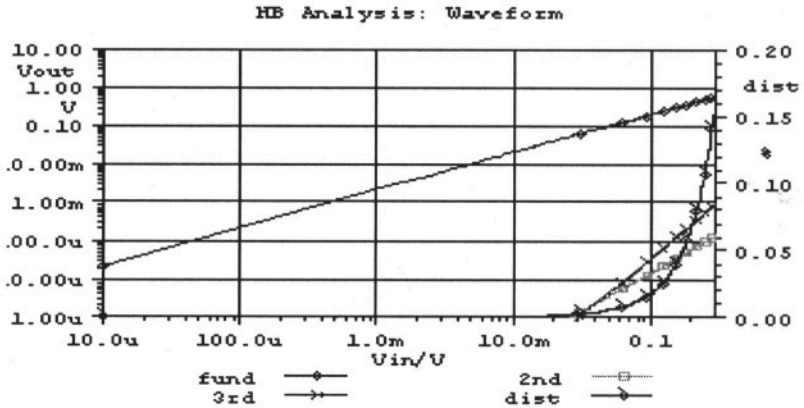
Figure 5.6. The variation of the output voltage at the fundamental frequency, second, and third harmonics, and the distortion level versus the input voltage.
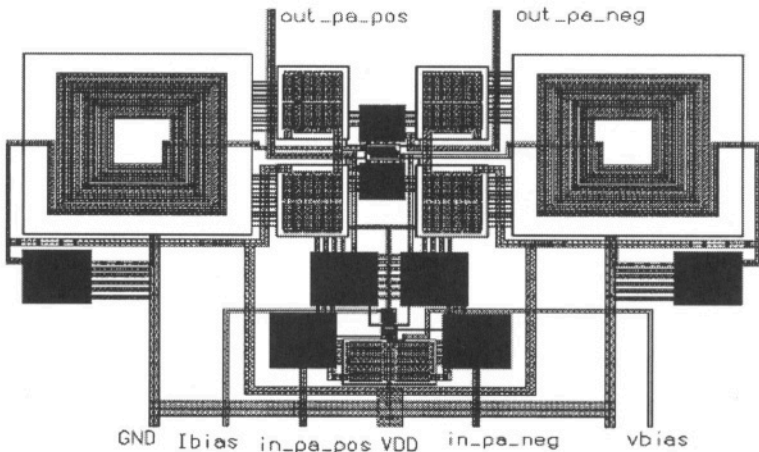
Figure 5.7. The layout of class 3 power amplifier to be connected to the VCO in the Bluetooth transmitter chain.

tooth amplifier. As mentioned earlier, using such a linear class of operation would enable using the amplifier for more applications targeting the same band (2.4GHz-2.48GHz), and thus the implementation of a Multi-mode amplifier. Although class AB relaxes the requirements on the breakdown voltage, the supply is limited to such a low value that using a single transistor amplifier as discussed in section 4.2 becomes impossible. Such a low supply demands low impedance level at the output, especially when package parasitics are considered. In order to boost the supply voltage, a cascode configuration , utilizing a thick gate transistor(operating at 3.3V) is used. Most available CMOS
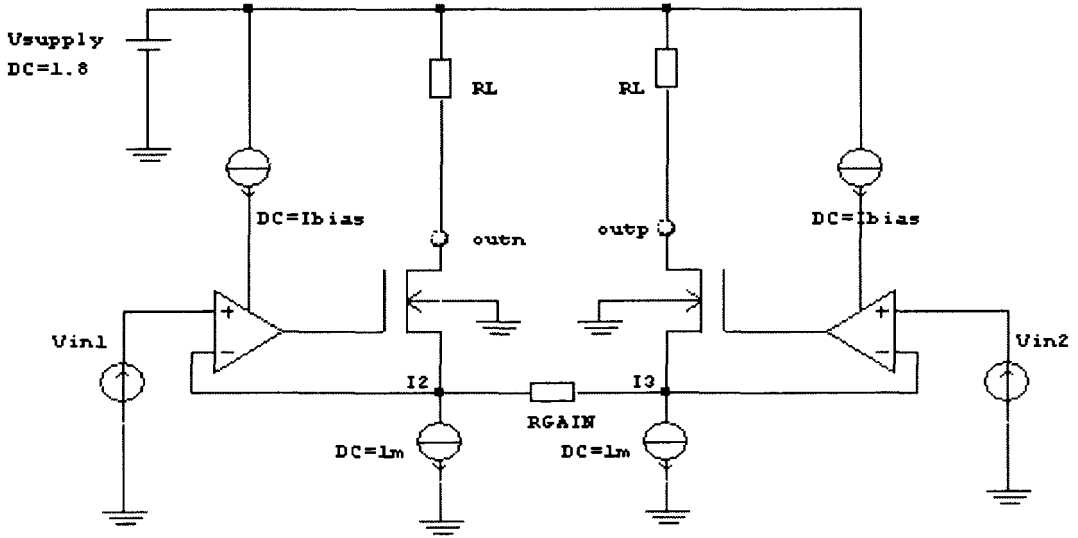
Figure 5.8. Simplified schematic of the VGA employed in a class 2/3 Bluetooth amplifier.
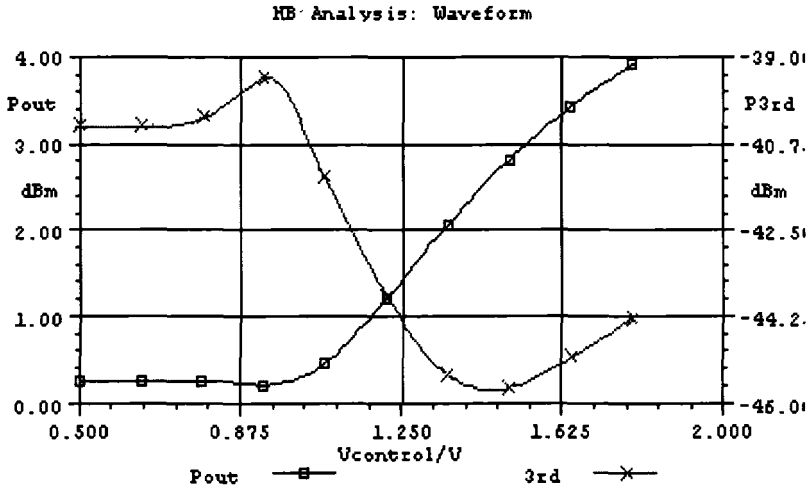
Figure 5.9. Simulation results of class 2 Bluetooth PA

technologies provide this added option of 3.3V transistors in deep sub-micron technologies to be used in the implementation of the I/O pads. Thus, this is not considered an added fabrication step.

Although using a 3.3V transistor would enable higher output power, and more reliability, it will affect the efficiency level of the PA. Besides increasing the current consumption, and having to support two supplies rather than one,

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vdd1	First supply voltage	1.6	1.8	2	V
Vdd2	Second supply voltage	3	3.3	3.6	V
I_{bias1}	Bias current		1		mA
I_{bias2}	Bias current		1.1		mA
T	Temperature	-30	27	85	°C

Table 5.1.   DC operating conditions

the cascode transistor in the output stage acts as a resistor in series with the main amplifier, thus lowering the expected efficiency.

The design of the PA proceeds as in section 4.2. The class AB output stage is designed first such that it is capable of delivering more than 20dBm, assuming that around 2dBm of power will be lost due to the effect of the board, and package. The cascode transistor is made as wide as possible to satisfy the compromise of having lower resistive effect, and at the same time, a reasonable drain capacitance at the output node that can be absorbed by a realizable inductance value.

The same steps of determining the optimum load are used. The first stage is designed to provide adequate gain to drive the output stage. The interstage-matching network is completely implemented on chip due to the availability of characterized inductors. Figure 5.10 shows the core of the amplifier consisting of gain stage, output class AB stage, and the bias circuit. It is worth noting that biasing is implemented using current rather than voltage to keep the parameters of the amplifier as constant as possible with temperature and process variation. A shutdown switch is also added.

After adding the effect of the pads and the bond-wire inductances, the stability of the amplifier was greatly affected. Several resistances were added to bring the k-factor above 1 for all frequencies. The core of the amplifier, together with the bond-wires, pads, and input-output matching are shown in Figure 5.11.

3.   Simulations Results

The amplifier has been tested under typical, fast, and slow processes in order to guarantee its full functionality. The dc operating conditions under which the amplifier is tested are shown in Table 5.1, and the input signal level, and frequency are shown in Table 5.2.
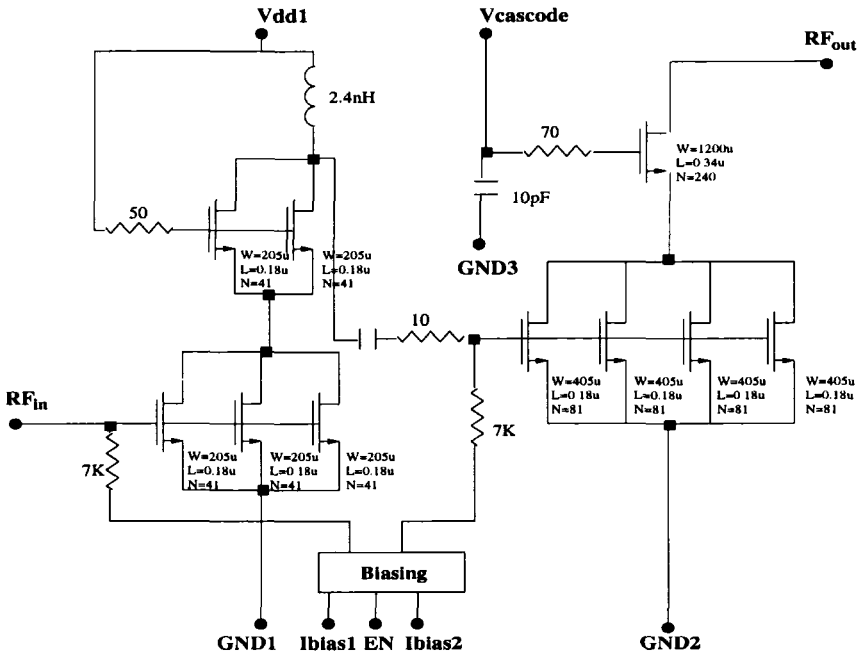
Figure 5.10. The schematic of the core of the class AB power amplifier.
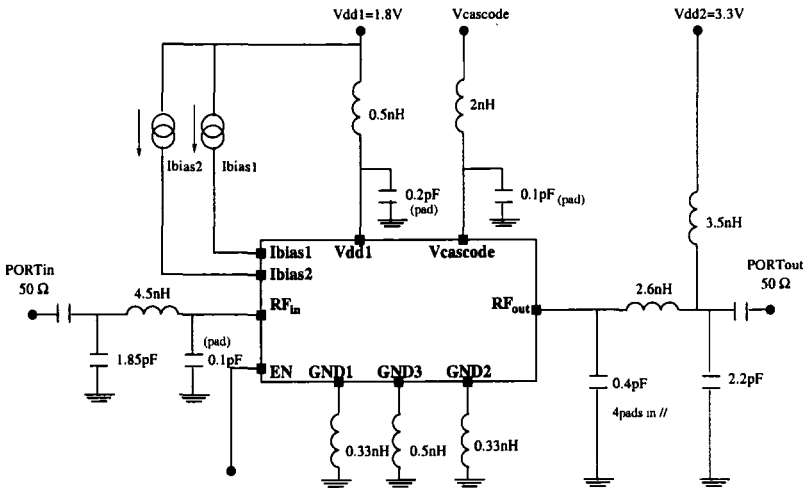

Figure 5.11. Power amplifier test setup.

3.1 Large Signal Simulations

The power amplifier is tested for satisfying the required output power within the band of interest by applying an input power signal of 4dBm, and measuring

Symbol	Parameter	Min.	Typ.	Max.	Unit
Pin	Input Power		4		dBm
F	Operating frequency	2.4		2.482	GHz

Table 5.2.   Input signal parameters

the output power at the 50-Ohm port. Figure 5.12 shows the variation of output power and efficiency versus the input signal frequency.

In order to test the linearity of the power amplifier, the input signal power is swept from -16dBm to 4dBm, and both the output power, and efficiency are plotted as a function of the input power in Figure 5.13. Figure 5.13 also shows the variation of the large signalgain as a function of input power. The PA gain drops from 31dB at small signal to reach 18.4dB at 4dBm input power.

The level of input, and output matching is also dependent on the input power. In fact, variation in input power will cause a shift in the level, and frequency of the matching point. The large signal input and output matching were tested at input power of 4dBm using Harmonic Balance Simulations, in a way similar to its measurement technique using the network analyzer. The input and output impedances are measured by applying a signal of known amplitude, and measuring the input and output currents when the other port is matched. Using the equations relating the S-parameters to the Z-parameters, S_{11}, and S_{22} are plotted as a function of frequency as shown in Figure 5.14. Table 5.3 summarizes the results of harmonic balance simulations at different process Corners.
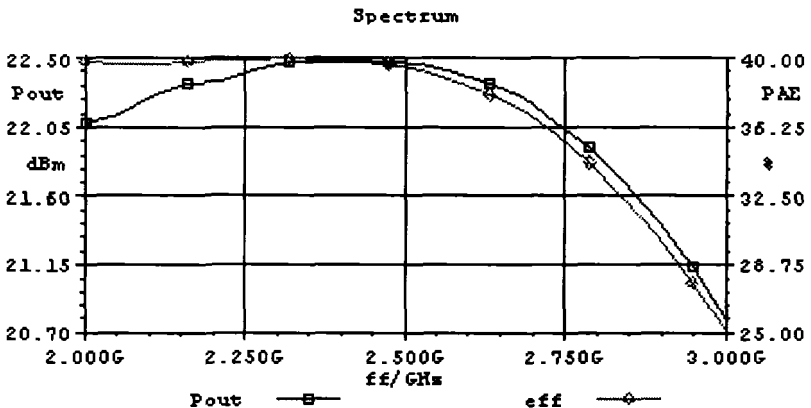

Figure 5.12.   The variation of output power, and PAE as a function of the input signal frequency.
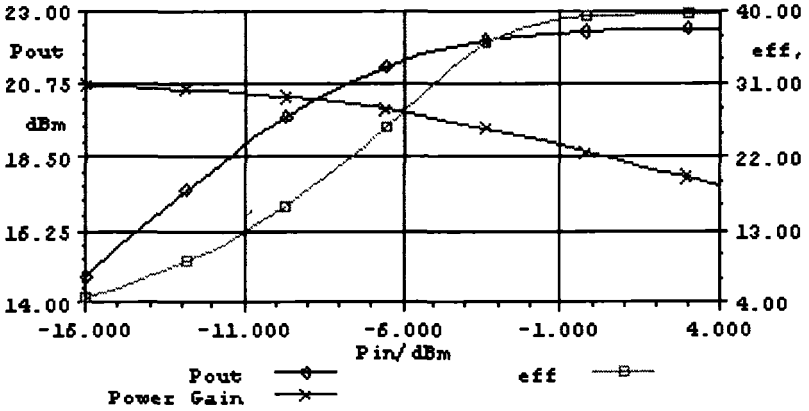
```
23.00                                              ⊟  40.00
Pout                                                   eff,
20.75                                                  31.00
dBm
18.50                                                  22.00

16.25                                                  13.00

14.00                                                  4.00
      -16.000   -11.000   -6.000   -1.000   4.000
                        Pin/ dBm
            Pout  ──◆──           eff   ──⊟──
       Power Gain  ──✕──
```

Figure 5.13. The variation of output power, and PAE, and power gain versus input power.

PA Input Impedance

```
300.0                                              0.00
Z/ Ohm                                             S11
200.0                                              -5.00

100.0                                              dB

0.00                                               -10.0

-100.0                                             -15.0

-200.0                                             -20.0
     2.200G   2.300G   2.400G   2.500G   2.600G
                        ff
         Re(Zin)  ──◆──        Im(Zin)  ──✕──
          S11     ────
```

(a)

PA Output Impedance

```
300.0                                              0.00
Z/ Ohm                                             S22
200.0                                              -5.00

100.0                                              dB

0.00                                               -10.0

-100.0                                             -15.0

-200.0                                             -20.0
     2.200G   2.300G   2.400G   2.500G   2.600G
                        ff
        Re(Zout)  ──◆──        Im(Zout)  ──⊟──
          S22     ──✕──
```

(b)
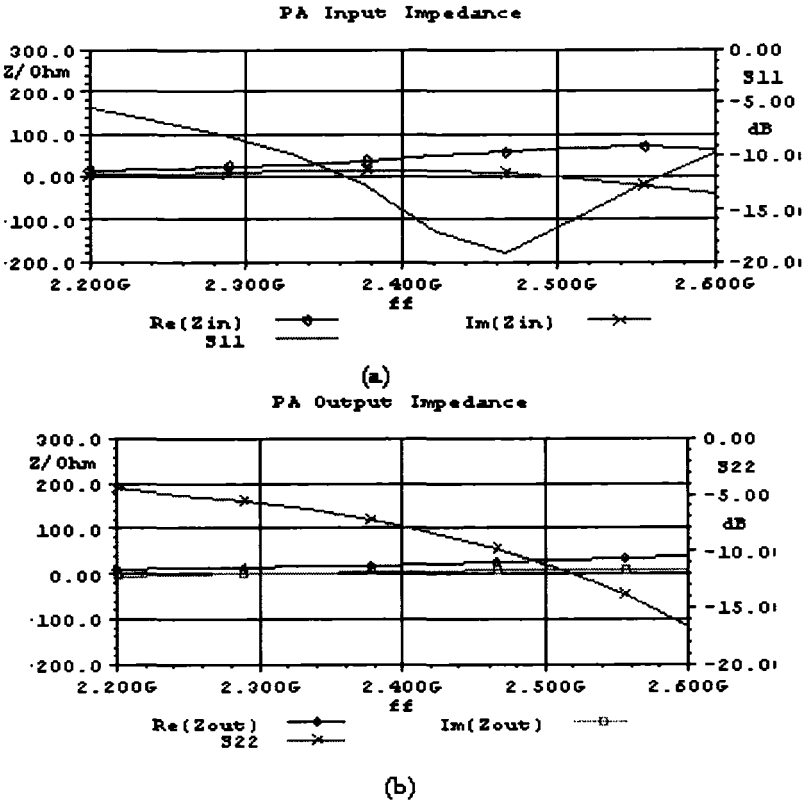
Figure 5.14. The input and output matching.

process	Ibias	Vdd	Temp	Pout	PAE	2f,3f	I_{sup1}	I_{sup2}
	(μA)	(V)	(C)	(dBm)	(%)	(dBc)	(mA)	(mA)
Typ.	200	1.8,3.3	27	22.5	39.7	-27,-39	113	41
Slow	200	1.6,3	85		27	-35, -42	74	27
Slow	200	1.6, 3	-30	19.7	33	-36, -42	80	29.5
fast	200	2,3.6	85	22.54	25	-28,-49	143	55
fast	200	2,3.6	-30	23	30.3	-28,-38	148	54

Table 5.3.   Harmonic-Balance and process corner simulations

3.2   Power Control

The output power can be controlled through the variation in the bias voltage applied to the cascode transistor in the output stage. It is worth noting that since the supply voltage in the output stage is higher than that of the first driver stage, controlling the gain of the driver stage can not bring the output power to low levels since the gain of the second stage is much higher. In order to have a wide range of output power variation, the biasing of the cascode transistor can be changed, thus changing the loading on the main amplifier, and therefore changes the output power, and efficiency. In order to achieve specific control steps, a Digital to Analog Converter (DAC) has to feed the cascode bias pin. Figure 5.15 shows the variation in output power, and efficiency versus the cascode voltage bias. Using the same technique of varying the width of the main amplifier in the output stage as discussed in section 4.2, has shown many stability issues compared to this technique.
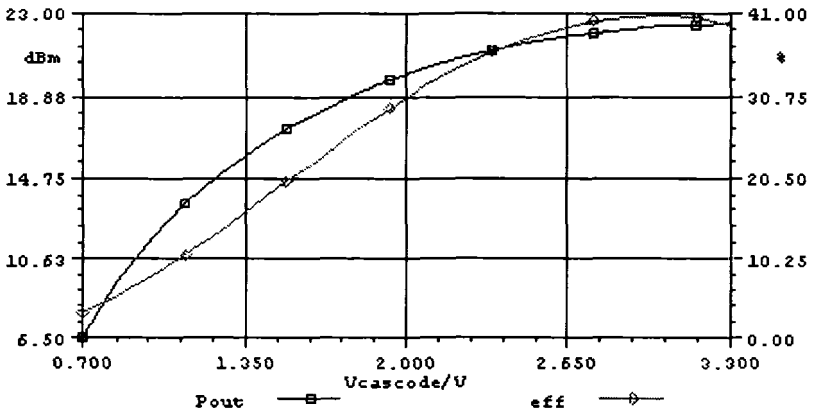

Figure 5.15.   Variation of output power and efficiency versus the cascode bias voltage.

process	Ibias(μ)	Vdd(V)	Temp (C)	S_{21}(dB)	S_{11} (dB)	S_{12} (dB)	G_{var}(dB)
Typ.	200	1.8,3.3	27	31.3	-45	-50	1
Slow	200	1.6,3	85	20.7	-12	-50.4	1.1
Slow	200	1.6, 3	-30	24	-14	-48	0.5
fast	200	2,3.6	85	29.2	-24	-42	0.9
fast	200	2,3.6	-30	32.6	-21	-43.6	0.8

Table 5.4. Small signal S-parameter variation with process corner and temperatures

3.3 Gain and Matching

large signalS-parameter simulations are performed to optimize the input matching. The power amplifier is not required to provide S_{22} below -10dB since it is usually matched for maximum output power and not maximum gain.

Input matching is provided by a series inductor and a shunt capacitor. The series inductor can be implemented using bond-wires. The complete matching network can be implemented totally on chip provided that more inductors are available in the library provided by the foundry. Table 5.4 summarizes the results of small signal s-parameter simulations at different process Corners.

3.4 Stability

The stability of the power amplifier has been checked using s-parameter (small signal simulations). It is determined by K, and Δ parameters[31], or the more recent μ factor. For the amplifier to be unconditionally stable, K has to be larger than 1, and simultaneously Δ smaller than one, or μ larger than 1. The amplifier has been tested for all frequencies. Small resistors have been added to the input, output, and the gates of the cascode transistors. The stability of the power amplifier is very much dependent on the ground inductance. In simulations, a 0.33nH (Three 1nH inductors connected in parallel) is assumed. If the ground inductance increases above this value, stability, and output power will be affected. If the amplifier is redesigned to be unconditionally stable for ground inductances above this value, the efficiency will be greatly sacrificed. Figure 5.16 shows the variation of the stability parameters with frequency.

4. Conclusion

A Power amplifier for Bluetooth standards has been implemented in 0.18μm CMOS process. The amplifier is capable of delivering 22.5dBm of maximum output power to a 50-Ohm load. This amplifier operates at class AB mode,

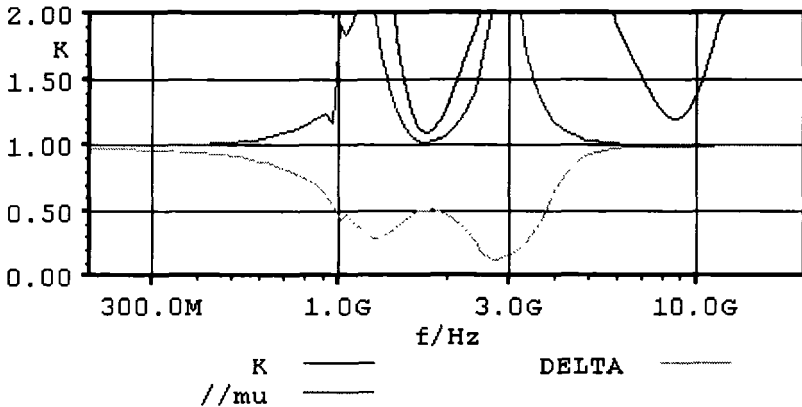*Figure 5.16.* Stability of the power amplifier (K >1 μ>1, and Δ < 1).

Symbol	Parameter	Min.	Typ.	Max.	Unit
Pout	Output Power	19.5	22.5	23	dBm
PAE	Power added efficiency at maximum power	25	39.7	39.7	%
G_{var}	Gain variation within band	0.8	1	1.1	dB
S_{21}	gain	12	18	20	dB
S_{11}	Input Matching	-12	-19		dB
$I_{supply1}$	Current consumption first supply	27	31	55	mA
$I_{supply2}$	Current consumption second supply	74	113	148	mA
2f, 3f	Harmonics	-27, -39	-27, -39	-36, -42	dBc

Table 5.5. Summary of simulated electric characteristics

thus it can be easily linearized to satisfy IEEE802.11 DSSS requirements. The amplifier requires a minimum number of external components, and occupies an area of 0.65mmx0.65mm, which is the least reported area in PA design. It is also the highest reported operating frequency using CMOS technology. The layout of the PA is shown in Figure 5.17. A summary of the most important simulated electrical characteristics is given in Table 5.5.

5. Summary

The implementation of two power amplifiers in 0.18μm CMOS technology has been discussed. The first PA targets class 3 Bluetooth transmission, and can be extended to cover both class 2, and 3 by adding a variable gain amplifier as a preceding stage. The second PA targets class 1 Bluetooth operation, and can be controlled down to 4dBm.The challenges of operating at deep sub-micron technologies, and with such low supply voltages have been presented. Finally

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Chapter 6

CONCLUSION

Considerations of cost, form factor, and power have motivated strong interest in monolithic CMOS transceivers. This work addresses the requirements, and challenges of realizing an efficient PA with the minimum number of external components in standard CMOS technology.

Applications employing two frequency bands are considered. A switching class-E 900MHz CMOS power amplifier is presented. The amplifier is implemented in a standard $0.35\mu m$ CMOS process. Measurement results from a fabricated prototype show that it is capable of delivering 24dBm of output power to a 50-Ohm load with maximum efficiency of 48% using a 2V supply. An output matching capacitor, and an input matching inductor are the only external components used, in addition to board traces acting as inter-stage and dc-feed inductors. The implementation and design aspects for realizing a dual mode/dual band PA are discussed. Implementing two standards having different output power levels, together with different frequency bands would result in performance degradation in the case of the lower output power standard. On the other hand, having Multi-band operation is possible using the same supply voltage, input power, but varying the input, and output matching, together with the inter-stage matching. A 1.9GHz power amplifier that uses the same core of the fabricated 900 MHz amplifier, with the slight variation in the drain capacitance to account for the different frequency bands, is presented. Thus proving that the same amplifier core can be utilized at a different frequency band, without sacrificing performance provided that the level of output power is preserved.

In order to target higher frequency applications, This work presents the design and implementation of a broadband radio-frequency power amplifier in a standard CMOS technology for short-range wireless applications. The amplifier is implemented in a standard $0.35\mu m$ triple metal CMOS process. The

amplifier is capable of delivering a maximum output power of 16.6dBm at 1.91GHz, and of 16dBm at 2GHz using a 3.3V supply with an overall measured power added efficiency (PAE) of 33%. The power amplifier employs a class AB output stage, which represents a compromise between efficiency and Linearity. A new technique based on switching a number of semi-cascode stages is used to control the output power in 2dB steps. By utilizing more accurate transistor models, the same concept can be extended to higher frequency applications such as Bluetooth radios, which use a controllable 20dBm transmitter. Operating at class AB, the power amplifier is relatively linear, and simple linearization techniques can be employed to make it suitable for non-constant envelope modulation standards.

A power amplifier for Bluetooth standards has been implemented in $0.18\mu m$ CMOS process. The amplifier is capable of delivering 22.5dBm of maximum output power to a 50-Ohm load. This amplifier operates at class AB mode, thus it can be easily linearized to satisfy more standards in the 2.4GHz-2.5GHz ISM band. The amplifier requires a minimum number of external components, and occupies an area of 0.65mmx0.65mm, which is the least reported area in CMOS power amplifier design. It is also the highest reported operating frequency in CMOS technology for power amplifiers . A 0dBm-4dBm PA is also presented, which when utilized with the 20dBm PA can present a complete Bluetooth transmitter solution. Issues related to integration are discussed as well.

With the trend moving towards lower power-class (20dBm-24dBm) transmitters in next generation wireless standards, the results achieved in this work present a step towards showing that CMOS PAs with good efficiencies are realistic despite steadily declining FET breakdown voltages.

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