Helsinki University of Technology
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Direct Digital Synthesizers: Theory, Design and Applications

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Preface

What has been will be again, what has been done will be done again; there is nothing new under the sun.

Ecclesiastes 1:9

This study was carried out at the Electronic Circuit Design Laboratory of the Helsinki University of Technology between 1996 - 2000.

I would like to express my thanks to Professor Veikko Porra, who initially introduced me DDS research.

I wish to express my sincere gratitude to Prof. Kari Halonen for providing the opportunity to carry out this study, and for guidance and support. I am also very grateful to all my colleagues at the Electronic Circuit Design Laboratory. I extend my warmest thanks especially to Marko Kosunen, Johan Sommarek and Mikko Waltari. Our secretary, Mrs. Helena Yllö, deserves special thanks for her kind help on various practical problems.

A significant part of this work was done in projects funded by the Technology Development Center (Tekes) and the Academy of Finland. Personal grants were received from the Nokia Foundation, Jenny and Antti Wihuri Foundation, Technology Development Foundation, Electronic Engineering Foundation, Sonera Foundation, IEEE Solid State Society Predoctoral Fellowship, the Finnet Foundation, and Foundation of Helsinki University of Technology.

My friends outside the field of engineering have kept me interested in matters other than just electronics. I have spent very relaxing moments with my friends taking part in different activities such as jogging, icewater swimming, hanging out in bars and so on, and hopefully will continue to do so.

Finally, my warmest thanks go to my parents, Eila and Eero Vankka, who have constantly encouraged me to study as much as possible, and given me the opportunity to do so.

Helsinki, October 26, 2000

Jouko Vankka

Abstract

Traditional designs of high bandwidth frequency synthesizers employ the use of a phase-locked-loop (PLL). A direct digital synthesizer (DDS) provides many significant advantages over the PLL approaches. Fast settling time, sub-Hertz frequency resolution, continuous-phase switching response and low phase noise are features easily obtainable in the DDS systems. Although the principle of the DDS has been known for many years, the DDS did not play a dominant role in wideband frequency generation until recent years. Earlier DDSs were limited to produce narrow bands of closely spaced frequencies, due to limitations of digital logic and D/A-converter technologies. Recent advantages in integrated circuit (IC) technologies have brought about remarkable progress in this area. By programming the DDS, adaptive channel bandwidths, modulation formats, frequency hopping and data rates are easily achieved. This is an important step towards a "software-radio" which can be used in various systems. The DDS could be applied in the modulator or demodulator in the communication systems. The applications of DDS are restricted to the modulator in the base station. The aim of this research was to find an optimal front-end for a transmitter by focusing on the circuit implementations of the DDS, but the research also includes the interface to baseband circuitry and system level design aspects of digital communication systems.

The theoretical analysis gives an overview of the functioning of DDS, especially with respect to noise and spurs. Different spur reduction techniques are studied in detail. Four ICs, which were the circuit implementations of the DDS, were designed. One programmable logic device implementation of the CORDIC based quadrature amplitude modulation (QAM) modulator was designed with a separate D/A converter IC. For the realization of these designs some new building blocks, e.g. a new tunable error feedback structure and a novel and more cost-effective digital power ramp generator, were developed.

Keywords: Direct Digital Synthesizer, Numerically Controlled Oscillator, GMSK Modulator, Quadrature Amplitude Modulation, and CORDIC algorithm

Table of Contents

List of Abbreviations

AC	Alternating current
ACP	First adjacent channel power
ADC	Analog-digital-converter
AFC	Automatic frequency control
ALT1	Second adjacent channel power
ALT2	Third adjacent channel power
ASIC	Application specific integrated circuit
BiCMOS	Bipolar complementary metal-oxide-semiconductor
BPF	Bandpass filter
CDMA	Code division multiple access
CIA	Carry increment adder
CICC	Custom integrated circuits conference
CLB	Configurable logic block
CLK	Clock
CMFB	Common-mode feedback
CMOS	Complementary metal-oxide-semiconductor
CORDIC	Co-ordinate digital computer
CPM	Continuous phase modulation
CSD	Canonic signed digit
CSFR	Constant scale factor redundant
D/A	Digital to analog
DAC	Digital to analog converter
dB	Decibel
dBc	Decibels below carrier
DCML	Differential current mode logic
DCORDIC	Differential CORDIC
DCS	Digital cellular system
DCT	Discrete cosine transform
DDFS	Direct digital frequency synthesizer
DDS	Direct digital synthesizer
DFF	Delay-flip-flop
DFT	Discrete Fourier transform
DL	Downlink
DNL	Differential non-linearity
DPCCH	Dedicated physical control channel
DPDCH	Dedicated physical data channel
DPSK	Differential phase-shift keying
DSP	Digital signal processing
ECL	Emitter coupled logic

EDGE	Enhanced data rates for global evolution
EF	Error feedback
ETSI	European telecommunications standards institute
EVM	Error vector magnitude
FCC	Federal communications commission
FFT	Fast Fourier transform
FH	Frequency hopping
FIR	Finite impulse response
FPGA	Field programmable gate array
GaAs	Gallium arsenide
GCD	Greatest common divisor
GMSK	Gaussian minimum shift keying
GSM	Groupe spécial mobile
HDL	Hardware description language
HPF	High-pass filter
IC	Integrated circuit
IEE	Institution of electrical engineers
IEEE	Institute of electrical and electronics engineers
IEICE	Institute of electronics, information and communication engineers
IF	Intermediate frequency
IIR	Infinite impulse response
INL	Integral non-linearity
ISI	Inter-symbol interference
ISM	Industrial, scientific and medicine
ISSCC	International solid-state circuits conference
L-FF	Logic-flip-flop
LE	Logic element
LMS	Least-mean-square
LO	Local oscillator
LPF	Low-pass filter
LSB	Least significant bit
LUT	Look-up table
MFSK	M-ary frequency-shift keying
MSB	Most significant bit
MSD	Most significant digits
NCO	Numerically controlled oscillator
OSC	Oscillator
P/F	Phase/frequency detector
PA	Power amplifier
PLD	Programmable logic device
PLL	Phase-locked loop

PN	Pseudo random
PPM	Part per million
QAM	Quadrature amplitude modulation
QDDS	Quadrature direct digital synthesizer
QPSK	Quadrature phase-shift keying
RF	Radio frequency
RMS	Root-mean-square
RNS	Residue number system
ROM	Read-only memory
RZ	Return-to-zero
SFDR	Spurious free dynamic range
Si. Bip.	Silicon bipolar
SIR	Signal-to-interference ratio
SNR	Signal-to-noise ratio
SS	Spread spectrum
TDD	Time division duplex
TDMA	Time division multiple access
TEKES	Technology development center
VCO	Voltage controlled oscillator
VHDL	Very high speed integrated circuit HDL
VLSI	Very large scale integration
WCDMA	Wideband code division multiple access
XOR	Exclusive or

List of Symbols

A	rotated angle, signal amplitude
a	weighting factor
$A(n)$	amplitude modulation
a_n	input symbol
Ang	total rotation angle after N CORDIC iterations
b	fractional bits, weighting factor
B	number of bits per pipelined stage
$B\,T_{sym}$	relative bandwidth of Gaussian filter in GMSK-modulation
b_i	FIR filter coefficients
c	fractional bits, weighting factor
C	phase accumulator output at moment of carry generation
C_n	carrier frequency control word
dc	dc offset
e_{A}	finite precision of sine samples stored in sine ROM
E_c	lowpass channel energy
$\mathrm{e}_{\mathrm{COM}}$	distortion from compressing sine ROM
e_{DA}	digital-to-analog conversion error
e_{F}	post-filter error
e_{FI}	truncation of ideal frequency path response of LUT
e_{FO}	finite word length output of LUT
$e_{\max}$	worst-case truncation error
e_P	truncation of phase accumulator bits addressing sine ROM
E_s	stopband energy
f	word length of phase error
f_0	desired frequency in cycles per second
f_b	lowpass channel's cut-off frequency
f_c	carrier frequency
f_{clk}	clock frequency
f_{ea}	largest allowed frequency error
f_d	maximum frequency deviation
f_g	gating rate
f_{LO}	output frequency of local oscillator
f_{min}	smallest frequency
f_{out}	output frequency
f_{ref}	reference frequency of PLL
F_s	sampling frequency
f_{sym}	symbol rate

G_n	gain
H	constant
$h(t)$	output of sample-and-hold, Gaussian filter
hr	receive filter
I	in-phase component
I_1	bit current
j	number of accumulator bits
J	integer
$J_i(\beta)$	Bessel functions of first kind
K	proportional constant
k	word length of phase accumulator output used to address ROM, index variable
$K(N)$	scaling factor in CORDIC algorithm
k_n	conversion factor
L	period of dither source
L_n	frequency modulation control word
m	word length of values stored in sine ROM, index variable
M	over-sampling ratio, division ratio
$\mathrm{m}(t)$	original modulated signal
n	index variable
N	total numbers of iterations in CORDIC algorithm, division ratio
n_c	center tap
n_{clk}	phase noise of clock frequency
N_{cs}	number of carriers generated digitally
$outw$	multiplier input width
$\Delta\mathrm{P}$	phase increment word
P	numerical period of phase accumulator sequence
$P(n)$	phase modulation, phase register value
P_A	signal power
PE	period of phase truncation error
Pe	numerical period of phase accumulator output sequence
PM	phase modulation word
$P_{\max}$	maximum acceptable spur power
PS	number of pipelined stages
q	index variable
Q	quadrature component
r	constant
R	$N \times N$ matrix
S	number of samples
S_l	$N \times K$ matrix
$\mathrm{sw}(t)$	periodical switching signal

T_b	burst length
T_r	ramp duration
T_{sym}	symbol duration
$v(t)$	sampled waveform
V_{CM}	common-mode input voltage
v_d	differential input voltage
V_{out}	output voltage
V_T	threshold voltage
W	$N \times N$ matrix
w	number of symbol stages in shift register
y	digital delay generator input
y_{err}	output error sequence
x	word length of amplitude error
z_A	amplitude dither
z_{HA}	high-pass filtered amplitude dither
z_{HP}	digital high-pass filtered dither signal
z_n	error due to angle quantization
z_P	phase dither
β	maximum value of phase deviation
ξ	damping factor
Λ	number of discrete spurs due to phase truncation
α	roll-off factor
Δ	quantization step size
ε	total phase truncation noise after phase dithering
φ_0	initial phase offset
$\Omega(t/T)$	unit rectangular pulse of duration T
Δ_A	amplitude quantization step size
ω_{BB}	baseband signal frequency
ω_{clk}	clock frequency of DDS
ϕ_{e1}	phase mismatch between I and Q
ϕ_{e2}	phase mismatch between I and Q LO signals
Δf	frequency error
Δf	frequency resolution
β_F	forward current gain of transistor
ω_m	offset frequency
θ_{min}	smallest phase value
ω_N	natural frequency of PLL loop
ω_{out}	output frequency of DDS
$\Delta P(n)$	frequency modulation
$*$	convolution

1. Introduction

1.1 Motivation

A major advantage of a direct digital synthesizer (DDS) is that its output frequency, phase and amplitude can be precisely and rapidly manipulated under digital processor control. Other inherent DDS attributes include the ability to tune with extremely fine frequency and phase resolution, and to rapidly "hop" between frequencies. These combined characteristics have made the technology popular in military radar and communications systems. In fact, DDS technology was previously applied almost exclusively to high-end and military applications: it was costly, power-hungry, difficult to implement, and required a discrete high speed D/A converter. Due to improved integrated circuit (IC) technologies, they now present a viable alternative to analog-based phase-locked loop (PLL) technology for generating agile analog output frequency in consumer synthesizer applications.

It is easy to include different modulation capabilities in the DDS by using digital signal processing methods, because the signal is in digital form. By programming the DDS, adaptive channel bandwidths, modulation formats, frequency hopping and data rates are easily achieved. The flexibility of the DDS makes it ideal for signal generator for software radio. The digital circuits used to implement signal-processing functions do not suffer the effects of thermal drift, aging and component variations associated with their analog counterparts. The implementation of digital functional blocks makes it possible to achieve a high degree of system integration. Recent advances in IC fabrication technology, particularly CMOS, coupled with advanced DSP algorithms and architectures are providing possible single-chip DDS solutions to complex communication and signal processing subsystems as modulators, demodulators, local oscillators (LOs), programmable clock generators, and chirp generators. The DDS addresses a variety of applications, including cable modems, measurement equipments, arbitrary waveform generators, cellular base stations and wireless local loop base stations.

The aim of this research is to find possible applications for DDSs in the radio communication system, where the DDS could be used in modulators and demodulators. The DDS is better suited to base stations than to mobiles, because power consumption is high in the wide output bandwidth DDS. The scaling of the IC technologies constantly reduces power consumption in digital circuitry. The same benefit is, however, not easily achieved in analog circuits. Therefore, the DDS might also be suitable for the mobiles in the future. The applications of DDS are restricted to the modulator in the base station. It follows that spurs and noise are the main concern, not power consumption. The spurious performance is not good in the wide output bandwidth DDS because of analog errors in D/A conversion.

The analog part of the DDS includes a D/A converter and a low pass filter. The DDS is a mixed signal device where sensitive analog blocks must tolerate the distortion from digital rail-to-rail signals. The cross-talk issue must be focused when the integration level increases. Another problem is the limited speed and resolution in D/A conversion. Unfortunately, the development of D/A converters does not keep up with the capabilities of digital signal processing with faster technologies.

1.2 Overview of Work

Three different architectures to implement digital synthesizers are presented: DDS (Chapter 2), indirect digital synthesizer (Chapter 3) and CORDIC algorithm (Chapter 4). The analysis of Chapters 5 to 7 gives an overview of the functioning of DDS, especially with respect to noises and spurs. Three up-conversion possibilities are introduced in Chapter 8: a DDS/PLL hybrid, a DDS/mixer hybrid and a DDS quadrature modulator. In Chapters 9-13 the circuit implementations of the digital synthesizer are introduced. Below is a more detailed description of the different chapters:

In Chapter 2, firstly a description of the conventional DDS is given. It is easy to include different modulation capabilities in the DDS with digital signal processing methods, because the signal is in digital form. Another type of DDS application is the digital chirp generator, used in sweep oscillators. Indirect digital sinusoidal oscillators are presented in Chapter 3.

In Chapter 4 it is seen that circular rotation can be implemented efficiently using the CORDIC algorithm, which is an iterative algorithm for computing many elementary functions [Vol59]. The CORDIC algorithm is studied in detail. The finite word length effects in the CORDIC algorithm are investigated. Redundant implementations of the CORDIC rotator are overviewed.

In Chapter 5 the DDS is shown to produce spurs (spurious harmonics) as well as the desired output frequency. The specifications of the D/A-converter are studied in detail, because the D/A-converter is the critical component in wide bandwidth applications.

In Chapter 6 an investigation into the blocks of the DDS is carried out, namely a phase accumulator, a phase to amplitude converter (conventionally a sine ROM) and a filter. Different techniques to accelerate the operation speed of the phase accumulator are considered. Different sine memory compression and algorithmic techniques and their trade-offs are investigated.

In Chapter 7 a study is made of how additional digital techniques (for example dithering, error feedback methods) may be incorporated in the DDS in order to reduce the presence of spurious signals at the DDS output. The spur reduction techniques used in the sine output direct digital synthesizers are reviewed.

In Chapter 8 three up-conversion possibilities are introduced: a DDS/PLL hybrid, a DDS/mixer hybrid and a DDS quadrature modulator. The basic idea is that the DDS provides only a part of the output signal band, and the up-conversion into higher frequencies is done by analog techniques, because the power consumption and the spurious performance are better in the low output bandwidth DDS. The critical paths of the signal could be accomplished by the DDS, which has the advantages of a fast switching time, a fine frequency resolution and coherent frequency hopping.

In Chapter 9, a DDS with an on-chip D/A-converter is designed and processed in a 0.8 µm BiCMOS. The on-chip D/A-converter avoids delays and line loading caused by inter-chip connections.

In Chapter 10, a quadrature IF frequency synthesizer/modulator IC has been designed and fabricated in a 0.5 µm CMOS. This quadrature IF frequency synthesizer/modulator is intended for use in a wide variety of indoor/outdoor portable wireless applications in the 2.4-2.4835 GHz ISM frequency band. This frequency synthesizer/modulator is capable of frequency and phase modulation. The major components are: a quadrature direct digital synthesizer, digital-to-analog converters and lowpass filters. By programming the quadrature direct digital synthesizer, adaptive channel bandwidths, modulation formats, frequency hopping and data rates are easily achieved.

In Chapter 11, a multi-carrier QAM modulator has been developed and processed in a 0.35 µm CMOS (in BiCMOS) technology. The multi-carrier QAM modulator contains four CORDIC based QAM modulators. Each QAM modulator accepts 13 bits in-phase and quadrature data streams, interpolates them by 16 and up-converts the baseband signal into a selected center frequency. The frequencies of the four carriers can be independently adjusted. The proposed multi-carrier QAM modulator does not use an analog I/Q modulator, therefore, the difficulties of adjusting the dc offset, the phasing and the amplitude levels between the in-phase and quadrature phase signal paths are avoided. The multi-carrier QAM modulator is designed to fulfill the spectrum and error vector magnitude (EVM) specifications of the wideband code division multiple access (WCDMA) system.

In Chapter 12, a CORDIC based QAM modulator has been developed and implemented with programmable logic devices (PLDs). D/A converters were implemented in a 0.5 µm CMOS technology. A conventional QAM modulator with quadrature outputs needs four multipliers, two adders and sine/cosine ROMs. The designed CORDIC based QAM modulator has about the same logic complexity as two multipliers and an adder with the same word sizes. The QAM modulator accepts 12 bits in-phase and quadrature data streams, interpolates them by 16 and up-converts the baseband signal into a selected center frequency. The QAM modulator is designed to fulfill the spectrum and EVM specifications of the WCDMA system.

In Chapter 13, a multi-carrier Gaussian minimum shift keying (GMSK) modulator has been developed and processed in a 0.35 μm CMOS (in BiCMOS) technology. The design contains four GMSK modulators, which generate GMSK modulated carriers at specified center frequencies. Utilization of the redundancy in the stored waveforms reduces the size of the GMSK trajectory look-up-table to less than one fourth of the original size in the modulator. Conventionally, the power ramping and output power level control are performed in the analog domain. A novel digital ramp generator and output power level controller performs both the burst ramping and the dynamic power control in the digital domain. The power control is realized by scaling the ramp curve, which follows a raised cosine/sine curve. The four GMSK modulated signals are combined together in the digital domain. The digital multi-carrier GMSK modulator is designed to fulfill the spectrum and phase error specifications of the GSM 900 and DCS 1800 systems.

1.3 Contributions to Advances in (Science and)* Technology

The purpose of the research project was to find an optimal front-end for a transmitter by focusing on circuit implementations of the DDS, but the research also includes the interface to baseband circuitry and the system level design aspects of digital communication systems. Theory of the DDS is reviewed. New bounds for the CORDIC rotator due to the finite word length effects have been derived in Section 4.3, based on the assumption that the errors are uncorrelated and uniformly distributed. The phase truncation error analysis in [Jen88b] is extended in Section 5.1 so that it includes the worst-case carrier to spur ratio bounds. A new bound for the noise level after the phase dithering has been derived in Section 7.2.2. A novel tunable error feedback structure in the DDS is developed in Section 7.4.2. In Section 11.3.2 a root raised cosine filter was designed to maximize the ratio of the main channel power to the adjacent channels' power under the constraint that the ISI is below 2 %. A novel ramp generator with an output power level controller was developed in Section 13.4.2.

Four ICs, which were the circuit implementations of the DDS, were designed. One PLD implementation of the CORDIC based QAM modulator was designed with a separate D/A converter IC.

The first DDS IC is presented in Chapter 9. The author carried out the system design and acted as project coordinator for this piece of work. Mr. Mikko Waltari designed the D/A-converter and the ROM block. Mr. Marko Kosunen designed the rest of the circuit logic.

The second DDS IC is presented in Chapter 10. The author carried out the system design and simulations. Mr. Marko Kosunen designed the digital part. Mr Lauri Sumanen designed the D/A converter. The low pass filter was based on Mr. Kimmo Koli's work.

* I use parentheses not to offend those who do not classify anything of this work as science.

In Chapter 11, the author carried out the system design and simulations. Mr. Marko Kosunen has designed the digital part and the D/A converter.

In Chapter 12, the PLD implementation of the CORDIC based QAM modulator was carried out. The author carried out the system design and simulations. Mr Lauri Sumanen designed the D/A converter.

The third DDS IC is presented in Chapter 13. All the system design and simulations were performed by the author. Mr. Johan Sommarek designed the digital part of the chip. Mr Jaakko Pyykönen designed the D/A converter.

1.4 Related Publications

Parts from the following publications or manuscripts have been used in this work:

[1] J. Vankka, "Methods of Mapping from Phase to Sine Amplitude in Direct Digital Synthesis," IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control, vol. 44, pp. 526-534, March 1997.

[2] J. Vankka, "A Direct Digital Synthesizer with a Tunable Error Feedback Structure," IEEE Transactions on Communications, vol. 45, pp. 416-420, April 1997.

[3] J. Vankka, "Digital Modulator for Continuous Modulations with Slow Frequency Hopping," IEEE Transactions on Vehicular Technology, vol. 46, pp. 933-940, Nov. 1997.

[4] J. Vankka, M. Waltari, M. Kosunen, and K. Halonen, "Direct Digital Syntesizer with on-Chip D/A-converter," IEEE Journal of Solid-State Circuits, Vol. 33, No. 2, pp. 218-227, Feb. 1998.

[5] M. Kosunen, J. Vankka, M. Waltari, L. Sumanen, K. Koli, and K. Halonen, "A CMOS Quadrature Baseband Frequency Synthesizer/Modulator", Analog Integrated Circuits and Signal Processing, Vol. 18, No. 1, pp. 55-67, Jan. 1999.

[6] J. Vankka, M. Kosunen, I. Sanchis, and K. Halonen "A Multicarrier QAM Modulator", IEEE Trans. on Circuits and Systems Part II, Vol. 47, No. 1, pp. 1-10, Jan. 2000.

[7] J. Vankka, M. Honkanen, and K. Halonen "A Multicarrier GMSK Modulator", accepted to IEEE Journal on Selected Areas in Communications: Wireless Communications Series.

Patents

[8] J. Vankka, “QAM Modulator”, PCT Patent Application PCT/FI99/00335, 1999.

[9] J. Vankka, and M. Honkanen, “Digital Ramp Generator with Output Power Level Controller”, PCT Patent Application PCT/FI99/92614, 1999.

Chapters in Books

[10] J. Vankka, "Methods of Mapping from Phase to Sine Amplitude in Direct Digital Synthesis", pp. 86–94, in (edited by) V. F. Kroupa, "Direct Digital Frequency Synthesizers", 1999, IEEE Press.

Refereed International Conference Papers

[11] J. Vankka, J. Pyykönen, J. Sommarek, M. Honkanen, and Kari Halonen, "A Multicarrier GMSK Modulator for Base Station," accepted to ISSCC, February 2001, San Francisco, CA, USA.

[12] J. Vankka, "Methods of Mapping from Phase to Sine Amplitude in Direct Digital Synthesis," in Proc. 1996 IEEE Frequency Control Symposium, Honolulu, Hawaii, July 5-7, 1996, pp. 942-950.

[13] J. Vankka, "Spur Reduction Techniques in Sine Output Direct Digital Synthesis," in Proc. 1996 IEEE Frequency Control Symposium, Honolulu, Hawaii, July 5-7, 1996, pp. 951-959.

[14] J. Vankka, "A Novel Spur Reduction Technique in Direct Digital Synthesizer," in Proc. IEEE NORSIG'96, Sept. 1996, pp. 199-202.

[15] J. Vankka, "Digital Modulator for Continuous Modulations with Slow Frequency Hopping," in Proc. IEEE Personal, Indoor and Mobile Radio Communications Conference, Oct. 15-18, 1996, Taipei, Taiwan, pp. 1039-1043.

[16] J. Vankka, M. Kosunen, M. Waltari, K. Halonen, "Direct Digital Syntesizer with on-Chip D/A-converter," in Proc. 14th NORCHIP conference, 4-5 November 1996, Helsinki, Finland, pp. 20-27.

[17] J. Vankka, M. Waltari, M. Kosunen, and K. Halonen, "Design a Direct Digital Syntesizer with an on-Chip D/A-converter," in Proc. IEEE International Symposium on Circuits and Systems, June 9-12, 1997, Hong Kong, pp. 21-24.

[18] J. Vankka, M. Waltari, M. Kosunen, and K. Halonen, "Direct Digital Syntesizer with on-Chip D/A-converter," in Proc. 23rd European Solid-State Circuits Conference, Sept. 16-18, 1997, Southampton, United Kingdom, pp. 216-219.

[19] M. Kosunen, J. Vankka, M. Waltari, K. Koli, L. Sumanen, and K. Halonen, "Design of a 2.4 GHz CMOS Frequency Hopped RF Transmitter IC," in Proc. 15th NORCHIP conference, Nov. 10-11, 1997, Tallinn, Estonia, pp. 296-303.

[20] M. Kosunen, J. Vankka, M. Waltari, L. Sumanen, K. Koli, and K. Halonen, "Design of a 2.4 GHz CMOS Frequency Hopped RF Transmitter IC," in Proc. ISCAS'98 conference, May 31-June 3, 1998 Monterey, California, USA, pp. 512-515.

[21] M. Kosunen, J. Vankka, M. Waltari, L. Sumanen, K. Koli, and K. Halonen, "Design of a 2.4 GHz CMOS Frequency Hopped RF Transmitter IC," in Proc. Baltic Electronic Conference 1998, 7-9 October 1998, Tallinn, Estonia, pp. 219-222.

[22] M. Kosunen, J. Vankka, M. Waltari, L. Sumanen, K. Koli, and K. Halonen, "A CMOS Quadrature Baseband Frequency Synthesizer/Modulator," in Proc. ESSCIRC'98, 22 - 24 Sep. 1998, The Hague, The Netherlands, pp. 340-343.

[23] J. Vankka, M. Kosunen, and K. Halonen, "A Multicarrier QAM Modulator," in Proc. IS-CAS'99 conference, May 30-June 2, 1999 Orlando, Florida, USA, Vol. IV, pp. 415 - 418.

[24] J. Vankka, I. Sanchis, M. Kosunen, and K. Halonen "A Cordic Based QAM Modulator," in Proc. ISIC'99 conference, 8–10 Sep., 1999 Singapore, pp. 300-303.

[25] J. Vankka, M. Kosunen, J. Hubach, and K. Halonen "A Cordic Based Multicarrier QAM Modulator," in Proc. Globecom'99 conference, Dec. 1999, pp. 173-177.

[26] J. Vankka, L. Sumanen, and K. Halonen "A QAM Modulator for WCDMA Base Station," in Proc. 13th Annual IEEE International ASIC/SOC Conference, Sept. 2000, pp. 65-69.

2. Direct Digital Synthesizer

In this chapter the operation of the direct digital synthesizer is first described. It is simple to add modulation capabilities to the DDS, because the DDS is a digital signal processing device. It is shown that the DDS produces spurs as well as the desired output frequency.

2.1 Conventional Direct Digital Synthesizer

The direct digital synthesizer (DDS) is shown in a simplified form in Figure 2.1. The direct digital frequency synthesizer (DDFS) or numerically controlled oscillator (NCO) is also widely used to define this circuit. The DDS has the following basic blocks; a phase accumulator, a phase to amplitude converter (conventionally a sine ROM), a digital to analog converter and a filter [Tie71], [Hut75], [Bra81]. The phase accumulator consists of a *j*-bit frequency register which stores a digital phase increment word followed by a *j*-bit full adder and a phase register. The digital input phase increment word is entered in the frequency register. At each clock pulse this data is added to the data previously held in the phase register. The phase increment word represents a phase angle step that is added to the previous value at each $1/f_{clk}$ seconds to produce a linearly increasing digital value. The phase value is generated using the modulo 2^j overflowing property of a *j*-bit phase accumulator. The rate of the overflows is the output frequency

$$f_{out} = \frac{\Delta P \, f_{clk}}{2^j} \qquad \forall \quad f_{out} \le \frac{f_{clk}}{2}, \tag{2.1}$$

where ΔP is the phase increment word, j is the number of phase accumulator bits, f_{clk} is the clock frequency and f_{out} is the output frequency. The constraint in (2.1) comes from the sampling theorem. The phase increment word in (2.1) is an integer, therefore the frequency resolution is found by setting $\Delta P = 1$

$$\Delta f = \frac{f_{clk}}{2^j}. \tag{2.2}$$

The read only memory (ROM) is a sine look-up table, which converts the digital phase information into the values of a sine wave. In the ideal case with no phase and amplitude quantization, the output sequence of the table is given by

$$\sin(2\pi \frac{P(n)}{2^j}), \tag{2.3}$$

where $P(n)$ is a (the j-bit) phase register value (at the nth clock period). The numerical period of the phase accumulator output sequence is defined as the minimum value of Pe for which $P(n) = P(n+Pe)$ for all n. The numerical period of the phase accumulator output sequence (in clock cycles) is

$$Pe = \frac{2^j}{\mathrm{GCD}(\Delta P, 2^j)}, \tag{2.4}$$

where GCD $(\Delta P, 2^j)$ represents the greatest common divisor of ΔP and 2^j. The numerical period of the sequence samples recalled from the sine ROM will have the same value as the numerical

period of the sequence generated by the phase accumulator [Dut78], [Nic87]. Therefore, the spectrum of the output waveform of the DDS prior to a digital-to-analog conversion is characterized by a discrete spectrum consisting of *Pe* points. The ROM output is presented to the D/A-converter, which develops a quantitized analog sine wave. The D/A-converter output spectrum contains frequencies $nf_{clk} \pm f_{out}$, where n = 0, 1, …etc. (see Appendix A). The amplitudes of these components are weighted by a function (see Appendix A)

$$\sin c(\frac{f}{f_{clk}}). \tag{2.5}$$

This effect can be corrected by an inverse sinc(f/f_{clk}) filter. The filter that is after the D/A converter removes the high frequency sampling components and provides a pure sine wave output. As the DDS generates frequencies close to $f_{clk}/2$, the first image (f_{clk} - f_{out}) becomes more difficult to filter. This results in a narrower transition band for the filter. The complexity of the filter is determined by the width of the transition band. Therefore, in order to keep the filter simple, the DDS operation is limited to less than 40 percent of the clock frequency (see Section 10.2).

2.2 Pulse Output DDS

The pulse output DDS is the simplest DDS type. It has only a phase accumulator. The MSB or

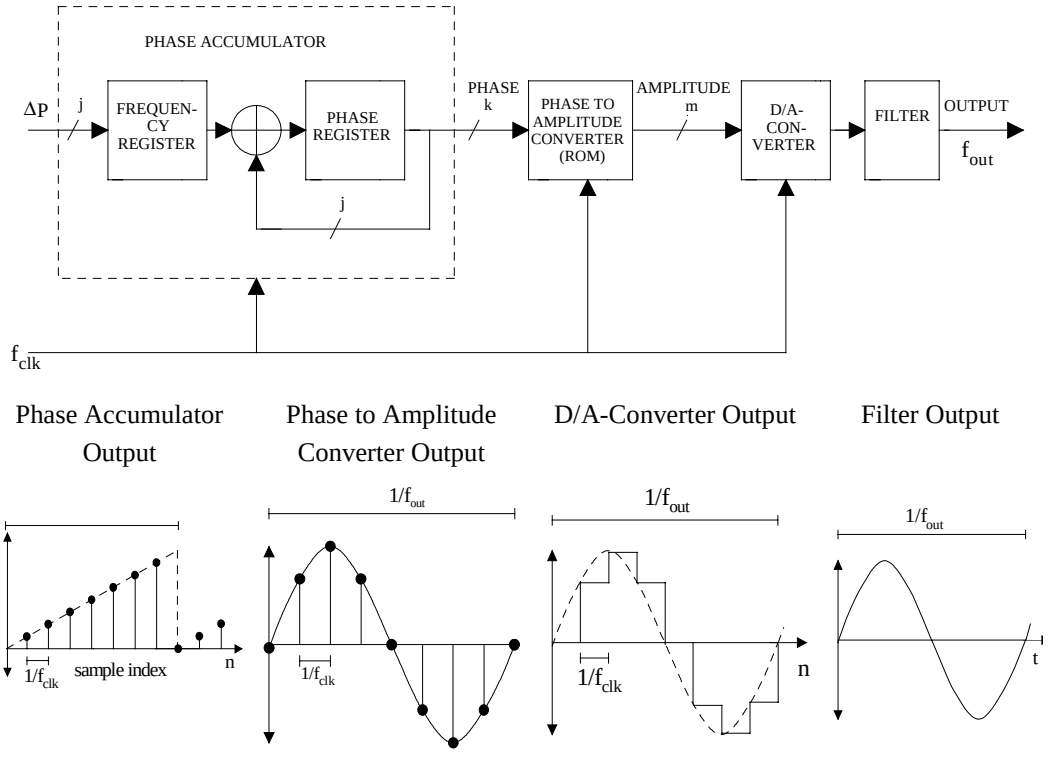

Figure 2.1. Simplified block diagram of the direct digital synthesizer, and the signal flow in the DDS.

Table 2.1. For an accumulator of 3 bits (j=3) controlled with an input of ΔP = 3 and ΔP = 2.

Accumulator output ΔP = 3 and j = 3	Carry output	Accumulator output ΔP = 2 and j = 3	Carry output
000 (0)	1 Cycle begins	000 (0)	1 Cycle begins
011 (3)	0	010 (2)	0
110 (6)	0	100 (4)	0
001 (1)	1	110 (6)	0
100 (4)	0	000 (0)	1
111 (7)	0	010 (2)	0
010 (2)	1	100 (4)	0
101 (5)	0	110 (6)	0
000 (0)	1	000 (0)	1

carry output signal of the phase accumulator is used as an output. The average frequency of the DDS is obtained from (2.1). As long as ΔP divides into 2^j, the output is periodic and smooth (see column 3 in Table 2.1), but all other cases create jitter. The output can change its state only at the clock rate. If the desired output frequency is not a factor (a divider) of 2^j, then a phase error is created between the ideal and the actual output. This phase error will increase (or decrease) until it reaches a full clock period, at which time it returns to zero and starts to build up again (see column 1 in Table 2.1). Ideally we would like to generate a transition every 8/3 = 2.6667 cycles (see column 1 in Table 2.1), but this is not possible because the phase accumulator can generate a transition only at integer multiples of the clock period. After the first transition the error is -1/3 clock period (we should transit after 2.6667 clocks, and we transit after 3), and after the second it is -2/3 clock period (we should transit after 5.33, and we do after 6). There is a clear relation between the error and the parameters ΔP (phase increment word) and C (phase accumulator output at the moment of carry generation). The error is exactly $-C/\Delta P$.

By using a digital delay generator (see Figure 2.2), the carry output is first connected to a logic circuit that calculates first the ratio $-C/\Delta P$ and delays the carry signal [Nuy90], [Gol96]. The negative delay must be converted into a positive delay, which is 1 - $C/\Delta P$, $\Delta P > C$ in all situations (the carry overflow error can never be as large ΔP).

It is assumed that the delay-time of the whole delay line meets exactly $T_{clk} = 1/f_{clk}$. For the delay components inside the delay line there are B-1 additional outputs with delay times

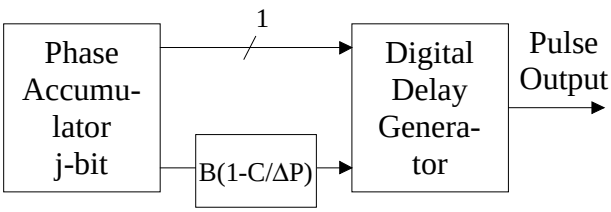

Figure 2.2. Single bit DDS with a digital delay generator.

$$T_{cv} = \frac{y\,T_{clk}}{B}, \quad \text{where } y = 1, ..., B-1, \tag{2.6}$$

and where $B = 2^b$ in this case. The applied delay (yT_{clk}/B) is a multiple of the delay components inside the delay line, and the positive delay time is

$$T_{clk} - \frac{C\,T_{clk}}{\Delta P}. \tag{2.7}$$

From these two equations, it is easy to solve y (digital delay generator input)

$$y = \left[B\left(1 - \frac{C}{\Delta P}\right) \right], \tag{2.8}$$

where [] denotes truncation to integer values. The division $C/\Delta P$ requires a lot of hardware.

The delay generator could also be implemented with analog techniques [Nak97], [Mey98], [Nie98].

2.3 DDS Architecture for Modulation Capability

It is simple to add modulation capabilities to the DDS, because the DDS is a digital signal processing device. In the DDS it is possible to modulate numerically all three waveform parameters

$$s(n) = A(n)\sin(2\pi(\Delta P(n) + P(n))), \tag{2.9}$$

where $A(n)$ is the amplitude modulation, $\Delta P(n)$ is the frequency modulation, and $P(n)$ is the phase modulation. All known modulation techniques use one, two or all three basic modulation types simultaneously. Consequently any known waveform can be synthesized from these three basic types within the Nyquist band limitations in the DDS. Figure 2.3 shows a block diagram of a basic DDS system with all three basic modulations in place [Zav88a], [McC88]. The frequency modulation is made possible by placing an adder before the phase accumulator. The phase modulation requires an adder between the phase accumulator and the phase to amplitude converter. The amplitude modulation is implemented by inserting a multiplier between the phase to amplitude converter and the D/A-converter. The multiplier adjusts the digital ampli-

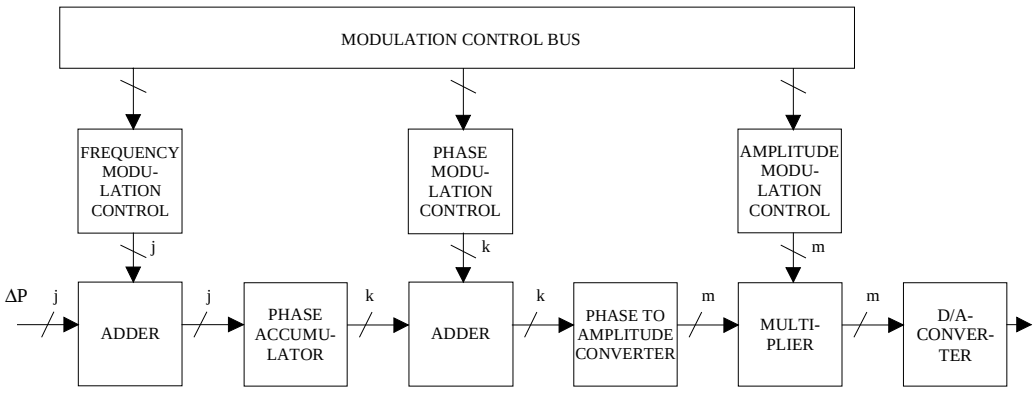

Figure 2.3. DDS architecture with modulation capabilities.

tude word applied to the D/A-converter. Also, with some D/A-converters it is possible to provide an accurate analog amplitude control by varying a control voltage [Sta94].

2.4 QAM Modulator

The block diagram of the conventional QAM modulator with quadrature outputs is shown in Figure 2.4. The output of the QAM modulator is

$$\begin{aligned} I_{out}(n) &= I(n)\cos(\omega_{QDDS}\ n) + Q(n)\sin(\omega_{QDDS}\ n) \\ Q_{out}(n) &= Q(n)\cos(\omega_{QDDS}\ n) - I(n)\sin(\omega_{QDDS}\ n), \end{aligned} \tag{2.10}$$

where ω_{QDDS} is the quadrature direct digital synthesizer (QDDS), and $I(n)$, $Q(n)$ are pulse shaped and interpolated quadrature data symbols [Tan95a]. The direct implementation of (2.10) requires a total of four real multiplications and two real additions, as shown in Figure 2.4. However, we can reformulate (2.10) as [Wen95]

$$\begin{aligned} I_{out}(n) &= I(n)(\cos(\omega_{QDDS}\ n) + \sin(\omega_{QDDS}\ n)) + \sin(\omega_{QDDS}\ n)(Q(n) - I(n)) \\ Q_{out}(n) &= Q(n)(\cos(\omega_{QDDS}\ n) - \sin(\omega_{QDDS}\ n)) + \sin(\omega_{QDDS}\ n)(Q(n) - I(n)). \end{aligned} \tag{2.11}$$

The term $\sin(\omega_{QDDS})$ $(Q(n) - I(n))$ appears in the both outputs. Therefore, the total number of real multiplications is reduced to three. This however is at the expense of having five real additions.

The pre-equalizer is used to compensate for the sinx/x roll-off function inherent in the sampling process of the digital-to-analog conversion, as shown in Figure 2.4. Furthermore, distortions in the phase and magnitude response of the analog filters (Figure 11.2) could be partly pre-compensated by the pre-equalizer. The analysis and compensation of the distortions from ana-

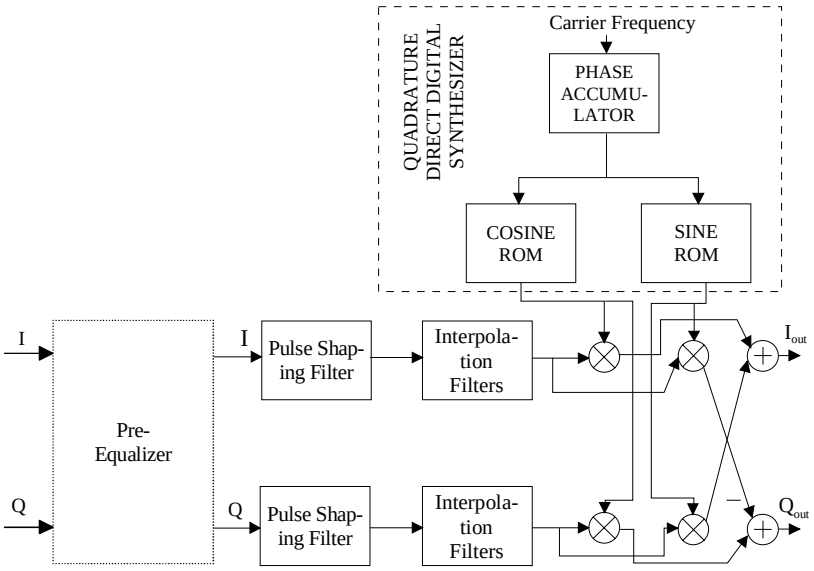

Figure 2.4. QAM modulator with quadrature outputs.

log filters are beyond the scope of this thesis. The pulse shaping filter reduces the transmitted signal bandwidth, which results in an increase in the number of available channels, and at the same time it maintains low adjacent channel interferences. Furthermore, it minimizes the inter-symbol interference (ISI). The interpolation filters increase the sampling rate and reject the extra images of the signal spectrum resulting from the interpolation operations. The quadrature DDS and the complex multiplier translate the signal spectrum from the baseband into the IF.

All the waveshaping is performed by the lower sample rate in the pulse shaping filter, and the interpolation filters must not introduce any additional magnitude and phase distortion [Cro83]. The interpolation filters are usually implemented with multirate FIR structures. There exists a well-known multirate architecture for implementing very narrow-band FIR filters, which consists of a programmable coefficient FIR filter, and half band filters followed by the cascaded-integrator-comb (CIC) structure [Hog81]. Unfortunately, the CIC structure is not well suited for implementing wideband filters because the frequency response of the CIC filter does not have a satisfactory stopband attenuation. Furthermore, the CIC filter introduces droop in the passband.

A variable interpolator allows the use of sampling rates which are not multiples of the symbol rates. It enables one to transmit signals having different symbol rates [Cho99], [Lun99]. Mathematically, there are a number of interpolation schemes that can perform the desired operation [Ram84]. However, many of them, such as sinc based interpolation, require excessive computational resources for a practical hardware implementation. For real time calculations, Erup [Eru93] et. al. found polynomial-based interpolation to yield satisfactory results while minimizing the hardware complexity. This structure can be easily implemented with hardware using the Farrow structure [Far88].

If the quadrature output is not needed, then the complex oscillator could be replaced with the two multipliers and an adder, as shown in Figure 2.5. At the system architectural design level, a

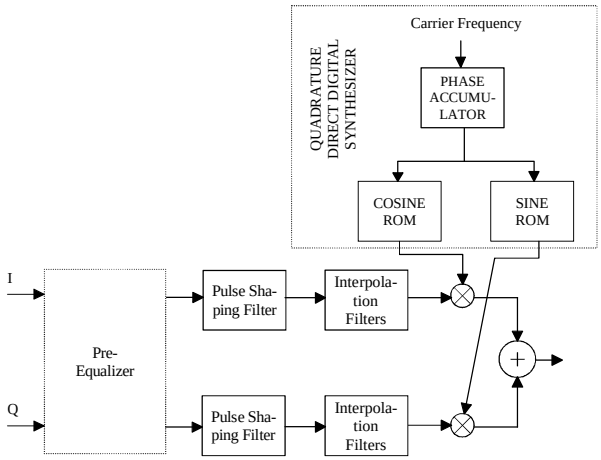

Figure 2.5. QAM modulator.

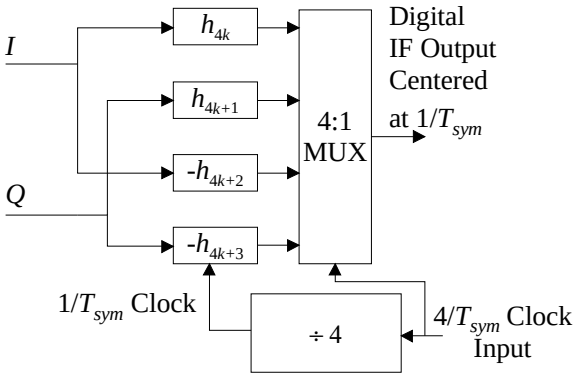

Figure 2.6. Simplified digital modulator.

substantial hardware reduction has been obtained by selecting a filter over-sampling factor of 4, and by forcing the IF center frequency to equal the symbol rate $1/T_{sym}$ [Won91]. This results in oscillator samples of $\cos(n\pi/2)$ and $\sin(n\pi/2)$ which have the trivial values of 1, 0, -1, 0, …, thus eliminating the need for high-speed digital multipliers and adders to implement the mixing functions. Furthermore, since half of the cosine and sine oscillator samples are zero, only a single interpolate-by-4 transmit filter can be used to process the data in both I and Q rails of the modulator, as shown in Figure 2.6. Thus the only hardware operating at $4/T_{sym}$ in the modulator is a 4:1 multiplexer at the output.

2.5 Digital Chirp DDS

Another type of DDS application is dedicated to digital chirp generators, used in sweep oscillators. The chirp generators generate a FM signal that is fully synthesized and therefore achieves linearity and accuracy not possible with regular analog techniques (VCOs). The digital synthesis of the chirp waveform is based on the realization that the quadratic time base

$$\phi(t) = C\,t^2 + B\,t + A, \tag{2.12}$$

can be generated numerically at high-speed using addition only. The digital chirp generator is similar to the regular direct digital synthesizer but includes a dual accumulator as shown in Figure 2.7. The outputs of the accumulators are stored in registers. Table 2.2 presents the contents of the rate register (R1), and the two phase accumulator outputs (i.e., R2 and R3) for the first few clock cycles in a chirp-generator sequence. This illustrates the process of the quadratic

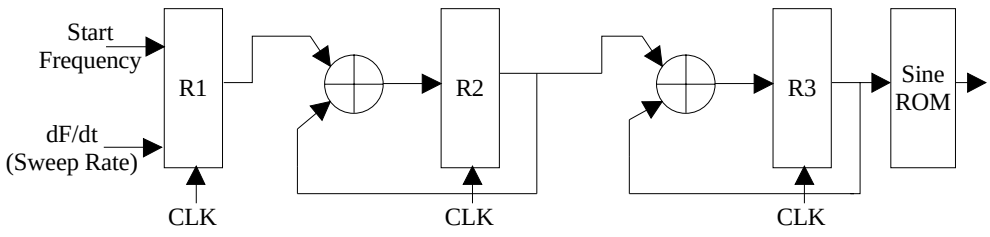

Figure 2.7. Digital chirp generator.

Table 2.2. Generation of Quadratic Time Using a Double Phase Accumulator.

Clock cycle	R1 Rate	R2 (Frequency)	R3 (Phase)
Initial values	$2C$	$C + B$	A
1	$2C$	$3\,C + B$	$1^2\,C + 1\,B + A$
2	$2C$	$5\,C + B$	$2^2\,C + 2\,B + A$
3	$2C$	$7\,C + B$	$3^2\,C + 3\,B + A$
4	$2C$	$9\,C + B$	$4^2\,C + 4\,B + A$
⋮	⋮	⋮	⋮
n	$2C$	$(2n + 1)\,C + B$	$n^2\,C + n\,B + A$

time base generation. After the register initialization, the results of R2 (or R3) at each clock cycle are obtained from the sum of data stored within itself and R1 (or R2) in the previous clock cycle. The phases generated in Table 2.2 are identical to those of (2.12) when t is replaced by nT_{clk}, where T_{clk} is the clock period. The initial frequency, B, and the sweep rate, C, are loaded into the registers asynchronously and held there until a chirp trigger signal is received.

A GaAs implementation for this device is presented in [And92]. The clock frequency is 450 MHz, power consumption is 18 W, and the phase accumulator width (j) is 28.

The chirp rate is perfect except that there is always a level of quantization. For example, the device described above has a minimum step size of 1.7 Hz (2.2). Another problem is the LPF group delay, especially at the high end of the band. If this becomes important in the application, a phase equalizer needs to be added to compensate for the filter group delay.

2.6 DDS Power Consumption and Spurious Level

Although the DDSs were invented decades ago [Tie71] they did not come to play a dominant role in wideband frequency generation until recently. Initially, the DDSs were limited to producing narrow bands of closely spaced frequencies, due to limitations of digital logic and D/A-converter technologies. It is likely that DDS technology will continue to improve as digital technology advances. Figure 2.8 and Figure 2.9 illustrate trade-offs that will pose problems: the wider the DDS output bandwidth, the higher the DC power consumption; the wider the DDS output bandwidth, the higher the spurious level. The critical path of the signal could be accomplished by the DDS, which has the advantages of a fast switching time, a fine frequency resolution, and coherent frequency hopping. In the wide output bandwidth DDSs, most spurs are generated less by digital errors (truncation or quantization errors) and more by analog errors in the D/A-converter such as clock feedthrough, intermodulation, glitch energy. In Figure 2.9, spurious performance is degraded approximately at the rate of 6 dB/octave in the output bandwidth (solid line). This is because the spurs are mostly due to glitch energy in the D/A-converter out-

put. As the output voltage is held for shorter periods of time, the glitch becomes a greater percentage of the output energy.

CMOS technology provides substantial cost and power advantages over those of silicon bipolar and GaAs technologies. The use of CMOS DDS technologies without parallel architecture has been restricted by their limited bandwidth [Bel00], [QuS91], [Ana94], [Ana99b], [NiB94], [Mad99], [Chapter 10], [Mor99], [Tan95a] (Figure 2.8, Figure 2.9). The use of parallelism to attain high throughput has been utilized for DDS applications [Tan95b]. Using the parallel architecture with four sine ROM tables, the CMOS-chip has an output bandwidth of 320 MHz ($0.4 \times f_{clk}$) [Tan95b]. The chip that uses only one sine ROM table has an output bandwidth of 80 MHz [Tan95a]. Efforts have been made to extend the DDS designs to silicon bipolar [SaA94], [Sau90], [Sci94] and GaAS [Sta94] processing technologies.

The above analysis is quite rough, because it does not include other signal processing capabilities that these circuits will have, e.g. modulation. These properties will increase power consumption compared with the 'standard DDS'. The output of the DDS is a pure sine wave in the above case.

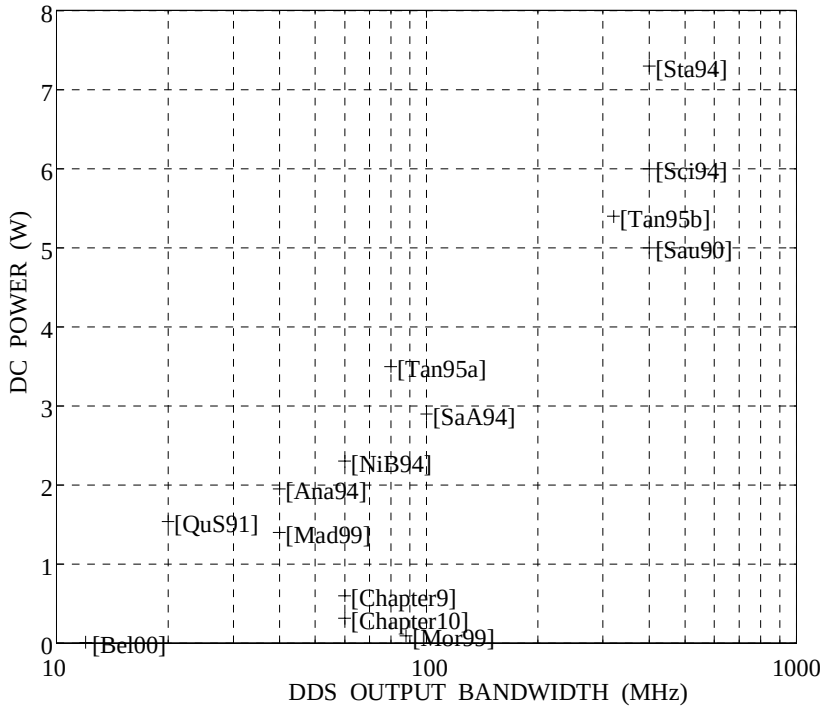

Figure 2.8 DDS Power Consumption vs. Output Bandwidth. Data points based on references [Bel00], [QuS91], [Ana94], [Mad99], [NiB94], [Chapter 9], [Chapter 10], [Tan95a], [Mor99], [SaA94], [Tan95b], [Sau90], [Sci94], [Sta94].

2.7 State of the Art in DDS ICs

Table D.1 (see Appendix D) shows different recently reported DDS ICs. A comparison is difficult because it does not include other signal processing capabilities that these circuits have. These properties increase power consumption and area compared with the 'standard DDS'. The power consumption and area of the DDS will continue to decrease as digital technology advances (see [Bel00] and [Mor99] in Figure 2.8). In Table D.1 the multi-carrier DDS modulators with the on-chip D/A converters are shown. These are original contributions to the subject of the thesis.

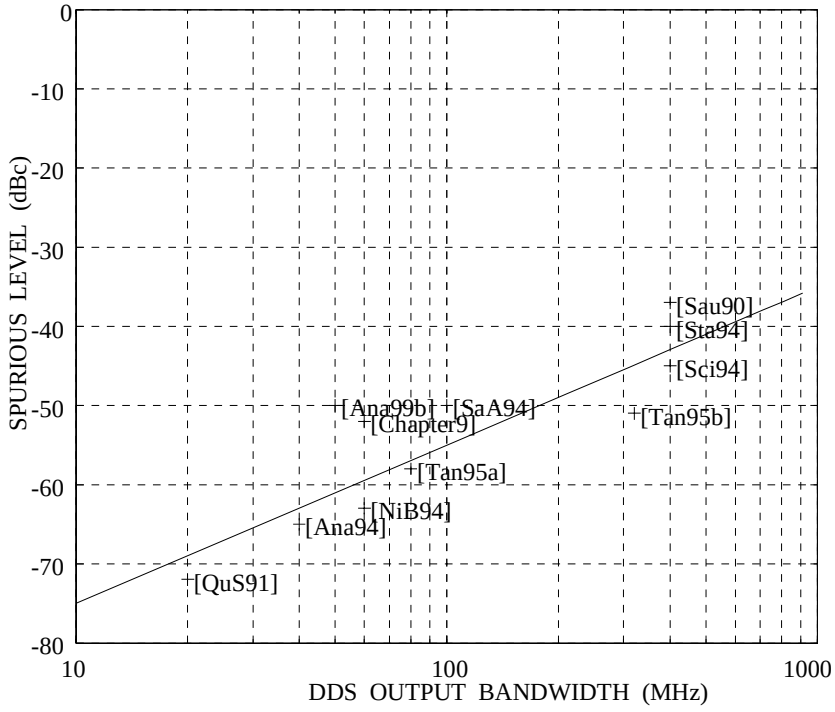

Figure 2.9 DDS Spurious Level vs. Output Bandwidth. Data points based on references [QuS91], [Ana94], [Ana99b], [NiB94], [Chapter 9], [Tan95a], [SaA94], [Tan95b], [Sau90], [Sci94], [Sta94].

3. Indirect Digital Synthesizer

In this chapter the operation of the indirect digital synthesizer is first described. It is shown that it produces spurs as well as the desired output frequency. A quadrature indirect digital synthesizer is also presented.

3.1 Direct-Form Oscillator

Figure 3.1 shows the signal flow graph of the well-known second-order direct-form feedback structure with state variables $x_1(n)$ and $x_2(n)$ [Gol69], [Fur75], [Abu86a]. The corresponding difference equation for this system is given by

$$x_2(n+2) = \alpha\, x_2(n+1) - x_2(n). \tag{3.1}$$

The two state variables are related by

$$x_1(n) = x_2(n+1). \tag{3.2}$$

Solving the one-sided z transform of (3.1) for $x_2(n)$ leads to

$$X_2(z) = \frac{(z^2 - \alpha z)\, x_2(0) + z\, x_1(0)}{z^2 - \alpha z + 1}, \tag{3.3}$$

where $x_1(0)$ and $x_2(0)$ are the initial values of the state variables. Identifying the second state variable as the output variable

$$y(n) = x_2(n), \tag{3.4}$$

as shown in Figure 3.1, and choosing the denominator coefficient α to be

$$\alpha = 2\cos\theta_0, \qquad \theta_0 = \omega_0 T = 2\pi\, f_0 / f_{clk}, \tag{3.5}$$

with f_0 being the oscillator frequency and f_{clk} the sampling frequency, then, on choosing the initial values of the state variables to be

$$x_1(0) = A'\cos\theta_0, \qquad x_2(0) = A', \tag{3.6}$$

we obtain from (3.3) a discrete-time sinusoidal function as the output signal:

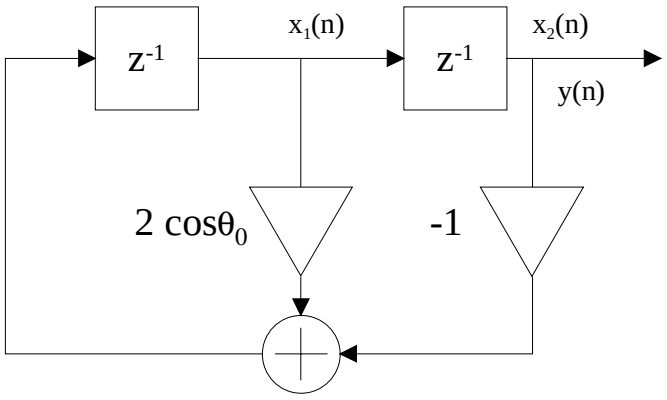

Figure 3.1. Recursive digital oscillator structure.

$$Y(z) = \frac{A'(z^2 - \cos\theta_0\ z)}{z^2 - 2\cos\theta_0\ z + 1}. \tag{3.7}$$

It has complex-conjugate poles at $p = \exp(\pm j\theta_0)$, and a unit sample response

$$y(n) = A'\cos(n\theta_0), \qquad n \geq 0. \tag{3.8}$$

Thus the impulse response of the second-order system with complex-conjugate poles on the unit circle is a sinusoidal waveform.

An arbitrary initial phase offset φ_0 can be realized [Fli92], namely,

$$y(n) = A'\cos(\theta_0 n + \varphi_0), \tag{3.9}$$

by choosing the initial values:

$$x_1(0) = A'\cos(\theta_0 + \varphi_0), \tag{3.10}$$

$$x_2(0) = A'\cos(\varphi_0). \tag{3.11}$$

Thus, any real-valued sinusoidal oscillator signal can be generated by the second-order structure shown in Figure 3.1.

The output sequence $y(n)$ of the ideal oscillator is the sampled version of a pure sine wave. The angle θ_0 represented by the oscillator coefficient is given by

$$\theta_0 = 2\pi\ f_0 / f_{clk}, \tag{3.12}$$

where f_0 is the desired frequency in cycles per second. In an actual implementation, the multiplier coefficient $2\cos\theta_0$ is assumed to have $b + 2$ bits. In particular, 1 bit is for the sign, 1 bit for the integer part and b bits for the remaining fractional part in the fixed-point number representation. Then the largest value of the coefficient $2\cos\theta_0$ which can be represented, is $(2 - 2^{-b})$. This value of the coefficient gives the smallest value of θ_{min}, which can be implemented by the direct form digital oscillator using b bits

$$\theta_{\min} = \cos^{-1}\left[\frac{1}{2}(2 - 2^{-b})\right]. \tag{3.13}$$

Therefore, the smallest frequency that the oscillator can generate is

$$f_{\min} = \frac{\theta_{\min}}{2\pi}\ f_{clk}, \tag{3.14}$$

where f_{clk} is the clock frequency (sampling frequency). As an example, let $b = 25$ bits. The largest oscillator coefficient ($2\cos\theta_0$) is 67108863/33554432 and $\theta_{min} = \cos^{-1}(67108863/67108864) \approx 0.00017263$. For $f_{clk} = 52$ MHz and $b = 25$, $f_{min} \approx 1.43$ kHz.

In this digital oscillator, besides the zero-input response $y(n)$ of the second-order system we get a zero-state response $y_{err}(n)$ due to the random sequence $e_2(n)$ acting as an input signal. From (3.1) we obtain

$$y(n + 2) = \alpha\, y(n + 1) - y(n) + e_2(n), \tag{3.15}$$

and by the z transformation

$$Y(z) = Y_{\text{ideal}}(z) + Y_{err}(z), \tag{3.16}$$

with $Y_{\text{ideal}}(z)$ derived from (3.7). The z transform of the output error $y_{\text{err}}(n)$ is given by

$$Y_{err}(z) = \frac{E_2(z)}{z^2 - 2\cos\theta_0\, z + 1}, \tag{3.17}$$

with $E_2(z)$ being the z transform of the quantization error signal $e_2(n)$. Transforming $Y_{\text{err}}(z)$ back into the time domain results in an output error sequence

$$y_{err}(n) = \frac{1}{\sin\theta_0} \sum_{k=2}^{n} e_2(k) \sin(\theta_0\,(n-k+1)), \quad \text{for } n \geq 2, \tag{3.18}$$

where $e_2(1)$ and $e_2(2)$ are assumed to be zero. Equation (3.18) shows that the output error is inversely proportional to $\sin(\theta_0)$, thus the output error increases with the decreasing digital oscillator frequency. A computer simulation of (3.15) and an evaluation of (3.18) lead to a sinusoidal output error signal $y_{err}(n)$ with the same frequency as that of $y_{\text{ideal}}(n)$, but with amplitude less than the amplitude of $y_{\text{ideal}}(n)$ [Fli92]. The output quantization error can be reduced by an appropriate error noise shaping [Abu86b]. In addition to the error noise shaping, a periodic oscillator reset could be applied. In order to eliminate an infinite accumulation of errors, the direct-form oscillator could be reset to its initial states after N samples (K cycles) if the normalized frequency $\theta_0/2\pi$ equals the rational number K/N [Fur75].

3.2 Coupled-Form Complex Oscillator

In some practical applications involving modulation of two sinusoidal carrier signals in phase quadrature, there is a need to generate the sinusoids $A'\sin\theta_0 n$ and $A'\cos\theta_0 n$ [Gol69], [Fli92]. These signals can be generated from the so-called coupled-form oscillator, which can be obtained from the trigonometric formulae

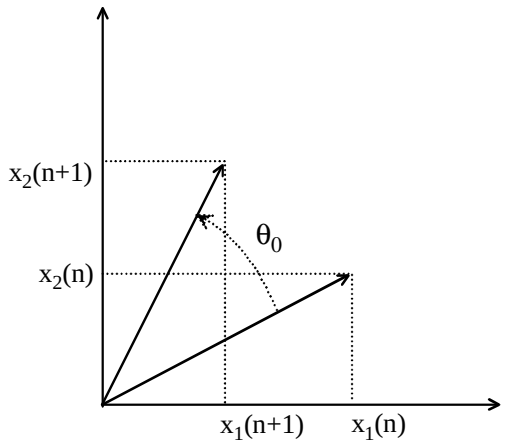

Figure 3.2. Vector rotation.

$$A'\cos(\alpha+\beta) = A'\cos(\alpha)\cos(\beta) - A'\sin(\alpha)\sin(\beta)$$
$$A'\sin(\alpha+\beta) = A'\cos(\alpha)\sin(\beta) + A'\sin(\alpha)\cos(\beta), \tag{3.19}$$

where, by definition, $\alpha = n\theta_0$, $\beta = \theta_0$, and

$$x_1(n+1) = A'\cos((n+1)\theta_0)$$
$$x_2(n+1) = A'\sin((n+1)\theta_0). \tag{3.20}$$

Thus we obtain the two coupled equations

$$x_1(n+1) = x_1(n)\cos(\theta_0) - x_2(n)\sin(\theta_0)$$
$$x_2(n+1) = x_1(n)\sin(\theta_0) + x_2(n)\cos(\theta_0), \tag{3.21}$$

that perform a general rotational transform anti-clockwise with angle θ_0; the coordinates of a vector in Figure 3.2 transform from (x_1(n), $x_2(n)$) to (x_1(n+1), $x_2(n+1)$). The structure for the realization of the coupled-form oscillator is illustrated in Figure 3.3. This is a two-output system which is not driven by any input, but which requires the initial conditions $x_1(0) = A'\cos(\theta_0)$ and $x_2(0) = A'\sin(\theta_0)$ in order to begin its self-sustaining oscillations.

From the z transform of the state equations (3.21)

$$z\,X = V\,X, \quad X = [X_1(z)\;X_2(z)]^T \tag{3.22}$$

the characteristic equation

$$D(z) = |z\,I - V| = \begin{vmatrix} z-\cos\theta_0 & \sin\theta_0 \\ -\sin\theta_0 & z-\cos\theta_0 \end{vmatrix}$$
$$= z^2 - 2\cos\theta_0\; z + \cos^2\theta_0 + \sin^2\theta_0 \tag{3.23}$$

can be derived. From (3.23) it is obvious that the eigenvalues are lying on the unit circle of the z plane. In a finite register length arithmetic, however, the eigenvalues almost never have exactly unit magnitude because the two coefficients $\cos(\theta_0)$ and $\sin(\theta_0)$ are realized separately. Thus we observe no stable limit cycle but a waveform with an increasing or decreasing amplitude.

Equation (3.21) shows that x_1 and x_2 will both be sinusoidal oscillations that are always in exact

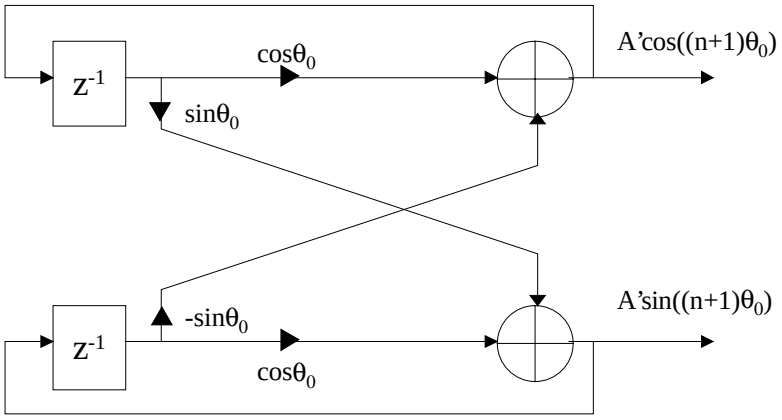

Figure 3.3. Coupled-form complex oscillator.

phase quadrature. Furthermore, if quantization effects are ignored, then, for any time n, the equality

$$x_1^2(n) + x_2^2(n) = x_1^2(0) + x_2^2(0) \tag{3.24}$$

holds. In order to reset the system so that, after every k iterations, the variables $x_1(n)$ and $x_2(n)$ are changed to satisfy (3.24), we can multiply both $x_1(n)$ and $x_2(n)$ by the factor

$$f(n) = \sqrt{\frac{x_1^2(0) + x_2^2(0)}{x_1^2(n) + x_2^2(n)}}. \tag{3.25}$$

Thus, for each k iterations of (3.21), we perform once the non-linear iteration

$$\begin{aligned} x_1(n+1) &= f(n)\left[x_1(n)\cos(\beta) - x_2(n)\sin(\beta)\right] \\ x_2(n+1) &= f(n)\left[x_1(n)\cos(\beta) + x_2(n)\sin(\beta)\right]. \end{aligned} \tag{3.26}$$

Execution of (3.26) effectively resets $x_1(n + 1)$ and $x_2(n + 1)$ so that (3.24) is satisfied. Thus, if $x_1(n)$ and $x_2(n)$ had both drifted by the same relative amount to a lower value, both would be raised, in one iteration cycle, to the value they would have had if no noise were present. If, however, $x_2(n)$ had drifted up and $x_1(n)$ down so that the sum of the squares were satisfied (3.24), then (3.26) would have no effect. Thus the drifts of phase are not compensated by (3.26). The most efficient method of eliminating the infinite accumulation of errors of the coupled-form complex oscillator is to reset its initial states after N samples (K cycles) if the normalized frequency $\theta_0/2\pi$ equals the rational number K/N.

The phase coherent frequency hopping is difficult to implement by the coupled form complex oscillator, because the new initial values must be updated phase coherently. To increase the frequency resolution requires that the word length of the whole complex oscillator is widened, however, in the case of the conventional direct digital synthesizer, it is only necessary to increase the phase accumulator word length (see (2.2)).

4. CORDIC Algorithm

4.1 Introduction

Algorithms used in communication technology require the computation of trigonometric functions, coordinate transformations, vector rotations, or hyperbolic rotations. The CORDIC, an acronym for COordinate Rotation DIgital Computer, algorithm offers an opportunity to calculate the desired functions in a rather simple and elegant way. The CORDIC algorithm was first introduced by Volder [Vol59]. Walter [Wal71] later developed it into a unified algorithm to compute a variety of transcendental functions. Two basic CORDIC modes leading to the computation functions exist, the rotation mode and the vectoring mode. For both modes the algorithm can be realized as an iterative sequence of additions/subtractions and shift operations which are rotations by a fixed rotation angle, but with a variable rotation direction. Due to the simplicity of the operations involved, the CORDIC is very well suited for a VLSI realization ([Sch86], [Dur87], [Lee89], [Not88], [Bu88], [Cav88a], [Cav88b], [Lan88], [Sar98], [Kun90], [Lee92], [Hu92b], [Fre95], [Hsi95], [Phi95], [Ahn98], [Dac98], [Mad99]). It has been implemented in pocket calculators like Hewlett Packard's HP-35 [Coc92], and in arithmetic coprocessors like Intel 8087.

In this thesis, the interest is in the rotation mode, because the QAM modulator (our application) performs a circular rotation (see (2.10)). The basic task performed in the CORDIC algorithm is to rotate a 2 by 1 vector through an angle using a linear, circular or hyperbolic coordinate system [Wal71]. This is accomplished in the CORDIC by rotating the vector through a sequence of elementary angles whose algebraic sum approximates the desired rotation angle.

The CORDIC algorithm provides an iterative method of performing vector rotations by arbitrary angles using only shifts and adds. The algorithm is derived from the general rotation transformation. In Figure 4.1, a pair of rectangular axes is rotated clockwise through the angle *Ang* by the CORDIC algorithm where the coordinates of a vector transform (*I*,*Q*) to (*I'*,*Q'*)

$$\begin{aligned} I' &= I\cos(Ang) + Q\sin(Ang) \\ Q' &= Q\cos(Ang) - I\sin(Ang). \end{aligned} \tag{4.1}$$

which rotates a vector clockwise in a Cartesian plane through the angle *Ang*, as shown in Figure 4.1. These equations can be rearranged so that

$$\begin{aligned} I' &= \cos(Ang)\,[I + Q\tan(Ang)] \\ Q' &= \cos(Ang)\,[Q - I\tan(Ang)]. \end{aligned} \tag{4.2}$$

If the rotation angles are restricted to $\tan(Ang_i) = \pm 2^{-i}$, the multiplication by the tangent term is reduced to a simple shift operation. Arbitrary angles of rotation are obtainable by performing a series of successively smaller elementary rotations. If the decision at each iteration, *i*, is in which direction to rotate rather than whether or not to rotate, then the term $\cos(Ang_i)$ becomes a constant, because $\cos(Ang_i) = \cos(-Ang_i)$. The iterative rotation can now be expressed as

$$I_{i+1} = K_i \left[I_i + Q_i \, d_i \, 2^{-i} \right]$$
$$Q_{i+1} = K_i \left[Q_i - I_i \, d_i \, 2^{-i} \right], \tag{4.3}$$

where $d_i = \pm 1$ and

$$K_i = \cos(\tan^{-1}(2^{-i})) = 1/\sqrt{(1+2^{-2i})}. \tag{4.4}$$

Removing the scale constant from the iterative equations yields a shift-add algorithm for the vector rotation. The product of the K_i's approaches 0.6073 as the number of iterations goes to infinity. The exact gain depends on the number of iterations, and obeys the relation

$$G_n = \prod_{i=0}^{n-1} \sqrt{(1+2^{-2i})}. \tag{4.5}$$

The CORDIC rotation algorithm has a gain, G_n, of approximately 1.647 as the number of iterations goes to infinity.

If both vector component inputs are set to the full scale simultaneously, the magnitude of the resultant vector is 1.414 times the full scale. This, combined with the CORDIC gain, yields a maximum output of 2.33 times the full-scale input.

The angle of a composite rotation is uniquely defined by the sequence of the directions of the elementary rotations. This sequence can be represented by a decision vector. The set of all possible decision vectors is an angular measurement system based on binary arctangents. Conversions between this angular system and others can be accomplished using an additional adder-subtractor that accumulates the elementary rotation angles at each iteration. The angle computation block adds a third equation to the CORDIC algorithm

$$z_{i+1} = z_i - d_i \, \tan^{-1}(2^{-i}). \tag{4.6}$$

The CORDIC algorithm can be operated in one of two modes. The first one, called rotation by Volder [Vol59], rotates the input vector by a specified angle (given as an argument). The second mode, called vectoring, rotates the input vector to the I axis while recording the angle required to make that rotation. The CORDIC circular rotator operates in the rotation mode. In this

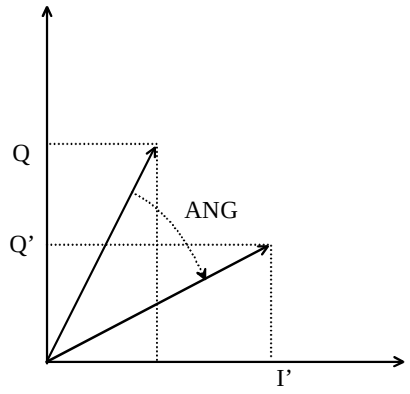

Figure 4.1. Vector rotation.

mode, the angle computation block is initialized with the desired rotation angle. The rotation decision at each iteration is made in order to decrease the magnitude of the residual angle in the angle computation block. The decision at each iteration is therefore based on the sign of the residual angle after each step. The CORDIC equations for the rotation mode are

$$\begin{aligned} I_{i+1} &= I_i + Q_i\, d_i\, 2^{-i} \\ Q_{i+1} &= Q_i - I_i\, d_i\, 2^{-i} \\ z_{i+1} &= z_i - d_i \tan^{-1}(2^{-i}), \end{aligned} \tag{4.7}$$

where d_i = -1 if $z_i < 0$, and +1 otherwise, so that z is iterated to zero. These equations provide the following result, after n iterations

$$\begin{aligned} I_n &= G_n \left[I_0 \cos(A) + Q_0 \sin(A) \right] \\ Q_n &= G_n \left[Q_0 \cos(A) - I_0 \sin(A) \right] \\ G_n &= \prod_{i=0}^{n-1} \sqrt{1 + 2^{-2i}} \\ A &= Ang - z_n, \end{aligned} \tag{4.8}$$

where A is the rotated angle

$$A = \sum_{i=0}^{n-1} d_i \tan^{-1}(2^{-i}). \tag{4.9}$$

The CORDIC rotation algorithm as stated is limited to rotation angles between -π/2 and π/2, because of the use of 2^0 for the tangent in the first iteration. For composite rotation angles larger than π/2, and initializing rotation is required. For example, if it is desired to perform rotations with rotation angles between -π and π, it is necessary to make an initial rotation of ±π/2

$$\begin{aligned} I_0 &= d\, Q_{in}, \\ Q_0 &= -d\, I_{in}, \\ z_0 &= z_{in} - d\ 2 \tan^{-1}(2^0), \end{aligned} \tag{4.10}$$

where d = -1 if $z_{in} < 0$, and +1 otherwise.

4.2 Scaling of I_n and Q_n

The results from the CORDIC operation have to be corrected because of the inherent magnitude expansion in the circular mode. This increases the latency and requires a lot of hardware. Many articles have dealt with this problem and have suggested different methods to reduce the cost of the scaling. Timmermann et al. compares the different approaches in [Tim91].

Each iteration of the CORDIC algorithm extends the vector [I_i Q_i] in the rotational mode. Because of this the resulting vector [I_n Q_n] has to be scaled with the scaling factor G_n given in (4.5). The correction due to the scaling factor can be performed in three different ways:

1. Post-multiplying the result I_n, Q_n or pre-multiplying the input I_0, Q_0 with $1/G_n$. This is the straightforward way to compensate for the scaling factor, and increases the latency with one multiplication.
2. Separate scaling iterations can be included in the CORDIC algorithm, or CORDIC iterations can be repeated, such that the scaling factor becomes a power of two, thus reducing the final scaling operation to a shift operation [Ahm82], [Hav80].
3. The CORDIC iterations can be merged with the scaling factor compensation (as was done in [Bu88]).

The conclusion in [Tim91] is that the third type of scaling tends to increase the overall latency. Therefore to minimize the latency the normal iterations and the scaling should be separated.

In our design the scaling factor is constant, because the number of the iterations is constant. The scaling factor is simply factored into an aggregate processing gain attributed to the filter chain in the QAM modulator (see Figure 2.4).

4.3 Quantization Errors in CORDIC Algorithm

Hu [Hu92a] provided an accurate description of the errors encountered in all modes of the CORDIC operation. In [Hu92a] two major sources of error are identified: the (angle) approximation error and the rounding error. The first type of error is due to the quantized representation of a CORDIC rotation angle by a finite number of elementary angles. The second one is due to the finite precision arithmetic used in a practical implementation. However, the bound for the approximation error has been set without taking into account the effects of the quantization of the angles (the inverse tangents). In [Kot93], the study of the numerical accuracy in the CORDIC includes the accuracy problem with the inverse tangent calculations. The error analysis in [Hu92a] and [Kot93] is based on the assumption that an error reaches its maximum value at each quantization step. This gives quite pessimistic results especially in QAM modulator applications where the I/Q inputs are random signals. In the following discussions only circular rotation mode errors will be treated. The following assumptions concerning the error signal are made:

1. The error signal is a stationary random process
2. The error signal is uncorrelated with the signal to be quantized
3. The sample values of the error process are uncorrelated ; i.e. the error is a white noise process
4. The probability distribution of the error sample values is uniform over the range of the quantization error.

4.3.1 Approximation Error

The equations (4.7) can be rewritten as

$$v_{i+1} = p_i \cdot v_i, \tag{4.11}$$

where $v_i = [I_i\ Q_i]^T$ is the rotation vector at the ith iteration, and

$$p_i = \begin{bmatrix} 1 & d_i 2^{-i} \\ -d_i 2^{-i} & 1 \end{bmatrix} = \sqrt{1+2^{-2i}} \begin{bmatrix} \cos a_i & d_i \sin a_i \\ -d_i \sin a_i & \cos a_i \end{bmatrix} \tag{4.12}$$

is an unnormalized rotation matrix. The magnitude of the elementary angle rotated in the ith iteration is $a_i = \tan^{-1}(2^{-i})$.

In the CORDIC algorithm, each rotation angle A is represented by a restricted linear combination of the n elementary angles a_i (n is the number of iterations), as follows:

$$Ang = \sum_{i=0}^{n-1} d_i\ a_i + z_n = A + z_n, \tag{4.13}$$

where z_n is the error due to this angle quantization. The CORDIC computation error in v_n due to the presence of "z_n" is defined as the approximation error. In the following derivations, infinite precision arithmetic will be applied in order to suppress the effect due to the rounding error.

Conventionally, in the CORDIC algorithm, two convergence conditions will be set [Hu92a]. The first condition states that the rotation angle must be bounded

$$|A| \le \sum_{i=0}^{n-1} a_i \equiv A_{\max}. \tag{4.14}$$

The second condition is set to ensure that if the rotation angle A satisfies (4.14), its angle approximation error will be bounded by the smallest elementary rotation angle a_{n-1}. That is,

$$|z_n| \le a_{n-1}. \tag{4.15}$$

To satisfy this condition, the elementary angle sequence (a_i; i = 0 to i = n-1) must be chosen so that [Wal71]

$$a_i - \sum_{j=i+1}^{n-1} a_j \le a_{n-1}. \tag{4.16}$$

Based on the above result, it is quite obvious that in order to minimize the approximation error, the smallest elementary rotation angle a_{n-1} must be made small. This can be achieved by increasing the number of the CORDIC iterations.

The variance of the approximation error is

$$\delta_{\text{app}}^2 = \frac{a_{n-1}^2}{3} = \frac{(\tan^{-1}(2^{-(n-1)}))^2}{3} \approx \frac{2^{-2(n-1)}}{3}. \tag{4.17}$$

The variance of the approximation error at the CORDIC rotator output is

$$\delta_{a\text{ppr}}^2 = G_n^2 \frac{a_{n-1}^2}{3} \|v_0\|^2 = G_n^2 \frac{a_{n-1}^2}{3} 2\delta^2, \tag{4.18}$$

where δ^2 is the variance of the I_0 and Q_0 data (mean value of I_0 and Q_0 is assumed to be zero), and G_n is from (4.5). An optimal iteration number selection, however, has to take into account the effects of the rounding errors (I, Q datapaths and inverse tangents).

4.3.2 Rounding Error of Inverse Tangents

If the phase accumulator output in Figure 11.5 has a long period (from (2.4)), then the approximation errors are uncorrelated and uniformly distributed within each quantization step

$$-a_{n-1} \le z_n \le a_{n-1}. \tag{4.19}$$

The quantization of the angles is defined as

$$e_i = a_i - Q[a_i], \tag{4.20}$$

where $Q[.]$ denotes the quantization operator and the rounding error is

$$-\frac{2\pi}{2^{ba+1}} \le e_i \le \frac{2\pi}{2^{ba+1}}, \tag{4.21}$$

for a fixed-point angle computation data path with *ba* bits, which is assumed to be greater than the number of iteration stages (n). This is a reasonable assumption because the size of the residual angle becomes smaller in the successive iteration stages, approximately by one bit after each iteration. The variance of this rounding error is

$$\delta_z^2 = \frac{\pi^2\, 2^{-2ba}}{3}. \tag{4.22}$$

The variance of the accumulated rounding error in the angle computation path is

$$\delta_{ze}^2 = \sum_{i=0}^{n-1} \delta_z^2(i) = (n-2)\,\delta_z^2. \tag{4.23}$$

The angle (45°) in the angle computation path could be presented without the quantization error in two's complement format [Gie91] and the last angle iteration has no effect on the rotation direction, therefore (n-2) is used in (4.23). The total variance of the approximation and the accumulated rounding errors at the CORDIC rotator output is

$$\delta_{\text{tot1}}^2 = G_n^2(\delta_{\text{app}}^2 + (n-2)\,\delta_z^2)\,2\,\delta^2. \tag{4.24}$$

4.3.3 Rounding Error of I_n and Q_n

The rounding error of z_n is rather straightforward as it involves only the inner product operation. Hence, the focus will be on the rounding error in I_n and Q_n. The quantization of the error $v_i = [I_i\ Q_i]^T$ is defined as

$$e_i = \begin{bmatrix} I_i \\ Q_i \end{bmatrix} - \begin{bmatrix} Q[I_i] \\ Q[Q_i] \end{bmatrix}, \tag{4.25}$$

where $e_i = [e_i^I\ e_i^Q]^T$ is an error vector due to rounding. For the fixed-point arithmetic, the absolute rounding error will be bounded by

$$\left|e_i^I\right| \le \frac{2^{-bb}}{2}, \qquad \left|e_i^Q\right| \le \frac{2^{-bb}}{2}, \tag{4.26}$$

where *bb* is the number of fractional bits in the angle rotation data path. The variance of the error is

$$\delta_I^2 = \delta_Q^2 = \frac{2^{-2bb}}{12}. \tag{4.27}$$

The variance of the rounding error of I_i and Q_i is

$$\delta_{IQ}^2 = \delta_I^2 + \delta_Q^2 = \frac{2^{-2bb}}{6}. \tag{4.28}$$

In each CORDIC iteration, the rounding error consists of two components: the rounding error propagated from the previous iterations and the rounding error introduced in the present iteration. Therefore the variance due to the rounding error of I_n and Q_n at the CORDIC rotator output is

$$\delta_{\text{tot2}}^2 = \delta_{IQ}^2 \left\{1 + \sum_{j=0}^{n-1} \left\| \prod_{i=j}^{n-1} K_i^2 \right\| \right\}, \tag{4.29}$$

where K_i^2 is $(1 + 2^{-2i})$ from equation (4.12).

4.3.4 Overall Error

The variance of the approximation error and the variance of the rounding error derived above may be combined to yield the overall error variance of the CORDIC computation. These two errors are assumed to be independent. The total variance due to the approximation errors and rounding effects is

$$\delta_{\text{tot}}^2 = \delta_{\text{tot2}}^2 + \delta_{\text{tot1}}^2 = \left\{1 + \sum_{j=0}^{n-1} \left\| \prod_{i=j}^{n-1} K_i^2 \right\| \right\} \frac{2^{-2bb}}{6} + G_n^2 \left(\frac{(a_{n-1})^2}{3} + (n-2)\frac{\pi^2\, 2^{-2ba}}{3}\right) 2\,\delta^2. \tag{4.30}$$

In this equation the term

Table 4.1. Number of the iteration stages in the CORDIC rotator and fractional bits in the data path and their effect on the output error variance.

n	*ba*	*bb*	δ_{tot}^2 from (4.30)	δ_{tot}^2 from (4.32)	Simulated δ_{tot}^2
10	16	15	2.3601e-006	2.3601e-006	2.3828e-006
11	16	15	5.9910e-007	5.9907e-007	5.9833e-007
12	17	16	1.4676e-007	1.4675e-007	1.4700e-007
13	17	16	4.0861e-008	4.0867e-008	4.0566e-008
14	18	17	1.0429e-008	1.0432e-008	1.0308e-008

$$\left\{1+\sum_{j=0}^{n\text{-}1}\left\|\prod_{i=j}^{n\text{-}1}K_i^2\right\|\right\} \tag{4.31}$$

is very close to 1.1792 n for all practical values of n. Thus the result reduces to

$$\delta_{\text{tot}}^2 \approx 1.1792\, n\frac{2^{-2bb}}{6}+G_n^2\left(\frac{2^{-2(n-1)}}{3}+(n-2)\frac{\pi^2\,2^{-2ba}}{3}\right)2\,\delta^2. \tag{4.32}$$

Table 4.1 shows the total variance at the CORDIC output for several values of n, ba and bb. The number of input samples (I/Q data) is 8192. The input data is uniformly distributed over the interval [-1, 1]. The variances from (4.30) and (4.32) agree with the simulated values.

4.3.5 Signal-to-Noise Ratio

The signal-to-noise ratio at the CORDIC rotator output is

$$\frac{S}{N}=\frac{2\,\delta^2}{\left\{1+\sum_{j=0}^{n\text{-}1}\left\|\prod_{i=j}^{n\text{-}1}P_i^2\right\|\right\}\frac{2^{-2bb}}{6}+G_n^2\left(\frac{(a_{n-1})^2}{3}+(n-2)\frac{\pi^2\,2^{-2ba}}{3}\right)2\,\delta^2}. \tag{4.33}$$

where δ^2 is the variance of the I_0 and Q_0 data (the mean of I_0 and Q_0 is assumed to be zero). The signal-to-noise floor ratio is

$$\frac{S}{NF}=\frac{Px\,2\,\delta^2}{\left\{1+\sum_{j=0}^{n\text{-}1}\left\|\prod_{i=j}^{n\text{-}1}P_i^2\right\|\right\}\frac{2^{-2bb}}{6}+G_n^2\left(\frac{(a_{n-1})^2}{3}+(n-2)\frac{\pi^2\,2^{-2ba}}{12}\right)2\,\delta^2}\frac{1}{BW}, \tag{4.34}$$

where BW is the CORDIC output signal bandwidth related to the Nyquist bandwidth. The signal power is assumed to be evenly distributed over the signal bandwidth. Px is the ratio of the signal power that lies in the output signal bandwidth. Figure 4.2 shows the CORDIC output, when

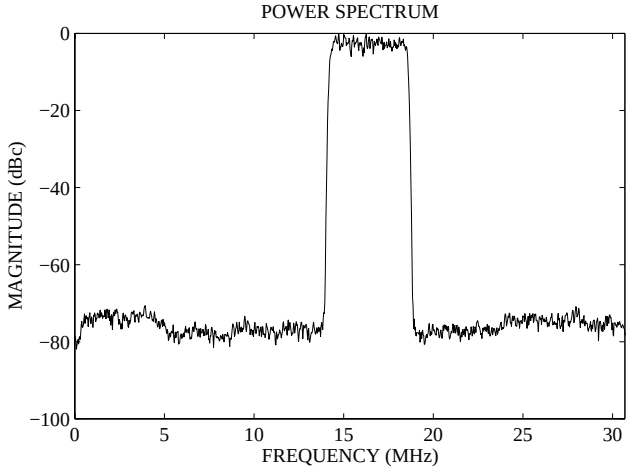

Figure 4.2. CORDIC circular rotator output.

ba is 16 bits, 16 is fractional bits in the I and Q data paths (*bb*), and there are 11 iteration stages (*n*). The signal-to-noise ratio appears to be 64.85 dB. The expected signal-to-noise ratio is 64.90 dB (4.33), which agrees closely with the theoretical value. The signal-to-noise floor ratio appears to be 73.35 dB. The expected signal-to-noise floor ratio is 73.94 dBc (4.34), where *BW* is 0.125 and *Px* is 1. These results agree closely with the theoretical values.

4.4 Redundant Implementations of CORDIC Rotator

The computation time and the achievable throughput of CORDIC processors using conventional arithmetic are determined by the carry propagation involved with the additions/subtractions, since the direction of the CORDIC microrotation is steered by the sign of the previous iteration results. This sign is not known prior to the computation of the MSB. The use of redundant arithmetic is well known to speed up additions/subtractions, because a carry-free or limited carry-propagation operation becomes possible. However, the application of redundant arithmetic in the CORDIC is not straightforward, because a complete word level carry-propagation is still required in order to determine the sign of a redundant number (this also holds for generalized signed digit numbers as described in [Par93]).

In order to overcome this problem, several authors proposed techniques for estimating the sign of the redundant intermediate results from a number of MSDs (most significant digits) ([Erc90], [Erc88], [Tak87]). If the sign, and therefore the rotation direction, cannot be estimated reliably from the MSDs, no microrotation occurs at all. However, the scaling factor involved in the CORDIC algorithm depends on the actual rotations. Therefore here, the scaling factor is variable, and has to be calculated in parallel to the usual CORDIC iteration. Additionally, a division by the variable scaling factor has to be implemented following the CORDIC iteration.

A number of publications dealing with constant scale factor redundant (CSFR) CORDIC implementations of the rotation mode ([Erc90], [Erc88], [Tak87], [Kun90], [Nol91], [Tak91], [Lin90], [Nol90], [Yos89]) describe sign estimation techniques, where every iteration is reactually performed, in order to overcome this problem. However, either a considerable increase (about 50 per cent) in the complexity of the iterations (double rotation method [Tak91]) or a 50 percent increase in the number of iterations (correcting iteration method [Tak91], [Nol90], [Kun90], [Nol91]) occurs.

In [Dup93], a different CSFR algorithm is proposed for the rotation mode. Using this "branching CORDIC", two iterations are performed in parallel if the sign cannot be estimated reliably, each assuming one of the possible choices for the rotation direction. It is shown in [Dup93] that at most two parallel branches can occur. However, this is equivalent to an almost twofold effort in terms of implementation complexity of the CORDIC rotation engine. In contrast to the above mentioned approaches, in [Daw96] transformations of the usual CORDIC iteration are developed resulting in a constant scale factor redundant implementation without additional or

branching iterations. It is shown in [Daw96] that this "Differential CORDIC (DCORDIC)" method compares favorably to the sign estimation methods.

However, the architecture described in this thesis does not use any of these techniques. The adder/subtracters used in the CORDIC rotator unit allow the operation frequency to be reached with carry-ripple arithmetic, and therefore the problem of sign estimation is avoided.

5. Sources of Noise and Spurs in DDS

The model of the noise and spurs in the DDS has six sources. These sources are depicted symbolically in Figure 5.1. The sources are: the truncation of the phase accumulator bits addressing the sine ROM (e_p), a distortion from compressing the sine ROM (e_{COM}), the finite precision of the sine samples stored in the ROM (e_A), the digital-to-analog conversion (e_{DA}), a post-filter (e_F), the phase noise of the clock frequency (n_{clk}), and the frequency error (Δf). The frequency error (Δf) causes a frequency offset (2.2), but not noise and spurs.

5.1 Phase Truncation Related Spu rious Effects

In ideal case, with no phase and amplitude truncation, the output sample sequence of the DDS is given by

$$s(n) = \sin(2\pi \frac{\Delta P}{2^j} n). \tag{5.1}$$

Since the amount of memory required to encode the entire width of the phase accumulator would usually be prohibitive, only k of the most significant bits of the accumulator output are generally used to calculate the sine-wave samples. If the phase accumulator value is truncated to k bits prior to performing the look-up operation, the output sequence must be modified as

$$s(n) = \sin(\frac{2\pi}{2^k}\left[\frac{\Delta P}{2^{j-k}} n\right]), \tag{5.2}$$

where [] denotes truncation to integer values. This may be rewritten as

$$s(n) = \sin(\frac{2\pi}{2^j}(\Delta P n - e_P(n))), \tag{5.3}$$

where $e_P(n)$ is the error associated with the phase truncation. The phase error sample sequence is also restricted in magnitude as

$$e_P(n) < 2^{j-k}, \tag{5.4}$$

and is also periodic with some period. The phase truncation occurs only when GCD (ΔP, 2^j) is smaller than 2^{j-k}. If GCD (ΔP, 2^j) is equal or greater than 2^{j-k}, then the phase bits are zeros below

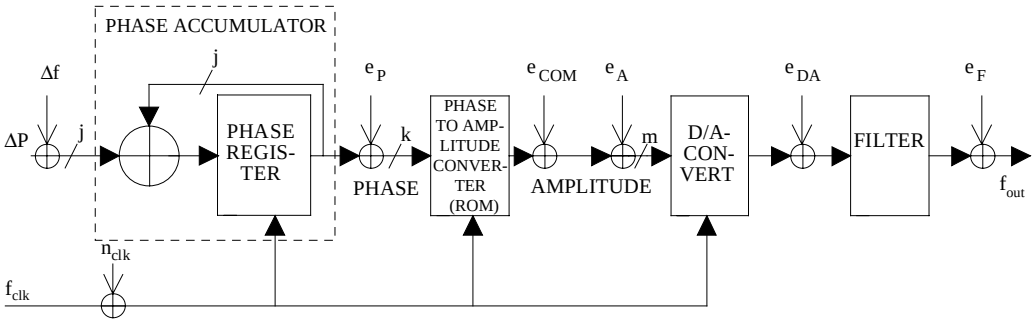

Figure 5.1. Block diagram of the sources of noise and spurs.

2^{j-k} and no phase error occurs.

This sawtooth waveform (see Figure 5.2) is identical to the waveform that would be generated by a phase accumulator of word length (*j-k*) with an input phase increment word of

$$(n\,\Delta P) \bmod 2^{\,j-k}. \tag{5.5}$$

A complete derivation of the phase accumulator truncation effects on the output spectrum is given in [Meh83], [Nic87], [Jen88b]. Although not mentioned in [Meh83], [Nic87], [Jen88b], it is interesting to note what a difference arises when phase accumulator rounding instead of truncation is assumed [Cra94]. Normally, this is never done because the rounding operation would require additional hardware to that required for a simple truncation.

The process of phase truncation occurs in a periodic pattern due to the periodic characteristics of the DDS. Jenq obtains the equivalence of the phase truncation with a non-uniform sampling process [Jen88b]. The phase increment (ΔP) is a number with an integer part W and a fractional part L/M, i.e.

$$\Delta P = W + L / M, \tag{5.6}$$

where L and M have no common factor. The integer part of the address increment register should be set to W, and its fractional part to L/M. Only the integer part of the phase accumulator is supplied to the addressing circuit of the sine ROM; data points sent to the D/A converter are offset from the intended uniform sampling instances except for those where the fractional part of the phase accumulator is zero. Since the ratio of M to L is a prime, M is the smallest integer to make $M\Delta P = M\,(W + L/M)$ an integer. Therefore, the output data sequence is obtained by sampling the sine wave stored in the sine ROM non-uniformly but having an overall period MT_{clk}, where M is

$$M = \frac{2^{\,j-k}}{\mathrm{GCD}(\Delta P, 2^{\,j-k})}, \tag{5.7}$$

and where GCD (ΔP, 2^{j-k}) denotes the greatest common divisor of ΔP and 2^{j-k}. The number of spurs due to the phase truncation is [Nic87]

$$Y = \frac{2^{\,j-k}}{\mathrm{GCD}(\Delta P, 2^{\,j-k})} - 1 = M - 1. \tag{5.8}$$

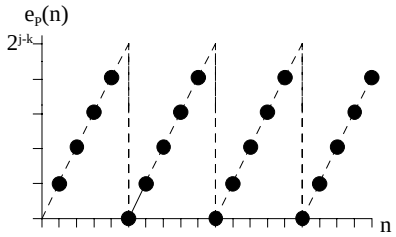

Figure 5.2. Phase accumulator error sequence.

It has been shown in [Jen88a] that if one samples a sinusoidal $e^{j\omega 0t}$ non-uniformly with sampling advancement offsets (i.e. sampling earlier than it should be) $\{t_m\ T_{clk}, m = 0, 1, 2, \ldots M\text{-}1\}$, then the digital spectrum of the sampled waveform is given by

$$G(\omega) = \frac{1}{T_{clk}} \sum_{r=-\infty}^{\infty} A(r)\ 2\pi\,\delta[\omega - \omega_0 - r(2\pi / M T_{clk})], \tag{5.9}$$

where the coefficient $A(r)$ is given by

$$A(r) = \sum_{m=0}^{M-1} \left[\frac{1}{M} e^{-j2\pi t_m f_0 / f_{clk}}\right] e^{-jrm(2\pi/M)}, \tag{5.10}$$

and $f_{clk} = 1/T_{clk}$ and $f_0 = \omega_0/2\pi$.

To utilize (5.9) and (5.10) for this situation, let Δ be the time duration corresponding to

$$(W + L/M)\,\Delta = T_{\text{clk}} \tag{5.11}$$

and let $[x]_{\text{frac}}$ be the fractional part of x, then we have

$$\begin{aligned} t_m / f_{clk} &= t_m\ T_{clk} \\ &= [m(W + L/M)]_{\text{frac}}\,\Delta \\ &= [mL/M]_{\text{frac}}\,\Delta \end{aligned} \tag{5.12}$$

$$f_0 = (W + L/M)\left(\frac{1}{NT_{clk}}\right), \tag{5.13}$$

where N is 2^k (k is the number of bits used to calculate the sine-wave samples).

Hence

$$\begin{aligned} 2\pi\, t_m f_0 / f_{clk} &= 2\pi\,[mL/M]_{\text{frac}} / N \\ &= \frac{2\pi \langle mL \rangle_M}{MN}, \end{aligned} \tag{5.14}$$

where $\langle mL \rangle_M$ stands for mL modulo M. Substituting (5.14) into (5.10), we then have

$$A(r, L, M, N) = \sum_{m=0}^{M-1} \left[\frac{1}{M} e^{-j2\pi \langle mL \rangle_M / (MN)}\right] e^{-jrm2\pi/M}. \tag{5.15}$$

It is noted from (5.15) that the finite sequence [A(r, L, M, N), r = 0, 1,…, M - 1] is the discrete Fourier transform (DFT) of the sequence [(1/M) $e^{-j2\pi tmf0/fclk}$, m = 0, 1,…, M - 1]; therefore, by Parseval's theorem, the sum of the squares of $|\,A(r, L, M, N)\,|$ for r = 0, 1,…, M – 1 is equal to M times the sum of the squares of $|\,(1/M)\ e^{-j2\pi tmf0/fclk}|$ which is unity, i.e.

$$\sum_{r=0}^{M-1} |A(r, L, M, N)|^2 = 1. \tag{5.16}$$

This result is used to calculate the S/N, which is defined as the ratio of the power of the desirable harmonic component to the sum of the powers of the spurious harmonic components, i.e.

$$S/N = 10\log_{10}\left[\frac{|A(0, L, M, N)|^2}{1-|A(0, L, M, N)|^2}\right], \tag{5.17}$$

where $|A(0, L, M, N)|^2$ can be readily obtained from (5.15)

$$|A(0, L, M, N)|^2 = \left[\frac{\sin^2(\pi/N)}{(\pi/N)^2}\,\frac{(\pi/MN)^2}{\sin^2(\pi/MN)}\right]. \tag{5.18}$$

There are three interesting properties of $|A(0, L, M, N)|^2$ worth mentioning:

1) For $M = 1$, $|A(0, L, 1, N)|^2 = 1$, hence there is no spurious harmonic component due to the phase truncation.
2) For a fixed N, $|A(0, L, M, N)|^2$ is a decreasing function of M. Therefore, the S/N is also decreasing on M.
3) For a fixed M, $|A(0, L, M, N)|^2$ is an increasing function of N. Hence, the S/N can be made arbitrarily large by choosing a sufficiently large N.

From the properties listed above, we can have closed-form expressions for both the maximum and the minimum S/N for a fixed N, by making $M = 2$ and ∞, respectively, as follows:

$$S/N(\max) = 20\log_{10}[\cot(\pi/2N)] \tag{5.19}$$

and

$$S/N(\min) = 10\log_{10}\left[\frac{[\sin(\pi/N)/(\pi/N)]^2}{1-[\sin(\pi/N)/(\pi/N)]^2}\right]. \tag{5.20}$$

For a reasonably large N, say $N > 10$ (in practice, N is larger than 1000), (5.19) and (5.20) can be simplified by expanding the arguments of the log function in (5.19) and (5.20) in Taylor's series form, and retaining only the first significant term. By doing so, we obtain

$$\begin{aligned} S/N(\max) &\approx 20\log_{10}(N) - 10\log_{10}(\pi/2) \\ &\approx 6.02k - 3.92 \text{ dB}, \end{aligned} \tag{5.21}$$

and

$$\begin{aligned} S/N(\min) &\approx 20\log_{10}(N) - 10\log_{10}(\pi^2/3) \\ &\approx 6.02k - 5.17 \text{ dB}. \end{aligned} \tag{5.22}$$

Equations (5.21) and (5.22) give very handy and accurate estimates of the S/N as a function of the size of the sine ROM [Jen88b].

The worst-case carrier to the spur ratio due to the phase truncation occurs when $r = 1$ and $M = 2$

$$\frac{C}{S}(\min) = 20\log_{10}\left[\frac{A(0, L, 2, N)}{A(1, L, 2, N)}\right] = 20\log_{10}\left[\cot(\frac{\pi}{2N})\right]. \quad (5.23)$$

The carrier to spur ratio due to the phase truncation when $r = 1$ and $M = \infty$ ($2^{j-k} >> \mathrm{GCD}(\Delta P, 2^{j-k})$ in (5.7)) is given by

$$\frac{C}{S}(\max) = 20\log_{10}\left[\frac{A(0, L, \infty, N)}{A(1, L, \infty, N)}\right] = 20\log_{10}[N+1]. \quad (5.24)$$

For a reasonably large N, say $N > 10$ (in practice, N is larger than 1000), (5.23) can be simplified by expanding the argument of the log function in (5.23) in Taylor's series form and retaining only the first significant term. By doing so, we obtain the worst-case carrier to spur ratio

$$\frac{C}{S}(\min) \approx 20\log_{10}(N) - 20\log_{10}\left[\frac{\pi}{2}\right] \approx 6.02k - 3.92 \text{ dB}. \quad (5.25)$$

The carrier to spur ratio due to the phase truncation when $r = 1$ and $M = \infty$ (from (5.24)) is

$$\frac{C}{S}(\max) \approx 20\log_{10}(N) = 6.02k. \quad (5.26)$$

The phase truncation error analysis in [Jen88b] is extended here so that it includes the worst-case carrier to spur ratio bounds ((5.25) and (5.26)). The spur power is concentrated in one peak in Figure 7.2, because M is 2 (5.8). The worst-case carrier-to-spur level due to the phase truncation appears to be 44.24 dBc. The expect worst-case carrier-to-spur value is 44.17 dBc (5.25), which agrees closely. If M is larger than 2, the spur power is spread over many peaks (see Figure 7.3). The number of spurs is 15 from (5.8) in Figure 7.3. Since $M = 16$ for this case, the expected worst-case carrier-to-spur value is approximately 48.16 dBc (5.26). The worst-case carrier-to-spur level due to the phase truncation appears to be 48.08 dBc.

5.2 Finite Precision of Sine Samples Stored in ROM

Finite quantization in the sine ROM values also leads to the DDS output spectrum impairments. If it is assumed that the phase truncation does not exist, then the output of the DDS is given by

$$\sin(\frac{2\pi}{2^j}(\Delta P\, n)) - e_A(n), \quad (5.27)$$

where $e_A(n)$ is the quantization error due to the finite sine ROM data word. The sequence of the ROM quantization errors is periodic, repeating every Pe samples (2.4). There are two limiting cases to consider i.e. the numerical period of the output sequence (Pe) is either long or short.

In the first case, the quantization error results in what appears to be a white noise floor, but is actually a "sea" of very finely spaced discrete spurs. The amplitude quantization errors can be assumed to be totally uncorrelated and uniformly distributed within each quantization step,

$$-\frac{\Delta_A}{2} \le e_A \le \frac{\Delta_A}{2}, \quad (5.28)$$

where the quantization step size is

$$\Delta_A = \frac{1}{2^m}, \tag{5.29}$$

and where m is the word length of the sine values stored in the sine ROM. Then the amplitude error power is [Ben48]

$$E\{e_A^2\} = \frac{1}{\Delta_A} \int_{-\frac{\Delta_A}{2}}^{\frac{\Delta_A}{2}} e_A^2 \, de_A = \frac{\Delta_A^2}{12}. \tag{5.30}$$

The signal power of the sine wave is

$$P_A = \frac{A^2}{2}, \tag{5.31}$$

where A is the amplitude of the sine wave. The DDS output is an odd function, therefore the spectrum of the amplitude error only contains odd frequency components (Pe/2 spurs). The sinusoid generated is a real signal, so its power is equally divided into negative and positive frequency components. Using these facts and ignoring the sinc-function effect (A.6), the carrier-to-spur power spectral density is approximately

$$\left(\frac{C}{S}\right) = 10 \times \log_{10}\left(\frac{P_A}{E\{e_A^2\}} \times \frac{Pe}{4}\right) = (1.76 + 6.02\,m + 10 \times \log_{10}\left(\frac{Pe}{4}\right)) \text{ dBc.} \tag{5.32}$$

In the second case, there will be no quantization errors if the samples match exactly the quantization levels, e. g., $f_{out} = f_{clk}/4$. The assumption that the error is evenly distributed in one period is really not valid due to the shortness of the period. Assuming that the amplitude error gets its maximum absolute value ($\Delta_A/2$) at every sampling instance and all the energy is in one spur, the carrier-to-spur ratio is

$$\left(\frac{C}{S}\right) = 10 \times \log_{10}\left(\frac{4P_A}{\Delta_A^2}\right) = (-3.01 + 6.02\,m) \text{ dBc.} \tag{5.33}$$

However, simulations indicate that in the worst-case the sum of the discrete spurs is approximately equal to

$$\left(\frac{C}{S_{sum}}\right) = \left(\frac{P_A}{E\{e_A^2\}}\right) = (1.76 + 6.02\,m) \text{ dBc.} \tag{5.34}$$

5.3 Distribution of Spurs

The phase accumulator can be considered as a permutation generator, where each value of ΔP provides a different permutation of the values from 0 to 2^j - 1 given by

$$_{\Delta P}P(n) = (n\,\Delta P) \bmod 2^j. \tag{5.35}$$

Any phase accumulator output vector can be formed from the permutation of another output vector, regardless of the initial phase accumulator contents, when GCD(ΔP, 2^j) = 1 for all values of ΔP (Figure 5.3). In Figure 5.4 the time vectors are formed from values which have the property GCD(ΔP, 2^j) = 2. From this figure it is evident that the phase accumulator is now char-

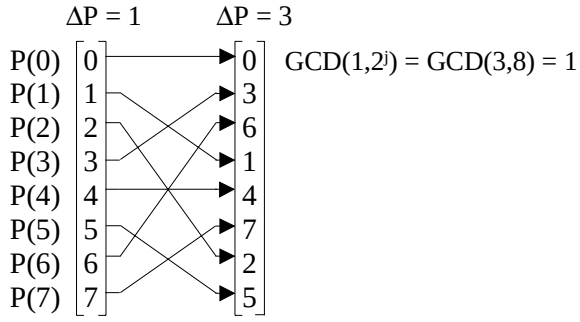

Figure 5.3. Time series vectors for a 3-bit phase accumulator for $\Delta P = 1$ and $\Delta P = 3$. The column vector for $\Delta P = 3$ can be formed from a permutation of the values of the $\Delta P = 1$ vector, regardless of the initial phase accumulator contents.

acterized by having two different sets of possible output vectors, depending on the initial contents of the phase accumulator.

The time output vector for ΔP can be formed from a permutation of the individual elements of the vector for $\Delta P = 1$,

$$_{\Delta P}P(n) = {}_1P((n\Delta P) \bmod 2^j), \tag{5.36}$$

where ΔP and 2^j are relatively prime. As in (5.36), all input time vectors may be formed from a permutation of another time vector by permuting the indices using $(n\Delta P) \bmod 2^j$. The converse follows from the existence of a unique integer $0 \le J < 2^j$ satisfying the relation

$$\Delta P\ J \bmod 2^j = 1. \tag{5.37}$$

This is a fundamental result of number theory which requires that ΔP and 2^j are relatively prime [McC79]. In a sense J is the multiplicative inverse of ΔP. From the above equation it follows that ΔP and J must be odd because 2^j is even. Therefore J and 2^j are relatively prime, too.

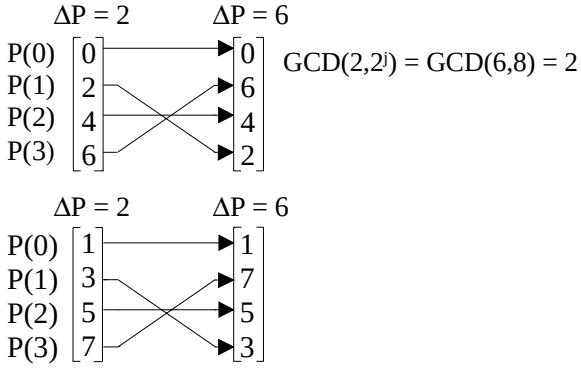

Figure 5.4. Time series vectors for a 3-bit accumulator for $\Delta P = 2$ and $\Delta P = 6$.

The DDS with a sinusoidal output operates by applying some memoryless non-linear function $s\{\}$ to the phase accumulator output to produce the sine function. The DFT of the phase to amplitude converter output using (5.36) is

$$S\{_{\Delta P}\, P(m)\} = \sum_{n=0}^{2^j-1} s\{_1 P((n\Delta P) \bmod 2^j)\} W_{2^j}^{mn} \quad m = 0, 1, \ldots, 2^j - 1, \qquad \text{where } W_{2^j} = e^{-j2\pi/2^j}, \tag{5.38}$$

and 2^j is the period of the phase accumulator when ΔP and 2^j are relatively prime (2.4). (5.37) can be used to show that permutation samples in the time domain produce the same type of permutation in the frequency domain by defining the new index

$$q = (n\Delta P) \bmod 2^j, \tag{5.39}$$

and noting that

$$\begin{aligned} qJ \bmod 2^j &= J((n\Delta P) \bmod 2^j) \bmod 2^j \\ &= n\,\Delta P\, J \bmod 2^j. \end{aligned} \tag{5.40}$$

Substituting from (5.37), (5.40) becomes

$$n = qJ \bmod 2^j. \tag{5.41}$$

Re-indexing (5.38) using (5.39) and (5.41), then

$$\begin{aligned} S\{_{\Delta P}\, P(m)\} &= \sum_{q=0}^{2^j-1} s\{_1 P(q)\} W_{2^j}^{m(qJ \bmod 2^j)} \\ &= \sum_{q=0}^{2^j-1} s\{_1 P(q)\} W_{2^j}^{q(mJ \bmod 2^j)} \\ &= S\{_1 P((mJ) \bmod 2^j)\} \quad m = 0, 1, \ldots, 2^j - 1. \end{aligned} \tag{5.42}$$

The above equation establishes that the permutation of the samples in the time domain results in

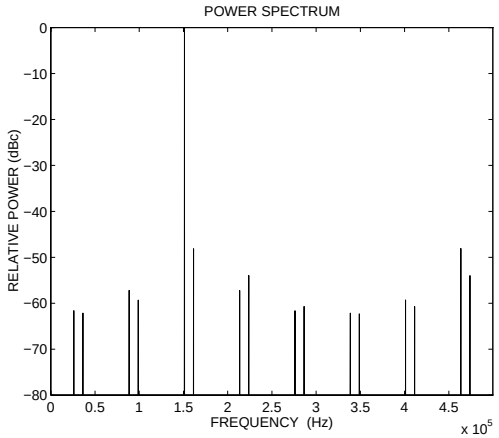

Figure 5.5. Discrete Fourier transform of the DDS output sequence for j = 12, k = 8 and ΔP = 619.

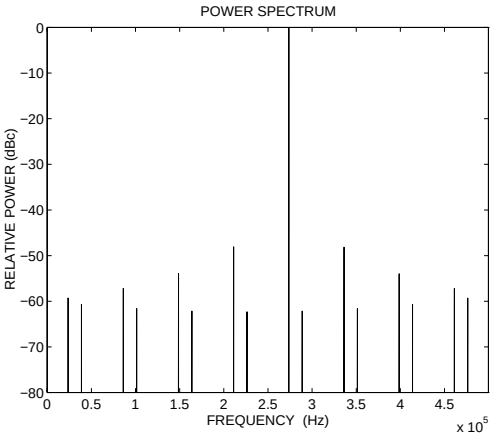

Figure 5.6. Discrete Fourier transform of the DDS output sequence for j = 12, k = 8 and ΔP = 1121.

the same type of permutation of the DFT samples in the frequency domain, because J and 2^j are relatively prime. This means that the spurious spectrum due to all system non-linearities can be generated from a permutation of another spectrum, when GCD (ΔP, 2^j) = 1 for all ΔP, because each spectrum will differ only in the position of the spurs and not in the magnitudes.

Two ΔP values 619 and 1121 are considered in the example. The DFT of the DDS output sequence for ΔP = 619 is shown in Figure 5.5, where the worst-case carrier-to-spur level due to the phase truncation appears to be 48.08 dBc. Since M >> 2 for this case, the expected worst-case carrier-to-spur value is 48.16 dBc (5.26), which agrees closely. The number of spurs in the figures is 15, from (5.8). The DFT spectrum for the second frequency case of ΔP = 1121 is shown in Figure 5.6. As predicted, since GCD (ΔP, 2^j) = 1 for this case as well, the worst-case

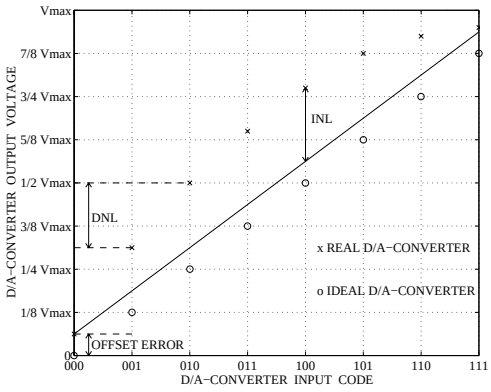

Figure 5.7. Differential (DNL), integral non-linearity (INL) and offset error.

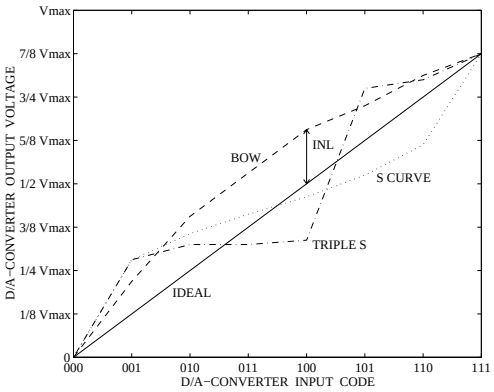

Figure 5.8. Transfer functions represented by the "bow", "S", and "triple-S" curves have the same INL measurement but a different frequency-domain effect.

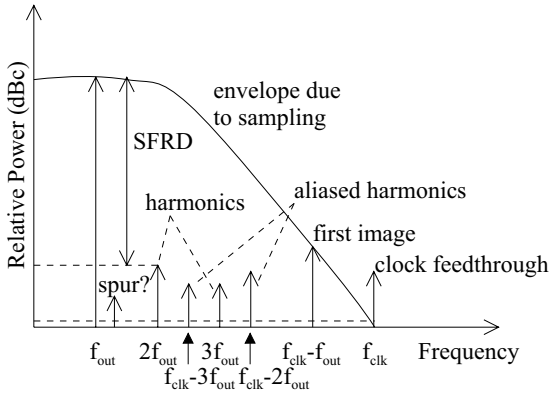

Figure 5.9. The true D/A-converter output spectrum includes not only quantization noise and images, but also harmonics, spurious distortion and clock feedthourgh.

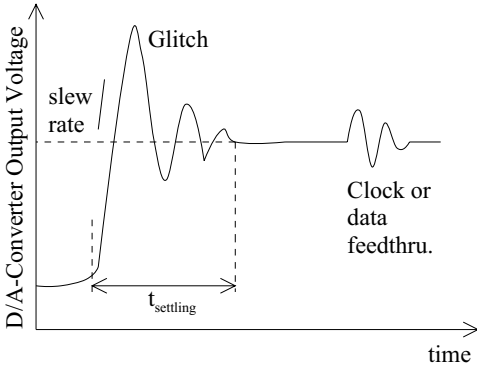

Figure 5.10. Glitch impulse and settling time.

carrier-to-spur level is unchanged and only the position of the spurs has been permutated.

5.4 D/A-Converter Errors

In high-speed and high-resolution (>10 bits, >50 MHz) DDSs, most of the spurs are generated less by digital errors (truncation or quantization errors), and more by analog errors in the D/A converter and the lowpass filter such as clock feedthrough, intermodulation, and glitch energy. The specifications of the D/A-converter are studied in detail because the D/A-converter is the critical component. Figure 5.7 illustrates an ideal and an actual transfer function for a 3-bit D/A-converter. Manufacturers typically specify offset, gain error, differential and integral non-linearity (DNL and INL) as approximations to this transfer function [Beh93]. The offset error, the gain error, INL and DNL are defined as static specifications. The output offset is usually defined as a constant DC offset in the transfer curve. The gain defines the full-scale output of the converter in relation to its reference circuit [Buc92]. The DNL is typically measured in the LSBs as the worst-case deviation from an ideal LSB step between adjacent code transitions. It can be a negative or a positive error. The D/A-converters, which have a DNL specification of less than -1 LSB, are not guaranteed to be monotonic. The INL is measured as the worst deviation from a straight-line approximation to the D/A-converter transfer function. Like the DNL specification, the INL measurement is a worst-case deviation. It does not indicate how many D/A-converter codes reach this deviation or in which direction away from the best straight line the deviation occurred. Figure 5.8 illustrates how this specification might be misinterpreted. Each of the curves represents a transfer curve having the same INL measurement but a different effect in the frequency domain. For example, the function corresponding to the "bow" in the INL curve will introduce a second-harmonic distortion, while the symmetrical "S curve" will tend to introduce a third-harmonic distortion. The SFDR specification defines the difference in the power between the signal of interest and the worst-case (highest) power of any other signal in the band of interest, Figure 5.9.

The AC specifications are settling time, output slew rate, and glitch impulse. The settling time should be measured as the interval from the time the D/A-converter output leaves the error band around its initial value to settling within the error band around its final value. The slew rate is a rate at which the D/A output is capable of changing [Zav88b]. A difference between a rising and falling slew rate produces spurious distortion. The glitch impulse, often considered an important key in DDS applications, is simply a measure of the initial transient response (overshoot) of the D/A-converter between the two output levels, Figure 5.10. The glitches become more significant as the output frequency increases [Sau93]. It is assumed that the glitch occurs only in one code transition. When the output frequency is low, there are many samples per the output cycle; and the glitch energy compared with the signal energy is low. When the output frequency is high, there are few samples per output cycle (example 000, 100, 000...). Consequently, the D/A-converter spurious content can be expected to degrade at higher frequencies. Of course there are high output frequencies, where the 'bad samples' do not occur. Transients

can cause ringing on the rising and/or falling edges of the D/A converter output waveform. Ringing tends to occur at the natural resonant frequency of the circuit involved and may show up as spurs in the output spectrum.

The anomalies in the output spectrum, such as the INL and DNL errors of the D/A converter, glitch energy associated with the D/A converter, and clock feed-through noise, will not follow the sin(X)/X roll-off response (see (2.5)). These anomalies will appear as harmonics and spurious energy in the output spectrum. The noise floor of the DDS is determined by the cumulative combination of substrate noise, thermal noise effects, ground coupling, and a variety of other sources of low-level signal corruption.

Various techniques have been used to attain full n-bit static linearity for n-bit D/A converters. These techniques have included sizing the devices appropriately for intrinsic matching, and utilization of certain layout techniques [Bas98], [Pla99], trimming [Mer94], [Tes97], calibration [Gro89], and dynamic element matching/averaging techniques [Moy99]. The static linearity is in general a prerequisite for obtaining a good dynamic linearity. For high-speed and high-resolution applications (>10 bits, >50 MHz), the current source switching architecture is preferred since it can drive a resistive load directly without the need for a voltage buffer. The dynamic performance of the current-switched D/A converter is degraded as the output frequency increases in Figure 9.12. There are several causes for this behavior; the major ones are summarized below.

1) Code-dependent settling time constants: The time constants of the MSB's, and LSB's are typically not proportional to the currents switched.
2) Code-dependent switch feedthrough: This results from the signal feedthrough across switches not being sized proportionately to the currents they are carrying, and therefore shows up as code-dependent glitches at the output.
3) Timing skew between current sources: Imperfect synchronization of the control signals of the switching transistors will cause dynamic non-linearities [Bas98]. Synchronization problems occur both because of delays across the die and because of improperly matched switch drivers. Thermometer decoding can make the time skew worse because of the larger number of segments [Mer94].
4) Major carry glitch: This can be minimized by thermometer decoding, but in higher resolution designs, where full thermometer decoding is not practical, it cannot be entirely eliminated [Lin98].
5) Current source switching: Voltage fluctuations occur at the internal switching nodes of the sources of the switching devices [Bas98]. Since the size of the fluctuation is not proportional to the size of the currents being switched, it again gives rise to a non-linearity.
6) On-chip passive analog components: Drain/source junction capacitances are non-linear; on-chip analog resistors also exhibit non-linear voltage transfer characteristics. These devices therefore cause dynamic non-linearities when they occur in analog signal paths.

7) Mismatch considerations: Device mismatch is usually considered in discussions of static linearity, but it also contributes to dynamic non-linearity because switching behavior is dependent on switch transistor parameters such as threshold voltage and oxide thickness. These differ for devices at different points on the die [Pel89], [Ste97], introducing code dependencies in the switching transients.

Alternatives to the current mode D/A converter have been proposed in the literature (for example, [Kha99]), but they are limited by the use of op-amps and/or low-impedance followers as output buffers. OP-amps introduce several dynamic non-linearities of their own, owing to their non-linear transconductance transfer functions (slew limiting in the extreme case). High-gain op-amps connected in feedback configurations also require buffers to drive lower impedance resistive loads. Buffers introduce further distortion, due to factors such as signal dependence of the bias current in the buffer devices and non-linear buffer output resistance.

One conceptual solution to the dynamic linearity problem is to eliminate the dynamic non-linearities of the D/A converter, all of which are associated with the switching behavior, by placing a track/hold circuit at the D/A converter output. The track/hold would hold the output constant while the switching is occurring, and track once the output has settled to their dc value. Thus, only the static characteristics of the D/A converter would show up at the output, and the dynamic ones would be attenuated or eliminated. The problem with this approach is that the track/hold circuit in practice introduced dynamic non-linearities of its own. A different approach, employing a return-to-zero (RZ) circuit at the output, is proposed in [Bug99]. The output stage implements a RZ action, which tracks the D/A converter once it has settled and then returns to zero. The problems of this approach are: large voltage steps cause extreme jitter sensitivity, large steps cause problems for the analog lowpass filter, and the output range (after filtering) is reduced by a factor of 2. To remedy these problems, current transients are sampled to an external dummy resistor load RD, and settled current to external output resistor loads RP and RN, by multiplexing two D/A converters [Bal87], as shown in Figure 13.15. The two D/A converters are sampled sequentially at half clock rate.

A problem inherent in mixed signal chips is switching noise. To minimize the coupling of the switching noise from the digital logic to the D/A converter output, the power supplies of the digital logic and the analog part are routed separately. To reduce the supply ripples further, additional supply and ground pins are used to reduce the overall inductance of packaging. On-chip decoupling capacitors are used to reduce the ground bounce in the digital part. A source of noise injection into the substrate exists since the digital power/ground supply is common to the substrate power/ground tie in cell libraries. To remedy this problem, a separate clean digital substrate power/ground line should be routed to all digital circuits in addition to the regular noisy power/ground supply. However this is not usually possible when standard cell libraries are used. In the D/A converter the current source and switch transistors (see Figure 12.4) should be put in the separate wells. The cell libraries of conventional (single-ended) static and dynamic

CMOS cells should be converted into differential implementations, which tend to generate substantially less switching noise. If the substrate is low ohmic, then the most efficient way to decrease the noise coupling through the substrate is to reduce the inductance in the substrate bias [Su93]. If the substrate is high ohmic, then separate guard rings and physical separation appear to be effective ways of decreasing the noise coupling to the analog output through the substrate [Su93]. A low inductance biasing increases the effectiveness of the guard rings [Su93]. The D/A converter should be implemented with a differential design, which results in reduced even-order harmonics and provides common-mode rejection to disturbances. Disturbances connected to the external bias should be filtered out on-chip with a low-pass filter.

Many mixed signal designs include one and more high frequency clocks on the chip. It is not uncommon for these clock signals to appear at the D/A-converter output by means of capacitive or inductive coupling. Any coupling of the clock signals into the D/A-converter output will result in spectral lines at the frequencies of the inferring clock signals. The feedthrough of data transitions to the D/A-converter output also adds to the frequency content of the output spectrum. Another possibility is that the clock signal is coupled to the D/A-converter's sample clock. This causes the D/A-converter output signal to be modulated by the clock signal. Proper layout and fabrication techniques are the only insurance against these forms of spurious contamination. These effects are also often related to the test circuit layout, and can be minimized with good layout techniques [McC91a]. Therefore, the only reliable method for obtaining knowledge about the spectral purity is to have the D/A-converter characterized in the laboratory.

5.5 Phase Noise of DDS Output

Leeson has developed a model that describes the origins of phase noise in oscillators [Lee66], and since it closely fits experimental data, the model is widely used in describing the phase noise of the oscillators [Roh83], [Man87]. In the model the clock signal (oscillator output) is phase modulated by a sine wave of frequency f_m

$$y_{clk}(t) = \cos(\omega_{clk} t + \beta \sin \omega_m t), \tag{5.43}$$

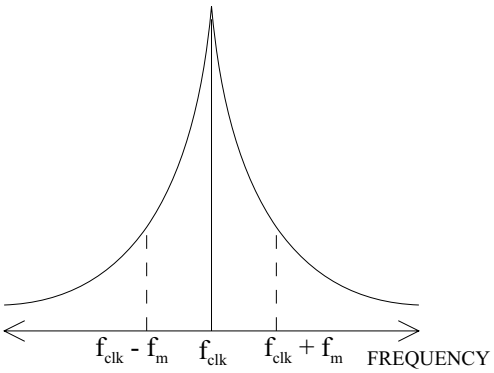

Figure 5.11. Typical phase noise sidebands of an oscillator.

ω_{clk} is the clock frequency of DDS, β is the maximum value of the phase deviation, ω_m is the offset frequency. The spectrum of the clock signal is shown in Figure 5.11.

The frequency of the clock signal is

$$f_{clk}(t) = \frac{1}{2\pi}\frac{d(\theta_{clk}(t))}{dt} = \frac{1}{2\pi}(\omega_{clk} + \beta\omega_m \cos\omega_m t). \tag{5.44}$$

The DDS could be described as a frequency divider, and so the output frequency of the DDS is

$$f_{out}(t) = \frac{\Delta P\, f_{clk}(t)}{2^j} = \frac{f_{clk}(t)}{N} = \frac{1}{2\pi}(\omega_{out} + \frac{\beta}{N}\omega_m \cos\omega_m t), \tag{5.45}$$

where j is the word length of the DDS phase accumulator, ΔP is the phase increment word, N is the division ratio. The phase of the DDS output is

$$\theta_{out}(t) = (\omega_{out} t + \frac{\beta}{N}\sin\omega_m t), \tag{5.46}$$

and the DDS output is

$$y_{out}(t) = \cos(\omega_{out} t + \frac{\beta}{N}\sin\omega_m t). \tag{5.47}$$

Comparing (5.43) and (5.47), the modulation index is changed from β to β/N, but the offset frequency is not changed. The spectrum of the DDS clock is given by inspection from the equivalent relationship

$$\begin{aligned} y_{clk}(t) &= \cos(\omega_{clk} t + \beta \sin\omega_m t) = \mathrm{Re}\left\{e^{j\omega_{clk}t} e^{j\beta\sin\omega_m t}\right\} \\ &= \mathrm{Re}\left\{e^{j\omega_{clk}t}\sum_{i=-\infty}^{\infty} J_i(\beta) e^{ji\omega_m t}\right\} = \sum_{i=-\infty}^{\infty} J_i(\beta)\cos(\omega_{clk} t + i\omega_m t), \end{aligned} \tag{5.48}$$

where $J_i(\beta)$ are Bessel functions of the first kind. The spectrum of the DDS output is given by inspection from the equivalent relationship

$$\begin{aligned} y_{out}(t) &= \cos(\omega_{out} t + \frac{\beta}{N}\sin\omega_m t) = \mathrm{Re}\left\{e^{j\omega_{out}t} e^{j\frac{\beta}{N}\sin\omega_m t}\right\} \\ &= \mathrm{Re}\left\{e^{j\omega_{out}t}\sum_{i=-\infty}^{\infty} J_i(\frac{\beta}{N}) e^{ji\omega_m t}\right\} = \sum_{i=-\infty}^{\infty} J_i(\frac{\beta}{N})\cos(\omega_{out} t + i\omega_m t). \end{aligned} \tag{5.49}$$

The relative power of the DDS output phase noise at offset $i\omega_m$ is from (5.48) and (5.49)

$$\frac{P_{out_i}}{P_{clk_i}} = \left(\frac{J_i(\frac{\beta}{N})}{J_i(\beta)}\right)^2. \tag{5.50}$$

If $\beta << 1$, then $J_0(\beta) \approx 1$, $J_0(\beta/N) \approx 1$, $J_1(\beta) \approx \beta/2$, $J_1(\beta/N) \approx \beta/(2N)$ and $J_i(\beta) \approx 0$ (i = 2, 3...), and

$$\left(\frac{P_{out_1}}{P_{clk_1}}\right)_{\mathrm{dB}} \approx -20\times\log_{10}(N)\ [\mathrm{dB}]. \tag{5.51}$$

From the above equation the relative power level of the DDS output phase noise depends on the ratio between the output frequency and clock frequency. The output signal will exhibit the improved phase noise performance

$$n_{clk} - 20 \times \log_{10}(\frac{f_{clk}}{f_{out}}). \quad (5.52)$$

The DDS circuitry has a noise floor, which at some point will limit this improvement. An output phase noise floor of -160 dBc/Hz is possible, depending on the logic family used to implement the DDS [Qua90]. The frequency accuracy of the clock is propagated through the DDS [Qua90]. Therefore, if the clock frequency is 0.1 PPM higher than desired, the output frequency will be also higher by 0.1 PPM.

Figure 9.14 shows the spectrum of the clock source at 150 MHz. Figure 9.15 shows the spectrum of 15 MHz output sine wave, where the clock frequency is 150 MHz. The relative phase noise level should improve by 20 dB ($20 \times \log_{10}(10)$) (5.52). The relative power level of the phase noise at the offset of 130 kHz from the carrier is about 42.5 dBc in Figure 9.14 and 64.2 dBc in Figure 9.15. The relative improvement in the close-in phase noise agrees with the theory.

5.6 Post-filter Errors

The sixth source of noise at the DDS output is the post-filter, e_F, which is needed to remove the high frequency sampling components. Since this post-filter is an energy storage device, the problem of the response time arises. The filter must have a very flat amplitude response and a constant group delay across the bandwidth of interest so that the perfectly linear digital modulation and frequency synthesis advantages are not lost. The output filter also affects the switching time of the DDS output.

6. Blocks of Direct Digital Synthesizer

The DDS is shown in a simplified form in Figure 2.1. In this chapter the blocks of the DDS are investigated: phase accumulator, phase to amplitude converter and filter. The D/A converter was described in Section 5.4. The methods of accelerating the phase accumulator are described in detail. Different sine memory compression and algorithmic techniques and their trade-offs are investigated.

6.1 Phase Accumulator

In practice the phase accumulator circuit cannot complete the multi-bit addition in a short single clock period, because of the delay caused by the carry bits rippling through the adder. In order to provide the operation at higher clock frequencies, one solution is a pipelined accumulator [Cho88], [Ekr88], [Gie89], [Lia97], shown in Figure 9.2. To reduce the number of the gate delays per clock period, a kernel 4-bit adder is used in Figure 9.2, and the carry is latched between successive adder stages. In this way the length of the accumulator does not reduce the maximum operating speed. To maintain the valid accumulator data during the phase increment word transition, the new phase increment value is moved into the pipeline through the delay circuit. All the bits of the input phase increment word must be delay equalized. The phase increment word delay equalization circuitry is thus very large. The number of D-flip-flops (DFFs) needed in this delay equalization is given by the formula [Che92]

$$\frac{B \times (PS^2 + PS)}{2}, \tag{6.1}$$

where B is the number of bits per pipelined stage, and PS is the number of the pipelined stages. For example, in Figure 9.2, a 32-bit accumulator with 4-bit pipelined segments requires 144 D-flip-flops for input delay equalization alone. These D-flip-flop circuits would impact the loading of the clock network. To reduce the number of pipeline stages a carry increment adder (CIA) in Section 10.4.1 and conditional sum adder in [Tan95b] are used. To reduce the cycle time and size of pipeline stages further, the outputs of the adder and the D-flip-flops could be combined to form “logic-flip-flop” (L-FF) pipeline stages [Yua89], [Rog96] (see Section 10.4.1); thereby their individual delays are shared, resulting in a shorter cycle time and smaller area.

Pre-skewing latches with pipeline control are used to eliminate the large number of D-flip-flops required by the input delay equalization registers [Che92], [Lu93], [Ert96]. The cost of this simplified implementation is that the frequency can be updated only at f_{clk}/PS, where PS is the number of the pipelined stages.

The phase increment inputs to the phase accumulator are normally generated by a circuitry that runs from a clock that is much lower in frequency than, and often asynchronous to, the DDS

clock. To allow this asynchronous loading of the phase increment word, double buffering is used at the input of the phase accumulator.

The output delay circuitry is identical to the input delay equalization circuitry, inverted so that the low-order bits receive a maximum delay while the most significant bits receive the minimum delay. In Figure 9.2 the data from the most significant 12 bits of the phase accumulator are delayed in pipelined registers to reach the phase to amplitude converter with full synchronization. A hardware simplification is provided by eliminating the de-skewing registers for the least significant *j-k* bits of the phase accumulator output. This is possible because only the *k* most significant phase bits are used to calculate the sine function. The only output bits that have to be delay equalized are those that form the address of the phase to amplitude converter.

The processing delay is from the time a new value is loaded into the phase register to the time when the frequency of the output signal actually changes, and the pipeline latency associated with frequency switching is 9 clock pulses, see Figure 9.2. In [Tho92] a look-ahead technique, rather than pipelining, was incorporated into the phase accumulator to reduce the frequency-tuning latency, but the phase increment word must be constant for four accumulator cycles for this method. The use of parallel phase accumulators to attain a high throughput has been utilized in [Gol90], [Tan95b]. The phase accumulator could be accelerated by introducing a Residue Number System (RNS) representation into the computation, and eliminating the carry propagation from each addition [Chr95]. The conversion and the re-conversion to/from the RNS representation reduces the gain in the computation speed.

The frequency resolution is from (2.2), when the modulus of the phase accumulator is 2^j. Few techniques have been devised to use a different modulus [Jac73], [Gol88], [McC91b], [Gol96], [Uus00]. The penalty of those designs is a more complicated phase address decoding [Gol96]. The benefit is a more exact frequency resolution (the divider is not restricted to a power of two in (2.2)), when the clock frequency is fixed [Gol96]. For example, 10 MHz is the industry standard for electronic instrumentation requiring accurate frequency synthesis [McC91b]. To achieve one hertz resolution in these devices, it is required to set the phase accumulator modulus equal to 10^6 (decimal) [Jac73], [Gol88]. The modulus of the phase accumulator is not necessarily a power of two or decimal in [McC91], [Uus00]. In this thesis the modulus of the phase accumulator is 2^j. The DDS is used to compensate the drifts of the local oscillator, so exact frequency resolution is not known beforehand.

6.2 Phase to Amplitude Converter

The spectral purity of the conventional direct digital synthesizer (DDS) is also determined by the resolution of the values stored in the sine table ROM. Therefore, it is desirable to increase the resolution of the ROM. Unfortunately, a larger ROM storage means higher power consumption, lower speed and greatly increased costs.

The most elementary technique of compression is to store only π/2 rad of sine information, and to generate the ROM samples for the full range of 2π by exploiting the quarter-wave symmetry of the sine function. After that, methods of compressing the quarter-wave memory include: a trigonometric identity, Nicholas' method, the Taylor series or the CORDIC algorithm. A different approach to the phase-to-sine-amplitude mapping is the CORDIC algorithm, which uses an iterative computation method. The costs of the different methods are an increased circuit complexity and distortions that will be generated, when the methods of memory compression are employed. Because the possible number of generated frequencies is large, it is impossible to simulate all of them to find the worst-case situation. If the least significant bit of the phase accumulator input is forced to one, then only one simulation is needed to determine the worst-case carrier-to-spur level (see Section 5.3). In this chapter 14-bit phase to 12-bit amplitude mapping is investigated. This mapping is used in the multi-carrier GMSK modulator in Chapter 13. The results are only valid for these requirements. Some examples of commercial circuits using the above methods are also presented.

A non-linear D/A-converter is used in the place of the sine ROM look-up table for the phase-to-sine amplitude conversion and linear D/A converter [Bje91], [Mor99]. The drawback of this technique is that the digital amplitude modulation cannot be incorporated into the DDS. In this thesis the aim is to design a QAM modulator which is based on the phase and amplitude modulation. Phase errors in an analog quadrature modulator could be compensated by the phase predistortion [Jon91], which is accomplished by adding a phase offset to the digital quadrature data. This is not possible in the non-linear D/A converter. So this technique is beyond the scope of this thesis.

6.2.1 Exploitation of Sine Function Symmetry

A well-known technique is to store only π/2 rad of sine information, and to generate the sine

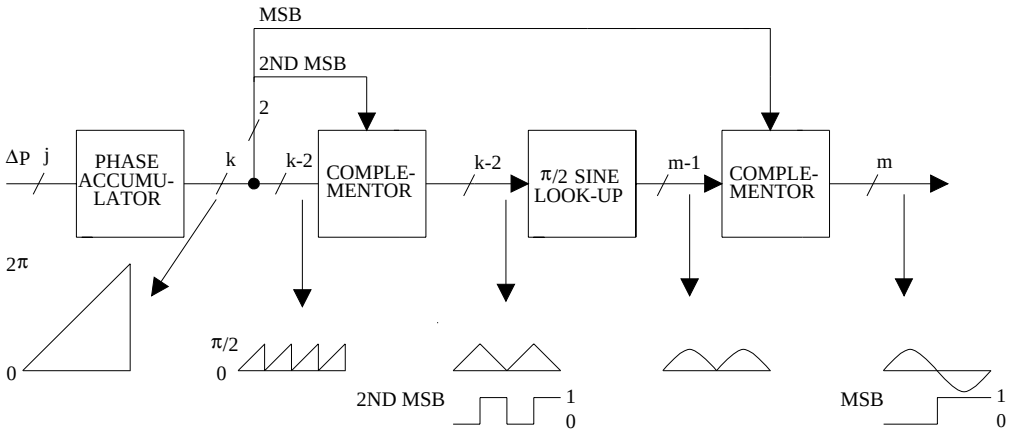

Figure 6.1. Logic to exploit quarter-wave symmetry.

look-up table samples for the full range of 2π by exploiting the quarter-wave symmetry of the sine function. The decrease in the look-up table capacity is paid for by the additional logic necessary to generate the complements of the accumulator and the look-up table output.

The details of this method are shown in Figure 6.1. The two most significant phase bits are used to decode the quadrant, while the remaining *k*-2 bits are used to address a one-quadrant sine look-up table. The most significant bit determines the required sign of the result, and the second most significant bit determines whether the amplitude is increasing or decreasing. The accumulator output is used "as is" for the first and third quadrants. The bits must be complemented so that the slope of the saw tooth is inverted for the second and fourth quadrant. As shown in Figure 6.1, the sampled waveform at the output of the look-up table is a full, rectified version of the desired sine wave. The final output sine wave is then generated by multiplying the full wave rectified version by -1 when the phase is between π and 2π.

In most practical DDS digital implementations, numbers are represented in a 2's complement format. Therefore 2's complementing must be used to invert the phase and multiply the output

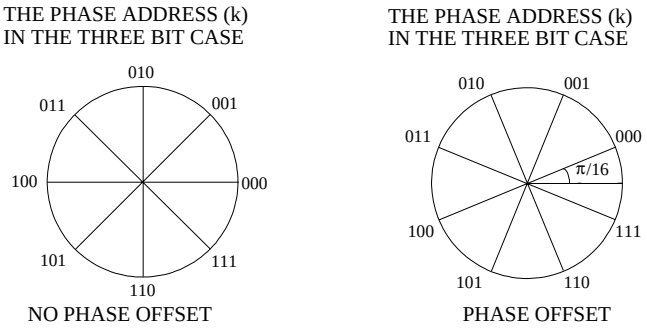

Figure 6.2. ½ LSB phase offset is introduced in all phase addresses. In this case ½ LSB correspond π/16. The 1/2 LSB phase offset is added to all the sine look-up table samples. In this figure it is shown, that 1's complementor maps the phase values to the first quadrant without error.

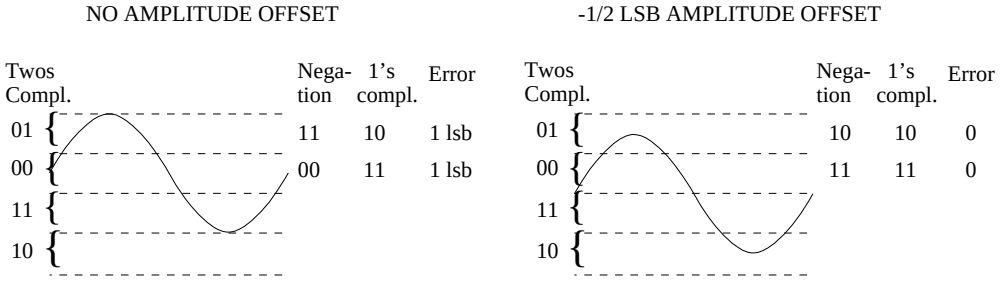

Figure 6.3. -1/2 LSB offset is introduced into the amplitude that is to be complemented; then the negation can be carried out with the 1's complementor without error in Figure 6.1. There must be a +1/2 LSB offset in the D/A-converter output.

of the look-up table by -1. However, it can be shown that if a 1/2 LSB offset is introduced into a number that is to be complemented, then a 1's complementor may be used in place of the 2's complementor without introducing error [Nic88], [Rub89]. This provides savings in hardware since a 1's complementor may be implemented as a set of simple exclusive-or gates. This 1/2 LSB offset is provided by choosing look-up table samples such that there is a 1/2 LSB offset in both the phase and amplitude of the samples [Nic88], [Rub89], as shown in Figure 6.2 and Figure 6.3. In Figure 6.2, the phase offset must be used to reduce the address bits by two. If there is no phase offset, 0 and $\pi/2$ have the same phase address, and one more address bit is needed to distinguish these two values.

6.2.2 Compression of Quarter-Wave Sine Function

In this section the quarter-wave memory compression is investigated. The width of the sine look-up table is reduced before taking advantage of the quadrant symmetry of the sine function (see Figure 6.1). First, a sine-phase difference algorithm will be presented. This algorithm is used in all the subsequent compression techniques except for the CORDIC algorithm. The compression techniques are a trigonometric approximation, the so-called Nicholas' architecture, the Taylor series method and the CORDIC algorithm. For each method, the total compression ratio, the size of memory, the worst-case spur level and additional circuits are presented in Table 6.1. The amplitude values of the quarter-wave compression could be scaled to provide an improved performance in the presence of amplitude quantization [Nic88]. The optimization of the value scaling constant provides only a negligible improvement in the amplitude quantization spur level, so it is beyond scope of this work.

6.2.2.1 Sine-Phase Difference Algorithm

Compression of the storage required for the quarter-wave sine function is obtained by storing the function

$$f(P) = \sin(\frac{\pi P}{2}) - P \tag{6.2}$$

instead of $\sin(\pi P/2)$ in the look-up table (Figure 6.4). Because

$$\max\left[\sin(\frac{\pi P}{2}) - P\right] \approx 0.21 \max\left[\sin(\frac{\pi P}{2})\right], \tag{6.3}$$

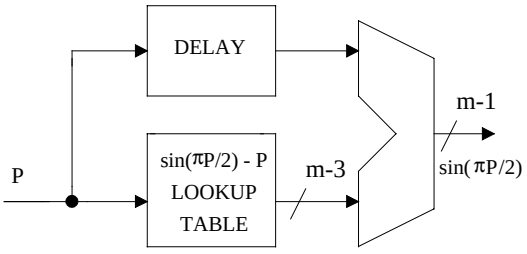

Figure 6.4. Sine-phase difference algorithm.

2 bits of amplitude in the storage of the sine function are saved [Nic88]. The penalty for this storage reduction is the introduction of an extra adder at the output of the look-up table to perform the operation

$$\left[\sin(\frac{\pi P}{2}) - P\right] + P. \tag{6.4}$$

The reduction could be increased by storing function [sin(πP/2) - rP], where r is greater than 1 [Lia97]. For example, the word length of the sine LUT in the quadrature DDS [Tan95a] could be shortened by 4 bits, when the sine LUT stores [sin(πP/2) - 1.375P] within [0, π/4] [Lia97]. The trade-off is three adders at the output of the sine LUT to perform the operation ([sin(πP/2)-1.375P] + 1.375P).

6.2.2.2 Modified Sunderland Architecture

The original Sunderland technique is based on simple trigonometric identities [Sun84]. There are two modifications to the original Sunderland paper. After this paper was published, a method for performing the two's complement negation function with only an exclusive-or was published, which does not introduce errors, when reconstructing a sine wave [Nic88], [Rub89]. This method works by introducing the 1/2-LSB offsets into the phase and amplitude of the sine ROM samples as described in Section 6.2.1. The sine-phase difference algorithm was also published after the Sunderland's paper [Sun84].

The phase address of the quarter of the sine wave is decomposed to $P = a + b + c$, with the word lengths of the variables being $a \rightarrow$ A, $b \rightarrow$ B, and $c \rightarrow$ C. In Figure 6.5, the twelve phase bits are divided into three 4-bit fractions such that a < 1, b < (2^{-4}), c < (2^{-8}). The desired sine function is given by

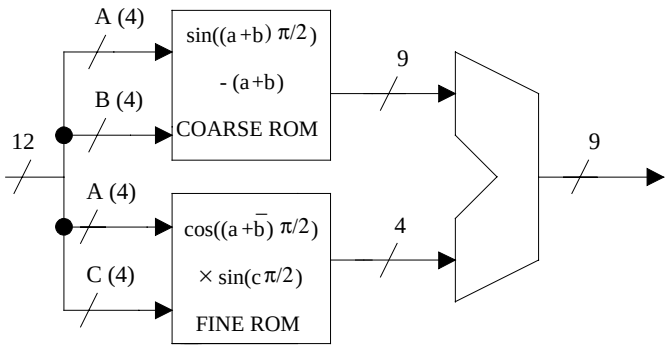

Figure 6.5. Block diagram of the modified Sunderland architecture for quarter-wave sine function compression.

$$\sin(\frac{\pi}{2}(a+b+c)) = \sin(\frac{\pi}{2}(a+b))\cos(\frac{\pi}{2}c) + \cos(\frac{\pi}{2}(a+b))\sin(\frac{\pi}{2}c). \quad (6.5)$$

Given the relative sizes of *a*, *b*, and *c*, this expression can be approximated by

$$\sin(\frac{\pi}{2}(a+b+c)) \approx \sin(\frac{\pi}{2}(a+b)) + \cos(\frac{\pi}{2}(a+\bar{b}))\sin(\frac{\pi}{2}c). \quad (6.6)$$

The approximation is improved by adding the average value of *b* to *a* in the second term. The trigonometric approximation in (6.6) produces a sine approximation error ((6.5) – (6.6)):

$$\sin(\frac{\pi}{2}(a+b))\left[\cos(\frac{\pi}{2}c)-1\right] + \sin(\frac{\pi}{2}c)\left[\cos(\frac{\pi}{2}(a+b)) - \cos(\frac{\pi}{2}(a+\bar{b}))\right]. \quad (6.7)$$

Replacing $\sin(\pi c/2)$ and $\cos(\pi c/2)$ by the first term of their Taylor series, the approximation error is

$$\frac{\pi}{2}c\left[\cos(\frac{\pi}{2}(a+b)) - \cos(\frac{\pi}{2}(a+\bar{b}))\right] = \pi c \sin(\frac{\pi}{4}(2a+b+\bar{b}))\sin(\frac{\pi}{4}(\bar{b}-b)). \quad (6.8)$$

Since the upper limit of sine is 1, and *b* is much smaller than 1, the following upper estimate defines the accuracy:

$$\frac{\pi^2}{4}|c|_{\max}\bar{b}. \quad (6.9)$$

In Figure 6.5 the twelve phase bits are divided into 4 bit fractions, and the estimated accuracy is 0.0003 (6.9). The size of the upper memory is reduced by the sine difference algorithm. The access time of the upper memory is more critical due to its larger size. In Figure 6.5 the coarse ROM provides low resolution phase samples, and the fine ROM gives additional phase resolution by interpolating between the low resolution phase samples.

6.2.2.3 Nicholas' Architecture

An alternative methodology for choosing the samples to be stored in the ROMs is based on numerical optimization [Nic88]. The phase address of the quarter of the sine wave is defined as *P* = *a* + *b* + *c*, where the word length of the variable *a* is A, the word length of *b* is B, and of *c* is C. The variables *a*, *b* form the coarse ROM address, and the variables *a*, *c* form the fine ROM address. In Figure 6.6 the coarse ROM samples are represented by the dot along the solid line, and the fine ROM samples are chosen to be the difference between the value of the "error bars" directly below and above that point on the solid line. In Figure 6.6 the function is divided into 4 regions, corresponding to *a* = 00, 01, 10, and 11. Within each region, only one interpolation value may be used between the error bars and the solid line for the same *c* values. The interpolation value used for each value of *c* is chosen to minimize either the mean square or the maximum absolute error of the interpolation within the region [Nic88]. Further storage compression is provided by exploiting the symmetry in the fine ROM correction factors, Figure 6.6. If the coarse ROM samples are chosen in the middle of the interpolation region, then the fine ROM samples will be approximately symmetric around the $c = (2^C - 1)/2$ point (*C* is the word length

of the variable *c*). Thus, by using an adder/subtractor instead of an adder to sum the coarse and fine ROM values, the size of the fine ROM may be halved. Some additional complexity must be added to the adder/subtractor control logic if this technique is used with the sine-phase difference algorithm, since the slope of the function in equation (6.2) changes sign at a non symmetry point between 0 and $\pi/2$ on the x-axis. For example, the digital logic required to perform this can be accomplished with less than four logic gates for the 13-bit phase case [Nic88]. Since the fine ROM is generally not in the critical speed path, the effective resolution of the fine ROM may be doubled, rather than halving the ROM. It allows the segmentation of the compression algorithm to be changed, effectively adding an extra bit of phase resolution to the look-up table, which thereby reduces the magnitude of the worst-case spur due to phase accumulator truncation.

Computer simulations determined that the optimum partitioning of the ROM address word lengths to provide a 13-bit phase resolution was A = 4, B = 4, and C = 5, using the notation in Figure 6.7, [Nic88]. The simulations showed that the mean square criterion gives better total spur level than the maximum absolute error criterion in this segmentation. The architecture for sine wave generation employing this look-up table compression technique is shown in Figure 6.7. The amplitude values of the coarse and fine ROMs could be scaled to provide an improved performance in the presence of amplitude quantization [Nic88]. The optimization of the value scaling constant provides only a negligible improvement in the amplitude quantization spur level, so it is beyond the scope of this thesis.

In a modified version of the above architecture the symmetry in the fine ROM samples is not utilized [Tan95a], so the extra bit of the phase resolution to the ROM address is not achieved. Therefore, the modified Nicholas architecture uses a 14-to-12-bit instead 15-to-12-bit phase to

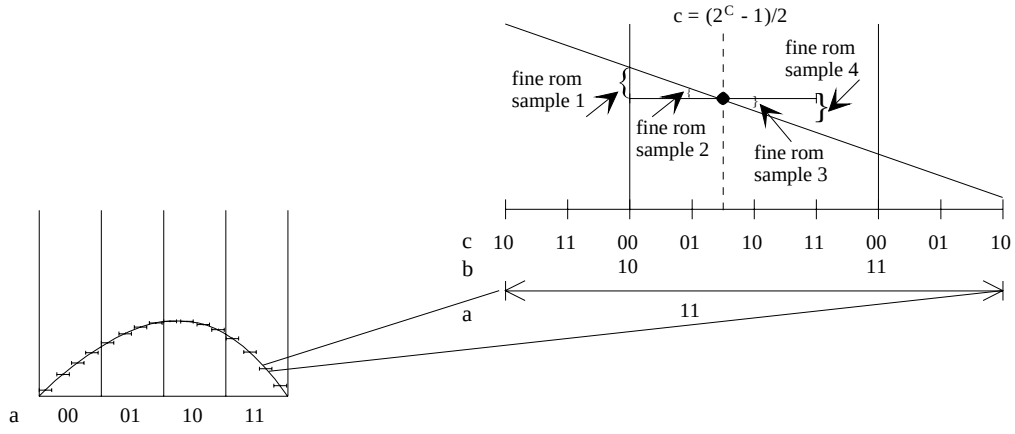

Figure 6.6. Fine ROM samples are used to interpolate a higher phase resolution function from the coarse samples, and the symmetry in the fine ROM samples around the $c=(2^C-1)/2$ point. Here C = 2.

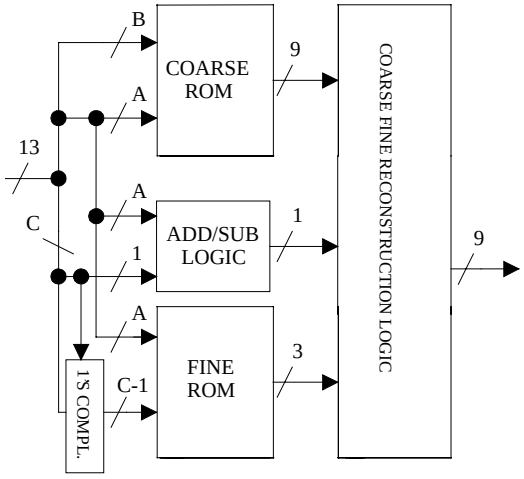

Figure 6.7. Sine function generation logic of Nicholas' architecture.

amplitude mapping in this case. Some hardware is saved, because an adder instead of an adder/subtractor is used to sum the coarse and fine ROM values, and the adder/subtractor control logic is not needed. The difference between the modified Nicholas architecture and the modified Sunderland architecture is that the samples stored in the sine ROM are chosen using the numerical optimization in the modified Nicholas architecture.

The IC realization of the Nicholas architecture is presented in [Nic91], where a CMOS chip has the maximum clock frequency of 150 MHz. Analog Devices has also used this sine memory compression method in their CMOS device, which has the output word length of 12 bits and 100 MHz clock frequency [Ana94]. The IC realization of the modified Nicholas architecture is presented in [Tan95a], where the CMOS quadrature digital synthesizer operates at a 200 MHz clock frequency. The modified Nicholas architecture has also been used in [Tan95b], where a CMOS chip has four parallel ROM tables to achieve four times the throughput of a single DDS. The chip that uses only one ROM table has the clock frequency of 200 MHz [Tan95a]. Using the parallel architecture with four ROM tables, the chip attains the speed of 800 MHz [Tan95b].

6.2.2.4 Taylor Series Approximation

The phase address "*P*" is divided into the upper phase address "*u*" and the lower phase address "*P*-*u*" [Wea90a], [Bel00]. The Taylor series is performed around the upper phase address (*u*)

$$\sin(\frac{\pi}{2}P) = \sin(\frac{\pi}{2}u) + k_1 (P-u)\cos(\frac{\pi}{2}u) - \frac{k_2 (P-u)^2 \sin(\frac{\pi}{2}u)}{2} + R_3, \tag{6.10}$$

where k_n represents a constant used to adjust the units of each series term. The adjustment in units is required because the phase values have angular units. Therefore it is necessary to have a

conversion factor k_n, which includes a multiple of $\pi/2$ to compensate for the phase units. The remainder is

$$R_n = \frac{d^n(\sin(\frac{\pi}{2}r))}{dr}\frac{(P-u)^n}{n!}, \quad \text{where } r\ \varepsilon\ [u, P]. \tag{6.11}$$

Since sine and cosine both have upper limits of 1, the following upper estimate defines the accuracy:

$$|R_n| = \left|\frac{k_n\ (P-u)^n}{n!}\right| \le \left|\frac{k_n\ |P-u|^n_{\max}}{n!}\right|. \tag{6.12}$$

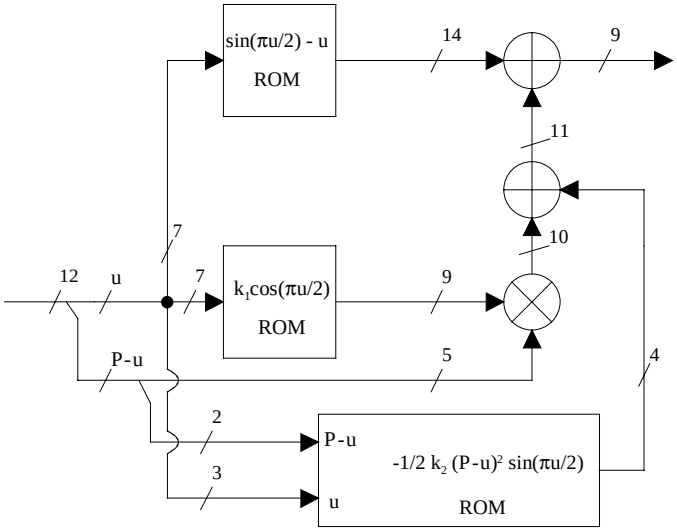

Figure 6.8. Taylor series approximation for the quarter sine converter.

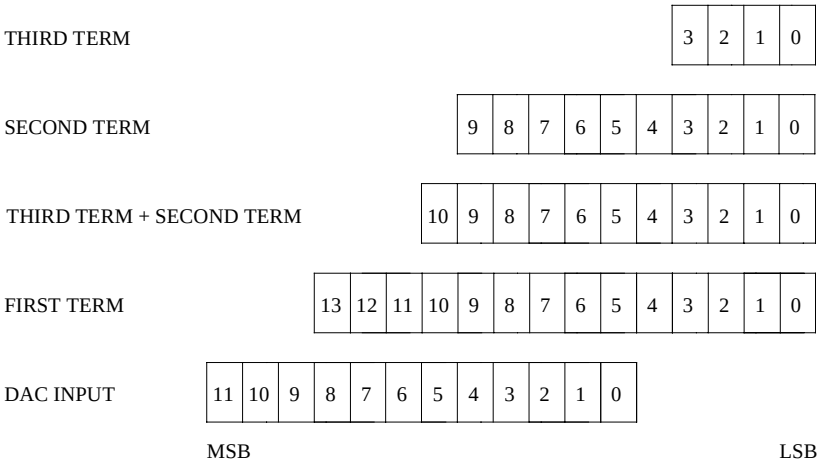

Figure 6.9. Relative bit positions of multi-bit data words used in implementing the circuit of Figure 6.8.

The Taylor series (6.10) is approximated in Figure 6.8 by taking three terms. While additional terms can be employed, their contribution to the accuracy is very small as shown in Figure 6.9 and, therefore, of little weight in this application. The estimated accuracy is 0.0000025 (6.12). Other inaccuracies present in the operation of current DDS designs override the finer accuracy provided by successive series terms. The seven most significant bits of the input phase are selected as the upper phase address "*u*" which is transferred simultaneously to a sine ROM and a cosine ROM as address signals as shown in Figure 6.8. The output of the sine ROM is the first term of the Taylor series and is transferred to a first adder, where it will be summed with the remaining terms involved. The size of the sine ROM is reduced by the sine difference algorithm. The output of the cosine ROM is configured to incorporate the predetermined unit conversion value k_1. The cosine ROM output is the first derivative of the sine. The least significant bits (*P*-*u*) are multiplied by the output of the cosine ROM to produce the second term. The third term is computed in a ROM by combining the second derivative of $\sin((\pi u)/2)$ and the square of the lower phase address "*P*-*u*". This is done by selecting the upper bits of "*P*-*u*" and "*u*" values as a portion of the address for the ROM. This is possible since the last term only roughly contributes 1/4 LSB to the D/A-converter input, as shown in Figure 6.9. As with the cosine ROM, the unit conversion factor is included in the values stored in the ROM. The third term ROM output is combined with the multiplier output in a second adder, and subsequently combined with the first term ROM output in the first adder.

QUALCOMM has used the Taylor series approximations in their device, which has the output word length of 12 bits and 50 MHz clock frequency [Qua91a]. The DDS is realized with a CMOS technology, which in part limits the speed.

6.2.2.5 Using CORDIC Algorithm as a Quarter Sine Wave Generator

The CORDIC algorithm performs vector coordinate rotations by using simple iterative shifts and add/subtract operations, which are easy to implement in hardware [Vol59]. The details of the CORDIC algorithm are presented in Chapter 4. If the initial values are chosen to be $I_0 = 1$ and $Q_0 = 0$ then P_0 is formed using the remaining *k*-2 bits of the phase register value from the DDS. From (4.8) the result will be

$$\begin{aligned} I_n &= G_n \cos(A) \\ Q_n &= -G_n \sin(A) \\ G_n &= \prod_{i=0}^{n-1} \sqrt{1 + 2^{-2i}} \\ A &= P_0 - P_n, \end{aligned} \tag{6.13}$$

where P_n is the angle approximation error.

If the initial values are chosen to be $I_0 = 1/G_n$, $Q_0 = 0$, and P_0 is the remaining *k*-2 bits of the phase register value from the DDS, then there is no need for a scaling operation after the COR-

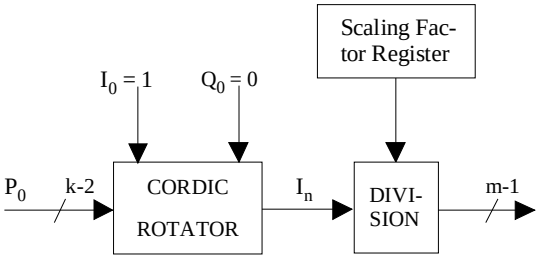

Figure 6.10. CORDIC rotator for a quarter sine converter.

DIC iterations. The amplitude of the output waveform could be modulated by changing the scaling factor. The value of I_n may then be transferred to an appropriate D/A-converter. The architecture for quarter sine wave generation employing this technique is shown in Figure 6.10.

The hardware costs of CORDIC and ROM based phase to amplitude converters were estimated in FPGA, which shows that the CORDIC based architecture becomes better than the ROM based architecture when the required accuracy is 9 bits or more [Par00]. The CORDIC algorithm is also effective for solutions where quadrature mixing is performed (see Chapter 12). The conventional quadrature mixing requires four multipliers, two adders and sine/cosine memories (see Figure 2.4). It replaces sine/cosine ROMs, four multipliers and two adders.

For example the GEC-Plessey I/Q splitter has a 20 MHz clock frequency with a 16-bit phase and amplitude accuracy [GEC93], and Raytheon Semiconductor's DDS has 25 MHz clock frequency with 16-bit phase and amplitude accuracy [Ray94].

6.2.3 Simulation

A computer program (in Matlab) has been created to simulate the direct digital synthesizer in Figure 2.1. The memory compression and algorithmic techniques have been analyzed with no phase truncation (the phase accumulator length = the phase address length), and the spectrum is calculated prior to the D/A-conversion. The number of points in the DDS output spectrum depends on ΔP (phase increment word) via the greatest common divisor of ΔP and 2^j (GCD(ΔP,2^j)) (2.4). Any phase accumulator output vector can be formed from a permutation of another output vector regardless of the initial phase accumulator contents, when GCD(ΔP,2^j) = 1 for all values of ΔP (see Section 5.3). A permutation of the samples in the time domain results in an identical permutation of the discrete Fourier transform (DFT) samples in the frequency domain (see Section 5.3). This means that the spurious spectrum due to all system non-linearities can be generated from a permutation of another spectrum, when GCD(ΔP,2^j) = 1 for all ΔP, because each spectrum will differ only in the position of the spurs and not in the magnitudes. When the least significant bit of the phase accumulator input is forced to one, it causes all of the phase accumulator output sequences to belong to the number theoretic class GCD(ΔP,2^j) = 1, regardless of the value of ΔP. Only one simulation need to be performed to determine the value of the worst-case spurious response due to system non-linearities. The number of samples has been

chosen (an integer number of cycles in the time record) so that problems of leakage in the fast Fourier transform (FFT) analysis can be avoided and unwindowed data can be used. The FFT was performed over the output period (2.4). The size of the FFT was 16384 points.

6.2.4 Summary of Memory Compression and Algorithmic Techniques

Table 6.1 comprises the summary of memory compression and algorithmic techniques. Table 6.1 shows how much memory and how many additional circuits are needed in each memory compression and algorithmic technique to meet the spectral requirement for the worst case spur level, which is about -85 dBc due to the sine memory compression. In the DDS, most spurs are normally not generated by digital errors but rather by the analog errors in the D/A-converter. The spur level (-85 dBc) from the sine memory compression is not significant in DDS applications because it will stay below the spur level of a high speed 12-bit D/A-converter [Bas98]. Unlike in Section 6.2.2.4, two terms are used for the Taylor series approximation in Table 6.1. Therefore, all memory compression and algorithmic techniques in Table 6.1 are comparable with almost the same worst case spur. In Table 6.1 the modified Nicholas architecture [Tan95a] is used and therefore the compression ratio and the worst-case spur level are different from that in the Nicholas architecture [Nic88]. The difference between the modified Nicholas architecture

Table 6.1. Memory compression and algorithmic techniques with the worst-case spur level due to the sine memory compression specified to be about –85 dBc.

Method	Needed ROM	Total compression ratio	Additional Circuits (not include quarter and sine difference logic)	Worst case Spur (below carrier)	Comments
Uncompressed memory	$2^{14} \times 12$ bits	1 : 1	-	-97.23 dBc	Reference
Mod. Sunderland architecture	$2^8 \times 9$ bits $2^8 \times 4$ bits	59 : 1	Adder	-86.91 dBc	Simple
Mod. Nicholas architecture	$2^8 \times 9$ bits $2^8 \times 4$ bits	59 : 1	Adder	-86.81 dBc	Simple
Taylor series approximation with two terms	$2^7 \times 9$ bits † $2^7 \times 5$ bits ††	110 : 1	Adder Multiplier	-85.88 dBc	Need multiplier
CORDIC algorithm	–	–	14 pipelined stages, 18-bit inner word length	-84.25 dBc	Much computation

† The first term ROM size, which is reduced by the sine difference algorithm.
†† The cosine ROM size.

and the modified Sunderland architecture is that the samples stored in the sine ROM are chosen according to the numerical optimization in the modified Nicholas architecture. In the 14-to-12-bit phase-to-amplitude mapping the numerical optimization gives no benefit, because the modified Sunderland architecture and the modified Nicholas architecture give almost the same spur levels.

6.3 Filter

There are many classes of filters that exist in literature. However, for most applications the field can be narrowed down to three basic filter families. Each is optimized for a particular characteristic in either the time or frequency domain. The three filter types are the Chebyshev, Gaussian, and Legendre families of responses [Zve67]. Filter applications that require fairly sharp frequency response characteristics are best served by the Chebyshev family of responses. However, it is assumed that ringing and overshoot in the time domain do not present a problem in such applications.

The Chebyshev family can be subdivided into four types of responses, each with its own special characteristics. The four types are the Butterworth response, the Chebyshev response, the inverse Chebyshev response, and elliptical response.

The Butterworth response is completely monotonic. The attenuation increases continuously as the frequency increases: i.e. there are no ripples in the attenuation curve. Of the Chebyshev family of filters, the passband of the Butterworth response is the flattest. Its cut-off frequency is identified by the 3dB attenuation point. Attenuation continues to increase with frequency, but the rate of attenuation after cut-off is rather slow.

The Chebyshev response is characterized by attenuation ripples in the passband followed by monotonically increasing attenuation in the stopband. It has a much sharper passband to stopband transition than the Butterworth response. However, the cost for the faster stopband roll-off is ripples in the passband. The steepness of the stopband roll-off is directly proportional to the magnitude of the passband ripples; the larger the ripples, the steeper the roll-off.

The inverse Chebyshev response is characterized by monotonically increasing attenuation in the passband with ripples in the stopband. Similar to the Chebyshev response, larger stopband ripples yields a steeper passband to stopband transition.

The elliptical response offers the steepest passband to stopband transition of any of the filter types. The penalty, of course, is attenuation ripples, in this case both in the passband and stopband.

Table 6.2. Low-pass filter order.

Type	Order
Elliptic	5
Chebyshev	7
Butterworth	12

The images of the D/A converter output must be removed by the low-pass filter, otherwise there will be in-band intermodulation products after up-conversion mixing in Figure 10.1. The low-pass filter requirements are a cut-off frequency of 50 MHz, a stopband attenuation of more than 60 dB, a passband ripple of 0.5 dB and a stopband edge of 100 MHz. The sharp transition of this low-pass filter requires a sharp cut-off filter. Therefore, a fifth-order elliptic filter is required [Zve67]. The other filter types require even higher orders, as listed in Table 6.2.

7. Spur Reduction Techniques in Sine Output Direct Digital Synthesizer

The drawback of the direct digital synthesizer (DDS) is the high level of spurious frequencies [Rei93]. In this chapter we only concentrate on the spurs that are caused by the finite word length representation of phase and amplitude samples. The number of words in the ROM (phase to amplitude converter) will determine the phase quantization error, while the number of bits in the digital-to-analog converter (D/A-converter) will affect amplitude quantization. Therefore, it is desirable to increase the resolution of the ROM and D/A-converter. Unfortunately, larger ROM and D/A-converter resolutions mean higher power consumption, lower speed, and greatly increased costs. Memory compression techniques could be used to alleviate the problem, but the cost of different techniques is an increase in circuit complexity and distortions (see Section 6.2).

Additional digital techniques may be incorporated in the DDS in order to reduce the presence of spurious signals at the DDS output. The Nicholas modified phase accumulator does not destroy the periodicity of the error sequences, but it spreads the spur power into many spur peaks [Nic88]. Non-subtractive dither is used to reduce the undesired spurious components, but the penalty is that the broadband noise level is quite high after dithering [Rei93], [Fla95]. To alleviate the increase in noise, subtractive dither can be used in which the dither is added to the digital samples and subtracted from the DDS analog output signal [Twi94]. The requirement of dither subtraction at the DDS output makes the method complex and difficult to implement in practice. The novel spur reduction technique presented in this work uses high-pass filtered dither [Car87], [Ble87], which has most of its power in an unused spectral region between the band edge of the low-pass filter and the Nyquist frequency. After the DDS output has been passed through the low-pass filter, only a fraction of the dither power will remain. From this point of view the low-pass filtering is a special implementation of the dither subtraction operation.

An error feedback (EF) technique is used to suppress low frequency quantization spurs [Lea91a], [Lea91b], [Laz94]. A novel tunable error feedback structure in the DDS is developed in Section 7.4.2. The drawback of conventional EF structures is that the output frequency is low with respect to the clock frequency, because the transfer function of the EF has zero(s) at DC. In the proposed architecture the clock frequency needs only to be much greater than the bandwidth of the output signal, whereas the output frequency could be any frequency up to somewhat below the Nyquist rate. The coefficients of the EF are tuned according to the output frequency.

7.1 Nicholas' Modified Accumulator

This method does not destroy the periodicity of the error sequences, but it spreads the spur power into many spur peaks [Nic88]. If GCD (ΔP, 2^{j-k}) is equal to 2^{j-k-1}, the spur power is concentrated in one peak, see Figure 7.2. The worst case carrier-to-spur ratio is from (5.25)

$$\left(\frac{C}{S}\right) = (6.02k - 3.992)\ \text{dBc}, \tag{7.1}$$

where k is the word length of the phase accumulator output used to address the ROM. If GCD (ΔP, 2^{j-k}) is equal to 1, the spur power is spread over many peaks in Figure 7.3. Then the carrier-to-spur ratio is approximately, from (5.26),

$$\left(\frac{C}{S}\right) = 6.02k\ \text{dBc} \quad \text{when } (j-k) >> 1. \tag{7.2}$$

Comparing (7.1) and (7.2) shows that the worst-case spur can be reduced in magnitude by 3.922 dB by forcing GCD (ΔP, 2^{j-k}) to be unity, i.e. by forcing the phase increment word to be relatively prime to 2^{j-k}. This causes the phase accumulator output sequence to have a maximal numerical period for all values of ΔP, i.e. all possible values of the phase accumulator output sequence are generated before any values are repeated. In Figure 7.1 the hardware addition is to modify the existing j-bit phase accumulator structure to emulate the operation of a phase accumulator with a word length of j+1 bits under the assumption that the least significant bit of the phase increment word is always one [Nic88]. It too has an effect of randomizing the errors introduced by the quantizied ROM samples, because in a long output period the error appears as "white noise" (5.32).

The disadvantage of the modification is that it introduces an offset of

$$f_{offset} = \frac{f_{clk}}{2^{j+1}} \tag{7.3}$$

into the output frequency of the DDS. The offset will be small, if the clock frequency is low and the length of the phase accumulator is long. If there is no phase truncation error in the original samples (GCD (ΔP, 2^j) $\geq 2^{j-k}$), then this method will make the situation worse for the phase error. Therefore, it is good that this spur reduction method is optional, depending on the phase increment word.

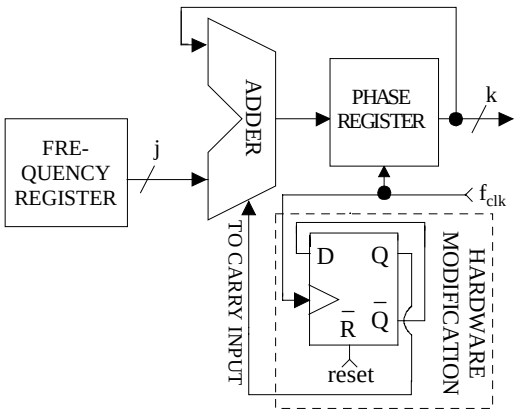

Figure 7.1. Hardware modification to force optional GCD (ΔP,2^{j-k+1}) = 1.

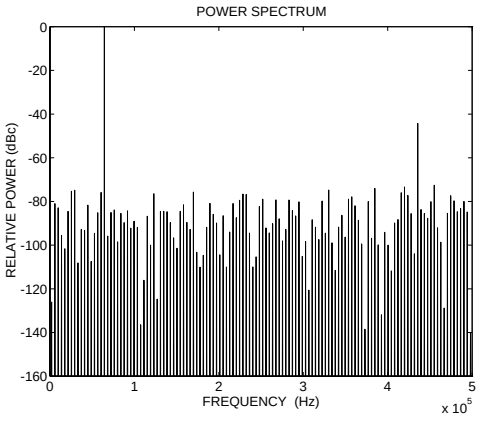

Figure 7.2. Spur due to the phase truncation, max. carrier-to-spur level 44.24 dBc (44.17 dBc (5.25) and (7.1)). There is a sea of amplitude spurs below the phase spur. The simulation parameters: j = 12, k = 8, m = 10, ΔP = 264, f_{clk} = 1 MHz, $f_{out} \approx$ 64453 Hz.

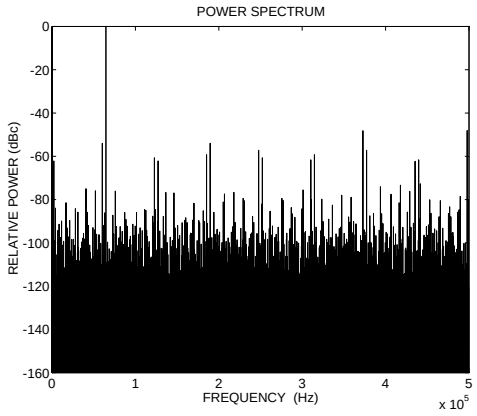

Figure 7.3. Spurs due to the phase truncation, max. carrier-to-spur level 48.08 dBc (48.16 dBc (5.26) and (7.2)). The simulation parameters same as Figure 7.2 but ΔP = 265, $f_{out} \approx$ 64697 Hz.

7.2 Non-subtractive Dither

In this section methods of reducing the spurs by rendering certain statistical moments of the total error statistically independent of the signal are investigated [Fla95]. In essence, the power of the spurs is still there, but spreads out as a broadband noise [Rei93]. This broadband noise is more easily filtered out than the spurs. In the DDS there are different ways to dither: some designs have dithered the phase increment word [Whe83], the address of the sine wave table [Jas87], [Zim92] and the sine-wave amplitude [Rei91], [Ker90], [Fla95] with pseudo random numbers, in order to randomize the phase or amplitude quantization error.

The dither is summed with the phase increment word in the square wave output DDS [Whe83]. The technique could be applied for the sine output DDS (source 1 in Figure 7.4), too. It is important that the dither signal is canceled during the next sample, otherwise the dither will be accumulated in the phase accumulator and there will be frequency modulation. The circuit will be complex due to the previous dither sample canceling, therefore this method is beyond the scope of this work.

It is important that the period of the evenly distributed dither source (L) satisfies [Fla95]

$$\frac{\Delta^2}{6L} < P_{\max}, \tag{7.4}$$

where P_{max} is the maximum acceptable spur power, and Δ is the step size for both the amplitude and phase quantization. In this work first-order dither signals (evenly distributed) are considered. The use of higher-order dither accelerates spur reduction with the penalty of a more complex circuit and higher noise floor [Fla93], [Fla95].

7.2.1 Non-subtractive Phase Dither

An evenly distributed random quantity $z_P(n)$ (source 2 in Figure 7.4) is added to the phase address prior to the phase truncation. The output sequence of the DDS is given by

$$x(n) = \sin(\frac{2\pi}{2^j}(P(n) + \varepsilon(n))), \tag{7.5}$$

where $P(n)$ is a phase register value. The total phase truncation noise is

$$\varepsilon(\mathrm{n}) = e_P(n) + z_P(n), \tag{7.6}$$

where the phase truncation error varies periodically as

$$e_p(n) = (P(n)) \bmod 2^{j-k}, \text{ when } \mathrm{GCD}(\Delta P, 2^{j-k}) < 2^{j-k}, \tag{7.7}$$

and the period of the phase truncation error (M) is from (5.7).

Using small angle approximation

$$x(n) \approx \sin(\frac{2\pi}{2^j}P(n)) + \frac{2\pi}{2^j}\varepsilon(n)\cos(\frac{2\pi}{2^j}P(n)) + O((\max(\varepsilon(n)))^2), \tag{7.8}$$

where $\max(\varepsilon(n))$ is 2^{-k}. The number of bits, k, must be large enough to satisfy the small angle assumption, typically, $k \geq 4$. The total quantization noise will be examined by considering the first two terms above, and then the second-order, $O((\max(\varepsilon(n)))^2)$, effect.

7.2.2 First-Order Analysis

The total phase fluctuation noise will be proportional to $e_P(n)$ [Fla95], when the random value $z_P(n)$ is added to the phase address before truncation to k-bits, as in Figure 7.5. The evenly distributed random quantity $z_P(n)$ varies in the range $[0, 2^{j-k})$. If $z_P(n)$ is less than the quantity $(2^{j-k} - e_P(n))$, then $e_P(n) + z_P(n))$ will be truncated to (0). The total phase truncation noise will be

$$\varepsilon(\mathrm{n}) = -e_P(n) \tag{7.9}$$

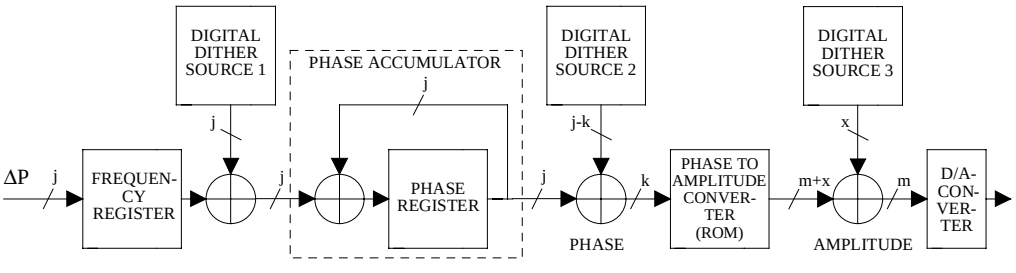

Figure 7.4. Different ways of dithering in the DDS.

with probability

$$\frac{(2^{j-k} - e_P(n))}{2^{j-k}}, \tag{7.10}$$

because there are (2^{j-k} - $e_P(n)$) values of $z_P(n)$ less than (2^{j-k} - $e_P(n)$), and there are 2^{j-k} values of $z_P(n)$. If $z_P(n)$ is equal to or greater than the quantity (2^{j-k} - $e_P(n)$), then ($e_P(n)$ + $z_P(n)$) will be truncated to (2^{j-k}). The total phase truncation noise will be

$$\varepsilon(\mathrm{n}) = (2^{j-k} - e_P(n)) \tag{7.11}$$

with the probability

$$\frac{e_P(n)}{2^{j-k}}, \tag{7.12}$$

because there are $e_P(n)$ values of $z_P(n)$ which are equal to or greater than (2^{j-k} - $e_P(n)$).

At all sample times *n* the first moment of the total phase truncation noise is zero

$$E\{\varepsilon(n)\} = -e_P(n)\frac{(2^{j-k} - e_p(n))}{2^{j-k}} + (2^{j-k} - e_p(n))\frac{e_P(n)}{2^{j-k}} = 0. \tag{7.13}$$

The second moment of the total phase truncation noise is

$$\begin{aligned} E\{\varepsilon^2(n)\} &= e_P^2(n)\frac{(2^{j-k} - e_p(n))}{2^{j-k}} + (2^{j-k} - e_p(n))^2\frac{e_P(n)}{2^{j-k}} \\ &= 2^{j-k}e_p(n) - e_P^2(n) \\ &= 2^{2(j-k)}\left(\frac{e_p(n)}{2^{j-k}} - \left(\frac{e_p(n)}{2^{j-k}}\right)^2\right). \end{aligned} \tag{7.14}$$

Two bounds are derived for the average value of the second moment (the power of the total truncation noise) based on the period of the error term (*M*). In the first case GCD (ΔP, 2^{j-k}) is 2^{j-k-1} and *M* is 2 (5.7), and the average value of the sequence (7.14) reaches its minimum non-zero value. The phase truncation error sequence is 0, 2^{j-k-1}, 0, 2^{j-k-1}, 0, 2^{j-k-1} … from (7.7). Then the sequence (7.14) becomes

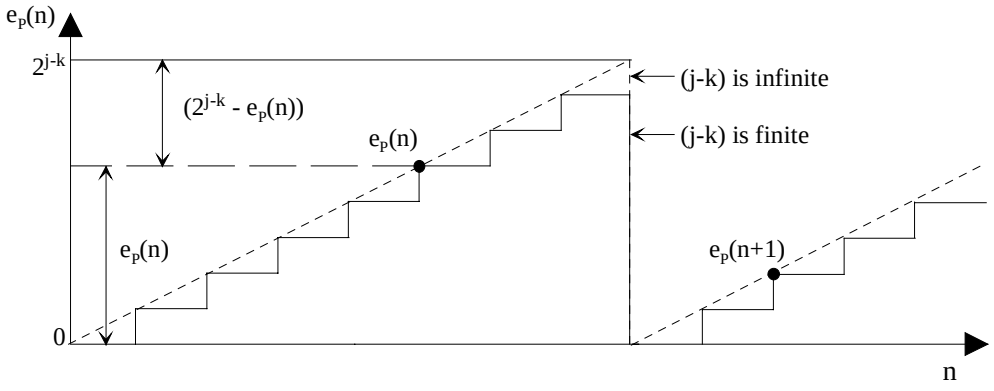

Figure 7.5. Phase truncation errors.

$$E\{\varepsilon^2\} = 0 + \frac{2^{2(j-k)}}{4} + 0 + \frac{2^{2(j-k)}}{4} + 0 + \frac{2^{2(j-k)}}{4} \ldots \tag{7.15}$$

The average value of this sequence is

$$\text{Avg}(E\{\varepsilon^2\}) = \frac{2^{2(j-k)}}{8}. \tag{7.16}$$

In the second case GCD (ΔP, 2^{j-k}) is 1 and M is 2^{j-k} (5.7), and the average value of the sequence (7.14) reaches its maximum value. In this case the phase truncation error sequence takes on all possible error values ([0, 2^{j-k})) before any is repeated. Then the average value of the sequence (7.14) becomes

$$\text{Avg}(E\{\varepsilon^2\}) = \frac{2^{2(j-k)}}{6}, \text{ when } j >> k. \tag{7.17}$$

Information about the spurs and noise in the power spectrum of $x(n)$ is obtained from the autocorrelation function. The autocorrelation of $x(n)$ is [Fla95]

$$\begin{aligned} E\{x(n)\, x(n+m)\} &\approx \sin(\frac{2\pi}{2^j}P(n)) \sin(\frac{2\pi}{2^j}P(n+m)) \\ &+ \frac{4\pi^2}{2^{2j}} \cos(\frac{2\pi}{2^j}P(n)) \cos(\frac{2\pi}{2^j}P(n+m))\, E\{\varepsilon(n)\, \varepsilon(n+m)\} + O(2^{-4k}). \end{aligned} \tag{7.18}$$

Spectral information is obtained by averaging over time [Lju87], resulting in [Fla95]

$$\bar{R}_{xx}[m] \approx \frac{1}{2}\left[1 + \frac{4\pi^2}{2^{2j}} \bar{R}_{ee}[m]\right] \cos(\frac{2\pi}{2^j}P(m)), \tag{7.19}$$

where $\bar{R}_{ee}[m]$ = $\text{Avg}_n(\text{E}\{\varepsilon(n)\varepsilon(n+m)\})$, the time-averaged autocorrelation of the total quantization noise. It should be remembered that, for any fixed time n, the probability distribution of $\varepsilon(n)$, a function of $p(n)$, is determined entirely by the outcome of the dither signal $z(n)$. When $z(n)$ and $z(n+m)$ are independent random variables for non-zero lag m, $\varepsilon(n)$ and $\varepsilon(n+m)$ are also independent for $m \neq 0$, and hence $\varepsilon(n)$ is spectrally white. In this case, the autocorrelation becomes [Fla95]

$$\bar{R}_{xx}[m] \approx \frac{1}{2}\left[1 + \frac{4\pi^2}{2^{2j}} \text{Avg}(\varepsilon^2)\, \delta(m)\right] \cos(\frac{2\pi}{2^j}P(m)), \tag{7.20}$$

where $\delta(m)$ is the Kronecker delta function ($\delta(0) = 1$, $\delta(m) = 0$, $m \neq 0$).

The signal-to-noise ratio is derived from (7.20), when $m = 0$, as

$$\text{SNR} \approx \frac{1}{\frac{4\pi^2}{2^{2j}} \text{Avg}(E\{\varepsilon^2\})}. \tag{7.21}$$

The upper bound to the signal-to-noise ratio is from (7.16)

$$\text{SNR} \approx 10 \times \log_{10}\left(\frac{2}{\pi^2 2^{-2k}}\right) \approx (6.02k - 6.93) \text{ dB}. \tag{7.22}$$

The lower bound to the signal-to-noise ratio is from (7.17)

$$\text{SNR} \approx 10 \times \log_{10}\left(\frac{6}{4\pi^2\, 2^{-2k}}\right) \approx (6.02k - 8.18)\ \text{dB}. \tag{7.23}$$

The sinusoid generated is a real signal, so its power is equally divided into negative and positive frequency components. The total noise power is divided to *S* spurs, where *S* is the number of samples and the period of the dither source is longer than *S*. Using these facts, the upper bound of the carrier-to-noise power spectral density is the same as in [Fla95]

$$\left(\frac{C}{N}\right) \approx (6.02k - 9.94 + 10\log_{10}(S))\ \text{dBc}. \tag{7.24}$$

The upper bound is achieved, when GCD (ΔP, 2^{j-k}) is 2^{j-k-1}. The lower bound of the carrier-to-noise power spectral density is

$$\left(\frac{C}{N}\right) \approx (6.02k - 11.19 + 10\log_{10}(S))\ \text{dBc}. \tag{7.25}$$

The lower bound is achieved, when $j >> k$ and GCD (ΔP, 2^{j-k}) is 1. The new bound (7.25) for the signal-to-noise spectral density is derived from these facts.

7.2.3 Second-Order: Residual Spurs

For a worst-case analysis of second-order effects [Fla95], expand the generated sine by the sum of the angles formula

$$\begin{aligned} x(n) &= \sin\left(\frac{2\pi}{2^j}(P(n) + \varepsilon(n))\right) = \sin\left(\frac{2\pi}{2^j}P(n)\right)\cos\left(\frac{2\pi}{2^j}\varepsilon(n)\right) \\ &\quad + \cos\left(\frac{2\pi}{2^j}P(n)\right)\sin\left(\frac{2\pi}{2^j}\varepsilon(n)\right). \end{aligned} \tag{7.26}$$

The information about the spurs in the power spectrum of $x(n)$ is obtained from the autocorrelation function at non-zero lags. When the dither sequence $z(n)$ is a sequence of i.i.d. variates, the autocorrelation function for $x(n)$, with lag m not equal to zero, is

$$R_{xx}[n, n+m] = E\{x(n)x(n+m)\}. \tag{7.27}$$

The excepted value of $x(n)$ is a deterministic function of time. From the above expression, it follows that spectral information about the random process $x(n)$, with the exception of noise floor information, is contained in $E\{x(n)\}$, which we call the "except waveform" [Lip92].

$$E\{x(n)\} = \sin\left(\frac{2\pi}{2^j}P(n)\right)\cos\left(\frac{2\pi}{2^j}\varepsilon(n)\right) + \cos\left(\frac{2\pi}{2^j}P(n)\right)\sin\left(\frac{2\pi}{2^j}\varepsilon(n)\right). \tag{7.28}$$

Since $\varepsilon(n)$ is zero mean at all sample times the excepted waveform reduces to

$$E\{x(n)\} \approx \left(1 - \frac{2\pi^2}{2^{2j}}E\{\varepsilon(n)^2\}\right)\sin\left(\frac{2\pi}{2^j}P(n)\right) + O(2^{-3k}). \tag{7.29}$$

The form of the excepted waveform clearly shows that the spurious content of the signal will be derived from the dependence of the second and higher order moments of the quantization noise

[Fla95]. It is this fundamental principle that will ultimately lead to the –12 dBc per phase bit behavior for uniformly phase-dithered sinusoidal generation [Fla95].

It remains to consider the second moment of the total phase (from (7.14))

$$E\{\varepsilon^2(n)\} = 2^{2(j-k)}\left(\frac{e_p(n)}{2^{j-k}} - \left(\frac{e_p(n)}{2^{j-k}}\right)^2\right). \tag{7.30}$$

The worst-case carrier to spur ratio due to the phase truncation occurs when GCD (ΔP, 2^{j-k}) is equal to 2^{j-k-1}. In the worst-case the model to consider is, from (7.15),

$$E\{\varepsilon^2(n)\} = 2^{2(j-k)}\ (1/8 - (1/8)\cos(\pi n)). \tag{7.31}$$

The expected waveform is

$$\begin{aligned} E\{x(n)\} &\approx \{1 - \pi^2/2^{2k+2} + (\pi^2/2^{2k+2})\cos(\pi n)\}\sin(\frac{2\pi}{2^j}P(n)) + \mathrm{O}(2^{-3k}) \\ &= (1 - \pi^2/2^{2k+2})\sin(\frac{2\pi}{2^j}P(n)) + (\pi^2/2^{2k+2})\sin(\frac{2\pi}{2^j}P(n) + n\pi) + O(2^{-3k}), \end{aligned} \tag{7.32}$$

clearly showing the desired signal and spur components. Thus, neglecting $O(2^{-3k})$ effects, a –18 dB per bit power behavior, the worst-case spur level relative to the desired signal after truncating to k bits is [Fla95]

$$\mathrm{SpSR} \approx 10\log_{10}(\frac{\pi^4}{2^{4k+4}(1-\pi^2/2^{2k+2})^2}) \approx 10\log_{10}(\frac{\pi^4}{2^{4k+4}}) \approx 7.84 - 12.04\,k \text{ dBc.} \tag{7.33}$$

The phase dithering provides for acceleration beyond the normal 6 dB per bit spur reduction (5.25) to a 12 dB per bit spur reduction (7.33). Since the size of the ROM ($2^k \times m$) is exponentially related to the number of the phase bits, the technique results in a dramatic decrease in the ROM size. The expense of the phase dithering is the increased noise floor. However, the noise

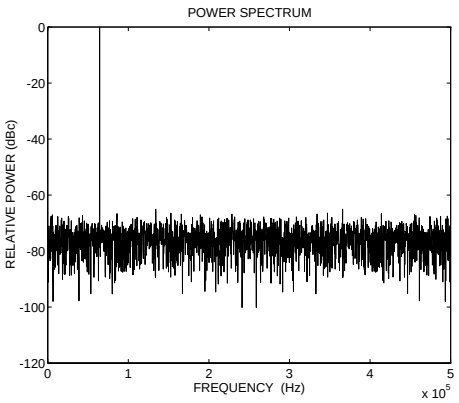

Figure 7.6. Dither is added into the phase address, when GCD (ΔP,2^{j-k}) = 1. Simulation parameters same as Figure 7.2.

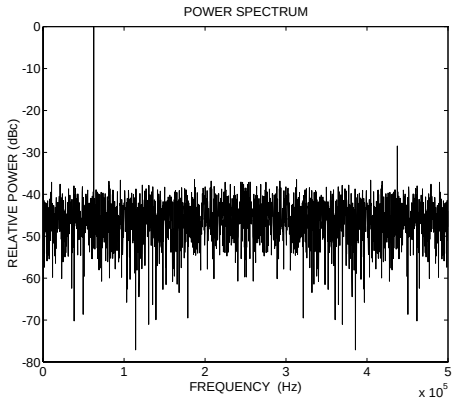

Figure 7.7. Dither is added into the phase address, when GCD (ΔP,2^{j-k}) = 2^{j-k-1} = 256. Simulation parameters: j = 12, k = 3, m = 10, ΔP = 256, f_{clk} = 1 MHz, f_{out} = 62.5 kHz.

power is spread throughout the sampling bandwidth, so the carrier-to-noise spectral density could be raised by increasing the number of the samples in (7.24), (7.25). The phase dithering requires dither generation and an adder, which makes the circuit more complex. The overflows due to dithering cause no problems in the phase address, because the phase accumulator works according to the overflow principle.

The number of the samples is 4096 in all figures in Chapter 7. The carrier-to-noise power spectral density in Figure 7.6 is 74.35 dBc per FFT bin, in agreement with the lower bound 74.34 dBc (7.25). In Figure 7.7 the carrier-to-spur level is 28.47 dBc (28.28 dBc (7.33)), and the carrier-to-noise power spectral density is 44.20 dBc, in agreement with the upper bound 44.24 dBc (7.24).

7.2.4 Non-subtractive Amplitude Dither

If a digital dither (from source 3 in Figure 7.4) is summed with the output of the phase to amplitude converter, then the output of the DDS can be expressed as

$$\sin(\frac{2\pi}{2^j}(\Delta P\, n - e_P(n))) + z_A(n) - e_A(n), \tag{7.34}$$

where $z_A(n)$ is the amplitude dither [Ker90], [Rei91], [Fla95]. The spurious performance of the D/A-converter input is the same as if the D/A-converter input were quantized to (m + x) bits [Fla95], because the $z_A(n)$ randomizes a part of the quantization error (x bits) in Figure 7.4. If the $z_A(n)$ is wideband evenly distributed on [-Δ_A/2, Δ_A/2), and independent of the $e_A(n)$, then the total amplitude noise power after dithering will be [Gra93]

$$E\{z_A^2\} + E\{e_A^2\} = \frac{\Delta_A^2}{12} + \frac{\Delta_A^2}{12}, \tag{7.35}$$

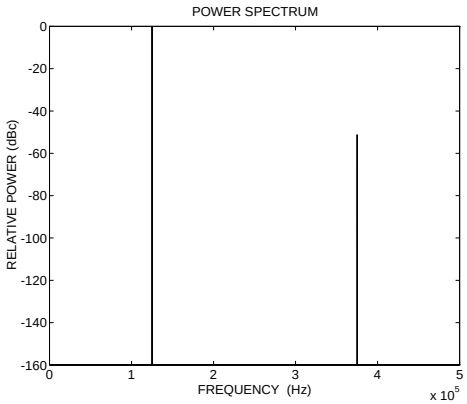

Figure 7.8. Without amplitude dithering, the carrier-to-spur level is 51.2 dBc. Simulation parameters: j, k = 12, m = 8, x = 8, ΔP = 512, f_{out} = 125 kHz, f_{clk} = 1 MHz.

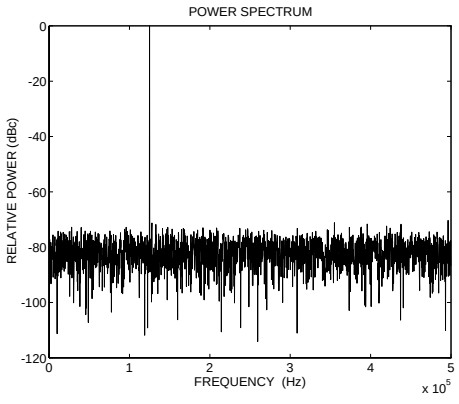

Figure 7.9. With amplitude dithering, the carrier-to-noise power spectral density is 80.1 dBc.

where $\Delta_A = 2^{-m}$, and $E\{ e_A^2 \}$ is from (5.32) or (5.34). The amplitude error power is doubled after dithering, but the error power is divided into all discrete frequency components. If the spur power is divided into the *Pe*/2 spurs (5.32), then, after dithering, the total noise power is divided into the *Pe* spurs and the carrier-to-spur power spectral density is not changed in the same measurement period (*Pe*). Then the carrier-to-noise power spectral density is the same as in (5.32)

$$\left(\frac{C}{N}\right) = (1.76 + 6.02\,m + 10\times\log_{10}\left(\frac{Pe}{4}\right)\text{dBc.} \qquad (7.36)$$

The penalty of amplitude dithering is a more complex circuit and a reduced dynamic range. In this method the size of the ROM increases by $2^k \times x$, where k is the word length of the phase address and x is the word length of the amplitude error. The output of the ROM must be reduced (scaled) so that the original signal plus the dither will stay within the non-saturating region. The loss may be small, when the number of quantization levels is large.

Figure 7.8 shows the power spectrum of a sine wave without amplitude dithering. Figure 7.9 shows the power spectrum of a 16 bit sinusoid amplitude dithered with a random sequence, which is distributed evenly over [$-2^{-8}/2$, $2^{-8}/2$), prior to the truncation into 8 bits. The carrier-to-noise power spectral density is 80.1 dBc per FFT bin (80.02 dBc (7.36)) in Figure 7.9.

For example, QUALCOMM has used the non-subtractive amplitude dither in their device [Qua91a].

7.3 Subtractive Dither

Non-subtractive dither is used to reduce the undesired spurious components, but the penalty is that the broadband noise level is quite high after dithering. To alleviate the increase in noise, subtractive dither can be used, in which the dither is added to the digital samples and subtracted from the DDS analog output signal [Twi94]. The requirement of the dither subtraction at the DDS output makes the method complex and difficult to implement in practical applications. The technique presented in this work uses a high-pass filtered dither [Car87], [Ble87], which

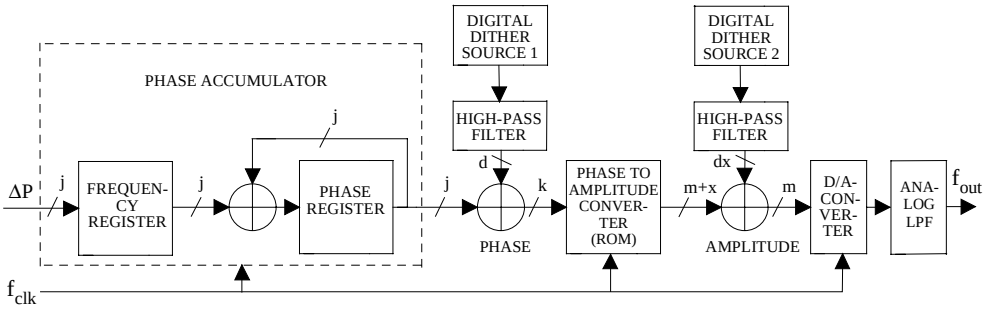

Figure 7.10. DDS with a high-pass filtered phase and amplitude dithering structures.

has most of its power in an unused spectral region between the band edge of the low-pass filter and the Nyquist frequency. After the DDS output has been passed through the low-pass filter, only a fraction of the dither power will remain [Ble87]. The low-pass filtering is a special implementation of the dither subtraction operation.

7.3.1 High-Pass Filtered Phase Dither

If a digital high-pass filtered dither signal $z_{HP}(n)$ (from source 1 in Figure 7.10) is added to the output of the phase accumulator, then the output of the DDS can be expressed as

$$\sin(\frac{2\pi}{2^j}(\Delta Pn - e_P(n) + z_{HP}(n))) - e_A(n). \tag{7.37}$$

If both the dither and the phase error are assumed to be small relative to the phase, then the DDS output signal (7.37) can be approximated by

$$\sin(2\pi\frac{f_{out}}{f_{clk}}n) + \cos(2\pi\frac{f_{out}}{f_{clk}}n)\frac{2\pi}{2^j}\left(z_{HP}(n) - e_P(n)\right) - e_A(n), \tag{7.38}$$

where f_{out} is the DDS output frequency and f_{clk} is the DDS clock frequency (2.1). The above phase dithering is in the form of an amplitude modulated sinusoid. The modulation translates the dither spectrum up and down in frequency by f_{out}, so that most of the dither power will be inside the DDS output bandwidth. So the high-pass filtered phase dither works only when the DDS output frequency is low with respect to the used clock frequency.

7.3.2 High-Pass Filtered Amplitude Dither

If a digital dither (from the source 2 in Figure 7.10) is summed with the output of the phase to amplitude converter, then the output of the DDS can be expressed as

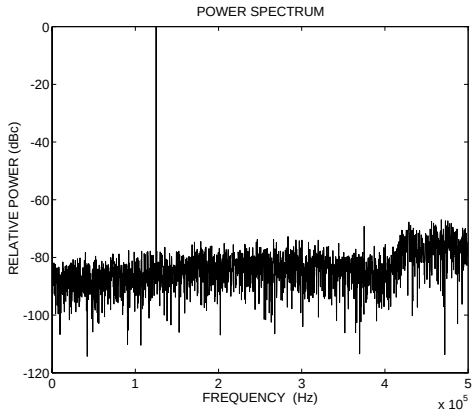

Figure 7.11. With high-pass filtered amplitude dithering, the carrier-to-spur level is increased to 69.25 dBc (see the level in Figure 7.8).

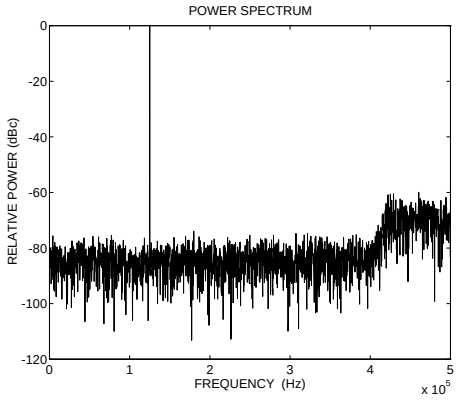

Figure 7.12. With high-pass filtered amplitude dithering, the carrier-to-noise power spectral density is 83.2 dBc (0 to 0.4 f_{clk}).

$$\sin(\frac{2\pi}{2^j}(\Delta P\, n - e_P(n))) + z_{HA}(n) - e_A(n), \tag{7.39}$$

where $z_{HA}(n)$ is the high-pass filtered amplitude dither, which has most of its power in an unused spectral region between the band edge of the low-pass filter and the Nyquist frequency. The benefits of the high-pass filtered amplitude dither are greater when it is used to randomize the D/A-converter non-linearities. The magnitude of the dither must be high in order to randomize the non-linearities of the D/A-converter [Wil91].

The high-pass filtered dither has poorer randomization properties than the wide band dither, which could be compensated by increasing the magnitude of the high-pass filtered dither [Ble87]. The spur reduction properties of the high-pass filtered amplitude dither are difficult to analyze theoretically, therefore only simulations are performed. The loss of the dynamic range is greater than in the case of the non-subtractive dither, because the magnitude of the high-pass filtered dither must be higher. However, the loss is small when the number of the quantization levels is large.

In this example the digital high-pass filter is a 4th-order Chebyshev type I filter with the cut-off frequency of 0.42 f_{clk}. Figure 7.8 shows the power spectrum of a sine wave without dithering. Figure 7.9 shows the power spectrum of a 16 bit sinusoid amplitude dithered with a random sequence that is distributed evenly over [$-2^{-8}/2$, $2^{-8}/2$), prior to truncation into 8 bits. Figure 7.11 shows the same example as Figure 7.9, but with a random sequence, which is distributed evenly over [$-2^{-7}/2$, $2^{-7}/2$). The processing is carried out by a digital high-pass filter, prior to dithering. In Figure 7.12 the amplitude range of the high-pass filtered dither is increased from over [$-2^{-7}/2$, $2^{-7}/2$) to over [$-2^{-6}/2$, $2^{-6}/2$) and so the spur reduction is accelerated. In Figure 7.12 the noise power spectral density is about 3 dB (half) lower in the DDS output bandwidth (0 to 0.4 f_{clk}) than in Figure 7.9.

7.4 Tunable Error Feedback in DDS

The error feedback (EF) technique is used to suppress low frequency quantization spurs in the DDS [Lea91a], [Lea91b]. The drawback of the conventional EF structures is that the output frequency is low with respect to the clock frequency (sampling frequency). This is necessary, because the transfer function of the EF has zero(s) at DC. A novel tunable error feedback structure in the DDS is developed in this section. In the proposed architecture the clock frequency need only be much greater than the bandwidth of output signal, whereas the output frequency could be any frequency up to somewhat below the Nyquist rate. The coefficients of the EF are tuned according to the output frequency.

The idea of the EF is to save the errors created after the quantization operation, feeding the errors back through a separate filter, in order to correct the product at the following sampling occasions [Can92]. The EF filter can be a second-order finite impulse response (FIR) filter (Figure

Table 7.1. Filter F(z) = $1 + b_1 z^{-1} + b_2 z^{-2}$

b_1	b_2	Zero	Zero*	$\frac{f_{zero}}{f_{clk}}$	$\frac{f^*_{zero}}{f_{clk}}$	$\lvert F(z)\rvert_{\infty}$ Y=2^x-1	Filter
0	0	-	-	-	-	0	-
1	0	0	-	0	-	1 × Y	LPF
-1	0	π	-	0.5	-	1 × Y	HPF
0	1	π/2	-π/2	0.25	0.75	1 × Y	BPF
-1	1	π/3	5π/3	0.1667	0.8333	2 × Y	BPF
1	1	2π/3	4π/3	0.3333	0.6667	2 × Y	BPF
2	1	π	π	0.5	0.5	3 × Y	LPF
-2	1	0	0	0	1	3 × Y	HPF

7.13). The filter creates a zero, which decreases the quantization spurs in a certain part of the frequency band. The output frequency of the DDS changes with the phase increment word (ΔP), and therefore we can make the EF filter tunable. This is carried out by changing the values of b_1 and b_2, which will move the zeros of the filter across the output frequency band. The zero(s) should be placed as near as possible to the desired output frequency. The zero frequency(ies) can be computed by solving the roots of the filter in the z-plane. Often b_1 is constrained to have powers-of-two values or zero [0, ±1, ±2] (so that the implementation requires only binary shift operations and adding/subtraction's). The values of b_2 can then only lie in [0,1]. Table 7.1 lists the properties of the filter with different b_1 and b_2 constrained like this. In Table 7.1 *x* is the word length of the error.

7.4.1 Tunable Phase Error Feedback in DDS

The EF has been placed between the phase accumulator and the ROM in Figure 7.13. It is possible to derive the following equation for the synthesizer output signal:

$$\sin\left(\frac{2\pi}{2^j}\left(\Delta P n - \left(e_P(n) + b_1\left[e_P(n-1)\right]_f + b_2\left[e_P(n-2)\right]_f\right)\right)\right) - e_A(n), \qquad (7.40)$$

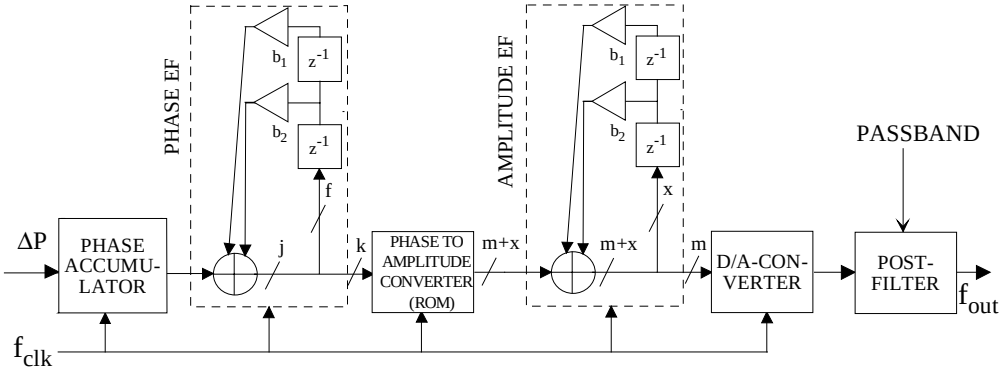

Figure 7.13. Error feedback in the DDS.

where $e_P(n)$ is the phase quantization error, f is the word length of the phase error and $e_A(n)$ is the amplitude quantization error. Here, only the phase EF is analyzed (7.40). Truncation $[]_f$ causes a secondary quantization error in the EF network. Simulations showed that the phase EF works only when the DDS output frequency is low with respect to the used clock frequency. Therefore, the coefficients of the phase EF cannot be tunable, because phase EF does not work at the higher frequencies. If the phase error is assumed small relative to the phase, then the output signal (7.40) can be approximated by

$$\sin(2\pi\frac{f_{out}}{f_{clk}}n) - \cos(2\pi\frac{f_{out}}{f_{clk}}n)\,\frac{2\pi}{2^j}\left(\sum_{q=0}^{2} e_P(n-q)\,b(q)\right) - e_A(n), \qquad (7.41)$$

where f_{out} is the DDS output frequency and f_{clk} is the DDS clock frequency (2.1). The phase EF, above, is in the form of an amplitude-modulated sinusoid. The modulation translates the error spectrum up and down in frequency by f_{out}, which explains the simulation results in the higher frequencies.

7.4.2 Tunable Amplitude Error Feedback in DDS

The EF has been placed after the ROM in Figure 7.13. It is possible to derive the following equation for the synthesizer output signal:

$$\sin(\frac{2\pi}{2^j}(\Delta P\, n - e_P(n))) - (\left[e_A(n)\right]_x + b_1\left[e_A(n-1)\right]_x + b_2\left[e_A(n-2)\right]_x), \qquad (7.42)$$

where x is the word length of the amplitude error. Here, only the amplitude EF in (7.42) is analyzed. The amplitude EF coefficients, which are given in Figure 7.14, depend on the output frequency of the DDS (Figure 7.13). The output frequencies of the DDS with the amplitude EF are divided into frequency bands, so that the amplitude error variance is minimized (the error term is assumed white). In the DDS the least significant bit of the phase accumulator input is forced

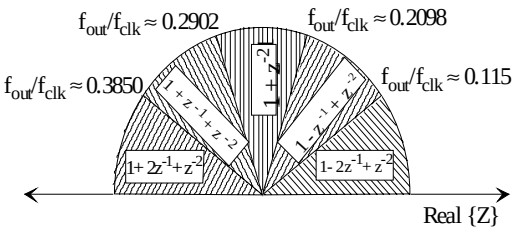

Figure 7.14. Optimal frequency bands for Table 7.1 EF coefficients.

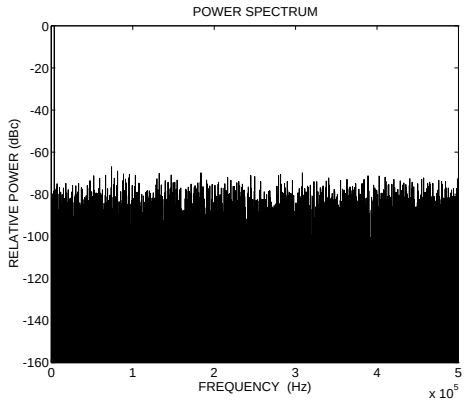

Figure 7.15. Without the amplitude EF. Simulation parameters: j = 12, k = 12, m = 8, f_{clk} = 1 MHz, $f_{out} \approx$ 3.62 kHz, ΔP = 15 and x = 8.

to one (and $j >> 1$), so that the output period (Pe) is long (2.4), and the amplitude error is approximately white (5.32) (see Figure 7.15). The amplitude EF filter coefficients, which are given in Figure 7.14, are chosen according to the output frequency of the DDS.

The penalty of the amplitude EF is a more complex circuit and a reduced dynamic range. The size of the ROM increases by $2^k \times x$, where k is the word length of the phase address and x is the word length of the amplitude error. The output of the ROM must be reduced (scaled) so that the original signal plus the maximum value of the EF will stay within the non-saturating region. The loss is small when the number of the quantization levels is large.

A computer program (Matlab) has been created to simulate the DDS in Figure 7.13, which includes EF structures. The phase accumulator length is equal to the phase address (no phase truncation) to avoid confusing the sources of the spurs. The output of the sine ROM is scaled with the maximum value of the EF filter magnitude response (3×Y in Table 7.1). In Figure 7.16 and Figure 7.17, the amplitude EF coefficients, which are chosen from Figure 7.14, depend on the output frequency of the DDS (2.1). The quantization noise at the DDS output frequencies is reduced so that a high carrier-to-noise ratio is obtained in a band around f_{out}. In Table 7.1 the tunable filter has two zeros at DC and one at $2\pi/3$, therefore the noise reduction around f_{out} is better in Figure 7.16 than in Figure 7.17.

The noise reduction properties of the EF depend on the word length of the error, the degree of the EF structure and the passband width of the analog filter at the output of the D/A-converter [Can92]. The architecture (Figure 7.13) used second-order EF but the use of higher-order EF is possible. A higher-order EF structure improves noise reduction in a band around f_{out} and gives

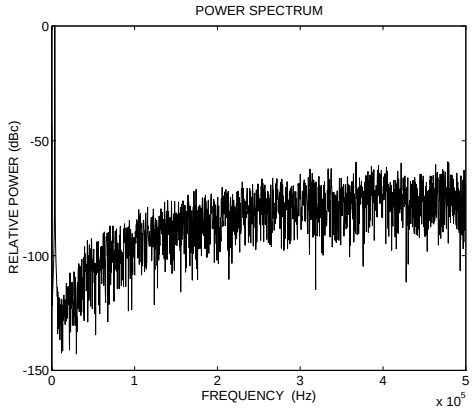

Figure 7.16. The second-order amplitude EF with coefficients b_1 = -2, b_2 = 1 ($f_{out}/f_{clk} \approx$ 0.0037). Simulation parameters same as Figure 7.15.

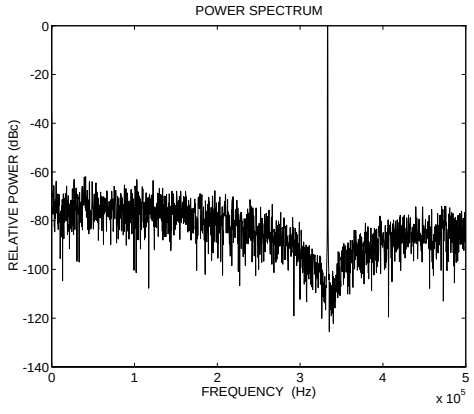

Figure 7.17. The second-order amplitude EF with coefficients b_1 = 1, b_2 = 1 ($f_{out}/f_{clk} \approx$ 0.3333). Simulation parameters: j = 12, k = 12, m = 8, ΔP = 1365, f_{clk} = 1 MHz, $f_{out} \approx$ 333 kHz.

better coverage of the DDS output bandwidth, but the penalty is a more complex circuit, and more noise further away from the DDS output. Narrower passband in the analog filter gives a better signal-to-noise ratio. The cost of narrowing the passband is that the frequency switching time of the DDS system will become slower.

The proposed DDS needs three input parameters: a phase increment word, the coefficients of the amplitude EF, and the passband of the analog filter (as in Figure 7.13 but no phase EF). The tunable analog passband filtering could be implemented, for example, with a phase-locked-loop which would tune automatically. In the proposed architecture the output frequency band is much greater than in the ordinary DDS with the fixed coefficients of the amplitude EF. The DDS with the tunable amplitude EF allows the use of a coarse resolution highly linear D/A-converter, because the spur performance is not limited by the number of bits in the D/A-converter, but rather by the linearity of the D/A-converter.

7.5 Summary

The reason why the dither techniques have not been applied very often to reduce the spurs due to the finite word length of the digital part of the DDS is because the effect of the D/A-converter non-linearities nullifies the contribution. It is difficult to implement a high-speed and highly accurate D/A-converter. With the amplitude EF, lower accuracy D/A-converters with a better inner spurious performance could be used. The problems with the amplitude EF are the increased circuit complexity and the difficulty in implementing the analog filters with variable passbands. The benefits of the high-pass filtered amplitude dither would be greater when it is used to randomize the D/A-converter non-linearities because the magnitude of the dither must be high in order to randomize the non-linearities of the D/A-converter.

8. Up-Conversion

The basic idea is that the DDS provides only a part of the output signal band, and up-conversion into the higher frequencies is carried out by analog techniques because the spurious performance and the power consumption are not good in the wide output bandwidth DDS (Figure 2.8, Figure 2.9). The critical path of the signal could be accomplished by the DDS, which has the advantages of a fast switching time, a fine frequency resolution, and a coherent frequency hopping. Three up-conversion possibilities are introduced in this chapter: a DDS/PLL hybrid, a DDS/mixer hybrid and a DDS quadrature modulator.

8.1 DDS/PLL Hybrid I

PLL synthesizers with the DDSs have been proposed. These synthesizers have the DDS in their PLL to generate the reference signal [Cra94] or to divide the output signal fractionally [Rei85], [Hie92].

The DDS could be used to provide a variable reference frequency for a following PLL [Wea90a], [Ito93]. The PLL no longer has to be designed for the frequency resolution, since the DDS can take over this task [Hir94]. This means that higher reference frequencies can be used, with such benefits as, for example, a faster frequency settling time. By linearly ramping the DDS output frequency, it is possible to keep the PLL in lock when changing the reference frequency. This can be done by continuously incrementing the digital phase increment word by a fixed value at a constant rate. In this way the locking can be maintained for a smaller loop bandwidth, meaning easier filtering of the reference sidebands [Har91]. Any multiplication of the reference frequency results in a degraded phase noise and spurs spectrum inside the loop bandwidth per the classical 20 $\log_{10}(N)$ rule [Gil90a]. Using the DDS to generate the reference frequency might not deliver the desired performance unless N is quite small, because the spuri-

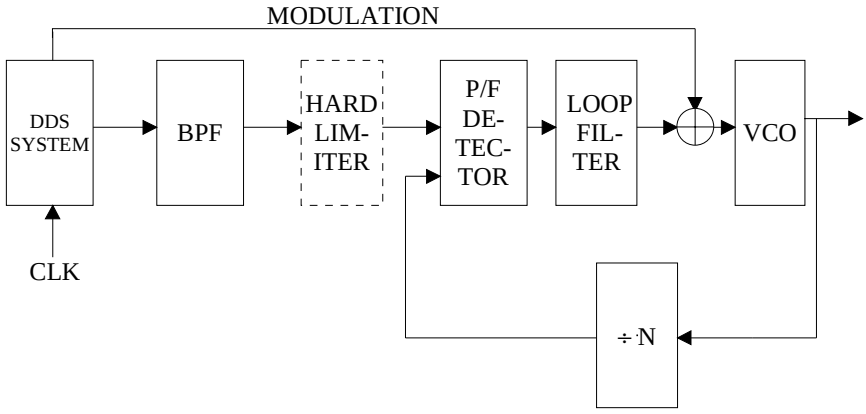

Figure 8.1. Block diagram of the hybrid DDS/PLL.

ous performance of the DDS output is not good.

If the divider in the PLL divides by integers only, then the output frequency step size is constrained to be equal to the reference frequency. In fractional synthesis the fractional divider (based on a DDS) is used instead of the integer divider in the PLL. This makes it possible to use higher reference frequencies because the output frequency step size is a fraction of the reference frequency [Cra94].

The PLL-technology has been used to generate modulation and frequency hopping in the transmitter. The simplest scheme, perhaps, one in which the modulation is applied at the voltage controlled oscillator (VCO) input [Jon91]. The change in the frequency at the VCO is sensed by the phase/frequency detector, that produces a voltage equal to the modulation, but in the opposite phase. This signal must be filtered by a loop filter to prevent the modulation from being canceled. The cut-off frequency of the loop filter should be low enough so that the loop filter attenuates all modulation frequencies. While this is essential for modulation, it inhibits a fast loop response. The modulated oscillator is only slightly better than the phase noise of the VCO, because the bandwidth of the loop is narrow. The channel spacing is achieved by changing the division ratio.

If only the reference frequency is modulated, a phase error will exist between the P/F detector inputs, because the loop cannot respond quickly to the change in the reference frequency. Therefore, the maximum data rates must be much below the loop bandwidth or else the wave shape information will be lost.

Figure 8.1 shows the DDS/PLL hybrid, where the modulation is carried out at the VCO and the reference. This method allows the loop bandwidth to be chosen independently of the modulating signal. The VCO modulation is compensated in the reference, which means that the loop bandwidth can be optimized for the phase noise performance and the frequency settling time of the PLL. In practice the difficulty is to match the tuning characteristics of the VCO and the reference. Any difference will increase the spurious modulation products in the output spectrum [Per93]. For example, in the GMSK-modulation, the absolute value of the deviation is not constant therefore it is difficult to cancel the modulation at the reference.

8.2 DDS/PLL Hybrid II

In conventional solutions, a hopping carrier signal is mixed with the single baseband CPM signal [Kop87] or I-Q signals [Suz84] in the transmitter. The frequency hopping gives frequency and interference diversities, which prevent interferences from decreasing the channel capacity [Mou92]. The hopping carrier signal is generated by a local oscillator (PLL(s)). The reference frequency of the basic PLL has to be equal to the carrier spacing specified by the system requirements because the frequency resolution of the PLL is equal to the PLL reference fre-

quency. The PLL is difficult to implement for very rapid frequency hopping, when the carrier spacing is narrow [Gar79]. That is why there must be many parallel PLLs for applications requiring rapid frequency hopping.

If the local oscillator is fixed and all the hopping carriers in the frequency band are generated digitally, then it is possible to change the carrier frequency within the symbol duration. The frequency bands can be tens of MHz. On the other hand, with high frequency output signals the high speed of the activity increases the power consumption and decreases the spurious performance.

If the frequency settling time of the PLL is below a guard time duration, then one PLL is only needed for the burst-by-burst carrier frequency hopping, and the complexity of the system is reduced. The frequency settling time of the PLL could be reduced by expanding the reference frequency to increase the natural frequency of the PLL. The frequency resolution of the PLL is degraded proportionally to an increase in the reference frequency. However, if the digital fre-

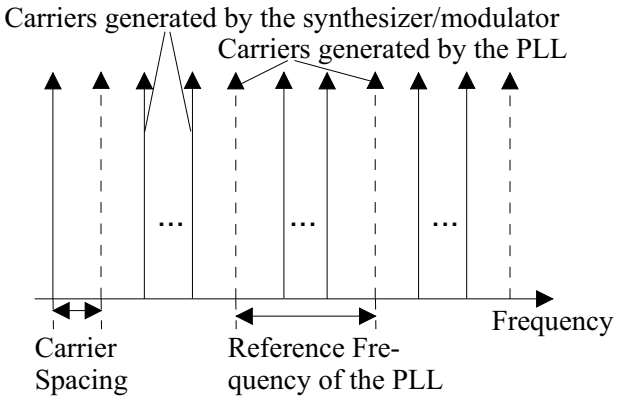

Figure 8.2. PLL generates coarse carrier frequencies, and digital frequency synthesizer/modulator interpolates between them.

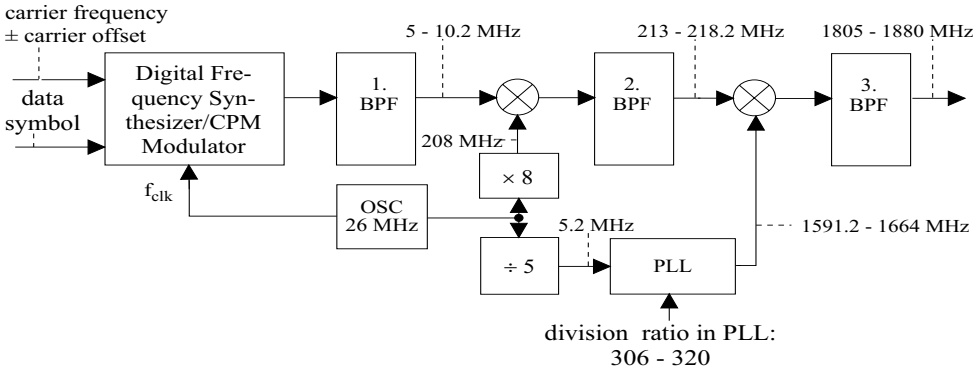

Figure 8.3. Block diagram of the architecture, which consists of the digital frequency synthesizer/CPM modulator and the RF synthesizer.

quency synthesizer/modulator interpolates the carrier frequencies between the output frequencies of the PLL [Sek94], then the reference frequency of the PLL could be increased without degrading the frequency resolution (Figure 8.2).

Figure 8.3 describes an architecture, which consists of a digital frequency synthesizer/CPM modulator and a fast frequency settling RF synthesizer with one PLL. The digital frequency synthesizer/CPM modulator interpolates the carrier frequencies between the output frequencies of the PLL (see Figure 8.2). The output frequency of the PLL is controlled by changing the programmable feedback divider ratio (integer).

The frequency settling time of the proposed architecture will be determined by the PLL, because the frequency settling time of the digital frequency synthesizer/CPM modulator is less than the symbol duration. When the frequency error is assumed to be less than the lock-in range [Gar79], the transient frequency error of the ideal second-order PLL due to a frequency step for an underdamped case is

$$f_e(t) = \Delta f\, e^{-\xi \omega_N t} \sqrt{1+(\frac{\xi}{\alpha})^2}\, \cos(\alpha\omega_N t + \tan^{-1}(\frac{\xi}{\alpha})), \tag{8.1}$$

where ξ is a damping factor (0.707), ω_N is the natural frequency of the loop, Δf is a frequency step, and α is $\sqrt{(1-\xi^2)}$. The frequency settling time is defined as the required time to reach the largest allowed frequency error (f_{ea}). The frequency settling time is achieved by equating the envelope of the transient frequency error (8.1) to the required frequency error. The frequency settling time is

$$t_s = \frac{1}{\xi\omega_N} \ln\left(\frac{\Delta f\, \sqrt{1+(\xi/\alpha)^2}}{f_{ea}}\right). \tag{8.2}$$

The reference frequency of the PLL constrains the natural frequency because the suppression of the reference spurs requires that the reference frequency is much higher than the loop filter bandwidth, which is set to the natural frequency. The natural frequency is expanded by increasing the reference frequency without degrading the frequency resolution (Figure 8.2). The frequency settling time is reduced by increasing the natural frequency (8.2). Figure 8.4 shows the frequency settling times when the frequency step is 75 MHz (from Table 8.1); the largest allowed frequency error (f_{ea}) is 20 Hz (below the frequency error specification from Table 8.1), and the natural frequency is 0.05 ω_{ref}. The reference frequency (f_{ref}) is equal to the carrier spacing (from Table 8.1) times (N_{cs}+1), where N_{cs} is the number of carriers generated digitally between the coarse carriers in Figure 8.2. The frequency settling time is reduced from 341 μs to less than 14 μs, which is less than the guard time (from Table 8.1) when twenty-five carriers are generated in the digital frequency synthesizer/CPM modulator and the PLL reference frequency is 5.2 MHz (200 kHz × (25+1)). The frequency settling time of the PLL must be shorter than half of this guard time because there must be time to smoothly reduce and raise transmit power between the bursts.

If the frequency settling time of the PLL is below the guard time, then the system needs only one PLL, and the complexity of the system is reduced. If the reference frequency of the PLL is equal to the carrier spacing, the RF synthesizer needs two PLLs to realize burst-by-burst carrier hopping with Table 8.1 values.

A large divider ratio leads to fairly high phase noise levels within the loop bandwidth. This noise can be reduced by increasing the reference frequency (decreasing feedback divider ratio). The wider PLL loop bandwidth for a given channel spacing allows reduced close-in phase noise requirements to be imposed on the voltage-controlled oscillator (VCO). With reduced close-in phase noise requirements, a lower cost VCO might be used. Adding extra poles and zeros, located far away from the natural frequency, provides more attenuation on the reference spurs without affecting the second-order nature of the loop. However, the analysis of the spurs and noise from the PLL is beyond the scope of this work.

The frequency settling time could be reduced more by employing a frequency pre-set PLL where the frequency error is set to zero when the output frequency is changed [End93]. The pretuning is difficult to adapt for aging and temperature changes therefore there will be undesirable disturbances [End93].

The frequency plan of the proposed architecture for this design example is shown in Figure 8.3. The PLL output frequency band is chosen to be outside the transmit and receive bands (from Table 8.1) in order to avoid the PLL output frequencies feed-throughs to these bands. This is achieved by choosing such a high intermediate frequency that the PLL output frequency band is lower than the receiver band. In this design example, the second bandpass filter should be a tun-

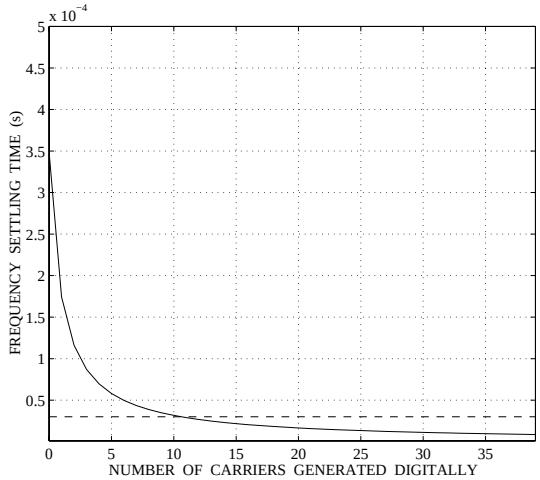

Figure 8.4. Relationship between the number of carriers generated digitally in the digital frequency synthesizer/CPM modulator and the frequency settling time of the PLL, 30 μs is the guard time (dashed line).

Table 8.1. Assumed system parameters.	
Base transmit	1805 – 1880 MHz
Base receive	1710 – 1785 MHz
Frequency band	75 MHz
Burst duration	576.9 µs
Guard time	30 µs
Symbol rate	270.833 Kb/s
Frequency error	0.05 ppm × carrier ≈ 90 Hz
Carrier spacing	200 kHz
Modulation	GMSK with BT_{sym} = 0.3

able narrowband filter in order to reduce the spurs from the D/A-converter and the first mixer. The tunable narrowband filter could be implemented by a PLL-circuit [Kop87]. The PLL loop filter bandwidth should be larger than the GMSK-modulated signal bandwidth, so that the modulation information is not lost.

8.3 DDS/Mixer Hybrid

The second scheme for up-conversion is the DDS/mixer [Gra88], [Gar91], [Yam98]. The DDS clock is provided by the constant high frequency oscillator which is the multiple of the DDS clock frequency [Wea90b], [Gil92] (Figure 8.5). Because the hopping part of the carrier frequency is accomplished digitally, the output of the local oscillator is constant. Therefore, the phase noise characteristics, the frequency accuracy and the frequency stability are easier to optimize than in the hopping local oscillator. The output from the direct digital synthesizer is connected into the mixer, where it is mixed with the high frequency local oscillator signal. The mixing process results in an infinite number of outputs at frequencies

$$\pm m f_{out} \pm n f_{LO}, \text{ where } m, n = 0, 1, 2,... \tag{8.3}$$

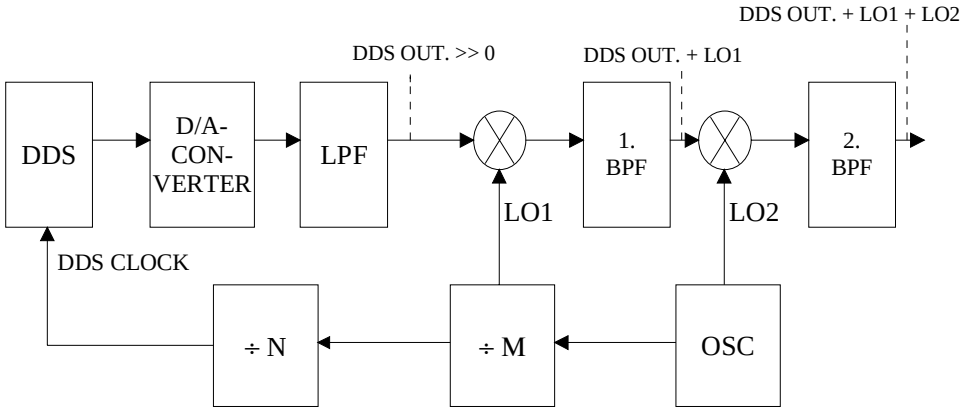

Figure 8.5. Block diagram of the hybrid DDS/mixers.

The bandpass-filter removes unwanted mirror and the spurs. The lowest output frequency of the DDS must be much higher than zero because it makes it easier to remove the unwanted mirror at the bandpass filter. It might be difficult to implement steep bandpass filters [End94], this is why there are two mixers and bandpass filters in the up-conversion chain (Figure 8.5).

In Figure 8.5 the system enables the use of the DDS without a need to notably sacrifice the other advantages obtained with the direct digital synthesizer (e.g. a fast frequency switching). The image of the D/A-converter output could be exploited in order to eliminate the LPF, the first LO and the mixer [Bje94]. The problem in using the image response in this way is that while the amplitude of the image responses decreases according to $\mathrm{sinc}(f_{out}/f_{clk})$, spurious responses due to the D/A-converter non-linearities (the higher frequency components contained in D/A-converter glitches) roll off much more slowly with the frequency.

8.4 DDS Quadrature Modulator

The third scheme for up-conversion is a quadrature modulator [Suz84]. The main problems are quadrature phase and differential gain errors between the in-phase (I) and the quadrature (Q) channels, as well as the local oscillator leakage [Roo89], because imbalances exist between the two LO components, the two anti-aliasing filters, the mixers, and the combiner. The spur levels of the best quality wideband quadrature modulators are about 40 dBc [Ota96].

The phase and amplitude of the DDS output signal are controlled by digital accuracy (see Section 2.3), so the analog errors can be pre-compensated digitally. In Figure 8.6 the method uses amplitude feedback to guide the adaptation of the DDS modulator that corrects for the carrier leakage, differential gain and phase mismatch errors. These errors vary with temperature and applied carrier frequency, therefore the readjustment is necessary. This technique has been demonstrated in [Chu81] and more recently in [Fau91], [Jon91], [Jon92], [Vin94]. In the feed-

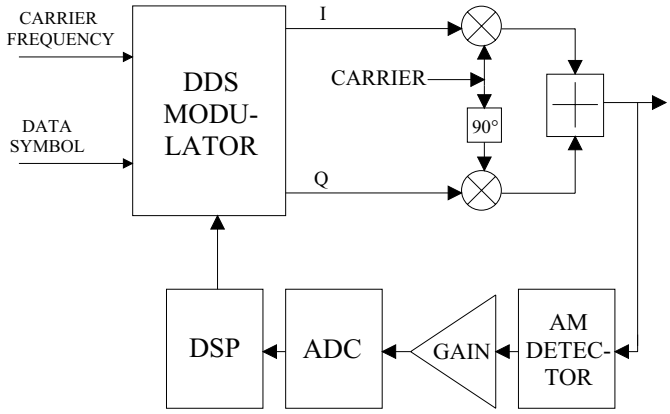

Figure 8.6. Block diagram of the quadrature modulator with the corrective feedback for a constant envelope modulation scheme.

back method the spur level is in excess of 60 dBc [Vin94]. It is possible to keep all the corrections independent of each other by applying them in the correct order [Fau91]:
1. The carrier leakage is corrected for zeroing the I and Q signals, and adjusting both DC levels until the carrier leakage is suppressed.
2. Amplitude imbalance: The amplitude of the I and Q branches are measured independently, and adjusted until both the channels are equal.
3. Phase imbalance: AM peaks and throughs are sampled, and the phase of the I and Q branches are independently adjusted until the envelope is below the desired level.

In the TDMA-system, operating in bursts, dummy slots can be assigned for correction purposes. The problem with the correction algorithms is that they require a lot of time, and the measurement of low level imbalances is difficult.

9. Direct Digital Synthesizer with an On-Chip D/A-Converter

9.1 Introduction

Traditional designs of high bandwidth frequency synthesizers employ the use of the PLL. The DDS provides many significant advantages over PLL approaches. Fast settling time, sub-Hertz frequency resolution, continuous-phase switching response and low phase noise are features easily obtainable in DDS systems. Although the principle of the DDS has been known for many years [Tie71], the DDS did not play a dominant role in wideband frequency generation until recently. Earlier DDSs were limited to producing narrow bands of closely spaced frequencies, due to limitations of digital logic and D/A-converter technologies. Recent advantages in integrated circuit (IC) technologies have brought about remarkable process in this area.

In [Nic91], [Tan95a], [Tan95b], digital parts of the DDS have been implemented with CMOS technology in one chip, and the off-chip D/A-converter is a bipolar or GaAs device. It is quite easy to increase the operating speed of the CMOS DDS up to 800 MHz by parallel architectures [Tan95b]. The D/A-converter is the bottleneck in the CMOS design, because the spectral degradation due to incomplete settling of the output and other dynamic effects restrict the operating speed of the D/A-converter below the digital part. A CMOS DDS with an on-chip D/A-converter has been reported with an operating clock frequency of 50 MHz fabricated in 1.0 µm CMOS [Cha94]. A bipolar DDS with an on-chip D/A-converter has been reported with an output bandwidth of 500 MHz fabricated in 1.0 µm silicon bipolar process with “trench” isolation [Sau90]. The power consumption of this device is 5 W in the sine wave output mode [Sau90]. The DDS presented in this section is designed and processed in BiCMOS, which allows CMOS logic functions of low power and high density to be produced on the same chip with a high-speed BiCMOS D/A-converter.

9.2 Applications and Design Requirements

DDS’s applications range from instrumentation and measurement to modern digital communications. This DDS is primarily intended for frequency agile communication systems, where fast frequency switching speed and fine frequency resolution of synthesizers are important. The primary considerations in the design of this DDS were a fine frequency resolution, spectral purity and low power dissipation.

This chip was based on a 0.8 µm double-metal double-poly BiCMOS process. The word length of the on-chip D/A-converter was selected to be 10 bits. Extra bits give no benefits at high output and clock frequencies because dynamic non-linearities dominate the D/A-converter output spectrum. To meet the distortion requirements of the 10-bit D/A-converter, the maximum clock frequency is limited to 150 MHz. The phase accumulator word length was chosen to be 32-bits

to achieve a frequency resolution of 0.0349 Hz at the clock rate of 150 MHz, according to (2.2). Since the amount of memory required to encode the entire width of the phase accumulator would be prohibitive, only 12 of the most significant bits of the accumulator output are used to calculate the sine-wave samples. The phase resolution of 12 bits results in a spurious performance due to the phase accumulator truncation of -72 dBc (5.26), which will be below the spur level of the 10-bit D/A-converter at 150 MHz.

9.3 Sine Memory Compression

A straightforward implementation of the sine memory requires a $2^{12} \times$ 10-bit ROM, whose access time reduces the maximum DDS clock frequency greatly below 150 MHz. Therefore, a sine memory compression technique is applied to reduce the size and access time of the sine ROM [Nic88].

The most elementary technique of the sine memory compression is to store only the $\pi/2$ rad of sine information, and to generate the ROM samples for the full range of 2π by exploiting the

Table 9.1. Memory compression and algorithmic techniques in the case of a 12-bit phase to 10-bit amplitude mapping.

Method	Needed ROM	Total compression ratio	Additional Circuits (not includes quarter-wave logic†)	Worst-case spur (below carrier)	Comments
Uncompressed memory	$2^{12} \times 10$ bits	1 : 1	-	-81.76 dBc	Reference
Mod. Sunderland architecture	$2^7 \times 7$ bits $2^7 \times 3$ bits	32 : 1	Adder†† Adder	-73.59 dBc	Simple
Mod. Nicholas architecture	$2^7 \times 7$ bits $2^7 \times 3$ bits	32 : 1	Adder†† Adder	-74.56 dBc	Simple
Taylor series approximation with two terms	$2^6 \times 7$ bits $2^6 \times 5$ bits	53 : 1	Adder†† Adder Multiplier	-73.28 dBc	Need multiplier
CORDIC algorithm	_	_	12 pipelined stages, 16-bit inner word length	-73.32 dBc	Much computation

† Using the quarter-wave symmetry of the sine function, complementors must be used to take the absolute value of the quarter phase and multiply the output of the sine look-up table by -1 (see Figure 6.1).
†† The word length of the sine ROM is shortened by 2-bits, because the sine ROM stores the difference between the sine amplitude and the phase. The penalty is an extra adder at the output of the sine ROM.

quarter-wave symmetry of the sine function. Beyond that, the methods of compressing the quarter-wave memory include: the trigonometric identity [Sun84], the Nicholas method [Nic88], the use of Taylor series [Wea90a], and the CORDIC algorithm [Gie91]. A computer program has been created to simulate the effects of the memory compression and algorithmic techniques on the output spectrum of the DDS. In the case of a 12-bit phase to 10-bit amplitude mapping, Table 9.1 shows how much memory and how many additional circuits are needed in each memory compression and algorithmic technique to meet the spectral requirement for the worst-case spur level, which is about -73 dBc, due to the sine memory compression. The spur level (-73 dBc) will stay below the spur level of the 10-bit D/A-converter at 150 MHz. The best compression ratio is given by the Taylor series approximation, but a multiplier is needed. In the VLSI implementation the problem of the CORDIC algorithm is in the hardware complexity. In this design the Modified Nicholas architecture is used, because it gives a lower worst-case spur level than the Sunderland architecture with the same hardware complexity.

9.3.1 Exploitation of Sine Function Symmetry

Due to the symmetry of the sine function only a quarter of the full samples are stored in the sine look-up table. The full wave output can be recovered by inverting the phase and amplitude appropriately, as shown in Figure 6.1. A 1/2 LSB offset is introduced by choosing the sine ROM samples so that there is a 1/2 LSB offset in both the phase and amplitude of the samples [Nic88], [Rub89], as shown in Figure 6.2 and Figure 6.3. Then the 1's complementors may be used in the place of 2's complementors without introducing errors, see Figure 9.1.

9.3.2 Compression of Quarter-wave Sine Function

In Figure 9.1 the size of the upper memory, whose access time is the most critical, is reduced by the sine difference algorithm [Nic88]. This saves 2 bits of amplitude in the storage of the sine function, but an extra adder is required at the coarse ROM output [Nic88]. The phase address of the quarter of the sine wave is defined as $P = a + b + c$, with the word length of the variable a to be A, the word length of b to be B, and of c to be C. In Figure 9.1 the variables a, b form the coarse ROM address, and the variables a, c form the fine ROM address. In Figure 6.6 the coarse

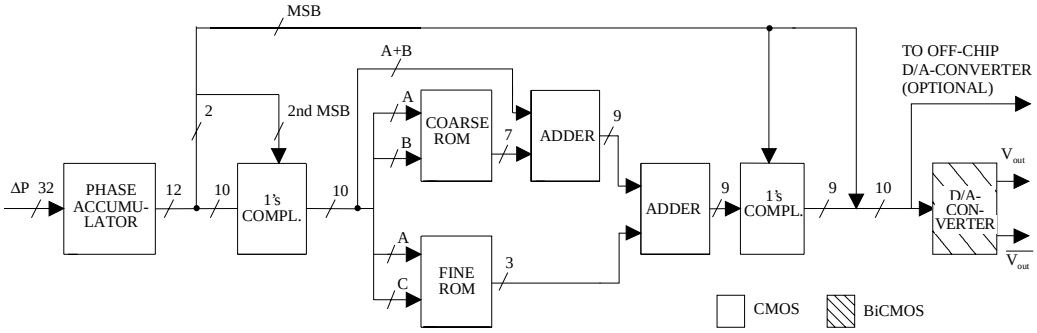

Figure 9.1. Block diagram of the DDS.

ROM samples are represented by the dot along the dashed line, and the fine ROM samples are chosen to be the difference between the value of the sine function along the dashed line and the value of the coarse ROM samples. In Figure 6.6, the function is divided into 4 regions, corresponding to a = 00, 01, 10, and 11. Within each region, only one interpolation value may be used between the sine function along the dashed line and the coarse ROM samples for all the same c values. The interpolation value used for each value of c is chosen to minimize either the mean square or the maximum absolute error of the interpolation within the region [Nic88]. Computer simulations determined that the optimum partitioning of the ROM address word lengths to provide a 10-bit phase resolution was A = 4, B = 3, and C = 3, using the notation in Figure 9.1. Simulations showed that the mean square criterion gives nearly the same maximum spur level as the minimum-maximum error criterion in this segmentation. The $2^{12} \times 10$ sine samples are compressed into $2^7 \times 7$ coarse samples and $2^7 \times 3$ fine samples resulting in a compressing ratio of 32:1. The architecture for this ROM compression technique is shown in Figure 9.1.

9.4 Phase Accumulator

In practice, the phase accumulator circuit cannot complete the 32-bit addition in a short single clock period because of the delay caused by the carry bits propagating through the adder. In order to enhance the operation to higher clock frequencies, one solution is a pipelined accumulator [Cho88], shown in Figure 9.2. To reduce the number of gate delays, a kernel carry rippling 4-bit adder is used in Figure 9.2, and the carry is latched between successive adder stages. In this way the length of the accumulator does not reduce the maximum operating speed, but the penalty is that the tuning latency increases. To maintain the valid accumulator phase during the phase increment word transition, the new phase increment word is moved into the pipeline through the delay circuit. The D-flip-flop (DFF) circuits in the input delay equalization demand substantial circuit area and power, and would impact the loading of the clock distribution net-

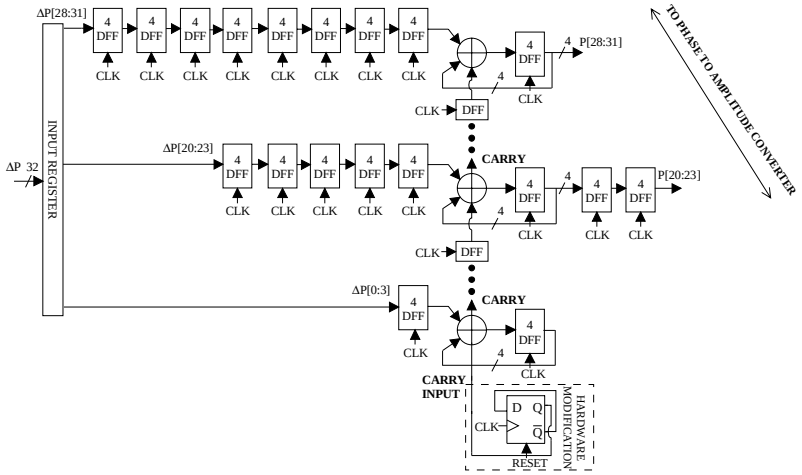

Figure 9.2. Pipelined 32-bit phase accumulator.

work.

The output delay circuitry is essentially identical to the input delay equalization circuitry, inverted so that the low-order bits have a maximum delay while the most significant bits have a minimum delay. The 12 most significant phase bits are used to calculate the sine function. Therefore only these 12 bits are delayed in Figure 9.2.

In Figure 9.2 for RESET = 1, the carry input toggles periodically between 0 and 1, with the effect of adding ½ LSB weight to the phase accumulator. This modifies the existing *j*-bit phase accumulator structure to emulate the operation of a phase accumulator with a word length of *j*+1 bits under the assumption that the least significant bit of the phase increment word is one. This causes the phase accumulator output sequence to have a maximal numerical period for all values of ΔP [Nic88]. It has an effect of randomizing errors introduced by the quantized sine ROM samples and averaging D/A-converter errors. In some phase increment words adding ½ LSB will make the output spectrum worse (see Section 7.1). Therefore, it is good that this spur reduction method is optional, depending on the phase increment word. For RESET = 0, the phase accumulator operates normally.

9.5 Circuit Design Issues

9.5.1 ROM Block Design

The block diagram of the ROM memory is shown in Figure 9.3. To achieve 150 MHz throughput, pipeline stages are inserted after the word and bit line decoding, and before the output buffer of the ROM. The first pipeline stage is latched with the falling clock edge and the next rising edge triggers the output buffers. The internal clock signal of the ROM is somewhat delayed due to buffering. This gives more time for the word and bit line decoding. The price paid for delaying the clock signal is that the stage following the memory would have less than one

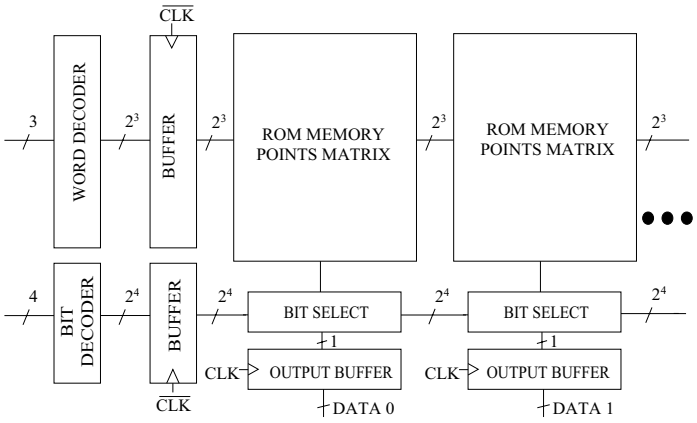

Figure 9.3. Block diagram of the ROM.

clock period to complete all transitions. The decoders for the word and bit lines use pseudo-NMOS logic [Tan95a]. This design has the advantage of being small and fast at the expense of some DC power dissipation. The high performance bit select is achieved by using a hierarchical evaluation scheme [Duh95].

In order to achieve high densities and good speed performances, the ROM memory point matrix is usually a wired-nor array. For these reasons we chose to use such an array, implemented classically using precharged logic [Duh95]. Figure 9.4 shows the ROM memory point matrix with associated word and bit lines. The memory works as follows: during precharge — high level of the clock —, all the bit lines are pulled up. The evaluating phase occurs when the clock goes low, hence conditionally discharging the bit lines. The word decoder selects a single word line, then transistors with the gate connected to that word line will turn on. Adding the ground switches between the transistors and the ground makes it possible to select the word line during the precharging. This increases the operation speed of the memory at the expense of some power dissipation, because the power consumption is increased due to the precharging and discharging of the ground lines at every clock cycle. If there is a transistor in the corner of the bit line and the selected word line, the ground switch will pull down the bit line to the ground when the clock goes low. If the transistor is absent, the bit line will remain high.

9.5.2 D/A-Converter

The designed IC-circuit has an on-chip D/A-converter, which avoids delays and line loading caused by inter-chip connections. This D/A-converter is based on a well-known weighted current array. The block diagram of the two-stage current array D/A-converter is shown in Figure 9.5. The input to the D/A-converter is converted into a differential ECL signal. One stage of registers has been inserted between the CMOS/ECL-converter and the current switches to enhance the switching speed and to ensure the simultaneous switching of all bits. The ten binary-

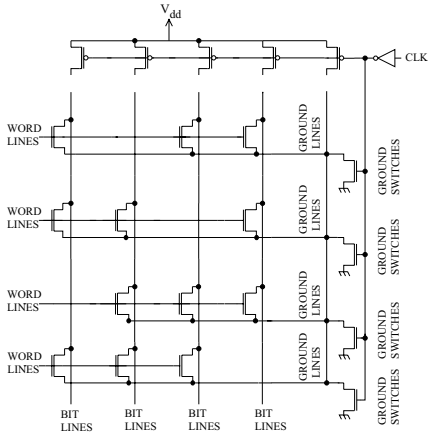

Figure 9.4. ROM memory points matrix.

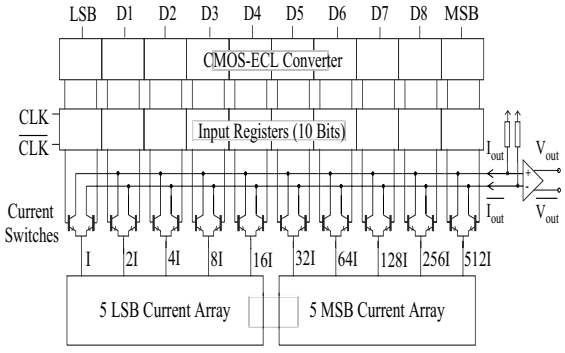

Figure 9.5. 10-bit two-stage current array D/A-converter.

weighted currents are switched to either the output branch or to the complementary output branch by current switches. The output currents are converted into voltages with resistors. Finally, there is an emitter follower buffering the output. The D/A-converter is implemented with a differential design, which results in reduced even-order distortion and provides common-mode rejection to noise.

In the two-stage weighted current array, only 31 MSB and 31 LSB equivalent unit current sources are required for a 10-bit D/A-converter. This structure saves 961 unit current sources (from 1023 to 62), compared to the straight forward current source configuration constructed from unit current sources. The reduced number of unit current sources makes it possible to design the current source transistors to be large enough to achieve a good tolerance against uncorrelated process variations, but still maintain the array to be sufficiently small to keep the mismatch due to the correlated process variations below the required level. The cascode structure is used to increase the output impedance of the unit current source, which improves the linearity of the D/A-converter.

The registers are implemented by differential current mode logic (DCML) D-flip-flops, which is faster than ECL type D-flip-flops. Figure 9.6 shows a D-flip-flop output buffer and a current switch for a single bit section. The bipolar current switch steers the current, I_1, between the two output branches. The current switch is connected to the output of the D-flip-flop buffer at the left hand-side of Figure 9.6. The D-flip-flop output buffer limits the control voltage swing and buffers between the input digital signal and the current switch.

In the process used, the MOS current switch cannot toggle the current between the complementary outputs at the clock rate of 150 MHz, so the bipolar current switch is used. Furthermore, the required control voltage swing at the input of the bipolar current switch is much lower compared to the required control voltage swing of a MOS current switch for a practical design. The problem with the bipolar switches is the error in the output current due to the finite forward current gain of the switch transistors. In Figure 9.6, the actual current I_{out} delivered to the output

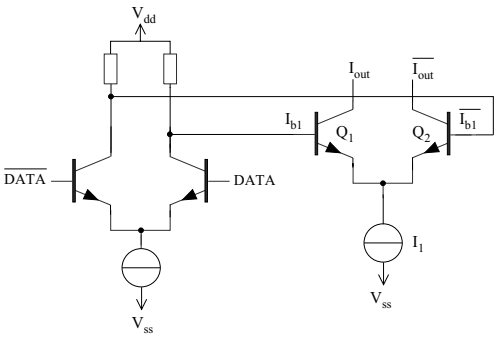

Figure 9.6. D-flip-flop output buffer and bipolar current switch.

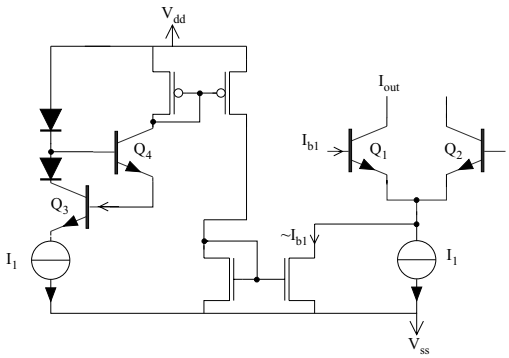

Figure 9.7. Base current compensation.

branch differs from the actual bit current I_1 by an amount equal to the base current I_{b1} of the transistor Q_1

$$I_{out} = I_1 - I_{b1} = \frac{1}{1 + \frac{1}{\beta_F}} I_1, \tag{9.4}$$

where β_F is the forward current gain of Q_1. This would only cause gain error (not errors in linearity) if the forward current gain of the transistors in all switching pairs were equal. Actually, the forward current gain depends on the magnitude of the current and the temperature, which vary over the current switches. Therefore the base currents have to be compensated to reduce linearity errors caused by variations in the forward current gain over bipolar current switch transistors. A simple way of minimizing the error is to use a Darlington-connected pair of transistors. Although this is used in some designs [Kel73], it tends to degrade the switching speed of the circuit significantly. In Figure 9.7 the idea of the base current compensation is to pre-distort the current of the binary current source (I_1) by a current which is equal to the base current of the current switch. In the base current compensation circuit a binary weighted amount of current (I_1) is driven through a bipolar transistor (Q_3), whose geometrical size is identical to the current switch transistor (Q_1). The operating point of the transistor Q_3 is set to the same as in the switch transistor Q_1 by a transistor (Q_4) and two diodes. Therefore, the base current of the transistor (Q_3) is almost the same as in the current switch transistor (Q_1). This current is mirrored with MOS current mirrors at the common emitter node of the current switches. With the base current compensation circuit the output current of the current switch transistor is approximately (see Appendix B)

Table 9.2. Power consumption and maximum operation frequency of the DDS blocks based on SPICE simulations at 25 °C.

Block of DDS	Power consumption	Maximum operation frequency
Phase accumulator	120 mW @ 5 V 40 mW @ 3.3 V	150 MHz @ 5 V 110 MHz @ 3.3 V
Rest of logic	200 mW @ 5 V 72 mW @ 3.3 V	160 MHz @ 5 V 114 MHz @ 3.3 V
ROM's	140 mW @ 5 V 50 mW @ 3.3 V	330 MHz @ 5 V 200 MHz @ 3.3 V
D/A-converter	120 mW @ 3.3 V	250 MHz @ 3.3 V†
DDS circuit	0.6 W at 150 MHz @ 5 V 0.282 W at 110 MHz @ 3.3 V	150 MHz @ 5 V 110 MHz @ 3.3 V

† The load capacitance C_L = 10 pF.

$$I_{out} \approx \frac{1}{1+\frac{2}{\beta_F^2}} I_1. \qquad (9.5)$$

Comparing (9.4) and (9.5) the error due to the finite β_F has been reduced from $1/\beta_F$ to $2/\beta_F^2$. According to the simulations the base current compensation circuit has a negligible effect on the speed of the D/A-converter.

9.5.3 Summary of the DDS Block Design

The digital parts of the chip are implemented with a CMOS design to reduce power consumption. The 10-bit D/A-converter is designed with BiCMOS technology in order to operate at a clock rate of 150 MHz. Table 9.2 shows the simulated power consumption and maximum clock frequencies for each DDS block. In Table 9.2 the bottleneck of this DDS is the phase accumulator operation speed of 150 MHz. It is quite easy to increase the operation speed of the phase accumulator and the additional logic by pipelining. But to meet the distortion requirements of the 10-bit D/A-converter, the maximum clock frequency of the DDS is limited to 150 MHz. For low power consumption applications, by reducing the supply voltage of the DDS the power consumption can be decreased from 0.6 W down to 0.28 W, but the maximum clock frequency is decreased from 150 MHz to 110 MHz (see Table 9.2).

9.5.4 Layout Considerations

A problem inherent in high-speed CMOS chips is power supply switching noise. To minimize the coupling of the switching noise from the digital logic to the output of the D/A-converter, the power supplies of the digital logic and the analog part are routed separately. Shielding between the analog signals routing and digital data lines have been used to minimize coupling between these. All the digital blocks are surrounded by guard rings, and the analog parts of the D/A-converter by double guard rings to minimize the noise injected into the analog output through the substrate. Separate pads connect the guard rings to the off-chip ground. Since the substrate is low ohmic, the most efficient way to decrease the noise coupling through the substrate is to reduce the inductance between the ground and the substrate [Su93]. In this circuit this induc-

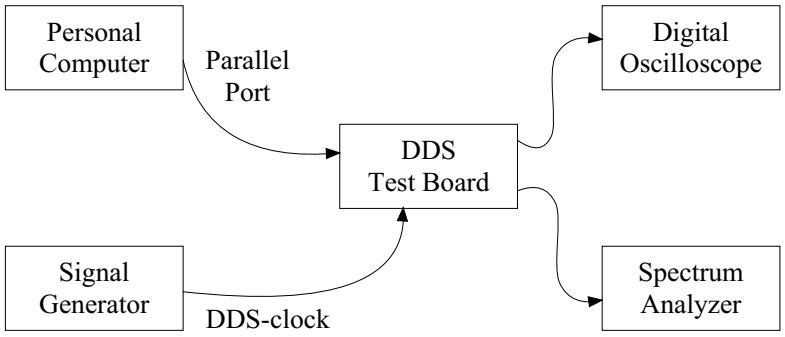

Figure 9.8. DDS test system.

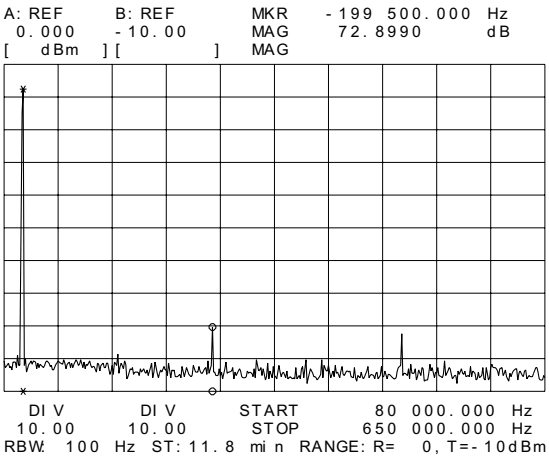

Figure 9.9. Spectrum of 0.1 MHz output sine wave, where the clock frequency is 150 MHz.

tance is small, because the ground level is connected through several bonding wires and package pins.

To eliminate process and temperature related gradients in the D/A-converter current source transistor arrays, a common-centroid layout is used [Bas91]. The D/A-converter clock controls the registers that drive the output current switches. Therefore it controls the digital-to-analog conversion process, and must be considered an analog signal. Its purity has a direct effect on the output spurs. In the layout the D/A-converter, clock signal is separated from the digital signals to prevent the switching currents from coupling onto the D/A-converter clock.

9.6 Experimental Results

To evaluate the DDS chip, a test board was built and a computer program was developed to control the measurement. In the software, the phase increment word could be written in HEX or

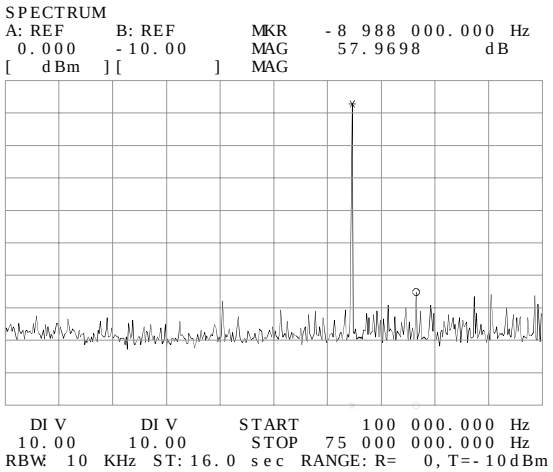

Figure 9.10. Spectrum of 48.5 MHz output sine wave, where the clock frequency is 150 MHz.

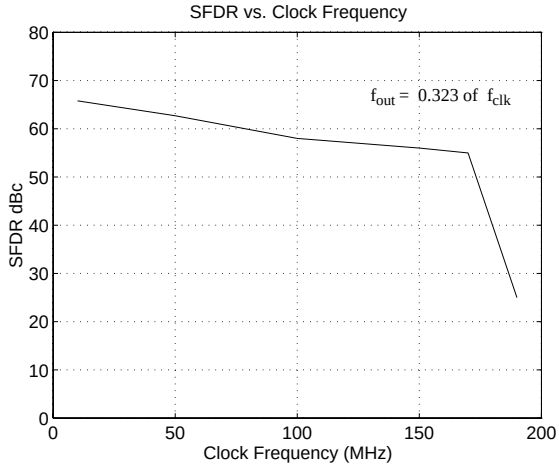

Figure 9.11. SFDR as a function of the clock frequency, for f_{out} = 0.323 of f_{clk}.

in the required frequency in MHz. In the latter case the software will calculate the corresponding phase increment word. The phase increment word and the other of the control signals are loaded into the test board via the parallel port of a personal computer. The block diagram of Figure 9.8 illustrates the DDS test system.

The effect of D/A-converter static non-linearities is investigated in Figure 9.9, where the clock frequency is 150 MHz and the output frequency is low. Even-order distortion is reduced due to the differential design. The spurious free dynamic range (SFDR) is 72.9 dBc in Figure 9.9, where the worst spurs are the third and fifth harmonics. The D/A-converter fulfills the requirement of a 10-bit static linearity.

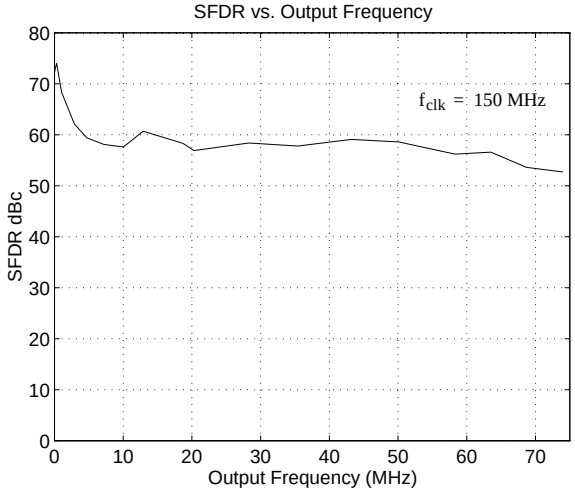

Figure 9.12. SFDR as a function of the output frequency, for f_{clk} = 150 MHz.

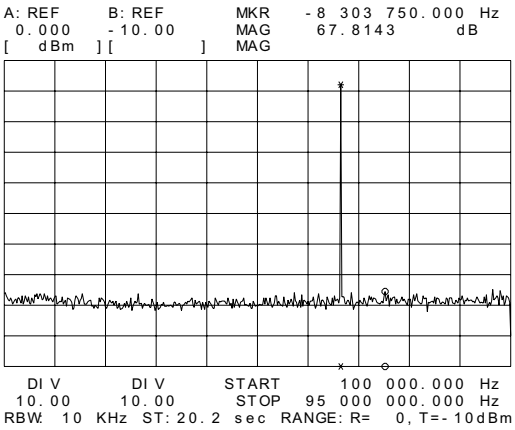

Figure 9.13. Spectrum of 63 1/3 MHz output sine wave, where the clock frequency is 190 MHz.

A DDS's worst-case close to the carrier spurs at the wideband (Nyquist bandwidth = DC to $f_{clk}/2$) typically occurs when the output frequency is tuned close to $f_{clk}/3$. The measured SFDR was 57.9 dBc at a generated frequency of 48.5 MHz in Figure 9.10, where the clock frequency is 150 MHz. The worst-case spur is the fifth aliased harmonic at 57.5 MHz ($2 \times f_{clk} - 5 \times f_{out}$). Figure 9.11 shows SFDR as a function of clock frequency, for $f_{out} = 0.323$ of f_{clk}. The phase increment word was set constant $(52C5F92C)_{16}$, and the clock frequency was swept over a range of frequencies from 10 MHz to 190 MHz. From Figure 9.11 it can be seen that with this phase increment word the DDS operates up to 170 MHz clock frequency, after which it does not produce a sine-wave at the output due to internal timing problems.

Figure 9.12 shows SFDR as a function of output frequency for a fixed clock frequency. At the 150 MHz clock frequency, the SFDR is better than 60 dBc at low synthesized frequencies, decreasing to 52 dBc at high synthesized frequencies in the output frequency band, as shown in Figure 9.12. In the high synthesized frequencies there will be output frequencies, where the SFDR is very good. For example, Figure 9.13 illustrates a spectrum plot of 63 1/3 MHz output sine wave, where the clock frequency is 190 MHz. In this case the aliased harmonics drop down to the generated frequency, and therefore the SFDR is better than 68 dBc.

The power consumption of the DDS chip agrees with simulated results of Table 9.2. Typically, the DDS operates up to the clock frequency of 190 MHz, after which, errors will occur due to the internal timing problems. However, in some phase increment words these errors will already occur at the clock rate of 180 MHz, so the maximum operating clock frequency is 170 MHz.

In the DDS the close-in phase noise is determined by the purity of the clock source. The DDS divides the clock frequency by some real number. Therefore the close-in phase noise is reduced by $20 \times \log_{10}(N)$ (5.52), where N is a division ratio between the DDS clock and output frequency. Of course, the DDS circuitry has a noise floor that, at some point, will limit this improvement.

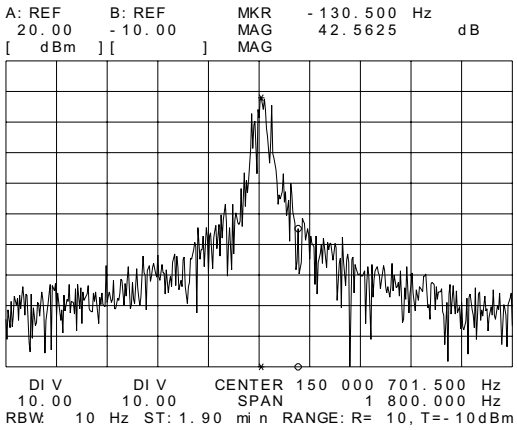

Figure 9.14. Close-in spectrum of the clock source at 150 MHz.

Figure 9.14 shows the spectrum of the clock source at 150 MHz. Figure 9.15 shows the spectrum of a 15 MHz output sine wave, where the clock frequency is 150 MHz. The relative phase noise level should improve by 20 dB ($20\times\log_{10}(10)$) (5.52). The relative power level of the phase noise at offset 130 kHz from the carrier is about 42.5 dBc in Figure 9.14 and 64.2 dBc in Figure 9.15. The relative improvement in the close-in phase noise agrees with the theory.

9.7 Summary

The DDS with an on-chip D/A-converter covers a bandwidth from DC to 75 MHz in steps of 0.0349 Hz with a frequency switching speed of 140 ns. The on-chip D/A-converter avoids delays and line loading caused by inter-chip connections. The two-stage current array D/A-converter reduces the number of the current sources, and thus simplifies the connection among

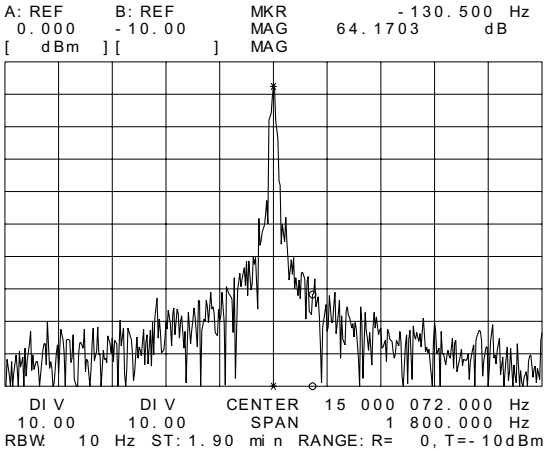

Figure 9.15. Close-in spectrum of 15 MHz output sine wave, where the clock frequency is 150 MHz.

Table 9.3. DDS chip specifications.

IC technology	0.8 μm double-metal double-poly BiCMOS
Max clock frequency	170 MHz @ 5 V
Tuning bandwidth	75 MHz (0.5 × 150 MHz)
Frequency resolution	0.0349 Hz (at 150 MHz)
Frequency switching time	140 ns (21 × 1/(150 MHz))
SFDR at low f_{out} SFDR at high f_{out}	> 60 dBc (at 150 MHz) > 52 dBc (at 150 MHz)
Transistor count	19,100
Power dissipation ($f_{out} = f_{clk}/3$)	0.6 W at 150 MHz @ 5 V
Die/Core size	12.2 mm^2/3.9 mm^2

these current sources and makes more efficient use of the chip area. At the 150 MHz clock frequency, the spurious free dynamic range (SFDR) is better than 60 dBc at low synthesized frequencies, decreasing to 52 dBc worst-case at high synthesized frequencies in the output frequency band (0 to 75 MHz). Table 9.3 summarizes chip specifications. Figure 9.16 shows the photomicrograph of the chip. This chip provides the fast frequency switching speed, fine frequency resolution and low power consumption, which are the key properties in many frequency agile communication systems.

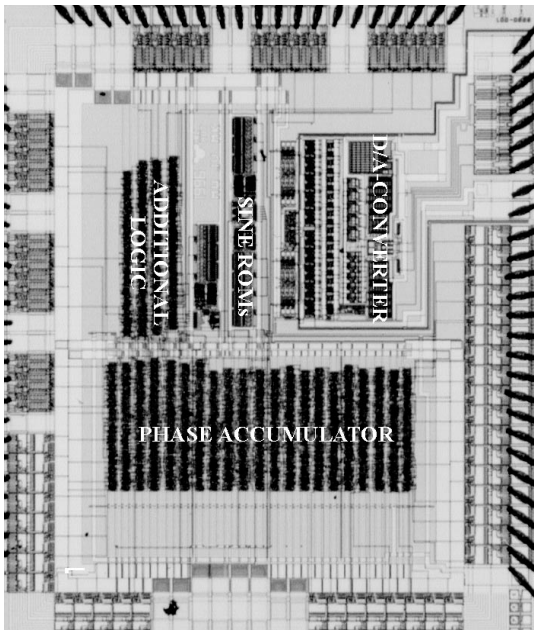

Figure 9.16. Photomicrograph of the chip.

10. CMOS Quadrature IF Frequency Synthesizer/Modulator

10.1 Introduction

Transmitter blocks are classically implemented in GaAs, Bipolar or BiCMOS technologies. The use of CMOS technologies is however much cheaper and it will become especially interesting when the analog front-end is implemented together with the digital part. The first monolithic CMOS RF transmitter has been presented in [Rof98]. The transmitter is part of a complete low-power transceiver operating in the 902-928 MHz ISM frequency band, which is one of the three Industrial, Scientific and Medicine (ISM) frequency bands opened in the USA by the Federal Communications Commission (FCC) for unlicensed spread-spectrum use.

This chapter describes a 3.3 V CMOS quadrature IF frequency synthesizer/modulator chip, which is intended for use in a wide variety of indoor/outdoor portable wireless applications in the 2.4-2.4835 GHz ISM frequency band. Frequency hopping spread spectrum (FH/SS) divides the available bandwidth into N channels and hops between these channels according to a pseudo-random (PN) code known to both the modulator and demodulator. The frequency hopping gives frequency and interference diversities, that prevent interferences from decreasing the channel capacity. FH systems may be categorized as either slow- or fast-hopping (relative to the data symbol rate). With slow hopping there are multiple data symbols per hop and with fast hopping there are multiple hops per data symbol. Systems employing M-ary frequency-shift keying (MFSK) modulation are generally fast hopping, while binary differentially coherent phase-shift keying (DPSK) modulation is often used with slow frequency hopping [Mag94]. A quadrature direct digital synthesizer (QDDS) is a core of this synthesizer/modulator, because it is ideal for signal generation of signals for the FH/SS systems. In the QDDS, it is easy to modulate both the phase and frequency with rapid carrier frequency hopping. With a variable signal to interference ratio (SIR) between hops it is better to allocate more bits to the channels (hops) with a good SIR. Therefore, a maximum throughput is achieved by adapting channel

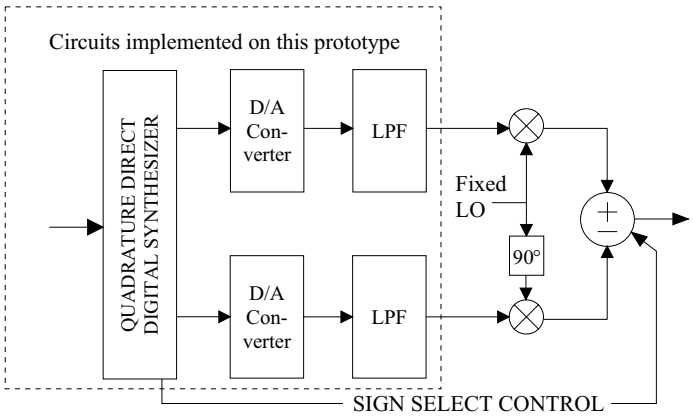

Figure 10.1. Block diagram of a synthesizer/modulator.

bandwidths, modulation formats, frequency hopping and data rates. By programming the QDDS, the adaptive channel bandwidths, modulation formats, frequency hopping and data rates are easily achieved.

The block diagram of the architecture is shown in Figure 10.1. The QDDS produces sine waves in quadrature with a frequency selectable from dc to 40 MHz. After low-pass filtering, these sine waves could be respectively up-converted by quadrature outputs from a 2.442 GHz local oscillator (LO). If the two up-converted outputs are added, the output frequency ranges from 2.442 GHz to 2.482 GHz; if they are subtracted, the frequency ranges from 2.402 to 2.442 GHz. The signed I-Q frequency synthesis architecture reduces the highest frequency required from the QDDS to 40 MHz, however this covers the desired 80 MHz hopping bandwidth. In TDD (Time-Division-Duplex) systems this architecture can use both the frequency synthesizer/modulator and a LO for the receiver, because the architecture can generate the transmit signal and the LO signal with a resolution of a few subhertz to the receiver [Rof98]. In this architecture the fixed frequency LO is used, and all the hopping carriers in the frequency band are generated by the QDDS. Then a voltage control oscillator (VCO) could be embedded in a wideband PLL. The wide PLL loop bandwidth allows reduced close-in phase noise requirements to be imposed on the VCO.

10.2 Design Requirements

The QDDS produces sine waves in quadrature from dc to 40 MHz. If the QDDS generates frequencies close to one half of the clock frequency, the first image becomes more difficult to filter. If the QDDS output band is limited to approximately 30% of the clock frequency, then the transition band of the on-chip filter is not so steep. To meet this requirement, the clock frequency of the QDDS was chosen to be 150 MHz. The word length of the on-chip digital-to-analog (D/A) converters was selected to be 10 b. Extra bits give no benefits at high output and clock frequencies, because dynamic non-linearities dominate the D/A converter output spectrum. The phase accumulator word length was chosen to be 32 bits to achieve a frequency resolution of 0.0349 Hz at the clock rate of 150 MHz (2.2). Since the amount of memory required to encode the entire width of the phase accumulator would be prohibitive, only 12 of the most significant bits of the accumulator output are used to calculate the sine wave samples. The phase resolution of 12 bits results in a spurious performance due to the phase accumulator truncation of -72 dBc [Nic88]. The 12-bit phase and the 10-bit amplitude resolution are required to obtain the worst-case digital output spectral purity of -70 dBc [Yam98], which will be below the spur level of the 10-bit D/A-converter at 150 MHz.

The images of the D/A converter output must be removed by a lowpass filter (LPF), otherwise there will be in-band intermodulation products after up-conversion mixing. An alternative method is to use a large over-sampling ratio between the D/A converter output and clock frequency [Rof98]. The images are suppressed by an off-chip bandpass filter [Rof98]. This method

requires a high over-sampling ratio, because the image frequencies must be higher than the output frequency band plus the transition band of the off-chip bandpass filter. This leads to high power consumption and D/A converter output spectrum degradation due to the high clock frequency. Furthermore, up-conversion mixers must be highly linear to avoid in-band spurs. It should be pointed out that the method in [Rof98] performs bandpass filtering after mixing, whereas the system here performs lowpass filtering before mixing.

The lowpass filter requirements are: a cut-off frequency of 50 MHz, a stopband attenuation more than 60 dB, a passband ripple of 0.5 dB and a stopband edge of 100 MHz. A low-order realization is used to reduce the size and power consumption. A fifth-order elliptic filter fulfills the requirements (see Table 6.2). The elliptic filter has a peaking in the group delay response around the cut-off frequency. High frequency parasitic problems generally result in a peaking in the amplitude response around the cut-off frequency. For these reasons, the cut-off frequency of the filter is 10 MHz above the QDDS maximum output frequency.

10.3 Quadrature IF Direct Digital Synthesizer

10.3.1 Direct Digital Synthesizer with Quadrature Outputs

The QDDS architecture used in this design was originally introduced in [Tie71]. The block diagram of the QDDS is shown in Figure 10.2. The input word (phase increment word) to the phase accumulator controls the frequency of the generated sine/cosine wave. The phase value is generated by using the modulo 2^{32} overflowing property of a 32-bit phase accumulator. The rate of the overflow is the output frequency. The phase accumulator addresses the sine/cosine read only memories (ROMs), which convert the phase information into the values of a sine/cosine wave. The sine/cosine ROM outputs are fed to the D/A converters, which develop a quantized analog sine/cosine wave.

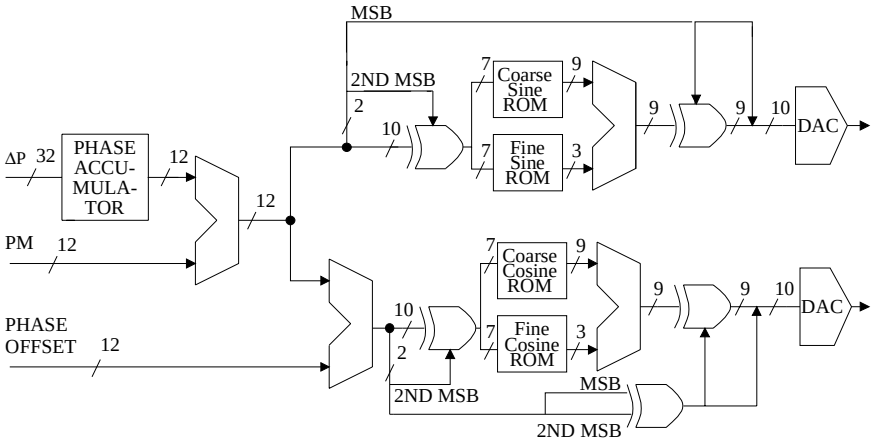

Figure 10.2. Block diagram of a quadrature direct digital synthesizer.

A straightforward implementation of the sine/cosine memory requires $2 \times 2^{12} \times 10$-bit ROMs, which access time reduce the maximum QDDS clock frequency considerably below 150 MHz. Therefore a sine/cosine memory compression technique is applied to reduce the size and access time of the sine/cosine ROMs [Tan95a]. This QDDS architecture takes advantage of the quarter-wave symmetry of a sine/cosine wave to reduce ROM storage requirements. Alternately, one could take advantage of the eighth wave symmetry of a sine and cosine waveform [McC84], [Tan95a]. Sine and cosine samples need only be stored from 0 to $\pi/4$. Due to a correction possibility of quadrature modulator analog phase errors by a digital phase distortion, the sine and cosine branches are not necessary in quadrature in the digital domain (see Section 10.3.3). So this more efficient sine/cosine memory compression method cannot be used. The word length of the sine/cosine ROMs could be shortened by 2 b, when the sine/cosine ROMs store the difference between the sine/cosine amplitude and phase (storing $[\sin(\pi x/2)-x]$ and $[\cos(\pi x/2)-\overline{x}]$, where x is a phase address) [Tan95a]. The trade-off is extra adders at the output of the sine/cosine ROMs to perform the operations ($[\sin(\pi x/2)-x] + x$) and ($[\cos(\pi x/2)-\overline{x}] + \overline{x}$). This method is not used, because the extra adders counteract the benefits in the chip area, and the 2-bit reduction in the output has a negligible effect on the speed of the ROMs in this design.

The coarse sine/cosine ROMs provide low resolution samples, and the fine sine/cosine ROMs give additional resolution by interpolating between the low resolution samples in Figure 10.2. The $2^{12} \times 10$ sine/cosine samples are compressed into $2^7 \times 7$ coarse samples and $2^7 \times 3$ fine samples, resulting in a compressing ratio of 32:1. A FFT of the compressed ROM contents gives the worst-case digital output spectral purity to be -74 dBc. However, the phase accumulator truncation to 12 bits is still the source of the worst-case digital output spur.

10.3.2 Modulation Capabilities

The chip has modulation capabilities that include a frequency and phase modulation. The frequency modulation could be superimposed on the hopping carrier by simply adding and subtracting a frequency offset to/from the phase increment word (ΔP). The phase modulation is accomplished by adding a phase modulation word (*PM*) to the phase accumulator output before addressing the sine/cosine ROMs. The chip accepts a 12-bit word for phase modulation.

10.3.3 Phase Offset

The I and Q components entering from the QDDS-based quadrature modulator pass through the active lowpass filter and mixer combination, which results in phase differences between the two output branches. The phase splitter at the fixed frequency LO does not produce an exact $\pi/2$ separation due to process variations, so two LO signals departure from the quadrature. For instance, with a 5 degree phase mismatch, the maximum achievable single side-band suppression is only 27.2 dB. These phase errors could be compensated by phase pre-distortion [Jon91], which is accomplished by adding a phase offset to the cosine phase value in Figure 10.2. The phase offset value can be adjusted with DSP techniques as described in [Jon91]. The resolution

of the phase offset is 0.088° ($360°/2^{12}$). Assuming the amplitude balance between the two branches is perfect, the image rejection is more than 62 dBc with this phase offset resolution. Furthermore, amplitude imbalances and LO leakage could be compensated by an algorithm described in [Fau91]. Test vector signals for this algorithm could be generated from sine/cosine ROMs by selecting appropriate phase addresses with the phase offset and phase modulation words.

The sign select control in Figure 10.1 is implemented digitally. After adding a 180° phase offset to the phase offset register, the two branches are added (see Appendix C). Without this phase offset the two branches are subtracted. Thus the lower or higher sideband is selected.

10.4 Circuit Design

10.4.1 Phase Accumulator

A full adder with a word length of 32 bits is necessary to produce the phase address for the sine/cosine ROMs. One possible candidate for this design is a pipelined carry ripple adder. To achieve 150 MHz operation, a kernel carry rippling 4-bit adder must be used. Due to the large word length needed, this adder would have to be extensively pipelined. This would result in the use of many registers and would impact the loading of the clock network. To reduce the latency and number of pipeline stages, a carry increment adder (CIA) is used (see Figure 10.3). In the CIA the sum and carry-out are computed at the first stage for carry-in zero (FAC = 0). In the second stage, the carry-in is used to pass or increment the pre-computed sum (incS) and carry-out (incCo) for a carry-in of one. The gates in the first block of the CIA are the well known generate (AND) and propagate (XOR) cells, while the increment can be computed using an XOR for the sum and an AND-OR for the carry-out. The 1-bit carry increment adder is extended to a 2-bit adder. The delay from carry-in to carry-out of the 2-bit adder is a single AND-OR gate delay. An 8-bit kernel adder of the phase accumulator is composed of four 2-bit adders. To achieve 150 MHz throughput, the carry is latched between successive 8-bit kernel adder

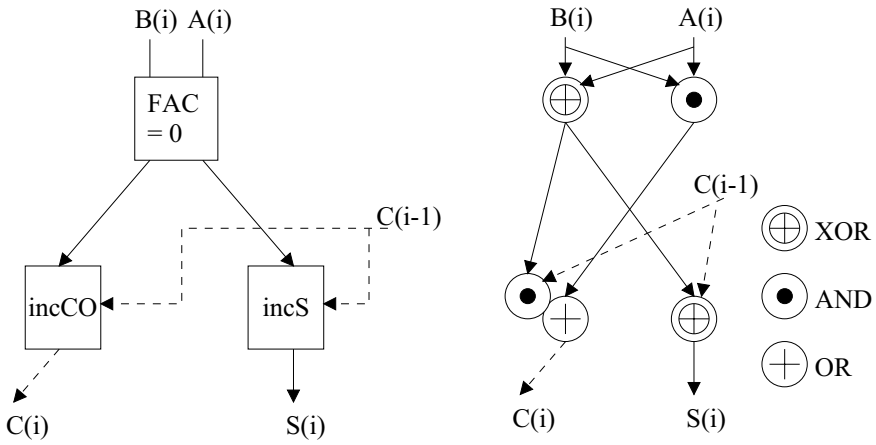

Figure 10.3. 1-bit full adder structure implemented in CIA logic, logic diagram of the CIA.

Table 10.1. Power consumption and maximum operation frequency of the QDDS blocks based on SPICE simulations with worst-case parameters.

Block of QDDS	Power consumption at 150 MHz (f_{out} = 1/3 of f_{clk})	Maximum operation frequency
Phase accumulator	40 mW at 3.3 V	150 MHz at 3.3 V
Additional logic	94 mW at 3.3 V	150 MHz at 3.3 V
ROMs	160 mW at 3.3 V	220 MHz at 3.3 V
D/A converters	20 mW at 3.3 V	250 MHz at 3.3 V
QDDS circuit	314 mW at 3.3 V	150 MHz at 3.3 V

stages. To meet the parallel input/output requirements, skewing registers are inserted into the phase accumulator for pre-skewing and de-skewing purpose.

To reduce the cycle time and size of pipeline stages further, the outputs of the 8-bit adder and the D-flip-flops are combined to form "logic-flip-flop" (L-FF) pipeline stages [Yua89], [Rog96]. Thereby, their individual delays are shared, resulting in a shorter cycle time and a smaller area. Table 10.1 summarizes the maximum operation speed and power consumption of different QDDS blocks.

10.4.2 ROM Block

The decoders for the word and bit lines use pseudo-NMOS logic [Tan95a]. The high performance bit selection is achieved by using a hierarchical evaluation scheme [Duh95]. To achieve high densities and good speed performances, the ROM memory point matrix is a wired-NOR array implementation in which a set of MOS transistors is connected in parallel to a bit line. Details pertaining to the design of the ROM block are discussed in Section 9.5.1.

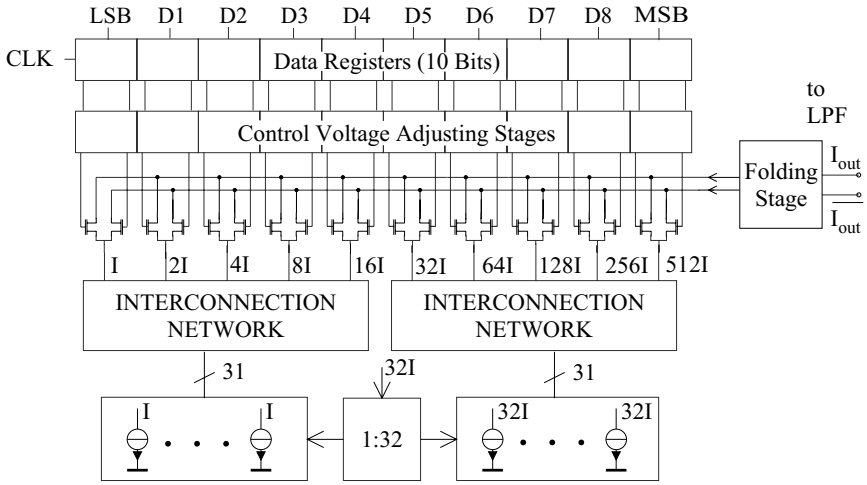

Figure 10.4. 10-bit two-stage current array D/A converter.

10.4.3 D/A Converter

The segmentation of a few of the most significant bits is usually used to minimize the glitch energy at the code where MSB switches from zero to one, and all other bits switch from one to zero. Simulations show that the following on-chip lowpass filters determine the worst-case spurious signal, therefore the segment architecture is not used.

The 10-bit D/A converter topology in Section 9.5.2 is design by CMOS technology in this section. In the two-stage weighted current array, only 31 most significant bit (MSB) and 31 least significant bit (LSB) equivalent unit current sources are required for a 10-bit D/A converter (see Section 9.5.2). The proper weighting between the two current arrays is realized with the bias current ratio of 1:32 in Figure 10.4. In the case of a 10-bit D/A-converter, an error in the bias current ratio must be below 1.7 %, and then the error in linearity is less than ± ½ LSB [Wal97]. In the two-stage current array the bias current to the LSB current array is generated from the MSB current array. This is often done in bipolar designs, but also applied in CMOS [Chi94]. In this D/A converter these two bias currents are generated with current mirrors from the reference current. This solution is better suited to low voltage realizations. The cascode folding stage sets the voltage range of the D/A converter output compatible with the lowpass filter input in Figure 10.4.

The voltage variation in the common source node of the differential pair causes the stray capacitance to be charged and discharged, which in turn slows down the settling of the output current. The voltage variation is minimized by overlapping the control signals in such a way that their cross point lies slightly below the maximum voltage level, as shown in Figure 10.5. This is done using a differential buffer with a cross-coupled PMOS load. The capacitive coupling to the analog output is minimized by limiting the amplitudes of the control signals to be just high enough to switch the tail current completely to the desired output branch of the differential pair.

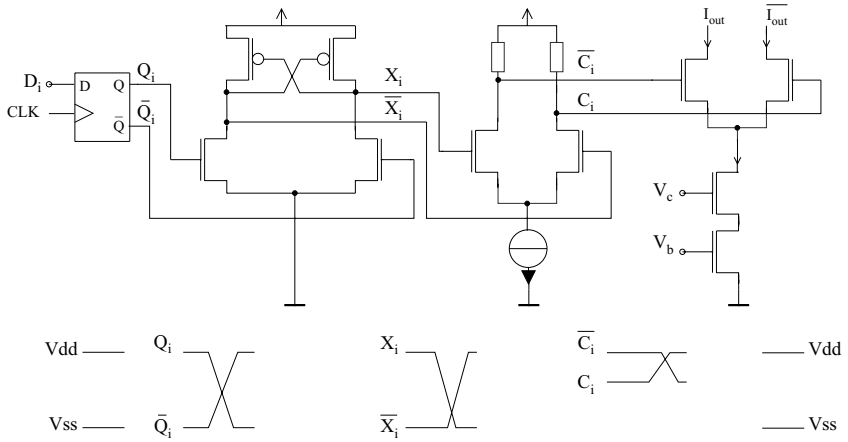

Figure 10.5. Control voltage adjusting stage and current switch. Control waveform is shown below the schematic.

The amplitude limited control waveform is obtained from the output of a source-coupled pair loaded with resistors. Short channel switch transistors were used to achieve the maximum speed and minimum glitch energy, and cascode current sources were used to produce a high output impedance.

10.4.4 Lowpass Filter

The continuous time lowpass filter is realized with a G_m - C technique, which is suitable for the design of low-voltage high frequency filters [Kol98]. The basic building block in this filter is a current integrator. The current mode topology is selected, because the D/A converter output has a current output. So an additional I-V converter is avoided. A circuit realization of a lossy integrator using a multi-output linearized transconductor is presented in Figure 10.6. In order to increase the impedance seen by the integrating node, an additional transimpedance driver has been developed. It provides a low impedance load to the transconductance block and high impedance in parallel with the integrating capacitor. A high transimpedance is achieved with the cascode current source (MP1-6) which is controlled by a common-mode feedback (CMFB) loop. The block of the CMFB consists of a common-mode sensing double differential pair [Kos98].

For better simulation accuracy a linearization method using MOS transistors operating in one operation region only is preferred. This operation region is preferably the saturation region because of the better speed and noise performance compared to other operation regions. The linearity of the transconductor was improved by using dynamic biasing [Dup90], which provides good linearization also at high frequencies. It makes it also possible to use relatively large sig-

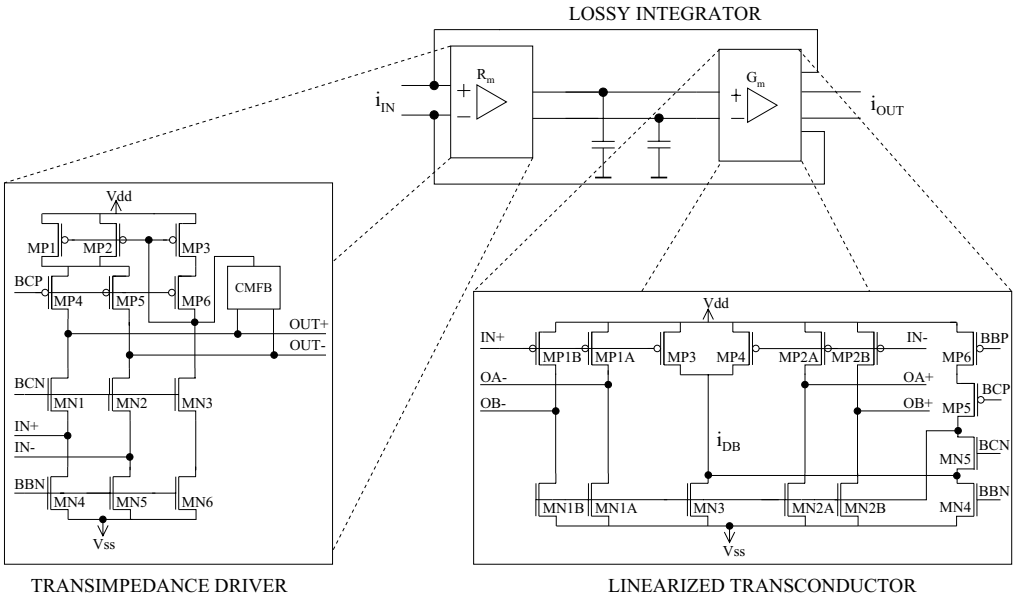

Figure 10.6. Principle of a lossy current mode Gm - C integrator using dynamic biasing.

nal currents compared to the bias current [Kol98]. This is not possible in a current mirror approach [Lee93] where bias currents should be very large compared to the signal currents in order for there to be good distortion properties.

In Figure 10.6 the transconductor uses PMOS transistors as main elements (MP1A-2B) and the dynamic biasing is generated by a PMOS differential pair (MP3 and MP4) [Kos98]. A dynamic bias current is generated by taking the common source current of the PMOS differential pair

$$i_{DB} = i_{D1} + i_{D2} = \frac{\beta}{2}\left(\frac{v_d}{2} + V_{CM} - V_T\right)^2 + \frac{\beta}{2}\left(-\frac{v_d}{2} + V_{CM} - V_T\right)^2 = \beta\left(V_{CM} - V_T\right)^2 + \frac{\beta}{4}v_d^2. \quad (10.1)$$

The above equation shows that the bias current depends on the square of the common-mode input voltage V_{CM} and the square of the differential input voltage v_d. This generated bias current (i_{DB}) is subtracted from both drain currents of the output transistors (MP1A-2B) by a NMOS current mirror (MN3 and MN1A-2B) with a mirroring ratio of ½. The results are output currents:

$$i_{oA+} = i_{oB+} = i_{D1} - \frac{i_{DB}}{2} = \frac{\beta}{2}\left(\frac{v_d}{2} + V_{CM} - V_T\right)^2 - \frac{\beta}{2}\left(V_{CM} - V_T\right)^2 - \frac{\beta}{8}v_d^2 = \frac{\beta}{2}v_d\left(V_{CM} - V_T\right), \quad (10.2)$$

$$i_{oA-} = i_{oB-} = i_{D2} - \frac{i_{DB}}{2} = \frac{\beta}{2}\left(-\frac{v_d}{2} + V_{CM} - V_T\right)^2 - \frac{\beta}{2}\left(V_{CM} - V_T\right)^2 - \frac{\beta}{8}v_d^2 = -\frac{\beta}{2}v_d\left(V_{CM} - V_T\right), \quad (10.3)$$

which depend linearly on v_d, and the V_{CM}-V_T sets the transconductance. Because the transconductance depends on the common-mode input voltage V_{CM}, the CMFB loop is needed to set the common-mode voltage at the transconductor input in Figure 10.6. The linearization accuracy is degraded by transistor mismatches. However, due to the balanced structure, the even-order distortion terms are reduced. In order to minimize the effect of the channel length modulation the common drain node of transistors MP3, MP4 and MN3 is set to the same potential as the transimpedance driver inputs. This is done by a cascode structure of transistors MN4-5 and MP5-6.

The ladder filter implementation of the fifth order elliptic filter is presented in Figure 10.7. Net phase lag errors are minimized by adding extra zeros with additional series resistors in the second and fourth integrator. The resistance R_Z is realized with a diode connected NMOS transistor biased in the saturation region. The value of the resistor can be controlled by adjusting the bias current of the transistor. To reduce the level of distortions, scaling for minimum distortions has

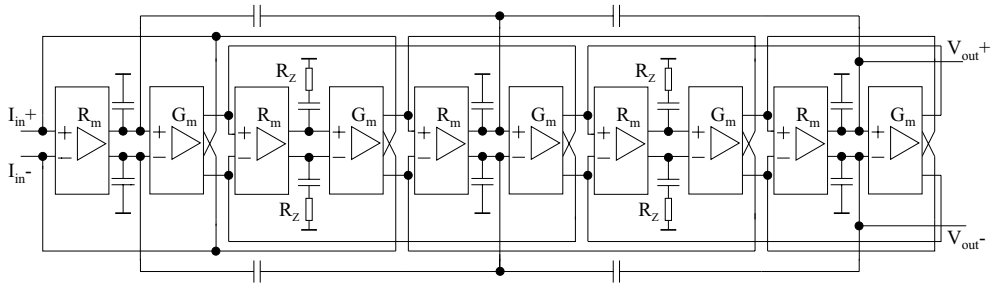

Figure 10.7. Realized filter.

Table 10.2. Simulated filter performance.

Cut-off frequency	50 MHz
Stopband rejection (f > 100 MHz)	> 52 dB
THD (input current 500 μA_{pp})	-55 dBc (0.18 %) @ 15 MHz
RMS noise (50 MHz BW)	160 μV_{RMS} @ Output Voltage 320 mV_{pp}
Dynamic range	57 dB (0.18% THD)
Power dissipation	91 mW at 3.3 V
Filter area	0.56 mm^2

been carried out. Details pertaining to the design of the lowpass filters are discussed in [Kos98].

Table 10.2 shows the simulated performance of the filter. Relatively high power dissipation is due to the large current amplitude at the input of the filter. In order to keep the distortion level low and to have a large dynamic range, the bias current has to be kept at the same level as the maximum peak signal current. The dynamic range, defined as the input signal amplitude at 0.18 % THD (total harmonic distortion) divided by the total rms noise integrated over 50 MHz, was 57 dB.

10.4.5 Layout

A problem inherent in high-speed CMOS chips is switching noise. The analog parts of this chip are implemented with a balanced design, which results in reduced even-order harmonics and provides common-mode rejection to disturbances. The layout is symmetric to obtain a good cancellation of common mode disturbances. To minimize the coupling of the switching noise from the digital logic to the analog output, the power supplies of the digital logic and the analog part are routed separately. To reduce the supply ripples even further, additional supply and ground pins are used to reduce the overall inductance of packaging. Since the substrate is low ohmic, the most efficient way to decrease the noise coupling through the substrate is to reduce the inductance between the ground and the substrate [Su93]. In this circuit this inductance is small, because a die with a conductive glue on the backplane is connected to the ground level

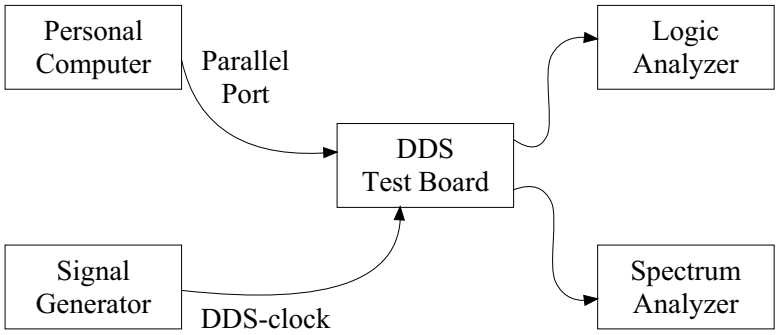

Figure 10.8. Evaluation system.

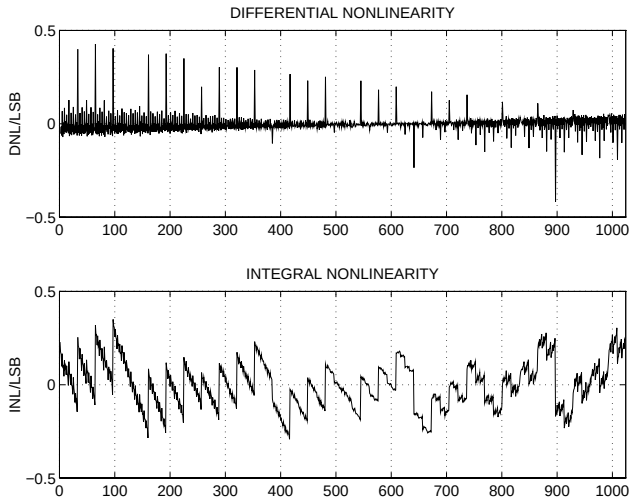

Figure 10.9. Measured DNL error is 0.43 LSB and INL error is 0.35 LSB.

through several bonding wires and package pins. Furthermore, all digital and analog parts are surrounded by separate guard rings to minimize noise coupling to the analog output through the substrate. Separate pads connect the guard rings to the off-chip ground.

To eliminate process related gradients in the D/A converter current source transistor arrays, the unit current sources are distributed in common centroid arrays, surrounded by dummy transistors [Bas91]. Equal substrate potential over the array is guaranteed by adding substrate contacts between the transistors.

10.5 Experimental Results

To evaluate the IC, a test board was built, and a computer program was developed to control the

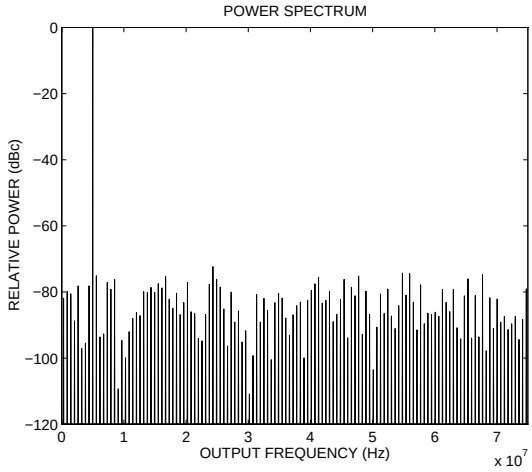

Figure 10.10. Spectrum plot of a 5 MHz digital output.

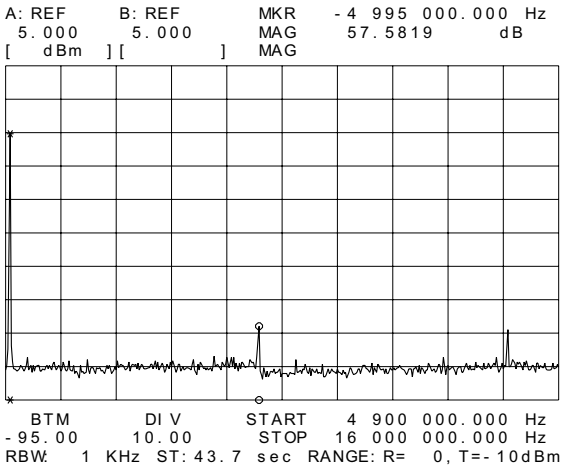

Figure 10.11. Spectrum of 5 MHz output sine wave at the D/A converter output, where the clock frequency is 150 MHz.

measurement. The phase increment word and other control signals are loaded into the test board via the parallel port of a personal computer. In a measurement set-up, the packaged chip is mounted on a 2-layer printed-circuit board. The evaluation system is shown in Figure 10.8.

A separate chip with the D/A converter utilized by this frequency synthesizer/modulator has also been fabricated. Figure 10.9 shows that typical integral linearity (INL) and differential linearity (DNL) errors are 0.43 and 0.35 LSB, respectively. In measurements, the clock frequency of the QDDS was 150 MHz. Figure 10.10 illustrates a spectrum plot of a 5 MHz output sine wave at the digital output. The spurious free dynamic range (SFDR) is 72.2 dBc. In the QDDSs, most of the spurs are generated less by digital errors (truncation or quantization errors) and more by analog errors in the D/A converter and the lowpass filter such as clock feed-

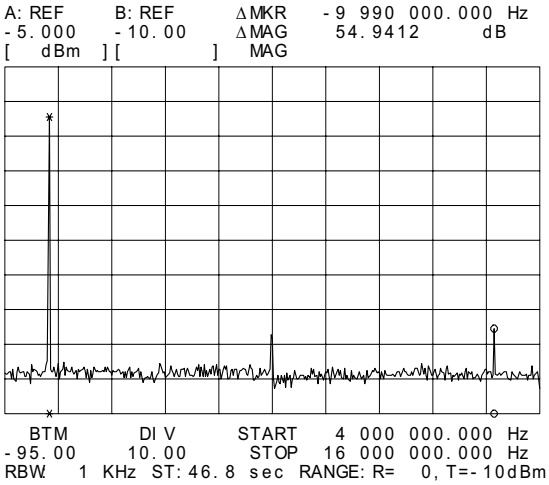

Figure 10.12. Spectrum of 5 MHz output sine wave at the lowpass filter output.

through, intermodulation, and glitch energy. Figure 10.11 illustrates a spectrum plot of a 5 MHz output sine wave at the D/A converter output. The SFDR is 57.6 dBc. Figure 10.12 illustrates a spectrum plot of a 5 MHz output sine wave at the lowpass filter output. The SFDR is 54.9 dBc.

Figure 10.13 shows the photomicrograph of the chip. Distribution of chip area among various blocks is shown in Figure 10.14, while the contribution of each block to the overall power consumption is shown in Figure 10.15. In Figure 10.15, the wideband lowpass filters consume a lot of power compared to the D/A converters. Table 10.3 summarizes the measured performance of the realized IC.

10.6 Summary

The CMOS quadrature IF frequency synthesizer/modulator chip with a signal bandwidth of 80 MHz has been designed and fabricated in a 0.5 μm CMOS. The highly integrated CMOS IF chip eliminates the need to route signals on low impedance lines between chips, thus saving power being wasted in buffers. This quadrature IF frequency synthesizer/modulator is intended for use in a wide variety of indoor/outdoor portable wireless applications in the 2.4-2.4835 GHz ISM frequency band. By programming the quadrature direct digital synthesizer, adaptive channel bandwidths, modulation formats, frequency hopping and data rates are easily achieved.

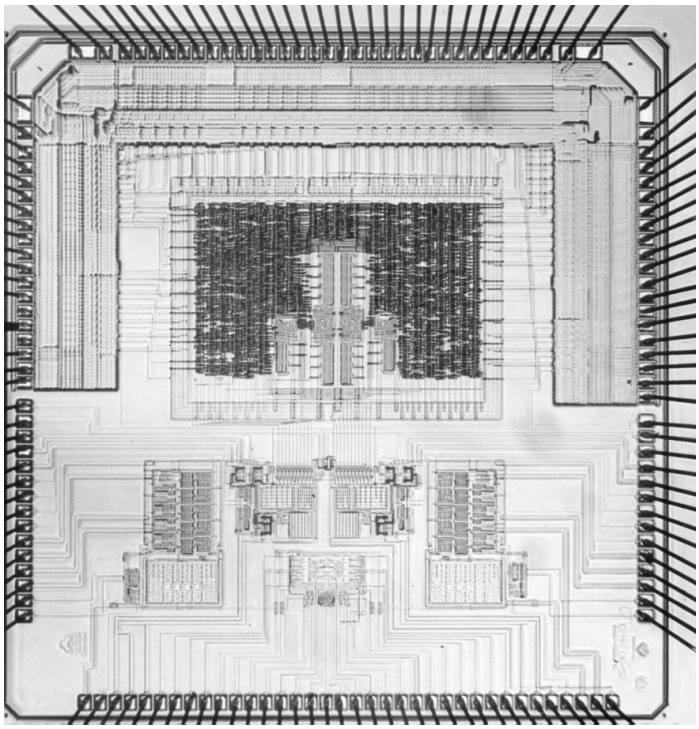

Figure 10.13. Photomicrograph of the chip.

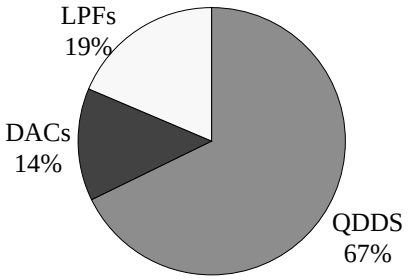

Figure 10.14. Distribution of the chip area among various blocks. The core area of the chip is 9 mm^2.

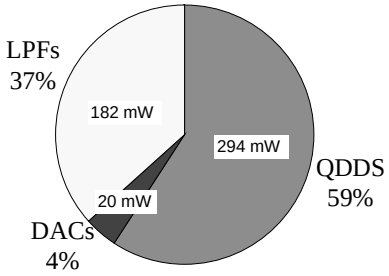

Figure 10.15. Distribution of power dissipation among various blocks. The total power dissipation is 496 mW.

Table 10.3. Measured frequency synthesizer/modulator performance.

Output bandwidth	80 MHz
Frequency resolution	0.0349 Hz (at 150 MHz)
Transistor count	17803
Power dissipation	496 mW at 3.3 V
Die/Core size	24 mm^2/ 9 mm^2

11. Multi-Carrier QAM Modulator

11.1 Introduction

For several years, code-division multiple access (CDMA) systems have gained widespread interest in mobile wireless communications. Wideband code division multiple access (WCDMA) [ETSI98] uses a wider channel compared to a narrowband CDMA channel [TIA93], which improves frequency diversity effects and therefore reduces fading problems. Due to its resistance to multipath fading, and other advantages such as increased capacity, the WCDMA was selected by the European Telecommunications Standards Institute (ETSI) for wideband wireless access to support third-generation services. This technology is optimized to make possible very high-speed multimedia services such as full-motion video, Internet access and videoconferencing.

In this WCDMA system, four QAM modulated carrier frequencies are generated in a base station. In conventional solutions, the four carriers are combined after power amplifiers (PAs) as shown in Figure 11.1. This chapter describes an architecture, where a multi-carrier QAM modulated IF signal is up-converted by two mixers and bandpass filters (BPFs) to RF, as shown in Figure 11.2. This saves a huge number of analog components, many of which require production tuning. Consequently, an expensive and tedious part of the manufacturing is eliminated. A single linear multi-carrier PA replaces the conventional high-level combination of individual

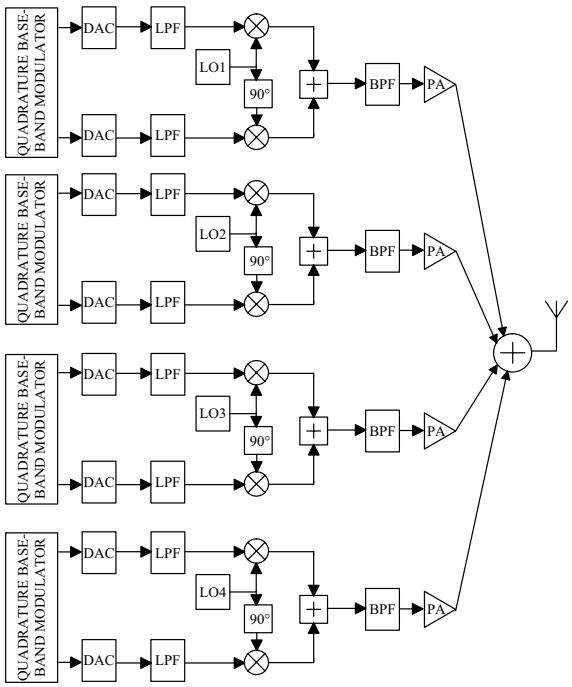

Figure 11.1. Conventional multi-carrier transmitter in base station.

amplifiers using selective cavities. The power losses in a hybrid combiner are avoided. The proposed multi-carrier QAM modulator does not use an analog I/Q modulator, therefore the difficulties of adjusting the dc offset, the phasing and the amplitude levels between the in-phase and quadrature phase signal paths are avoided. The analog I/Q modulator causes a considerable part of the error vector magnitude (EVM) in a practical design [Ota96]. The drawback of the proposed system is high linearity requirements for the wideband up-conversion mixers and the linearized PA, because four carriers are passing through them. However, the linearized PA is also needed in the case of the single carrier, because the modulation method used does not have a constant envelope.

This thesis only concentrates on the parameters of the digital multi-carrier QAM modulator, which generates the IF signal in Figure 11.2. The block diagram of the multi-carrier QAM modulator is shown in Figure 11.3. The analysis of spurs, harmonics and noise from the filters, mixers and the power amplifier is beyond the scope of this thesis.

11.2 Architecture Description

11.2.1 Multi-Carrier QAM Modulator

The QAM modulator includes a pair of root raised cosine filters ($\alpha = 0.22$) and three half-band filters connected to the CORDIC rotator, for directly translating the baseband signal into IF (5 – 25 MHz). The frequencies of the four carriers can be independently adjusted digitally. The four QAM modulated carriers are combined as shown in Figure 11.3. The multi-carrier signal is then filtered by an inverse sinx/x filter to compensate for the sinx/x roll-off function inherent in the sampling process of the digital-to-analog conversion. The analog IF signal is up-converted by two mixers and bandpass filters to RF, as shown in Figure 11.2.

The number of samples per symbol (S) and the clock frequency (f_{clk}) of the multi-carrier QAM modulator are related by

$$f_{clk} = f_{sym} \times S \geq 2.4 \times (f_{IF} + (N \times B)), \tag{11.1}$$

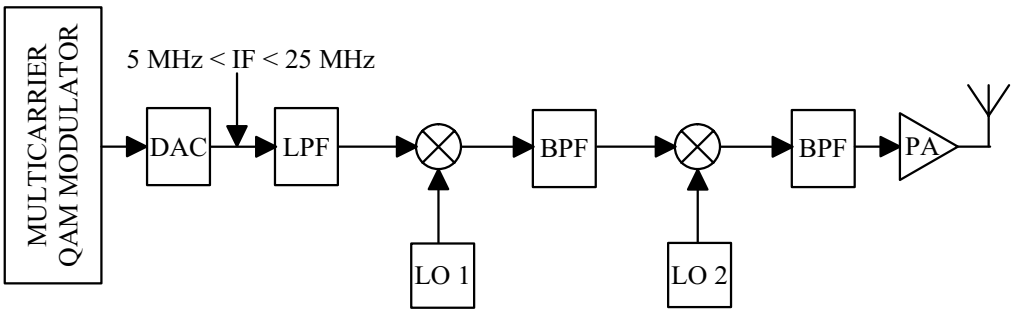

Figure 11.2. Multi-carrier QAM modulator and up-conversion chain.

where the symbol rate (f_{sym}) is 3.84 Mb/s, f_{IF} is 5 MHz, the number of channels (N) is 4 and the carrier spacing (B) is 5 MHz. When S is 16, and f_{sym} is 3.84 Mb/s, f_{clk} is 61.44 MHz. As the multi-carrier QAM modulator generates frequencies close to one half of the clock frequency the first image becomes more difficult to filter. Therefore, the output frequency is limited approximately to 0.41 times the clock frequency. Thus in (11.1) the clock frequency is 2.4 times higher than the maximum output frequency. In Figure 11.2 the first bandpass filter is difficult to implement, if the output frequency range begins near dc. Therefore the digital multi-carrier QAM modulator output range is from 5 MHz (f_{IF}) to 25 MHz, so that the transition band of the first bandpass filter must be below 10 MHz in Figure 11.2.

11.2.2 CORDIC-Based QAM Modulator

The block diagram of the conventional QAM modulator is shown in Figure 2.5. The output of the QAM modulator is

$$s(n) = I(n)\cos(\omega_{QDDS}\ n) + Q(n)\sin(\omega_{QDDS}\ n), \tag{11.2}$$

where ω_{QDDS} is the output frequency of the quadrature direct digital synthesizer (QDDS), and $I(n)$, $Q(n)$ are pulse shaped and interpolated quadrature data symbols [Tan95a].

The QAM modulator performs a circular rotation of $[I(n), Q(n)]^T$. The circular rotation can be implemented efficiently using a CORDIC algorithm, which is an iterative algorithm for computing many elementary functions [Vol59]. In the receiver, the CORDIC-based digital demodulator was presented in [Che95]. However, the problem of this structure is a long latency time, because the CORDIC algorithm is an iterative algorithm. This can cause a stability problem, since the demodulator has a feedback loop for phase tracking. In this QAM modulator the long latency time is not a problem, because there is no feedback loop as shown in Figure 11.4.

In Figure 4.1, a pair of rectangular axes is rotated clockwise through the angle *Ang* by the

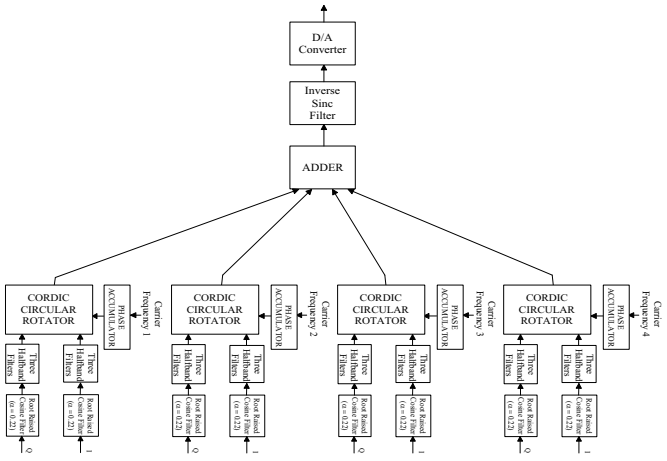

Figure 11.3. Multi-carrier QAM modulator.

CORDIC algorithm; then the coordinates of a vector transform from (I, Q) to (I', Q')

$$\begin{aligned} I' &= I\cos(Ang) + Q\sin(Ang) \\ Q' &= Q\cos(Ang) - I\sin(Ang). \end{aligned} \tag{11.3}$$

The QAM modulator could be implemented by taking the I' term (in-phase) at the CORDIC circular rotator output. These equations can be rearranged so that

$$\begin{aligned} I' &= \cos(Ang)\,[I + Q\tan(Ang)] \\ Q' &= \cos(Ang)\,[Q - I\tan(Ang)]. \end{aligned} \tag{11.4}$$

Arbitrary angles of rotation are obtainable by performing a series of successively smaller elementary rotations. The rotation angles are restricted to $\tan(Ang_i) = \pm 2^{-i}$ so that the multiplication by the tangent term will be reduced to binary shift operations. The iterative rotation can now be expressed as

$$\begin{aligned} I_{i+1} &= K_i\,[I_i + Q_i\,d_i\,2^{-i}] \\ Q_{i+1} &= K_i\,[Q_i - I_i\,d_i\,2^{-i}], \\ K_i &= \cos(\tan^{-1}(2^{-i})), \end{aligned} \tag{11.5}$$

where d_i = -1 if $z_i < 0$, and +1 otherwise. In rotation, the third variable z (phase value) is iterated to zero

$$z_{i+1} = z_i - d_i\,\tan^{-1}(2^{-i}). \tag{11.6}$$

While the inverse tangent of 2^0 is only 45°, the circular rotator must accommodate angles as large as ± 180°. Therefore, the initialization cycle, which performs ±90° rotation, is added:

$$\begin{aligned} I_0 &= d\,Q_{in}, \\ Q_0 &= -d\,I_{in}, \\ z_0 &= z_{in} - d\,2\,\tan^{-1}(2^0), \end{aligned} \tag{11.7}$$

where d = -1 if $z_{in} < 0$, and +1 otherwise.

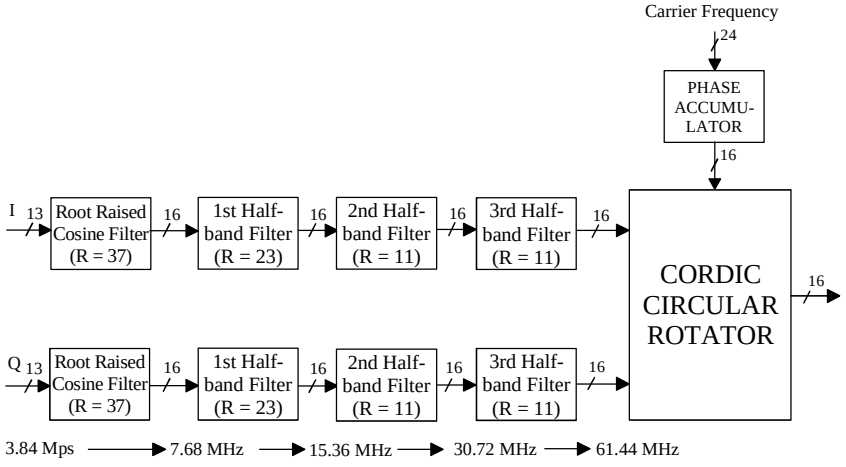

Figure 11.4. Details of the single QAM modulator in the multi-carrier QAM modulator (Figure 11.3). R is number of taps in FIR.

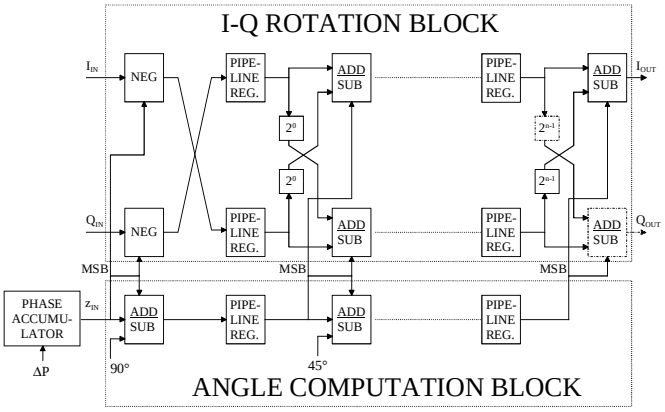

Figure 11.5. Block diagram of CORDIC circular rotator.

Removing the scaling constant (K_i) from the iterative equations yields a shift-add algorithm for the vector rotation. This constant approaches 0.6073 as the number of iterations goes to infinity therefore, the CORDIC rotation algorithm has a gain of approximately 1.647 (4.5). If both the vector component inputs achieve their full scale simultaneously, the maximum magnitude of the resulting vector is 1.414 times the full scale. As the CORDIC rotator has a gain of approximately 1.647, the maximum output is 2.33 times the full-scale input. The CORDIC rotator requires 2 'guard' bits to accommodate the maximum growth without overflowing. In Figure 11.4 the last half-band filter coefficients could be scaled so that only one guard bit is required.

The block diagram of the CORDIC circular rotator is shown in Figure 11.5. To implement the CORDIC rotator, only pipeline registers, adders/subtracters and binary shifters are used. In order to minimize the wiring expense for shift operations between two stages, both data paths for I and Q should be bit-by-bit interleaved with one another. The amount of residual angle becomes smaller in successive iteration stages, therefore the word length in the angle computation block can be reduced approximately by one bit after each iteration [Gie91].

The expected signal-to-noise floor ratio is 83.53 dBc (4.34), when *ba* is 16 bits, 16 is fractional bits in I and Q data paths (*bb*), 13 iteration stages (*n*), *BW* is 0.125 and *Px* is 1. This signal-to-

Table 11.1. Assumed digital multi-carrier modulator specifications in WCDMA base station.	
First adjacent channel power	-65 dBc/3.84 MHz
Second adjacent channel power	-65 dBc/3.84 MHz
Third adjacent channel power	-65 dBc/3.84 MHz
Modulation	Dual Channel QPSK
Carrier spacing	5 MHz
Number of carriers	Four
EVM at digital output	2% rms or less
Frequency error	0.02 ppm × 2 GHz ≈ 40 Hz
Symbol rate for I and Q data	3.84 Mps
Input word length	13 b

noise floor ratio fullfils the adjacent/first alternate channel to the channel power requirements from Table 11.1.

11.2.3 Phase Accumulator

The input word (phase increment word) to the phase accumulator controls the frequency of the generated QAM modulated signal. The phase value is generated by using the modulo 2^j overflowing property of a j-bit phase accumulator. The frequency resolution will be 3.7 Hz by (2.2), when f_{clk} is 61.44 MHz, and j is 24. The frequency resolution is much better than the given frequency error specification in Table 11.1 [ETSI98]. The drift of the LOs can be compensated by the CORDIC rotator, having a frequency resolution of 3.7 Hz. The output of the phase accumulator (z_{IN}) is the address to the CORDIC circular rotator as shown in Figure 11.5.

11.2.4 Inverse Sinx/x Filter

Digital-to-analog converters exhibit a fully sampled-and-hold output that causes amplitude distortions in the spectrum of the converted analog signals [Sam88]. This corresponds to a lowpass filtering function expressed as

$$|H(f)| = |\mathrm{sinc}(\pi\, f\, /\, f_{clk})|, \tag{11.8}$$

where f_{clk} is the clock frequency of the multi-carrier QAM modulator. In the multi-carrier QAM modulator the output band is from 5 MHz to 25 MHz. This introduces a droop of –2.4149 dB,

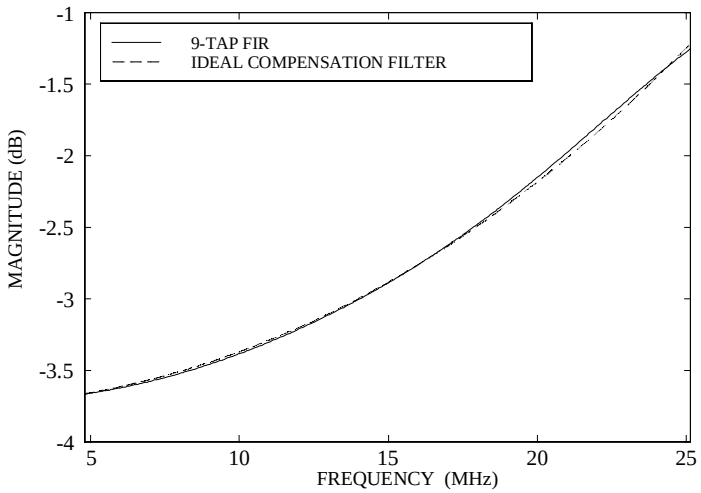

Figure 11.6. Frequency response and impulse response coefficients of a 9-tap FIR compensation filter (--- ideal compensation filter).

which is not acceptable. One method is to compensate the sinx/x roll-off by the pre-equalizer (see Figure 2.5). This requires four complex equalizers in this multi-carrier QAM modulator. Therefore the droop is compensated with the inverse sinx/x filter in the IF frequency. The inverse sinx/x filter is designed so that the frequency bands (0-5 MHz and 25-30.72 MHz) are defined as “don’t care bands”. Attempting to compensate the distortion over the entire Nyquist bandwidth requires significantly longer filters. The inverse sinx/x filter was designed by the method in [Sam88]. The impulse response coefficients and the frequency response of the filter are shown in Figure 11.6. The peak error is ± 0.0327 dB over the frequency band from 5 MHz through 25 MHz in Figure 11.6.

11.3 Filter Architecture and Design

11.3.1 Filter Architecture

In the multi-carrier QAM modulator, phase distortion cannot be tolerated, thus the filters are required to have a linear phase response. It is well known that a FIR filter can be guaranteed to have an exact linear phase response if the coefficients are either symmetric or antisymmetric about the center point. Multirate systems are efficiently implemented using the polyphase structure in which sampling rate conversion and filtering operations are combined. It can be shown that for an interpolation of M, a N-tap filter running at the sampling rate, F_s, is equivalent to M N/M-tap subfilters running at F_s/M. The decomposition into subfilters is accomplished by sampling every Mth coefficient of the original impulse response. When the prototype filter has symmetric or antisymmetric coefficients, however, the decomposition of the filter into M subfilters will usually result in subfilters with unsymmetric coefficients, and, thus, possibly increased complexity as compared to the prototype filter. In fact, at most, two of the subfilters have (anti)symmetric coefficients [Haw96]. In Figure 11.4 the root raised cosine filter (α = 0.22) is an interpolating FIR with a 1:2 interpolation ratio, and so the both subfilters have symmetric coefficients. The subfilters were implemented using the transpose direct form structure in order to use common subexpression sharing [Har96].

Taking advantage of the fact that in the multi-carrier QAM modulator (see Figure 11.3) data streams in the four I and Q paths are processed with the same functional blocks, a further hardware reduction could be achieved by using interleaving techniques [Jia97]. The structure of the interleaved polyphase filter with an interpolation of 2 is presented in Figure 11.7. The interleaver combines K data streams into one stream, which is clocked with a K times higher sampling frequency. The two subfilters E(z) and O(z) in the polyphase decomposition are replaced with $E(z^K)$ and $O(z^K)$. The deinterleaver is used to arrange data samples into the desired order in time. The sampling frequency (clock frequency) is limited by dividing the data to N streams (deinterleaving). The maximum sampling frequency is 61.44 MHz from (11.1). This leads to the filter chain presented in Figure 11.8. The interleaving technique also reduces the level of in-band interference at the output of the on-chip D/A converter generated by the substrate-coupled clock signals, because the amount of hardware using the lower (in-band) frequencies is reduced.

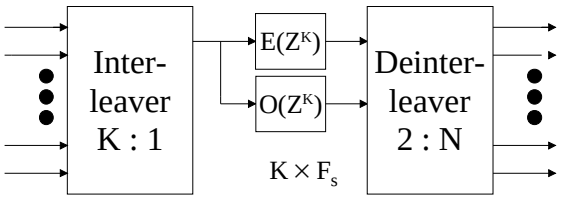

Figure 11.7. Interleaved polyphase filter (interpolation ratio of 2).

Half-band filters are filters whose passband and stopband have symmetry at the ¼ sampling frequency. In three half-band filters all but one of the odd coefficients are zero, thereby reducing the hardware complexity by approximately 50%. This reduction, coupled with their symmetric impulse responses, allows the first, second and third half-band filters to be specified by only 7, 4, 4 non-zero coefficients, respectively. The magnitude response of the three half-band filters and the root raised cosine ($\alpha = 0.22$) filter are shown in Figure 11.9. The combination of the filters provides more than 75 dB image rejection.

11.3.2 Root Raised Cosine Filter Coefficient Design

The root raised cosine filter ($\alpha = 0.22$) was designed to maximize the ratio of the main channel power to the adjacent channels' power under the constraint that the EVM is below 2%. A 2% EVM is assigned to the digital parts (from Table 11.1). The 37-tap root raised cosine filter is characterized by an EVM of 0.56%.

The *N*-tap transmit filter is characterized by the coefficient vector $h = (h_0, h_1, ..., h_{N-1})^T$, which is clocked at the rate *M*/*T* corresponding to an over-sampling ratio *M*. The receive filter (*hr*) is a *K* tap filter, which is *M* times over-sampled from the root raised cosine function. The transmit filter is convolved with the receive filter. Ideally, the result of the convolution will be an ideal raised cosine filter. There will be an EVM due to the truncation of the receive filter impulse response, if the length of the receive filter is short. Therefore, it is better to use a long receive fil-

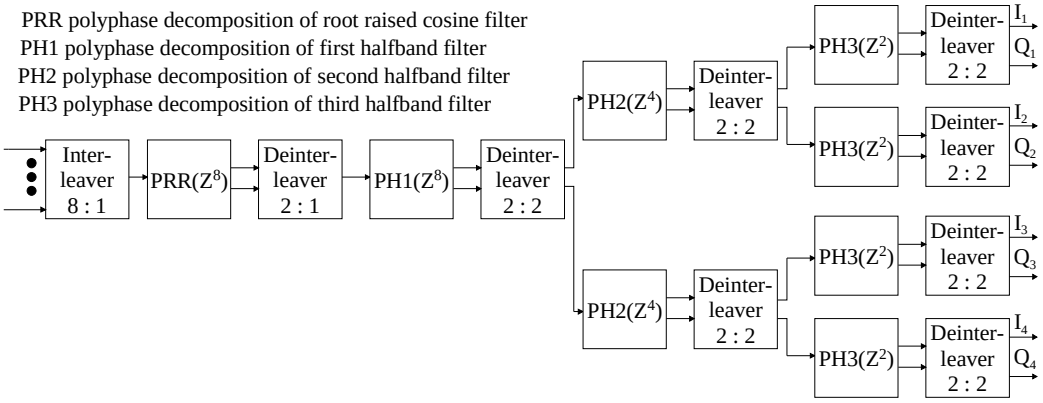

Figure 11.8. Interleaved filter chain.

ter so that the transmit filter will dominate the EVM.

The transmit and receive filter lengths are assumed to be either even or odd, so as to have one middle sample for decision in the composite pulse $RC(n)$. The convolution of the transmitter and receiver filters should satisfy the zero inter-symbol interference constraint:

$$RC(n) = 0, \quad n = n_c \pm lM, \quad l = 1, 2, ..., L, \tag{11.9}$$

where n_c is the center tap and M is the over-sampling ratio. The center tap is (N+K-2)/2. The total number of the terms in (11.9) is 2L, where $L = \lfloor n_c/M \rfloor$, and $\lfloor x \rfloor$ denotes the integer part of x. The equation (11.9) can be written as

$$RC(n_c + Ml) = \sum_{i=0}^{N-1} h_i \, hr_{i+Ml} = h^T \, S_l \, hr, \quad l = \pm 1, \pm 2, ..., \pm L, \tag{11.10}$$

where the elements of the "shift" matrices S_l are zero, except $s_{i,k}(l) = 1$ for i - k = (N-K)/2 + Ml [Che82]. The "shift" matrices S_l are $N \times K$ matrices.

The passband ripples of the linear phase half-band filters (interpolation filters in Figure 11.4) cause EVM as well, which could be partly compensated for by pre-distortion of the pulse shaping filter. The receive filter (hr) could be convolved with the interpolation filters. This convolution could be calculated with the noble identities [Vai93]. The result is decimated back to the M over-sampled ratio and convolved with the transmit filter in (11.10).

One code channel is transmitted, when the EVM is measured. The EVM consists of two components, which are mutually uncorrelated:

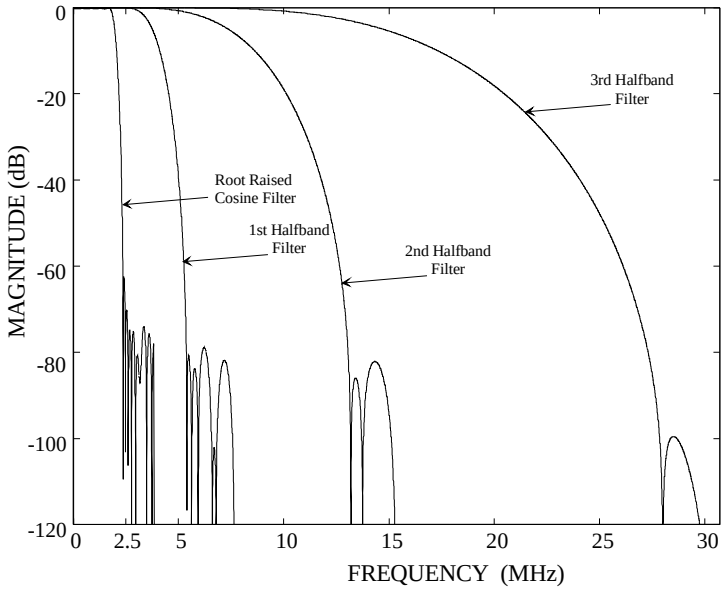

Figure 11.9. Magnitude responses of half-band filters and root raised cosine filter (α = 0.22).

$$\sigma_{EVM}^2 = \sum_{\substack{l=-L \\ l\neq 0}}^{L} (h^T S_l \; hr \;)^2 + \delta_e^2, \tag{11.11}$$

where δ_e^2 is the quantization noise due to finite word length effects. The D/A converter dominates this quantization noise, because it is the most critical component. The effect of the D/A converter word length on the EVM is shown in Figure 11.12. The ISI term is

$$\begin{aligned} \delta_{ISI}^2 &= \sum_{\substack{l=-L \\ l\neq 0}}^{L} (h^T \, S_l \, hr)^2 = h^T \, W \, h, \\ \text{where } W &= \sum_{\substack{l=-L \\ l\neq 0}}^{L} S_l \, hr \, (S_l \, hr)^T, \end{aligned} \tag{11.12}$$

and W is a $N \times N$ matrix. The EVM is scaled with the symbol magnitude in (11.21). Therefore, a linear constraint is added to guarantee proper scaling of the pulse peak

$$RC(n_c) = h^T \, S_0 \, hr = 1. \tag{11.13}$$

The lowpass channel energy (E_c) from dc to f_b (lowpass channel's cut-off frequency) is

$$E_c = \int_{f=-f_b}^{f=f_b} |H(f)|^2 \, df = \sum_{i=0}^{N-1} \sum_{k=0}^{N-1} h_i \, h_k \int_{f=-f_b}^{f=f_b} e^{-j2\pi f(i-k)T/M} \, df = \sum_{i=0}^{N-1} \sum_{k=0}^{N-1} h_i \, h_k \, r_{ik} = h^T \, R \, h, \tag{11.14}$$

where R is a $N \times N$ matrix with elements

$$\mathrm{r_{ik}} = \begin{cases} 2 \, f_b & i = k \\ \dfrac{\sin(2\pi \, f_b \, (i-k)T/M)}{\pi (i-k)T/M} & i \neq k. \end{cases} \tag{11.15}$$

The stopband energy (E_s) from f_s (stopband corner frequency) to M/(2T) is

$$\mathrm{E_s} = 2 \int_{f=f_s}^{f=M/(2T)} |H(f)|^2 \, df = 2 \sum_{i=0}^{N-1} \sum_{k=0}^{N-1} h_i \, h_k \int_{f=f_s}^{f=M/(2T)} e^{-j2\pi f(i-k)T/M} \, df = \sum_{i=0}^{N-1} \sum_{k=0}^{N-1} h_i \, h_k \, v_{ik} = h^T \, V \, h, \tag{11.16}$$

where V is a $N \times N$ matrix with elements

$$v_{ik} = \begin{cases} M/T - 2 \, f_s & i = k \\ \dfrac{\sin(\pi(i-k))}{\pi(i-k)T/M} - \dfrac{\sin(2\pi \, f_s \, (i-k)T/M)}{\pi(i-k)T/M} & i \neq k. \end{cases} \tag{11.17}$$

The ISI can be traded off against the power ratio of the main channel power to the adjacent channels' power. The ISI performance decreases while the power ratio of the main channel power to the adjacent channels' power increases. The cost function, which should be maximized, is written as

$$E = a \times E_c - b \times E_s - c \times \delta_{ISI}^2. \tag{11.18}$$

The objective is to maximize the ratio of the main channel power to the adjacent channels' power under the constraint that the ISI is below 2%. Therefore weighting terms, a, b and c are

added. No well-developed method exists for choosing the weighting terms, *a*, *b* and *c*. Suitable values have to be found by trial and error. Employing the Lagrangian method for the maximization of (11.18) subject to (11.13), the objective function is

$$\begin{aligned}\Phi(h,\lambda) &= a \times h^T\, R\, h - b \times h^T\, V\, h - c \times h^T\, W\, h - \lambda\ (h^T\, S_0\, hr - 1) \\ &= h^T\, D\, h - \lambda\ (h^T\, S_0\, hr - 1),\end{aligned} \tag{11.19}$$

where $D = a \times R - b \times V - c \times W$. The solution is found with the standard Lagrange multiplier techniques (by setting the derivatives with respect to $h(0),...,h(N\text{-}1)$ and λ to zero) to be

$$h = \frac{D^{-1}\, S_0\, hr}{(S_0\, hr)^T\, D^{-T}\, S_0\, hr}. \tag{11.20}$$

Figure 11.10 shows frequency responses of two 37-tap root raised cosine filters designed by different methods:

(i) When sampling from the root raised cosine function

(ii) When maximizing the ratio of the main channel power to the adjacent channels' power under the constraint that the ISI is below 2%. It is seen in this example that this design method provides additional 35 dB adjacent channels' suppression. The ISI performance decreases from 0.11% to 0.56%.

11.3.3 Half-Band Filter Coefficient Design

Half-band filters were first designed with floating-point coefficients using a least-squares FIR design method. A least-squares stopband rather than an equiripple stopband is more desirable,

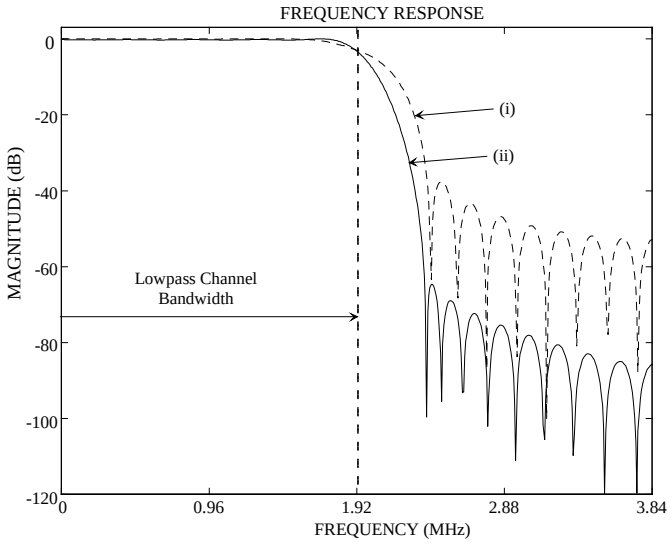

Figure 11.10. Root raised cosine filter using two designs: (I) When sampling from the root raised cosine function (ISI = 0.11%): and (ii) When maximizing the ratio of the main channel power to the adjacent channels' power under the constraint that ISI is below 2% (ISI = 0.56%).

because the objective is to maximize the ratio of the main channel power to the adjacent channels' power. An equiripple stopband minimizes the peak stopband amplitude. However, the total stopband energy is much larger than in a least-squares design.

For applications with fixed coefficients, a fully parallel multiplier is not required and would indeed be a waste of area. Instead, multiplication by a fixed binary number can be accomplished with (N-1) adders, where N is the number of non-zero bits in the coefficient. A more efficient technique is to recode the coefficients from a binary code to a canonic signed digit (CSD) code containing the digits {-1, 0, 1}. Recoded in this way, a limited number of non-zero digits can be used to adequately represent the coefficients. The effect of quantizing the filter coefficients to a limited number of CSD digits is difficult to study analytically, so simulations were used to optimize the selected codes. The CSD coefficients were then determined using a modified version of the optimization program in [Sam89]. The program in [Sam89] was modified to accommodate a least-squares stopband.

11.4 Multi-Carrier QAM Signal Characteristics

The simulation results presented in this section examine the multi-carrier QAM signal characteristics, which are often expressed as a ratio of the peak value to the rms value of a waveform or a crest factor. The simulation length was 8192 symbols, and 16 samples per symbol were taken. The multi-carrier QAM simulation employed a regular carrier spacing of 5 MHz and a symbol rate $1/T_{sym}$ = 3.84 Mbit/s. The pulse shaping filter is a root raised cosine filter with a roll-off factor α of 0.22. The data of both the I and Q inputs are normally distributed, and after clipping the crest factor of the input I/Q data is approximately 10 dB. Different pseudo-random number generators are used to generate each digital modulation source, thus ensuring low correlation between the resulting carriers. The crest factors are given in Table 11.2 for from one to four carriers. The increase in the number of the carriers does not increase significantly the crest factor, as shown in Table 11.2. Theoretical crest factors are significantly higher than the simulated crest factors. These results can be explained by the fact that to reach the theoretical crest factor, not only do all the carriers have to reach the same phase at the same time, but the I/Q data peaks also have to occur at the same time. Since this condition is extremely unlikely to occur in any given period, the simulated crest factor is significantly lower than the theoretical maximum. This is confirmed by the magnitude probability histogram of the QAM modulated carriers shown in Figure 11.11. The histogram clearly indicates that for an increasing number of carriers, the signal magnitude spends an increasing proportion of its time well below the theoretical maximum peak value.

Table 11.2. Crest factors of multi-carrier QAM.

Number of carriers	Crest factor [dB]	Theoretical crest factor [dB]
1	12.55	15.22
2	12.85	18.23
4	12.95	21.24

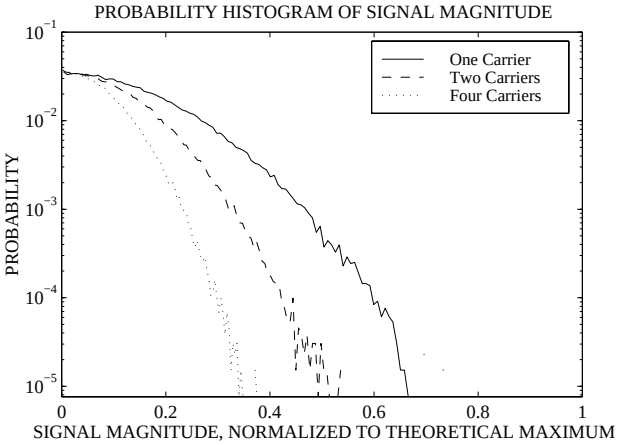

Figure 11.11. Magnitude probability histogram of a multi-carrier-QAM signal.

If the peak values of the signal were to be reduced, then the dynamic range requirements of the D/A converter would be lessened. One method of decreasing the peak values is to use clipping [Ben97]. The distortion generated by the clipping would have to conform to the WCDMA specifications (see Table 11.1). The clipping level of 0.4375 (normalized to the theoretical peak amplitude) is used to reduce peak values of the multi-carrier signal before the D/A converter.

11.5 Simulation Results

Table 11.1 summarizes the assumed digital modulator specifications in the WCDMA base station. The modulation is a dual channel QPSK, where an uplink dedicated physical data channel (DPDCH) and a dedicated physical control channel (DPCCH) are mapped to the I and Q branches, respectively [ETSI98]. In the base station, the multi-user I/Q data is combined and weighted. Therefore, the input of the I/Q branches is 13 bits in Table 11.1.

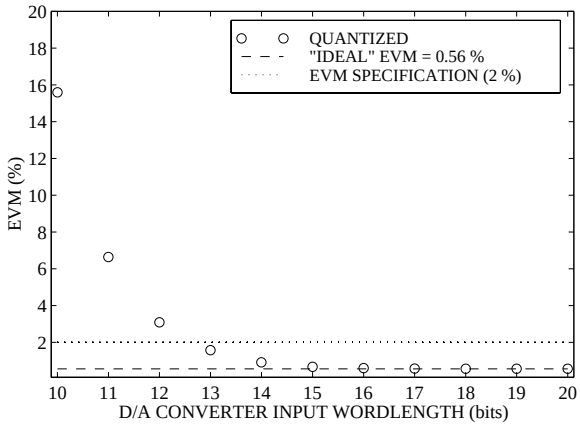

Figure 11.12. EVM vs. the D/A converter input.

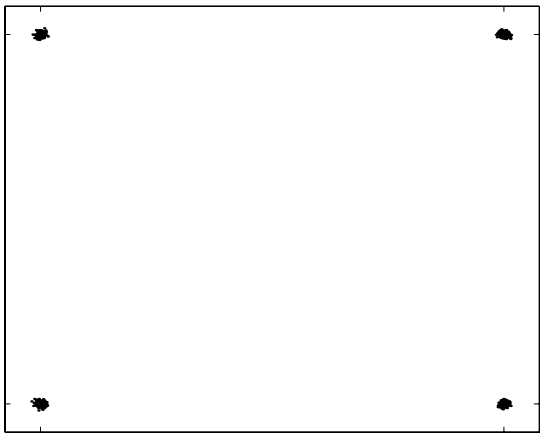

Figure 11.13. Symbol constellation of 4 QAM based on simulation (EVM = 1.06%).

In this WCDMA system, the error vector magnitude (EVM) is specified to be less than 12.5% rms [GPP99]. A 2% rms EVM is assigned to the digital parts. The EVM is the difference between the ideal vector convergence point and the transmitted point in the signal space. The EVM is defined as the rms value of the error vectors in relation to the magnitude at a given symbol,

$$\text{EVM} = \left(\frac{\text{r.m.s. Error Magnitude}}{\text{Symbol Magnitude}} \right) \times 100\%. \tag{11.21}$$

One code channel is transmitted (4 QAM), when the EVM is measured. During the measurement the symbol magnitude is defined to be 40 dB below the maximum symbol level. This means that the symbol is 6-7 bits below the full-scale input. The modulator output was directly connected to the ideal demodulator input. The wideband and high resolution D/A converter is an expensive device, so it is the most critical component in the multi-carrier QAM modulator. In Figure 11.12, the EVM was plotted as a function of the input word length of the D/A con-

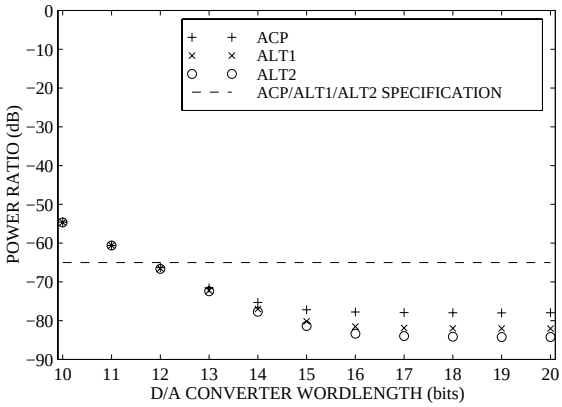

Figure 11.14. Ratio between adjacent channels' power to channel power vs. D/A converter word length.

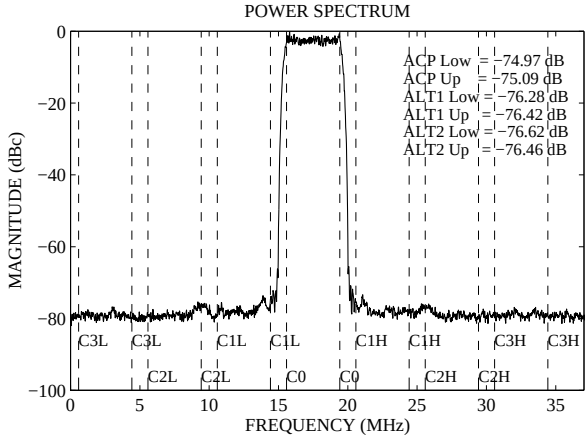

Figure 11.15. Spectrum of single carrier with Table 11.3 parameters.

verter. The EVM of 0.56% is the maximum achievable performance of the finite word length architecture with the given set of CSD filter coefficients. The 4 QAM symbol constellation with Table 11.3 parameters is shown in Figure 11.13 (EVM is 1.06%).

The ratio of the integrated first adjacent/second adjacent/third adjacent channel power (3.84 MHz bandwidth) to the integrated channel power (3.84 MHz bandwidth) should be below -65/-65/-65 dB, respectively, as shown in Table 11.1. This must be confirmed in all channels. During this simulation, the data of both the I and Q inputs were normally distributed, and after clipping the crest factor of the input I/Q data is approximately 10 dB. In Figure 11.14, the ratio between the adjacent channels' power to the channel power was plotted as a function of the word length of the D/A converter. The ACP/ALT1/ALT2 means the power ratio between the first adjacent/second adjacent/third adjacent channel to the channel, respectively. The 14-bit D/A converter fulfills clearly the EVM (see Figure 11.12) and the adjacent channels' power specifications (from Table 11.1). The simulated spectrum for the single carrier is shown in Figure 11.15. Figure 11.16 shows the multi-carrier QAM modulator output.

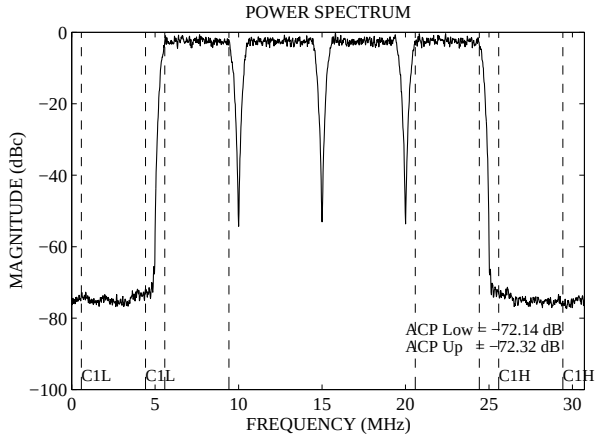

Figure 11.16. Spectrum of four carriers with Table 11.3 parameters.

Table 11.3. Digital multi-carrier QAM modulator parameters.	
Word lengths	See Figure 11.4.
Internal word lengths in interpolation filters and INV Sinx/x filter	17, 17, 17, 17 and 17 b
Clock frequency	61.44 MHz
Frequency resolution	3.7 Hz
D/A converter word length	14 b

11.6 Implementation

This multi-carrier QAM modulator was synthesized by Synopsys software from the VHDL description using the 0.35 µm CMOS standard cell library. Static timing check and prelayout timing simulations were performed for the netlist, and the chip layout was completed using Cadence place and route tools. Last, based on the parasitic information extracted from the layout, the post-layout delays were back-annotated to gate-level simulations to ensure satisfactory chip timing. The photomicrograph is shown in Figure 11.17. The features of the designed circuit are summarized in Table 11.4.

11.7 D/A Converter

For high-speed and high-resolution applications (>10 bits, >50 MHz), the current source switching architecture is preferred since it can drive a resistive load directly, without the need for a voltage buffer. The segmented architecture is most frequently used to combine a high conversion rate with high resolution. In [Lin98], it is stated that a complete unitary implementation would lead to the best dynamic performance in terms of total harmonic distortion. The number

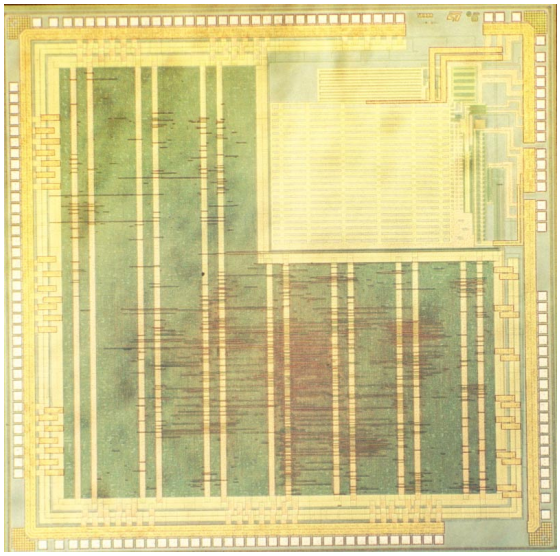

Figure 11.17. Photomicrograph of multi-carrier QAM modulator.

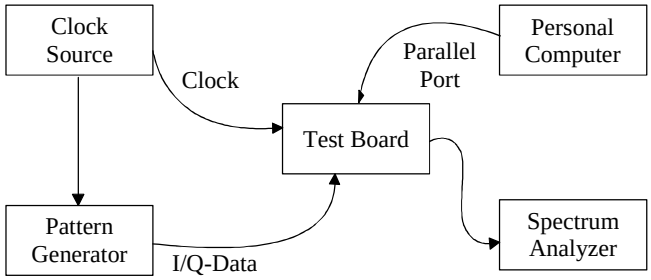

Figure 11.18. Block diagram of test system.

of unitary implemented bits is limited by the increased coding complexity ($\alpha\ 2^N$) and area constraints. The area constraints (routing of switch/latch and current source array) resulted in a 6-8 segmented architecture as a good trade-off. The 6 MSBs are decoded from the binary to a thermometer code in the thermometer decoder, which steers the unitary weighted current source array. The D/A-converter relies on the intrinsic process matching and layout techniques [Bas91] to get 14 bits static linearity at the expense of some additional area.

One stage of registers was inserted before the current switches to ensure simultaneous switching of all bits. A high spectral purity is achieved by properly adjusting the cross point of the control voltages, and by limiting their amplitude at the gates of the current switches (see Figure 10.5). To ensure equal operation speed of the different switches, the current densities in the switch transistors have to be the same, which is obtained by scaling the width of the transistors. Disturbances connected to the external bias current are filtered out on the chip with a simple one pole low-pass filter. The cascode structure is used to increase the output impedance of the unit current source, which improves the linearity of the D/A-converter. To eliminate process related gradients in the D/A converter current source transistor arrays, the unit current sources are distributed in common centroid arrays surrounded by dummy transistors [Bas91].

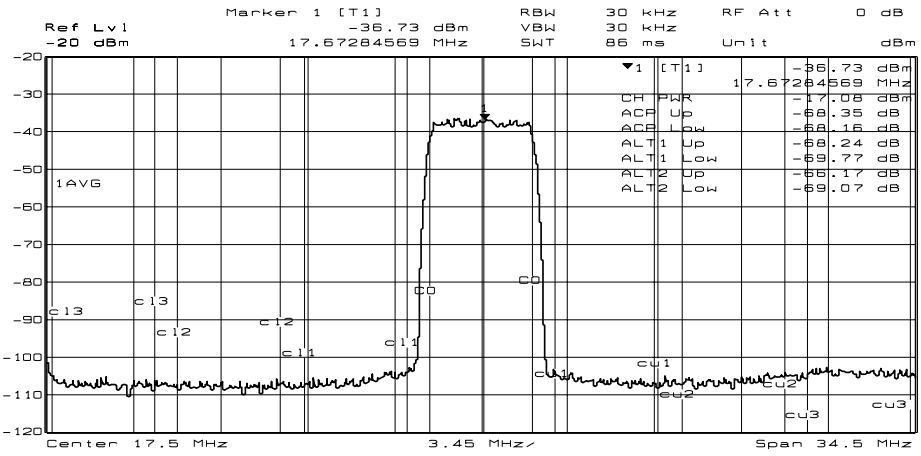

Figure 11.19. QAM-modulated signal at the off-chip D/A converter output. Resolution and video bandwidth is 30 kHz, sweep time is 86 ms and averaging is used.

11.8 Layout

The multi-carrier QAM modulator is a mixed-signal high-precision monolithic device, which requires a significant design effort at the physical level. The D/A-converter is implemented with a differential design, which results in reduced even-order harmonics, and provides a common-mode rejection of disturbances. To minimize the coupling of the switching noise from the digital logic to the analog output, the power supplies of the digital logic and the analog part are routed separately. On-chip decoupling capacitors (total capacitance of 1 nF) are used to reduce the ground bounce in the digital part. To reduce the supply ripples even further, additional supply and ground pins are used to reduce the overall inductance of packaging. In the triple well BiCMOS it is possible to place analog and digital parts in the isolated wells, which is a very effective way of eliminating substrate coupling. The interferences at the on-chip D/A converter output band are reduced, avoiding hardware using in-band clock frequencies (see Section 11.3.1).

11.9 Measurement Results

To evaluate the multi-carrier QAM modulator, a test board was built and a computer program was developed to control the measurement. Figure 11.18 illustrates the block diagram of the multi-carrier QAM modulator test system. Firstly, an off-chip D/A converter [Ana99a] was used. The ratio of the integrated first adjacent/second adjacent/third adjacent channel power (3.84 MHz bandwidth) to the integrated channel power (3.84 MHz bandwidth) should be below -65/-65/-65 dB, respectively. The carrier spacing is 5 MHz (see Table 11.1). Figure 11.19 shows the single carrier output spectrum centered at 17.5 MHz. The power ratios fulfill the specifications (-65/-65/-65 dB) in the case of the single carrier. The specifications are -45/-55/-55 dB, when the spectrum is measured at the base station RF port [GPP99]. The measurement results are well below these specifications. Figure 11.20 shows the multi-carrier signal at the

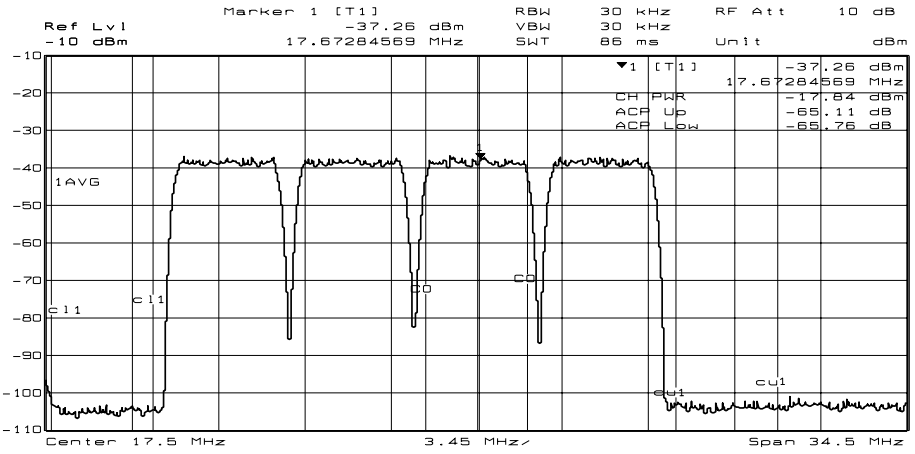

Figure 11.20. Multi-carrier QAM-modulated signal at the off-chip D/A converter output. Resolution and video bandwidth is 30 kHz, sweep time is 86 ms and averaging is used.

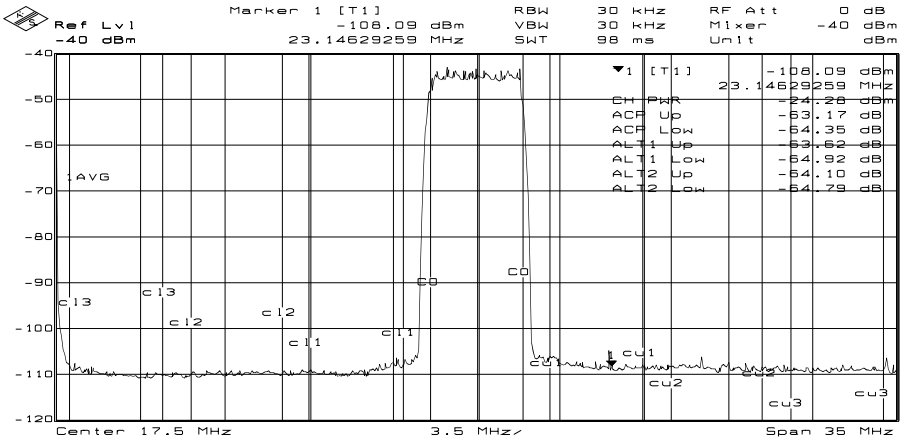

Figure 11.21. QAM-modulated signal at the on-chip D/A converter output. Resolution and video bandwidth is 30 kHz, sweep time is 98 ms and averaging is used.

off-chip D/A converter output. The first adjacent channel power fulfills the specification (-65 dB). It is possible to use steep analog bandpass filters around the multi-carrier signal in Figure 11.2, and the second adjacent/third adjacent channel powers around the multi-carrier signal can be further reduced.

Next, the on-chip D/A converter was used in the measurement. Figure 11.21 shows the single carrier output spectrum centered at 17.5 MHz. The power ratios don't fulfill the specifications (-65/-65/-65 dB) in the case of the single carrier. The specifications are -45/-55/-55 dB, when the spectrum is measured at the base station RF port [GPP99]. The measurement results fulfill these specifications. Figure 11.22 shows the multi-carrier signal at the on-chip D/A converter output. The first adjacent channel power fulfills the specification (-45 dB) at the base station RF port.

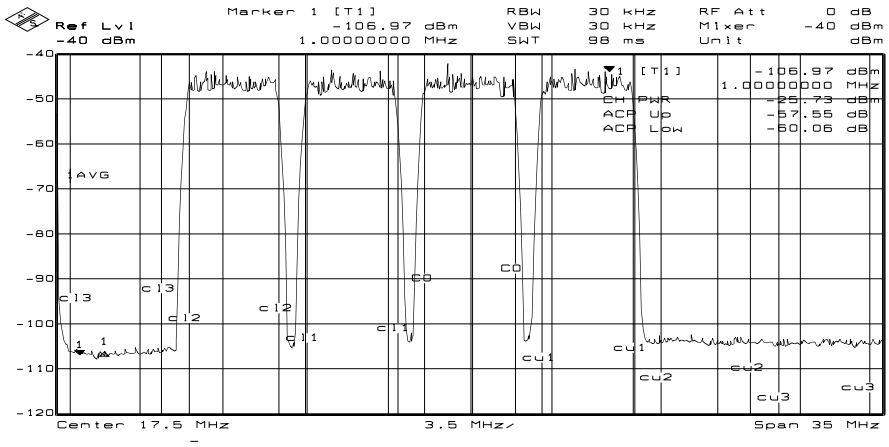

Figure 11.22. Multi-carrier QAM-modulated signal at the on-chip D/A converter output. Resolution and video bandwidth is 30 kHz, sweep time is 98 ms and averaging is used.

Table 11.4. Features of designed multi-carrier QAM modulator.

IC technology	0.35 μm CMOS (in BiCMOS)
Operating clock frequency	61.44 MHz @ 3 V
Power dissipation	1.47 W at 61.44 MHz @ 3 V
Die/Core size	25.76 mm^2/20.1 mm^2

11.10 Summary

The multi-carrier QAM modulator chip contains four CORDIC based QAM modulators. The proposed multi-carrier QAM modulator does not use an analog I/Q modulator therefore the difficulties of adjusting the dc offset, the phasing and the amplitude levels between the in-phase and quadrature phase signal paths are avoided. The multi-carrier QAM modulator was designed to fulfill the spectrum and EVM specifications of the WCDMA system.

12. Single Carrier QAM Modulator

12.1 Conventional QAM Modulator

The block diagram of the conventional QAM modulator is shown in Figure 2.4. The output of the QAM modulator is

$$\begin{aligned} I_{out}(n) &= I(n)\cos(\omega_{QDDS}\, n) + Q(n)\sin(\omega_{QDDS}\, n) \\ Q_{out}(n) &= Q(n)\cos(\omega_{QDDS}\, n) - I(n)\sin(\omega_{QDDS}\, n), \end{aligned} \tag{12.1}$$

where ω_{QDDS} is the output frequency of the quadrature direct digital synthesizer (QDDS), and $I(n)$, $Q(n)$ are pulse shaped and interpolated quadrature data symbols [Tan95a]. In the base station, the multi-user I/Q data is combined and weighted and so the input of the I/Q branches is 12 bits in Table 12.1. The specifications are not so strict in Table 12.1 as in Table 11.1 because it is possible to use steep analog bandpass filters around the single carrier signal in Figure 11.2, and the adjacent channels' power around the single carrier signal can be further reduced.

12.2 CORDIC Based QAM Modulator

The block diagram of the CORDIC circular rotator is shown in Figure 11.5. To implement the CORDIC rotator, only pipeline registers, adder/subtractors and binary shifters are used, which are easy to implement in hardware. In the case of most PLD architectures there are already registers present in each logic cell, so the addition of the pipeline registers incurs no extra hardware cost. The CORDIC rotator would require 2 'guard' bits to accommodate the maximum growth without overflowing (see Section 11.2.2). In Figure 12.1 the last half-band filter coefficients could be scaled so that only one guard bit is required.

The expected signal-to-noise floor ratio is 73.94 dBc (4.34) when *ba* is 16 bits; the number fractional bits in the I and Q data paths (*bb*) is 16; there are 11 iteration stages (*n*); *BW* is 0.125, and *Px* is 1. This signal-to-noise floor ratio fulfills the adjacent/first alternate channel to the

Table 12.1. Assumed digital modulator specifications (in case of single carrier) in WCDMA base station.

Adjacent channel power	-55 dBc/3.84 MHz
Next neighboring channel power	-60 dBc/3.84 MHz
Modulation	Dual Channel QPSK
Carrier spacing	5 MHz
EVM at digital output	5% rms or less
Frequency error	0.02 ppm × 2 GHz ≈ 40 Hz
Symbol rate for I and Q data	3.84 Mps
Input word length	12 b

channel power requirements from Table 12.1.

12.3 Phase Accumulator

The input word (phase increment word) in the phase accumulator controls the frequency of the generated QAM modulated signal. The phase value is generated by using the modulo 2^j overflowing property of a j-bit phase accumulator. The frequency resolution will be 3.7 Hz by (2.2), when f_{clk} is 61.44 MHz, and j is 24. The frequency resolution is much better than the given frequency error specification in Table 12.1 [ETSI98]. The output of the phase accumulator (z_{IN}) is the address in the CORDIC circular rotator as shown in Figure 11.5.

12.4 Filter Architectures and Design

12.4.1 Filter Architectures

In the QAM modulator, phase distortion cannot be tolerated and thus the filters are required to have a linear phase. A FIR filter can be guaranteed to have an exact linear phase response if the coefficients are either symmetric or antisymmetric about the center point. All the FIR filters in the interpolation chain are implemented using a polyphase structure. The magnitude response of the three half-band filters and the root raised cosine ($\alpha = 0.22$) filter are shown in Figure 12.2. The combination of the filters provides more than 60 dB image rejection. Taking advantage of the fact that in the QAM modulator data streams in the I and Q paths are processed with the same functional blocks, a further hardware reduction can be achieved by interleaving techniques (see Figure 12.3). In Figure 12.3 the filters are modified to handle two channels by doubling the delay between taps and the sampling rate.

12.4.2 Filter Coefficient Design

The root raised cosine filter ($\alpha = 0.22$) was designed to maximize the ratio of the main channel power to the adjacent channels' power under the constraint that the EVM is below 5 % (see Section 11.3.2). Half-band filters were first designed with floating-point coefficients using a

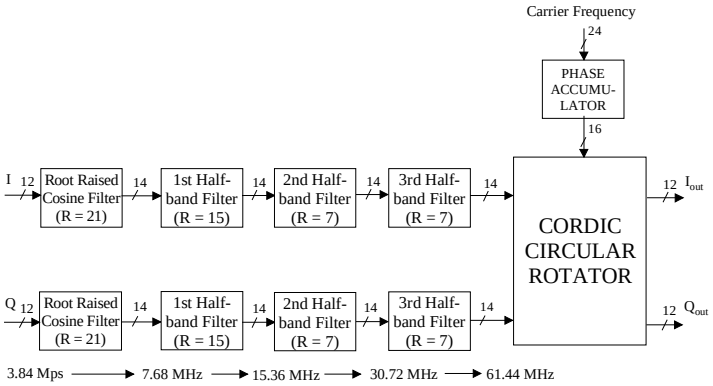

Figure 12.1. CORDIC based QAM modulator.

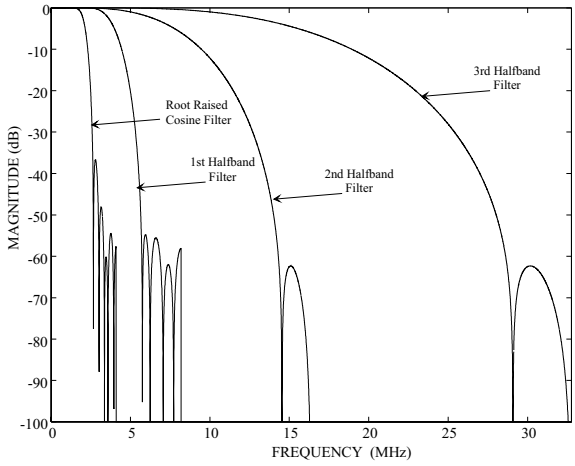

Figure 12.2. Magnitude Responses of half-band filters and root raised cosine filter (α = 0.22).

least-squares FIR design method because the objective is to maximize the ratio of the main channel power to the adjacent channels' power.

For applications with fixed coefficients a fully parallel multiplier is not required. The multiplication process is greatly simplified by replacing filter coefficients with CSD numbers. The CSD coefficients were determined using a version of the optimization program in [Sam89] which was modified to accommodate a least squares stopband.

12.5 D/A-Converter

The 10-bit D/A converter in Section 10.4.3 is extended to 12-bits. In the two-stage weighted current array, only 63 MSB and 63 LSB equivalent unit current sources are required for a 12-bit D/A-converter in Figure 12.4. The proper weighting between the two current arrays is realized with the bias current ratio of 64:1. The stray capacitance associated with the weighted current sources is rather small due to the reduced number of parallel unit current sources. This makes

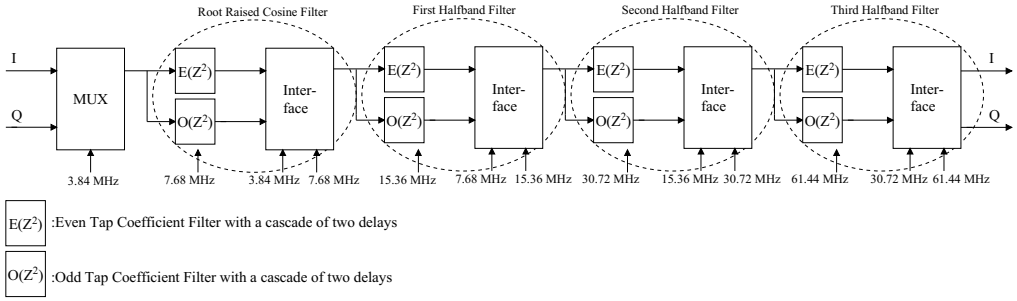

Figure 12.3. Hardware reduction scheme using polyphase and interleaving techniques for root raised cosine filter and three halfband filters.

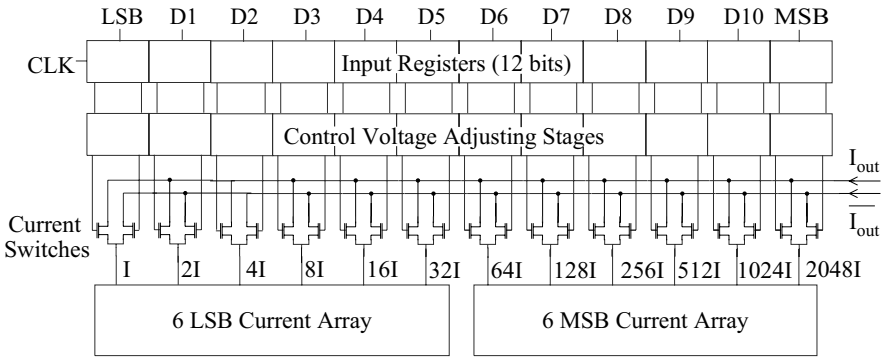

Figure 12.4. 12-bit two-stage current array D/A-converter.

the settling of the output fast. In the case of a 12-bit D/A-converter an error in the bias current ratio must be below 0.8 %, then an error in linearity is less than ± ½ LSB [Wal97]. One stage of registers has been inserted before the current switches in order to ensure simultaneous switching of all bits. A high spectral purity is achieved by properly adjusting the cross point of the control voltages, and by limiting their amplitude at the gates of the current switches (see Figure 10.5). To ensure an equal operational speed of the different switches the current densities in the switch transistors have to be the same, which is obtained by scaling the width of the transistors. The scaling is done only for the switches corresponding to the 4 MSBs to avoid unpractical large transistor sizes. Disturbances connected to the external bias current are filtered out on-chip with a simple one pole low-pass filter. The cascode structure is used to increase the output impedance of the unit current source, which improves the linearity of the D/A-converter. The D/A-converter is implemented with a differential design, which results in reduced even-order distortions and provides a common-mode rejection to disturbances. Figure 12.5 shows the photomicrograph of the chip. The die/core area is 1.64 mm^2/0.29 mm^2 (0.5 µm CMOS technology).

12.6 Implementation with the PLDs

The CORDIC based QAM modulator is an array of interconnected adder/subtractors. Therefore,

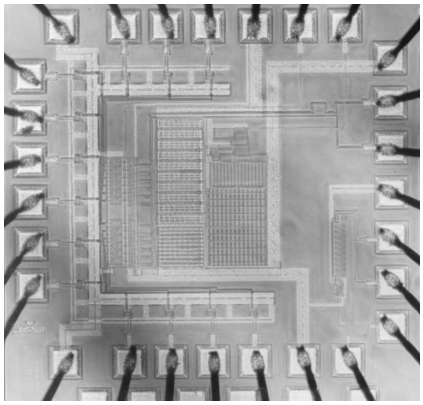

Figure 12.5. Photomicrograph of D/A converter.

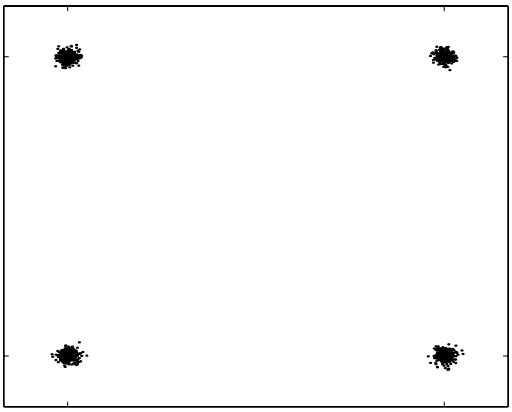

Figure 12.6. Symbol constellation of 4 QAM based on simulation (EVM = 2.88 %).

it can be realized with basic logic structures in the existing PLDs, i.e. the logic structures that correspond to the configurable logic blocks (CLBs) for the Xilinx XC4000 family [Xil98], and the logic elements (LEs) for the Altera's FLEK devices [Alt98] in particular. The CORDIC-based QAM modulator was implemented with the Altera FLEK 10KA-1 series devices [Alt98]. The pair of root raised cosine and three half-band filters in Figure 12.1 (a design using poly-phase and interleaving techniques as shown in Figure 12.3 [Cho99]) requires 2144 (42% of the total) LEs in the EPF10K100A device. The CORDIC rotator and the phase accumulator require 1159 (23% of the total) LEs in the EPF10K100A device. The maximum operating frequency of the CORDIC-based multi-carrier QAM modulator is 79.36 MHz, which is higher than the operating frequency (61.44 MHz). The QAM modulator can be implemented with two EPF10K100A devices.

Two 14 x 14 bits multipliers and the adder in the conventional QAM modulator (see Figure 2.4) require 1068 LEs in the EPF10K100A device. The operating frequency of the two multipliers and the adder is 61.44 MHz. These multipliers were implemented with the parameterized mod-

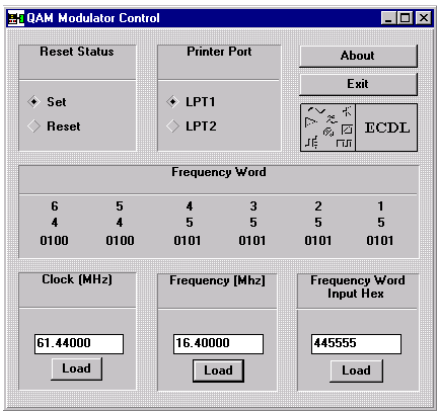

Figure 12.7. User interface.

ule [Alt96], which is optimized for performance and density in the PLDs. The CORDIC rotator requires 1094 LEs in the EPF10K100A device. The CORDIC based QAM modulator has similar complexity of logic as the two multipliers and the adder (1068 LEs) with the same word sizes. The conventional QAM modulator with the quadrature outputs requires four multipliers, two adders and sine/cosine memories (see Figure 2.4). It replaces sine/cosine ROMs ($2 \times 2^{16} \times$ 14 b), four multipliers and two adders.

12.7 Simulation Results

A 5 % rms EVM is assigned to the digital parts as shown in Table 12.1. The EVM is defined as the difference between the ideal vector convergence point and the transmitted point in the signal space. The EVM is defined as the rms value of the error vectors in relation to the magnitude at a given symbol in percent. One channel is transmitted (4 QAM) while the EVM is measured. During the measurement the symbol magnitude has to be set 40 dB below the maximum symbol level. This means that the symbol is 6-7 bits below the full-scale input. An ideal demodulator was used to demodulate the QAM modulator output signal to the baseband. The 4 QAM symbol constellation is shown in Figure 12.6 (EVM is 2.88%).

12.8 Measurement Results

To evaluate the QAM modulator a test board was built and a computer program was developed to control the measurement. The phase increment word and the other control signals are loaded into the test board via the parallel port of a personal computer. The operating software runs under Microsoft® Windows (see Figure 12.7). Figure 12.8 illustrates the block diagram of the QAM modulator test system.

The ratio of the integrated adjacent/first alternate channel power (3.84 MHz bandwidth) to the integrated channel power (3.84 MHz bandwidth) should be below -55/-60 dB respectively. The carrier spacing is 5 MHz (see Table 12.1). During the measurement, the input I/Q data is normally distributed, and after clipping the crest factor of the input I/Q data is approximately 10 dB. Figure 12.9 shows the QAM modulator output spectrum centered at 16.4 MHz. The droop in the signal spectrum is caused by the sinc-effect (see Appendix A) and a differential to single

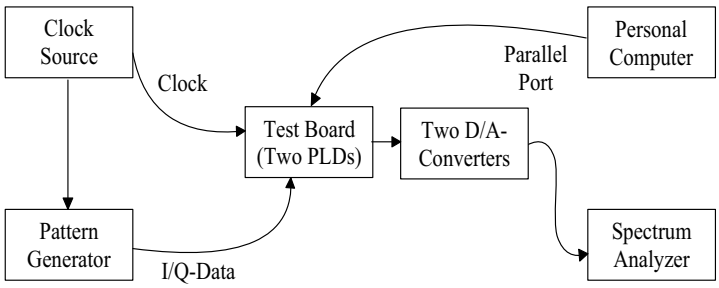

Figure 12.8. Block diagram of test system.

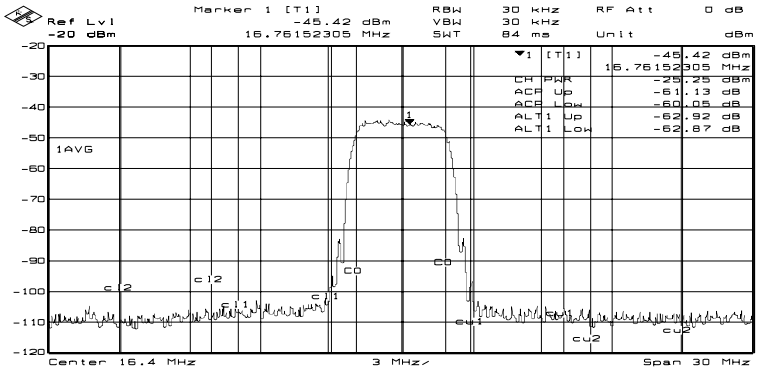

Figure 12.9. QAM modulator output centered at 16.4 MHz.

end transformer (balun). The ACP/ALT1 means the power ratio between the adjacent/first alternate channel to the channel, respectively. The power ratios fulfill the specifications (-55/-60 dB) in this figure. The specifications are -45/-55 dB, when the spectrum is measured at the base station RF port [GPP99]. The measurement results are well below these specifications.

12.9 Summary

The CORDIC based QAM modulator was developed and implemented. The digital QAM modulator and the D/A converters were designed to fulfill the spectrum and EVM specifications of the WCDMA system.

13. Multi-Carrier GMSK Modulator

13.1 Introduction

In conventional base station solutions, the transmitted carriers are combined after the power amplifier (PA), as shown in Figure 11.1. This chapter describes an architecture where a multi-carrier GMSK modulated IF signal is up converted to RF by two mixers and bandpass filters (BPFs) as shown in Figure 13.1. This saves a huge number of analog components, many of which require production tuning. Consequently, an expensive and tedious part of the manufacturing will be eliminated. The proposed multi-carrier GMSK modulator does not use an analog I/Q modulator, therefore the difficulties of adjusting the dc offset, the phasing and the amplitude levels between the in-phase and quadrature phase signal paths are avoided. A single linearized multi-carrier power amplifier replaces a bank of individual amplifiers whose high-power outputs are conventionally combined by using selective cavities. Hence, power losses inherent to cavity-filter combiners are avoided which results in space and cost savings as well as greater reliability. The GMSK modulation method used in the GSM 900 and the DCS 1800 is a constant envelope modulation scheme. As a number of these GMSK carriers are combined to produce a multi-carrier signal, the beneficial properties are lost. Because of the strongly varying envelope of the composite signal, very stringent linearity requirements are imposed on the wideband D/A converter, up conversion mixers and the PA.

13.2 Interface

The base station back-ends produce downlink (DL) bursts, which contain all required RF control information in addition to the actual data bits. The DL bursts are sent once per time slot. The interface FPGA in Figure 13.2 extracts data bits and the frequency control words from the four DL bursts obtained from the base station back-end. The FPGA also separates the power level indication from the downlink burst to be used in the dynamic power control. Additionally, there are certain initialization and control data, which must be separated from the downlink bursts, and this is also to be done in FPGA. The FPGA feeds necessary data and control bits to the multi-carrier GMSK modulator with fixed timing. The interface block was implemented with the Xilinx XC4000 family series device [Xil98].

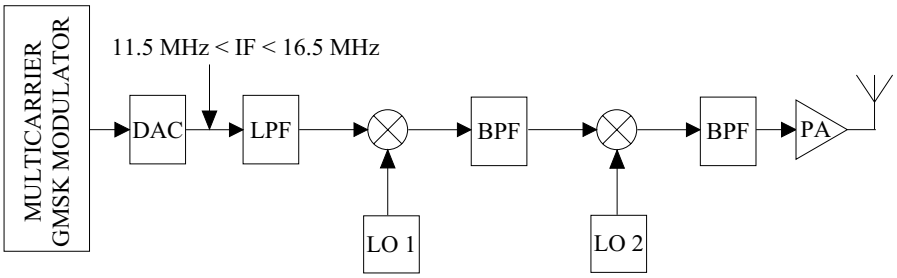

Figure 13.1. Multi-carrier GMSK modulator and up conversion chain.

13.3 GMSK Modulator

The block diagram of the GMSK-modulator is shown in Figure 13.3. The system consists of a shift register, counter, frequency trajectory look-up-table (LUT), adder/subtracter, phase accumulator, carrier frequency register, phase to amplitude converter (conventionally a sine ROM) and a D/A-converter. The use of the LUT as a digital filter has been described in [Bou77]. Incoming data symbols to the Gaussian low-pass filter [GSM92] are stored in the shift register (see Figure 13.3). The input data to the Gaussian low-pass filter are a series of rectangular pulses

$$c(t) = \sum_{n=-\infty}^{\infty} a_n \, \Omega(\frac{t - nT_{sym}}{T_{sym}}), \tag{13.1}$$

where a_n is the input symbol, and $\Omega(t/T_{sym})$ is a unit rectangular pulse of duration T_{sym} and centered at the origin [Mur81]. The pre-modulation Gaussian filter is defined as

$$h(t) = \sqrt{\frac{2\pi}{\ln(2)}} \, B \exp\left(-\frac{2\pi^2 (Bt)^2}{\ln(2)} \right), \tag{13.2}$$

where B is the 3 dB bandwidth, and $BT_{sym} = 0.3$.

The filter response to a unit rectangular pulse centered at the origin is

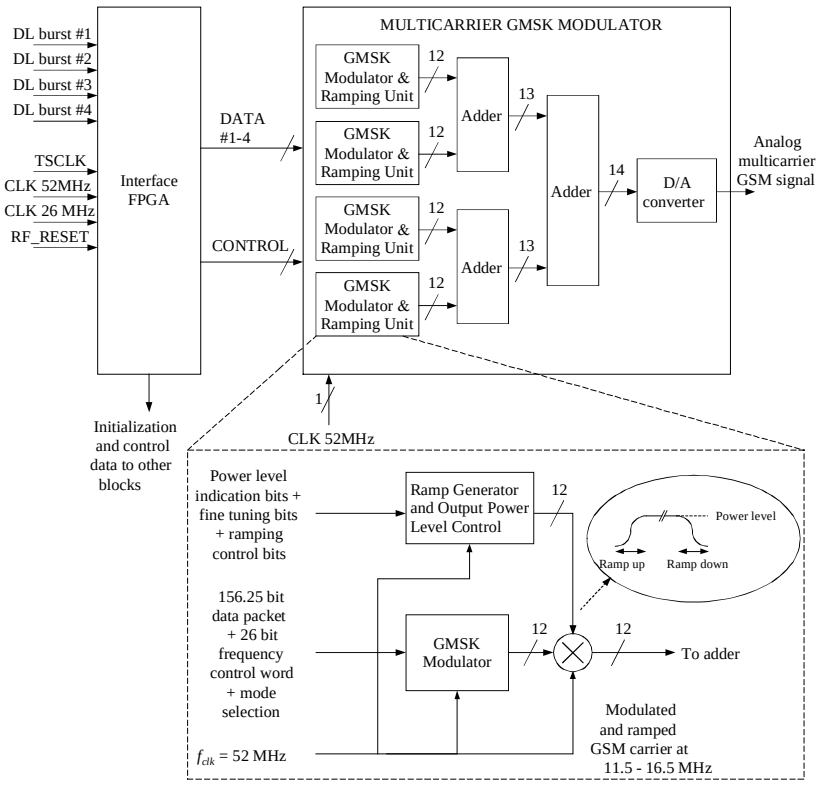

Figure 13.2. Multi-carrier GMSK modulator.

$$g(t) = \Omega(\frac{t}{T_{sym}}) * h(t), \tag{13.3}$$

where an asterisk denotes the following convolution:

$$g(t) = \sqrt{\frac{2\pi}{\ln(2)}}\, B \int_{t-T_{sym}/2}^{t+T_{sym}/2} \exp\left(-\frac{2\pi^2 (B\,x)^2}{\ln(2)}\right) dx, \tag{13.4}$$

$$= 0.5\left[\operatorname{erf}\left(-\sqrt{\frac{2}{\ln(2)}}\,\pi\, B\left(t-\frac{T_{sym}}{2}\right)\right) + \operatorname{erf}\left(\sqrt{\frac{2}{\ln(2)}}\,\pi\, B\left(t+\frac{T_{sym}}{2}\right)\right)\right], t > 0, \tag{13.5}$$

$$g(t) = g(-t),$$

where

$$\operatorname{erf}(y) = \frac{2}{\sqrt{\pi}} \int_0^y \exp(-u^2)\, du, \tag{13.6}$$

$$\operatorname{erf}(y) = -\operatorname{erf}(-y). \tag{13.7}$$

The input signal to the FM modulator is

$$b(t) = \sum_{n=-\infty}^{\infty} a_n\, g(t - nT_{sym}). \tag{13.8}$$

Equation (13.8) shows that the pulse response extends theoretically from -∞ to +∞, so the response to a pulse train inside a given symbol interval has interference from all past and future symbols. The LUT generates a frequency path with inter-symbol interference over $(w\text{-}1)T_{sym}$ [Bou77], where T_{sym} is the symbol duration, and w is the number of the symbol stages in the shift register in Figure 13.3. To reduce the LUT size, the extent of the pulse response is usually considered limited to only the nearest neighbors [Lin96]. The simulation shows that in order to meet modulation spectrum requirements, the impulse response of the Gaussian filter can be

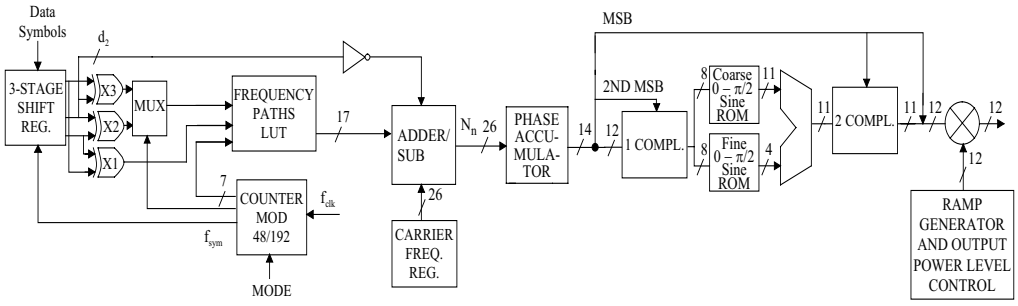

Figure 13.3. Details of the single GMSK modulator in the multi-carrier GMSK modulator (Figure 13.2).

truncated to a 2-bit width (three stages in the shift register) (see Table 13.4). Therefore, we limit the pulse response to only the two nearest neighbors in Figure 13.4. As the pulses can have one of two possible values (0 or 1), we can have $2^3 = 8$ possible curves. Since the frequency of the modulated signal has to be proportional to g(t) [see (13.8)], the curves are called "frequency trajectories". The trajectories can be obtained from (13.8), substituting particular values for the a_n. The frequency trajectories for $BT_{sym} = 0.3$, where B is the 3 dB bandwidth, are shown in Figure 13.4. Other frequency trajectories can be obtained from [000, 001, 101, 100] by sign changes. The frequency trajectory LUT takes advantage of this symmetry in Figure 13.3. Therefore, the two XORs (X1 and X2) are used to decode the LUT address. The absolute values of the GMSK frequency trajectories are saved in the frequency path LUT. If the second bit is inverted, it can be used as a sign bit, as shown in Figure 13.4. Therefore there is no need to save the sign bits in the LUT (see Figure 13.3). The frequency trajectories are symmetric around the time axes in Figure 13.4. It follows that the counter moves in a forward direction at the first half portion and in a backward direction at the second half portion in Figure 13.3. Furthermore, the MUX and the XOR (X3) are needed to decode the address. The frequency trajectory is constant when the address of the frequency trajectory LUT is [000] or [111]. The required LUT size is reduced to less than one quarter of the original size (1:5.3) by eliminating the redundant data. Of course, the complexity of the address decoder has increased, but the decrease of the LUT size compensates more than enough.

The number of samples per symbol is 192 (see Section 13.5). The burst length is 156.25 bits in the GSM 900 and DCS 1800 systems [GSM96a]. A quarter of a guard bit (= 0.25×192 = 48 samples) is inserted after each burst after the eight guard bit ones [GSM96a]. Therefore the counter has 48/192 modes in Figure 13.3.

The output of the adder/subtracter is

$$N_n = (C_n \pm L_n), \tag{13.9}$$

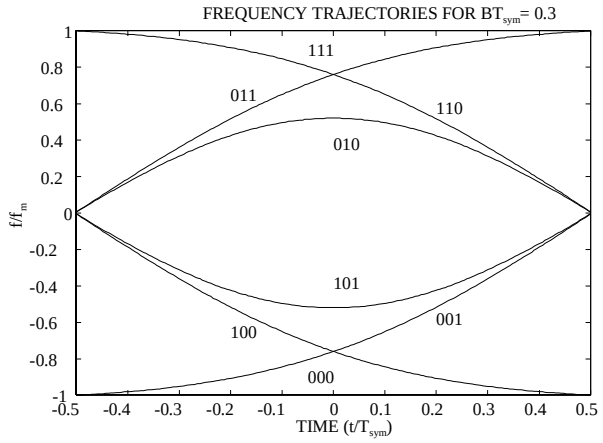

Figure 13.4. Frequency trajectories for $BT_{sym} = 0.3$.

where C_n is the carrier frequency (± carrier offset) control word, L_n is the frequency modulation control word (the LUT output), N_n is the input to the phase accumulator, n being the time index. The phase value of the phase accumulator is

$$P_n = (N_n + P_{n-1}) \bmod 2^j, \tag{13.10}$$

where j is the phase accumulator width. The phase accumulator acts as a digital integrator followed by a modulo 2^j operator. The output frequency is

$$f_{out} = \frac{\Delta P_n}{\Delta T} = \frac{N_n f_{clk}}{2^j}, \tag{13.11}$$

where f_{clk} is the clock frequency. The input to the phase accumulator, N_n, can only have integer values, therefore the frequency resolution is found setting, $N_n = 1$, as

$$\Delta f = \frac{f_{clk}}{2^j}. \tag{13.12}$$

The phase accumulator addresses the sine read only memory (ROM), which converts the phase information into the values of a sine wave. An alternative method to implement the sine synthesis and multiplier is to use the CORDIC algorithm (see Section 6.2.2.5). A straightforward implementation of the sine memory requires a $2^{14} \times 12$ bits ROM. Therefore a sine memory compression technique is applied to reduce the size and access time of the sine ROM [Tan95a]. This DDS architecture takes advantage of the symmetry of a sine wave to reduce ROM storage requirements. Table 6.1 shows how much memory and additional circuits are needed in each memory compression and algorithmic technique to meet the spectral requirement for the worst-case spur level, which is about -85 dBc due to the sine memory compression. The spur level (-85 dBc) will stay below the spur level of the 14-bit D/A-converter at a 15 MHz IF output. The best compression ratio is given by the Taylor series approximation, but a multiplier is needed. In the VLSI implementation the problem of the CORDIC algorithm is in the hardware complexity. In this design the Modified Sunderland architecture is used, because it gives a lower worst-case spur level than the Nicholas architecture with the same hardware complexity. The word length of the sine ROMs could be shortened by 2 b, when the sine ROMs store the difference between the sine amplitude and the phase (storing [sin(πx/2)-x]) (see Section 6.2.2.1). The trade-off is an extra adder at the output of the sine ROM to perform the operation ([sin(πx/2)-x] + x). This method is not used, because the extra adder trade-offs the benefits in the chip area, and the 2-bit reduction in the output has a negligible effect on the speed of the ROMs in this design.

One only needs to store sine samples from 0 to π/2, as shown in Figure 13.3. The coarse sine ROM provides low resolution samples, and the fine sine ROM gives additional resolution by interpolating between the low resolution samples in Figure 13.3. The $2^{14} \times 12$ sine samples are compressed into $2^8 \times 11$ coarse samples and $2^8 \times 4$ fine samples, resulting in a compression ratio of 51:1. A FFT of the compressed ROM contents gives a worst-case digital output spectral purity of -87 dBc. The multiplier controls the amplitude of the digital GMSK modulated IF signal in Figure 13.3. The four GMSK modulated signals are combined together in the digital domain

Table 13.1. Specification of power ramping and power control block.

Ramp-up time	14 μs
Ramp-down time	14 μs
Ramp curve type	Raised cosine/sine
Output word length	12 bits
Power control range	0...-32 dB
Power control step	2 dB
Power control fine tuning step	0.25 dB

as shown in Figure 13.2. Next, the signal is presented to the D/A converter, which develops an analog signal.

13.4 Ramp Generator and Output Power Level Controller

13.4.1 Conventional Solutions

Multi-carrier transmission with digital carrier combining necessitates power control to be implemented in the digital domain. Otherwise, it would not be possible to adjust the relative power of a single carrier with respect to the others. Therefore the digital ramp generator and output power level controller is used in Figure 13.3.

The conventional ramp generator and output power level controller is shown in Figure 13.5. The size of the memory is about $(f_{clk} \times T_r) \times$ outw, where f_{clk} is the digital IF modulator clock frequency (sampling frequency), T_r is the pulse duration and outw is the multiplier input width in Figure 13.3. The clock frequency is high in the digital IF modulators, therefore the size of the memory is large. For example, if the clock frequency is 52 MHz and the ramp duration is 14 μs, as shown in Table 13.1, then the size of the memory will be about 728 × 12 bit in Figure 13.5. Furthermore, the multiplier is needed to set the output power level in Figure 13.5.

Another conventional method for implementing the ramp generator and output power controller is to use a FIR-filter. The number of FIR filter taps is $(f_{clk} \times T_r)$, where f_{clk} is the digital IF

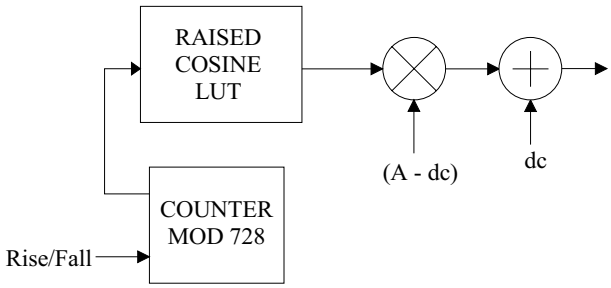

Figure 13.5. Conventional ramp generator.

modulator clock frequency and T_r is the pulse duration. Due to the high clock frequency in the IF modulators, there are many taps in the FIR. For example, if the clock frequency is 52 MHz and the ramp duration is 14 μs, as shown in Table 13.1, then the number of the FIR filter taps will be 728. Multistage implementations may reduce the number of the taps somewhat.

13.4.2 Novel Ramp Generator and Output Power Controller

The downlink dynamic power control in the GSM 900/DCS 1800 uses 16 power levels with a 2 dB separation. The power control range of the proposed design is 0...-32 dB, where the 0 dB level is the nominal maximum power. The additional 2 dB range is reserved to assist transmit chain gain stabilization. Furthermore, a power control fine tuning step (0.25 dB) is required for this purpose (see Table 13.1). The power level can be changed burst by burst. The digital GMSK modulated IF signal is multiplied by the ramp signal for a smooth rise and fall of the burst in Figure 13.3. The power control is realized by scaling the ramp curve, which follows a raised cosine/sine curve. Hence, the ramp-up curve starts from the minimum power level, but settles to the level specified by the power level indication as shown in Figure 13.6.

The burst signal can be considered to be the product of the original modulated signal m(t) and a periodical switching signal sw(t). The spectrum of the burst signal is the square of the absolute value of convolution of these two signals in the frequency domain.

For rectangular switching, we get

$$W(f) = \left|M(f - f_c) * SW(f)\right|^2 = K \left| \sum_{n=-\infty}^{\infty} M(f - f_c - nf_g) \frac{\sin \pi n f_g T_b}{\pi n f_g T_b} \right|^2 , \quad (13.13)$$

where * denotes convolution, f_c is the carrier frequency, f_g is the burst gating rate, T_b is the burst length, and K is a proportional constant.

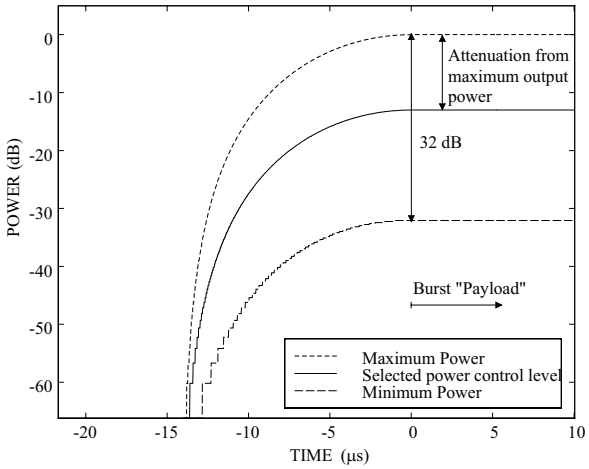

Figure 13.6. Power control feature combined to power ramping.

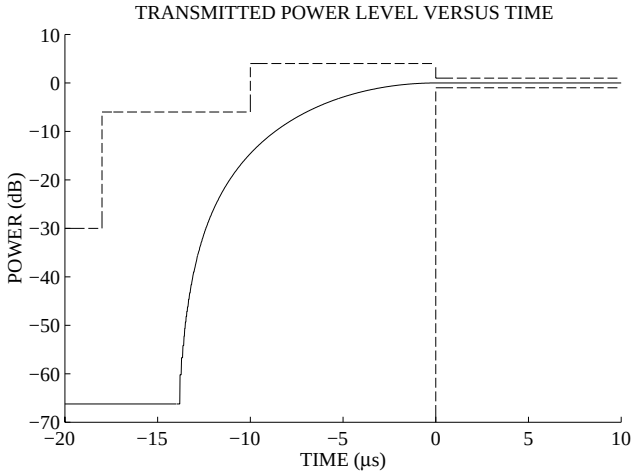

Figure 13.7. Ramp up profile of a transmitted time slot.

For raised cosine/sine switching, we get

$$W(f) = H \left| \sum_{n=-\infty}^{\infty} M(f - f_c - nf_g) \frac{\sin \pi n f_g (T_b - T_r)}{\pi n f_g (T_b - T_r)} \frac{\cos \pi T_r n f_g}{1 - (2 T_r n f_g)^2} \right|^2, \quad (13.14)$$

where T_r is the ramp duration, and H is a proportional constant.

The spectrum of the periodic burst signal consists of infinite numbers of secondary spectral lobes which have the same shape as M(f), separated by the burst gating rate f_g, and have decreasing amplitudes. The secondary spectral lobes decay faster in (13.14) than in (13.13), and for this reason the raised cosine/sine switching is used. The following function is used to smooth out the rise of the burst

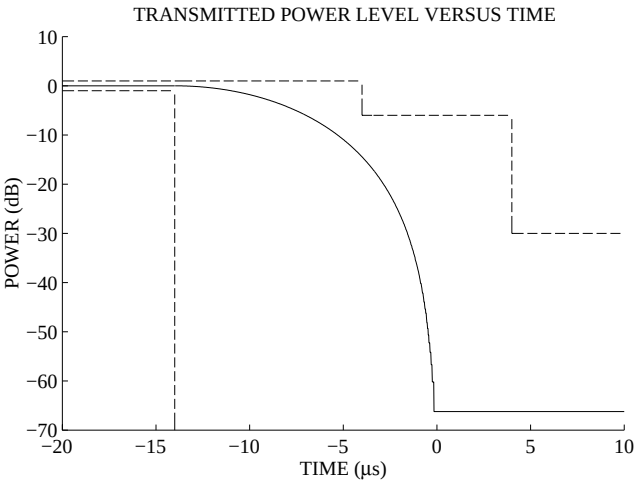

Figure 13.8. Ramp down profile of a transmitted time slot.

$$(A - dc)\sin(\frac{\pi t}{2T_r})^2 + dc, \tag{13.15}$$

where T_r indicates the ramp duration, t is [0 T_r], A is the amplitude of the GMSK-modulated signal, and dc is the dc offset (determines the starting power level in Figure 13.7). Using trigonometric identities, this expression can be presented as

$$\frac{1}{2}\left\{(A + dc) + (A - dc)\cos(\frac{\pi t}{T_r} + \pi)\right\} \tag{13.16}$$

In the above equation the cosine/sine term is not raised and so it could be implemented by a sinusoidal oscillator. The following function is used to smooth out the fall of the burst:

$$(A - dc)\cos(\frac{\pi t}{2T_r})^2 + dc. \tag{13.17}$$

Using trigonometric identities, this expression can be presented as

$$\frac{1}{2}\left\{(A + dc) + (A - dc)\cos(\frac{\pi t}{T_r})\right\} \tag{13.18}$$

where dc is the dc offset (sets the power level after the ramp in Figure 13.8).

The novel ramp generator and output power level controller is shown in Figure 13.9. The core of this structure is a well-known second-order direct-form feedback structure. The constant (A+dc) in (13.16) and (13.18) is added to the sinusoidal oscillator output. The amplitude of the cosine term is (A-dc) from (13.16) and (13.18). The binary shift (2^{-1}) is implemented with wiring. During the ramp period the signal sel is low in Figure 13.9 and the multiplexer conducts the ramp signal to the multiplier (Figure 13.3). After the ramp duration (T_r) the signal sel becomes high; the output of the multiplexer is connected to the input of the multiplexer; and the output power level is constant. The cosine term is implemented by the second-order difference equation in Figure 13.9 [Gol69]. Figure 13.9 shows the signal flow graph of the second-order direct-form feedback structure with state variables $x_1(n)$ and $x_2(n)$. The details of this structure are presented in Section 3.1. Any real-valued sinusoidal oscillator signal can be generated by the sec-

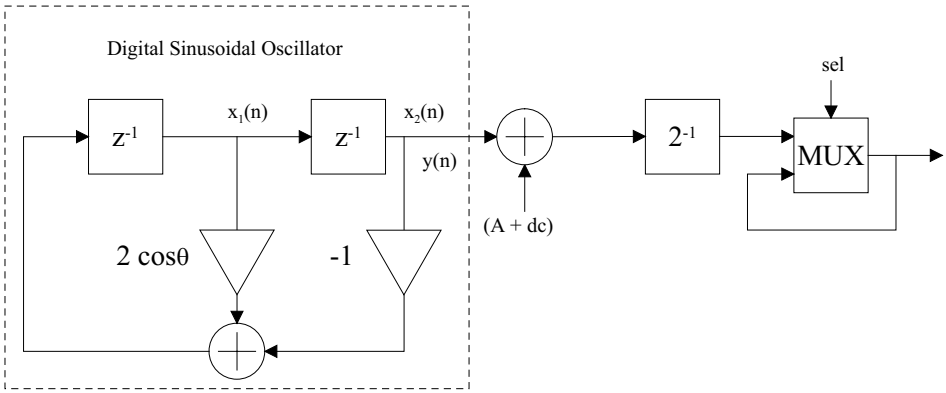

Figure 13.9. Ramp generator.

ond-order structure shown in Figure 13.9. The digital oscillator amplitude (*A'*) is (*A* - *dc*) from (13.16) and (13.18). The initial phase offsets of the digital oscillator are 0 for the ramp down and π for the ramp up, from (13.16) and (13.18). The initial values for these phase offsets are calculated from (3.10) and (3.11). Hence, for the falling ramp ($\varphi_0 = 0$), the initial values are

$$x_1(0) = (A - dc)\cos(\theta_0), \tag{13.19}$$

$$x_2(0) = (A - dc). \tag{13.20}$$

For the raising ramp ($\varphi_0 = \pi$)

$$x_1(0) = -(A - dc)\cos(\theta_0), \tag{13.21}$$

$$x_2(0) = -(A - dc). \tag{13.22}$$

The initial values for the ramp up are the negatives of the initial values for the ramp down.

The output sequence $y(n)$ of the ideal oscillator is a sampled version of a pure sine wave. The angle θ_0 represented by the oscillator coefficient is given by

$$\theta_0 = 2\pi\, f_0 / f_{clk}, \tag{13.23}$$

where f_0 is the desired frequency in cycles per second. In an actual implementation, the multiplier coefficient $2\cos\theta_0$ is assumed to have $b + 2$ bits. In particular, one bit is for the sign, one bit for the integer part and b bits for the remaining fractional part in the fixed-point number representation. Then the largest value of the coefficient $2\cos(\theta_0)$ which can be represented is $(2 - 2^{-b})$. This value of the coefficient gives the smallest value of θ_{min}, which can be implemented by the direct form digital oscillator using b bits:

$$\theta_{\min} = \cos^{-1}\left[\frac{1}{2}(2 - 2^{-b})\right]. \tag{13.24}$$

Therefore, the smallest frequency, which the oscillator can generate, is

$$f_{\min} = \frac{\theta_{\min}}{2\pi}\, f_{clk}, \tag{13.25}$$

where f_{clk} is the clock frequency (sampling frequency). As an example, let $b = 25$ bits. The largest oscillator coefficient ($2\cos(\theta_0)$) is 67108863/33554432, and thus $\theta_{min} = \cos^{-1}(67108863/67108864) \approx 0.00017263$. For $f_{clk} = 52$ MHz and $b = 25$, $f_{min} \approx 1.43$ kHz.

During the ramp the phase change is π in (13.16) and (13.18), and therefore the required output frequency is

$$f_0 = \frac{1}{2T_r}. \tag{13.26}$$

The smallest frequency (f_{min}) should be below f_0. For $T_r = 14$ μs, $f_0 \approx 35.71$ kHz.

The power control is realized by scaling the ramp curve. The amplitude of the sinusoidal is controlled by A in (13.16) and (13.18). The downlink dynamic power control in the GSM 900/DCS 1800 uses 16 power levels with a 2 dB separation. The power control range is 0...-32

dB, where the 0 dB level is the nominal maximum power. Therefore, the amplitude (A) value range of the initial values is from 0.0251 to 0.999. The simulated power control resolution (see Section 13.4.3) is below 0.25 dB (see Table 13.1).

If the ramp time is variable, then a fully parallel multiplier is needed. For applications with a fixed ramp time, a fully parallel multiplier is not required and it would indeed be a waste of silicon area. Instead, multiplication by a fixed binary number can be accomplished with (N-1) adders, where N is the number of non-zero bits in the coefficient. If the clock frequency is 52 MHz, the output frequency of the oscillator is 35.71 kHz and b is 25, and the coefficient $2\cos(2\pi f_0/f_{clk})$ is 1.99998137757162 $(01111111111111111110110001111)_2$. This requires 21 adders. One way to reduce the hardware complexity of the direct-form digital oscillator was proposed in [Abu86a] and can be obtained by setting

$$2\cos(\theta) = 2 - 2^{-b1}\left\lfloor 2^{b1}(2 - 2\cos(\theta))\right\rfloor,$$
$$\text{where} \quad b1 = \left\lceil \log_2 \frac{1}{2(1-\cos\theta)} \right\rceil, \tag{13.27}$$

and $[r]$ is the smallest integer greater than or equal to r. The coefficient $(2–2\cos(2\pi f_0/f_{clk}))$ is 0.00001862 $(00000000000000000001001110000)_2$. The total number of adders required to implement the coefficient $2\cos(2\pi f_0/f_{clk})$ is reduced from 21 to 4. The coefficient is formed by multiplying the small fraction $(2 - 2\cos(2\pi f_0/f_{clk}))$ by the factor 2^{b1}, where $b1$ is 15. This reduces hardware complexity by reducing the maximum word length needed in the adders. The output of the adders must be multiplied by 2^{-b1} to keep the overall gain unchanged. The number of adders could be reduced further using the CSD numbers. The block diagram of the modified ramp generator and output power controller is shown in Figure 13.10. The novel ramp generator and output power level controller in Figure 13.10 can be implemented with the aid of three two-input adders, two delays, one multiplexer and the fixed multiplier, which can be accomplished with (N-1) adders, where N is the number of non-zero bits in the coefficient. The novel ramp generator and output power level controller need neither a memory nor a fully parallel multiplier (see Figure 13.5), so it can be easily implemented with standard cells.

The D/A converter exhibits a fully sampled-and-hold output that causes the sinx/x roll-off

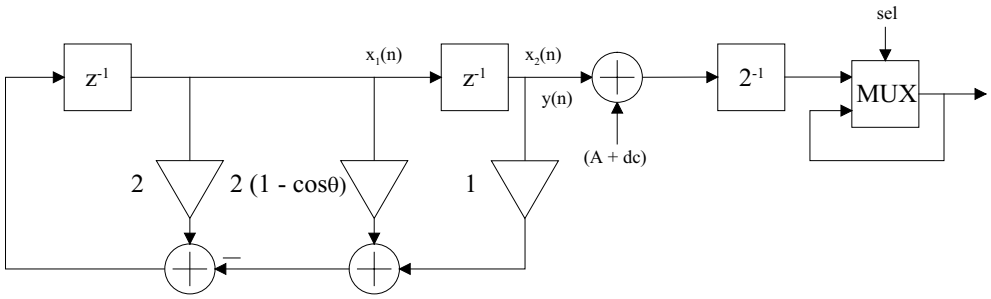

Figure 13.10. Modified ramp generator.

function on the spectrum of the converted analog signals. In the multi-carrier GMSK modulator the output band is from 11.5 MHz to 16.5 MHz. This introduces a droop of –0.779 dB, which is not acceptable. One method is to compensate the sinx/x roll-off by the inverse sinx/x filter in the IF frequency [Sam88]. The digital ramp generator and output power level controller could compensate for this droop when the bandwidth of the single carrier is narrow. The sinx/x roll-off is taken into account when the power level (amplitude) value of the carrier is calculated.

The dynamic range in the transmission could be optimized digitally by setting the multi-carrier signal peak value equal to the D/A converter full scale. However, this approach is not utilized in this design due to required power compensation in the analog domain. The problem with the analog solutions is the inaccuracy due to aging, temperature and component variations. Furthermore, the analog solutions are complex, and stability might be a problem. This design enables digital fine-tuning of the carrier power level with adjustable accuracy.

13.4.3 Finite Word length Effects in Ramp Generator and Output Power Controller

The error at the ramp generator output consists of two components:

$$e(n) = e_1(n) + e_2(n), \tag{13.28}$$

where $e_1(n)$ is the error due to the ramp generator output truncation, and $e_2(n)$ is the error that has been accumulated as a result of the recursive computations in the digital oscillator.

The bounds for $e_1(n)$ are given by

$$-2^{-c} < e_1 \leq 0, \tag{13.29}$$

for truncation, and by

$$-\frac{2^{-c}}{2} \leq e_1 \leq \frac{2^{-c}}{2}, \tag{13.30}$$

for rounding where c is the number of fractional bits in the output of the ramp generator and output power level controller.

Table 13.2. Assumed multi-carrier GMSK modulator specifications.

Symbol rate	270.833 Kbit/s
Frequency error	2 Hz
Hopping bandwidth	5 MHz
Output bandwidth	11.5 – 16.5 MHz
Hopping frequency	1.733 kHz (GSM burst-by-burst)
System clock frequency	52 MHz
Number of carriers	Four
Carrier spacing	200 kHz
Modulation	GMSK with $BT_{sym} = 0.3$
Phase error rms	1.5°
Phase error peak	2.5°

If truncation is used, the right-hand side of (13.29) is negative, since $e_2(k)$ is negative (see (2.15)), and $\sin(\theta_0(n\text{-}k\text{+}1))$ is positive, because the digital oscillator generates only half of the sine wave period (see (13.16) and (13.18)). The fact that the error is a deterministic signal [Fli92] forces us to investigate the worst-case, which corresponds to the case where every truncation suffers from the maximum absolute error value. In this case the digital oscillator generates one half of the period, and thus the upper limit for the output error becomes

$$y_{\max err}(M) = \frac{e_{\max}}{\sin\theta_0}\sum_{k=2}^{M}\sin(\theta_0\,(M-k+1)) \approx \frac{2^{-b}}{\sin\theta_0\,\sin(\theta_0/2)} \approx \frac{2^{-b+1}}{\theta_0^2}, \qquad (13.31)$$

where $e_{\max} = -2^{-b}$ is the worst-case truncation error, b is the number of fractional bits in the digital oscillator, $0 < \theta_0 << 1$, $M = [\pi/\theta_0]$ and $[r]$ is the smallest integer greater than or equal to r.

If rounding is used, $e_2(k)$ will have positive and negative values and so the output error sequence will have lower values than in the case of truncation (see Figure 13.11). The simulations indicate that the accumulated error is below the output quantization error when rounding is used, b is 25 and c is 12.

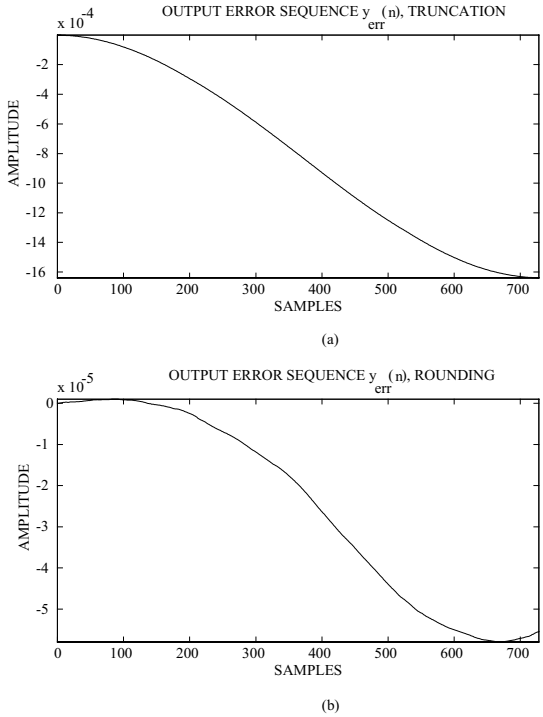

Figure 13.11. Output error sequence for (a) truncation and (b) rounding. (Parameters: sampling frequency 52 MHz, output frequency 35.71 kHz and 25 fractional bits).

13.5 Design Example

In this section an investigation will be carried out into which parameter values of the digital GMSK modulator are required to accomplish the system specifications for a base station modulator [GSM96d].

1. Determining of the number of samples per symbol and the clock frequency

$$f_{clk} = S \times f_{sym}, \tag{13.32}$$

where f_{sym} is 270.833 Kbit/s. When S is 192, and f_{sym} is 270.833 Kbit/s, f_{clk} is 52 MHz.

2. The frequency resolution will be 0.77 Hz by (13.12), when f_{clk} is 52 MHz, and j is 26. The frequency resolution is better than the target frequency error specification in Table 13.2.

3. Determining the LUT output word length (e)

$$\frac{2^e f_{clk}}{2^j} > f_d, \tag{13.33}$$

where f_d is the maximum absolute value of the frequency deviation due to the modulation, and f_d is $f_{sym}/4$ in this design example. If e is equal to 17, then equation (13.33) is true.

Other word lengths in the multi-carrier GMSK modulator are shown in Figure 13.2. and Figure 13.3. The D/A converter word length is 14 bits, which is the maximum word length in state of the art IF D/A converters [Bug00]. After the four carriers are combined together in Figure 13.2, the power per carrier is not changed, but the noise floor is increased by 6 dB. Thus, the carrier to noise ratio is decreased by 6 dB. Increasing the word lengths of the sine ROM and the multiplier, and doing the quantization after the carrier combination could reduce this degradation. In the GMSK IF modulator, most of the spurs are generated less by digital errors (quantization errors) and more by analog errors in the D/A converter. Hence the spectral improvement in the digital output would not be visible in the D/A converter IF output. The word lengths used are sufficient to fulfill the spectrum requirements due to the modulation, as shown in Figure 13.20 and Figure 13.21. The increased word lengths of the multipliers and sine ROMs will add complexity and enlarge the core area. Therefore, it was decided that the word lengths shown in Figure 13.2 and Figure 13.3 should be used.

13.6 Multi-Carrier GSM Signal Characteristics

The GMSK modulation method used in the GSM 900 and DCS 1800 is a constant envelope modulation scheme. This property is very desirable from the linearity point of view in the single

Table 13.3. Crest factors of multi-carrier GSM 900/DCS 1800 signals.

Number of GSM 900 carriers	Simulated crest factor [dB]	Theoretical crest factor [dB]
1	3.0122	3.0103
2	6.0229	6.0206
4	9.0294	9.0309
8	12.0396	12.0412

carrier transmission, because, as such, it allows the usage of fairly non-linear components in the transmission chain [And86]. On the other hand, the multi-carrier signal has very unfavorable characteristics because signals with a constant envelope quite often sum up in the phase. Therefore the multi-carrier signal has a high ratio of peak value to rms value of a waveform (a high crest factor).

In order to discover the multi-carrier GSM signal characteristics, simulations were carried out using the modulator model. The simulation length was 1800 symbols, and 192 amplitude samples per one symbol were taken. The multi-carrier GMSK simulation employed a regular channel spacing of 600 kHz and a data rate $1/T_{sym}$ = 270.833 Kbit/s, together with a Gaussian low-pass pulse shaping filter with a normalized bandwidth BT_{sym} of 0.3. In the simulations the burst structure is 3 tail bits (0's), 58 payload bits (random 0's & 1's), 26 training sequence bits (8 different (here TS 0)) [GSM96b], 58 payload bits (random 0's & 1's), 3 tail bits (0's), 8 guard timing bits (1's), a quarter guard bit (1). Different pseudo-random number generators are used to generate each digital modulation source, thus ensuring a low correlation between the resulting carriers.

In the case of the multi-carrier GSM 900/DCS 1800, the crest factors are given in Table 13.3 for one to eight carriers. The disadvantageous behavior of the multi-carrier-GSM signal is clearly revealed by Table 13.3. For a large number of carriers, the peak power in the signal is significantly higher than the rms power (increased crest factor). An increasing amount of the signal energy is concentrated around the mid-scale values of the D/A converter in the multi-carrier GMSK modulator. As a result, a "small-scale" dynamic and static linearity of the D/A converter becomes increasingly critical in obtaining a low intermodulation distortion, and maintaining a sufficient carrier-to-noise ratio. Since the power amplifier is normally most non-linear in saturation at high powers, peaks in the signal amplitude signify a non-linear amplification. This, in turn, dictates the intermodulation and spectral regrowth. However, the analysis of spurs, har-

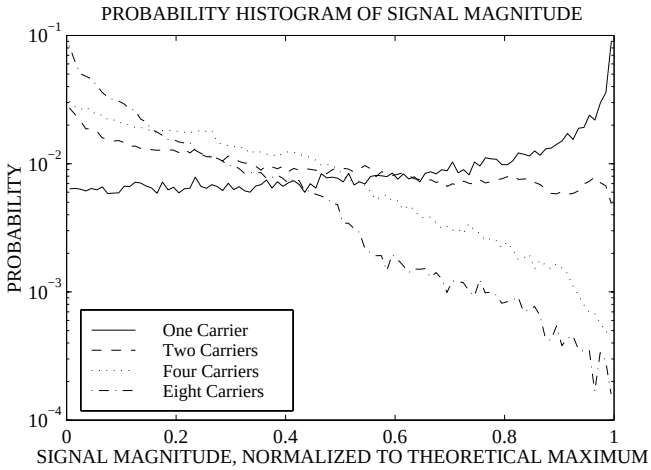

Figure 13.12. Magnitude probability density of multi-carrier GMSK signals.

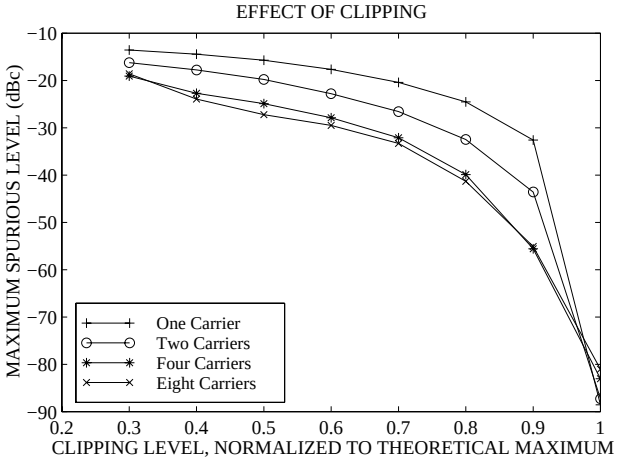

Figure 13.13. Maximum spurious level due to clipping.

monics and noise from the filters, mixers and the power amplifier are beyond the scope of this thesis.

Nevertheless, the crest factors do not characterize the signal comprehensively. What really matters is how big a percentage of the time the signal amplitude lies in the range of high values, i.e. how probable is it that peak powers will actually occur. Magnitude probability densities of multi-carrier signals are shown in Figure 13.12. The magnitude probability density presented confirms that the probability of the amplitude magnitude reaching the theoretical maximum (during a given time period) decreases for an increasing number of carriers.

If the peak values of the signal were reduced then the dynamic range requirements of the D/A converter would be alleviated. One method of decreasing the peak values is to use clipping [Ben97]. Figure 13.13 clearly illustrates the effect of clipping. The harder the clipping is done, the higher is the distortion level. The distortion generated by clipping would have to conform to the spectral purity specifications of –76 dBc. Therefore, the clipping level must be set near the theoretical maximum magnitude in order to meet the spectral purity requirements, as shown in Figure 13.13.

Table 13.4. Number of symbol stages (w) in shift register.

w	rms Phase error	Peak Phase error	Spectrum Req.	Transient Req.	The size of the LUT †
2	6.138°	11.537°	No	No	768×17 bits
3	0.931°	1.754°	Yes	Yes	1536×17 bits
4	0.039°	0.090°	Yes	Yes	3072×17 bits
5	0.006°	0.012°	Yes	Yes	6144×17 bits

† The size of the uncompressed LUT is 2^(w)×192×17 bits, where w is the number of the symbol stages in the shift register in Figure 13.3.

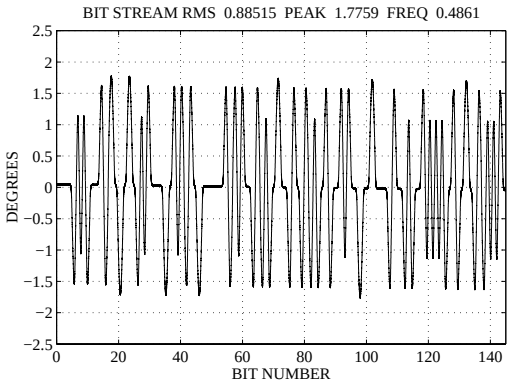

Figure 13.14. Phase errors, when shift register width is 3, in Figure 13.3.

13.7 Simulation Results

A computer model of the digital GMSK modulator has been built to simulate the effect of the parameters on the output signal. The phase trajectory of the GMSK-modulated signal generated by the digital GMSK modulator is compared with the mathematically computed ideal phase trajectory to determine the phase difference between the transmitted signal and the ideal signal. The phase difference is fitted to a linear regression line [GSM92]. The slope of the regression line provides an estimate of the frequency error of the transmitter, and the regression line subtracted from the phase difference provides an estimate of the phase error. The phase error target is specified to be 1.5° rms with the peak at 2.5° (see Table 13.2). The pseudo-random bit stream will be any 148-bit sub-sequence of the 511-bit pseudo-random bit stream [CCI92]. Table 13.4 shows phase errors with different numbers of symbol stages in the shift register. Other word lengths in the GMSK modulator are shown in Figure 13.3. In Figure 13.20 the dashed line represents the spectrum requirements in Table 13.4. Transient Req. in Table 13.4 means the spectrum due to the switching transients, which requirements are shown in the third column of Table 13.5. Figure 13.14 shows the rms phase and maximum peak error when the impulse response is truncated to 2-bit width. These phase error levels meet the assumed specifications (see Table 13.2).

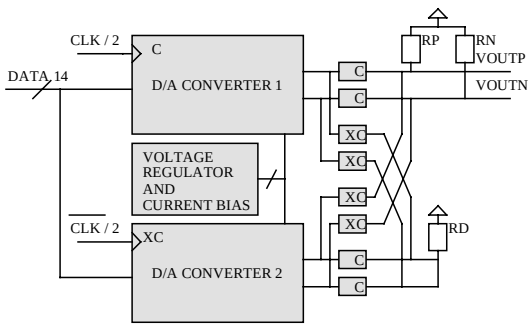

Figure 13.15. D/A converter system.

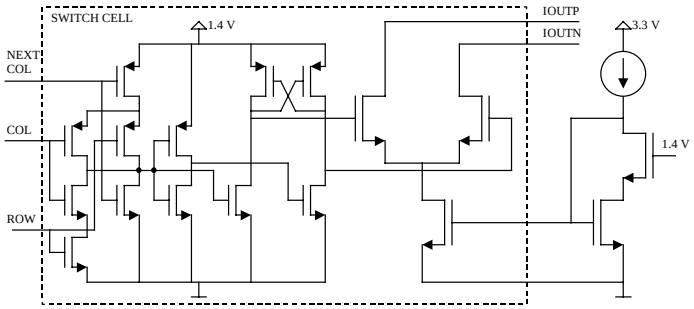

Figure 13.16. MSB switch cell of D/A converter and biasing.

Figure 13.7 and Figure 13.8 show the ramp up and the ramp down profile of a transmitted time slot. Dashed lines show the time mask for the burst by burst power ramping. The curves fully satisfy the GSM 900/DCS 1800 masks [GSM98].

13.8 Implementation

The multi-carrier GMSK modulator design was synthesized by Synopsys software from the VHDL description using the 0.35 μm CMOS standard cell library. The photomicrograph is shown in Figure 13.17. The features of the designed circuit are summarized in Table 13.6.

13.9 D/A Converter

The 14-bit D/A converter is based on a segmented current steering architecture. It consists of a 6-bit thermometer coded MSB segment, a 3-bit thermometer coded second segment and a binary coded 5-bit LSB segment. The dynamic linearity is important in this multicarrier IF modulator because the strongly varying envelope of the composite signal. The static linearity, which is achieved by sizing the current sources for intrinsic matching [Lin98], is in prerequisite to obtaining a good dynamic linearity. The maximum dynamic performance is obtained by

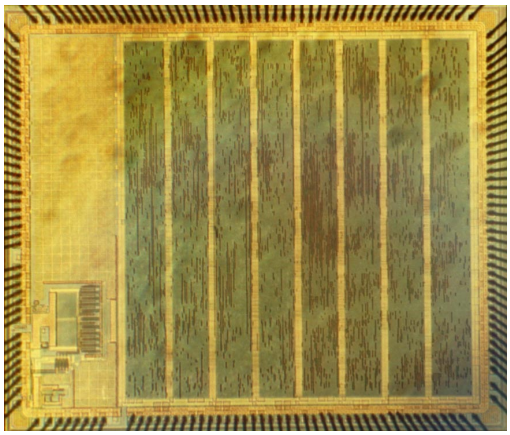

Figure 13.17. Photomicrograph of multi-carrier GMSK modulator.

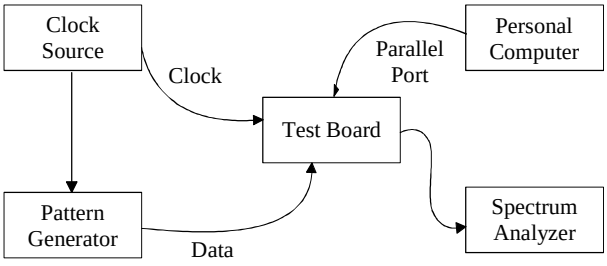

Figure 13.18. Block diagram of test system.

multiplexing two D/A converters with output sampling switches [Bal87], which are transmission gates. The D/A converter system, two D/A converters that are sampled sequentially at half clock rate, is shown in Figure 13.15. With the output switches, current transients are sampled to an external dummy resistor load RD and settled current to external output resistor loads RP and RN. As the output current is sampled, need to latch data inside the D/A converters is reduced; the D/A converter structure is simplified and the digital noise coupled to analog output current is reduced. A high swing cascode current mirror is used to bias the current source transistors of the D/A converter (Figure 13.16). The high swing cascode current mirrors enable a large V_{GS} voltage to the current source transistors and thus improved matching between the current sources, due to the decreased effect of the variation of V_T. A 1.4 V supply voltage is regulated and stabilized internally for the digital parts of the D/A converter and for the high swing current mirrors. The layout of the D/A converter 1 and 2 consists of switch cells, latched thermometer coders, LSB latches and input registers.

13.10 Layout

The multi-carrier GMSK modulator is a mixed-signal high-precision monolithic device, which required a significant design effort at the physical level. The D/A-converter is implemented with a differential design, which results in reduced even-order harmonics and provides com-

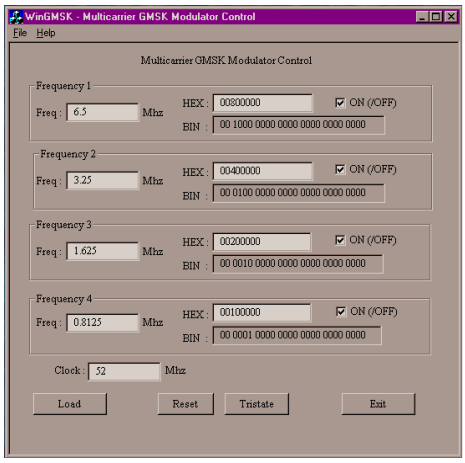

Figure 13.19. User interface.

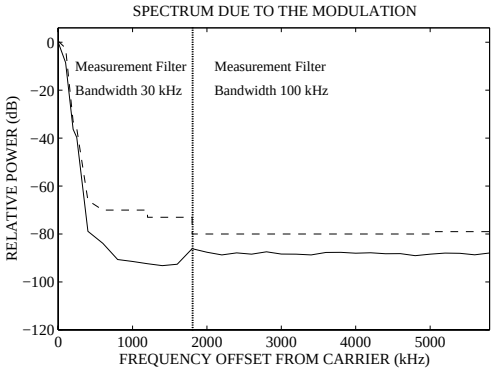

Figure 13.20. Spectrum due to the modulation in the case of the single carrier. Some margin (6 dB) has been left between the most stringent modulation spectrum requirement defined for GSM 900 and DCS 1800 BTS in [GSM98] and the values specified in Figure 13.20 at offsets larger than 1800 kHz, because in the case of the multi-carrier digital modulator it is not possible to use steep analog bandpass filters (Figure 13.1) around each carrier.

mon-mode rejection to disturbances. To minimize the coupling of the switching noise from the digital logic to the analog output, the power supplies of the digital logic and the analog part are routed separately. On-chip decoupling capacitors (total capacitance of 2 nF) are used to reduce the ground bounce in the digital part. To reduce the supply ripples even further, additional supply and ground pins are used to reduce the overall inductance of packaging. Since the substrate is low ohmic, the most efficient way to decrease noise coupling through the substrate is to reduce the inductance in the substrate bias [Su93]. In this circuit this inductance is small because the die with a conductive glue on the backplane is connected to the ground level through several bonding wires and package pins. The D/A converter was surrounded by separate guard rings to minimize the noise coupling to the analog output through the substrate. Separate pads connect the guard rings to the off-chip ground. The interferences at the on-chip D/A converter output band are reduced, avoiding hardware using in-band clock frequencies (frequency planning).

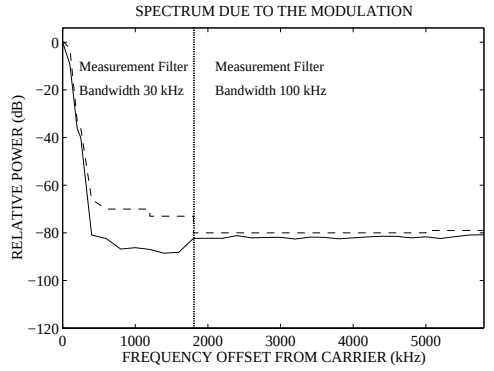

Figure 13.21. Spectrum due to the modulation in the case of the multi-carrier. Some margin (6 dB) has been left between the most stringent modulation spectrum requirement defined for GSM 900 and DCS 1800 BTS in [GSM98] and the values specified in Figure 13.20 at offsets larger than 1800 kHz, because in the case of the multi-carrier digital modulator it is not possible to use steep analog bandpass filters (Figure 13.1) around each carrier.

13.11 Measurement Results

To evaluate the multi-carrier GMSK modulator, a test board was built and a computer program was developed to control the measurement. Figure 13.18 illustrates the block diagram of the multi-carrier GMSK modulator test system. The program runs under Microsoft® Windows (see Figure 13.19).

The modulation and power level switching spectra can produce a significant interference in adjacent bands. The dashed line shows the spectrum requirements due to the modulation in Figure 13.20. All time slots will be set up to transmit at full power [GSM98]. Some margin (6 dB) has been left between the values in [GSM98] and the values specified in Figure 13.20 after 1800 kHz because in the case of the multi-carrier digital modulator, it is not possible to use steep analog bandpass filters (Figure 13.1) around each carrier. Figure 13.20 shows the spectrum due to the modulation in the case of the single carrier. Figure 13.21 shows the spectrum due to the modulation in the case of the multi-carrier transmission. After the four carriers are combined together in Figure 13.2, the power per carrier is not changed, but the noise floor is increased by 6 dB. Therefore the noise floor is about 6 dB higher in Figure 13.21 than in Figure 13.20. Increasing the word lengths of the sine ROM and the multiplier, and changing the quantization to

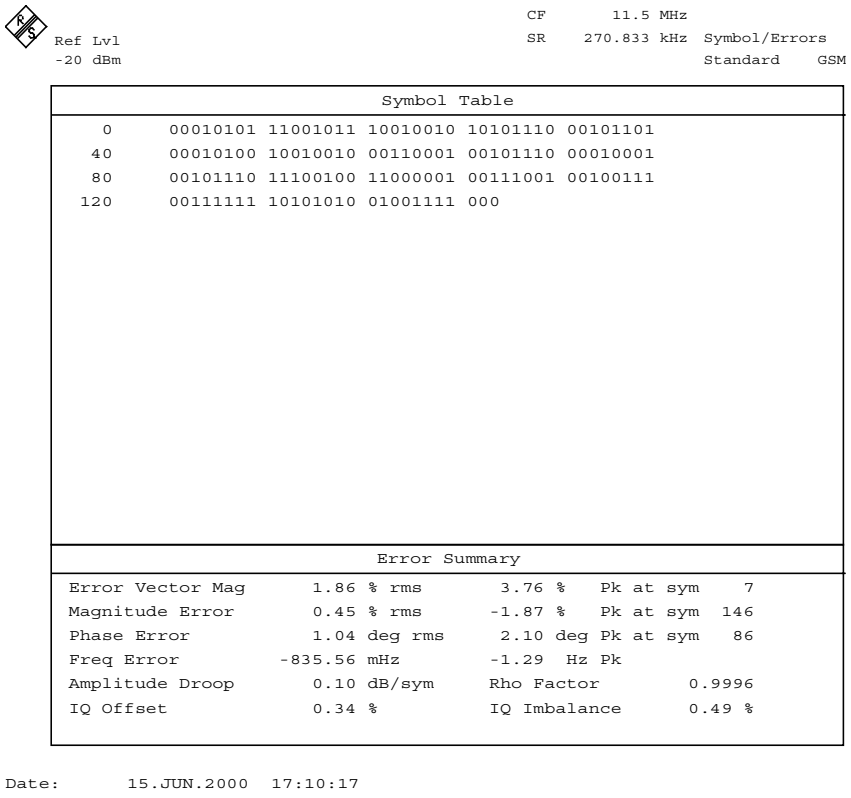

Figure 13.22. Measured phase and frequency errors.

be done after the carrier combining, could reduce this degradation. In the GMSK IF modulator, most of the spurs are generated less by digital errors (quantization errors) and more by analog errors in the D/A converter. Hence the spectral improvement in the digital output would not be visible in the D/A converter IF output. The word lengths used are sufficient to fulfill the spectrum requirements due to the modulation as shown in Figure 13.20 and Figure 13.21. The increased word lengths of the multipliers and sine ROMs will add complexity and enlarge core area. Therefore, it was decided that the word lengths shown in Figure 13.2 and Figure 13.3 should be used.

The phase error target is specified to be 1.5° rms with the peak at 2.5°, and the target frequency error is 2 Hz (see Table 13.2). The measured rms phase error is 1.04° with a maximum peak deviation 2.1°, and frequency error –1.2 Hz at the D/A converter output (see Figure 13.22).

Figure 13.23 shows the measured ramp up and down profiles of the transmitted burst, which satisfy the GSM 900/DCS 1800 base station masks. The power measured due to switching transients, which determines allowed spurious responses originating from the power ramping before and after the bursts, will not exceed the values shown in Table 13.5 [GSM98]. Some margin (3 dB) has been left between the values in [GSM98] and the values specified in Table 13.5. This

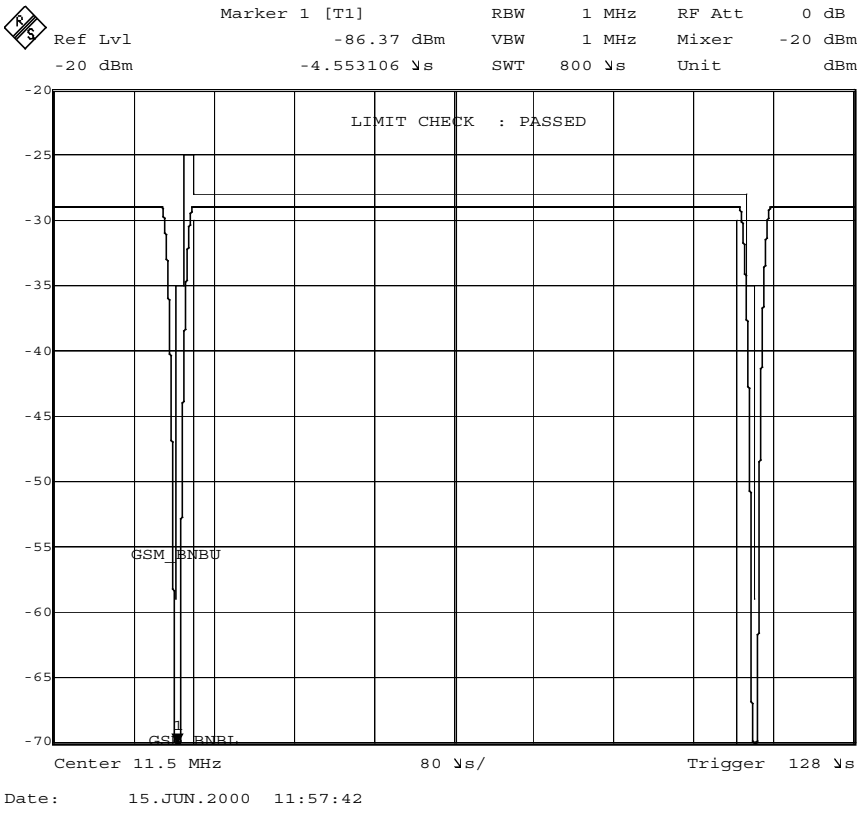

Figure 13.23. Transmitted power level of burst versus time.

Table 13.5. Spectrum due to switching transients (peak-hold measurement, 30 kHz filter bandwidth, reference ≥ 300 kHz with zero offset).

Offset (kHz)	Maximum power limit (dBc)		Measured Max. power (dBc) at digital output	Measured Max. power (dBc) at D/A converter output
	GSM 900	DCS 1800/1900		
400	- 60	- 53	-71.20	-63.85
600	- 70	- 61	-78.09	-62.56
1200	- 77	- 69	-84.97	-64.66
1800	- 77	- 69	-86.23	-63.88

margin should take care of the other transmitter stages that might degrade the spectral purity of the signal. The power levels measured at the digital output are well below the limits shown in Table 13.5. The power levels measured at the D/A converter output are not below the limits shown in Table 13.5.

The output signal in Figure 13.24 fulfills the spectrum mask requirements [GSM98]. Figure 13.25 shows the multi-carrier output, where all carriers are at maximum dynamic power level. Figure 13.26 and Figure 13.27 show carriers with different power levels. The problem with a digital ramp generator and output power level controller is reduced carrier to noise ratio at low power levels, because the dynamic power control is realized by scaling in the digital domain. According to specifications, modulation and power level switching spectra are measured at maximum dynamic power level [GSM98], so that the reduced carrier to noise ratio at low power levels presents no problems in meeting the specifications. Of course the base station performance will be degraded due to the reduced carrier to noise ratio.

13.12 Summary

A multi-carrier GMSK modulator has been developed and implemented. It comprises four GMSK modulators, which generate GMSK modulated carriers at the specified center frequencies. Utilization of the redundancy in the stored waveforms reduces the size of the GMSK trajectory LUT to less than a quarter of the original size in the modulator. The novel digital ramp generator and output power level controller performs both the burst ramping and the dynamic power control in the digital domain. The four GMSK modulated signals are combined together in the digital domain. Thus only one up-conversion chain is needed, which results in huge savings in the number of the required analog components.

Table 13.6. Features of designed multi-carrier GMSK modulator.

IC technology	0.35 μm CMOS (in BiCMOS)
Operating clock frequency	52 MHz @ 3.3 V
Power dissipation	706 mW at 52 MHz @ 3.3 V
Die/Core size	26.8 mm^2/ 19.1 mm^2

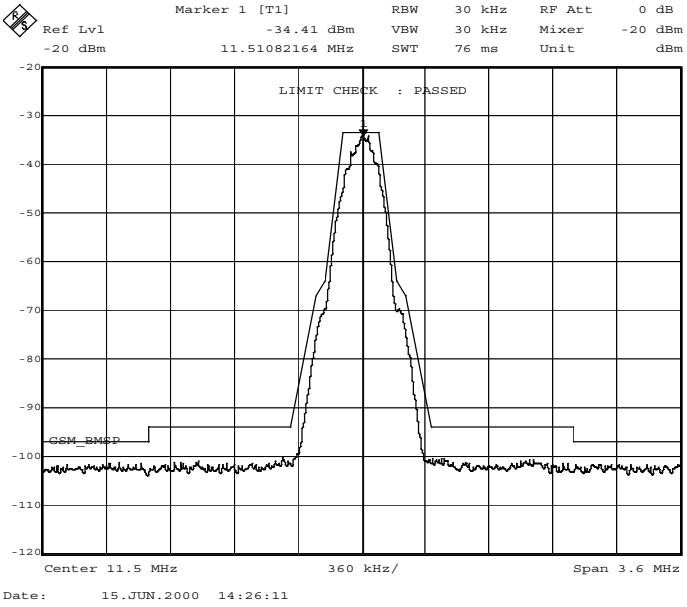

Figure 13.24. Power spectrum of modulated carrier.

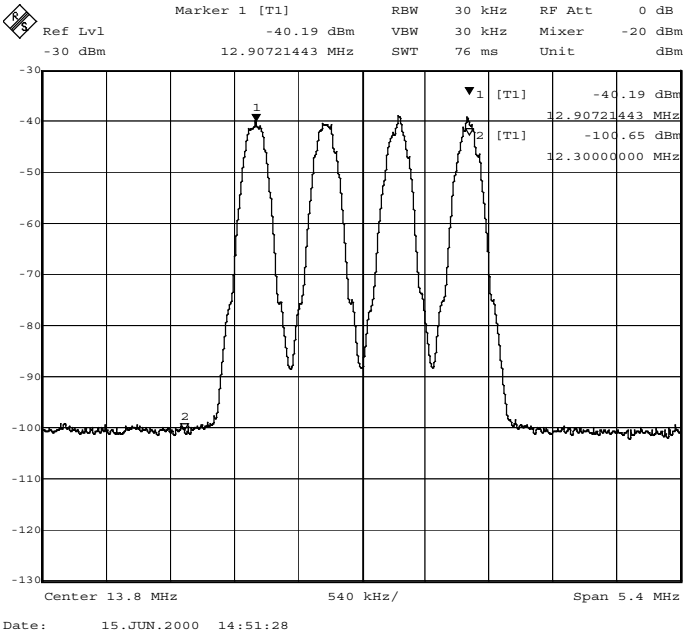

Figure 13.25. Power spectrum of modulated multi-carrier signal.

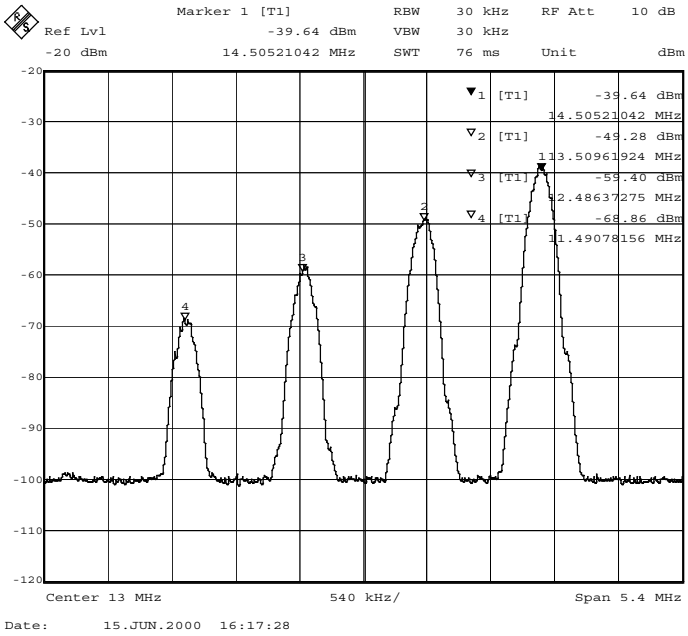

Figure 13.26. Four carriers with different power levels (relative power level difference is 10 dB).

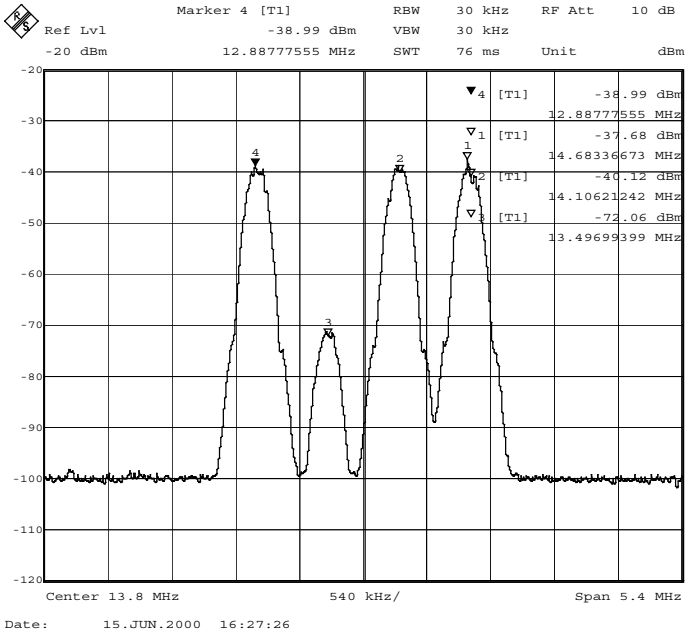

Figure 13.27. Four carriers from which one is 32 dB below the others.

14. Conclusions

The aim of this research was to find an optimal front-end for a transmitter by focusing on the circuit implementations of the DDS, but the research also includes the interface to baseband circuitry and system level design aspects of digital communication systems. The theoretical analysis gives an overview of the functioning of DDS, especially with respect to noise and spurs. Although most of this material is already present in the literature, the author extends the analysis at several places:

- The quantization errors in the CORDIC algorithm are determined for a uniform distribution, independent of the signal. Previous analyses made the pessimistic assumption that the error obtains its maximum value at each quantization step.
- The worst-case carrier-to-spur ratio bounds resulting from phase truncation are derived.
- A new analysis is presented for the carrier-to-noise power with non-subtractive phase dithering.

Four ICs, which were the circuit implementations of the DDS, were designed. One programmable logic device implementation of the CORDIC based QAM modulator has been carried out. In Chapter 10 the complete DDS, including the D/A converters and low-pass filters, are integrated in the same die. According to my knowledge it is the first complete integrated DDS. The multi-carrier designs of Chapters 11 and 13 are important. These implementations show that the use of DDS techniques can result in an optimal front-end, with respect to performance, cost, and flexibility, for the transmitter of the base station. The flexibility of the solution makes this also a major step towards software radio base stations. For the realization of these designs some new building blocks, e.g. a new tunable error feedback structure and a novel and more cost-effective digital power ramp generator, were developed.

The most important circuit topology contribution is the novel ramp generator and output power level controller in Section 13.4.2. In future studies, the ramp generator and power level controller could support a Blackman window. It gives more attenuation of switching transients than the Hanning window (raised cosine/sine). The extra cosine term requires one more digital resonator in the ramp generator and power level controller. A parallel multiplier should be used so that the ramp time is flexible. The use of parallelism to attain high throughput could be utilized for the ramp generator and output power level controller.

In future studies, a variable interpolator could be used in the modulator. The variable interpolator allows the use of the sampling rates that are not multiples of the symbol rates. It enables one to transmit signals having different symbol rates. This is important in multi-standard modulators.

Another interesting field for further research is the implementation of interpolation filters using IIR filters. The main benefit of IIR filters is high efficiency, i.e. high stopband attenuation and a narrow transition band may be achieved with very few coefficients. Due to the feedback loop in

IIR filters, they may have parasitic oscillations. The phase response of IIR filters is not linear, which causes phase distortions that may corrupt the information stored in the signal. There exists a special class of IIR filters whose phase responses are approximately linear.

References

[Abu86a] A. I. Abu-El-Haija, and M. M. Al-Ibrahim, “Digital Oscillator Having Low Sensitivity and Roundoff Errors,” IEEE Trans. on Aerospace and Electronic Systems, Vol. AES-22, No. 1, pp. 23-32, Jan. 1986.

[Abu86b] A. I. Abu-El-Haija, and M. M. Al-Ibrahim, “Improving Performance of Digital Sinusoidal Oscillators by Means of Error-Feedback Circuits,” IEEE Trans. Circuits Syst., Vol. CAS-33, pp. 373-380, Apr. 1986.

[Ahm82] H. M. Ahmed, “Signal Processing Algorithms and Architectures,” Ph. D. dissertation, Department of Electrical Engineering, Stanford University, CA. Jun. 1982.

[Ahn98] Y. Ahn, and S. Nahm, ”VLSI Design of a CORDIC-based Derotator,” in Proc. ISCAS’98, Vol. 2, June 1998, pp. 449-452.

[Alt96] Implementing Multipliers in FLEX 10K Devices, Altera Application Note 53, Altera Corp., San Jose, CA, 1996.

[Alt98] FLEK 10K Embedded Programmable Logic Family Data Sheet, Altera Corp., San Jose, CA, Oct. 1998.

[Ana94] Analog Devices AD 9955 data sheet, Rev. 0, 1994, and AD9712A data sheet, Rev. 0, 1994.

[Ana99a] Analog Devices AD 9754 data sheet, Rev. 0, 1999.

[Ana99b] Analog Devices AD9850 data sheet, Rev. E, 1999.

[And86] J. B. Anderson, T. Aulin, and C.-E. Sundberg, "Digital Phase Modulation," New York: Plenum, 1986.

[And92] V. Andrews et al., “A Monolithic Digital Chirp Synthesizer Chip with I and Q Channels,” IEEE J. of Solid State Circuits, Vol. 27, No. 10, pp. 1321-1326, Oct. 1992.

[And98] R. A. Andraka, “A Survey of CORDIC Algorithms for FPGA based Computers,” in Proc. 1998 ACM/SIGDA sixth international symposium on Field Programmable Gate Arrays, Feb. 1998, pp. 191-200.

[Bal87] G. Baldwin, et al., "Electronic Sampler Switch," U. S. Patent 4,639,619, Jan. 27, 1987.

[Bas91] C. A. A. Bastiaansen, D. W. J. Groeneveld, H. J. Schouwenaars, and H. A. H. Termeer, “A 10-b 40-MHz 0.8-µm CMOS Current-Output D/A-Converter”, IEEE J. Solid-State Circuits, Vol. 26, No. 7, pp. 917-921, July 1991.

[Bas98] J. Bastos, A. M. Marques, M. S. J. Steyaert, and W. Sansen, “A 12-bit Intrinsic Accuracy High-Speed CMOS DAC,” IEEE J. Solid-State Circuits, Vol. 33, No. 12, pp. 1959-1969, Dec. 1998.

[Beh93] S. Behrhorst, "Design DDS Systems and Digitize IFs with DACs/ADCs", Microwaves & RF, Aug. 1993, pp. 111-119.

[Bel00] A. Bellaouar, et al, “Low-Power Direct Digital Frequency Synthesis for Wireless Communications,” IEEE J. Solid-State Circuits, Vol. 35, No. 3, pp. 385-390, Mar. 2000.

[Ben48] W. R. Bennett, “Spectra of Quantized Signals,” Bell Sys. Tech. J., Vol. 27, pp. 446-472, July 1948.

[Ben97] D. W. Bennett, P. B. Kenington, and R. J. Wilkinson, "Distortion Effects of Multicarrier Envelope Limiting," IEE Proc. on Commun., Vol. 144, No. 5, pp. 349-356, Oct. 1997.

[Bje91] B. E. Bjerede, ”Suppression of Spurious Frequency Components in Direct Digital Frequency Synthesizer,” U.S. Patent 5 073 869, Dec. 17, 1991.

[Bje94] B. Bjerede, J. Lipowski, J. Petranovich, and S. Gilbert, "An Intermediate Frequency Modulator using Direct Digital Synthesis Techniques for Japanese Personal Handy Phone (PHP) and Digital European Cordless Telecommunications (DECT)", in Proc. IEEE Vehicular Techn. Conf., June 1994, pp. 467-471.

[Ble87] B. A. Blesser, and B. N. Locanthi, "The Application of Narrow-Band Dither Operating at the Nyquist Frequency in Digital Systems to Provide Improved Signal-to-Noise Ratio over Conventional Dithering," J. Audio Eng. Soc., Vol. 35, pp. 446-454, June 1987.

[Bou77] N. Boutin, C. Porlier, and S. Morissette, "A Digital Filter-Modulation Combination for Data Transmission," IEEE Trans. on Commun., Vol. COM-25, pp. 1242-1244, Oct. 1977.

[Bra81] A. L. Bramble, "Direct Digital Frequency Synthesis," in Proc. 35th Annu. Frequency Contr. Symp., USERACOM (Ft. Monmouth, NJ), May 1981, pp. 406-414.

[Bu88] J. Bu, E. F. Deprettere, and F. du Lange, “On the Optimization of Pipelined Silicon CORDIC Algorithm,” in Proc. European Signal Processing Conference (EUSIPCO), Sep. 1988, pp. 1,227-1,230.

[Buc92] D. Buchanan, "Choose DACs for DDS System Applications", Microwaves & RF, Aug. 1992, pp. 89-98.

[Bug99] A. R. Bugeja, B. S. Song, P. L. Rakers, and S. F. Gillig, “A 14-b, 100-MS/s CMOS DAC Designed for Spectral Performance,” IEEE J. Solid-State Circuits, Vol. 34, No. 12, pp. 1719-1732, Dec. 1999.

[Bug00] A. R. Bugeja, and B. S. Song, "A Self-Trimming 14b 100MSample/s CMOS DAC," Proc. IEEE 1999 ISSCC, pp. 44-45, Feb. 2000.

[Can92] J. C. Candy, and G. C. Temes, "Oversampling Delta-Sigma Data Converters," IEEE Press, New York, 1992.

[Car87] L. R. Carley, "An Oversampling Analog-to-Digital Converter Topology for High-Resolution Signal Acquisition Systems," IEEE Trans. Circuits and Syst., CAS-34, pp. 83-90, Jan. 1987.

[Cav88a] J. R. Cavallaro, and F. T. Luk, “Floating Point CORDIC for Matrix Computations,” in Proc. IEEE International Conference on Computer Design, Oct. 1988, pp. 40-42.

[Cav88b] J. R. Cavallaro, and F. T. Luk, “CORDIC Arithmetic for a SVD processor,” Journal of Parallel and Distributed Computing, Vol. 5, pp. 271-290, June 1988.

[CCI92] CCITT Recommendation O.153: "Basic Parameters for the Measurement of Error Performance at Bit Rates below the Primary Rate," Oct. 1992.

[Cha94] G. Chang, A. Rofougaran, M. Ku, A. A. Abidi, and H. Samueli, "A Low-Power CMOS Digitally Synthesized 0-13 MHz Agile Sinewave Generator," In Proc. Int. Solid-State Circuits Conf., Feb. 1994, pp. 32-33.

[Che82] P. R. Chevillat, and G. Ungerboeck, “Optimum FIR Transmitter and Receiver Filters for Data Transmission over Band-Limited Channels,” IEEE Trans. Commun., Vol. 30, No. 8, pp. 1909-1915, Aug. 1982.

[Che92] B. W. Cheney, D. C. Larson and A. M. Frisch, "Delay Equalization Emulation for High Speed Phase Modulated Direct Digital Synthesis," U. S. Patent 5,140,540, Aug. 18, 1992.

[Che95] A. Chen, R. McDanell, M. Boytim, and R. Pogue, "Modified CORDIC demodulator implementation for digital IF-sampled receiver," in Proc. GLOBECOM '95, Singapore, Nov. 1995, pp. 1450 -1454.

[Chi94] S. Y. Chin, and C. Y. Wu, "A 10-bit 125-MHz CMOS Digital-to-Analog Converter (DAC) with Threshold-Voltage Compensated Current Sources," IEEE J. of Solid State Circuits, Vol. 29, No. 11, pp. 1374-1380, Nov. 1994.

[Cho88] J. Chow, F. F. Lee, P. M. Lau, C. G. Ekroot, and J. E. Hornung, "1.25 GHz 26-bit Pipelined Digital Accumulator", 1988 GaAs IC Symp. Technical Digest, Nov. 1988, pp. 131-134.

[Cho99] K. H. Cho, J. Putnam, and H. Samueli, "A VLSI Architecture for a Frequency-Agile Single-Chip 10-Mbaud Digital QAM Modulator," Proc. Globecom'99, Dec. 1999, pp. 168-172.

[Cho00] K. H. Cho, and H. Samueli, "A 8.75-Mbaud Single-Chip Digital QAM Modulator with Frequency-Agility and Beamforming Diversity," in Proc. IEEE Custom Integrated Circuits Conf., 2000, pp. 27-30.

[Chr95] W. A. Chren, Jr., "RNS-Based Enhancements for Direct Digital Frequency Synthesis," IEEE Trans. Circuits Syst. - Analog and Digital Signal Processing, Vol. CAS-42, No. 8, pp. 516-524, Aug. 1995.

[Chu81] F. E. Churchill, G. W. Ogar and B. J. Thompson, "The Correction of I and Q Errors in a Coherent Processor," IEEE Trans. AES, Vol. AES-17, No. 1, pp. 131-136 Jan. 1981.

[Coc92] D. Cochran, "Algorithms and Accuracy in the HP-35," Hewlett-Packard Journal, pp. 10-11, Jun. 1992.

[Cra94] J. A. Crawford, "Frequency Synthesizer Design Handbook," Artech House, 1994.

[Cro83] R. E. Crochiere, and L. R. Rabiner, "Multirate Digital Signal Processing," Englewood Cliffs, NJ: Prentice-Hall, 1983.

[Dac98] M. Dachroth, B. Hoppe, H. Meuth, and U. W. Steiger, ”High-Speed Architecture and Hardware Implementation of a 16-bit 100 MHz Numerically Controlled Oscillator,” in Proc. ESSCIRC’98, Sept. 1998, pp. 456-459.

[Daw96] H. Dawid, and H. Meyr, “The Differential CORDIC Algorithm: Constant Scale Factor Redundant Implementation without Correcting Iterations,” IEEE Trans. on Computers, Vol. 45, No.3, pp. 307-318, Mar. 1996.

[Duh95] M. Duhalde, and A. Greiner, “A High Performance Modular Embedded ROM Architecture,” in Proc. ISCAS95, Seattle, WA, May 1995, pp. 1057-1060.

[Dup90] S. Dupuie, and M. Ismail, “High Frequency CMOS Transconductors,” In: C. Toumazou, F. Lidgey, D. Haigh (ed.), Analogue IC Design: The Current-Mode Approach, Peter Peregnirus Ltd on the behalf of IEE: London, UK, 1990, pp. 181-238 (Chapter 5).

[Dup93] J. Duprat, and J. M. Muller, “The CORDIC Algorithm: New Results for Fast VLSI Implementation,” IEEE Trans. on Computers, Vol. 42, No. 2, pp. 168-178, Feb. 1993.

[Dur87] R. A. Duryea, and C. Pottle, “Finite Precision Arithmetic Units in Jacobi SVD Architectures,” School of Electrical Engineering, Cornell University, Ithacaa, NY, Technical Report EE-CEG-87-11, Mar. 1987.

[Dut78] D. L. Duttweiler, and D. G. Messerschmitt “Analysis of Digitally Generated Sinusoids with Application to A/D and D/A Converter Testing,” IEEE Trans. on Commun., Vol. COM-26, pp. 669-675, May 1978.

[Ekr88] C. G. Ekroot, and S. I. Long, "A GaAs 4-b Adder-Accumulator Circuit for Direct Digital Synthesis", IEEE J. Solid-State Circuits, Vol. 23, pp. 573-580, April 1988.

[End93] T. J. Endres, G. T. Calvetti, and J. B. Kirkpatrick, "Induced End-of-Life Errors in a Fast Settling PLL", in Proc. IEEE Int. Frequency Cont. Symp., June 1993, pp. 261-269.

[End94] T. J. Endres, R. B. Hall, and A. M. Lopez, "Design and Analysis Methods of a DDS-based Synthesizer for Military Spaceborne Applications," in Proc. IEEE Int. Frequency Cont. Symp., June 1994, pp. 624-632.

[Erc88] M. D. Ercegovac, and T. Lang, “Implementation of Fast Angle Calculation and Rotation Using On-Line CORDIC,” in Proc. IEEE International Symposium on Circuits and Systems (ISCAS), June 1988, pp. 2,703-2,706.

[Erc90] M. D. Ercegovac, and T. Lang, “Redundant and On-Line CORDIC Application to Matrix Triangularization and SVD,” IEEE Trans. on Computers, Vol. 38, No. 6, pp. 725-740, June 1990.

[Eru93] L. Erup, F. M. Gardner, and R. A. Harris, ”Interpolation in Digital Modems–Part II: Implementation and Performance,” IEEE Trans. on Commun., Vol. COM-41, pp. 998-1008, June 1993.

[Ert96] R. Ertl, and J. Baier, “Increasing the Frequency Resolution of NCO-Systems Using a Circuit Based on a Digital Adder,” IEEE Trans. Circuits and Systems II, Vol. 43, No. 3, pp. 266 - 269, Mar. 1996.

[ETSI98] The ETSI UMTS Terrestrial Access (UTRA) ITU-R RTT Candidate Submission, SMG2 260/98, July 1998.

[Far88] C. W. Farrow, ”A Continuosly Variable Digital Delay Element,” in Proc. IEEE International Symposium on Circuits and Systems (ISCAS), June 1988, pp. 2641-2645.

[Fau91] M. Faulkner, T. Mattsson, and W. Yates, "Automatic Adjustment of Quadrature Modulators," Electron. Lett., Vol. 27, No.3, pp. 214-216, Jan. 1991.

[Fla93] M. J. Flanagan, and G. A. Zimmerman, "Spur-Reduced Digital Sinusoid Generation Using Higher-Order Phase Dithering," Asilomar Conf. on Signals, Syst. and Comput., Nov. 1993, pp. 826-830.

[Fla95] M. J. Flanagan, and G. A. Zimmerman, "Spur-Reduced Digital Sinusoid Synthesis," IEEE Trans. Commun., Vol. COM-43, pp. 2254-2262, July 1995.

[Fli92] N. J. Fliege, and J. Wintermantel, “Complex Digital Oscillators and FSK Modulators,” IEEE Trans. on Signal Processing, Vol. SP-40, No. 2, pp. 333-342, Feb. 1992.

[Fre95] S. Freeman, and M. O’Donnell, ”A Complex Arithmetic Digital Signal Processor Using Cordic Rotators”, in Proc. ICASSP-95, Vol. 5, pp. 3191-3194, May 1995.

[Fur75] K. Furuno, S. K. Mitra, K. Hirano, and Y. Ito, “Design of Digital Sinusoidal Oscillators with Absolute Periodicity,” IEEE Trans. on Aerospace and Electronic Systems, Vol. AES-11, No. 6, pp. 1286-1298, Nov. 1975.

[Gar79] F. M. Gardner, "Phaselock Techniques," 2nd Edition, New York: John Wiley and Sons, Inc., 1979.

[Gar91] R. A. Garcia, "Digital Data and Analog Radio Frequency Transmitter," U. S. Patent 5,010,585, Apr. 23, 1991.

[GEC93] GEC-Plessey Semiconductors, Data Sheet PDSP16350 I/Q Splitter/NCO, Dec. 1993.

[Gie89] B. Giebel, J. Lutz, and P. L. O’Leary, "Digitally Controlled Oscillator", IEEE J. Solid-State Circuits, Vol. 24, pp. 640-645, June 1989.

[Gie91] G. Gielis, R. van de Plassche, and J. van Valburg, "A 540 MHz 10b Polar-to-Cartesian Converter," ISSCC Digest of Technical Papers, Feb. 1991, pp. 160-161.

[Gil90a] R. Gilmore, and R. Kornfeld, "Hybrid PLL/DDS Frequency Synthesizers," in Proc. RF Techn. EXPO, Mar. 1990, pp. 419-436.

[Gil90b] R. P. Gilmore, "Direct Digital Frequency Synthesizer Driven Phase Lock Loop Frequency Synthesizer," U. S. Patent 4,965,533, Oct. 23, 1990.

[Gil92] R. P. Gilmore, "Direct Digital Synthesizer/Direct Analog Synthesizer Hybrid Frequency Synthesizer," U. S. Patent 5,128,623, Jul. 7, 1992.

[Gol69] B. Gold, and C. M. Rader, “Digital Processing of Signals,” New York: McGraw-Hill, 1969.

[Gol88] B. G. Goldberg, "Digital Frequency Synthesizer," U. S. Patent 4,752,902, June 21, 1988.

[Gol90] B. G. Goldberg, "Digital Frequency Synthesizer Having Multiple Processing Paths," U. S. Patent 4,958,310, Sep. 18, 1990.

[Gol96] B. G. Goldberg, "Digital Techniques in Frequency Synthesis," McGraw-Hill, 1996.

[GPP99] 3rd Generation Partnership Project (3GPP) Technical Specification Group (TSG) RAN WG4 UTRA (BS) FDD: ”Radio Transmission and Reception,” S 4.01B v1.0.1, Apr. 1999.

[Gra88] J. Grandfield, et al., "Direct Frequency Synthesizer," U. S. Patent 4,791,377, Dec. 13, 1988.

[Gra93] R. M. Gray, and T. G. Stockholm, "Dithered Quantizers," IEEE Trans. Inform. Theory., Vol. 39, pp. 805-812, May 1993.

[Gro89] D. W. J. Groeneveld, H. J. Schouwenaars, H. A. H. Termeer, and C. A. A. Bastiaansen, “A Self-Calibration Technique for Monolithic High-Resolution D/A Converters,” IEEE J. Solid-State Circuits, Vol. 24, No. 6, pp. 1517 -1522, Dec. 1989.

[GSM92] GSM Recommendation 05.04: "Modulation," Feb. 1992.

[GSM96a] GSM Recommendation 05.10: "Digital Cellular Telecommunications System (Phase 2+); Radio Subsystem Synchronisation," May 1996.

[GSM96b] GSM Recommendation 05.02: "Digital Cellular Telecommunications System (Phase 2+); Multiplexing and Multiple Access on the Radio Path," Aug. 1996.

[GSM96d] GSM Recommendation 11.21: "Digital Cellular Telecommunications System (Phase 2); Base Station System (BSS) Equipment Specification; Part 1: Radio Aspects," Nov. 1996.

[GSM98] GSM Recommendation 05.05: "Radio Transmission and Reception," Dec. 1998.

[Har91] M. V. Harris, "A J-Band Spread-Spectrum Synthesiser Using a Combination of DDS and Phaselock Techniques," IEE Coll. Digest 1991/172 on Direct Digital Frequency Synthesis, Nov. 1991, pp. 8/1-10.

[Har96] R. I. Hartley, ”Subexpression Sharing in Filters Using Canonic Signed Digit Multipliers,” IEEE Trans. Circuits and Systems II, Vol. 43, No. 10, pp. 677 -688, Oct. 1996.

[Hav80] G. L. Haviland, and A. A. Tuszynski, “A CORDIC Arithmetic Processor Chip,” IEEE Trans. on Computers, Vol. 29, No. 2, pp. 68-79, Feb. 1980.

[Haw96] R. A. Hawley et al., ”Design Techniques for Silicon Compiler Implementations of High-Speed FIR Digital Filters,” IEEE J. of Solid State Circuits, Vol. 31, No. 5, pp. 656-667, May 1996.

[Hen97] P. Hendriks, “Specifying Communications DAC’s,” IEEE Spectrum, Vol. 34, pp. 58-69, July 1997.

[Hie92] A. W. Hietala, et al., "Digital Frequency Synthesizer Having AFC and Modulation Applied to Frequency Divider," U. S. Patent 5,111,162, May 5, 1992.

[Hir94] M. Hirata, and O. Yamamoto, "Radio Transmitter," U. S. Patent 5,353,311, Oct. 4, 1994.

[Hog81] E. B. Hogenauer, “An Economial Class of Digital Filters for Decimation and Interpolation,” IEEE Trans. Acoust., Speech, Signal Process., Vol. ASSP-29, No. 2, pp. 155-162, Apr. 1981.

[Hsi95] S. F. Hsiao, and J. M. Delosme, ”Householder CORDIC Algorithms,” IEEE Trans. Comput., Vol. 44, No. 8, pp. 990-1001, Aug. 1995.

[Hu92a] Y. H. Hu, "The Quantization Effects of the CORDIC Algorithm," IEEE Trans. Signal Processing, Vol. 40, No. 4, pp. 834-844, April 1992.

[Hu92b] H. Y. Hu, "CORDIC-Based VLSI Architectures for Digital Signal Processing," IEEE Signal Processing Magazine, pp. 16-35, July 1992.

[Hut75] B. H. Hutchison, Jr., "Frequency Synthesis and Applications," IEEE Press, New York, NY, USA, 1975.

[Ito93] K. Itoh, et al., "Frequency Synthesizer," U. S. Patent 5,184,093, Feb. 2, 1993.

[Jac73] L. B. Jackson, "Digital Frequency Synthesizer," U. S. Patent 3,735,269, May 22, 1973.

[Jas87] S. C. Jasper, "Frequency Resolution in a Digital Oscillator," U. S. Pat. 4,652,832, Mar. 24, 1987.

[Jen88a] Y. C. Jenq, "Digital Spectra of Nonuniformly Sampled Signals: Fundamentals and High-Speed Waveform Digitizers," IEEE Trans. Inst. and Meas., Vol. 37, pp. 245-251, June 1988.

[Jen88b] Y. C. Jenq, "Digital Spectra of Nonuniformly Sampled Signals - Digital Look-Up Tunable Sinusoidal Oscillators," IEEE Trans. on Inst. and Meas., Vol. 37, No. 3, pp. 358-362, Sept. 1988.

[Jia97] Z. Jiang, and A. N. Willson, ”Efficient Digital Filtering Architectures Using Pipelining/Interleaving,” IEEE Trans. Circuits Systems II, Vol. 44, No. 2, pp. 110-119, Feb. 1997.

[Jon91] A. E. Jones, and J. G. Gardiner, "Phase Error Correcting Vector Modulator for Personal Communications Network (PCN) Transceivers," Electron. Lett., Vol. 27, No. 14, pp 1230-1231, July 1991.

[Jon92] A. E. Jones, and J. G. Gardiner, "Generation of GMSK Using Direct Digital Synthesis," IEE Colloquium on 'Implementations of Novel Hardware for Radio Systems', London UK 1992, pp. 4/1-9.

[Kel73] G. Kelson, H. Stellrecht, and D. Perloff, "A Monolithic 10-b Digital-to-Analog Converter Using Ion Implantation”, IEEE J. Solid-State Circuits, Vol. 8, No. 6, pp. 396-403, Dec. 1973.

[Ker90] R. J. Kerr, and L. A. Weaver, "Pseudorandom Dither for Frequency Synthesis Noise," U. S. Pat. 4,901,265, Feb. 13, 1990.

[Kha99] K. Khanoyan, F. Behbahani, and A. Abidi, “A 10b, 400 MS/s Glitch-Free CMOS D/A Converter,” in 1999 Symp. VLSI Circuits Dig. Tech. Papers, pp. 73-76.

[Kol98] K. Koli, and K. Halonen, "Current-mode temperature compensated continuous-time CMOS transconductance-C filter", Analog Integrated Circuits and Signal Processing, 15 (1), pp. 59-69, Jan. 1998.

[Kop87] A. Kopta, S. Budisin, and V. Jovanovic, "New Universal All-Digital CPM Modulator," IEEE Trans. on Commun., Vol. COM-35, pp. 458-462, April 1987.

[Kos98] M. Kosunen, K. Koli, and K. Halonen, “A 50 MHz 5^{th} Order Elliptic LP-filter Using Current mode Gm-C Topology”, in Proc. ISCAS98, Monterey, CA, USA, June 1998, pp. 512-515.

[Kot93] K. Kota, and J. R. Cavallaro, “Numerical Accuracy and Hardware Tradeoffs for CORDIC Arithmetic for Special-Purpose Processors,” IEEE Trans. Comput., Vol. 42, No. 7, pp. 769-779, July 1993.

[Kou93] C. S. Koukourlis, P. H. Houlis, and J. N. Sahalos, "A General Purpose Differential Digital Modulator Implementation Incorporating a Direct Digital Synthesis Method," IEEE Trans. on Broadc., Vol. 39, pp. 383-389, Dec. 1993.

[Kun90] H. Kunemund, S. Soldner, S. Wohlleben, and T. Noll, “CORDIC Processor with Carry Save Architecture,” in Proc. ESSCIRC’90, Sep. 1990, pp.193-196.

[Kur84] C. N. Kurby, "Radio-Frequency Synthesizer for Duplex Radios," U. S. Patent 4,449,250, May. 15, 1984.

[Lan88] A. A. de Lange, A. J. van der Hoeven, E. F. Deprettere, and J. Bu, “An Optimal Floating-Point Pipeline CMOS CORDIC Processor,” in Proc. IEEE International Symposium on Circuits and Systems (ISCAS), June 1988, pp. 2,043-2,047.

[Laz94] G. Lazzari, F. Maloberti, G. Oliveri, and G. Torelli, "Sinewave Modulation for Data Communication by Direct Digital Synthesis and Sigma Delta Techniques," European Trans. Telecommun. and Related Technologies, Vol. 5, pp. 689-695, Nov.-Dec. 1994.

[Lea91a] P. O' Leary, M. Pauritsch, F. Maloberti, and G. Raschetti, "An oversampling-based DTMF generator," IEEE Trans. Commun., Vol. COM-39, pp. 1189-1191, Aug. 1991.

[Lea91b] P. O' Leary, and F. Maloberti, "A Direct Digital Synthesizer with Improved Spectral Performance," IEEE Trans. Commun., Vol. COM-39, pp. 1046-1048, July 1991.

[Lee66] D. B. Leeson, “A Simple Model of Feedback Oscillator Noise Spectrum,” IEEE Proc., Vol. 54, pp. 329-330, Feb. 1966.

[Lee89] J. Lee, and T. Lang, “On-Line CORDIC for Generalized Singular Value Decomposition,” SPIE High Speed Computing II Vol 1058, pp.235-247, 1989.

[Lee92] J. Lee, and T. Lang, "Constant-Factor Redundant CORDIC for Angle Calculation and Rotation," IEEE Trans. Comput., Vol. 41, No. 8, pp. 1016-1025, Aug. 1992.

[Lee93] S-S Lee, R. H. Zele D. J. Allstot, and G. Liang, “CMOS Continuous-Time Current-Mode Filters for High-Frequency Applications,” IEEE J. of Solid-State Circuits, Vol. 28, No. 3, pp. 323-329, Mar. 1993.

[Lia97] S. Liao, and L-G. Chen, "A Low-Power Low-Voltage Direct Digital Frequency Synthesizer," in Proc. Int. Symp. on VLSI Technology, Systems, and Applications, Hsinchu, Taiwan, June 1997, pp. 265-269.

[Lin90] H. X. Lin, and H. J. Sips, “On-Line CORDIC Algorithms,” IEEE Trans. on Computers, Vol. 38, No. 8, pp. 1,038-1,052, Aug. 1990.

[Lin98] C. Lin, and K. Bult, “A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2,” IEEE J. Solid-State Circuits, Vol. 33, No. 12, pp. 1948-1958, Dec. 1998.

[Lin96] A. Linz, and A. Hendrickson, ”Efficient Implementation of an I-Q GMSK Modulator,” IEEE Trans. Circuits and Systems II, Vol. 43, No. 1, pp. 14 - 23, Jan. 1996.

[Lip92] S. P. Lipshitz, R. A. Wannamaker, and J. Vanderkooy, ”Quantization and Dither: A Theoretical Survey,” J. Audio Eng. Soc., Vol. 40, No. 5, pp. 355-374, May 1992.

[Lju87] L. Ljung, ”System Identification: Theory for the User,” Englewood Cliffs, NJ: Prentice-Hall, 1987.

[Lu93] F. Lu, H. Samueli, J. Yuan, and C. Svensson, "A 700-MHz 24-b Pipelined Accumulator in 1.2 μm CMOS for Application as a Numerically Controlled Oscillator", IEEE J. Solid-State Circuits, Vol. 26, pp. 878-885, Aug. 1993.

[Lun99] L. J. D’Luna, et. al, “A Single Chip Universal Cable Set-Top Box/Modem Transceiver,” IEEE J. Solid-State Circuits, Vol. 34, No. 11, pp. 1647-1660, Nov. 1999.

[Mad99] A. Madisetti, A. Kwentus, and A. N. Wilson, Jr., "A 100-MHz, 16-b, direct digital frequency synthesizer with a 100-dBc spurious-free dynamic range," IEEE J. of Solid State Circuits, Vol. 34, No. 8, pp. 1034-1044, Jan. 1999.

[Mag94] D. T. Magill, F. D. Natali, and G. P. Edwards, “Spread-Spectrum Technology for Commercial Applications,” Proceedings of the IEEE, Apr. 1994, pp. 572-584.

[Man87] V. Manassewitsch, Frequency Synthesizers Theory and Design, 3nd Edition, New York: Wiley, 1980.

[McC84] R. D. McCallister, and D. Shearer, III, "Numerically Controlled Oscillator Using Quadrant Replication and Function Decomposition," U. S. Patent 4,486,846, Dec. 4, 1984.

[McC79] J. H. McClellan, and C. M. Rader, “Number Theory in Digital Signal Processing,” Englewood Cliffs, NJ: Prentice-Hall, 1979.

[McC88] E. W. McCune, Jr., "Number Controlled Modulated Oscillator," U. S. Patent 4,746,880, May 24, 1988.

[McC91a] E. McCune Jr., "Create Signals Having Optimum Resolution, Response, and Noise", EDN, pp. 95-108, Mar. 1991.

[McC91b] E. W. McCune, Jr., "Variable Modulus Digital Synthesizer," U. S. Patent 5,053,982, Oct. 1, 1991.

[Meh83] S. Mehrgardt, "Noise Spectra of Digital Sine-Generators Using the Table-Lookup Method," IEEE Trans. Acoust., Speech, Signal Process., Vol. ASSP-33, No. 4, pp. 1037-1039, Aug. 1983.

[Mer94] D. Mercer, “A 16-b D/A Converter with Increased Spurious Free Dynamic Range,” IEEE J. Solid-State Circuits, Vol. 29, No. 10, pp. 1180–1185, Oct. 1994.

[Mey98] U. Meyer-Bäse, S. Wolf, and F. Taylor, “Accumulator-Synthesizer with Error-Compensation,” IEEE Trans. Circuits and Systems II, Vol. 45, No. 7, pp. 885 - 890, July 1998.

[Mol95] F.T Moller, et. al, “PSEUDEC: Implementation of the Computation-intensive PARTRAN Functionality Using a Dedicated on-line CORDIC Co-processor,” in Proc. ICASSP-95, Vol. 5, May 1995, pp. 3207 –3210.

[Mor99] S. Mortezapour, and E. K. F. Lee, ”Design of Low-Power ROM-Less Direct Digital Frequency Synthesizer Using Nonlinear Digital-to Analog Converter,” IEEE J. Solid-State Circuits, Vol. 34, No. 10, pp. 1350-1359, Oct. 1999.

[Mou92] M. Mouly, and M. B. Pautet, "The GSM System for Mobile Communications," Palaiseau Mouly & Pautet, Jan. 1992.

[Moy99] M. Moyal, M. Groepl, and T. Blon, “A 25-kft, 768-kb/s CMOS Analog Front End for Multiple-Bit-Rate DSL Transceiver,” in ISSCC Dig. Tech. Papers, 1999, pp. 244-245.

[Mur81] K. Murota, and K. Hirade, ”GMSK Modulation for Digital Mobile Radio Telephony,” IEEE Trans. Commun., Vol. 29, pp. 1044-1050, July 1981.

[Nak97] T. Nakagawa, H. Nosaka, “A Direct Digital Synthesizer with Interpolation Circuits,” IEEE J. of Solid State Circuits, Vol. 32, No. 5, pp. 766-770, May 1997.

[Nic87] H. T. Nicholas, and H. Samueli, "An Analysis of the Output Spectrum of Direct Digital Frequency Synthesizers in the Presence of Phase-Accumulator Truncation," in Proc. 41st Annu. Frequency Contr. Symp., June 1987, pp. 495-502.

[Nic88] H. T. Nicholas, H. Samueli, and B. Kim, "The Optimization of Direct Digital Frequency Synthesizer in the Presence of Finite Word Length Effects Performance," in Proc. 42nd Annu. Frequency Contr. Symp., June 1988, pp. 357-363.

[Nic91] H. T. Nicholas, and H. Samueli, "A 150-MHz Direct Digital Frequency Synthesiser in 1.25-µm CMOS with -90-dBc Spurious Performance," IEEE J. Solid-State Circuits, Vol. 26, pp. 1959-1969, Dec. 1991.

[NiB94] H. T. Nicholas, and H. Samueli, "A 150-MHz Direct Digital Frequency Synthesiser in 1.25-µm CMOS with -90-dBc Spurious Performance", IEEE J. Solid-State Circuits, vol. 26, pp. 1959-1969, Dec. 1991, and Burr-Brown data sheet DAC600, Data Conversion Products, 1994.

[Nie98] J. Nieznanski, “An alternative approach to the ROM-less direct digital synthesis,” IEEE J. of Solid State Circuits, Vol. 33, No. 1, pp. 169 -170, Jan. 1998.

[Nol90] T. Noll, “Carry-Save Arithmetic for High-Speed Digital Signal Processing,” in Proc. IEEE International Symposium on Circuits and Systems (ISCAS), Vol. 2, May 1990, pp. 982-986.

[Nol91] T. Noll, “Carry-Save Architectures for High-Speed Digital Signal Processing,” Journal of VLSI Signal Processing, Vol. 3, pp. 121-140, June 1991.

[Not88] S. Note, J. van Meerbergen, Catthoor, and H. de Man, “Automated Synthesis of a High Speed CORDIC Algorithm with the Cathedral-III Compilation System,” in Proc. IEEE International Symposium on Circuits and Systems (ISCAS), June 1988, pp. 581-584.

[Nuy90] P. Nuytkens, and P. V. Broekhoven, "Digital frequency synthesizer," U. S. Pat. 4,933,890, June 12, 1990.

[Opp75] A. V. Oppenheim, and R. W. Schafer, "Digital Signal Processing," Prentice-Hall, Englewood Cliffs, New Jersey, 1975.

[Ota96] S. Otaka et al., “A Low Local Input 1.9 GHz Si-Bipolar Quadrature Modulator with No Adjustment,” IEEE J. of Solid State Circuits, Vol. 31, No. 1, pp. 30-37, Jan. 1996.

[Par93] B. Parhami, “On the Implementation of Arithmetic Support Functions for Generalized Signed-Digit Number Systems,” IEEE Trans. on Computers, Vol. 42, No. 3, pp. 379-384, Mar. 1993.

[Par00] M. Park, K. Kim, and J. A. Lee, “CORDIC-Based Direct Digital Synthesizer: Comparison with a ROM-Based Architecture in FPGA Implementation,” IEICE Trans. Fundam., Vol. E83-A, No. 6 June 2000.

[Pel89] M. Pelgrom, A. Duinmaijer, and A. Webers, “Matching Properties of MOS Transistors,” IEEE J. Solid-State Circuits, Vol. 24, No. 5, pp. 1433-1440, Oct. 1989.

[Per93] M. Perez, and A. Fernandez, "A Contribution to DECT in Frequency Synthesis and Modulation Using DDS", in Proc. IEEE Vehicular Techn. Conf., May 1993, pp. 949-952.

[Phi95] L. Philips, I. Bolsens, and H. D. Man, “A Programmable CDMA IF Transceiver ASIC for Wireless Communications,” in Proc. IEEE Custom Integrated Circuits Conf., 1995, pp. 307-310.

[Pla99] G. A. M. Van der Plas, J. Vandenbussche, W. Sansen, M. S. J. Steyaert, and G. G. E. Gielen, “A 14-bit Intrinsic Accuracy Q^2 Random Walk CMOS DAC,” IEEE J. Solid-State Circuits, Vol. 34, No. 12, pp. 1708 -1718, Dec. 1999.

[QuS91] Qualcomm Q2334 Technical Data Sheet, June 1991, and Sony CX20201A-1 data sheet, Jan. 1990.

[Qua90] Qualcomm, "Hybrid PLL/DDS Frequency Synthesiser," AN2334-4, 1990.

[Qua91a] Qualcomm Q2334, Technical Data Sheet, June 1991.

[Ram84] T. A. Ramstad, ”Digital Methods for Conversion Between Arbitrary Sampling Frequencies,” IEEE Trans. Acoust., Speech, Signal Process., Vol. ASSP-32, No. 3, pp. 577-591, June 1984.

[Ray94] Raytheon Semiconductor Data Book, Data Sheet TMC2340, 1994.

[Rei85] V. S. Reinhardt, "Direct Digital Synthesizers," in Proc. 17th Annual Precise Time and Time Interval Applications and Planning Meeting (NASA/DOD), Washington, D.C., Dec. 1985.

[Rei91] V. S. Reinhardt et al., "Randomized Digital/Analog Converter Direct Digital Synthesiser," U. S. Pat. 5,014,231, May 7, 1991.

[Rei93] V. S. Reinhardt, "Spur Reduction Techniques in Direct Digital Synthesizers," in Proc. IEEE Int. Frequency Cont. Symp., June 1993, pp. 230-241.

[Rof98] A. Rofougaran, G. Chang, J. J. Rael, J. Y.-C. Chang, M. Rofougaran, P. J. Chang, M. Djafari, M-K. Ku, E. W. Roth, A. A. Abidi, and H. Samueli, “A Single-Chip 900-MHz Spread-Spectrum Wireless Transceiver in 1-µm CMOS—Part I: Architecture and Transmitter Design,” IEEE J. of Solid State Circuits, Vol. 33, No. 4, pp. 515-534, Apr. 1998.

[Rog96] R. Rogenmoser, and Q. Huang, “A 800-MHz 1-µm CMOS Pipelined 8-b Adder Using True Single-Phase Clocked Logic-Flip-Flops,” IEEE J. of Solid State Circuits, Vol. 31, No. 3, pp. 401-409, Mar. 1996.

[Roh83] U. L. Rohde, Digital PLL Frequency Synthesizers Theory and Design, Prentice-Hall Inc., 1983.

[Roo89] S. J. Roome, "Analysis of Quadrature Detectors Using Complex Envelope Notation", IEE Proc. F, Vol. 136, No. 2, pp. 95-100, April 1989.

[Rub89] P. W. Ruben, E. F. Heimbecher, II, and D. L. Dilley, "Reduced Size Phase-to-Amplitude Converter in a Numerically Controlled Oscillator," U. S. Patent 4,855,946, Aug. 8, 1989.

[SaA94] P. H. Saul, and M. S. J. Mudd, "A Direct Digital Synthesizer with 100-MHz Output Capability," IEEE J. Solid-State Circuits, Vol. 23, pp. 819-821, June 1988, and Analog Devices AD 9720 data sheet, Rev. 0, 1994.

[Sam88] H. Samueli, “The Design of Multiplierless FIR Filters for Compensating D/A Converter Frequency Response Distortion,” IEEE Trans. Circuits and Syst., Vol. 35, No. 8, pp. 1064-1066, Aug. 1988.

[Sam89] H. Samueli, “An Improved Search Algorithm for the Design of Multiplierless FIR Filters with Powers-of-Two Coefficients,” IEEE Trans. Circuits and Syst., Vol. 36, No. 7, pp. 1044-1047, July 1989.

[Sar98] R. Sarmiento, et al., “A CORDIC Processor for FFT Computation and Its Implementation Using Gallium Arsenide Technology,” IEEE Trans. on VLSI Systems, Vol. 6, No. 1, pp. 18-30, Mar. 1998.

[Sau90] P. H. Saul, and D. G. Taylor, "A High-Speed Direct Frequency Synthesizer," IEEE J. Solid-State Circuits, Vol. 25, No. 1, pp. 215-219, Feb. 1990.

[Sau91] P. H. Saul, "Technological Limitations in Direct Digital Synthesis," IEE Coll. Digest 1991/172 on Direct Digital Frequency Synthesis, Nov. 1991, pp. 3/1-5.

[Sau93] P. Saul, and T. Coffey, "Current Achievements in Direct Digital Synthesis", Microwave Eng. Europe, pp. 31-36, Dec./Jan. 1993.

[Sch86] G. Schmidt, D. Timmermann, J. F. Bohme, and H. Hahn, “Parameter Optimization of the CORDIC Algorithm and Implementation in a CMOS Chip,” in Proc. European Signal Processing Conference (EUSIPCO), Sep. 1986, pp. 1,291-1,222.

[Sci94] Sciteq Electronics ADS-431, Frequency Synthesizers & RF Engineering, pp. 24, 1994.

[Sek94] K. Seki, T. Sakata and S. Kato, "A Digitalized Quadrature Modulator for Fast Frequency Hopping," IEICE Trans. Commun., Vol. E77-B, No. 5 May 1994.

[Sta94] Stanford Telecom STEL-2173 Data Sheet, the DDS Handbook, Fourth Edition, and Triquint Semiconductor TQ6122 Data Sheet, TQS Digital Communications and Signal Processing, 1994.

[Ste97] M. S. J. Steyaert, V. Peluso, J. Bastos, P. Kinget, and W. Sansen, “Custom Analog Low Power Design: the Problem of Low Voltage and Mismatch,” in Proc. IEEE Custom Integrated Circuits Conf., 1997, pp. 285-292.

[Su93] D. K. Su, M. J. Loinaz, S. Masui, and B. A. H. Wooley, “Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits”, IEEE J. Solid-State Circuits, Vol. 28, No. 4, pp. 420-429, April 1993.

[Sun84] D. A. Sunderland, R. A. Strauch, S.S. Wharfield, H. T. Peterson, and C. R. Cole, "CMOS/SOS Frequency Synthesizer LSI Circuit for Spread Spectrum Communications," IEEE J. of Solid State Circuits, Vol. SC-19, pp. 497-505, Aug. 1984.

[Suz82] H. Suzuki, and Y. Yamao, "Design of Quadrature Modulator for Digital FM Signalling with Digital Signal Processing," Electron. & Commun. in Japan, Vol. 65-B, No. 9, pp. 66-73, Sept. 1982.

[Suz84] H. Suzuki, Y. Yamao, and K. Momma, "Single-Chip Baseband Waveform Generator CMOS-LSI for Quadrature-type GMSK Modulator," Electron. Lett., Vol. 20, pp. 875-876, Oct. 1984.

[Tak87] N. Takagi, T. Asada, and S. A. Yajima, “Hardware Algorithm for Computing Sine and Cosine using Redundant Binary Representation,” Systems and Computers in Japan, Vol. 18, No. 9, pp. 1-9, 1987.

[Tak91] N. Takagi, T. Asada, and S. A. Yajima, “Redundant CORDIC Methods with a Constant Scale Factor for a Sine and Cosine Computation,” IEEE Trans. on Computers, Vol. 40, No. 9, pp. 989-995, Sep. 1991.

[Tan95a] L. K. Tan, E. W. Roth, G. E. Yee, and H. Samueli, "A 800 MHz Quadrature Digital Synthesizer with ECL-Compatible Output Drivers in 0.8 μm CMOS," IEEE J. of Solid State Circuits, Vol. 30, No. 12, pp. 1463-1473, Dec. 1995.

[Tan95b] L. K. Tan, and H. Samueli, "A 200 MHz Quadrature Digital Synthesizer/Mixer in 0.8 μm CMOS," IEEE J. of Solid State Circuits, Vol. 30, No. 3, pp. 193-200, Mar. 1995.

[Tes97] B. Tesch, and J. Garcia, “A Low Glitch 14-b 100-MHz D/A Converter,” IEEE J. Solid-State Circuits, Vol. 32, No. 9, pp. 1465 -1469, Sept. 1997.

[Tho92] M. Thompson, "Low-Latency, High-Speed Numerically Controlled Oscillator Using Progression-of-States Technique," IEEE J. Solid-State Circuits, Vol. 27, pp. 113-117, Jan. 1992.

[TIA93] TIA/EIA Interim Standard, “Mobile Station-Base Station Compatibility Standard for Dual-Mode Wideband Spread Spectrum Cellular System, TIA/EIA/IS-95,” July 1993.

[Tie71] J. Tierney, C. Rader, and B. Gold "A Digital Frequency Synthesizer," IEEE Trans. Audio and Electroacoust., Vol. AU-19, pp. 48-57, Mar. 1971.

[Tim91] D. Timmermann, H. Hahn, B. J. Hostica, and B. Rix, “A New Addition Scheme and Fast Scaling Factor Compensation Methods for CORDIC Algorithms,” INTEGRATION, the VLSI Journal, Vol. 11, pp. 85-100, 1991.

[Tri94] Triquint Semiconductors Inc., Data Sheet TQ6122, 1994.

[Twi94] E. R. Twitchell, and D. B. Talbot, "Apparatus for Reducing Spurious Frequency Components in the Output Signal of a Direct Digital Synthesizer," U. S. Pat. 5,291,428, Mar. 1, 1994.

[Uus00] R. Uusikartano, and J. Niittylahti, "A Compact Frequency Synthesizer for GSM IF Up/Downconverter," in Proc. ISCAS'2000 conference, May 28-31, 2000 Geneva, Switzerland, pp. III/113-115.

[Vai93] P.P. Vaidyanathan, "Multirate Systems and Filter Banks", Prentice-Hall, 1993.

[Vin94] R. I. Vinchentzio, "Cut DDS Images in Hopping SSB Mixer/modulator," Microwaves & RF, pp. 134-141, Mar. 1994.

[Voe68] H. B. Voelcker, "Generation of Digital Signaling Waveforms," IEEE Trans. on Commun. Tech., Vol. Com.-16, No. 1, pp. 81-93, Jan. 1968.

[Vol59] J. E. Volder, "The CORDIC Trigonometric Computing Technique," IRE Trans. on Electron. Comput., EC-8:330-334, Sept. 1959.

[Wal71] J. S. Walther, "A Unified Algorithm for Elementary Functions," in Proc. Spring Joint Computer Conference, May 1971, pp. 379-385.

[Wal97] M. Waltari, "Integration of a Direct Digital Synthesizer with BiCMOS Process," Master thesis, Helsinki University of Technology, Electronic Circuit Design Laboratory, Apr. 1997.

[Wea90a] L. A. Weaver, and R. J. Kerr, "High Resolution Phase To Sine Amplitude Conversion," U. S. Patent 4,905,177, Feb. 27, 1990.

[Wea90b] L. A. Weaver, "Synchronous Up-Conversion Direct Digital Synthesizer," U. S. Patent 4,926,130, May 15, 1990.

[Wen95] A. Wenzler, and E. Lüder, "New Structures for Complex Multipliers and their Noise Analysis," in Proc. IEEE International Symposium on Circuits and Systems (ISCAS), 1995, pp. 1,432-1,435.

[Whe83] C. E. Wheatley, III, "Digital Frequency Synthesiser with Random Jittering for Reducing Discrete Spectral Spurs," U. S. Pat. 4,410,954, Oct. 18, 1983.

[Wil91] M. P. Wilson, and T. C. Tozer, "Spurious Reduction Techniques for Direct Digital Synthesis," IEE Coll. Digest 1991/172 on Direct Digital Frequency Synthesis, Nov. 1991, pp. 4/1-4/5.

[Won91] B. C. Wong, and H. Samueli, “A 200-MHz All-Digital QAM Modulator and Demodulator in 1.2-µm CMOS for Digital Radio Applications,” IEEE J. Solid-State Circuits, Vol. 26, No. 12, pp. 1970-1979, Dec. 1991.

[Xil98] The Programmable Logic Data Book, Xilinx Inc., San Jose, Calif., 1998.

[Yam98] A. Yamagishi, M. Ishikawa, T. Tsukahara, and S. Date, “A 2-V, 2-GHz Low-Power Direct Digital Frequency Synthesizer Chip-Set for Wireless Communication,” IEEE J. of Solid State Circuits, Vol. 33, No. 2, pp. 210-217, Feb. 1998.

[Yos89] H. Yoshimura, T. Nakanishi, and H. Yamauchi, “A 50 MHz CMOS Geometrical Mapping Processor,” IEEE Trans. on Circuits and Systems, Vol. 36, No. 10, pp. 1,360-1,363, 1989.

[Yua89] J. Yuan, and C. Svensson, “High-Speed CMOS Circuit Technique,” IEEE J. of Solid State Circuits, Vol. 24, No. 1, pp. 62-70, Feb. 1989.

[Zav88a] R. J. Zavrel, Jr., "Digital Modulation Using the NCMO," RF Design, pp. 27-32, Mar. 1988.

[Zav88b] R. Zavrel, and E. W. McCune, "Low Spurious Techniques & Measurements for DDS Systems," in RF Expo East Proc., 1988, pp. 75-79.

[Zim92] G. A. Zimmerman, and M. J. Flanagan, "Spur Reduced Numerically-Controlled Oscillator for Digital Receivers," Asilomar Conf. on Signals, Syst. and Comput., Dec. 1992, pp. 517-520.

[Zve67] A. Zvever, “Handbook of Filter Synthesis,” John Wiley & Sons, New York, 1967.

Appendix A: Fourier Transform of DDS Output

The DDS output can be represented by

$$s(t) = \sum_{n=-\infty}^{\infty} v(nT_{clk})h(t - nT_{clk}), \tag{A.1}$$

where $T_{clk} = 1/f_{clk}$, $h(t) = 1$ for $0 \le t < T_{clk}$ and 0 otherwise. The function $h(t)$ represents the output sample-and-hold (see the D/A-converter stepped output in Figure 2.1). The sampled signal is represented by the waveform $v(t)$. From the sampling theorem, the Fourier transform of the sampled waveform is given by [Opp75]

$$F[v*(t)] = \frac{1}{T_{clk}} \sum_{n=-\infty}^{\infty} V(f - \frac{n}{T_{clk}}). \tag{A.2}$$

Since $v(t)$ is assumed to be periodic with some frequency f_{out}, it can be represented by its Fourier series as

$$V(f) = \sum_{m=-\infty}^{\infty} c_m \sigma(f - m\, f_{out}), \tag{A.3}$$

where f_{out} is the DDS fundamental output frequency, and

$$c_m = \int_{-T_{out}/2}^{T_{out}/2} v(t) e^{-j2\pi f_{out} mt}\, dt, \tag{A.4}$$

where $T_{out} = 1/f_{out}$. On substitution of (A.3) into (A.2), the Fourier representation is given by

$$F[v*(t)] = f_{clk} \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} c_m \sigma(f - n f_{clk} - m f_{out}). \tag{A.5}$$

The holding function simply appends a shaping function on $F[v^*(t)]$ and is given by

$$H(f) = e^{-j\pi f T_{clk}} \frac{\sin(\pi f T_{clk})}{\pi f T_{clk}}. \tag{A.6}$$

Hence, the final result is given as [Rei85]

$$S(f) = e^{-j\pi f T_{clk}} \frac{\sin(\pi f T_{clk})}{\pi f T_{clk}} \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} c_m \sigma(f - n f_{clk} - m f_{out}). \tag{A.7}$$

To summarize, the DDS action causes all frequency components residing in $v(t)$ to be aliased about every harmonic of the clock frequency f_{clk}. Therefore, if $v(t)$ is a perfect sine wave, then the spectrum contains the frequencies $n\, f_{clk} \pm f_{out}$. The component corresponding to n = 0 is the desired sine wave, and the others are commonly referred to as images. On the other hand, the MSB of the phase accumulator could be used alone to generate a square wave. The spectrum contains the frequencies $n\, f_{clk} \pm m\, f_{out}$, where m takes all the odd values from 1 to ∞ for a square wave. The harmonics of the square wave would then be aliased arbitrarily close to the desired fundamental output frequency and a substantially different spurious performance would be realized.

Appendix B: Derivation Output Current of Bipolar Current Switch with Base Current Compensation

In the base current compensation circuit (Figure 9.7) a binary weighted amount of current (I_1) is driven through a bipolar transistor (Q_3), whose geometrical size is identical to the current switch transistor (Q_1). The operating point of the transistor (Q_3) is set to be the same as in the switch transistor (Q_1) by a transistor (Q_4) and two diodes. Therefore the forward current gain of the transistor (Q_3) is the same as in the current switch transistor (Q_1). The base current of the transistor (Q_3) is

$$I_{b3} = \frac{I_1}{1 + \beta_F}. \tag{B.1}$$

where β_F is the forward current gain of the transistor (Q_3). The collector current of the cascode transistor (Q_4) is

$$I_{C4} = \frac{I_{b3}\beta_{F4}}{1 + \beta_{F4}} = \frac{\beta_{F4}}{(1 + \beta_{F4})(1 + \beta_F)} I_1. \tag{B.2}$$

where β_{F4} is the forward current gain of (Q_4). The collector current of the transistor (Q_4) is mirrored with MOS current mirrors at the node of the current switches. If the current mirrors are assumed ideal, then the emitter current of the current switch transistor is

$$I_E = I_1 + I_{C4} = \frac{(1 + \beta_{F4})(1 + \beta_F) + \beta_{F4}}{(1 + \beta_{F4})(1 + \beta_F)} I_1. \tag{B.3}$$

The output current of the current switch transistor (Q_1) is

$$I_{out} = \frac{I_E \beta_F}{1 + \beta_F} = \frac{\beta_F ((1 + \beta_{F4})(1 + \beta_F) + \beta_{F4})}{(1 + \beta_{F4})(1 + \beta_F)(1 + \beta_F)} I_1. \tag{B.4}$$

If it is assumed that $\beta_F = \beta_{F4}$, then the output current of the current switch is

$$I_{out} = \frac{\beta_F + 3\beta_F^2 + \beta_F^3}{1 + 3\beta_F + 3\beta_F^2 + \beta_F^3} I_1 = \frac{1}{1 + \frac{1 + 2\beta_F}{\beta_F + 3\beta_F^2 + \beta_F^3}} I_1. \tag{B.5}$$

With the base current compensation circuit the output current of the current switch could be approximated by

$$I_{out} = \frac{1}{1 + \frac{1 + 2\beta_F}{\beta_F + 3\beta_F^2 + \beta_F^3}} I_1 \approx \frac{1}{1 + \frac{2}{\beta_F^2}} I_1. \tag{B.6}$$

Appendix C: Digital Phase Pre-distortion of Quadrature Modulator Phase Errors

The following is an analysis of the digital phase pre-distortion of the quadrature modulator analog phase errors. In this analysis the amplitude balance between two branches is assumed to be perfect. The quadrature IF signals are

$$x(t) = \sin(\omega_{BB}\, t) \tag{C.1}$$

$$y(t)=\cos(\omega_{BB} t+\phi_{e1}+\phi_d) \tag{C.2}$$

where ω_{BB} is an IF signal frequency, and ϕ_d is the digital phase offset to pre-distort the quadrature modulator phase errors. The matching between the D/A converters and post-filters is not perfect, so there is phase imbalance between the two branches. This phase error is defined as ϕ_{e1}. For example, a 92° phase difference between the two branches would be represented by ϕ_{e1} = 2°. The IF signals are multiplied by the I and Q LOs, and the resulting signal at RF can be expressed as

$$z(t) = x(t)\sin(\omega_{LO}\, t) + y(t)\cos(\omega_{LO}\, t + \phi_{e2}) \tag{C.3}$$

where the phase mismatch between the I and Q LO signals is defined as ϕ_{e2}. Substituting (C.1), (C.2) into (C.3) and using trigonometric identities, we can expand (C.3) as

$$\begin{aligned} z(t) = &\frac{1}{2}\left[\cos\left((\omega_{LO}+\omega_{BB})\, t + (\phi_{e1}+\phi_{e2}+\phi_d)\right) + \cos\left((\omega_{LO}+\omega_{BB})\, t\right)\right] \\ &+ \frac{1}{2}\left[\cos\left((\omega_{LO}-\omega_{BB})\, t\right) - \cos\left((\omega_{LO}-\omega_{BB})\, t - (\phi_{e1}-\phi_{e2}+\phi_d)\right)\right]. \end{aligned} \tag{C.4}$$

Again, using trigonometric identities, we can simplify (C.4) as

$$\begin{aligned} z(t) = &\cos\left(\frac{\phi_{e1}+\phi_{e2}+\phi_d}{2}\right)\cos\left((\omega_{LO}+\omega_{BB})\, t + \left(\frac{\phi_{e1}+\phi_{e2}+\phi_d}{2}\right)\right) \\ &+ \sin\left(\frac{-\phi_{e1}+\phi_{e2}-\phi_d}{2}\right)\sin\left((\omega_{LO}-\omega_{BB})\, t - \left(\frac{\phi_{e1}-\phi_{e2}+\phi_d}{2}\right)\right). \end{aligned} \tag{C.5}$$

In (C.5), the first term is the upper sideband signal and the second term is the lower sideband signal. If the upper sideband is selected, then the digital phase offset value should be tuned to

$$\phi_d = -\phi_{e1} + \phi_{e2} \tag{C.6}$$

and the image (lower sideband) disappears in (C.5), which results in

$$z_{USB}(t) = \cos(\phi_{e2})\cos((\omega_{LO}+\omega_{BB})\, t + \phi_{e2}). \tag{C.7}$$

If the lower sideband is selected, then the digital phase offset value should be tuned to

$$\phi_d = 180° - \phi_{e1} - \phi_{e2} \tag{C.8}$$

and the image (upper sideband) disappears in (C.5), which results in

$$z_{LSB}(t) = \cos(\phi_{e2})\cos((\omega_{LO}-\omega_{BB})t - \phi_{e2}). \tag{C.9}$$

The term $\cos(\phi_{e2})$, where ϕ_{e2} is the phase mismatch between the I and Q LO signals, will reduce gain in (C.7), (C.9). This gain reduction might be adjusted after the phase pre-distortion. How-

ever, in this fixed quadrature LO the phase mismatch between the I and Q LO signals is small. Most phase errors are caused by a mismatch between two post-filters.

Appendix D: Different Recently Reported DDS ICs

Table D.1. Different Recently Reported DDS ICs.

	[Nic91]	[Tan95a]	[Mad99]	[Mor99]	[Bel00]	[Cho00]	This work Chapter 9	This work Chapter 10	This work Chapter 11	This work Chapter 13
Technology	1.25 µm CMOS	0.8 µm CMOS	1.0 µm CMOS	0.5 µm CMOS	0.8 µm CMOS	0.6 µm CMOS	0.8 µm BiCMOS	0.5 µm CMOS	0.35 µm BiCMOS	0.35 µm BiCMOS
Max clock frequency (MHz)	150 @ 5 V	200 @ 5 V	100 @ 5 V	230 @ 3.3 V	30 @ 3.3 V	200 @ 3.3 V	110 @ 3.3 V	150 @ 3.3 V	61.44 @ 3 V	52 @ 3.3 V
Frequency resolution (Hz)	0.035	0.047	0.0015	-	29	0.047	0.0256	0.0349	0.0143	0.77
Amplitude resolution (bits)	12	12	16	11	9	10	10	10	14	14
Phase modulation	No	Yes	No	No	No	Yes	No	Yes	Yes	No
Amplitude modulation	No	Yes	No	No	No	Yes	No	No	Yes	No
QAM modulation	No	Yes	No	No	No	Yes	No	No	Yes	No
Multi-carrier	No	No	No	No	No	No	No	No	Yes	Yes
Quadrature outputs	No	Yes	Yes	Yes	No	No	No	Yes	No	No
On-chip DAC's	No	No	No	Yes	No	No	Yes	Yes	Yes	Yes
On-chip LPF's	No	No	No	No	No	No	No	Yes	No	No
Digital SFDR (dBc)	90.3	84.3	100	-	60	84.3	72	72	84.3	84.3
Analog SFDR (1/3fclk) (dBc)	-	-	-	25	-	-	52	40	-	52
Power dissipation	1 W @ 5 V	2 W @ 5 V	1.4 W @ 5 V	92 mW @ 3.3 V	9.5 mW @ 3.3 V	1.82 W @ 3.3 V	282 mW @ 3.3 V	314 mW @ 3.3 V	1.47 W @ 3.3 V	706mW @ 3.3 V
Transistor count	35 000	52 000	58 000	-	-	430 000	19 100	17 803	-	500 000
Active area	16 mm^2	16 mm^2	12 mm^2	1.6 mm^2	0.9 mm^2	64 mm^2	3.9 mm^2	9 mm^2	20.1 mm^2	19.1 mm^2