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Design of Low Power and Low Area Passive Sigma Delta Modulators for Audio Applications

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Preface

Digital integrated circuits have increased in importance and use in computational and signal processing fields. Since the world has an analog nature, data converters are needed to interface it to the digital processing core. To keep up with the rising speed of the digital circuits, data converters need to increase in speed and accuracy. Oversampling converters, which work at a sampling frequency many times higher than the Nyquist rate, are able to achieve the required high resolutions, at reasonably high speeds. These converters use a considerable amount of digital circuitry, which is getting cheaper, increasing their popularity in many applications.

The objective of the project described in this book is the design of a Sigma Delta Modulator ($\Sigma\Delta$M), an oversampling converter, for portable audio applications. This means both its circuit area and power dissipation must be minimized. The target bandwidth of the modulator is 20 kHz, meaning it is useful for audio applications, such has hearing aids. This also means it needs high resolution, a SNDR higher than 90 dB. The modulator uses passive integrators based on the ultra incomplete settling (UIS) concept, employing a switched-capacitor topology, eliminating the need of a high gain amplifier. Through high level models, three modulators were designed and optimized: a second order $\Sigma\Delta$M and two versions of a third order MASH $\Sigma\Delta$M, one using a monostable circuit to reduce the size of the components.

Electrical simulations show that the second order $\Sigma\Delta$M achieves a peak SNDR of 81.84 dB, a FOM$_W$ of 115 fJ/conv-step, and a FOM$_S$ of 168 dB, while dissipating 46.5 μW. The third order MASH $\Sigma\Delta$M achieved a peak SNDR of 92.72 dB, a FOM$_W$ of 96 fJ/conv-step, and a FOM$_S$ of 174 dB, while dissipating 137.4 μW. The second version of the third order MASH $\Sigma\Delta$M, using the monostable circuit, achieved a peak SNDR of 92.06 dB, a FOM$_W$ of 65.6 fJ/conv-step, and a FOM$_S$ of 176 dB, while dissipating 85.97 μW.

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Acronyms

$\Sigma\Delta$M	Sigma Delta Modulator
ADC	Analog to Digital Converter
CBT	Clock Bootstrap
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital to Analog Converter
DC	Direct Current
DCL	Digital Cancellation Logic
DR	Dynamic Range
EDA	Electronic Design Automation
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FOM	Figure of Merit
GBW	Gain-Bandwidth
MASH	Multi-stage Noise Shaping
MOS	Metal-Oxide Semiconductor
NMOS	N-type Metal-Oxide Semiconductor
NTF	Noise Transfer Function
OSR	Oversampling Ratio
PMOS	P-type Metal-Oxide Semiconductor
RC	Resistor-Capacitor
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
STF	Signal Transfer Function
SC	Switched-Capacitor
UIS	Ultra Incomplete Settling

Chapter 1
Introduction

1.1 Motivation and Background

Digital circuits have an increasingly important role in computational and signal processing tasks, due to their robustness and simple, small structures, which can be combined to form accurate, fast, and complex systems. Due to the inherent analog nature of the physical world, data converters, namely an analog to digital converter (ADC) and a digital to analog converter (DAC), are needed to interface with the digital signal processing core. The speed and density of digital integrated circuits rises every year, meaning these converters must increase in speed and accuracy to keep up with technology advancements.

Data converters can be classified according to their sampling frequency: Nyquist rate and oversampling converters. Nyquist rate converters work at a sampling rate which is twice its input signal bandwidth, and have a one-to-one correspondence between their input and output samples. This means it has no memory, each input sample is processed independently. Matching accuracy of its analog components determines the linearity and accuracy of the converter. In practice, the effective number of bits (ENOB) of these converters is around 12.

Higher resolution and linearity is required for many applications, like digital audio, and can be as high as 20 bits. Integrating or counting converters can achieve such performance, but are too slow for most signal processing applications.

Oversampling converters, such as Sigma-Delta Modulators ($\Sigma\Delta$M), can achieve this required resolution at reasonably high speeds by using a much higher sampling frequency, typically 8–512 times the Nyquist rate. These converters have memory, each output uses all preceding input values. The accuracy is measured as the Signal to Noise Ratio (SNR) for a sine wave input and is used to calculate the ENOB through the expression:

$$\text{SNR} = 6.02 * \text{ENOB} + 1.76 \tag{1.1}$$

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A considerable amount of digital circuits is needed in oversampling converters, but the accuracy requirements of the analog components are relaxed. Through digital integrated circuits technology advancements, digital circuitry is getting cheaper and oversampling converters are replacing Nyquist rate converters in many applications [1, Sect. 1.1, p. 1].

The first $\Sigma\Delta$M was proposed in 1962 by Inose et al. [2], achieving a SNR of almost 40 dB with a signal bandwidth of about 5 kHz. Since the trade-off between analog accuracy and higher speed and additional digital hardware was not attractive at the time, development of this technology was sparse.

During the decades of 1970 and 1980, theory, analysis, and design techniques for $\Sigma\Delta$ modulation were developed at Bell Laboratories by J.C. Candy and his collaborators, where the Multi-Stage Noise Shaping (MASH) structure was also first proposed [3], which was first applied in a $\Sigma\Delta$ ADC by Hayashi et al. [4] in 1986.

In the following years, many advancements were made, both in theory and implementation, of $\Sigma\Delta$ modulation. More recently, the increase in use of portable devices motivated the development of low power and low voltage design techniques [1, Sect. 1.8, p. 17].

This book presents the study and design of discrete time, switched capacitor, passive $\Sigma\Delta$ modulators, working as ADC, suited for audio applications. This means the circuit area and consumed power have to be minimized. The passive integrator is constructed using resistor-capacitor (RC) branches working under Ultra Incomplete Settling (UIS). Two modulators were designed, a second order $\Sigma\Delta$M and a third order MASH $\Sigma\Delta$M, both working for a signal bandwidth of 20 kHz. The target Signal to Noise and Distortion Ratio (SNDR) for the second order modulator was 80 dB and for the third order was 90 dB.

For the third order modulator, two versions were designed. One using the values of the components obtained through optimization, and the other using a monostable circuit to reduce the components size, while maintaining performance.

With these performance parameters, the modulators can be used in a wide range of audio applications. In the field of biomedicine, it can be used in hearing aids. These devices need an ADC to interface the microphone with the digital processing core, which operates on the signal and then passes it to the speaker, through a DAC. The SNDR of the ADC needs to be at least 60 dB and its dynamic range 120 dB, to capture the sound pressure levels of a normal hearing person, ranging from hearing threshold to the level of discomfort. This dynamic range is difficult to implement, especially considering that power consumption is a problem, but a value above 90 dB is considered sufficient in practice. In order to extend battery live, power consumption must be minimized, as is the circuit area in order to reduce fabrication cost [5].

1.2 Book Organization

This book is composed of five chapters, including this introduction. In Chap. 2, a general overview of Sigma-Delta modulation is presented. Its working principles, advantages, and disadvantages are discussed. Low order modulators are presented, as well as the problems associated with high order ones, along with design approaches that address said problems.

The proposed architecture is presented in Chap. 3. Its performance is studied, in terms of signal and transfer function. The design of the passive integrator used is explained, which is based on the UIS of switched-capacitor circuits. An analysis of an RC branch based on this approach is presented and studied, and is shown how it can be used to implement the passive integrator, replacing the high gain amplifier typically used. Optimization results of the modulators are shown, along with the high level models used to obtain and validate them. Finally, it is explained how a monostable circuit can be used to reduce the size of the capacitors used, while not affecting the performance of the modulator.

All the electrical circuits that are part of the modulators are presented in Chap. 4. Their design methodologies are explained and electrical simulations are used to validate their proper behavior. The measured results obtained from electrical simulations of the three designed modulators are also shown in this chapter.

Lastly, in Chap. 5, the achieved results are compared to the expected results obtained by the models and to other approaches for $\Sigma\Delta$ modulators, working in similar signal bandwidth. From these comparisons, some conclusions are drawn, along with possible future research suggestions to improve the methodology used.

Chapter 2
Sigma-Delta Modulation

2.1 Introduction

The Sigma-Delta Modulator ($\Sigma\Delta$M) is a type of data converter that, when used as an ADC, uses oversampling, sampling the input signal at a rate several times higher than the Nyquist rate, to achieve higher resolution, at the cost of speed, when compared with ADCs that use the Nyquist rate, such as flash, pipeline, or successive approximation ADCs.

The Nyquist rate is defined as $f_N = 2B$ where B is the signal bandwidth and f_N is the sample rate. This means that two samples are taken over a period of the input signal. In the case of the $\Sigma\Delta$M, hundreds of samples may be taken over the same period due to oversampling. Higher resolution is achieved by using digital processing techniques, instead of complex and precise analog circuits, making the modulator independent of component matching or precise sample-and-hold circuitry (S/H), needing only a small amount of analog circuitry.

The typical process of an ADC consists in filtering the input signal, to minimize aliasing effects, sampling, quantization, and digital encoding of the input signal. In the case of the oversampling ADC, no dedicated sampling circuit is needed, a modulator does the quantization, and, usually, a digital filter performs the encoding of the signal. Figure 2.1 shows the typical block diagrams for both of these types of ADCs.

One of the main differences between these two types of ADCs is that the oversampling converter does not require a complex high order anti-aliasing filter. That is because it samples the signal at many times its bandwidth. Aliasing happens because when sampled, a signal is reproduced, in the frequency domain, at multiples of the sampling frequency, as band-limited signals. When using Nyquist rate, these signal reproductions are very close together, as seen in Fig. 2.2a. This may lead to

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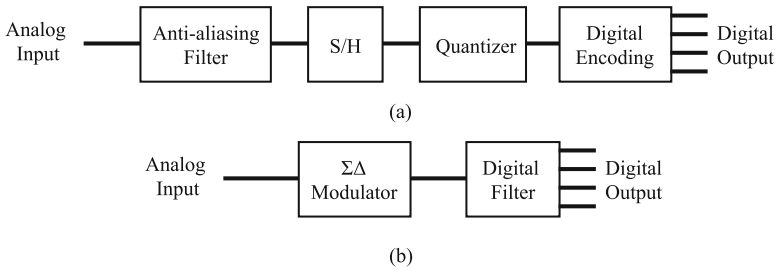


Fig. 2.1 Block diagram for (**a**) typical Nyquist rate ADCs and (**b**) for oversampling ADCs. Adapted from [6, Sect. 29.2.6, p. 1008]

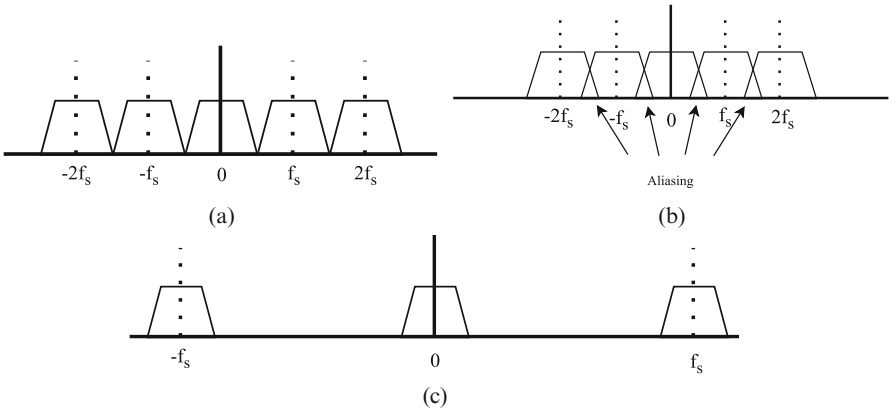


Fig. 2.2 Frequency domain for (**a**) Nyquist rate ADC, (**b**) the aliasing effect, and (**c**) oversampling ADC. Adapted from [6, Sect. 29.2.6, p. 1008]

aliasing problems, which is the overlapping of the signal reproductions, as seen in Fig. 2.2b. This does not occur when oversampling is used, since the signal reproductions are very far apart, as seen in Fig. 2.2c.

Oversampling ADCs are normally constructed using switched-capacitor (SC) circuits and the modulator's output is obtained in real time, so there is no need of a dedicated sample-and-hold circuit.

The modulator quantizes the input as a pulse-density modulated signal. This density represents the average value of the input over a specific period. When the input signal value increases, the amount of high pulses also increases, and vice versa. Figure 2.3 represents the output of the modulator for the positive half of a sine wave, where this behavior is shown.

This output is then processed digitally to filter quantization noise and spurious signals out of the band. Lastly, the signal is downsampled to the Nyquist rate, transforming it in digital data that represents the average value of the analog voltage at the input. The values of the Signal to Noise ratio (SNR) and dynamic range (DR) obtained determine the resolution of the converter [6, Sect. 29.2.6, p. 1007].

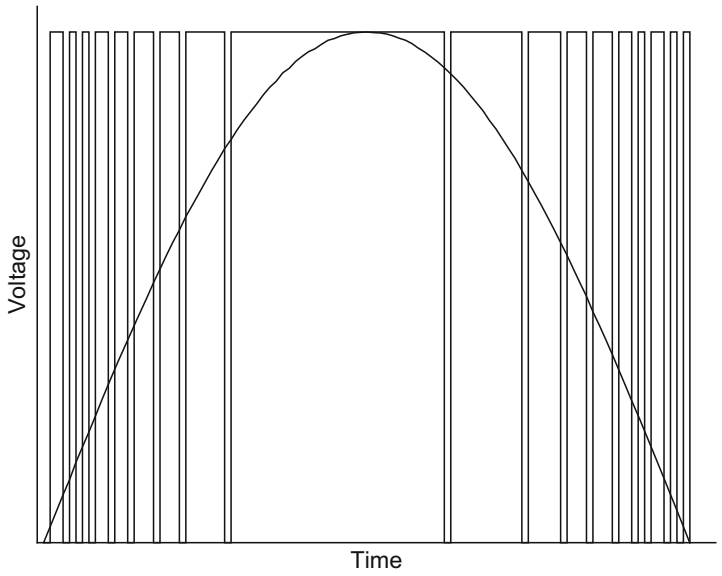


Fig. 2.3 Digital output signal of the $\Sigma\Delta$M for a positive half sine wave

The SNR value is often used to determine the ENOB of the modulator using Eq. (2.1), which represents the typical relationship between SNR and ENOB for ideal Nyquist rate converters, excited with a sine-wave signal [1, Sect. 1.1, p. 4].

$$\text{SNR} = 6.02\text{ENOB} + 1.76 \quad \text{(dB)} \tag{2.1}$$

An important parameter of the oversampling converter is the oversampling ratio (OSR), shown in Eq. (2.2), where B is the signal bandwidth and f_s is the sampling frequency. This value defines how much faster is the signal sampled by the oversampling converter, when compared with the Nyquist rate one [1, Sect. 1.2, p. 8].

$$\text{OSR} = \frac{f_s}{2B} \tag{2.2}$$

2.2 First Order Sigma-Delta Modulator

The basic structure of a first order $\Sigma\Delta$M is presented in Fig. 2.4a. It is built using an integrator, a 1-bit ADC and a 1-bit DAC in the feedback path. The 1-bit ADC is a comparator that produces either a high or a low output. The 1-bit DAC uses the comparator output to determine what is summed with the input, either $+V_{\text{REF}}$ or $-V_{\text{REF}}$. The labeled signals are expressed in terms of the sampling time, T, and an integer, k, meaning these are discrete time signals.

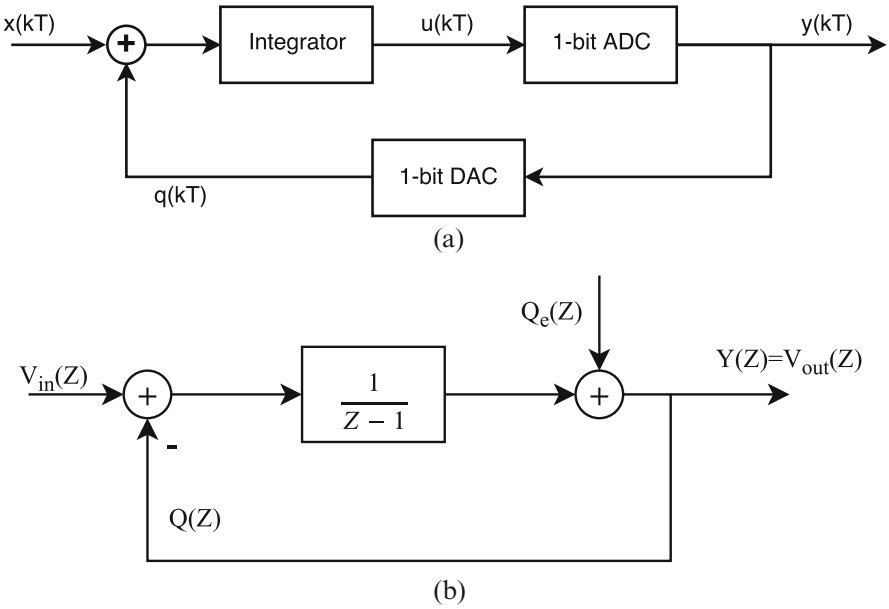


Fig. 2.4 First order $\Sigma\Delta$M structure (**a**) and its frequency domain model (**b**)

To obtain the expression of the output signal, $y(kT)$, ideal components are considered. The integrator simply sums its previous input and output signals:

$$u(kT) = x((k-1)T) - q((K-1)T) + u((k-1)T). \tag{2.3}$$

The ideal 1-bit ADC has a quantization error defined by the difference between its output and its input:

$$Q_e(kT) = y(kT) - u(kT). \tag{2.4}$$

The ideal 1-bit DAC produces a positive or negative reference voltage, according to the logic level of its input. Since these logic levels are defined using the same reference voltages, its easy to assume that the ideal 1-bit DAC is a unity gain block, its output is equal to its input:

$$q(kT) = y(KT). \tag{2.5}$$

Using Eqs. (2.3) and (2.4) in Eq. (2.5), the output of the first order $\Sigma\Delta$M, $y(kT)$, is defined by:

$$y(kT) = x((k-1)T) + Q_e(kT) - Q_e((k-1)T). \tag{2.6}$$

Equation (2.6) shows that the output of the modulator is equal to the quantized value of the input, delayed by one sampling period, plus the difference between the current and late quantization error. This means that the quantization noise cancels itself to the first order [6, Sect. 29.2.6, p. 1011].

Considering the ideal frequency domain model of the modulator, shown in Fig. 2.4b, these results may once again be reached. The modulator is modeled in the z-domain, in which the integrator is modeled by its transfer function, $\frac{1}{z-1}$, the 1-bit ADC is assumed to be a quantization error source, $Q_e(z)$, and the 1-bit DAC is modeled in a way that $Q(z)$ is equal to the output $Y(z)$, as seen previously. Using feedback theory on the model, the output becomes:

$$V_{\text{out}}(z) = z^{-1}V_{\text{in}}(z) + (1 - z^{-1})Q_e(z). \tag{2.7}$$

The output can be written in the general form:

$$V_{\text{out}}(z) = \text{STF}(z)V_{\text{in}}(z) + \text{NTF}(z)Q_e(z). \tag{2.8}$$

The STF(z) and NTF(z) correspond to signal and noise transfer functions, respectively. In Fig. 2.5 is plotted their squared magnitude, by setting $z = e^{j2\pi f}$, and considering the sampling frequency, f_s, equal to 1. This yields:

$$\left|\text{NTF}(e^{j2\pi f})\right|^2 = [2\sin(\pi f)]^2 . \tag{2.9}$$

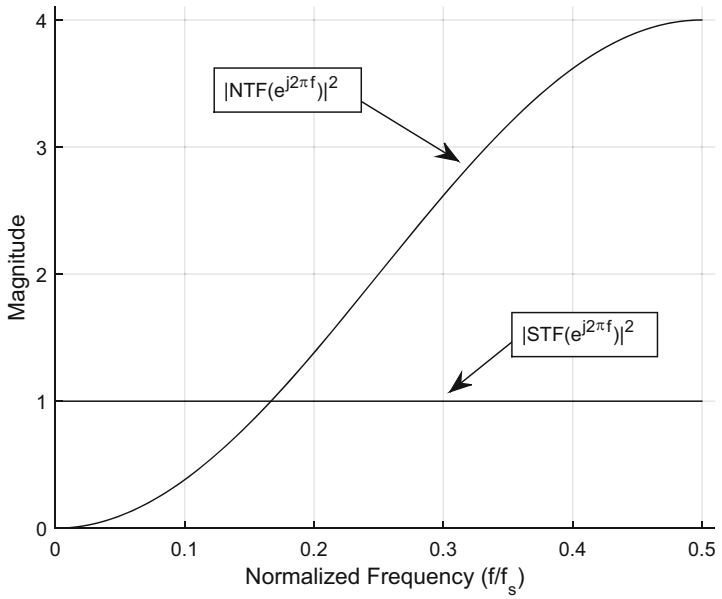


Fig. 2.5 Frequency response of the first order $\Sigma\Delta$M

Equation (2.9) can be approximated by $|\text{NTF}|^2 = (2\pi f)^2$, for $f \ll 1$. Figure 2.5 and Eq. (2.7) show that, in the signal bandwidth, which is as close to 0 as higher the OSR is, the signal maintains its strength, suffering only from a one sample delay, and the quantization noise is heavily attenuated and pushed to higher, out-of-band frequencies, where it is amplified, showing a high-pass characteristic. This is called *noise shaping* and is characteristic of $\Sigma\Delta$ modulation and it is the reason of its effectiveness. A low-pass filter must then be used at the output to reduce this quantization noise and obtain the final high resolution output by downsampling. These operations are most often realized by *sinc filters*, which are implemented in stages [1, Sect. 2.9, p. 54].

Considering a large, randomly varying input at the DAC, the error can be treated as white noise with mean-square value $\sigma_e^2 = \frac{1}{3}$ and a 1-sided power spectral density of $S_e(f) = 2\sigma_e^2 = \frac{2}{3}$. In this scenario, the in-band noise power of the output is approximately:

$$\sigma_q^2 = \int_0^{1/(2\cdot\text{OSR})} |\text{NTF}|^2 \cdot S_e(f) df = \frac{\pi^2}{9(\text{OSR})^3}. \tag{2.10}$$

Assuming a sine wave as input, with peak amplitude A, the output signal power is $\sigma_u^2 = \frac{A^2}{2}$, since $|\text{STF}|^2 = 1$. The SNR is then given by:

$$\text{SNR} = \frac{\sigma_u^2}{\sigma_q^2} = \frac{9A^2(\text{OSR})^3}{2\pi^2} \quad (\text{dB}). \tag{2.11}$$

Equation (2.11) shows that when the OSR doubles, the SNR increases by a factor of 8, equivalent to 9 dB, and, according to Eq. (2.1), the resolution, ENOB, is increased by 1.5 bits. This means that, even for a relatively high OSR value, for instance 256, will result in a relatively low SNR, less than 70 dB [1, Sect. 2.4, pp. 36–38].

Its important to note that the nonlinear distortion of the DAC is not affected by the *noise shaping*, thus limiting the overall performance of the modulator. The simplest solution to this problem is using single-bit quantization, using, for instance, a comparator as the ADC. This leads to the DAC's operation becoming inherently linear, since it only consists of two points. In this case, and with an input signal with magnitude below or equal to 1, it is proved that the first order $\Sigma\Delta$M is stable [1, Sect. 1.2, p. 7; Sect. 2.7, p. 49].

2.3 Second Order Sigma-Delta Modulator

Figure 2.6a shows the structure of a second order $\Sigma\Delta$M. It is obtained by replacing the quantizer, the 1-bit ADC, in the first order $\Sigma\Delta$M with a copy of a first order $\Sigma\Delta$M. Considering again ideal components, the output, $y(kT)$, takes the form:

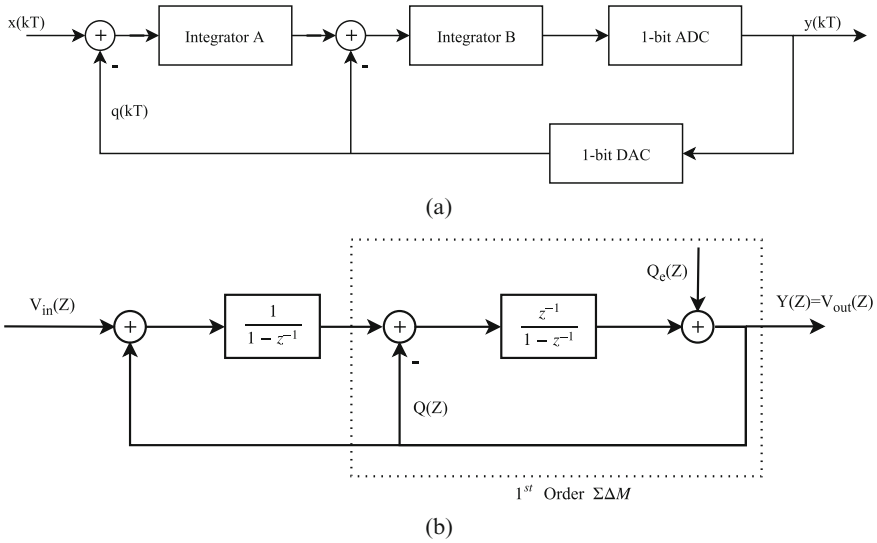


Fig. 2.6 Second order $\Sigma\Delta$M structure (**a**) and its frequency domain model (**b**)

$$y(kT) = x((k-1)T) + Q_e(kT) - 2Q_e((k-1)T) + Q_e((k-2)T). \tag{2.12}$$

Equation (2.12) shows that the output is still a delayed quantized input signal, but this time with a second order differencing of the quantization noise. Figure 2.6b shows its linear z-domain model, from which the NTF and the STF can be obtained:

$$V_{\text{out}}(z) = \text{STF}(z)V_{\text{in}}(z) + \text{NTF}(z)Q_e(z) = z^{-1}V_{\text{in}}(z) + (1-z^{-1})^2 Q_e(z). \tag{2.13}$$

The squared magnitude of the NTF is then given by:

$$\left|\text{NTF}(e^{j2\pi f})\right|^2 = [(2\sin(\pi f)]^4 \approx (2\pi f)^4, \text{ for } f \ll 1. \tag{2.14}$$

In Fig. 2.7, the squared magnitudes of the STF and NTF are plotted, showing that, like in the first order $\Sigma\Delta$M, the signal is unaffected and that the quantization noise is highly attenuated in the band of the signal, near 0, but is highly boosted in high, out-of-band frequencies, more than in case of the first order $\Sigma\Delta$M. This means that the total quantization noise power at the output of the second order $\Sigma\Delta$M is greater, but since it is located out of the signal bandwidth, it can be easily filtered, by a digital decimation filter at the output of the system.

The in-band noise power of the modulator can be calculated similarly as in the first order $\Sigma\Delta$M:

$$\sigma_q^2 = \int_0^{1/(2\cdot\text{OSR})} |\text{NTF}|^2 \cdot S_e(f)df = \frac{\pi^4}{15(\text{OSR})^5}. \tag{2.15}$$

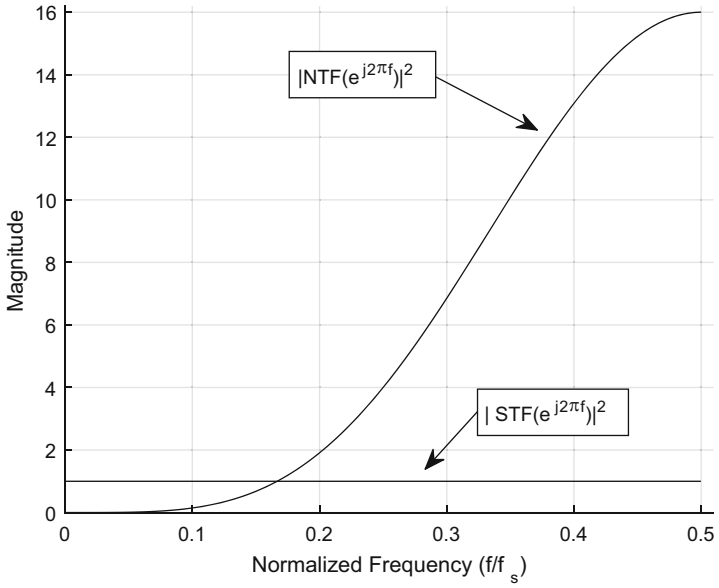


Fig. 2.7 Frequency response of the second order $\Sigma\Delta$M

Considering again a sine wave as an input signal with power $\sigma_u^2 = \frac{A^2}{2}$, the SNR of the second order $\Sigma\Delta$M is thus:

$$\text{SNR} = \frac{\sigma_u^2}{\sigma_q^2} = \frac{15A^2(\text{OSR})^5}{2\pi^4} \quad \text{(dB)}. \tag{2.16}$$

From Eq. (2.16), the doubling of the OSR leads to an increase by a factor of 32, equivalent to 15 dB, of the SNR, which translates, according to Eq. (2.1), in an increase of 2.5 bits in resolution, ENOB. This means that to achieve the same value of SNR, the second order $\Sigma\Delta$M needs a lower OSR, leading to a lower sampling frequency, when compared with the first order $\Sigma\Delta$M. The downside is the increased total noise power, as stated previously.

If a single bit quantizer is used, the second order $\Sigma\Delta$M is inherently linear, under the same conditions as the first order $\Sigma\Delta$M, that is the magnitude of the input signal is lower than 1. The nonidealities of the components are treated as noise and are affected by the NTF, and shifts in component values lead to a shift in the pole and zero locations of the STF and NTF, not into nonlinearities [1, Sect. 3.1, pp. 63–66].

The output filtering and downsampling are once again achieved using decimation filters, normally based on cascaded sinc filters. These filters can be used for any Lth order modulator, and to achieve adequate results, its order, K, must be higher than the modulator's order, that is $K > L$ [1, Sect. 3.5, p. 86].

2.4 Higher Order Sigma-Delta Modulator

Higher order modulators offer increased resolution and more noise shaping, for the same OSR. The amount of quantization noise added is increased, but more is pushed to higher frequencies, decreasing the noise in the signal band. The output is still a delayed version of the input with a differencing of the quantization noise proportional to the order of the modulator.

The easiest way to construct an n-order modulator is to simply adding $n - 1$ integrators to the structure of the first order SDM. However, because this structure employs feedback loops, stability starts to become a critical issue [6, Sect. 29.2.6, p. 1014].

The range of the input signal magnitude in which the modulator works as intended is called stable input range. This range is determined by the full-scale range of the feedback DAC, usually being a few dB lower for single-bit quantization. This happens because when the input signal of the modulator approaches the edge of the overload region of the quantizer, extra quantization noise added may push the quantizer into the overload region. Because of feedback, the modulator enters a vicious cycle causing the quantizer to overload and leading to the saturation of the active blocks, turning the modulator unstable. Stability may not be restored by returning the input to the stable input range, thus it is often required an external intervention, such as a reset of the integrators in the modulator.

The stability properties of a single bit modulator are ruled by its NTF. However, there are no linear models that can predict stability with total reliability due to the signal dependency of the quantizer gain, which cannot be captured by any linear model. Extensive simulations using worst case input signals must be performed to study stability.

There are some criteria which can help predict instabilities, but are either too conservative or only work for specific modulators. The most widely used is the *Lee criterion* [7], which is neither necessary nor sufficient to determine stability, has no solid theoretical foundations, but, due to its simplicity, it is very popular [1, Sect. 4.2, pp. 97–103].

One way to deal with the stability issues is to use a multi-bit quantizer. However, its complexity rises exponentially with the number of bits, limiting it to 4 or 5 bits maximum.

A different approach is to cancel the quantization noise, rather than filter it, using multi-stage, or cascade, structures. Several such structures exist, like the *Leslie-Singh Structure* [8], and the one used in this work is called MASH (for Multi-stAge-noise-SHaping), which will be discussed in the next section [1, Sect. 4.5, p. 122].

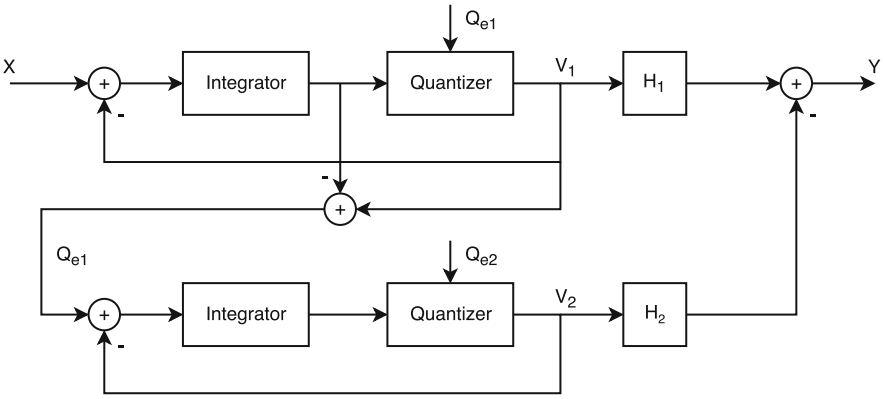


Fig. 2.8 Structure of a 2-stage 1-1 MASH $\Sigma\Delta$M

2.4.1 The MASH Structure

A Multi-stAge-noise-SHaping (MASH) structure is constructed using $\Sigma\Delta$M in stages, where the input of the next stage is the quantization error introduced by the quantizer of the current stage, that is the difference between its output and input. The outputs of the individual stages are then digitally filtered and combined in a way that the quantization noise of each stage, excluding the last, is canceled at the overall output of the structure.

In Fig. 2.8 is shown a 2-stage MASH structure using a first order $\Sigma\Delta$M in each stage. In terms of signal (STF) and noise (NTF) transfer functions, the output of the first stage is:

$$V_1(z) = \mathrm{STF}_1(z)X(z) + \mathrm{NTF}_1(z)Q_{e1}(z). \tag{2.17}$$

Considering that the input of the second stage is the quantization error of the first stage, its output is given by:

$$V_2(z) = \mathrm{STF}_2(z)Q_{e1}(z) + \mathrm{NTF}_2(z)Q_{e2}(z). \tag{2.18}$$

The digital filters H_1 and H_2 must be designed in order to cancel the quantization error, Q_{e1}, of the first stage at the output of the structure, Y. To achieve it, the following condition must be true:

$$H_1 \cdot \mathrm{NTF}_1 - H_2 \cdot \mathrm{STF}_2 = 0. \tag{2.19}$$

The simplest way to satisfy Eq. (2.19) is to make $H_1 = \mathrm{STF}_2$ and $H_2 = \mathrm{NTF}_1$. The overall output is then given by:

$$Y = H_1V_1 - H_2V_2 = \mathrm{STF}_1 \cdot \mathrm{STF}_2 \cdot X - \mathrm{NTF}_1 \cdot \mathrm{NTF}_2 \cdot Q_{e2}. \tag{2.20}$$

Considering the transfer functions of the first order $\Sigma\Delta$M, discussed in a previous section, namely STF $= z^{-1}$ and NTF $= 1 - z^{-1}$, Eq. (2.20) becomes:

$$Y(z) = z^{-2} \cdot X(z) - (1 - z^{-1})^2 \cdot Q_{e2}(z). \tag{2.21}$$

Equation (2.21) shows that the structure has a performance of a second order $\Sigma\Delta$M. If second order $\Sigma\Delta$Ms were used instead, the overall structure would have the noise shaping performance of a fourth order modulator. This principle can be extended to a 3-stage structure, where if second order $\Sigma\Delta$Ms were used, it would perform as a sixth order modulator. The third stage would cancel the quantization noise from the second and the cancellation conditions are found in exactly the same way.

The overall stability of the structure is determined by the modulators used in each stage, so by using only first or second order modulators, stability becomes less of an issue. In practice, the input of each additional stage must be scaled to fit the stable input range, and its inverse must be included in H_2 for the noise cancellation.

Since quantization error, which is similar to noise, is used as input, the quantization error in that stage is very close to true white noise, even if the first stage noise contains tones. This reduces the need for dithering. Also no harmonic distortion of the signal is generated in these stages and the small noise added by the DAC's nonlinearity is tolerable. This structure also allows the use of multi-bit quantizer in the second or higher stages without correction of the DAC nonlinearity, because it is high-pass filtered by the NTF of the previous stage, suppressing it at the baseband.

To achieve good performance, that is a large SNR value, the MASH structure relies on the accurate cancellation of the quantization noise. This requires a good matching between the transfer functions of the modulators used in the stages and the transfer functions of the digital filters, so that the conditions like in Eq. (2.19) holds. Any mismatch results in a degradation of the noise cancellation and leads to lower SNR values. This is called noise leakage and requires accurate behavioral simulations to understand its effect on the performance of the structure and to reduce it to acceptable levels. The increase in number of stages leads to more noise leakage and more complex equations describing it [1, Sect. 4.5.2, pp. 127–132].

Chapter 3
Architecture and High Level Model

3.1 Passive Integrator

One of the main components of a Sigma-Delta Modulator is the integrator, which is typically built using switched-capacitor (SC) circuits, making it a discrete time integrator. This approach requires an amplifier and, in order to obtain a lossless integrator, it must have an infinite DC gain, that is an ideal amplifier.

Noting that all real amplifiers have a finite gain-bandwidth (GBW), the response of a switched-capacitor integrator is that of a first order low-pass filter. To achieve small settling error, the amplifier must be designed with a high enough GBW which, for high clock frequencies, leads to a large power dissipation [9].

To mitigate this power dissipation, passive SC circuits which implement a similar low-pass filter response may be used. In [10], such a circuit was present which used a first order RC circuit, where an SC branch replaced the resistor.

In this project, the passive SC circuit used as integrator for the modulator is based on an alternative approach, first proposed in [11] and further developed in [12, 13] and [14], which uses ultra incomplete settling (UIS) of the capacitors.

3.1.1 Ultra Incomplete Settling

When applying a step signal as input to an RC circuit, the voltage at the capacitor is given by Eq. (3.1), where V_{in} is the step amplitude, V_{C0} is the voltage at the capacitor just before the input step was applied, and $R \cdot C$ is the multiplication of the resistor and capacitor values, also called the circuit's time constant.

$$v_c(t) = V_{\text{in}} \cdot \left(1 - e^{\frac{-t}{R \cdot C}}\right) + V_{C0} \cdot e^{\frac{-t}{R \cdot C}} \quad \text{(V)}. \tag{3.1}$$

D. Fouto, N. Paulino, *Design of Low Power and Low Area Passive Sigma Delta Modulators for Audio Applications*, SpringerBriefs in Electrical and Computer Engineering, DOI 10.1007/978-3-319-57033-4_3

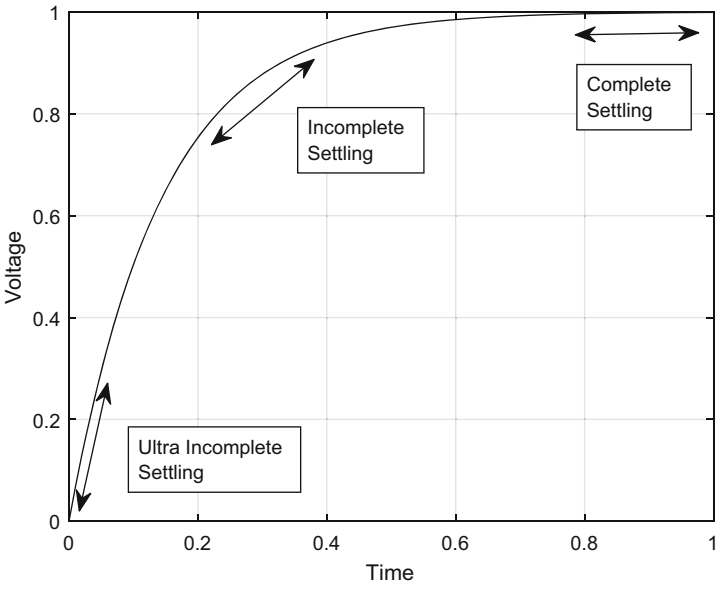


Fig. 3.1 Capacitor voltage response of a unity step input (normalized time). Adapted from [12]

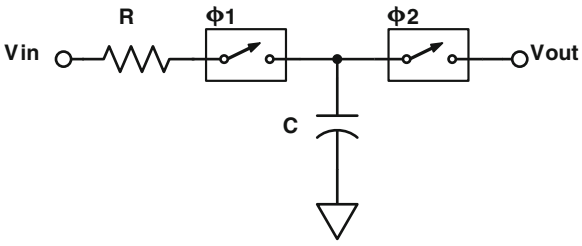


Fig. 3.2 Schematic of the proposed UIS SC passive integrator

Figure 3.1 shows a plot of Eq. (3.1), for generic R and C values, where it can be seen the different settling conditions: complete (very small settling error), incomplete (moderate settling error), and ultra incomplete (very large settling error).

In normal conditions, an SC circuit is expected to work under complete settling conditions, meaning the capacitors are almost completely charged or discharged, at the end of each clock phase, meaning also that the capacitor voltage in the current clock phase becomes independent of its voltage value at the previous clock phase.

Figure 3.2 shows a simplified schematic of the proposed passive integrator. It is an SC circuit using a two phases clock. In the first phase ($\phi 1$) the input signal is sampled in the capacitor, and in the second ($\phi 2$), the capacitor voltage is passed to the next circuit. For this circuit to operate under the UIS conditions, the duration of the clock phase must be much smaller than the time constant of the circuit ($T_s << R \cdot C$). This is achieved by adding an explicit resistor with an appropriate value, in series with the switch, so that, together with the switch's *on* resistance

(R_{on}), this condition is satisfied. This resistor is placed before the switch, to prevent its influence on the capacitor voltage during the second clock phase. Under these conditions, at the end of the clock cycle, the voltage at the capacitor is a function of the input voltage and of the capacitor's voltage value in the previous clock cycle, as stated in Eq. (3.1).

3.1.2 Discrete Time Transfer Function of the SC Integrator

For a constant input voltage V_{in}, the capacitor's voltage at the end of n clock cycles can be calculated by applying the UIS condition, $T_s << R \cdot C$, to Eq. (3.1):

$$v_c(n \cdot T_s) \approx V_{in} \cdot \frac{T_s}{R \cdot C} + V_c[(n-1) \cdot T_s] \cdot \left(1 - \frac{T_s}{R \cdot C}\right) \quad \text{(V)}. \tag{3.2}$$

In Eq. (3.2), T_s is the period of the clock phase. Its Z transform is given by:

$$H(z) = \frac{V_c(z)}{V_{in}(z)} = \frac{z^{-\frac{1}{2}} \cdot \frac{T_s}{R \cdot C}}{z - \left[1 - \left(\frac{T_s}{R \cdot C}\right)\right]} = \frac{\alpha \cdot z^{-\frac{1}{2}}}{1 - \beta \cdot z^{-1}}. \tag{3.3}$$

The parameters α and β take the form:

$$\alpha = \frac{T_s}{R \cdot C} \quad ; \qquad \beta = 1 - \alpha. \tag{3.4}$$

Equation (3.3) shows that, under the right conditions, a switched-capacitor branch behaves like a passive discrete time first order filter. The circuit also introduces a half period delay, because in the first phase it samples the input and in the second phase passes it to the next circuit. The maximum and minimum gain values of the circuit are given by, considering Eq. (3.3):

$$H_{max} = |H(z=1)| = \left|\frac{\alpha}{1-\beta}\right| = 1 \quad ; \tag{3.5}$$

$$H_{min} = |H(z=-1)| = \left|\frac{\alpha}{1+\beta}\right| = \frac{\alpha}{2-\alpha}. \tag{3.6}$$

In order to increase the ratio between the maximum and minimum gain, the circuit gain (α) must be reduced, according to the expressions of Eq. (3.6), which leads to a very small signal amplitude. Therefore, the loop gain is concentrated in the quantizer, which needs high gain to convert these small amplitude signals to a digital level. This can be achieved by using a positive feedback comparator.

3.1.3 Thermal Noise Analysis

In equilibrium, the thermal noise power of the capacitor inside an RC circuit is given by kT/C, where k is the Boltzmann constant and T is the temperature [15]. Since in the UIS conditions the capacitor's voltage does not have time to reach the equilibrium, it is necessary to recalculate it, considering that the switch is closed during a finite time T_s. The response of the circuit to a step impulse is divided in two parts, one before the switch opens ($t < T_s$), given by Eq. (3.1), and the other after it opens ($t > T_s$), given by a constant, equal to the sampled voltage value. The derivative of the step response yields the impulse response of the circuit:

$$h(t) = \begin{cases} \frac{1}{R \cdot C} \cdot e^{-t/R \cdot C} & 0 \leq t \leq T_s \\ 0 & t > T_s \end{cases} \approx \begin{cases} \frac{1}{R \cdot C} & 0 \leq t \leq T_s \\ 0 & t > T_s \end{cases} \tag{3.7}$$

Applying the Fourier Transform to Eq. (3.7) yields:

$$H(f) = \int_{-\infty}^{+\infty} h(t) \cdot e^{-2 \cdot \pi \cdot f \cdot t} dt = \frac{\sin(\pi \cdot f \cdot T_s)}{\pi^2 \cdot f \cdot R \cdot C}. \tag{3.8}$$

The thermal noise power sampled into the capacitor, at the end of a clock period, becomes:

$$P_{\mathrm{NT}} = \int_0^{+\infty} 4 \cdot k \cdot T \cdot R \cdot |H(f)|^2 df = \frac{2 \cdot k \cdot T \cdot T_s}{R \cdot C^2}. \tag{3.9}$$

The input referred noise then results in:

$$P_{\mathrm{NTinput}} = \frac{P_{\mathrm{NT}}}{\alpha^2} = \frac{2 \cdot k \cdot T \cdot R}{T_s} = \frac{2 \cdot k \cdot T}{C \cdot \alpha}. \tag{3.10}$$

Equation (3.10) shows that the input referred noise is higher in passive switched-capacitor circuits, since the value of α is small. To achieve similar noise performances, the passive circuit must use larger capacitances, which increases the circuit area. This is not a major concern because the power dissipation does not increase, due to the lack of an amplifier in the circuit. Furthermore, due to the incomplete settling behavior of the circuit, the reference voltage buffers need only supply a very small amount of charge [11–14].

3.2 Modulator Block Diagram

Building a first order Sigma-Delta Modulator using the passive SC circuit based on UIS is straightforward: the integrator is replaced by a switched RC branch, a comparator is used as a 1-bit ADC and the 1-bit DAC is a simple unity gain block.

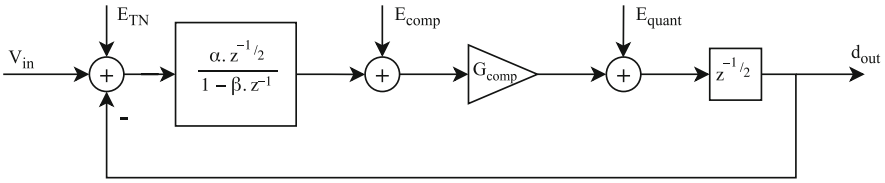


Fig. 3.3 Linear block diagram model of the first order $\Sigma\Delta$M using UIS. Adapted from [12]

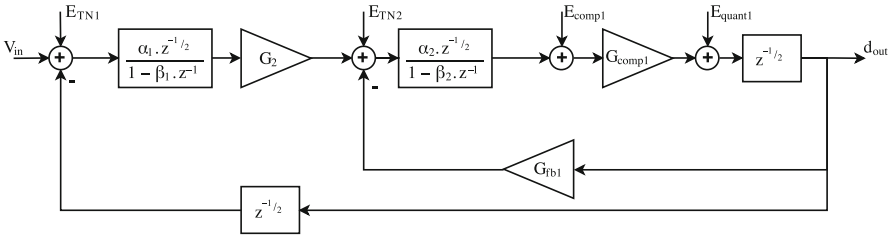


Fig. 3.4 Linear block diagram model of the second order $\Sigma\Delta$M using UIS. Adapted from [11]

The linear block diagram model of the modulator is represented in Fig. 3.3, where it is also included its noise sources: thermal, comparator, and quantization noises.

To build higher order modulators it is necessary to cascade various passive SC circuits. This leads to partial charge redistribution between the capacitors. In the SC integrators, this happens when the capacitor in the next circuit is sampling the voltage of the previous capacitor, and causes a change in the voltage of the previous capacitor. A simple gain stage (G_2) is used in order to isolate the two circuits. This gain stage also attenuates the input referred noise of the comparator. A scaling of the feedback signal fed to the second integrator, gain G_{fb1}, is also used to add extra gain to the loop. In Fig. 3.4 is shown the linear block diagram model of a second order $\Sigma\Delta$M, once again with its noise sources represented.

3.2.1 Signal and Noise Transfer Functions

Considering the first order $\Sigma\Delta$M diagram shown in Fig. 3.3, the signal transfer function of the modulator is given by:

$$\text{STF} = \frac{G_{\text{comp}} \cdot \alpha \cdot z^{-1}}{1 + (G_{\text{comp}} \cdot \alpha - \beta) \cdot z^{-1}}. \tag{3.11}$$

The exact gain value of the comparator (G_{comp}) can only be determined by simulation and is defined as the ratio between the root mean square (rms) value of its output and the rms value of its input. An approximate expression for this gain value was obtained, through simulation, in [12], and is given by:

$$G_{\text{comp}} \approx \frac{1}{\alpha}. \tag{3.12}$$

Using Eq. (3.12) in Eq. (3.11), considering a very small α value and remembering that $\beta = 1 - \alpha$ results in:

$$|\text{STF}|^2 \approx 1. \tag{3.13}$$

Meaning that the signal is not affected by the modulator, which is in line with the results obtained in Chap. 2 for the signal transfer function of a first order $\Sigma\Delta$M.

The quantization noise transfer function ($\text{NTF}_{\text{quant}}$), based in Fig. 3.3, is given by:

$$\text{NTF}_{\text{quant}} = \frac{(1 - \beta \cdot z^{-1}) \cdot z^{-1/2}}{1 + (\alpha \cdot G_{\text{comp}} - \beta) \cdot z^{-1}}. \tag{3.14}$$

This represents a high-pass transfer function, which is shown in Fig. 3.5, where $|\text{NTF}_{\text{quant}}|^2$ is plotted. Once again, this is the expected result for a $\Sigma\Delta$ modulator.

The thermal noise (NTF_{TN}) and the comparator noise (NTF_{comp}) transfer functions can also be obtained from Fig. 3.3:

$$\text{NTF}_{\text{TN}} = \frac{G_{\text{comp}} \cdot \alpha \cdot z^{-1}}{1 + (G_{\text{comp}} \cdot \alpha - \beta) \cdot z^{-1}}, \tag{3.15}$$

$$\text{NTF}_{\text{comp}} = \frac{G_{\text{comp}} \cdot (1 - \beta \cdot z^{-1}) \cdot z^{-1/2}}{1 + (G_{\text{comp}} \cdot \alpha - \beta) \cdot z^{-1}}. \tag{3.16}$$

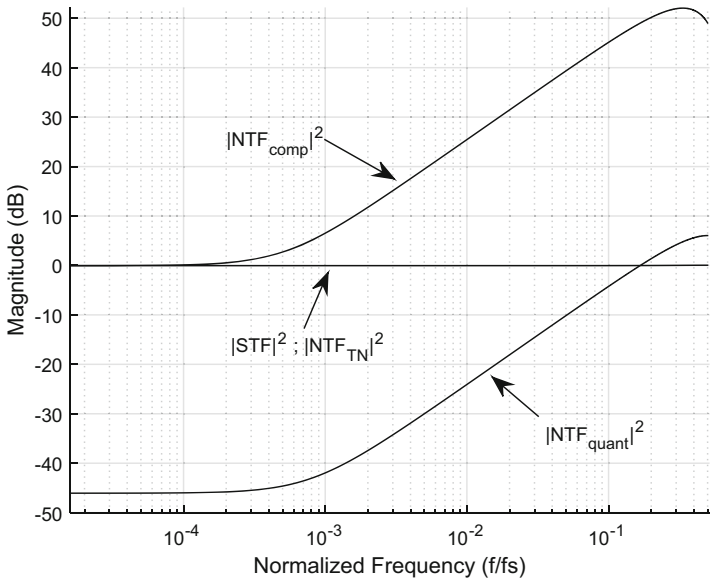


Fig. 3.5 Signal and noise transfer functions of the first order $\Sigma\Delta$M using UIS

The squared magnitude of Eqs. (3.15) and (3.16) are plotted in Fig. 3.5. These plots show that the power of the thermal noise has the same behavior of the signal transfer function, being neither amplified nor attenuated. For low frequencies, the same happens with the comparator noise, which is amplified for high frequencies.

To obtain the transfer functions of the second order modulator, a similar analysis is applied to the diagram of Fig. 3.4:

$$\mathrm{STF}=\frac{G_2 \cdot G_{\mathrm{comp}} \cdot \alpha_1 \cdot \alpha_2 \cdot z^{-1}}{1+(G_{\mathrm{fb1}} \cdot G_{\mathrm{comp}} \cdot \alpha_2-\beta_1-\beta_2) \cdot z^{-1}+G_{\mathrm{comp}} \cdot \alpha_2 \cdot (G_{\mathrm{fb1}} \cdot \beta_1+G_2 \cdot \alpha_1) \cdot z^{-2}}, \tag{3.17}$$

$$\mathrm{NTF}_{\mathrm{quant}} = \frac{z^{-1/2} \cdot [1-(\beta_1+\beta_2) \cdot z^{-1}+\beta_1 \cdot \beta_2 \cdot z^{-2}]}{1+(G_{\mathrm{comp}} \cdot G_{\mathrm{fb1}} \cdot \alpha_2-\beta_1-\beta_2) \cdot z^{-1}+[G_{\mathrm{comp}} \cdot \alpha_2 \cdot (G_2 \cdot \alpha_1-G_{\mathrm{fb1}} \cdot \beta_1)+\beta_1 \cdot \beta_2] \cdot z^{-2}}. \tag{3.18}$$

In Eqs. (3.17) and (3.18), α_1 and β_1 are the coefficients of the first integrator and α_2 and β_2 of the second. The quantization noise transfer function is only shown for its importance to the digital cancellation logic of the MASH modulator which will be discussed later.

3.3 Proposed Architecture

Figure 3.6 shows the schematic of the circuit of the second order $\Sigma\Delta$ modulator developed for this book. It is based on the structure designed in [11]. It uses a fully differential signal path, to increase the voltage swing and the power supply rejection ratio, and uses the SC branch based on UIS as the integrator. The gain stage between integrators is a differential pair loaded by resistors. These resistors are used in the SC branch of the next integrator. A comparator produces a logical level, according to the voltage difference of the capacitors at the second integrator, which is stored in a *D-type flip-flop*. The feedback loop is done using a set of switches which sum $V_{\mathrm{ref}+}$ or $V_{\mathrm{ref}-}$ to the capacitors voltage, according to the logical value of the output of the *flip-flop*.

The circuit functions in two non-overlapping phases. In the first phase ($\Phi 1$), the input signal is sampled in the first integrator by capacitors C_1. In the second phase ($\Phi 2$), the voltage at the capacitors is passed to the second integrator, through the gain stage, and is sampled by capacitors C_2. Back to the first phase, the voltage at capacitors C_2 is passed to the comparator, which produces the output logical level and it is stored by the *flip-flop*, while the input signal is sampled again.

This modulator is used, alongside a first order $\Sigma\Delta$M, to build a third order modulator using a MASH structure. Figure 3.7 shows its block diagram. The first stage uses the second order modulator of Fig. 3.6 and the second stage uses a first order $\Sigma\Delta$M, which also relies on the ultra incomplete settling of the capacitors to achieve integration and its schematic can be seen in Fig. 3.8.

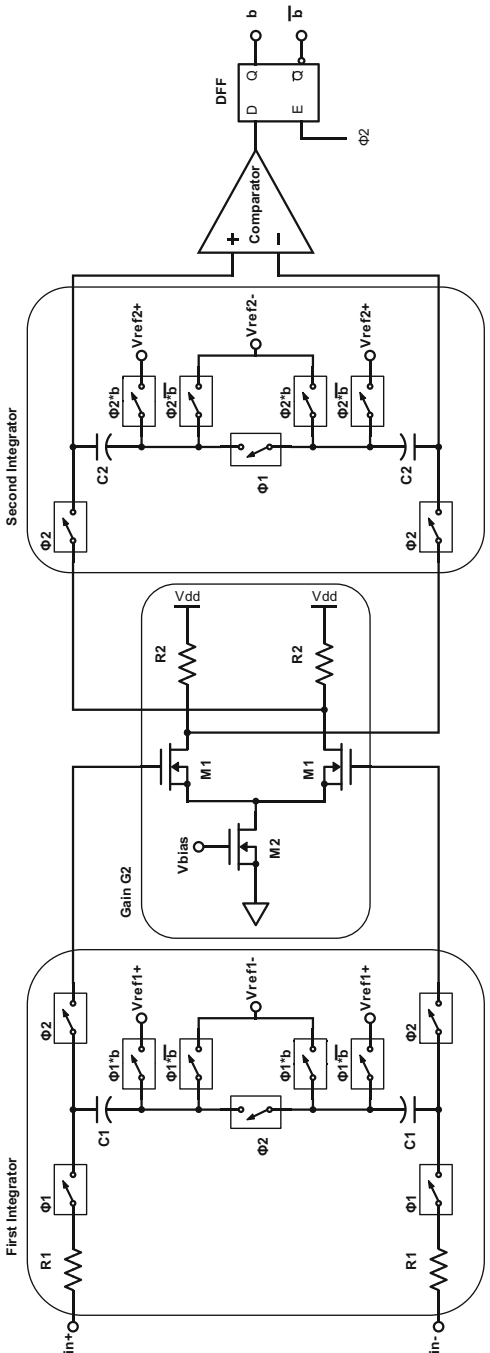


Fig. 3.6 Schematic of the second order $\Sigma\Delta$M using UIS

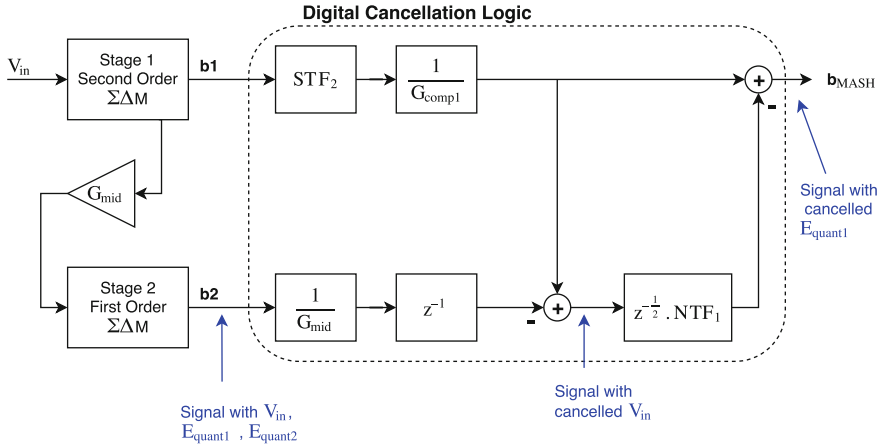


Fig. 3.7 Block diagram of the third order MASH $\Sigma\Delta$M structure. Adapted from [13]

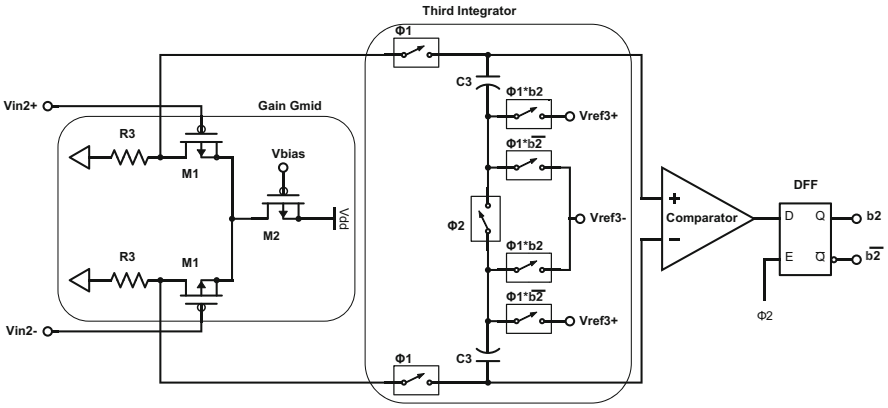


Fig. 3.8 Schematic of the first order $\Sigma\Delta$M used in the second stage of the MASH modulator and gain block G_{mid}

The structure of the MASH modulator is based on the one used in [13] and is a little different than the one presented in Chap. 2, but has the same working principle and goal: cancellation of the quantization noise of the first stage to achieve higher SNDR. The input of the second stage is the output of the second integrator of the first stage, amplified by the gain G_{mid}, a differential pair loaded by resistors. The digital cancellation logic (DCL) block then takes the outputs of both stages and produces an output in which the quantization noise of the first stage is canceled.

The output of the second stage contains the quantization noise of the first and the second stages (E_{quant1} and E_{quant2}) and the input signal of the first stage (V_{in}). The V_{in} component is canceled using the output of the first stage. The final output only contains the quantization noise of the second stage, which is shaped by the noise

transfer functions of both stages, resulting in a third order noise shaping. The gain blocks $1/G_{comp1}$ and $1/G_{mid}$ are necessary to compensate the gain of the comparator of the first stage and of the gain stage G_{mid}, respectively. The delay blocks are used to compensate the delays introduced by the *flip-flops*. The DCL also uses the signal transfer function of the second stage and the quantization noise transfer function of the first stage, which were obtained in the previous section, and are presented in Eqs. (3.11) and (3.18), respectively.

3.4 High Level Model

To optimize the values of the components in the circuiti in order to comply with the desired specifications of a SNDR value higher than 80 dB, for a bandwidth of 20 kHz, a high level model for the second order $\Sigma\Delta$ modulator, based in Fig. 3.6, was developed in the *MATLAB®* environment.

Due to the ultra incomplete settling of the voltage of the capacitors, the SC branch, which is acting as an integrator, is viewed as a first order RC filter. The transfer function of such filter is given by:

$$H_{RC}(s) = \frac{1}{RC \cdot s + 1} = \frac{B(s)}{A(s)}. \tag{3.19}$$

This transfer function, in the s-domain, is obtained considering a continuous time signal. Since *MATLAB®* works with discrete time signals, it must be converted to the z-domain. This is done using bilinear transformation, which maps the complex s-plane into the complex z-plane through the substitution:

$$s = 2 \cdot f_{ss} \frac{z-1}{z+1}. \tag{3.20}$$

In Eq. (3.20), f_{ss} is the equivalent sampling frequency at which the voltage at the capacitor is computed by *MATLAB®*. It depends on the sampling frequency of the modulator (f_s) and of the accuracy (number of points) desired. A thousand points was deemed sufficient for the computation, done using the *filter* function, available in *MATLAB®*. This simulates the charging or discharging of the capacitor during the period it is sampling the voltage of the input signal of the previous stage. Only the last value obtained in this process is important and is sampled by the next stage or passed to the comparator. Thermal noise is also added to the input signal of the capacitor. The thermal noise originates mostly from the resistor and its standard deviation voltage can be calculated by:

$$v_{N_R} = \sqrt{\frac{4 \cdot k \cdot T \cdot R}{2 \cdot T_{ss}}} \quad \text{(V)}. \tag{3.21}$$

In Eq. (3.20), k is the Boltzmann constant, T is the temperature, and T_{ss} is the estimation period ($1/f_{ss}$). An ambient temperature of 370 K was considered.

The comparator is modeled through the *sign* function, which returns 1 if the input is greater than 0 or -1 if it is lower, which corresponds to the logical high and low values. An offset voltage can also be added in order to make the comparator's behavior more real. The feedback is obtained by multiplying this logical value by the reference voltage and a feedback gain, and subtracting the result to the input of the RC filter. The differential pair used between stages is implemented simply by multiplying the output of the first stage by its gain, G_2, and passing it to the second stage. Listing 3.1 shows the *MATLAB*® code for the main loop of the modulator's model.

Listing 3.1 Main loop of the second order $\Sigma\Delta$M model

```
% Second order Sigma Delta Modulator main loop

%filter coefficients for the first RC circuit
a=[C1*Ron 1];
b=1;
[zB1,zA1]=bilinear(b,a,1/Tss1);

%filter coefficients for the second RC circuit
a2=[C2*R2 1];
b2=1;
[zB2,zA2]=bilinear(b2,a2,1/Tss2);

for i=2 : number_points

  % Comparator output
  dout(i) = sign( Vc2(i-1) + Voffset );

  % Noise generation (npn=number of points in estimation)
  VnR1 = randn(1,npn) * sqrt( 4*k*T*R1 / (2*Tss1) );
  VnR2 = randn(1,npn) * sqrt( 4*k*T*R2 / (2*Tss2) );

  % First integrator response
  y1 = filter( zB1 , zA1 , VnR1 + Vin(i) - Vref*dout(i) , ...
        Vc1(i-1));
  Vc1(i) = y1(end);

  % Second integrator response
  y2 = filter( zB2 , zA2 , VnR2 + G2*Vc1(i) - ...
        Vref*Gfb1*dout(i) , Vc2(i-1) );
  Vc2(i) = y2(end);

end
```

The model of the third order MASH modulator was created from the second order one by adding a third integrator to the main loop, representing the first order $\Sigma\Delta$M of the second stage, and implementing a model of the digital cancellation logic. This DCL model was created by transforming its transfer function, obtained

through Fig. 3.7, into difference equations and implementing them in a loop which uses as input, the output signals of the modulators of each stage. The model of the third $\Sigma\Delta$M is shown in Listing 3.2 and the model of the DCL is shown in Listing 3.3.

Listing 3.2 Main loop of the third order MASH $\Sigma\Delta$M model

```
%filter coefficients for the first RC circuit
a=[C1*Ron 1];
b=1;
[zB1,zA1]=bilinear(b,a,1/Tss1);
%filter coefficients for the second RC circuit
a2=[C2*R2 1];
b2=1;
[zB2,zA2]=bilinear(b2,a2,1/Tss2);
%filter coefficients for the third RC circuit
a3=[C3*R3 1];
b3=1;
[zB3,zA3]=bilinear(b3,a3,1/Tss3);

% Third order Sigma Delta Modulator main loop
for i=2 : number_points

  % First stage comparator output
  dout1(i) = sign( Vc2(i-1) + Voffset );

  % Second stage comparator output
  dout2(i) = sign( Vc3(i-1) + Voffset );

  % Noise generation (npn=number of points in estimation)
  VnR1 = randn(1,npn) * sqrt( 4*k*T*R1 / (2*Tss1) );
  VnR2 = randn(1,npn) * sqrt( 4*k*T*R2 / (2*Tss2) );
  VnR3 = randn(1,npn) * sqrt( 4*K*T*R3 / (2*Tss3) );

  % First integrator response
  y1 = filter( zB1 , zA1 , VnR1 + Vin(i) - Vref*dout(i) , ...
        Vc1(i-1));
  Vc1(i) = y1(end);

  % Second integrator response
  y2 = filter( zB2 , zA2 , VnR2 + G2*Vc1(i) - ...
        Vref*Gfb1*dout(i) , Vc2(i-1) );
  Vc2(i) = y2(end);

  %Third integrator response
  y3 = filter( zB3 , zB3 , VnR3 + Gmid*vc2(i) - ...
        Vref*Gfb2*dout2(i) , Vc3(i-1));
  vc3(i)=y3(end);

end
```

Listing 3.3 Implementation of the DCL block

```
%DCL coefficients
alpha1 = Ts / (2*R1*C1);
alpha2 = Ts / (2*R2*C2);
alpha3 = Ts / (2*R3*C3);

beta1 = 1-alpha1;
beta2 = 1-alpha2;
beta3 = 1-alpha3;

%Digital Cancellation Logic Loop
for i=3:number_points

  %output of the STF block
  out_stf(i)  = ( alpha3*Gcomp2*dout1(i-1) ) / Gcomp1 + ...
          ( (-Gfb2*Gcomp2*alpha3+beta3)*out_stf(i-1) );

  %input of the NTF block
  in_ntf(i)   = out_stf(i) - dout2(i)/Gmid;

  %output of the NTF block
  out_ntf(i)  = in_ntf(i) - ( beta2+beta1 )*in_ntf(i-1) + ...
          ( beta1*beta2 )*in_ntf(i-2) - ...
          ( Gcomp1*alpha2*b22-beta1-beta2 )*out_ntf(i-1) - ...
          ( beta1*beta2 - Gcomp1*alpha2*beta1*Gfb1 + ...
          Gcomp1*G2*alpha2*alpha1 )*out_ntf(i-2);

  %final output
  dout_MASH(i) = out_stf(i) - out_ntf(i);

end

%NOTE: Gfb2 is the feedback gain of the first order modulator
%      of the second stage
```

3.5 Optimization

The objective of the optimization is to adjust the various parameters of the modulator in order to make it achieve a maximum SNDR of at least 80 dB. The power consumption and area of the modulator are not included in the model, so in order to try to minimize both, some constraints were considered for the values of the parameters. The values of the capacitors and resistors affect their size, so their values must be minimized in order to reduce the modulator's area. The clock frequency and the gain of the amplifier affect the overall power consumption of the modulator. To minimize it, these parameter's values must also be minimized. Table 3.1 shows the parameters that were subject to optimization, as well as their respective base values and range. This approach was applied to the model of the second order $\Sigma\Delta$ modulator.

Table 3.1 Optimization parameters and their values

Parameter	R_1	C_1	$\alpha 1$	R_2	C_2	$\alpha 2$	f_s	G_2	b_{22}
Range	100–2000	0.5–10	0.005–0.1	100–2000	0.5–10	0.005–0.1	1–10	6–10	0.01–0.1
Base value	2000	10	0.005	2000	10	0.005	5	6	0.5
Unit	kΩ	pF	–	kΩ	pF	–	MHz	–	–

To obtain the SNDR, a sine wave signal of 2 kHz and amplitude inferior to $V_{\text{REF}} = 1.1$ V is applied to the model. The FFT of the output is calculated, using Blackman–Harris window, and the SNDR is obtained through the ratio of the power of the input signal and the noise and distortion power, considering the bandwidth of the modulator to be 20 kHz:

$$\text{SNDR} = \left.\frac{P_{\text{signal}}}{P_{\text{noise}} + P_{\text{distortion}}}\right|_{B=20\,\text{kHz}} \quad (\text{dB}) \tag{3.22}$$

To increase the precision of the results, this process is repeated several times, specifically ten times, and the final result of the SNDR is an average of these repetitions. The number of points used for the calculation of the FFT determines the precision of the model. Through simulation, it was determined that for more than 20,000 points the precision does not increase significantly, so that was the number chosen.

To obtain the maximum SNDR of the modulator, its DR must be calculated. This is done by varying the amplitude of the input signal, and calculating the SNDR for each of the values of amplitude. Figure 3.9 shows the plot of the DR of the modulator for the parameter's base values. The peak SNDR is 75.42 dB. It is highlighted the point at which the SNDR is maximum and the point at which the SNDR is 0 dB. From these two points, the DR obtained is $20 * \log_{10}(^{1.08}/_{5.75*10^{-4}}) = 65.48$ dB. The DR plot is obtained from 200 points. From 10^{-7} to 0.4 V there are 100 logarithmically spaced points and the remaining 100 points are spaced linearly from 0.4 V and V_{ref}.

The optimization of the modulator was done by varying each parameter listed in Table 3.1 individually, keeping the base values for the others, between the values also listed in the same table, and calculating the DR for each value. Through this process, the way each individual parameter affects the SNDR of the output becomes apparent.

As seen in a previous section, the parameters α_1 and α_2 depend on the values of the corresponding capacitor and resistor. This means these parameters can vary in two ways, by varying the value of the resistor or the value of the capacitor. Both of these approaches were considered and the range of the variation of the components was chosen so that the parameter α would vary between the values listed in Table 3.1. In Fig. 3.10 is plotted the DR as function of the capacitor C_1 and in Fig. 3.11 is the DR as function of the resistor R_1. Figure 3.12 shows the effect of the capacitor C_2 and Fig. 3.13 of the resistor R_2. The variation of these parameters

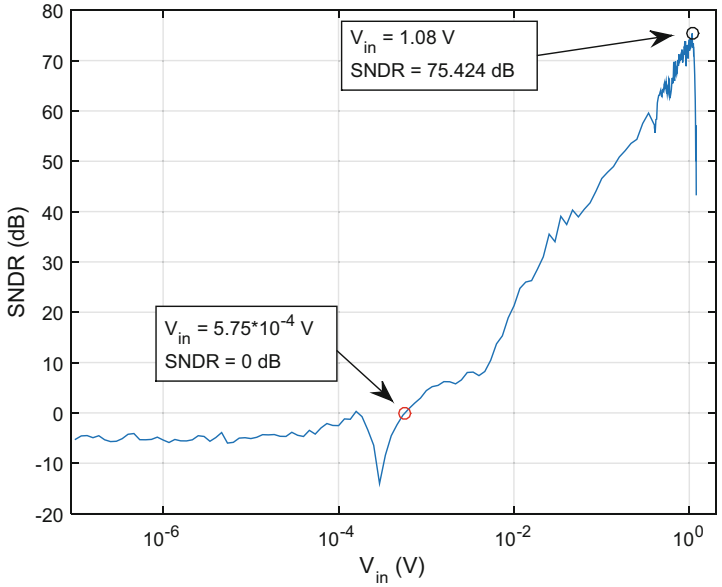


Fig. 3.9 Dynamic range of the second order model using the base parameters

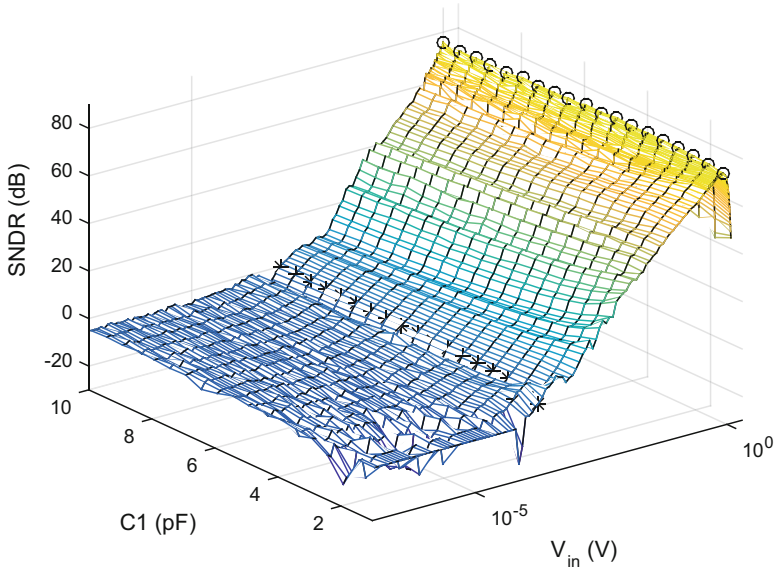


Fig. 3.10 Dynamic range of the second order model as function of C_1

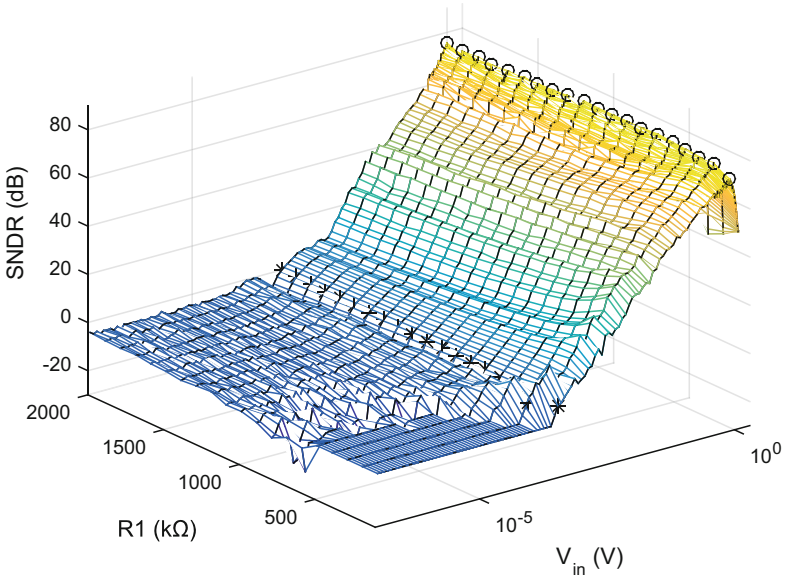


Fig. 3.11 Dynamic range of the second order model as function of R_1

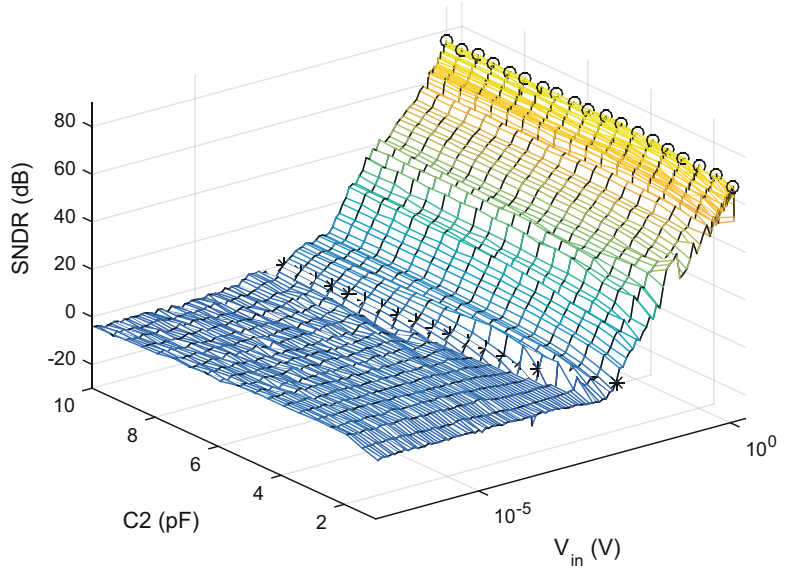


Fig. 3.12 Dynamic range of the second order model as function of C_2

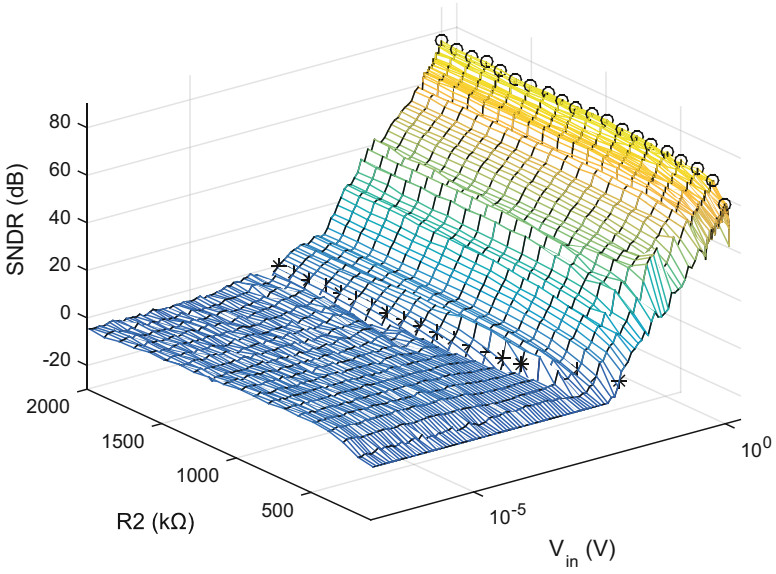


Fig. 3.13 Dynamic range of the second order model as function of R_2

Table 3.2 Maximizing values of capacitors and resistors

Parameter	C_1	R_1	α_1	C_2	R_2	α_2
Optimal value	4.5 pF	2000 kΩ	0.0056	9 pF	2000 kΩ	0.0028
Maximum SNDR	77.58 dB	78.57 dB	–	75.89 dB	75.95 dB	–

was done using 20 points linearly spaced between 0.5 and 10 pF in the case of the capacitors, and between 100 and 2000 kΩ for the resistors, which corresponds to a variation of the parameters α_1 and α_2 between 0.005 and 0.1, as shown in Table 3.1.

The values of these parameters that maximize the SNDR, for each individual simulation, are shown in Table 3.2, along with the corresponding maximum SNDR achieved in each simulation.

The remaining parameters to optimize are the clock frequency (f_s), the gain of the amplifier between stages (G_2), and the feedback gain of the second stage (G_{fb1}). The dynamic range as function of the clock frequency is shown in Fig. 3.14. Ten points linearly spaced between 1 and 10 MHz were used for the simulation. The results show that an increase in the clock frequency leads to an increase in the SNDR of the modulator. The downside is that it also leads to an increase in power consumption. The upper limit for the frequency was fixed at 10 MHz with the purpose to attenuate this problem. For this frequency value, and a bandwidth of 20 kHz, the OSR of the modulator is 250.

The variation of the gain of the amplifier used between the stages, G_2, was between 1 and 10, using 10 points with linear spacing. Once again, the range was chosen with the minimization of the power consumption. In Fig. 3.15 is plotted the dynamic range of the modulator as a function of this gain.

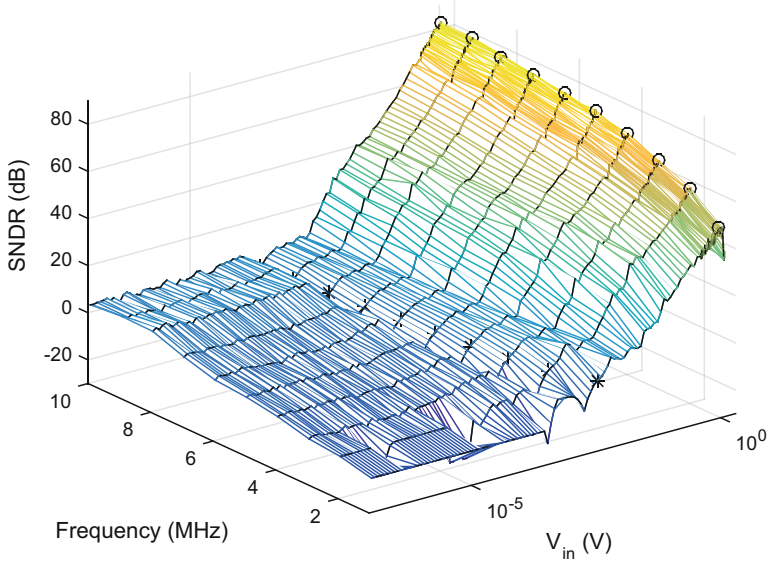


Fig. 3.14 Dynamic range of the second order model as function of f_s

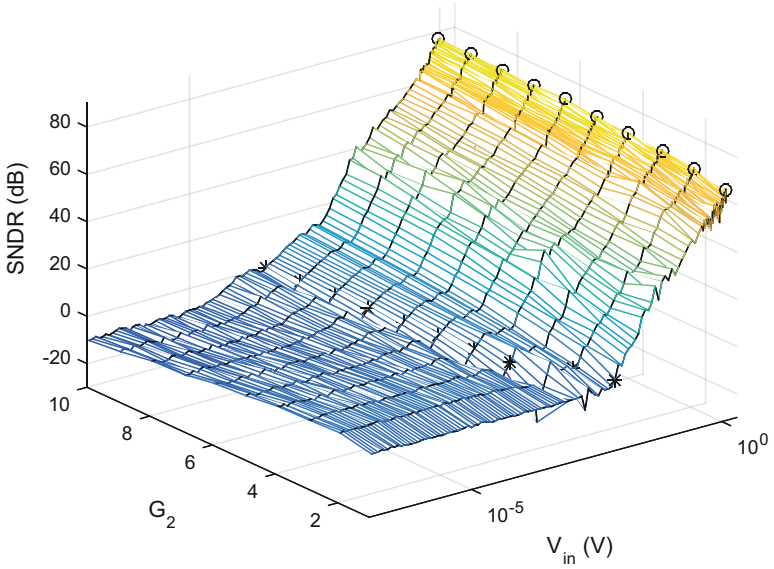


Fig. 3.15 Dynamic range of the second order model as function of G_2

Lastly, the optimization of the second stage feedback path's gain, G_{fb1} was done using 20 linearly spaced points between the values 0.01 and 1. Figure 3.16 shows the results of this simulation.

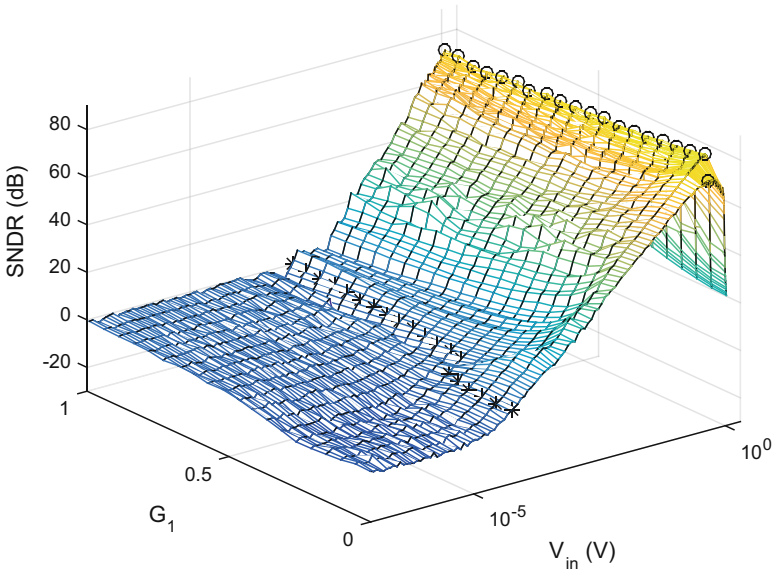


Fig. 3.16 Dynamic range of the second order model as function of G_{fb1}

Table 3.3 Maximizing values of f_s, G_2 and G_{fb1}

Parameter	f_s	G_2	G_{fb1}
Optimal value	10 MHz	10	0.0621
Maximum SNDR (dB)	82.56	76.82	81.20

In Table 3.3 is listed the maximum SNDR achieved in each of these simulations, with the correspondent optimal value of the parameter.

Using the results obtained in these previous simulations, shown in Tables 3.2 and 3.3, a simulation was made which yielded the results plotted in Fig. 3.17. A SNDR of 85.16 dB was achieved, with an 85.87 dB of dynamic range. The parameters were then adjusted in order to maximize the SNDR, based on the obtained results as how each parameter affects this value, and, at the same time, achieve the secondary goals of minimizing both the power consumption and the area of the modulator. With this in mind, the value of the gain of the amplifier between stages, G_2, was chosen as 6, since for greater values, the maximum SNDR achieved was not significantly increased, as seen in Fig. 3.15. Both resistors were also adjusted to the value of 900 kΩ. The remaining parameters, capacitors C_1 and C_2, clock frequency, f_s, and second stage feedback gain, G_{fb1}, retained the values obtained through simulation. In Table 3.4 are listed the adjusted values of the parameters used in this simulation, which achieved a SNDR value of 86.84 dB and a dynamic range of 87 dB, as shown in Fig. 3.18.

The optimization of the third order MASH $\Sigma\Delta$M was done using a different model. This model takes into account the thermal, quantization, and comparator noises of the modulator and a Monte-Carlo analysis is performed at each iteration,

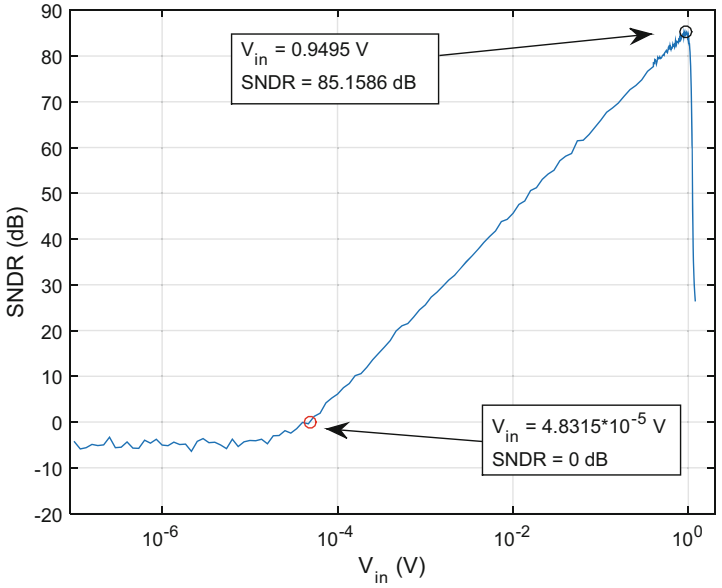


Fig. 3.17 Dynamic range of the second order model with maximizing values

Table 3.4 Adjusted second order model parameters

Parameter	C_1	R_1	α_1	C_2	R_2	α_2	f_s	G_2	G_{fb1}
Value	9 pF	900 kΩ	0.0123	4.5 pF	900 kΩ	0.0062	10 MHz	6	0.0621

where process and mismatch variations of the components are included, to calculate an average SNDR. The optimization is done using a genetic algorithm to maximize the SNDR. This model is based on the one used in [14], which uses the work developed in [16]. This optimization was done for a sampling frequency of 10 MHz and a signal bandwidth of 20 kHz, and the obtained values for the components are shown in Table 3.5. In these conditions, the expected maximum SNDR is 97.46 dB.

The gain G_{fb2} corresponds to the feedback gain of the first order modulator used in the second stage.

To validate the results obtained through optimization, these parameters values where used in the third order model described in the previous section. The resulting DR is 104.3 dB, as shown in Fig. 3.19, resulting in a maximum SNDR of 104.2 dB. This increase in maximum SNDR is explained by the fact that the model used to verify the optimization process is less precise in terms of noise.

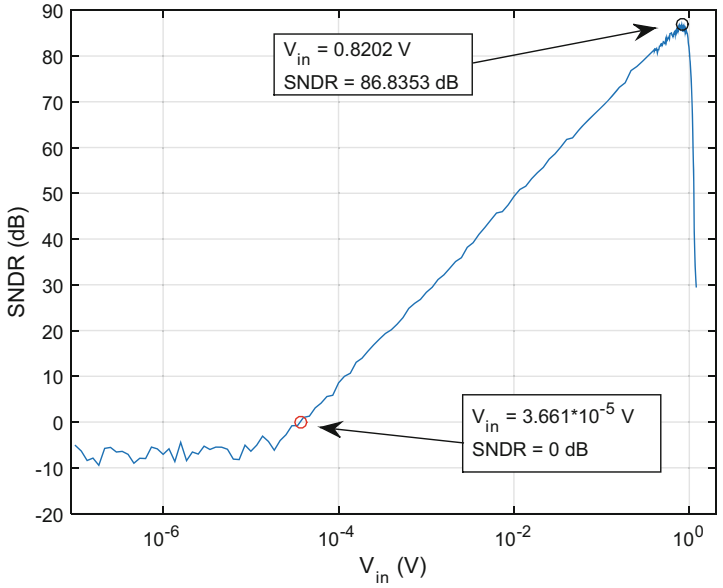


Fig. 3.18 Dynamic range of the second order model with adjusted values

Table 3.5 Optimized third order model parameters

Parameter	R_1	C_1	α_1	R_2	C_2	α_2	R_3	C_3	α_3
Value	34.4 kΩ	99 pF	0.0147	30.9 kΩ	100 pF	0.0162	950 kΩ	8 pF	0.0066

Parameter	G_{fb1}	G_2	G_{fb2}	G_{mid}	f_s	B
Value	0.22	10	0.154	10	10 MHz	20 kHz

3.6 Reducing the Size of the Capacitors

The values of the capacitors obtained through optimization are larger than the maximum value of 10 pF imposed in this project. This leads to an increase of the total area of the circuit. Looking at the expression of the α parameter, repeated here in Eq. (3.23), it is clear that in order to reduce the capacitor value, either the resistor value is increased proportionally or the sampling period is reduced. It is worth noting the factor $1/2$, which reflects the duration of the integration, half of the sampling period.

$$\alpha = \frac{T_s}{2 \cdot C \cdot R}. \tag{3.23}$$

Since increasing the value of the resistor also leads to an increase in the area, the chosen approach was to reduce the sampling period. The easiest way to do so is to increase the sampling frequency, which was not considered since it leads to an

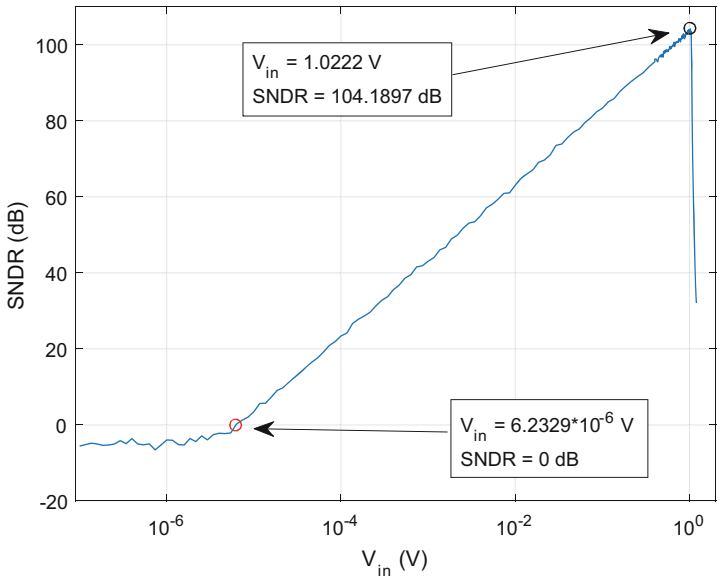


Fig. 3.19 Dynamic range of the third order model with optimized values

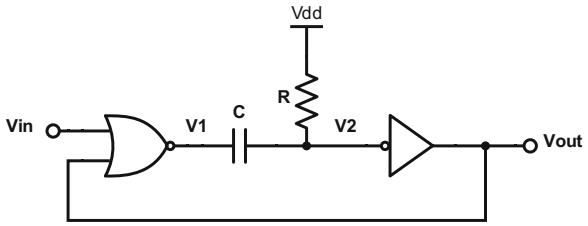


Fig. 3.20 Schematic of a monostable circuit. Adapted from [6]

increase in overall power consumption. The solution is to maintain the sampling frequency, and reduce the sampling time of the capacitor. This is done using a monostable circuit.

The monostable is a type of digital circuit which is only stable in one output state, either *high* or *low*. When a trigger impulse is applied, it produces an output pulse with a fixed duration, which is typically defined by a time constant of an RC circuit, returning to the stable state until it is re-triggered. In Fig. 3.20 is shown a possible implementation of this circuit.

In its stable state, with V_{in} *low*, the NOR gate output, V_1, is *high* and voltage in node V_2 is pulled *high* through the resistor, which makes the output of the monostable, V_{out}, *low*. When a trigger impulse is applied, that is the signal V_{in} goes *high*, the voltages V_1 and V_2 both go *low*, making the output go *high*, holding the voltage V_1 *low*, through the NOR gate. The capacitor starts charging through the resistor and its voltage is given by Eq. (3.24).

$$V_C(t) = V_2(t) - V_1(t) = V_{dd} \cdot (1 - e^{-t/\text{RC}}) \tag{3.24}$$

Considering that the inverter switching point voltage is $V_{dd}/2$, then the time it takes the capacitor to charge to this voltage is given by Eq. (3.25).

$$t = \mathrm{RC} \cdot \ln\left(\frac{V_{dd}}{V_{dd} - V_{dd}/2}\right) = \mathrm{RC} \cdot \ln(2) \approx 0.7\mathrm{RC} \tag{3.25}$$

This time defines the output pulse width, since it makes the inverter switch to *low*, causing voltage V_1 to go to *high* and V_2 to $V_{dd} + V_{dd}/2$. The time the capacitor takes to discharge back to V_{dd} defines the rate at which the monostable can be re-triggered. The trigger pulse can be longer than the output pulse, which is intended in this project [6, Sec 18.2, p. 529].

To reduce the capacitance values used in the MASH modulator to the limit of 10 pF defined for this project, the monostable must generate an output pulse ten times smaller than the clock phase. A 10 MHz sampling frequency has a 100 ns period, with a 50 ns of *high* time. The monostable uses this signal as input trigger and produces a 10 MHz signal, but with only 5 ns *high* time. In the model, this is done by calculating the sampling period as:

$$T_s = \frac{1}{10} \cdot \frac{1}{f_s}. \tag{3.26}$$

This affects the estimation period of the capacitors voltage (T_{ss}), which in turn affects the thermal noise generated by the resistors. Since the capacitors values are reduced in the same proportion, the α parameters remains the same. The exception is α_3, because the capacitor of the third integrator, C_3, already has a value between the imposed limits, so it was not changed. This results in a α_3 value ten times inferior ($\alpha_3 = 0.00066$). The new values for the capacitors are $C_1 = 9.9\,\mathrm{pF}$ and $C_2 = 10\,\mathrm{pF}$.

The DR obtained through the third order MASH model in these conditions has a value of 95.57 dB and a maximum SNDR of 94.62 dB, as shown in Fig. 3.21. These results show a decrease of about 10 dB in both maximum SNDR and DR, when compared with the model without the monostable circuit. The ten times decrease in sampling period results in a ten time increase in thermal noise generated by the resistors, leading to a 10 dB increase on the overall noise, since this is only noise source considered. Nevertheless, these results are within the desired specifications, and as such show that the use of a monostable circuit to reduce the size of the components without compromising performance is a valid approach.

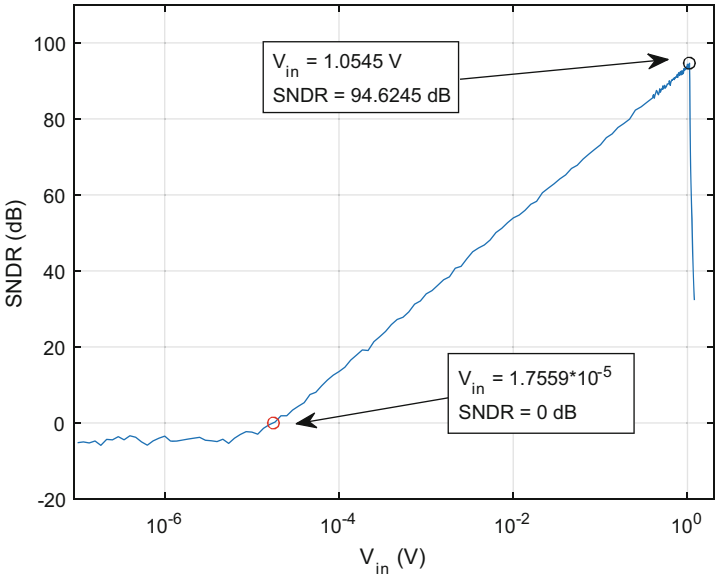


Fig. 3.21 Dynamic range of the third order model with the monostable circuit

Chapter 4
Electrical Circuits and Simulation Results

4.1 Introduction

In this chapter it will be discussed and explained in detail the electrical circuits used in the construction of the Sigma-Delta Modulator based on the UIS approach. Figure 4.1 presents a complete schematic of the first and second stages of the third order MASH modulator, composed of a second and first order $\Sigma\Delta$ modulators, respectively. It is also presented the clock circuitry and the switch circuitry timing and control. These circuits were designed in a standard 65 nm CMOS technology with a power supply voltage value of 1.1 V and using standard voltage threshold (V_{th}) transistors. The circuits were subject to electrical transient-noise simulations using the *Virtuoso Platform*, an EDA software developed by Cadence Design Systems.

4.2 Digital Circuitry

4.2.1 Logic Gates

Logic gates are the building blocks of digital systems. They take one or various input signals and produce an output expressing a certain boolean logic between them. This is generally achieved by using CMOS transistors acting as electronic switches, and using PMOS and NMOS transistors in complementary and symmetrical pairs.

One of the simplest and more widely used logic gates is the inverter, or NOT gate, which produces an output which is the logical counterpart of its input signal. It is implemented using two transistors, one PMOS and the other a NMOS, as seen in Fig. 4.2a. To maximize its switching speed, the transistors are designed with the minimum length and width allowed by the used technology. However,

D. Fouto, N. Paulino, *Design of Low Power and Low Area Passive Sigma Delta Modulators for Audio Applications*, SpringerBriefs in Electrical and Computer Engineering, DOI 10.1007/978-3-319-57033-4_4

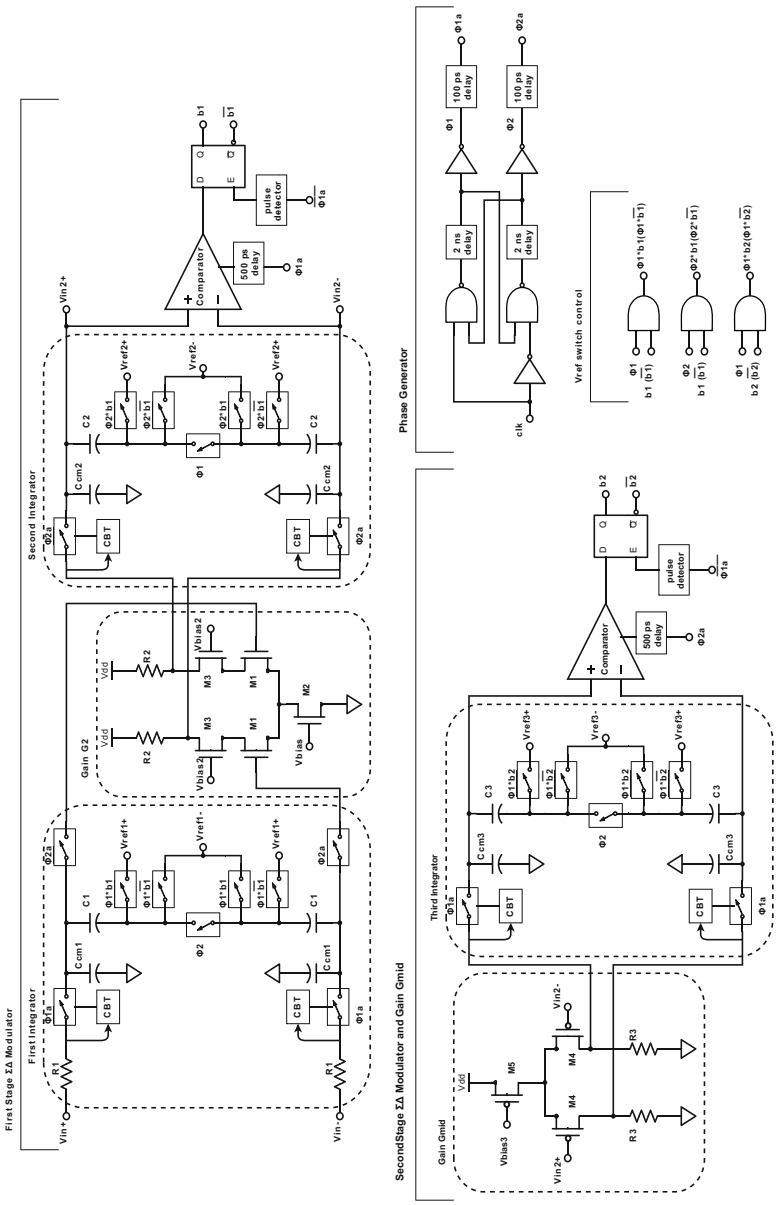


Fig. 4.1 Complete schematic of the first and second stages of the third order MASH $\Sigma\Delta$M with clock circuitry

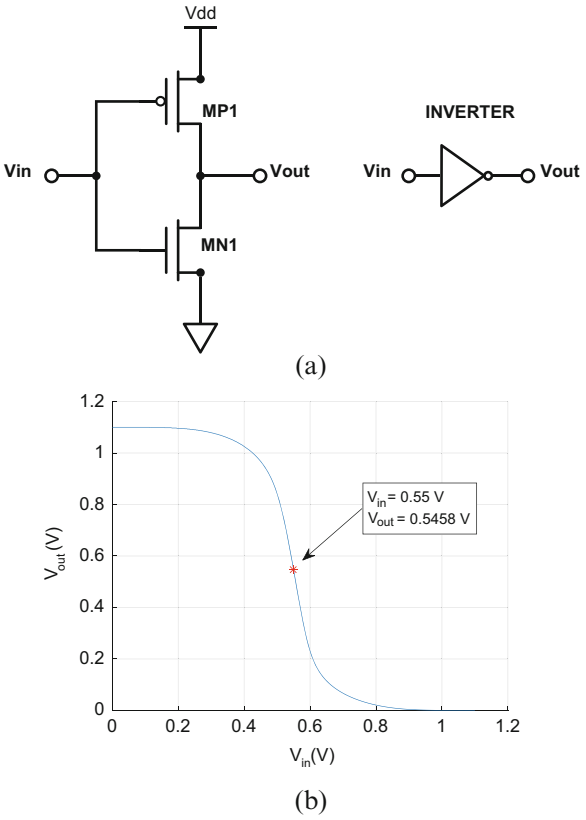


Fig. 4.2 CMOS implementation and symbol of the inverter logic gate (**a**) and its characteristic response (**b**)

since PMOS transistors are "weaker" than the NMOS ones, they must have a larger width in order for the inverter switching point voltage be at half the power supply voltage. This occurs when the width of the PMOS transistors is 2.5 times that of its NMOS counterpart, for the technology used. This ratio of the transistor's width is maintained in the rest of the digital circuits. Figure 4.2b shows the output of the inverter as function of its input, where it can be seen that its switching point voltage is at half the power supply voltage (1.1 V).

Another logic gate designed was the NAND gate, which is considered an "universal gate," since it can be used to make any logic gate or function, if enough gates are available. Figure 4.3 shows its implementation using CMOS transistors and in Table 4.1 is shown its truth table. This gate, in combination with the inverter, was used to implement all the digital logic used in this project, like AND gates, shown in Fig. 4.4a, and the *flip-flops*, discussed in a later section.

4.2.2 Delay Circuits

In order to guarantee a stable operation of the modulator, some synchronization of the switching circuitry is required. For instance, when in the same clock phase, some

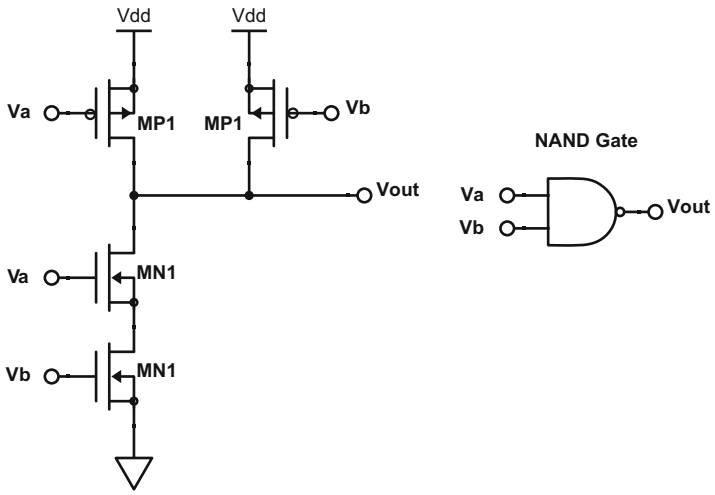
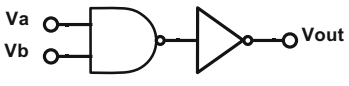


Fig. 4.3 CMOS implementation of a NAND gate and its symbol

Table 4.1 NAND gate truth table

V_a	V_b	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 4.4 Implementation of an AND gate using NAND and inverter gates (**a**) and its truth table (**b**)



(a)

V_a	V_b	V_{out}
0	0	0
0	1	0
1	0	0
1	1	1

(b)

switches must close after others to allow voltage stabilization in the capacitors. This is done by delaying the clock signal for those switches. This is achieved by using the inherent signal delay introduced by an inverter gate. The delay circuit is composed of two inverters in series. The first inverter is "weaker," taking some time to respond to a change in its input signal. The second one is "stronger" and quickly responds to a change in its input signal, which is the output of the first inverter. Changing the sizes of the transistors of the inverters changes the delay that this circuit provides. Figure 4.5 shows the input and output signals of the delay circuit, as well as the output signal of the first inverter (V_{mid}), for a rising edge of the input signal.

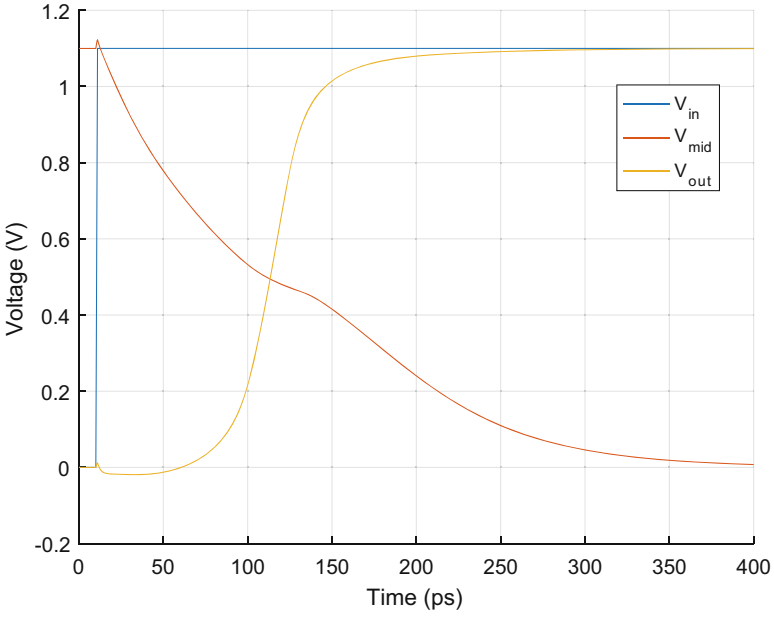


Fig. 4.5 Simulated input, output and first inverter output signals of the delay circuit

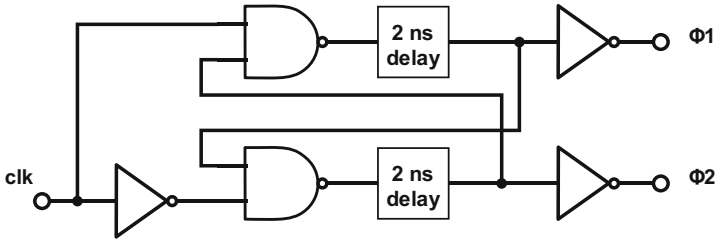


Fig. 4.6 Schematic of the phase generator circuit

The circuit was designed to produce a delay close to 100 ps. To produce higher delay times, a series of these circuits is used, resulting in a delay of $n \times 100$ ps, where n is the number of delay circuits used.

4.2.3 Phase Generator

The schematic of the phase generator circuit is presented in Fig. 4.6. It consists of a pair of two cross coupled NAND gates and delay circuits, and generates two non-overlapping square signals with frequency equal to the input clock signal. The delay circuits are used to define the non-overlapping time.

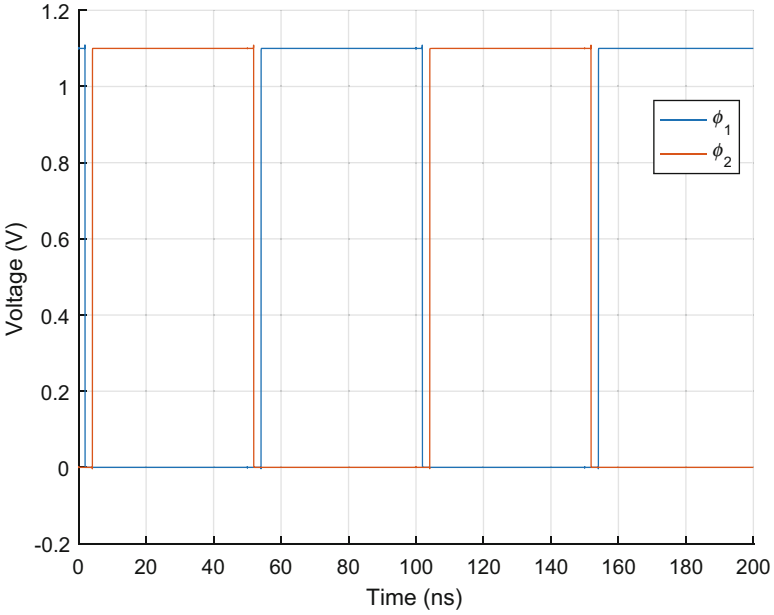


Fig. 4.7 Simulated output of the phase generator circuit

The output of this circuit is shown in Fig. 4.7 for a square input signal with frequency 10 MHz and a duty cycle of 50%.

4.2.4 Flip-Flop

In order to save the output of the modulator, which is used in the next clock cycle, a *flip-flop* is needed. This circuit uses a synchronous D latch to store information in the cross coupled NOR gates. These gates are constructed using inverter and NAND gates, as shown in Fig. 4.8. A pulse detector responds to the rising edge of the clock signal by generating a small pulse which causes the latch to store the information at its input. The delay circuit defines the width of this pulse. Figure 4.9 shows the schematic of the *flip-flop*.

The pulse detector generates a pulse with a width of nearly 100 ps, enough for the latch to save the information. Figure 4.10 shows its output to a rising edge of the input signal.

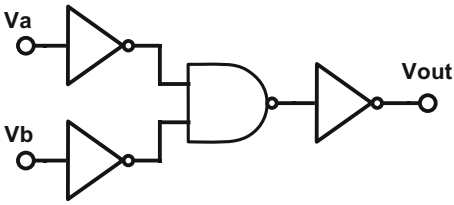


Fig. 4.8 A NOR gate constructed with NAND and inverter gates

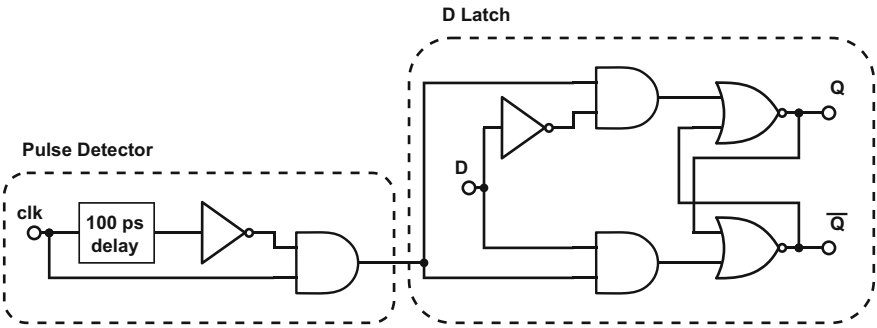


Fig. 4.9 Schematic of the *flip-flop*

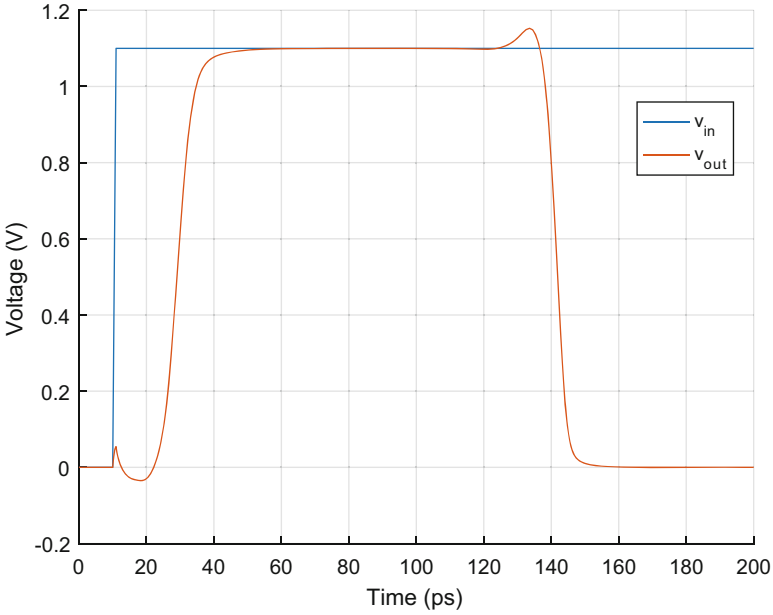


Fig. 4.10 Output of the pulse detector circuit

4.3 Amplifiers

Although an objective of this project was designing a passive $\Sigma\Delta$ modulator, which does not need a high gain amplifier to perform integration, two low gain amplifiers are still needed. Their main function is not signal amplification, but to isolate the capacitors of adjacent integrators. This is required to avoid partial charge redistribution between them, when one is sampling the voltage from the previous integrator. The amplifiers are implemented with a simple common source differential pair loaded by resistors topology. The resistors are not only the load of the gain stages but are also part of the following integrator RC time constant.

4.3.1 Gain G_2

One amplifier is used to isolate the two integrators of the second order $\Sigma\Delta$M, used in the first stage of the MASH modulator, and its schematic is shown in Fig. 4.11. It uses a differential cascode common source topology using NMOS transistors loaded by resistors. The cascode configuration is used to increase the output resistance of the amplifier, thus better isolating the two integrators. Using the hybrid-pi model of the MOS transistor for small signals, the voltage gain of the amplifier is given approximately by:

$$A_v = \frac{v_{\text{out}}}{v_{\text{in}}} \approx -2 \cdot g_{m1} \cdot R_2. \tag{4.1}$$

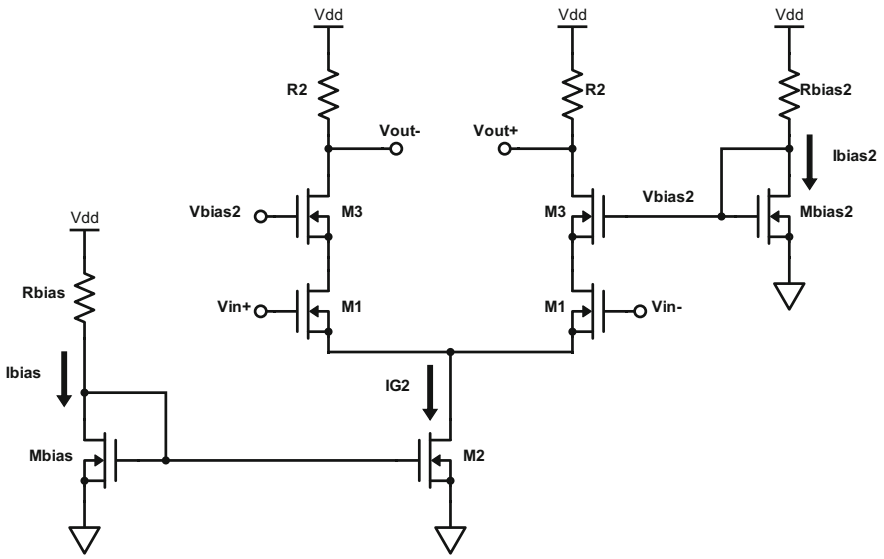


Fig. 4.11 Schematic of the G_2 amplifier

In Eq. (4.1), g_{m1} is the transconductance of transistor $M1$. The two factor comes from the use of a balanced differential pair. Since resistor R_2 is also used in the RC constant of the next integrator, its value is fixed, and was obtained previously by optimization. So to obtain the desired gain, transistor $M1$'s g_m must be adjusted. This value is dependent on the DC drain-source current (I_D), gate-source (V_{GS}), and threshold (V_{th}) voltages of the transistor:

$$g_m = \frac{2 \cdot I_D}{V_{\text{GS}} - V_{\text{th}}}. \tag{4.2}$$

Since the modulator uses a common mode voltage of half the power supply voltage, the amplifier is expected to maintain this value at its output. However, this means the transistors $M1$ and $M3$ do not have enough voltage to work in saturation mode ($V_{\text{GS}} > T_{\text{th}}$ and $V_{DS} \geq (V_{\text{GS}} - T_{\text{th}})$), and the amplifier does not work. The common mode voltage is then increased to almost 700 mV, which is not a problem for the following circuits, since the signals have low amplitude. The common mode voltage at the output is given by:

$$V_{\text{CM}_{\text{out}}} = V_{dd} - (I_{R_2} * R_2) \tag{4.3}$$

The current of the resistor R_2, which is the same as the transistor $M1$'s, I_{D_1}, is chosen to produce the desired common voltage at the output. This current is set by transistor $M2$, through which passes current I_{G_2} that has double the value of I_{D_1}. Transistor M_{bias} mirrors its current, I_{bias}, to transistor $M1$ with a ratio 1:10. This is done by making M_{bias}'s width about ten times smaller than $M2$'s. This is explained by considering the expression of the DC current of a MOS transistor in saturation mode:

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{\text{GS}} - V_{\text{th}})^2 \tag{4.4}$$

The only free variable between these two transistors is the ratio $\frac{W}{L}$, since V_{GS} of M_{bias} is mirrored to $M2$ and the remaining parameters are technology dependent, meaning an increase in the width of transistor $M2$ will produce an increase in its current, when compared with the current of M_{bias}.

Transistor M_{bias2} is used to polarize the cascode transistor $M3$ to the saturation zone, also affecting transistor $M1$. A balance of the sizing of these three transistors must be achieved in order to $M1$ and $M3$ work in saturation mode, the target gain is achieved and a minimum I_{bias2} current is used.

The voltage gain of the amplifier is defined as the differential ratio between the output and the input signals:

$$A_v = \frac{v_{\text{out}+} - v_{\text{out}-}}{v_{\text{in}+} - v_{\text{in}-}}. \tag{4.5}$$

Two gain G_2 amplifiers were designed, one to use in the standalone second order $\Sigma\Delta$M and the second to be used in the second order $\Sigma\Delta$M implemented as the first stage of the third order MASH modulator. Tables 4.2 and 4.3 present the sizes of the components used in each amplifier, and Figs. 4.12 and 4.13 show the graphs of the voltage gains of each, as function of the differential input voltage.

4.3.2 Gain G_{mid}

This gain stage is used to isolate the two stages of the MASH modulator and provide some amplification, since the output signal of the second integrator of the first stage has very low amplitude. It also uses a differential common source topology, but without the cascode transistors. Due to the increase of the common mode voltage performed by the G_2 amplifier, it uses PMOS transistors to lower it, as shown in Fig. 4.14. Once again, it cannot be set as half of the power supply voltage, because then transistor $M1$ would not have enough voltage to work in saturation mode, so it was set as 480 mV. This value is given by:

$$V_{\text{CM}_{\text{out}}} = I_{R_3} * R_3 \tag{4.6}$$

From Eq. (4.6) the value of the current in transistor $M1$ is determined, since the value of resistor R_3 is set by the optimization process. This current is supplied by a current mirror formed by $M2$ and M_{bias}, with a ratio of 1:1 from I_{bias} to $I_{G_{\text{mid}}}$.

The components sizes and values of the amplifier are shown in Table 4.4 and Fig. 4.15 shows the plot of its gain as function of the input signal.

4.4 Comparator

One bit quantization is used in this project and a comparator is used as the 1-bit quantizer. Due to the passive nature of the integrators, the signal at the input of the comparator has a small amplitude. The comparator must amplify it to a digital level and, as such, must have a large gain. This is done by employing positive feedback, which makes the comparator saturate very rapidly to either V_{dd} or 0 V. The comparator responds to the rising edge of its clock signal and holds the output while the clock is *high*. The comparator used was based on the one from [12], which was adapted from [17], and its schematic is shown in Fig. 4.16.

Table 4.2 Design parameters of the gain stage G_2 used in the second order $\Sigma\Delta$M

	Gain		$\frac{W}{L}$ (µm/µm)					Resistors (MΩ)			lurrent (nA)			
Parameter	Target	Maximum	$M1$	$M2$	$M3$	M_{bias}	M_{bias2}	R_2	R_{bias}	R_{bias2}	I_{G_2}	I_{bias}	I_{bias2}	$V_{\text{cm}_{\text{out}}}$ (V)
Value	6	6.226	$\frac{1}{4}$	$\frac{5}{0,2}$	$\frac{14}{1}$	$\frac{1}{1}$	$\frac{1}{10}$	0.95	11.27	1.295	900	90	400	0.695

Table 4.3 Design parameters of the gain stage G_2 used in the third order MASH $\Sigma\Delta$M

	Gain		$\frac{W}{L}$ (µm/µm)					Resistors (kΩ)			lurrent (µA)			
Parameter	Target	Maximum	$M1$	$M2$	$M3$	M_{bias}	M_{bias2}	R_2	R_{bias}	R_{bias2}	I_{G_2}	I_{bias}	I_{bias2}	$V_{\text{cm}_{\text{out}}}$ (V)
Value	10	10.011	$\frac{21}{0.3}$	$\frac{20}{0.14}$	$\frac{12.11}{0.5}$	$\frac{1}{0.5}$	$\frac{0.5}{10}$	31	343.8	171.5	26	2.6	2.6	0.697

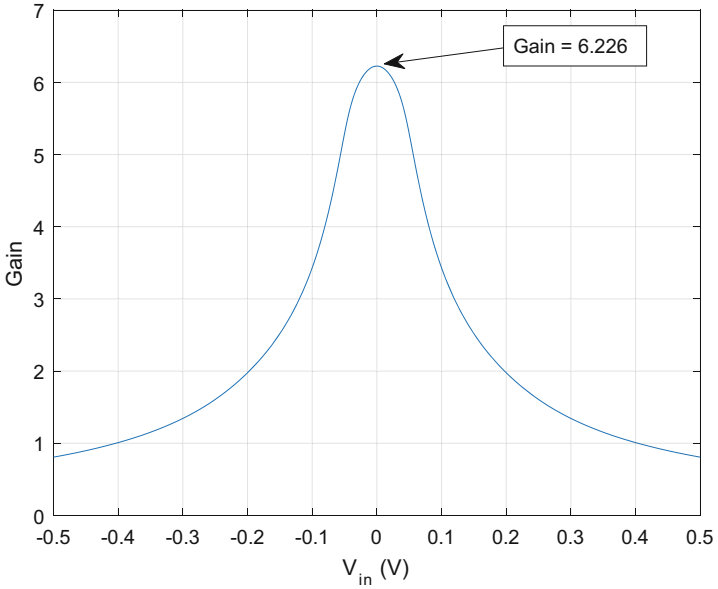


Fig. 4.12 Gain as a function of the differential input voltage of the G_2 amplifier used in the second order $\Sigma\Delta$M

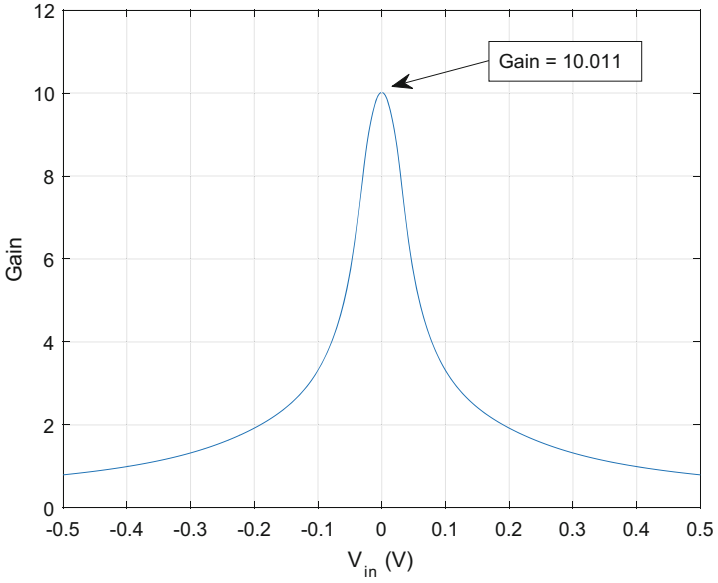


Fig. 4.13 Gain as a function of the differential input voltage of the G_2 amplifier used in the third order MASH $\Sigma\Delta$M

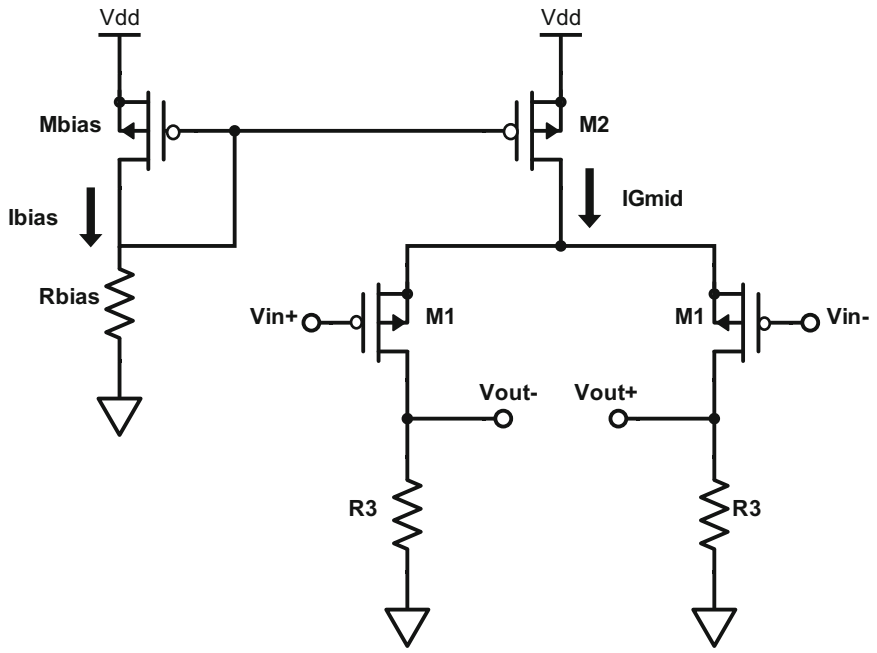


Fig. 4.14 Schematic of the G_{mid} amplifier

Table 4.4 Design parameters of the gain stage G_{mid} used in the third order MASH $\Sigma\Delta$M

	Gain		$\frac{W}{L}$ (µm/µm)			Resistors (kΩ)		lurrent (µA)		
Parameter	Target	Maximum	$M1$	$M2$	M_{bias}	R_3	R_{bias}	I_{G_2}	I_{bias}	$V_{\text{cm}_{\text{out}}}$ (V)
Value	10	10.531	$\frac{4}{1.3}$	$\frac{5.2}{1}$	$\frac{5}{1}$	950	846	1	1	0.482

4.5 Switching Circuitry

Switches are necessary to implement a discrete time SC circuit, setting the timing for charging or discharging capacitors and allowing charge to pass between them. A simple way to implement a switch is using a MOS transistor, either NMOS or PMOS. A clock signal is fed to the gate of the transistor and when it is active, the transistor passes the signal between its source and drain, in either direction. When the clock signal is not active, the transistor does not conduct and its source and drain are in a high impedance state, not allowing the signal to pass.

A switch implemented with a NMOS transistor is active when the clock signal is *high*. Since a NMOS needs at least a V_{GS} voltage equal to the threshold voltage, V_{th_n}, when it passes a high amplitude signal, it does so with a voltage drop. The maximum voltage it can pass is $V_{dd} - V_{\text{th}_n}$. It can be said that it is good at passing a "0" and bad at passing a "1", digitally speaking.

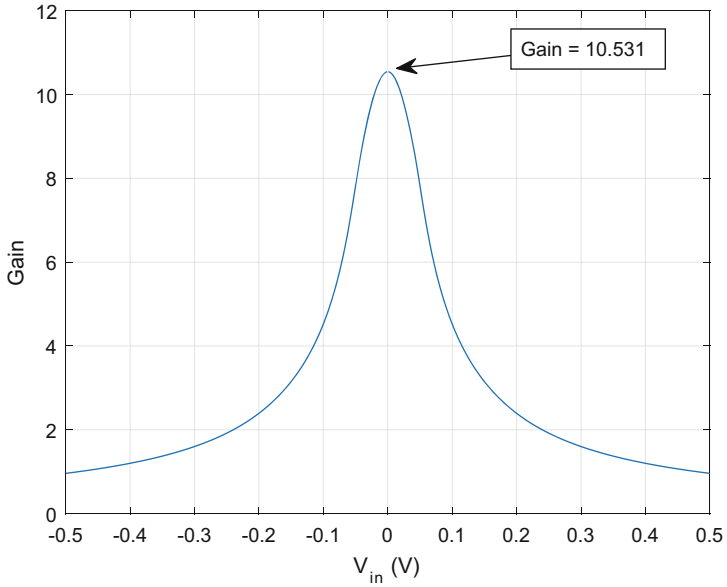


Fig. 4.15 Gain as a function of the differential input voltage of the G_{mid} amplifier used in the third order MASH $\Sigma\Delta$M

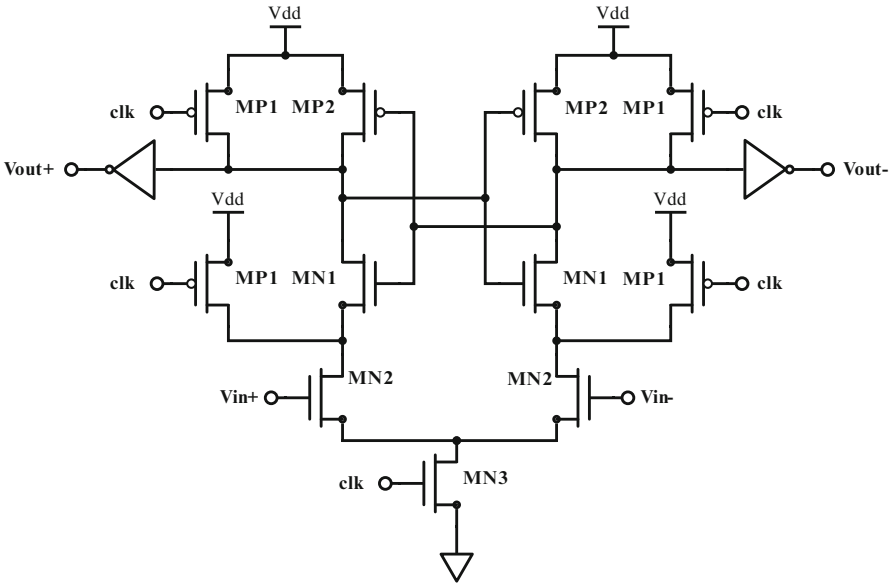


Fig. 4.16 Schematic of the comparator

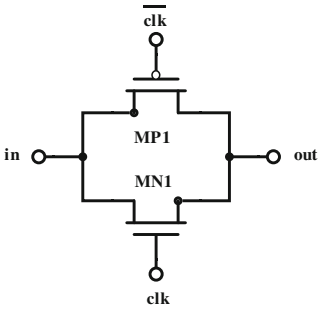


Fig. 4.17 Schematic of the CMOS transmission gate

A PMOS used as switch as the same behavior, but reversed. It is active when the clock signal is *low* and it passes low amplitude signals with a voltage increase, being V_{th_n} the minimum. In terms of digital signals, it can be said it is good at passing a "1" and bad at passing a "0".

Connecting the two complementary MOS transistors in parallel produces a transmission gate, a switch that uses the advantages of both MOS types, canceling their shortcomings, meaning it is good at passing the full range of the signal. This leads to an increase of the layout area and the need to use two control signals, the clock signal and its complement. In Fig. 4.17 is shown the schematic of the transmission gate [6, Sect. 10.2, p. 321].

Another important characteristic of the transmission gate is its on-resistance. It is approximately equal to the parallel of the equivalent resistance of both transistors. This leads to a lower on-resistance which has less variation, when compared to a MOS switch. This leads to a lower harmonic distortion and reduces the switch effect on the RC time constant of the integrators [12, 18].

The sizes of the transistors influence the on-resistance and the total harmonic distortion (THD) of the transmission gate. The objective was to reach a THD of less than $-80\,\text{dB}$, while minimizing the on-resistance. The values that satisfied these conditions were a width of $5\,\mu\text{m}$ and a length of 60 nm, for both transistors. This yielded a THD value of $-82.55\,\text{dB}$, considering 10 harmonics, as shown in Fig. 4.18, and a maximum on-resistance of $270\,\Omega$, seen in Fig. 4.19.

4.5.1 Clock Bootstrapped Switch

As previously stated, the switch introduces harmonic distortion to the circuit, mainly due to their nonlinear on-resistance, which is affected by the V_{GS} voltage of the transistors, which varies with the input signal. One way to linearize the on-resistance is using clock bootstrapping (CBT) techniques on the switches. This circuit adds the input voltage to the clock signal of the switch, when it is active, making the voltage at the gate of the transistor be equal to $V_{dd} + V_{\text{in}}$, which in turn makes the voltage

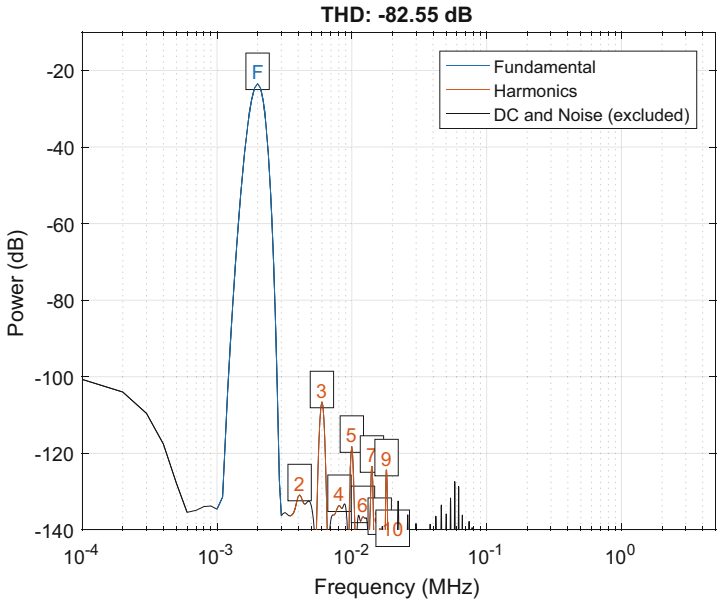


Fig. 4.18 Total harmonic distortion of the transmission gate from a 2 kHz sinusoidal input signal

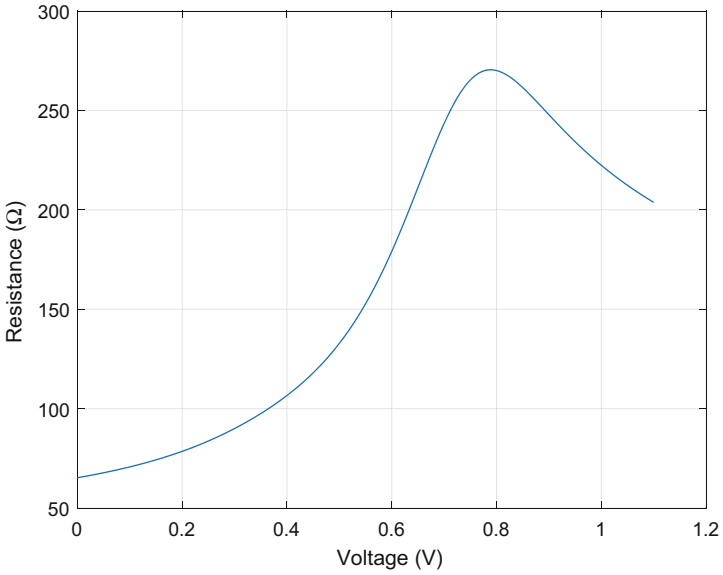


Fig. 4.19 On-resistance of the transmission gate as a function of the input signal amplitude

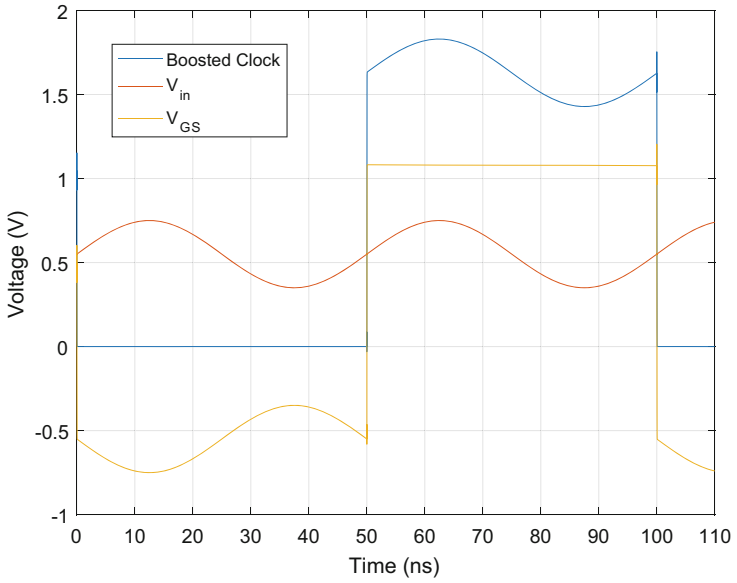


Fig. 4.20 Behavior of the CBT circuit

V_{GS} remain constant. This results in an on-resistance independent of the input signal, reducing distortion. However, this means that the gate voltage of the transistor can be greater than V_{dd}, which may lead to degradation of the transistor. This behavior can be seen in Fig. 4.20.

The CBT circuit is shown in Fig. 4.21 and is based on the circuit used in [13]. A NMOS switch was used (MN2), since its shortcomings are compensated by the CBT, with a width of 5 µm and a length of 60 nm. These switches were used in the signal path, at the entrance of each integrator, where good linearity is most important.

4.6 Feedback and Reference Voltages

The feedback is employed using switches which connect the bottom plate of the capacitors to a reference voltage, either $V_{\text{ref}+}$ or $V_{\text{ref}-}$, as seen in Fig. 4.22. The values of these voltages depend on the feedback gain G_{fb}, subject to optimization, and on the common mode voltage, V_{cm}, of the integrator:

$$\begin{cases} V_{\text{ref}+} = V_{\text{cm}} + \frac{V_{dd} \cdot G_{\text{fb}}}{2} \\ V_{\text{ref}-} = V_{\text{cm}} - \frac{V_{dd} \cdot G_{\text{fb}}}{2} \end{cases} \tag{4.7}$$

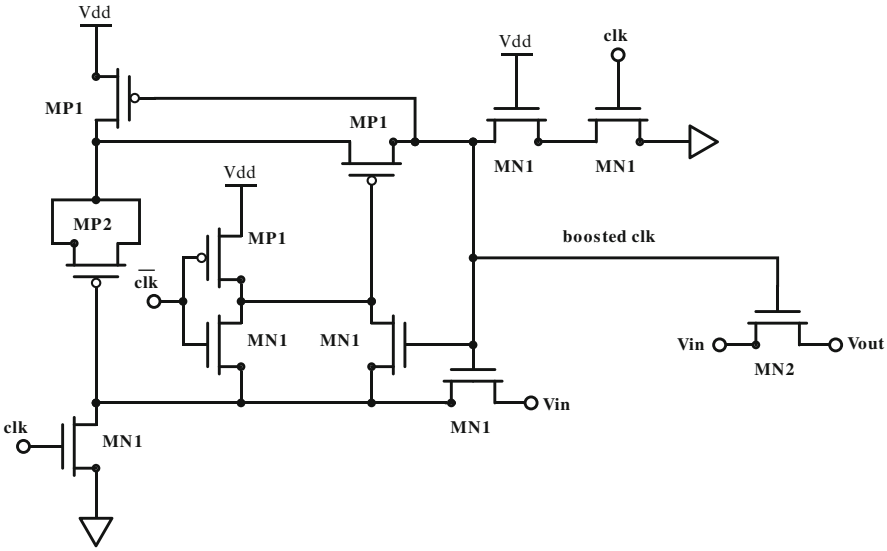
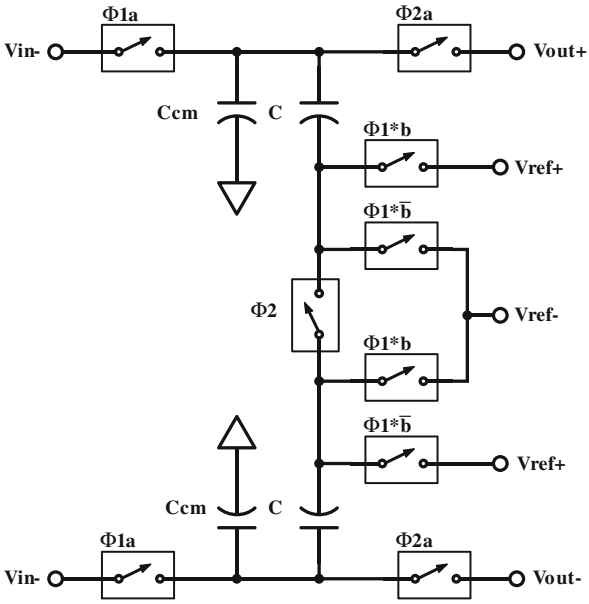


Fig. 4.21 NMOS switch with clock bootstrapping circuit

Fig. 4.22 Schematic of an integrator with feedback path and reference voltages



Since the $\Sigma\Delta$ modulator employs negative feedback, the positive reference voltage is summed to the capacitor when the output of the modulator is *low*, and vice versa. For a differential approach, a second capacitor is used that works in reverse, positive reference is summed when the output is *high*, and vice versa. The control of the reference voltages switches is done using AND gates, as shown in Fig. 4.23.

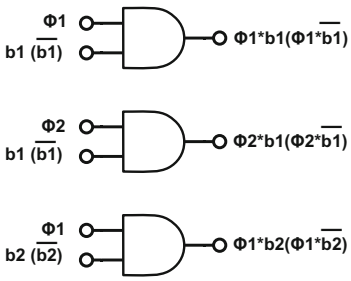


Fig. 4.23 Schematic of the reference voltages switch control

Table 4.5 Reference voltage values of the second order $\Sigma\Delta$M

Parameter	V_{ref1+}	V_{ref1-}	V_{cm1}	V_{ref2+}	V_{ref2-}	V_{cm2}
Voltage (V)	1.1	0	0.55	0.76331	0.62669	0.695

Table 4.6 Reference voltage values of the third order MASH $\Sigma\Delta$M

Parameter	V_{ref1+}	V_{ref1-}	V_{cm1}	V_{ref2+}	V_{ref2-}	V_{cm2}	V_{ref3+}	V_{ref3-}	V_{cm3}
Voltage (V)	1.1	0	0.55	0.816	0.574	0.695	0.5547	0.3853	0.47

The feedback switches close before the switches that connect to the input and output, which use a delayed clock signal ($\phi 1a$ and $\phi 2a$). This is to allow the capacitors time to adjust to the new voltage at their bottom plate before integrating the input or passing it to the next integrator. This is called bottom plate sampling and is used to reduce the distortion added by charge distribution from the switches.

Additional capacitors, C_{cm}, are used to reduce the common mode voltage swing at the output. Their capacity is 10% of the capacitor of the integrator.

Tables 4.5 and 4.6 show the values of the reference voltages used in the second order modulator and in the third order MASH modulator, respectively.

4.7 Monostable Circuit

Figure 4.24 shows the schematic of the monostable circuit used to generate shorter phase signals, with the purpose to reduce the size of the capacitors used in the third order MASH $\Sigma\Delta$ modulator, which was adapted from the one used in [19]. In practice, it delays the rising edge of the input, by a time defined by an RC constant. When the input is *low*, the capacitor is charged, through transistor MP1, to V_{dd} and transistor MN1 pulls the output to ground. When the input goes *high*, MN1 and MP1 are turned off and the capacitor starts discharging, according to the RC constant, until MP2 is turned on and pulls the output *high*. A feedback loop, through MN3, and a feedforward loop, through MN4, as well as capacitor C_2 and the output inverters, increase the speed of the rising edge of the output to reduce jitter noise.

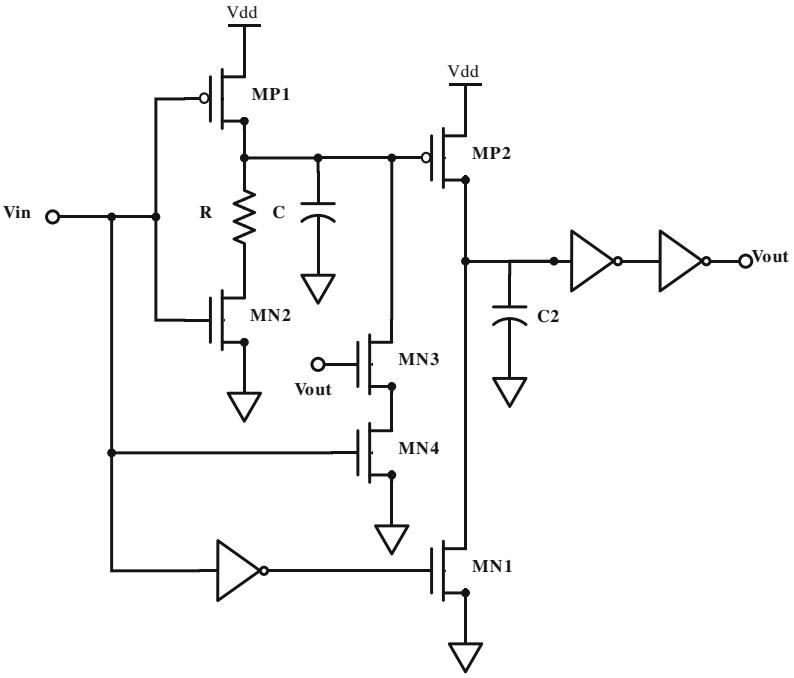


Fig. 4.24 Schematic of the rising edge delay monostable

To produce a 5 ns pulse from a 50 ns one, a 226.5 kΩ resistor and a 5 pF capacitor are used. Figure 4.25 shows the output of the monostable, as well as the voltage at the capacitor.

Unfortunately, this monostable circuit generates too much jitter noise, and when applied to the modulator, the resulting SNDR was significantly inferior to the expected from the model. As such, an alternative topology for the monostable circuit was considered. The schematic of the circuit can be seen in Fig. 4.26 and is based on the circuit of the pulse detector used to generate the clock signal of the *flip-flop*. When the input is *low*, the AND gate pulls the output to *low* and the capacitor is charged, through the resistor, to V_{dd}. When the input goes *high*, the AND gate pulls the output to *high*, since the voltage at the capacitor is V_{dd}, and the capacitor starts discharging. When its voltage reaches the switching point voltage of the AND gate, the output is pulled to *low*, remaining until the next rising edge of the input signal. The values of the capacitor and the resistor determine the duration of the output pulse, and for it to last for 5 ns, an 8 kΩ resistor and a 700 fF capacitor were used. The inverters at the output are used to decrease the falling time of the pulse, thus reducing the jitter noise. In Fig. 4.27 is shown the behavior of the monostable in these conditions.

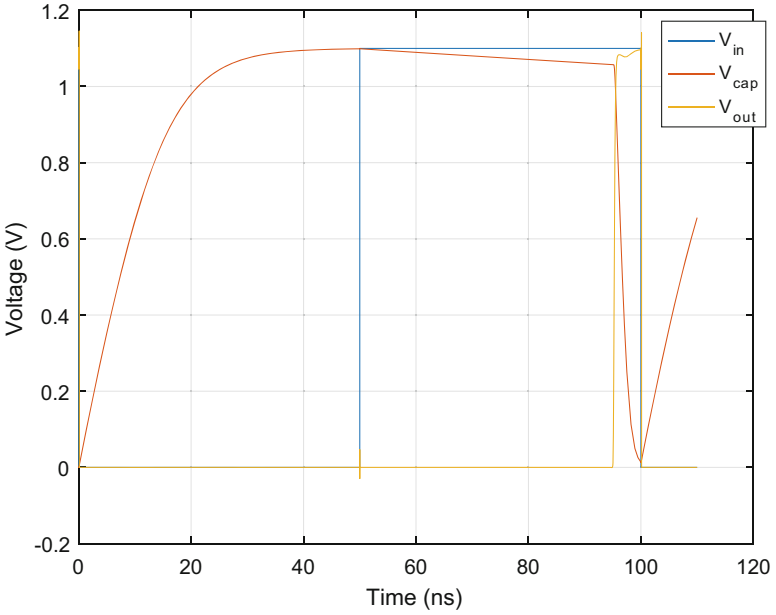


Fig. 4.25 Simulated input, output and capacitor voltages of the rising edge delay monostable

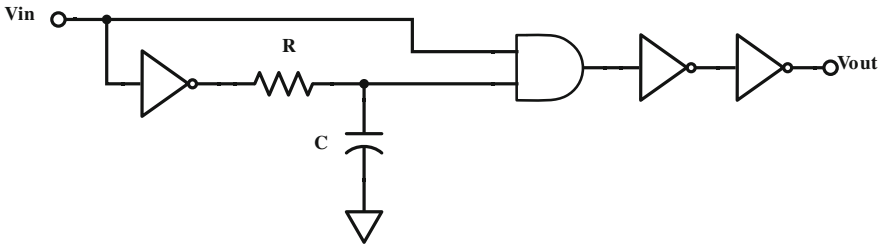


Fig. 4.26 Schematic of the rising edge triggered monostable

Since the modulator works in two phases, two monostable circuits are used, and each uses as input one of the outputs of the phase generator. With the addition of these circuits, overlapping of the phases ceases to be a problem, so the phase generator used with them is slightly different. The delay circuits used are no longer required, so they were removed, which lowered the power consumption. Figure 4.28 shows the complete schematic of the new phase generator, where the monostable circuits were added.

The output of the rising edge trigger monostable is shown in Fig. 4.29. The two new phase signals have a pulse duration of 5 ns and same phase pulses are separated by 100 ns, meaning their frequency is still 10 MHz. There is also a half period, 50 ns, delay between both phases.

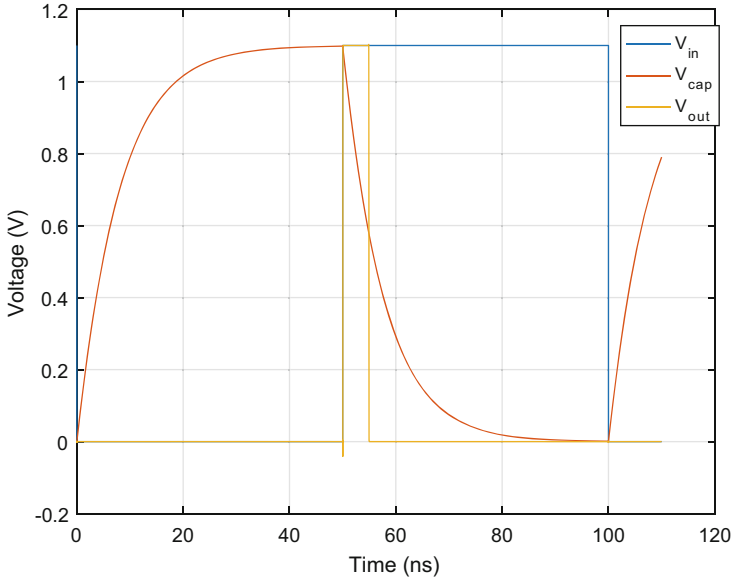


Fig. 4.27 Simulated input, output and capacitor voltages of the rising edge trigger monostable

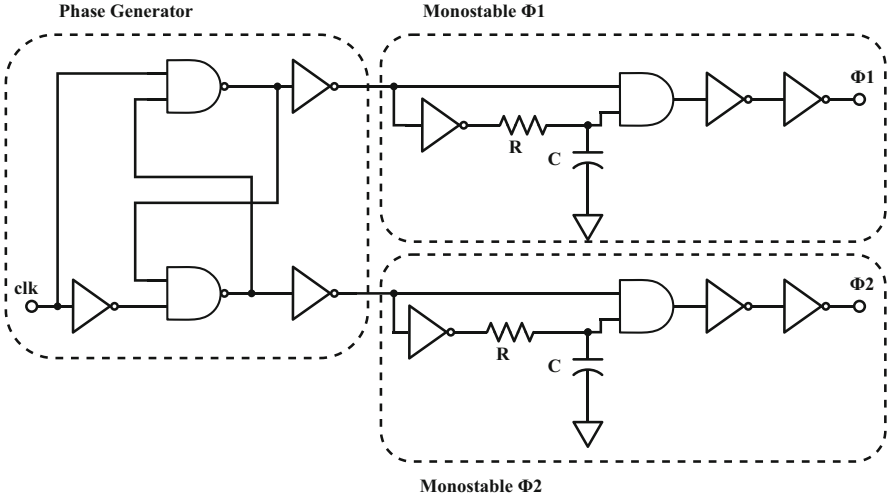


Fig. 4.28 Schematic of the phase generator with monostable used for the third order MASH $\Sigma\Delta$M

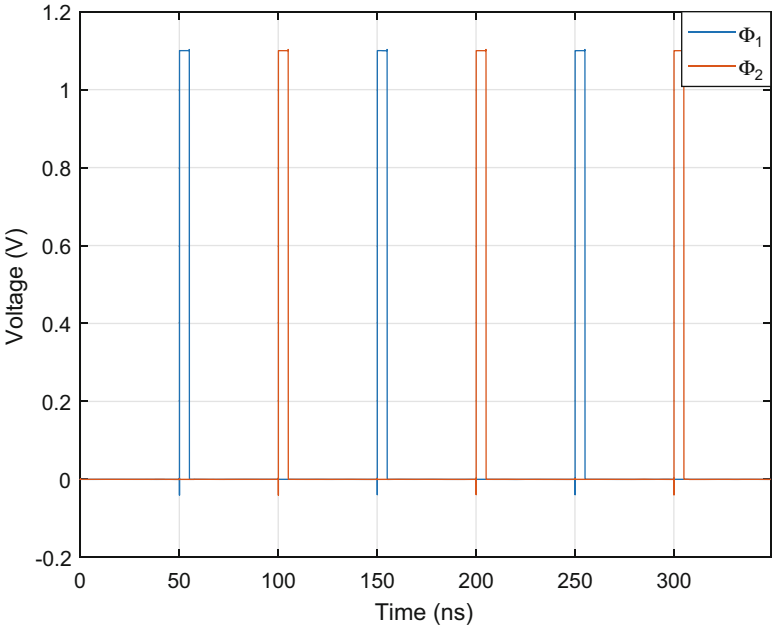


Fig. 4.29 Simulated phase signals generated by the rising edge trigger monostable

4.8 Simulation Results

In this section, electrical simulation results of the three designed modulators are presented. As stated previously, the circuits were designed in a standard 65 nm CMOS technology with a power supply voltage value of 1.1 V and using standard voltage threshold transistors. These results were obtained through transient-noise simulations using the *Virtuoso Platform* EDA software.

4.8.1 Second Order ΣΔ Modulator

The second order $\Sigma\Delta$ was simulated using the optimization values obtained through the *MATLAB*® model, explained in Chap. 3. These values are once again shown in Table 4.7. The value of the feedback gain of the second integrator, G_{fb1}, was doubled to increase the stability of the modulator and achieve performance similar with that of the model. The transient output of the modulator was sampled at the rate of the clock signal, 10 MHz, one sample per 100 ns, and its FFT was obtained, using Blackman–Harris window and 20k points, in order to calculate its SNDR. Figure 4.30 shows the FFT for a 2 kHz input signal with amplitude of 10 and

Table 4.7 Parameters values used in simulation of the second order $\Sigma\Delta$M

Parameter	$C1$	$R1$	$C2$	$R2$	f_s	G_2	G_{fb1}
Value	9 pF	900 kΩ	4.5 pF	900 kΩ	10 MHz	6	0.1242

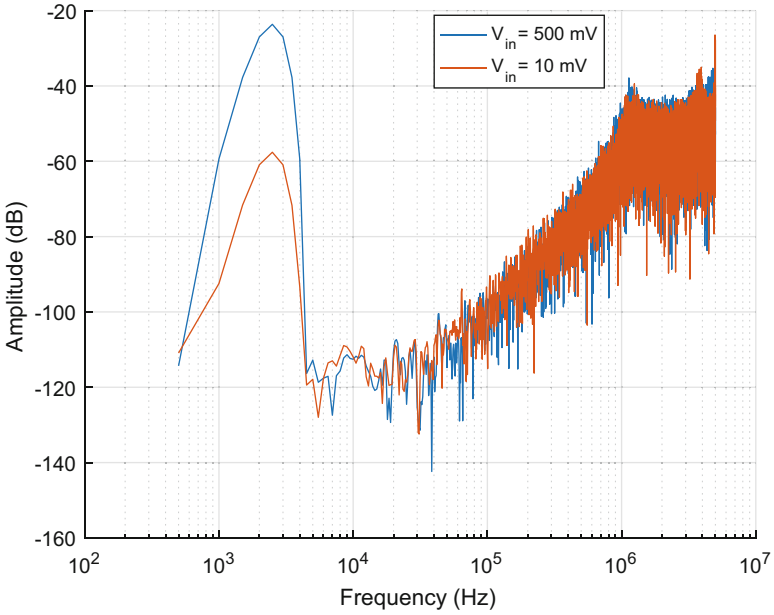


Fig. 4.30 A 20k point FFT with Blackman–Harris window of the second order $\Sigma\Delta$M output signal for 10 and 500 mV amplitudes for a 2 kHz input signal

500 mV, which resulted in a SNDR of 44.08 and 79.42 dB, respectively. It can also be seen from the figure the expected behavior of a $\Sigma\Delta$M, where the magnitude of the noise is low on the signal band, and is pushed and amplified to higher, out-of-band frequencies. This noise must them be low-pass filtered.

The modulator achieved a peak SNDR value of 81.84 dB for an input signal of 650 mV, as seen in Fig. 4.31, where its DR is compared with the one obtained from the model. The DR value from these results is 88.9 dB, calculated from the SNDR peak to the point it intersects the 0 dB line.

The power consumption was calculated by measuring the average current at the supply voltages of each circuit, for a period of the 2 kHz input signal with amplitude correspondent to the peak SNDR, 650 mV. The power consumption of the whole modulator is 46.5 μW. Presented in Table 4.8 is the power consumption of each individual circuit, and in Fig. 4.32 is represented their relative values, in percentage. In these, "Supply Voltage" refers to the rest of the circuits used, like logic gates, switches, and delay blocks.

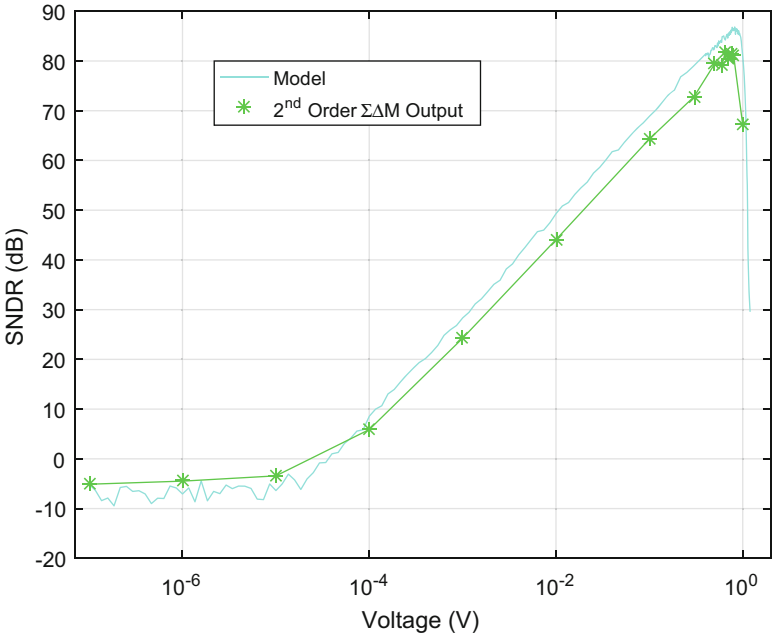


Fig. 4.31 Comparison between the DR of the second order $\Sigma\Delta$M obtained by electrical simulation and obtained using the high level model

Table 4.8 Power consumption by circuit of the second order $\Sigma\Delta$M

Circuit	Reference voltages	Supply voltage V_{dd}	Phase generator	Amplifier G_2	Comparator	*flip-flop*	Total
Power (μW)	0.084	19.83	22.01	1.65	1.78	1.14	46.5

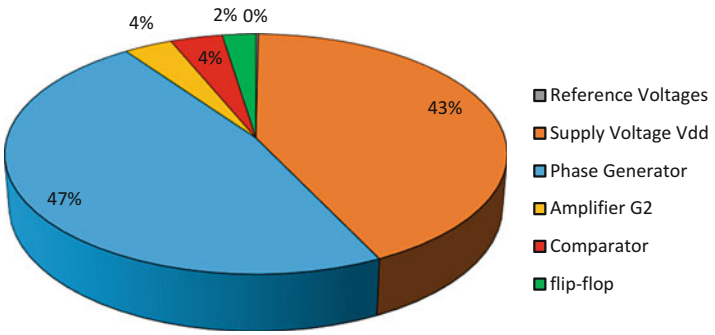


Fig. 4.32 Relative power consumption by circuit of the second order $\Sigma\Delta$M

To understand better if the modulator's performance is good, and to compare it to other $\Sigma\Delta$ circuits, figures of merit (FOM) must be calculated. The most widely used FOMs for ADCs are the Walden FOM (FOM_W), in Eq. (4.8), and the Schreier FOM (FOM_S), in Eq. (4.9).

$$\text{FOM}_W = \frac{\text{Power}}{2 \cdot \text{Bandwidth} \cdot 2^{\text{ENOB}}} \text{(J/conv-step)} \tag{4.8}$$

$$\text{FOM}_S = \text{SNDR} + 10 \cdot \log_{10}\left(\frac{\text{Bandwidth}}{\text{Power}}\right) \text{(dB)} \tag{4.9}$$

A different version of the FOM_S can be used, where the DR value is used, instead of the SNDR.

The ENOB of the modulator is calculated using the maximum SNDR obtained and has the value 13.3 bits. This leads to a FOM_W of 115 fJ/conv-step, and a FOM_S of 168 dB.

4.8.2 Third Order MASH $\Sigma\Delta$ Modulator

The MASH structure requires a DCL block to produce an output where the quantization noise is canceled. In this project, the DCL was simulated using *MATLAB*® based on the DCL used on the third order modulator model, presented in Chap. 3. The gains of the comparators are used in this block and have to be calculated, which is not easily done, since they depend on their input signal. These gains can be considered as a ratio between the rms values of the output and the input signals and obtained from simulations. From [13], the comparators gains are defined as:

$$\begin{cases} G_{\text{comp1}} = \frac{K_{gc1}}{\alpha_2} \\ G_{\text{comp2}} = \frac{K_{gc2}}{\alpha_3} \end{cases} \tag{4.10}$$

Factors K_{gc1} and K_{gc2} are obtained empirically. Since the noise cancellation relies on accurate matching between the transfer functions of the MASH stages and the ones modeled in the DCL, these factors are useful to adjust any mismatch between them. An adjustment gain, G_{adj}, was also required in order to minimize this mismatch. This gain is placed at the output of the first stage, before the cancellation of the quantization noise at the output.

These three factors were chosen in order to maximize the SNDR at the output of the DCL, and took the values:

Table 4.9 Parameters values used in simulation of the MASH $\Sigma\Delta$M

Parameter	$R1$	$C1$	$R2$	$C2$	$R3$	$C3$	G_{fb1}	G_2	G_{fb2}	G_{mid}
Value	34.4 kΩ	99 pF	31 kΩ	100 pF	950 kΩ	8 pF	0.22	10	0.154	10

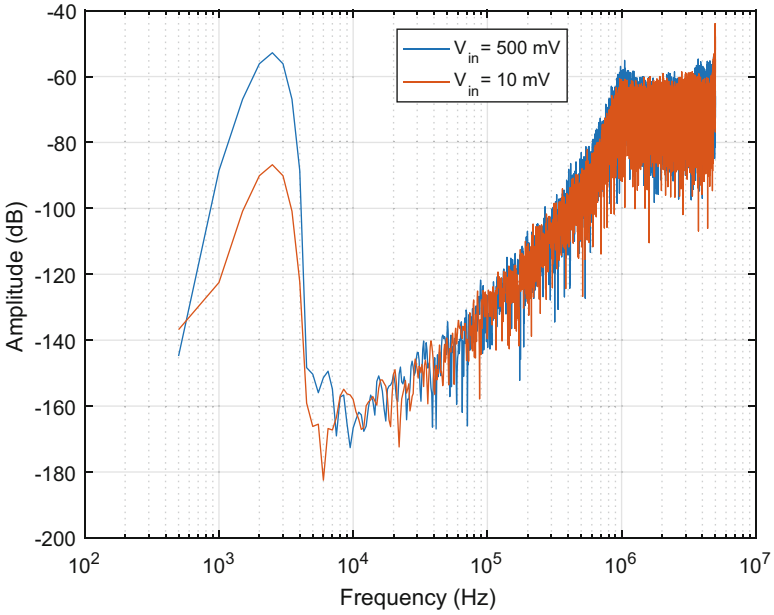


Fig. 4.33 A 20k point FFT with Blackman–Harris window of the third order $\Sigma\Delta$M output signal for 10 and 500 mV amplitudes for a 2 kHz input signal

$$\begin{cases} K_{gc1} = 2.15 \\ K_{gc2} = 0.06 \\ G_{adj} = 0.81 \end{cases} \tag{4.11}$$

The values of the components used in the simulation of the third order MASH $\Sigma\Delta$ are shown in Table 4.9 and are the ones obtained through optimization. The FFT for 2 kHz input signals with amplitudes 10 and 500 mV are shown in Fig. 4.33. The SNDR achieved by these two signals is 58.40 and 90.89 db, respectively.

The modulator achieves a peak SNDR of 92.72 dB for an input signal of 800 mV. The obtained DR is 150.2 dB and can be seen in Fig. 4.34, where the results are compared with the model.

The total power consumption of the modulator is 137.4 μW, which is divided by its circuits as shown in Table 4.10, and in Fig. 4.35 as a percentage of the total power.

The modulator achieves an ENOB of 15.1 bits, a FOM_W of 96 fJ/conv-step, and a FOM_S of 174 dB.

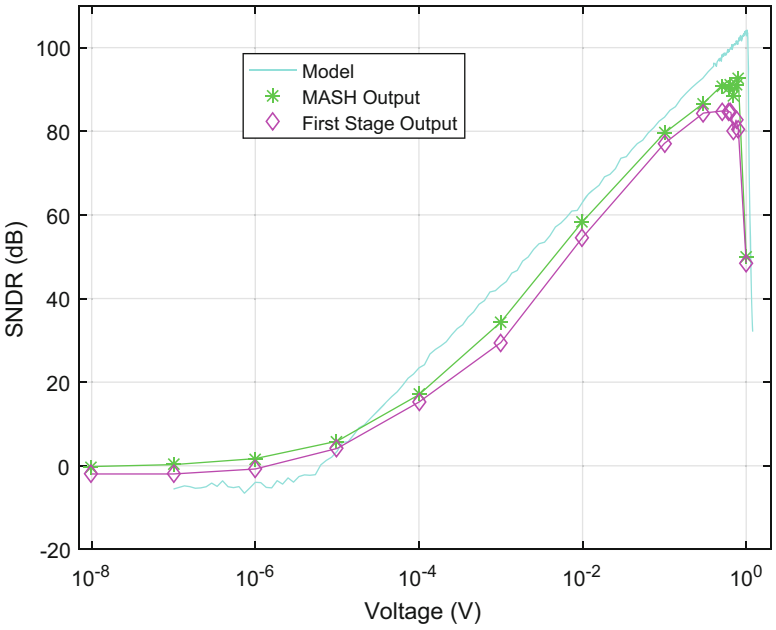


Fig. 4.34 Comparison between the DR of the MASH $\Sigma\Delta$M obtained by electrical simulation and obtained using the high level model

Table 4.10 Power consumption by circuit of the third order MASH $\Sigma\Delta$M

Circuit	Reference voltages	Supply voltage V_{dd}	Phase generator	Amplifier G_2	Comparators	*flip-flops*	Amplifier G_{mid}	Total
Power (μW)	2.96	69.93	22	34.56	3.47	2.26	2.22	137.4

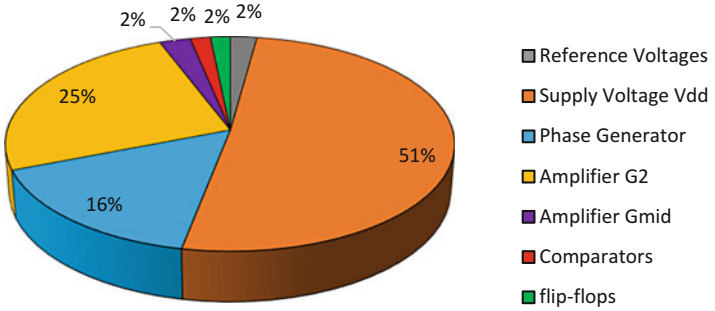


Fig. 4.35 Relative power consumption by circuit of the third order MASH $\Sigma\Delta$M

Table 4.11 Parameters values used in simulation of the MASH $\Sigma\Delta$M with monostable

Parameter	$R1$	$C1$	$R2$	$C2$	$R3$	$C3$	G_{fb1}	G_2	G_{fb2}	G_{mid}	T_s
Value	34.4 kΩ	10 pF	31 kΩ	10 pF	950 kΩ	8 pF	0.22	10	0.154	10	5 ns

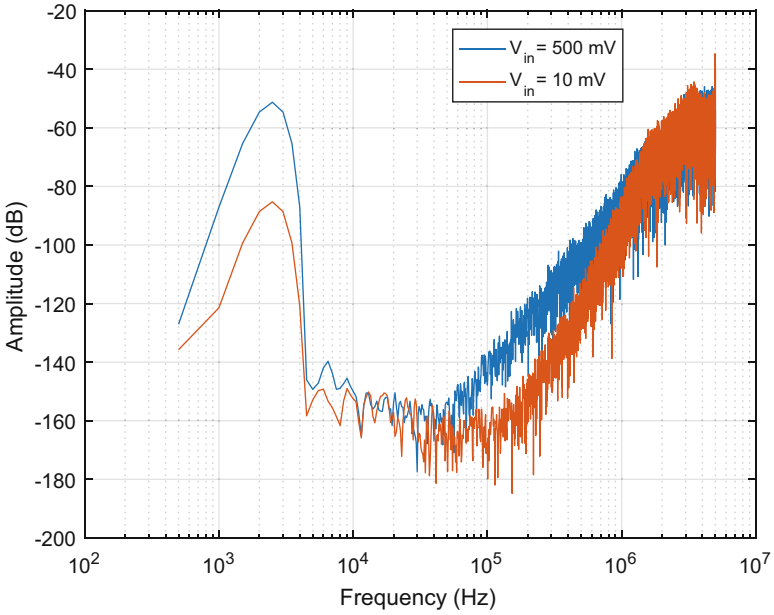


Fig. 4.36 A 20k point FFT with Blackman–Harris window of the third order $\Sigma\Delta$M with monostable output signal for 10 and 500 mV amplitudes for a 2 kHz input signal

4.8.3 Third Order MASH ΣΔM with Monostable Circuit

Table 4.11 shows the values of the components used in the simulation of the third order MASH $\Sigma\Delta$M with monostable circuit. The FFT for a 2 kHz input signal with 10 and 500 mV of amplitude is shown in Fig. 4.36, achieving a SNDR of 56.03 and 85.76 dB, respectively. The parameters of the DCL were adjusted in order to maximize the SNDR:

$$\begin{cases} K_{gc1} = 10.45 \\ K_{gc2} = 0.01 \\ G_{\text{adj}} = 4.87 \end{cases} \tag{4.12}$$

The peak SNDR achieved by the modulator is 92.06 dB, for an input signal of 600 mV, and a DR value of 111.4 dB, which can be seen in Fig. 4.37, where the simulation results are compared with the ones obtained by the model and with the output of the first stage of the MASH structure.

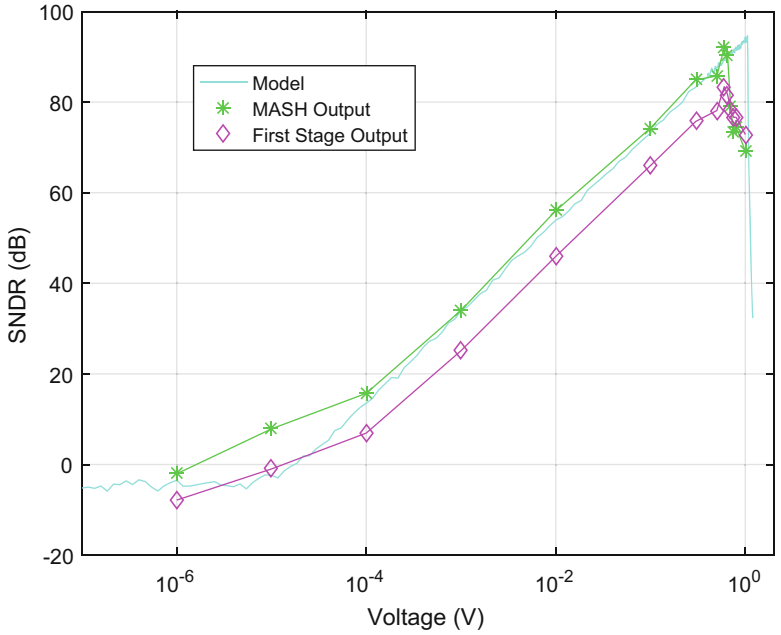


Fig. 4.37 Comparison between the DR of the MASH $\Sigma\Delta$M with monostable obtained by electrical simulation and obtained using the high level model

Table 4.12 Power consumption by circuit of the third order MASH $\Sigma\Delta$M with monostable

Circuit	Reference voltages	Supply voltage V_{dd}	Phase generator	Amplifier G_2	Comparators	*flip-flops*	Amplifier G_{mid}	Total
Power (μW)	5.43	17.7	20.93	34.56	2.86	2.26	2.23	85.97

The whole modulator dissipates a total of 85.97 μW, divided by its circuits as shown in Table 4.12, and Fig. 4.38 shows these results in terms of percentage.

The modulator achieves an ENOB of 15 bits, a FOM_W of 65.6 fJ/conv-step, and a FOM_S of 176 dB.

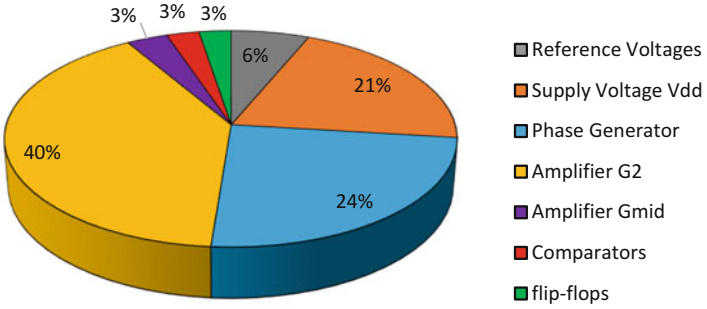


Fig. 4.38 Relative power consumption by circuit of the MASH $\Sigma\Delta$M using the monostable circuit

Chapter 5
Conclusions

5.1 Final Remarks

In this book, the design of discrete time $\Sigma\Delta$ modulators using passive, switched-capacitor integrators working under the ultra incomplete settling, operating in the 20 kHz bandwidth, was presented. Three ADC circuits were designed: a second order $\Sigma\Delta$M and two versions of a third order MASH $\Sigma\Delta$M, working with a sampling frequency of 10 MHz, corresponding to an OSR of 250. Optimization techniques, based on high level models of the circuits, were used in order to maximize the performance while, at the same time, minimizing power consumption and circuit area of the modulators. Table 5.1 summarizes the key performance parameters of the designed modulators, where it can be seen that the target SNDR was achieved, 80 dB for the second order $\Sigma\Delta$M and 90 dB for the third order $\Sigma\Delta$Ms.

Electrical simulations showed the limitations of the developed high level *MATLAB®* model. It does not include all noise sources nor it takes into account the nonlinearity to the saturation of electrical circuits, and leads to more optimistic results. Nevertheless, it proved useful in the design of the circuits, as well in validating the electrical simulations and the optimization results obtained for the third order MASH $\Sigma\Delta$M.

As expected, the third order MASH modulator achieved a higher SNDR, of nearly 10 dB, than the second order one. However, power consumption rose nearly three times. This increase is due to the addition of an extra integrator, and the circuitry that comes with it, switches, delay blocks, reference voltage and its control switches, the amplifier G_{mid}, comparator, and a *flip-flop*. The use of bigger capacitors also influences this problem. The use of smaller resistors as the load of the differential pair, in amplifier G_2, led to an increase of its static current, to keep the desired common mode voltage at its output. This resulted in a significant increase in the power consumption of the amplifier.

D. Fouto, N. Paulino, *Design of Low Power and Low Area Passive Sigma Delta Modulators for Audio Applications*, SpringerBriefs in Electrical and Computer Engineering, DOI 10.1007/978-3-319-57033-4_5

Table 5.1 Key performance parameters obtained by electrical simulation

	SNDR (dB)	ENOB (bit)	DR (dB)	Power (μW)	FOM_W (fJ/conv-step)	FOM_S (dB)
Second order $\Sigma\Delta$M	81.836	13.3	88.9	46.5	115	168
Third order MASH $\Sigma\Delta$M	92.7227	15.1	150.2	137.4	96	174
Third order MASH $\Sigma\Delta$M with monostable	92.0602	15	111.437	85.97	65.6	176

It is worth noting the increase in size of the capacitors resulted in an increase of charge distribution effect between them and the used switches. Since this was not the final modulator, and its main purpose is to compare performance, ideal switches were used between capacitors of the same integrator, instead of redesigning the switches, for simulation purposes. The MASH modulator with monostable once again uses the designed CMOS transmission gate switches.

The use of the monostable circuit, to generate smaller pulses, to be used as the modulator clock phases, had the main objective of reducing the size of the capacitors used, while maintaining performance. The capacitors used were ten times smaller than the ones used in the MASH modulator without monostable. The capacitor of the second stage was not reduced, since it already had an acceptable size. This also led to a decrease in the power consumed by the modulator, since the active time of the circuits was reduced. Overlapping of the clock phases ceases to be a problem, so many delay blocks were no longer needed for synchronization, especially in the phase generator circuit, which also contributed to the reduction of the consumed power. The amplifier G_2 remained the same, and now represents 40% of the total power consumption of this modulator.

In terms of performance, based on the figures of merit, the best modulator was the third order MASH $\Sigma\Delta$M with monostable. It achieved both the lowest FOM_W, 65.6 fJ/conv-step, and the highest FOM_S, 176 dB. It also achieved a good DR of 111 dB, less than the one obtained from the MASH $\Sigma\Delta$M without monostable, and an ENOB of 15 bits.

The simulated performance of the MASH modulator using the monostable circuit is compared with state-of-the-art, and most recent, $\Sigma\Delta$ modulators designed for audio applications in Table 5.2. It achieves the best FOM_W and one of the best FOM_S. Its power dissipation is the lowest and achieves a good DR. Although its peak SNDR and ENOB are one of the lowest, they are still good values. In conclusion, the third order MASH $\Sigma\Delta$ modulator shows a good performance, validating the use of a monostable circuit to reduce the size of the components used on the passive integrator, validating also the use of ultra incomplete settling to build said integrators. Since its performance is comparable to that of previous modulators used in audio applications, the designed modulator might have its uses in the field.

Table 5.2 Performance comparison of the MASH $\Sigma\Delta$M with monostable with state-of-the-art audio $\Sigma\Delta$Ms. Adapted from [20]

	This work	Berti et al. [20]	Gönen et al. [21]	Billa et al. [22]	Sukumaran and Pavan [23]	Wang et al. [24]	Lo [25]	Park et al. [26]
Technology (nm)	65	160	160	180	180	180	40	180
Architecture	SC	CT	SC	CT	CT	SC	CT/SC	SC
Supply voltage (V)	1.1	1.6	1.8	1.8	1.8	5.0/1.8	2.5/1.2	0.7
Power (mW)	0.086	0.39	1.65	0.28	0.28	1.1	0.5	0.87
Bandwidth (kHz)	20	20	20	24	24	20	24	25
OSR	250	75	282	128	128	64	135	100
Peak SNDR (dB)	92.06	91.3	98.3	98.5	98.2	99.3	90	95
DR (dB)	111.4	103.1	107.5	103.6	103	101.3	102	100
ENOB (bit)	15	14.9	16	16.1	16	16.2	14.7	15.5
FOM_W (fJ/conv-step)	65.6	325	614	84.8	87.8	365	403	379
$\text{FOM}_{S(\text{SNDR})}$ (dB)	176	168	169	178	178	172	167	170
$\text{FOM}_{S(\text{DR})}$ (dB)	195	180	178	183	183	174	179	175

In order to validate the simulation results, a physical implementation of the modulator must be performed. The layout of the circuit is required to obtain its total area, an important design constraint for the intend purpose of the modulator.

As said before, a significant part of the power consumption of the modulator comes from the amplifier used to isolate both integrators of the first stage, G_2. The use of relatively small resistors and the chosen amplifier topology led to this. The use of a different topology might be the answer to this problem. Another solution might be increasing the resistor's value and adjusting the rest of the circuit in order to keep the same performance, for instance reducing the size of the capacitor in the same proportion, keeping the time constant of the RC circuit.

Another important future consideration is the implementation of the DCL circuit. This circuit was only simulated, but its implementation certainly affects the performance of the modulator, in terms of circuit area and power consumption. Careful design must be performed, since its impact on the overall performance depends on the matching between it and the modulator.

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