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Alessandro De Gloria
Editor

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Preface

This is the fifth edition of the ApplePies Conference, held in Rome, Italy, in September 2016. The conference aims at offering a wide and reasoned overview of electronic applications in several domains, demonstrating how electronics has become pervasive and ever more embedded in everyday objects and processes.

The computational, storage, and communication power of current electronic systems is such that we may really say that their applications are limited only by the designer's fantasy. This represents a great challenge for practitioners, managers, and academicians in ICT Engineering. The challenge also stresses the importance of multidisciplinary knowledge, expertise, and collaboration, in order to support a virtuous iterative cycle from user needs to new products and services. The cycle goes through the whole system engineering process, which typically encompasses requirement elicitation, specification management, software and hardware design, laboratory and user testing and verification, and maintenance management.

For either an embedded or cyberphysical system to be successful in the current globalized market competition, at least one of the following features must be provided: innovation, high performance, and good cost/performance ratio. Designing and implementing each one of such features requires a deep knowledge of both the system's target application and domain, and of the technologies that are potentially able to fulfill the expected goals.

One of the most important factors for the success of a project consists in the adoption of a suited design flow and related tools. Only seldom are simple top-down or bottom-up methods able to meet the time- and cost-related challenges of nowadays market scenarios. Even if every application stems from recognizing one or more key user needs, a proper design, implementation, and maintenance require mastering the most suited technologies and tools in order to support efficient and effective development and life cycle management of electronics applications. Support tools must also be able to capture and share a team's experience in the design and implementation process, as it allows anticipating possible problems that may not appear on the paper.

All these challenging aspects call for the importance of the role of the university as a place where new-generation designers can learn and practice with

cutting-the-edge technological tools and are stimulated to devise solutions for challenges coming from a variety of application domains, such as healthcare, transportation, education, tourism, entertainment, cultural heritage, and energy.

This conference wants to report and discuss several examples of designs and become a reference point in the field of electronics systems design, trying to fill at scientific and technological R&D level a gap that the most farsighted industries have already indicated and are striving to cover.

Genoa, Italy Alessandro De Gloria

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Long-Range Radio for Underground Sensors in Geothermal Energy Systems

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Abstract. The paper presents the design of a temperature monitoring system in a very harsh environment, such as Shallow Geothermal Systems (SGS), where the information of underground temperature is necessary to assess the thermal potential of the soil, for maximizing the efficiency of the SGS. The challenge is to get information at different depths (sometimes up to −100 m), to transmit data wirelessly in rural areas where conventional wireless connections (e.g. WiFi, GSM) are not guaranteed and energy availability poses severe limits. Our design exploits a recent new modulation protocol developed for long-range transmission, at the minimum energy cost, and a two-tier hardware architecture for measuring underground temperature. Aggressive duty cycling permits to achieve lifetime of several years. Experimental results demonstrate the utility of such a system during the design and the operational activity of a SGS.

Keywords: LoRa · Geothermal energy systems · Underground monitoring · Long-range radio · Smart sensors

1 Introduction

In recent years, energy saving in several industrial and agricultural areas, such as food and pharmaceutical industries, became an important topic [1]. Geothermal systems are among the most promising technologies to contain heating and air conditioning consumptions and have proved to be an effective solution to reduce the electrical bill, especially in sectors where air conditioning for large spaces or tight temperature control is necessary, such as cold-chain storage for food production or distribution, and cold biopharma warehouses [2]. In such systems, accurate, long-term underground measurements are essential, because the temperatures in the upper soil's layers show significant daily and annual fluctuations and the correct knowledge of the subsoil state drives the control of the geothermal system. The heat flow below the ground level is influenced by several parameters, such as air temperature, wind speed, season, shading/irradiation, soil thermal properties, which are characterized by irregular variability. Forecasting the solar irradiation some days in advance is not enough [3].

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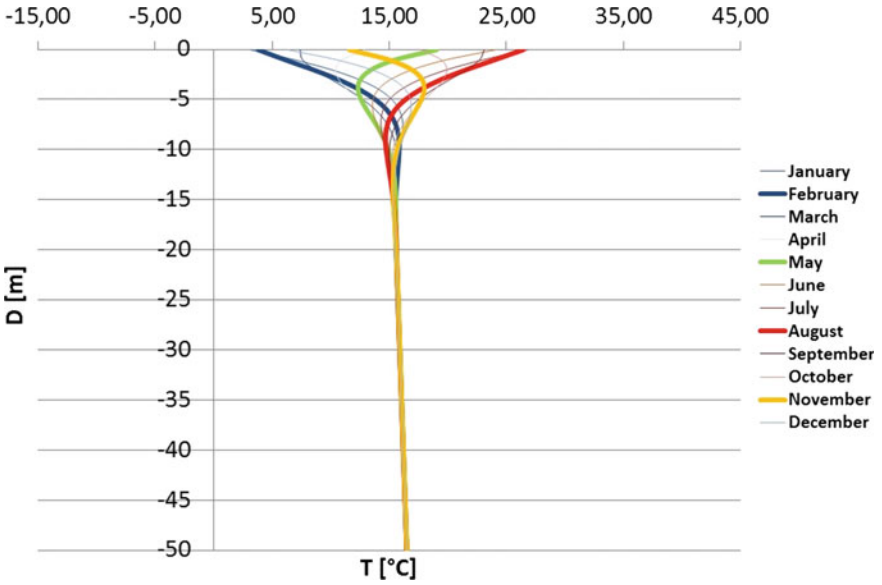

Fig. 1. Graphical representation of the simplified model for the underground temperature evolution along depth for a specific site

Therefore, subsoil temperature estimation is often a hard task, in particular within the layers at few meters of depth, where the influence factors are multiple [4] and where the seasons and air temperature play a crucial role, as seen in Fig. 1; where each month of the year shapes differently the profile of the average temperatures at various depths.

The use of fiber cables thermometers in the shallow geothermal measurements projects has been applied [5], while many other applications preferred the use of wireless sensors installed in the ground or within the boreholes [6]. Unfortunately, most of them have short transmission range. For example, some Wireless Sensor Networks (WSN) permit to measure and to control applications in viticulture [7], large farms [8] and other plants [9], but radio technology is not suitable for underground measurements, unless using very high power for transmissions, in the order of Watts [4], hardly compatibles with low-power system and long-life constraints.

We present a novel, inexpensive and robust monitoring system for long-term underground temperature measurements. This apparatus consists in a set of sensors capable to acquire, to process and to transmit measured temperatures at different depths and on different humidity conditions, with the accuracy and time constraints typical of the industrial control applications. In detail, the SGS underground area contains a cylindrical basket heat exchanger of 1.5 m high and 0.6 m radius, deployed as shown in Fig. 2.

Heat transfer is evaluated by measuring how subsoil layers temperature changes over time. Required depths for the measurements are −2, −4 and −6 m, at a distance of 1.4 m from the geothermal basket, used as heat exchanger, and around 8 m from the Thermal Response Test machine (TM) as illustrated in Fig. 3. A Micro-Thermal

Fig. 2. The installation of the buried heat exchanger with the shape of a cylindrical basket whose performance is influenced by thermal properties of the soil

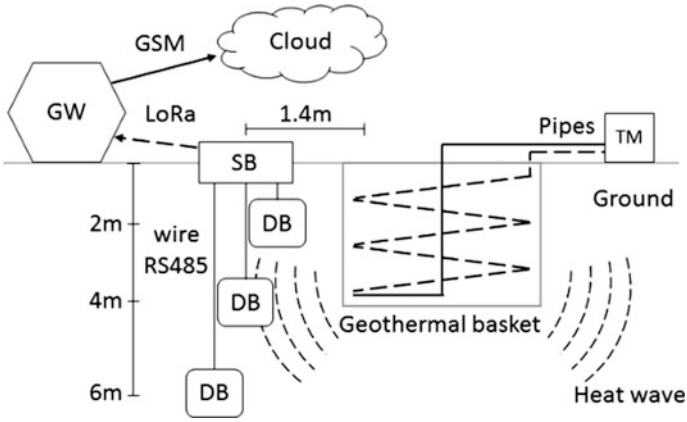

Fig. 3. The model (not to scale) of the area where underground monitoring is necessary for a SGS

Response Test (M-TRT) machine has been designed to assess the thermal resistance of the soil and the performance of a SGS in [10].

2 System Architecture

We used an innovative hybrid approach to address the challenges of underground sensing, mixing wired connectivity to the deep sensors and wireless long-range, low-power connectivity for the near-surface units to the main gateway. A series of devices designed with a temperature sensor are placed underground, through specific boreholes, called Depth Board (DB), as illustrated in Fig. 3. These are wired connected to another board, called Surface Board (SB), positioned few centimeters below the

ground level and repaired inside a concrete manhole. Classic radio technologies such as WIFI or GSM are too much expensive and energy-hungry for this context. Even other traditional sub-GHz radio technologies in underground WSN [4] need too much power for the required system lifetime. Thus, we used a recent technology based on Long-Range (LoRa) wireless transmission (at sub-GHz frequency) that allows low-power connectivity with some km range for the near-surface units. Moreover, aggressive application duty cycle permits to achieve multi-year lifetime when battery powered. The SBs are organized in a star-topology, and transmit wirelessly the acquired data to a gateway (GW), which is the collection point for the WSN. The connection is peer-to-peer without the need of a complex MAC protocol. The GW aggregates and forwards the information to the Cloud through an internet connection (e.g. GSM).

2.1 Depth Board (DB)

This board is manufactured to fit a sealed container and to be powered from the surface through a cable that carries RS485 communication signals. RS485 is used for wired connections to a SB node, and each surface node can manage up to 3 DB nodes. The depth-node is subject to power gating, in fact it can be completely switched off when measuring underground temperature is not necessary, as illustrated in Fig. 3. The sensor SHT21 (manufactured by Sensirion) has been mounted to measure the temperature with one hundredth of a degree accuracy. The TI MSP430FR5969 microcontroller features low power consumption while RS485 communication is realized using a Maxim MAX3485 transceiver to achieve a transmission distance of up to 100 m.

2.2 Surface Board (SB)

The main characteristic of these boards, shown in Fig. 4, is the exploitation of a Long-Range radio transceiver at 868 MHz. With the aim of low power consumption, the same low-power MCU is used, TI MSP430FR5969, equipped by a Real Time Clock for synchronizing the tasks to execute and the transmissions to the gateway. Wireless communication to the gateway is realized using LoRa radio technology provided by Semtech [11], operating at 868 MHz.

LoRa takes advantage of a proprietary modulation technique based on the spreading spectrum that gives it a strong noise immunity and thanks to a −148 dB high sensitivity, allows reaching long distances with a very low power consumption. In addition, we added a boost power amplifier that can transmit up to +20 dB power, which is the maximum allowed in industrial applications and permits a transmission range of several kilometers.

The radio parameters are adjusted for the optimal trade-off between power consumption and transmission range, after dimensioning the bandwidth and the spreading factor. We set a payload of 13 bytes, and a symbol time T_s = 8.19 ms. Therefore, according to the datasheet, T_{packet} = 247.81 ms the total time-on-air of a packet. We configured +2 dB for signal output power that is sufficient to cover the distance

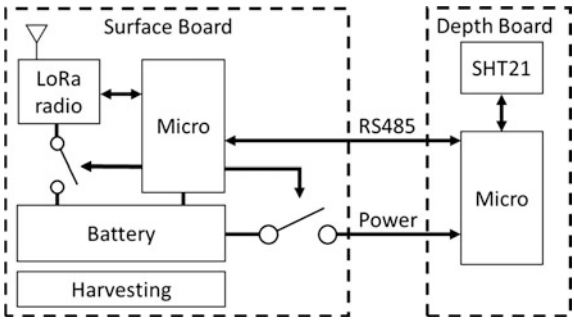

Fig. 4. Architecture of multi-module sensor node with power gating

between sensors and the gateway in our case and in any weather condition, we measured a 38 mA for as current consumption during the interval time T_{packet}. This accounts for about 31 mJ in the total energy budget. Further improvements can be achieved using aggressive data compression techniques as proposed in [12–14].

The nodes are equipped with a lithium polymer battery of 1000 mAh, and mounts a high efficiency DC/DC based on TI BQ25570, which can ensure multi-year long lifetime to the system and host also energy harvesting modules (see [15, 16]). Since the radio transceiver is the most energy hungry component, we have implemented a power gating mechanism, using a MOSFET to enable the transceiver supply when needed and to achieve zero power consumption, when communication is off. The prototype of the Surface Board is shown in Fig. 5.

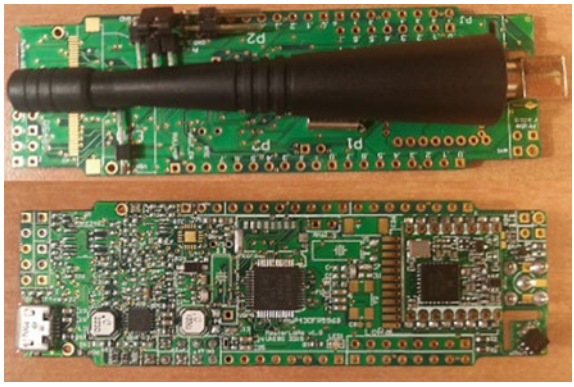

Fig. 5. Prototypes of the wireless module with LoRa transceiver

3 Experimental Results

The power consumption profile is presented in Fig. 6. The peak of current consumption is required when transmitting the information and may reach about 38 mA. During the sleep interval, the power consumption cut down to few μW, which is enough to guaranteed adequate operating time. Typical sending intervals are in the order of 15 min or hours.

In detail, after a first initialization of the peripherals and the clock, where the consumption can be neglected considering that it occurs only at the beginning, the breakdown of the power consumption can be modeled as in Fig. 7. Every cycle can be split into three intervals: sensing/processing interval (T_{sp}), transmission interval (T_{tx}) and sleep interval in ultralow power mode (T_{lowp}). We measured T_{sp} = 0.3 s and an average current consumption of I_{sp} = 3 mA, which results in an energy of 2.97 mJ for each DB connected.

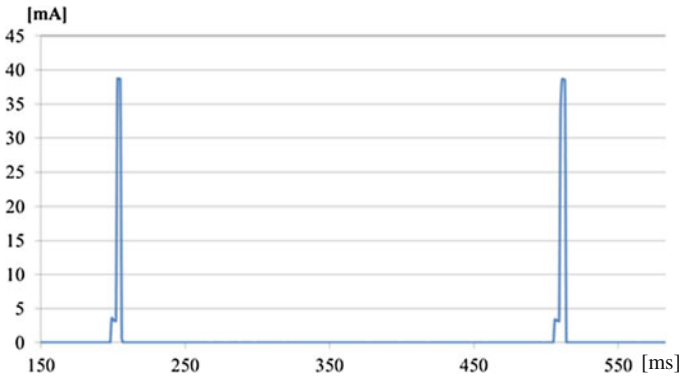

Fig. 6. Power profile of the SB during operation

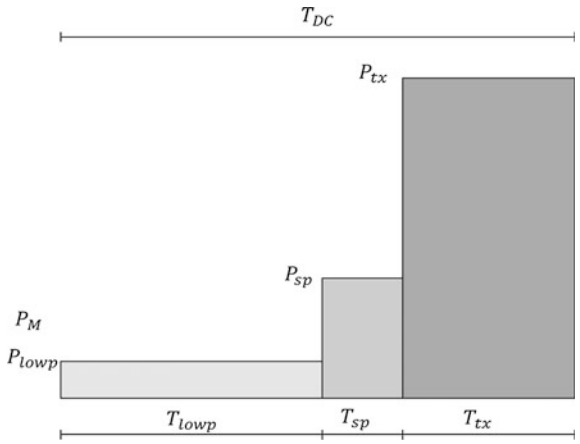

Fig. 7. Power profile model of the SB

When the system is in low-power mode, during sleep interval, the total system consumption drops down to I_{low} = 3 μA, because only the RTC is powered. Considering that the measuring rate for such kind of applications is about T_{meas} = 15 min, the application runs with a Duty-cycle D = 0.06%. and the average power consumption squeezes to 47.6 μW. Therefore, the operating lifetime of the system, if powered with a lithium polymer battery of 1000 mAh and all the three DB are connected, is estimated in T_{life} = 3.1 years.

Figure 8 shows an image of the real deployment used to perform the tests. The surface board is clearly visible connected to the cables to three depth nodes.

The trend of the temperature measurement and an example of usage is depicted in Fig. 9, where temperature oscillations at the depth of −2 m (blue), −4 m (orange) and −6 m (green) are provided. A deeper analysis of the curves indicates how underground thermal diffusivity influences the heat transfer velocity at different depths and distances from the basket.

In fact, we performed more long-duration tests, started on March 24th, 2016 with the injection of hot water into the geothermal basket. The test was conducted

Fig. 8. Prototype of the long-range radio module

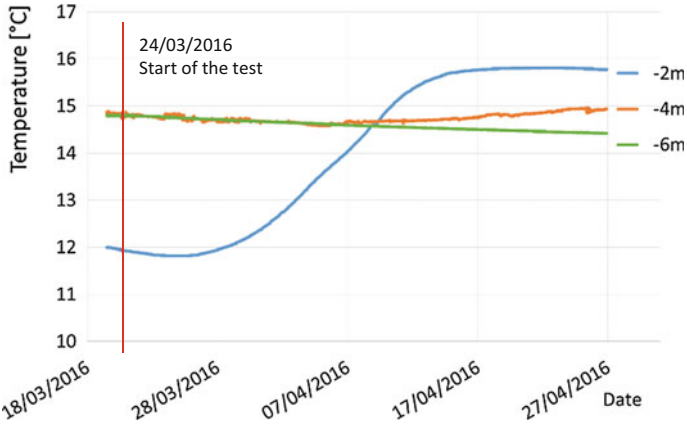

Fig. 9. Plot of underground temperature inside the borehole, at 2, 4 and 6 m depth

uninterruptedly for 12 days, with a constant water flow of 800 l/h and a 1500 W electric resistance was used to heat the water at the inlet of the basket. Then we kept the water circulating into the basket without the heating resistance, for a release period of additional 12 days. The heat wave arrived after 4 days at 2 m depth and 1.4 m far from the geothermal basket, and after 11 days at 4 m depth; while it never reached 6 m depth in the considered period. We note that this is extremely valuable information for the experts asked to design the geothermal system, because these measurements indicate that there is no need of large spacing among multiple baskets, in the considered test site. In addition to the initial test phase, this sensor deployment will be used in long-term measurements after the construction of the SGS system, because underground real-time temperatures will drive the geothermal control system, according to specific temperature damping model.

4 Conclusion

We discussed the design of an autonomous wireless monitoring system for underground temperatures. A complete set of sensors designed to operate several meters below ground level was designed and deployed to understand the external factors influencing the behavior of the soil when a geothermal system is to be installed. Design challenges such as battery lifetime and radio transmission over long distances at the lowest power consumption have been addressed. The designed boards are capable to operate unattended for at least 3 years, sending information to a gateway located several km away.

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Embedding Monitoring Systems for Cured-In-Place Pipes

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Abstract. This paper proposes a non-intrusive electrical measurement system for monitoring some relevant parameters in pipeline systems. Temperature and flow-rate are monitored, using MEMS sensors. The flow-rate is evaluated by measuring pipe vibration, with a 3 axis accelerometer, induced by turbulence when fluid flows within the tube. The sensors are embedded, during the curing process of the cured-in-place pipes, in the pipes wall making the system suitable to be installed in renewed or new pipeline. The first experimental results show that it may be possible to obtain, at low-cost, a fully monitored distribution network.

Keywords: Smart pipes · CIPP technologies · Trenchless technologies · Embedded sensors · Low power electronics · Microcontrollers

1 Introduction

Drinkable water is one of the most important natural resource. There is an effort, technological and social, to reduce waste and enhance conservation of vital resources. The major problem in wasting is the efficiency of the water distribution networks, average losses are around 30% of the input volume with peaks near 60% in certain areas. Hence, the rehabilitation and control of the existing pipeline networks is a crucial point to avoid waste and reduce running costs.

Cured-In-Place Pipe (CIPP) is one of the trenchless methods most widely used in rehabilitation of existing pipelines. It offers several advantages compared to the traditional open cut methods by eliminating costly and time-consuming excavations, reducing the discomfort of service interruption, etc.

Including a monitoring system during this rehabilitation process can lead to a fully monitored system in a few years. Having a monitored network can be useful for the

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network distribution manager in terms of fast leaks detection and more generally for network control.

The aim of this paper is to investigate a non-intrusive, low-cost electrical measurement technique for sensing flow-rate, temperature as well as others relevant parameters, likely, in pipeline systems. It is designed and developed for cured-in-place pipes, where sensors and communication bus are suitably embedded between two layers of the liner; the resin cure step will afterward embed the whole measurement system.

By measuring pipe vibration, induced by turbulence when fluid flows within the tube, it's possible, through suitable processing, to evaluate a magnitude related to the liquid flow-rate [1–4], while detecting local temperature at the same time. The technique is based on a tailored digital processing applied to the signal coming out from a tri-axial accelerometer, laying inside the pipe wall. Thanks to MEMS technology, this technique can be potentially very low power and low cost, especially if exploiting economies of scale possibilities.

1.1 Flow Measurement Principle

The flow turbulence is responsible of the transverse vibration induced onto the pipe walls; it depends, among other factors, on the flow rate and the pipe diameter. The molecules of the fluid approaching the wall have kinetic energy, this energy is converted to heat but most is converted into potential energy in the form of pressure. The pressure deforms the pipe converting the energy in kinetic energy, and then again in potential energy when the elasticity of the pipe material applies a restoring force and the deformation end. This cycle of energy conversion causes the vibration of the pipe.

Researches on the turbulent flow show that the fluctuations of the fluid velocity are proportional to the pressure fluctuation and the pressure fluctuations in the fluid are proportional to the acceleration of the pipe. As demonstrated in [1, 2], the standard deviation of the instantaneous velocity in the direction of the primary pipe axis, u, is proportional to the average velocity, $\bar{u}$ (1). The instantaneous velocity can be written as sum of the time averaged speed and the fluctuation velocity. The above mentioned considerations suggest that the standard deviation of the pipe vibration is proportional to the average flow rate (see (1)).

$$\bar{u} \propto \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}\left[u_i(t)-\bar{u}\right]^2} \tag{1}$$

2 System Overview

A simplified block diagram of the system hardware is shown in Fig. 1. Multiple sensor nodes, embedded inside the pipe walls, are connected to the same electrical bus. The bus is also used to deliver power supply to the sensors. The acquisition system, based on an Atmel ATxmega128A1 microcontroller [3], collects the data and estimates the value of the flow-rate and temperature. The measures can be visualized on a display,

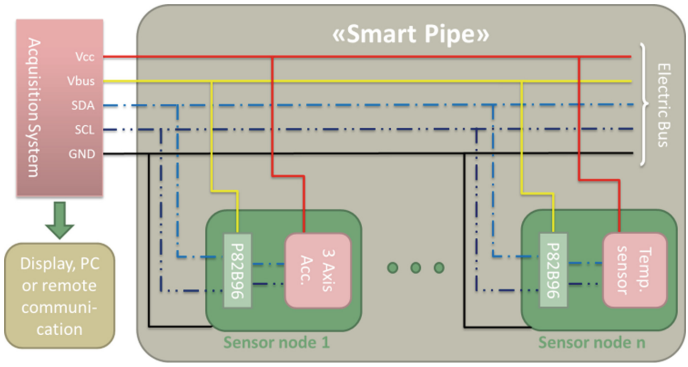

Fig. 1. Functional block diagram of the system

can be sent to a PC or to a remote communication system. The system uses a simple I^2C bus to communicate with the sensors, while further range extension of the reachable length has been obtained with some suitable bus extenders (P82B96 [6]). Using bus extender, the I^2C reach up to 20 m of wire length at 400 Kbit/s.

2.1 Bus Sensor and Installation

Each sensor node has the approximate dimensions of 13 × 11 × 6 mm, connector included. A bus with two accelerometer (LIS3DH [7]) sensor nodes and one temperature sensor (AT30TS75A [8]) node has been installed in every monitored pipe, as it is shown in Fig. 2.

The temperature sensors have a range of –55 to +125 °C with ±0.5 °C of accuracy. The accelerometers have 12 bit of resolution in a range of ±2 to ±16 g and data rate up to 5 kHz.

CIPP liners are made of tubular layers of non-woven polyester felt or fiber reinforced fabric, with an external impermeable layer. The felt is impregnated with polyester, vinyl ester epoxy or silicate catalyzed thermosetting resin using vacuum,

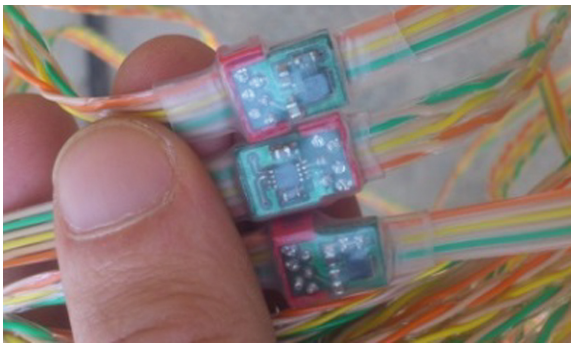

Fig. 2. Sensor nodes mounted on the bus

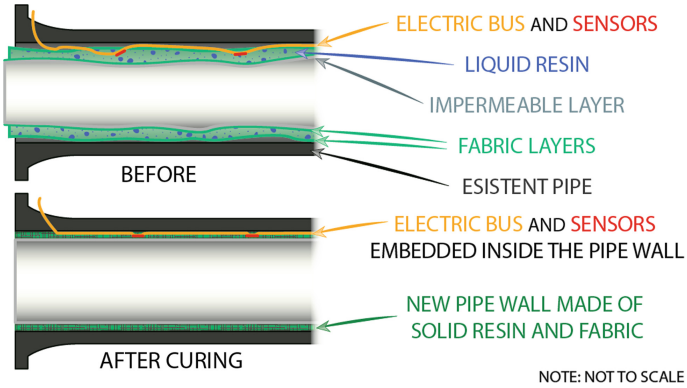

Fig. 3. Installation and curing process effects

gravity or other applied pressure. The CIPP liner is transported to the installation site with refrigerated truck and inserted inside the host pipe by inversion or winched. Then, the CIPP liner is filled with hot water or steam to activate the resin curing phase, while the pressure makes the liner to expand against the host pipe walls.

The effect of the CIPP liner curing process and the sensor bus is depicted in Fig. 3. The pressure, applied during the curing process, expands the bus and the sensors are automatically placed against the pipe wall. As result, the sensor and the bus become embedded into the walls of the CIPP.

3 Test Setting and Results

Once the system has been set up, some tests, described hereafter, were carried out on a test lab of the hydraulic Department at the University of Palermo where part of a 200 m long pipe circuit has been dedicated to the test bed. A nominal diameter of a host pipe of 140 mm of diameter and 647 cm of length inserted in the existing circuit in which the flow control can be controlled by using a valve and measured with a standard and independent flow meter (Fig. 4) sampling the real flow on the return pipe every 5 s.

The accelerometer data was initially acquired using various sample rates and number of samples. Based on these preliminary results, a procedure acquiring 1024 samples with a sample rate of 100 samples/s was used to acquire the measured data, according to the formula (2).

$$\text{flow} \propto \sqrt{\frac{1}{1024}\sum_{i=0}^{1023}\left(|A|_i - |\overline{A}|\right)^2}, \text{ where } |A| = \sqrt{A_x^2 + A_y^2 + A_z^2} \tag{2}$$

Thus, we obtain a measure every about 10 s. To reach a better estimation, the results of several acquisition can be averaged reducing some unwanted fluctuations but at the cost of increasing measurement time. System tests were carried out by measuring

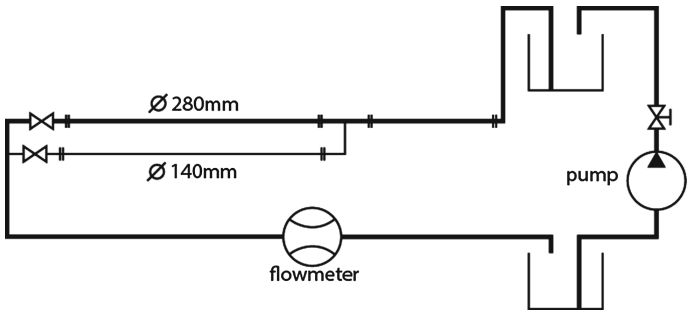

Fig. 4. Simplified hydraulic circuit of the utilized test bed

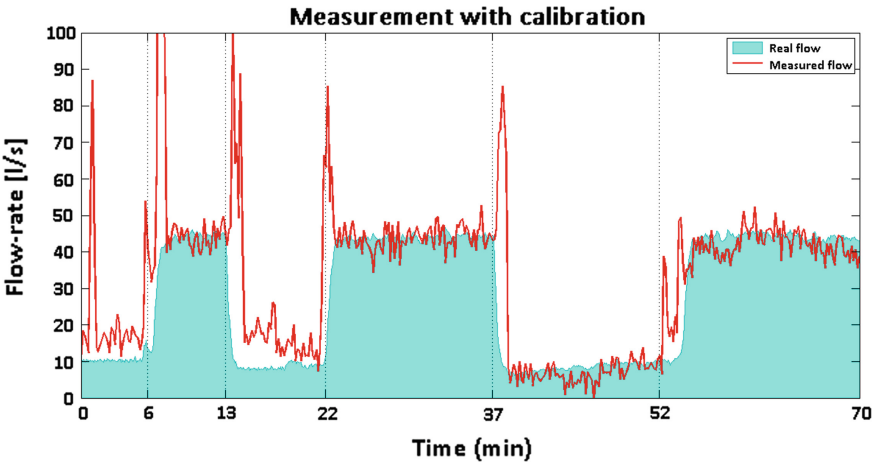

Fig. 5. Measurement results using calibration, compared to the real measured flow

the data related to a series of opening and partially closing the gate valve that controls the flow.

Applying a proper calibration, it is quite clear a relation between the values measured with an ultrasonic flow meter and the ones measured using the, accelerometer based designed system, as showed in Fig. 5.

As for calibration it has been used a linear relationship between the estimated value without any flow and the estimated value at a fixed flow level, detected by using the flowmeter. To reach a better estimation more complex models must be used, as in [3].

The peaks around transitions are caused by the manual opening and closing of the gate valve. Since the pipe is attached to other pipes and mounted on the same supports, there are other sources of vibration and noise present in the data. The effect of these noises is more visible at lower flow rate, hence producing a bigger variation of the estimated flow. For higher flow rate, the effect of the noises is smaller and the estimated signal is more stable.

4 Conclusions

In this work it has been shown that it is possible to set up a cured-in-place pipe process with embedded electronic sensors and bus, despite of the mechanical stress involved in the pipes realization process.

A magnitude related to the flow was calculated by sampling the induced accelerations with a 3 axis MEMS chip. By using a simple calibration process, measured values of the flow-rate has been obtained. The developed algorithm has a computational cost suitable for embedded application on low end microcontrollers. The proposed system has an overall cost of few hundreds of euros to monitor one pipe, but the system can monitor multiple buses, adding only the cost of the buses (tens of euros) to the overall cost. In order to properly cover pipes networks, a data aggregator has to considered and the cost of a global solution may actually increase, while this growth can also bring the typical advantages of economics scale use cases thus lowering the total cost per measuring point. Finally it must also be said that today conventional measurement techniques are usually very expensive (thousands of euros per measured point).

Further studies are needed on some topics in order to obtain a better estimation of the flow, such as noise canceling, external vibration isolation, system response characterization etc. but still the solution appears to be very promising for future developments.

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Delay Tolerant Wireless Sensor Network for Animal Monitoring: The Pink Iguana Case

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Abstract. The design of GPS tracking devices and the related data collection infrastructure is an old task that still presents several research challenges from both a technical and biological point of view. Weight, size, and power consumption of such devices must be made compatible with small-sized species so as not to interfere with their lives and habits. To target the design of the monitoring device and the data collection infrastructure, we choose the Galápagos Pink Land Iguana (*Conolophus marthae*) as a reference case. While the monitoring area is relatively small, the difficulty of the terrain, the lack of any available communication infrastructure and hard logistics offer several challenges. In this paper we present: (i) the board designed and developed by an interdisciplinary collaboration; (ii) the energy budget of the WSN device; (iii) the analysis for the selection of the frequency bands.

Keywords: Animal monitoring · Sensor network · *Conolophus marthae* · Delay tolerant network

1 Introduction

A Wild Animal monitoring network basically consists of a set of devices applied to animals that periodically collect parameters of interest (e.g. position, temperature etc.) and gather them to a collection node (sink node). Despite the apparent simplicity of this specification, the implementation of such devices and the related data collection infrastructure presents several research challenges both from a technical and a biological point of view. Indeed, only recently weight, size and power consumption of electronic appliances became compatible with small-sized species, without interfering with their lives and habits. In addition, system design is a multi-disciplinary task that requires tight collaboration among researchers of different fields to properly understand the relevant parameters to monitor, how to acquire and communicate data collected. Last, but

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not least, how to apply the device on animals without disturbing animals' lives and ecosystem is also an issue.

The Pink Iguana (*Conolophus marthae*) of the Galápagos is considered a strategic species and is used as flag of programs contributing to global conservation funding [1]. The species is assessed as Critically Endangered in the IUCN Red List, that establishes priorities of research needed and conservation actions. Among high priority researches needed are those that attempt to (i) clarify the area of distribution of *C. marthae*; (ii) clarify times and usage patterns of the area; (iii) provide sensible data to develop habitat suitability models; (iv) identify nesting sites; (v) monitor a feral cat population impacting the area. The application of long-term animal-tracking techniques would clearly allow for the accomplishment of such tasks. However prior attempts proved to be ineffective due to a combination of the difficulty of the terrain and hard logistics that limit the duration of field trips, lack of suitable tracking devices, and absence of a network infrastructure.

The Pink Iguana occurs a relatively small area of about $20\,\mathrm{km}^2$, along the slopes of the northern side of the Wolf volcano in the Isabela Island, from 600 m to the top (1700 m). A suitable networking architecture has been studied to retrieve collected data without relying on any pre installed terrestrial communication infrastructure such as cellular networks, which is not usually available in that wild environment. Thus a Delay Tolerant Wireless Sensor Network (DWSN) architecture has been selected for the collection infrastructure.

This paper presents the electronic-design aspects of the delay tolerant wireless sensor node (DWSN node) developed. In particular we presents: (i) the wireless node design in terms of components and sensors selection; (ii) the board energy budget and some harvesting enhancement; (iii) the radio frequency band selection also supported by a preliminary measurement campaign to asses the wireless communication range.

2 Related Work

2.1 Animal Tracking Technology

There are several commercial and research products to track the movements of pets and wild animals such as [2–4]. Among them, the Mataki project [4] has developed an open hardware/open-source low-cost device based on GPS and IEEE 802.15.4 wireless connectivity. The specification of this device have been used as a starting point for the hardware designing activity of our device. It is worth noting that none of the previously mentioned works tackles the problem of data gathering with a Delay Tolerant Networking (DTN), which instead has only been simulated [5].

2.2 Animal Monitoring Networks and Devices

WSNs are an ensemble of distributed nodes that operate at low power, usually interconnected with a low data rate communication infrastructure. An early remarkable experiment of using WSN for animal monitoring is [6]. However only in recent years the development of technology has allowed the development of more complex systems such

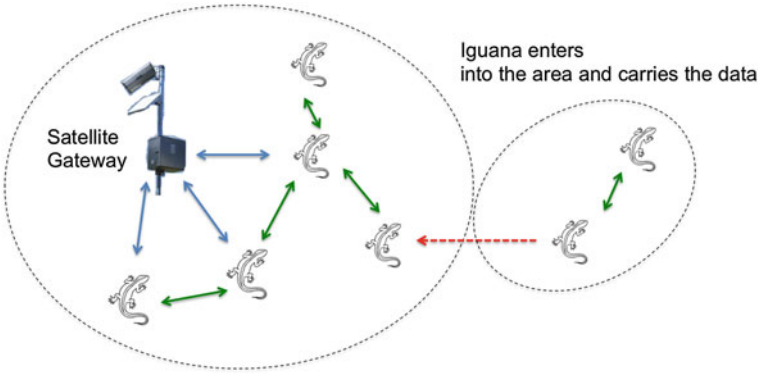

Fig. 1. The Delay Tolerant Wireless Sensor Network scenario with a satellite gateway

as the one described in [7]. DTN studies how several networking nodes can communicate in an intermittently connected networking scenario. Several research works have studied and provided solutions to the problem of data exchange between nodes of these networks, minimizing network latency, power consumption, or memory constraints [8–12]. The introduction of DTN techniques in the WSN can provide an improvement in data gathering performance achievable from the WSN [13,14] and allows the design of an infrastructure network for data collection, mixing long- and short-range wireless technology with ad-hoc routing protocols to realize a low-cost, self-healing networking system. A recent work that make use of this paradigm is [15], but it relays on the cellular network infrastructure for the data collection.

3 Network Scenario

The overall devised communication system is depicted in the Fig. 1. The animals are equipped with the WSN nodes that are able to communicate with the gateway and exploit the opportunistic device-to-device connections available due to animal mobility. The network is connected to the Internet by a M2M satellite transceiver that sends the collected information to a remote server in a delay tolerant manner. Data are exchanged among the device nodes and with the satellite gateway, minimizing power consumption of network devices. Communication is based on advances of delay tolerant network forwarding and routing systems to opportunistically exchange data between terminals in visibility.

To increase the amount of collected data, each terminal stores in a temporary memory the data received by other terminals and forward them to the satellite master or to other terminal when possible. This is a typical DTN scheme, where some of the routing techniques can be used to reach the targets (e.g. adopting a geographical utility function [16]). Given the memory constraints of each device, a suitable strategy to handle data overflow must be taken into account [11]. One reasonable pattern is to provide each data message with a timestamp and a node identifier and to keep at least the two more

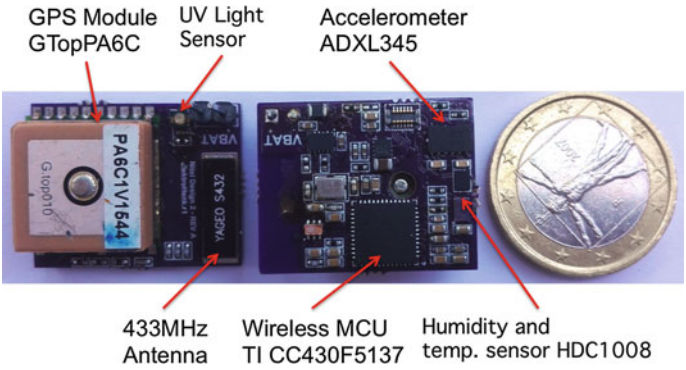

Fig. 2. The first prototype of the designed WSN node

recent packets for each devices for acquiring the last position, speed and direction of the drift of a node.

4 WSN Node Design

4.1 Device Requirements

The monitoring device periodically checks animal movements using the GPS technology and save the positions on a persistent storage. The device must be able to monitor temperature and humidity of the environment, light conditions, animal movement and finally the battery state. To fulfill the measurement campaign requirements, the battery must guarantee at least one GPS point per day for 1 year.

The device has to integrate a low power wireless technology to discover and communicate with the other devices and with gateways.

4.2 Components

Figure 2 shows the first prototype of the WSN node that has been assembled with the following components:

Wireless MCU: the core of the board is the *TI CC430F5137*, a 16-Bit ultra low power MCU that integrates the CC1101 an high performance sub-1-GHz RF transceiver offering a programmable data rate from 0.6 to 500 kBaud in several frequency bands between 300 and 928 MHz.

GPS Module: the monitoring module is the *GlobalTop PA6C* an ultracompact Patch On Top GPS Module that based on the MT3339 GPS Chipset. It has a very good sensitivity (−165 dBm) and a relatively fast TimetoFirst Fix (TTFF) with a low power consumption characteristic both for acquisition and tracking. The GPS module can be switched off with the *TI TPS22967* an ultra-Low resistance load switch.

Sensors: the board is equipped with a *Digital Accelerometer ADXL345*, a *UV Light Sensor VEML6070* and an *Humidity and Temperature Sensor HDC1008*. All the sensors will be used both for biological data collection and for providing data to the firmware to optimize power consumption.

Persistent Storage: the collected positioning data are temporarily buffed in the *ST M24M01*, an I2C compatible EEPROM with 1 Mbit capacity.

5 Power Management

5.1 Energy Budget

The main contributions in the energy budget comes from the GPS receiver (GlobalTop PA6C) and the Wireless MCU (TI CC430F5137): Table 1 reports the energy required for their different operating conditions. We assume as reference case that the device executes one position measurement every 24 h and transmits the position via RF every hour.

The GPS device takes about 33–35 s to calculate the first position (cold start) requiring 3.2375 J of energy in clear sky conditions. Then it can operate in tracking mode and taking only 3–5 s to calculate the new position and requiring about 0.37 J. When the GPS is not needed a switch power the device off. However when the device operates in open areas surrounded by vegetation it can experience some degradation in performances as reported in [17]. In our energy budget we consider the case of only 1 TTFF per day with 5 s of delay due to vegetation. Thus the overall energy required for the position acquisition is about 3.6 J per day. The MCU consumes a large amount of energy for the wireless communication (24 s of transmission requires 2.93 J). When the GPS or RF is not active the microcontroller is in standby mode (LPM3 RTC Mode).

With those assumptions we need a battery of 260 mAh (corresponding to 3463 J) to guarantee about 1 year of device lifetime.

5.2 Energy Harvesting Design

Due to the relatively high power consumption of the GPS module and of the RF module, an energy harvesting circuit has been specifically designed. The new charging components is based on the TI BQ25570, that can efficiently extract up to microwatts (μW) of power generated from a photovoltaic (solar) generator without collapsing those sources. The battery and supercapacitor management features ensure that they will not be overcharged by the extracted power, with voltage boosted, or depleted beyond safe limits by a system load.

In addition to the highly efficient boosting charger, this system integrates a highly efficient, nano-power buck converter for providing a second power rail to sensor devices that have stringent power and operational demands. The use of supercapacitors is strictly required to assure the high power delivery for the duration needed for data packets to be transmitted. Supercapacitors are energy storage devices where capacitance is proportional to charge storage area divided by the charge separation distance, using high surface area carbon to deliver much higher energy density and to hold charges

Table 1. Energy budget of the Wireless MCU and the GPS Module

GPS		Wireless MCU	
Times on in 24 h	1	Times on in 24 h	24
Total on time (s)	40	Total on time (s)	24
Cold start time (s)	35	MCU on time (s)	24
Cold start current (mA)	25	Tx current +13 dBm (mA)	33
Cold start power (W)	0.09	Total on power (W)	0.12
Cold start energy (J)	**3.24**	**Transmission energy (J)**	**2.93**
Tracking time (s)	5	MCU core clock (MHz)	24
Tracking current (mA)	20	μA/MHz	160
Tracking power (W)	0.07	Core clock power (W)	0.01
Tracking energy (J)	**0.37**	**Core clock energy (J)**	**0.34**
Total off time (s)	86360	Total off time (s)	86376
Current consumption off (μA)	0.00	Current consumption off (μA)	7.00
Standby/off power (W)	0.00	Standby/off power (W)	2.6e-5
Standby/off energy (J)	**0.00**	**Standby/off energy (J)**	**2.24**
Total GPS energy in 24 h (J)	**3.61**	**Total micro energy in 24 h (J)**	**5.51**
Total energy in 24 h (J)	**9.12**		

longer than conventional capacitors. Moreover, they have theoretically infinite charge cycle life and very low leakage current compared to rechargeable batteries.

For example let we consider two solar cells 22 mm × 7 mm (KXOB22-04X3L) that can produce up to 240 J per hour in full sun. In this configuration the device needs about a minute of sun for 1 GPS measurement.

6 Transmission Band Selection

There are multiple frequency bands suitable for WSN. The main choice for small low power devices is in the 400 or 800 MHz band.

6.1 433 Versus 868 MHz

433 MHz The 433 MHz band is probably the widest used ISM band. Indeed the 433 MHz band is used throughout Europe and much of the rest of the world also (excluding the US). Both, simple wideband units and sophisticated longer ranged narrowband radios are available. *Pros*: Extremely wide choice of modules from many manufacturers. Integrated circuit solutions are also available, for even lower costs. As the band shows lower path loss than 868 MHz band, so less transmit power is required to reach the same communication range. *Cons*: Low power (10 mW, or 25 mW in Australia). This band is overcrowded in some areas and there are some very low quality hardware on the market, which makes this selection hazardous. Antennas tend to be bigger (a 1/4 wavelength monopole is 16 cm long).

868 MHz A band harmonized throughout the European Union. To improve band usability, some frequency regions within the band are assigned to specific applications (fire alarms, security) and in certain sub-bands there are some regulation constraints that limit the transmission of duty cycle or operating mode (e.g. "Listen Before Talk" or LBT operations). Transmit power varies from 5 to 500 mW. *Pros*: Small antennas, reasonable range. Relatively little band congestion (helped by the sub-band allocations). Wide range of modules available from long range 500 mW units to very simple short ranged 1 mW devices. *Cons*: Greater path loss and worst performance with vegetation. Stronger RF coupling with the animal skin leads to sensible frequency shifts.

6.2 Wireless Coverage

Since the effective coverage area plays an important role in the real effectiveness of the collection network we performed a measurement campaign using the Olimex MSP430-CCRF that is equipped with the CC430F5137 and is designed for the 868 and 915 MHz bands. It comprises an on board antenna that presents 4 dBi of gain and can output up to 10 dBm of radiated power.

We selected a Standard reference configuration with a 1.2 kBaud data rate transmitted using a 2-GFSK modulation and a receiver filter with a 58.03 kHz.

We measured the RSSI and Packet Error Rate (PER) in a open field scenario with the devices suspended at 50 cm from the ground and in a light vegetated environment with one device positioned inside a bush and while the other device is placed near the trees. The results are reported in Fig. 3. The RSSI is measured with 2 min of continuous transmission while the PER is evaluated by sending 100 packets two times with 30 bytes of data.

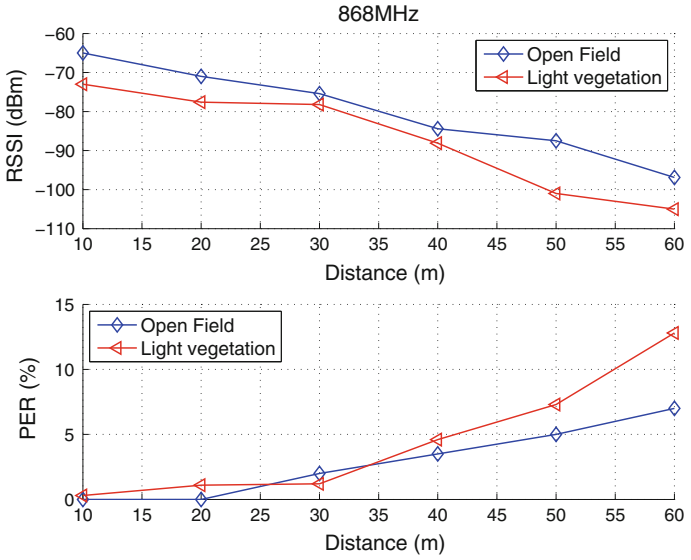

Fig. 3. Measurement campaign at 868 MHz

7 Conclusions

This work shows the importance of interdisciplinary collaboration in the design process of a delay tolerant wireless sensor node for animal tracking. This effort has produced a very interesting prototype that is currently under testing.

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Low Dose-Rate, High Total Dose Set-Up for Rad-Hard CMOS I/O Circuits Testing

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Abstract. In this paper, the planning of low dose-rate, high total dose testing campaign for I/O circuits is reported. In particular, the paper describes all development steps, starting from the rad-hard I/O circuits design and the implementation of the test-chip, which is meant to allow comparative testing between rad-hard and standard devices. The designed experimental setup permits in situ measurements, therefore the circuits behavior can be remotely monitored for very long periods. This feature enables low dose-rate testing up to very high dose.

Keywords: Low dose rate · Rad-hard I/O circuits · Radiation effect

1 Introduction

In space environment, semiconductor integrated circuits (ICs) suffer radiation effects, which cause degradation of devices characteristics and circuits failures [1]. In fact, specifically in MOS devices and circuits, ionizing radiation leads to Total Ionizing Dose (TID) effects, which are caused by radiation-induced oxide-trap charge or interface-trap charge buildup. Oxide-trap charge determines negative threshold-voltage shifts and excessive leakage in MOS gate-oxide and parasitic field-oxide structures. On the other hand, interface-trap charge causes positive threshold-voltage shifts in n-channel MOS transistors, which can lead to speed and output drive performance degradation in CMOS devices and circuits [2–4]. Therefore, in space applications, hardening circuits against radiation effects is essential to avoid premature failures.

An IC must communicate with the harsh external world handling voltage and current signals that may destroy the device itself. Input and output (I/O) circuits provide proper interface and communication between the external environment and the internal core circuits. Specifically, I/O libraries have to cope with buffering, translating and interfacing of signals from external devices to internal circuits and vice versa [5, 6].

Correct communications from and to an IC are essential in electronic applications, therefore, in radiation environments, avoiding that radiation affects I/O circuits is crucial for allowing ICs to receive/send uncorrupted commands and signals. In effect, erroneous behavior of I/O circuits would determine the IC to be isolated from other

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external devices and consequently the functionality of the entire electronic apparatus, the affected IC is exploited in, would be corrupted. Therefore, the design of radiation hardened I/O circuits is mandatory.

The radiation hardness of designed circuits has to be checked through proper testing campaigns. In particular, as far as TID testing is concerned, measurements must provide the cumulative dose a component can withstand without failing. Moreover, in order to accurately stress the system for highlighting possible weaknesses in conditions as much similar as the operating ones, the proper dose-rate has to be chosen. In fact, the types of radiation effects and the dose at which the circuits fail, strongly depend on technological process, bias conditions, radiation type and dose rates [7–9]. Space is considered a low-dose-rate environment and space missions are long-term, determining a high amount of cumulative dose in the electronic apparatus. Therefore, low-dose-rate, high TID irradiations should be performed for evidencing specific effects, such as nMOS threshold voltage rebound. Moreover, low-dose rate irradiation causes more severe degradation in terms of leakage current than high-dose rate irradiation [7, 10].

In this paper, we describe the design of radiation-hardened-by-design (RHBD) I/O circuits in the IHP 250 nm Si-Ge BiCMOS technology, whose CMOS masks have been exploited. The designed circuits were integrated in a test-chip specifically planned for low-dose-rate TID testing. In particular, the test-chip features redundant testing structures and separated supply lines in order to monitor the current leakage and the timing characteristics of the different circuits.

2 RHBD ESD Protections

Electrostatic discharge (ESD) is the transient discharge of static charge, which can arise from human handling or contact with machines and whose characteristic is high voltage or current stress occurring for a very short interval of time [11]. In the semiconductor industry, ESD represents one of the most critical reliability issue: in fact, the high voltages result in large electric fields and high current densities in the integrated devices, which can cause breakdown of insulators and thermal damage in the ICs.

The solution to protect ICs from ESD events is to discharge the high current via a low impedance shunting path or clamp the pad voltage to a sufficiently low level or ground. Typical circuital solutions consist in exploiting properly designed clamp devices, such as diodes and nMOS transistors.

In our design, we employed foundry supplied ESD diodes to protect both analog and I/O pads: Fig. 1a shows the circuital schematic. On the other hand, gate-grounded nMOS clamp transistors, which have greater current handling capabilities than diodes, protect the power supplies pads: Fig. 1b shows the circuital schematic. The foundry supplied nMOS clamp devices consist of two-edge multi-fingers transistor structure with proper gate-drain offset and silicidation blocking of source and drain diffusions in order to increase the resistance between gate and drain contact and force a more uniform current flow through all the fingers of the nMOS transistor. Since a two-edge MOS structure is exploited, TID induced edge current leakage can occur, especially at high dose, with the consequent increase of power consumption from the supply. Therefore, in our design, we hardened the cells against the reported TID effect. The

nMOS clamp devices were developed by exploiting an annular layout while keeping the drain-gate offset and the silicidation blocking of source and drain diffusions.

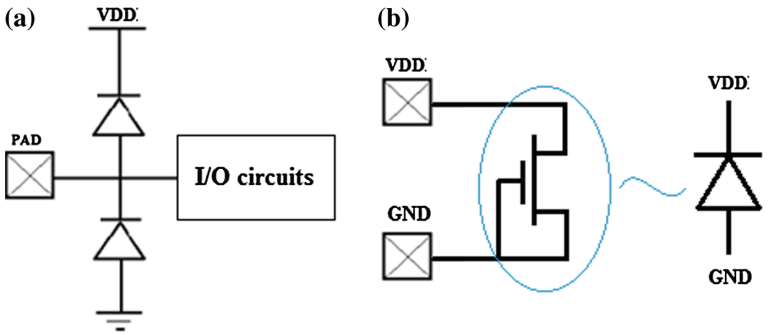

Fig. 1. ESD clamp devices connections: **a** ESD diodes protect signal I/O circuits, **b** ESD NMOS clamp transistor protects supply pads

3 RHBD I/O Circuits Design

A typical I/O circuits library basically consists of input pads to drive the signals from the external world to the core IC, an output pad to buffer the core signals to the external devices and a bidirectional pad acting as input/output pad. Each I/O circuit must contain ESD protections and buffer circuits to drive the IC pads or the internal routes to the core circuits.

In our RHBD I/O library, an input pad with 16x buffer and a bidirectional pad were implemented in order to have the same circuits topologies as in the standard library provided in the design kit. As an example, a simplified schematic of the designed bidirectional pad, whose input branch consists of a 16x buffer, is reported in Fig. 2.

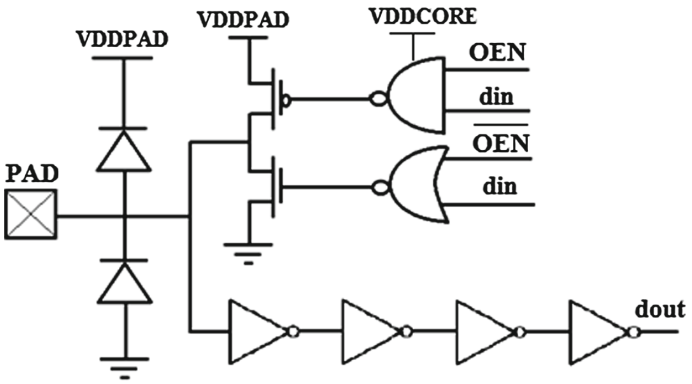

Fig. 2. Simplified circuital schematic of implemented I/O bidirectional pad

The designed I/O circuits exploit two separated supply rails, i.e. V_{DDPAD} and V_{DDCORE}: long channel MOS transistors implement the circuits connected to V_{DDPAD}, while minimum channel devices are exploited for the design of the circuits supplied by V_{DDCORE}.

Moreover, we designed two simple analog pads consisting of ESD diodes protections and metal structures in order to be used for directly connecting I/O circuits nodes to the bonding pad.

The following designing techniques were used to mitigate the radiation effects:

- Both nMOS and pMOS devices exploit an enclosed layout: this allows for preventing leakage currents and threshold voltage shifts;
- nMOS and pMOS devices are integrated in separated wells and guard rings are employed generously for preventing latch-up phenomena and intra-devices leakage currents.

Signal pads are protected against ESD through diode devices, which are not affected by TID effects since insulating oxide layers are not exploited, whilst the modified ESD clamps described before are exploited as supplies protections.

4 Test-Chip Design

The test-chip was specifically designed for performing functional tests of I/O circuits in both standard conditions and under radiation (TID) and for evaluating the radiation tolerance of the rad-hard I/O circuits with respect to the standard ones. Those testing structures allow for creating an input/output communication to and from the test-chip and for testing the single I/O circuit functionality. Moreover, in order to monitor the current consumption of the different testing devices several separated supplies are exploited. In particular, a dedicated supply powers the analog pads in order to allow for monitoring the current consumption of the ESD devices. Figure 3 shows one of the integrated testing structures, which exploits the implemented bidirectional circuit. The figure highlights also the power lines used to supply each circuital block.

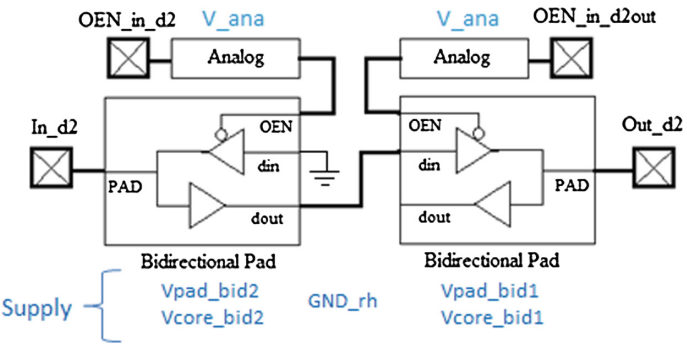

Fig. 3. Testing structure integrated in the test-chip: bidirectional pad in input mode connected to a bidirectional pad in output mode with enable pins wired to analog pads

Finally, it is worthwhile underlining that the test-chip integrates both rad-hard and standard I/O circuits in a symmetric layout.

5 Tests Campaign Planning

Since we target to reach high dose, i.e. several Mrad, even though maintaining a low-dose rate condition, we decide to use an in situ testing method in order to automatically collect the measures of interest over a long period. In this way, the long-term effects can be measured too. In particular, the test-chip characterization has the following targets:

a. Performing behavioral tests at standard conditions and under ionizing radiation (^{60}Co source) in order to estimate the radiation tolerance of designed circuits with respect to the standard ones;
b. Evaluating the TID effects at different doses and dose rates, in particular on timing characteristics, power consumption and leakage currents of both digital circuits and ESD devices.

Gamma irradiation tests will be performed with ^{60}Co sources by exploiting the IGS-3 irradiator at the Department of Energy, Information Engineering and Mathematical Models of the University of Palermo [12]. The IGS-3 is located inside a bunker with controlled environmental condition. The test campaign will be performed according to the European Standard ESCC 22,900 in the low-dose rate range, i.e. from 36 to 360 rad/h [13].

The timing characteristics of the testing structures, i.e. input-output delay and rising-falling edges, are evaluated through the analysis of input-output waveforms plotted on an oscilloscope. The use of redundant supply pads allows for monitoring the power consumption of the different circuits, working in specific load conditions. Moreover, we can monitor the power consumptions variations with TID of both long channel devices based circuits and minimum channel devices based circuits by keeping the external supply V_{DDPAD} separated from the core supply $V_{DDCORE.}$ The current consumption is measured from each one of the integrated supply pads in normal operating conditions, that is at 2.5 V power supply and 1 MHz square wave input signal, while the leakage current is monitored in static conditions, at both low level input and high level input.

The described testing campaign will be performed exploiting the experimental setup shown in Fig. 4, which consists of the following main functional blocks:

- A 12 V power supply is used for biasing the switch matrix and a linear regulator generates the 2.5 V supply for the testing board;
- A switch matrix (relays) allows for switching the DUT supplies between the main 2.5 V supply (normal mode) and the Source/Measure Unit (SMU) (testing mode) set in voltage mode and current measurement at 2.5 V;
- A STM Nucleo-F401RE microcontroller board generates the 1 MHz square wave signal, the dc input signals and the relays control signals;

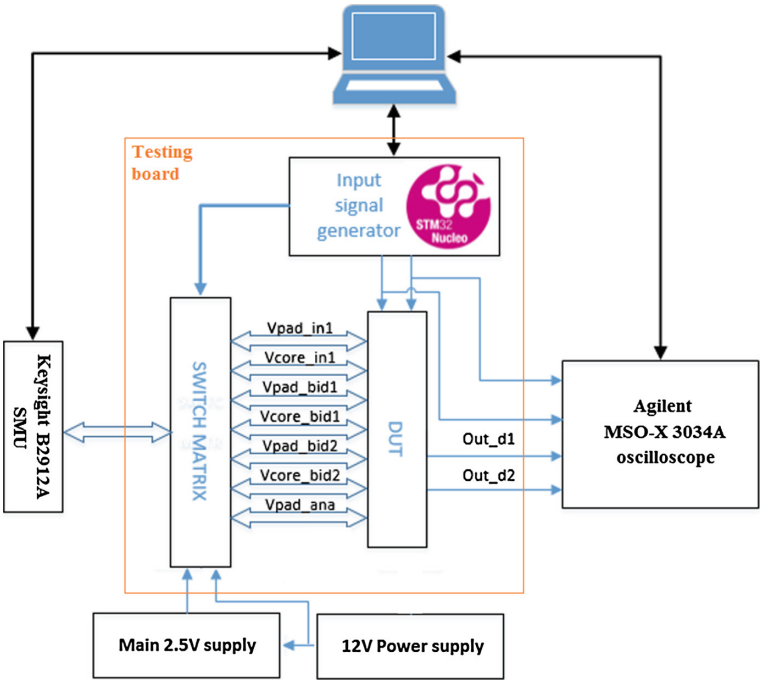

Fig. 4. Simplified block diagram of the proposed experimental setup

- An Agilent MSO-X 3034A oscilloscope allows for visualizing and for acquiring the DUT input-output waveforms;
- A Keysight B2912A SMU allows for accurately measuring the current consumption.

A dedicated software developed in the NI Labwindows/CVI environment manages the implemented setup and gathers the measurement data.

6 Expected Results and Discussion

The planned testing campaign will allow for estimating the radiation tolerance of the designed I/O circuits with respect to the standard solution. Moreover, the implemented setup will permit to characterize the circuits at low dose-rate, for long time, during normal operating conditions in harsh environment.

We expect that radiation effects up to few Megarad will not affect the radiation hardened I/O circuits. On the other hand, standard pads should suffer leakage currents and behavioral variations starting from few tens of kilorad.

With respect to [14], the proposed experimental setup together with the designed test-chip permit to investigate deeply TID radiation effects on the implemented I/O circuits: in fact, both current consumption from each supply line and dynamic behavior

of integrated devices can be monitored. In particular, the former allows for analyzing leakage effects in different biasing and operating conditions of the I/O circuits.

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Engaging Self-powered Environmental Sensors via Serious Gaming

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Abstract. The monitoring of the Urban Environment requires the placement of many sensors around the City. Regular replacement of batteries is a significant additional cost. Can we enlist the public to keep the sensors charged, while keeping it entertained and engaged? The gamification of energy generation aims at inviting members of the public to interact with the energy generating device (EGD) to ensure that environmental sensors are constantly powered. As a collateral benefit, the physical and emotional involvement of the public with the EGD and the game are expected to raise their awareness and acceptance of environmental monitoring. Here we introduce the development of a hand-powered EGD and its installation on Newcastle University Campus.

Keywords: Energy harvesting · Environmental monitoring · Serious gaming · IoT

1 Introduction

The locution "energy scavenging" was coined a few decades ago to indicate the generation of small electrical energy starting from some other form of energy present in the environment: vibrations, heat, radiation, etc. The initial purpose was simply the powering of small wireless sensors (a.k.a. motes) without recurring to batteries [1]. The term energy harvesting (EH) has recently been extended to include large scale generation from alternative sources or the tapping of energy which is not entirely free, but may require modest amounts of primary energy. Examples are radiation-based harvesters incorporating small radioactive sources [2] and most forms of wearable EH, where muscular work, often from a deliberate action, is converted into electrical energy [3].

Modern cities are becoming smarter and smarter. Applications of the Internet of Things (IoT) permit the integration of transport, the optimisation of traffic, the monitoring and control of air pollution, the coordination of emergency actions. Essential to several of the possibilities just mentioned is the deployment of sensors to collect a wide range of data. Besides the cost of purchase, the costs of installation and maintenance (dominated by battery replacement, if this is how sensors are powered) are the main deterrents to an ever denser distribution of sensors around cities.

The use of nano-turbines at the roadside to power road signs, often supplemented with small photovoltaic panels, has become quite common in recent years. Within the

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built environment of a city, neither energy generator is ideal, either for want of direct sunlight or for safety concerns. An alternative source of energy would be welcome.

Another important factor is of a completely different nature: how do citizens feel about such tight monitoring of their environment? do they see the advantages or do they feel hostility against what could be perceived as a big brother?

Newcastle University is currently funding, via Science Central, an ambitious project to monitor the City at multiple scales. As part of the Urban Observatory, a web portal (http://uoweb1.ncl.ac.uk/) presents live and stored data including air quality, parking spaces, river levels, etc. The aim of the project summarised in this work was to design and deploy an energy generating device (EGD) capable to supply electrical energy to environmental sensors while engaging the public in a game, to foster public uptake and participation.

1.1 EGD's Topology and Game Mechanics

The design of the EGD was governed by two main objectives: efficacy and engagement. It was desired to develop a device capable of generating with a maximum efficacy to make the most of each user's interaction. Large powers were sought, being careful not to demand too much time, as this could reduce future interactions. Naturally, as the most efficient generator would produce no power without input work, the second main objective was to design a game that engaged the public. Several ideas were considered: pedals pushed by stepping on them were discarded due to the difficult installation; bellows that could be used to forge a virtual sword required an overly complex game to support them. Additional considerations included, weather worthiness, public safety, cost and resilience to vandalism.

The selected design is based on a handle-driven EGD mounted at shoulder level. The game runs on a mobile phone for quick and easy adoption by the public. As the handle rotates, an LED panel, monitored by the game via the phone's camera, flashes at a frequency proportional to the handle's speed. The game mechanics was designed to encourage the optimal rotational speed of the handle, as dictated by the efficiency of the generator: a clock handle ticks away and can be held back by turning the handle at the correct speed. As time passes, the required accuracy increases until it becomes impossible to achieve it and the game ends.

The EGD was programmed to flash some data—energy produced and battery level—at the end of the game, based on which the user is rewarded. The reward is proportional to the need of a specific sensor to be recharged. The game displays the battery levels of all sensors available (as this EGD was a unique prototype, this aspect of hunting for the best reward was not applicable).

2 The Energy Generating Device

Design of the mechatronic system and selection of the components were done with a holistic view, but they are here split in subsections for convenience.

2.1 Electromechanical Generator

Since it was expected that power would be produced in short but energetic bursts, electromechanical generators were deemed more appropriate than alternatives like piezoelectric transducers, commonly used in EH. From ergonomics data [4] it was found that a comfortable operating condition could be achieved with a crank of radius ~20 cm rotated at about 1 turn/second and requiring a force of 15–25 N, corresponding to a torque of 3–5 Nm and a mechanical power of about 20–30 W.

The selection of the generator was quickly narrowed down to the Maxon range of DC and 3-phase AC motors due to the reputability of the manufacturer and the availability of all technical specifications required. The objective was to identify a machine with rated power in the range 20–50 W, appropriate torque and optimal winding. Early considerations showed that the efficiency of the AC range was not significantly superior to DC machines, which were therefore preferred, for the greater simplicity of early power management.

For the selection of wiring and gear ratio, an analytical approach was taken, which is briefly summarised below.

The power balance before and after the Power Management Unit (PMU) is:

$$\eta_{PMU} V_g I_g = V_{out} I_{out} \tag{1}$$

where η_{PMU} indicates the efficiency of the PMU, the g and *out* subscripts refer to quantities *from the generator* and *out of the PMU*, respectively. Considering that the input comes from an electromechanical machine and the output charges the batteries:

$$V_g = kg\omega_h - R_g I_g; V_{out} = V_b + R_b I_{out} \tag{2}$$

where k is the electromechanical constant, g the gear ratio, ω_h the angular speed of the handle, R_g the armature resistance, V_b the batteries' voltage and R_b their resistance. Combining (1) and (2), solving for I_g and selecting the lower branch:

$$I_g(\omega_h) = \frac{k\omega_h g}{2R_g} - \sqrt{\frac{k^2\omega_h^2 g^2}{4R_g^2} - \frac{(V_b + R_b I_{out})I_{out}}{R_g \eta_{PMU}}} \tag{3}$$

where we indicated that the interest is in the dependence on the handle's speed. The discriminant Δ is negative if we attempt to draw more current than is actually available. This means that as long as the demand of I_{out} cannot be satisfied, it will be limited by the power available (and calculated by setting $\Delta = 0$); in the same regime, I_g will increase linearly with ω_h (this is reflected in the initial linear region in Fig. 2a, since $\tau_h = kgI_g$). Once the limiting power becomes the one at the output (determined by the required I_{out}), I_g must decrease as ω_h (and therefore V_g) keeps increasing. The plots in Fig. 2 were obtained assuming $V_b = 3.7$ V and $R_b = 0.1\ \Omega$; the resulting V_{out} was always below 4.2 V. The data plotted in Fig. 2 were calculated assuming the PMU had an efficiency of 80%.

The idea was to introduce a control system which regulated the handle's resistive torque τ_h via the output current from the PMU, since, assuming a viscous friction in the generator with coefficient c:

$$\tau_h = g\frac{kI_g + c\omega_h g}{\eta_{gh}} \tag{4}$$

where η_{gh} is the mechanical efficiency of the gearhead.

Expression (3) and others derived from it were plotted in MATLAB with parameters from Maxon's datasheets and expected operating conditions and used to select the optimal generator. Particular attention was devoted to: the overall efficiency of the EGD; the torque demanded on the handle; V_g, as the PMU, essentially a buck converter, would not switch on below about 6 V. Some examples, for the motor-gearhead selected, are reproduced in Fig. 2. A 36 V motor (Maxon RE 30, P/N 310,008) was selected, paired with a 79:1 ceramic planetary gearhead (P/N 166941) that can handle up to 6.0 Nm. Although a 1:1 transmission was deemed suitable, a V-belt was introduced between handle and gearhead-generator to isolate the latter from excessive torques or loads, axial or radial, applied, deliberately or accidentally, to the handle.

2.2 Power Management and Energy Storage

The core of the PMU is a DC-DC buck converter based on the LTC3741-1. This was configured for a maximum output voltage of 4.2 V to satisfy the manufacturer's recommendation regarding the batteries charging (two 4.5 Ah Li-Ion batteries of nominal voltage 3.7 V). The output current I_{out} is set by the voltage applied to a control pin, which was wired to an analogue output of the ATMEGA328P microcontroller.

A 24 V Zener diode (Solid State, 1N3321B) with power dissipation of up to 50 W was connected to the output of the rectifier to limit the voltage to the PMU, whose MOSFETs are rated V_{DS} = 30 V. This means that, if the crank is turned too fast, power in excess of what can be injected in the batteries will be dissipated.

The role of a 15-A full bridge rectifier (Vishay, GSIB1580-E3/45), connected to the output of the generator, is twofold: to permit either direction of rotation of the handle and to prevent the battery from driving the generator as a motor through the body diodes of the switching MOSFETs. A current monitor (Diodes Inc., ZXCT1110W5-7) paired with a 20 mΩ resistor (1% accuracy) sensed the current I_g entering the PMU; this was used to estimate the input torque (τ_h) and the electrical power into the PMU (V_g was directly measured).

2.3 Controller

The EGD is controlled by an ATMEG328P on an Arduino Uno board. This was selected for rapid development, although it is recognised that a host of ancillary components on the board significantly increases the overall power consumption.

The microcontroller is normally off but connected to the PMU. As soon as the handle's rotation generates sufficient voltage to power it up, the microcontroller

switches a latching relay to ensure it is constantly supplied from the batteries. It then monitors the input torque, estimated via the generator's current (Eq. 4). A PI algorithm adjusts the output current from the PMU to help the user crank at constant speed: if faster, more current/power is demanded, which increases handle resistance, and viceversa if the handle's rotation slows down. The result is a comfortable operation. At every iteration, a tally is updated of the cumulative energy produced in the session. Periodically, data are saved to an SD card in a running log: time; instantaneous voltage and current from generator; handle speed. When the generator voltage drops below a set threshold, the microcontroller enters a waiting state, to determine if the user really intends to stop playing. Once that timeout elapses, the microcontroller disconnects itself and the batteries from the PMU via another latching relay, the batteries voltage is measured and usage data are saved to an SD card in a summary log as well as transmitted to the phone via a sequence of alternate flashes of red and green LEDs. One byte of information is transmitted, twice for redundancy: one nibble contains the battery voltage, the other the energy produced in the session. Finally, the microcontroller reconnects to the PMU and switches itself off by triggering the fist relay mentioned.

3 Results and Discussion

As Fig. 1 shows, the EGD has been decorated with original characters to appeal to passers-by; a QR code is printed on the front to give a quick way of downloading the game; 3-step instructions are offered in text format on the side and graphically on the front. The EGD has been installed on a metal post on Newcastle University campus, near the Devonshire building, in September 2015. The device has been removed a year after to assess the condition of the internal components and to download the usage data stored in the SD card. Unfortunately, the weather-proofing was not successful and tens of cubic centimeters of water were found inside. The water did not directly submerge any electronic component, but it created a saturate atmosphere: abundant condensation covered every internal component. Despite rust and oxidation, the EGD was still perfectly operational once new batteries were connected, but the original ones had suffered serious damage and, once generation had stopped, were unable to keep

Fig. 1. The Energy Generating Device installed on Newcastle University Campus

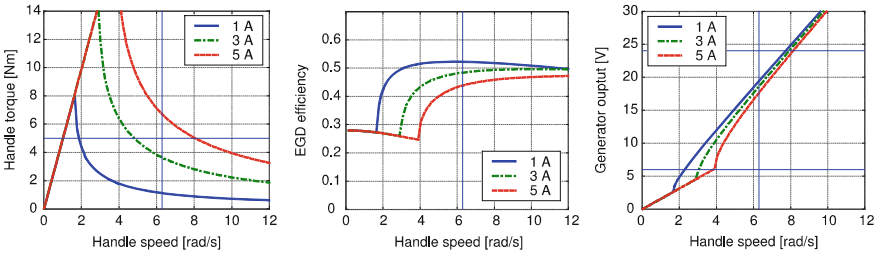

Fig. 2. Some performance indicators of the EGD, calculated from Eqs. 3 and 4 as a function of handle speed for a selection of required output currents. Some *straight lines* are added to indicate targeted speed, torque and voltage requirements

supplying neither the micro-controller nor the real time clock (RTC). For this reason, the last time-stamped entry found on the SD card is dated 2016-04-10; subsequent entries were all time-stamped 2000-01-01, indicating the RTC had reset. The summary logs are absent after that date, since they are saved on battery power.

Focusing on the first 7 months, when complete and reliable data is available, about 330 distinct interactions have taken place. As Fig. 3 shows, they were most often very brief events in which very little energy was produced (80% below 50 J). It is possible to imaging that in these cases the users turned the handle once or twice, just to see what happened. Regarding the time distribution, higher interest is observed at the beginning, coinciding with the beginning of the term (first week of October). The cumulative energy output by the DC generator is also reported on the last graph in Fig. 3 and shows how the numerous events observed in September/October 2015 have been very low energy ones. A total of 18 kJ were generated in the 2400 s of activity, with an average power (while active) of 7.4 W and an overall average power of 1 mW. A further 200 events were recorded between April 2016 (when the RTC reset) and the beginning of September 2016, when the EGD was removed, but reliable data on total energy produced is not available for them.

Regarding the game, issues with the server and with camera-compatibility prevented the collection of usage data, although we do know that the game was

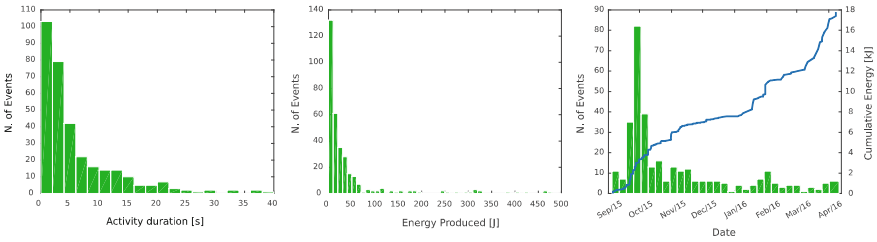

Fig. 3. Histogram plots indicating the number of interactions from users binned with respect to their duration (*left*) and the energy produced (*right*). Five more events lasted more than 40 s and another five produced more than 500 J each

downloaded 16 times, including by people associated with the project. It is estimated that about a dozen genuine users have used the game and registered an account.

4 Conclusions

A hand-powered electromechanical generator has been designed, built and installed on campus for 12 months. The device worked as designed during lab testing, however insufficient weather-proofing caused anomalies 7 months after installation due to water infiltration.

The large number of interactions recorded suggests that the device was successful in attracting the attention of passers-by, although most of these appear to be just occasional users who produced little energy. When this level of interest is contrasted with the very low number of game downloads, we deduce that the targeted public (mostly university students) is reluctant to engage in this way. It is suggested that focus is given to some form of immediate "action" happening on the EGD itself, to satisfy the initial curiosity of the occasional users and keep them engaged. The lack of sustained interest from the public translated into overall poor power generation. A sheltered location would be beneficial not only to the EGD itself but also for public interaction, in particular if it was, rather than a transit area, a place where people stop to rest or socialise.

Acknowledgements. The gaming aspects of the project were developed by Dr. Graham Morgan and Richard Davison from the School of Computing Science, Newcastle University. The original characters that decorate the EGD were kindly created by Perry Bakas. The project was supported by Science Central via the Urban Observatory, both of Newcastle University.

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Flora Monitoring with a Plant-Microbial Fuel Cell

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Abstract. Plant-Microbial Fuel Cells are a promising technology as energy supplier for many different applications in precision agriculture and environmental monitoring. In this article, we discuss and analyze the possibility to use it also a small scale biosensor to monitor a plant health and report information with an embedded wireless sensor node. We present a prototype that exploits the electric energy generated by bacteria to power the embedded electronics and some sensors, while the rate of energy generation is used as a feedback on plant's health state.

Keywords: Microbial fuel cell · MFC · Energy harvesting · Energy neutral · Transient computing · Internet of things

1 Introduction

Going low power and having a low or neutral impact on the environment is nowadays a key feature for embedded systems, as electronics is nested not only in industry but even in almost everything close to everyday life. In this paper we present a self-sustaining, ultra-low power smart device, powered by Terrestrial Microbial Fuel Cell (MFC) and capable of sensing light, temperature and humidity and sending via radio transmission to the end user. The choice of a MFC as an energy harvester leads to a portable, compact and green solution and, thus MFC is an alternative to other fuel cells [1] or accumulator technologies [2].

Energy harvesting is a process by which energy is collected from the surrounding environment and used to increase the battery autonomy exploiting wind [3, 4] light [5], thermoelectric generators [6] or magnetic harvesters [7]. However, the design of an embedded system based solely on these technologies may be a difficult task due to the difficulties in managing sporadic spikes of power consumption and to predict energy intake [8]. Moreover, harvesters may not provide constant energy throughout the day: a solar cell is efficient only during daytime, and a thermoelectric harvester strongly depends on the temperature difference between the heat source and the external environment.

We propose the use of Terrestrial Microbial Fuel Cells as a valid and sustainable alternative to both conventional energy harvesters and common batteries. In fact, despite being a fascinating field of study for biologists/scientists, this technology has not been fully exploited for powering consumer electronics yet and we strongly believe

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that, in a near future, it could become a solid alternative to other renewable sources. MFCs do not produce additional greenhouse gases or waste of any kind [9], can be deployed in a wide range of environmental conditions and can be used to build a self-sustaining system. We prototyped a compact, portable, self-sustaining and green out-of-the-box solution capable of sensing environmental conditions such as temperature, humidity and light intensity and periodically send them through a radio transmission to the main node.

As a main concept/idea, the solution we created can be part of a smart building as a green client node able to independently perform environmental measurements and communicate wirelessly to the server; however, it can be also embedded in a bigger green city area, e.g. parks.

Fuel cells are energy harvesting devices that produce electricity out of chemical energy by breaking chemical bonds of specific substances; in general, they are made up of two electrodes (an anode and a cathode) and an electrolyte that allows the flow of protons from the lower potential electrode to the higher one.

Typically, oxidation happens on the anode, where electrons are produced from Hydrogen and cations (positively charged ions, e.g. in this case H+) are released. Electrons then move from the anode to the cathode through a wire to power the load, while cations are free to move directly to the cathode thanks to a Proton Exchange Membrane (also indicated as PEM), a special medium that facilitates this operation but avoids electrons from passing through it, forcing them to flow through the electronic circuit. At the cathode, protons, electrons and usually oxygen are combined to form the waste product, in this case water. As long as fuel (typically hydrogen) is supplied to the system, the reaction keeps going on and electrical energy is produced.

Terrestrial Microbial Fuel Cells operate in a very similar way, consisting of a bio-electrochemical system that produces current by exploiting the capability of particular species of micro-organisms (electrogenic bacteria such as Shewanella and Geobacter) to produce electrons as a result of their metabolic processes [10]. In this kind of fuel cells, soil is used both as a proton exchange membrane and as source of organic matter. Bacteria fulfil the role of catalyst as a biofilm that donates electrons to the anode, and chemical reactions involve simple sugars that produce carbon dioxide, electrons and protons, the latter two combining at the cathode with oxygen to obtain water. The presence of electrogenic bacteria in nearly every kind of soil is one of the further advantages of this technology. In general, the system operates with satisfactory results in mild conditions (between 20 and 40 °C, at pH 7).

The cell used in our prototypes consists of a cylindrical plastic can with height of 10.1 cm and width of 9.5 cm, filled with nutrient enriched soil to feed the bacterial culture, as illustrated in Fig. 1.

Plant-Microbial Fuel Cells (P-MFC) can be seen an evolution of MFCs, as illustrated in Fig. 2, and make use of naturally occurring processes around the roots of plants to provide additional nutrients to the bacteria, in addition to substances that are already present in the soil. The plant produces organic matter from sunlight and CO_2 via photosynthesis. Up to 70% of this organic matter ends up in the soil as dead root material, that can be oxidized by bacteria living at and around the roots, releasing CO_2, protons and electrons. Since the metabolic process of the bacteria only implies the use of waste material, plants increase the energy production of the fuel cell without any

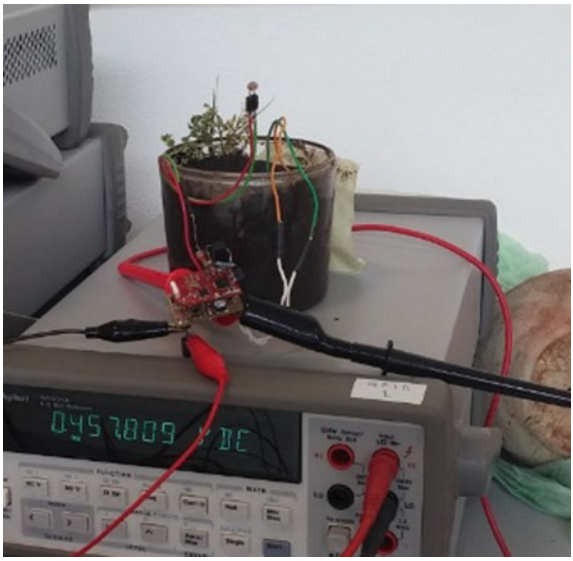

Fig. 1. Cylindrical plastic container filled with nutrient enriched soil used for our tests

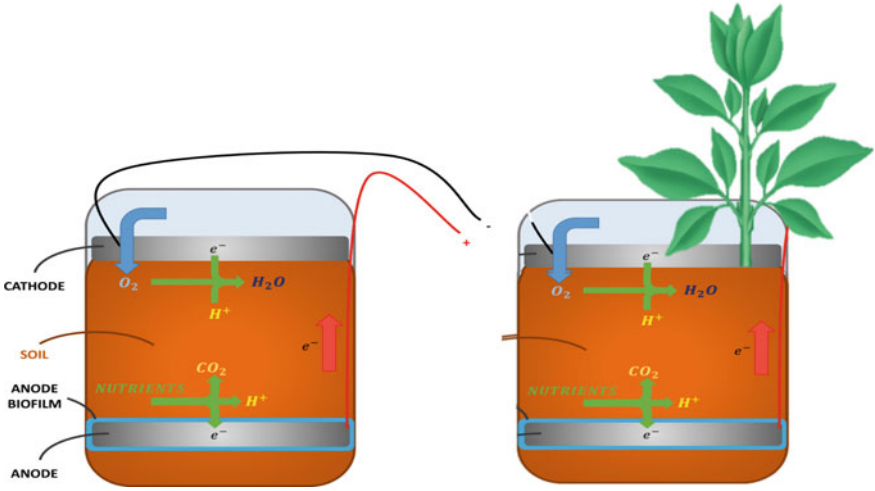

Fig. 2. Schematic principle that turns a MFC into a PMFC

negative consequence on their health. Closing the loop, the combination of plants and mud can be used to generate small, yet sustainable, green and available amounts of electricity.

The cellular metabolism of bacteria in an anaerobic environment generates electrical energy, and the PMFC can be modeled as a variable DC source that mainly

depends on the health of the colony. The cell potential (driving force for current generation) is the difference between cathode and anode potentials. The maximum potential difference between the two is determined by the reduction and oxidation processes.

The reduction process in the cathode is, oxygen reduction in water,

$$O_2 + 4H^+ + 4e^- \rightarrow 2H_2O \tag{1}$$

and the oxidation process in most MFCs uses acetate-like oxidation

$$CH_3COO^- + 4H_2O \rightarrow 2HCO_3^- + 9H^+ + 8e^- \tag{2}$$

This biosystem can have a very long autonomy, if the soil is rich of nutrients and the current drained by the load is sustainable (e.g. months without feeding the cell). The output voltage that a cell can provide is determined by the redox potential between the two electrode environments and the theoretical maximum open circuit voltage between the two electrodes is 1.2 V, with a healthy bacteria colony [11, 12]. We did experiments to characterize the electrical performance of the MFC, and results show that the maximum power achieved in our setup is about 300 μW with a load resistance of Rload ≈800 Ω.

When the PMFC has grown a stable colony of bacteria, the electric production changes regularly with the amount of nutrient and according to the lifecycle of the plant (e.g. day and night). In fact, the plant's roots fuel the electrochemically active bacteria at the anode by excreting chemical organic compounds, including sugars and organic acids, into the soil that eventually enriches the amount of bacteria's nutrients. The main factor that can influence the production of energy is the status of health of the plant. In fact, if the plant is attacked by parasites or the growth is not regular, the production of organic compounds from the roots is not regular.

In this paper we show how to monitoring the health of the plants, by measuring the electrogenic potential of the colony of bacteria. The role of the PMFC is twofold:

(1) it is the *biosensor* used to verify the *health* of the plant;
(2) it is the *battery* of the electronic system, and it is used to supply a microcontroller, additional sensors and a low-power radio to transmit periodically health status and other information about the plant.

We show how the duty-cycle of the transmission directly depends on the amount of generated power, thus the rate of received data packets gives an immediate feedback on the health of the Plant-MFC system.

The design of the electronic system is driven by the ultra-low power consumption constraint and it is low-cost. The average power consumption is μW, because of very long *sleep* intervals (i.e. hours) allowed by the application, when data sampling and transmission is not necessary and the whole circuit can be switched off. The built prototype is shown in Fig. 3. Among the pool of additional sensors available on-board, a light sensor permits to correlate the production of the energy of the Plant-MFC with the ambient light that enables photosynthesis and the production of organics from the

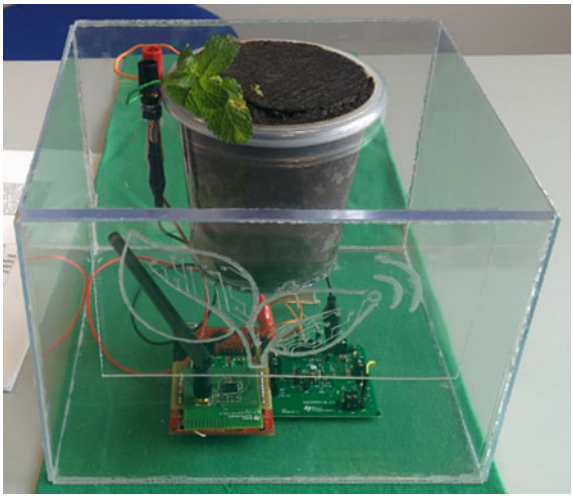

Fig. 3. Prototype of the sensor to transmit wirelessly the status of the plant's health

roots. To save energy for packet transmission, data can be compressed using recent techniques for smart sensors networks [13].

2 Experimental Results

In a controlled environment, we verified that a well-started colony of bacteria can recharge a 10 mF supercapacitor in about 5 min (thanks to an MPPT enabled DC boost converter) allowing duty-cycled monitoring application virtually forever. We tested the system for several weeks, and Fig. 4 shows some hours of our experiments. Notice that the spikes of current consumption correspond to the transmission events, and their rate depends on the status of the accumulator charged by the biosystem Plant-MFC.

In detail, monitored data include µC current consumption, supercapacitor voltage and PMFC voltage. A detail of the current consumption profile during the transmission stage is also provided. The total acquisition time is 3 h 20 min. In the first part of the test, with PMFC voltage above 300 mV, the radio module performs regular transmissions with the imposed timing. Under this voltage value, the fuel cell is no longer able to recover all the required energy and transmissions occur less frequently. Current bursts show that the system dynamically adapts the transmissions to the available energy and therefore to the "health" of the P-MFC.

We characterized the capability of the MFCs to provide current using different loads. The amount of generated current is not constant over time, because it depends on environmental conditions, size of the colony, availability of nutrients and many other factors. For this reason, the operating point of the MFC, which delivers the maximum power (Maximum Power Point MPP), is not constant over the time.

However, starting with a MFC (without a plant), the load where the maximum power transfer is registered, is within a limited range: 800 Ω < Rload < 1000 Ω. In

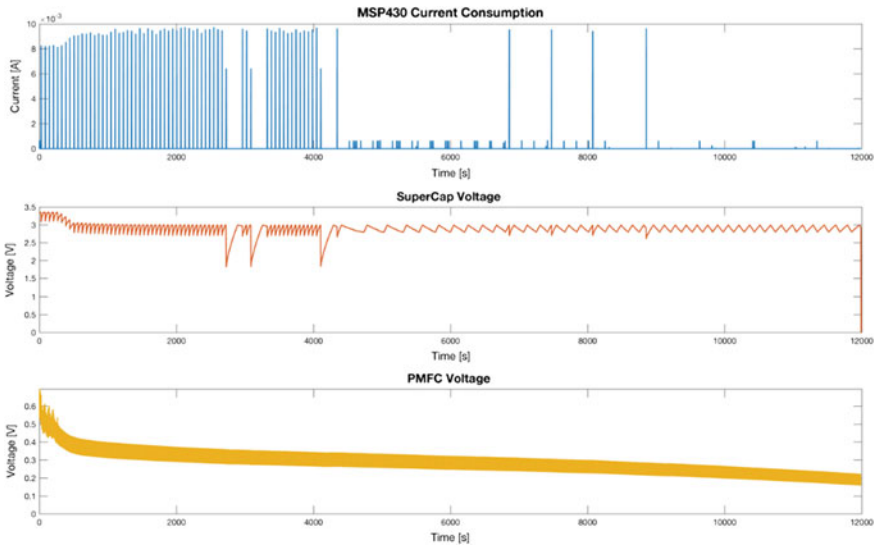

Fig. 4. Sustainability test of the application

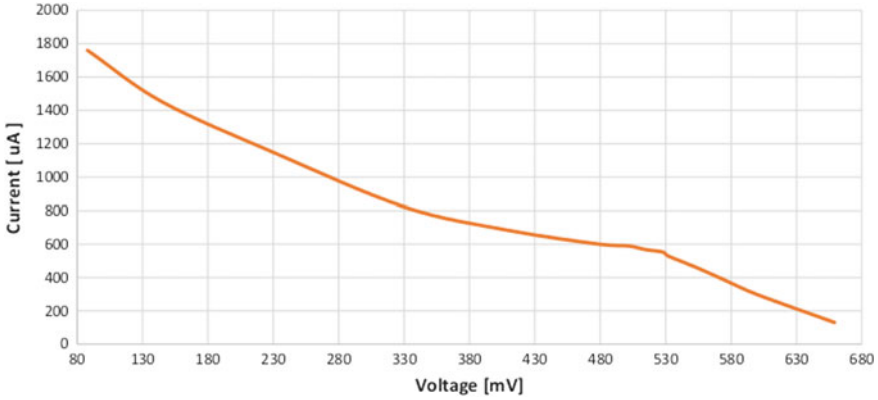

Fig. 5. Current-voltage characteristic of the MFC, obtained different loads (from 1 Ω to 10 kΩ)

such conditions, we measured a maximum output voltage of 502 mV and a maximum current of 590 μA, generated by the cell, as depicted in Fig. 5.

Then we added a plant turning the MFC into a P-MFC and measuring the output power, during the growth of the plant. We executed several tests in different conditions. The maximum power increases during the days of the experiments, while the plant is growing. This demonstrates that the status of plant health can be assessed by measuring the power generated, as can be seen in the characteristic curves reported in Fig. 6. Notice, that the contribution of the plant is remarkable, because there is a relevant increment of the generated power (roughly 2×) thanks to organic nutrients provided.

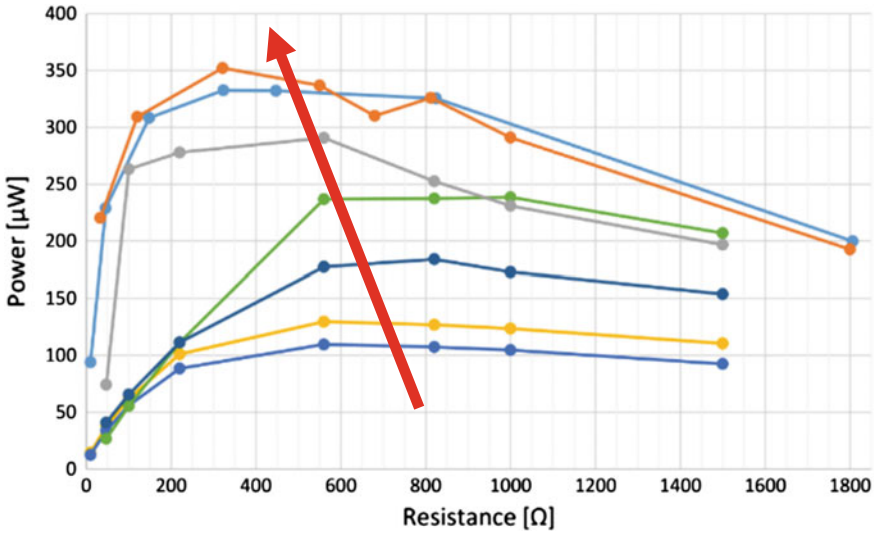

Fig. 6. Output power of the PMFC as a function of the load, while the plant is growing day by day (*red arrow*)

3 Conclusions and Future Works

In this paper we have shown that it is possible to determine the status of the health of a plant using microbial fuel cell. In particular, we presented the design of a complete energy neutral sensor capable to assess environmental parameters and the health of the plant, using the sole energy generated by the bacteria in the soil. Measurements can be done every 5 min and sent wirelessly, keeping the energy balance neutral and thus the smart sensor operating unattended for years. Future work will optimize the energy conversion efficiency and will investigate more complex setup.

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Automotive

Developing ICT Solutions for Dynamic Charging of Electric Vehicles

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Abstract. Dynamic charging technology has the potential to solve the range anxiety problem of electric vehicles. The FABRIC project is assessing the feasibility of using the dynamic charging technology on a large scale. The project developed the ICT platform to support dynamic charging. This paper presents some ICT systems developed within FABRIC.

Keywords: Dynamic charging · Wireless charging · ICT · FABRIC

1 Introduction

The sales of fully electric vehicles (FEV) are still limited compared to the conventional internal combustion engine (ICE) vehicle. Many customers are discouraged from buying electric cars instead of ICE cars because of their limitations, while for commercial use, current FEVs are only suitable for certain types of operation. In fact, the electric vehicle (EV) is expensive due to the high cost of the battery and needs several hours for a full recharge. Even with a full charged battery, an affordable electric vehicle cannot cover more than 160 km on average and this limitation can lead to "range anxiety"—the fear of being stranded due to battery depletion and the absence of an available charging facility [1]. Dynamic wireless charging technology [2] is expected to increase the FEV range and hence reduce the uncertainty and anxiety associated with electric vehicle use.

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The FABRIC project [3] assesses the feasibility of dynamic charging technology for large scale use by FEVs and ICT [4, 5] is expected to play a major role to achieve this target [6]. The project proposes an ICT electric mobility platform for supporting dynamic charging operations. The platform connects the charging infrastructure, the FEV user, the road operator and the grid operator. The present paper aims to present some ICT systems developed in FABRIC. The user needs for the ICT systems have been defined in [7] and a review of the existing ICT systems for inductive charging has been realized in [8]. The specifications of the ICT systems have been defined in [9].

The reminder of this paper is organized as follows: the Sect. 2 will present the interaction between the ICT systems of FABRIC. These systems are the charging infrastructure (CI), the FABRIC backend, the load balancing system (LBS) and the lane keeping system (LKS). The Sect. 3 will present some details about the ICT systems. The Sect. 4 will present a conclusion.

2 Overall System Architecture

The FABRIC systems exchange charging related information to achieve the dynamic charging operations. Figure 1 explains the data exchange. In case the vehicle is in need of an electric charge, it contacts the FABRIC Backend using a wireless connection to retrieve the location of a dynamic charging station. When the vehicle is near a dynamic charging station, it requests a charge according to its charging device parameters and the charging station delivers the electric charge and the corresponding energy bill that will be stored in the vehicle system. The EV needs to be aligned with the charging device located in the centre of the lane in order to increase the energy transfer efficiency and the lane keeping system is used to assist the EV driver in this task. The number of the EVs using the dynamic charging station varies per day and the load balancing system keeps the balance between the EVs charging demand and the electric grid load. A thorough analysis of each module follows in the subsequent paragraphs.

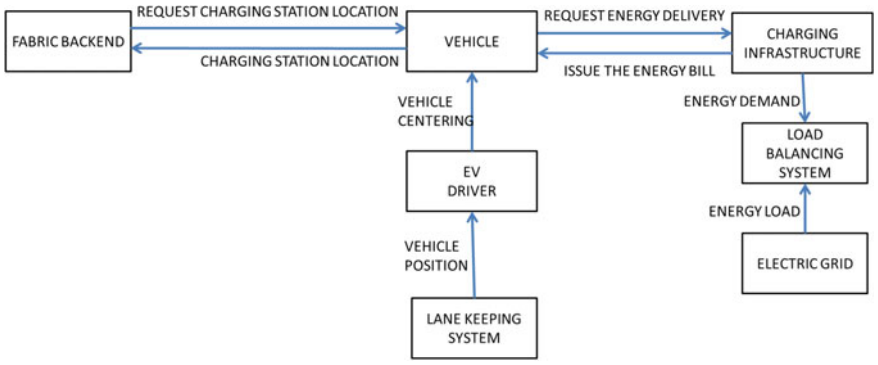

Fig. 1. High-level block diagram of the dynamic charging system

3 Description of the Systems

This section describes in detail the charging infrastructure, the backend, the load balancing system and the lane keeping system.

3.1 Charging Infrastructure

The charging infrastructure delivers the electric energy to the EV. It is composed of the Charging Station Control Unit (CSCU) and the Electric Vehicle Supply Equipment (EVSE) operator. The CSCU manages and controls the power electronics of the charging facility and communicates with the EVSE-Operator in order to provide the authentication, authorization accounting (AAA) services and monitoring information. The EVSE Operator subsystem is the backend of the charging infrastructure. It communicates with a set of CSCUs, for gathering monitoring and status information, and triggering some actions (such as booking of the charging station). It implements the server-side of the AAA operations for the charging process. On the other hand it communicates with the FABRIC backend for reporting the status of the charging facilities (monitoring) and providing accounting information. The load balancing controller-charging station control unit (LBC-CSCU) agent, the load balancing controller-electric vehicle supply equipment operator (LBC-EVSEO) agent and the load balancing controller web service are the components of the load balancing system that keeps the equilibrium between the EVs charging demand and the electric grid load.

The architecture of the charging infrastructure is presented in Fig. 2.

The tests demonstrated that the AAA module can retrieve the vehicle ID and can determine the actually charged energy in kWh and retain it at the EVSE operator. The monitoring module tests demonstrated that the CSCU can send charging procedure control (CPC) status to the EVSE operator including the power at which the EV is charging, the internal status of the CPC state, and eventually the electrical failures in case they occur. The CPC module tests demonstrated the CSCU ability to send and receive CAN messages to and from the power electronics and to acquire the plate number from the automatic number plate recognition (ANPR) camera. The web

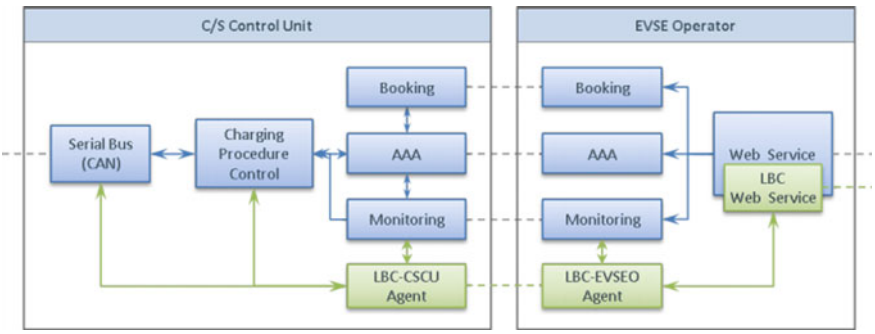

Fig. 2. Charging infrastructure architecture

services testing proved the capacity of the CSCU to push the status change of any charge point to the backend.

3.2 Backend

The Backend is envisioned as the gateway between FABRIC and the EV and it is mostly based on the backend component defined in the eCo-FEV project [9]. It will handle all communications with the EV and the end-users. In that way, it reduces the load for the core FABRIC electric mobility platform. It includes a set of user applications with a set of supporting functionalities to realize the FABRIC use cases and communicates with infrastructure operators. The components of the Backend are represented in Fig. 3.

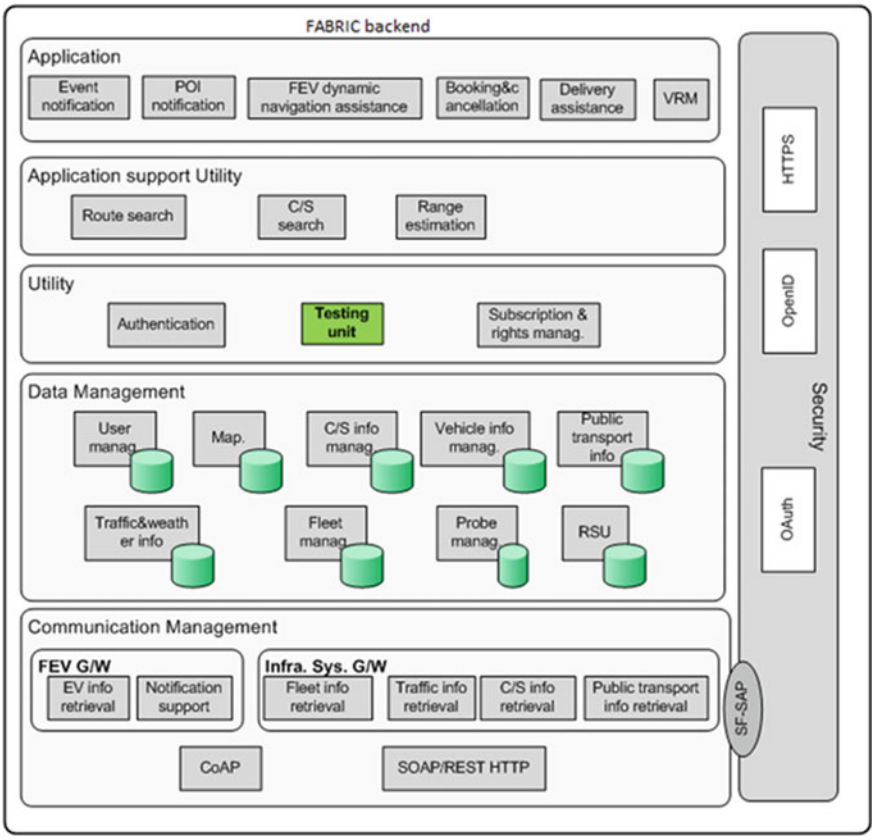

Fig. 3. Backend architecture. The communication management module interfaces with other sub systems and external infrastructure systems for data collection and data distribution. It also ensures the information exchange with other Backend modules, e.g. database modules at data management layer. The Data Management module includes the components and databases to store and manage the various data that are necessary for the applications and their components. Finally, the Utilities module includes utilities and components that support the operation of the high level applications

The communication management modules and interfaces tests demonstrated the backend ability to retrieve the EV information, inform the user regarding the EV position and targeted destination, and retrieve the status of the charging infrastructure. The data management module tests demonstrated the ability to manage the user data, the charging infrastructure data and the vehicle information.

3.3 Load Balancing

Load balancing aims to maintain equilibrium between grid supply and demand taking into account many parameters relevant to the EV battery management system (BMS), charging infrastructure operating characteristics, grid stability, power quality and user preferences. It is essential to ensure that net capacity and transformer limits of the grid are not exceeded. Moreover it ensures that highly unpredictable energy sources can be integrated (wind, solar) by shaping the overall demand due to charging operations to match the available supply. The high-level flow chart of the load balancing system is presented in Fig. 4. The solution implements a distributed rate control algorithm; i.e. the Additive Increase Multiplicative Decrease approach. According to this methodology, EVs additively increase their charging rate up to the maximum allowed charging rate. If the infrastructure requires a decrease in the overall charging rate, a congestion

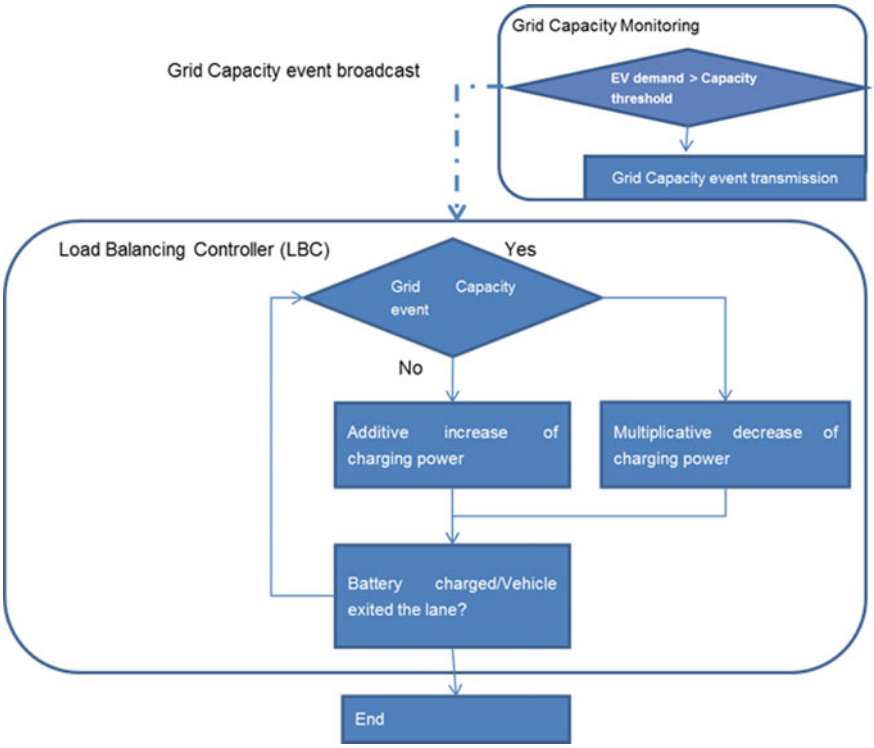

Fig. 4. High-level flowchart of the load balancing module

signal is broadcasted to all EVs, which in turn reduce their charging rate by a multiplicative factor.

The tests demonstrated the grid capacity monitoring module ability to retrieve the current demand and the maximum power to be transmitted to the vehicles. During tests, the load balancing controller infrastructure was able to receive a message indicating that the overall power transfer capacity of the system has been reached. The tests demonstrated that the vehicle can correctly receive the charging power set point from the load balancing controller, check the battery status and accept charging at a given charging point.

3.4 Lane Keeping System

The vehicle charging device needs to be aligned within 20 cm of the road charging device in order to maximize the energy transfer efficiency. The lane keeping system helps the driver to keep within this limit by relying on a camera placed in the vehicle. Two lane keeping systems were developed in FABRIC. One was developed by the University of Genoa and will be tested in Italy. The second one was developed by VEDECOM and will be tested in France. The Italian lane keeping system calculates the lateral distance between vehicle and the lane mark and displays it on a Tablet. The driver uses the information displayed on the tablet to stay in the center of the lane. The high-level schema of the system implemented in the Italian test site is depicted in Fig. 5.

The Italian lane keeping system is based on the following work [10]. The road marks are detected in the inverse perspective view using Hough Transform and then the lateral distance between the camera and the road mark is calculated. The lane keeping system for the Italian test site was able to detect the lane marks in straight and curved roads and in the presence of shadow. It was also able to calculate the vehicle position inside the lane.

The lane keeping system developed by VEDECOM for testing in Satory in France detects the lanes by optical contrast and tracks them with a multi-agent system,

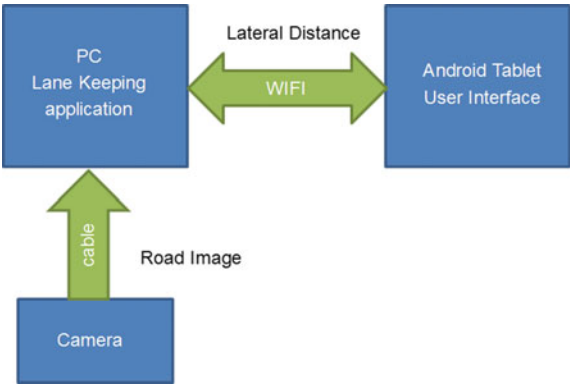

Fig. 5. High-level schema of the lane keeping sub-system

providing lane description as cubic spline [11]. It computes the position of the centre-line of the lanes in the viewing frustum using an original algorithm. By projection and transformation from the camera frame to the vehicle frame, the distance between the vehicle's medium plan and the lanes can therefore be calculated in Y direction (in vehicle reference frame, assuming the vehicle direction of travel is parallel to the lane centrelines). The main advantage of this kind of algorithm is to take into account road curvature. It allows the lane-centre position to be improved by taking into account the lack of curvature of the FABRIC test track at Satory and to allow the testing of this system on another track which contains curves. The lane keeping system for the French test site was able to detect the road lanes in day and night time, with any kind of curvatures and in highway, peri-urban and urban scenario.

4 Conclusions and Future Work

The charging infrastructure, the FABRIC backend, the load balancing system and the lane keeping system have been developed during the FABRIC project to assist the driver in charging the FEV. These systems have been tested in laboratory conditions and demonstrated positive results. Starting from fall/winter 2016, these systems will be tested in two test sites. The first one is in Susa, near Turin in Italy. The second site is Satory, near Versailles in France.

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Maximizing Power Transfer for Dynamic Wireless Charging Electric Vehicles

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Abstract. Dynamic (on the go) wireless electrical charging is a new, challenging frontier for vehicular technologies, as it would allow a dramatic increase in the feasible distance range of electrical vehicles. This paper presents a system under development for optimizing the power transfer for dynamic charging vehicles. The system relies on a coil coupling sensor and a camera. The coupling sensor measures the coupling level between the road and vehicle coils, while the camera detects the distance of the vehicle from the two lines of the lane. A sensor fusion system is needed because, on one hand, the coil sensor is highly accurate but cannot distinguish the direction of the misalignment, while the camera is less precise but can provide information about the position of the lane center, where the centroid of the transmitting coil is expected to be and complete a series of other non-magnetic information needed like the obstacle presence.

Keywords: Wireless power transfer · Electric Vehicles · Alignment detection · ICT · Camera

1 Introduction

Dynamic (while driving) Inductive Power Transfer (IPT) for Electric Vehicles (EV) is a pioneering technology that promises to dramatically increase the driving range, thus reducing the battery size with possible reduction in the vehicles overall cost [1]. Dynamic IPT is essentially based on the magnetic coupling of two resonant coils. One coil is called transmitter and is buried under the road pavement in the center of the lane. The transmitter is connected to a power source and transfers the electric power wirelessly to another coil called receiver placed under the EV. The power collected by the receiver is stored in the EV battery or can power directly the EV engine. The EV needs to align its receiver with the transmitter to increase the power transfer capabilities. Previous work has been done to align the receiver and the transmitter in case of static charging [2]. Also a study on the effects of misalignment in the case of on-road charging has been presented in [3]. A method to guide the vehicle to a high coupling area was developed for low speed vehicles (0.8 m/s) and presented in [4].

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In the dynamic case, the alignment system has to be able to provide information to keep the driver in the center of the lane also at high speed. This can be achieved with state of the art lane keeping systems (LKS) [2]. However, the transmitter may be not placed exactly in the center of the lane, so the LKS may not be sufficient for maximizing the power transfer. This is a specificity of the new alignment challenge given by the IPT requirements. To the best of our knowledge, this issue has been addressed in literature only by Hwang et al. [3], so far. [5] presents an alignment system which is based on two voltage sensor units. In this paper, we propose to use a magnetic coupling sensor that can measure the level of mutual coupling between the transmitter and the receiver. As this mutual coupling depends on the coils' relative position, this information can be used to estimate the vehicle misalignment. Nevertheless, the coupling sensor alone is not able to distinguish the direction of the misalignment, which is necessary to indicate if the vehicle should turn left or right to increase the power transfer. This is the main motivation for developing a lane keeping system based on a camera and a coupling sensor in order to optimize the power transfer.

The reminder of this paper is organized as follows. Section 2 presents the fundamentals of IPT, Sect. 3 the sensor fusion alignment system and Sect. 4 the conclusions.

2 IPT Fundamentals

An IPT system for automotive application is based on the inductive coupling of transmitter and receiver coils. Figure 1 shows the scheme of the system analyzed in this paper. The transmitter is supplied through a power electronics converter providing a high-frequency current I_1 producing a magnetic field that links with the receiver. When a load is connected to the receiver, an induced current I_2 can flow giving rise to the power transfer. The receiver can be connected, by means of a rectification stage, to the battery of the vehicle allowing its charge.

The absence of physical contacts allows the possibility to use this technology during the movement by installing a series of transmitters that can be sub sequentially energized in correspondence of the vehicle passage. This application is commonly known as dynamic IPT.

In order to improve the power transfer capabilities of the system together with the efficiency of the power transfer, the coil are usually compensated by means of capacitors insertion [6, 7] or more complex compensation networks [8].

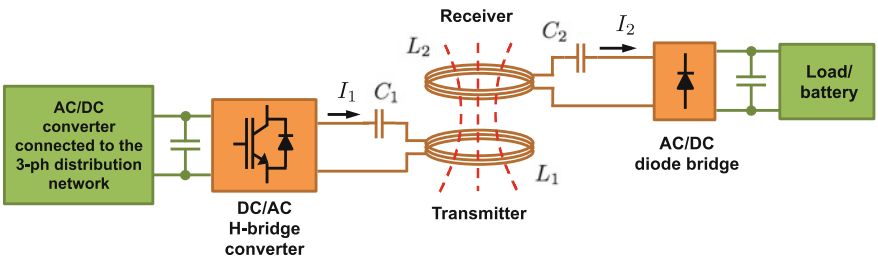

Fig. 1. Block diagram of an IPT system

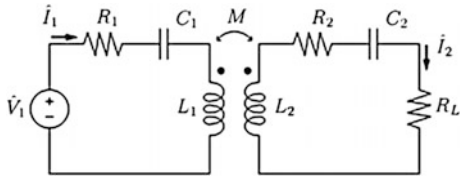

Fig. 2. Equivalent circuit of the IPT system

In the present case, a series-series compensation has been proposed (a capacitor in series with the transmitter coil and one capacitor in series with the receiver coil).

Adopting a first harmonic approximation [9] the system can be represented through the equivalent circuit shown in Fig. 2 where V_1 is the first harmonic of the supplying voltage, L_1 and L_2 are the self-inductances of transmitter and receiver respectively while C_1 and C_2 are their compensation capacitors. Resistors R_1 and R_2 models the equivalent losses of coil and capacitors. M represents the mutual inductance between the two coils. According to the presence of the diode bridge, the resistor R_L is an equivalent representation of the load whose value is given as the ratio between the first harmonic of voltage and the current at the rectifier input [10].

According to the proposed model, it is possible to write an equation for each side as:

$$\widehat{\boldsymbol{V}}_1 = \boldsymbol{R}_1\widehat{\boldsymbol{I}}_1 + \boldsymbol{j}\left(\boldsymbol{\omega L}_1 - \frac{1}{\boldsymbol{\omega C}_1}\right)\widehat{\boldsymbol{I}}_1 - \boldsymbol{j\omega M}\widehat{\boldsymbol{I}}_2 \tag{1}$$

$$\boldsymbol{j\omega M}\,\widehat{\boldsymbol{I}}_1 = \boldsymbol{R}_2\,\widehat{\boldsymbol{I}}_2 + \boldsymbol{j}\left(\boldsymbol{\omega L}_2 - \frac{1}{\boldsymbol{\omega C}_2}\right)\widehat{\boldsymbol{I}}_2 + \boldsymbol{R}_L\widehat{\boldsymbol{I}}_2 \tag{2}$$

Expressing I_2 in terms of I_1 in (2) and substitute it into (1), it is possible to find the ratio between the source voltage and current I_1. This ratio is commonly indicated as total impedance ZT and it is expressed as:

$$\widehat{\boldsymbol{Z}}_{\boldsymbol{T}} = \frac{\widehat{\boldsymbol{V}}_1}{\widehat{\boldsymbol{I}}_1} = \boldsymbol{R}_1 + \boldsymbol{j}\left(\boldsymbol{\omega L}_1 - \frac{1}{\boldsymbol{\omega C}_1}\right) + \frac{\boldsymbol{\omega}^2\boldsymbol{M}^2}{\boldsymbol{R}_2 + \boldsymbol{j}\left(\boldsymbol{\omega L}_2 - \frac{1}{\boldsymbol{\omega C}_2}\right) + \boldsymbol{R}_L} \tag{3}$$

Supplying the system with an imposed resonance pulsation 0 defined as:

$$\omega_0 = \frac{1}{\boldsymbol{L}_1\boldsymbol{C}_1} = \frac{1}{\boldsymbol{L}_2\boldsymbol{C}_2} \tag{4}$$

The inductive and capacitive terms disappear so the total impedance become purely resistive. In that case, relation (3) can be rewritten as

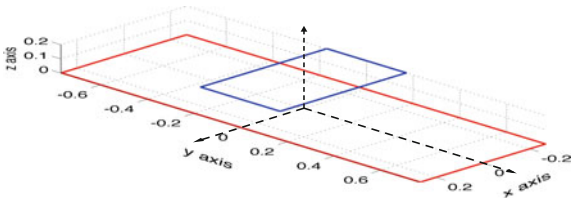

Fig. 3. Example of coils for a dynamic IPT system

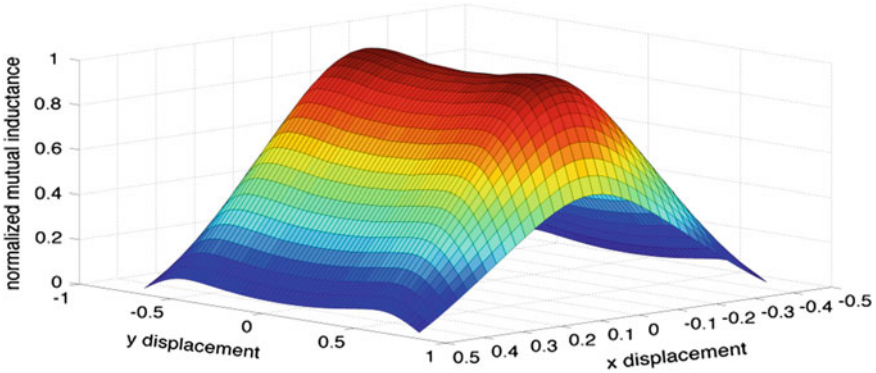

Fig. 4. Map of variation of the mutual inductance versus the receiver coil displacement. Values are normalized with respect to the value in perfect alignment condition (Fig. 3)

$$M = \sqrt{\frac{V_1}{I_1}\left(\frac{R_2 + R_L}{\omega_0^2}\right) - \frac{R_1 R_L}{\omega_0^2}} \tag{5}$$

where the product R_1R_2 is considered negligible with respect to the other terms.

Equation (5) shows that, if the resistive parameters are known and fixed, it is possible to estimate the mutual inductance by measuring the values of voltage and current at the DC/AC output.

These parameters have to be measured with high accuracy for the control of the system so information about them can be easily available for the estimation of the position.

With reference to the coil system depicted in Figs. 3 and 4 shows the variation of the mutual coupling versus the possible misalignment of the coil centers of symmetry.

The next section will describe the lane keeping system based on the coupling sensor and the camera.

3 Sensor Fusion Alignment System

In order to optimize the level of transferred power, the receiver needs to be aligned with the transmitter. A coupling sensor can support this by measuring the mutual coupling between the receiver and the transmitter. The misalignment between the receiver and the transmitter is estimated based on the value of the coupling, as seen in the previous section.

Figures 5 and 6 show two different alignments of the receiver and the transmitter. In Fig. 5, increasing the coupling requires moving the receiver to the right. The opposite is true for the case in Fig. 6. Since the absolute value of the horizontal misalignment is the same in both cases, the coupling sensor cannot distinguish the different situations. These cases show that the coupling sensor alone is not enough to manage the misalignment issue.

To this end, we have thought of integrating the coupling sensor with information from a camera. The optic sensor detects the lateral lines of the lane and estimates the position of the center of the lane. While the inductance sensor is expected to be highly precise (in the order to the centimeter), camera precision is lower, also because the actual center of the transmitting coil may not be placed exactly in the center of the lane. However, optical information is important in order to estimate the direction (to the left or to the right) of the displacement, which is not directly available from the coil sensor.

The IPT maximization sensor fusion system that we are developing is modeled in Fig. 7, where the feedback control system is based on an extended Kalman filter (EKF) [11], characterized by the following equations, under a constant speed hypothesis:

$$x(k+1) = x(k) + u(k+1) + v(k+1) \tag{6}$$

$$y_1(k) = |x(k)| + w_1(k) \tag{7}$$

$$y_2(k) = x(k) + w_2(k) \tag{8}$$

Fig. 5. Alignment A

Fig. 6. Alignment B

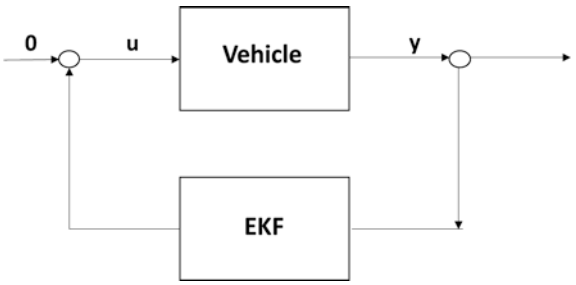

Fig. 7. Block diagram of the sensor fusion alignment system

Where the state x is the actual misalignment between the transmitting and receiving coils, while y_1 and y_2 represent the coupling sensor and the camera misalignment measurement respectively. v represents the coil center displacement between two consecutive road segments, u is the input to the system it can either be right left or straight, while w_1 and w_2 model the inaccuracy in the coupling and camera sensor measurements.

4 Conclusions and Future Work

Dynamic IPT for electric vehicle needs an accurate alignment between the road and vehicle coils in order to maximize the power transfer. In order to support this, we have proposed an alignment system fusing information from a coil coupling sensor and a camera. The ongoing work includes simulating the system in straight and curved roads, considering different vehicle speeds.

Further steps include the upgrade of the control system also keeping into account the discretization of the coils in the road, thus decreasing the quantity of information from the coupling sensor. Moreover, the image processing outcomes could be used for introducing a long term trajectory planning factor, in order to minimize the vehicle's steering activities. In fact, coil provides a valuable estimation instantaneously, while the camera can understand the winding of a road at a distance. Further inputs may be considered, such as vehicular signals and geographic maps. Overall, all this information may lead to the design of a different type of controller.

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A Serious Game Architecture for Green Mobility

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Abstract. Good driving behavior is a significant factor for road safety and green mobility. A countermeasure to overcome the coarse driving behavior and a methodology to captivate optimal driving traits are discussed in this work. For which, the serious games concept was exploited to improvise the driver performance by deploying diversified game logics (scores, incentives and live game for performance evolution) on a smartphone-based user interface. The application was tested in ASTA ZERO (Active Safety Test Area) in Sweden. The tests comprised of variations (good and bad driving behavior) in driving pattern for analyzing the impact of the application on the driver performance.

Keywords: Serious games · Service-oriented architecture · Collaborative green mobility · Mobile computing · Infotainment systems

1 Introduction

The advancement in automotive industry comprises of numerous embedded applications (in-vehicle devices) to facilitate the driving experience as pleasant and safe for the users. The abilities of these in-vehicle devices are limitless and one major factor that has to be addressed over here is, what are the implications of these devices on the users (drivers)?. Because, it's the ability and tendency of the driver that determines the road safety and environmental aspects to a greater extent and also, the inadequate driver performance incurs many fatalities and chaos amongst the road users [1]. So, this factor gives an emergence and a need for the in-vehicle systems (equipped with the user-friendly framework) that will foster the green and safe driving abilities to disarm the on-road hazards. As it's important for an in-car HMI (Human Machine Interface) to provide the drivers with comprehensive information to aid in safe mobility [2, 3]. The training process will induce the knowledge and awareness to driver about the driving circumstances and for this motive, we are using the serious game concept and smartphone utilities. Serious games are a purpose based tool rather than an aspect of entertainment [4, 5] and they are widely used in various sectors such as education, military, healthcare and business [6] for captivating users to comprehend an information. Compared to traditional games that focus only on the engagement of the users, serious games does have a much higher responsibility, as it has to leverage and instill

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the concepts as well [7, 8]. An intense care and responsibility are needed in crafting a serious game framework and this leads to a prominent aspect of using instructional design (the use of technology and multimedia tools to enrich the informative content). Projecting a serious game concept through an instructional design (representation on HMI) promotes the higher degree of visual feedback for the user and this visual feedback takes a substantial effect on driving conditions [9]. Thus, to inculcate safe driving behavior and establish a collaborative gaming structure, we developed a smartphone-based serious gaming architecture with diversified game logics to enhance the driver performance. The reference architecture is a Service-Oriented architecture [10]. The game logics act as an informative box that supplies the feedback to the users (drivers) in various ways such as scores, virtual coins (incentives that can be used on real-world entities) and live game for displaying the performance evolution. As the serious game provides a behavioral influence on driving, the constant impact of it will act as an emergence of optimal driving behavior amongst the road users and benefit the environmental safety as well.

2 TEAM Applications

Our research activity is part of TEAM (Tomorrow's Elastic Adaptive Mobility) a European Union FP7 project and the project aims at delivering solutions for transportation elasticity and safety [11]. The TEAM applications focus on various aspects of smart and collaborative mobility such as navigation, parking, games for green mobility and etc.

- EFP, Eco Friendly Parking is an in-vehicle Team app aimed at helping drivers in finding parking slots, also thanks to collaboration among them.
- CONAV, Collaborative Navigation is a TEAM app (implemented both on vehicle and on a smartphone) that provides navigation according to criteria suitable for large groups of people, not a single person.
- CPTO, Collaborative Public Transport Optimization is a TEAM app that considers preferences and real-time information from various users in order to adapt the public transport bus service accordingly.
- CCA, Co-modal coaching support from virtual avatar users is a co-modal transportation support app with post trip cost/benefit analysis functionalities, made through a comparison of the behaviors of the real user and the "virtual" avatar user.
- SG-CB, The Serious Games and Community Building application includes competitions, rankings, comparisons, virtual coins and a basic networking environment to support better driving.

3 Serious Game System Architecture

The framework of serious games and community building (SG-CB) application comprises of various modules and these modules interact seamlessly to estimate and affect the driver performance (see Fig. 1). The TEAM applications are the virtual sensors and

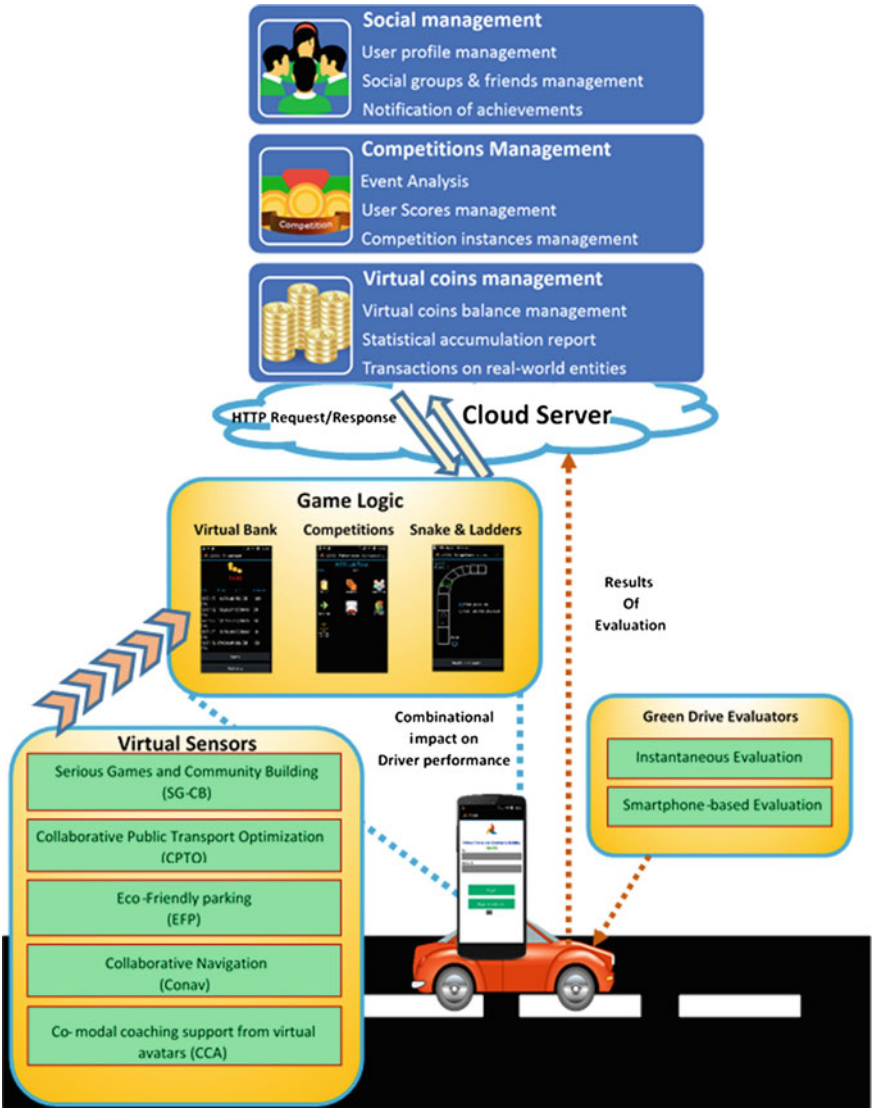

Fig. 1. Serious gaming framework

they feed inputs to respective strategy in the game logic. The SG-CB application intends to support a community of road users, who share results and various information [12]. The SG-CB contributes for all the three game logics (virtual bank, competitions and snake and ladders). The SG-CB's assessment of driver behavior is performed by two green drive evaluators:

- *Instantaneous evaluator*—an in-car evaluator, which assess the vehicular signals (such as acceleration, speed, engine RPM and brake) and provide scores based on it.

The vehicle signals such acceleration, brake, engine RPM and speed are extracted through CAN bus and sent to the driver performance evaluators housed in car for processing. Based on the evaluation criterion the users are provided scores for the performance.

- *Smartphone-based evaluator*—utilizes the in-built functionalities of a smartphone such as GPS (Global Positioning System), accelerometer and gyroscope and provides the result by associating them with the performance of the driver. The user just needs to mount the smartphone on the dashboard of the car and then the evaluator extracts the signals from smartphone sensors (as discussed before) and evaluates the performance of the user. Periodically, the scores are transmitted to the cloud server.

Both these evaluators run simultaneously in-car and evaluate the driver performance on two distinct metrics and the evaluation results (the scores ranging from 0 to 100) are then transmitted to the cloud server for further processing. Each user has a separate account in which they can manage their gaming activities and the entire workflow is displayed on a smartphone with detailed representation of scores, virtual bank and snake and ladders.

3.1 Virtual Coins

The user gains *virtual coins* (rewards granted based on the individual performance) for optimal driving. The virtual coins are accumulated in the virtual bank and they can be used on real-world entities such as purchasing bus tickets, reservation of parking space and etc. Each application grants virtual coins for various aspects, for example, Eco-Friendly Parking (EFP) provides virtual coins if the user manages the parking slot and time in a loyal manner by parking the vehicle in requested time limit (Fig. 2).

3.2 Competitions

In competitions approach, the user can take part in a time framed *competition* (a competition might last from 10 to 15 min depending on the locality) by subscribing for the open competitions (the competitions are opened on timely basis) and exhibit better driving behavior to surpass the peers in competition. The term competition in this occasion can be defined as a geographical location associated with any road network in a city. In a competition, users are evaluated for their performance by the two green drive evaluators on the basis of vehicle signals (acceleration, brake, engine RPM, and speed) and the smartphone signals (GPS, accelerometer, and gyroscope). While, on the go the users can check the scores of their subscribed competitions and also can look for the fluctuations in scores based on the performance in competition. On completion of a competition, users can check their detailed report of scores, rankings, performances and comparison with peers. The competition strategy, grant scores and generate the rankings based on the comparison of user performance with the performance of peers, so this aspect comprises of impact in evaluation from various users in the competition. Some virtual coins are also granted for scores secured in the competitions. Whilst, analyzing the performance in competition, the users are also assessed on harsh driving events such as harsh braking, high acceleration and high levels of engine RPM. At the end of

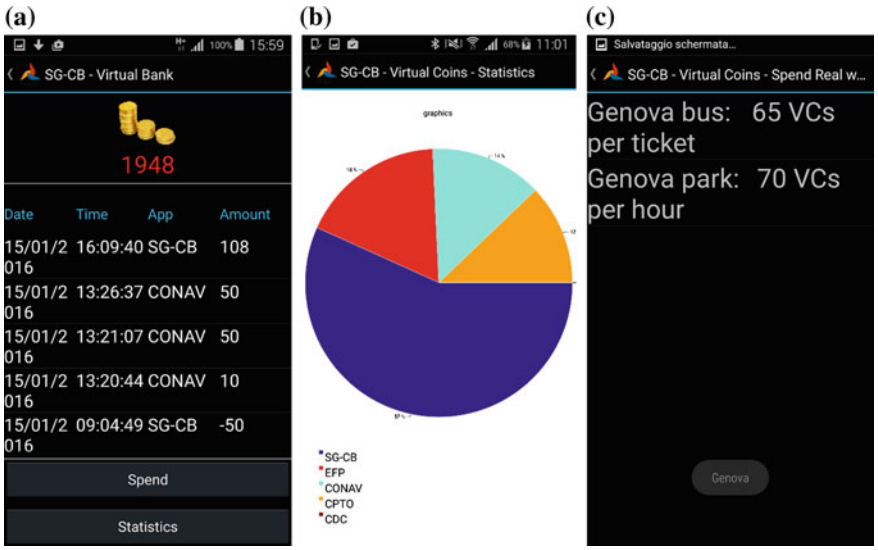

Fig. 2. Virtual bank screen from SG-CB application, **a** virtual bank home with virtual coins balance, **b** graphical representation of virtual coins gained from various TEAM applications, **c** options to spend virtual coins on real-world applications

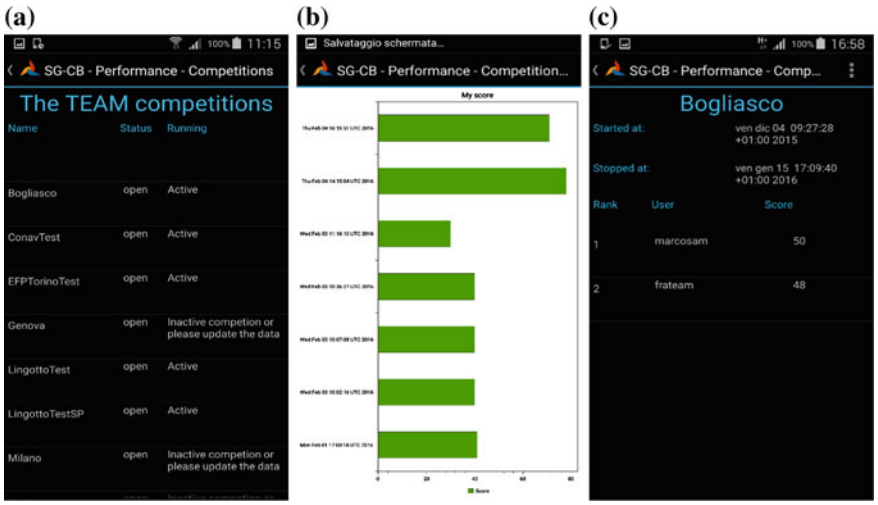

Fig. 3. The Competition menu in SG-CB application, **a** the list of open competitions in which user can participate, **b** graphical representation of user scores in competitions, **c** ranking and performance of users in a competition

competition, the tracked harsh events are displayed on Google maps along with the harshness level (high or average) and this methodology would serve the purpose of training drivers by making aware of the harsh patterns exhibited during the drive (Fig. 3).

3.3 Snake and Ladders

The snake and ladders is a live gaming aspect and this approach is linked to the *virtual coins* (rewards for the performance). The entire snake and ladders game is manipulated with a slate comprising a set of slots (ladder) for the users to progress based on their performance. When the user acquires virtual coins, it's converted to the roll up numbers in dice and rolled virtually and this advances the user position on slots. The user climbs the ladder and advances the levels as a result of their performance. The snake and ladders approach provides a gamified environment for users to visualize the evolution of their performance and also to compete with the peers associated with the competition. The snake and ladders game comprises of two levels and the complexity increases as user progresses and winner of the game secures a championship and additional points (Fig. 4).

As the gaming methodology provides a competitive aspect, the goal of user becomes to gather incentives and excel. On the pursuit of it, there will be an understanding and need for developing the driver performance. The major impact of these game logics on driver performance would be an emphasis on two attributes, which are the rewards and downfall. The rewards will act as a factor of motivation to improvise the driving behavior and to maintain the optimal performance to earn incentives. Whereas, the downfall in scores would provide an extensive analysis of performance, which enables the user to understand and react towards eradicating the bad driving behavior. The cloud server organizes the entire workflow of competitions, scores,

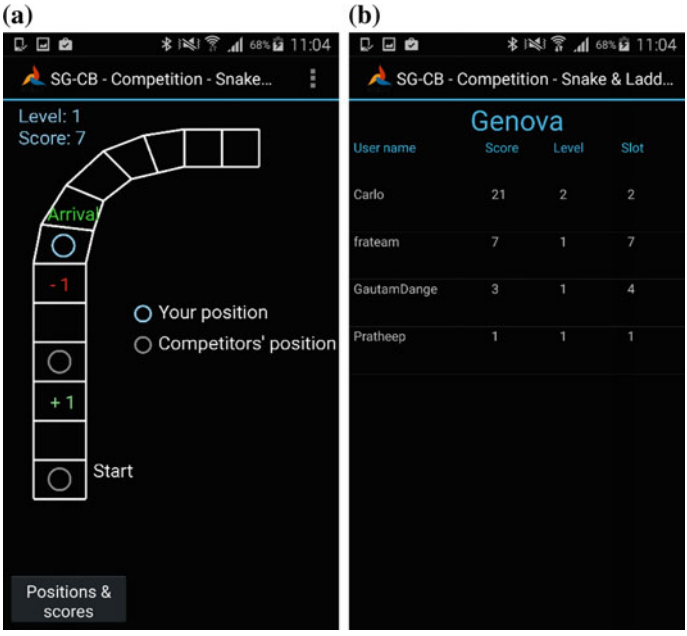

Fig. 4. The snake and ladders gaming screen, **a** the game interface representing the position of user and competitors, **b** position and scores of users associated with the game

virtual bank, user profiling, authentication and social networking (see Fig. 1). The performance details can be accessed anytime from a smartphone using the credentials supplied by the providers (In our case, the user has to register in Telecom Italia's website to secure the credentials). Overall, it's a central hub that manages all the utilities required to establish a serious gaming framework on the go.

4 Field Test Scenario and Results

We tested the entire control flow of our system, by deploying the application in ASTA ZERO (Active Safety Test Area) test track in Gothenburg, Sweden on 10 March 2016. For the test, we used BMW sedan and a Samsung Galaxy s5 smartphone (with SG-CB application installed on it) and the smartphone was mounted on the dashboard. The test run comprised of two laps on the test track, out of which the first drive (Lap 1) comprised of bad driving behavior with frequent harsh driving events and the second lap comprised of optimal driving performance with a minimal amount of harsh patterns. Each lap lasted approximately for 10 min around the same locality. The main consideration behind these two types of driving style is to compare and estimate the quality of driving and test the functionality of the game logics implemented in our system. We extracted the vehicle signals and the evaluation results from our green drive evaluators (the Instantaneous and smartphone-based evaluations).

The results of these two laps are analyzed independently in this section and at first place let's see the outcome of bad driving behavior by comparing the vehicle signals and the event analysis data acquired from two evaluators (Fig. 5).

The vehicle signals (acceleration, speed, engine RPM, and brake) look quite harsh with ample number of peaks denoting the harshness of the drive. Our signal evaluation metrics focused on green drive and for which, we tracked the rapid high values of these vehicle signals, as they can occur during the rash driving behavior. For example, we can consider the engine RPM and brake signals from Fig. 5a, where the peak values of signal hits 6500 and 2300 respectively. We also evaluated for the course of events that driver exhibited during the trip (events such as harsh braking, high acceleration, and RPM levels) and signaled the captured harsh events along with their geo-references to our cloud server and later these events were retrieved and displayed on Google maps in Smartphone.

The event analysis (Fig. 6) represents a detailed report comprising of:

- *Diary*—the list wise representation of all the events based on timestamp and level of intensity (red for high and yellow for average).
- *Summary*—comprises of overall grade for the impact of individual signal on the scale of green (good), yellow (average) and red (bad).
- *Map*—the representation of all the events on Google maps based on the geo-reference acquired during the event.

The harsh events of the brake, engine RPM and acceleration are projected on the map and each evaluator holds a different grading pattern such as, the instantaneous

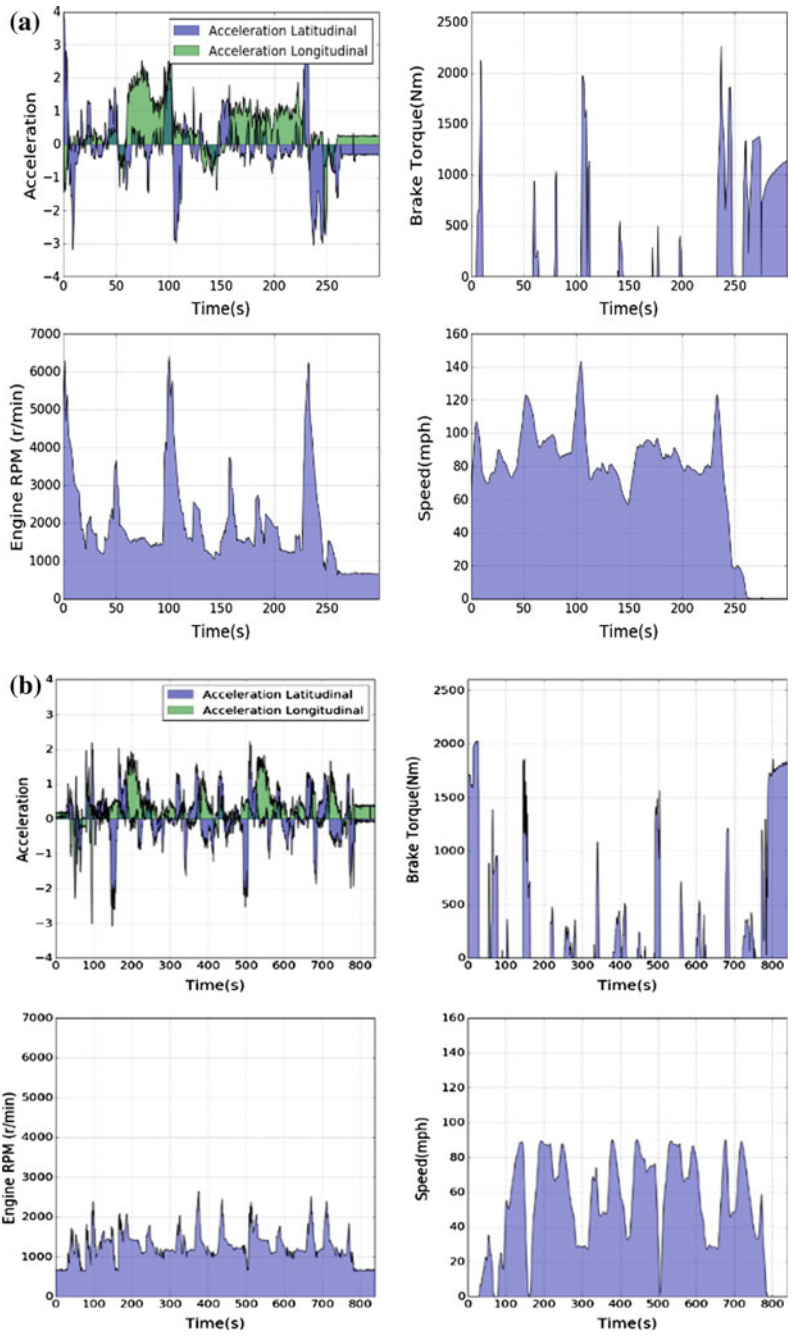

Fig. 5. Vehicle signals (acceleration, brake, engine RPM and speed) extracted during the test: **a** Harsh driving behavior. **b** Optimal driving behavior

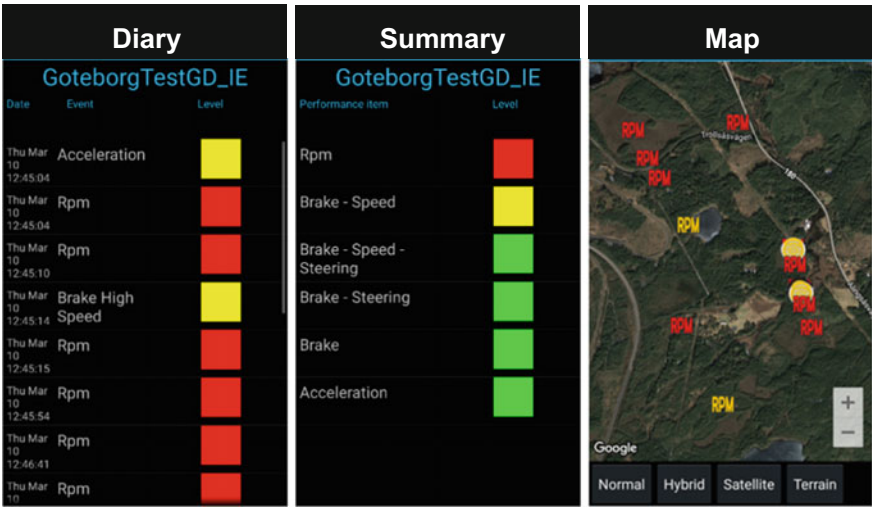

Fig. 6. Event analysis results of instantaneous evaluation for coarse driving behavior

evaluation processes every single vehicle signal acquired from CAN bus (Controller Area Network) and looks for high values and classifies them. The smartphone-based evaluation exploits the GPS (Global Positioning System), accelerometer and gyroscope of the smartphone to determine the harshness in driving pattern (by evaluating the acceleration and brake signals). These two evaluation methods form a solid base for assessing the driver behavior and providing the user with a detailed analysis of harsh events. We can notice ample number of events on the map from the evaluators (see Fig. 6). Let's analyze the second lap of the test run comprising of the optimal driver behavior. As we can see from the signals graph there are not many occurrences of peak values (see Fig. 5b), for example, the engine RPM signal of harsh driving behavior had a peak value of 6500 (see Fig. 5a) and from the optimal driving session, the values of engine RPM haven't exceeded 3000 (see Fig. 5b). As there wasn't much scope of harshness in driving pattern, the driver had secured less number of events during this test run in lap 2 (see Fig. 7) compared to lap 1 (which comprised of bad driving behavior). The event analysis acquired from both the evaluators show the optimal performance of the driver on aspects such as gradually managing the vehicle's motion, less exhibition of coarse driving behavior and overall maintaining a nominal driving pattern.

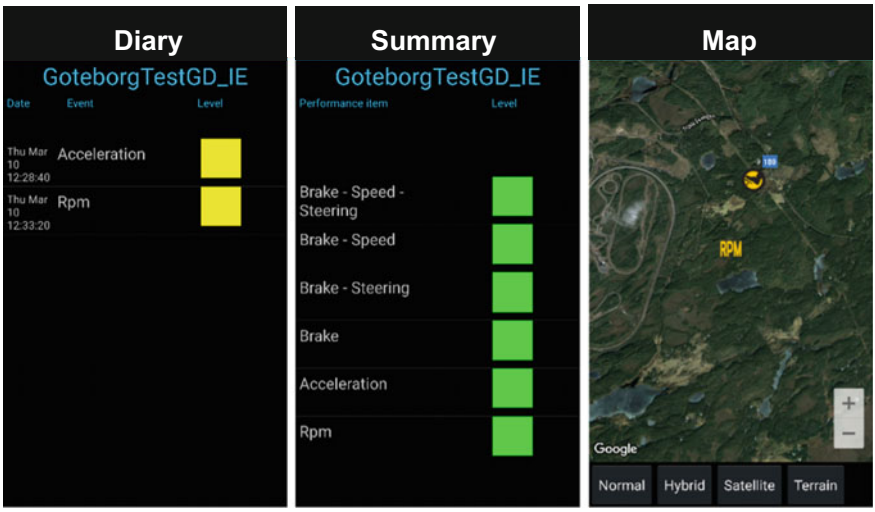

Fig. 7. Event analysis results of instantaneous evaluation for optimal driver performance

5 Conclusion and Outlook

The results from the test drive comprised of good and bad driver behaviors, emphasize on the fact that the gaming aspect gives a bigger space for the users to understand the driving context and enable them to develop their driving standards, especially when the performance is low. We consider the major importance of our tool is the serious gaming framework, which played a pivotal role in bringing out the qualities of the driver, by creating an awareness of one's own driving skills with a detailed report of the drive. From the extracted results of test run, we noted certain factors of our system such as: In real-world scenarios, the gaming methodology would induce a competitive viewpoint among the road users and encourages the drivers to adapt optimal driving traits. The HMI comprised of the detailed representation of the game logics will impact the driver behavior to a greater extent, as it provides a broader analysis of performance aspects like representation of scores, acquired virtual coins, and display of harsh driving events on Google Maps with a detailed summary. Thus, the potential of serious games can be used to captivate the road users for exhibiting better driving qualities and the pervasiveness of smartphones can reinforce the task of conveying the information in an efficient way. These factors contribute in maintaining the safe environment and would pave the way for prominent community building of the road users.

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Design and Implementation of an Electronic Control Unit for a CFR Bi-Fuel Spark Ignition Engine

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Abstract. In this work an Electronic Control Unit for the management of a CFR engine will be described. The engine, which is used both for fuel octane rating (both in terms of RON and MON) and for research purpose, is equipped with a double injection system, with the aim to independently operate both with liquid and gaseous fuels. The developed ECU, hence, is able to control the injections of both kind of fuel, together with the spark ignition. Furthermore the system is also able to measure fuel's consumption, instantaneous engine speed of rotation and air-fuel ratio, showing all the running parameters both on a local LCD display and on a PC based graphical user interface.

Keywords: Engine control unit · Spark ignition · STM-Nucleo board · Embedded programming

Symbols and Acronyms

A/F	Air/fuel ratio
BDC	Bottom dead centre
BTDC	Before top dead centre
CAD	Crank angle degrees
ECU	Electronic control unit
IMEP	Indicated mean effective pressure
CFR	Cooperative fuel research
COV	Coefficient of variation (ratio between standard deviation and mean value)
MON	Motor octane number
RON	Research octane number
SA	Spark advance
TDC	Top dead centre
λ	Relative Air/Fuel ratio = actual A/F divided by stoichiometric A/F

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1 Introduction

The CFR (Cooperative Fuel Research) engine is a four-stroke two valve stationary single-cylinder spark-ignition engine currently prescribed by the ASTM standard D2700 [1] for fuel octane rating [2, 3]; it features a particular head arrangement that allows to accurately vary the volumetric compression ratio from 4.5 to 16: this characteristic allow to carry out a wide variety of experimental test, thus making the CFR a robust and versatile research engine [4–6]. The unit employed in this work, moreover, has been further equipped with an electronic ignition control module and a double injection system with the aim to perform the independent injection of both liquid and gaseous fuels, thus allowing to test almost liquid or gaseous fuel, as well as their mixtures [7], which is nowadays a fundamental part of internal combustion engine research and development for pollutant reduction and sustainable mobility purpose [8]. This setting allows the CFR engine to precisely determine the octane number of fuels mixture, such as natural gas-gasoline or propane-gasoline [9]. The main characteristics of the CFR engine used in this work (model F4) are detailed in the mentioned ASTM standard D2700 [1].

1.1 Engine Control Unit Specifications

In order to exploit the full potential of the CFR engine, a control unit is necessary for the precise control of both the spark generation inside the combustion chamber and the fuels injection in the intake duct, according to the user-defined settings and parameters.

The *input signals* for the desired ECU are hence:

- Two digital pulse trains generated by an optical encoder, mounted on the engine crankshaft, necessary for engine speed measurement (one pulse per revolution) and for crank position determination (360 pulses per revolution);
- One digital signal coming from the CFR native ignition system, used as phase reference signal;
- Some analog signals, such as the Coriolis type fuel mass flow meters and the Venturi air flow meter, used for fuel consumption and Air/Fuel ratio measurement.

In this work, the gasoline mass flow has been easily obtained on the basis of the fuel injection time and of the injector flow map previously determined by the gravimetric method, using a high precision laboratory grade scale. The designed system can enable or disable the fuel injection control in *closed loop* both for gasoline or gaseous fuel. The control in *closed loop for gasoline injection* is carried out using as set-point value the overall Air/Fuel ratio (A/F), while the *closed-loop for gas injection* is performed using as set-point value either the A/F or the gas mass fraction when a fuels mixture is adopted. Starting from these input parameter, the ECU is capable to output the following signals:

- The command pulse for ignition coil (engine ignition). In particular the pulse width was fixed (8 ms) and pre-calibrated, while a programmable starting point with respect to the engine phase signal was implemented in order to precisely set the spark advance with respect to engine Top Dead Centre (TDC);

- The command pulse for the gasoline injection, whose duration can be set by the user (in *open loop* mode) or heuristically calculated when the *closed loop* control on the injection is enabled;
- The command for gas injection, in *open* or *closed loop*.

Some digital outputs are taken into consideration and sent to a host PC to be displayed at user convenience: rotation speed, air mass flow, fuels mass flow, spark ignition advance and measured A/F. Communication between ECU and the remote PC is implemented with a Bluetooth module and the whole unit is battery powered.

2 ECU Hardware Features

The adopted solution was designed around an STM32-NUCLEO development board (F401RE) [10]. It is based on STM32F4 microcontroller (ARM CortexM4 32bit 84 MHz, Flash 512 Mb, SDRAM 96 Kb), where the ECU management firmware was running. A custom designed expansion board was designed to host the *level shifter* CD4504 [11] necessary to move the logical levels of the optical encoder signals from 5 V TTL to 3.3 V CMOS; and some diodes (1N4148), for protection against spikes for the three digital inputs to the ECU. A keypad controller ADP5585 [12] was also helpful for fast menu management, some voltage dividers for analog conditioning and the drivers IRS4427 [13] for the IGBT, driving the ignition coil. Furthermore another board has been designed and realized in order to properly implement a MAX1758 [14] based battery charger controller.

Figure 1 shows the block diagram of custom designed expansion board, while in Fig. 2 the generic block diagram of the ECU firmware is represented.

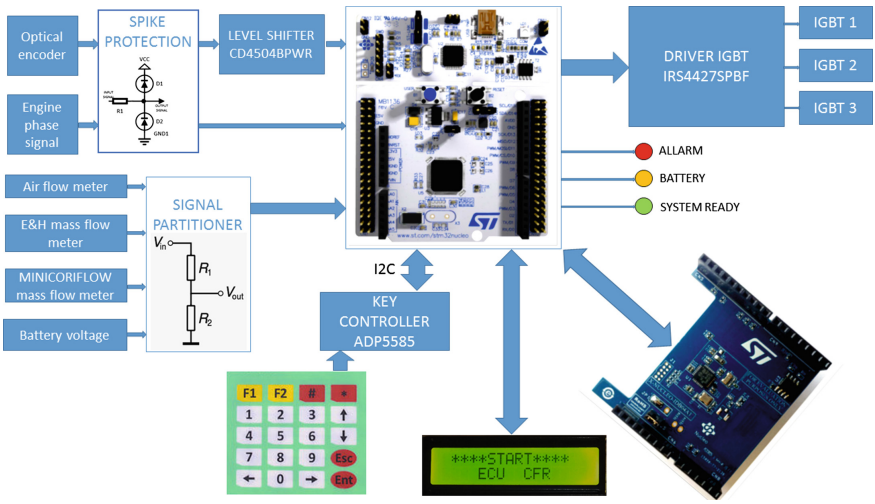

Fig. 1. Block diagram of the custom designed expansion board

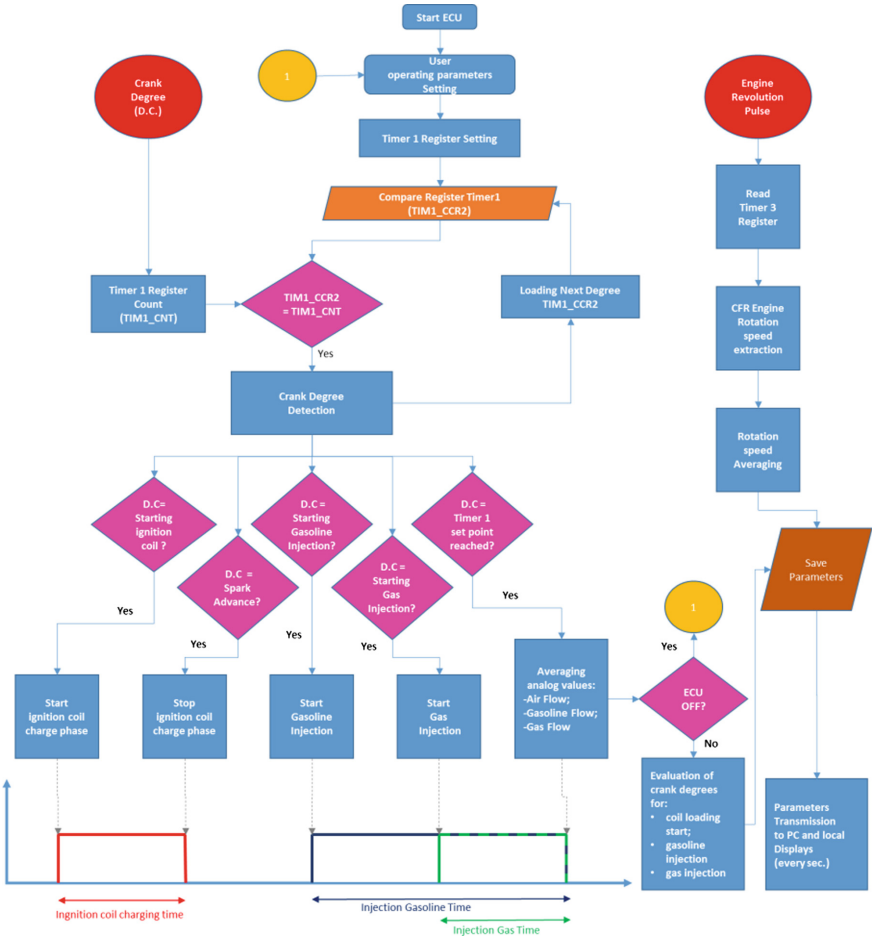

Fig. 2. Block diagram of the ECU Firmware

2.1 ECU User Interface

The user can set and display the ECU and engine operating parameters via a PC based software (running on Windows 10 OS and coded with Visual Studio 2015 IDE) connected via Bluetooth 4.0 provided through an X-NUCLEO [15] expansion board, or via a local keypad and a 16 × 2 local display (Fig. 3).

2.2 Engine Management

The engine management consists in the generation of the injection signals for both fuels and the ignition signal, all adequately phased with respect to the piston position and movement. As mentioned before, the ignition pulse has a duration of 8 ms, previously calibrated as the correct dwell time (primary coil charging time) [16]. The phase of this

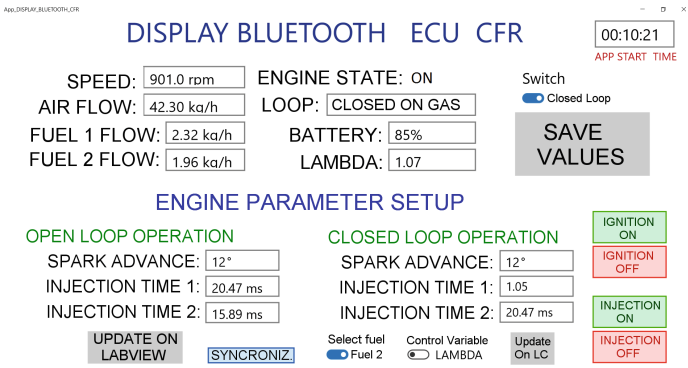

Fig. 3. PC GUI in the *upper part* the output parameters and saved values are shown, while in the *lower part* the setting parameters are reported

ignition pulse is instead determined on the basis of user input, thus accomplishing the desired Spark Advance (SA), expressed as Crank Angle Degrees (CAD) Before Top Dead Centre (BTDC).

The duration of each injection pulses is attained either in *Open Loop* or in *Closed Loop*, thanks to the measured fuels and air mass flows. The phase of both injection pulses, instead, has been previously determined and fixed with respect to the trigger pulse, aiming to ensure that the conclusion of each fuel injection happens to be not later than 90 crank angle degrees before the start of intake stroke [17].

Firmware is organized with some actions routinely done as main assignment while the most delicate engine management functions are arranged in a prioritized interrupts fashion in order to reach the required low latency performances. In particular four interrupt routines are used, with decreasing priority and implemented by using internal MCU timers.

ROUTINE 1: it has the highest priority, generates the injection and the ignition signals and computes the necessary moving averages parameters values starting from the measured analog inputs. It is started as a result of an interrupt request which provides to count the crank angle degrees.

At $start_{inj1}$ and $start_{inj2}$ crank positions, gasoline and gaseous fuel injector are respectively started, and the timer counts for the two injection durations *Tinj*1 and *Tinj*2.

The primary coil charging time (set to 8 ms in this work) can be varied by acting on the *start_bob* and *stop_bob* values (in crank degrees) via local od PC interface as long as some suitable limits are respected. The computation of moving average values of each necessary parameter runs once every engine cycle. The number of cycles to employ for each average can be set by the user from 1 to 500.

ROUTINE 2: it is started by the single pulse per revolution of the optical encoder and measures the time interval between two consecutive pulses in order to determine the engine speed of rotation.

ROUTINE 3: it is invoked by the transition from the high to low logic level of the CFR original ignition signal, and its task is to generate the phase reference signal used for injection and ignition control.

ROUTINE 4: it is called up for the acquisition of analog input signals, with a frequency that can be set by the user from 1 to 5 kHz. In the acquisition, the ADC has been set up in DMA mode (Direct Memory Access) with maximum resolution (12 bit) and with an averaging time interval of 15 engine cycles.

3 Experimental Results

The developed ECU was put to a test-bed with a CFR engine fuelled with commercial LPG, comparing its ignition and injection control performance with the performance obtained by a previously developed system, described in detail in [2, 3], based on the use of a DAQCard 6062E, a multifunction data acquisition board from National Instruments (NI). The DAQCard was connected, through the proper BNC2120 Connector Block, to the engine sensors and actuators, thus performing the injection control of both fuels, the ignition control and the data acquisition. A Kistler piezoelectric pressure sensor, flush mounted in the engine combustion chamber, was also employed for the in-cylinder pressure sampling thus allowing to perform combustion instability analysis. When using the developed ECU for the engine management, the NI DAQCard was employed only for data acquisition purpose.

The performance of the ECU injection control was evaluated in two different tests: the first aimed to verify the capability of the system to maintain the desired Air/Fuel ratio constant during the steady state operation, while the second was dedicated to evaluate the rapidity of the control system to bring the A/F inside the allowed interval (i.e. objective A/F $\pm$ 2%) [16, 17]. For the steady state operation, the comparison parameter is the Standard Deviation of the measured A/F within 100 consecutive engine cycles, while, for the second kind of test, the parameter taken into consideration for the comparison is the time interval employed by the control system to definitively enter the allowed interval values of the A/F, starting from a 10% higher value.

Figure 4 shows the results of this first series of test, normalized with respect to the values measured with the reference DAQCard based system: as clear, the developed ECU revealed a higher precision (i.e. lower dispersion) in maintaining the desired A/F objective value, and approximately the same rapidity in reaching the control window.

As concern the ignition control, the comparison tests aimed to verify both the reliability of the system to ignite the air-fuel mixture and the instability of the combustions produced. For the first comparison, the observed parameter is the number of misfires detected within 200 consecutive engine cycles [18], while for the second comparison two different parameters have been taken into consideration: the Coefficient of Variation (COV) of the Indicated Mean Effective Pressure (IMEP, a fundamental parameter for the characterization of internal combustion engine performances, [19]) and the maximum value of the standard deviation of the in-cylinder pressure measured during the combustion process: both parameters, evaluated over 200 consecutive engine cycles, increase with the combustion instability.

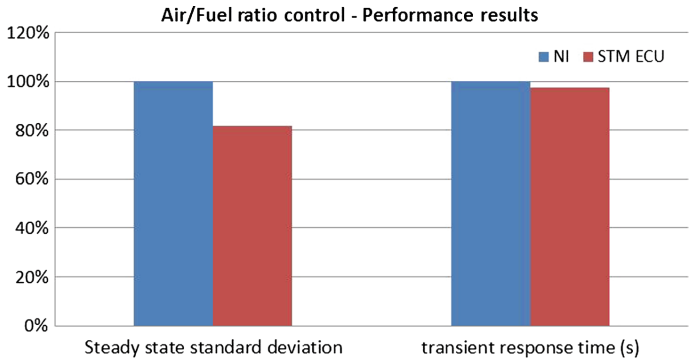

Fig. 4. Results of the Air/Fuel ratio control comparison test

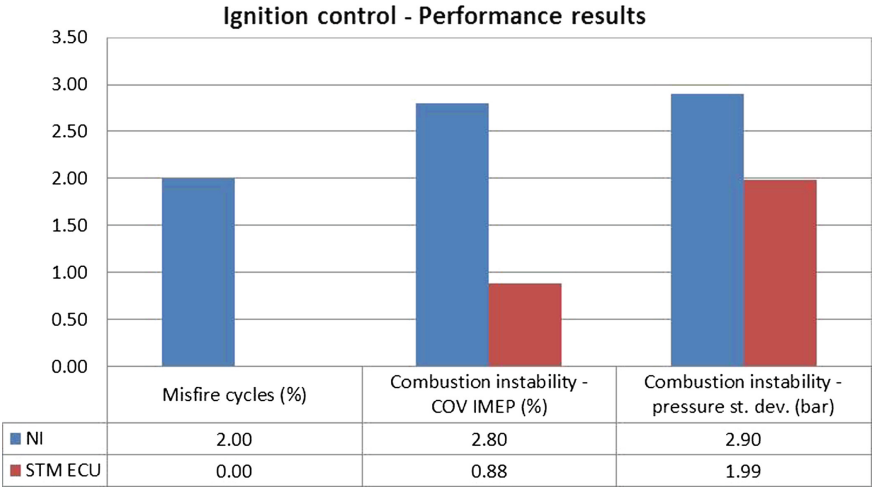

Fig. 5. Results of the ignition control comparison test

As reported in Fig. 5, the developed ECU exhibited a very good reliability, with no misfires detected in the tests. Moreover, the ignition control performed by the ECU revealed also a remarkable lower instability, as resumed by the measured comparison parameters.

The adopted hardware configuration proved a good precision in the acquisition of the analog and digital signals tanks to the microcontroller's computing power; the battery, adequately charged via MAX1758chip, provided up to 8 h of operation thus allowing to work without connecting to the electricity grid and hence without the related electrical interferences; the communication with the PC was ensured by the Low Energy Bluetooth, while the interface with the user revealed very simple and intuitive, allowing to adequately set all the necessary operating parameters of the ECU and of the engine.

4 Conclusions

This work concerns the design and implementation of an electronic control unit for a CFR Bi-Fuel spark ignition engine, based on an ST-Nucleo development board. The designed ECU allows the user to precisely set up the ECU and engine operating parameters, through two different user interfaces:

- Interface with local display and keypad.
- Interface based on the Bluetooth communication protocol between the ECU and an host PC.
- a dedicated application has been created in order to implement the input parameters control view and a live visualization of the engine status from the host PC.

ECU was built with some tailored PCB boards that host all needed components for controlling proper engine operations and the correct acquisition of the analog and digital signals.

It was also developed the firmware for the acquisition of analog and digital signals for the generation of control pulses for the fuel injections and for loading of the ignition coil.

The total cost for the construction of the system is very low compared to other systems that offer the same characteristics.

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Testing of DC/DC Converters for 48 V Electric Vehicles

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Abstract. DC/DC applications in automotive market are expected to require new system specifications in next years. Because of the spreading of electrical cars, the power line at 48 V will be very common. Moreover, the converter chips and external passives are required to occupy less area. A DC/DC solution, meeting such requirements, is presented in this work. The switched capacitors architecture is intended to reduce external passive devices space occupation, whereas sustained electrical power is kept high. This paper discusses a preliminary version of the converter, with experimental results from measurements, and presents the final chip architecture, with some simulation result data.

Keywords: Automotive electronics · Electric/hybrid vehicles · Instrumentation · Measurement systems

1 Introduction

In electric vehicles the DC supply system is moving towards 48 V to manage increased electric power levels, but avoiding to increase too much the current level and hence the cable losses. Due to the presence on-board of low-voltage electronics, 48 V DC/DC converters are key components of next vehicle generation to supply sensors, microcontrollers and memories directly from the 48 V. In the framework of the ATHENIS_3D EU project [1], with VALEO and ams AG industrial partners, we designed two DC/DC converters. A first version has been designed to interface the 48 V with already existing 12 V DC power bus on board vehicles. This version has off-chip control thus allowing to implement the desired control strategy on an external microcontroller.

The final DC/DC version integrates multiplestages to directly supply from the 48 V low-voltage loads (5 and 1.65 V). Due to cranking and overvoltage phenomena, the 48 V nominal battery voltage can vary from 6 to 60 V. Since linear regulators would be too inefficient for applications with a large difference between the input and the output voltage levels, a switching DC/DC converter approach has been followed. Hereafter the new DC/DC converter architecture in its two configurations is briefly presented (Sect. 2). Section 3 presents the testing plan for the DC/DC converter characterization

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phase. Section 4 presents the design of the testing board and the achieved experimental results related to electrical and thermal characterization. Conclusions are drawn in Sect. 5.

2 48 V DC/DC Converter Architectures

The first proposed version of the converter allows to make compatible the classic 12 V automotive devices with the new 48 V standard. A switching technique is used to keep the power efficiency, measured as ratio between output and input electrical power, higher than a linear converter. The converter is an inductorless DC/DC, designed to improve the integration in a single die. It is a step-up/step-down switched capacitor converter. This architecture, see circuit schematic in Fig. 1, is called serial-parallel converter for its typical operating modes. It allows to implement three voltage conversion ratios (VCRs) 2, 1, $1/2$, K in the equation in Fig. 1. Thus with two cascade converters it is possible to convert the wide range voltage in a voltage around 12 V. In particular, a $K = 2$ behavior is obtained by charging the C_{FLY} taking as reference the ground voltage, and by discharging it to output by switching its reference to V_{IN}. The loss in case of load current depends on the flying capacitance value and on the switching frequency used to drive the switches; it is also dependent on η factor, which represents the circuit topology and switches driving.

For this first 48 V converter, it has been decided to implement a single stage in each chip and use two separate chips to convert the 48 V power line to 12 V (see Fig. 4 in Sect. 3). This allows to make more deep test than other configurations. The switch topologies have been specifically designed for this application. HV-MOSFETs in ams AG 0.35 µm technology have been used, that can operate up to 70 V. The used switching frequency is 90 kHz, which has been derived after EMI/EMC (electromagnetic interference, electromagnetic compatibility) analysis in the automotive field. In order to test some control techniques as PWM (Pulse Width Modulation), skip, PFM (Pulse Frequency Modulation) and analyze the best control solution, an external digital block has been implemented for the test chip. The skip and the PFM modes allow for a spreading of the generated electromagnetic noise and hence they improve the EMI performance versus classic PWM. The skip mode is simpler to implement since it does not

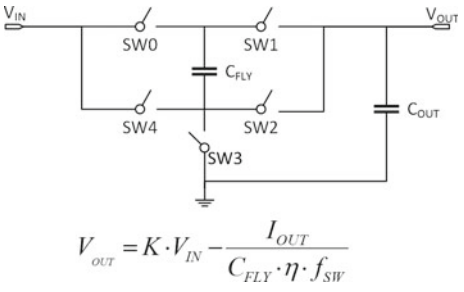

Fig. 1. Circuit schematic

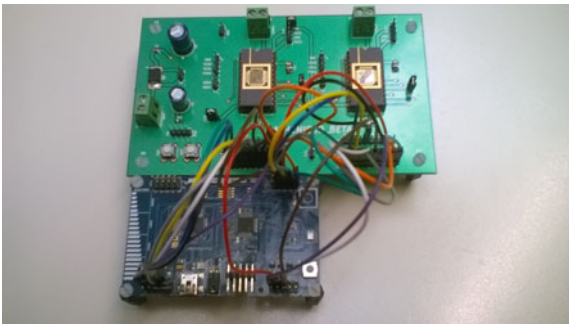

Fig. 2. Test board of the first system version

require voltage controlled oscillators but it can create substrate injection problems when skipping for a long time period in case of low current values. The test version of the DC/DC converter has been bonded in a DIL24 ceramic package. The test board in Fig. 2 has been designed with SMD capacitors, however the project concept aims at stacking capacitors on top of the converter IC, thus minimizing PCB area.

The second converter version is an upgrade of the first one. It converts the wide input voltage (6 V up to 60 V) in two regulated voltages, 5 and 1.65 V, with a target load current from few tens of mA up to 300 mA. This converter is a multi-stage system composed by the same first version converter, a galvanic insulator block (we patented in [2]), another DC/DC converter stage and two low-dropout regulators (LDO) Fig. 3. The entire system is integrated in a single die of 36 mm^2 (including the area of the big PADs) in 0.35 µm HV-CMOS technology.

The principle of operation of the insulator block is to insert one or several serial capacitors to guarantee the output-to-input insulation, even in case of switches failures. A switched capacitor technique has been used in order to avoid bulky inductors and transformers. If at least one switch (or more) fails, there is no possibility to have over-voltage at the output. The aim of the second converter stage is to decrease the voltage around 6 V and to keep a high efficiency level. This stage allows to obtain the VCRs

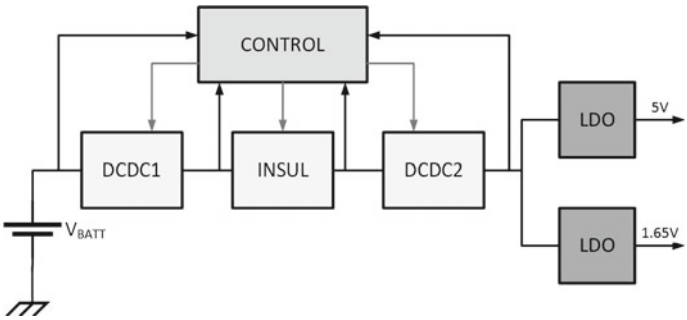

Fig. 3. Multistage architecture of the complete ATHENIS_3D 48 V DC/DC converter

1/2 and 1/3 by using two flying capacitors and more switches. A flash ADC converter is used to choose the operating mode of both converter stages. It compares the input voltage with reference voltages and generates a digital signal for the control block. About the LDOs blocks, integrated architectures we already proposed in literature [3] have been adopted. Operating with an input voltage much lower than 48 V, the LDO regulators have acceptable efficiency.

Both the converters have been designed and simulated in all PVT (Process-Voltage-Temperature) corner cases at layout level with Cadence-Virtuoso tools and the results are compared with those obtained from the measurements. The regulation capability of each switching-capacitor DC/DC converter stage depends on the switching frequency f_{SW}, on the size of the capacitor C_{FLY} plus a terms η depending on the conversion ratio: $V_{OUT} = KV_{IN}I_{OUT}/(\eta \cdot C_{FLY} \cdot f_{SW})$. The power supply rejection ratio (PSRR) of the whole converter in Fig. 3 is at least -40 dB at low frequencies and -90 dB at the switching frequency. As result, without using inductors but just capacitors (with values from 100 nF to 10 µF) the design allows to regulate high input voltages (one order of magnitude of variation from 6 to 60 V). With respect to 48 V DC/DC converters using inductors, our converter has a comparable efficiency when supplying low-voltage loads with output currents limited to hundreds of mA, and reduces size and weight avoiding inductors and transformers.

3 Testing Plan

The architecture for a preliminary testing of the system is shown in Fig. 4. Since the test chip version only implements the first DC/DC stage of the complete ATHENIS_3D system, its testing has been designed in order to measure the performances of a series of two stages.

The switching phases control is implemented on the microcontroller unit: no digital part has been included in the test chip version of ATHENIS_3D. The goal of such architecture is to measure some of the performance parameters of the DC/DC, both for a single stage and for a series configuration, and to check the reliability of the ASIC simulations in real application. The devices under test (hereafter, DUTs) have been mounted in the same functional configuration (i.e. flying and load capacitance included). An anti-EMI filter to block the electromagnetic conductive interference to V_{BATT} source has been designed for this application, too.

3.1 Microcontroller Block

The microcontroller block is responsible for generating the phase signals for driving the power MOSFETs acting as switches (architecture shown in Fig. 1) of both DUTs. It performs the skip control in case of too large output voltage; it also initializes the devices with proper startup signal. The chosen microcontroller for this application was an ATMEL® AT32UC3L064. It has been adopted in a ready-to-use evaluation board, UC3-L0 XPLAINED, for its good availability of I/O PINs to be connected to DUTs.

For each DUT, seven phase signals had to be generated, whose behavior depended on the current DUT input voltage state. Some of the phases for the second stage can be

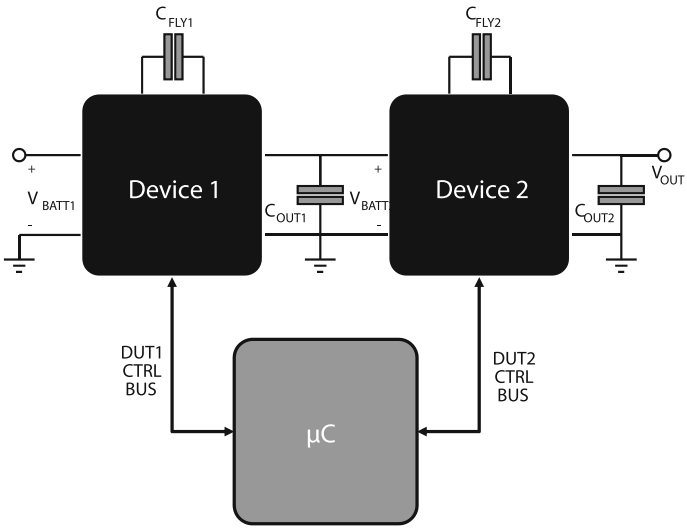

Fig. 4. Test concept scheme

kept in fixed (logic 1 or logic 0) state, since the testing architecture allows the second DUT to be driven only in unitary and half modes (as shown in Sect. 2). Phases are conventionally called 'positive' when the positive edge is occurring in the first half of the period, 'negative' when the positive edge is in the second half of the period. Some phases are always on or off, depending on the current driving mode. An important condition on the phases driving is that two in-phase signals must be fully overlapped: the first signal set must be reset after the reset event of the other signal. The period of the phases lasts $11.125\,\mu s$, corresponding to about $90\,kHz$. The phase generation has been implemented by the configuration of a microcontroller timer counter resource. The skip control is only enabled once a switching event has been fully completed (i.e. after all the rising and falling edges at the beginning and in the middle of a period). If the skip request is received, all phases are frozen in their current state. The startup procedure simply keeps in set state (i.e. '1') a signal for a period of $1.79\,ms$.

3.2 Parameters Under Test

The device configurations to be tested are summarized in Table 1.

4 Test Setup and Results

The testing board (Fig. 2) developed for the beta version of ATHENIS_3D implements the testing scheme proposed in previous section (Fig. 4). It has the input filter on-board and configurable connectors to measure the output voltage of both stages. Other connectors are used to link the microcontroller I/O signals (switching phases, skip and startup signals) and to monitor them, and to configure the phase generation mode for

Table 1. DC/DC parameters under test

Test name	Procedure	Notes
Line regulation test	Sweep V_{BATT} input and measure DUT1 and DUT2 output voltage	*Test performed in nominal load conditions*
Load regulation test	Sweep load with nominal V_{BATT} applied to input	
Efficiency test	Measure the ratio between output and input electrical power	*Wait the transients to be finished*
No load test	Measure output voltage in case of zero-current sinking	
Ripple test	Measure min, mean and max output voltages to find out ripple factor	*Ripple factor γ is the ratio between ripple voltage and mean voltage*

both the DUTs. The SMD capacitors used for test purposes were $3.3\,\mu$F for the C_{FLY} and $10\,\mu$F for the C_{out}, for both DUTs. Some preliminary tests have been performed, following the test protocol summarized in Table 1. Input voltage range has been swept from 6 to 60 V and output current has been set to a wide range of values, from 0 A up to 1 A, in order to simulate different load conditions. Preliminary results show correct operations for nominal input voltage (48 V) and load currents up to 240 mA. In the same input nominal condition and for 150 mA sunk at the output, we measured an efficiency of 80.5%. An important parameter for such a switching architecture is the output ripple voltage. The ripple factor was measured to be 0.13% in nominal conditions ($V_{BATT} = 48$ V, $I_{LOAD} = 150$ mA): the output voltage was 10.33 V, while the peak-to-peak ripple voltage excursion was 13 mV.

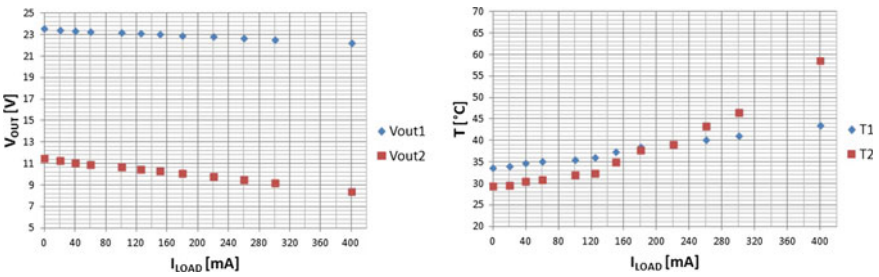

Fig. 5. Load regulation test results. Output voltages profiles and temperature profiles for both devices by sweeping load current

Some more detailed data have been acquired in order to characterize the architecture by ranging the load current (Load Regulation Test). In Fig. 5 output voltages (of both devices) for a $V_{BATT} = 48\,\mathrm{V}$ test are shown. The load current has been swept from $0\,\mathrm{A}$ up to $400\,\mathrm{mA}$. As an innovation with respect to the state of the art, the proposed $48\,\mathrm{V}$ DC/DC converter avoids cumbersome transformers versus inductor based converters, [3,4], and increases the working voltage and current levels versus known switched-cap converters [5,6], typically limited to low-power applications.

5 Conclusions

This work aims at presenting a novel architecture for implementing next-generation DC/DC converters in harsh automotive application (large temperature range, high-voltages, hard reliability and safety requirements) [7,8], where the power line at $48\,\mathrm{V}$ is expected to spread in electric car applications. The architecture is based on switching capacitors, in order to reduce die size by avoiding the usage of inductors.

This work has been carried out within the EU project ATHENIS_3D. The test chip architecture has been presented and evaluated through experimental measurements. At $48\,\mathrm{V}$ its ripple factor is 0.13%, whereas the measured efficiency is 80.5% Experimental results of the test chip and deeper simulations suggest the final architecture of ATHENIS_3D to meet the efficiency and stability requirements.

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Miscellaneous

Wake up for Power Line Communication in Street Lighting Networks

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Abstract. Street lighting is responsible of a big share of electricity consumption of a city. The modernization of such a big network is required to meet the needs of energy saving for the future Smart City, helping to reach a reduction of greenhouse gas emissions also. In this work, we introduce a wake-up system, which permits to reduce the power consumption of receiving modem in power line communication, with particular attention to street lighting networks. Experimental and simulation results will show the optimal parameter configuration necessary to the system.

Keywords: Power Line Communication · PLM · Embedded systems · Wake-up ove power line · Energy harvesting

1 Introduction

Power Line Communication (PLC) is a well-known technology, widespread in many application fields thanks to its versatility. In fact, the use of the same conductor both for powering the device and transmit data over a network permits to save the money for a dedicated communication infrastructure. For this driving reason, PLC is commonly used for remote monitoring and metering in Smart Grid. PLC technology expose also some drawbacks, as the limited communication range achievable by high bandwidth PLC for instance [1]. In M2M (and metering also) communication however low throughput communication are usually enough to ensure the service, because data has low data rate can be often compressed using recent and efficient techniques [2–4]. This kind of technology falls under the Narrowband PLC (NB-PLC) classification (frequency bands between 3 and 148.5 kHz), while higher data rates require higher transmitting frequencies that classify the PLC as Broadband (BB-PLC) also used for last-mile internet connectivity. The PLC technology electrical requirements and constraints (e.g. transmitting power, impedance) are regulated in Europe by norms EN-50065, which define the mentioned frequency bands [5].

We focused our attention on NB-PLC for smart lighting systems, already widespread in many lighting lines in Europe, for monitoring and controlling the lights in a smart and energy-aware way [6, 7]. This allows to save a big share of energy with an intelligent management of the lighting posts, as envisioned nowadays in any Smart City [8]. Just to provide some figures, the outdoor lighting electricity share reach the 19% of

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the total electricity consumption of a city and lighting in general is responsible for 6% of the total greenhouse gasses emissions globally [8–11]. The designed wake-up mechanism permits to save 0.5 W from each modem in receiving mode, that is the power consumption of the modem in stand-by mode, allowing to turn on selectively the modem on a specific lamp post and then manage its lamp.

A wake-up mechanism is well known for radio frequency signals [12]. Here, we propose and describe a version for Power Line Communication, with a circuit capable to keep switched off the PLC modem until a specific message is injected into the network. The wake-up signal can be broadcasted or addressed to a specific node. The receiver decodes the wakeup message and, in case of matching, turns the main modem on to let the PLC communication begin. In this way, a zero-power stand-by system is implemented, allowing to reduce the power consumption when no communication is needed.

This paper provides an extensive description of the hardware designed to realize the wakeup method, with details on implementation and tests performed on prototypes. Furthermore, some effects that often occurs in street lighting PLC networks are analyzed, and configuration parameters are optimized to keep the overall power consumption as low as possible.

The paper is organized as follows: Wake-up system concepts and hardware are provided in the next Section, while the architecture of the network is introduced in Sect. 3, with the effects of common elements characterizing a street lighting network. In Sect. 4, simulation results are presented and the optimal addressing technique is identified. Then conclusion remarks are provided with some future improvements.

2 Wake up System

A street lighting line is usually managed by a concentrator (a kind of a server), which communicates to the modems installed on each lamp post through PLC. To turn on only a specific modem over the line, some elements are added to each modem, i.e. an energy harvesting module, capable of scavenging the energy needed to decode the signal and eventually turn on the main electronics; and a decoder element, that is necessary to detect if the system receives a correct address for triggering the PLC modem.

The energy harvester implemented on our lasts prototypes [13, 14] is shown in Fig. 1. It is a Cockcroft-Walton voltage multiplier used to scavenge a usable voltage from the low signal input. Note that the signal used is the very same that propagates through the network and it is used by the main modem to communicate. In terms of received power by the system, this could be a serious problem because the impedance of the line is not matched and even the modem itself, when turned off, can represent a disturbing element, attenuating the signal. Therefore, it is needed add a switch that enable to route the incoming signal either to the modem or the wake-up system.

The next microcontroller decodes the signal thanks to a comparator used as an envelope detector with the signal coming from the voltage multiplier. The address in fact is encoded in a plain OOK (On-Off Keying) modulation allowing a simple detection. If the code matches the address, a solid state relay is triggered, turning on the

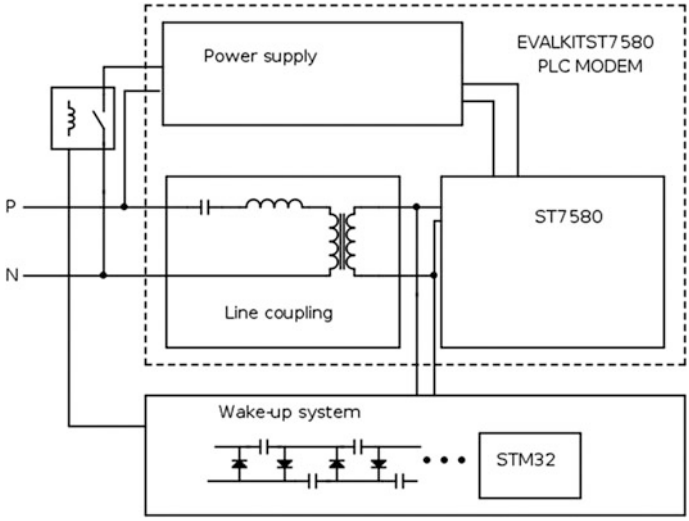

Fig. 1. Architecture of the wake-up system for PLC

modem, that otherwise the modem remains off. The whole system, is based on ST7580 evaluation kit as modem and a STM32 low power microcontroller as decoder, all provided by STMicroelectronics. Figure 2 shows the real prototype with the modem we used.

The test needed to characterize the system has been carried out by means of a 90 m electric line typically used for street lighting. The modems and some High-Intensity Discharge lamp (HID) ballasts represent each lamp post accurately. The test bed allows to validate the data simulated in a SPICE environment and presented in the following besides understanding the problems related to a typical street lighting network.

3 Effect of Street Lighting Elements on Transmitted Signal

We evaluated the performance of the system in scenario similar to a real street lighting network. Regarding this, two type of experiments have been investigated, one for understanding the effect of the line impedance and the other one for the effect of the lamp ballast. The measurement are performed with a testbed in laboratory made of a 90 m cable with the same characteristics of the one used for lighting networks, with some branches at specific distances. The measurements are used also to validate the simulations showed in the upcoming sections.

3.1 Effect of Line Impedance

The assessment of the system is performed with a 5 Ω impedance connected to the line, which represents an impedance discontinuity present on power lines that leads to mismatches in PLC networks. Main causes of the discontinuity are lines branches and

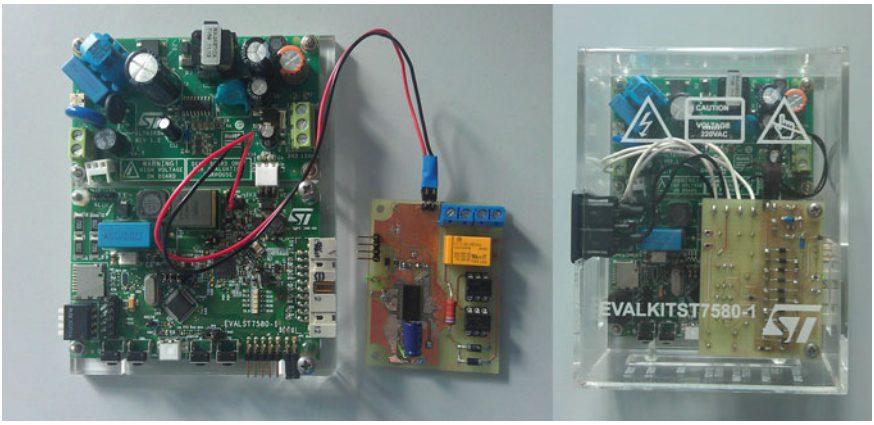

Fig. 2. Pictures of the designed prototype with the main PLC modem used for the tests

interconnections, that can be seen as low impedance loads or impedance discontinuity. Consequently, the presence of low disturbing impedance leads to signal attenuation at the receiver. With this respect, 5 Ω impedance was placed in different positions, before or after receiver to explore the signal attenuation at the receiver. The same experiments were done for both FSK and B-PSK modulations.

Figure 3 illustrates the results when 5 Ω load is placed in various position with respect to transmitter and receiver. When 5 Ω load is between transmitter and receiver, signal attenuation at the receiver incremented for both FSK and B-PSK, see case 2 and 4. For instance, signal attenuation for FSK in case 2 compared to case 1 is increased from 6 to 14 dB. It is evident that FSK with respect to Coded B-PSK has less signal attenuation (almost 2 dB).

3.2 Effect of Lamp Ballast

Considering that lamp ballasts are used in real street lighting network, it is needed to investigate its effect on the received signal and in the specific, how it affects the propagation of the signal through the network. For this reason, we have used lamp ballast before and after the receiver node that we would like to turn on. Indeed, this experiment was conducted to see whether lamp ballast would attenuate the signal at the receiver or not. Figure 4 demonstrates that when lamp ballast was positioned between transmitter and receiver, signal attenuation was decreased.

Although the effect of street lighting elements on transmitted signal in laboratory environment is very important to provide an insight for the performance of the wake up system in street lighting, another key concern is regarding simulation of street lighting network with optimal transmission architecture.

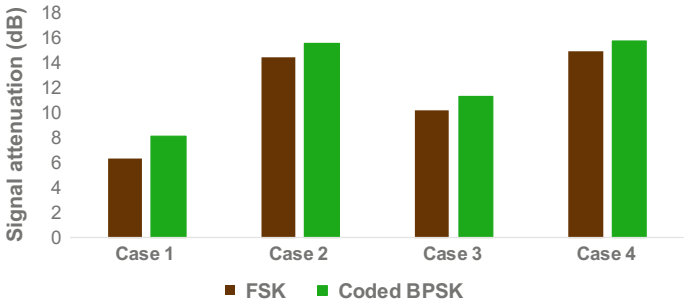

Fig. 3. Signal attenuation when 5 Ω is placed along the line. *Case 1* Transmitter at 0 m, receiver at 90 m. *Case 2* Transmitter at 0 m, lamp ballast at 60 m, 5 Ω impedance at 70 m, receiver at 90 m. *Case 3* Transmitter at 0 m, receiver at 60 m, 5 Ω impedance at 90 m. *Case 4* Transmitter at 0 m, 5 Ω impedance at 60 m, receiver at 90 m

4 Simulation of Street Lighting Network for the Best Routing Method

The main purpose of this investigation is to find a routing configuration that minimizes the total transmission power while remotely controlling the lamps, i.e. Transmission through several paths (hops) to reach the desired node. With this respect, tests were conducted to obtain an optimal routing configuration, which leads to minimum consumed power. The search is in the direction to find an efficient transmission and receiver structure that leads to minimum total transmission power from transmitter until the node we would like to turn on. Regarding this, the simulation network model for the whole network and the result of various network architectures are provided.

We chose to use a simple but powerful approach modeling each element of the network as a SPICE element, using the very same schematic from the producer of the ballast and the PLC modem (in our case STMicroelectronics, but many other implementations do not differ too much). The cable on the other hand was modeled as a RL element, as shown in previous contribution [13] to be suitable because of the negligible effect of the cable capacitance that is actually dominated by the end-points of the network (total capacity of the lamp ballast and input stages of PLC modem).

4.1 Simulation of the Whole Network

PLC network was simulated according this model: the total length of the line is 240 m, one transmitter is placed at one end, followed by 10 receivers (each one composed by lamb ballast, PLC modem and wake up system). Two 10 Ω loads was added in the system to take in account the line impedance attenuation.

The purpose of the simulation was to convey various voltage levels in order to identify the set-up that allows to turn on a specific lamp using the minimum total transmission power. The main constraint was on the output of energy harvesting system

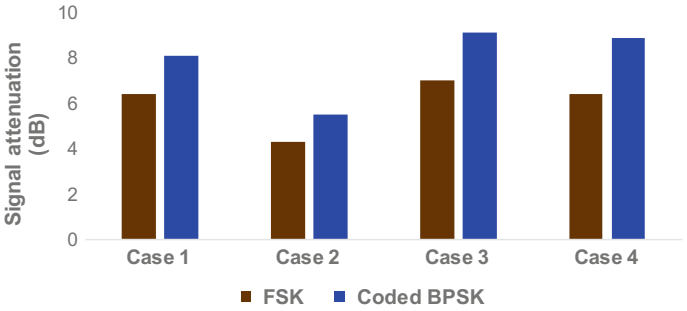

Fig. 4. Signal attenuation when HID lamp ballast is placed along the line. *Topology 1* Transmitter at 0 m, receiver at 90 m. *Topology 2* Transmitter at 0 m, lamp ballast at 60 m, receiver at 90 m. *Topology 3* Transmitter at 0 m, receiver at 60 m, lamp ballast at 90 m. *Topology 4* Transmitter at 0 m, lamp ballast at 60 m, receiver at 70 m, lamp ballast at 90 m

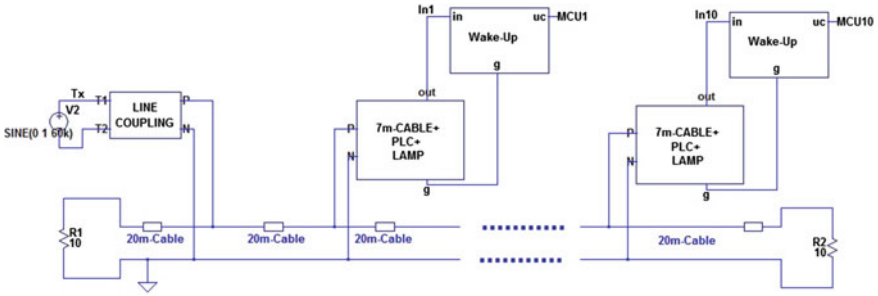

Fig. 5. Schematic of the simulations

that should provide at least 1.8 V to ensure the operation of the microcontroller; for instance, to reach this value at least 0.7 Vpp should be provided at the input of receiver.

We keep in consideration several network architectures. In particular, we design the simulation to provide one hop, two hops and multiple hops see Fig. 6 and the relative simulation in Fig. 5. A configuration with less hopes need less re-transmission of the signal, but inevitably require more power due to the long distance to be covered. In case of two or multiple hops we considered the total amount of power as the sum of power required to re-transmit the signal at each hop. As an example, one could turn on the 8th receiver with one hop which requires one transmission. However, two hops require retransmission, transmission up to 4th node then retransmission from that lamp up to 8th node.

4.2 Result of Various Simulations

Figure 7 shows that on one hand, one hop transmitting for long distance consumes more power than more hops (retransmissions). This is due to the presence of two 10 Ω

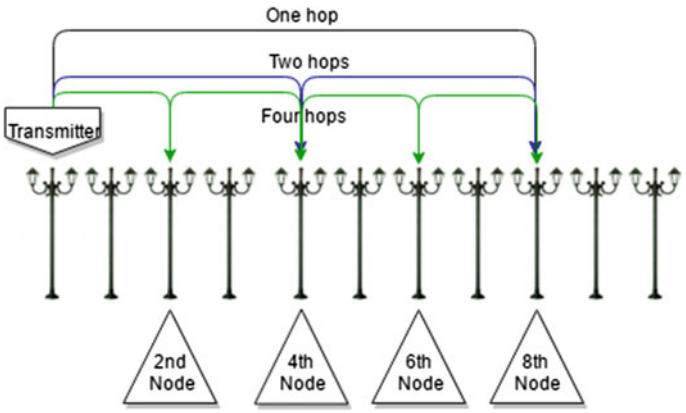

Fig. 6. Turning on desired lamp (8th lamp) through different hopping structure

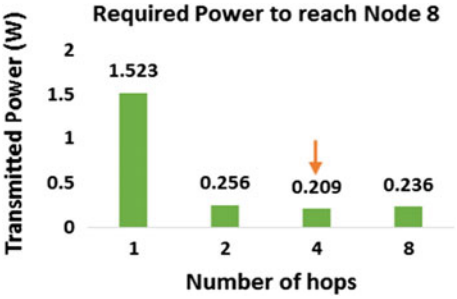

Fig. 7. Measured transmission power for each hopping structure to turn on the 8th lamp

disturbing impedances in parallel to the network, that represents line impedance, i.e. unknown part of the line, that can actually be longer than the one simulated. Besides this, the nonlinearity of the system also causes the growth of the transmitting power. In fact the wake-up system added to each lamp post has different response for different signal gain, showing higher impedance for lower signals. On the other hand, increasing number of hops in the way that every lamp would wake up only the next nearest lamp is not convenient neither. As it is apparent form the Fig. 7, the minimum total transmission power is decreasing by increasing number of paths (hops) to reach desired node until the system reaches an optimal number of hops. In fact, the most efficient solution is found with four hops, because it requires less power to turn on the 8th lamp. In this case, first we transmit wake up signal to 2nd node. After turning on the second node, that node retransmits signal to 4th node, then 4th node do the same and retransmit to 6th node until eventually 6th node retransmits to 8th lamp. Therefore, the desired 8th lamp will be turned on through 4 hops (paths).

Of course, we tested different configuration also, finding that to reach the 6th node 3 hops are the optimal solution, while the 10th node is reachable with 5 hops.

5 Conclusion

We presented how to approach the problem of stand-by power consumption in a street lighting network, with particular emphasis on optimizing the system from a network architecture point of view. Various tests have been performed and reported for identify the effect of network elements. Results from simulation highlight the optimal number of hops needed to address the 8th node with the minimum amount of power. The work still need some improvements to meet the high performance requirement of the actual PLC networks, but for quite small lighting system has been proved to be suitable.

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High Resolution Time Domain Reflectometry for Dielectric State Monitoring in High Voltage Cables

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Abstract. A high resolution Time Domain Reflectometry system has been designed in order to investigate the possibility of measuring with good accuracy the dielectric properties of high voltage cables insulator materials by means of Time-of-Flight measures. The system employs a dedicated Time-To-Digital Converter in order to achieve a time resolution of 90 ps. By exploiting averaging techniques the resolution has been further increased. Experimental results showed the possibility of measuring the dielectric constant with a resolution of 0.03%.

Keywords: Time Domain Reflectometry · Time-of-Flight measurement · Time-to-Digital Converter · Dielectric state monitoring

1 Introduction

Time Domain Reflectometry (TDR) is a well-known technique employed in a large number of applications comprising RADAR, LIDAR, SONAR and fiber optic test. In all these cases an impulsive signal is used to probe the characteristics of a medium by processing the reflected energy. In cable industry TDR is commonly used to detect and locate faults, damages or even theft of cables. However in these cases the parameter of interest is essentially the length of the cable, that can be evaluated from the pulse Time-of-Flight, i.e. the time that the pulse takes to propagate to the end of the cable and back to the source after the reflection due to the impedance discontinuity at the end of the cable, and the resolution is in the range of 1–10 m, as in [1], where the system is usually bulky and expensive. Some others cable fault-test instruments are based instead on patented tone injection signals [2] and are usually handheld but suffer of substantially lower accuracy, especially with longer cables.

In case of High Voltage (HV) and Medium Voltage (MV) cables, or also for coaxial cables and transmission lines, the pulse propagation velocity (directly affecting the pulse Time-of-Flight) is strictly related to the line impedance and so to the dielectric

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properties of the insulating material from which the cable is composed. In normal condition this is a known and very stable parameter. However in case of degradation of the dielectric material, the dielectric constant and in turn the propagation velocity may slightly change. The pulse propagation velocity can be so employed as a diagnostic parameter, related to dielectric aging, wear and integrity.

In this paper we describe a small, low power and low cost embedded system designed to precisely monitor the dielectric properties of an electric cable by measuring the pulse Time-of-Flight with a high degree of accuracy. The system has been designed specifically for testing and monitoring of HV and MV cables, where the dielectric layer has a primary importance in guaranteeing the proper operation of the asset. In particular the system allows to precisely determine the propagation velocity and so the dielectric constant given a fixed length of cable.

Section 2 introduces the theory of operation of the TDR technique and the system, Sect. 3 describes the system implementation, Sect. 4 shows some experimental results, and finally in Sect. 5 some conclusions are drawn.

2 TDR Theory of Operation

The employed electric TDR technique is based on the generation of an impulsive electric signal, its transmission on the cable, acting as a transmission line, and the time domain analysis of the reflected signal from an abrupt impedance discontinuity (typically the end of the line).

The designed TDR circuit injects a voltage pulse, whose duration is much smaller than the expected Time-of-Flight, typically in the order of 10 ns, that propagates along the line and is reflected back at the cable end. As known from transmission line theory, if the cable end is left open or is closed on a low-impedance resistive load the reflected pulse has approximately the same amplitude of the impinging pulse.

The designed circuit generated the pulse and measures the time between its injection and the reflection. This time equals to the Time-of-Flight (ToF), that as already mentioned, is related to the length of the cable, the propagation velocity and the dielectric constant of the insulator material, according Eq. (1):

$$2 \cdot L = ToF \cdot \frac{1}{\sqrt{\varepsilon_r \cdot \mu_r}} \cdot c \Rightarrow \varepsilon_r = \left(\frac{ToF}{2 \cdot L}\right)^2 \cdot \frac{1}{\mu_r} \tag{1}$$

where c is the speed of light, ε_r is the dielectric constant, L is the cable length, whereas μ_r is the magnetic permeability that usually is very close to 1.

So, from the measurement of the ToF it is possible to determine the cable length L or precisely detect small variations of the dielectric constant with respect the nominal value.

The ToF is precisely measured by using a dedicate Time-To-Digital Converter (TDC) unit and the resolution is further increased by employing a simple, yet effective, averaging technique.

3 System Implementation

Despite its good performances, the implemented system is quite simple. Its block diagram is shown in Fig. 1. An STM32 microcontroller (MCU), based on an ARM Cortex M4 core that handles all the measurement sequence, consisting in setting the detection threshold on the Analog Front-End, generating the pulses and configuring the TDC unit to take the measure. The sequence is repeated a programmable number of times and the results averaged in order to increase the resolution via oversampling technique.

The front-end circuit includes a pulses generator and a pulse detection circuit and is shown in Fig. 2. The pulse generator is implemented by a simple differentiator capacitor (C1). One pin of the microcontroller, configured as high slew-rate digital output, is connected directly to the differentiator that generates a very narrow voltage pulse at each level transition of the output pin. This signal is applied to the cable (directly o by means of suitable capacitive or inductive couplers).

The pulse detection circuit is implemented with a high speed voltage comparator (TVL3501) that also receives as reference voltage (at its inverting input) the threshold voltage set by the MCU, generated with its internal DAC. The threshold is automatically determined by the micro-controller by sweeping the voltages level until the TDC detects the reflected pulses. The injected pulse (that is also detected by the comparator) and the reflected ones are sent to the TDC inputs in order to measure their time distance. The TDC is configured to take into account only the first two pulses (there may be more than one reflection). Figure 3 shows some of the signals taken at the front-end: the blue signal is the one applied to the cable, showing the first (injected) pulse and two reflections, the red signal is the comparator output for the chosen threshold level.

The TDC unit is an ACAM TDC-GP22, featuring a resolution of 90 ps. It is connected by an SPI interface to the MCU. The TDC has a START channel and two STOP channels. It has been programmed for measuring the time between two subsequent pulses on one STOP channel (connected to the comparator). The START signal is provided by the MCU and is asserted just before generating the pulse to inject.

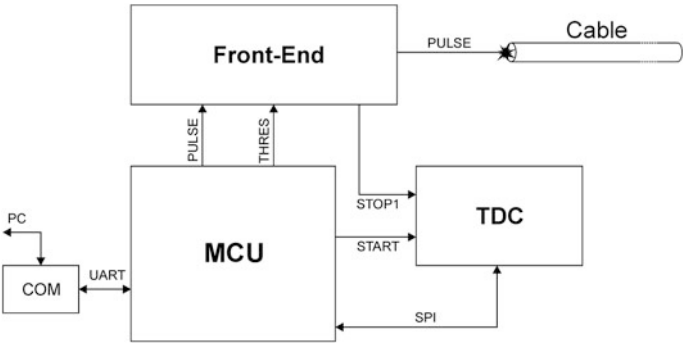

Fig. 1. Block diagram of the TDR system

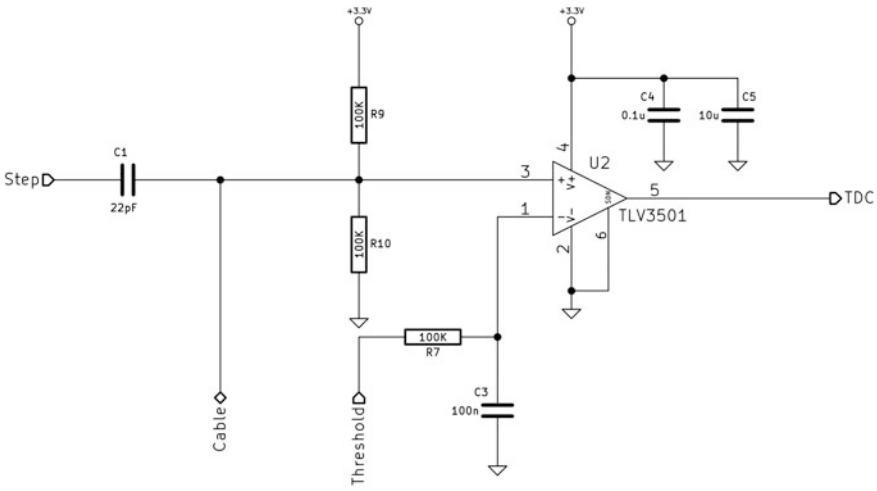

Fig. 2. Electric schematic of the front-end circuit

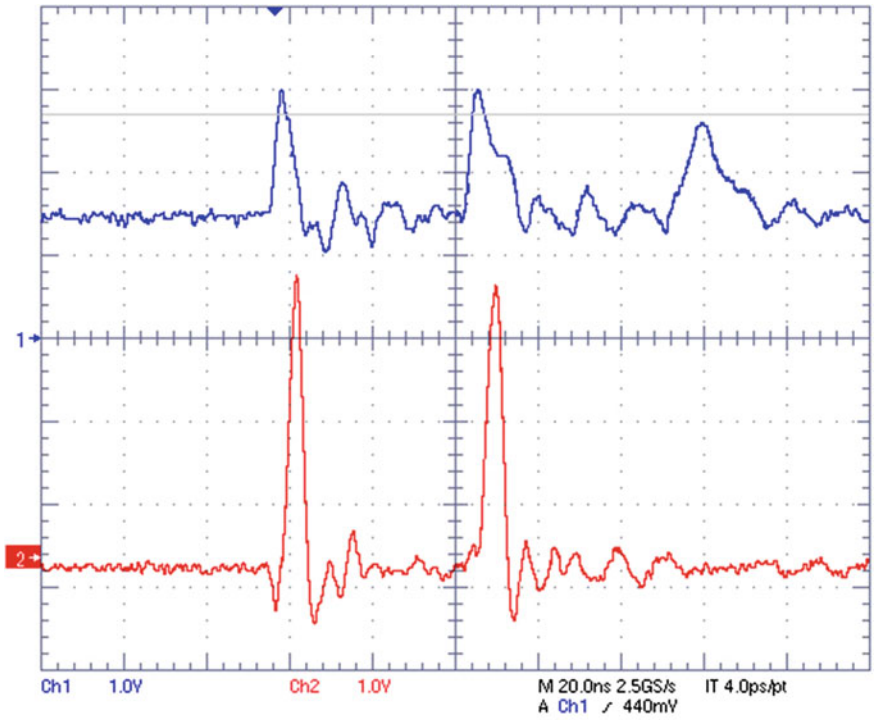

Fig. 3. Injected pulse with the first and second reflection are shown in *blue*. The injected pulse and the first reflected pulse detected from the threshold comparator are shown in *red*

This configuration allows to achieve the maximum resolution and to overcome the 3.5 ns dead time that the TDC has following the assertion of the START signal.

The measurement results are accumulated and processed in the MCU memory, performing an average. The output values are provided by a serial connection with a PC that is also used to issue commands and settings to the system.

4 Experimental Results

A series of tests were performed directly connecting a cable, terminated in an open circuit, to the measurement setup and measuring the ToF at different lengths.

A radio frequency coaxial cable was chosen for test due to its structural similarity with HV and MV cables. The coaxial cable had defined and precisely known length, and the electrical characteristics reported in Table 1.

The initial cable length was 5.722 m and the dielectric constant was evaluated by ToF measurement through the relation (1). Each measure was achieved by averaging the ToF of 2048 pulses. In order to evaluate the robustness of the method and system, and the consistency of the results, a set of 82 measures were taken at various cable lengths. In particular the cable was shortened of 1 mm at each measurement. Results

Table 1. Electric characteristics reported on the datasheet of the tested coaxial cable

Diameter (mm)	Impedance (Ω)	Speed factor	Capacity (pF/m)
6.8	75	0.8	55

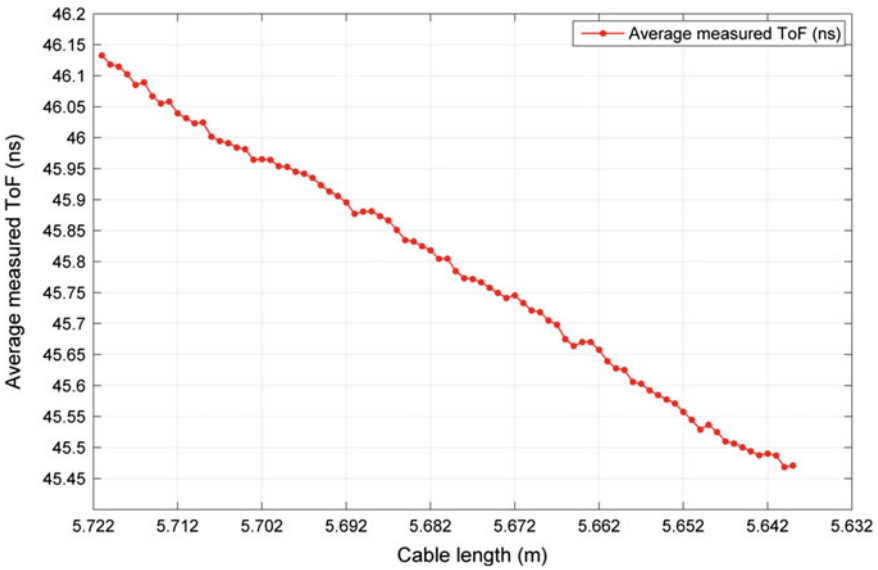

Fig. 4. ToF measured for different cable length by the average of 2048 samples

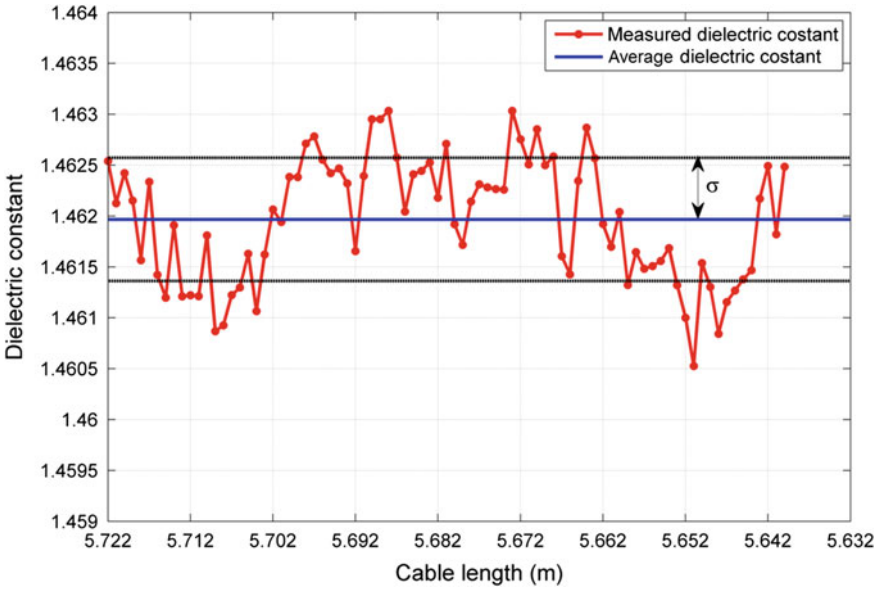

Fig. 5. Dielectric constant evaluated for each cable length in *red*; Average value (coincident with nominal value) in *blue*

are reported in Fig. 4. As it can be seen, the averaging technique was quite effective in enhancing the measurement resolution, in fact it was possible to detect the difference of 1 mm in length with a nominal temporal resolution of 90 ps, that should only guarantee a spatial resolution of 21 mm. Starting from the obtained ToF measurements the dielectric constant has been evaluated, as plotted in Fig. 5.

From these data an average dielectric constant of 1.4619 was obtained (this value is confirmed by nominal cable data) with a standard deviation σ evaluated as the following value:

$$\sigma = 6.0593 \times 10^{-4}$$

This very small value allows to conclude that measurements with the proposed system achieved a very good accuracy and repetitiveness, also very small variation of dielectric constant as well as length can be detected.

5 Conclusions

A powerful yet very low cost dielectric constant measurement system has been designed and experimentally tested. Based on a TDC and an STM32 microcontroller, the developed system has been capable to automatically measure, with very high accuracy, the dielectric properties of cables, reaching a time resolution well beyond the TDC native one, by means of simple and fast averaging techniques. Finally the system

present very versatile features, thus envisaging the possibilities to be used as an effective and portable instrument whenever Time of Flight based test could improve investigations.

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A Calorimetry Based System for Measuring the Power Losses of Switching Power Devices

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Abstract. A system made of a custom designed heat flow sensor, a thermo-electric heat-pump, and a microcontroller based control board is presented for the measure of the power losses in power switches, e.g. MOSFETs or BJTs, operating in dynamic repetitive regime. The heat-flux sensor consists of two highly linear proportional to absolute temperature (PTAT) CMOS sensors. The thermoelectric module holds the case of the device under test at ambient temperature, so that heat entirely flows through the calorimeter. As the dissipated power measurement relies on the measurement of a heat flow, the apparatus is particularly suitable, and provides reliable results, in fast switching devices, regardless of the switching frequency, thus overcoming the problems associated with direct electrical measurements.

Keywords: Calorimetry · Heat-flux sensor · Power losses measurement · PTAT sensor

1 Introduction

The measurement of the efficiency of a power electronic converter is crucial to evaluate the performance and reliability of any electronic system as a whole. However, these measurements are getting more and more difficult because of the rise of the operating frequencies of semiconductor devices, due to limitations intrinsic to electrical measurement methods. In fact, direct electrical measurement methods of the power losses based on the instantaneous product of current times voltage, $i \times v$, can be performed easily and with good precision only for low frequency waveforms. As frequency increases, they present errors associated with the limited precision of the digital instruments, affected by probes delays, phase shifts between acquisition channels, sampling errors, and non-linearity of A/D converters [1].

The calorimetric methods allow to measure the power losses as the heat dissipated by a device, and they are not affected by the aforesaid problems also for signals at very high frequencies. Among the several calorimetric systems presented in literature [1–3], a simple method is that based on a heat-flux sensor, in which the heat generated by the switching device flows through a heat-flux, generating a temperature gradient proportional to the power losses. The solution adopted in this work is very simple because it does not require the use of isolated chambers or sophisticated controls, and can be built with a small expense.

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The working principle of the apparatus was already presented in [4]. Differently from previous realizations [4–6], in this paper we present a new implementation of the heat-flux sensor, realized by stacking two custom designed microchips [7], each integrating a temperature sensor and control electronics.

2 Apparatus

A schematic view of the apparatus is shown in Fig. 1. The thermoelectric module (TEM) is used to extract the heat from the device under test (DUT) and to keep it at ambient temperature. The apparatus is isolated from the ambient with a polystyrene structure to further reduce the heat-leakage, whereas a heat-sink is attached to the thermoelectric module to dissipate the heat generated. When the device is in thermal equilibrium with air, the heat exchange only occurs through the heat-flux sensor.

The apparatus is controlled by a microcontroller based board that reads the temperatures of the various sensors and implements a digital PID regulator. It regulates, through a PWM signal, the bias of the TEM and therefore the temperature of the DUT such that it converges to the temperature of the ambient. The board includes some circuits for the amplification and acquisition of the analog signals from the PTAT sensors that constitute the heat-flux sensor, and from two PT100 resistive temperature detectors used to detect the temperature of the ambient and of the DUT package. A computer application allows to set the working parameters of the controller and to monitor the measurements.

The measurements of the temperature gradient (ΔT) across the heat-flux sensor are made when the DUT is steadily at room temperature, such that they will represent the whole power dissipated by the device with a minimum error.

A picture of the whole system is shown in Fig. 2.

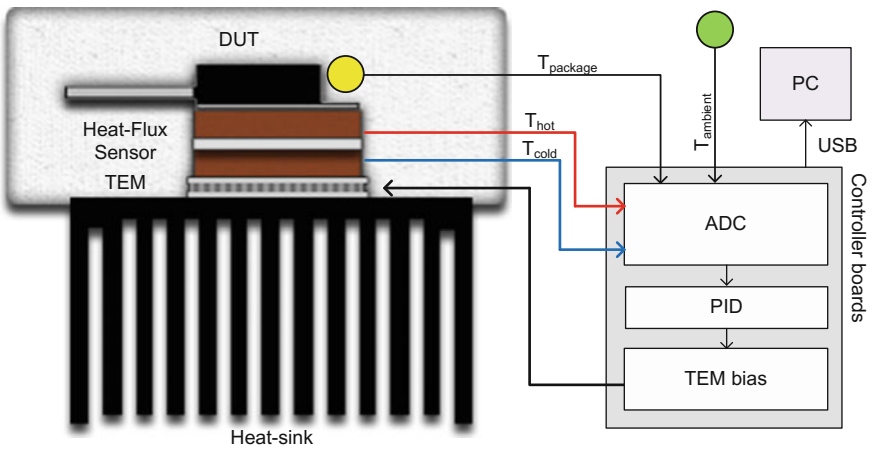

Fig. 1. Structure of the apparatus, comprising the heat-flux sensor, between the DUT and the TEM, isolated from the ambient with polystyrene layers

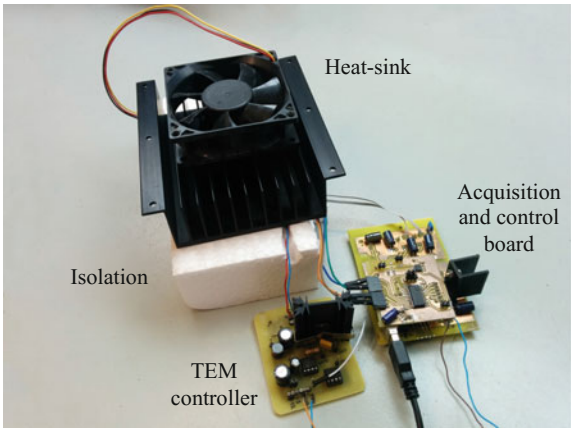

Fig. 2. Image of the apparatus and boards that constitute the acquisition and control system

3 PTAT-Based Heat-Flux Sensor

The heat-flux sensor is realized by stacking two custom designed 0.35 μm CMOS integrated microchips (Austria Micro Systems), each including a PTAT sensor [7] that offers high accuracy and high linearity in the range of our interest.

The sensor consists of a PTAT voltage generator and a differential amplifier. The output signal, proportional to absolute temperature, is obtained by using two identical diode-connected BJTs, driven by different currents.

The PTAT is biased by a MOSFET current mirror. The MOSFETs have been sized with different aspect ratios W/L (one with L = 1 μm W = 1 μm, and the other with L = 1 μm W = 10 μm) such that the diode-connected transistors are driven by two currents with a ratio equal to 10. The reference current I_{ref} of 11.5 μA is generated through an integrated bias current generator (BBIAS), a standard cell library designed to be independent from temperature and supply voltage.

The sensitivity of the PTAT is 2 mV/°C, therefore an amplifier stage has been introduced to obtain a higher voltage level that can be easily read by an ADC. A differential amplifier with active load, as current-stable nonlinear resistors, has been tuned in order to exhibit a higher small-signal impedance, compared to the use of large resistor passive loads, thus resulting in an increase of the AC gain of the amplifier. The amplified signal presents a higher sensitivity (19 mV/°C) while preserving the linearity in the range of interest (below 80 °C).

The PTAT circuit draws a current of 150 μA at 2.8 V, resulting in a very low power consumption, well below the power dissipated by the DUT. To further reduce the influence of self-heating of the PTAT sensing microchip, their functioning has been duty-cycled allowing the power-on only for the time required for the measurement.

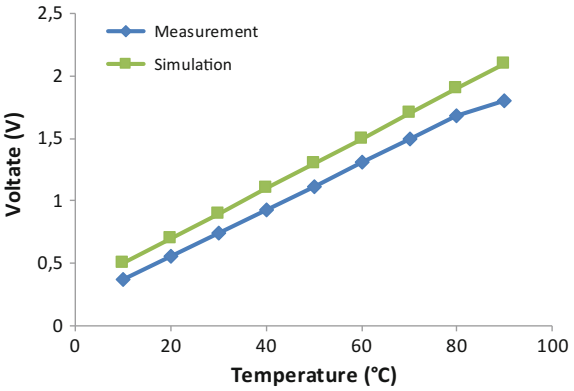

Fig. 3. Experimental and simulated characteristics of the amplified PTAT sensors chip used in this work

The output voltage versus temperature curve is shown in Fig. 3. Simulations were carried within the Cadence Virtuoso Analog Environment tool. The output signal obtained through simulations of the same circuit is provided for comparison, showing a good agreement with the results achieved from the tests on the fabricated chip.

4 Measurement and Results

Tests were done on a commercial MOSFET used as a DUT. The dissipated power is determined in two steps. A preliminary calibration is required to determine the relation between the ΔT measured across the heat-flux sensor and the power dissipated by the DUT. This step is performed operating the DUT in DC, when it is possible to measure

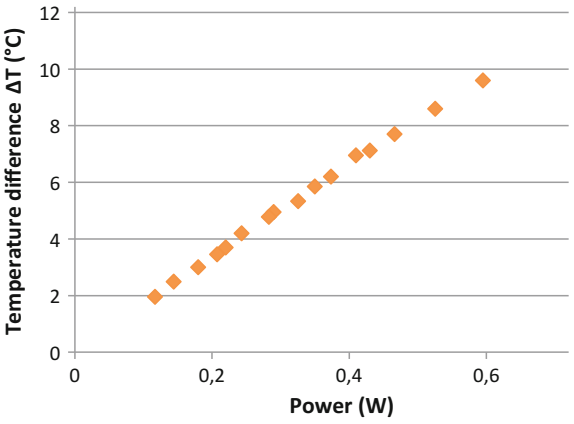

Fig. 4. Calibration curve of the apparatus that relates the temperature difference (ΔT) and power dissipated by the DUT in DC operation

the losses with high precision also with electrical methods. After the initial calibration step, the losses can be estimated on the basis of the calibration data for any arbitrary operating condition, even for highly distorted electrical signals that are difficult to acquire with traditional instruments.

The calibration was performed by biasing the MOSFET at different operating points and measuring the ΔT across the heat-flux sensor at know values of power losses. The power losses were simply calculated as the product of V_{DS} voltage and I_D current.

Figure 4 shows the calibration curve that relates the power dissipated by the transistor and the temperature difference ΔT measured with the PTAT-based heat-flux sensor.

To verify the measurement of the realized apparatus, we used a MOSFET operating at increasing frequency. The gate of the transistor was driven by a square wave at various frequencies, whereas a fixed load was connected to the drain. The losses estimated by our apparatus in such conditions were compared with the power measurement made with a 1 GHz LeCroy Wavepro digital oscilloscope. Figure 5 shows the estimated power losses compared with the oscilloscope measures.

At increasing frequencies, the difference between the two measurements increases, due to the highly distorted signals that are not correctly acquired by the oscilloscope, yielding an underestimation of the losses.

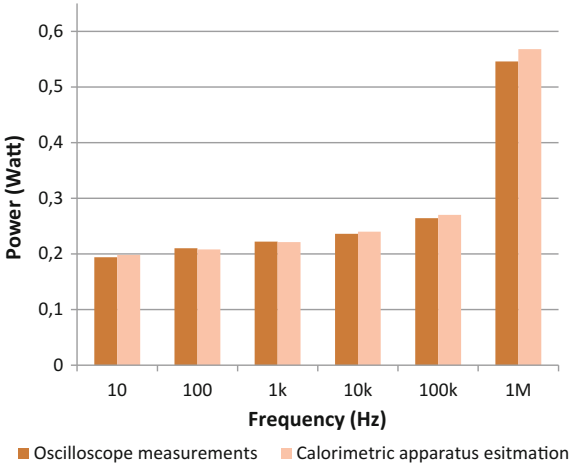

Fig. 5. Comparison between the losses estimated by our system and those measured by a digital oscilloscope at different frequencies and a fixed load

5 Conclusions

An alternative method for the measurement of the power loss in a switching device has been proposed. The set-up is based on a heat-flux sensor, a control circuit, and a thermoelectric module which absorbs the heat, and keeps the device at the same temperature of the air, thus minimizing the heat leakage.

The new heat-flux sensor is constituted of two PTAT sensor microchips used to measure the temperature difference across a substrate; this is an effective and simple solution to realize a heat-flux sensor and achieve measurements with high sensitivity (19 mV/°C) and linearity ($R^2 = 0.99962$).

The presented prototype allows to measure losses up to one watt for devices operating in dynamic repetitive conditions. However, the setup could be easily scaled for other ranges of the measurements.

The apparatus allows to overcome the problems associated with direct electrical measurements, providing reliable results also in very fast switching devices and distorted waveforms. Moreover, it is simpler than other calorimetric set-ups because it does not require the use of complex controls or a vacuum-sealed chamber.

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ZnO-rGO Composite Thin Film Resistive Switching Device: Emulating Biological Synapse Behavior

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Abstract. We have fabricated Sol-Gel synthesised Zinc Oxide (ZnO)-Reduced Graphene Oxide (rGO) on Fluorine-doped tin oxide (FTO) glass electrodes using a Dip Coating process. The Ag/ZnO-rGO/FTO sandwich structure showed bipolar resistive switching behavior. The resistive switching behavior can be attributed to the oxygen vacancies in the ZnO-rGO composite thin film giving rise to the formation and annihilation of conducting filament along the thin film. Good resistive switching (RS) characteristics with good On-OFF was also observed with good stability. The fabricated device has characteristics similar to that of biological synaptic plasticity and can be used for making electronics dynamical synapse.

Keywords: Resistive switching · Zinc oxide · Graphene oxide · ZnO-rGO · Thin film · Synapse

1 Introduction

After "Hewlett-Packard" in 2008 presented the first prototype of a new two-terminal resistive switching (RS) device using a sandwiched Pt-TiO-Pt structure [1]. Significant progress has been made in the study related to the theory, modelling, fabrication and applications of the resistive switching device. Resistive switching device apart from showing the ability to store the last resistance/conductance value after the applied voltage is taken out (i.e. non-volatile), also has an excellent ability to form crossbar array (high density), low power consumption, fast switching speed and high write-erase cycle stability [2–5]. Also, In recent years RS device has been researched for replicating plastic synapses like behaviour in neural systems. The multi-value resistance/conductance change concerning the polarity and magnitude of the applied signal and ability to store the previous resistance state are similar to the characteristic behaviour of the biological synapses [4,6,7].

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Recently ZnO-rGO based composites have generated a lot of interest for new electronics device design and fabrication because of the decent performance with less complex and suitability with current CMOS manufacturing process for the variety of electronics applications be it optoelectronic, pure electronics or photo catalytic applications [8]. In recent works [9] on the synthesis of ZnO-rGO based composites, the specific materials are prepared separately and then mixed, which has its limitation in large scale production and also is not suitable for thin film formation.

In this work we present RS device based on Sol-Gel synthesised ZnO-rGO (Zinc Oxide- Reduced Graphene Oxide) composite thin film. ZnO and GO both exhibits several advantages like excellent structural, chemical and electrical stability, wide band gap and are compatible with current CMOS fabrication processes. The fabricated device has electro forming free activation, good stability and suitability for emulating the biological synaptic behaviour.

2 Material and Method

Zinc acetate dehydrate, ethanol and ethanolamine were obtained from Sigma-Aldrich. Graphene oxide powder (1 gm) was received was from Abalonyx (Norway). All the reagents were of analytical grade and used as received. The same author has presented More detailed description of the Sol-Gel synthesis of ZnO-rGO composite film in [10].

The Ag/ZnO-rGO/FTO device structure shown in Fig. 1a. In this work, above mentioned Sol-Gel synthesised ZnO-GO solution is used to make the thin film, and after thermal annealing, GO reduce to rGO, this reduction creates free oxygen vacancies responsible for RS property of the device. The PL spectra shift in Fig. 1b signifies the reduction of Go to rGO. The as prepared ZnO-rGO thin film is used as the sandwich layer between Silver (Ag) top electrode (TE) and FTO as the bottom electrode (BE).

The FTO makes an Ohmic contact with the thin film; hence, FTO is used as the BE. We use Dip coating technique for the deposition of Sol-Gel processed and thermally annealed ZnO-rGO film onto an FTO-coated glass substrate. The continuity and thickness of the thin film are controlled by controlling the dipping and lifting speed of the dip coater and by repeating the coating process. For this work, the coating process was repeated two times to get a uniform thin film of about 100 nm. After the deposition of the thin film, the as produced device was subjected to thermal annealing at 500 °C in ambient air atmosphere.

TE for the device is a 100 nm thick Silver (Ag) with 2 mm × 2 mm active area and deposited by inkjet printing using a drop on demand Inkjet printer from Microdrop Technologies (Germany) and commercial silver nanoparticle ink from ANP co. Ltd (Korea). The piezoelectric nozzle used has 70 um diameter. The completed device was annealed at 130 °C for about 30 min to remove the residual solvents.

The operating mechanism of ZnO thin film resistive switching device is considered to be based on the formation and annihilation of the conducting path so called as filament between the TE and BE [11]. The filament is a continuous chain of free vacancies within the thin film. The free vacancies can either be created by the thermal or electrical reduction of the material or by interstitial defects present in the film. For our device thermal annealing is done for creating the vacancies. ZnO-GO both undergo reduction

at 500 °C thereby creating free oxygen vacancies, these vacancies under the effect of applied electric field create an electrical path between TE or BE (i.e. formation of the filament), by changing the polarity or and by lowering the magnitude of the applied field the state of filament could be disturbed (i.e. annihilation of the filament) Fig. 1. Also the Ag which is a well known active material improve the device performance with generating Ag ions which work as free vacancies. Previously for many of the oxide based RS devices, an extra step known as electroforming is necessary or in some case may not be particularly necessary but is used to activate the device. This is because the pristine state oxide materials have a low density of defects like vacancies or interstitials.

3 Results

The DC electrical measurement was done using a Keithley 2612 source meter with Ag as TE connected to supply and FTO as BE is connected to ground. Voltage sweep between -5 and $+5$ V was applied to the TE with step size 0.1 V and current compliance 200 mA. From Fig. 2a the pinched hysteresis I-V curve for the memristor device,

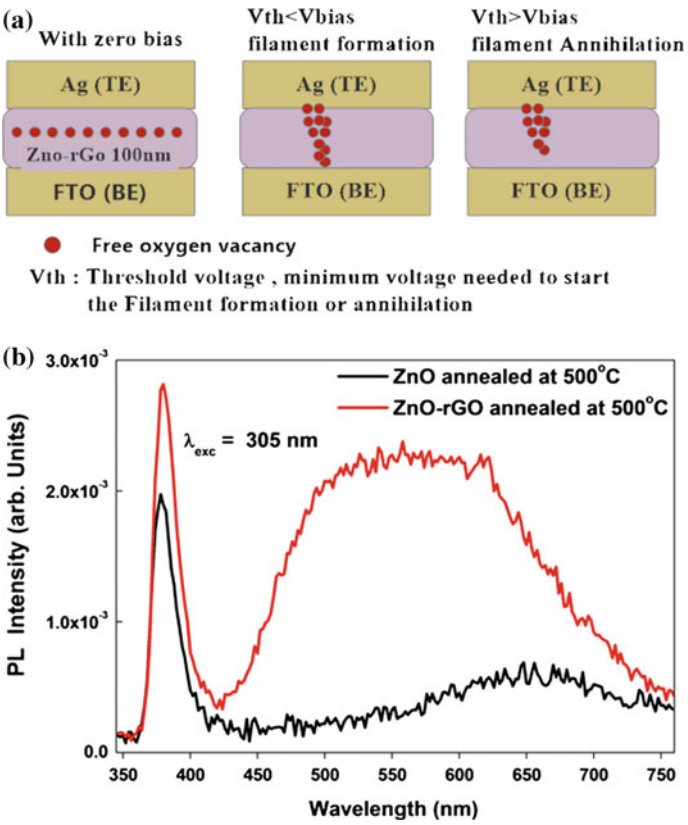

Fig. 1. a Device structure and switching dynamics, **b** PL spectra of ZnO-rGO composite

at $+3.5$ V the device has been switched to LRS and this voltage value is V_{set} of our device. Similarly, at -3.5 V device has been switched to HRS and this voltage is V_{reset} of our device. Therefore at V_{set} and V_{reset} the device switch from HRS to LRS and from LRS to HRS respectively. The R_{on} (HRS resistance) and R_{off} (LRS resistance) ratio R_{on}/R_{off} is approximately 10^2 measured at 3.5 V. Also, the device showed good

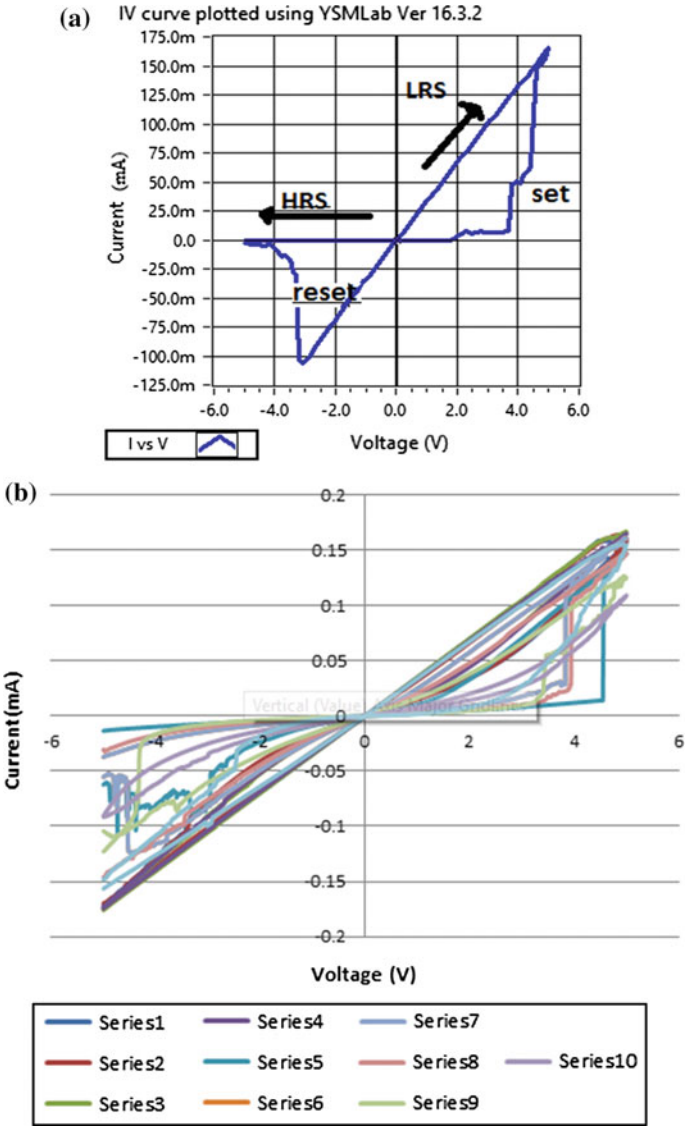

Fig. 2. a I-V curve for ZnO-rGO RS device, **b** I-V curve for ZnO-rGO RS device for 10 continuous voltage sweeps

stability after 10 continuous voltage sweeps Fig. 2b. A good On-Off Ratio and Good switching stability show that the device can be used for ReRAM and emulate synapse behaviour.

As already discussed filament formation between TE and BE make device conductive and the device is said to be in LRS; whereas as a rapture of the conduction filament makes the device highly resistive, and the device is said to be in HRS. Therefore the distance between filament and BE edge dictate the overall state of the device. By changing the polarity and or the strength of the input signal it is possible to control the effective distance between the BE and Conduction filament edge. Moreover, since the movement of the filament is based on applied field, it is possible to have multiple resistive states based on the distance of the filament and BE edge.

Variations in memristor pinched hysteresis loop with the frequency of input signal is well-understood phenomena [11, 12]. It has been noted in another experiment by the authors that also the delay time and NPLC (number of power line cycles) of the source meter can also affect the I-V characteristics of the device because scan rate can be changed by changing either delay time or NPLC [13].

4 Application: Emulating Biological Synaptic Behavior

Spiking neural networks emulate the biological neural systems accurately, as described in [14]. The transmission between two or more neuron is allowed by synapses. We use the analogy presented in literature [15] that a particular internal resistance value of memristor correspond to a particular internal state of synapses. Similar to memristor where the memristance change depends on the previously passed value of current or voltage, the internal state of the synapse depends on the strength of the previously passed neuron spike. The possibility of state modulation concerning applied signal and the ability to store the last state value even after supply is taken out make memristor a suitable candidate for emulating the synapse behaviour. As can be seen from the From Fig. 3 ZnO-rGO based RS device present characteristics similar to biological plastic synapses behaviour based on symmetric Hebbian learning rule. Here we would like to mention that the results are based on reading the conductance state of the device at different voltage and plotting it with respect to time. Same Authors have also developed in PSpice as well as in PCB a circuit to imitate the biological neuron model that drive the memristor (As synapses) to obtain Spike Time Dependence Behavior, Pspice model of said circuit is described in [16] and PCB prototype have been explained in another paper currently under review.

5 Conclusion

In this work, we have introduced a low-cost Sol-Gel prepared ZnO-rGO thin film resistive switching device. The new device is forming free and show good On-Off ratio with repeatability. Also it has been demonstrated that the I-V behavior of the device is similar to the behavior of a biological synapse. One issue with the presented ZnO-rGO RS device is high current around 150 mA at relative low voltage around 4 V, this could attribute to top electrode metal and contact area. Further study has been planned

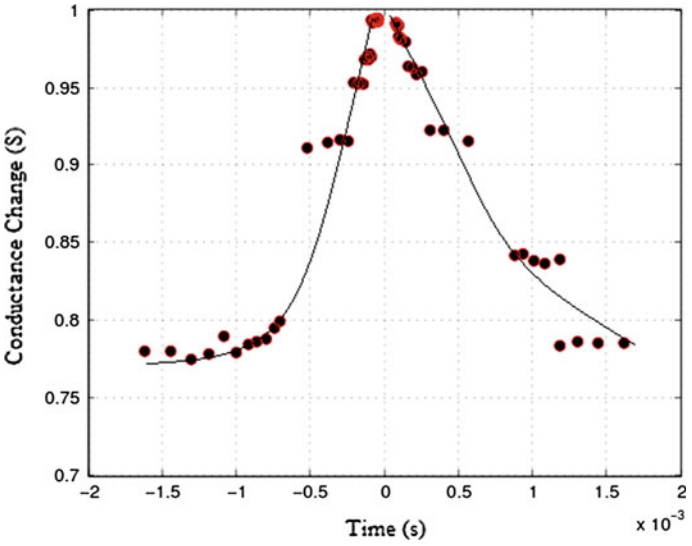

Fig. 3. Synapses behavior based on symmetric Hebbian learning rule

in order to characterize the device with different top electrode material and area. Also, fabrication of 4×4 cross bar array of the ZnO-rGO resistive switch is underway for developing more memristor/restive switch based applications.

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Embedded System for Prosthetic Interface Mapping of Lower Limbs Amputees

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Abstract. The realization of lower limb prosthesis is mainly a handmade job. Even if today machines and computer aided design can speed-up the process, the residual limb modification in time requires a fine tuning of the socket that is done manually by artisans. In this work we present an embedded system designed to map the stress in the contact points between lower limb amputees and the prosthesis socket. The wearable system interfaces a matrix of 32 force sensors hosted by a flexible substrate. Data are collected in real-time and streamed wirelessly during normal daily activities, to provide a complete set of information to shape a prosthetic interface tailored to the patient. An aggressive power management allows the system to be autonomous for a full working day with high accuracy of the multiple data acquisition.

Keywords: Force mapping · Embedded systems · Lower limb prosthesis · IoT-ready · Battery powered

1 Introduction

Limb loss and amputations have different causes, like vascular disease (including diabetes and peripheral arterial disease), trauma, infection and cancer. The number of people that experienced a limb loss in U.S. is nearly 2 M, more than 500 per day, as reported by the leading U.S. organizations on limb loss and disease prevention [1–3]. The process of prosthesis fabrication is, still today, mainly a handmade job done by experienced artisans with long time required and high costs. The innovations introduced in this field by 3D scanners and CAD/CAM machines [4], ease the work of prosthetists to acquire high resolution images of the limb and to realize customized sockets in less than one hour (e.g. Fig. 1). Unfortunately, the prototype socket must be further adjusted (by hand) according to patients needs before being comfortable, and eventually replaced with a

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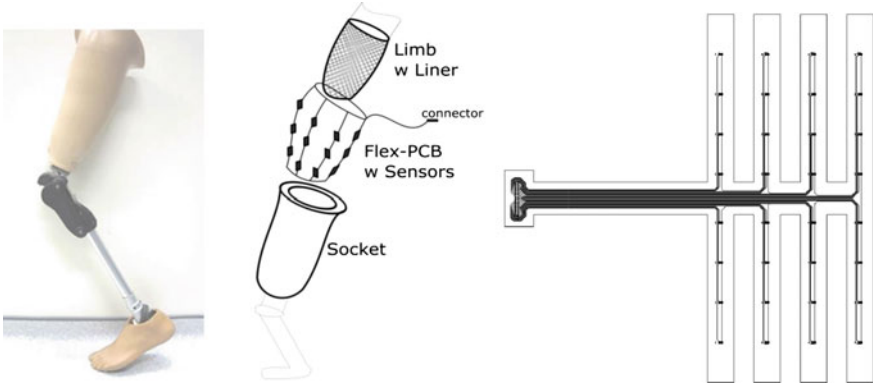

Fig. 1. Lower limb prosthesis example (*left* [14]), force mapping implant schematics (*middle*) and flexible sensor support design (*right*)

new one every few months (usually twice a year). To overcome the limitation of the current technology and reduce patients pain and stress, different solutions have been proposed to monitor the health and the modification in time of the anatomical profile of the residual limb. These researches highlight how the continuous monitoring of parameters such as the shear stress and normal pressure interaction between the limb and the socket plays an important role to ease the customization process done by prosthetists [5].

In this work is presented the design of a wearable embedded system with wireless communication interface that includes a modular and flexible support for up to 32 force sensors, designed for integration into prosthesis's socket. In particular, main contributions are (i) the design of the flexible substrate hosting sensors, (ii) the design of the modular and battery powered embedded system with up to 8 h of energy autonomy, (iii) the design of the digitally controlled analog frontend for the readout of the 32 force sensors with tunable sampling rate (up to 62.5 ksps), and, finally (iv) the integration of multiple output interfaces for local data logging and/or wireless streaming through secure Wi-Fi channel. Furthermore, the proposed system features are extreme low cost and large flexibility, thanks to the modular design and the powerful microcontroller included, and real-time feedback from the sensors.

In the following, Sect. 2 presents the review of related works in prosthetic interface design, while Sect. 3 presents the proposed low power design. Section 4 presents the performance evaluation of sensors readout section and overall energy consumption. Finally, Sect. 5 sums up the conclusion of the work.

2 State of the Art

Prosthesis are recently registered fast-paced improvements till the recent implementation with sensors and actuators [6,7]. However, one of the main problems dealing with any type of prosthesis's socket design, is related with the modifications that naturally occur to the residual limb through time. In this application, it is necessary to replicate the anatomical profile of the limb and to further adjust its shape to make the prosthesis comfortable during daily activities, when user is standing and walking [8]. According to

medical reviews in this field (e.g. [9,10]), force distribution and magnitude are the most important parameters to track during the execution of different tasks, to understand and map the stress between the residual limb and the socket that is used to fit the prosthesis firmly and correctly. Most of the research in this field is related to the development of new sensing instruments, with modern low cost 3D printing technologies [11] or traditional micromachining ones [12]: smart sensors with embedded readout electronics and digital interface, meant to reduce fabrication costs and ease the integration inside prosthetic sockets. Unfortunately, sensors encapsulated into rigid sockets are not easy to replace or fix in case of failures.

Recently, solutions developed by the robotic community have been considered promising to be integrated into prosthesis sockets thanks to the intrinsic flexibility, sensitivity and spatial resolution provided [13]. Moreover, synthetic skin makes possible to fit the sensing layer in between the rigid socket and the liner (the tissue that a patient must wear to allow vacuum lock). To the best of our knowledge, the missing part both in the literature and in the market, is an interface system able to readout, log and communicate sensors readings to the user and to specialists, that is affordable and can be worn by patients during daily activities.

3 Sensing Interface Design

The readout system has been developed with a modular design to maximize flexibility, adaptability and customization, to make it suitable for different working conditions. It consists of three modules, (i) the flexible sensor substrate, (ii) the analog frontend and (iii) the MCU controller board.

The flexible sensor support, shown in Fig. 1 right, has been shaped to allow the fitting and the contact of sensors with the residual limb. It hosts up to 32 passive force sensors with dedicated readout routes and common ground, to enable the single sensor tuning and readout. It is suitable for different sensing technologies, like piezoresistive and/or piezoelectric, that can potentially be used at the same time, since conditioning and supply are managed by the readout board. Routes and sensor's socket are realized on a single 50 μm kapton foil, with relative distance of 4.5 cm between sensors in line and 8 cm spacing between sensing fingers (for a total occupancy of $\approx 46 \times 46$ cm). A single 34 channel connector (32 signals and 2 shared ground signals for reference) provides interface with the other modules.

The conditioning unit depends on the kind of sensor included in the design. For example, piezoresistive sensors require a basic amplification stage made with a non-inverting amplifier, and thanks to their stationary response can be readout with a low speed analog to digital converter. Piezoelectric devices, on the other side, exhibit a dynamic response proportional to the applied force, they require a charge amplifiers and a high speed ADC (w.r.t. the previous ones) to precisely detect the instant and the amplitude of each stimulus. To accommodate both sensing technologies we designed a digitally controlled—analog conditioning circuitry which implements 32 parallel amplification stages that can be accessed individually by means of multiplexers. This multiplexed acquisition has been exhaustively tested in a previous version [15] and has been arranged in two separate boards with 16 channels each and enables single sensor tuning.

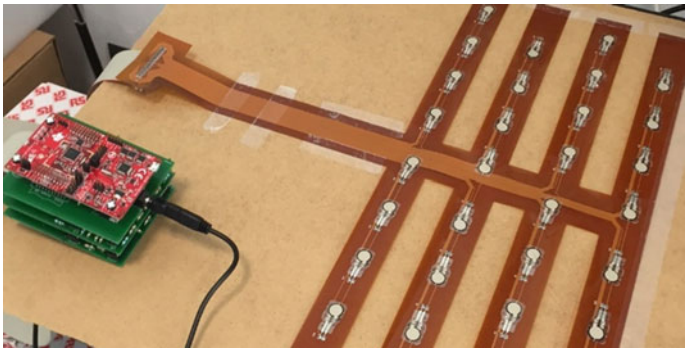

Fig. 2. The prototype system developed with the Launchpad CC3200 MCU board on top (*left*) and the flexible substrate with sensors (*right*)

In this way, a single acquisitions system can be used for different sensing technologies by simply changing one layer of the system. From the point of view of data rate, the payload can be further reduced by applying recent compression techniques as presented in [16].

The core of the system has been developed on top of the low-power CC3200 microcontroller from Texas Instruments, which is the first commercial SoC that integrates a low-power MCU with a Wi-Fi radio. This SoC provides an ARM M3 core for user applications and an ARM M0 core dedicated to the Wi-Fi network stack. It provides standard digital communication interfaces and an 8-channels SAR ADC (only 4 available for user application with fixed sampling rate of 62.5 ksps while the remaining are internally managed by the Wi-Fi stack). Figure 2 depicts the complete prototype realized and used to collect the results presented in the following. The prototype is arranged in 4 layers, the MCU, two analog frontend and, finally, the power delivery subsystem that provides separated 5 V and 3.3 V for analog and digital sections respectively. The detailed block scheme is presented in Fig. 3, with colors indicating layers.

4 Results

We developed a complete prototype for testing purposes, a selection of results is presented in Figs. 4, 5 and 6. In these tests, we selected commercial piezoresistive force sensors (Tekscan A301, 4 N range) and customized the readout sensing board to interface these devices.

For the sake of completeness we realized a graphical user interface (Fig. 4, in Matlab environment) to collect samples and perform offline analysis.

Figure 5 presents a selection of the output obtained during the characterization of the prototype. Results show that few samples are required to stabilize the response and each sensor must be tuned and characterized individually, in fact the absolute response differs for each sensor. However, they also exhibit a standard deviation in the range of 2–30 mV (with an average of 10 mV among the 32 sensors) in response to a repeated stimulus using a 50 g weight (corresponding to $\approx$0.5 N). Overall, we observe that the

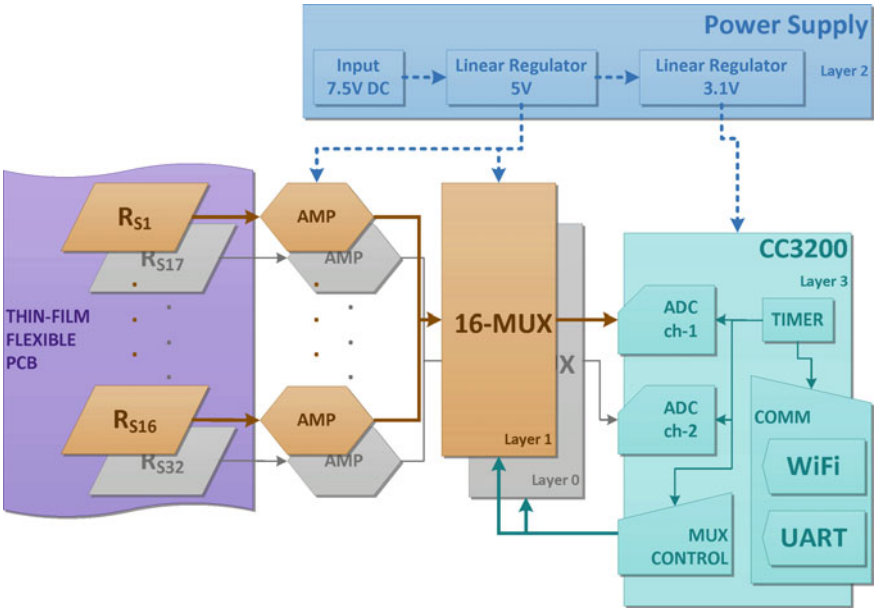

Fig. 3. Block diagram of the multi-sensor readout design

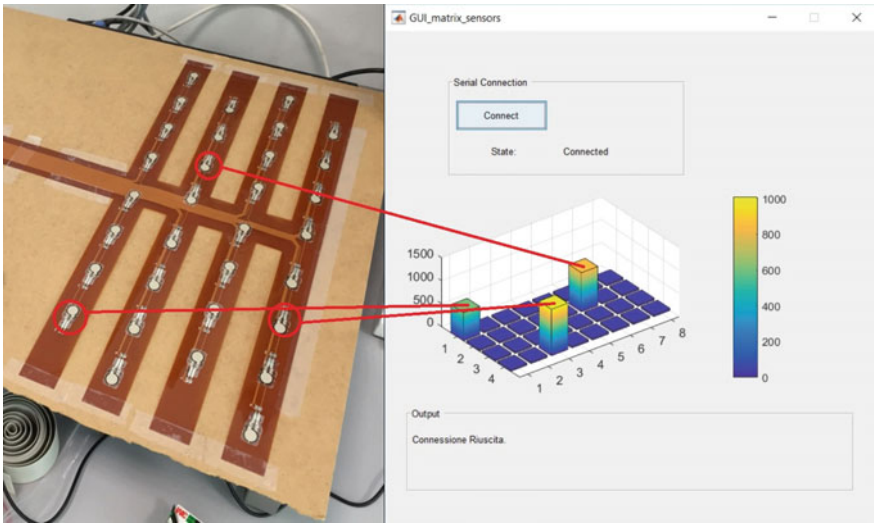

Fig. 4. Setup for the characterization of piezoresistive sensor response

system is able to precisely map and detect multiple stimuli at the same time thanks to the very reduced response deviation, but an improvement of manufacturing and assembling is required to reduce the difference among channels.

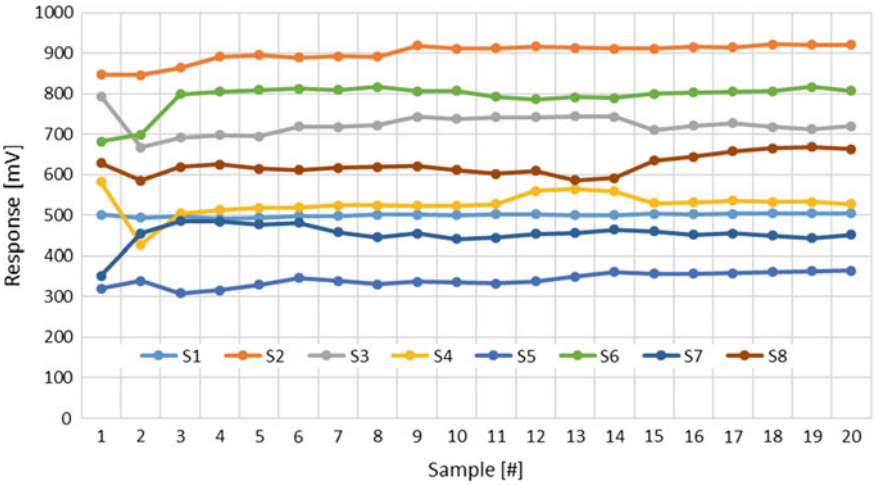

Fig. 5. Piezoresistive sensor response in time with 0.5 N

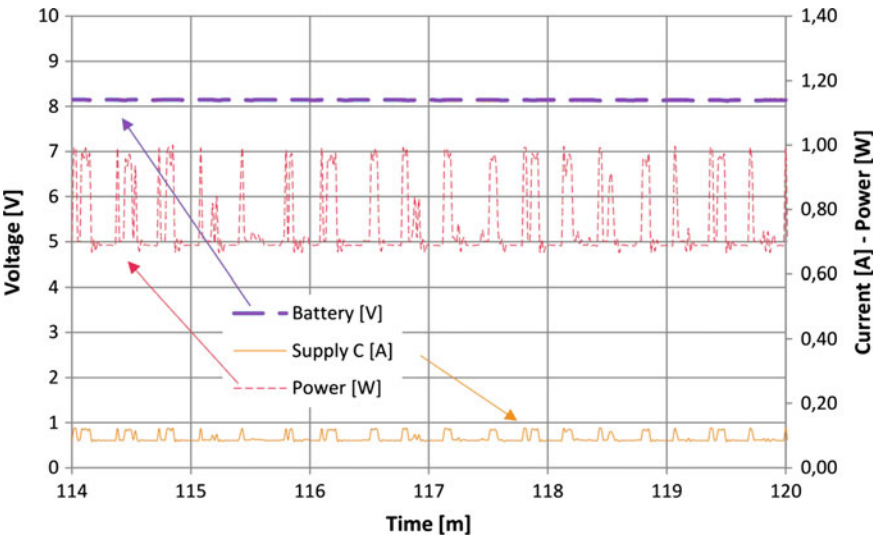

Fig. 6. Prototype power consumption and other electrical parameters when battery supplied

In the last presented test, we evaluated the power consumption with battery supply which is in average 750 mW (Fig. 6), providing up to 8 h of autonomy with a 7.5 V, 2.2 Ah, lithium-ion battery pack. As a conclusion we can say that the system exhibits negligible cross correlation and good response with very small stimulus (in the range 0–400 g).

5 Conclusions

We presented a wearable embedded system designed to map the contact stress of lower limb amputees with the prosthesis interface. The system exploits a flexible substrate to fit a matrix of 32 force sensors in contact with the residual limb, to monitor patients daily activities unobtrusively. The real-time parallel readout and wireless streaming of readout data complete the rich set of features provided by the system. Moreover, the modular design is suitable for different sensing technologies to be embedded and interfaced with the microcontroller unit. The power management implemented achieves 8 h autonomy on a lithium battery.

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Wideband mmWave Antenna for Wireless Network-On-Chip/Network-On-Board Communications

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Abstract. Wireless network-on-chip (WiNoC) and network-on-board (WiNoB) are new paradigms, which allow Gb/s communication among processing cores and/or memories integrated in the same system-on-chip or in the same electronic board. This work presents the design of an antenna, operating at mm-waves (mmW), which can be printed on-board or on-chip using the top metal layer. The antenna is characterized from 50 to 100 GHz. When compared to the state-of-the-art the antenna stands for its better trade-off between bandwidth, gain, size and beamwidth.

Keywords: Wireless communications · Printed circuit boards (PCB) · Radio frequency (RF) electronics

1 Introduction

The increased complexity of multi-core computing systems, implemented on-chip or on printed circuit board (PCB), has forced the evolution from standard circuit-switched bus connections to packet-switched network-on-chip (NoC) or Network-on-Board (NoB) solutions [1–10]. At physical layer, standard metal-wired links suffer of poor scalability and increased delay when transferring high data rates, several Gb/s, among cores and/or memories placed at distances higher than 1 cm [3]. This is the case of different chips on a PCB, or different cores placed at the opposite sides of a big chip.

Optical [3] or wireless (WiNoC/WiNoB) [1–4, 11] links are investigated in literature as an alternative solution, the latter being easier to integrate by printing the antennas on chip or on the PCB using top metal layers. Since the antenna design and integration is the key issue of WiNoC and WiNoB systems, this work presents the design of a mm-wave (mmW) antenna, allowing for a compact size implementation and large covered spectrum range.

The rest of the paper is organized as follows. Section 2 presents the antenna topology. Section 3 discusses the antenna layout and its performance characterization. Section 4 presents a comparison to state-of-the-art. Section 5 draws some conclusions.

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2 Antenna Topology

As operating frequency, we selected mmW above 50 GHz. Today, transceivers operating at such frequencies can be designed using low-cost/low-power CMOS technologies [12, 13]. The wavelength is few millimeters and this helps reducing transceiver and antenna size versus designs operating below 10 GHz, such as [2, 11]. A common mmW frequency is 60 GHz, adopted in high-rate communications (WiGiG or Wireless HD alliances) due to the availability of a large unlicensed spectrum from 57 to 66 GHz. However, cm-range communications in WiNoC or WiNoB scenario do not have licensing problems being spatial self-contained. New CMOS SOI (Silicon on Insulator) technologies allow operating also at 100 GHz. Targeting a wide band antenna design, easily to scale in terms of operating frequency from 50 to 100 GHz we selected a bow-tie topology. Differently from classic antennas such as half- or quarter-wave ones, where the size depends on the wavelength and hence they are frequency-specific, the bow-tie antenna is specified by angles.

Figure 1 shows the layout of the antenna. For the implementation, we considered both on-chip realization in 65 nm SOI technology, and on-board realization using PCB copper layer on RO4003 substrate. In the on-chip realization a 0.9 μm copper layer is printed on a multi-layer substrate made up of 2.76 μm thick layer with dielectric permittivity $\varepsilon r = 3.5$, 0.15 μm of buried oxide with $\varepsilon r = 4$, and a 350 μm thick high-resistivity substrate ($\rho = 5$ kΩ·cm, $\varepsilon r = 11.7$). The antenna feed is realized through a Co-Planar Strip-line (CPS). The worst case is the integration on-chip since the PCB uses thicker copper layer to print the antenna (e.g. 17 μm) on a RO4003 substrate, which has better behaviour at high frequency ($\varepsilon r = 3.48$, thickness from minimum 0.203 to 1.524 mm). Since the worst-case is the on-chip antenna, then the performance results in this work refer to this case.

After several trade-offs carried out in the Ansys HFSS (High Frequency Structural Simulator) environment, in Fig. 1 the angle α has been sized at 24°, whereas the parameters L_bowtie, W and L_CPS are 0.32 mm, 65 μm and 0.64 mm respectively. The width of the CPS is 12 μm, whereas the gap among the two strip-lines is 1.2 μm.

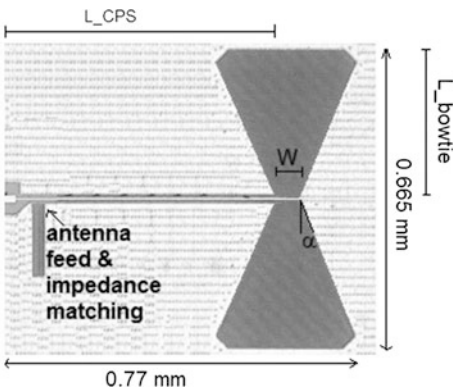

Fig. 1. Antenna layout in 65 nm CMOS SOI

The area of the rectangle including the antenna is 0.512 mm^2, much lower than the cm^2 antennas used in [2, 11]. This sizing is not valid only for a specific frequency, but the same antenna has been characterized in a wide frequency range. The real area occupation of the antenna should consider that other active or passive circuits can not be placed in the near reactive-field region of the radiating structure. This imposes a distance from the antenna structure of at least $\lambda/2\pi$, about 400 μm at 60 GHz. Thus, the area that is no more available for other circuits is 1.17×1.465 $mm^2 \sim 1.7$ mm^2.

It is worth noting in the layout of Fig. 1 some modifications versus ideal layouts proposed in literature:

(i) the passive circuitry for antenna feeding;
(ii) the corners of the bow-tie that have been rounded to avoid charge accumulation.

3 Antenna Performance

Figure 2 shows, for the antenna whose layout is in Fig. 1, the projection of the 3D radiation pattern along the X-Y plane and the X-Z plane, and the relevant half-power beamwidth (HPBW) angles.

Table 1 shows the main antenna performance at 60 GHz in terms of S-parameters, maximum gain (S21) and minimum return loss (S11), % radiation efficiency η, HPBW angles along the X-Y and X-Z planes. The antenna bandwidth in literature is calculated as the frequency range where S11 is below −10 dB. Figure 3 shows the S11 antenna performance versus frequency. From Fig. 3, in the range 51–100 GHz the return loss is always below −10 dB.

For WiNoC and WiNoB applications where a processing core has to be connected with another core or memory placed on the same plane, the radiated power of interest is that along the X-Y plane. The power radiated along the Z-axis is just wasted, unless a

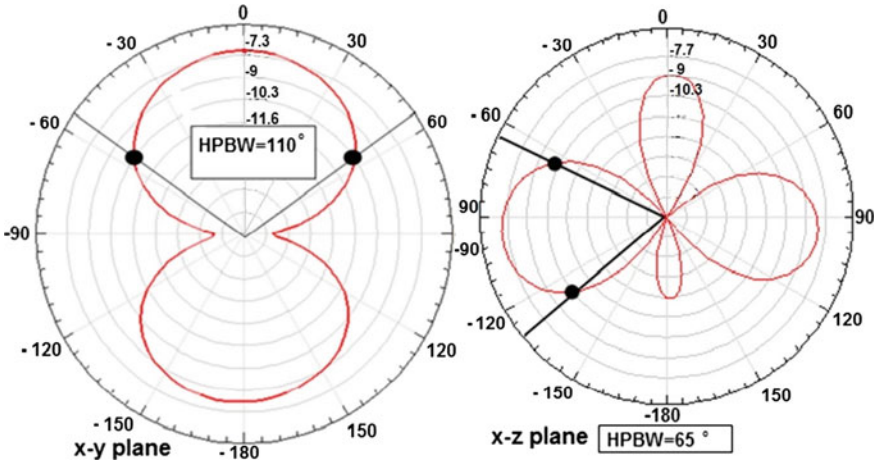

Fig. 2. Antenna radiation pattern at 60 GHz

Table 1. Antenna parameters at 60 GHz

S11 min	S21 max	HPBWxy	HPBWyz	η
−39 dB	−7.3 dB	110°	65°	20%

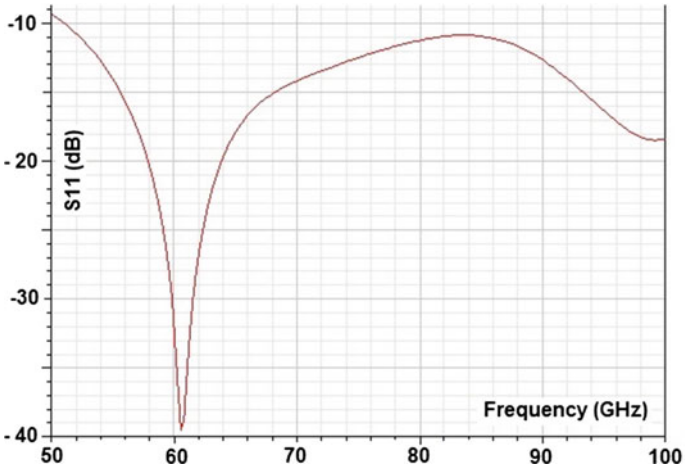

Fig. 3. Return loss (S11) of the antenna as a function of frequency

3D assembly technology is used and the wireless link is between cores aligned in vertical direction.

4 Comparison to the State-of-the-Art

Table 2 compares the achieved performance versus the state-of-the-art.

With respect to antennas in the sub −10 GHz domain [2, 11] the area occupation of our design is limited to 0.512 mm^2, a value compliant with both on-chip and on-board integration. Instead, in [2, 11] the size is orders of magnitude higher. More in detail, [2] proposes a 3 cm^2 dipole antenna with a 2.8 dB gain and 85° HPBW at 10 GHz and a 3.75 cm^2 Vivaldi antenna with a gain of 5.8 dBi and a HPBW of 65° at 10 GHz.

With respect to other 60 GHz on-chip antennas proposed in literature, our design allows for a better trade-off between size, gain, bandwidth and HPBW. For example, the zig-zag antenna adopted for WiNoC in [3] has been designed with 10 μm trace width, 60 μm arm length and 30° bend angle, an axial length of 0.38 mm. In [3] the substrate is represented by a 2 μm thick SiO_2 layer, $\varepsilon r = 3.9$, and 633 μm of high-resistivity silicon substrate with $\rho = 5$ kΩ·cm, $\varepsilon r = 11.7$. The same antenna has been adopted also in [1]. The zig-zag antenna has a lower size, 60 μm × 380 μm (without considering the feeding and impedance matching network) but its maximum gain is only −26.8 dB at 60 GHz (19.5 dB lower than our design), which limits the connections distance to 20 mm [3]. The return loss (S11) for the zig-zag antenna is below −10 dB only from 51 to 66 GHz, whereas our antenna has no upper bound limit

Table 2. Comparison to the state-of-art

Antenna	Size, mm^2	Gain, dB	HPBWxy	Bandwidth
This work	0.512	−7.3 @ 60 GHz	110°	51–100 GHz
[1, 3]	*0.023	−26.5 @ 60 GHz	60°	51–66 GHz
[2], Dipole	375	5.8 @ 10 GHz	65°	8–11 GHz
[2], Vivaldi	300	2.8 @10 GHz	85°	9–11 GHz
[4]	156	5 @ 60 GHz	184°	57–64 GHz

* without feed/matching circuit

(it has been characterized up to 100 GHz). In terms of HPBW, along the X-Y plane of interest, the zig-zag antenna has a value of about 60°, almost halved versus the 110° of our design in Fig. 2. A lower HPBW leads to a lower number of cores that can be reached by the WiNoC. The half-wave dipole and the double-slot antennas proposed in 65 nm SOI technologies in [13], having a comparable size to the bow-tie design, reach a positive gain of few dB, but using a PEC plane under the chip. Similarly, the slot bow-tie antenna in [14] has an area 2.5 times higher than the proposed design. Realized in 180 nm SiGe technology, and using a PEC layer under the substrate, [14] achieves a gain from −3 to 0 dB operating from 70 to 110 GHz. However, for the antennas in [13, 14] the radiation pattern is directed along the Z-axis, which is unsuitable for WiNoC applications where the communication is towards co-planar nodes. High gain antennas have been proposed at 60 GHz such as the Fan-Like antenna in [4]. The antenna in [4] exhibits a beamwidth of 184°, a gain varying from 1.6 to 6.4 dB from 57 to 64 GHz, but for an area of 156 mm^2 which is orders of magnitude higher than our proposed design.

5 Conclusions

This work has presented the design of a mmW antenna to enable wideband wireless communications on chip, WiNoC, to interconnect multiple macrocells [1–10, 15], or in a single PCB board, WiNoB, to interconnect multiple chip. The antenna has been characterized in the range from 50 to 100 GHz. With respect to the state-of-the-art, the antenna stands for a better trade-off in terms of size, gain, HPBW and bandwidth.

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Failure Effect Analysis of Patch-Clamp Electronic Instrumentation in Electrophysiology Experiments

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Abstract. The patch-clamp technique is an extremely powerful and exquisitely sensitive means for studying the biophysics and pharmacology of ion channels. Aiming at acquiring ionic currents, in the range from few pA to nA, while controlling the voltage across the membrane of a biological cell and continuously perfusing physiological solutions containing the molecules under investigation, patch-clamp measurements require: an accurate calibration phase, a low noise front-end, and a temperature control. After describing a patch-clamp electronic system, the paper discusses the most frequently encountered and well-fitting examples of how failures in the electronic instrumentation are related to errors and/or accuracy degradation in the electrophysiological measurement. The paper refers to experimental data recorded with this technique under the whole-cell voltage-clamp configuration.

Keywords: Biomedical measurements · Biomedical electronics · Electrophysiology · Patch clamp · Failure Mode and Effect Analysis (FMEA)

1 Introduction

Evaluation of the effects of drugs on ion channels, central in signalling pathways controlling various biological functions, is fundamental to get the best clues of drug mechanism of action. The patch-clamp technique represents the gold standard assay for ion current recordings [1–4]. In fact, it allows direct recording of currents from functional channels, embedded in their physiological environment. The basic concept of this technique associates a living cell to an electrical circuit, the number and permeability of ion channels representing conductance, while cell membrane phospholipids represent capacitance. Generally, cells, either isolated from fresh tissue or cultured, are placed in a cell chamber and perfused with a physiological salt solution. As shown in Fig. 1a, they are patched with a thin glass pipette filled with a conducting solution in contact with a recording electrode, connected with a low-noise, feedback amplifier. Under the right experimental conditions, the pipette will form a GΩ seal with

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the cell membrane, thus allowing the recording of the ion current through different channels with different recording configurations. These measurements need a long, preliminary calibration as well as a pivotal acquisition phase. It is of interest to understand how a failure in the electronic equipment may affect current recordings in order to: (1) properly interpret the data acquired; (2) improve the equipment auto diagnostic tools and allow on-line prediction of malfunctioning; (3) find a way to analyse recordings although affected by artifacts. To this end, it is important to associate the effects on experimental data acquisition of some failures in the patch clamp electronic instrumentation. This analysis is of particular interest given the trend towards fully automatic patch clamp measurements performed by robots [2, 3]. Hereafter, Sect. 2 presents the instrumentation and the main operational phases (calibration, acquisition, data analysis) of a real voltage clamp experiment. Section 3 analyzes three more frequently encountered causes of degradation in the electronic system. First, we discuss the degradation of the Peltier cell used to control the temperature of the input channel in order to have a cooled and hence a low-noise amplification of the acquired cell signal. Then we discuss the coupling of Electromagnetic interference (EMI), between the sensing analog front-end and spike noise sources, such as switching power supplies or the motorized pump injecting the physiological liquid with the molecule under test. Finally, the degradation of the pipette and electrode impedance compensating circuit [4] is analyzed. Section 4 shows, from real-world electro-physiological experiments, the effect of the above degradation on acquired traces. Section 5 draws some conclusions.

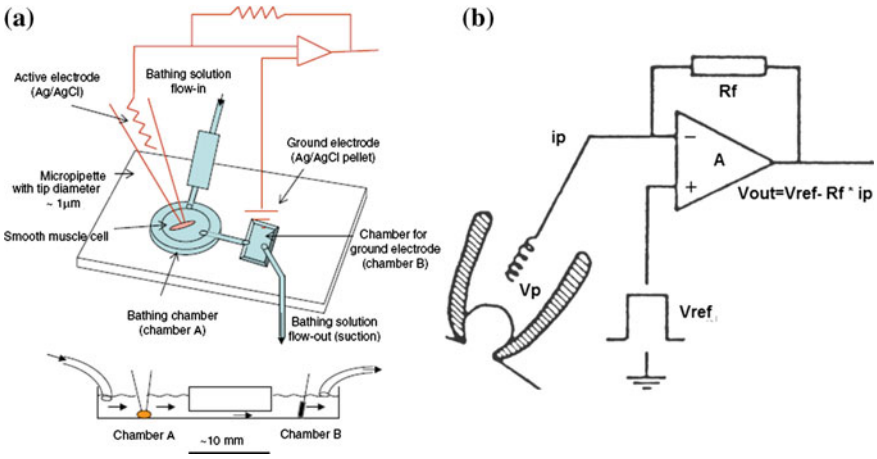

Fig. 1. **a** Patch clamp experiment; **b** measuring amplifier

2 The Patch-Clamp Technique: System and Experiments

The patch-clamp technique, see Fig. 1 refers to both voltage- and current-clamp measurements. In a voltage-clamp experiment, the most widely used, one controls the membrane voltage and measures the transmembrane current required to maintain that voltage. By holding the membrane potential constant (or at the very least, constant after a rapid step), the measured current is directly related to the conductance through ionic channels. By this method, a specific transmembrane voltage difference is maintained with a feedback circuit using very fast, low-noise differential amplifiers. In brief, as the pipette tip is approaching the cell, a low-voltage square wave is applied to the pipette electrode, allowing the monitoring of seal resistance (Fig. 2).

When the tip comes in contact with the cell surface, the current decreases and application of a gentle suction will lead to the formation of a GΩ-seal, which is signalled by a sudden increase in resistance with virtually no current recorded. At this stage, application of "pipette capacitance compensation" allows adjustment of undesired transients. Then, membrane patch is ruptured by applying a pulse of suction through the patch pipette, thereby creating a hole in the plasma membrane to gain access to the cell interior (whole-cell configuration). At this stage, "whole cell parameters" compensation allows the evaluation of both whole cell capacitance and series resistance. It is now possible to record ion currents, isolated by placing certain ions as well as specific blockers or stimulators in the pipette and/or bath solution, by setting a fixed holding potential, or by applying well-designed voltage protocols. Drugs are then assessed by adding known concentrations to a reservoir containing the physiological solution, which is perfused through the cell chamber by means of a peristaltic pump. Data presented here refer to voltage-dependent Ca^{2+} currents recorded in single myocytes isolated from the rat tail main artery cells [5]. A peristaltic pump (LKB 2132), at a flow rate of 400 μl/min, was used. The conventional whole-cell

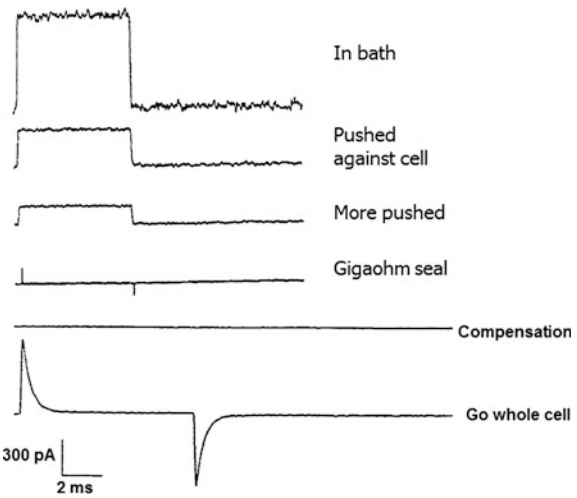

Fig. 2. Waveforms during the initial calibration phase

patch-clamp method [6] was employed to voltage-clamp smooth muscle cells. Recording electrodes were pulled from borosilicate glass capillaries (WPI) and fire-polished to obtain a pipette resistance of 2–5 MΩ when filled with internal solution. An Axopatch 200B patch-clamp amplifier, equipped with an actively cooled CV 203BU capacitor feedback headstage [7], was used to generate and apply voltage pulses to the clamped cells and record the corresponding membrane currents. At the beginning of each experiment, the junction potential between the pipette and bath solution was electronically adjusted to zero. Current signals were low-pass filtered at 1 kHz and digitized at 3 kHz prior to being stored on the computer hard disk. Electrophysiological responses were assessed at room temperature (20–22 °C). L-type Ba^{2+} current ($I_{Ba(L)}$) was always recorded in external solution containing 30 mM tetraethylammonium and 5 mM Ba^{2+}. Current was elicited with 250 ms clamp pulses (0.067 Hz) to 10 mV from a V_h of −80 mV.

3 Electronic System Degradation Analysis

This Section analyzes three main causes of degradation in the electronic system occurred/detected during standard experiments in an ion channel pharmacology laboratory. First, a Peltier cell is used to lower the temperature of the headstage thus having a low-noise amplification of the acquired cell signal. Indeed, according to Friis'formula, the noise of the first amplification stage determines the noise of the whole acquisition channel. When the Peltier cell is not working, the headstage temperature T_{head} raises from 253 K to about 290–293 K. The variation of about 40 K will cause an increase in the background thermal noise power (modeled as a white Gaussian noise whose root-mean-square power is proportional to $B_f \cdot k_B \cdot T_{head}$, being k_B the Boltzmann' constant, 1.38×10^{-23} J/K, and B_f the bandwidth of the low-pass filter) of about 16%.

Another source of noise is caused by non-properly shielded EMI from switching power supplies and/or electric motors, such as that of the peristaltic pump continuously injecting the physiological liquid into the bath with the cell under test. Finally, another main source of error is the degradation of the impedance compensating circuit. Due to this degradation, in Fig. 2 the spikes after the GΩ-seal are not canceled and they will appear in the acquired traces, thereby reducing the capability to detect small ionic currents.

4 Experimental Results

Figures 3 and 4 show a trace acquired from an actual voltage-clamp experiment when measuring Ca^{2+} ion channels and the relevant background noise, which limits the measurement sensitivity to ionic current events of ±5 pA. When the Peltier cell is working the background noise is limited within ±4 pA. One measure of particular interest is that of the peak current, whose dynamic range in Fig. 3 is about 60 pA.

Figure 5 shows the effects of the interference coupling due to the peristaltic pump motor, when applying a depolarization step to the cell membrane from −80 to 10 mV,

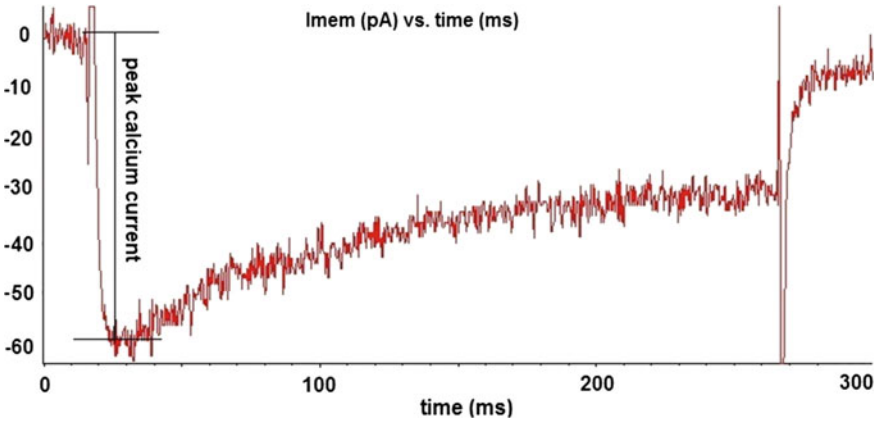

Fig. 3. Calcium current trace recorded in a whole-cell patch-clamp experiment

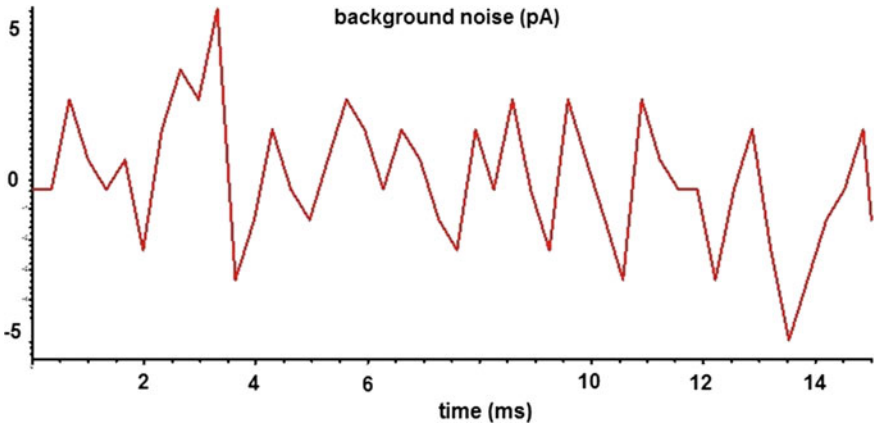

Fig. 4. Background noise when the Peltier cell is not working

then clamping the membrane voltage at +10 mV for about 250 ms, and finally coming back to the initial −80 mV membrane voltage. This voltage stimulus allows the activation of voltage-dependent ionic channels. In Fig. 5 two experiments are reported, using (B) or not (A) nifedipine, an L-type calcium channel blocker. The blocking effect can be noticed from the fact that in experiment B the dynamic range of the ionic current, apart the interference spikes, is limited between 0 and −30 pA, whereas in case A the dynamic range is from 0 and −70 pA. For each experiment, A or B, it is worth noting the interference due to spikes with a dynamic range up to 90 pA and with a random repetition in time. To be noted that in Fig. 5, for both A and B traces, the measurement of the peak calcium current parameter is not possible due to the spikes superimposed on the curve minimum, i.e. during the time slot when the channel activation ends and the channel inactivation phase starts.

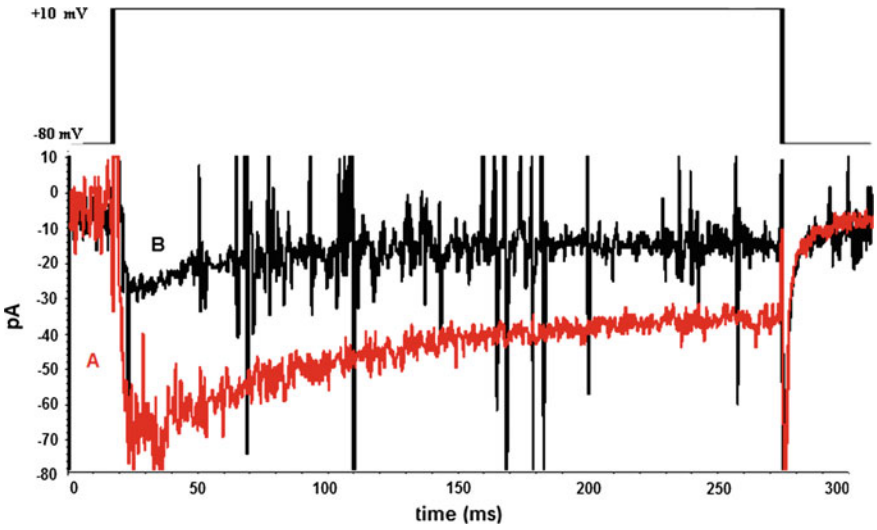

Fig. 5. Effects of the coupling interference due to peristaltic pump motor

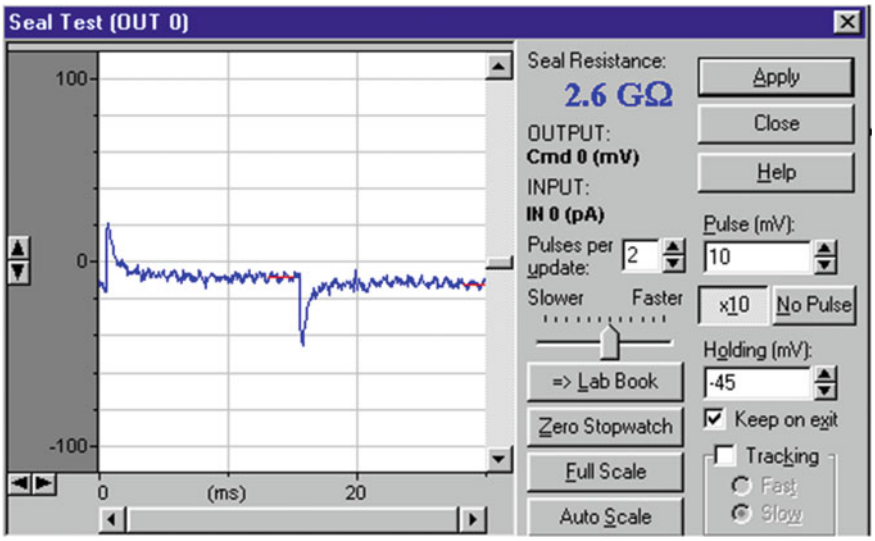

Fig. 6. Effects of badly compensating pipette/electrode impedance

Finally, Fig. 6 shows the uncompensated peaks (from +20 to −40 pA) that remain at the end of the calibration phase, instead of having a flat curve as in the 4th curve of Fig. 2 (“compensation”), when the pipette impedance compensation is not perfectly working. These peaks will be super-imposed on the acquired traces thus limiting the accuracy of the experiment. The main difference with respect to the random spikes due

to unshielded EMI sources, is that the repetition of the uncompensated spikes in Fig. 6 is periodic. Therefore, it is easy to detect and cancel them by off-line signal processing.

5 Conclusions

We have discussed different types of failure occurred in the electronic instrumentation for patch-clamp experiment and their effect on the acquired measurements. The patch-clamp is an electrophysiological technique that allows the study of single or multiple ion channels in a variety of normal and pathological cell types. Moreover, electrophysiological approaches can be employed to screen drugs for their effects on ion channels. Faults in the Peltier cell, used to keep the measuring head-stage cold, cause an increase by 20% of the background noise with a white noise having maximum peaks of about ±5 pA. This can be a problem only in single channel measurements, when very low ionic currents are acquired. Otherwise, the blocking or stimulating effect of a drug on ionic channels causes a variation of several tens of pA, which can still be detected also in the presence of increased background noise. Instead, interference from incorrectly shielded AC sources such as motors (e.g. of the peristaltic pump) or of the switching power supply, cause random spikes, difficult to remove, with a dynamic higher than 50 pA. A bad compensation for the pipette impedance can cause also spikes, up to 20 pA, although they have a periodic repetition and hence are easier to detect and remove.

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ICs and Memories

Performance Evaluation of Non Volatile Memories with a Low Cost and Portable Automatic Test Equipment

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Abstract. This paper presents a versatile and portable test equipment, called portable ATE for research and development of non-volatile memories functionalities. The system is based on STM32-NUCLEO assembled with a custom designed daughter board, in order to host non-volatile memories test-chips, to manage the needed power supplies and generate suitable signals stimuli for correct operations. The system is controlled and programmed by a personal computer, via USB interface. In particular the system can perform: memory reading, writing and erasing, with settings flexibility on time and voltage levels; Electrical Stress Tests (Drain, Gate and Bulk Stress); Cycling Tests; debugging algorithms (erase or program with verify, refresh, etc.…) thanks to tailored test programs running in the microcontroller. This system has already been used to achieve early stage characterization of STMicroelectronics memory test-chips described in this work and a lot of other appropriate combinations of the setting parameters are also available for future developments.

Keywords: Flash memory · Testing · ATE · Portable ATE · USB · Characterization

1 Introduction

The reliability of stored data retention is one of the fundamental issues of flash memory; they are routinely tested in production, with specific procedures, implemented on ATE (Automated Test Equipment) in order to detect possible faulty events during reading, programming and erasing actions. Proper trimming of flash memories internal parameters are also carried out trying to identify possible fault conditions while moving parameter's values within their admitted ranges.

In recent decades, besides ATE classical testing, chip designers introduced BIST (Built-In-Self-Test) techniques that, by using additional hardware and/or software

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within the integrated circuits, allow the self-test (functional and/or parametric) in order to decrease their dependence on external ATE and thereby significantly reducing the run time of the completed test, while improving the accuracy and especially allowing the implementation of IC test at any time and operating conditions (so-called in-field tests).

During normal use by the end user, in-field memory test (i.e.: on power up or during periods of inactivity/idle) has become essential in order to optimize memory operation and to ensure the longest possible lifetime. For this reason the so-called Transparent BIST technique [1] is also developed; it allows data storage in memory and operates in a mode resulting transparent to the user.

More recently a further step in the in-field testing has been carried out through the development of SBST techniques (Software-Based Self Test) [2]; these are based on the use of the microprocessor located within the memory chip to carry out the necessary tests via software, without the need to design and implement the additional integrated hardware, as it happens in the case of BIST structures within the circuit.

The SBST techniques have shown considerable flexibility and a total coverage of previously performed tests via BIST with the only increase in the overall testing time but without the need for additional hardware.

Keeping in mind the state of the art of the above described testing techniques, the study, design and implementation of an innovative circuit solution called Portable-ATE for testing of Memory Test Chip was performed.

The Portable-ATE, shown in Fig. 1, is designed for performance evaluation at research and development (R&D) level where testing adaptability, configurability together with capability to get immediate results are the most significant factors in the development process [3, 4].

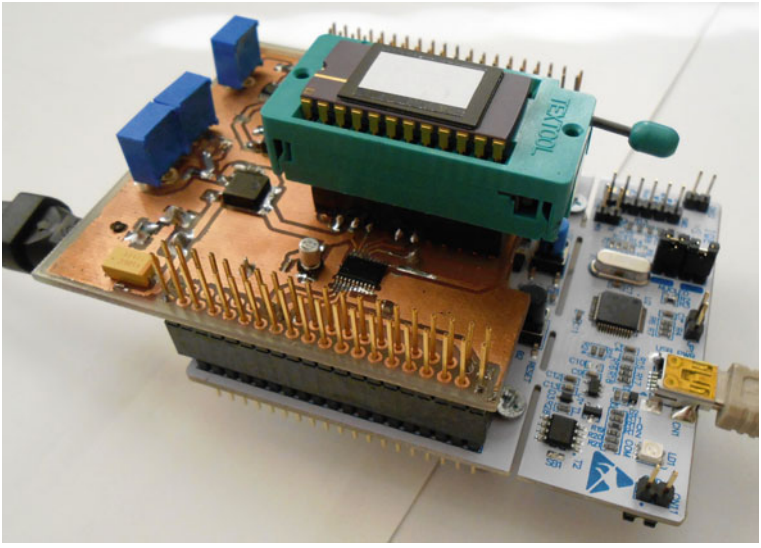

Fig. 1. Portable ATE with memory STMicroelectronics test-chip on board

It is a microcontroller based testing board, working in conjunction with a low end general purpose personal computer, designed to investigate performances of single non-volatile memories test-chips, with the same reliability and reproducibility of industrial ATEs but with some added features in term of flexibility and configurability [5].

The portable ATE was developed starting from an ARM based STM32-NUCLEO (STM32F072RB) and a daughter custom board has been added to the overall design in order to host the non-volatile memory test-chip, to manage the necessary power supplies and to generate suitable signals stimuli for correct operations.

The STM32-NUCLEO was linked to a PC via USB interface, both for firmware downloading and to control, via Graphic User Interface, memory testing and data collections.

2 The Test System

The test equipment uses an STM-NUCLEO board (STM32F072RB) running with a 48 MHz clock and a custom board hosting the memory under test (MUT) and capable to collect data via SPI with a maximum speed up to 12 MHz. The block diagram of the whole portable ATE is shown in Fig. 2.

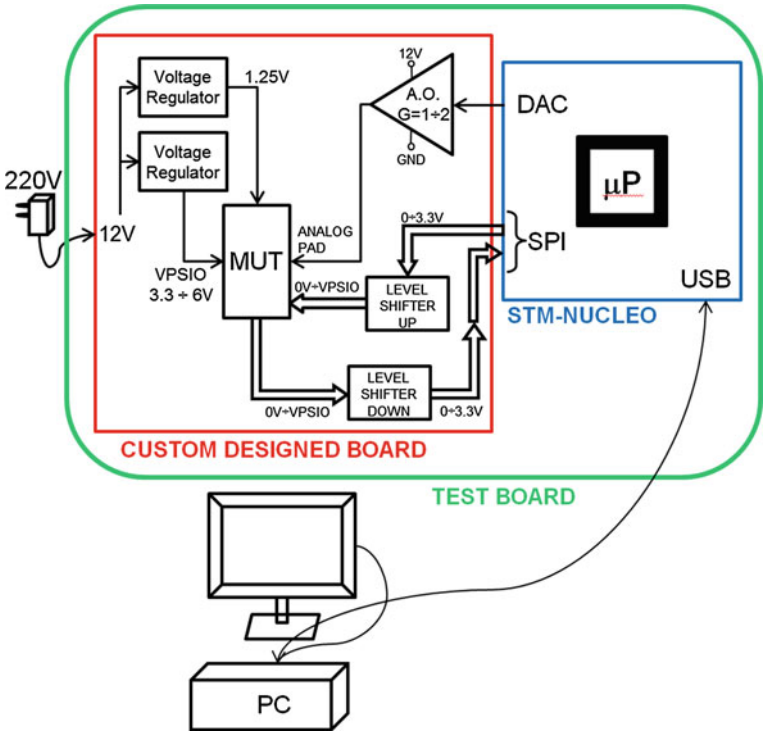

Fig. 2. Portable ATE—architecture block diagram

The power supply voltages needed for correct operations are: a 1.25 V reference voltage and a controllable VPSIO ranging from 3.3 up to 6 V. They are generated by two linear regulators, fed by a plug-in power supply (220 V).

The VPSIO is the maximum high-level voltage delivered to the MUT's pads and in some tests it is necessary to increase its value from nominal 3.3 up to 6 V as, for example, in the case of monitoring/forcing the bit line voltage while programming through the analog pad, also shown in the architecture. If the VPSIO must go above 3.3 V, this high-level memory voltage is unreachable with the STM32-NUCLEO, since its maximum sustainable voltage is 3.3 V, therefore some bidirectional level shifters have been added to tailor the voltage levels of all needed signals.

Moreover an analog pad is controlled by the DAC output of the STM32_NUCLEO main board; it is suitably amplified (Gain range 1÷2) in order to provide a maximum level voltage of 6.6 V and, through appropriate settings, it can control several significant signals within the MUT as gate, bitline, wordline or bulk signal. Therefore it can be used to carry out noteworthy analysis as threshold distributions, different voltage stress and several other investigations. The same analog pad can also be disconnected from the DAC output, through a jumper, and it is also used for reading signal voltages coming out from the MUT.

The STM32-NUCLEO communicates with the memory test-chip via the SPI protocol, it implements the following 5 commands:

- Test Chip Register Write;
- Test Chip Register Read;
- Memory Array Write;
- Memory Array Read;
- Multiple Memory Array Read.

The related software has been developed in C language and managed to perform a number of relevant tests whose results are described hereafter and to show the attained results through a user friendly graphic interface, running within the host PC. The easy use of developed software allows a huge user flexibility, with a perfect customization of all operations, tests and algorithms debugging.

In particular the system can perform: memory reading, writing and erasing, with settings flexibility on time and voltage levels; Electrical Stress Test (Drain, Gate, Bulk Stress); Cycling Tests; threshold distributions; debugging algorithms (erase or program with verify, refresh, etc.…).

3 Experimental Results

In this section an example of drain stress testing with the proposed portable ATE is described. The Fig. 3 shows a graph with the results of a Drain Stress analysis carried out on a memory semi-array (256 pages, 128 words per page).

In particular plotted data were collected after a previous ageing phase obtained through a 128,000 program/erase cycles carried out onto half of the memory array. Therefore in the other semi-array, a standard checkboard test of has been done with a total of 100,000 cycles grouped in steps of 20,000 program/erase cycles.

X-axis reports the relative threshold voltages (ΔV_{TH}) referred to the V_{TH} sensing value and results highlight the expected convergence of distributions to its central value, after ageing.

To validate the results obtained with Portable-ATE, these have been compared with a drain stress test carried out with classic ATE Teradyne J750 (Fig. 4 shows the results of this test). In particular the test was developed on a 64 pages (128 words per page) aged through a 100,000 program/erase cycles where a standard checkboard was written. The graphs in Figs. 3 and 4 show the same trend of the curve as cycles number increased. In particular the results highlight the same closing window behavior between the erased and programmed cells, as number of ageing cycles is increasing; furthermore the bell shape of the programmed cells tends to became slightly narrower and with a taller peak value in both cases.

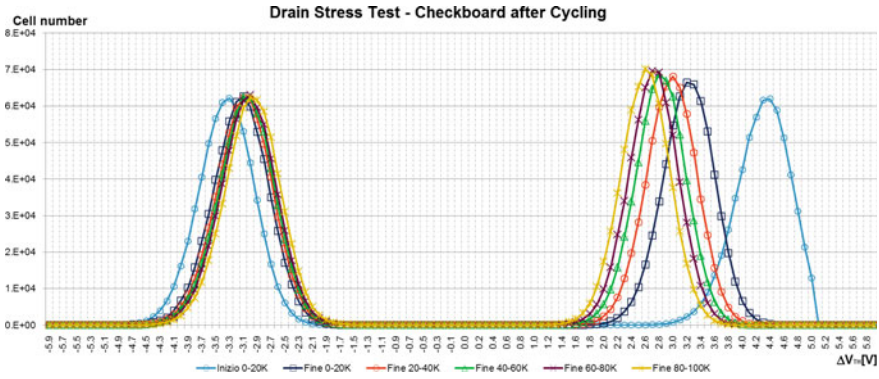

Fig. 3. Results of drain stress on cycled memory cells

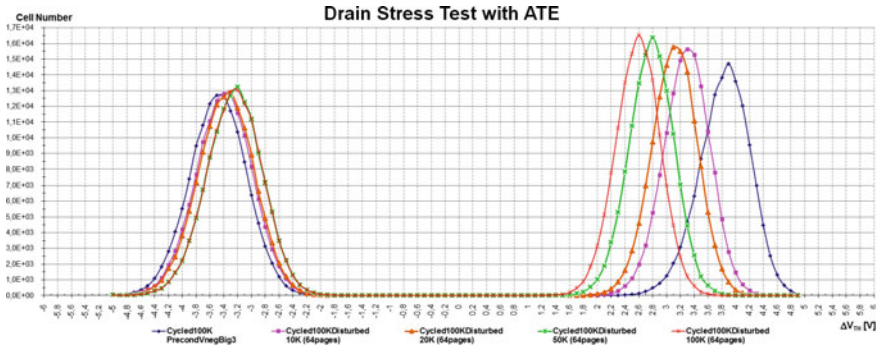

Fig. 4. Drain stress on cycled memory cell with classic ATE (Teradyne J750)

4 Conclusion

This paper presents the implementation of a very low cost and portable ATE based on STM32-NUCLEO, assembled with a custom designed board and running a C firmware linked to a host PC via USB interface.

This system has already been used to achieve early stage characterization of STMicroelectronics memory test-chips by performing electrical, stress and reliability tests; it was done by changing numerous internal parameters without using additional resources.

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An Emulator for Approximate Memory Platforms Based on QEmu

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Abstract. In this paper, an emulation environment for approximate memory architectures is presented. In the context of error tolerant applications, in which energy is saved at the expense of the occurrence of errors in data processing, approximate memories play a relevant part. Approximate memories are memories where read/write errors are allowed with controlled probability. In general these errors are the result of circuital or architectural techniques (i.e. voltage scaling, refresh rate reduction) introduced to save energy. The ability to simulate these systems is particularly important since the amount of tolerated error is application dependent. Simulation allows to analyze the behavior of an application and explore its tolerance to actual error rates, determining the trade-off between saved energy and output quality. We have developed an emulation environment for such architectures, based on QEmu, which allows the execution of programs that can allocate some of their data in a memory zone subject to faults. We present the emulated architecture, the fault injection model and a case of study showing results that can be obtained by our emulator.

Keywords: Embedded systems emulation · Approximate computing · Approximate memory

1 Introduction

In the last few years, an increasing interest has been concentrated on the possibility of implementing systems that are capable of trading off computation accuracy for speed or power consumption [1–4]. Such systems rely on the fact that for many applications the quality of results perceived by the user is not affected by a certain degree of approximation in the output data. Examples are portable multi-media applications [5,6] and, to some extent, data mining applications that extract statistical information from big data structures.

Approximate computing can be implemented through different paradigms as:

- Data-level approximate computing [7,8];
- Instruction level approximate computing [3,9];
- Algorithmic level approximate computing [2];

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While algorithmic level and, less incisively, instruction level approximate computing are more aggressive and challenging from a technical point of view, data-level approaches can be of major relevance because most applications that are suitable for approximate computing utilize large amounts of dynamically allocated data memory (e.g. multi-media processing [10,11]) and it is generally agreed that memory devices accounts by far for the largest parts of static power consumption in modern ICs [8,12].

In order to open the way for reliable data-level approximate application development, it is required an evaluation environment to simulate the actual output of the application when processing true inaccurate data. Inaccuracy can occur at different degrees in different memory segments, can be caused by single random events or can be correlated to read and write accesses, can be differently distributed in the bytes of the memory word.

This paper presents an emulator for approximate memories based on the QEmu environment [13], it allows modeling at architectural level of a complete platform, containing all QEmu hardware units as processors, memories, interrupts, I/O and graphical peripherals, mass storage, communication and interconnection peripherals, plus the presence of approximate memories. The environment features approximate memory units with different levels of accuracy, tunable at byte level and at segment level, being intended to support present and future solutions for approximate memory device implementation. The emulator can run applications using approximate memory, in order to evaluate the actual output produced by approximate data and the impact of different approximation levels and strategies.

The article is organized as follows: in Sect. 2 we outline the architecture emulated and the specific applications it is built for; in Sect. 3 we describe the models we introduced to account for different phenomena causing errors on physical memory cells, depending on their technology (static or dynamic memory), circuit/logic level strategies for reducing power consumption (e.g. voltage scaling, refresh rate reduction) and the actual amount of their entity; in Sect. 4 we show a case of study and results that can be obtained using the emulator.

2 Definition of the Emulated Architecture

The platform we intend to emulate is showed in Fig. 1. It is a CPU based architecture with peripherals, exact memory (i.e. normal memory) and approximate memory.

Approximate memory is a particular physical memory where circuit-level or architecture-level measures have been implemented in order to save energy at the expense of errors occurring in memory cells. We underline that exact memory has still to be present because even in error-tolerant applications, some data structures must be kept exact. These data structures are typically those determining control flow decisions in the algorithm, for example data that are used in conditional statements.

Error-tolerant data are usually the result of real world measures or sampling or, on the other side, data that must be sent to the real world (e.g. signals, audio, images) or actuators. These data are inherently affected by approximation and errors, hence storing it in approximate memory, under controlled conditions, may have tolerated effects on the application, while pushing the trade-off toward energy saving.

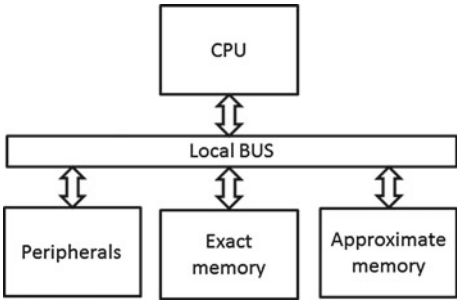

Fig. 1. Emulated architecture

We implemented approximate memory as a device in QEmu, mapping it in the address space, beside exact memory. All read and write accesses to this device are intercepted and faults are injected according to the model presented in the following section.

3 Error Injection Model

The scope of approximate computing is to save energy by relaxing the requirements on data integrity, allowing for a significant amount of errors to be introduced at bit level. As regard memories, we can consider different design strategies to be actively used in order to introduce approximation, depending on memory technology. For example, in static RAM supply voltage scaling can be applied, while in dynamic RAM refresh rate can be reduced in order to save energy.

Considering this two main techniques and different circuital implementations [7,8,14], we produced a model based on the assumption that, in approximate memories, errors on cells can be introduced by access operations or can occur randomly during time, even if the cell is not accessed.

3.1 Error on Access

The error on access happens when a cell is activated to perform a read or write operation. Depending on the access we distinguish between three kind of errors.

- Error on write: introduced during a write operation, the bit stored in the cell is different from the one coming from the data bus
- Destructive error on read: introduced during a read operation, the bit stored in the cell is corrupted and passed to the data bus (both cell and data bus contain the corrupted bit)
- Non-destructive error on read: introduced during a read operation, the bit stored in the cell is not corrupted during the operation, but it is passed corrupted to the data bus.

For each of this kind of errors, a uniform probability distribution is applied by fault injection code, expressed in terms of probability of error per access.

3.2 Spontaneuos Errors

Spontaneous errors are random errors occurring spontaneously in the cell during time, even if the cell is not accessed. Fault injection in this case emulates the degrading of data over time. We assumed a uniform probability distribution in the array of cells, expressing the fault rate in terms of number of errors per second per bit. In order to implement this second mechanism, we instantiated a QEmu single-shot timer, whose waking delays are generated using a Poisson distribution, emulating single independent fault events.

3.3 Looseness Mask

While being physically equal, cells in a memory array store bits that have different weights in terms of data representation. In other words, given a certain data (e.g. a 32-bit integer number), a fault in a cell that store one of the most significant bits (MSBs) has a larger impact on the value, with respect to a fault occurring in one of the least significant bits (LSBs). Starting from this consideration, some circuital and architectural energy saving solutions allow for introducing distinct levels of degradation in the cells of the memory array.

In order to support the emulation of these techniques, we inserted the concept of looseness mask in the emulator. The looseness mask is a 32-bit configurable mask (constant for the whole memory array) that is applied to every 32-bit location in memory. It allows the protection from faults of selective bits (i.e. the MSBs) in every 32-bit memory location. Bits in the memory locations are not affected by faults when the corresponding bit in the looseness mask is set to zero (i.e. with a looseness mask set to 0x0FFFFFFF, the 4 MSBs are exact, while the 28 LSBs are affected by faults).

4 Results on a Case of Study

In order to show the kind of results that can be obtained through the emulator, we present here, as case of study of a typical error tolerant application, a digital filter. We developed a 100-taps FIR filter program (configured as low-pass filter) working on audio signals, allocating data on approximate memory. In particular, Fig. 2 shows the diagram of data flowing from the input file to the output file. The program allocates in

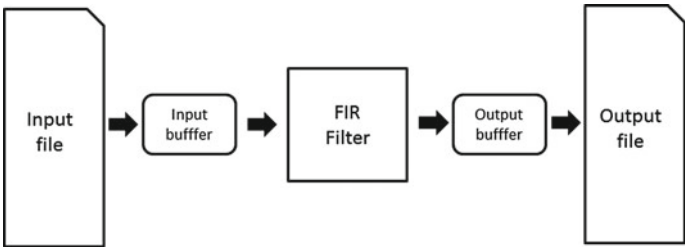

Fig. 2. FIR program data flow structure

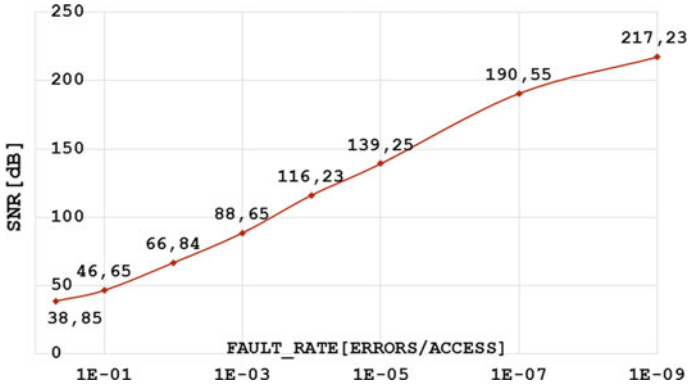

Fig. 3. SNR in function of fault rate, looseness mask 0x0FFFFFFF

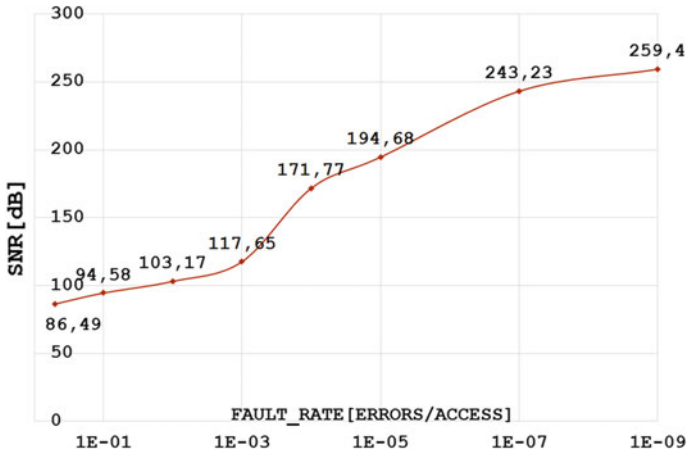

Fig. 4. SNR in function of fault rate, looseness mask 0x00FFFFFF

approximate memory the input buffer, the output buffer and the internal tap registers of the FIR filter.

As quality metric, we used SNR, measured considering noise as the difference between the output of the exact filter and the output of the approximated filter. Figure 3 shows SNR as function of error rate, considering only error on access (the three error on access rates are set equal) and looseness mask set to 0x0FFFFFFF. We can see that the SNR progressively degrades from very high values for lower fault rates to smaller values for very high fault rates. The level of SNR which can be considered acceptable depend on the application, hence reinforcing the importance of an emulation environment able to produce these results. Considering the actual function (filtering of a 16-bit audio signal) reference SNR values to be used as comparison are, for example, SNR ratios of typical music or voice applications. As further comparison, Fig. 4 shows SNR with the looseness mask set to 0x00FFFFFF (i.e. only the 24 LSBs in the word are

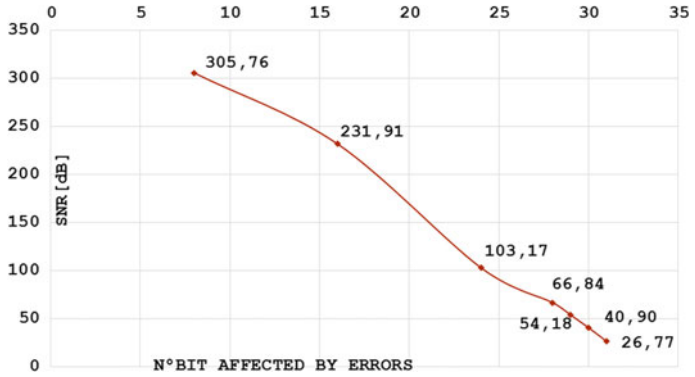

Fig. 5. SNR in function of number of bits affected by errors, fault rate $10^{-2}\, errors/access$

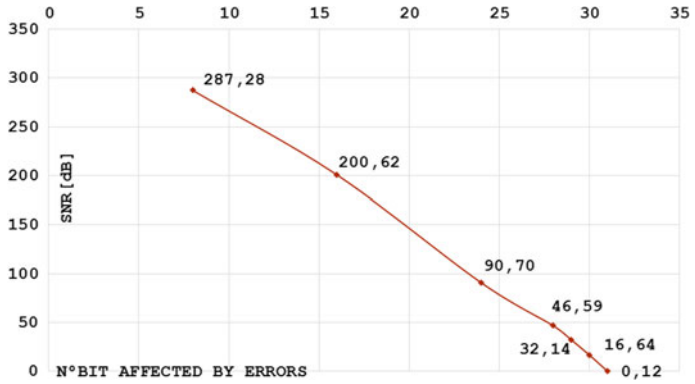

Fig. 6. SNR in function of number of bits affected by errors, fault rate $10^{-1}\, errors/access$

affected by errors). We can see how the effect of leaving more MSBs exact results in higher SNRs for the same fault rates.

Figures 5 and 6 shows instead the dependence of SNR on the number of LSBs affected by faults (i.e. varying the looseness mask), considering respectively fault rates of $10^{-2}\, errors/access$ and $10^{-1}\, errors/access$. We can see how the idea of maintaining exact a small number of MSBs has anyway a deep impact in rising SNR.

5 Conclusions

In the paper we presented an emulator based on QEmu which introduces approximate memory in the architecture. Faults are injected during the simulation, based on models built to reproduce the effects on memory cells of circuital and architectural techniques for approximate memories. The tool is able to execute programs that can allocate exact and approximate memory, evaluating their behavior depending on configurable fault rates and probabilities. We showed through a case of study how our emulator is able to

reproduce the effects on the output data of faults in memory and allow the evaluation of their impact on the application.

Future works may include the modification of an operating system (e.g. Linux) in order to add the support of approximate memory zones and allow for dynamic allocation and deallocation at user level of approximate memory, as for normal exact memory.

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Failure Analysis of Plastic Packages for Low-Power ICs

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Abstract. The paper analyses the trend in packaging for low-power integrated circuits (IC) and the principal failures that can occur. A Fault-tree (FT) analysis is proposed, as well an analysis of the failure distribution (FD), which can be useful in safety-critical applications such as industrial and automotive.

Keywords: Failure mode and effect analysis (FMEA) · Functional safety · Automotive electronics · Integrated Circuits (ICs) · Packaging

1 Introduction

Plastic encapsulated microelectronics (PEMs) technology use plastic material to encapsulate ICs for environmental protection in which the encapsulate materials contact with the die, lead-frame and bonding interconnects. Many advantages can be gained with PEMs, such as lower cost, smaller size, lighter weight, greater availability of different packages and functions. However, the plastic mold materials used to encapsulate the ICs are hygroscopic and absorptive. When they are applied into a high temperature environment, such as automotive or industrial, the moisture vapors could lead to delamination and/or cracking which affect the long-term reliability of PEMs. The mismatched coefficient of thermal expansion (CTE) between the epoxy molding materials and the various interfaces of PEMs would cause thermos-mechanical stresses. This damages the IC and leads to a failure of the device. To address the problem of PEM reliability in safety-critical applications such as automotive and industrial, Sect. 2 reviews the packaging trends, whereas Sects. 3 and 4 present an analysis of the FT, of the FD rate, and discuss the main sources of interference and the possible countermeasures. Conclusions are shown in Sect. 5.

2 Package Trends

A market analysis of the most used package types for the chips of interest (low-power MCU from 80 to 800 pins in automotive or industrial applications) highlights that the market is dominated by LQFP package of plastic-type, see Fig. 1.

This type of package is preferred for devices with a pin number from 80 to 140 for its reliability. For devices that require a greater number of pins, BGA (ball grid array)

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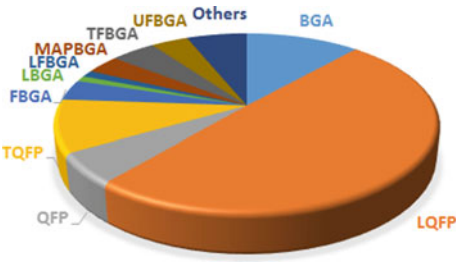

Fig. 1. Market of packages (%) for low-power microcontrollers (MCUs)

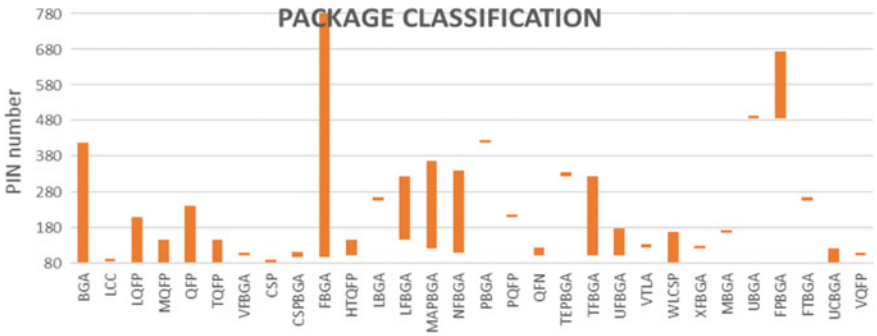

Fig. 2. Package classification based on pin number

packages are preferred for their big ratio pin for area. Figure 2 instead, shows a classification of pin numbers for each package type. The package with the biggest range of applications, based on the pin number is the FBGA. The most diffuse package is the LQFP despite the smaller range of application (from 80 to 220 pin).

The data has been extracted from the biggest online electronic distributors like Farnell, RS Components, Mouser Electronics, Digi-Key and Arrow Electronics.

3 Fault Tree and Fault Distribution Analysis

The Fault Tree (FT) analysis method is the most widely used technique to give an indication on the cause-effect relationships. For electronic components a specific failure mode is considered as "top event". The structure is aiming to evidence the failure logical relationship between faults and their causes. An important observation is the probability that a failure event happens [1]. The higher is the probability, the higher should be the action to reduce it. In this paper we propose two main FTs where two main failures are separately considerate "Open failure" in Fig. 3 and "Close failure" in Fig. 4. The first takes into account the failures due to the interruption of the signal or power supplies, while the second considers the failures created by the connection of signal paths each other or with the power supplies (stuck at VCC or stuck at GND). Table 1 shows the distribution of faults for the FTA, which has been derived from the analysis of real components in the market.

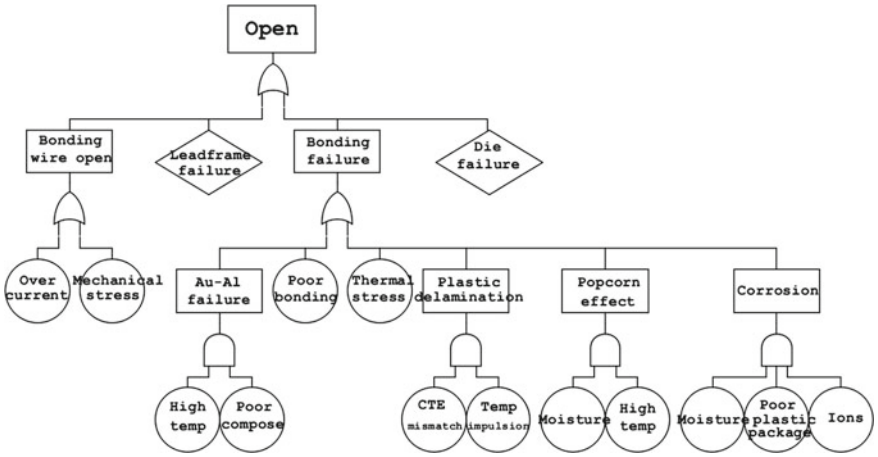

Fig. 3. FTA for open fault

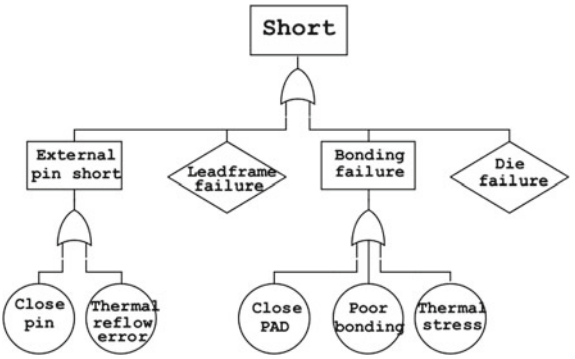

Fig. 4. FTA for short fault

Table 1. % of FTA for short fault

Failure mechanism	%	Description
Broken wires/bonds and lifted wires	32.3	Failures seen at the second stitch bonds on the lead frame or substrates
Die cracking	15.54	Die chipping, passivation cracking or metal traces cracking in the die
Delamination and popcorn effect	12.71	Interface delamination, such as mold/die interface
Die damage/wafer defects	12.14	Die surface damage or scratch
Package/substrate cracking	10.17	Organic substrate crack and solder mask cracks
Other	17.23	Other failures. e.g. solderability, foreign materials

4 Failure Type Analysis

4.1 Bonding Failure

According to the correlative statistic data, percentage of wire-bonding resulting in IC's failure is about 32.3%. It has a significant effect in IC long-term reliability [2]. During the bonding Au–Al or Cu–Al a small portion of the Au wire is melt forming a ball as the wire material solidifies. The ball is pressed to the pad on the die with sufficient force to cause deformation and inter-diffusion of the wire and the underlying metallization, which ensures the contact between the two metal surfaces.

4.2 Au–Al Bonding

The problem of Au–Al bond reliability in IC devices under high temperature is very important. The failure of Au/Al wire-bonding results in poor contact, wire shifting or failure off. High working temperature, poor heat-spreading of the die or large current are all causes of Au/Al failure. The creation of Au/Al intermetallic compound and Kirkendall voids result in increasing of contact resistance and intermittently or permanent open failure mode. Intermetallic compounds form when two metals diffuse into one another creating other species materials. For the Au/Al bonding, there are five different intermetallic compounds that can form. These intermetallic elements are always present in Au/Al bonds but their concentration increases with high temperature and time. During the change of the temperature, the bond wires change their shape and the bond's mechanical strength increases. This may break the wire or divide the bond balls from the die pads so intermittently or permanently open appear. To improve the reliability of bonding, it is important that the control of manufacturing equipment and selection of materials is properly conducted to secure the initial joint properties. Unnecessary heating on semiconductor devices after the bonding process the atomic inter-diffusion, because Au goes into Al much faster than Al goes into Au. The result is an increase of vacancies at the Au side of the intermetallic stack. In the end of the useful life, bond's contact resistance increase, degrading the chip performance, and finally becomes open. The formation of Kirkendall voids principally depend on time, temperature and chemical concentration of the diffusion species.

4.3 Cu–Al Bonding

The problem with the intermetallic compounds (IMC) forms can be reduce using Cu wires instead Au wires, see Fig. 5. The IMC layers are fundamental for the bonding but these should be thin. IMC are fragile, with poor conductivity and lead to crack at the interface. Thicker IMC layers reduce the IC reliability and performance.

The Cu–Al interface is characterized of an initial thinner layer of IMC than Au–Al bonding. Furthermore, the IMC layer growing of Cu–Al is very slower during the storage than the other metal couple. Cu–Al rarely fails due to defective IMC structure, which is typical of Au/Al bonds. An important element consideration should be made about the IMC interface coverage. The coverage of the bonding ball should be upper than 60% for a good reliability [3]. The Cu higher hardness than Au may is an

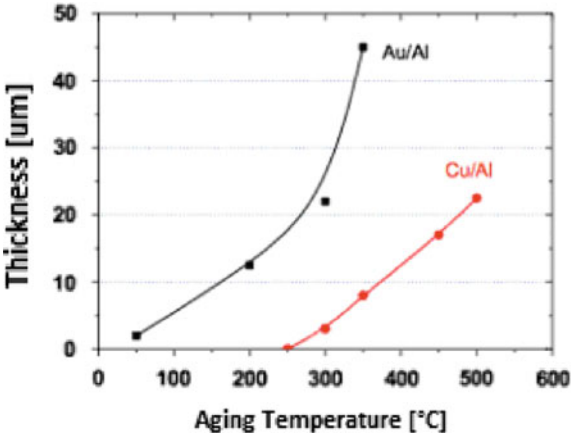

Fig. 5. Intermetallic growth. Au/Al IMC layer is thicker than Cu/Al at same temp

advantage on a hand, but on the other is a problem. More stress is transmitted to the underlying substrate during bonding for harder wire. This can result in fracture of the underlying substrate (cratering). If the bonding process guarantees a good join of Cu wire, reducing the creation of crater, this solution is more indicated for automotive applications.

4.4 Popcorn Effect

Popcorn is a common failure mechanism in plastic-encapsulated microcircuit [4]. It occurs when the device is rapidly exposed to high-temperature (as reflow soldering or harsh environment). At these temperatures the moisture absorbed by plastic materials in package suddenly vaporizes and expands resulting in rapidly increasing vapor pressure inside of package. When the high vapor pressure increases the void or defects along the interface will grow to result in delamination, and formation of cracks. When the crack reaches the package exterior, high pressure vapor is rapidly released, producing an audible sound like popcorning. This effect can be close to die, going to move the die from the lead-frame, damaging the bonding wires. If the crack reaches the exterior

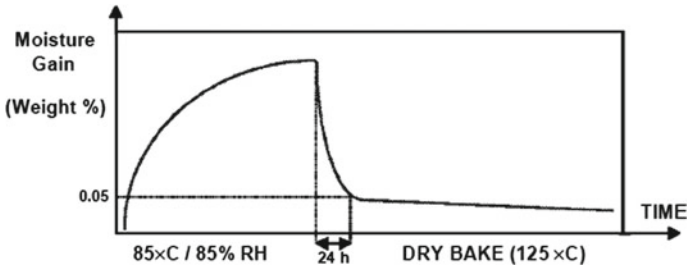

Fig. 6. Moisture inside the package. Effect of backed the chip

other corrosive elements may get inside damaging the die and the bonding structures. Popcorning may result in immediate or long-term failure of the device (Fig. 6).

To reduce this effect some precaution should be taken:

- Control the humidity and temperature of the place where semiconductor devices are stored and the duration of it.
- Use the devices as soon as the moisture-proof pack is opened. These pack should have inside a desiccant.
- Mount devices at as low a temperature as possible and in as short a time as possible while controlling the moisture absorption.
- The stored period is important. If the devices are stored over the specific period need to be baked at 125 °C for 24 h (under nitrogen atmosphere). Like shows in the graphic, this reduces drastically the moisture absorbed and so reduces the risk of popcorning during the solder reflow.

4.5 Different CTE

When PEMs is applied to rapid temperature changed environment. The mismatched coefficient of thermal expansion (CTE) between the molding compound and the lead-frame or die may cause delamination or crack between the surfaces. Especially the thermal expansion coefficient of molding compound is almost one order of magnitude larger than the silicon (molding compound $\approx 25 \times 10^{-6}$ °C^{-1}, Silicon $\approx 2.3 \times 10^{-6}$ °C^{-1}, gold $\approx 14 \times 10^{-6}$ °C^{-1}), when the temperature changes, during the thermal solder reflow or other situation, the size change of package and chip will be greater which bring out stress. This stress may cause a weak adhesion on the chip pad bonding, and the shift of the bonding ball may create short circuit or open circuit. The shear stress may create crack under the die, between the plastic package and the die, leads to pockets of air that reduce the heat dissipation. The passivation peeled off and even damages the chip, resulting in device failure. To avoid the problems relative to the CTE mismatch is necessary use materials with comparable CTE.

4.6 BGA and QFP Failures

The growth in popularity of BGA packages is due to the need of higher I/O number and the reduced package area than quad flat packs (especially for pin counts greater than 160). Many types of BGA packages can be placed up to a half pad off center and will self-align upon reflow of the solder balls. Potential package reliability problems can still occur: excessive solder joint deformation induced by substrate warpage, large variation in solder ball size, voiding as a result of flux entrapment and improper padholder mask design. In most of the cases the crack initiates in the corner solder ball of the packages. In almost all cases, the primary crack initiated at the package interface and later a secondary crack initiated at the board interface. The challenge of bigger packages in QFP (176 pin count) is not only on package reliability, but also critical on solder joint reliability during temperature cycling. The deformation of the metal QFP pin allows to reduce the stress on the solder join, generated from thermal expansion of

plastic package. The pin shape plays a fundamental role in the package reliability. This is one of the causes that make the QFP package more reliable (under thermal stress) of the BGA package. The balls of BGA are subject to shear stress at the interface with the package and the PCB increasing the probability of failure.

5 Conclusions

For no-critical systems, the forecasted request of multi core systems to elaborate complex algorithms could lead to increase the pins count of the packages, therefore favor the BGA packages. But on the other side, in critical systems like automotive or industrial vision applications [5–8], the increasing use of ASICs (Application Specific Integrated Circuits) and the improving of SIP (System In Package) technologies like WLP (Wafer Level Packaging) don't request high pin count favoring QFP packages for their reliability.

The current trend in packaging for low-power MCUs has been analyzed in the paper together with the principal failure that can occur. After reviewing the main causes of failures, a Fault-tree (FT) analysis is proposed, as well an analysis of the failure distribution (FD), which can be useful in industrial and automotive safety-critical applications.

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Smart Cities

Towards a Virtual Reality Interactive Application for Truck Traffic Access Management

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Abstract. This paper presents an ongoing work towards the realization of a virtual reality system providing an advanced visualization of the access of trucks to a critical road segment, such as a tunnel. The system is currently based on optical and laser sensors, and is able to recognize a truck in a dedicated road lane, and to produce a 3D model of the identified vehicle. The 3D model is then employed inside an interactive 3D application usable in real-time by personnel in a dedicated access/traffic management center. The final goal is to integrate several layers of sensor data (e.g., also including infrared information on the temperature of the truck components) in order to support monitoring and control of the critical road segment.

Keywords: Virtual reality · Laser scanner · Point cloud · Image processing · Unity 3D · Traffic management

1 Introduction

Trucks represent a key vector for freight transportation. Trucks are a very flexible transportation means, that require limited infrastructure and are suited and effective for small-size loads. However, truck transportation implies well known issues in terms of traffic congestion and safety. This is particularly true in special road segments, such as tunnels and bridges. As part of the ITS Italy 2020, Italian Technological Cluster project, we are developing a virtual reality system to allow an advanced visualization of the access of trucks to a critical road segment.

This paper presents a system, based on optical and laser sensors, able to recognize a truck in a dedicated road lane, and to produce a 3D model of the identified truck. The 3D model is then employed inside an interactive 3D application. While the work is in progress, the final goal is to have a virtual reality system able to integrate several layers of sensor data (e.g., also including infrared information on the temperature of the truck components) in an interactive photorealistic model usable in real-time by personnel in a center for traffic monitoring/management. This would be particularly relevant for critical road infrastructure segments; such as tunnels or gateways.

3D model extraction from cameras and texture mapping, also in real time, is an established technique, with promising applications especially in video-surveillance [1].

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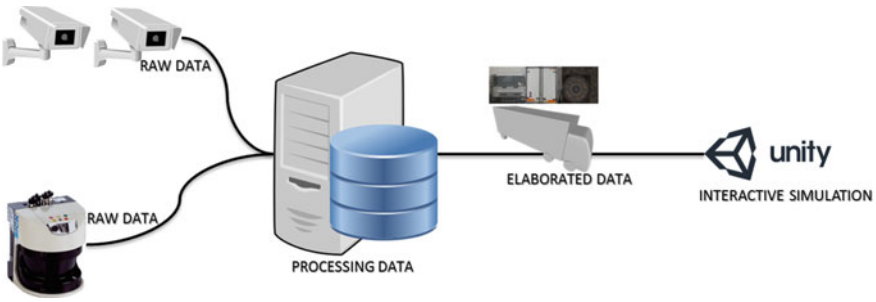

Fig. 1. Overall workflow and system architecture

The main novelty of this paper consists in the proposal of an application workflow combining different sensors and producing its output on an interactive simulation engine such as Unity3D [2] (Fig. 1).

The prototype system has been developed enhancing an existing truck access control system deployed by Aitek S.p.A in an area of the maritime port of Genoa, Italy.

2 Point Cloud Processing and 3D Model Selection

The laser scanner employed in the installation is a SICK LMS 511 2D infrared laser scanner, which is placed over the lane, creating a vertical beam perpendicular to the ground, and covering the whole width of the lane. Thanks to this sensor, it is possible to get the point cloud for a passing through truck (Fig. 2). The cloud point is recorded as a .ply file, that will be later processed.

The system includes a database of cloud points corresponding to different sample trucks, with their associated 3D models. Such cloud points are employed as comparison classes for the data obtained from the laser scanning the current vehicle.

The comparison is performed by a C++ program exploiting the Point Cloud Library (PCL). PCL is an open source stand-alone library devoted to the processing of 2D and 3D images and of point clouds [4].

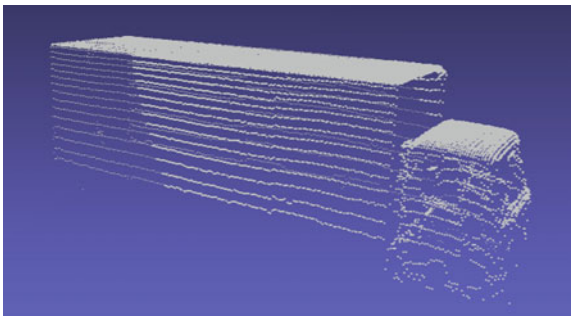

Fig. 2. Point cloud displayed through the open-source Meshlab software [3]

Fig. 3. Synthesis of the point cloud processing workflow

The first step for the comparison algorithm consists in making the inputs coherent with the comparison models, that were preliminarily made coherent among each other. To this end, it is first necessary to implement a scaling transformation, in order to make the point clouds uniform at one dimension on the axis corresponding to the length of the vehicle. Then, a decimation is needed, in order to reduce the number of points, thus diminishing the computational burden of the algorithm, as we'll discuss in Sect. 5.

After these preliminary steps, the actual classification takes place. To this end, the distance is computed from every point in the cloud with the closest point in each comparison model [5]. The average of all these distances is then computed, which is used as classification parameter. The algorithm thus returns the model with the lowest point to point average distance with the cloud of the passing-by vehicle.

The database currently contains 6 models and was built with models taken from the recordings or adapted from those available online freely or in the stores. At present, the comparison is made thoroughly, for all the models. This is feasible, given the current size of the database. Optimization techniques will be needed as the size grows.

The point cloud processing workflow presented in this section is sketched in Fig. 3.

3 Image Processing and Texture Extraction

In parallel with the point cloud processing, the system proceeds with image processing aimed at the recognition of the vehicle and the extraction of the relevant textures, that will be applied over the 3D model to be used in the final virtual reality environment.

In order to illustrate the followed procedure, we'll exploit a running-through case study of a small truck. Figure 4 shows images taken from the two cameras, pointing towards the two ends of the monitored lane.

The images are analysed in real-time by a software written in C++. The program exploits the Open Source Computer Vision (OpenCV) library, a reference library for computer vision applications (acquisition, processing and analysis of images) [6].

The first operation is a pixel-by-pixel background subtraction [7], performed by comparing two different frames at a 0.5 s distance. This operation highlights the moving blobs, extracting them from the background (Fig. 5a).

Among the detected moving blobs, only those are selected, whose bounding boxes (or compounded bounding boxes) have sizes compatible with a truck. A second filtering keeps just the bounding box in the interest area (i.e., the lane). The choice of the sizes and of the coordinates for the interest area are made empirically, depending on the position and orientation of the cameras (Fig. 5b).

The moving object is tracked for up to 4 frames, in order to detect the direction, which is needed in order to identify the front or the back of the truck.

Fig. 4. Picture taken from the back and front cameras

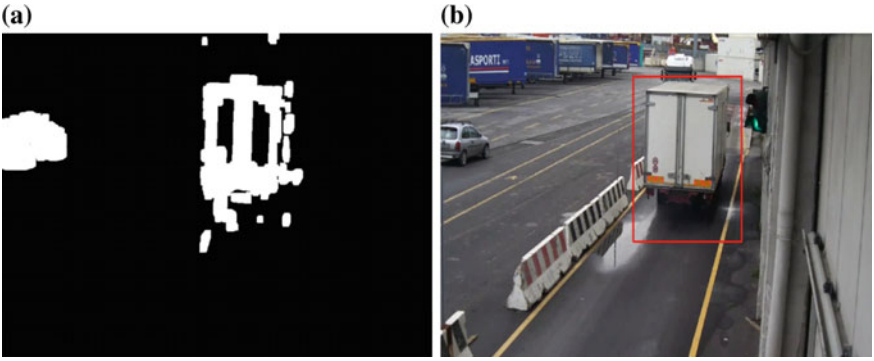

Fig. 5. Background subtraction (**a**) and bounding box extraction (**b**)

The second step processes only the image portion inside the chosen bounding box, with the goal to identify as closely as possible the shape of the vehicle. To this end, we have used the Hough transform [8], a well-established feature extraction technique—particularly straight lines in our case (Fig. 6a). Of all the detected lines, only those are chosen that meet some parameters defined a priori on the basis of the perspective due to the camera angles. In particular, the algorithm searches for two horizontal and two vertical lines. Considering the given perspective, we consider as horizontal the lines with an angle of -0.05 ± 0.05 radians wrt the horizon and as vertical those with an inclination of 0.05 ± 0.05 to the right. This leads to the extraction of a 4 side polygon, that is expected to enclose the vehicle figure. If one of the two lines is not detected (typically because of lighting conditions or of a particular shape of the vehicle), it is placed at a predefined distance. If neither line is detected, a pre-defined bounding box is chosen. We have empirically verified (e.g., Fig. 6) that the final visual effect is quite negligible.

The polygonal image extracted at the previous step then undergoes a perspective correction operation [9], in order to have a rectangular texture usable in a 3D model (Fig. 6b).

The described procedure is performed for both the cameras, and the results put in a single image file, together with a standard image for the wheels (Fig. 7). This single file is then used for the standard texture mapping typical of any 3D model.

The optical processing workflow presented in this section is synthetized in Fig. 8.

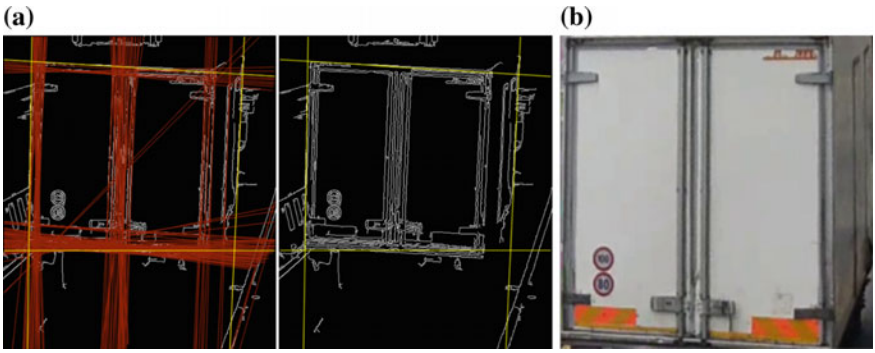

Fig. 6. Hough transform (**a**) and perspective correction (**b**)

Fig. 7. The complete texture

Fig. 8. Synthesis of the optical processing workflow

4 Virtual 3D Environment

The last step of the procedure consists in the insertion of a photorealistic representation of the detected vehicles in an interactive 3D application aimed at the monitoring of the passing-by vehicles.

The application exploits the Unity3D simulation engine. Unity3D features a multi-platform development environment mostly oriented to video-games but useful to implement all those applications—typically simulations—that need managing interactive 3D models.

After loading the 3D model selected as described in Sect. 2, to which the

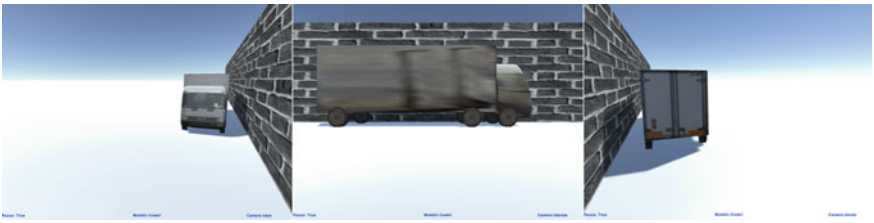

Fig. 9. Three different views of the Unity3D-based simulator

textures prepared in Sect. 3 are applied, the developed simulation program simply makes the model moving at a pre-defined speed and allows an operator to watch the reconstructed scene from different perspectives (Fig. 9).

Given the fact that the current experimental installation only includes the two front and rear camera. The 3D model selected in the database is stretched in order to meet the actual sizes of the real vehicle. If the selected 3D model includes a tractor and a trailer, the stretching distinguishes between the two. Moreover, since the current installation lacks a lateral view of the truck, the sides of the 3D model are depicted with an interpolation of the values of the back texture.

The application runs endlessly, continuously waiting for the outcomes of the two modules described in Sects. 2 and 3. As soon as material for a new vehicle is ready, the 3D model is built and displayed to the end user.

5 Performance Analysis

Performance tests have been realized employing a notebook equipped with an Intel i7-6700HQ processor and 16 GB RAM, compiling the software for a 64 bit architecture and the Windows 10 operating system. The image processing works on recorded videos, while the final installation should process real-time streaming.

The original cloud points present a number of clouds between 30,000 and 65,000, apart from some particular cases of a 4,000 point van and a 8,000 point tractor. After the decimation operation, we work on a dataset of 1,700 to 2,500 points. Decimation has a very minor impact on the pre-processing (879 vs 844 ms), where most of the time is spent for loading the *.ply* pointcloud file. The comparison time for a single model takes 14–21 ms in case of decimation, compared to the original 235–756 ms Given the accuracy of the point clouds, the matching results are highly satisfactory, even if accurate tests are needed with much more database models and test vehicles. Also the current exhaustive search matching algorithm will need to be optimized in order to keep the execution times below 1 s.

Model selection and texture extraction run concurrently. The bottleneck is now given by the optical processing path, taking about 1 s for the direction identification (which currently involves processing 2–4 frames) plus 470 ms for texture extraction. The former step, however, can be skipped in case of one way lanes.

6 Conclusions and Future Work

New generation mobility management systems rely on a combination of ICT technologies, including sensor signal processing and fusion, semantic image elaboration, secure digital processing of sensible data [10]. In the ITS Italy 2020 project, we are developing a virtual reality interactive application for truck traffic access management, starting on the basis of an existing access control system deployed by Aitek S.p.A. in the port of Genoa. The main novelty consists in an application workflow combining different types of sensors and producing its output on an interactive simulation engine.

The current installation does not include a camera taking a lateral view of the truck, which impedes a complete texturization of the truck model. In any case, the placement of the cameras and the quality of the images—in particular of luminosity in different weather condition—are fundamental for the application.

The model database for point cloud classification is still very limited. We strive to improve and extend it through recordings and exploiting other models available on digital stores. Increasing the database will require an optimization of the comparison techniques, possibly resorting to machine learning methodologies as well.

The work is in progress and the implementation is limited. However, the current system already represents a basis for a photorealistic real-time virtual reality simulator. New types of sensors are planned to be integrated. Speed detection will allow moving the models accordingly. More interestingly, availability of far infrared cameras will allow superimposing a thermal map on the visual photorealistic model, enabling an immediate inspection and detection of anomalous heat sources (e.g., different from the engine or a refrigerator, that are obviously warm). This system—once installed in critical road infrastructure points, such as tunnel entrances—is expected to increase safety by preventing dangerous situations.

Finally, since the Unity3D environment is available also on mobile devices, it will be interesting to study the utilization of the tool by field workers as well.

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A Contactless, Energy-Neutral Power Meter for Smart City Applications

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Abstract. Electrical energy management is fundamental to optimize the generation and usage of power within a Smart Grid; and the measurement of parameters of electrical systems is crucial for achieving efficient control on electric loads. Most of the existing smart metering devices use voltage probes which are invasive, because they need a direct connection to the electric conductor. We present an innovative three-phase clamp-on power meter that can be installed without breaking the circuit under measurement and without temporary interruption of the supply. It is used tight around the cable insulators and it measures both current and voltage of the underneath wire. Moreover, it enables the use of advanced signal processing algorithms such as Non-Intrusive Load Monitoring (NILM), which provides fine grain load detection even if a single point of measurement is used.

Keywords: Smart meters · Non-Intrusive Load Monitoring · NILM · Current transformer

1 Introduction

Continuous electrical energy usage monitoring is a major trend in research and commercial deployments, because of the widespread diffusion of distributed generation from renewable and non-programmable energy sources and the increased attention toward increased energy efficiency in appliances and electrical loads in general. We focus on the design of innovative power meters for smart city applications. Our research effort, in cooperation with Telecom Italia Laboratories (TIM), is aligned with the requirements put forward by the Horizon2020 Flexmeter project.[1] Our group is one of the main partners in the Flexmeter consortium, which aims at developing an innovative load profiling

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[1] http://flexmeter.polito.it/.

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system, using household level smart meters. These devices need to be low-cost, unobtrusive, and they must be installed with simple procedures, possibly even without the presence of certified technician. The smart meter should also be able to perform NILM (Non-Intrusive Load Monitoring), analyzing the energy consumption with a breakdown of each single residential appliance. This will permit the utilities to suggest changing user behavior modifications to promote energy savings and to reduce the electric bill, by proposing some scheduling of the loads [1], together with a management of the available renewable and accumulators [2]. In this work we present our smart metering platform design and demonstrate several unique features related to unobtrusiveness and self-sustainability.

Distributed sensing frameworks are replacing the classical centralized energy meters, opening the way to a fine grain energy monitoring based on a distributed network of sensing elements [3]. These nodes must be robust, unobtrusive and low cost while they are required to measure the energy consumption of a power line with accuracies comparable to professional instruments [4,5]. Nevertheless, most of the existing smart metering devices available on the market miss at least one of the necessary requirements for a large diffusion. First of all, current and voltage probes are usually *invasive*, namely they need a direct connection with the cable conductors, thus forcing to shutdown temporarily the electrical appliances under measurement, for the installation of the meters, expensive operation not always feasible. Finally, most of the smart meters are either battery operated or directly connected to the mains. Both these supply method are not adequate, because batteries needs periodic maintenance, while connection to the mains needs specialized operators for the installation in residential, commercial or industrial buildings.

This work presents an innovative clamp-on energy-neutral smart meter designed both for mono- and three- phase non-invasive simultaneous measurement of voltage and current waveforms. It can be installed without temporary interruption of the supply, directly on the cable insulators: three clamp-on current transformers are used both for the current measurement and for harvesting the necessary energy to operate unattended theoretically for ever. Furthermore, innovative and robust voltage probes are introduced to measure voltage waveforms of the underneath wire without a direct connection to the copper wire. The system provides measurement of apparent power, active power, reactive power and power factor, with accuracy and performance comparable with those of professional instruments. Experimental results also demonstrate the autonomy of the small-size smart power meter presented.

The presented system is ready to use disaggregation techniques, like Non-intrusive Load Monitoring (NILM), a recent technique to analyze changes in the voltage and current consumptions of a household and retrieving fine-grain run-time information about what appliances are used with a break-down of the power consumption [3].

2 System Description

The block diagram of the system connected to a three-phase power line is presented in Fig. 1. A contactless capacitive-coupling voltage sensor is set around each of the three phase cables and around the neutral cable, while a contact-less inductive-coupling current sensor is applied around just each of the three phase lines. All the signals from the

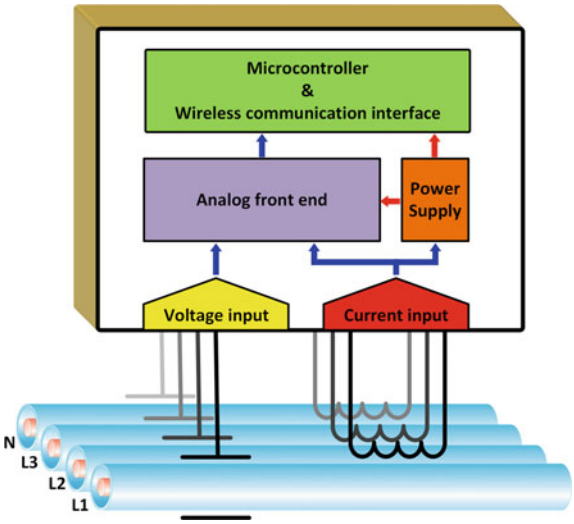

Fig. 1. Block diagram of the system block diagram of the system

voltage and current probes are filtered by an advanced analog front-end and then elaborated by a microcontroller capable of computing the voltage and current waveforms starting from the analog to digital conversion. The microcontroller calculates apparent power, active power, reactive power and power factor, and transmits the results wirelessly to a gateway using a IEEE 802.15.4 radio. Moreover, the split-coil transformers (SCT), needed as current sensors, are shared for harvesting the energy to the circuit, exploiting a switching system. This method permits to minimize the cost, without affecting the performance of the measurements, as demonstrated in [6,7].

The microcontroller is the 32-bit ultra-low power high-performance NXP JN5148 module, which features a 2.4 GHz IEEE 802.15.4 compliant radio transceiver. We implemented the transmission using the ZigBee PRO protocol with Home Automation profile to be compliant to any ZigBee gateway available on the market.

Figure 2 (top) shows The voltage sensor applied on each of the two wires in the case of a standard single-phase 230V AC power line. It is replicated for each couple L-N (i.e. L1-N, L2-N, L3-N) in case of the tree-phase version. The contact-less voltage probe consists of a small and thin copper film placed around the insulating sheath of the cable, thus creating a 2.5 cm-length cylindrical capacitor between the conductor inside the cable and the conductor film around it. Hence the differential input of the system is equivalent to two capacitors in series to the voltage signal, as shown in Fig. 2 (bottom).

The sensors of current, with a switch system controlled by the microcontroller, are used also to harvest energy from the line with the load under measurement during the sleep time, which lasts more than the measurement wake time. Since the system operates few measurements per minute and each measurement takes few milliseconds, most of the time is used to charge a supercapacitor which acts as energy buffer and powers the entire system. The circuit harvests the energy during the sleep time, through a bridge rectifier (which acts as an AC to DC converter) for each line; while the analog

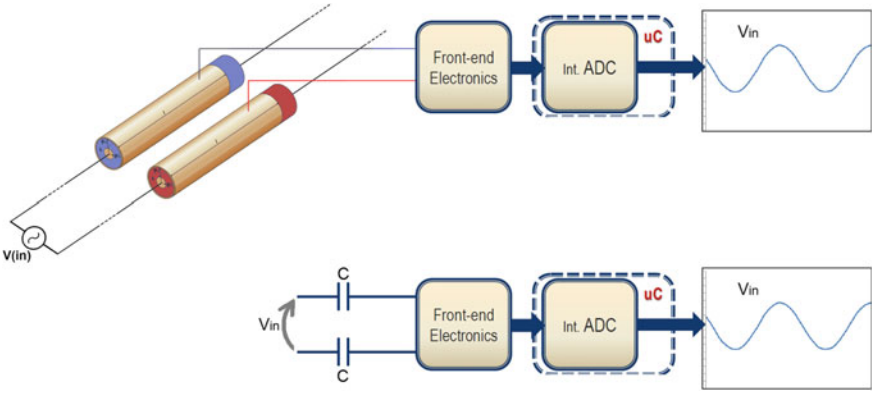

Fig. 2. Contact-less probes for voltage measurements, and equivalent model

front-end, the microcontroller and the radio are in ultra-low power mode or switched off.

To sample simultaneously all the voltage and current waveforms, and then getting accurate phase angle between them and obtaining a real three-phase measurement, we used the 14-bit low-power Linear Technology LTC1408 ADC, which permits to sample simultaneously six differential channels and convert signals at 600 ksps.

Voltage and current data are then sent via SPI to the MCU, which calculates the power features and sends reports via ZigBee radio.

It is important to note that this system can also be used with the three-phase in delta configuration (i.e. without the neutral cable), widespread in industrial scenarios.

Figure 3 shows a prototype of the three-phase smart meter described above. Notice how it is easy to clamp the cables with the voltage probes, avoiding any access to the internal wires.

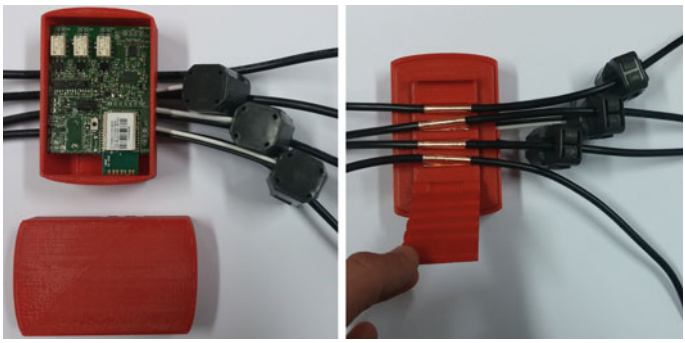

Fig. 3. The prototype of the three-phase smart meter in its case

3 Experimental Results

Experimental results for the voltage measuring system demonstrate the high accuracy of this measurement method, with maximum errors within 3%, as can be noted in Fig. 4, which shows the comparison between the voltage waveform of a single phase measured with a direct contact with the conductors of the cables using a professional instrument (i.e. Chauvin Arnoux CA8334B) and the voltage waveform measured using the contactless probe and analog front-end of the system presented above.

The accuracy in power quality analysis is even higher, with maximum errors $<2\%$, as shown in Table 1, which presents the results for the Power Factor measurement comparison for several kinds of loads.

The energy sustainability of the meter has been extensively demonstrated in [8,9]. The sleep time of the node can be characterized as a function of the load power dissi-

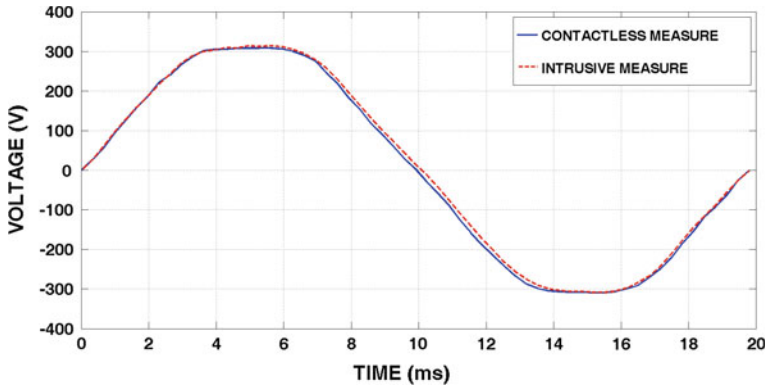

Fig. 4. Voltage measurement of the line (L1) of the three-phase plant. Comparison between a classic instrument which use a direct contact to the electric cable, and the presented contact-less probe

Table 1. Results for PF measurements, compared with the intrusive power meter measurements

	PF measured with our non-intrusive smart meter	PF measured with a professional instrumentation	Error (in%)
Load 1	0.9985	1.000	0.15
	0.9982	1.000	0.18
	0.9986	1.000	0.14
Load 2	0.6186	0.610	1.41
	0.6169	0.610	1.13
	0.6156	0.610	0.92
Load 3	0.4789	0.470	1.89
	0.4769	0.470	1.47
	0.4777	0.470	1.64

pation: the higher the power consumption of the load, the higher is the power harvested for the meter and then smaller is the minimum sleep time between consecutive measurements. Thus, the measurement rate (e.g. number of measurements every minute) is constrained by the load. Of course, data compression techniques [10] might help increasing the rate, but If the required measurement updates is too high, the meter will not meet an energy neutral balance and additional energy reservoirs are necessary.

4 Conclusion

We discussed the performance and the design of a non-invasive wireless smart meter with has contact-less probes both for current and for voltage measurements. The meter has been designed to be exploitable both for single-phase and three-phase power lines, it is safe and easy to install and is completely energy-neutral, thanks to an energy harvesting system that gets the energy needed for the measurements directly from the cables, in the same contact-less way. We demonstrated that the performance of the device is comparable with professional and intrusive measurement instruments, showing that errors are negligible.

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Signal Processing and Communications

Emerging Applications of Whispering Gallery Mode Photonic Resonators

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Abstract. Whispering Gallery Mode photonic resonators are emerging as key building blocks in many application fields especially because their resonant frequency is very sensitive to the variation of any physical or geometrical parameter. The basic properties and the applications of these resonators are discussed in this paper, with a specific attention to three very important application fields, i.e. Space, health-care, and environment monitoring.

Keywords: Integrated photonics · Photonic resonators · Gyroscopes · Biosensors

1 Introduction

Since several decades, photonics is considered a key enabling technology in many scientific/technological areas such as telecommunications, aerospace and defense, life science, health-care, and lighting. Typical advantages of the photonic systems over the competing technologies are low power consumption, small size/weight, electromagnetic interference immunity, and high transmission/processing speed.

The benefits of photonics could be exploited in several systems and components, conventionally implemented with microelectronic technologies, such as wireless networks, high-precision sensors, analog RF front-ends, analog-to-digital converters and so on. Furthermore, the functionalities of the photonic integrated circuits can be enhanced by integrating both electronic and photonic circuits in a monolithic or hybrid mode to realize complex electronic/photonic systems-on-chip.

Whispering Gallery Mode (WGM) photonic resonant cavities [1] with high ($>10^5$) and ultra-high ($>10^8$) quality Q-factor are currently the topic of an increasing research effort. They are now considered key building blocks in many photonic devices and circuits. Some of these components have already reached the commercialization stage, e.g. add-drop multiplexers and multi-analyte biosensing platforms.

In this paper, some recent advances in the field of WGM photonic resonators and their emerging applications in components to be potentially used in spacecraft engineering, medical diagnostics, and environmental monitoring, are discussed.

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2 Overview of Photonic WGM Resonators

In WGM resonators light is strongly confined within the structure, and high values of the Q-factor can be achieved when light absorbtion and/or scattering are minimized.

In several applications, compact size (small modal volume, V), high mode Q-factor (ratio between the energies stored and dissipated by the light in a optical cycle) and large free spectral range (FSR) (difference between two adjacent resonance peaks in the frequency domain) are required. A small footprint leads to a high integration density, a high Q-factor ensures a narrow resonance linewidth and a long decay time of the resonant mode. A wide FSR is important for reducing the crosstalk between the adjacent channels in wavelength division multiplexing (WDM) applications.

Several configurations of ultra-high Q-factor WGM resonant cavities with different shapes, i.e. truncated spheroid, microtorus, microsphere, wedge-resonator, have been reported in literature [2–5] for telecommunications, quantum electrodynamics and sensing applications. In 2007, Savchenkov et al. [2] demonstrated a calcium fluoride truncated spheroid with a Q factor of 3×10^{11}, that represents the state-of-the-art for the WGM resonators. In [3], an ultra-high Q-factor of 8.75×10^8 has been demonstrated in a wedge resonator with a diameter of 7.5 mm, for rotation sensing and microcombs applications. A silica microsphere resonator (diameter = 750 μm) with a Q-factor equal to 8×10^9 at about 633 nm has been proposed in [4]. Silica microtoroids have demonstrated both ultra-high Q-factors ($>10^6$) and small modal volumes, due to the additional transverse spatial confinement of the optical mode [5]. The key drawback of the above mentioned WGM resonators is the non-planarity, which limits the integration and, then, the realization of fully integrated photonic circuits.

Due to their easier fabrication process and the possibility of their monolithic/hybrid integration within complex photonic integrated circuits, planar ring resonators are usually preferred to the other class of WGM resonators. Ring resonators have been widely used in telecommunications, space, non linear optics, microwave photonics, and biological/chemical sensing with a Q-factor within some tens of millions.

The typical approach to enhance the Q-factor is the reduction of the waveguide propagation loss [6]. A record Q-factor of 10^7 has been recently demonstrated in a Si_3N_4 platform with propagation losses of only 0.1 dB/m [7]. The resonant device, with a radius equal to 9.65 mm, can be integrated in a hybrid way, with active devices, i.e. laser diodes, modulators, and photodiodes [8]. Ring resonators can be integrated with active components also through a monolithic approach based on an InP technological platform. Recently, a ring resonator based on a waveguide with propagation loss <0.5 dB/cm has demonstrated a Q-factor of about 10^6 [9, 10].

The performance of a standard ring resonator can be improved by slowing the resonant light. To achieve the slow light effect and an accurate control of the resonant mode group velocity, a dispersive structure such as a 1D photonic crystal (PhC) can be embedded in the ring. In fact, a 1D-PhC ring resonator (1D-PhCRR) [11] merges the properties of a conventional ring resonator with those of a PhC, achieving resonances at the edges of the band-gap with a Q factor up to 10^9 or more [12], which means at least two orders of magnitude higher than the values of a standard ring resonator.

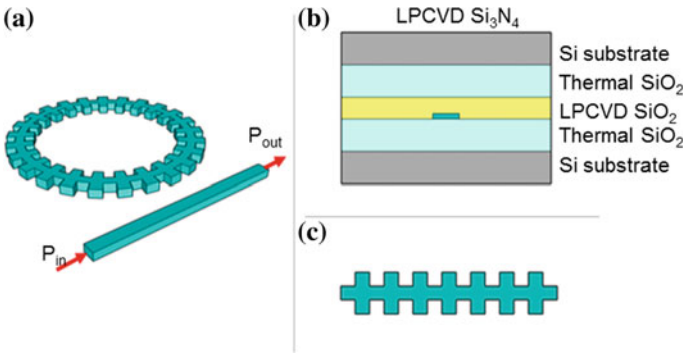

Fig. 1. **a** Configuration of the silicon nitride 1D-PhCRR. **b** Cross section of the Si_3N_4 waveguide. **c** Configuration of the sidewall grating. LPCVD: Low pressure chemical vapor deposition [15]

Several PhC configurations embedded in a ring resonant path have been proposed, such as air holes etched in the waveguide core [13] or periodic modulation of the waveguide width [14]. The main target applications of the reported 1D-PhCRRs are lasing, filtering in WDM telecommunications, and sensing.

Standard numerical methods, such as finite element method and finite difference time domain method, require high memory consumption and long simulation time when they are used for a numerical study of PhCRRs.

We have implemented a mathematical method for a robust and accurate analysis of 1D-PhCRRs [12]. The method significantly reduces the computation time and assures an accurate solution, taking into account all mode contributions in the coupling region. By using this mathematical method we have designed a 1D-PhCRR where the PhC is realized by modulating the waveguide width (Fig. 1). The waveguide is a 100 nm 2800 nm Si_3N_4 strip, as reported in [15]. The resonator, optimized at 1550 nm, has a footprint of 64 mm^2, an extinction ratio of 8 dB and a Q-factor of 10^9. This value is more than 100 times larger than the one of a conventional resonator of the same footprint.

3 Space Application

One of the most interesting applications of a high-Q ring resonators in the spacecraft engineering is as sensitive element in gyroscopes based on the Sagnac effect. A gyroscope measures the angular velocity, around a fixed axis, in an inertial reference system. In the inertial navigation systems, the real-time monitoring of the angular orientation, without referring to external landmarks, defines the current position relative to a known starting point. Inertial navigation systems are required for Attitude and Orbital Control Systems of satellites or for autonomous navigation of planetary rovers. For space applications accurate gyroscopes (resolution $\leq 10°/h$) are strongly demanded because small measurement errors can quickly become large position errors.

Resonant Micro-Optic Gyroscopes (RMOGs) [16, 17] are currently the topic of an increasing research effort focused on the demonstration of a small size (volume < 100 cm^3) devices, with a power consumption of a few Ws and with bias stability and resolution comparable to those of the bulky optical gyros currently used in almost all space missions, i.e. fiber optic gyros and ring laser gyros.

The sensing element of a RMOG is a ring resonator, where two counter-propagating resonant modes are excited. According to the Sagnac effect, the difference between the resonance frequencies of counter-propagating modes is proportional to the angular velocity. The main performance parameters are strongly influenced by the Q-factor of the resonator. For example, the sensor resolution, i.e. the minimum detectable angular velocity, is given by:

$$\delta\Omega = \frac{1}{Qd\sqrt{P_{PD}}}\sqrt{\frac{2hc^3}{\lambda_0 \eta \tau_{int}}} \tag{1}$$

with d the resonator diameter, Q the quality factor, λ_0 the operating wavelength, τ_{int} the integration time, P_{PD} the power at the photodetector, η the photodetector quantum efficiency, and h the Planck constant. In Table 1, the resolution estimated for the RMOG based on a Si_3N_4 1D-PhCRR [12] is summarized, assuming τ_{int} = 1 s, η = 0.9, P_{PD} = 1 mW.

Data in Table 1 show that by including a 1D-PhCRR with Q-factor > 10^9 within the RMOG, we can get a resolution < 0.01°/h with a ring radius < 10 mm.

Another possible space application of ultra-high Q-factor ring resonators is in the optical atomic clocks [18], which have attracted an increasing interest in the last years, thanks to their greater stability with respect to the conventional microwave atomic clocks. The complex system includes an ultra-stable laser with a linewidth of 1 Hz or less, and an optical frequency comb transforming the laser frequency into the radio frequency domain.

WGM resonators with ultra-high Q-factor can be used to implement the optical frequency comb. In 2014, Popp et al. [19] proposed a time-keeping system based on a 2 mm silica disk, which generates a comb spectrum with a 25 THz span. A frequency comb operating in the visible, that is based on a silicon nitride ring resonator, has been reported in [20]. The system uses the third-harmonic generation and third-order sum-frequency effects to convert the IR laser frequency comb in green light comb.

Table 1 Performance of the RMOG based on the 1D-PhCRR [12]

Radius (mm)	Footprint (cm^2)	ER (dB)	Q	Calculated resolution (°/h)
2	0.16	9.1	8×10^7	2.873
4	0.64	8.8	3.1×10^9	0.042
6	1.44	8.7	5.2×10^9	0.017
8	2.56	8.9	6.8×10^9	0.009
10	4	8.5	7.8×10^9	0.007

4 Health-Care and Environmental Applications

The detection of several analytes in a liquid sample without the need of labelling the target molecules is a highly demanded functionality in medical diagnostics, drug development, environmental monitoring, food quality control, and homeland security.

Label-free optical resonant sensors [21], which enable this functionality, are attracting an increasing research effort [22]. When the optical waveguide is properly functionalized, ring resonators can be used for implementing high resolution label-free sensors. The sensors operating principle is based on the highly selective binding between the target molecules dispersed in the solution surrounding the resonator and the molecules forming the functionalization adlayer on the surface of the resonator waveguide. Due to the binding, the adlayer thickness increases inducing a change in the mode effective index. The effective index variation can be accurately read out by real-time monitoring the resonance wavelength of the ring. The limit-of-detection (LOD), i.e. the minimum detectable analyte mass per unit area, of label-free ring resonator based sensors is inversely proportional to the resonator Q-factor [21, 23]. This means that a Q-factor increase induces an LOD enhancement. For example, we expect a LOD < 1 fg/mm^2 for a sensor based on the 1D-PhCRR with a Q-factor of the order of 10^9.

The simultaneous detection of properly selected sets of protein cancer biomarkers is another interesting application of label-free optical resonant sensors in medical diagnostics.

Recently a very sensitive label-free platform with LOD = 0.06 pg/mm^2 and resolution = 0.2 ng/mL based on five high-Q ring resonators has been designed [24]. The device target application is the early detection of the lung cancer by monitoring five protein biomarkers, i.e. Alpha-1 antitrypsin (A1AT), cytokeratin fragment 21–1 (Cyfra 21–1), insulin-like growth factor 1 (IGF1), regulated upon activation normal T cell expressed and secreted (RANTES), and alpha-fetoprotein (AFP).

The fast analysis of the drinking water with the identification of the dispersed pesticides traces is an emerging research topic in the field of environmental monitoring. The EU regulations set maximum allowable concentration values for several chemical substances in the drinking water. The total pesticide concentration limit is 500 ng/mL and for each pesticide the limit is 100 ng/mL. A sensing platform, such as in [24], could enable the fast and simultaneous detection of many pesticides in a small sample of water.

5 Conclusions

The main features and some application domains of WGM photonic resonators have been briefly reviewed. An innovative technique for enhancing the Q-factor of ring resonators by slowing the resonant light through 1D PhC strucures, has been presented. Some numerical results proving that this technique allows Q-factor values of the order of 10^9 have been reported. The potential of such ultra-high-Q ring resonators in space engineering, medical diagnostics and drinking water monitoring has been discussed. In the above-mentioned application domains the 1D-PhCRR allows the achievement of

system-level performance parameters that are not obtainable by the competing technologies. For example in the field of angular velocity sensing, the 1D-PhCRR could be the key element of a miniaturized gyro with a resolution < 0.01°/h. The MEMS competing technology, in which several miniaturized gyros have been demonstrated, enables a resolution several orders of magnitude worse.

The encouraging results on the 1D-PhCRR suggest the development of the first prototype of the resonant device aiming at experimentally demonstrate the first planar ring resonator with a Q-factor > 10^8.

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Compressive Sensing Reconstruction for Complex System: A Hardware/Software Approach

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Abstract. Today, a number of applications need to process large bandwidth signals. These applications frequently require the use of fast ADCs and very efficient DSP structures that are difficult to design. An interesting solution for facing these issues is the Compressive Sensing (CS) method, which, assuming to know some properties of the signal, allows to reduce the sampling rate well below the Nyquist rate. A negative aspect of CS is the need to introduce an additional element for the reconstruction the sampled signal. This reconstruction requires techniques that generally have an high computational cost, representing a critical element for a real-time implementation of CS systems. In this work we present the implementation of one of these reconstruction algorithms, named Orthogonal Matching Pursuit (OMP). This algorithm involves heavy computational cost (in particular for the matrix computation), which limits its use in the case of a strictly real-time applications, as in the case of radar systems. To overcome this limitation authors propose a solution that uses for the implementation a mixed software/hardware approach. The proposed architecture was implemented on the Xilinx ZYNQ FPGA. The experimental results show a significant speed-up of the algorithm.

Keywords: Compressive sensing · FPGA · Microprocessor · SOC · Hybrid architecture · Mixed hardware/software

1 Introduction

Nowadays, different systems (as radar and autonomous radio receivers systems) require to process signals with large bandwidth and with the real-time constraint. To fulfill these requirements fast analog to digital converters (frequently with conversion rate >1 Gsps) and very efficient DSP algorithms must be employed. However, it is difficult to design and realize high speed ADC, maintaining good quantization noise (it is directly related to the number of bits of ADC) and Spurious Free Dynamic Range (SFDR) performances. In this negative picture, a positive aspect is that often signals have characteristics that make them particularly suited to be sampled following the theory of compressive sensing (or sampling) (CS). This approach reduces dramatically the

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number of samples needed to reconstruct the signal (for example the echo signals in a radar application). Consequently, the performance of the ADC present in the front-end of the system can be relaxed.

In CS application the algorithm for the reconstruction of the signal has an important effect on the system performance. The complexity of this algorithm makes the task very critical for an effective implementation of CS. Signal reconstruction operation is used to recover the original signal from the CS sub-Nyquist sampled signal. This operation is complicated by the presence of matrix operations—e.g., multiplication of matrix by vector and inverse calculation. The complexity of these operations limited the matrix dimensions used in the reconstruction operations presented in the literature [1–5]. Moreover, most papers use off-line software processing while the hardware implementation of CS is proposed rarely. In this paper the authors propose to solve the issue of dealing with large matrix dimensions in CS reconstruction using an implementation based on a mixed hardware and software approach. The approach to use mixed hardware/software implementation for speeding-up critical operations has been already used by the authors for improving speed and/or power consumption in other applications, as described in [6–11]. The resulting architecture allows the real-time processing of big matrices, as required in different CS application, like radar systems [5]. The used platform is based on the Zynq FPGA Xilinx (ZC7Z020). The entire algorithm is split up in two parts; one runs on the microprocessor ARM cortex A9 and the other (the most critical one) on FPGA. The second part is the most critical, because it involves multiplication of matrices with several entries. For our architecture we consider a matrix with complex entries and a maximum dimension of 1000 rows and 100 columns. The reconstruction algorithm used is the Orthogonal Matching Pursuit (OMP) [12–14]. The following sections describe the algorithm structure. In Sect. 2 a brief description of Compressive Sensing is given, while in Sect. 3 the proposed solution is described and analyzed. The experimental results are reported in Sect. 4. Finally, in Sect. 5, the conclusions and the future works are presented.

2 A Brief Summary on Reconstruction Algorithm

The main idea behind this type of algorithm (see Fig. 1) is the following. Considering the acquired signal y, we search its projection on a set of vectors stored in the columns of a matrix (Φ). At each iteration we get the column of matrix Φ that is the most correlated with the vector of input y. The search ends when y is projected on a number of columns equal to the sparsity level m.

Summarizing, the inputs of the algorithm are [14]:

INPUT:

- A $N \times M$ measurement matrix Φ
- A N dimensional data vector y
- The m sparsity level of the signal

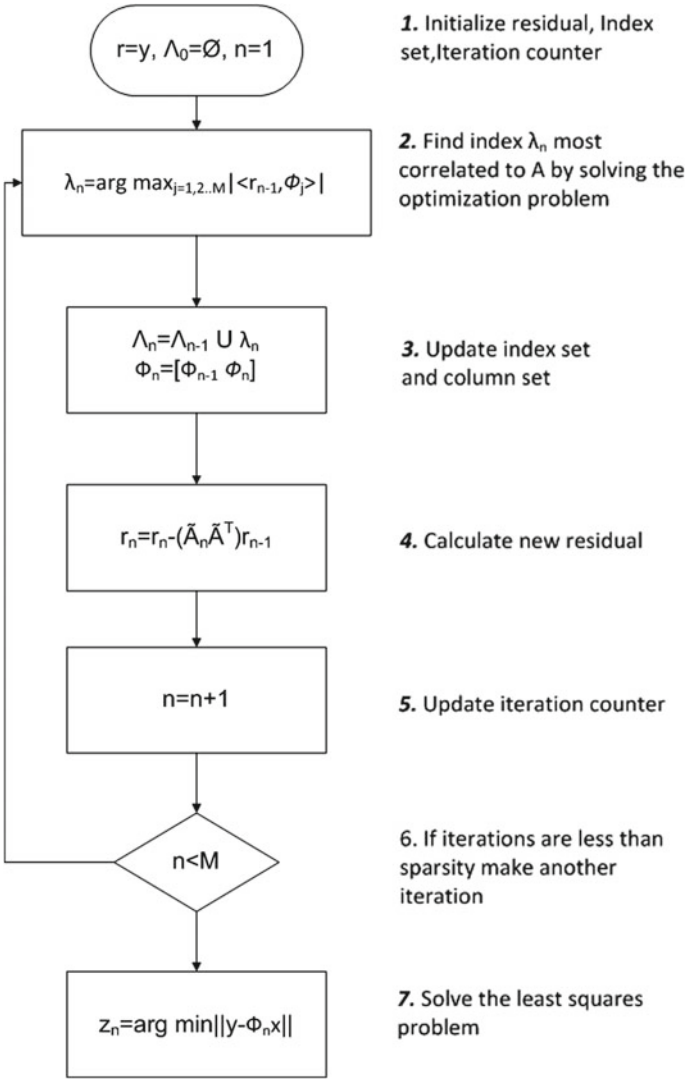

Fig. 1. The OMP architecture flow diagram

The outputs are:

OUTPUT:

- An estimate x for the ideal signal
- A set Λ_m containing m elements from $1 \ldots .M$
- A N dimensional approximation a_m of the data y
- A N dimensional residual $r_m = y - a_m$

The algorithm is then represented by following steps:

PROCEDURE:

1. Initialize the residual $r_0 = y$, the index set $\Lambda_0 = \oslash$ and the variable counter $n = 1$;
2. Find the index λ_n that solves the optimization problem $\lambda_n = argmax_{j=1,\ldots,M} |\langle r_{n-1}, \phi_j \rangle|$
3. Update the ensemble $\Lambda_n = \Lambda_{n-1} \cup \lambda_n$ and the column set $\Phi_n = [\Phi_{n-1}, \phi_n]$
4. Solve the least square problem to find $z_n = argmin||y - \Phi_n x||$
5. Calculate the new approximation of the data and the new residual $a_n = \Phi_n x_n$ and $r_n = y - a_n$
6. Increment n and go to the step 2 if it is less than m
7. The estimate x for signal has non zero indices at Λ_m.

3 OMP Algorithm Acceleration

Before to start with the architecture definition we performed a profiling of the software implementation of the algorithm. The estimation of the critical functions has been performed using the gprof profiler for the XILINX Zynq with a linux operating system.

Profiling results confirm that the 65% of the time is spent to compute the product between a complex vector and a complex matrix. In our experiments we have considered a complex matrix of dimension 1000×100 and a vector of 1000 elements.

As a consequence of the large dimensions of the matrix and considering that each complex multiplication requires 3 or 4 multipliers (depending on the used architectures) it is impossible to realize a full parallel hardware architecture on the Zynq (300000 or 400000 hardware multipliers will be required).

For this reason it was necessary to provide a hardware architecture capable of ensuring sufficient acceleration without requiring a such high number of multipliers.

These requirements have been met realizing a coprocessor for the matrix product that operates in the following way:

1. Divide the 1000×100 matrix in 10 sub-matrices of 100×100 entries, processed in different time
2. Processing each 100×100 sub-matrix using a pseudo parallel approach, performing 10 complex multiplication per clock cycle.

The coprocessor is able to perform a matrix by vector multiplication in $100 \times 10 = 1000$ clock cycles.

3.1 Hardware Implementation

The coprocessor architecture is composed by 4 main blocks (see Fig. 2). The "Scalar Product Block" performs the vector by matrix multiplication and represents the most complex unit in terms of hardware, meanwhile the other three blocks are used for storing matrix coefficients and for control. In particular the "Scalar Product block" is composed by 100 Complex Multiply and Accumulate units (CMAC) (see Fig. 3).

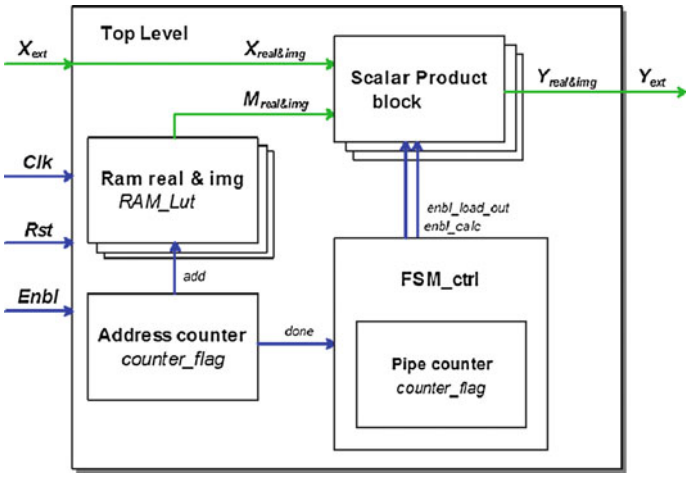

Fig. 2. Hardware accelerator architecture

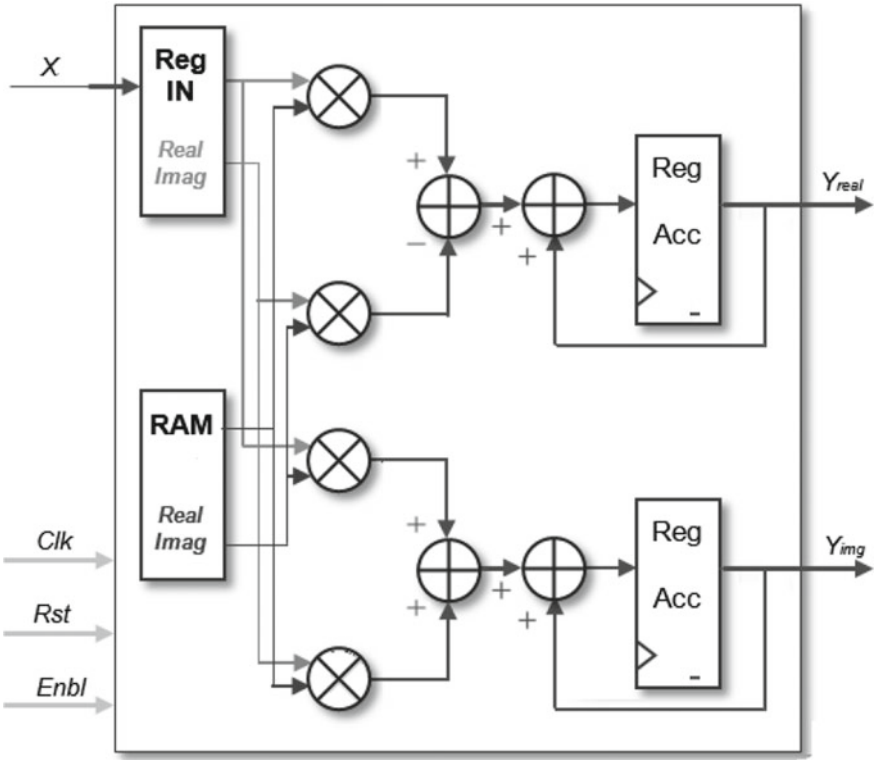

Fig. 3. Architecture of complex multiply and accumulator (CMAC)

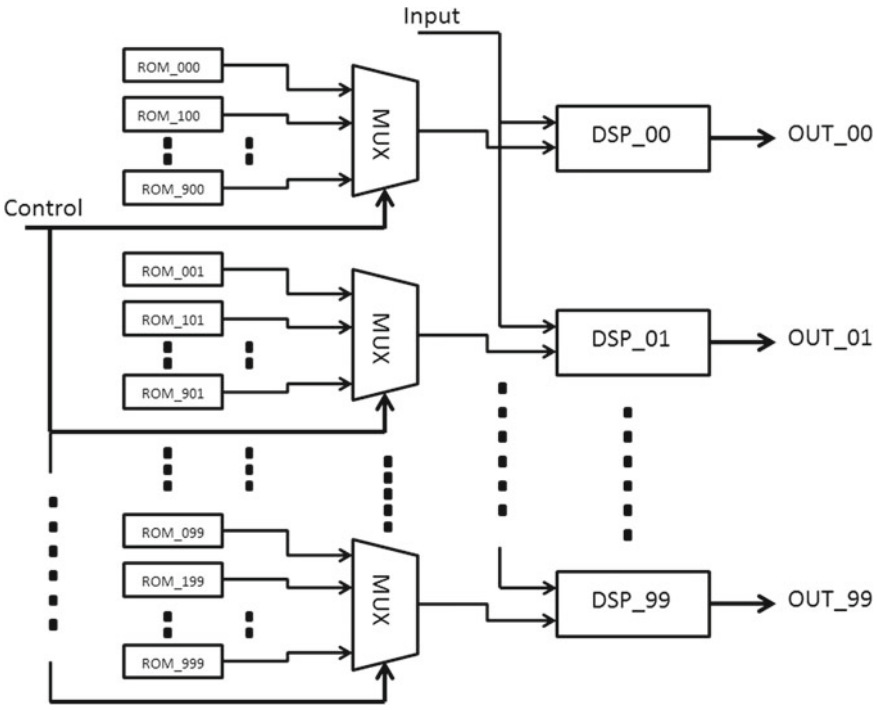

Fig. 4. Architecture implemented of scalar product block (SPB)

The data size in terms of number of bit of each component has been estimated by a fixed point MATLAB simulation of a radar system [5]. In our experiments the input and matrix coefficients are represented with 8 bit, while the outputs use 23 bits.

In Fig. 4 it is shown a more accurated block diagram of the coprocessor. Every complex multiply and accumulation (called DSP_i) performs a complex dot product between the matrix element and the input vector.

Sub-matrix coefficients are stored in ROMs and multiplexers are used to select the appropriate Sub-matrix.

4 Experimental Results

The entire coprocessor architecture has been described in VHDL. Synthesis and place and route have been performed using the VIVADO tool chain. Table 1 shows the implementation results with resources required for the implementation on a Zynq-7000 SOC (containing a FPGA programmable logic and a hardware ARM microprocessor). The FPGA layout (representing the used lines of routing) is shown in Fig. 5.

The above OMP algorithm was implemented on the Zedboard equipped with the mentioned Xilinx Zynq-7000. The programmable logic of Zynq-7000 contains 85 K of logic cells and 220 DSP block. The microprocessor in the SOC is an ARM cortex A9 with a maximum clock frequency of 660 MHz and 256 KB on chip memory.

Table 1. Resource utilization

Number of BUFGs	2 out of 32	6%
Number of DSP48E1s	208 out of 220	94%
Number of external IOBs	65 out of 125	52%
Number of OLOGICE2s	46 out of 200	23%
Number of RAMB18E1s	270 out of 280	96%
Number of slices	10506 out of 13300	78%
Number of slice LUTS	38374 out of 53200	72%
Number of slice LUT-flip flop pairs	39892 out of 53200	74%

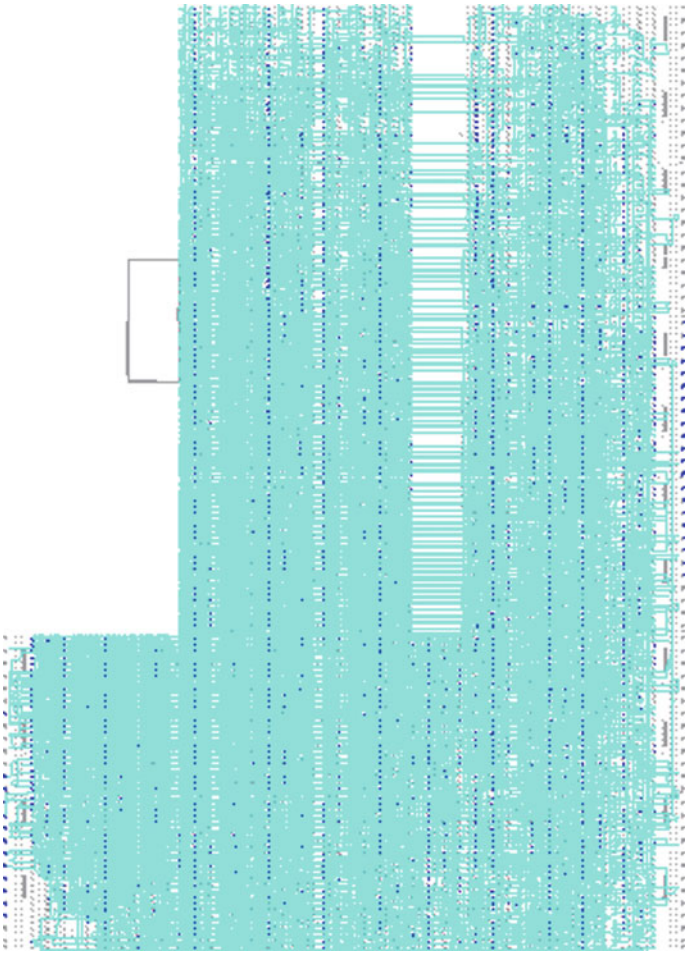

Fig. 5. System layout for the FPGA implementation

Table 2. Global performance

Frequency MHz	Clock cycle	Throughput MS/s
103	1000	300

Table 3. Estimated performance of acceleration

ARM 660 MHz	1.56 s
FPGA 103 MHz	9.629 µs
Speed up matrix	162 k
Speed up algorithm	2.92

Table 2 shows the experimental results obtained by the coprocessor performing a single Vector by Matrix product. These figures are obtained considering zero delay for the data transfer to the coprocessor.

In the Table 3 we show the obtained speed-up for the proposed architecture.

5 Conclusion and Future Works

This paper shows a mixed hardware/software approach for improving the performance of the OMP algorithm. This algorithm represents a bottleneck in the implementation of CS systems for high speed signals. The proposed architecture of the accelerator has been implemented on a SOC of new generation (containing a FPGA and a processor). The proposed solution is based on the use of a mixed hardware/software strategy for the implementation of the high-complexity matrix by vector multiplications. Experiments have permitted to evaluate the computation speed-up, supposing negligible the delay time needed for the transfer of the data from the FPGA to the processor. We obtained an hardware speedup for the matrix operations of about 162k, while for the complete algorithm the speedup is about 3.

Further experiments are underway for evaluating the speed-up of the matrix computation when we consider the effects of the transfer time between the processor and the programmable logic. Preliminary results show that the overall speedup is not degraded, a value of about 3 has been measured.

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Experimental Evaluation of 3D Ultrasound Palmprint Recognition Techniques Based on Curvature Methods and Under Skin Principal Lines

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Abstract. In this work, two procedures to extract 3D Palmprint features from a 3D ultrasound image of the human palm are presented and experimentally evaluated by using a database composed of 172 samples from 71 different users. Appreciable recognition results were found.

Keywords: Ultrasound imaging · 3D palmprint · Biometrics

1 Introduction

In the last years, the demand of automated systems based on person identification is increasing and, consequently, the importance of biometric systems is growing [1]. Multimodal biometric systems, which use more than one independent source of information to recognize individuals in order to improve recognition accuracy, have been successfully developed are more and more exploited in applications [2]. Among the other technologies, Ultrasound has shown several advantages, including the capabilities of proving a 3D representation of the biometric characteristics and of detecting life (Doppler mode).

Recently, the authors have experimented with the possibility to acquire a volume of the human hand or finger with a linear array. The technique has been exploited for extracting and evaluating different biometrics characteristics based on ultrasound by exploiting both piezoelectric and cMUT linear arrays: the internal hand geometry [3], hand vein pattern [4], fingerprint [5, 6] and palmprint [6, 7]. In a recent work [8], a new system for the acquisition of the ultrasound images is proposed; it is based on the open ultrasound platform ULA OP [9], which allows non standard and dedicated transmit/receive strategies and is able of providing a very quick acquisition. An improved automated system, which exploit a numeric controlled pantograph, is employed to guarantee stable and repeatable measurements. 3D images acquired with this systems have been elaborated and several kind of features that contain different 3D information of the palmprint were extracted [10, 11].

In this work, the whole biometric systems that is based on the fusion of all the different features is experimentally evaluated by exploiting a test database.

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2 Ultrasound Imaging

Ultrasound imaging is nowadays a well-established diagnostic technique in many biomedical applications. Basically, the image is achieved by sending an ultrasound pulse into tissue by using a piezoelectric or, more recently, cmut transducer (probe). The reflected echoes are recorded as an image. 3D ultrasound is a more sophisticated technique that is extensively used both in obstetric ultrasonography (during pregnancy) and in the non-destructive evaluation of materials for purity and failure assessment. The authors experimented with this technique for biometric recognition purposes.

The experimental setup used for getting 3D ultrasound palmprint images is shown in Fig. 1. The user's hand is properly aligned by some marks and is completely immersed in water with the palm facing upwards. The probe (LA435 by Esaote S.p.a., Italy) is tied on a numeric controlled pantograph. An advanced open platform for ultrasound research (ULA OP) [9] is employed as ultrasound imaging system. Both the pantograph and ULA OP are controlled in MATLAB environment (The Math Works, Inc., MA, USA). In order to acquire 3D ultrasound imaging data, the probe is shifted along the elevation direction while 250 B-mode images are one by one acquired and stored. With this technique, a 3D ultrasound image corresponding to a volume of $30 \times 50 \times 15$ mm^3 is acquired in about 5 s. The volumetric image is then reconstructed in post process by simply grouping the acquired B-mode images in a 3D matrix.

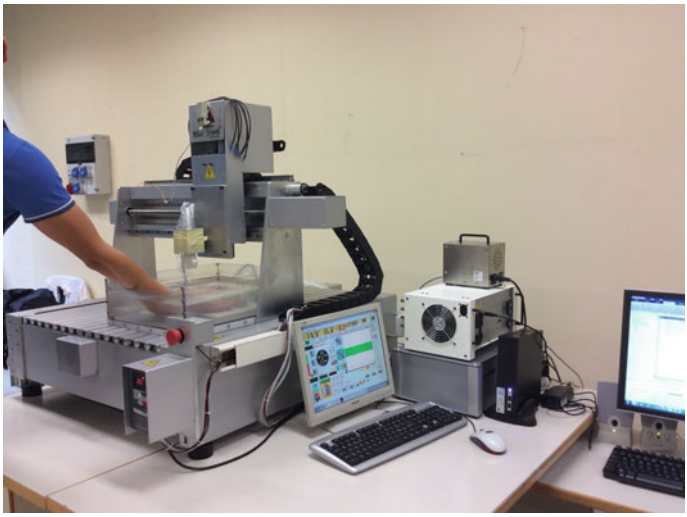

Fig. 1. A photo of the experimental set-up

3 Templates Extraction from 3D Information

An ad hoc software written in MATLAB code provides several renderings that allow to appreciate 3D information of the palmprint. As an example, Fig. 2a shows a 3D rendering of a portion of a human hand: the curvature of the palm together with the principal traits can be clearly appreciated. Figure 2b shows the extracted palm surface that can be used for applying curvature methods. 2D renderings, i.e., projections of the palmprint on a plane (2D palmprint) can be also achieved: Fig. 2c, d show two of such images at two different under skin depths. This is an important peculiarity of the ultrasound, which cannot be found in classical 2D optical palmprints; it can exploited to extract a template that contains 3D information of the principal lines as well.

3.1 Curvature Methods

A first recognition procedure is based on the analysis of the principal curvatures of palm surface, i.e., mean curvature image (MCI), Gaussian curvature image (GCI), and surface type (ST) [10, 12]. Mean and Gaussian curvatures are the most widely used measurements for surface classifications. As it is known, the signs of mean and Gaussian curvature yield nine basic STs. Figure 3 shows the templates obtained by extracting and post elaborating MCI (a), and GCI (b). Similar procedures were applied to the images representing the basic Surface Types. The resulting templates are shown in Fig. 4.

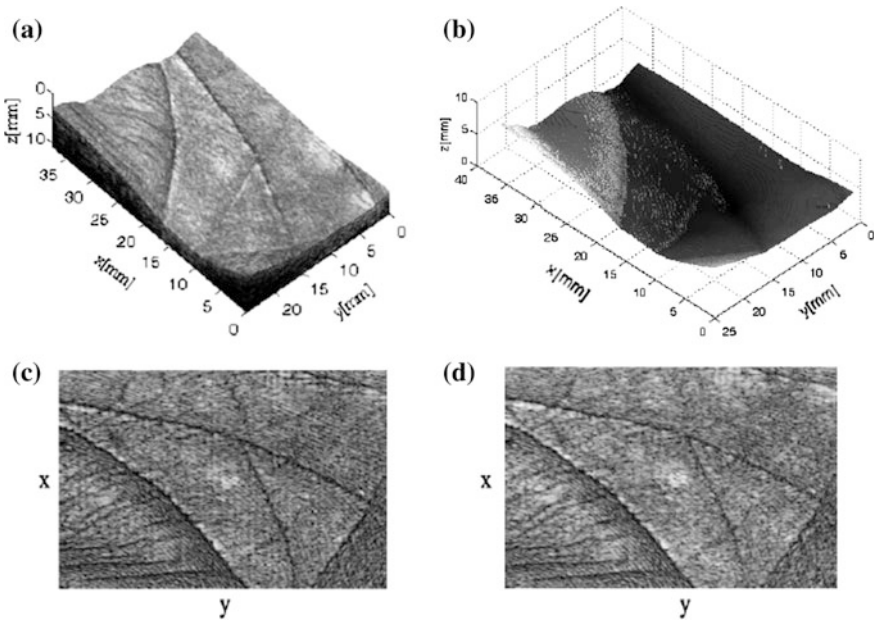

Fig. 2. Several renderings of the Palmprint: **a** 3D view, **b** extracted palm surface, **c** 2D palmprint at 0.03 mm and **d** 2D palmprint at 0.09 mm

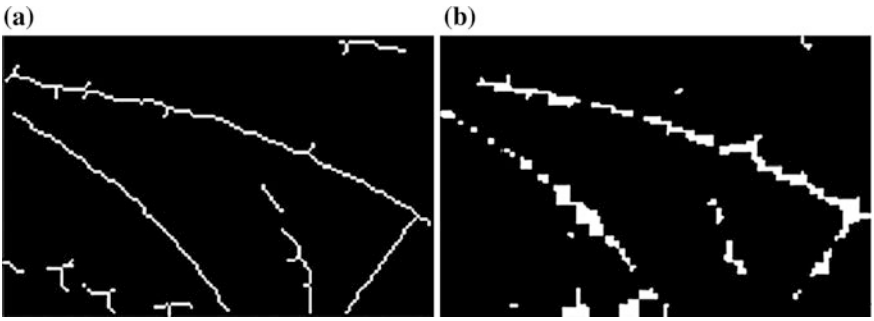

Fig. 3. **a** MCI and **b** GCI template images

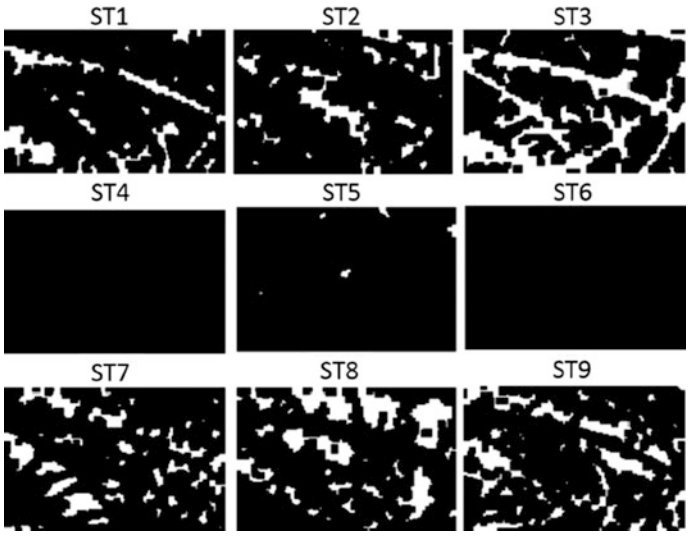

Fig. 4. STs template images

3.2 Under Skin Principal Lines

Another recognition procedure has been developed by exploiting a couple of 2D images acquired at different under skin depths. The images are merged and, successively, a templates that hence contain 3D information of the principal lines of the palm has been extracted [11]. Figure 5 shows the template extracted by combining the 2D images (ML) shown in Fig. 2c, d.

Fig. 5. Template of under skin principal lines

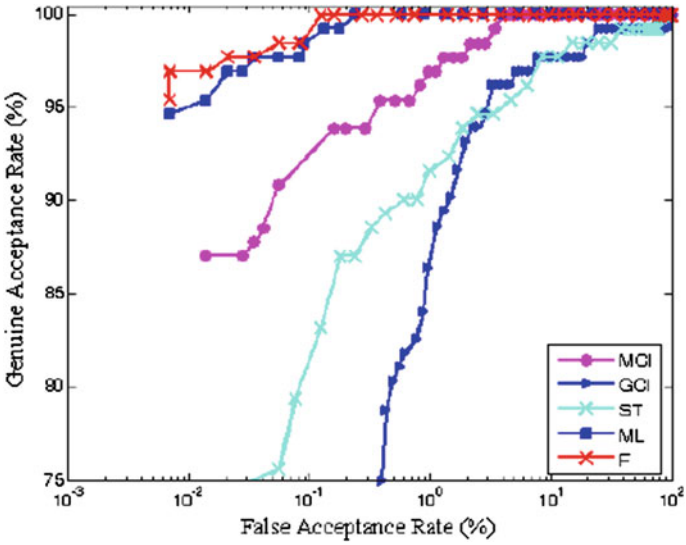

Fig. 6. ROC curves for the various features

4 Recognition Results

In order to provide a first evaluation of the proposed 3-D palmprint recognition system, an experimental database was established. The database contains 172 samples collected at two separate times from 41 volunteers and at three separate times from 30 more users. Experiments of verification have been performed exploiting this database. For all extracted features, the method used to implement the matching is the so called pixel-to-area matching [10, 11]. Figure 6 shows the receiver operating characteristic (ROC) curves for extracted features: MCI, GCI, ST and ML.

Table 1. EER for each feature

	MCI	GCI	ST	ML	F
EER	1.57%	2.89%	1.46%	0.25%	0.12%

A further possibility consists in fusing the four matching scores (MCI, GCI, ST e ML) and then taking the decision on the base of a fused score F, which is computed as in [10], Eq. 6, and its ROC Curve is add to Fig. 6. The EER values of MCI, GCI, ST, ML and F are summarized in Table 1.

5 Conclusion

In this work, an experimental evaluation of 3D Ultrasound Pamprint recognition technique has been performed. Results have shown that by fusing four independent features a quite good recognition rate can be achieved. Next work will be devoted to study new feature extraction and matching techniques to further improve recognition performance.

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RFID Eavesdropping Using SDR Platforms

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Abstract. Radio Frequency Identification (RFID) devices have been recently introduced in several applications and services such as National Identification Cards, Passports, Credit Cards, etc. In this paper, we investigate the security of such devices by showing the possibility of conducting RFID eavesdropping using simple and common devices such as a Software Defined Radio platform. Generally classical RF attacks can be made on long range transmission protocols, however we extend the standard RF attacks to cover RFID communication protocols. In this manuscript, an off-line step-by-step analysis is developed to prove the feasibility of reversing a complete RFID protocol. A real-time implementation is also realized to highlight a real threat in the everyday life.

Keywords: Software defined radio · Real time · Eavesdropping

1 Introduction

Radio-Frequency Identification (RFID) is a contactless use of Radio-Frequency (RF) electromagnetic fields to transfer data between a reader and a RFID tag. Nowadays, RFID is widely used in access control systems, public transports and stock control. RFID can be implemented in different technologies, however the widely used one is described by the standard ISO14443 [1]. Using sophisticated and expensive equipment, previous work demonstrates the vulnerability of this technology. Indeed, interception, decoy or jamming hacks of the "RFID air interface" demonstrate the weakness of systems using contactless chips [2]. Many studies have shown that encryption algorithms or sophisticated protocols can not completely guarantee the communication security between a reader and a RFID tag [3–5].

To prevent harmful attacks on RFID devices, various vulnerabilities should be clearly identified [4,5]. Many references in the literature describe in details these security holes, for example: The relay attack on credit card presented in [6] or the Mifare classic cloning tag attack presented in [7]. Due to their big number of varieties, RFID attacks can not be easily classified. However, the wireless RFID attacks can be mainly divided into two classes:

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- Passive attack: The attacker only intercepts the communication between a reader and a tag. Eavesdropping [8] or side-channel attacks (or side channel analysis) [9] are the most used passive attacks.
- Active attack: The attacker transmits radio signals in order to stimulate the tag. Activation or deactivation, skimming [10] emulation/spoofing [11] and relay [6] are often used to prove the insecurity of RFID.

In specific applications (such as digital distribution broadcast, similar to Google Play Store), smartphones can be used to carry out some attacks and therefore increase the threats of such attacks. However, Near Fiel Communication (NFC) chips implemented in smartphones make applications to become highly platform dependent. For example, applications running on new devices using NFC chip can't read classic tags (as Mifare classic tags); otherwise the NFC chip manufacturer should get the autorisation of NXP through the purchase of an additional license [12]. To be more efficient, a hacker should deploy a simple system that allows him to attack a large panel of applications independently of the target platform. To reach his goals, that attacker could develop his system using new technology called SDR (Software Defined Radio) along with development tools like gnuradio [13]. In fact, serval studies have recently shown that such devises can handle LTE applications [14], GPS [15, 16] or AIS spoofing [17], and ADS-B eavesdropping [18]. SDR and gnuradio can be used to easily inject smart hijacking codes in the communication protocol of target devices.

2 Reverse Engineering

In RFID passive applications, the reader generates a RF signal to activate the RFID tag who starts transmitting toward the reader its unique identifier code with useful data using a load modulation. In Near filed applications, when the distance between the reader and the device antennas becomes comparable to the carrier wavelength, an inductive coupling between the two antennas will exist. While in far filed applications, the two antennas are coupled using a radiative coupling. Different standards for RFID with respect to applications and distances are summarized in Table 1.

Most common cheap tags use Low or High Frequencies with inductive coupling. In this case, the reader (called Proximity Coupling Device (PCD)) establishes a magnetic

Table 1. RFID working range

Band	Coupling	Distance	Applications
LF: 125–135 kHz	Inductive	$<$10 cm	Animal identification
			Factory collection
HF: 13.56 MHz	Inductive	0.3–3 m	Credit card
			Transportation card
UHF: 865–956 MHz	Radiative	$<$10 m	Remote control Tracking
			International Article Number
MW: 2.4 MHz; 5.8 GHz	Radiative	$>$15 m	Electronic toll

coupling with the tag (called Proximity IC Card (PICC)) which enables us to power-up the passive tag and push this one to exchange data with the reader.

2.1 Attack Context

In modern societies, connected objects are invading our everyday life. These smart relatively small sensors will be deployed in outrageous number and they will exchange data among themselves using new network technology such as the Internet of the Things (IoT). Some of them will use a RFID technology. To demonstrate the concept of an eavesdropping attack on a RFID tag, we targeted in our experience RFID toys.[1] The targeted PICC toys "Rabbits" can exchange data with a computer through a PCD device called "mirror". In the original application, PCD is used to identify a PICC and trigger specific applications (such as reading a weather forecast or playing music).

2.2 Temporal Analysis

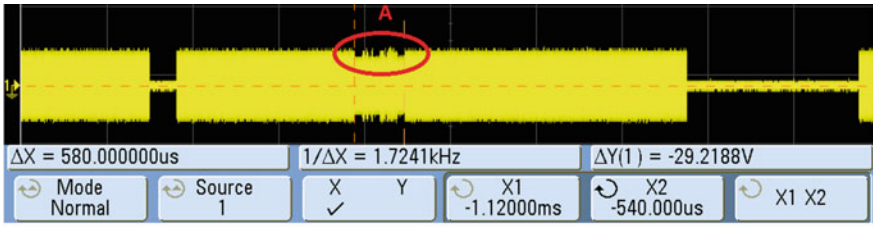
The signal shown in Fig. 1a was obtained without the presence of any tag. By making a zoom over the time axis, we can notice the existence of a simple carrier at $f_c = 13.56$ MHz which can be related to the RFID standard[2] ISO/IEC14443-2 [1]. According to that standard, PCD generates periodic scanning signals. Each scanning cycle can be divided into: an active simple carrier period (11.6 ms) (a part of this time is shown in Fig. 1a), a silence period of 300 µs, then the carrier is again activated before being periodically modulated during 580 µs (see the red circle A of Fig. 1a), after that the carrier will be again transmitted without any modulation and the cycle will be ended by another silence period of 1.8 ms.

After the modulation period A of the PCD (see Fig. 1b), a near PICC transmits its data by modulating the load of its antenna, see the red circle B of the same figure. The load modulation is generated using a subcarrier $f_{sub} = f_c/16 = 847.5$ kHz, as it is given by the standard [1]. The bandpass signal generated by the tag is the sum of two band-pass signals at $f_c - f_{sub} = 12.713$ MHz and $f_c + f_{sub} = 14.408$ MHz. We should mention the existante of two RFID standards ISO/IEC 14443-2 and ISO/IEC 15693 defined with two types of communication schemes, types A or B with the same carrier frequency $f_c = 13.6$ MHz and the same bit rate $D_b = 106$ kb/s. Each standard use a specific modulation as illustrated in Table 2. Type A uses On-off-keying (OOK). While type B uses an amplitude shift keying (ASK) modulation with an index of 10%. PICC modulates its data using a binary phase shift keying modulation (BPSK). Figures 1a, b show PCD → PICC transmission (in area A) using an ASK 10% and a subcarrier around 800 kHz, therefore so the used standard can be ISO/IEC 14443 (type B).

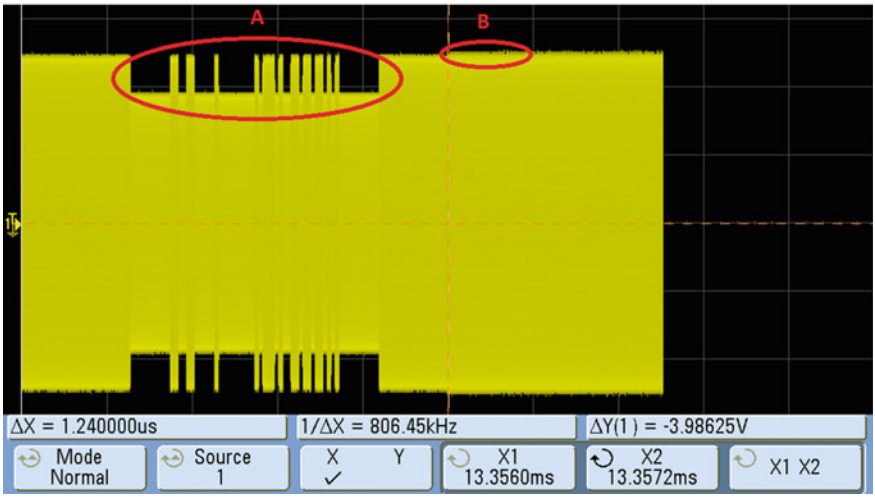
3 Platform Description

Our platform contents a RFID antenna, a Digital Video Broadcasting—Terrestrial (DVB-T) receiver, an upconverter and a computer with gnuradio [13]. Since we are using passive tags, the PICC signals are very weak, therefore a specific RFID antenna

[1] For further details on the used toys, see http://www.journaldulapin.com/tag/karotz.
[2] RFID and NFC standards are summarized in [5].



(a) Without tag



(b) With tag

Fig. 1. Scope observations

Table 2. RFID stabdard at 13.56 MHz

Standard	Type	Direction	Modulation	Line code	Subcarrier	Rate (kbps)
14443	A	PCD → PICC	ASK 100%	Miller	no	106
		PICC → PCD	ASK	Manchester	847.5 kHz	
	B	PCD → PICC	ASK 10%	NRZ	no	
		PICC → PCD	BPSK		847.5 kHz	
15693	Low	PCD → PICC	ASK 100 or 10%	8-PPM	no	1.65
		PICC → PCD	ASK or FSK	Manchester	**423**/485 kHz	6.62
	Fast	PCD → PICC	ASK 100% or 10%	2-PPM	no	26.5
		PICC → PCD	ASK or FSK	Manchester	**423**/485	

DLP-FANT was successfully introduced to eavesdrop PCD ↔ PICC communication. The DVB-T (R820T dongle from NooElec) is a common USB2 television tuner based on RTL2832u. Palosaari showed that this device can be used an a SDR platform. In our platform, we select the NooElec dongle. Using a chip Rafael Micro R820T, NooElec

dongle can sample a radio signal from 24 to 1766 MHz at 2.4 Msps over an USB2. It is worth mentioning that the RTL2832u device can not handle the 13.56 MHz RFID frequency because it is out side its range. To solve that problem, a frequency converter (*Ham It Up v1.2* from NooElec) has been used to upconvert the signal at 125 MHz. In spite of the 10 dB conversion loss measured with a vectorial network analyzer, the upconvertor can receive a strong PCD signal and a correct PICC signal.

4 RFID Eavesdropping: Signal Recording

Using the platform described in the previous section and the graphical tool *GNU Radio Companion* (*GRC*) software (in GRC, DVB-T devices is given as a source block), we recorded our signals. In our application, the central frequency has been set to the upper side band of PICC signal according to: $f_c + f_{sub} + f_{IF} = 13.56\,\text{MHz} + 847.5\,\text{kHz} + 125\,\text{MHz} = 139.4075$ MHz. Figure 2 shows a cyclic PCD signal registered and processed later on using Matlab. The Upper peaks grouped by three are the BPSK signal replies by PICC to PCD.

5 PICC Signal Demodulation

The spectrum of a PICC signal is shown in Fig. 3a, where a subcarrier is located at $f_{sub} = 847.6$ kHz with a BPSK bandwidth less than $\frac{D_{sym}}{2} = \frac{D_b}{2} = \frac{f_c/128}{2} \approx 53$ kHz. We considered an elementary time unit representing a symbol duration: $ETU = 1/D_b = 9.44\,\mu\text{s}$. A sampling frequency $f_s = 2.4$ MHz is used for the acquisition. The number of samples per symbol becomes $N_s = f_s/D_b \approx 23$. To reduce the computation

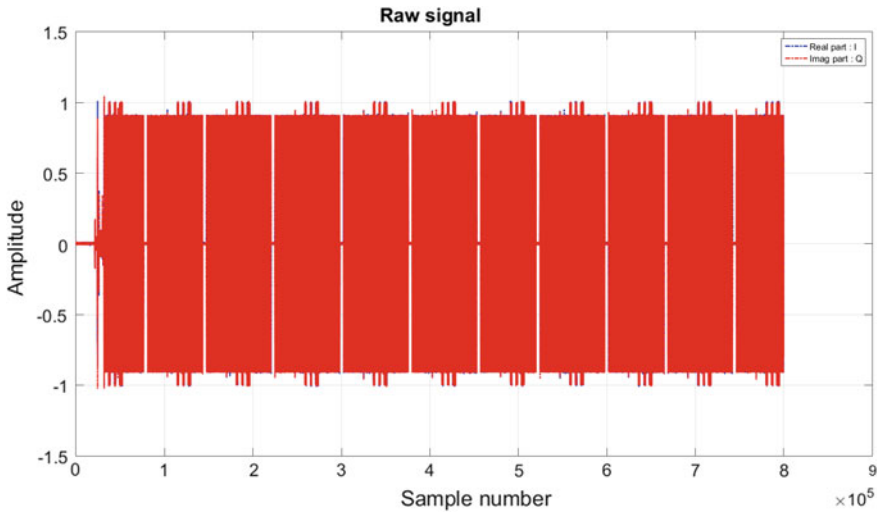
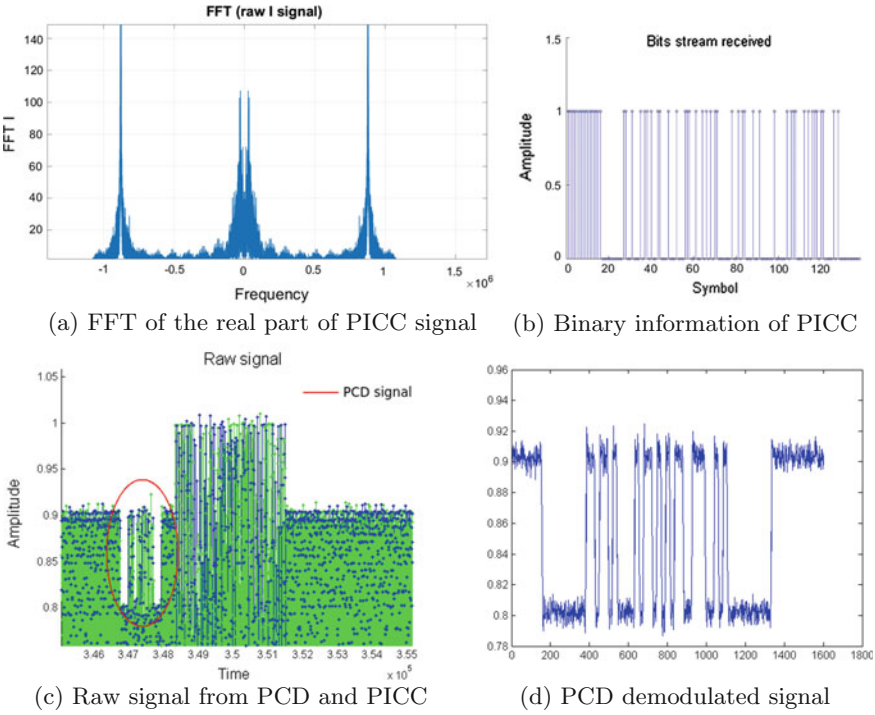


Fig. 2. Raw signal recorded with a GRC application



(a) FFT of the real part of PICC signal (b) Binary information of PICC

(c) Raw signal from PCD and PICC (d) PCD demodulated signal

Fig. 3. PICC Signal

time, one can reduce f_s to get a lower but suffisant N_s. The constellation of Fig. 3b contains the BPSK signal but suffering from a rotation artifact due unsynchronized carrier frequency. To synchronize the signal a Costas loop is used [19]. After processing, we obtained the final binary information with a phase ambiguity are illustrated in Fig. 3b.

6 PCD Signal Demodulation

To demodulate the PCD signal, we used similar techniques as done for the PICC signal. Figure 3c shows the ASK signal and the PICC response characterized by a higher amplitude due to the load modulation of the subcarrier. A frequency translation followed by a low pass filtering gives the signal of Fig. 3d. Using the latter signal and a simple thresholding procedure, one can obtain the binary data and reverse the complete protocol.

7 Conclusion

a RFID eavesdropping is successfully implemented using a low-cost hardware and an open source software. Moreover, we have shown that the association of Python or Matlab with gnuradio toolkit makes signal processing on physical radio signals very powerful and easy to prototype. Using similar procedure but more sophisticated tools such as

Wireshark, one can perform a GSM eavesdropping. In future work, it's expected to perform more complex RFID attacks on SDR platform. Our recent works shown that RFID attacks are easily portable to other SDR platforms. On the contrary of R820T, BladeRF or HackRF platforms can be easily used to perform a jamming. In future works, the feasibility of advanced attacks such as skimming or emulation will be explored. In the software radio community, these kinds of attack are viewed as a smart waveform because antenna, transceiver and terminal times are different. Thus, absolute, relative and immediate time concepts are crucial to manage smart waveform. Our coming work will focus on an API transceiver proposed by the WinnF.

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Non Destructive Ultrasound Equipment to Evaluate the Concrete Compressive Strength

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Abstract. Concrete is composed of sands, aggregates and cement powders mixed in water to produce a chemical reaction, named Hydration, that causes concrete hardening. The monitoring of the compressive strength during hydration is crucial to assess the concrete quality. The standard approach used to measure concrete strength consists of a manual and expensive process made by crushing concrete cubes in a compression machine. A non-destructive method based on monitoring the reflection coefficient of the ultrasound waves at the interface where the material is poured can replace the standard approach. In this work we present a system that embeds all the electronics needed for generating, acquiring and processing the ultrasound signal for automatically monitoring the concrete strength during and after the hydration process.

Keywords: Concrete strength · Cement · Ultrasound pulse wave · Hydration

1 Introduction

Monitoring the evolution of the mechanical properties of concrete is of high importance in building industries. The assessment of the compressive strength is widely used to evaluate the quality of the concrete. Standard approach consists of performing destructive compression tests on molded concrete specimens. Current test procedure needs the commitment of an operator, the automation is minimal and as consequences tests are expensive and time consuming. The application of non-destructive techniques can solve the problem, however, the evaluation of the compressive strength is a challenging task. Various techniques are currently in use: some focused on the heat release of the cement paste during the hydration process [1], others on conductivity of the concrete [2]. In this work an ultrasound electronic system capable of measuring mechanical properties of the concrete in site, is presented [3, 4]. The system, based on Ultrasound Pulse Echo Reflectometry (UPER) technique, uses the propagation of ultrasound waves inside the concrete to assess the acoustic properties. The measurement of the wave attenuation at the interface between concrete and a wave guide allows to measure the shear modulus G, and therefore the compressive strength σ, which is proportional to G^n [5–7].

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The proposed UPER system is fully programmable and embeds all of the electronics needed to manage the ultrasound signals, to store and transmit data to the host for estimating the shear modulus G of the concrete. Measurements performed by this system are compared to the standard approach for method validation.

2 The System

In the typical operation sequence the system is normally in power-down mode, to save power. A Real Time Clock (RTC) commands the wake-up of the system, and an Ultrasound Measurement Cycle (UMC) starts. During the UMC, the system fires an ultrasound bursts sequence at a period given by the Pulse Repetition Interval (PRI). The echoes are acquired and used for the measurement. After the measurement, the system goes back in sleep mode, waiting for another start. The UMC interval can be programmed between minutes-hours.

The UPER main board (UPER-MB) block scheme is depicted in Fig. 1. For each PRI the Ultrasound section, managed by Field Programmable Gate Array (FPGA) (Altera Cyclone III EP3C5F256I7) performs the measurement. During the transmission, an Arbitrary Wave Generator (AWG) integrated on the FPGA produces the digital samples of the sinusoidal burst, which are converted by a Digital to Analog Converter

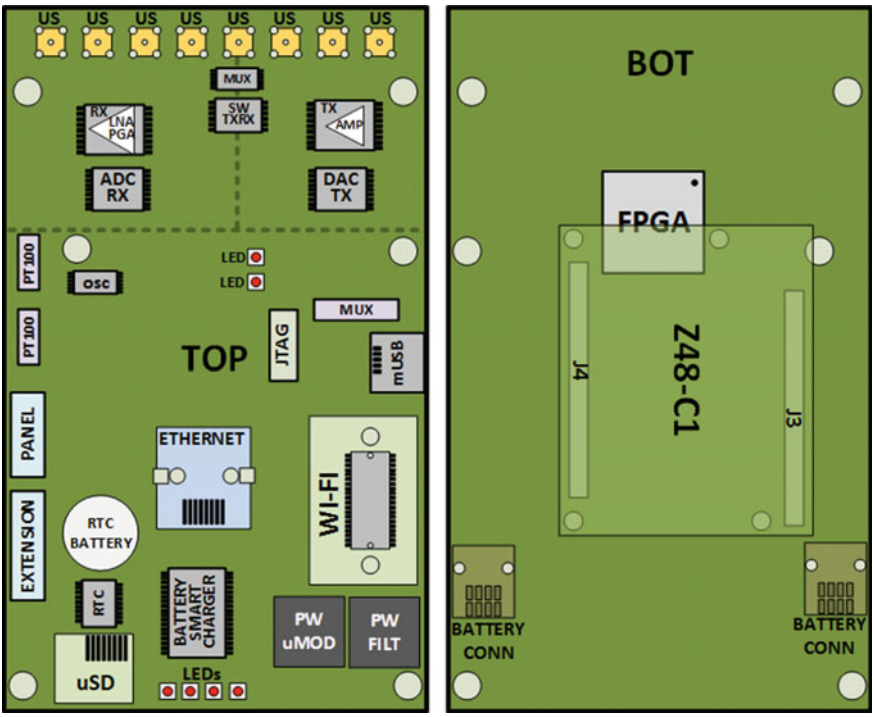

Fig. 1. UPER-MB block scheme

(ADC) at 75 Msps and amplified (TX AMP). After the transmission the front-end is commuted in reception (RX). The Tx section is disabled, the weak received echo is processed by a Low Noise Amplifier (LNA) followed by a Programmable Gain Amplifier (PGA). The amplified signal is converted by Analog to Digital Converter (ADC) at 75 Msps and acquired by the FPGA.

An analog switch connects Tx/Rx end of the chain to one out of eight different transducers connected to the board. This allows to carry out the measurements automatically in 8 different regions of the sample.

At the end of the UMC the FPGA sends the data to the microprocessor board (Schmidt Z48-C1), installed on the bottom of the UPER-MB. The Z48-C1 board is a mixed signal core module designed for industrial purposes and based on the ADSP-BF548 processor. It measures the temperature of the concrete by two temperature sensors PT-100 and manages a control panel and external multiplexer to expand further the number of available transducers. All measured data, (Temperatures and Ultrasound) can be stored in the µSD or sent to host for high level processing by a 100 Mbit Ethernet, Wi-Fi or USB connection. The power section can be connected to power supply or a Li-ION smart battery. A smart battery charger (Linear Technology LTC4100) manages and controls the charge of the battery. Furthermore, battery and charger share status and the charge parameters through System Management Bus (SMBus) with the FPGA and the Z48-C1.

Figure 2 shows the UPER-MB powered by a Li-ION battery. The main features of the UPER system are listened in Table 1.

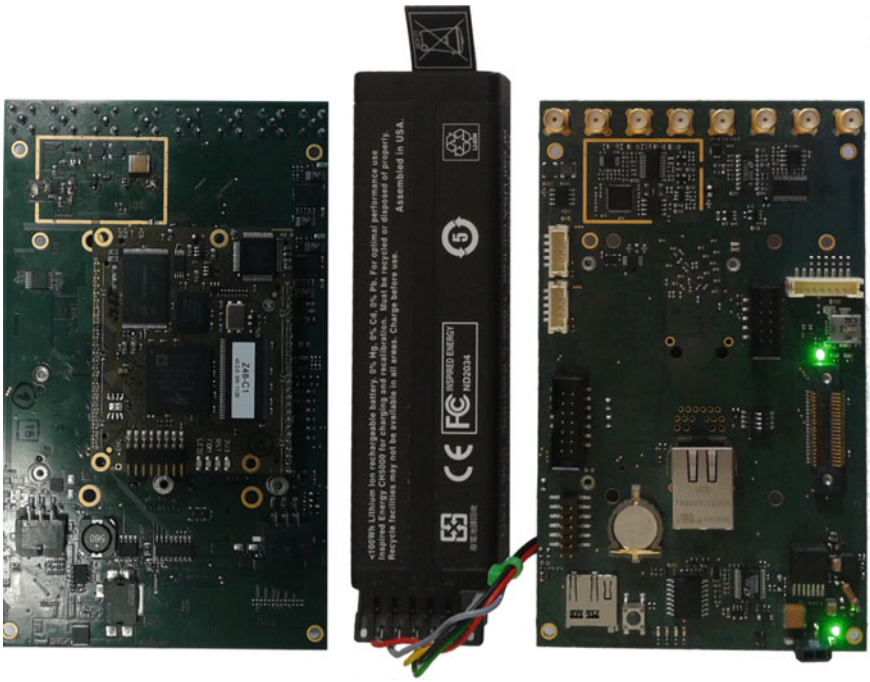

Fig. 2. UPER-MB powered by Inspired Energy Li-ION smart battery. *Bottom view* with Z48-C1 on the *left* and *top view* on the *right*

Table 1 UPER system Features

Features	Value
Tx channels	8, Multiplexed
Rx channels	8, Multiplexed
TX/RX freq.	0.7–5 MHz
Sampling frequency	75 Msps
TX voltage	5 Vpp
Supply voltage	10–24 Vcc Li-ION battery/Power supply
Power	5 W
Communication	Ethernet 100 Mbit, USB 1.0
Flash memory	μSD up to 64 MB
Dimension	15 × 9 cm

3 Experiments

The experimental setup is depicted in Fig. 3, it consists of transducer and a plexiglass wave guide. At the end of the guide the concrete sample is placed.

During the system set-up, the Ultrasound bursts are transmitted inside the wave guide in contact with air (without concrete). Since the acoustic impedance of the plexiglass Z_1 is much higher than the acoustic impedance of the air Z_a, the reflection coefficient is $r_{1a} = \frac{Z_a - Z_1}{Z_a + Z_1} \approx -1$. Therefore, the transmitted wave A_i is almost totally reflected in A_r and acquired back by the system. The measured amplitude of A_r can be considered the amplitude of the transmitted wave A_i, and is used as reference (see below).

Now the concrete sample is coupled to the plexiglass interface. The transducer transmits a new short burst of ultrasounds. The wave A_i travels through the wave guide until reaches the interface, where it is partially reflected (A_r), and partially transmitted in concrete (A_t). The reflected wave is received back by the transducer and acquired together with the flight time t_{f1}. The reflection coefficient r_{21} between concrete and wave-guide can be obtained by:

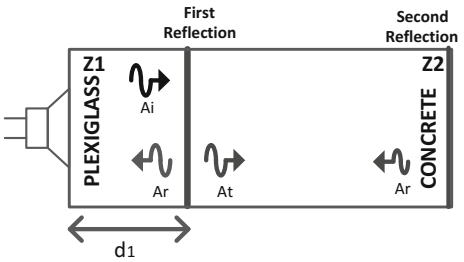

Fig. 3. Experimental setup: incident, transmitted and reflected waves

$$r_{21} = \frac{A_r}{A_i} \tag{1}$$

where A_r and A_i represents the amplitude of the received echo with and without concrete, respectively. The Impedance of plexiglass is Z_1:

$$Z_1 = \rho_1 v_1 = \frac{\rho_1}{t_{f1}} d_1 \tag{2}$$

where ρ_1 is the density of the Plexiglas and d_1 the length of the wave guide.

Finally, the Shear modulus of the concrete G_2 is obtained:

$$G_2 = \rho_2 v_2^2 = \rho_2 \frac{Z_2^2}{\rho_2^2} = \frac{Z_2^2}{\rho_2} = \frac{Z_1^2}{\rho_2} \left(\frac{1 - r_{21}}{1 + r_{21}}\right)^2 \tag{3}$$

where Z_2 and ρ_2 are the acoustical impedance and the density of the of the concrete.

Figure 4a shows the evolution of the strength measured with ultrasound, as a function of time for the concrete prepared with four different percentages of rounded aggregates. The measurements are made on the interface between the sample and the wave guide, with the ultrasound bursts at frequency f = 0.8 MHz.

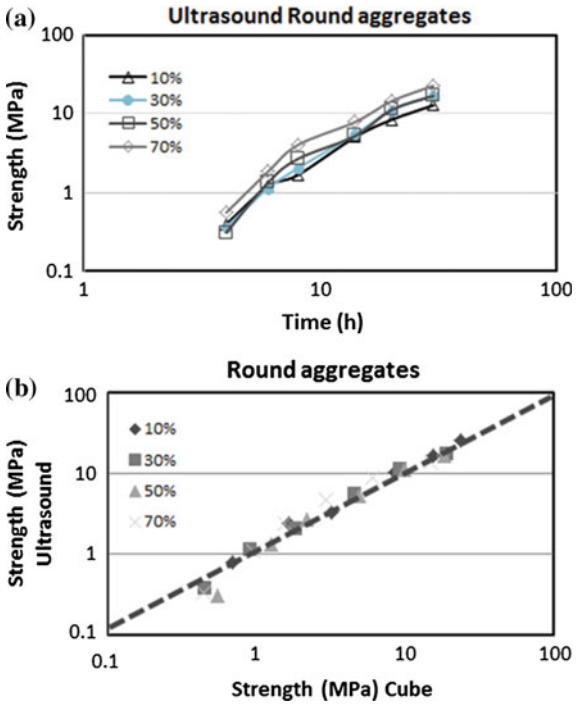

Fig. 4. **a** Evolution of the strength measured with ultrasound. **b** Direct comparison of the two type of measurements

Figure 4b shows a comparison of the strength measured with cubes and ultrasound, performed with different concentration of aggregates. The correlation is good for all concentrations except for the high content of aggregates (70%) where multi-scattering influences the measures and a difference of a factor of 1.6–1.8 is obtained.

4 Conclusion

The UPER system is capable to evaluate the strength of concrete by using the ultrasound wave reflection. The correlation with the classic approach is good except for the concrete with high content of aggregates where multi-scattering occurs. Thanks to the programmable architecture, managed by FPGA and the Z48-C1, the acquisition strategies are programmable and data can be stored and/or transmitted through wired and wireless communication protocol. These features, jointly with battery power supply, makes the system ideal for in-site industrial application. In-site measurements will be performed in the near future to evaluate the performances of the UPER system on industrial environment.

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Pulse Compression: From Radar to Real-Time Ultrasound Systems

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Abstract. Initially proposed for radar applications, pulse compression is a technique that enables the transmission of long coded pulses and matched filtering in reception in order to improve the range without sacrificing the resolution. Even if the effectiveness of pulse compression was demonstrated also for medical ultrasound systems, no details on the implementation of pulse compression methods in real-time imaging or Doppler systems using array probes have been presented for long time. In this work, the pulse compression technique was implemented in a low-cost research scanner and it is shown that it can be suitably used for both imaging and spectral Doppler investigations in real-time. An in vivo example is also presented, and it highlights that high SNR gain (up to 13 dB) can be obtained.

Keywords: Pulse compression · Ultrasound · Matched filtering · Chirp · Real-time

1 Introduction

Pulse compression is a classic technique, widely used in radar systems [1], to solve the apparent conflict between range and resolution in pulsed wave mode. In fact, when single-tone bursts are transmitted, the shorter their length, the better the resolution and the shorter the range. Conversely, pulse compression consists in the transmission of T-long "coded" pulses covering a wide bandwidth, B, centered at f_0. The received echo-pulses are sent to a matched filter, whose output is a pulse with reduced length ($1/B$) and signal-to-noise ratio (SNR) increased by a factor $B \times T$ (see Fig. 1).

Although the technique was introduced several years ago [2], for long time it has been actually used only in radar systems. The first implementations were in fact based on surface acoustic wave (SAW) devices for both generation of the transmission waveform and for matched filtering [3], and the cost of these devices discouraged an extensive application in other fields. Later, the introduction of powerful Digital Signal Processors (DSPs) and Field Programmable Gate Arrays (FPGAs) finally allowed the design and implementation of digital pulse compression systems at reasonable cost [4, 5].

Medical ultrasound echography is, in principle, an ideal field for the application of digital pulse compression methods [6]. Deep regions in the human body are typically investigated by transmitting long pulses that inherently involve poor resolution. Even though the possible advantages of coded transmission are evident [7–9], no details on the implementation of pulse compression methods in real-time imaging systems using array probes have been presented in the literature for long time. Even more surprising is

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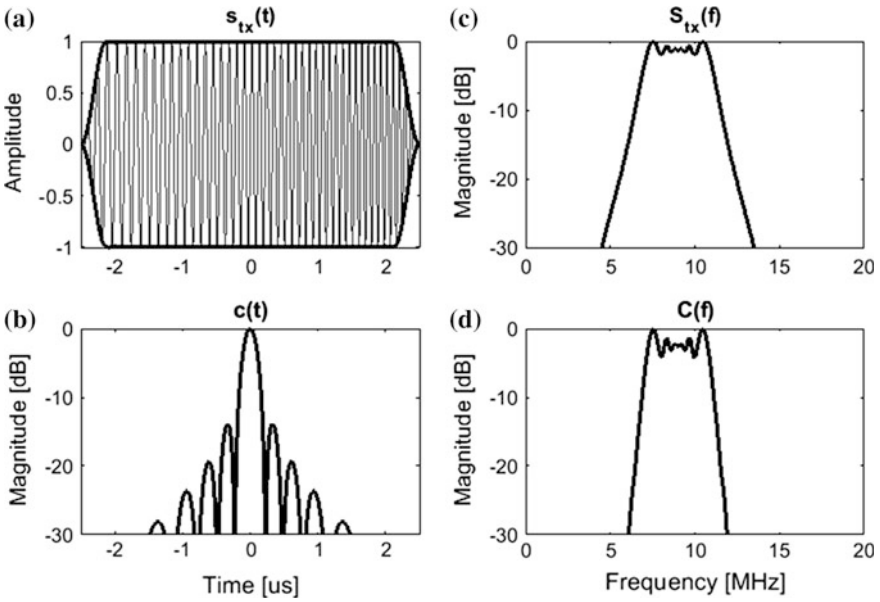

Fig. 1. Example of main waveforms and spectra involved in a pulse compression system. Typical TX signal (**a**) and related spectrum (**c**); compressed pulse (**b**) and related spectrum (**d**)

the situation in medical Doppler ultrasound, where the possible SNR improvement offered by pulse compression could be crucial to allow the visualization of blood flow in deeply located vessels [10].

In this paper, the implementation of the pulse compression technique in a low-cost research scanner (ULA-OP) is described and a sample comparative in vivo exam shows the effectiveness of pulse compression for both imaging and Doppler applications.

2 Methods

2.1 ULA-OP Real-Time Processing

Processing flow. In the ULA-OP system, the processing operations [11] are shared among the host PC, the onboard DSP (TMS320C6455, Texas Instruments, USA) and the FPGAs (Fig. 2). The software running on the PC controls the system and displays the elaboration results. During the set-up phase, the software synthesizes 64 transmission (TX) signals and transfers them to the ULA-OP memory.

Once ULA-OP is properly configured, one line of the scanned region is obtained in the following way. For each pulse repetition interval, the FPGAs read out the stored signals, which are amplified and channeled to the 64 active elements of a linear array probe. In reception (RX), the weak radiofrequency (RF) echo-signals received by the same elements are passed through low noise amplifiers, and sampled at 50 MSPS by 12-bit analog to digital converters. Four front-end FPGAs dynamically "beamform" (like in radar antenna arrays) the echoes by delaying, weighting and summing the

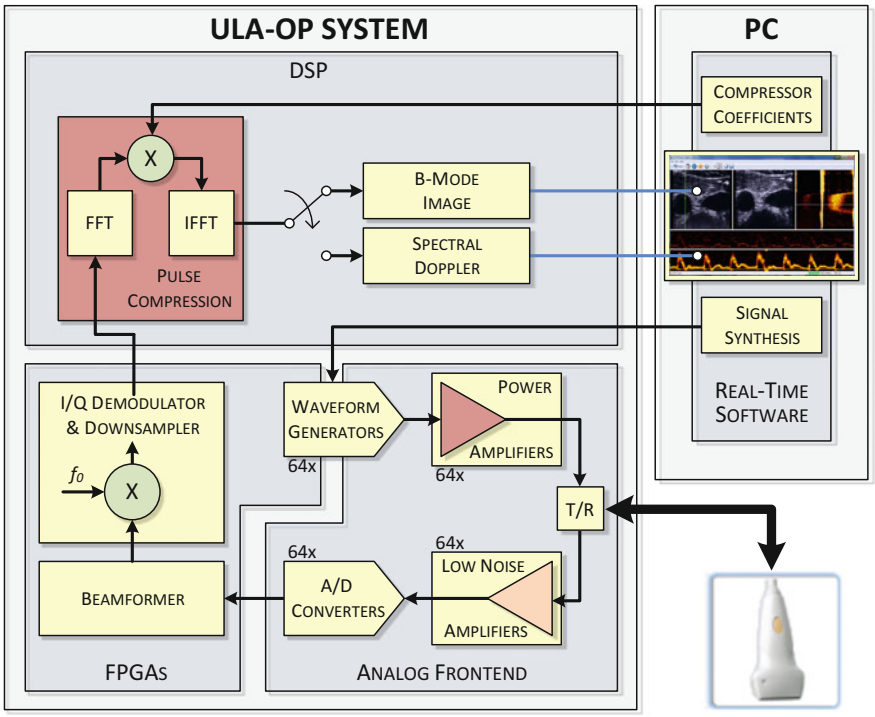

Fig. 2. Block-diagram of the real-time processing flow during pulse compression experiments

samples received by the 64 elements. A fifth FPGA coherently demodulates the beamformed RF signal, and down-samples the quadrature base-band components. The latter are elaborated by the DSP and the PC through the processing modules described below. Different lines of the region of interest may be scanned by using different groups of active elements.

Pulse compression module. The real-time pulse compression module, sketched in the red block of Fig. 2, runs on the ULA-OP DSP. The quadrature samples related to the same scan line are first passed through a complex 1024-point Fast Fourier Transform (FFT). The output data are multiplied by the complex coefficients of the compression filter, initialized by the PC in the DSP memory during the initial setup phase. Then, the DSP transforms the spectral data back to the time domain through a 1024-point Inverse FFT and selects the 512 valid output samples, thus completing the pulse compression operation.

The whole process is time critical and the DSP has to manage a large amount of data in real-time. For this reason, the code was hand-optimized by massive use of specific DSP functionalities (opcodes) that execute multiple operations in a single instruction, still maintaining 32-bit fixed point precision to maximize the accuracy.

B-Mode module. B-Mode images, representing the morphology of the area under exam, can be produced either by the compressed data or directly by the quadrature (uncompressed) data. The DSP processes each sample (corresponding to an image pixel) by logarithmically compressing the power of the signal. The logarithm is efficiently implemented by means of a DSP intrinsic instruction for the most significant part of the result, and by a 128-element look up table for the least significant part. The result is then thresholded and converted to a 256 gray-scale color map for display.

Multigate Spectral Doppler module. Likewise B-Mode, Multigate Spectral Doppler (MSD) [12] can be computed from the pulse compression processing chain or directly from the customary processing flow. First, the DSP reorders the samples in the external memories by the so-called corner-turning operation. Those complex samples are then processed through 128-point FFTs to produce real-time Doppler spectra related to one or multiple (up to 512) depths. The modules of the resulting spectra are displayed as spectrograms, i.e. the representation of the Doppler spectrum as it varies with time. When the spectral analysis is extended to multiple sample volumes, e.g. 512, an MSD frame is generated [13], and displayed by the host PC in a 512 × 128-pixel color-map.

2.2 Experimental Setup

In this application, the ULA-OP was linked to the LA533 linear-array (Esaote SpA, Florence, Italy), whose −6 dB bandwidth is between 3.5 and 13 MHz.

The ULA-OP system was programmed to interleave the transmission of 4 different pulses, two for B-Mode (with and without pulse compression) and two for Doppler mode (with and without pulse compression). The two signals used in each mode, i.e. a sine-burst and a frequency modulated linear chirp, had the same bandwidth and central frequency, see Table 1. The machine PRF was set to 10 kHz, so that the effective PRF for each mode, either B-Mode or Doppler, was 2.5 kHz. Two B-Mode images, two MSD frames, and the related sonograms were simultaneously displayed in real-time.

Table 1 Transmitted signal characteristics

Modes	Linear FM chirps		B (MHz)	f_0 (MHz)	Sine-Bursts	
	T (μs)	Tapering			Weighting	Number of cycles
B-mode	5	10% Tukey	2.7	8	Hamming	5.0
Doppler			3.2	7		4.0

3 Experimental Test

Figure 3 illustrates the ULA-OP real-time interface used during the in vivo scan of the abdominal aorta artery and the inferior vena cava of a healthy volunteer. The B-Mode images (Fig. 3a, b) show transverse sections of the two vessels. It may be observed that the typical B-Mode image (Fig. 3a) is affected by a low SNR, especially at higher depths where the signal almost merges with noise. On the contrary, the coded transmission (Fig. 3b) allows investigating the entire range of interest with good image quality (higher brightness and less noise). The estimated SNR gain due to pulse compression was here 13 dB [14].

Also for the spectrograms from the vessel center (Fig. 3e, f), it may be seen that the SNR obtained by pulse compression is clearly improved. The SNR gain, here estimated to be 10 dB [15], is also evident in the MSD images (Fig. 3c, d). While the SNR obtained with the transmission of the sine burst was not sufficient to properly examine the aorta (the velocity profiles are barely visible in Fig. 3c, e), the spectra in Fig. 3d, f are clearly detected and the profile shapes are well defined. More detailed and comprehensive experimental results are shown in [14, 15].

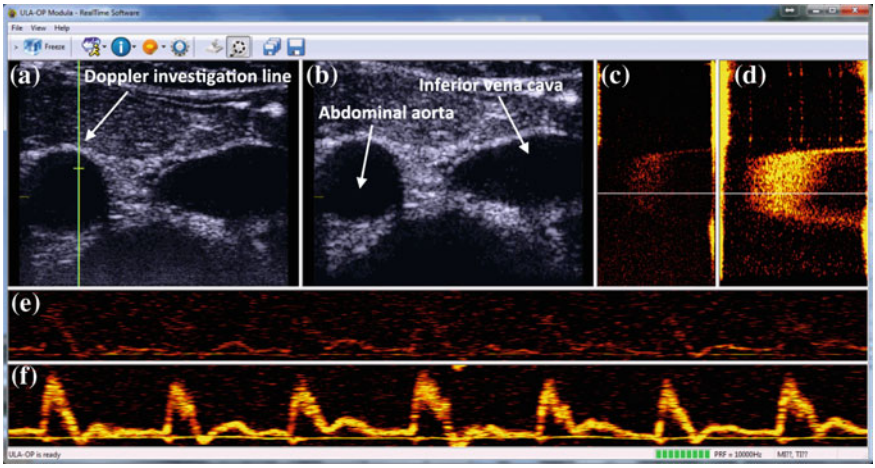

Fig. 3. ULA-OP real-time display frozen during the late systole. The B-mode images were obtained in conventional (**a**) and in pulse compression (**b**) mode. The *yellow line* highlights the Doppler investigation line. Multigate spectral Doppler frames obtained in conventional (**c**) and pulse compression (**d**) mode. Spectrograms (**e**, **f**) related to the depth selected through the *white cursor* in (**c**) and (**d**), respectively. The depth range was here 8–45 mm

4 Discussion and Conclusion

The availability of coded transmission and pulse compression was recently advertised in the description of some hi-end commercial systems for color Doppler imaging (iU22 by Philips Healthcare, and the ACUSON Sequoia 512 by Siemens Healthcare Germany), but no related technical information was given. At the best of our knowledge, this paper has shown, for the first time, that the pulse compression technique may be integrated in low-cost scanners, to be profitably used in both B-Mode and spectral Doppler applications. The proposed implementation operates on beamformed, demodulated and down-sampled data. Differently from the baseband time domain approach discussed and off-line evaluated in [16], the data processing is performed in real-time in the frequency domain. Each image line is obtained in final form (i.e. including suitable dynamic range compression) in only 19 μs. Hence, the single onboard DSP is sufficient to simultaneously perform pulse compression for B-Mode imaging and spectral Doppler applications, with SNR gain up to 13 dB.

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