YASUHISA OMURA

SOI LUBISTORS

LATERAL, UNIDIRECTIONAL, BIPOLAR-TYPE INSULATED-GATE TRANSISTORS

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Preface

In the fields of material science and device technology, the technical term of silicon-on-insulator technology refers to a very interesting system with a long history. In the 1970s, the silicon-on-insulator technology emerged as one of the pre-eminent multi-layer substrate concepts. Many variants were proposed, but most were never commercialized owing to crucial shortcomings in attributes such as reproducibility and qualification. Despite these problems, SIMOX (Separation by IMplanted OXygen), Unibond®, and ELTRAN® wafers are now commercially available.

Among device technologies, the partially depleted (PD) SOI MOSFET, the fully depleted (FD) SOI MOSFET, and the volume-inversion (VI) SOI MOSFET have been extensively studied. After the 1990s, FinFET and GAA MOSFET started to attract attention due to their benefits of intrinsic drivability and immunity to the short-channel effect. IBM successfully developed SOI processor LSIs and alliance companies developed the Cell chip. These LSIs use ESD protection devices for which the SOI device architecture is eminently suitable. One of the ESD protection devices is the SOI Lubistor (Lateral, Uni-directional, Bipolar-type, Insulated-gate transiSTOR); SOI LSIs with Lubistors are already being implemented in many products.

The SOI Lubistor is a pn-junction device and has various operation characteristics including macroscopic minority carrier injection, microscopic carrier recombination, and full quantum-mechanical behavior. I have continuously investigated the device physics of the SOI Lubistor since 1982, resulting in many technical papers. Even though it was invented 30 years ago, no one authorative source on the SOI Lubistor has emerged that can help engineers to understand fully the device physics of the SOI Lubistor. I believe that this book will be useful to device engineers, circuit engineers, and students aiming at future professional positions.

Finally, let me express my great thanks to my wife, Kikuyo, for her strong support over 35 years.

Yasuhisa Omura
Kanagawa, Japan
December 2012

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Introduction to an Exotic Device World

The point-contact junction structure was studied before World War II in order to realize a rectifier suitable for use in the receiver of a radio set. After n-type and p-type semiconductor materials such as Ge were discovered, the physics of the pn junction were extensively studied; research groups in Bell Laboratory provided outstanding contributions to the development of semiconductor technology, as is well known.

The invention of the transistor by Drs J. Bardeen, W.H. Brattain, and W. Shockley (later, the bipolar junction transistor, BJT) obviously introduced a new paradigm, the electronics industry of the United States of America.

On later import, the metal-oxide-semiconductor field-effect transistor (MOSFET) was successfully realized in the 1960s, and its complementary-type MOS (CMOS) circuit gave the worldwide electronics industry a new opportunity for expanding business activities. Today's Internet society has been built upon the wisdom generated by the foregoing scientists and technical staffs in many companies.

I commenced my research into CMOS technology in 1975 in NTT Communication Laboratories after graduating from the Graduate School of Applied Science, Kyushu University. The laboratory staff believed that the MOSFET would be a technology leader in the future and that the known scaling rule promised the appealing device technology to come. However, I was not so interested in the widely studied mainstream technology because I wished to open a new gate leading to a completely new field of device technology.

In 1980, I considered the possibility of subjecting bipolar currents to field-effect control as a result of solitary brainstorming. No published book even raised the possibility of this control. I suppose that nobody could imagine such a peculiar phenomenon because according to the conventional idea, such control is impossible in bulk substrates. One lucky break for me was the silicon-on-insulator (SOI) technology that was being studied in the laboratory; separation by implanted oxygen (SIMOX) technology proved to be the answer I needed! Dr K. Izumi invented the SIMOX technology in the 1970s in NTT Communication Laboratories; later, he was my boss from 1982 to 1996. In the 1980s, I and the collaborating staff in the laboratory successfully fabricated a 50-nm-thick mono-crystalline silicon film using the advanced SIMOX technology. My thought was that such a thin film would be useful in controlling bipolar currents. No book had suggested the concept of the lateral-field-based control of bipolar current because the insulated-gate field effect enables either type of carrier, not both types. However, I did not mind making this off-the-wall prediction because I considered that

the confinement of electrons and holes might yield a quasi-single-carrier transport or new recombination physics.

The first fabrication result was not very successful, but it gave me an important hint for the success of the following study; I summarized the fundamental operation of the device, named the Lubistor, based on the physical concept of the device in 1982. In an early stage of the study, I could not fully analyze its characteristics owing to the rather raw quality of the SIMOX substrates available in the 1980s. For a couple of years, I investigated the mysterious behavior of the Lubistor in detail; this study was not published for various reasons. However, through further experimental investigations in the 1980s, I was able to discover, in most part, the physics of the Lubistor. This is described in Chapter 5. For about 10 years after this work, I was unable to devote myself to further investigate the Lubistor owing to the obligations imposed by the laboratory.

I resumed the study in the 1990s after the restructuring of NTT Laboratories. In the 1990s, many scientists in the field of solid-state device physics became interested in nano-scale devices. The fabrication of thin-film Lubistors led me to a new stage in the advanced study of the Lubistor. The possibility that the forward-biased tunneling phenomenon could be found at the pn junction made me excited because it promised a new suite of Lubistor applications.

One surprise was the application of the Lubistor to the ESD protection circuit; IBM developed a Lubistor with an advanced device structure that could be applied to high-power devices. This was probably the real debut of the Lubistor (!) because it was implemented on the SOI processor LSI. I now frequently see the name ‘Lubistor’ in papers published in the field of optical communications; this suggests the next development in Lubistor application. I have provided a necessarily short history of the Lubistor. Although I have watched over the evolution of Lubistor technology, I look forward to being surprised at the exotic applications that might emerge in the next ten years.

In Part One, fundamental physics of pn-junction devices are summarized and advanced consideration is also addressed. Part Two discusses the physics and modeling of SOI Lubistors for the case of a thick-film device; of particular note, the original theory and model are introduced for the first time. In Part Two, the original behavior of the Lubistor stemming from the electric-field shielding layer is discussed along with the other behaviors of Lubistors fabricated on the buried insulator with an abrupt interface. Chapters 6 and 7 of Part Two, and all chapters of Parts Three to Seven, assume the use of a buried-oxide layer with an abrupt interface. In Part Three, the physics and modeling of SOI Lubistors are discussed for the case of thin-film devices. In Part Four, various circuit applications are demonstrated. Applications to ESD protection, the neural logic circuit, the voltage reference circuit, the conventional logic circuit, and the MOS gate-controlled bipolar action in the dynamic threshold SOI MOSFET are discussed. In Part Five, its recent application to the transmission mode tuning of photonic waveguides is introduced. In Part Six, some examples of SOI Lubistors being used as testing tools are reviewed. In Part Seven, the future of SOI Lubistors is briefly foretold.

Part One

Brief Review and Modern Applications of pn-Junction Devices

1

Concept of an Ideal pn Junction

As briefly described in the Introduction, Drs J. Bardeen and W. H. Brattain of Bell Laboratory discovered the amplification of signals by the point-contact transistor [1,2]. Within a few years, Dr W. Shockley developed the pn-junction-based bipolar transistor based on the physics of the pn junction [3].

Before the proposal of the bipolar junction transistor by Dr W. Shockley, many scientists had theoretically analyzed the role of electrons and holes in various semiconductors [4–6]; they used quantum mechanics to understand the potential of semiconductor materials. To acquire a comprehensive understanding of transport properties, many assumptions were introduced and the model of Ge-based pn junction characteristics was proposed. The basic assumptions are as follows:

1. All abrupt transitions in the depletion region, p-type, and n-type regions outside the depletion region are assumed to be quasi-neutral.
2. Carrier density (electrons and holes) outside the depletion region is described by the electrostatic potential difference between the quasi-neutral n-type and p-type regions.
3. A low injection level is assumed. The density of minority carriers injected from the counterpart region is negligibly small so that the local density of majority carriers is altered by the injection.
4. No generation and recombination current exists in the depletion region. The electron current and the hole current are constant across the depletion region.
5. The built-in potential and applied voltages are supported by a dipole layer with abrupt boundaries, not by the quasi-neutral n-type region or by the quasi p-type region.

The above assumptions make it possible easily to derive the so-called Shockley current equation [3]:

$$I_A = I_S\left[\exp\left(\frac{qV_A}{k_BT}\right) - 1\right], \tag{1.1}$$

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where I_S denotes the saturation current as a function of the diffusion constant and the minority carrier lifetime for electrons and holes. This equation is derived assuming that the junction current consists of the diffusion current components in the n-type and p-type regions outside the depletion region. V_A denotes the supply voltage applied to the diode terminals. Given the assumption of the recombination process in the depletion region, the theoretical calculation of a forward-biased junction current has to face a couple of difficulties. The usual solution is just simplification because the experimental current–voltage curve is roughly the same as the ideal in Equation (1.1). In order to match the experimental results, the above equation is modified to [7]

$$I_A = I_S\left[\exp\left(\frac{qV_A}{nk_BT}\right) - 1\right], \tag{1.2}$$

where n is the ideality factor that effectively takes account of the recombination process; n takes a value between 1 and 2. When the parasitic resistance of quasi-neutral regions (R_{pn}) is not neglected, Equation (1.2) must be rewritten as

$$I_A = I_S\left\{\exp\left[\frac{q(V_A - R_{pn}I_A)}{nk_BT}\right] - 1\right\}, \tag{1.3}$$

where V_A denotes the supply voltage applied to the diode terminals. This equation assumes that the parasitic resistance is almost constant. As this is a transcendental equation, numerical calculation is needed to obtain the current versus voltage characteristics.

As many engineers know, this equation is frequently used in analyzing the actual current characteristics of the Si-based pn-junction diode. A remaining issue is the expression of the saturation current (I_0) for the reverse-biased condition. In Equations (1.1) to (1.3), no generation and recombination current is assumed in the depletion region. In the presence of the generation and recombination phenomena, it is known that the junction current increases as the reverse bias voltage rises [7]. In a simplified approximation, this behavior of the pn junction can be integrated into the expression of I_0 [7]. The behavior of the pn junction under reverse bias is applied to the photodetector (p-*i*-n diode and avalanche photodiode), technologies that are familiar to the optical communication field [7]. Recently, the theoretical basis of the pn junction was reviewed in detail [8] in order to develop more reliable numerical simulations. In the following chapters, more realistic and advanced physics-based modeling is considered in order to assist consideration of the Lubistor operation mechanisms.

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2

Understanding the Non-ideal pn Junction – Theoretical Reconsideration

2.1 Introduction

Since the pn junction is fabricated classically by diffusion, the characteristics of the pn junction depend on the fabrication technique used [1]. The doping technique uses a specific impurity supplied by a solid source, a liquid source, or a gas source [1]. The diffusion of the impurity is sensitive to the semiconductor's quality because diffusion proceeds via vacancies to realize the atomic transfer mechanism. When the substrate has defects, diffusion is strongly affected by the defects; usually the diffusion constant increases [1].

The current characteristics of pn junctions that are fabricated by various techniques usually depart from those predicted by the ideal, shown by Equation (1.1) in the previous chapter, for a variety of reasons. Sometimes the lifetime of minority carriers is shorter than expected. In that case, engineers usually change the value of I_S because I_S is a function of the minority carrier lifetime of electrons and holes [2]. However, Equation (1.1) is not assured of reproducing measured results because the assumptions made for Equation (1.1) are overly simplistic. The physics critical to understanding the practical pn junction device are discussed here and in Part Two. How to reproduce the measured results precisely has been little discussed so far because empirical and optional changes to Equation (1.1) are commonly used to overcome the difficulty. Recently, Laux and Hess proposed an advanced theory to reproduce pn junction characteristics [3]. In constructing the circuit simulation model, they considered that the current equation can be expressed only by the diffusion current component. However, their simulation results reveal that the model works well as far as can be seen.

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2.2 Bulk pn-Junction Diode

2.2.1 Assumptions

Here I introduce new assumptions to analyze bulk pn-junction current characteristics. Figure 2.1 shows the schematic band diagram of a bulk pn-junction diode under forward bias; Figure 2.1(a) shows the band alignment assumed by Shockley [4] and Figure 2.1(b) the band alignment considered here. In Figure 2.1(a), the quasi-Fermi levels of electrons (E_{Fn}) and holes (E_{Fp}) in the quasi-neutral region are constant inside the depletion layer adjacent to the metallurgical junction, as Shockley assumed. On the other hand, they decline inside the depletion layer in Figure 2.1(b); it is assumed that the decline of the quasi-Fermi levels is due to the generation–recombination process of minority carriers. The subsequent theoretical calculation of the junction current is performed based on Figure 2.1(b).

In Figure 2.1(b), the quasi-Fermi levels (*imref*s), $\phi_{Fn}(x)$ for electrons and $\phi_{Fp}(x)$ for holes, are defined inside the depletion region and we have the following relations for them; that is,

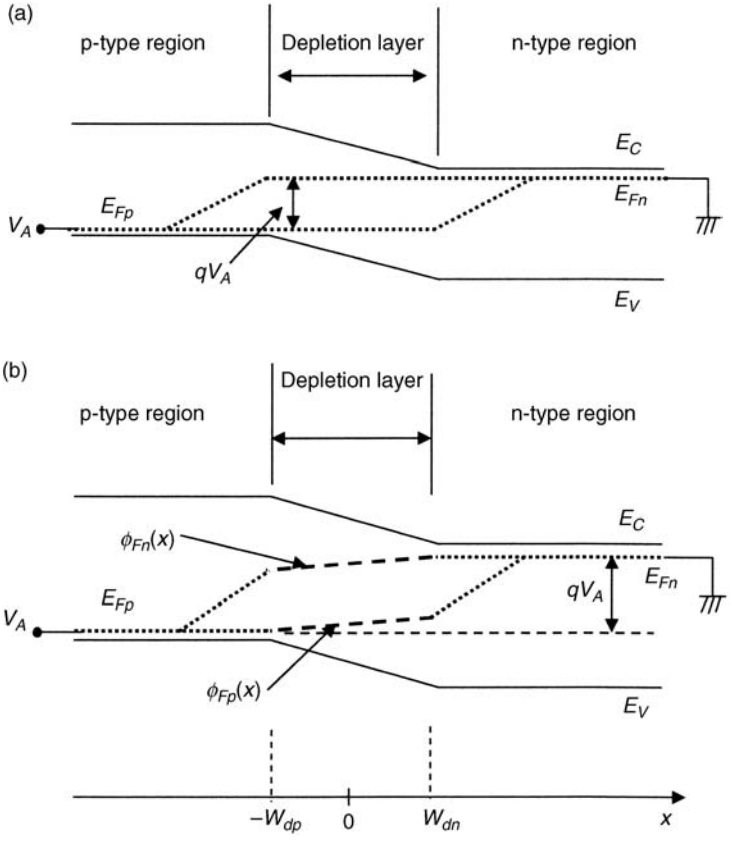

Figure 2.1 Schematic band models of the pn junction under the forward-biased condition. (a) Shockley model. (b) Advanced model.

here we assume that

$$\phi_{Fn}(x) = E_{Fn} + E_n(x) - \frac{\Delta_n(V_A)}{2}, \tag{2.1}$$

where

$$-\frac{\Delta_n(V_A)}{2} < E_n(x) < \frac{\Delta_n(V_A)}{2} \tag{2.2}$$

and

$$\phi_{Fp}(x) = E_{Fp} + E_p(x) + \frac{\Delta_p(V_A)}{2}, \tag{2.3}$$

where

$$-\frac{\Delta_p(V_A)}{2} < E_p(x) < \frac{\Delta_p(V_A)}{2}. \tag{2.4}$$

Here $E_n(x)$ and $E_p(x)$ give the effective variation in quasi-Fermi levels in the depletion layer, where $E_n(0) = E_p(0) = 0$; Δ_n and Δ_p are the maximal deviations of the quasi-Fermi levels and are functions of V_A.

When we follow the above model, an electric field induces the carrier drift in the depletion region. This means that we must start from the following continuity equation in order to derive an expression for the carrier density and current density of the pn junction. For the n-type region, we have

$$D_p \frac{d^2 p_n}{dx^2} - \mu_p F(x) \frac{dp_n}{dx} - \frac{p_n - p_{n0}}{\tau_p} - p_n \mu_p \frac{dF(x)}{dx} = 0. \tag{2.5}$$

The differential equation can be solved by taking the following two models, where, for simplicity, we assume the doping concentration of the n-type region (N_D) equals that of the p-type region (N_A).

2.2.2 *Model A – Low Doping Case*

1. Constant electric field in the depletion layer
   Here we assume that the local electric field ($F(x)$) primarily stems from the *imref* gradient because of the low loping condition. Given the constant electric field $F(x)$ for holes in the depletion layer, we have

$$F(x) = \frac{dE_p(x)}{qdx} = F_{D_p}, \tag{2.6}$$

   where F_{Dp} is the electric field due to the *imref* gradient of holes in the n-type region. It should be noted that F_{Dp} (and F_{Dn} later) is positive, in contrast to the negative space-charge-induced field. This electric field yields the drift current of carriers in the depletion region.

2. Neglecting the space-charge effect in the depletion layer
   The fourth term on the left-hand side of Equation (2.5) is neglected because of the low doping condition; the space-charge effect is not explicitly considered.

2.2.2.1 Solution with Model A

Equation (2.5) is reduced to the following equation inside the depletion layer:

$$D_p \frac{d^2 p_n}{dx^2} - \mu_p F_{Dp} \frac{dp_n}{dx} - \frac{p_n - p_{n0}}{\tau_p} = 0. \tag{2.7}$$

Assuming $Q = p_n - p_{n0}$, we have

$$\frac{d^2 Q}{dx^2} - \frac{\mu_p F_{Dp}}{D_p} \frac{dQ}{dx} - \frac{Q}{L_p^2} = 0, \tag{2.8}$$

where $L_p^2 = D_p \tau_p$. Under the low-field condition, we have the Einstein relation

$$D_p = \frac{k_B T}{q} \mu_p. \tag{2.9}$$

Thus Equation (2.8) is rewritten as

$$\frac{d^2 Q}{dx^2} - \frac{q F_{Dp}}{k_B T} \frac{dQ}{dx} - \frac{Q}{L_p^2} = 0. \tag{2.10}$$

Using the operator representation $(d/dx \equiv s)$, we have

$$s^2 - \frac{q F_{Dp}}{k_B T} s - \frac{1}{L_p^2} = 0. \tag{2.11}$$

Equation (2.11) yields the following solutions (α and β) for the operator:

$$\alpha_p = \frac{\dfrac{q F_{Dp}}{k_B T} + \sqrt{\left(\dfrac{q F_{Dp}}{k_B T}\right)^2 + \dfrac{4}{L_p^2}}}{2}, \tag{2.12a}$$

$$\beta_p = \frac{\dfrac{q F_{Dp}}{k_B T} - \sqrt{\left(\dfrac{q F_{D_p}}{k_B T}\right)^2 + \dfrac{4}{L_p^2}}}{2}. \tag{2.12b}$$

Here, $\alpha_p > 0$ and $\beta_p < 0$ according to Equation (2.6). The general solution for $p_n(x)$ is given by

$$p_n(x) - p_{n0} = C_1 \exp(\alpha_p x) + C_2 \exp(\beta_p x). \tag{2.13}$$

From Figure 2.1(b), each quasi-Fermi level deviates by Δ_n or Δ_p from the ideal one at the edges of the depletion layer. As it is expected that the *pn product* will hold its meaning, the

hole density at the edge of the depletion layer is expressed as

$$p_n(W_{dn}) = \frac{n_i^2}{n_n(W_{dn})} \exp\left(\frac{qV_A - \Delta_p}{k_B T}\right). \tag{2.14}$$

We also need to take account of the following boundary condition at $x = 0$:

$$p_n(0) = \frac{n_i^2}{n_n(0)} \exp\left(\frac{qV_A - \Delta_p/2}{k_B T}\right). \tag{2.15}$$

The two constants of Equation (2.13) should be determined for the above conditions. When we link Equation (2.13) to Equations (2.14) and (2.15), we have

$$C_1 = \frac{\dfrac{n_i^2}{n_n(W_{dn})} \exp\left(\dfrac{qV_A - \Delta_p}{k_B T}\right) - \dfrac{n_i^2}{n_n(0)} \exp\left(\dfrac{qV_A - \Delta_p/2}{k_B T}\right) \exp(\beta_p W_{dn}) + p_{n0}\left[\exp(\beta_p W_{dn}) - 1\right]}{\exp(\alpha_p W_{dn}) - \exp(\beta_p W_{dn})} \tag{2.16}$$

and

$$C_2 = \frac{\dfrac{n_i^2}{n_n(0)} \exp\left(\dfrac{qV_A - \Delta_p/2}{k_B T}\right) \exp(\alpha_p W_{dn}) - \dfrac{n_i^2}{n_n(W_{dn})} \exp\left(\dfrac{qV_A - \Delta_p}{k_B T}\right) + p_{n0}\left[1 - \exp(\alpha_p W_{dn})\right]}{\exp(\alpha_p W_{dn}) - \exp(\beta_p W_{dn})}. \tag{2.17}$$

Finally, we have

$$\begin{aligned} p_n(x) = {} & p_{n0} \\ & + \frac{\dfrac{n_i^2}{n_n(W_{dn})} \exp\left(\dfrac{qV_A - \Delta_p}{k_B T}\right) - \dfrac{n_i^2}{n_n(0)} \exp\left(\dfrac{qV_A - \Delta_p/2}{k_B T}\right) \exp(\beta_p W_{dn}) + p_{n0}\left[\exp(\beta_p W_{dn}) - 1\right]}{\exp(\alpha_p W_{dn}) - \exp(\beta_p W_{dn})} \exp(\alpha_p x) \\ & + \frac{\dfrac{n_i^2}{n_n(0)} \exp\left(\dfrac{qV_A - \Delta_p/2}{k_B T}\right) \exp(\alpha_p W_{dn}) - \dfrac{n_i^2}{n_n(W_{dn})} \exp\left(\dfrac{qV_A - \Delta_p}{k_B T}\right) + p_{n0}\left[1 - \exp(\alpha_p W_{dn})\right]}{\exp(\alpha_p W_{dn}) - \exp(\beta_p W_{dn})} \exp(\beta_p x). \end{aligned} \tag{2.18}$$

In the present model, the *imref* of holes is expressed as

$$\phi_{Fp}(x) = E_{Fp} + qF_{Dp}x + \frac{\Delta_p(V_A) W_{dp}}{W_{dp} + W_{dn}}. \tag{2.19}$$

Since we can assume that there exists no field at the edge of the depletion layer, we have

$$F_{Dp} = \frac{\Delta_p(V_A)}{q(W_{dp} + W_{dn})}. \tag{2.20}$$

Thus the *imref* of holes is, for $-W_{dp} < x < W_{dn}$, written as

$$\phi_{Fp}(x) = E_{Fp} + \frac{\Delta_p(V_A)}{W_{dp} + W_{dn}} x + \frac{\Delta_p(V_A) W_{dp}}{W_{dp} + W_{dn}}. \tag{2.21}$$

Finally, the hole current density (J_{pd}) in the depletion region is derived from Equations (2.18) and (2.20). Since the boundary conditions for two current components can be taken at $x=0$ because of current continuity, we have

$$J_{pd} = -qD_p\frac{dp_n(x)}{dx}\bigg|_{x=0} + q\mu_p p_n(0)F_{Dp}$$

$$= -qD_p\alpha_p\frac{\dfrac{n_i^2}{n_n(W_{dn})}\exp\left(\dfrac{qV_A-\Delta_p}{k_BT}\right) - \dfrac{n_i^2}{n_n(0)}\exp\left(\dfrac{qV_A-\Delta_p/2}{k_BT}\right)\exp(\beta_p W_{dn}) + p_{n0}\left[\exp(\beta_p W_{dn})-1\right]}{\exp(\alpha_p W_{dn})-\exp(\beta_p W_{dn})}$$

$$-qD_p\beta_p\frac{\dfrac{n_i^2}{n_n(0)}\exp\left(\dfrac{qV_A-\Delta_p/2}{k_BT}\right)\exp(\alpha_p W_{dn}) - \dfrac{n_i^2}{n_n(W_{dn})}\exp\left(\dfrac{qV_A-\Delta_p}{k_BT}\right) + p_{n0}\left[1-\exp(\alpha_p W_{dn})\right]}{\exp(\alpha_p W_{dn})-\exp(\beta_p W_{dn})}$$

$$+q\mu_p F_{Dp}\frac{n_i^2}{n_n(0)}\exp\left(\frac{qV_A-\Delta_p/2}{k_BT}\right). \tag{2.22}$$

In a similar manner, electron density $n_p(x)$ in the depletion layer of the p-type region is calculated as

$$n_p(x) = n_{p0}$$

$$+\frac{\dfrac{n_i^2}{p_p(-W_{dp})}\exp\left(\dfrac{qV_A-\Delta_n}{k_BT}\right) - \dfrac{n_i^2}{p_p(0)}\exp\left(\dfrac{qV_A-\Delta_n/2}{k_BT}\right)\exp(-\beta_n W_{dp}) + n_{p0}\left[\exp(-\beta_n W_{dp})-1\right]}{\exp(-\alpha_n W_{dp})-\exp(-\beta_n W_{dp})}\exp(\alpha_n x)$$

$$+\frac{\dfrac{n_i^2}{p_p(0)}\exp\left(\dfrac{qV_A-\Delta_n/2}{k_BT}\right)\exp(-\alpha_n W_{dp}) - \dfrac{n_i^2}{p_p(-W_{dp})}\exp\left(\dfrac{qV_A-\Delta_n}{k_BT}\right) + n_{p0}\left[1-\exp(-\alpha_n W_{dp})\right]}{\exp(-\alpha_n W_{dp})-\exp(-\beta_n W_{dp})}\exp(\beta_n x). \tag{2.23}$$

Similar to Equation (2.22), electron current density (J_{nd}) in the depletion layer is given by

$$J_{nd} = qD_n\frac{dn_p(x)}{dx}\bigg|_{x=0} + q\mu_n n_p(0)F_{Dn}$$

$$+\ qD_n\alpha_n\frac{\dfrac{n_i^2}{p_p(-W_{dp})}\exp\left(\dfrac{qV_A-\Delta_n}{k_BT}\right) - \dfrac{n_i^2}{p_p(0)}\exp\left(\dfrac{qV_A-\Delta_n/2}{k_BT}\right)\exp(-\beta_n W_{dp}) + n_{p0}\left[\exp(-\beta_n W_{dp})-1\right]}{\exp(-\alpha_n W_{dp})-\exp(-\beta_n W_{dp})}$$

$$+\ qD_n\beta_n\frac{\dfrac{n_i^2}{p_p(0)}\exp\left(\dfrac{qV_A-\Delta_n/2}{k_BT}\right)\exp(-\alpha_n W_{dp}) - \dfrac{n_i^2}{p_p(-W_{dp})}\exp\left(\dfrac{qV_A-\Delta_n}{k_BT}\right) + n_{p0}\left[1-\exp(-\alpha_n W_{dp})\right]}{\exp(-\alpha_n W_{dp})-\exp(-\beta_n W_{dp})}$$

$$+\ q\mu_n F_{Dn}\frac{n_i^2}{p_p(0)}\exp\left(\frac{qV_A-\Delta_n/2}{k_BT}\right), \tag{2.24}$$

where

$$\alpha_n = \frac{-\frac{qF_{Dn}}{k_BT} + \sqrt{\left(\frac{qF_{Dn}}{k_BT}\right)^2 + \frac{4}{L_n^2}}}{2} \tag{2.25a}$$

and

$$\beta_n = \frac{-\frac{qF_{Dn}}{k_BT} - \sqrt{\left(\frac{qF_{Dn}}{k_BT}\right)^2 + \frac{4}{L_n^2}}}{2}. \tag{2.25b}$$

The above electron and hole currents must be followed by the conventional diffusion current of minority carriers in the quasi-neutral region given that current continuity is maintained.

Finally, we address the current equation in the quasi-neutral region. In the quasi-neutral n-type region, the continuity equation for holes is given by

$$\frac{d^2p_n}{dx^2} - \frac{p_n - p_{n0}}{D_p\tau_p} = 0. \tag{2.26}$$

This equation must be solved while taking account of the boundary condition at the edge of the depletion layer, shown in Figure 2.1(b); according to Shockley's assumption, the effective potential difference at the edge of the depletion layer is given by $VA - \Delta p/q$. The hole density profile in the quasi-neutral n-type region is thus given by

$$p_n(x) = p_{n0} + p_{n0}\left[\exp\left(\frac{qV_A - \Delta_p(V_A)}{k_BT}\right) - 1\right]\exp\left(\frac{W_{dn} - x}{L_p}\right). \tag{2.27}$$

On the other hand, we can introduce parameter $p_n(W_{dn})$ using Equation (2.18) to obtain an expression of $p_n(x)$ in the quasi-neutral region. In that case, we have the following expression for $p_n(x)$ in the quasi-neutral region:

$$p_n(x) = p_{n0} + K_p(V_A, \Delta_p)\exp\left(\frac{W_{dn} - x}{L_p}\right), \tag{2.28}$$

where

$$K_p(V_A,\Delta_p) = \frac{\frac{n_i^2}{n_n(W_{dn})}\exp\left(\frac{qV_A-\Delta_p}{k_BT}\right) - \frac{n_i^2}{n_n(0)}\exp\left(\frac{qV_A-\Delta_p/2}{k_BT}\right)\exp(\beta_pW_{dn}) + p_{n0}\left[\exp(\beta_pW_{dn}) - 1\right]}{\exp(\alpha_pW_{dn}) - \exp(\beta_pW_{dn})}\exp(\alpha_pW_{dn})$$
$$+ \frac{\frac{n_i^2}{n_n(0)}\exp\left(\frac{qV_A-\Delta_p/2}{k_BT}\right)\exp(\alpha_pW_{dn}) - \frac{n_i^2}{n_n(W_{dn})}\exp\left(\frac{qV_A-\Delta_p}{k_BT}\right) + p_{n0}\left[1 - \exp(\alpha_pW_{dn})\right]}{\exp(\alpha_pW_{dn}) - \exp(\beta_pW_{dn})}\exp(\beta_pW_{dn}). \tag{2.29}$$

Since Equations (2.27) and (2.28) should be equivalent to each other, we can determine the value of Δ_p self-consistently.

In a similar manner, when Shockley's assumption is made, the electron density profile in the quasi-neutral p-type region is given by

$$n_p(x) = n_{p0} + n_{p0}\left\{\exp\left[\frac{qV_A - \Delta_n(V_A)}{k_BT}\right] - 1\right\}\exp\left(\frac{W_{dp} + x}{L_n}\right). \tag{2.30}$$

In addition, we also have the following optional expression for $n_p(x)$ in the quasi-neutral region:

$$n_p(x) = n_{p0} + K_n(V_A, \Delta_n)\exp\left(\frac{W_{dp} + x}{L_n}\right), \tag{2.31}$$

where

$$K_n(V_A, \Delta_n) =$$

$$\frac{\frac{n_i^2}{p_p(-W_{dp})}\exp\left(\frac{qV_A - \Delta_n}{k_BT}\right) - \frac{n_i^2}{p_p(0)}\exp\left(\frac{qV_A - \Delta_n/2}{k_BT}\right)\exp\left(-\beta_n W_{dp}\right) + n_{p0}\left[\exp\left(-\beta_n W_{dp}\right) - 1\right]}{\exp\left(-\alpha_n W_{dp}\right) - \exp\left(-\beta_n W_{dp}\right)}\exp\left(\alpha_n W_{dp}\right)$$

$$+\frac{\frac{n_i^2}{p_p(0)}\exp\left(\frac{qV_A - \Delta_n/2}{k_BT}\right)\exp\left(-\alpha_n W_{dp}\right) - \frac{n_i^2}{p_p(-W_{dp})}\exp\left(\frac{qV_A - \Delta_n}{k_BT}\right) + n_{p0}\left[1 - \exp\left(-\alpha_n W_{dp}\right)\right]}{\exp\left(-\alpha_n W_{dp}\right) - \exp\left(-\beta_n W_{dp}\right)}\exp\left(\beta_n W_{dp}\right). \tag{2.32}$$

Using Equations (2.30) and (2.31), we can determine the value of Δ_n self-consistently.

When Equations (2.27) and (2.30) are used for simplicity, the total junction current density (J) is given by

$$\begin{aligned} J &= J_{pd} + J_{nd} + J_p + J_n \\ &= J_{pd} + J_{nd} + J_{p0}\left\{\exp\left[\frac{qV_A - \Delta_p(V_A)}{k_BT}\right] - 1\right\} + J_{no}\left\{\exp\left[\frac{qV_A - \Delta_n(V_A)}{k_BT}\right] - 1\right\}, \end{aligned} \tag{2.33}$$

where

$$J_{p0} = \frac{qD_p p_{n0}}{L_p}, \tag{2.34a}$$

$$J_{n0} = \frac{qD_n n_{p0}}{L_n}, \tag{2.34b}$$

$$\Delta_p(V_A) = qF_{Dp}(W_{dp} + W_{dn}), \tag{2.35a}$$

$$\Delta_n(V_A) = qF_{Dn}(W_{dp} + W_{dn}). \tag{2.35b}$$

When Equations (2.28) and (2.31) are used, the total junction current density (J) is given by

$$\begin{aligned} J &= J_{pd} + J_{nd} + J_p + J_n \\ &= J_{pd} + J_{nd} + \frac{qD_p}{L_p} K_p(V_A, \Delta_p) + \frac{qD_n}{L_n} K_n(V_A, \Delta_n). \end{aligned} \tag{2.36}$$

2.2.2.2 Simulation Results – Model A

1. Use of Equation (2.33)
   J–V characteristics of a pn-junction device are calculated using Equation (2.33), where the following assumptions are made:

   a. $N_D = N_A = 1 \times 10^{15}\ \mathrm{cm}^{-3}$.
   b. $\Delta_n/q = \Delta_p/q = 0.1\ V_A$.
   c. Other physical parameters such as lifetime values of minority carriers are summarized in Table 2.1.

   Figure 2.2 shows calculated J–V curves for two different *imref* gradient conditions. For comparison, the J–V characteristic calculated assuming Equation (1.1) in Chapter 1 is also shown. It is worthwhile to note that the current level of the pn junction increases when the *imref* gradient is assumed in the depletion region. This simulation result clearly reveals that the drift and diffusion process of minority carriers in the depletion region greatly impacts the pn-junction current level. This also suggests that the *imref* gradient in the depletion region yields the drift of minority carriers to be injected into the counterpart region. It is revealed that a small gradient of *imref* ($\Delta_n/q = \Delta p/q = 0.1\ V_A$) apparently yields a *sub-one* ideality factor ($n < 1$). On the other hand, a large *imref* gradient ($\Delta_n/q = \Delta p/q = 0.5\ V_A$) results in a large ideal factor ($n > 1$). One of the important features of Equation (2.33) is the super-exponential behavior of the current density for $V_A > 0.55$ V. It is anticipated that this behavior stems from the fact that the depletion layer disappears for $V_A > V_{bi}$ (built-in voltage). Since the model loses the physical base for $V_A > V_{bi}$, it should be improved in the future so that it is applicable to a high-voltage condition.

Table 2.1 Physical parameters assumed in calculations for Model A (forward bias condition)

Parameters	Values [unit]	References
Lifetime of electrons (τ_n)	3.33×10^{-6} [s]	[5]
Lifetime of holes (τ_p)	1.00×10^{-6} [s]	[5]
Electron mobility (μ_n)	1.13×10^{3} [cm^2/V s]	[2]
Hole mobility (μ_p)	4.20×10^{2} [cm^2/V s]	[2]
Intrinsic carrier concentration (n_i)	1.09×10^{10} [cm^{-3}]	[2]
Temperature (T)	3.00×10^{2} [K]	

2. Use of Equation (2.36)
   J–V characteristics of a pn-junction device are also calculated using Equation (2.36) and the same assumptions as those shown above. Figure 2.3 shows calculated *J–V* curves for two different *imref* gradient conditions. For comparison, the *J–V* characteristic calculated assuming Equation (1.1) in the previous chapter is also shown. It should also be noted that both the primary behaviors and the current levels of the pn junction obtained by Equation (2.36) are almost identical to those by Equation (2.33), which suggests that the model used in Equation (2.36) is identical to that in Equation (2.33).

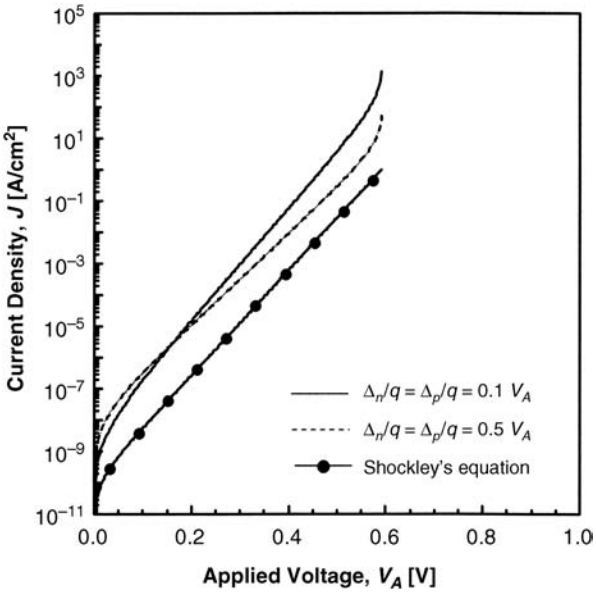

Figure 2.2 *J–V* characteristics for two different conditions of *imref* gradient with Equation (2.33) assumed.

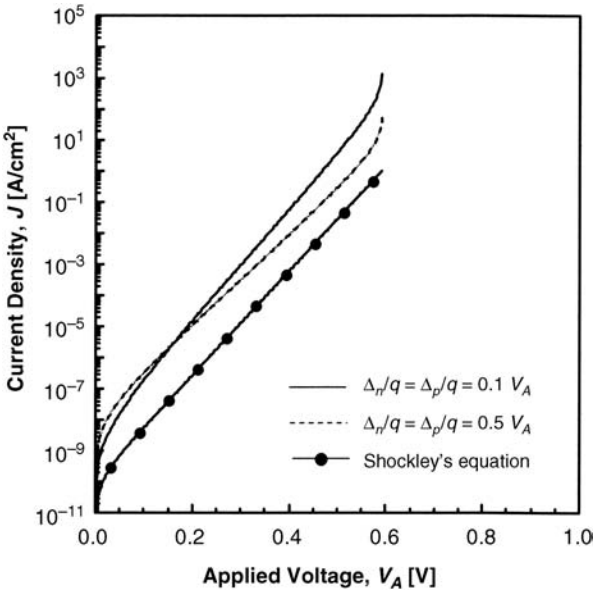

Figure 2.3 *J–V* characteristics for two different conditions of *imref* gradient with Equation (2.36) assumed.

In the case of Model A, a low doping pn junction is assumed; this suggests that we can in most cases neglect the gradient of the quasi-Fermi level (*imref*). Thus, assuming that $\Delta_n \ll qV_A$ and $\Delta_p \ll qV_A$, we can rewrite Equation (2.33) as follows:

$$\begin{aligned} J &= J_{p0}\left[\exp\left(\frac{qV_A - \Delta_P}{k_BT}\right) - 1\right] + J_{n0}\left[\exp\left(\frac{qV_A - \Delta_n}{k_BT}\right) - 1\right] \\ &= J_{p0}\left\{\exp\left[\frac{qV_A(1 - \Delta_P/qV_A)}{k_BT}\right] - 1\right\} + J_{n0}\left\{\exp\left[\frac{qV_A(1 - \Delta_n/qV_A)}{k_BT}\right] - 1\right\} \\ &\cong J_{p0}\left\{\exp\left[\frac{qV_A}{(1 + \Delta_P/qV_A)k_BT}\right] - 1\right\} + J_{n0}\left\{\exp\left[\frac{qV_A}{(1 + \Delta_n/qV_A)k_BT}\right] - 1\right\} \\ &= J_{p0}\left[\exp\left(\frac{qV_A}{n_{jp}k_BT}\right) - 1\right] + J_{n0}\left[\exp\left(\frac{qV_A}{n_{jn}k_BT}\right) - 1\right], \end{aligned} \tag{2.37}$$

where n_{jp} and n_{jn} are the ideality factor (larger than unity) for holes and electrons, respectively. This expression is almost identical to Equation (1.2) in the previous chapter. As a result, it can be concluded that the apparent value of the ideality factor does not always reflect the generation–recombination process of minority carriers in the quasi-neutral region.

2.2.3 Model B – High Doping Case

1. Depletion approximation
   Here we assume that the local electric field ($F(x)$) primarily stems from the ionized dopants because of the high doping condition. When a depletion approximation is taken in the depletion region, we have

$$F(x) = -\frac{qN_D}{\varepsilon_S}(W_{dn} - x) = F_{Dn}(x) \qquad (0 < x < W_{dn}), \tag{2.38a}$$

$$F(x) = -\frac{qN_A}{\varepsilon_S}(W_{dp} + x) = F_{Dp}(x) \qquad (-W_{dp} < x < 0), \tag{2.38b}$$

   where $F_{Dn}(x)$ (and $F_{Dp}(x)$) is the electric field due to the space charge (ionized imprity) in the case of Model B. Since this electric field hinders the injection of minority carriers, it must be taken into account when deriving the carrier distribution function from Equation (2.3).

2. The electric field ($F_{imref}(x)$) created by the *imref* gradient
   This yields the drift current in the depletion region [2,4]. Accordingly, the drift current component is calculated using this electric field component.

2.2.3.1 Solution with Model B

Assuming Equation (2.38a), Equation (2.5) is reduced to the following equation inside the depletion layer:

$$D_p\frac{d^2p_n}{dx^2} - \frac{qN_D\mu_p}{\varepsilon_S}(x - W_{dn})\frac{dp_n}{dx} - \frac{p_n - p_{n0}}{\tau_p} - \frac{qN_D\mu_p}{\varepsilon_S}p_n = 0. \tag{2.39}$$

Equation (2.39) is written as

$$\frac{d^2P_n}{dx^2} - A_{0p}(x - W_{dn})\frac{dP_n}{dx} - \frac{P_n}{L_p^2/(1 + L_p^2A_{0p})} = 0, \tag{2.40}$$

where we define the following:

$$P_n(x) = p_n(x) - p_{n0}/\left(1 + L_p^2A_{0p}\right), \tag{2.41}$$

$$L_p = \sqrt{D_p\tau_p}, \tag{2.42}$$

$$A_{0p} = \frac{qN_D\mu_p}{D_p\varepsilon_s}. \tag{2.43}$$

Applying the standard method of analysis [6], we can assume the following solution of Equation (2.40):

$$P_n(x) = R(x)I(x), \tag{2.44}$$

$$I(x) = \exp\left[\frac{A_{0p}}{2}\int_0^x (t - W_{dn})dt\right] \quad (0 < x < W_{dn}). \tag{2.45}$$

Substituting these equations into Equation (2.40) yields

$$\frac{d^2R(x)}{dx^2} - B(x)R(x) = 0, \tag{2.46}$$

$$B(x) = \frac{A_{0p}^2}{4}(x - W_{dn})^2 + \frac{A_{0p}}{2} + \frac{1}{L_p^2}. \tag{2.47}$$

Since

$$\frac{A_{0p}}{2} + \frac{1}{L_p^2} \le B(x) \le \frac{A_{0p}^2 W_{dn}^2}{4} + \frac{A_{0p}}{2} + \frac{1}{L_p^2},$$

we can, using the center value, approximate function $B(x)$ as

$$B(x) \cong \frac{A_{0p}^2 W_{dn}^2}{8} + \frac{A_{0p}}{2} + \frac{1}{L_p^2} = B_{0p}. \tag{2.48}$$

Applying this approximation to Equation (2.46), we have the following general solution of Equation (2.46):

$$R(x) = B_1 \exp[-\sqrt{B_{0p}}x] + B_2 \exp[\sqrt{B_{0p}}x], \tag{2.49}$$

where B_1 and B_2 are constants. Thus we have the following approximate solution of Equation (2.39) from Equation (2.44):

$$P_n(x) = p_n(x) - \frac{p_{n0}}{1 + L_p^2 A_{0p}} = \left[B_1 \exp(-\sqrt{B_{0p}}x) + B_2 \exp(\sqrt{B_{0p}}x)\right]\exp\left[\frac{A_{0p}}{2}\int_0^x (t - W_{dn})dt\right], \tag{2.50}$$

where B_1 and B_2 are determined by the boundary conditions at $x = 0$ and $x = W_{dn}$ as

$$B_1 = \frac{-P_n(W_{dn})\exp\left(\frac{A_{0p}W_{dn}^2}{4}\right) + P_n(0)\exp(\sqrt{B_{0p}}W_{dn})}{2\sinh(\sqrt{B_{0p}}W_{dn})}, \tag{2.51a}$$

$$B_2 = \frac{P_n(W_{dn})\exp\left(\frac{A_{0p}W_{dn}^2}{4}\right) - P_n(0)\exp(-\sqrt{B_{0p}}W_{dn})}{2\sinh\ (\sqrt{B_{0p}}W_{dn})}, \tag{2.51b}$$

$$P_n(W_{dn}) = p_n(W_{dn}) - \frac{p_{n0}}{1 + L_p^2 A_{0p}}, \tag{2.52}$$

$$P_n(0) = p_n(0) - \frac{p_{n0}}{1 + L_p^2 A_{0p}}. \tag{2.53}$$

In a similar manner, we have the following solution for the electron distribution function in the p-type region:

$$N_p(x) = n_p(x) - \frac{n_{p0}}{1 + L_n^2 A_{0n}} = \left[D_1\exp(-\sqrt{B_{0n}}x) + D_2\exp(\sqrt{B_{0n}}x)\right]\exp\left[\frac{A_{0n}}{2}\int_0^x (t + W_{dp})dt\right], \tag{2.54}$$

$$D_1 = \frac{N_p(-W_{dp})\exp\left(\frac{A_{0n}W_{dp}^2}{4}\right) - N_p(0)\exp(-\sqrt{B_{0n}}W_{dp})}{2\sinh(\sqrt{B_{0n}}W_{dp})}, \tag{2.55a}$$

$$D_2 = \frac{-N_p(-W_{dp})\exp\left(\frac{A_{0n}W_{dp}^2}{4}\right) + N_p(0)\exp(\sqrt{B_{0n}}W_{dp})}{2\sinh(\sqrt{B_{0n}}W_{dp})}, \tag{2.55b}$$

where

$$N_p\left(-W_{dp}\right) = n_p(-W_{dp}) - \frac{n_{p0}}{1 + L_n^2 A_{0n}}, \tag{2.56}$$

$$N_p(0) = n_p(0) - \frac{n_{p0}}{1 + L_n^2 A_{0n}}, \tag{2.57}$$

$$L_n = \sqrt{D_n \tau_n}, \tag{2.58}$$

$$A_{0n} = \frac{qN_A\mu_n}{D_n\varepsilon_S}, \tag{2.59}$$

and

$$B_{0n} = \frac{A_{0n}^2 W_{dp}^2}{8} + \frac{A_{0n}}{2} + \frac{1}{L_n^2}. \tag{2.60}$$

Thus the hole current density (J_{pd}) in the depletion region of the n-type region is derived from Equations (2.38a) and (2.50). Current continuity yields the following boundary condition:

$$J_{pd} = -qD_p \left.\frac{dp_n(x)}{dx}\right|_{x=0} + q\mu_p p_n(0) F_{imref,p}(0), \tag{2.61}$$

where

$$F_{imref,p}(0) = \frac{\Delta_p}{q(W_{dp} + W_{dn})}. \tag{2.62}$$

Here, $F_{imref,p}(0)$ is the electric field due to the gradient of the quasi-Fermi level $\phi_{Fp}(x)$, shown in Figure 2.1(b). Equation (2.61) is rewritten as

$$J_{pd} = qD_p \left[B_1 \sqrt{B_{0p}} - B_2 \sqrt{B_{0p}} + (B_1 + B_2) \frac{A_{0p} W_{dn}}{2} \right] + q\mu_p p_n(0) F_{imref,p}(0). \tag{2.63}$$

When the modified Shockley's model, shown in Figure 2.1(b), is applied to Equation (2.63), $p_n(0)$ and $p_n(W_{dn})$ are expressed as

$$p_n(0) = p_{n0} \exp\left(\frac{qV_A - \Delta_p/2}{k_B T}\right), \tag{2.64a}$$

$$p_n(W_{dn}) = p_{n0} \exp\left(\frac{qV_A - \Delta_p}{k_B T}\right). \tag{2.64b}$$

Similarly, the electron current density (J_{nd}) is given by

$$J_{nd} = qD_n \left.\frac{dn_p(x)}{dx}\right|_{x=0} + q\mu_n n_p(0) F_{imref,n}(0), \tag{2.65}$$

where

$$F_{imref,n}(0) = \frac{\Delta_n}{q(W_{dp} + W_{dn})}. \tag{2.66}$$

Here, $F_{imref,n}(0)$ is the electric field due to the gradient of the quasi-Fermi level $\phi_{Fn}(x)$, shown in Figure 2.1(b). Equation 2.65 is rewritten as

$$J_{nd} = qD_n \left[-D_1 \sqrt{B_{0n}} + D_2 \sqrt{B_{0n}} + (D_1 + D_2) \frac{A_{0n} W_{dp}}{2} \right] + q\mu_n n_p(0) F_{imref,n}(0). \tag{2.67}$$

When the modified Shockley's model is applied to Equation (2.67), $n_p(0)$ and $n_p(-W_{dp})$ are expressed as

$$n_p(0) = n_{p0} \exp\left(\frac{qV_A - \Delta_n/2}{k_B T}\right), \tag{2.68a}$$

$$n_p(-W_{dp}) = n_{p0} \exp\left(\frac{qV_A - \Delta_n}{k_B T}\right). \tag{2.68b}$$

In the quasi-neutral region, we can make the rough assumption of no electric field; this yields Shockley's type of solution based on the differential Equation (2.39). In that case, we have the following expression from Equation (2.50):

$$\begin{aligned} J_p &= -qD_p \left.\frac{dp_n(x)}{dx}\right|_{x=W_{dn}} \\ &= qD_p \left[B_1 \sqrt{B_{0p}} \exp(-\sqrt{B_{0p}} W_{dn}) - B_2 \sqrt{B_{0p}} \exp(\sqrt{B_{0p}} W_{dn})\right] \exp\left(-\frac{A_{0p}}{4} W_{dn}^2\right). \end{aligned} \tag{2.69}$$

On the other hand, in the quasi-neutral region of the p-type region, we have the following expression from Equation (2.54):

$$\begin{aligned} J_n &= qD_n \left.\frac{dn_p(x)}{dx}\right|_{x=-Wdp} \\ &= qD_n \left[-D_1 \sqrt{B_{0n}} \exp(\sqrt{B_{0n}} W_{dp}) + D_2 \sqrt{B_{0n}} \exp(-\sqrt{B_{0n}} W_{dp})\right] \exp\left(-\frac{A_{0n}}{4} W_{dp}^2\right). \end{aligned} \tag{2.70}$$

Total current density (J) is expressed by the full set of the above equations as follows:

$$\begin{aligned} J &= J_{pd} + J_{nd} + J_p + J_n \\ &= qD_p \left[B_1 \sqrt{B_{0p}} - B_2 \sqrt{B_{0p}} + (B_1 + B_2) \frac{A_{0p} W_{dn}}{2}\right] + \frac{\mu_p p_n(0) \Delta_p}{W_{dp} + W_{dn}} \\ &\quad + qD_n \left[-D_1 \sqrt{B_{0n}} + D_2 \sqrt{B_{0n}} + (D_1 + D_2) \frac{A_{0n} W_{dp}}{2}\right] + \frac{\mu_n n_p(0) \Delta_n}{W_{dp} + W_{dn}} \\ &\quad + qD_p \left[B_1 \sqrt{B_{0p}} \exp(-\sqrt{B_{0p}} W_{dn}) - B_2 \sqrt{B_{0p}} \exp(\sqrt{B_{0p}} W_{dn})\right] \exp\left(-\frac{A_{0p}}{4} W_{dn}^2\right) \\ &\quad + qD_n \left[-D_1 \sqrt{B_{0n}} \exp(\sqrt{B_{0n}} W_{dp}) + D_2 \sqrt{B_{0n}} \exp(-\sqrt{B_{0n}} W_{dp})\right] \exp\left(-\frac{A_{0n}}{4} W_{dp}^2\right), \end{aligned} \tag{2.71}$$

where $p_n(0)$ and $n_p(0)$ are given by Equations (2.64a) and (2.68a), respectively.

Table 2.2 Physical parameters assumed in calculations for Model B (forward bias condition)

Parameters	Values [unit]	References
Lifetime of electrons (τ_n)	4.98×10^{-8} [s]	[5]
Lifetime of holes (τ_p)	1.49×10^{-8} [s]	[5]
Electron mobility (μ_n)	1.18×10^{2} [cm^2/V s]	[2]
Hole mobility (μ_p)	1.08×10^{2} [cm^2/V s]	[2]
Intrinsic carrier concentration (n_i)	1.09×10^{10} [cm^{-3}]	[2]
Temperature (T)	3.00×10^{2} [K]	

2.2.3.2 Simulation Results – Model B

J–V characteristics of a pn-junction device are calculated using Equation (2.71), where the following assumptions are made:

a. $N_D = N_A = 1 \times 10^{18}\,\mathrm{cm}^{-3}, 1 \times 10^{19}\,\mathrm{cm}^{-3}$.
b. $\Delta_n/q = \Delta_p/q = 0.1\,V_A$.
c. Other physical parameters such as lifetime values of minority carriers are summarized in Table 2.2.

Figure 2.4 shows calculated curves, where the curve calculated using Shockley's equation is also shown for comparison. It is clearly seen that Equation (2.71) ascribes an exponential behavior to the current density. However, the ideality factor (n) of Equation (2.71) is larger than unity and its value is larger than that of Equation (2.33) for the *imref* gradient of $0.5V_A$.

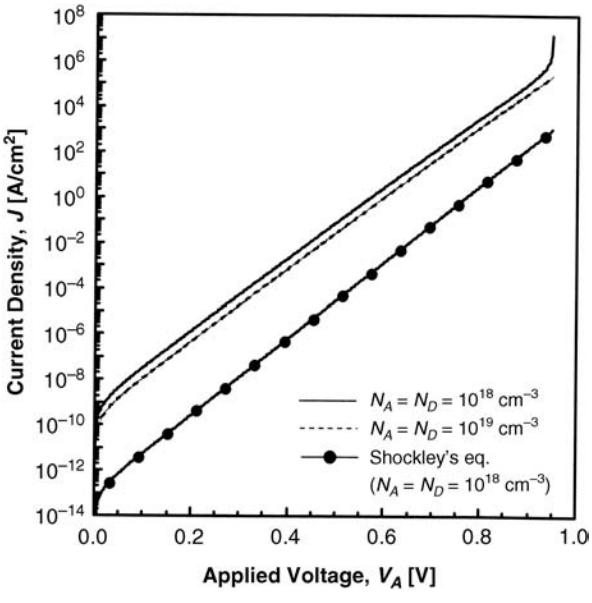

Figure 2.4 *J–V* characteristics calculated with Equation (2.71).

It is strongly suggested that the *imref* gradient enhances the recombination of the minority carriers in the depletion region; ideality factor (n) becomes larger than unity, even when the conventional recombination process is not assumed. The super-exponential behavior of the current density is also seen. This behavior is based on the same mechanism as that mentioned before.

2.3 Bulk pn-Junction Diode – Reverse Bias

2.3.1 Model A – Low Doping Case

First, the schematic band diagram for the reverse-biased pn-junction diode is illustrated in Figure 2.5. Notations are the same as those in Figure 2.1. For the reverse-biased condition, the drift current component is not theoretically needed in calculations of the junction current because the recombination process is not dominant. Therefore, the physical model that should be assumed is almost the same as Shockley's model. The total junction current density (J) under the reverse-biased condition is rewritten from Equation (2.33) as

$$J = J_{ge}(V_A) + (J_{p0} + J_{n0})\left[\exp\left(\frac{qV_A}{k_BT}\right) - 1\right], \tag{2.72}$$

where J_{ge} is the generation current density due to electrons and holes in the depletion region; for example, J_{ge} is expressed as [7]

$$J_{ge}(V_A) = -\frac{qn_i(W_{dp} + W_{dn})}{\tau_g} + J_{ge}(V_A = 0), \tag{2.73}$$

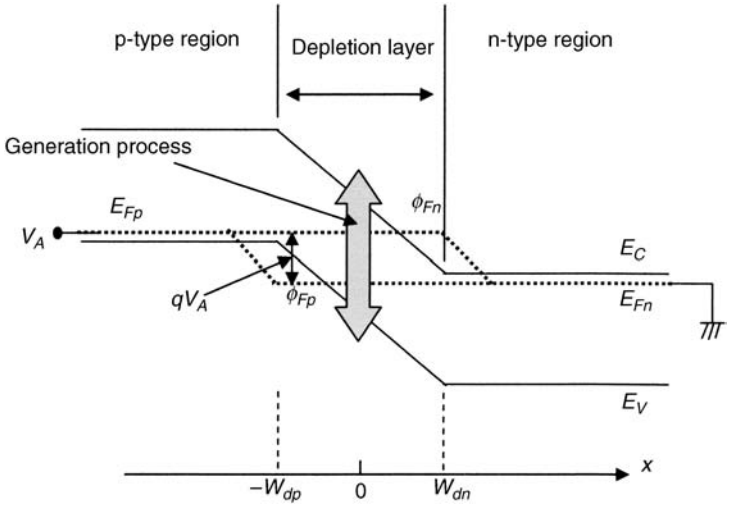

Figure 2.5 Schematic band models of the pn junction under the reverse-biased condition for the low doping case ($V_A < 0$).

where $J_{ge}(V_A = 0)$ is inserted in order to cancel out the generation current in the depletion region at $V_A = 0$ V. Parameter τ_g denotes the generation lifetime defined by

$$\tau_g = \frac{\sigma_n \exp[(E_t - E_i)/k_B T] + \sigma_p \exp[(E_i - E_t)/k_B T]}{\sigma_n \sigma_p v_{th} N_t}, \tag{2.74}$$

where σ_n, σ_p, v_{th}, N_t, E_t, and E_i are the electron capture cross-section, the hole capture cross-section, the thermal velocity of carriers, the trap density, the energy level of traps, and the intrinsic Fermi level, respectively.

As a result, it is not necessary for us to consider new non-ideal behaviors of the pn-junction diode except for the conventional generation process in the depletion region. In the low doping case, the avalanche phenomenon will not be needed when modeling the current characteristics provided $|V_A|$ is not too large.

2.3.2 Model B – High Doping Case

For the high doping case, we have to reconsider the junction current characteristics, unlike the low doping case, because we cannot neglect the space-charge effect in the depletion region; we must assume Equations (2.38a) and (2.38b). It is anticipated that the schematic band diagram is not identical to Figure 2.5. Of course, the depletion layer width will be reduced compared to the low doping case at the same reverse bias. Here we assume a non-conventional band diagram (see Figure 2.6), where the *imref* of electrons is explicitly inclined in the depletion layer of the n-type region and that of holes is also explicitly inclined in the depletion layer of the p-type region. It is assumed that the *imref*s disappear at the edge of the depletion layer; that is, the drift and diffusion process is limited to the depletion layer. This is based on the physics-based idea in which electrons (holes) are generated in the p-side (n-side) depletion

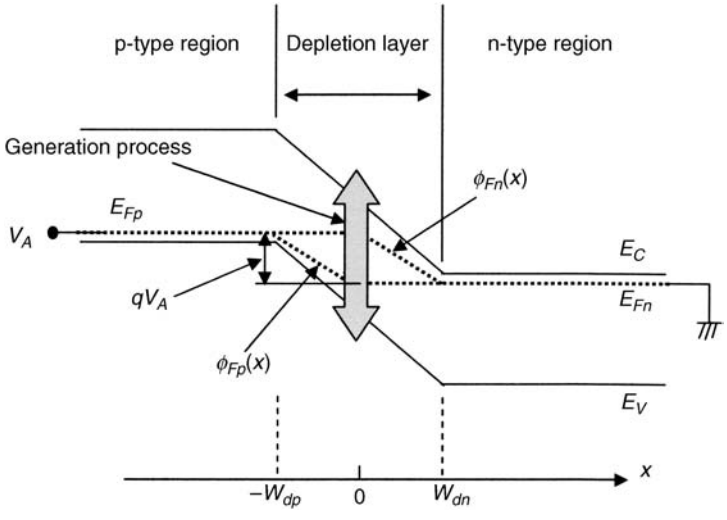

Figure 2.6 Schematic band model of the pn junction under the reverse-biased condition for the high doping case ($V_A < 0$).

region and are accelerated by the space-charge-induced field in the n-side (p-side) depletion region. Since the majority carrier density is very high in the quasi-neutral region, the carrier injection effect is neglible; this suggests that we can assume no diffusion effect and no field in the quasi-neutral region.

We start our consideration from the following current continuity equation for holes in the n-type region in the steady state:

$$D_p \frac{d^2 p_n}{dx^2} - \frac{qN_D\mu_p}{\varepsilon_S}(x - W_{dn})\frac{dp_n}{dx} + G - \frac{qN_D\mu_p}{\varepsilon_S}p_n = 0, \tag{2.75}$$

where G denotes the generation rate per unit volume. This equation will give the hole density generated inside the n-type region. Since the generation process simultaneously yields the density of electrons (equal to that of holes given by the above equation), we will utilize this relation in calculating the total current density.

Equation (2.75) is written as

$$\frac{d^2 P_n}{dx^2} - A_{0p}(x - W_{dn})\frac{dP_n}{dx} - A_{0p}P_n = 0, \tag{2.76}$$

where we define the following:

$$P_n(x) = p_n(x) - G/A_{0p}D_p. \tag{2.77}$$

A_{0p} is given by Equation (2.43). Applying the standard method of analysis [6], we can assume the following solution of Equation (2.76):

$$P_n(x) = R_r(x)I(x), \tag{2.78}$$

$$I(x) = \exp\left[\frac{A_{0p}}{2}\int_0^x (t - W_{dn})dt\right] \quad (0 < x < W_{dn}). \tag{2.79}$$

Substituting these equations into Equation (2.76) yields

$$\frac{d^2 R_r(x)}{dx^2} - B_r(x)R_r(x) = 0, \tag{2.80}$$

$$B_r(x) = \frac{A_{0p}^2}{4}(x - W_{dn})^2 + \frac{A_{0p}}{2}. \tag{2.81}$$

Since

$$\frac{A_{0p}}{2} \le B_r(x) \le \frac{A_{0p}^2 W_{dn}^2}{4} + \frac{A_{0p}}{2},$$

we can approximate the function $B_r(x)$ using the center value as

$$B_r(x) \cong \frac{A_{0p}^2 W_{dn}^2}{8} + \frac{A_{0p}}{2} = B_{r0p}. \tag{2.82}$$

Applying this approximation to Equation (2.80), we have the following general solution of Equation (2.80):

$$R_r(x) = B_{r1} \exp(-\sqrt{B_{r0p}}x) + B_{r2} \exp(\sqrt{B_{r0p}}x), \tag{2.83}$$

where B_{r1} and B_{r2} are constants. Thus we have the following approximate solution of Equation (2.75) from Equation (2.78):

$$P_n(x) = p_n(x) - \frac{G}{A_{0p}D_p} = \left[B_{r1} \exp(-\sqrt{B_{r0p}}x) + B_{r2} \exp(\sqrt{B_{r0p}}x)\right] \exp\left[\frac{A_{0p}}{2}\int_0^x (t - W_{dn})dt\right], \tag{2.84}$$

where B_{r1} and B_{r2} are determined by the boundary conditions at $x = 0$ and $x = W_{dn}$:

$$B_{r1} = \frac{-P_n(W_{dn}) \exp\left(\frac{A_{0p}W_{dn}^2}{4}\right) + P_n(0) \exp(\sqrt{B_{r0p}}W_{dn})}{2 \sinh(\sqrt{B_{r0p}}W_{dn})}, \tag{2.85a}$$

$$B_{r2} = \frac{P_n(W_{dn}) \exp\left(\frac{A_{0p}W_{dn}^2}{4}\right) - P_n(0) \exp(-\sqrt{B_{r0p}}W_{dn})}{2 \sinh(\sqrt{B_{r0p}}W_{dn})}, \tag{2.85b}$$

$$P_n(W_{dn}) = p_n(W_{dn}) - \frac{G}{A_{0p}D_p}, \tag{2.86}$$

$$P_n(0) = p_n(0) - \frac{G}{A_{0p}D_p}. \tag{2.87}$$

Since $p_n(0)$ must be larger than $p_n(W_{dn})$ due to the generation process of holes in the depletion region, we assume for simplicity that $p_n(0)$ and $p_n(W_{dn})$ are expressed as

$$p_n(0) = \frac{G}{A_{0p}D_p} + p_{no}, \tag{2.88a}$$

$$p_n(W_{dn}) = p_{n0}. \tag{2.88b}$$

The first term of Equation (2.88a) is the contribution of hole generation in the depletion region.

In a similar manner, we have the following solution for the electron distribution function in the p-type region:

$$N_p(x) = n_p(x) - \frac{G}{A_{0n}D_n} = \left[D_{r1}\exp(-\sqrt{B_{r0n}}x) + D_{r2}\exp(\sqrt{B_{r0n}}x)\right]\exp\left[\frac{A_{0n}}{2}\int_0^x (t + W_{dp})dt\right], \tag{2.89}$$

$$D_{r1} = \frac{N_p(-W_{dp})\exp\left(\dfrac{A_{0n}W_{dp}^2}{4}\right) - N_p(0)\exp(-\sqrt{B_{r0n}}W_{dp})}{2\sinh(\sqrt{B_{r0n}}W_{dp})}, \tag{2.90a}$$

$$D_{r2} = \frac{-N_p(-W_{dp})\exp\left(\dfrac{A_{0n}W_{dp}^2}{4}\right) + N_p(0)\exp(\sqrt{B_{r0n}}W_{dp})}{2\sinh(\sqrt{B_{r0n}}W_{dp})}, \tag{2.90b}$$

where

$$N_p(-W_{dp}) = n_p(-W_{dp}) - \frac{G}{A_{0n}D_n}, \tag{2.91}$$

$$N_p(0) = n_p(0) - \frac{G}{A_{0n}D_n}. \tag{2.92}$$

Since $n_p(0)$ must be larger than $n_p(-W_{dp})$ due to the generation process of electrons in the depletion region, we assume for simplicity that $n_p(0)$ and $n_p(-W_{dp})$ are expressed as

$$n_p(0) = \frac{G}{A_{0n}D_n} + n_{p0}, \tag{2.93a}$$

$$n_p(-W_{dp}) = n_{p0}. \tag{2.93b}$$

The first term of Equation (2.93a) is the contribution of electron generation in the depletion region. In addition, we have

$$B_{r0n} = \frac{A_{0n}^2W_{dp}^2}{8} + \frac{A_{0n}}{2}. \tag{2.94}$$

The hole current density (J_{pd}) in the depletion region of the n-type region can be derived from Equations (2.38a) and (2.84). The boundary condition for the diffusion current

component differs from that for the drift current component. Since the diffusion of holes starts at the depletion layer edge of the n-type region, we must take it at $x = W_{dn}$. Thus we have

$$J_{pd} = -qD_p \left.\frac{dp_n(x)}{dx}\right|_{x=W_{dn}} + q\mu_p p_n(0) F_{imref,p}(0), \tag{2.95}$$

where

$$F_{imref,p}(0) = \frac{V_A}{W_{dn}}. \tag{2.96}$$

It should be noted that $F_{imref,p}(0)$ has negative polarity, so Equation (2.95) is rewritten as

$$J_{pd} = qD_p\left[B_{r1}\sqrt{B_{r0p}}\exp(-\sqrt{B_{r0p}}W_{dn}) - B_{r2}\sqrt{B_{r0p}}\exp(\sqrt{B_{r0p}}W_{dn})\right]\exp\left(-\frac{A_{0p}W_{dn}^2}{4}\right) + \left(\frac{G}{A_{0p}D_p} + B_{r1} + B_{r2}\right)\frac{q\mu_p V_A}{W_{dn}} - J_{pd}(V_A = 0), \tag{2.97}$$

where J_{pd} $(V_A = 0)$ is inserted in order to cancel out the diffusion current in the depletion region at $V_A = 0$ V.

Similarly, the electron current density (J_{nd}) is given by

$$J_{nd} = qD_n \left.\frac{dn_p(x)}{dx}\right|_{x=-W_{dp}} + q\mu_n n_p(0) F_{imref,n}(0), \tag{2.98}$$

where

$$F_{imref,n}(0) = \frac{V_A}{W_{dp}}. \tag{2.99}$$

Similarly, Equation (2.98) is rewritten as

$$J_{nd} = qD_n\left[-D_{r1}\sqrt{B_{r0n}}\exp(\sqrt{B_{r0n}}W_{dp}) + D_{r2}\sqrt{B_{r0n}}\exp(-\sqrt{B_{r0n}}W_{dp})\right]\exp\left(-\frac{A_{0n}W_{dp}^2}{4}\right) + \left(\frac{G}{A_{0n}D_n} + D_{r1} + D_{r2}\right)\frac{q\mu_n V_A}{W_{dp}} - J_{nd}(V_A = 0). \tag{2.100}$$

The total current density (J) is expressed by the full set of above equations as per the following:

$$\begin{aligned} J &= J_{pd} + J_{nd} \\ &= qD_p\left[B_{r1}\sqrt{B_{r0p}}\exp(-\sqrt{B_{r0p}}W_{dn}) - B_{r2}\sqrt{B_{r0p}}\exp(\sqrt{B_{r0p}}W_{dn})\right]\exp\left(-\frac{A_{0p}W_{dn}^2}{4}\right) \\ &\quad + qD_n\left[-D_{r1}\sqrt{B_{r0n}}\exp(\sqrt{B_{r0n}}W_{dp}) + D_{r2}\sqrt{B_{r0n}}\exp(-\sqrt{B_{r0n}}W_{dp})\right]\exp\left(-\frac{A_{0n}W_{dp}^2}{4}\right) \\ &\quad + \left(\frac{G}{A_{0p}D_p} + B_{r1} + B_{r2}\right)\frac{q\mu_p V_A}{W_{dn}} + \left(\frac{G}{A_{0n}D_n} + D_{r1} + D_{r2}\right)\frac{q\mu_n V_A}{W_{dp}} - J_{pd}(V_A = 0) - J_{nd}(V_A = 0). \end{aligned} \tag{2.101}$$

2.3.2.1 Simulation Results – Model B

The *J–V* characteristics of a pn-junction device are calculated using Equation (2.101), where the following assumptions are made:

a. $N_D = N_A = 1 \times 10^{18}\,\mathrm{cm}^{-3}$, $1 \times 10^{19}\,\mathrm{cm}^{-3}$.
b. $G = 0$, $G = n_i/\tau_g$. Parameter τ_g is given by Equation (2.74).
c. Other physical parameters such as lifetime values of minority carriers are summarized in Table 2.3.

Figures 2.7 and 2.8 show calculated curves; Figure 2.7 is for $N_D = N_A = 1 \times 10^{18}\,\mathrm{cm}^{-3}$ and Figure 2.8 is for $N_D = N_A = 1 \times 10^{19}\,\mathrm{cm}^{-3}$; the influence of carrier generation conditions ($G = 0$ and $G = n_i/\tau_g$) on current density behavior is compared.

Figure 2.7 reveals that the reverse-biased current given by Equation (2.101) increases with applied voltage, even for $G = 0$, which is quite different from Shockley's ideal curve. The present model assumes that the *imref* gradient in the depletion region yields the drift and diffusion current of carriers. The model suggests that the averaged velocity of holes served by the n-type region and that of electrons served by the p-type region are accelerated with the *imref*-gradient-induced field and the rising applied voltage increases the reversed-biased current. Therefore, we must analyze carefully the measured results when it is not clear whether many defects exist in the material. On the other hand, in Figure 2.7, it is also found that the reverse-biased current level is about 10 times higher than that without the generation when account is taken of the finite G value. Therefore, the conventional extraction of lifetime and other physical parameters is technically validated when observation by another technique indicates that many defects exist in the material. It is anticipated that the conventional generation model overestimates the generation current. The reverse-biased current is roughly proportional to the applied voltage, which means that the drift current component in Equation (2.101) is a dominant factor.

Table 2.3 Physical parameters assumed in calculations for Model B (reverse bias condition)

Parameters	Values [unit]	References
Lifetime of electrons (τ_n)	4.98×10^{-8} [s] ($N_A = 10^{18}$ [cm^{-3}])	[5]
	5.00×10^{-9} [s] ($N_A = 10^{19}$ [cm^{-3}])	[5]
Lifetime of holes (τ_p)	1.49×10^{-8} [s] ($N_D = 10^{18}$ [cm^{-3}])	[5]
	1.50×10^{-9} [s] ($N_D = 10^{19}$ [cm^{-3}])	[5]
Electron mobility (μ_n)	188 [cm^2/V s] ($N_D = 10^{18}$ [cm^{-3}])	[5]
	102 [cm^2/V s] ($N_D = 10^{19}$ [cm^{-3}])	[5]
Hole mobility (μ_p)	108 [cm^2/V s] ($N_A = 10^{18}$ [cm^{-3}])	[5]
	62.3 [cm^2/V s] ($N_A = 10^{19}$ [cm^{-3}])	[5]
$\lvert E_i - E_t \rvert$	0.0 [eV]	
Trap density (N_t)	10^{16} [cm^{-3}]	
Capture cross-section of electrons (σ_n)	5.00×10^{-16} [s]	[3]
Capture cross-section of holes (σ_p)	5.00×10^{-16} [s]	[3]
Intrinsic carrier concentration (n_i)	1.09×10^{10} [cm^{-3}]	[3]
Temperature (T)	3.00×10^{2} [K]	

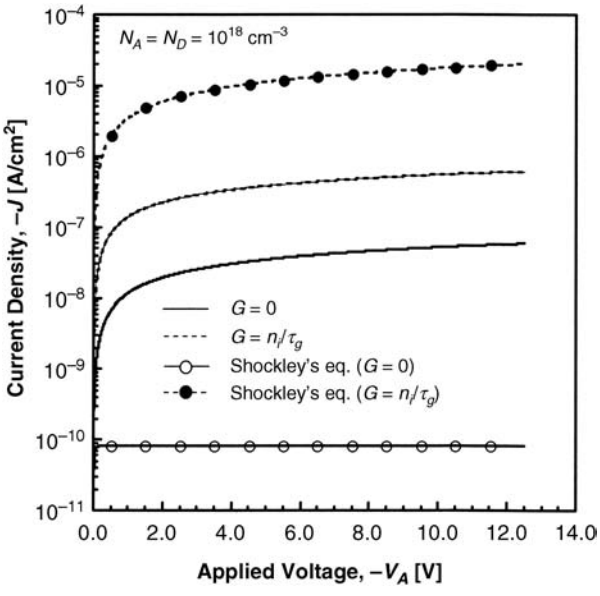

Figure 2.7 *J–V* characteristics calculated with Equation (2.101) for $N_A = N_D = 10^{18}\,\mathrm{cm}^{-3}$.

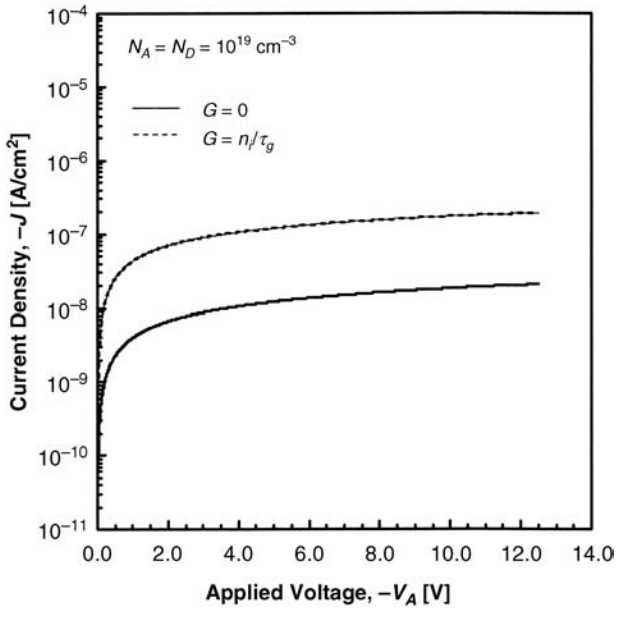

Figure 2.8 *J–V* characteristics calculated with Equation (2.101) for $N_A = N_D = 10^{19}\,\mathrm{cm}^{-3}$.

Figure 2.8 also reveals that the reverse-biased current given by Equation (2.101) increases with applied voltage, even for $G = 0$. A comparison with the curves in Figure 2.7 shows that higher doping levels reduce the reverse-biased current because the depletion region is narrowed compared to that in Figure 2.7.

2.4 The Insulated-Gate pn Junction of the SOI Lubistor – Forward Bias

The physical impacts of the insulated gate on pn-junction operation are described in Parts Two and Three. A brief consideration is given here in order to assist the reader's understanding of the physics of the Lubistor. Figure 2.9 shows the schematic structure and the bias configuration of the insulated-gate pn-junction device on the silicon-on-insulator (SOI) substrate; the coordinate system is also designated. Parameter t_S denotes the SOI layer thickness.

2.4.1 The Positive Gate Voltage Condition

When the gate voltage is positive, the surface of the p-type region is depleted or inverted. Consider the case in which the p-type region beneath the gate electrode is fully depleted and the top surface of the p-type region is inverted, as shown in Figures 2.10(a) and 2.11(a) . The original metallurgical junction is not meaningful with regard to operation characteristics, and the virtual junction created around the gate electrode edge adjusted to the p-type region works as the actual junction, as shown in Figure 2.10(a). Electrons of the inversion layer diffuse from the gate-controlled inversion layer edge into the quasi-neutral p-type region, where they

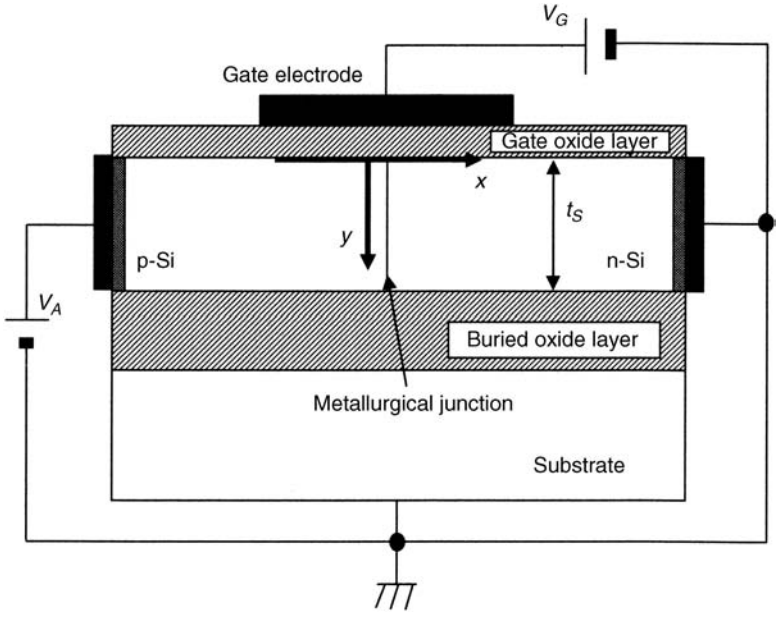

Figure 2.9 Schematic structure of the insulated-gate pn-junction device on the SOI substrate.

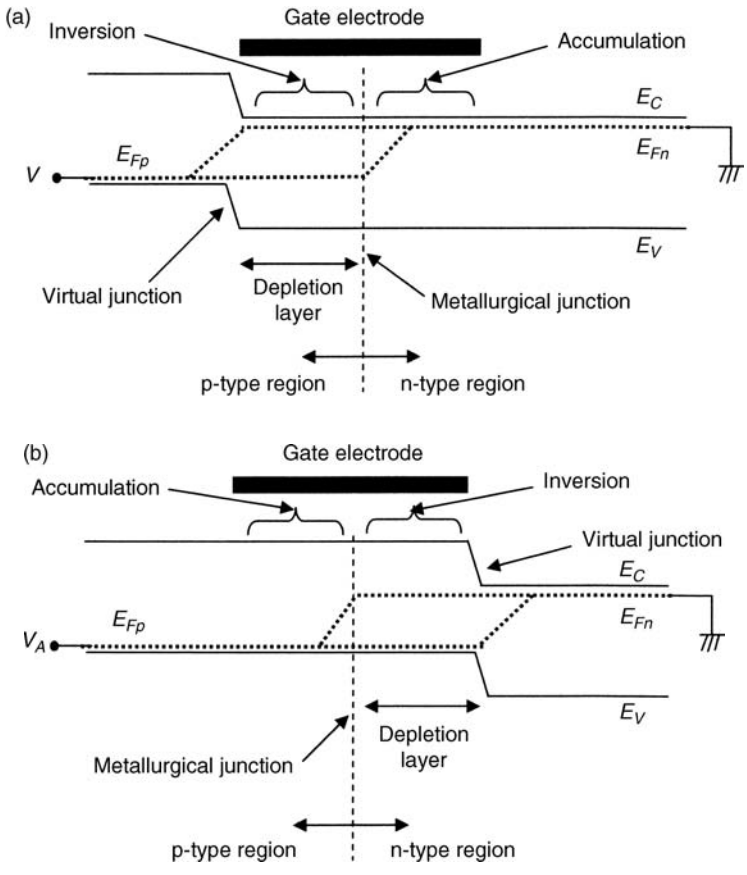

Figure 2.10 Schematic band model of the SOI Lubistor. It is assumed that the pn junction is under the forward-biased condition. (a) Positive gate voltage ($V_G > 0$). (b) Negative gate voltage ($V_G < 0$).

recombine with the holes present. On the other hand, holes of the quasi-neutral region are injected into the region depleted by the gate-induced field, but it is anticipated that they recombine with electrons in the quasi-neutral region. It should be pointed out that most of the holes injected into the depletion region do not recombine with electrons inside the depletion layer of the p-type region because they are basically isolated around the bottom surface. When the bottom surface of the SOI layer has ideal properties, they reach the metallurgical junction and recombine with electrons in the n-type region; the behavior of electrons and holes is illustrated in Figure 2.11(a). This behavior of holes is quite different from that in the bulk pn-junction diode shown in Figure 2.1(a). In addition, it should be noted in Figures 2.10(a) and 2.11(a) that *imref*s of electrons and holes beneath the gate electrode are roughly flat due to the gate-induced field as long as the current level is not very high. This feature of *imref*s is also different from that in the bulk pn-junction diode shown in Figure 2.1(a) and (b).

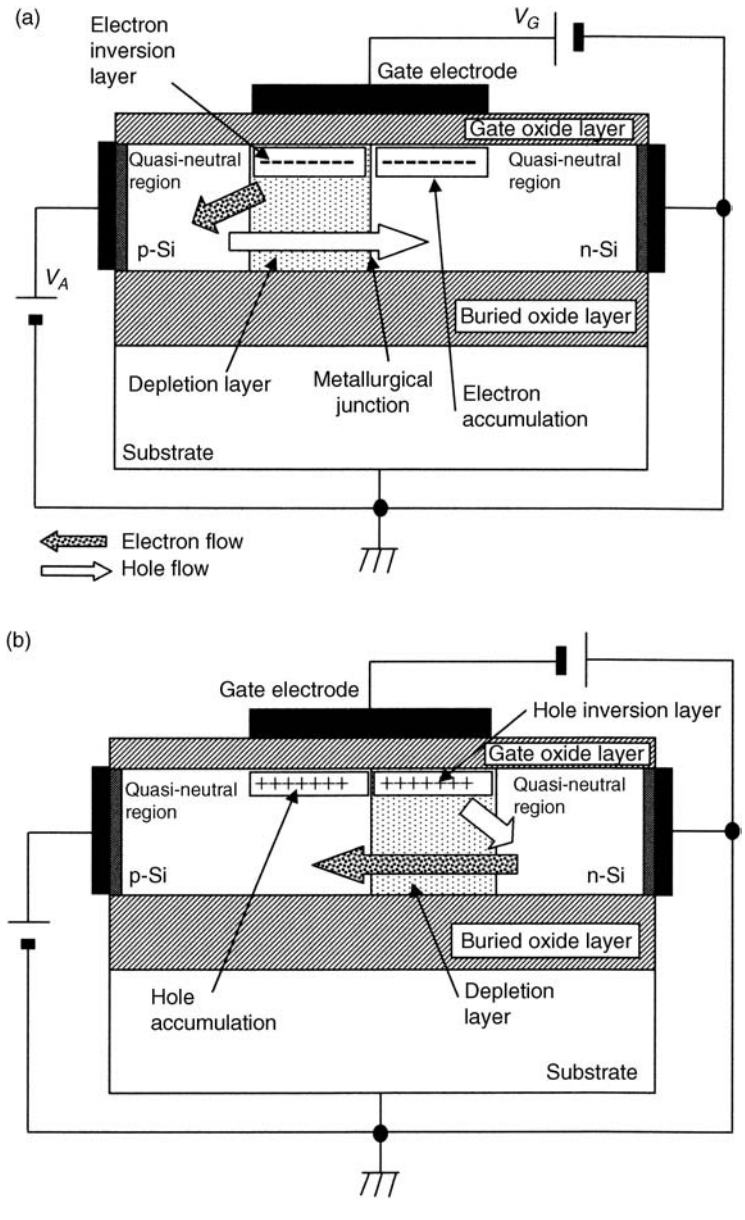

Figure 2.11 Schematic view of the forward-biased SOI Lubistor. It is assumed that the SOI layer is thinner than the expected depletion layer width. (a) Positive gate voltage ($V_G > 0$). (b) Negative gate voltage ($V_G < 0$).

When we follow Shockley's simplified model, the forward-biased junction current (J) can be expressed approximately as

$$J = J_p + J_n = J_{p0}(V_G)\left[\exp\left(\frac{qV_A}{k_BT}\right) - 1\right] + J_{n0}(V_G)\left[\exp\left(\frac{qV_A}{k_BT}\right) - 1\right], \qquad (2.102)$$

where we assume

$$J_{p0}(V_G) = \frac{\int_0^{t_S} qD_p p_n(V_G, y)}{t_S L_p(V_G, y)} dy, \tag{2.103a}$$

$$J_{n0}(V_G) = \frac{\int_0^{t_S} qD_n n_p(V_G, y)}{t_S L_n(V_G, y)} dy. \tag{2.103b}$$

$L_p(V_G,y)$ and $L_n(V_G,y)$ are the in-depth profiles of the gate-controlled diffusion length of holes and electrons, respectively, and $p_n(V_G,y)$ and $n_p(V_G,y)$ are the in-depth profiles of the gate-controlled carrier density of holes and electrons, respectively. In the case of a positive gate voltage, $L_n(V_G,y)$ is basically insensitive to the gate voltage, but $L_p(V_G,y)$ is very sensitive to the gate voltage if the thickness of the n-type region beneath the gate electrode is thinner than the Debye length of the n-type region. The electron accumulation layer created by the very high positive gate voltage fully covers the SOI layer, and $p_n(V_G,y)$ is drastically reduced because of the relation

$$\int_0^{t_S} p_n(V_G, y)dy \int_0^{t_S} n_n(V_G, y)dy \approx t_S^2 n_i^2 \exp\left(\frac{qV_A}{k_B T}\right), \tag{2.104}$$

where the semi-classical condition is assumed for simplicity. As we must assume

$$\int_0^{t_S} p_n(V_G, y)dy \ll \int_0^{t_S} n_n(V_G, y)dy, \tag{2.105}$$

$L_p(V_G,y)$ must be greatly reduced.

When the electric field shielding (EFS) layer exists near the bottom of the SOI layer [8–10], the value of the hole density around the bottom surface of the p-type SOI layer is greatly lowered. This basically suppresses the hole current near the bottom of the p-type region depleted by the gate electrode. The value of the electron density around the bottom surface of the n-type SOI layer is also greatly lowered. This phenomenon yields the Lubistor's peculiar behaviour, as noted in the 1980s [11,12]. Details of the physics of the EFS layer are described in Chapter 5.

2.4.2 The Negative Gate Voltage Condition

The physical picture for this condition is shown in Figures 2.10(b) and 2.11(b). The expected phenomena are almost identical to the above description, with the roles of electrons and holes reversed. In fabricated devices, some deviation may be observed because the impact of the interface property of the gate oxide layer/SOI layer interface and the SOI layer/buried oxide layer interface on the transport characteristics depends on the polarity of the semiconductor.

2.5 The Insulated-Gate pn Junction of the SOI Lubistor – Reverse Bias

The previous section briefly characterized the forward-biased operation of the SOI Lubistor to allow readers to catch the important features of the device. Important physics in reverse-biased operation of the thin-film SOI Lubistor as discerned in experiments are discussed in

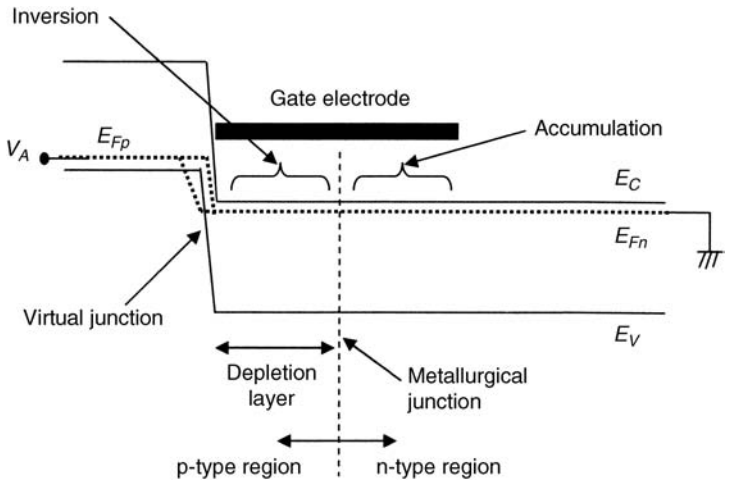

Figure 2.12 Schematic band model of the SOI Lubistor. It is assumed that the pn junction is under the reverse-biased condition ($V_A < 0$). The band diagram illustrated assumes $V_G > 0$.

Part Three. Here I briefly address some of the points that differ from the forward-bias condition. When forward bias is applied to the SOI Lubistor, the insulated-gate creates a virtual junction at the gate electrode edge, as illustrated in Figures 2.10(a) and 2.11(a). When the reverse bias is applied to the SOI Lubistor, the virtual junction is also created at the gate electrode edge, as shown in Figures 2.12 and 2.13. However, the aspect of *imref*s is quite

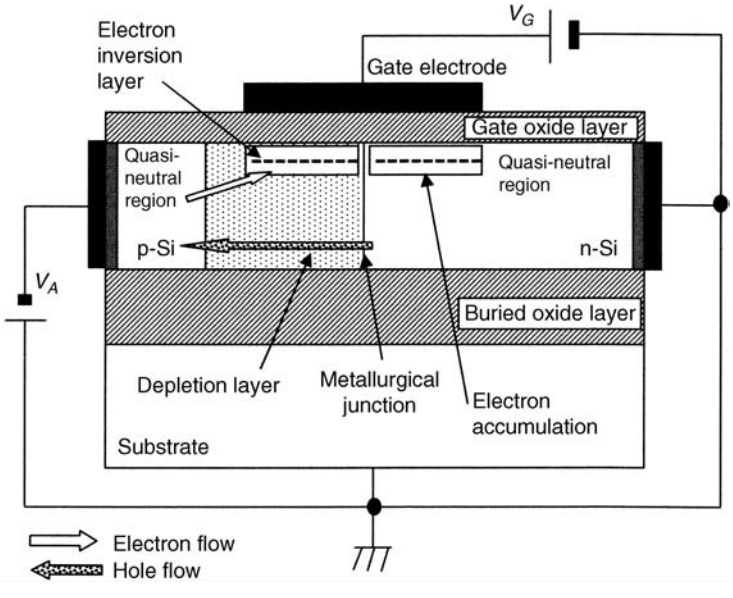

Figure 2.13 Schematic view of the reverse-biased SOI Lubistor. It is assumed that the SOI layer is thinner than the expected depletion layer width ($V_A < 0$). The illustration assumes $V_G > 0$.

different from that for the forward bias condition because no minority carrier injection exists; that is, no notable split of *imref*s. Figure 2.12 suggests that we can predict interband electron tunneling from the valence band of the p-type region to the conduction band of the n-type region; this is identical to the tunnel field-effect transistor (FET. When the SOI layer is extremely thin or narrow, other quantum-mechanical phenomena are expected. Details are discussed in Parts Three and Seven.

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3

Modern Applications of the pn Junction

A new stage of the pn-junction physics commenced with the discovery of the tunneling phenomenon [1]. Dr L. Esaki demonstrated tunneling in the pn junction structure in 1958 [1]. Since indirect bandgap materials, such as Ge and Si, have low tunneling probability (i.e., low tunneling current density), few scientists paid attention to the fabrication of Si tunnel devices [2]. In 1992, Dr T. Baba proposed the surface tunnel transistor (STT) using the epitaxial GaAs layer stack [3]; this idea is similar to the proposal by J.J. Quinn, G. Kawamoto, and B.D. McCombe [2]. Drs T. Uemura and T. Baba successfully observed negative conductance in STT in 1994 [4]. In 1996, a couple of papers on Si tunnel devices influenced the Si device technology field. Drs J. Koga and A. Toriumi published the paper titled 'Negative differential conductance in three-terminal silicon tunneling device' (a p^+n^+ diode with a metal oxide semiconductor (MOS) gate) [5]; this is a bulk-based STT working at 80 K. I also published the paper titled 'Negative conductance properties in extremely thin silicon-on-insulator insulated-gate pn-junction devices (silicon-on-insulator surface tunnel transistor)' as an application of the Lubistor [6]; this is an extremely thin SOI-based STT working at 90 K. Excitingly, Drs J. Koga and A. Toriumi demonstrated a thin SOI-based STT working at room temperature in IEEE 1996 IEDM [7]. This was a very exciting race as a result, although the timing of the three publications was indeed just a coincidence!

A recent notable event in pn-junction device history is the application of the Lubistor to the electrostatic discharge (ESD) protection circuit [8]; this is the first commercial application of the Lubistor. Since ESD protection circuits in conventional laser sheet imaging (LSI) used simple pn-junction devices, this was a significant event to the scientists and engineers investigating SOI technology.

Most recent and challenging studies are the proposals of the *i*-MOS [9], tunnel FET [10], and feedback FET [11]. I think that all these are advanced applications of the Lubistor. The *i*-MOS utilizes the surface enhancement of the avalanche breakdown of the pn junction [12,13]. The *i*-MOS device can produce a very small swing. However, scaled *i*-MOS transistors with low-voltage operation are not easily realized because the scaled device should have a wire-like

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structure; the small volume of the nano-scale wire needed restricts the total amount of carriers generated by the avalanche phenomenon because of the reduced density of the states. Therefore, engineers must reconsider the useful applications of the *i*-MOS transistor. The concept of the tunnel FET (TFET) closely follows the STT described in the above paragraphs. Since the tunneling process cannot produce a high-level current because of the high tunnel resistance, the tunnel FET should be applied to low-energy circuits. Some of the issues with the tunnel FET are addressed in Part Three. The idea of the feedback FET is unique and interesting. The device is still under study so its potential is not as clear. Recently, a couple of new device applications have been proposed [14–16]. These exotic device applications and the potential of the Lubistor are described in Parts Five and Seven.

Most readers will notice from this brief introduction that the pn junction is still *an important element* in the proposal of any new device, that is, *source of invention*. Therefore, the pn junction is expected to produce more interesting and more useful device applications in the future.

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Part Two

Physics and Modeling of SOI Lubistors – Thick-Film Devices

4

Proposal of the Lateral, Unidirectional, Bipolar-Type Insulated-Gate Transistor (Lubistor)

4.1 Introduction

Since the invention of the well-known point contact transistor by Shockley and his group [1] at Bell Laboratories, many innovative solid-state devices (the junction-type bipolar transistor, the field-effect transistor, etc.) have been developed. This chapter proposes the Lubistor, a lateral, unidirectional, bipolar-type insulated-gate transistor that exhibits triode-like current–voltage characteristics. The basic characteristics of this new device and the physical concepts underlying its operation are discussed here.

4.2 Device Structure and Parameters

A cross-sectional view of the Lubistor is shown in Figure 4.1. The Lubistor has three main structural features: (a) it has an n^+–n(or p)–p^+ structure, with a 'Type I' Lubistor having an n^+–n–p^+ structure and a 'Type II' Lubistor having an n^+–p–p^+ structure, schematically shown in Figure 4.1; (b) it has an insulated gate structure in the n (or p) region; and (c) the thickness of the n (or p) region is approximately equal to, or less than, the effective Debye length. The following text refers to the 'Type I' Lubistor.

The effective Debye length (L_{DE}) is defined as

$$L_{DE} = \sqrt{\frac{2\varepsilon_S k_B T}{q^2 N_D}}, \tag{4.1}$$

where ε_S is the permittivity of the semiconductor, k_B is Boltzmann's constant, T is the absolute temperature, q is the magnitude of electronic charge, and N_D is the majority-carrier

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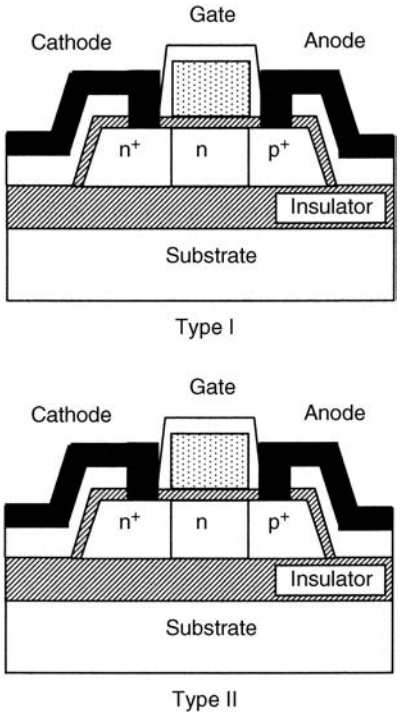

Figure 4.1 Cross-sectional view of the Lubistor. Reprinted with permission from Y. Omura, *Applied Physics Letters*, vol. 40, p. 528. Copyright 1982, American Institute of Physics.

concentration. We have chosen to look at the p^+–n–n^+ structure in this section. We call the p^+ region the anode and the n^+ region the cathode, paralleling the work on thyristors.

The Lubistor was fabricated on a buried oxide [2] formed by ion implantation of oxygen atoms into a monocrystalline silicon wafer. Dimensions of the fabricated Lubistor are shown in Table 4.1.

Table 4.1 Dimensions and doping concentrations for the fabricated Lubistor. Reprinted with permission from Y. Omura, *Applied Physics Letters*, vol. 40, p. 528. Copyright 1982, American Institute of Physics.

Parameters	Values [unit]
Gate length (L_G)	5 [μm]
Gate oxide thickness (t_{ox})	50 [nm]
Channel region thickness (t_S)	0.26 [μm]
Doping concentration in channel region	4×10^{14} [cm^{-3}]
Buried oxide thickness (t_{BOX})	0.47 [μm]

($L_{DE} = 0.29$ μm at 300 K.)

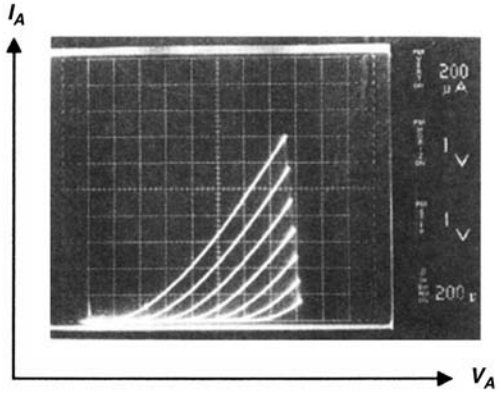

Figure 4.2 Typical current–voltage characteristics for the Lubistor. The $I_A - V_A$ curve shifts continuously toward the positive direction of V_A as the gate-to-cathode voltage increases. Reprinted with permission from Y. Omura, *Applied Physics Letters*, vol. 40, p. 528. Copyright 1982, American Institute of Physics.

4.3 Discussion of Current–Voltage Characteristics

The triode-like current–voltage characteristics shown in Figure 4.2 were obtained from the positive anode-to-cathode voltage V_A. The anode-to-cathode current, denoted by I_A, increases monotonically with V_A. A high current density, of the order of $\sim 10^5$ A cm^{-2}, is achieved. The I_A–V_A curve shifts continuously toward the positive direction of V_A as the gate-to-cathode voltage (V_G) increases.

According to Figure 4.2, the following empirical equation is obtained:

$$I_A = A[V_A - B(V_G - V_{FB})]^n \quad (2 < n < 3), \tag{4.2}$$

where A is a constant, B is a constant (less than unity), and V_{FB} is the flat-band voltage at which the band bending vanishes at the gate insulator/semiconductor interface. The current level depends only on the effective difference between the anode-to-cathode voltage and the gate-to-cathode voltage.

The physical concepts behind the Lubistor's operation are speculated to be as follows (see Chapter 5). The case where the channel region thickness (t_c) is approximately equal to or less than the effective Debye length (L_{DE}) can be taken as an example. As the accumulation layer thickness for the majority carriers is approximately equal to $(\pi/2)L_{DE}$, the majority-carrier (electrons in this case) concentration over the channel region [3,4] is enhanced as shown in Figure 4.3(a) for $V_G > V_{FB}$.

The *OFF* state is achieved at $B(V_G - V_{FB}) > V_A$. Near the anode junction, the effective potential difference between the gate electrode and the channel region is equal to $B(V_G - V_{FB}) - V_A$. As long as the $V_A < B(V_G - V_{FB})$ relationship holds, the number of majority carriers in the channel region is enhanced. This means that minority carriers are swept out of the channel region and that hole injection from the anode to the channel region is limited. Thus, a reverse-biased condition is effectively achieved across the anode junction. Electrons, which accumulate in the channel region, play a major role in that they increase the channel potential. However, they basically contribute nothing to the channel current.

The *ON* state is achieved at $V_A > B(V_G - V_{FB})$, as shown in Figure 4.3(b). The anode junction is effectively forwardly biased, by the amount of $V_A - B(V_G - V_{FB})$. A large number of holes are injected from the anode into the channel region; consequently, the hole concentration near the anode junction becomes higher than the electrode concentration.

It is believed that all the holes injected from the anode recombine in the channel region, which is suggested by the fact that the current magnitude is determined by the power of the supplied anode-to-cathode voltage [5]. This recombination of holes is followed by electron injection from the cathode. While most electrons recombine with holes in the channel region, some electrons partially reach the anode and are injected into it.

Additional experimental results are revealed in Reference [6], where some electrical characteristics of the offset-gate Lubistors are demonstrated. The offset-gate Lubistor reveals tetrode characteristics. Some experimental results of the offset-gate Lubistor are introduced in the following chapter, which also discusses device physics.

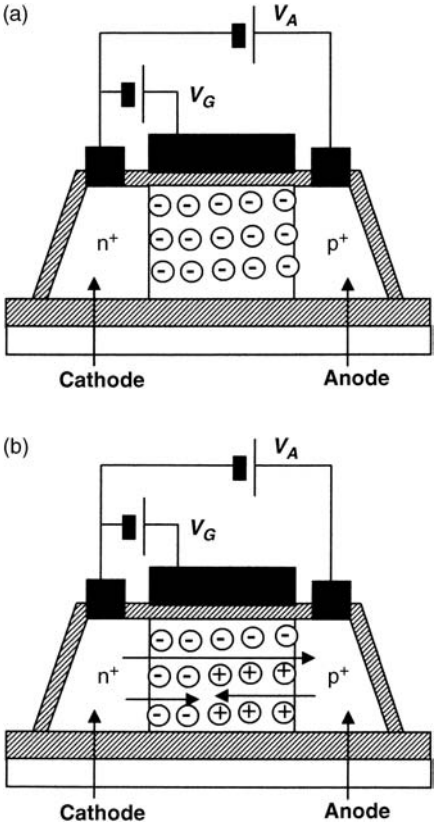

Figure 4.3 Physical concepts for the Lubistor's operation: + and – stand for electron and hole. (a) *OFF* state: $B(V_G - V_{FB}) > V_A$. Majority carriers (electrons) are enhanced over the entire channel region. (b) *ON* state: $B(V_G - V_{FB}) < V_A$. Minority carriers (holes) are injected from the anode and recombine in the channel region. Most electrons injected from the cathode recombine with holes. Electrons partially reach the anode and are injected into it. Reprinted with permission from Y. Omura, *Applied Physics Letters*, vol. 40, p. 528. Copyright 1982, American Institute of Physics.

4.4 Summary

I have proposed and fabricated a lateral, unidirectional, bipolar-type insulated-gate transistor (Lubistor), which has a lateral p^+-n-n^+ (or n^+-p-p^+) diode structure on top of an insulator. The Lubistor aligns the insulated gate on top of the n (or p) region, and the thickness of this n (or p) region is approximately equal to, or less than, the effective Debye length. Basically the Lubistor reveals triode characteristics. Though preliminary experimental results are introduced here, there exist a couple of substantial questions. One of which is how is the bipolar current successfully controlled by the insulated gate? The physics of Lubistor operation is discussed in detail in the following chapter.

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5

Experimental Consideration for Modeling of Lubistor Operation

5.1 Introduction

Many extensive efforts have been made [1,2] to apply the SOI technique to achieve high-speed, high-packing density MOS LSIs, as the SOI structure is not only applicable to high-speed devices but also to high-voltage devices [3]. In the light of this knowledge, I proposed a new device (Lubistor) using a thin silicon film on a buried oxide layer [4,5]. The Lubistor is one of the transistors that show triode-like current voltage characteristics [6,7] and is based on a new insulated-gate bipolar transistor concept. The idea behind the Lubistors is to control the forward-biased pn-junction-diode current effectively in order to realize devices with high drivability for application in SOI LSIs and in magnetosensitive devices [8,9]. In particular, the most significant purpose is to realize the *OFF* state of the anode current under enhancement-mode insulated-gate bias. Although some speculation about its operation mechanism was reported in Reference [5], several significant points remained unclear.

In this chapter, an experimental characterization of the Lubistor and a simplified analysis are introduced to speculate on the operation mechanism. Some kinds of Lubistors are utilized to characterize Lubistor operation. The following sections mainly describe the characteristics of the p^+–p–n^+ (Type II) Lubistor.

5.2 Experimental Apparatus

A cross-sectional view of the Lubistor is shown in Figure 5.1(a). Features of this structure are as follows:

1. A gate-controlled p^+–p–n^+ (Type II) or p^+–n–n^+ (Type I) diode on an insulator.
2. An oxygen-doped silicon (ODS) layer that acts as an electric-field shielding (EFS) layer [10,11] is placed between the SOI layer and the buried oxide layer.

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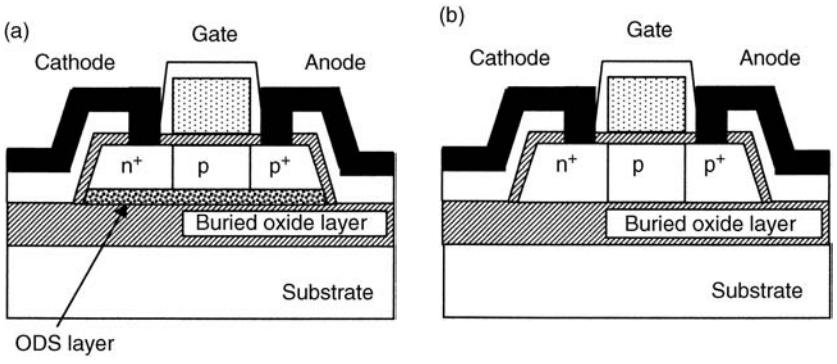

Figure 5.1 Cross-sectional view of Lubistors. (a) Lubistor with an ODS layer (A type), (b) Lubistor without an ODP layer (B type).

For comparison, a device similar to the Lubistor, shown in Figure 5.1(b), was also fabricated. This device has no ODS layer [12]. The *I–V* characteristics of these devices were measured. Special devices with tap electrodes, one of which is shown in Figure 5.2, were also fabricated, and potential profiles were measured. The behavior of majority and minority carriers in these devices was studied.

The major steps of the fabrication process are shown in Figure 5.3. A buried oxide layer was formed by oxygen ion implantation into n-type or p-type (100) Si wafers 75 mm in diameter. The following two types of oxygen implantation conditions were employed:

1. Condition A: an ODS layer was formed between the SOI layer and the buried oxide layer [10,11].
   Energy: 150 kV
   Dose of oxygen atoms: $1.8 \times 10^{18}\,\mathrm{cm}^{-2}$
   Ion-beam current density on the wafer: 17–19 $\mu\mathrm{A\,cm}^{-2}$.
2. Condition B: no ODS layer was formed [12].
   Energy: 150 kV
   Dose of oxygen atoms: $2.4 \times 10^{18}\,\mathrm{cm}^{-2}$
   Ion-beam current density on the wafer: 23–25 $\mu\mathrm{A\,cm}^{-2}$.

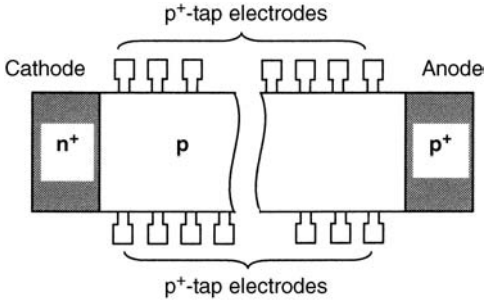

Figure 5.2 Lubistor layout with taps.

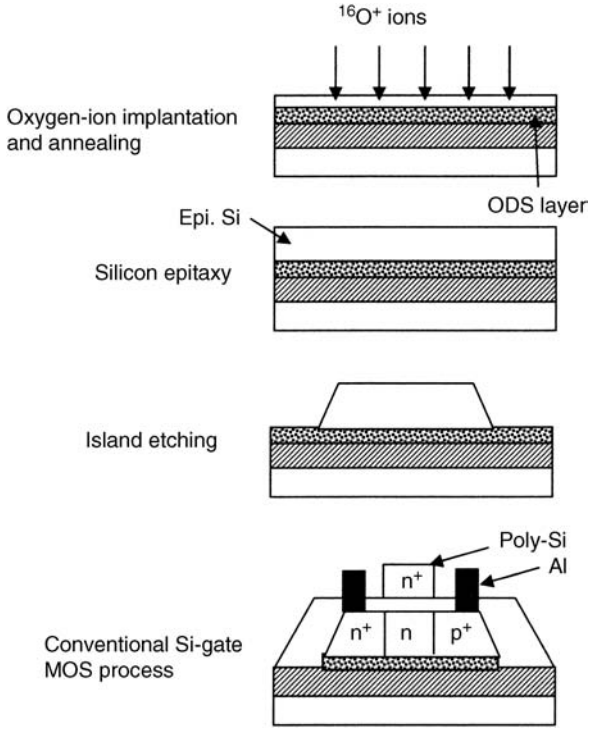

Figure 5.3 Fabrication steps of Lubistors with or without the ODS layer.

After oxygen implantation, crystallinity of the damaged SOI layer was improved through high-temperature annealing in an N_2 ambient and an epitaxial silicon layer was formed on the top of the SOI layer. The usual fabrication process for MOS devices was utilized after silicon island patterns for active regions were made by means of reactive ion etching. Major device parameters are summarized in Table 5.1.

Table 5.1 Device parameters of Lubistors

	Values [unit]	
Parameters	Type A[a]	Type B[b]
Gate oxide thickness (t_{ox})	80 [nm]	50 [nm]
SOI layer thickness (t_S)	40 [nm]	50 [nm]
Gate length (L_G)	10, 20, 50 [μm]	
Gate width (W_G)	50 [μm]	30 [μm]
Doping concentration of SOI layer (N_D)	1×10^{15} [cm^{-3}]	
Buried oxide thickness (t_{BOX})	370 [nm]	500 [nm]
EFS layer thickness	80 [nm]	—

[a]With EFS layer.
[b]Without EFS layer.

5.3 Current–Voltage Characteristics of Lubistors

Two different current–voltage characteristics of Type II Lubistors are shown in Figure 5.4; Figure 5.4(a) shows the terminal configuration and Figure 5.4(b) and (c) show I_K–V_K characteristics with and without the ODS layer, respectively. Here, the anode common configuration was employed; the cathode-to-anode voltage and the gate-to-anode voltage are negative values. In Figure 5.4(b), the cathode current is cut off in spite of the enhancement mode at the negative gate bias, which is a salient feature of the original Lubistor. On the other hand, in Figure 5.4(c), the cathode current is not cut off at the enhancement mode gate bias in the case of the device without the ODS layer. Thickness of the SOI layers of these devices is less than the Debye length. Therefore, the most important previous hypothesis, that the SOI layer thickness must be less than the Debye length in order to achieve the *OFF* state, must be revised.

The cathode current (I_K) dependence on the cathode-to-anode voltage (V_K) and the gate length (L_G) of Lubistors are shown in Figures 5.5 and 5.6, respectively. From the figures, the following empirical relationship is obtained:

$$I_K \propto \frac{V_K^n}{L_G^m}, \tag{5.1}$$

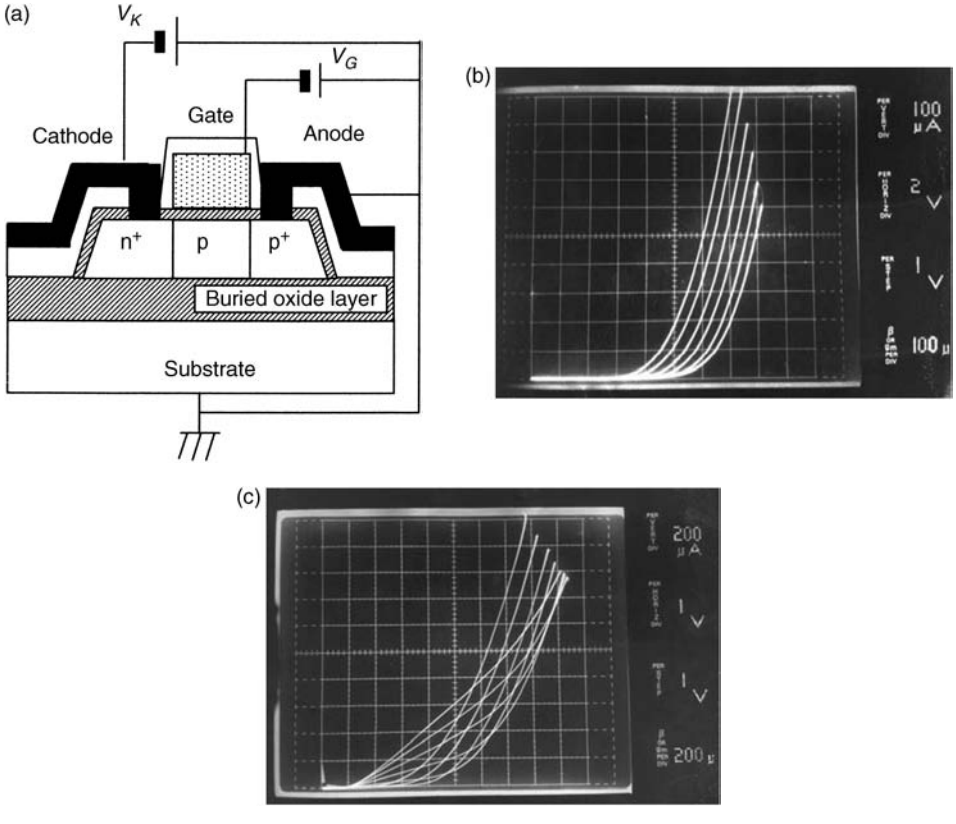

Figure 5.4 I_K–V_K characteristics of Type II Lubistors with L_G of 10 μm: (a) terminal configuration, (b) with the ODS layer (A type) for 0 V > V_G > −7 V, (c) without the ODS layer (B type) for 0 V > V_G > −7 V.

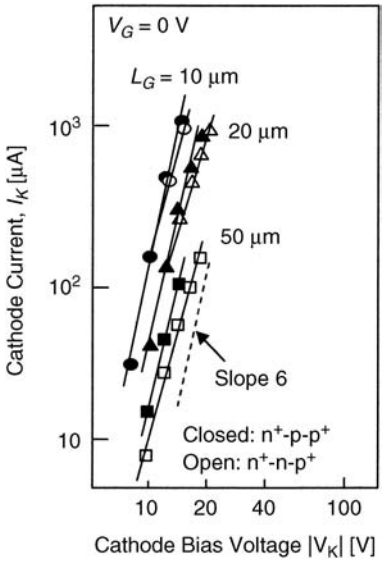

Figure 5.5 I_K–V_K characteristics of Lubistors for various gate lengths (A type).

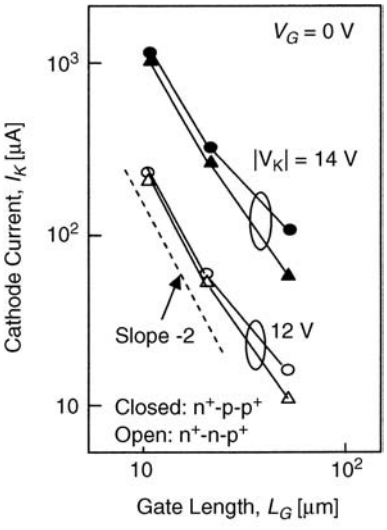

Figure 5.6 I_K dependence on gate length for various V_K conditions (A type).

where $n \sim 6$ and $m \sim 2$ for short-gate devices and $n \sim 6$ and $m < 2$ for long-gate devices. This indicates that the nature of the cathode current cannot be attributed mainly to surface-bound carrier drift in the short-gate devices, because I_K is not in linear proportion to the inverse of the gate length L_G. However, it is considered that the nature of the cathode current includes the contribution from the drift current in the long-gate devices.

Furthermore, we have

$$\frac{I_K(\mathrm{n}^+ - \mathrm{p} - \mathrm{p}^+)}{I_A(\mathrm{p}^+ - \mathrm{n} - \mathrm{n}^+)} \approx 1, \tag{5.2}$$

where $I_K(\mathrm{p}^+\text{–p–n}^+)$ denotes the cathode current of the Type II Lubistor and $I_A(\mathrm{p}^+\text{–n–n}^+)$ denotes the anode current of the Type I Lubistor for short-gate Lubistors, and

$$\frac{I_K(\mathrm{n}^+ - \mathrm{p} - \mathrm{p}^+)}{I_A(\mathrm{p}^+ - \mathrm{n} - \mathrm{n}^+)} \approx 2, \tag{5.3}$$

for long-gate Lubistors. I_K was measured for the anode common configuration and all biases are negative. I_A was measured for the cathode common configuration and all biases are positive.

Figure 5.6 and Equation (5.2) suggest that high-concentrated electrons and holes play an important role in determining the Lubistor bipolar operation of short-gate devices. On the other hand, Equation (5.3) suggests that minority carriers play a major role in the operation of long-gate devices, because the current ratio is nearly equal to the carrier mobility ratio.

Detailed current–voltage characteristics of the Lubistor are shown in Figures 5.7 and 5.8 for various gate lengths. Devices are set in the anode common configuration. In general, no

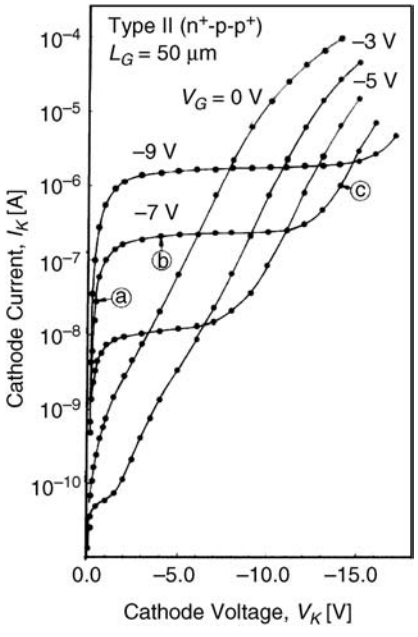

Figure 5.7 I_K–V_K characteristics of a Type II Lubistor with L_G of 50 μm for various gate biases (A type).

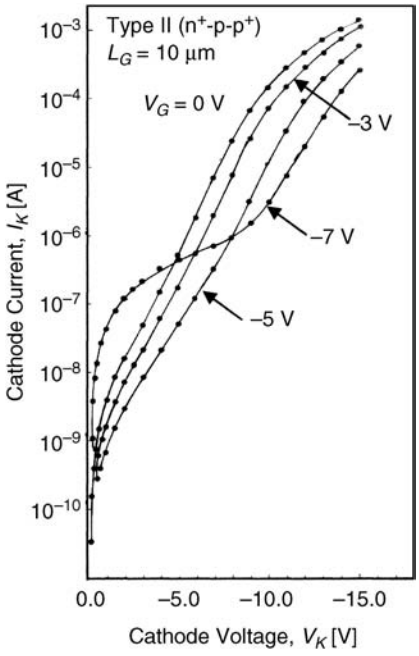

Figure 5.8 I_K–V_K characteristics of a Type II Lubistor with L_G of 10 μm for various gate biases (A type).

significant difference in the characteristics between the two cases was found. Plateaus appear at the negative gate bias below −5 V.

For $L_G = 50$ μm, holes (majority carriers) accumulate under the gate oxide layer due to the negative gate bias in region (a), so that the cathode current is ruled mainly by the pn-junction forward-bias current. This speculation is supported by the fact that the more increasingly negative gate bias leads to a sharper cathode current slope. In region (b), the increasingly negative anode bias leads to more negative potential in the p-type region, which reduces the effective gate-induced electric field and therefore a reduction in the hole concentration. Electron injection from the cathode is followed by hole drift from the anode in order to maintain charge neutrality and recombination. The hole concentration reduction accentuates the suppression of the electron injection from the cathode, saturating the cathode current. In region (b), however, a negative gate bias beyond the threshold voltage of the MOS system generates leakage current between the anode and the cathode, which reduces the *off-sustain voltage* between the anode and the cathode.

In region (C), the gate potential measured from the p-type region potential becomes positive near the cathode junction. In this condition, many electrons can exist in the p-type region near the cathode, indicating that many electrons are injected from the cathode. Some of these electrons recombine near the anode while others are injected into the anode. On the other hand, hole injection into the anode depends on gate length, which is supported by the information given in the previous section (see Figure 5.5).

Here, the roles of the ODS layer should be considered. Hereafter, I will call the layer the *electric-field shielding (EFS) layer*, because the layer acts as such a layer; theoretical bases are

described in Chapter 8. Without the EFS layer, the negative gate bias induces a substantial number of holes (majority carriers) under the gate oxide and electrons (minority carriers) at the bottom of the SOI layer. This means that a very large cathode current flow exists owing to electron induction in region (b), as shown in case (b) in Figure 5.1. On the other hand, the EFS layer successfully suppresses electron induction at the bottom [10,11], which results in the cathode current reduction seen in this region, as shown in case (a) in Figure 5.1. Therefore, the EFS layer is necessary if the Lubistor is to achieve its original characteristics whereby the anode current is cut off by the enhancement mode gate bias.

The EFS layer has a large number of localized trap levels located near the center of the forbidden band gap [11]; the Fermi level is pinned near the midgap. An external electric field charges a lot of traps, and the EFS layer blocks the external electric field through those charged traps [11]. The EFS layer then causes the SOI layer to deplete upward from the bottom of the SOI layer. At the same time, the EFS layer does not generate any inversion layer between the silicon layer and itself. As a result, both surface- and buried-channel MOSFETs effectively contribute to the *normally off mode* [10,13].

5.4 Lubistor Potential Profiles and Features

The potential profile of the Type II Lubistor is shown in Figure 5.9. The condition of $V_G = 0\,\mathrm{V}$ corresponds to the *ON* state and that of $V_G = -7\,\mathrm{V}$ to the *OFF* state:

1. *ON* state
   In the *ON* state, a large potential drop exists only near the anode. Both the n^+-tap potential and the p^+-tap potential near the cathode are nearly equal to the cathode potential, which means that electron concentration is high and hole concentration is low near the cathode. This result corresponds to Equation (5.3) because the gate length of this device is very long. In the case of the short gate, however, the above-mentioned situation will not hold according to Equation (5.2), that is, both the electron and hole concentrations are high near the cathode. The potential at both the n^+ tap and p^+ tap near

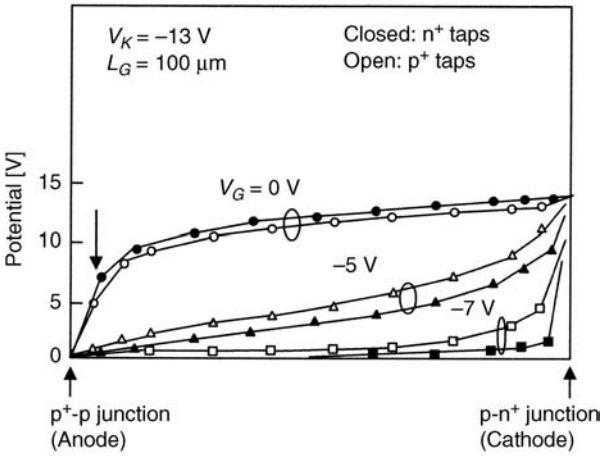

Figure 5.9 Potential profiles in a Type II Lubistor (A type).

the anode approach the anode potential; that is, hole concentration is high while electron concentration is low, independent of gate length.

2. *OFF* state
   In the *OFF* state, a large potential drop exists only near the anode junction. One can estimate the carrier concentration from the potential profile. Near the anode, the p^+-tap potential is almost equal to the anode potential, indicating that the accumulation layer of majority carriers (holes in this case) extends from the anode toward the cathode. On the other hand, a large difference exists between the cathode and n^+-tap potentials near the anode, which indicates that few electrons appear near the anode.

   Near the cathode, the p^+-tap potential is more negative than the n^+-tap potential, which means that a depletion layer with a high anode-to-cathode electric field exists near the cathode. A large part of the cathode-to-anode bias is sustained by this depletion layer. It cannot be considered, however, that this depletion layer reaches the cathode junction, because the contact between this depletion layer and the cathode junction does not maintain the *OFF* state.

5.5 Discussion

5.5.1 Simplified Analysis of Lubistor Operation

Neudeck *et al*. [14,15] showed a model for *a*-Si:H thin-film transistor (TFT) devices. Current characteristics of the devices in the low level are similar to those of Lubistors, suggesting that the mechanism of Lubistor operation is similar to that of the *a*-Si:H TFT. They mainly studied the drain current characteristics in the low level.

Since the Lubistor has a pn junction as a terminal, the operation mechanism may differ from the TFT at high current levels. In this section, a simplified analysis is introduced to speculate on Lubistor operation. A structural model is shown in Figure 5.10. Label L_G denotes the gate

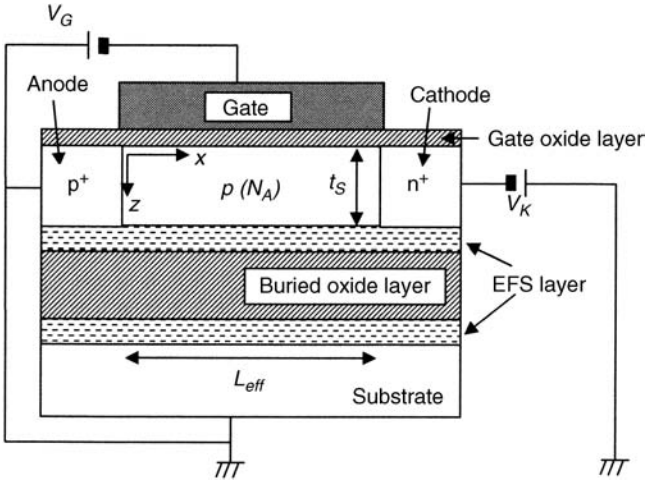

Figure 5.10 Schematic device model for a one-dimensional approximation.

length, label t_S the SOI layer thickness, label N_A the doping concentration in the SOI layer, and label V_G the gate-to-anode bias. The gate oxide layer thickness is assumed to be equal to t_{ox}.

In this structure, the following important assumptions are made for the analysis:

1. The analysis is restricted to the *ON* state.
2. The active SOI layer thickness is less than the Debye length. Thus the majority carriers fulfill the SOI layer in the enhancement mode.
3. At the vicinity of the SOI layer/EFS layer interface, the silicon region depletes and both electrons and holes rarely exist there in the case where the gate-to-anode bias is nearly equal to the flat-band voltage of the device.
4. The SOI layer thickness is much smaller than the gate length.

The fourth assumption allows the use of the one-dimensional approximation along the anode-to-cathode direction. In this section, the analysis starts from the following simple Poisson equation and the current equations:

$$\frac{d^2V(x)}{dx^2} = \frac{q[n(x) - p(x) - N_A]}{\varepsilon_S}, \tag{5.4}$$

$$\frac{J_n(x)}{q\mu_n} = n(x)E(x) + \frac{k_BT}{q}\frac{dn(x)}{dx}, \tag{5.5}$$

$$\frac{J_p(x)}{q\mu_p} = p(x)E(x) - \frac{k_BT}{q}\frac{dp(x)}{dx}, \tag{5.6}$$

$$\frac{d}{dx}\left[\frac{J_n(x)}{q\mu_n} - \frac{J_p(x)}{q\mu_p}\right] = \left(\frac{1}{\mu_n} - \frac{1}{\mu_p}\right)R, \tag{5.7}$$

where $V(x)$ is the one-dimensional potential function measured from the anode electrode, $n(x)$ the electron concentration, $p(x)$ the hole concentration, ε_S the dielectric constant of silicon, q the electronic charge, $J_n(x)$ the one-dimensional electron current density, $J_p(x)$ the one-dimensional hole current density, μ_n the electron mobility, μ_p the hole mobility, $E(x)$ the electric field along the anode-to-cathode direction, R the recombination rate, k_B Boltzmann's constant, and T the temperature in K.

Under the one-dimensional approximation, the charge in the SOI layer, $q(n - p - N_A)$, is expressed as

$$q[n(x) - p(x) - N_A] = \frac{C_{ox}}{t_S}[V_{GF} - V(x)], \tag{5.8}$$

$$V_{GF} = V_G - V_{FB}, \tag{5.9}$$

where V_{FB} is the flat-band voltage. On solving Poison's equation, Equation (5.8) and the following boundary conditions can be employed:

$$V(0) = \frac{dV(0)}{dx} = 0 \tag{5.10a}$$

at the anode junction interface and

$$V(L_{eff}) = V_K \tag{5.10b}$$

and

$$\frac{dV(L_{eff})}{dx} \cong 0 \tag{5.10c}$$

at the cathode junction interface. The solution of Poisson's equation is given by

$$V(x) = V_{GF} - \left(2a_1 V_{GF}^2 + 4C_1\right)\sin[-\sqrt{a_1}(x + C_2)], \tag{5.11}$$

$$a_1 = \frac{\varepsilon_{ox} t_S}{\varepsilon_S t_{ox}}, \tag{5.12}$$

$$C_1 = a_1\left(0.5V_K^2 - V_{GF}V_K\right), \tag{5.13}$$

$$C_2 = -\left(\frac{1}{\sqrt{a_1}}\right)\sin^{-1}\left[\frac{0.5V_{GF}}{a_1(V_{GF} - V_K)^2}\right]. \tag{5.14}$$

On the other hand, the current equations can be solved if the model of recombination rate R is given. Here, R is, for simplicity, expressed as

$$R = \frac{n(x)}{\tau_n}, \tag{5.15}$$

where τ_n is the electron lifetime.

The minority carrier lifetime is on the order of 10^{-9} s in real Lubistors and the diffusion length of carriers is about 1 μm. The diffusion component of the current equation can be neglected since the gate length is much longer than the diffusion length of minority carriers. From Equation (5.7), the following solution is obtained:

$$n(x) = -\frac{\tau_n \mu_n a_1}{b+1}[V_{GF} - V(x)]\{a_2[V_{GF} - V(x)] - N_A\}, \tag{5.16}$$

$$a_2 = \frac{\varepsilon_{ox} t_S}{q t_{ox}}, \tag{5.17}$$

$$b = \frac{\mu_n}{\mu_p}, \tag{5.18}$$

where the following relations are used:

$$n(x) - p(x) = a_2[V_{GF} - V(x)] - N_A, \tag{5.19}$$

$$\frac{dE(x)}{dx} = -a_1[V_{GF} - V(x)]. \tag{5.20}$$

The total current density, $J(x)$, at the long-channel limit can be calculated from Equations (5.5), (5.6), (5.11), and (5.16). The final form is expressed as

$$J(x) = -\left(\frac{q\tau_n\mu_n\mu_p a_1}{L}\right)\frac{V_1 + \dfrac{k_B T}{q}(b+1)}{(b+1)V_2}, \tag{5.21}$$

$$V_1 = a_2\frac{(V_{GF} - V_K)^3}{3} - \frac{N_A(V_{GF} - V_K)^2}{2} - a_2\frac{V_{GF}^3}{3} + \frac{N_A V_{GF}^2}{2}, \tag{5.22}$$

$$V_2 = (V_{GF} - V_K)[a_2(V_{GF} - V_K) - N_A] - V_{GF}(a_2 V_{GF} - N_A). \tag{5.23}$$

From the above solution, a few of the important points to be summarized are listed below:

1. $J(x)$ is proportional to the inverse of L_G at the long-gate limit. This is supported by the experimental results shown in Figure 5.6.
2. $J(x)$ is a function of the power of $(V_{GF} - V_K)$. This is supported by the experimental results basically shown in Figure 5.5.
3. It is predicted that thinning the gate insulator leads to larger currents.

We can emphasize that the above simplified analysis basically supports the more significant experimental results.

5.5.2 *On the Design of Lubistors*

In the 1980s, little experimental data were available for device design. However, it is likely that the gate length (L_G) the gate width (W_G), the SOI layer width (t_S), and the doping concentration (N_D) will be the main factors determining the I_K–V_K characteristics of Lubistors. Thus, the following points may be made with respect to the design of Type I Lubistors:

1. The dependence of cathode-to-anode current (I_K) on device dimensions is expressed as

$$I_K \propto \left(\frac{W_G}{L_G^2}\right)(V_K - r_1 V_G)^6 \qquad \text{(short-gate devices)}, \tag{5.24a}$$

$$I_K \propto \left(\frac{W_G}{L_G}\right)(V_K - r_2 V_G)^6 \qquad \text{(long-gate devices)}, \tag{5.24b}$$

where r_1 and r_2 are constants.

2. SOI layer thickness must be smaller than the thickness of the depletion layer (W_d), which is generated upwards from the bottom of the SOI layer due to the EFS layer, that is,

$$t_S < \sqrt{\frac{2\varepsilon_S \phi_F}{qN_D}}, \tag{5.25}$$

$$\phi_F = \left(\frac{k_B T}{q}\right)\ln\left(\frac{N_D}{n_i}\right), \tag{5.26}$$

where ϕ_F is the Fermi potential and n_i is the intrinsic carrier concentration.

3. The gate length must be longer than the diffusion length of minority carriers from the standpoint of the current controllability provided by the gate electrode. Further discussion in detail is presented in the following section.

5.6 Summary

An experimental characterization of Lubistors was carried out in detail by the employment of SIMOX technology. As a result, the following points have been concluded:

1. An electric-field shielding (EFS) layer is necessary to achieve the original Lubistor characteristic whereby the anode current is cut off by the enhancement mode gate bias. This is based on the facts that the EFS layer makes the SOI layer deplete upwards from the bottom of the SOI and that it does not generate an inversion layer between the SOI layer and itself.
2. Current–voltage characteristics of Lubistors indicate that they are basically bipolar devices. High-concentrated electrons and holes play an important role in short-gate Lubistors while minority carriers play the main role in long-gate Lubistors.
3. In the *ON* Lubistor state, a large potential drop exists only near the high–low junction terminal. This drop must be supported by the depletion region.
4. In the *OFF* Lubistor state, a large potential drop exists only near the pn-junction terminal. This drop must be supported by the depletion layer. However, this layer does not reach the pn-junction terminal because its contact with the pn-junction terminal does not maintain the *OFF* state.

This simplified analysis basically supports the more significant experimental results.

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6

Modeling of Lubistor Operation Without an EFS Layer for Circuit Simulations

6.1 Introduction

Recent progress in device integration technology has been significant, and the gate length of individual MOSFETs is already below 0.1 μm at the research level [1–3]. Given this background, the SOI MOSFET structure has attracted considerable attention since it can eliminate the technological barriers to device miniaturization. This structure has several advantages such as its suppression of the short-channel effect, low voltage and high-speed operation, and low production costs [4,5]. Furthermore, the SOI structure is being exploited to build new application paradigms [6–8], such as optical waveguides [9] and light emission diodes [10]. Such developments are essential because advances in broadband communication technologies and high-frequency analog technologies are urgently needed.

Throughout the history of semiconductor devices, one fundamental goal has been to clarify the basic characteristics of SOI devices [11]. However, few studies have examined the behavior of thin-film SOI pn-junction devices (Lubistors) [12–15]. Since the SOI structure is expected to support digital applications [16], as well as analog applications [17], its basic operation mechanisms must be elucidated.

In this chapter, SOI Lubistors [12,18] are investigated with the goal of achieving useful circuit simulations. Equivalent circuit models for circuit applications are presented. Device simulations of SOI Lubistors are performed to assist the detailed analysis of the operation mechanisms of Lubistors. Equivalent circuit models that reproduce the device characteristics are proposed for circuit simulations.

6.2 Device Structure and Measurement System

A schematic cross-section of an SOI Lubistor is shown in Figure 6.1. Although the basic device structure is analogous to that of SOI MOSFETs, the device differs in having a lateral p^+–n–n^+

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

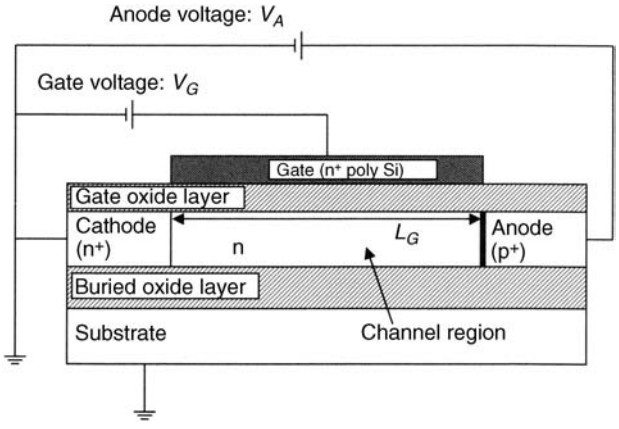

Figure 6.1 Schematic cross-section of an SOI Lubistor. Reproduced by permission of The Electrochemical Society from S. Wakita and Y. Omura, Device models of SOI insulated-gate p-n junction devices, *Journal of Electrochemical Society*, vol. 150, pp. G816–G820, 2003.

junction structure. There are three main regions: anode, channel, and cathode. The devices considered in this study were fabricated on SOI wafers made by implanted oxygen (SIMOX) technology [19]. Here, we examine two kinds of devices (Device A and Device B). Device A has an SOI layer of poor quality while Device B has an SOI layer of normal quality; their differences help us understand device operations as mentioned later. Device A had an SOI layer thickness (t_s) of 80 nm, gate oxide layer thickness (t_{ox}) of 80 nm, and buried oxide layer thickness (t_{BOX}) of 380 nm. The gate width W_G was 50 μm and the gate length L_G was 10 μm. Device B had an SOI layer thickness (t_s) of 200 nm, gate oxide layer thickness (t_{ox}) of 20 nm, and buried oxide layer thickness (t_{BOX}) of 380 nm. The parameters of the devices are listed in Table 6.1.

The DC characteristics of the SOI Lubistors were measured using the cathode common configuration, as shown in Figure 6.1. The DC characteristics were measured using an

Table 6.1 Device parameters of fabricated devices. Reproduced by permission of The Electrochemical Society from S. Wakita and Y. Omura, Device models of SOI insulated-gate p-n junction devices, *Journal of Electrochemical Society*, vol. 150, pp. G816–G820, 2003.

	Values [unit]	
Parameters	Device A	Device B
Gate length (L_G)	10, 20, 50 [μm]	10 [μm]
Gate width (W_G)	50 [μm]	50 [μm]
SOI layer thickness (t_s)	80 [nm]	200 [nm]
Gate oxide layer thickness (t_{ox})	80 [nm]	20 [nm]
Buried oxide layer thickness (t_{BOX})	380 [nm]	380 [nm]
SOI body doping concentration (n type)	1×10^{15} [cm^{-3}]	1×10^{15} [cm^{-3}]
Substrate doping concentration (n type)	1×10^{15} [cm^{-3}]	1×10^{15} [cm^{-3}]
Gate doping concentration (n type)	1×10^{20} [cm^{-3}]	1×10^{20} [cm^{-3}]
Anode doping concentration (p type)	1×10^{20} [cm^{-3}]	1×10^{20} [cm^{-3}]
Cathode doping concentration (n type)	1×10^{20} [cm^{-3}]	1×10^{20} [cm^{-3}]

HP4156B precision semiconductor parameter analyzer; bias parameters ranged from 0V to 7V for both anode and gate voltages.

6.3 Equivalent Circuit Models of an SOI Lubistor

6.3.1 Device Simulation

Various applications of SOI Lubistors can be expected because they offer both the non-saturation current characteristics of the pn-junction and saturation current characteristics of MOSFETs. I demonstrate a possible application to a neural logic element [14], while S. Voldman of IBM proposed their application to ESD protection circuits [16,20]. However, device operation mechanisms and equivalent circuit models, which are necessary for realizing circuit applications, have not been studied in sufficient detail. In this section, the operation mechanisms of the SOI Lubistor are examined in detail by a commercial semiconductor device simulator [21] (ISETCAD).

In trial simulations, physical parameters of the device were adjusted to match the *I–V* characteristics of actual devices. Nominal values of device parameters of the measured devices are shown in Table 6.1. Representative *I–V* characteristics of an actual device (Device A) with L_G of 10 μm are shown in Figure 6.2(a) . Non-saturation current characteristics appear under the condition of low gate voltages and high anode voltages. An identical device structure (two-dimensional) was assumed in the device simulations, which were carried out under bias conditions identical to the experiments. The simulations used the materials' default values for physical parameters, such as minority carrier lifetime and low-mobility parameters (See Table 6.2). Drift-diffusion equations were used for transport analysis; the following physical models were also applied [21]:

1. Shockley–Read–Hall statistics and Auger recombination models [22].
2. Mobility model including doping dependence, high-field saturation of carrier velocity, and degradation due to the electric field normal to the silicon–oxide interface [23].
3. Effective intrinsic carrier density model based on Slotboom's bandgap narrowing model [24].

Simulation results of the device with $L_G = 10$ μm are shown in Figure 6.3(a) . They are quite different from the characteristics of the actual device; the current saturation does not appear in the medium anode voltage region and the magnitude of the simulated anode current is two orders larger than that of the experimental result. Furthermore, the anode current is independent of the gate voltage. I examined the current distribution inside the device; holes and electrons injected into the channel region from the anode and the cathode, respectively, pass through the channel region with virtually no recombination. The characteristic difference is due to the very long diffusion length assumed in the simulated device. According to pn-junction theory, the diffusion length of carriers is given by the square root of the product of the diffusion constant and lifetime [20]; the diffusion constant is tied to carrier mobility by Einstein's relation in the equilibrium state. The actual devices used for the comparison had many dislocations because a high oxygen-dose SIMOX wafer [19] was used, so the quality of the SOI layer is inferior to modern production levels; a lot of defects exist in the SOI layer, and both the lifetime and mobility are smaller than those achievable with current technologies. It follows that it should be possible to compensate for the difference between the experiment and

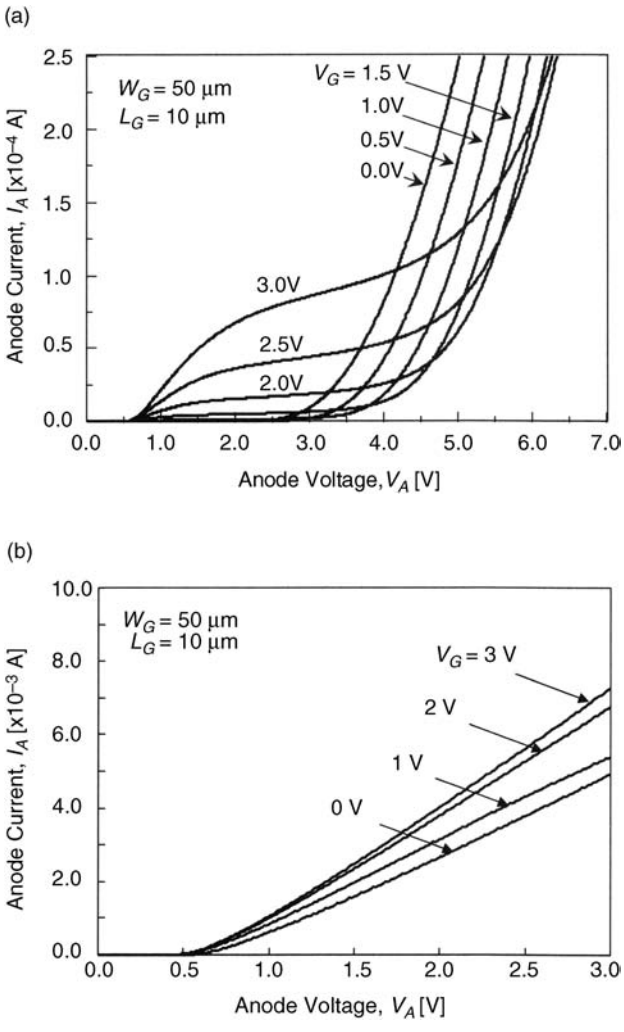

Figure 6.2 Current versus voltage characteristics of a fabricated device with a 10 μm gate. Non-saturation current characteristics appear under low gate voltages and high anode voltages. (a) Experimental results (Device A). (b) Experimental results (Device B). Reproduced by permission of The Electrochemical Society from S. Wakita and Y. Omura, Device models of SOI insulated-gate p-n junction devices, *Journal of Electrochemical Society*, vol. 150, pp. G816–G820, 2003.

the simulation results by adjusting the simulated lifetime and mobility. The generation and recombination of carriers in semiconductors is governed by Shockley–Read–Hall (SRH) statistics. Accordingly, the refined simulations used adjusted physical parameters: the lifetime of 10^{-12} s and the mobility of 100 cm^2/V s for both electrons and holes (see Table 6.2). These features of smaller lifetime and mobility have already been verified experimentally; we saw a minority carrier lifetime of 1 ns (experimental), not 1 ps. This difference cannot be attributed to interface states or charges inside oxide layers because such an assumption does not explain the experimental results. According to the TEM observation, it is known that there are point

Table 6.2 Physical parameters in device simulations. Reproduced by permission of The Electrochemical Society from S. Wakita and Y. Omura, Device models of SOI insulated-gate p-n junction devices, *Journal of Electrochemical Society*, vol. 150, pp. G816–G820, 2003.

	Default values[b]		Modified values[a]	
Physical parameters [unit]	Electrons	Holes	Electrons	Holes
Lifetime [s]	10^{-7}	10^{-7}	10^{-12}	10^{-12}
Low-field mobility [cm^2/V s]	1417	470	100	100

[a]These are used for analysis of Device A.
[b]These are used for analysis of Device B.

defects and micro twins near the SOI layer/buried oxide layer in the SIMOX substrate fabricated around the 1990s; it is anticipated that such defects degrade the lifetime of minority carriers. Improved simulation results are shown in Figure 6.3(b).

Simulated *I–V* characteristics match the experimental results well; namely, the physical model must be accurately described if we are to reproduce the experimental current–voltage characteristics. In order to demonstrate the validity of the modified physical parameters, I show the current–voltage characteristics at a low anode voltage for various gate voltage conditions in Figure 6.4. Figure 6.4(a) shows the experimental results and Figure 6.4(b) the device simulation results. It can be clearly seen that the simulation results match the experimental results well.

Device B, on the other hand, yielded a normal diode-like characteristic (measured) as shown in Figure 6.2(b); we verified experimentally that Device B had a high-quality SOI layer. The current–voltage characteristics basically match the simulation results shown in Figure 6.3(a); the lower anode current in Figure 6.2(b) is due to lower carrier mobility. We can understand that holes and electrons injected into the channel region from the anode and the cathode, respectively, pass through the channel region with virtually limited recombination. The characteristic difference from Figure 6.2(a) is due to the very long diffusion length, as expected.

After conducting many simulations of Device A, we found that there are two operation modes and that activation is controlled by the relation between gate voltage V_G and anode voltage V_A. We first consider the case of $V_G > V_A$. In this case, the electron accumulation layer is formed in the channel region. The accumulation layer is confined by the SOI layer and the carrier density depends on gate voltage V_G. Accordingly, the device behaves like a surface accumulation mode nMOSFET. The nMOSFET operates at the saturation condition shown in Figure 6.5(a).

Next, we consider the case of $V_G < V_A$. Simulation results indicate that the hole inversion layer is formed on the anode side of the channel region. Here we assume a virtual pMOSFET having a p^+ source terminal (p^+ anode in the real device); the n^+ cathode is a virtual drain for the virtual pMOSFET. A virtual gate voltage ($V_A - V_G$) and a virtual drain voltage (V_A) are added to the virtual pMOSFET, which operates at the saturation condition shown in Figure 6.5(b). In this operation condition, non-saturation current characteristics appear as the anode voltage increases; this idea is utilized in the following section to develop an equivalent circuit model for the device.

We can freely switch between these two operation modes by setting the gate and anode voltages appropriately. The fundamental characteristics described here are utilized to create equivalent circuit models of the SOI Lubistor.

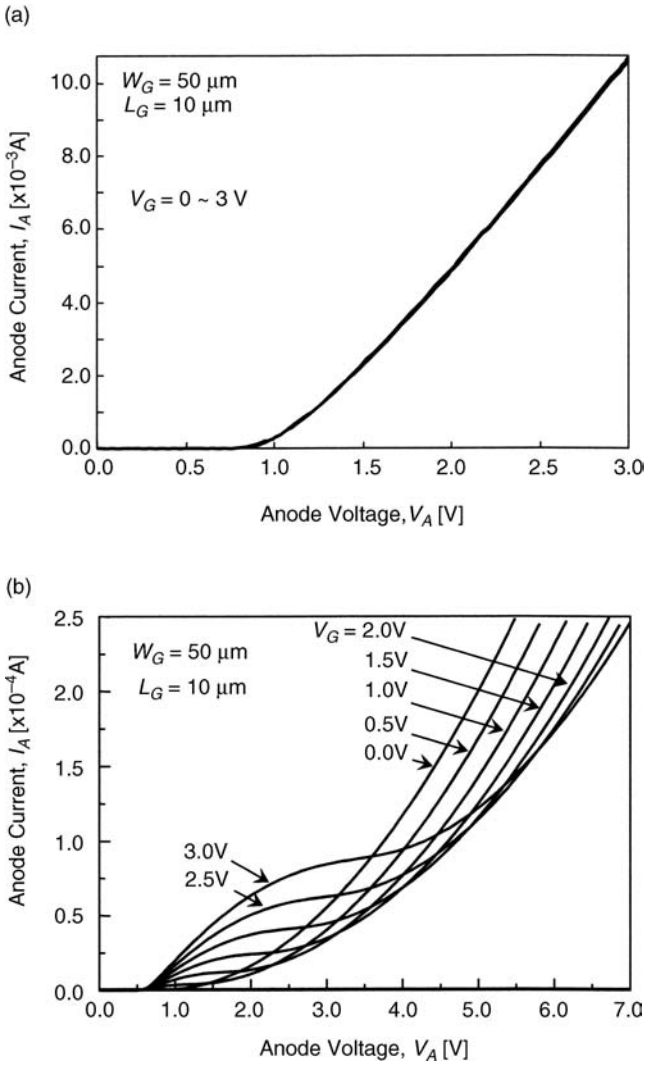

Figure 6.3 Simulated current versus voltage characteristics. (a) Default physical parameters are assumed. (b) Modified physical parameters are assumed. Reproduced by permission of The Electrochemical Society from S. Wakita and Y. Omura, Device models of SOI insulated-gate p-n junction devices, *Journal of Electrochemical Society*, vol. 150, pp. G816–G820, 2003.

6.3.2 Equivalent Circuit Models

From the simulation results described above, it is clear that, for Device A, the SOI Lubistor has two operation modes, and that the modes can be selected by setting the gate and anode voltages. When the gate voltage is lower than the anode voltage ($V_G < V_A$), the non-saturation current characteristics of a pMOSFET appear. When the gate voltage is higher

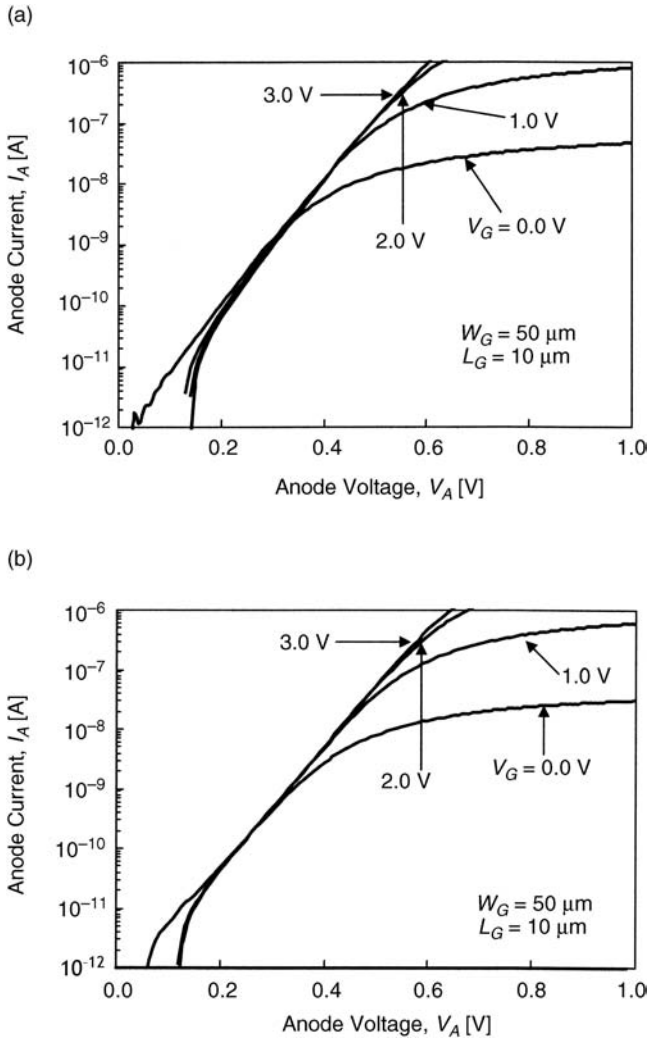

Figure 6.4 Current versus voltage characteristics in a low anode voltage condition. (a) Experimental results (Device A). (b) Simulation results. Modified physical parameters are assumed. Reproduced by permission of The Electrochemical Society from S. Wakita and Y. Omura, Device models of SOI insulated-gate p-n junction devices, *Journal of Electrochemical Society*, vol. 150, pp. G816–G820, 2003.

than the anode voltage ($V_G > V_A$), the saturation current characteristics of an nMOSFET appear. Fortunately, we have found that the characteristics described above can be reproduced by conventional device models. This allows us to propose the equivalent circuit model shown in Figure 6.6(a) for SPICE circuit simulations that use the standard circuit components of the SPICE simulator.

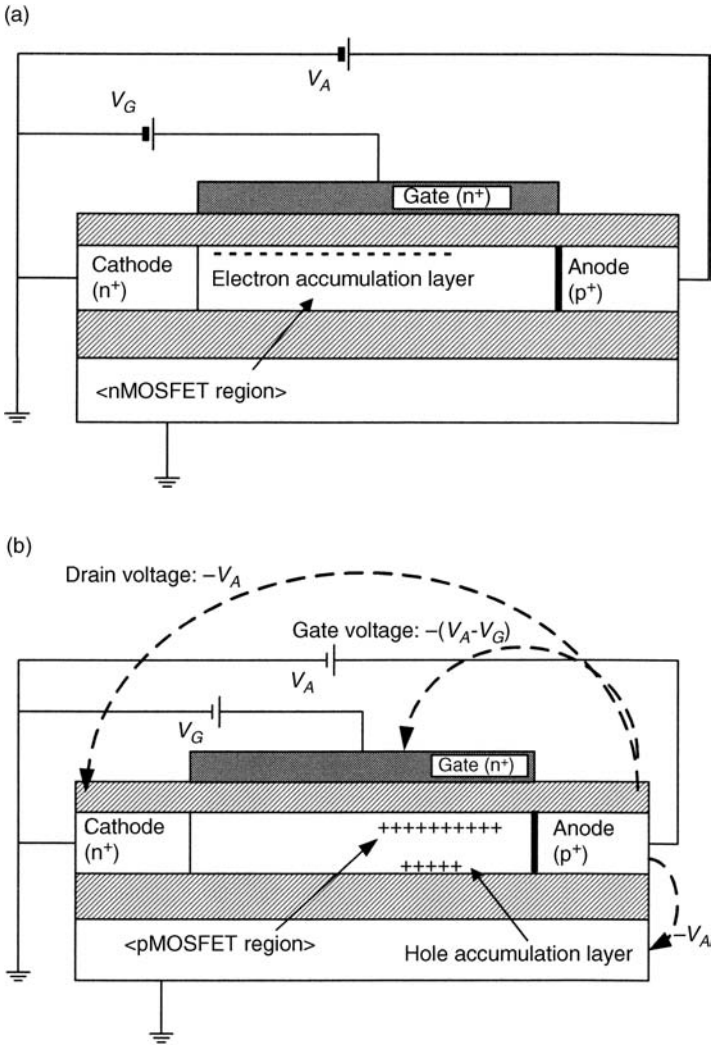

Figure 6.5 Classification of operation modes in an SOI Lubistor. (a) Saturation mode operation (nMOSFET-like operation), (b) Non-saturation mode operation (pMOSFET-like operation). Reproduced by permission of The Electrochemical Society from S. Wakita and Y. Omura, Device models of SOI insulated-gate p-n junction devices, *Journal of Electrochemical Society*, vol. 150, pp. G816–G820, 2003.

Two current components yielding the *I–V* characteristics of the SOI Lubistor are represented as the current flow component P1 and the current flow P2 in Figure 6.6(a). The gate electrode and the drain electrode of the pMOSFET are connected in common. For current path P1, diode D1 plays the role of low anode voltage operation (see Figure 6.4 or

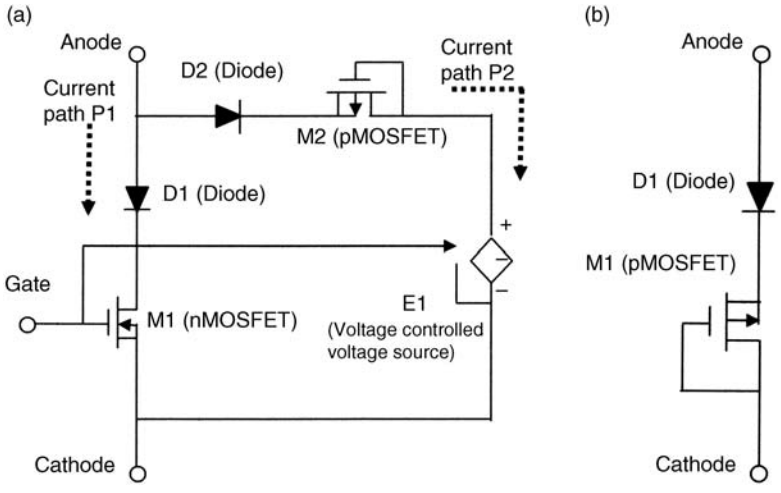

Figure 6.6 Proposed equivalent circuit model of the SOI Lubistor. (a) Modified physical parameters are assumed. (b) Default physical parameters are assumed. Reproduced by permission of The Electrochemical Society from S. Wakita and Y. Omura, Device models of SOI insulated-gate p-n junction devices, *Journal of Electrochemical Society*, vol. 150, pp. G816–G820, 2003.

Figure 6.7(b)). The nMOSFET exhibits current saturation in current path P1. For current path P1, the pMOSFET establishes triode-like operation at high anode voltages; diode D2 is connected to the pMOSFET to ensure compatibility with the model shown in Figure 6.6 (b). The voltage source, connected between the pMOSFET and the cathode terminal, generates voltage kV_G, which is proportional to the gate voltage, where k is the fitting parameter.

Another circuit model is shown in Figure 6.6(b). This is proposed for Device B, which has a high-quality SOI layer. Device B basically shows diode-like I–V characteristics (see Figure 6.2(b) or Figure 6.3(a)). It can simply be considered that the circuit model needs diode D1 only. However, since for long channel devices series resistance limits the diode current, we connect the pMOSFET M1 to diode D1 in series.

The simulated I–V characteristics of the equivalent circuit model are shown for Device A in Figure 6.7(a) together with those obtained by device simulations; Figure 6.7(a) shows the characteristics at high anode currents and Figure 6.7(b) for low anode currents. Good agreement is achieved between experimental and simulation results in Figure 6.7(a), while a notable difference of I_A behavior is seen at low gate voltages in Figure 6.7(b). However, the proposed circuit model covers most circuit simulations well. The present model could be slightly improved to simulate low-power applications. The proposed equivalent circuit model is virtually scalable in any of the device architecture characteristics because it is physics-based. The model also works well in a dynamic regime (not shown here); details are described in Chapter 16 of Part Four [25].

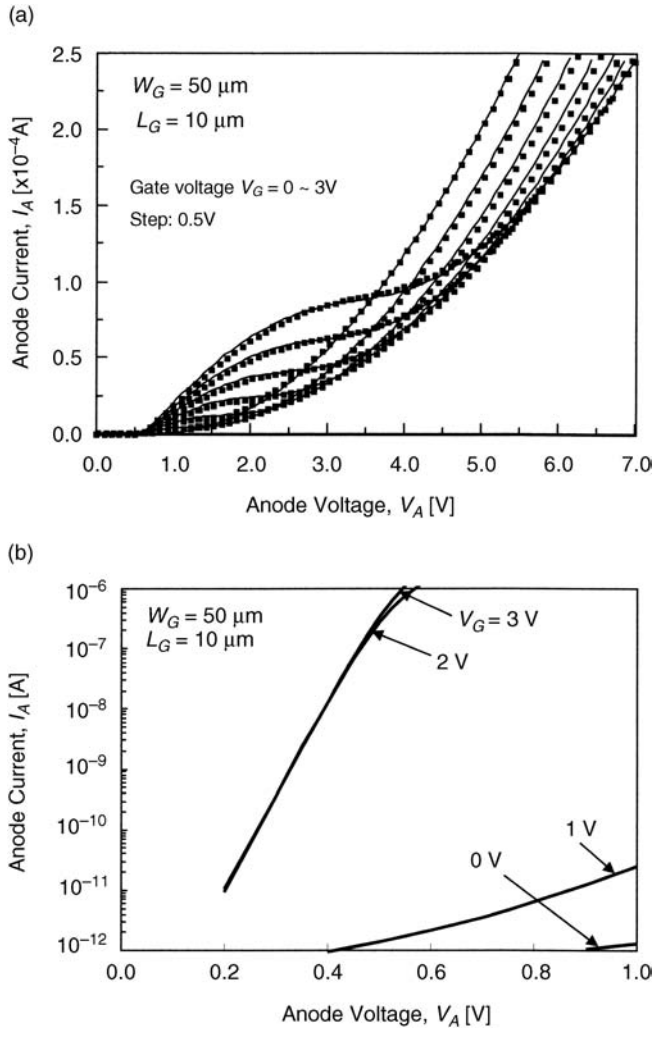

Figure 6.7 Current versus voltage characteristics obtained by the equivalent circuit model shown in Figure 6.6(a). Modified physical parameters are assumed. (a) *I–V* characteristics in the high anode current region. Solid lines are experimental results and dots are the simulation results of SPICE. (b) *I–V* characteristics in the low anode current region. Reproduced by permission of The Electrochemical Society from S. Wakita and Y. Omura, Device models of SOI insulated-gate p-n junction devices, *Journal of Electrochemical Society*, vol. 150, pp. G816–G820, 2003.

6.4 Summary

This chapter has described the direct current characteristics of various SOI Lubistors and has also proposed equivalent circuit models for circuit simulations. It has been clarified that device characteristics can be explained on the basis of complex operations performed within pn-junction, nMOSFET, and pMOSFET components. The circuit models proposed here on the basis of the DC operation model support the evaluation of various circuits such as electrostatic discharge (ESD) protection circuits.

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7

Noise Characteristics and Modeling of Lubistor

7.1 Introduction

Recent progress in device integration technology has been significant and the gate length of an individual MOSFET is already below 0.1 μm at the research level [1–3]. Given this background, the SOI MOSFET structure has attracted considerable attention for breaking down the technological barriers to device miniaturization. This structure has several advantages, such as its suppression of the short-channel effect, low voltage and high-speed operation, and lower production costs [4,5]. Furthermore, the SOI structure is being exploited to build new application paradigms [6–8], such as optical waveguides [9] and light emission diodes [10]. Such developments are essential because broadband communication technology and high-frequency analog technology are urgently needed.

Throughout the history of semiconductor devices, one fundamental subject has been to clarify the basic characteristics of SOI devices [11]. However, few studies have examined the behavior of thin-film SOI pn-junction devices [12–15], and noise characteristics have hardly been studied at all. Since the SOI structure is expected to support digital applications [16], as well as analog applications [17], basic operation mechanisms must be elucidated.

This chapter considers the noise characteristics of SOI Lubistors experimentally and theoretically using a model of DC characteristics. A theoretical model of noise characteristics is proposed to elucidate the noise characteristics unique to such devices.

7.2 Experiments

7.2.1 Device Structure

A schematic cross-section of an SOI Lubistor is shown in Figure 7.1(a). Although the basic device structure is analogous to that of SOI MOSFETs, the device differs in having a lateral p^+–n–n^+ junction structure. There are three main regions: anode, channel, and cathode. Measurements were carried out on devices having three different offset lengths at the anode

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

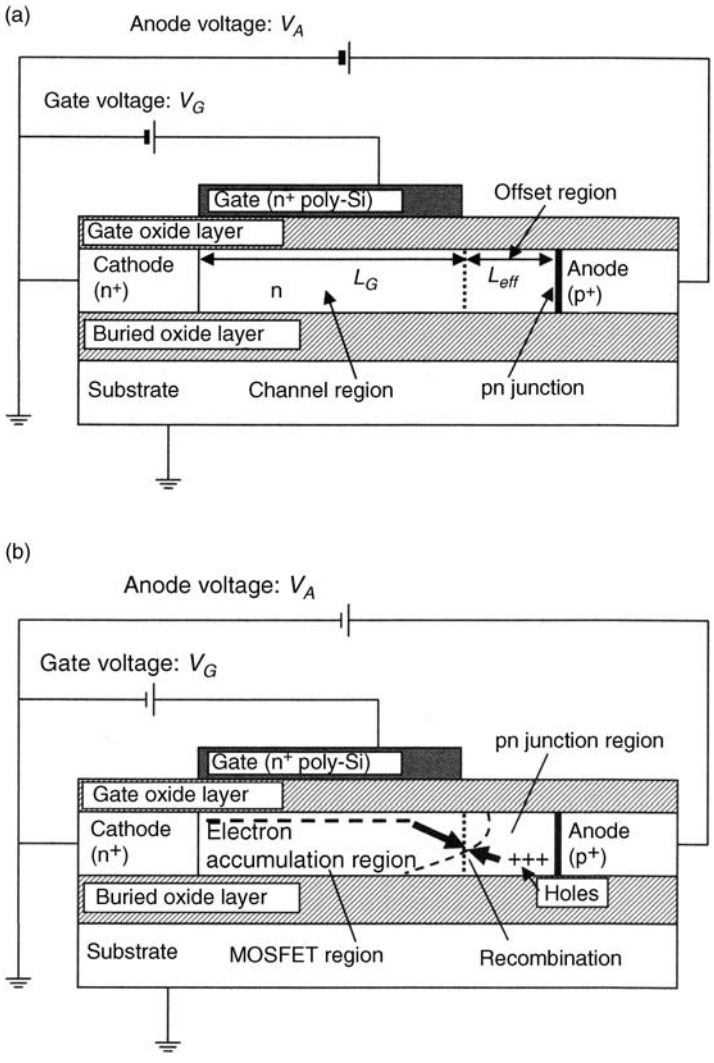

Figure 7.1 Schematic cross-section of an SOI Lubistor and physical model. (a) Device structure and bias condition. (b) Physical model for the DC characteristics. Reprinted with permission from S. Wakita and Y. Omura, *Journal of Applied Physics*, vol. 91, p. 2143, 2002. Copyright 2002, American Institute of Physics.

side. The devices used in this study were fabricated on SOI wafers using implanted oxygen (SIMOX) technology [18]. The SOI layer thickness (t_s) was 80 nm, the gate oxide layer thickness (t_{ox}) 80 nm, and the buried oxide layer thickness (t_{BOX}) 380 nm. The gate width (W_G) was 50 μm and the gate length (L_G) was 10 μm. The three offset lengths, L_{off}, examined were 5 μm, 10 μm, and 15 μm. The device parameters of the devices are listed in Table 7.1.

Table 7.1 Device parameters for the investigated device. Reprinted with permission from S. Wakita and Y. Omura, *Journal of Applied Physics*, vol. 91, p. 2143, 2002. Copyright 2002, American Institute of Physics

Parameters	Values [unit]
Gate length (L_G)	10 [μm]
Offset length (L_{off})	5, 10, 15 [μm]
Channel width (W_G)	50 [μm]
SOI silicon layer thickness (t_s)	80 [nm]
Gate oxide layer thickness (t_{ox})	80 [nm]
Buried oxide layer thickness (t_{BOX})	380 [nm]
SOI doping concentration	1×10^{15} [cm^{-3}]
Substrate doping concentration	1×10^{15} [cm^{-3}]
Gate doping concentration	1×10^{20} [cm^{-3}]
Anode doping concentration	1×10^{20} [cm^{-3}]
Cathode doping concentration	1×10^{20} [cm^{-3}]

7.2.2 Measurement System

The DC characteristics and the noise characteristics of the SOI Lubistors with the anode offset region were measured on the cathode common configuration, as shown in Figure 7.1(a). The DC characteristics were measured using an HP4156B precision semiconductor parameter analyzer; bias parameters ranged from 0 V to 7 V for both anode and gate voltages. Low-frequency noise measurements (3 Hz to 30 kHz) were performed using a digital storage oscilloscope (DSO). The noise signal, which occurred between the anode and cathode of the device, was amplified by a low-noise amplifier and transferred to the DSO. The measured noise voltage was converted into anode noise current spectral density $S_I(f)$ by anode conductance, which was obtained from DC measurements. The entire noise measurement system was implemented in a metal-shielded box. A battery was used as the power supply for the device and the amplifier operation, and the noise originating from the noise measurement system was subtracted from the measured values.

7.3 Results and Discussion

7.3.1 I–V Characteristics of an SOI Lubistor and a Simple Analytical Model

The measured DC current–voltage characteristics of the SOI Lubistors are shown in Figure 7.2. Figures 7.2(a) and 7.2(b) are for devices with L_{off} of 5 μm and 15 μm, respectively. It is readily anticipated that the device would basically show normally-on operation. In the devices, however, the current virtually does not flow when positive bias is not applied to the gate electrode because the channel region is depleted by negative charges inside the buried oxide layer (this was confirmed by an n-type buried-channel MOSFET on the same chip that is not shown here). When a positive bias is applied to the gate electrode, an accumulation layer of electrons appears near the top surface of the channel region. When a positive anode-to-cathode voltage is applied to the device, the pn junction is forward-biased. The DC current characteristics reflect the aforementioned device structure; the anode current is observed when anode-to-cathode voltages exceed the built-in voltage of the pn junction, and current saturation similar to MOSFET is observed at high anode-to-

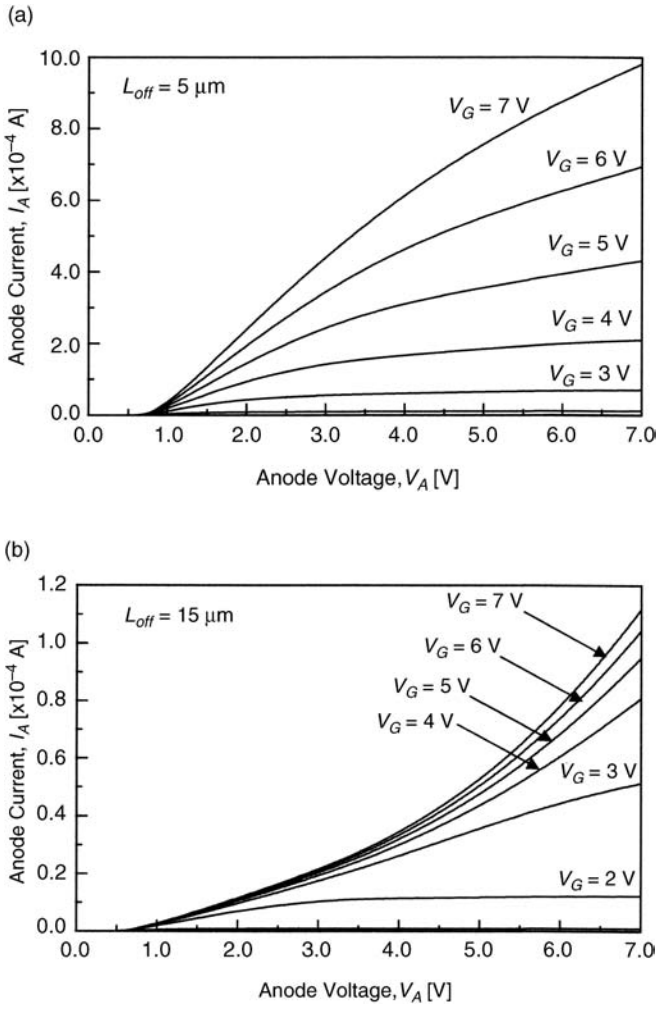

Figure 7.2 Current versus voltage characteristics of the SOI Lubistor with a 5 μm gate. (a) $L_{off} = 5$ μm. (b) $L_{off} = 15$ μm. Reprinted with permission from S. Wakita and Y. Omura, *Journal of Applied Physics*, vol. 91, p. 2143, 2002. Copyright 2002, American Institute of Physics.

cathode voltages. Therefore, the SOI Lubistor is considered as a series connection of p^+n junction diode and MOSFET, and a simplified model of the DC characteristics can be proposed (see Figure 6.6 in Chapter 6). The model is shown in Figure 7.1(b). The channel region is divided into two regions. The region of the anode side behaves as a pn-junction device (labeled *pn-junction region* in Figure 7.1(b)), and the region of the cathode side behaves as an MOSFET (labeled *MOSFET region* in Figure 7.1(b)). It is expected that the hole diffusion current is dominant in the *pn-junction region* and that the electron current is dominant in the *MOSFET region*.

The boundary of the two regions is estimated by the hole diffusion length (L_p). In SOI Lubistors without an offset region, the hole diffusion length (L_p) should vary with both anode

and gate biases. However, the devices used here have an offset region in the channel, so the anode current tends to saturate at high anode-to-cathode voltages, as shown in Figure 7.2(a). Accordingly, we consider that the offset length is longer than the hole diffusion length ($L_{off} > L_p$), or $L_{off} \sim L_p$, and that the holes injected into the channel almost recombine with electrons inside the offset region. Though the boundary between the *pn-junction region* and the *MOSFET region* should move slightly in the offset region, it is assumed that the length of the MOSFET region is almost the same as the gate length (L_G).

When modeling the DC characteristics of the device, the widely accepted mathematical expression for characteristics is used to describe the characteristics of the above two regions. The *MOSFET region* intrinsically behaves like a buried channel MOSFET. Since the surface accumulation layer rules the channel current at high gate voltages, the mathematical expression of channel current should be close to that of the inversion channel MOSFET. For the sake of simplicity, I use the following expression of channel current (I_A) in the *MOSFET region* [19]:

$$I_A = \alpha \left(V_{GT} - \frac{1}{2} V_D^* \right) V_D^*, \tag{7.1}$$

where $\alpha = (W_G/L_G)\mu_n C_{ox}$, $V_{GT} = V_G\text{-}V_{TH}$, μ_n is the electron effective mobility, C_{ox} is the gate capacitance per unit area, V_G is the gate voltage, V_{TH} is the threshold voltage of the MOSFET region, and V_D^* is the virtual drain voltage that can be considered to be applied in the *MOSFET region*.

Next, I assume that the pn junction operates under low-level injection. The current characteristics are represented by the following Shockley equation [20]:

$$I_A = I_0 \left[\exp\left(\beta V_{pn}^* \right) - 1 \right], \tag{7.2}$$

$$I_0 = qA \frac{p_0 D_p}{L_p}, \tag{7.3}$$

where $\beta = q/(nk_BT)$, $V_{pn}^* = V_A - V_D^*$ is the bias across the pn junction, I_0 is the saturation current, q is the elemental charge, n is the ideality factor of the pn junction ($\sim$1.7), k_B is Boltzmann's constant, T is absolute temperature, p_0 is the hole concentration of the channel region in equilibrium, and D_p is the hole diffusion constant. Since hole diffusion and recombination processes are dominant in the n-type channel region, I_0 is represented by the hole current term.

Virtual drain voltage (V_D^*) and saturation current (I_0) are derived from the above expression for the channel current. From Equation (7.1), V_D^* is given by

$$V_D^* = V_{GT} - \sqrt{V_{GT}^2 - \frac{2}{\alpha} I_A} \tag{7.4}$$

and, from Equation (7.2), I_0 is given by

$$I_0 = I_A \left[\exp\left(\beta V_{pn}^* \right) - 1 \right]^{-1}. \tag{7.5}$$

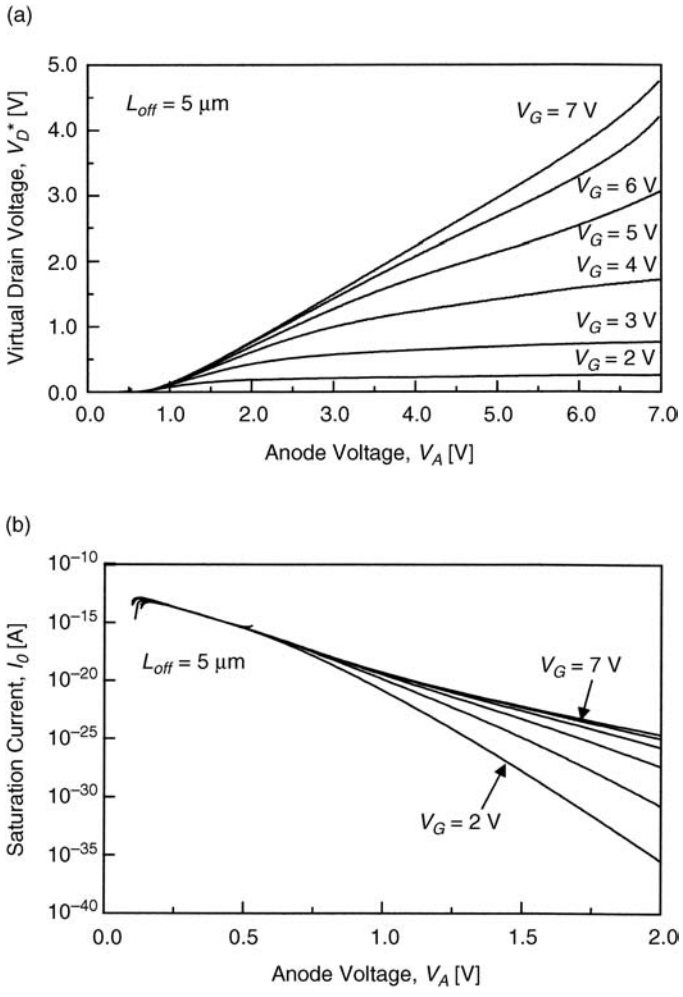

Figure 7.3 $V_D{}^* - VA$ and $I_0 - V_A$ characteristics of the SOI Lubistor ($L_{off} = 5\,\mu m$) extracted from $I_A - V_A$ characteristics by using Equations (7.4) and (7.5), respectively. (a) $V_D{}^*$ versus V_A characteristics. (b) I_0 versus V_A characteristics. Reprinted with permission from S. Wakita and Y. Omura, *Journal of Applied Physics*, vol. 91, p. 2143, 2002. Copyright 2002, American Institute of Physics.

Practical values of V_D^* and I_0 are extracted by applying Equations (7.4) and (7.5) to the DC characteristics shown in Figure 7.3. V_D^* and I_0 dependencies on V_A are shown in Figures 7.3(a) and 7.3(b), respectively. It can be seen in Figure 7.3(a) that V_D^* monotonously increases with both anode and gate biases and that V_A dependence on V_D^* is similar to that of the anode current; in other words, the largest part of V_A is applied to the pn-junction region. It can be seen in Figure 7.3(b) that I_0 monotonously decreases as V_A increases, which can be explained as follows. Though hole injection from the p^+ anode to the channel is enhanced as V_A increases, the hole diffusion is forcibly collapsed at the edge of the MOSFET region. In other words, the hole lifetime decreases as V_A increases; it is also anticipated that the hole diffusion constant decreases as V_A increases.

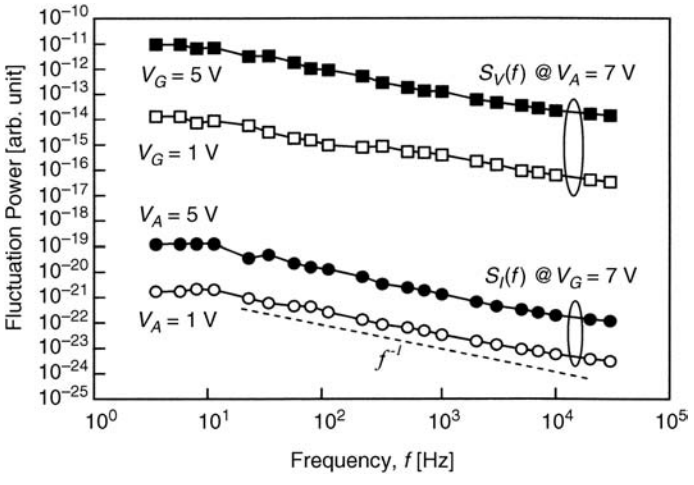

Figure 7.4 Frequency dependencies of noise spectral densities $S_I(f)$ and $S_V(f)$, measured using the device with L_{off} of 5 μm. Reprinted with permission from S. Wakita and Y. Omura, *Journal of Applied Physics*, vol. 91, p. 2143, 2002. Copyright 2002, American Institute of Physics.

7.3.2 Noise Spectral Density of SOI Lubistors and Their Feature

At the beginning of this section, we show the measured noise characteristics of the SOI Lubistors and examine the past model for the pn-junction noise characteristics [21–31]. Since the noise characteristics of the three devices are similar, the noise characteristics of the device with L_G of 10 μm and L_{off} of 5 μm are shown in Figure 7.4 as an example; the fluctuation power observed in DSO is shown as a function of the frequency, f. Solid lines with symbols in the figure show experimental results. The noise power shows a $1/f^{\gamma}$-type frequency dependence in the measured frequency range ($\gamma \sim 1$). Since the noise spectral density includes the background thermal noise, γ is slightly smaller than unity. Accordingly, experimental results at $f = 5$ Hz, which are not influenced by the thermal noise, are shown in the following figures. Anode current noise spectral density $S_I(f)$ dependence on anode current I_A is shown in Figure 7.5 for the device with L_{off} of 5 μm. Here the anode current I_A is controlled by V_A at V_g of 6 V. Since the anode current increases monotonously with V_A in this bias condition, the AC short-circuit model must be assumed in the noise analysis. This is the reason for plotting parameter $S_I(f)$ in Figure 7.5. On the other hand, the $S_V(f)$ dependence on anode current I_A is shown in Figure 7.5 for the same device. Here the anode current is controlled by V_G at V_A of 7 V. Though the anode current increases monotonously with V_G, it is almost independent of V_A for the present bias condition because of current saturation. Thus the AC open-circuit model must be assumed in the noise analysis. This is the reason for plotting parameter $S_V(f)$ in Figure 7.5. $S_I(f)$ is proportional to I_A^2 and $S_v(f)$ is proportional to $I_A{}^{1.5}$, as shown in Figure 7.5.

Kleinpenning proposed a theoretical expression for the current noise characteristics ($S_I(f)$) of the pn junction that is founded in Hooge's empirical mobility-fluctuation-induced $1/f$ noise model [23,32]. We investigate whether applying his theory to a noise analysis of the SOI Lubistors allows the present experimental results to be explained. According to the Hooge

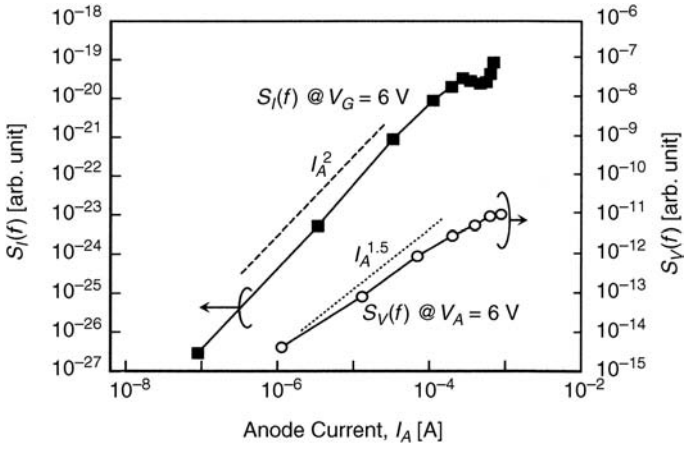

Figure 7.5 Anode current dependencies of $S_I(f)$ and $S_V(f)$, measured at $f = 5$ Hz using the device with L_{off} of 5 μm. Reprinted with permission from S. Wakita and Y. Omura, *Journal of Applied Physics*, vol. 91, p. 2143, 2002. Copyright 2002, American Institute of Physics.

model, the $1/f$ noise spectral density due to the mobility fluctuation in a homogeneous system is given by [32]

$$\frac{S_I(f)}{I_A^2} = \frac{\alpha}{Nf}, \tag{7.6}$$

where α is the Hooge parameter and N is the total number of free carriers in the sample.

When the $1/f$ noise due to the mobility fluctuation is considered in long p^+n diodes, the mobility fluctuation results in diffusivity fluctuation that yields the current fluctuation [23]. According to the Kleinpenning model, the anode current fluctuation $\delta I(x,t)$ caused by mobility fluctuation $\delta\mu_p(x,t)$ at point x in the quasi-neutral hole diffusion region at time t is

$$\delta I_A(x,t) = \frac{1}{2}\left\langle \frac{I_A(x)}{\mu_p} \right\rangle \delta\mu_p(x,t). \tag{7.7}$$

The anode current noise spectral density $S_I(f)$ is calculated by integrating Equation (7.7) over the whole device length L:

$$\begin{aligned} S_I(f) &= \frac{1}{(2\mu_p L)^2} \int \int_0^{L_p} I_A(x) I_A(x') S_{\mu_p}(x,x',f)\, dx\, dx' \\ &= \frac{\alpha}{4AfL^2} \int_0^{L_p} \frac{I_A^2(x)}{p(x)} dx, \end{aligned} \tag{7.8a}$$

$$p(x) = p_0[e^{qV/kT} - 1]e^{-x/L_p} + p_0, \tag{7.8b}$$

where A is the cross-section of the diode, $S_{\mu p}(x,x',t)$ is the cross-correlative spectral density on the mobility fluctuation at points x and x', $p(x)$ is the hole density at point x, V is the local potential at point x, and p_0 is the hole density at $V=0$. Integrating Equation (7.8a) yields the following expression:

$$S_I(f) = \frac{\alpha q I_0}{4f\tau}[\exp(\beta V_A) - \beta V_A], \tag{7.9}$$

where τ is the minority carrier lifetime. Since Equation (7.9) indicates that $S_I(f)$ is in some way a linear function of I_A, it cannot explain the experimental results shown in Figure 7.5. Though Kleinpenning derived theoretical expressions of $S_I(f)$, such as Equation (7.9), for a long or short pn-junction diode [23], he got the relation of $S_I(f) \sim I_A$ in each case. His theory was based on the low-level injection. This indicates that the Kleinpenning model based on the low-level injection fails to analyze the present experimental results. We can see that $V_{pn}^* > 1$ V in Figure 7.3(a) and that $S_I(f) \sim I_A^2$ in Figure 7.5. This means that we have to reconsider the Kleinpenning model because the high-level injection should be assumed in the device.

In the previous section, we considered that $L_p > L_{off}$ or $L_p \sim L_{off}$ for the device with L_{off} of 5 μm. The anode current of the device with L_{off} of 5 μm does not saturate completely, as shown in Figure 7.2(a). Therefore, we can assume for simplicity that the hole concentration, $p(x)$, across the offset region is almost constant, which is practically equivalent to the assumption of high-level injection. Consequently, the anode current, $I_A(x)$, should be approximately constant. When it is assumed that $p(x) = p_{offset}$ (constant) and $I_A(x) = I_A(V_A)$ in the offset region, we have the following approximate expression for $S_I(f)$ from Equation (7.8a):

$$S_I(f) = \frac{\alpha q I_A(V_A)^2}{4AfL_{off}p_{offset}}. \tag{7.10}$$

Equation (7.10) seems to be able to explain qualitatively the experimental results of $S_I(f)$ shown in Figure 7.5. However, the Kleinpenning model including Equation (7.10) does not consider the current saturation mode; Equation (7.10) does not yield an appropriate and comprehensive explanation for the experimental results shown in Figure 7.5. In addition, the model does not give us any suggestion for $S_I(f)$ dependence on L_{off}, as discussed later, because the exponent of I_A in $S_I(f)$ goes beyond two as L_{off} increases.

Since the current saturation mode has never been considered in past theories, there is no theory for $S_v(f)$. This means that we have to consider an advanced model for $S_I(f)$ and $S_v(f)$ to explain the above-described noise characteristics comprehensively.

7.3.3 Advanced Analysis of Anode Noise Spectral Density

Since the noise characteristics of SOI Lubistors cannot be explained by any past model, we introduce a phenomenalistic technique in order to analyze the noise characteristics. As mentioned above, the device is modeled as a series connection of the pn-junction region and the MOSFET region. I assume that the pn junction modulates the noise generated in the MOSFET region because $S_I(f)$ and $S_v(f)$ show a strong dependence on I_A. The anode current

fluctuation δI_A induced by the anode voltage fluctuation δV_A and the gate voltage fluctuation δV_G is given by

$$\delta I_A = \frac{\partial I_A}{\partial V_A}\delta V_A + \frac{\partial I_A}{\partial V_G}\delta V_G. \tag{7.11}$$

Here I classify two kinds of noise analyses. The first analysis derives the theoretical expression for $S_I(f)$ and the second derives one for $S_v(f)$. As the first step, I discuss the expression for $S_I(f)$. When using the short-circuit model to consider $S_I(f)$, it must be assumed that $\delta V_A = 0$. The mean square value of anode current fluctuation is given by

$$\left\langle \delta I_A^2 \right\rangle = \left(\frac{\partial I_A}{\partial V_G}\right)^2 \left\langle \delta V_G^2 \right\rangle, \tag{7.12}$$

where $\langle \delta X^2 \rangle$ is the time average of the self-correlation on δX. Given the continuity condition, the current in the pn-junction region should coincide with that in the MOSFET region. I now consider the operation region in which the pn junction determines the current mechanisms. I use the current equation of the pn junction to describe the channel current throughout the device. Accordingly, the anode current noise spectral density $S_I(f)$ is given by

$$S_I(f) = \left(\frac{\partial I_A}{\partial V_G}\right)^2 S_{VG}(f), \tag{7.13}$$

where $S_{VG}(f)$ corresponds to the spectral density of equivalent input noise. As the second step, I tackle the expression for $S_V(f)$. When the open-circuit model is used to consider $S_V(f)$, it must be assumed that $\delta I_A = 0$. The mean square value of anode voltage fluctuation is given by

$$S_V(f) = \left\{ \frac{\partial I_A}{\partial V_G} \Big/ \frac{\partial I_A}{\partial V_A} \right\}^2 S_{VG}(f). \tag{7.14}$$

The simulated dependencies of $S_I(f)$ and $S_V(f)$ on I_A are shown in Figure 7.6. In Figure 7.6, $S_I(f)$ and $S_V(f)$ are calculated by Equations (7.13) and (7.14), assuming that $S_{VG}(f) = C/f$, where $C = \alpha_{pn0} V_G{}^m / I_A$ $(m > 0)$ on the basis of the Hooge model [32] and a comparison with Figure 7.5. Here, α_{pn0} is the fitting parameter. In practice, the case of $m = 12$ reproduces the best curve. The proposed expression for $S_{VG}(f)$ does not immediately appear to be compatible to the conventional Hooge model because $m > 2$. However, the model can be compatible to the Hooge model if we assume that the Hooge parameter (α_{pn}) depends on V_G; namely, $\alpha_{pn} = \alpha_{pn0} V_G{}^{10}$. Therefore, it is assumed here that $S_{VG}(f) = \alpha_{pn0} V_G{}^{12}/fI$ and $\alpha_{pn0} = 1 \times 10^{-24}$ $(\mathrm{A/V}^{10})$. It can be seen that the proposed model can successfully reproduce the experimental results of noise spectral density.

When the offset length (L_{off}) increases, it can be seen that the exponent (η) of I_A in $S_I(f)$ and $S_V(f)$ also increases, as shown in Figure 7.7. This suggests that the minority carrier density in the offset region depends on L_{off}. When L_{off} is smaller than the hole diffusion length (L_p), holes are forced to recombine with electrons at the gate edge; the device with L_{off} of 5 μm equals this case. In this case, the increase in the hole concentration in the offset region is suppressed; the anode current is controlled by the concentration of electrons supplied from the MOSEFT region. When L_{off} is larger than L_p, on the other hand, the hole concentration continuously increases with V_A and approaches the level of the anode hole concentration. The devices with L_{off} of 10 μm and

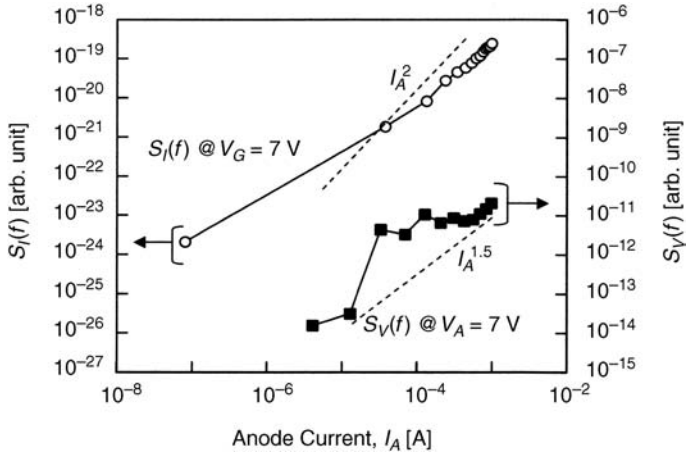

Figure 7.6 Calculated anode current dependencies of $S_I(f)$ and $S_V(f)$. It is assumed that $S_{VG}(f) = \alpha_{pn0} V_G{}^{12}/fI_A$. Reprinted with permission from S. Wakita and Y. Omura, *Journal of Applied Physics*, vol. 91, p. 2143, 2002. Copyright 2002, American Institute of Physics.

15 μm equal this case. Since most holes recombine with electrons inside the offset region in this case, the anode current does not easily saturate, even at high values of V_A, just like an ideal pn-junction diode. In such cases, however, the model for $S_{VG}(f)$ should be reconsidered. Here a simple empirical model is proposed for the exponent η of I_A in $S_I(f)$ and $S_V(f)$:

$$\eta = s + \left(\frac{L_{off}}{15}\right)^2, \tag{7.15}$$

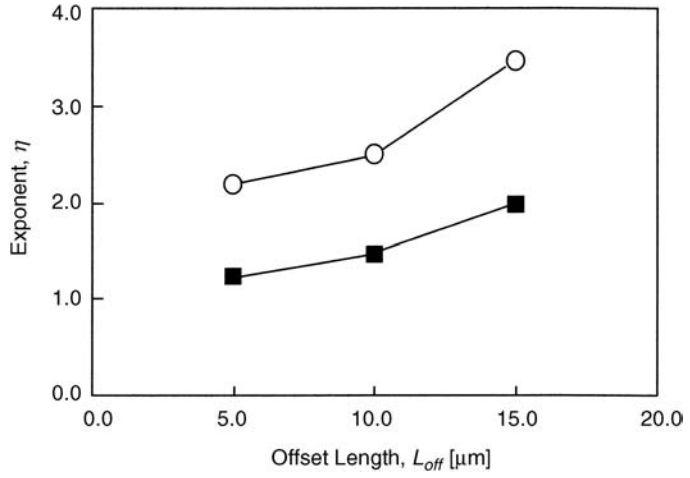

Figure 7.7 Exponent η as a function of offset length L_{off}. Open circles are experimental results for $S_I(f)$ and closed squares for $S_V(f)$. Reprinted with permission from S. Wakita and Y. Omura, *Journal of Applied Physics*, vol. 91, p. 2143, 2002. Copyright 2002, American Institute of Physics.

where s is equal to 1.5 for $S_V(f)$ and 2.0 for $S_I(f)$. L_{off} is in units of μm. Using Equation (7.15), we have the following expression for $S_V(f)$:

$$S_V(f) = \alpha_{pn0} V_G^{12+4(L_{off}/15)^2} / f I_A, \tag{7.16}$$

where it is assumed that $\alpha_{pn} = \alpha_{pn0} {V_G}^{10}$. The exponent of V_G in Equation (7.16) is determined by the fact that the anode current I is approximately proportional to ${V_G}^4$. It is assumed that $S_{VG}(f)$ is independent of L_{off} and that

$$\left\{ \frac{\partial I_A}{\partial V_G} \Big/ \frac{\partial I_A}{\partial V_A} \right\}^2 \propto V_G^{4(L_{off}/15)^2}$$

in Equation (7.14). A similar equation for calculating $S_I(f)$ is obtained as

$$S_I(f) = \alpha_{pn0} V_G^{12} {I_A}^{2+(L_{off}/15)^2} / f, \tag{7.17}$$

where it is assumed that

$$\left(\frac{\partial I_A}{\partial V_G} \right)^2 \propto {I_A}^{3+(L_{off}/15)^2}$$

in Equation (7.13). These expressions can be applicable to estimation of the noise spectral density of devices.

7.4 Summary

In this chapter, I described the noise characteristics of various SOI Lubistors with anode-offset regions. The static characteristics of the devices were modeled for a noise analysis; the new model is a series of a MOSFET and a pn junction. It has been shown experimentally that the noise power of such devices is proportional to ${I_A}^n$ $(n > 0)$, where I_A is the anode current. Since the noise characteristics are not explained by conventional theory, a new model was proposed from the results of a phenomenological consideration. It has been shown that the proposed basic model can explain the experimental results. The influence of anode-offset length was also discussed and an empirical model was proposed.

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8

Supplementary Study on Buried Oxide Characterization

A Macroscopic Physical Model and Capacitance Response of the Buried Oxide Having a Transition Layer in a SIMOX Substrate

8.1 Introduction

The silicon-on-insulator (SOI) structure has been attracting attention because it improves the switching speed and packing density of devices. SIMOX technology is one of the most promising SOI technologies [1] and the authors have reported SIMOX LSI performances that show its prospects for VLSI [2,3]. In conventional SIMOX substrates, there exists a transition layer composed of Si, SiO_2 and SiO_x between the superficial silicon layer and the buried oxide layer. The physical structure of the transition layer is very complicated. The transition layer acts as both the semiconductor and the insulator because, just as in the case of a semi-insulating polysilicon (SIPOS) film [4], it includes many oxygen atoms compared to the usual semiconductor silicon. Therefore, it is difficult to analyze the capacitance response by the introduction of a microscopic model.

In this chapter, a macroscopic physical model that reflects the microscopic feature of the transition layer is proposed to evaluate the capacitive nature. Two-dimensional numerical analysis is carried out to investigate the capacitance property of the buried oxide with the transition layer.

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

8.2 Physical Model for the Transition Layer

Many kinds of processing techniques for fabricating SIMOX substrates have been reported so far. According to one recent paper, it is possible to eliminate the transition layer adjacent to the buried oxide by high-temperature annealing at over 1200 °C [5]. In the present study, we focus on SIMOX substrates having the buried oxide with a transition layer. The transition layer is apt to remain at the interface between the superficial silicon layer and the buried oxide in the case of the annealing temperature below 1200 °C; according to the analysis by Auger electron spectroscopy (AES), an SiO_2 cluster distribution can be approximately expressed as a Gaussian profile [1,6].

It is assumed that there are many SiO_2 clusters at the Si/SiO_2 interface, as shown in Figure 8.1; the cluster fraction is equal to 100% at the buried oxide and to 0% at the superficial silicon layer or substrate silicon. The SiO_2 cluster density function $N(x)$ in the transition layer can be expressed as

$$N(x) = N_m \exp\left(-\frac{x^2}{\Delta^2}\right), \tag{8.1a}$$

$$N_m = \frac{3}{4\pi r^3}, \tag{8.1b}$$

where the buried oxide/transition layer interface locates at $x = 0$, r is the radius of the cluster, and Δ is the decay distance of the SiO_2 cluster distribution.

Here we will suppose that the transition layer is a continuous medium consisting of Si clusters and SiO_2 clusters. In this case, the Clausius–Mossotti relationship can be applied to

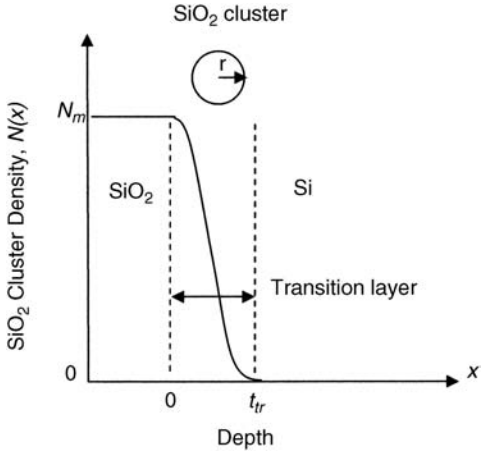

Figure 8.1 SiO_2 cluster profile model. © 1992 IEEE. Reprinted, with permission, from Y. Omura and K. Izumi, A macroscopic physical model and capacitive response of the buried oxide having a transition layer in a SIMOX substrate, *IEEE Transactions on Electron Devices*, vol. 39, pp. 1916–1921, 1992.

the transition layer as a dielectric material [7]. In case of two kinds of dielectric materials, the relationship is expressed as [8]

$$\frac{\varepsilon_{tr}(x)-1}{\varepsilon_{tr}(x)+2}=\frac{\alpha_0 N(x)}{3}+\frac{\alpha_S[N_m-N(x)]}{3}, \tag{8.2}$$

[Total] [SiO_2] [Si]

where ε_{tr} is the relative dielectric constant of the transition layer, α_0 is the susceptibility of SiO_2, α_S is the susceptibility of Si, and $N(x)$ is the cluster density function of the transition layer. The relative dielectric constant of the transition layer is derived from Equation (8.2) as

$$\varepsilon_{tr}(x)=\frac{1+\frac{2}{3}\{\alpha_0 N(x)+\alpha_S[N_m-N(x)]\}}{1-\frac{1}{3}\{\alpha_0 N(x)+\alpha_S[N_m-N(x)]\}}. \tag{8.3}$$

Boundary conditions at both the top and the bottom of the transition layer yield the following equations:

$$\alpha_0 N_m=3\frac{\varepsilon_{ox}-1}{\varepsilon_{ox}+2}, \tag{8.4}$$

$$\alpha_S N_m=3\frac{\varepsilon_S-1}{\varepsilon_S+2}. \tag{8.5}$$

It is considered that the transition layer behaves like a semiconductor under a quasi-static potential so it may be possible to estimate the bandgap energy of the transition layer. According to the conventional data for optics, there exists the following empirical relationship between the energy gap E_g and the refractive index n, which is known as the Moss law [9]:

$$E_g n^4=77. \tag{8.6}$$

The relative dielectric constant is approximately related to n^2. These equations are applied to the transition layer. Then, the energy gap of the transition layer $E_{gtr}(x)$ is expressed as

$$E_{gtr}(x)=\frac{154}{[\varepsilon_{tr}(x)]^2}. \tag{8.7}$$

Here we employed a new constant '154' rather than '77' in Equation (8.6) to get the quantitative coincidence with experimental data. The calculated results shown in Figure 8.2 indicate the usefulness of Equation (8.7). Thus we can draw a bandgap scheme as shown in Figure 8.3.

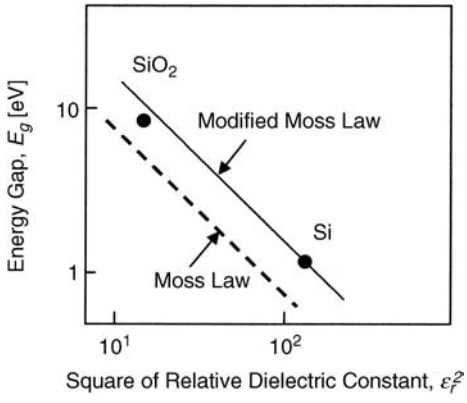

Figure 8.2 Relationship between energy gap and dielectric constant. © 1992 IEEE. Reprinted, with permission, from Y. Omura and K. Izumi, A macroscopic physical model and capacitive response of the buried oxide having a transition layer in a SIMOX substrate, *IEEE Transactions on Electron Devices*, vol. 39, pp. 1916–1921, 1992.

The energy gap information makes it possible to calculate the carrier concentrations. For an n-type transition layer, the electron concentration $n(x)$ is expressed as

$$n(x) = n_i(x)\exp\left[\frac{q\phi(x)}{kT}\right], \tag{8.8}$$

$$n_i(x) = 3.87 \times 10^{16} T^{3/2} \exp\left[-\frac{E_{gtr}(x)}{2kT}\right], \tag{8.9}$$

where $\phi(x)$ is the intrinsic potential in the transition layer and $n_i(x)$ is the intrinsic carrier concentration in the transition layer.

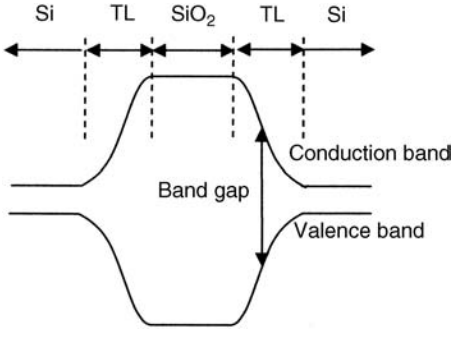

Figure 8.3 A bandgap scheme of the buried oxide with the transition layer. TL: transition layer. © 1992 IEEE. Reprinted, with permission, from Y. Omura and K. Izumi, A macroscopic physical model and capacitive response of the buried oxide having a transition layer in a SIMOX substrate, *IEEE Transactions on Electron Devices*, vol. 39, pp. 1916–1921, 1992.

Next, the transition layer thickness t_{tr} should be defined. Oxygen atom concentration is generally about $1 \times 10^{18}\,\mathrm{cm}^{-3}$ in the monocrystalline silicon substrate. Then it is assumed, for example, that the concentration of SiO_2 clusters is $5 \times 10^{17}\,\mathrm{cm}^{-3}$ at the silicon-side edge of the transition layer and that $N_m = 2 \times 10^{22}\,\mathrm{cm}^{-3}$. For the DC potential, the transition layer thickness is derived from Equation (8.1) as

$$t_{tr} = \sqrt{[5\ln(10) - \ln(2.5)]}\Delta(0), \tag{8.10}$$

where $\Delta(0)$ is the decay distance when the measurement frequency is equal to zero. On the other hand, the transition layer itself contains a lot of deep traps and the trapping and detrapping processes depend on the measurement frequency. Traps do not respond beyond a certain critical frequency f_o; the transition layer behaves like a semiconductor below f_o with the trap response and like an insulator beyond f_o without the trap response. Here, for simplicity, we do not directly make a trap model for the transition layer, but propose a model for the effective thickness of the transition layer influenced by the deep traps. Then the effective thickness of the transition layer $t_{eff}(f)$ depending on frequency can be expressed as

$$t_{eff}(f) = t_{tr}\left[1 - \exp\left(-\frac{f}{f_0}\right)\right], \tag{8.11}$$

where f is the measurement frequency. From this expression, the frequency-dependent decay distance $\Delta(f)$ is expressed as

$$\Delta(f) = \Delta(0)\left[1 - \exp\left(-\frac{f}{f_0}\right)\right]. \tag{8.12}$$

The cluster density function $N(x,f)$ can also be rewritten as

$$N(x,f) = N_m \exp\left[-\frac{x^2}{\Delta^2(f)}\right]. \tag{8.13}$$

Therefore, the relative dielectric constant of the transition layer is rewritten using Equations (8.12) and (8.13) as

$$\varepsilon_{tr}(x,f) = \frac{1 + \frac{2}{3}\{\alpha_0 N(x,f) + \alpha_S[N_m - N(x,f)]\}}{1 - \frac{1}{3}\{\alpha_0 N(x,f) + \alpha_S[N_m - N(x,f)]\}}. \tag{8.14}$$

8.3 Capacitance Simulation

8.3.1 A Structure to Evaluate Capacitance

In this study, the specific capacitance simulator was used to evaluate the parasitic capacitance of an actual device. The simulator can deal with the structure shown in Figure 8.4(a). The

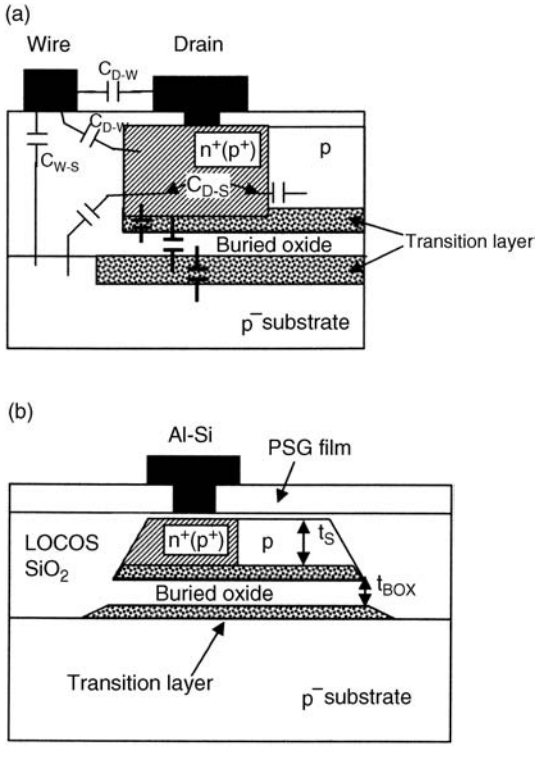

Figure 8.4 Device structure. LOCOS: local oxidation of silicon. (a) Simulated device structure. (b) Cross-sectional view of fabricated device. © 1992 IEEE. Reprinted, with permission, from Y. Omura and K. Izumi, A macroscopic physical model and capacitive response of the buried oxide having a transition layer in a SIMOX substrate, *IEEE Transactions on Electron Devices*, vol. 39, pp. 1916–1921, 1992.

drain-to-substrate capacitance, $C_{D\text{-}S}$, drain-to-wire capacitance, $C_{D\text{-}W}$, and wire-to-substrate capacitance, $C_{W\text{-}S}$, were mainly calculated using this structure. The physical model of the transition layer was incorporated into the evaluation.

8.3.2 Numerical Simulation Technique

The simulator only solves Poisson's equation based on the equilibrium condition of carriers as follows:

[Si layer including the transition layer]

$$\varepsilon_0 \varepsilon_S(x,y)\nabla^2\phi(x,y) = -q[p(x,y) - n(x,y) - N_D(x,y)], \tag{8.15a}$$

[SiO_2 layer]

$$\varepsilon_0 \varepsilon_{ox}\nabla^2\phi(x,y) = 0, \tag{8.15b}$$

where ε_0 is the dielectric constant of the vacuum, ε_{ox} is the relative dielectric constant of SiO_2, $\varepsilon_S(x,y)$ is the relative dielectric constant of silicon and the transition layer, $\phi(x,y)$ is the intrinsic potential at the mesh point, $p(x,y)$ is the hole concentration, $n(x,y)$ is the electron concentration, and $N_D(x,y)$ is the net ionized impurity doping concentration including the sign.

In the calculation, the conventional linear expansion technique was used and the numerical analysis was carried out. However, I did not explicitly take into account the effects of any traps for simplicity of the analysis.

8.4 Device Fabrication

MOSFETs/SOI with various silicon thicknesses were fabricated using three SIMOX substrates; processing parameters are summarized for each substrate in Table 8.1(a) to (c). The presence or absence of a transition layer is determined by AES and a cross-sectional scanning electron microscope (XSEM) for substrates 'A' and 'B', and a cross-sectional transmission

Table 8.1 Processing parameters for SIMOX substrates. © 1992 IEEE. Reprinted, with permission, from Y. Omura and K. Izumi, A macroscopic physical model and capacitive response of the buried oxide having a transition layer in a SIMOX substrate, *IEEE Transactions on Electron Devices*, vol. 39, pp. 1916–1921, 1992

(a) Substrate A

Parameters [unit]		Process condition	
Implantation energy [keV]		150	
Dose of oxygen atoms [cm^{-2}]	1.2×10^{18}	1.8×10^{18}	2.4×10^{18}
Anneal temperature [°C]		1150	
Anneal time [min]		120	
Comments	Thick TL	Thin TL	No TL

(b) Substrate B

Parameters [unit]	Process condition
Implantation energy [keV]	80
Dose of oxygen atoms [cm^{-2}]	1.0×10^{18}
Anneal temperature [°C]	1150
Anneal time [min]	120
Comments	Thick TL

(c) Substrate C

Parameters [unit]	Process condition
Implantation energy [keV]	150
Dose of oxygen atoms [cm^{-2}]	2.0×10^{18}
Anneal temperature [C]	1350
Anneal time [min]	240
Comments	No TL

TL: Transition layer.

electron microscope (XTEM) for substrate 'C'. A schematic cross-section of the fabricated device is shown in Figure 8.4(b).

After high-temperature annealing, an epitaxial silicon layer was grown on top of substrates 'A' and 'B'. In these substrates, devices were isolated by the conventional local-oxidation-of-silicon (LOCOS) technique. In substrate 'C', devices were isolated by a silicon etching technique. After doping to adjust the threshold voltage, thin gate oxide was formed, followed by a polysilicon film deposition for the gate electrode. Ion implantation was carried out for doping into the gate and source/drain region. The final step was aluminum metallization.

8.5 Results and Discussion

8.5.1 Electrode-to-Electrode Capacitance Dependence on Frequency

Drain-to-substrate capacitance dependence on frequency measured using devices on the substrate 'A' is shown in Figure 8.5. Capacitance decreases with increasing frequency. For the oxygen doses of $1.2 \times 10^{18}\,\mathrm{cm}^{-2}$ and $1.8 \times 10^{18}\,\mathrm{cm}^{-2}$, however, peaks are found around 4 MHz; the existence of the transition layer in samples with those doses are confirmed by AES and XSEM [1,6]. For the oxygen dose of $2.4 \times 10^{18}\,\mathrm{cm}^{-2}$, no peak is found; no transition layer is found in this substrate by AES and XSEM [6].

For the oxygen doses of $1.2 \times 10^{18}\,\mathrm{cm}^{-2}$ and $1.8 \times 10^{18}\,\mathrm{cm}^{-2}$, the capacitance is smaller at any frequency than that for the dose of $2.4 \times 10^{18}\,\mathrm{cm}^{-2}$,in spite of the fact that the buried oxide thicknesses for the oxygen doses of $1.2 \times 10^{18}\,\mathrm{cm}^{-2}$ and $1.8 \times 10^{18}\,\mathrm{cm}^{-2}$ are smaller than that for the dose of $2.4 \times 10^{18}\,\mathrm{cm}^{-2}$. We guess that the depletion layer due to charged traps exists around the transition layer for low-dose cases.

On the other hand, calculated capacitance dependence on frequency is shown in Figure 8.6 for $C_{D\text{-}S}$, $C_{D\text{-}W}$, and $C_{W\text{-}S}$. In the calculation, a device on the substrate 'A' with the transition layer is supposed and the critical frequency f_o is assumed to be 1 MHz. The device parameters

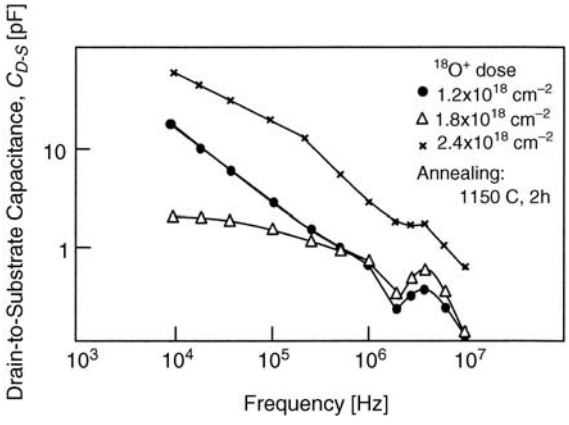

Figure 8.5 Drain-to-substrate capacitance on frequency: experimental results. © 1992 IEEE. Reprinted, with permission, from Y. Omura and K. Izumi, A macroscopic physical model and capacitive response of the buried oxide having a transition layer in a SIMOX substrate, *IEEE Transactions on Electron Devices*, vol. 39, pp. 1916–1921, 1992.

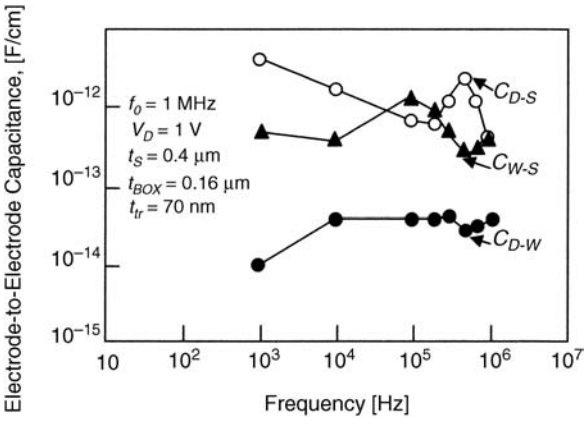

Figure 8.6 Electrode-to-electrode capacitance dependence on freqency: simulated results. © 1992 IEEE. Reprinted, with permission, from Y. Omura and K. Izumi, A macroscopic physical model and capacitive response of the buried oxide having a transition layer in a SIMOX substrate, *IEEE Transactions on Electron Devices*, vol. 39, pp. 1916–1921, 1992.

are listed in Table 8.2. A peak is found on the curve of $C_{D\text{-}S}$. In a device on the substrate 'A' without the transition layer, such a peak is not found on the curve of $C_{D\text{-}S}$. The fact that the peaks appear only for substrates having a buried oxide with the transition layer implies that the peaks are related to the electronic response of the transition layer.

The simulated results are in good agreement with the points of primary capacitance dependence on frequency and the appearance of the peaks. The model suggests that the critical frequency f_o is nearly equal to 8 MHz.

Here, we use the model to speculate on the origin of the peaks. Equivalent capacitance of the transition layer, $C_{tr}(f)$, is expressed as

$$C_{tr}(f) = \varepsilon_0 \left[\frac{d\varepsilon_{tr}}{dx} + \varepsilon_{tr} \frac{d}{d\varepsilon_{tr}} \left(\frac{d\varepsilon_{tr}}{dx} \right) \right]. \tag{8.16}$$

Table 8.2 Structural parameters of calculated device. © 1992 IEEE. Reprinted, with permission, from Y. Omura and K. Izumi, A macroscopic physical model and capacitive response of the buried oxide having a transition layer in a SIMOX substrate, *IEEE Transactions on Electron Devices*, vol. 39, pp. 1916–1921, 1992

Parameters	Values [unit]
Silicon layer thickness	400 [nm]
Buried oxide layer thickness	160 [nm]
Transition layer thickness	70 [nm]
Doping concentration in silicon layer	6×10^{16} [cm^{-3}]
Doping concentration in substrate	1×10^{13} [cm^{-3}]

The first term of the right-hand side originates from the internal electric field of the transition layer and the second from the deviation of the internal electric field by the external electric field. The derivative, $d\varepsilon_{tr}/dx$, is expressed using the cluster density $N(x,f)$ as

$$\frac{d\varepsilon_{tr}(x,f)}{dx} \propto \frac{dN(x,f)}{dx}, \tag{8.17}$$

where

$$\frac{dN(x,f)}{dx} = -\left(\frac{2x}{\Delta^2}\right) N_m \exp\left(-\frac{x^2}{\Delta^2}\right), \tag{8.18}$$

$$\Delta(f) = \Delta(0)\left[1 - \exp\left(-\frac{f}{f_0}\right)\right]. \tag{8.19}$$

As shown in Equations (8.16) to (8.19), $C_{tr}(f)$ is a Gaussian function Δ and peaks at $f = f_o/2$. Equation (8.16) reflects the capacitance peaks originating from the transition layer.

8.5.2 Drain-to-Substrate Capacitance Dependence on Bias

Drain-to-substrate capacitance, $C_{D\text{-}S}$, dependence on drain bias is shown in Figure 8.7(a). Capacitance was measured using devices on substrates 'B' and 'C'. In devices with thick transition layers, capacitance does not depend on the bias. In devices without a transition

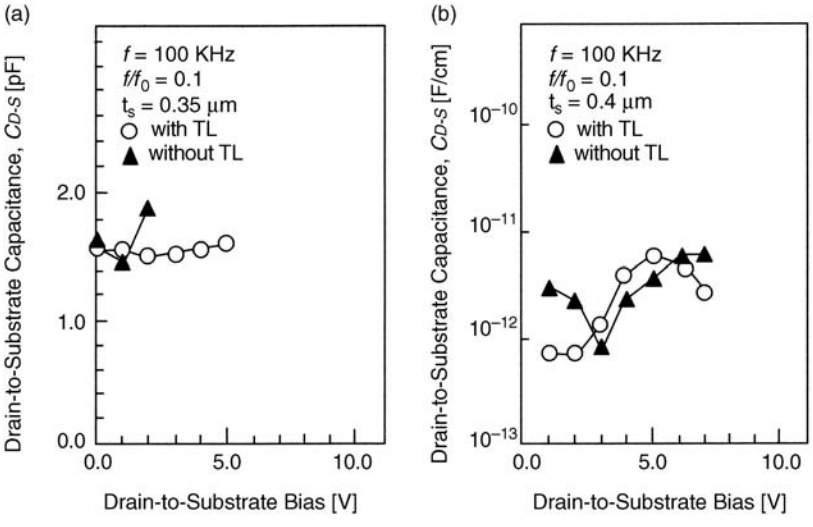

Figure 8.7 Drain-to-substrate capacitance dependence on bias. (a) Experimental results. (b) Simulated results. © 1992 IEEE. Reprinted, with permission, from Y. Omura and K. Izumi, A macroscopic physical model and capacitive response of the buried oxide having a transition layer in a SIMOX substrate, *IEEE Transactions on Electron Devices*, vol. 39, pp. 1916–1921, 1992.

layer, however, normal capacitance dependence on bias is obtained. Lee and Cristoloveanu have reported capacitance dependence on bias in a MOS capacitor on the SIMOX substrate having a buried oxide without the transition layer [10]. Their result is quite similar to ours without the transition layer.

Calculated results for drain-to-substrate capacitance dependences on bias with or without the transition layer are shown in Figure 8.7(b). In the case with the transition layer, the capacitance strongly depends on bias. Without the transition layer, the normal capacitance dependence on bias is obtained. In this case, the inversion layer is presumed to be formed below the buried oxide at the minimum of capacitance.

A comparison of Figure 8.7(a) with Figure 8.7(b) confirms that the calculated results without the transition layer are reasonable. Calculated results with the transition layer, however, do not indicate the behavior observed experimentally, which might be due to the lack of a realistic trap model in the transition layer.

To verify the model, we now discuss the cause of the drain-to-substrate capacitance dependence on the bias in the case with a transition layer. Calculated results on the relationship between the applied voltage and the voltage drop in the buried oxide are shown in Figure 8.8. Device parameters used in the simulation are the same as shown in Table 8.2. Without the transition layer, the surface potential of the top of the substrate (the bottom of the buried oxide) is pinned at $2\phi_F$ after the onset of the inversion. Therefore, the voltage drop of the buried oxide increases linearly with increasing applied voltage. With the transition layer, however, the voltage drop of the buried oxide is very small and almost constant, which means that almost all applied voltage is applied to the transition layer. This suggests that the capacitive response of the buried oxide with the transition layer is strongly influenced by the capacitive response of the transition layer, and that this result is attributable to the

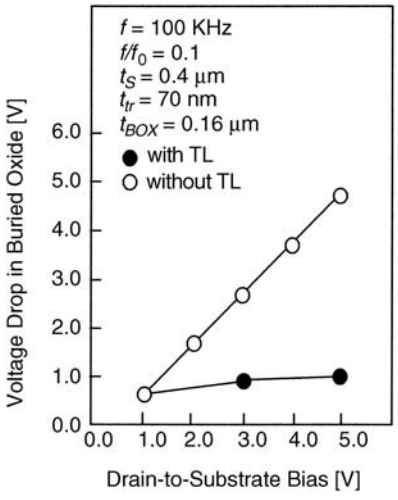

Figure 8.8 Voltage drop dependence on drain-to-substrate bias in buried oxide: simulated results. © 1992 IEEE. Reprinted, with permission, from Y. Omura and K. Izumi, A macroscopic physical model and capacitive response of the buried oxide having a transition layer in a SIMOX substrate, *IEEE Transactions on Electron Devices*, vol. 39, pp. 1916–1921, 1992.

macroscopic band structure model of the transition layer shown in Figure 8.3. As depicted in the figure, the bandgap of the transition layer varies from the value of the silicon to the value of the oxide, which indicates the presence of a large internal electric field in the transition layer. A part of the external electric field is absorbed by the internal electric field in the transition layer. In our model, however, all carriers in the transition layer can respond to the external electric field owing to no traps; that is, the capacitance strongly depends on the bias. Since, in a practical case, there are many traps in the transition layer, most of carriers are trapped in the transition layer and they do not respond to the external electric field; the capacitance does not show such a sensitive behavior on bias.

To clarify the above discussion on the internal electric field in the transition layer, the internal electric field and the effective charge density of the transition layer are calculated and shown in Figure 8.9. In the calculation, we assume that the thickness of the transition layer is equal to 70 nm and use the standard parameters for silicon and SiO_2. The internal electric field and the effective charge density are expressed as

$$\text{Internal electric field} = -\frac{dE_{gtr}(x,f)}{qdx}, \tag{8.20}$$

$$\text{Effective charge density} = -\frac{d^2E_{gtr}(x,f)}{qdx^2}. \tag{8.21}$$

It can be seen from Figure 8.9 that a strong internal electric field exists in the transition layer. The maximal electric field is beyond 10^5 V/cm, which could easily cause the transition layer to charge up. It is considered that the electrons emitted from the transition layer constitute the charged double layer below the transition layer, which would explain why

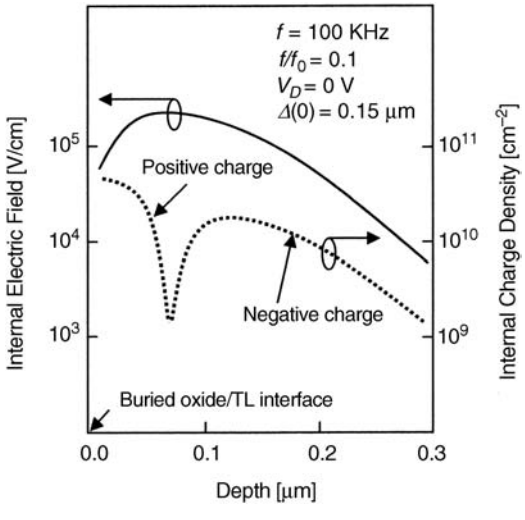

Figure 8.9 Internal electric field and charge density in the transition layer: simulated results. © 1992 IEEE. Reprinted, with permission, from Y. Omura and K. Izumi, A macroscopic physical model and capacitive response of the buried oxide having a transition layer in a SIMOX substrate, *IEEE Transactions on Electron Devices*, vol. 39, pp. 1916–1921, 1992.

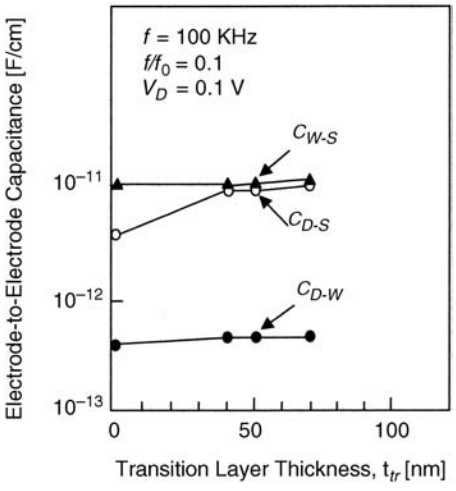

Figure 8.10 Electrode-to-electrode capacitance dependence on the transition layer thickness: simulated results. © 1992 IEEE. Reprinted, with permission, from Y. Omura and K. Izumi, A macroscopic physical model and capacitive response of the buried oxide having a transition layer in a SIMOX substrate, *IEEE Transactions on Electron Devices*, vol. 39, pp. 1916–1921, 1992.

almost all of the externally applied voltage is applied to the transition layer; the charge-up process of the transition layer prevents the voltage-drop increase in the buried oxide core. Therefore, the proposed model adequately explains the nature of the transition layer except for the capacitance dependence on the bias.

8.5.3 Electrode-to-Electrode Capacitance Dependence on Transition Layer Thickness

Calculated capacitance dependences on transition layer thickness are shown in Figure 8.10. Drain-to-wire capacitance and wire-to-substrate capacitance are not affected. Drain-to-substrate capacitance, however, increases with increasing transition layer thickness. A capacitance increase is attributed to the increase in the charge induced by the transition layer itself. The transition layer should be eliminated from the viewpoint of the parasitic capacitance reduction.

8.6 Summary

To evaluate the capacitance of the buried oxide layer with a transition layer, a macroscopic physical model was proposed using the Clausius–Mossotti relationship for two media. The capacitive response of the transition layer was discussed using numerically analyzed and experimental data. The results are summarized as follows:

1. Peaks in the capacitance dependence on frequency were found only in the devices with the buried oxide having a transition layer. These phenomena can be explained by the proposed model.

2. The capacitance dependence on applied voltage cannot be sufficiently explained by the model. However, the model can reasonably explain the nature of the transition layer.
3. It is shown that the transition layer between the superficial silicon and buried oxide layer should be eliminated to reduce parasitic capacitance.

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Part Three

Physics and Modeling of SOI Lubistors – Thin-Film Devices

9

Negative Conductance Properties in Extremely Thin SOI Lubistors

9.1 Introduction

Recently, low-dimensional transport properties of SOI structures have attracted attention due to the potential usefulness of these properties in future quantum-effect devices fabricated on SOI substrates [1–6]. Some features of low-dimensional transport are found not only in such majority carrier devices but also in minority carrier devices, such as simple pn-junction devices [7,8].

Fundamental features of two-dimensional transport in extremely thin SOI insulated-gate pn-junction devices fabricated on SIMOX substrates have previously been described [7,8]. In these devices, two-dimensionally quantized injection of carriers was clearly observed at low temperatures. Because the above device structure is essentially the same as that of a surface tunnel transistor (STT) [9], we anticipated the manifestation of negative conductance. However, it was observed in a bulk MOS structure only at very low temperatures [10]. In the present study the occurrence of negative conductance in an extremely thin SOI Lubistor (SOI surface tunnel transistor: SOI STT) is clearly demonstrated. Features of the negative conductance in the SOI structure are also discussed.

9.2 Device Fabrication and Measurements

Two types of SOI STTs, the device structures of which are shown schematically in Figure 9.1(a), were fabricated on SIMOX substrates with very small surface and interface roughness [11]. One had a 10-nm-thick silicon layer (t_s) and a 5-nm-thick gate oxide layer (t_{ox}), and the other had a 90-nm-thick silicon layer and a 5-nm-thick gate oxide layer. The gate length (L_G) was 3 μm. The thin gate oxide layer was formed by rapid thermal oxidation, followed by deposition of n-type polysilicon as a gate electrode. Since no intentional ion implantation into the p-type body region was carried out, the body region had a doping concentration of less than $1 \times 10^{16}\,\mathrm{cm}^{-3}$. A p-type diffusion region (anode) was formed by boron ion implantation, while an n-type diffusion region (cathode) was formed by phosphorus ion implantation.

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

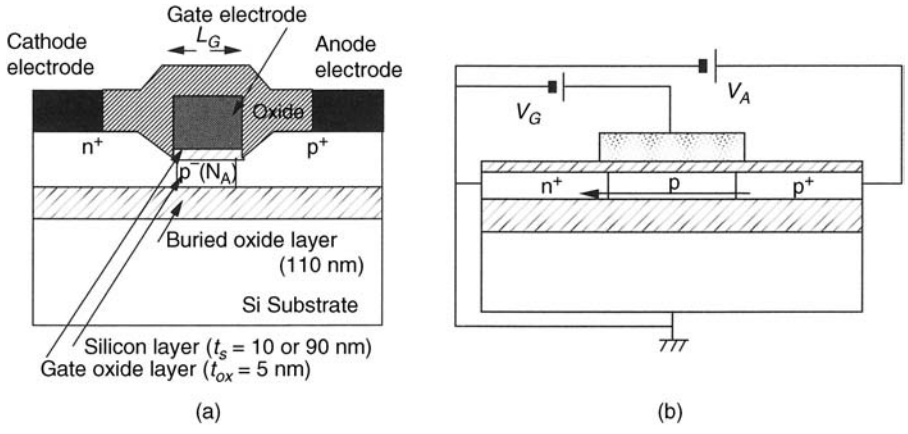

Figure 9.1 Device structure and bias configuration of an ultra-thin SOI Lubistor. (a) A schematic device cross-section. (b) Measurement configuration. Copyright 1996. The Japan Society of Applied Physics. [Y. Omura, Negative conductance properties in extremely thin silicon-on-insulator (SOI) insulated-gate pn-junction devices (SOI surface tunnel transistors), *Japanese Journal of Applied Physics*, vol. 35, pp. L1401–L1403, 1996].

The measurement configuration for the SOI STTs is shown in Figure 9.1(b). Measurements with the cathode common configuration were carried out at temperatures ranging from 45 K to 300 K. Substrate bias was not applied.

9.3 Results and Discussion

The anode current (I_A) and anode differential conductance (g_A) dependences on anode voltage (V_A) at 45 K are shown for $t_s = 10$ nm in Figure 9.2. As mentioned in previous papers [7,8], g_A curves show step-like anomalies that correspond to the two-dimensional subband structure of the system. When the gate voltage (V_G) is 2 V, clear negative conductance is detected at V_A of around 0.7 V. Negative conductance is not detected at V_G of 1 V or 3 V. At V_G of 1 V, the electron concentration of the inversion layer is not high enough for the tunneling to occur. At V_G of 3 V, however, the situation is different. The surface of the gate-overlapping anode region is depleted partially by the high positive V_G, as shown in Figure 9.2, and most of the junction current flows near the silicon layer/buried oxide layer interface. Because the electron concentration in this region is lower than that at the upper surface of the silicon layer, tunneling is suppressed.

On the other hand, the anode voltage where the negative conductance is detected is slightly higher than that in bulk tunneling devices [10]. In extremely thin SOI devices, the potential difference between the upper and lower surfaces of the silicon layer is very small. Thus, the confinement of electrons raises the internal potential of the whole silicon layer at the same time [12]. This is an important feature of extremely thin SOI devices.

I_A dependence on V_A at a V_G of 2 V for five different temperatures is shown in Figure 9.3. Negative conductance becomes unclear at temperatures higher than 100 K. Negative conductance is detected at temperatures of less than 90 K. The maximum temperature is limited by both the increase in background hole concentration, which is determined by the intrinsic

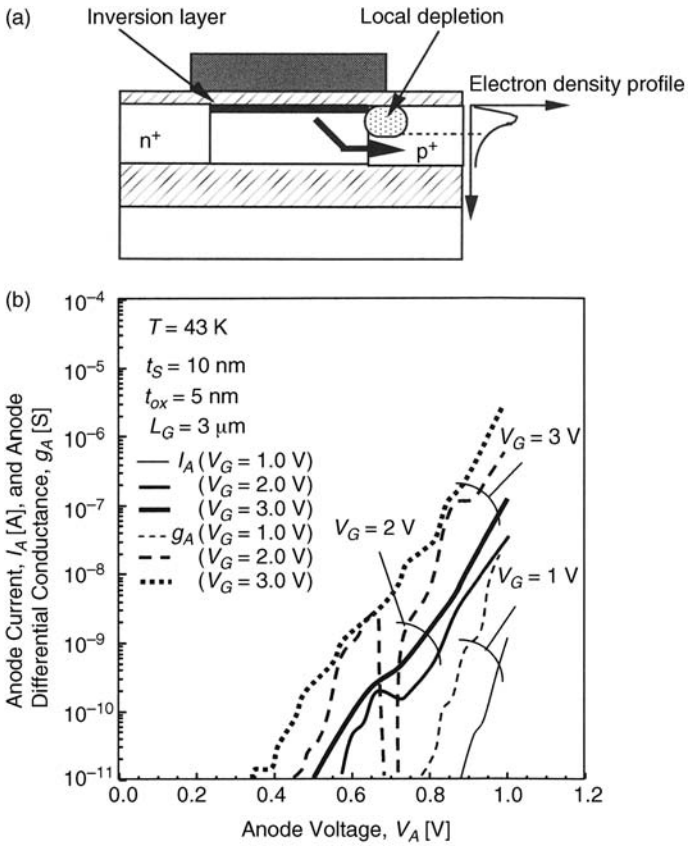

Figure 9.2 Anode current (I_A) and anode differential conductance (g_A) dependences on anode voltage (V_A) at 45 K for three-different gate voltages (V_G). The silicon layer is 10 nm thick. (a) A schematic of the setup used during operation at V_G of 3 V. (b) I_A and g_A characteristics as a function of V_A. Copyright 1996. The Japan Society of Applied Physics. [Y. Omura, Negative conductance properties in extremely thin silicon-on-insulator (SOI) insulated-gate pn-junction devices (SOI surface tunnel transistors), *Japanese Journal of Applied Physics*, vol. 35, pp. L1401–L1403, 1996].

carrier concentration [7,8], and the smearing of the two-dimensional subband structure, the occurrence of which is confirmed by comparison of the thermal energy and the energy splitting of the subband.

Negative conductance was also detected at a V_G of 3 V in an SOI STT with a 90-nm-thick silicon layer, as shown in Figure 9.4. The gate voltage at which the negative conductance was detected was higher than that for the SOI STT with a 10-nm-thick silicon layer, shown in Figure 9.2. This is because the confinement of electrons under the gate becomes relatively loose in the thicker SOI device and a higher V_G is necessary to hold the same electron density as that for $t_s = 10$ nm. In this device, it must be considered similarly that the local depletion occurs around the gate-overlapping anode region at a high gate voltage. This is consistent with the result shown in Figure 9.2 for the 10-nm-thick SOI device because the negative conductance disappears when the gate voltage

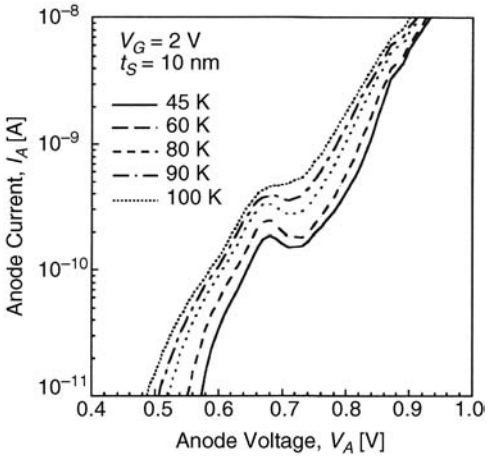

Figure 9.3 Anode current (I_A) dependence on anode voltage (V_A) at $V_G = 2$ V for five different temperatures ranging from 45 K to 100 K. Copyright 1996. The Japan Society of Applied Physics. [Y. Omura, Negative conductance properties in extremely thin silicon-on-insulator (SOI) insulated-gate pn-junction devices (SOI surface tunnel transistors), *Japanese Journal of Applied Physics*, vol. 35, pp. L1401–L1403, 1996].

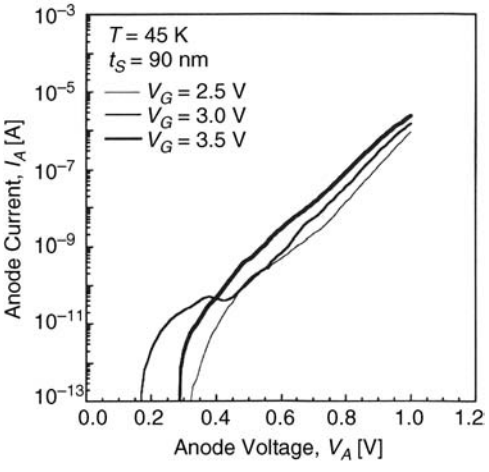

Figure 9.4 Anode current (I_A) dependence on anode voltage (V_A) at 45 K for three different gate voltages (V_G). The silicon layer is 90 nm thick. Copyright 1996. The Japan Society of Applied Physics. [Y. Omura, Negative conductance properties in extremely thin silicon-on-insulator (SOI) insulated-gate pn-junction devices (SOI surface tunnel transistors), *Japanese Journal of Applied Physics*, vol. 35, pp. L1401–L1403, 1996].

becomes high. However, quantitative analysis is required for obtaining a complete explanation of the difference between these device characteristics shown in Figures 9.2 and 9.4.

On the other hand, the anode voltage at which the negative conductance was detected was lower than that for $t_s = 10\,\text{nm}$. In thicker SOI devices, naturally the potential difference between the upper and lower surfaces of the silicon layer becomes large and the confinement of electrons does not lead to a sufficient potential shift of the silicon layer. Thus, the anode bias at which the negative conductance occurs decreases. In other words, the mechanism of the negative conductance resembles that of the bulk devices. The maximum temperature at which negative conductance is detected is 60 K.

In Figures 9.1 and 9.3, the peak-to-valley ratio of negative conductance is small. This is due to states in the forbidden gap [13], which are created by ion implantation and remained after the device fabrication process.

9.4 Summary

Negative conductance was detected at temperatures of less than 90 K in an SOI surface tunnel transistor (Lubistor) with a 10-nm-thick silicon layer fabricated on an SIMOX substrate. Through comparison with the performance of an SOI surface tunnel transistor (Lubistor) with a 90-nm-thick silicon layer, the advantages of the two-dimensional confinement effect were shown.

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10

Two-Dimensionally Confined Injection Phenomena at Low Temperatures in Sub-10-nm-Thick SOI Lubistors

10.1 Introduction

The ultra-thin SOI structure is attracting attention due to the remarkable improvement it has achieved in MOSFET performances [1–3]. It is believed that ultra-thin SOI MOSFETs are the most promising devices of the many kinds of MOS devices. On the other hand, I proposed the Lubistor [4]. It is an ultra-thin SOI device and exhibits gate-controlled bipolar operation. Generally speaking, bipolar devices do not operate at low temperatures owing to a lack of free minority carriers. However, since the insulated gate can induce any type of carrier, the insulated gate structure is a good candidate for bipolar device applications. Recently, quantum mechanical effects in ultra-thin SOI MOSFETs have been studied by some researchers [5–7], but there have been no reports of these effects in pn-junction devices in spite of their importance for future applications.

This chapter describes fundamental properties of thin SOI Lubistors at low temperatures. Two-dimensionally confined effects on carrier injection are discussed based on the low-temperature characteristics. These effects are examined by theoretical simulations. Finally, possible influences on the characteristics of ultra-thin SOI MOSFET devices are mentioned.

10.2 Experiments

Schematic device structures [4] and measurement configurations are shown in Figure 10.1(a) and (b). Devices with a 16-μm-wide gate and a 7-nm-thick gate oxide were fabricated on a SIMOX substrate with an 8-nm-thick superficial silicon layer and an 80-nm-thick buried oxide

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

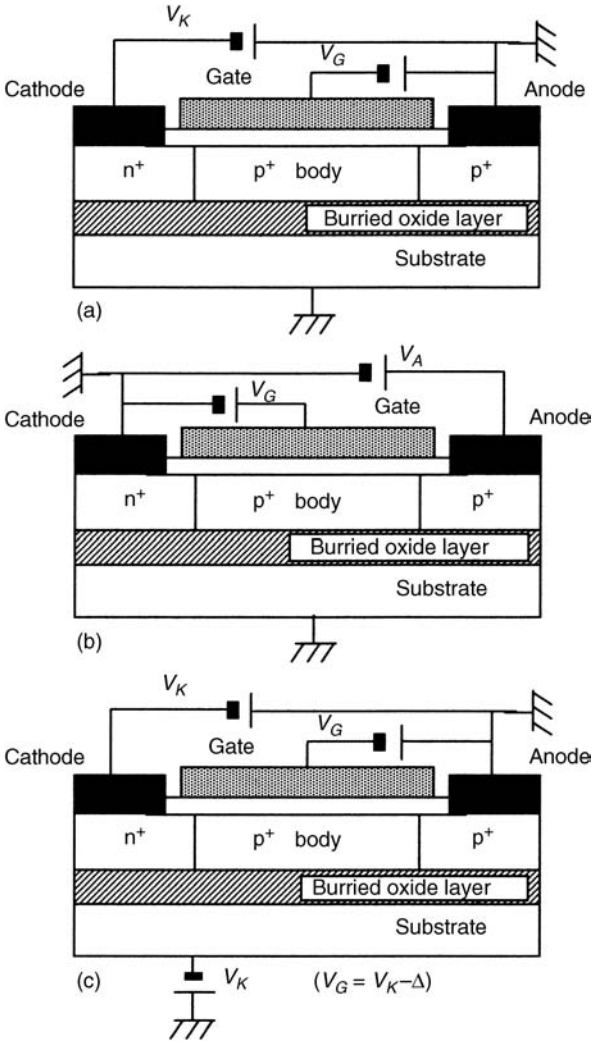

Figure 10.1 Schematic device structure of Lubistor and measurement configurations. (a) Anode common configuration. (b) Cathode common configuration. (c) Reformed geometry for cathode common configuration. (Note that the effective substrate bias exists in order to assist the front gate bias. Gate bias is deeper than the cathode bias by Δ.) © 1996 IEEE. Reprinted, with permission, from Y. Omura, Two-dimensionally confined injection phenomena at low temperatures in sub-10-nm-thick SOI insulated-gate p-n-junction devices, *IEEE Transactions on Electron Devices*, vol. 43, pp. 436–443, 1996.

layer [3]. The gate length is 0.3 μm. The p-type body has a doping concentration of $1 \times 10^{17}\,\mathrm{cm}^{-3}$. An extremely thin SOI structure was used in the expectation of manifesting a two-dimensional subband system (2DSS) [5].

The energy difference between the lowest subband level and the bottom of the conduction band is 20 meV (at 240 K) for the 8-nm-thick superficial silicon layer. The measurements were carried out from 300 K to 28 K.

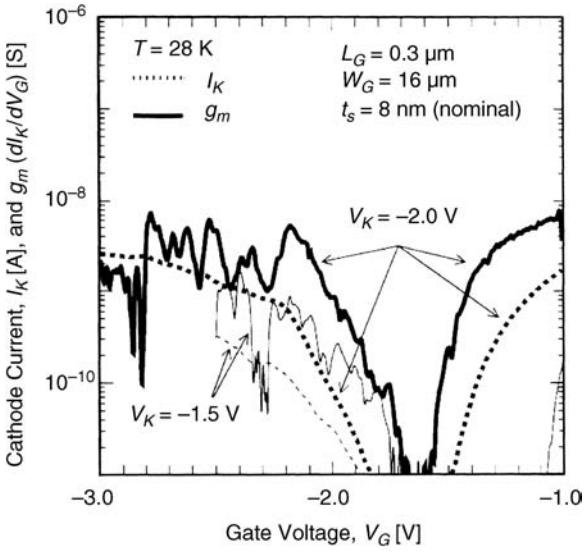

Figure 10.2 Forward cathode current (I_K) and transconductance (g_m) dependences on gate voltage at 28 K. Absolute values are plotted for g_m values. © 1996 IEEE. Reprinted, with permission, from Y. Omura, Two-dimensionally confined injection phenomena at low temperatures in sub-10-nm-thick SOI insulated-gate p-n-junction devices, *IEEE Transactions on Electron Devices*, vol. 43, pp. 436–443, 1996.

10.2.1 Anode Common Configuration

Cathode current (I_K) and g_m ($=dI_K/dV_G$) dependences on gate voltage (V_G) measured at 28 K are shown in Figure 10.2. Here, I_K dips around $V_G \sim -1.6$ V. At the dip, the injection mode changes drastically because the surface potential polarity switches; at $V_G < -1.6$ V, holes accumulate under the gate, and at $V_G > -1.6$ V, an electron inversion layer exists under it. At $V_G < -1.6$ V, hole injection from the p^- region to the n^+ region becomes dominant owing to both hole accumulation in the p^- region and a decrease in the number of electrons in the n^+ region under the gate.

This means that I_K must be mainly composed of hole current. At $V_G > -1.6$ V, on the other hand, electron injection from the n^+ region to the p^- region becomes dominant owing to the inversion layer in the p^- region. Therefore, in contrast to the former ($V_G < -1.6$ V), I_A must be mainly composed of electron current.

It should be noted that distinct kinks in I_K can be found at $V_G < -1.6$ V. These kinks can be supported by the specific features in g_m characteristics. At $-2.2\,\text{V} < V_G < -1.0\,\text{V}$, the g_m curve has step-like features, and at $V_G < -2.2$ V, it has strong oscillation-like features for $Vc = -2.0$ V.

Since the sweep of V_G corresponds to that of the Fermi levels of both the p^- body region and the n^+ region under the gate, the above features of g_m curves are most likely to originate from the 2DSS of the thin SOI structure. However, no specific features in I_K and g_m could be found at temperatures higher than 100 K.

10.2.2 Cathode Common Configuration

The cathode common configuration shown in Figure 10.1(b) is a little complicated with respect to each net terminal bias, so the configuration was rearranged as in Figure 10.1(c). The

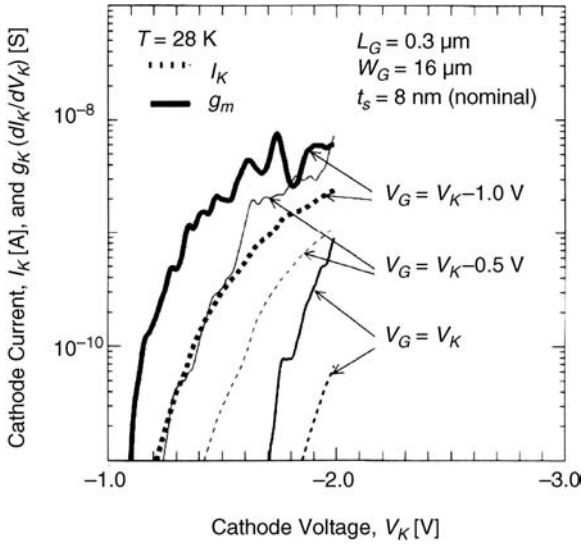

Figure 10.3 Forward cathode current (I_K) and cathode conductance (g_K) dependences on cathode voltage at 28 K. Absolute values are plotted for g_K values. © 1996 IEEE. Reprinted, with permission, from Y. Omura, Two-dimensionally confined injection phenomena at low temperatures in sub-10-nm-thick SOI insulated-gate p-n-junction devices, *IEEE Transactions on Electron Devices*, vol. 43, pp. 436–443, 1996.

effective configuration indicates that the cathode bias, the gate bias and the substrate bias are swept at the same time. The gate bias is set relatively high compared to the cathode bias, which holds the hole accumulation under the top and bottom interfaces of the superficial silicon layer at a high negative V_c.

Cathode current (I_K) and g_K ($=dI_K/dV_K$) dependences on cathode voltage (V_K) measured at 28 K are shown in Figure 10.3. The I_K curves show distinct kinks, whereas the g_K curves show clear step-like features for a low negative V_K and oscillation-like features for a high negative V_K. Not only the cathode voltage but also the gate voltage is swept at this configuration, and the change in the gate bias results in the Fermi-level shift.

This is the same situation as that of the anode common configuration. Therefore the enhancement of the step-like features probably originates from the effective substrate bias, which assists the front gate bias as shown in Figure 10.1(c) [6]. Detailed mechanisms are discussed in the following chapter.

Though not described here, similar experimental results were obtained for positive gate biases.

10.3 Physical Models and Simulations

10.3.1 Fundamental Models

First, the band scheme in this device is discussed. Since the distance between the impurity sites is about 1 nm in the n^+ and p^+ regions, the conventional 2DSS can be employed in these regions.

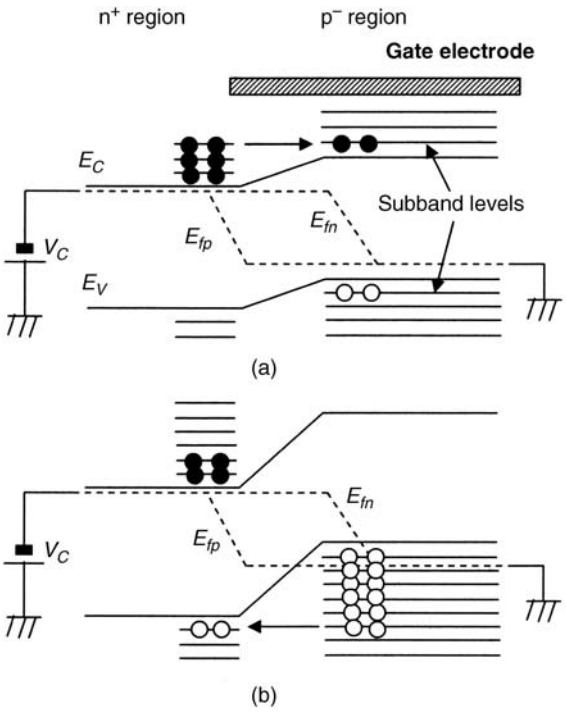

Figure 10.4 Band diagrams in the device under the two different gate voltage conditions. (a) Low negative gate voltage. (b) High negative gate voltage. E_c: conduction band bottom; E_v: valence band top; E_{fp}: quasi-Fermi level of holes; E_{fn}: quasi-Fermi level of electrons. © 1996 IEEE. Reprinted, with permission, from Y. Omura, Two-dimensionally confined injection phenomena at low temperatures in sub-10-nm-thick SOI insulated-gate p-n-junction devices, *IEEE Transactions on Electron Devices*, vol. 43, pp. 436–443, 1996.

In the p^- region, however, the distance is about 35 nm owing to the low doping; that is, the local impurity site affects the binding energy of the impurity and the eigen energy decreases owing to the increase in binding energy [8]. While this is quite important for optical responses, only static characteristics are discussed in this section. Hence, limited semiquantitative discussions are presented with respect to the previously mentioned quantum mechanical influences.

Simple schematic band diagrams of the device operation are shown in Figure 10.4. Here, the influence of local impurity sites is neglected. The carrier injection mechanism for a low negative V_G is shown in Figure 10.4(a) and that for a high negative V_G is shown in Figure 10.4(b). Since the whole SOI layer is 8 nm thick, the 2DSS must be created over the whole SOI layer. In Figure 10.4(a) for a low negative V_G, many electrons still exist even at high energy levels in the n^+ region. In this case electron injection from the n^+ to the p^- region might be possible because the electron concentration in the p^- region is not so low. In Figure 10.4(b) for a high negative V_G, on the other hand, many holes exist even at high energy levels in the p^- region because the hole Fermi level incidentally goes below the valence band top, which results in a decrease in electron concentration in the p^- region.

In contrast, in the n^+ region, the electron Fermi level goes below the conduction band bottom, which results in a relative increase in the hole concentration. Therefore, the previous

electron injection is suppressed and the hole injection from the p^- to n^+ region is strongly promoted.

Both of the above experimental results and the band scheme suggest that each injection mode is ruled by the two-dimensional (2-D) subband levels and the density of states of each carrier type, and that both g_m and g_K directly reflect the two-dimensional subband structure. Since the transition region of the pn junction is thin, the region is also quantized. Even in the transition region carriers must fundamentally show the two-dimensional transport nature. Here, a physical picture of the transition region is discussed by using Figure 10.5 to assist in the understanding of the device operation.

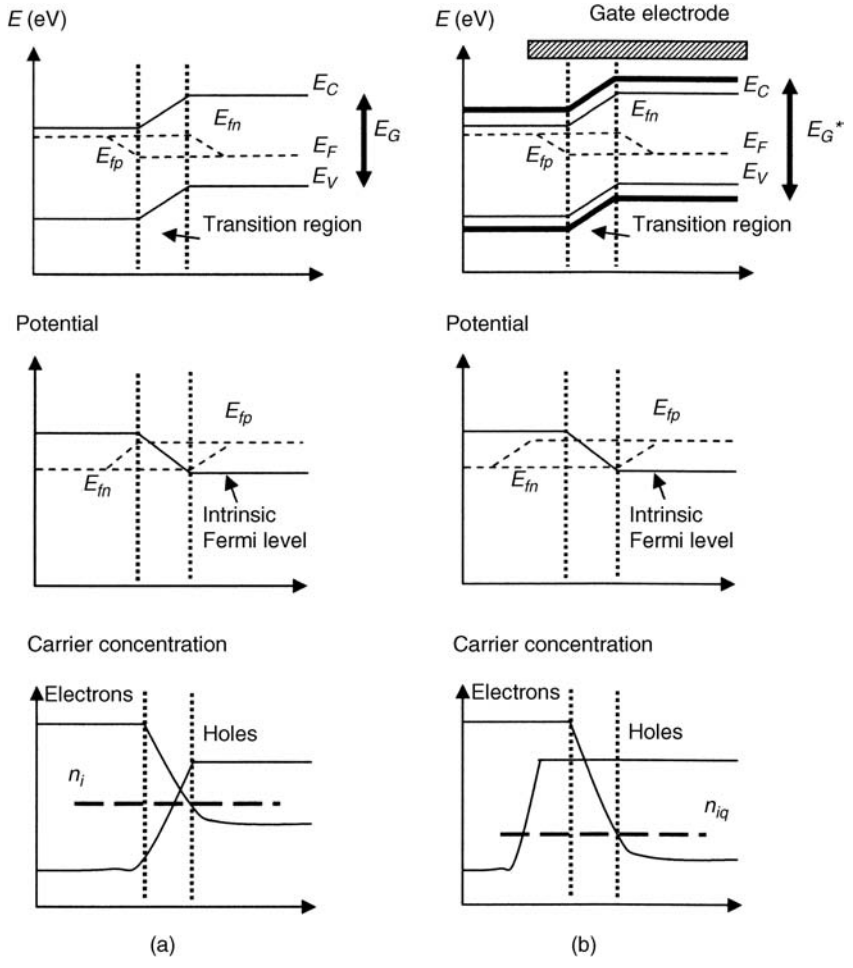

Figure 10.5 Schematic energy band diagram, intrinsic Fermi level (ψ), quasi-Fermi level (E_{fn} and E_{fp}), and carrier distributions under forward-biased conditions for two-dimensional and three-dimensional systems. (a) Bulk three-dimensional system. (b) Thin SOI two-dimensional system. © 1996 IEEE. Reprinted, with permission, from Y. Omura, Two-dimensionally confined injection phenomena at low temperatures in sub-10-nm-thick SOI insulated-gate p-n-junction devices, *IEEE Transactions on Electron Devices*, vol. 43, pp. 436–443, 1996.

First, the conventional assumptions and approximations for the three-dimensional system are summarized below:

1. Boltzmann approximation for the carrier statistics: the Fermi level is given by a simple expression.
2. Low-injection level assumption: minority carrier concentration inside the injected region is much smaller than majority carrier concentration. In the three-dimensional system, as shown in Figure 10.5(a), the *imref*s are constant in the transition region and the minority carrier concentration dramatically decreases in the transition region by the bias factor of $\exp[qV_K/k_BT]$.
3. Abrupt depletion approximation: depletion layers have clear boundaries and their outside regions are neutral.

In the two-dimensional system, the corresponding assumptions are summarized below and the corresponding illustration is shown in Figure 10.5(b).

1. Carrier statistics: assuming that the Fermi level stays inside the forbidden bandgap, which is reasonable for the low-injection level, the Boltzmann-like statistics for carriers can be employed (see Appendix 10A) and the intrinsic carrier concentration (n_{iq}) is given by Equation (10A.8). The expression is quite similar to the conventional three-dimensional case except for both the increase in the effective bandgap and the decrease in the effective density of states. In other words, Equation (10A.8) for n_{iq} can be used as an expression for the quasi-Boltzmann statistics.
2. Low-injection level assumption: the gate electrode covers the metallurgical junction surface including the transition region in the thin SOI Lubistor (see Figures 10.1 and 10.4). Therefore, *imref*s are almost constant inside the transition region and both electron and hole concentrations are also almost constant, as shown in Figure 10.5(b). It should be noted that the latter is quite different from the three-dimensional case. However, the boundary conditions for carrier concentrations at the gate electrode edge are similar to the three-dimensional case owing to constant *imref*s inside the transition region. Therefore, the diffusion equation for the carrier has an expression almost equivalent to the three-dimensional case.
3. Depletion approximation in the transition region: depletion approximation is not fundamentally affected by the low-dimensional nature. However, it should be noted that the effective increase in the bandgap (E_G^* in Figure 10.5(b)) leads to the relative expansion of the depletion layer.

Therefore, the above assumptions and approximations for the two-dimensional SOI system are very similar to those for the three-dimensional system except for the specific condition for carrier concentration inside the transition region.

Now, since *imref*s are constant inside the transition region, carriers must move along the oblique energy band structure. Thus it can be considered that they show their transitions between subband levels. As a result, it is quite natural from the microscopic point of view that the transport characteristics of carriers reflect the 2DSS.

As aforementioned, however, the carrier concentration inside the transition region is almost constant owing to the gate electrode, which means the specific transport characteristics are masked partially. Therefore, this suggests that the existence of the special transition region

causes no practical problems. This approximation is acceptable for DC analysis. Thus, for simplicity, details of the mathematical manipulation for the transition region are not shown here.

10.3.2 Theoretical Simulations

The above experimental results are examined by a simplified theoretical model, where a plain rectangular potential well, a low-injection level, and a single subband system for each carrier are assumed for simplicity. Here it is considered that the carrier transport in the transition region of the pn junction is macroscopically identical to the conventional three-dimensional system as mentioned above.

Since the exact transport scheme for this region is complicated, a detailed theoretical formulation was described in Part One. Thus at the low-injection level, I_K can be written as

$$I_K = I_{K0}\left[\exp\left(\frac{qV_K}{nk_BT}\right) - 1\right], \tag{10.1}$$

$$I_{K0} = \frac{qD_p p(V_G)}{L_p} + \frac{qD_n n(V_G)}{L_n} \tag{10.2}$$

where I_{K0} is the saturation current density, D_p is the hole diffusion constant, D_n is the electron diffusion constant, L_p is the hole diffusion length, and L_n is the electron diffusion length. The index n is the ideality factor. In the calculations, L_p and L_n are

$$L_p = \sqrt{D_p\tau_p} \tag{10.3}$$

and

$$L_n = \sqrt{D_n\tau_n}, \tag{10.4}$$

where τ_p and τ_n are lifetimes for holes and electrons, respectively. A typical value of 10 μs was used for τ_p and τ_n. Diffusion constants were determined from the specific mobility values based on the Einstein relation and $p(V_G)$ and $n(V_G)$ are the hole and electron concentrations depending on V_G, respectively.

These parameters also depend on the band structure of the 2DSS. In such a thin-SOI system, the potential difference between the top surface potential and the bottom surface potential of the superficial silicon layer is very small. Hence the top surface potential can be used as a representative of the internal potential. Thus $p(V_G)$ and $n(V_G)$ are expressed approximately as

$$p(V_G) = \frac{n_{iq}^2}{n_{SOI}} \exp\left(\frac{-q\phi_{sn}}{k_BT}\right) \tag{10.5}$$

and

$$n(V_G) = \frac{n_{iq}^2}{p_{SOI}} \exp\left(\frac{q\phi_{sp}}{k_BT}\right), \tag{10.6}$$

where n_{iq} is the intrinsic carrier concentration for the 2DSS, n_{SOI} is the electron concentration in the n^+ region at thermal equilibrium, p_{SOI} is the hole concentration in the p^- region at thermal equilibrium, ϕ_{sn} is the top surface potential in the n^+ region, and ϕ_{sp} is the top surface potential in the p^- region. These surface potentials are functions of V_G. Derivations of n_{iq} and the Fermi level are described in Appendix 10A and the method for calculating $n(V_G)$ and $p(V_G)$ is described in Appendix 10B.

Simulated I_K and g_m dependences on V_G at 28 K for the anode common configuration are shown in Figure 10.6(a) for the two different uniform superficial silicon layer thicknesses. Here, it is assumed for simplicity that $n = 1$ in Equation (10.1). In the I_K curves there are kinks at low negative V_G and undulations at high negative V_G, while in the g_m curves there are steps at low negative V_G and oscillation-like features at high negative V_G. The comparison between the simulation results and the experimental results suggests that $n > 1$ in a practical device.

In simulations shown in Figure 10.6(a), the bias condition of V_K is not -1.5 V, but -1.2 V. When $V_K = -1.5$ V, it has been found that the oscillation-like feature in g_m characteristics appears at a higher negative gate voltage compared with the experimental result. This suggests that the actual thickness of the SOI layer is slightly thinner than 8 nm. Since the main purpose of theoretical simulations is to clarify the fundamental mechanism, the above simulation results are plotted as they are.

The steps in the g_m curves are attributed to hole injection from the p^- region to the n^+ region. Since holes share the subband levels in both the p^- region and the n^+ region when V_G increases in the negative direction, the density of injected holes reflects the band structure of the 2DSS. It should be noted that the hole injection into the n^+ region becomes fundamentally dominant for a negative V_G and that the concentration of holes injected into the n^+ region is proportional to the concentration of holes that can share hole subband-level sites in the n^+ region.

Since, for a low negative V_G, most subband-level sites for holes are vacant in the n^+ region owing to the predominance of electrons, the hole injection reflects the density-of-state function of holes in the n^+ region. The oscillation-like features for the high negative V_G are the results of a slightly complicated mechanism. It should be noted that holes have already shared subband-level sites predominantly in the n^+ region.

Since the hole concentration is controlled by both the pn product and the charge neutrality in the thin SOI system, the increase rate of the holes is incidentally affected by the decrease rate of the electron density, especially in the n^+ region. In other words, hole injection into the n^+ region strongly reflects the electron density-of-state function – meaning a change of injection mechanism.

The aforementioned oscillation feature in g_m characteristics is found during the change of the injection mechanism. This is why the g_m curves have such complicated features. Nevertheless, these features still seem to differ from the experimental results. The origin of this difference is discussed later.

As already described, the simulated results shown in Figure 10.6(a) still seem to differ from the experiments. Since the top surface of the buried oxide layer has a rugged square-mosaic morphology in practical devices, as shown in Figure 10.7, and the top surface of the superficial silicon layer is rather smooth [9], the influence of the silicon layer thickness modulation must be considered. Figure 10.7 shows that the gate electrode widely covers the square morphology across the gate width, so the simple step model, one of the previously proposed geometrical models [7], is used here.

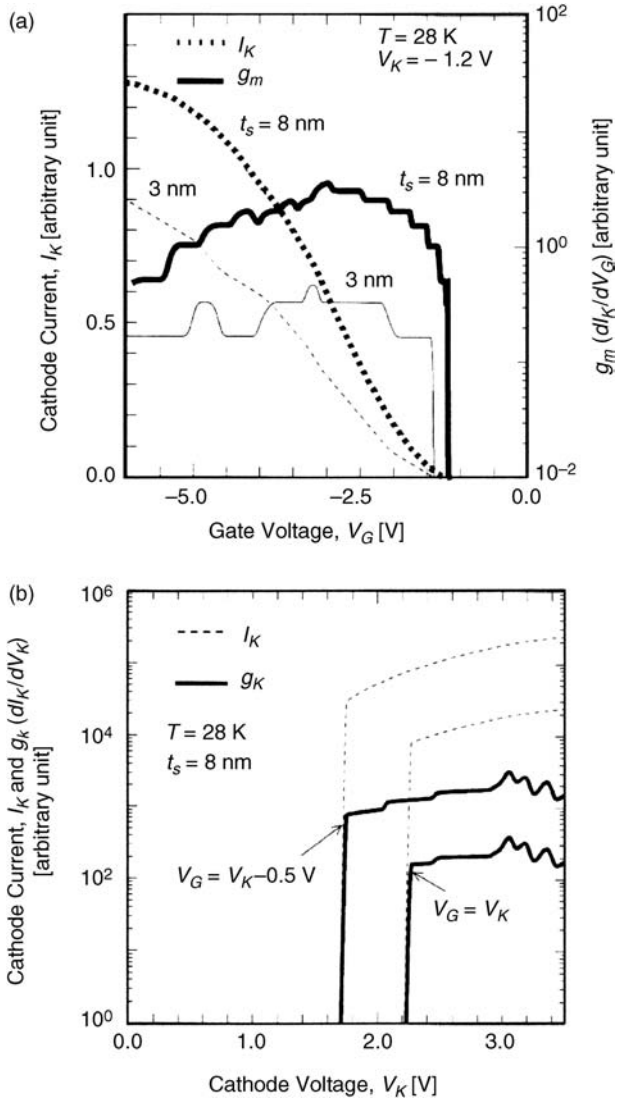

Figure 10.6 Simulated characteristic curves at low temperature. Absolute values are plotted for g_m and g_A values. (a) I_A and g_m dependence on V_G for two different silicon layer thicknesses. (b) I_A and g_A dependence on V_c for two different gate biases. © 1996 IEEE. Reprinted, with permission, from Y. Omura, Two-dimensionally confined injection phenomena at low temperatures in sub-10-nm-thick SOI insulated-gate p-n-junction devices, *IEEE Transactions on Electron Devices*, vol. 43, pp. 436–443, 1996.

Simulated I_K and g_m dependences on V_G for the anode common configuration are shown in Figure 10.8 for two different nominal silicon layer thicknesses. Here, it is also assumed that $n = 1$. Step-like features in the simulated g_m curves are modified and strong oscillation-like features can be seen. Since the features of the simulated g_m curves are very similar to those in

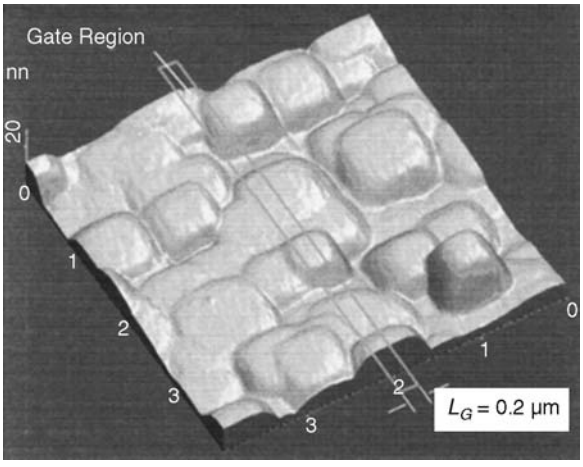

Figure 10.7 Surface morphology of the buried oxide layer. The image was observed by atomic force microscopy (AFM). Horizontal scale: 1 μm/division. Vertical scale: 20 nm/division. © 1996 IEEE. Reprinted, with permission, from Y. Omura, Two-dimensionally confined injection phenomena at low temperatures in sub-10-nm-thick SOI insulated-gate p-n-junction devices, *IEEE Transactions on Electron Devices*, vol. 43, pp. 436–443, 1996.

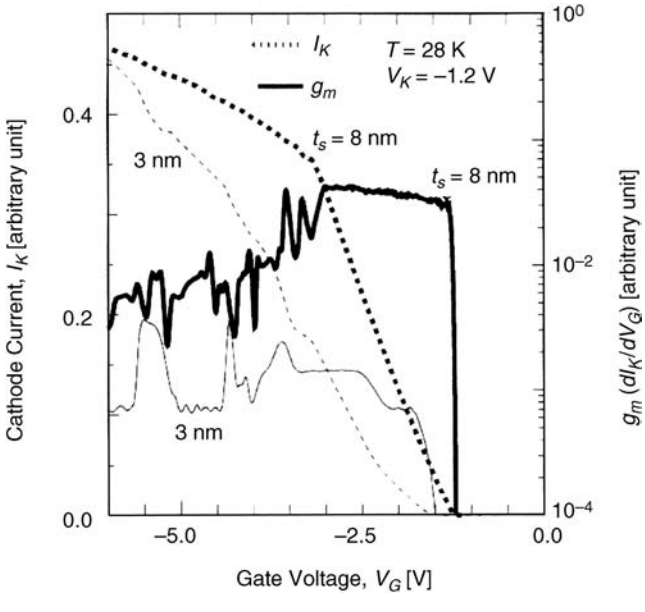

Figure 10.8 Simulated I_K and g_m dependence on V_G for two different nominal silicon layer thicknesses. Absolute values are plotted for g_m values. © 1996 IEEE. Reprinted, with permission, from Y. Omura, Two-dimensionally confined injection phenomena at low temperatures in sub-10-nm-thick SOI insulated-gate p-n-junction devices, *IEEE Transactions on Electron Devices*, vol. 43, pp. 436–443, 1996.

Figure 10.2, the experimental results can be interpreted as the modified appearance of quantum mechanical effects. If we assume $n > 1$, the simulation results can reflect a more realistic behavior. On the other hand, it is still unclear why the I_K and g_K dependences on V_K in Figure 10.6(b) are not modified to any great extent by the surface morphology of the buried oxide layer.

However, it can be strongly suggested that the simultaneous sweep of the front and back gate voltages with the cathode voltage (V_K) must play an important role. Here, the influence of interface properties of the buried oxide layer on the characteristics is not discussed because both the fixed oxide charge density (N_f) and the interface state density (D_{it}) of the layer, which were evaluated by MOSFETs on the same wafer, are much smaller than either electron or hole density in the bias range discussed here. N_f was evaluated from the front-gate threshold voltage dependence on substrate voltage, and is about $5 \times 10^{10}\,\mathrm{cm}^{-2}$. D_{it} was evaluated from the subthreshold swing, and is about $1 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$.

10.3.3 Influences on Characteristics of Extremely Ultra-Thin SOI MOSFET Devices

Parasitic bipolar action (PBA) is the most important influence on ultra-thin SOI MOSFETs. PBA is based on the double injection at the source junction. When the thin SOI layer is two-dimensionally quantized, the effective density of states decreases [5].

Furthermore, owing to the quantization, the transport property of either type of carrier is affected by the other through the pn product. For ultra-thin SOI MOSFETs with a sub-10-nm-thick SOI layer, even at room temperature, the two physical mechanisms above lead to the suppression of carrier injection across the source junction, which results in the suppression of PBA.

Another effect will also assist the suppression of PBA. The two-dimensional quantization of the thin SOI layer leads to an increase in the effective bandgap, as shown in Equation (10A.7). This suppresses not only the carrier injection but also the impact ionization near the drain. Thus it can be expected that the breakdown voltage in extremely thin SOI MOSFET devices will be moderately improved.

10.4 Summary

This section has described two-dimensional confined effects on carrier injection phenomena in thin SOI Lubistors fabricated on SIMOX substrates. At 28 K the conductance shows step-like anomalies due to the manifestation of 2DSS in an 8-nm-thick SOI structure at a low gate bias. Conductance also shows an oscillation-like feature at a high gate bias owing to an injection mode change. These influences were examined fundamentally by theoretical simulations based on quantum mechanics. In practical devices, some influence was found from the surface morphology of the buried oxide layer. These effects were successfully simulated using existing geometrical models.

Appendix 10A: Intrinsic Carrier Concentration (n_{iq}) and the Fermi Level in 2DSS

The Fermi level must be reconsidered in a 2DSS such as an ultra-thin SOI system because the quantum mechanical concept of the effective bandgap (E_G^*) appears. In a thin SOI system it is considered that the subband energy levels are almost independent of the external electric

field [10]. Hence in such a simple case, electron concentration ($n(z)$) and hole concentration ($p(z)$) are

$$n(z) = D_{osn} k_B T \sum_{n=1}^{\infty} \chi_{nn}^2(z) \ln\left[1 + \exp\left(\frac{-E_F + E_{nn}}{k_B T}\right)\right] \tag{10A.1}$$

and

$$p(z) = D_{osp} k_B T \sum_{n=1}^{\infty} \chi_{pn}^2(z) \ln\left[1 + \exp\left(\frac{E_F - E_{pn}}{k_B T}\right)\right], \tag{10A.2}$$

where D_{osn} and D_{osp} are the electron density of state and the hole density of state, and $\chi_{nn}(z)$ and $\chi_{pn}(z)$ are the wave functions of the nth subband level for electrons and holes.

These are approximated by trigonometric functions. The z axis is normal to the top surface of the superficial silicon layer. E_F is the Fermi level, E_{nn} is the nth subband energy level for electrons, and E_{pn} is the nth subband energy level for holes. According to Figure 10.9, for $-E_F + E_{nn} < 0$ and $E_F - E_{pn} < 0$, most of the electrons share the lowest level E_{n1} and most of the holes share the lowest level E_{p1}. Thus Equations (10A.1) and (10A.2) are rewritten approximately as

$$n(z) = D_{osn} k_B T \chi_{n1}^2(z) \ln\left[1 + \exp\left(\frac{-E_F - E_{n1}}{k_B T}\right)\right] \tag{10A.3}$$

and

$$p(z) = D_{osp} k_B T \chi_{p1}^2(z) \ln\left[1 + \exp\left(\frac{E_F - E_{p1}}{k_B T}\right)\right]. \tag{10A.4}$$

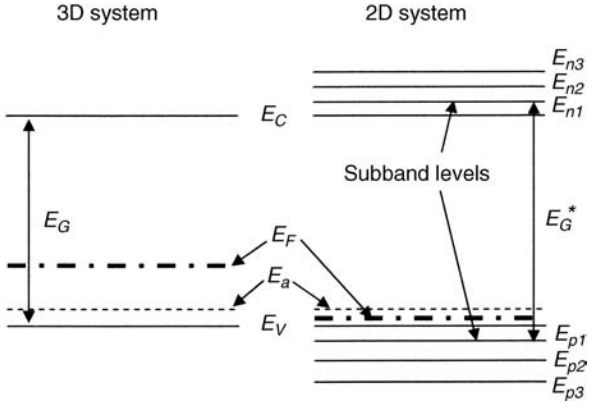

Figure 10.9 Schematic band diagram of the two-dimensional subband system in a thin SOI structure compared with the three-dimensional system. © 1996 IEEE. Reprinted, with permission, from Y. Omura, Two-dimensionally confined injection phenomena at low temperatures in sub-10-nm-thick SOI insulated-gate p-n-junction devices, *IEEE Transactions on Electron Devices*, vol. 43, pp. 436–443, 1996.

Since the pn product must hold its meaning even in a quantum mechanical system,

$$p(z)n(z) = n_{iq}^2, \tag{10A.5}$$

where n_{iq} is the intrinsic carrier concentration. Since the SOI layer is very thin, it is considered that the averaged values for the pn product over the entire SOI layer are acceptable for this discussion. In the practical calculation the following mathematical manipulation is applied:

$$\begin{aligned} \frac{1}{t_S}\int_0^{t_S} \chi_{n1}^2(z)\chi_{p1}^2(z)dz &= \frac{1}{t_S}\int_0^{t_S} \sin^2\left(\frac{\pi z}{t_S}\right)\sin^2\left(\frac{\pi z}{t_S}\right)dz \\ &= \frac{3}{8} \\ &\sim 1, \end{aligned} \tag{10A.6}$$

where an infinite barrier height is assumed. Furthermore, the following series expansion for the logarithmic function is employed:

$$\log(1+x) \cong x - \frac{x^2}{2} + \frac{x^3}{3}. \tag{10A.7}$$

Thus from Equations (10A.3) to (10A.7), n_{iq} is approximately derived as

$$n_{iq} = \frac{k_B T\sqrt{D_{osn}D_{osp}}}{t_S}\exp\left(\frac{-E_G^*}{2k_BT}\right), \tag{10A.8}$$

$$E_G^* = E_{n1} - E_{p1}, \tag{10A.9}$$

where E_G^* is the effective bandgap in the 2DSS. Next, the Fermi level at the thermal equilibrium must be considered. For a p-type body region, the following condition is used in order to determine the Fermi level:

$$\frac{N_A t_S}{1 + g\exp\left(\dfrac{E_F - E_a}{k_BT}\right)} = D_{osp}k_BT\exp\left(\frac{-E_{p1} + E_F}{k_BT}\right), \tag{10A.10}$$

where g is the degeneracy, E_a is the impurity energy level for the acceptor, and N_A is the acceptor doping concentration. As $(E_{p1} - E_a)/k_BT \gg 1$, from Equation (10A.10) the Fermi level is derived as

$$E_F = \frac{E_{p1} + E_a}{2} + \frac{k_BT}{2}\ln\left(\frac{N_A t_S}{qD_{osp}k_BT}\right). \tag{10A.11}$$

The Fermi level of the n^+ region is similarly derived.

Appendix 10B: Calculation of Electron and Hole Densities in 2DSS

In the thin SOI system the entire charge neutrality must be taken into account for device operation. The Poisson equation for the 2DSS is

$$\frac{d^2\phi(z)}{dz^2} = -\frac{q}{\epsilon_S}[p(V_G) - n(V_G)], \tag{10B.1}$$

where $\phi(z)$ is the potential in the thin SOI region and ε_s is the dielectric constant of silicon. Concrete expressions for $p(V_G)$ and $n(V_G)$ are given by Equations (10A.1) and (10A.2). Since the practical device has a metal–insulator–semiconductor–insulator–semiconductor (MISIS) structure, the potential and electric field boundary conditions at the superficial silicon layer/buried oxide layer interface are given so as to reflect the back gate bias effect. Therefore, either one of the carrier densities is affected by the other through the Poisson equation and the pn product.

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11

Two-Dimensional Quantization Effect on Indirect Tunneling in SOI Lubistors with a Thin Silicon Layer

11.1 Introduction

In the 1990s, we have been able to realize a silicon oxide/silicon/silicon oxide structure with a sub-10-nm-thick monocrystalline silicon layer using silicon device technology [1–3]. Recent technological progress has also made it possible to form a silicon wire with a one-dimensional transport nature [4] and a single-electron transistor [5] and to clarify their physics [6].

I recently fabricated Lubistors with a 10- or 90-nm-thick monocrystalline silicon layer on an insulator [7] using an SOI material with a long minority carrier lifetime, and, in a brief letter, reported that clear negative conductance was observed at temperatures below 100 K [8]. The experimental results suggested qualitatively that two-dimensional carriers play an essential role in high-temperature observation. This temperature range is very high considering past data [9,10]. Negative conductance was recently observed at 300 K in a surface-planar structure made of SOI substrate [11]. In the case of direct gap semiconductors, it has already been observed at room temperature [12].

Indirect tunneling in semiconductors such as silicon requires an additional energy for band-to-band transition. It is considered that such additional energy is usually supplied by optical phonons. In low-dimensional systems made from indirect bandgap semiconductors, this point has not been examined adequately. The tunneling process has already been studied using the silicon MOSFET [13]. Since, in that configuration, tunneling occurs in the direction perpendicular to the silicon oxide/silicon interface of the MOS structure, where carriers are two-dimensionally quantized, a very simple situation can be assumed. In the case of lateral tunneling between the two-dimensionally quantized electron inversion layer and the p^+ layer, however, the relationship between the Fermi potential controlled by the gate voltage and the p^+ (anode) voltage becomes complicated. Therefore, experimental results must be analyzed carefully.

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

In recent experiments using direct and indirect bandgap semiconductors, two-dimensional-system-to-three-dimensional-system (2D-to-3D) [13], one-dimensional-system-to-two-dimensional-system (1D-to-2D) [14], and one-dimensional-system-to-three-dimensional-system (1D-to-3D) [15] transitions have been observed. The discussion in those works is concerned with the spectroscopic study of band structure or momentum conservation. These studies consider tunneling normal to the confined plane. The density of electronic states for conserving momentum is not so restricted because the momentum conserved is parallel to the confined plane [13] or the confined wire [14,15]. However, in a pn junction formed laterally in a thin film, tunneling occurs parallel to the confined plane [8]. The density of electronic states to conserve momentum will be lower than in the former cases. The tunneling spectra should be weak and depend strongly on the subband structure.

This chapter discusses the significant features of tunneling and negative conductance in a Lubistor structure with a two-dimensionally quantized thin silicon layer. The tunneling mechanism and the indirect tunneling process in an extremely thin film system are also discussed based on experimental results and theoretical formulations.

11.2 Experimental Results

11.2.1 Junction Current Dependence on Anode Voltage

The schematic device structure is shown in Figure 11.1(a). The device has a gate electrode/silicon oxide layer (gate oxide layer)/silicon layer/silicon oxide layer (buried oxide layer)/silicon substrate composite structure in the vertical direction and an n^+–p^-–p^+ structure in the horizontal direction. The device is fabricated on a (100) Si surface and the n^+–p^-–p^+ structure lies along the ⟨100⟩ direction. The gate oxide layer is 5.0 nm thick and the buried oxide layer is 110 nm thick. The middle silicon layer, which is monocrystalline in nature, is 10 nm or 90 nm thick. These physical parameters were measured by an optical interference technique and cross-sectional transmission electron microspectroscopy (XTEM). The doping concentration (N_A) in the p^- region is about $1 \times 10^{16}\,\mathrm{cm}^{-3}$.

The measurement configuration is shown in Figure 11.1(b). Measurements were carried out at temperatures ranging from 35 K to 300 K. The anode current (I_A) dependence on anode voltage (V_A) at 43 K is shown for the device with a 10-nm-thick silicon layer in Figure 11.2. The gate length (L_G) is 3 μm and the gate width (W_G) is 10 μm. When the gate voltage (V_G) ranges from 2.2 V to 2.6 V, clear negative conductance is detected at V_A of around 0.7 V. It should be noted that two-dimensional-system-to-two-dimensional-system (2D-to-2D) tunneling occurs in this device because the pn junction is formed adjacent to the edges of the two-dimensionally-confined p-type and n-type silicon layers. Negative conductance is not detected at V_G lower than 2.1 V or higher than 2.8 V. At V_G of 2 V, the electron concentration of the inversion layer ($>1 \times 10^{19}\,\mathrm{cm}^{-3}$) is sufficiently high to induce tunneling. Nevertheless, negative conductance is not clearly observed. This results from the still thick tunneling barrier, which becomes thinner as the gate-induced electric field increases because the inversion layer expands laterally toward the p^+ region. At a V_G of 3 V, however, the situation is different. One possible reason for this is that the surface of the gate overlapping the anode region is depleted partially by the high positive V_G, as shown in Figure 11.2, and most of the junction current flows near the silicon layer/buried oxide layer interface. Because the electron concentration in this region is lower than that at the upper surface of the silicon layer, tunneling is suppressed. When a more abrupt p^+n junction

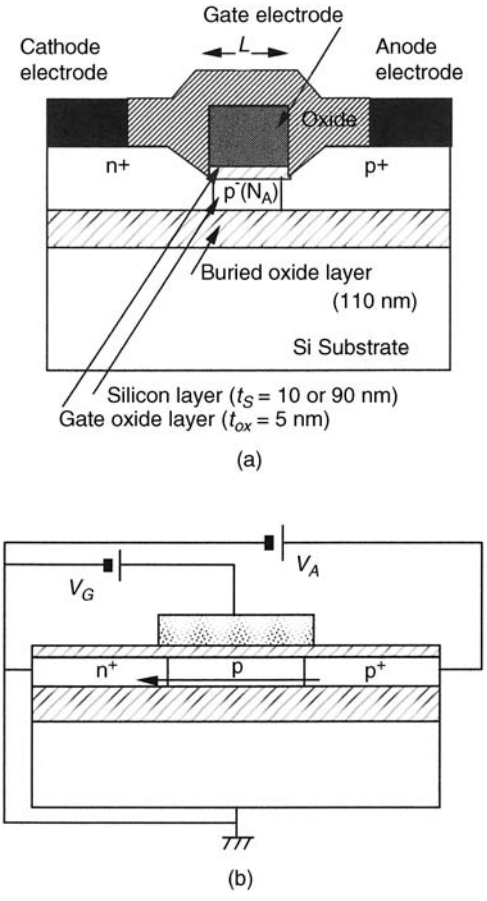

Figure 11.1 Device structure and measurement configuration. (a) Schematic cross-section of Lubistor. (b) Measurement configuration. The device was fabricated on a (100) surface. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-Dimensional Quantization Effect in Indirect Tunneling in an Insulated-Gate Lateral pn-Junction Structure with a Thin Silicon Layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

with a higher doped p^+ region is formed, the problem can be overcome [11], because it is anticipated that reducing the silicon layer's thickness suppresses the internal potential difference between the top and bottom interfaces of the silicon layer and that the almost uniform high-density electrons yield a large negative conductance.

In the Esaki diode with a three-dimensional structure [16,17], the applied voltage at which negative conductance is detected is entirely consumed by the interaction with optical phonons because the built-in electric field is very high in the implemented impurity density profile. On the other hand, in planar devices, the gate voltage controls the electron density and the potential in the inversion layer; the potential profile across the pn junction is not easily deduced.

As seen in Figure 11.2, the anode voltage at which negative conductance is detected is slightly higher than that in bulk planar-type tunneling devices [11]. In extremely thin silicon

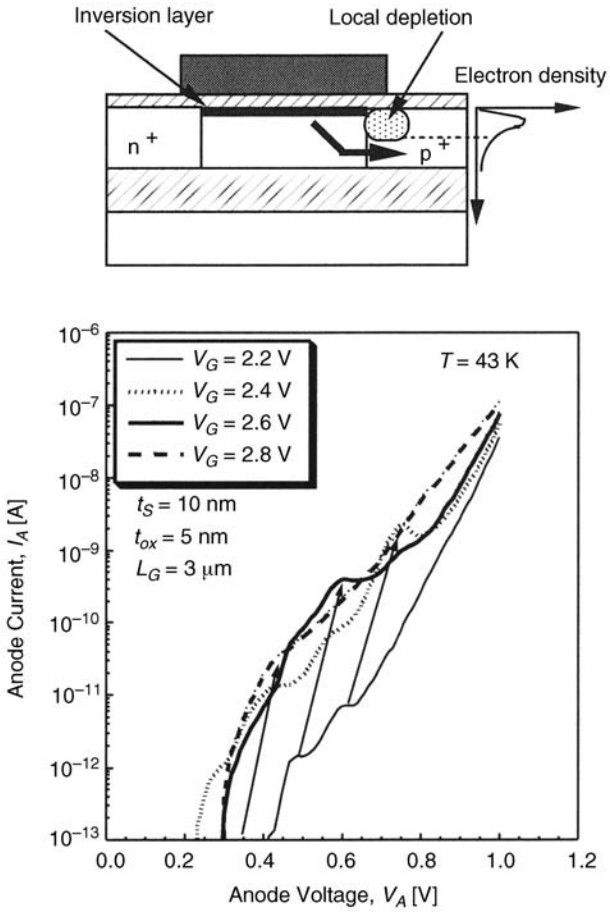

Figure 11.2 Anode current (I_A) dependence on anode voltage (V_A) at 43 K for three different gate voltages (V_G). The silicon layer is 10 nm thick. A schematic of the setup used during operation at V_G of 2.8 V is shown above. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-Dimensional Quantization Effect in Indirect Tunneling in an Insulated-Gate Lateral pn-Junction Structure with a Thin Silicon Layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

layer devices, the potential difference between the upper and lower surfaces of the silicon layer is very small. This confinement of electrons raises the body potential of the whole silicon layer owing to capacitance coupling [7,18]. Consequently, this raises the anode voltage to satisfy the tunneling condition, which is an important feature of extremely thin silicon layer devices. In the present wafer, there exists a local fluctuation of silicon layer thickness. However, it is confirmed that such a local difference in silicon layer thickness does not seriously influence the negative conductance property.

Negative conductance was also detected at a V_G of 3 V in the device with a 90-nm-thick silicon layer, as shown in Figure 11.3. In this case, it appears that two-dimensional-system-to-three-dimensional-system (2D-to-3D) tunneling occurs due to the thick p^+ region, which is hardly confined electrically at all, acting as a three-dimensional system, in contrast to the

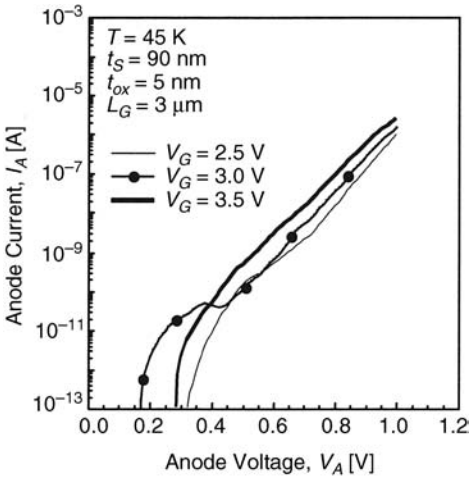

Figure 11.3 Anode current (I_A) dependence on anode voltage (V_A) at 45 K for three different gate voltages (V_G). The silicon layer is 90 nm thick. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-Dimensional Quantization Effect in Indirect Tunneling in an Insulated-Gate Lateral pn-Junction Structure with a Thin Silicon Layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

case shown in Figure 11.2. However, this configuration leads to an interesting conclusion, as discussed later. The gate voltage at which negative conductance was detected was higher than that for the device with the 10-nm-thick silicon layer, as shown in Figure 11.3. This is because the confinement of electrons under the gate becomes relatively loose in the thicker silicon layer device and a higher V_G is necessary to achieve the same electron density as that in the device for $t_s = 10$ nm. In the device with the 10-nm-thick silicon layer, the gate electrode-to-substrate capacitance coupling enhances the electron density in the silicon layer. For the device in Figure 11.3, it must be considered that local depletion occurs around the gate-overlapping anode region only at a high gate voltage. This is consistent with the result shown in Figure 11.2 for the 10-nm-thick silicon layer device because the negative conductance disappears when the gate voltage becomes high. However, detailed analyses are required to explain fully the difference between the device characteristics shown in Figures 11.2 and 11.3.

On the other hand, the anode voltage at which negative conductance was detected in the device with the 90-nm-thick silicon layer was lower than that for $t_s = 10$ nm. In thicker silicon layer devices, the potential difference between the upper and lower surfaces of the silicon layer naturally becomes large and a sufficient body potential shift over the whole silicon layer is not realized. Thus, the anode bias at which negative conductance occurs does not easily increase. In other words, it can be anticipated that the mechanism of the negative conductance would resemble that seen in devices without a narrow square potential well [11].

Since temperature dependence of the negative conductance ($=dI_A/dV_A$) has already been described in a previous paper [8], details are not discussed here.

11.2.2 Junction Current Dependence on Gate Voltage

The experimental junction current dependences on gate voltage are shown with anode voltage as a parameter in Figure 11.4 for $t_s = 10$ nm. The anode current (I_A) characteristics show many Λ-shaped anomalies corresponding to negative transconductances ($dI_A/dV_G < 0$). The evolution of Λ-shaped anomalies with V_A in the current curves suggests that the anode voltage slightly affects the body potential near the anode because current curves shift slightly toward the lower gate voltage side. As mentioned previously, there exists a local fluctuation of silicon layer thickness in the wafer. However, it is also confirmed that such a local difference in silicon layer thickness does not seriously influence the feature of junction current except for the threshold voltage in the MOS structure.

As shown in Figure 11.4, at gate voltages where negative conductance occurs, salient increases in the anode current (I_A) are found ('→' in the figure). This abnormal increase in the junction current suggests that a tunneling channel has opened across the junction, as discussed below. We must also note two points: one is that the junction current slope in the low gate voltage region is very steep for low anode voltages and the other is that the junction current increases exponentially as a function of the gate voltage for high anode voltages. The latter means that a high anode voltage results in an increase in the direct injection current across the junction.

The Λ-shaped anomalies in Figure 11.4 hold their fine structures even at 100 K, as shown in Figure 11.5, where junction current dependence on gate voltage is shown with temperature as the parameter for $t_s = 10$ nm. This suggests that the energy level difference between corresponding subband ladders is larger than k_BT (∼8 meV at 100 K).

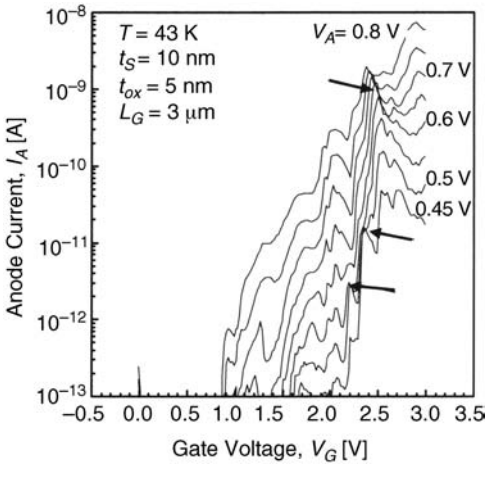

Figure 11.4 Anode current (I_A) dependence on gate voltage (V_G) at 43 K for various anode voltages in the device with the 10-nm-thick silicon layer. The arrow indicates the bias point at which negative conductance is observed. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-Dimensional Quantization Effect in Indirect Tunneling in an Insulated-Gate Lateral pn-Junction Structure with a Thin Silicon Layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

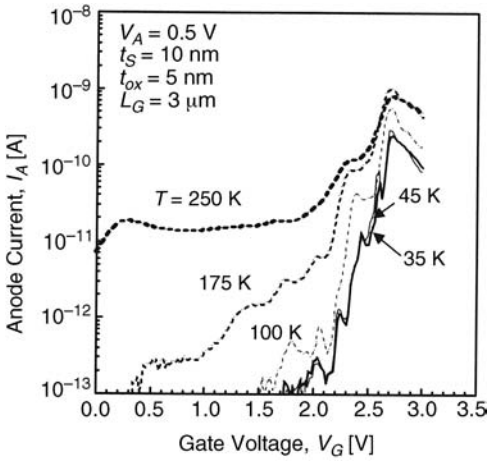

Figure 11.5 Anode current (I_A) dependence on gate voltage (V_G) for various temperatures in the device with the 10-nm-thick silicon layer. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-Dimensional Quantization Effect in Indirect Tunneling in an Insulated-Gate Lateral pn-Junction Structure with a Thin Silicon Layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

On the other hand, the experimental junction current dependences on gate voltage is shown with anode voltage as the parameter in Figure 11.6 for $t_s = 90\,\text{nm}$. The junction current characteristics do not show distinctive Λ-shaped anomalies. Thus, it is apparent that the transport mechanisms are different from those for $t_s = 10\,\text{nm}$. However, we must carefully

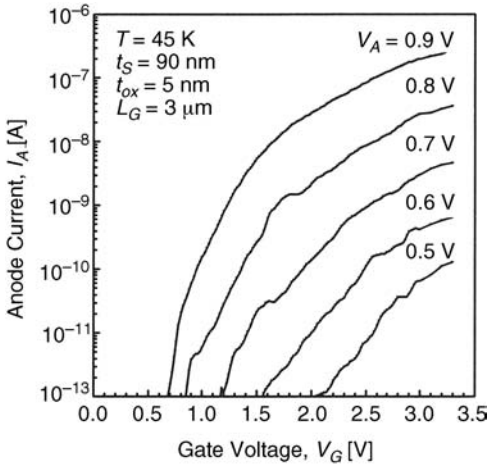

Figure 11.6 Anode current (I_A) dependence on gate voltage (V_G) at 45 K for various anode voltages in the device with the 90-nm-thick silicon layer. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-Dimensional Quantization Effect in Indirect Tunneling in an Insulated-Gate Lateral pn-Junction Structure with a Thin Silicon Layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

consider the characteristics because two-dimensional quantization of carriers near the upper surface must be reflected in the transport characteristics. Unfortunately, in the case of $t_s = 90\,\text{nm}$, a large direct-injection current readily flows across the junction in the bottom region of the silicon layer. Thus, fine structures in the junction current may be diminished.

As shown in Figure 11.3, the *single negative conductance* is observed in the device with a 90-nm-thick silicon layer and is clearly different from the features in Figure 11.2. Since the surface electrons in the inversion layer are two-dimensionally quantized and holes in the thick p^+ anode region are not, it can be considered that a two-dimensional-system-to-three-dimensional-system (2D-to-3D) tunneling system is formed in the case of $t_s = 90\,\text{nm}$. Therefore, the mechanism of the *single negative conductance* for $t_s = 90\,\text{nm}$ is probably different from that of the *multi-negative conductanc*e property for $t_s = 10\,\text{nm}$.

11.3 Theoretical Discussion

11.3.1 Qualitative Consideration of the Low-Dimensional Indirect Tunneling Process

Here, at first, we discuss very roughly the nature of the tunneling process in lateral pn-junction devices before introducing a theoretical formulation; that is, the following theoretical expression of junction current does not include the conventional diffusion current with the recombination. The coordinate configuration of the device fabricated on the (100) surface and band diagrams for two-dimensional-system-to-two-dimensional-system (2D-to-2D) and two-dimensional-system-to-three-dimensional-system (2D-to-3D) tunneling processes are shown in Figure 11.7, although only one subband system for heavy holes is drawn for simplicity. For the two-dimensional-system-to-two-dimensional-system (2D-to-2D) tunneling process (Figure 11.7(a)), as an example, we consider the case in which an electron with a certain Fermi wave vector $\boldsymbol{k_F}(k_{i,x}, k_{i,y})$ in the X valley tunnels to an empty state in the Γ valley for holes. The wave number component $k_{i,x}$ of the pre-tunneling electron, which is parallel to the surface, must be conserved, although $k_{i,y}$ along the tunneling is not. Since the transition requires scattering with phonons, post-tunneling electrons with the component $k_{f,y}$ must receive additional momentum and energy from the phonons.

On the other hand, in the case of two-dimensional-system-to-three-dimensional-system (2D-to-3D) tunneling (Figure 11.7(b)), its difference from two-dimensional-system-to-two-dimensional-system (2D-to-2D) tunneling is whether post-tunneling electrons can select the component $k_{f,z}$ in a wide range during the phonon-assisted tunneling process as well as the component $k_{f,y}$. Actually, as discussed in detail below, there exists no possible value of $k_{f,z}$ except for the value of zero (as discussed in Appendix 11A) owing to the substantial difference between the wave functions of both sides. This means that tunneling is very limited in such a system.

11.3.2 Theoretical Formulations of Tunneling Current and Discussion

The probability (P) for a transition between the two states of the two systems on each side of the tunneling barrier is given by Fermi's golden rule:

$$P = \left(\frac{2\pi}{\hbar}\right) \sum_{m,n} \sum_{k_i,k_f} |M_{i\to f}|^2 \{f(E_i) - f(E_f)\} \delta(E_f - E_i - eV_A), \tag{11.1}$$

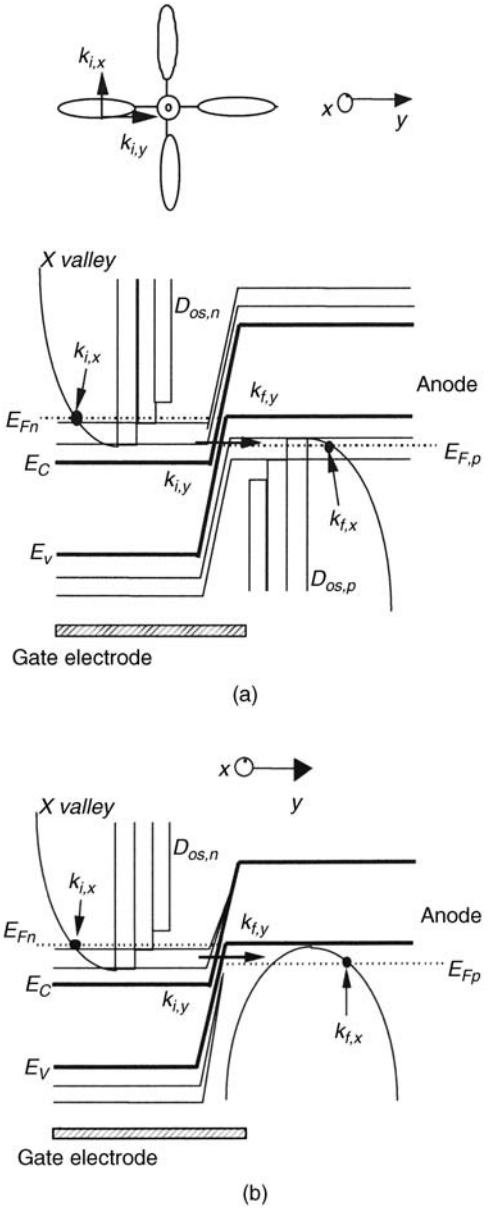

Figure 11.7 Schematic band diagram of forward-biased insulated-gate pn-junction device when tunneling occurs. The tunneling current flows along the y axis and surface quantization manifests itself along the z axis. $D_{OS,n}$ and $D_{OS,p}$ are the densities of states for electrons and holes, respectively. Here, only one subband system for heavy holes is drawn for simplicity. E_{Fn} and E_{Fp} are the Fermi levels for electrons and holes, respectively. E_c and E_v are the conduction band bottom and the valence band top, respectively. (a) 2D-to-2D tunnelling, (b) 2D-to-3D tunneling. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-Dimensional Quantization Effect in Indirect Tunneling in an Insulated-Gate Lateral pn-Junction Structure with a Thin Silicon Layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

where subscripts '*i*' and '*f*' mean *initial* and *final*, $f(E)$ is the Fermi–Dirac function, $\hbar$ is Planck's constant, and the δ function represents the conservation of the total energy assuming that the applied bias voltage V_A drops partially across the barrier [19]. The matrix element $M_{i\to f}$ can be written in terms of the current density operator [20] based on the effective mass approximation such that

$$M_{i\to f} = \left(-\frac{\hbar^2}{2m^*}\right)\left\{\psi_f^* \frac{\partial \psi_i}{\partial y} - \psi_i \frac{\partial \psi_f^*}{\partial y}\right\}\delta(k_{f,x} - k_{i,x})\left\langle \phi_f | \phi_i \right\rangle_z, \tag{11.2}$$

where it is assumed that the tunneling current flows in the y direction and two-dimensional electrons are quantized in the z direction; $\psi_i(y)$, $\psi_f(y)$, $\phi_i(z)$ and $\phi_f(z)$ are the components of wave functions in the specific direction. In the following description, '*i*' stands for the electron system and '*f*' for the hole system.

11.3.2.1 Two-Dimensional-System-to-Two-Dimensional-System Tunneling

In the two-dimensional-to-two-dimensional-system (2D-to-2D) tunneling process, $\langle \phi_f | \phi_i \rangle_z$ has a finite value only for the same quantum number on both sides because wave functions are identical, which means a *resonance effect* [14]. In this condition, incident electrons can tunnel to the anode region after their interaction with phonons. This is the significant feature in such a lateral two-dimensional-system-to-two-dimensional-system (2D-to-2D) tunneling process. When a plane waveform in the tunneling direction is assumed, we have

$$|M_{i\to f}|^2 = \left(\frac{\hbar^2}{2m_y^*}\right)^2 \left(k_{i,y} + k_{f,y}\right)^2 \delta(k_{f,x} - k_{i,x}) \tag{11.3}$$

and, consequently, the tunneling current density $J_{2D\text{-}2D}$ is given by

$$\begin{aligned} J_{2D-2D} = &\left(\frac{\pi e \hbar^3}{m_y^{*2}}\right) \sum_{n=m} \sum_{k_i, k_f} \left\{f_f(E_{f2D}) - f_i(E_{i2D})\right\} \\ &\times (k_{i,y} + k_{f,y}) \delta(k_{f,x} - k_{i,x}) \delta(E_{f2D} - E_{i2D} - eV_A). \end{aligned} \tag{11.4}$$

The summation on k_i and k_f is replaced with energy integrals that include the one-dimensional density-of-state functions, $D_{OS(1D)}$, $n(E_{i2D})$ for electrons and $D_{OS(1D)}$, $p(E_{f2D})$ for holes, because the integrals with $k_{i,z}$ and $k_{f,z}$ are absorbed into the summation $\Sigma_{n=m}$. Here we consider only one subband system for electrons and holes for simplicity. This yields

$$\begin{aligned} J_{2D-2D} = &\left(\frac{e\hbar^3}{\pi m_y^{*2}}\right) \sum_{n=m} \iint D_{OS(1D),n}(E_{i2D}) D_{OS(1D),p}(E_{f2D}) dE_{i2D} dE_{f2D} \left\{f_f(E_{f2D}) - f_i(E_{i2D})\right\} \\ &\times \delta(k_{f,x} - k_{i,x}) \times \iint dk_{i,y} dk_{f,y} (k_{i,y} + k_{f,y}) \delta(E_{f2D} - E_{i2D} - eV_A), \end{aligned} \tag{11.5}$$

$$D_{OS(1D),n}(E_{i2D}) = \frac{D_{OS(1D),n0}}{(E_{i2D} - E_{zn,m})^{1/2}}, \tag{11.6a}$$

$$D_{OS(1D),p}(E_{f2D}) = \frac{D_{OS(1D),p0}}{(E_{zp,m} - E_{f2D})^{1/2}}, \tag{11.6b}$$

where $D_{OS(1D),n0}$ and $D_{OS(1D),p0}$ are one-dimensional densities of states for electrons and holes, respectively, and $E_{zn,m}$ and $E_{zp,m}$ are the mth subband energies for two-dimensional electrons and two-dimensional holes, respectively. The energy integrals are carried out in the transverse direction. The integrations should be done numerically at finite temperatures. Here, however, we approximate the integrals to discuss the major features at very low temperatures. We find that the δ function reduces the integral and that $k_{i,y} < k_{Fn}$ and $k_{f,y} < k_{Fp}$. In addition, we must take into account the energy conservation. Finally, we have

$$J_{2D-2D} = J_0 \sum_m \left[\left\{ 3(E_{Fn} - E_{zn,m}) + eV_A \right\} \left\{ (E_{Fn} - E_{zn,m})^{1/2} - (E_{Fn} - E_{zn,m} - eV_A)^{1/2} \right\} \right. \\ \left. - \left\{ (E_{Fn} - E_{zn,m})^{3/2} - (E_{Fn} - E_{zn,m} - eV_A)^{3/2} \right\} \right], \tag{11.7a}$$

$$J_0 = e\frac{\sqrt{2m_x^*}}{2\pi h^2}, \tag{11.7b}$$

where it is assumed that carrier masses in both initial and final states are identical. E_{Fn} is the Fermi levels for electrons and m_x^* is the electron effective mass in the x direction that is parallel to the oxide/silicon interface and perpendicular to the tunneling direction. In Equation (11.7a), both the Fermi level and the subband energy levels in the p-type region are not included explicitly because the summation of the initial and final states of possible transitions eliminates them; the anode bias (V_A) includes the effect of the Fermi level in the p-type region and the effect of the subband energy levels in the p-type region is reflected on the summation by the subscript m in Equation (11.7a). Tunneling current characteristics can be calculated using the above expression.

Simulation results of the tunneling current component dependence on the anode voltage are shown in Figure 11.8 for $T = 43$ K. Theoretical curves show multi-negative conductance properties with the Λ-shape for various gate voltages. This feature basically coincides with that of experimental results, although experimental results include a direct injection current component. Simulation results indicate that the anode voltage at a current peak slightly increases with the gate voltage. Gate-voltage-induced evolution of the junction current is shown in Figure 11.2 ('$\rightarrow$' in the figure), where the anode voltage at a current peak slightly increases with the gate voltage. Therefore, the theoretical behavior of the tunneling current component shown in Figure 11.8 explains the experimental results. Simulation results of the tunneling current component dependence on the anode voltage are shown in Figure 11.9 for various temperatures. Theoretical curves indicate that temperature is not sensitive to the negative conductance, in contrast to what might be expected. Instead, as described in the previous section, the Λ-shape of negative conductance is diminished as the temperature is increased. It can be considered that the Λ-shape diminishes in the experimental results because actual experimental results include a large direct injection current component, which increases with temperature.

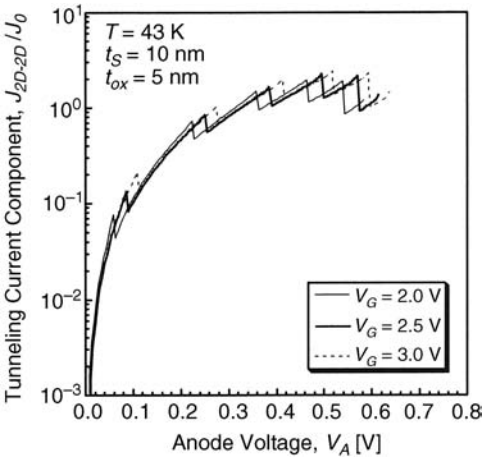

Figure 11.8 Tunneling current component dependence on anode voltage for $T = 43$ K in the device with t_s of 10 nm (simulation results). It is assumed that the surface threshold voltage is 1.5 V, which is measured by using a MOS transistor on the same chip. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-Dimensional Quantization Effect in Indirect Tunneling in an Insulated-Gate Lateral pn-Junction Structure with a Thin Silicon Layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

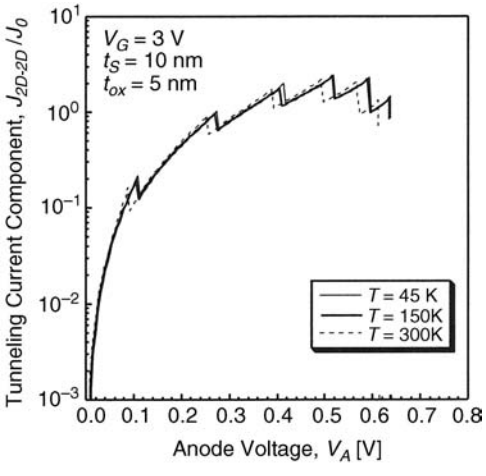

Figure 11.9 Tunneling current component dependence on anode voltage for various temperatures in the device with t_s of 10 nm (simulation results). It is assumed that the surface threshold voltage is 1.5 V and is independent of temperature for simplicity. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-Dimensional Quantization Effect in Indirect Tunneling in an Insulated-Gate Lateral pn-Junction Structure with a Thin Silicon Layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

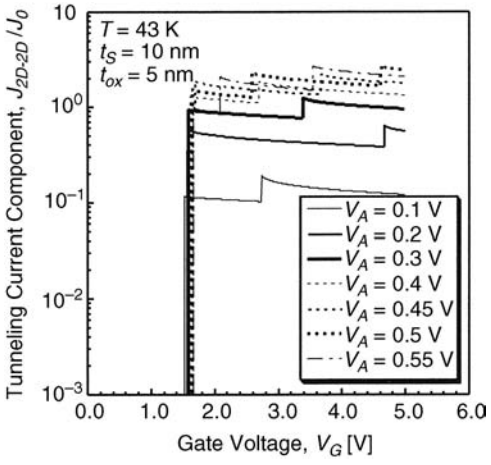

Figure 11.10 Tunneling current component dependence on gate voltage for $T = 43$ K in the device with t_s of 10 nm (simulation results). It is assumed that the surface threshold voltage is 1.5 V. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-Dimensional Quantization Effect in Indirect Tunneling in an Insulated-Gate Lateral pn-Junction Structure with a Thin Silicon Layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

Simulation results of the tunneling current component dependence on the gate voltage are shown in Figure 11.10 for $T = 43$ K. Theoretical curves show multi-negative transconductance properties with the Λ-shape for various anode voltages. This feature basically coincides with that of experimental results, although experimental results include a large direct injection current component for high anode voltages. A pair of curves cross each other, resulting in the negative conductance ($dJ_{2D\text{-}2D}/dV_G < 0$), shown in Figure 11.9. This behavior of the tunneling current component also concurs with the experimental results shown in Figure 11.4. Simulation results of the tunneling current component dependence on the gate voltage are shown in Figure 11.11 for various temperatures. Theoretical curves indicate that the temperature is not so sensitive to the Λ-shape of negative transconductance, in contrast to simple expectation. Experimental results partially support the theoretical prediction for $T < 100$ K, as shown in Figure 11.5. Generally speaking, theoretical simulations are verified by the experimental results.

11.3.2.2 Two-Dimensional-System-to-Three-Dimensional-System Tunneling

In the apparent two-dimensional-system-to-three-dimensional-system (2D-to-3D) tunneling process, on the other hand, we must carefully examine the integral $\langle \phi_f | \phi_i \rangle_z$ owing to the substantial difference in the two wave functions. As a result, the integral $\langle \phi_f | \phi_i \rangle_z$ holds a meaningful value only for $k_{f,z} = 0$, which means that the tunneling is very limited (see Appendix 11A). Therefore, it can be expected that the two-dimensional-system-to-three-dimensional-system (2D-to-3D) tunneling mechanism mentioned in previous papers [13–15] is very different from that of the two-dimensional-system-to-two-dimensional-system (2D-to-2D) tunneling process. Detailed theoretical formulation is not shown here because only the

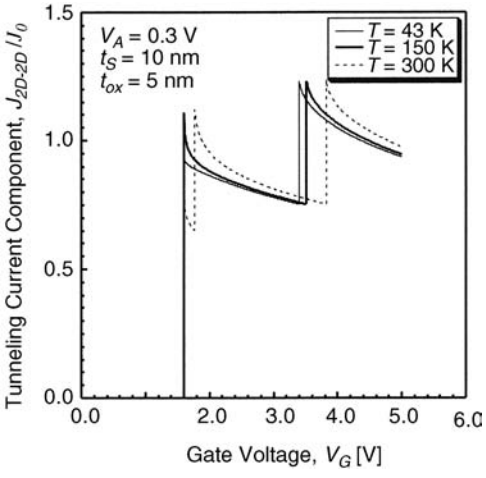

Figure 11.11 Tunneling current component dependence on gate voltage for various temperatures in the device with t_s of 10 nm (simulation results). It is assumed that the surface threshold voltage is 1.5 V and is independent of temperature for simplicity. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-Dimensional Quantization Effect in Indirect Tunneling in an Insulated-Gate Lateral pn-Junction Structure with a Thin Silicon Layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

two-dimensional-system-to-two-dimensional-system (2D-to-2D) tunneling process is focused on in this paper.

Comparing the magnitudes of the tunneling current components in Figures 11.2 and 11.3, we note that the theoretical prediction mentioned in Appendix 11A is reasonable; that is, the magnitude of the tunneling current component in Figure 11.3 ($t_s = 90$ nm) is two orders smaller than that in Figure 11.2 ($t_s = 10$ nm). Furthermore, it should be noted that only one clear case of negative conductance is observed in Figure 11.3 in contrast to Figure 11.2. This is due to the mechanism in which the wave number in the final state of transition is effectively limited to only one value ($k_{f,z} = 0$).

Finally, we would like to emphasize the above results. As shown in the figures, negative conductance is observed at anode voltages over ~0.5 V. This is considered to be a significant aspect of such surface-planar devices, because negative conductance is observed at anode voltages below ~0.2 V in bulk devices [16,21]. When we explore some device applications, a very low voltage supply is not preferred from the point of view of the dynamic range. Thus, surface-planar devices are more preferable than previous bulk devices.

11.4 Summary

A multi-negative conductance property was detected at low temperatures in a silicon-on-insulator insulated-gate pn-junction device with a 10-nm-thick mono-crystalline silicon layer fabricated on an insulator. Important aspects of the lateral low-dimensional tunneling process were examined and discussed using a theoretical formulation. A comparison of the characteristics of devices with a 10-nm-thick or a 90-nm-thick silicon layer indicates that the strong two-dimensional confinement effect plays an important role in multi-negative

conductance. The theory predicts that a resonance effect between two subband levels is significant for the multi-negative conductance in the tunneling of the device with the 10-nm-thick silicon layer.

Appendix 11A: Wave Function Coupling Effect in the Lateral Two-Dimensional-System-to-Three-Dimensional-System (2D-to-3D) Tunneling Process

Here, we examine the integral $\langle \phi_f | \phi_i \rangle_z$ for the lateral two-dimensional-system-to-two-dimensional-system (2D-to-3D) tunneling process. In the case of $t_s = 90$ nm, surface quantization is very similar to that in the bulk surface [22]. Therefore, it is reasonable to employ the conventional Stern trial wave function [23] for the lowest subband level as

$$\phi_i(z) = c_1 z \ \exp(-c_2 z/2), \tag{11A.1}$$

where c_1 and c_2 are parameters that depend on the gate-induced electric field. On the other hand, ϕ_f is given by

$$\phi_f(z) = c_3 \ \exp(-ik_{f,z} z), \tag{11A.2}$$

where c_3 is the normalized constant. Then the integral $\langle \phi_f | \phi_i \rangle_z$ is carried out in the following way. The transition probability of electrons is in proportion to the real part of the integral:

$$\begin{aligned} \langle \phi_f | \phi_i \rangle_z &= \mathrm{Re} \left[\int_0 c_1 c_3 z \ \exp(-ik_{f,z} z) \ \exp(-c_2 z/2) dz \right] \\ &= \mathrm{Re} \left[\frac{c_1 c_3}{c_2^2/4 + k_{f,z}^2} \ \exp(i2\theta) \right], \end{aligned} \tag{11A.3}$$

$$\exp(i2\theta) = \frac{c_2}{2\left(\frac{c_2^2}{4} + k_{f,z}^2\right)^{1/2}} + \frac{ik_{f,z}}{\left(\frac{c_2^2}{4} + k_{f,z}^2\right)^{1/2}}. \tag{11A.4}$$

The real part of the integral takes a maximum value at $k_{f,z} = 0$. This is true even for higher subband levels. Thus, two-dimensional-system-to-three-dimensional-system (2D-to-3D) tunneling in this configuration is, theoretically, very limited.

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12

Experimental Study of Two-Dimensional Confinement Effects on Reverse-Biased Current Characteristics of Ultra-Thin SOI Lubistors

12.1 Introduction

The author proposed the Lubistor for high-current device applications in 1982 [1]. It has recently been applied to electrostatic destroy (ESD) protection circuits [2,3]. Since the Lubistor has a pn junction, band-to-band tunneling across the junction and negative differential conductance were expected. Several articles reporting the negative differential conductance have already been published [4–8] and the fundamental mechanisms of negative differential conductance have been analyzed successfully [7,8]. Some people recently discussed the reverse-biased characteristics of the Lubistor at room temperature, focusing on fast switching device applications [9], where three-dimensional (3-D) transport was assumed. However, low-temperature transport characteristics of a reversed-biased ultra-thin film Lubistor have not been evaluated. The carrier confinement effect on the generation–recombination process attracts attention because it should suggest great merit of low-dimensional minority carrier injection.

In this chapter, the author discusses the results of experiments conducted on ultra-thin film Lubistors at low temperatures (down to 35 K) to evaluate the impact of two-dimensional (2-D) transport on the generation–recombination and tunnel phenomena.

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

12.2 Device Structures and Experimental Apparatus

A Lubistor with a lateral n^+–p–p^+ structure was fabricated on a (001) Si SIMOX wafer with a 110-nm buried oxide layer; it has a 5-nm-thick gate oxide layer and a 10-nm-thick Si layer [5]; the schematic device structure is shown in Figure 12.1(a). The n^+-poly-Si gate is 3-μm long.

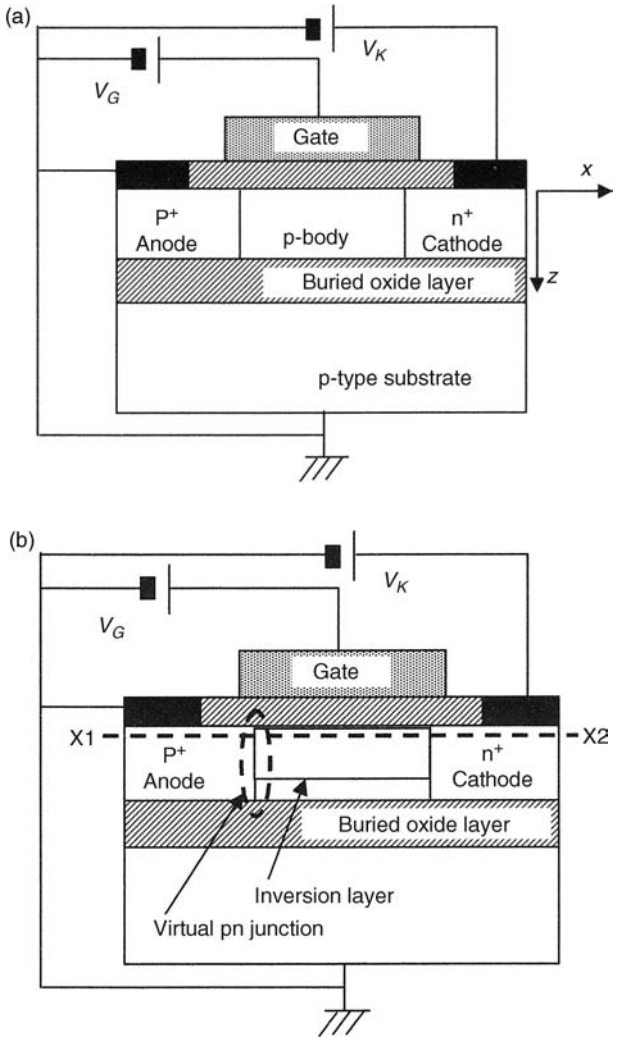

Figure 12.1 Schematic device structure and operations of Lubistor. (a) Schematic device structure of Lubistor. (b) Operation under the reverse-biased condition: tunnel at the virtual pn junction. (c) Schematic band structure along the X1–X2 cut line. Copyright 2007. The Japan Society of Applied Physics. [Y. Omura, Experimental study of two-dimensional confinement effects on reverse-biased current characteristics of ultrathin silicon-on-insulator lateral, unidirectional, bipolar-type insulated-gate transistors, *Japanese Journal of Applied Physics*, vol. 46, pp. 2968–2972, 2007.]

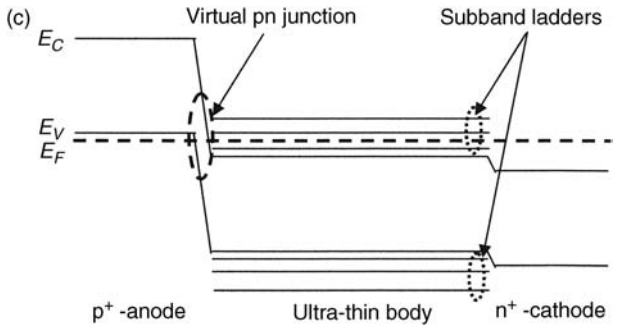

Figure 12.1 (*Continued*)

The cathode electrode is positively biased ($0 < V_K < 1$ V) for the reverse-biased experiment and the gate electrode is always positively biased to induce an inversion layer (electrons) ($1.0 < V_G < 3.5$ V), as shown in Figure 12.1(b). Therefore, in addition to the built-in junction between the n^+ cathode and the p^- body, a *virtual junction* is made between *the inversion layer* composed of electrons and the p^+*anode* as shown in Figure 12.1(c). In this experiment, we did not apply the negative bias to the gate electrode. When the negative gate bias induces an accumulation layer (holes) beneath the gate oxide layer, the confinement is directly ruled by the SOI layer thickness (t_S). On the other hand, when the positive gate bias induces an inversion layer (electrons) beneath the gate oxide layer, the confinement is ruled by the inversion layer thickness (t_{inv}), which is smaller than t_S. This means that a more significant two-dimensional confinement effect appears in the inversion layer; this is the reason why the positive gate bias is used.

12.3 Results and Discussion

12.3.1 I–V Characteristics under the Reverse-Biased Condition

Though the Lubistor has a built-in pn junction between the n^+ cathode and the p^- body inside an extremely thin silicon layer, we do not activate this junction and make a *virtual junction* between *the inversion layer* composed of electrons and the p^+*anode* (see Figure 12.1(c)); the Fermi level of the inversion layer and that of the n^+ cathode are almost the same as long as the reverse bias is not very high. In this way, it is expected that the reverse-biased leakage current should be modulated by energy quantization inside the SOI layer ($E_1 - E_C > 15$ meV (< 170 K) for two degenerate bands and other phenomena should also be influenced by such quantum effects. This will be discussed in detail below.

Reverse-biased cathode current (I_K) characteristics were measured as a function of cathode voltage (V_K) at temperatures ranging from 300 K to 35 K. At 300 K, I_K simply shows asymptotic saturation behavior at a low V_G in Figure 12.2(a), while I_K shows a slight modulation as detected by differential conductance ($g_K = dI_K/dV_K$) as shown in Figure 12.3(a). At 35 K, I_K clearly shows a step-like behavior independently of the V_G value in Figure 12.2(b). In both cases shown in Figure 12.2, however, I_K curves are almost flat for $V_K > 0.4$ V independently of

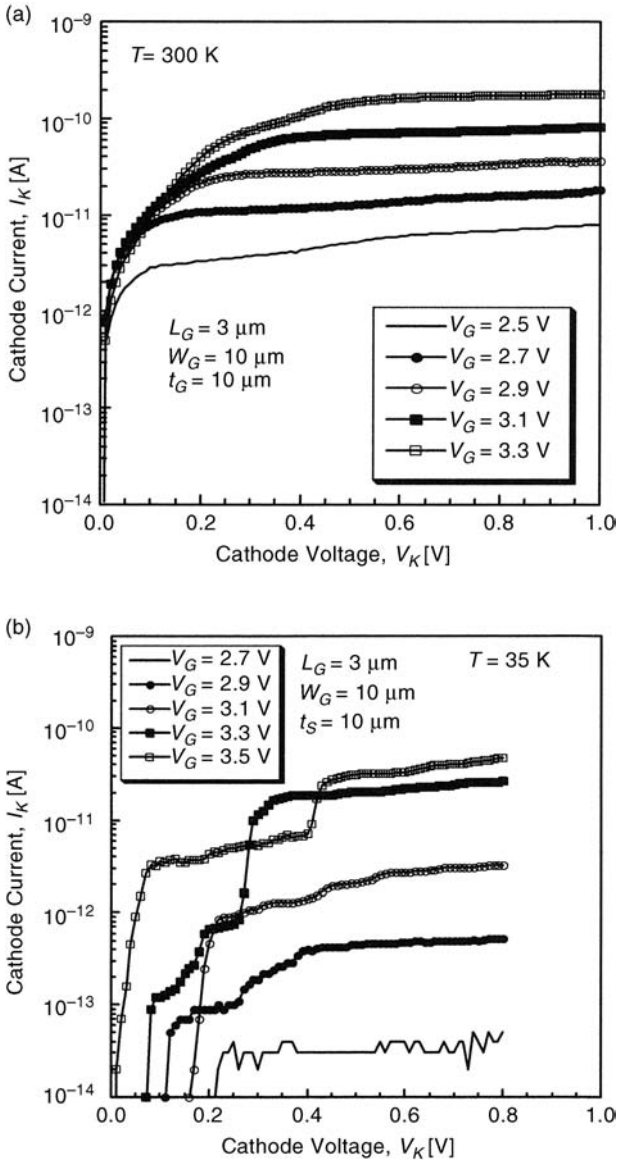

Figure 12.2 Reverse-biased current–voltage characteristics of Lubistor: (a) 300 K, (b) 35 K. Copyright 2007. The Japan Society of Applied Physics. [Y. Omura, Experimental study of two-dimensional confinement effects on reverse-biased current characteristics of ultrathin silicon-on-insulator lateral, unidirectional, bipolar-type insulated-gate transistors, *Japanese Journal of Applied Physics*, vol. 46, pp. 2968–2972, 2007.]

the V_G value, which suggests that lateral expansion of the depletion layer from the built-in n^+-cathode junction is limited by the geometrical effect [10]. Accordingly, it can be considered that the bulk-like nature of generation–recombination is hardly observed. The modulation of I_K curves (peaks of A1, A2, and B1 denoted in Figure 12.3) suggests some influence of carrier confinement in the SOI body. In Figure 12.2(b), we can see that I_C curves move to the positive side of the horizontal axis (V_K axis) when the V_G value rises, which also supports carrier confinement inside the SOI layer because the increase in V_G results in the Fermi level rising. Surprisingly, it is seen that the major peaks of g_K observed at 35 K appear at almost the same V_K values that are seen at 300 K, which also strongly suggests the existence of quantum confinement effects [4].

Since an inversion layer of electrons is created beneath the gate oxide layer by the positive gate bias, at first two-dimensional tunneling of carriers across the *virtual pn junction* between the inversion layer (n^+) and the p^+ anode can be considered [8]. A thin barrier to possible tunneling is formed across the *virtual pn junction*, as shown in Figure 12.1(c). Electron tunneling from the valence band of the anode to the conduction band of the body surface region (inversion layer) can be expected given the present gate bias configuration; this transport process does not guarantee a large tunnel current owing to two-dimensional-system-to-two-dimensional-system (2D-to-2D) tunneling [8]. This behavior can be explained by the following theoretical view [8].

The probability ($P_{i\to f}$) for a transition between the two states of the two systems on each side of the tunneling barrier is given by Fermi's golden rule:

$$P_{i\to f} = \left(\frac{2\pi}{\hbar}\right) \sum_{m,n} \sum_{k_i,k_f} \left|M_{i\to f}\right|^2 \left[f(E_i) - f(E_f)\right] \delta(E_f - E_i - q|V_K|), \tag{12.1}$$

where subscripts '*I*' and '*f*' mean *initial* and *final*, $f(E)$ is the Fermi–Dirac function, $\hbar$ is the reduced Planck's constant, and the δ function represents the conservation of the total energy assuming that the applied bias voltage V_K drops partially across the barrier [11]. The matrix element can be written in terms of the current density operator [12] based on the effective mass approximation, such that

$$M_{i\to f} = -\left(\frac{\hbar^2}{2m^*}\right) \left(\psi_f^* \frac{\partial \psi_i}{\partial x} - \psi_i \frac{\partial \psi_f^*}{\partial x}\right) \left\langle \phi_f \,|\, \phi_i \right\rangle_z \delta(k_{f,y} - k_{i,y}), \tag{12.2}$$

where it is assumed that the tunneling current flows in the x direction and two-dimensional electrons are quantized in the z direction; $\psi_i(x)$, $\psi_f(x)$, $\phi_i(z)$, and $\phi_f(z)$ are the components of wave functions in the specific directions. Finally, the tunnel current density ($J_{C,2D}$) is expressed as

$$J_{C,2D} = q\left(\int P_{A\to B} \frac{1}{\hbar} \frac{\partial E_k}{\partial k_x} d\boldsymbol{k} - \int P_{B\to A} \frac{1}{\hbar} \frac{\partial E_k}{\partial k_x} d\boldsymbol{k}\right), \tag{12.3}$$

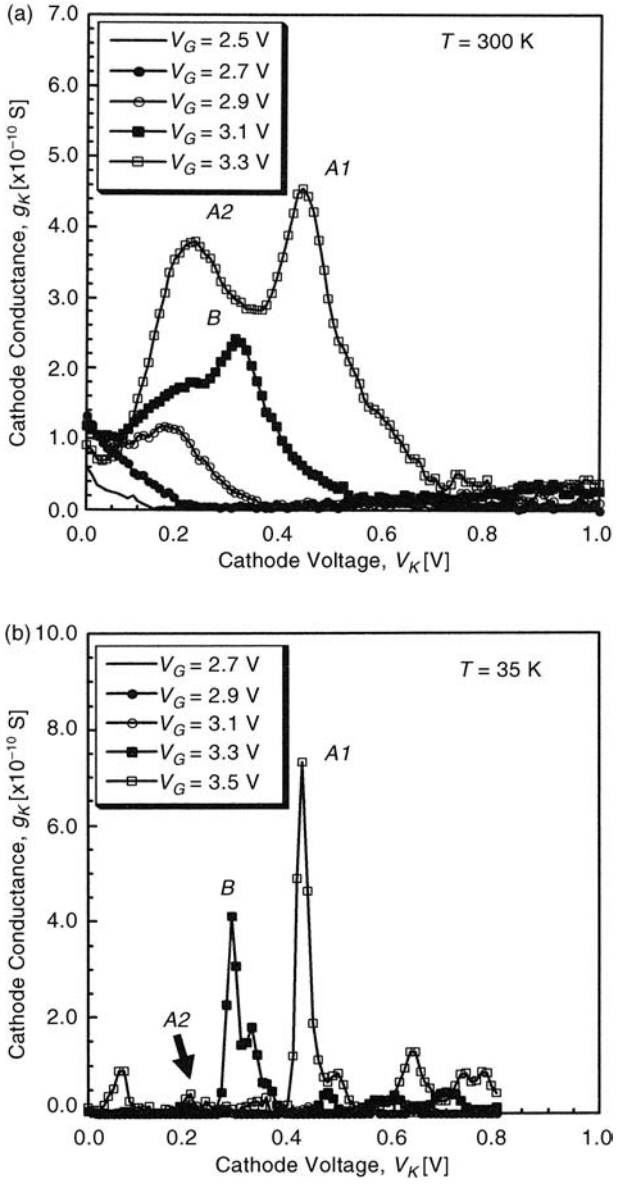

Figure 12.3 The g_K–cathode voltage characteristics of Lubistor: (a) 300 K, (b) 35 K. Copyright 2007. The Japan Society of Applied Physics. [Y. Omura, Experimental study of two-dimensional confinement effects on reverse-biased current characteristics of ultrathin silicon-on-insulator lateral, unidirectional, bipolar-type insulated-gate transistors, *Japanese Journal of Applied Physics*, vol. 46, pp. 2968–2972, 2007.]

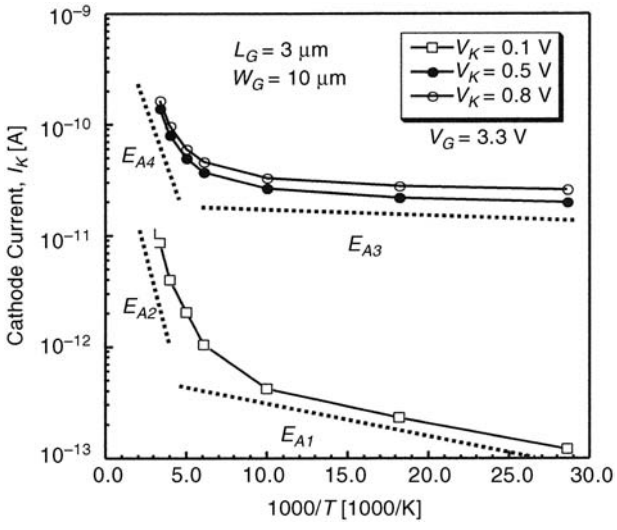

Figure 12.4 Arrhenius plots of cathode current at $V_G = 3.3$ V. Copyright 2007. The Japan Society of Applied Physics. [Y. Omura, Experimental study of two-dimensional confinement effects on reverse-biased current characteristics of ultrathin silicon-on-insulator lateral, unidirectional, bipolar-type insulated-gate transistors, *Japanese Journal of Applied Physics*, vol. 46, pp. 2968–2972, 2007.]

where $P_{A\rightarrow B}$ stands for the tunnel probability from the anode to the body, E_k is the energy of electrons having the wave number k, and k_x is the wave number of electrons contributing to the tunnel current $J_{C,2D}$. Detail of theoretical consideration is described in Chapter 11.

When the gate bias rises, the Fermi level in the SOI body goes high; electron density increases and the tunnel-barrier width of the virtual pn junction is reduced. Thus, we can see that I_K is an exponential function of V_G for $V_K > 0.2$ V [4], as seen in Figure 12.2(a) (300 K). In Figure 12.2(b) (35 K), on the other hand, it is seen that the I_K curve moves to the left side of the V_K axis when V_G rises. This is due to reduction of the tunnel-barrier width of the virtual pn junction because the inversion layer is formed and its edge approaches the p^+ anode when V_G rises.

Arrehnius plots of I_K are shown in Figure 12.4 at $V_G = 3.3$ V for three different V_K values. Curves suggest that at low temperature I_K is the result of a tunnel and/or shallow-level-induced generation–recombination process of the small dependence on $\exp(-E_{Ai}/kT)$; at $V_K = 0.1$ V, we have $E_{A1} = 58$ meV (35 K $< T <$ 100 K) and $E_{A2} = 100$ meV (250 K $< T <$ 300 K), and at $V_K = 0.5$ V (and 0.8 V), we have $E_{A3} = 13$ meV (35 K $< T <$ 100 K) and $E_{A4} = 70$ meV (250 K $< T <$ 300 K). These activation energy values suggest that the reverse-biased leakage current does not result from a deep-level-induced generation–recombination process. Since deep-level defects due to dislocations are always anticipated in the SOI layer fabricated by SIMOX technology [12], the fact of these small activation energy values (long lifetime) is quite interesting; this phenomenon has been theoretically predicted in Reference [13]. The authors consider that it is a quantum confinement effect with the assistance of the multiple-phonon interaction process. Their theoretical expression of the minority-carrier lifetime is given as [13]

$$\tau_n(z)^{-1} = \frac{N_t \bar{c}_n^0 \sum_v m_{xy}^v \sum_i |\varphi_{vi}(z)|^2 \sum_{l \geq l_0^{vi}(z)} L(l) f_c(E_l)}{kT \sum_v m_{xy}^v \sum_i |\phi_{vi}(z)|^2 F_0\left(\frac{E_F^n - E_{vi}}{kT}\right)}, \tag{12.4}$$

$$L(l) = \exp\left[-S(2n_{ph}+1)\right]\left(\frac{n_{ph}+1}{n_{ph}}\right)^{l/2} I_l\left[2S\sqrt{n_{ph}(n_{ph}+1)}\right], \tag{12.5}$$

where E_{vi} is the subband energy level, $\phi_{vi}(z)$ is the in-depth wave function of confined carriers in the subband with the index of vi, $m_{xy}^v$is the in-plane carrier effective mass, $F_0(X)$ is the zeroth-order Fermi–Dirac integral on X, $f_c(E_l)$ is the value of the Fermi–Dirac function at $E = E_l$, n_{ph} is the phonon density described by the Planck distribution function, S is the Huang–Rhys factor [14], I_l is the modified Bessel function of order l, and the others have the conventional meanings.

At high temperatures, when we assume the Boltzmann's statistics, $E_t \gg h\omega_0/(2\pi)$, and the function I_l has the asymptotic form, the above expression can be reduced to the following expression (see Appendix 12A):

$$\tau_n(z)^{-1} = \tau_0(T, \varepsilon_R, n_{ph},) \exp\left(-\frac{E_{act}^{QM}}{kT}\right), \tag{12.6}$$

$$E_{act}^{QM} = \frac{\left[E_t + E_0 - E_c(z) - \varepsilon_R\right]^2}{4\varepsilon_R}, \tag{12.7}$$

$$\varepsilon_R = S\hbar\omega_0, \tag{12.8}$$

where $\tau_0(X)$ is the pre-factor of lifetime, $E_c(z)$ is the local conduction band bottom energy modulated by the external electric field, and E_0 is the lowest subband energy. When there is no external transversal field inside the SOI layer, we approximately have $E_0 - E_c = 0.015$ eV. When we assume that $E_c - E_t = 0.55$ eV (mid-gap level), $S = 4$ and $h\omega_0/(2\pi) = 0.06$ eV (phonon energy), the estimated E_{act}^{QM} value is about 0.13 eV. This value approximately matches the E_{act} value extracted from experimental results; that is, $E_{act} = 0.07 \sim 0.1$ eV for 250 K $< T <$ 300 K.

Therefore, we think the present experimental result supports their prediction because a high gate voltage (3.3 V) enhances the carrier confinement.

On the other hand, at low temperature, when we assume the Fermi–Dirac statistics and $E_t \gg h\omega_0/(2\pi)$, Equation (12.1) can be reduced to the following expression (see Appendix 12A):

$$\tau_n(z)^{-1} = \tau_0(E_F - E_0, N_t, S) \frac{1}{1 + \left(1 + \frac{kT}{E_F - E_0}\right) \exp\left(\frac{E_0 - E_F}{kT}\right)}, \tag{12.9}$$

where all notations are already explained. When the device is in the *ON* state, we usually have $E_F - E_0 \sim k_B T$ owing to the low temperature. This implies that ${E_{act}}^{QM} < E_F - E_0$ in Equation (12.6); we have ${E_{act}}^{QM} < kT \sim 8$ meV at 100 K. Since the E_{act} value extracted from experimental results ranges from 13 meV to 58 meV, we think the theoretical estimation shown above is acceptable.

Finally, we address here the influence of the two-dimensional avalanche phenomenon. A depletion region appears across the cathode pn junction near the SOI layer bottom. However, as described previously, the geometrical effect limits the lateral expansion of depletion, which usually increases the lateral electric field across the cathode pn junction. In the present bias condition, the electric field across the cathode pn junction is not very high because $|V_K|$ is at most 1 V. Therefore, we think that the avalanche near the cathode junction is not significant.

12.4 Summary

In this chapter the reverse-biased current characteristics of Lubistors with a 10-nm-thick Si body at low temperature were extensively examined. At low temperature, the two-dimensional tunneling process is strongly suggested. On the other hand, at around room temperature, the suggestion is that the generation–recombination process primarily rules transport. However, over the whole temperature range, it has been discovered that the activation energy of the generation–recombination process is much smaller than simply expected from the fabrication process (SIMOX technology); this feature can be understood when the influence of quantum confinement on the generation–recombination process is assumed as the theoretical prediction suggests.

Appendix 12A: Derivation of Equations (12.6) and (12.9)

Since the approximate expressions (Equations (12.6) and (12.7)) at high temperatures are already given by Hoehr, Schenk and Fichtner [13], we do not describe how Equation (12.4) is reduced to them.

At a low temperature, the phonon density n_{ph} is approximated as

$$n_{ph} = \frac{1}{\exp(\hbar\omega_0/kT) - 1} \approx \exp(-\hbar\omega_0/kT) \ll 1. \tag{12A.1}$$

The function $L(l)$ given by Equation (12.5) is reduced to

$$L(l) = \exp(-S)\exp\left(\frac{l\hbar\omega_0}{2kT}\right) I_l\left[2S\exp\left(-\frac{\hbar\omega_0}{2kT}\right)\right]. \tag{12A.2}$$

Here, the modified Bessel function $I_l(x)$ can be calculated for $x \ll 1$ as

$$\begin{aligned} I_l(x) &= \frac{1}{\pi}\int_0^{\pi} \exp(x\cos\theta)\cos(l\theta)d\theta \\ &\approx \frac{1}{\pi}\int_0^{\pi} (1 + x\cos\theta)\cos(l\theta)d\theta \\ &= \frac{x}{2}. \end{aligned} \tag{12A.3}$$

Since almost all carriers in the conduction band occupy the lowest subband ($l = 1$), from Equation (12A.2) we have

$$L(l) \approx L(1) = S\exp(-S). \tag{12A.4}$$

Since the low temperature condition is assumed, we must take into account that $l = 1$ and $i = 1$ in Equation (12.4). Therefore, we have the following approximate expression for Equation (12.4):

$$\tau_n(z)^{-1} \approx \frac{N_t \bar{c_n^0} L(1) f_c(E_1)}{kTF_0\left(\dfrac{E_F^n - E_1}{kT}\right)}, \tag{12A.5}$$

where $f_c(E_1)$ and $F_0[(E_F{}^n - E_1)/(kT)]$ are expressed as

$$f_c(E_1) = \frac{1}{1 + \exp\left(\dfrac{E_1 - E_F^n}{kT}\right)}, \tag{12A.6}$$

$$\begin{aligned} F_0\left(\frac{E_F^n - E_1}{kT}\right) &= \ln\left[1 + \exp\left(\frac{E_F^n - E_1}{kT}\right)\right] \\ &= \ln\left\{\exp\left(\frac{E_F^n - E_1}{kT}\right)\left[1 + \exp\left(\frac{E_1 - E_F^n}{kT}\right)\right]\right\} \\ &= \frac{E_F^n - E_1}{kT} + \ln\left[1 + \exp\left(\frac{E_1 - E_F^n}{kT}\right)\right]. \end{aligned} \tag{12A.7}$$

Therefore, Equation (12A.5) can be rewritten as

$$\tau_n(z)^{-1} = \left(\frac{N_t \bar{c_n^0}}{kT}\right) \frac{S\exp(-S)}{\left\{\left(\dfrac{E_F^n - E_1}{kT}\right) + \ln\left[1 + \exp\left(\dfrac{E_1 - E_F^n}{kT}\right)\right]\right\}\left[1 + \exp\left(\dfrac{E_1 - E_F^n}{kT}\right)\right]}. \tag{12A.8}$$

When the surface inversion layer is formed, we can expect $E_F{}^n - E_1 > kT$. This leads to $\exp[(E_1 - E_F{}^n)/(kT)] \ll 1$. Then, we have the following approximation flow:

$$\begin{aligned} \tau_n(z)^{-1} &\approx \left(\frac{N_t \bar{c_n^0}}{kT}\right) \frac{S\exp(-S)}{\left\{\left(\dfrac{E_F^n - E_1}{kT}\right) + \exp\left(\dfrac{E_1 - E_F^n}{kT}\right)\right\}\left[1 + \exp\left(\dfrac{E_1 - E_F^n}{kT}\right)\right]} \\ &= \left(\frac{N_t \bar{c_n^0}}{E_F^n - E_1}\right) \frac{S\exp(-S)}{\left\{1 + \left(\dfrac{kT}{E_F^n - E_1}\right)\exp\left(\dfrac{E_1 - E_F^n}{kT}\right)\right\}\left[1 + \exp\left(\dfrac{E_1 - E_F^n}{kT}\right)\right]} \\ &\approx \left(\frac{N_t \bar{c_n^0}}{E_F^n - E_1}\right) \frac{S\exp(-S)}{1 + \left(\dfrac{kT}{E_F^n - E_1} + 1\right)\exp\left(\dfrac{E_1 - E_F^n}{kT}\right)}. \end{aligned} \tag{12A.9}$$

Thus, Equation (12.9) was obtained.

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13

Supplementary Consideration of *I-V* Characteristics of Forward-Biased Ultra-Thin Lubistors

13.1 Introduction

Since the Lubistor has a pn junction, band-to-band tunneling across the junction and negative differential conductance were expected. Several articles reporting the negative differential conductance have already been published [1–5] and the fundamental mechanisms of negative differential conductance have been analyzed successfully [4, 5]. In addition, the impact of carrier confinement on the generation–recombination process is attracting attention because it suggests the significant benefit of low-dimensionality minority carrier injection.

This chapter introduces some of the results of experiments conducted on ultra-thin film Lubistors at low temperatures (down to 35 K) to evaluate the impact of forward-biased two-dimensional transport on generation–recombination.

13.2 Device Structures and Bias Configuration

A Lubistor with a lateral n^+–p–p^+ structure was fabricated on a (001) Si SIMOX wafer with a 110-nm buried oxide layer; it has a 5-nm-thick gate oxide layer and a 10-nm-thick Si layer [2]; the schematic device structure is shown in Figure 13.1. The n^+-poly-Si gate is 3-μm long. The cathode electrode is negatively biased for the forward-biased experiment ($V_K = -0.5$ V) and the gate electrode is always positively biased to induce inversion layer (electrons) ($1.0 < V_G < 3.5$ V). Thus, in addition to the built-in junction between the n^+ cathode and the p^- body, a *virtual junction* is created between the *inversion layer* composed of electrons and the p^+*anode*. When the positive gate bias induces an inversion layer (electrons) beneath the gate oxide layer, the confinement is ruled by the inversion layer thickness (t_{inv}), which is smaller than t_S. This means that a more significant two-dimensional confinement effect appears in the inversion layer; this explains the use of the positive gate bias.

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

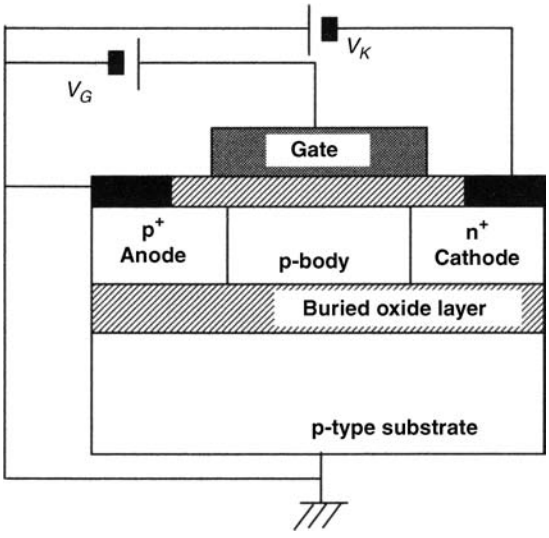

Figure 13.1 Schematic device structure of a forward-biased Lubistor.

13.3 Results and Discussion

Forward-biased cathode current (I_K) characteristics were measured as a function of negative cathode voltage (V_K) at temperatures ranging from 300 K to 35 K. Since I have already published papers describing the negative conductance characteristics of Lubistors [2–5], here cathode current (I_K) versus gate voltage (V_G) characteristics are shown in Figure 13.2 for the sake of the following discussion.

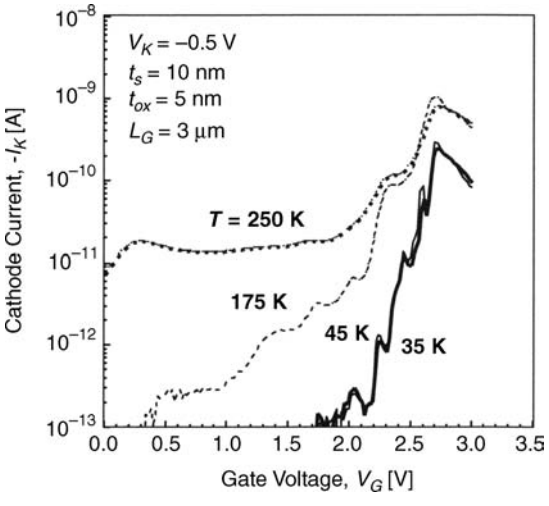

Figure 13.2 Forward-biased I_K–V_G characteristics of Lubistor [5].

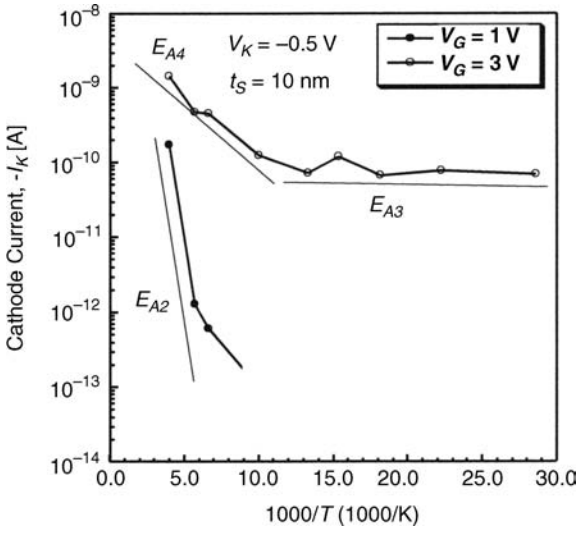

Figure 13.3 Arrehnius plots of cathode current at $V_K = -0.5$ V.

At 35 K and 45 K, the I_K curve clearly shows a step-like feature, which suggests crossing over the Fermi levels in the subband ladder one by one [6]. At 250 K, however, I_K does not show such a clear step-like feature, which suggests that carrier transport is disturbed by the thermal energy.

Arrhenius plots of I_K at $V_K = -0.5$ V are shown in Figure 13.3. Figure 13.3 also suggests that, at low temperatures, I_K is the result of tunneling and/or a shallow-level-induced generation–recombination process, which has a small dependence on $\exp(-E_{Ai}/kT)$; at $V_G = 1$ V, we have $E_{A2} = 240$ meV (175 K $< T <$ 250 K) and at $V_G = 3$ V, we have $E_{A3} =$ 3.4 meV (35 K $< T <$ 65 K) and $E_{A4} = 58$ meV (175 K $< T <$ 250 K). It appears possible to consider that these activation energy values do not correspond to deep-level-induced generation–recombination processes.

As described in Chapter 12, it should be considered that the carrier confinement effect reduces the activation energy of deep levels [7]. At $V_G = 1$ V, the activation energy is relatively large at around 250 K, which is acceptable because the gate-induced field for carrier confinement is low. At $V_G = 3$ V, on the other hand, the activation energy is very small because the gate-induced field for carrier confinement is very high. From a theoretical estimation of the activation energy value described in Chapters 11 and 12, we can consider that the experimental values of activation energy basically match the theoretical prediction.

13.4 Summary

In this supplementary description, the low-temperature forward-biased current characteristics of Lubistors with a 10-nm-thick Si body were extensively examined. At low temperature, the two-dimensional tunneling process is strongly suggested. On the other hand, at around room temperature, the suggestion is that the generation–recombination process is the primary determiner of transport. However, over the whole temperature range, it has been discovered

that the activation energy of the generation–recombination process is much smaller than that simply expected from the fabrication process (SIMOX technology); this feature can be understood by assuming that quantum confinement influences the generation–recombination process as the theoretical prediction in the previous chapter suggests.

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14

Gate-Controlled Bipolar Action in the Ultra-Thin Dynamic Threshold SOI MOSFET

14.1 Introduction

The voltage-controlled bipolar SOI MOSFET was proposed in 1987 [1] with the goal of achieving high drive currents. The dynamic threshold SOI MOSFET (DT-MOSFET) was proposed in 1997 [2] to realize sub-1-volt operation with a sharp swing. However, both devices have a serious problem in that their opposite drain current (I_D) is large at low drain voltages (V_D) when a high gate voltage (V_G) is applied to the body contact. This is due to their thick SOI layer.

This chapter demonstrates some interesting attributes of the ultra-thin DT-MOSFET, which has a confined structure; the bipolar action is suppressed or enhanced by the gate following the mechanism of Lubistor operation [3]. In addition, the next section turns to experimental results to address the channel polarity dependence of the bipolar action of the ultra-thin-body DT-MOSFET.

14.2 Device and Experiments

Two-different n-channel underlapped single-gate fully depleted (FD) SOI MOSFETs (Devices A and B) with a body contact were fabricated on (001) SIMOX substrates with an 80-nm-thick BOX layer. The schematic device layout is shown in Figure 14.1. Device parameters are summarized in Table 14.1. This study evaluated room-temperature I_D–V_G characteristics of various DT-MOSFETs at various substrate biases (V_{sub}) because the focus is on gate-controlled double injection [3].

14.3 Results and Discussion

14.3.1 $\mathrm{I_D}$–$\mathrm{V_G}$ *and* $\mathrm{I_G}$–$\mathrm{V_G}$ *Characteristics of the Ultra-Thin-Body DT-MOSFET*

Figure 14.2 shows I_D–V_G curves for Devices A and B at $V_{sub} = 0$ V. Device A with a thick SOI layer shows a significant opposite drain current (I_D) at low drain voltage (V_D). In contrast, Device B shows a very low opposite drain current (I_D) at low drain voltage (V_D). These

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

Table 14.1 Device parameters. © 2007 IEEE. Reprinted, with permission, from Y. Omura and T. Tochio, Gate-Controlled Bipolar Action in Ultrathin-Body Dynamic-Threshold SOI MOSFET, *Proceedings of the IEEE International SOI Conference*, Indian Wells, October 2007, pp. 63–64. © 2008 IEEE. Reprinted, with permission, from T. Tochio and Y. Omura, Transport Aspects and Comparison of n-Channel and p-Channel Ultra-Thin-Body Dynamic-Threshold MOSFETs, *Digest of the IEEE International Meeting for Future of Electron Devices*, Kansai (IMFEDK2008), pp. 53–54

Parameters [unit]	Device A	Device B
t_{ox} [nm]	7	7
t_S [nm]	50	25
t_{BOX} [nm]	80	80
N_A [cm^{-3}]	$<3 \times 10^{17}$	$<3 \times 10^{17}$
W_G [μm]/L_G [μm]	16/1	16/1
V_{TH} of FD MOSFET[a] [V] at $V_D = 0.10$ [V]		
At $V_{sub} = 0$ [V]	0.14	−0.030
At $V_{sub} = -5$ [V]	0.72	0.66
At $V_{sub} = 3$ [V]	−0.15	−0.29

[a]Without gate-body connection.

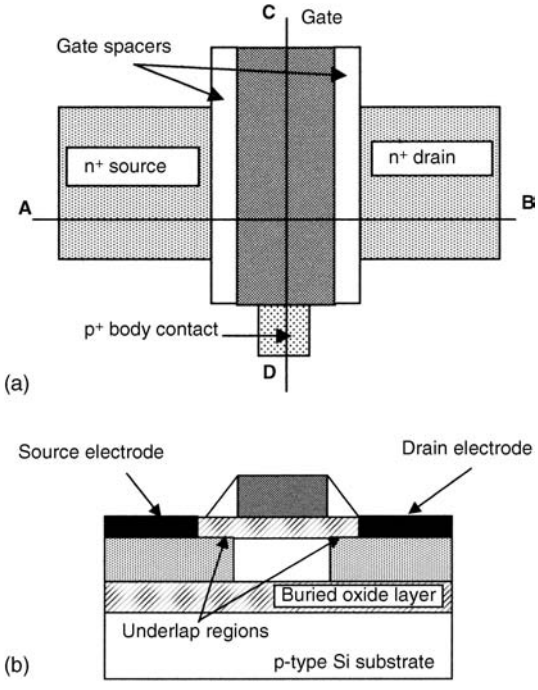

Figure 14.1 Schematic layout of fabricated devices. (a) Top view of SOI DT-MOSFET. (b) Cross-section of SOI DT-MOSFET: A–B cut line. © 2007 IEEE. Reprinted, with permission, from Y. Omura and T. Tochio, Gate-Controlled Bipolar Action in Ultrathin-Body Dynamic-Threshold SOI MOSFET, *Proceedings of the IEEE International SOI Conference*, Indian Wells, October 2007, pp. 63–64. © 2008 IEEE. Reprinted, with permission, from T. Tochio and Y. Omura, Transport Aspects and Comparison of n-Channel and p-Channel Ultra-Thin-Body Dynamic-Threshold MOSFETs, *Digest of the IEEE International Meeting for Future of Electron Devices*, Kansai (IMFEDK2008), pp. 53–54.

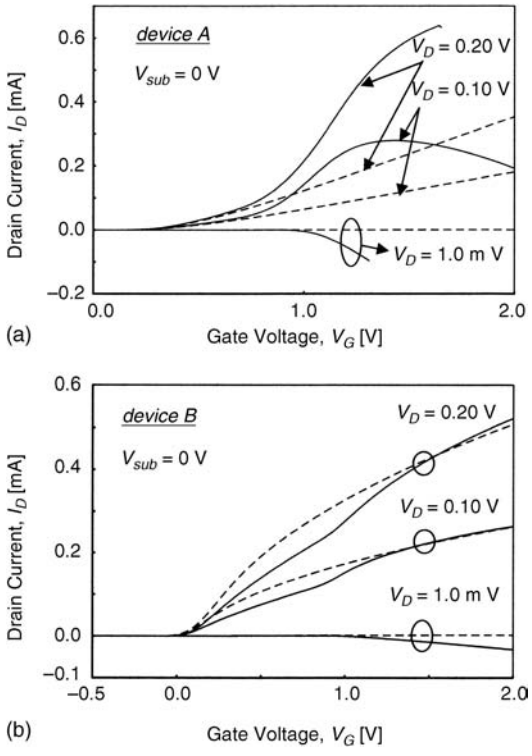

Figure 14.2 I_D–V_G characteristics of Devices A and B (solid lines stand for DT-MOSFET and broken lines for MOSFET with the body floating): (a) Device A, (b) Device B. © 2007 IEEE. Reprinted, with permission, from Y. Omura and T. Tochio, Gate-Controlled Bipolar Action in Ultrathin-Body Dynamic-Threshold SOI MOSFET, *Proceedings of the IEEE International SOI Conference*, Indian Wells, October 2007, pp. 63–64. © 2008 IEEE. Reprinted, with permission, from T. Tochio and Y. Omura, Transport Aspects and Comparison of n-Channel and p-Channel Ultra-Thin-Body Dynamic-Threshold MOSFETs, *Digest of the IEEE International Meeting for Future of Electron Devices*, Kansai (IMFEDK2008), pp. 53–54.

behaviors stem from the gate current injected from the body contact. Corresponding I_G–V_G characteristics are shown in Figure 14.3. The I_G level of Device B is lower than that of device A owing to the strong fully depleted (FD) condition in the body [4].

Schematic band diagrams are shown in Figure 14.4 in order to discuss the bipolar operation. Since Device A has a thicker SOI layer, the body potential can be more easily modulated by the substrate bias (V_{sub}); in other words, the body potential can be controlled by the body contact. The A–B band diagram for Device A at a low gate voltage (V_G) is schematically shown in Figure 14.4(a) and the C–D band diagram in Figure 14.4(c); the hole injection from the body contact reaches far, although holes are primarily injected into the source. The A–B band diagram at high V_G is shown in Figure 14.4(b); holes are also injected into the drain since $V_G > V_D$, resulting in the opposite drain current (I_D) seen in Figure 14.2(a).

The A–B band diagram of Device B shows a limited gate voltage impact because the body potential is strongly defined by the gate voltage (V_G). As a result, the C–D band diagram can be approximated as shown in Figure 14.4(d), where hole injection into the drain is quite limited; the opposite drain current (I_D) is very low.

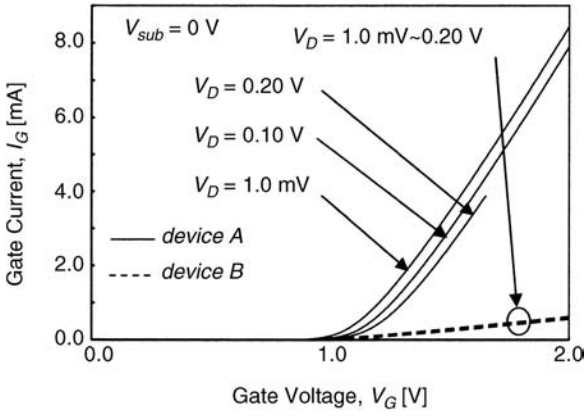

Figure 14.3 I_G–V_G characteristics of Devices A and B. I_G is insensitive to V_{sub}. © 2007 IEEE. Reprinted, with permission, from Y. Omura and T. Tochio, Gate-Controlled Bipolar Action in Ultrathin-Body Dynamic-Threshold SOI MOSFET, *Proceedings of the IEEE International SOI Conference*, Indian Wells, October 2007, pp. 63–64. © 2008 IEEE. Reprinted, with permission, from T. Tochio and Y. Omura, Transport Aspects and Comparison of n-Channel and p-Channel Ultra-Thin-Body Dynamic-Threshold MOSFETs, *Digest of the IEEE International Meeting for Future of Electron Devices*, Kansai (IMFEDK2008), pp. 53–54.

14.3.2 Control of Bipolar Action by the MOS Gate

Device A with a thick body suggests a small bipolar gain (∼0.3) at $V_D = 0.2$ V, while Device B has a bipolar gain of ∼2. In Device A, we can extract the transport efficiency (α_T) from Figure 14.2(a); $\alpha_T \sim 0.25$ at $V_D = 0.2$ V. In contrast, in Device B, we have $\alpha_T \sim 0.7$ at $V_D = 0.2$ V, which suggests a diffusion length of ∼1 μm. It is considered that the difference in α_T comes from the *stickiness* of the Fermi level pinned by surface majority electrons in the body. In fact, this stickiness of the Fermi level appears in Figure 14.3; the gate current (I_G) is quite insensitive to the substrate bias (V_{sub}) in Device B. This consideration is supported by the I_D–V_G characteristics at various V_{sub} values (not shown here).

14.4 Channel Polarity Dependence of Bipolar Action

14.4.1 $\mathbf{I_D}$–$\mathbf{V_G}$ *and* $\mathbf{g_m}$–$\mathbf{V_G}$ *Characteristics of the Ultra-Thin-Body DT-MOSFET*

Figure 14.5 shows I_D–V_G, I_G–V_G, g_m–V_G, and $I_{D,DT}/I_{D,MOS}$ (ratio of DT-MOS drain current to MOS drain current) curves for n-channel and p-channel Device A ($t_S = 100$ nm) at $V_{sub} = 0$ V. Both devices show a significant opposite flow of drain current (I_D) at low drain voltage (V_D). In addition, the g_m curve of the n-channel device shows a large peak corresponding to bipolar operation, while the g_m peak corresponding to MOS operation is very small. In contrast to the n-channel device, however, the p-channel DT-MOS device is characterized by a simple curve; a single peak is seen for each drain voltage condition.

It is anticipated that the difference in drain current behavior stems from the difference in threshold voltage of the n-channel and p-channel devices. Since both devices have an

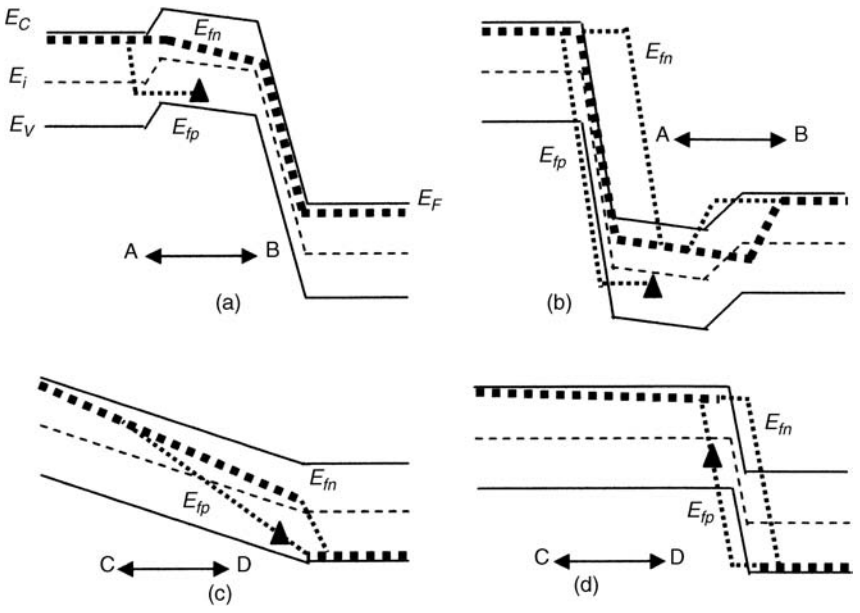

Figure 14.4 Schematic band diagrams of SOI DT-MOSFETs. Closed triangles in the bandgap show the crossover between two quasi-Fermi levels of holes (E_{fp}): (a) A–B band diagram for Device A at low gate voltage, (b) A–B band diagram for Device A at high gate voltage, (c) C–D band diagram for Device A at low gate voltage, (d) C–D band diagram for Device B at low gate voltage. © 2007 IEEE. Reprinted, with permission, from Y. Omura and T. Tochio, Gate-Controlled Bipolar Action in Ultrathin-Body Dynamic-Threshold SOI MOSFET, *Proceedings of the IEEE International SOI Conference*, Indian Wells, October 2007, pp. 63–64. © 2008 IEEE. Reprinted, with permission, from T. Tochio and Y. Omura, Transport Aspects and Comparison of n-Channel and p-Channel Ultra-Thin-Body Dynamic-Threshold MOSFETs, *Digest of the IEEE International Meeting for Future of Electron Devices*, Kansai (IMFEDK2008), pp. 53–54.

n^+-poly-Si gate and have reciprocal junction configurations of n^+–p–n^+ for nMOS and p^+–n–p^+ for pMOS, the threshold voltage of pMOS is very high; the top surface of the SOI body of pMOS has an electron accumulation layer at $V_G = 0$ V, as shown in Figure 14.6 (a). On the other hand, the SOI body of the n-channel DT-MOS is almost fully depleted due to the work function of the n^+-poly-Si gate; this difference from the p-channel DT-MOSFET plays an important role in the present discussion.

14.4.2 Difference of Bipolar Operation between the n-Channel DT-MOS and the p-Channel DT-MOS

To consider how the threshold voltage of devices impacts the bipolar operation, the ratio ($I_{D,DT}/I_{D,MOS}$) of the drain current of DT-MOS to that of a body-tied MOSFET is also plotted in Figure 14.5 for Device A ($t_S = 100$ nm).

In the n-channel DT-MOS, the ratio remains basically at unity for $V_G < 0.5$ V and rapidly rises up to about 10 for $V_G > 0.5$ V, followed by an abrupt decrease for $V_G > 1$ V due to an

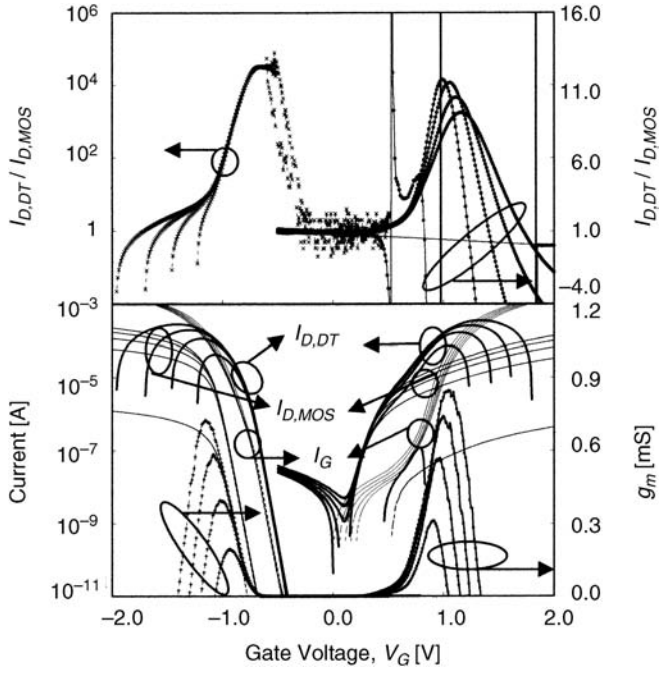

Figure 14.5 I_D–V_G, I_G–V_G, g_m–V_G, and $I_{D,DT}/I_{D,MOS}$ characteristics of Device A. © 2007 IEEE. Reprinted, with permission, from Y. Omura and T. Tochio, Gate-Controlled Bipolar Action in Ultrathin-Body Dynamic-Threshold SOI MOSFET, *Proceedings of the IEEE International SOI Conference*, Indian Wells, October 2007, pp. 63–64. © 2008 IEEE. Reprinted, with permission, from T. Tochio and Y. Omura, Transport Aspects and Comparison of n-Channel and p-Channel Ultra-Thin-Body Dynamic-Threshold MOSFETs, *Digest of the IEEE International Meeting for Future of Electron Devices*, Kansai (IMFEDK2008), pp. 53–54.

opposite drain current. On the other hand, in the p-channel DT-MOS, the ratio rapidly rises up to about 10^4 for $V_G > -0.5$ V and rapidly falls down to unity for $V_G < -0.7$ V, followed by polarity change for $V_G < -1$ V due to an opposite drain current.

It should be noted in Figure 14.5 that the subthreshold drain current curve of the pMOSFET lies far to the left side, by ∼0.25 V, of the gate current curve of the p-channel DT-MOS. Therefore, in the p-channel DT-MOS examined here, MOS-like operation cannot be expected, but bipolar operation is significant.

14.4.3 Impact of Body Thickness on Bipolar Operation

Finally, we address the impact of body thickness on bipolar operation. Figure 14.7 shows the ratio of the drain current of DT-MOS to that of body-tied MOSFET ($I_{D,DT}/I_{D,MOS}$) for $t_S = 50$ nm (Device B); I_D–V_G, I_G–V_G, and g_m–V_G characteristics are also shown in Figure 14.7 to assist understanding. It is seen that the ratio curve of the n-channel device has lower peaks than in Figure 14.5 because the bipolar operation is suppressed [5]. In contrast to the n-channel device, the ratio curve of the p-channel device almost retains its aspect, shown in Figure 14.5, because the threshold voltage is not as sensitive to the SOI layer thickness (t_S) in this range.

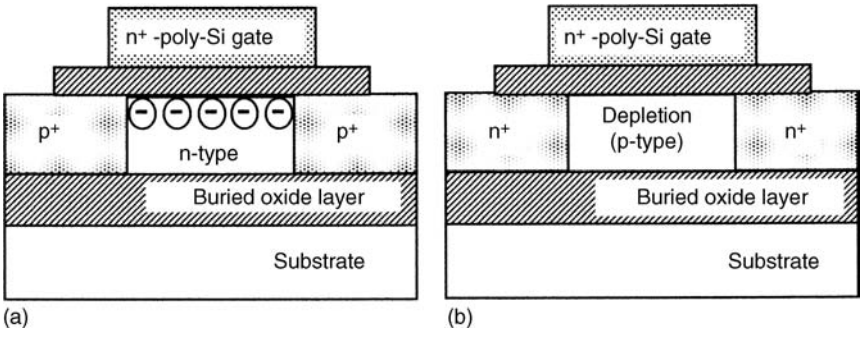

Figure 14.6 Schematic views of device operation: (a) pMOS, (b) nMOS. © 2007 IEEE. Reprinted, with permission, from Y. Omura and T. Tochio, Gate-Controlled Bipolar Action in Ultrathin-Body Dynamic-Threshold SOI MOSFET, *Proceedings of the IEEE International SOI Conference*, Indian Wells, October 2007, pp. 63–64. © 2008 IEEE. Reprinted, with permission, from T. Tochio and Y. Omura, Transport Aspects and Comparison of n-Channel and p-Channel Ultra-Thin-Body Dynamic-Threshold MOSFETs, *Digest of the IEEE International Meeting for Future of Electron Devices*, Kansai (IMFEDK2008), pp. 53–54.

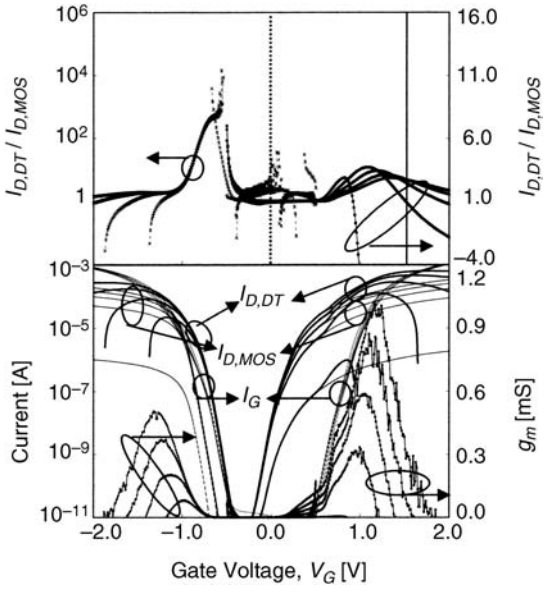

Figure 14.7 I_D–V_G, I_G–V_G, g_m–V_G, and $I_{D,DT}/I_{D,MOS}$ characteristics of Device B. © 2007 IEEE. Reprinted, with permission, from Y. Omura and T. Tochio, Gate-Controlled Bipolar Action in Ultrathin-Body Dynamic-Threshold SOI MOSFET, *Proceedings of the IEEE International SOI Conference*, Indian Wells, October 2007, pp. 63–64. © 2008 IEEE. Reprinted, with permission, from T. Tochio and Y. Omura, Transport Aspects and Comparison of n-Channel and p-Channel Ultra-Thin-Body Dynamic-Threshold MOSFETs, *Digest of the IEEE International Meeting for Future of Electron Devices*, Kansai (IMFEDK2008), pp. 53–54.

14.5 Summary

This chapter considered the potential of the ultra-thin SOI DT-MOS from the point of view of application to 1-V operation circuits. As a result, it is strongly suggested that we can expect to realize a DT-MOSFET that suits low-power operation by suppressing the parasitic bipolar action and low-noise circuit applications by utilizing the remaining bipolar nature of its operation.

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15

Supplementary Study on Gate-Controlled Bipolar Action in the Ultra-Thin Dynamic Threshold SOI MOSFET

15.1 Introduction

The voltage-controlled bipolar-silicon-on-insulator (SOI) MOSFET was proposed in 1987 [1] to achieve high drive currents. The dynamic threshold SOI MOSFET (DT-MOSFET) was proposed in 1997 [2] to realize sub-1-volt operation with a sharp swing. However, both devices have a serious problem in that their opposite drain current (I_D) is large at low drain voltage (V_D) when a high gate voltage (V_G) is applied to the body contact. It is anticipated that this is due to their thick SOI layer. Authors have already demonstrated some interesting attributes of the ultra-thin DT-MOSFET, which has a confined structure at room temperature [3]. It was demonstrated that the bipolar action is suppressed or enhanced by the gate voltage following the mechanism of Lubistor operation [4,5].

This chapter demonstrates significant aspects of low-temperature minority-carrier injection in the n-channel dynamic threshold (DT) MOSFET with various SOI layer thicknesses. $I_D - V_G$ and $I_G - V_G$ characteristics are evaluated at temperatures ranging from 300 K to 30 K and minority carrier injection is characterized.

15.2 Device Structures and Parameters

n-Channel underlapped single-gate fully depleted (FD) SOI MOSFETs (Devices A and B) with body contact were fabricated on (001) SIMOX substrates with an 80-nm-thick or 480-nm-thick buried oxide (BOX) layer [6]. The schematic device layout and cross-sectional

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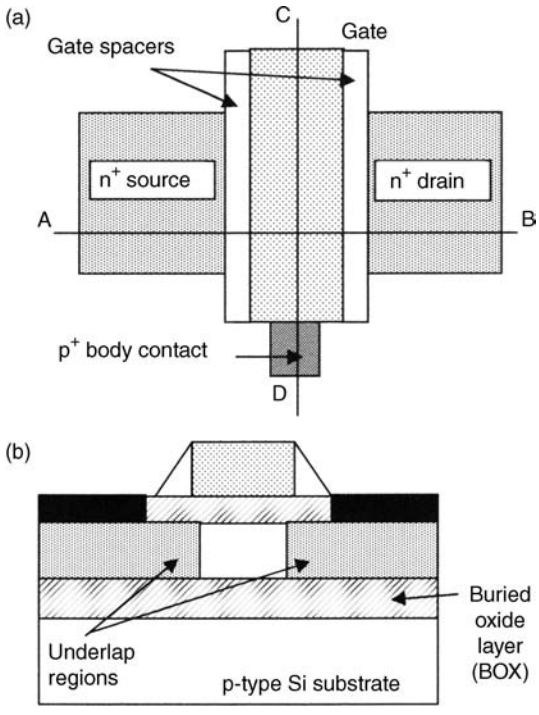

Figure 15.1 Schematic layout of fabricated devices. (a) Top view of SOI DT-MOSFET, (b) cross-section of SOI DT-MOSFET: A–B cut line. Reprinted from *Cryogenics*, vol. 49, Y. Omura and T. Tochio, Significant aspects of minority carrier injection in dynamic-threshold SOI MOSFET at low temperature, pp. 611–614. Copyright 2009, with permission from Elsevier.

view are shown in Figure 15.1. Device parameters are summarized in Table 15.1. This study primarily evaluated the temperature-dependent I_D–V_G and I_G–V_G characteristics of various DT-MOSFETs at zero substrate bias ($V_{sub} = 0\,\mathrm{V}$) for $V_D < 0.2\,\mathrm{V}$ because our discussion focuses on gate-controlled double injection [4,5].

Table 15.1 Device parameters. Reprinted from *Cryogenics*, vol. 49, Y. Omura and T. Tochio, Significant aspects of minority carrier injection in dynamic-threshold SOI MOSFET at low temperature, pp. 611–614. Copyright 2009, with permission from Elsevier

Parameters [unit]	Device A	Device B
t_{ox} [nm]	7	7
t_S [nm]	100	50
t_{BOX} [nm]	480	80
N_A [cm^{-3}]	$<1 \times 10^{17}$	$<3 \times 10^{17}$
L_{eff} [μm]	0.94–0.32	0.94–0.32
V_{TH} of FD MOSFET[a] [V] at $V_D = 0.10$ [V] and $V_{sub} = 0$ [V]	0.25	0.14

[a]Without gate-body connection.

15.3 Results and Discussion

15.3.1 SOI MOSFET Mode and DT-MOSFET Mode

Figure 15.2 shows I_D–V_G curves for Device A with the channel length (L_{eff}) of 0.94 μm and zero substrate bias ($V_{sub} = 0$ V); Figure 15.2(a) is for the SOI MOSFET mode and Figure 15.2(b) is for the DT-MOSFET mode. In the DT-MOSFET mode, the device shows a significant opposite drain current (I_D) at low drain voltages (V_D), regardless of temperature, owing to the thick SOI layer [3]. In the SOI MOSFET mode, the drain current (I_D) at 30 K is larger than that at 300 K owing to high electron mobility. In contrast to the SOI MOSFET, the drain current (I_D) of the DT-MOSFET at 30 K is lower than that at 300 K, while the gate current (I_G) at 30 K is higher than that at 300 K (see Figure 15.3). This suggests that the gate current (hole injection from the body contact) does not primarily contribute to

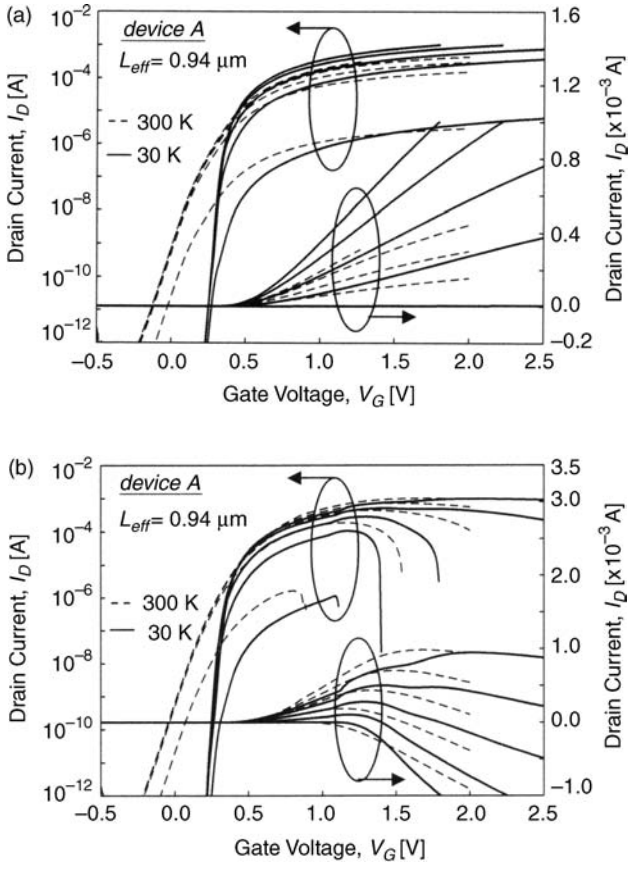

Figure 15.2 I_D–V_G characteristics of Device A for $L_{eff} = 0.94$ μm at 300 K and 30 K. (a) Body-tied SOI MOSFET, (b) DT-MOSFET. Reprinted from *Cryogenics*, vol. 49, Y. Omura and T. Tochio, Significant aspects of minority carrier injection in dynamic-threshold SOI MOSFET at low temperature, pp. 611–614. Copyright 2009, with permission from Elsevier.

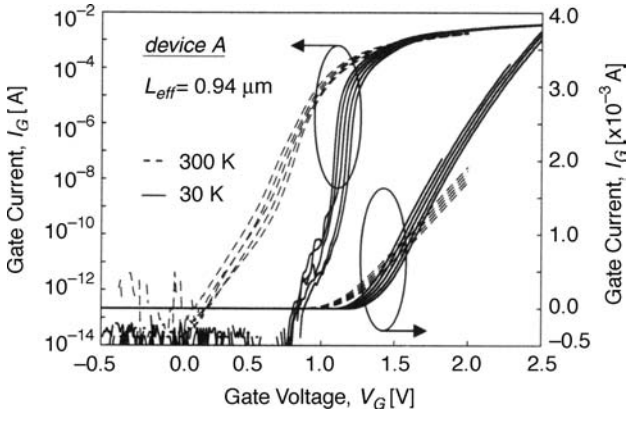

Figure 15.3 I_G–V_G characteristics of Device A for $L_{eff} = 0.94$ μm at 300 K and 30 K. I_G is sensitive to temperature. Reprinted from *Cryogenics*, vol. 49, Y. Omura and T. Tochio, Significant aspects of minority carrier injection in dynamic-threshold SOI MOSFET at low temperature, pp. 611–614. Copyright 2009, with permission from Elsevier.

the enhancement of the drain current (I_D), which is quite different from the drain current behavior seen at 300 K [3,7].

In Figure 15.3, it is seen that the threshold voltage (V_{TG}) of the gate current rises as the temperature falls, although its subthreshold swing (S_G) at 30 K is more abrupt than that at 300 K; the effective body-contact resistance is about 1000 Ω for $V_G > 1.5$ V regardless of temperature. This strongly suggests (i) that the threshold voltage of the gate current (V_{TG}) rises due to the freeze-out effect of majority carriers (holes) and the resulting increase in the pn-junction barrier height at the source junction, and (ii) once holes are injected into the source region, the subthreshold swing (S_G) is reduced because most impurities (donors) are frozen out of the source region and many holes can be accepted in the source region; the effective diffusion length in the source region increases at low temperature.

15.3.2 *Temperature Evolution of Transconductance* (g_m) *Characteristics and Impact of Channel Length on* g_m *Characteristics*

The *gate voltage dependence of transconductance* (g_m) is shown in Figure 15.4 at 300 K and 30 K; Figure 15.4(a) shows the transconductance behavior for $L_{eff} = 0.94$ μm and Figure 15.4(b) shows that for $L_{eff} = 0.8$ μm. In Figure 15.4(a), at 300 K, the transconductance (g_m) curves reveal three peculiar peaks (labeled P1, P2, and P3). P1 occurs at about $V_G = 0.7$ V; it appears because the gate-induced positive body bias lowers the threshold voltage. P2 occurs at about $V_G = 0.8$ V; it appears because the steep increase in gate current induces electron injection from the source junction. P3 occurs when $V_G > 1$ V; this peak appears because, apparently, the drain current is decreased by hole injection into the drain. Such transconductance behavior stems from the non-flat in-depth potential profile; Device A has a thick SOI layer and the body potential is easily modulated by the body contact potential, as suggested in Reference [3]. In Figure 15.4(a), at 30 K, on the other hand, the transconductance curves reveal two peaks, labeled P2a and P3a. P2a occurs at about $V_G = 1.2$ V and

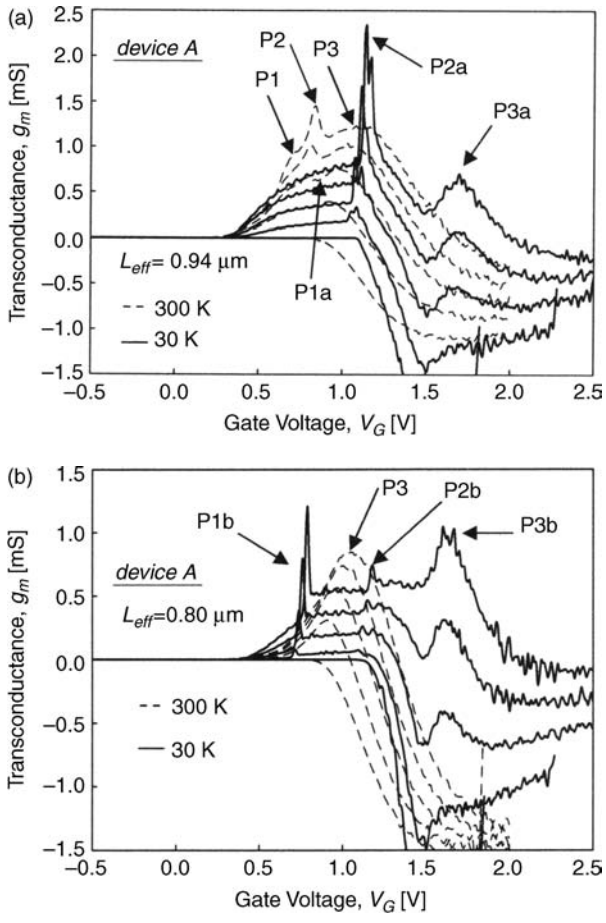

Figure 15.4 g_m–V_G characteristics of two different Devices A (DT-MOSFET) at 300 K and 30 K. (a) $L_{eff} = 0.94$ μm, (b) $L_{eff} = 0.80$ μm. Reprinted from *Cryogenics*, vol. 49, Y. Omura and T. Tochio, Significant aspects of minority carrier injection in dynamic-threshold SOI MOSFET at low temperature, pp. 611–614. Copyright 2009, with permission from Elsevier.

this peak appears because the gate current curve has a large shoulder at $V_G \sim 1.2$ V; the shoulder of the gate current curve appears after the first steep increase in the gate current (see Figure 15.5(a)). P3a occurs at about $V_G = 1.7$ V because the gate current curve has a second steep increase in gate current at $V_G \sim 1.5$ V (see Figure 15.5(a)). The first steep increase in the gate current curve represents hole injection into the source and the second steep increase is due to hole injection into the drain. This complex behavior of the transconductance is due to the freeze-out effect of the body and source/drain region.

In Figure 15.4(b), at 300 K, the transconductance curves reveal a single peak, labeled P3. P3 occurs at $V_G > 1$ V and appears, apparently, because the drain current is decreased by hole injection into the drain; this is the same mechanism as that seen in Figure 15.4(a). At 30 K, on the other hand, the transconductance curves display complex behavior. They evidence three

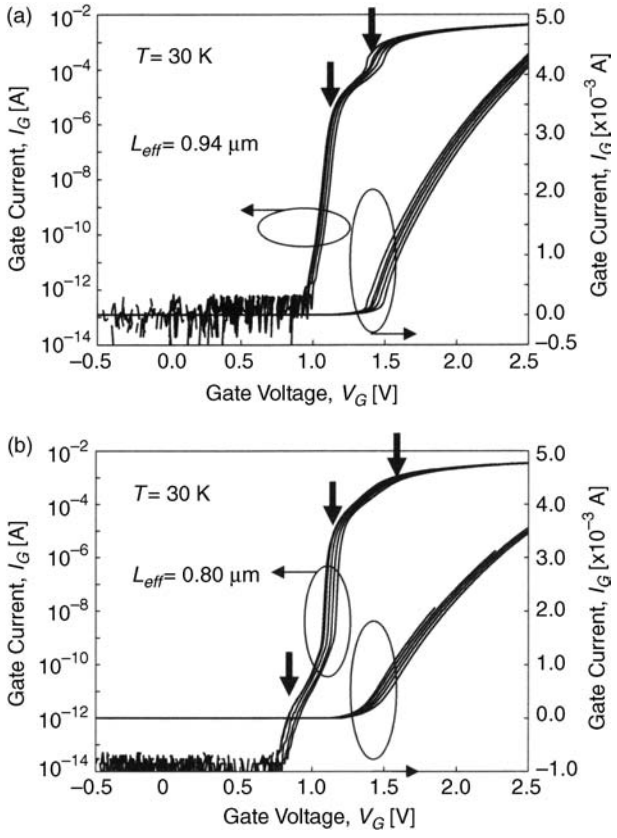

Figure 15.5 I_G–V_G characteristics of two different Devices A (DT-MOSFET) at 30 K. (a) L_{eff} = 0.94 μm, (b) L_{eff} = 0.80 μm. Reprinted from *Cryogenics*, vol. 49, Y. Omura and T. Tochio, Significant aspects of minority carrier injection in dynamic-threshold SOI MOSFET at low temperature, pp. 611–614. Copyright 2009, with permission from Elsevier.

peaks, labeled P1b, P2b, and P3b. The mechanisms underlying P2b and P3b are the same as those for P2a and P3a, as explained in Figure 15.4(a) (see Figure 15.5(b)). In contrast to the first two transconductance peaks, P1b occurs at $V_G \sim 0.8$ V. This peak is attributed to the steep increase in the gate current at $V_G \sim 0.8$ V as seen in Figure 15.5(b). It is anticipated that the latter gate current behavior stems from trap-assisted conduction of holes [8] at the SOI/BOX interface because the SIMOX substrate used in device fabrication has many point defects near the interface [9].

In addition, we investigated the impact of channel length (L_{eff}) on transconductance behavior at low temperature. Transconductance characteristics are shown as a function of the gate voltage for various channel length values in Figure 15.6. The transconductance curves basically have three peaks, labeled P1x, P2x, and P3x; the gate voltage values at which every peak appears are not sensitive to the channel length (L_{eff}). However, the following aspects should be noted: (i) P1x appears in short-channel devices, (ii) P2x appears in long-channel devices, and (iii) the appearance of P3x is insensitive to the channel length (L_{eff}). When trap-

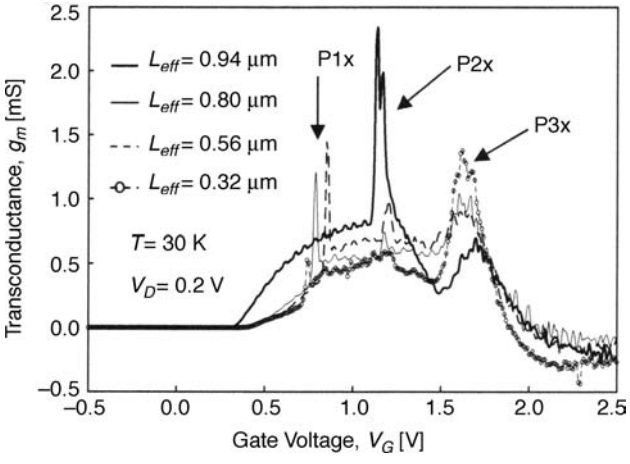

Figure 15.6 g_m–V_G characteristics of four different Devices A (DT-MOSFET) at 30 K. L_{eff} ranges from 0.94 μm to 0.32 μm. Reprinted from *Cryogenics*, vol. 49, Y. Omura and T. Tochio, Significant aspects of minority carrier injection in dynamic-threshold SOI MOSFET at low temperature, pp. 611–614. Copyright 2009, with permission from Elsevier.

assisted conduction is assumed, the behavior of P1x matches the known physics. Since the body-potential modulation of short-channel devices by hole injection from the body contact is very uniform, unlike long-channel devices, it is anticipated that the primary shoulder of the gate current characteristic observed at $V_G \sim 1$ V in Figure 15.5 merges with the second shoulder, resulting in the disappearance of P2x in short-channel devices.

15.3.3 Impact of SOI Layer Thickness on g_m *Characteristics*

Figure 15.7 shows the transconductance characteristics of Devices A and B as functions of the gate voltage at 30 K. Given the previous discussion, we can understand the transconductance behaviors shown in Figure 15.7 as follows. When the SOI layer is thin, the first shoulder appears at $V_G \sim 1$ V, not at $V_G \sim 0.8$ V. Therefore, only P2x is observed in Device B, not P1x. On the other hand, P3x is not distinctly observed in Device B because the gate current level is lower than that of Device A for $V_G > 1.5$ V.

15.4 Summary

This chapter demonstrated significant features of the low-temperature bipolar operation of the ultra-thin-body DT-MOSFET with various silicon-on-insulator (SOI) layer thicknesses. The drain current versus gate voltage and gate current versus gate voltage characteristics were evaluated at temperatures ranging from 300 K to 30 K and minority-carrier injection was characterized. Impacts of temperature, channel length, and silicon-on-insulator layer thickness on opposite drain current behavior were discussed by examining transconductance behavior. It was shown that the transconductance curves have at most three peaks, which are characterized as follows. The first peak corresponds to the gate-induced positive body bias at room temperature and yields a steep increase in gate current at low temperature. The second peak stems from the steep increase in gate current. A steep increase in another gate current

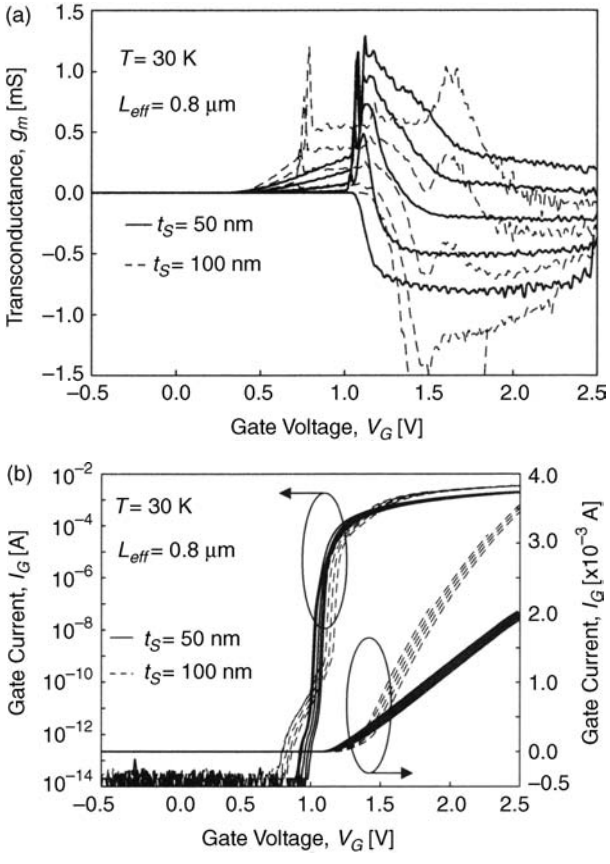

Figure 15.7 The g_m characteristics and I_G characteristics at 30 K for Devices A and B. $L_{eff} = 0.8\,\mu m$, (a) g_m characteristics, (b) I_G characteristics. Reprinted from *Cryogenics*, vol. 49, Y. Omura and T. Tochio, Significant aspects of minority carrier injection in dynamic-threshold SOI MOSFET at low temperature, pp. 611–614. Copyright 2009, with permission from Elsevier.

component appears in a range of sub-1-volt at low temperature; it is anticipated that this is responsible for trap-assisted conduction. The third peak appears due to the drain current decrease created by hole injection into the drain. At low temperature, the freeze-out effect of the body and source/drain region complicates the g_m characteristics.

However, when the opposite drain current is sufficiently suppressed, the results suggest that the DT-MOSFET can be applied to low-voltage and low-power digital LSIs that operate in low-temperature environments, such as satellites and spacecraft.

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Part Four
Circuit Applications

16

Subcircuit Models of SOI Lubistors for Electrostatic Discharge Protection Circuit Design and Their Applications

16.1 Introduction

Recent progress in device integration technology has been significant and the gate length of individual MOSFETs is already below 0.1 μm at the research level [1–3]. Given this background, the SOI MOSFET structure has attracted considerable attention since it can break down the technological barriers to device miniaturization. This structure has several advantages such as its suppression of the short-channel effect, low voltage and high-speed operation, and lower production costs [4,5]. Furthermore, the SOI structure is being exploited to build new application paradigms [6–8], such as optical waveguides [9] and light emission diodes [10]. Such developments are essential because broadband communication technology and high-frequency analog technology are urgently needed.

Throughout the history of semiconductor devices, one fundamental goal has been to clarify the basic characteristics of SOI devices [11]. However, few studies have examined the behavior of thin-film SOI Lubistors [12–15]. Since the SOI structure is expected to support digital applications [16–20], as well as analog applications [21], basic operation mechanisms must be elucidated.

In this chapter, SOI Lubistors [12,22] are investigated as a source of SOI ESD protection circuits. Equivalent circuit models for circuit applications are presented. Device simulations of the SOI Lubistors are performed to assist the analysis of operation mechanisms of Lubistors in detail. Equivalent circuit models that reproduce the device's characteristics are proposed for circuit simulations. The equivalent circuit models are applied to evaluate the performance of the ESD protection circuit.

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

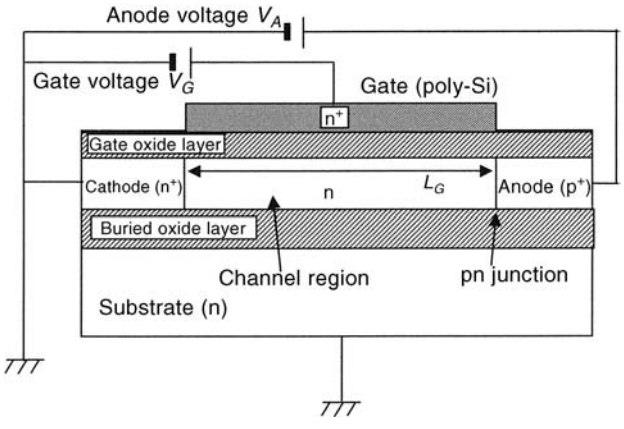

Figure 16.1 Schematic cross-section of an SOI Lubistor. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

16.2 Equivalent Circuit Models of SOI Lubistors and their Applications

16.2.1 Device Structure and Device Simulation

A schematic cross-section of an SOI Lubistor is shown in Figure 16.1. Although the basic device structure is analogous to that of SOI MOSFETs, the device differs in having a lateral p^+–n–n^+ junction structure. There are three main regions: anode, channel, and cathode. The device parameters of the devices are listed in Table 16.1.

Table 16.1 Device parameters of fabricated devices. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier

Parameters	Values [unit]
Gate length (L_G)	10, 20, 50 [μm]
Gate width (W_G)	50 [μm]
SOI layer thickness (t_s)	80 [nm]
Gate oxide layer thickness (t_{ox})	80 [nm]
Buried oxide layer thickness (t_{BOX})	380 [nm]
SOI body doping concentration (n-type)	1×10^{15} [cm^{-3}]
Substrate doping concentration (n-type)	1×10^{15} [cm^{-3}]
Gate doping concentration (n-type)	1×10^{20} [cm^{-3}]
Anode doping concentration (p-type)	1×10^{20} [cm^{-3}]
Cathode doping concentration (n-type)	1×10^{20} [cm^{-3}]

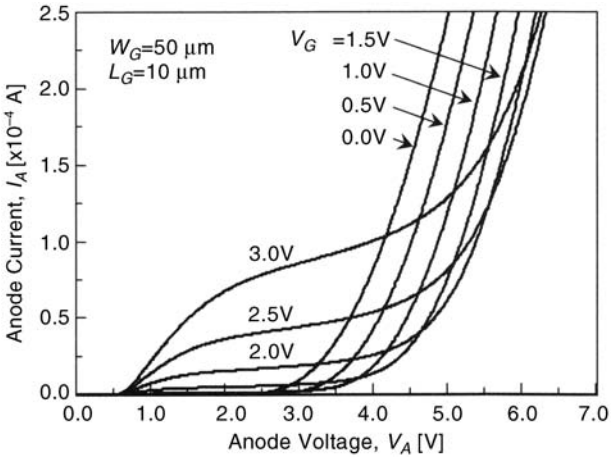

Figure 16.2 Current versus voltage characteristics of a fabricated device with a 10 μm gate. Non-saturation current characteristics appear under low gate voltages and high anode voltages. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

Various applications of SOI Lubistors can be expected because they offer both the non-saturation current characteristics of pn-junction and saturation current characteristics of MOSFETs. The author has demonstrated a possible application to a neural logic element [14], while S. Voldman with IBM proposed their application to ESD protection circuits [20,23–25]. However, device operation mechanisms and equivalent circuit models, which are necessary for realizing circuit applications, have not been studied in sufficient detail. In this section, the operation mechanisms of the SOI Lubistor are examined in detail by a commercial semiconductor device simulator [26] (ISETCAD).

In trial simulations, physical parameters of the device were adjusted to match the *I–V* characteristics of actual devices. Representative *I–V* characteristics of an actual device with L_G of 10 μm are shown in Figure 16.2. Non-saturation current characteristics appear under the condition of low gate voltages and high anode voltages. An identical device structure (two-dimensional) was assumed for device simulations, and simulations were carried out under bias conditions identical to the experiments. The simulations used the materials' default values for physical parameters, such as minority carrier lifetime and low-mobility parameters (see Table 16.2).

Table 16.2 Physical parameters in device simulations. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier

	Default values		Modified values	
Physical parameters [unit]	Electrons	Holes	Electrons	Holes
Lifetime [s]	10^{-7}	10^{-7}	10^{-12}	10^{-12}
Low-field mobility [cm^2/V s]	1417	470	100	100

Drift-diffusion equations were used for transport analysis and the following physical models were also applied [26]:

1. Shockley–Read–Hall statistics and Auger recombination models [27].
2. Mobility model including doping dependence, high-field saturation of carrier velocity, and degradation due to the electric field normal to the silicon–oxide interface [28].
3. Effective intrinsic carrier density model based on Slotboom's bandgap narrowing model [29].

Simulation results of the device with $L_G = 10\,\mu$m are shown in Figure 16.3(a). They are quite different from the characteristics of the actual device; the current does not saturate in the

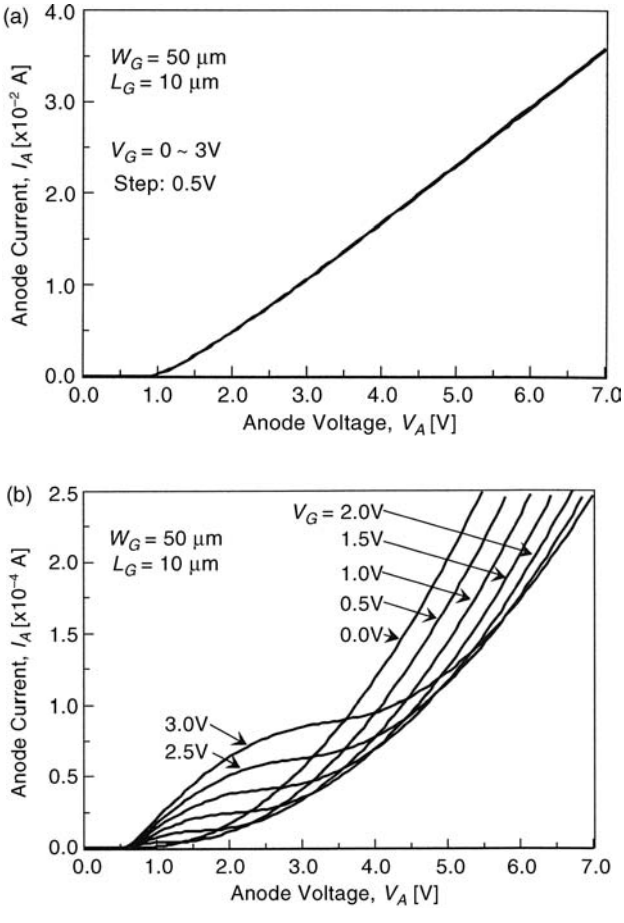

Figure 16.3 Simulated current versus voltage characteristics. (a) Default physical parameters are assumed. (b) Modified physical parameters are assumed. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

medium anode voltage region and the magnitude of the simulated anode current is 100 times as large as that of the experimental result. Furthermore, the anode current is independent of the gate voltage. We examined the current distribution inside the device; holes and electrons injected into the channel region from the anode and cathode, respectively, pass through the channel region virtually without recombination. The characteristic difference is due to the very long diffusion length assumed in the simulated device. According to pn-junction theory, the diffusion length of carriers is given by the square root of the product of the diffusion constant and the lifetime [27]; the diffusion constant is tied to the carrier mobility by Einstein's relation in the equilibrium state. The actual devices used for the comparison had many defects (dislocations) because the high oxygen-dose SIMOX wafer was used for device fabrication [30]. Therefore the quality of the SOI layer is inferior to modern production levels and both lifetime and mobility are smaller compared to those achievable with current technologies. It follows that the difference between the experiment and the simulation results should be compensated by adjusting the simulated lifetime and mobility. The generation and recombination of carriers in semiconductors is governed by Shockley–Read–Hall (SRH) statistics. Accordingly, the refined simulations used adjusted physical parameters, the lifetime of 10^{-12} s and the mobility of $100\,\mathrm{cm^2/V\ s}$ for both electrons and holes (see Table 16.2). Improved simulation results are shown in Figure 16.3(b). Simulated *I–V* characteristics match the experimental results well; namely, the physical model must be accurately described if we are to reproduce the experimental current–voltage characteristics.

16.2.2 Equivalent Circuit Models

After conducting many simulations, we have found that the characteristics described above can be reproduced by conventional device models [26]. This allows us to propose the equivalent circuit model shown in Figure 16.4(a) for the SPICE circuit simulation in which the standard circuit components of the SPICE simulator are used.

Two current components yielding the *I–V* characteristics of the SOI Lubistor are represented as the current flow component P1 and the current flow P2 in Figure 16.4(a). The gate electrode and the drain electrode of the pMOSFET are connected in common. In this configuration, the pMOSFET operates in the current saturation condition. The voltage source, connected between the pMOSFET and the cathode terminal, generates voltage kV_G, which is proportional to the gate voltage, where k is the fitting parameter. The simulated *I–V* characteristics of the equivalent circuit model are shown in Figure 16.5, together with those obtained by device simulation. Good agreement is achieved between the experimental and simulation results.

16.3 ESD Protection Circuit

Electrostatic discharge (ESD) is a fast transition phenomenon that involves a large current flow over time periods ranging from a few ns to 1 μs [31,32]. If an integrated circuit with no protection circuit experiences ESD, large currents of the order of several amperes can flow through the device, leading to fatal damage. Generally speaking, the input and output (I/O) circuits are quite sensitive to external disturbances. The I/O buffer and internal circuits can be protected from ESD by placing an ESD protection circuit in parallel to the I/O circuit. The ESD protection circuit acts as a voltage clamp and current shunt.

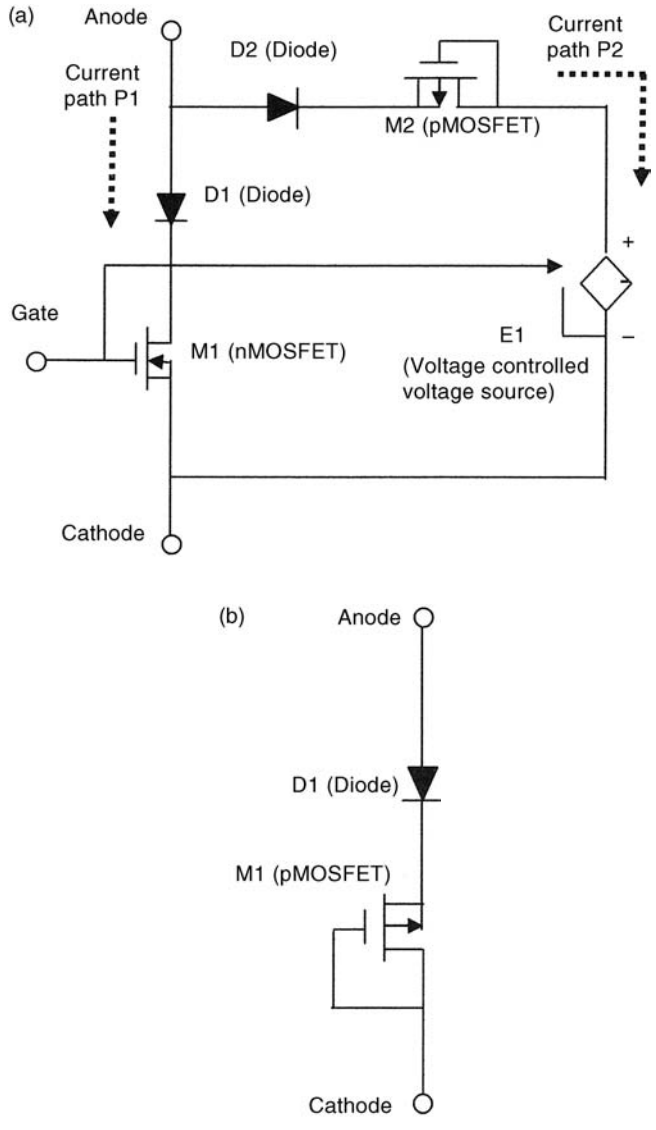

Figure 16.4 Proposed equivalent circuit model of the SOI Lubistor. (a) Modified physical parameters are assumed. (b) Default physical parameters are assumed. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

Effective ESD protection devices are needed if SOI technology is to yield advanced high-performance complementary metal oxide semiconductor (CMOS) integrated circuits. A major problem is the poor thermal conductivity of the buried oxide layer, which makes it difficult to handle the large current flows expected. Phenomena specific to SOI devices, such as the

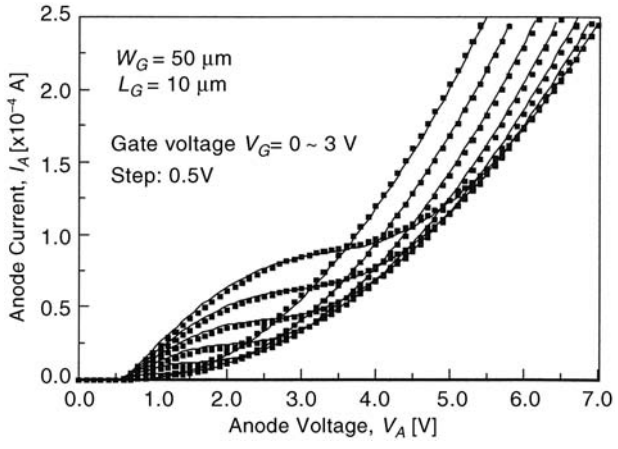

Figure 16.5 Current versus voltage characteristics obtained by the equivalent circuit model shown in Figure 16.4(a). Solid lines are experimental results and dots are the simulation results of SPICE. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

floating body effect and the parasitic bipolar effect, result in lower breakdown voltages compared to bulk devices. It is for this reason that some reports equate the ESD robustness of SOI technology to only half that of conventional bulk-Si technology [33,34]. Furthermore, the thick field oxide or thyristor technology popular in bulk-Si devices is not easily achieved in SOI devices. Therefore, a new ESD protection method that suits SOI technology is needed. As already mentioned, Voldman *et al*. proposed an ESD protection method that uses SOI Lubistors [16,20], where the ESD protection designs established for bulk-Si technology can be easily applied to SOI technology [22]. They assert that shifting from the bulk-Si technology to the SOI technology eliminates interaction between the integrated circuit elements and also eliminates unpredictable circuit behavior. The use of SOI technology also makes the ESD protection structure more scalable. However, they failed to provide design guidelines and details of protection behavior under ESD events.

We examine their protection circuit using the SPICE circuit simulator. The behavior of the ESD protection circuit under ESD events is investigated in combination with the electro-thermal device simulation of semiconductor elements. Since the circuit simulations give us the dynamic behavior of node voltages and currents, the identification of weak points is possible.

The ESD protection circuit proposed by Voldman *et al*. [20,23–25] is shown in Figure 16.6. The SOI Lubistors and MOSFETs are used as circuit elements. The SOI Lubistors are used as a clamp diode and the charge set up by the ESD event is shunted to the power line so that the signal line does not receive excessive voltages. The snapback behavior of the grounded-gate nMOSFET protects the circuit, as is explained later. A pass transistor and two grounded-gate nMOSFETs are connected to the CMOS inverter, which acts as an input buffer at the end of this circuit.

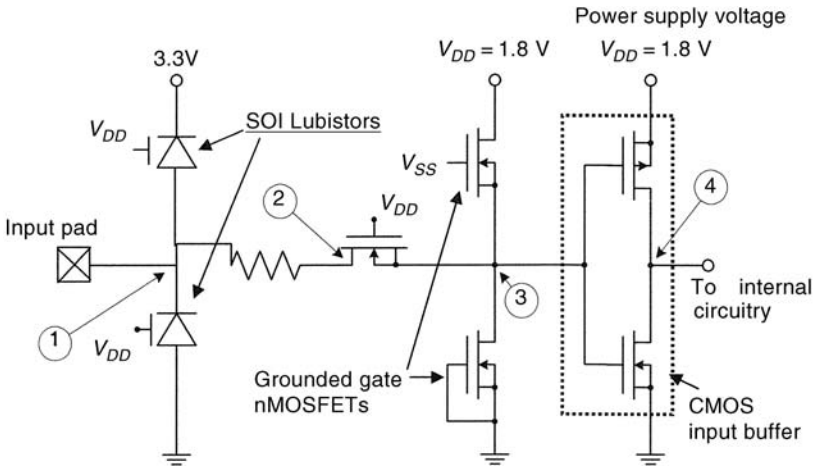

Figure 16.6 SOI ESD protection circuit proposed by Voldman *et al*. [20,23–25]. The circled numbers indicate examined nodes. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

We employed the following procedure in circuit simulations since ESD events are not normal operation events. Two-step simulations were performed to follow the reliable behavior of the MOSFETs and SOI Lubistors in the ESD protection circuit. The first step was to carry out drift-diffusion simulation without the self-heating effect and avalanche multiplication and obtain the DC characteristics of the components. The device model parameters for the SPICE simulator were then selected so as to match the DC characteristics obtained by device simulations. The second step was to carry out hydrodynamic simulation with the self-heating effect and avalanche multiplication using the device simulator, and investigate the behavior of the devices under ESD. By applying the present two-step simulations, we can extract the influence of very fast transient phenomena from actual dynamic operation. We can obtain significant data from simulation results in order to overcome reliability issues. The following circuit simulation of the whole ESD protection circuit was carried out after the device model parameters for the SPICE simulator were readjusted according to the hydrodynamic simulation results.

16.4 Direct Current Characteristics of the ESD Protection Devices and Their SPICE Models

In order to evaluate DC performance of the devices in the ESD protection circuit, the characteristics of MOSFETs and SOI Lubistors were simulated by using the semiconductor process and device simulator [26]. The DC characteristics were analyzed by solving the drift-diffusion equation. In order to reduce the computation time, self-heating and impact ionization were not considered. The same simulation technique was applied to the SOI Lubistors. The lifetime and the mobility of minority carriers were lowered in some

simulations of the SOI Lubistors to reproduce the experimental results; the manipulation degraded the anode current. In the following simulations of SOI Lubistors, therefore, we carried out two simulations; one used the lowered lifetime and lowered mobility of minority carriers, the other used the default values. On the other hand, we simulated the performance of the MOSFETs using the default parameter values defined in the device simulator because MOSFET is not as sensitive as most parameters, except for the mobility. The meaning of the physical parameter values for ESD protection is discussed in the following analysis.

The geometries of the MOSFETs and the SOI Lubistors were determined on the basis of 0.18 μm SOI CMOS technology [20,25]. Characteristics of all devices shown hereafter are for an assumed gate width of 1 μm. The simulations were carried out for two different buried oxide film thickness (100 nm or 400 nm). All devices were designed assuming a p-type substrate. The MOSFET threshold voltage ranged from 0.3 V to 0.4 V by adjusting the body doping concentration. The threshold voltage of 0.4 V was obtained for both nMOSFET and pMOSFET when the body doping concentration was $9 \times 10^{17}\,\mathrm{cm}^{-3}$. Parameter values of the simulated devices are shown in Table 16.3. Here, we assume that the SOI Lubistor has a thick gate oxide layer (80 nm) because the device experiences a very high voltage at the gate electrode. On the other hand, we assume that CMOS devices have a thin gate oxide layer because a high-speed operation is required. In fabrications, the gate oxide layer of the SOI Lubistor is formed first, followed by the thin gate oxide layer of CMOS devices; this fabrication step is frequently applied to modern ULSIs.

Table 16.3 Device parameters used in ESD circuits. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier

(a) MOSFETs	
Parameters	Values [unit]
Gate length (L_G)	0.18 [μm]
SOI layer thickness (t_s)	100 [nm]
Gate oxide layer thickness (t_{ox})	3.5 [nm]
Buried oxide layer thickness (t_{BOX})	100, 400 [nm]
SOI body doping concentration (n-type)	9×10^{17} [cm^{-3}]
Substrate doping concentration (n-type)	1×10^{15} [cm^{-3}]
Gate doping concentration (n-type)	1×10^{20} [cm^{-3}]
Source/drain doping concentration (n-type)	1×10^{20} [cm^{-3}]
(b) SOI Lubistors	
Gate length (L_G)	0.5 [μm]
SOI layer thickness (t_s)	100 [nm]
Gate oxide layer thickness (t_{ox})	80 [nm]
Buried oxide layer thickness (t_{BOX})	100, 400 [nm]
SOI body doping concentration (n-type)	1×10^{15} [cm^{-3}]
Substrate doping concentration (n-type)	1×10^{15} [cm^{-3}]
Gate doping concentration (n-type)	1×10^{20} [cm^{-3}]
Anode doping concentration (p-type)	1×10^{20} [cm^{-3}]
Cathode doping concentration (n-type)	1×10^{20} [cm^{-3}]

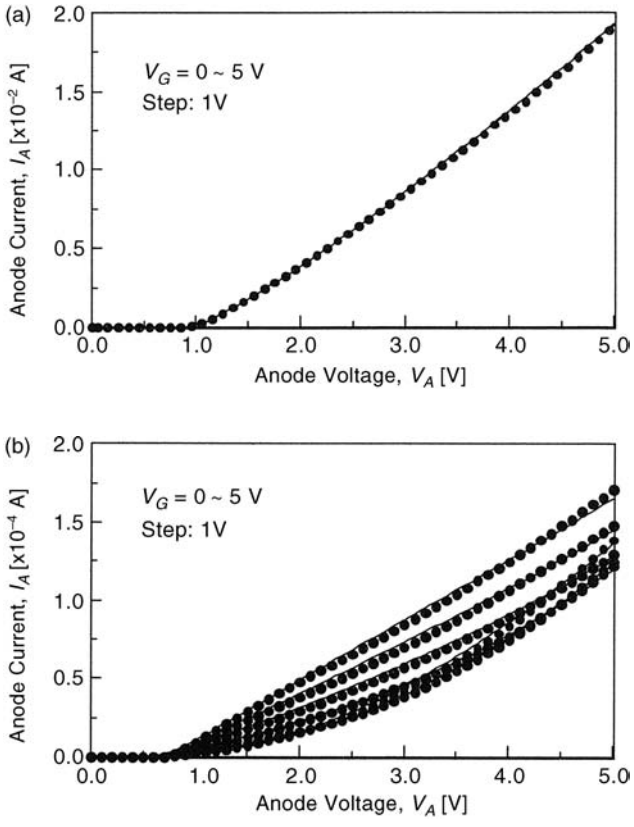

Figure 16.7 Simulated current versus voltage characteristics of the equivalent circuit models for the SOI Lubistor. Solid lines are obtained by device simulations and dots were yielded by SPICE simulations. (a) Default physical parameters are assumed. (b) Modified physical parameters are assumed. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

The device simulation results clearly show that the difference in buried oxide layer thickness only slightly influenced the DC characteristics (not shown here). Accordingly, the characteristics of the device with a buried oxide thickness of 100 nm are shown below. The simulation results for the two physical parameter values are shown for the SOI Lubistors in Figure 16.7(a) and (b).

These DC characteristics were used for extracting the model parameters for SPICE simulations. The Level 3 MOS model of the SPICE simulator was used for modeling the MOSFETs and the Level 1 MOS model was used to create the subcircuit model of the SOI Lubistors [35]. The simulation results of the SOI Lubistor, see Figure 16.7(a), suggest that the equivalent circuit model can be simplified owing to the lack of any gate voltage dependency; default physical parameters are assumed. A possible simplified equivalent circuit model is shown in Figure 16.4(b). Here, we connect the MOSFET and the diode in series because we

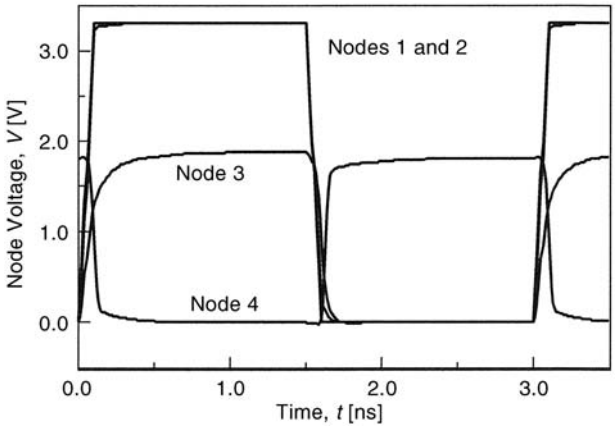

Figure 16.8 Time evolutions of node voltages. Node numbers are defined in Figure 16.6. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

think that the Lubistor does not work as an ideal diode, but a diode with a series resistance. The MOSFET works as a series resistance in the subcircuit shown in Figure 16.4(b). The optimized SPICE models (denoted by dots) are compared to the device simulation results (denoted by solid lines) in Figure 16.7 for the SOI Lubistors. All simulation results show reasonable agreement with the experimental results. The parasitic capacitances of the device play an important role in the transient analysis. Here, they were estimated by the method used for bulk technology, and they were corrected by comparing them to the transient device simulation results [36]. In the following, default physical parameters and modified parameters for minority carrier lifetime and mobility shown in Table 16.2 are used for comparison in simulations of characteristics of the SOI Lubistors.

The ESD protection circuit is composed of devices with the optimized device parameters for the SPICE model. The gate widths of the input buffer CMOS device were set large enough to drive the load capacitance connected behind it; the nMOSFET (pMOSFET) gate width is 10 (21.4) μm. A pass transistor (nMOSFET) has a 10-μm-long gate width and the threshold voltage of 0 V; the threshold voltage was adjusted by the body doping concentration. In order to examine practical circuit operation, a rectangle pulse of 330 MHz was applied to the circuit and a transient analysis was carried out. The time evolution of each node voltage is shown in Figure 16.8. The delay time of each device is not a significant problem in this case, and the input buffer operates normally.

16.5 ESD Event and Performance Evaluation of an ESD Protection Circuit

The shape of the ESD pulse is modulated by the impedance of the pulse's source. This work adopts the human body model (HBM), which is the most general model. The HBM represents the electrostatic discharge from a charged human body. This process is analyzed

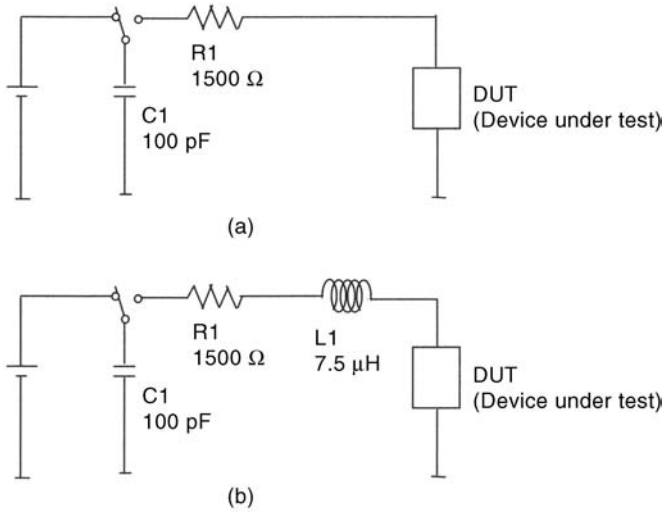

Figure 16.9 Equivalent circuit model of the HBM ESD model. (a) Standard HBM equivalent circuit model. (b) The improved circuit model. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

using the equivalent circuit model shown in Figure 16.9(a). Capacitor C1 represents the equivalent capacitance of the human body and resistor R1 represents the resistance of human skin. The charge accumulated in capacitor C1 is discharged through the resister and the device under test. When the HBM test voltage is 2 kV, the initial voltage of the capacitor before discharge is 2 kV. In order to realize a practical discharge waveform, we connected an inductor L1 in series to resistor R1; the improved equivalent circuit is shown in Figure 16.9(b). The simulated discharge current for the 2 kV HBM pulse is shown in Figure 16.10. The current pulse has a maximum amplitude of 1.2 A over several hundred nanoseconds. Generally speaking, commercial integrated circuits require an ESD robustness of 2 kV to 4 kV.

During the ESD event, semiconductor devices exhibit unnatural behavior because the ESD event is a transient process that entails high voltage and high current, as shown in Figure 16.10. Therefore, when the ESD event is simulated, it is necessary to consider the very high current behavior of the semiconductor device. Since the semiconductor device model of the SPICE simulator does not detail such high current characteristics, we must think that SPICE simulation results are not reliable in some cases. Therefore, we must create a suitable equivalent circuit model that can reproduce the high current behavior of devices. The key requirement is to consider the self-heating effect and avalanche multiplication simultaneously. As mentioned before, we carried out two-step simulations; in the final circuit simulations, we used device parameters in which hydrodynamic simulation results are taken into account. This approach was used to investigate the behavior of semiconductor devices under ESD and to guarantee circuit reliability.

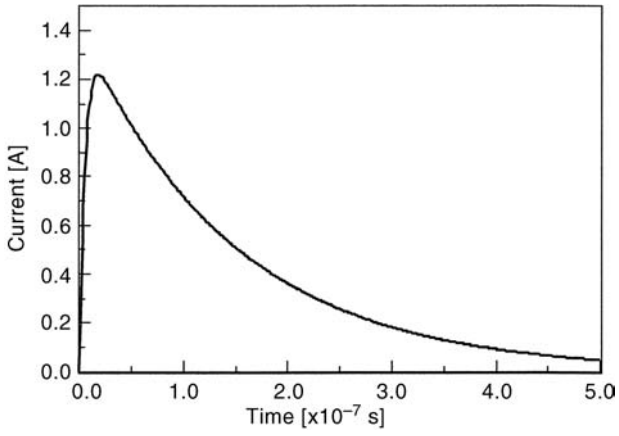

Figure 16.10 Time evolution of 2 kV HBM ESD source pulse. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

In the hydrodynamic simulation for the SOI Lubistor, slight differences could be seen between the DC characteristics and the transient characteristics, except for small snapback characteristics. Therefore, the equivalent circuit model of the SOI Lubistor extracted from the DC characteristics was slightly modified by taking account of hydrodynamic simulation results. Before evaluating the ESD behavior of the full ESD protection circuit, the worn-out phenomenon of individual devices was investigated by using the device simulator and the modified SPICE model; here *worn-out* means the fatal thermal destruction in devices. The thermal destruction usually takes place when the device temperature becomes higher than the intrinsic temperature (T_i), where the intrinsic temperature is the temperature at which the intrinsic carrier concentration equals the background doping concentration [37]. Therefore, most device simulations were performed in order to discover what ruled the worn-out criterion of the device.

In general, there are two crucial factors associated with the destruction of semiconductor devices under ESD. One is the breakdown of the gate oxide film by the high electric field and the other is heat-induced destruction. In conventional semiconductors, the destruction of integrated circuits assumes that the HBM is dominated by the thermal effect because the ESD protection circuit clamps the ESD-induced voltage before the gate oxide film is destroyed by the high field. Given the continued progress in downscaling of MOSFETs, gate oxide film thickness, and thus the breakdown voltage of the gate oxide film, continues to fall. Thus ESD protection devices fabricated by deep submicrometer technology must offer low turnover voltages and low holding voltages. Since it is difficult to detect the gate oxide film breakdown in the present simulation and there are very few papers addressing the gate oxide breakdown under ESD, we tentatively define the breakdown field to be 10 MV/cm. In the case of a 3.5-nm-thick gate oxide film, the breakdown criterion of the gate oxide film is assumed to be 3.5 V.

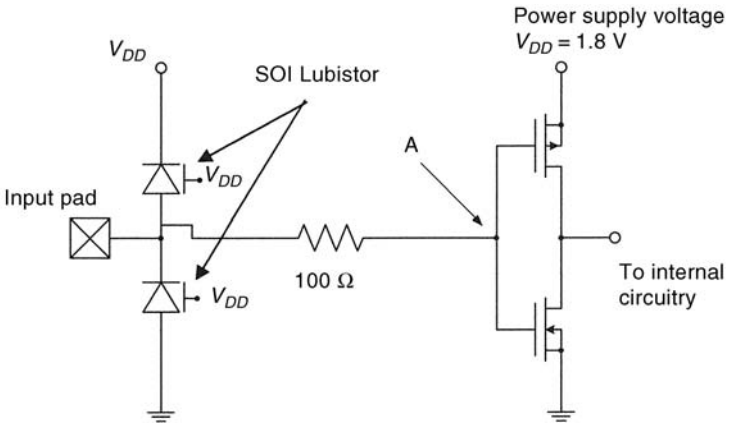

Figure 16.11 Simplified ESD protection circuit for the SOI Lubistor. Node 'A' is tested here. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

As mentioned above, the thermal destruction process becomes critical when the local temperature exceeds the intrinsic temperature (T_i). When the local temperature of a semiconductor device exceeds T_i the second breakdown occurs for the MOSFET case. The second breakdown has to be avoided because the permanent destruction of the device occurs by a large current filament. Three heating mechanisms are present in semiconductor devices: Joule, recombination, and Thomson heating [38]. In device simulations of SOI Lubistors and MOSFETs, Joule heating is usually dominant in all areas of the device except at the junctions of SOI Lubistors, where recombination heating is dominant. Thomson heating is insignificant compared to the other two mechanisms. Though recombination heating is important, for simplicity we consider only Joule heating. Since this makes device heating proportional to power consumption (P), low holding voltages and low on-resistances decrease the heating effect for the same current flow.

According to the above consideration, we compared the characteristics of two SOI Lubistors with different physical parameter values. The performance of the simple clamp diode circuit shown in Figure 16.11 with two different physical parameters as estimated by the SPICE simulator (Table 16.2) was assessed. The gate width of the SOI Lubistor was 400 μm. The time evolution of node voltage (the node is denoted by 'A' in Figure 16.11) at the input pad for a 1500-V-positive HBM pulse is shown in Figure 16.12. The device with reduced lifetime and reduced minority carrier mobility experiences a higher node voltage. This is because the reduction in lifetime and minority carrier mobility results in a low anode current. The reduction in lifetime and mobility increases the on-resistance, resulting in a higher holding voltage at the device. This leads not only to enhanced self-heating but also to occasional breakdown of the gate oxide film. Therefore, devices with short lifetimes and small minority carrier mobility are not suitable for realizing ESD protection circuits. Consequently, the model of the SOI Lubistor considered hereafter for ESD analysis offers a long lifetime and

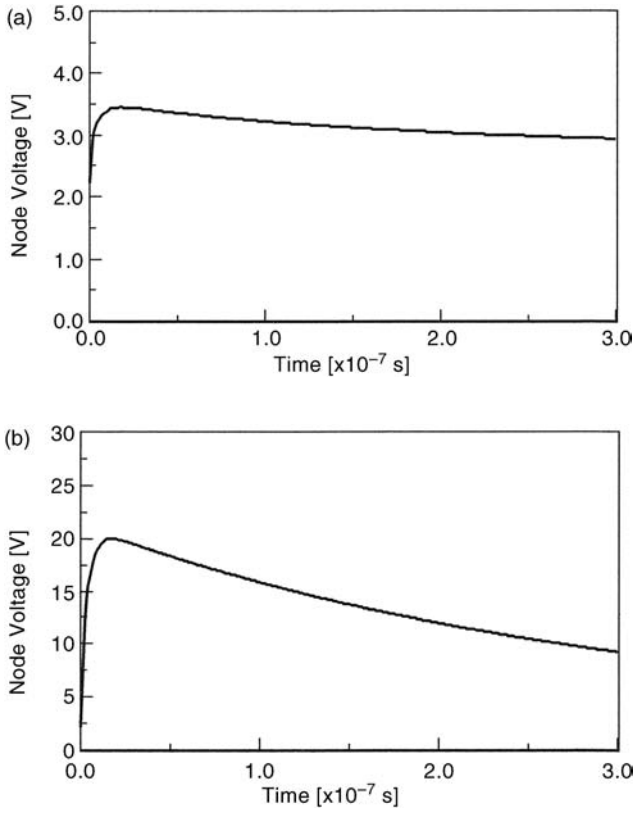

Figure 16.12 Simulation results of the proposed ESD protection circuit: two different physical parameters. Node 'A' is tested here. (a) Default physical parameters are assumed. (b) Modified physical parameters are assumed. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Subcircuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

significant minority carrier mobility; the default physical parameters in Table 16.2 are assumed.

The intrinsic carrier density, n_i, increases rapidly with temperature. At high temperatures, therefore, thermal generation can be the dominant process of carrier generation. Thus, the intrinsic temperature, T_i, depends on impurity concentration, and increases with the impurity concentration. The impurity density in the simulated device is lowest in the channel region. The intrinsic temperature of the channel region of the SOI Lubistor (n-type, $1 \times 10^{15}\,\mathrm{cm}^{-3}$) is about 500 K, and the intrinsic temperature of the channel region of the MOSFET (p-type, $1 \times 10^{17}\,\mathrm{cm}^{-3}$) is about 1000 K. In order to investigate the thermal destruction of the devices, various HBM pulses were applied to SOI Lubistors and MOSFETs. The application of a 15 V/μm HBM pulse to the SOI Lubistor forces the local temperature to reach the intrinsic temperature. When a 13 V/μm HBM pulse is applied to the MOSFET, the local temperature

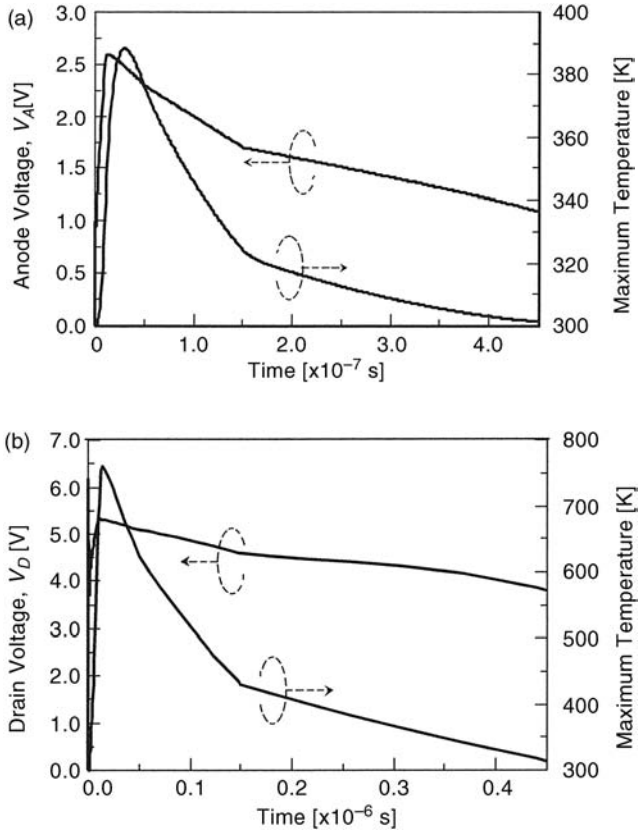

Figure 16.13 Simulated time evolution of the anode voltage of the SOI Lubistor and nMOSFET. The HBM source pulse of 10 V was applied to the device under test; gate width is 1 μm. (a) SOI Lubistor, (b) nMOSFET. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

reaches the intrinsic temperature. The relationship between the HBM metric and the maximum current is given by $I_{HBM} = V_{HBM}/1500$, where I_{HBM} and V_{HBM} are the maximum current and the maximum voltage that induce device destruction, respectively. From this relationship, when the current of 10 (8.7) mA/μm flows into an SOI Lubistor, the device should be destroyed. In an SOI Lubistor, the temperature of the entire channel region is raised by the heating that occurs at the two junctions. On the other hand, in a MOSFET, the temperature rise occurs in the vicinity of the reverse-biased drain junction due to Joule heating. The buried oxide did not affect the local temperature in the thickness range examined here. This is because the accumulated thermal power is dissipated to the surrounding materials over a period of 20–30 ns. Figure 16.13 shows the time evolution of the terminal voltage and maximum temperature of the SOI Lubistor and a MOSFET after the 10 V/μm HBM pulse. Here device parameters shown in Table 16.3 are used, except for the gate width in simulations; it is assumed the gate width is 1 μm.

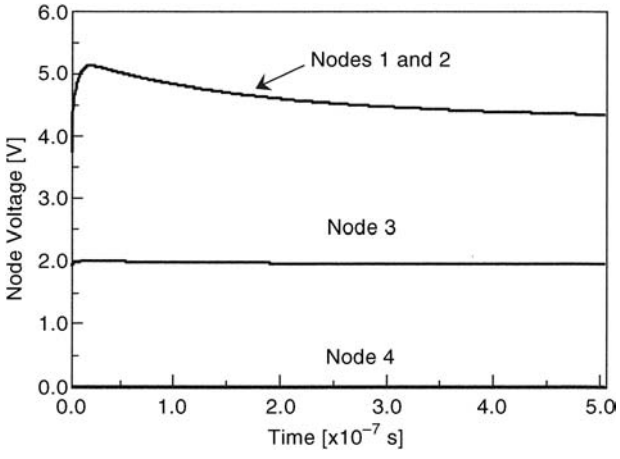

Figure 16.14 Time evolution of node voltages in the proposed ESD protection circuit shown in Figure 16.6. Reprinted from *Solid-State Electronics*, vol. 47, S. Wakita and Y. Omura, Sub-circuit models of silicon-on-insulator insulated-gate pn-junction devices for electrostatic discharge protection circuit design and their applications, pp. 1943–1952. Copyright 2003, with permission from Elsevier.

Since the destruction metrics of the individual devices were determined, HBM pulses were applied to the ESD protection circuit shown in Figure 16.13, and its circuit performance was evaluated. Figure 16.14 shows the time evolution of voltage at each internal node for the 2 kV HBM pulse. The gate width of the SOI Lubistor was 400 μm and that of the grounded-gate nMOSFET was 100 μm. Almost all HBM-induced current flows through the SOI insulated-gate pn-junction device connected to the V_{DD} power supply line; the terminal voltage was shunted to the V_{DD} power supply line. In this situation, the pass transistor and the grounded-gate nMOSFET did not induce snapback. The pass transistor limits the current that flows into the following CMOS gate because the pass transistor operates in the saturation region. Therefore, the gate voltage of the CMOS buffer does not exceed the power-supply voltage providing the pass transistor does not trigger snapback; in other words, the input buffer is protected. From previous device simulations, we can state that the SOI Lubistor has an HBM immunity of about 15 V/μm and can handle currents of up to 10 mA/μm. A simple calculation shows that a device with a 400-μm gate width can sustain a 6-kV HBM pulse.

We note that gate oxide breakdown may be a more serious problem than thermal loads. In Figure 16.14, the maximum voltage of node 2 is about 5.2 V; the maximum voltage of about 3.4 V is applied to the gate oxide film of the pass transistor because its gate voltage is 1.8 V. Since this is close to 3.5 V, the destruction criterion of the gate oxide film, the destruction of the gate oxide film may limit ESD protection circuit performance when a sub-3.5-nm-thick oxide film is used in the device.

The above simulation results show that lowering the holding voltage of the ESD protection circuit is necessary to improve its performance. We can improve the current–voltage characteristics of the SOI Lubistor by reducing its gate length; $L_G = 0.18$ μm. The body doping concentration should be increased to $9 \times 10^{17}\,\mathrm{cm}^{-3}$ in order to improve the intrinsic temperature (T_i). The anode current of this device structure is three times as large as that

shown in Figure 16.7(a). In the HBM test, the local temperature did not exceed the intrinsic temperature for the current pulse of 30 V/μm.

We developed a SPICE model of this ESD protection circuit and subjected it to an HBM test; the result was that ESD protection circuits that have devices with gate widths of 400 μm offer an HBM immunity of 8 kV. This is twice the general HBM metric of 2 kV to 4 kV, so the ESD protection circuit has satisfactory performance. This ESD protection circuit is a promising way to boost the further development of SOI technology.

16.6 Summary

This chapter has proposed equivalent circuit models of SOI Lubistors for circuit simulations. It has been clarified that device characteristics can be explained on the basis of complex operations performed within pn-junction, nMOSFET, and pMOSFET components. The circuit models proposed here on the basis of the DC operation model were used to evaluate an enhanced electrostatic discharge (ESD) protection circuit.

Equivalent circuit models of the devices were described that consist of standard SPICE circuit elements. The models, based on the operation mechanism, have been investigated by a device simulator, and in a trial study they were applied to evaluate the performance of the SOI ESD protection circuit. It has been shown that SOI Lubistors have sufficient performance to realize effective ESD protection devices.

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17

A New Basic Element for Neural Logic Functions and Capability in Circuit Applications

17.1 Introduction

Neural logic devices and circuits have been extensively studied [1,2], and recently a νMOS transistor and its logic circuits were proposed [3,4]. While quantum effect devices may contribute to new functional applications [5–7] and many other devices have also been examined [8,9], they are still somewhat immature in terms of practical applications.

Hopefully, neural logic devices should be compatible with conventional CMOS logic circuits to utilize the well-known designs available with silicon LSI technology. It is considered that the νMOS transistor, which shows a neuron-like operation (sum of product), is one of the desirable solutions. However, it can be considered that the νMOS transistor does not reflect a synaptic operation flexibly.

In this chapter, a new neural logic device, which is recently proposed with a synaptic function [10], and simulation results of some circuit operations are described and discussed in detail. The device, the Lubistor [11,12], can be used to realize a signal pre-processing, whose operation is very similar to synapse, for key neural logic operations. Since the operation of the Lubistor is composed of the tetrode mode and the triode mode, flexible logic operations can be designed. The following sections discuss basic operations and possible function feasibility.

17.2 Device Structure, Model, and Proposal of a New Logic Element

17.2.1 Device Structure and Fundamental Characteristics

A cross-sectional view of the Lubistor and typical experimental *I–V* characteristics are shown in Figures 17.1 and 17.2, respectively. In Figure 17.2, the silicon layer thickness (t_s) is 10 nm, the gate oxide layer thickness (t_{ox}) is 5 nm, the buried oxide layer thickness (t_{BOX}) is 110 nm, the gate length (L_G) is 5 μm, and the gate width (W_G) is 10 μm [13]. When the bias

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

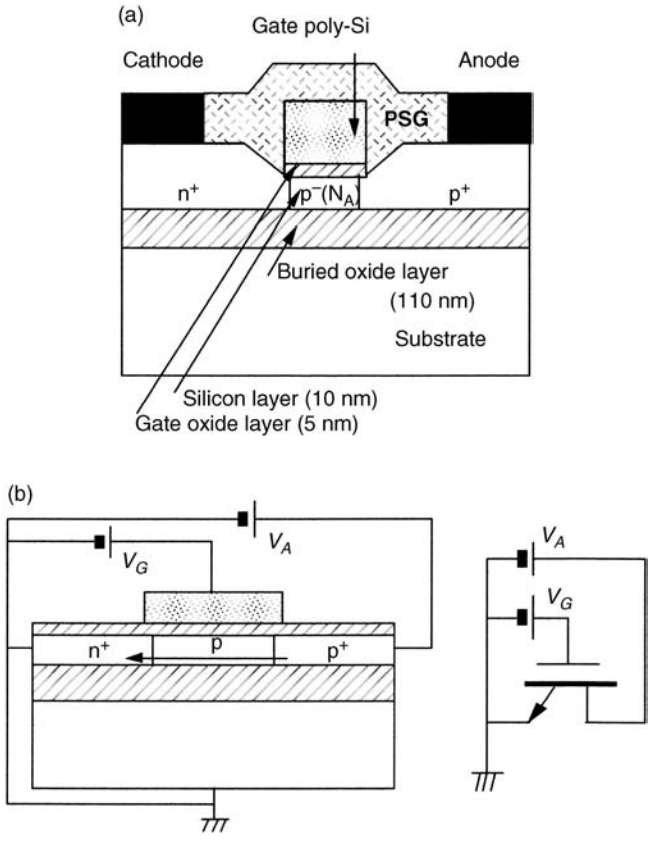

Figure 17.1 Schematic of the device structure and its symbol. (a) Schematic of the structure of the Lubistor. (b) Bias configuration for device operation and symbol of the device. Copyright 2002. The Institute of Electronics Engineers of Korea. [Y. Omura, A new basic element for neural logic functions and capability in circuit applications, *Journal of Semiconductor Technology and Science*, vol. 2, pp. 70–81, 2002.] © 1999 IEEE. Reprinted, with permission, from Y. Omura, Neuron firing operations by a new basic logic element, *IEEE Electron Device Letters*, vol. 20, pp. 226–228, 1999.

configuration is as shown in Figure 17.1(b), the Lubistor shows a tetrode characteristic at high gate voltages (V_G) and a modified triode characteristic at low gate voltages [11,12]. Thus, the Lubistor can have two natures: one is the feature of a MOSFET/SOI device at high gate voltages and the other is the feature of a forward-biased pn-junction device at low gate voltage. It is an important point that the anode current is suppressed as the gate voltage (V_G) increases at high anode voltages [11–13]; the negative transconductance is observed in this bias region. Therefore its operation can be symbolized as shown on the right-hand side of Figure 17.1(b). In the *OFF* state, the Lubistor has a built-in pn junction at the cathode side. In the *ON* state, however, the Lubistor has an actual pn junction, which is formed by the electron inversion layer and the p^+ anode, at the anode side. Since the Lubistor has a pn junction, the anode current is observed clearly at V_A larger than 0.7 V, which is different from the conventional MOSFET. At anode voltages that are a little bit high, the anode current saturates so that the

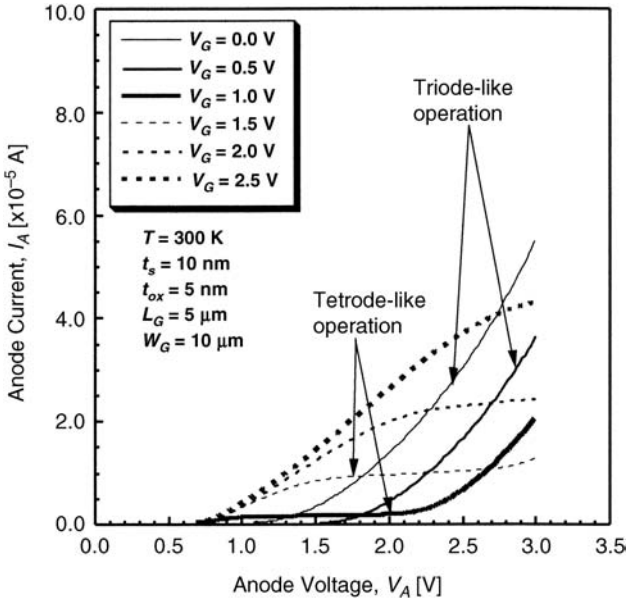

Figure 17.2 Current–voltage characteristics of the Lubistor. Tetrode-like or triode-like characteristics are found in different anode voltage regions. Copyright 2002. The Institute of Electronics Engineers of Korea. [Y. Omura, A new basic element for neural logic functions and capability in circuit applications, *Journal of Semiconductor Technology and Science*, vol. 2, pp. 70–81, 2002.]

device shows a tetrode-like operation. In this V_A range, saturation of the anode current results from the fact that the number of electrons, which contribute to the recombination with injected holes, is controlled by the gate voltage V_G.

It should also be noted that the electron inversion layer reduces the effective hole diffusion length. At fairly high anode voltages, however, the anode current increases again so that the device shows a triode-like operation. In this V_A range, the anode bias diminishes electrons in the body because the body potential increases; the electron inversion layer disappears near the anode. In other words, the hole diffusion length increases with the anode voltage and the anode current increases again. Therefore, the critical voltage for V_A is about $V_G + V_{TH} + 0.7$ (V), as observed in the figure.

17.2.2 Device Model for the Lubistor

Since the Lubistor has two natures, as described in the previous section, we propose a model for DC simulations, which is shown in Figure 17.3(a). The transistor Tr-1 is the parasitic SOI MOSFET at the cathode side, the diode D is the intrinsic pn-junction device at the anode side, and the transistor Tr-2 is the implicit device to raise the cathode voltage of D by the resistor R. Since the supply voltage of the auxiliary terminal is set, usually, as the anode voltage, the gate width of Tr-2 has been set large in order to keep the voltage drop of R large. The device parameters for simulations are tabulated in Table 17.1, where the device parameters are tuned to the usual 0.5-μm-CMOS technology for simplicity.

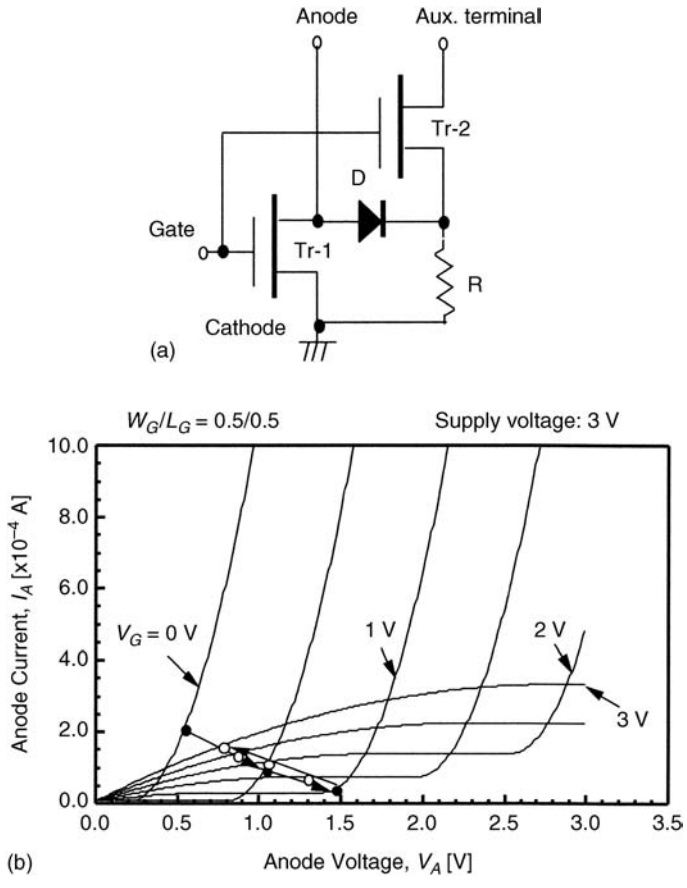

Figure 17.3 An equivalent circuit model for the Lubistor. (a) An equivalent device model for the Lubistor. The auxiliary terminal is only used for adjusting the cathode voltage of the diode and the terminal is set as being equal to the anode voltage of the Lubistor. (b) Simulation results based on the model. Copyright 2002. The Institute of Electronics Engineers of Korea. [Y. Omura, A new basic element for neural logic functions and capability in circuit applications, *Journal of Semiconductor Technology and Science*, vol. 2, pp. 70–81, 2002.]

Simulation results of the Lubistor are shown in Figure 17.3(b). Simulation results show a tetrode-like feature in the range of low anode voltages and a triode-like feature in the range of high anode voltages. The significant feature that the anode current at the high anode voltage is suppressed by the increase in the gate voltage is reproduced by the proposed equivalent circuit model. However, it can be seen that simulated results are slightly different from Figure 17.2. The difference appears in the low anode voltage region. This is due to the deficiency of the circuit model. The model should be improved in future. However, the characteristic difference in the low anode voltage region hardly affects the following simulations because all applications presented here are considered in high anode voltages.

Table 17.1 Device parameters for simulations. Copyright 2002. The Institute of Electronics Engineers of Korea. [Y. Omura, A new basic element for neural logic functions and capability in circuit applications, *Journal of Semiconductor Technology and Science*, vol. 2, pp. 70–81, 2002.]

Parameters*	Values [unit]
Gate oxide layer thickness (t_{ox})	10 [nm]
Gate length (L_G)	0.5 [μm]
Gate width (W_G)	100 [μm] (Tr-2)
	5 [μm] (Tr-1)
Threshold voltage (V_{TH})	0.2 [V]
Electron mobility (μ_0)	500 [cm^2/V s] (Tr-1, Tr-2)
Resistor (R)	10 [Ω]
Ideality factor (n)	1.5 (diode)

*These parameters are only used for the basic logic element.

Basic device parameters are tuned to the usual 0.5-μm-CMOS process technology. Closed circles indicate loci of V_{out} in the logic element shown in Figure 17.4(a). The locus moves as the gate voltage increases along with the arrow.

17.2.3 Proposal of a New Logic Element

Figure 17.4(a) shows, as an example, the simplest logic element, which is composed of an SOI nMOSFET and a p^+–p–n^+ (Type II) Lubistor. The logic element has a control gate terminal (denoted by 'C'), an input signal terminal (denoted by 'I'), and an output signal terminal (denoted by 'O'). Simulated results of input–output characteristics are shown as a parameter of the control gate voltage in Figure 17.4(b). It can be seen that the output voltage (V_{out}) initially increases as the input voltage (V_{in}) increases and reaches a peak at V_{op}. Subsequent increase in V_{in} leads to a steady fall in V_{out}. V_{op} and V_{ic} increase as the control gate voltage (V_{cg}) increases. Locus points of V_{out} are shown in Figure 17.3(b) to explain the operation of this logic element, where it assumed $V_{cg} = 3$ V. The trace of loci is complicated, but interesting. The drain-to-source voltage of the load MOSFET traces along with the loci. When V_{in} is lower than V_{ic} (−1.3 V), the anode current of the Lubistor decreases with an increase in V_{in} because the Lubistor is in the triode-like mode; in operation, the anode voltage of the Lubistor increases as shown in Figure 17.3(b). When V_{in} is higher than V_{ic} (−1.3 V), the anode current of the Lubistor increases with an increase in V_{in} because the Lubistor is in the tetrode-like mode; the anode voltage decreases in this operation. Thus, V_{out} increases with V_{in} when $V_{in} < V_{ic}$ (−1.3 V) and it falls when $V_{in} > V_{ic}$. This characteristic is very interesting and useful because the operation of the logic element works like a synapse, as discussed below.

Here, we simply explain the relationship between the operation of the logic element and the neural operation. A detailed discussion is described in the next section. The simplified model of the neural function is expressed mathematically as [14]

$$V_i(t + \Delta t) = f\left[\sum_{j=1}^{N} J_{ij} V_j(t) - U\right] \quad (i = 1, \ldots, N), \tag{17.1}$$

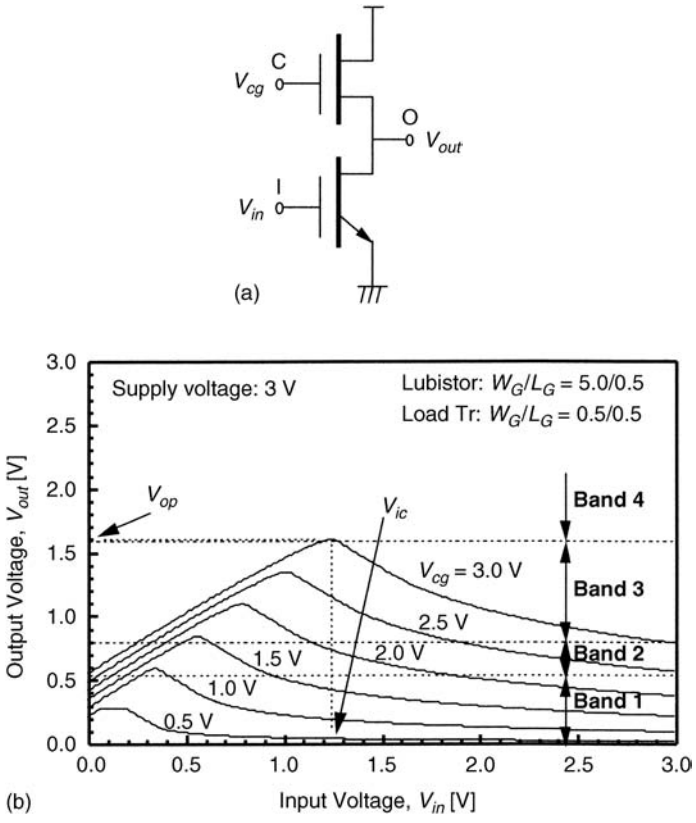

Figure 17.4 A basic element and input–output voltage characteristics. (a) Basic logic element. (b) Input–output characteristics of the basic logic element. Copyright 2002. The Institute of Electronics Engineers of Korea. [Y. Omura, A new basic element for neural logic functions and capability in circuit applications, *Journal of Semiconductor Technology and Science*, vol. 2, pp. 70–81, 2002.] © 1999 IEEE. Reprinted, with permission, from Y. Omura, Neuron firing operations by a new basic logic element, *IEEE Electron Device Letters*, vol. 20, pp. 226–228, 1999.

where $V_j(t)$ is the jth activated neuron potential at the time t, Δt is the delay time for the neuron to fire, U is the threshold potential to fire, J_{ij} is the synaptic strength between the ith neuron and the jth neuron, and $f(x)$ is the sigmoid function [14,15]. The νMOS transistor successfully simulates the sigmoid function in Equation (17.1) with specifically fixed synaptic strengths [3]. However, flexible synaptic strengths are required to design variable functions. In the νMOS transistor, for example, apparent flexibility of synaptic strength can be realized by using digitized input signals.

The basic logic element proposed here can simulate very flexible synaptic strength by using the control gate 'C' in Figure 17.4(a). The combination of one basic logic element and two following CMOS inverters with a certain logic threshold (V_{LT}) is shown in Figure 17.5(a). In the following, we consider the case of $V_{cg} = 3$ V (supply voltage) for simplicity. We assume that the pulse frequency modulation signal is used here as an input signal. When V_{LT} is smaller

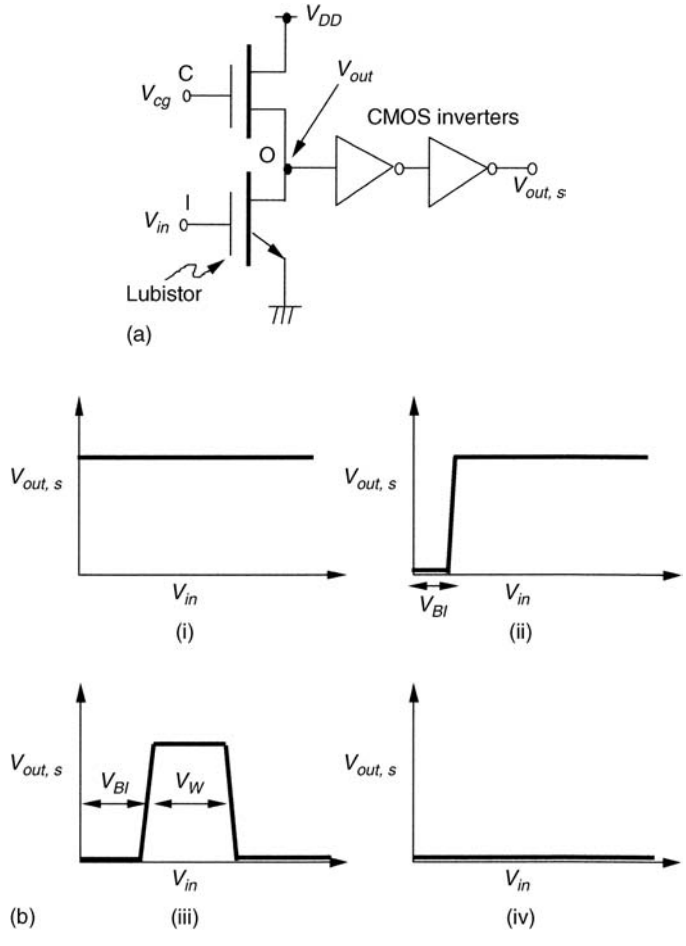

Figure 17.5 Simplified logic unit simulating a synaptic operation. (a) The simplest circuit for synaptic operation. (b) Schematics diagrams of synaptic operations. (i) $V_{out,s}$ for $V_{LT} < V_{out}$ at $V_{in} = 0$ V, (ii) '*excitatory pattern*' of $V_{out,s}$, (iii) '*semi-exitatory pattern*' of $V_{out,s}$, (iv) '*inhibitory pattern*' of $V_{out,s}$ for $V_{LT} > V_{op}$. Copyright 2002. The Institute of Electronics Engineers of Korea. [Y. Omura, A new basic element for neural logic functions and capability in circuit applications, *Journal of Semiconductor Technology and Science*, vol. 2, pp. 70–81, 2002.] © 1999 IEEE. Reprinted, with permission, from Y. Omura, Neuron firing operations by a new basic logic element, *IEEE Electron Device Letters*, vol. 20, pp. 226–228, 1999.

than V_{out} at $V_{in} = 0$ V (band 1 in Figure 17.4(b)), the output voltage ($V_{out,s}$) of the last CMOS inverter is always equal to 3 V without regard for the input voltage (V_{in}); the logic element operates like an *axon* (pattern (i) in Figure 17.5(b)).

When V_{LT} is between V_{out} at $V_{in} = 0$ V and V_{out} at $V_{in} = 3$ V (band 2 in Figure 17.4(b)), the output voltage ($V_{out,s}$) of the last CMOS inverter changes abruptly from 0 V to 3 V as the input signal voltage (V_{in}) increases; the synapse characteristic is *excitatory* (pattern (ii) in Figure 17.5(b)). The input voltage (V_{B1} in Figure 17.5(b), pattern (ii)) at which the synapse

goes excitatory depends on both V_{LT} and the control gate voltage (V_{cg}), which means that the sensitivity of the synapse can be controlled by either V_{LT} or V_{cg} or both. As an example, consider the case where a capacitor is connected to the control gate terminal 'C' of the proposed logic element in Figure 17.5(a). When charges are transferred to the capacitor from the other terminal, such as memory circuits, the amount of charge determines the control gate voltage V_{cg} (equivalently the weight to input signal for neural devices). Since the given weight modulates V_{B1} of the logic element, the logic element works as a weighted logic gate.

When V_{LT} is between V_{out} at $V_{in} = 3$ V and V_{op} (band 3 in Figure 17.4(b)), the last CMOS inverter gives a single pulse-like signal, which can be used as a window function (or literal function) [15]; the synapse characteristic is *semi-excitatory* (pattern (iii) in Figure 17.5(b)). This pattern shape is controllable by V_{cg}. The input voltage (V_{B1} in Figure 17.5(b), pattern (iii)) at which the synapse goes excitatory also depends on either V_{LT} or the control gate voltage (V_{cg}) or both; this is also true for the bias window (V_W in Figure 17.5(b), pattern (iii)). This means that the sensitivity of the synapse can also be controlled by both V_{LT} and V_{cg}.

When V_{LT} is larger than V_{op} (band 4 in Figure 17.4(b)), CMOS inverters are not activated and the output voltage ($V_{out,s}$) of the last CMOS inverter holds at 0 V without regard for the input signal voltage (V_{in}); the synapse characteristic is *inhibitory* (pattern (iv) in Figure 17.5(b)).

By designing the logic threshold of the CMOS inverters appropriately, one of the above four functions can be chosen for a certain fixed V_{cg} value. Of particular interest, operations (i), (ii), and (iv) are applicable to setting the weight factor (α_w) in neural applications: (i) for $\alpha_w = 0$, (ii) for $0 < \alpha_w < 1$, and (iv) for $\alpha_w = 1$. Since a pair of CMOS inverters gives a binary logic output signal, the logic element shown in Figure 17.5(a) is compatible with conventional LSIs.

The important point is that the above four operations are flexibly changed by the control gate ('C') voltage. In other words, the control gate voltage (V_{cg}) directly determines the synaptic strength. It is easily noticed that the output signal patterns shown in Figure 17.5(b) can be used as an input signal to a νMOS transistor. The combination of the basic logic element and an SOI νMOS transistor should yield new functional applications. Examples of important applications and functions of the proposed basic element are discussed later.

Circuit operations similar to Figure 17.4(b) have already been examined by Y. Sekine *et al*. [16]. However, the aim of their work was to produce pulse series to simulate output signals of neurons by use of the negative conductance characteristics. The circuit needs several passive elements such as quite a large capacitor, which means that monolithic LSIs would be difficult to realize. As discussed later, a similar operation is easily demonstrated in a very simple circuit without any additional passive elements by using the basic logic element proposed here.

17.3 Circuit Applications and Discussion

17.3.1 Examples of Fundamental Elements for Circuit Applications

The important characteristic of the logic element shown in Figure 17.4 was discussed simply in the previous section. This section discusses more practical circuit operations including a couple of important applications. Examples are shown in Figures 17.6 to 17.8.

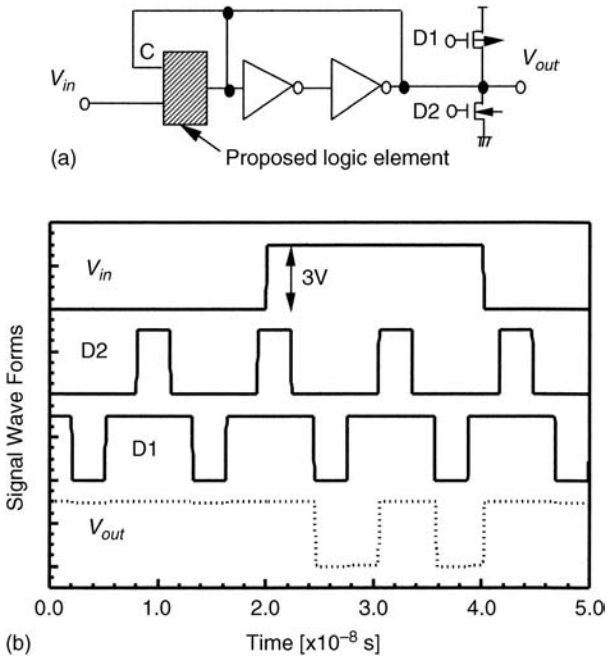

Figure 17.6 An example of a circuit application and input–output characteristics. (a) A *data holding function*. (b) Simulation results of the *data holding function*. Copyright 2002. The Institute of Electronics Engineers of Korea. [Y. Omura, A new basic element for neural logic functions and capability in circuit applications, *Journal of Semiconductor Technology and Science*, vol. 2, pp. 70–81, 2002.]

Figure 17.6(a) shows a small circuit element that has the function of data holding. In this circuit, just the output signals of the proposed basic logic element and the last CMOS inverter are fed back to the control gate terminal in the element shown in Figure 17.5(a). The two CMOS inverters also work as a positive-feedback amplifier.

The MOSFET for 'D1' is of a p-channel type and that for 'D2' is of an n-channel type. Simulation results are shown in Figure 17.6(b). It is assumed that the V_{LT} of the first CMOS inverter lies inside band 3 at low control gate voltages and low V_{in} (see Figure 17.4(b)). When the input signal (V_{in}) is at level '0' and the output signal of the last CMOS inverter, which is equivalent to that of the control gate terminal ('C'), is at level '1', any input signal from 'D1' or 'D2' to replace the data with new data is rejected and V_{out} holds the '1' level. This is because the output level of the proposed logic element is beyond V_{LT} of the first CMOS inverter and the output level of the first CMOS inverter goes down to the '0' level. This state is fixed by the positive-feedback effect of the two CMOS inverters. In this case, naturally V_{out} is insensitive to any disturbance from the 'D1' or 'D2' terminal. On the other hand, when the input signal (V_{in}) is at the '1' level, the data at the V_{out} terminal are replaced with new data by a signal from 'D1' or 'D2', as shown in Figure 17.6(b). As shown in Figure 17.4(b), this is because, at high V_{in}, the V_{LT} of the first CMOS inverter lies inside band 3 at low control gate voltages and it lies inside band 1 at high control gate voltages. When V_{out} is changed from level '1' to level '0' by the signal from 'D2', V_{out} becomes lower than V_{LT} of the

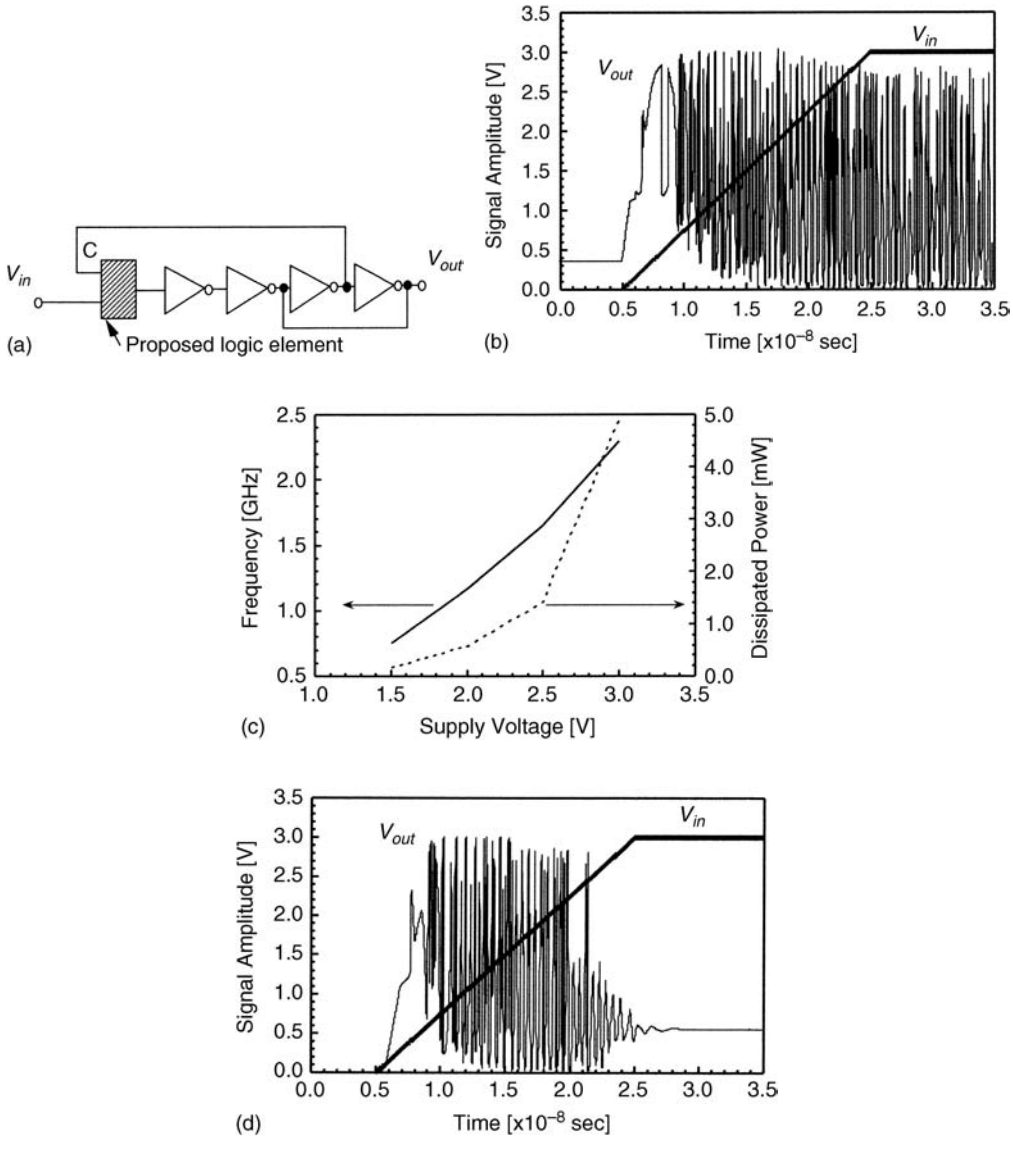

Figure 17.7 An example of a circuit application and input–output characteristics. (a) A selective *oscillation function*. (b) Simulation results of the selective *oscillation function*. (c) Dependence of oscillation characteristics on the supply voltage. (d) Simulation results of the *geyser function*. Copyright 2002. The Institute of Electronics Engineers of Korea. [Y. Omura, A new basic element for neural logic functions and capability in circuit applications, *Journal of Semiconductor Technology and Science*, vol. 2, pp. 70–81, 2002.] © 1999 IEEE. Reprinted, with permission, from Y. Omura, Neuron firing operations by a new basic logic element, *IEEE Electron Device Letters*, vol. 20, pp. 226–228, 1999.

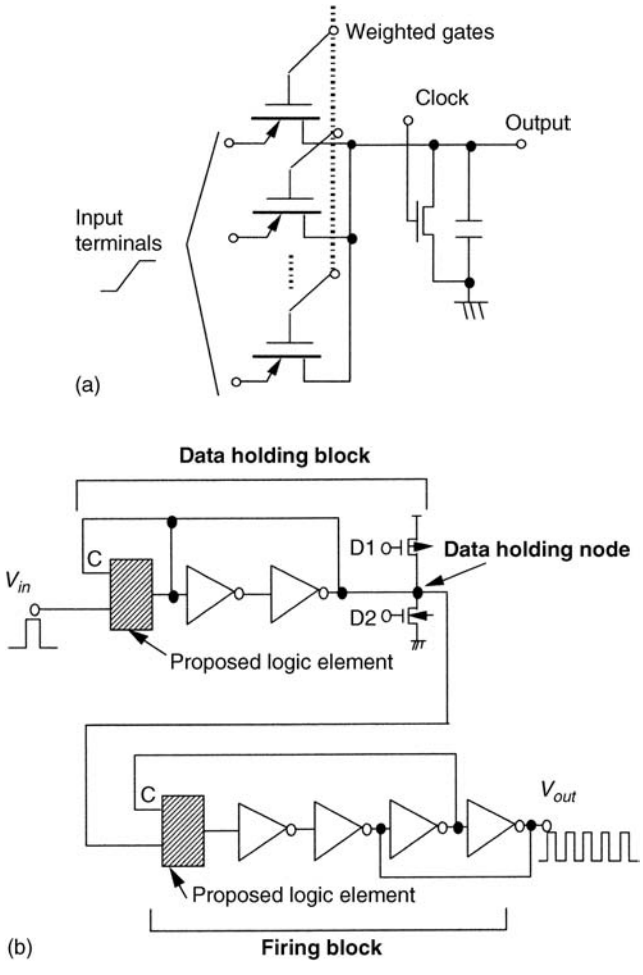

Figure 17.8 An example of a Boltzmann machine neuron block. (a) A sum-of-product unit using Lubistors. (b) A stochastic-response unit. Copyright 2002. The Institute of Electronics Engineers of Korea. [Y. Omura, A new basic element for neural logic functions and capability in circuit applications, *Journal of Semiconductor Technology and Science*, vol. 2, pp. 70–81, 2002.]

first CMOS inverter. This state is stable due to the positive-feedback effect of the two CMOS inverters. When V_{out} is changed from level '0' to level '1' by the signal from 'D1', V_{out} becomes higher than V_{LT} of the first CMOS inverter. This state is also stable due to the positive-feedback effect. Thus, the circuit shows a *data holding function* when V_{in} is at the '1' level.

Figure 17.7(a) shows a circuit that has the function of selective oscillation. In this circuit, the output signal of the third CMOS inverter is fed back to the control gate terminal ('C') in the element shown in Figure 17.5(a), and the output signal of the last CMOS inverter is fed back to the third CMOS inverter. First, we consider the case where the V_{LT} of the first CMOS inverter lies inside band 2 (see Figure 17.4(b)).

Simulation results are shown in Figure 17.7(b). It should be noted that the output signal level (V_{out}) oscillates during the transition and the level '1' of V_{in}. When the input signal (V_{in}) is at level '0' and the control gate terminal ('C') is also at level '0', the output signal of the first CMOS inverter is automatically at level '1' because the output signal level of the proposed basic element does not reach the V_{LT} of the first CMOS inverter, which is obvious in Figure 17.4(b). This means that the output level of the third CMOS inverter, which is equivalent to the level of 'C', should change to level '1'. Consequently, the output signal level (V_{out}) oscillates. Figure 17.7(c) shows the dependence of the oscillation characteristic on the supply voltage. The circuit oscillates at the GHz rate with low-power dissipation.

Second, we consider the case where the V_{LT} of the first CMOS inverter is inside band 3 (see Figure 17.4(b)). Simulation results are shown in Figure 17.7(d). It should be noted that the output signal level (V_{out}) oscillates only during the transition of V_{in}, unlike the former case, although the fundamental oscillation mechanism is identical. Since the V_{LT} of the first CMOS inverter lies inside band 3, the first CMOS inverter shows the operation of function (iii) in Figure 17.5(b) during the transition of V_{in}. An intermittent pulse is obtained at the output terminal of the proposed logic element. Therefore, the oscillation mode can be modulated by the intermittent pulse to produce a *geyser*. The width of the *geyser* is determined by the logic threshold of the CMOS inverter; namely, the width is defined by V_W, as shown in function (iii) of Figure 17.5(b). When the CMOS inverter following the proposed logic element is replaced with a NOR block or a NAND block, this function is extended to a multi-input circuit. The number of input terminals is not limited.

The above consideration suggests that the proposed basic element is applicable to a Boltzmann machine neuron circuit. The Boltzmann machine is a kind of feedback neural network that can solve various complicated problems [14,15] and consists of a large network of neurons interconnected bidirectionally with various connection strengths. In its basic form, the Boltzmann machine neuron consists of a sum-of-product unit and a stochastic-response unit. An example of a sum-of-product unit is shown in Figure 17.8(a). In Figure 17.8(a), the Lubistor plays an important role because it has the nature of a *unilateral* current path. The sum-of-product result is automatically obtained in the capacitor. It can be reset by the MOSFET to yield a *clock* terminal. The weight at each input terminal can be defined by weighted gate pulses that have different heights or widths. Data from input terminals are gathered into the capacitor.

A practical example of a neuron block as a stochastic-response unit composed of nine equivalent CMOS inverters is shown in Figure 17.8(b). Since this block includes a memory unit using the data holding function proposed in Figure 17.7(a), it is superior to conventional neuron circuits. The stochastic operation to determine whether a neuron fires or not is controlled by a digital pulse from V_{in} in Figure 17.8(b). For example, level '0' of V_{in} results in the continuous oscillation signal (*firing* of neuron) at the V_{out} terminal. On the other hand, level '1' of V_{in} results in the selective oscillation signal depending on the data at the data holding node. The oscillation mode is selected by signals from 'D1' and 'D2' terminals. In this case, it is preferable to use the output voltage of the circuit in Figure 17.8(a) as input to 'D1' and 'D2' terminals. In other words, the sum-of-product is reflected by the state of the neuron; the level '0' signal for the 'D1' terminal changes the neuron state to an *excitatory* state and the level '1' signal for the 'D2' terminal changes the neuron state to an *inhibitory* state. In this operation, functions (i), (ii), and (iii) in Figure 17.5(b) are all used automatically. Consequently, these blocks work as a unit in the Boltzmann machine neuron circuit.

17.3.2 On the Further Improvement of Functions of the Basic Logic Element

In this section, we described the basic logic element to simulate a synapse. In this *synapse*, the synaptic strength has to be controlled by the voltage of the control gate ('C'). In practical applications, this must be overcome to improve the flexibility of synapse strengths. In other words, the flexibility of the synapse means a memory effect in synapses. To realize a synapse with some memory effect, we must use some ferroelectric material as a gate insulator to simplify the complicated circuit.

On the other hand, the design issue of Lubistors is one of the remaining problems. However, since the device operation is not very complicated and the device model can be simplified, the design technique will be readily developed. Then, at least, we think that the combination of an advanced logic element with the memory effect and the νMOS transistor will result in greatly improved circuit performance in the future.

17.4 Summary

A basic element for new neural logic operation devices has been proposed and some functions such as a synaptic function have been demonstrated. It has been shown that a key device for the logic operation is the insulated-gate pn-junction device on SOI substrates. The device model for simulations was proposed. Using the model, features of practical circuits were examined. The basic element shows various characteristics depending on the device dimension and the control gate voltage. It has been shown that operation of the basic element is applicable to neural circuits. One important aspect is that the basic element offers an interface quite compatible to that of conventional CMOS circuits. Therefore, many kinds of circuit applications seem possible.

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Sub-1-V Voltage Reference Circuit Technology as an Analog Circuit Application

18.1 Review of Bandgap Reference

The bandgap reference can produce references having TC_F values of the order of 10 ppm/ °C over the temperature range of 0 to 70 °C [1–3]. The fundamental principle behind the bandgap reference circuit can be explained using the illustration shown in Figure 18.1 [1].

Voltage V_{BE} is generated from the pn-junction component of bipolar junction transistor (BJT); its temperature coefficient is about −2 mV/ °C around room temperature. The thermal voltage (k_BT/q) is also generated; its temperature coefficient is 0.085 mV/ °C around room temperature [1]. The circuit shown in Figure 18.1 produces the output voltage given as

$$V_{REF} = V_{BE} + Gk_BT/q. \tag{18.1}$$

Differentiating Equation (18.1) with respect to temperature leads to a value of G that gives zero temperature dependence. A theoretical expression of the temperature dependence of V_{BE} is necessary to achieve the desired performance. Since V_{BE} should have little dependence on the supply voltage, it is anticipated that the supply-voltage dependence of the bandgap reference is very small.

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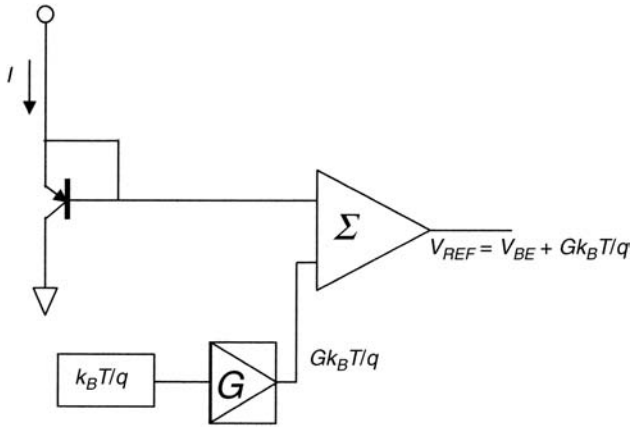

Figure 18.1 Principle of the bandgap reference [1]. By permission of Oxford University Press, Inc. *CMOS Analog Circuit Design*, 2E by Philip E. Douglas R. Holberg (2002).

18.2 Challenging Study of Sub-1-V Voltage Reference

A conventional CMOS bandgap reference circuit that works as a sub-1-V source is shown in Figure 18.2. The reference voltage of the circuit is written as

$$V_{REF} = V_{BE2} + \frac{R_2}{R_1} V_{R1}, \tag{18.2}$$

where V_{BE2} is the base-to-emitter voltage of transistor Q_2.

As shown in Equation (18.1), the reference voltage of conventional circuits is expressed by the sum of the proportional-to-absolute-temperature (*PTAT*) voltage and the complementary-to-absolute-temperature (*CTAT*) voltage; this is approximately equal to the material's

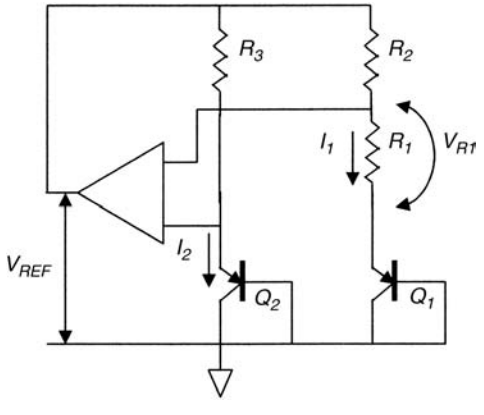

Figure 18.2 A conventional bandgap reference circuit [1]. By permission of Oxford University Press, Inc. *CMOS Analog Circuit Design*, 2E by Philip E. Douglas R. Holberg (2002).

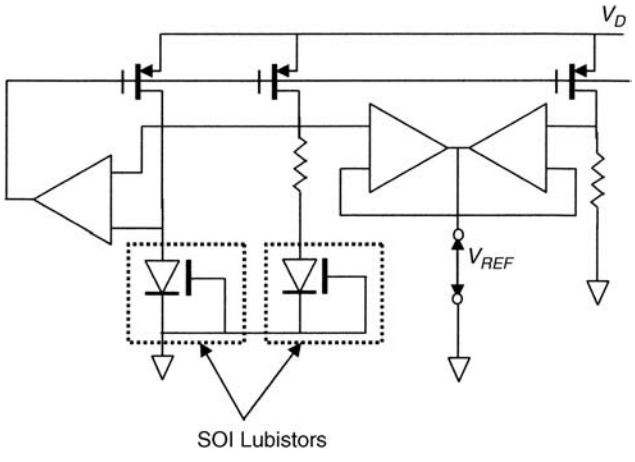

Figure 18.3 Sub-1-V voltage reference circuit proposed in Reference [5]. © 2009 IEEE. Reprinted, with permission, from A.J. Annema, P. Veldhorst, G. Doornbos, and B. Nauta, A Sub-1V Bandgap Voltage Reference in 32 nm FinFET, *Proceedings of the 2009 IEEE International Solid-State Circuit Conference,* February 2009.

bandgap. The *CTAT* voltage is typically achieved by a forward-biased pn-junction diode. As a result, the reference voltage is about 1.2 V, which does not suit the supply voltages of recent advanced CMOS technologies. In addition, a recent proposal still has a large area penalty [4] because the circuit uses many high-ohmic resistors to suppress the power consumption.

Annema *et al*. proposed a sub-1-V bandgap voltage reference circuit in which two SOI Lubistors are implemented [5]; two BJTs that work as pn-junction diodes are replaced with SOI Lubistors. The schematic circuit block proposed in Reference [5] is shown in Figure 18.3. The circuit uses two relatively small resistors and resistorless weighted-averaging to realize area-efficient sub-1-V bandgap voltage references. The reference voltage served by the circuit is expressed as

$$V_{REF} = \frac{PTAT + CTAT}{m} \approx \frac{1.2V}{m}. \tag{18.3}$$

The circuit yields $m = 2$ and hence an output voltage of about 0.6 V.

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19

Possible Implementation of SOI Lubistors into Conventional Logic Circuits

The initial research motivation behind the silicon surface tunnel transistor (Si STT) in the twentieth century was the scientific interest in the potential of the semiconductor Si [1–6]. In the twenty-first century, the primary interest of many scientists and engineers is now focused on how the tunnel phenomenon can contribute to innovations in device performance.

When the bulk-type tunnel FET (TFET) was proposed in 2004 [7,8], the major purpose of the proposal was to achieve MOSFETs with a sub-60-mV/decade subthreshold swing, because such a steep swing promised ultra-low-voltage analog and digital processes. Nirschl *et al*. examined the performances of bulk-type TFETs fabricated with 130 nm and 90 nm process flows [9]. TFETs with good performance were demonstrated. They also investigated a mixed TFET/CMOS (TCMOS) logic family, where TCMOS is composed of a p-channel MOSFET and an n-channel TFET. A schematic of the TCMOS inverter is shown in Figure 19.1 [9]. Although the switching delay of the TCMOS inverter is not superior to that of the conventional CMOS with identical dimensions, simulation results suggest that the TCMOS latch has a better static noise margin than the conventional CMOS latch. The most impressive attribute of the TCMOS inverter is its definite reduction in power dissipation [10].

Recently, a new type of SOI-based CMOS inverter (CLTFET) with a Lubistor load and a TFET driver was proposed [11]. The schematic CLTFET layout is shown in Figure 19.2(a). It has been demonstrated that a CLTFET-based logic circuit is faster than a CTFET logic circuit (see Figure 19.2(b)) designed on the same fabrication technology [11]. The CLTFET inverter revealed the best results in terms of noise margin and low crowbar current, which should contribute to a reduction in supply voltage and short-circuit power dissipation, respectively. It has been demonstrated that the switching delay time of the CLTFET inverter was smaller by about 30% than that of the CTFET inverter [11].

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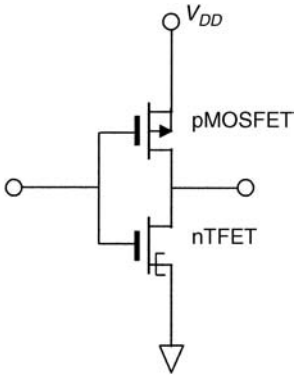

Figure 19.1 Schematic of the TCMOS inverter. The driver device is the n-channel TFET.

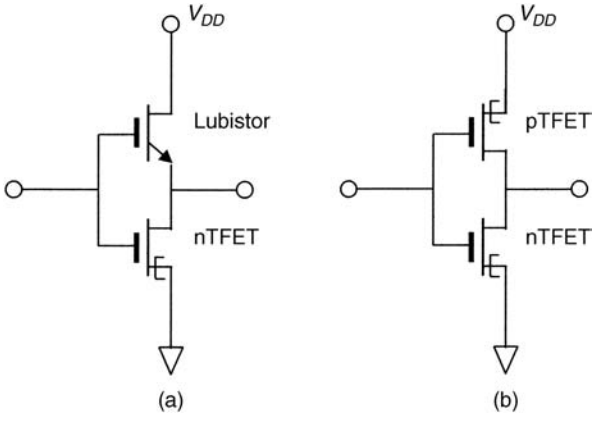

Figure 19.2 Schematic of the TFET-based inverter. (a) CLTFET inverter, (b) CTFET inverter.

This kind of logic element will be applied to future low-energy circuit applications, for example, medical implant applications [12–14], because these devices are very easily scaled and compatible with the conventional SOI LSIs that have already been commercialized.

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Part Five

Optical Device Applications of SOI Lubistors

20

Potentiality of Electro-Optic Modulator Based on the SOI Waveguide

20.1 Introduction

The rapid adoption of international telecommunication services has already exceeded our expectations. Traditional TDM (time division multiplex) and FDM (frequency division multiplex) systems will soon reach their limits in terms of communication capability and efficiency. One key solution is WDM (wavelength division multiplexing). However, the low precision with which frequency can be currently controlled limits the multiplexing level to 16, which blocks future growth in telecommunication services [1].

The realization of high-performance WDM systems appears to depend on the photonic crystal [2–15] waveguide. We can manipulate the optical characteristics of the photonic crystal waveguide such as the transmission frequency band and the forbidden frequency band (i.e., photonic bandgap, PBG) by varying its periodic geometry. In addition, when we introduce a *defect* that destroys (locally) the periodicity of the photonic crystal waveguide, it is known that an optical wave with a specific transmitting mode, generated within the photonic bandgap due to the defect, can propagate through the waveguide [2–5]. Thus, photonic crystal waveguides should have wide application due to the apparent simplicity with which their characteristics can be set. We note that two-dimensional (2-D) photonic crystal structures are also being studied to realize various optical circuits [6]. However, the one-dimensional (1-D) photonic crystal structure has sufficient potential for applications such as non-linear optical devices and wavelength filters.

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20.2 Characterization of the Quasi-One-Dimensional Photonic Crystal Waveguide

Three-dimensional (3-D) electromagnetic simulations based on the finite difference time domain (FDTD) method were performed to investigate the feasibility of the quasi-one-dimensional photonic crystal (Q1DPC) waveguide [16] shown in Figure 20.1; the study started with the analogy of super-lattices in semiconductor devices. Calculated transmission spectra for the Q1DPC Si waveguide with a height of 200 nm are shown in Figure 20.2; the frequency range plotted is 100 THz to 400 THz because we focus on infrared optical communication systems. A clear and wide PBG exists from 159 THz to 219 THz; light waves beyond 219 THz are attenuated by 10 dB.

We focus on how modulation of the unit cell structure impacts the optical properties of the Q1DPC waveguide. We also address the physics and applications of the modulated unit cell structure in the Q1DPC waveguide theoretically. This study is very important from the technological point of view because such a waveguide is frequently applied to various optical communication systems as an optical modulator.

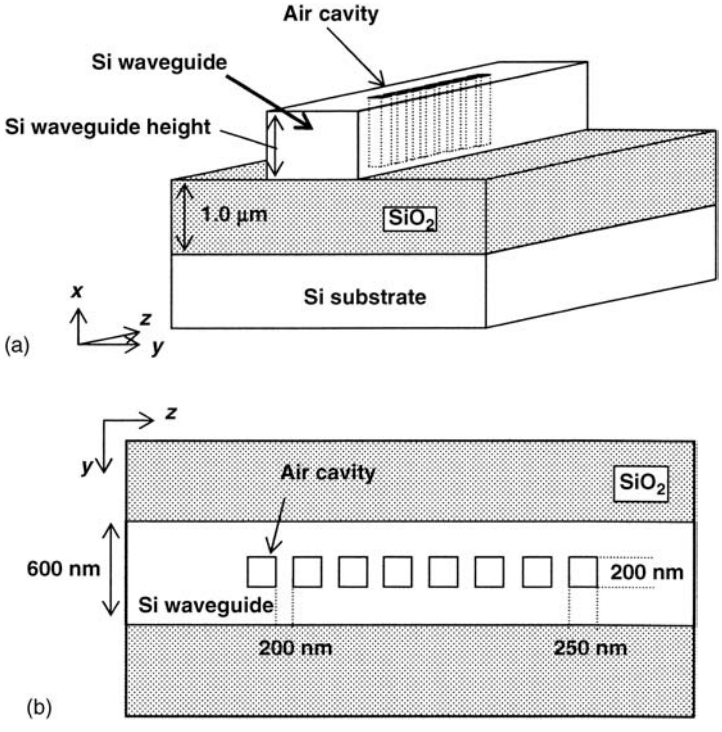

Figure 20.1 Quasi-one-dimensional photonic-crystal waveguide [16]. (a) Bird's eye view of the Q1DPC waveguide. (b) Top view of the Q1DPC waveguide. Cavity period (p) is 450 nm. Reproduced by permission of The Pleiades Publishing, Ltd and Springer. [Y. Ogawa, T Kinoshita, Y. Omura, and Y. Iida, "Photonic band structure and transmission control in quasi-one-dimensional photonic-crystal waveguide with a modulated unit cell structure", *Laser Physics*, vol. 14, pp. 712–719, 2004.]

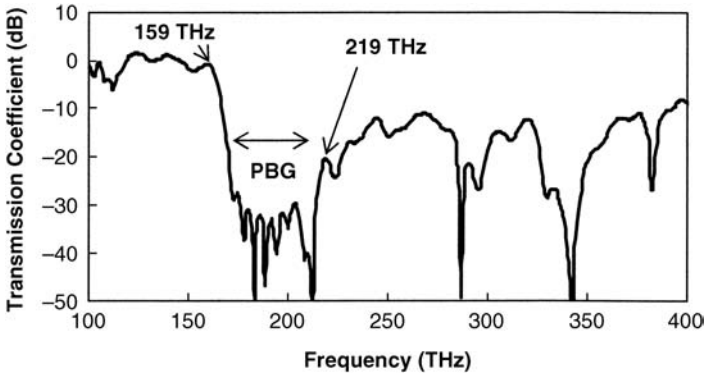

Figure 20.2 Transmission coefficient dependence on frequency: Si waveguide height is 200 nm. Reproduced by permission of The Pleiades Publishing, Ltd and Springer. [Y. Ogawa, T Kinoshita, Y. Omura, and Y. Iida, "Photonic band structure and transmission control in quasi-one-dimensional photonic-crystal waveguide with a modulated unit cell structure", *Laser Physics*, vol. 14, pp. 712–719, 2004.]

Here we simulate the optical characteristics of a Q1DPC waveguide with different modulated unit-cell structures. Figure 20.3 shows four modulated air cavity alignment patterns; the unit cell has two air cavities in Figure 20.3(a), three cavities in Figure 20.3(c), four cavities in Figure 20.3(e) and five cavities in Figure 20.3(g). The other physical parameters of the waveguide are the same as those shown in Figure 20.1; the waveguide height is constant at 200 nm. The total air cavity number (N_{AC}) is 16 for the two-air-cavity unit cell and the four-air-cavity unit cell, and 15 for the three-air-cavity unit cell and the five-air-cavity unit cell.

We introduce air-cavity interval parameters α and β as shown in Figure 20.3; α is the interval length between air cavities inside the unit cell and β is the interval length between unit cells. Here we hold $\alpha + \beta = 400$ nm for the two-air-cavity unit cell, $2\alpha + \beta = 600$ nm for the three-air-cavity unit cell, $3\alpha + \beta = 800$ nm for the four-air-cavity unit cell, and $4\alpha + \beta = 1000$ nm for the five-air-cavity unit cell. To investigate the influence of air-cavity alignment on optical transmission characteristics, we changed the value of α from 200 nm to 0 nm. In this case, since the air cavity is 250 nm long, the revised periodic length (p_r) is 900 nm for the two-air-cavity unit cell, 1350 nm ($2\alpha + \beta$) for the three-air-cavity unit cell, 1800 nm ($3\alpha + \beta$) for the four-air-cavity unit cell, or 2250 nm ($4\alpha + \beta$) for the five-air-cavity unit sell; each periodic length is constant regardless of α or β. Due to space concerns, the following provides only part of the simulation results.

We illustrate photonic bandgap maps obtained by the three-dimensional simulations as a function of α in Figure 20.4(a) for the two-air-cavity unit cell and Figure 20.5(a) for the four-air-cavity unit cell. Gray zones indicate frequency ranges within which the transmission coefficient is less than –20 dB. Though these maps are not very exact in terms of defining the photonic bandgap edge, they are sufficiently meaningful to allow discussion of the general aspects of the PBGs of various modulated unit-cell structures.

To understand the properties of the calculated PBGs comprehensively, we also calculated the band structures of a one-dimensional multi-layer film system that had the same periodic structure as the Si waveguide discussed above; all air films are 250 nm thick and the Si film thickness is α or β. Figures 20.3(b), (d), (f), and (h) show the one-dimensional multi-layer

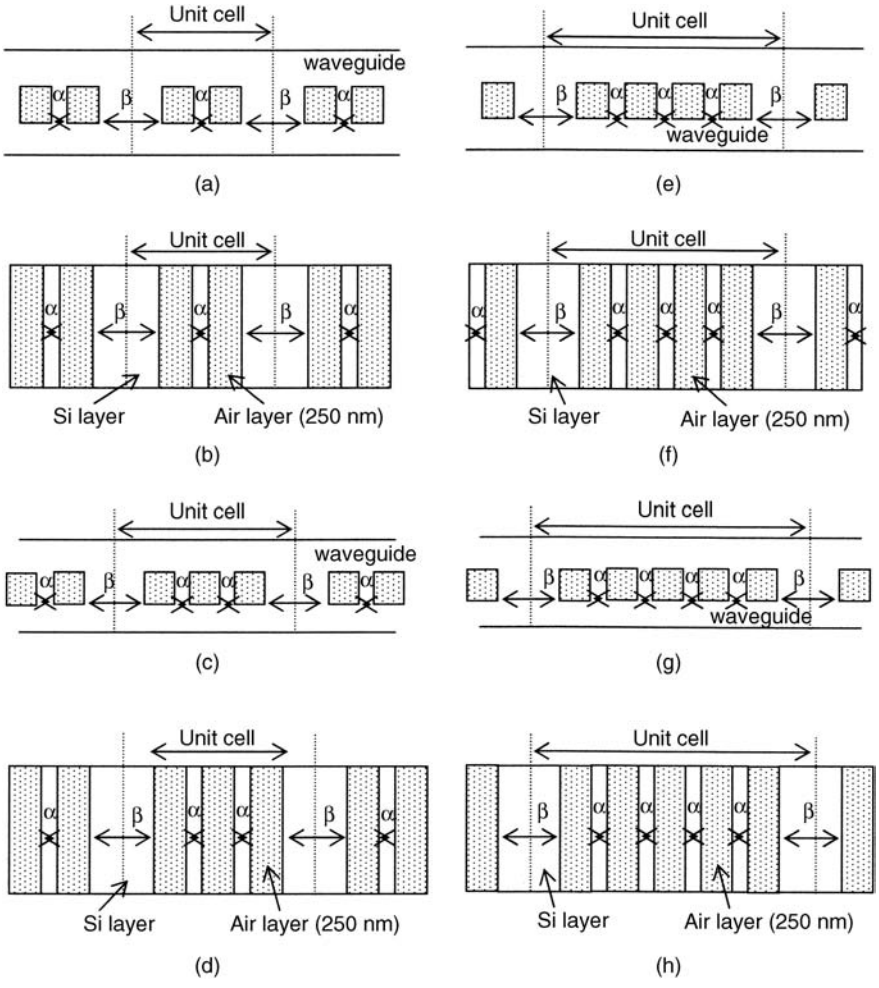

Figure 20.3 Modulated unit-cell structures. (a) Q1DPC waveguide with a two-air-cavity unit cell and periodic length of 900 nm. (b) Multi-layer system with a two-air-film unit cell and periodic length of 900 nm. (c) Q1DPC waveguide with a three-air-cavity unit cell and periodic length of 1350 nm. (d) Multi-layer system with a three-air-film unit cell and periodic length of 1350 nm. (e) Q1DPC waveguide with a four-air-cavity unit cell and periodic length of 1800 nm. (f) Multi-layer system with a four-air-film unit cell and periodic length of 1800 nm. (g) Q1DPC waveguide with a five-air-cavity unit cell and periodic length of 2250 nm. (h) Multi-layer system with a five-air-film unit cell and periodic length of 2250 nm. Reproduced by permission of The Pleiades Publishing, Ltd and Springer. [Y. Ogawa, T Kinoshita, Y. Omura, and Y. Iida, "Photonic band structure and transmission control in quasi-one-dimensional photonic-crystal waveguide with a modulated unit cell structure", *Laser Physics*, vol. 14, pp. 712–719, 2004.]

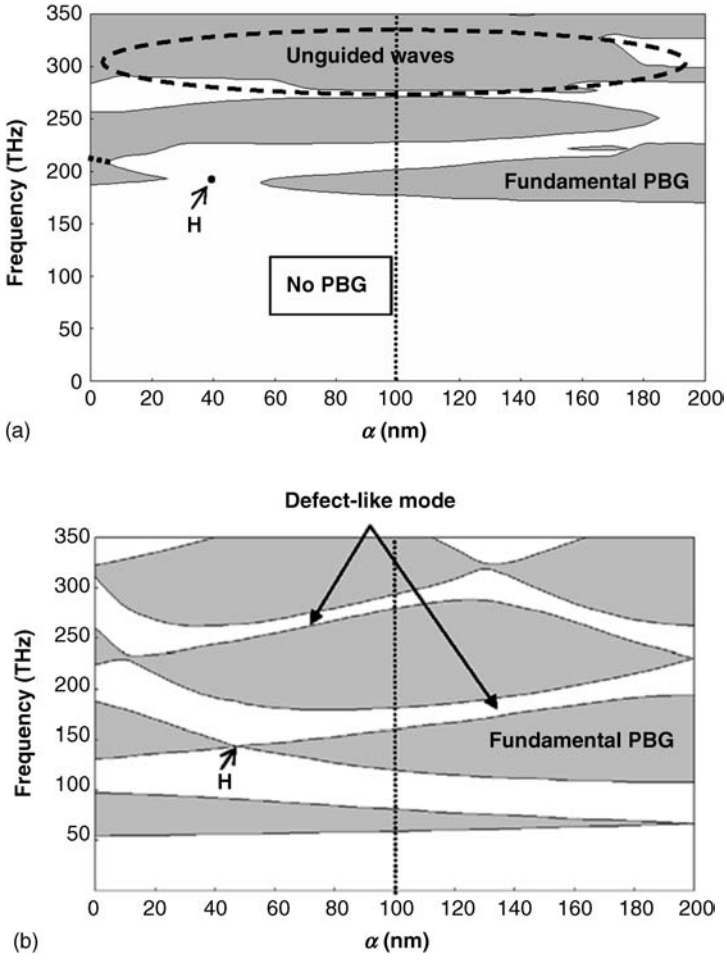

Figure 20.4 The photonic bandgap map of modulated unit-cell structures as a function of α. (a) Q1DPC waveguide with a two-air-cavity unit cell. Gray zones indicate regions in which the transmission coefficient is less than −20 dB. (b) Multi-layer system with a two-air-film unit cell. Gray zones indicate the photonic bandgap. Reproduced by permission of The Pleiades Publishing, Ltd and Springer. [Y. Ogawa, T Kinoshita, Y. Omura, and Y. Iida, "Photonic band structure and transmission control in quasi-one-dimensional photonic-crystal waveguide with a modulated unit cell structure", *Laser Physics*, vol. 14, pp. 712–719, 2004.]

film system with the modulated unit-cell structure. Here we assume that the one-dimensional multi-layer system has an infinite periodic structure. Modulation rules of unit-cell structures are the same as those of the waveguide structures shown in Figures 20.3(a), (c), (e), and (g). We extracted from calculations the dispersion relation of a light wave propagating in the direction normal to the multi-layer film system. We illustrate a map of the photonic bandgap in the one-dimensional multi-layer film system in Figure 20.4(b) for the two-air-film unit cell and Figure 20.5(b) for the four-air-film unit cell. The figures

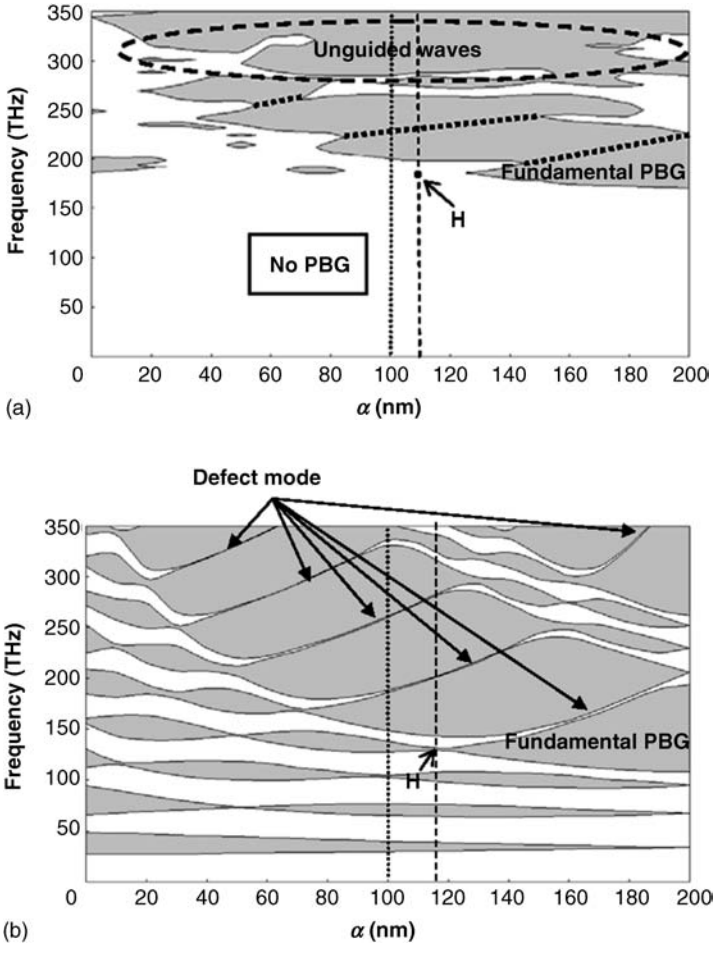

Figure 20.5 The photonic bandgap map of modulated unit-cell structures as a function of α. (a) Q1DPC waveguide with a four-air-cavity unit cell. Gray zones indicate regions in which the transmission coefficient is less than −20 dB. (b) Multi-layer system with a four-air-film unit cell. Gray zones indicate the photonic bandgap. Reproduced by permission of The Pleiades Publishing, Ltd and Springer. [Y. Ogawa, T Kinoshita, Y. Omura, and Y. Iida, "Photonic band structure and transmission control in quasi-one-dimensional photonic-crystal waveguide with a modulated unit cell structure", *Laser Physics*, vol. 14, pp. 712–719, 2004.]

show how the photonic bandgap varies with parameter α. Gray zones represent the photonic bandgap frequency range.

Upon comparing the photonic bandgap behavior of waveguides with that of multi-layer systems, we find large differences at frequencies below 150 THz and over 280 THz. Below 150 THz, the waveguide has no photonic bandgap because this wavelength is too long, compared to waveguide height, to establish strong Bragg reflection. Above 280 THz, on the other hand, the light wave is not guided along the Si core (not shown here in detail) because the wavelength is too short, compared to the waveguide width, to maintain single-mode

propagation. Since the waveguide height is lower than 1000 nm, the frequency range of the photonic bandgap shifts to a higher frequency range than that of the multi-layer system [16].

Since all zones where the transmission coefficient is less than –20 dB are shown in the same way, full details of the photonic bandgap are missing from the photonic bandgap map. Since the quality factor of the photonic crystal is very high for $N_{AC} = 15$ or 16, the so-called defect mode is not easily identified in the simulation results owing to its very sharp spectrum. On the other hand, when the cavity number (N_{AC}) is eight, the defect mode is very clearly observed owing to the photonic crystal's lower quality. In Figure 20.4(b) and Figure 20.5(b), the defect modes seen in the one-dimensional multi-layer system are indicated by arrows. Corresponding defect modes in Figure 20.4(a) and Figure 20.5(a) are not clearly identified for the Q1DPC waveguide. However, attenuated defect modes are indicated by the bold dotted lines in Figure 20.4(a) and Figure 20.5(a); in other words, the remaining one-dimensionality of the Q1DPC waveguide is quite limited.

Over certain frequencies, some aspects of the waveguide's photonic bandgap are very similar to those of the multi-layer system. We show transmission spectra of the waveguide with a four-air-cavity unit cell in Figure 20.6(a). The corresponding dispersion curves for the multi-layer system with α of 100 nm are shown in Figure 20.6(b). In Figure 20.6(a), distinct PBGs for the waveguide are the gaps labeled *X* and *Y* at low frequencies. These gaps correspond to those labeled *X* and *Y* in Figure 20.6(b). The defect mode (denoted by 'A) seen in Figure 20.6(b) is attenuated in Figure 20.6(a).

These results indicate that, within a certain frequency range, the major optical transmission characteristics of the Q1DPC waveguide follow those of a one-dimensional multi-layer system. This correspondence is, however, quite limited, as described above.

Finally, we discuss the applicability of a Q1DPC waveguide with a modulated unit-cell structure. Please refer to the 'H' symbol in Figures 20.4 and 20.5. At the frequency denoted by 'H', the fundamental PBG disappears; this characteristic occurs regardless of dimensionality, as seen in Figures 20.4 and 20.5. The value of α at which the fundamental PBG disappears depends on the number of air cavities in the unit cell as seen in the figures. A very narrow transmission mode appears near the frequency denoted by 'H'; it should be noted that the group velocity of the light wave at the frequency denoted by 'H' is very high. Up to this point, the defect mode has been considered for achieving specific mode selection. However, the defect mode has quite a low group velocity because of its nature. It is reasonable to suggest that the transmission mode denoted by 'H' will yield high-speed signal processing of light waves.

A typical example is illustrated in Figure 20.7; this figure, a part of the band structure shown in Figure 20.5(b), shows dispersion curves in the one-dimensional multi-film system with α of 100 nm and 116.9 nm for the four-air-film unit cell structure. When $\alpha = 116.9$ nm, the PBG vanishes and a single transmission mode labeled 'H' is created. It is obvious that the light wave denoted 'H' has a much higher speed than the defect mode in general. The transmission coefficient dependence on frequency for the Q1DPC waveguide is shown Figure 20.8 for $\alpha = 100$ nm and 110 nm. Each curve is taken from Figure 20.5(a). When $\alpha = 110$ nm, as seen in Figure 20.8, the light wave labeled 'H' is successfully transmitted through the waveguide. However, when $\alpha = 110$ nm, the light wave denoted by 'H' is severely attenuated. This suggests that we can control light wave transmission by locally modulating the photonic crystal structure; an example of this local modulation has already

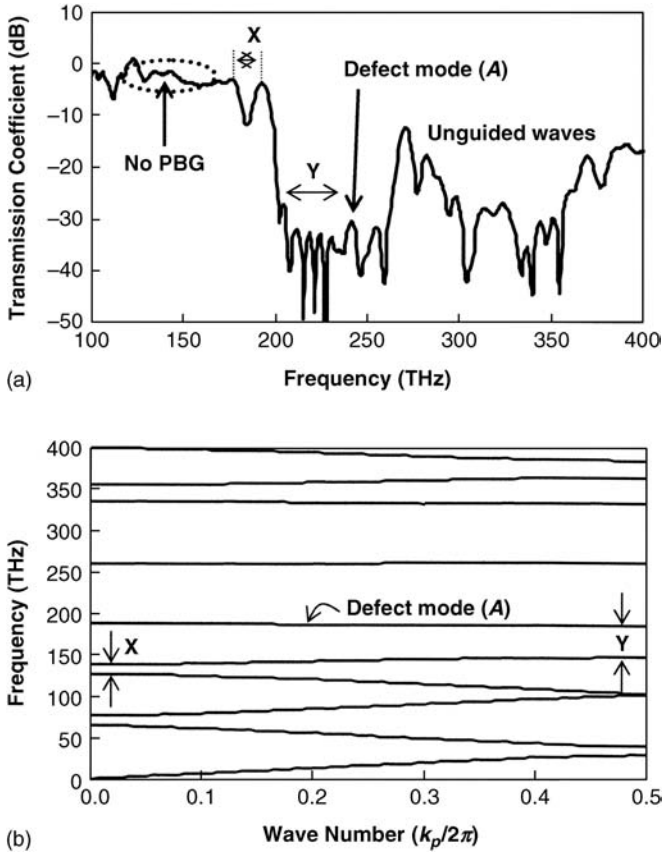

Figure 20.6 Transmission coefficient of waveguide versus frequency and dispersion relation for a multi-layer system. (a) Q1DPC waveguide with a four-air-cavity unit cell and α of 100 nm. (b) Multi-layer with a four-air-film unit cell and α of 100 nm. Reproduced by permission of The Pleiades Publishing, Ltd and Springer. [Y. Ogawa, T Kinoshita, Y. Omura, and Y. Iida, "Photonic band structure and transmission control in quasi-one-dimensional photonic-crystal waveguide with a modulated unit cell structure", *Laser Physics*, vol. 14, pp. 712–719, 2004.]

been proposed [17]. To strengthen the attenuation of the light wave for $\alpha = 100$ nm, we must increase the number of air cavities, which will increase the quality factor of mode selection in the photonic crystal structure.

20.3 Electro-Optic Modulator Based on the SOI Waveguide

The previous section suggests that designing an optical modulator is not easy because the transmission coefficient and the photonic bandgap are sensitive to the Q1DPC's physical parameters. In an attempt to overcome this difficulty, an electro-optic modulator was proposed by Soref and Bennett [18]. Its schematic device structure is shown in Figure 20.9. The p-*i*-n

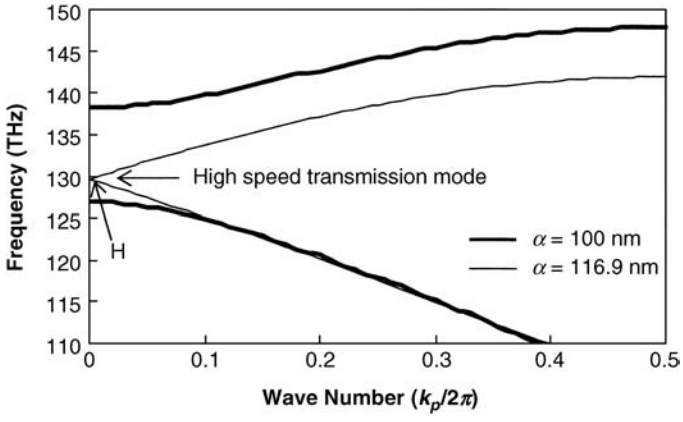

Figure 20.7 Dispersion relations for different α values in the four-air-film unit cell structure. Taken from Figure 20.6(b). Reproduced by permission of The Pleiades Publishing, Ltd and Springer. [Y. Ogawa, T Kinoshita, Y. Omura, and Y. Iida, "Photonic band structure and transmission control in quasi-one-dimensional photonic-crystal waveguide with a modulated unit cell structure", *Laser Physics*, vol. 14, pp. 712–719, 2004.]

diode connected to the waveguide injects electrons and holes into the waveguide and those carriers raise the local refractive index of the waveguide. Since light beam transmission is sensitive to the local increase in the refractive index, the light beam propagation through the waveguide is modulated by activating the p-*i*-n diode.

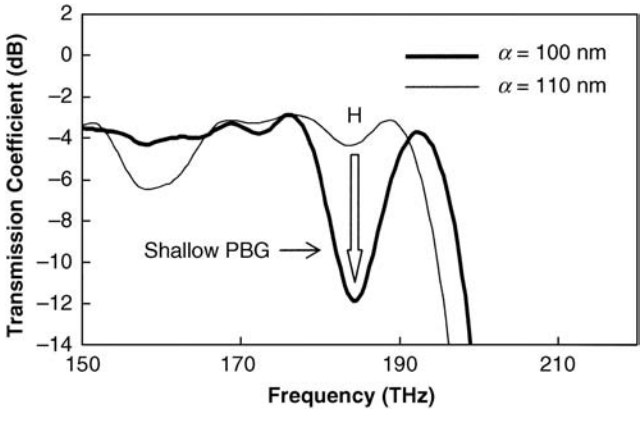

Figure 20.8 Transmission coefficient dependence on frequency for different α values in the Q1DPC wave guide with the four-air-cavity unit-cell structure. Reproduced by permission of The Pleiades Publishing, Ltd and Springer. [Y. Ogawa, T Kinoshita, Y. Omura, and Y. Iida, "Photonic band structure and transmission control in quasi-one-dimensional photonic-crystal waveguide with a modulated unit cell structure", *Laser Physics*, vol. 14, pp. 712–719, 2004.]

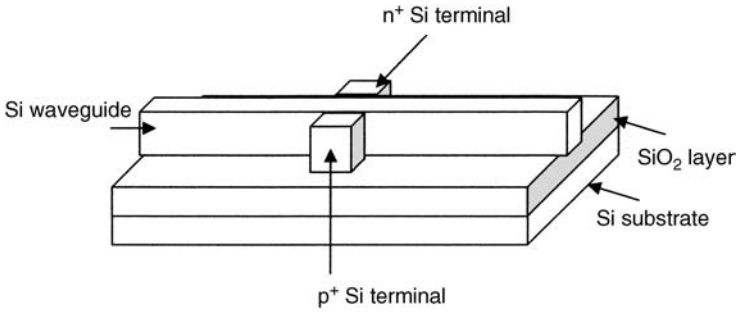

Figure 20.9 Schematic structure of an electro-optic modulator [18].

Soref and Bennett compared their experimental results with the Drude model of crystalline Si (c-Si) [18]. The well-known formulas for refraction and absorption due to free electrons and free holes are as follows:

$$\Delta n = -\left(\frac{q^2\lambda^2}{8\pi^2 c^2 \varepsilon_0 n}\right)\left(\frac{\Delta N_e}{m^*_{ce}} + \frac{\Delta N_p}{m^*_{ch}}\right), \tag{20.1}$$

$$\Delta \alpha = \left(\frac{q^3\lambda^2}{4\pi^2 c^3 \varepsilon_0 n}\right)\left(\frac{\Delta N_e}{m^{*2}_{ce}\mu_e} + \frac{\Delta N_p}{m^{*2}_{ch}\mu_h}\right), \tag{20.2}$$

where q is the electronic charge, λ is the wavelength of the propagating light beam, ε_0 is the permittivity of free space, n is the refractive index of unperturbed c-Si, m^*_{ce} is the conductivity effective mass of electrons, m^*_{ch} is the conductivity effective mass of holes, μ_e is the electron bulk mobility, μ_h is the hole bulk mobility, ΔN_e is the excess electron density, and ΔN_h is the excess hole density. In calculations, they assumed $m^*_{ce} = 0.26\, m_0$ and $m^*_{ch} = 0.39\, m_0$. They found that free holes are more effective in perturbing the index than free electrons. Their experimental results revealed that $10^{-4} < |\Delta n| < 10^{-1}$ for various possible injection conditions.

In recent years, various novel Si-based electro-optic modulators have been proposed and demonstrated [19,20]. The Si ring resonator-based electro-optic modulator was proposed by Xu *et al*. [19] and Zhou and Poon [20]. Past modulators employing a p-*i*-n configuration offer high modulation depth, resulting in relatively slow operation speeds due to the slow injection of electrons and holes in forward-bias operation.

In contrast to the simplicity of the p-*i*-n configuration, the MOS configuration is expected to achieve high-speed operation, of the order of GHz, although the modulation depth is relatively shallow due to the use of the inversion layer. An SOI waveguide electro-optic modulator with an MOS capacitor was demonstrated recently by Kajikawa, Tabei, and Sunami [21]. The waveguide fabricated by these authors is shown schematically in Figure 20.10. The mode of the light propagating through the Si waveguide is modulated by the MOS gate. The original idea had already been proposed by Omura, Iida and Nagayama in 2001 [22], where the use of the majority carrier accumulation layer is assumed because, generally speaking, the accumulation layer is thicker than the inversion layer.

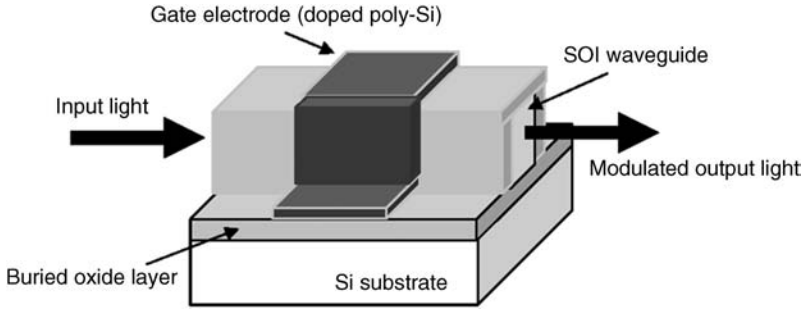

Figure 20.10 Bird's eye view of the Si optical modulator.

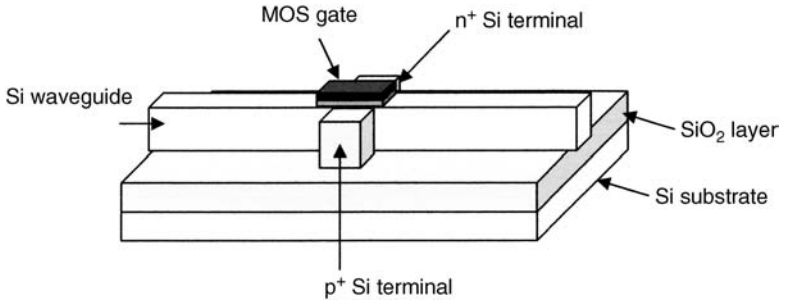

Figure 20.11 Bird's eye view of the Si optical modulator coupled with the Lubistor.

As mentioned above, Xu *et al*. proposed a ring resonator-based electro-optic modulator [19] that utilizes the optical resonance of a micro-ring. This device structure achieves optical transmission at the resonance wavelength, which is quite sensitive to small index changes. As a result, high-speed operation of the modulator was demonstrated; currently this is the most promising technique.

One way of overcoming the shortcomings of the p-*i*-n type modulator shown in Figure 20.9 is shown in Figure 20.11. The Si waveguide is coupled with a Lubistor. The MOS gate can establish an inversion layer or accumulation layer very quickly because the Lubistor has two carrier sources of electrons and holes. Since the carrier sources also work as the drain of the carriers, a very fast response can be expected.

20.4 Summary

The consideration described here strongly suggests that the combination of the SOI Lubistor and the Si waveguide promises a high-speed electro-optic modulator that can be fabricated on an SOI substrate. Since the SOI Lubistor is already applied in various SOI integrated circuits, the SOI electro-optical modulator combined with the SOI LSI is very promising for realizing future optical communication technologies.

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Part Six

SOI Lubistor as a Testing Tool

21

Principles of Parameter Extraction

Bulk pn-junction diodes are often used to derive the ideality factor (n) of the current–voltage characteristic under the forward-biased condition [1]. The experiment is based on the modified Shockley equation described in Part One:

$$I_A = I_S\left\{\exp\left(\frac{qV_A}{nkT}\right) - 1\right\}. \tag{21.1}$$

It is also applied to evaluate the minority carrier lifetime under reverse bias. The experiment is based on the following model [1, 2]:

$$I_R = S_J q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + S_J\frac{qn_iW_d}{\tau_n}, \tag{21.2}$$

with

$$\tau_n = \frac{\sigma_p\sigma_n v_{th}N_t}{\sigma_n\exp\left(\dfrac{E_t - E_i}{k_BT}\right) + \sigma_p\exp\left(\dfrac{E_i - E_t}{k_BT}\right)}, \tag{21.3}$$

where τ_n is the electron lifetime, τ_p is the hole lifetime, W_d is the depletion region width, σ_p is the cross-section of the hole trap, σ_n is the cross-section of the electron trap, N_t is trap density, E_t is the trap level located at the bandgap, and S_J is the cross-sectional area of the junction. It is anticipated that the reverse-biased current characterizes the minority carrier lifetime ruled by the trap energy level and the cross-section of traps.

In the case of an SOI substrate, the I–V characteristics of the pn-junction diode include important information on the generation–recombination process at the gate oxide/Si

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

interface and the Si/buried oxide interface as well as the bulk property of the SOI layer [3,4]. Since the substrate works as the back gate of the device, the substrate bias alters the band bending at the SOI layer/buried oxide interface; the substrate bias easily creates an accumulation of majority carriers, the flat-band state, the depletion region around the interface, and the inversion layer. Since the pn-junction current with the MOS gate is very sensitive to the semiconductor/insulator interface condition, the technique is very convenient for characterizing the interface quality of the MOSFET. Therefore, the SOI Lubistor is a very good testing tool for top-and-bottom interface characterization [3,4].

The leakage current of a reversed-biased SOI Lubistor is basically induced by carrier generation mechanisms. The different regions of the structure wherein carriers are generated may be identified by monitoring the gate (or substrate) voltage as indicative of the leakage current. Figure 21.1 reveals the schematic characteristic of the leakage current in the SOI Lubistor with the p-type body, where a certain substrate bias is applied so that the Si/buried oxide interface holds the flat-band condition or the accumulation condition. When the front gate voltage is lower than the flat-band voltage ($V_G < V_{FB}$), the front surface is accumulated and leakage current I_{R1} is originated from the junction-controlled depletion region. When the front surface is depleted, but not inverted ($V_{FB} < V_G < V_{TH}$), carrier generation prevails in the front depletion region. Once the front gate voltage exceeds the threshold voltage ($V_G > V_{TH}$), the inversion at the front surface eliminates the interfacial generation rate.

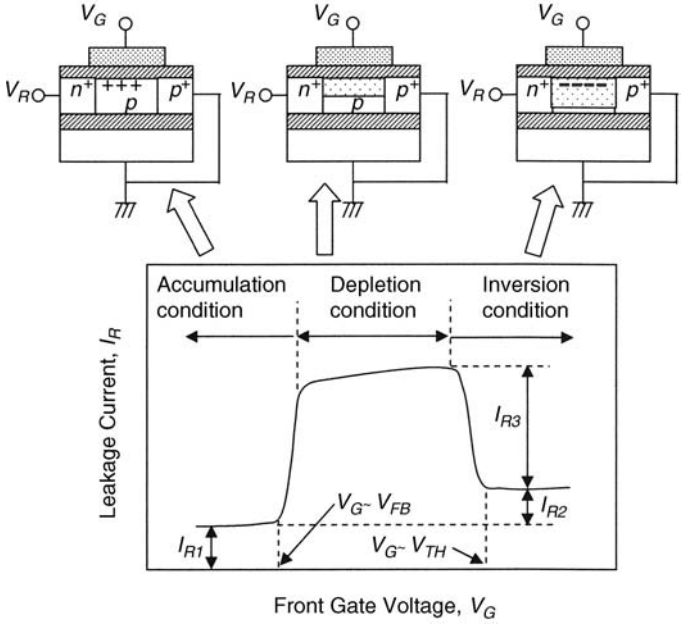

Figure 21.1 Leakage current characteristics as a function of front gate voltage. The SOI Lubistor has the lateral n^+–p–p^+ structure. V_{FB} denotes the front-gate flat-band voltage and V_{TH} denotes the front-gate threshold voltage [4]. Copyright 1995 Springer.

The rise and fall edges of the leakage current characteristic shown in Figure 21.1 represent the flat-band voltage and the threshold voltage, respectively. The slope of the plateau ($V_G > V_{FB}$) reveals the expansion of the gate-controlled depletion region:

$$I_{R2} = \frac{qn_i W_d LW}{2\tau_g}, \tag{21.4}$$

where τ_g denotes the generation lifetime in the depletion region, L the effective channel length, and W the channel width. The excess current (I_{R3}) for $V_G > V_{TH}$ is proportional to the surface generation velocity (S_G):

$$I_{R3} = \frac{qn_i S_G LW}{2}. \tag{21.5}$$

The above description is a fundamental instruction for engineers. Practical techniques to extract various physical parameters are described in detail in References [3] and [4]. Recent progress in measurement techniques using the SOI Lubistor is introduced in detail by Manley [5].

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22

Charge Pumping Technique

22.1 Introduction

This chapter describes the suitability of the charge pumping technique for characterizing the degradation of X-ray irradiated interfaces. We evaluated X-ray-induced degradation and recovery by H_2 annealing of gate SiO_2 film (GOX) and buried SiO_2 film (BOX) of ultra-thin SOI MOSFETs. As expected, various defects are created in the oxide films by X-ray irradiation. Though these defects yield the threshold-voltage shift of MOSFET, it is known that the SOI MOSFET has excellent radiation hardness [1]. The experiments identify interesting aspects of buried-oxide degradation.

22.2 Experimental and Simulation Details

Devices used in this study are fully depleted (FD) SOI MOSFETs fabricated on an SIMOX wafer. Device parameters are shown in Table 22.1, where t_{GOX}, t_{SOI}, and t_{BOX} denote the front-gate-oxide thickness, the SOI layer thickness, and the buried-oxide thickness, respectively. nMOSFET is the inversion-channel device and pMOSFET is the buried-channel device. Integrated X-ray irradiation is 1.0 J/cm^2 and a typical wavelength of X-rays is about 1 nm. Hydrogen annealing is carried out for 30 min at 400 °C.

The experimental setup for front-gate charge pumping is shown in Figure 22.1 and that for back-gate charge pumping is shown in Figure 22.2, where the pulse frequency is basically 10 kHz. It is suggested that the front-gate pulse voltage influences the buried-oxide surface potential; in other words, the charge-pumping current is apt to include the contribution of both front- and back-interface traps [2]. This means that we have effectively to fix the back-surface potential by applying back-gate voltage. We have to fix the front-gate bias when evaluating the buried-oxide interface traps.

The subthreshold slope of the device is given by Reference [3] as

$$S^{w,inv} = \left(1 + \frac{C_{BOX} + C_{DitB}}{C_{Si}}\right) S^{dep}, \tag{22.1}$$

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

Table 22.1 Device parameters

	Values [unit]	
Parameters	nMOSFET	pMOSFET
t_{GOX}	7 [nm]	7 [nm]
t_{BOX}	80 [nm]	80 [nm]
t_{SOI}	50 [nm]	50 [nm]
N_A	3×10^{17} [cm^{-3}]	2×10^{17} [cm^{-3}]
N_{sub}	1×10^{12} [cm^{-3}]	1×10^{12} [cm^{-3}]
Channel width	20.6 [μm]	20.6 [μm]
Channel length	0.7 [μm]	0.7 [μm]

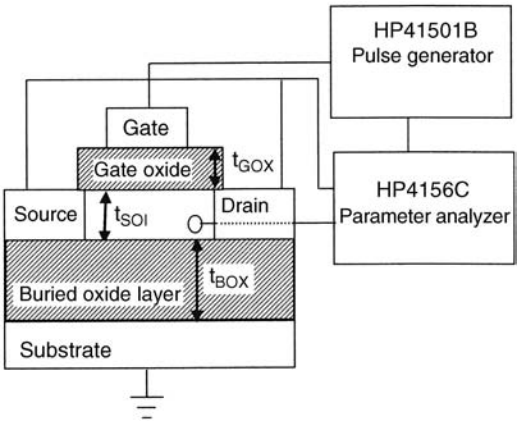

Figure 22.1 Experimental setup for front-gate charge pumping.

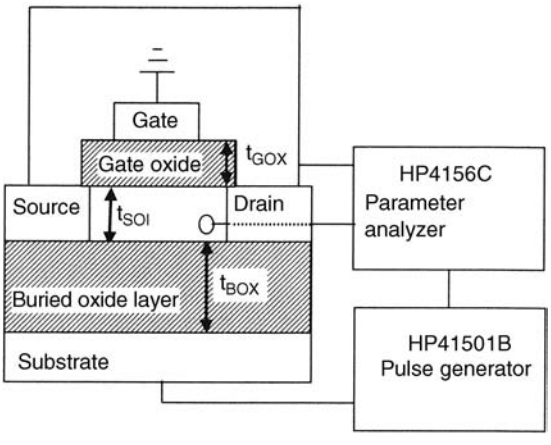

Figure 22.2 Experimental setup for back-gate charge pumping.

where $S^{w,inv}$ is the subthreshold swing at weak inversion, S^{dep} is the subthreshold swing at the depletion condition, C_{BOX} is the buried-oxide capacitance, C_{DitB} is the buried-oxide interface-trap capacitance, and C_{Si} is the SOI-layer capacitance.

22.3 Results and Discussion

Figures 22.3 and 22.4 show the front-gate and back-gate charge-pumping current characteristics measured at 10 kHz, respectively. The post-irradiated devices have larger charge-pumping current than the virgin and H_2-annealed devices, as expected. This indicates that most gate-oxide and buried-oxide interface traps are created by X-ray irradiation [4,5] and that they are almost completely passivated by H_2 annealing.

Figure 22.5 shows the impact of X-ray irradiation and H_2 annealing on the generation and passivation of interface traps. For the nMOSFET, X-ray irradiation increased, by 130 times, the charged trap density (D_{it}) at the gate-oxide/SOI layer interface. On the other hand, D_{it} at the SOI layer/buried-oxide interface was increased 260 times. After H_2 annealing, D_{it} at the gate-oxide/SOI layer interface was reduced to 1/40; however, D_{it} at the SOI layer/buried-oxide interface was reduced to 1/20. This indicates that the buried oxide (BOX) is easily degraded by X-ray irradiation and the difficulty of recovering its property by H_2 annealing.

For the pMOSFET, the X-ray irradiation increased D_{it} at the gate-oxide/SOI layer interface by 110 times. On the other hand, D_{it} at the SOI layer/buried-oxide interface was increased by 400 times. After H_2 annealing, D_{it} at the gate-oxide/SOI layer interface was reduced to 1/60; however, D_{it} at the SOI layer/buried-oxide interface was reduced to 1/300. We can see that the buried oxide (BOX) is easily degraded by X-ray irradiation, but recovers easily with H_2 annealing. The same is not true for the gate oxide.

Figure 22.6 shows the impact of X-ray irradiation and H_2 annealing on subthreshold swing; simple calculation results with D_{it} values (measured at 10 kHz) shown in Figure 22.5 are also shown, where Equation (22.1) was used. It can be seen that the subthreshold swing value of

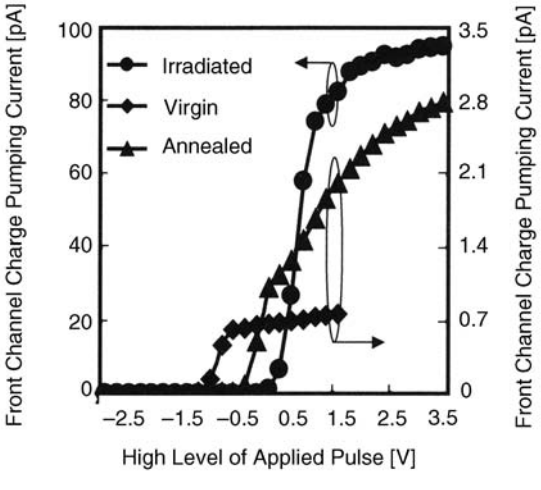

Figure 22.3 Front-gate charge-pumping current curves for virgin, X-ray irradiated, and H_2 annealed devices.

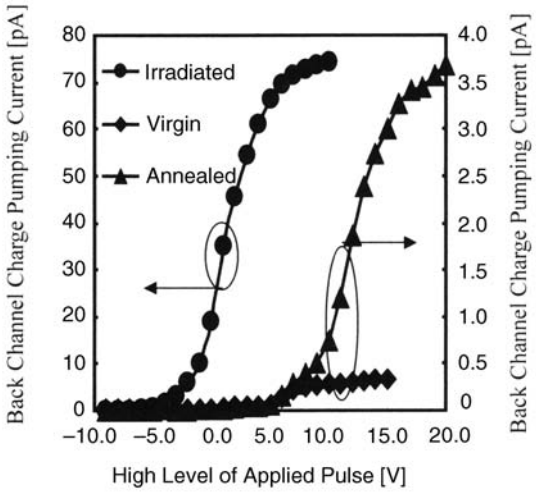

Figure 22.4 Back-gate charge-pumping current curves for virgin, X-ray irradiated, and H_2 annealed devices.

nMOSFET is more easily degraded than that of pMOSFET. Calculation results do not reproduce the subthreshold swing values of post-X-ray-irradiated devices. This suggests that traps are distributed depth-wise in insulators; actually, we found that D_{it} values depend on measurement frequency.

Recombined charge per pulse cycle was extracted from the charge-pumping current (see Figure 22.7), where the pulse frequency was altered. In the low-frequency range, the recombined charge increases rapidly, which suggests that specific traps are created inside the buried oxide by X-ray irradiation. Since the local emission time constant ($\tau_T(x)$) in the buried

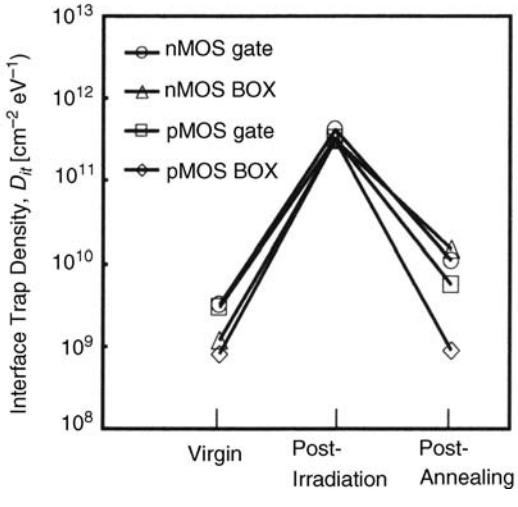

Figure 22.5 Degradation of D_{it} and recovery by H_2 annealing.

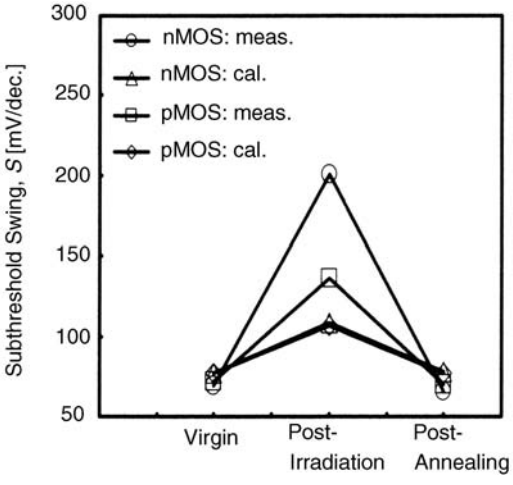

Figure 22.6 Evolution of the subthreshold swing value.

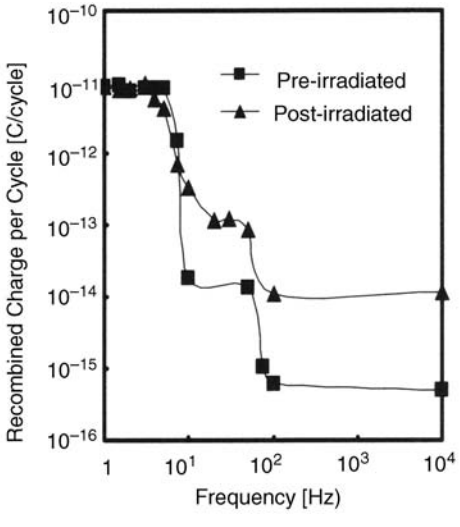

Figure 22.7 Recombined charge per pulse cycle is shown as a function of measurement frequency.

oxide is related to the tunneling of trapped carriers, the effective depth of trap sites can be estimated from the following relation [6]:

$$\tau_T(x) = \frac{m_1^{*2} x\left(1 + \dfrac{1}{2\alpha_1 x}\right)}{\pi^2 2\alpha_2 \hbar^3 D_{it}} \exp(2\alpha_1 x), \tag{22.2}$$

where m_1^* is the effective mass of carriers and α_1 and α_2 are constants. The estimated depths of trap sites are summarized in Table 22.2, where the trap level of $E_c - E_t = 1.5$ [eV] is assumed

Table 22.2 Depths of traps in the buried oxide[a]

	Values [unit]	
Time constant (s)	Before irradiation	After irradiation
0.1	3.1 [nm]	3.8 [nm]
0.01	2.8 [nm]	3.5 [nm]

[a] $m_1^* = 0.3\,m_0$ (electron effective mass in SiO_2), $m_2^* = 0.98\,m_0$ (electron effective mass in Si).

[7]. It can be seen that the pre-irradiated buried oxide has trap depths of 2.8 nm and 3.1 nm, while the post-irradiated buried oxide has trap depths of 3.5 nm and 3.8 nm; the X-ray irradiation appears to have erased the initial traps and created new traps. This is a new finding and reveals the potential of the charge pumping technique.

22.4 Summary

Charge-pumping measurements indicate that buried oxide, but not gate oxide, is easily degraded by X-ray irradiation for both the nMOSFET and pMOSFET. For the nMOS, however, D_{it} of buried oxide is only slightly reduced by H_2 annealing, while for the pMOSFET, D_{it} of gate oxide is only slightly reduced. The experiments demonstrated here strongly suggest that X-ray-induced traps distribute depth-wise in insulators. This indicates that the charge pumping technique is applicable to the interface quality characterization of SOI MOSFETs.

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Part Seven

Future Prospects

23

Overview

23.1 Introduction

The Lubistor is an insulated-gate lateral single pn-junction device. A few scientists including myself have investigated its forward-biased conduction including the tunnel phenomenon [1–4]. The fundamental physics of tunneling in thin-film Lubistors have been extensively studied, with the focus on features of low-dimensional tunneling. It has been revealed in some articles that the band structure of material characterizes the tunneling spectroscopy [1,5–7].

23.2 *i*-MOS Transistor

In 2002, an *i*-MOS transistor with a steep swing was proposed [8]. Avalanche multiplication results in a sharp swing of better than 60 mV/decade; the avalanche condition is controlled by the insulated gate. The device structure is shown schematically in Figure 23.1(a) together with the bias configuration.

Authors state the fundamental conditions allowing the device to exhibit the sharp subthreshold swing [9]:

1. The *amplification* mechanism must be internal to be the device and must arise from some gain mechanism within the device.
2. The devices must not latch up and a fast mechanism like drift, rather than recombination [10], must remove all injected carriers when the device switches from the *ON* to the *OFF* state.
3. Finally, the most fundamental challenge arises from the understanding that there is a finite bandwidth associated with every gain mechanism and, depending on the magnitude of the gain desired, this gain–bandwidth product may impose fundamental limitations on the *intrinsic* device switching speed.

The idea was that impact-ionization would be the gain mechanism that satisfied all of the above conditions. In the *i*-MOS device, as shown in Figure 23.1(b), the p-*i*-n device is reverse

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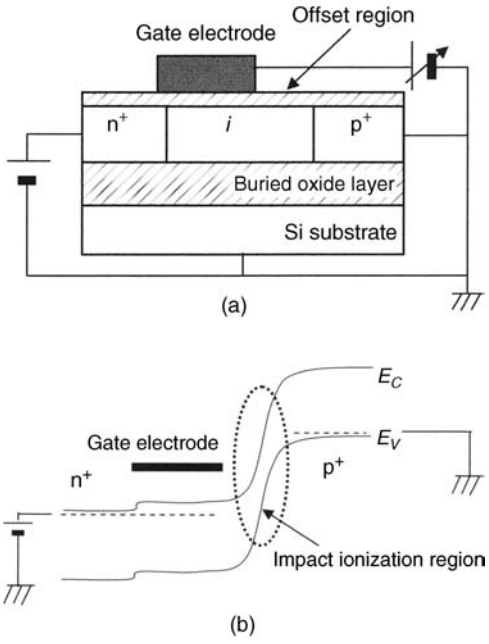


Figure 23.1 Schematic device structure of *i*-MOS transistor: (a) schematic device structure, (b) band diagram.

biased; the insulated gate controls the impact ionization in the depleted *i* region near the p^+ region in this case. The schematic *I–V* characteristic is shown in Figure 23.2.

A sharp swing of 5 mV/dec was predicted from device simulations, which assumed a 25-nm-long gate, 25-nm-long offset length, 1-nm-thick gate oxide, and 25-nm-thick SOI layer [9]. In addition, a sub-1-V threshold voltage was predicted from simulations [9], as shown in Figure 23.2.

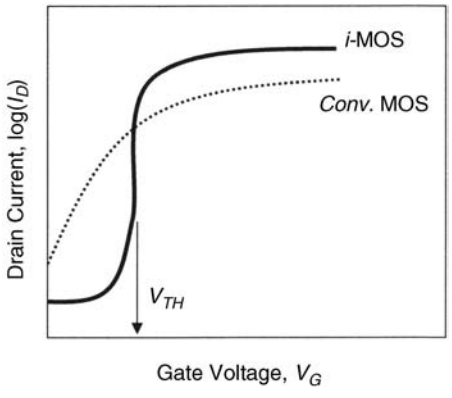


Figure 23.2 Schematic *I–V* characteristics of the *i*-MOS transistor and the conventional MOS transistor.

Si-based *i*-MOS devices were fabricated and tested [11]. No sub-1-V threshold voltage was observed because of the high breakdown voltage of the p-*i*-n diode. The results were very unstable due to the hot-carrier-induced degradation of the gate oxide and the buried oxide. A prediction was made that the Ge-based *i*-MOS might be able to realize sub-1-V operation because its breakdown voltage is less than 1 V [11].

However, it is anticipated that impact ionization will be enhanced in the gate-all-around narrow wire pn junction because the geometric confinement should enhance the electric field normal to the highly doped terminal surface. This mechanism, which enhances local impact ionization, is identical to one that suppresses the short-channel effects of narrow-wire MOSFETs.

23.3 Tunnel FET

In 2004, the tunnel FET (TFET) was proposed, aiming at a steep swing [12,13]. The device structure is basically the same as the Lubistor, as shown in Figure 23.3; strong constraints on the TFET device structure are high doping levels and an abrupt source or drain junction.

The fundamental idea of TFET operation is the reverse-biased conduction of a pn junction; tunneling is controlled by the insulated gate. A schematic view of a typical *I–V* characteristic, obtained experimentally, is shown in Figure 23.4. It should be noted that the steep swing appears only in a very narrow gate voltage range; this is a shortcoming of this device, at least up to now [12–14].

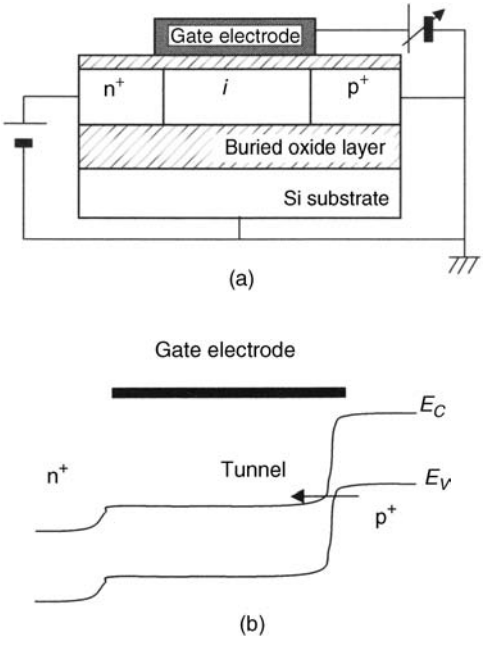


Figure 23.3 Schematic device structure of the tunnel FET: (a) schematic device structure, (b) band diagram.

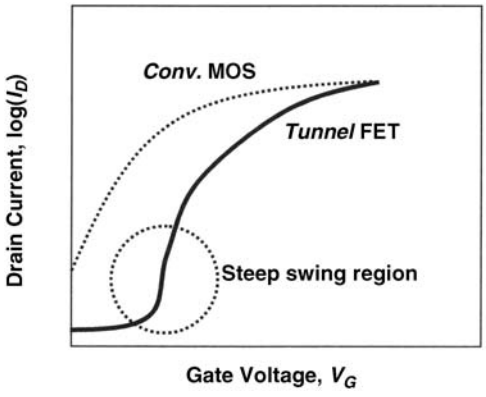


Figure 23.4 Schematic *I–V* characteristics of the tunnel FET and the conventional MOS transistor.

The simulations of Bhuwalka *et al*. predict that thinning the gate oxide will lead to a steep swing [12]. They insert a δp^+ layer adjacent to the p^+ terminal in order to raise the electric field across the *i*-to-p^+ junction [12,13]. They predicted a sub-60-mV/decade swing in Reference [13]. The subthreshold swing formula they propose is given by [14]:

$$S_{Tunnel} = \frac{V_G^2 \ln(10)}{2V_G + B_{Kane} E_G^{3/2}/D}, \tag{23.1}$$

where B_{Kane} and D are constants. This clearly suggests that a low V_G is needed to sharpen the swing, as shown in Figure 23.4 [12–15]. This formula is derived from the band-to-band tunnel (BTBT) current equation by assuming that the drain current (I_D) consists only of the BTBT current (I_{BTBT}). Semiconductor devices operating at room temperature, however, always have a semi-classical thermal generation current (I_{gen}) around the junction:

$$I_D = I_{BTBT} + I_{gen}. \tag{23.2}$$

When $I_{BTBT} > I_{gen}$, Equation (23.2) approximately yields the following modified expression for the swing value:

$$S_{Tunnel}^C \cong \frac{S_{Tunnel}}{1 + S_{Tunnel} \dfrac{d}{dV_G}\left(\dfrac{I_{gen}}{I_{BTBT}}\right)}. \tag{23.3}$$

As

$$\frac{d}{dV_G}\left(\frac{I_{gen}}{I_{BTBT}}\right)$$

takes a negative value, we have $S^{C}_{Tunnel} > S_{Tunnel}$, which is an intrinsic drawback if the device operates at room temperature. In other words, a sharp swing depends on the *purity* of the tunneling process.

In addition to the above consideration, one more issue of the TFET must be pointed out; that is, the gate-induced transversal field enhances or suppresses the reverse-biased tunnel of the junction, which depends on the polarity of the gate voltage. As suggested in Part Three [3,6], when positive bias is applied to the gate on the n^- body of the forward-biased p^+–n–n^+ type Lubistor, the gate overlapped p^+ region near the p^+n junction is depleted and the tunnel area across the junction is reduced, as shown in Figure 23.5(a); this degrades the probability of tunneling across the junction and reduces the tunnel current component across the junction, as

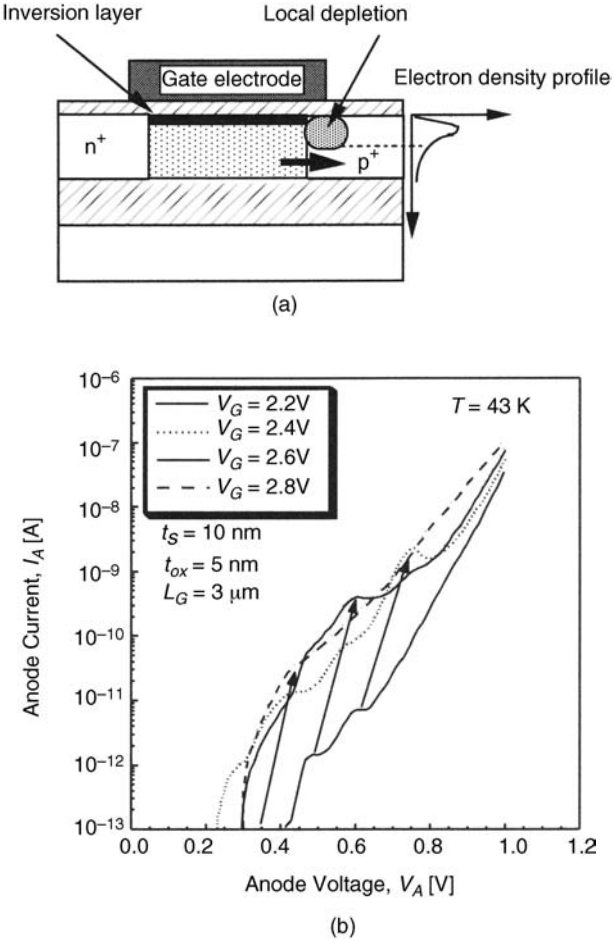


Figure 23.5 Anode current (I_A) dependence on anode voltage (V_A) at 43 K for three different gate voltages (V_G). The silicon layer is 10 nm thick. (a) Local depletion around the pn junction, (b) I_A–V_A characteristics. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-dimensional quantization effect in indirect tunneling in an insulated-gate lateral pn-junction structure with a thin silicon layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

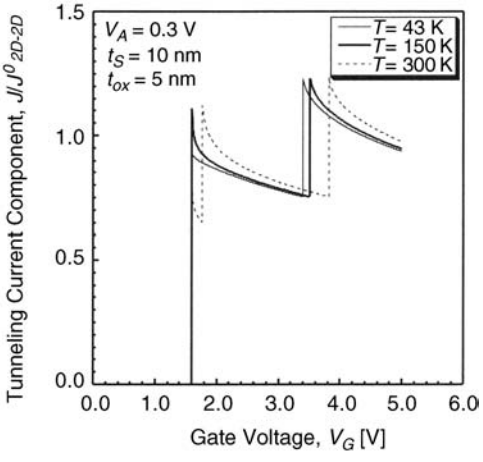


Figure 23.6 Simulated tunneling current component dependence on gate voltage for various temperatures in the device with t_s of 10 nm. It is assumed that the surface threshold voltage is 1.5 V and independent of temperature for simplicity. Copyright 2000. The Japan Society of Applied Physics. [Y. Omura, "Two-dimensional quantization effect in indirect tunneling in an insulated-gate lateral pn-junction structure with a thin silicon layer", *Japanese Journal of Applied Physics*, vol. 39, pp. 1597–1603, 2000.]

shown in Figure 23.5(b). Recently, an advanced TFET device structure was proposed and its performance was predicted by simulations [16]. Although it is not an SOI device, but a bulk device, the mechanism is applicable to an SOI device structure.

The present author's article [6] theoretically considers the tunnel current of the ultrathin Lubistor under the forward-biased condition. The calculation results of tunnel current suggest that a very steep swing is possible, as shown in Figure 23.6, if the tunnel current is well controlled (see Part Three). As the theory simply assumes pure tunneling across the pn junction, the simulation results suggest a high potential of the ultrathin Lubistor. To realize a steep swing, however, Equation (23.3) demands the ideality of the tunnel current regardless of the bias condition of the pn junction.

23.4 Feedback FET

In 2008, the feedback FET was proposed to achieve a steep swing [17]. The device structure is similar to the Lubistor; the geometrical difference from the Lubistor is the underlapped gate electrode of feedback FET as shown in Figure 23.7(a). The feedback FET has gate side walls in gate-offset spaces; SOI body regions under the gate side walls work as an energy barrier to electrons around the source junction (n^+-i junction) and that of holes around the drain junction (i-p^+ junction). When the gate electrode is biased positively, some holes are trapped in the *low energy well* beneath the gate side wall near the source junction and some electrons are trapped in the *low energy well* beneath the gate side wall near the drain junction. Trapped holes lower the potential barrier of electrons near the source junction and trapped holes lower the potential barrier of holes near the drain junction. This results in an abrupt reduction in potential barrier height and an abrupt subthreshold swing (~2 mV/decade). The schematic view of the I–V characteristic is very similar to that shown in Figure 23.2.

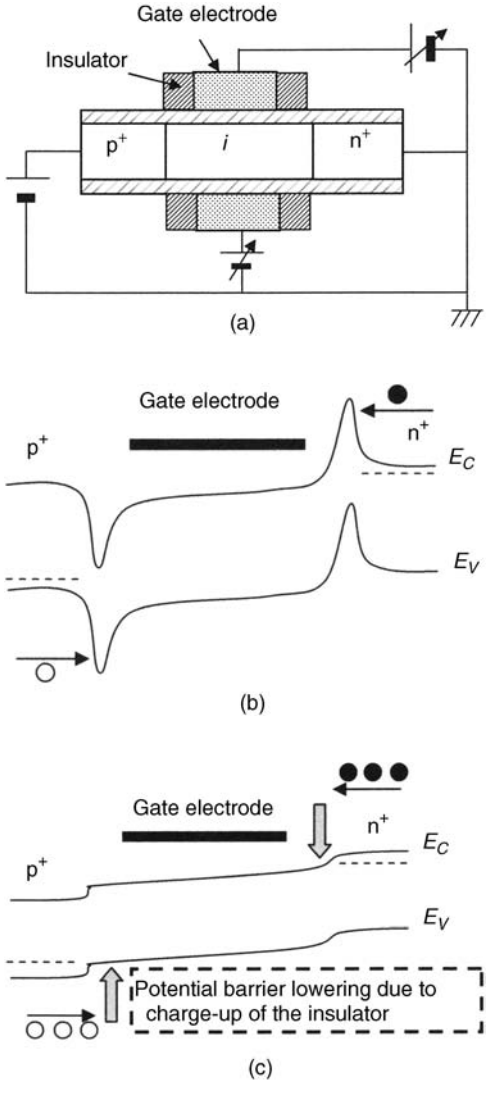
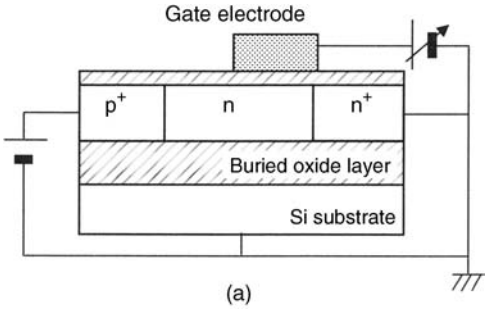


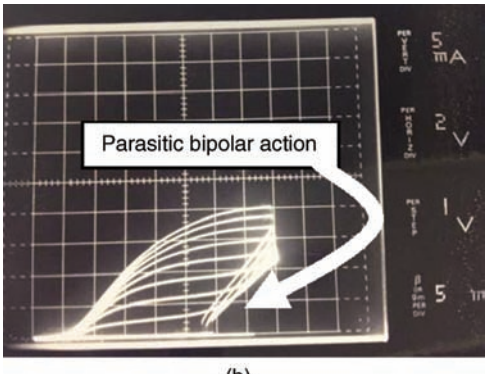
Figure 23.7 Schematic device structure of feedback FET: (a) schematic device structure, (b) band diagram at the *OFF* state, (c) band diagram at the *ON* state.

Transition from the *non-active* state to the *active* state demands that the side wall insulator be charged up [17]. This is not a shortcoming of the device, but the following issues remain:

1. The threshold voltage on the forward sweep is different from that on the reverse sweep.
2. The threshold voltage depends on the drain voltage.



(a)



(b)

Figure 23.8 Schematic device structure of anode-offset-gate Lubistor and *I–V* characteristics: (a) schematic device structure, (b) *I–V* characteristics. (b) Copyright 1982. The Japan Society of Applied Physics. [Y. Omura, "Lateral Unidirectional Bipolar-Type Insulated-Gate Transistors", *Digest Technical Papers, The 14th Conference (1982 International) on Solid State Devices, Tokyo, 1982*, pp. 89–90.]

23.5 Potential of Offset-Gate Lubistor

Primary and important device characteristics and physics of Lubistors were demonstrated and discussed in Parts One to Seven. In this section, I would like to address the potential of the offset-gate Lubistor [18]. The first demonstration of the offset-gate Lubistor with a p^+ poly-Si gate was described in Reference [18], where the p^+–n–n^+ type anode offset-gate Lubistor with the 5-μm-long gate (the n^- region is 10 μm long), the 110-nm-thick SOI layer, 50-nm-thick gate oxide, and 470-nm-thick buried oxide was demonstrated. The schematic device structure is shown in Figure 23.8(a).

The anode offset-gate Lubistor shows conventional pentode-like *I–V* characteristics with the positive bias configuration shown in Figure 23.8(b). Figure 23.8(b) also reveals the positive feedback parasitic bipolar characteristic at around $V_{AK} = 10$ V. Expected band diagrams of the p^+–n–n^+ type anode offset-gate Lubistor are schematically shown in Figure 23.9. This behavior is similar to the feedback FET described in Section 23.3 in this chapter because the n^- region beneath the MOS gate is fully depleted by the p^+ poly-Si gate and the MOS gate controls the hole diffusion in the n^- region beneath the MOS gate. The *OFF* state is realized at a negative gate voltage because of full depletion of the n^- region

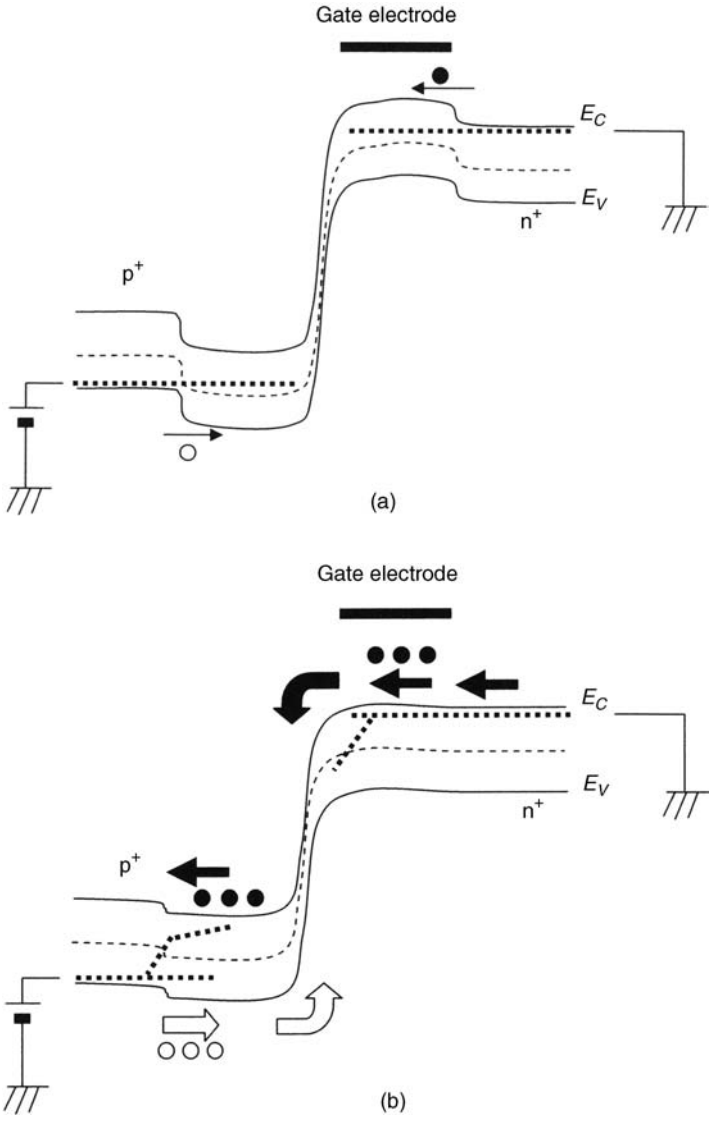


Figure 23.9 Expected band diagrams of p^+–n–n^+ type anode offset-gate Lubistor: (a) *OFF* state, (b) *ON* state.

beneath the MOS gate; the hole injection from the p^+ anode is well suppressed because the n^+ cathode does not supply electrons for hole recombination. When the gate voltage is so positive that an electron accumulation layer is generated in the n^- region beneath the MOS gate, sufficient electrons are supplied by the cathode and the holes can recombine with the electrons. This is the *ON* state. This transition will be sharp because of the bipolar action [19,20].

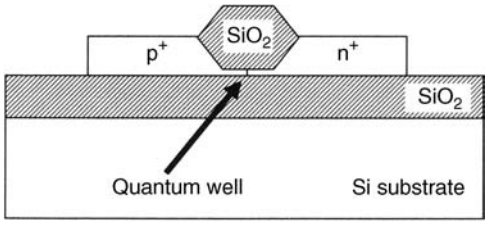


Figure 23.10 Schematic device structure of the Si planar QW LED.

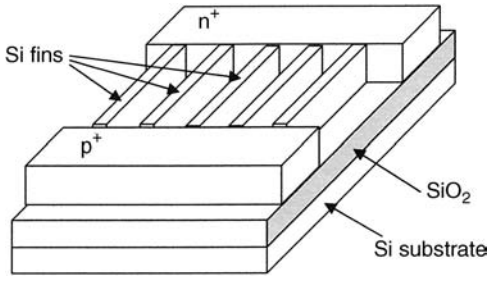


Figure 23.11 Schematic device structure of Si multi-QW LED.

23.6 Si Fin LED with a Multi-quantum Well

Recently, the Si light emitting diode (LED) is attracting attention for realizing optical interconnects on LSI chips. Electroluminescence was observed with lateral carrier injection into the Si planar quantum well (QW) [21]; the cross-section of the device structure is schematically shown in Figure 23.10. In addition, stimulated emissions were observed by embedding the Si QW in a free-standing resonant cavity with distributed feedback structures made of Si_3N_4 and SiO_2 [22]. On the other hand, the pn junction structure on the SOI layer was applied to the Si fin LED [23], where a planar multi-quantum well (MQW) structure suitable for Si technologies was proposed, as shown in Figure 23.11. These devices promise compound-semiconductor-free optical communication systems.

23.7 Future of the pn Junction

The junctionless transistor is drawing attention due to its high potential in future LSI applications [24]. Moreover, we must recall that the pn junction has two highly attractive functions: determining current-flow direction and switching, a basic function for electronic devices. It is anticipated that many kinds of heterojunctions will play important roles in future devices; solar cells and organic electroluminescence devices are likely targets as they need junctions with high performance levels. In 2004, the carbon nanotube pn-junction diode was experimentally demonstrated, where two insulated gates were used to control the polarity of the nanotube [25]. Thus, many kinds of junctions, including the pn junction, will retain their key positions in the electronics industry.

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24

Feasibility of the Lubistor-Based Avalanche Phototransistor

24.1 Introduction

The impact ionization event occurs when high-energy carriers collide with the lattice, which transfers their excess energy to bound electrons in the valence band, promotes electrons into the conduction band, and leave holes in the valence band. This process initiates the avalanche multiplication of carriers. In this chapter, we discuss the avalanche phenomenon of the pn-junction diode.

Impact ionization is commonly referred to as the inverse Auger effect. Impact ionization and the avalanche phenomenon are briefly explained with recourse to Figure 24.1 [1], which illustrates the impact-ionization-based multiplication process of electrons and holes under a high electric field. The basic process is available in direct-bandgap semiconductors because the impact-ionization process is assumed to include the first-order transition [2].

In the 1980s and 1990s, quantum-well-based avalanche photodiodes and photomultipliers attracted attention because of their high quantum efficiency and high multiplication factors [3–8]. A device geometry that offers impact ionization across the band-edge discontinuity of quantum wells is shown in Figure 24.2 [4]. Incident electrons (e.g., optically generated electrons) are accelerated by the external field and collide with the electrons confined in the quantum wells. As expected from Figure 24.2, the ionization rates due to higher level subbands are clearly important because electrons in those subbands are more easily ionized; the avalanche multiplication factor is definitely enhanced. In the following sections, the theoretical basis of the phenomenon is described and performance prospects are addressed.

24.2 Theoretical Formulation of the Avalanche Phenomenon in Direct-Bandgap Semiconductors

In this section, the formulation of the impact ionization of electrons across the conduction band-edge discontinuity in a heterolayer structure (see Figure 24.2) is introduced. First, the transition rate due to electron–electron interaction is discussed. When we assume an incident

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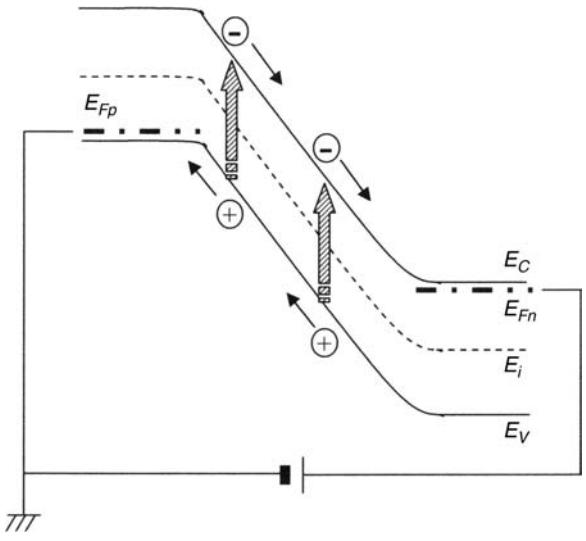

Figure 24.1 Schematic view of avalanche multiplication in the reverse-biased pn junction.

free electron interacting with a bound electron in a quantum well, the total average transition rate per unit volume (P_{tr}) is given by [4,6–8]

$$P_{tr} = \frac{1}{V}\sum_{k_1}\sum_{k_2}\sum_{k_{1'}}\sum_{k_{2'}} P_{k_1k_2}^{k_{1'}k_{2'}} f(k_1)f(k_2)[1-f(k_{1'})][1-f(k_{2'})], \tag{24.1}$$

where $f(k)$ is the Fermi–Dirac function and $P_{k_1k_2}^{k_{1'}k_{2'}}$ is the quantum mechanical transition rate between the initial state of electron '1' in state k_1, electron '2' in state k_2, and the final

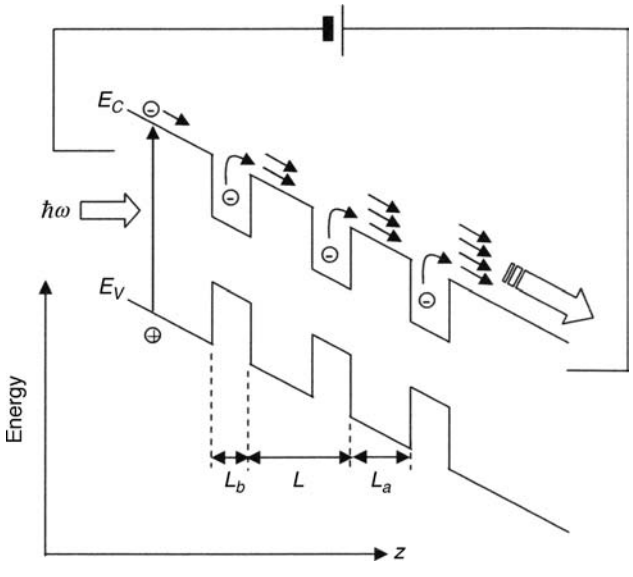

Figure 24.2 A schematic structure of quantum wells exhibiting impact ionization. $L = L_a + L_b$.

state of electron '1' in state k_1' and electron '2' in state k_2' due to the electron–electron interaction [4,6–8]:

$$P_{k_1k_2}^{k_{1'}k_{2'}} = \frac{2\pi}{\hbar}|\langle 12|H_S|1'2'\rangle|^2\delta(E_1 + E_2 - E_{1'} - E_{2'}). \tag{24.2}$$

We can assume that the incident high-energy electron collides with an electron in the valence band, producing two electrons in the conduction band. Since the electron–electron interaction is essentially a two-body collision, we can introduce a screened Coulomb interaction. Thus, the square of the matrix element for the interaction by a screened Coulomb potential is given by

$$|\langle 12|H_S|1'2'\rangle|^2 = 4\left|\int \psi_{k_1}^*(r_1)\psi_{k_2}^*(r_2)\frac{e^2\exp\left(-q_{SC}|r_1 - r_2|\right)}{4\pi\varepsilon_S|r_1 - r_2|}\psi_{k_{1'}}(r_1)\psi_{k_{2'}}(r_2)dr_1dr_2\right|^2, \tag{24.3}$$

where q_{SC} is the screening parameter and e is the electronic charge. In Equation (24.3), '1' and '2' are the electron states before scattering and '1′' and '2′' denote electron states after scattering. It depends on transport dimensionality, and some important points will be discussed in a later section.

Chuang and Hess calculated the average impact ionization rate (the total transition rate per incident electron, P_{tr}/n_0) for an AlGaAs/GaAs heterolayer [4]:

$$P_{tr}/n_0 \cong \int \frac{dk_{0z}}{2\pi}\left(\frac{\pi\hbar^2}{2m_a^*k_BT_e}\right)^{1/2}\exp\left(-\frac{\hbar^2k_{0z}^2}{2m_a^*k_BT_e}\right)\frac{1}{\tau(E_{0z})}, \tag{24.4}$$

$$\frac{1}{\tau(E_{0z})} = \frac{4\pi e^4}{\hbar\varepsilon_S^2}\left(\frac{L_{zn}}{L}\right)^2\int \frac{dk_{2t}}{(2\pi)^2L_{zn}}f(k_{2t})\left[S(k_1, k_{1n}^+) + S(k_1, k_{2n}^-)\right], \tag{24.5}$$

$$S(k_1, k_{2n}^{\pm}) = \frac{m_b^*}{8\pi^2\hbar^2q^2}\frac{\left|k_1 - k_{2n}^{\pm}\right|^2}{\left|k_1 - k_{2n}^{\pm}\right|^2 + q^2}, \tag{24.6}$$

where T_e is the electron temperature, m_a^* is the effective mass of the electron in the conduction band of the wide bandgap material, m_b^* is the effective mass of the electron in the quantum well, and the subscript '0' characterizes the electrons in the wide bandgap material. Vector $\boldsymbol{k_{2t}}$ denotes the wave vector on the k_x–k_y plane, the subscript 'n' denotes the nth subband, and q denotes the wave number of the associated phonon.

Numerical simulation results for the GaAs/AlGaAs heterolayer structure [4] revealed the following features:

1. The impact ionization rate given by Equation (24.5) almost saturates when the energy of the incident electrons is larger than 1 eV.
2. The average ionization rate is sensitive to the doping concentration. It is strongly suggested that it depends on transport dimensionality.

24.3 Theoretical Formulation of the Avalanche Phenomenon in Indirect-Bandgap Semiconductors

To obtain a realistic impact ionization rate formula for the indirect-bandgap semiconductor, Kamakura *et al*. took the local empirical pseudo-potential method for the bulk Si; its validity was verified by comparing simulation and experimental results [9,10]. Impact ionization is an electron–electron interaction process that takes place in a semiconductor under a high electric field, as mentioned in the previous section [11]. A schematic representation of the impact ionization process is shown in Figure 24.3.

The fundamental formulation by Kamakura *et al*. is similar to that in the previous section. They introduced the following expression for the impact ionization rate based on first-order perturbation theory [9]:

$$S_{II}(1,2;1',2') = \frac{2\pi}{\hbar}\left[|M_a|^2 + |M_b|^2 + |M_a - M_b|^2\right]\delta(E_1 + E_2 - E_{1'} - E_{2'}), \tag{24.7}$$

where the sum of spin variables 2, 1′, and 2′ are assumed, and M_a and M_b denote direct and exchange matrix elements, respectively. In calculating the matrix elements, the following Coulomb potential is assumed:

$$V(\boldsymbol{r}_1, \boldsymbol{r}_2) = \frac{1}{V}\sum_q \frac{e^2}{q^2 \varepsilon_S(q,\omega)} \exp\left[i\boldsymbol{q}\cdot(\boldsymbol{r}_1 - \boldsymbol{r}_2)\right], \tag{24.8}$$

where $\varepsilon(\boldsymbol{q},\omega)$ is the frequency- and wave-vector-dependent dielectric function, and $\boldsymbol{r}_1$ and $\boldsymbol{r}_2$ are the local coordinates of two carriers.

They compared simulation results to past experimental results and obtained the best fitted curve given by [9]

$$S_{II}(E) = 1.0 \times 10^{11}(E - 1.1)^{4.6}. \tag{24.9}$$

The large exponent of 4.6 is obtained instead of 2.0 that is expected from the Keldysh formula, which indicates a soft threshold of impact ionization [12].

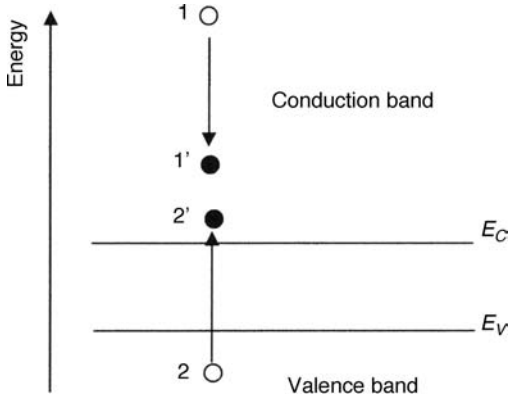

Figure 24.3 Schematic view of an impact ionization process: '1' and '2' are the electron states before scattering, '1′' and '2′' denote electron states after scattering.

24.4 Theoretical Consideration of the Avalanche Phenomenon in a One-Dimensional Wire pn Junction

It is suggested that impact ionization depends on transport dimensionality in Section 24.2. Although one-dimensional transport is expected in a wire pn junction with nano-scale width, the electronic states (represented by a momentum, p) of carriers need to have large uncertainty in terms of Δp. This suggests that coherency of electronic states of carriers is usually apt to be degraded during traveling from either electrode of the carrier source to the counterpart electrode when ballistic transport [13,14] is discussed. Therefore, we must assume *single subband transport* without change of the subband index for a certain bias condition, where we can minimize the elastic scattering event so that the fraction of ballistic electrons is high.

A schematic band structure and a physical picture of conduction in a wire pn junction are illustrated in Figure 24.4, where an Si wire pn junction with width of t_S is assumed because it is predicted that the one-dimensional Si has a direct bandgap [15,16]; it is also anticipated that Ge will reveal this property. In Figure 24.4, it is assumed that the wire is geometrically confined along the y and z axes. Notations in the figure are the same as those appearing in Figure 10.9 of Chapter 10 in Part Three. In Figure 24.4(a), we assume that $E_{n2} - E_{n1} \sim E_G + eV_R$, which needs $t_S \sim 2.9$ nm for $V_R = 1$ V using $m^*/m_0 = 0.19$ [17]. To trigger impact ionization, the length of the low-doping region should be less than 10 nm for $V_R = 1$ V.

I will start by introducing a physical picture to formulate the theoretical expression for electron transport. In Figure 24.4, when the doping level of the p^+ region (left side) is high, the electron density is quite low; we can create a situation in which almost no electron is activated in the conduction band. When one photon is absorbed around the edge of the p^+ region, it is expected that one electron is generated in the conduction band (P_{A1}) and the electron is accelerated by the high field toward the n^+ region (right side) (P_{A2}). The hole generated in the p^+ region is automatically thermalized. When the mean-free path is about 10 nm long, the electron will lose almost all its energy after it has obtained the energy of over 1 eV from the field (T_{Gn1}). Here, the mean-free path of about 10 nm must be *designed* so that the impact ionization takes place near the n^+ region. The hole simultaneously generated is accelerated toward the p^+ region; the mean free path of the hole must be larger than 10 nm. Both electrons, the one that has lost energy and the one generated by impact ionization, are accelerated again toward the n^+ region.

Next, I advance to a theoretical consideration on the basis of the above device geometry and device configuration. In order to determine the total impact ionization rate of the material, we must determine the rate at which carriers attain the threshold energy; that is, the total impact ionization rate depends on the transition rate for impact ionization as well as on the survival rate of high-energy carriers. Shockley's lucky electron model is one of the models known to satisfy the above request [18]. The model assumes that impact ionization is mainly due to *lucky electrons* suffering no collisions in attaining the threshold energy [18]. Accordingly, I try below to formulate the impact ionization rate based on the lucky electron theory.

We assume that $1/\tau(E)$ is the scattering probability of a carrier per unit time. This is similar to Equation (24.5). We also define $P(t)$ as the probability of the carrier's not being scattered. The probability that the carrier is not scattered in time dt is expressed as [19]

$$P(t + dt) = P(t)\left[1 - \frac{dt}{\tau(E)}\right]. \tag{24.10}$$

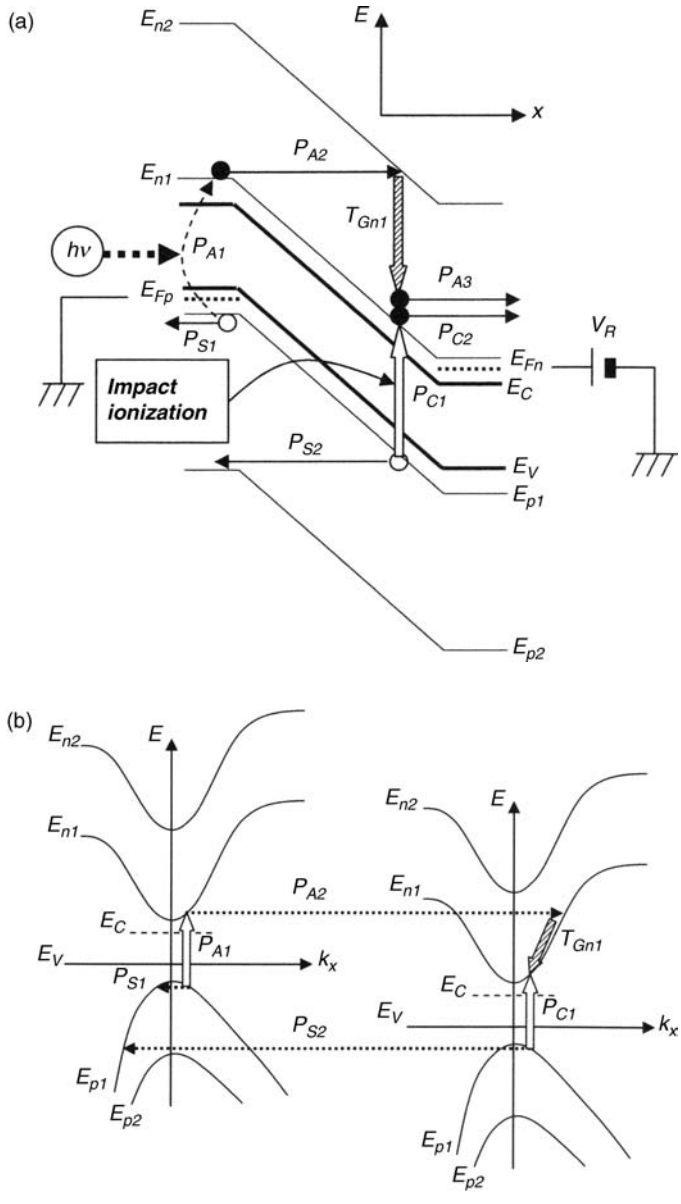

Figure 24.4 Schematic view of an impact ionization and transport processes in the direct-bandgap semiconductor pn junction. P_{C1} shows the impact ionization process, and solid and broken arrows show the ballistic transport from the initial state to the final state without any change of the subband index. (a) Wire pn junction with subbands. (b) Band scheme of local semiconductor with a direct-bandgap semiconductor.

Equation (24.10) yields the following relation because $P(t+dt)$ can be expanded by a power series:

$$P(t_m) = \exp\left[-\int_0^{t_m} \frac{dt'}{\tau(E)}\right], \tag{24.11}$$

where t_m means the mean free time between impact ionization events. $P(t_m)$ is the probability that a carrier will run away without collisions. When a parabolic energy band is assumed, the threshold energy of ionization (E_{th}) is simply expressed as

$$E_{th} = \frac{\hbar^2 k_f^2}{2m^*}, \tag{24.12}$$

where it is assumed that the carrier has no effective energy before ionization occurs, k_f denotes the wave number at which ionization occurs, and $m*$ denotes the effective mass of the carrier. When the carrier starts its drift from the subband edge without collisions (see Figure 24.4(a)), we have

$$k_f = \frac{eFt_m}{\hbar}, \tag{24.13}$$

where F is the electric field. Equations (24.12) and (24.13) yield the mean free time:

$$t_m = \frac{\sqrt{2m^* E_{th}}}{eF}. \tag{24.14}$$

Therefore, the probability that the carrier successfully escapes collisions within time t_m is given by

$$P(t_m) = \exp\left[-\int_0^{E_{th}} \frac{dE}{\tau(E)} \Big/ \frac{dE}{dt}\right]. \tag{24.15}$$

In order to find an expression for the impact ionization rate, we must know the expression of $\tau(E)$. When it is assumed $\tau(E)$ is constant, we have Shockley's expression for the impact ionization rate.

In this section, we assume one-dimensional ballistic transport through a confined semiconductor material, such as an Si crystalline wire. One possible assumption for $\tau(E)$ is

$$\tau(E) = \tau_{00}(E/E_{th})^{-B}, \tag{24.16}$$

where τ_{00} and B are positive constants; this is equivalent to the Keldysh formula [18]. In addition to Equation (24.16), we can assume the following expression for dE/dt:

$$\frac{dE}{dt} = eF\sqrt{\frac{2E(t)}{m^*}}, \tag{24.17}$$

because ballistic transport is assumed. Substituting Equations (24.16) and (24.17) into Equation (24.15), we have

$$P(t_m) = \exp\left[-\frac{\sqrt{m^* E_{th}}}{\sqrt{2}(B+0.5)eF\tau_{00}}\right]. \tag{24.18}$$

This expression is substantially identical to Shockley's model for impact ionization; in other words, Shockley's model is not sensitive to the mechanism of the transition process.

In the device geometry illustrated in Figure 24.4, it is assumed that $E_{th} = 1\,\text{eV}$ and $F = 10^6\,\text{V/cm}$. This yields the mean-free time $t_m = 1.5 \times 10^2\,\text{ps}$ from Equation (24.14). When it is assumed that $\tau(E)$ is constant, we have $P(t_m) = \exp(-2.36)$; this means that the probability that a carrier will escape collision is 0.094. On the other hand, when Equation (24.16) is assumed with $\tau_{00} = 1.5 \times 10^2\,\text{ps}$ and $B = 5$, we have $P(t_m) = \exp(-0.21)$; this means that the probability that a carrier will escape collision is 0.81. As a result, it suggests that we must design the physical parameter so that $\tau(E)$ is basically constant.

From the physics-based point of view, we must also consider how the information of the incident photon is transferred to the electron via the P_{A1} process and how the information of the electron is transferred to the generated electron via the P_{C1} process. Since an inelastic collision usually erases the information of the pre-colliding electron, we must propose a physical mechanism to satisfy the above mandatory condition.

Recently *spintronics* is attracting attention from the viewpoint of low-power electronics and functional devices [20,21]. Therefore, let us consider the ferromagnetic-material-based Schottky junction implemented in the Lubistor; the schematic device structure is shown in Figure 24.5. The MOS-gate-induced electric field changes the spin state of electrons traveling through the channel; this is called the Rashba effect [22,23]. It is known as the spin–orbital interaction in a two-dimensional electron gas [22,23]. Since the relaxation time of the spin–orbital interaction is so long (~10 ns at 300 K [20]), silicon is one of the most promising materials for spintronics applications [20,21]. When an ion silicide is applied to the Schottky junction [21], the photon will be effectively absorbed and the spin state of the generated electron can be specified before its injection into the Si body. The electron will be accelerated

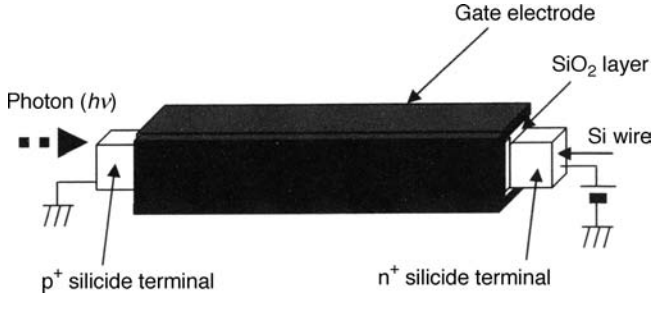

Figure 24.5 Schematic view of the device concept proposed here. A one-dimensional wire Si Lubistor with ion-based silicide Schottky junctions is assumed; the left ion silicide is doped with boron and the right ion silicide is doped with phosphorus. The incident photon will be absorbed at the left side of the device.

till it has threshold energy (E_{th}) before it arrives at the counterpart electrode, and it will lose its energy by the collision, followed by generation of the electron as a result of the impact ionization. The remaining issue is to specify the spin state of the generated electron [24]. This may be possible by the use of an ion-based silicide as the counterpart electrode, but this is a future issue.

24.5 Summary

In this chapter, it was suggested that the Si wire Lubistor based on the one-dimensional transport mechanism is a very promising device for future communication systems. The considerations introduced above must be confirmed in detail by experiments and theoretical simulations. However, I believe that the discussion introduced here will trigger further advances in many other studies. Combined effort will yield better results!

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Part Eight

Summary of Physics for Semiconductor Devices and Mathematics for Device Analyses

25

Physics of Semiconductor Devices for Analysis

25.1 Free Carrier Concentration and the Fermi Level in Semiconductors [1]

GaAs has a single conduction band, while Ge and Si have multiple equivalent conduction bands. Hereafter, we assume semiconductor silicon for convenience. In the intrinsic Si, the average electron density (n) for the single conduction band is theoretically expressed as

$$n = \int_{E_C}^{\infty} D_C(E) f(E) dE, \tag{25.1}$$

where $f(E)$ denotes the Fermi–Dirac function and $D_C(E)$ denotes the electronic density of states of the conduction band per volume. They are expressed as

$$f(E) = \frac{1}{1 + \exp\left(\dfrac{E - E_F}{k_B T}\right)}, \tag{25.2}$$

$$D_C(E) = 4\pi \left(\frac{2m_{dc}^*}{h^2}\right)^{3/2} (E - E_C)^{1/2}. \tag{25.3}$$

Here, E_F is the Fermi level, m_{dc}^* is the density-of-state effective mass of electrons in the conduction band, h is Planck's constant, and E_C is the energy level of the conduction band bottom. Depending on where the Fermi level E_F lies, semiconductors can be classified as either degenerate semiconductors or nondegenerate semiconductors. When the Fermi level is either in the conduction band or in the valence band, the two situations are similar to those in metals, the former corresponding to a metal where we have electron conduction and the latter to a metal where we have hole conduction. These are called degenerate semiconductors.

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

In many semiconductor devices, the nondegenerate semiconductor provides the active region. Therefore, the following description is limited to nondegenerate semiconductors.

For nondegenerate semiconductors, the Fermi level lies somewhat below the conduction band bottom or somewhat higher than the top of the valence band. In many semiconductors, the bandgap energy (E_G) is of the order of 1 eV, whereas k_BT is about 26 mV at room temperature. Thus the condition of $E_C - E_F > k_BT$ suggests that the following approximation is reasonable for Equation (25.1)):

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_BT}\right)} \cong \exp\left(-\frac{E - E_F}{k_BT}\right). \tag{25.4}$$

Using Equation 25.4, from Equation 25.1 we find the electron density of the conduction band to be

$$n = N_C \exp\left(-\frac{E_C - E_F}{k_BT}\right), \tag{25.5}$$

where

$$N_C = 2\left(\frac{2\pi m^*_{dc}}{h^2}\right)^{3/2}. \tag{25.6}$$

N_C is the effective density of conduction-band states. In a similar way, the hole density of the valence band is given by

$$p = N_V \exp\left(-\frac{E_F - E_V}{k_BT}\right), \tag{25.7}$$

$$N_V = 2\left(\frac{2\pi m^*_{dh}}{h^2}\right)^{3/2}, \tag{25.8}$$

where N_V is the effective density of valence-band states and m^*_{dh} is the density-of-state effective mass of holes of the valence band. In the intrinsic semiconductor, we should have $n = p$, so Equations 25.5 and 25.7 lead to

$$pn = (N_V N_C) \exp\left(-\frac{E_C - E_V}{k_BT}\right) = n_i^2, \tag{25.9}$$

or

$$n = p = n_i = (N_V N_C)^{1/2} \exp\left(-\frac{E_G}{2k_BT}\right), \tag{25.10}$$

where n_i is the intrinsic carrier concentration.

25.2 Impurity Doping in Semiconductors [1]

Various impurities are doped into semiconductors in order to change the carrier density. We assume that donors and acceptors are doped into the semiconductor, with respective doping concentrations of N_D and N_A. Since the semiconductor crystalline must remain charge neutral, even after doping, we have

$$n + N_A^- = p + N_D^+. \tag{25.11}$$

Using Equation (25.9), Equation (25.11) leads to

$$n = \frac{N_D^+ - N_A^-}{2} + \sqrt{\left(\frac{N_D^+ - N_A^-}{2}\right)^2 + n_i^2}, \tag{25.12}$$

for n-type semiconductors ($N_D{}^+ > N_A{}^-$). Since $N_D{}^+ \gg n_i$, we have

$$n = N_D^+ - N_A^-. \tag{25.13}$$

In the non-degenerate semiconductor, all the donor and acceptor impurities are expected to be almost completely ionized:

$$N_D^+ \cong N_D \tag{25.14}$$

and

$$N_A^- \cong N_A. \tag{25.15}$$

25.3 Drift and Diffusion of Carriers and Current Continuity in Semiconductors [1]

Combining the drift and diffusion currents yields the total electron current density and the total hole current density:

$$\vec{\boldsymbol{J}}_n = en\mu_n\vec{\boldsymbol{E}} + eD_n\vec{\nabla}n, \tag{25.16}$$

$$\vec{\boldsymbol{J}}_p = ep\mu_p\vec{\boldsymbol{E}} - eD_p\vec{\nabla}p, \tag{25.17}$$

where e is the elementary charge of electrons, and μ_n and μ_p are electron mobility and hole mobility, respectively. In the following description, we use 'e' as the elementary charge of electrons to avoid confusion between the elementary charge and the wave vector. D_n and D_p are the electron diffusion constant and the hole diffusion constant, respectively. Thermal equilibrium yields the Einstein relations:

$$D_n = \frac{\mu_n k_B T}{e}, \tag{25.18}$$

$$D_p = \frac{\mu_p k_B T}{e}. \tag{25.19}$$

Using Equations (25.16) and (25.17), the time-dependent current continuity equations are given by

$$\frac{\partial n}{\partial t} = D_n \nabla^2 n + \mu_n n \vec{\nabla} \cdot \vec{E} + \mu_n \vec{E} \cdot \vec{\nabla} n - \frac{n - n_0}{\tau_n} + G, \tag{25.20}$$

$$\frac{\partial p}{\partial t} = D_p \nabla^2 p - \mu_p p \vec{\nabla} \cdot \vec{E} - \mu_p \vec{E} \cdot \vec{\nabla} p - \frac{p - p_0}{\tau_n} + G, \tag{25.21}$$

where τ_n and τ_p are the electron lifetime and the hole lifetime, respectively. G denotes the carrier generation rate.

25.4 Stationary-State Schrödinger Equation to Analyze Quantum-Mechanical Effects in Semiconductors [2]

In the following, the simplified derivation of Schrödinger's equation is introduced at the stationary state. We start from the differential equation describing classical waves ($\varphi(x, y, z; t)$) with the phase velocity (v) given by

$$\nabla^2 \varphi - \frac{1}{v^2} \frac{\partial^2 \varphi}{\partial t^2} = 0, \tag{25.22}$$

where ∇^2 is the differential operator [3]. Assuming a monochromatic wave, its solution is given by

$$\varphi(\vec{r}, t) = \psi(\vec{r}) \exp(-2\pi i f t). \tag{25.23}$$

When this solution is substituted into Equation 25.22, we have the following equation for $\psi(\vec{r})$.

$$\nabla^2 \varphi - \frac{4\pi^2 f^2}{v^2} \frac{\partial^2 \varphi}{\partial t^2} = 0 \tag{25.24}$$

Here, we use the relation of $v/f = \lambda$ for the propagating wave, so Equation (25.24) is rewritten as

$$\nabla^2 \varphi - \frac{4\pi^2}{\lambda^2} \frac{\partial^2 \varphi}{\partial t^2} = 0. \tag{25.25}$$

Now, quantum mechanics sets $\lambda = h/p$ (relation proposed by de Bloglie) as the representation of momentum (p). Using this relation, we can eliminate λ in Equation (25.25), yielding

$$\nabla^2\varphi - \frac{4\pi^2 p^2}{h^2}\frac{\partial^2\varphi}{\partial t^2} = 0. \tag{25.26}$$

On the other hand, for particles having effective mass m^* in solid-state materials, for example, the total energy, E, at the stationary state is expressed as

$$E = \frac{p^2}{2m^*} + V(\vec{r}\,), \tag{25.27}$$

where $V(r)$ is the potential energy for electrons in solid-state materials. We can eliminate the momentum parameter in Equation (25.26) using Equation (25.27). As a result, we gain Schrödinger's equation at the stationary state:

$$\left\{-\frac{\hbar^2}{2m^*}\nabla^2 + V(\vec{r}\,)\right\}\psi(\vec{r}\,) = E\psi(\vec{r}\,). \tag{25.28}$$

This equation successfully describes both the particle nature and the wave nature of various elementary particles at the stationary state. The mathematical formulation of Schrödinger's equation described here will not be proved formally because no consideration of the Hamiltonian operator is explicitly made. The above derivation procedure for Schrödinger's equation is only to recognize the impact of de Bloglie's concept ($\lambda = h/p$). The appearance of Planck's constant divides the physics; that is, Planck's constant appears only in quantum-mechanical phenomena. In the next section, we consider the time-dependent Schrödinger equation.

25.5 Time-dependent Schrödinger Equation to Analyze Dynamics in Semiconductors [3]

We start by expressing the propagating wave with angular frequency of ω as

$$\varphi(\vec{r}\,, t) = \psi(\vec{r}\,)\exp(-i\omega t). \tag{25.29}$$

Differentiating Equation (25.29) with time, we have

$$-\frac{\partial}{\partial t}\varphi(\vec{r}\,, t) = i\omega\varphi(\vec{r}\,, t). \tag{25.30}$$

de Bloglie proposed the hypothesis that states that a particle with its effective mass and a quasi-particle without its effective mass manifest their wave nature when they have the energy of E:

$$\omega = \frac{E}{\hbar}. \tag{25.31}$$

Equation (25.31) alters the expression of Equation (25.30) to

$$-\frac{\hbar}{i}\frac{\partial}{\partial t}\varphi(\vec{r}\,, t) = E\varphi(\vec{r}\,, t). \tag{25.32}$$

Considering a particle with the effective mass of m^*, we can introduce the Hamiltonian operator $\hat{H}$ for the particle into Equation (25.32):

$$-\frac{\hbar}{i}\frac{\partial}{\partial t}\varphi(\vec{\boldsymbol{r}},t) = \hat{H}\varphi(\vec{\boldsymbol{r}},t), \tag{25.33}$$

where the Hamiltonian $\hat{H}$ has the dimension of energy; it is expressed as

$$\hat{H} = \frac{\hat{p}^2}{2m^*} + V(\vec{\boldsymbol{r}}), \tag{25.34}$$

where $\hat{p}$ is the momentum operator given by

$$\hat{p} = \frac{\hbar}{i}\vec{\nabla}, \tag{25.35}$$

where $\vec{\nabla}$ is the differential vector operator [3]. Equation (25.33) gives the time-dependent Schrödinger equation that is applicable to the analysis of dynamics. Equation (25.29) is one of many solutions for Equation (25.33). When the energy of a particle does not change in the system, we can assume Equation (25.31); this is called the *stationary state*. At the energy stationary state, we can easily find that Equation (25.33) is reduced to Equation (25.28).

25.6 Quantum Size Effects in Nano-Scale Semiconductors

The major characteristics of quantum-mechanical effects are understood by observing distinct energy discretization [3], coherence [3] and interference [4] of propagating waves, resonant tunneling [5–7], energy radiation [8], and other phenomena that can not be described by classical physics; these specific phenomena stem from the wave characteristics of electrons. Since many books provide only a simplified theoretical discussion, many students often feel that these quantum-effect-based phenomena can be observed easily. In practice, however, few phenomena can be experimentally observed at room temperature [6,9].

Most quantum-mechanical effects can only be observed in a low-temperature system because thermal smearing of discrete energy levels and scattering-induced incoherence prevents observation. Here, many of the quantum-effect phenomena observed at low temperatures are briefly discussed [10,11].

When the behaviors of electrons and holes in three-dimensional space are studied, the manifestation of discrete energy eigenvalues is not usually taken into consideration because the structures are much larger than the carrier wavelength and the density of states in a specific allowed band is also very large in practice. That is, electronic states can be assigned continuous values. On the other hand, the conduction channel length and/or the conduction channel width of recent nano-scale MOSFETs and semiconductor wires have reached the sub-10-nm level in laboratory devices. This value approximates the carrier wavelength, so it must be possible to model the *confinement effect* of the material precisely to advance structure design.

The discrete energy levels of carriers are also manifested by confining carriers inside a small semiconductor space; for instance, a semiconductor sandwiched between two

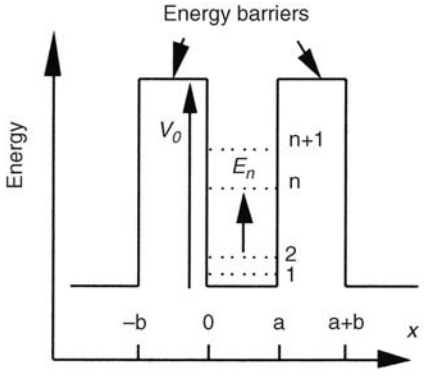

Figure 25.1 Energy barriers and energy quantization ($b > a$) [11]. Copyright 2001 Springer, Chapter 8.

high-energy barriers such as insulators. As an example, we consider the one-dimensional confinement of electrons (see Figure 25.1). Energy eigenvalues and eigenfunctions are obtained by solving the following Schrödinger equation [3]:

$$\left\{-\frac{\hbar^2}{2m^*}\nabla^2 + V_0\right\}\psi_n(\vec{\boldsymbol{r}}) = E\psi_n(\vec{\boldsymbol{r}}), \tag{25.36}$$

where $\psi_n(r)$ is the wavefunction, m^* is the effective mass of bound electrons in the isotropic semiconductor, and V_0 is the barrier height measured from the conduction band bottom of the semiconductor. Since electrons are confined along the x axis, the wavefunction is rewritten as

$$\psi_n(\vec{\boldsymbol{r}}) = \varphi(y,z)\phi_n(x). \tag{25.37}$$

Using Equation (25.37), the Schrödinger equation (Equation (25.36)) is reduced to

$$\left\{-\frac{\hbar^2}{2m^*}\frac{d^2}{dx^2} + V_0\right\}\phi_n(x) = E_n\phi_n(x), \tag{25.38}$$

where E_n is the energy eigenvalue of the bound electrons and is expressed as

$$E_n = E - E_{||}. \tag{25.39}$$

Then

$$E_{||} = \frac{\hbar^2}{2m^*}(k_y^2 + k_z^2), \tag{25.40}$$

where $E_{||}$ denotes the electron energy in the yz plane and k_y and k_z are the wavenumbers along the y axis and z axis, respectively.

Imposing boundary conditions on $\phi_n(x)$ and $d\phi_n(x)/dx$ at the barrier interfaces, the wavefunctions of the nth subband (ϕ_n) are expressed as

$$\phi_n(x) = B_1 \exp(-i\gamma_n x) + B_2 \exp(i\gamma_n x) \qquad (0 < x < a), \tag{25.41}$$

$$\phi_n(x) = A_1 \exp(\beta_n x) \qquad (x < 0), \tag{25.42}$$

$$\phi_n(x) = A_1 \exp[-\beta_n (x - a)] \qquad (x < a), \tag{25.43}$$

$$\beta_n^2 = 2m^*(V_0 - E_n)/\hbar^2, \tag{25.44}$$

$$\gamma_n^2 = 2m^* E_n/\hbar^2, \tag{25.45}$$

where A_1, B_1, and B_2 are constants. The energy eigenvalue (E_n) is given by

$$E_n = E_1 n^2 \left\{ \frac{1}{1 + \left(\frac{2}{\pi}\right)\left(\frac{E_1}{V_0}\right)^{1/2}} \right\}^2, \tag{25.46}$$

$$E_1 = \frac{\hbar^2 \pi^2}{2m^* a^2}. \tag{25.47}$$

Equation (25.46) is derived approximately from Equations (25.41) to (25.45) using the boundary conditions of the quantum well, where the condition of $E_1 \ll V_0$ is assumed. The above equations yield an approximate value of E_n. For $V_0 \to \infty$, Schroedinger's equation must be resolved by setting $A_1 = 0$. In that case, the following well-known solution is obtained:

$$E_n = \frac{\hbar^2 n^2 \pi^2}{2m^* a^2}. \tag{25.48}$$

Simulation results for an SiO_2/Si/SiO_2 system are shown in Figure 25.2, where Equation (25.46) is used. The simulation indicates that we can approximately consider $V_0 \to \infty$ in the SiO_2/Si/SiO_2 system. It is also found that the energy level difference is moderate. In contrast to the silicon system, the infinite barrier approximation is not appropriate for many hetero semiconductor systems. The energy difference is usually smaller than that in the silicon layer with identical width that is sandwiched by two SiO_2 layers. For a system sandwiched by two barriers with infinite height, the energy difference ΔE_n ($=E_{n+1} - E_n$) is given by

$$\Delta E_n = \frac{\hbar^2 (2n + 1)\pi^2}{2m^* a^2}. \tag{25.49}$$

Let us consider that $E_F \sim E_n$. When $\Delta E_n < k_B T$, electrons can easily transit from E_n to E_{n+1} with high probability due to thermal energy [3]. In other words, we cannot assume that the density of electrons occupying energy level E_{n+1} is quite low while that of electrons

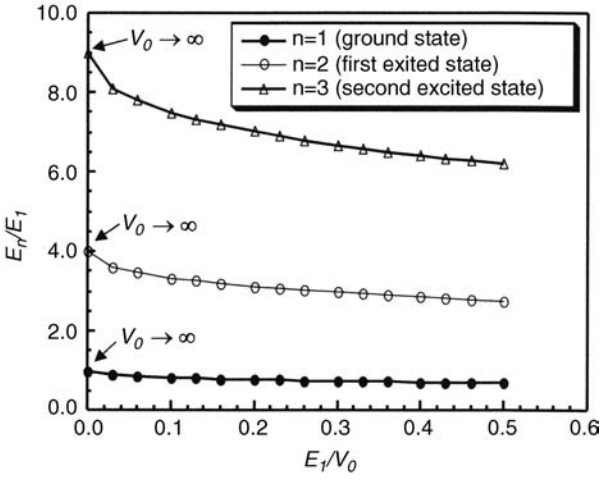

Figure 25.2 Normalized energy values for various states as a function of barrier height. E_1 is the ground state energy and V_0 is the barrier height [11]. Copyright 2001 Springer, Chapter 8.

occupying the energy level E_n is higher. This clearly suggests that the condition of $\Delta E_n \gg k_B T$ is needed to distinguish each quantized energy level of electrons.

25.7 Tunneling through Energy Barriers in Semiconductors

When the tunnel phenomenon is discussed, the theoretical tunnel probability is usually calculated assuming a single energy barrier as shown in Figure 25.3 [3]. When the monochromatic wave with energy (E_k) lower than the barrier height (V_0) approaches the left side of the energy barrier, a part of the wave is reflected at the left side interface of the barrier. The rest of the wave tunnels through the energy barrier with tunnel probability ($T(E_k)$). The tunnel probability in the simplified system shown in Figure 25.3 is given by

$$T(E_k) = \frac{1}{1 + \frac{1}{4}\frac{V_0^2}{E_k(V_0 - E_k)} \sinh\left(\frac{a}{\hbar}\sqrt{2m^*(V_0 - E_k)}\right)}. \tag{25.50}$$

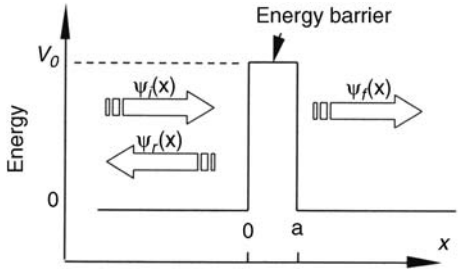

Figure 25.3 Single energy barrier and tunneling through the energy barrier ($E < V_0$).

The tunnel current density (J_T) through the energy barrier can be expressed as

$$J_T = \int T(E_k)[f_C(E_k) - f_V(E_k)]D_C(E_k)D_V(E_k)dE_k, \tag{25.51}$$

where $f_C(E_k)$ and $f_V(E_k)$ are Fermi–Dirac functions for the conduction band and for the valence band, respectively; their form is given in Equation (25.2), where $D_C(E_k)$ and $D_V(E_k)$ denote the density of states of the conduction band and of the valence band, respectively. However, this expression is not convenient in practice for estimating the tunnel current density because integration over the entire density of states is not easy and the assumption is too simple.

In contrast to the above formulation, the tunnel phenomenon of carriers through an energy barrier is frequently expressed using the probability current [3,12]. When the energy barrier stands as shown in Figure 25.3, the current density operator (J_T) along the x axis is expressed by the effective mass approximation as in

$$J_T = \left(-\frac{\hbar^2}{2m^*}\right)\left\{\psi_f^* \frac{\partial \psi_i}{\partial x} - \psi_i \frac{\partial \psi_f^*}{\partial x}\right\}, \tag{25.52}$$

where $\psi_i(x)$ is the wave function of the initial state and $\psi_f(x)$ is the wave function of the final state. Taking the momentum conservation on the barrier surface along the y axis and the z axis, we rewrite Equation (25.52) as

$$M_{i\to f} = \left(-\frac{\hbar^2}{2m^*}\right)\left\{\psi_f^* \frac{\partial \psi_i}{\partial x} - \psi_i \frac{\partial \psi_f^*}{\partial x}\right\}\delta(k_{f,||} - k_{i,||}), \tag{25.53}$$

where $k_{i,||}$ and $k_{f,||}$ are the wave vectors on the energy barrier surface for the initial state and for the final state, respectively. This is the transition matrix element for unconfined electrons that alter their electronic states from the initial state to the final state. This expression of the transition matrix element is very useful in calculating the tunnel current density in low-dimensional electron systems.

25.8 Low-Dimensional Tunneling in Nano-Scale Semiconductors

To assess tunneling in low-dimensional systems, Equation (25.53) must be carefully reconsidered. Here we consider the tunneling phenomenon in a two-dimensional electron system. A schematic configuration of the tunneling path and the electron system is shown in Figure 25.4, where the pn junction is assumed; moreover, the pn-junction film is assumed to be physically confined along the z axis and carrier transport is parallel to the x axis. As suggested in Figure 25.4(b), we can expect many transition paths between the subband of the p-type region and the subband of the n-type region, depending on the Fermi level. Since the Fermi level modulates the tunnel spectra, this configuration is useful when characterizing the band structure of semiconductors.

Probability (P) for a transition between the two states of the two systems on each side of the tunneling barrier is given by Fermi's golden rule [3]:

$$P = \left(\frac{2\pi}{\hbar}\right)\sum_{m,n}\sum_{k_i,k_f} |M_{i\to f}|^2 \{f(E_i) - f(E_f)\}\delta(E_f - E_i - eV_A), \tag{25.54}$$

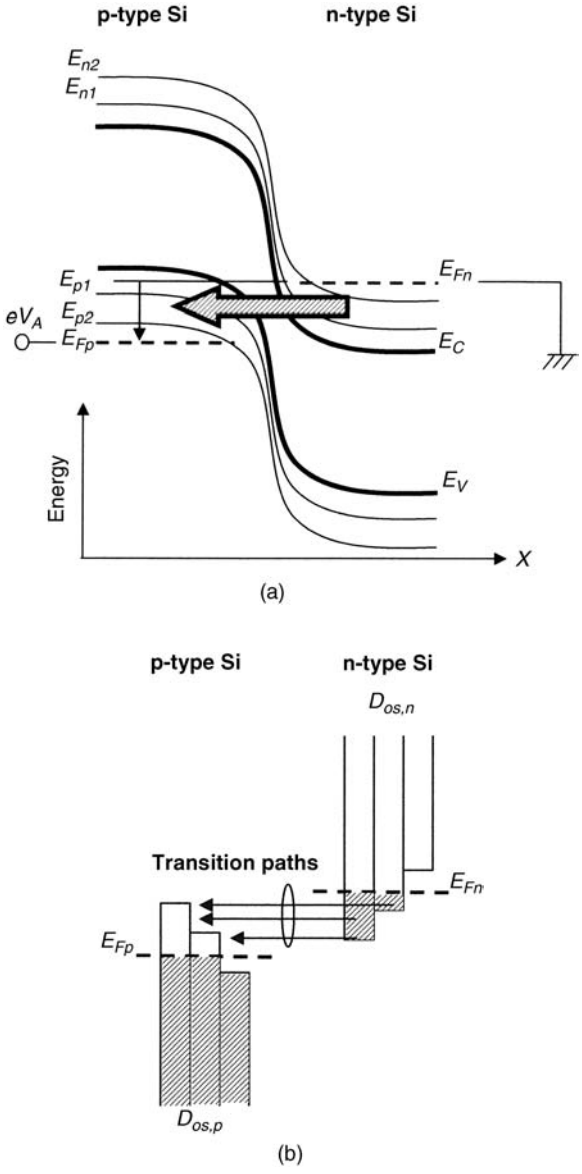

Figure 25.4 Tunnel in forward-biased pn junction consisting of two different two-dimensional semiconductors: (a) band diagram, (b) density of states and possible transition paths.

where the subscripts i and f mean *initial* and *final*, and the δ function represents conservation of the total energy assuming that the applied bias voltage V_A drops partially across the barrier; k_i and k_f denote wave numbers of the initial state and the final state, respectively, and m and n denote subband indices that the initial and the final states are attributed to, respectively.

In the present case shown in Figure 25.4, matrix element $M_{i\to f}$ can be written in terms of the current density operator given by Equation (25.52) [12] such that

$$M_{i\to f} = \left(-\frac{\hbar^2}{2m^*}\right)\left\{\psi_f^* \frac{\partial \psi_i}{\partial x} - \psi_i \frac{\partial \psi_f^*}{\partial x}\right\}\delta(k_{f,y} - k_{i,y})\langle \phi_f | \phi_i \rangle_z, \tag{25.55}$$

where $\psi_i(x)$, $\psi_f(x)$, $\phi_i(z)$, and $\phi_f(z)$ are the components of wave functions in the specific direction. The expression of the transition matrix suggests that tunneling should manifest its one-dimensional nature. In the following description, *i* stands for the electron system and *f* for the hole system.

In the two-dimensional-to-two-dimensional tunneling system, $\langle \phi_f | \phi_i \rangle_z$ has a finite value only for the same quantum number on both sides because identical wave functions represent the *resonance effect* [13,14]. In this condition, incident electrons can tunnel to the anode region after their interaction with phonons. This is a significant feature of such lateral two-dimensional-to-two-dimensional tunneling systems.

In the one-dimensional-to-one-dimensional tunneling system, such as the wire pn junction, Equation (25.55) must be written as

$$M_{i\to f} = \left(-\frac{\hbar^2}{2m^*}\right)\left\{\psi_f^* \frac{\partial \psi_i}{\partial x} - \psi_i \frac{\partial \psi_f^*}{\partial x}\right\}\langle \zeta_f | \xi_i \rangle_y \langle \phi_f | \phi_i \rangle_z, \tag{25.56}$$

where $\xi_i(y)$ and $\xi_f(y)$ are wave function components along the *y* axis. In this condition, incident electrons can also tunnel to the anode region after their interaction with phonons. However, it is anticipated that $\langle \zeta_f | \xi_i \rangle_y \langle \phi_f | \phi_i \rangle_z$ significantly reduces the transition rate between the n-type region and the p-type region because the overlap integral is small due to the limitation of wave function matching. This is a significant feature of lateral one-dimensional-to-one-dimensional tunneling systems. In contrast, it is predicted theoretically that the one-dimensional Si wire has a direct bandgap structure [15,16], which suggests that the transition matrix takes a large value based on the band structure.

25.9 Photon Absorption and Electronic Transitions

25.9.1 Fundamental Formulations

The transition rate for a quantum-mechanical process is generally determined using the time-dependent perturbation theory. The transition rate to first order is given by Fermi's golden rule as

$$W_{i\to f} = \left(\frac{2\pi}{\hbar}\right)\left|\left\langle f\left|\hat{H}'\right|i\right\rangle\right|^2 \delta(E_f - E_i), \tag{25.57}$$

for the time-independent perturbation potential H'. In order to calculate the optical transition rate from Fermi's golden rule, we must evaluate the matrix element $\langle f | H' | i \rangle$ between the initial and the final states. First, we determine the form of H'. The Hamiltonian describing the carrier motion in a semiconductor under a magnetic field is expressed as

$$\hat{H} = \left(\frac{1}{2m^*}\right)(\vec{\boldsymbol{p}} - e\vec{\boldsymbol{A}})^2 + V(r), \tag{25.58}$$

where $\boldsymbol{A}$ is the vector potential associated with the electromagnetic field and $V(r)$ is the periodic crystalline potential. Equation (25.58) is rewritten as

$$\hat{H} = \hat{H}_0 + \hat{H}', \tag{25.59}$$

where

$$\hat{H}_0 = \left(\frac{1}{2m^*}\right)p^2 + V(r), \tag{25.60}$$

$$\hat{H}' = \left(\frac{1}{2m^*}\right)\left[-e(\hat{p}\cdot\vec{\boldsymbol{A}} + \vec{\boldsymbol{A}}\cdot\hat{p}) + e^2\boldsymbol{A}^2\right]. \tag{25.61}$$

The term $\boldsymbol{A}^2$ can usually be neglected in Equation (25.61). When the Coulomb gage ($\vec{\nabla}\cdot\vec{\boldsymbol{A}} = 0$) is taken in Equation (25.61), the first term of Equation (25.61) vanishes, resulting in

$$\hat{H}' = -\left(\frac{e}{m^*}\right)\vec{\boldsymbol{A}}\cdot\hat{p}. \tag{25.62}$$

When a monochromatic incidental wave is assumed, H' is decomposed into the absorption event and the emission event as

$$\hat{H}' = \hat{H}_{ab} + \hat{H}_{em}, \tag{25.63}$$

$$\hat{H}_{ab} = -\left(\frac{eA_0}{2m^*}\right)\exp\,(ik_p r)\vec{\boldsymbol{u}}_a\cdot\hat{p}, \tag{25.64}$$

$$\hat{H}_{em} = -\left(\frac{eA_0}{2m^*}\right)\exp\,(-ik_p r)\vec{\boldsymbol{u}}_a\cdot\hat{p}, \tag{25.65}$$

where $A_0/2$ is the amplitude of the vector potential, k_p is the wave vector of the vector potential, and $\boldsymbol{u_a}$ is the unit vector in the propagation direction. With Equation (25.57), the absorption rate is given by

$$W_{ab} = \left(\frac{2\pi}{\hbar}\right)\left(\frac{e^2A_0^2}{4m^{*2}}\right)\left|\left\langle f\left|\vec{\boldsymbol{u}}_a\cdot\hat{p}\right|i\right\rangle\right|^2\delta(E_f - E_i - \hbar\omega). \tag{25.66}$$

The emission rate is also derived from Equation (25.65) in the similar manner.

25.9.2 Interband Transition – Direct Bandgap

To evaluate the matrix elements, we must choose the wave functions for the initial and the final states. For the band-to-band transition, we assume that the initial and the final states are

Bloch-type wave functions. As momentum $\boldsymbol{p}$ is the operator, we have the following integration form for the matrix element:

$$\langle f|\vec{\boldsymbol{u}}_a \cdot \hat{p}|i\rangle = \int \left[u_{k'}^*(r)\exp\,(-ik'r)\right]\exp\,(ik_p r)u_a\left(\frac{\hbar}{i}\vec{\nabla}\right)[u_k(r)\exp\,(ikr)]d^3r, \tag{25.67}$$

where $u_k(r)$ is the amplitude function (labeled with the electronic state k) representing the Bloch-type nature of the wave function. Equation (25.67) is rewritten as

$$\langle f|\vec{\boldsymbol{u}}_a \cdot \hat{p}|i\rangle = \left(\frac{\hbar}{i}\right)\delta(k-k'+k_p)\int u_{k'}^*(r)\left[\vec{\boldsymbol{u}}_a \cdot \vec{\nabla}u_k(r) + i\vec{\boldsymbol{u}}_a \cdot k\vec{\boldsymbol{u}}_k(r)\right]d^3r. \tag{25.68}$$

The delta function represents momentum conservation at the band-to-band transition. The overlap integrals between two different states ($u_{k'}(r)$ and $u_k(r)$) for different bands vanish because they are orthogonal to each other. In contrast to the former, the first term of integration

$$\int u_{k'}^*(r)\vec{\boldsymbol{u}}_a \cdot \vec{\nabla}u_k(r)d^3r$$

has a finite value as the first-order allowed transition. When the band structure of the material is theoretically determined, we can numerically calculate the integral of Equation (25.68) [17].

25.9.3 Interband Transition – Indirect Bandgap

In elementary semiconductors such as Si, Ge, and C, the crystalline structures exhibit only indirect transitions. They primarily occur in materials in which the conduction band minimum occurs at a point in k space different from the valence band maximum. This transition requires not only energy conservation but also momentum conservation. First, for example, the electron absorbs the photon and makes a transition to an intermediate state within the bandgap. Next, the electron absorbs (or emits) a phonon with a large wave vector and completes the transition to the conduction band. The process can be described physically using second-order time-dependent perturbation theory as [3]

$$W_{i\to f} = \left(\frac{2\pi}{\hbar}\right)\left|\sum_m \frac{\langle f|\hat{H}'|m\rangle\langle m|\hat{H}'|i\rangle}{E_i - E_m}\right|^2 \delta(E_f - E_i + \hbar\omega), \tag{25.69}$$

where the sum over m represents the sum over intermediate states (possible virtual states) between the initial and the final states. The combined probability of photon absorption and phonon absorption is lower than the probability of either event occurring separately; the second-order indirect transition occurs obviously less frequently than the first-order direct transition. This supports the historical fact that indirect semiconductors, such as silicon, are not good materials for detecting optical radiation. However, a recent study suggests that one-dimensional silicon wire should exhibit the direct band transition so that Si-based lasers can be realized [15,16]. In addition, one-dimension silicon wire is also a promising material for spintronics engineering, as discussed in Part Seven.

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26

Mathematics Applicable to the Analysis of Device Physics

26.1 Linear Differential Equation [1]

First we consider the following differential equation:

$$\frac{dy}{dx} + P(x)y = Q(x), \tag{26.1}$$

where $P(x)$ and $Q(x)$ are functions of x. One way to solve Equation (26.1) is to initially set $Q(x) = 0$. This yields

$$\frac{dy}{dx} + P(x)y = 0. \tag{26.2}$$

Separating the variables on either side, we have

$$\frac{dy}{y} = -P(x)dx. \tag{26.3}$$

Next, we have the integration form:

$$\int \frac{dy}{y} = -\int P(x)dx. \tag{26.4}$$

This yields the following tentative solution:

$$y(x) = C_0 \exp\left[-\int P(x)dx\right], \tag{26.5}$$

SOI Lubistors: Lateral, Unidirectional, Bipolar-type Insulated-gate Transistors, First Edition. Yasuhisa Omura.

where C_0 is constant. We assume that the final solution of Equation (26.1) takes the form

$$y(x) = C_0 f(x) \exp\left[-\int P(x)dx\right]. \tag{26.6}$$

When Equation (26.6) is substituted into Equation (26.1), we have final solution

$$y(x) = \exp\left[-\int P(x)dx\right]\left\{\int Q(x)\exp\left[\int P(x)dx\right]dx + C_1\right\}, \tag{26.7}$$

where C_1 is a constant.

26.2 Operator Method

We consider the following differential equation with constant coefficients:

$$\frac{d^2y}{dx^2} + b\frac{dy}{dx} + cy = 0. \tag{26.8}$$

When we define the operator $D = d/dx$, Equation (26.8) is rewritten as

$$D^2y + bDy + cy = 0, \tag{26.9}$$

$$(D^2 + bD + c)y = 0. \tag{26.10}$$

Thus, we consider the following auxiliary equation:

$$D^2 + bD + c = 0. \tag{26.11}$$

The solutions of Equation (26.11), D_1 and D_2, give the final solution in the form of

$$y(x) = C_1 \exp(D_1 x) + C_2 \exp(D_2 x), \tag{26.12}$$

$$D_1 = \frac{-b + \sqrt{b^2 - 4c}}{2}, \tag{26.13}$$

$$D_2 = \frac{-b - \sqrt{b^2 - 4c}}{2}. \tag{26.14}$$

The reason why the solution of Equation (26.8) is given by Equation (26.12) is based on linear algebra.

26.3 Klein–Gordon-Type Differential Equation [2,3]

This is known as a relativistic version of Schroedinger's equation; it is different in that it is second order in time. The equation describes the motion of a quantum scalar or pseudo-scalar field. It is known that a solution to the Dirac equation is also a solution to the Klein–Gordon equation.

The Klein–Gordon equation is generally expressed as

$$\frac{1}{c^2}\frac{\partial^2\psi(r,t)}{\partial t^2} - \nabla^2\psi(r,t) + \frac{m^2c^2}{\hbar^2}\psi(r,t) = 0, \tag{26.15}$$

where c is the speed of light and m is the mass of the particle. For the time-independent case, the Klein–Gordon equation becomes

$$\left(\nabla^2 - \frac{m^2c^2}{\hbar^2}\right)\psi(r) = 0. \tag{26.16}$$

This is called the homogeneous screened Poisson equation. Here we simplify Equation (26.16) to

$$\left(\frac{d^2}{dx^2} - a^2\right)y(x) = 0, \tag{26.17}$$

where a is the real constant. Equation (26.17) can be solved using the operator method described in Section 26.2; that is, we have

$$(D^2 - a^2)y = 0. \tag{26.18}$$

This yields the solution for D:

$$D = \pm a. \tag{26.19}$$

D takes real values. Thus the solution of Equation (26.17) is given by

$$y(x) = C_1\exp(ax) + C_2\exp(-ax). \tag{26.20}$$

This solution consists of decay and divergent functions along the x axis.

Next, we consider the following differential equation.

$$\left(\frac{d^2}{dx^2} + a^2\right)y(x) = 0. \tag{26.21}$$

In a similar way, we have

$$(D^2 + a^2)y = 0. \tag{26.22}$$

This yields the solution for D:

$$D = \pm ia. \tag{26.23}$$

D takes two imaginary values. Thus the solution of Equation (26.21) is given by

$$y(x) = C_1 \exp(iax) + C_2 \exp(-iax). \tag{26.24}$$

The solution expresses the oscillation (wave) function along the x axis.

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